Experimental Test of 3.6 kW Totem-Pole Converter Using State of the Art SiC MOSFETs

Master's Thesis

Benjamin Spragg Sørensen

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Software programs utilized in the report.

1. LTSpice
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Synopsis:

Dette projekt undersøger effektivitetsforbedringen for en eksisterende konverter fra en svejsemaskine udviklet af Migatronic. Effektiviteten forbedres ved at bygge en totempæl-konfiguration kombineret med SiC MOSFET'er. Konverteren er blevet designet, simuleret og eksperimentelt valideret for at vurdere dens ydeevne og effektivitet. For at opfylde Migatronics designkrav er der udført en analyse af komponenttab, konverterkonfiguration og transistorvalg.

Abstract

This project explores the efficiency improvement for an existing converter from a wielding machine developed by Migatronic. The efficiency is improved by building a Totem-pole configuration combined with SiC MOSFETs.
The converter has been designed, simulated, and experimentally validated to assess its performance and efficiency. In order to meet Migatronic's design requirements, an analysis of component losses, converter configuration, and transistor selection has been conducted. Two control systems have been developed on an FPGA development board. The first control system controls the converter in a DC-DC configuration which operates at 100 kHz with a dead-time implemented. Another control system controls the converter in an inverter configuration with the goal of generating a 50 Hz fundamental sine-wave duty cycle with a 100 kHz switching frequency and dead-time implemented. Both controllers are tested in a laboratory setting and have proven performance. In the project, SiC MOSFET C3M0045065K is chosen for the HF leg and C3M0025065K is chosen for the LF leg. A simulation model has been made that estimates the converter's performance. A series of simulations are then conducted. When testing the converter in a DC-DC configuration, the converter is able to boost the voltage to 397 V. The output voltage ripple is measured as $\pm$ 5.85 V and the inductor current ripple is measured to 2.34 A. When testing the converter in inverter configuration, the output voltage and current are a sinusoidal waveform operating at 228.9 V rms and 15.48 A rms with a fundamental frequency of 50 Hz. The simulated efficiency reaches 98.9 %.

The converter has been experimentally validated with a 2-layer PCB. The converter has been tested in a DC-DC configuration. with a switching frequency of 100 kHz. The voltage boosting capability has been tested with various duty cycles. It is shown that the converter is capable of converting different voltage ranges from 39 V up to 415 V. The efficiency is estimated to be 99.1 % at 2.3 kW and estimated efficiency is 99.3% at 3.6 kW. The converter is then tested with an inverter configuration. A 3.3 μF capacitor is added to remove the voltage ripple. The inverter worked correctly and is capable of turning a 329 V DC signal into a 168 V rms sine wave. The estimated efficiency is 98.9 % at 1860 W.

Table 1: Nomenclature of symbols throughout the report.

Nomenclature	
Symbol	**Description**
f_s	Switching Frequency
f_c	Clock Frequency
C	Capacitance
C_{par}	Parasitic Capacitance
L	Inductance
L_{par}	Parasitic Inductance
η	Efficiency
t_r	Rise Time
t_f	Fall Time
R_{on}	On Resistance
R_L	Load Resistor
I_{ac}	AC Current
I_{dc}	DC Current
I_L	Inductor Current
V_{ac}	AC Voltage
V_{dc}	DC Voltage
V_s	Input Voltage
V_f	Forward Voltage
V_{peak}	Peak Voltage
V_o	Output Voltage
V_g	Gate Voltage
V_C	Capacitor Ripple Voltage
V_{rms}	Root-Mean-Square Voltage
P_o	Output Power
P_{Diode}	Diode Power Loss
P_L	Inductor Power Loss
P_{con}	Conduction Loss
P_{sw}	Switching Loss
P_{Cap}	Capacitor Power Loss
D_Q	Duty Cycle
T	Period/Temperature
k_d	Dead Time Ratio
Q_{rr}	Reverse Recovery
c_s	Ratio between clock and switching frequency
N	Counter
ζ	Damping ratio

Table 2: Nomenclature of abbreviations throughout the report.

Nomenclature	
Abbreviation	**Description**
MIG	Metal Inert Gas
TIG	Titanium Inert Gas
$MOSFET$	Metal-Oxide-Semiconductor Field-Effect Transistor
Si	Silicon
SiC	Silicon Carbide
GaN	Gallium Nitride
$GaNFET$	Gallium Nitride Field-Effect Transistors
PFC	Power Factor Correction
LF	Low Frequency
HF	High Frequency
$CrCM$	Critical Conduction Mode
EMI	Electromagnetic Interference
PCB	Printed Circuit Board
$FPGA$	Field-Programmable Gate Array
$VHDL$	Very High Speed Integrated Circuit Hardware Description Language
DCR	DC Resistance
ESR	Equivalent Series Resistance
Q_{rr}	Reverse Recovery Charge
$CrCM$	Critical Conduction Mode
CCM	Continuous Conduction Mode
PWM	Pulse Width Modulation
LF	Low Frequency
HF	High Frequency
LUT	Lookup Table
LFM	Linear Feet per Minute

Preface

Aalborg University, June 20, 2025

This master thesis is written by Benjamin Spragg Sørensen studying at Aalborg University. Simulations on circuit design are done in LTSpice and for the results analysis MATLAB has been used. The illustrations are made in Lucidchart and Microsoft PowerPoint.

The prerequisites for reading the report are a certain knowledge of mathematics, physics, circuit analysis theory, power electronics, semiconductor technologies.

The author would like to thank the supervisor Stig Munk-Nielsen and Tamás Kerekes for instructive guidance as well as constructive criticism. Thanks to Walter Neumayr for helping with the laboratory experiments. Thanks to my parents and girlfriend for their support throughout the project period.

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Introduction

Welding is the process of joining materials together; this usually consists of metals that are fused together using a combination of heat, pressure and a filler material. Up until the end of the 19th century, the only welding method was forge welding, which was predominantly carried out by blacksmiths[1]. This method fused two metals together by heating them up and then hammering the metals together. At the end of the century new methods were developed, such as gas welding, resistance welding and arc welding. These methods quickly became the standard during the 20th century as the demand for faster, cheaper and more reliable ways of joining metals increased.

Gas welding relies on the use of a gas flame as the heat source to melt and join metals. A filler material is typically used to facilitate the fusion process. This method is highly versatile, as it can be applied to a wide range of metal types[1]. However, gas welding will not be discussed further.

Resistance welding and arc welding utilize electrical energy to heat metals. In resistance welding, two metal pieces are clamped together under pressure and exposed to electrical current. The heat generated by the current flowing through the resistive metals causes them to melt at the junction. As the metals cool, they fuse to form a weld. This method is primarily used for joining thin metal plates and does not require any filler material[1].

Arc welding creates an electrical arc between an electrode and the metal surface. The arc generates intense heat that melts the metals, allowing them to fuse. Unlike resistance welding, arc welding uses a filler material that serves as a medium to aid in the fusion process. There are several arc welding techniques, such as stick welding, metal inert gas (MIG), and titanium inert gas (TIG) techniques. Each method offers different advantages depending on the application[1].

An important factor in both resistance and arc welding is the ability to generate high currents, as this is essential to generate sufficient heat for the metals to melt. These currents can typically vary between 50-500 amperes. To generate such currents, it is necessary to reduce the high voltage of the mains supply[1].

Throughout most of the 20th century, welding machines relied on large transformers connected directly to the mains power supply. These high-power transformers operated at the standard 50 Hz frequency and as such required a large core to prevent magnetic saturation. As a result, welding machines were bulky, often weighing several hundred kilograms. They also had poor efficiency and were expensive to buy and operate[5]. By the late 20th century a new generation of welding machine based on converter technology emerged. This new approach replaced the large transformer with converters, consisting of a front end rectifier coupled together with an inverter. The rectifier converted the mains AC signal to DC, which the inverter then converted to a high frequency AC voltage signal in the kilohertz range. The high frequency AC signal allowed for the use of a much smaller transformer as the required core size decreases with increasing frequency[5].

The shift to converter-based technology brought many significant improvements to welding machines. A depiction of two Migatronic welding machines is presented. This consists of an older MTE model from the 1990s and a modern CenTIG model. Both models are TIG type welding machines. Figure 1.1 shows the illustrations of both machines.

(a) Transformer Based MTE Model[15]

(b) Inverter Based CenTig Model [14]

Figure 1.1: Welding machine technology types

Figure 1.1 (a) shows the older MTE welding machine, which operates on a transformer-based design. This machine has a limited duty cycle, which means it can only operate for a portion of a 10-minute period before requiring a cooldown. It is characterized by its large size, heavy weight, and relatively low efficiency[15]. In contrast, Figure 1.1 (b) shows the modern CenTig welding machine. This model utilizes converter technology, which allows it to operate continuously without cooldown periods. It is significantly smaller, lighter, and more efficient compared to the older transformer-based design[14]. A comparison of the models is shown in Table 1.1.

Feature	**Older MTE Model**	**Modern CenTig Model**
Welding Current	220 A	200 A
Duty Cycle	30% (3 minutes on, 7 minutes off)	100% (continuous operation)
Weight	135 kg	13.6 kg
Volume	0.225 m^3	0.0463 m^3
Efficiency	60%	86%
Technology	Transformer-based	Converter-based

Table 1.1: Comparison of older MTE model and modern converter-based welding machine[14][15]

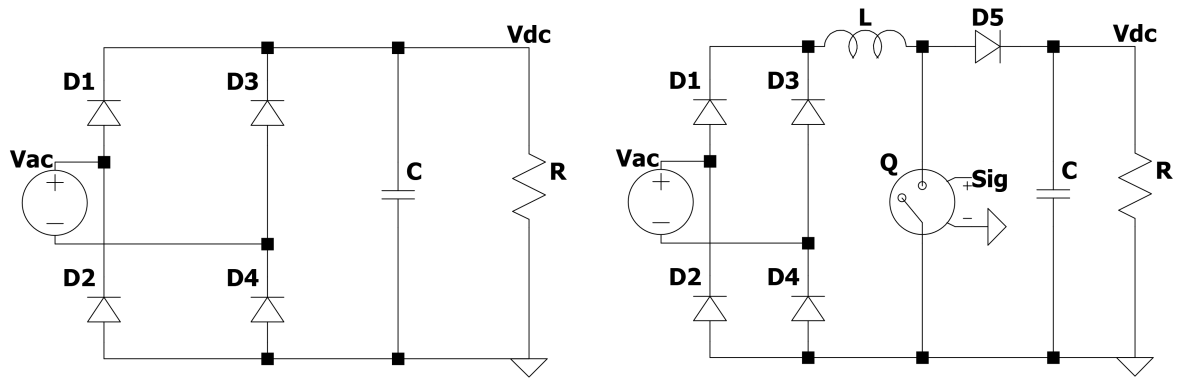
Today, all new welding machines are converter-based, a shift driven not only by technological advancements but also by regulatory requirements. To better understand modern welding machines, it is important to examine the three main circuits that form the core functionality.

1.1 Converter-based Welding Machine

Modern welding machines rely on three key circuits to convert mains power into a controlled output suitable for welding: the PFC rectifier, the high-frequency inverter, and the high-frequency transformer. These circuits work together to meet regulatory requirements, improve efficiency, and enable compact and lightweight designs.[5].

1.1.1 PFC rectifier

The first circuit is the PFC rectifier, whose primary function is to convert the main AC signal to DC, which can then be used by the inverter. The PFC rectifier has other important functions and is required by law. To understand why this is the case, it is helpful to compare its operation with that of a passive diode bridge rectifier. An illustration of each converter configuration is shown in Figure 1.2.



(a) Passive diode rectifier **(b)** Active PFC rectifier

Figure 1.2: Schematic comparison of a passive rectifier with an active PFC rectifier, where R represents the load

In the passive configuration shown in Figure 1.2a, the mains AC supply is connected to a diode full bridge, which converts the AC signal into a DC waveform. A capacitor is connected on the DC side to smooth out the voltage ripple, ensuring stable DC output. The capacitor charges to the maximum voltage of the AC input $V_{DC} \approx V_{peak} = \sqrt{2} \cdot V_{rms}$ and maintains a DC voltage higher than the AC input voltage for most of the cycle. As a result, current can only flow from the mains during the brief intervals when the AC voltage exceeds the DC voltage. This leads to short, high-amplitude current pulses drawn from the grid as shown in Figure 1.3.

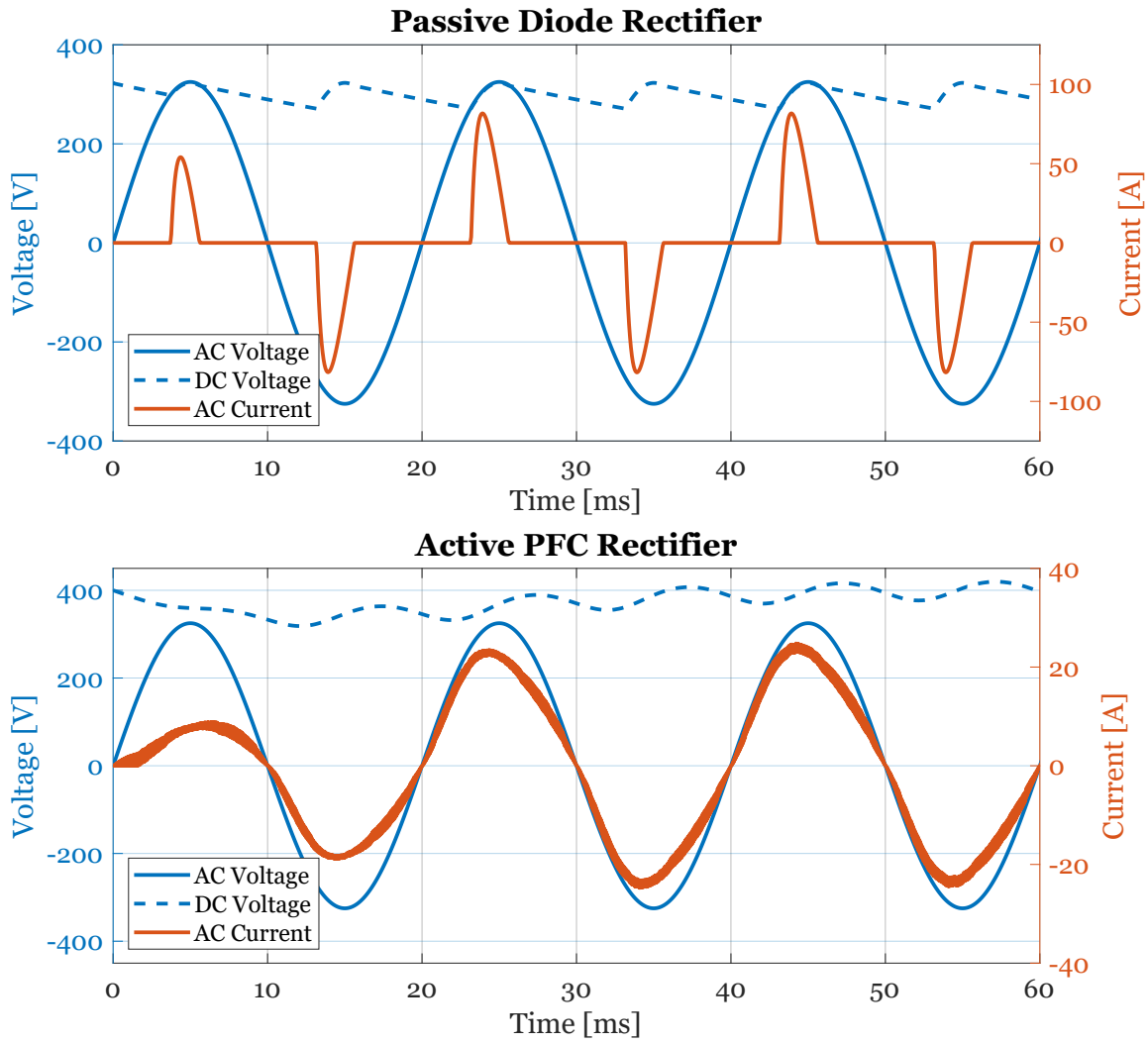


Figure 1.3: Comparison of current waveform of a passive diode rectifier against a PFC rectifier, Initial condition of 325 V DC is included to remove inrush current

Since current can only be drawn during short intervals, the current amplitude reaches nearly 80 A to fully charge the capacitor. However, the current that can be drawn from the grid is much lower than that. This limits the DC output power to a fraction of the 3.68 kW that could theoretically be achieved with a sinusoidal current draw.

The PFC configuration shown in Figure 1.2b adds a DC boost stage between the diode bridge and the smoothing capacitor. This allows the current to be controlled by either charging or discharging the inductor depending on the state of the switch. If controlled correctly, the current can be shaped to follow a sinusoidal curve in phase with the AC voltage as shown in Figure 1.3. This means that power is transferred during the whole AC cycle and the capacitor is continuously charged, because of this the peak current is significantly reduced. This in turn allows more power to be supplied. Additionally, the boost stage also allows the DC voltage magnitude to be higher than the peak voltage of the AC voltage. This is also shown in Figure 1.3, where the average DC voltage is 400 V. Furthermore, because the PFC rectifier shapes the current to follow the voltage, it significantly reduces the introduction of higher-order harmonics. This is shown in Figure 1.4 where the AC frequency spectrum of both rectifiers is compared.

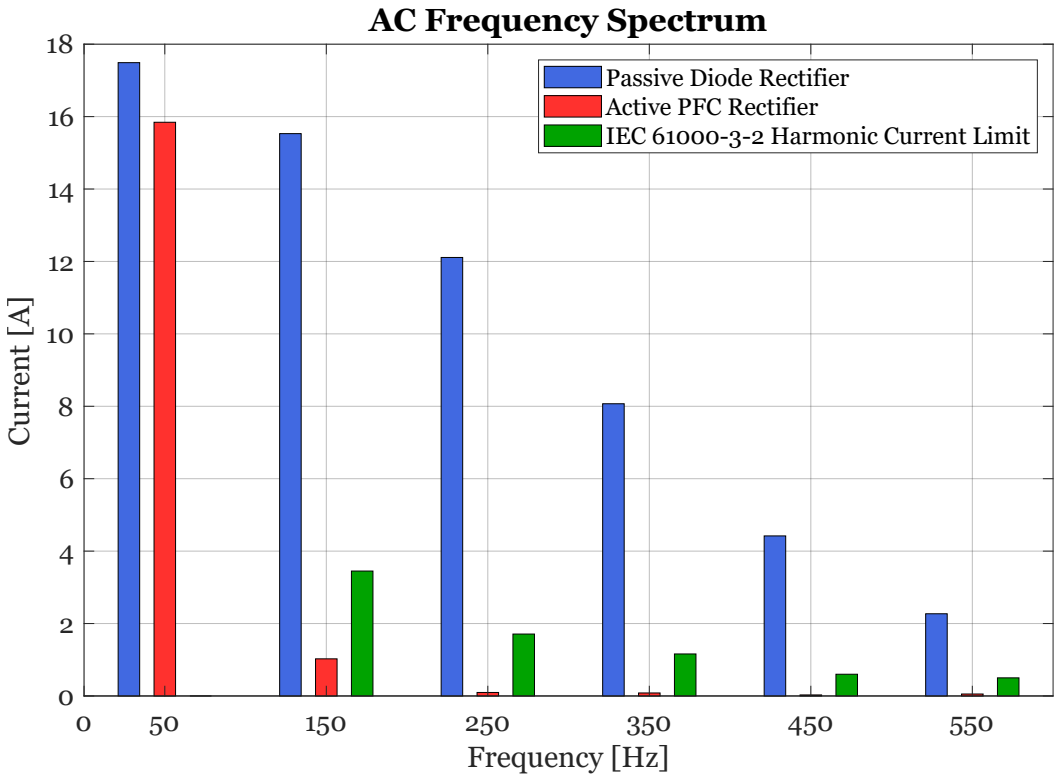


Figure 1.4: Comparison of AC frequency spectrum, showing the fundamental and first five harmonics. The diode Rectifier is above the IEC limit whereas the PFC rectifier is below [2].

As shown in Figure 1.4, the AC current from the passive diode rectifier contains significant harmonic content, with multiple high-order frequency components contributing to the total current. Here, the third harmonic alone is nearly equal to that of the fundamental. This distortion is undesirable, as it degrades power quality and negatively affects the power grid. To prevent this, the IEC 61000-3-2 standard sets regulatory requirements for the amplitude of harmonics in welding equipment. As seen, the AC current exceeds the limits for all harmonics shown in Figure 1.4 and it would not be possible to implement this configuration in commercial welding equipment [2]. In contrast, the PFC rectifier generates substantially lower harmonic content, with higher-order harmonics diminishing rapidly beyond the third, becoming nearly negligible. The amplitude of each harmonic is also lower than the IEC 61000-3-2 limit, and it would therefore meet the requirements of the standard[2].

1.1.2 Frequency inverter

The high-frequency inverter is connected to the output of the PFC rectifier. It converts the DC voltage into a high-frequency AC wave, typically in the range of 30 to 50 kHz[5]. Together, the PFC rectifier and inverter effectively function as a frequency drive by increasing the fundamental frequency from the standard 50 Hz to a much higher value. This increase in frequency allows for a significant reduction in transformer size. This is because the reactance of the transformer is given by $X = 2 \cdot \pi \cdot f \cdot L$, where f is the frequency and L is the inductance. At higher frequencies, the reactance is dominated by the term f, reducing the influence of the inductance L, which is related to the number of windings and the physical size of the transformer core. As a result, a smaller and lighter transformer can be used without compromising performance. A schematic of the inverter is shown in Figure 1.5.

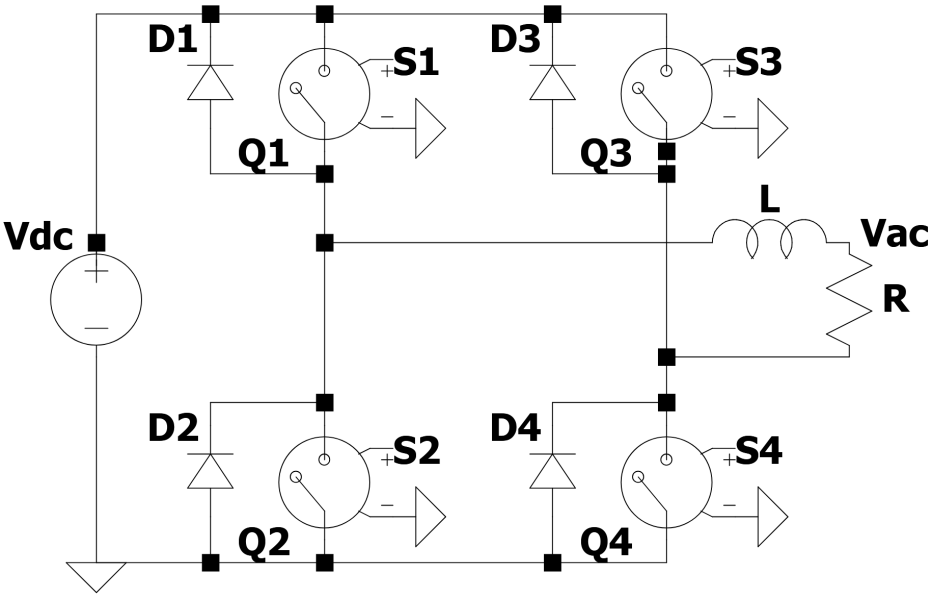


Figure 1.5: A frequency inverter, converting the DC input to a high frequency AC signal

Using the four switches, the inverter can change the DC input into the desired AC waveform, typically this would be a sine or square wave. In addition, the amplitude of the output voltage can be controlled according to the value of the duty cycle. This allows the inverter to control the voltage seen on the transformers output terminals depending on the load conditions and the operator power target. An inverter operating example is shown in Figure 1.6.

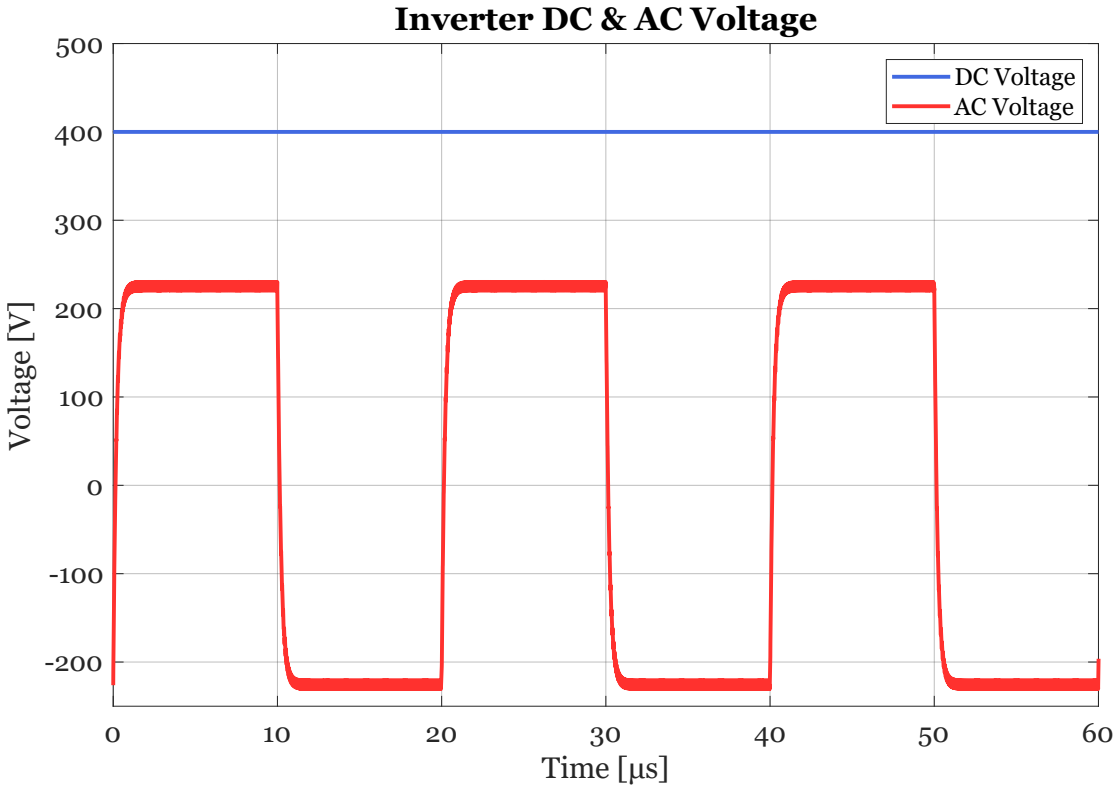


Figure 1.6: Inverter operation, converting a DC signal into a 50 kHz AC square wave.

As shown, a 400 V DC signal is converted into a 50 kHz 230 V AC square wave. This signal is applied across the transformer represented by the inductor L and resistor R in Figure 1.7.

1.1.3 High frequency transformer

At the back end of the system is a high frequency step-down transformer connected to the output of the inverter. This transformer serves several functions. Primarily, it reduces voltage while increasing current, which is necessary to generate the high heat required to effectively join materials during welding[1]. In addition, the transformer improves the stability of the welding arc by compensating for power fluctuations from the supply, ensuring that voltage spikes at the input are not transmitted to the welding arc. This contributes to a more consistent and controlled welding process. The transformer also provides galvanic isolation between the high voltage inverter stage and the low voltage welding terminals, which are exposed and can be touched by the user. This isolation significantly reduces the risk of electric shock and increases operational safety. A schematic of the transformer circuit is shown in Figure 1.7.

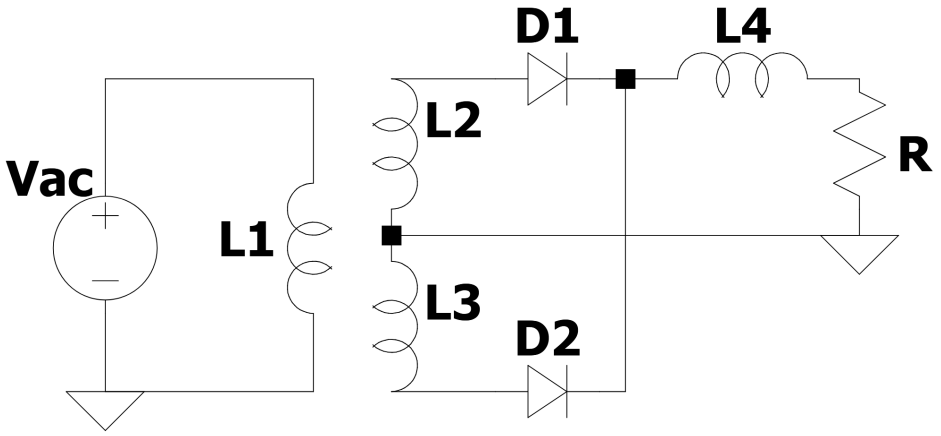


Figure 1.7: A step down center-tapped transformer with secondary side diode rectifier

The secondary side of the transformer is center tapped so that the neutral wire is connected at the midpoint of the secondary winding. Each live wire is then connected to the load through diodes. This rectifies the current such that a DC output is provided between the terminals and the welding materials, represented in the circuit by R. An operational example of an almost ideal transformer is shown in Figure 1.8 where a 230 V 50 kHz square wave is applied to the transformer with a step-down ratio of 9.2.

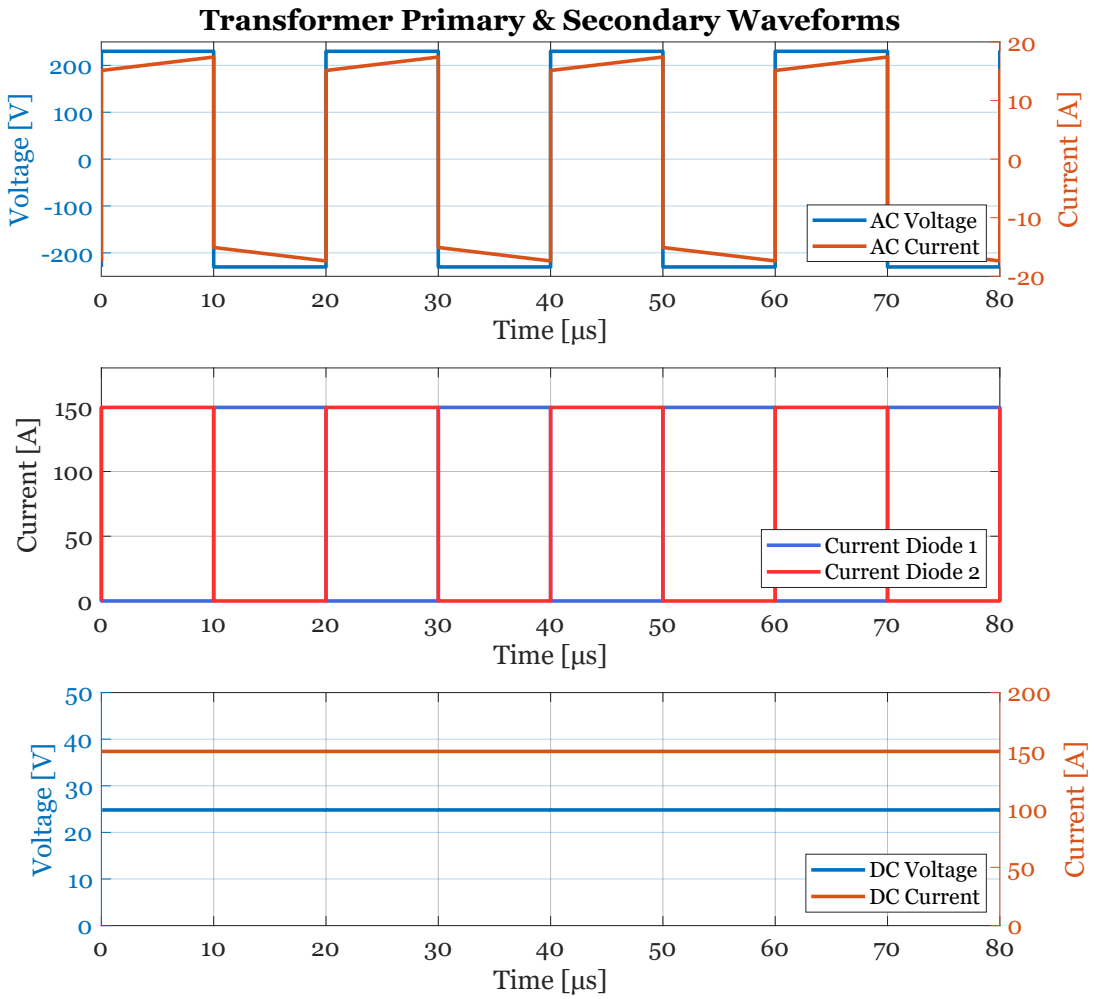


Figure 1.8: Transformer voltage and current signals.

As shown in Figure 1.8 the AC voltage is lowered from 235 V to 25 V. The secondary side voltage is then rectified through the diodes, resulting in a DC signal at the output terminal of low voltage and high current. At this point, the output can now be used for welding.

1.1.4 Improving efficiency in modern welding equipment

One of the goals in the welding industry today is to further improve the performance of each of the three circuits described above. Here, efficiency has been a key driver, as any reduction in power loss and thereby heat generation can improve many aspects of welding equipment, such as production cost, operating costs, equipment size, and system weight. One such company, Migatronic, is looking to improve the design of their existing welding equipment, focusing on their PFC rectifier. Currently, they are looking for new configurations that can improve efficiency over their current design.

To this end, the focus of this project will be examining Migatronic's current PFC rectifier design to identify potential improvements related to efficiency. As a result, the scope of this work will be limited to the PFC rectifier circuit. Although the high-frequency inverter and step-down transformer stages are important to the overall system, they will not be investigated further in this project. In addition, different types of welding methods, such as TIG or MIG, are outside the scope of this project and therefore will not be considered.

Evaluation of Migatronic's Converter and Proposed Improvements

This chapter presents the converter operating requirements set out by Migatronic. A brief presentation of Migatronic's existing converter is also shown. Here, a calculation of the existing converters losses is made in order to identify the main loss generating components. From this a new converter configuration is proposed with the intent to maximize efficiency. Then a comparison of different types of transistor is made with the intention of picking one. From this a problem formulation is then created that outlines the overall goals of the project.

2.0.1 Migatronic Design Requirements

The converter requirements are based on the criteria set out by Migatronic. According to Migatronic the converter should be capable of drawing full power from a single phase, which is equated to 3.6 kW. The output voltage should be 400 V DC with a maximum ripple of $\pm$ 20 V. The maximum current ripple should be between 10-20 %. Finally, the total efficiency of the converter should exceed 97 % at full power.
Assuming that the converter is ideal, the input power is equal to the output power, as such the expected input current can be calculated from the given design parameters as:

$$I_{ac} = \frac{P_o}{V_{ac}} \tag{2.1}$$

This results in an estimated input current of 15.6 A rms. This estimate serves as a reference to determine the rating requirements of the components to be selected. All parameters are listed in Table 2.1.

V_{ac}	230 V
I_{ac}	15.6 A $\pm$ 1.56-3.12 A
V_{dc}	400 V $\pm$ 20 V
P_o	3.6 kW
η	>97 %

Table 2.1: Migatronic PFC converter requirements.

Migatronic currently uses an interleaved bridge PFC rectifier for their single-phase welding machines. This converter consists of two sections, which serve to rectify the current, increase the power factor (PF), and boost the output voltage. A schematic of the PFC rectifier is shown in Figure 2.1.

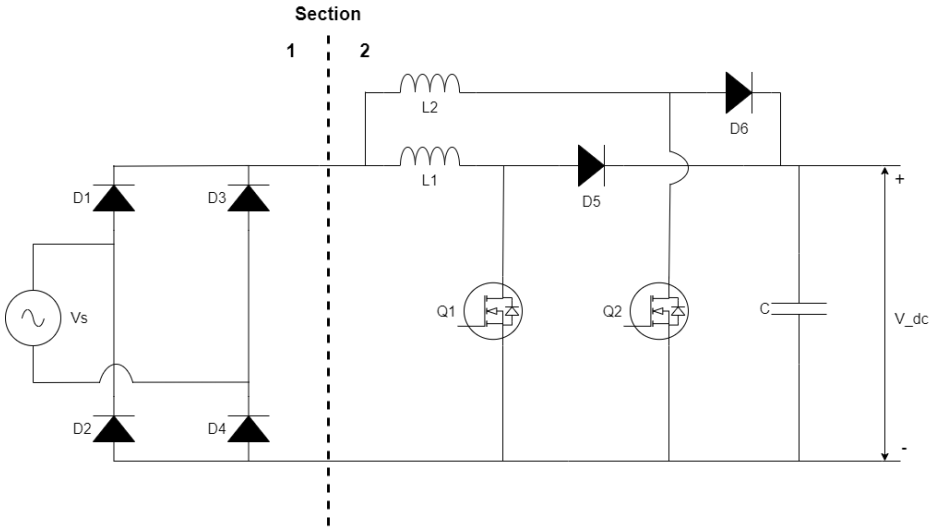


Figure 2.1: Interleaved bridge rectifier

The first section is a diode bridge that rectifies the input current. This is transferred to the second section, which improves the PF and increases the output to 400 V DC. The converter also implements an interleaved design, meaning that two boost converters are connected in parallel. This helps to improve efficiency and reduce component stress by splitting the input current and therefore reducing conduction losses. The two boost sections operation are also phase shifted 180 degrees from each other. As a result, the two currents are also phase shifted 180 degrees, this in turn reduces the ripple current at the output stage.

2.1 Estimation of Converter Component Loss

To estimate the performance of the converter, a loss calculation is performed. The loss calculation is based on data provided by Migatronic where available. For components without supplied data, real components were selected based on datasheet specifications that meet Migatronic converter design requirements. Table 2.2 lists all the components used. Following the schematic of Figure 2.1 from left to right, the component losses are calculated.

Component	Model	Parameter	Value	Unit
SI MOSFET	FCP170N60	R_{on}	175	mΩ
		t_r (Rise time)	12	ns
		t_f (Fall time)	3.8	ns
Rectifier Diode	GBPC3512W	V_f	1.1	V
Schottky Diode	IDV20E65D1	V_f	1.3	V
Inductor	PHBC24N-2R0A0219V	DCR	19.5	mΩ
Capacitor	ALC70(1)821EN600	ESR	163	mΩ

Table 2.2: Overview of chosen components and loss-relevant parameters based on 100 °C operating temperature [4] [18] [7] [13] [11]

The first major losses are seen in the diode bridge, which comes from the forward voltage drop during conduction. Here D1 and D4 conduct for the positive half-cycle, and D2 and

D3 conduct during the negative half-cycle. The total loss seen in the diode bridge can be calculated using Equation 2.2.

$$P_{Diode,slow} = 2 \cdot V_f \cdot I_{ac,rms} \tag{2.2}$$

Next are the inductor losses, where only the resistive losses will be considered. Given that the average inductor currents are equal to each other, I_L is given as $I_L = I_{L1} = I_{L2}$. The inductor losses are then calculated using Equation 2.3.

$$P_L = 2 \cdot I_L^2 \cdot R_L \tag{2.3}$$

Two fast diodes are present, with one in each switching leg where most of the losses consist of the conduction losses from the forward voltage drop. The total losses of the fast diodes are calculated using Equation 2.4.

$$P_{Diode,fast} = 2 \cdot V_f \cdot I_L \cdot (1 - D) \tag{2.4}$$

Here, D is the duty cycle, where the average duty cycle is 0.5. The MOSFET losses are made up of the conduction and switching losses. Here, the conduction losses are calculated using Equation 2.5

$$P_{con} = 2 \cdot I_L^2 \cdot R_{on} \cdot D \tag{2.5}$$

Likewise, the switching losses can be found using Equation 2.6.

$$P_{sw} = V_o \cdot I_L \cdot (t_r + t_f) \cdot f_{sw} \tag{2.6}$$

Lastly, capacitor losses can be found using Equation 2.7

$$P_{cap} = I_o^2 \cdot R_{esr} \tag{2.7}$$

All the calculated component losses are shown in figure 2.2.

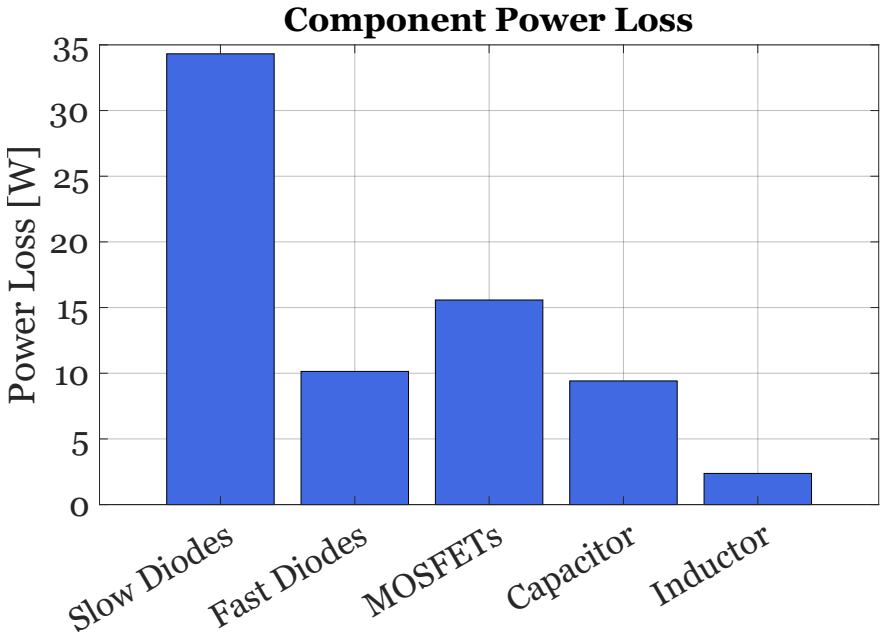


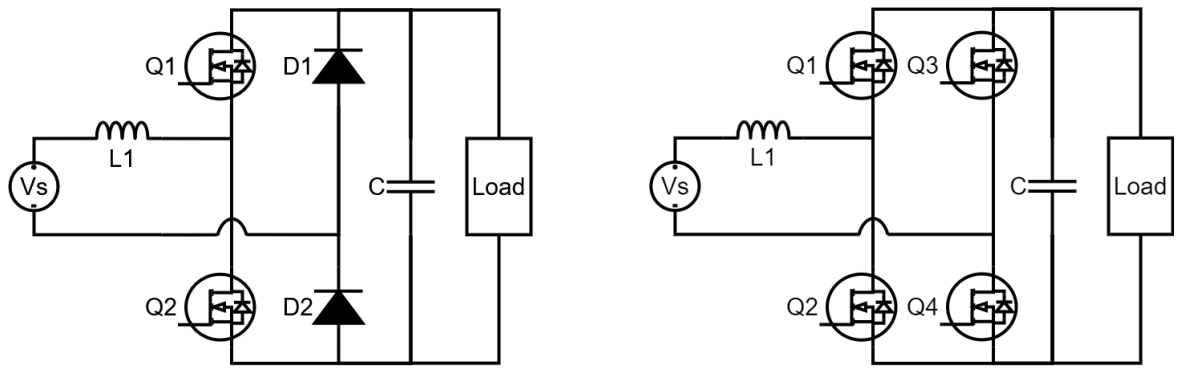
Figure 2.2: Estimation of component losses in Migatronic's existing converter based on datasheet parameters

From Figure 2.2 the total component losses are 71.8 Watt, which gives a converter efficiency of 98 % this is 1 % higher than the stated 97 % which Migatronics estimates their converter efficiency to be. However, some difference is expected since estimations of components had to be made as not all data was available from Migatronic. Additionally, the equations used to calculate the losses are only estimates and do not consider things such as the reverse recovery of the diodes or the impact of gate driver design on MOSFET losses. Regardless of the difference, Figure 2.2 reveals that the majority of component losses occur in the diodes and MOSFETs where the combined losses constitute 60 W of the total losses. While the capacitor and inductor losses are also significant, these are harder to reduce as the loss parameters are directly related to the design requirements of the converter, such as breakdown voltage, inductance, capacitance and rated current. In contrast, many of the MOSFET and diode losses can be reduced or completely eliminated by using a different converter configuration. With this in mind, a new converter configuration is investigated with the goal of improving efficiency.

2.2 Converter Configuration & Transistor choice

In order to reduce the number of components and reduce the complexity of the control, interleaved configurations will not be investigated. Additionally, only full bridge configurations will be considered to reduce the size of the DC link capacitor. There exist several configurations that use a bridgeless design. However, as the main objective is to increase efficiency, the totem pole configuration is selected for further analysis. This configuration is chosen because it incorporates only two or no diodes, as such it holds the potential to achieve a high efficiency. The totem pole configuration consists of two variants. The following diagrams presented in Figure 2.3 show the two totem pole configurations that will be described.

The classic Totem Pole, shown in (a), uses two switches in the High-Frequency (HF) leg and two diodes in the Low-Frequency (LF) leg. This configuration simplifies the control, since the diodes passively determine the current direction depending on the input voltage polarity. The downside is the losses caused by the diode forward voltage [9, 17]. In order to improve efficiency, the diodes can be replaced with switches that turn on and off according to the input voltage polarity. This allows the switches to mimic the behavior of the diodes, while reducing losses. This configuration requires a more complicated control scheme since the LF leg requires active control to turn on and off the switches. As the stated goal of this project is to maximize efficiency, the second configuration is chosen. [9, 17]



(a) Classical Totem-Pole **(b)** Improved Totem-Pole

Figure 2.3: Totem-Pole configurations

The Totem pole configuration offers high efficiency potential but has historically faced challenges in high-power applications. Because Q1 and Q2 are stacked on top of each other, it is required to have dead-time between each switching cycle. During the dead-time period, the body diode of Q1 conducts until Q2 turns on. As a result of this, the body diode goes through a reverse recovery period t_{rr}. In Si MOSFEts the reverse recovery charge Q_{rr} is very high compared to the newer SiC MOSFET as shown in Figure 2.4

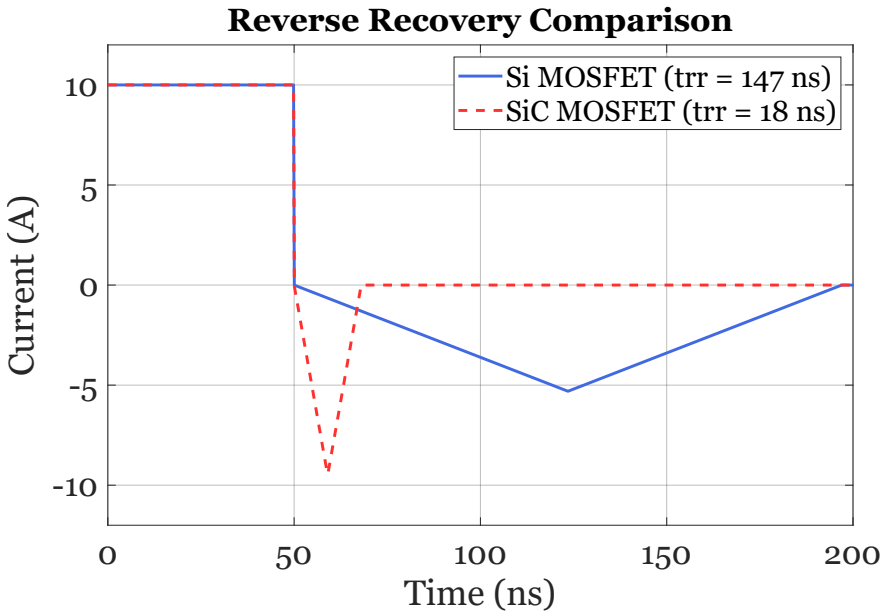


Figure 2.4: Reverse recovery comparison of SiC and Si based on datasheet values of MOSFETs "IPBE65R099CFD7A" and "C3M0045065K" [21] [8]

Since the reverse recovery period is much larger in the Si MOSFET the switching frequency is limited to avoid high switching losses. Consequently, this requires large inductors to meet the ripple current requirements. However, large inductors are typically not viable due to cost and size restrictions. Alternatively, running the converter in critical conduction mode (CrCM) could eliminate ripple requirements, but CrCM poses other problems in the form of high peak currents, increasing the rating of components and a varying switching frequency, which complicates filter design for EMI compliance. Therefore, Si MOSFETs are not considered for the converter.

As such, the two semiconductor technologies considered are SiC and GaN. Compared to traditional Si devices, both offer significantly improved performance characteristics, including lower conduction and switching losses. In addition, SiC has a much lower reverse recovery charge (Q_{rr}) and GaNFETs do not have reverse recovery at all because they do not have a body diode. Therefore, both are viable choices for a totem pole configuration. However, there are some significant differences between them that are worth discussing.

SiC is similar to Si as both are MOSFETs with the same structural build-up. as such, the difference is in the material composition. SiC offers several advantages over Si, including a higher dielectric breakdown voltage and great thermal conductivity. This results in a lower On resistance due to a reduced material path length.[10]

GaN transistors have historically been used for low-power high-switching-frequency applications. This has been primarily due to the low capacitance of the gate drain resulting in high switching speeds and due to the lack of a body diode resulting in no reverse recovery Q_{rr}. More recently GaN transistors have started to see increased use in power applications

where voltages of 600-800 V are used. They are generally a good choice for maximizing efficiency, as they have very low switching losses.[10]
The following is a table of the main advantages and limitations of SiC and GaN transistors.

SiC MOSFETs

- **Advantages:**
  - Good power scalability, with options above 3 kV breakdown voltage.
  - Low conduction losses due to low ON resistance.
  - Low switching losses, due to low Q_{rr} and fast switching speeds.
  - Higher thermal conductivity, resulting in simpler and smaller cooling solutions
  - High temperature stability, Performance characteristics like on resistance only increase slightly % from 25 °C to 125 °C.
- **Limitations:**
  - High body diode forward voltage of 3-5 V, leading to high losses during dead time operation.
  - Negative bias turn-off voltage, resulting in a more complex gate drive design.
  - Prone to gate driver ringing due to fast switching speeds.

GaN Transistors

- **Advantages:**
  - High efficiency potential
  - Low conduction losses due to low ON resistance.
  - The absence of a body diode means that there are no reverse recovery losses.
  - Low switching losses, due zero Q_{rr} and fast switching speeds.
  - Reduced losses in dead time operation range compared to SiC, due to reverse conduction voltage drop of 2-3 V.
- **Limitations:**
  - Low thermal conductivity, meaning more complex cooling solutions.
  - Low temperature stability, performance characteristics are sensitive to changes in temperature, resistance can double from 25 °C to 125 °C.
  - Negative bias turn-off voltage, resulting in more complex gate drive design.
  - Prone to gate driver ringing due to fast switching speeds.

In summary, while both SiC and GaN transistors present significant advancements over Si MOSFETs and are suitable for high-efficiency totem pole configurations, they have distinct characteristics and trade-offs. SiC MOSFETs are advantageous for high-power applications because of their robust thermal performance and higher breakdown voltage capabilities. GaN transistors excel in high-frequency applications due to their superior switching performance but can face challenges in power scalability and thermal management.

Although GaN transistors show great promise, this project chose to go with SiC MOSFETs. This choice was made for several reasons. Firstly, SiC MOSFETs were already available for use at the start of the project, which speeds up the design process. Additionally, the thermal advantages of SiC is a significant benefit, as they simplify the cooling solution required.

2.3 Project Scope

In order to achieve a higher converter efficiency, a more efficient topology has to be applied. One of the topologies that has the highest potential to increase efficiency is the Totem pole configuration. Compared to traditional topologies that use diodes in their design, the Totem pole configuration reduces losses by removing the need for diodes. When combined with improved conduction and switching characteristics of SiC MOSFETs relative to conventional silicon, the opportunity for enhancing overall converter efficiency is considerable.

Therefore, this project will investigate a 3.6 kW Totem-Pole converter using SiC MOSFETs, as this provides great potential for improvements in efficiency compared to Migatronic's existing converter.

Given the limited time available and the project being undertaken by one individual, several simplifications are made.
The converter will be tested in a DC-DC and inverter configuration. This allows the converter to be tested using an open-loop control structure, which in turn removes the need for measuring circuits.
A common mode filter will not be implemented to simplify the design process.
An external power supply will be used to power the gate driver circuits.
A 2-layer PCB will be used to increase the speed at which the converter can be constructed.
In-house components will be used when possible to speed up the design process.

2.4 Problem Statement

From the contents discussed, a problem statement is constructed. The problem statement aims to describe the primary problem that will be addressed in this project. Several objectives will be presented that aim to outline the necessary steps that are required to answer the problem statement. The following problem statement is constructed.
How can a single phase 3.6 kW totem-pole converter be constructed and operated using state-of-the-art SiC MOSFETs, which achieve a higher efficiency than Migatronic's current design?

- Develop a control system to operate the converter
- Identify components which fulfill Migatronic's requirements.
- Create a simulation model to verify converter operation
- Design a PCB circuit for the converter
- Build and test the prototype, in order to identify key problems that need to be solved
- Verify correct converter operation and estimate the efficiency

Control Strategy of Converter

This chapter addresses the design process of the converter control system. This includes the motivation to test the converter in a DC-DC and inverter configuration. The implementation of the control schemes will be presented, and an explanation of the code structure and verification of the control signals will be shown.

3.1 Selection of Hardware Implementation Platform

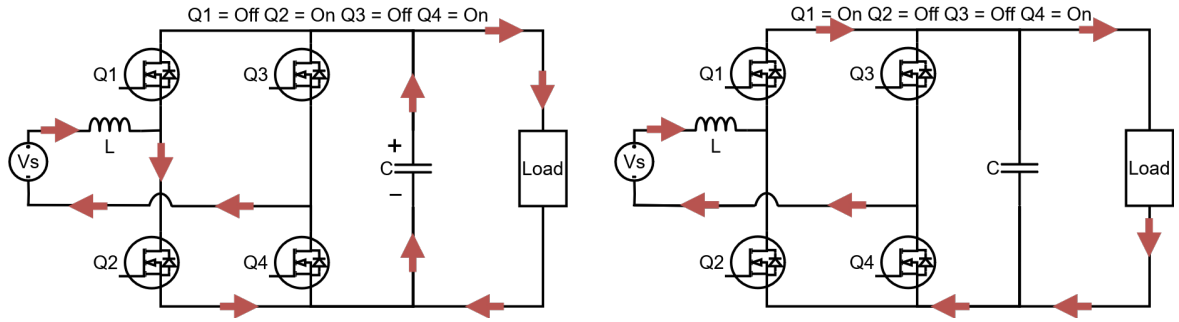
In order to control the converter, an FPGA-based solution is selected. Unlike microcontrollers, which rely on software execution, an FPGA is a hardware-based platform that allows digital logic to be directly implemented. Furthermore, because FPGAs are hardware-based, their performance is significantly better for high-speed operations. They are able to generate PWM with very little latency and precise timing, which is important for things such as accurate dead-time implementation[19]. The control structure is implemented using a Cmod S7 programmable development board, which is built around a Xilinx Spartan 7 FPGA. This board includes 32 digital I/O pins, two analog input signals, and a 5V rail. The board also includes a 12 MHz oscillator and a USB circuit for power and programming[3]. VHDL is used to program the FPGA using the Xilinx Vivado software.

3.2 Rationale for testing in DC-DC and Inverter Configuration

The evaluation of the converter will be carried out in a DC-DC and inverter configuration. This allows the converter to be operated in an open loop, removing the need for a feedback loop. There is also no need to measure the input voltage and current since they are constant. As such, the control system can be operated independently from the rest of the converter, while the output voltage is adjusted based on the governing equations and known variables. This simplifies the control system design and enhances its robustness, since any noise or transients originating from the converter will not adversely impact the controller. Furthermore, the converter can still be operated in a way that gives a good estimation of the converter's efficiency, since the current and voltages will be similar to the converter operating in PFC mode.

3.3 DC-DC Control Operating Principle

In this setup, the first leg consisting of Q1 and Q2 is treated as one pair when Q1 is in the "ON" state, Q2 is in the "OFF" state, and vice versa. In the second leg, Q3 is always turned "OFF" and Q4 is always turned "ON". When Q1 is "OFF" and Q2 is "ON", the current of the inductor will flow through Q2 and Q4 back to the source, causing the inductor to charge and the capacitor to discharge, as illustrated in Figure 3.1 (a). When Q1 is "ON" and Q2 is "OFF", the inductor current will flow through the capacitor and the load, causing the inductor to discharge and the capacitor to charge, as illustrated in Figure 3.1 (b).



(a) Inductor charging state **(b)** Inductor discharging state

Figure 3.1: Converter switching states in DC-DC configuration

As such, the relationship between the charge state of the inductor and capacitor depends only on switches Q1 and Q2. This, in turn, simplifies the control since only the first leg has to be controlled.

3.3.1 Duty cycle derivation of DC control structure

It is important to understand the relationship between the output voltage and the duty cycle of switches Q1 and Q2. This can be derived from the inductor current equations. In the charging state, the voltage across the inductor is the same as the input voltage V_S as given in Equation 3.1. During discharge, the inductor voltage is given by the output voltage V_o minus the input voltage V_s as seen in equation 3.2. Included in the equations are D_{Q2} for the duty cycle of Q2 and T for the period. These variables represent the amount of charge/discharge time with respect to a period.

$$\Delta I_L = \frac{V_s}{L} \cdot D_{Q2} \cdot T \qquad (3.1) \qquad \Delta I_L = \frac{< V_o > - V_s}{L} \cdot (1 - D_{Q2}) \cdot T \qquad (3.2)$$

According to the steady-state condition, the average inductor current ΔI_L over a period must be constant, and as such the positive and negative change in current must be equal, so that $\Delta I_L - \Delta I_L = 0$. Therefore, equations 3.1 and 3.2 can be set equal and variables L and T will cancel out. This is given in Equation 3.3.

$$V_s \cdot D_{Q2} = (< V_o > - V_s) \cdot (1 - D_{Q2}) \qquad (3.3)$$

Writing out the terms gives Equation 3.4.

$$V_s \cdot D_{Q2} = < V_o > - V_s - < V_o > \cdot D_{Q2} + V_s \cdot D_{Q2} \qquad (3.4)$$

From this, the term $V_s \cdot D_Q$ cancels out, giving Equation 3.5

$$V_s = < V_o > - < V_o > \cdot D_{Q2} \qquad (3.5)$$

Factoring the output voltage $< V_o >$ gives Equation 3.6.

$$V_s = (1 - D_{Q2}) \cdot < V_o > \qquad (3.6)$$

The equation can then be rearranged with respect to D_{Q2} as seen in Equation 3.7

$$D_{Q2} = 1 - \frac{V_s}{V_o} \tag{3.7}$$

Since the duty cycle D ranges from 0-1, it can be concluded that the converter operates in boost mode.
Before implementation, it is necessary to incorporate dead time. Dead time is a short time interval between each switching cycle in which both switches are off. This measure aims to prevent a shoot-through scenario in which the switches, Q1 and Q2, are turned on simultaneously. Avoiding this is crucial to avoid a situation where the DC capacitor is effectively short-circuited, resulting in the generation of high currents that would damage the converter. An implementation method is to reduce the ON time of both switches equally so that the duty ratio does not change. However, in this case, this would affect the output voltage since during the dead time the converter is still conducting because of the body diodes present in the switches. As a result of the orientation of the body diode, the current flows through Q1 and Q4, which is the same conduction state as shown in Figure 3.1 (b). To account for this effect, the inductor current equations can be rewritten as Equation 3.8.

$$\Delta I_L = \frac{V_s}{L} \cdot D_{Q2} \cdot T - \frac{< V_o > - V_s}{L} \cdot k_d \cdot T \tag{3.8}$$

And Equation 3.9

$$\Delta I_L = \frac{< V_o > - V_s}{L} \cdot D_{Q1} \cdot T + \frac{< V_o > - V_s}{L} \cdot k_d \cdot T \tag{3.9}$$

Where, k_d represents the fraction of time spent in dead time with respect to the period T. From equations 3.8 and 3.9 it is shown that the inductor discharges at an additional rate equal to twice the dead time. This also means that the dead time affects only the inductor discharge rate. Therefore, only the duty cycle of Q1 needs to be adjusted to account for the dead time. As such, the relationship between D_{Q1} k_d can be derived. Equations 3.8 and 3.9 are set equal and the variables L and T cancel out, giving Equation 3.10.

$$V_s \cdot D_{Q2} = (V_o - V_s) \cdot D_{Q1} + 2 \cdot k_d \cdot (V_o - V_s) \tag{3.10}$$

Isolating for D_{Q1} gives Equation 3.11.

$$D_{Q1} = \frac{V_s \cdot D_{Q2}}{V_o - V_s} - 2 \cdot k_d \tag{3.11}$$

Substituting D_{Q2} with Equation 3.7, then gives the final Equation 3.12.

$$D_{Q1} = \frac{V_s}{V_o} - 2 \cdot k_d \tag{3.12}$$

From this, the duty cycle can be set on the basis of a given input voltage, a desired output voltage, and a dead time.

3.3.2 Implementation of DC control system

Since the oscillator acts as a clock reference for the FPGA, it will be used to define the switching frequency in terms of clock cycles. By tracking each rising edge of the clock, the elapsed time can be recorded; at 12 MHz this equals 83.33 ns for a period. As such, the number of clock cycles to a given switching frequency can be calculated as the ratio of the clock frequency and the switching frequency given as $c_s = f_c / f_s$. The duty cycle can then

also be defined in terms of clock cycles by multiplying the duty cycle by c_s as $D_s = D \cdot c_s$. Lastly, the dead time k_d can also be defined in terms of clock cycles. Then a series of *if* statements can be constructed that check whether the time counter is below or above the thresholds set by D_s, k_d, and c_s. An illustration of the control process using a flow chart is shown in Figure 3.2.

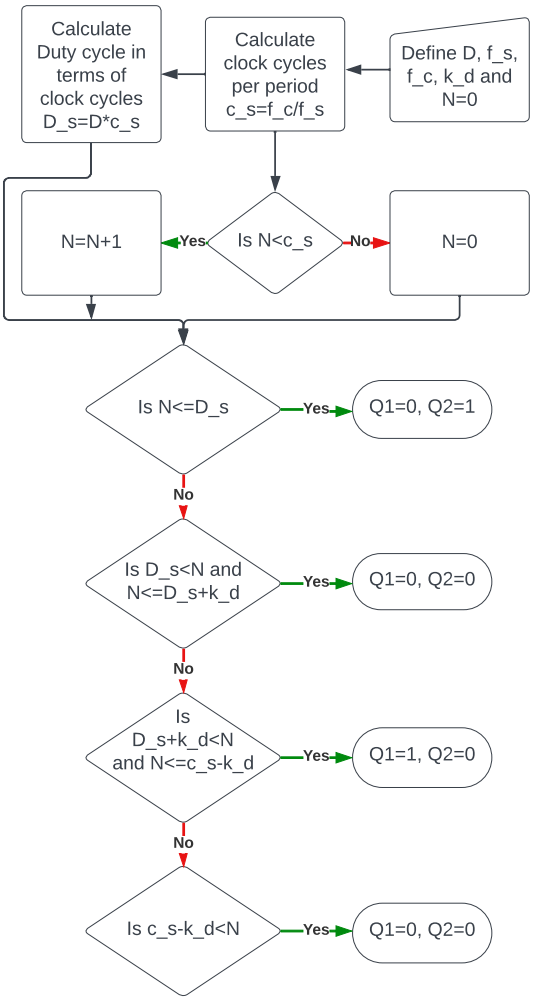


Figure 3.2: Flowchart diagram of the control process for FPGA signal generation

Because time is tracked through a clock in finite increments, timing errors can occur. If the chosen duty cycle is not an integer multiplicative of the clock period, the output signal will deviate from the intended one. In the worst case, this can be up to half the clock period. Furthermore, the relative error increases at lower duty cycles, since the absolute timing error is constant relative to the on-time. To reduce the relative error, a higher frequency oscillator is needed, or the switching frequency has to be reduced. To test the program, the code is executed with a duty cycle of $D_{Q1} = 0.56$, a dead time of 1 clock cycle, and a switching frequency of 100 kHz. The FPGA output signals are shown in Figures 3.3 and 3.4.

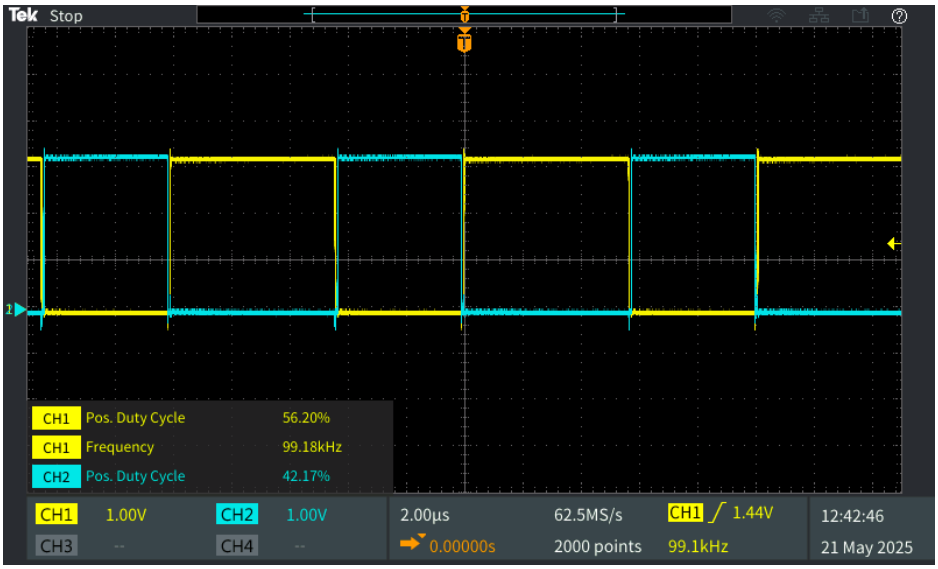


Figure 3.3: FPGA gate control signals, showing duty cycle and frequency

According to Figure 3.3, the switching frequency is 99.2 kHz, which corresponds well to the approximate period of 10μs, the on time of Q1 is 5.62μs, which gives a discrepancy from the desired value. However, this is expected since the difference of 0.08μs is approximately equal to one clock cycle of dead time. The Q2 on time is 4.217μs and is also slightly lower due to the dead time. Finally, Figure 3.4 shows the rise and fall time of the control signals and the dead time period, here the fall and rise time is between 6.5-7 ns and the dead-time period is 83 ns which lines up exactly with the oscillators clock period.

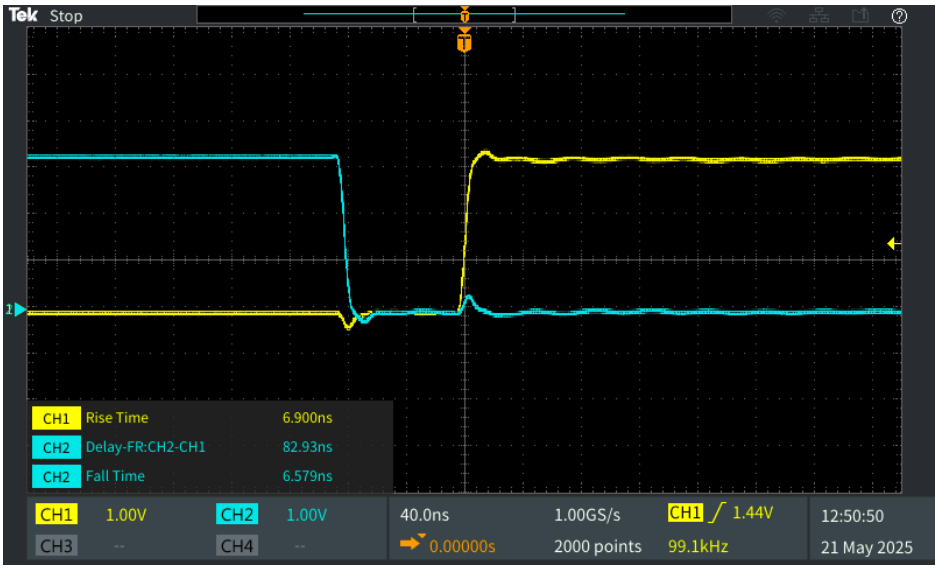
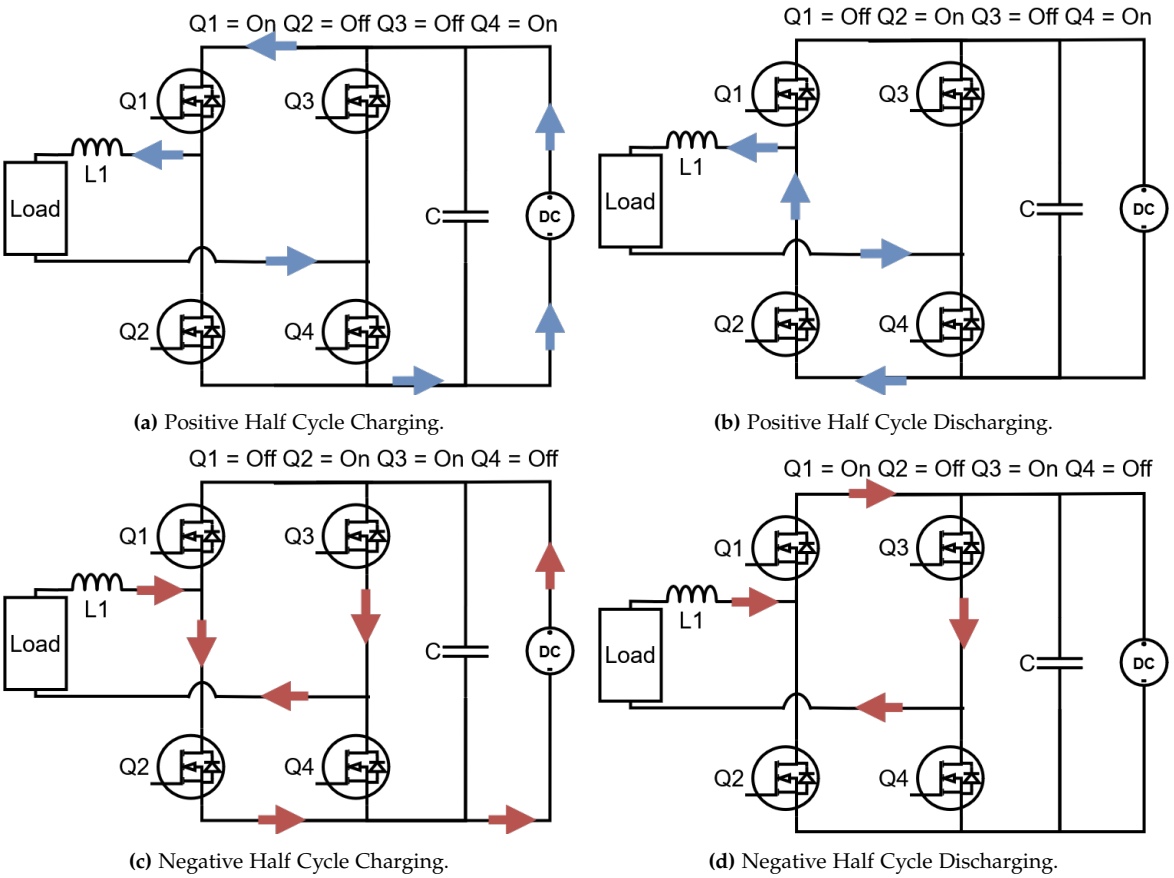


Figure 3.4: FPGA Gate control signals, showing the rise time, fall time and dead time

According to both graphs, the FPGA output is very close to the desired output. From this, it is shown that the code works as intended and that the FPGA output can be used to drive the converter in a DC-DC configuration.

3.4 Inverter Control Operating Principle

For the inverter, unipolar switching is used. This control strategy is used because it is the reverse of the operating strategy used when the converter is operating in PFC mode. This means that the current and voltage through the switches would be the same. This in turn allows the switch losses calculated in the inverter configuration to be used directly as reference for the losses that can be expected in a PFC converter configuration. In this control strategy, the first leg consisting of Q1 and Q2 is treated as one pair, here when Q1 is in the "ON" state, Q2 is in the "OFF" state, and vice versa. In the second leg, Q3 and Q4 are also complementary, so when one is off, the other is on. In this setup, the two legs will operate at different frequencies. Here, the HF leg consisting of Q1 and Q2 will operate at 100 kHz, while the LF leg Q3 and Q4 will operate at 50 Hz. During operation there are 4 different states, each of these states determines whether the inductor is charging or discharging and what the polarity is. In the positive half-cycle, Q3 is off and Q4 is on. Therefore, the inductor charges when Q1 is on and Q2 is off and discharges when Q1 is off and Q2 is on, this can be seen in Figures 3.5 (a) and (b). During the negative half-cycle, Q3 is on and Q4 is off. Here, the inductor charges when Q1 is off and Q2 is on and discharges when Q1 is on and Q2 is off. This is shown in Figures 3.5 (c) and (d). As a result, it can be concluded that the inductor charge/discharge state is only dependent on the duty cycle of Q1 and Q2. Furthermore, the duty cycle applied to the HF leg during the positive cycle just has to be inverted during the negative cycle. As such, the duty cycle only needs to be derived for one half-cycle.



(a) Positive Half Cycle Charging.

(b) Positive Half Cycle Discharging.

(c) Negative Half Cycle Charging.

(d) Negative Half Cycle Discharging.

Figure 3.5: Operation principle in inverter configuration

3.4.1 Duty cycle derivation of inverter control structure

To control the converter, it is important to understand the relationship between the output voltage and the duty cycle of switches Q1 and Q2. This can be derived from the inductor current equations in the positive half-cycle. In the charging state, the voltage across the inductor is equal to the input voltage V_S minus the output voltage V_o as given in Equation 3.13. During discharge, the inductor voltage is equal to the output voltage V_o as seen in the equation 3.14. The equations are D_{Q1} for the duty cycle of Q1 and T for the period.

$$\Delta I_L = \frac{V_s - < V_o >}{L} \cdot D_{Q1,pos} \cdot T \quad (3.13) \qquad \Delta I_L = \frac{< V_o >}{L} \cdot (1 - D_{Q1,pos}) \cdot T \quad (3.14)$$

According to the steady-state conditions, the change in current should be the same for charging and discharging, so equations 3.13 and 3.14 can be set equal and variables L and T cancel out, giving equation 3.15.

$$(V_s - < V_o >) \cdot D_{Q1,pos} = < V_o > \cdot (1 - D_{Q1,pos}) \quad (3.15)$$

The derivation of equation 3.15 and isolating for $D_{Q1,pos}$ gives the relationship between the Duty cycle and the input and output voltage, as shown in equation 3.16 .

$$D_{Q1,pos} = \frac{V_o}{V_s} \quad (3.16)$$

Since the duty cycle can only be between 0 and 1 and the output voltage decreases when the duty cycle decreases, it can be concluded that the converter operates in buck mode. Similarly to the DC configuration, dead time is also needed in order to avoid shoot-through, in this case from the DC supply. In this case during dead-time it results in additional discharging of the inductor. To compensate for this, the duty cycle of $D_{Q2,pos}$ is shown in equation 3.17.

$$D_{Q2,pos} = 1 - D_{Q1,pos} - 2 \cdot k_d \quad (3.17)$$

Now that the duty cycle for the positive half wave has been derived, the negative wave duty cycles are simply the inverted values as shown in equations 3.18 and 3.19.

$$D_{Q1,neg} = D_{Q2,pos} \quad (3.18) \qquad D_{Q2,neg} = D_{Q1,pos} \quad (3.19)$$

With these equations, the relationship between the input voltage and the output voltage is known. However, in order to generate a sinusoidal output voltage waveform the duty cycle needs to vary over time, in order to do this a control system is implemented on the FPGA controller.

3.4.2 Implementation of inverter control system

In order to output the correct PWM signals, a carrier and duty cycle must be created. These must be designed according to the desired output voltage, fundamental frequency, and switching frequency. The output of the carrier and duty cycle is then compared in a comparator, which then outputs the necessary PWM signals.

To create a carrier wave f_s, f_c, N, and N_{dir} are defined, each representing the switching frequency, the clock frequency, the counter and the direction accordingly. The amplitude of the carrier signal is chosen as 7500. Then in order to obtain the correct frequency of the carrier, the step size has to be set such that the number of clock cycles it takes to go through one carrier period is equal to 10 μs. This is calculated using equation 3.20.

$$N_{step} = \frac{2 \cdot 7500 \cdot f_s}{f_c} \tag{3.20}$$

With the step size calculated as 125 a series of if statements is constructed. This is shown in Figure 3.6.

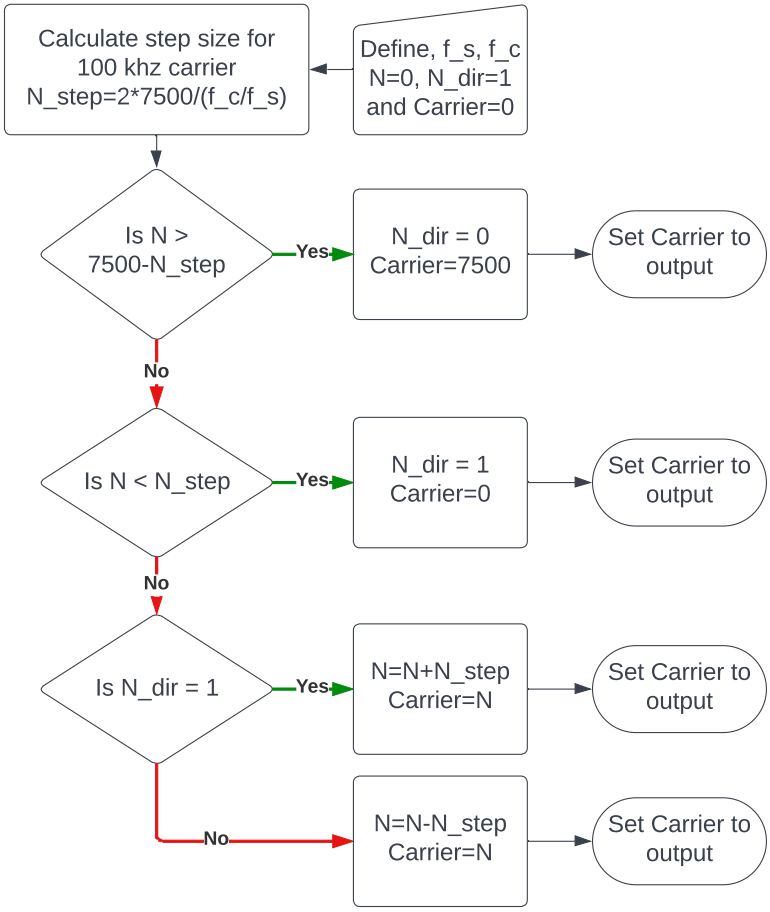


Figure 3.6: Flowchart diagram of the generated carrier wave

The *if* statements compare the value of N to check what the value of the carrier should be. Furthermore, when N reaches 0 or 7500 the value of N_{dir} is flipped, which is then used to determine whether the carrier signal should increase or decrease. The final result is a 100 kHz carrier wave changing in steps of 125 between 0 and 7500. The carrier signal is then connected to the output so that it can be used by the comparator.

To generate a sinusoidal voltage output using PWM signals, the duty cycle must be varied over time to look like the half-cycle of a sine waveform. In an FPGA, a sine waveform can be represented using a lookup table (LUT). Here, the LUT stores multiple points on the sine waveform. These values are then accessed using a counter to produce a digital

representation of the sine waveform. To generate the sine LUT values for one half-cycle, equation 3.21 is used.

$$Lut(N) = M \cdot 7500 \cdot sin(\pi \cdot N) \tag{3.21}$$

Here, $M = V_o/V_s$ is the modulation index that is used to generate values that give the correct output voltage. 7500 is the amplitude and is included to scale the values to the carrier wave range. N is an integer that goes from 1 to 500 in step sizes of 1. The generated value is then stored in the LUT for each value of N. This gives a LUT with 500 values. Lastly, because the LUT values at the beginning and end are very low, this will result in a very low duty cycle that can go below 1 %. At a 100 kHz switching frequency, this would result in a turn-on time of less than 100 ns. This is too short when considering the dead time that is needed and the rise time of the gate source voltage. As a result, the duty cycle at the extremes is clamped, so it cannot go below 6.5 %. With the LUT generated, it can be implemented in a VHDL structure, a flowchart of this is shown in Figure 3.7.

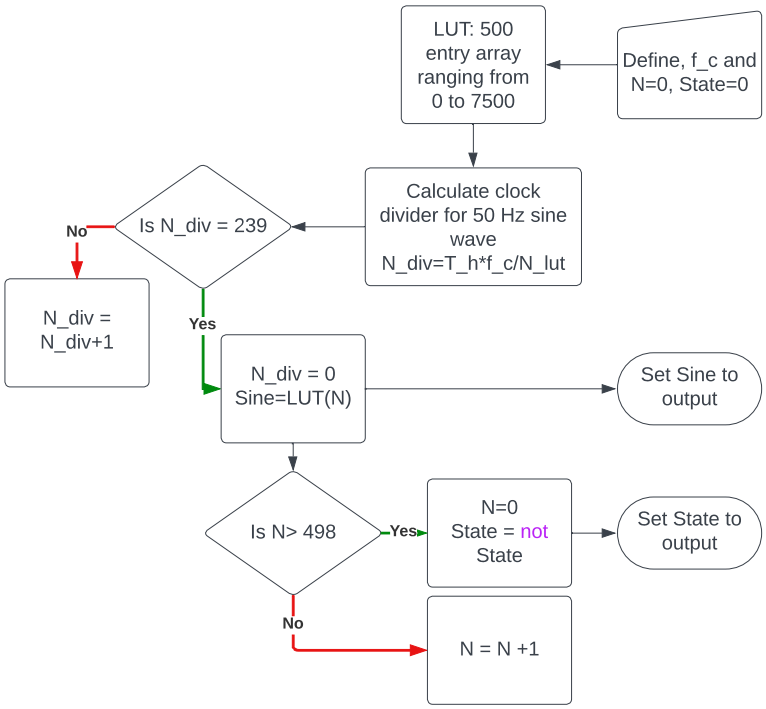


Figure 3.7: Flowchart diagram of the Sine Wave Look Up Table

In order to shift through the values in the LUT f_c, N, *Sine* and *State* is defined, where *State* is used to determine polarity, and *Sine* is a LUT value used for the duty cycle. Since the frequency of the duty cycle is determined by the speed at which the counter N increments through the LUT, this would result in a frequency of approximately 24 kHz when N follows the clock frequency f_c. This is much faster than the required 50 Hz. Therefore, a clock divider is required to reduce the frequency. The clock dividers values is determined using equation 3.22.

$$N_{div} = \frac{f_{sine} \cdot f_c}{500} \tag{3.22}$$

where f_{sine} is the desired frequency of the duty cycle. With this, the clock divider N_{div} is calculated as 240. Through a series of if statements, the value of N_{div} and N is checked. When N_{div} reaches its maximum value, *Sine* is updated to the next LUT value using N. Furthermore, when N reaches the end of the LUT table represented by 499, the *State* signal is inverted. This allows *State* to record each time a half-cycle has passed. Both the *State* and *Sine* signals are connected to the output. These are then used in combination with the carrier signal to generate the PWM signals.
The comparator uses the three inputs *Sine*, *State*, and *Carrier* to determine the value of switches Q1, Q2, Q3, and Q4. This is done using a series of *if* statements shown in Figure 3.8.

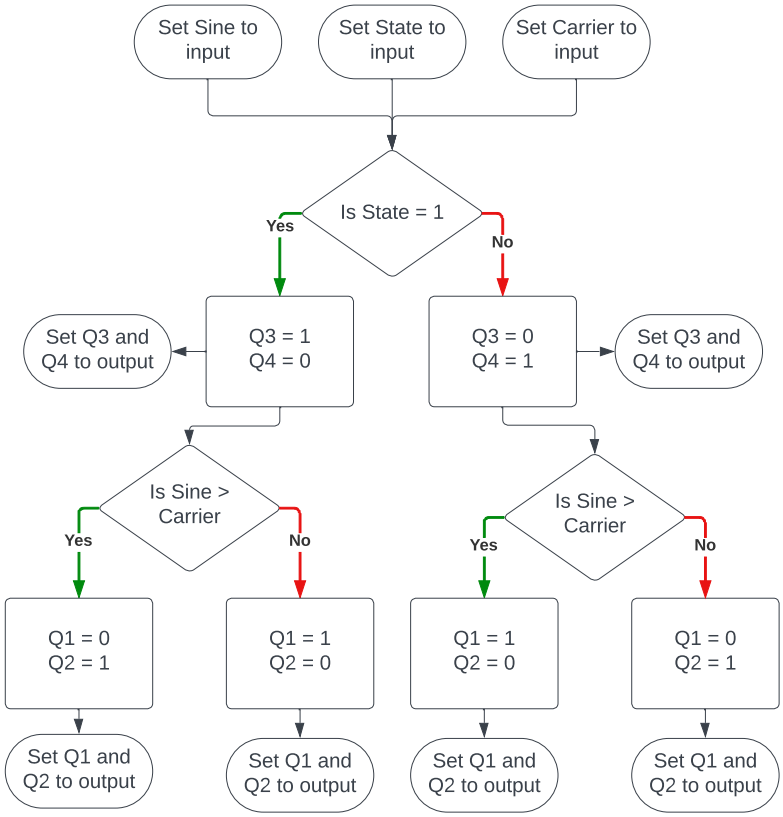


Figure 3.8: Flowchart diagram of the comparator for PWM signal generation

First, the signal *State* is checked to determine the polarity where Q3 and Q4 are set on the basis of this polarity. For Q1 and Q2, *State* inverts their PWM behavior, and their switching is controlled by the comparison between *Sine* and *Carrier*. Q1, Q2, Q3, and Q4 are connected to the output terminals. Using this all 4 PWM signals are generated and vary with respect to a sine waveform and the polarity. However, before this can be implemented into the FPGA dead-time is required during each switching transition. To implement dead-time, a delay structure is created. The delay structure for Q1 is shown in Figure 3.9.

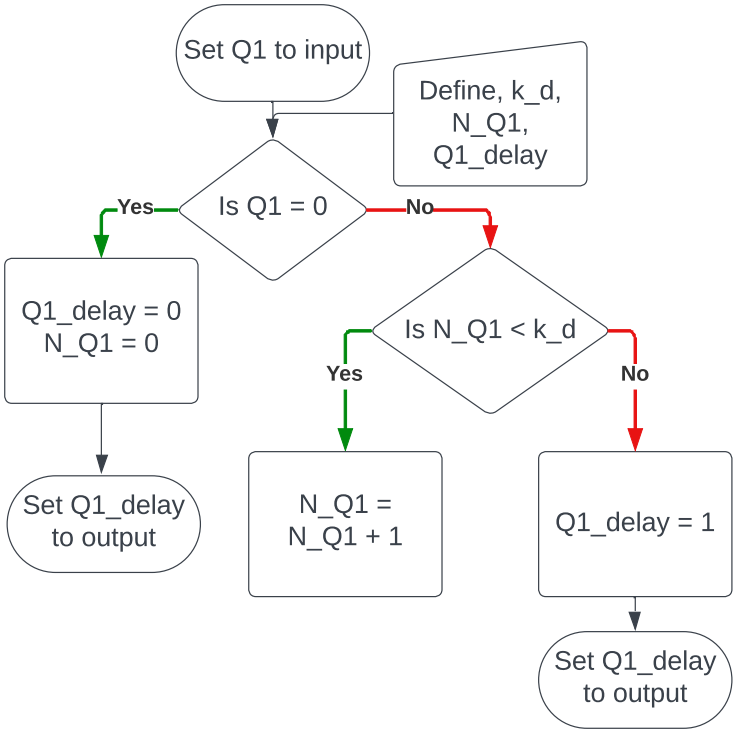


Figure 3.9: Flowchart diagram of the dead time implementation shown for Q1

Here, k_d, N_{Q1}, and $Q1_{delay}$ are defined, representing the dead-time in the number of clock cycles, the Q1 counter, and the delayed output signal, respectively. Then a series of if statements is used to check the value of the input signal Q1. If Q1 is 1 a counter is started and the input Q1 is first transferred to the output $Q1_{delay}$ when the counter N_{Q1} is equal to the dead-time in clock cycles k_d. This structure allows dead-time to be implemented in increments of 83.33 ns. This same structure is connected to Q2 Q3 and Q4 as well to implement dead time on all PWM signals.
With this, all 4 control structures, the Carrier generator, the Sine LUT, the PWM comparator, and the delay block are finalized. As such, this can then be implemented into the FPGA and the PWM signals can be tested.
In Figure 3.10 the PWM signals of Q1 and Q2 are shown represented as "CH1" and "CH2", respectively. Here, the frequency is 98.35 kHz, which is close to the expected frequency target, indicating that the carrier frequency is correct. Furthermore, there is also a dead time of 84 ns between switching transitions, which indicates that the delay block is working as intended. The Q1 PWM signal has a duty cycle of 67 %. Compared to the Q1 duty cycle in Figure 3.11, which is 9.9 %, this shows that the Q1 duty cycle is changing over time.

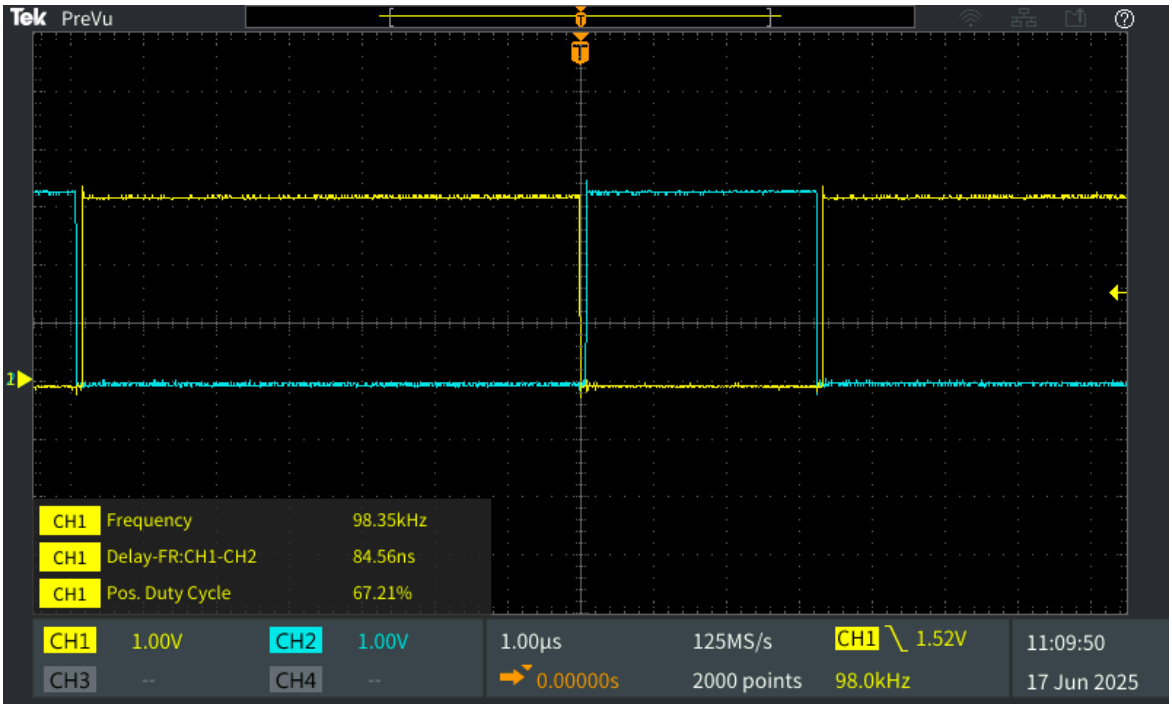


Figure 3.10: PWM signals of Q1 and Q2 showing correct frequency and dead time

From Figure 3.11. The four PWM signals Q1 Q2 Q3 and Q4 are shown. Here, Q3 and Q4 are represented as "CH3" and "CH4", respectively. It can be seen that when Q3 and Q4 switch, so do Q1 and Q2 and their duty cycle inverts. Indicating that the "State" signal is working as intended to change polarity. It can also be seen that there is a dead time between Q3 and Q4, showing that the delay block also works here.

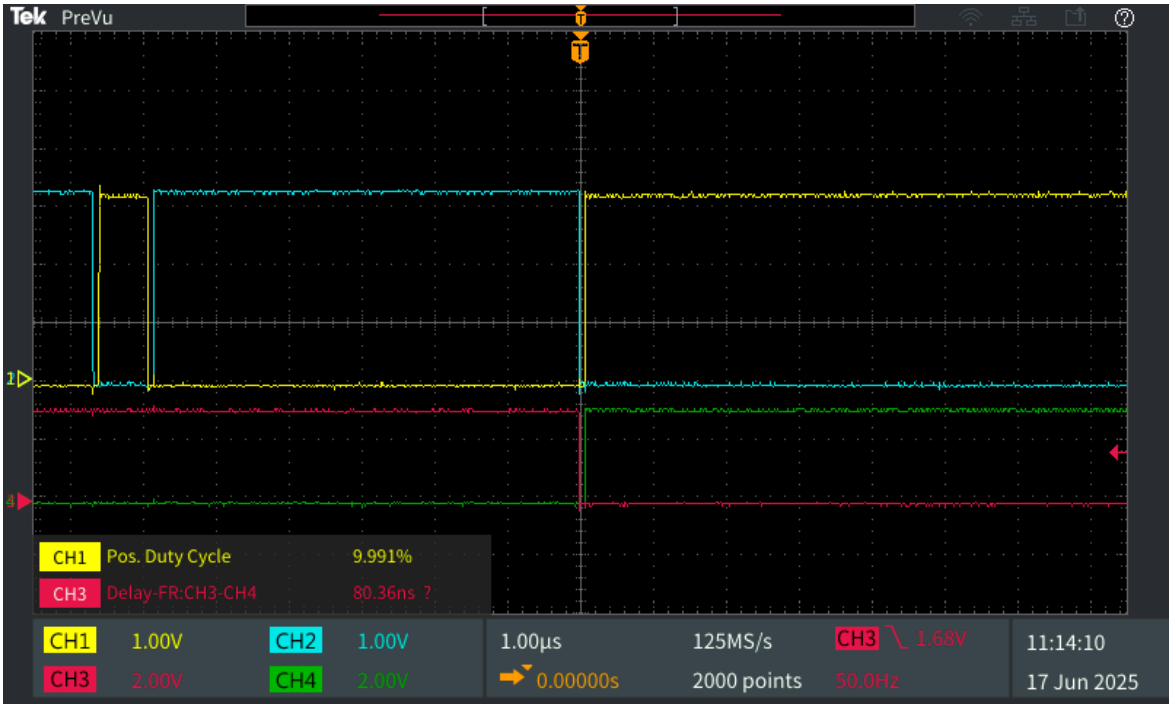


Figure 3.11: PWM signals at the end of a half cycle, showing a low duty cycle of Q1

In Figure 3.12, Q3 and Q4 are shown over a longer time span. Here, it can be seen that the frequency is 50 hz, indicating that the clock divider logic is working as intended.

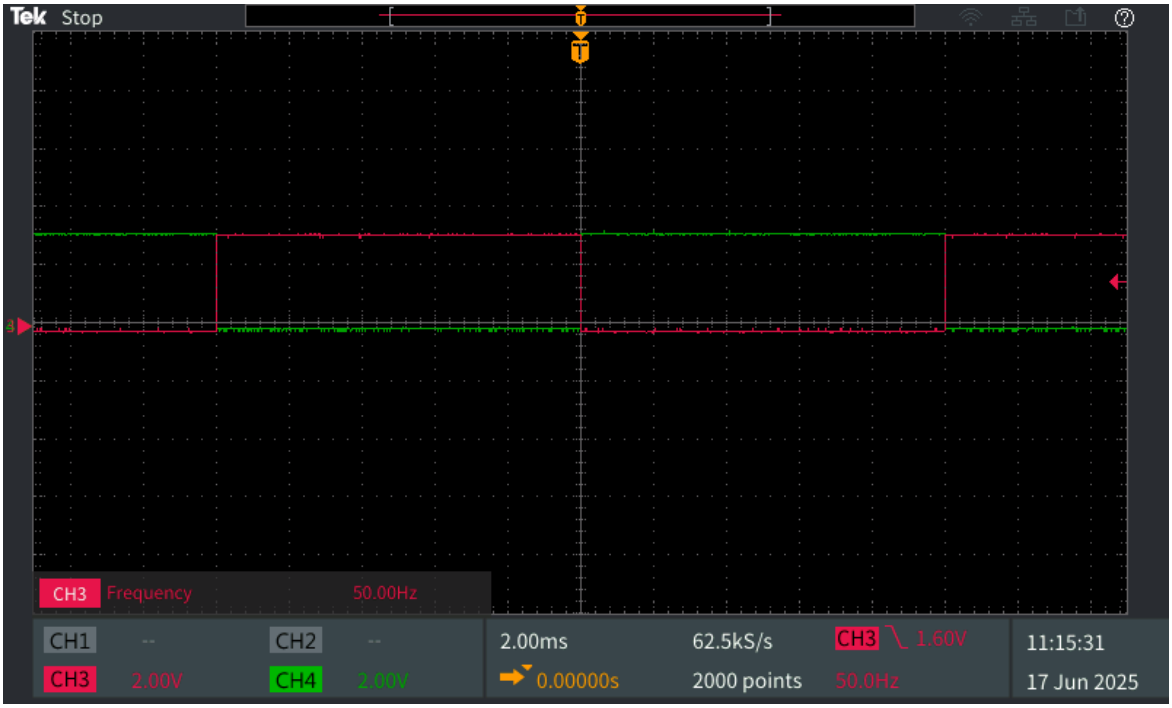


Figure 3.12: PWM signals of Q3 and Q4 with a 50 Hz frequency

To ensure that the PWM signals behave correctly over an entire half-cycle, the duty cycle is evaluated. In order to show the duty cycle, an RC filter is constructed here the cut-off frequency is set to 1000 Hz. a 100 nF capacitor and a 1.6 Ω resistor are used. This is then connected to the PWM signal of Q1. The schematic of this is shown in Figure 3.13

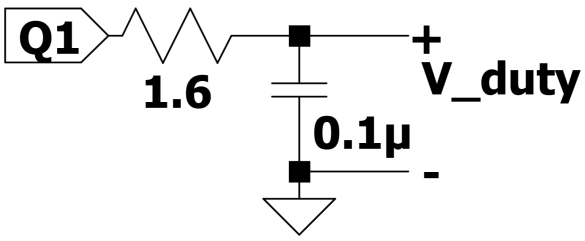


Figure 3.13: RC filter used to measure the duty cycle of Q1

The voltage is then measured across the capacitor to display the duty cycle. This is shown in Figure 3.14. Looking at the duty cycle, it can be seen that it follows a sinusoidal waveform. Furthermore, the half-cycle frequency is 100 Hz, which is the desired frequency. Additionally, after each half-cycle the duty cycle flips, which indicates that the polarity is working.

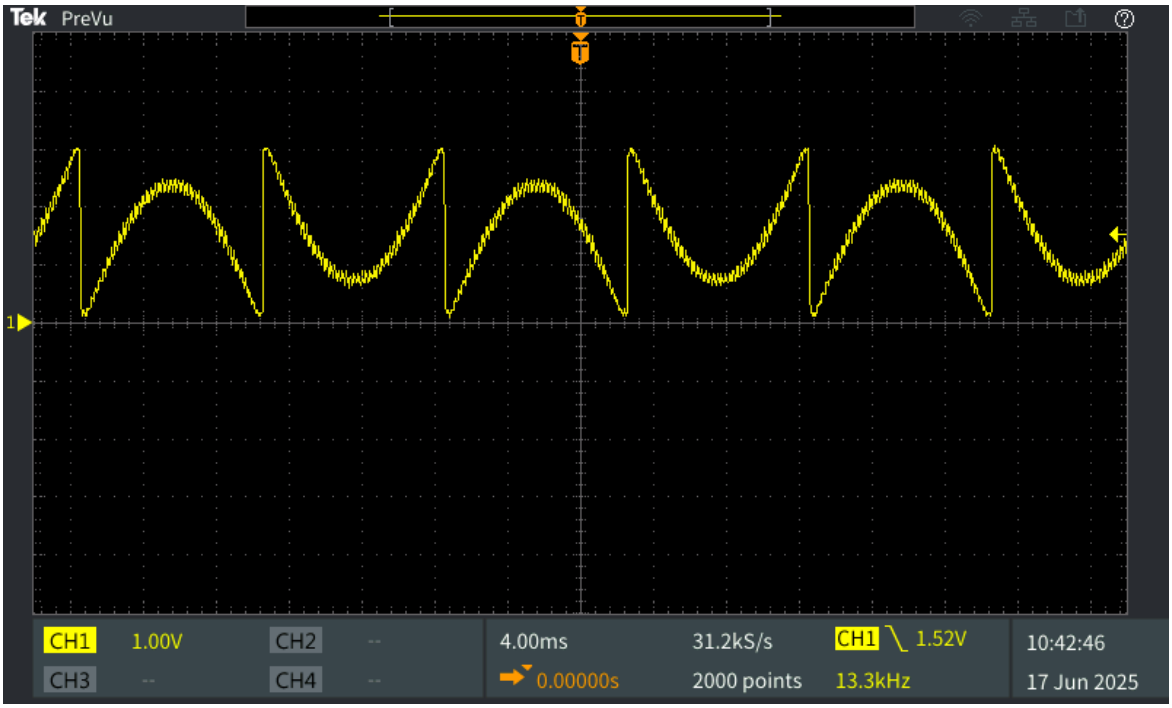


Figure 3.14: Duty cycle of Q1 measured through an RC filter

Looking at the edges of the duty cycle where the maximum and minimum voltages occur, it can be seen that these range between 0.3 V and 3V. The duty cycle does not go above or below this range even though the Q1 PWM output from the controller is 0 or 3.3 V. This shows that the duty cycle clamping is working so that the turn on/off time does not get too small.
It is shown that the inverter control code is working as intended and can be used to drive the converter in the inverter configuration.

Power Stage, Gate Driver Design and Passive Component Selection

In order to build the converter four switches are required. The choice of these switches is important because the conduction and switching characteristics directly impact the total losses of the converter. It is therefore important to consider how much loss can be expected in a given switch such that the efficiency of the converter can be as high as possible. In addition, the choice of switches also affects the necessary gate driver circuit required to operate them as intended. To this end, this chapter will decide the choice of switches based on a calculation of the estimated losses. The gate driver and the gate driver circuit will then be based on the operating criteria of the chosen switches.

4.1 Selection of SiC MOSFETs

One of the main design requirements of the switches is to reduce the losses so that the converter efficiency is higher than that of a Migatronic's existing configuration. According to Figure 2.2 the total losses currently seen in the switches and diodes are 60 W. As such, the goal is to use switches with total losses lower than this. To this end, the two primary losses that are relevant are the conduction losses and the switching losses. It is therefore also important to consider each converter leg individually, as the switching frequency is different. The two switches primarily considered are the SiC MOSFET's C3M0025065K and C3M0045065K from Wolfspeed, as these are already available in the laboratory, and they both are within the current rating required and have a sufficient breakdown voltage for this project. To compare both switches, the device characteristics of each switch are given in table 4.1.

Switch Model:	C3M0045065K	C3M0025065K
On-State Resistance [$m\Omega$]	45	25
Turn-On Switching Energy [μJ]	57	121
Turn-Off Switching Energy [μJ]	14	53
Gate Threshold Voltage [V]	2.6	2.3
Recommended Vgs,on [V]	15	15
Recommended Vgs,off [V]	-4	-4
Internal Gate Resistance [Ω]	3	1.3
Recommended Gate Resistance [Ω]	2.5	2.5
Body Diode Forward Voltage [V]	4.8	5

Table 4.1: Device characteristics of two SiC MOSFET's from Wolfspeed [21] [20]

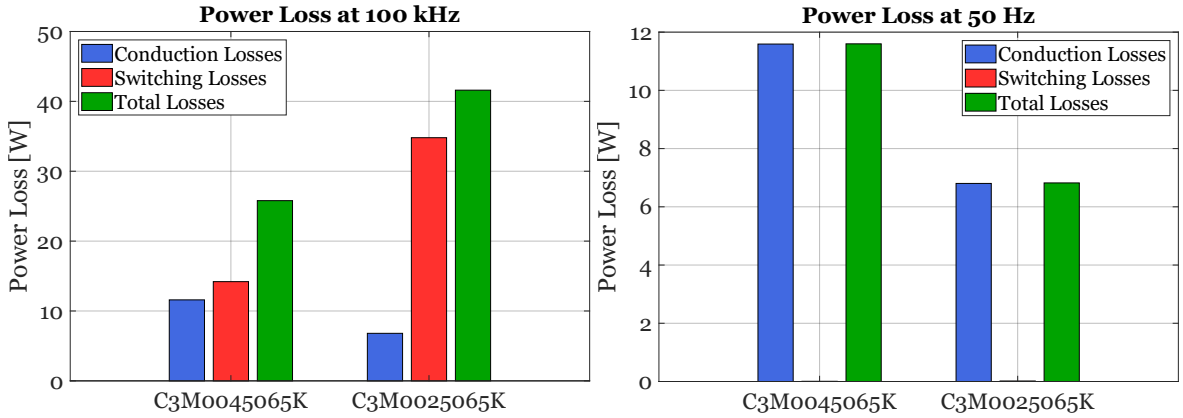
Based on the device characteristics given in Table 4.1 the estimated losses that each switch leg will produce can be calculated. Here, the conduction losses consist of two parts. The losses when the switch is on and the losses during the dead-time when the body diode conducts. This can be calculated using Equation 4.1

$$P_{conduction} = I_{ac}^2 \cdot R_{on} \cdot \frac{T - t_d}{T} + I_{ac} \cdot V_f \cdot t_d \tag{4.1}$$

Where R_{on} is the switch on resistance, V_f is the body diode forward voltage; and T, t_d are the time period and dead time, respectively.
The total switching losses can be calculated as the sum of the turn on and off energy multiplied by the switching frequency. This is then multiplied by two to get the losses for both switches as given in Equation 4.2.

$$P_{switching} = 2 \cdot (E_{turn,on} + E_{turn,off}) \cdot f_s \tag{4.2}$$

With these equations, the estimated losses of each switch can be calculated and the results are shown in Figure 4.1



(a) Estimated Power Losses for High Frequency Leg

(b) Estimated Power Losses for Low Frequency Leg

Figure 4.1: Comparison of estimated switch power losses for each converter leg

As shown in Figure 4.1, the losses differ significantly for each converter leg due to the difference in frequency. In the HF leg, the C3M0045065K is the best choice as the superior switching characteristics make the total losses less than the C3M0025065K. In contrast, the C3M0025065K's better conduction properties excel in the LF leg, since the switching losses here are negligible. As a result, the C3M0045065K is chosen for the high frequency leg and the C3M0025065K is chosen for the low frequency leg. This gives a combined loss for both legs of 33 W. Approximately half of the diode and MOSFET losses in Migatronic's existing converter.

4.2 Gate Driver Choice and Driver Circuit

In order to turn the MOSFETs on and off, a gate driver is required. The gate driver should be chosen with regard to the recommended specifications of the MOSFET manufacturer as this helps to reduce switching losses and accidental turn on. The first consideration is the Gate driver turn on and turn of voltage. These values are important to consider as they directly impact ON resistance during conduction. This correlation is shown in Figure 4.2

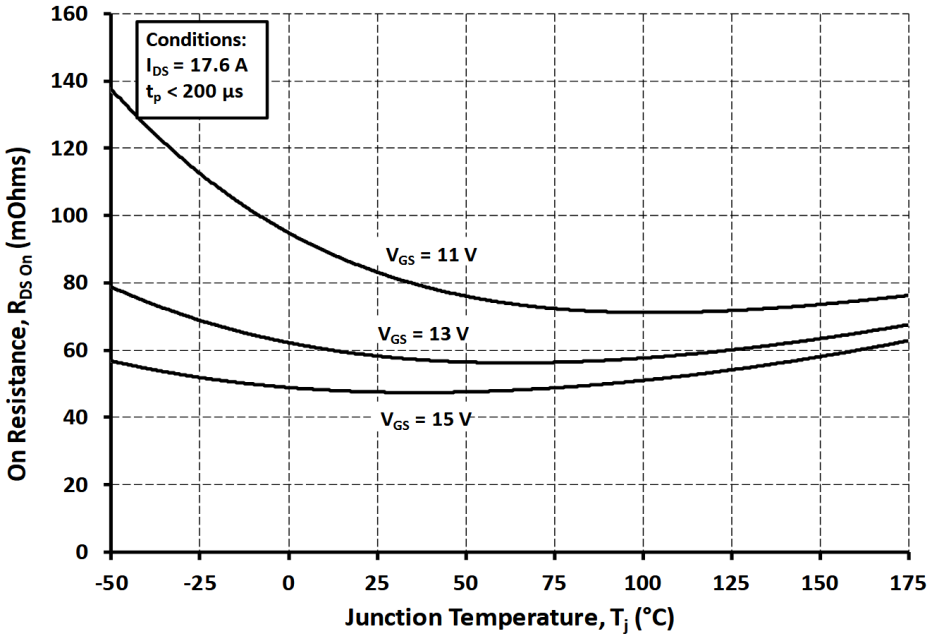


Figure 4.2: The Corrolation between On resistance and Gate Driver voltage shown for C3M0045065K [21]

As seen, the best turn on voltage is 15 V as this gives the lowest ON resistance, which is also the recommended voltage given by the datasheet shown in Table 4.1.
To turn of the MOSFET the gate source voltage has to be below the threshold voltage of 2.6 V as this is the point when the MOSFET changes from its conducting state to its blocking state. However, the recommended turn-off voltage, as seen in Table 4.1, is -4 V. This negative bias voltage is recommended in order not to have an accidental turn-on triggered as a result of voltage spikes during switching. The last requirement is a gate driver that can deliver enough current to turn on the switch fast enough. The required current can then be calculated using Equation 4.3.

$$I_p = \frac{V_{gs+} - V_{gs-}}{R_{IG} + R_{EG}} \tag{4.3}$$

Using the internal resistance and the recommended gate resistance together with the recommended gate voltage, the minimum required drive current is 3.45 A. To this end, the Infineon "2EDS9265H" gate driver is chosen. This driver features a dual channel setup such that each switch leg needs only one driver. The driver can source 4 A during turn on and sink 8 A during turn off and can supply up to 20 V across the gate source. Furthermore, this driver implements galvanic isolation between the control and power side. This is implemented for safety reasons as it decouples the signal ground from the power ground. Allowing the control side to be designed with a different ground reference than the power side. In addition, galvanic isolation also protects the control side circuit from transients that are present at the gate driver from the parasitic capacitance coupling between the gate and the drain. A block diagram of the gate driver is shown in Figure 4.3

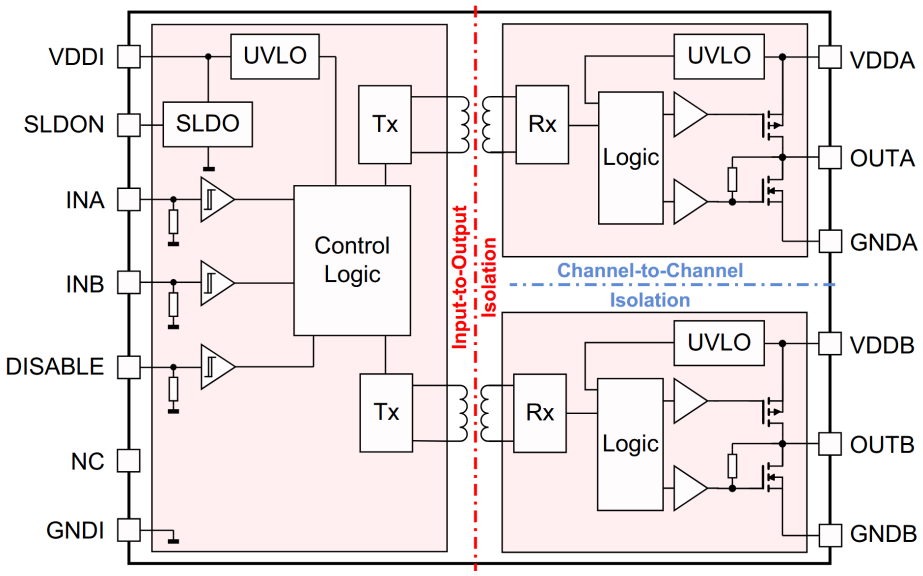


Figure 4.3: Block diagram of Infineon "2EDS9265H" gate driver [6]

The left side of the block diagram consists of the control signal ports; here, "InA" and "INB" are connected to the signal ports of the FPGA. To power the control side, a 3.3 V or 5 V signal is required at the "VDDI" port. To enable the 5 V supply mode "SLDON" is connected to ground and a 1 $k\Omega$ resistor is connected to "VDDI". The 5 V is supplied by the FPGA power pin. This is then connected to a common signal ground "GNDI". A filter capacitor is also connected between "VDDI" and "GNDI" to stabilize the voltage sufficiently, as recommended in the datasheet[6]. The right side of the block diagram consists of two isolated channels, which supply the gate source voltage to the MOSFETs. In order to supply the -4 V during the turn off, an external circuit is required for each channel which can provide a negative voltage bias, A schematic of the circuit is shown in Figure 4.4.

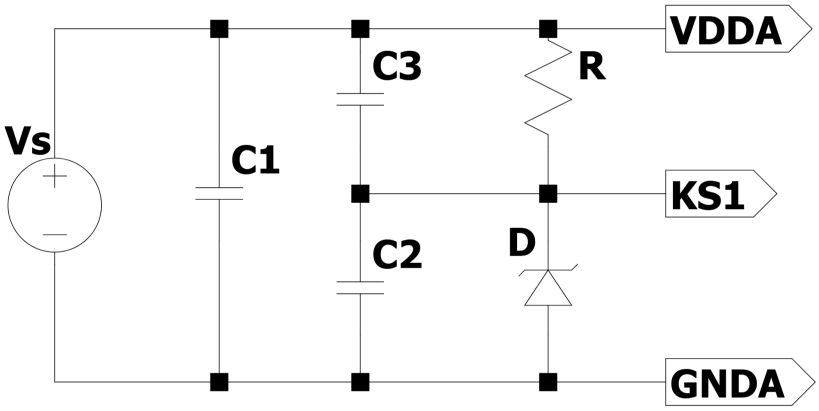


Figure 4.4: Negative bias voltage circuit using a Zener Diode

Across the circuit, an external voltage supply V_s is connected, which supplies the power to the gate driver. Here, $C1$ and $C3$ are connected to stabilize the source voltage. To obtain the negative bias during the turn off, a Zener diode D and a capacitor $C2$ are connected between the points "GNDA" and "KS1" where the breakdown voltage is chosen according to the desired turn of voltage and the capacitor stabilizes the voltage. Therefore, to obtain

the desired gate voltages the voltage supply V_s is set to 19 V and a Zener diode with a breakdown voltage of 4V is chosen so that the outputs are as follows.

$$V_{gs,on} = 19V - 4V = 15V \qquad (4.4) \qquad V_{gs,off} = 0V - 4V = -4V \qquad (4.5)$$

Before "OUTA" can be connected to the MOSFET, a gate resistor is needed. The chosen gate resistor is important because it determines how fast the switch turns on. This is especially important in order to reduce the time spent in the Miller plateau which occurs during each turn on and off cycle. This plateau is caused by the parasitic capacitance connected across the MOSFETs terminals and is an inherent effect of the MOSFETs structure. A schematic of a MOSFET with parasitic capacitance is shown in Figure 4.5.

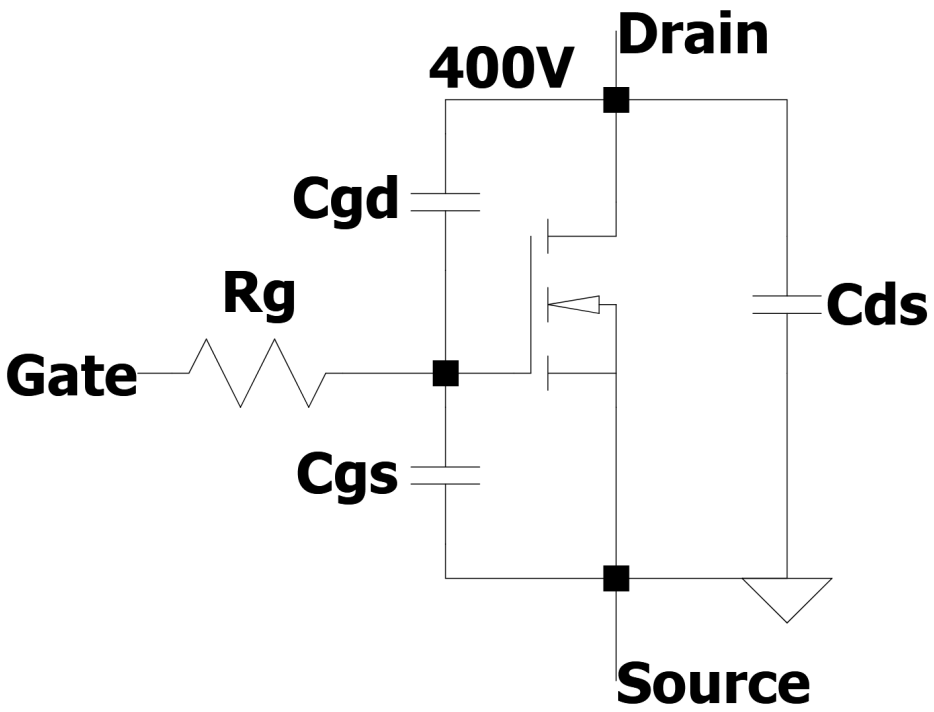


Figure 4.5: Illustration of MOSFET with parasitic capacitance blocking 400 V

In the example shown in Figure 4.5 the switch is turned off and 400 V is being blocked at the drain. At the gate, the voltage is -4 V since the switch is turned off. This causes the parasitic capacitance C_{gd} to charge until it reaches 400 V. As the voltage across the gate increases, the MOSFET begins to turn on. This causes the capacitor C_{gd} to become connected between the Gate and drain instead. As a result, there is now a -400 V potential between the gate and the source. This prevents the gate driver from increasing the voltage across the gate source until the capacitor charge has been depleted. This effect is shown in Figure 4.6

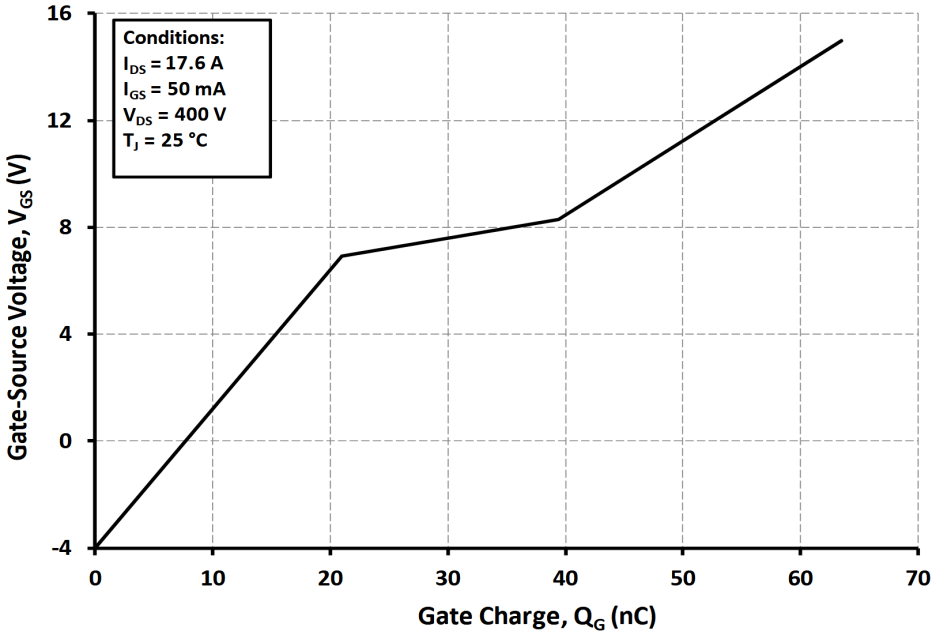


Figure 4.6: Gate charge characteristics shown for "C3M0045065K" [21]

Here, the voltage increases until the switch is turned on, at which point it only changes slightly as the gate charge increases. In this operating condition the switch losses are very high since the switch is conducting but at the same time the On resistance is also very high. In order to minimize losses, the time spent on the Miller plateau should be as low as possible. According to the datasheet, a 2.5 Ω gate resistor is recommended. However, a slightly larger 4 Ω turn-on resistor was selected to improve the gate driver's robustness against ringing during each switching cycle. In parallel with the turn-on resistor, there is a diode and a separate 4 Ω resistor. This configuration reduces the effective gate resistance during the turn-off to 2 Ω, allowing for a faster turn-off time. The fast turn-off in conjunction with the dead time helps to prevent both MOSFETs from being on simultaneously, thereby avoiding shoot-through conditions. A schematic of the gate circuit is shown in Figure 4.7.

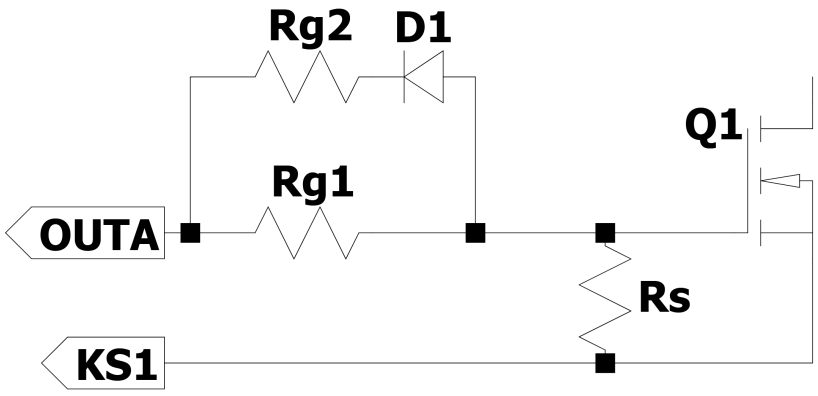


Figure 4.7: Schematic of gate resistor circuit

In figure 4.7, the gate resistor circuit is connected to "OUTA" which is the output terminal of the gate driver. The source is connected to "KS1" in the Zener diode circuit to provide the negative bias voltage during turn-off. Between the terminals is a 10k Ω pull-down

resistor R_s, which is there to allow the gate driver to discharge when the voltage is zero. These gate resistor values are used for both the HF leg MOSFETs Q1 and Q2. For the LF leg, a simple 15 Ω resistor is used to turn on and off. A lower value is not necessary because of the very low frequency and because switching only occurs during zero current and voltage, it is therefore not necessary to have an aggressive value since switching losses will be negligible.
As mentioned, the gate driver needs a power supply, which will be provided by an external source. Directly connecting the supply to the gate driver is fine for the low side MOSFET since the source of switch Q2 is connected to the ground. However, this is not possible on the high-side MOSFET Q1 because of the dynamic happening when Q2 turns off. An example of this is shown in the schematic in Figure 4.8

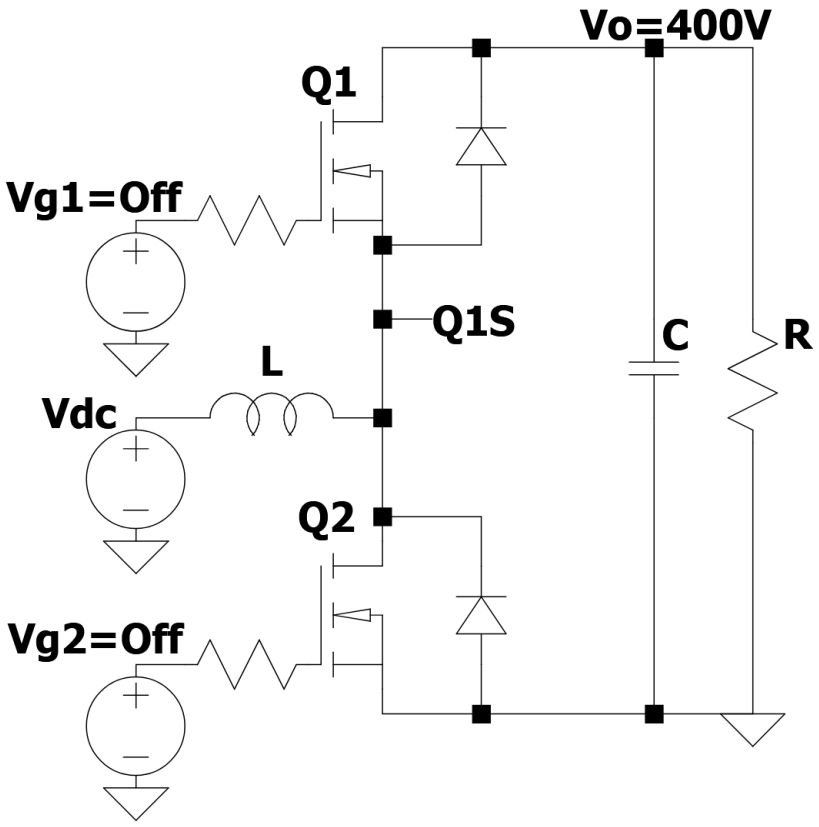


Figure 4.8: Illustration of the high-side switching problem, $Q1S$ node floats when Q2 turns off

As Q2 is turned off, node Q_{1S} is no longer grounded and instead floating. The voltage at this point is now equal to $V_{Q1S} = V_L + V_{dc} \approx 400V$ and the current flows through the body diode of Q1. At this point V_{g1} turns on so that Q1 conducts. However, because V_{g1} is grounded to the same reference as the power side, the voltage across V_{g1} has to be equal to $V_{g1} = V_L + V_{dc} + 15V \approx 415V$. in order for $V_{gs,Q1} = V_{g1} - V_{Q1S} = 15V$. As such, simply connecting a power supply across the high-side gate driver terminals would not be possible as the resulting voltage required is too high. To solve this issue, an isolated power supply is connected between the external power supply and the gate driver. For this the Murata "MGJ1D241505MPC" is chosen. This isolated DC-DC power supply is galvanically isolated between the input and output so that the external power supply can safely be connected without exceeding the voltage limit.

4.3 Passive Component Dimensioning

The choice of inductor and capacitor is an important design consideration, as together with the switching frequency, they govern the current and voltage ripple seen in the converter. Therefore, the relationship between the component values and the frequency should be derived so that an acceptable ripple can be achieved. The derivation will be based on the converter operating in the DC-DC configuration.
The inductors function is to keep the input current stable during the different switching states of the converter by limiting the rate of change of the current. In addition, for a short time period, the inductor acts as a current source. As such, charging it will force a current to flow. The magnitude of this current is determined by the time that is spent charging the inductor. Since a current is forced to flow, the voltage across the inductor has to rise. This behavior can be derived from Equation 4.6.

$$V_L = L \cdot \frac{\partial I_L}{\partial t} \tag{4.6}$$

As seen in Equation 4.6, the rate of change in current depends on the voltage across the inductor and the inductance. As such, the change in current over time must then be the rate of change multiplied by a given time span. In the DC-DC charging state, the voltage across the inductor V_L can be replaced with the input voltage V_S as they are equal. This gives Equation 3.1, which was used to derive the duty cycle in the DC-DC configuration. To find the inductance value, the equation can be isolated for L giving Equation 4.7.

$$L = \frac{V_s \cdot D_{Q2} \cdot T}{\Delta I_L} \tag{4.7}$$

Substituting D_{Q2} with Equation 3.7 and the period T with $1/f_s$ gives Equation 4.8.

$$L = \frac{V_s \cdot (V_o - V_s)}{V_o \cdot \Delta I_L \cdot f_s} \tag{4.8}$$

Using this equation, the maximum level of ripple current can be set and the required inductance can then be found.
A capacitor is connected to the output terminals. This serves to stabilize the output voltage by limiting its rate of change. When the inductor is discharging, it supplies power to the capacitor, which in turn increases the voltage across it. The capacitor acts as a voltage supply that supplies power to the load while the inductor is in its charging state. The capacitor ripple voltage can be derived from Equation 4.9

$$I_C = C \cdot \frac{\partial V_C}{\partial t} \tag{4.9}$$

To obtain the voltage change of the capacitor during the charging state of the inductor, Equation 4.9 is multiplied by period T and duty cycle D_{Q2}. Furthermore, the change in capacitor voltage ΔV_C can be replaced by the change in output voltage ΔV_o since they are the same. Isolating for C gives Equation 4.10.

$$C = \frac{I_C \cdot D_{Q2} \cdot T}{\Delta V_o} \tag{4.10}$$

Then D_{Q2} is substituted with Equation 3.7 and the period T with $1/f_s$. Furthermore, the current of the capacitor I_C is equal to the output current I_o during the charging state of the inductor and since I_o is equal to V_o/R_o this can be substituted, giving Equation 4.11.

$$C = \frac{V_o - V_s}{R_o \cdot \Delta V_o \cdot f_s} \tag{4.11}$$

The final capacitor equation is derived and can be used to achieve the desired ripple voltage.
The inductor and capacitor values can now be calculated according to the Migatronic requirements given in Table 2.1.

4.3.1 Selection of Capacitor and Inductor

According to the Migatronic design requirements, the maximum voltage ripple should be $\pm$ 20 V. To achieve this when running in the DC to DC configuration, the capacitor should be a minimum of 0.975 μF. In this project, the "C4AQHBU4330P1WJ" capacitor from KEMET is chosen. This has a higher capacitance of 3.3 μF[12], which will give a lower voltage ripple of 5.8 V. This was chosen because it was available in the lab at the time and because it had a breakdown voltage of 600 V, which is suitable for the voltages of this project.
In order to obtain a ripple current between 10-20 % the inductance needs to be between 313 and 627 μH. A self-made inductor from a previous project was already available; however, before choosing it, two tests are conducted on the inductor in order to find its DC resistance and inductance.
This is shown in Figure 4.9 where a DC voltage is supplied across the inductor. Then, current and voltage are measured to determine the DC resistance.

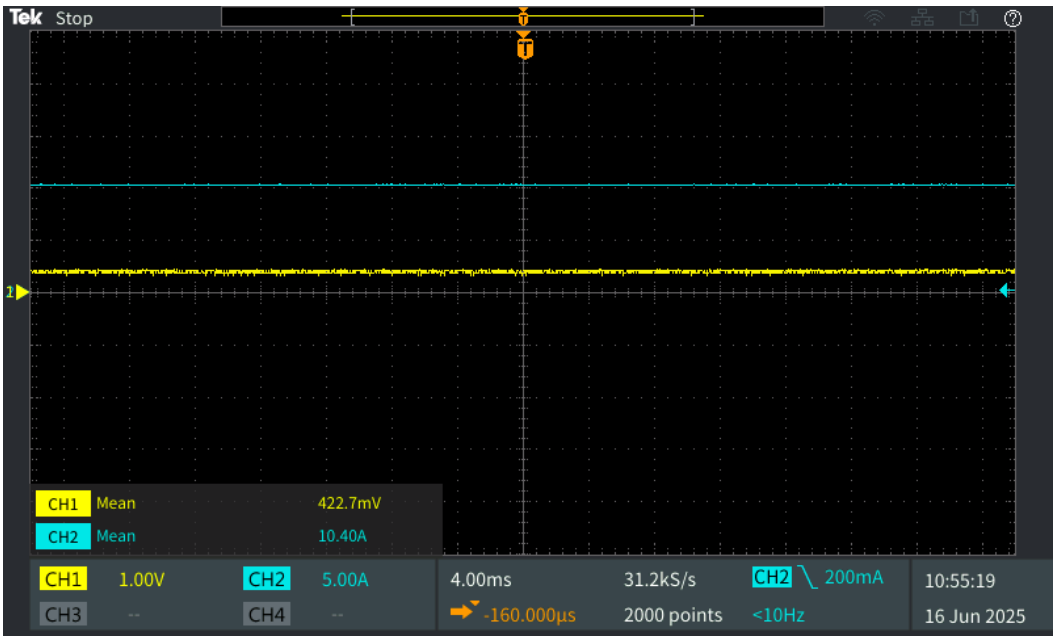


Figure 4.9: DC Voltage applied across the inductor

According to Figure 4.9, the voltage is 0.4227 V and the current is 10.40 A. From this, the resistance is calculated as $R_{DCR} = 40.6$ mΩ.
Next, a 50 Hz sine wave voltage is applied across the inductor and the voltage and current is measured, this is shown in Figure 4.10. It can also be seen that the inductor is not saturating.

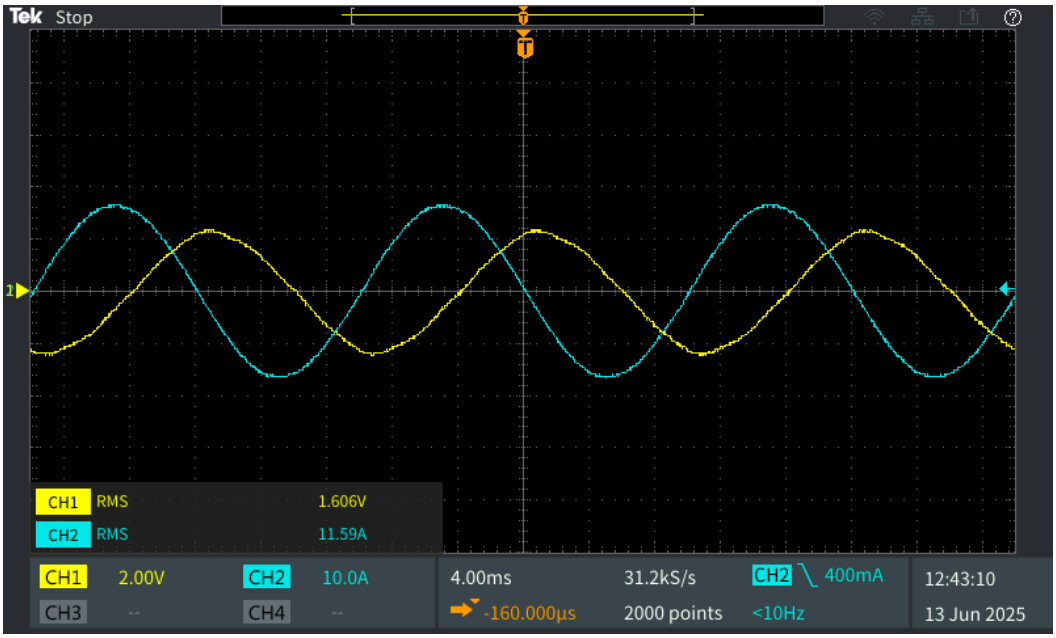


Figure 4.10: 50 Hz Sine wave applied across the inductor

According to Figure 4.10. The RMS voltage and current are 1.606 V and 11.59 A, respectively. Since the voltage magnitude is given as equation 4.12.

$$V = Z \cdot I = \sqrt{R_{DCR}^2 + (2 \cdot \pi \cdot 50 \cdot L)^2} \cdot I \tag{4.12}$$

With the DC resistance, AC current, and AC voltage known, the inductance of the inductor can be calculated by rewriting equation 4.12 to equation 4.13.

$$L = \frac{1}{2 \cdot 50 \cdot \pi} \cdot \sqrt{\frac{V^2}{I^2} - R_{DCR}^2} \tag{4.13}$$

The inductance is then calculated as 421 μH, which will give an expected ripple current of 2.32 A, which is equivalent to 14.8 % and is within the requirement. The final values for the inductor and capacitor are given in table 4.2.

Component	Inductance / Capacitance	Resistance
Inductor	421μH	40.6 mΩ
Capacitor	3.3μF	18.7mΩ

Table 4.2: Component parameters for the inductor and capacitor[12]

With the inductor and capacitor chosen, all major components of the converter have been selected. In order to verify the converter operation and performance, an LTspice simulation model is built using the parameters of the chosen components.

Simulation-Based Verification of Converter and Thermal Design

With the creation of the control code, the sizing and test of the inductor and choice of capacitor, the choice of MOSFETs and design of gate driver system finished, a detailed simulation model of the converter is created in LTspice. This includes manufacturer-made MOSFET and gate driver models that approximate the real-life performance of the devices. This simulation model serves to estimate the performance that can be expected during laboratory operation. Finally, the estimated switch losses will be used to determine an appropriate heat sink. A schematic of the Full Model is given in Appendix A.

5.1 Simulation of Converter in DC-DC Configuration

First, the model is simulated in DC-DC configuration to test the gate driver voltages, the voltage boost capability, and the ripple voltage and current. A list of control parameters and component values is given in Table 5.1.

Parameter	Variable	Value
Input Voltage	V_s	230 V
Output Voltage	V_o	400 V
Switching Frequency	f_s	100 kHz
Dead Time	t_d	83 ns
Inductance	L	421 μH
Capacitance	C	3.3 μF
Load Resistor	R	44.44 Ω

Table 5.1: Control parameters and component values used, The ESR of the capacitor and DCR of the inductor is included

A graph of the output voltage and current is shown in Figure 5.1. It can be seen that there is an initial output voltage of 226 V and an output/inductor current of 5 A, even though the initial conditions are set to 0. This happens because the Q4 switch is always on, causing the voltage source to be connected to the ground. Furthermore, the Q1 diode allows the current to flow immediately. Lastly, since the source is DC, the inductor is short-circuited, and the capacitor is open-circuited. All of this leads to the voltage source being connected across the load through a body diode. This causes the output voltage to be equal to the voltage source minus the diode forward voltage drop. This in turn leads to the initial current that is seen.

As shown, there is some transient during startup, but the converter reaches steady state after approximately 1.5 ms. The output voltage reaches an average voltage of 397 V. This is slightly lower than 400 V and is most likely due to component losses. However, this is still close to the target output voltage. The voltage ripple is $\pm$5.85 V, which is also very close to the calculated value for a 3.3 μF capacitor. Similarly, the average output current is 9 A, which in turn gives an average output power of 3552 W. From this, it is shown that the correct output voltage, power, and voltage ripple is achieved.

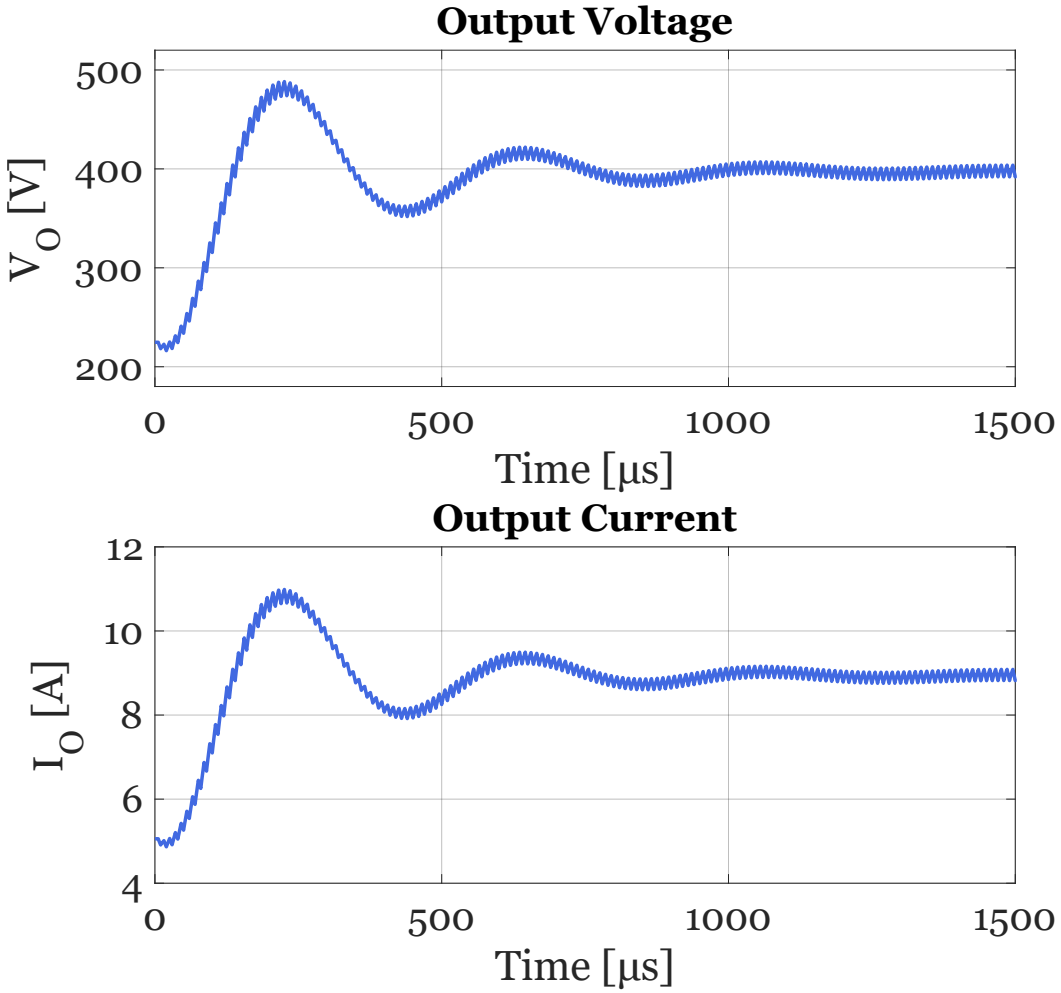


Figure 5.1: Output voltage and current

A graph of the drain source voltages of Q1 and Q2 is shown in Figure 5.2. As shown, the voltage of each switch is stable and no spikes are present in the voltage signals, and they follow the expected duty cycle. Figure 5.2 also shows the drain current of Q2, where there is a spike in the current when Q2 turns on. Before Q2 turns on, Q1 is conducting through the body diode as a result of the dead-time, as a result when Q2 turns on, the Q1 body diode begins to conduct in the opposite direction to clear the forward voltage across the diode. As such, the current spike is caused by the reverse recovery of the body diode in Q1. This spike is approximately 35 A and is well within the rated pulse current of the "C3M0045065K" MOSFET which is 132 A according to the Datasheet [21].

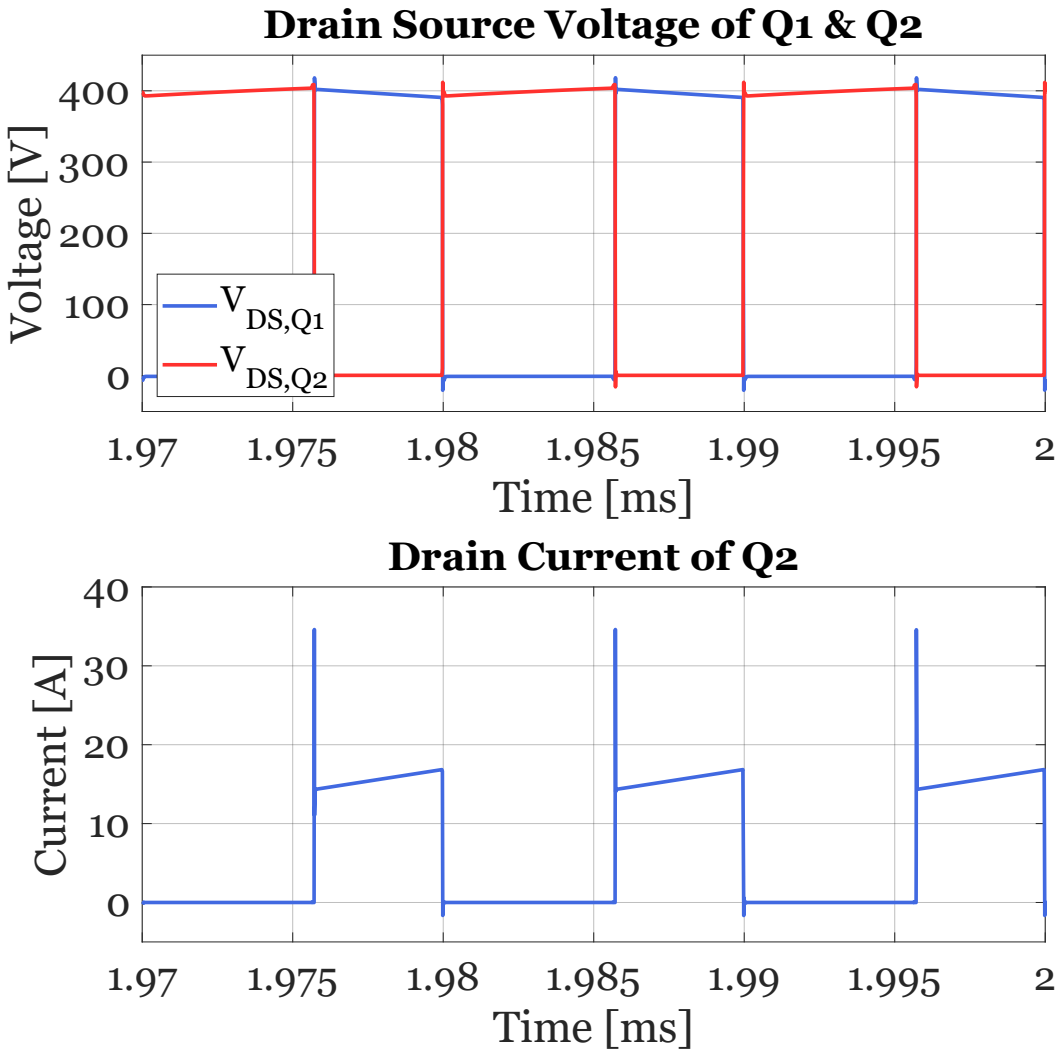


Figure 5.2: Drain source voltage and drain current of switches Q1 and Q2 during steady state.

In Figure 5.3 it is shown that the inductor current initially overshoots, this is due to the output voltage being lower than 400 V during start-up. This causes the inductor to initially discharge slower than expected, since the duty cycle is calculated on the basis of a 400 V output. The overshoot during start-up could be removed by varying the duty cycle with respect to the initial output voltage. The inductor reaches a steady state value of 15.6 A with a current ripple of 2.34 A, which is very close to the calculated current ripple.

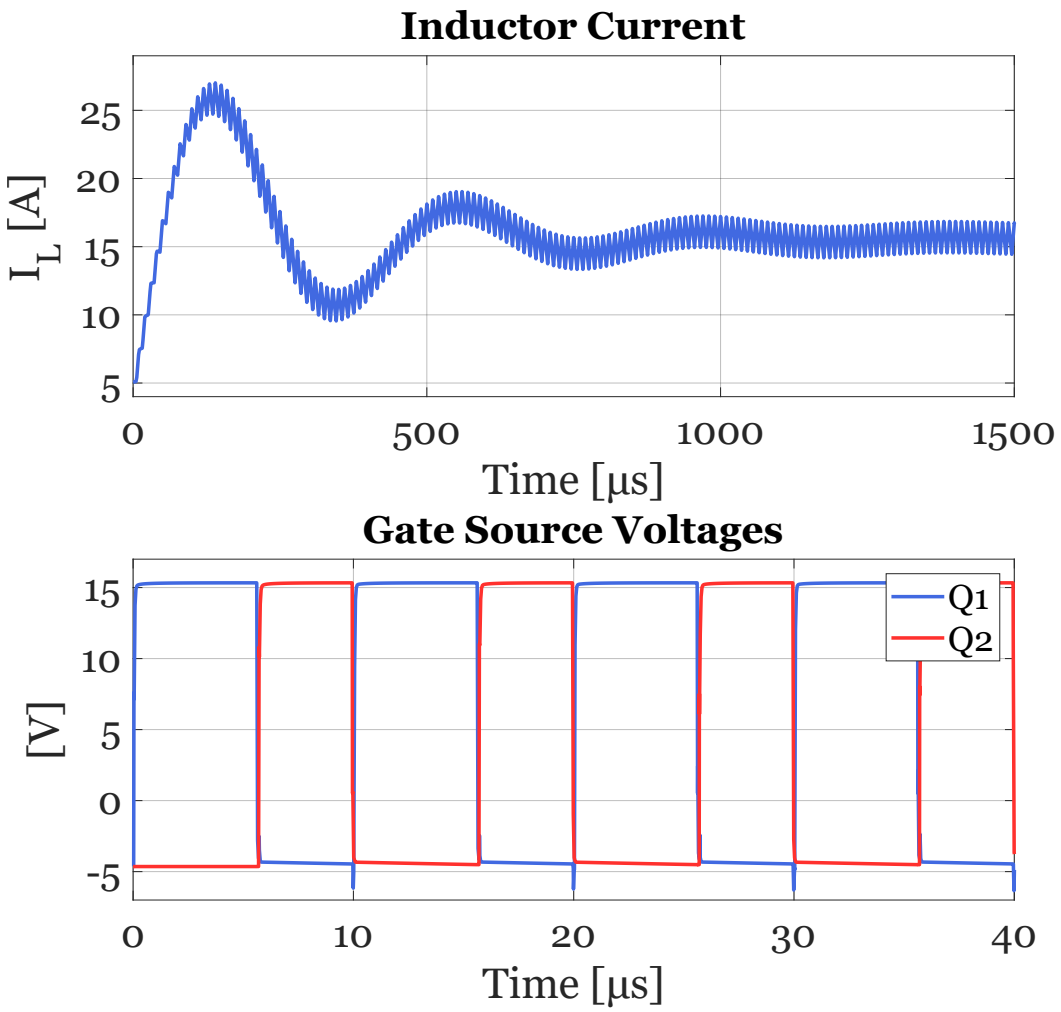


Figure 5.3: Inductor current and gate control signals

As shown in Figure 5.3 the Gate source voltage is 15 V during turn-on and goes to -4 V at turn-off. As this is the desired output, the gate driver circuit is functioning as intended. From this it is shown that the converter correctly raises the output voltage to the desired level and that the inductor current settles to the expected value. Furthermore, the voltage and current ripple is very close to the calculated ripple.

5.2 Simulation of Converter in Inverter Configuration

A simulation of the converter model in the inverter configuration is performed to validate that the output voltage waveform and amplitude are correct. In addition, component losses and converter efficiency will be simulated. The simulation is tested using the parameters shown in Table 5.1. With the exception that the input voltage and the desired output voltage are opposite and have a load resistor of $R = 14.7\Omega$. The output voltage and current are shown in Figure 5.4.

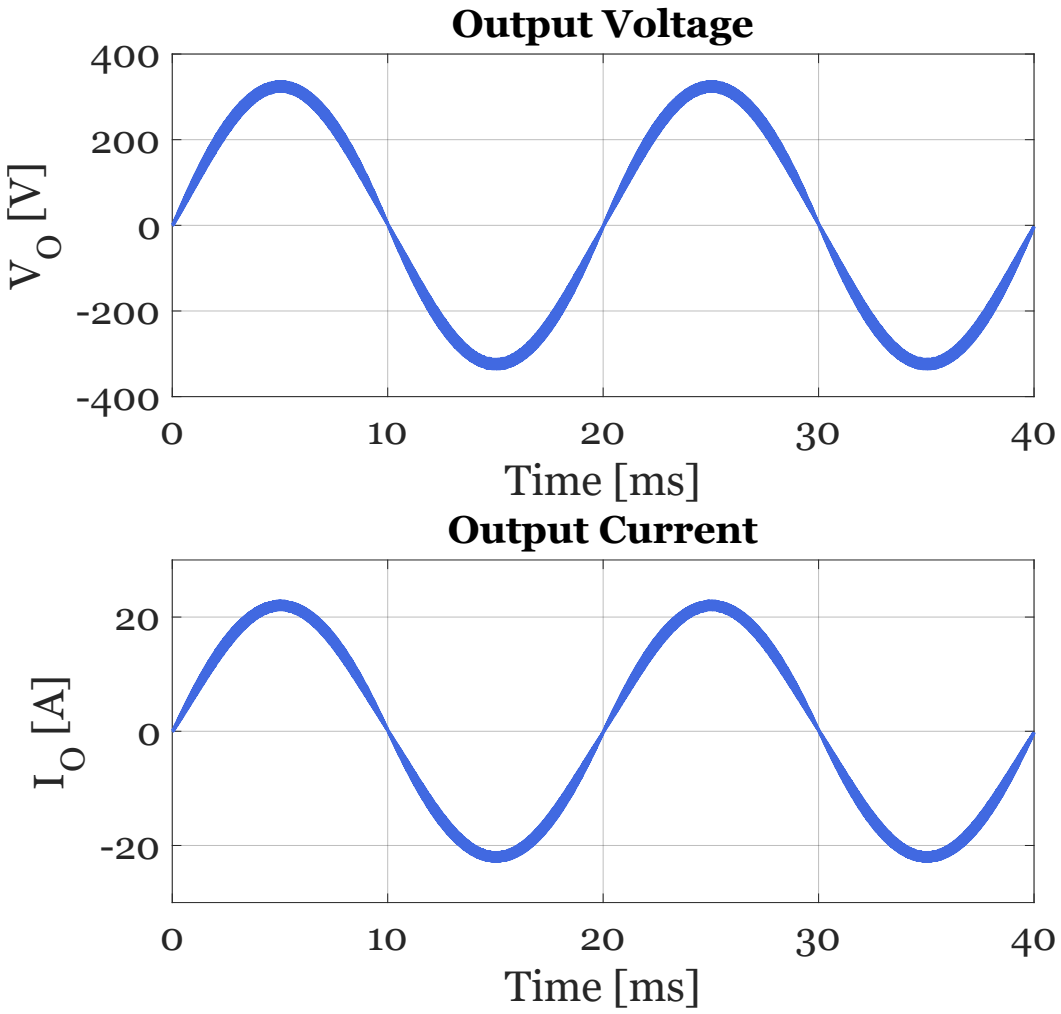


Figure 5.4: Output voltage and current of converter

As seen, the output voltage reaches a peak value of 323.8 V and the current reaches 21.9 A. This gives an RMS voltage and current of 228.9 V and 15.48 A, respectively. In addition, the maximum voltage and current ripple are 33.8 V and 2.25 A. The voltage ripple is significantly larger in the inverter configuration because it is dependent on the current ripple. To determine the expected efficiency of the converter, the power loss of all MOSFETs and passive components is measured. A bar graph of the results is shown in Figure 5.5.

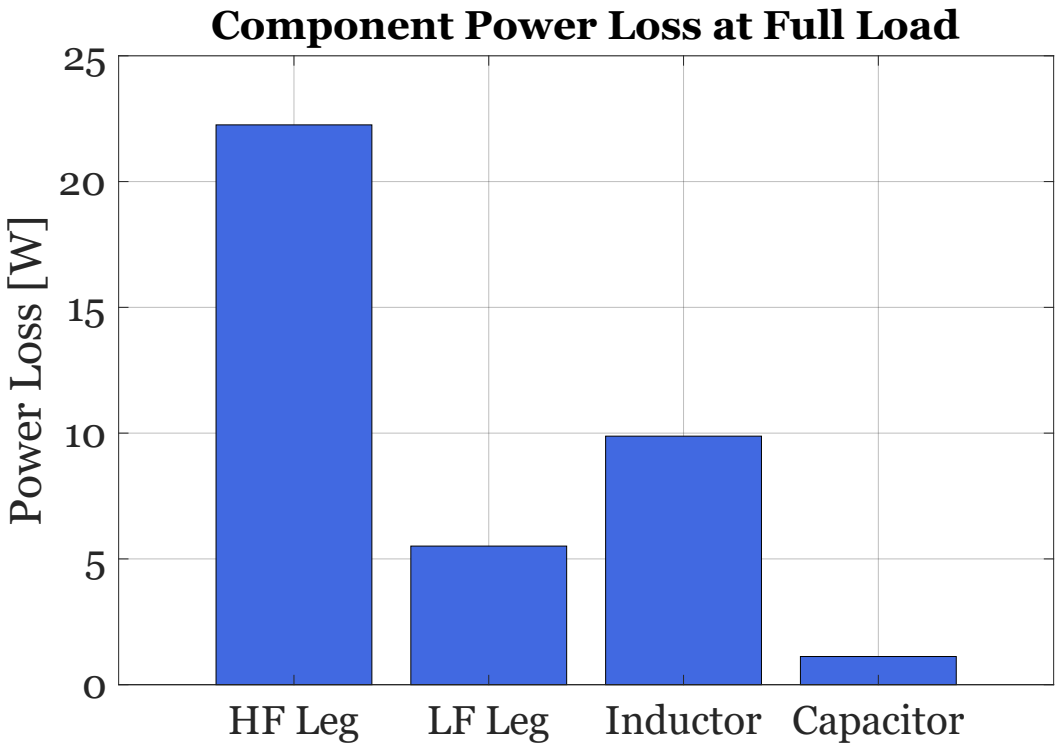


Figure 5.5: Simulated component losses. showing MOSFET, inductor and capacitor losses

According to the graph, most of the losses are in the HF leg, consisting of MOSFETs Q1 and Q2. This is as expected since there are both switching and conduction losses. The LF losses are approximately 5 W, which comes purely from conduction. In addition, there are also copper losses in the inductor coil, which is 10 W. Lastly, the loss of the DC link capacitor is approximately 1 W. This gives a total loss of 38.7 W. With this, the converter efficiency can be calculated and the total converter efficiency is 98.9 %.

5.3 Thermal Design

During converter operation, both switching and conduction losses generate heat, causing the temperature of the MOSFETs to increase over time. To prevent overheating, a heat sink is required. To estimate the required size of the heat sink, a thermal equivalent circuit is created. Here, the simulated switch and conduction losses and the thermal characteristics of the MOSFETs are used to determine the expected junction temperature. The thermal data for the MOSFETs are given in Table 5.2.

MOSFET Type:	C3M0045065K	C3M0025065K
Thermal Resistance R_{JC} [°C/W]	0.85	0.46
P_H High Side [W]	11	2.5
P_L Low Side [W]	11	2.5
R_{on} at 25 °C	45	25
R_{on} at 100 °C	49.5	27.5

Table 5.2: Thermal Resistance from junction to case, Simulated Power loss and On resistance according to temperature [21] [20]

According to the Datasheet of both MOSFETs the lowest On resistance is at 25 °C, however, this only increases slightly at a junction to case temperature of 100 °C as shown in Table 5.2.

For this reason a maximum junction to case temperature of 100 °C is chosen. Assuming an ambient temperature of 25 °C, a thermal equivalent circuit is created to determine the required thermal resistance of the heat sink, to avoid exceeding the maximum junction temperature. A schematic of the thermal equivalent circuit is shown in Figure 5.6.

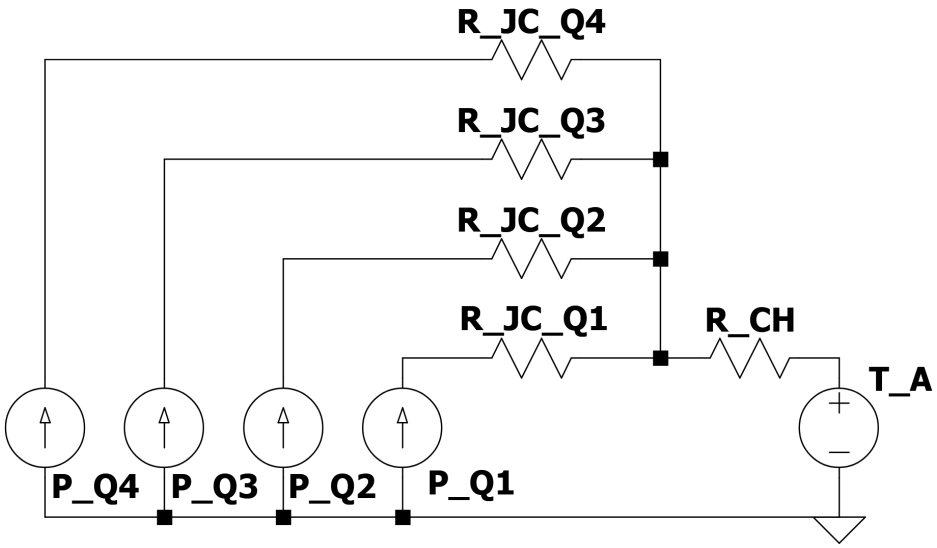


Figure 5.6: Thermal equivalent circuit of the 3 operating MOSFETs

The thermal equivalent circuit consists of 4 parallel current sources, each representing the power loss of their respective MOSFET. In series with each current source is the junction-to-case resistor of each MOSFET. The output of each branch converges at a common node, which is connected to a shared case-to-heat sink thermal resistor. Lastly, a voltage source representing the ambient temperature is connected. Since MOSFET Q1 has the highest power loss of 11 W and the highest junction-to-case thermal resistance, the thermal resistance of the heat sink is calculated with respect to it. From figure 5.6 the thermal equation can be derived as 5.1.

$$T_{JC,Q1} = P_{Q1} \cdot R_{JC,Q1} + (P_{Q1} + P_{Q2} + P_{Q3} + P_{Q4}) \cdot R_{CH} + T_A \tag{5.1}$$

Given that the power loss for all MOSFETs P_{Q1} P_{Q2} P_{Q3} P_{Q4}, the desired junction to case temperature $T_{JC,Q2}$, the ambient temperature T_A and junction to case thermal resistance R_{JC} are known variables. The required thermal resistance of the heat sink R_{CH} can be found by rewriting equation 5.1 into equation 5.2.

$$R_{CH} = \frac{T_{JC} - R_{JC,Q1} \cdot P_{Q1} - T_A}{P_{Q1} + P_{Q2} + P_{Q3} + P_{Q4}} \tag{5.2}$$

Using equation 5.2, the thermal resistance of the heat sink is calculated as $R_{CH} = 2.43$ C/W. Using this value, the junction to case temperature of each MOSFET can be calculated and is given in Table 5.3.

MOSFET	Junction to Case Temperature [°C]
Q1	100
Q2	100
Q3	91.78
Q4	91.78

Table 5.3: The calculated junction to case temperature of each MOSFET With a heat sink thermal resistance of 2.43 $°C/W$

With the thermal resistance of the heat sink calculated, a heat sink model is chosen. To this end, the "OMNI-UNI-30-50-D" from "Wakefield Thermal" is selected. This is a large heat sink that can be placed across 4 MOSFETs simultaneously. The thermal resistance is 2.4 $°C/W$ at an air flow velocity of 100 linear feet per minute (LFM), which can be achieved with a small fan [16]. The expected temperature of the heat sink is 90 °C.

With the converter model tested through simulation, it is shown that the converter operates as expected and that the efficiency at full load is 98.9 %, which exceeds the Migatronic requirement of 97 %. In addition, a thermal design was created based on component losses. Therefore, to test the converter, a PCB is designed in order to experimentally validate the converter performance.

PCB Design and Experimental Results

6.1 PCB Layout

For the converter a 2-layer PCB is used. This was chosen because the laboratory had a 2 layer PCB maker tool available in-house, which allowed PCB designs to be quickly created and evaluated in the laboratory. As such, many of the design considerations were made with this in mind. During the design process, the three main circuits considered were the control circuit, the gate driver circuit, and the power circuit. Each of these circuits were designed with the intent of minimizing interference from the power circuit to the gate driver circuit and control signals. A schematic of the PCB is shown in Figure 6.1.

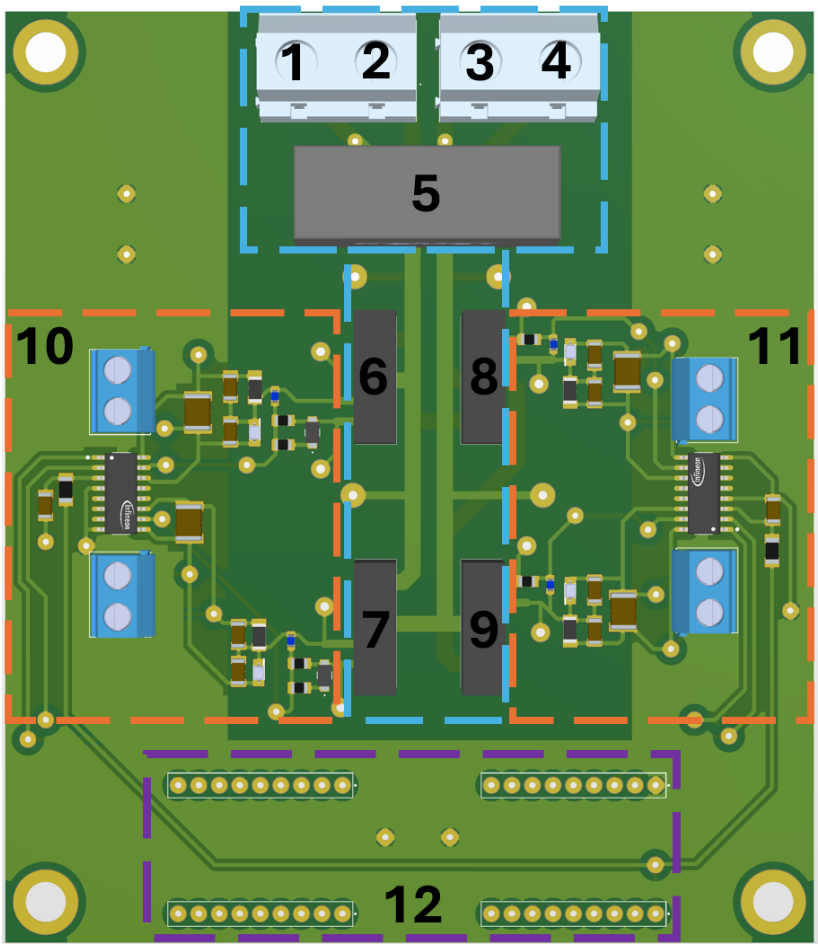


Figure 6.1: 3D representation of the PCB with components, the blue outline shows power circuit, the orange outlines shows gate driver circuits, and the purple shows the controller placement

The power circuit was designed with both input and output terminals located on the same side of the PCB. Terminals 1 and 4 are designated as inputs, while terminals 2 and 3 serve as outputs in the DC-DC configuration and opposite in the inverter configuration. This is shown in Figure 6.1. This configuration was chosen for several reasons. It reduces the number of vias required in the power plane by minimizing trace crossings, thereby simplifying the overall routing. Additionally, it allows all power traces to remain within

the MOSFET bridge area, which allows the gate driver circuit to be placed outside this region. This separation simplifies the gate driver layout by eliminating the need to route around high-current power traces. Finally, placing all terminals on one side ensures that the bottom area of the PCB remains free of power traces, making it an ideal location for the controller circuit. The DC link capacitor, denoted component 5, and the MOSFET bridge are placed as close as possible to the output terminals to minimize trace lengths. This helps reduce parasitic inductance to reduce voltage ringing during switching transitions. The MOSFETs labeled 6 and 7 form the HF leg, while 8 and 9 form the LF leg. The spacing and alignment of the MOSFETs are set according to the dimensions of the heat sink positioned between them.
The gate driver circuits denoted with 10 and 11 were designed to be as close to the MOSFETs as possible; this was done to reduce the trace length and thereby minimize the parasitic inductance. In addition, the gate driver circuits were placed perpendicular to the power traces to minimize crosstalk from the power circuit to the gate driver circuit. The controller circuit where the FPGA is located is placed at the bottom of the PCB to ensure distance between the weak control signals and the power traces. Across the rest of the PCB, on both the top and bottom sides, a large copper plane is poured, which is used as a ground reference for the control signals.
An additional PCB is created for the isolated power supplies that are connected to the high-side MOSFETs. This is shown in Figure 6.2.

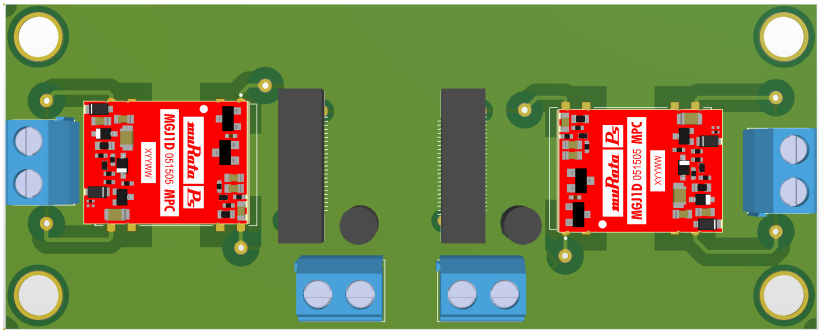


Figure 6.2: 3D representation of the gate driver power supply PCB. Consisting of the Murata isolated power supply and an LC filter

LC filters are placed on the input, placed between the isolated power supplies and the external supply. These circuits are there to stabilize the external supply. The isolated power supplies are connected to output terminals which are then connected to the high side gate driver circuit's power terminals. With the PCB finished the converter can be tested.

6.2 Test of Converter in DC-DC Configuration

This section aims to test the converters operation in DC-DC configuration with the goal of verifying the converters performance regarding gate driver signals, voltage boosting capability, high power operation, and estimation of efficiency.

6.2.1 DC-DC gate driver signals

The gate source voltages of Q1 and Q2 are shown in Figure 6.3 represented by "CH1" and "CH2", respectively. As shown in the graph, the gate source voltage of Q1 changes between 15.6 V and -3.6 V, while Q2 changes between 14.4 V and -3.6 V. This slight difference is

due to the isolated power supply used to power the gate driver of Q1. The isolated supply has its own zener diode connected, which slightly changes the voltage. However, the gate source voltages of Q1 and Q2 are close to the recommended values and can be used to drive the converter. Furthermore, the frequency is above 99 kHz and is very close to the target value.

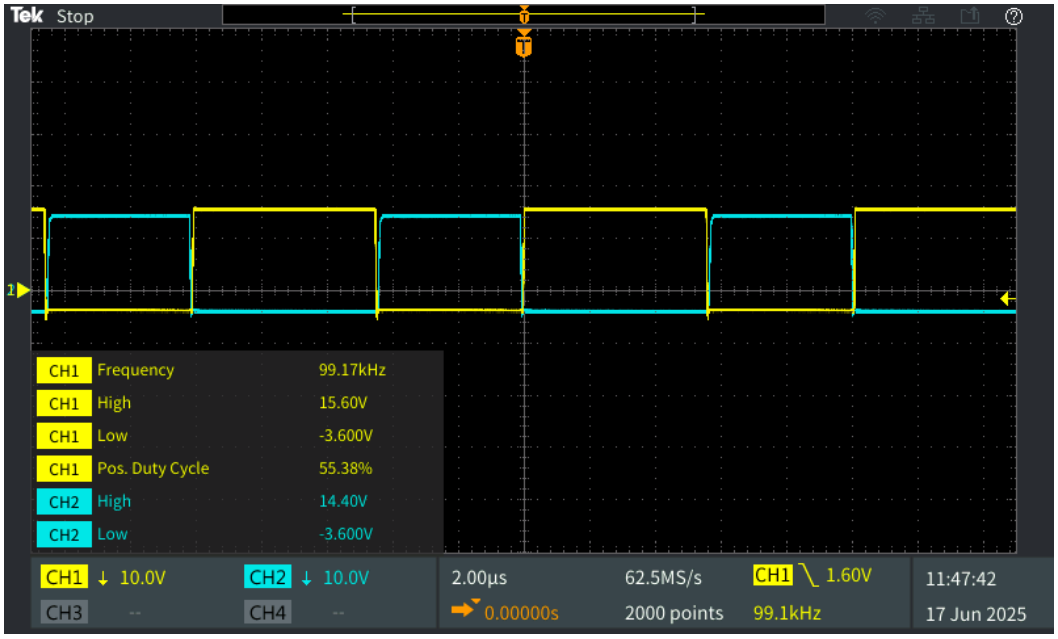


Figure 6.3: Gate source voltage of Q1 and Q2 showing correct voltage ranges and switching frequency

Looking at Figure 6.4, the rise time of Q1 and the fall time of Q2 are 31 ns each. Furthermore, the dead time is 77 ns, and, as seen, the voltage of Q2 is -3.6 V before Q1 turns on.

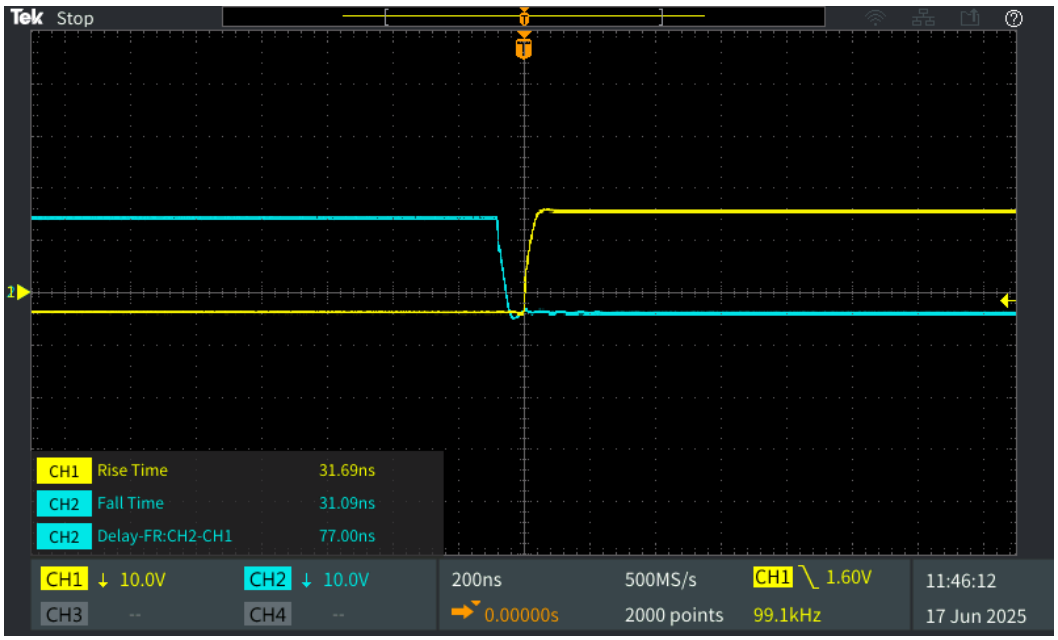


Figure 6.4: Gate source voltage fall and rise time of Q1 and Q2 and dead time, showing no crossover between signals

Figure 6.5 shows the fall time of Q1 and the rise time of Q2. Comparing the rise and fall time of Q2 with Q1 it can be seen that Q2 is significantly slower. This is because the gate resistors of Q2 were changed from 4 Ω to 8 Ω during testing. This was done because of voltage ringing of the gate source of Q2 and so to limit the amplitude the resistance was increased.

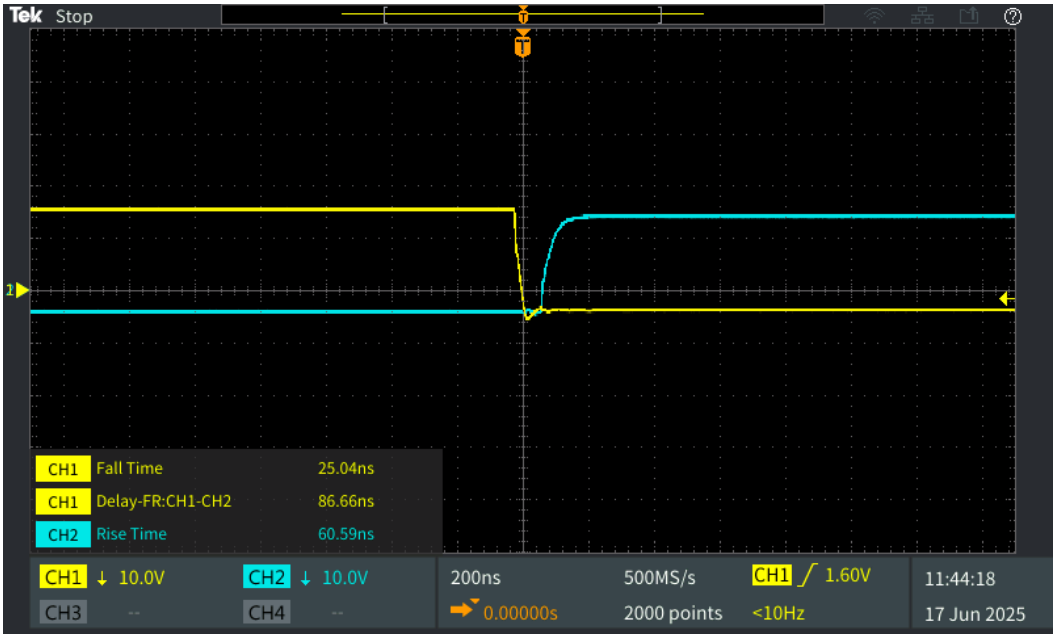


Figure 6.5: Gate source voltage rise and fall time of Q1 and Q2 respectively, showing different switching speeds as a result of higher gate resistance on Q2

According to the gate driver results, the gate source voltages are operating within the correct voltage range, and the frequency is very close to 100 kHz. Furthermore, there is sufficient dead time for the voltage to rise and fall separately.

6.2.2 Drain source voltage of Q1 and Q2

The drain source voltage of switches Q1 and Q2 is shown alongside their respective gate driver voltage in Figure 6.6. As shown, the Q1 drain source voltage represented by "CH1" changes from 0 to 396 V during the switching transition from on to off. Likewise, the drain source voltage of Q2 represented by "CH2" also changes from 0 to 396 V. Additionally, the gate source voltage signals Q1 and Q2 represented by "CH3" and "CH4" respectively are switching between 15 V during turn on and -4 V during turn off. Furthermore, there is a delay between when the gate source voltage of Q1 falls to -4 V and when the drain source voltage of Q1 rises, this is because of the dead-time period, causing the Q1 body diode to conduct, and therefore the voltage across Q1 is still low. However, as soon as the gate source voltage of Q2 increases, the drain source voltage of both Q1 and Q2 changes. This is expected behavior and indicates that the converter is operating as expected. During the turn-off period of both Q1 and Q2, there is voltage ringing. This is most prevalent across switch Q1 and a zoomed-in look of the Q1 drain source voltage is shown in Figure 6.7.

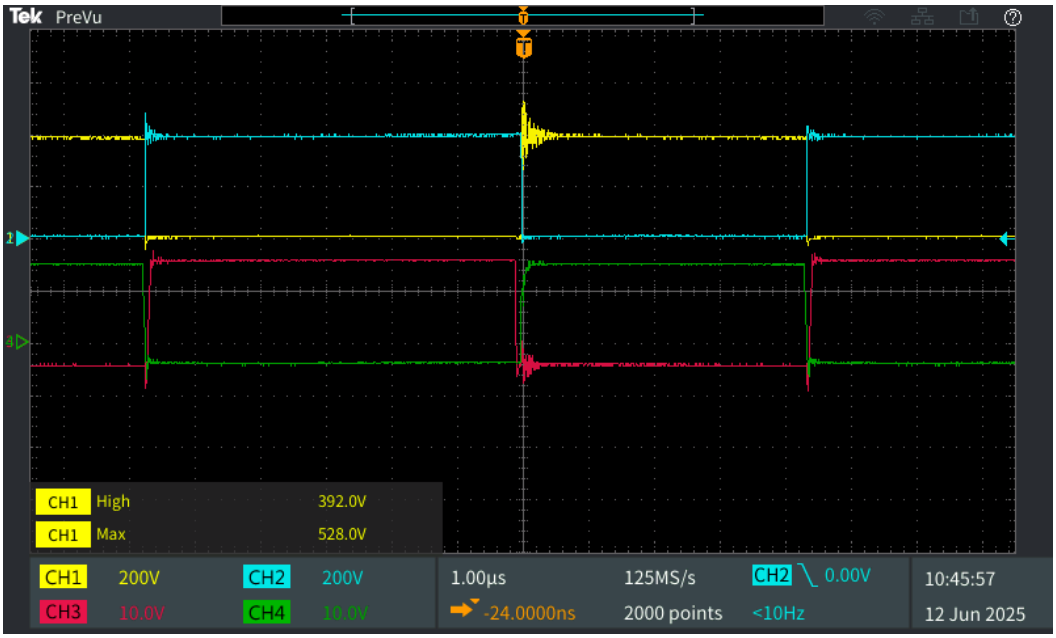


Figure 6.6: Drain-source voltage and gate driver voltage of Q1 as "CH1" and "CH3" and Q2 in "CH2" and "CH4".

As shown in Figure 6.7. There is significant ringing of the voltage when Q1 is turned off. Here, the amplitude is 528 V which is equivalent to and overshoot of 136 V. Since the breakdown voltage of the MOSFET is 650 V, this spike is not enough to destroy the MOSFETs. However, this ringing also propagates into the gate source voltage of Q1. This can be problematic as it can increase the chance of accidental turn-on, which in turn increases losses and can damage the converter if the capacitor is shorted to ground. As such, to improve the performance of the converter, the voltage ringing should be minimized.

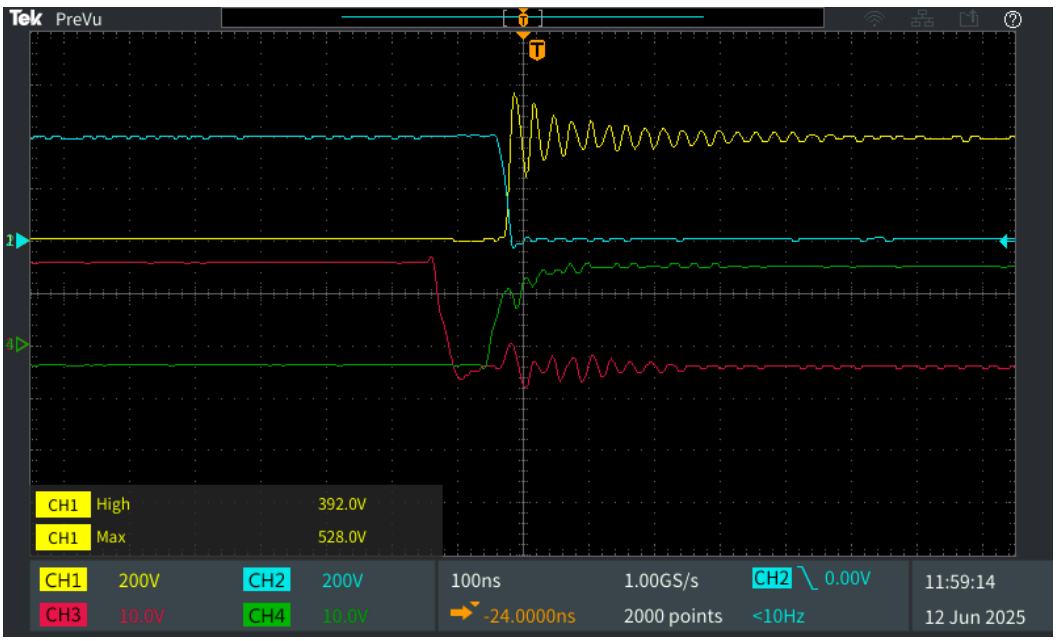


Figure 6.7: Voltage ringing across the drain source of Q1 during turn-off

The voltage ringing seen is likely coming from resonance between the parasitic inductance

in the power traces of the PCB and the drain source parasitic capacitance of the MOSFET. This happens because the current flowing through Q1 drops from 10 A to 0 A in a few nanoseconds. Since $V_L = L \cdot di/dt$, this causes a large voltage spike across the parasitic inductor. In order to reduce this, an RC-snubber can be placed across the drain and source terminals of the MOSFET. To this end, an RC-snubber circuit is designed.

6.2.2.1 RC-snubber circuit

According to Figure 6.6, the voltage ringing period T_r is approximately 32 ns, which gives a resonance frequency f_r of 31.25 MHz.
Using the datasheet, the parasitic capacitance of the drain source C_{par} is estimated to be 92 pF[21]. Since f_r is known, the resonance frequency equation can be isolated to give equation 6.1.

$$L_{par} = \frac{1}{4 \cdot f_r^2 \cdot \pi^2 \cdot C_{par}} \tag{6.1}$$

From this, the parasitic inductance can be calculated as 270 nH. With the parasitic capacitance and inductance known, an RC-snubber can be made to reduce the voltage ringing. Although it would be ideal to remove the ringing completely, this requires a large capacitor. However, as the capacitance increases, so do the losses in the RC-snubber. To find the estimated power loss the capacitor energy equation multiplied by the switching frequency can be used. This is shown in Equation 6.2.

$$P_{rc} = \frac{1}{2} \cdot C_{sn} \cdot V^2 \cdot f_{sw} \tag{6.2}$$

In general, the snubber capacitor C_{sn} should be 2-10 times larger than the parasitic capacitance C_{par}. A 220 pF capacitor is chosen. This will likely still give some voltage ringing, but was chosen as a compromise between power loss and voltage ringing. The expected power loss is 3.45 W. Lastly, a resistor value is required. Here, this value is based on the damping ratio equation for an RLC circuit. The equation is given in 6.3.

$$\zeta = \frac{R}{2} \cdot \sqrt{\frac{C}{L}} \tag{6.3}$$

With the known valuables C_{par}, L_{par} and C_{sn} and using a critical damping factor $\zeta = 1$ equation 6.3 can be rewritten as equation 6.4

$$R_{sn} = 2 \cdot \sqrt{\frac{L_{par}}{C_{par} + C_{sn}}} \tag{6.4}$$

From this, the snubber resistor R_{sn} is calculated to be 59 Ω. With the RC-snubber parameters calculated, the RC-snubber is placed across the drain and source of Q1. The drain source voltage with the RC-snubber implemented is shown in Figure 6.8.

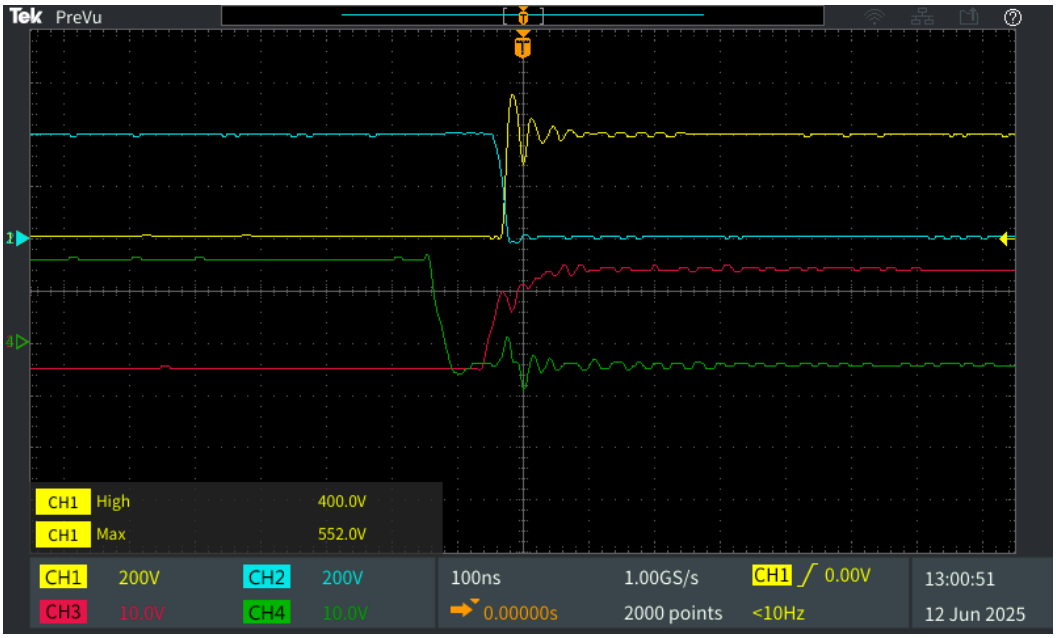


Figure 6.8: Drain source voltage of Q1 with RC-snubber present. The voltage ringing disappears much faster

As shown, there is still voltage ringing across MOSFET Q1 during turn-off with a significant overshoot, but compared to Figure 6.7, the voltage ringing dampens much faster and the resonance disappears after 100 ns. Looking at the Gate drive signal of Q1 there is still some ringing present but as seen the voltage never goes above zero so no accidental turn-on occurs.

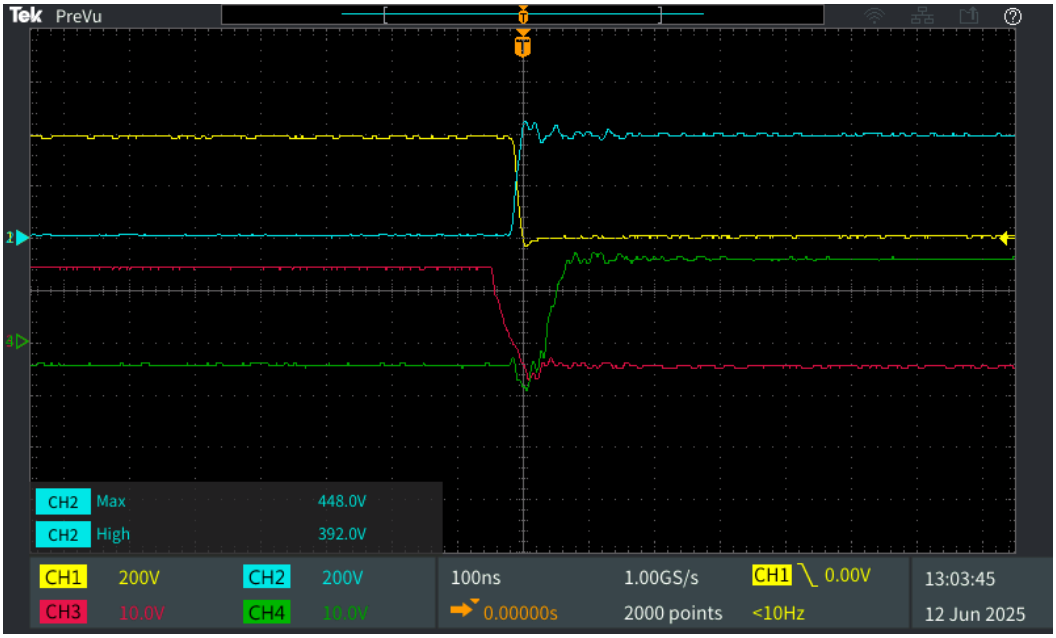


Figure 6.9: Drain source voltage Q2 with no RC-snubber

Looking at the drain source voltage of Q2 during turn-off in Figure 6.9, it is seen that there is a significantly smaller overshoot of about 60 V. It also has a negligible effect on the gate source voltages of both Q1 and Q2. Furthermore, the voltage ringing disappears quickly. Therefore, it is not necessary to place an RC-snubber across Q2.

6.2.3 Voltage boosting capability

In order to test the converters ability to boost the voltage. Four different tests are conducted with the aim of stepping up different input voltages to a 400 V output voltage. The converter is first tested with a low duty cycle, which is then increased for each subsequent test. Here, the expectation is that the input voltage required to reach 400 V becomes smaller as the duty cycle increases. A 160 Ω load resistor is used for the first three tests. The input voltage and current are represented by "CH1" and "CH3" respectively. The output voltage and current are represented by "CH2" and "CH4", respectively.

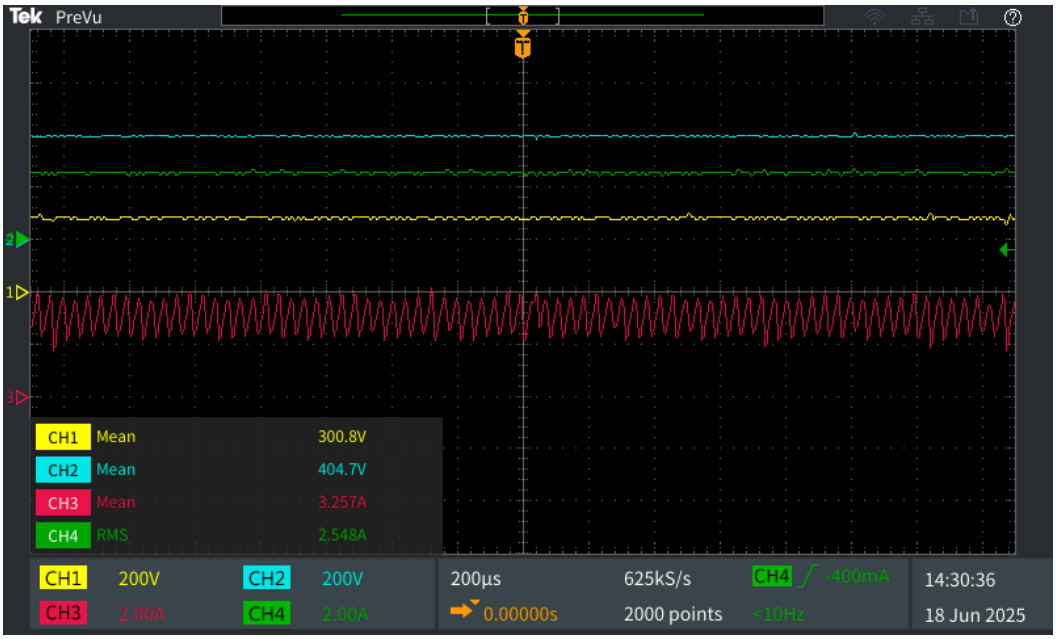


Figure 6.10: Converter voltage boosting using a 25 % duty cycle. Giving 300 V input and 404 V output

The converter is first tested with a duty cycle of 25 %. As shown in Figure 6.10, the input voltage is 300 V, and the output voltage is 404 V. Furthermore, the input current is approximately 25 3.2 A and the output current is 2.5 A.

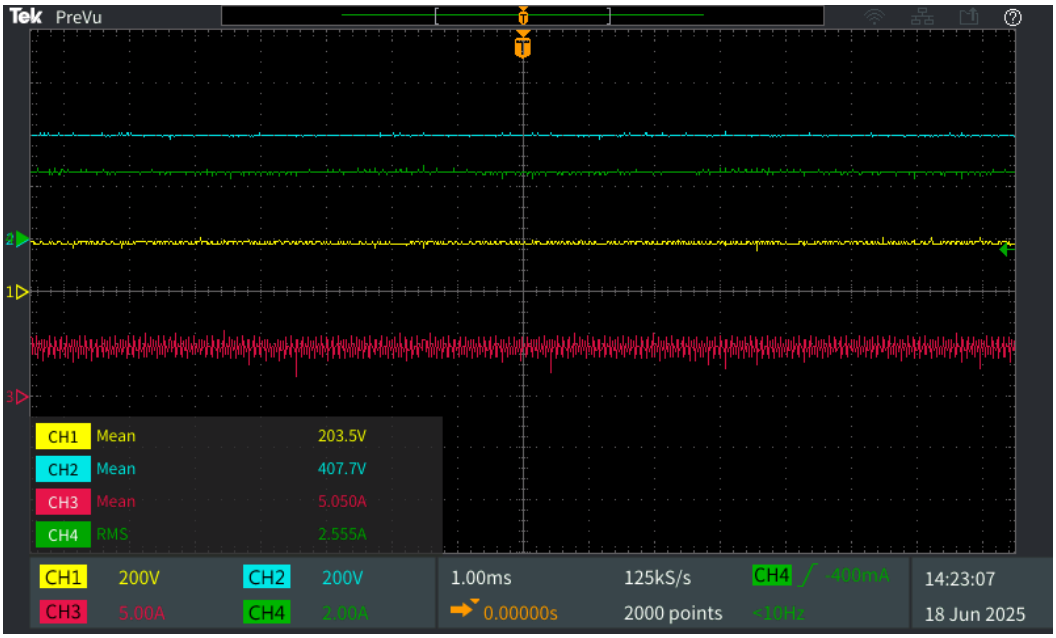


Figure 6.11: Converter voltage boosting using a 50 % duty cycle. Giving 203 V input and 407 V output

In the second test, the duty cycle is changed to 50 %. Looking at the voltage and current in Figure 6.11 it can be seen that the input voltage is 203 V and the output voltage is 407 V. In addition, the input current is 5 A and the output current is 2.5 A.

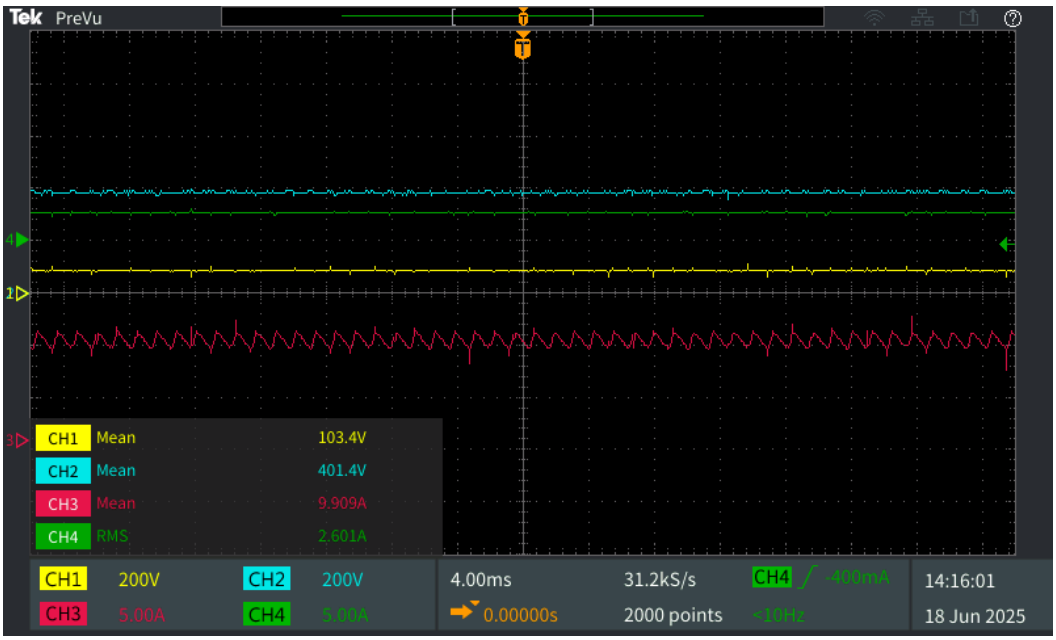


Figure 6.12: Converter voltage boosting using a 75 % duty cycle. Giving 103 V input and 401 V output

In the third test, the duty cycle is changed to 75 %. In Figure 6.12 the input voltage is given as 103 V and the output voltage is 401 V. Furthermore, the input current is 9.9 A and the output current is 2.6 A, which is an approximate difference of 4 times.

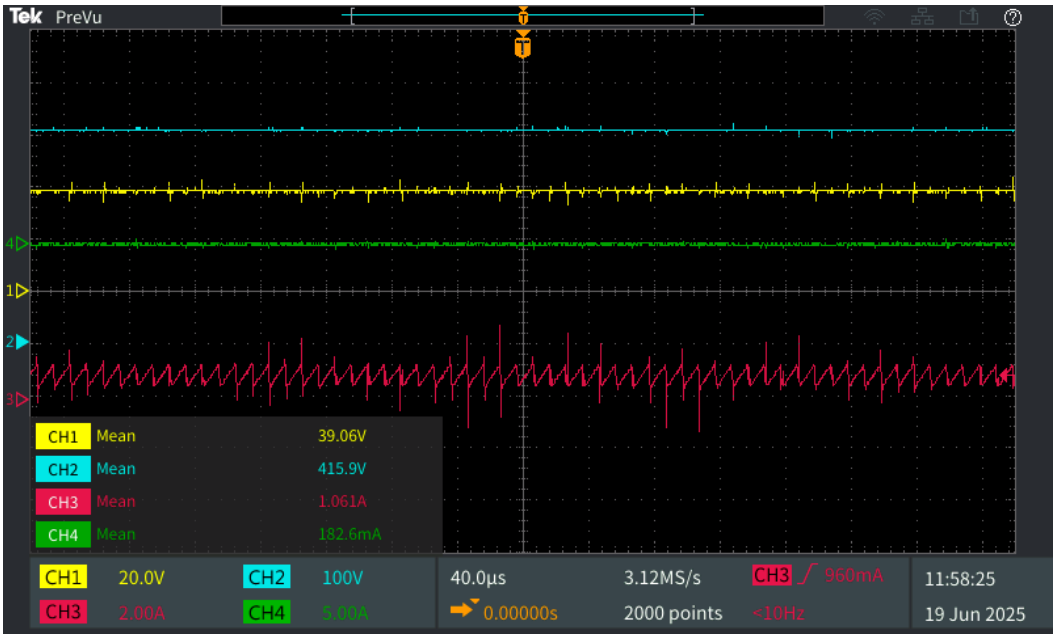


Figure 6.13: Converter voltage boosting using a 90 % duty cycle. Giving 39 V input and 415 V output

In the last test, the duty cycle is set to 90 %. Additionally, the load resistor is changed to 5k Ω since the voltage supply is not capable of delivering more than 10 A. As can be seen in Figure 6.13, the input voltage is 39 V and the output voltage is 415 V. Furthermore, the input current is 1 A and the output current is 180 mA. This does give a discrepancy between the expected ratio of input and output current, but is most likely due to measuring error, since the current is very small. According to the results shown in the figures, it can be seen that the voltage boosting capability of the converter is working as intended.

6.2.4 Power analysis and efficiency at 230 V input

In order to test the performance, the input voltage is set to 230 V and boosted to 400 V, which is similar to the average voltage conditions to which the converter performing in PFC configuration would be exposed. However, because the maximum current the laboratory voltage source can supply is 10 A, the input power at 230 V is limited to 2300 W. This power rating is used to test the performance and efficiency of the converter when boosting from 230 V to 400 V. A load resistance of 69 Ω is used to achieve the desired power rating. The input and output voltages and currents are shown in Figure 6.14.

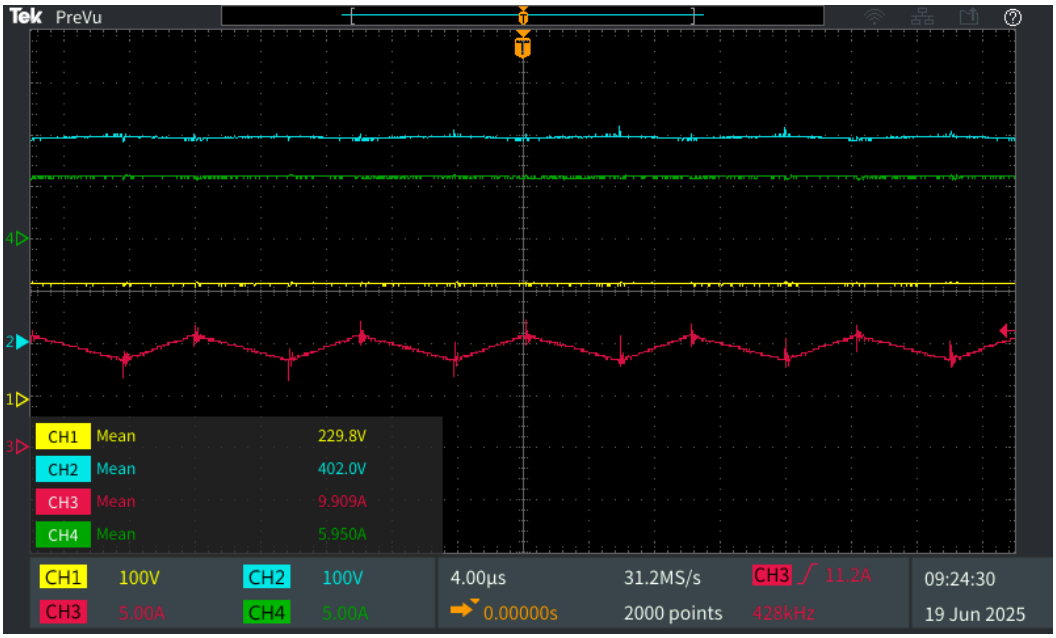


Figure 6.14: Converter running at 230 V input voltage and a power output of 2.3 kW

According to the results shown in Figure 6.14, the converter is working as intended, the input voltage is 229.8 V and the input current is 9.909 A with a current ripple of 2.2 A, which is very close to the calculated current ripple of 2.32 A. The resulting input power is 2277 W. In contrast, the output voltage is 402 V and the voltage ripple is very low, so its difficult to estimate exactly. Furthermore, the output current is 5.95 A, which gives an output power of 2391 W. This is of course not possible as this would mean that the efficiency is 105 %. In addition, comparing this with the power analyzers shows a similar result. This is shown in Figure 6.15.

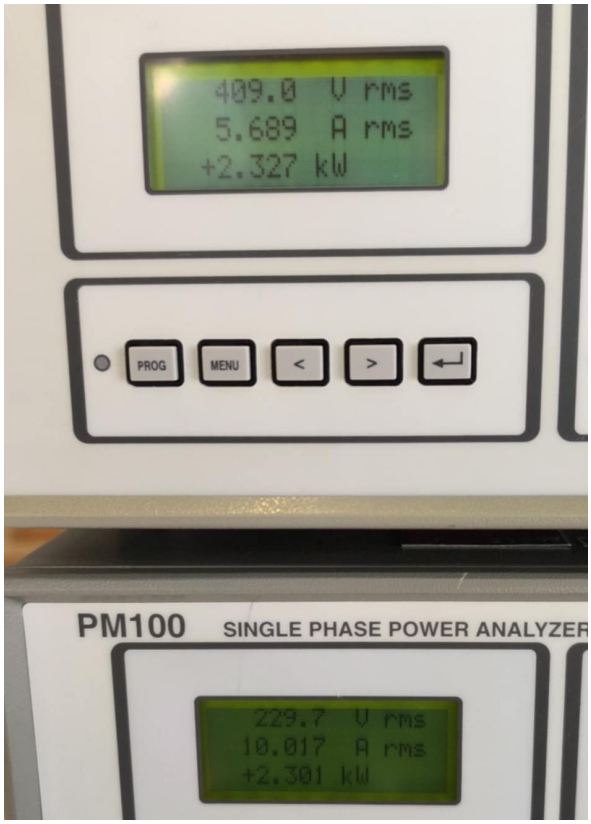


Figure 6.15: Measured voltage, current and power by analyzers

Here, the input power is 2301 W and the output is 2327 W, which would mean that the efficiency is also over 100 % This is of course, also not possible. As a result, it shows that looking at the measured currents and voltages is not an accurate method to estimate the efficiency of this converter. This makes sense when considering the fact that there is a large difference in the number range of the current, which is around 10 A, and the voltage around 400 V. As such, a small error in the measured current will lead to a large deviation in the calculated power.
So in order to estimate the efficiency, a different approach is needed. The efficiency estimate will be based on the losses in the inductor, the capacitor, and the MOSFETs. The measured inductor resistance DCR and the ESR of the capacitor datasheet will be used together with the measured currents from the power analyzer to calculate the passive component losses. Then in order to calculate the estimated losses in the MOSFETs the temperature of the heat sink is measured, this will then be used in conjunction with its known thermal resistance to calculate the total MOSFET losses. The efficiency calculation will not include the losses in the gate driver since these will be very low, this is shown using Equation 6.5.

$$P_G = Q_g \cdot V_{gs} \cdot f_s \tag{6.5}$$

Since this is frequency dependent, the LF leg can be ignored, as there will be no losses. The estimated HF losses can be calculated using the "C3M0045065K" datasheet. The driver loss is calculated as 0.1 W, which is negligible. Furthermore, the FPGA controller used will also not be considered as it uses less than 0.1 W. The last component which will not be considered is the PCB. Here, there are probably some losses that could be relevant. However, including them is too complicated, so they are not considered.

With this in mind. The converter was left operating for 15 minutes, At this point a thermal camera was used to measure the temperature of the heat sink. As shown in Figure 6.16

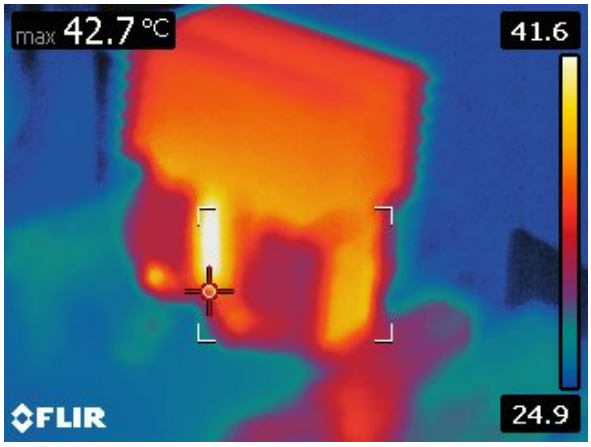


Figure 6.16: Temperature of the heat sink after 15 minutes of operation

From this it can be seen that the temperature of the heat sink close to the MOSFETs is 42.7 °C. Because the LFM of the fan used during the testing was significantly higher than initially estimated, being closer to 400-500 LFM instead of 100 LFM, the equivalent thermal resistance of the heat sink R_{HA} is between 1.2 and 1.3 °C/W according to the datasheet [16]. With these values, the total power loss of the MOSFETs can be estimated using equation 6.6.

$$P_L = \frac{T_{HS} - T_A}{R_{HA}} \tag{6.6}$$

Where T_{HS} is the temperature of the heat sink, T_A is the ambient temperature, which was measured at 25 °C in the laboratory before testing. According to this, the total estimated power loss is between 13 and 14.75 W.
In order to verify that this estimate is correct, the LTspice DC-DC model is used to estimate the MOSFET losses when the power is 2300 W. The results are given in Table 6.1.

Parameter	**Q1**	**Q2**	**Q3**	**Total Loss (W)**
Simulated Loss (W)	6	7.58	2.28	15.86
Calculated Loss (W)	N/A	N/A	N/A	13-14.75

Table 6.1: Comparison of simulated and calculated MOSFET losses

As can be seen in Table 6.1, the calculated and simulated losses of the MOSFETs are similar, indicating that the calculated losses are reasonably accurate and that the heat sink method can be used to give an estimate of the MOSFET losses. The highest value calculated is used for further calculations.
Then in order to estimate the efficiency of the converter, the inductor losses are calculated using its measured resistance, and the capacitor loss using the ESR from the datasheet. The power analyzers measured current is used for the calculation. The values are given in Table 6.2.

Component	Loss (W)
Inductor	4.07
Capacitor	0.6

Table 6.2: Losses in passive components

In order to find the converters estimated efficiency, the losses are subtracted from the analyzer's power input value. This gives an estimated efficiency of the converter of 99.1 % when running at 2.3 kW.

6.2.5 Power Analysis and Efficiency at 360 V input

To test the converter at 3.6 kW power, the input voltage is raised to 360 V. This makes it possible to test the converter's ability to operate at full power without exceeding the current limit of the voltage source. A 44.5 Ω resistor is used as a load. The results of the test are shown in Figure 6.17.

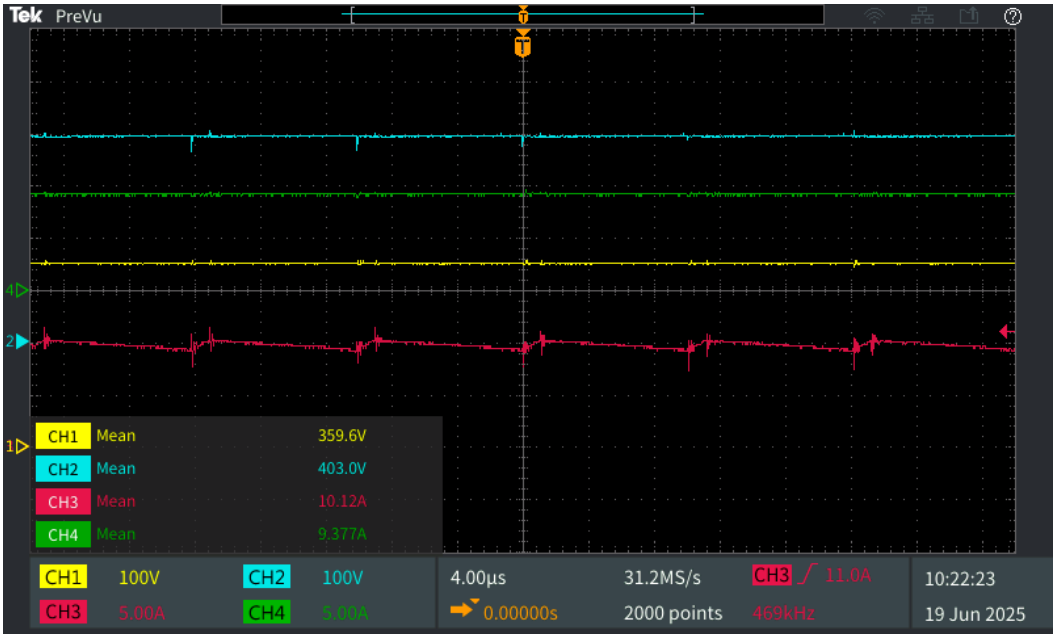


Figure 6.17: Converter running at 360 V input and a power output of 3.6 kW

As shown in Figure 6.17, the converter is capable of boosting the input 360 V input to 400 V. Looking at the inductor current, the current ripple is significantly smaller than in the previous case. However, this is expected since the current ripple depends on the input voltage as shown in Equation 4.8. The peak-to-peak current ripple is approximately 1 A. In this test, it is also not possible to estimate the efficiency using the measured voltage and currents, as such the same approach used previously is used here. The power analyzer measurements are shown in Figure 6.18.

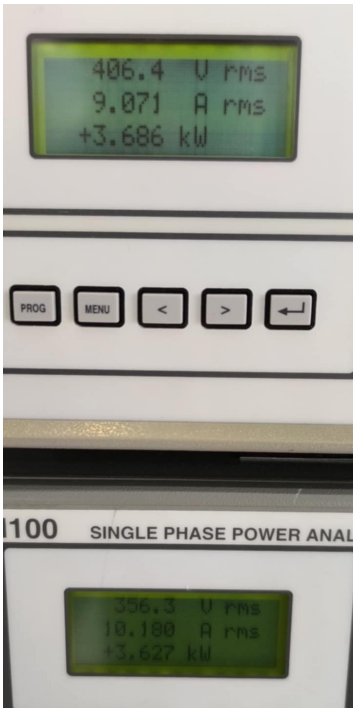


Figure 6.18: Measurements by power analyzer at 360 V input

In order to measure the temperature of the heat sink the converter is operated for 15 minutes to allow the converter to heat up. The results are shown in Figure 6.19.

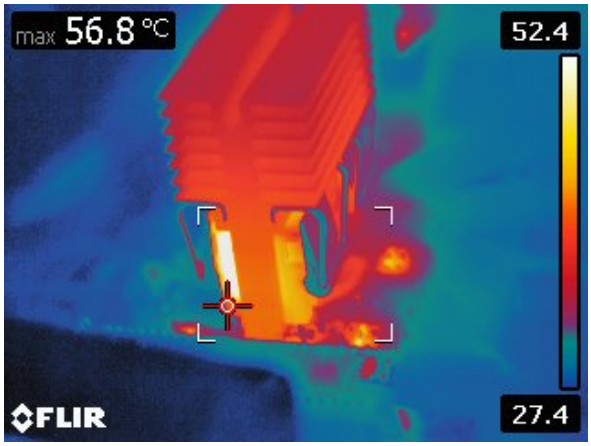


Figure 6.19: Heat sink temperature at 360 V input and 3.6 kW power

According to Figure 6.19. The heat sink is about 48 °C. Using equation 6.6, the estimated MOSFET losses are 17-19.16 W.
Inductor and capacitor losses are calculated using current measurements from power analyzers and are given in Table 6.3.

Component	Loss (W)
Inductor	4.1
Capacitor	1.5

Table 6.3: Losses in passive components at 360 V

Then subtracting the calculated power loss the from the input power of the power analyzer to estimate the output power the estimated efficiency is 99.3 %. This gives a very high efficiency. However, this is a result of the high voltage input needed in order to reach 3.6 kW it is expected the efficiency would be lower if the 3.6 kW were tested with 230 V input because of increased conduction losses.

6.3 Inverter Configuration

This section aims to test the converters operation in inverter configuration. Here, the goal is to verify the converters performance with respect to gate driver signals, correct sine waveform output, high-power operation, and estimation of efficiency.

6.3.1 Inverter gate driver signals

The gate source voltage of Q2 at its lowest duty cycle of 6.5 % is shown in Figure 6.20. As shown in the graph, the gate source voltage of Q2 is capable of reaching its required voltage when the duty cycle is at the lowest value which is necessary at the start and end of a half-cycle.

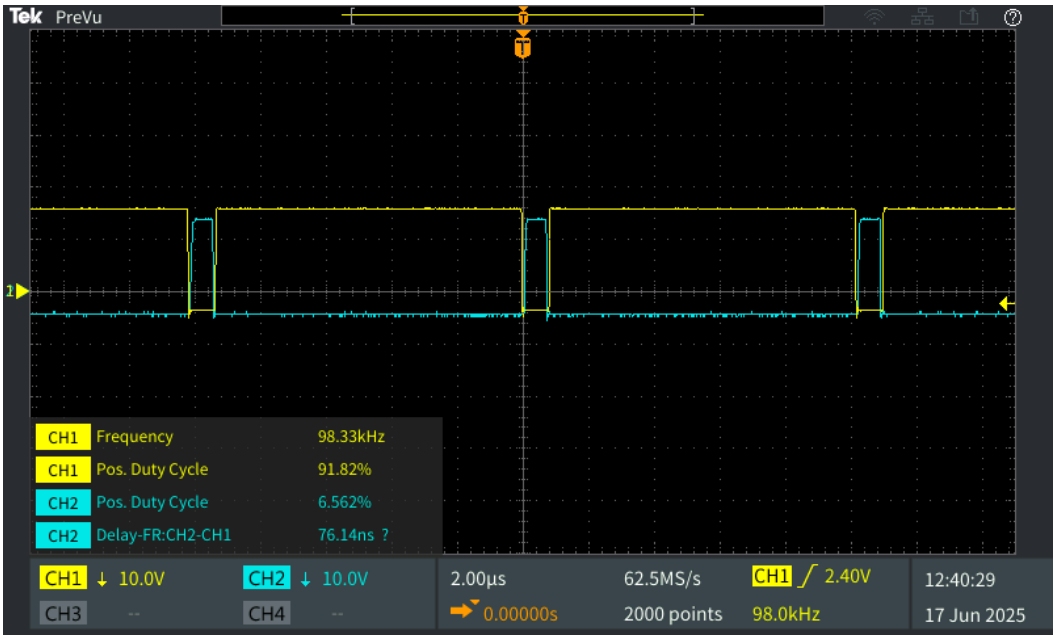


Figure 6.20: Test of gate source voltage at the lowest duty cycle value

The gate source voltages of Q3 and Q4 are shown in Figure 6.21. As seen, the gate source voltage is close to the recommended voltages and the switching frequency is 50 Hz. As such, this is working as intended.

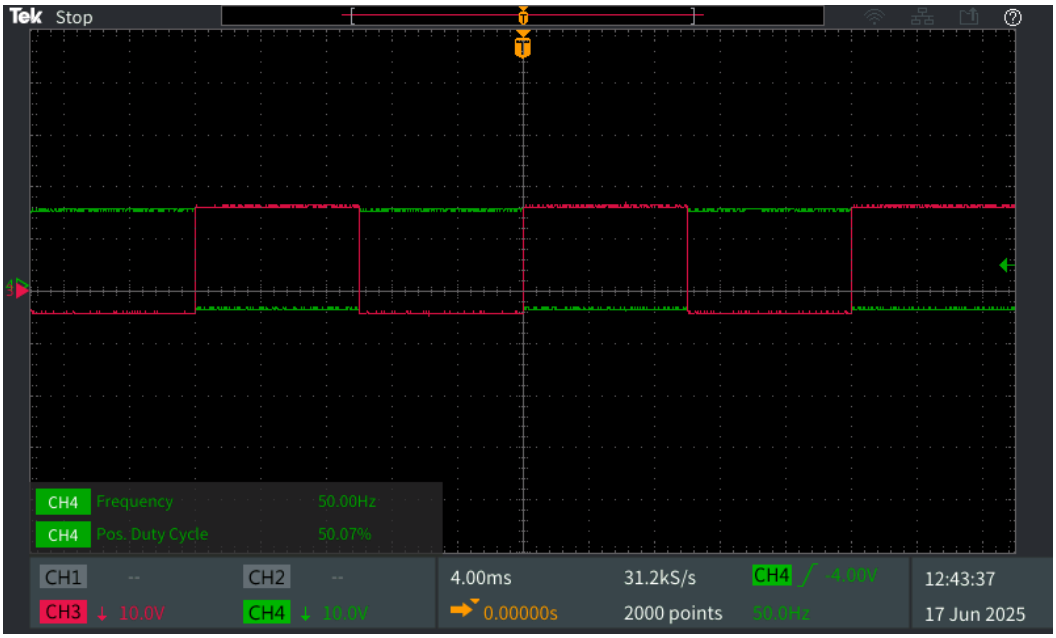


Figure 6.21: Gate source voltage of Q3 and Q4 operating at 50 Hz

The fall time of Q3 and the rise time of Q4 are shown in Figure 6.22. Here, dead time is also shown. However, even with dead-time implemented, there is a significant crossover of both voltages. This is because the gate resistor for Q3 and Q4 is 15 Ω. As a result, the switching speed is not fast enough to turn off Q3 before Q4 starts to rise. This is a problem, as it can result in a short circuit of the voltage supply.

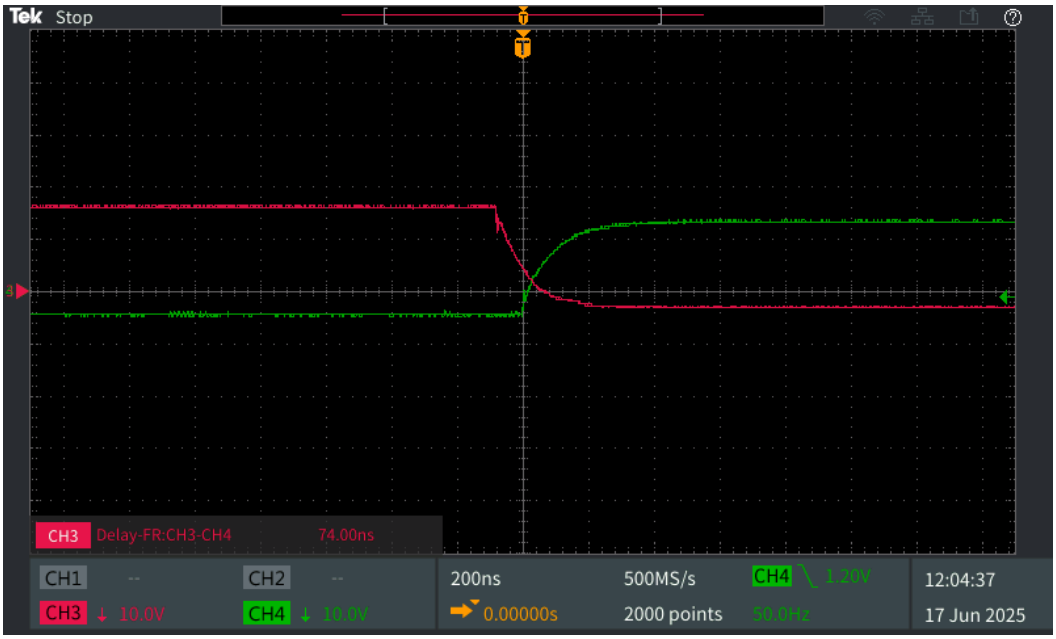


Figure 6.22: Crossover of the gate source voltage of Q3 and Q4 because a too short dead time

In order to remove the crossover the dead times of Q3 and Q4 are increased from 1 clock cycle to 3 clock cycles, giving an expected dead time of 249 ns. The results are shown in Figure 6.23. With increased dead time, there is no longer any crossover between the gate source voltages of Q3 and Q4. Therefore, Q3 and Q4 are now working as expected.

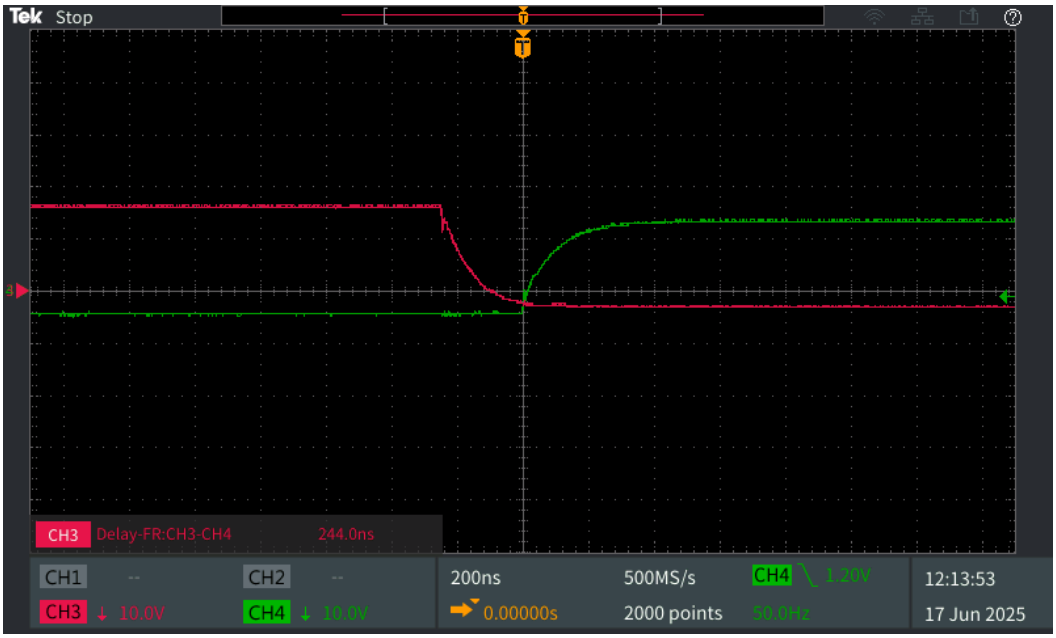


Figure 6.23: Crossover of gate source voltages of Q3 and Q4 removed with increased dead time

With the gate driver results verified, the converter can now operate in the inverter configuration.

6.3.2 Initial test of converter operating in inverter configuration

An initial inverter test is carried out to verify basic functionality and confirm that the controller and power stage operate as intended. which includes analyzing the voltage and current output waveform to see if they match the expected behavior. The first test is shown in Figure 6.24 .

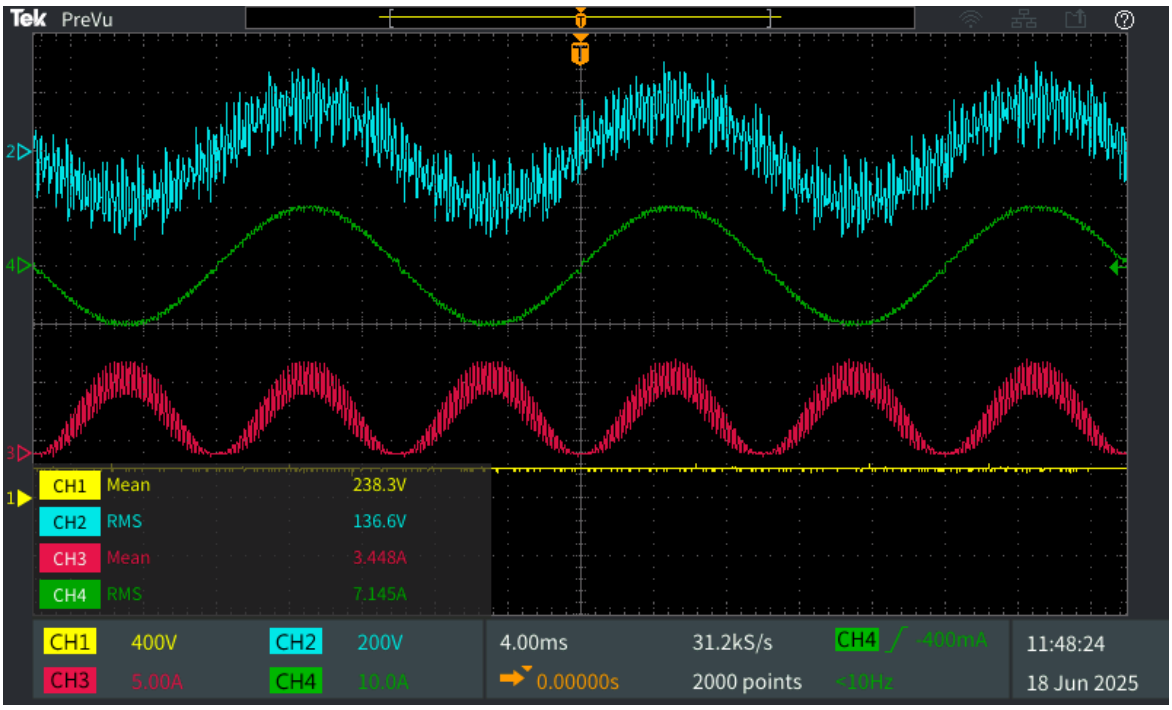


Figure 6.24: Initial test of inverter without a capacitor at the output

As can be seen in Figure 6.24. The output current is shaped as a sine wave, and the fundamental frequency is 50 Hz. This is exactly as expected, and the output current is correct. The output voltage has a very large 100 kHz voltage ripple with peak-to-peak values over 200 V. This is because there is no capacitor connected across the load. Therefore, to reduce the voltage ripple, a 3.3 μ F capacitor is connected across the load resistor. The results are shown in Figure 6.25.

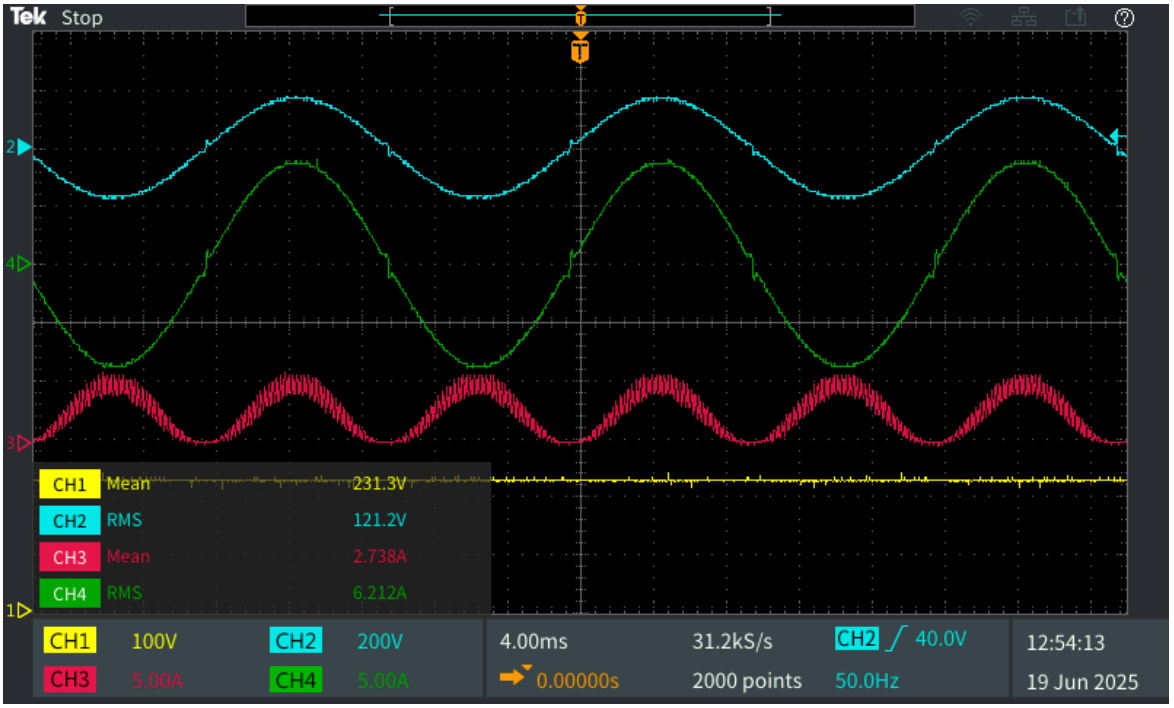


Figure 6.25: Inverter test with capacitor placed at the output

As shown in Figure 6.25, the output voltage ripple is gone and both the current and voltage waveforms follow a sinusoidal waveform. However, there is some distortion near the zero crossing point. This is because the duty cycle clamp engages when the duty cycle is too low, which causes the waveform to output a constant voltage. After a short time period the half cycle ends and the polarity is flipped by the controller, this causes a sharp spike until the voltage reaches the value where the duty cycle clamp is disengaged and the controller can start varying the duty cycle again. This is intended and is part of the controller design in order not to output a duty cycle value which is too small for the gate driver to turn on the MOSFETs properly. Therefore, it is shown that the inverter works as expected and can be tested with higher power.

6.3.3 Power analysis Analysis and Efficiency at 330 V input

To test the power capability of the inverter, the load resistor is set to 15 Ω and the input voltage is increased. Initially, the aim was to reach 400 V at the input and have the converter operate at 3.6 kW. However, when the current drawn from the voltage supply exceeded 4.8 A, it started to fail, so in order not to destroy the voltage supply, the voltage is only raised to 330 V and 4.7 A input current. The results are shown in Figure 6.26.

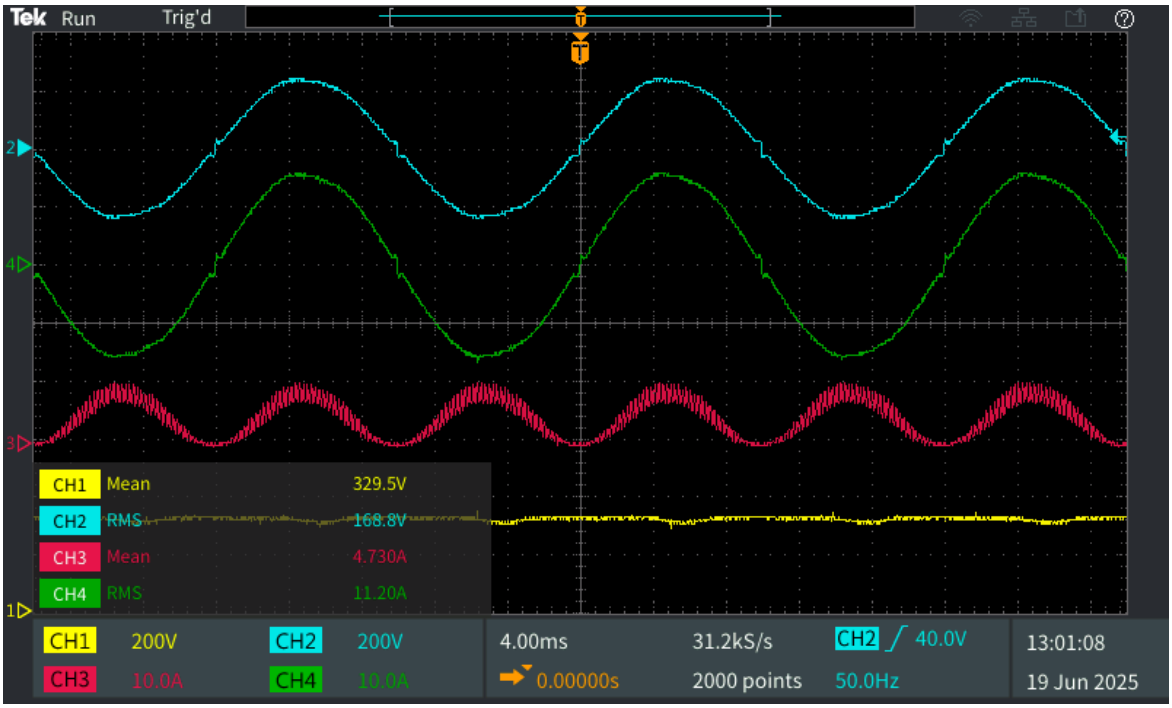


Figure 6.26: Test of inverter operating at 330 V input voltage and a power of 1550 W

Looking at Figure 6.26. The input voltage is 329.5 V and the input current is 4.7 A while the output voltage is 168.8 V rms and the output current is 11.2 A rms. Using these values to calculate the power would result in the output being higher than the input, as was also seen in the DC-DC configuration To get a better estimate of the input and output power, the power analyzer is used to measure the power, which is shown in Figure 6.27.

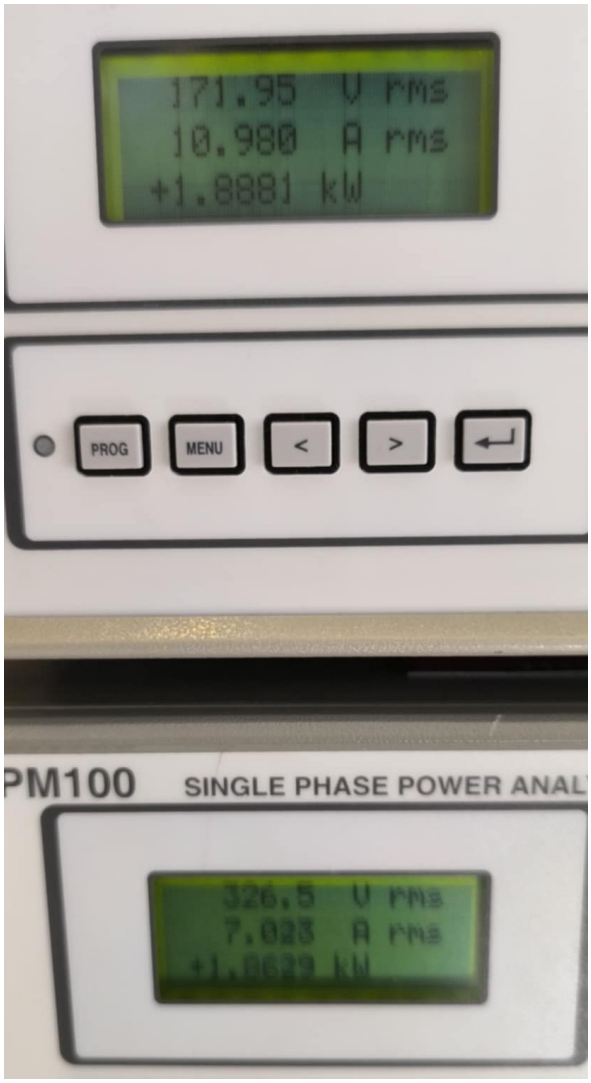


Figure 6.27: Measured input and output power by analyzer

The input of the power analyzer is used as a reference to estimate the efficiency of the converter.
In order to measure the temperature of the heat sink, the inverter is running continuously for 15 minutes, at which point the temperature of the heat sink is measured to estimate the power losses in the MOSFETs. The temperature of the heat sink is shown in Figure 6.28.

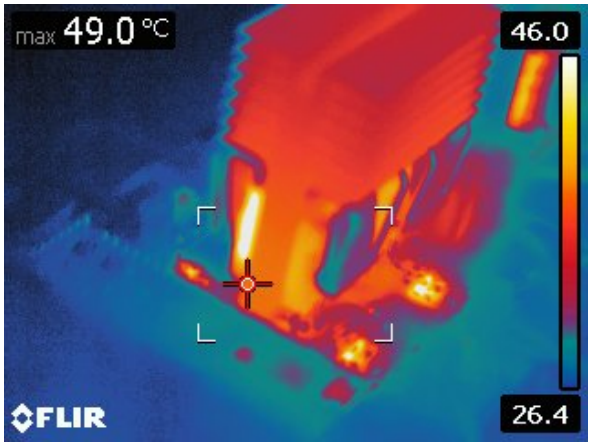


Figure 6.28: Temperature of heat sink during 330 V inverter operation

According to Figure 6.28, the heat sink is about 40 °C. To calculate the total MOSFET losses equation 6.6 is used. The estimated MOSFET losses are 11.5 to 12.5 W. The inductor and capacitor losses are then calculated based on the power analyzers measured input and output current. These are given in table 6.4.

Component	Loss (W)
Inductor	4.84
Capacitor	2.1

Table 6.4: Losses in passive components

With these values measured, the efficiency is estimated by subtracting the calculated losses from the power analyzer's measured input power to find the expected output power. The estimated efficiency is then given as 98.9 %

6.3.4 400 V input voltage test

To test the inverter with a 400 V input voltage so that the ability to reach 230 V rms at the output can be tested, the load resistor is increased to 20 Ω.

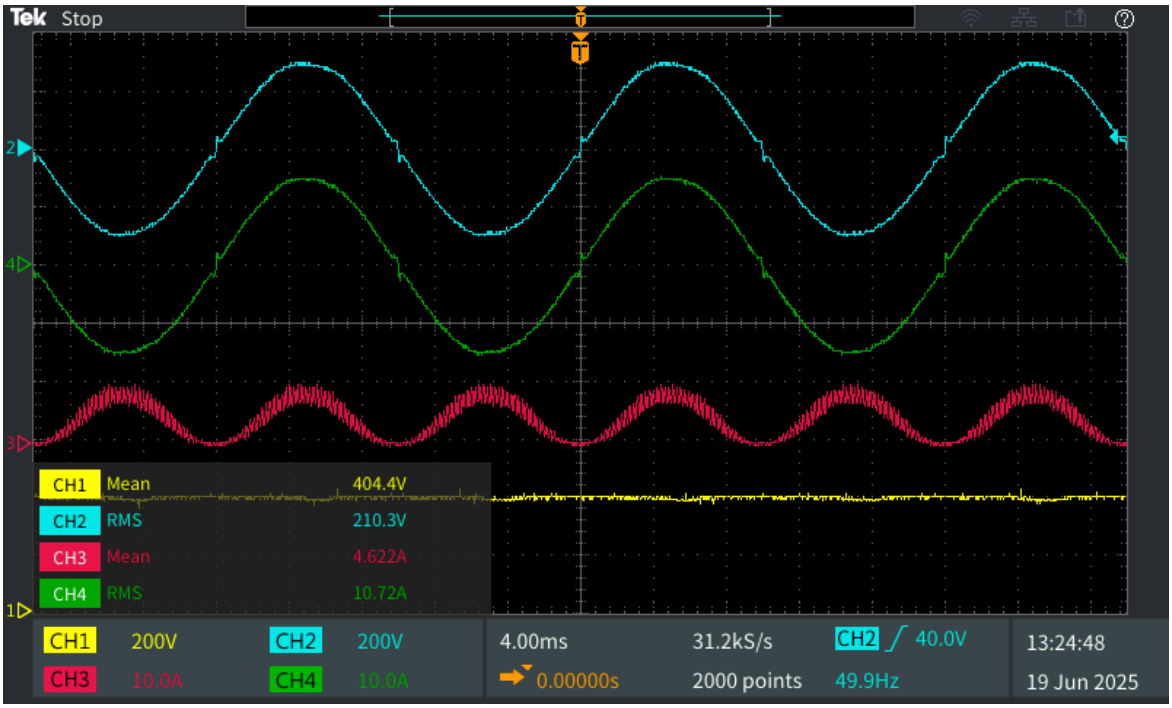


Figure 6.29: Test of inverter operating at 400 V input and a power output of 2247 W

Looking at Figure 6.29. The input voltage is 404 V and the input current is 4.6 A while the output voltage is 210 rms and the output current is 10.7 A rms. Here, the output power is approximately 2247 W. This test was only conducted for a short time as it negatively affected both the voltage supply and the gate driver supplies. It is suspected that a significant amount of common mode current was running back into the gate driver voltage supply, and a common mode choke is probably needed to reduce it. However, it is shown that the converter can run in an inverter configuration with a 400 V input voltage.

Discussion

In this chapter, limitations and assumptions made to reduce the complexity of the project due to limited time will be discussed.

Since the converter was not operated as a PFC rectifier, the total capacitor losses are less than what can be expected when operating as a PFC rectifier. This is because a much larger DC link capacitor is necessary to maintain the required voltage ripple. As a result, the ESR would also be much higher, which in turn will increase the power losses in the converter. However, the MOSFET and inductor losses will be similar since the current and voltages in the DC-DC and inverter configurations are similar to the PFC rectifier. Therefore, the efficiency results in DC-DC and inverter configurations can still be used as a good indicator of the potential converter efficiency when operating in PFC mode.
A common mode filter at the input was not included in the converter. The additional passive components of such a filter would have increased the losses. These increased losses would in turn have reduced the converter efficiency.

In a fully operational PFC converter, there are also additional losses in the measuring circuits and the gate drivers, which would increase the losses in the converter. These are not considered in the efficiency estimation. However, the total losses for these circuits would be small and so the power loss would be relatively small. Therefore, the tested converter can still be used as a reference for the potential efficiency gains that can be made.

During converter operation, it was not possible to determine converter efficiency by measuring input and output power. A possible reason for this is the high level of noise in the PCB board. This could be due to a lack of filtering, but also because a 2-layer board was used, making it difficult to create a good layout with proper grounding and signal routing.

During the power loss estimation of Migatronic's existing converter many of the components were not known. Therefore, several assumptions were made about the components used in their converter, As such, the calculated component losses are only an estimation. However, since the calculated efficiency was higher than the stated efficiency, the component loss data are still used.

The converter efficiency was estimated by calculating the losses in the inductor, capacitor, and MOSFETs. However, there were other components such as the gate drivers, controller, and the PCB traces which generated losses that were not included. However, these components only make up a small fraction of the total converter losses, so disregarding them will not affect the converters calculated efficiency much.

The MOSFET power losses were based on the increase in the temperature of the heat sink during converter operation. Although this gave an estimate of the power losses and was also compared with simulated losses to verify the method, it still has a degree of uncertainty because it is easy to overestimate or underestimate key parameters such as the thermal resistance.

Conclusion

This project investigated how a 3.6 kW Totem pole converter could be built and operated with the intent of reaching an efficiency higher than that of the Migatronic's existing converter with a stated efficiency of 97 %.

Two control systems were developed on an FPGA development board. The first control system allowed the converter to be controlled in a DC-DC configuration. This control system is designed to operate at 100 kHz and has dead-time implemented between switching transitions. The control system is tested in the laboratory and the controller PWM outputs worked as expected. A second control system is developed to control the converter in an inverter configuration. Here, four different control structures are made, consisting of a sine look-up table, a carrier wave, a PWM comparator, and a delay block to implement dead time. These are designed with the goal of generating a 50 Hz fundamental sine-wave duty cycle with a 100 kHz switching frequency and dead time between switching transitions. This was then tested in the laboratory where the PWM generated signals are measured directly and an RC filter is used to see the duty generated cycle. The control system worked as expected.
The components are selected with the goal of achieving high efficiency. Here, several calculations are performed to estimate the switching and conduction losses of two SiC MOSFET models. The SiC MOSFET C3M0045065K is chosen for the HF leg due to its superior switching performance. In the LF leg, the C3M0025065K is chosen for its superior conduction performance. To drive the MOSFETs, a gate driver is needed. The Infineon 2EDS9265H is chosen because it is specially designed for SiC MOSFETs and can drive the recommended turn on and turn off voltages of the MOSFETs, which are 15 V and -4 V respectively. In order to achieve a negative turn-off voltage, a negative bias circuit is created. This uses a Zener diode to create a negative voltage during turn-off. For the C3M0045065K MOSFET a 4 Ω resistor is chosen as the input gate resistor and a 2 Ω resistor is used during the turn off. For the C3M0025065K MOSFET 15 Ω resistor is used for both turn on and off because of the very low switching frequency. Two isolated DC-DC power supplies are used across MOSFETs Q1 and Q3. The passive components equations are derived and used to find the necessary inductance and capacitance needed for the required current and voltage ripple. A self-made inductor from a previous project is chosen. To test the Inductors parameters, a DC and an AC voltage is applied across the inductor the resulting inductor current and voltage are then measured and used to estimate the inductance and DC resistance.
A converter simulation model is created that included manufacturer-made models of the chosen gate drivers and MOSFETS, negative bias voltage circuits, and the gate resistor circuit. Furthermore, the chosen inductor and capacitor with their DCR and ESR are also included. A series of simulations are then conducted to verify the converter's performance. First, the converter is tested in the DC-DC configuration. Here, the converters ability to boost the input voltage is tested, where 397 V is reached. Furthermore, the output voltage ripple is measured at $\pm$ 5.85 V, which is very close to the calculated value. Furthermore, the inductor current ripple is measured at 2.34 A, which is also very close to the calculated value. The gate driver signals are then tested. Here, the gate source turn ON voltage

was 15 V and the turn-off voltage is -4 V. Therefore, the simulation model verified that the converter worked in DC-DC configuration. The converter is then tested in the inverter configuration. Here, the output voltage and current are a sinusoidal waveform operating at 228.9 V rms and 15.48 A rms with a fundamental frequency of 50 Hz. The component power losses are then simulated and all are within an acceptable range to reach the required efficiency. The simulated efficiency of the inverters is 98.9 %. The simulated MOSFET power losses are then used to design a thermal solution. Here, the heat sink is designed so that the MOSFETs Q1 and Q2 reach a steady-state junction temperature of 100 °C.

In order to experimentally validate the converter, a 2-layer PCB is designed. Here, the PCB is designed with the intent of minimizing interference from the power circuit to the gate driver circuit and the control circuit. This is achieved by placing the power plane, the MOSFETs, and the terminals on the top side of the board. Then the control circuit is placed at the bottom to increase the distance between the controller and the power plane. On each side of the board are gate driver circuits. These are placed as close to the gate source legs of the MOSFETs as possible to minimize parasitic inductance in the gate driver circuit. An additional PCB is designed which contains the high-side isolated power supplies required to turn on the high-side MOSFETS during operation.

The converter is first tested in the DC-DC configuration. The gate source voltages are tested first. The gate source voltages are 15 V at turn on and -3.6 V during turn off, the gate driver is operating at 100 kHz and a 83 ns dead time is present between each switching transient. Therefore, they are working as expected. An initial converter test is conducted and the drain source voltage of MOSFET Q1 and Q2 is measured. Here, a significant amount of voltage ringing is present when Q1 turns off, this is due to parasitic inductance in the traces resonating with the parasitic capacitance in the MOSFET. To minimize this, an RC-snubber is placed across the drain and source of Q1. This significantly reduced high-side ringing to an acceptable level. The voltage boosting capability is then tested, where the duty cycle is varied four times, first at 25 % from 300 V to 404 V, then 50 % from 203 V to 407 V, then 75 % from 103 V to 401 V and finally at 90 %. from 39 V to 415 V. The converter is capable of converting all voltage ranges tested. The converter is then tested with at 230 V and 10 A input. Here, the converter operated correctly and boosted the voltage to 402 V. The inductors current ripple is estimated at 2.32 A, which is close to the calculated current ripple. An attempt is made to calculate the efficiency using the measured voltages and currents. However, this is not accurate and gave incorrect results, so instead the efficiency is measured differently. First the temperature of the heat sink is measured after 15 minutes of operation. This is then used to determine the total power loss in the MOSFETs, and then the inductor and capacitor losses are calculated. These combined losses are then subtracted from the input power measured by the power analyzer to find the estimated efficiency. The efficiency is estimated to be 99.1 % at 2.3 kW. The converter is then tested at 3.6 kW. Due to a 10 A current limitation on the voltage supply, this is instead achieved by raising the input voltage to 360 V. Here, the converter also operated as expected and boosted the voltage to 403 V. The current ripple is significantly smaller, but this is expected since the input voltage has changed. The estimated efficiency is 99.3% at 3.6 kW.

The converter is then tested in an inverter configuration. The gate source voltages are tested first. Here, the gate drivers ability to turn on with a small duty is shown. Then the Q3 and Q4 PWM signals are tested, and they operate at 50 Hz. The 83ns dead time is too small for Q3 and Q4, so it is changed to 249 ns after this. All the PWM signals worked as expected. An initial inverter test is conducted and the output current follows a

50 Hz sinusoidal waveform, which is the correct output. The voltage ripple is very large because no capacitor is connected at the output, so a 3.3 μF capacitor is added and the voltage ripple is removed. The inverter is then tested at 329 V and 7 A input. The inverter worked correctly and is capable of turning a 329 V DC signal into a 168 V rms sine wave. The efficiency is estimated in the same way as in the DC-DC configuration. The estimated efficiency is 98.9 % at 1860 W. The converter is then tested at 400 V input. However, this caused problem for for the voltage supply so only the ability to operate at this voltage range is shown, and the efficiency is not estimated.
From this it is shown that a 3.6 kW converter was built and operated correctly at up to 3.6 kW and that the estimated efficiency significantly exceeded the 97 % requirement set by Migatronic.

Further Investigation

It would be interesting to redesign the converter with measuring circuits and active PFC control so that the performance and efficiency can be estimated as a PFC rectifier. Furthermore, with more time and a more complicated PCB it would potentially also be possible to reduce noise. This in turn could potentially allow the converter efficiency to be measured more accurately.
Testing the converter with GaN FETs would also be interesting in order compare the performance difference between SiC and GaN Transistors, this would also allow a better comparison of the advantages and limitations of each transistor type.

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Appendix 1

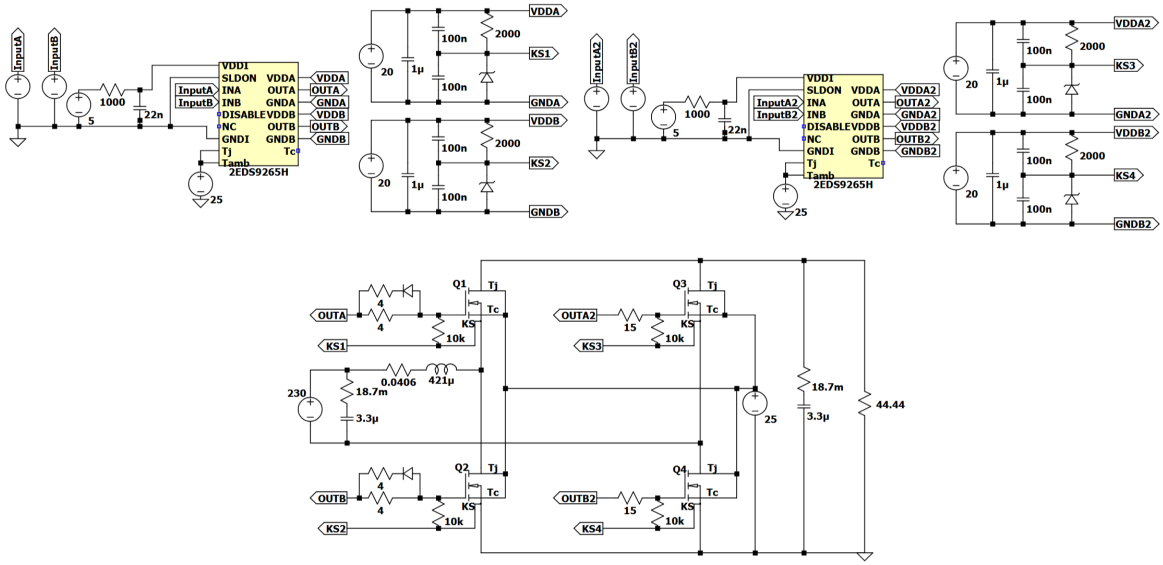

Figure A.1: Circuit Schematic of Simulation Model