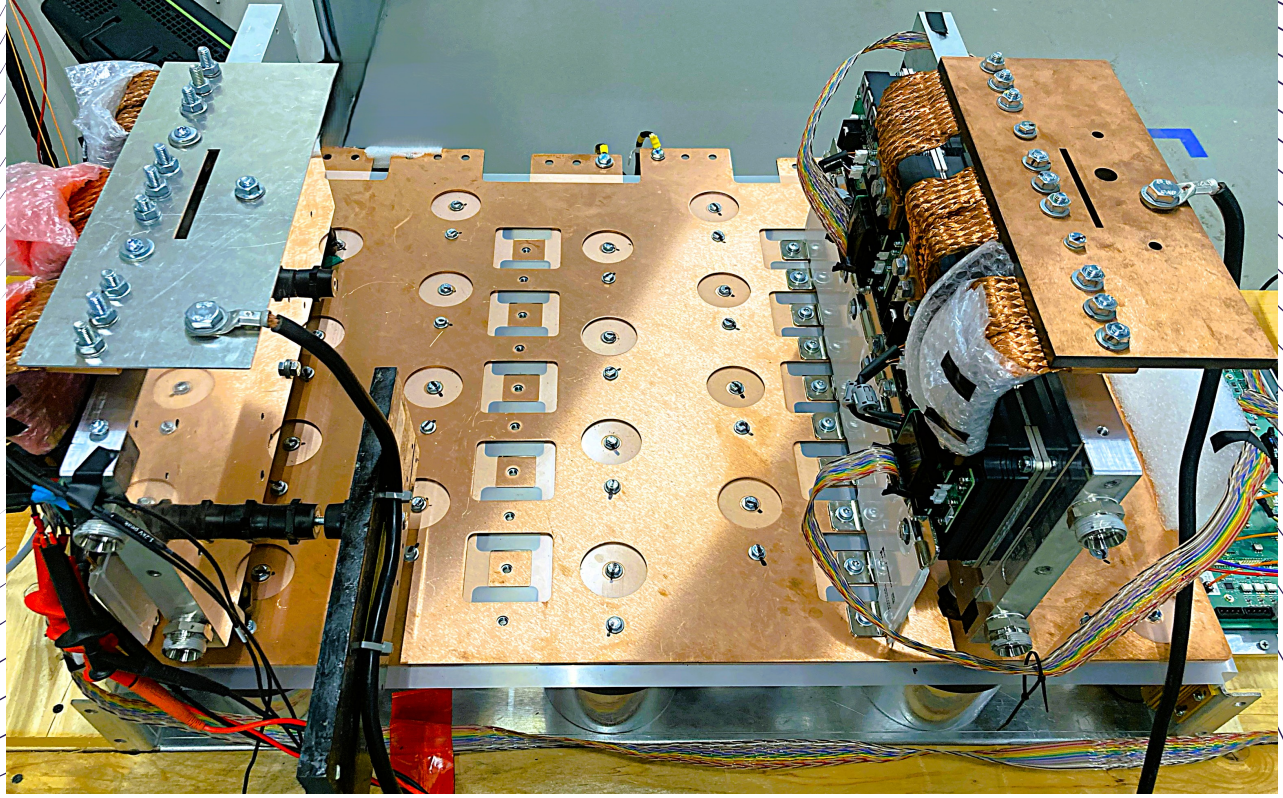

Optimization Tool for Layout Stack to ensure Even Current Sharing among Paralleled Switching Devices

Layout impedance balance for paralleled power devices

Project collaboration with KK Wind Solutions

Shubham Gupta

Energy Engineering, PED4-1048, 2025

Master Thesis

STUDENT REPORT

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Participant(s):
Shubham Gupta

Supervisor(s):

Academic Supervisor
Szymon Michal Beczkowski
Co-supervisors
Stig Munk-Nielsen
Pawel Piotr Kubulus

Industrial Supervisor
Anders Eggert Maarbjerg

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Abstract:

The project explores a pragmatic approach to achieve balanced current sharing among paralleled power modules by optimizing external layout of the system using Genetic Algorithm (GA). The goal is to enable detection of impedance imbalances in complex system layouts, making it easier for designers to visualize and mitigate issues during the early stages of development. A key feature of this project is the use of FastHenry, an open-source software tool. Its accessibility and transparency provide users with full control over design and operation, while its seamless integration with MATLAB, the workflow becomes more efficient, enabling automated simulations, equation solving, and interactive visualizations. For a fully open-source alternative, Python can be used as well to achieve similar integration. To validate the tool's output, several layout variants with varying complexity were generated using the algorithm and tested using a Double Pulse Test (DPT) setup at KK Wind Solutions' facility. Further developments shall include improving the accuracy of the Fast Henry model, refining the optimization tool for convergence speed and making it user-interactive.

Index Terms - "Genetic Algorithm (GA), Current Sharing, Paralleled Power Modules, Impedance Balancing, FastHenry, MATLAB Integration, Python, Double Pulse Test (DPT), Layout Optimization, Open-Source"

The content of this report is freely available, but publication (with reference) may only be pursued due to agreement with the author.

Preface

This report has been prepared by PED4-1048 as part of the MSc in Power Electronics and Drives master's thesis semester at Aalborg University, in collaboration with KK Wind Solutions.

I would like to express my sincere gratitude to my academic supervisor, **Szymon Michal Beczkowski**, co-supervisors **Stig Munk-Nielsen**, and **Pawel Piotr Kubulus** from **Aalborg University** for their outstanding supervision and invaluable insights throughout the project. Their guidance helped me develop the ability to break down complex problems into manageable parts, identify core challenges, and implement effective solutions. As someone new to electromagnetic multi-physics tools and genetic algorithm optimization, this project was a significant learning experience. It boosted my confidence and deepened my understanding of how to approach and solve complex engineering problems.

I also extend my heartfelt thanks to our project partner, **KK Wind Solutions**, for their continuous support and collaboration. I am especially grateful to the company for granting access to their facilities for carrying out tests relevant to the project. Special thanks goes to **Anders Eggert Maarbjerg** for his expert guidance and unwavering support, which were instrumental in shaping the direction of this work. I also appreciate the contributions of **Jakob Diechgraeber** and **Bjørn Rannestad**, with whom the brainstorming sessions and idea bouncing greatly enriched the project developments.

A special note of thanks to my wife, **Pooja**, for her unwavering belief in me. Her encouragement during the challenging phases of the project kept me motivated and inspired.

This project was conducted during the spring semester of 2025, from February to June.

This project investigates the detection and mitigation of layout-induced parasitic imbalances in paralleled power modules—an issue that can significantly affect system performance due to the arbitrary nature of external layouts. To address this, a Genetic Algorithm (GA)-based optimization method was developed to automate layout balancing. By integrating the open-source simulation tool FastHenry with MATLAB, the approach offers a transparent and flexible solution for early-stage layout evaluation. Its effectiveness was validated through Double Pulse Test (DPT) measurements at KK Wind Solutions, using algorithm-generated layout variants, demonstrating the tool's practical value in real-world applications.

Reading guide

This summary report is separated into chapters which are numbered progressively. These chapters are further separated into sections. The reference method used in this project report is that of the Institute of Electrical and Electronics Engineers (IEEE). Several appendices are attached, including MATLAB scripts, Fast Henry scripts and results.

The following programs have been used during the course of the project:

- Overleaf by WriteLatex Ltd.
- Drawio by JGraph Ltd and draw.io AG
- MATLAB by MathWorks
- Plecs by Plexim GmbH
- LT Spice by Analog Devices
- FastHenry2
- FreeCAD EM Workbench

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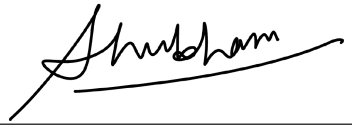

Shubham Gupta
sgupta23@student.aau.dk

Summary

As the demand for high-power systems grows—particularly in renewable energy and Power-to-X (PtX) applications—paralleling power modules is becoming increasingly popular to scale power capacity. However, this introduces a critical design challenge: **layout-induced parasitic imbalances** caused by ambiguous system layouts. These imbalances lead to **uneven current sharing**, which can degrade system performance, reduce reliability, and shorten the operational lifespan of components.

The project investigates an automated optimization approach to mitigate the external layout impedance imbalances for equal and uniform current carried out through each module in parallel.

A comprehensive and automated workflow was developed, integrating **FastHenry**, an open-source multiphysics simulation tool, with **MATLAB** for scripting, data processing, and optimization. The methodology is structured into three main components:

- **Test System Modeling** - FastHenry was used to model the parasitic impedance of external layouts. A digital representation of the test setup was created, incorporating key parasitic elements such as interconnect inductances. The model neglects internal module characteristics and gate driver influence to focus on layout-induced effects. It outputs impedance matrix of the layout, enabling analysis of imbalance patterns.
- **Automation Layer** - MATLAB was employed to automate the generation and execution of FastHenry scripts, parse simulation outputs, and manage optimization. This automation significantly reduces manual effort, improves repeatability, and allows for scalability to systems with varying numbers of paralleled modules.
- **Optimization via Genetic Algorithm (GA)** - A Genetic Algorithm approach was selected for its robustness in handling non-linear, multi-variable problems. The GA modifies layout parameters within defined constraints, seeking to minimize current imbalance. Penalty functions were introduced to guide the search toward feasible and practical solutions. The algorithm iteratively evolves layout configurations, comparing generations to converge on optimal designs.

To validate the Fast Henry model and Optimization tool, a few layout variants generated by the GA were physically manufactured and tested using a **Double Pulse Test (DPT)** setup at **KK Wind Solutions**. The validation confirmed that the simulation accurately predicted **current distribution trends** across modules, under various test conditions (e.g., load positions, cable distances from DC link busbar). However, the **magnitude of current deviations** in simulation was often higher than in physical measurements. This discrepancy was traced to model simplifications and the exclusion of certain real-world effects. Despite this, the tool proved effective in identifying problematic layout configurations and guiding improvements. Depending on the preferences of the user, it is possible to carryout analysis based on the project requirements.

To conclude, this thesis attempts to solve the problem of external layouts using an automated approach to layout optimization for paralleled power modules, addressing a critical challenge in high-power electronics. By combining open-source simulation with

intelligent optimization, the tool offers a practical solution for early-stage design validation and improvement. With further development, it has the potential to become a valuable asset in the design of efficient, reliable power systems.

Future works may include improving the accuracy of the Fast Henry model by introducing more components and increasing fidelity. Parameters such as current density, voltage overshoots and thermal aspects can be analysed and considered as feeedbacks for refining the solution by introducing realistic electrical constraints. The GUI can be developed to make the code easily accessible and more interactive. The target applications can focus on the end goals of system topologies for rectifiers and DC-DC buck converters for solution's direct implementation into the system.

Abbreviations

Abbreviation	Explanation
DPT	Double Pulse Test
AC	Alternating Current
DC	Direct Current
MCPM	Multi-Chip Power Module
RSM	Response Surface Modeling
FET	Field-effect Transistors
IGBT	Insulated-Gate Bipolar Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
WBG	Wide-Band Gap
GaN HEMTs	Gallium Nitride High-Electron Mobility Transistor
FEA	Finite Element Analysis
GA	Genetic Algorithm
PSO	Particle Swarm Optimization
SA	Simulated Annealing
ACO	Ant Colony Optimization
PCB	Printed Circuit Board
PV	Photo-Voltaic
Si	Silicon
SiC	Silicon Carbide
EMC	Electro-magnetic Compatibility
PEEC	Partial Element Equivalent Circuit
CAD	Computer-Aided Design
KVL	Kirchhoff's Voltage Law
EM	Electromagnetic
ESL	Equivalent Series Inductance
CO_2	Carbon Dioxide
MVAC	Medium Voltage Alternating Current
HVDC	High Voltage Direct Current
MMC	Modular Multilevel Converter
WBG	Wide-Bandgap
REN	Renewable Energy
IEA	International Energy Agency
IRENA	International Renewable Energy Agency
AFE	Active Front End
DSO	Digital Signal Oscilloscope
DB	Dead Band
P2X or PtX	Power-to-X
EV	Electric Vehicle
P2H	Power-to-Hydrogen
EMI	Electromagnetic Interference
DUT	Device Under Test

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Chapter 1 Introduction

In modern power electronics, power modules are compact assemblies that integrate power semiconductor devices. These modules are widely employed in demanding applications such as home, renewable energy systems, industrial electrolyzers, and tractions where high performance, reliability, and scalability are crucial.

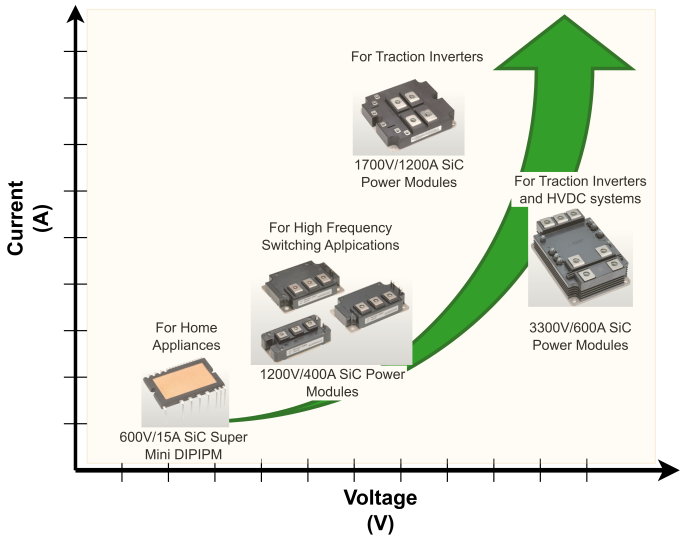


Figure 1.1: Power Modules for various applications [1]

Figure 1.1 shows a range of SiC Power modules used in various applications from Home Appliances, High frequency switching applications and Traction & HVDC applications from Mitsubishi [1].

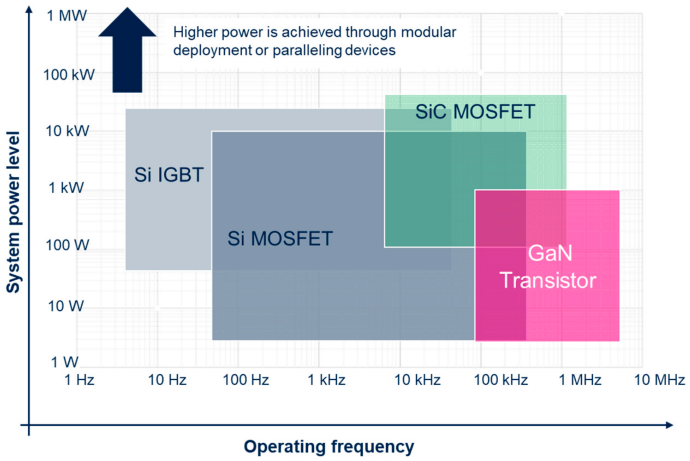


Figure 1.2: Power modules - System power level [2]

As shown in figure 1.2, to meet these growing demands, paralleling multiple power modules has emerged as a key design strategy. This approach enables systems to achieve higher power density, improved thermal performance, and enhanced fault tolerance, all while preserving modularity for easier maintenance and future expansion. Figures 1.3 and 1.4 are indicatives of increasing power demands in renewable energy sectors.

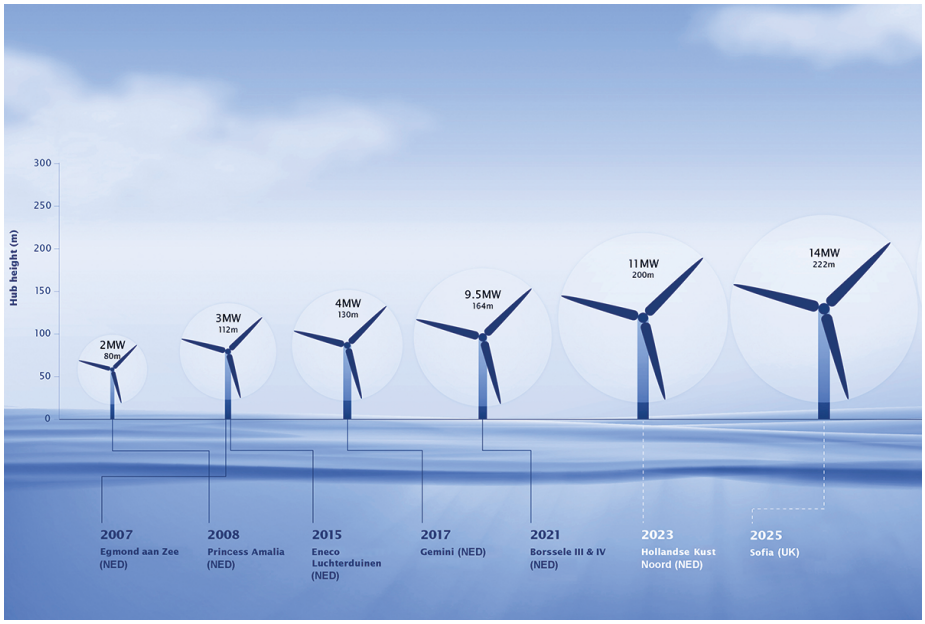


Figure 1.3: Capacity increase - Wind Power [3]

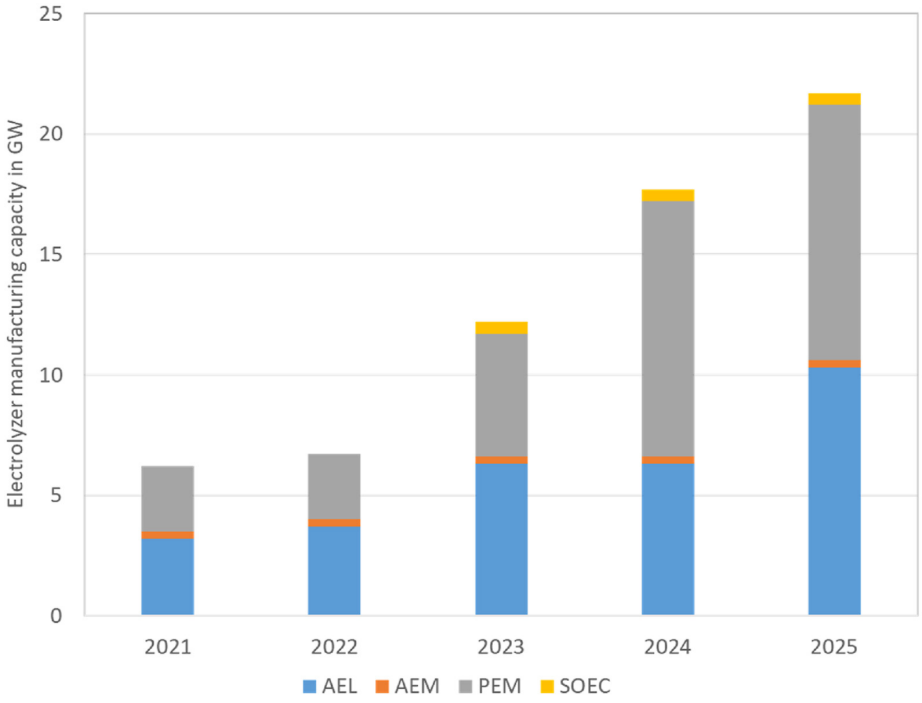


Figure 1.4: Cumulated electrolyzer manufacturing capacities in gigawatt sorted by technology [4]

The global push toward sustainability is accelerating the adoption of such technologies. The environmental impacts of fossil fuels and greenhouse gas emissions have prompted 131 countries—responsible for 88% of global emissions—to commit to achieving net-zero emissions by 2050. This ambitious goal is driving a rapid transformation in the energy landscape[5].

Renewable energy is a crucial part of this transition. According to recent forecasts, re-

newable energy consumption across the power, heat, and transport sectors is expected to increase by nearly 60% between 2024 and 2030. The electricity sector is the primary driver of this growth, accounting for more than three-quarters of the overall increase. This surge is supported by falling technology costs, favorable policies in over 130 countries, and the expanding use of electricity in road transport and power generation sectors such as wind and solar PV [6].

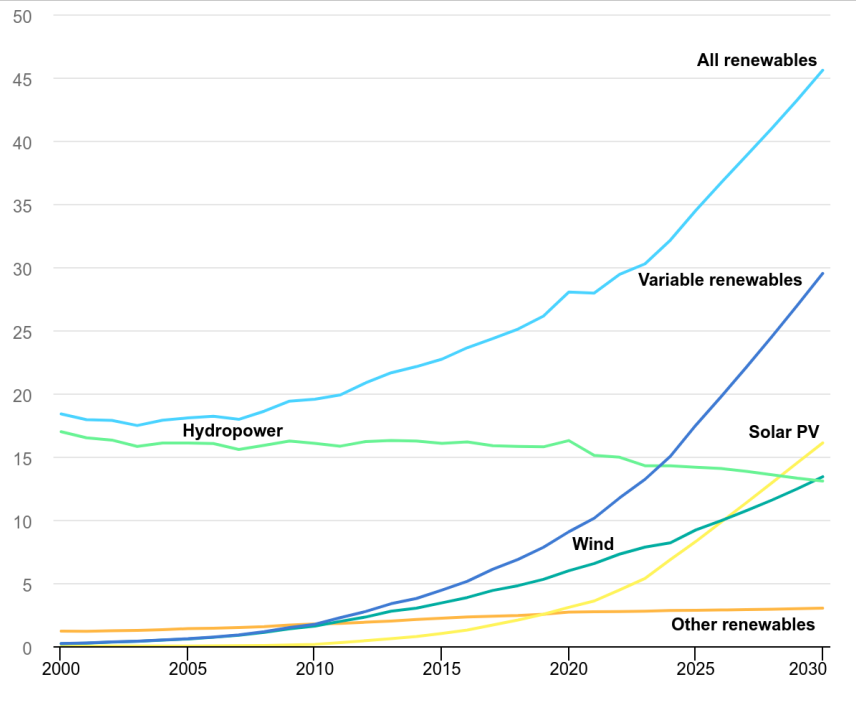


Figure 1.5: Electricity generation from wind and solar PV indicate potential generation including current curtailment rates [7]

The figure 1.5 shows the percentage share of the renewables in the electricity sector with Wind and Solar PV contributing the major share.

While the demand and growth in these sectors are substantial, The energy transistion involves broader range of Renewable Energy (REN) resources beyond wind, solar PV, and battery storage, moving towards multienergy vector-based systems. These also include hydrogen pipelines via power-to-X (P2X) technology and the heat generation areas. Integrating these diverse energy vector requires power conversion interfaces with varying ratings, configurations, control and operation strategies, to harmonise the working of these renewables and getting the desired system output, robustness and stability.

1.1 Review of State of Art

For these multi-Megawatt applications effective power handling, scalability and system reliability are of utmost importance. Power Electronics plays a crucial role in harnessing the energy generated from these varied sources to make it consistent with the outputs. Distinct configurations such as Medium Voltage AC (MVAC), High Voltage DC (HVDC)

connections, for power distribution and delivery, AC and DC coupling and decoupling using Multi-Level Modular (MMC) converters, AC to DC, DC to DC and DC to AC power conversions for compatibility with other power sources and employing different topologies to translate throughput requirement provide a strong foundation for utilising these renewable resources as an alternate for the conventional fossil fuel based resources. The production of muti-chip power modules, paralleled power modules and stacks has been an inherent part of the power electronics for sustaining and scaling equipments pertaining to these high current applications.

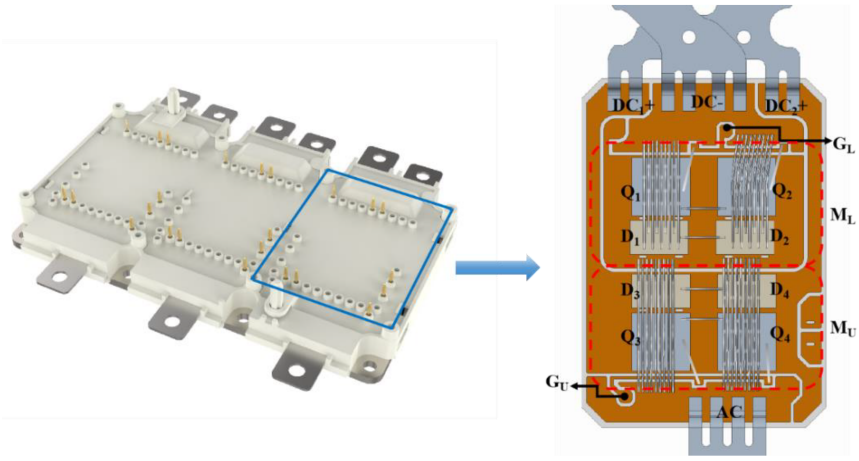


Figure 1.6: Multi-chip power modules [8]

The report "Solutions for Wind Energy Systems" by Infineon Technologies [9] emphasizes the critical role of paralleling power modules in enhancing the reliability and efficiency of wind energy systems. By distributing the load across multiple modules, the system achieves better thermal management, reducing the risk of overheating and improving overall efficiency. This approach also enhances scalability, allowing systems to be easily expanded to meet increasing power requirements. Paralleling addresses key challenges such as effective heat dissipation, redundancy for uninterrupted power supply, and lower inductance for faster switching speeds and reduced losses, making it essential for reliable and efficient wind energy conversion using their IGBTs with a notable emphasis on modular designs and the explicit support for paralleling modules or sub-assemblies.

The paper ,"Hard Paralleling SiC MOSFET Based Power Modules" [10], explores the technical and commercial aspects of paralleling power modules for high current applications. It talks about the importance of paralleling of power modules instead of using higher rated single modules. The more critical aspect is improved thermal performance, reduced inductances in both power loops and gate drivers as compared to large physical packages. Commercially, smaller, high-volume packages are cost-effective and scalable.

The report "Designing for Scalability in High Power Applications" by Wolfspeed [11] emphasizes the advantages of using Silicon Carbide (SiC) MOSFETs for scalable high-power applications. It highlights how paralleling discrete SiC MOSFETs enhances flexibility, scalability, and thermal management, addressing issues like current imbalances and parasitic inductances. This approach ensures efficient and reliable operation, making it ideal

for both system upgrades and new configurations. The report underscores the importance of optimizing power density, design simplicity, system costs, and reliability through the use of SiC technology.

Power module paralleling plays a crucial role in the handling of high power suited for the electrolyzer requirement, the nature article [12] titled, "Power electronics for green hydrogen with focus on methods, topologies, and comparative analysis", discusses paralleling of advanced power electronic devices such as (Active Front End) AFEs, DC-DC converters are crucial for meeting the high current and stable DC voltage demands of industrial electrolyzers. They ensure high efficiency, and power quality of the electrolyzer to operate smoothly. With possibility of smoother integration with fluctuating power outputs from renewables sources, they hold the key towards development of the green hydrogen infrastructure.

As seen from the above researches, it is evident that paralleling plays a crucial role for such applications. One of the key challenges in this approach is managing internal current imbalances, which can arise due to variations in device characteristics and thermal conditions. To address this, ongoing research is focused on optimizing chip design and packaging to enable more balanced current sharing across modules. Recent advancements in these areas are steadily improving the practicality and performance of paralleled configurations, making them increasingly viable for integration into complex, high-current energy systems.

The paper titled “Parallel Connection of Silicon Carbide MOSFETs—Challenges, Mechanism, and Solutions” by Helong Li [13] describes the complexities and solutions associated with the parallel connection of Silicon Carbide (SiC) MOSFETs. The article, [14] explains impacts of static and dynamic current imbalance in paralleled power MOSFETs leading to uneven conduction and switching losses, causing thermal issues and reliability problems. It highlights strategies to manage these imbalances for efficient and reliable operation. The paper, "Optimization and Validation of Current Sharing in IGBT Modules With Multichips in Parallel" [15], also aims towards balanced power distribution by equalising the circuit parasitics within IGBTs to reduce chip stress.

The paper titled “Switching Current Imbalance Mitigation in Power Modules with Parallel Connected SiC MOSFETs” [16] addresses the challenge of uneven current sharing in paralleled SiC MOSFETs due to layout-induced parasitic asymmetries. These imbalances can cause excessive current overshoot and stress on individual devices. To mitigate this, the authors propose a method of tuning individual source inductances. The approach is validated through numerical parasitic extraction and experimental testing, showing significant improvement in current sharing and switching behavior.

A notable study from the University of Arkansas introduces a methodology for fast and accurate parasitic extraction in the layout design of Multi-Chip Power Modules (MCPMs) [17] using response surface modeling (RSM). This approach supports multi-objective optimization by enabling rapid evaluation of layout-induced parasitics, which is critical for high-performance power module design. The research integrates FastHenry, an open-source tool, to simulate frequency-dependent parasitic inductances across various layout

configurations. FastHenry stands out in this context due to its accessibility, accuracy, and ease of integration into automated workflows. By leveraging this method, designers can explore thousands of layout variants efficiently, balancing electrical performance, thermal behavior, and physical constraints—ultimately accelerating the development of optimized, low-parasitic Multi-Chip Power Modules (MCPMs) for applications such as electric vehicles, renewable energy systems, and industrial drives.

Another aspect is the external layout parasitics which plays an important role towards balanced power distribution. This ensures higher reliability and long term operation of the power devices. There are several variants of the high voltage power modules in the market which are designed specific to the application requirements for instance, a 2kV or 2.3kV module is developed for the electrolyzer and wind power applications, 3.3kV modules are available for the traction loads etc. Paralleling these modules efficiently can scale up the current carrying capability and enhance power handling capacity. Figure 1.7 shows an example of paralleled power modules for high power handling capability.

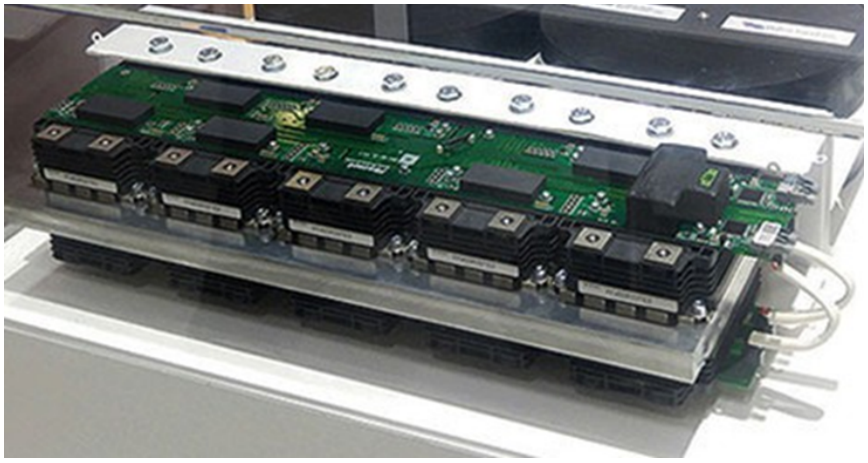


Figure 1.7: Paralleled Power Modules [18]

Since layout is not always standard and is specific to a designer, a careful analysis of the imbalances needs to be placed in order to meet the current requirements. Partial impedance computation and analysis using multi-physics softwares necessitates the understanding of influence of parasitics on the system behaviour. This helps to develop a balanced layout which generates an equalized impedance seen by each module either equally good or equally bad, ensuring balanced current sharing among the modules. As the current level grows higher, the significance of the layout becomes more and more prominent. That is why it is a good idea to develop a model for deeper analysis.

The study titled “Lumped Parameter Modeling Based Power Loop Analysis Technique of Power Circuit Board with Wide Conduction Area for WBG Semiconductors” [19] proposes a simplified yet effective method for analyzing parasitic effects in power circuit layouts used with wide-bandgap (WBG) semiconductors. The technique models the power loop using lumped parameters to capture the influence of layout-induced parasitics, which are critical in high-speed switching environments. To validate the model, the researchers employed PSpice for circuit-level simulation and ANSYS Q3D Extractor for 3D electromagnetic parasitic extraction. While commercial tools like ANSYS Q3D of-

fer comprehensive multiphysics capabilities, open-source alternatives such as FastHenry can also be used for inductance extraction, offering a lightweight and accessible option for academic and early-stage design workflows.

The thesis titled "Design and Optimisation of a Half-Bridge Switching Module With Parallel GaN HEMTs for High Power Applications Using Finite-Element Analysis" [20] focuses on developing a high-performance power switching module using gallium nitride (GaN) high-electron-mobility transistors (HEMTs). The work emphasizes minimizing parasitic inductance and optimizing thermal and electrical performance through finite-element analysis (FEA). It explores the challenges of paralleling GaN devices, such as current sharing and layout symmetry, and proposes design strategies to ensure reliable high-power operation. The study also includes simulation and experimental validation of the proposed module design.

Although these models are very effective in identifying the parasitic imbalances, the layout optimization can take several iterations to solve an acceptable solution. The thesis [20], iterates the process by developing a PCB layout, analysing the model in FEA software, extracting the parasitics and simulating in LT SPICE for inductance equalization and reevaluating to match them closely.

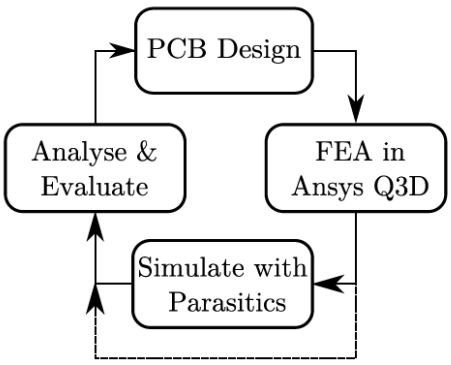


Figure 1.8: Flow Chart for Digital Design [20]

Figure 1.8 shows the Flow Chart for Digital Design. This is a good close loop approach to mitigate the problem with balancing and is being currently used in the industry as well.

The investigation on the element of automation adds an extra layer to the layout balancing and expedites the process to develop a suitable solution. This will reduce layout reconstruction iterations and provide more time for in-depth analysis of the set layout, ensuring reduced failures of paralleled modules. Power Electronics implementation of automation is limited, however, there are some that shows promise in the method and have witnessed good results.

The papers "Metaheuristic Optimization Methods Applied to Power Converters: A Review" [21] and "Review of Power Module Automatic Layout Optimization Methods" [22], give a comprehensive view of how metaheuristic algorithms are applied to layout optimization in power electronics. The first paper emphasizes the versatility of metaheuristic

methods like Genetic Algorithms (GA), Particle Swarm Optimization (PSO), and Simulated Annealing (SA) in handling the nonlinear, high-dimensional design spaces typical in power converter development. The second paper narrows the focus to layout optimization in power modules, comparing these algorithms based on their search capabilities, convergence behavior, and implementation complexity. Together, they highlight that while no single method is universally best, GA and PSO are particularly effective for global exploration, SA excels in local refinement, and Ant Colony Optimization (ACO) is well-suited for routing tasks within layout design.

In this study we looked into Genetic Algorithms (GAs) in greater details as its applications matched more with the given problem and there is high utilization of this algorithm in similar applications of impedance balancing for equal current sharing.

The PhD thesis titled “Efficient Automated Design and Optimization for Wide-Bandgap Semiconductor Power Modules” [23] focuses on developing automated design methodologies for power modules using wide-bandgap (WBG) semiconductors like SiC and GaN. The work integrates digital twin concepts, parasitic-aware modeling, and GA optimization technique to enhance layout design. It emphasizes the use of simulation tools and automated workflows to accelerate the design process while ensuring high efficiency and reliability in high-power applications. The research contributes to scalable and intelligent design strategies for next-generation power electronics systems.

The project, "Automatic PCB Layout Optimization of a DC-DC Converter Through Genetic Algorithm Regarding EMC Constraints", [24] explores the use of genetic algorithms to automate the PCB layout optimization of DC-DC converters, with a specific focus on minimizing electromagnetic compatibility (EMC) issues. Traditional manual layout methods often struggle to balance electrical performance with EMC compliance, especially in high-frequency switching environments. By leveraging evolutionary computation, the approach aims to intelligently evolve PCB designs that meet both functional and regulatory requirements. The study integrates EMC-aware constraints into the optimization process, ensuring that the resulting layouts are both efficient and compliant.

1.2 Problem Analysis

This section utilizes the review done in the previous section to base the problem introduction and solution investigation in the forthcoming sections.

With this higher push towards green energy and electrification, it is important to invest resources into paralleling of the developed power modules to increase the power handling capabilities of the power converters. One such application is the hydrogen electrolyzer power supply requiring a 3MW to 12 MW load supply as part of the internship project last semester [25].

This project investigated paralleling of two SiC MOSFET power modules for balanced current sharing. This approach was majorly recalibration of the test bench to achieve the point of minima. The project shows the test steps carried out to find the influence of each aspect in the setup to identify the major contributors. Out of the several aspects

considered, the external layout for the Double Pulse Test (DPT) was chalked out to have a large contribution towards the current imbalance. The limitation of this approach was, first, that there was limited flexibility to find the balance points. Secondly, it took several iterations to work out a solution and it was not completely replicable to other sites. Although, this project utilizes FastHenry for its computations, however, it was done ideally to verify the model with the test setup and simulate the influence of load cable modification through rotation to find the balance as most of the components were already fixed.

The importance of multi-physics softwares to create a digital model for such ambiguous systems is getting recognized with the arrival of power modules like IGBTs and MOSFETs. These devices tend to switch at higher speeds and carry large currents. The impact of layout parasitics became more pronounced on efficiency, and reliability of these modules.

Several multi-physics softwares are available in the market which helps in development of accurate parasitic analysis and provide close enough results. FastHenry is one such tool available in the market to develop such a model. The automation facilitation of this software makes it user-friendly and easy to work with optimization algorithms. This project utilizes this tool for analysis of the Double Pulse Test setup and developing a lumped model of parasitic components in the system.

FastHenry stands out as a potential candidate for inductance extraction due to its open-source nature, making it freely accessible to researchers, engineers, and students worldwide. Unlike many commercial alternatives, it allows users to inspect, modify, and extend its source code, enabling customization for specific applications or integration into larger simulation workflows. Its lightweight design and command-line interface make it highly portable and easy to incorporate into automated design environments. This flexibility, combined with its proven accuracy in modeling complex 3D geometries and frequency-dependent effects, makes FastHenry a preferred choice in both academic and industrial settings.

It has been used for similar applications, for instance, The paper “Accurately Modelling of Parasitics in Power Electronics Circuits Using an Easy RLC-Extraction Method” [26] presents a practical and accessible approach for modeling parasitic inductance and capacitance in power electronic circuits. It utilizes the open-source tools FastCap and FastHenry to extract RLC parameters from 3D geometries, enabling accurate simulation of circuit behavior. The method is demonstrated through a case study involving a buck converter, showing how layout-induced parasitics significantly affect switching performance.

The integration of FastHenry with MATLAB opens a lot of possibilities into in-depth analysis of the system at hand and will provide valuable insights of the benefits to automation of the process. One of the researches done along this lines is the paper, "Partial Element Equivalent Circuit (PEEC) Toolbox for MATLAB, integrating FastCap2 and FastHenry2 for Calculation Partial Elements and Multisim or LTspice for circuit simulation" [27]. This paper presents a MATLAB-based PEEC Toolbox designed to streamline the modeling of electromagnetic problems by converting them into circuit equivalents. It integrates FastCap2 and FastHenry2 for calculating partial capacitance and inductance

elements, respectively. The toolbox supports geometry definition, meshing, and netlist generation, enabling seamless simulation in LTspice or Multisim. This integration offers a flexible, open, and automated workflow for EMC-aware circuit design and analysis.

It is therefore, prudent to make a fast and reliable software impedance computation for making the analysis faster and explore more dimensions. The tendencies were observed by moving and changing the size of the cutouts in the switch-node busbar and inorder to find the minima point, the approach was taken to increase the computation efficiency. This is a solid approach by making a digital model and developing a method for finding the best possible layout creating the possibility of minimizing the impact of layout interference in paralleling operation.

An automated approach towards using the initial design as reference and defining the parameters of freedom or mobility can expedite the approach towards a feasible solution ensuring the accuracy and precision of results.

1.3 Problem Statement

Formulating a precise research problem is a foundational step in any scientific inquiry, as it defines the study's scope, direction, and relevance. As Pardede (2018) [28] explains, this process involves systematically narrowing a broad area of interest into a specific researchable issue considering theoretical, contextual, and methodological factors. Complementing this, the thesis by Kenneth C. Bowen [29] underscores the importance of aligning the research problem with real-world challenges and the availability of analytical tools, ensuring both feasibility and impact.

Guided by these principles, this study focuses on identifying and addressing critical gaps in the paralleling of multi-chip power modules—specifically the influence of external layout parasitics, utilizing the development of accurate digital models, and the use of automation to enable faster computation and more comprehensive analysis.

"*Is it possible to develop an algorithm aimed at modifying and reiterating the FastHenry script providing an automated approach to minimize the effects of layout while conforming to practical system limitations?*"

1.3.1 Objectives

In this project the main objectives are:

- To develop a FastHenry model to accurately emulate the parasitics of the test setup for Double Pulse Testing.
- To automate the loading, execution and parameter storage of FastHenry model for further analysis using MATLAB.

- To develop an optimization algorithm aimed at modifying and reiterating the FastHenry script to minimizing the effects of layout while conforming to practical system limitations.
- Validate the solutions obtained using lab testing on the Double Pulse Test Setup at KK Wind Solutions.

1.3.2 Scope, Constraints and Assumptions

This project involves the development of an optimization tool designed to mitigate current imbalance arising from impedance mismatches between paralleled power modules.

Since, the power stacks are in production and are used as a modular unit for the power supply of the electrolyzers, the scope of the tool is limited to changing DUT switch-node busbar and point of load connection. Based on conclusions drawn in the previous semester [25], a new switch-node busbar will be designed to address the imbalance introduced in the power stack layout. This approach allows full flexibility in configuring the DUT connection busbar, which is essential for the optimization tool's effectiveness.

It is important to note that the project is limited to the analysis of the DPT setup as it is easier to verify the model and optimization method there. It can be later extended to three-phase inverter or rectifier operation, which is the end goal.

The power modules and gate drivers are not the part of in-house development and limited information is available on the structure and design due to the proprietary nature. Also, adhering to the timelines and limited manpower, the pace of decision-making, project planning, and further resource availability are crucial aspects to be taken into consideration.

Given the project's scope, the gate drivers are treated as ideal components and the power module's (IGBT in this case) forward voltage drop and emitter inductance only are taken into consideration. While their influence on switching behaviors and overall module performance is acknowledged, it is considered negligible for the project's objectives. Nonetheless, their effects are still analyzed within the project's defined parameters. It is also assumed that the quasi-steady state behavior of the power module shall be the same and will show similar results during testing.

It is assumed that the DC link voltage remains at the same potential for the test duration. The capacitors are assumed to contain the ripple content within grid standards and are not taken into consideration for the project scope. Also, the inductor is considered ideal and is taken as air core to not saturate at the operating currents as well as its inductance is assumed to be constant for the test duration.

1.3.3 Limitations

The project aims to resolve only the current imbalances in the system and does not focuses on analyzing the gate-emitter and collector-emitter voltages. However, the switching is ensured with sufficient dead time for shoot-through protection.

A single frequency of 10 kHz is taken for impedance extraction to lower the computation time. This frequency is of high importance as the industry wishes to evaluate the switching frequency from 4-10 kHz operation for its IGBTs and MOSFET power modules. Although, this is a quasi-static analysis done using the Double Pulse Testing, this influence and behavior of system at this ramp up frequency shall provide insights into the device operation.

For the Double Pulse Test, since the input is a DC voltage which essentially becomes a step response during the switch operation. Therefore, an impedance matrix computed at single frequency and further circuit model based on it will contain an error margin which shall impact the accuracy of the model. A reduced order model is an approach to help with the circuit analysis combining the output at various frequencies and developing a state space model of the parasitics valid for a range of frequencies. However, taking the project timeline into consideration, this approach might not be completely feasible.

1.3.4 Trade-off Analysis: Utilization vs Developmental Cost

This thesis aims towards investigating the integration of FastHenry and MATLAB for automation, and in-depth analysis of the test system. It is worth questioning the credibility of the optimization tool along the development time and further analysis prospects.

"Since it is targeted towards a single objective and the scope of modification is limited, will it be an investment or a tedious activity saving small time which is far less than the development time of the tool?"

Despite the model's narrow focus, the development of a dedicated optimization tool proves to be a worthwhile investment. While manual tuning might yield comparable results in simple cases, the tool provides substantial benefits in terms of automation, repeatability, and design exploration:
The tool serves various important purposes as mentioned below:

- **Scalability** – The tool supports configurations with 2 to 4 parallel power modules, allowing flexible adaptation to future design iterations where minimizing layout-induced parasitics becomes increasingly critical.
- **Customizability** – Designers can control the number, shape, and positioning of cutouts, as well as the point-of-load connection. This enables a tailored balance between computational load and model precision depending on the use case.
- **Sensitivity Analysis** – The automated nature of the tool facilitates parameter sweeps and sensitivity studies, helping highlight design variables with the most significant influence. This accelerates debugging and supports informed decision-making.

1.4 Thesis Outline

This chapter is dedicated to familiarize the reader with the overall structure of the thesis based on the sequential chapters.

Chapter 2 is divided into two main parts. The first part focuses on the modeling of the Double Pulse Test (DPT) setup using FastHenry in combination with FreeCAD. It introduces the rationale behind the model development, outlines the step-by-step process followed, and discusses the complexity involved in creating an accurate and functional model. The second part presents the development of an optimization tool designed to minimize impedance imbalance, which is critical for ensuring equal current sharing among paralleled power modules. The tool takes the FastHenry script as a reference for modification in the model. It details the modifications made to the model, the constraints applied, and the optimization process used to achieve the lowest possible impedance. The goal is to enhance the model's output by systematically refining its parameters within defined limits.

Additionally, this chapter discusses the development of an analytical model for post analysis of the output from the optimization tool. It applies KVL to the DPT loop including the parasitics obtained. It helps to compute the power module current values at the time point of interest.

Chapter 3 displays the lab setup and identifies the components of the Double Pulse Test (DPT). It provides the specifications of the system components and the measurement devices for monitoring operation.

Chapter 4 presents the testing procedure and operating conditions for the Double Pulse Test (DPT) setup. The testing is done for three variants of the busbar at different points of load connection. The testing is done step-by-step to analyze the simulation and measurement results for comparing their current sharing to analyse the accuracy of the Fast Henry Model.

Chapter 5 does the analysis obtained results including parameter sweep for sensitivity analysis, current density and distribution in the system and fidelity analysis for accuracy of simulations with the measurements.

Chapter 6 concludes the thesis with the results, findings, learnings and oversights, taking the whole project duration, manpower and available resources into account. This paves the way for further developments on the project and how it can be improved and what directions could be some of the methods towards further developing the project into a more adoptable version. The future works needs to mend the project to make it more refined, computationally faster and user friendly. This section presents the possible directions of the project for future developments.

Chapter 2 Modeling

2.1 FastHenry Modeling

To accurately characterize the parasitic interactions in a Double Pulse Test (DPT) setup for paralleled power modules, including IGBTs and MOSFETS, a dedicated electromagnetic model was developed using FastHenry.

This modeling effort was driven by the need to capture parasitic inductances that critically influence the current sharing of the paralleled modules. The model serves as a foundational tool for evaluating layout strategies, optimizing interconnect geometries, and ensuring reliable operation of modern power electronic systems.

As mentioned in the section 1.1, capturing the parasitics for busbars and ambiguous layouts is difficult and a software like FastHenry can be a useful source for implementing and analysing the test bench for the project.

The software provides integration with FreeCAD, facilitated by tools such as the export-to-FastHenry python script from the EM Workbench project. This significantly enhances the modeling workflow by providing a visual and parametric interface for geometry creation. It allows user to design and visualise complex 3D conductor layouts which can be translated directly to a FastHenry compatable code. This workflow empowers engineers to iterate quickly, visualize parasitic paths, and better understand the physical layout's impact on electrical performance.

The development of FreeCAD models using EM workbench were referred using the resources available online [30], [31] and [32] which were essential learning materials for providing both theoretical background and practical modeling support. It is worth mentioning KK Wind Solutions to provide a reference FreeCAD model to speed up the model development process. I am grateful to the company for such important contribution for the project. With modifications to the switch-node busbars, adding load connection cables and required nodes and ports, the model could be used for further computations.

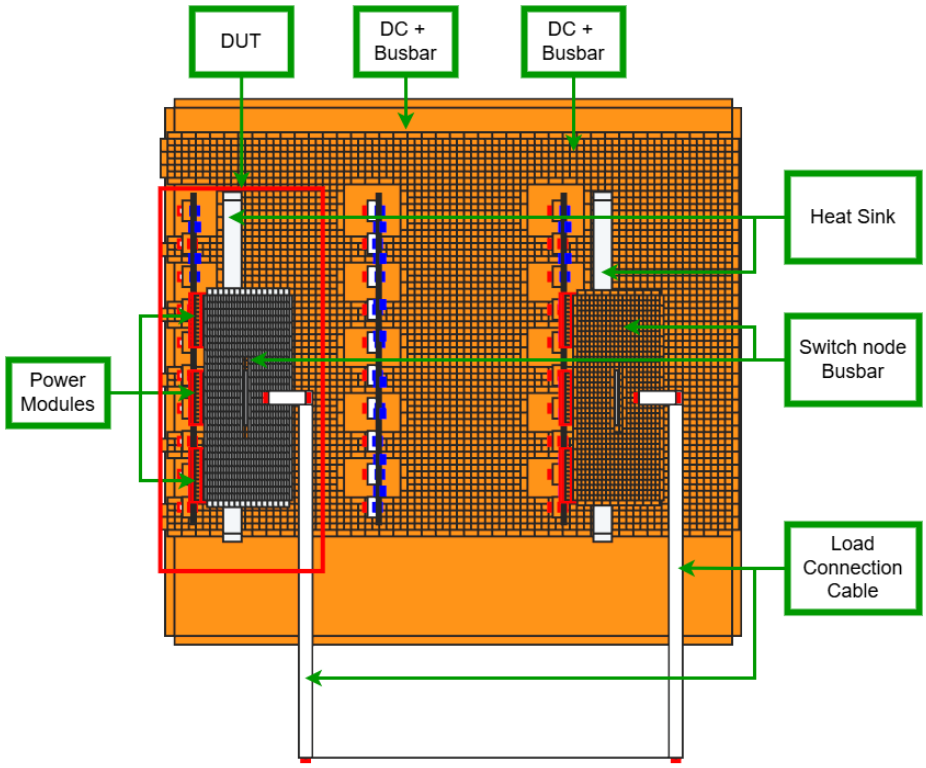


Figure 2.1: Complete FreeCAD Model

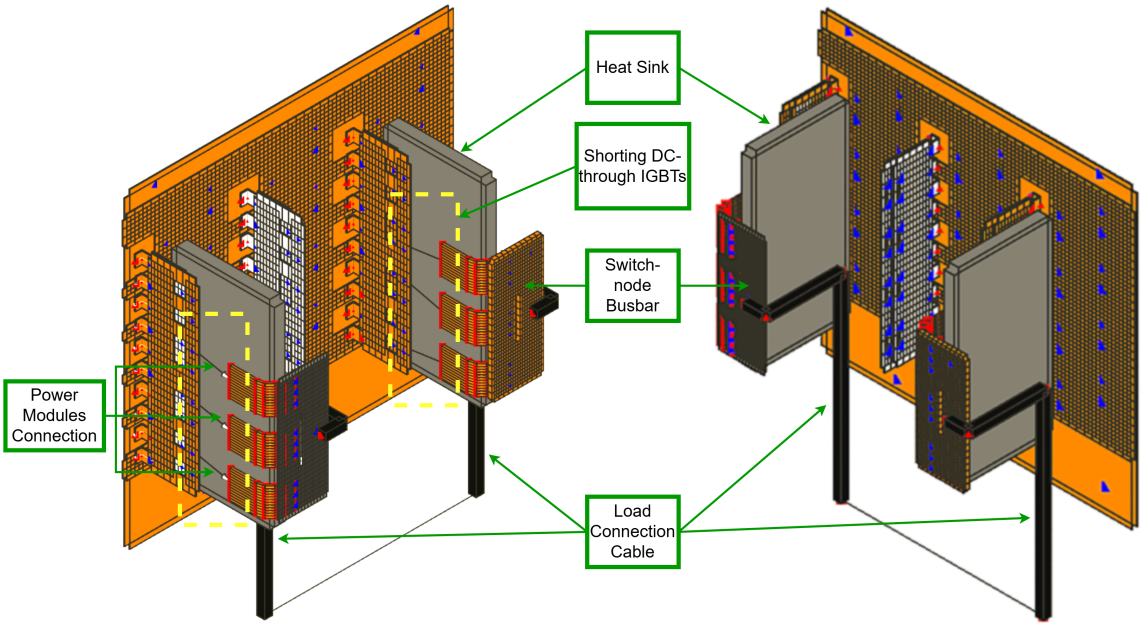


Figure 2.2: FreeCAD Model - Orthogonal View

The model shown in figures 2.1 and 2.2 represent the digital design of the test bench at KK Wind Solutions. The ports are connected on the DUT for visualization of impedance seen by the top IGBT of power modules.

There are certain critical details for the model as shared below:

1. DUT Switch node busbar is made of Aluminum for testing purposes. The busbar conductivity is taken as 35,000 S/mm. For all the other conduction path, the default conductivity is taken as 58,000 S/mm for Copper.

2. The DC link capacitors are shorted to avoid their influence in impedance analysis. Consideration of internal parameters like ESL and ESR shall provide more realistic flow of currents based on the placement of the capacitors and the DC link busbar resistance. It is however difficult to model since we are analysing in Fast Henry environment.

3. The auxuliary power modules for testing the DUT has bottom IGBT of power module turned ON before starting the test. It provides the path for current to flow from switch node to DC-. In the model however, the DC - is shown shorted with the braided busbar assuming IGBTs are always ON.

4. Heat sinks are modeled in the system to take into account the eddy currents generated due to magnetic coupling of the load cable and the nearby busbars.

5. The load cable length is kept larger than 500 mm so that to avoid the change in mutual coupling when the load point of connection sweep is done. From the previous semester [25], it was concluded that if the length of the cable is larger than the switch-node busbar, then the change in influence of the busbar's mutual coupling can be neglected for further increase in length.

6. The solver frequency is set to *10 kHz* to match the module's switching frequency specified by KK Wind Solutions. Skin effect was not modeled due to complexity in applying skin depth across the uniform conductive plane, though it would improve accuracy of the results.

There is a good correlation to the segmentation and skin depth given in the user manual [33] for fine tuning of the model. The discretization of filaments in a segment (for eq. load cable, and braided busbars etc.) for emulating skin effect can be referred to in **Appendix A.2**. These are not extendable to busbars (uniform conductive plane).

Nonetheless, This model provides a solid foundation for further development and analysis of the system's parasitics. This model is then exported to FastHenry for processing and obtaining the corresponding impedance matrix.

For developing an understanding on the FastHenry model, simulation, operation and command line interface, two resources were referenced — FastHenry User Guide - Part 1 [33] , and the FastHenry2 GitHub repository by ediloren [34]. The *FastHenry User Guide* provides foundational theory, usage instructions and advanced techniques like automation facilitation, current density plots etc. making it essential for understanding solver's capabilities and limitations. And, the *FastHenry2 GitHub repository* by ediloren extends the original solver with enhancements such as Windows compatibility, GUI support, and integration scripts such as SPICE netlist generation, making it more accessible and practical for modern engineering workflows.

The paper "FASTHENRY: A Multipole-Accelerated 3-D Inductance Extraction Program" [35] introduces a fast, scalable solver for computing frequency-dependent inductances

in complex 3D geometries using multipole acceleration. Complementing this, "Efficient Techniques for Inductance Extraction of Complex 3-D Geometries" [36] presents numerical strategies like preconditioned iterative solvers and optimized discretization. These papers helped in the utilization of functions for computing the impedance matrix in FastHenry.

This project progresses to exploit the automation facilitation of FastHenry. MATLAB is used for running the automation commands. The reference FastHenry file created using FreeCAD is loaded, the FastHenry program is run in the background and the obtained impedance matrix is stored against frequency in the MATLAB workspace.

Since the FastHenry script, command and operations are accessible through MATLAB, this provides opportunity for defined loops, carrying out sensitivity analysis using sweeps, modification of different elements of the model to add/remove components, increase/decrease the complexity and details on each busbar and cable assembly. This opens up greater possibilities to play around with the model. The optimization techniques and tuning of parameters are discussed in the next section.

2.2 Design Tool Modeling

Genetic algorithms (GAs), as detailed in Metaheuristics for Hard Optimization [37], are particularly effective for solving complex, high-dimensional optimization problems where traditional methods struggle due to nonlinearity, multi-modality, or lack of gradient information. In the context of layout parasitics matching—where the goal is to minimize impedance mismatches caused by parasitic effects in circuit layouts—GAs offer a robust population-based search strategy that can explore a wide design space and adaptively converge toward optimal or near-optimal configurations. Their ability to balance exploration and exploitation through crossover and mutation makes them especially suitable for navigating the intricate trade-offs inherent in parasitic-aware layout optimization.

Since FastHenry scripts are text-based, modifications can be made directly using MATLAB without relying on FreeCAD. However, because this alters the standard process flow, it is crucial to proceed carefully and develop the process step-by-step to ensure accurate results. A reliable approach is to consistently compare the output generated by the optimization tool with the output from FreeCAD, allowing for avoiding errors.

For the project, as mentioned in chapter 1, we proceed to modify only the DUT switch node busbar and the point of load connection in the scope of the project. Other parts of the system remain as is.

2.2.1 Development of the optimization algorithm

Implementation of GAs is possible on the FastHenry script due to the possibility of controlling the FastHenry program using MATLAB. There are certain steps followed towards creating the optimization tool.

Initial Validation
Using the FreeCAD model shown in figure 2.3 from the previous semester, [25], for two modules paralleling was used as a reference for development.

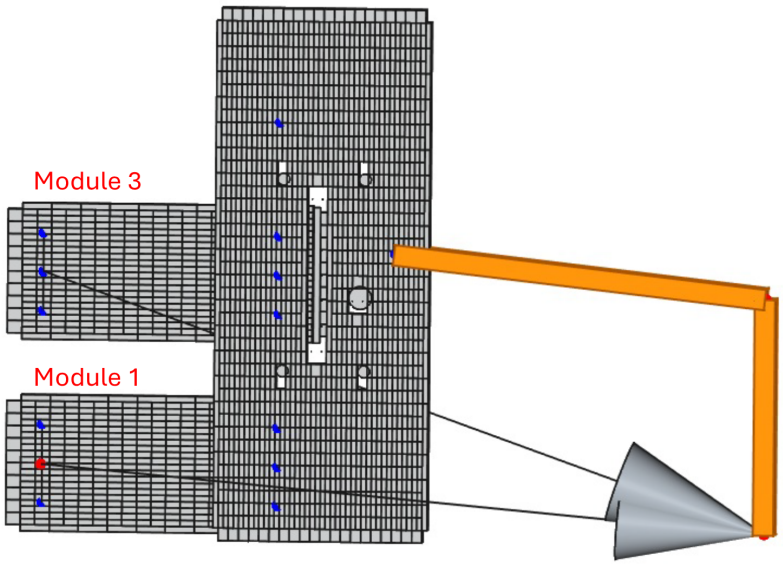


Figure 2.3: Fast Henry Model with two modules

An iterative method was developed to alter the position and size of the rectangular cutout in MATLAB. It was done to explore the automation potential of FastHenry through MATLAB. This approach enabled a sweep of the cutout across the busbar within the system constraints. It was found that the current imbalance came to 1/6th of the observed value during experimentation. With these results, it was ensured that the studying these cutouts impact is germane to our impedance analysis.

This approach was essential and accurate although, it was rudimentary since it requires high number of variables, nested loops and was highly time consuming to approach a solution. Therefore, the optimization techniques were explored in section 1.1 to find a solution for the complex non-linear system. The iterative approach here provides a good reference for comparing genetic algorithm accuracy, effectiveness and speed for further development.

Figure 2.4 shows the flow chart for Fast Henry Automation representing the steps involved for the processing of results and obtaining minimum current imbalance.

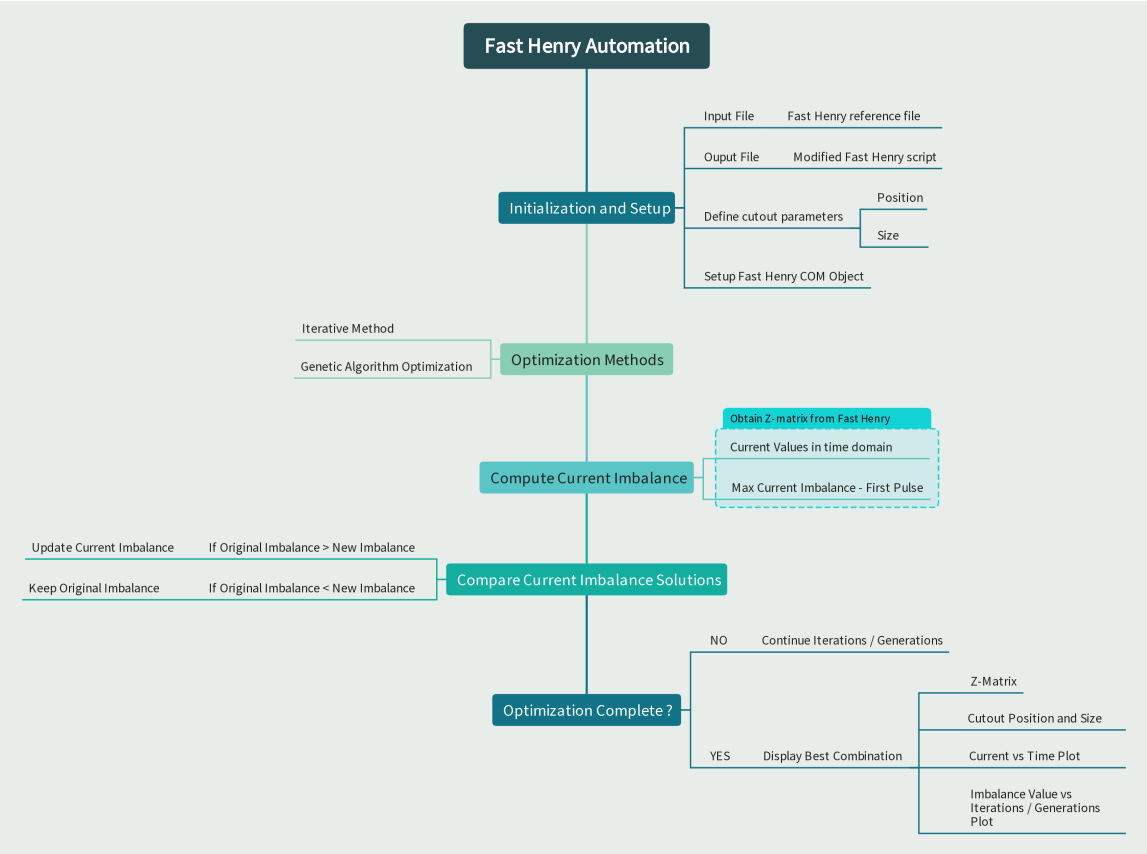


Figure 2.4: Fast Henry Automation Work Flow

The Genetic Algorithm (GA) optimization, it was configured using MATLAB's optimoptions function to optimize the performance of the solver. Each option was selected to balance solution quality, computational efficiency, and robustness. Below is a explanation of parameters used:

1. **Population Size:** This parameter defines the number of individuals in each generation. The paper, "Genetic Algorithms, Noise and the Sizing of populations" [38] examines how impacts Genetic Algorithm (GA) performance and proposes a population-sizing model to maintain reliable selection of building blocks. The model is validated using test functions, demonstrating that correct population sizing ensures better convergence and solution quality in GAs.

   The population size N in a Genetic Algorithm can be determined using the following equation:

$$N = 2ck\left(\frac{\sigma_M^2}{d^2}\right) \tag{2.1}$$

   where:

   - N = required population size
   - c = constant (related to confidence level)

- k = number of building blocks (or number of variables)
- σ_M^2 = variance of the fitness of building blocks
- d = difference in fitness between the best and second-best building blocks

The theoretical value comes around 20 for the minimum population size using this formula. A population size of 50 is chosen for the experiment which provides a good enough population size providing reasonable trade-off between genetic diversity and computational cost.

2. **Max Generations:** This sets the maximum number of generations the algorithm will run. It acts as a termination criterion to prevent infinite execution. A limit of 100 generations allows sufficient opportunity for convergence while maintaining practical runtime constraints.

3. **Crossover Fraction:** This specifies the proportion of the next generation that is produced through crossover (recombination of parent solutions). For this evaluation the default *crossoverscattered* is used. It creates a random binary vector to choose the traits from each parent. A value of 0.8 emphasizes exploration by combining traits from different individuals, which helps in discovering better solutions.

4. **Mutation Function:** The mutation function introduces random variations to individuals, promoting diversity. The mutationadaptfeasible function adapts the mutation step size and ensures that mutated individuals remain within feasible bounds, which is particularly important for constrained optimization problems.

5. **Stall Generation Limit:** This parameter defines the number of generations with no improvement in the best fitness value before the algorithm terminates. This is combined with the maximum generations limit to form a pragmatic stopping criteria for the algorithm. A decent value of 5 stall generation ensures that the algorithm stops if it is no longer making progress, thus saving computational resources. It provides sufficient generations for the solution to diversify and avoid local minima.

6. **Output Function:** A custom output function is specified to execute at each generation. This function was used to log intermediate results such as population history, generation progression, best outputs for each generation etc., and visualize progress using plots. The implementation of *gaOutputFcn* is tailored to the specific needs of the project. Details of the function can be referred to in **Appendix B**.

7. **Parallel Processing:** Enabling parallel computation allows the fitness function to be evaluated simultaneously across multiple cores or workers. This significantly reduces computation time, especially for expensive fitness evaluations. The program enables the choice of assigning number of cores to make it feasible for designer to carry out other tasks alongwith running the GA computation.

8. **Elite Count:** specifies the number of individuals that are guaranteed to survive to the next generation. To ensure good solutions are not lost in the earlier generation 2% of the best population goes to the next generation as is.

9. **Creation Function:** The default function *gacreationuniform* initializes the population randomly using a uniform distribution within the specified population range adjusted to fit the defined lower and upper bounds.

10. **Selection Function:** The selection function *selectionstochunif* selects parents using stochastic uniform selection, where individuals are chosen based on their scaled fitness values divided proportionally.

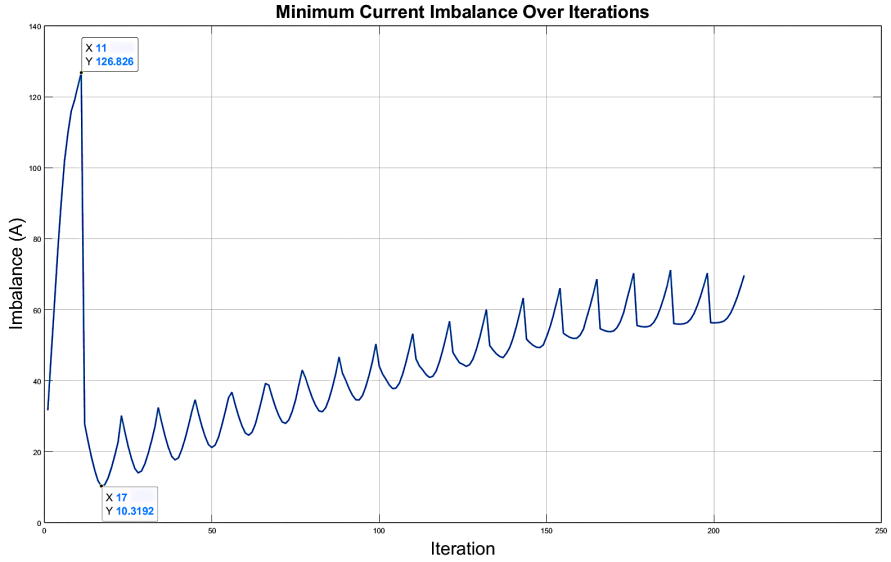
The options used for the GA help towards a systematic development of GA solver. As the problem explores more dimensions and becomes more complex, the values of these options are updated to suit the required convergence.

Comparing the two approaches, It was found that the time for reaching the same minima point by genetic algorithm within the same constraints came to half of the iterative approach, however, it was seen that 1 out of 4 times the algorithm was stuck at a local minima. Penalty application is an effective technique to avoid this issue, therefore the penalty methods were explored.

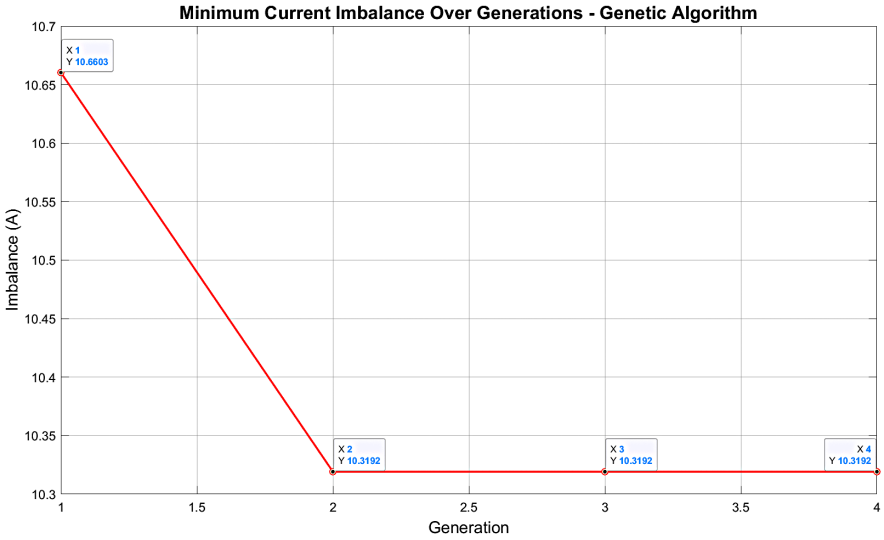
This study explores the integration of penalty function methods within genetic algorithms (GAs) for solving constrained optimization problems. Drawing from the paper "A Brief Review of Penalty Methods in Genetic Algorithms for Optimization" [39] and the applied framework in "Constrained Optimization Using Penalty Function Method Combined with Genetic Algorithm" [40], it was examined how penalty functions can effectively transform constraint problems into unconstrained formulations by incorporating constraint violations into the fitness evaluation. The applied study demonstrates the practical implementation of these methods, emphasizing the importance of adaptive penalty parameter tuning to guide the evolutionary process toward feasible and high-quality solutions.

Parameter	**Iterative Method**	**GA Optimization Method**
Current imbalance optimal	10.3192	10.3192
Computation Time	31.5 minutes	17.4 minutes

Table 2.1: Comparison of Iterative Method and GA Optimization Method



(a) Solution Evaluation Graph - Iterative Method



(b) Convergence Graph - Genetic Algorithm

Figure 2.5: Comparison Iterative Method v/s Genetic Algorithm

The table 2.1 and figure 2.5, demonstrates that the GA optimization method produces the exact results for the current imbalance in nearly half the computation time. This outcome serves as a good reference to establish credibility of the GA approach. The ability of GA to achieve accurate results more efficiently highlights its potential as a robust optimization tool. This success opens the door for further exploration and refinement of the GA-based approach, including the integration of advanced selection, crossover, and mutation techniques. Future studies can focus on including larger system models, including more variables per power module for exploring scalability, and defining higher scope of system modification to achieve better results.

Full System Modeling

Upon positive results from the initial validation, a full model of the system was developed in FreeCAD as shown in figure 2.1. Further development on the optimization

algorithm takes place utilizing this Fast Henry script as the reference file.

In the initial investigation, fixed penalties worked well for the optimization procedure as the solution space was limited and the number of variables were also small.

For the complete system model, both fixed and gradual penalty approaches were taken into consideration by taking inputs from [39] and [40] papers.

The fixed penalty method, which imposes a constant cost for any constraint violation, was found to be less effective because it treated all violations equally, regardless of severity. As a result, the GA often spent more generations exploring infeasible solutions, leading to slower convergence. In contrast, the gradual penalty approach dynamically adjusted the penalty based on the extent of the violation, providing a more nuanced guide for the optimization process. This adaptive approach effectively directed the GA to gradually reduce constraint violations, accelerating convergence and improving the quality of solutions by maintaining focus on feasible regions of the search space.

The table 2.2 below provides an overview of the dynamic penalties introduced. For details on the code, **Appendix B** can be referred.

Genetic Algorithm Penalties		
Quadratic Penalty (for Boundary Violations)	**Geometric Penalty (for Overlapping)**	**Proximity Penalty (for Diversity)**
The penalty for violating boundary constraints is calculated as the square of the violation magnitude.	Penalty is based on the calculated overlap area between two geometric shapes (rectangles or circles).	Penalty is calculated based on the proximity of the current solution to other solutions in the population.
$\text{Penalty}_{\text{Boundary}} = k_{\text{violations}} \cdot (\text{violations})^2$	$\text{Penalty}_{\text{Overlapping}} = k_{\text{overlap}} \cdot (\text{overlaparea})^2$	$\text{Penalty}_{\text{Diversity}} = 1 + \frac{\min(\text{distance})}{k_{\text{diversity}} \cdot \text{diversity}}$

Table 2.2: Dynamic Penalties for GA Full Model

The constants can be tuned to be severe or soft penalty values based on the solution requirement for the GA. For each member of the generation evaluated, goes through the penalty function according to the suitable penalty it falls into else there is no penalty added to the solution value.

The optimization tool is developed step-by-step improving the design, computational time and robustness of the tool. There are three stages of development involved:

1. **Relative Current Computation** - The current computation is done using the values of impedance matrix at a desired frequency obtained from the Fast Henry results. Using Kirchhoff's law for calculating voltages in the circuit and applying Forward

Euler Method for integration in time domain, the max current values and maximum current imbalance for the first pulse are obtained.

$$
\begin{aligned}
\mathrm{dt} &= \Delta t \\
n_{max} &= \frac{t_{total}}{\Delta t} \\
v_{total} &= v_R + v_L \\
\mathbf{i} &= \begin{bmatrix} i_1(t) \\ i_2(t) \end{bmatrix} \\
\mathbf{Z} &= \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix}
\end{aligned}
$$

$$
\begin{aligned}
\mathbf{v}_R(:,n) &= \mathrm{Re}(\mathbf{Z}) \cdot \mathbf{i}(:,n-1) \\
\mathbf{v}_L(:,n) &= \mathbf{v}_{tot}(:,n) - \mathbf{v}_R(:,n) \\
\mathbf{i}(:,n) &= \mathbf{i}(:,n-1) + \mathbf{Z}_{imag}^{-1} \cdot \Delta t \cdot \mathbf{v}_L(:,n)
\end{aligned}
$$

$$
\begin{aligned}
\text{Current Imbalance} &= |i_1(t_{imb}) - i_2(t_{imb})| \\
where, t_{imb} &= t_{total} \times \frac{t_{imb}}{t_{total}}
\end{aligned}
$$

A voltage is injected initially and iterated at each Δt to reach the desired current value. This is a good approach to find the absolute values of currents although there are certain methods such as Runge-Kutta method which are more accurate for finding the solution.

The existing approach of calculating absolute current values for each population member is computationally expensive due to the need for multiple loops and complex numerical integration. This not only increases the iteration time but also hinders the efficiency of the optimization process. To address this, a more efficient method is adopted, where a relative value of current is determined using a single voltage injection, and the imbalance among the modules is quantified using the variance of the resulting current values. Variance is chosen because it is a general measure of dispersion, making it applicable to any number of modules, whether two, three, or more. It effectively captures both the total imbalance (overall variance) and individual imbalances (deviation of each module's current from the mean). This method significantly reduces computational complexity while maintaining accuracy in detecting current imbalances.

2. **Introducing More Variables** - Following from the start of GA development, there has been a single rectangular cutout whose size and position are being altered to bring out the desired solution for the GA current equalization. Due to a single

cutout, limited flexibility is offered to carryout the impedance matching. Also taking other factors into consideration such as reduced busbar strength due to large cutout, higher temperature rise due to lesser path for current flow and also offering current balancing only to a certain extent necessitates the inclusion of smaller cutouts at the localized points keeping the material strength intact and offering higher flexibility of modifications in the layout. Therefore, the introduction of more variables to the solution space makes logical sense.

As a first step, typically two types of cutouts were considered, namely, rectangular and circular. These shapes are easily adoptable in the script. The GA optimization assigns certain number of circular and rectangular holes based on the accuracy, complexity and computational cost to the solution space.

As each cutout type has its own characteristics, therefore, higher number of cutouts adds to the processing time while providing more variables to the algorithm to explore the minima point. Although, more computations are needed for the optimization, but the solutions are more refined and adept.

To ensure that cutouts remain within the defined solution space, users are allowed to specify the lower and upper bounds for the cutout parameters. Based on these bounds, the boundary conditions for the start and end points of the cutout are automatically updated. This dynamic adjustment prevents the generation of out-of-bounds cutouts. Additionally, the penalty function guides any out-of-bounds solutions gradually back into the feasible region, promoting convergence. Strict upper bound constraints are also enforced to minimize the risk of overlapping cutouts and to ensure compliance with boundary conditions.

Cutout Definition - For defining the cutouts, certain set of variables were assigned to each type, which aligns with the definition in FastHenry as well as easier for the user to define the parameters. The z-coordinate remains the same for the cutout as the movement of cutout is along x and y plane.

- **Circular Cutout** – A circular cutout is defined by three parameters: the center coordinates (x,y) and the radius r. These variables determine the position and size of the circle. This format is directly compatible with FastHenry's input syntax: + *hole circle (x, y, z, radius)*. For present computations, maximum radius of cutout is considered as 10 mm.

- **Rectangular Cutout** – A rectangular cutout is characterized by four parameters: the starting point ($x1$,$y1$), along with the length and width of the rectangle. This representation provides a clearer understanding of the cutout's dimensions. Although this format does not directly match FastHenry's required syntax + *hole rect (x1, y1, z1, x2, y2, z2)*, the conversion is straightforward. The length and width can be used to compute the opposite corner coordinates, enabling easy adaptation to the required format. For present computations, maximum length and width of the cutouts is considered as 20 mm each.

Different Points of Load cable connection - As observed in the last semester, the rotation of load connection cable had an influence on the current sharing of the modules. Therefore, it is important to parameterize the influence of proximity of the load connection cable from the power module and the distance of the cable from the switch-node busbar.

To facilitate this analysis, two key positional variables are introduced: one governs the location of the load connection along the y-axis on the switch-node busbar, and the other defines the z-axis distance of the load cable from the DC-link busbar. A parametric sweep is conducted—first along the y-axis and then along the z-axis—to systematically evaluate the impact of these parameters on system behavior.

The y-axis position of the load connection influences the direction and distribution of current flow from the modules to the load point, as well as the degree of mutual coupling introduced by the load cable. Meanwhile, the z-axis distance from the DC-link busbar affects the strength of magnetic field interactions between the load cable and the switch-node busbar, thereby influencing electromagnetic coupling. Together, these two parameters play a critical role in layout optimization, offering valuable insights into how proximity and positioning of load cables affect system performance during operation.

Both increasing the number of cutouts of different types and points of load connections are integrated into the code for complete control of the solution space using the affected parameters. This makes the GA efficiently work towards finding the optimal solution for the external layout impedance matching.

3. **Scalable Design** - This is the last step towards building the algorithm. Since all the variables are put into place and the cutouts and cables positions are integrated, it enables the design tool to create a diverse population converging towards a minima. Still there are a few considerations to be taken into account before going into manufacturing.

   Scalability is one of the defining strength of this tool, directly contributing to its long-term utility and justifying the initial development cost. To accommodate varying system complexities, the tool is designed to construct solutions for multiple configurations—specifically, two, three, and four modules connected in parallel. Developing support for each scenario adds to the versatility of the tool and enhances tool's practical utility. By enabling automated handling of diverse layout challenges across configurations, the tool reduces manual intervention, accelerates design iterations, and supports broader application.

   To enable this, the solution space is divided into sections pertaining to each power module with a margin of 20 % on each side of the power module connection.

   For each module, it is possible to assign certain number of cutouts both circular and rectangular to balance the impedance for the complete layout. Since, the sections

are divided module-wise, it is possible to extend the number of modules and the variables assigned to each section can be replicated with increasing module numbers. Connecting modules with the sections of the solution space makes sure that each module is solved individually as well as a complete solution without manually adding/removing parameters every time there is an increase/decrease in the number of paralleled modules.

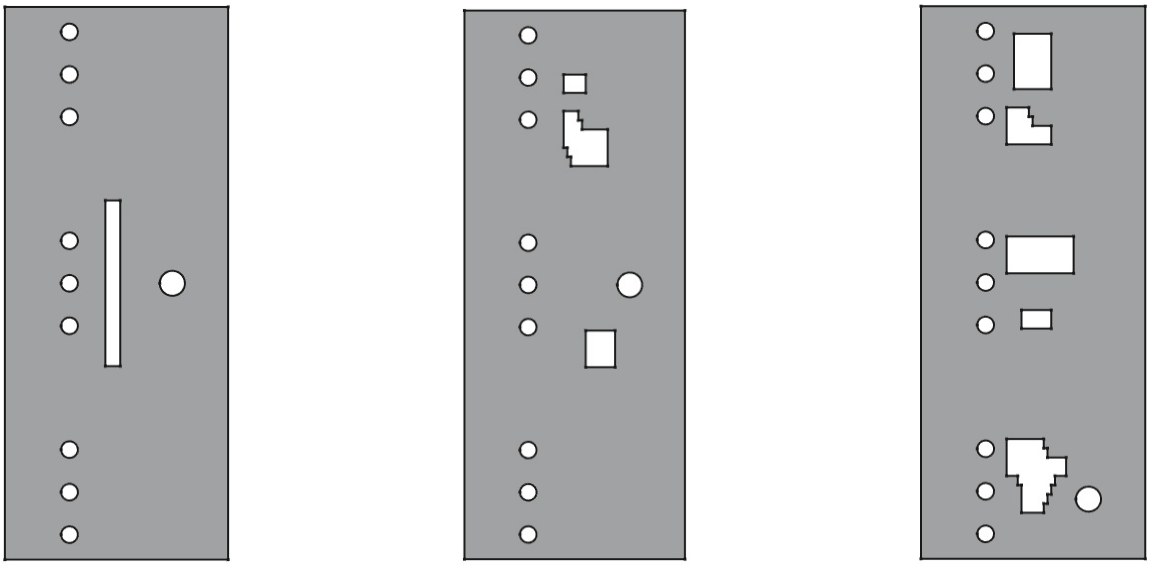
Secondly, To make sure sufficient number of cutouts are assigned to each solution section without over burdening the tool's penalty function for meeting the boundary and overlapping criteria, an existance variable is introduced against each cutout. This shall limit the number of cutouts to the section where not many are required for the balancing while making sure enough cutouts are available to balance out the highly disproportionate sections of the system.

Each decision variable in the optimization problem is defined over a continuous range and is therefore treated as a real-valued parameter, allowing for smooth and incremental variation during the optimization process. However, the *existance* variables—used to represent binary decisions such as the presence or absence of specific features—are inherently discrete and must be restricted to integer values (0 or 1). To accommodate this mixed-variable structure, the genetic algorithm is configured for **mixed-integer optimization**, where only the existance variables are constrained to be integers, while the remaining variables are optimized as continuous real numbers.

This is implemented using the `IntCon` parameter, which explicitly defines the indices of the integer-constrained variables. The `CreationFcn` is set to *@gacreationuniformint*, a function that respects these constraints by generating integer values for the specified variables, all within the bounds defined by `InitialPopulationRange`. This configuration ensures that the initial population is both valid and diverse, with each individual adhering to the appropriate variable types. Throughout the optimization process, the genetic algorithm maintains these constraints, enabling efficient and accurate exploration of the solution space while preserving the integrity of the problem formulation. The complete code for GA can be referred in **Appendix B**

Considering all three steps of the GA development, three variants of the switch-node busbar are developed for lab testing to validate the Fast Henry model as well as the GA optimization algorithm.

Following are the three variants developed:



(a) Variant 1 **(b)** Variant 2 **(c)** Variant 3

Figure 2.6: Switch-node busbar variants for Lab Testing

It can be seen from figure 2.6, variants produced using the Genetic Algorithm. The Variant 1 having a single rectangular cutout was directly taken from a reference busbar for evaluation, The Variant 2 having multiple cutouts with mid-point load connection and Variant 3 having multiple cutouts with end-point load connection along with different distance from the DC Link as well are produced by the optimization tool. These three variants shall be used for testing in lab for verification of the credibility of the Fast Henry model as well as the design tool.

2.3 Analytical Modeling for DPT

In this section, the analytical model of the system is presented for calculating the current values through each power module and finding the percentage imbalance across the modules. The model also takes into account the manufacturer-provided forward voltage drop and inductance values.

Since the design tool outputs three variants of different complexity considering three power modules in parallel adhering to the test specifications. The analytical model is also developed for three paralleled power modules.

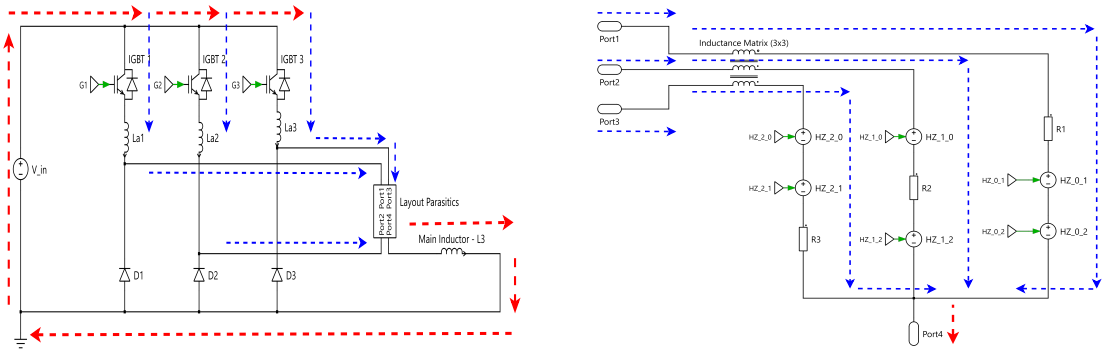
To investigate the influence of load cable positioning on current imbalance, the system evaluates three distinct configurations using impedance matrices derived from different layout variants. The analysis is structured in three phases. The distance mentioned on the z-axis is the distance from the DC link and the load connection cable:

1. **Mid-point connection at z = 153 mm:** The impedance matrices corresponding to the mid-point connection of the load cable are applied across all three layout variants.

2. **End-point connection at z = 153 mm:** The load cable is connected to the end of the busbar, positioned 153 mm from the DC link busbar, and is evaluated for the three variants.

3. **End-point connection at z = 103 mm:** The same end-point connection is analyzed again, but with the load cable placed 103 mm from the DC-link busbar.

For each configuration, the corresponding impedance matrix is used to solve the symbolic current equations, yielding the absolute values of the power module currents. These values are then used to compute the percentage imbalance, defined as the deviation of each power module current from the mean current. This methodology enables a quantitative comparison of how these different variants affect current distribution among the power modules. The results provide insights into the impact of layout variations on electrical performance.



(a) Current Flow DPT

(b) Current Flow Subsystem - DPT

Figure 2.7: Kirchhoff's Law DPT

To analyze the current imbalance in a system with mutual inductance and resistance, we define the symbolic currents I_1, I_2, and I_3 for each path. The system is governed by the following equations using Kirchhoff's law:

$$\begin{aligned} V_{\text{in}} - V_{f1} = (L_{a1} + L_{b11})\frac{\Delta I_1}{\Delta t} + M_{12}\frac{\Delta I_2}{\Delta t} + M_{13}\frac{\Delta I_3}{\Delta t} \\ + R_1 I_1 + H_{12} I_2 + H_{13} I_3 + L_3 \cdot \frac{\Delta I_1 + \Delta I_2 + \Delta I_3}{\Delta t} \end{aligned} \tag{2.2}$$

$$\begin{aligned} V_{\text{in}} - V_{f2} = (L_{a2} + L_{b22})\frac{\Delta I_2}{\Delta t} + M_{21}\frac{\Delta I_1}{\Delta t} + M_{23}\frac{\Delta I_3}{\Delta t} \\ + R_2 I_2 + H_{21} I_1 + H_{23} I_3 + L_3 \cdot \frac{\Delta I_1 + \Delta I_2 + \Delta I_3}{\Delta t} \end{aligned} \tag{2.3}$$

$$\begin{aligned} V_{\text{in}} - V_{f3} = (L_{a3} + L_{b33})\frac{\Delta I_3}{\Delta t} + M_{31}\frac{\Delta I_1}{\Delta t} + M_{32}\frac{\Delta I_2}{\Delta t} \\ + R_3 I_3 + H_{31} I_1 + H_{32} I_2 + L_3 \cdot \frac{\Delta I_1 + \Delta I_2 + \Delta I_3}{\Delta t} \end{aligned} \tag{2.4}$$

Where:

- L_{ai}: Power Module inductance for module 1 , module 2 and module 3 i = 1, 2, 3
- L_{bii}: Self-inductance terms from the impedance matrix

- M_{ij}: Mutual inductance terms i = 1, 2, 3 and j = 1, 2, 3
- R_i: Self-resistance terms from the impedance matrix
- H_{ij}: Mutual resistance terms i = 1, 2, 3 and j = 1, 2, 3
- Δt: Time point of interest
- V_{f_i}: Forward voltage drop of IGBT
- $L3$: Main inductor

The system is solved symbolically to obtain I_1, I_2, and I_3. The mean current is computed as:

$$I_{\text{mean}} = \frac{I_1 + I_2 + I_3}{3}$$

The percentage deviation of each current from the mean is given by:

$$\text{Deviation}_i = \left| \frac{I_i - I_{\text{mean}}}{I_{\text{mean}}} \right| \times 100\%, \quad i = 1, 2, 3$$

The model is developed in MATLAB, and the equations can be solved for current shared by each module. This approach is effective as it offers the potential to use MATLAB's loops and optimization to find the solution that closely matches the real environment. It is possible to carry out a sweeps for range of the parameters to debug the model issues by comparison with measurement results.

Chapter 3 Laboratory Setup

In this chapter, the laboratory setup is presented for carrying out the Double Pulse Test (DPT) for testing paralleled power modules. It identifies different segments of the setup and their usage.

The experimental work for this study was conducted in a controlled laboratory environment designed to ensure precision, repeatability, and safety throughout the research process. The setup was tailored to meet the specific requirements of the study, incorporating specialized equipment, calibrated instruments, and standardized procedures.

As mentioned in chapter 2, three different variants of the busbar are prepared with varied complexity to obtain current balancing and establish credibility of the model with the prepared test setup.

3.1 System Identification

This section outlines the various segments of the Double Pulse Test (DPT) setup, providing a structured understanding of the system architecture. Each unit within the setup is identified along with its specific function, technical specifications, and role in the overall testing process. The segmentation helps clarify the system components, and measurement units to enable accurate and reliable testing of paralleled Si-IGBTs and SiC MOSFETs.

3.1.1 System Components

Following are system components:

Power Module
For the layout optimization, it is possible to parallel any power modules as they are considered ideal for the external layout optimization by the design tool. However, the impact of inter-module variance among the similar power modules units would be visible during testing which is not taken into account.

The project takes a Mitsubishi Si-IGBT half-bridge power module - **CM1200DW-40T** for testing. With rated voltage (*Vces*) of 2 kV and rated current (*Ic*) of 1200 A , this module is appropriate for the electrolyzer power supply application used by KK Wind Solutions.

The module structure and basic connection details are shown in the figure 3.1 below:

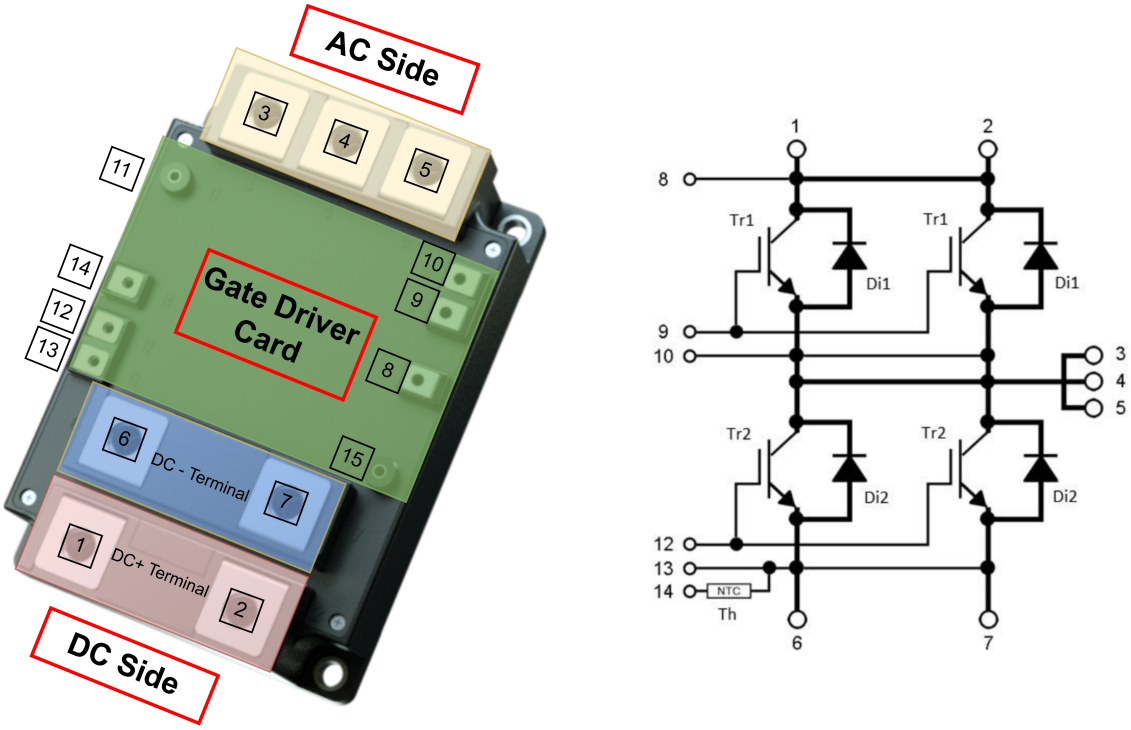


Figure 3.1: IGBT Power Module Structure and Connection Diagram

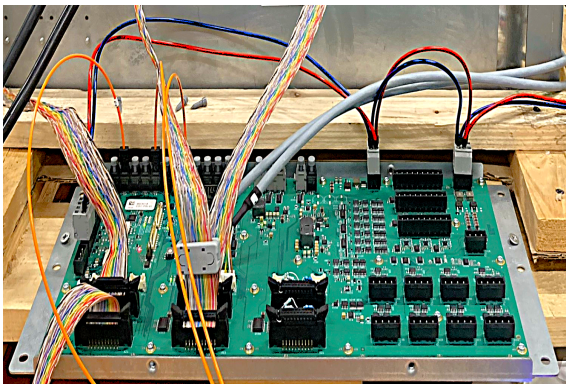
The specifications of IGBT Power Module in figure 3.1 are given the table 3.1.

Table 3.1: Specifications - 100mm IGBT Power Module

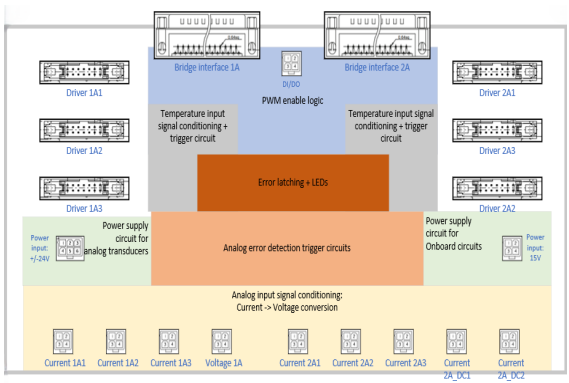
Parameter	Symbol	Rating
1. Collector-emitter voltage	V_{CES}	2000 V
2. Collector current	I_C	1200 A
3. Repetitive peak collector current	I_{CRM}	2400 A
4. Gate-emitter voltage	V_{GES}	$\pm$20 V
5. Collector-emitter saturation voltage	$V_{CE(sat)}$	2.15 V

COMIC Board

The COMIC board also known as common-interface board provides an interface between the KK controller unit and the master gate driver of the SiC MOSFET power modules.



(a) COMIC Board - Lab Setup



(b) COMIC Board - Block Diagram

Figure 3.2: COMIC Board

As shown in figure 3.2, the common interface board consists of auxiliary power supplies for the gate driver unit, condition monitoring capability including current, voltage and thermal measurements, and provides gate signals to and carry error or alarm messages from the gate driver to the KK controller unit.

Load Inductor

The load inductor is a crucial segment of the Double Pulse Testing. It is an air-core inductor as shown in figure 3.3. It is required for the ramp up operation and decides the di/dt at an applied voltage across its terminals and for power circulation during free-wheeling operation. The inductance value and current handling capability are the critical features to look into before selecting the inductor.

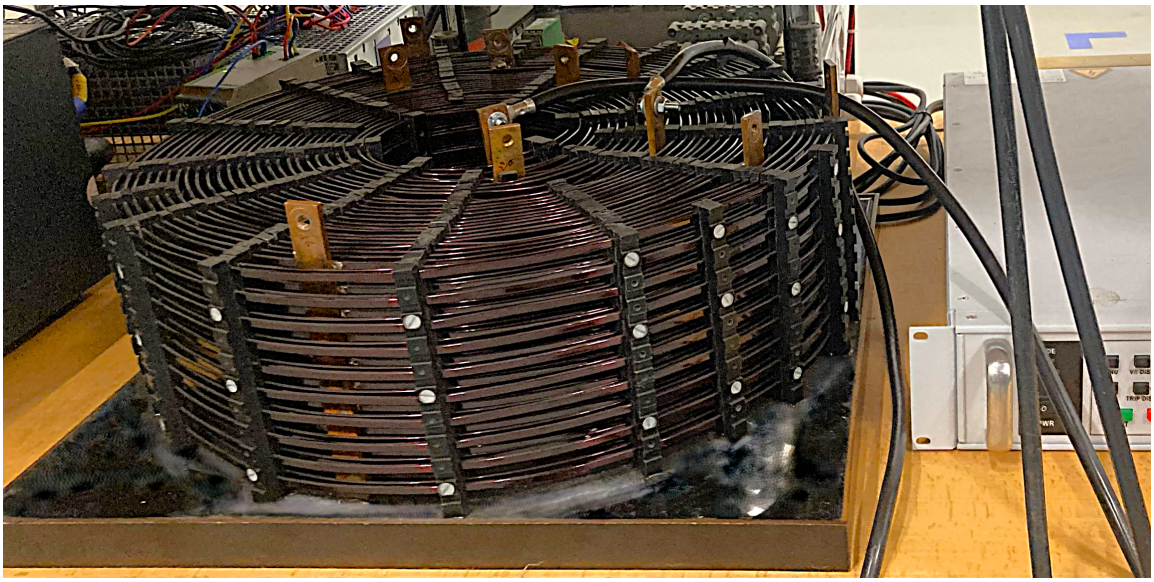


Figure 3.3: Load Inductor - Air Core

The nameplate details for the inductor was missing so the parameters were obtained through measurements by KK personnel. Following are the details of the inductor unit:

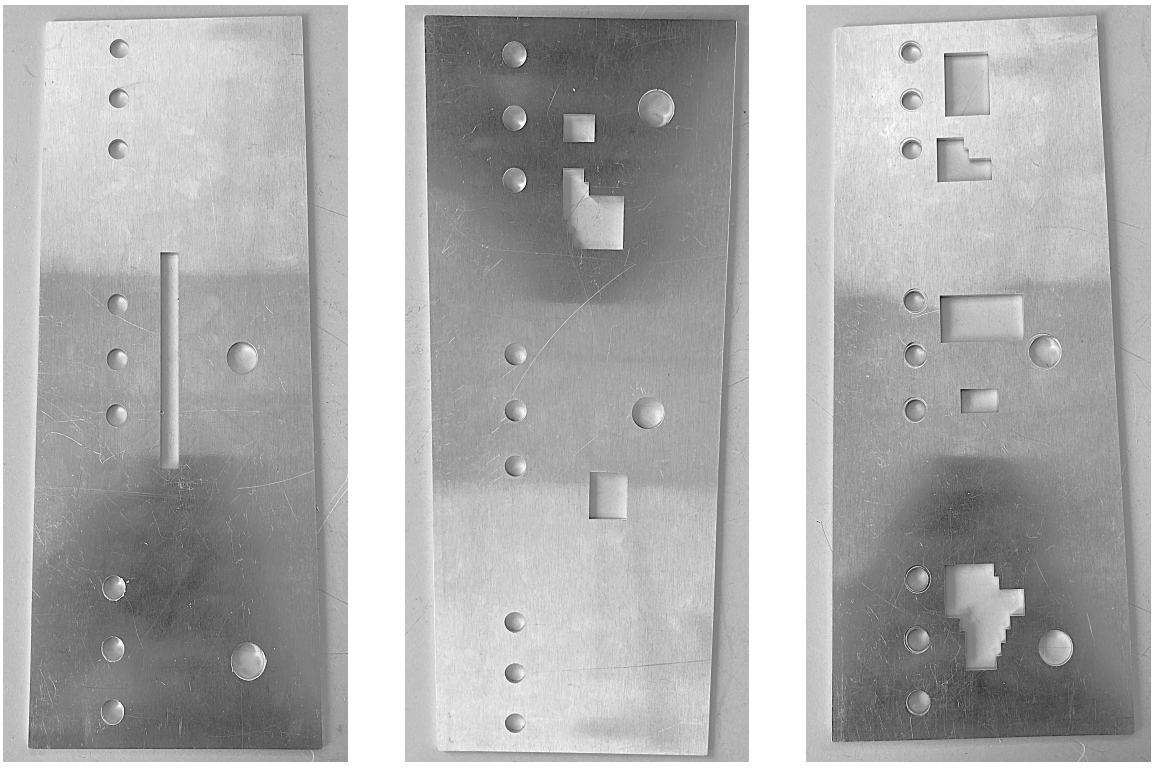
Table 3.2: Specifications - Load Inductor

Parameter	Rating
1. Type	Air Core Inductor
2. Connection type	1-phase multi point connection
3. Rated Inductance, L	20.7 μH connected, (Range - 3.38 μH to 120.8 μH on various tappings)
4. Tested current for DPT	2960A

For the initial calculations the tapping is chosen to get the value of 20.7 μH. As per the connection shown in the figure 3.3.

The DPT purposes, the inductance and current values of the inductor are sufficient to get the desired power circulation using the testing software available inside the lab.

Design Tool output - Busbar Variants
For testing purposes, the design tool outputs three variants based on the complexity of the solution desired by the user. With increasing variables, the solution convergence is improved. The realized variants are shown in the figure 3.4 below:



(a) Variant 1 Connection **(b)** Variant 2 Connection **(c)** Variant 3 Connection

Figure 3.4: Switch-node busbar variants for Lab Testing

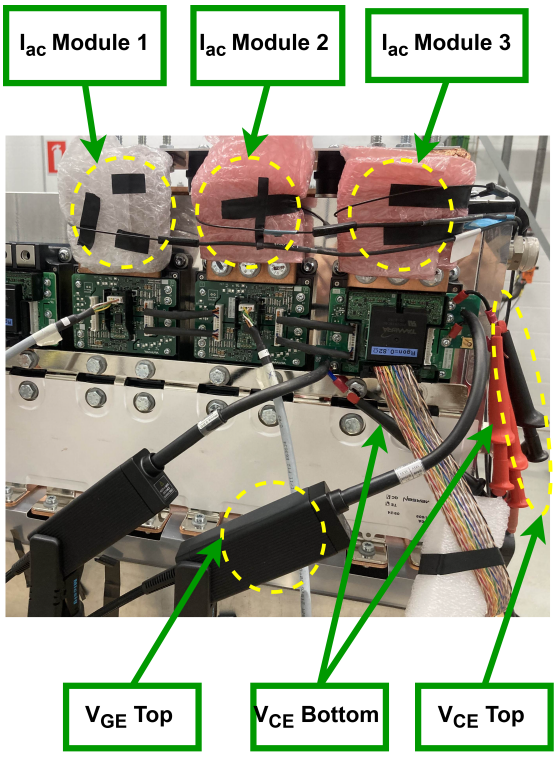
3.1.2 Measurement Equipment

The test setup uses the following measurement equipments for testing the system:

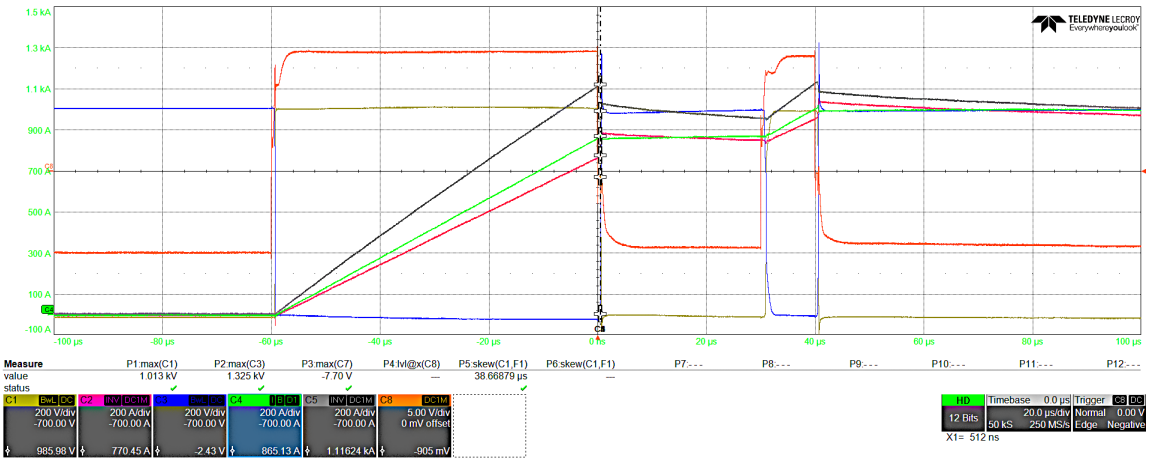
Measurement	Description	Type	Test Equipment
DPT Graph visualization	V_{CE} , V_{GE} and I_{ac} graph	Oscilloscope	LeCroy - WaveRunner 8058HD
Collector-Emitter Voltage (V_{CE})	1. Ch 1 - V_{CE} Top IGBT 2. Ch 3 - V_{CE} Bottom IGBT	Voltage Probes - Differential	LeCroy - HVD3206A-6M
Gate-Emitter Voltage (V_{GE})	1. Ch 8 - V_{GE} Top IGBT	Voltage Probes - Optical	Micsig - MOIP350P
Switch-node Current (I_{ac})	1. Ch 2 - I_{ac} Module 1 2. Ch 4 - I_{ac} Module 2 3. Ch 5 - I_{ac} Module 3	Current Probe - Rogowski coil	PEM - CWT Ultra Mini (30MHz) CWTUM/30/B

Table 3.3: Measurement Equipments

Figure 3.5a shows the connections of the measurement devices on the modules and the corresponding oscilloscope window against the measurements. The unused equipments remain connected in the system but are not monitored on the oscilloscope.



(a) Measurement Devices



(b) Oscilloscope Window

Figure 3.5: Lab Setup - Measurements

DC Link Capacitors

The DC link capacitor is required to stabilize the input voltage during the testing.

Following are the details of the capacitor:

Parameter	Value
Part Number	$E50.R14 - 424NT0$ 420
Capacitance	420 μF
Voltage (DC)	1400 V
I_{max}	90 A
Self Inductance	40 nH
No of units in parallel	24

Table 3.4: DC-Link Capacitor Details

The capacitors are sized to stabilize the voltage during the Double Pulse Test (DPT) duration. The capacitors offer low self inductance during operation due to large number of units connected in parallel. The information on ESL v/s frequency is not provided in the datasheet.

3.2 Setup Assembly

This section presents the complete Double Pulse Test (DPT) setup showing three paralleled Si-IGBT power modules and its measurement devices, load inductor and its connections along with the design tool output busbar integrated to the DPT bench in figure 3.6 below:

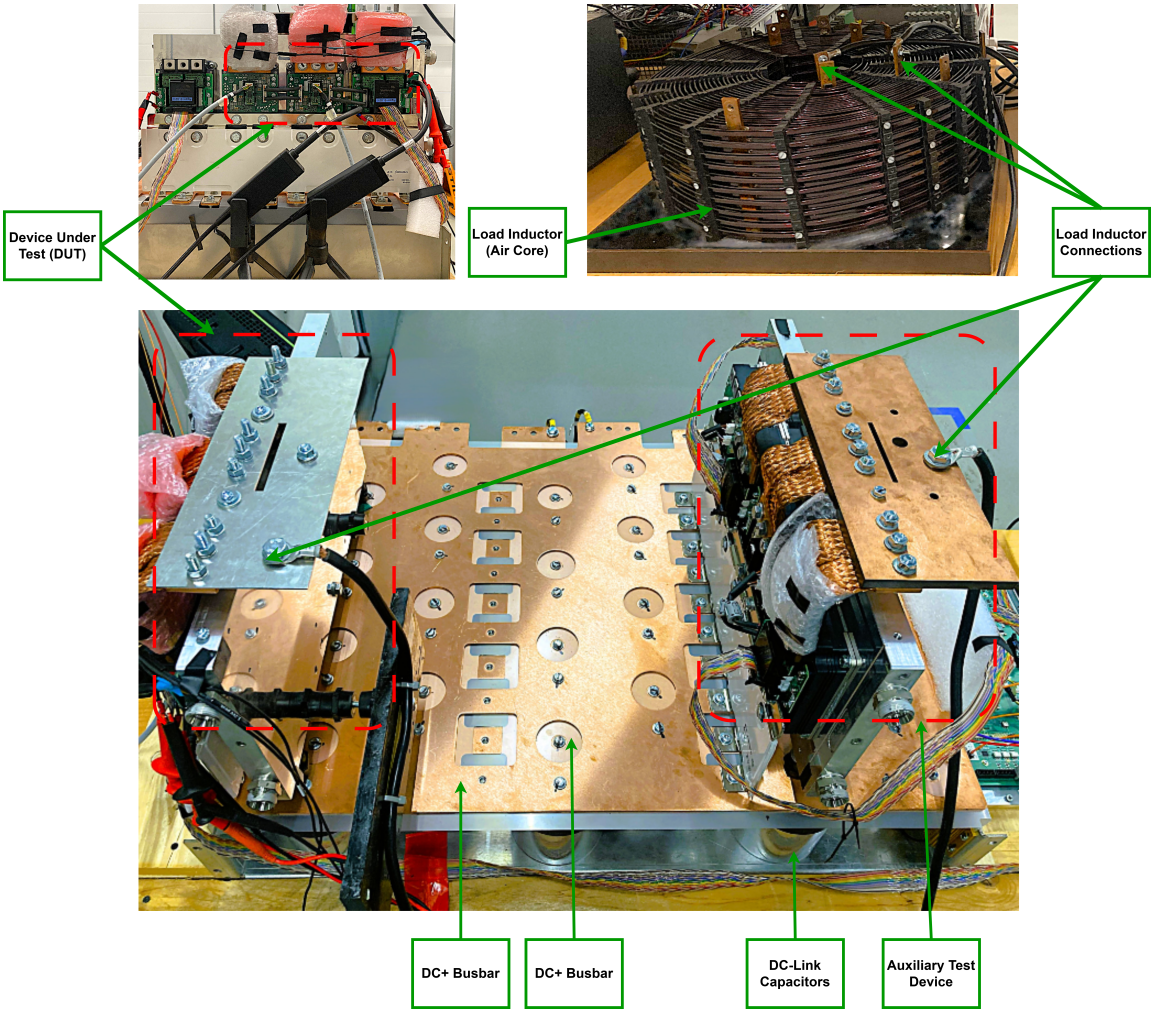


Figure 3.6: System Overview - Double Pulse Test (DPT) Setup

The Device Under Test (DUT) and the auxiliary test device both uses the same Si-IGBT power modules 3.1. The auxiliary test device connects the load inductor to the DC+/DC- terminals, depending on whether the high-side or low-side IGBT of the half-bridge module is being tested. One IGBT (top or bottom) is always turned on before the test to ensure a continuous current path.

This setup allows testing of both high-side and low-side devices using a single configuration. To handle the current requirements of DUTs with 2 to 4 paralleled devices, the auxiliary device includes four power modules in parallel for increased current capability. The algorithms solves for three power modules in parallel therefore, the DUT is setup accordingly.

Chapter 4 Testing and Validation

The chapter 4 presents the testing procedures for validating the design variants obtained from the optimization tool in the laboratory. This chapter navigates through the specifications, setting up, and verification of the test object and test bench for each variant that is tested at different points of the load connections through its sections.

4.1 Test Procedure

This section deals with defining the verification plan for the output of the optimization tool. Following are the procedures carried out:

1. **Test Conditions** - The Double Pulse Test (DPT) is setup to make each module carry a maximum of $1000A$ of current when equally sharing during the first pulse. Following are the test specifications for DPT.

Parameter	Value
Load Inductor	20.7 μH
Voltage Applied	1000 V
First Pulse Duration	60 μsec
Freewheeling Pulse Duration	30 μsec
Second Pulse Duration	10 μsec

Table 4.1: Test Specifications

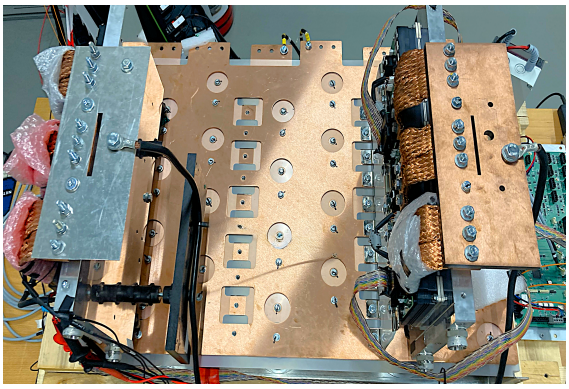
   For estimating the total currents during the first and the second pulses, current rise is calculated for using the inductor equation:

$$V = L_{\text{load}} \cdot \frac{di}{dt} \tag{4.1}$$

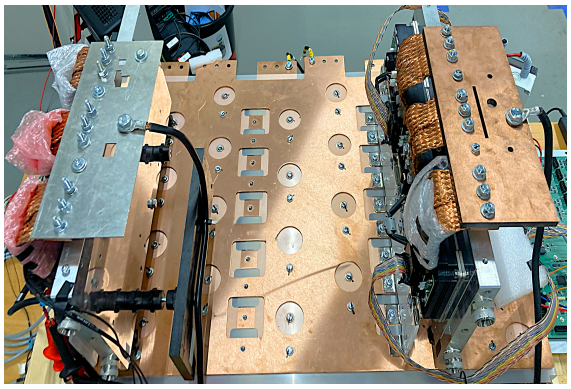
   Where, $V = 1000V$(same as measurement value), $L = 20.7\ \mu H$ (only main inductor taken into account) and dt is taken as $60\mu sec$ and considering the ramp up time for the first pulse and a second pulse of $10\mu sec$ for completing the test. The second pulse is kept relatively short to prevent a high increase in the currents. This gives out a total current of $I = 2898.55A$ for the first pulse duration and $I = 3381.64A$ after the second pulse.

2. **Test Plan** - To evaluate the impact of physical layout on system performance, the design tool produced three distinct layout variants. Testing these layout performances on the lab setup will reveal the optimization tool's - assumptions, limitations, and inaccuracies. This will provide a strong foundation for improving the model accuracy and implementing techniques to rectify the optimization algorithm for better results.

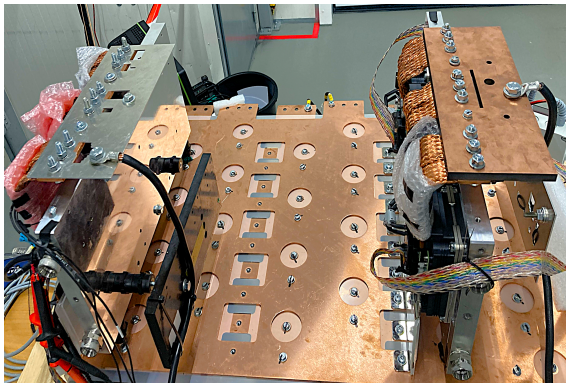
   To visualize the test configurations, images of the three design variants are shown in figure 4.1 below as integrated with the DPT setup. KK Wind solutions suggested including the impacts of the distance of the load cable from the DC link as derived from their independent experience. As the mutual coupling changes with the cable proximity, this dimension was also explored by the optimization tool for impedance matching.



(a) Mid-Point Connection Variant 1



(b) Mid-Point Connection Variant 2



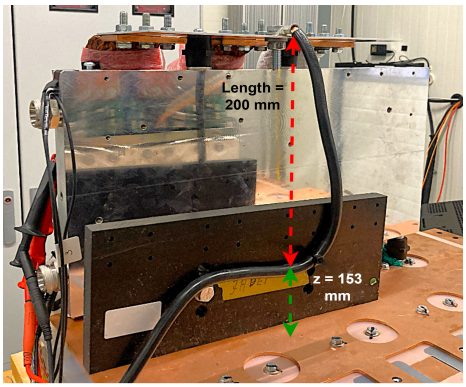
(c) End-Point Connection Variant 3

Figure 4.1: Test Setup - Load Connection Arrangement

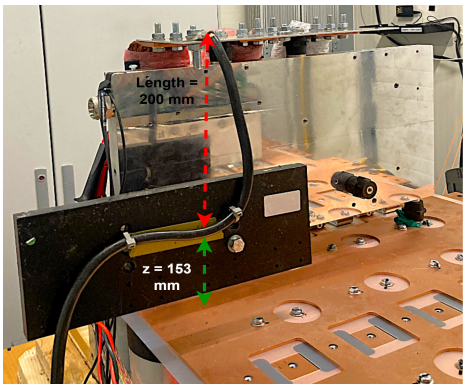
Although, Testing is initially intended to be carried out on only these variants, however, to ensure a thorough analysis, tests were conducted on all three variants under three different scenarios. These scenarios helps to isolate and highlight the effects of the changing variables. By testing each variant under all conditions, we were able to observe how layout arrangement and orientation influences the behavior of the system keeping certain variables constant. This was done to study the impact of two key variables:

(a) Load connection point, and

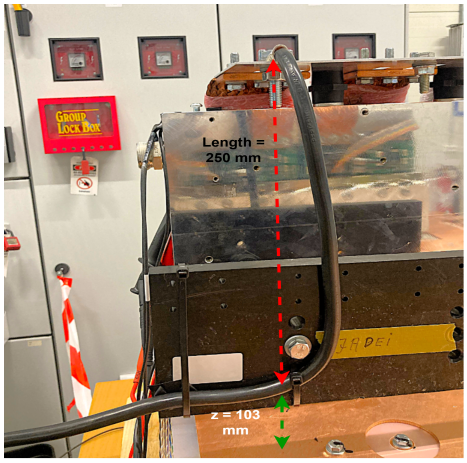
(b) Distance between the cable and the DC-Link busbar.



(a) Mid-Point Connection at z = 153mm



(b) End-Point Connection at z = 153mm



(c) End-Point Connection at z = 103mm

Figure 4.2: Test Setup - Load Cable Arrangement

Figure 4.2 shows the cable arrangement done for the test setup.

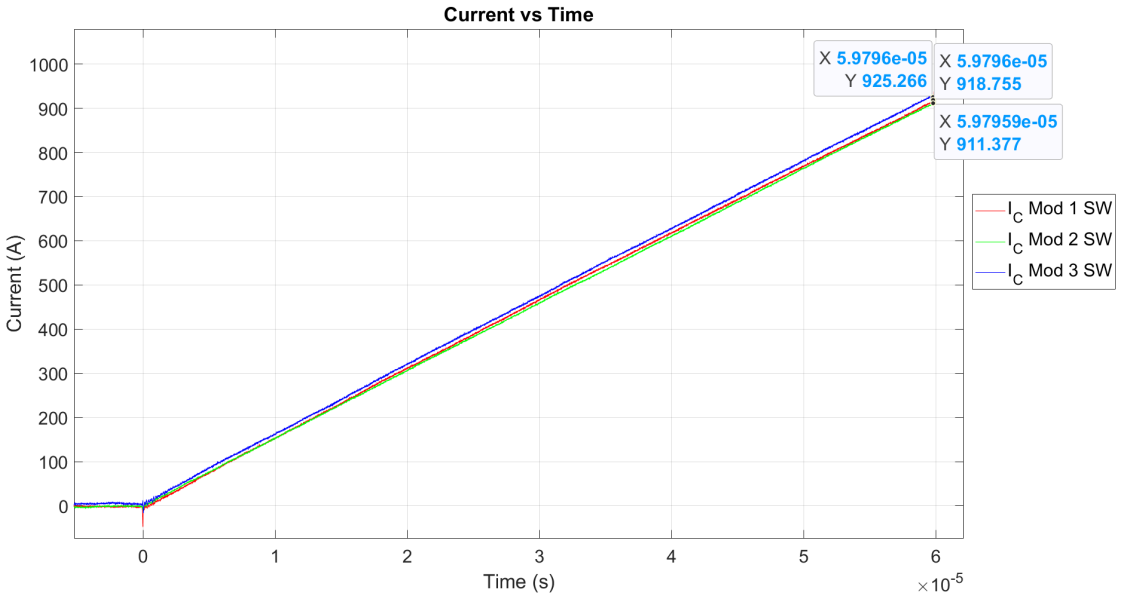
The test plan involves evaluating three busbar variants under two load connection configurations: mid-point and end-point connections. Each configuration is tested at distances of 153 mm and 103 mm from the DC-Link to observe the impact of load connection and distance from DC-link busbar.

4.2 Lab results

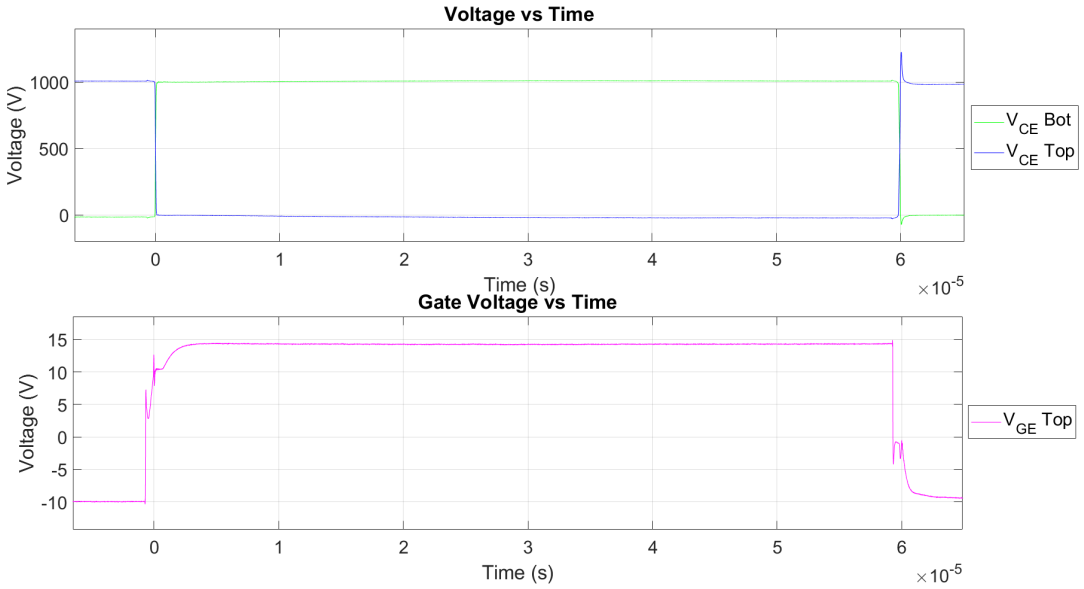
In this section, the results obtained from the lab testing are presented. Following the test procedure in the previous section, the tests are carried out on the DPT setup. Although the tests are performed on the all the variants for each load connection type, only the outputs of the optimization tool are shown in the figures below. For all the graphs please refer to the **Appendix D**

Referring to the system followed in section 2.3,

1. **Mid-point connection at z = 153 mm:** The impedance matrices corresponding to the mid-point connection of the load cable are applied. The design tool outputs variant 1 and variant 2 with different cutout but same point of load connection and distance from DC link.

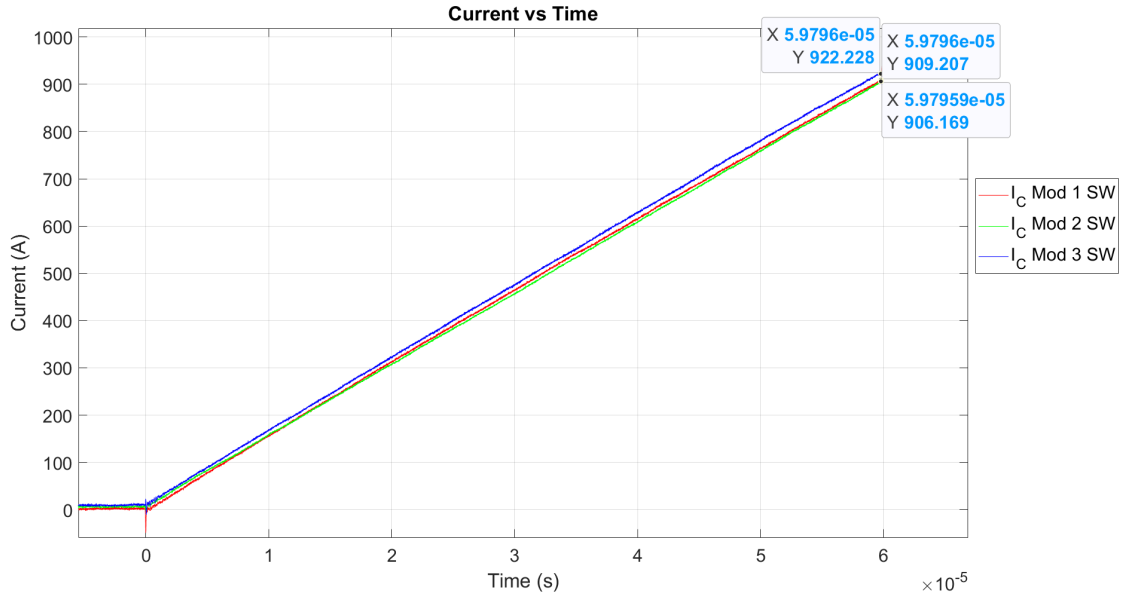


(a) Current Sharing - Variant 1

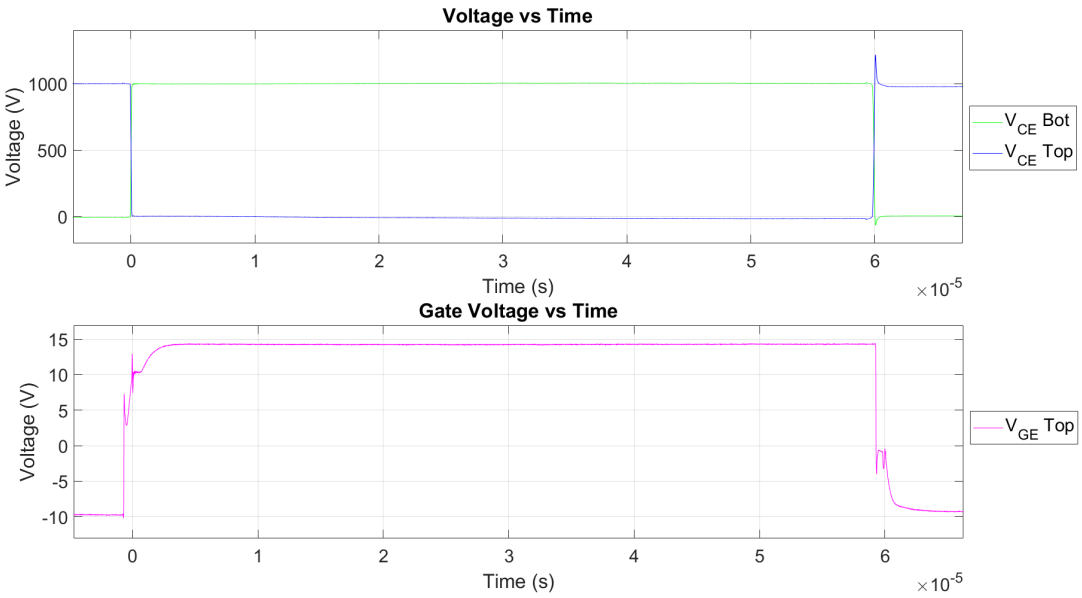


(b) Voltage Graphs - Variant 1

Figure 4.3: Mid-point connection - Variant 1



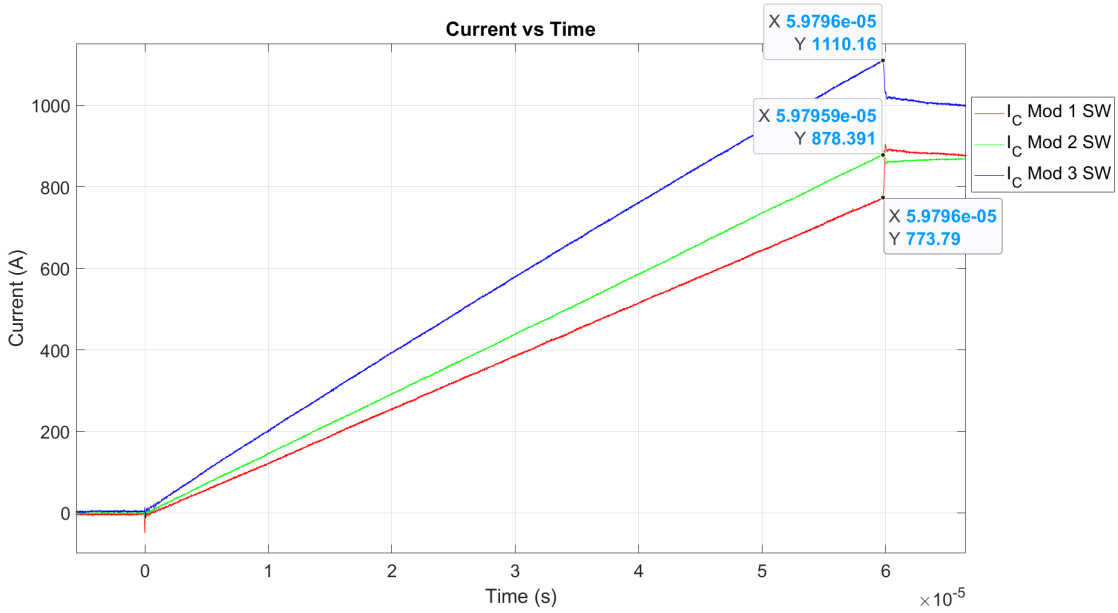
(a) Current Sharing - Variant 2



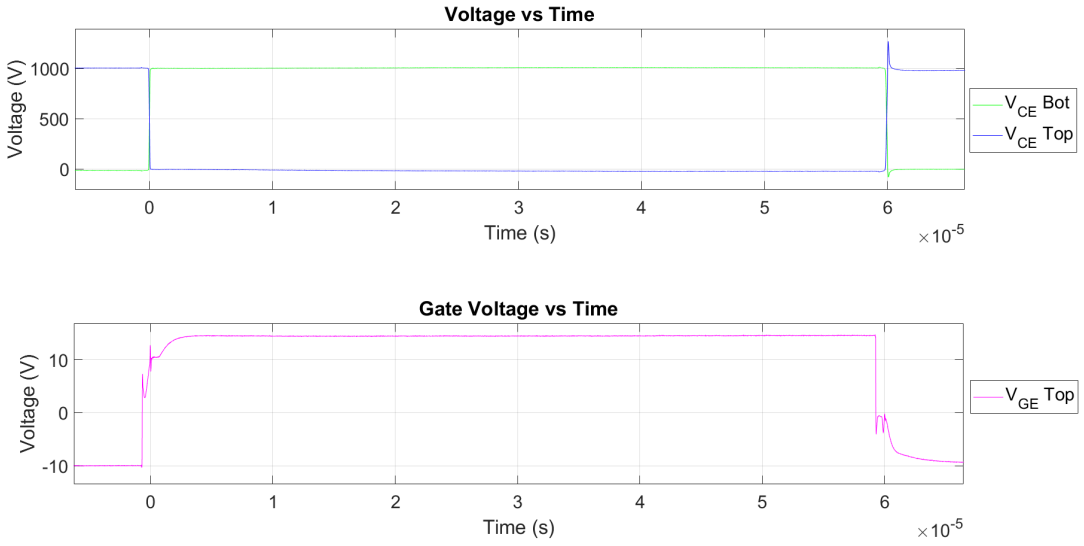
(b) Voltage Graphs - Variant 2

Figure 4.4: Mid-point connection - Variant 2

2. **End-point connection at z = 103 mm:** The measurement results for end-point connection of the load cable are applied. The design tool outputs variant 3 with multiple cutouts, different position of cable connection and distance from the DC-link busbar.



(a) Current Sharing - Variant 3



(b) Voltage Graphs - Variant 3

Figure 4.5: End-point connection - Variant 3

4.3 Design Tool Modifications

Lab results revealed significant inconsistencies between the measured outputs and the output calculated by the Analytical Model 2.3. As the lab setup was properly calibrated by carrying out tests on measurement equipments, and running DPT on standard copper busbar, before testing according to test procedure.

This discrepancy highlights a critical gap in the model's and design tool's accuracy and suggests the need for further refinement of the model or a reassessment of the design tool in case of oversights or inaccuracies in the tool development.

4.3.1 Observed Phenomenon and Corrective Methods

It was observed that the current sharing trend, i.e, if module 1 is taking highest current, and module 2 is taking lowest current seen in measurements, similarly, module 1 is taking highest current, and module 2 is taking lower current from the analytical model of DPT. It was consistent for all mid-point connections but for end point load connections this trend was not followed. This led to speculations on the correctness of the design tool output.

As there is a change in the ordinary process flow, it is possible that there are certain oversights during the modifications and reiteration of the scripts through MATLAB. Instead of generating the FreeCAD model, then exporting the Fast Henry script for processing and obtaining output matrix, MATLAB is being used to carryout the script modifications and eliminating the need for going into FreeCAD tool environment.

The logical way forward was to compare the scripts obtained through MATLAB process and FreeCAD model scripts to find the discrepancies in the codes and rectify the inaccuracies of the MATLAB process

Genetic Algorithm produces a genome containing the traits of the each solution, which in our case is the details on the cutouts, including, how many, which type, dimensions and positioning alongwith point of load connection and distance from the DC-link busbar. All this information is stored against each population member and is used by each generation produced either for cross-over, mutation etc. The tool displays the genome for the best combination for each variant alongwith the corresponding impedance matrix obtained and saves the **Best Cutout Combination** Fast Henry script which shall help in the debugging process.

Following are steps taken for problem identification:

- Using the information stored in the genome, the FreeCAD model was modified including positioning the cutouts and load connections, changing the aluminum busbar conductivity and segmentation etc.
- An input file was produced against each of the 9 combinations by exporting the Fast Henry script through FreeCAD.
- Taking the **Best Cutout Combination** input file generated using MATLAB, both the scripts were compared for debugging.

The observations and corrective methods implemented for the input file are listed below:

1. **Incorrect current conductivity and busbar thickness**:
   (a) **Observations** - While making changes in the model from copper switch-node busbar to aluminium busbar, the conductivity default conductivity was changed to 35000 S/mm corresponding to aluminium material. Also, the busbar thickness was set to 10mm thickness while the corresponding aluminium was 2mm thick.

(b) **Corrective Implementations** - As the rest of the system was developed with copper except the heatsinks and switch-node busbars, the default was set to 58000 S/mm for the copper busbars and only heatsinks and switch-node busbars are defined with aluminium characteristics. Due to this, the current density plots were seen different.

2. **Node modification inconsistent**

(a) **Observations** - Total of 6 nodes are modified for changing the load connection point as well as the distance from the DC link busbar, namely, $Noutput - busbar - interface$, $NFHNode443$ and $NFHNode444$ (responsible for load point connection), $NFHNode446$, $NFHNode447$ and $NFHNode450$ (responsible for distance from the DC link busbar). These are all critical for getting a correct result, however, the nodes $NFHNode447$ and $NFHNode443$ were not correctly updated due to wrong algebraic operations. This resulted in incorrect matrix creation due to incorrect orientation of load cables.

(b) **Corrective Implementations** - The nodes were matched with the results from FreeCAD and corrected manually for removing the inconsistencies in the results.

3. **Missing internal nodes**

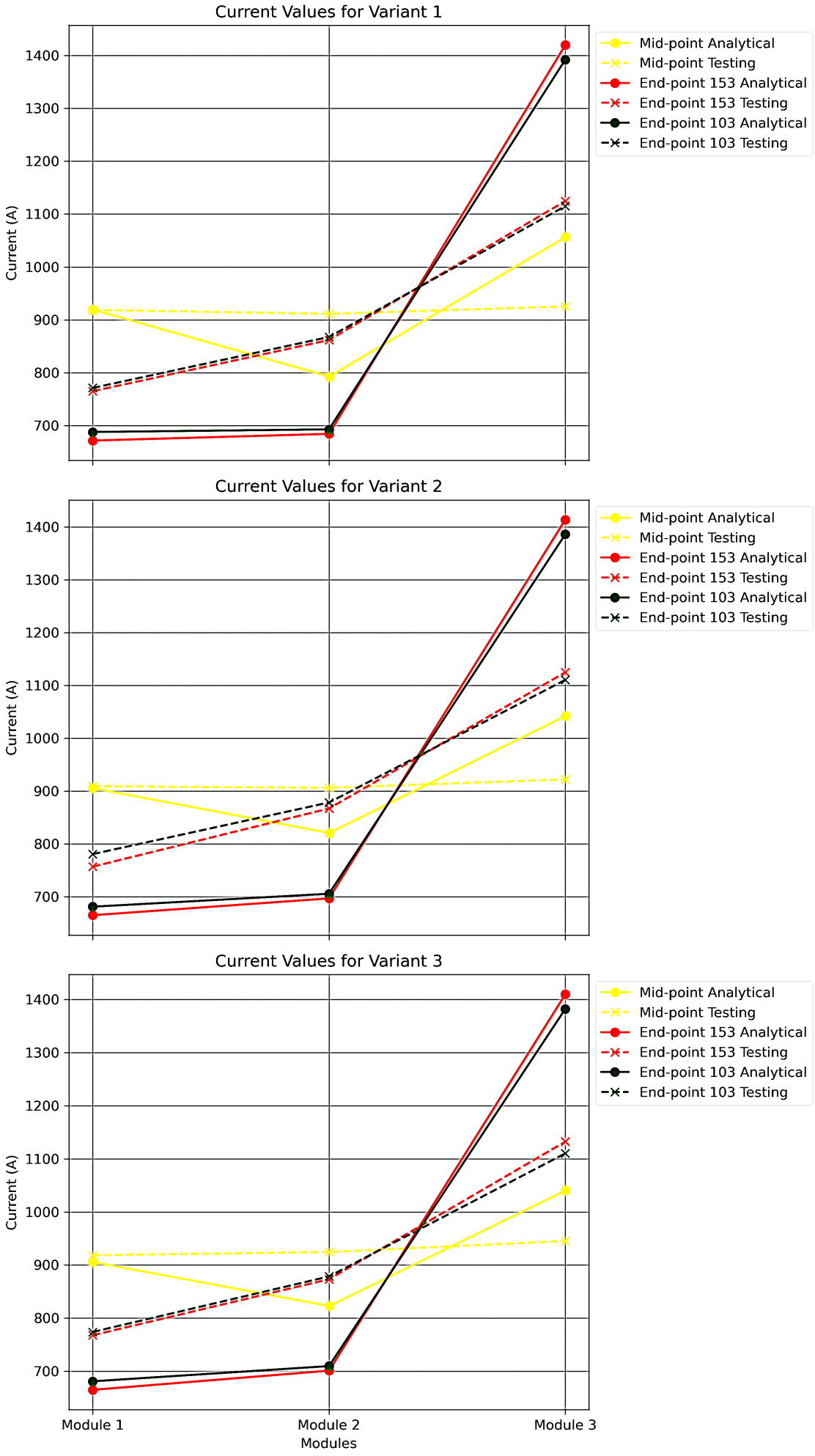
(a) **Observations** - Corresponding to the external user defined nodes mentioned in point 2, the FreeCAD generated script contained internal nodes shorted with the external nodes for current flow. These internal nodes are used by Fast Henry to interpret the connection of the current plane with either another conductive plane or another segment. In our case, the connection of switch-node busbar with load cable was wrongly interpreted by Fast Henry. As these nodes were not taken into consideration by the optimization tool, all the currents flows to the internal node placed at mid-point and then jumps to the external node placement position through virtual short.

(b) **Corrective Implementations** - With the progression of Genetic algorithm, the external nodes are updated to represent the end-point connection. This jump of current results in incorrect evaluations of the results by the optimization tool. Using manual updations to match the same positions as the FreeCAD output, the problem was rectified. **Results showed drastic changes in the output matrices**. These nodes have now been included in the optimization tool as well for future proofing.

After these corrective method implementations, the analytical model is run again to obtain the current values. The analytical model takes power module inductance and forward voltage drop for IGBT as equal for each device as they are from the same lot. The values for inductance and forward voltage drop are 12 nH and 2.25 V nominal values respectively. The results are compared at t = 60 μsec (end of first pulse). Following are the result comparison for the measurement output and analytical model shown in table 4.2:

Current Values and Deviations						
Mid-point connection at z = 153 mm	**Analytical Model Results**			**Testing Results**		
	Module 1	**Module 2**	**Module 3**	**Module 1**	**Module 2**	**Module 3**
Variant 1	919.3	792.7	1056.5	918.7	911.4	925.3
Variant 2	905.4	820.7	1042.6	909.2	906.2	922.2
Variant 3	905.5	822.7	1040.4	918.3	924.4	945.2
End-point connection at z = 153 mm	**Analytical Model Results**			**Testing Results**		
	Module 1	**Module 2**	**Module 3**	**Module 1**	**Module 2**	**Module 3**
Variant 1	671.8	684.5	1419.4	765.1	861.9	1124.5
Variant 2	665.0	696.9	1413.9	756.9	867.1	1124.9
Variant 3	664.8	701.0	1409.8	767.7	873.2	1132.3
End-point connection at z = 103 mm	**Analytical Model Results**			**Testing Results**		
	Module 1	**Module 2**	**Module 3**	**Module 1**	**Module 2**	**Module 3**
Variant 1	688.0	693.0	1391.8	771.2	867.54	1114.94
Variant 2	681.1	705.6	1386.2	780.7	878.4	1110.6
Variant 3	680.9	709.6	1382.3	773.8	878.4	1110.2

Table 4.2: Comparison - Analytical Model v/s Testing Results


Current Values for Variant 1
Current Values for Variant 2
Current Values for Variant 3
Current (A)
1400
1300
1200
1100
1000
900
800
700
Mid-point Analytical
Mid-point Testing
End-point 153 Analytical
End-point 153 Testing
End-point 103 Analytical
End-point 103 Testing
Module 1
Module 2
Module 3
Modules

4.3.2 Discussions and Remarks

There are a few observations that were understood from the table 4.2,

- **Same Current Tendencies** - It can be seen that the current tendencies for the Analytical Model and the Testing Results is always the same for all cases: Mid-Point, and both End-Point scenarios. Only exception found is the variant 3 of Mid-Point connection at z = 153 mm.

  This shows two things, the Fast Henry model and GA optimization tool have been able to successfully emulate the system behavior proving their credibility. Secondly, the spread of current or deviation in currents is higher than the measurement results, making a conservative approach, however, the accuracy of the FreeCAD model needs to be evaluated for improving the model's output.

- **Higher influence of Load Point Connections** - It is evident from top to bottom in table 4.2 that within the same load connection point—highlighted in yellow for the mid-point connection, and in red and grey for the end-point connections—the current distribution across the three power modules shows relatively minor variation for each variant. The same trend is observed for Power Modules 2 and 3.

  In contrast, the variation in current across different connection points for the same module and variant is significantly larger. This indicates that the location of the load connection has a more pronounced impact on current distribution than the introduction of cutouts. While cutouts serve as a means of fine-tuning the current sharing, the load connection point acts as a primary driver of distribution behavior.

Chapter 5 Results and Analysis

5.1 Post Validation Analysis

Based on the results obtained from section 4.3, it was observed that the current imbalance was more pronounced with the point of load connections and cutouts and distance from the DC-link busbar could be used for fine tuning. As the initial assumption was that the cutouts were sufficient enough for balancing the external layout connections while the point of load connections remains the same. It was necessary to understand the underlying cause behind this observation.

An analysis was carried out to visualize the current flow distribution by plotting the current density across the system for the three variants. This model is created to align with the observations from the previous section as well as develop better understanding of the current distribution.

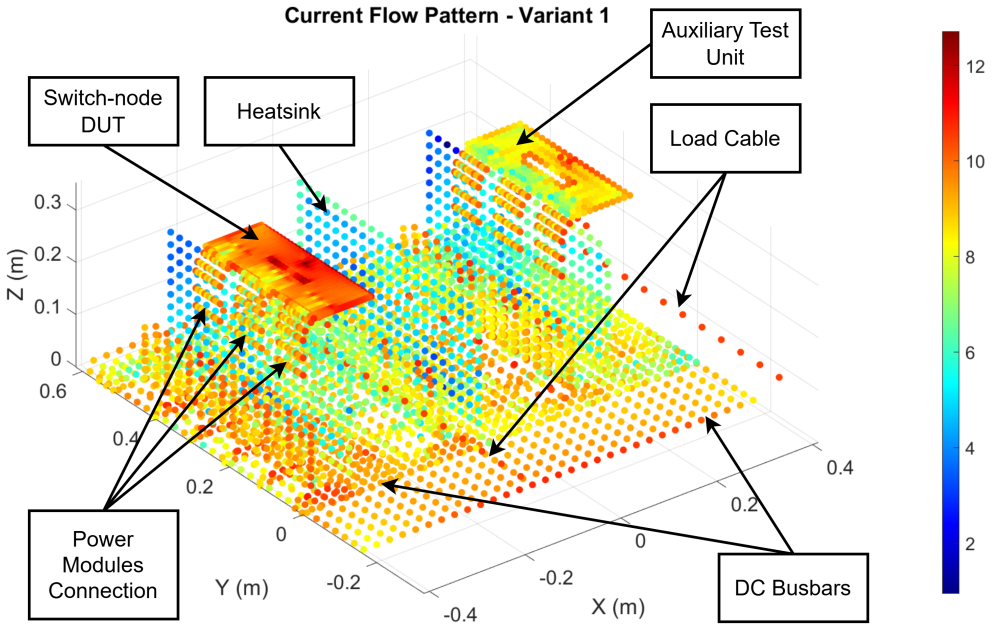


Figure 5.1: Logarithmic Current Distribution - Complete System 2.1

Figure 5.1 refers to the FreeCAD model presented in 2.1. The plot is identifies key components into the system for the reader's ease of visualization.

There are few general observations applicable to the complete system and are unaffected by the variant integrated in the system.

- **Difference in DUT and Auxiliary Test Unit currents** - It can be seen that the current density of the switch-node busbar at the auxiliary test unit is lower than the DUT switch-node busbar. This doesn't make logical sense. However, the distribution is inconsistent as the Fast Henry model considers only the currents on the surface of the busbars.

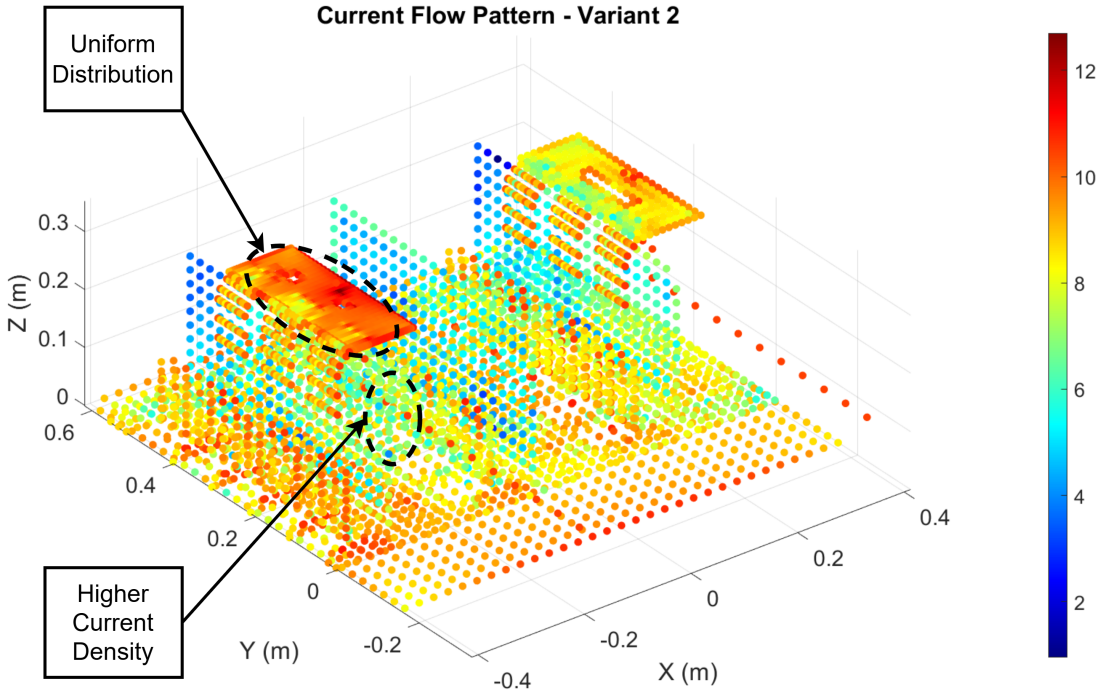
  Since the thickness of the busbars are different í.e, **DUT** - Aluminium busbar - Thickness - 2 mm and **Auxiliary Test Unit** - Copper Busbar - Thickness - 10 mm,

only the current observed on the surface is captured by the software. This can be confirmed by seeing the power module connection braided busbars, since these busbar are exactly same for both units, the current patterns are highly similar for both of them.

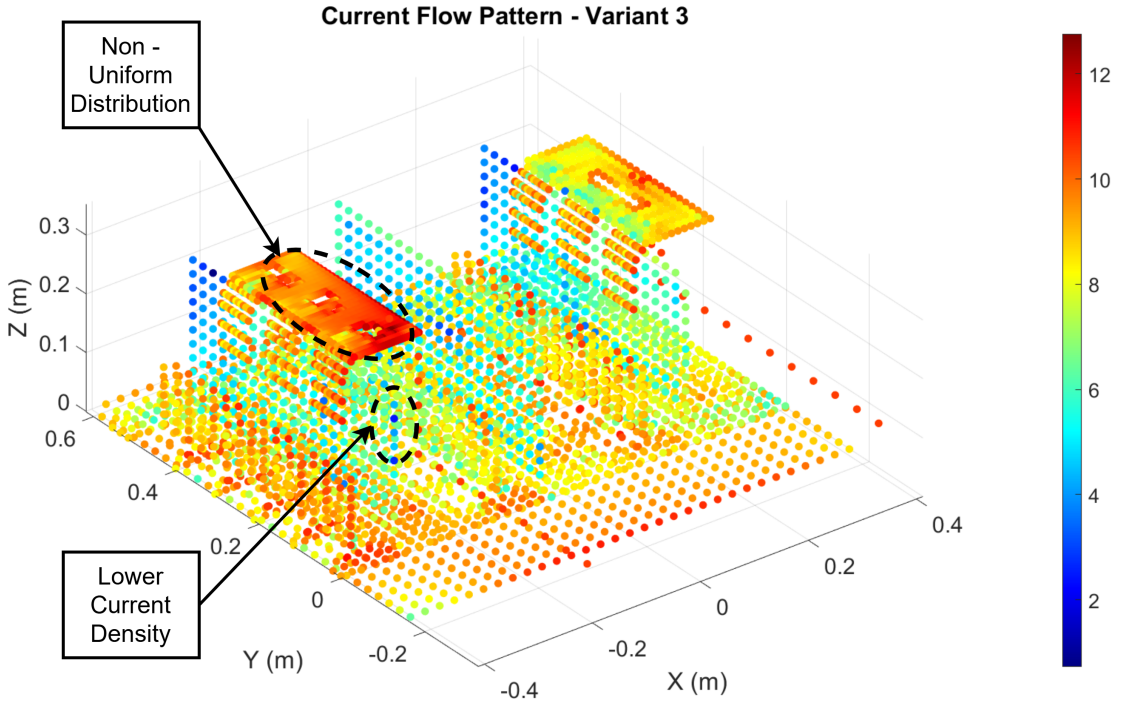
If the skin effect was correctly modeled the difference would have been relatively lowered for 10 kHz input signal. However, since the shape of the busbars are exactly matching, the current distribution is consistent in both the busbars.

- **Inclusion of Heat Sink** - Heat sinks were included in the model to see if circulating currents are developing due to the system current flow. It can be seen that with the proximity effect from the load cable, the currents in the heatsink show the introduction of eddy current in the body making the heatsink less affective on those regions.
- **Localised concentration of currents** - It can be seen that at the points of cutout, the current is more crowded suggesting loacalised hotspots development in the system. Upon further refining of the optimization tool as part of future works, current density parameter could be included to limit these crowdedness in the solution, including cutout shapes which lowers the current rise.

Figure 5.2, presents the similar current distribution for variant 2 and variant 3 respectively.



(a) Current Flow Pattern - Variant 2



(b) Current Flow Pattern - Variant 3

Figure 5.2: Current Distribution - Variant 2 and Variant 3

Refering the analytical model section 2.3, the three variants have different attributes adhering to the cutouts, point of load connections and distance of the cables from the DC link. Here are a few observations from the model which are specific to the model.

- **Current distribution** - For variant 1 and variant 2, since the load connection is done on the mid-point, it can be seen that the current patterns concentrate at the mid-point while the current is almost similar for all the modules as shown in figure 5.2a. While in the variant 3, since the load connection is done on the end-point, significantly high current is taken by the module 3 as shown in figure 5.2b. This confirms the observation from the table 4.2.
- **Effect of Load Cable** - With the proximity of load cable to the Module 3, in variants 1 and 2, the mutual coupling from the load cable makes the impedance higher in the module 3 equalising the curren shared by the modules. As opposed to the connection in variant 3 where the load cable's influence is quite low, the module 3 takes the highest load current. Even on the heatsink it can be observed that the eddy currents are lower (showing a dark blue pattern near module 3) 5.2b since the cable is more closer to the DC-link as compared to the other variants.

Although, this study in itself is not self-sufficing but it instigates detailed analysis of the flow patterns and their understanding. This shall enable refining the optimization tool further by taking considerations of the current density distributions, hotspot formations and influence of mutual couplings (both intensity vs distance and effect on current distribution patterns), skin and proximity effects.

Chapter 6 Conclusion and Future Work

This chapter summarizes the key findings and contributions of the project, reflecting on the objectives set at the outset and the extent to which they have been achieved. The chapter also discusses the limitations encountered during the project and proposes potential directions for future research and development.

6.1 Conclusion

The project is set out to answer the following problem statement:

"Is it possible to develop an algorithm aimed at modifying and reiterating the FastHenry script providing an automated approach to minimize the effects of layout while conforming to practical system limitations?"

This project builds on the premise of multi-physics software FastHenry to visualize the system impedance for the paralleled power modules. Building upon the development learnings from last semester [25], a comprehensive model is developed in the software to correctly emulate the testing enviroment digitally. The project investigates the automation potential of Fast Henry and implements commands to run the software remotely and obtain processed data for storage and further analysis.

From the review of state of art, it was concluded to move forward with Genetic Algorithm (GA) optimization as the approach has been proved effective with non-linear complex problems of similar kind both computationally inexpensive while maintaining high accuracy of the results. Approach to find the minima of current deviation by modifying the FastHenry script and continually comparing with other population members across the generations made the algorithm find formidable solution under the given constraints and variables.

To validate the model accuracy and the optimization tool's credibility, a Double Pulse Test (DPT) setup was used to test different complexity solutions output from the optimization tool. Finding the inaccuracies due to oversights in the optimization tool, manual adjustments were done to the obtained genome to correct the result. The model was found to be giving always the same tendencies as seen during measurements. This established strong correlation between the model and the test setup. Manual corrective approaches were also reflected in the Genetic Algorithm (GA) optimization tool for future developments. To bridge the gap between the actual measurements and simulations, model fidelity analysis could be carried out giving higher accuracy for more realistic models. However, there is always an difference between both the results due to not taking gate driver units, and taking limited parameters of power modules into consideration.

Overall, the project instigated a study of the parasitics for external layout of a system and provided an understanding of the impacts of components, their placement, proximity and orientation on the current sharing of paralleled power modules. With deeper analysis and further investigation, this approach can be made more adoptable to expedite design process improving layout solutions for balanced magnetics.

6.2 Future Works

While this thesis successfully demonstrates the integration of FastHenry with MATLAB for automated layout optimization and analysis, several promising directions remain to enhance the tool's capabilities.

Future work should focus on improving the accuracy of results, streamlining the user experience, and expanding the tool's applicability across a broader range of use cases, including higher and lower paralleled devices, inclusion and validation of wide-band gap power devices in this setting. Although the current version focuses on a specific objective with limited scope for modification, its potential as a scalable and customizable solution makes it a worthwhile investment.

Enhancing these features further—such as GUI development asking for user inputs and tuning the algorithm operation accordingly, integrating Python for full open-source compatibility, and refining the optimization techniques in the tool—could transform the tool into a comprehensive, one-stop solution for layout analysis and design by KK Wind Solutions.

Following are the possible directions of the project:

1. **Improving model accuracy** - Further investigations will focus on improving the effectiveness of the model. This approach will focus on identifying the high and low impact components in the system. Building upon the information from post validation analysis 5.1 and measurement results 4, a trade-off can be investigated which makes the components and variables with more influence be made closer to reality while the rest can be set to minimum resolution to balance the computational cost and get higher accuracy on the results obtained. The non-uniform busbar and meshing options can be utilized while modeling, to locally introduce higher fidelity within the solution space. This will ensure the time of algorithm to reach minima is not very high while significantly improving the accuracy of solutions.

2. **Electrical design considerations** - The solution provided still not fully considers the electrical parameters. The current density as a variable for optimizations, can be integrated into the design tool, based on the current density analysis done in chapter 5, this parameter can be fed back to limit the higher concentration of currents, include cutouts shapes that are more friendly to the current flow, avoid sharp edges, thereby lessening the hotspot formation during continuous conduction process. Also, with equally good or equally bad impedance paths, it is possible to ensure equal current sharing, however, the effects of voltage overshoots in the design due to high parasitics of the layout are individual and could lead to device damage. Considering the overshoots and other transient characteristics in the optimization tool is critical to the power module operation.

3. **GUI and user-interactive design tool** - The current version of the optimization tool has been developed without incorporating user input mechanisms, which limits its adaptability and ease of use. As it stands, some manual adjustments in the code are required when scaling the tool for different numbers of paralleled

modules—whether increasing or decreasing the count. To enhance the user experience and streamline the workflow, future development should focus on integrating user-defined inputs and building an interactive graphical user interface (GUI). Such a GUI would allow users to configure key parameters—such as the number of modules, layout constraints, and optimization goals—directly through an intuitive interface, reducing the need for manual intervention and making the tool more accessible and efficient for a broader range of users.

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Appendix A Fast Henry Model

In this chapter, the script for Fast Henry Evaluation and Modeling calculations are presented.

A.1 Fast Henry Evaluation Script

```
1  * FastHenry input file created using FreeCAD's ElectroMagnetic Workbench
2  * See http://www.freecad.org, http://www.fastfieldsolvers.com and ...
       ↪ http://epc-co.com
3
4  .units mm
5
6  .default sigma=58000.0 nhinc=1 nwinc=1 rh=1 rw=1
7
8  * Nodes
9  NSM1+_IGBTinterface x=-370.65 y=444.00000000000006 z=108.09999999999997
10 NSM1-_IGBTinterface x=-374.0 y=444.0 z=137.59999999999994
11 NSM1+_IGBTinterface001 x=-370.65 y=398.00000000000006 z=108.09999999999995
12 NSM1-_IGBTinterface001 x=-374.0 y=397.99999999999994 z=137.5999999999999
13 NSM1+_IGBTinterface002 x=-370.65 y=331.0 z=108.09999999999995
14 NSM1-_IGBTinterface002 x=-374.0 y=331.0 z=137.5999999999999
15 NSM1+_IGBTinterface003 x=-370.65000000000003 y=285.0 z=108.09999999999991
16 NSM1-_IGBTinterface003 x=-374.00000000000006 y=285.0 z=137.59999999999988
17 NSM1+_IGBTinterface004 x=-370.65000000000003 y=218.00000000000006 ...
       ↪ z=108.09999999999991
18 NSM1-_IGBTinterface004 x=-374.00000000000006 y=218.00000000000006 ...
       ↪ z=137.59999999999988
19 NSM1+_IGBTinterface005 x=-370.65000000000003 y=172.00000000000006 ...
       ↪ z=108.09999999999988
20 NSM1-_IGBTinterface005 x=-374.00000000000006 y=172.00000000000006 ...
       ↪ z=137.59999999999988
21 NSM1+_IGBTinterface006 x=-370.65000000000003 y=105.00000000000006 ...
       ↪ z=108.09999999999987
22 NSM1-_IGBTinterface006 x=-374.00000000000006 y=105.00000000000006 ...
       ↪ z=137.59999999999985
23 NSM1+_IGBTinterface007 x=-370.65000000000003 y=59.00000000000006 ...
       ↪ z=108.09999999999987
24 NSM1-_IGBTinterface007 x=-374.00000000000006 y=59.00000000000006 ...
       ↪ z=137.59999999999985
25 NSM1_DCinterface x=-375.50000000000006 y=35.50000000000006 ...
       ↪ z=30.499999999999876
26 NSM1_DCinterface001 x=-375.50000000000006 y=131.50000000000006 ...
       ↪ z=30.499999999999826
27 NSM1_DCinterface004 x=-375.5 y=227.50000000000003 z=30.499999999999854
28 NSM1_DCinterface003 x=-375.5 y=323.5 z=30.49999999999988
29 NSM1_DCinterface002 x=-375.5 y=419.5 z=30.499999999999908
30 NDCinterface009 x=-372.15000000000003 y=83.50000000000006 ...
       ↪ z=27.99999999999989
31 NDCinterface008 x=-372.15000000000003 y=179.50000000000006 ...
       ↪ z=27.99999999999992
32 NDCinterface007 x=-372.15 y=275.5 z=27.999999999999943
33 NDCinterface006 x=-372.15 y=371.5 z=27.99999999999997
34 NSM1interface001 x=-389.9999998461609 y=419.4999999920201 ...
       ↪ z=1.4999999972176954
35 NSM1interface002 x=-389.9999998815646 y=323.49999999202015 ...
       ↪ z=1.4999999978679035
```

```
NSM1interface003 x=-389.9999999169679 y=227.49999999202004 ...
    ↪ z=1.4999999985181116
NSM1interface004 x=-389.9999999523709 y=131.49999999202007 ...
    ↪ z=1.4999999991683195
NSM1interface x=-389.99999998777423 y=35.49999999202008 z=1.4999999998185278
NSM2interface x=-119.99999984616096 y=419.4999998924482 z=1.499999997754995
NSM2interface001 x=-119.99999988156463 y=323.4999998924482 ...
    ↪ z=1.4999999984052028
NSM2interface002 x=-119.99999991696797 y=227.49999989244813 ...
    ↪ z=1.4999999990554111
NSM2interface003 x=-119.99999995237096 y=131.49999989244813 ...
    ↪ z=1.499999999705619
NSM2interface004 x=-119.99999998777429 y=35.49999989244816 ...
    ↪ z=1.5000000003558271
NSM3interface x=150.0000000122256 y=35.49999979287624 z=1.5000000008931267
NSM3interface001 x=150.00000004762904 y=131.49999979287622 ...
    ↪ z=1.5000000002429186
NSM3interface002 x=150.00000008303215 y=227.4999997928762 ...
    ↪ z=1.4999999995927105
NSM3interface003 x=150.00000011843537 y=323.49999979287634 ...
    ↪ z=1.4999999989425024
NSM3interface004 x=150.00000015383904 y=419.4999997928763 ...
    ↪ z=1.4999999982922945
NDCcap x=-314.00028122022 y=419.99999996400936 z=1.4999999973655482
NDCcap001 x=-314.0002812681621 y=289.9999999640094 z=1.4999999982460384
NDCcap002 x=-201.4169787522141 y=354.99999992249036 z=1.4999999980298337
NDCcap003 x=-201.41697870427208 y=484.9999999224904 z=1.4999999971493438
NDCcap004 x=-201.41697880015616 y=224.99999992249042 z=1.4999999989103239
NDCcap005 x=-44.0002812681621 y=289.99999986443754 z=1.4999999987833377
NDCcap006 x=-44.000281220220074 y=419.9999998644374 z=1.4999999979028478
NDCcap007 x=68.58302129572792 y=484.9999998229185 z=1.4999999976866434
NDCcap008 x=225.9997187797798 y=419.99999976486555 z=1.4999999984401473
NDCcap009 x=338.58302129572786 y=484.9999997233466 z=1.4999999982239427
NDCcap010 x=68.58302124778584 y=354.9999998229184 z=1.4999999985671333
NDCcap011 x=338.5830212477858 y=354.99999972334655 z=1.4999999991044328
NDCcap012 x=225.99971873183773 y=289.9999997648656 z=1.4999999993206372
NDCcap013 x=68.58302119984381 y=224.99999982291848 z=1.4999999994476234
NDCcap014 x=338.5830211998438 y=224.99999972334658 z=1.4999999999849227
NDCcap015 x=225.99971868389565 y=159.99999976486546 z=1.5000000002011273
NDCcap016 x=338.58302115190173 y=94.99999972334656 z=1.5000000008654129
NDCcap017 x=225.99971863595368 y=29.999999764865482 z=1.5000000010816175
NDCcap018 x=68.58302115190179 y=94.99999982291848 z=1.5000000003281135
NDCcap019 x=-44.00028131610412 y=159.9999998644374 z=1.499999999663828
NDCcap020 x=-44.000281364046145 y=29.9999998644374 z=1.500000000544318
NDCcap021 x=-201.41697884809818 y=94.9999999224904 z=1.499999999790814
NDCcap022 x=-314.0002813161041 y=159.9999999640093 z=1.4999999991265285
NDCcap023 x=-313.9999594421053 y=29.999999964009202 z=1.500000000007019
NSM1interface005 x=-389.99999999999784 y=467.49999999999307 ...
    ↪ z=-1.0000000041749733
NSM1interface006 x=-389.9999999999979 y=371.4999999999932 ...
    ↪ z=-1.0000000035247654
NSM1interface007 x=-389.99999999999784 y=275.4999999999932 ...
    ↪ z=-1.000000002874557
NSM1interface008 x=-389.99999999999926 y=179.4999999999973 ...
    ↪ z=-1.0000000022243491
NSM1interface009 x=-389.9999999999993 y=83.49999999999739 ...
    ↪ z=-1.000000001574141
```

```
78  NSM2interface005 x=-119.99999999999915 y=467.49999999999727 ...
        ↪ z=-1.0000000036376737
79  NSM2interface006 x=-119.99999999999926 y=371.4999999999974 ...
        ↪ z=-1.0000000029874658
80  NSM2interface007 x=-119.99999999999801 y=275.49999999999307 ...
        ↪ z=-1.0000000023372577
81  NSM2interface008 x=-119.99999999999795 y=179.49999999999304 ...
        ↪ z=-1.0000000016870496
82  NSM2interface009 x=-119.99999999999801 y=83.4999999999931 ...
        ↪ z=-1.0000000010368417
83  NSM3interface005 x=150.0000000000021 y=83.49999999999304 ...
        ↪ z=-1.0000000004995422
84  NSM3interface006 x=150.000000000002 y=179.49999999999292 z=-1.00000000114975
85  NSM3interface007 x=150.000000000002 y=275.49999999999295 ...
        ↪ z=-1.0000000017999584
86  NSM3interface008 x=150.0000000000021 y=371.49999999999295 ...
        ↪ z=-1.0000000024501663
87  NSM3interface009 x=150.00000000000222 y=467.49999999999284 ...
        ↪ z=-1.0000000031003744
88  NDCcap024 x=-313.99999999999784 y=469.99999999999307 z=-1.000000004040666
89  NDCcap025 x=-201.41669750802086 y=534.9999999999934 z=-1.0000000042568704
90  NDCcap026 x=-43.99999999999778 y=469.99999999999295 z=-1.0000000035033665
91  NDCcap027 x=68.58330249197911 y=534.9999999999933 z=-1.0000000037195709
92  NDCcap028 x=226.000000000002 y=469.99999999999295 z=-1.000000002966067
93  NDCcap029 x=338.58330249197917 y=534.9999999999932 z=-1.0000000031822716
94  NDCcap030 x=-313.9999999999979 y=339.9999999999932 z=-1.000000003160176
95  NDCcap031 x=-201.41669750802095 y=404.9999999999933 z=-1.0000000033763805
96  NDCcap032 x=-43.9999999999979 y=339.99999999999307 z=-1.0000000026228766
97  NDCcap033 x=68.58330249197911 y=404.99999999999307 z=-1.000000002839081
98  NDCcap034 x=226.000000000002 y=339.99999999999295 z=-1.000000002085577
99  NDCcap035 x=338.58330249197894 y=404.99999999999295 z=-1.0000000023017814
100 NDCcap036 x=-313.99999999999795 y=209.99999999999315 z=-1.0000000022796858
101 NDCcap037 x=-201.41669750802095 y=274.9999999999932 z=-1.0000000024958902
102 NDCcap038 x=-43.99999999999801 y=209.99999999999304 z=-1.0000000017423862
103 NDCcap039 x=68.58330249197905 y=274.99999999999295 z=-1.0000000019585908
104 NDCcap040 x=226.00000000000188 y=209.99999999999292 z=-1.000000001205087
105 NDCcap041 x=338.58330249197894 y=274.99999999999295 z=-1.0000000014212915
106 NDCcap042 x=-313.999999999998 y=79.99999999999318 z=-1.0000000013991959
107 NDCcap043 x=-201.41669750802103 y=144.9999999999932 z=-1.0000000016154003
108 NDCcap044 x=-43.99999999999801 y=79.99999999999307 z=-1.0000000008618963
109 NDCcap045 x=68.58330249197905 y=144.9999999999931 z=-1.0000000010781007
110 NDCcap046 x=226.00000000000188 y=79.99999999999298 z=-1.0000000003245968
111 NDCcap047 x=338.58330249197905 y=144.99999999999304 z=-1.0000000005408012
112 NFHNode141 x=-120.0 y=83.5 z=1.5
113 NFHNode142 x=-120.0 y=35.50000000000009 z=4.0
114 NIGBTinterface016 x=-100.65000000000002 y=444.00000000000006 ...
        ↪ z=108.09999999999997
115 NIGBTinterface017 x=-104.00000000000001 y=444.0 z=137.59999999999994
116 NIGBTinterface018 x=-100.65000000000002 y=398.00000000000006 ...
        ↪ z=108.09999999999995
117 NIGBTinterface019 x=-104.00000000000001 y=397.99999999999994 ...
        ↪ z=137.5999999999999
118 NIGBTinterface020 x=-100.65000000000003 y=331.0 z=108.09999999999995
119 NIGBTinterface021 x=-104.00000000000003 y=331.0 z=137.5999999999999
120 NIGBTinterface022 x=-100.65000000000003 y=285.0 z=108.09999999999991
121 NIGBTinterface023 x=-104.00000000000003 y=285.0 z=137.59999999999988
122 NIGBTinterface024 x=-100.65000000000005 y=218.00000000000006 ...
        ↪ z=108.09999999999991
```

```
123 NIGBTinterface025 x=-104.00000000000004 y=218.00000000000006 ...
        ↪ z=137.59999999999988
124 NIGBTinterface026 x=-100.65000000000005 y=172.00000000000006 ...
        ↪ z=108.09999999999988
125 NIGBTinterface027 x=-104.00000000000004 y=172.00000000000006 ...
        ↪ z=137.59999999999988
126 NIGBTinterface028 x=-100.65000000000006 y=105.00000000000006 ...
        ↪ z=108.09999999999987
127 NIGBTinterface029 x=-104.00000000000006 y=105.00000000000006 ...
        ↪ z=137.59999999999985
128 NIGBTinterface030 x=-100.65000000000006 y=59.00000000000006 ...
        ↪ z=108.09999999999987
129 NIGBTinterface031 x=-104.00000000000006 y=59.00000000000006 ...
        ↪ z=137.59999999999985
130 NFHNode159 x=-105.5 y=35.50000000000009 z=4.0
131 NDCinterface010 x=-105.50000000000004 y=35.50000000000006 ...
        ↪ z=30.499999999999876
132 NFHNode161 x=-120.0 y=131.5 z=4.0
133 NFHNode162 x=-105.5 y=131.5 z=4.0
134 NDCinterface011 x=-105.50000000000004 y=131.50000000000006 ...
        ↪ z=30.499999999999826
135 NDCinterface012 x=-105.50000000000003 y=227.50000000000003 ...
        ↪ z=30.499999999999854
136 NDCinterface013 x=-105.50000000000001 y=323.5 z=30.49999999999988
137 NDCinterface014 x=-105.5 y=419.5 z=30.499999999999908
138 NFHNode167 x=-120.0 y=227.5 z=4.0
139 NFHNode168 x=-105.5 y=227.5 z=4.0
140 NFHNode169 x=-120.0 y=323.5 z=4.0
141 NFHNode170 x=-105.5 y=323.5 z=4.0
142 NFHNode171 x=-120.0 y=419.5 z=4.0
143 NFHNode172 x=-105.5 y=419.5 z=4.0
144 NFHNode173 x=-102.15 y=83.5 z=1.5
145 NDCinterface015 x=-102.15000000000005 y=83.50000000000006 ...
        ↪ z=27.99999999999989
146 NFHNode175 x=-120.0 y=179.5 z=1.5
147 NFHNode176 x=-102.15 y=179.5 z=1.5
148 NDCinterface016 x=-102.15000000000003 y=179.50000000000006 ...
        ↪ z=27.99999999999992
149 NFHNode178 x=-120.0 y=275.5 z=1.5
150 NFHNode179 x=-102.15 y=275.5 z=1.5
151 NDCinterface017 x=-102.15000000000003 y=275.5 z=27.999999999999943
152 NFHNode181 x=-120.0 y=371.5 z=1.5
153 NFHNode182 x=-102.15 y=371.5 z=1.5
154 NDCinterface018 x=-102.15000000000002 y=371.5 z=27.99999999999997
155 NFHNode184 x=-120.0 y=467.5 z=1.5
156 NFHNode185 x=-102.15 y=467.5 z=1.5
157 NDCinterface019 x=-102.15 y=467.5 z=27.999999999999996
158 NSM1_braidedBB1_ x=-315.9 y=341.0 z=330.1
159 NSM1_braidedBB1_091 x=-373.65 y=341.00000000000006 z=230.60000000000002
160 NSM1_braidedBB1_092 x=-373.65 y=341.0 z=297.1
161 NSM1_braidedBB1_093 x=-369.22883832488645 y=341.0 z=313.6
162 NSM1_braidedBB1_094 x=-357.15 y=341.0 z=325.6788383248865
163 NSM1_braidedBB1_095 x=-340.65 y=341.0 z=330.1
164 NSM1_braidedBB1_075 x=-315.9 y=335.0 z=330.1
165 NSM1_braidedBB1_070 x=-373.65 y=335.0 z=230.60000000000002
166 NSM1_braidedBB1_071 x=-373.65 y=335.0 z=297.1
167 NSM1_braidedBB1_072 x=-369.22883832488645 y=335.0 z=313.6
168 NSM1_braidedBB1_073 x=-357.15 y=335.0 z=325.6788383248865
```

```
169 NSM1_braidedBB1_074 x=-340.65 y=335.0 z=330.1
170 NSM1_braidedBB1_082 x=-315.9 y=329.0 z=330.1
171 NSM1_braidedBB1_077 x=-373.65 y=329.0 z=230.60000000000002
172 NSM1_braidedBB1_078 x=-373.65 y=329.0 z=297.1
173 NSM1_braidedBB1_079 x=-369.22883832488645 y=329.0 z=313.6
174 NSM1_braidedBB1_080 x=-357.15 y=329.0 z=325.6788383248865
175 NSM1_braidedBB1_081 x=-340.65 y=329.0 z=330.1
176 NSM1_braidedBB1_089 x=-315.9 y=323.0 z=330.1
177 NSM1_braidedBB1_084 x=-373.65 y=323.0 z=230.60000000000002
178 NSM1_braidedBB1_085 x=-373.65 y=323.0 z=297.1
179 NSM1_braidedBB1_086 x=-369.22883832488645 y=323.0 z=313.6
180 NSM1_braidedBB1_087 x=-357.15 y=323.0 z=325.6788383248865
181 NSM1_braidedBB1_088 x=-340.65 y=323.0 z=330.1
182 NSM1_braidedBB1_033 x=-315.9 y=317.0 z=330.1
183 NSM1_braidedBB1_028 x=-373.65 y=317.0 z=230.60000000000002
184 NSM1_braidedBB1_029 x=-373.65 y=317.0 z=297.1
185 NSM1_braidedBB1_030 x=-369.22883832488645 y=317.0 z=313.6
186 NSM1_braidedBB1_031 x=-357.15 y=317.0 z=325.6788383248865
187 NSM1_braidedBB1_032 x=-340.65 y=317.0 z=330.1
188 NSM1_braidedBB1_040 x=-315.9 y=311.0 z=330.1
189 NSM1_braidedBB1_035 x=-373.65 y=311.0 z=230.60000000000002
190 NSM1_braidedBB1_036 x=-373.65 y=311.0 z=297.1
191 NSM1_braidedBB1_037 x=-369.22883832488645 y=311.0 z=313.6
192 NSM1_braidedBB1_038 x=-357.15 y=311.0 z=325.6788383248865
193 NSM1_braidedBB1_039 x=-340.65 y=311.0 z=330.1
194 NSM1_braidedBB1_047 x=-315.9 y=305.0 z=330.1
195 NSM1_braidedBB1_042 x=-373.65 y=305.0 z=230.60000000000002
196 NSM1_braidedBB1_043 x=-373.65 y=305.0 z=297.1
197 NSM1_braidedBB1_044 x=-369.22883832488645 y=305.0 z=313.6
198 NSM1_braidedBB1_045 x=-357.15 y=305.0 z=325.6788383248865
199 NSM1_braidedBB1_046 x=-340.65 y=305.0 z=330.1
200 NSM1_braidedBB1_054 x=-315.9 y=299.0 z=330.1
201 NSM1_braidedBB1_049 x=-373.65 y=299.0 z=230.60000000000002
202 NSM1_braidedBB1_050 x=-373.65 y=299.0 z=297.1
203 NSM1_braidedBB1_051 x=-369.22883832488645 y=299.0 z=313.6
204 NSM1_braidedBB1_052 x=-357.15 y=299.0 z=325.6788383248865
205 NSM1_braidedBB1_053 x=-340.65 y=299.0 z=330.1
206 NSM1_braidedBB1_061 x=-315.9 y=293.0 z=330.1
207 NSM1_braidedBB1_056 x=-373.65 y=293.0 z=230.60000000000002
208 NSM1_braidedBB1_057 x=-373.65 y=293.0 z=297.1
209 NSM1_braidedBB1_058 x=-369.22883832488645 y=293.0 z=313.6
210 NSM1_braidedBB1_059 x=-357.15 y=293.0 z=325.6788383248865
211 NSM1_braidedBB1_060 x=-340.65 y=293.0 z=330.1
212 NSM1_braidedBB1_068 x=-315.9 y=287.0 z=330.1
213 NSM1_braidedBB1_063 x=-373.65 y=287.0 z=230.60000000000002
214 NSM1_braidedBB1_064 x=-373.65 y=287.0 z=297.1
215 NSM1_braidedBB1_065 x=-369.22883832488645 y=287.0 z=313.6
216 NSM1_braidedBB1_066 x=-357.15 y=287.0 z=325.6788383248865
217 NSM1_braidedBB1_067 x=-340.65 y=287.0 z=330.1
218 NSM1_braidedBB1_019 x=-315.9 y=281.0 z=330.1
219 NSM1_braidedBB1_014 x=-373.65 y=281.0 z=230.60000000000002
220 NSM1_braidedBB1_015 x=-373.65 y=281.0 z=297.1
221 NSM1_braidedBB1_016 x=-369.22883832488645 y=281.0 z=313.6
222 NSM1_braidedBB1_017 x=-357.15 y=281.0 z=325.6788383248865
223 NSM1_braidedBB1_018 x=-340.65 y=281.0 z=330.1
224 NSM1_braidedBB1_026 x=-315.9 y=275.0 z=330.1
225 NSM1_braidedBB1_021 x=-373.65 y=275.0 z=230.60000000000002
226 NSM1_braidedBB1_022 x=-373.65 y=275.0 z=297.1
```

```
227 NSM1_braidedBB1_023 x=-369.22883832488645 y=275.0 z=313.6
228 NSM1_braidedBB1_024 x=-357.15 y=275.0 z=325.6788383248865
229 NSM1_braidedBB1_025 x=-340.65 y=275.0 z=330.1
230 NSM1_braidedBB2_ x=-315.9 y=228.0 z=330.1
231 NSM1_braidedBB2_091 x=-373.65 y=227.99999999999997 z=230.60000000000002
232 NSM1_braidedBB2_092 x=-373.65 y=228.0 z=297.1
233 NSM1_braidedBB2_093 x=-369.22883832488645 y=228.0 z=313.6
234 NSM1_braidedBB2_094 x=-357.15 y=228.0 z=325.6788383248865
235 NSM1_braidedBB2_095 x=-340.65 y=228.0 z=330.1
236 NSM1_braidedBB2_075 x=-315.9 y=222.0 z=330.1
237 NSM1_braidedBB2_070 x=-373.65 y=221.99999999999997 z=230.60000000000002
238 NSM1_braidedBB2_071 x=-373.65 y=222.0 z=297.1
239 NSM1_braidedBB2_072 x=-369.22883832488645 y=222.0 z=313.6
240 NSM1_braidedBB2_073 x=-357.15 y=222.0 z=325.6788383248865
241 NSM1_braidedBB2_074 x=-340.65 y=222.0 z=330.1
242 NSM1_braidedBB2_082 x=-315.9 y=216.0 z=330.1
243 NSM1_braidedBB2_077 x=-373.65 y=215.99999999999997 z=230.60000000000002
244 NSM1_braidedBB2_078 x=-373.65 y=216.0 z=297.1
245 NSM1_braidedBB2_079 x=-369.22883832488645 y=216.0 z=313.6
246 NSM1_braidedBB2_080 x=-357.15 y=216.0 z=325.6788383248865
247 NSM1_braidedBB2_081 x=-340.65 y=216.0 z=330.1
248 NSM1_braidedBB2_089 x=-315.9 y=210.0 z=330.1
249 NSM1_braidedBB2_084 x=-373.65 y=209.99999999999997 z=230.60000000000002
250 NSM1_braidedBB2_085 x=-373.65 y=210.0 z=297.1
251 NSM1_braidedBB2_086 x=-369.22883832488645 y=210.0 z=313.6
252 NSM1_braidedBB2_087 x=-357.15 y=210.0 z=325.6788383248865
253 NSM1_braidedBB2_088 x=-340.65 y=210.0 z=330.1
254 NSM1_braidedBB2_033 x=-315.9 y=204.0 z=330.1
255 NSM1_braidedBB2_028 x=-373.65 y=203.99999999999997 z=230.60000000000002
256 NSM1_braidedBB2_029 x=-373.65 y=204.0 z=297.1
257 NSM1_braidedBB2_030 x=-369.22883832488645 y=204.0 z=313.6
258 NSM1_braidedBB2_031 x=-357.15 y=204.0 z=325.6788383248865
259 NSM1_braidedBB2_032 x=-340.65 y=204.0 z=330.1
260 NSM1_braidedBB2_040 x=-315.9 y=198.0 z=330.1
261 NSM1_braidedBB2_035 x=-373.65 y=197.99999999999997 z=230.60000000000002
262 NSM1_braidedBB2_036 x=-373.65 y=198.0 z=297.1
263 NSM1_braidedBB2_037 x=-369.22883832488645 y=198.0 z=313.6
264 NSM1_braidedBB2_038 x=-357.15 y=198.0 z=325.6788383248865
265 NSM1_braidedBB2_039 x=-340.65 y=198.0 z=330.1
266 NSM1_braidedBB2_047 x=-315.9 y=192.0 z=330.1
267 NSM1_braidedBB2_042 x=-373.65 y=191.99999999999997 z=230.60000000000002
268 NSM1_braidedBB2_043 x=-373.65 y=192.0 z=297.1
269 NSM1_braidedBB2_044 x=-369.22883832488645 y=192.0 z=313.6
270 NSM1_braidedBB2_045 x=-357.15 y=192.0 z=325.6788383248865
271 NSM1_braidedBB2_046 x=-340.65 y=192.0 z=330.1
272 NSM1_braidedBB2_054 x=-315.9 y=186.0 z=330.1
273 NSM1_braidedBB2_049 x=-373.65 y=185.99999999999997 z=230.60000000000002
274 NSM1_braidedBB2_050 x=-373.65 y=186.0 z=297.1
275 NSM1_braidedBB2_051 x=-369.22883832488645 y=186.0 z=313.6
276 NSM1_braidedBB2_052 x=-357.15 y=186.0 z=325.6788383248865
277 NSM1_braidedBB2_053 x=-340.65 y=186.0 z=330.1
278 NSM1_braidedBB2_061 x=-315.9 y=180.0 z=330.1
279 NSM1_braidedBB2_056 x=-373.65 y=179.99999999999997 z=230.60000000000002
280 NSM1_braidedBB2_057 x=-373.65 y=180.0 z=297.1
281 NSM1_braidedBB2_058 x=-369.22883832488645 y=180.0 z=313.6
282 NSM1_braidedBB2_059 x=-357.15 y=180.0 z=325.6788383248865
283 NSM1_braidedBB2_060 x=-340.65 y=180.0 z=330.1
284 NSM1_braidedBB2_068 x=-315.9 y=174.0 z=330.1
```

```
285 NSM1_braidedBB2_063 x=-373.65 y=173.99999999999997 z=230.60000000000002
286 NSM1_braidedBB2_064 x=-373.65 y=174.0 z=297.1
287 NSM1_braidedBB2_065 x=-369.22883832488645 y=174.0 z=313.6
288 NSM1_braidedBB2_066 x=-357.15 y=174.0 z=325.6788383248865
289 NSM1_braidedBB2_067 x=-340.65 y=174.0 z=330.1
290 NSM1_braidedBB2_019 x=-315.9 y=168.0 z=330.1
291 NSM1_braidedBB2_014 x=-373.65 y=167.99999999999997 z=230.60000000000002
292 NSM1_braidedBB2_015 x=-373.65 y=168.0 z=297.1
293 NSM1_braidedBB2_016 x=-369.22883832488645 y=168.0 z=313.6
294 NSM1_braidedBB2_017 x=-357.15 y=168.0 z=325.6788383248865
295 NSM1_braidedBB2_018 x=-340.65 y=168.0 z=330.1
296 NSM1_braidedBB2_026 x=-315.9 y=162.0 z=330.1
297 NSM1_braidedBB2_021 x=-373.65 y=161.99999999999997 z=230.60000000000002
298 NSM1_braidedBB2_022 x=-373.65 y=162.0 z=297.1
299 NSM1_braidedBB2_023 x=-369.22883832488645 y=162.0 z=313.6
300 NSM1_braidedBB2_024 x=-357.15 y=162.0 z=325.6788383248865
301 NSM1_braidedBB2_025 x=-340.65 y=162.0 z=330.1
302 NSM1_braidedBB3_095 x=-315.9 y=115.00000000000001 z=330.1
303 NSM1_braidedBB3_090 x=-373.65 y=114.99999999999999 z=230.60000000000002
304 NSM1_braidedBB3_091 x=-373.65 y=115.0 z=297.1
305 NSM1_braidedBB3_092 x=-369.22883832488645 y=115.0 z=313.6
306 NSM1_braidedBB3_093 x=-357.15 y=115.0 z=325.6788383248865
307 NSM1_braidedBB3_094 x=-340.65 y=115.00000000000001 z=330.1
308 NSM1_braidedBB3_074 x=-315.9 y=109.00000000000001 z=330.1
309 NSM1_braidedBB3_069 x=-373.65 y=108.99999999999999 z=230.60000000000002
310 NSM1_braidedBB3_070 x=-373.65 y=109.0 z=297.1
311 NSM1_braidedBB3_071 x=-369.22883832488645 y=109.0 z=313.6
312 NSM1_braidedBB3_072 x=-357.15 y=109.0 z=325.6788383248865
313 NSM1_braidedBB3_073 x=-340.65 y=109.00000000000001 z=330.1
314 NSM1_braidedBB3_081 x=-315.9 y=103.00000000000001 z=330.1
315 NSM1_braidedBB3_076 x=-373.65 y=102.99999999999999 z=230.60000000000002
316 NSM1_braidedBB3_077 x=-373.65 y=103.0 z=297.1
317 NSM1_braidedBB3_078 x=-369.22883832488645 y=103.0 z=313.6
318 NSM1_braidedBB3_079 x=-357.15 y=103.0 z=325.6788383248865
319 NSM1_braidedBB3_080 x=-340.65 y=103.00000000000001 z=330.1
320 NSM1_braidedBB3_088 x=-315.9 y=97.00000000000001 z=330.1
321 NSM1_braidedBB3_083 x=-373.65 y=96.99999999999999 z=230.60000000000002
322 NSM1_braidedBB3_084 x=-373.65 y=97.0 z=297.1
323 NSM1_braidedBB3_085 x=-369.22883832488645 y=97.0 z=313.6
324 NSM1_braidedBB3_086 x=-357.15 y=97.0 z=325.6788383248865
325 NSM1_braidedBB3_087 x=-340.65 y=97.00000000000001 z=330.1
326 NSM1_braidedBB3_032 x=-315.9 y=91.00000000000001 z=330.1
327 NSM1_braidedBB3_027 x=-373.65 y=90.99999999999999 z=230.60000000000002
328 NSM1_braidedBB3_028 x=-373.65 y=91.0 z=297.1
329 NSM1_braidedBB3_029 x=-369.22883832488645 y=91.0 z=313.6
330 NSM1_braidedBB3_030 x=-357.15 y=91.0 z=325.6788383248865
331 NSM1_braidedBB3_031 x=-340.65 y=91.00000000000001 z=330.1
332 NSM1_braidedBB3_039 x=-315.9 y=85.00000000000001 z=330.1
333 NSM1_braidedBB3_034 x=-373.65 y=84.99999999999999 z=230.60000000000002
334 NSM1_braidedBB3_035 x=-373.65 y=85.0 z=297.1
335 NSM1_braidedBB3_036 x=-369.22883832488645 y=85.0 z=313.6
336 NSM1_braidedBB3_037 x=-357.15 y=85.0 z=325.6788383248865
337 NSM1_braidedBB3_038 x=-340.65 y=85.00000000000001 z=330.1
338 NSM1_braidedBB3_046 x=-315.9 y=79.00000000000001 z=330.1
339 NSM1_braidedBB3_041 x=-373.65 y=78.99999999999999 z=230.60000000000002
340 NSM1_braidedBB3_042 x=-373.65 y=79.0 z=297.1
341 NSM1_braidedBB3_043 x=-369.22883832488645 y=79.0 z=313.6
342 NSM1_braidedBB3_044 x=-357.15 y=79.0 z=325.6788383248865
```

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343 NSM1_braidedBB3_045 x=-340.65 y=79.00000000000001 z=330.1
344 NSM1_braidedBB3_053 x=-315.9 y=73.00000000000001 z=330.1
345 NSM1_braidedBB3_048 x=-373.65 y=72.99999999999999 z=230.60000000000002
346 NSM1_braidedBB3_049 x=-373.65 y=73.0 z=297.1
347 NSM1_braidedBB3_050 x=-369.22883832488645 y=73.0 z=313.6
348 NSM1_braidedBB3_051 x=-357.15 y=73.0 z=325.6788383248865
349 NSM1_braidedBB3_052 x=-340.65 y=73.00000000000001 z=330.1
350 NSM1_braidedBB3_060 x=-315.9 y=67.00000000000001 z=330.1
351 NSM1_braidedBB3_055 x=-373.65 y=66.99999999999999 z=230.60000000000002
352 NSM1_braidedBB3_056 x=-373.65 y=67.0 z=297.1
353 NSM1_braidedBB3_057 x=-369.22883832488645 y=67.0 z=313.6
354 NSM1_braidedBB3_058 x=-357.15 y=67.0 z=325.6788383248865
355 NSM1_braidedBB3_059 x=-340.65 y=67.00000000000001 z=330.1
356 NSM1_braidedBB3_067 x=-315.9 y=61.00000000000001 z=330.1
357 NSM1_braidedBB3_062 x=-373.65 y=60.999999999999986 z=230.60000000000002
358 NSM1_braidedBB3_063 x=-373.65 y=61.0 z=297.1
359 NSM1_braidedBB3_064 x=-369.22883832488645 y=61.00000000000001 z=313.6
360 NSM1_braidedBB3_065 x=-357.15 y=61.00000000000001 z=325.6788383248865
361 NSM1_braidedBB3_066 x=-340.65 y=61.00000000000001 z=330.1
362 NSM1_braidedBB3_018 x=-315.9 y=55.00000000000001 z=330.1
363 NSM1_braidedBB3_013 x=-373.65 y=54.999999999999986 z=230.60000000000002
364 NSM1_braidedBB3_014 x=-373.65 y=55.0 z=297.1
365 NSM1_braidedBB3_015 x=-369.22883832488645 y=55.00000000000001 z=313.6
366 NSM1_braidedBB3_016 x=-357.15 y=55.00000000000001 z=325.6788383248865
367 NSM1_braidedBB3_017 x=-340.65 y=55.00000000000001 z=330.1
368 NSM1_braidedBB3_025 x=-315.9 y=49.00000000000001 z=330.1
369 NSM1_braidedBB3_020 x=-373.65 y=48.999999999999986 z=230.60000000000002
370 NSM1_braidedBB3_021 x=-373.65 y=49.0 z=297.1
371 NSM1_braidedBB3_022 x=-369.22883832488645 y=49.00000000000001 z=313.6
372 NSM1_braidedBB3_023 x=-357.15 y=49.00000000000001 z=325.6788383248865
373 NSM1_braidedBB3_024 x=-340.65 y=49.00000000000001 z=330.1
374 Nbraided_busbar_interface002 x=-315.89999997257235 y=331.9999999963371 ...
        ↪ z=334.0999999998092
375 Nbraided_busbar_interface006 x=-315.89999997487035 y=307.9999999963371 ...
        ↪ z=334.0999999998164
376 Nbraided_busbar_interface010 x=-315.8999999771684 y=283.9999999963372 ...
        ↪ z=334.0999999998236
377 Nbraided_busbar_interface014 x=-315.89999998339226 y=218.99999999633712 ...
        ↪ z=334.0999999998431
378 Nbraided_busbar_interface018 x=-315.89999998569033 y=194.99999999633712 ...
        ↪ z=334.0999999998503
379 Nbraided_busbar_interface022 x=-315.8999999879884 y=170.9999999963371 ...
        ↪ z=334.0999999998575
380 Nbraided_busbar_interface026 x=-315.8999999942123 y=105.99999999633707 ...
        ↪ z=334.099999999877
381 Nbraided_busbar_interface030 x=-315.8999999947518 y=81.99962084088011 ...
        ↪ z=334.0999999998842
382 Nbraided_busbar_interface034 x=-315.89999999880837 y=57.99999999633704 ...
        ↪ z=334.0999999998914
383 NFHNode443 x=-210.39999999999998 y=195.0 z=353.1
384 NFHNode444 x=-264.15 y=195.0 z=353.1
385 NFHNode446 x=-210.4 y=195.0 z=353.1
386 NFHNode447 x=-210.39999999999984 y=-329.99999999999994 z=153.09999999999985
387 Noutput_busbar_interface x=-264.1499999857096 y=194.99999999137978 ...
        ↪ z=334.0999999997084
388 NFHNode450 x=-210.39999999999995 y=194.99999999999994 z=153.09999999999997
389 NLoad_connection_SM1 x=-210.39999999999583 y=-130.00000000001438 ...
        ↪ z=-0.9999999997707019
```

```
390 NFHNode452 x=-372.15 y=467.5 z=28.0
391 NFHNode453 x=-372.15 y=467.5 z=1.5
392 NFHNode454 x=-390.0 y=467.5 z=1.5
393 NFHNode455 x=-372.15 y=467.5 z=1.5
394 NFHNode456 x=-372.15 y=371.5 z=28.0
395 NFHNode457 x=-372.15 y=371.5 z=1.5
396 NFHNode458 x=-390.0 y=371.5 z=1.5
397 NFHNode459 x=-372.15 y=371.5 z=1.5
398 NFHNode460 x=-372.15 y=275.5 z=28.0
399 NFHNode461 x=-372.15 y=275.5 z=1.5
400 NFHNode462 x=-390.0 y=275.5 z=1.5
401 NFHNode463 x=-372.15 y=275.5 z=1.5
402 NFHNode464 x=-372.15 y=179.5 z=28.0
403 NFHNode465 x=-372.15 y=179.5 z=1.5
404 NFHNode466 x=-390.0 y=179.5 z=1.5
405 NFHNode467 x=-372.15 y=179.5 z=1.5
406 NFHNode468 x=-372.15 y=83.5 z=28.0
407 NFHNode469 x=-372.15 y=83.5 z=1.5
408 NFHNode470 x=-390.0 y=83.5 z=1.5
409 NFHNode471 x=-372.15 y=83.5 z=1.5
410 NDCinterface005 x=-372.15 y=467.5 z=27.999999999999996
411 NFHNode472 x=-375.5 y=419.5 z=30.5
412 NFHNode473 x=-375.5 y=419.5 z=4.0
413 NFHNode474 x=-390.0 y=419.5 z=4.0
414 NFHNode475 x=-375.5 y=419.5 z=4.0
415 NFHNode476 x=-375.5 y=323.5 z=30.5
416 NFHNode477 x=-375.5 y=323.5 z=4.0
417 NFHNode478 x=-390.0 y=323.5 z=4.0
418 NFHNode479 x=-375.5 y=323.5 z=4.0
419 NFHNode480 x=-375.5 y=227.5 z=30.5
420 NFHNode481 x=-375.5 y=227.5 z=4.0
421 NFHNode482 x=-390.0 y=227.5 z=4.0
422 NFHNode483 x=-375.5 y=227.5 z=4.0
423 NFHNode484 x=-375.5 y=131.5 z=30.5
424 NFHNode485 x=-375.5 y=131.5 z=4.0
425 NFHNode486 x=-390.0 y=131.5 z=4.0
426 NFHNode487 x=-375.5 y=131.5 z=4.0
427 NFHNode488 x=-375.5 y=35.50000000000001 z=30.5
428 NFHNode489 x=-375.5 y=35.5 z=4.0
429 NFHNode490 x=-390.0 y=35.5 z=4.0
430 NFHNode491 x=-375.5 y=35.5 z=4.0
431 NSM3+_IGBTinterface x=169.35000000000002 y=444.00000000000006 ...
      ↪ z=108.09999999999997
432 NSM3-_IGBTinterface x=165.99999999999997 y=444.0 z=137.59999999999994
433 NSM3+_IGBTinterface001 x=169.35 y=398.00000000000006 z=108.09999999999995
434 NSM3-_IGBTinterface001 x=165.99999999999997 y=397.99999999999994 ...
      ↪ z=137.5999999999999
435 NSM3+_IGBTinterface002 x=169.35 y=331.0 z=108.09999999999995
436 NSM3-_IGBTinterface002 x=165.99999999999997 y=331.0 z=137.5999999999999
437 NSM3+_IGBTinterface003 x=169.35 y=285.0 z=108.09999999999991
438 NSM3-_IGBTinterface003 x=165.99999999999997 y=285.0 z=137.59999999999988
439 NSM3+_IGBTinterface004 x=169.35 y=218.00000000000006 z=108.09999999999991
440 NSM3-_IGBTinterface004 x=165.99999999999997 y=218.00000000000006 ...
      ↪ z=137.59999999999988
441 NSM3+_IGBTinterface005 x=169.34999999999997 y=172.00000000000006 ...
      ↪ z=108.09999999999988
442 NSM3-_IGBTinterface005 x=165.99999999999994 y=172.00000000000006 ...
      ↪ z=137.59999999999988
```

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443 NSM3+_IGBTinterface006 x=169.34999999999997 y=105.00000000000006 ...
        ↪ z=108.09999999999987
444 NSM3-_IGBTinterface006 x=165.99999999999994 y=105.00000000000006 ...
        ↪ z=137.59999999999985
445 NSM3+_IGBTinterface007 x=169.34999999999997 y=59.00000000000006 ...
        ↪ z=108.09999999999987
446 NSM3-_IGBTinterface007 x=165.99999999999994 y=59.00000000000006 ...
        ↪ z=137.59999999999985
447 NDCinterface020 x=164.49999999999994 y=35.50000000000006 ...
        ↪ z=30.499999999999876
448 NDCinterface021 x=164.49999999999997 y=131.50000000000006 ...
        ↪ z=30.499999999999826
449 NDCinterface022 x=164.49999999999997 y=227.50000000000003 ...
        ↪ z=30.499999999999854
450 NDCinterface023 x=164.49999999999997 y=323.5 z=30.49999999999988
451 NDCinterface024 x=164.5 y=419.5 z=30.499999999999908
452 NDCinterface025 x=167.84999999999997 y=83.50000000000006 z=27.99999999999989
453 NDCinterface026 x=167.85 y=179.50000000000006 z=27.99999999999992
454 NDCinterface027 x=167.85 y=275.5 z=27.999999999999943
455 NDCinterface028 x=167.85000000000002 y=371.5 z=27.99999999999997
456 NDCinterface029 x=167.85000000000002 y=467.5 z=27.999999999999996
457 NFHNode518 x=167.85000000000002 y=467.5 z=28.0
458 NFHNode519 x=167.85000000000002 y=467.5 z=1.5
459 NFHNode520 x=150.00000000000003 y=467.5 z=1.5
460 NFHNode521 x=167.85000000000002 y=467.5 z=1.5
461 NFHNode522 x=167.85000000000002 y=371.5 z=28.0
462 NFHNode523 x=167.85000000000002 y=371.5 z=1.5
463 NFHNode524 x=150.00000000000003 y=371.5 z=1.5
464 NFHNode525 x=167.85000000000002 y=371.5 z=1.5
465 NFHNode526 x=167.85000000000002 y=275.5 z=28.0
466 NFHNode527 x=167.85000000000002 y=275.5 z=1.5
467 NFHNode528 x=150.00000000000003 y=275.5 z=1.5
468 NFHNode529 x=167.85000000000002 y=275.5 z=1.5
469 NFHNode530 x=167.85000000000002 y=179.5 z=28.0
470 NFHNode531 x=167.85000000000002 y=179.5 z=1.5
471 NFHNode532 x=150.00000000000003 y=179.5 z=1.5
472 NFHNode533 x=167.85000000000002 y=179.5 z=1.5
473 NFHNode534 x=167.85000000000002 y=83.5 z=28.0
474 NFHNode535 x=167.85000000000002 y=83.5 z=1.5
475 NFHNode536 x=150.00000000000003 y=83.5 z=1.5
476 NFHNode537 x=167.85000000000002 y=83.5 z=1.5
477 NFHNode538 x=164.5 y=419.5 z=30.5
478 NFHNode539 x=164.5 y=419.5 z=4.0
479 NFHNode540 x=150.0 y=419.5 z=4.0
480 NFHNode541 x=164.5 y=419.5 z=4.0
481 NFHNode542 x=164.5 y=323.5 z=30.5
482 NFHNode543 x=164.5 y=323.5 z=4.0
483 NFHNode544 x=150.0 y=323.5 z=4.0
484 NFHNode545 x=164.5 y=323.5 z=4.0
485 NFHNode546 x=164.5 y=227.5 z=30.5
486 NFHNode547 x=164.5 y=227.5 z=4.0
487 NFHNode548 x=150.0 y=227.5 z=4.0
488 NFHNode549 x=164.5 y=227.5 z=4.0
489 NFHNode550 x=164.5 y=131.5 z=30.5
490 NFHNode551 x=164.5 y=131.5 z=4.0
491 NFHNode552 x=150.0 y=131.5 z=4.0
492 NFHNode553 x=164.5 y=131.5 z=4.0
493 NFHNode554 x=164.5 y=35.50000000000001 z=30.5
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494 NFHNode555 x=164.5 y=35.5 z=4.0
495 NFHNode556 x=150.0 y=35.5 z=4.0
496 NFHNode557 x=164.5 y=35.5 z=4.0
497 NSM3_braidedBB1_095 x=224.10000000000002 y=341.0 z=330.1
498 NSM3_braidedBB1_090 x=166.35000000000002 y=341.0 z=230.60000000000002
499 NSM3_braidedBB1_091 x=166.35000000000002 y=341.0 z=297.1
500 NSM3_braidedBB1_092 x=170.77116167511355 y=341.0 z=313.6
501 NSM3_braidedBB1_093 x=182.85000000000002 y=341.0 z=325.6788383248865
502 NSM3_braidedBB1_094 x=199.35000000000002 y=341.0 z=330.1
503 NSM3_braidedBB1_074 x=224.10000000000002 y=335.0 z=330.1
504 NSM3_braidedBB1_069 x=166.35000000000002 y=335.0 z=230.60000000000002
505 NSM3_braidedBB1_070 x=166.35000000000002 y=335.0 z=297.1
506 NSM3_braidedBB1_071 x=170.77116167511355 y=335.0 z=313.6
507 NSM3_braidedBB1_072 x=182.85000000000002 y=335.0 z=325.6788383248865
508 NSM3_braidedBB1_073 x=199.35000000000002 y=335.0 z=330.1
509 NSM3_braidedBB1_081 x=224.10000000000002 y=329.0 z=330.1
510 NSM3_braidedBB1_076 x=166.35000000000002 y=329.0 z=230.60000000000002
511 NSM3_braidedBB1_077 x=166.35000000000002 y=329.0 z=297.1
512 NSM3_braidedBB1_078 x=170.77116167511355 y=329.0 z=313.6
513 NSM3_braidedBB1_079 x=182.85000000000002 y=329.0 z=325.6788383248865
514 NSM3_braidedBB1_080 x=199.35000000000002 y=329.0 z=330.1
515 NSM3_braidedBB1_088 x=224.10000000000002 y=323.0 z=330.1
516 NSM3_braidedBB1_083 x=166.35000000000002 y=323.0 z=230.60000000000002
517 NSM3_braidedBB1_084 x=166.35000000000002 y=323.0 z=297.1
518 NSM3_braidedBB1_085 x=170.77116167511355 y=323.0 z=313.6
519 NSM3_braidedBB1_086 x=182.85000000000002 y=323.0 z=325.6788383248865
520 NSM3_braidedBB1_087 x=199.35000000000002 y=323.0 z=330.1
521 NSM3_braidedBB1_032 x=224.10000000000002 y=317.0 z=330.1
522 NSM3_braidedBB1_027 x=166.35000000000002 y=317.0 z=230.60000000000002
523 NSM3_braidedBB1_028 x=166.35000000000002 y=317.0 z=297.1
524 NSM3_braidedBB1_029 x=170.77116167511355 y=317.0 z=313.6
525 NSM3_braidedBB1_030 x=182.85000000000002 y=317.0 z=325.6788383248865
526 NSM3_braidedBB1_031 x=199.35000000000002 y=317.0 z=330.1
527 NSM3_braidedBB1_039 x=224.10000000000002 y=311.0 z=330.1
528 NSM3_braidedBB1_034 x=166.35000000000002 y=311.0 z=230.60000000000002
529 NSM3_braidedBB1_035 x=166.35000000000002 y=311.0 z=297.1
530 NSM3_braidedBB1_036 x=170.77116167511355 y=311.0 z=313.6
531 NSM3_braidedBB1_037 x=182.85000000000002 y=311.0 z=325.6788383248865
532 NSM3_braidedBB1_038 x=199.35000000000002 y=311.0 z=330.1
533 NSM3_braidedBB1_046 x=224.10000000000002 y=305.0 z=330.1
534 NSM3_braidedBB1_041 x=166.35000000000002 y=305.0 z=230.60000000000002
535 NSM3_braidedBB1_042 x=166.35000000000002 y=305.0 z=297.1
536 NSM3_braidedBB1_043 x=170.77116167511355 y=305.0 z=313.6
537 NSM3_braidedBB1_044 x=182.85000000000002 y=305.0 z=325.6788383248865
538 NSM3_braidedBB1_045 x=199.35000000000002 y=305.0 z=330.1
539 NSM3_braidedBB1_053 x=224.10000000000002 y=299.0 z=330.1
540 NSM3_braidedBB1_048 x=166.35000000000002 y=299.0 z=230.60000000000002
541 NSM3_braidedBB1_049 x=166.35000000000002 y=299.0 z=297.1
542 NSM3_braidedBB1_050 x=170.77116167511355 y=299.0 z=313.6
543 NSM3_braidedBB1_051 x=182.85000000000002 y=299.0 z=325.6788383248865
544 NSM3_braidedBB1_052 x=199.35000000000002 y=299.0 z=330.1
545 NSM3_braidedBB1_060 x=224.10000000000002 y=293.0 z=330.1
546 NSM3_braidedBB1_055 x=166.35000000000002 y=293.0 z=230.60000000000002
547 NSM3_braidedBB1_056 x=166.35000000000002 y=293.0 z=297.1
548 NSM3_braidedBB1_057 x=170.77116167511355 y=293.0 z=313.6
549 NSM3_braidedBB1_058 x=182.85000000000002 y=293.0 z=325.6788383248865
550 NSM3_braidedBB1_059 x=199.35000000000002 y=293.0 z=330.1
551 NSM3_braidedBB1_067 x=224.10000000000002 y=287.0 z=330.1
```

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552 NSM3_braidedBB1_062 x=166.35000000000002 y=287.0 z=230.60000000000002
553 NSM3_braidedBB1_063 x=166.35000000000002 y=287.0 z=297.1
554 NSM3_braidedBB1_064 x=170.77116167511355 y=287.0 z=313.6
555 NSM3_braidedBB1_065 x=182.85000000000002 y=287.0 z=325.6788383248865
556 NSM3_braidedBB1_066 x=199.35000000000002 y=287.0 z=330.1
557 NSM3_braidedBB1_018 x=224.10000000000002 y=281.0 z=330.1
558 NSM3_braidedBB1_013 x=166.35000000000002 y=281.0 z=230.60000000000002
559 NSM3_braidedBB1_014 x=166.35000000000002 y=281.0 z=297.1
560 NSM3_braidedBB1_015 x=170.77116167511355 y=281.0 z=313.6
561 NSM3_braidedBB1_016 x=182.85000000000002 y=281.0 z=325.6788383248865
562 NSM3_braidedBB1_017 x=199.35000000000002 y=281.0 z=330.1
563 NSM3_braidedBB1_025 x=224.10000000000002 y=275.0 z=330.1
564 NSM3_braidedBB1_020 x=166.35000000000002 y=275.0 z=230.60000000000002
565 NSM3_braidedBB1_021 x=166.35000000000002 y=275.0 z=297.1
566 NSM3_braidedBB1_022 x=170.77116167511355 y=275.0 z=313.6
567 NSM3_braidedBB1_023 x=182.85000000000002 y=275.0 z=325.6788383248865
568 NSM3_braidedBB1_024 x=199.35000000000002 y=275.0 z=330.1
569 NSM3_braidedBB2_095 x=224.10000000000002 y=228.0 z=330.1
570 NSM3_braidedBB2_090 x=166.35000000000002 y=227.99999999999997 ...
        ↪ z=230.60000000000002
571 NSM3_braidedBB2_091 x=166.35000000000002 y=228.0 z=297.1
572 NSM3_braidedBB2_092 x=170.77116167511355 y=228.0 z=313.6
573 NSM3_braidedBB2_093 x=182.85000000000002 y=228.0 z=325.6788383248865
574 NSM3_braidedBB2_094 x=199.35000000000002 y=228.0 z=330.1
575 NSM3_braidedBB2_074 x=224.10000000000002 y=222.0 z=330.1
576 NSM3_braidedBB2_069 x=166.35000000000002 y=221.99999999999997 ...
        ↪ z=230.60000000000002
577 NSM3_braidedBB2_070 x=166.35000000000002 y=222.0 z=297.1
578 NSM3_braidedBB2_071 x=170.77116167511355 y=222.0 z=313.6
579 NSM3_braidedBB2_072 x=182.85000000000002 y=222.0 z=325.6788383248865
580 NSM3_braidedBB2_073 x=199.35000000000002 y=222.0 z=330.1
581 NSM3_braidedBB2_081 x=224.10000000000002 y=216.0 z=330.1
582 NSM3_braidedBB2_076 x=166.35000000000002 y=215.99999999999997 ...
        ↪ z=230.60000000000002
583 NSM3_braidedBB2_077 x=166.35000000000002 y=216.0 z=297.1
584 NSM3_braidedBB2_078 x=170.77116167511355 y=216.0 z=313.6
585 NSM3_braidedBB2_079 x=182.85000000000002 y=216.0 z=325.6788383248865
586 NSM3_braidedBB2_080 x=199.35000000000002 y=216.0 z=330.1
587 NSM3_braidedBB2_088 x=224.10000000000002 y=210.0 z=330.1
588 NSM3_braidedBB2_083 x=166.35000000000002 y=209.99999999999997 ...
        ↪ z=230.60000000000002
589 NSM3_braidedBB2_084 x=166.35000000000002 y=210.0 z=297.1
590 NSM3_braidedBB2_085 x=170.77116167511355 y=210.0 z=313.6
591 NSM3_braidedBB2_086 x=182.85000000000002 y=210.0 z=325.6788383248865
592 NSM3_braidedBB2_087 x=199.35000000000002 y=210.0 z=330.1
593 NSM3_braidedBB2_032 x=224.10000000000002 y=204.0 z=330.1
594 NSM3_braidedBB2_027 x=166.35000000000002 y=203.99999999999997 ...
        ↪ z=230.60000000000002
595 NSM3_braidedBB2_028 x=166.35000000000002 y=204.0 z=297.1
596 NSM3_braidedBB2_029 x=170.77116167511355 y=204.0 z=313.6
597 NSM3_braidedBB2_030 x=182.85000000000002 y=204.0 z=325.6788383248865
598 NSM3_braidedBB2_031 x=199.35000000000002 y=204.0 z=330.1
599 NSM3_braidedBB2_039 x=224.10000000000002 y=198.0 z=330.1
600 NSM3_braidedBB2_034 x=166.35000000000002 y=197.99999999999997 ...
        ↪ z=230.60000000000002
601 NSM3_braidedBB2_035 x=166.35000000000002 y=198.0 z=297.1
602 NSM3_braidedBB2_036 x=170.77116167511355 y=198.0 z=313.6
603 NSM3_braidedBB2_037 x=182.85000000000002 y=198.0 z=325.6788383248865
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604 NSM3_braidedBB2_038 x=199.35000000000002 y=198.0 z=330.1
605 NSM3_braidedBB2_046 x=224.10000000000002 y=192.0 z=330.1
606 NSM3_braidedBB2_041 x=166.35000000000002 y=191.99999999999997 ...
        ↪ z=230.60000000000002
607 NSM3_braidedBB2_042 x=166.35000000000002 y=192.0 z=297.1
608 NSM3_braidedBB2_043 x=170.77116167511355 y=192.0 z=313.6
609 NSM3_braidedBB2_044 x=182.85000000000002 y=192.0 z=325.6788383248865
610 NSM3_braidedBB2_045 x=199.35000000000002 y=192.0 z=330.1
611 NSM3_braidedBB2_053 x=224.10000000000002 y=186.0 z=330.1
612 NSM3_braidedBB2_048 x=166.35000000000002 y=185.99999999999997 ...
        ↪ z=230.60000000000002
613 NSM3_braidedBB2_049 x=166.35000000000002 y=186.0 z=297.1
614 NSM3_braidedBB2_050 x=170.77116167511355 y=186.0 z=313.6
615 NSM3_braidedBB2_051 x=182.85000000000002 y=186.0 z=325.6788383248865
616 NSM3_braidedBB2_052 x=199.35000000000002 y=186.0 z=330.1
617 NSM3_braidedBB2_060 x=224.10000000000002 y=180.0 z=330.1
618 NSM3_braidedBB2_055 x=166.35000000000002 y=179.99999999999997 ...
        ↪ z=230.60000000000002
619 NSM3_braidedBB2_056 x=166.35000000000002 y=180.0 z=297.1
620 NSM3_braidedBB2_057 x=170.77116167511355 y=180.0 z=313.6
621 NSM3_braidedBB2_058 x=182.85000000000002 y=180.0 z=325.6788383248865
622 NSM3_braidedBB2_059 x=199.35000000000002 y=180.0 z=330.1
623 NSM3_braidedBB2_067 x=224.10000000000002 y=174.0 z=330.1
624 NSM3_braidedBB2_062 x=166.35000000000002 y=173.99999999999997 ...
        ↪ z=230.60000000000002
625 NSM3_braidedBB2_063 x=166.35000000000002 y=174.0 z=297.1
626 NSM3_braidedBB2_064 x=170.77116167511355 y=174.0 z=313.6
627 NSM3_braidedBB2_065 x=182.85000000000002 y=174.0 z=325.6788383248865
628 NSM3_braidedBB2_066 x=199.35000000000002 y=174.0 z=330.1
629 NSM3_braidedBB2_018 x=224.10000000000002 y=168.0 z=330.1
630 NSM3_braidedBB2_013 x=166.35000000000002 y=167.99999999999997 ...
        ↪ z=230.60000000000002
631 NSM3_braidedBB2_014 x=166.35000000000002 y=168.0 z=297.1
632 NSM3_braidedBB2_015 x=170.77116167511355 y=168.0 z=313.6
633 NSM3_braidedBB2_016 x=182.85000000000002 y=168.0 z=325.6788383248865
634 NSM3_braidedBB2_017 x=199.35000000000002 y=168.0 z=330.1
635 NSM3_braidedBB2_025 x=224.10000000000002 y=162.0 z=330.1
636 NSM3_braidedBB2_020 x=166.35000000000002 y=161.99999999999997 ...
        ↪ z=230.60000000000002
637 NSM3_braidedBB2_021 x=166.35000000000002 y=162.0 z=297.1
638 NSM3_braidedBB2_022 x=170.77116167511355 y=162.0 z=313.6
639 NSM3_braidedBB2_023 x=182.85000000000002 y=162.0 z=325.6788383248865
640 NSM3_braidedBB2_024 x=199.35000000000002 y=162.0 z=330.1
641 NSM3_braidedBB3_095 x=224.10000000000002 y=115.00000000000001 z=330.1
642 NSM3_braidedBB3_090 x=166.35000000000002 y=114.99999999999999 ...
        ↪ z=230.60000000000002
643 NSM3_braidedBB3_091 x=166.35000000000002 y=115.0 z=297.1
644 NSM3_braidedBB3_092 x=170.77116167511355 y=115.0 z=313.6
645 NSM3_braidedBB3_093 x=182.85000000000002 y=115.0 z=325.6788383248865
646 NSM3_braidedBB3_094 x=199.35000000000002 y=115.00000000000001 z=330.1
647 NSM3_braidedBB3_074 x=224.10000000000002 y=109.00000000000001 z=330.1
648 NSM3_braidedBB3_069 x=166.35000000000002 y=108.99999999999999 ...
        ↪ z=230.60000000000002
649 NSM3_braidedBB3_070 x=166.35000000000002 y=109.0 z=297.1
650 NSM3_braidedBB3_071 x=170.77116167511355 y=109.0 z=313.6
651 NSM3_braidedBB3_072 x=182.85000000000002 y=109.0 z=325.6788383248865
652 NSM3_braidedBB3_073 x=199.35000000000002 y=109.00000000000001 z=330.1
653 NSM3_braidedBB3_081 x=224.10000000000002 y=103.00000000000001 z=330.1
```

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654 NSM3_braidedBB3_076 x=166.35000000000002 y=102.99999999999999 ...
        ↪ z=230.60000000000002
655 NSM3_braidedBB3_077 x=166.35000000000002 y=103.0 z=297.1
656 NSM3_braidedBB3_078 x=170.77116167511355 y=103.0 z=313.6
657 NSM3_braidedBB3_079 x=182.85000000000002 y=103.0 z=325.6788383248865
658 NSM3_braidedBB3_080 x=199.35000000000002 y=103.00000000000001 z=330.1
659 NSM3_braidedBB3_088 x=224.10000000000002 y=97.00000000000001 z=330.1
660 NSM3_braidedBB3_083 x=166.35000000000002 y=96.99999999999999 ...
        ↪ z=230.60000000000002
661 NSM3_braidedBB3_084 x=166.35000000000002 y=97.0 z=297.1
662 NSM3_braidedBB3_085 x=170.77116167511355 y=97.0 z=313.6
663 NSM3_braidedBB3_086 x=182.85000000000002 y=97.0 z=325.6788383248865
664 NSM3_braidedBB3_087 x=199.35000000000002 y=97.00000000000001 z=330.1
665 NSM3_braidedBB3_032 x=224.10000000000002 y=91.00000000000001 z=330.1
666 NSM3_braidedBB3_027 x=166.35000000000002 y=90.99999999999999 ...
        ↪ z=230.60000000000002
667 NSM3_braidedBB3_028 x=166.35000000000002 y=91.0 z=297.1
668 NSM3_braidedBB3_029 x=170.77116167511355 y=91.0 z=313.6
669 NSM3_braidedBB3_030 x=182.85000000000002 y=91.0 z=325.6788383248865
670 NSM3_braidedBB3_031 x=199.35000000000002 y=91.00000000000001 z=330.1
671 NSM3_braidedBB3_039 x=224.10000000000002 y=85.00000000000001 z=330.1
672 NSM3_braidedBB3_034 x=166.35000000000002 y=84.99999999999999 ...
        ↪ z=230.60000000000002
673 NSM3_braidedBB3_035 x=166.35000000000002 y=85.0 z=297.1
674 NSM3_braidedBB3_036 x=170.77116167511355 y=85.0 z=313.6
675 NSM3_braidedBB3_037 x=182.85000000000002 y=85.0 z=325.6788383248865
676 NSM3_braidedBB3_038 x=199.35000000000002 y=85.00000000000001 z=330.1
677 NSM3_braidedBB3_046 x=224.10000000000002 y=79.00000000000001 z=330.1
678 NSM3_braidedBB3_041 x=166.35000000000002 y=78.99999999999999 ...
        ↪ z=230.60000000000002
679 NSM3_braidedBB3_042 x=166.35000000000002 y=79.0 z=297.1
680 NSM3_braidedBB3_043 x=170.77116167511355 y=79.0 z=313.6
681 NSM3_braidedBB3_044 x=182.85000000000002 y=79.0 z=325.6788383248865
682 NSM3_braidedBB3_045 x=199.35000000000002 y=79.00000000000001 z=330.1
683 NSM3_braidedBB3_053 x=224.10000000000002 y=73.00000000000001 z=330.1
684 NSM3_braidedBB3_048 x=166.35000000000002 y=72.99999999999999 ...
        ↪ z=230.60000000000002
685 NSM3_braidedBB3_049 x=166.35000000000002 y=73.0 z=297.1
686 NSM3_braidedBB3_050 x=170.77116167511355 y=73.0 z=313.6
687 NSM3_braidedBB3_051 x=182.85000000000002 y=73.0 z=325.6788383248865
688 NSM3_braidedBB3_052 x=199.35000000000002 y=73.00000000000001 z=330.1
689 NSM3_braidedBB3_060 x=224.10000000000002 y=67.00000000000001 z=330.1
690 NSM3_braidedBB3_055 x=166.35000000000002 y=66.99999999999999 ...
        ↪ z=230.60000000000002
691 NSM3_braidedBB3_056 x=166.35000000000002 y=67.0 z=297.1
692 NSM3_braidedBB3_057 x=170.77116167511355 y=67.0 z=313.6
693 NSM3_braidedBB3_058 x=182.85000000000002 y=67.0 z=325.6788383248865
694 NSM3_braidedBB3_059 x=199.35000000000002 y=67.00000000000001 z=330.1
695 NSM3_braidedBB3_067 x=224.10000000000002 y=61.00000000000001 z=330.1
696 NSM3_braidedBB3_062 x=166.35000000000002 y=60.999999999999986 ...
        ↪ z=230.60000000000002
697 NSM3_braidedBB3_063 x=166.35000000000002 y=61.0 z=297.1
698 NSM3_braidedBB3_064 x=170.77116167511355 y=61.00000000000001 z=313.6
699 NSM3_braidedBB3_065 x=182.85000000000002 y=61.00000000000001 ...
        ↪ z=325.6788383248865
700 NSM3_braidedBB3_066 x=199.35000000000002 y=61.00000000000001 z=330.1
701 NSM3_braidedBB3_018 x=224.10000000000002 y=55.00000000000001 z=330.1
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NSM3_braidedBB3_013 x=166.35000000000002 y=54.999999999999986 ...
    ↪ z=230.60000000000002
NSM3_braidedBB3_014 x=166.35000000000002 y=55.0 z=297.1
NSM3_braidedBB3_015 x=170.77116167511355 y=55.00000000000001 z=313.6
NSM3_braidedBB3_016 x=182.85000000000002 y=55.00000000000001 ...
    ↪ z=325.6788383248865
NSM3_braidedBB3_017 x=199.35000000000002 y=55.00000000000001 z=330.1
NSM3_braidedBB3_025 x=224.10000000000002 y=49.00000000000001 z=330.1
NSM3_braidedBB3_020 x=166.35000000000002 y=48.999999999999986 ...
    ↪ z=230.60000000000002
NSM3_braidedBB3_021 x=166.35000000000002 y=49.0 z=297.1
NSM3_braidedBB3_022 x=170.77116167511355 y=49.00000000000001 z=313.6
NSM3_braidedBB3_023 x=182.85000000000002 y=49.00000000000001 ...
    ↪ z=325.6788383248865
NSM3_braidedBB3_024 x=199.35000000000002 y=49.00000000000001 z=330.1
Nbraided_busbar_interface035 x=224.10000002743863 y=331.9999999963383 ...
    ↪ z=338.0999999998092
Nbraided_busbar_interface036 x=224.1000000251406 y=307.9999999963383 ...
    ↪ z=338.0999999998164
Nbraided_busbar_interface037 x=224.10000002284255 y=283.9999999963384 ...
    ↪ z=338.0999999998236
Nbraided_busbar_interface038 x=224.10000001661868 y=218.99999999633832 ...
    ↪ z=338.0999999998431
Nbraided_busbar_interface039 x=224.10000001432064 y=194.99999999633832 ...
    ↪ z=338.0999999998503
Nbraided_busbar_interface040 x=224.1000000120226 y=170.99999999633832 ...
    ↪ z=338.0999999998575
Nbraided_busbar_interface041 x=224.10000000579868 y=105.99999999633826 ...
    ↪ z=338.099999999877
Nbraided_busbar_interface042 x=224.1000000035007 y=81.99999999633826 ...
    ↪ z=338.0999999998842
Nbraided_busbar_interface043 x=224.1000000012026 y=57.999999996338225 ...
    ↪ z=338.0999999998914
NFHNode784 x=275.85 y=195.0 z=353.1
Noutput_busbar_interface001 x=275.8500000143014 y=194.99999999138097 ...
    ↪ z=338.0999999997084
Nload_connection_SM3 x=329.59999999999974 y=615.0000000000002 ...
    ↪ z=-1.0000000037419885
NDC_choke_connection x=344.600000000016 y=-100.00000000005463 ...
    ↪ z=-0.999999998869443
NAir_choke_connection1 x=-339.99999999999625 y=610.9999999999858 ...
    ↪ z=-1.000000005047399
Noutput_busbar_interface002 x=275.84939709091003 y=324.99986085084385 ...
    ↪ z=338.0999999996694
Noutput_busbar_interface003 x=275.8500000143014 y=194.99999999138103 ...
    ↪ z=338.0999999997084
NFHNode812 x=329.6 y=195.0 z=353.1
NFHNode813 x=275.85 y=195.0 z=353.1
NFHNode814 x=329.6 y=195.0 z=353.1
NFHNode815 x=329.6000000000001 y=-330.00000000000006 z=153.10000000000008
NFHNode816 x=329.6000000000001 y=194.99999999999994 z=153.09999999999997

* Segments
EDCport010 NFHNode142 NFHNode159 w=3.0 h=30.0 wx=0.0 wy=0.0 wz=1.0
EFHSegment021 NDCinterface010 NFHNode159 w=3.0 h=30.0
EDCport011 NFHNode161 NFHNode162 w=3.0 h=30.0 wx=0.0 wy=0.0 wz=1.0
EFHSegment023 NFHNode162 NDCinterface011 w=3.0 h=30.0
EDCport012 NFHNode167 NFHNode168 w=3.0 h=30.0 wx=0.0 wy=0.0 wz=1.0
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```
741 EDCport013 NFHNode169 NFHNode170 w=3.0 h=30.0 wx=0.0 wy=0.0 wz=1.0
742 EFHSegment026 NFHNode168 NDCinterface012 w=3.0 h=30.0
743 EFHSegment027 NFHNode170 NDCinterface013 w=3.0 h=30.0
744 EDCport014 NFHNode171 NFHNode172 w=3.0 h=30.0 wx=0.0 wy=0.0 wz=1.0
745 EFHSegment029 NFHNode172 NDCinterface014 w=3.0 h=30.0
746 EDCport015 NFHNode173 NFHNode141 w=3.0 h=30.0 wx=0.0 wy=0.0 wz=1.0
747 EFHSegment031 NDCinterface015 NFHNode173 w=3.0 h=30.0
748 EDCport016 NFHNode176 NFHNode175 w=3.0 h=30.0 wx=0.0 wy=0.0 wz=1.0
749 EFHSegment033 NDCinterface016 NFHNode176 w=3.0 h=30.0
750 EDCport017 NFHNode179 NFHNode178 w=3.0 h=30.0 wx=0.0 wy=0.0 wz=1.0
751 EFHSegment035 NDCinterface017 NFHNode179 w=3.0 h=30.0
752 EDCport018 NFHNode182 NFHNode181 w=3.0 h=30.0 wx=0.0 wy=0.0 wz=1.0
753 EFHSegment037 NDCinterface018 NFHNode182 w=3.0 h=30.0
754 EDCport019 NFHNode185 NFHNode184 w=3.0 h=30.0 wx=0.0 wy=0.0 wz=1.0
755 EFHSegment039 NDCinterface019 NFHNode185 w=3.0 h=30.0
756
757 * Segments from paths
758 ESM1_braidedBB1_0120 NSM1_braidedBB1_091 NSM1_braidedBB1_092 w=6.0 h=6.0
759 ESM1_braidedBB1_0121 NSM1_braidedBB1_092 NSM1_braidedBB1_093 w=6.0 h=6.0
760 ESM1_braidedBB1_0122 NSM1_braidedBB1_093 NSM1_braidedBB1_094 w=6.0 h=6.0
761 ESM1_braidedBB1_0123 NSM1_braidedBB1_094 NSM1_braidedBB1_095 w=6.0 h=6.0
762 ESM1_braidedBB1_0124 NSM1_braidedBB1_095 NSM1_braidedBB1_ w=6.0 h=6.0
763 ESM1_braidedBB1_0090 NSM1_braidedBB1_070 NSM1_braidedBB1_071 w=6.0 h=6.0
764 ESM1_braidedBB1_0091 NSM1_braidedBB1_071 NSM1_braidedBB1_072 w=6.0 h=6.0
765 ESM1_braidedBB1_0092 NSM1_braidedBB1_072 NSM1_braidedBB1_073 w=6.0 h=6.0
766 ESM1_braidedBB1_0093 NSM1_braidedBB1_073 NSM1_braidedBB1_074 w=6.0 h=6.0
767 ESM1_braidedBB1_0094 NSM1_braidedBB1_074 NSM1_braidedBB1_075 w=6.0 h=6.0
768 ESM1_braidedBB1_0100 NSM1_braidedBB1_077 NSM1_braidedBB1_078 w=6.0 h=6.0
769 ESM1_braidedBB1_0101 NSM1_braidedBB1_078 NSM1_braidedBB1_079 w=6.0 h=6.0
770 ESM1_braidedBB1_0102 NSM1_braidedBB1_079 NSM1_braidedBB1_080 w=6.0 h=6.0
771 ESM1_braidedBB1_0103 NSM1_braidedBB1_080 NSM1_braidedBB1_081 w=6.0 h=6.0
772 ESM1_braidedBB1_0104 NSM1_braidedBB1_081 NSM1_braidedBB1_082 w=6.0 h=6.0
773 ESM1_braidedBB1_0110 NSM1_braidedBB1_084 NSM1_braidedBB1_085 w=6.0 h=6.0
774 ESM1_braidedBB1_0111 NSM1_braidedBB1_085 NSM1_braidedBB1_086 w=6.0 h=6.0
775 ESM1_braidedBB1_0112 NSM1_braidedBB1_086 NSM1_braidedBB1_087 w=6.0 h=6.0
776 ESM1_braidedBB1_0113 NSM1_braidedBB1_087 NSM1_braidedBB1_088 w=6.0 h=6.0
777 ESM1_braidedBB1_0114 NSM1_braidedBB1_088 NSM1_braidedBB1_089 w=6.0 h=6.0
778 ESM1_braidedBB1_0030 NSM1_braidedBB1_028 NSM1_braidedBB1_029 w=6.0 h=6.0
779 ESM1_braidedBB1_0031 NSM1_braidedBB1_029 NSM1_braidedBB1_030 w=6.0 h=6.0
780 ESM1_braidedBB1_0032 NSM1_braidedBB1_030 NSM1_braidedBB1_031 w=6.0 h=6.0
781 ESM1_braidedBB1_0033 NSM1_braidedBB1_031 NSM1_braidedBB1_032 w=6.0 h=6.0
782 ESM1_braidedBB1_0034 NSM1_braidedBB1_032 NSM1_braidedBB1_033 w=6.0 h=6.0
783 ESM1_braidedBB1_0040 NSM1_braidedBB1_035 NSM1_braidedBB1_036 w=6.0 h=6.0
784 ESM1_braidedBB1_0041 NSM1_braidedBB1_036 NSM1_braidedBB1_037 w=6.0 h=6.0
785 ESM1_braidedBB1_0042 NSM1_braidedBB1_037 NSM1_braidedBB1_038 w=6.0 h=6.0
786 ESM1_braidedBB1_0043 NSM1_braidedBB1_038 NSM1_braidedBB1_039 w=6.0 h=6.0
787 ESM1_braidedBB1_0044 NSM1_braidedBB1_039 NSM1_braidedBB1_040 w=6.0 h=6.0
788 ESM1_braidedBB1_0050 NSM1_braidedBB1_042 NSM1_braidedBB1_043 w=6.0 h=6.0
789 ESM1_braidedBB1_0051 NSM1_braidedBB1_043 NSM1_braidedBB1_044 w=6.0 h=6.0
790 ESM1_braidedBB1_0052 NSM1_braidedBB1_044 NSM1_braidedBB1_045 w=6.0 h=6.0
791 ESM1_braidedBB1_0053 NSM1_braidedBB1_045 NSM1_braidedBB1_046 w=6.0 h=6.0
792 ESM1_braidedBB1_0054 NSM1_braidedBB1_046 NSM1_braidedBB1_047 w=6.0 h=6.0
793 ESM1_braidedBB1_0060 NSM1_braidedBB1_049 NSM1_braidedBB1_050 w=6.0 h=6.0
794 ESM1_braidedBB1_0061 NSM1_braidedBB1_050 NSM1_braidedBB1_051 w=6.0 h=6.0
795 ESM1_braidedBB1_0062 NSM1_braidedBB1_051 NSM1_braidedBB1_052 w=6.0 h=6.0
796 ESM1_braidedBB1_0063 NSM1_braidedBB1_052 NSM1_braidedBB1_053 w=6.0 h=6.0
797 ESM1_braidedBB1_0064 NSM1_braidedBB1_053 NSM1_braidedBB1_054 w=6.0 h=6.0
798 ESM1_braidedBB1_0070 NSM1_braidedBB1_056 NSM1_braidedBB1_057 w=6.0 h=6.0
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799 ESM1_braidedBB1_0071 NSM1_braidedBB1_057 NSM1_braidedBB1_058 w=6.0 h=6.0
800 ESM1_braidedBB1_0072 NSM1_braidedBB1_058 NSM1_braidedBB1_059 w=6.0 h=6.0
801 ESM1_braidedBB1_0073 NSM1_braidedBB1_059 NSM1_braidedBB1_060 w=6.0 h=6.0
802 ESM1_braidedBB1_0074 NSM1_braidedBB1_060 NSM1_braidedBB1_061 w=6.0 h=6.0
803 ESM1_braidedBB1_0080 NSM1_braidedBB1_063 NSM1_braidedBB1_064 w=6.0 h=6.0
804 ESM1_braidedBB1_0081 NSM1_braidedBB1_064 NSM1_braidedBB1_065 w=6.0 h=6.0
805 ESM1_braidedBB1_0082 NSM1_braidedBB1_065 NSM1_braidedBB1_066 w=6.0 h=6.0
806 ESM1_braidedBB1_0083 NSM1_braidedBB1_066 NSM1_braidedBB1_067 w=6.0 h=6.0
807 ESM1_braidedBB1_0084 NSM1_braidedBB1_067 NSM1_braidedBB1_068 w=6.0 h=6.0
808 ESM1_braidedBB1_0010 NSM1_braidedBB1_014 NSM1_braidedBB1_015 w=6.0 h=6.0
809 ESM1_braidedBB1_0011 NSM1_braidedBB1_015 NSM1_braidedBB1_016 w=6.0 h=6.0
810 ESM1_braidedBB1_0012 NSM1_braidedBB1_016 NSM1_braidedBB1_017 w=6.0 h=6.0
811 ESM1_braidedBB1_0013 NSM1_braidedBB1_017 NSM1_braidedBB1_018 w=6.0 h=6.0
812 ESM1_braidedBB1_0014 NSM1_braidedBB1_018 NSM1_braidedBB1_019 w=6.0 h=6.0
813 ESM1_braidedBB1_0020 NSM1_braidedBB1_021 NSM1_braidedBB1_022 w=6.0 h=6.0
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817 ESM1_braidedBB1_0024 NSM1_braidedBB1_025 NSM1_braidedBB1_026 w=6.0 h=6.0
818 ESM1_braidedBB2_0120 NSM1_braidedBB2_091 NSM1_braidedBB2_092 w=6.0 h=6.0
819 ESM1_braidedBB2_0121 NSM1_braidedBB2_092 NSM1_braidedBB2_093 w=6.0 h=6.0
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821 ESM1_braidedBB2_0123 NSM1_braidedBB2_094 NSM1_braidedBB2_095 w=6.0 h=6.0
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823 ESM1_braidedBB2_0090 NSM1_braidedBB2_070 NSM1_braidedBB2_071 w=6.0 h=6.0
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826 ESM1_braidedBB2_0093 NSM1_braidedBB2_073 NSM1_braidedBB2_074 w=6.0 h=6.0
827 ESM1_braidedBB2_0094 NSM1_braidedBB2_074 NSM1_braidedBB2_075 w=6.0 h=6.0
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835 ESM1_braidedBB2_0112 NSM1_braidedBB2_086 NSM1_braidedBB2_087 w=6.0 h=6.0
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839 ESM1_braidedBB2_0031 NSM1_braidedBB2_029 NSM1_braidedBB2_030 w=6.0 h=6.0
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842 ESM1_braidedBB2_0034 NSM1_braidedBB2_032 NSM1_braidedBB2_033 w=6.0 h=6.0
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849 ESM1_braidedBB2_0051 NSM1_braidedBB2_043 NSM1_braidedBB2_044 w=6.0 h=6.0
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854 ESM1_braidedBB2_0061 NSM1_braidedBB2_050 NSM1_braidedBB2_051 w=6.0 h=6.0
855 ESM1_braidedBB2_0062 NSM1_braidedBB2_051 NSM1_braidedBB2_052 w=6.0 h=6.0
856 ESM1_braidedBB2_0063 NSM1_braidedBB2_052 NSM1_braidedBB2_053 w=6.0 h=6.0
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859 ESM1_braidedBB2_0071 NSM1_braidedBB2_057 NSM1_braidedBB2_058 w=6.0 h=6.0
860 ESM1_braidedBB2_0072 NSM1_braidedBB2_058 NSM1_braidedBB2_059 w=6.0 h=6.0
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873 ESM1_braidedBB2_0020 NSM1_braidedBB2_021 NSM1_braidedBB2_022 w=6.0 h=6.0
874 ESM1_braidedBB2_0021 NSM1_braidedBB2_022 NSM1_braidedBB2_023 w=6.0 h=6.0
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878 ESM1_braidedBB3_0110 NSM1_braidedBB3_090 NSM1_braidedBB3_091 w=6.0 h=6.0
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898 ESM1_braidedBB3_0020 NSM1_braidedBB3_027 NSM1_braidedBB3_028 w=6.0 h=6.0
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902 ESM1_braidedBB3_0024 NSM1_braidedBB3_031 NSM1_braidedBB3_032 w=6.0 h=6.0
903 ESM1_braidedBB3_0030 NSM1_braidedBB3_034 NSM1_braidedBB3_035 w=6.0 h=6.0
904 ESM1_braidedBB3_0031 NSM1_braidedBB3_035 NSM1_braidedBB3_036 w=6.0 h=6.0
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906 ESM1_braidedBB3_0033 NSM1_braidedBB3_037 NSM1_braidedBB3_038 w=6.0 h=6.0
907 ESM1_braidedBB3_0034 NSM1_braidedBB3_038 NSM1_braidedBB3_039 w=6.0 h=6.0
908 ESM1_braidedBB3_0040 NSM1_braidedBB3_041 NSM1_braidedBB3_042 w=6.0 h=6.0
909 ESM1_braidedBB3_0041 NSM1_braidedBB3_042 NSM1_braidedBB3_043 w=6.0 h=6.0
910 ESM1_braidedBB3_0042 NSM1_braidedBB3_043 NSM1_braidedBB3_044 w=6.0 h=6.0
911 ESM1_braidedBB3_0043 NSM1_braidedBB3_044 NSM1_braidedBB3_045 w=6.0 h=6.0
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913 ESM1_braidedBB3_0050 NSM1_braidedBB3_048 NSM1_braidedBB3_049 w=6.0 h=6.0
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956 ESM1-terminal0070 NFHNode483 NFHNode482 w=30.0 h=3.0
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965 EDC+terminal0140 NFHNode527 NFHNode526 w=3.0 h=30.0
966 EDC+terminal0150 NFHNode529 NFHNode528 w=30.0 h=3.0
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968 EDC+terminal0170 NFHNode533 NFHNode532 w=30.0 h=3.0
969 EDC+terminal0180 NFHNode535 NFHNode534 w=3.0 h=30.0
970 EDC+terminal0190 NFHNode537 NFHNode536 w=30.0 h=3.0
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972 ESM1-terminal0120 NFHNode541 NFHNode540 w=30.0 h=3.0
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976 ESM1-terminal0160 NFHNode549 NFHNode548 w=30.0 h=3.0
977 ESM1-terminal0170 NFHNode551 NFHNode550 w=3.0 h=30.0
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983 ESM3_braidedBB1_0112 NSM3_braidedBB1_092 NSM3_braidedBB1_093 w=6.0 h=6.0
984 ESM3_braidedBB1_0113 NSM3_braidedBB1_093 NSM3_braidedBB1_094 w=6.0 h=6.0
985 ESM3_braidedBB1_0114 NSM3_braidedBB1_094 NSM3_braidedBB1_095 w=6.0 h=6.0
986 ESM3_braidedBB1_0080 NSM3_braidedBB1_069 NSM3_braidedBB1_070 w=6.0 h=6.0
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988 ESM3_braidedBB1_0082 NSM3_braidedBB1_071 NSM3_braidedBB1_072 w=6.0 h=6.0
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1023 ESM3_braidedBB1_0062 NSM3_braidedBB1_057 NSM3_braidedBB1_058 w=6.0 h=6.0
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1112 ESM3_braidedBB3_0091 NSM3_braidedBB3_077 NSM3_braidedBB3_078 w=6.0 h=6.0
1113 ESM3_braidedBB3_0092 NSM3_braidedBB3_078 NSM3_braidedBB3_079 w=6.0 h=6.0
1114 ESM3_braidedBB3_0093 NSM3_braidedBB3_079 NSM3_braidedBB3_080 w=6.0 h=6.0
1115 ESM3_braidedBB3_0094 NSM3_braidedBB3_080 NSM3_braidedBB3_081 w=6.0 h=6.0
1116 ESM3_braidedBB3_0100 NSM3_braidedBB3_083 NSM3_braidedBB3_084 w=6.0 h=6.0
1117 ESM3_braidedBB3_0101 NSM3_braidedBB3_084 NSM3_braidedBB3_085 w=6.0 h=6.0
1118 ESM3_braidedBB3_0102 NSM3_braidedBB3_085 NSM3_braidedBB3_086 w=6.0 h=6.0
1119 ESM3_braidedBB3_0103 NSM3_braidedBB3_086 NSM3_braidedBB3_087 w=6.0 h=6.0
1120 ESM3_braidedBB3_0104 NSM3_braidedBB3_087 NSM3_braidedBB3_088 w=6.0 h=6.0
1121 ESM3_braidedBB3_0020 NSM3_braidedBB3_027 NSM3_braidedBB3_028 w=6.0 h=6.0
1122 ESM3_braidedBB3_0021 NSM3_braidedBB3_028 NSM3_braidedBB3_029 w=6.0 h=6.0
1123 ESM3_braidedBB3_0022 NSM3_braidedBB3_029 NSM3_braidedBB3_030 w=6.0 h=6.0
1124 ESM3_braidedBB3_0023 NSM3_braidedBB3_030 NSM3_braidedBB3_031 w=6.0 h=6.0
1125 ESM3_braidedBB3_0024 NSM3_braidedBB3_031 NSM3_braidedBB3_032 w=6.0 h=6.0
1126 ESM3_braidedBB3_0030 NSM3_braidedBB3_034 NSM3_braidedBB3_035 w=6.0 h=6.0
1127 ESM3_braidedBB3_0031 NSM3_braidedBB3_035 NSM3_braidedBB3_036 w=6.0 h=6.0
1128 ESM3_braidedBB3_0032 NSM3_braidedBB3_036 NSM3_braidedBB3_037 w=6.0 h=6.0
1129 ESM3_braidedBB3_0033 NSM3_braidedBB3_037 NSM3_braidedBB3_038 w=6.0 h=6.0
1130 ESM3_braidedBB3_0034 NSM3_braidedBB3_038 NSM3_braidedBB3_039 w=6.0 h=6.0
1131 ESM3_braidedBB3_0040 NSM3_braidedBB3_041 NSM3_braidedBB3_042 w=6.0 h=6.0
1132 ESM3_braidedBB3_0041 NSM3_braidedBB3_042 NSM3_braidedBB3_043 w=6.0 h=6.0
1133 ESM3_braidedBB3_0042 NSM3_braidedBB3_043 NSM3_braidedBB3_044 w=6.0 h=6.0
1134 ESM3_braidedBB3_0043 NSM3_braidedBB3_044 NSM3_braidedBB3_045 w=6.0 h=6.0
1135 ESM3_braidedBB3_0044 NSM3_braidedBB3_045 NSM3_braidedBB3_046 w=6.0 h=6.0
1136 ESM3_braidedBB3_0050 NSM3_braidedBB3_048 NSM3_braidedBB3_049 w=6.0 h=6.0
1137 ESM3_braidedBB3_0051 NSM3_braidedBB3_049 NSM3_braidedBB3_050 w=6.0 h=6.0
1138 ESM3_braidedBB3_0052 NSM3_braidedBB3_050 NSM3_braidedBB3_051 w=6.0 h=6.0
1139 ESM3_braidedBB3_0053 NSM3_braidedBB3_051 NSM3_braidedBB3_052 w=6.0 h=6.0
1140 ESM3_braidedBB3_0054 NSM3_braidedBB3_052 NSM3_braidedBB3_053 w=6.0 h=6.0
1141 ESM3_braidedBB3_0060 NSM3_braidedBB3_055 NSM3_braidedBB3_056 w=6.0 h=6.0
1142 ESM3_braidedBB3_0061 NSM3_braidedBB3_056 NSM3_braidedBB3_057 w=6.0 h=6.0
1143 ESM3_braidedBB3_0062 NSM3_braidedBB3_057 NSM3_braidedBB3_058 w=6.0 h=6.0
1144 ESM3_braidedBB3_0063 NSM3_braidedBB3_058 NSM3_braidedBB3_059 w=6.0 h=6.0
1145 ESM3_braidedBB3_0064 NSM3_braidedBB3_059 NSM3_braidedBB3_060 w=6.0 h=6.0
1146 ESM3_braidedBB3_0070 NSM3_braidedBB3_062 NSM3_braidedBB3_063 w=6.0 h=6.0
```

```
ESM3_braidedBB3_0071 NSM3_braidedBB3_063 NSM3_braidedBB3_064 w=6.0 h=6.0
ESM3_braidedBB3_0072 NSM3_braidedBB3_064 NSM3_braidedBB3_065 w=6.0 h=6.0
ESM3_braidedBB3_0073 NSM3_braidedBB3_065 NSM3_braidedBB3_066 w=6.0 h=6.0
ESM3_braidedBB3_0074 NSM3_braidedBB3_066 NSM3_braidedBB3_067 w=6.0 h=6.0
ESM3_braidedBB3_0 NSM3_braidedBB3_013 NSM3_braidedBB3_014 w=6.0 h=6.0
ESM3_braidedBB3_1 NSM3_braidedBB3_014 NSM3_braidedBB3_015 w=6.0 h=6.0
ESM3_braidedBB3_2 NSM3_braidedBB3_015 NSM3_braidedBB3_016 w=6.0 h=6.0
ESM3_braidedBB3_3 NSM3_braidedBB3_016 NSM3_braidedBB3_017 w=6.0 h=6.0
ESM3_braidedBB3_4 NSM3_braidedBB3_017 NSM3_braidedBB3_018 w=6.0 h=6.0
ESM3_braidedBB3_0010 NSM3_braidedBB3_020 NSM3_braidedBB3_021 w=6.0 h=6.0
ESM3_braidedBB3_0011 NSM3_braidedBB3_021 NSM3_braidedBB3_022 w=6.0 h=6.0
ESM3_braidedBB3_0012 NSM3_braidedBB3_022 NSM3_braidedBB3_023 w=6.0 h=6.0
ESM3_braidedBB3_0013 NSM3_braidedBB3_023 NSM3_braidedBB3_024 w=6.0 h=6.0
ESM3_braidedBB3_0014 NSM3_braidedBB3_024 NSM3_braidedBB3_025 w=6.0 h=6.0
Eoutput_busbar0020 NFHNode813 NFHNode812 w=20.0 h=20.0
Eoutput_busbar0030 NFHNode815 NFHNode816 w=20.0 h=20.0
Eoutput_busbar0031 NFHNode816 NFHNode814 w=20.0 h=20.0

* Planes
GSM1-plane x1=-375.5 y1=477.5 z1=30.4999999999999 x2=-375.5 y2=25.5 ...
    ↪ z2=30.4999999999999
+         x3=-375.5 y3=25.5 z3=142.6
+         thick=3.0 seg1=15 seg2=7
+         NSM1-_IGBTinterfacep (-374.0,444.0,137.59999999999994)
+         NSM1-_IGBTinterface001p ...
    ↪ (-374.0,397.99999999999994,137.5999999999999)
+         NSM1-_IGBTinterface002p (-374.0,331.0,137.5999999999999)
+         NSM1-_IGBTinterface003p ...
    ↪ (-374.00000000000006,285.0,137.59999999999988)
+         NSM1-_IGBTinterface004p ...
    ↪ (-374.00000000000006,218.00000000000006,137.59999999999988)
+         NSM1-_IGBTinterface005p ...
    ↪ (-374.00000000000006,172.00000000000006,137.59999999999988)
+         NSM1-_IGBTinterface006p ...
    ↪ (-374.00000000000006,105.00000000000006,137.59999999999985)
+         NSM1-_IGBTinterface007p ...
    ↪ (-374.00000000000006,59.00000000000006,137.59999999999985)
+         NSM1_DCinterfacep ...
    ↪ (-375.50000000000006,35.50000000000006,30.499999999999876)
+         NSM1_DCinterface001p ...
    ↪ (-375.50000000000006,131.50000000000006,30.499999999999826)
+         NSM1_DCinterface002p (-375.5,419.5,30.499999999999908)
+         NSM1_DCinterface003p (-375.5,323.5,30.49999999999988)
+         NSM1_DCinterface004p ...
    ↪ (-375.5,227.50000000000003,30.499999999999854)
+         hole circle (-374.0,444.00000000000017,108.1,15.0)
+         hole circle (-374.0,398.0000000000001,108.09999999999998,15.0)
+         hole circle (-374.0,331.0000000000001,108.09999999999998,15.0)
+         hole circle ...
    ↪ (-374.00000000000006,285.0000000000001,108.09999999999997,15.0)
+         hole circle ...
    ↪ (-374.00000000000006,218.0000000000001,108.09999999999997,15.0)
+         hole circle ...
    ↪ (-374.00000000000006,172.00000000000006,108.09999999999997,15.0)
+         hole circle ...
    ↪ (-374.00000000000006,105.00000000000006,108.09999999999995,15.0)
+         hole circle ...
    ↪ (-374.00000000000006,59.00000000000006,108.09999999999995,15.0)
```

```
1190
1191 * Connecting internal plane nodes to actual nodes
1192 .equiv NSM1-_IGBTinterface NSM1-_IGBTinterfacep
1193 .equiv NSM1-_IGBTinterface001 NSM1-_IGBTinterface001p
1194 .equiv NSM1-_IGBTinterface002 NSM1-_IGBTinterface002p
1195 .equiv NSM1-_IGBTinterface003 NSM1-_IGBTinterface003p
1196 .equiv NSM1-_IGBTinterface004 NSM1-_IGBTinterface004p
1197 .equiv NSM1-_IGBTinterface005 NSM1-_IGBTinterface005p
1198 .equiv NSM1-_IGBTinterface006 NSM1-_IGBTinterface006p
1199 .equiv NSM1-_IGBTinterface007 NSM1-_IGBTinterface007p
1200 .equiv NSM1_DCinterface NSM1_DCinterfacep
1201 .equiv NSM1_DCinterface001 NSM1_DCinterface001p
1202 .equiv NSM1_DCinterface002 NSM1_DCinterface002p
1203 .equiv NSM1_DCinterface003 NSM1_DCinterface003p
1204 .equiv NSM1_DCinterface004 NSM1_DCinterface004p
1205
1206 GSM1+plane x1=-372.15 y1=477.5 z1=27.9999999999999 x2=-372.15 y2=25.5 ...
        ↪ z2=27.9999999999999
1207 +          x3=-372.15 y3=25.5 z3=113.1
1208 +          thick=3.0 seg1=15 seg2=5
1209 +          NSM1+_IGBTinterfacep ...
        ↪ (-370.65,444.00000000000006,108.09999999999997)
1210 +          NSM1+_IGBTinterface001p ...
        ↪ (-370.65,398.00000000000006,108.09999999999995)
1211 +          NSM1+_IGBTinterface002p (-370.65,331.0,108.09999999999995)
1212 +          NSM1+_IGBTinterface003p ...
        ↪ (-370.65000000000003,285.0,108.09999999999991)
1213 +          NSM1+_IGBTinterface004p ...
        ↪ (-370.65000000000003,218.00000000000006,108.09999999999991)
1214 +          NSM1+_IGBTinterface005p ...
        ↪ (-370.65000000000003,172.00000000000006,108.09999999999988)
1215 +          NSM1+_IGBTinterface006p ...
        ↪ (-370.65000000000003,105.00000000000006,108.09999999999987)
1216 +          NSM1+_IGBTinterface007p ...
        ↪ (-370.65000000000003,59.00000000000006,108.09999999999987)
1217 +          NDCinterface006p (-372.15,371.5,27.99999999999997)
1218 +          NDCinterface007p (-372.15,275.5,27.999999999999943)
1219 +          NDCinterface008p ...
        ↪ (-372.15000000000003,179.50000000000006,27.99999999999992)
1220 +          NDCinterface009p ...
        ↪ (-372.15000000000003,83.50000000000006,27.99999999999989)
1221 +          NDCinterface005p (-372.15,467.5,27.999999999999996)
1222
1223 * Connecting internal plane nodes to actual nodes
1224 .equiv NSM1+_IGBTinterface NSM1+_IGBTinterfacep
1225 .equiv NSM1+_IGBTinterface001 NSM1+_IGBTinterface001p
1226 .equiv NSM1+_IGBTinterface002 NSM1+_IGBTinterface002p
1227 .equiv NSM1+_IGBTinterface003 NSM1+_IGBTinterface003p
1228 .equiv NSM1+_IGBTinterface004 NSM1+_IGBTinterface004p
1229 .equiv NSM1+_IGBTinterface005 NSM1+_IGBTinterface005p
1230 .equiv NSM1+_IGBTinterface006 NSM1+_IGBTinterface006p
1231 .equiv NSM1+_IGBTinterface007 NSM1+_IGBTinterface007p
1232 .equiv NDCinterface006 NDCinterface006p
1233 .equiv NDCinterface007 NDCinterface007p
1234 .equiv NDCinterface008 NDCinterface008p
1235 .equiv NDCinterface009 NDCinterface009p
1236 .equiv NDCinterface005 NDCinterface005p
1237
```

```
1238 GFHPlane002 x1=-411.65702315386 y1=2.343389583628662 z1=1.5 ...
     ↪ x2=411.6568542494904 y2=2.343145446888445 z2=1.5000000016383648
1239 +          x3=411.6570233641878 y3=572.6566101127589 z3=1.4999999977756164
1240 +          thick=2.0 seg1=40 seg2=30
1241 +          NSM1interface001p ...
     ↪ (-389.9999998461609,419.4999999920201,1.4999999972176954)
1242 +          NSM1interface002p ...
     ↪ (-389.9999998815646,323.49999999202015,1.4999999978679035)
1243 +          NSM1interface003p ...
     ↪ (-389.9999999169679,227.49999999202004,1.4999999985181116)
1244 +          NSM1interface004p ...
     ↪ (-389.9999999523709,131.49999999202007,1.4999999991683195)
1245 +          NSM1interfacep ...
     ↪ (-389.99999998777423,35.49999999202008,1.4999999998185278)
1246 +          NSM2interfacep ...
     ↪ (-119.99999984616096,419.4999998924482,1.499999997754995)
1247 +          NSM2interface001p ...
     ↪ (-119.99999988156463,323.4999998924482,1.4999999984052028)
1248 +          NSM2interface002p ...
     ↪ (-119.99999991696797,227.49999989244813,1.4999999990554111)
1249 +          NSM2interface003p ...
     ↪ (-119.99999995237096,131.49999989244813,1.499999999705619)
1250 +          NSM2interface004p ...
     ↪ (-119.99999998777429,35.49999989244816,1.5000000003558271)
1251 +          NSM3interfacep ...
     ↪ (150.0000000122256,35.49999979287624,1.5000000008931267)
1252 +          NSM3interface001p ...
     ↪ (150.00000004762904,131.49999979287622,1.5000000002429186)
1253 +          NSM3interface002p ...
     ↪ (150.00000008303215,227.4999997928762,1.4999999995927105)
1254 +          NSM3interface003p ...
     ↪ (150.00000011843537,323.49999979287634,1.4999999989425024)
1255 +          NSM3interface004p ...
     ↪ (150.00000015383904,419.4999997928763,1.4999999982922945)
1256 +          NDCcapp (-314.00028122022,419.99999996400936,1.4999999973655482)
1257 +          NDCcap001p ...
     ↪ (-314.0002812681621,289.9999999640094,1.4999999982460384)
1258 +          NDCcap002p ...
     ↪ (-201.4169787522141,354.99999992249036,1.4999999980298337)
1259 +          NDCcap003p ...
     ↪ (-201.41697870427208,484.9999999224904,1.4999999971493438)
1260 +          NDCcap004p ...
     ↪ (-201.41697880015616,224.99999992249042,1.4999999989103239)
1261 +          NDCcap005p ...
     ↪ (-44.0002812681621,289.99999986443754,1.4999999987833377)
1262 +          NDCcap006p ...
     ↪ (-44.000281220220074,419.9999998644374,1.4999999979028478)
1263 +          NDCcap007p ...
     ↪ (68.58302129572792,484.9999998229185,1.4999999976866434)
1264 +          NDCcap008p ...
     ↪ (225.9997187797798,419.99999976486555,1.4999999984401473)
1265 +          NDCcap009p ...
     ↪ (338.58302129572786,484.9999997233466,1.4999999982239427)
1266 +          NDCcap010p ...
     ↪ (68.58302124778584,354.9999998229184,1.4999999985671333)
1267 +          NDCcap011p ...
     ↪ (338.5830212477858,354.99999972334655,1.4999999991044328)
```

```
1268 +         NDCcap012p ...
     ↪ (225.99971873183773,289.9999997648656,1.4999999993206372)
1269 +         NDCcap013p ...
     ↪ (68.58302119984381,224.99999982291848,1.4999999994476234)
1270 +         NDCcap014p ...
     ↪ (338.5830211998438,224.99999972334658,1.4999999999849227)
1271 +         NDCcap015p ...
     ↪ (225.99971868389565,159.99999976486546,1.5000000002011273)
1272 +         NDCcap016p ...
     ↪ (338.58302115190173,94.99999972334656,1.5000000008654129)
1273 +         NDCcap017p ...
     ↪ (225.99971863595368,29.999999764865482,1.5000000010816175)
1274 +         NDCcap018p ...
     ↪ (68.58302115190179,94.99999982291848,1.5000000003281135)
1275 +         NDCcap019p ...
     ↪ (-44.00028131610412,159.9999998644374,1.499999999663828)
1276 +         NDCcap020p ...
     ↪ (-44.000281364046145,29.9999998644374,1.500000000544318)
1277 +         NDCcap021p ...
     ↪ (-201.41697884809818,94.9999999224904,1.499999999790814)
1278 +         NDCcap022p ...
     ↪ (-314.0002813161041,159.9999999640093,1.4999999991265285)
1279 +         NDCcap023p ...
     ↪ (-313.9999594421053,29.999999964009202,1.500000000007019)
1280 +         hole rect ...
     ↪ (-414.0027447188822,447.4933902792168,0.4999999969803308,-355.00273285770965,487.4933
1281
1282 +         hole rect ...
     ↪ (-414.0015330757505,255.49339027884906,0.4999999982807493,-355.00152121457796,295.4933
1283
1284 +         hole rect ...
     ↪ (-414.00213889731634,351.4933902790329,0.4999999976305401,-355.0021270361438,391.49337
1285
1286 +         hole rect ...
     ↪ (-414.0009272541848,159.4933902786652,0.4999999989309586,-355.00091539301224,199.49337
1287
1288 +         hole rect ...
     ↪ (-414.0003214326189,63.49339027848133,0.49999999958116786,-355.00030957144634,103.4933
1289
1290 +         hole rect ...
     ↪ (-149.99689115382324,447.49331199372904,0.49999999750570245,-90.99687929265068,487.493
1291
1292 +         hole rect ...
     ↪ (-149.99694808746108,255.49331199373748,0.49999999880611845,-90.99693622628851,295.493
1293
1294 +         hole rect ...
     ↪ (-149.99691962064213,351.4933119937332,0.49999999815591045,-90.99690775946956,391.4932
1295
1296 +         hole rect ...
     ↪ (-149.99697655427997,159.4933119937417,0.49999999945632645,-90.9969646931074,199.49329
1297
1298 +         hole rect ...
     ↪ (-149.99700502109886,63.49331199374592,0.5000000001065344,-90.99699315992629,103.49329
1299
1300 +         hole rect ...
     ↪ (120.00310884616471,447.49323193080085,0.49999999804300244,179.00312070733727,487.4932
1301
```

```
+         hole rect ...
    ↪ (120.00305191252693,255.49323193080932,0.49999999934341843,179.0030637736995,295.4932
+         hole rect ...
    ↪ (120.00308037934582,351.49323193080494,0.49999999869321043,179.00309224051838,391.4932
+         hole rect ...
    ↪ (120.00302344570804,159.49323193081355,0.49999999999362643,179.0030353068806,199.4932
+         hole rect ...
    ↪ (120.00299497888915,63.49323193081774,0.5000000006438344,179.00300684006172,103.493214


* Connecting internal plane nodes to actual nodes
.equiv NSM1interface001 NSM1interface001p
.equiv NSM1interface002 NSM1interface002p
.equiv NSM1interface003 NSM1interface003p
.equiv NSM1interface004 NSM1interface004p
.equiv NSM1interface NSM1interfacep
.equiv NSM2interface NSM2interfacep
.equiv NSM2interface001 NSM2interface001p
.equiv NSM2interface002 NSM2interface002p
.equiv NSM2interface003 NSM2interface003p
.equiv NSM2interface004 NSM2interface004p
.equiv NSM3interface NSM3interfacep
.equiv NSM3interface001 NSM3interface001p
.equiv NSM3interface002 NSM3interface002p
.equiv NSM3interface003 NSM3interface003p
.equiv NSM3interface004 NSM3interface004p
.equiv NDCcap NDCcapp
.equiv NDCcap001 NDCcap001p
.equiv NDCcap002 NDCcap002p
.equiv NDCcap003 NDCcap003p
.equiv NDCcap004 NDCcap004p
.equiv NDCcap005 NDCcap005p
.equiv NDCcap006 NDCcap006p
.equiv NDCcap007 NDCcap007p
.equiv NDCcap008 NDCcap008p
.equiv NDCcap009 NDCcap009p
.equiv NDCcap010 NDCcap010p
.equiv NDCcap011 NDCcap011p
.equiv NDCcap012 NDCcap012p
.equiv NDCcap013 NDCcap013p
.equiv NDCcap014 NDCcap014p
.equiv NDCcap015 NDCcap015p
.equiv NDCcap016 NDCcap016p
.equiv NDCcap017 NDCcap017p
.equiv NDCcap018 NDCcap018p
.equiv NDCcap019 NDCcap019p
.equiv NDCcap020 NDCcap020p
.equiv NDCcap021 NDCcap021p
.equiv NDCcap022 NDCcap022p
.equiv NDCcap023 NDCcap023p

GFHPlane003 x1=-401.660000000002 y1=-152.33999999999324 z1=-1.0 ...
    ↪ x2=411.6499999999621 y2=-152.34024117027923 z2=-0.9999999983815426
+         x3=411.6502284195079 y3=617.9697588296868 z3=-1.0000000035987018
+         thick=2.0 seg1=30 seg2=30
```

```
1355 +         NDCcap039p ...
     ↪ (68.58330249197905,274.99999999999295,-1.0000000019585908)
1356 +         NDCcap047p ...
     ↪ (338.58330249197905,144.99999999999304,-1.0000000005408012)
1357 +         NSM1interface005p ...
     ↪ (-389.99999999999784,467.49999999999307,-1.0000000041749733)
1358 +         NSM3interface005p ...
     ↪ (150.0000000000021,83.49999999999304,-1.0000000004995422)
1359 +         NSM2interface006p ...
     ↪ (-119.99999999999926,371.4999999999974,-1.0000000029874658)
1360 +         NSM3interface009p ...
     ↪ (150.00000000000222,467.49999999999284,-1.0000000031003744)
1361 +         NDCcap030p ...
     ↪ (-313.9999999999979,339.9999999999932,-1.000000003160176)
1362 +         NSM3interface006p ...
     ↪ (150.000000000002,179.49999999999292,-1.00000000114975)
1363 +         NDCcap024p ...
     ↪ (-313.99999999999784,469.99999999999307,-1.000000004040666)
1364 +         NSM3interface008p ...
     ↪ (150.0000000000021,371.49999999999295,-1.0000000024501663)
1365 +         NSM1interface007p ...
     ↪ (-389.99999999999784,275.4999999999932,-1.000000002874557)
1366 +         NDCcap028p ...
     ↪ (226.000000000002,469.99999999999295,-1.000000002966067)
1367 +         NDCcap038p ...
     ↪ (-43.99999999999801,209.99999999999304,-1.0000000017423862)
1368 +         NDCcap026p ...
     ↪ (-43.99999999999778,469.99999999999295,-1.0000000035033665)
1369 +         NDCcap032p ...
     ↪ (-43.9999999999979,339.99999999999307,-1.0000000026228766)
1370 +         NSM1interface006p ...
     ↪ (-389.9999999999979,371.4999999999932,-1.0000000035247654)
1371 +         NSM1interface009p ...
     ↪ (-389.9999999999993,83.49999999999739,-1.000000001574141)
1372 +         NSM2interface005p ...
     ↪ (-119.99999999999915,467.49999999999727,-1.0000000036376737)
1373 +         NSM1interface008p ...
     ↪ (-389.99999999999926,179.4999999999973,-1.0000000022243491)
1374 +         NDCcap029p ...
     ↪ (338.58330249197917,534.9999999999932,-1.0000000031822716)
1375 +         NSM2interface008p ...
     ↪ (-119.99999999999795,179.49999999999304,-1.0000000016870496)
1376 +         NSM2interface007p ...
     ↪ (-119.99999999999801,275.49999999999307,-1.0000000023372577)
1377 +         NSM2interface009p ...
     ↪ (-119.99999999999801,83.4999999999931,-1.0000000010368417)
1378 +         NDCcap027p ...
     ↪ (68.58330249197911,534.9999999999933,-1.0000000037195709)
1379 +         NSM3interface007p ...
     ↪ (150.000000000002,275.49999999999295,-1.0000000017999584)
1380 +         NDCcap031p ...
     ↪ (-201.41669750802095,404.9999999999933,-1.0000000033763805)
1381 +         NDCcap025p ...
     ↪ (-201.41669750802086,534.9999999999934,-1.0000000042568704)
1382 +         NDCcap046p ...
     ↪ (226.00000000000188,79.99999999999298,-1.0000000003245968)
1383 +         NDCcap035p ...
     ↪ (338.58330249197894,404.99999999999295,-1.0000000023017814)
```

```
+          NDCcap033p ...
    ↪ (68.58330249197911,404.99999999999307,-1.000000002839081)
+          NDCcap037p ...
    ↪ (-201.41669750802095,274.9999999999932,-1.0000000024958902)
+          NDCcap036p ...
    ↪ (-313.99999999999795,209.99999999999315,-1.0000000022796858)
+          NDCcap034p ...
    ↪ (226.000000000002,339.99999999999295,-1.000000002085577)
+          NDCcap041p ...
    ↪ (338.58330249197894,274.99999999999295,-1.0000000014212915)
+          NDCcap040p ...
    ↪ (226.00000000000188,209.99999999999292,-1.000000001205087)
+          NDCcap042p ...
    ↪ (-313.999999999998,79.99999999999318,-1.0000000013991959)
+          NDCcap044p ...
    ↪ (-43.99999999999801,79.99999999999307,-1.0000000008618963)
+          NDCcap045p ...
    ↪ (68.58330249197905,144.9999999999931,-1.0000000010781007)
+          NDCcap043p ...
    ↪ (-201.41669750802103,144.9999999999932,-1.0000000016154003)
+          NLoad_connection_SM1p ...
    ↪ (-210.39999999999583,-130.00000000001438,-0.9999999997707019)
+          Nload_connection_SM3p ...
    ↪ (329.59999999999974,615.0000000000002,-1.0000000037419885)
+          NDC_choke_connectionp ...
    ↪ (344.600000000016,-100.00000000005463,-0.999999998869443)
+          NAir_choke_connection1p ...
    ↪ (-339.99999999999625,610.9999999999858,-1.000000005047399)

* Connecting internal plane nodes to actual nodes
.equiv NDCcap039 NDCcap039p
.equiv NDCcap047 NDCcap047p
.equiv NSM1interface005 NSM1interface005p
.equiv NSM3interface005 NSM3interface005p
.equiv NSM2interface006 NSM2interface006p
.equiv NSM3interface009 NSM3interface009p
.equiv NDCcap030 NDCcap030p
.equiv NSM3interface006 NSM3interface006p
.equiv NDCcap024 NDCcap024p
.equiv NSM3interface008 NSM3interface008p
.equiv NSM1interface007 NSM1interface007p
.equiv NDCcap028 NDCcap028p
.equiv NDCcap038 NDCcap038p
.equiv NDCcap026 NDCcap026p
.equiv NDCcap032 NDCcap032p
.equiv NSM1interface006 NSM1interface006p
.equiv NSM1interface009 NSM1interface009p
.equiv NSM2interface005 NSM2interface005p
.equiv NSM1interface008 NSM1interface008p
.equiv NDCcap029 NDCcap029p
.equiv NSM2interface008 NSM2interface008p
.equiv NSM2interface007 NSM2interface007p
.equiv NSM2interface009 NSM2interface009p
.equiv NDCcap027 NDCcap027p
.equiv NSM3interface007 NSM3interface007p
.equiv NDCcap031 NDCcap031p
.equiv NDCcap025 NDCcap025p
.equiv NDCcap046 NDCcap046p
```

```
1428 .equiv NDCcap035 NDCcap035p
1429 .equiv NDCcap033 NDCcap033p
1430 .equiv NDCcap037 NDCcap037p
1431 .equiv NDCcap036 NDCcap036p
1432 .equiv NDCcap034 NDCcap034p
1433 .equiv NDCcap041 NDCcap041p
1434 .equiv NDCcap040 NDCcap040p
1435 .equiv NDCcap042 NDCcap042p
1436 .equiv NDCcap044 NDCcap044p
1437 .equiv NDCcap045 NDCcap045p
1438 .equiv NDCcap043 NDCcap043p
1439 .equiv NLoad_connection_SM1 NLoad_connection_SM1p
1440 .equiv Nload_connection_SM3 Nload_connection_SM3p
1441 .equiv NDC_choke_connection NDC_choke_connectionp
1442 .equiv NAir_choke_connection1 NAir_choke_connection1p
1443
1444 GFHPlane004 x1=-105.5 y1=477.5 z1=30.4999999999999 x2=-105.5 y2=25.5 ...
        ↪ z2=30.4999999999999
1445 +          x3=-105.5 y3=25.5 z3=142.6
1446 +          thick=3.0 seg1=15 seg2=7
1447 +          NIGBTinterface017p (-104.00000000000001,444.0,137.59999999999994)
1448 +          NIGBTinterface019p ...
        ↪ (-104.00000000000001,397.99999999999994,137.5999999999999)
1449 +          NIGBTinterface021p (-104.00000000000003,331.0,137.5999999999999)
1450 +          NIGBTinterface023p (-104.00000000000003,285.0,137.59999999999988)
1451 +          NIGBTinterface025p ...
        ↪ (-104.00000000000004,218.00000000000006,137.59999999999988)
1452 +          NIGBTinterface027p ...
        ↪ (-104.00000000000004,172.00000000000006,137.59999999999988)
1453 +          NIGBTinterface029p ...
        ↪ (-104.00000000000006,105.00000000000006,137.59999999999985)
1454 +          NIGBTinterface031p ...
        ↪ (-104.00000000000006,59.00000000000006,137.59999999999985)
1455 +          NDCinterface010p ...
        ↪ (-105.50000000000004,35.50000000000006,30.499999999999876)
1456 +          NDCinterface011p ...
        ↪ (-105.50000000000004,131.50000000000006,30.499999999999826)
1457 +          NDCinterface014p (-105.5,419.5,30.499999999999908)
1458 +          NDCinterface013p (-105.50000000000001,323.5,30.49999999999988)
1459 +          NDCinterface012p ...
        ↪ (-105.50000000000003,227.50000000000003,30.499999999999854)
1460 +          hole circle (-104.00000000000001,444.00000000000017,108.1,15.0)
1461 +          hole circle ...
        ↪ (-104.00000000000001,398.0000000000001,108.09999999999998,15.0)
1462 +          hole circle ...
        ↪ (-104.00000000000003,331.0000000000001,108.09999999999998,15.0)
1463 +          hole circle ...
        ↪ (-104.00000000000003,285.0000000000001,108.09999999999997,15.0)
1464 +          hole circle ...
        ↪ (-104.00000000000004,218.0000000000001,108.09999999999997,15.0)
1465 +          hole circle ...
        ↪ (-104.00000000000004,172.00000000000006,108.09999999999997,15.0)
1466 +          hole circle ...
        ↪ (-104.00000000000006,105.00000000000006,108.09999999999995,15.0)
1467 +          hole circle ...
        ↪ (-104.00000000000006,59.00000000000006,108.09999999999995,15.0)
1468
1469 * Connecting internal plane nodes to actual nodes
```

```
.equiv NIGBTinterface017 NIGBTinterface017p
.equiv NIGBTinterface019 NIGBTinterface019p
.equiv NIGBTinterface021 NIGBTinterface021p
.equiv NIGBTinterface023 NIGBTinterface023p
.equiv NIGBTinterface025 NIGBTinterface025p
.equiv NIGBTinterface027 NIGBTinterface027p
.equiv NIGBTinterface029 NIGBTinterface029p
.equiv NIGBTinterface031 NIGBTinterface031p
.equiv NDCinterface010 NDCinterface010p
.equiv NDCinterface011 NDCinterface011p
.equiv NDCinterface014 NDCinterface014p
.equiv NDCinterface013 NDCinterface013p
.equiv NDCinterface012 NDCinterface012p

GFHPlane005 x1=-102.15 y1=477.5 z1=27.9999999999999 x2=-102.15 y2=25.5 ...
    ↪ z2=27.9999999999999
+         x3=-102.15 y3=25.5 z3=113.1
+         thick=3.0 seg1=15 seg2=5
+         NIGBTinterface016p ...
    ↪ (-100.65000000000002,444.00000000000006,108.09999999999997)
+         NIGBTinterface018p ...
    ↪ (-100.65000000000002,398.00000000000006,108.09999999999995)
+         NIGBTinterface020p (-100.65000000000003,331.0,108.09999999999995)
+         NIGBTinterface022p (-100.65000000000003,285.0,108.09999999999991)
+         NIGBTinterface024p ...
    ↪ (-100.65000000000005,218.00000000000006,108.09999999999991)
+         NIGBTinterface026p ...
    ↪ (-100.65000000000005,172.00000000000006,108.09999999999988)
+         NIGBTinterface028p ...
    ↪ (-100.65000000000006,105.00000000000006,108.09999999999987)
+         NIGBTinterface030p ...
    ↪ (-100.65000000000006,59.00000000000006,108.09999999999987)
+         NDCinterface019p (-102.15,467.5,27.999999999999996)
+         NDCinterface018p (-102.15000000000002,371.5,27.99999999999997)
+         NDCinterface017p (-102.15000000000003,275.5,27.999999999999943)
+         NDCinterface016p ...
    ↪ (-102.15000000000003,179.50000000000006,27.99999999999992)
+         NDCinterface015p ...
    ↪ (-102.15000000000005,83.50000000000006,27.99999999999989)

* Connecting internal plane nodes to actual nodes
.equiv NIGBTinterface016 NIGBTinterface016p
.equiv NIGBTinterface018 NIGBTinterface018p
.equiv NIGBTinterface020 NIGBTinterface020p
.equiv NIGBTinterface022 NIGBTinterface022p
.equiv NIGBTinterface024 NIGBTinterface024p
.equiv NIGBTinterface026 NIGBTinterface026p
.equiv NIGBTinterface028 NIGBTinterface028p
.equiv NIGBTinterface030 NIGBTinterface030p
.equiv NDCinterface019 NDCinterface019p
.equiv NDCinterface018 NDCinterface018p
.equiv NDCinterface017 NDCinterface017p
.equiv NDCinterface016 NDCinterface016p
.equiv NDCinterface015 NDCinterface015p

GAC_busbar_plane x1=-354.14861323961185 y1=45.49944344811606 z1=334.1 ...
    ↪ x2=-234.14999999999742 y2=45.49999998694893 z2=334.0999999996726
+         x3=-234.15138672786904 y3=344.50055653883345 z3=334.0999999995876
```

```
1518 +         thick=2.0 seg1=30 seg2=30
1519 +         sigma=35000.0
1520 +         Noutput_busbar_interfacep ...
     ↪ (-264.1499999857096,194.99999999137978,334.0999999997084)
1521 +         Nbraided_busbar_interface002p ...
     ↪ (-315.89999997257235,331.9999999963371,334.0999999998092)
1522 +         Nbraided_busbar_interface006p ...
     ↪ (-315.89999997487035,307.9999999963371,334.0999999998164)
1523 +         Nbraided_busbar_interface010p ...
     ↪ (-315.8999999771684,283.9999999963372,334.0999999998236)
1524 +         Nbraided_busbar_interface014p ...
     ↪ (-315.89999998339226,218.99999999633712,334.0999999998431)
1525 +         Nbraided_busbar_interface018p ...
     ↪ (-315.89999998569033,194.99999999633712,334.0999999998503)
1526 +         Nbraided_busbar_interface022p ...
     ↪ (-315.8999999879884,170.9999999963371,334.0999999998575)
1527 +         Nbraided_busbar_interface026p ...
     ↪ (-315.8999999942123,105.99999999633707,334.099999999877)
1528 +         Nbraided_busbar_interface030p ...
     ↪ (-315.8999999947518,81.99962084088011,334.0999999998842)
1529 +         Nbraided_busbar_interface034p ...
     ↪ (-315.89999999880837,57.99999999633704,334.0999999998914)
1530 +         hole rect ...
     ↪ (-299.14912108776,154.99969853018436,333.09999999981636,-295.1494921179811,234.999717
1531
1532
1533 * Connecting internal plane nodes to actual nodes
1534 .equiv Noutput_busbar_interface Noutput_busbar_interfacep
1535 .equiv Nbraided_busbar_interface002 Nbraided_busbar_interface002p
1536 .equiv Nbraided_busbar_interface006 Nbraided_busbar_interface006p
1537 .equiv Nbraided_busbar_interface010 Nbraided_busbar_interface010p
1538 .equiv Nbraided_busbar_interface014 Nbraided_busbar_interface014p
1539 .equiv Nbraided_busbar_interface018 Nbraided_busbar_interface018p
1540 .equiv Nbraided_busbar_interface022 Nbraided_busbar_interface022p
1541 .equiv Nbraided_busbar_interface026 Nbraided_busbar_interface026p
1542 .equiv Nbraided_busbar_interface030 Nbraided_busbar_interface030p
1543 .equiv Nbraided_busbar_interface034 Nbraided_busbar_interface034p
1544
1545 GHeatsink_SM1 x1=-317.15 y1=-2.899999999999977 z1=48.10000000000002 ...
     ↪ x2=-317.15 y2=483.0 z2=48.10000000000002
1546 +         x3=-317.15 y3=483.0 z3=286.19999999999993
1547 +         thick=27.0 seg1=20 seg2=10
1548 +         sigma=35000.0
1549
1550 GSM3-plane001 x1=164.5 y1=477.5 z1=30.4999999999999 x2=164.5 y2=25.5 ...
     ↪ z2=30.4999999999999
1551 +         x3=164.5 y3=25.5 z3=142.6
1552 +         thick=3.0 seg1=15 seg2=7
1553 +         NSM3-_IGBTinterfacep (165.99999999999997,444.0,137.59999999999994)
1554 +         NSM3-_IGBTinterface001p ...
     ↪ (165.99999999999997,397.99999999999994,137.5999999999999)
1555 +         NSM3-_IGBTinterface002p ...
     ↪ (165.99999999999997,331.0,137.5999999999999)
1556 +         NSM3-_IGBTinterface003p ...
     ↪ (165.99999999999997,285.0,137.59999999999988)
1557 +         NSM3-_IGBTinterface004p ...
     ↪ (165.99999999999997,218.00000000000006,137.59999999999988)
```

```
1558 +          NSM3-_IGBTinterface005p ...
         ↪ (165.99999999999994,172.00000000000006,137.59999999999988)
1559 +          NSM3-_IGBTinterface006p ...
         ↪ (165.99999999999994,105.00000000000006,137.59999999999985)
1560 +          NSM3-_IGBTinterface007p ...
         ↪ (165.99999999999994,59.00000000000006,137.59999999999985)
1561 +          NDCinterface020p ...
         ↪ (164.49999999999994,35.50000000000006,30.499999999999876)
1562 +          NDCinterface021p ...
         ↪ (164.49999999999997,131.50000000000006,30.499999999999826)
1563 +          NDCinterface024p (164.5,419.5,30.499999999999908)
1564 +          NDCinterface023p (164.49999999999997,323.5,30.49999999999988)
1565 +          NDCinterface022p ...
         ↪ (164.49999999999997,227.50000000000003,30.499999999999854)
1566 +          hole circle (166.0,444.00000000000017,108.1,15.0)
1567 +          hole circle ...
         ↪ (165.99999999999997,398.0000000000001,108.09999999999998,15.0)
1568 +          hole circle ...
         ↪ (165.99999999999997,331.0000000000001,108.09999999999998,15.0)
1569 +          hole circle ...
         ↪ (165.99999999999997,285.0000000000001,108.09999999999997,15.0)
1570 +          hole circle ...
         ↪ (165.99999999999997,218.0000000000001,108.09999999999997,15.0)
1571 +          hole circle ...
         ↪ (165.99999999999997,172.00000000000006,108.09999999999997,15.0)
1572 +          hole circle ...
         ↪ (165.99999999999994,105.00000000000006,108.09999999999995,15.0)
1573 +          hole circle ...
         ↪ (165.99999999999994,59.00000000000006,108.09999999999995,15.0)
1574
1575 * Connecting internal plane nodes to actual nodes
1576 .equiv NSM3-_IGBTinterface NSM3-_IGBTinterfacep
1577 .equiv NSM3-_IGBTinterface001 NSM3-_IGBTinterface001p
1578 .equiv NSM3-_IGBTinterface002 NSM3-_IGBTinterface002p
1579 .equiv NSM3-_IGBTinterface003 NSM3-_IGBTinterface003p
1580 .equiv NSM3-_IGBTinterface004 NSM3-_IGBTinterface004p
1581 .equiv NSM3-_IGBTinterface005 NSM3-_IGBTinterface005p
1582 .equiv NSM3-_IGBTinterface006 NSM3-_IGBTinterface006p
1583 .equiv NSM3-_IGBTinterface007 NSM3-_IGBTinterface007p
1584 .equiv NDCinterface020 NDCinterface020p
1585 .equiv NDCinterface021 NDCinterface021p
1586 .equiv NDCinterface024 NDCinterface024p
1587 .equiv NDCinterface023 NDCinterface023p
1588 .equiv NDCinterface022 NDCinterface022p
1589
1590 GSM3+plane001 x1=167.85000000000002 y1=477.5 z1=27.9999999999999 ...
         ↪ x2=167.85000000000002 y2=25.5 z2=27.9999999999999
1591 +          x3=167.85000000000002 y3=25.5 z3=113.1
1592 +          thick=3.0 seg1=15 seg2=5
1593 +          NSM3+_IGBTinterfacep ...
         ↪ (169.35000000000002,444.00000000000006,108.09999999999997)
1594 +          NSM3+_IGBTinterface001p ...
         ↪ (169.35,398.00000000000006,108.09999999999995)
1595 +          NSM3+_IGBTinterface002p (169.35,331.0,108.09999999999995)
1596 +          NSM3+_IGBTinterface003p (169.35,285.0,108.09999999999991)
1597 +          NSM3+_IGBTinterface004p ...
         ↪ (169.35,218.00000000000006,108.09999999999991)
```

```
1598 +          NSM3+_IGBTinterface005p ...
         ↪ (169.34999999999997,172.00000000000006,108.09999999999988)
1599 +          NSM3+_IGBTinterface006p ...
         ↪ (169.34999999999997,105.00000000000006,108.09999999999987)
1600 +          NSM3+_IGBTinterface007p ...
         ↪ (169.34999999999997,59.00000000000006,108.09999999999987)
1601 +          NDCinterface028p (167.85000000000002,371.5,27.99999999999997)
1602 +          NDCinterface027p (167.85,275.5,27.999999999999943)
1603 +          NDCinterface026p (167.85,179.50000000000006,27.99999999999992)
1604 +          NDCinterface025p ...
         ↪ (167.84999999999997,83.50000000000006,27.99999999999989)
1605 +          NDCinterface029p (167.85000000000002,467.5,27.999999999999996)
1606
1607 * Connecting internal plane nodes to actual nodes
1608 .equiv NSM3+_IGBTinterface NSM3+_IGBTinterfacep
1609 .equiv NSM3+_IGBTinterface001 NSM3+_IGBTinterface001p
1610 .equiv NSM3+_IGBTinterface002 NSM3+_IGBTinterface002p
1611 .equiv NSM3+_IGBTinterface003 NSM3+_IGBTinterface003p
1612 .equiv NSM3+_IGBTinterface004 NSM3+_IGBTinterface004p
1613 .equiv NSM3+_IGBTinterface005 NSM3+_IGBTinterface005p
1614 .equiv NSM3+_IGBTinterface006 NSM3+_IGBTinterface006p
1615 .equiv NSM3+_IGBTinterface007 NSM3+_IGBTinterface007p
1616 .equiv NDCinterface028 NDCinterface028p
1617 .equiv NDCinterface027 NDCinterface027p
1618 .equiv NDCinterface026 NDCinterface026p
1619 .equiv NDCinterface025 NDCinterface025p
1620 .equiv NDCinterface029 NDCinterface029p
1621
1622 GAC_busbar_plane001 x1=185.85138676039907 y1=45.49944344811725 z1=338.1 ...
         ↪ x2=305.8500000000135 y2=45.499999986950115 z2=338.0999999996726
1623 +          x3=305.8486132721504 y3=344.50055653883464 z3=338.0999999995876
1624 +          thick=10.0 seg1=10 seg2=20
1625 +          Noutput_busbar_interface001p ...
         ↪ (275.8500000143014,194.99999999138097,338.0999999997084)
1626 +          Nbraided_busbar_interface035p ...
         ↪ (224.10000002743863,331.9999999963383,338.0999999998092)
1627 +          Nbraided_busbar_interface036p ...
         ↪ (224.1000000251406,307.9999999963383,338.0999999998164)
1628 +          Nbraided_busbar_interface037p ...
         ↪ (224.10000002284255,283.9999999963384,338.0999999998236)
1629 +          Nbraided_busbar_interface038p ...
         ↪ (224.10000001661868,218.99999999633832,338.0999999998431)
1630 +          Nbraided_busbar_interface039p ...
         ↪ (224.10000001432064,194.99999999633832,338.0999999998503)
1631 +          Nbraided_busbar_interface040p ...
         ↪ (224.1000000120226,170.99999999633832,338.0999999998575)
1632 +          Nbraided_busbar_interface041p ...
         ↪ (224.10000000579868,105.99999999633826,338.099999999877)
1633 +          Nbraided_busbar_interface042p ...
         ↪ (224.1000000035007,81.99999999633826,338.0999999998842)
1634 +          Nbraided_busbar_interface043p ...
         ↪ (224.1000000012026,57.999999996338225,338.0999999998914)
1635 +          Noutput_busbar_interface002p ...
         ↪ (275.84939709091003,324.99986085084385,338.0999999996694)
1636 +          Noutput_busbar_interface003p ...
         ↪ (275.8500000143014,194.99999999138103,338.0999999997084)
1637 +          hole rect ...
         ↪ (240.85046224541998,154.9999999947308,333.09999999981636,244.8500912152012,235.0000185
```

```
1638
1639
1640 * Connecting internal plane nodes to actual nodes
1641 .equiv Noutput_busbar_interface001 Noutput_busbar_interface001p
1642 .equiv Nbraided_busbar_interface035 Nbraided_busbar_interface035p
1643 .equiv Nbraided_busbar_interface036 Nbraided_busbar_interface036p
1644 .equiv Nbraided_busbar_interface037 Nbraided_busbar_interface037p
1645 .equiv Nbraided_busbar_interface038 Nbraided_busbar_interface038p
1646 .equiv Nbraided_busbar_interface039 Nbraided_busbar_interface039p
1647 .equiv Nbraided_busbar_interface040 Nbraided_busbar_interface040p
1648 .equiv Nbraided_busbar_interface041 Nbraided_busbar_interface041p
1649 .equiv Nbraided_busbar_interface042 Nbraided_busbar_interface042p
1650 .equiv Nbraided_busbar_interface043 Nbraided_busbar_interface043p
1651 .equiv Noutput_busbar_interface002 Noutput_busbar_interface002p
1652 .equiv Noutput_busbar_interface003 Noutput_busbar_interface003p
1653
1654 GHeatsink_SM2 x1=-47.14999999999998 y1=-2.899999999999977 ...
        ↪ z1=48.10000000000002 x2=-47.14999999999998 y2=483.0 ...
        ↪ z2=48.10000000000002
1655 +          x3=-47.14999999999998 y3=483.0 z3=286.19999999999993
1656 +          thick=27.0 seg1=20 seg2=10
1657 +          sigma=35000.0
1658
1659 GHeatsink_SM3 x1=222.85000000000002 y1=-2.899999999999977 ...
        ↪ z1=48.10000000000002 x2=222.85000000000002 y2=483.0 ...
        ↪ z2=48.10000000000002
1660 +          x3=222.85000000000002 y3=483.0 z3=286.19999999999993
1661 +          thick=27.0 seg1=20 seg2=10
1662 +          sigma=35000.0
1663
1664
1665 * Node shorts
1666 .equiv NSM1+_IGBTinterface NSM1+_IGBTinterface001
1667 .equiv NSM1-_IGBTinterface NSM1-_IGBTinterface001
1668 .equiv NDCcap024 NDCcap
1669 .equiv NDCcap030 NDCcap001
1670 .equiv NDCcap036 NDCcap022
1671 .equiv NDCcap042 NDCcap023
1672 .equiv NDCcap025 NDCcap003
1673 .equiv NDCcap031 NDCcap002
1674 .equiv NDCcap037 NDCcap004
1675 .equiv NDCcap043 NDCcap021
1676 .equiv NDCcap044 NDCcap020
1677 .equiv NDCcap038 NDCcap019
1678 .equiv NDCcap032 NDCcap005
1679 .equiv NDCcap026 NDCcap006
1680 .equiv NDCcap027 NDCcap007
1681 .equiv NDCcap033 NDCcap010
1682 .equiv NDCcap039 NDCcap013
1683 .equiv NDCcap045 NDCcap018
1684 .equiv NDCcap028 NDCcap008
1685 .equiv NDCcap029 NDCcap009
1686 .equiv NDCcap035 NDCcap011
1687 .equiv NDCcap034 NDCcap012
1688 .equiv NDCcap041 NDCcap014
1689 .equiv NDCcap040 NDCcap015
1690 .equiv NDCcap047 NDCcap016
1691 .equiv NDCcap046 NDCcap017
```

```
.equiv NFHNode184 NSM2interface005
.equiv NFHNode171 NSM2interface
.equiv NFHNode181 NSM2interface006
.equiv NFHNode169 NSM2interface001
.equiv NFHNode178 NSM2interface007
.equiv NFHNode167 NSM2interface002
.equiv NFHNode175 NSM2interface008
.equiv NFHNode161 NSM2interface003
.equiv NFHNode141 NSM2interface009
.equiv NFHNode142 NSM2interface004
.equiv NIGBTinterface016 NIGBTinterface018
.equiv NIGBTinterface017 NIGBTinterface019
.equiv NIGBTinterface020 NIGBTinterface022
.equiv NIGBTinterface021 NIGBTinterface023
.equiv NIGBTinterface024 NIGBTinterface026
.equiv NIGBTinterface025 NIGBTinterface027
.equiv NIGBTinterface028 NIGBTinterface030
.equiv NIGBTinterface029 NIGBTinterface031
.equiv NSM1+_IGBTinterface002 NSM1+_IGBTinterface003
.equiv NSM1-_IGBTinterface002 NSM1-_IGBTinterface003
.equiv NSM1+_IGBTinterface004 NSM1+_IGBTinterface005
.equiv NSM1-_IGBTinterface004 NSM1-_IGBTinterface005
.equiv NSM1+_IGBTinterface006 NSM1+_IGBTinterface007
.equiv NSM1-_IGBTinterface006 NSM1-_IGBTinterface007
.equiv NSM1_braidedBB1_091 NSM1_braidedBB1_070
.equiv NSM1_braidedBB1_070 NSM1_braidedBB1_077
.equiv NSM1_braidedBB1_077 NSM1_braidedBB1_084
.equiv NSM1_braidedBB1_084 NSM1_braidedBB1_028
.equiv NSM1_braidedBB1_028 NSM1_braidedBB1_035
.equiv NSM1_braidedBB1_035 NSM1_braidedBB1_042
.equiv NSM1_braidedBB1_042 NSM1_braidedBB1_049
.equiv NSM1_braidedBB1_049 NSM1_braidedBB1_056
.equiv NSM1_braidedBB1_056 NSM1_braidedBB1_063
.equiv NSM1_braidedBB1_063 NSM1_braidedBB1_014
.equiv NSM1_braidedBB1_014 NSM1_braidedBB1_021
.equiv NSM1_braidedBB2_091 NSM1_braidedBB2_070
.equiv NSM1_braidedBB2_070 NSM1_braidedBB2_077
.equiv NSM1_braidedBB2_077 NSM1_braidedBB2_084
.equiv NSM1_braidedBB2_084 NSM1_braidedBB2_028
.equiv NSM1_braidedBB2_028 NSM1_braidedBB2_035
.equiv NSM1_braidedBB2_035 NSM1_braidedBB2_042
.equiv NSM1_braidedBB2_042 NSM1_braidedBB2_049
.equiv NSM1_braidedBB2_049 NSM1_braidedBB2_056
.equiv NSM1_braidedBB2_056 NSM1_braidedBB2_063
.equiv NSM1_braidedBB2_063 NSM1_braidedBB2_014
.equiv NSM1_braidedBB2_014 NSM1_braidedBB2_021
.equiv NSM1_braidedBB3_090 NSM1_braidedBB3_069
.equiv NSM1_braidedBB3_069 NSM1_braidedBB3_076
.equiv NSM1_braidedBB3_076 NSM1_braidedBB3_083
.equiv NSM1_braidedBB3_083 NSM1_braidedBB3_027
.equiv NSM1_braidedBB3_027 NSM1_braidedBB3_034
.equiv NSM1_braidedBB3_034 NSM1_braidedBB3_041
.equiv NSM1_braidedBB3_041 NSM1_braidedBB3_048
.equiv NSM1_braidedBB3_048 NSM1_braidedBB3_055
.equiv NSM1_braidedBB3_055 NSM1_braidedBB3_062
.equiv NSM1_braidedBB3_062 NSM1_braidedBB3_013
.equiv NSM1_braidedBB3_013 NSM1_braidedBB3_020
.equiv NFHNode444 Noutput_busbar_interface
```

```
.equiv NSM1_braidedBB1_061 NSM1_braidedBB1_068
.equiv NSM1_braidedBB1_068 NSM1_braidedBB1_019
.equiv NSM1_braidedBB1_019 NSM1_braidedBB1_026
.equiv NSM1_braidedBB1_026 Nbraided_busbar_interface010
.equiv NSM1_braidedBB1_033 NSM1_braidedBB1_040
.equiv NSM1_braidedBB1_040 NSM1_braidedBB1_047
.equiv NSM1_braidedBB1_047 NSM1_braidedBB1_054
.equiv NSM1_braidedBB1_054 Nbraided_busbar_interface006
.equiv NSM1_braidedBB1_ NSM1_braidedBB1_075
.equiv NSM1_braidedBB1_075 NSM1_braidedBB1_082
.equiv NSM1_braidedBB1_082 NSM1_braidedBB1_089
.equiv NSM1_braidedBB1_089 Nbraided_busbar_interface002
.equiv NSM1_braidedBB2_ NSM1_braidedBB2_075
.equiv NSM1_braidedBB2_075 NSM1_braidedBB2_082
.equiv NSM1_braidedBB2_082 NSM1_braidedBB2_089
.equiv NSM1_braidedBB2_089 Nbraided_busbar_interface014
.equiv NSM1_braidedBB2_033 NSM1_braidedBB2_040
.equiv NSM1_braidedBB2_040 NSM1_braidedBB2_047
.equiv NSM1_braidedBB2_047 NSM1_braidedBB2_054
.equiv NSM1_braidedBB2_054 Nbraided_busbar_interface018
.equiv NSM1_braidedBB2_061 NSM1_braidedBB2_068
.equiv NSM1_braidedBB2_068 NSM1_braidedBB2_019
.equiv NSM1_braidedBB2_019 NSM1_braidedBB2_026
.equiv NSM1_braidedBB2_026 Nbraided_busbar_interface022
.equiv NSM1_braidedBB3_095 NSM1_braidedBB3_074
.equiv NSM1_braidedBB3_074 NSM1_braidedBB3_081
.equiv NSM1_braidedBB3_081 NSM1_braidedBB3_088
.equiv NSM1_braidedBB3_088 Nbraided_busbar_interface026
.equiv NSM1_braidedBB3_032 NSM1_braidedBB3_039
.equiv NSM1_braidedBB3_039 NSM1_braidedBB3_046
.equiv NSM1_braidedBB3_046 NSM1_braidedBB3_053
.equiv NSM1_braidedBB3_053 Nbraided_busbar_interface030
.equiv NSM1_braidedBB3_060 NSM1_braidedBB3_067
.equiv NSM1_braidedBB3_067 NSM1_braidedBB3_018
.equiv NSM1_braidedBB3_018 NSM1_braidedBB3_025
.equiv NSM1_braidedBB3_025 Nbraided_busbar_interface034
.equiv NFHNode452 NDCinterface005
.equiv NDCinterface006 NFHNode456
.equiv NFHNode460 NDCinterface007
.equiv NFHNode464 NDCinterface008
.equiv NFHNode468 NDCinterface009
.equiv NFHNode455 NFHNode453
.equiv NFHNode457 NFHNode459
.equiv NFHNode467 NFHNode465
.equiv NFHNode463 NFHNode461
.equiv NFHNode471 NFHNode469
.equiv NFHNode472 NSM1_DCinterface002
.equiv NSM1_DCinterface003 NFHNode476
.equiv NSM1_DCinterface004 NFHNode480
.equiv NSM1_DCinterface001 NFHNode484
.equiv NSM1_DCinterface NFHNode488
.equiv NFHNode473 NFHNode475
.equiv NFHNode477 NFHNode479
.equiv NFHNode487 NFHNode485
.equiv NFHNode483 NFHNode481
.equiv NFHNode491 NFHNode489
.equiv NSM3+_IGBTinterface NSM3+_IGBTinterface001
.equiv NSM3-_IGBTinterface NSM3-_IGBTinterface001
```

```
.equiv NSM3+_IGBTinterface002 NSM3+_IGBTinterface003
.equiv NSM3-_IGBTinterface002 NSM3-_IGBTinterface003
.equiv NSM3+_IGBTinterface004 NSM3+_IGBTinterface005
.equiv NSM3-_IGBTinterface004 NSM3-_IGBTinterface005
.equiv NSM3+_IGBTinterface006 NSM3+_IGBTinterface007
.equiv NSM3-_IGBTinterface006 NSM3-_IGBTinterface007
.equiv NFHNode518 NDCinterface029
.equiv NDCinterface028 NFHNode522
.equiv NFHNode526 NDCinterface027
.equiv NFHNode530 NDCinterface026
.equiv NFHNode534 NDCinterface025
.equiv NFHNode521 NFHNode519
.equiv NFHNode523 NFHNode525
.equiv NFHNode533 NFHNode531
.equiv NFHNode529 NFHNode527
.equiv NFHNode537 NFHNode535
.equiv NFHNode538 NDCinterface024
.equiv NDCinterface023 NFHNode542
.equiv NDCinterface022 NFHNode546
.equiv NDCinterface021 NFHNode550
.equiv NDCinterface020 NFHNode554
.equiv NFHNode539 NFHNode541
.equiv NFHNode543 NFHNode545
.equiv NFHNode553 NFHNode551
.equiv NFHNode549 NFHNode547
.equiv NFHNode557 NFHNode555
.equiv NSM1interface005 NFHNode454
.equiv NSM1interface001 NFHNode474
.equiv NSM1interface006 NFHNode458
.equiv NFHNode478 NSM1interface002
.equiv NSM1interface007 NFHNode462
.equiv NSM1interface003 NFHNode482
.equiv NSM1interface008 NFHNode466
.equiv NSM1interface004 NFHNode486
.equiv NFHNode470 NSM1interface009
.equiv NFHNode490 NSM1interface
.equiv NFHNode520 NSM3interface009
.equiv NFHNode540 NSM3interface004
.equiv NFHNode524 NSM3interface008
.equiv NFHNode544 NSM3interface003
.equiv NFHNode528 NSM3interface007
.equiv NFHNode548 NSM3interface002
.equiv NFHNode532 NSM3interface006
.equiv NFHNode552 NSM3interface001
.equiv NFHNode536 NSM3interface005
.equiv NFHNode556 NSM3interface
.equiv NSM3_braidedBB1_090 NSM3_braidedBB1_069
.equiv NSM3_braidedBB1_069 NSM3_braidedBB1_076
.equiv NSM3_braidedBB1_076 NSM3_braidedBB1_083
.equiv NSM3_braidedBB1_083 NSM3_braidedBB1_027
.equiv NSM3_braidedBB1_027 NSM3_braidedBB1_034
.equiv NSM3_braidedBB1_034 NSM3_braidedBB1_041
.equiv NSM3_braidedBB1_041 NSM3_braidedBB1_048
.equiv NSM3_braidedBB1_048 NSM3_braidedBB1_055
.equiv NSM3_braidedBB1_055 NSM3_braidedBB1_062
.equiv NSM3_braidedBB1_062 NSM3_braidedBB1_013
.equiv NSM3_braidedBB1_013 NSM3_braidedBB1_020
.equiv NSM3_braidedBB2_090 NSM3_braidedBB2_069
```

```
.equiv NSM3_braidedBB2_069 NSM3_braidedBB2_076
.equiv NSM3_braidedBB2_076 NSM3_braidedBB2_083
.equiv NSM3_braidedBB2_083 NSM3_braidedBB2_027
.equiv NSM3_braidedBB2_027 NSM3_braidedBB2_034
.equiv NSM3_braidedBB2_034 NSM3_braidedBB2_041
.equiv NSM3_braidedBB2_041 NSM3_braidedBB2_048
.equiv NSM3_braidedBB2_048 NSM3_braidedBB2_055
.equiv NSM3_braidedBB2_055 NSM3_braidedBB2_062
.equiv NSM3_braidedBB2_062 NSM3_braidedBB2_013
.equiv NSM3_braidedBB2_013 NSM3_braidedBB2_020
.equiv NSM3_braidedBB3_090 NSM3_braidedBB3_069
.equiv NSM3_braidedBB3_069 NSM3_braidedBB3_076
.equiv NSM3_braidedBB3_076 NSM3_braidedBB3_083
.equiv NSM3_braidedBB3_083 NSM3_braidedBB3_027
.equiv NSM3_braidedBB3_027 NSM3_braidedBB3_034
.equiv NSM3_braidedBB3_034 NSM3_braidedBB3_041
.equiv NSM3_braidedBB3_041 NSM3_braidedBB3_048
.equiv NSM3_braidedBB3_048 NSM3_braidedBB3_055
.equiv NSM3_braidedBB3_055 NSM3_braidedBB3_062
.equiv NSM3_braidedBB3_062 NSM3_braidedBB3_013
.equiv NSM3_braidedBB3_013 NSM3_braidedBB3_020
.equiv NFHNode784 Noutput_busbar_interface001
.equiv NSM3_braidedBB1_060 NSM3_braidedBB1_067
.equiv NSM3_braidedBB1_067 NSM3_braidedBB1_018
.equiv NSM3_braidedBB1_018 NSM3_braidedBB1_025
.equiv NSM3_braidedBB1_025 Nbraided_busbar_interface037
.equiv NSM3_braidedBB1_032 NSM3_braidedBB1_039
.equiv NSM3_braidedBB1_039 NSM3_braidedBB1_046
.equiv NSM3_braidedBB1_046 NSM3_braidedBB1_053
.equiv NSM3_braidedBB1_053 Nbraided_busbar_interface036
.equiv NSM3_braidedBB1_095 NSM3_braidedBB1_074
.equiv NSM3_braidedBB1_074 NSM3_braidedBB1_081
.equiv NSM3_braidedBB1_081 NSM3_braidedBB1_088
.equiv NSM3_braidedBB1_088 Nbraided_busbar_interface035
.equiv NSM3_braidedBB2_095 NSM3_braidedBB2_074
.equiv NSM3_braidedBB2_074 NSM3_braidedBB2_081
.equiv NSM3_braidedBB2_081 NSM3_braidedBB2_088
.equiv NSM3_braidedBB2_088 Nbraided_busbar_interface038
.equiv NSM3_braidedBB2_032 NSM3_braidedBB2_039
.equiv NSM3_braidedBB2_039 NSM3_braidedBB2_046
.equiv NSM3_braidedBB2_046 NSM3_braidedBB2_053
.equiv NSM3_braidedBB2_053 Nbraided_busbar_interface039
.equiv NSM3_braidedBB2_060 NSM3_braidedBB2_067
.equiv NSM3_braidedBB2_067 NSM3_braidedBB2_018
.equiv NSM3_braidedBB2_018 NSM3_braidedBB2_025
.equiv NSM3_braidedBB2_025 Nbraided_busbar_interface040
.equiv NSM3_braidedBB3_095 NSM3_braidedBB3_074
.equiv NSM3_braidedBB3_074 NSM3_braidedBB3_081
.equiv NSM3_braidedBB3_081 NSM3_braidedBB3_088
.equiv NSM3_braidedBB3_088 Nbraided_busbar_interface041
.equiv NSM3_braidedBB3_032 NSM3_braidedBB3_039
.equiv NSM3_braidedBB3_039 NSM3_braidedBB3_046
.equiv NSM3_braidedBB3_046 NSM3_braidedBB3_053
.equiv NSM3_braidedBB3_053 Nbraided_busbar_interface042
.equiv NSM3_braidedBB3_060 NSM3_braidedBB3_067
.equiv NSM3_braidedBB3_067 NSM3_braidedBB3_018
.equiv NSM3_braidedBB3_018 NSM3_braidedBB3_025
.equiv NSM3_braidedBB3_025 Nbraided_busbar_interface043
```

```
.equiv NFHNode443 NFHNode446
.equiv NFHNode812 NFHNode814
.equiv NFHNode447 NFHNode815
*.equiv NSM3+_IGBTinterface002 NSM3+_IGBTinterface003
.equiv NSM3+_IGBTinterface003 NSM3_braidedBB1_041
.equiv NSM3_braidedBB2_041 NSM3+_IGBTinterface004
*.equiv NSM3+_IGBTinterface004 NSM3+_IGBTinterface005
*.equiv NSM3+_IGBTinterface006 NSM3+_IGBTinterface007
.equiv NSM3+_IGBTinterface007 NSM3_braidedBB3_041
.equiv Noutput_busbar_interface003 NFHNode813

* Ports

.external NSM1_braidedBB1_035 NSM1-_IGBTinterface002
.external NSM1_braidedBB2_035 NSM1-_IGBTinterface004
.external NSM1_braidedBB3_034 NSM1-_IGBTinterface006

.freq fmin=10000.0 fmax=10000.0 ndec=1.0

.end
```

A.2 Skin Depth Calculations

To analyse the testing results in detail, it was though to visualise the current flow in the system. The skin depth is calculated using the equation below:

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}}$$

where:

- δ is the skin depth,
- f is the frequency (in Hz),
- μ is the permeability (in H/m) - (μ_r = 0.999991 - For Copper and μ_r = 1.00002 - For Aluminum),
- σ is the conductivity (in S/m) - (58000 S/m - For Copper and 35000 S/m - For Aluminum)

Parameter	**Value**
μ_0 (H/m)	1.25664×10^{-6}
μ_r (Copper)	0.999991
μ_r (Aluminium)	1.00002

Table A.1: Magnetic Permeability Parameters

Input Data	**Value**
σ (Copper) (1/(m·Ω))	5.80×10^7
σ (Aluminium) (1/(m·Ω))	3.50×10^7
Frequency (Hz)	1.00×10^4
Segment Width (m)	Custom for each unit
Width Ratio (r_w) or Height Ratio (r_h)	Depends on segment width or height

Table A.2: Electrical and Geometrical Input Data

The skin depth comes out to be $\delta = 0.660857905\ mm$ and $\delta = 0.850710448\ mm$ for Copper and Aluminium respectively.

There is a good correlation to the segmentation and skin depth given in the user manual [33] for fine tuning of the model. The rule of thumb says to keep the discretization such that the width of the smallest filament is roughly equal to the skin depth.

For the segments, it is divided along the width and height into smaller filaments to emulate the skin effect.

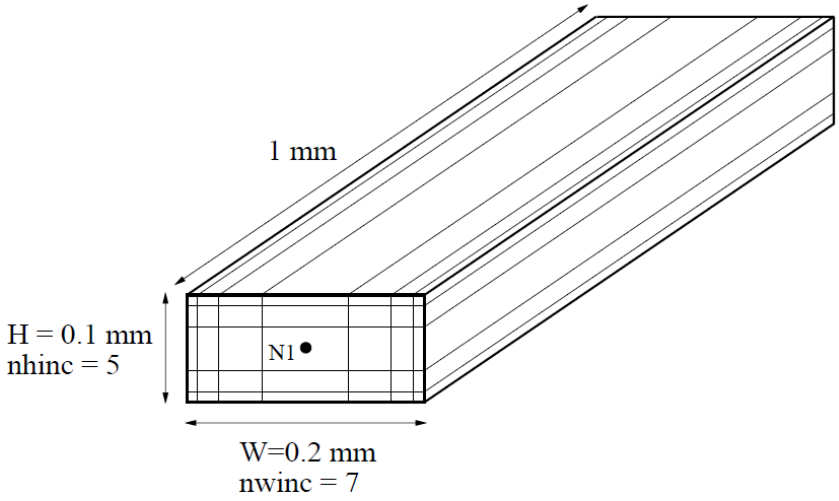


Figure A.1: Segment Discretization [33]

There are two elements to form this discretization, *nhinc* and *nwinc* are the number of filaments along the height and width and *rh* and *rw* is the ratio of adjacent filament along the height and width respectively.
Following is an example of the filament details based on the width of the segment calculated for Copper and Aluminum:

$$SmallestFilament = \frac{SegmentWidth}{sum(Discretizationwidthsequence)}$$

Segment Width (w)	**nwinc**	**rw**	**Discretization width sequence**	**Smallest Filament (Nearly equal to skin depth)**
Copper Segment - 6 mm	3	7	1, 7, 1	$6.67E-04$
Aluminium Segment - 10 mm	3	9	1, 9, 1	$9.09E-04$

Table A.3: Example calculations of width variables

The same values can be computed for the height to match the smallest filament length equivalent to skin depth. This calculation shall provide a good reference accurately modeling the skin depth in segments. However, for uniform conductive plane the width changes with internal node creation and is not taken into the scope of the project.

Appendix B Optimization Tool

```
clc; clear; close all;

% File input and output
inputFileOriginal = ...
    ↪ 'C:\Users\poohg\OneDrive\Desktop\Master_Thesis_Semester\KK Wind ...
    ↪ Project\Optimization Techniques\GA Optimization full ...
    ↪ system\Step4_Introducing_Full_Model\DCneg_SM1_1filament_GA_full_model_AL.inp'; ...
    ↪ % Updated path
outputFile = 'C:\Users\poohg\OneDrive\Desktop\Master_Thesis_Semester\KK ...
    ↪ Wind Project\Optimization Techniques\GA Optimization full ...
    ↪ system\Step4_Introducing_Full_Model\Modified_Position_GA_full_model.inp'; ...
    ↪ % Updated path and file name

% Number of workers to use for parallel processing
numWorkers = 6; % Modify this value to define the number of workers

% Initialize Parallel Pool (if not already open)
if isempty(gcp('nocreate'))
    parpool(numWorkers);
end

% FastHenry COM object initialization
try
    fh = actxserver('FastHenry2.Document');
    disp('FastHenry2 Automation Object created successfully.');
catch ME
    fprintf('Error initializing FastHenry2: %s\n', ME.message);
    return;
end

% Validate file
if ~isfile(inputFileOriginal)
    fprintf('Input file not found: %s\n', inputFileOriginal);
    return;
end


%Based on node connections y min = 45.5 and y max = 344.5, x min = -315.9
% xmax = -264.15

% Defining lower and upper bounds


% Dimensions - These are the maximum possible dimensions of section 1
% width, length, radius = [51.75, 75, 51.75]

width = 20;
length = 20;
radius = 10;

%Section Defination

%Section 1 -

sec1_lb = [-315.9 , 262 , 0 , 0 , -315.9 + 2*radius , 262 + radius , 0];
sec1_ub = [-264.15 - 1.1*width , 340 - 1.1*length , width , length , ...
    ↪ -264.15 - 2*radius , 340 - 2*radius , radius];
```

```
50
51 %Section 2 -
52
53 sec2_lb = [-315.9, 143, 0, 0, -315.9 + radius, 143 + radius, 0];
54 sec2_ub = [-264.15 - 1.1*width, 247 - 1.1*length, width, length, -264.15 ...
       ↪ - radius, 247 - radius, radius];
55
56 %Section 3 -
57
58 sec3_lb = [-315.9, 45.5+ 1.1*length, 0, 0, -315.9 + 2*radius, 45.5 + ...
       ↪ 2*radius, 0];
59 sec3_ub = [-264.15 - 1.1*width, 128 - 1.1*length, width, length, -264.15 ...
       ↪ - 2*radius, 128 - radius, radius];
60
61 % Lower Bound and Upper Bound Varibles
62
63 lb_1 = repmat(sec1_lb,1,2);
64 lb_2 = repmat(sec2_lb,1,2);
65 lb_3 = repmat(sec3_lb,1,2);
66
67 ub_1 = repmat(sec1_ub,1,2);
68 ub_2 = repmat(sec2_ub,1,2);
69 ub_3 = repmat(sec3_ub,1,2);
70
71 % Number of design variables:
72
73 varible_rectangle = 4; % Number of variables for rectangular hole
74 variable_circle = 3; % Number of variables for circular hole
75
76 hole_rectangle = 2; % Defines rectangular holes per section
77 hole_circle = 2; % Defines circular holes per section
78
79 sections = 3; % Number of sections
80
81 existance = hole_rectangle*sections + hole_circle*sections;
82 e_lb = zeros(1,existance);
83 e_ub = ones(1,existance);
84
85 % Defining number of variables
86 nVars = varible_rectangle*hole_rectangle*sections + ...
       ↪ variable_circle*hole_circle*sections + 1 + 1 + numel(e_lb);
87 %[x_rect,y_rect, width, height, x_circ, y_circ, radius]*2(Two circles and
88 %Two rectangles per section)*3(Three sections) + Movement of output busbar
89 %+ Distance of output busbar from DC link + Existance variables
90
91 lb = [lb_1,lb_2,lb_3,70.00,30.00,e_lb];
92 ub = [ub_1,ub_2,ub_3,320.00,300.00,e_ub];
93
94 % y distance for different connection points
95 % and z distance for different distance from DC link have been added
96 % and Hole Existance variable
97
98 % Define GA options
99
100 % Define integer constraints (all variables should be integers)
101 first_integer_var = nVars - existance + 1;
102 IntCon = first_integer_var:nVars; % Integer constraints (only existance ...
       ↪ variables)
```

```
103
104 populationSize = 10 ; % EliteCount calculation defined separately
105 eliteCount = ceil(0.05 * populationSize); % Top 2% as elite
106
107 % Define the initial population range
108 initialPopulationRange = [lb; ub];
109
110 options = optimoptions('ga', ...
111     'PopulationSize', populationSize, ...
112     'MaxGenerations', 10, ...
113     'CrossoverFraction', 0.8, ...
114     'MutationFcn', @mutationadaptfeasible, ...
115     'Display', 'iter', ...
116     'PlotFcn', [], ...
117     'StallGenLimit', 3, ... % Increased to prevent premature stopping
118     'OutputFcn', @gaOutputFcn, ...
119     'UseParallel', true, ...
120     'EliteCount', eliteCount, ...
121     'CreationFcn', @gacreationuniformint, ... % Use uniform creation ...
        ↪ function
122     'InitialPopulationRange', initialPopulationRange); % Set initial ...
        ↪ population range'); % Keep top 2% of individuals
123
124 tic;
125
126 % Run the genetic algorithm
127 [x_opt, fval] = ga(@busbarFitnessWithPenalty, nVars, [], [], [], [], lb, ...
    ↪ ub, [], IntCon, options);
128
129 toc;
130
131 disp('Optimal cutout parameters:');
132 disp(x_opt);
133 disp('Optimal asymmetry measure:');
134 disp(fval);
135
136 % Save the best configuration to a separate file
137 bestFile = 'C:\Users\poohg\OneDrive\Desktop\Master_Thesis_Semester\KK ...
    ↪ Wind Project\Optimization Techniques\GA Optimization full ...
    ↪ system\Step4_Introducing_Full_Model\Best_cutout_combination.inp';
138 saveBestDesign(bestFile, x_opt, IntCon);
139
140 % Calculate percentage imbalance for the best combination
141 [imbalance, percentage_imbalance, errorMessage,Z, Z_omega] = ...
    ↪ busbarFitness(x_opt);
142 disp('Percentage Imbalance for the Best Combination:');
143 disp(percentage_imbalance);
144 disp('Impedance Matrix for the Best Combination $(R+jL)$:');
145 disp(Z);
146 disp('Impedance Matrix for the Best Combination $(R+jwL)$:');
147 disp(Z_omega);
148
149 % Single Frequency SPICE Model Generation
150 generateSpiceNetlist('C:\Users\poohg\OneDrive\Desktop\Master_Thesis_Semester\KK ...
    ↪ Wind Project\Optimization Techniques\GA Optimization full ...
    ↪ system\Step4_Introducing_Full_Model\Zc.mat', ...
    ↪ 'SingleFrequency.cir', ...
    ↪ 'C:\Users\poohg\OneDrive\Desktop\Master_Thesis_Semester\KK Wind ...
```

```
    ↪ Project\Optimization Techniques\GA Optimization full ...
    ↪ system\Step2_SPICE_Model_Integration\MakeLcircuit.c', ...
    ↪ 'C:\Users\poohg\OneDrive\Desktop\Master_Thesis_Semester\KK Wind ...
    ↪ Project\Optimization Techniques\GA Optimization full ...
    ↪ system\Step2_SPICE_Model_Integration\cmplx.h')
fprintf('SPICE netlist successfully generated')


%% Introducing Constraint penalty

function [total_imbalance, imbalance, penalties] = ...
    ↪ busbarFitnessWithPenalty(x)
    % Define busbar boundaries for each section
    busbar_bounds = [
        -315.9, -264.15, 262, 340; % Section 1
        -315.9, -264.15, 143, 247; % Section 2
        -315.9, -264.15, 45.5, 128; % Section 3
    ];

    % Define penalty constants
    k_rect = 1000; % Penalty constant for rectangular hole
    k_circ = 1000; % Penalty constant for circular hole
    k_overlap = 10000; % Penalty constant for overlap
    k_diversity = 1000; % Penalty constant for diversity

    % Function to calculate gradual penalty for rectangular hole
    function penalty = gradual_rect_penalty(x, y, width, height, bounds)
        penalty = 0;
        if x < bounds(1)
            penalty = penalty + k_rect * (bounds(1) - x)^2;
        end
        if (x + width) > bounds(2)
            penalty = penalty + k_rect * ((x + width) - bounds(2))^2;
        end
        if y < bounds(3)
            penalty = penalty + k_rect * (bounds(3) - y)^2;
        end
        if (y + height) > bounds(4)
            penalty = penalty + k_rect * ((y + height) - bounds(4))^2;
        end
    end

    % Function to calculate gradual penalty for circular hole
    function penalty = gradual_circ_penalty(x, y, radius, bounds)
        penalty = 0;
        if (x - radius) < bounds(1)
            penalty = penalty + k_circ * (bounds(1) - (x - radius))^2;
        end
        if (x + radius) > bounds(2)
            penalty = penalty + k_circ * ((x + radius) - bounds(2))^2;
        end
        if (y - radius) < bounds(3)
            penalty = penalty + k_circ * (bounds(3) - (y - radius))^2;
        end
        if (y + radius) > bounds(4)
            penalty = penalty + k_circ * ((y + radius) - bounds(4))^2;
        end
    end
```

```
203
204     % Function to calculate gradual penalty for hole overlap
205     function penalty = gradual_overlap_penalty(rect_x, rect_y, ...
            ↪ rect_width, rect_height, circ_x, circ_y, circ_radius)
206         penalty = 0;
207         rect_x_max = rect_x + rect_width;
208         rect_y_max = rect_y + rect_height;
209         circ_x_min = circ_x - circ_radius;
210         circ_x_max = circ_x + circ_radius;
211         circ_y_min = circ_y - circ_radius;
212         circ_y_max = circ_y + circ_radius;
213         if rect_x < circ_x_max && rect_x_max > circ_x_min && rect_y < ...
                ↪ circ_y_max && rect_y_max > circ_y_min
214             overlap_area = max(0, min(rect_x_max, circ_x_max) - ...
                    ↪ max(rect_x, circ_x_min)) * ...
215                            max(0, min(rect_y_max, circ_y_max) - ...
                                ↪ max(rect_y, circ_y_min));
216             penalty = k_overlap * overlap_area^2;
217         end
218     end
219
220     % Calculate penalties for all holes in all sections
221     rect_penalty = 0;
222     circ_penalty = 0;
223     overlap_penalty = 0;
224
225     for i = 1:3 % Three sections
226         bounds = busbar_bounds(i, :);
227         rect_penalty = rect_penalty + ...
                ↪ gradual_rect_penalty(x((i-1)*14+1), x((i-1)*14+2), ...
                ↪ x((i-1)*14+3), x((i-1)*14+4), bounds);
228         circ_penalty = circ_penalty + ...
                ↪ gradual_circ_penalty(x((i-1)*14+5), x((i-1)*14+6), ...
                ↪ x((i-1)*14+7), bounds);
229         overlap_penalty = overlap_penalty + ...
                ↪ gradual_overlap_penalty(x((i-1)*14+1), x((i-1)*14+2), ...
                ↪ x((i-1)*14+3), x((i-1)*14+4), x((i-1)*14+5), ...
                ↪ x((i-1)*14+6), x((i-1)*14+7));
230
231         rect_penalty = rect_penalty + ...
                ↪ gradual_rect_penalty(x((i-1)*14+8), x((i-1)*14+9), ...
                ↪ x((i-1)*14+10), x((i-1)*14+11), bounds);
232         circ_penalty = circ_penalty + ...
                ↪ gradual_circ_penalty(x((i-1)*14+12), x((i-1)*14+13), ...
                ↪ x((i-1)*14+14), bounds);
233         overlap_penalty = overlap_penalty + ...
                ↪ gradual_overlap_penalty(x((i-1)*14+8), x((i-1)*14+9), ...
                ↪ x((i-1)*14+10), x((i-1)*14+11), x((i-1)*14+12), ...
                ↪ x((i-1)*14+13), x((i-1)*14+14));
234     end
235
236     % Diversity penalty using distances
237     global state;
238     if isempty(state) || ¬isfield(state, 'Population')
239         diversity_penalty_value = 0; % No penalty if no population data
240     else
241         % Compute pairwise distances between current solution and population
```

```
242         distances = pdist2(x, state.Population); % Compute distances ...
                ↪ from x to all other individuals
243         distances(distances == 0) = inf; % Ignore self-distance ...
                ↪ (distance to itself is 0)
244         min_distance = min(distances); % Smallest nonzero distance
245 
246         % Define a threshold for diversity
247         diversity_threshold = 10; % Minimum required diversity distance
248 
249         % Apply penalty if min_distance is too small
250         if min_distance < diversity_threshold
251             diversity_penalty_value = k_diversity / (1 + min_distance); ...
                    ↪ % Larger penalty for closer solutions
252         else
253             diversity_penalty_value = 0; % No penalty if sufficiently ...
                    ↪ diverse
254         end
255     end
256 
257     % Total penalty
258     penalties = round(rect_penalty + circ_penalty + overlap_penalty + ...
            ↪ diversity_penalty_value, 2);
259 
260     % Compute original imbalance score
261     imbalance = busbarFitness(x);
262 
263     % Apply penalty to fitness function
264     total_imbalance = imbalance + penalties;
265 end
266 
267 
268 
269 %% Fitness Function
270 function [imbalance, percentage_imbalance, errorMessage,Z, Z_omega] = ...
        ↪ busbarFitness(x)
271     % Define constants
272         inputFileOriginal = ...
                ↪ 'C:\Users\poohg\OneDrive\Desktop\Master_Thesis_Semester\KK ...
                ↪ Wind Project\Optimization Techniques\GA Optimization full ...
                ↪ system\Step4_Introducing_Full_Model\DCneg_SM1_1filament_GA_full_model_AL.inp';
                ↪ % Updated path
273         outputFile = ...
                ↪ 'C:\Users\poohg\OneDrive\Desktop\Master_Thesis_Semester\KK ...
                ↪ Wind Project\Optimization Techniques\GA Optimization full ...
                ↪ system\Step4_Introducing_Full_Model\Modified_Position_GA_full_model.inp'; ...
                ↪ % Updated path and file name
274 
275     targetFrequency = 10000; % Target frequency (Hz)
276     errorMessage = '';
277 
278     % FastHenry COM object initialization
279     try
280         fh = actxserver('FastHenry2.Document');
281     catch ME
282        errorMessage = sprintf('Error initializing FastHenry2: %s\n', ...
               ↪ ME.message);
283        fprintf('%s\n', errorMessage);
284         imbalance = inf;
```

```
285         return;
286     end
287 
288  try
289     % Read the original file content
290     fileContent = fileread(inputFileOriginal);
291 
292     % Define the original hole line to be removed
293     originalHoleLine = '+         hole rect ...
        ↪ (-299.14912108776,154.99969853018436,333.09999999981636,-295.1494921179811,234.999
294 
295     % Remove the original hole line
296     newFileContent = strrep(fileContent, originalHoleLine, '');
297 
298     % Find the position where the original hole line was located
299     holePosition = strfind(fileContent, originalHoleLine);
300     if isempty(holePosition)
301         error('Could not find the original hole line.');
302     end
303 
304     % Initialize a string for new holes
305     newHoleLines = "";
306     IntCon = [45 46 47  48  49  50  51  52  53  54  55  56];
307 
308 % Generate the correct indexing for 3 sections (2 holes per section)
309 for i = 0:2  % Three sections (indexing shift)
310     rect_idx = [1,2,3,4] + i*14;  % x, y, width, height
311     circ_idx = [5,6,7] + i*14;    % x, y, radius
312     rect_idx_2 = [8,9,10,11] + i*14;  % Second rectangle in section
313     circ_idx_2 = [12,13,14] + i*14;   % Second circle in section
314 
315     % Rectangular hole 1 existence check
316     exist_idx_rect1 = IntCon(4*i + 1);  % Correct alternating pattern
317     if x(exist_idx_rect1) == 1
318         rectHoleLine = sprintf('+         hole rect ...
            ↪ (%0.1f,%0.1f,333.09999999981636,%0.1f,%0.1f,333.09999999981636)',...
319             x(rect_idx(1)), x(rect_idx(2)), x(rect_idx(1)) + ...
                ↪ x(rect_idx(3)), x(rect_idx(2)) + x(rect_idx(4)));
320         newHoleLines = newHoleLines + rectHoleLine + newline;
321     end
322 
323     % Circular hole 1 existence check
324     exist_idx_circ1 = IntCon(4*i + 2);
325     if x(exist_idx_circ1) == 1
326         circHoleLine = sprintf('+         hole circle ...
            ↪ (%0.1f,%0.1f,333.09999999981636,%0.1f)',...
327             x(circ_idx(1)), x(circ_idx(2)), x(circ_idx(3)));
328         newHoleLines = newHoleLines + circHoleLine + newline;
329     end
330 
331     % Rectangular hole 2 existence check
332     exist_idx_rect2 = IntCon(4*i + 3);
333     if x(exist_idx_rect2) == 1
334         rectHoleLine = sprintf('+         hole rect ...
            ↪ (%0.1f,%0.1f,333.09999999981636,%0.1f,%0.1f,333.09999999981636)',...
335             x(rect_idx_2(1)), x(rect_idx_2(2)), x(rect_idx_2(1)) + ...
                ↪ x(rect_idx_2(3)), x(rect_idx_2(2)) + x(rect_idx_2(4)));
336         newHoleLines = newHoleLines + rectHoleLine + newline;
```

```
337     end
338
339     % Circular hole 2 existence check
340     exist_idx_circ2 = IntCon(4*i + 4);
341     if x(exist_idx_circ2) == 1
342         circHoleLine = sprintf('+         hole circle ...
                ↪ (%0.1f,%0.1f,333.09999999981636,%0.1f)',...
343             x(circ_idx_2(1)), x(circ_idx_2(2)), x(circ_idx_2(3)));
344         newHoleLines = newHoleLines + circHoleLine + newline;
345     end
346 end
347
348
349     % Insert the new holes in the file at the original hole's position
350     newFileContent = [fileContent(1:holePosition-1), newHoleLines, ...
            ↪ fileContent(holePosition+length(originalHoleLine):end)];
351
352
353     % Node replacements
354     node_443 = 'NFHNode443 x=-210.39999999999998 y=195.0 z=353.1';
355     nodeReplacement_443 = sprintf('NFHNode443 x=-210.39999999999998 ...
            ↪ y=%0.2f z=353.1', x(43));
356
357     node_444 = 'NFHNode444 x=-264.15 y=195.0 z=353.1';
358     nodeReplacement_444 = sprintf('NFHNode444 x=-264.15 y=%0.2f ...
            ↪ z=353.1', x(43));
359
360     node_446 = 'NFHNode446 x=-210.4 y=195.0 z=353.1';
361     nodeReplacement_446 = sprintf('NFHNode446 x=-210.4 y=%0.2f z=353.1', ...
            ↪ x(43));
362
363     node_447 = 'NFHNode447 x=-210.39999999999995 y=-130.00000000000006 ...
            ↪ z=153.10000000000005';
364     nodeReplacement_447 = sprintf('NFHNode447 x=-210.39999999999995 ...
            ↪ y=%0.2f z=%0.2f', -130.00000000000006 -195.0 + x(43), x(44));
365
366     node_output_busbar = 'Noutput_busbar_interface x=-264.1499999856986 ...
            ↪ y=194.99999999138097 z=334.0999999997084';
367     nodeReplacement_output_busbar = sprintf('Noutput_busbar_interface ...
            ↪ x=-264.1499999856986 y=%0.2f z=334.0999999997084', x(43));
368
369     node_450 = 'NFHNode450 x=-210.39999999999995 y=194.99999999999994 ...
            ↪ z=153.09999999999997';
370     nodeReplacement_450 = sprintf('NFHNode450 x=-210.39999999999995 ...
            ↪ y=%0.1f z=%0.1f', x(43), x(44));
371
372     % Apply node replacements
373     newFileContent = strrep(newFileContent, node_443, nodeReplacement_443);
374     newFileContent = strrep(newFileContent, node_444, nodeReplacement_444);
375     newFileContent = strrep(newFileContent, node_446, nodeReplacement_446);
376     newFileContent = strrep(newFileContent, node_447, nodeReplacement_447);
377     newFileContent = strrep(newFileContent, node_output_busbar, ...
            ↪ nodeReplacement_output_busbar);
378     newFileContent = strrep(newFileContent, node_450, nodeReplacement_450);
379
380
381     % Write the new content to the output file
382     fid = fopen(outputFile, 'w');
```

```
383     fprintf(fid, '%s', newFileContent);
384     fclose(fid);
385 catch ME
386     errorMessage = sprintf('Error modifying the input file: %s', ...
            ↪ ME.message);
387     fprintf('%s\n', errorMessage);
388     imbalance = inf;
389     return;
390 end
391     % Run FastHenry with modified file
392     try
393         couldRun = invoke(fh, 'Run', ['"' outputFile '"']);
394         if ¬couldRun
395             errorMessage = sprintf('Error running FastHenry with file: ...
                    ↪ %s', outputFile);
396             fprintf('%s\n', errorMessage);
397             imbalance = inf;
398             return;
399         end
400 
401             % Show FastHenry console window
402              %invoke(fh, 'ShowWindow');
403              %disp('FastHenry console window is now visible.');
404 
405         % Wait for simulation to complete
406         while invoke(fh, 'IsRunning')
407             pause(1);
408         end
409 
410          % Retrieve frequencies
411             frequenciesCell = invoke(fh, 'GetFrequencies');
412             if isempty(frequenciesCell)
413             error('No frequencies returned from FastHenry.');
414             end
415             frequencies = cell2mat(frequenciesCell);
416 
417           % Find index of target frequency
418             [¬, targetIdx] = min(abs(frequencies - targetFrequency));
419             targetFreq = frequencies(targetIdx);
420             %disp(['Target Frequency: ', num2str(targetFreq), ' Hz']);
421 
422           % Retrieve impedance and resistance data for the target frequency
423             rawImpedance = invoke(fh, 'GetInductance');
424             rawResistance = invoke(fh, 'GetResistance');
425 
426             if isempty(rawImpedance) || isempty(rawResistance)
427                 error('No impedance or resistance data returned.');
428             end
429 
430           % Determine the matrix dimensions dynamically (assuming square ...
                ↪ matrix)
431             numElements = numel(rawImpedance(targetIdx, :));
432             numNodes = sqrt(numElements);
433             if mod(numElements, numNodes) ≠ 0
434                 error('Matrix dimensions are not square.');
435             end
436 
437           % Extract and reshape resistance and inductance matrices
```

```
438             R_matrix = reshape(cellfun(@double, rawResistance(targetIdx, ...
                    ↪ :)), [numNodes, numNodes]);
439             L_matrix = reshape(cellfun(@double, rawImpedance(targetIdx, ...
                    ↪ :)), [numNodes, numNodes]);
440 
441           % Compute impedance Z
442             omega = 2 * pi * targetFrequency;
443             Z_omega = R_matrix + 1i * omega * L_matrix;
444             Z = R_matrix + 1i*L_matrix;
445 
446          % Display the computed impedance matrix
447             %disp(['Impedance Matrix at ', num2str(targetFrequency), ' ...
                    ↪ Hz:']);
448             %disp(Z);
449 
450         % % Time Domain Simulation
451         % imag_inv = inv(imag(Z));
452         %
453         % dt=0.01e-6;
454         % nmax = round(50e-6/dt);
455         % time=dt*(0:(nmax-1));
456         % ii =zeros(2,nmax);
457         % L = 51.15e-6;
458         % V_expected = 1350;
459         % t = 50e-6;
460         % expected_I = V_expected*t/L;
461         % expected_I_r1 = 3777.48;
462         %
463         % vtot = ones(2, nmax);  % Initialize voltage array (scaled ...
              ↪ externally)
464         % x = 1.0;               % Scaling factor
465         % current_sum = 0;       % Initialize current sum
466         %
467         % while current_sum < round(expected_I)
468         %     for n = 2:nmax
469         %         vr(:, n) = real(Z) * ii(:, n-1);       % Voltage ...
              ↪ across resistance
470         %         vl(:, n) = vtot(:, n) - vr(:, n);     % Voltage across ...
              ↪ inductance
471         %         ii(:, n) = ii(:, n-1) + imag_inv * dt * vl(:, n); % ...
              ↪ Update current
472         %     end
473         %
474         %     current_sum = sum(ii(1, end) + ii(2, end)); % Calculate ...
              ↪ total current
475         %
476         %     if current_sum < round(expected_I)
477         %         x = x + 0.1;   % Increment voltage scaling
478         %         vtot = x * ones(2, nmax);  % Apply scaling
479         %     else
480         %         break;
481         %     end
482         % end
483         %
484         % % Calculate imbalance at 47 μs
485         % idx_47us = round(nmax * 47 / 50);
486         % current_mod1 = ii(2, idx_47us);
487         % current_mod3 = ii(1, idx_47us);
```

```
488         % imbalance = abs(current_mod1 - current_mod3);
489         % percentage_imbalance = imbalance*100;
490      % Frequency Domain Simulation (for any square impedance matrix Z_omega)
491             % Compute reference current response with unit voltage
492             V_injected = 100*ones(numNodes, 1);
493             I_f = inv(Z_omega) * (V_injected);
494             I_f_mod = abs(I_f);
495 
496               % Imbalance computed from distance from the mean
497               I_f_mean = mean(I_f_mod);
498               % Compute imbalance for each node
499               percentage_imbalance = ((abs(I_f_mod - ...
                      ↪ I_f_mean))/I_f_mean)*100;
500 
501             % Compute variance of imbalance (fitness function)
502             imbalance = var(I_f_mod);
503 
504             % Store variables in the workspace
505             %assignin('base', 'I_f_mod', I_f_mod);
506             %assignin('base', 'I_f_mean', I_f_mean);
507             assignin('base', 'percentage_imbalance', percentage_imbalance);
508             assignin('base', 'imbalance', imbalance);
509             %assignin('base', 'a', a);
510             %assignin('base', 'percentage_imbalance', percentage_imbalance);
511 
512     catch ME
513         errorMessage = sprintf('Error in FastHenry simulation: %s', ...
                ↪ ME.message);
514         fprintf('%s\n', errorMessage);
515         imbalance = inf;
516         percentage_imbalance = inf;
517         % I_f = [];
518         % I_f_mean = [];
519         % V_injected = [];
520         % percentage_imbalance =[];
521     end
522 
523     % Cleanup FastHenry
524     try
525         invoke(fh, 'Quit');
526         release(fh);
527     catch ME
528         errorMessage = sprintf('Error terminating FastHenry2: %s', ...
                ↪ ME.message);
529         fprintf('%s\n', errorMessage);
530     end
531 end
532 
533 
534 %% GA Output Function for Visualization and Custom Stopping Criterion
535 
536 function [state, options, optchanged] = gaOutputFcn(options, state, flag)
537     persistent bestHistory populationHistory
538     optchanged = false;
539     switch flag
540         case 'init'
541             disp('Starting Genetic Algorithm...');
542             bestHistory = [];
```

```
543             populationHistory = struct('GenerationData', {});
544             figure; hold on;
545             xlabel('Generation'); ylabel('Best Fitness');
546             title('GA Convergence');
547         case 'iter'
548             [bestFit, ¬] = min(state.Score); % Best fitness value and ...
                    ↪ its index
549             bestHistory(end+1) = bestFit; % Track the best fitness
550 
551             % Calculate percentage imbalance, error messages, imbalance, ...
                    ↪ raw imbalance, and penalties for each genome
552             percentageImbalance = cell(size(state.Population, 1), 1);
553             errorMessages = cell(size(state.Population, 1), 1);
554             imbalance = zeros(size(state.Population, 1), 1);
555             raw_imbalance = zeros(size(state.Population, 1), 1); % Track ...
                    ↪ raw imbalance
556             penalties = zeros(size(state.Population, 1), 1); % Track ...
                    ↪ penalties
557             maxPercentageImbalance = zeros(size(state.Population, 1), ...
                    ↪ 1); % Track max percentage imbalance
558 
559             for i = 1:size(state.Population, 1)
560                 try
561                     [imbalance(i), raw_imbalance(i), penalties(i)] = ...
                            ↪ busbarFitnessWithPenalty(state.Population(i, :));
562                     [¬, percentageImbalance{i}, errorMessages{i},¬,¬] = ...
                            ↪ busbarFitness(state.Population(i, :));
563                     maxPercentageImbalance(i) = max(percentageImbalance{i});
564                 catch ME
565                     percentageImbalance{i} = inf;
566                     errorMessages{i} = ME.message;
567                     imbalance(i) = inf;
568                     raw_imbalance(i) = inf;
569                     penalties(i) = inf;
570                     maxPercentageImbalance(i) = inf;
571                 end
572             end
573 
574             % Store each population member's data together
575             populationHistory(state.Generation).GenerationData = ...
                    ↪ arrayfun(@(i) struct( ...
576                 'Genome', state.Population(i, :), ...
577                 'PercentageImbalance', percentageImbalance{i}, ...
578                 'ErrorMessage', errorMessages{i}, ...
579                 'Imbalance', imbalance(i), ...
580                 'RawImbalance', raw_imbalance(i), ...
581                 'Penalties', penalties(i), ...
582                 'MaxPercentageImbalance', maxPercentageImbalance(i)), ...
                        ↪ 1:size(state.Population, 1));
583 
584             fprintf('Generation %d: Best Fitness = %.4f\n', ...
                    ↪ state.Generation, bestFit);
585             plot(state.Generation, bestFit, 'bo-'); % Plot best fitness
586             drawnow;
587 
588             % Custom stopping criterion
589             if all(maxPercentageImbalance < 4)
```

```
590                 disp('Stopping criterion met: Maximum percentage ...
                        ↪ imbalance is less than 5%');
591                 state.StopFlag = 'Maximum percentage imbalance is less ...
                        ↪ than 5%';
592             end
593
594         case 'done'
595             disp('Genetic Algorithm Completed.');
596             assignin('base', 'bestHistory', bestHistory);
597             assignin('base', 'populationHistory', populationHistory);
598
599             % 2D Convergence Plot
600             figure;
601             plot(1:length(bestHistory), bestHistory, 'r-o', 'LineWidth', 2);
602             xlabel('Generation'); ylabel('Best Fitness');
603             title('Genetic Algorithm Convergence (2D)');
604             grid on;
605     end
606 end
607
608 %% Function to Save Best Cutout Design
609 function saveBestDesign(bestFile, x_opt,IntCon)
610 % Define constants
611 inputFileOriginal = ...
        ↪ 'C:\Users\poohg\OneDrive\Desktop\Master_Thesis_Semester\KK Wind ...
        ↪ Project\Optimization Techniques\GA Optimization full ...
        ↪ system\Step4_Introducing_Full_Model\DCneg_SM1_1filament_GA_full_model_AL.inp';
612
613  try
614     % Read the original file content
615     fileContent = fileread(inputFileOriginal);
616
617     % Define the original hole line to be removed
618     originalHoleLine = '+         hole rect ...
            ↪ (-299.14912108776,154.99969853018436,333.09999999981636,-295.1494921179811,234.999
619
620     % Remove the original hole line
621     newFileContent = strrep(fileContent, originalHoleLine, '');
622
623     % Find the position where the original hole line was located
624     holePosition = strfind(fileContent, originalHoleLine);
625     if isempty(holePosition)
626         error('Could not find the original hole line.');
627     end
628
629     % Initialize a string for new holes
630     newHoleLines = "";
631     %IntCon = [45 46    47  48  49  50  51  52  53  54  55  56];
632
633 % Generate the correct indexing for 3 sections (2 holes per section)
634 for i = 0:2  % Three sections (indexing shift)
635     rect_idx = [1,2,3,4] + i*14;  % x, y, width, height
636     circ_idx = [5,6,7] + i*14;    % x, y, radius
637     rect_idx_2 = [8,9,10,11] + i*14;  % Second rectangle in section
638     circ_idx_2 = [12,13,14] + i*14;   % Second circle in section
639
640     % Rectangular hole 1 existence check
641     exist_idx_rect1 = IntCon(4*i + 1);  % Correct alternating pattern
```

```
642
643     if x_opt(exist_idx_rect1) == 1
644         rectHoleLine = sprintf('+         hole rect ...
                ↪ (%0.1f,%0.1f,333.09999999981636,%0.1f,%0.1f,333.09999999981636)',...
645             x_opt(rect_idx(1)), x_opt(rect_idx(2)), x_opt(rect_idx(1)) + ...
                    ↪ x_opt(rect_idx(3)), x_opt(rect_idx(2)) + ...
                    ↪ x_opt(rect_idx(4)));
646         newHoleLines = newHoleLines + rectHoleLine + newline;
647     end
648
649     % Circular hole 1 existence check
650     exist_idx_circ1 = IntCon(4*i + 2);
651     if x_opt(exist_idx_circ1) == 1
652         circHoleLine = sprintf('+         hole circle ...
                ↪ (%0.1f,%0.1f,333.09999999981636,%0.1f)',...
653             x_opt(circ_idx(1)), x_opt(circ_idx(2)), x_opt(circ_idx(3)));
654         newHoleLines = newHoleLines + circHoleLine + newline;
655     end
656
657     % Rectangular hole 2 existence check
658     exist_idx_rect2 = IntCon(4*i + 3);
659     if x_opt(exist_idx_rect2) == 1
660         rectHoleLine = sprintf('+         hole rect ...
                ↪ (%0.1f,%0.1f,333.09999999981636,%0.1f,%0.1f,333.09999999981636)',...
661             x_opt(rect_idx_2(1)), x_opt(rect_idx_2(2)), ...
                    ↪ x_opt(rect_idx_2(1)) + x_opt(rect_idx_2(3)), ...
                    ↪ x_opt(rect_idx_2(2)) + x_opt(rect_idx_2(4)));
662         newHoleLines = newHoleLines + rectHoleLine + newline;
663     end
664
665     % Circular hole 2 existence check
666     exist_idx_circ2 = IntCon(4*i + 4);
667     if x_opt(exist_idx_circ2) == 1
668         circHoleLine = sprintf('+         hole circle ...
                ↪ (%0.1f,%0.1f,333.09999999981636,%0.1f)',...
669             x_opt(circ_idx_2(1)), x_opt(circ_idx_2(2)), ...
                    ↪ x_opt(circ_idx_2(3)));
670         newHoleLines = newHoleLines + circHoleLine + newline;
671     end
672 end
673
674     % Insert the new holes in the file at the original hole's position
675     newFileContent = [fileContent(1:holePosition-1), newHoleLines, ...
            ↪ fileContent(holePosition+length(originalHoleLine):end)];
676
677     % Node replacements
678     node_443 = 'NFHNode443 x=-210.39999999999998 y=195.0 z=353.1';
679     nodeReplacement_443 = sprintf('NFHNode443 x=-210.39999999999998 ...
            ↪ y=%0.2f z=353.1', x_opt(43));
680     node_444 = 'NFHNode444 x=-264.15 y=195.0 z=353.1';
681     nodeReplacement_444 = sprintf('NFHNode444 x=-264.15 y=%0.2f ...
            ↪ z=353.1', x_opt(43));
682     node_446 = 'NFHNode446 x=-210.4 y=195.0 z=353.1';
683     nodeReplacement_446 = sprintf('NFHNode446 x=-210.4 y=%0.2f z=353.1', ...
            ↪ x_opt(43));
684     node_447 = 'NFHNode447 x=-210.39999999999995 y=-130.00000000000006 ...
            ↪ z=153.10000000000005';
```

```
685     nodeReplacement_447 = sprintf('NFHNode447 x=-210.39999999999995 ...
            ↪ y=%0.2f z=%0.2f', -130.00000000000006 -195.0 + x_opt(43), ...
            ↪ x_opt(44));
686     node_output_busbar = 'Noutput_busbar_interface x=-264.1499999856986 ...
            ↪ y=194.99999999138097 z=334.0999999997084';
687     nodeReplacement_output_busbar = sprintf('Noutput_busbar_interface ...
            ↪ x=-264.1499999856986 y=%0.2f z=334.0999999997084', x_opt(43));
688     node_450 = 'NFHNode450 x=-210.39999999999995 y=194.99999999999994 ...
            ↪ z=153.09999999999997';
689     nodeReplacement_450 = sprintf('NFHNode450 x=-210.39999999999995 ...
            ↪ y=%0.1f z=%0.1f', x_opt(43), x_opt(44));
690
691     % Apply node replacements
692     newFileContent = strrep(newFileContent, node_443, nodeReplacement_443);
693     newFileContent = strrep(newFileContent, node_444, nodeReplacement_444);
694     newFileContent = strrep(newFileContent, node_446, nodeReplacement_446);
695     newFileContent = strrep(newFileContent, node_447, nodeReplacement_447);
696     newFileContent = strrep(newFileContent, node_output_busbar, ...
            ↪ nodeReplacement_output_busbar);
697     newFileContent = strrep(newFileContent, node_450, nodeReplacement_450);
698
699     % Write the new content to the output file
700     fid = fopen(bestFile, 'w');
701     fprintf(fid, '%s', newFileContent);
702     fclose(fid);
703     fprintf('Best cutout design saved in: %s\n', bestFile);
704
705 catch ME
706     fprintf('**Error writing to file: %s**\n', bestFile);
707     fprintf('**Error message:** %s\n', ME.message);
708     fprintf('**Stack trace:**\n');
709     disp(ME.stack);
710     return;
711 end
712
713 % FastHenry COM object initialization for showing the window
714 try
715     fh = actxserver('FastHenry2.Document');
716     invoke(fh, 'ShowWindow');
717     disp('FastHenry console window is now visible.');
718 catch ME
719     fprintf('Error opening FastHenry window: %s\n', ME.message);
720 end
721
722 end
723
724
725 %% SPICE Model Integration
726
727 function generateSpiceNetlist(inputFile, outputFile, cFilePath, hFilePath)
728     % generateSpiceNetlist - Generates a SPICE netlist using FastHenry C ...
            ↪ code
729     %
730     % Syntax: generateSpiceNetlist(inputFile, outputFile, frequency, ...
            ↪ cFilePath, hFilePath)
731     %
732     % Inputs:
733     %    inputFile - The input file for FastHenry
```

```
734     %     outputFile - The output SPICE netlist file
735     %     frequency - The frequency for the equivalent circuit
736     %     cFilePath - Full path to MakeLcircuit2.c
737     %     hFilePath - Full path to cmplx.h
738
739     % Compile the C code
740     compileCommand = sprintf('gcc -o MakeLcircuit "%s" "%s"', cFilePath, ...
            ↪ hFilePath);
741     [status, cmdout] = system(compileCommand);
742     if status ≠ 0
743         error('Error compiling C code: %s', cmdout);
744     end
745
746     % Run the compiled C code
747     runCommand = sprintf('MakeLcircuit "%s" > "%s"', inputFile, outputFile);
748     [status, cmdout] = system(runCommand);
749     if status ≠ 0
750         error('Error running C code: %s', cmdout);
751     end
752
753     fprintf('SPICE netlist generated successfully: %s\n', outputFile);
754
755     % Open the SPICE file in Notepad (Windows)
756     system(sprintf('notepad "%s"', outputFile));
757 end
```

Appendix C Theory

C.1 Power Electronics Devices

Power electronics has become an indispensable pillar of modern electrical engineering, enabling the efficient conversion, control, and conditioning of electric power across a wide spectrum of applications—from industrial drives and renewable energy systems to electric vehicles and PtX. At the core of these systems are power semiconductor devices, which have evolved from early bipolar junction transistors and thyristors to advanced MOSFETs, IGBTs, and wide-bandgap devices like SiC and GaN.

The power semi-conductor devices handle high voltages and currents while switching at high frequencies, making them essential for achieving compact, efficient, and reliable power conversion. The integration of these devices into power modules has further enhanced their thermal and electrical performance, allowing for higher power densities and modular scalability.

C.1.1 Device Paralleling

Looking at the current trends of higher power demands, IGBTs and MOSFET power modules are gaining popularity due to their paralleling potential. It begs the question why these devices are more suited towards connecting in parallel as compared to other power devices such as BJTs, Thyristors and SCRs etc.

There are certain aspects which enable the devices to stand out. Following are some of the reasons:

- **Positive Temperature Coefficient** - Both IGBTs and MOSFETs exhibit positive temperature co-efficient in their on-state characteristics which favors uniform current distribution within chips. This self-balancing feature with continuous conduction makes them ideal for paralleling.
- **Voltage-Controlled Operation** - These devices are voltage-driven, as opposed to their current-controlled counter parts requiring careful current injection for operation. The voltages can be better controlled by the gate-driver units allowing paralleling operation of multiple power devices.
- **Fast Switching and Controlled Turn-off** - IGBTs and MOSFETs can be turned on and off precisely using gate signals, allowing for synchronized switching in parallel configurations. While Thyristors and SCRs latch on and cannot be turned off by gate control. They require external commutation circuits, making synchronized parallel operation complex and unreliable. The complexity of circuits with high component counts for the Thyristors and SCRs making it a costly construction.

C.2 Challenges with Parasitics

In high-power electronic systems, it is common to connect these multiple semiconductor devices in parallel to share current and increase overall power handling capability. At first glance, these devices might appear to inherently balance their current distribution due to their self-regulating electrical characteristics. For instance, a MOSFET with a higher current will heat up, leading to an increase in $R_{DS(on)}$, and thereby reducing its

current. Similarly, an IGBT's $V_{CE(on)}$ rises with temperature, theoretically pushing the device toward balanced operation.

However, practical implementation reveals that self-balancing alone is often insufficient.

Parasitic Balancing in Parallel Devices: Why It Is Essential?

The self-balancing effect is not instantaneous and is only effective in steady-state conditions. During switching or transient events, self-balancing mechanisms cannot react quickly enough to mitigate current imbalances. Therefore, both internal and external parasitic balancing is critical to ensure reliable, safe, and uniform current sharing among parallel-connected devices.

One of the key issues is that during turn-on, current distribution is highly sensitive to, parasitic inductances, and device threshold mismatches. If even one device conduct more current than its counterparts, the risks of thermal or electrical overstress rises.

Additionally, high-speed switching introduces significant voltage transients due to parasitic inductances in PCB traces or bond wires. These fast, high-energy transitions can lead to voltage overshoot, ringing, or oscillations, especially if one path has significantly lower inductance.

Furthermore, asymmetries in PCB or busbar layout—such as trace length, via count, or pad positioning—can introduce unequal inductive and resistive paths. This undermines the electrical environment of each device, preventing natural balancing.

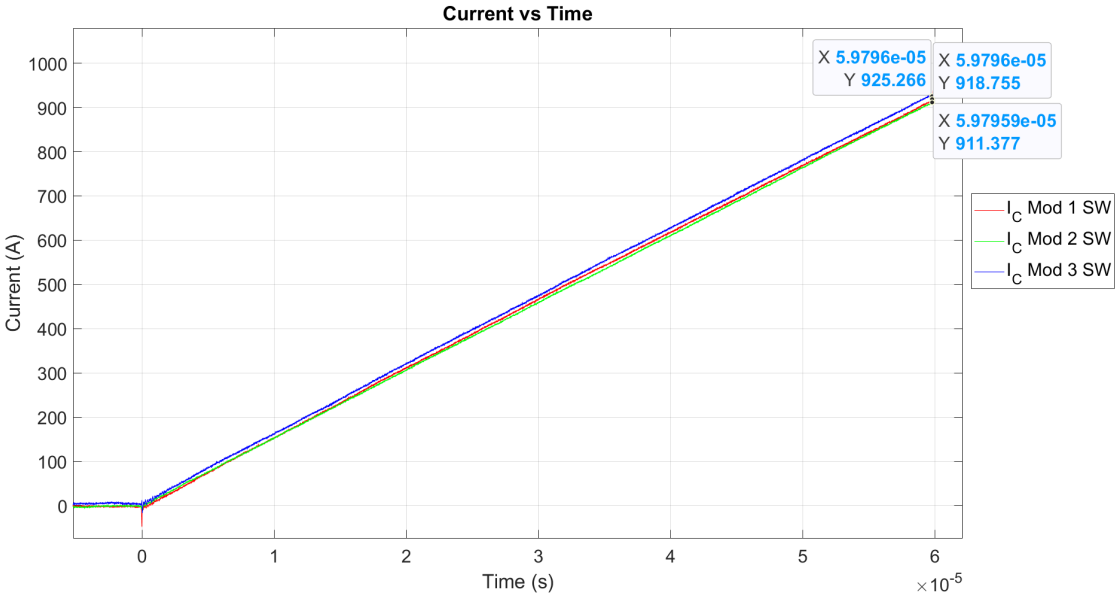
To address these concerns, designers must ensure both:

- **Internal Balancing:** Symmetric design of the module—e.g., matched bond wires and emitter paths.
- **External Balancing:** Symmetric PCB or busbar layout to equalize impedance from each device to the power source and load.

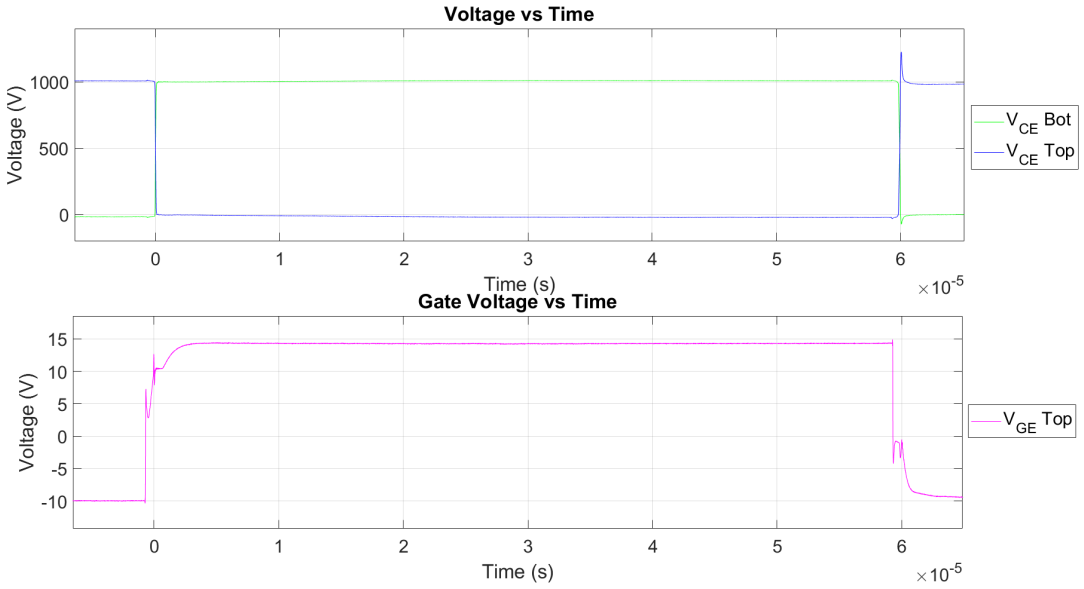
Therefore, Even though self-balancing characteristics are helpful during continuous conduction, they are not sufficient for dynamic conditions in high-speed power converters. Meticulous internal and external layout design is necessary to prevent current concentration, ensure reliable operation, and protect against premature device failure in parallel power modules. This makes it is necessary to model such parameters to quantify the imbalances and mitigate the issues caused due to these imbalances.

Appendix D Lab Test Results

D.1 Mid-point connection at z = 153 mm

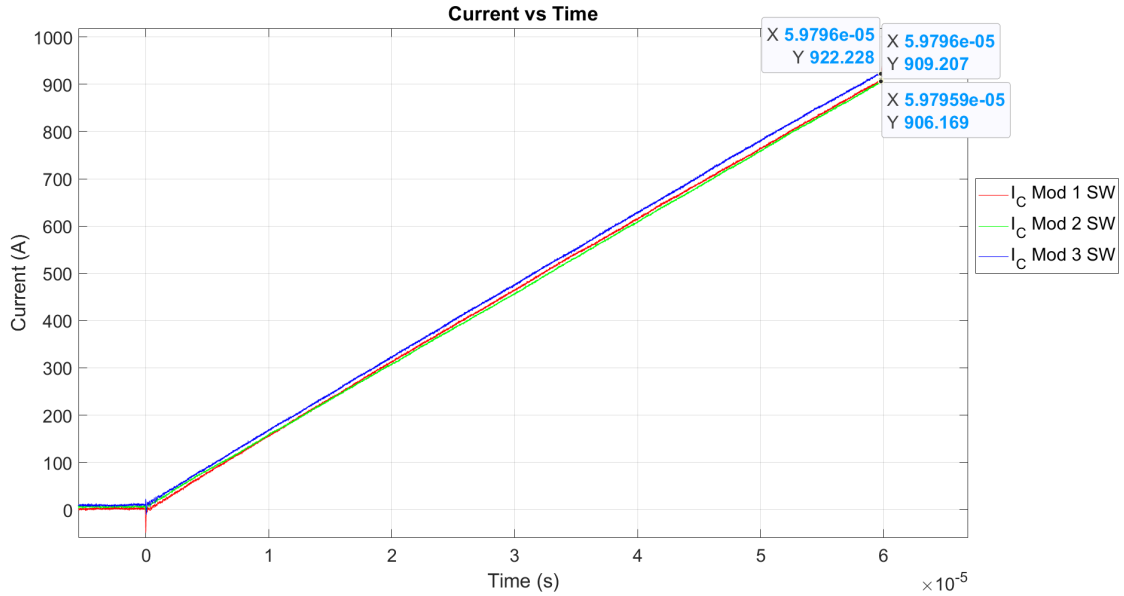


(a) Current Sharing - Variant 1

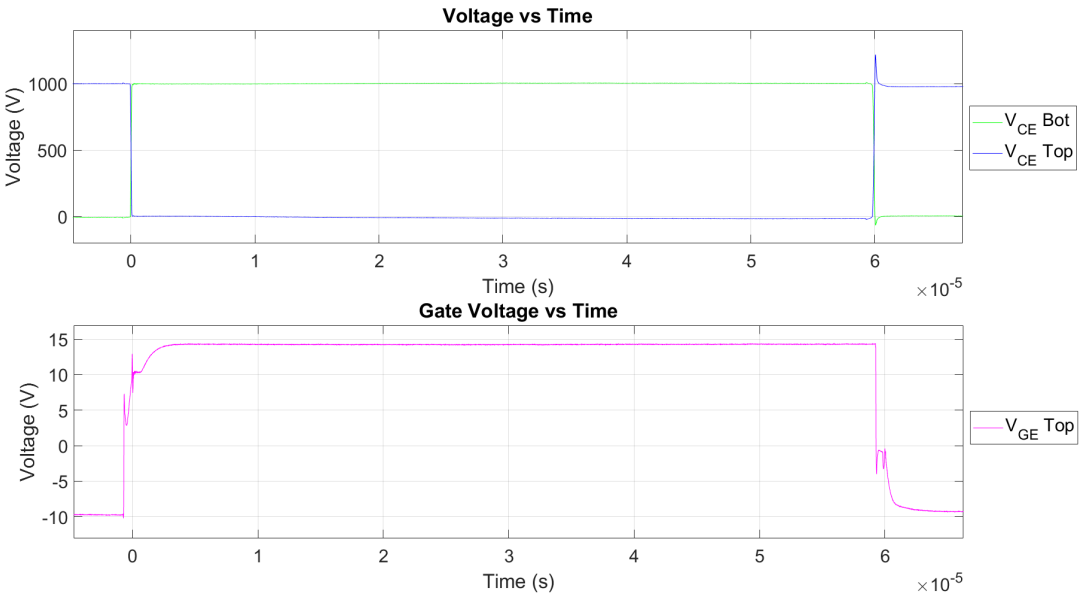


(b) Voltage Graphs - Variant 1

Figure D.1: Mid-point connection - Variant 1

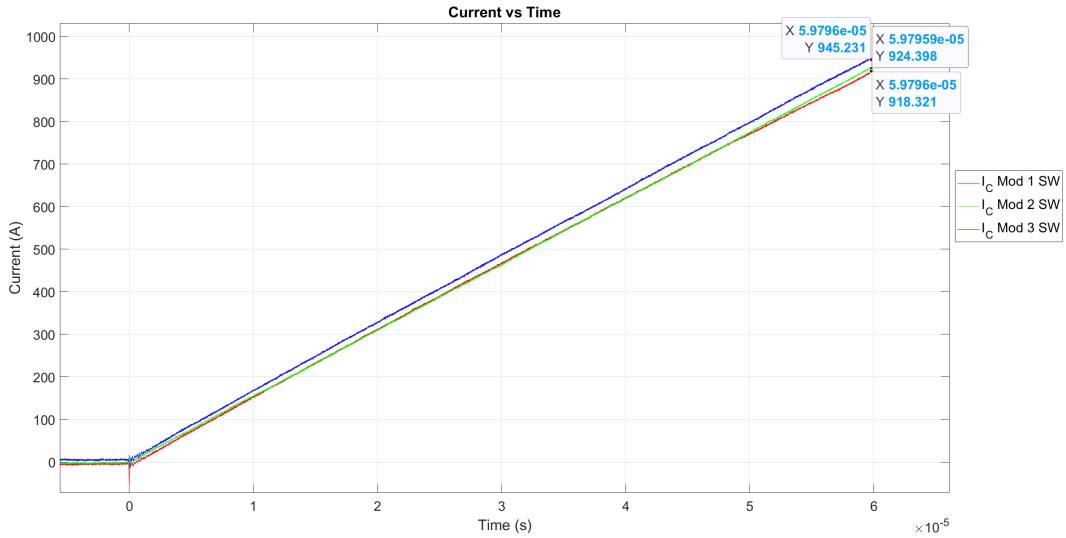


(a) Current Sharing - Variant 2

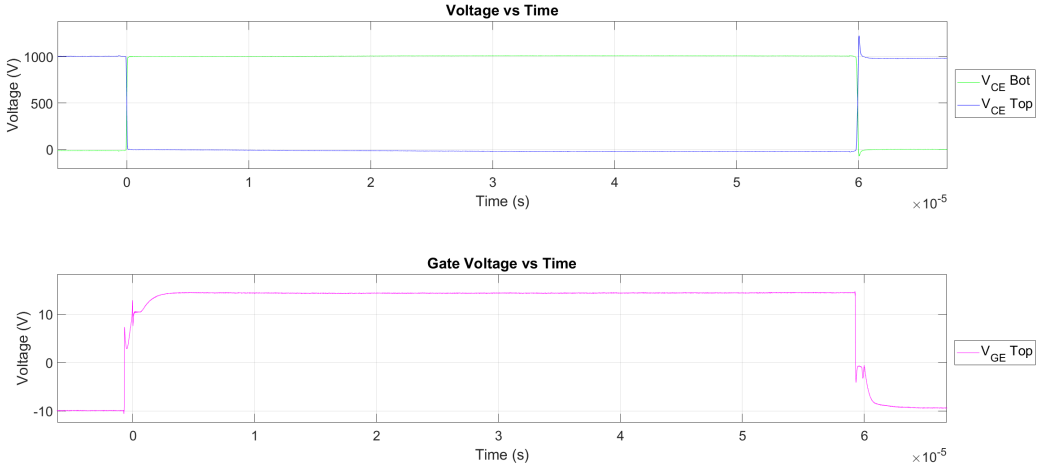


(b) Voltage Graphs - Variant 2

Figure D.2: Mid-point connection - Variant 2



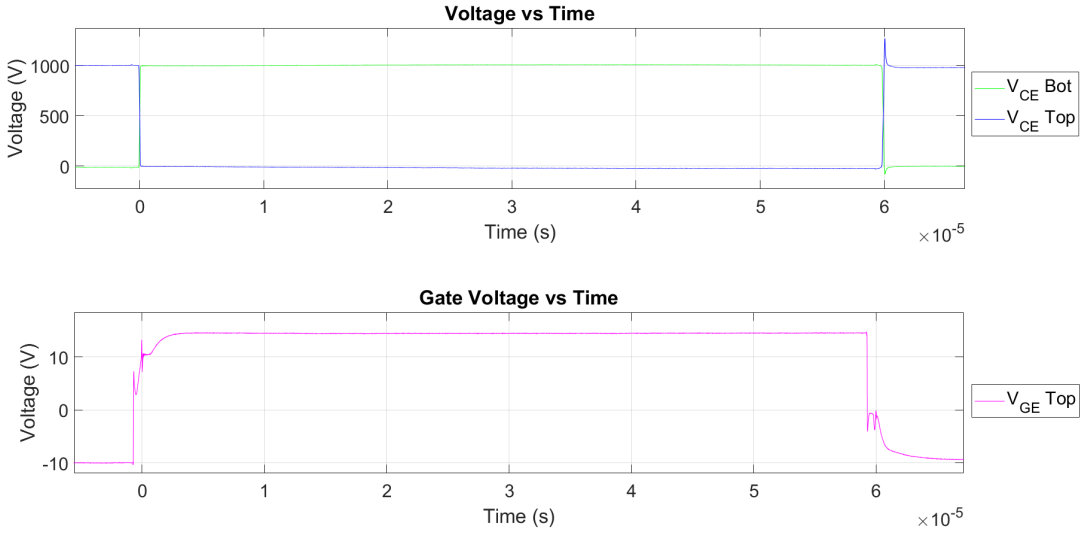
(a) Current Sharing - Variant 3



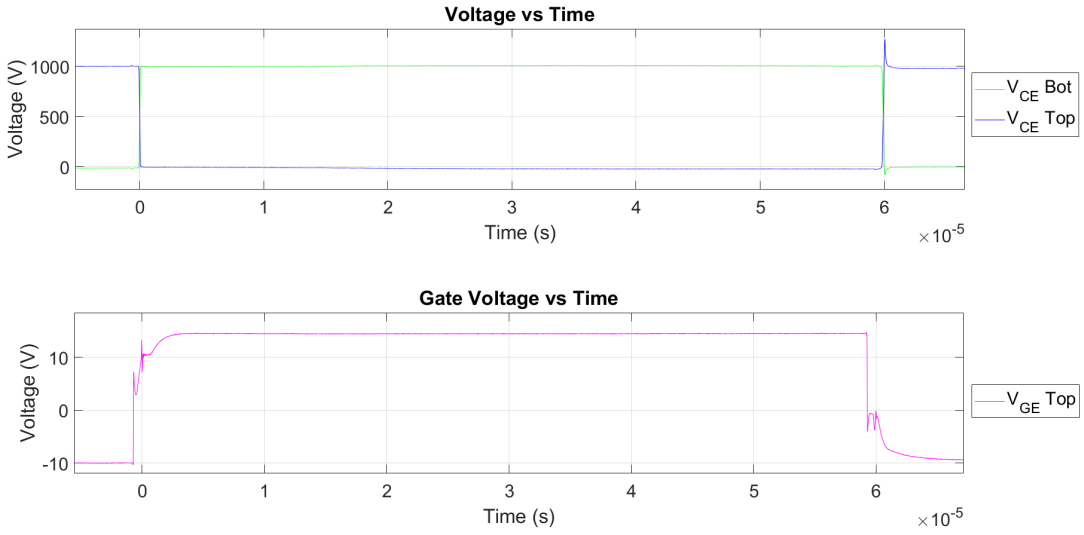
(b) Voltage Graphs - Variant 3

Figure D.3: Mid-point connection - Variant 3

D.2 End-point connection at z = 153 mm

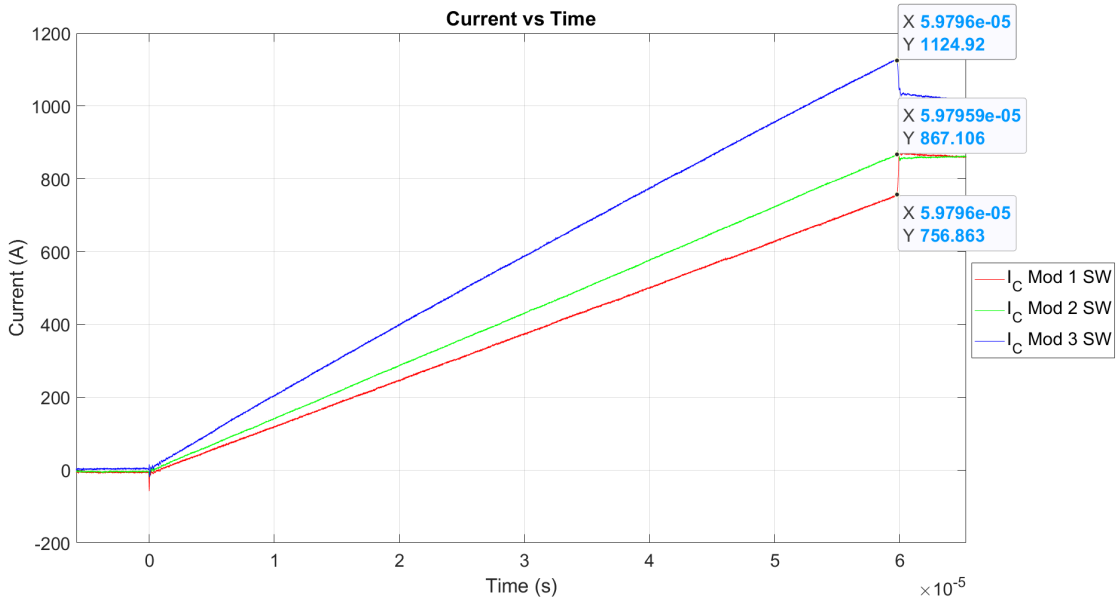


(a) Current Sharing - Variant 1

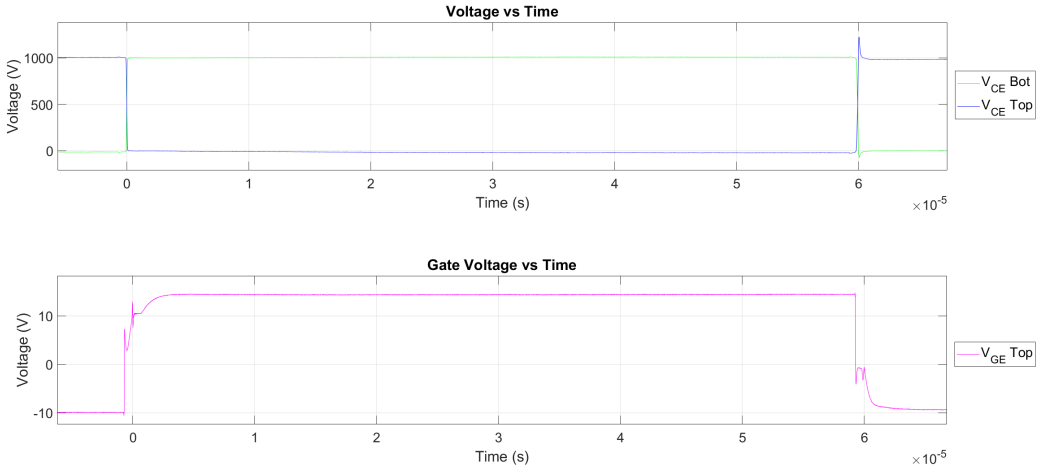


(b) Voltage Graphs - Variant 1

Figure D.4: End-point connection - Variant 1

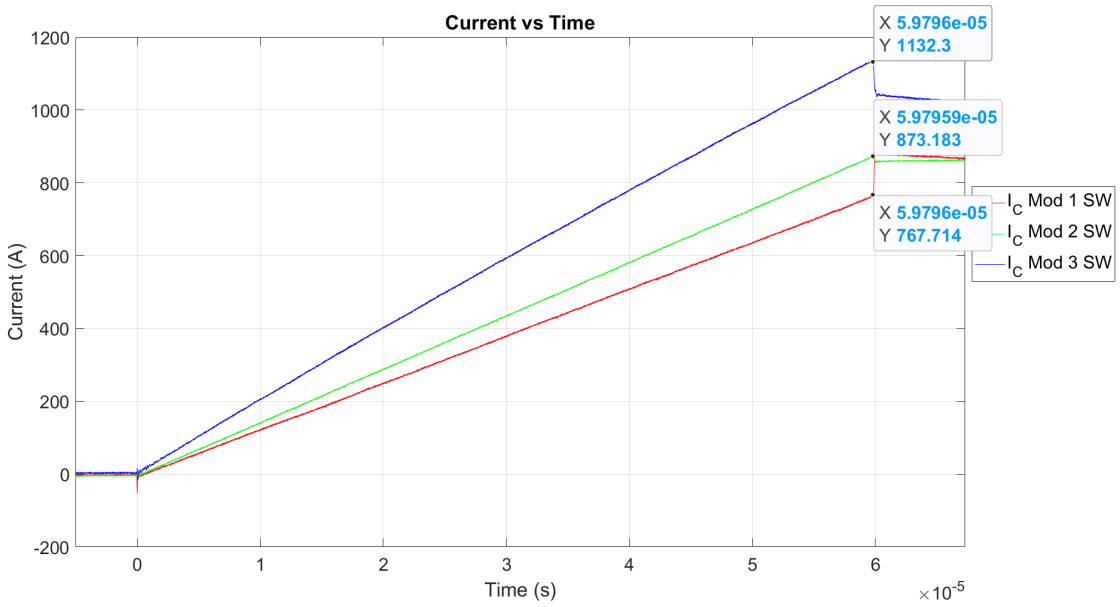


(a) Current Sharing - Variant 2

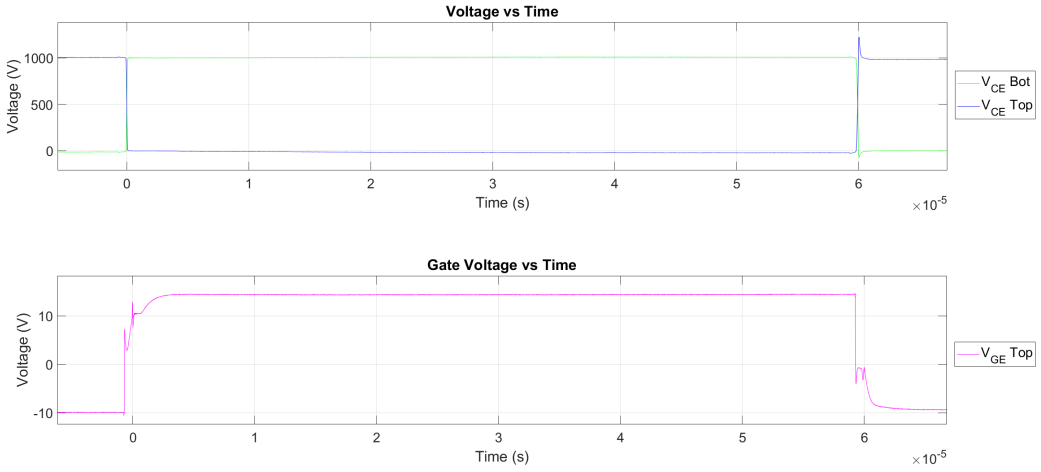


(b) Voltage Graphs - Variant 2

Figure D.5: End-point connection - Variant 2



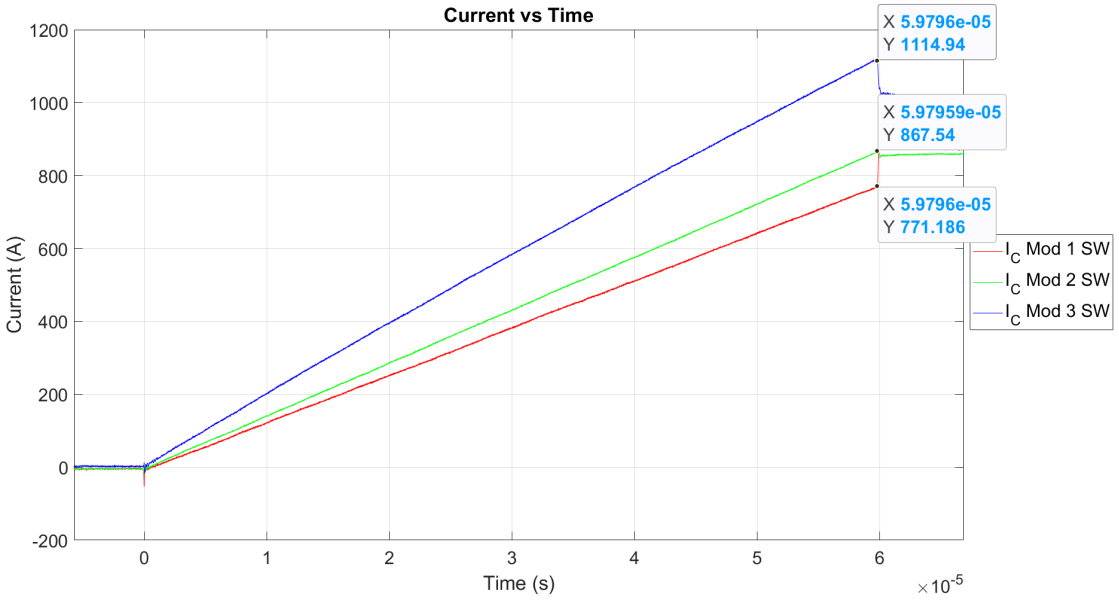
(a) Current Sharing - Variant 3



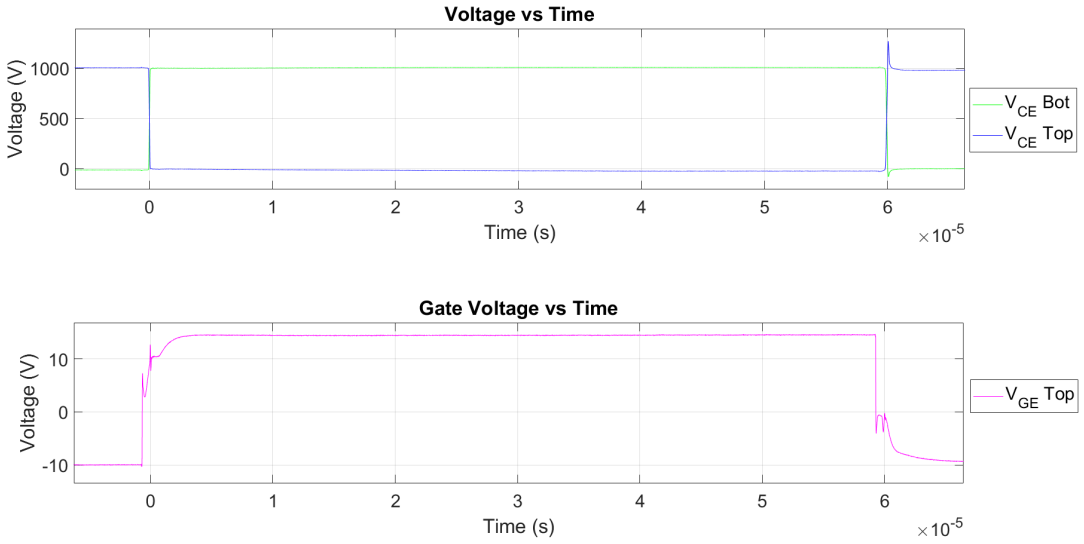
(b) Voltage Graphs - Variant 3

Figure D.6: End-point connection - Variant 3

D.3 End-point connection at z = 103 mm

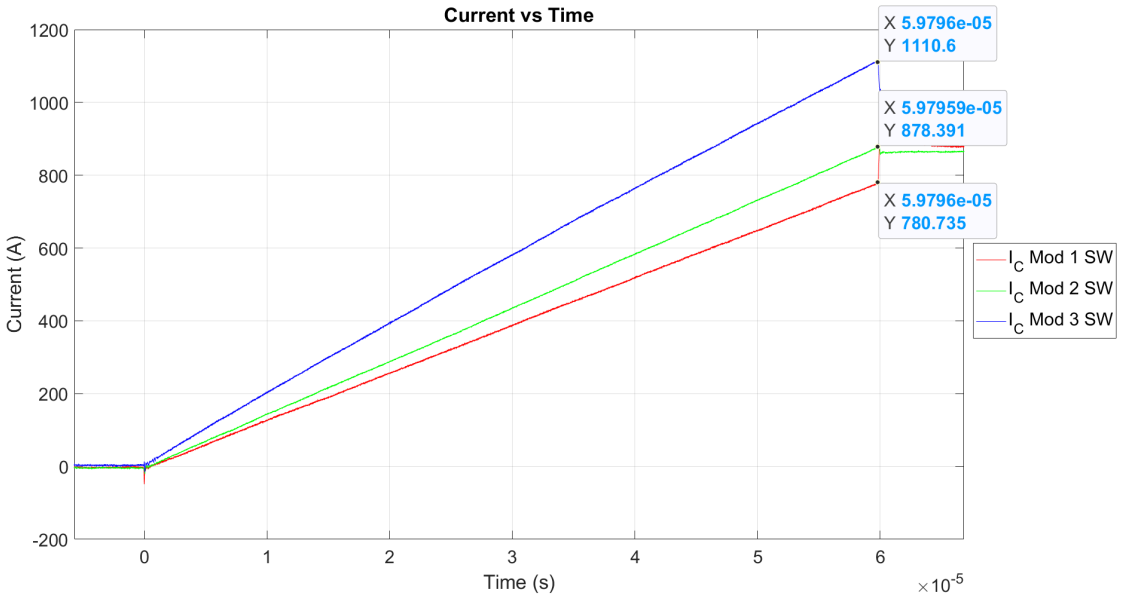


(a) Current Sharing - Variant 1

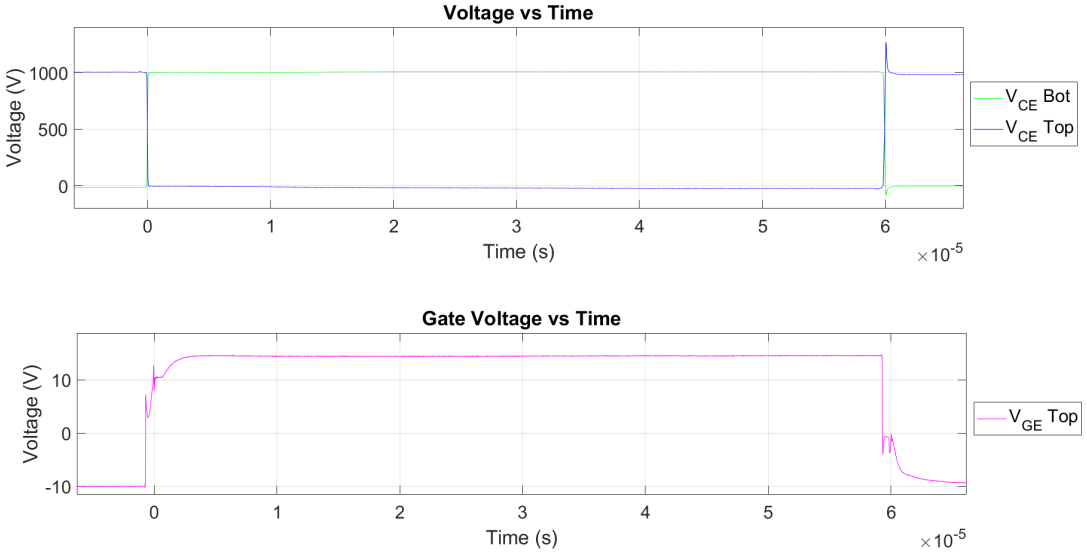


(b) Voltage Graphs - Variant 1

Figure D.7: End-point connection - Variant 1

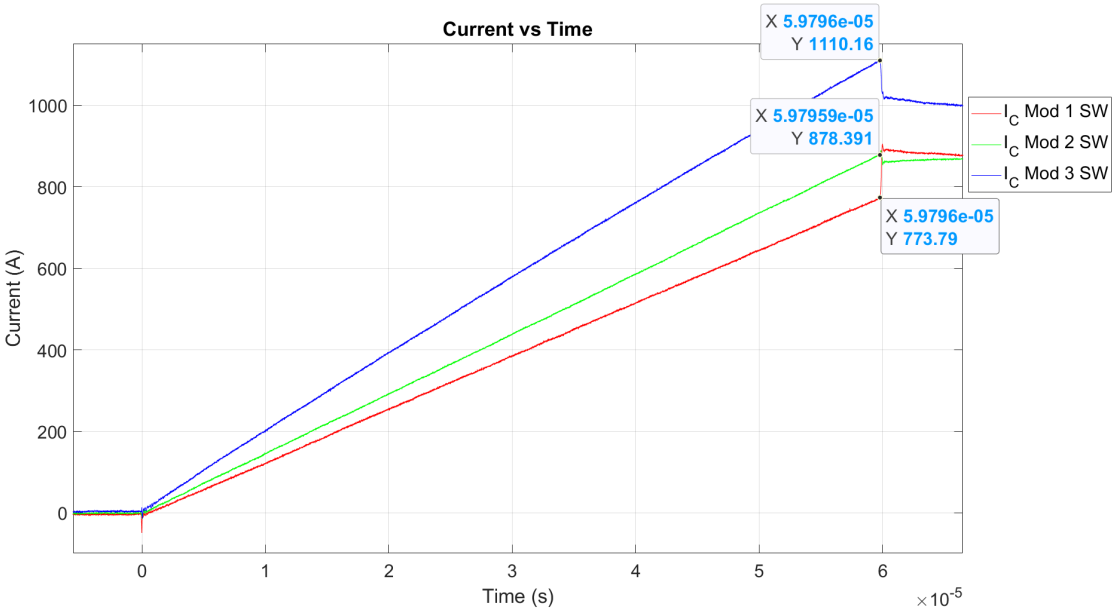


(a) Current Sharing - Variant 2

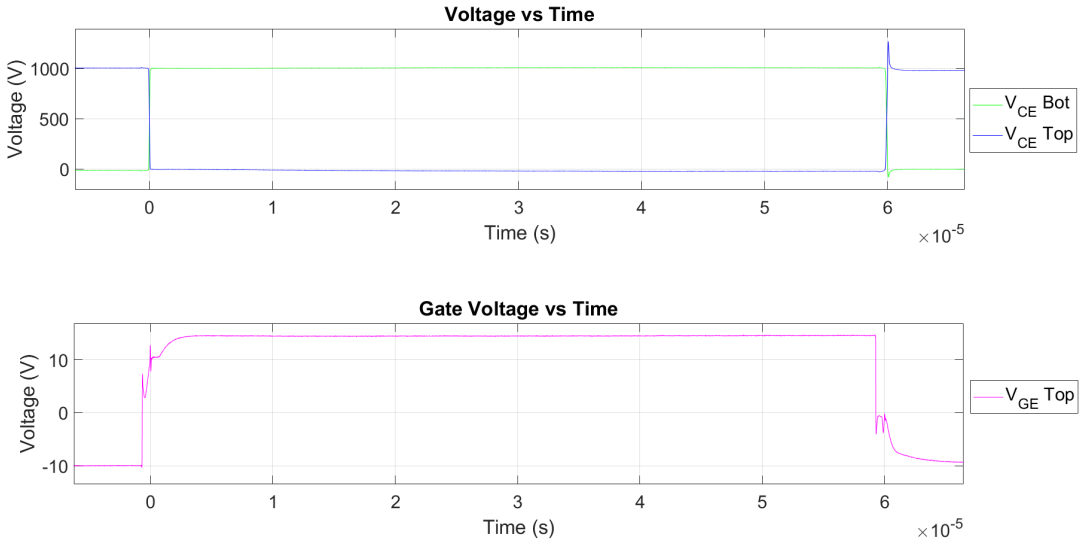


(b) Voltage Graphs - Variant 2

Figure D.8: End-point connection - Variant 2



(a) Current Sharing - Variant 3



(b) Voltage Graphs - Variant 3

Figure D.9: End-point connection - Variant 3