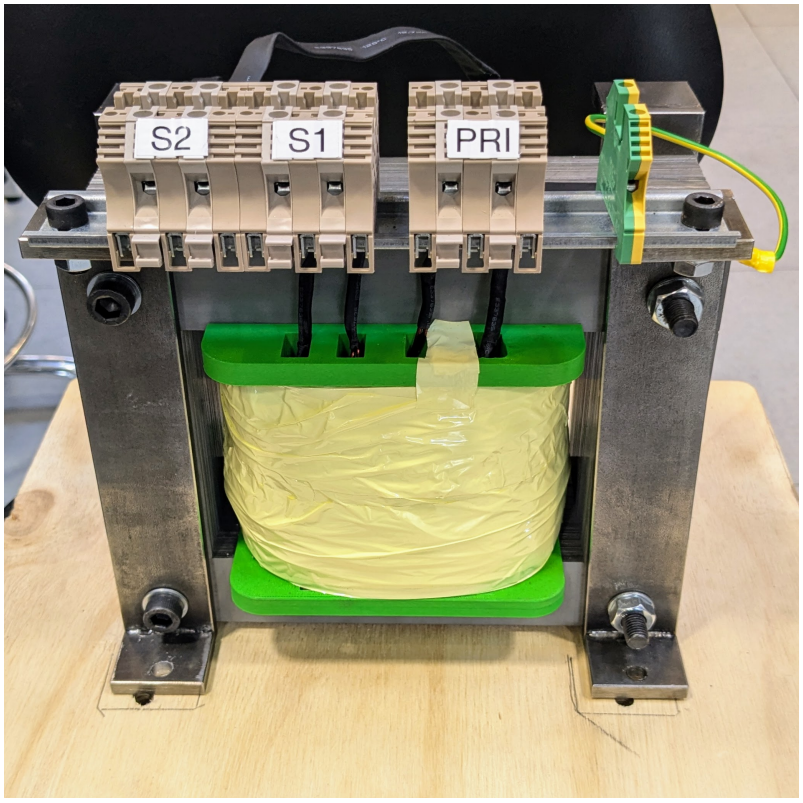

Multiwinding Medium Frequency Transformer for Application in Proposed EV Fast Charging Architecture Incorporating a 400 Hz Microgrid

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Power Electronics and Drives, PED4-1040, 2024-05

Master Thesis

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Abstract:

Electric vehicles (EVs) have witnessed a tremendous growth in the recent years, driven by technological advancements and a global push towards sustainability. DC fast charging alongside has emerged as a promising charging architecture, reducing the charging times and making long distance travel more feasible, but faces issues of reliable protection and metering standards. Another prevalent problem is the different bus voltages of the EVs. This thesis focuses on solving these problems by proposing a DC fast charging architecture based on 400 Hz AC microgrid and multiwinding transformer. The main focus is the design of a 10 kVA multiwinding transformer tested on a dual output SAB converter. Various aspects of the design of the transformer like core material selection, conductor sizing, optimum operating flux density, and manufacturing of the transformer are discussed. The transformer is then tested with open circuit and short circuit tests and on the dual output SAB converter within certain limitations. The results, shortcomings, and possible solutions are highlighted. The thesis concludes as a starting platform for the implementation of the proposed architecture by discussing the faced challenges and extracted learnings.

Index Terms - "Electric Vehicles (EVs) 1 DC fast charging 2 400 Hz Ac microgrid 3 Multiwinding transformer 4 Single Active Bridge (SAB) 5"

Summary

Electric vehicles (EVs) have witnessed tremendous growth in recent years, driven by technological advancements and a global push towards sustainability. Despite the supportive ecosystem, widespread adoption still faces challenges like range anxiety, as current EVs often fall short in range when compared to traditional internal combustion engine (ICE) vehicles [1]. A promising solution to this concern is the deployment of DC fast charging, which significantly reduces charging time and enhances the practicality of EVs for long-distance travel. However, the existing DC fast charging architecture has problems in reliable protection and metering standards. Also, the varying bus voltages in different EVs incept different charging standards and increase the complexity of integration of chargers with EVs [1]. This thesis tries to find a common solution to both of these problems.

The thesis proposes a DC fast charging architecture based on a 400 Hz microgrid with a multiwinding transformer. The proposed architecture takes advantage of the existing work on 400 Hz grids primarily used in aviation to solve the reliable protection and metering standards problem [2] [3], and reduces the complexity of integration of varying EV bus voltages with the multiwinding transformer providing simultaneous charging.

The objective of the thesis is to design and build a three-winding 10 kVA transformer and test it using a dual output Single Active Bridge converter.

The requirements of the system and the transformer are derived by scaling down the specifications of the proposed architecture. The transformer is designed by selecting the core material, the conductors and analyzing the optimum flux density of operation. Calculations are performed to ensure the mechanical integration of the core and the bobbin. The winding strategy is decided taking into consideration the capacitance and the leakage inductance. The values of the estimated leakage inductances and magnetizing inductances are calculated.

The manufacturing methodology of the transformer is discussed and the challenges are highlighted. The transformer is tested for open circuit and short circuit tests, the results are discussed with variation in frequency. All the parameters of the transformer are obtained and the transformer is then tested with the assembled system within its constraints and the results are discussed.

The challenges faced and the leanings obtained during the design and testing are collated and presented. The thesis concludes as a starting platform for the implementation of the proposed architecture. It highlights important learnings and considerations in the direction of successfully testing the proof of concept for the proposed DC fast charging architecture withing its assumptions and limitations.

Preface

This thesis report is made by group PED4-1040 on the 4th semester of MSc in Power Electronic and Drives at Aalborg University. The thesis is conducted in the time period from February through May 2025 accounting for a workload of 30 ECTS points for each participating student. The thesis is therefore officially a short thesis and should be considered as such, within the rules and regulations governing submission of written work.

Acknowledgments

The group would like to express its gratitude to the supervisors for their constant guidance and support.

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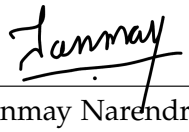
And a heartfelt thanks to Narendra Walawalkar and Shubham Gupta for their constant encouragement, study sessions and motivation.

Reading guide

This summary report is separated into chapters which are numbered progressively. These chapters are further separated into sections. The reference method used in this project report is that of the Institute of Electrical and Electronics Engineers (IEEE). Several appendices are attached.
The following programs have been used during the course of the project:

- Overleaf by WriteLatex Ltd.
- Drawio by JGraph Ltd and draw.io AG
- MATLAB by MathWorks
- PLECS by Plexim
- FreeCAD

Aalborg University, May 27, 2025



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Abbreviations

Abbreviation	Explanation
EV	Electric Vehicle
DC	Direct Current
SAB	Single Active Bridge
CO2	Carbon di Oxide
AC	Alternating Current
PHEV	Plug in Hybrid electric Vehicle
MCS	Megawatt Charging System
DKK	Danish Krone
EU	European Union
SAE	Society of Automotove Engineers
IEA	International Energy Agency
SoC	State of Charge
PEV	Plug in electric Vehicle
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
TAB	Triple Active Bridge
PCB	Printed Circuit Board
PV	Photo Voltaic
ESS	Energy Storage System
BESS	Battery Energy Storage System
MV	Mega Volt
MFT	Medium Frequency Transformer
SST	Solid State Transformer
V_{TH}	Threshold voltage
FEM	Finite Element Model
AFE	Active Front End
PWM	Pulse Width Modulation
NPC	Neutral Point Clamped
CCS	Combined Charging System
NACS	North American Charging System
SiC	Silicon Carbide
SPWM	Sine Pulse Width Modulation
ZVS	Zero Voltage Switching
ADC	Analog to Digital Converter
NTC	Negative Temperature Coefficient

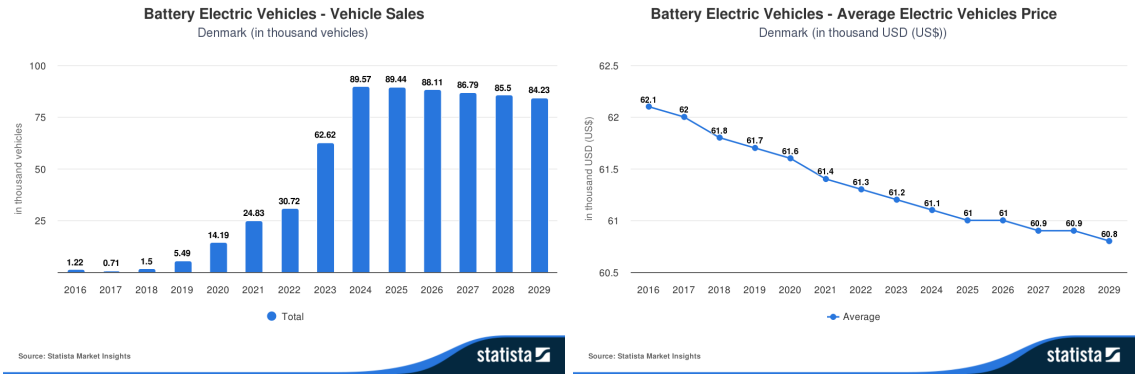
Contents

Chapter 1 Introduction

1.1 State of Art - EV Charging

1.1.1 Current Trends

In the last few decades the world has seen a revolution in electric vehicles to shift from fossil fuels and reduce CO2 emissions. Denmark's strong commitment to sustainability and renewable energy has driven a surge in demand for Battery Electric Vehicles in the country. The Battery Electric Vehicles market (BEV) segment in Denmark is anticipated to witness a remarkable growth in revenue, with projections indicating it will reach US$5.5bn by the year 2025 [4]. The figure 1.1 shows the increasing trend in current and predicted sales of Battery Electric Vehicle (BEV) sales in Denmark. It also shows the current and predicted average price of the BEV which has a decreasing trend. The electrification of the transport industry is also supported by the Danish government in the form of tax benefits for registration and ownership of EV. It can be seen that the current trends converge towards aggressive growth of the EVs in the future.



(a) BEV sales Denmark [4]

(b) Average vehicle price Denmark[4]

Figure 1.1: BEV trends in Denmark

The current EV market trends also point towards a need of growth of the charging infrastructure and technology. The graph 1.2 from European Alternative Fuels Observatory, shows the increase in total number of charging points from 2020 to 2024 in Denmark. The growth in AC charging shows the wide adoption of personal EVs as AC charging is primarily used in homes where owners can charge overnight conveniently. The DC charging is mostly used in fast charging networks installed in public spaces like parking stations and has seen a slow but sure growth. As a part of the green politics for Denmark, the government has allowed giving a discount when charging an EV or PHEV. The government has provided DKK 50 million for public charging stations and other benefits like tax exemption for commercial charging, and subsidy for charge point installation at housing associations etc. to invest and promote the adoption of EVs[5].

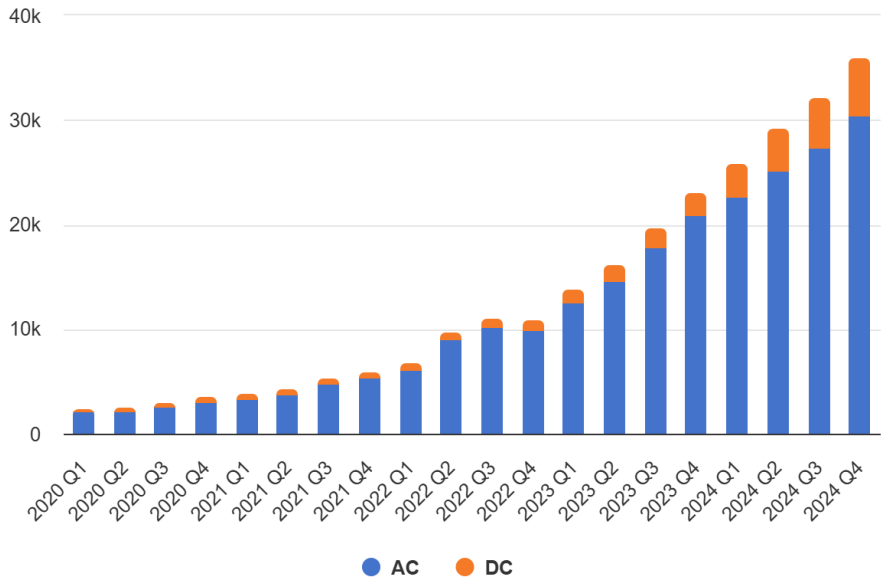


Figure 1.2: EV charging points in Denmark [5]

Despite the current trends and government incentives which are conducive to the growth of the EVs, their wide adoption still faces challenges. Among many, one of the prominent one is the range anxiety [1]. EVs currently fall short in comparison to the traditional Internal Combustion Engine (ICE) vehicles in terms of the time, availability and ease of refueling. While, improvements in battery technology is one solution, the problem could also be reduced by wide spread fast EV charging infrastructure. The Tesla Supercharger [6] which gives a range of about 300 kms in 15 minutes, and ABB Terra HP[7] 350 kW charger are some examples in this direction. Several charging standards supporting fast charging have emerged like CHAdeMO, CCS, NACS, GB/T, CharIN, IEC 6185 etc. which can provide an output power in hundreds of kilo Watts [1]. MCS or Megawatt Charging System has also emerged in the past years which can give an output power in the range of megawatts. These chargers are ideal for charging E-trucks like solutions from Kempower[8] or could have multiple outputs like Alpitronic HYC 1000 [9] which can charge several vehicles simultaneously. This promising fast charging architecture is mainly prevalent in public spaces where it encounters the problem of idling. Establishments like parking stations, tie one parking space to one charger and the later cannot be used if the parking space is occupied. A charging architecture that can charge multiple vehicles in parallel in a short time would decouple the charging spot from the charger, and can partially address the problem of idling. The motivation of this project is to understand the existing issues with the DC fast charging architecture and explore potential solutions to address them.

1.1.2 EV Fast Charging

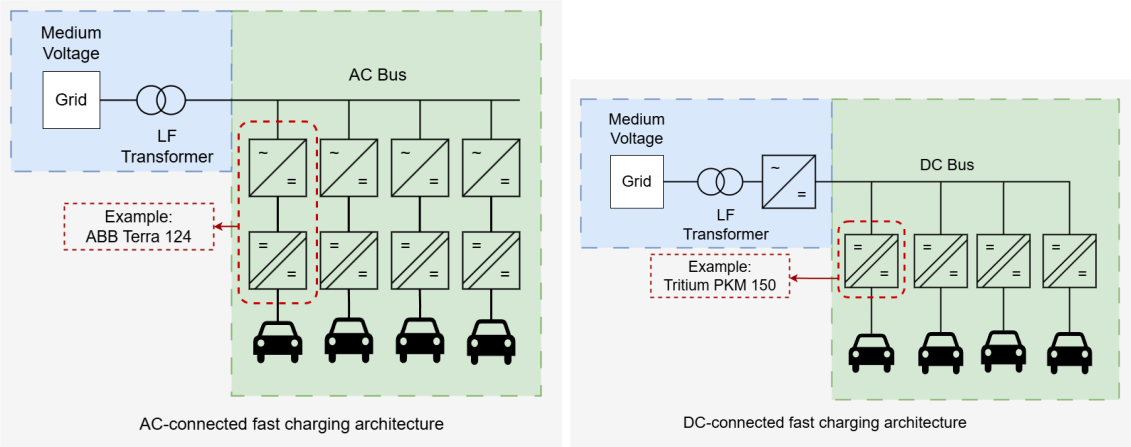
Considering the motivation, fast charging in EVs was decided as the application for this project. This section highlights the background and current scenario, and establishes the need of the intended application.

Background of EV charging
The EV charging is divided into three levels based on the output power. The level 1 and level 2 consists of AC charging which is usually associated with slow charging rates and are characterized by the presence of an onboard charger. The level 3 consists of the DC fast charging and delivers higher power than level 1 and 2. It is associated with off-board charging because of the space requirements at the output power it provides. Another classification consists of 4 different modes of charging depending on the vehicle to grid connection type, safety requirements and output power. Mode 1 and 2 involves charging using a home socket. Mode 3 is one of the most commonly used mode and involves a stationary charging unit. Mode 4 comprises of the DC fast charging.

The SAE J1772 standard used in the United States, Japan, and South Korea, has a maximum power of 1.9 kW in level 1 and 19.2 kW in level 2. The IEC 6185 is the charging standard used in Europe and Australia, has a maximum power of 13.3 kW in mode 1 and 22 kW in modes 2-3. GB/T used in China and India provides a maximum power transfer of 12.8 kW. For DC charging standard CHAdeMO, a standard spread globally offers a maximum power of 400 kW and an output voltage from 50 V to 1000 V. CCS type 1 used in the United States and South Korea and type 2 used in Europe and Australia offer 350 kW maximum power from 200 V to 1000 V output voltage. GB/T adopted in China and India offers a maximum charging power of 237.5 kW with an output voltage from 250 V to 950 V. NACS developed by Tesla offers a maximum charging power of 350 kW with an output voltage from 300 V to 480 V. The megawatt charging system (MCS) was proposed by CharIN and is rated for up to 3.75 MW of charging power with an output voltage of 500–1250 V and an output current of 3000 A[1].

In the above mentioned, the level 1 charging is typically used in home or office spaces, level 2 is private and public outlets, and level 3 in commercial spaces, which is analogous to a fueling station but has a significantly higher cost of investment. Basic home charging stations with 3.7 kW cost approximately US $ 500 in USA, whereas DC fast-charging stations with 300–600 kW power costs $ 12,000–30,000. The cost of constructing and installing high-powered electric vehicle supply equipment (EVSE) is a key factor in the performance of the DC fast charging [10]. As per IEA, in 2021 in Europe, there were 307 thousand publicly available slow chargers and 49 thousand fast chargers [11].

DC fast charging
As mentioned in the motivation, DC fast charging has emerged as a promising solution to the range anxiety issue for the EV owners. The number of fast charging points in Europe have grown eight times from 2015 to 2021 [11].
The DC fast charging stations can be connected to an AC or a DC microgrid and for simplicity, could be referred to as AC-connected and DC-connected fast charging networks. The figure 1.3 shows both of these architectures. Currently, AC-connected architecture is more widely adopted because of the reliable protection and metering standards, but requires an AC-DC conversion stage for each charger, increasing cost and reducing efficiency. On the other hand, the DC-connected architecture requires only one rectification stage, but lack protection and metering standards [1].



(a) AC-connected fast charging architecture **(b)** DC-connected fast charging architecture

Figure 1.3: DC fast charging architectures [1]

1.2 Problem Formulation

This section aims to define the problem statement and constraints the project into objectives. The process starts with establishing a background which is mentioned in the motivation and application and identifying the existing problems. The crux of this process is defined as the problem statement that the project then intends to solve. Possible solutions are hypothesized which translate into the project objectives. At this point, the project has a well defined direction which has emerged from a real-world problem. The scopes, limitation, and assumptions are defined next to have clear and concise boundaries.

Problem identification

As mentioned in the previous section, the AC-connected and DC-connected architectures have certain advantages and disadvantages. While AC-connected systems are more adopted as they provide reliable protection and metering standards, they come with added cost and an extra conversion stage of rectification on each output instead of a central rectification stage. The DC-connected architecture reduces the rectification stage for each charger but has problems with protection and metering standards, making the prior more prevalent.

Another problem prevalent in the EV charging is the different bus voltages of the EV powertrain. Traditionally EVs operated on a bus voltage of 400 V like Tesla Model 3 and Nissan Leaf, but 800 V EVs have also emerged like the Porsche Tycan [1]. This creates a compatibility issue for the chargers because of the absence of a common voltage level. The article [12] discusses some solutions until the charging architecture achieves this compatibility. One solution is to split the battery into two 400 V sub modules but presents a challenge to control and equalize the State of Charge (SoC) between the two sub modules. Another solution would be to use a dedicated onboard DC/DC converter that requires high power density and low cost which is difficult to achieve. The article proposes a solution where the electric drive of the vehicle, consisting of the inverter and the electric motor, is reconfigured into a multiphase DC/DC boost converter, adapting the battery voltage to the off-board charger

Since the DC fast charging is primarily used in public spaces, a problem arises on the planning part of the facility and real use case of the same. [13] discusses the problem of idling of PEVs in public charging spaces. Here the charging port is tied with the parking spot and the former can be left unused if the later is occupied by a PEV which is currently not charging. The architectures discussed in the article try to decouple the charger and the parking spot by multiple mechanical connections. The authors propose a multiple charger multiple port system and a planning model for coordinated charging. It would not be wrong to assume a similar problem of idling of EVs in public charging spaces would arise in the fast charging networks as their usage increases.
There are existing solutions present in the market for simultaneous charging of vehicles meaning that the charger could serve more than one parking spots [14],[15]. This is highly advantageous as it decreases the cost of investment of the charging infrastructure. These solutions have multiple modules connected in parallel and divide the power among the several vehicles connected to them. This means that the charging power is less during simultaneous charging compared to standalone charging.

Possible solution
A charging architecture which could take the protection and metering advantages of AC-connected system without increasing the number of power conversion stages would be ideal to solve the problem of lack of protection and metering standards in DC-connected architecture and the extra conversion stage in the AC-connected architecture.. Furthermore, if the charging architecture could provide simultaneous charging without power reduction and could cater to different bus voltages would be highly advantageous.

Referring to the figure 1.3 a possible architecture could be to have a single DC-AC converter instead of having it for each charger and form a AC microgrid. A multi-winding transformer could be used instead of an individual transformer for each charger, that would cater to different bus voltages and could also provide simultaneous charging without the reduction in power. For the current DC fast charging architecture two different transformers would be required to cater to different EV bus voltages which could be done by a single multiwinding transformer. An AC to DC conversion stage would be present after the multiwinding transformer in the proposed architecture which is similar to the DC fast charging architecture with individual chargers. In the current DC fast charging architecture the individual DC-DC converters operate at high frequencies which would be non-ideal over long distances to form the AC microgrid because of the high impedances. Using a frequency of 50 Hz is an option but this would mean bulky transformers and would be disadvantageous in terms of space and material. IEC 61851-23 states that DC fast charging stations with multiple outputs require isolation in each output, and hence the transformer cannot be eliminated. A possible solution would be operating at a medium frequency such as 400 Hz which could be transmitted over the area of the charging station and would also not have a bulky transformer. The figure 1.4 shows the architecture discussed above.
One possible argument in the negation of the proposed architecture would be that the DC-AC conversion stage would have to be rated for much higher power than the other architectures having DC-AC conversion stage for each charger. This is because in the current DC-fast charging architecture, each charger has an exclusive DC-AC conversion stage delivering power to one EV, however in the proposed architecture, the common

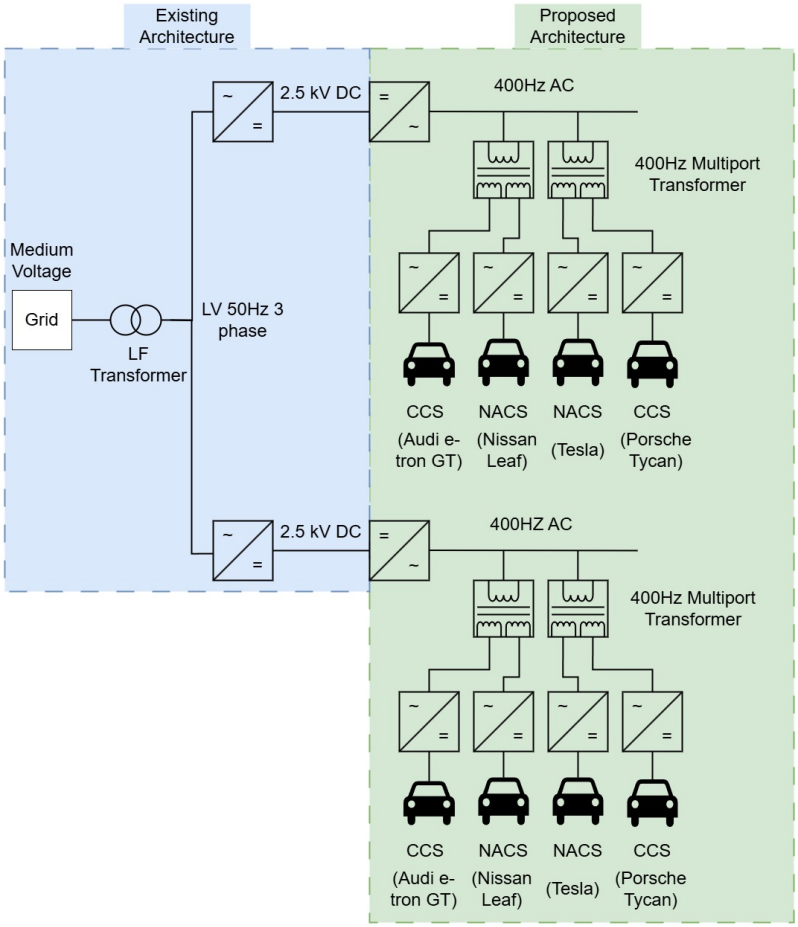


Figure 1.4: Proposed architecture with 400 Hz AC microgrid and multi-winding transformer

DC-AC conversion stage would provide power to all the EVs The Application section 1.1.2 mentions the Megawatt Charging System which would also require high power converters. Companies like Kempower[8], Siemens[16], and ABB[17] have taken strides in achieving this power level. With these facts and growing efforts for high power semiconductor switches, a fair assumption could be made that the converters required for the DC-AC conversion stage in the proposed architecture would be technologically and financially feasible.
To condense, the proposed architecture would have the following advantages.

- Reduce the number of converters and High-Frequency transformers.
- Simultaneous charging of EVs could be achieved.
- Take advantage of the protection and metering standards available for AC.
- Cater to different levels of bus voltages of EV powertrain.

Selection of 400 Hz **frequency** The considerations for the selection of frequency were that it would have to transmit power over the entire charging station and be beneficial in terms of space and cost. A 50 Hz multiwinding transformer would be too bulky

and expensive compared to a 400 Hz transformer. Also, 400 Hz frequency is very commonly used in the aircraft industry as mentioned in [2].The article discusses in detail the 400 Hz electrical distribution systems for the aerospace industry. The article [3] proposes a 400 Hz AC system to distribute power to all CMS (Compact Muon Solenoid) sub detectors at CERN. The paper presents the proposed power distribution system and describes the design considerations for distributing power quality to the front-end electronics at CMS. The article [18] discusses a 415 Hz power system for mainframe computer systems in 1989. It can be understood that comprehensive work has been done for establishing a 400 Hz distribution system in the literature which would serve as the building blocks for the architecture being proposed in this project. A fair assumption would be that the protection and metering standards would be well established for this medium frequency, which eliminates one of the current problems of the DC grid.

Problem Statement The aim of this project is to propose a solution for the following problems:

- Lack of reliable protection and metering standards in the current DC fast charging architecture.
- Simultaneous charging of EVs with varying powertrain bus voltages.

Primary Objective : The primary objective of the project is to design and build a 3 winding 10 kVA transformer and test it in a Single Active Bridge converter with two outputs which could serve as a part of proof of concept for the proposed architecture.

1.2.1 Scopes, constraints, and assumptions

- The scope of the project is limited to the transformer and the SAB converter. It will not explore the design of the entire proposed architecture and its associated sections and components.
- The analysis of the effect of the proposed architecture on the grid is out of the scope of this project.
- The project will not have active bridges on the secondary side, and the controls and modulation of this kind of converter, namely the Triple Active Bridge (TAB) is out of the scope of this project.
- The thermal aspect of the transformer design and its solutions are not in the scope of this project.
- The project assumes that having a single DC-AC conversion stage for the entire charging network would be technologically and financially viable.
- The project assumes that the protection and metering standards would be present or could be extended for 400 Hz frequency for the required power levels.
- The selection of the core material will be a constraint of ease of availability and procurement, as the project has definite timelines.
- The transformer will be manufactured manually and will not be able to control the transformer parameters accurately.

Chapter 2 State of the Art

This chapter presents the specific state of the art for different sections of the project. The system architecture consists of the details for the possible architecture options connected to the secondary side of the transformer. The sections Multiwinding Transformers discuss the current state-of-the-art in the respective area. The purpose of this section is to have a better understanding of the topics before the design, to have better arguments for the proposed architecture, and extract information useful for the design.

2.1 System Architecture

The secondary sides of the multiwinding transformer, need to be connected to a rectifier for delivering controlled DC power to the battery. This can be done by using active bridges or by using a combination of diode rectifiers and non-isolated DC-DC converters. For the active bridges, one such topology is the Triple Active Bridge (TAB) converter.
Article [19] analyzes the TAB shown in Figure 2.1 converter as a candidate for a multiport converter for integration of EV chargers with DC traction supply systems used for the stationary charging of EVs. It determines the critical length of the overhead trolley grid section below which the three-port converter is more efficient than the two-port converter based integration of EV charger.
Article [20] presents a novel multi-port multi-cell (MPMC) topology, which combines the features of two independent two-port converter systems, which are commonly used in state-of-the-art EVs. It also introduces a control strategy for the MPMC topology proposed. The building blocks of this converter are series and parallel connected TAB converters.
Article [21] proposes an isolated multiport converter based on TAB with power flow in multiple directions which integrates EV charging with Energy storage systems and PV cells. The topology uses buck and boost converters after the rectification by the active bridge to meet the required power levels. Paper [22] also integrates the EV charging with ESS system and an MV grid using the TAB architecture. Furthermore, an enhanced power flow management strategy is presented for the TAB converter to optimize the integration between EVs and BESS.
The problem of different voltage levels of charging prevalent in the industry is addressed in the article [23], which proposes a TAB converter and a MFT of 50 kHz. It provides modeling and simulation of the system. It solves one of the problems on which this project is based on, but does not take a microgrid approach as taken in this project. Article [24] also proposes charging of two EVs using a TAB, but focuses on the control strategy. The converter is controlled using a hybrid scheme comprising of proportional-integral (PI) and deep reinforcement learning (DRL) algorithm to improve the charging efficiency of two electric vehicle batteries and provides simulation results for the same.

It is very evident that the TAB is a popular choice when dealing with a multiport converter architecture whether to integrate different power sources to manage the peak power demand, or to improve efficiency and reduce components by eliminating the use of two DABs, or to meet different voltage requirements for EV charging. Though it posses the problem of circulating current as discussed in [25], the TAB could be a promising topology to implement in the proposed architecture in the project.

Another approach to the architecture is to achieve the rectification stage on the secondary sides by the use of diode bridges and control the output power using a DC-DC converter

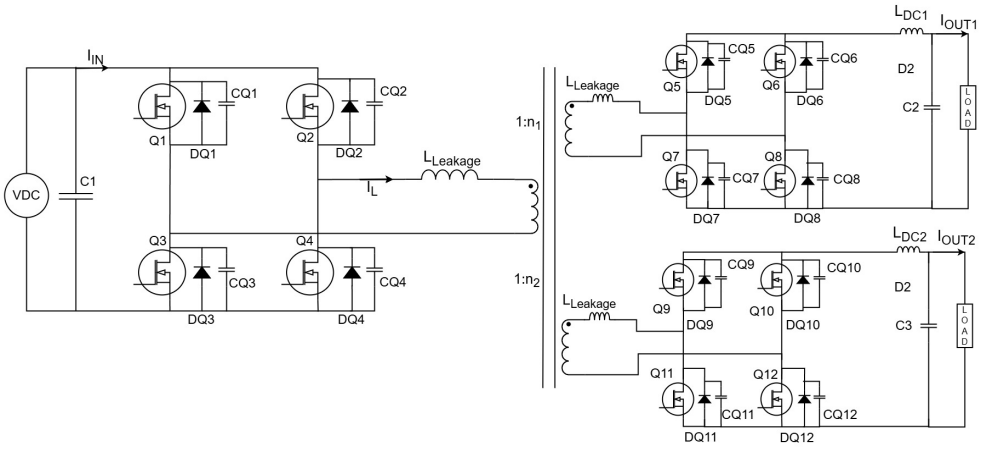


Figure 2.1: Triple Active Bridge

like the buck converter. The article [26] proposes a similar architecture. The proposed topology consists of an LLC resonant converter with dual secondary sides; two interleaved triangular current mode (TCM) buck converters, and three additional auxiliary switches for reconfiguration. It uses a similar topology to TAB but uses a resonant power converter and replaces the active bridges on the secondary sides with diode rectifiers and buck converters. The paper models the converter and also shows the experimental results over the load range from 400 W to 11 kW. This architecture would be easy to implement and control for the proposed EV charging system in the project. Also, this would be an extension to the system on which the transformer is being tested for the project.

2.2 Multiwinding transformer

This section presents the literature and state of art for the multiwinding transformer design.

The article [27] presents a physically based electrical model of a high voltage multi winding transformer. Each component in the electrical model corresponds to a physical quantity of the transformer. A method is also presented to calculate the leakage inductance for non uniformly spaced windings. The final electrical model is derived directly from the actual magnetic structure under investigation, and all the parameters in the model have a one-to-one relationship with corresponding physical quantities in the original magnetic structure. The magnetic equivalent circuits are translated into electrical equivalent circuits using the Duality theorem.

Article [28] presents an equivalent circuit for the leakage inductance of a three-winding transformer. The model is also derived from the principle of duality and matches the terminal leakage inductance measurements. It starts by discussing the traditional equivalent circuit for a three-winding transformer and explains the reason for the negative inductance. The duality model is then explained, and the limitation of the model is explained in the estimation of the leakage inductance. A new duality-derived model is presented which matches the values of the terminal model, by expressing one of the inductance as mutual inductance between the other two windings. It also discusses the interpretation of magnetizing components based on the transformer's geometry. The equivalent circuit presented in the paper is shown in the figure 2.2. In the article [29], the above approach is generalized for a transformer with n windings. Both articles also discuss the procedure

for terminal measurements used to calculate the leakage inductances.

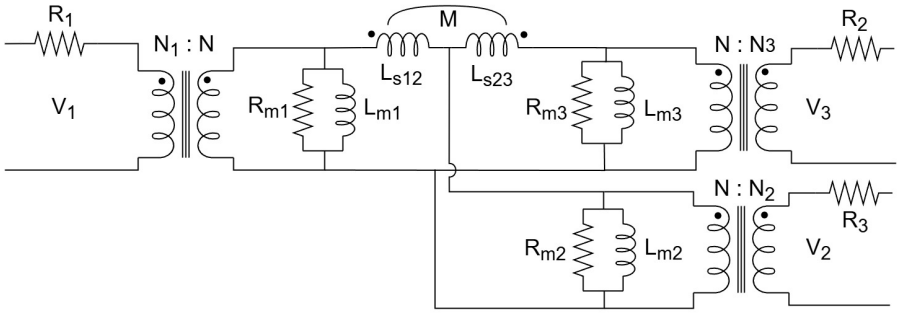


Figure 2.2: 3 winding transformer equivalent circuit [28]

The article [30] presents a solution to adjust the leakage inductances in a multiwinding transformer. The method is based on the use of split and partly overlapping windings. It is suitable for transformers with both even and uneven transformation ratios. As the method is based on fundamental geometrical properties, it is relatively robust. The concept has been tested with a 4-winding transformer with different voltage transformation ratios.
The article [31] presents the deign for high frequency multiport SST. The key takeaway from the paper was the core selection, where four different core materials are compared on different aspects. The paper also discusses cable selection and the placement strategy for the windings.
A method for determining leakage inductances of a single phase multiwinding transformer is presented in [32]. The paper uses the mathematical model of the transformer to represent the leakage and the magnetizing inductances in a matrix form and uses 3D FEM simulation to calculate them.
The above literature helps to understand the multiwinding transformer on a deeper level and also helps in deciding the nature and sequence of it's testing.

Chapter 3 Dual Output SAB system

This chapter presents an overview of the system being built and tested. It starts with the system diagram, and then identifies each component of the same.

3.1 System Diagram and specifications

The figure 3.1 shows the dual output SAB system on which the transformer is tested. The input of the system is constant DC power from a power supply. In the intended application, the rectification stage will be performed by an Active front end (AFE) such as PWM rectifier, NPC converter, Vienna rectifier, etc., as mentioned in [1]. The DC power is fed in to a single-phase full bridge inverter whose output is 400 Hz AC. The transformer then steps down this AC power into two parallel outputs of 400 Hz of different voltage levels with a ratio of 2.5:1 and 5.2:1 (The calculations are discussed in the next section 3.1.1). Both outputs are then rectified using full-bridge diode rectifiers, filtered using a second order filter connected to the load. In the intended application, the rectification could be performed by active converters to control the output power levels, which is out of the scope of this project; hence, for simplicity, diode bridge rectifiers are used in the project. Again, for simplicity, a resistive load will be used in this project instead of a battery owing to the complex control algorithms.

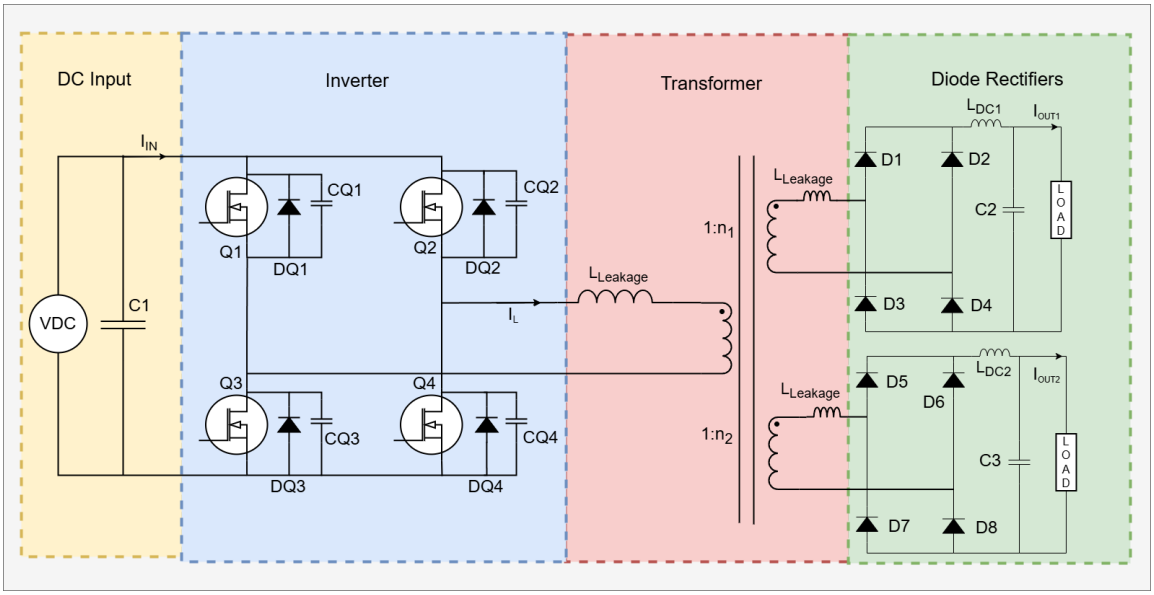


Figure 3.1: Dual output SAB system

3.1.1 System specifications

It is of prime importance to establish the power levels of the different conversion stages for the proposed charging architecture to derive the specifications of the corresponding components of the system. As per [33], a typical EV fast charging site requires a power of about 1.5 MW to 3 MW when all stations are operated in parallel. This power will be distributed using the 400 Hz microgrid. The voltage level of this microgrid needs to be decided accounting for the length of the wiring and the corresponding voltage drop. The article [18] gives the impedance per 100 ft of copper three conductor jacketed cable at 415 Hz inside a rigid aluminium conduit. Assuming a total wiring length of about 100 m (300 ft), voltage drop for a voltage level of 2.5 kV can be calculated as,

$$Current \cdot length\ of\ wire \cdot impedance\ of\ wire\ per\ unit\ length = Voltage\ drop\ across\ the\ wire \tag{3.1}$$

i.e.

$$1000A \cdot 0.00023 \cdot 300 = 61V \tag{3.2}$$

The obtained voltage drop for a 4/0 AWG wire is about 2.5% of the bus voltage.
To decide on the transformer specifications, it was decided that the system would emulate the outputs of two different charging standards, the CCS and the NACS. The former has a maximum bus voltage of 1000 V with 350 kW of power and the later has a maximum bus voltage of 480 V with 250 kW of power.
The following calculations show how the parameters of the system are obtained. As stated before, assuming a bus voltage of 2500 V for the AC grid and the voltage levels of the CCS and NACS, the ratios obtained are,

$$N1 = \frac{Bus\ Voltage}{CCS\ Voltage} = \frac{2500}{1000} = 2.5 \tag{3.3}$$

Similarly,

$$N2 = \frac{Bus\ Voltage}{NACS\ Voltage} = \frac{2500}{480} = 5.2 \tag{3.4}$$

To obtain the voltages of the transformer, the above ratios are applied to 750 V, giving 300 V, and 144 V. The output current is calculated by obtaining the ratios of the powers for NACS and CCS systems as follows.

$$Power\ for\ CCS\ output = \frac{CCS\ power \cdot SAB\ power}{CCS\ power + NACS\ power} = \frac{350kW \cdot 7500}{350kW + 250kW} = 4.375kW \tag{3.5}$$

Dividing by the output voltage of 300 V, the current comes out to be 14.6 A. Similarly, for the output emulating NACS the power can be calculated as follows.

$$Power\ for\ NACS\ output = \frac{NACS\ power \cdot SAB\ power}{CCS\ power + NACS\ power} = \frac{250kW \cdot 7500}{350kW + 250kW} = 3.125kW \tag{3.6}$$

Dividing by the output voltage of 144 V, the current comes out to be 21.7 A.
The requirements are condensed in the table 3.1. The values in the table represent the maximum values.

Parameter	Value	Unit
Input voltage	750	V
Input current	10	A
Input power	7.5	kW
Output 1 voltage	300	V
Output 1 current	14.6	A
Output 1 power	4.4	kW
Output 2 voltage	144	V
Output 2 current	21.7	A
Output 2 power	3.1	kW

Table 3.1: System specifications

3.2 Component Identification

This section presents the details and workings of the different components of the system essential for power delivery. The section only introduces these parts of the system to have an overview while reading. Each of these part, with different detail levels is further discusses in the thesis. These components are finally assembled together and tested as discussed later in the thesis.

3.2.1 Full Bridge Inverter

In the charging system proposed in the problem formulation 1.2, the rectified DC voltage needs to be converted into 400 Hz AC which will form the microgrid used to transmit power to the individual charging stations. For this project, this conversion is achieved by a single-phase full-bridge inverter based on SiC MOSFETs full bridge module from Wolfspeed. The specifications of the same can be found in the table 3.2

Parameter	Value	Unit
Part number	CBB032M12FM3	
Max Voltage	1200	V
Rds ON	32	mΩ
Max Drain Current	39	A
Max temperature	150	°C

Table 3.2: Full-bridge module specifications

Modulation strategy

The purpose of the converter in the project is twofold; it presents a proof of concept for the proposed charging architecture, and it provides a platform to test the transformer. The later, motivates having different modulation strategies to compare the performance of the transformer for each. The project will use phase-shifted modulation and Bipolar SPWM, thus enabling comparison of the transformer's performance on a square wave and a sinusoidal wave. Based on these, the project could serve as a starting point to implement ZVS, taking into account the leakage inductance of the transformer.

3.2.2 Multi-winding Transformer

The multi-winding transformer performs the power division and voltage and current transformation and is the prime focus of this thesis. The design, manufacturing and testing of the transformer are discussed in detail in the sections 4.1.1, and 6.1.

3.2.3 Rectification and Filtering

In the proposed architecture, the rectification could be achieved by either active bridges or by a combination of diode rectifiers and DC/DC converters in line with the battery charging algorithm as mentioned in section 2.1. The project limits itself to rectification by full bridge diode rectifiers for simplicity. The specifications of the rectifier used can be found in the table 3.3.

Parameter	Value	Unit
Part number	APTDF200H60G	
Peak reverse voltage	600	V
Max average forward current	270	A
Max diode forward voltage	2	V

Table 3.3: Diode rectifier specifications

The filtering of the output voltage and current is performed by a second order LC filter discussed in section 4.2.

Chapter 4 System Design

4.1 Transformer Design

This section discusses the design, calculations, and manufacturing of the transformer. The design methodology presents the requirements, mathematics, and considerations such as proximity and skin effects. The Transformer manufacturing entails the manufacturing methodology, winding strategy, and deviations from the ideal manufacturing that lead to differences from the design.

4.1.1 Transformer Design Methodology

Transformer Theory

The simplest form of a transformer can be thought of as two different coils that share a common magnetic flux. When this shared or mutual flux produced by the first coil varies in time, there is an induced voltage in the second coil, following Faraday's law of induction. This voltage produced is directly proportional to the rate of change of flux and the number of turns in the second coil.

A magnetic material or core, which essentially is a material that offers high permeability to magnetic flux, can be used to confine the majority of the flux in a well-defined path under the maximum flux limits of the material. This reduces the leakage flux (flux that is not common to both coils) and increases the induced voltage.

The fig 4.1 shows the basic structure of the two-winding transformer wound on a core material. The primary coil, consisting of N_p turns is connected to a voltage source V_p varying in time, providing a current of I_ϕ responsible for producing the magnetic flux ϕ in the core (assuming no leakage flux). e_p is the induced voltage in the primary coil, produced because of V_p, and can be expressed as follows.

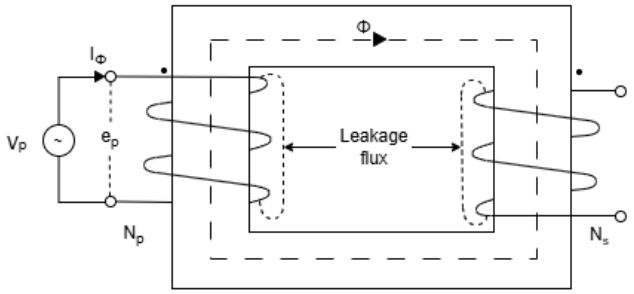


Figure 4.1: Two Winding Transformer

$$V_p = e_p = N_p \cdot \frac{d\phi}{dt} \tag{4.1}$$

Flux density, B is defined as flux per unit area, A_c. The area here would be the area of the core material.

$$B = \frac{\phi}{A_c} \tag{4.2}$$

By 4.1, and 4.2,

$$V_p = e_p = N_p \cdot A_c \cdot \frac{dB}{dt} \tag{4.3}$$

The rate of change of flux depends on the rate of change of the V_p. For a sinusoidal variation with frequency ω, the rate of change of flux becomes,

$$\frac{dB}{dt} = B_{max} \cdot \omega \cdot cos(\omega.t) \tag{4.4}$$

where B_{max} is the peak value of the flux density produced by V_p.
The equations 4.4 and 4.3 give the peak value of the induced voltage, $e_{p,max}$

$$e_{p,max} = N_p \cdot A_c \cdot B_{max} \cdot \omega \tag{4.5}$$

Expressing in terms of RMS value and linear frequency,

$$V_{p.RMS} = e_{p,RMS} = 4.44 \cdot N_p \cdot A_c \cdot B_{max} \cdot f \tag{4.6}$$

For a voltage varying as a square wave, the rate of change of flux density will be,

$$\frac{dB}{dt} = \frac{2 \cdot B_{max}}{t/2} \tag{4.7}$$

This gives the induced voltage as,

$$V_p = e_p = 4 \cdot N_p \cdot A_c \cdot B_{max} \cdot f \tag{4.8}$$

The equation for the induced voltage can be generalized as,

$$V_p = e_p = k_v \cdot N_p \cdot A_c \cdot B_{max} \cdot f \tag{4.9}$$

where k_v is the waveform factor depending upon the nature of the variation of the input voltage and hence flux density, and is summarized in Table 4.1.

Type	k_v
Sine input	4.44
Square input	4

Table 4.1: k_v values for sine and square inputs

The same equation can be used to obtain the induced voltage in the secondary winding of the transformer. It can be seen that the voltage per turn produced depends on the A_c, B_{max}, and f. Transformers operating at higher frequencies have a higher voltage per turn ratio and are smaller in size. The term B_{max} is critical to the selection of the core material and also the core losses produced in the transformer.
The ratio of the primary and secondary voltages and currents can be found by the equations 4.8 and 4.9.

$$\frac{V_p}{V_s} = \frac{I_s}{I_p} = \frac{N_p}{N_s} \tag{4.10}$$

The above basic theory can be extended to multi-winding transformers. In this case, for a transformer with a single input or primary and two outputs or secondary, the ratios can be expressed as follows.

$$\frac{V_p}{V_{s1}} = \frac{N_p}{N_{s1}} \quad \& \quad \frac{V_p}{V_{s2}} = \frac{N_p}{N_{s2}} \tag{4.11}$$

And, considering the division of power in the secondaries the current ratio will be as follows

$$N_p \cdot I_p = N_{s1} \cdot I_{s1} + N_{s2} \cdot I_{s2} \tag{4.12}$$

Core Selection

The selection of the core material could be regarded as the most important design decision, as it affects important parameters like the size, cost, and power losses of the transformer. The selection of core material is governed by the maximum flux density B_{max}, operating frequency f, power losses, cost, and availability. Articles [31], [34], [35], and [36] discuss the selection of core material for medium and high frequency transformers. The four common materials considered are Silicon steel, Ferrite, Amorphous, and Nanocrystalline. The table 4.2 shows the comparison of these core materials.

	Si Steel	Ferrite	Amorphous	Nanocrystalline
Frequency	<1 kHz	< 100 MHz	<300 kHz	<30 kHz
Flux density (T)	1.5–1.8	0.2–0.5	0.5–1.6	1–2
Core losses	High	Low	High	Low
Cost	Low	Low	Medium	High

Table 4.2: Core material comparison

The availability of the core material was the most critical part for the core selection for the project. Owing to this M 165-35S Silicon steel from Wassner was selected, which was readily available. The details of this core material can be found in the Appendix.

Transformer Specifications

After the selection of the core material, the next step is to establish the specifications of the transformer to enable the cable selection and core geometry. Based on the system requirements from table 3.1, assuming a 0.8 power factor, the transformer kVA rating for square wave comes out to be 9.4 kVA. The voltage and current specifications are condensed in table 4.3. The specifications are represented in the peak value of the square wave.

Parameter	Value	Unit
Input voltage	750	V
Input current	12.5	A
Input power	9.4	kVA
Output 1 voltage	300	V
Output 1 current	18.8	A
Output 2 voltage	144	V
Output 2 current	27.5	A

Table 4.3: Transformer specifications

Cable Selection
Another important design decision is the cable selection for the transformer. At medium and higher frequencies, the AC resistance of the wires changes due to the skin effect and the proximity effect. The cable selection also determines the copper losses in the transformer and contributes to the overall efficiency.

Skin effect: There is a concentration of current near the wire surface at higher frequencies, which is termed the skin effect. This is the result of magnetic flux lines that generate eddy currents in the magnet wire. Skin effect accounts for the fact that the ratio of effective alternating current resistance to direct current is greater than unity. The skin depth is defined as the distance below the surface where the current density has fallen to $1/\epsilon$ or 37 percent of its value at the surface. [37].

$$\epsilon = K \cdot \frac{66.2}{\sqrt{f}} \tag{4.13}$$

where f is the operating frequency, and K is 1 for copper. At 400 Hz the value of the skin depth is 3.31 mm. Using a wire that has a smaller diameter than the skin depth would mean that the current density would remain same in the entire cross section and the skin effect would be reduced significantly.
Based on the availability of the magnet wire for the length required (which is calculated later in this section), lacquered copper wire of diameter 1.8 mm was selected. To meet the current specifications, multiple wires are wound in parallel to achieve the required current density. For the secondary winding with higher current, a copper sheet with 0.45 mm thickness, which was readily available was selected. The current density was taken to be $5\,\mathrm{A/mm^2}$ with a width of 10 mm. Generally the current density has a range of $1\,\mathrm{A/mm^2}$ to $5\,\mathrm{A/mm^2}$ depending upon the placement and cooling.

Area Product and Window Area
From equation 4.9, to obtain the voltage per turn, there are two parameters that can vary, area of core A_c and the maximum magnetic flux B_{max}. Varying these two parameters will affect the number of turns. A high value of B_{max} would reduce the number of turns and the core area but would lead to higher core losses. A larger A_c would mean less number of turns and lower B_{max} but less space for winding for a given geometry and a bulkier transformer. Low value of both these parameters would mean a higher number of turns increasing copper losses, increasing cost and making the transformer bulky. To find a harmony between these parameters, traditionally the approach of area product is widely adopted. The area product is defined as the product of the window area W_a and the core area A_c. Window area is the available area for the windings for a given geometry of core. The Area product (A_p) can be mathematically derived from the equation 4.9 and can be expressed as,

$$A_p = \frac{\Sigma VA}{k_v \cdot k_u \cdot B_{max} \cdot f \cdot J_o} \tag{4.14}$$

where,

$$\Sigma VA = N_p \cdot I_p + N_{s1} \cdot I_{s1} + N_{s2} \cdot I_{s2} \tag{4.15}$$

k_u is the window utilization factor which is the ratio of total conductor area to the total window area, and J_o is the common current of the conductor common for all windings.

Transformer Calculations
Now that the requirements, core material selection, and conductor selection is concluded, the transformer calculations could be performed to determine the number of turns, operating B_{max} and core geometry selection. It is important to understand that the selection of the mentioned parameters is an iterative process owing to the different combinations. The approach in the project was not to select the most spatially efficient parameters but to select something that could be used with surety and with a margin of safety for errors.

The core geometry selection was a decision based on the availability and procurement time. Custom cut cores take time to manufacture and could cause delays. Hence, it was decided to select EI240 core geometry readily available from the Waasner catalogue (Image of the catalog in the appendix). This resulted a fixed area of core of 64 cm^2 considering a square geometry for the same. The performance details for the core M 165-35 S at 400 Hz was provided by Waasner (can be found in appendix) which included a Magnetic filed density (B) vs Power Loss (P_s) per kilo grams curve which is used in the calculations to obtain the core losses at different operating flux densities. The total weight is calculated by estimating the number of sheets with each sheet being 0.35 mm in width.

Power losses: The next step is to calculate the number of turns and operating flux density, which are inversely proportional. Increasing B would increase the core losses, whereas increasing the number of turns would increase the copper losses. The total losses are the summation of both of these losses.

$$P_{tot} = P_{Cu} + P_{Fe} \tag{4.16}$$

The core losses (P_{Fe}) are made up of eddy current losses and hysteresis losses, both dependent on the flux density according to the classical theory [38]. For simplicity of calculations, the core losses are calculated using the core material data provided by Waasner as stated earlier. The total power losses of the transformer are parabolic in nature with increasing flux density. The minimum point of total losses is obtained where the rate of change of copper losses and core losses with respect to flux density are equal in magnitude [39].

$$\frac{\Delta P_{tot}}{\Delta B} = \frac{\Delta P_{Cu}}{\Delta B} + \frac{\Delta P_{Fe}}{\Delta B} = 0 \tag{4.17}$$

$$\frac{\Delta P_{Cu}}{\Delta B} = -\frac{\Delta P_{Fe}}{\Delta B} \tag{4.18}$$

The P_{Cu} is calculated by multiplying the length of the wire used with the resistance of the wire per unit length and the square of the rated current 4.19.

$$P_{Cu} = I^2 \cdot l_{wire} \cdot \rho \tag{4.19}$$

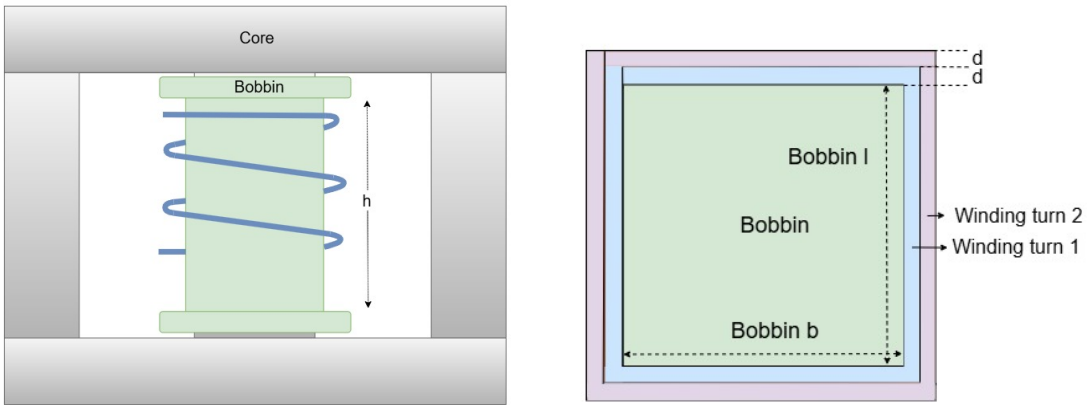
A simple approximation is considered to calculate the length of the wire. For a wire wound once around a square bobbin, the length of the wire would be the perimeter of the bobbin. When a second turn is wound on top of the first turn, the length of the second turn would be the new perimeter obtained by considering the increase in perimeter of the bobbin due to the first winding. It can be observed from the figure 4.2 that with each

turn, both the original bobbin length and breadth is increased by twice the wire diameter. This can be generalized mathematically by the equation 4.20, where (l_{bobbin}, b_{bobbin} are the length and breadth of bobbin, n is the n^{th} number of turn, and d_{wire} is the diameter of the wire.

$$L_{n-winding} = 2 \cdot (l_{bobbin} + b_{bobbin} + 4 \cdot n \cdot d_{wire}) \tag{4.20}$$

Total Length of the wire used can be given by equation 4.21 where, Nh is the number of times the full height of the bobbin is covered by the particular winding.

$$L_{wire-tot} = \sum_{n=0}^{Nh-1} Nh \cdot 2 \cdot (l_{bobbin} + b_{bobbin} + 4 \cdot n \cdot d_{wire}) \tag{4.21}$$

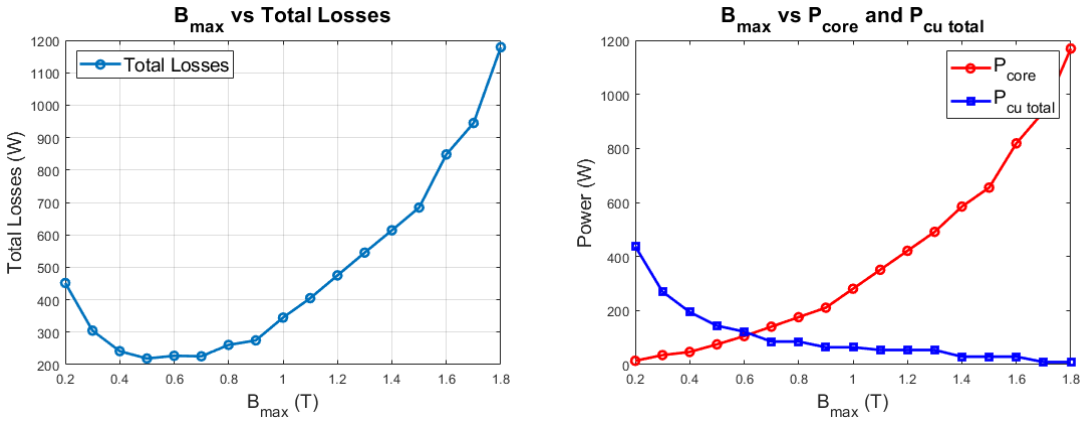


(a) Transformer winding with core and bobbin

(b) Transformer winding on bobbin

Figure 4.2: Transformer winding details

For each winding the (l_{bobbin} and b_{bobbin} will change based on the space occupied by the previous winding. It is important to understand that this method gives an approximate result, and certain overheads are considered while making the calculations. Also, during physically winding the transformer, more deviations may be introduced based on the winding strategy and the method of winding used, but still the above calculations give a good estimate for procurement and calculations.
Using the equations in this section, calculations were performed in MATLAB (code in the appendix) by varying the flux density from 0.2 T to 1.8 T. The image 4.3 shows the core losses and copper losses, and their summation wrt flux density. The ideal B is around 0.6 T. The primary number of turns and length of wire for 0.6 T are 122 and 122 m respectively. Since the transformer is wound by hand, it was decided to select 0.8 T as the operating B_{max} to reduce the number of windings and length of the wire while still keeping the losses minimal. The table 4.4 consolidates the calculations for 0.8 T of flux density.



(a) Transformer Total losses vs flux density

(b) Transformer core and copper losses vs flux density

Figure 4.3: Transformer losses vs flux density

Parameter	Value	Unit
Volts per turn	8.2	
Total power losses	260	W
Core losses	175	W
Copper losses	85	W
N_p	92	
N_{s1}	37	
N_{s2}	18	
A_p	1886	cm^4
W_a	29.5	cm^2
A_c	64	cm^2

Table 4.4: Transformer calculations

Proximity effect: Focusing on the current flowing in two windings of the transformer, the magnetic field produced by one wire produces eddy currents in the other wire, creating a situation similar to the skin effect. The resulting effect is that the current density becomes higher on one side of the wire than the other side thus reducing the effective area for the current to flow and hence increasing the AC resistance. This effect increases with the increasing number of layers in the transformer. P.L. Dowell quantified the proximity effect in his original paper in 1966 [40]. The proximity factor K is defined as the ratio of effective AC resistance to the DC resistance for the given wire. A higher value of K means a higher proximity effect and higher AC resistance. A proximity effect calculator [41] is used to calculate the value of K based on the number of layers obtained from the transformer calculations presented in above.

$$K = \frac{R_{AC}}{R_{DC}} = 1.1 \tag{4.22}$$

Since the ratio is close to 1, it is fairly assumed that the proximity effect will not affect the performance of the transformer.

Winding Strategy
The winding strategy significantly affects the performance of the transformer. The leakage inductances and winding capacitances can be changed based on how the wires are wound. To start with, the transformer was decided to be a Shell type as it has higher efficiency, less core losses, and ease of manufacturing. The three windings: Primary, Secondary 1, and Secondary 2 are wound around a common bobbin on the central limb of the EI core. Colonel Wm. T. McLyman in [37] discusses the different winding strategies and their associated leakage inductance. A longer bobbin reduces the leakage inductance along with sandwiching the primary winding between the secondary windings (interleaving), however this presents a significant manufacturing challenge. Using Bifilar windings will drastically reduce the leakage inductance, which is inline with the project's approach of using multiple 1.8 mm wires in parallel. To reduce the layer to layer capacitance [37] proposes interleaving of the windings, increasing insulation between layers (which will increase leakage inductance), and a foldback technique shown in figure 4.4.
It was decided to adopt the bifilar winding for reducing the leakage inductance and using the foldback technique for reducing the layer to layer capacitance as they are easy to implement given the manufacturing constraints.
The primary, secondary 1, and secondary 2 windings are wound on top of each other and are not sectioned. This was done to ensure the bobbin would fit inside the core when assembled.

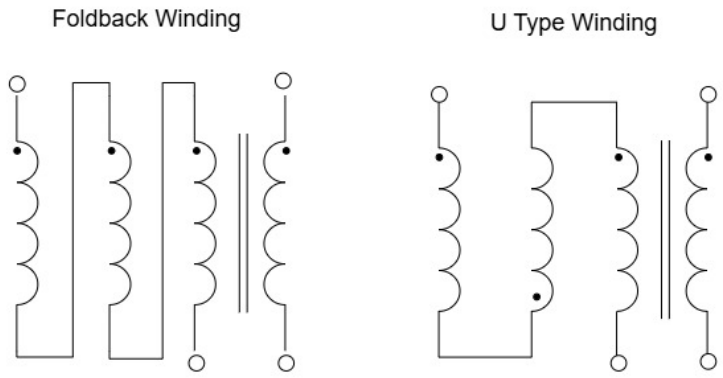


Figure 4.4: Foldback and U type winding [37]

Leakage Inductance
Leakage inductance represents the magnetic flux which does not link with the other windings. The leakage flux produced by any winding flows through the gaps between the windings and does not enclose the other windings. Based on the winding strategy, article [28] discusses how to calculate the leakage inductances of a three winding transformer based on the duality model. L_{s12}, L_{s23}, and L_{s13} represent the leakage inductances between winding 1-2, 2-3, and 1-3. For the context of this project, Winding 1, 2, and 3 are the primary, secondary 1, and secondary 2 windings of the transformer, respectively.

$$L_{s12} = \frac{\mu_o \cdot N^2 MPL}{h} \cdot [\frac{a_1}{3} + d_{12} + \frac{a_2}{3}] \tag{4.23}$$

$$L_{s23} = \frac{\mu_o \cdot N^2 MPL}{h} \cdot [\frac{a_2}{3} + d_{23} + \frac{a_3}{3}] \tag{4.24}$$

$$L_{s13} = \frac{\mu_o \cdot N^2 MPL}{h} \cdot [\frac{a_1}{3} + d_{12} + a_2 + d_{23} + \frac{a_3}{3}] \tag{4.25}$$

where, MPL = Mean path length of winding
h = Height of the windings
a_x = Width of the winding x
d_{xy} = Width of the air gap between x and y winding
N = is the common number of turns
The individual leakage inductance values Ls_1, Ls_2, Ls_3 can be obtained as,

$$Ls_1 + Ls_2 = L_{s12} \tag{4.26}$$

$$Ls_2 + Ls_3 = L_{s23} \tag{4.27}$$

$$Ls_1 + Ls_3 = L_{s13} \tag{4.28}$$

The table 4.5 shows the calculated leakage inductance values. These values are obtained by approximate lengths and can differ from the practical values depending on the manufacturing.

Parameter	Value	Unit
L_1	2.5	μH
L_2	-0.3	μH
L_3	1.5	μH

Table 4.5: Calculated leakage inductances

The negative value of L_2 is expected, as this interpretation is from the terminal model of the multiwinding transformer.

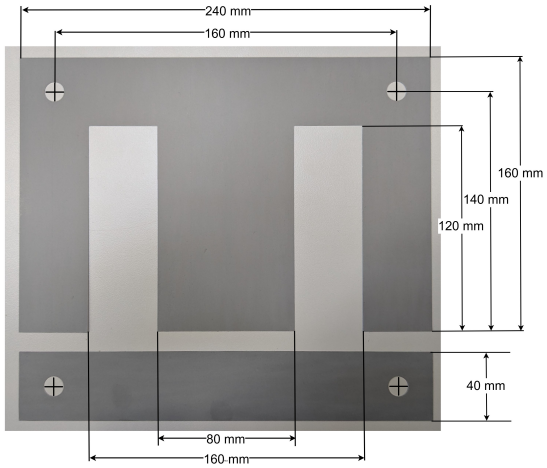
Magnetizing inductance
The magnetizing inductance is related to the flux produced in the core when one of the winding is excited at the rated voltage and the other windings are kept open. It can be calculated by calculating the inductance of one of the windings with the corresponding number of turns as follows.

$$L_m = \frac{\mu_o \cdot \mu_r \cdot N^2 \cdot A_c}{l_e} \tag{4.29}$$

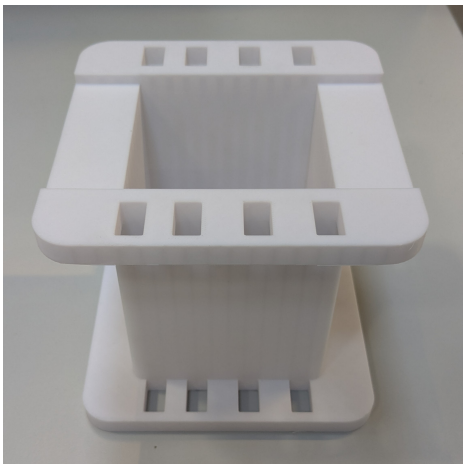
where μ_o, μ_r, N, A_c, and l_e are the absolute permeability of free space, relative permeability of the material, number of turns, area of core, and mean magnetic path length respectively.
Taking the area of core as 0.0064 cm^2, mean magnetic path length as 0.52 m, from the EI core details, $\mu_o \cdot \mu_r$ as 0.0145 from the BH curve of the manufacturer (in appendix), the L_m comes out to be 1.51 H.

4.1.2 Transformer Manufacturing

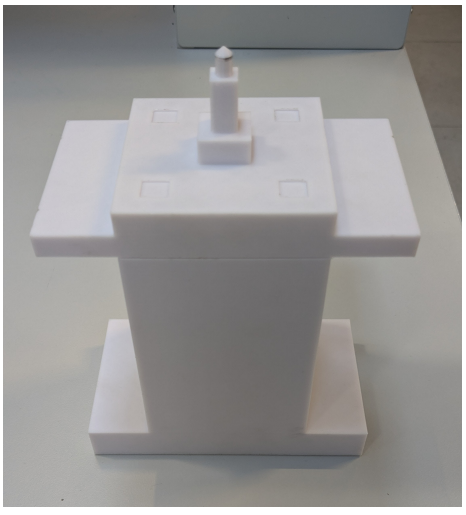
The manufacturing of the transformer involves the procurement of materials like the core, wires, bobbin, and the use of some sort of winding tool. The image 4.5a shows the procured EI plates which form the core of the transformer. The bobbin was designed and 3D printed using the university resources. The image 4.5b shows the 3D printed bobbin. The final version of the bobbin used was made using the same design but printed with ABS plastic that can withstand higher temperatures upto 100 °C. Since the number of turns is relatively high and multiple wires are in parallel, the winding of the transformer presents a challenge in itself. It was decided to use an existing rotating machine shown in image 4.6a, on which the bobbin could be mounted with the help of a winding assembly. The image 4.5c shows the winding tool assembly, which would house the bobbin and mount it on the rotating machine. The windings and turns count are done manually. This manufacturing method is not ideal, but it was the best available option in the given timelines.



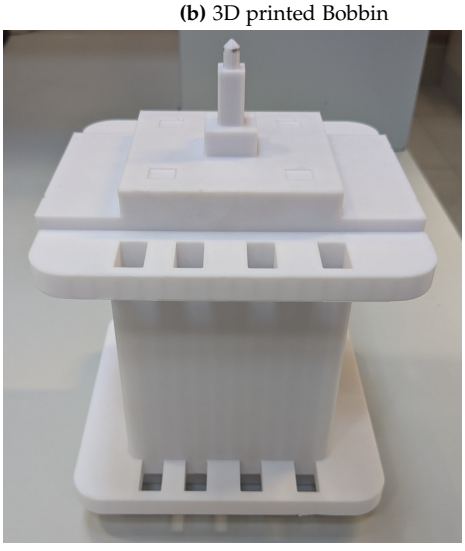
(a) Core EI plates



(b) 3D printed Bobbin

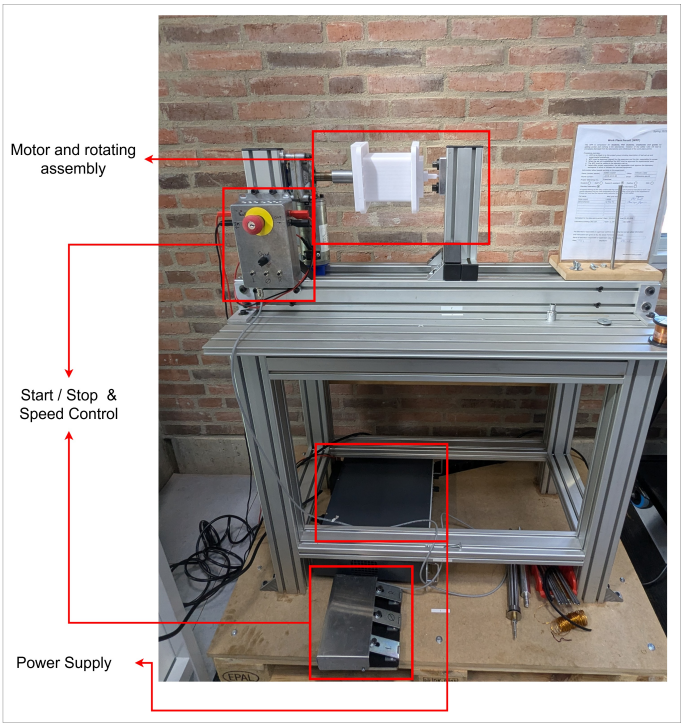


(c) Winding tool assembly



(d) Winding tool assembly with Bobbin

Figure 4.5: Core EI plates and 3D printed Bobbin and winding assembly



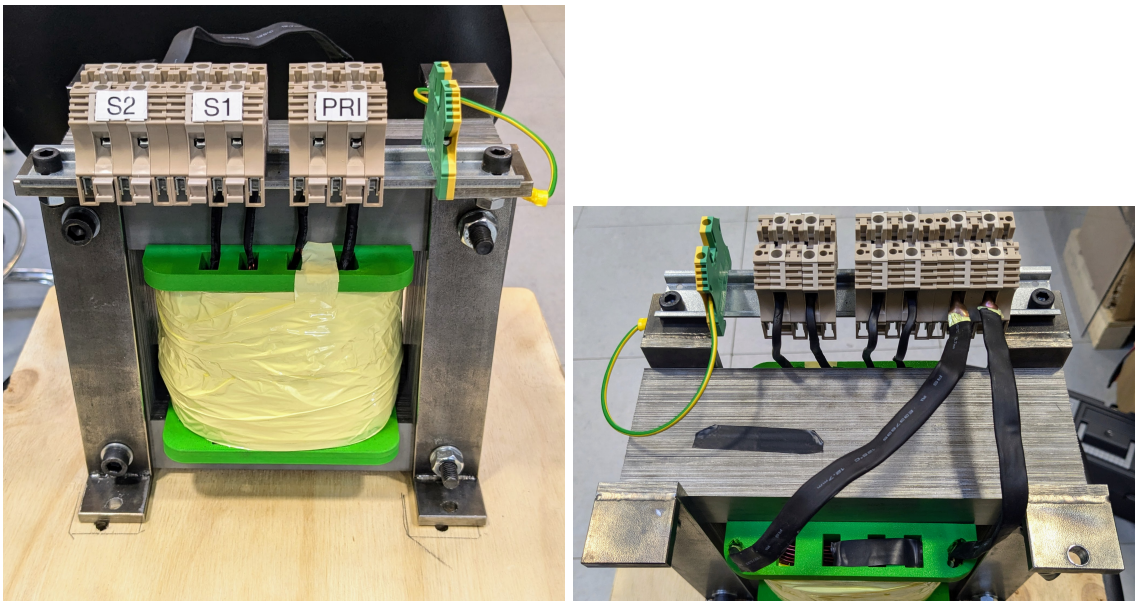
(a) Rotating machine used for winding

Figure 4.6: Rotating machine

Observations while manufacturing: Because of the nature of the manufacturing process chosen, certain deviations from the ideal scenario were introduced.

- There was a gap between the primary windings and the bobbin, as the wires tend to form a more circular shape rather than the shape of the bobbin. This could be avoided by making a more circular bobbin.
- A significant gap was introduced between different layers of primary winding because of the foldback winding strategy.
- Significant gaps were also introduced between the wires of the same winding, which would have a significant impact on the value of the leakage inductances. To avoid this, a layer of thin tape could be introduced after every layer to have better visibility while winding, if winding by hand. For significantly reducing these gaps, some mechanism of maintaining tension in the wires needs to be introduced.
- Since there was no counter to measure the number of turns, errors were introduced in the count, which would affect the transformer ratio.

The image 4.7 shows the manufactured and assembled transformer. The steel brackets provide mechanical stability to the transformer and a support for the DIN rail to mount the connectors.



(a) Manufactured transformer front view **(b)** Manufactured transformer top view

Figure 4.7: Manufactured transformer

4.2 Output filter

The output DC voltage and current are expected to contain ripple of 800 Hz owing to the 400 Hz fundamental frequency and diode rectifier. These ripple need to be filtered out in order to obtain a smooth power delivery. For this project, a second order low pass LC filter is designed for both outputs.

Capacitor calculation The capacitor is selected based on the percentage of allowable voltage ripple on the output, giving the value of ΔV. Now by considering the maximum output current and the frequency of the ripple as 800 Hz, the capacitor value is calculated using the below equation.

$$I = C \cdot \frac{\Delta V}{\Delta t} \tag{4.30}$$

Taking the peak voltages and currents as 150 V 22 A, and 300 V 16 A for secondary 2 and secondary 1 respectively, and the ripple frequency to be 800 Hz, the capacitor value for both the outputs for a voltage ripple of 5% are 14 mF and 5 mF for secondary 2 and secondary 1 respectively.

Inductor calculation Now that the capacitor value is known, the inductor value is calculated by the cut-off frequency (ω) required. Since the output ripple is expected to be of 800 Hz, the cutoff frequency is considered 10 times less as 80 Hz.

$$\omega_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C}} \tag{4.31}$$

The inductor values obtained are 0.7 mH and 0.2 mH for secondary 2 and secondary 1, respectively. It was decided to use the components readily available in the lab, hence, the final components selected are shown in table 4.6. It can be observed that the cut off frequencies are well below the required number.

Parameter	Value	Units
Secondary 1 capacitor	12	mF
Secondary 1 inductor	6	mH
Secondary 1 cut off frequency	18.8	Hz
Secondary 2 capacitor	15	mF
Secondary 2 inductor	0.9	mH
Secondary 2 cut off frequency	43.3	Hz

Table 4.6: Output filter details

4.3 Modulation

As mentioned in section 3.2, the converter is tested with two modulation strategies, Phase-shifted modulation and SPWM. This section discusses the development of the code for both modulations. The modulation is implemented using the development board STM32L476RG from STMicroelectronics. The switching frequency is chosen to be 20 kHz as the inverter had been successfully tested on the same frequency at 7.5 kW for an existing project.

Phase Shifted Modulation
The phase shift modulation can be understood as a square wave modulation in which there is a phase difference between the two legs of the inverter. From the figure 4.8, the MOSFETs Q1 and Q2 are ON simultaneously while Q3 is complementary to Q1, and Q4 is complimentary to Q2 and are also ON simultaneously. In this scenario the output voltage produced by the inverter is 0 V. When a phase shift is introduced in one of the legs of the inverter, an output voltage is produced by the inverter switching between the input DC (V_{DC})and zero. By varying the amount of phase shift, the output duty cycle is varied. The advantages of phase shift modulation are that the switching is between zero voltage and DC voltage thus producing less harmonics as compared to a bipolar SPWM that switches between $+V_{DC}$ and $-V_{DC}$, Zero voltage switching (ZVS) can be achieved by using the leakage inductor of the transformer during the period of overlap between the switches. During this time the leakage inductance current facilitates the charge transfer between the capacitors of the MOSFETs of the same leg. Since the capacitor of the MOSFET is discharged before it's turn on, the MOSFET turns on at zero voltage.

Implementation:

- A reference triangular wave or the carrier wave is generated with the switching frequency (f_c).
- 2 square waves are then generated with the required fundamental frequency (f_o) with 180°phase shift representing each leg of the inverter.
- The square waves are then compared with the carrier wave to generate the complementary gate logic signals for each leg.
- The duty cycle of the output voltage is controlled by the amplitude of the square waves compared with the amplitude of the carrier wave.
- The figure 4.9, shows the implementation of the logic in PLECS.

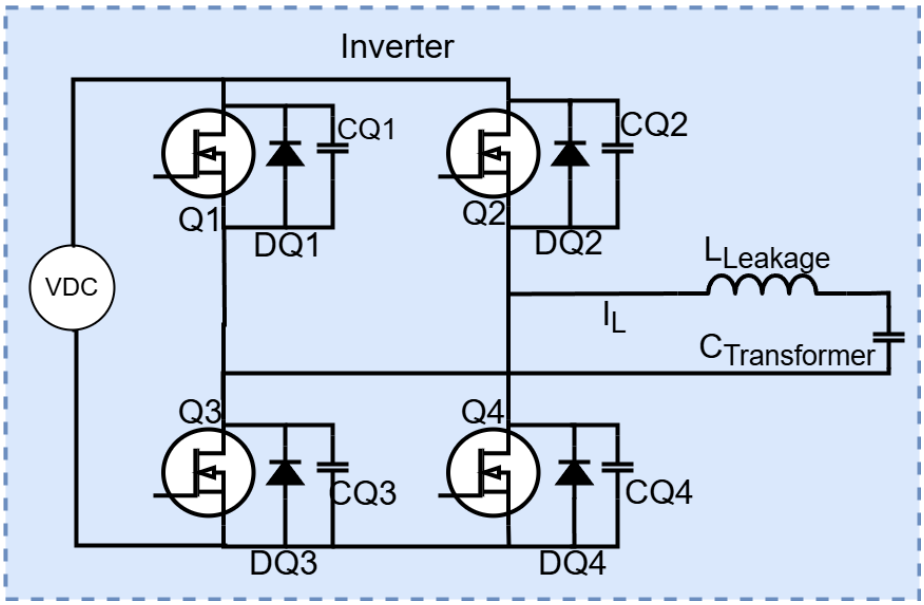


Figure 4.8: Single phase inverter

Implementation in STM32:

- For the implementation in the microcontroller, it's PWM module is utilized by using the timer 1.
- A 20 kHz triangular wave is generated by configuring the timer 1 in center-aligned PWM mode, which has 2 channels with 2 complementary outputs each.
- 2 square waves of 400 Hz as the fundamental frequency are generated using timer 3 and timer 4.
- An external input is taken on the ADC to control the duty cycle externally. By default, a 0.2 duty cycle is implemented, which can be increased till 0.8 by the external signal.
- Depending on which timer among 3 and 4 is positive, the 2 channels of timer 1 are compared with the square wave, and the gate signals are generated with the set duty cycle.
- A dead time is inserted between the complementary pair of signals by using the timer 1 dead time functionality.

Sine Pulse Width Modulation
The SPWM can be understood as a pulse width modulation, in which the width of the pulses is not constant but varies to produce an average sine wave output. In Bipolar SPWM, the MOSFETs Q1 and Q4 turn on to produce a positive voltage across the output. Then the MOSFETs Q1 and Q4 are turned off, and the MOSFETs Q2 and Q3 are turned on to produce a negative voltage on the output.The duration of these two sequences or the width of the positive and negative pulses governs the polarity and amplitude of the output voltage.

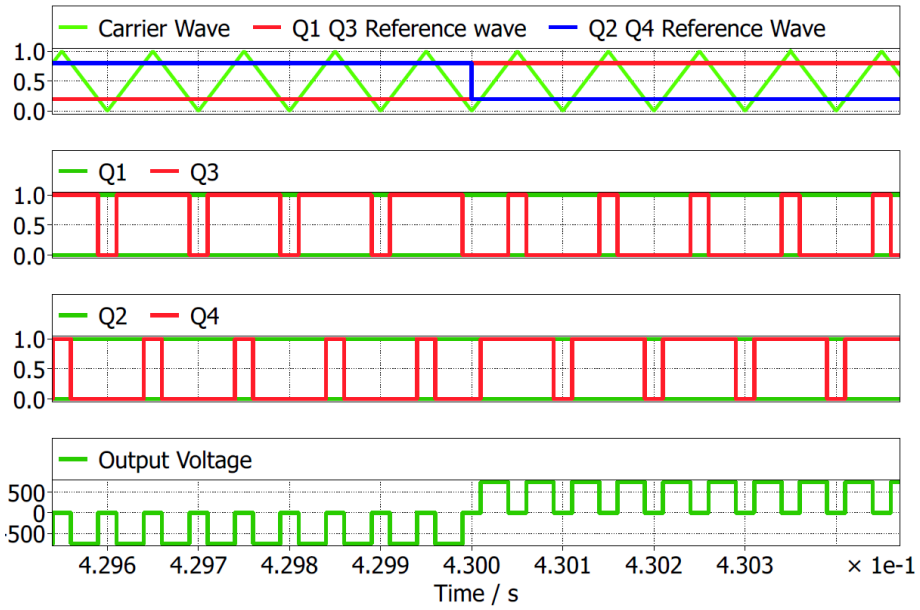


Figure 4.9: Phase shift modulation from PLECS

Implementation:

- The reference or the carrier wave is the same as the Phase shift modulation and decides the switching frequency of the MOSFETs (f_c).
- A sine wave is generated with the required fundamental frequency (f_o).
- The sine wave is compared to the carrier wave to generate the gate signals. The signals for MOSFETs Q1 and Q3 are the same as they turn on at the same time. The signals for MOSFET Q2 is complementary to Q1, and those of Q4 are complementary to Q3, which in turn makes the signals for Q2 and Q4 the same.
- The maximum width of the on pulse is governed by the difference in amplitudes of the carrier wave and the sine wave.
- The figure 4.10 shows the implementation of the logic in PLECS.

Implementation in STM32:

- Similar to the phase shift modulation, the carrier wave is generated using the timer 1, which is a 20 kHz triangular wave in center-aligned PWM mode, with 2 channels with 2 complementary outputs each.
- Timer 2 is then initialized with its Interrupt functionality with the same frequency as the carrier wave.
- Inside the Interrupt Service Routine, a sine function is defined with the required frequency, offset, and amplitude. In every interrupt the value of the angle of the sine function is incremented by the reciprocal of the switching frequency. The value of the sine function is scaled to match the same level as the carrier wave.

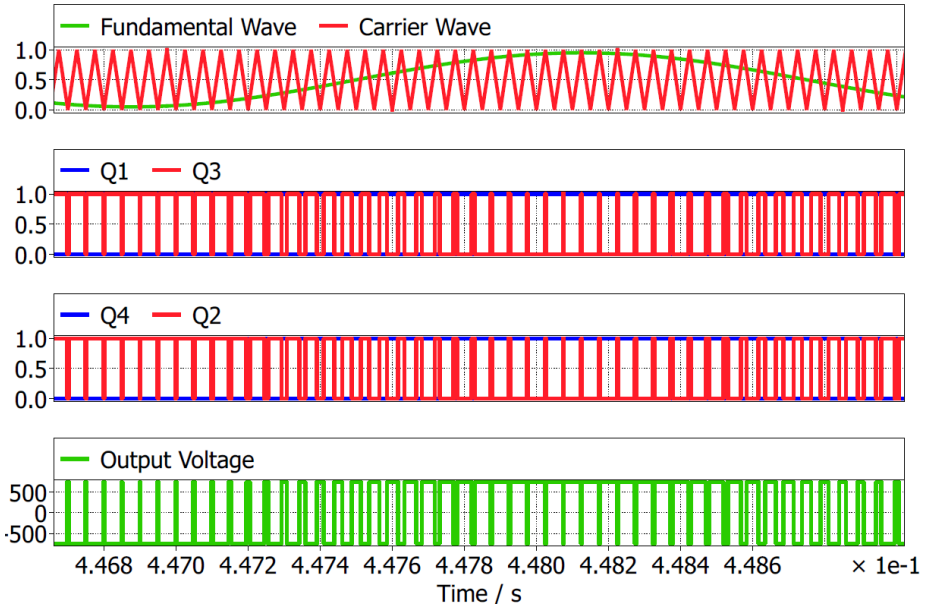


Figure 4.10: SPWM from PLECS

- The value obtained is then compared with the carrier wave of timer 1, and corresponding outputs are generated as the gate signals.
- A dead time is configured using the Timer 1 dead time functionality.

Chapter 5 Laboratory Setup

This chapters covers the hardware setup of the converter, highlighting its individual elements, and finally showing the entire assembly. As mentioned in section 3.1, The purpose of the converter is to test the transformer and also serve as proof of concept for the proposed charging architecture.

5.1 System Segments

This section presents the hardware setup of the different components of the system, namely: full bridge inverter, transformer, full bridge diode rectifier, and DC filter, and discusses the details of the same.

Full bridge inverter

The full bridge inverter is adopted from a previous project, and has been successfully tested for a power of 7.8 kW with pulse width modulation. The inverter is composed of different sections, namely: Low power board consisting of the microcontroller and its accessories, differential transceiver, gate driver, and high power board consisting of DC link capacitor and MOSFETs (image in appendix). The MOSFETs have an NTC that is biased using a resistor divider network and its potential is monitored continuously. A different resistor divider network is also used to translate an input voltage into the logic voltage for the microcontroller to control the duty cycle in phase shift modulation. The table 5.1, and image 5.1 shows the details of the same.

Component Name	Part Number / Details	Image Reference
Microcontroller	STM32 NUCLEO-L476RG	1
Differential Transceiver	CGD12HB00D	2
Gate Driver	CGD1700HB2M-UNA	3
MOSFETs	CBB032M12FM3T	4
DC Link Capacitor	B32320I0107K000	4

Table 5.1: Full bridge inverter details

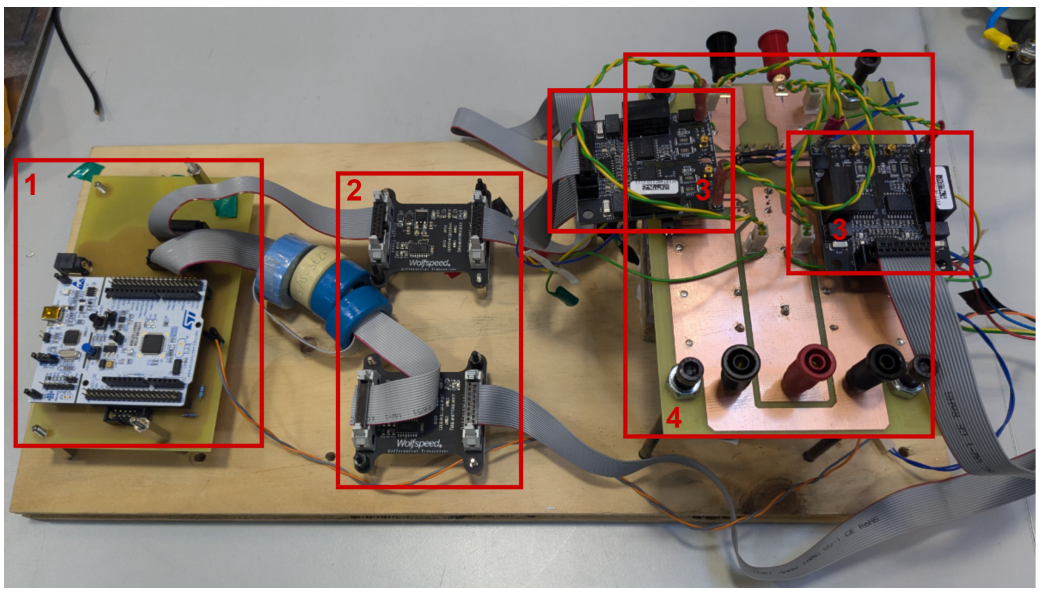


Figure 5.1: Full bridge inverter setup

Full bridge diode rectifier and output filter
The table 3.3 in section 3.2 shows the specifications of the same. In the interest of time and cost, it was decided to use the existing diode rectifier APTDF200H60G from Onsemi available in the lab. These rectifiers are mounted on a heat sink with a fan for managing their thermal stress during testing. The image 5.2 shows the shows the same.

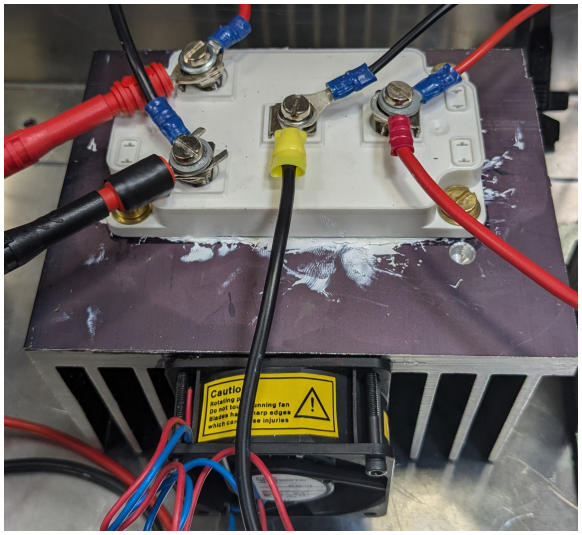
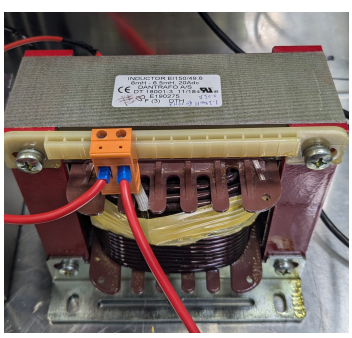
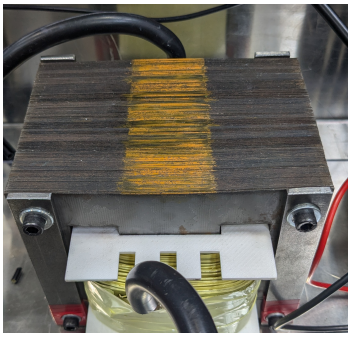


Figure 5.2: Full bridge diode rectifier

The calculations and the selection of components for the output filter is mentioned in 4.2. The image 5.5 shows the output filters for both the secondary sides.



(a) 6 mH inductor for secondary 1



(b) 0.9 mH inductor for secondary 2

Figure 5.4: Output filter capacitors 12 mF and 15 mF

Figure 5.5: Output filter

5.2 Assembled System

The images 5.6, and 5.7 show the entire system assembled together and the power supply and load. The table 5.2 identifies and lists all these components.

Groudning to chasis: The metallic chasis of the setup is connected to the Earth. The negatives of both the DC outputs are connected to the chasis to avoid the inrush current that would have resulted because of the capacitance between the chasis and the DC output negative lines.

Component Name	Image reference
Microcontroller and full bridge inverter	1
Multiwinding transformer	2
Full bridge diode rectifier for secondary 2	3
Output filter inductor for secondary 2	4
Full bridge diode rectifier for secondary 1	5
Output filter inductor for secondary 1	6
Output filter capacitor for secondary 2	7
Output filter capacitor for secondary 1	8
Input DC power supply	9
Electronic load for secondary 2	10
Bleeder resistors for input DC link capacitor	12
Resistive loads for secondary 1	13

Table 5.2: Assembled system components details

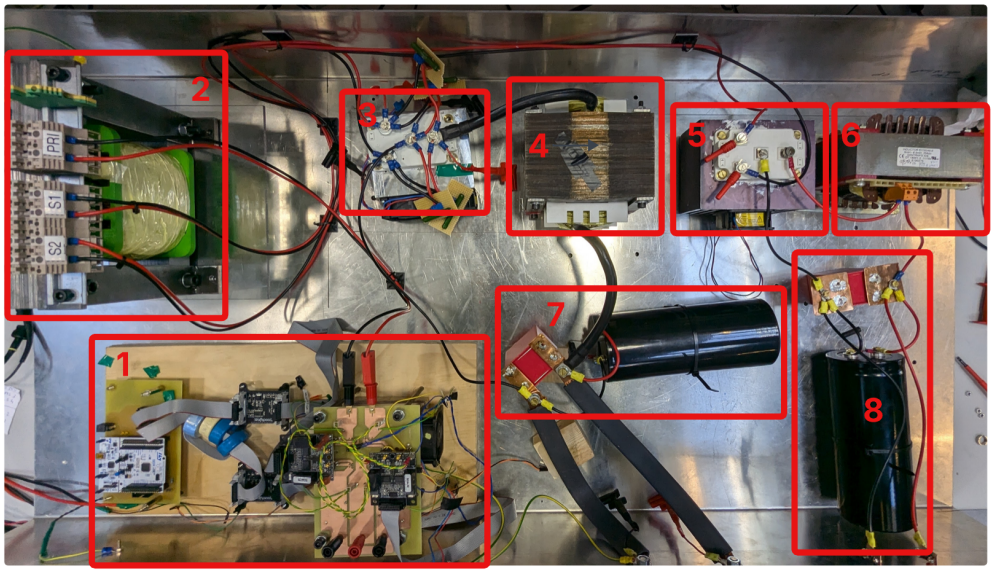


Figure 5.6: Assembled Dual output SAB system setup

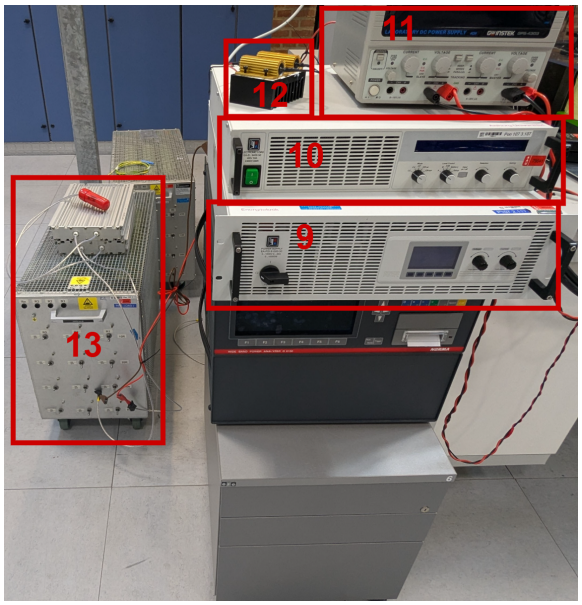


Figure 5.7: Power supplies and loads

Chapter 6 Testing

This chapter entails the individual testing of the transformer and the testing of the dual output SAB system. The individual transformer testing is important to obtain the parameters of the transformer, as they affect the overall system performance. Also, any short comings during manufacturing and design can be identified before the system level testing.

6.1 Transformer Testing

The testing of the transformer comprises the open circuit and the short circuit tests. These tests aim to practically obtain the parameters of the transformer namely magnetizing inductance, core resistance, leakage inductances, series resistances, and the voltage ratio of the windings. Both tests are done using the TC.ACS grid simulator from Regatron to provide the necessary voltage and current waveforms at the desired frequency. The image 6.1 shows the testing setup for the transformer tests.

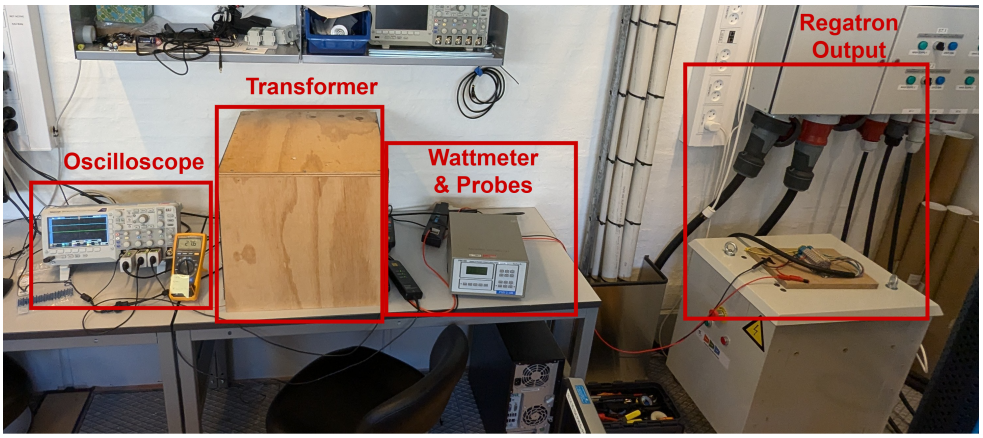


Figure 6.1: Transformer testing Lab setup

6.1.1 Shortcomings of the transformer

Owing to design and manufacturing errors, the ratio and current ratings of the transformer have deviated from the intended design.

- Due to the incorrect sizing of the conductors in the initial design phase, the transformer's currents are limited to 23 ARMS, and 15 A RMS on the secondary 2 and secondary 1 respectively.
- After the manufacturing process, the ratio achieved between the primary and secondary 1 is 2.8 instead of 2.5, and the ratio between the primary and secondary 2 is 7.4 instead of 5.2. This is likely due to an error in counting the turns. The ratings of the actual manufactured transformer for a square wave input are presented in table 6.1.

Parameter	Value	Unit
Input voltage	750	V
Input current	5.9	A
Input power	4.5	kVA
Output 1 voltage	268	V
Output 1 current	10.6	A
Output 2 voltage	101	V
Output 2 current	16.3	A

Table 6.1: Manufactured transformer specifications

6.1.2 Short Circuit Tests

The short-circuit tests for the three-winding transformer are performed according to the procedure stated in [28]. There are three impedances for three windings following the terminal model of the transformer as shown in figure 6.2. Three equations and thus three tests are required to obtain these impedances. The inductances Ls_{12}, Ls_{13}, Ls_{23}, and resistances R_{12}, R_{13}, R_{23} are obtained from the short circuit tests. These are lumped values obatined during a particular test. For examples Ls_{12} includes leakage inductances Ls_1, and Ls_2.
In the first test the Secondary 1 winding is short circuited, and the voltage is applied on the primary winding. The calculations are performed as follows.

$$Z_{12} = \frac{V_{inRMS}}{I_{inRMS}} \tag{6.1}$$

Power is obtained by taking the mean of the element-wise multiplication of the input voltage and input current.

$$R_{12} = \frac{P^2}{I_{inRMS}} \tag{6.2}$$

$$Ls_{12} = \frac{\sqrt{Z_{12}^2 - R_{12}^2}}{2 \cdot \pi \cdot f} \tag{6.3}$$

In the second test, the Secondary 2 winding is shorted, and the voltage is again applied to the primary side. In the third test, the Secondary 2 winding is short circuited , now, the voltage is applied to the Secondary 1 winding. The R_{12}, Ls_{12} and R_{23}, Ls_{23} are obtained in the same way as done for the first test.

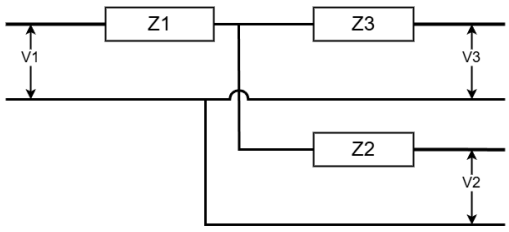


Figure 6.2: Series impedances of 3 winding transformer

The figure 6.3 shows the test setup for the short circuit test from the primary side with secondary 1 winding short-circuited. The transformer is connected to TC.ACS grid simulator from Regatron to provide the power at the desired frequency. A Tektronix oscilloscope is connected to measure the input current, input voltage, and the short-circuit current using the Tektronix current and voltage probes. PM100 wattmeter from Voltech is also connected for backup for monitoring the input voltage and current. The calculations are done by processing the data of the oscilloscope in MATLAB (can be found in Appendix).

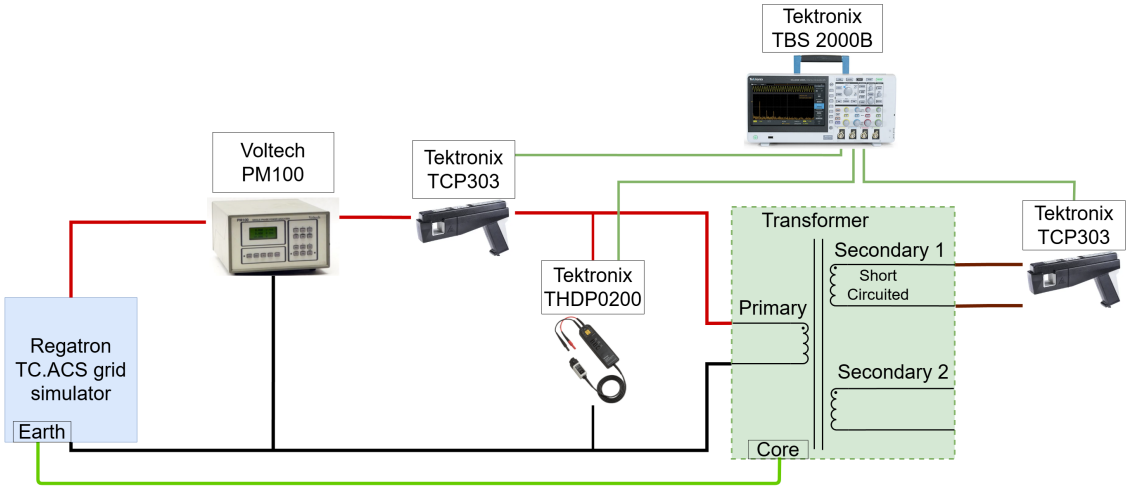


Figure 6.3: Short Circuit test setup

The table 6.2 shows the results for the sinusoidal input, and the table 6.3 shows the results for the square input.

Freq (Hz)	R1 (Ω)	Ls1 (mH)	R2 (Ω)	Ls2 (mH)	R3 (Ω)	Ls3 (mH)
100	0.40	0.30	0.47	0.13	2.15	0.61
200	0.39	0.38	0.48	0.02	2.17	0.44
300	0.40	0.39	0.47	-0.01	2.22	0.39
400	0.40	0.39	0.46	-0.02	2.21	0.38
500	0.42	0.41	0.47	-0.03	2.24	0.37
600	0.42	0.41	0.48	-0.03	2.25	0.37

Table 6.2: Short circuit results for sinusoidal input

Freq (Hz)	R1 (Ω)	Ls1 (mH)	R2 (Ω)	Ls2 (mH)	R3 (Ω)	Ls3 (mH)
100	0.18	0.46	0.63	0.18	2.04	1.08
200	0.23	0.53	0.59	-0.01	2.03	0.60
300	0.21	0.48	0.63	-0.01	1.99	0.51
400	0.25	0.45	0.59	-0.01	2.05	0.47
500	0.24	0.45	0.61	-0.01	2.05	0.45
600	0.23	0.45	0.66	-0.01	2.05	0.42

Table 6.3: Short circuit results for square input

The figure 6.4 shows the variation of measured leakage inductances Ls_{12}, Ls_{13}, and Ls_{23}

with frequency. and figure 6.5 shows the variation of leakage inductances Ls_1, Ls_2, and Ls_3 with frequency.

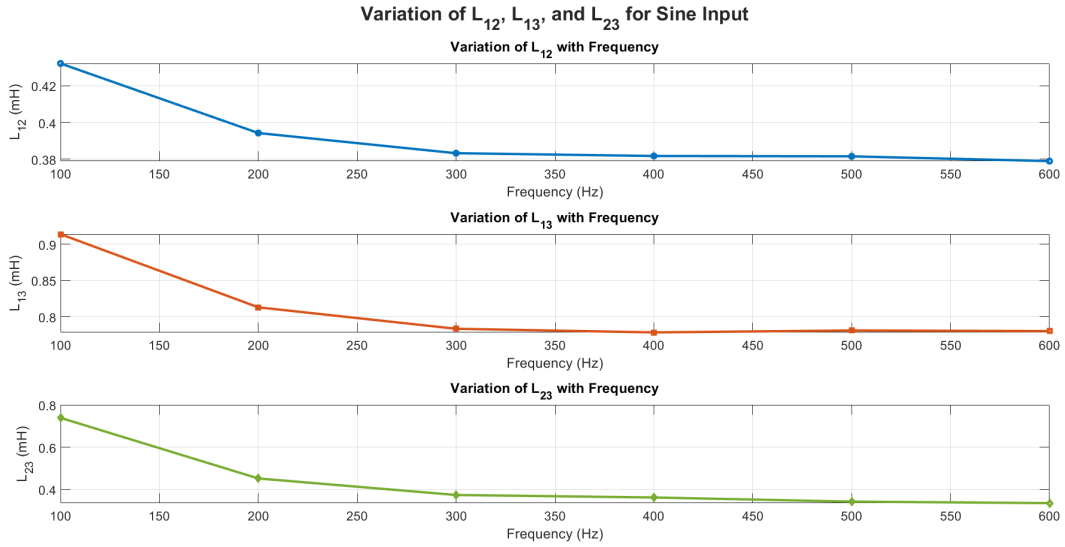


Figure 6.4: variation of measured leakage inductances for sine input

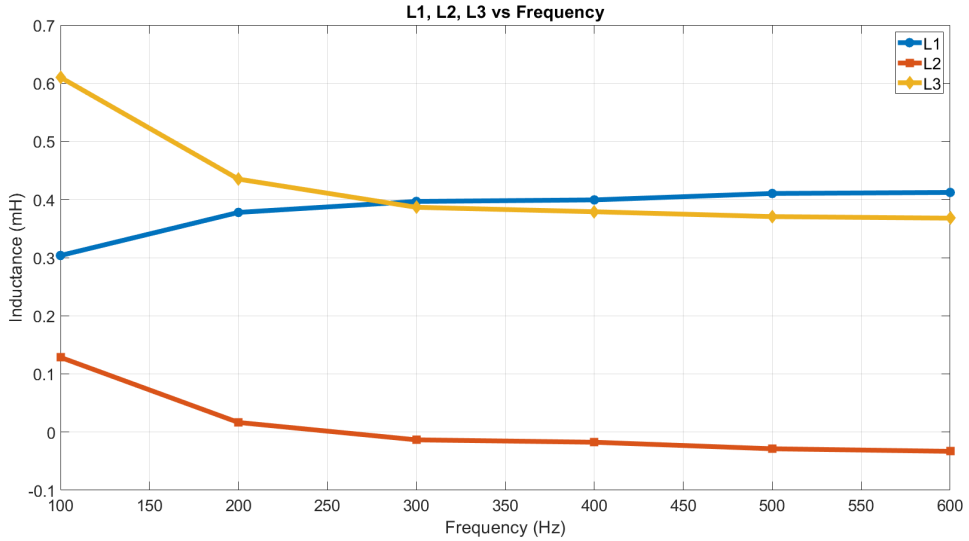


Figure 6.5: Variation of leakage inductancesLs_1, Ls_2, and Ls_3 with frequency

Observations and explanations

- The leakage inductances obtained from testing are significantly higher than the calculated values in the section 4.1.1. The most probable reason for this is the gaps between the wires of the same winding and gaps introduced because of the fold-back technique, as mentioned in section4.1.2. The leakage inductance calculation now only considers gaps between the windings but does not account for the gaps between individual wires of the same windings.

- The leakage inductances Ls_{12}, Ls_{13}, and Ls_{23} significantly decrease with the increasing frequency and become stable after 400 Hz.
- The leakage inductances Ls_1, Ls_2, and Ls_3 also vary at lower frequencies and stabilize after 400 Hz. The table 6.4 shows the maximum percentage difference between all the values of the leakage inductances obtained from the tests, first for all frequencies and then for 400 Hz to 600 Hz for sine inputs. This can be linked to the variation of Ls_{12}, Ls_{13}, and Ls_{23}. A possible reason for this could be the higher permeability of the material at lower frequencies, thus resulting in a lower reluctance and higher inductance values. The data for the permeability and B-H curve of the core material can be found in the appendix.
- The inductance values of sine and square inputs are similar.

Inductances	100 Hz-600 Hz	400 Hz-600 Hz
Ls_1 Sine	26%	3%
Ls_2 Sine	125%	47%
Ls_3 Sine	39%	3%

Table 6.4: Percentage variation in leakage inductance values

Calculation for square input: It is important to understand that the above method of calculation using the RMS values does not hold true for the square wave. For the project they are calculated using the same way and have similar results to sine wave input but, a different approach should be adopted to calculate the leakage inductances for a square wave, which is as follows.

$$L_{leakage} = \frac{\Delta V \cdot \Delta t}{\Delta I} \tag{6.4}$$

where, ΔV is the peak to peak voltage, Δt is the time for the current to reach from one peak to the other peak, and ΔI is the peak-to-peak current value. The figure 6.6 shows a snippet of the square wave input with current, with the parameters of the above equation defined.

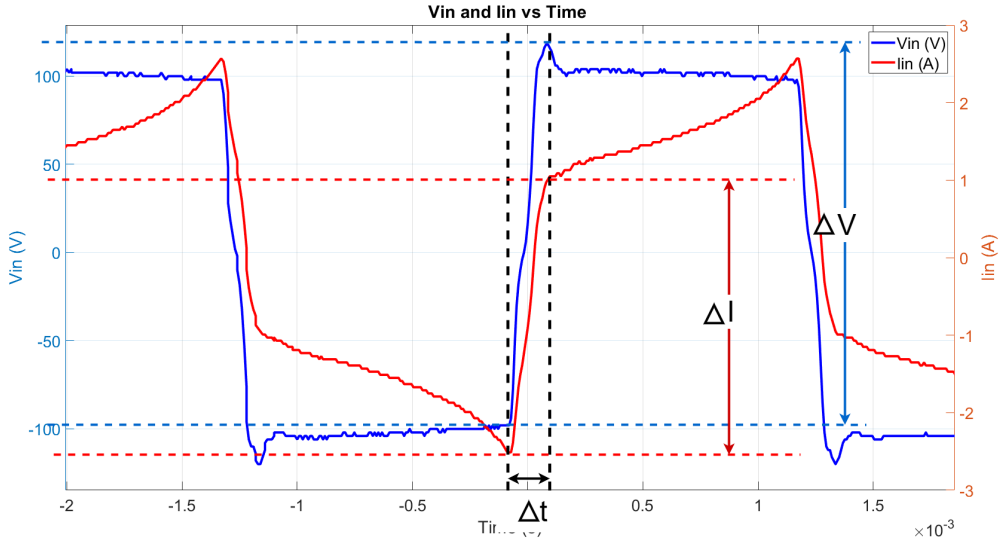


Figure 6.6: ΔV, Δt, and ΔI for a square wave input

6.1.3 Open Circuit test

The open-circuit tests on the transformer are performed to obtain the magnetizing inductance and the core losses of the transformer represented by the core resistance. The test setup is similar to the short-circuit test setup except that no winding is short-circuited. One of the windings is excited at the maximum rated voltage, and the other windings are left open. The figure 6.7 shows the setup of the open circuit test.

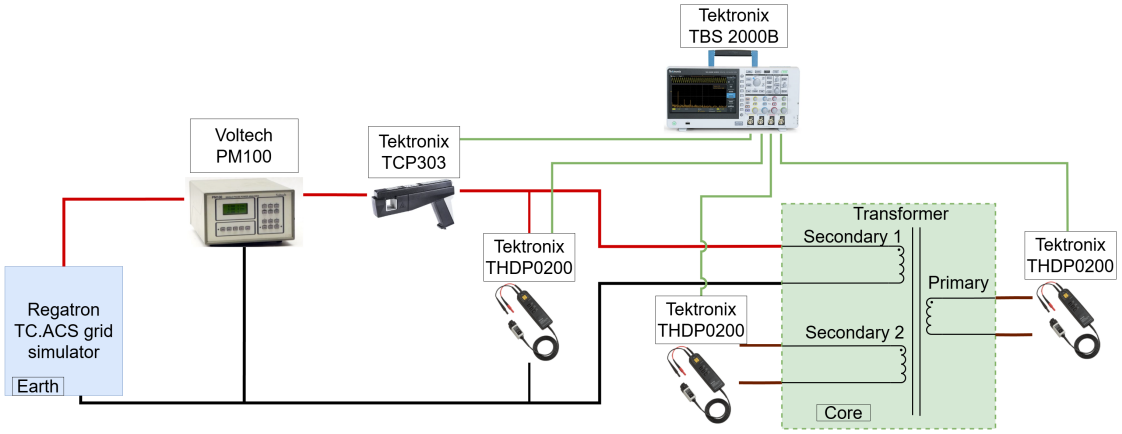


Figure 6.7: Open Short Circuit test setup

The test is performed by exciting both the secondary windings in turns with square and sine wave inputs at different frequencies to analyze the performance of the transformer. The magnetizing inductance and core resistance are calculated as follows. First, the apparent power is calculated by

$$S = V_{inRMS} \cdot I_{inRMS} \tag{6.5}$$

Real power P is then obtained by taking the mean of the element-wise multiplication of the input voltage and input current. Next, the power factor is calculated by the following

equation.

$$PF = \frac{P}{S} \tag{6.6}$$

The real current and imaginary current are then calculated using the following equations.

$$I_{Real} = I_{inRMS} \cdot PF \tag{6.7}$$

$$I_{Imaginary} = I_{inRMS} \cdot sin(acos(PF)) \tag{6.8}$$

The magnetizing inductance and core resistance are then calculated by the following equations

$$L_{magnetizing} = \frac{V_{inRMS}}{I_{Imaginary}} \cdot \frac{1}{(2 \cdot \pi \cdot frequency)} \tag{6.9}$$

$$R_{Core} = \frac{P}{I_{Real}^2} \tag{6.10}$$

The values from the secondary side are then multiplied by the square of their corresponding ratios to shift them to the primary side.

$$Parameters'_{Secondary1} = Parameters_{Secondary1} \cdot 2.8^2 \tag{6.11}$$

$$Parameters'_{Secondary2} = Parameters_{Secondary2} \cdot 7.4^2 \tag{6.12}$$

The table 6.5, and 6.6 show the results of the test for sine and square input for windings secondary 1 and secondary 2 respectively. All parameters are referred to the primary side by multiplying the square of corresponding turns ratio.

Frequency (Hz)	Sine Wave			Square Wave		
	L_m (H)	R_c (kΩ)	Power (W)	L_m (H)	R_c (kΩ)	Power (W)
400	3.51	3.48	84.59	3.60	3.49	129.02
500	2.94	3.65	80.82	3.17	3.72	113.03
600	2.52	3.79	78.03	2.71	3.88	100.89
700	2.20	3.91	75.87	2.31	3.87	100.91

Table 6.5: Open circuit test results for Secondary 1

Frequency (Hz)	Sine Wave			Square Wave		
	L_m (H)	R_c (kΩ)	Power (W)	L_m (H)	R_c (kΩ)	Power (W)
400	3.63	3.65	79.68	3.66	3.61	148.86
500	3.07	3.82	77.02	3.41	3.89	136.11
600	2.65	3.96	75.08	3.01	4.07	128.15
700	2.27	4.09	71.52	2.59	4.22	120.90

Table 6.6: Open circuit test results for Secondary 2

The figures 6.8, and 6.9 show the magnetizing inductance, core resistance, and power loss for secondary 1 sine, secondary 2 sine respectively with frequency.

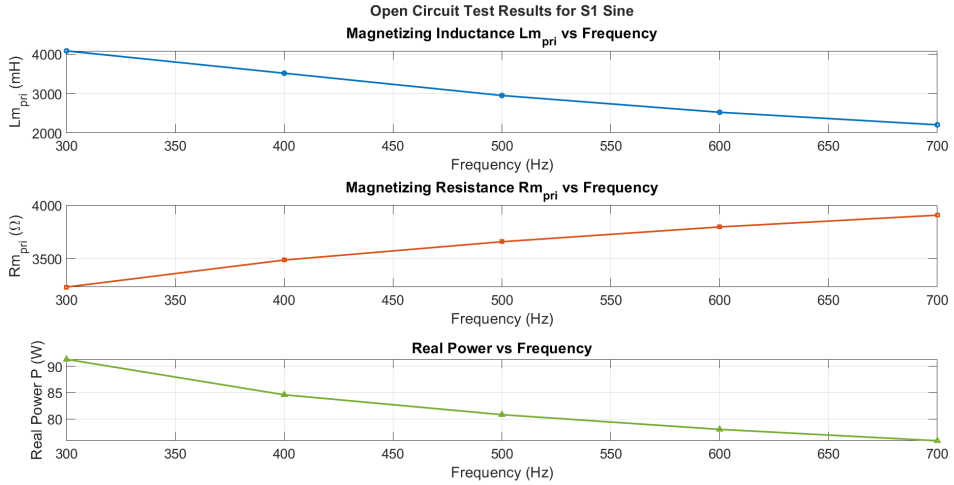


Figure 6.8: Open Circuit test secondary 1 sine input

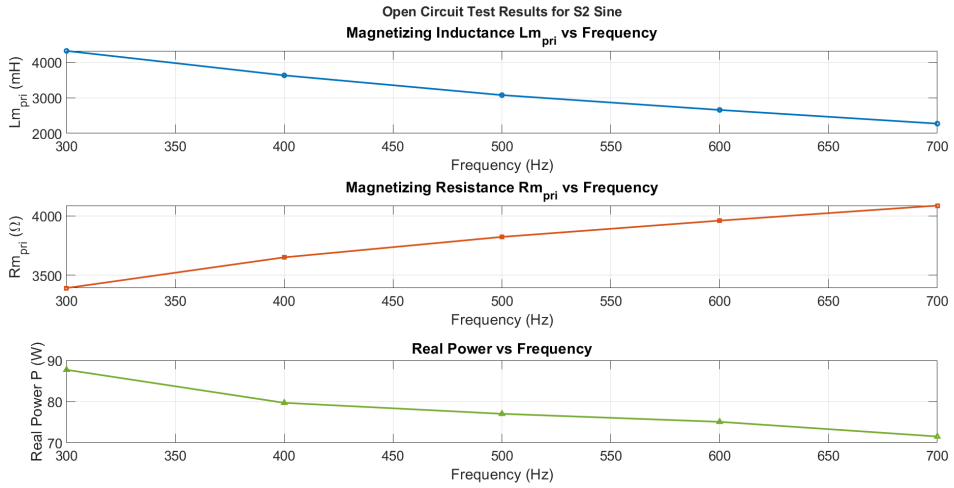


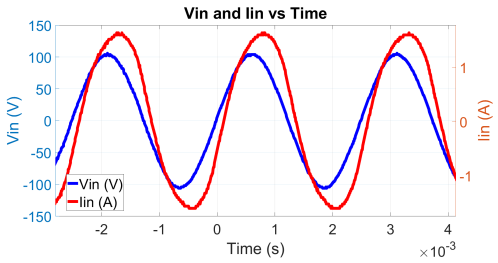
Figure 6.9: Open Circuit test secondary 2 sine input

Observations and explanations

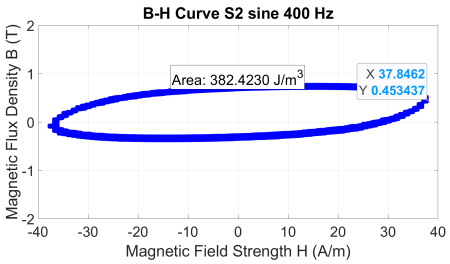
- The power dissipation of square wave input is higher than that of the sine wave input, as the hysteresis losses also depend on the max operating flux density.
- The estimated power losses in calculation (from the estimated weight and manufacturer information) for sine and square at their corresponding flux densities are 74 W and 175 W respectively from figure 4.3. This gives an error of 13% and 18% respectively.
- A similar trend is observed against frequencies for magnetizing inductance, core resistance and power losses for all the cases. This trend is expected as with the increasing frequency because of the reduction in the operating flux density and hence permeability with increasing frequency. The manufacturer's data for the permeability, and of 400 Hz can be found in the appendix.
- The magnetizing inductance value obtained at 400 Hz is 2.4 times larger than the calculated value. This variation maybe caused by the transformer operating at a

higher flux, having a higher value of permeability, but needs further investigation to find the exact reason.

Calculation for square input: It is important to understand that the above method of calculation using the RMS values and power factor calculations does not hold true for the square wave. Though the results are similar, A different approach should be adopted to calculate the leakage inductances for a square wave, which is mentioned in the short-circuit tests.
The figures 6.10,6.11,6.12, and 6.13 show the B-H curve for sine wave 400 Hz,700 Hz and square wave 400 Hz, 700 Hz for open circuit tests from the secondary 2. From figure, 6.12, it can be seen that the maximum H value for square input is 60 A/m. The H value calculated from the B-H curve provided by the manufacturer at a flux density of 0.8 T is 55 A/m. The H values of sine wave inputs are less as it operates on a lower B value than the square wave. A reduction in area is also observed with increasing frequency.

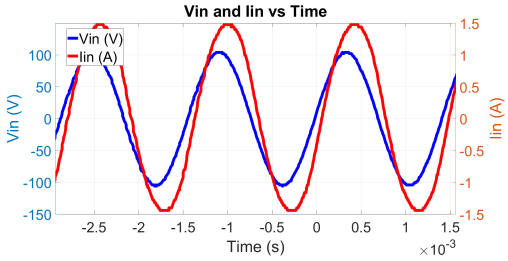


(a) Input voltage and current sine wave 400 Hz

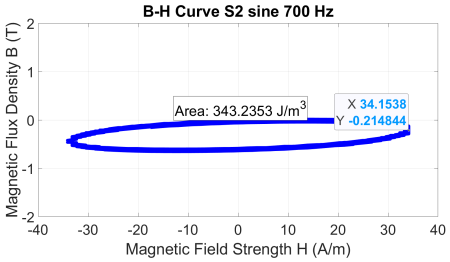


(b) B-H curve for sine wave 400 Hz

Figure 6.10: B-H curve for 400 Hz sine wave input

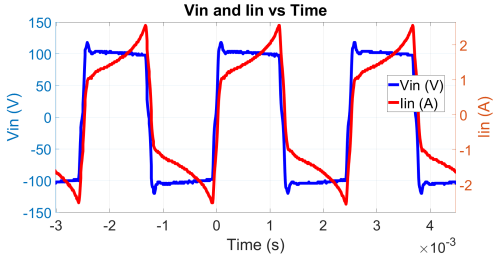


(a) Input voltage and current sine wave 700 Hz

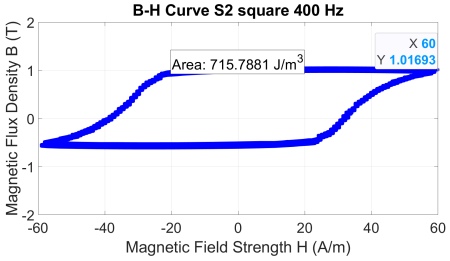


(b) B-H curve for 700 Hz sine wave input

Figure 6.11: B-H curve for 700 Hz sine wave input

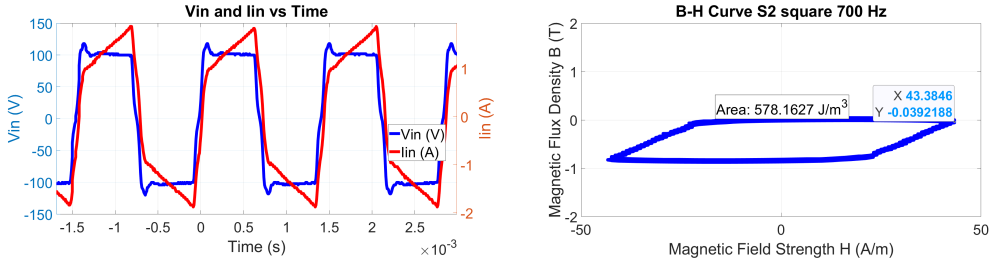


(a) Input voltage and current square wave 400 Hz



(b) B-H curve for 400 Hz square wave

Figure 6.12: B-H curve for 400 Hz square wave input



(a) Input voltage and current square wave 700 Hz

(b) B-H curve for square wave 700 Hz

Figure 6.13: B-H curve for 700 Hz square wave input

Resistance measurement Since the proximity and skin effect will have a minimal affect on the transformer, the DC resistances of windings are calculated by measuring the resistance drop on the windings under a constant current of 0.96 A from a power supply. The resistance is measured using the Fluke 45 dual display multimeter. The table 6.7 shows the values of the resistances. These are not referred to any common side of the transformer.

Parameter	Primary	Secondary 1	Secondary 2
Voltage (mV)	143.64	57.52	20.71
Current (mA)	96	96	96
Resistance (Ω)	1.49	0.60	0.21

Table 6.7: DC winding resistances

Capcitor measurement The inter-winding and intra-winding capacitances were measured using the Keysight/Agile E4990A impedance analyzer. The table 6.8 shows the values of the same.

Capacitance	Value	Unit
$C_{p\text{-}p}$ (between primary windings)	213	pF
$C_{s1\text{-}s1}$ (between secondary 1 windings)	836	pF
$C_{s2\text{-}s2}$ (between secondary 2 windings)	52	pF
$C_{p\text{-}s1}$ (between primary and secondary 1)	790	pF
$C_{p\text{-}s2}$ (between primary and secondary 2)	77	pF
$C_{s1\text{-}s2}$ (between secondary 1 and secondary 2)	822	pF

Table 6.8: Capacitance values of the transformer

6.2 System Testing

The purpose of this section is to experimentally verify the performance of the transformer on the dual output SAB system. Based on the time constraints, the system is tested upto 60 V input DC voltage for Phase shift modulation and SPWM modulation. The results of the testing are shown and the observations are explained. The table 6.9 shows the probing setup used to record the data.

	DSO1	DSO2	DSO3
Channel 1	MOSFET Q4 VDS	Trafo S1 Voltage	S1 output DC current
Channel 2	Inverter output voltage	Trafo S1 Current	S2 output DC current
Channel 3	Inverter output current	Trafo S2 Voltage	S2 output DC voltage
Channel 4		Trafo S2 Current	S1 output DC voltage

Table 6.9: Channel configuration for each DSO

6.2.1 Testing for Phase shift modulation

For this test, 60 V DC input is provided to the converter, and a current of 2.2 A is drawn from it. The duty cycle was controlled to be 0.8. The table 6.10 shows the details of the test performed. The input is the voltage and current noted from the power supply, and the DC voltages and currents are the mean value from the oscilloscope. The efficiency is calculated by adding the power of both outputs.

Parameter	Value	Unit
Input Voltage	60	V
Input Current	2.2	A
DC Voltage Output 1	14.8	V
DC Current Output 1	5	A
DC Voltage Output 2	4.3	V
DC Current Output 2	8	A
Efficiency	82	%

Table 6.10: Phase shift modulation testing

The figures 6.14 and 6.15 show the waveforms for the DSO 1. Figures 6.16 and 6.17 show the waveforms for the secondary 1 output of transformer from DSO 2. Figures 6.18 and 6.19 show the waveforms for the secondary 2 output of the transformer from DSO2. Figure 6.20 shows the output voltages and currents from DSO 3.

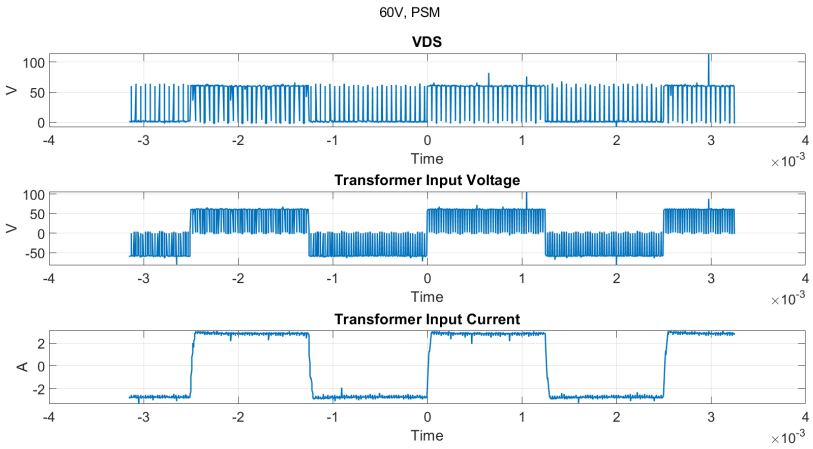


Figure 6.14: MOSFET VDS, transformer output voltage and current

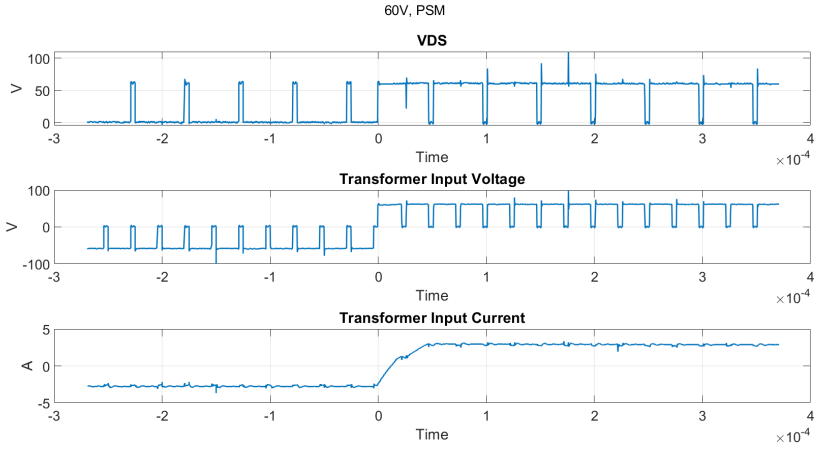


Figure 6.15: MOSFET VDS, transformer output voltage and current zoomed in

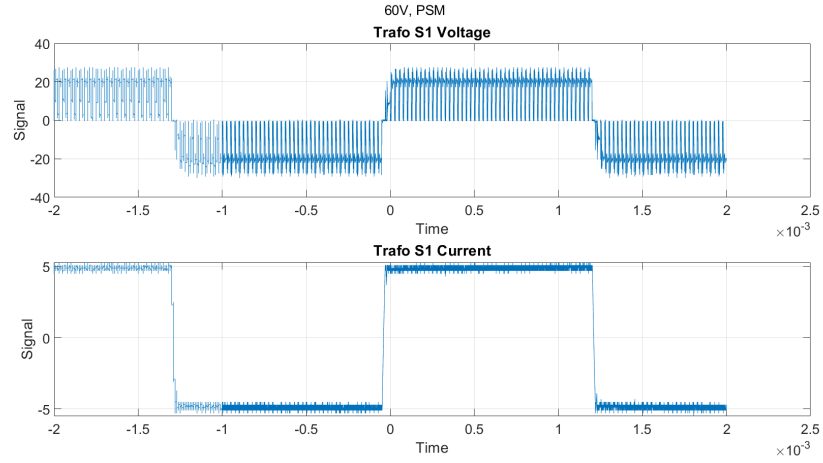


Figure 6.16: Transformer secondary 1 output voltage and current

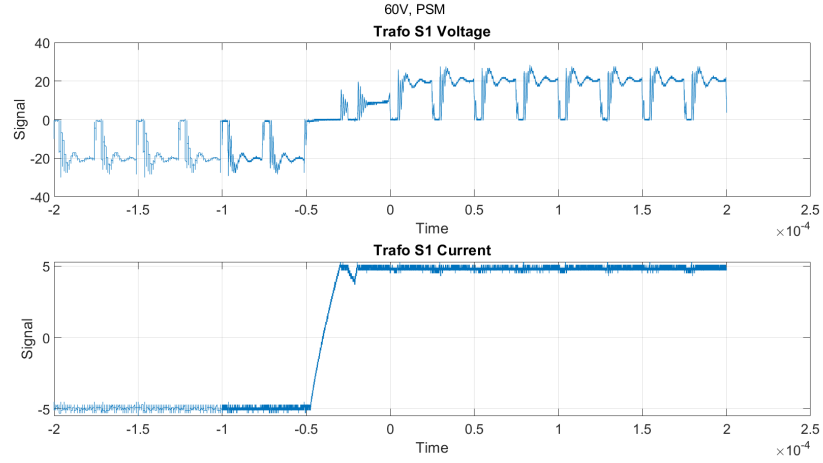


Figure 6.17: Transformer secondary 1 output voltage and current zoomed in

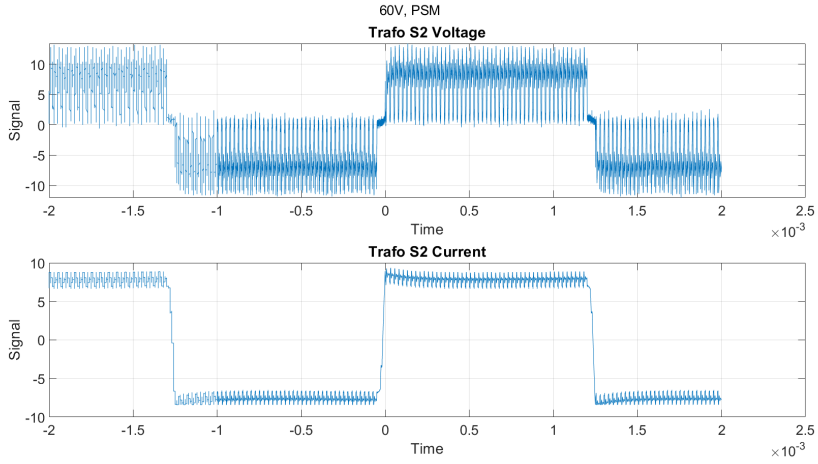


Figure 6.18: Transformer secondary 2 output voltage and current

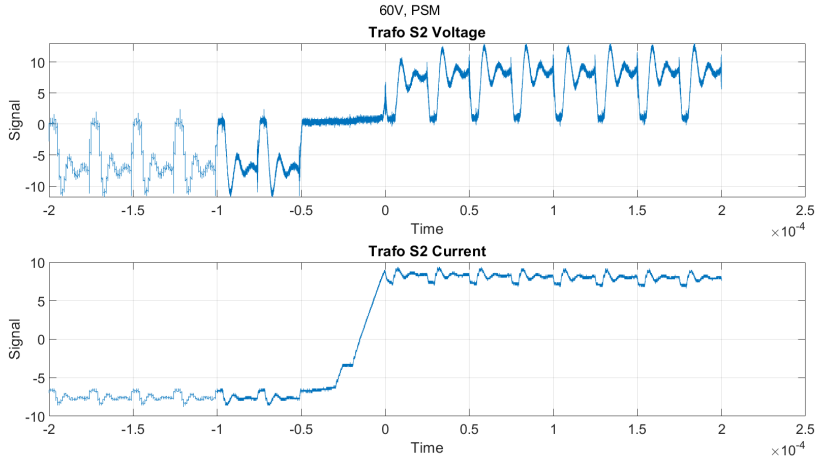


Figure 6.19: Transformer secondary 2 output voltage and current zoomed in

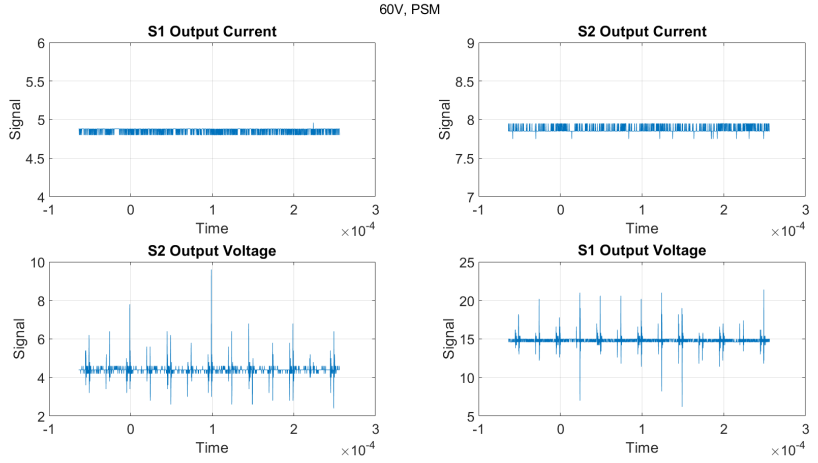


Figure 6.20: Output voltages and currents

Observations and explanations

- Transformer ratios: For the input voltage of 60 V, the secondary 1 and secondary 2 outputs are 21 V and 8.1 V, which gives a conversion ratio of 2.8 and 7.4, respectively.
- Unipolar pulses of voltage can be observed on the voltages of the transformer input and both outputs. Square current waveforms can also be observed on the same. The frequency of these is 400 Hz as expected.
- On both the secondary outputs, a voltage similar to an underdamped system can be observed. This could be due to the leakage inductance of the transformer and the capacitance of the diode bridge forming a resonance circuit.
- A 40 kHz noise can be observed on both the output DC voltages. The probable cause for this is the switching noise getting coupled from the chassis to the output. Switching noise of 40 kHz can be observed on the VDS waveform in the figure 6.21.
- On both the secondary outputs, the voltage remains zero until the current transitions from negative to the max positive value. This phenomenon is unexpected and needs further investigation.

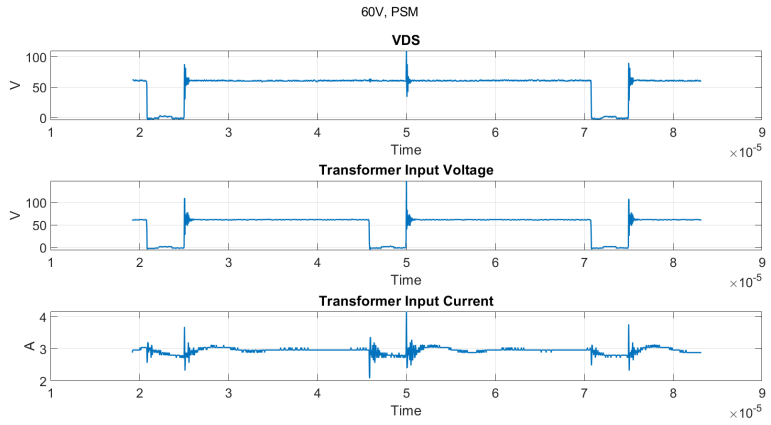


Figure 6.21: Zoomed in waveform of MOSFET VDS, Transformer input voltage and current

6.2.2 Testing for SPWM modulation

For this test, 60 V DC input is provided to the converter, and a current of 0.91 A is drawn from it. The duty cycle was controlled to be 0.9 from the code. The table 6.11 shows the details of the test performed. The input is the voltage and current noted from the power supply, and the DC voltages and currents are the mean value from the oscilloscope. The efficiency is calculated by adding the power of both outputs.

Parameter	Value	Unit
Input Voltage	60	V
Input Current	0.91	A
DC Voltage Output 1	12.1	V
DC Current Output 1	2.16	A
DC Voltage Output 2	3.1	V
DC Current Output 2	4.85	A
Efficiency	75	%

Table 6.11: SPWM testing

The figures 6.22 and 6.23 show the waveforms for the DSO 1. Figures 6.24 and 6.25 show the waveforms for the secondary 1 output of transformer from DSO 2. Figures 6.26 and 6.27 show the waveforms for the secondary 2 output of the transformer from DSO2. Figure 6.28 shows the output voltages and currents from DSO 3.

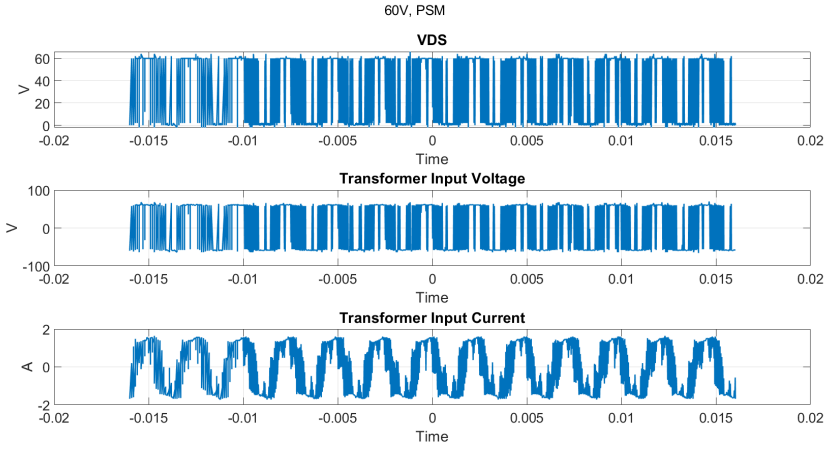


Figure 6.22: MOSFET VDS, transformer output voltage and current SPWM

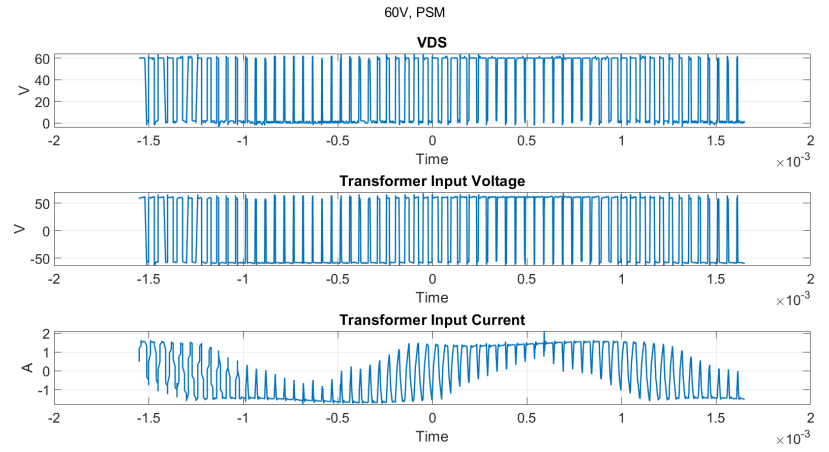


Figure 6.23: MOSFET VDS, transformer output voltage and current zoomed in SPWM

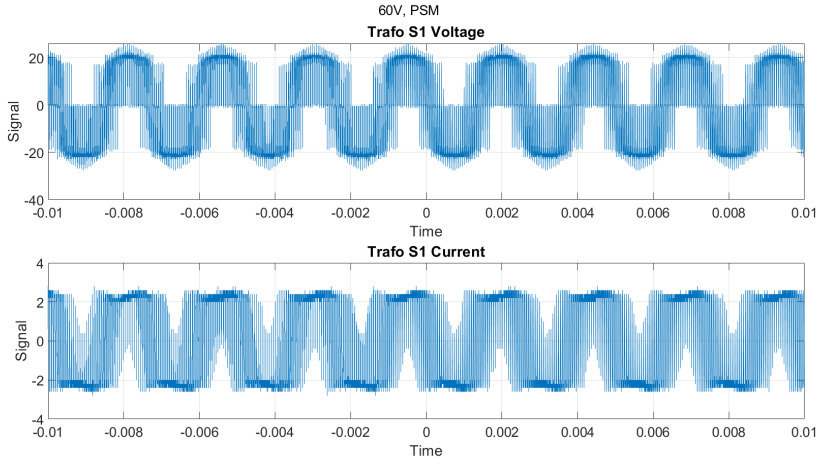


Figure 6.24: Transformer secondary 1 output voltage and current SPWM

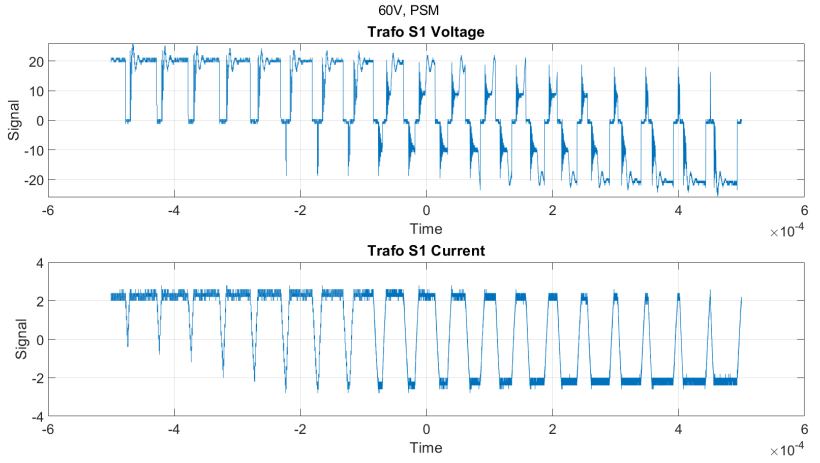


Figure 6.25: Transformer secondary 1 output voltage and current zoomed in SPWM

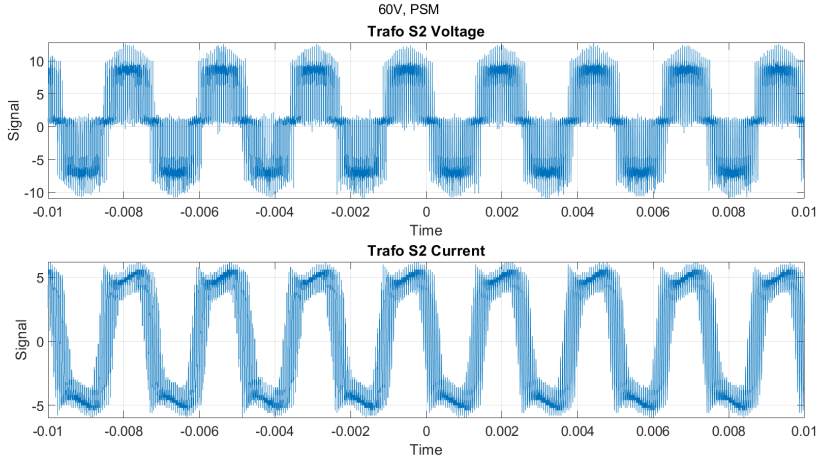


Figure 6.26: Transformer secondary 2 output voltage and current SPWM

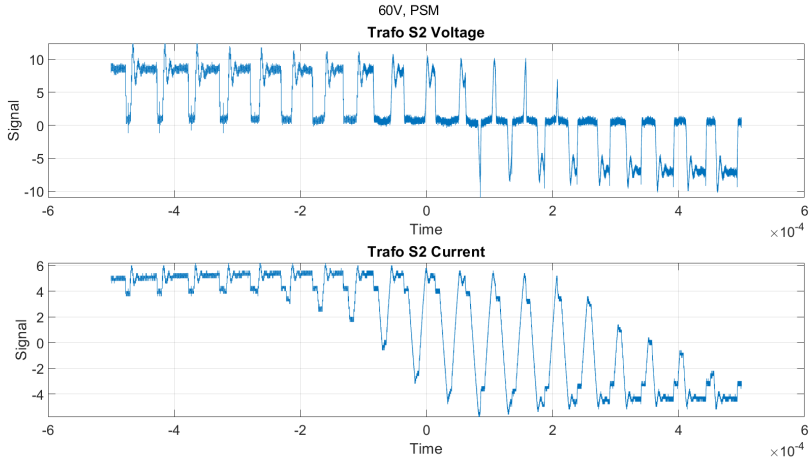


Figure 6.27: Transformer secondary 2 output voltage and current zoomed in SPWM

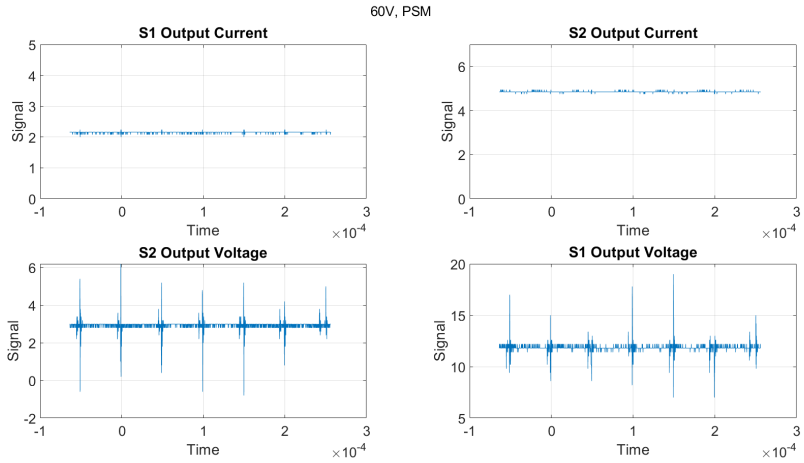


Figure 6.28: Output voltages and currents SPWM

Observations and explanations

- Transformer ratios: For the input voltage of 60 V, the secondary 1 and secondary 2 outputs are 21 V and 8 V, which gives a conversion ratio of 2.8 and 7.5, respectively.
- Bipolar pulsed sine wave voltage and current can be observed on the transformer primary and both secondaries. The frequency of these waves is 413 Hz.
- On both the secondary outputs, a voltage similar to an underdamped system can be observed, similar to the phase shift modulation. This could be due to the leakage inductance of the transformer and the capacitance of the diode bridge forming a resonance circuit as stated before.
- Similar to the phase shift modulation, a 20 kHz noise can be observed on both the output DC voltages. The probable cause for this is the switching noise getting coupled from the chassis to the output. Since in bipolar SPWM, there is no zero voltage stage produced by overlapping of MOSFETs, the output noise is same as the switching frequency.

Chapter 7 Discussion

This chapter discusses the observed results in the previous chapters, key findings, and the learnings associated with them.
The objective of the project was to build a multiwinding transformer and integrate it with a dual output SAB system. Apart from testing the transformer and converter, against the designed specifications, the objective was also to gain valuable insights into the challenges associated with designing, testing, and analysis of the transformer and the system which could serve as a reference for future designs of a similar architecture.

7.1 Transformer

During the testing of the transformer, multiple points highlighted themselves which could be taken care of in the design, and manufacturing stage of the transformer.

Transformer design

- Care must be taken in translating the system specifications into the transformer specifications and also when translating the transformer specifications from square wave to sine wave and vice versa. For the same power, the currents for sine input are higher than that for the square input and the conductor of the transformer must be sized for these higher currents of sine input with appropriate deratings.
- The high voltage windings should be wound on the outermost part of the bobbin to ensure no insulation failures happen in case the core is connected to earth.
- Better calculation methods for leakage inductance calculations should be explored. A possible way is to create a detailed FEMM model with the winding arrangements as close as possible to the actual manufactured transformer. Other methods which can consider the gaps between the wires of the same windings could be explored.

Transformer manufacturing

The manufacturing of the transformer could prove challenging and introduce significant errors if not planned with attention to detail. Things that could seem straightforward on their face value like the number of turns, also need detailed planning as deviations in these could have a significant impact on the transformer.

- While winding multiple layers by hand for a particular winding, it gets practically difficult to ensure tight spacing because of the same color of the magnet wire. This seems a simple problem and also has simple solutions like putting thin tapes after every round for better visibility but is worth mentioning because of its impact.
- Even when winding by hand, an external mechanism of creating tension in the wire would help ensure tightly spaced windings.
- The best solution to these problems is to use a transformer winding machine which would ensure tightly spaced windings, and count the number of turns. It would also enable to use more complicated winding strategies like interleaving and sectionalized windings and thus the leakage inductance and capacitance could be controller in a more mature manner.

Transformer testing

- A biasing capacitor should be added for the open circuit tests of the transformer as shown in [42]. This ensures that in case of a DC bias present on the output of the amplifier, the transformer is unaffected by it.
- As mentioned in the section 6.1, the variation of the leakage inductances with frequency, and the delta in the calculated and obtained magnetizing inductance needs to be investigated further.

Manufacturing and testing a low power prototype of the transformer would prove beneficial as it would give critical information about the core losses, B-H curve, any anomalies with testing setup, winding strategy, and help verify the transformer parameters like magnetizing inductance, leakage inductance, and capacitance with calculations. It would also help to identify the challenges with the manufacturing and help to ensure better preparedness for manufacturing the main transformer.

7.2 Dual output SAB system

- A biasing capacitor should be added in series with the transformer to compensate for any DC bias generated by the inverter.
- The leakage inductances of the transformer affect the power delivering capabilities of the converter and should be analyzed before the design of transformer.
- Operating the transformer at low values of B ensures minimal core losses but increases the number of turns, thus increasing the leakage inductance. An comparative analysis between core losses and the affect of leakage inductance of power transfer capability would be beneficial in optimizing the leakage inductance and the operating flux density.
- If the transformer needs to be used to achieve ZVS for the phase shift modulation, the leakage inductances and capacitance need to be sized accordingly as they form the network for energy transfer with the capacitance of the MOSFETs to achieve ZVS.
- The voltage ratio of the transformer needs to be adjusted for the drop due to leakage inductance and resistance and possible duty cycle losses present in the phase shift modulation.

7.3 Assumptions and constraints

- The proposed architecture would need high power, microgrids and system architecture expertise to realize more practical challenges and to design and implement the system.
- With increasing power, isolation and thermal considerations would have to be taken into account for the transformer.
- An analysis for the best possible options for the secondary side need to be identified in terms of control schemes for delivering power to the battery.

Chapter 8 Conclusion

The thesis started with the vision presented in the introduction which is stated below.

> *To find a solution that can solve the problem of reliable protection and metering standards in DC fast charging architecture and the problem of simultaneous charging of EVs with different bus voltages*

The proposed charging architecture conceptually solves this problem by the introduction of the multiwinding transformer with the medium frequency microgrid. The idea is to build upon the existing work done on 400 Hz AC grid as stated in section 1.2 to tackle the problem of reliable protection and metering standards and use the multiwinding transformer to provide isolation, and flexibility in bus voltages required for different EVs. On the assumption of technological and financial feasibility of high power converters mentioned in section 1.2, the proposed architecture also reduces the number of converters and high frequency transformers.
For the proposed solution, the project zooms in to firstly the possible designs for power delivery to the EVs mentioned in the SOA section 2.1 providing direction for the future works and then secondly into the multiwinding transformer mentioned in section 2.2.
The implementation of the objective of the project is started by introducing the dual output SAB system and its different components in the chapter 3. Once all the components are identified, the multiwinding transformer is brought into focus. The theory, design methodology, and design considerations are presented in the section 4.1.1 in detail and the manufacturing and its challenges are discussed in section 4.1.2. This brings the transformer design from the paper to the real world and the challenges of this process are also highlighted.
The calculations and implementation of other components of the system are then discussed followed by a detailed description of the assembly of the setup 5.
Once the manufacturing is completed, the transformer is tested with the open circuit and short circuit tests as discussed in section 6.1. The shortcomings of the transformer are identified and critical leanings are concluded. The tests show the performance of the transformer and the variation of its parameters against different frequencies. The delta between the design and testing is identified and the possible reasons are hypothesized. The system is then tested within its constraints as discussed in section 6.2. Important observations are obtained from the testing confirming transformer's basic operation, and also hinting some potential issues that require attention.
The important learnings are collated in the section 7 to provide a better understanding of the challenges and some possible solutions and directions to avoid and tackle them.
The thesis concludes with providing a starting platform for the implementation of the proposed architecture. It falls short to achieve the required power levels for the converter and the transformer, but it highlights important learnings and considerations in the direction of successfully testing the proof of concept for the proposed DC fast charging architecture withing its assumptions and limitations.

Chapter 9 Future Work

This chapter comprises of the possible future works based on the context and learnings of this thesis.

- Testing of the dual output SAB converter at rate power as this would provide more key insights of transformer's performance with the converter. Also, this would mean that the two different modulations could be compared by the converter's performance.
- Investigation of deltas between the calculations and testing of the transformer would open doors to some new learnings on the design, calculations, testing and the core material. An Epstein frame could also be used to analyze the core material properties against the manufacturer's data.
- Adding buck converters after the diode bridges or replacing diode bridges with active switches to implement battery charging algorithms.
- Comparison of results of the current converter at rated power with other single output converters in the same power range.
- Performing a mature FEMM analysis of the transformer to compare against the testing results.
- A power flow analysis for a three port converter could be performed based on the analysis provided in the paper [43].

Long term future works would have a vast spectrum considering the the architecture proposed. This would include not only analyzing the technical feasibility of integration of different segments but also financial feasibility of the system.

Bibliography

[1] G. Arena, A. Chub, M. Lukianov, R. Strzelecki, D. Vinnikov, and G. De Carne, "A comprehensive review on dc fast charging stations for electric vehicles: Standards, power conversion technologies, architectures, energy management, and cybersecurity," *IEEE Open Journal of Power Electronics*, vol. 5, pp. 1573–1611, 2024. DOI: 10.1109/OJPEL.2024.3466936.

[2] J. P. Guyer, *An introduction to 400 hz electrical distribution systems*, https://pdhonline.com/courses/e455/e455content.pdf, Accessed: 2025-05-11, 2020.

[3] C. Rivetta, F. Arteche, and F. Szoncsó, "A common 400hz ac power supply distribution system for cms front-end electronics," in *8th Workshop on Electronics for LHC Experiments*, Accessed: 2025-05-11, CERN, 2002, pp. 203–208. DOI: 10.5170/CERN-2002-003.203. [Online]. Available: https://cds.cern.ch/record/593922/files/p203.pdf.

[4] "Battery electric vehicles - denmark." (), [Online]. Available: https://www.statista.com/outlook/mmo/electric-vehicles/battery-electric-vehicles/denmark.

[5] "Charging infrastructure - denmark." (), [Online]. Available: https://alternative-fuels-observatory.ec.europa.eu/transport-mode/road/denmark.

[6] "Tesla superchargers." (), [Online]. Available: https://www.tesla.com/supercharger.

[7] "Abb-terra hp." (), [Online]. Available: https://new.abb.com/ev-charging/high-power-charging.

[8] "Kempower." (2024), [Online]. Available: https://kempower.com/solution/megawatt-charging-system/.

[9] "Alpitronic hyc 1000." (), [Online]. Available: https://www.alpitronic.it/en/hypercharger/hyc-1000/.

[10] G. Rajendran, C. A. Vaithilingam, N. Misron, K. Naidu, and M. R. Ahmed, "A comprehensive review on system architecture and international standards for electric vehicle charging stations," *Journal of Energy Storage*, vol. 42, p. 103 099, 2021, ISSN: 2352-152X. DOI: https://doi.org/10.1016/j.est.2021.103099. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2352152X21008045.

[11] "Trends in charging infrastructure." (2022), [Online]. Available: https://www.iea.org/reports/global-ev-outlook-2022/trends-in-charging-infrastructure.

[12] G. Rizzoli, M. Mengoni, L. Vancini, G. Sala, A. Tani, and L. Zarri, "Integrated boost-converter for 400 v - 800 v fast-charging compatibility," in *2022 Second International Conference on Sustainable Mobility Applications, Renewables and Technology (SMART)*, 2022, pp. 1–8. DOI: 10.1109/SMART55236.2022.9990158.

[13] H. Chen, Z. Hu, H. Luo, J. Qin, R. Rajagopal, and H. Zhang, "Design and planning of a multiple-charger multiple-port charging system for pev charging station," *IEEE Transactions on Smart Grid*, vol. 10, no. 1, pp. 173–183, 2019. DOI: 10.1109/TSG.2017.2735636.

[14] "Simultaneous charging." (2023), [Online]. Available: https://www.evgo.com/blog/simultaneous-charging-less-equipment-more-happy-customers/.

[15] "Simultaneous charging." (2023), [Online]. Available: https://www.noodoe.com/blog/simultaneous-charging.

[16] "Siemens-press." (2024), [Online]. Available: https://press.siemens.com/global/en/pressrelease/megawatt-charging-system-siemens-delivers-1-mw-charge-first-time-during-testing.

[17] "Abb press release." (2024), [Online]. Available: https://new.abb.com/news/detail/113917/abb-e-mobility-and-man-demonstrate-megawatt-charging-on-the-etruck-for-the-first-time.

[18] T. Gruzs, "Design considerations for powering 415 hz computer systems," in *Conference Record of the 1988 IEEE Industry Applications Society Annual Meeting*, 1988, 1495–1503 vol.2. DOI: 10.1109/IAS.1988.25255.

[19] A. Shekhar, G. C. R. Mouli, S. Bandyopadhyay, and P. Bauer, "Electric vehicle charging with multi-port converter based integration in dc trolley-bus network," in *2021 IEEE 19th International Power Electronics and Motion Control Conference (PEMC)*, 2021, pp. 250–255. DOI: 10.1109/PEMC48073.2021.9432590.

[20] J. Schäfer, D. Bortis, and J. W. Kolar, "Multi-port multi-cell dc/dc converter topology for electric vehicle's power distribution networks," in *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2017, pp. 1–9. DOI: 10.1109/COMPEL.2017.8013326.

[21] S. A. Khan, M. R. Islam, Y. Guo, and J. Zhu, "A new isolated multi-port converter with multi-directional power flow capabilities for smart electric vehicle charging stations," *IEEE Transactions on Applied Superconductivity*, vol. 29, no. 2, pp. 1–4, 2019. DOI: 10.1109/TASC.2019.2895526.

[22] H. Cao, L. Du, F. Guo, Z. Ma, and Y. Zhao, "A triple active bridge (tab) based solid-state transformer (sst) for dc fast charging systems: Architecture and control strategy," in *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2023, pp. 855–860. DOI: 10.1109/ECCE53617.2023.10362803.

[23] M. T. Gabriel, D.-E. A. Mansour, M. Shoyama, and S. M. Abdelkader, "A triple-active bridge based solid state transformer fast charging station topology for electric vehicles," in *2024 IEEE International Conference on Environment and Electrical Engineering and 2024 IEEE Industrial and Commercial Power Systems Europe (EEEIC / ICPS Europe)*, 2024, pp. 01–06. DOI: 10.1109/EEEIC/ICPSEurope61470.2024.10750986.

[24] A. Ahmad and I. Thirumarai-Chelvan, "Hybrid control scheme for more efficient charging of two electric vehicle batteries simultaneously," in *2024 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, 2024, pp. 707–712. DOI: 10.1109/CCECE59415.2024.10667156.

[25] M. D. Alam, M. Mahinur Rahman, I. Husain, and S. Lukic, "Circulating power and winding current minimization in a triple active bridge dc-dc converter with optimized leakage inductance design," in *2024 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2024, pp. 474–480. DOI: 10.1109/APEC48139.2024.10509037.

[26] B. O. Aarninkhof, D. Lyu, T. B. Soeiro, and P. Bauer, "A reconfigurable two-stage 11 kw dc–dc resonant converter for ev charging with a 150–1000 v output voltage range," *IEEE Transactions on Transportation Electrification*, vol. 10, no. 1, pp. 509–522, 2024. DOI: 10.1109/TTE.2023.3279211.

[27] J. Wang, A. Witulski, J. Vollin, T. Phelps, and G. Cardwell, "Derivation, calculation and measurement of parameters for a multi-winding transformer electrical model," in *APEC '99. Fourteenth Annual Applied Power Electronics Conference and Exposition. 1999 Conference Proceedings (Cat. No.99CH36285)*, vol. 1, 1999, 220–226 vol.1. DOI: 10.1109/APEC.1999.749513.

[28] F. de Leon and J. A. Martinez, "Dual three-winding transformer equivalent circuit matching leakage measurements," *IEEE Transactions on Power Delivery*, vol. 24, no. 1, pp. 160–168, 2009. DOI: 10.1109/TPWRD.2008.2007012.

[29] C. Alvarez-Marino, F. de Leon, and X. M. Lopez-Fernandez, "Equivalent circuit for the leakage inductance of multiwinding transformers: Unification of terminal and duality models," *IEEE Transactions on Power Delivery*, vol. 27, no. 1, pp. 353–361, 2012. DOI: 10.1109/TPWRD.2011.2173216.

[30] U. Steiger and S. Mariéthoz, "Method to design the leakage inductances of a multi-winding transformer for a multisource energy management system," in *2010 IEEE Vehicle Power and Propulsion Conference*, 2010, pp. 1–6. DOI: 10.1109/VPPC.2010.5729027.

[31] M. Rashidi, A. Bani-Ahmed, R. Nasiri, A. Mazaheri, and A. Nasiri, "Design and implementation of a multi winding high frequency transformer for mpsst application," in *2017 IEEE 6th International Conference on Renewable Energy Research and Applications (ICRERA)*, 2017, pp. 491–494. DOI: 10.1109/ICRERA.2017.8191108.

[32] A. Wilk, "Determination of leakage inductances of multi-winding and single-phase transformer," *Most Wiedzy*, 2012, Accessed: 2025-05-11. [Online]. Available: https://mostwiedzy.pl/pl/publication/download/1/determination-of-leakage-inductances-of-multi-winding-and-single-phase-transformer_65838.pdf.

[33] "Charging infrastructure of medium voltage station upped to megawatt class." (1/152025), [Online]. Available: https://www.ise.fraunhofer.de/en/press-media/press-releases/2025/charging-infrastructure-of-medium-voltage-station-upped-to-megawatt-class.html.

[34] İ. Sefa, S. Balci, and M. B. Bayram, "A comparative study of nanocrystalline and sife core materials for medium-frequency transformers," in *Proceedings of the 2014 6th International Conference on Electronics, Computers and Artificial Intelligence (ECAI)*, 2014, pp. 43–48. DOI: 10.1109/ECAI.2014.7090196.

[35] Z. Li, W. Han, Z. Xin, Q. Liu, J. Chen, and P. C. Loh, "A review of magnetic core materials, core loss modeling and measurements in high-power high-frequency transformers," *CPSS Transactions on Power Electronics and Applications*, vol. 7, no. 4, pp. 359–373, 2022. DOI: 10.24295/CPSSTPEA.2022.00033.

[36] P. Huang, C. Mao, D. Wang, *et al.*, "Optimal design and implementation of high-voltage high-power silicon steel core medium-frequency transformer," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 6, pp. 4391–4401, 2017. DOI: 10.1109/TIE.2017.2674591.

[37] C. W. T. McLyman, *Transformer and Inductor Design Handbook*, 3rd. New York: CRC Press, 2004, ISBN: 978-0824753931.

[38] S. Kulkarni and S. Khaparde, *Transformer Engineering: Design and Practice*. New York: CRC Press, 2004, ISBN: 9780824757281.

[39] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd. Boston: Kluwer Academic Publishers, 2001, ISBN: 978-0792372707.

[40] P. Dowell, "Effects of eddy currents in transformer windings," *Proceedings of the Institution of Electrical Engineers*, vol. 113, pp. 1387–1394, 8 1966. DOI: 10.1049/piee.1966.0236. eprint: https://digital-library.theiet.org/doi/pdf/10.1049/piee.1966.0236. [Online]. Available: https://digital-library.theiet.org/doi/abs/10.1049/piee.1966.0236.

[41] e-Magnetica Team, *Proximity effect from dowell curves – e-magnetica*, Accessed: 2025-05-07, n.d. [Online]. Available: https://www.e-magnetica.pl/doku.php/calculator/proximity_effect_from_dowell_curves.

[42] National Energy Technology Laboratory, "3% silicon steel core material (grain-oriented electrical steel)," U.S. Department of Energy, Tech. Rep. Revision 0.1, Sep. 2018, Prepared under DOE Office of Electricity's Transformer Resilience and Advanced Components (TRAC) program, contract DE-FE0004000. [Online]. Available: https://www.netl.doe.gov/sites/default/files/netl-file/Core-Loss-Datasheet---3-percent%5B1%5D.pdf.

[43] C. Zhao, S. D. Round, and J. W. Kolar, "An isolated three-port bidirectional dc-dc converter with decoupled power flow management," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2443–2453, 2008. DOI: 10.1109/TPEL.2008.2002056.

Appendix A C code

This appendix includes the C codes for phase shift and SPWM modulation implemented on STM32CubeIDE.

A.1 Phase shift modulation

```
/* USER CODE BEGIN Header */
/**
  ******************************************************************************
  * @file           : main.c
  * @brief          : Main program body
  ******************************************************************************
  * @attention
  *
  * Copyright (c) 2024 STMicroelectronics.
  * All rights reserved.
  *
  * This software is licensed under terms that can be found in the LICENSE file
  * in the root directory of this software component.
  * If no LICENSE file comes with this software, it is provided AS-IS.
  *
  ******************************************************************************
  */
/* USER CODE END Header */
/* Includes ------------------------------------------------------------------*/
#include "main.h"

/* Private includes ----------------------------------------------------------*/
/* USER CODE BEGIN Includes */

/* USER CODE END Includes */

/* Private typedef -----------------------------------------------------------*/
/* USER CODE BEGIN PTD */

/* USER CODE END PTD */

/* Private define ------------------------------------------------------------*/
/* USER CODE BEGIN PD */
int pwmMValue1;
int pwmMValue2;
uint32_t adc_val;
uint32_t buffer;
uint32_t duty;
volatile uint32_t duty_buffer[2];
uint8_t buffer_index = 0;
/* USER CODE END PD */

/* Private macro -------------------------------------------------------------*/
/* USER CODE BEGIN PM */

/* USER CODE END PM */

/* Private variables ---------------------------------------------------------*/
ADC_HandleTypeDef hadc1;
DMA_HandleTypeDef hdma_adc1;

TIM_HandleTypeDef htim1;
TIM_HandleTypeDef htim3;
TIM_HandleTypeDef htim4;

/* USER CODE BEGIN PV */

/* USER CODE END PV */

/* Private function prototypes -----------------------------------------------*/
void SystemClock_Config(void);
```

```
static void MX_GPIO_Init(void);
static void MX_DMA_Init(void);
static void MX_ADC1_Init(void);
static void MX_TIM4_Init(void);
static void MX_TIM3_Init(void);
static void MX_TIM1_Init(void);
/* USER CODE BEGIN PFP */

/* USER CODE END PFP */

/* Private user code ---------------------------------------------------------*/
/* USER CODE BEGIN 0 */

void HAL_TIM_PWM_PulseFinishedCallback(TIM_HandleTypeDef *htim)
{
 uint32_t current_duty = duty_buffer[(buffer_index == 0) ? 1 : 0];
 if (htim->Instance == TIM4)
     {
   // Adjust phase of TIM4 relative to TIM1
  __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_1, 1800 - current_duty); //Its 100 in place of any diff number
  __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_2, current_duty);  //Its current_duty in place of any number

  // Force an update event for TIM1 to apply the changes immediately
  HAL_TIM_GenerateEvent(&htim1, TIM_EVENTSOURCE_UPDATE);

     }
 if (htim->Instance == TIM3)
  {
   // Adjust phase of TIM4 relative to TIM1
  __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_1, current_duty);  //Its current_duty in place of any number
  __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_2, 1800 - current_duty); //Its 100 in place of any diff number

        // Force immediate update event to make changes take effect
        HAL_TIM_GenerateEvent(&htim1, TIM_EVENTSOURCE_UPDATE);

  }

}


void HAL_ADC_ConvCpltCallback(ADC_HandleTypeDef *hadc)
{
 /***
 duty = HAL_ADC_GetValue(&hadc1);

 //if the conversion is disabled we need to start the adc again
  *
  *HAL_ADC_Start_IT(&hadc1);
 ***/


 duty = buffer; // store the ADC value in adc_val

    // Constrain the duty cycle to the range 400 - 2500
 // Apply the constraint logic to the new ADC value
 if (duty < 1050) {
  duty = 1050;
 } else if (duty > 1700) {
  duty = 1700;
 }

 // Store the constrained value in the duty buffer
 duty_buffer[buffer_index] = duty;

 // Toggle the buffer index
 if (buffer_index == 0) {
  buffer_index = 1;
```

```
 } else {
  buffer_index = 0;
 }
    /***
    pwmMValue1 = __HAL_TIM_GET_COUNTER(&htim4); // get the current timer count
    pwmMValue2 = __HAL_TIM_GET_COUNTER(&htim3); // get the current timer count

    // PWM1 and PWM2 for the first half-bridge (A and B)
    if (pwmMValue1 <= 500)
    {
        // PWM A ON
        __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_1, 200);
        __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_2, duty);
        // PWM B OFF (inverse of A)
        //__HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_2, 400);
    }
    if (pwmMValue2 <= 500)
    {
        // PWM A OFF
        __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_1, duty);
        __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_2, 200);
        // PWM B ON (inverse of A)
        //__HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_2, 3200);
    }

//This is the line where the code is not applied from*

    // PWM3 and PWM4 for the second half-bridge (A and B)
       if (pwmMValue2 <= 500)
       {
           // PWM A ON
           //__HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_1, 3200);
           // PWM B OFF (inverse of A)
           __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_2, duty);
       }
       else
       {
           // PWM A OFF
           //__HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_1, 400);
           // PWM B ON (inverse of A)
           __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_2, 400);
       }

    // PWM3 and PWM4 for the second half-bridge (C and D)
    if (pwmMValue > duty)
    {
        // PWM C ON
        __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_3, duty);
        // PWM D OFF (inverse of C)
        __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_4, 50);
    }
    else
    {
        // PWM C OFF
        __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_3, 50);
        // PWM D ON (inverse of C)
        __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_4, duty);
    }
    ***/
}


/* USER CODE END 0 */

/**
  * @brief  The application entry point.
  * @retval int
```

```
  */
int main(void)
{

  /* USER CODE BEGIN 1 */

  /* USER CODE END 1 */

  /* MCU Configuration--------------------------------------------------------*/

  /* Reset of all peripherals, Initializes the Flash interface and the Systick. */
  HAL_Init();

  /* USER CODE BEGIN Init */

  /* USER CODE END Init */

  /* Configure the system clock */
  SystemClock_Config();

  /* USER CODE BEGIN SysInit */

  /* USER CODE END SysInit */

  /* Initialize all configured peripherals */
  MX_GPIO_Init();
  MX_DMA_Init();
  MX_ADC1_Init();
  MX_TIM4_Init();
  MX_TIM3_Init();
  MX_TIM1_Init();
  /* USER CODE BEGIN 2 */



  HAL_TIM_PWM_Start(&htim1, TIM_CHANNEL_1);
  HAL_TIMEx_PWMN_Start(&htim1, TIM_CHANNEL_1);
  HAL_TIM_PWM_Start(&htim1, TIM_CHANNEL_2);
  HAL_TIMEx_PWMN_Start(&htim1, TIM_CHANNEL_2);

  //HAL_Delay(100);
  HAL_TIM_PWM_Start_IT(&htim4, TIM_CHANNEL_1);
  HAL_TIM_OC_Start(&htim4, TIM_CHANNEL_2);

  HAL_TIM_PWM_Start_IT(&htim3, TIM_CHANNEL_1);
  HAL_TIM_OC_Start(&htim3, TIM_CHANNEL_2);
  //HAL_TIM_OC_Start(&htim3, TIM_CHANNEL_1);

  HAL_ADC_Start_DMA(&hadc1, &buffer, 1); //start in DMA mode
  //HAL_ADC_Start_IT(&hadc1);
  //HAL_ADC_Start(&hadc1);

  /* USER CODE END 2 */

  /* Infinite loop */
  /* USER CODE BEGIN WHILE */
  while (1)
  {
    /* USER CODE END WHILE */

    /* USER CODE BEGIN 3 */
  }
  /* USER CODE END 3 */
}

/**
  * @brief System Clock Configuration
```

```
  * @retval None
  */
void SystemClock_Config(void)
{
  RCC_OscInitTypeDef RCC_OscInitStruct = {0};
  RCC_ClkInitTypeDef RCC_ClkInitStruct = {0};

  /** Configure the main internal regulator output voltage
  */
  if (HAL_PWREx_ControlVoltageScaling(PWR_REGULATOR_VOLTAGE_SCALE1) != HAL_OK)
  {
    Error_Handler();
  }

  /** Configure LSE Drive Capability
  */
  HAL_PWR_EnableBkUpAccess();
  __HAL_RCC_LSEDRIVE_CONFIG(RCC_LSEDRIVE_LOW);

  /** Initializes the RCC Oscillators according to the specified parameters
  * in the RCC_OscInitTypeDef structure.
  */
  RCC_OscInitStruct.OscillatorType = RCC_OSCILLATORTYPE_LSE|RCC_OSCILLATORTYPE_MSI;
  RCC_OscInitStruct.LSEState = RCC_LSE_ON;
  RCC_OscInitStruct.MSIState = RCC_MSI_ON;
  RCC_OscInitStruct.MSICalibrationValue = 0;
  RCC_OscInitStruct.MSIClockRange = RCC_MSIRANGE_6;
  RCC_OscInitStruct.PLL.PLLState = RCC_PLL_ON;
  RCC_OscInitStruct.PLL.PLLSource = RCC_PLLSOURCE_MSI;
  RCC_OscInitStruct.PLL.PLLM = 1;
  RCC_OscInitStruct.PLL.PLLN = 36;
  RCC_OscInitStruct.PLL.PLLP = RCC_PLLP_DIV7;
  RCC_OscInitStruct.PLL.PLLQ = RCC_PLLQ_DIV2;
  RCC_OscInitStruct.PLL.PLLR = RCC_PLLR_DIV2;
  if (HAL_RCC_OscConfig(&RCC_OscInitStruct) != HAL_OK)
  {
    Error_Handler();
  }

  /** Initializes the CPU, AHB and APB buses clocks
  */
  RCC_ClkInitStruct.ClockType = RCC_CLOCKTYPE_HCLK|RCC_CLOCKTYPE_SYSCLK
                              |RCC_CLOCKTYPE_PCLK1|RCC_CLOCKTYPE_PCLK2;
  RCC_ClkInitStruct.SYSCLKSource = RCC_SYSCLKSOURCE_PLLCLK;
  RCC_ClkInitStruct.AHBCLKDivider = RCC_SYSCLK_DIV1;
  RCC_ClkInitStruct.APB1CLKDivider = RCC_HCLK_DIV1;
  RCC_ClkInitStruct.APB2CLKDivider = RCC_HCLK_DIV1;

  if (HAL_RCC_ClockConfig(&RCC_ClkInitStruct, FLASH_LATENCY_4) != HAL_OK)
  {
    Error_Handler();
  }

  /** Enable MSI Auto calibration
  */
  HAL_RCCEx_EnableMSIPLLMode();
}

/**
  * @brief ADC1 Initialization Function
  * @param None
  * @retval None
  */
static void MX_ADC1_Init(void)
{

  /* USER CODE BEGIN ADC1_Init 0 */
```

```
  /* USER CODE END ADC1_Init 0 */

  ADC_MultiModeTypeDef multimode = {0};
  ADC_ChannelConfTypeDef sConfig = {0};

  /* USER CODE BEGIN ADC1_Init 1 */

  /* USER CODE END ADC1_Init 1 */

  /** Common config
  */
  hadc1.Instance = ADC1;
  hadc1.Init.ClockPrescaler = ADC_CLOCK_SYNC_PCLK_DIV4;
  hadc1.Init.Resolution = ADC_RESOLUTION_12B;
  hadc1.Init.DataAlign = ADC_DATAALIGN_RIGHT;
  hadc1.Init.ScanConvMode = ADC_SCAN_DISABLE;
  hadc1.Init.EOCSelection = ADC_EOC_SINGLE_CONV;
  hadc1.Init.LowPowerAutoWait = DISABLE;
  hadc1.Init.ContinuousConvMode = ENABLE;
  hadc1.Init.NbrOfConversion = 1;
  hadc1.Init.DiscontinuousConvMode = DISABLE;
  hadc1.Init.ExternalTrigConv = ADC_SOFTWARE_START;
  hadc1.Init.ExternalTrigConvEdge = ADC_EXTERNALTRIGCONVEDGE_NONE;
  hadc1.Init.DMAContinuousRequests = ENABLE;
  hadc1.Init.Overrun = ADC_OVR_DATA_OVERWRITTEN;
  hadc1.Init.OversamplingMode = DISABLE;
  if (HAL_ADC_Init(&hadc1) != HAL_OK)
  {
    Error_Handler();
  }

  /** Configure the ADC multi-mode
  */
  multimode.Mode = ADC_MODE_INDEPENDENT;
  if (HAL_ADCEx_MultiModeConfigChannel(&hadc1, &multimode) != HAL_OK)
  {
    Error_Handler();
  }

  /** Configure Regular Channel
  */
  sConfig.Channel = ADC_CHANNEL_1;
  sConfig.Rank = ADC_REGULAR_RANK_1;
  sConfig.SamplingTime = ADC_SAMPLETIME_640CYCLES_5;
  sConfig.SingleDiff = ADC_SINGLE_ENDED;
  sConfig.OffsetNumber = ADC_OFFSET_NONE;
  sConfig.Offset = 0;
  if (HAL_ADC_ConfigChannel(&hadc1, &sConfig) != HAL_OK)
  {
    Error_Handler();
  }
  /* USER CODE BEGIN ADC1_Init 2 */

  /* USER CODE END ADC1_Init 2 */

}

/**
  * @brief TIM1 Initialization Function
  * @param None
  * @retval None
  */
static void MX_TIM1_Init(void)
{

  /* USER CODE BEGIN TIM1_Init 0 */
```

```
/* USER CODE END TIM1_Init 0 */

TIM_SlaveConfigTypeDef sSlaveConfig = {0};
TIM_MasterConfigTypeDef sMasterConfig = {0};
TIM_OC_InitTypeDef sConfigOC = {0};
TIM_BreakDeadTimeConfigTypeDef sBreakDeadTimeConfig = {0};

/* USER CODE BEGIN TIM1_Init 1 */

/* USER CODE END TIM1_Init 1 */
htim1.Instance = TIM1;
htim1.Init.Prescaler = 0;
htim1.Init.CounterMode = TIM_COUNTERMODE_CENTERALIGNED1;
htim1.Init.Period = 1800 -1;
htim1.Init.ClockDivision = TIM_CLOCKDIVISION_DIV1;
htim1.Init.RepetitionCounter = 0;
htim1.Init.AutoReloadPreload = TIM_AUTORELOAD_PRELOAD_DISABLE;
if (HAL_TIM_Base_Init(&htim1) != HAL_OK)
{
  Error_Handler();
}
if (HAL_TIM_PWM_Init(&htim1) != HAL_OK)
{
  Error_Handler();
}
sSlaveConfig.SlaveMode = TIM_SLAVEMODE_TRIGGER;
sSlaveConfig.InputTrigger = TIM_TS_ITR2;
if (HAL_TIM_SlaveConfigSynchro(&htim1, &sSlaveConfig) != HAL_OK)
{
  Error_Handler();
}
sMasterConfig.MasterOutputTrigger = TIM_TRGO_RESET;
sMasterConfig.MasterOutputTrigger2 = TIM_TRGO2_RESET;
sMasterConfig.MasterSlaveMode = TIM_MASTERSLAVEMODE_DISABLE;
if (HAL_TIMEx_MasterConfigSynchronization(&htim1, &sMasterConfig) != HAL_OK)
{
  Error_Handler();
}
sConfigOC.OCMode = TIM_OCMODE_PWM1;
sConfigOC.Pulse = 0;
sConfigOC.OCPolarity = TIM_OCPOLARITY_HIGH;
sConfigOC.OCNPolarity = TIM_OCNPOLARITY_HIGH;
sConfigOC.OCFastMode = TIM_OCFAST_DISABLE;
sConfigOC.OCIdleState = TIM_OCIDLESTATE_RESET;
sConfigOC.OCNIdleState = TIM_OCNIDLESTATE_RESET;
if (HAL_TIM_PWM_ConfigChannel(&htim1, &sConfigOC, TIM_CHANNEL_1) != HAL_OK)
{
  Error_Handler();
}
sConfigOC.OCMode = TIM_OCMODE_PWM2;
if (HAL_TIM_PWM_ConfigChannel(&htim1, &sConfigOC, TIM_CHANNEL_2) != HAL_OK)
{
  Error_Handler();
}
sBreakDeadTimeConfig.OffStateRunMode = TIM_OSSR_DISABLE;
sBreakDeadTimeConfig.OffStateIDLEMode = TIM_OSSI_DISABLE;
sBreakDeadTimeConfig.LockLevel = TIM_LOCKLEVEL_OFF;
sBreakDeadTimeConfig.DeadTime = 100;
sBreakDeadTimeConfig.BreakState = TIM_BREAK_DISABLE;
sBreakDeadTimeConfig.BreakPolarity = TIM_BREAKPOLARITY_HIGH;
sBreakDeadTimeConfig.BreakFilter = 0;
sBreakDeadTimeConfig.Break2State = TIM_BREAK2_DISABLE;
sBreakDeadTimeConfig.Break2Polarity = TIM_BREAK2POLARITY_HIGH;
sBreakDeadTimeConfig.Break2Filter = 0;
sBreakDeadTimeConfig.AutomaticOutput = TIM_AUTOMATICOUTPUT_DISABLE;
if (HAL_TIMEx_ConfigBreakDeadTime(&htim1, &sBreakDeadTimeConfig) != HAL_OK)
```

```
  {
    Error_Handler();
  }
  /* USER CODE BEGIN TIM1_Init 2 */

  /* USER CODE END TIM1_Init 2 */
  HAL_TIM_MspPostInit(&htim1);

}

/**
  * @brief TIM3 Initialization Function
  * @param None
  * @retval None
  */
static void MX_TIM3_Init(void)
{

  /* USER CODE BEGIN TIM3_Init 0 */

  /* USER CODE END TIM3_Init 0 */

  TIM_SlaveConfigTypeDef sSlaveConfig = {0};
  TIM_MasterConfigTypeDef sMasterConfig = {0};
  TIM_OC_InitTypeDef sConfigOC = {0};

  /* USER CODE BEGIN TIM3_Init 1 */

  /* USER CODE END TIM3_Init 1 */
  htim3.Instance = TIM3;
  htim3.Init.Prescaler = 25-1;
  htim3.Init.CounterMode = TIM_COUNTERMODE_UP;
  htim3.Init.Period = 7200-1;
  htim3.Init.ClockDivision = TIM_CLOCKDIVISION_DIV1;
  htim3.Init.AutoReloadPreload = TIM_AUTORELOAD_PRELOAD_DISABLE;
  if (HAL_TIM_Base_Init(&htim3) != HAL_OK)
  {
    Error_Handler();
  }
  if (HAL_TIM_PWM_Init(&htim3) != HAL_OK)
  {
    Error_Handler();
  }
  if (HAL_TIM_OC_Init(&htim3) != HAL_OK)
  {
    Error_Handler();
  }
  sSlaveConfig.SlaveMode = TIM_SLAVEMODE_TRIGGER;
  sSlaveConfig.InputTrigger = TIM_TS_ITR3;
  if (HAL_TIM_SlaveConfigSynchro(&htim3, &sSlaveConfig) != HAL_OK)
  {
    Error_Handler();
  }
  sMasterConfig.MasterOutputTrigger = TIM_TRGO_OC2REF;
  sMasterConfig.MasterSlaveMode = TIM_MASTERSLAVEMODE_DISABLE;
  if (HAL_TIMEx_MasterConfigSynchronization(&htim3, &sMasterConfig) != HAL_OK)
  {
    Error_Handler();
  }
  sConfigOC.OCMode = TIM_OCMODE_PWM1;
  sConfigOC.Pulse = 3600;
  sConfigOC.OCPolarity = TIM_OCPOLARITY_HIGH;
  sConfigOC.OCFastMode = TIM_OCFAST_DISABLE;
  if (HAL_TIM_PWM_ConfigChannel(&htim3, &sConfigOC, TIM_CHANNEL_1) != HAL_OK)
  {
    Error_Handler();
  }
```

```
  sConfigOC.OCMode = TIM_OCMODE_ACTIVE;
  if (HAL_TIM_OC_ConfigChannel(&htim3, &sConfigOC, TIM_CHANNEL_2) != HAL_OK)
  {
    Error_Handler();
  }
  /* USER CODE BEGIN TIM3_Init 2 */

  /* USER CODE END TIM3_Init 2 */
  HAL_TIM_MspPostInit(&htim3);

}

/**
  * @brief TIM4 Initialization Function
  * @param None
  * @retval None
  */
static void MX_TIM4_Init(void)
{

  /* USER CODE BEGIN TIM4_Init 0 */

  /* USER CODE END TIM4_Init 0 */

  TIM_MasterConfigTypeDef sMasterConfig = {0};
  TIM_OC_InitTypeDef sConfigOC = {0};

  /* USER CODE BEGIN TIM4_Init 1 */

  /* USER CODE END TIM4_Init 1 */
  htim4.Instance = TIM4;
  htim4.Init.Prescaler = 25-1;
  htim4.Init.CounterMode = TIM_COUNTERMODE_UP;
  htim4.Init.Period = 7200-1;
  htim4.Init.ClockDivision = TIM_CLOCKDIVISION_DIV1;
  htim4.Init.AutoReloadPreload = TIM_AUTORELOAD_PRELOAD_DISABLE;
  if (HAL_TIM_PWM_Init(&htim4) != HAL_OK)
  {
    Error_Handler();
  }
  if (HAL_TIM_OC_Init(&htim4) != HAL_OK)
  {
    Error_Handler();
  }
  sMasterConfig.MasterOutputTrigger = TIM_TRGO_OC2REF;
  sMasterConfig.MasterSlaveMode = TIM_MASTERSLAVEMODE_DISABLE;
  if (HAL_TIMEx_MasterConfigSynchronization(&htim4, &sMasterConfig) != HAL_OK)
  {
    Error_Handler();
  }
  sConfigOC.OCMode = TIM_OCMODE_PWM1;
  sConfigOC.Pulse = 3600;
  sConfigOC.OCPolarity = TIM_OCPOLARITY_HIGH;
  sConfigOC.OCFastMode = TIM_OCFAST_DISABLE;
  if (HAL_TIM_PWM_ConfigChannel(&htim4, &sConfigOC, TIM_CHANNEL_1) != HAL_OK)
  {
    Error_Handler();
  }
  sConfigOC.OCMode = TIM_OCMODE_ACTIVE;
  if (HAL_TIM_OC_ConfigChannel(&htim4, &sConfigOC, TIM_CHANNEL_2) != HAL_OK)
  {
    Error_Handler();
  }
  /* USER CODE BEGIN TIM4_Init 2 */

  /* USER CODE END TIM4_Init 2 */
  HAL_TIM_MspPostInit(&htim4);
```

```
}

/**
  * Enable DMA controller clock
  */
static void MX_DMA_Init(void)
{

  /* DMA controller clock enable */
  __HAL_RCC_DMA1_CLK_ENABLE();

  /* DMA interrupt init */
  /* DMA1_Channel1_IRQn interrupt configuration */
  HAL_NVIC_SetPriority(DMA1_Channel1_IRQn, 15, 0);
  HAL_NVIC_EnableIRQ(DMA1_Channel1_IRQn);

}

/**
  * @brief GPIO Initialization Function
  * @param None
  * @retval None
  */
static void MX_GPIO_Init(void)
{
/* USER CODE BEGIN MX_GPIO_Init_1 */
/* USER CODE END MX_GPIO_Init_1 */

  /* GPIO Ports Clock Enable */
  __HAL_RCC_GPIOC_CLK_ENABLE();
  __HAL_RCC_GPIOA_CLK_ENABLE();
  __HAL_RCC_GPIOB_CLK_ENABLE();

/* USER CODE BEGIN MX_GPIO_Init_2 */
/* USER CODE END MX_GPIO_Init_2 */
}

/* USER CODE BEGIN 4 */

/* USER CODE END 4 */

/**
  * @brief  This function is executed in case of error occurrence.
  * @retval None
  */
void Error_Handler(void)
{
  /* USER CODE BEGIN Error_Handler_Debug */
  /* User can add his own implementation to report the HAL error return state */
  __disable_irq();
  while (1)
  {
  }
  /* USER CODE END Error_Handler_Debug */
}

#ifdef  USE_FULL_ASSERT
/**
  * @brief  Reports the name of the source file and the source line number
  *         where the assert_param error has occurred.
  * @param  file: pointer to the source file name
  * @param  line: assert_param error line source number
  * @retval None
  */
void assert_failed(uint8_t *file, uint32_t line)
{
```

```
  /* USER CODE BEGIN 6 */
  /* User can add his own implementation to report the file name and line number,
     ex: printf("Wrong parameters value: file %s on line %d\r\n", file, line) */
  /* USER CODE END 6 */
}
#endif /* USE_FULL_ASSERT */
```

A.2 SPWM

```
    /* USER CODE BEGIN Header */
/**
  ******************************************************************************
  * @file           : main.c
  * @brief          : Main program body
  ******************************************************************************
  * @attention
  *
  * Copyright (c) 2025 STMicroelectronics.
  * All rights reserved.
  *
  * This software is licensed under terms that can be found in the LICENSE file
  * in the root directory of this software component.
  * If no LICENSE file comes with this software, it is provided AS-IS.
  *
  ******************************************************************************
  */
/* USER CODE END Header */
/* Includes ------------------------------------------------------------------*/
#include "main.h"
#include "math.h"
/* Private includes ----------------------------------------------------------*/
/* USER CODE BEGIN Includes */

/* USER CODE END Includes */

/* Private typedef -----------------------------------------------------------*/
/* USER CODE BEGIN PTD */

/* USER CODE END PTD */

/* Private define ------------------------------------------------------------*/
/* USER CODE BEGIN PD */

/* USER CODE END PD */

/* Private macro -------------------------------------------------------------*/
/* USER CODE BEGIN PM */

/* USER CODE END PM */

/* Private variables ---------------------------------------------------------*/
TIM_HandleTypeDef htim1;
TIM_HandleTypeDef htim2;

UART_HandleTypeDef huart2;

/* USER CODE BEGIN PV */

/* USER CODE END PV */

/* Private function prototypes -----------------------------------------------*/
void SystemClock_Config(void);
static void MX_GPIO_Init(void);
static void MX_USART2_UART_Init(void);
static void MX_TIM1_Init(void);
```

```
static void MX_TIM2_Init(void);
/* USER CODE BEGIN PFP */
uint16_t sine;  // Sine lookup table
uint16_t i =0;
uint32_t resolution = 20000;
uint16_t frequency = 545;
uint16_t pi =3.14;
/* USER CODE END PFP */

/* Private user code ---------------------------------------------------------*/
/* USER CODE BEGIN 0 */

// Generate sine lookup table
//void generateSineTable() {
//    for (uint8_t i = 0; i < 3600; i++) {
//        sine = (uint16_t)((7200) * (0.5 + 0.45*sin(2 * M_PI * i *400 /3600)));
//    }
//}

// Timer interrupt callback
void HAL_TIM_PeriodElapsedCallback(TIM_HandleTypeDef *htim) {


 sine = (uint16_t)((1800) * (0.5 + 0.45*sin(2 * M_PI  *frequency * i/resolution)));

 if (htim->Instance == TIM2) {
        __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_1, sine);
        __HAL_TIM_SET_COMPARE(&htim1, TIM_CHANNEL_2, sine);
        i++;
        if(i>= resolution)
        {
         i=0;
        }
    }
}

/* USER CODE END 0 */

/**
  * @brief  The application entry point.
  * @retval int
  */
int main(void)
{

  /* USER CODE BEGIN 1 */

  /* USER CODE END 1 */

  /* MCU Configuration--------------------------------------------------------*/

  /* Reset of all peripherals, Initializes the Flash interface and the Systick. */
  HAL_Init();

  /* USER CODE BEGIN Init */

  /* USER CODE END Init */

  /* Configure the system clock */
  SystemClock_Config();

  /* USER CODE BEGIN SysInit */

  /* USER CODE END SysInit */

  /* Initialize all configured peripherals */
  MX_GPIO_Init();
```

```
  MX_USART2_UART_Init();
  MX_TIM1_Init();
  MX_TIM2_Init();
  /* USER CODE BEGIN 2 */
//     generateSineTable();
     HAL_TIM_PWM_Start(&htim1, TIM_CHANNEL_1);
     HAL_TIMEx_PWMN_Start(&htim1, TIM_CHANNEL_1);
     HAL_TIM_PWM_Start(&htim1, TIM_CHANNEL_2);
     HAL_TIMEx_PWMN_Start(&htim1, TIM_CHANNEL_2);
     HAL_TIM_Base_Start_IT(&htim2);

  /* USER CODE END 2 */

  /* Infinite loop */
  /* USER CODE BEGIN WHILE */
  while (1)
  {
    /* USER CODE END WHILE */

    /* USER CODE BEGIN 3 */
  }
  /* USER CODE END 3 */
}

/**
  * @brief System Clock Configuration
  * @retval None
  */
void SystemClock_Config(void)
{
  RCC_OscInitTypeDef RCC_OscInitStruct = {0};
  RCC_ClkInitTypeDef RCC_ClkInitStruct = {0};

  /** Configure the main internal regulator output voltage
  */
  if (HAL_PWREx_ControlVoltageScaling(PWR_REGULATOR_VOLTAGE_SCALE1) != HAL_OK)
  {
    Error_Handler();
  }

  /** Initializes the RCC Oscillators according to the specified parameters
  * in the RCC_OscInitTypeDef structure.
  */
  RCC_OscInitStruct.OscillatorType = RCC_OSCILLATORTYPE_HSI;
  RCC_OscInitStruct.HSIState = RCC_HSI_ON;
  RCC_OscInitStruct.HSICalibrationValue = RCC_HSICALIBRATION_DEFAULT;
  RCC_OscInitStruct.PLL.PLLState = RCC_PLL_ON;
  RCC_OscInitStruct.PLL.PLLSource = RCC_PLLSOURCE_HSI;
  RCC_OscInitStruct.PLL.PLLM = 1;
  RCC_OscInitStruct.PLL.PLLN = 9;
  RCC_OscInitStruct.PLL.PLLP = RCC_PLLP_DIV7;
  RCC_OscInitStruct.PLL.PLLQ = RCC_PLLQ_DIV2;
  RCC_OscInitStruct.PLL.PLLR = RCC_PLLR_DIV2;
  if (HAL_RCC_OscConfig(&RCC_OscInitStruct) != HAL_OK)
  {
    Error_Handler();
  }

  /** Initializes the CPU, AHB and APB buses clocks
  */
  RCC_ClkInitStruct.ClockType = RCC_CLOCKTYPE_HCLK|RCC_CLOCKTYPE_SYSCLK
                              |RCC_CLOCKTYPE_PCLK1|RCC_CLOCKTYPE_PCLK2;
  RCC_ClkInitStruct.SYSCLKSource = RCC_SYSCLKSOURCE_PLLCLK;
  RCC_ClkInitStruct.AHBCLKDivider = RCC_SYSCLK_DIV1;
  RCC_ClkInitStruct.APB1CLKDivider = RCC_HCLK_DIV1;
  RCC_ClkInitStruct.APB2CLKDivider = RCC_HCLK_DIV1;
```

```
  if (HAL_RCC_ClockConfig(&RCC_ClkInitStruct, FLASH_LATENCY_4) != HAL_OK)
  {
    Error_Handler();
  }
}

/**
  * @brief TIM1 Initialization Function
  * @param None
  * @retval None
  */
static void MX_TIM1_Init(void)
{

  /* USER CODE BEGIN TIM1_Init 0 */

  /* USER CODE END TIM1_Init 0 */

  TIM_ClockConfigTypeDef sClockSourceConfig = {0};
  TIM_MasterConfigTypeDef sMasterConfig = {0};
  TIM_OC_InitTypeDef sConfigOC = {0};
  TIM_BreakDeadTimeConfigTypeDef sBreakDeadTimeConfig = {0};

  /* USER CODE BEGIN TIM1_Init 1 */

  /* USER CODE END TIM1_Init 1 */
  htim1.Instance = TIM1;
  htim1.Init.Prescaler = 0;
  htim1.Init.CounterMode = TIM_COUNTERMODE_CENTERALIGNED1;
  htim1.Init.Period = 1800-1;
  htim1.Init.ClockDivision = TIM_CLOCKDIVISION_DIV1;
  htim1.Init.RepetitionCounter = 0;
  htim1.Init.AutoReloadPreload = TIM_AUTORELOAD_PRELOAD_ENABLE;
  if (HAL_TIM_Base_Init(&htim1) != HAL_OK)
  {
    Error_Handler();
  }
  sClockSourceConfig.ClockSource = TIM_CLOCKSOURCE_INTERNAL;
  if (HAL_TIM_ConfigClockSource(&htim1, &sClockSourceConfig) != HAL_OK)
  {
    Error_Handler();
  }
  if (HAL_TIM_PWM_Init(&htim1) != HAL_OK)
  {
    Error_Handler();
  }
  sMasterConfig.MasterOutputTrigger = TIM_TRGO_RESET;
  sMasterConfig.MasterOutputTrigger2 = TIM_TRGO2_RESET;
  sMasterConfig.MasterSlaveMode = TIM_MASTERSLAVEMODE_DISABLE;
  if (HAL_TIMEx_MasterConfigSynchronization(&htim1, &sMasterConfig) != HAL_OK)
  {
    Error_Handler();
  }
  sConfigOC.OCMode = TIM_OCMODE_PWM1;
  sConfigOC.Pulse = 0;
  sConfigOC.OCPolarity = TIM_OCPOLARITY_HIGH;
  sConfigOC.OCNPolarity = TIM_OCNPOLARITY_HIGH;
  sConfigOC.OCFastMode = TIM_OCFAST_DISABLE;
  sConfigOC.OCIdleState = TIM_OCIDLESTATE_SET;
  sConfigOC.OCNIdleState = TIM_OCNIDLESTATE_RESET;
  if (HAL_TIM_PWM_ConfigChannel(&htim1, &sConfigOC, TIM_CHANNEL_1) != HAL_OK)
  {
    Error_Handler();
  }
  if (HAL_TIM_PWM_ConfigChannel(&htim1, &sConfigOC, TIM_CHANNEL_2) != HAL_OK)
  {
    Error_Handler();
```

```
  }
  sBreakDeadTimeConfig.OffStateRunMode = TIM_OSSR_DISABLE;
  sBreakDeadTimeConfig.OffStateIDLEMode = TIM_OSSI_DISABLE;
  sBreakDeadTimeConfig.LockLevel = TIM_LOCKLEVEL_OFF;
  sBreakDeadTimeConfig.DeadTime = 100;
  sBreakDeadTimeConfig.BreakState = TIM_BREAK_DISABLE;
  sBreakDeadTimeConfig.BreakPolarity = TIM_BREAKPOLARITY_HIGH;
  sBreakDeadTimeConfig.BreakFilter = 0;
  sBreakDeadTimeConfig.Break2State = TIM_BREAK2_DISABLE;
  sBreakDeadTimeConfig.Break2Polarity = TIM_BREAK2POLARITY_HIGH;
  sBreakDeadTimeConfig.Break2Filter = 0;
  sBreakDeadTimeConfig.AutomaticOutput = TIM_AUTOMATICOUTPUT_DISABLE;
  if (HAL_TIMEx_ConfigBreakDeadTime(&htim1, &sBreakDeadTimeConfig) != HAL_OK)
  {
    Error_Handler();
  }
  /* USER CODE BEGIN TIM1_Init 2 */

  /* USER CODE END TIM1_Init 2 */
  HAL_TIM_MspPostInit(&htim1);

}

/**
  * @brief TIM2 Initialization Function
  * @param None
  * @retval None
  */
static void MX_TIM2_Init(void)
{

  /* USER CODE BEGIN TIM2_Init 0 */

  /* USER CODE END TIM2_Init 0 */

  TIM_ClockConfigTypeDef sClockSourceConfig = {0};
  TIM_MasterConfigTypeDef sMasterConfig = {0};

  /* USER CODE BEGIN TIM2_Init 1 */

  /* USER CODE END TIM2_Init 1 */
  htim2.Instance = TIM2;
  htim2.Init.Prescaler = 0;
  htim2.Init.CounterMode = TIM_COUNTERMODE_UP;
  htim2.Init.Period = 1800-1;
  htim2.Init.ClockDivision = TIM_CLOCKDIVISION_DIV1;
  htim2.Init.AutoReloadPreload = TIM_AUTORELOAD_PRELOAD_ENABLE;
  if (HAL_TIM_Base_Init(&htim2) != HAL_OK)
  {
    Error_Handler();
  }
  sClockSourceConfig.ClockSource = TIM_CLOCKSOURCE_INTERNAL;
  if (HAL_TIM_ConfigClockSource(&htim2, &sClockSourceConfig) != HAL_OK)
  {
    Error_Handler();
  }
  sMasterConfig.MasterOutputTrigger = TIM_TRGO_RESET;
  sMasterConfig.MasterSlaveMode = TIM_MASTERSLAVEMODE_DISABLE;
  if (HAL_TIMEx_MasterConfigSynchronization(&htim2, &sMasterConfig) != HAL_OK)
  {
    Error_Handler();
  }
  /* USER CODE BEGIN TIM2_Init 2 */

  /* USER CODE END TIM2_Init 2 */

}
```

```
/**
  * @brief USART2 Initialization Function
  * @param None
  * @retval None
  */
static void MX_USART2_UART_Init(void)
{

  /* USER CODE BEGIN USART2_Init 0 */

  /* USER CODE END USART2_Init 0 */

  /* USER CODE BEGIN USART2_Init 1 */

  /* USER CODE END USART2_Init 1 */
  huart2.Instance = USART2;
  huart2.Init.BaudRate = 115200;
  huart2.Init.WordLength = UART_WORDLENGTH_8B;
  huart2.Init.StopBits = UART_STOPBITS_1;
  huart2.Init.Parity = UART_PARITY_NONE;
  huart2.Init.Mode = UART_MODE_TX_RX;
  huart2.Init.HwFlowCtl = UART_HWCONTROL_NONE;
  huart2.Init.OverSampling = UART_OVERSAMPLING_16;
  huart2.Init.OneBitSampling = UART_ONE_BIT_SAMPLE_DISABLE;
  huart2.AdvancedInit.AdvFeatureInit = UART_ADVFEATURE_NO_INIT;
  if (HAL_UART_Init(&huart2) != HAL_OK)
  {
    Error_Handler();
  }
  /* USER CODE BEGIN USART2_Init 2 */

  /* USER CODE END USART2_Init 2 */

}

/**
  * @brief GPIO Initialization Function
  * @param None
  * @retval None
  */
static void MX_GPIO_Init(void)
{
  GPIO_InitTypeDef GPIO_InitStruct = {0};
  /* USER CODE BEGIN MX_GPIO_Init_1 */

  /* USER CODE END MX_GPIO_Init_1 */

  /* GPIO Ports Clock Enable */
  __HAL_RCC_GPIOC_CLK_ENABLE();
  __HAL_RCC_GPIOH_CLK_ENABLE();
  __HAL_RCC_GPIOA_CLK_ENABLE();
  __HAL_RCC_GPIOB_CLK_ENABLE();

  /*Configure GPIO pin Output Level */
  HAL_GPIO_WritePin(LD2_GPIO_Port, LD2_Pin, GPIO_PIN_RESET);

  /*Configure GPIO pin : B1_Pin */
  GPIO_InitStruct.Pin = B1_Pin;
  GPIO_InitStruct.Mode = GPIO_MODE_IT_FALLING;
  GPIO_InitStruct.Pull = GPIO_NOPULL;
  HAL_GPIO_Init(B1_GPIO_Port, &GPIO_InitStruct);

  /*Configure GPIO pin : LD2_Pin */
  GPIO_InitStruct.Pin = LD2_Pin;
  GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
  GPIO_InitStruct.Pull = GPIO_NOPULL;
```

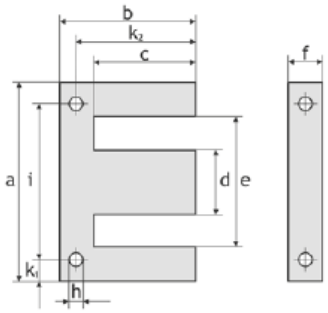
```
  GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
  HAL_GPIO_Init(LD2_GPIO_Port, &GPIO_InitStruct);

  /* USER CODE BEGIN MX_GPIO_Init_2 */

  /* USER CODE END MX_GPIO_Init_2 */
}

/* USER CODE BEGIN 4 */

/* USER CODE END 4 */

/**
  * @brief  This function is executed in case of error occurrence.
  * @retval None
  */
void Error_Handler(void)
{
  /* USER CODE BEGIN Error_Handler_Debug */
  /* User can add his own implementation to report the HAL error return state */
  __disable_irq();
  while (1)
  {
  }
  /* USER CODE END Error_Handler_Debug */
}

#ifdef  USE_FULL_ASSERT
/**
  * @brief  Reports the name of the source file and the source line number
  *         where the assert_param error has occurred.
  * @param  file: pointer to the source file name
  * @param  line: assert_param error line source number
  * @retval None
  */
void assert_failed(uint8_t *file, uint32_t line)
{
  /* USER CODE BEGIN 6 */
  /* User can add his own implementation to report the file name and line number,
     ex: printf("Wrong parameters value: file %s on line %d\r\n", file, line) */
  /* USER CODE END 6 */
}
#endif /* USE_FULL_ASSERT */
```

This appendix consists of the data of the core material of the transformer received from the manufacturer.

Appendix B Core details

This appendix consists of the data of the core material of the transformer received from the manufacturer. The image B.1 shows the EI plates details (EI-240) selected for the project from Waasner. The complete catalogue can be found on the Waasner's website under the name ready core laminations. The two PDFs show the core's performance at 400 Hz, and permiability data for different frequencies respectively.

EI-KERNBLECHE / EI-CORE LAMINATIONS

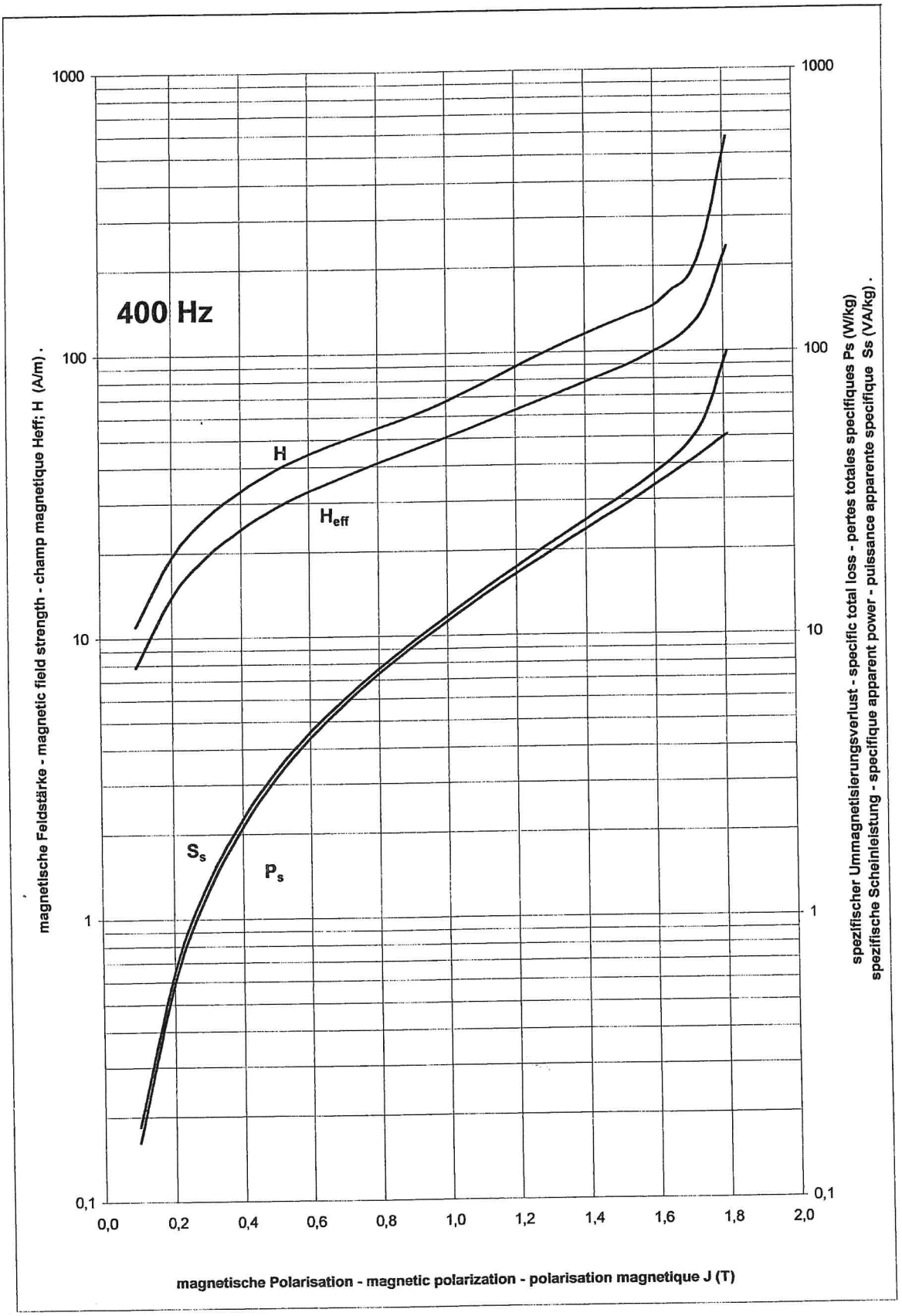


Bestell-Nr. Order-No.	Typ Type	IEC	a	b	c	d	e	f	h	i	k_1	k_2
11.005	EI 30	YEI 1 - 10	30,0	20,0	15,0	10,0	20,0	5,0	0,0	0,0	0,00	0,00
11.010	EI 38	YEI 1 - 13	38,4	25,6	19,2	12,8	25,6	6,4	0,0	0,0	0,00	0,00
11.020	EI 42	YEI 1 - 14	42,0	28,0	21,0	14,0	28,0	7,0	3,5	35,0	3,50	24,50
11.030	EI 48	YEI 1 - 16	48,0	32,0	24,0	16,0	32,0	8,0	3,5	40,0	4,00	28,00
11.040	EI 54	YEI 1 - 18	54,0	36,0	27,0	18,0	36,0	9,0	3,5	45,0	4,50	31,50
11.050	EI 60	YEI 1 - 20	60,0	40,0	30,0	20,0	40,0	10,0	3,5	50,0	5,00	35,00
11.060	EI 66	YEI 1 - 22	66,0	44,0	33,0	22,0	44,0	11,0	4,5	55,0	5,50	38,50
11.085	EI 75	YEI 1 - 25	75,0	50,0	37,5	25,0	50,0	12,5	4,5	62,5	6,25	43,75
11.095	EI 78		78,0	52,0	39,0	26,0	52,0	13,0	4,5	65,0	6,50	45,50
11.110	EI 84	YEI 1 - 28	84,0	56,0	42,0	28,0	56,0	14,0	4,5	70,0	7,00	49,00
11.120	EI 90		90,0	60,0	45,0	30,0	60,0	15,0	4,5	75,0	7,50	52,50
11.130	EI 96	YEI 1 - 32	96,0	64,0	48,0	32,0	64,0	16,0	5,5	80,0	8,00	56,00
11.140	EI 105		105,0	70,0	52,5	35,0	70,0	17,5	5,5	87,5	8,75	61,25
11.150	EI 108	YEI 1 - 36	108,0	72,0	54,0	36,0	72,0	18,0	5,5	90,0	9,00	63,00
11.160	EI 120	YEI 1 - 40	120,0	80,0	60,0	40,0	80,0	20,0	7,0	100,0	10,00	70,00
11.170	EI 126		126,0	84,0	63,0	42,0	84,0	21,0	7,0	105,0	10,50	73,50
11.180	EI 135		135,0	90,0	67,5	45,0	90,0	22,5	7,5	112,5	11,25	78,75
11.190	EI 150 N	YEI 1 - 50	150,0	100,0	75,0	50,0	100,0	25,0	8,0	125,0	12,50	87,50
11.200	EI 174	YEI 1 - 58	174,0	116,0	87,0	58,0	116,0	29,0	10,5	145,0	14,50	101,50
11.202	EI 180		180,0	120,0	90,0	60,0	120,0	30,0	10,0	150,0	15,00	105,00
11.210	EI 192	YEI 1 - 64	192,0	128,0	96,0	64,0	128,0	32,0	11,0	160,0	16,00	112,00
11.213	EI 240	YEI 1 - 80	240,0	160,0	120,0	80,0	160,0	40,0	11,5	200,0	20,00	140,00

Figure B.1: Selected EI plates catalogue

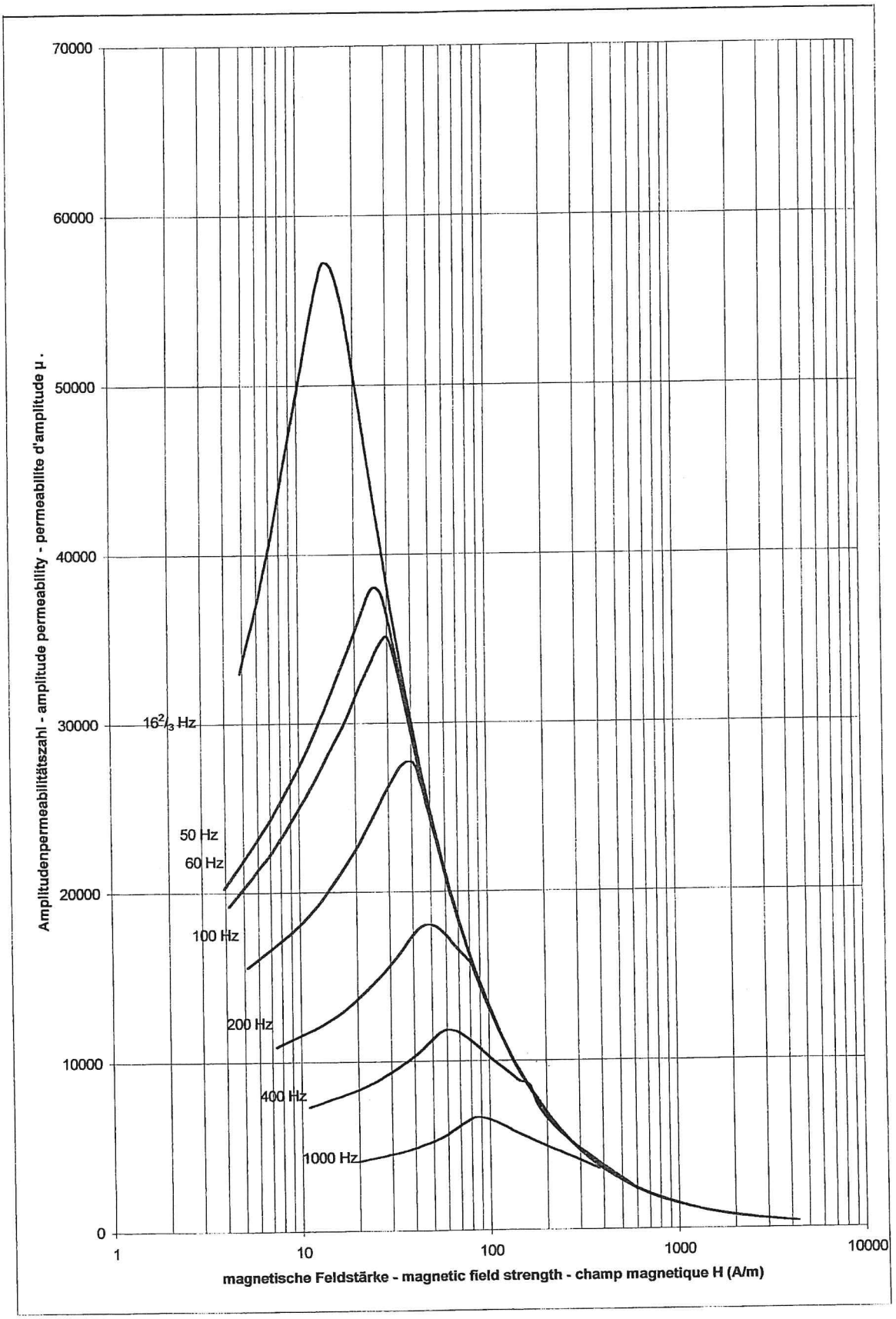
Material M 165-35 S

Messung an entspannten Epsteinproben
Magnetisierung in Walzrichtung



Material M 165-35 S

Messung an entspannten Epsteinproben
Magnetisierung in Walzrichtung



Appendix C Matlab Codes

This appendix contains all the MATLAB codes used for calculations and data extraction.

C.1 Code for transformer calculations

```
    clc;
clear all;
close all;

% Transformer specifications
V_pri = 750;
I_pri = 12.5;
V_sec1 = 300;
I_sec1 = 18.8;
V_sec2 = 144;
I_sec2 = 27.5;
f = 400;
PF = 0.8;

% Transformer constants
kj = 534; % constant for Ap as per book
ku = 0.4; % packing factor
kf = 4; % Square wave
kv = 19.7; % Constant for volume as per book - not used
kw = 68.2; % Constant for weight as per book - used to calulate weight

% Wire Data
Wire_r = 1.8/20; % cm 14 AWG wire
Wire_area = pi * Wire_r^2;
W_res = 82.8e-6; % Ohms per cm  from book and from online sources
W_res_sec_2 = 37.3e-6;

% Number of Wires taken approximately from online data for current and
% what was used last time
Wire_n_pri = 2;
Wire_n_sec1 = 2;
Wire_n_sec2 = 1;


% Current densities calculated
J_pri = I_pri/(Wire_area*Wire_n_pri);
J_sec1 = I_sec1/(Wire_area*Wire_n_sec1);
J_sec2 = I_sec2/(0.045*Wire_n_sec2);

% Core parameters Assuming a square core for simplicity
e=16;
l_core = 8; % cm
b_core = 8; % cm
A_core = l_core * b_core;
h = 12; % cm This is the height of the core

%Weight of core
Number_of_sheets = round(b_core/.035);
Area_of_sheet = 20*24 - (16-8)*12;
Volume_of_sheet = Area_of_sheet*0.035;
Total_volume = Volume_of_sheet*Number_of_sheets; % cm3
Weight = Total_volume*7.6/1000;

% Given Bmax and Ps values. Values taken from the data for the NO/NGO steel
Bmax_values = [0.2, 0.3, 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1, 1.1, 1.2, 1.3, 1.4, 1.5, 1.6, 1.7, 1.8];
Ps_values = [0.6, 1.5, 2, 3.2, 4.5, 6, 7.5, 9, 12, 15, 18, 21, 25, 28, 35, 40, 50];

% Arrays for plotting
Total_losses = zeros(size(Bmax_values));
Window_Area = zeros(size(Bmax_values));
N1_values = zeros(size(Bmax_values));
Total_wire_length_values = zeros(size(Bmax_values));
Pcore_arr = zeros(size(Bmax_values));
```

```
Pcu_total_arr = zeros(size(Bmax_values));
Area_product = zeros(size(Bmax_values));
EMF = zeros(size(Bmax_values));
Final_length = zeros(size(Bmax_values));
Pri_length = zeros(size(Bmax_values));
Sec1_length = zeros(size(Bmax_values));
Sec2_length = zeros(size(Bmax_values));

% Loop through each Bmax and corresponding Ps
for i = 1:length(Bmax_values)
    Bmax = Bmax_values(i);
    Ps = Ps_values(i);

    sigma_VA = (V_pri * I_pri + V_sec1 * I_sec1 + V_sec2 * I_sec2);

    % Area Product
    A_p = ((sigma_VA * 10^4) / (J_pri * kf * f * Bmax * ku*PF));
    Area_product(i) = A_p;

    % Output volt-per-turn calculation
    V_N = A_core * f * Bmax * kf / 10000;
    N1 = round(V_pri / V_N);
    N2 = round(V_sec1 / V_N);
    N3 = round(V_sec2 / V_N);
    N1_values(i) = N1;
    EMF(i) =V_N;


    % Bobbin Area
    Effective_h = h - 2; % cm deratig h by 2cm
    N_turns_in_h = round(0.8 * Effective_h / (2 * Wire_r))+1; % Turns that covers the height 1 time
    N_turns_in_h_s2 = round(0.8 * Effective_h / (1))+1;
    N_h_pri = (N1 * Wire_n_pri / N_turns_in_h);
    N_h_sec1 = (N2 * Wire_n_sec1 / N_turns_in_h);
    N_h_sec2 = (N3 * Wire_n_sec2 / N_turns_in_h_s2);

    h_covererd = round(N_h_pri + N_h_sec1 + N_h_sec2) + 1; % Total times height is covered
    final_l = (l_core + (2 * h_covererd * Wire_r * 2)) +2;
    final_b = (b_core + (2 * h_covererd * Wire_r * 2)) +2;

    Final_length(i)= (final_l - l_core)/2;

    % Window Area Calculation
    Wa_Ap = A_p / A_core;
    Wa_calculated = h * (final_l - l_core)/2;

    % Wire length calculation
    length_pri = 0;
    for n = 0:(N_h_pri-1)
        length_pri = length_pri + 2 * N_turns_in_h * (l_core + b_core + 4 * n * 2 * Wire_r);
    end
    P_Cu_pri = I_pri^2 * length_pri * W_res / Wire_n_pri;

    length_sec1 = 0;
    for n = 1:N_h_sec1
        length_sec1 = length_sec1 + 2 * N_turns_in_h * (l_core+2 + b_core + 4 * n * 2 * Wire_r);
    end
    P_Cu_sec1 = I_sec1^2 * length_sec1 * W_res / Wire_n_sec1;

    length_sec2 = 0;
    for n = 1:N_h_sec2
        length_sec2 = length_sec2 + 2 * N_turns_in_h_s2 * (l_core+4 + b_core + 4 * n * 2 * 0.045);
    end
    P_Cu_sec2 = I_sec2^2 * length_sec2 * W_res_sec_2 / Wire_n_sec2;

    Pri_length(i)  = length_pri;
    Sec1_length(i) = length_sec1;
```

```
    Sec2_length(i) = length_sec2;


    % Total wire length
    Total_wire_length = (length_pri + length_sec1 + length_sec2) / 100;
    Total_wire_length_values(i) = Total_wire_length;

    % Total losses
    P_Cu = P_Cu_pri + P_Cu_sec1 + P_Cu_sec2;
    Pcu_total_arr(i) = P_Cu;
    P_core = Ps * Weight;
    Pcore_arr(i) = P_core;
    Total_losses(i) = P_core + P_Cu;
    Window_Area(i) = Wa_calculated;
end

% Plot the results
figure;

plot(Bmax_values, Total_losses, '-o', 'LineWidth', 2, 'MarkerSize', 6);
ylabel('Total Losses (W)', 'FontSize', 14);
hold on;

% Uncomment if needed:
% yyaxis right;
% plot(Bmax_values, Window_Area, '-s', 'LineWidth', 1.5, 'MarkerSize', 6, 'Color', 'r');
% ylabel('Window Area (cm^2)', 'FontSize', 14);

% Add a horizontal line at Wa = 96
% yline(h*(e - l_core)/2, '--k', 'Cutoff', 'LineWidth', 1.5, 'FontSize', 12);

xlabel('B_{max} (T)', 'FontSize', 14);
title('B_{max} vs Total Losses', 'FontSize', 16);
legend('Total Losses', 'Location', 'northwest', 'FontSize', 14);
grid on;
hold off;

% xlabel('Bmax (T)');
% title('Bmax vs Total Losses & Window Area');
% legend('Total Losses', 'Window Area', 'Location', 'northwest');
% grid on;
% hold off;

% Plot Bmax vs N1 and Total Wire Length with separate Y-axes
figure;
yyaxis left;
plot(Bmax_values, N1_values, '-o', 'LineWidth', 1.5, 'MarkerSize', 6);
ylabel('N1 (Turns)');

yyaxis right;
plot(Bmax_values, Total_wire_length_values, '-s', 'LineWidth', 1.5, 'MarkerSize', 6, 'Color', 'r');
ylabel('Total Wire Length (m)');

xlabel('Bmax (T)');
title('Bmax vs N1 and Total Wire Length');
grid on;

figure;
plot(Bmax_values, Pcore_arr, 'r-o', 'LineWidth', 2);
hold on;
plot(Bmax_values, Pcu_total_arr, 'b-s', 'LineWidth', 2);

xlabel('B_{max} (T)', 'FontSize', 14);
ylabel('Power (W)', 'FontSize', 14);
title('B_{max} vs P_{core} and P_{cu total}', 'FontSize', 16);
legend('P_{core}', 'P_{cu total}', 'FontSize', 14);
```

```
% Optionally increase tick font size without set/gca? Not directly.


figure;
plot(Bmax_values, Area_product, 'r-o', 'LineWidth', 1.5);
xlabel('B_{max} (T)');
ylabel('Area Product');
title('Graph: B_{max} vs Area product');
grid on;

figure;
plot(Bmax_values, EMF, 'r-o', 'LineWidth', 1.5);
xlabel('B_{max} (T)');
ylabel('Volts per turn');
title('Graph: B_{max} vs Volts per turn');
grid on;

figure;
plot(Bmax_values, Area_product/A_core, 'r-o', 'LineWidth', 1.5);
xlabel('B_{max} (T)');
ylabel('Winidow area required as per area core and area product');
title('Graph: B_{max} vs Required window area');
grid on;

figure;
plot(Bmax_values, Final_length, 'r-o', 'LineWidth', 1.5);
xlabel('B_{max} (T)');
ylabel('Length of the window covered by wire');
yline((e-l_core)/2, '--k', 'Cutoff', 'LineWidth', 1.5);
title('Graph: B_{max} vs Length of the window covered by wire ');
grid on;

figure;
plot(Bmax_values, Pri_length/100, 'r-o', 'LineWidth', 1.5);
xlabel('B_{max} (T)');
ylabel('length of wire primary');

title('Graph: B_{max} vs length of wire primary ');
grid on;

figure;
plot(Bmax_values, Sec1_length/100, 'r-o', 'LineWidth', 1.5);
xlabel('B_{max} (T)');
ylabel('length of wire Sec1');
title('Graph: B_{max} vs length of wire Sec1 ');
grid on;


figure;
plot(Bmax_values, Sec2_length/100, 'r-o', 'LineWidth', 1.5);
xlabel('B_{max} (T)');
ylabel('length of wire primary');
title('Graph: B_{max} vs length of wire sec2 ');
grid on;
```

C.2 Open circuit test data

The below code is used for extraction and calculation of open circuit test for the secondary 1 side. Similar code is used for processing the data of secondary 2 side with necessary modifications.

```
    clc;
clear all;

% === CSV Files and Frequencies ===
csv_files = {
```

```
    'T0051.csv',
    'T0052.csv',
    'T0053.csv',
    'T0054.csv',
    'T0055.csv',
};
frequencies = [ 300, 400, 500, 600, 700];

% === Initialize Arrays ===
vin_rms_all = zeros(1, length(csv_files));
iin_rms_all = zeros(1, length(csv_files));
vpri_rms_all = zeros(1, length(csv_files));
vs2_rms_all = zeros(1, length(csv_files));
P_all = zeros(1, length(csv_files));
PF_all = zeros(1, length(csv_files));
Ire_all = zeros(1, length(csv_files));
Im_all = zeros(1, length(csv_files));
Xm_all = zeros(1, length(csv_files));
lm_all = zeros(1, length(csv_files));
Rm_all = zeros(1, length(csv_files));
Lm_pri_all = zeros(1, length(csv_files));
Rm_pri_all = zeros(1, length(csv_files));

% === Loop through files ===
for idx = 1:length(csv_files)
    filename = csv_files{idx};
    frequency = frequencies(idx);

    % === Read Data ===
    data = readmatrix(filename);
    time = data(:, 1);
    vin = data(:, 2);
    iin = data(:, 3);
    vs2 = data(:, 5);
    vpri = data(:, 4);

    % === RMS Calculations ===
    vin_rms = rms(vin);
    iin_rms = rms(iin);
    vpri_rms = rms(vpri);
    vs2_rms = rms(vs2);

    % === Power Calculations ===
    S = vin_rms * iin_rms;
    P = mean(vin .* iin);
    PF = P / S;
    Ire = iin_rms * PF;
    theta = acos(PF);
    Im = iin_rms * sin(theta);
    Xm = vin_rms / Im;
    lm = Xm / (2 * pi * frequency);
    Rm = P / Ire^2;
    Lm_pri = lm * 2.8^2;
    Rm_pri = Rm * 2.8^2;

    % === Store Values ===
    vin_rms_all(idx) = vin_rms;
    iin_rms_all(idx) = iin_rms;
    vpri_rms_all(idx) = vpri_rms;
    vs2_rms_all(idx) = vs2_rms;
    P_all(idx) = P;
    PF_all(idx) = PF;
    Ire_all(idx) = Ire;
    Im_all(idx) = Im;
    Xm_all(idx) = Xm;
    lm_all(idx) = lm;
    Rm_all(idx) = Rm;
```

```
    Lm_pri_all(idx) = Lm_pri * 1e3;
    Rm_pri_all(idx) = Rm_pri;
end

% === Plot Lm_pri, Rm_pri, P vs Frequency ===
figure('Name','Open circuit test S1 Sine','NumberTitle','off','Color','w');
tiledlayout(3,1,'Padding','compact','TileSpacing','compact');
sgtitle('Open Circuit Test Results for S1 Sine', 'FontSize', 22, 'FontWeight', 'bold');
% Graph styling
lineWidth = 2.5;
axisFontSize = 20;
titleFontSize = 20;

% Plot Lm_pri
nexttile;
plot(frequencies, Lm_pri_all, '-o', 'LineWidth', lineWidth, 'Color',[0 0.4470 0.7410]);
grid on;
xlabel('Frequency (Hz)', 'FontSize', axisFontSize);
ylabel('Lm_{pri} (mH)',     'FontSize', axisFontSize);
title('Magnetizing Inductance Lm_{pri} vs Frequency', 'FontSize', titleFontSize);
set(gca,'FontSize',axisFontSize);

% Plot Rm_pri
nexttile;
plot(frequencies, Rm_pri_all, '-s', 'LineWidth', lineWidth, 'Color',[0.8500 0.3250 0.0980]);
grid on;
xlabel('Frequency (Hz)', 'FontSize', axisFontSize);
ylabel('Rm_{pri} (\Omega)', 'FontSize', axisFontSize);
title('Magnetizing Resistance Rm_{pri} vs Frequency', 'FontSize', titleFontSize);
set(gca,'FontSize',axisFontSize);

% Plot Real Power P
nexttile;
plot(frequencies, P_all, '-^', 'LineWidth', lineWidth, 'Color',[0.4660 0.6740 0.1880]);
grid on;
xlabel('Frequency (Hz)', 'FontSize', axisFontSize);
ylabel('Real Power P (W)',  'FontSize', axisFontSize);
title('Real Power vs Frequency', 'FontSize', titleFontSize);
set(gca,'FontSize',axisFontSize);

% === Export to PNG ===
exportgraphics(gcf, 'OpenCircuitTestS1.png', 'Resolution',300);

% === Create Output Table ===
results_table = table(frequencies.', ...
    vin_rms_all.', iin_rms_all.', vpri_rms_all.', vs2_rms_all.', ...
    P_all.', PF_all.', Ire_all.', Im_all.', Xm_all.', lm_all.', ...
    Rm_all.', Lm_pri_all.', Rm_pri_all.', ...
    'VariableNames', {'Frequency_Hz', ...
    'Vin_RMS', 'Iin_RMS', 'Vpri_RMS', 'Vs1_RMS', ...
    'P', 'PF', 'Ire', 'Im', 'Xm', 'Lm', ...
    'Rm', 'Lm_pri', 'Rm_pri'});

disp(results_table);
fprintf('\n=== Copy-Paste Friendly Table for Google Sheets ===\n');
fprintf(['Freq(Hz)\tIm(A)\tIre(A)\tP(W)\tPF\t', ...
         'Xm(Ohm)\tLm(H)\tRm(Ohm)\tLm_pri(H)\tRm_pri(Ohm)\n']);

fprintf('\n=== Copy-Paste Friendly Table for Google Sheets ===\n');
fprintf(['Freq(Hz)\tVin_RMS(V)\tIin_RMS(A)\tVpri_RMS(V)\tVs2_RMS(V)\t' ...
         'Im(A)\tIre(A)\tP(W)\tPF\tXm(Ohm)\tLm(H)\tRm(Ohm)\tLm_pri(mH)\tRm_pri(Ohm)\n']);

for i = 1:length(frequencies)
    fprintf('%d\t%.4f\t%.4f\t%.4f\t%.4f\t%.4f\t%.4f\t%.4f\t%.4f\t%.4f\t%.4f\t%.6f\t%.4f\t%.6f\t%.4f\n', ...
        frequencies(i), ...
        vin_rms_all(i), iin_rms_all(i), vpri_rms_all(i), vs2_rms_all(i), ...
        Im_all(i), Ire_all(i), P_all(i), PF_all(i), Xm_all(i), ...
```

```
        lm_all(i), Rm_all(i), Lm_pri_all(i), Rm_pri_all(i));
end
```

C.3 Short circuit test data

The below code is used for extraction and calculation of short circuit test for the secondary 1 side with the primary winding excited. Similar code is used for processing the data of secondary other short circuit tests with necessary modifications.

```
    clc;
clear all;

% === CSV filenames and corresponding frequencies ===
filenames = {
    'TEK00118.csv',  % 100 Hz
    'TEK00117.csv',  % 200 Hz
    'TEK00119.csv',  % 300 Hz
    'TEK00116.csv',  % 400 Hz
    'TEK00120.csv',  % 500 Hz
    'TEK00121.csv'   % 600 Hz
};
frequencies = [100, 200, 300, 400, 500, 600];  % Hz

% === Preallocate Arrays ===
vin_rms_all = zeros(size(frequencies));
iin_rms_all = zeros(size(frequencies));
mean_power_all = zeros(size(frequencies));
L_values = zeros(size(frequencies));
R_values = zeros(size(frequencies));
X_values = zeros(size(frequencies));
Z_values = zeros(size(frequencies));

% === Loop through all CSVs ===
for i = 1:length(filenames)

    filename = filenames{i};
    frequency = frequencies(i);

    % === Read CSV file ===
    data = readmatrix(filename);
    data = data(~any(isnan(data), 2), :);  % Remove rows with NaN if any

    % === Extract signals ===
    time = data(:, 1);   % Time (s)
    vin = data(:, 2);    % Input voltage (V)
    iin = data(:, 3);    % Input current (A)
    isc = data(:, 4);    % Short circuit current (A)

    % === RMS Calculations ===
    vin_rms = sqrt(mean(vin.^2));
    iin_rms = sqrt(mean(iin.^2));
    isc_rms = sqrt(mean(isc.^2));

    % === Power Calculation ===
    inst_power = vin .* iin;
    mean_power = mean(inst_power);

    % === Impedance and Reactance ===
    Z = vin_rms / iin_rms;
    R = mean_power / (iin_rms^2);
    X = sqrt(Z^2 - R^2);
    L = X * 1000 / (2 * pi * frequency);  % Convert to mH

    % === Store Values ===
    vin_rms_all(i) = vin_rms;
    iin_rms_all(i) = iin_rms;
    mean_power_all(i) = mean_power;
```

```
    L_values(i) = L;
    R_values(i) = R;
    X_values(i) = X;
    Z_values(i) = Z;

    % === Frequency detection via FFT (Optional) ===
    %{
    Fs = 1 / mean(diff(time));
    N = length(vin);
    vin_fft = abs(fft(vin));
    f_axis = (0:N-1) * Fs / N;
    [~, idx] = max(vin_fft(2:floor(N/2)));
    measured_freq = f_axis(idx + 1);
    fprintf('Detected Frequency: %.2f Hz\n', measured_freq);
    %}
end

% === Create and Display Summary Table ===
results_table = table(frequencies.', ...
    vin_rms_all.', iin_rms_all.', mean_power_all.', ...
    Z_values.', R_values.', X_values.', L_values.', ...
    'VariableNames', {'Frequency_Hz', 'Vin_RMS_V', 'Iin_RMS_A', 'Power_W', ...
                      'Impedance_Z_Ohms', 'Resistance_R_Ohms', ...
                      'Reactance_X_Ohms', 'Inductance_L_mH'});

disp('=== Summary Table ===');
disp(results_table);

% === Plot Results ===
figure('Name', 'Short Circuit Test: Primary to S1 (Zp and Zs1)', 'NumberTitle', 'off');
tiledlayout(3, 1);

% --- Plot 1: Inductance ---
nexttile;
plot(frequencies, L_values, '-o', 'LineWidth', 6, 'Color', [0 0.4470 0.7410]);
grid on;
ylabel('Inductance L (mH)');
title('Inductance vs Frequency');

% --- Plot 2: Reactance ---
nexttile;
plot(frequencies, X_values, '-s', 'LineWidth', 6, 'Color', [0.8500 0.3250 0.0980]);
grid on;
ylabel('Reactance X (Ohms)');
title('Reactance vs Frequency');

% --- Plot 3: Resistance ---
nexttile;
plot(frequencies, R_values, '-d', 'LineWidth', 6, 'Color', [0.4660 0.6740 0.1880]);
grid on;
xlabel('Frequency (Hz)');
ylabel('Resistance R (Ohms)');
title('Resistance vs Frequency');

sgtitle('Short Circuit Test: Primary to S1 (Zp and Zs1)');

fprintf('\n=== Copy-Paste Friendly Table for Google Sheets ===\n');
fprintf('Freq(Hz)\tVin_RMS(V)\tIin_RMS(A)\tPower(W)\tZ(Ohms)\tR(Ohms)\tX(Ohms)\tL(mH)\n');
for i = 1:length(frequencies)
    fprintf('%d\t%.4f\t%.4f\t%.4f\t%.4f\t%.4f\t%.4f\t%.4f\n', ...
        frequencies(i), vin_rms_all(i), iin_rms_all(i), mean_power_all(i), ...
        Z_values(i), R_values(i), X_values(i), L_values(i));
end
```

The code below is used for calculating the values of Ls_1, Ls_2, and Ls_3.

```
    clc
clear all
```

```
% === Given Data ===
Frequency = [100, 200, 300, 400, 500, 600];

L12_mH = [0.4322, 0.3943, 0.3833, 0.3818, 0.3816, 0.3790]; % in mH
L13_mH = [0.9137, 0.8128, 0.7832, 0.7782, 0.7809, 0.7800]; % in mH
L23_mH = [0.0942 * 2.8^2, ...
          0.0576 * 2.8^2, ...
          0.0476 * 2.8^2, ...
          0.0461 * 2.8^2, ...
          0.0436 * 2.8^2, ...
          0.0427 * 2.8^2]

R12 = [0.8699, 0.8720, 0.8715, 0.8603, 0.8943, 0.9047];
R13 = [2.5475, 2.5595, 2.6175, 2.6134, 2.6631, 2.6773];
R23 = [0.3332 * 2.8^2, ...
          0.3381 * 2.8^2, ...
          0.3430 * 2.8^2, ...
          0.3407 * 2.8^2, ...
          0.3456 * 2.8^2, ...
          0.3490 * 2.8^2];

% === Initialize ===
Z12 = zeros(size(Frequency));
Z13 = zeros(size(Frequency));
Z23 = zeros(size(Frequency));

Z1 = zeros(size(Frequency));
Z2 = zeros(size(Frequency));
Z3 = zeros(size(Frequency));

R1 = zeros(size(Frequency));
R2 = zeros(size(Frequency));
R3 = zeros(size(Frequency));

L1 = zeros(size(Frequency));
L2 = zeros(size(Frequency));
L3 = zeros(size(Frequency));

MagZ1 = zeros(size(Frequency));
MagZ2 = zeros(size(Frequency));
MagZ3 = zeros(size(Frequency));

% === Calculations ===
for i = 1:length(Frequency)
    f = Frequency(i);
    omega = 2 * pi * f;

    % Convert L from mH to H
    L12_H = L12_mH(i) / 1000;
    L13_H = L13_mH(i) / 1000;
    L23_H = L23_mH(i) / 1000;

    % Calculate pairwise Z
    Z12(i) = R12(i) + 1j * omega * L12_H;
    Z13(i) = R13(i) + 1j * omega * L13_H;
    Z23(i) = R23(i) + 1j * omega * L23_H;

    % Calculate Z1, Z2, Z3
    Z1(i) = 0.5 * (Z12(i) - Z23(i) + Z13(i));
    Z2(i) = 0.5 * (Z12(i) + Z23(i) - Z13(i));
    Z3(i) = 0.5 * (-Z12(i) + Z23(i) + Z13(i));

    % Extract R and L in mH
    R1(i) = real(Z1(i));
    R2(i) = real(Z2(i));
    R3(i) = real(Z3(i));
```

```
    L1(i) = 1000 * imag(Z1(i)) / omega;
    L2(i) = 1000 * imag(Z2(i)) / omega;
    L3(i) = 1000 * imag(Z3(i)) / omega;

    % Magnitudes
    MagZ1(i) = abs(Z1(i));
    MagZ2(i) = abs(Z2(i));
    MagZ3(i) = abs(Z3(i));
end

% === Output Table ===
ZRL_table = table(Frequency.', ...
                  Z1.', R1.', L1.', MagZ1.', ...
                  Z2.', R2.', L2.', MagZ2.', ...
                  Z3.', R3.', L3.', MagZ3.', ...
    'VariableNames', {'Frequency_Hz', ...
                      'Z1_Complex', 'R1_Ohm', 'L1_mH', 'MagZ1_Ohm', ...
                      'Z2_Complex', 'R2_Ohm', 'L2_mH', 'MagZ2_Ohm', ...
                      'Z3_Complex', 'R3_Ohm', 'L3_mH', 'MagZ3_Ohm'});

disp(ZRL_table);

% === Plot R and L ===
figure;

% subplot(2,1,1);
% plot(Frequency, R1, '-o', 'LineWidth', 2); hold on;
% plot(Frequency, R2, '-s', 'LineWidth', 2);
% plot(Frequency, R3, '-d', 'LineWidth', 2);
% grid on;
% xlabel('Frequency (Hz)');
% ylabel('Resistance (Ohm)');
% title('R1, R2, R3 vs Frequency');
% legend('R1', 'R2', 'R3');

% subplot(2,1,2);
plot(Frequency, L1, '-o', 'LineWidth', 6); hold on;
plot(Frequency, L2, '-s', 'LineWidth', 6);
plot(Frequency, L3, '-d', 'LineWidth', 6);
grid on;

xlabel('Frequency (Hz)', 'FontSize', 20);
ylabel('Inductance (mH)', 'FontSize', 20);
title('L1, L2, L3 vs Frequency', 'FontSize', 20);
legend('L1', 'L2', 'L3', 'FontSize', 20);

set(gca, 'FontSize', 20);  % Axis ticks and labels

fprintf('\n=== Copy-Paste Friendly Table for Google Sheets ===\n');
fprintf(['Freq(Hz)\t', ...
         'Z1(Ohm)\tR1(Ohm)\tL1(mH)\t|Z1|(Ohm)\t', ...
         'Z2(Ohm)\tR2(Ohm)\tL2(mH)\t|Z2|(Ohm)\t', ...
         'Z3(Ohm)\tR3(Ohm)\tL3(mH)\t|Z3|(Ohm)\n']);

for i = 1:length(Frequency)
    fprintf('%d\t%.4f + %.4fi\t%.4f\t%.4f\t%.4f\t%.4f + %.4fi\t%.4f\t%.4f\t%.4f\t%.4f + %.4fi\t%.4f\t%.4f\t%.4f\n', ...
        Frequency(i), ...
        real(Z1(i)), imag(Z1(i)), R1(i), L1(i), MagZ1(i), ...
        real(Z2(i)), imag(Z2(i)), R2(i), L2(i), MagZ2(i), ...
        real(Z3(i)), imag(Z3(i)), R3(i), L3(i), MagZ3(i));
end
```

C.4 B-H curve

The code below is used for plotting the B-H curve for the open circuit tests done for secondary 1 for 400 Hz

```
    % Parameters (you should update these with your actual values)
Ac = 64e-4;         % Core cross-sectional area in m^2
Np = 33;           % Number of primary turns
l = 0.52;            % Mean magnetic path length in meters

% Load CSV data
data = readmatrix('T0058.csv');
time = data(:,1);
voltage_raw = data(:,2);
current_raw = data(:,3);

% === Remove DC Offset ===
voltage = voltage_raw ;
current = current_raw ;

% === Calculate dt (time steps) ===
dt = diff(time);

% === Compute Flux: Phi = V dt / Np ===
Phi = cumsum([0; voltage(1:end-1) .* dt]) / Np;

% === Magnetic flux density B (T) ===
B = Phi / Ac;

% === Magnetic field strength H (A/m) ===
H = (Np .* current) / l;

% === Plot B-H Loop ===
% === Plot B-H Loop ===
figure;
plot(H, B, 'b', 'LineWidth', 1.5);
xlabel('Magnetic Field Strength H (A/m)');
ylabel('Magnetic Flux Density B (T)');
title('B-H Loop');
grid on;

ylim([-2 2]);  % Fix B scale between -2 and 2

% === Hysteresis Loss Calculation ===
area = trapz(H, B);  % Integral of B w.r.t. H
areaText = ['Area: ', num2str(abs(area), '%.4f'), ' J/m^3'];

% Display area on plot
text(mean(H), max(B) * 0.9, areaText, ...
     'HorizontalAlignment', 'center', ...
     'VerticalAlignment', 'bottom', ...
     'FontSize', 12, ...
     'BackgroundColor', 'white');

% Display in command window
disp(['Area inside the B-H curve (Hysteresis Loss): ', ...
      num2str(abs(area), '%.4f'), ' J/m^3']);
```

Appendix D Setup Images

The images D.1, D.2, and D.3 show the images of the MOSFET, bulk capacitor, and soldered PCB of the inverter respectively.

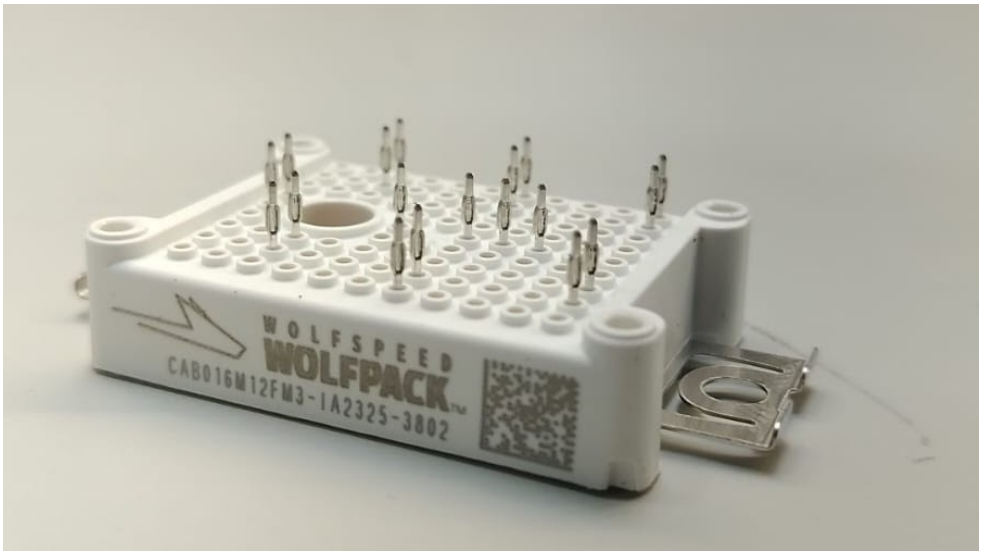


Figure D.1: Inverter MOSFET CBB032M12FM3

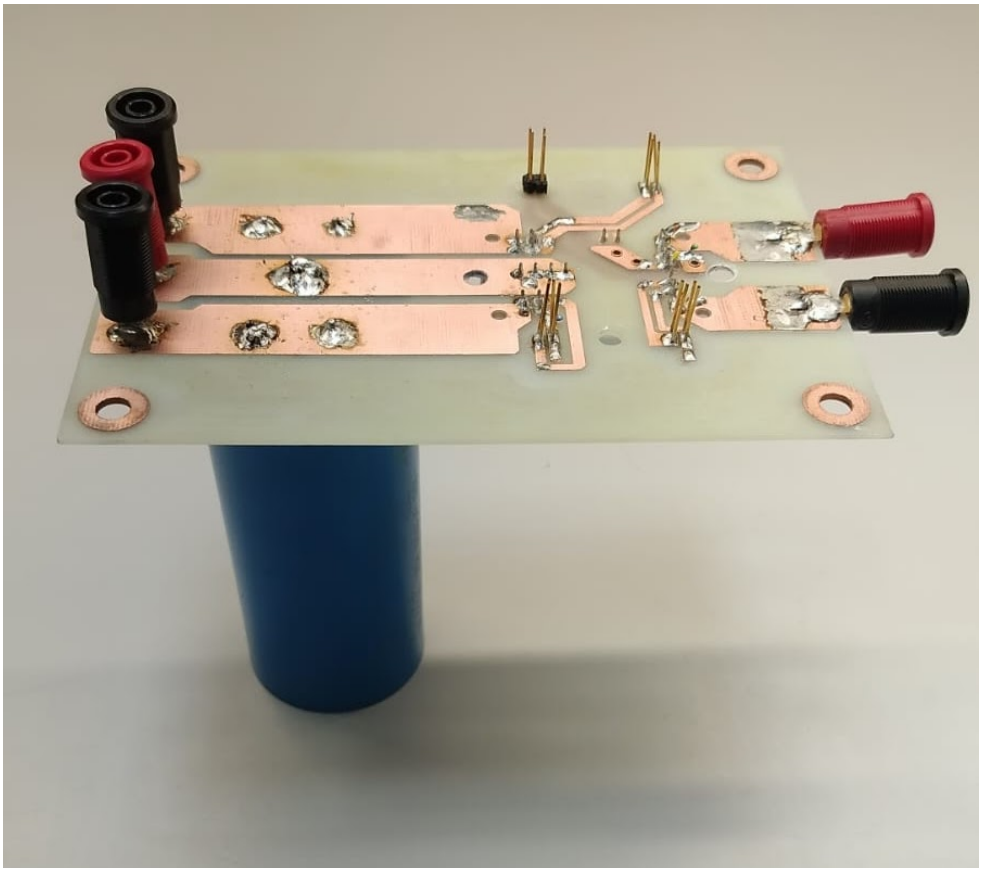


Figure D.2: Bulk capacitor and MOSFET soldered

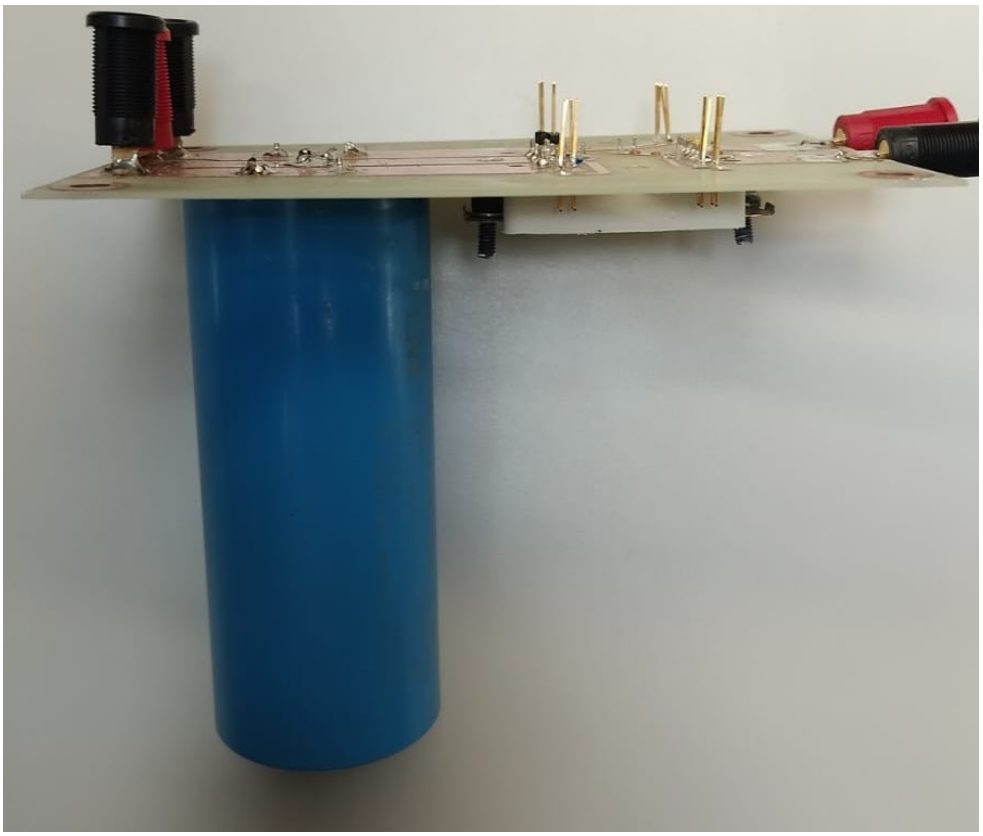


Figure D.3: MOSFET, bulk capacitor, and Inverter PCB soldered

Appendix E Test results

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The chapter presents the results of different tests conducted on the transformer.

E.1 Open circuit test- Primary side

Freq (Hz)	Im (A)	Ire (A)	P (W)	PF	Xm (Ω)	Lm (H)	Rm (Ω)
300	0.0618	0.1522	76.7513	0.9266	8159.4858	4.3287	3312.3142
400	0.0568	0.1395	68.9054	0.9262	8700.7894	3.4619	3540.5347
500	0.0542	0.1347	67.1314	0.9278	9203.1522	2.9295	3701.0077
600	0.0525	0.1313	65.8361	0.9286	9559.1320	2.5356	3819.6123
700	0.0520	0.1259	62.6620	0.9242	9560.6723	2.1738	3950.6398

Table E.1: Open circuit test – Primary side sine wave input

Freq (Hz)	Im (A)	Ire (A)	P (W)	PF	Xm (Ω)	Lm (H)	Rm (Ω)
300	0.0702	0.1679	95.1312	0.9226	8076.2296	4.2846	3376.2171
400	0.0601	0.1496	80.9309	0.9279	8996.7284	3.5797	3614.3972
500	0.0547	0.1374	70.6484	0.9290	9400.5876	2.9923	3743.5791
600	0.0517	0.1279	62.1814	0.9271	9409.0669	2.4958	3802.8076
700	0.0494	0.1156	51.7207	0.9195	9044.3987	2.0564	3867.3297

Table E.2: Open circuit test – Primary side square wave input