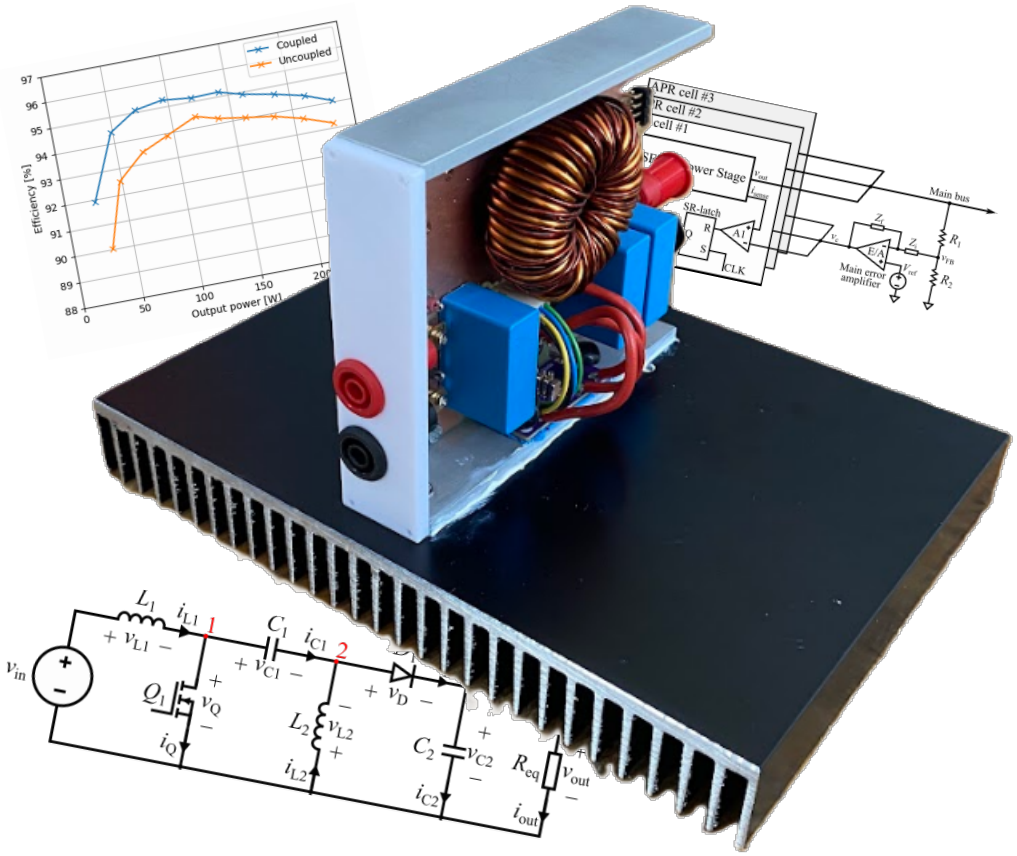
Versatile Array Power Regulator for Electric Propulsion Spacecraft

Feasibility of the Single-Ended Primary-Inductor Converter as a High-Power Solar Array Regulator in Spacecrafts



Master's Thesis

PED4-1046

Aalborg University, Department of AAU Energy

MSc. in Power Electronics and Drives

AALBORG UNIVERSITY
STUDENT REPORT

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Abstract:

With the advent of Electric Propulsion (EP) the power demand of the Electrical Power System (EPS) in spacecrafts is increasing. A higher Photovoltaic (PV) string voltage results in higher risk of Electrostatic Discharge (ESD) due to spacecraft charging. Thus this project revolves around evaluating the feasibility of a step-up-and-down topology to maintain the PV string voltage at an acceptable level. The Single-Ended Primary-Inductor Converter (SEPIC) was selected as the most suitable topology, because it has a continuous input current and a non-inverted output. To assess the feasibility of the SEPIC, a power loss estimation algorithm was developed alongside a laboratory prototype. To minimise the power losses, the prototype was developed with a Schottky diode and a Galium Nitride (GaN) High-Electron-Mobility Transistor (HEMT). The power loss estimation algorithm and results of experimental testing were used to demonstrate that the SEPIC exhibits a better efficiency when the inductors are coupled on the same core. During the laboratory testing peak efficiencies of 92.2% and 96.8% were measured for at a switching frequency of 500 kHz and 250 kHz, respectively. Finally the small-signal dynamics of the SEPIC were studied, revealing that the SEPIC consist of Right-Hand Plane (RHP) zeros. By implementing peak current-mode control and compensating the control loop with a type-II compensator, it was found that it is possible to attain a sufficient bandwidth with the SEPIC. Through LTspice simulations it was proven that this control strategy is capable of fulfilling the ECSS standards regarding static- and transient regulation.

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Resumé

I forbindelse med udbredelsen af elektrisk fremdrift til rumfartøjer, udsættes den elektriske forsyning for et stigende effektbehov. Missioner med øget effektevne er påkrævet at have en højere spænding på hovedbussen. Buck-konvertere er hyppigt anvendt til at regulere solpanelerne, hvorfor solcellestrengene da må have en større spænding end selve hovedbussen. Men med stigende spændinger på solpanelerne, som er udsat for rummets miljø, er der en øget risiko for elektrostatisk udladning som kan resultere i beskadiget solceller. Denne problematik danner rammen for analysen i dette projekt, hvor der undersøges hvorvidt en buck-boost lignende konverter kan erstatte buck-konvertere til regulering af solpanelerne, og derved sikre at spændingen på solcellestrengene forbliver tilstrækkelig lav.

Som følge af en komparativ analyse mellem buck-boost konvertertopologier blev SEPIC-topologien valgt som den bedst egnede. SEPIC-topologien består af 2 kondensatorer, 2 spoler, samt 2 halvledere. Begrundelsen for dette valg er at den bisidder en kontinuert indgangsstrøm, samt en positiv udgangspolaritet. SEPIC-topologien blev derefter dimensioneret til at opfylde de operationelle krav, som blandt andet består af en maksimal rippelspænding på $\pm 5\,\mathrm{mV}$. For at opnå dette blev en skiftefrekvens på $500\,\mathrm{kHz}$ valgt. Desuden blev det bevist at halvlederne i SEPIC-topologien bliver udsat for en betydelig mængde belastning, i kraft af at de hver især skal blokere summen af indgang- og udgangsspændingen, men også summen af strømmen gennem begge spoler. Derudover blev det påvist at de 2 spoler i SEPIC-topologien kan implementeres på en fælles kerne grundet deres lignende volt-sekund balance.

En del af evalueringen bestod af at analysere effekttabene i SEPIC-topologien, og dermed også udlede en estimering af nyttevirkningen. For at realisere dette blev effekttabene i hver af de 6 komponenter gennemgået, og i den forlængelse blev en estimeringsalgoritme udarbejdet i Python. Algoritmen tog udgangspunkt i en konstruktion der bestod af en GaN halvleder og en Schottky diode. Estimeringsalgoritmen efterviste at dioden resulterede i størstedelen af tabene og at GaN transistoren også havde betydelige tab. Især for transistoren var størstedelen forårsaget af skiftetab samt tab fra den parasitiske output-kapacitet, C_{oss}. På bagrund af algoritmen, som var baseret på de basale tabsligninger, blev det eftervist at nyttevirkningen var højest når spolerne var koplet på den samme kerne. Derudover blev det vurderet at det er muligt at implementere synkroniseret transistorere i SEPIC-topologien, med henblik på at øge nyttevirkningen yderligere. Dog blev dette ikke videre eftervist grundet den øget kompleksitet, som ville været vanskeligt at implementere indenfor projekts tidsramme.

SEPIC-topologiens reguleringsegenskaber blev også analyseret. Her blev en AC model udledt for at analysere dynamikken. I den sammenhæng blev det eftervist at SEPIC-topologien består af nulpunkter i det højre halvplan, samt er overføringsfunktionerne i fjerde orden. Dette fører bevis for at SEPIC-topologien besidder forholdsvis vanskelig reguleringsdynamik. Det blev udledt at peak-strømregulering kunne implementeres ved at kompensere kontrolsløjfen med en type-II regulator. I den sammenhæng blev en båndbredde i området mellem 6 til $9\,\mathrm{kHz}$ opnået, med

en fasemargen på $> 60°$ og en forstærkningsmargen på $> 6\,\text{dB}$. Dette er i overenstemmelse med specifikationerne fra ECSS-retningslinjerne. Hertil blev reguleringsdynamikken evalueret igennem LTspice simuleringer, som efterviste at retningslinjerne i henhold til transient- og statisk regulering også kunne overholdes. Dermed blev det verificeret at SEPIC-topologien kan reguleres i overenstemmelse med ECSS-retningslinjerne.

Sidste led i analysen bestod af det praktisk arbejde. Her blev en mekanisk ramme designet og udarbejdet i overenstemmelse med de tilladte mål. Rammens dimensioner indikerede, at arealet til at afsætte tabsvarmen var begrænset. Indenfor den mekaniske ramme blev der designet og opbygget en SEPIC prototype. Prototype er opbygget af 2 printplader, hvor den ene bestod af halvlederne og det andet bestod af de mere pladskrævende passive komponenter. Printpladen bestående af halvlederne var designet til at monteres direckte på væggen af den mekaniskeramme for at maksimere varmeoverførsel. Der blev opbygget 2 forskellige prototyper med både afkoblede og koblede spoler for at tillade en sammenligning herimellem. Prototypen viste signalformer i overenstemmelse med teorien, blandt andet at spolen L_1 gennemsnitligt leder indgangsstrømmen og at L_2 ligeledes leder udgangstrømmen. Igennem laboratorieforsøg viste det sig at SEPIC protoypen opnåede en maksimal nyttevirkning på 92.2% og 96.8% for skiftefrekvenser på henholdsvis 500 kHz og 250 kHz. Dog viste det sig at det termiske design med hensyn til GaN halvlederen ikke var tilstrækkelig som medførte overophedning af komponenten. Årsagen til dette er transistorhuset, som var beregnet til at blive nedkølet igennem den øverste overflade. I den forlængelse vurderes det at den valgte GaN halvleder ikke fremstår tilstrækkelig, og det lader til at prototypen havde været mere optimal med en halvleder som nedkøles igennem bunden.

På baggrund af analysen i dette projekt vurderes SEPIC-topologien at være egnet til regulering af solpanelerne i rumfartøjer med et øget effektbehov. Dette konkluderes ud fra den efterviste nyttevirkning, samt evnen til at overholde retninglinjerne for transient- og statisk regulering. Derudover vurderes det at en bundkølet GaN-transistor er nødvendig for at opnå et tilstrækkelig termisk design, taget modulstørrelsen og det begrænset varmeledningsareal i betragtning.

Preface

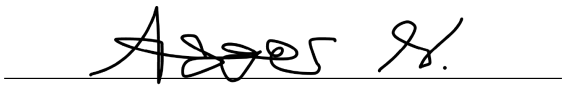
This master's thesis report is written by group PED4-1046 on the 4^{th} semester MSc. of the Power Electronics and Drives specialisation, at Aalborg University. This project was conducted in collaboration with Terma A/S, specifically the space systems department. Supervision was carried out by Assistant Professor Asger B. Jørgensen, Postdoctoral Researcher Faheem Ahmad, and Senior Engineer Hans Jensen. The project period lasted from February 3^{rd} to May 28^{th}. The project work was conducted at Aalborg University.

This project report is comprised of 9 chapters and 6 appendixes, in which figures, tables, and equations are numbered by chapter or appendix accordingly; i.e. having the following format respectively: figure 1.1, table 2.2, and equation (3.3).

The following software have been used during the project work:

- Code Composer Studio for embedded software implementation.
- FreeCAD 0.21 for 3D model design.
- FLIR thermal Studio for post-processing of thermal measurements.
- Inkscape for figure composing.
- JupyterLab and Spyder for data processing and computation.
- KiCad for printed circuit board design.
- LTspice for simulations.
- Maple 2023.2 for mathematical derivation.
- Overleaf for LaTeXdocument processing.

A ZIP folder containing miscellaneous files is uploaded to Digital Eksamen together with this report. In this folder the following can be access: CAD- and PCB files, Simulation files, Python scripts, embedded software code, and the test data.



Asger Brorsen Hebsgaard

I would like to express my sincere gratitude to everyone who helped me throughout this project. Special thanks go to Hans Jensen, Asger B. Jørgensen, Faheem Ahmad, Szymon M. Beczkowski, Narendra Walawalkar, and my colleagues at Terma.

I also extend my appreciation to Efficient Power Conversion for generously providing me with free component samples.

Abbreviations

APR Array Power Regulator

BCDR Battery Charge- and Discharge Regulator

CCM Continuous Conduction Mode

ECSS European Corporation for Space Standardization

EP Electric Propulsion

EPS Electrical Power System

ESD Electrostatic Discharge

GaN Galium Nitride

HEMT High-Electron-Mobility Transistor

KCL Kirchhoff's Current Law

KVL Kirchhoff's Voltage Law

LCLs Latching Current Limiters

MEA Main Error Amplifier

MPPT Maximum Power Point Tracking

PCB Printed Circuit Board

RHP Right-Hand Plane

PV Photovoltaic

PWM Pulse Width Modulation

RMS Root Mean Square

SEPIC Single-Ended Primary-Inductor Converter

SMD Surface Mounted Device

SMPS Switch-Mode Power Supply

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Nomenclature

Symbol	Explanation	Unit
ΔI_{DD}	Transistor drain current ripple	[A]
ΔI_{in}	Input current ripple	[A]
ΔV_{in}	Input voltage ripple	[V]
ζ	Damping coefficient	[−]
η	Efficiency	[%]
λ	Magnetic flux linkage	[Wb]
λ_{sys}	State-space eigenvalues (poles)	[−]
μ	Permeability	$[\frac{\mathrm{H}}{\mathrm{m}}]$
Φ_{l1}	Leakage flux	[Wb]
Φ_m	Magnetic core flux	[Wb]
$\mathbf{A}$	System matrix	[−]
$\mathbf{A}_1$	System matrix (ON state)	[−]
$\mathbf{A}_2$	System matrix (OFF state)	[−]
A_{c}	Cross-sectional area	[m^2]
$\mathbf{B}$	Input matrix	[−]
$\mathbf{B}_1$	Input matrix (ON state)	[−]
$\mathbf{B}_2$	Input matrix (OFF state)	[−]
B	Magnetic flux density	[T]
C	Arbitrary Capacitance	[F]
$\mathbf{C}$	Output matrix	[−]
$\mathbf{C}_1$	Output matrix (ON state)	[−]
$\mathbf{C}_2$	Output matrix (OFF state)	[−]
C_1	C_1 capacitance	[F]
C_2	C_2 capacitance	[F]
C_{ds}	Drain-to-source capacitance	[F]
C_{gd}	Gate-to-drain capacitance	[F]
C_{gs}	Gate-to-source capacitance	[F]
C_{hs}	High-side clamping capacitor	[F]
C_{in}	Input filter capacitance	[F]
C_{j}	Junction capacitance	[F]
C_{cout}	Output capacitance	[F]
C_{p}	Parasitic parallel capacitance	[F]
CLK	Clock signal	[V]
D	Duty-cycle	[−]
D_1	Diode	[−]
D_{wire}	Wire diameter	[m]
$\mathbf{E}$	Input-to-output matrix	[−]
E_{hyst}	Core hysteresis energy loss	[J]
E_{on}	Turn on energy loss	[J]

E_{oss}	Output capacitance energy	[J]
E_{off}	Turn off energy loss	[J]
f_{p}	Frequency of compensator pole	[Hz]
f_{sw}	Switching frequency	[Hz]
f_{z}	Frequency of compensator zero	[Hz]
$G(s)$	Arbitrary transfer function	[−]
$G_{\text{i}}(s)$	Transfer function of inner current loop	[−]
$G_{\text{id1}}(s)$	Input-to-output transfer function of the L_1 inductor current	[−]
$G_{\text{id2}}(s)$	Input-to-output transfer function of the L_2 inductor current	[−]
$G_{\text{id}}(s)$	Input-to-output transfer function of the transistor on current	[−]
$G_{\text{vi}}(s)$	Transistor-current-to-output voltage transfer function	[−]
$G_{\text{ol}}(s)$	Open-loop transfer function	[−]
H	Magnetisation force (H-field)	[Oe]
H_{max}	Maximum H-field	[Oe]
I_{b}	Maximum burden current	[A]
I_{C}	Capacitor RMS current	[A]
i_{C}	Arbitrary capacitor current	[A]
i_{C1}	Current in C_1 capacitor	[A]
i_{C2}	Current in C_1 capacitor	[A]
i_{D}	Diode current	[A]
i_{DD}	Transistor drain current	[A]
I_{f}	Diode forward current	[A]
i_{in}	Input current	[A]
I_{L}	Inductor RMS current	[A]
i_{L1}	Current in L_1 inductor	[A]
i_{L2}	Current in L_2 inductor	[A]
i_{out}	Output current	[A]
I_{ON}	mean on-state transistor current	[A]
i_{Q}	Transistor current	[A]
I_{sc}	Short-circuit current	[A]
i_{sense}	Current sensor output	[V]
i_{sw}	Transistor current	[A]
J	Ampacity	$[\frac{\text{A}}{\text{m}^2}]$
$\mathbf{K}$	Coupling matrix	[−]
k	Coupling factor	[−]
K	Controller gain	$[\frac{\text{V}}{\text{V}}]$
K_{CS}	Current sensor gain	$[\frac{\text{V}}{\text{A}}]$
K_{cont}	UC1845 internal gain	$[\frac{\text{V}}{\text{V}}]$
L	Arbitrary inductance	[H]
L_1	L_1 self-inductance	[H]

L_2	L_2 self-inductance	[H]
l_e	Effective path length	[m]
L_eff	Effective inductance	[H]
L_oc	Open-circuit test inductance	[H]
L_s	Series inductance	[H]
L_sc	Short-circuit test inductance	[H]
M	Mutual inductance	[H]
n	Arbitrary amount	[−]
n_1	No. of turns in winding 1	[−]
n_2	No. of turns in winding 2	[−]
N_CT	Current sense transformer turns-ratio	[−]
P	Power throughput	[W]
$P_\mathrm{D,\ cond}$	Diode conduction loss	[W]
$P_\mathrm{C,\ ESR}$	Capacitor ESR loss	[W]
P_j	Power loss due to junction capacitance	[W]
$P_\mathrm{L,\ cond}$	Inductor conduction loss	[W]
P_now	Nominal power throughput	[W]
P_oss	Power loss from output capacitance	[W]
P_rr	Reverse recovery loss	[W]
$P_\mathrm{Q,\ cond}$	Transistor conduction loss	[W]
P_rr	Reverse recovery loss	[W]
P_sense	Sensor power loss	[W]
P_sw	Switching power loss	[W]
Q_1	Master transistor	[−]
Q_g	Total gate charge	[C]
Q_rr	Reverse recovery charge	[C]
R_1	Upper resistor in voltage divider	[Ω]
R_2	Lower resistor in voltage divider	[Ω]
R_b	Burden resistor	[Ω]
$R_\mathrm{ds(on)}$	Drain-to-source resistance	[Ω]
R_eq	Equivalent load resistance	[Ω]
R_hs	High-side driving resistor	[Ω]
R_j	Junction resistance	[Ω]
R_p	Parallel resistance	[Ω]
R_r	Reverse-biased resistance	[Ω]
R_s	Series resistance	[Ω]
t	Time	[s]
T	Switching period	[s]
T_core	Core temperature	[°]
t_f	Fall time	[s]
T_J	Junction temperature	[°]
t_r	Rise time	[s]
$\mathbf{u}$	Input vector	[V]
V_bus	Main bus voltage	[V]

v_{C1}	Voltage on C_1 capacitor	[V]
v_{C2}	Voltage on C_2 capacitor	[V]
v_c	Control voltage (error amplifier)	[V]
v_D	Voltage on diode	[V]
V_{DS}	Drain-to-source voltage	[V]
V_{err}	Voltage error	[V]
V_f	Forward-bias voltage	[V]
v_{FB}	Feedback sensor voltage	[V]
V_{GS}	Gate-to-source voltage	[V]
V_{in}	Input voltage	[V]
V_{ka}	Cathode-to-anode voltage	[V]
v_L	Arbitrary inductor voltage	[V]
v_{L1}	Voltage on L_1 inductor	[V]
v_{L2}	Voltage on L_2 inductor	[V]
V_{oc}	Open-circuit voltage	[V]
V_{out}	Output voltage	[V]
V_R	Reverse-bias voltage	[V]
V_{ref}	Reference voltage	[V]
V_{PV}	Solar string voltage	[V]
v_Q	Voltage on transistor	[V]
$\mathbf{x}$	State vector	[V], [A]
$\mathbf{y}$	Output vector	[V], [A]
Z_f	Feedback impedance	[Ω]
Z_i	Input impedance	[Ω]

Contents

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1 Introduction

The advent of spacecraft technology in the 60's sparked the beginning of human kinds journey of exploration in outer space. Outer space is a wildly uninhabitable environment for humans, and sending vehicles into space is exceptionally costly. However, the exploitation of outer space have yielded knowledge of the universe, technological advancements, educational benefits, offered commercial opportunities and much more, thereby highlighting the prosperity associated with the development of spacecrafts [1].

Traditionally, chemical propulsion has been used to thrust and navigate spacecrafts. However, this requires a large reserve of chemical matter to be carried along with the spacecraft, thus resulting in a spacecrafts with increased mass. Recently Electric Propulsion (EP) has become a popular alternative, where thrust is generated from electrical power. This solves the mass drawback of chemical propulsion while also providing much higher levels of specific impulse, thus allowing smaller and more efficient spacecrafts. On the other hand EP is limited in thrust while also being costly, and it requires a relatively large amount of electrical power. Nonetheless, EP is a significant technological advancement which has enabled many notable space missions in recent years. But it does put a larger demand on the EPS which is required to evolve conjointly, and thus causes a bottleneck in terms of further EP advancements [2]. The Electrical Power System (EPS) of a spacecraft is covered in the following section 1.1.

1.1 Spacecraft Electrical Power System

In the emptiness of space, power sources are scarce. In general two power sources are utilised for for spacecraft: radio-isotope generators and Photovoltaic (PV) arrays. Radio-isotope generators are beneficial at great distances from the sun, but are rare, historically, in the context of European space missions [3]. Therefore a PV source is considered more relevant in the scope of this project. A spacecraft EPS based on PV power, with n loads, is illustrated in figure 1.1.

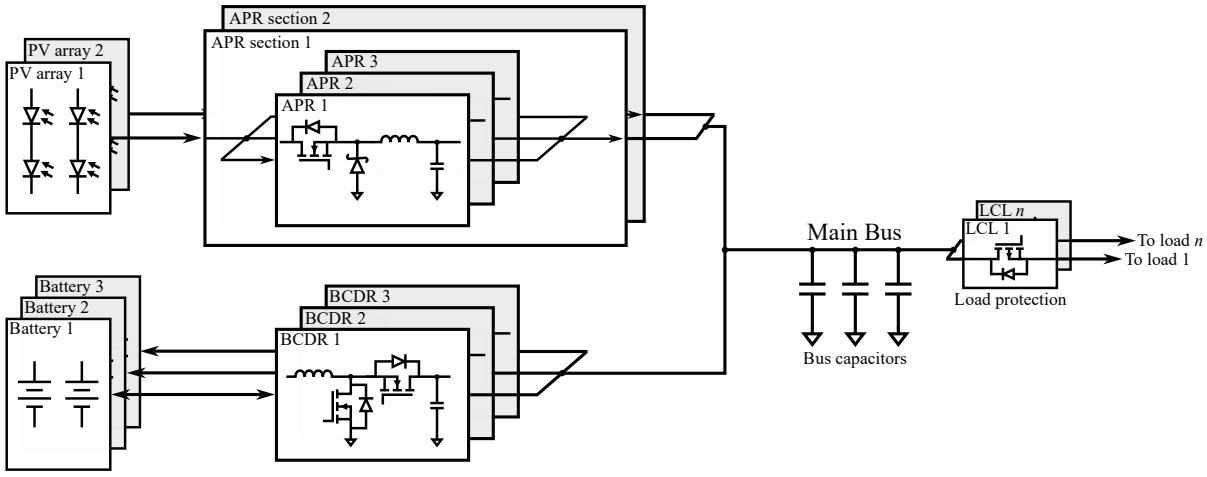


Figure 1.1 Top-level schematic representation of a regulated space EPS [4].

As presented in figure 1.1, the PV cells are arranged in a solar array to provide the correct string voltage and array power. Two solar arrays are present at opposing sides of the spacecraft, often times referred to as the solar wings. The solar arrays are interfaced to the EPS main bus through the Array Power Regulator (APR), which is typically a step-down converter topology. To ensure power during eclipse and the launch event, a battery pack is also included in the EPS. The battery pack is interfaced to the main bus through a Battery Charge- and Discharge Regulator (BCDR), which has to allow bidirectional power flow, for charging and discharging scenarios. The main bus is stabilised through distributed capacitors, to provide the proper bus impedance. Lastly all the system loads are connected to the EPS through n number of Latching Current Limiters (LCLs). The LCLs consists of a p-channel transistor operated in the linear region which latches the current in case of an over-current scenario, and for a prolonged over-current it can trip off a load entirely. Note that the EPS is configured with many subsystems in parallel for redundancy, thereby ensuring a reliable single-point-failure-free system which is necessary for long-lasting space missions where maintenance is impossible [5].

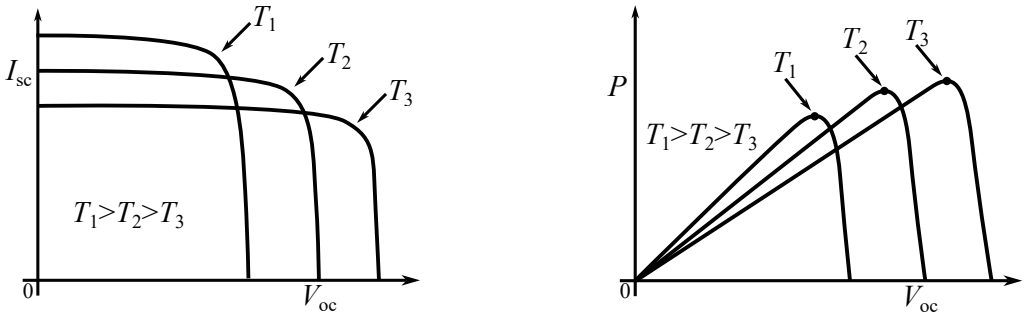
The EPS topology presented in figure 1.1 is a regulated topology, in which the APR and BCDR regulate the main bus to a fixed voltage. The European Corporation for Space Standardization (ECSS) specifies the following bus voltages for a regulated bus: 28 V, 50 V, and 100 V for power levels of $\leq$1.5 kW, $\leq$8 kW, and >8 kW, respectively [6]. The voltage is regulated in what is commonly referred to as 3-domain control, which allows the APR to operate in Maximum Power Point Tracking (MPPT) mode. Thereby the BCDR is either charging- or discharging the battery to ensure the system bus voltage set point. Unregulated busses are also common, and the main difference is simply that they do not have a BCDR subsystem, meaning the main bus voltage fluctuates with the battery voltage [5].

To facilitate the power demands from EP, it is advantageous to increase the voltage levels of the EPS to ensure that current levels do not become excessively high. Here the environment of outer space introduces some constraints which are outlined in the following section 1.2.

1.2 Constraints of the Space Environment

In the vacuum of space there is no air present, therefore it is not possible to dissipate heat by convection. Therefore it is essential to keep power losses as low as possible, since heat can only be dissipated by conduction or radiation. Moreover, objects in space experience large temperature variation. The PV arrays can reach levels higher than 80 °C during irradiation, and as low as -170 °C at the point of an eclipse exit event [5]. The general temperature characteristic of PV cells are illustrated in figure 1.2.

From figure 1.2a it is clear how lower temperatures, T, result in a higher open-circuit voltage, V_{oc}. Similarly from figure 1.2b it is seen how the maximum power point is shifted toward a higher voltage for lower temperatures, and vice versa. This temperature dependence results in a large PV array voltage range, resulting from the large surface temperature swings. As outlined in section 1.1, the APR is typically a step-down topology, implying that the PV string voltage must be greater than the bus voltage. Thus in view of the large temperature swings, the PV



(a) PV cell $I(V)$ characteristic. **(b)** PV cell power characteristic.

Figure 1.2 PV cell characteristics at different operating temperatures [5] [7].

voltage can reach very high voltage levels. This can be problematic in space, as outlined in section 1.2.1.

1.2.1 Electrostatic Discharge and Arcing of Solar Arrays in Space

The outer space medium consists of plasma, which is essentially charged particles. These charged particles will accumulate at the surface of dielectric materials, charging the given surface to a potential. This phenomenon is referred to as spacecraft charging. When electrons accumulate on a dielectric it charges the surface to a negative voltage in reference to the spacecraft ground, possibly reaching levels as low as -kV [9]. On PV arrays the cover glass is often of concern, where this dielectric surface can result in a ESD event. The ESD can then trigger a sustained arc which can potentially damage the solar arrays. An example of a damaged PV array from sustained arcing is presented in figure 1.3. It is required by the ECSS standard that the PV arrays are designed to keep surface charging within acceptable limits, however risk of ESD confines the operating voltage of the PV arrays. For PV arrays that are not designed to mitigate surface charging, ESD events have been observed at voltages as low as 75 V [8]. The large voltage range of the PV arrays in space posses a challenge in view of spacecraft charging. This is further outlined in section 1.3.

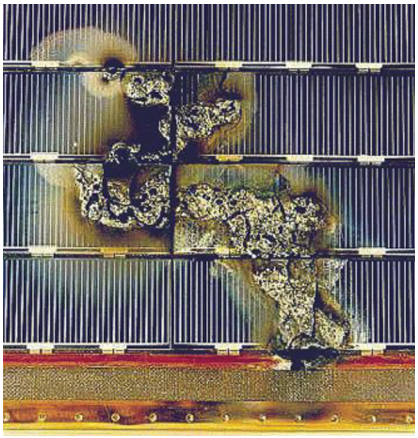


Figure 1.3 Arc damage on the ESA EURECA mission [8].

1.3 Problem Statement

The large voltage range of the PV arrays make it difficult to achieve the main bus voltage levels necessary to power EP based spacecraft. This is because of the step-down converter topology, which implies that the PV array voltage must be higher than the main bus voltage at all times. For example, to enable the 100 V main bus voltage necessary for high-power EP with a a step-down topology, requires the PV array voltage to not go below 100 V during the mission span. This lower 100 V PV array reference occurs when the PV array is warmest, however when a spacecraft experiences an eclipse exit event, the PV arrays can reach as low as $-170\,^{\circ}\mathrm{C}$ which would result in a cold PV string voltage of almost 300 V in the case of quadruple junction PV cells [10]. This high voltage increases the risk of ESD on the PV arrays, which can trigger arcing. Thus it is apparent that a step-down converter topology requires the PV string voltage to reach hazardous levels. To solve this issue, an APR converter topology that allows both step-up and step-down capabilities, can limit the PV array voltage to acceptable levels while still maintaining the EPS main bus voltage at the specified set point, e.g. 28 V, 50 V, or 100 V. Hence the scope of this project is to analyse and test if a universal step-up-and-down type converter can substitute the traditional step-down APR topology, in view of the conditions experienced during a space mission, and a PV power source. The project scope is defined in view of the 4 month project period.

Problem Formulation:

To what extend is a step-up-and-down converter topology suitable to replace the traditional step-down APR converter in a space EPS for 1 kW power transfer, and why? Furthermore, to what extent can a step-up-and-down topology achieve high efficiency in view of the wide input voltage range of a space PV array, ensuring a low enough voltage to mitigate the risk of ESD?

Project Objectives:

- Analyse and select a suitable step-up-and-down converter topology in view of a spacecraft EPS with a regulated 50 V main bus supplied from an input PV array.
- Model an APR converter cell analytically, aiming for 97% efficiency, and validate the performance through simulation software.
- Develop a prototype of the step-up-and-down converter cell, based on space equivalent components.
- Validate the converter operation and performance experimentally.
- Evaluate the feasibility of a comprehensive step-up-and-down converter module, in the context of a spacecraft EPS and the ECSS standards.

2 System Modelling

This chapter covers the modelling and theory regarding a suitable step-up-and-down converter. As a foundation of the system model, Terma A/S has specified an exemplary EPS system scheme consisting of the parameters presented in table 2.1.

Table 2.1 Specified APR module requirements [11].

Parameter	Value
Nom. APR module power	1000 W
PV string voltage	$35\,\mathrm{V} \leq V_{\mathrm{PV}} \leq 100\,\mathrm{V}$
Main bus voltage	50 V regulated
Module efficiency	$\geq 97\%$
PV voltage ripple	$\leq 5\,\mathrm{mV}$
Input filter capacitance	$\leq 20\,\mu\mathrm{F}$
Max. module volume	$(282 \times 150 \times 24)\,\mathrm{mm}$

The APR requirements of table 2.1 are elaborated based on EPS parameters that emulate those of real spacecraft. The given power level requirement is for the comprehensive module. For the EPS of an unmanned spacecraft, the failure tolerance requirement is that the system must be single-point-failure free which implies a redundancy level of $n + 1$ [3]. Therefore it is selected that the APR module shall consist of $3 \times 500\,\mathrm{W}$ converter cells. This configuration ensures that, in the advent of a single converter cell failure then the module is still capable of supplying the required 1000 W. This module configuration is depicted in figure 2.1.

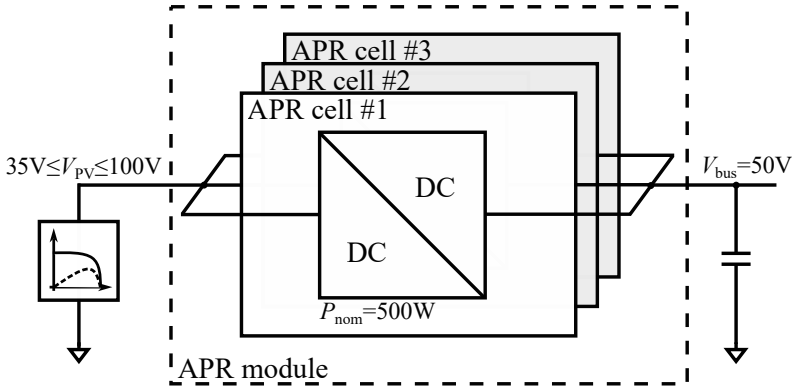


Figure 2.1 Schematic illustration of the APR module with the 3 cell configuration.

From the presented APR module configuration of figure 2.1, it is also apparent that the 3 converter cells must operate in hot redundancy to supply the 1000 W to the main bus [5]. In this chapter, only a single APR cell will be considered to avoid repetitive analysis.

The required module efficiency is a function of the module heat management. Essentially a total loss of 3% is acceptable, yielding an allowed power loss of 15 W per APR cell at full power throughput, following the specifications of table 2.1. Additionally, the PV voltage ripple and input filter capacitance requirements are necessary to ensure that the power is extracted properly from the PV source. The limit on the capacitance is set to avoid interfering with the MPPT

command module [11]. Lastly, the input PV string voltage, and output bus voltage parameters are what imply the need of a step-up-and-down topology. In the following section 2.1, possible converter topologies are covered.

2.1 Converter Topology Comparison and Selection

As given by the APR module requirements, presented in table 2.1, each APR converter cell must be a step-up-and-down topology, also referred to as a buck-boost topology. This is because the wide input range of the PV strings vary above- and below the output bus voltage. This section serves to introduce and compare various DC/DC buck-boost converter topologies with the aim of determining the most suitable topology in view of this project's context.

The converter topology must be able to satisfy three essential requirements. Firstly, the converter must be buck-boost capable within the specified input range of 35 V to 100 V. Secondly, the input current of the converter must be continuous to meet the ripple requirements specified for the PV strings. Lastly, the converter must have a non-inverting input-to-output voltage relationship. While the latter requirement is less intuitive, it relates to the grounding scheme of the PV arrays which serve to prevent ESD caused by spacecraft charging, as introduced in section 1.2.1. For this project, a variety of buck-boost converter topologies are analysed and categorised based on the aforementioned requirements. The selected topologies are chosen in view of the project duration, hence more advanced topologies are excluded from this analysis. The analysed topologies are presented in table 2.2.

Table 2.2 Analysed converter topologies and their relevant characteristics [7] [12].

Topology	Buck-boost capability	Continuous input current	Non-inverting input-to-output	Schematic
Buck-boost	Yes	**No**	**No**	figure A.3a
4-switch buck-boost	Yes	**No**[1]	Yes	figure A.3b
Forward	Yes[2]	**No**	Yes	figure A.3c
Flyback	Yes	**No**	Yes	figure A.3d
SEPIC	Yes	Yes	Yes	figure A.3e
Zeta	Yes	**No**	Yes	figure A.3f
Cúk	Yes	Yes	**No**	figure A.3g

From the topologies of table 2.2 it is observed that only the Single-Ended Primary-Inductor Converter (SEPIC) fulfils the three requirements simultaneously. The flyback and forward converters are isolated topologies which is not a requirement in this context. Continuous input currents could also be achieved with interleaving of converter cells. However, the input current in this case would still be highly distorted [7] [12].

Based on the inherent ability to fulfil all the requirements, along with its relative simplicity, the SEPIC topology is selected as the most promising topology for this project. In spaceflight applications, relative simplicity of circuits is beneficial due to a decreased number of failure

[1] This is only true when the converter is operating in buck mode.
[2] Only true with an adequate turns-ratio.

modes [3]. In the following section 2.2, the SEPIC is covered in greater detail.

2.2 Modelling the Single-Ended Primary-Inductor Converter

This section covers the operational principle of the SEPIC topology, with the aim of developing an analytical model of its characteristics. This analysis forms the necessary framework to design and dimension the SEPIC in accordance with the operational scenario. A detailed schematic of the SEPIC topology is presented in figure 2.2.

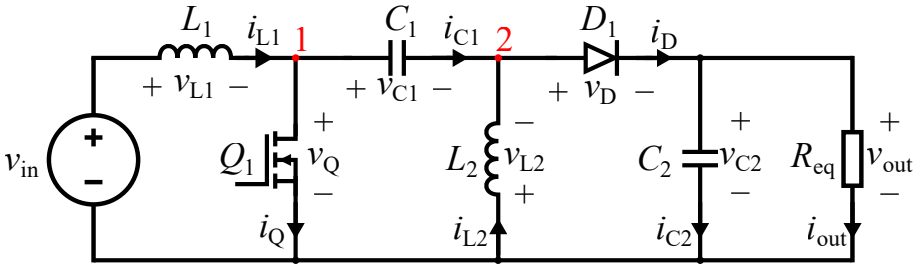


Figure 2.2 SEPIC topology with component polarities [13].

From the SEPIC presented in figure 2.2, it is observed that the topology exists of two inductors, L_1 and L_2, two capacitors, C_1 and C_2, a transistor, Q_1, a diode, D_1, and finally an equivalent load resistance R_{eq}. The input- and output voltage are denoted as v_{in} and v_{out}, respectively.

As with any Switch-Mode Power Supply (SMPS), the instantaneous circuit dynamics depend on the transistor state. Thus, to obtain an analytical model of the SEPIC which properly captures the steady-state as well as the transient dynamics, the topology is modelled following the state-space averaging approach. This involves deriving the state expressions in each transistor state and then averaging the state expressions across each state to eliminate the switching dynamics. The standard state variable model is formulated as presented in equations (2.1) and (2.2).

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{2.1}$$

$$\mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{E}\mathbf{u} \tag{2.2}$$

where $\mathbf{x}$ is the state vector, $\mathbf{u}$ is the input vector, $\mathbf{y}$ is the output vector, $\mathbf{A}$ is the system matrix, $\mathbf{B}$ is the input matrix, $\mathbf{C}$ is the output matrix, and $\mathbf{E}$ is the input-to-output coupling matrix [14]. From the state-space system of equations it is apparent that the system is formulated as a linear system of equations, which is a result of state-space averaging [14]. The following analysis revolves the SEPIC topology in each-state assuming steady-state operation. In this section only Continuous Conduction Mode (CCM) is considered.

2.2.1 Transistor ON State Mode of Operation

When the transistor Q_1 is ON during interval $0 \geq t > D \cdot T$, node 1 is essentially pulled to ground. Here D and T refer to the duty-cycle and switching period, respectively. Therefore node 2 is forced to the inverse voltage across C_1, which in turn reverse biases the diode, D_1. Thereby the state equations regarding the inductors are derived based on Kirchhoff's Voltage Law (KVL), and similarly the state equations for the capacitors are obtained through Kirchhoff's Current

Law (KCL). The state expressions for L_1, L_2, C_1, and C_2, when Q_1 is ON, are presented in equations (2.3), (2.4), (2.5) and (2.6), respectively.

$$v_{\mathrm{L1}} = V_{\mathrm{in}} \quad = \quad L_1 \frac{\mathrm{d}i_{\mathrm{L1}}}{\mathrm{d}t} = V_{\mathrm{in}} \tag{2.3}$$

$$v_{\mathrm{L2}} = v_{\mathrm{C1}} \quad = \quad L_2 \frac{\mathrm{d}i_{\mathrm{L2}}}{\mathrm{d}t} = v_{\mathrm{C1}} \tag{2.4}$$

$$i_{\mathrm{C1}} = -i_{\mathrm{L2}} \quad = \quad C_1 \frac{\mathrm{d}v_{\mathrm{C1}}}{\mathrm{d}t} = -i_{\mathrm{L2}} \tag{2.5}$$

$$i_{\mathrm{C2}} = -\frac{v_{\mathrm{out}}}{R_{\mathrm{eq}}} \quad = \quad C_2 \frac{\mathrm{d}v_{\mathrm{C2}}}{\mathrm{d}t} = -\frac{v_{\mathrm{C2}}}{R_{\mathrm{eq}}} \tag{2.6}$$

Where V_{in} and v_{out} are the input and output voltage, respectively. Utilising equations (2.3) to (2.6) the state-space model, when the transistor is ON, is obtained as presented in equations (2.7) and (2.8).

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{L1}} \\ i_{\mathrm{L2}} \\ v_{\mathrm{C1}} \\ v_{\mathrm{C2}} \end{bmatrix} = \mathbf{A}_1\mathbf{x} + \mathbf{B}_1\mathbf{u} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_2 R_{\mathrm{eq}}} \end{bmatrix} \begin{bmatrix} i_{\mathrm{L1}} \\ i_{\mathrm{L2}} \\ v_{\mathrm{C1}} \\ v_{\mathrm{C2}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{\mathrm{in}} \tag{2.7}$$

$$v_{\mathrm{out}} = \mathbf{C}_1\mathbf{x} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{\mathrm{L1}} & i_{\mathrm{L2}} & v_{\mathrm{C1}} & v_{\mathrm{C2}} \end{bmatrix}^{\intercal} \tag{2.8}$$

where $\mathbf{A}_1$, $\mathbf{B}_1$, and $\mathbf{C}_1$ are the state-space arrays when the transistor Q is ON. Note also here that V_{in} and $v_{\mathrm{out}} = v_{\mathrm{C2}}$ are defined as the system input and -output, respectively.

2.2.2 Transistor OFF State Mode of Operation

When the transistor, Q_1, is turned off during the interval $D \cdot T \geq t > T$, the capacitor C_1 will have a blocking effect on the supply side, while the inductors will discharge to the load. The discharge of the inductor L_2 will forward bias the diode, D_1, effectively pulling up node 2 to v_{out}. Thereby the state expressions are derived as presented in equations (2.9), (2.10), (2.11) and (2.12).

$$V_{\mathrm{in}} = v_{\mathrm{L1}} + v_{\mathrm{C1}} + v_{\mathrm{C2}} \quad = \quad L_1 \frac{\mathrm{d}i_{\mathrm{L1}}}{\mathrm{d}t} = V_{\mathrm{in}} - v_{\mathrm{C1}} - v_{\mathrm{C2}} \tag{2.9}$$

$$v_{\mathrm{L2}} = -v_{\mathrm{C2}} \quad = \quad L_2 \frac{\mathrm{d}i_{\mathrm{L2}}}{\mathrm{d}t} = -v_{\mathrm{C2}} \tag{2.10}$$

$$i_{\mathrm{C1}} = i_{\mathrm{L1}} \quad = \quad C_1 \frac{\mathrm{d}v_{\mathrm{C1}}}{\mathrm{d}t} = i_{\mathrm{L1}} \tag{2.11}$$

$$i_{\mathrm{L1}} + i_{\mathrm{L2}} = i_{\mathrm{C2}} + \frac{v_{\mathrm{C2}}}{R_{\mathrm{eq}}} \quad = \quad C_2 \frac{\mathrm{d}v_{\mathrm{C2}}}{\mathrm{d}t} = i_{\mathrm{L1}} + i_{\mathrm{L2}} - \frac{v_{\mathrm{C2}}}{R_{\mathrm{eq}}} \tag{2.12}$$

Thereby the state-space system of equations are given as presented in equations (2.13) and (2.14).

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\mathrm{L1}} \\ i_{\mathrm{L2}} \\ v_{\mathrm{C1}} \\ v_{\mathrm{C2}} \end{bmatrix} = \mathbf{A}_2\mathbf{x} + \mathbf{B}_2\mathbf{u} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & -\frac{1}{L_1} \\ 0 & 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_1} & \frac{1}{C_1} & 0 & -\frac{1}{C_2 R_{\mathrm{eq}}} \end{bmatrix} \begin{bmatrix} i_{\mathrm{L1}} \\ i_{\mathrm{L2}} \\ v_{\mathrm{C1}} \\ v_{\mathrm{C2}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{\mathrm{in}} \tag{2.13}$$

$$v_{\text{out}} = \mathbf{C}_2\mathbf{x} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{\text{L1}} & i_{\text{L2}} & v_{\text{C1}} & v_{\text{C2}} \end{bmatrix}^{\intercal} \tag{2.14}$$

where $\mathbf{A}_2$, $\mathbf{B}_2$, and $\mathbf{C}_2$ are the state-space arrays when the transistor Q_1 is OFF. The state-space equations in each switching state can be used to derive an average model as presented in the following section 2.2.3.

2.2.3 State-Space Averaging

To obtain an average model of the circuit across both switching states, the state expressions are weighted by the duty-cycle to produce an average state-space model. This is necessary to obtain the steady-state equilibrium points, but also to model the transient dynamics of the SEPIC with a linear system of equations. The weighted average is a consequence of inductor volt-second balance and capacitor charge balance relations. The averaging technique effectively eliminates the switching dynamics across a switching period. The averaging assumes that the switching frequency is much faster than the analogue dynamics [14]. The average state-space model is presented in equations (2.15) and (2.16).

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} = [\mathbf{A}_1 d + \mathbf{A}_2(1-d)]\mathbf{x} + [\mathbf{B}_1 d + \mathbf{B}_2(1-d)]\mathbf{u} \tag{2.15}$$

$$\mathbf{y} = \mathbf{C}\mathbf{x} = [\mathbf{C}_1 d + \mathbf{C}_2(1-d)]\mathbf{x} \tag{2.16}$$

where $\mathbf{A}$, $\mathbf{B}$, and $\mathbf{C}$ are the averaged state-space matrices [14]. Then by substituting the state equations (2.7) and (2.13) into equations (2.15) and (2.16), yields equations (2.17) and (2.18).

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_{\text{L1}} \\ i_{\text{L2}} \\ v_{\text{C1}} \\ v_{\text{C2}} \end{bmatrix} = \mathbf{A} + \mathbf{B}\mathbf{u} = \begin{bmatrix} 0 & 0 & -\frac{1-d}{L_1} & -\frac{1-d}{L_1} \\ 0 & 0 & \frac{d}{L_2} & -\frac{1-d}{L_2} \\ \frac{1-d}{C_1} & -\frac{d}{C_1} & 0 & 0 \\ \frac{1-d}{C_2} & \frac{1-d}{C_2} & 0 & -\frac{1}{C_2} \end{bmatrix} \begin{bmatrix} i_{\text{L1}} \\ i_{\text{L2}} \\ v_{\text{C1}} \\ v_{\text{C2}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{\text{in}} \tag{2.17}$$

$$v_{\text{out}} = \mathbf{C}\mathbf{x} = \begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{\text{L1}} & i_{\text{L2}} & v_{\text{C1}} & v_{\text{C2}} \end{bmatrix}^{\intercal} \tag{2.18}$$

Thereby the averaged state-space model of the SEPIC is derived per equations (2.17) and (2.18). Note here that all states, as well as the output, are time-variant signals, denoted by the lowercase variables. To construct a DC model the variables are split into a DC- and small-signal components as presented in equations (2.19) to (2.23).

$$i_{\text{L1}} = I_{\text{L1}} + \tilde{i}_{\text{L1}} \tag{2.19}$$

$$i_{\text{L2}} = I_{\text{L2}} + \tilde{i}_{\text{L1}} \tag{2.20}$$

$$v_{\text{C1}} = V_{\text{C1}} + \tilde{v}_{\text{C1}} \tag{2.21}$$

$$v_{\text{C2}} = V_{\text{C2}} + \tilde{v}_{\text{C2}} \tag{2.22}$$

$$d = D + \tilde{d} \tag{2.23}$$

where the uppercase variables represent the steady-state equilibrium points, and the variables marked by '$\sim$' represent small-signal perturbations thereof. Note here that the input vector, $\mathbf{u}$, is not constructed with any small-signal component, as it is assumed to be an ideal voltage source. To solve for the steady-state equilibrium points, the time-variant small-signal components are

set to zero, which results in $\dot{X} = 0$ because only the DC component remain. Then the state- and output vector are isolated, resulting in the steady-state equilibrium points presented in equations (2.24) and (2.25).

$$0 = \mathbf{AX} + \mathbf{BU} \quad \Leftrightarrow \quad \mathbf{X} = -\mathbf{A}^{-1}\mathbf{BU} \quad = \quad \begin{bmatrix} I_{\mathrm{L1}} \\ I_{\mathrm{L2}} \\ V_{\mathrm{C1}} \\ V_{\mathrm{C2}} \end{bmatrix} = \begin{bmatrix} \frac{D^2}{(1-D)^2}\frac{V_{\mathrm{in}}}{R_{\mathrm{eq}}} \\ \frac{D}{1-D}\frac{V_{\mathrm{in}}}{R_{\mathrm{eq}}} \\ V_{\mathrm{in}} \\ \frac{D}{1-D}V_{\mathrm{in}} \end{bmatrix} \tag{2.24}$$

$$\mathbf{Y} = (-\mathbf{CA}^{-1}\mathbf{B})\mathbf{U} \quad = \quad V_{\mathrm{out}} = \frac{D}{1-D}V_{\mathrm{in}} \tag{2.25}$$

where $\mathbf{X}$ and $\mathbf{U}$ represent the equilibrium state- and input vector, respectively. D is the steady-state duty-cycle. From the steady-state equilibrium points it is validated that the voltage ratio of the SEPIC is that of a non-inverting buck-boost converter. Additionally it is observed that capacitor C_1 carries the input voltage independently of the duty-cycle [14].

Assuming an ideal system, input-to-output power balance indicates that inductor L_2 carries the output load current, $I_{\mathrm{out}} = V_{\mathrm{out}}/R_{\mathrm{eq}}$, while the inductor L_1 carries the input supply current, I_{in}. This is derived from equation (2.25) as presented in equation (2.26).

$$V_{\mathrm{out}} \cdot I_{\mathrm{out}} = V_{\mathrm{in}} \cdot V_{\mathrm{in}} \quad \Leftrightarrow \quad \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{I_{\mathrm{in}}}{I_{\mathrm{out}}} = \frac{D}{1-D}$$

$$\begin{bmatrix} I_{\mathrm{L1}} \\ I_{\mathrm{L2}} \\ V_{\mathrm{C1}} \\ V_{\mathrm{C2}} \end{bmatrix} = \begin{bmatrix} \frac{D^2}{(1-D)^2}\frac{V_{\mathrm{in}}}{R_{\mathrm{eq}}} \\ \frac{D}{1-D}\frac{V_{\mathrm{in}}}{R_{\mathrm{eq}}} \\ V_{\mathrm{in}} \\ \frac{D}{1-D}V_{\mathrm{in}} \end{bmatrix} = \begin{bmatrix} \frac{D}{1-D}\frac{V_{\mathrm{out}}}{R_{\mathrm{eq}}} \\ \frac{V_{\mathrm{out}}}{R_{\mathrm{eq}}} \\ V_{\mathrm{in}} \\ V_{\mathrm{out}} \end{bmatrix} = \begin{bmatrix} I_{\mathrm{in}} \\ I_{\mathrm{out}} \\ V_{\mathrm{in}} \\ V_{\mathrm{out}} \end{bmatrix} \tag{2.26}$$

Note that $V_{\mathrm{in}} = V_{\mathrm{PV}}$ as each APR cell is in parallel to the same source. Based on equation (2.26) the state equations during each switching state might be simplified as presented in the following.

Transistor ON State interval ($0 \geq t > DT$):

Equations (2.4) to (2.6) are simplified to equations (2.27), (2.28) and (2.29), respectively.

$$v_{\mathrm{L2}} = L_2\frac{\mathrm{d}i_{\mathrm{L2}}}{\mathrm{d}t} = V_{\mathrm{in}} \tag{2.27}$$

$$i_{\mathrm{C1}} = C_1\frac{\mathrm{d}v_{\mathrm{C1}}}{\mathrm{d}t} = -I_{\mathrm{out}} \tag{2.28}$$

$$i_{\mathrm{C2}} = C_2\frac{\mathrm{d}v_{\mathrm{C2}}}{\mathrm{d}t} = -I_{\mathrm{out}} \tag{2.29}$$

Transistor OFF State Interval ($DT \geq t > T$):

Similarly, equations (2.9) to (2.12) are simplified to equations (2.30), (2.31), (2.32) and (2.33), respectively.

$$v_{\mathrm{L1}} = L_1\frac{\mathrm{d}i_{\mathrm{L1}}}{\mathrm{d}t} = -V_{\mathrm{out}} \tag{2.30}$$

$$v_{\mathrm{L2}} = L_2\frac{\mathrm{d}i_{\mathrm{L2}}}{\mathrm{d}t} = -V_{\mathrm{out}} \tag{2.31}$$

$$i_{C1} = C_1 \frac{\mathrm{d}v_{C1}}{\mathrm{d}t} = I_{in} \tag{2.32}$$

$$i_{C2} = C_2 \frac{\mathrm{d}v_{C2}}{\mathrm{d}t} = I_{in} \tag{2.33}$$

From equations (2.27), (2.28) and (2.33) it is observed that the mean voltage and -current in each component is constant. However, when inductors discharge the current magnitude decreases linearly, and similarly when capacitors discharge the voltage decrease linearly. This is used to derive the waveforms in each component as presented in the following section 2.2.4.

2.2.4 Component Switching Waveforms

Based on the state expressions of sections 2.2.1 to 2.2.3 and the principle of inductor volt-sec as well as capacitor charge balance, the waveforms across each circuit element is obtained as presented in figure 2.3. With the knowledge of the derived component waveforms, the component values and stresses can be comprehended. The component values are presented in the following section 2.3.

2.3 Passive Component Values in the SEPIC

This section aims to determine the component values in the SEPIC to satisfy the SMPS requirements of table 2.1. This is achieved based on the theory presented in section 2.2. The root to properly determining the values of the passive component are all derived based on the governing equations of a capacitor and an inductor, as presented in Equations (2.34).

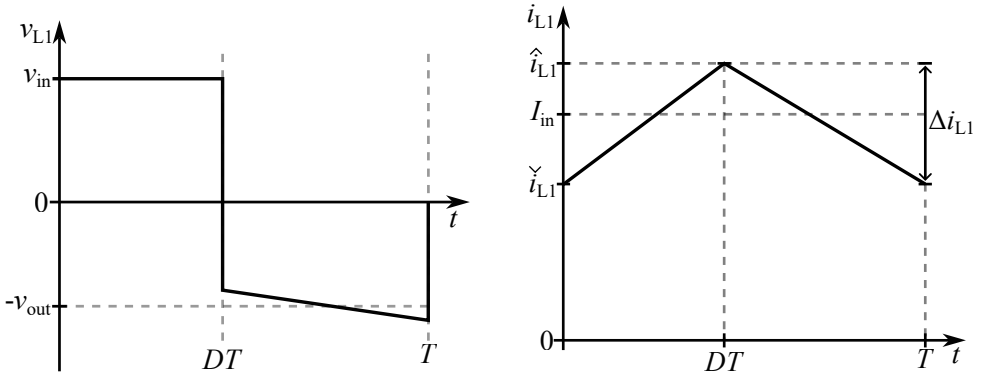
$$v_L = L\frac{\mathrm{d}i_L}{\mathrm{d}t} \approx L\frac{\Delta I_L}{\Delta t} \quad , \quad i_C = C\frac{\mathrm{d}v_C}{\mathrm{d}t} \approx C\frac{\Delta V_C}{\Delta t} \tag{2.34}$$

where v_L is the inductor voltage, L is the inductance, i_L is the inductor current, i_C is the capacitor current, C is the capacitance, and v_C is the capacitor voltage. That is for a given operating point, the magnitude of the passive component determines the ripple magnitude of the signal, i.e. capacitor voltage or inductor current. It is apparent that the inductance relates to current ripple, while capacitance relates to voltage ripple [14].

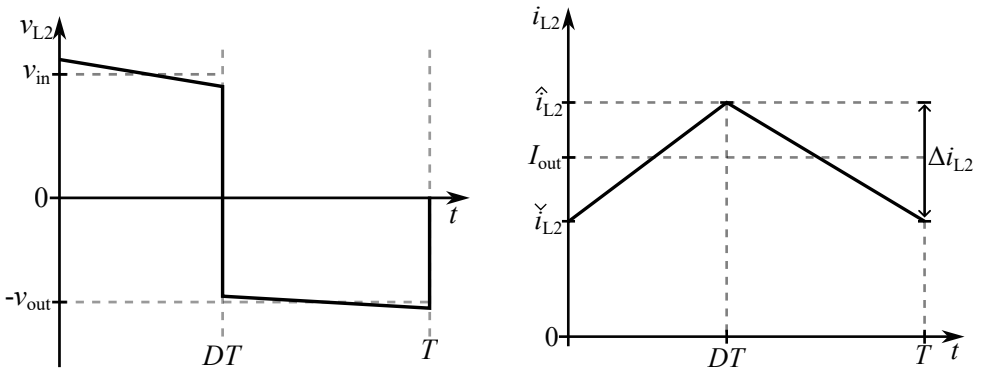
However, in table 2.1 a requirement for the input voltage is given, and not for the current. This relationship is given by the input filter capacitance which acts as a decoupling capacitor. The purpose of this capacitor is therefore to source- and sink the current ripple from the SEPIC such that the ripple is not supplied directly by the PV arrays. Thus from the current ripple in the capacitor, the relationship between the input voltage ripple and -current ripple is given by equation (2.35).

$$\Delta V_{in} = \frac{\Delta I_{in}}{8 \cdot f_{sw} \cdot C_{in}}$$
$$\Delta I_{in} = 8 \cdot \Delta V_{in} \cdot C_{in} \cdot f_{sw} \tag{2.35}$$

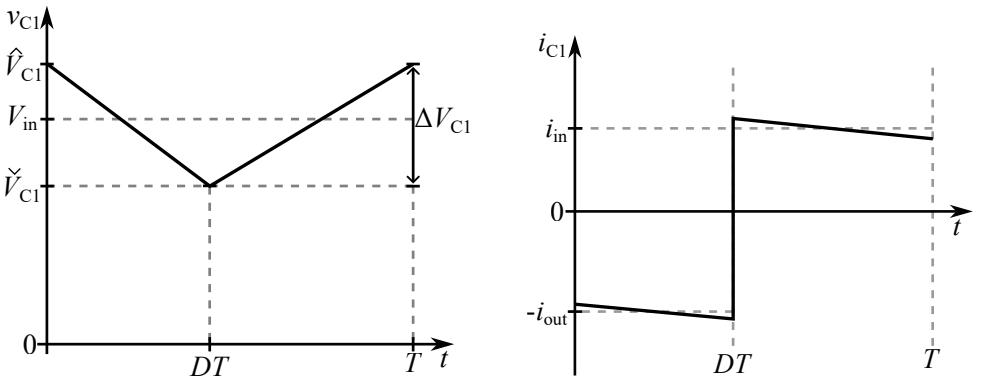
where ΔV_{in} is the input voltage ripple, ΔI_{in} is the input current ripple, C_{in} is the input filter capacitance, and f_{sw} is the SEPIC switching frequency. The derivation of equation (2.35) is outlined in appendix A.1. As derived in equation (2.26), the input current, I_{in}, flows in L_1 and the waveforms are presented in figure 2.3a. Hence, based on equation (2.34) and the voltage



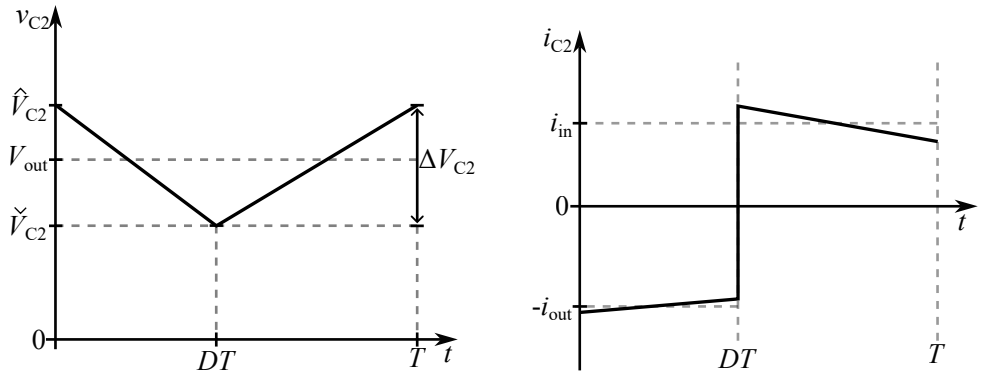
(a) Waveforms of L_1.



(b) Waveforms of L_2.



(c) Waveforms of C_1.



(d) Waveforms of C_2.

Figure 2.3 Stacked visualization of component waveforms in the SEPIC topology.

across L_1 during $0 \geq t > DT$, the inductance L_1 relates to the input current ripple, ΔI_{in}, as presented in equation (2.36).

$$V_{\text{in}} = L_1 \frac{\Delta I_{\text{in}}}{\Delta t} \quad \Leftrightarrow \quad L_1 = \frac{V_{\text{in}}}{\Delta I_{\text{in}}} \frac{D}{f_{\text{sw}}} \tag{2.36}$$

Similarly, the relationship between component value and ripple magnitude can be found for all passive components in the SEPIC based in the subinterval $0 \geq t > DT$. Thus these relationships for L_2, C_1, and C_2 are also presented in equations (2.37), (2.38) and (2.39), respectively.

$$L_2 = \frac{V_{\text{in}}}{\Delta I_{\text{out}}} \frac{D}{f_{\text{sw}}} \tag{2.37}$$

$$C_1 = \frac{I_{\text{out}}}{\Delta V_{\text{in}}} \frac{D}{f_{\text{sw}}} \tag{2.38}$$

$$C_2 = \frac{I_{\text{out}}}{\Delta V_{\text{out}}} \frac{D}{f_{\text{sw}}} \tag{2.39}$$

From equations (2.36) to (2.39) the values of the passive components in the SEPIC topology, can be derived based on the current- and voltage ripple amplitudes. These are used to compute the component values in the following section 2.3.1.

2.3.1 Computation of the Passive Component Values

In this project, the component values of the SEPIC topology must be dimensioned to fulfil the APR module requirements, as presented in table 2.1. To apply the relations derived in equations (2.36) to (2.39), the steady-state input- and output magnitudes must be computed. To compute this, the state-space equilibrium expressions of equations (2.24) and (2.25) are used, in regards to an operating point of 500 W ($R_{\text{eq}} = 5\,\Omega$), resulting in the values of table 2.3.

Table 2.3 Steady-state current- and voltage magnitudes of the SEPIC operated at $P = 500\,\text{W}$.

Parameter	LV input	HV input
V_{in}	35 V	100 V
V_{out}	50 V	50 V
D	0.588	0.333
I_{in}	14.3 A	5.0 A
I_{out}	10.0 A	10.0 A

In view of the largest allowable input capacitance of 20 µF, the maximum allowable input current ripple is computed using equation (2.36) as presented in equation (2.40).

$$\Delta I_{\text{in}} \leq 8 \cdot 5\,\text{mV} \cdot 20\,\mu\text{F} \cdot 500\,\text{kHz} = 0.4\,\text{A} \tag{2.40}$$

From equation (2.40) it is revealed that a switching frequency of 500 kHz is used for the SEPIC in this project. This relatively high switching frequency is selected to allow a smaller and more compact construction. The value is selected heuristically, without conducting any thorough optimisation study. The implication of this switching frequency is further elaborated and discussed in chapter 7 near the end of this report. Then the value of L_1 is computed using equation (2.36) as presented in equation (2.41).

$$L_1 = \frac{35\,\text{V} \cdot 0.588}{0.4\,\text{A} \cdot 500\,\text{kHz}} = 102.90\,\mu\text{H} \quad , \quad L_1 = \frac{100\,\text{V} \cdot 0.333}{0.4\,\text{A} \cdot 500\,\text{kHz}} = 166.67\,\mu\text{H} \tag{2.41}$$

On the other hand, the ripple magnitudes of L_2, C_1, and C_2 are not subject to any explicit constraint. Therefore ripple values of 20%, 5%, and 1% are chosen for L_2, C_1, and C_2, respectively. Thus utilising equations (2.37), (2.38) and (2.39) in view of the chosen ripple amplitudes, the component values for, L_2, C_1, and C_2 are computed in a similar manner. Each equation is computed in terms of the input voltage bounds, that is $V_{\text{in}} = 35\,\text{V}$ and $V_{\text{in}} = 100\,\text{V}$. For the results of each computation the highest value is selected to ensure that the ripple requirements are met within the entire input voltage range. This results in the minimum component values presented in table 2.4.

Table 2.4 SEPIC component values to fulfil the ripple requirements within the PV input voltage range.

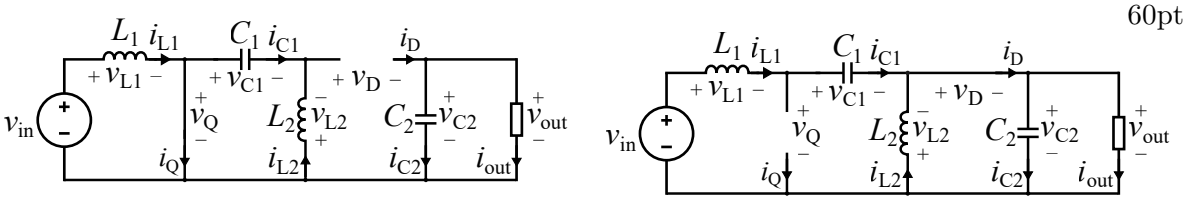
Component	L_1	L_2	C_1	C_2
Value	$\geq 166.67\,\mu\text{H}$	$\geq 33.33\,\mu\text{H}$	$\geq 6.72\,\mu\text{F}$	$\geq 23.53\,\mu\text{F}$

From the computed values of table 2.4 it should be noted that C_2 is not the actual bus capacitance. In practice all APR cells would interface to the main bus capacitance, as represented in figure 2.1, meaning C_2 is in parallel to the main bus capacitance. The main bus is required by the ECSS standards to fulfil a certain impedance mask [6]. For a 28 V regulated bus the impedance mask requirement results in a necessary capacitance of around 1.5 mF/kW [15].

2.4 Semiconductor Stresses in the SEPIC

To achieve an optimal design of a SEPIC, it is necessary to have an understanding of the semiconductor stresses. As outlined in section 2.2, when the transistor, Q_1, is conducting, then the diode, D_1 is in reverse-bias mode and vice versa. Thus Q_1 and D_1 operate in a complimentary manner, both switching at a frequency of f_{sw}. Each switching state of the SEPIC topology is presented in figure 2.4.

60pt



(a) ON state.

(b) OFF state.

Figure 2.4 SEPIC topology in each of the ON and OFF switching states.

In the ON state, depicted in figure 2.4a, L_1 and C_1 are shorted to ground. L_2 is being charged by C_1 through the transistor. Moreover, the anode of the diode is at a potential of $-V_{\text{C1}}$, while the cathode is at the output voltage of V_{C2}. Therefore the current in the transistor and the voltage of the diode, in the ON state, is given as presented in equations (2.42) and (2.43), respectively.

$$I_{\text{Q(ON)}} = I_{\text{L1}} + I_{\text{L2}} \approx I_{\text{in}} + I_{\text{out}} \tag{2.42}$$

$$V_{\text{D(ON)}} = -V_{\text{C1}} - V_{\text{C2}} \approx -(V_{\text{in}} + V_{\text{out}}) \tag{2.43}$$

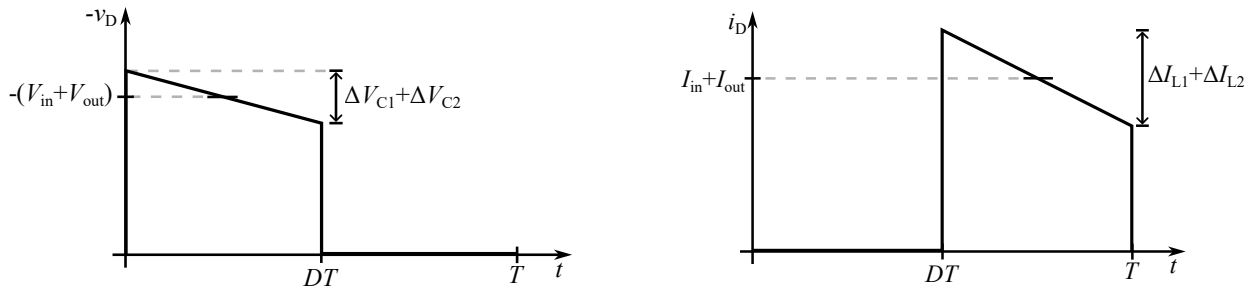
In the OFF state illustrated in figure 2.4b, the diode is conducting the sum of I_{L1} and I_{L2} through to the load and capacitor C_2, as depicted in figure 2.3d. Furthermore, the drain of

the transistor is seeing C_1 and C_2 is series which are both charging up through the diode, as illustrated from figures 2.3c and 2.3d. Thus the transistor blocking voltage and the diode current is given in equations (2.44) and (2.45), respectively.

$$V_{\mathrm{Q(OFF)}} = V_{\mathrm{C1}} + V_{\mathrm{C2}} \approx V_{\mathrm{in}} + V_{\mathrm{out}} \tag{2.44}$$

$$I_{\mathrm{D(OFF)}} = I_{\mathrm{L1}} + I_{\mathrm{L2}} \approx I_{\mathrm{out}} + I_{\mathrm{in}} \tag{2.45}$$

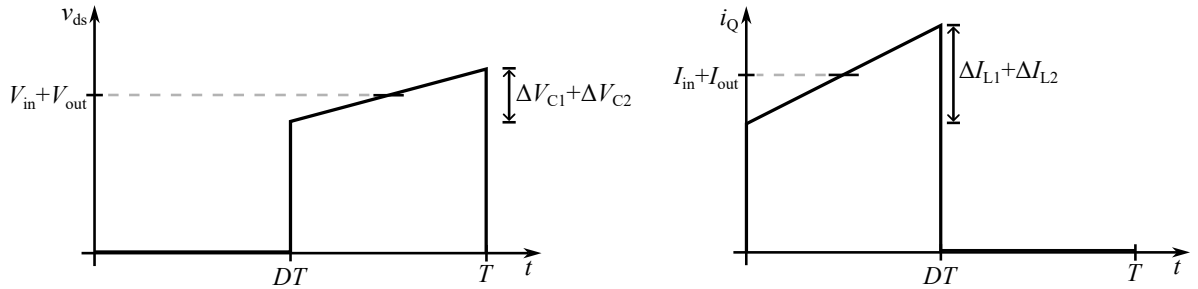
From the derived voltage- and current magnitudes, the semiconductor waveforms can be derived. The diode waveforms are derived from equations (2.43) and (2.45) and are depicted in figure 2.5.



(a) Voltage. **(b)** Current.

Figure 2.5 Waveforms of the diode in the SEPIC topology in CCM.

Similarly, the transistor waveforms are derived from equations (2.42) and (2.44) and depicted in figure 2.6.



(a) Voltage. **(b)** Current.

Figure 2.6 Waveforms of the transistor in the SEPIC topology in CCM.

Thus it is apparent that the stresses on the semiconductors in the SEPIC topology is rather high. This is an important observation, especially when it comes to selecting the specific components for the transistor, Q_1, and the diode, D_1 [13].

2.5 Coupled Inductors in the SEPIC Topology

As presented in section 2.2.4, the inductors, L_1 and L_2, share the same volt-sec balance. Therefore L_1 and L_2 can be wound on the same magnetic core [14]. A schematic of the SEPIC with a coupled inductor is presented in figure 2.7.

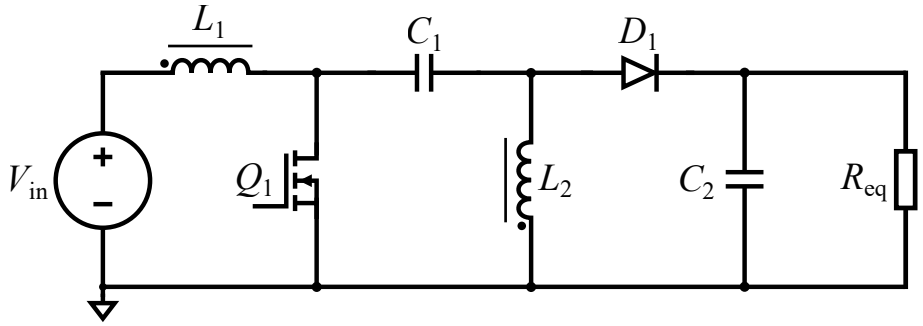
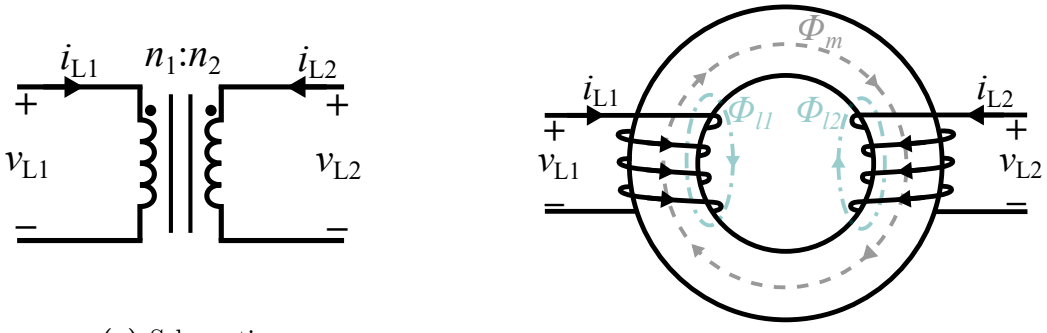


Figure 2.7 Schematic of the SEPIC topology with a coupled inductor.

The coupled SEPIC topology is directly derived from the uncoupled counterpart illustrated in figure 2.2. The polarity is derived from the dot convention, ensuring that the voltage phase relationship is maintained [14].

2.5.1 Fundamentals of the Coupled Inductor

The principle of the coupled inductor is illustrated in figure 2.8.



(a) Schematic.

(b) On toroid core.

Figure 2.8 Illustration of a coupled inductor on a common magnetic core.

where n_1 and n_2 represent each windings number of turns, Φ_m represent the core magnetic flux, and Φ_{l1} and Φ_{l2} represent leakage magnetic flux of each winding. The generated flux on each coil consists of magnetisation flux and leakage flux, as presented in equation (2.46).

$$\Phi_1 = \Phi_{m1} + \Phi_{l1} \quad , \quad \Phi_2 = \Phi_{m2} + \Phi_{l2} \tag{2.46}$$

The total core magnetic flux is given by the sum of each magnetisation fluxes, as their flux paths close through the magnetic core. However, on each coil there is a certain amount of leakage flux, as depicted in figure 2.8b. This means that each coil is magnetically coupled through the magnetic core, as given from the flux linkage in equations (2.47) and (2.48).

$$\lambda_1 = n_1\Phi_{m1} + n_1\Phi_{l1} + n_1\Phi_{m2} = \frac{n_1\Phi_{m1}}{i_{L1}} \cdot i_{L1} + \frac{n_1\Phi_{l1}}{i_{L1}} \cdot i_{L1} + \frac{n_1\Phi_{m2}}{i_{L2}} \cdot i_{L2}$$

$$\lambda_1 = (L_{m1} + L_{l1}) \cdot i_{L1} + M_{12} \cdot i_{L2} \tag{2.47}$$

Similarly:

$$\lambda_2 = n_2\Phi_{m2} + n_2\Phi_{l2} + n_2\Phi_{m1} = \frac{n_2\Phi_{m2}}{i_{L2}} \cdot i_{L2} + \frac{n_2\Phi_{l2}}{i_{L2}} \cdot i_{L2} + \frac{n_2\Phi_{m1}}{i_{L1}} \cdot i_{L1}$$

$$\lambda_2 = (L_{m2} + L_{l2}) \cdot i_{\mathrm{L2}} + M_{21} \cdot i_{\mathrm{L1}} \tag{2.48}$$

where λ_1 and λ_2 are the flux linkages, and M_{12} and M_{12} are the mutual inductance terms. Then equations (2.47) and (2.48) can be derived further through the use of Faraday's law of induction, to yield the system of equations presented in equation (2.49).

$$\begin{bmatrix} v_{\mathrm{L1}} \\ v_{\mathrm{L2}} \end{bmatrix} = \begin{bmatrix} L_1 & M_{12} \\ M_{21} & L_2 \end{bmatrix} \begin{bmatrix} \frac{\mathrm{d}i_{\mathrm{L1}}}{\mathrm{d}t} \\ \frac{\mathrm{d}i_{\mathrm{L2}}}{\mathrm{d}t} \end{bmatrix} \tag{2.49}$$

where $L_1 = (L_{m1} + L_{l1})$, and $L_2 = (L_{m2} + L_{l2})$ [16]. Note that in the SEPIC topology each winding must have the same number of turns: $n_1 = n_2$, to satisfy that: $v_{\mathrm{L1}} = v_{\mathrm{L2}}$, as outlined in section 2.2. Furthermore, it is given that $\Phi_m \propto i_{\mathrm{L1}}$ and $\Phi_m \propto i_{\mathrm{L2}}$, thereby the mutual inductances are symmetrical as: $M = M_{12} = M_{21}$. Thus, from comparing equation (2.49) to equation (2.34), it is apparent that the effective inductance of each winding is given by equations (2.50) and (2.51).

$$L_{\mathrm{eff,\ 1}} = L_1 + M \tag{2.50}$$

$$L_{\mathrm{eff,\ 2}} = L_2 + M \tag{2.51}$$

where $L_{\mathrm{eff,\ 1}}$ and $L_{\mathrm{eff,\ 2}}$ are the effective inductances seen at winding 1 and -2, respectively. From equations (2.50) and (2.51) it is observed that the mutual inductance adds to the self inductance of each winding. Thereby less number of turns are required to reach the same effective inductance on each winding, in comparison to the uncoupled version of the SEPIC topology. The mutual inductance is related to the self inductance by equation (2.52).

$$M = k\sqrt{L_1 L_2} \tag{2.52}$$

where k is the coupling factor. The coupling factor is a coefficient that describes the degree of coupling between the two windings [12]. It is clear that in the case of the SEPIC, a high degree of coupling is desired, as it results in a higher mutual inductance. This in turn means that less number of turns are needed to achieve the required effective inductance value. On the other hand, as an equal number of turns are required on both windings, it is possible that the total amount of wire is not reduced in comparison to an uncoupled SEPIC topology. This can result in a greater effective inductance on the secondary side than necessary, however it also results in less current ripple in the SEPIC [14]. This is entirely dependant on the required inductance values from the specific design.

Based on equation (2.49) the equivalent circuit of the coupled inductor can be derived as presented in section 2.5.1. Here it is seen that the terms $L_1 - M$ and $L_2 - M$ correspond to the leakage inductances. Furthermore if parasitic inter-winding capacitance is considered it is observed from figure 2.7 that it is simply in parallel with the input voltage source, or the capacitor C_1. That is, inter-winding capacitance is not an issue in the SEPIC. Thus it is reasonable to coupled the inductors with the highest possible coupling factor, to have as much mutual inductance as possible. Furthermore

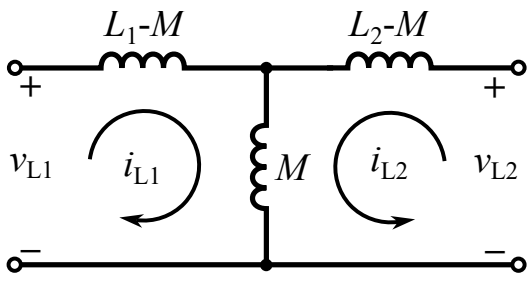


Figure 2.9 Equivalent circuit of equation (2.49).

it is seen that if there is a difference in v_{L1} and v_{L2}, the residual voltage will form be across the leakage inductances. Thus the leakage inductances also serve to ensure balance of Faraday's law in case of voltage differences. However, to establish a voltage across the leakage inductance, a rate-of-change of current must flow. So in case of large voltage deviates between v_{L1} and v_{L2}, additional current will have to flow into the inductor. Thus it is clear that it is desirable that the voltages, v_{L1} and v_{L2}, are as close as possible to limit additional current from flowing due to voltage across the leakage inductances. Therefore it is necessary to have $n_1 = n_2$ for the SEPIC topology with coupled inductors.

Additionally, as the magnetising flux of each winding is generated in the same direction, the resulting magnetising flux is the sum of each flux generated, as presented in (2.53).

$$H = \frac{n_1 i_{L1} + n_2 i_{L2}}{l_e} \tag{2.53}$$

where l_e is the effective length of the flux path [14]. Thus the selected core must ensure that saturation does not occur even when both windings carry maximum current. The utilisation of the theory outlined in this section is used to determine the necessary core parameters, and the required number of turns. This is described in appendix A.3.

3 Efficiency Analysis of the SEPIC

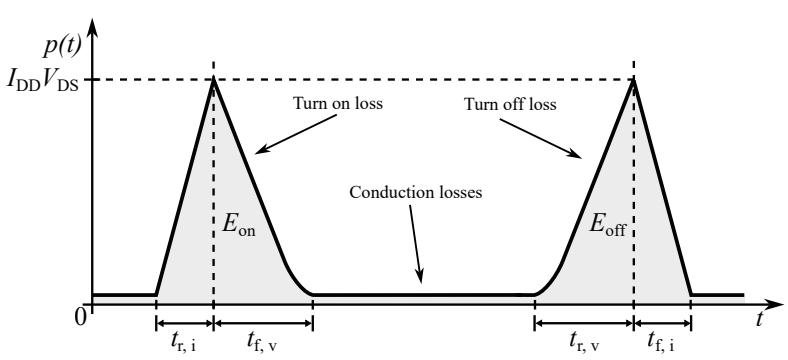
As outlined in section 1.3, one of the objectives of this project is to evaluate the feasible efficiency of the chosen step-up-and-down topology. Therefore this chapter revolves around the power losses of the SEPIC topology. To evaluate the power losses comprehensively, the losses of each components in the SEPIC topology are analysed separately. The goal of this analysis is to model, estimate, and ultimately determine how the power losses of the SEPIC topology are minimised.

3.1 Component Power Losses in the SEPIC

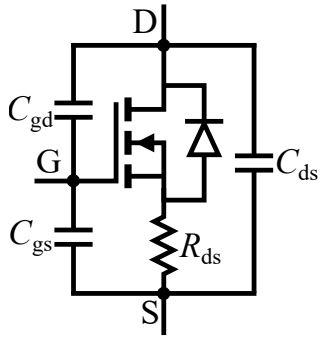
The SEPIC consists of 4 passive components and 2 active components, each of which are analysed further in this section. This analysis describes the power losses associated with each component, the influencing parameters, and how they affect the losses.

3.1.1 Transistor Power Losses

To simplify the transistor loss analysis for this project, the following loss mechanisms are considered: Switching losses, conduction losses, and output capacitance losses. In general these losses occur either during a switching event, or during conduction as illustrated in figure 3.1a. Where figure 3.1b illustrated the parasitics of a transistor, which are the fundamental reason why a switching event is non-ideal.



(a) Simplified time-domain power losses in a transistor.



(b) Transistor with parasitic elements.

Figure 3.1 Power losses in transistor with a diode-clamped inductive output [7].

where E_{on} and E_{off} are the turn on- and off energy loss, respectively. I_{DD} is the on-state drain current and V_{DS} is the off-state drain-to-source voltage. Finally t_r and t_f describe the rise- and fall time interval, respectively, with 'i' or 'v' designating whether the period refers to current- or voltage transients.

Switching Losses

Switching losses in a transistor occur during each turn-on and turn-off event. In a diode clamped inductive output, as the presented version of the SEPIC topology, it is assumed that the voltage and current do not fall/rise simultaneously. For example, in the turn on example the drain

current rises when the gate threshold voltage is applied. But when the drain current reaches full load current, the gate-to-drain capacitance, C_{gd} must subsequently be charged by the gate drive which causes the drain-to-source voltage to drop subsequently to the current rise. During the fall time of the drain-to-source voltage, v_{ds}, the gate-to-source voltage is clamped while while charge is transferred into the gate-to-drain capacitance, C_{gd}, which is the cause of the common gate-to-drain plateau. The important take away here, is the two distinct periods where the voltage and current rises and falls non-simultaneously. This causes an overlap of current and voltage, resulting in a energy loss [7].

In figure 3.1a two periods of overlap are observed, one where the current changes and one where the voltage changes, where the point in-between is the point of largest instantaneous energy loss, as the current and voltage are at full magnitude simultaneously. Due to this pattern, the amount of energy during each transient can be approximated by equation (3.1).

$$E_{\text{on}} = \frac{1}{2} V_{\text{DS}} I_{\text{DD}} t_{\text{r}} \qquad , \qquad E_{\text{off}} = \frac{1}{2} V_{\text{DS}} I_{\text{DD}} t_{\text{f}} \tag{3.1}$$

where t_{r} and t_{f} is the accumulative rise- and fall transient periods, respectively. During each switching cycle, there will always occur a pair of on- and off overlap losses as presented in equation (3.1), thereby the power loss can be approximated as given from equation (3.2).

$$P_{\text{sw}} = \frac{1}{2} V_{\text{DS}} I_{\text{D}} (t_{\text{r}} + t_{\text{f}}) f_{\text{sw}} \tag{3.2}$$

where P_{sw} are the switching losses due to voltage- and current overlap [7] [14].

Conduction Losses

Conduction losses occur during the ON time of the transistor. This period exhibits losses due to the intrinsic resistance of the conduction channel in the transistor, which is represented with $R_{\text{ds(on)}}$ as depicted in figure 3.1b. Thereby the conduction loss of a transistor is given by equation (3.3).

$$P_{\text{Q, cond}} = {I_{\text{DD}}}^2 \cdot R_{\text{ds(on)}} \tag{3.3}$$

where $P_{\text{Q, cond}}$ is the conduction power loss in the transistor, I_{DD} is the Root Mean Square (RMS) value of the transistor drain current, and $R_{\text{ds(on)}}$ is the transistor on-resistance. The RMS value of the pulsating drain current with a linear ripple is given by equation (3.4).

$$I_{\text{DD}} = I_{\text{on}} \sqrt{D} \sqrt{1 + \frac{1}{3} \left(\frac{\Delta i_{\text{DD}}}{I_{\text{on}}} \right)^2} \tag{3.4}$$

where I_{on} is the mean on-state current and Δi_{D} is the ripple amplitude [7] [14].

Output Capacitance Losses

When the transistor is OFF, and is blocking the full drain-to-source voltage, V_{ds}, then the output capacitance, $C_{\text{oss}} = C_{\text{ds}} + C_{\text{gd}}$ is charged. When the transistor turns on, the stored energy in the parasitic capacitance is dissipated in the transistor. The stored energy in the drain-to-source capacitance is given from .

$$E_{\text{oss}} = \frac{1}{2} C_{\text{oss}} {V_{\text{DS}}}^2 \tag{3.5}$$

where E_{oss} is the energy stored in the output capacitance. This occurs every turn-on event, thereby the device capacitance power losses are given from equation (3.6).

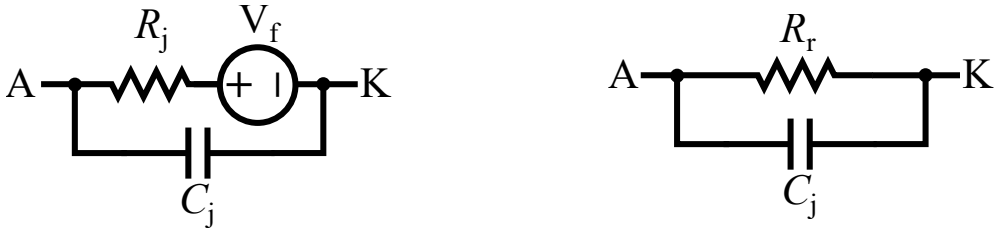
$$P_{oss} = E_{oss} \cdot f_{sw} = \frac{1}{2} C_{oss} {V_{DS}}^2 \cdot f_{sw} \tag{3.6}$$

where P_{oss} is the switching loss caused from parasitic capacitance. It is noteworthy that these losses are related to the square of the drain-to-source voltage, thus at higher voltage these losses can become critical. On the other hand, the parasitic drain-to-source capacitance also decrease as a function of increasing voltage magnitude, so the relationship is not strictly quadratic [14].

The power losses of a transistor, as introduced in this section, is a simplification of the true switching transients and a highly idealised view. In practice switching losses are highly non-linear and can be very complex to model. However, the theory of this section outlines the principles, and can be used to give a rough estimate of the power losses in a transistor. It is essential to note that per equations (3.2), (3.3) and (3.6) that the switching losses are linearly dependant on the current magnitude, whereas the conduction losses are quadratically dependant on the current magnitude [7].

3.1.2 Diode Power Losses

A schematic representation of a diode including parasitics in each state is presented in figure 3.2.



(a) Forward biased. **(b)** Reverse biased.

Figure 3.2 Equivalent circuit of a diode in forward biased- and reverse biased mode [7].

where A and K denote the anode- and cathode terminal, respectively. When the diode is forward-biased, figure 3.2a is seen by the circuit, where R_j is the junction resistance, V_f is the constant junction forward voltage, and C_j is the junction capacitance. When the diode becomes reverse biased figure 3.2b is seen, where R_r is the reverse biased resistance, which causes leakage current to flow from cathode to anode.

Conduction Losses

The most prominent factor of losses in a diode is due to the forward voltage of the p-n junction during conduction. As depicted in figure 3.2a, the channel of a diode has a given resistance, while the space-charge region exhibits an electric field which causes a constant voltage drop. The forward losses of a diode is given from equation (3.7).

$$P_{forw} = I_D \cdot (V_F + I_D \cdot R_j) \tag{3.7}$$

where $P_{D,\,cond}$ is the diode conduction loss, I_f is the diode forward RMS current, and V_f. The forward voltage of diodes are typically $< 1\,V$, however the forward voltage is not constant, and

varies with operational conditions. The RMS of the diode current in the SEPIC is also computed with equation (3.4) due to symmetry, but with a duty cycle of $1 - D$ [14].

Junction Capacitance Losses

Similar to the charge capacitance losses of a transistor during turn on, described in section 3.1.1, the diode also has capacitive losses during turn on. This is caused by the junction capacitance, C_j, which is a direct consequence of stored charge in the space charge region. As the diode turns on, the junction capacitance is forced to discharge, which is does through the channel resistance of the diode. Thereby the junction capacitance losses of the diode is given as presented in equation (3.8).

$$P_\mathrm{j} = \frac{1}{2} C_\mathrm{j} {V_\mathrm{R}}^2 \cdot f_\mathrm{sw} \tag{3.8}$$

where P_j is the junction capacitance power loss and V_R is the reverse-bias blocking voltage of the diode prior to turn on [17].

Reverse Recovery Losses

When a diode is turn off by imposing a reverse-biased voltage, the minority charges stored in the space charge region cannot instantly recover to a blocking state. During this time the diode will actually be able to conduct in the negative direction. This phenomenon is known as reverse recovery. During this transient there occurs a period of overlap between the reverse current and the reverse voltage. The reverse recovery power loss in a diode can be approximated to be as in equation (3.9).

$$P_\mathrm{rr} = \frac{Q_\mathrm{rr} V_\mathrm{R}}{3} \cdot f_\mathrm{sw} \tag{3.9}$$

where P_rr is the reverse recovery power loss and Q_rr is the reverse recovery charge. Schottky diodes and wide bandgap diodes have negligible reverse recovery losses, at the expense of having much higher leakage currents and lower voltage ratings [14].

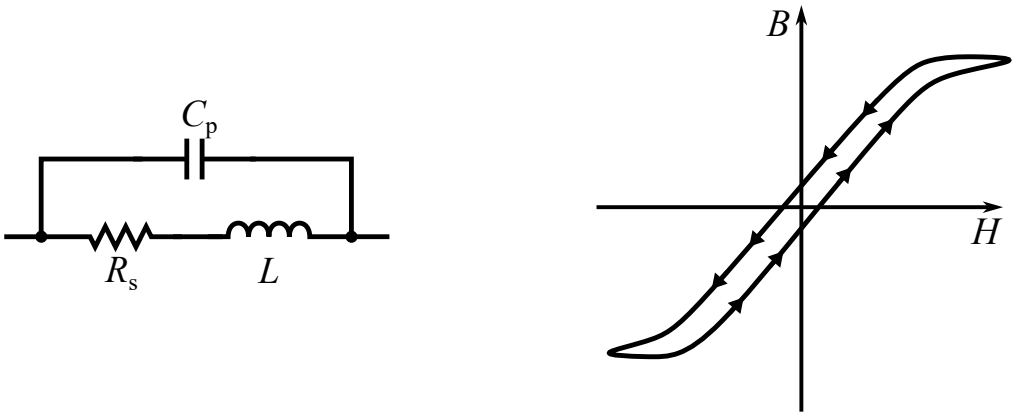
3.1.3 Inductor Power Losses

The behaviour if a real inductor can be modelled with parasitic elements as presented in figure 3.3.

From figure 3.3a it is observed that the inductor has series resistance, R_s, which is attributed from the winding conductor. Thereby the conduction losses of the inductor is given by equation (3.10).

$$P_{\mathrm{L,\ cond}} = {I_\mathrm{L}}^2 \cdot R_\mathrm{s} \tag{3.10}$$

where $P_{\mathrm{L,\ cond}}$ is the conductive losses in the inductor windings and I_L is the RMS value of the winding current. As current flows in the windings, a magnetising force is generated, denoted by H, as presented in figure 3.3b. The H-field is proportional to the magnetic flux density, B, by the core permeability, μ, when the cores is far from saturation. The ripple amplitude of the current in the inductor windings therefore result in a ripple in the magnetic flux density, ΔB. As depicted in the non-ideal BH curve of figure 3.3b, an AC component encloses a hysteresis area, which results in energy loss per unit volume. Hysteresis energy loss in the cores is given



(a) Equivalent inductor circuit. **(b)** Inductor core BH curve.

Figure 3.3 Parasitic elements of a practical inductor [18].

by equation (3.11).

$$E_{\text{hyst}} = (A_c\, l_e) \int_{\text{one cycle}} H \, \mathrm{d}B \tag{3.11}$$

where E_{hyst} is the energy loss during one flux density ripple cycle, A_c is the core cross-section area and l_e is the effective path length of the cores. This type of loss occurs one every switching cycle, therefore the continuous power loss is given from equation (3.12).

$$P_{\text{hyst}} = (A_c\, l_e) f_{\text{sw}} \int_{\text{one cycle}} H \, \mathrm{d}B \tag{3.12}$$

The hysteresis loss is often computed with the appriximation of equation (3.13).

$$P_{\text{hyst}} = k(A_c\, l_e) {f_{\text{sw}}}^a (\Delta B)^d \tag{3.13}$$

where k, a, and d are core dependant parameters [7].

3.1.4 Capacitor Power Losses

An illustration of a non-ideal capacitor is presented in figure 3.4.

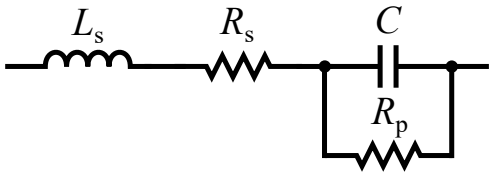


Figure 3.4 Equivalent circuit of a capacitor [18].

Like the inductor, a capacitor has series resistance, R_s, which will result in conduction losses as given in equation (3.14).

$$P_{\text{C, ESR}} = {I_C}^2 \cdot R_s \tag{3.14}$$

where $P_{\text{C, ESR}}$ is the losses due to equivalent series resistance, and I_C is the RMS capacitor current. As presented in figures 2.3c and 2.3d, the current waveforms of the capacitor consists of piecewise trapezoidal segments. Thereby the RMS value can be computed piecewise as presented in equation (3.15).

$$I_C = \sqrt{D \cdot {i_{c,\,\text{ON}}}^2 + (1-D) \cdot {i_{c,\,\text{OFF}}}^2} \tag{3.15}$$

where $i_{c,\,ON}$ and $i_{c,\,OFF}$ is the capacitor current during the interval when the transistor is either ON or OFF, respectively. Additionally R_p represents leakage currents across the capacitor. This values is often very large, and thus the leakage losses can be neglected [14].

3.2 SEPIC Design for Higher Efficiency

Based on the power losses in the SEPIC, presented in section 3.1, it is possible to evaluate how the losses in each component is minimised. For the transistor, there are three main parameters which are component dependant. Firstly, overlap losses are dependant on the rise- and fall times, t_r and t_f. Hence reducing the rise- and fall time, will result in less overlap losses during switching. Secondly, the conduction losses depend on the on-resistance, R_{ds}, which means a transistor with low on-resistance will result in less conduction losses. Lastly, the switching losses can be further reduced by having less output capacitances. This is minimised by selecting a transistor with minimal parasitic output capacitance, C_{oss}. In the diode, forward losses are reduced by selecting a diode with as low a forward voltage, V_f, as possible per equation (3.7). This includes both the junction voltage but also a low junction resistance, R_j. Furthermore, the junction capacitance losses are reduced by selecting a diode with as low junction capacitance as possible per equation (3.8). Lastly it is wise to select a Schottky diode to have negligible reverse recovery losses. In an inductor losses are minimised in two ways. Firstly the series resistance, R_s, must be reduced by having as few turns as possible as observed from equation (3.10). This is achieved by having a core with high permeability, μ, however core saturation must be avoided. Secondly, from equation (3.13) it is clear that hysteresis losses are reduced by selecting a core material with lower losses, but also the flux density ripple, ΔB, must be reduced. For the capacitor losses are simply limited by selecting a capacitor with as equivalent resistance as possible per equation (3.14).

3.2.1 Component Selection for High Efficiency

To quantify the losses in the SEPIC topology, a prototype converter model based on real components is developed. This prototype is described further and also validated experimentall in the following chapter chapter 6. For the transistor a GaN HEMT is selected. GaN transistors achieve very low on-resistance, while at the same time requiring extremely low gate charge to turn on. Therefore, they yield low conduction losses while at the same time they are able to switch on and off in a very short time period [14]. Furthermore, in context of space flight, GaN HEMTs have an additional advantage since they are less prone to degradation from total ionizing dose [19]. For the diode, a Schottky diode is selected due to its low forward voltage and negligible reverse recovery loss.

For the capacitors and inductors, the selection is more constrained. The constraint regarding the inductor is the volume restriction of the module, as specified in table 2.1. Smaller inductors would usually mean that the core would saturate, so a compromise was found with a powder core, which would slightly reach saturation at full current. For the capacitors, electrolytic capacitors are out of the question, as they are not representative in the space environment [5]. Therefore film capacitors were selected, also constrained by its package size.

All selected components for the SEPIC topology are selected to yield the computed values in section 2.3.1. Also the components must be rated for the component stresses presented in sections 2.2.4 and 2.4. Accounting for all these factors, the selected components are presented in table 3.1.

Table 3.1 Selected components for the SEPIC topology.

Component	Parameter	Value / Description
GaN HEMT (EPC2304) [20]	Drain-to-source voltage, V_{ds}	200 V
	On-resistance, R_{ds}	5 mΩ
	Output capacitance, C_{oss}	704 pF (at 100 V)
	Gate charge, Q_g	21 nC
	Package volume, ν	$(5 \times 3 \times 0.7)$mm
Gate Driver (UCC27611) [21]	Gate voltage, V_g	5 V
	Peak Source current, $I_{drv,\,on}$	4 A
	Peak Sink current, $I_{drv,\,off}$	6 A
	Package volume, ν	$(2 \times 2 \times 0.8)$mm
Schottky Diode (V30K202) [22]	Reverse voltage, V_R	200 V
	Forward voltage, V_F	0.53 V (at 5 A)
	Junction Capacitance, C_j	100 pF (at $\geq$ 100 V)
	Package volume, ν	$(6 \times 5 \times 1)$mm
Inductor Core 1 (0074083A7) [23]	Inductance factor, A_L	82 nH/turn^2
	Relative Permeability, μ_r	60
	Saturation flux density, B_{sat}	1.6 T
	Toroid Volume, ν	$(41 \times 41 \times 15)$mm
Inductor Core 2 (0059050A2) [24]	Inductance factor, A_L	56 nH/turn^2
	Relative Permeability, μ_r	125
	Saturation flux density, B_{sat}	1.5 T
	Toroid Volume, ν	$(14 \times 14 \times 6)$mm
C_1 Capacitors (CGA5L3X7T) [25]	Capacitance, C	0.22 µF
	Voltage rating, V_{DC}	250 V
	Eq. series resistance, R_s	5 mΩ (at 100 kHz)
	Package volume, ν	$(3.2 \times 1.6 \times 1.6)$mm
C_2 Capacitors (B32524R3106) [26]	Capacitance, C	10 µF
	Voltage rating, V_{DC}	250 V
	Eq. series resistance, R_s	7.5 mΩ (at 100 kHz)
	Package volume, ν	$(22 \times 31 \times 22)$mm

The components, especially the semiconductors, are selected in view of similar space grade components to ensure a more representative analysis in the context of power supplies for spaceflight. The UCC27611 gate driver is a sophisticated GaN gate driver, with a regulated 5 V gate voltage. This specific component is selected due to its high source/sink current, which will allow the GaN HEMT to turn on and -off rapidly, ideally decreasing switching losses. The data of the inductor core is used to determine the necessary number of turns for each winding to achieve the proper inductance. Further details regarding the inductor design procedure are presented in appendix A.3.

3.3 Python-Based SEPIC Loss Model

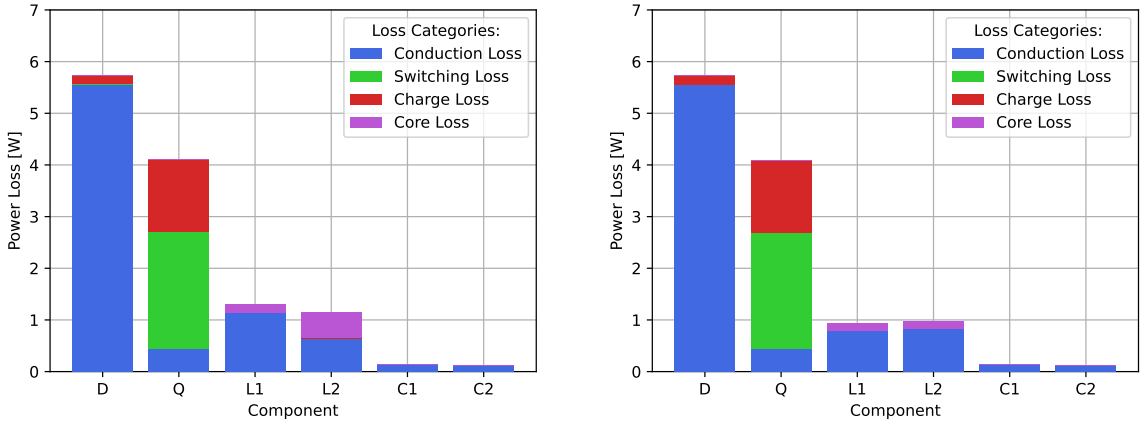
The power loss equations for the SEPIC topology, introduced in section 3.1, are used to model and calculate its expected losses. In this project, this loss model is developed in Python through a function defined as: `P_loss_SEPIC()`. The `P_loss_SEPIC()` function code is presented and described in appendix F.1. The function essentially takes five input: The power level, P, the input- and output voltage, V_{in} and V_{out}, the switching frequency, f_{sw}, and lastly the coupling scheme of the inductors. The function returns the distribution of losses based on the relations of section 3.1. The distribution of losses are analysed in the following subsections. Note that 'charge loss' refers to losses due to either output capacitance, C_{oss} or junction capacitance, C_{j}, in the transistor and diode, respectively.

3.3.1 Component Loss Evaluation Using Python-Based SEPIC Model

In this part the `P_loss_SEPIC()` function is used to analyse the losses of each component, at a number of different operational scenarios. The following analysis will consider a regulated 50 V output voltage in all scenarios. Furthermore, all scenarios are computed at 250 W, to ensure that the magnetic cores are not considerable into their saturated region. The results from all of the following analyses are subsequently summarised in table 3.2.

Estimated Power Loss of the SEPIC at a Lower Input Voltage

In this part of the analysis, the operational scenario revolves around $f_{\text{sw}} = 500\,\text{kHz}$, $P = 250\,\text{W}$, and $V_{\text{in}} = 35\,\text{V}$. This analysis evaluates how the distribution of power losses is affected by using either a coupled- or uncoupled version of the SEPIC topology. The computed distributions of the power losses are presented in figure 3.5.



(a) Uncoupled SEPIC. **(b)** Coupled SEPIC.

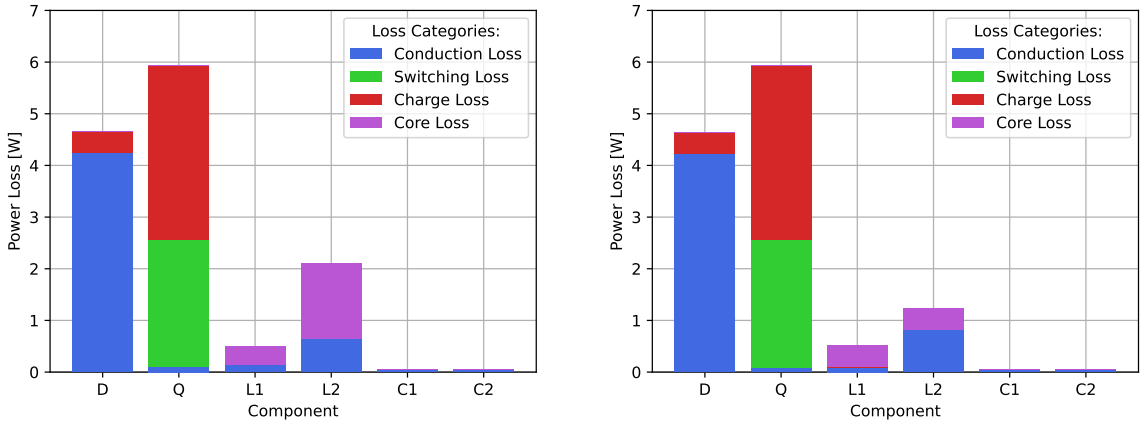
Figure 3.5 Estimated distribution of power losses in each component of the SEPIC using the `P_loss_SEPIC()` Python function for an input voltage of $V_{\text{in}} = 35\,\text{V}$.

In this scenario the total power losses are 12.54 W and 12.01 W, for the uncoupled- and coupled SEPIC, respectively. This implies that the coupled SEPIC exhibits 4.23% lower total power losses relatively to the uncoupled version. By comparing figures 3.5a and 3.5b the only noticeable difference is in the power losses of the two inductors, L_1 and L_2. This is because the mean

current- and voltage values are unchanged, thus the diode, transistor, and capacitors see almost identical RMS values except for the slight change due to increased current ripple in L_2. As the inductance L_2 is 5 times larger in the coupled scenario, the current ripple will also be 5 times smaller as per equation (2.37). The larger current ripple amplitude in L_2 for the uncoupled SEPIC will result in higher core losses due to the increased alternating flux density as presented in equation (3.13). On the other hand, less turns are needed thus the conduction losses on L_2 are slightly decreased, but as there is a neglectable amount of mutual inductance, the number of turns in L_1 must also be increased accordingly.

Estimated Power Loss of the SEPIC at a Higher Input Voltage

In this scenario it is evaluated what the losses are at the highest input voltage of $V_{\text{in}} = 100\,\text{V}$. The other operational parameters are $f_{\text{sw}} = 500\,\text{kHz}$ and $P = 250\,\text{W}$. In this scenario the power losses are distributed as presented in figure 3.6.



(a) Uncoupled SEPIC. **(b)** Coupled SEPIC.

Figure 3.6 Estimated distribution of power losses in each component of the SEPIC for an input voltage of $V_{\text{in}} = 100\,\text{V}$.

In this case the total power losses are 13.29 W and 12.42 W, for the uncoupled- and coupled SEPIC, respectively, thus showing a relative reduction in power losses of 6.55% for the coupled version of the SEPIC at this operational point. At $V_{\text{in}} = 100\,\text{V}$ the input side current magnitude is also decreased by inverse proportion. This means that the conduction losses are decreased, however the losses due to output capacitance are related quadratically to the voltage level, as per equations (3.6) and (3.8). This explain why the transistor losses are increased compared to the $V_{\text{in}} = 35\,\text{V}$ scenario, surpassing the losses of the diode. Furthermore it is seen that the uncoupled SEPIC exhibits considerably more cores losses compared to the coupled SEPIC. This is because of the higher voltage magnitude, meaning that the current ripple amplitude is increased relative to the lower voltage case as given by equation (2.37). For the high-voltage scenario the current ripple reaches $\Delta I_{\text{L2}} = 3.0\,\text{A}$ for the uncoupled case, which is a considerable magnitude for such a relatively small core. For the coupled topology the core losses are also increased in view of the higher input voltage, but not that significantly due to comparably lesser current ripple of 0.6 A.

As observed in figure 3.6 the power losses due to switching and output capacitance are

remarkably large. Thus it is also analysed how the the loss distribution changes due to a switching frequency of $f_{sw} = 250\,\text{kHz}$. The analytical results hereof are documented in appendix B.1. However, in the case of $f_{sw} = 250\,\text{kHz}$ the ripple requirements are no longer fulfilled, and the passive component values are no longer sufficient. This analysis is therefore only relevant in terms of the transistor losses.

Summary of Power Loss Distribution from Python-Based SEPIC Model

utilising the `P_loss_SEPIC()` Python function, the power loss contribution of each component is quantifiable. The power loss amount from each component, subject to the above presented scenarios, is presented in table 3.2. All losses are computed with an output load of 250 W to allow a straightforward comparison.

Table 3.2 Component power loss distribution in the SEPIC with a power throughput of 250 W and a switching frequency of 500 kHz.

Comp.	**Param.**	**Uncoupled**		**Coupled**	
	V_{in}	35 V	100 V	35 V	100 V
GaN HEMT	$P_{Q,\,cond}$	0.44 W	0.10 W	0.44 W	0.10 W
	P_{sw}	2.26 W	2.46 W	2.26 W	2.46 W
	P_{oss}	1.40 W	3.38 W	1.40 W	3.38 W
Schottky	$P_{D,\,cond}$	5.56 W	4.24 W	5.56 W	4.23 W
	P_j	0.17 W	0.41 W	0.17 W	0.41 W
Inductor(s)	$P_{L1,\,cond}$	1.14 W	0.14 W	0.79 W	0.10 W
	$P_{L1,\,hyst}$	0.16 W	0.36 W	0.15 W	0.41 W
	$P_{L2,\,cond}$	0.65 W	0.65 W	0.83 W	0.83 W
	$P_{L2,\,hyst}$	0.49 W	1.46 W	0.15 W	0.41 W
Capacitors	$P_{C1,\,ESR}$	0.14 W	0.05 W	0.14 W	0.05 W
	$P_{C2,\,ESR}$	0.12 W	0.04 W	0.12 W	0.04 W
Sum of losses		12.5 W	13.3 W	12.01 W	12.42 W
Estimated efficiency		95.22%	95.95%	95.42%	95.27%

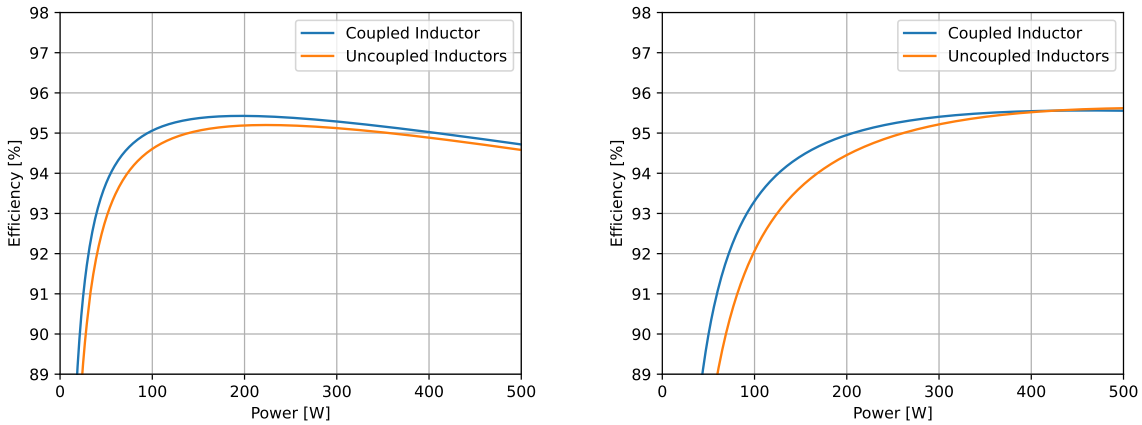
The main take away from the loss distribution at 250 W, is that the coupled version of the SEPIC topology appear to exhibit a slightly higher efficiency, compared to the uncoupled topology. This shift is mainly caused from the increased core losses of L_2, in the attempt to have a small inductor with fewer windings. To mitigate the high core loss of L_2, one would have to increase the inductance of L_2, to yield less current ripple amplitude. Doing so would mean the inductances of L_1 and L_2 would shift further toward each other, at which point it is most likely more beneficial to have the windings on the same core, to reduce both copper losses and volume.

3.3.2 Efficiency Profiles of the SEPIC Across Varying Power Throughput

The analysis of section 3.3.1 revolved around the analytical SEPIC power losses at a fixed power throughout, it being 250 W. However, the power losses are dependent on the current magnitude in a non-linear relationship, as presented in section 3.1. Thereby it is important to also analyse the SEPIC power losses as a function of varying power throughout levels. This is the topic of this subsection, where the `P_loss_SEPIC()` Python function is utilised.

Uncoupled- Versus Coupled Inductor Efficiency Profiles

To analyse how the coupled- and uncoupled versions of the SEPIC perform, each scenario is evaluated across the entire power range. The results hereof are presented in figure 3.7 at a constant switching frequency of 500 kHz.



(a) $V_{\text{in}} = 35\,\text{V}$ scenario. **(b)** $V_{\text{in}} = 100\,\text{V}$ scenario.

Figure 3.7 Efficiency profiles of uncoupled- and coupled versions of the SEPIC.

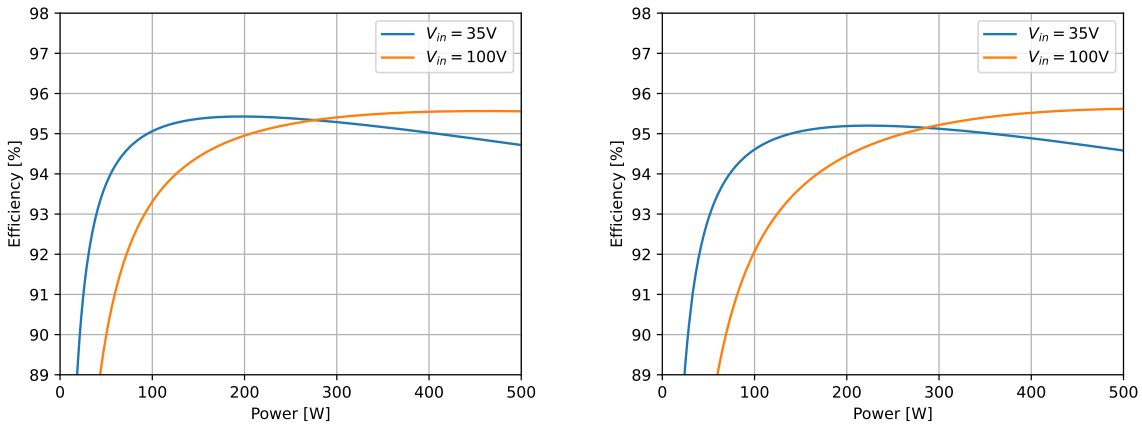
For the $V_{\text{in}} = 35\,\text{V}$ case, it is observed that the coupled inductor has superior efficiency across the entire efficiency range. On the other hand, the coupled version in the $V_{\text{in}} = 100\,\text{V}$ case has a superior efficiency at lower power levels, while close to maximum power it becomes more efficient for the uncoupled version. This switch is likely caused by the fact that the inductor core of L_2 is driven fairly far out into its saturation, thereby meaning that the increased ripple current amplitude will not cause any further ripple in the magnetic flux density, B. The dynamics of saturation are not thoroughly implemented in the `P_loss_SEPIC()`, and thus it is reasonable to doubt this result. This point is further discussed in chapter 7. Nonetheless, the average efficiency improvement of the coupled SEPIC compared to the uncoupled version across the full power range is $0.43\%_{\text{pp}}$ and $0.87\%_{\text{pp}}$, for the $V_{\text{in}} = 35\,\text{V}$ and $V_{\text{in}} = 100\,\text{V}$ scenarios, respectively. This suggest that the coupled version of the SEPIC exhibits the highest efficiency, analytically. The peak efficiency of each scenario, along with the power level at which it occurs, is presented in table 3.3.

Table 3.3 Peak efficiency points on the power curve of the SEPIC with uncoupled- and coupled inductors.

Parameter	**Uncoupled**		**Coupled**	
Input voltage, V_{in}	35 V	100 V	35 V	100 V
Peak efficiency, $\hat{\eta}$	95.20%	95.62%	95.42%	95.56%
Power level, P	224 W	500 W	197 W	460 W

Efficiency Profile of SEPIC at Various Input Voltage Levels

From table 3.3 it is observed that for higher input voltage levels, it appears that the power level, P, at which the peak efficiency, $\hat{\eta}$, occurs is shifted toward higher levels. This is visualised for the SEPIC with uncoupled- and coupled inductors separately, as presented in figure 3.8.



(a) Uncoupled inductors scenario.

(b) Coupled inductors scenario.

Figure 3.8 Efficiency profiles of the uncoupled- and coupled versions of the SEPIC at different input voltages.

From figures 3.8a and 3.8b it is evident that for a higher input voltage, then the point of peak efficiency, $\hat{\eta}$, is shifted toward higher power levels. Some losses, such as losses due to output capacitance, are current independent. Thus at low power output, but fixed voltage, these losses will dominate. As current is increased, switching losses and conduction losses begin to impact the efficiency. The optimum point occurs when the dominating power losses transition from switching losses to conduction losses. This occurs because conduction losses are quadratically proportional to the current, whereas the switching losses are linearly proportional to the current, as presented in section 3.1. For the scenario presented in figure 3.8 the crossover at which the $V_{\text{in}} = 100\,\text{V}$ scenario begins to exhibit higher efficiency than the $V_{\text{in}} = 35\,\text{V}$ scenario occurs at $P = 286\,\text{W}$ and $P = 277\,\text{W}$ for the uncoupled- and coupled SEPIC version, respectively. The points at which the efficiency peak occurs are also presented in table 3.3.

The computed efficiency plots of the SEPIC operating at a switching frequency of 250 kHz are also presented in appendix B.2.2. Here the analytical model reveals a peak efficiency of $\hat{\eta} = 96.31\%$.

3.4 Synchronous Rectification of the SEPIC Topology

From the distribution of power losses in the SEPIC topology, presented in section 3.3.1, it is clear that the diode contribute a significant portion of the total losses due to its conduction losses, e.g. see figure 3.5a. This raises the question of whether the diode can be replaced by a complimentary transistor, $\bar{Q}_1$, thereby further reducing power losses. A schematic of this concept is presented in figure 3.9.

Driving the master transistor, Q_1, is straightforward as the source is referenced to ground. But driving the complimentary transistor, $\bar{Q}_1$, is not as simple because it is a high-side transistor. $\bar{Q}_1$ has the source connected to node 2, marked in figure 3.9, thus a positive voltage beyond the gate threshold voltage must be generated in reference to node 2 to turn the GaN HEMT on. The recommended gate-to-source voltage of the EPC2304 is 5 V.

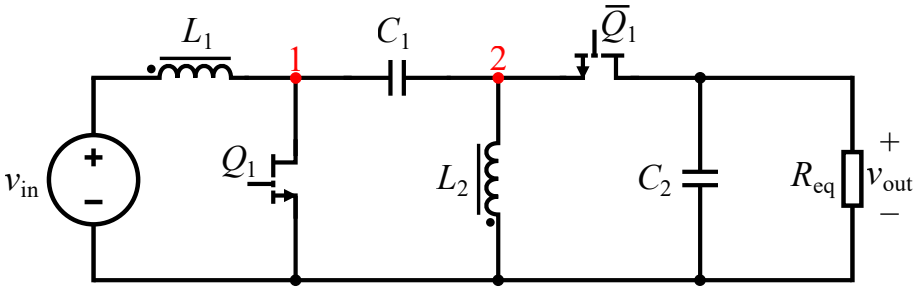


Figure 3.9 Schematic of synchronous SEPIC with GaN HEMTs and coupled inductors.

A key remark is that the output voltage, V_{out}, can be considered to remain constant, while node 2 alternates between $-V_{in}$ and $+V_{out}$, as depicted in figure 2.3b. Thereby the drain-to-source voltage of the high-side GaN HEMT, $\bar{Q}_1$, momentarily blocks $V_{DS} = V_{out} - (-V_{in})$. In the extreme scenario of: $V_{out} = 50\,V$ and $V_{in} = 100\,V$, the peak drain-to-source voltage is therefore: $V_{DS} = 150\,V$. Based on the aforementioned conditions some possible solutions are presented and discussed in the following subsections.

3.4.1 Modified Bootstrap Circuit

A typical bootstrap circuitry will not work for the high-side transistor in the SEPIC. This is because the source node never become referenced to ground [12]. Therefore the bootstrap circuit must be modified, as presented in figure 3.10. A zener diode and a parallel capacitor, C_{hs}, is used to clamp the supply voltage at 5 V, with a resistor to block the residual drain-to-source voltage. In the case of $V_{DS} = 150\,V$ the stress on the high-side resistor, R_{hs}, becomes relatively high which results in considerable losses. However, in lower voltage SEPICs this might be perfectly resonable, while remaining a fairly simply solution.

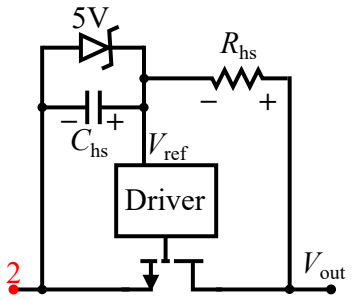


Figure 3.10 Modified bootstrap circuit for high-side supply in SEPIC.

3.4.2 Isolated DC/DC Supply

An auxiliary isolated DC/DC converter, such as a regulated flyback converter, can be used to generate a floating supply voltage of 5 V [12]. While this solution would theoretically yield less power loss than the solution presented in section 3.4.1, it also comes at the expense of added complexity. Furthermore, for fast switching transistors, such as a GaN HEMT, the switching time is in the order of a few nanoseconds causing very high common-mode dv/dt. Therefore even a tiny amount of inter-winding capacitance in the flyback transformer can result in damaging transient current.

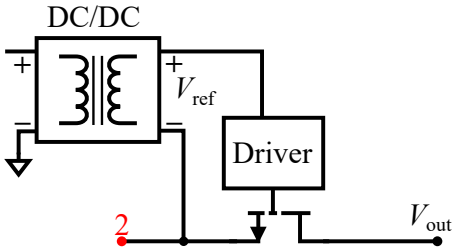


Figure 3.11 Isolated DC/DC for high-side supply in SEPIC.

3.4.3 Pulse Transformer

A high-frequency transformer can directly drive the high-side transistor, as shown in figure 3.12 [12]. Since the transformer passes only the AC component, a series diode ensures positive gate pulses, while a zener diode clamps the gate-source voltage to 5 V. However, as the duty cycle increases, the positive AC peak may fall below the threshold voltage. As in section 3.4.2, inter-winding capacitance can also cause harmful transients in the Pulse Width Modulation (PWM) transformer. Additional circuitry is also needed to prevent core saturation. Due to the fragile gate structure of GaN HEMTs, the PWM transformer approach may not be suitable [14].

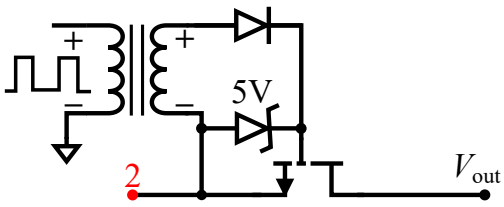


Figure 3.12 PWM transformer for high-side driving in SEPIC.

3.4.4 Floating DC/DC Supply

A floating non-isolated DC/DC converter can also be used to generate the 5 V reference, as presented in figure 3.13. This concept is developed based on the fact that the flying capacitor, C_1, in the SEPIC topology on average carries the input voltage. Thereby a floating step-down converter can use the capacitor as it's input voltage, and step-down the voltage to 5 V. In this way, the common reference point of the transistor and the step-down regulator is the same point. C_1 must be large enough to carry a somewhat stable voltage to ensure proper regulation, and the output voltage must be very stable. Furthermore, for high voltage SEPICs, the step-down ratio can be very high, especially when driving the gate of a GaN HEMT.

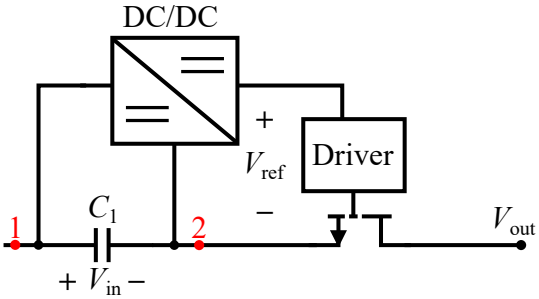


Figure 3.13 Floating DC/DC converter for high-side supply in SEPIC.

In summary, there exists several possible solutions to drive the high-side transistor in a synchronous SEPIC. However, the available options are either inefficient or relatively complex. This raises the question of whether the synchronous version of the SEPIC is truly advantageous within the operational range of this project. Furthermore, the added complexity may compromise reliability. Given the limited timeline of this project, developing a synchronous prototype is regarded unrealistic; therefore, the diode-based SEPIC topology will be considered for the remainder of the project.

4 Control of the SEPIC Topology

Evaluating the control loop is essential in assessing the feasibility of the SEPIC topology within the APR module. This is the scope of this chapter. MPPT of the PV arrays is not addressed, effectively emulating a scenario where the battery pack is fully charged or disconnected.

4.1 Control Loop Architecture

The APR module consists of three SEPICs in parallel, as presented in figure 2.1. This implies that the control scheme revolves around three SEPICs in parallel, regulating the same output voltage. To achieve full power throughput, the converters must share the power among them, indicating that the module is operated with hot redundancy. Having three DC/DC converters operated simultaneously in parallel like that, means that voltage mode control is not feasible. Therefore it is necessary to implement each SEPIC with current-mode control [7]. The APR module with three parallel SEPICs in current-mode control is illustrated in figure 4.1.

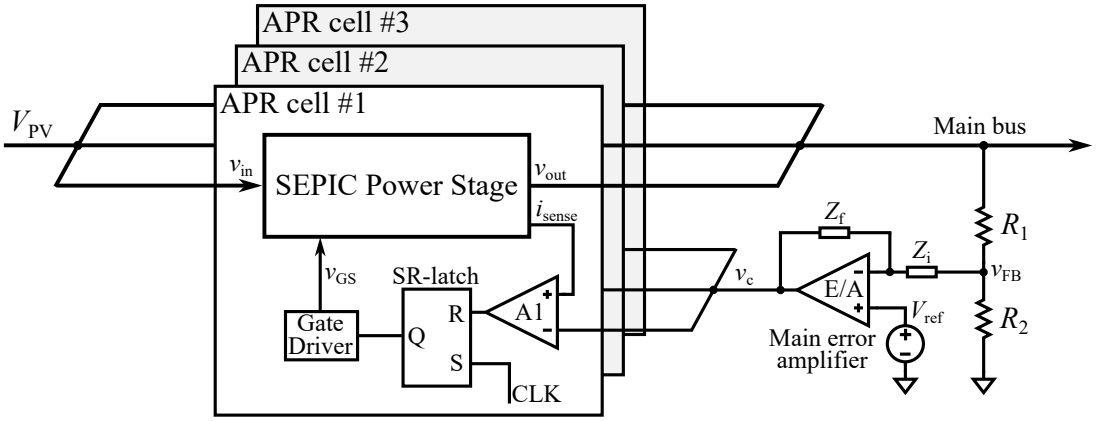


Figure 4.1 Three parallel SEPICs with peak current-mode control regulating the main bus [14].

In figure 4.1 it is observed that each APR cell has a local current-control scheme, while there is a global Main Error Amplifier (MEA). This architecture means that each APR cell is regulated from the same control voltage, v_c, resulting in equal current sharing among the three SEPICs. In practice, a majority voting logic is implemented around the MEA to eliminate a single point failure mode [5].

4.1.1 Peak Current-Mode Control of the SEPIC

The general rationale behind peak current-mode control, is that the peak current of the power stage is the control variable. In the context of figure 4.1, peak current-mode control is implemented in the comparator A1 and the associated SR flip-flip, where the regulated current is denoted as i_{sense}. Technically i_{sense} is a voltage, since it is sensed by a current sensor. The control waveforms in figure 4.2 illustrates the operational principle of this type of peak current-mode control.

When the sensed current, i_{sense}, reaches the control voltage, v_{c}, the comparator, A1, is pulled to the positive supply rail. The high pulse from the comparator triggers the reset pin of the SR flip-flip, effectively pulling the gate voltage, v_{GS}, low. After some time, the clock signal, CLK, will trigger the set pin of the SR flip-flop, thus pulling v_{GS} high. As the transistor is turned on, the inductor current increases, as depicted in figure 2.6b, until it i_{sense} reaches the reference control voltage, v_{c}, initiating a new cycle. This also implies that the frequency of the CLK signal dictates the switching frequency of the transistor.

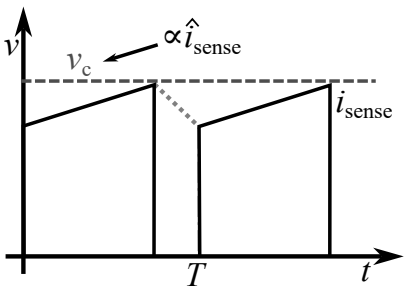


Figure 4.2 Peak current-mode control of an inductive current, i_{sense}.

For the SEPIC, the question is then where the current sensor should be located. Three candidate locations, denoted with 1, 2, and 3, are presented in figure 4.3.

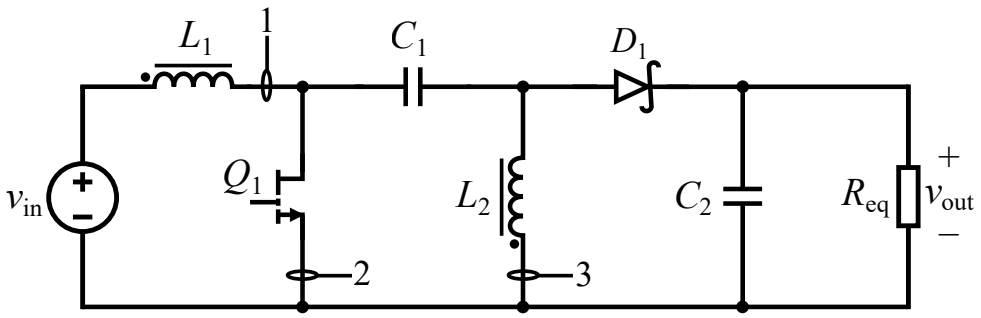


Figure 4.3 Candidate current sensor location for peak current-mode control in the SEPIC topology.

In location 1, the measured current is the input current, or i_{L1}, which is similar to current control of a boost converter. However, this point is switched in and out of very high common mode voltage levels, which means it is not a straightforward solution. Location 2 replicates the typical peak current-mode control of any conventional converter, where it is typical to sense the transistor current. However for the SEPIC, the transistor current is the sum of i_{L1} and i_{L2}, complicating its application in peak current-mode control. In location 3 the output current is sensed, or i_{L2}, which is similar to how a buck converter is controlled in peak current-mode control. If the output current can be regulated like this, the voltage plant is decreased to a first order transfer function, allowing nice system response and damping [14]. Both location 2 and 3 are at very low common mode voltage, and thus are more practical than location 1.

However, location 3 presents a critical issue: a state may occur in which the transistor Q_1 becomes latched high, causing the full current to flow through i_{L1}. In this condition, i_{L2} gets stuck low and never ramps up, preventing the reset signal from being triggered. As a result, the transistor remains on indefinitely, effectively shorting the input and allowing the current through the switch to increase uncontrollably. Therefore, location 2 is seen as the only viable option for peak current-mode control in the SEPIC topology. The small-signal dynamics of the SEPIC when regulated in this manner is covered in the following section 4.2.

4.2 Small-Signal Dynamics of the SEPIC Topology

The small-signal state-space model of the SEPIC topology is derived by linearizing the averaged equations presented in section 2.2.3. This is achieved by solving for the small-signal perturbation states, as presented in equations (4.1) and (4.2).

$$\frac{\mathrm{d}\tilde{\mathbf{x}}}{\mathrm{d}t} = \mathbf{K}^{-1}\left[\mathbf{A}\tilde{\mathbf{x}} + \mathbf{B}\tilde{\mathbf{u}} + \{(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}\}\ \tilde{d}\right] \tag{4.1}$$

$$\tilde{\mathbf{y}} = \mathbf{C}\tilde{\mathbf{x}} + \{(\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X}\}\ \tilde{d} \tag{4.2}$$

where $\mathbf{K}$ is the coupling matrix which is simply an alternative way of expressing the system matrix, $\mathbf{A}$, ultimately allowing mutual inductances to be implemented in the small signal model [14]. As $\tilde{\mathbf{u}}$ is assumed to 0, the second term of equation (4.1) is eliminated. This effectively means that the small-signal duty cycle, $\tilde{d}$ has become the system input. The resulting linearised small-signal state space models are therefore derived as presented equations (4.3) and (4.4), for the uncoupled- and coupled version of the SEPIC topology, respectively.

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix}\tilde{i}_{\mathrm{L1}}\\ \tilde{i}_{\mathrm{L2}}\\ \tilde{v}_{\mathrm{C1}}\\ \tilde{v}_{\mathrm{C2}}\end{bmatrix} = \begin{bmatrix}0 & 0 & -\frac{1-D}{L_1} & -\frac{1-D}{L_1}\\ 0 & 0 & \frac{D}{L_2} & -\frac{1-D}{L_2}\\ \frac{1-D}{C_1} & -\frac{D}{C_1} & 0 & 0\\ \frac{1-D}{C_2} & \frac{1-D}{C_2} & 0 & -\frac{1}{C_2 R_{\mathrm{eq}}}\end{bmatrix}\begin{bmatrix}\tilde{i}_{\mathrm{L1}}\\ \tilde{i}_{\mathrm{L2}}\\ \tilde{v}_{\mathrm{C1}}\\ \tilde{v}_{\mathrm{C2}}\end{bmatrix} + \begin{bmatrix}\frac{V_{\mathrm{in}}}{(1-D)L_1}\\ \frac{V_{\mathrm{in}}}{(1-D)L_2}\\ -\frac{DV_{\mathrm{in}}}{(1-D)^2 C_1 R_{\mathrm{eq}}}\\ -\frac{DV_{\mathrm{in}}}{(1-D)^2 C_2 R_{\mathrm{eq}}}\end{bmatrix}\tilde{d} \tag{4.3}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix}\tilde{i}_{\mathrm{L1}}\\ \tilde{i}_{\mathrm{L2}}\\ \tilde{v}_{\mathrm{C1}}\\ \tilde{v}_{\mathrm{C2}}\end{bmatrix} = \begin{bmatrix}0 & 0 & \frac{(1-D)L_2+DM}{M^2-L_1L_2} & \frac{(1-D)(L_2-M)}{M^2-L_1L_2}\\ 0 & 0 & \frac{D(M-L_1)-M}{M^2-L_1L_2} & \frac{D(M-L_1)+(L_1-M)}{M^2-L_1L_2}\\ \frac{1-D}{C_1} & -\frac{D}{C_1} & 0 & 0\\ \frac{1-D}{C_2} & \frac{1-D}{C_2} & 0 & -\frac{1}{C_2 R_{\mathrm{eq}}}\end{bmatrix}\begin{bmatrix}\tilde{i}_{\mathrm{L1}}\\ \tilde{i}_{\mathrm{L2}}\\ \tilde{v}_{\mathrm{C1}}\\ \tilde{v}_{\mathrm{C2}}\end{bmatrix} + \begin{bmatrix}\frac{(L_2-M)V_{\mathrm{in}}}{(1-D)(L_1L_2-M^2)}\\ \frac{(L_1-M)V_{\mathrm{in}}}{(1-D)(L_1L_2-M^2)}\\ -\frac{DV_{\mathrm{in}}}{(1-D)^2 C_1 R_{\mathrm{eq}}}\\ -\frac{DV_{\mathrm{in}}}{(1-D)^2 C_2 R_{\mathrm{eq}}}\end{bmatrix}\tilde{d} \tag{4.4}$$

The eigenvalues, λ, and the corresponding damping, ζ, of the uncoupled-, and coupled state-space models, using the parameters of table 2.4, are presented in table 4.1.

Table 4.1 Eigenvalues of the uncoupled- and coupled small-signal state-space models.

Uncoupled SEPIC				**Coupled SEPIC**			
Re(λ)	Im(λ)	ζ	Frequency	Re(λ)	Im(λ)	ζ	Frequency
-1938	$\pm j10\,030$	0.1897	1.62 kHz	-2125	$\pm j9076$	0.228	1.48 kHz
-187	$\pm j43\,010$	0.004348	6.85 kHz	-0.0003241	$\pm j298\,800$	1.09×10^{-9}	47.56 kHz

From table 4.1, it can be observed that both small-signal models exhibit two pairs of complex-conjugate eigenvalues: one associated with low-frequency and the other with high-frequency. The dominant pole-pair (low-frequency) of the coupled version has comparably higher damping relatively to the uncoupled version. The high frequency pole-pair of the coupled SEPIC is shifted to much higher value than the uncoupled version, but the damping is on the other hand also considerably low. This means that case must be taken regarding these high frequency poles, especially ensuring that they don't result in high-frequency oscillations. Nonetheless, it is seen that the dominant eigenvalue-pair in the coupled version of the SEPIC is better damped than that of the uncoupled version. This is seen to have a significant effect on transient dynamics, as presented in appendix C.4, where it is seen that the coupled SEPIC appears to exhibit superior transient relative to the uncoupled version. The small-signal system, eigenvalues, and responses are computed using a small-signal python script, which is further documented in appendix F.2.

4.2.1 Closed Loop Control of SEPIC

With the developed small-signal state space model, the transient dynamics of the SEPIC are modelled. With this, the control loop dynamics can be evaluated and a compensator can be designed to obtain a stable closed-loop system. Based on the peak current-mode control concept presented in figure 4.1, the block diagram of figure 4.4 is derived.

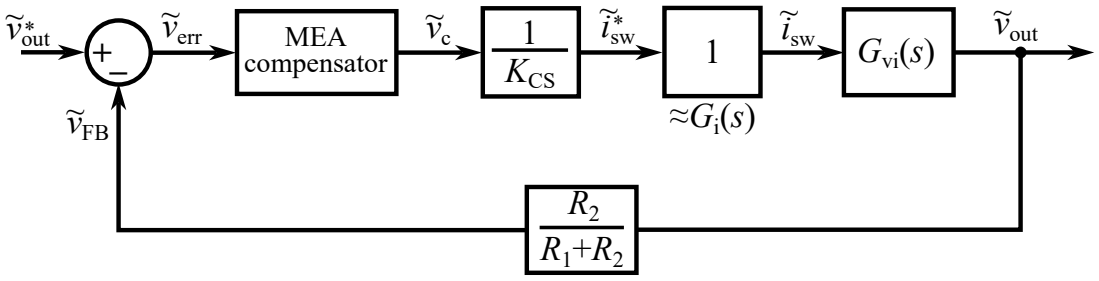


Figure 4.4 Closed-loop block diagram representation of the SEPIC in peak current-mode control

From figure 4.4 it is clear that the peak current-mode control loop consists of two cascaded control loops. Firstly there is the inner current control loop, $G_{\mathrm{i}}(s)$ and then there is the outer voltage control loop, G_{vi}. The control voltage, v_{c}, is directly proportional to the transistor current reference, $\tilde{i}^*_{\mathrm{sw}}$, by the gain of the current sensor K_{CS}. The inner loop is simplified to a unity gain. This simplification is fair because the inner loop regulates every switching cycle, and is therefore expected to have much higher bandwidth than the outer voltage control loop. The input-to-output transfer function of each state is obtained with equation (4.5).

$$G(s) = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} \tag{4.5}$$

where $G(s)$ is the input-to-output transfer functions, and $\mathbf{I}$ is the identity matrix [27]. Using equation (4.5) and the component values from table 2.4, the control-to-output transfer function for the coupled SEPIC at $V_{\mathrm{in}} = 35\,\mathrm{V}$ and $P = 500\,\mathrm{W}$ is computed from the state-space model in equation (4.4), resulting in equations (4.6), (4.7) and (4.8).

$$G_{\mathrm{vd}}(s) = \frac{\tilde{v}_{\mathrm{out}}}{\tilde{d}} = \frac{-1.032 \times 10^6 s^3 + 1.794 \times 10^{10} s^2 - 9.223 \times 10^{16} s + 1.602 \times 10^{21}}{s^4 + 8500 s^3 + 8.938 \times 10^{10} s^2 + 7.59 \times 10^{14} s + 7.759 \times 10^{18}} \tag{4.6}$$

$$G_{\mathrm{id1}}(s) = \frac{\tilde{i}_{\mathrm{L1}}}{\tilde{d}} = \frac{5.126 \times 10^6 s^3 + 2.173 \times 10^{12} s^2 + 7.225 \times 10^{16} s + 9.152 \times 10^{20}}{s^4 + 8500 s^3 + 8.938 \times 10^{10} s^2 + 7.59 \times 10^{14} s + 7.759 \times 10^{18}} \tag{4.7}$$

$$G_{\mathrm{id2}}(s) = \frac{\tilde{i}_{\mathrm{L2}}}{\tilde{d}} = \frac{5.126 \times 10^6 s^3 - 2.163 \times 10^{12} s^2 1.924 \times 10^{16} s + 3.203 \times 10^{20}}{s^4 + 8500 s^3 + 8.938 \times 10^{10} s^2 + 7.59 \times 10^{14} s + 7.759 \times 10^{18}} \tag{4.8}$$

where equation (4.6) is the power-stage transfer function in voltage control mode. As proven in section 2.4 the current in the transistor is given as $i_{\mathrm{sw}} = i_{\mathrm{L1}} + i_{\mathrm{L2}}$, thus resulting in equation (4.9).

$$G_{\mathrm{id}}(s) = G_{\mathrm{id1}}(s) + G_{\mathrm{id2}}(s) = \frac{\tilde{i}_{\mathrm{L1}} + \tilde{i}_{\mathrm{L2}}}{\tilde{d}} = \frac{\tilde{i}_{\mathrm{sw}}}{\tilde{d}} \tag{4.9}$$

where $G_{\mathrm{id}}(s)$ is analogous to the power stage transfer function of the inner current loop, $G_{\mathrm{i}}(s)$, as observed in figure 4.4. By combining equations (4.6) and (4.9) the outer loop power stage transfer function is derived as presented below, resulting in equation (4.10).

$$G_{\mathrm{vi}}(s) = \frac{\frac{\tilde{v}_{\mathrm{out}}}{\tilde{d}}}{\frac{\tilde{i}_{\mathrm{sw}}}{\tilde{d}}} = \frac{G_{\mathrm{vd}}(s)}{G_{\mathrm{id}}(s)} = \frac{\tilde{v}_{\mathrm{out}}}{\tilde{i}_{\mathrm{sw}}}$$

$$G_{\mathrm{vi}}(s) = \frac{\tilde{i}_{\mathrm{sw}}}{\tilde{d}} = \frac{-1.007 s^3 + 1.75 \times 10^4 s^2 - 9.00 \times 10^{10} s + 1.56 \times 10^{15}}{s^3 + 9748 s^2 + 8.93 \times 10^{10} s + 1.21 \times 10^{15}} \tag{4.10}$$

A further frequency-domain analysis of the power stage transfer functions of both the uncoupled- and coupled version of the SEPIC, subject to various operational scenarios, is presented in appendix C.1. From the frequency-domain analysis of appendix C.1 it is found that the SEPIC power stage consist of zeros in the Right-Hand Plane (RHP). Finally from figure 4.4 the uncompensated open-loop transfer function in peak current-mode control is given as presented in equation (4.11).

$$G_{\mathrm{ol}}(s) = \frac{\tilde{v}_{\mathrm{FB}}}{\tilde{v}_{\mathrm{c}}} = \frac{1}{K_{\mathrm{CS}}} \frac{R_2}{R_1 + R_2} G_{\mathrm{vi}}(s) \tag{4.11}$$

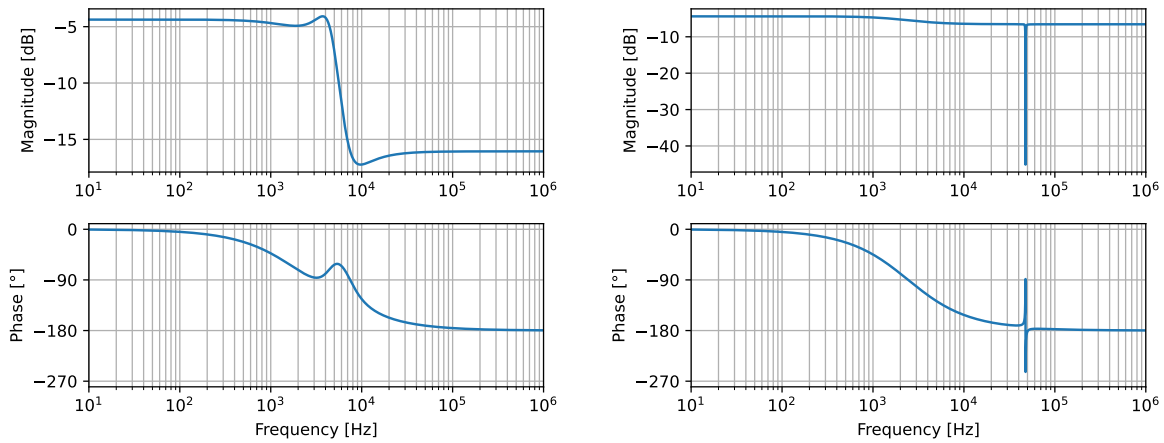
Then there is but to obtain the values of K_{CS}, R_1, and R_2. Here it is relevant to know what the reference voltage of the MEA operational-amplifier is. Furthermore, in peak current-mode control the positive supply voltage of the error amplifier also acts as a current limit threshold of the switch current reference, which is a beneficial feature of the peak current-mode control concept. Therefore it is important to know the voltage levels of the amplifiers in the control scheme. It is assumed that the control scheme is based on the military grade UC1843 PWM controller by Texas Instruments [28]. In the UC1843 the control voltage, v_{c}, gets clamped at maximum 1 V, which can be used to set the current limit. The current limit is selected as 28 A which is slightly more than full load current of 24.3 A as specified through table 2.3 and figure 2.6b. This leads to the necessary current sensor gain of equation (4.12).

$$K_{\mathrm{CS}} = \frac{1\,\mathrm{V}}{28\,\mathrm{A}} = 35.7\,\frac{\mathrm{mV}}{\mathrm{A}} \Leftrightarrow 35.7\,\mathrm{m\Omega} \tag{4.12}$$

Upon further assessment it is found that a shunt resistor of 35.7 mΩ would yield harmful power dissipation in the resistor. Therefore a current sense transformer is used to achieve the same gain, but with acceptable losses, the design of which is further documented in appendix C.2. Additionally the UC1843 has a gain of $\frac{1}{3}$ after the internal error amplifier, that is: $K_{\mathrm{cont}} = \frac{1}{3}\frac{\mathrm{V}}{\mathrm{V}}$. Finally the internal reference to the error amplifier in the UC1843 is 2.5 V, therefore a resistive voltage divider based on $R_2 = 10\,\mathrm{k\Omega}$ that yields $v_{\mathrm{FB}} = 2.5\,\mathrm{V}$ at $v_{\mathrm{out}} = 50\,\mathrm{V}$, is designed as presented in equation (4.13).

$$R_1 = \frac{V_{\mathrm{out}} - V_{\mathrm{FB}}}{V_{\mathrm{FB}}} R_2 = \frac{50\,\mathrm{V} - 2.5\,\mathrm{V}}{2.5\,\mathrm{V}} \cdot 10\,\mathrm{k\Omega} = 190\,\mathrm{k\Omega} \tag{4.13}$$

Using $K_{\mathrm{cont}} = \frac{1}{3}\frac{\mathrm{V}}{\mathrm{V}}$, $K_{\mathrm{CS}} = 35.7\,\frac{\mathrm{mV}}{\mathrm{A}}$, $R_1 = 190\,\mathrm{k\Omega}$, and $R_2 = 10\,\mathrm{k\Omega}$ the uncompensated open-loop transfer function is computed by equation (4.11), where the resulting frequency response of the uncoupled- and coupled versions for $G_{\mathrm{vi}}(s)$ is presented in figure 4.5. The considered operational parameters are still $P = 500\,\mathrm{W}$ and $V_{\mathrm{in}} = 35\,\mathrm{V}$.



(a) $G_{\mathrm{vi}}(s)$ of uncoupled SEPIC. **(b)** $G_{\mathrm{vi}}(s)$ of coupled SEPIC.

Figure 4.5 Uncompensated open-loop transfer functions of the SEPIC power stage in current-mode control.

Comparing figures 4.5a and 4.5b it is seen that the uncoupled dynamics are fairly smooth in the low frequency range, whereas the uncoupled dynamics are quite uneven. However the uncoupled transfer function has the very poorly damped resonance occurring at 47.56 kHz, which in this case is a complex-conjugate zero and complex-conjugate pole located very close to each other. For an ideally coupled SEPIC this complex-conjugate pole-zero pair will cancel. The pole and zero locations are thoroughly covered in appendix C.1.

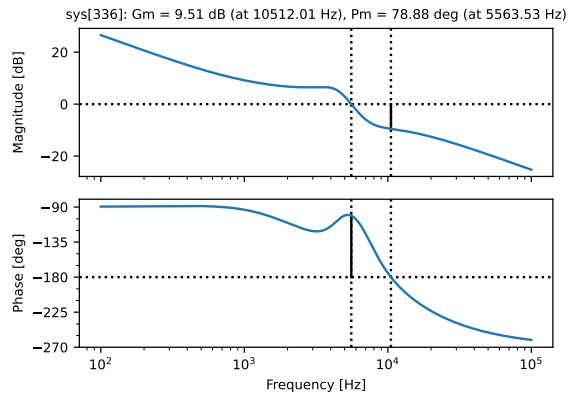
Per the ECSS standard the control loop requirements are: GM ≥ 6 dB, PM $\geq 60°$, and that any transient in the main bus voltage due to a 50% load step should be $\leq 1\%$ of the nominal bus voltage. Moreover, the ECSS standard indirectly required control loop bandwidth to be in the range of $f_{\mathrm{BW}} = [100\,\mathrm{Hz}, 10\,\mathrm{kHz}]$ [6]. To fulfil these requirements a type-II compensator is used to compensate the loop characteristics while ensuring a relatively high bandwidth [7]. The type-II compensator transfer function is presented in equation (4.14).

$$G_{\mathrm{c}}(s) = K\frac{(s + 2\pi f_{\mathrm{z}})}{s(s + 2\pi f_{\mathrm{p}})} \tag{4.14}$$

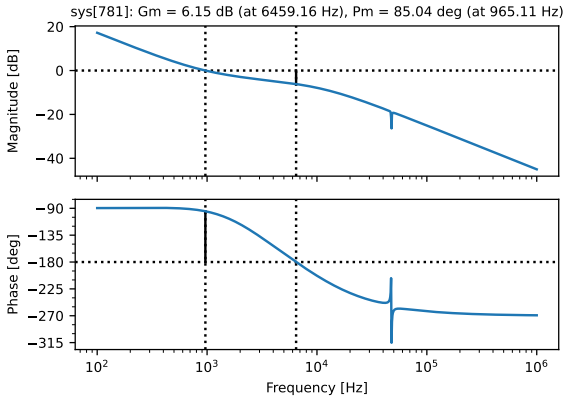
where K is the controller gain, f_{z} is the frequency of the zero, and f_{p} is the frequency of the pole. The type-II compensator is used to amplify the low frequency band to eliminate steady-state error, and also the real pole is used to attenuate the high frequency content. The designed compensators and their resulting control loop dynamics are presented in table 4.2, and the compensated open-loop frequency response is presented in figure 4.6.

Table 4.2 Compensated control loop parameters for the uncoupled- and coupled SEPIC topology.

Parameter	Uncoupled SEPIC	Coupled SEPIC
Controller gain, K	$220 \times 10^3\ \frac{\mathrm{V}}{\mathrm{V}}$	$75 \times 10^3\ \frac{\mathrm{V}}{\mathrm{V}}$
Zero frequency, f_{z}	1.0 kHz	1.0 kHz
Pole frequency, f_{p}	10.0 kHz	10.0 kHz
Gain margin, GM	9.5 dB	6.2 dB
Phase margin, PM	78.9°	85.0°
Bandwidth, f_{b}	6.1 kHz	8.9 kHz



(a) Compensated $G_{\mathrm{ol}}(s)$ of uncoupled SEPIC.



(b) Compensated $G_{\mathrm{ol}}(s)$ of coupled SEPIC.

Figure 4.6 Compensated open-loop transfer functions of the SEPIC in current-mode control.

From the compensated control loop parameters presented in table 4.2 it is seen that both uncoupled- and coupled versions of the SEPIC is capable of fulfilling the requirements of the ECSS standard. Additionally it is seen that a relatively high bandwidth in the range of 6 to 9 kHz is achieved. Also for the compensated open-loop dynamics of figure 4.6b it is seen that the high-frequency complex-conjugate pole-zero pair is

sufficiently attenuated. The type-II compensator design and realisation is documented in appendix C.3. Moreover the small-signal dynamics are evaluated experimentally as described in figure C.11. The experimental response indicated that the laboratory prototype converter had a higher level of damping, perhaps as a consequence of resistances in the setup.

In this section the current-mode control dynamics of the SEPIC are demonstrated. In general it is observed that the coupled version of the SEPIC has superior dynamics in the low frequency band, whereas the coupled version does not suffer from the undamped complex conjugate pole-zero pair at high frequency. Nonetheless it is proven that both control loops can be compensated accordingly with a type-II compensator, yielding control loop dynamics which fulfil the stability margin requirements of the ECSS standard for both the uncoupled- and coupled version of the SEPIC topology.

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5 Simulations

This chapter revolves around the simulations developed during this project. The simulations serve to validate the analytical modelling and design procedures. For this project two main categories of simulations were developed: Firstly there are the open-loop simulations, and then there are the closed-loop simulations. Each of them are presented in the following sections of this chapter. The simulation software used in this project is LTspice.

5.1 Open-loop Simulations of the SEPIC Topology

To evaluate the steady-state analytical operation of the SEPIC, an open-loop simulation is developed with ideal components, as presented in figure 5.1. The values of the passives are based on those derived in table 2.4.

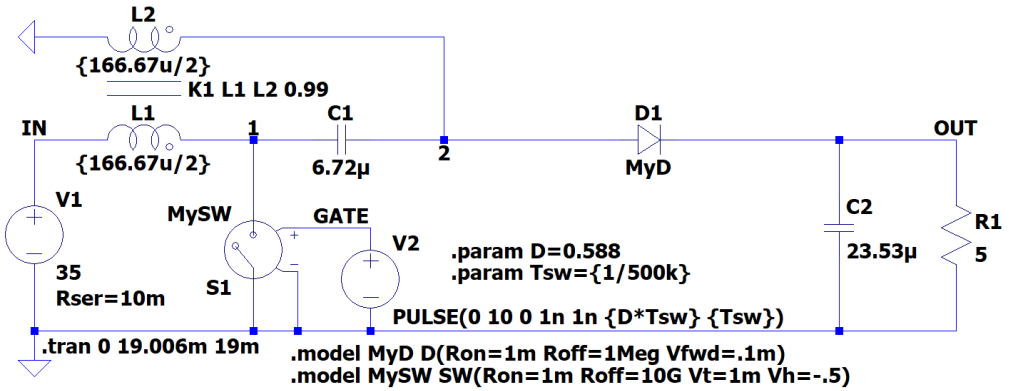
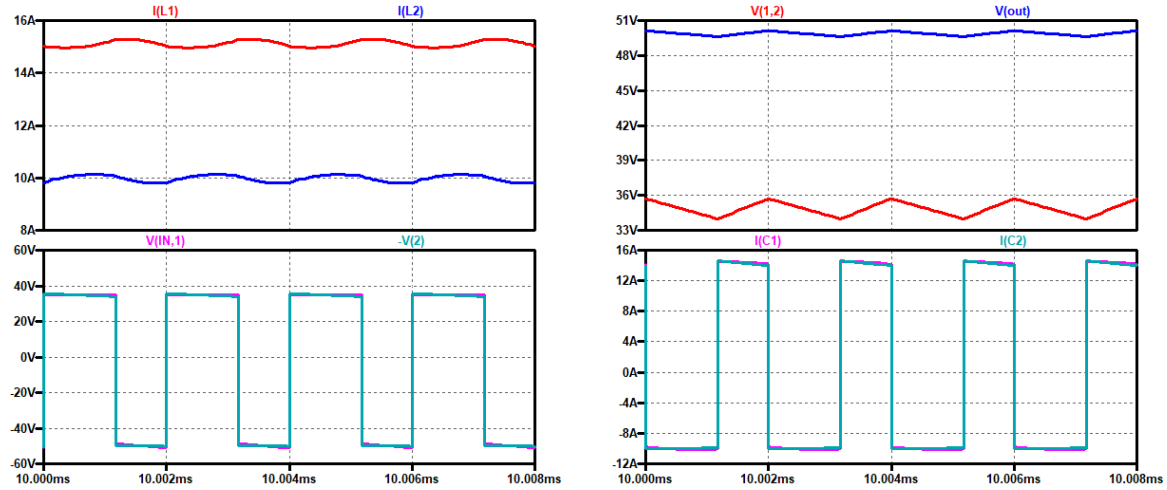


Figure 5.1 Schematic view of open-loop SEPIC simulation in LTspice.

From figure 5.1 it is seen that the open-loop simulation implements the coupled SEPIC topology. The passive components are ideal with no DC resistance, and the active components are defined by the SPICE model directives: `MySW` and `MyD`, effectively defining an ideal transistor and an ideal diode. On the other hand there is a series resistance in the voltage source, to make the simulation less stiff and aid the SPICE solver. In the schematic of figure 5.1 the scenario with $V_{\text{in}} = 35\,\text{V}$ and $P = 500\,\text{W}$ is presented, where the ideal transistor is driven by a pulse voltage source. The voltage source is specified at a switching frequency of 500 kHz and a duty cycle of 0.588, as defined by the SPICE parameters: `D` and `Tsw`. The waveforms of the inductors and capacitors are presented in figure 5.2.



(a) L_1 and L_2 waveforms. **(b)** C_1 and C_2 waveforms.

Figure 5.2 Steady-state waveforms of the passive components in the open-loop SEPIC simulation.

From the waveforms of the passive components it is seen that they resemble the analytical waveforms presented in figure 2.3. Furthermore it is found that inductor waveforms are not perfectly zig-zag, which is due to the voltage variation across them during ON and OFF state. This voltage variation is influenced primarily by the size of C_1, as proven and discussed in appendix D.1. From appendix D.1 it is also found that the coupled version of the SEPIC requires a higher value of C_1 in comparison to the uncoupled version. This is to limit the currents drawn from the leakage inductances. The inductor current- and capacitor voltage ripple amplitudes are computed using the SPICE measurement directives presented in listing 5.1.

```
.meas TRAN I_L1_ripple   PP I(L1)      FROM 18ms TO 19ms
.meas TRAN I_L2_ripple   PP I(L2)      FROM 18ms TO 19ms
.meas TRAN V_C1_ripple   PP V(1,2)     FROM 18ms TO 19ms
.meas TRAN V_C2_ripple   PP V(OUT)     FROM 18ms TO 19ms
.meas TRAN I_L1_avg      AVG I(L1)     FROM 18ms TO 19ms
.meas TRAN I_L2_avg      AVG I(L2)     FROM 18ms TO 19ms
.meas TRAN V_C1_avg      AVG V(1,2)    FROM 18ms TO 19ms
.meas TRAN V_C2_avg      AVG V(OUT)    FROM 18ms TO 19ms
```

The computed ripple amplitudes using listing 5.1 are presented in table 5.1.

Table 5.1 Component ripple and average signal values at different input voltages.

Component	L_1		L_2		C_1		C_2	
Input voltage	35 V	100 V	35 V	100 V	35 V	100 V	35 V	100 V
Ripple amplitude	0.32 A	0.40 A	0.32 A	0.40 A	1.76 V	1.00 V	0.50 V	0.28 V
Average value	14.32 A	5.07 A	9.98 A	10.02 A	34.86 V	99.95 V	49.89 V	50.09 V
Relative ripple	2.23%	7.89%	3.21%	3.99%	5.04%	1.00%	1.00%	0.56%

From table 5.1 it is apparent that the ripple amplitudes follow the analytical design goals presented in section 2.3. This is seen because the maximum input ripple is 0.4 A, the maximum C_1 ripple is around 5%, and the maximum C_2 ripple is 1%. L_2 is also at 0.4 A because this is the coupled SEPIC. This also means the interaction between mutual inductance and the self inductances behave as expected, effectively doubling the inductance. Finally the waveforms of the transistor and diode is evaluated. The resulting waveforms form the open-loop simulation is presented in figure 5.3.

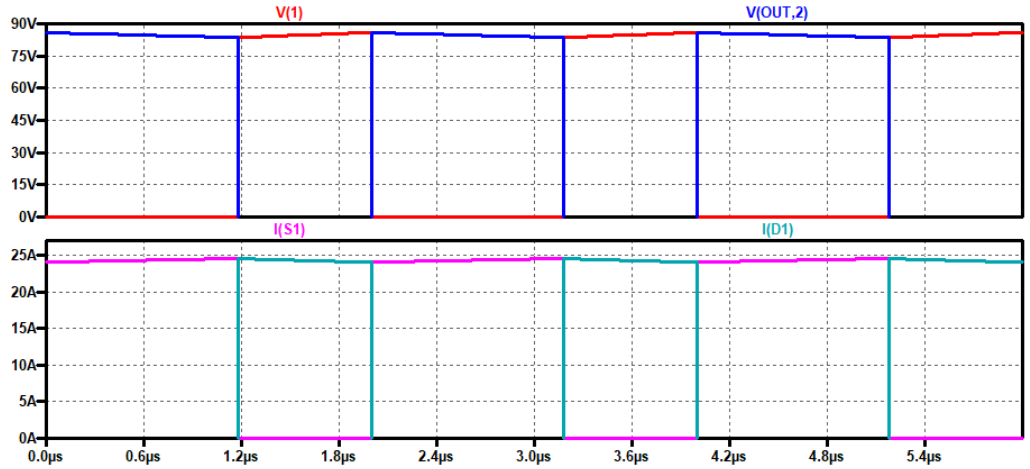
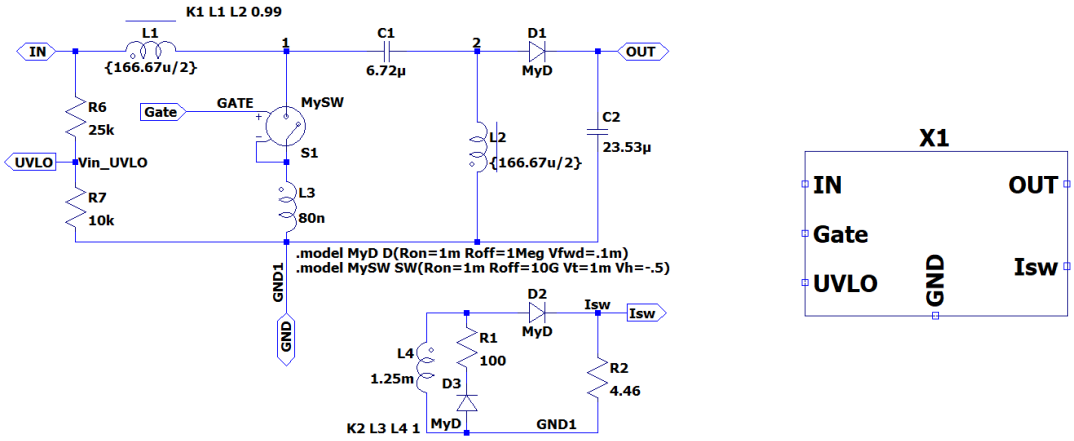


Figure 5.3 Steady-state waveforms of the transistor and diode in the open-loop SEPIC simulation.

From the transistor and diode waveforms it is observed how the semiconductors operate in a complimentary manner. It is also observed how that the current is ramped up when the transistor is conducting, and vice versa when the diode is conducting. Additionally it is seen that the diode and transistor block the sum of input and output voltage: $v_{\text{in}} + v_{\text{out}}$, thus validating the analytically derived waveforms of figures 2.5 and 2.6. Thereby the open-loop simulations validate the component sizing methods, as well as the theory regarding coupled inductors for the SEPIC topology. In the following section 5.2, closed-loop simulations of the SEPIC topology is covered.

5.2 Closed-Loop Simulation of the SEPIC

To asses the performance of the SEPIC in closed-loop control, a series of simulations due to various operational scenarios are developed. To test the same SEPIC in different scenarios, a test-bench structure for the simulation is developed. This revolves defining the SEPIC as a hierarchical block, and thereafter developing different test-benches around it. The hierarchical SEPIC block is defined as presented in figure 5.4.



(a) Sub-schematic of the SEPIC entry. **(b)** Hierarchical block.

Figure 5.4 Hierarchical definition of the SEPIC.

As seen in figure 5.4a the SEPIC hierarchical sub-schematic has three inputs: `IN`, `GND`, and `GATE`, and it has 3 outputs: `OUT`, `Isw`, and `UVLO`. The `GATE` is the gate connection to the transistor, `Isw` is the output

of the current sense transformer, located at the transistor source, and `UVLO` is a voltage used to disable the closed-loop control in case of under voltage at the input (under-voltage lockout). The current sense transformer has the required voltage gain, derived in equation (4.12), and has maximum losses of $\frac{1}{4}$W. The current sense transformer is further documented in appendix C.2.

5.2.1 Steady-State Regulation of the SEPIC

To asses the static regulation of the SEPIC a test bench with the parameters: $P = 500\,\text{W}$, and $V_{\text{in}} = 35\,\text{V}$ is developed. Analog Devices offer an equivalent component to the UC1843, being the LT124x component of PWM controllers. Since components from Analog Devices is readily available in LTspice, the LT1243 is used for the closed-loop control simulations. The static regulation test bench is presented in figure 5.5.

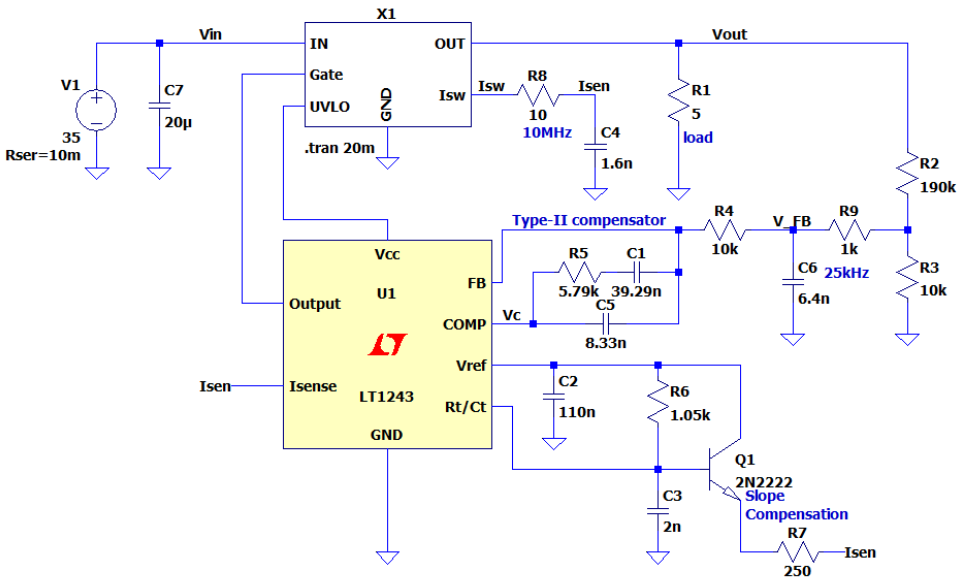
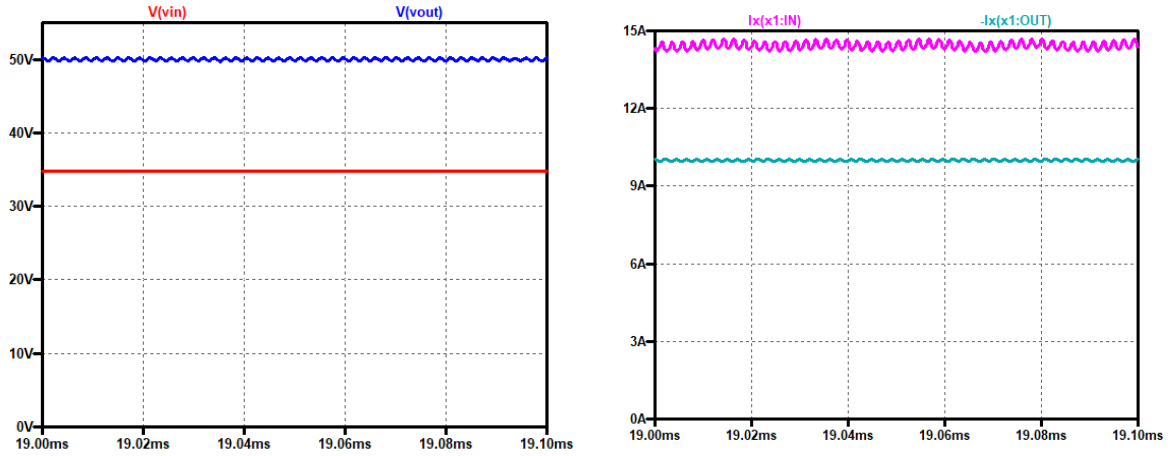


Figure 5.5 SEPIC simulation test bench for static regulation assessment.

From the schematic of figure 5.5 the entire feedback control system is observed. For the transistor current feedback a 10 MHz lowpass filter is implemented through `R8` and `C4`, to attenuate leading edge spikes. Also for the output voltage feedback a 25 kHz lowpass filter consisting of `R9` and `C6` is implemented to attenuate switching ripple. The type-II compensator is implemented with analogue components `R4`, `R5`, `C1`, and `C5`, to yield the compensator values of table 4.2, this conversion being described in appendix C.3. Finally the internal oscillator frequency of the LT1243 is set at the Rt/Ct pin with `R6` and `C3` to achieve $f_{\text{sw}} = 500\,\text{kHz}$. The resulting steady-state input- and output waveforms are presented in figure 5.6.

It is observed that the regulation scheme is following the reference without any steady state error. The mean voltage in the displayed period is 50.0 V, and the ripple amplitude is 537 mV corresponding to a static regulation ripple of 1.1% (or ±0.55%). The observed ripple is at switching frequency. Additionally it is seen from the current waveforms of figure 5.6b that the input- and output current are also subject to switching ripple. The current amplitudes follow the expected values for a 5 Ω equivalent load, and the average power within the displayed limits is 500.0 W, thereby confirming correct static operation of the feedback control scheme. An additional oscillation is observed in the input current of figure 5.6b. This oscillation is around 47.5 kHz, indicating a link to the high-frequency eigenvalues of the coupled scenario, presented in table 4.1.



(a) Input- and output voltage.

(b) Input- and output current.

Figure 5.6 Steady-state input- and output waveforms of closed-loop SEPIC static simulation test.

A common challenge with peak mode-current control is resulting sub-harmonic oscillations when the duty-cyle is greater than 50%. This is typically solved by adding a fixed ramp to the transistor current, which is commonly referred to as slope compensation [7]. This is implemented through `Q1` and `R7` which adds a ramp on top of the measured transistor current, `Isen`. The resulting slope compensation is visualised in figure 5.7.

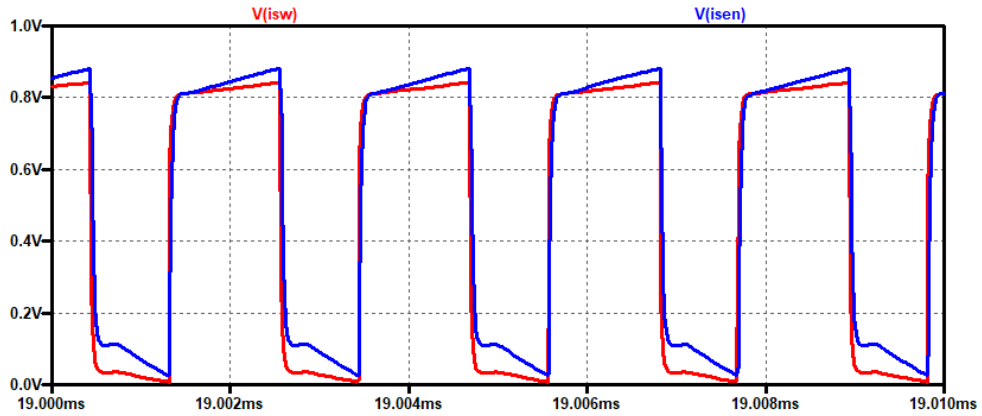


Figure 5.7 Slope compensation on the measured transistor current in the closed-loop SEPIC simulation.

From figure 5.7 it is clear that an additional ramp is added on top of `Isw`, resulting in `Isen` with a greater slope. The value of `R7` was chosen to yield a fair amount of slope compensation, however too aggressive slope compensation will make the regulation scheme behave more and more like voltage control, so a compromise exists [7].

5.2.2 Transient Regulation of the SEPIC

To asses the transient performance of the control loop a test bench is developed where a 50% load step occurs on the output, effectively increasing the power from 250 W to 500 W. The control loop will be evaluated in terms of how it responds to the change, and how it regulates the voltage to the reference 50 V. The test bench for the load step simulation is presented in figure 5.8. The load step is implemented by switching an additional equivalent resistance, `R10`, between the output voltage bus and ground. The load step is performed at 5 ms by turning ON the transistor `M1`. The voltage- and current waveforms during the load step transient is presented in figure 5.9.

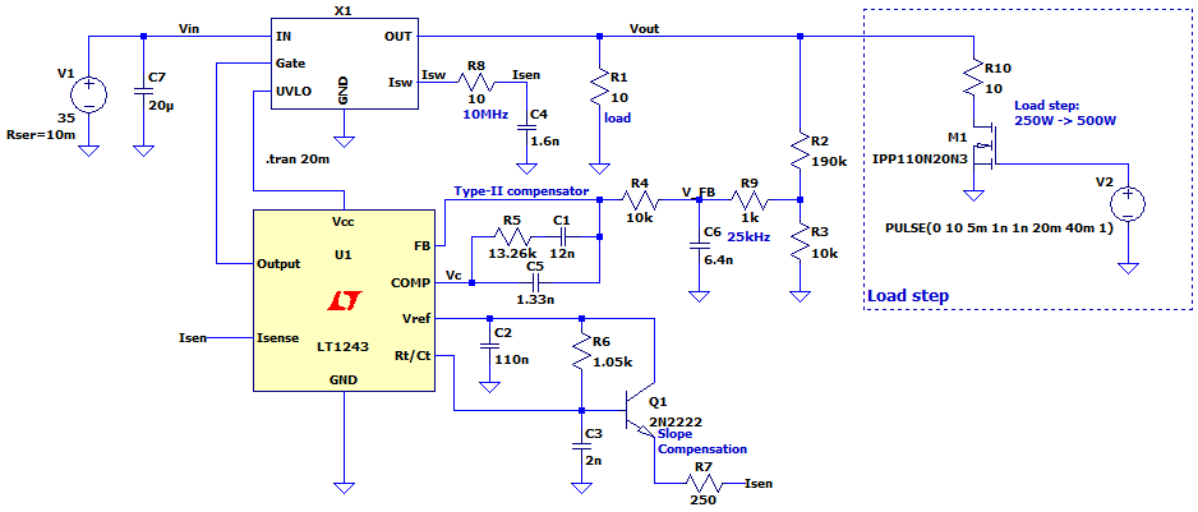
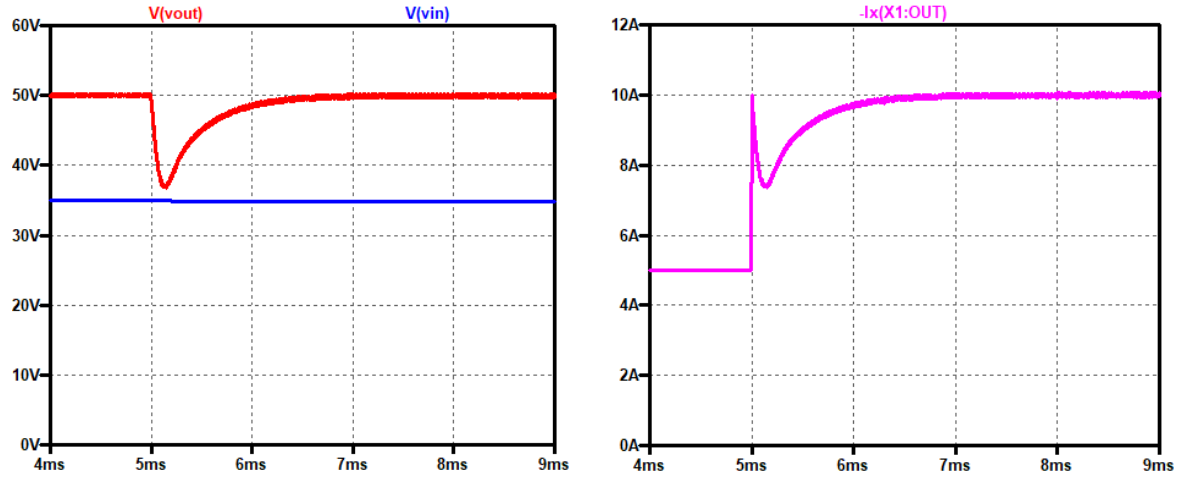


Figure 5.8 Test bench of the load step simulation test.



(a) Input- and output voltage.

(b) Output current.

Figure 5.9 Transient voltage- and current waveforms of the closed-loop SEPIC simulation subject to a 50% load increase.

From the transient voltage waveform of figure 5.9a a significant voltage nadir is observed due to the load change. Subsequently the control loop re-establishes 50 V within a timespan of 2 ms. For the SEPIC output current in figure 5.9b it is seen that the current initially spikes as the current is dropped, and thereafter it gradually reaches the full load current of 10 A. The spike is attributed from the output capacitance of the SEPIC as it discharges rapidly in response to the load change. The observed voltage drop of approximately 13 V is excessive and not in accordance with the required maximum transient of 1% in the ECSS standard. However it is also noted that this is a single SEPIC cell operating isolated, without any main bus. The main bus would typically have a capacitance that is orders of magnitude higher than the 23.53 µF of this APR cell, in order to fulfil the ECSS impedance mask requirement. A higher capacitance would also limit the voltage nadir as it inherently resists change in the voltage. In appendix D.2, it is shown that with a 5 mF main bus capacitance, the compensated SEPIC exhibits a voltage transient of 0.5% of 50 V in response to a 50% load step. Thereby it is clear that the SEPIC can fulfil the control-loop requirements from the ECSS standard. Combined with the static regulation validation of section 5.2.1, the peak current-mode control scheme for the SEPIC is validated comprehensively along with the small-signal modelling- and compensator design of section 4.2.

6 Laboratory Work

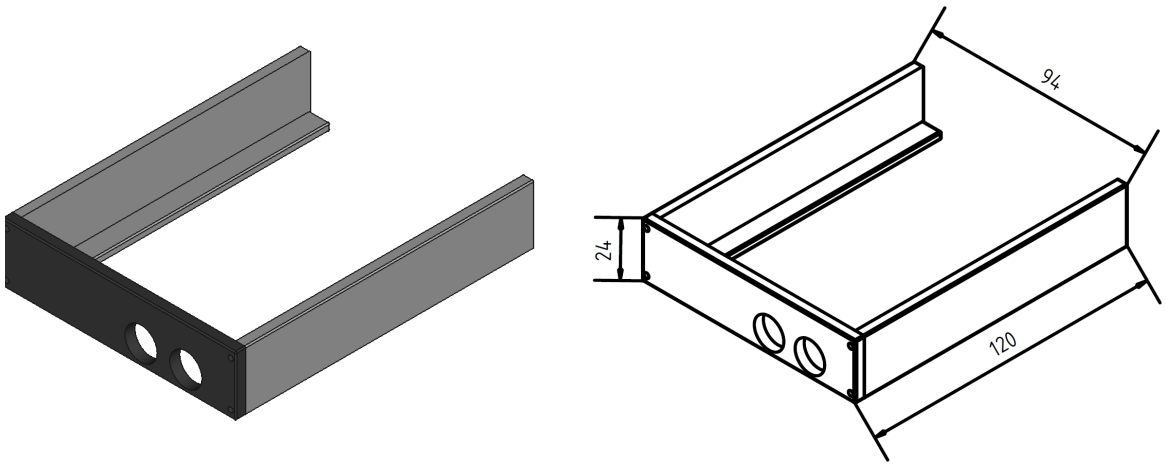
This chapter revolves around the work conducted in the laboratory. For this project, the laboratory work refers to the initial hardware design of a SEPIC and then the subsequent test campaign. The focus of the test campaign is to evaluate the efficiency of the developed SEPIC topology at different operational scenarios, especially evaluating the comparative performance of the uncoupled- and coupled SEPIC topology. Additionally the laboratory work also serves to asses the implications of the real world implementation and how it relates to design and modelling of the SEPIC topology.

6.1 Hardware Development and Implementation of SEPIC

This section covers the development of the SEPIC prototype used for the laboratory testing, and also serves to present some of the taken measures regarding the hardware implementation.

6.1.1 Framework and Mechanical Constraints

To properly analyse the feasibility of the SEPIC in regards to hardware implementation, it is relevant to take the mechanical constraints into account. In practice, the EPS consists of several modules, which are assembled in a modular fashion to suit the specific requirements of an associated mission [4]. For this project, the maximum APR module volume is presented in table 2.1. Considering that the APR module consists of 3 APR cells then a module of a single APR cell must be 1/3 of the maximum volume, that is: $(94 \times 150 \times 24)$ mm. The resulting frame design for a single APR cell is presented in figure 6.1.



(a) 3D view. **(b)** Dimensions.

Figure 6.1 Designed mechanical frame for the SEPIC hardware setup. Units are in mm.

From figure 6.1a is is observed that the frame has 3 faces. The front face (marked in black) is where the source terminals are connected, in this case the laboratory power supply. The rear face is open, as this would in principle connect to other modules via a backplane connector. Lastly are the frame sides which would be connected to the chassis of the satellite, and also is used to connect other modules together. Since the modules are stacked vertically, the frame sides act as thermal spreaders and effectively serve as the module's heatsink. Lastly it is observed from the dimensions of figure 6.1b that the designed module is confined within the maximum volume constraint. The exact dimensions result from a concurrent design process involving the Printed Circuit Board (PCB)s, components, and the mechanical frame.

Dual PCB Format

As presented in section 3.3 the most significant power loss contributors are the Schottky diode and the GaN HEMT. These two components have to dissipate several watts, while at the same time having relatively small footprints as presented in table 3.1. To keep the devices as well-cooled as possible, it is decided to mount the semiconductors directly on the heatsink. This is sought possible as the footprints are fairly small. This means that the SEPIC construction will consist of two PCBs, as illustrated in figure 6.2.

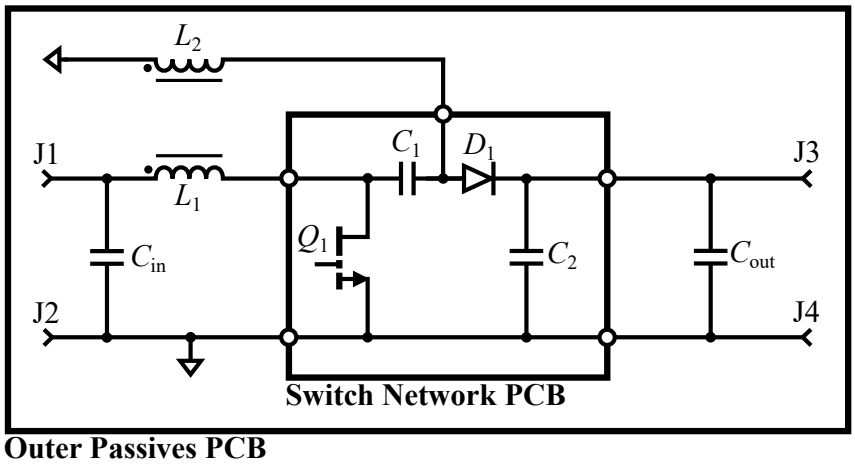
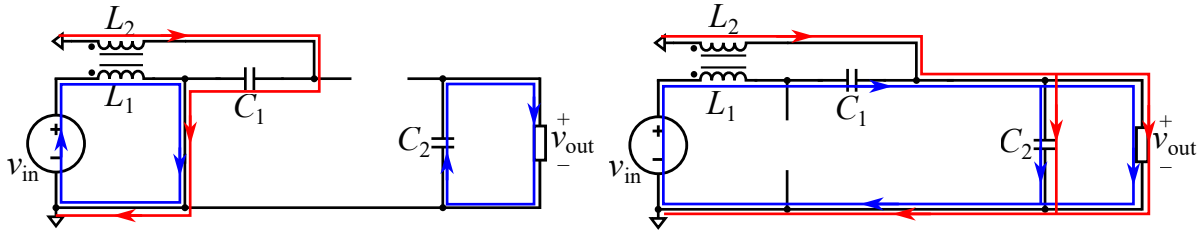


Figure 6.2 Schematic representation of the 2 PCB format. The switch network PCB is intended to sit on the side walls of the APR cell's frame.

From figure 6.2 is is observed that the inner switch network PCB consists of the Schottky diode, D_1, and the GaN HEMT, Q_1. The capacitors, C_1 and C_2, are sought to be implemented with Surface Mounted Device (SMD) footprints, thus make it possible for the switch network PCB to be adequately small to fit on the side of the frame. The switch network PCB is connected to the outer passives PCB through small cables. The outer passives PCB consists primarily of the more bulky passive components. Additionally the outer passives PCB facilitates sensors, signal filtering, and also logic- and power connectors.

6.1.2 Switch Network PCB Design

As presented in figure 6.2 the switch network PCB consists of the active components, that being the transistor, Q_1, and diode, D_1. Thus the main design goal of the switch network PCB is to achieve acceptable switching performance. For SMPSs incorporating GaN HEMTs, special attention should be at minimising the parasitic inductance of the high-frequency power loop [29]. The high-frequency power loop is a consequence of the high $\mathrm{d}i/\mathrm{d}t$ paths in the circuit due to switching. The current paths during each switch state of the SEPIC is presented in figure 6.3.



(a) ON state. **(b)** OFF state.

Figure 6.3 Current paths in the SEPIC during ON and OFF state.

Comparing figures 6.3a and 6.3b it is clear that the components which experience an alternating current are: The transistor, the diode, C_1, and C_2. That is, these components experience high $\mathrm{d}i/\mathrm{d}t$ during each switching event, thereby forming the SEPIC power loop presented in figure 6.4.

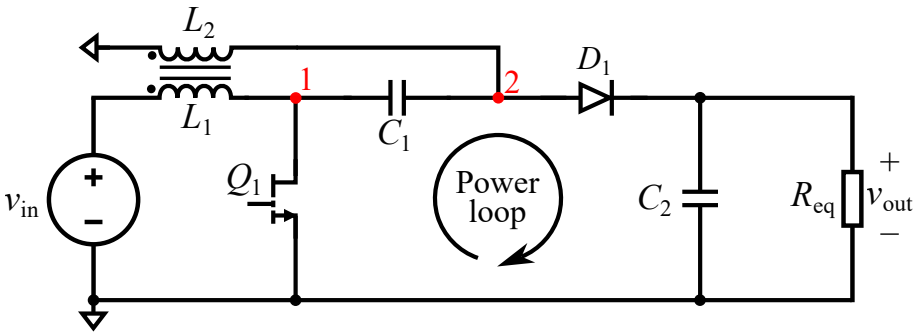


Figure 6.4 High-frequency power loop in the SEPIC topology.

The physical volume formed by the power loop results in parasitic inductance in the power loop, which can be approximated by equation (6.1).

$$L_{\text{loop}} = \mu_0 \frac{h}{w} l \tag{6.1}$$

where L_{loop} is the approximate power loop inductance, μ_0 is the permeability of free space, h is the height between the the hot- and return conductors, w is the width of the conduction path, and l is the length of the conduction path [29]. Thus to minimise the power loop inductance it is clear that h and l must be minimised, while w should ideally be as wide as possible. To achieve this, the switch network PCB layout attempts to minimise the length and height of the power loop as illustrated in figure 6.5.

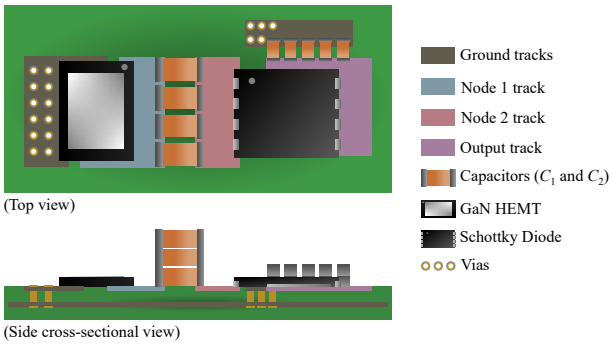


Figure 6.5 Switch network PCB layout [29].

The switch network PCB is a 4-layer PCB where the power loop is implemented on the top layer and with the return in the uppermost internal layer, to minimise h as much as possible. It is observed that the GaN HEMT, C_1 capacitor bank, and the Schottky diode are aligned in a vertical manner. At the output the C_2 capacitor bank goes in the horizontal direction in an attempt to increase the effective w, and reduce the return path length in an attempt to reduce l. The return occurs in the immidiate upper internal layer, to decrease the power loop areas as much as possible. In an attempt to reduce the inductance of the capacitor packages C_1 and C_2 are implemented with multiple packages in parallel (horizontally), and then multiple stacked (vertically) to achieve the required capacitance value. The C_1 capacitor bank consists of 4×3 220 nF 1206 SMD capacitors rated for 220 V, effectively resulting in a total capacitance of 2.64 µF. C_2 capacitor bank is composed of 5×2 330 nF 0402 SMD capacitors rated for 63 V, effectively resulting in a total capacitance of 3.30 µF. It is noteworthy that the C_1 capacitor bank deviates considerably compared to the analytical C_1 capacitance of 6.72 µF, however the amount of capacitors is limited by the available space which is also seen in the physical construction of figure 6.8. Additionally gate driver and connectors are also present on the switch network PCB. Lastly the bottom layer consists of exposed pads connected to the upper layer with thermal vias such that the switch network PCB is cooled from the bottom side. The CAD files regarding the switch network PCB can be accessed via the uploaded ZIP folder.

6.1.3 Outer Passives PCB

The switch node PCB of section 6.1.2 is connected to the outer passives PCB with short cables as illustrated in figure 6.2. The outer passives PCB incorporates the inductors L_1 and L_2 (uncoupled or coupled) as well as the input- and output capacitors, C_{in} and C_{out} respectively. In this laboratory setup C_{in} works as a decoupling capacitor consisting of a single 10 µF film capacitor, and C_{out} acts as the bulk capacitance at the output consisting of 2×10 µF film capacitors. The inductor core(s) and bulk capacitors are those presented in table 3.1. During the design process, the experience was that the module height constraint had a rather large impact on the number of suitable components. Additionally the outer passives PCB also consists of input- and output voltage sensors, as well as a low-side current sensor in series with L_2. A schematic of the outer passives PCB is presented in figure 6.6.

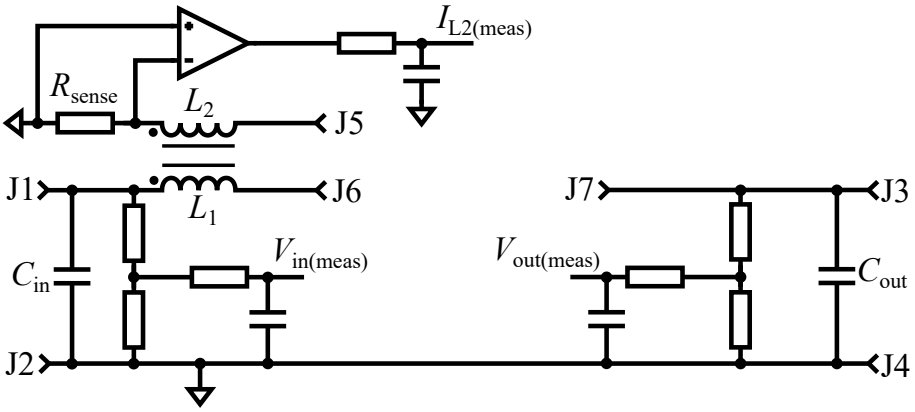


Figure 6.6 Simplified schematic of the outer passives PCB.

The connectors J1 and J2 are the source input terminals, J3 and J4 are the output terminals, J5, J6, and J7 all connect to the switch network PCB, as presented in figure 6.2. The input- and output voltage sensor consist of a simple voltage divider and a series lowpass filter to attenuate switching noise. The current sensor is implemented with a shunt resistor and associated current sense amplifier also with a lowpass filter at the output. Note that there is no current sensor in the transistor path, thus peak-current mode control was not possible to validate with the developed laboratory setup. The CAD files regarding the outer passives PCB can be accessed via the uploaded ZIP folder.

6.1.4 The Comprehensive SEPIC Test Module for Laboratory Work

The 4 layer switch network PCB was ordered externally while the outer passives PCB and the module frame was manufactured in house. The comprehensive SEPIC module was assembled in the laboratory at Aalborg University by attaching the switch network PCB to the module heatsink walls. The fully assembled SEPIC test module is presented in figure 6.7.

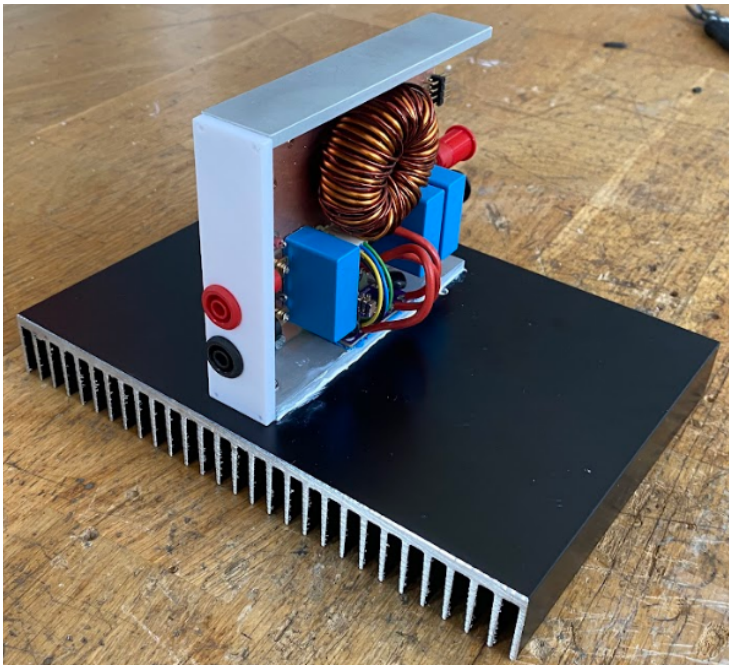
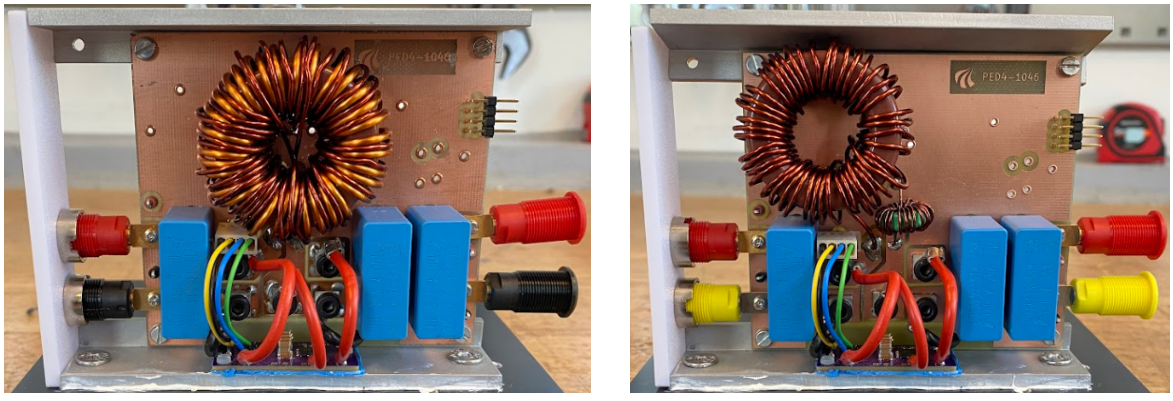


Figure 6.7 Developed SEPIC test module for laboratory use, with coupled inductors.

From figure 6.7 it is observed that an additional heatsink is attached to the SEPIC tests module. This is to emulate a connection of the entire EPS to the spacecraft chassis. The heatsink is attached to the module with a thin layer of thermal paste to optimise the surface contact. Additionally the switch network PCB is attached to the heatsink walls with a dielectric 1 mm thermal sheet and nylon screws. figure 6.7 showcases the module with coupled inductors, but the footprints of the outer passives PCB was also designed for uncoupled inductors, to allow testing hereof. Both uncoupled- and coupled SEPIC test modules are presented in figure 6.8.



(a) Coupled test module. **(b)** Uncoupled test module.

Figure 6.8 Top views of the SEPIC test modules.

In both figures 6.8a and 6.8b it is observed how the switch network PCB is connected to the outer passives

PCB. The cable connection make the inductor currents accessible with a current probe. The 8-pin header on the back side of the module connects to an external microcontroller for PWM generation, sampling of sensors, enabling of signals etc. In the microcontroller the following trip events are implemented: under-voltage lockout based on the input voltage, over-current protection based on the L_2 current measurement, and finally over-voltage protection based on the output voltage sensor. Thereby the input and output should be failure protected in case of either short-circuits or open-circuits on the input- or output-side. The microcontroller C code is presented in appendix F.3.

6.2 Experimental Evaluation of the SEPIC Prototype Module

To perform the experimental tests on the developed SEPIC prototype module, a laboratory setup was constructed in the Electrical Engineering Laboratory at Aalborg University. The laboratory test setup is presented in figure 6.9.

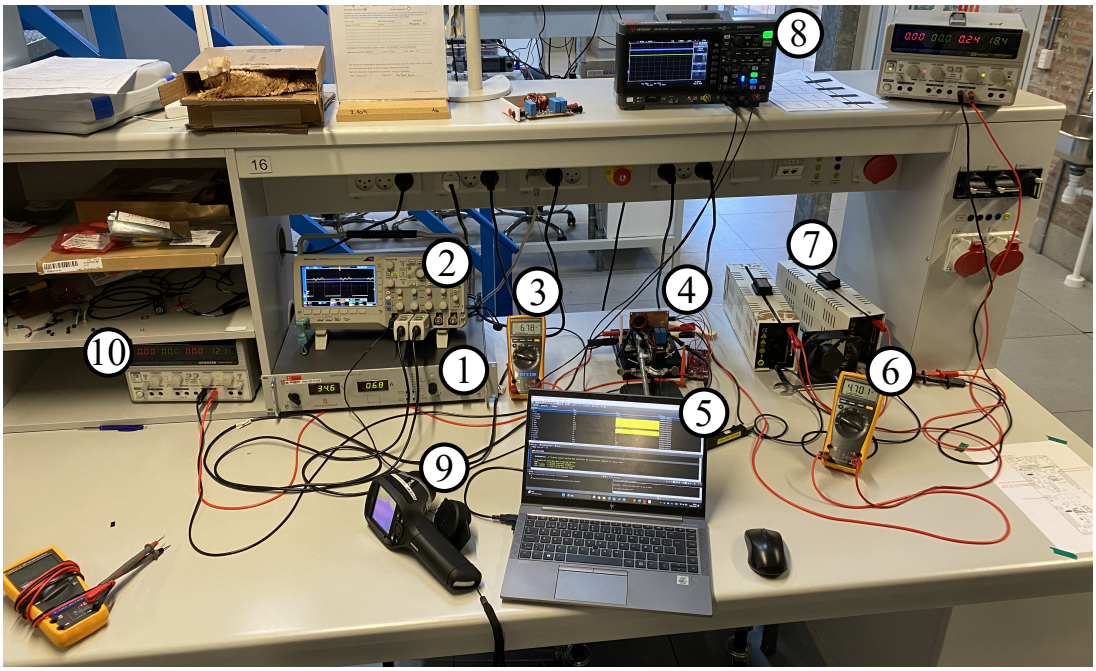


Figure 6.9 Laboratory Setup: 1) main power supply, 2) 1st oscilloscope, 3) input ammeter, 4) SEPIC test prototype, 5) control computer, 6) output ammeter, 7) equivalent load resistance, 8) 2nd oscilloscope, 9) thermal camera, 10) gate drive power supply.

At the centre of the laboratory setup is the SEPIC prototype module presented in section 6.1.4, and the surrounding devices specifications are all listed in table 6.1. At the input side of the SEPIC prototype the main power supply is connected through a multimeter. Similarly the output side is connected to the equivalent load resistance through another multimeter. The multimeters are used to measure the DC currents at the input and output to accurately estimate the converter efficiency. Furthermore 2 oscilloscopes are used to capture plenty of signals in the laboratory setup. The 1st oscilloscope is used to measure high-frequency signals, such as the drain-to-source voltage, the diode voltage, the inductor currents. The 2nd oscilloscope is only used to measure DC voltages at the input and output, which in combination with the multimeters are used to compute the efficiency of the SEPIC prototype. To power the UCC27611 gate driver an external power supply is used.

To generate PWM and implementing control- and protection mechanisms the TMS320F28069M microcontroller is used. The microcontroller is connected to the computer which allows real time monitoring and -control of the setup. After initialising the setup a thermal camera was used to obtain the

hotspots in the setup. Each thermal reading was recorded after a minimum of 2 minutes in steady-state operation.

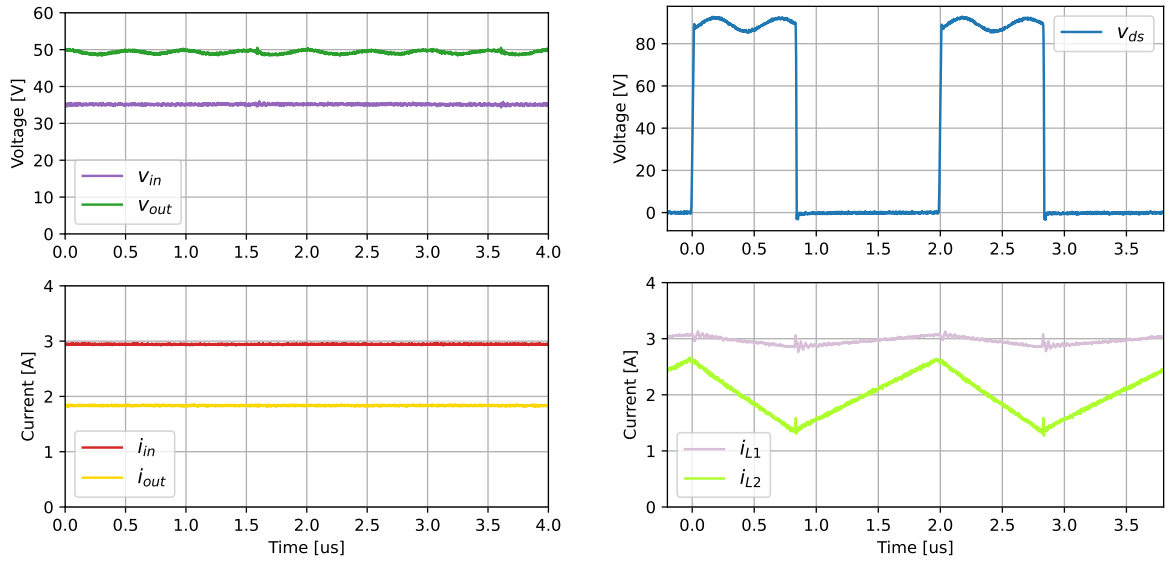
Table 6.1 Specifications of the devices used in the laboratory setup.

Device	Model	Manufacturer	Notes
Main power supply	SM70-22	Delta Elektronika	Max 70 V, 22 A
Oscilloscope 1	DPO4054B	Tektronix	4-channel, 500 MHz, 1 GS/s
Oscilloscope 2	DSOX1204G	Keysight	4-channel, 70 MHz, 2 GS/s
Multimeter(s)	Model 179	FLUKE	Max 10 A with $\pm 1\% + 3$
Microcontroller	TMS320F28069M	Texas Instruments	90 MHz, 12 bit ADC
Thermal Camera	E60	Teledyne Flir	-20 to 650 °C, ±0.05°C
Gate drive supply	IPS4304	ELFA Distrelec	Max 30 V, 3 A

The SEPIC prototype was tested up to an input voltage of 50 V at a fixed output voltage of $\approx$ 50 V. Additionally the tests were performed for a switching frequency of 250 kHz and 500 kHz. The variation in voltage and switching frequency allows an evaluation of the correlation to power losses.

6.2.1 Waveforms of the Uncoupled SEPIC Prototype

To evaluate the performance of the SEPIC prototype and relate it to the theoretically derived waveforms of section 2.2.4, the experimental waveforms of the uncoupled SEPIC prototype are analysed in this section. The presented waveforms are recorded with the SEPIC prototype operated in open-loop. The input-to-output waveforms as well as dynamic switching waveforms during steady-state are presented in figure 6.10



(a) Input and output waveforms. **(b)** Dynamic waveforms.

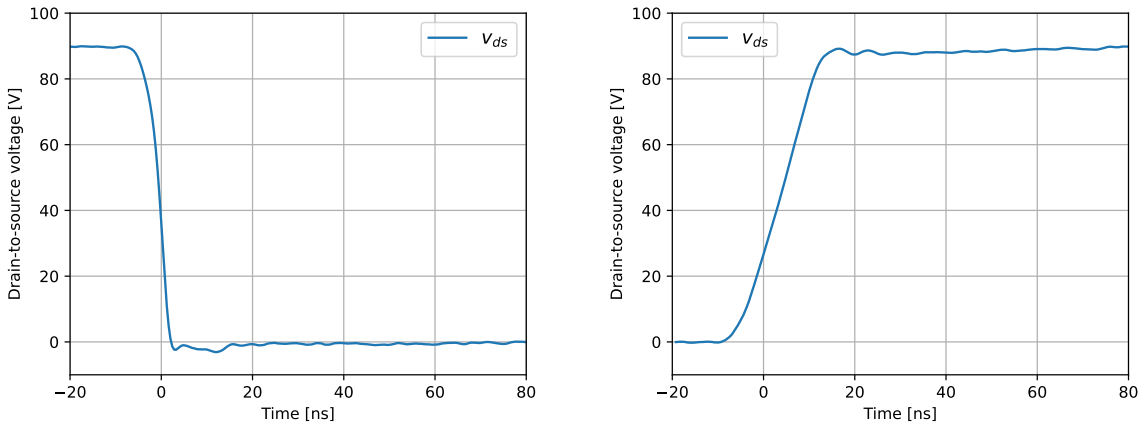
Figure 6.10 Steady-state waveforms of the uncoupled SEPIC prototype with $V_{\text{in}} = 35$ V at $P = 100$ W.

In figure 6.10a the input- and output voltages and -currents are plotted. Here it is observed that the SEPIC prototype successfully operates as intended with an input voltage of 35 V, and an output voltage in the range of 50 V. The mean output voltage is $V_{\text{out}} = 49.3$ V, deviating from the 50 V as a result of the open-loop duty-cycle and losses in the converter. The currents are inversely scaled with the voltage maintaining the power balance. These current are measured with the TCP0030 current probe. Additionally a 2 MHz oscillation is present on the output voltage with an amplitude of ±1.16 V, yielding

a relative ripple of 2.4%. This implies that the design aim of $< 1\%$ ripple is not realised in the laboratory. It noteworthy that the 2 MHz oscillation is not in the same range as the switching frequency.

Furthermore the transistor drain-to-source voltage, v_{ds}, the input current, i_{in}, and the inductor currents, i_{L1} and i_{L2}, are plotted in figure 6.10b. Here it is seen how the transistor is clearly turning on and off at a period of 2 µs corresponding to the 500 kHz switching frequency. When the transistor is ON, it observed how the inductors are ramping up indicating that they are charging up, and are discharging during the OFF period. It is also observed that i_{L1} and i_{L2} oscillate around i_{in} and i_{out}, respectively, matching the analytical derivations of equation (2.26). Aside from natural laboratory deviations, the waveforms resemble the expected waveforms of the ideal uncoupled SEPIC, presented in figures 2.3 and 2.6. Thereby the analytical modelling of the SEPIC is validated. Moreover, when the transistor is blocking, a 2 MHz voltage ripple is also observed similarly to that of the output voltage. Additional figures including the waveforms of the coupled SEPIC, as well as the diode waveforms, and waveforms at higher voltages are presented in appendix E.1. In regards to the observed 2 MHz ripple on the output- and the drain-to-source voltage, the root cause was unfortunately not identified within the project timeframe.

To asses the dynamics during each switching event, the GaN HEMT drain-to-source voltage, v_{ds}, during turn-on and turn-off is presented in figure 6.11.



(a) Turn ON event. **(b)** Turn OFF event.

Figure 6.11 Drain-to-source voltage, v_{ds}, of the GaN HEMT during turn ON and -OFF.

From the turn on event of figure 6.11a it is seen that the voltage rapidly drops, with a fall time of just 5.2 ns. This means that the transistor in this case is switching with 17.3 $\frac{\text{V}}{\text{ns}}$. For the turn OFF event the voltage rises with less rate-of-change, where in this case the rise time is 15.6 ns. This is because of the output capacitance of the transistor, C_{oss}, which is charged up after the transistor is turned off. Subsequent ringing occurs at a frequency of 156.3 MHz, indicating a power loop inductance of just 1.3 nH. The analysis of the power loop is further documented in appendix E.1.3. The drain-to-source voltage waveform was recorded with a 200 MHz TPP0200 passive probe.

6.2.2 Thermal Characteristics of the SEPIC Prototype

To characterise the performance limits of the SEPIC prototype, the thermal performance is assessed to avoid over-heating of any device. Especially the diode, inductor(s), and transistor are of concern due to the analytical components losses, presented in section 3.3. The upper temperature limits provided by the component datasheets are presented in table 6.2 where T_{J} and T_{core} are the junction- and core temperature, respectively.

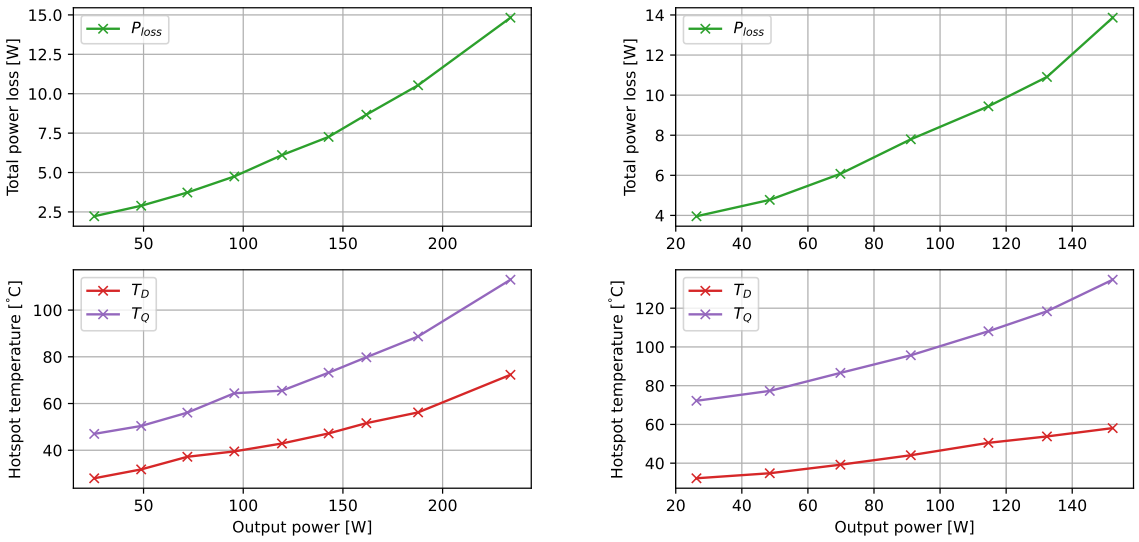
Table 6.2 Upper thermal limits of the critical power dissipating components [20] [22] [23] [24].

Component	Part number	Thermal Limit
GaN HEMT	EPC2304	$T_{\mathrm{J}} = 150\,^{\circ}\mathrm{C}$
Schottky diode	V30K202	$T_{\mathrm{J}} = 165\,^{\circ}\mathrm{C}$
Coupled inductor core	0074083A7	$T_{\mathrm{core}} = 200\,^{\circ}\mathrm{C}$
Independent L_2 core	0059050A2	$T_{\mathrm{core}} = 200\,^{\circ}\mathrm{C}$

Universally for all possible combinations of switching frequency, coupled- or uncoupled inductors, and output power of the SEPIC prototype it was found that the thermally limiting component was the transistor, Q_1. In the following analysis the output power was increased until reaching the temperature limit for the EPC2304 GaN HEMT, in this case limited to 135 °C, since the thermal camera is reading the hotspot temperature and not the junction temperature. In the datasheet it is however noteworthy that it is specified that the thermal resistance in-between junction and case is merely: $R_{\mathrm{th(J\rightarrow C)}} = 0.2\,\frac{\mathrm{K}}{\mathrm{W}}$.

Semiconductor Thermal Characteristic

The temperature curves subject to various output powers and switching frequencies are presented in figure 6.12, where T_{D} and T_{Q} are the hotspot temperatures of the diode and transistor, respectively.



(a) $f_{\mathrm{sw}} = 250\,\mathrm{kHz}$ scenario. **(b)** $f_{\mathrm{sw}} = 500\,\mathrm{kHz}$ scenario.

Figure 6.12 Temperature curves of the Schottky diode and GaN HEMT due to a sweep in output power. Input voltage is 35 V.

From the power loss it is seen that the trend is not linearly dependent on the output power. This is because the output power is proportional to the current, and the power losses due to conduction loss are proportional to the current squared. It is observed that the transistor temperature, T_{Q}, is higher than the diode temperature, T_{D}, at all power levels. Using the `P_loss_SEPIC()` function presented in appendix F.1, the relative contributions of diode and transistor losses can be estimated. This enables the determination of the thermal resistance from the hotspot to ambient. This estimation is computed based on the last three measured data point with an ambient temperature of 25 °C, resulting in the estimated parameters of table 6.3. The estimated diode- and transistor loss contributions are computed at 200 W and 125 W for the $f_{\mathrm{sw}} = 250\,\mathrm{kHz}$ and $f_{\mathrm{sw}} = 500\,\mathrm{kHz}$ scenarios, respectively.

From the estimated thermal resistances of table 6.3 it is observed that the diode exhibits a superior

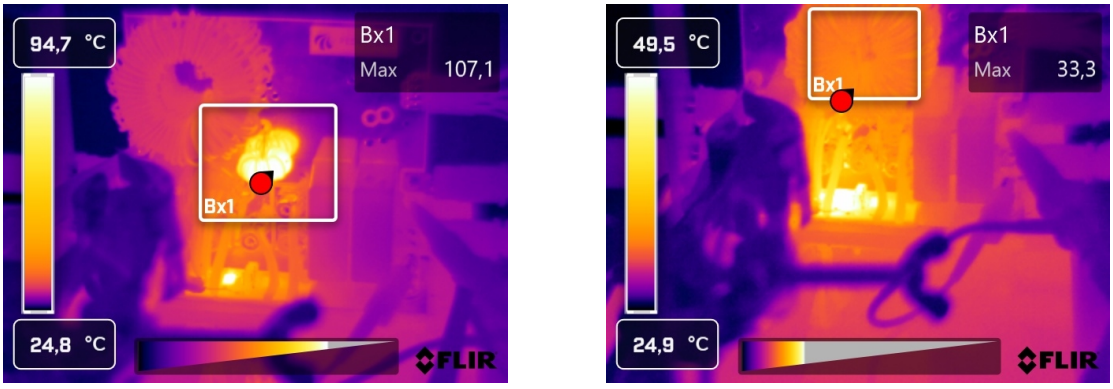
Table 6.3 Estimation of the diode's- and transistor's thermal resistance in the SEPIC prototype.

Parameter (Estimated)	250 kHz scenario	500 kHz scenario
Diode loss contribution	54.5%	43.4%
Transistor loss contribution	24.0%	44.0%
Diode thermal resistance, $R_{\text{th(HS}\rightarrow\text{A)}}$	5.64 $\frac{\text{K}}{\text{W}}$	6.2 $\frac{\text{K}}{\text{W}}$
Transistor thermal resistance, $R_{\text{th(HS}\rightarrow\text{A)}}$	24.9 $\frac{\text{K}}{\text{W}}$	19.7 $\frac{\text{K}}{\text{W}}$

thermal conductivity in comparison to the transistor. The high thermal resistance of the transistor also reveals a problem in terms of limiting the peak power that the SEPIC prototype can be operated at. In general the prototype is limited to $P < 300\,\text{W}$ and $P < 150\,\text{W}$ for the $f_{\text{sw}} = 250\,\text{kHz}$ and $f_{\text{sw}} = 500\,\text{kHz}$ scenarios, respectively. This also explains the reason why a $f_{\text{sw}} = 250\,\text{kHz}$ scenario is tested, because it allows the converter to be operated to higher power throughput levels, although no longer satisfying the ripple requirements. It should be noted that switching losses in theory scales linearly with the switching frequency, thus the total power loss curve is expected to be shifted vertically mostly.

Inductors Thermal Characteristic

The thermal characteristics of the inductors are also evaluated. This is done by comparing the coupled version- to the uncoupled version of the SEPIC prototype. Steady-state thermal images subject to $f_{\text{sw}} = 500\,\text{kHz}$ and $V_{\text{in}} = 50\,\text{V}$ are presented in figure 6.13.



(a) Uncoupled inductors. **(b)** Coupled inductors.

Figure 6.13 Temperatures of the uncoupled- and coupled versions of the SEPIC prototype.

By comparing figures 6.13a and 6.13b it is seen that the version with uncoupled inductors reaches a significantly higher temperature of 107.1 °C. This higher temperatures occurs in the small L_2, which is likely due to the core having considerably less volume and surface area. Additionally the ripple current is much higher in the uncoupled scenario, resulting in higher losses in the cores as outlined in equation (3.13). Using equation (2.37) the ripple currents in L_2 are $\Delta i_{\text{L2}} = 0.3\,\text{A}$ and $\Delta i_{\text{L2}} = 1.5\,\text{A}$ for the coupled- and uncoupled versions of the SEPIC prototype, respectively. The latter ripple amplitude is also observed in the L_2 current waveform of figure 6.10b.

The analysis outlined in this section suggests that the SEPIC prototype is functioning in accordance with the analytical expressions of chapter 2. However there exists some expected real life deviations, of which the thermal performance has a rather large impact on the following analysis as the obtainable maximum power level is limited. However, the tendencies should still hold at lower power levels, and when necessary the switching frequency can be lowered to 250 kHz to analyse the tendency at higher power level.

6.2.3 Evaluation of SEPIC Prototype's Efficiency

As part of the laboratory testing, the efficiency of the SEPIC prototype is evaluated. The goal of this analysis is to compare the experimental performance to the analytical loss model, presented in section 3.3. To be able to evaluate the impact of coupling, voltage level, and switching frequency on the efficiency characteristic, the tests of table 6.4 were conducted during the laboratory work.

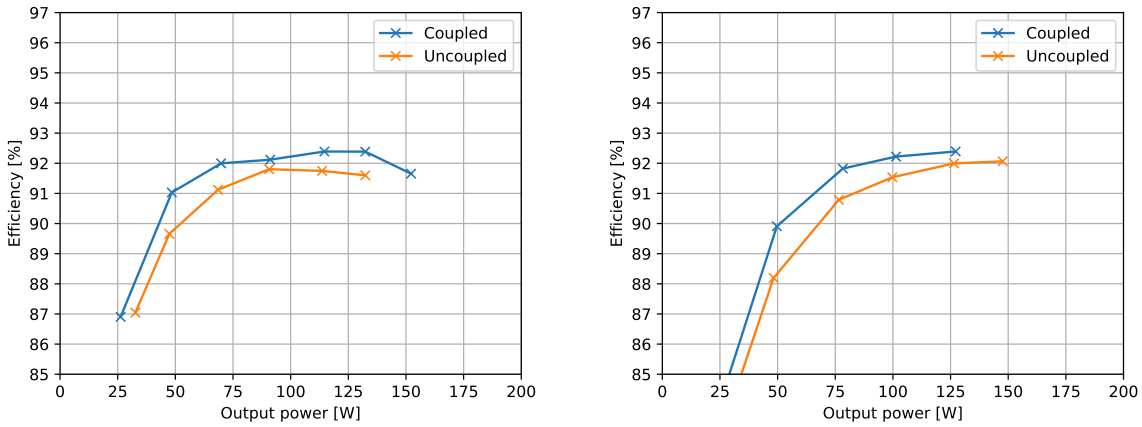
Table 6.4 Combinations of conducted laboratory tests.

	Uncoupled		**Coupled**	
V_{in} / f_{sw}	35 V	50 V	35 V	50 V
250 kHz	*Done*	*Done*	*Done*	*Done*
500 kHz	*Done*	*Done*	*Done*	*Done*

For the $f_{sw} = 500\,\text{kHz}$ tests the efficiency is evaluated up to about 150 W, and for the $f_{sw} = 250\,\text{kHz}$ tests the efficiency is evaluated up to about 250 W. This power limit is a consequence of the thermal constraints, presented in section 6.2.2. The $f_{sw} = 250\,\text{kHz}$ tests do not comply with the ripple requirements, but are used to evaluate the general trend at higher power. The results of the $f_{sw} = 250\,\text{kHz}$ tests are presented in appendix E.2.1. In the following subsections the efficiency results from the $f_{sw} = 500\,\text{kHz}$ tests are evaluated. In all tests the input- and output current is measured using the FLUKE 179 multimeter in combination with TPP0100 passive probes to measure the input- and output voltage of the module.

Impact of Magnetic Coupling on the SEPIC Prototype Efficiency

In this part, the impact from the inductors coupling is analysed based on the experimental results. This is done by evaluating the efficiency characteristic of the uncoupled- and coupled version of the SEPIC prototype. The efficiency results in this scenario is presented in figure 6.14.



(a) $V_{in} = 35\,\text{V}$ scenario. **(b)** $V_{in} = 50\,\text{V}$ scenario.

Figure 6.14 Efficiency profiles of uncoupled- and coupled versions of the SEPIC.

From the efficiency curves of figure 6.14a it is seen that the coupled version of the SEPIC prototype has a higher efficiency in comparison to the uncoupled version across all data points. The mean difference in efficiency across all data points is $0.64\%_{pp}$. This is in accordance with the modelled efficiency curve of figure 3.7a, indicating that the tendency of the model is accurate. On the other hand the efficiency is shifted vertically, yielding a lower efficiency than the analytical model. This suggests that the magnitude of the experimental losses are greater than the modelled losses. The peak efficiency and the power level at which it occurs is presented in table 6.5.

From the efficiency curve of figure 6.14b with higher voltage it is also seen that the coupled version of the SEPIC prototype exhibits a higher level of efficiency in comparison to the uncoupled version. The mean difference in efficiency across all data points is $0.72\%_{\text{pp}}$. In view of the power range, this also matches the tendency of the analytical model presented in figure 3.7b, suggesting that the modelled tendency for higher voltage is also correct. Similarly to the lower voltage case, the efficiency level is shifted vertically, exhibiting lower efficiency than the analytical model. Furthermore, the analytical model indicated that at peak efficiency the uncoupled case will become the most efficient configuration. This cannot be validated from the laboratory curve, however it is observed that the curve tendency does seem to match within the available power range with a shrinking difference in efficiency. The peak efficiency and the power level at which it occurs is presented in table 6.5.

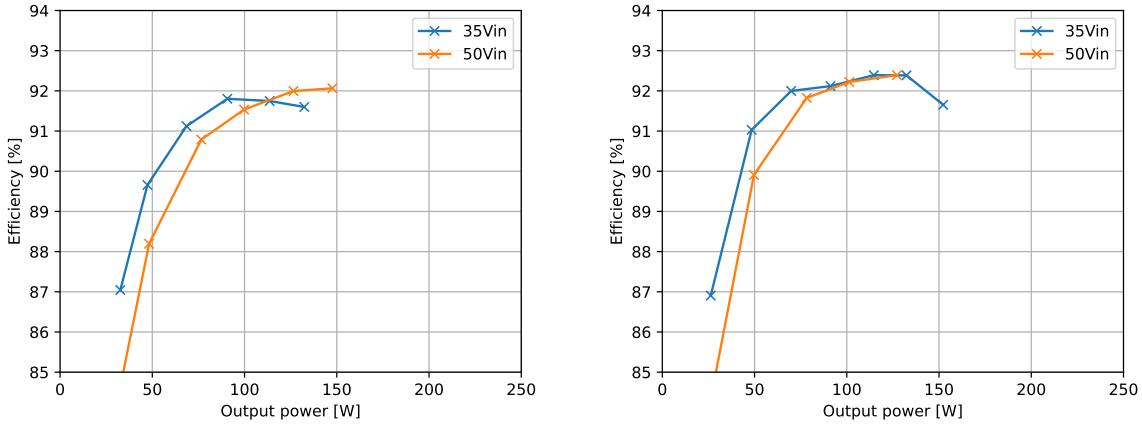
Table 6.5 Peak efficiency points on the power curve of the experimental SEPIC prototype with uncoupled- and coupled inductors.

Parameter	**Uncoupled**		**Coupled**	
Input voltage, V_{in}	35 V	50 V	35 V	50 V
Peak efficiency, $\hat{\eta}$	91.8%	92.0%	92.4%	92.4%
Power level, P_{out}	90.7 W	147.6 W	114.6 W	127.2 W

The general trend from table 6.5 compared with the analytical efficiency curve of table 3.3 is that the point of peak efficiency is less than estimated, and also the point of peak power is shifted toward lower power level. This suggests that the conduction losses are higher in the experimental results compared to the expected losses from the analytical model. The same comparison but with a switching frequency of 250 kHz is presented in appendix E.2.1. The results hereof show the same tendency, reaching a peak efficiency of 96.8% for the coupled version of the SEPIC prototype.

Impact of the Input Voltage Magnitude on the SEPIC Prototype Efficiency

In this part of the analysis the experimental efficiency curve is evaluated in regard to different input voltage levels. The measured efficiency curves due to different voltage levels, for the uncoupled- and coupled version of the SEPIC prototype separately, is presented in figure 6.15.



(a) Uncoupled inductors scenario. **(b)** Coupled inductors scenario.

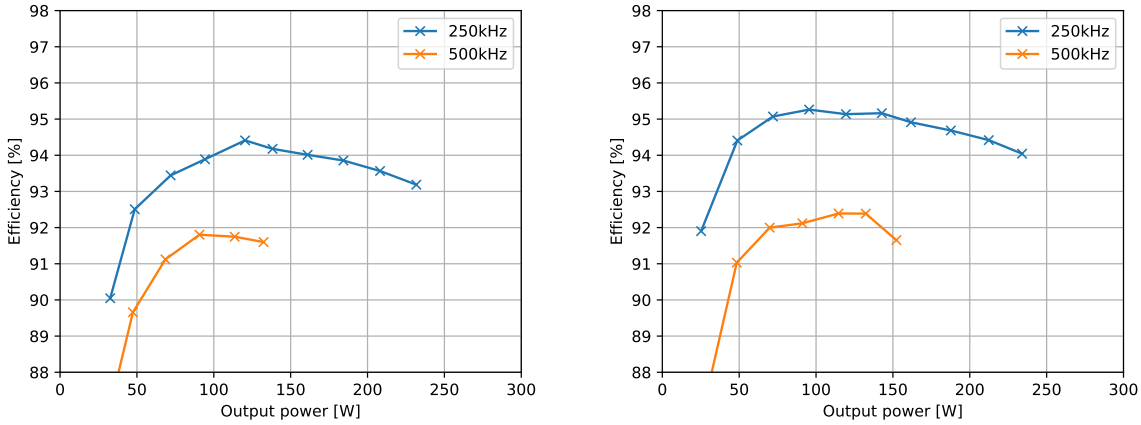
Figure 6.15 Efficiency profiles of the uncoupled- and coupled versions of the SEPIC prototype at different input voltages.

From the experimental efficiency curves of figure 6.15 it is observed that the higher voltage cases has

the peak efficiency point shifted to higher power levels. This is in accordance with the same tendency of the analytical efficiency model, as presented in figure 3.8. It is also the case here that the points of peak efficiency are shifted to lower power levels, supporting that the experimental conduction losses are greater than expected in both input voltage scenarios. The peak efficiency pints and the power levels at which they occur are also presented in table 6.5. The efficiency curves at various voltage level for a switching frequency of 250 kHz is presented in appendix E.2.1 yielding the same tendency.

Impact of the Switching Frequency on the SEPIC Prototype Efficiency

Lastly it is evaluated how the experimental losses compare at different switching frequency. The experimental efficiency curves for the SEPIC prototype with an input voltage of 35 V at a switching frequency of 250 kHz and 500 kHz are presented in figure 6.16b



(a) Uncoupled inductors scenario.

(b) Coupled inductors scenario.

Figure 6.16 Efficiency profiles of the uncoupled- and coupled versions of the SEPIC prototype at an input voltage of 35 V and a switching frequency of 250 kHz and 500 kHz.

From figure 6.16 it is apparent that the scenario with lowest switching frequency also exhibits the highest efficiency across the entire power range. It is found that the mean efficiency difference is $2.58\%_{\text{pp}}$ and $3.34\%_{\text{pp}}$ for the uncoupled- and coupled configuration of the SEPIC prototype, respectively. In comparison to the results of the analytical model, presented for the comparison regarding switching frequency in appendix B.2.2, the mean efficiency differences were just $0.43\%_{\text{pp}}$ and $0.99\%_{\text{pp}}$ for the uncoupled- and coupled versions of the SEPIC. This indicates that the difference in switching frequency has a greater impact on the experimental SEPIC prototype, than what was indicated by the analytical model. Furthermore it also suggests that the EPC2304 is perhaps not suitable for a switching frequency of 500 kHz in view of the scenarios accounted in this project.

Summary of the SEPIC Prototypes Efficiency

Based on the analysis of this section, the experimental efficiency curves of the SEPIC prototype has been evaluated. In combination with the $f_{\text{sw}} = 250$ kHz scenario, described in appendix E.2.1, all combinations conducted in the laboratory has been evaluated. The measured peak efficiencies are summarised in table 6.6.

From the experimental peak efficiencies of table 6.6, it is observed that in all scenarios the coupled configuration of the SEPIC prototype exhibits a higher peak efficiency. This is to a large extent the same result as that of the analytical efficiency model from section 3.3.2. One caveat is that the analytical model showed that the uncoupled version could have better efficiency close to the 500 W limit when having a

Table 6.6 Measured peak efficiencies during of each conducted laboratory test.

	Uncoupled		**Coupled**	
V_{in} / f_{sw}	35 V	50 V	35 V	50 V
250 kHz	94.4%	94.3%	95.3%	96.8%
500 kHz	91.8%	92.0%	92.4%	92.4%

higher input voltage, as observed in figure 3.7b. However, the laboratory results were only evaluated up to a maximum of around 250 W, thus explaining this subtle difference. Thus, within the range up to 250 W, it is supported by both the experimental results as well as the analytical model, that the coupled version of the SEPIC exhibits a higher efficiency in all scenarios. Additionally the transient dynamics of the SEPIC are also evaluated experimentally by commanding a step in the duty-cycle and measuring the state response. This analysis is found in figure C.11, showing that the laboratory SEPIC prototype had a more damped response compared with the analytical small-signal model. This could suggest that the SEPIC prototype has more resistance in the circuit.

7 Discussion

This chapter serves to discuss the findings of the project. The purpose is to asses the findings, put them into perspective, and ultimately evaluate the credibility of each part.

The SEPIC topology was selected as the most suitable step-up-and-down topology. It is able to regulate the voltage up and down, it has a continuous input current, and also it has a non-inverting output voltage. Thus it is able to fulfil the requirements of the converter. However, from an analysis of the small-signal dynamics it is found that the SEPIC has quite complex dynamics including RHP zeros and 4^{th} order transfer functions. Furthermore it is found that the stresses on the semiconductors of the SEPIC topology are high. However, the alternative converter topologies presented in section 2.1 exhibit other, and perhaps more significant drawback such as inverting output, discontinuous input current etc. Thus in view of the analysed topologies, the SEPIC is perhaps the only viable option.

The implication of the inductors of the SEPIC was also analysed in this project. The SEPIC can be implemented with coupled- or uncoupled inductors. Through the analysis it was found that the coupled version of the SEPIC resulted in reduced volume due to the mutual inductance of each inductor. But when putting two windings on the same core in the SEPIC, the magnetic flux's sum together, resulting in a higher flux density in the core. On the other hand less turns are also needed due to the mutual inductance, and it was found that the maximum H-field in the coupled core was not much greater than the uncoupled core, as presented in table A.2. To maximise the mutual inductance a high coupling factor is convenient, and the interwinding capacitance does not pose a problem in the SEPIC because it is simply in parallel with either of the C_{in}- or C_1 capacitor. The ripple amplitude of the current in L_2 is not not subject to any requirement, making a small inductance seem acceptable, however the efficiency model (section 3.3.2) shows that core losses become excessive when L_2 is too small. Therefore, L_2 must be sufficiently large to limit losses, at which point the coupled version is more efficient regardless. On the other hand when L_1 and L_2 are coupled, the C_1 capacitance must be sufficiently large to ensure that the instantaneous voltage on each winding does not drift too far apart, which is not a limitation of the uncoupled version. Additionally, small-signal modelling showed that the coupled version exhibits improved damping.

For the python-based efficiency algorithm, the fundamental power loss equations were used to estimate the component losses. These equation, presented in section 3.1, are highly idealised and do not take into account parameter drifts due to: temperature, voltage, current, frequency etc. This is mitigated by extracting the data points from the datasheets of the semiconductors, as mentioned in section 3.3.2. Furthermore, the BH-curve of a magnetic material saturates after a certain point which results in a dropping inductance for high DC-bias currents. While this is implemented for the core loss computation it was not updating the current ripple amplitude, which means that when the core becomes saturated the ripple was not changed. This is problematic as the core L_2 would be saturated beyond 50% at full output current, as mentioned in appendix A.3.3, thereby the current ripple should have increased. While it is true that at high H-field magnitude the flux density amplitude is less, this simplification can skew the results by making the core losses less when the core is saturated. This also means that the results of the python-based loss estimation are unlikely to be very accurate in the high power range for the uncoupled version of the SEPIC. Nonetheless the python-based efficiency algorithm yielded the same tendency as those measured in the laboratory, indicating that the fundamental equation yield a good estimat of the tendency. This also includes comprehending what component parameters cause losses, and ultimately it can be used to determine efficient components.

The fundamental power loss equation were studied to identify ways of reducing power losses, especially in the semiconductors. To reduce power losses from the transistor, it was chosen to utilise a GaN HEMT because of their ability to reach very short switching periods, thus reducing switching losses. Additionally it is desirable to have as low on-resistance as possible to reduce conduction losses. Therefore the EPC2304 transistor was selected based on it being a GaN HEMT with just $R_{\mathrm{ds(on)}} = 5\,\mathrm{m\Omega}$ and $Q_{\mathrm{g}} = 21\,\mathrm{nC}$. However, the EPC2304 has relatively large output capacitance $C_{\mathrm{oss}} \approx 800\,\mathrm{pF}$ at $V_{\mathrm{ds}} = 100\,\mathrm{V}$, which caused the losses to be excessive at $f_{\mathrm{sw}} = 500\,\mathrm{kHz}$. Even in the scenario of $P = 25\,\mathrm{W}$ the transistor would reach 80 °C. As $R_{\mathrm{ds(on)}}$ increases with temperature the conduction losses become even worse at 500 kHz. While the EPC2304 is a top-side cooled device, it was attempted to cool the transistor through thermal vias. However, this proved to not be effective, yielding a thermal resistance estimated to be as high as $R_{\mathrm{th(HS\rightarrow\ A)}} = 24.9\,\frac{\mathrm{K}}{\mathrm{W}}$. This suggests that the EPC2304 was perhaps not an efficient choice in the context of this project. Thus to achieve a better thermal design a bottom-cooled GaN HEMT should be considered, with as low output capacitance as possible. But a lowered output capacitance tend to result in higher on-resistance, but as seen in figure 3.5 the switching losses are much more severe. This could enable testing the SEPIC prototype across the full power range, while also reducing temperature dependence and switching losses. Silicon-based transistor can have low on-resistance and output capacitance, but the switching times are for the most part prolonged due to increased Q_{g}. Thus silicon-based transistors are probably not suitable in view of $f_{\mathrm{sw}} = 500\,\mathrm{kHz}$.

Due to the limited project timeframe, a switching frequency of $f_{\mathrm{sw}} = 500\,\mathrm{kHz}$ was chosen without conducting a thorough optimisation study. This value formed the basis of the inductors and capacitors, to achieve the ripple amplitude requirements. Through laboratory testing of the SEPIC prototype, it was found that the peak efficiency at $f_{\mathrm{sw}} = 500\,\mathrm{kHz}$ reached just 92.4%. But testing with $f_{\mathrm{sw}} = 250\,\mathrm{kHz}$ yielded an experimental peak efficiency of 96.8%, as summarised in table 6.6, suggesting that the selected $f_{\mathrm{sw}} = 500\,\mathrm{kHz}$ is perhaps too high. However, given the achieved efficiency of 96.3%, it seems feasible to reach the $> 97\%$ target with a more optimal choice of switching frequency. Further improvements could be achieved by selecting a better-suited transistor and implementing synchronous rectification. On the other hand, selecting a lower switching frequency would require larger passive components which will possibly result in increased conduction losses and volume, thus the frequency can not be too low.

To analyse the closed-loop performance of the SEPIC, the small-signal state-space model was derived. It was shown that the small-signal dynamics of the SEPIC are quite complex, consisting of RHP zeros and 4^{th} order transfer functions. The small-signal dynamics were evaluate in lab, as presented in appendix C.5, where it was seen that the small-signal state-space model had some deviations. It was seen that the laboratory response was much better damped than the analytical state-space response. However, this is most likely an indication of additional resistance in the experimental prototype, which are dampening the resonances of the plant. In the analytical small-signal model, ideal components were considered. To more accurately model the real dynamics, one would have to include parasitic elements and resistances of each component. Additionally, resistances of PCB tracks, vias, connectors, wires, etc. would all need to be included. However, the analytical plant was used to design a type-II compensator, which through simulations resulted in satisfactory closed-loop regulation. This indicates that the small-signal state-space model was derived correctly, and could be used to compensate the loop. For each APR cell to operate in parallel, voltage mode control is not adequate hence a peak current-mode control scheme was analysed for the SEPIC. In the SEPIC the transistor current is the sum of each inductor current, where the ripple amplitude is therefore also added together. But in the average small-signal model, switching dynamics are omitted thus essentially revolving the mean inductor currents. But using peak current-mode control, means that the peak transistor current is regulated, and not the mean. However, the type-II compensator has a pole at origin, thus the DC error contributed from the ripple amplitude, is eliminated. Furthermore it was seen that the SEPIC control loop performance is capable of fulfilling the ECSS standard requirements, both in terms of static- and transient regulation. But it does require a

significantly large main bus capacitance. To implement peak current-mode control, requires the transistor current to be sensed and used as feedback. This raises concern in a construction utilising a GaN HEMT, because a current sensor in series with the transistor would add inductance in the power loop. Thus it can be argued that there is a point in which the transistor can have too fast switching periods, which would result in excessive voltage overshoot when implementing peak current-mode control in a SEPIC. Lastly it was seen from the coupled small-signal transfer function that there was a pair of complex poles and -zeros at high frequency, refer to appendix C.1.2, which had really low damping. But in the laboratory this high frequency content was not observed, but it was observed in the input current of the closed-loop simulation. This is perhaps due to using ideal components in the small-signal model and simulation, while in the lab there are parasitic resistances.

For the SEPIC prototype a mechanical frame was designed and manufactured throughout the project, as presented in section 6.1.1. The mechanical frame was designed in view of the maximum module volume specified by Terma A/S. This design and manufacturing took quite some time, and it can be argued that this was perhaps outside the scope of the project. However, the mechanical constraints set by the frame dimensions resulted in a more realistic analysis of the problem. Without the mechanical constraints, unrealistically large components could have been used thus resulting in less credible findings in view of the context. The volume constraints makes it necessary to have a high switching frequency to limit the size of the passive components, as well as the available heatsink area. Because of the mechanical frame, problems such as the thermal dissipation and passive sizes were exposed and analysed.

For the laboratory work a microcontroller was used to generate the PWM signal as well as realtime monitoring. In view of spaceflight this is perhaps not so realistic, however this was not the intent. The microcontroller was utilised for rapid prototyping, which allowed many different experimental tests to be performed. To implement a closed-loop system for spaceflight based around a microcontroller can be very risky, since a microcontroller has many different failure mechanisms. Typically a PWM controller is utilised, such as the control scheme presented in section 5.2. However, it must be addressed that commercially available PWM controllers are often made for silocon-based transistors, and a solution must be analysed to drive GaN HEMTs. Nonetheless the microcontroller could have been used to evaluate the peak current-mode control in the laboratory, however in the SEPIC prototype there was not implemented a sensor in the transistor path. This was to limit the parasitic inductance in the power loop, as described in appendix E.1.3. The power loop performanc was evaluated using a 500 MHz oscilloscope and a 200 MHz passive probe. In view of the power loop parasitics being in the range of a few nH and nF, it can be argued that higher bandwidth devices should have been utilised. Additionally a thermal camera was used to measure the component temperature. This is not quite the full picture, as this shows the hotspot temperature, and not the junction temperature. Additionally, the thermal images were taken in a fully lit laboratory with many people, thus emissivity effects could have caused further discrepancies.

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8 Conclusion

In this chapter the conclusions and findings of the project work are presented. The project objective was to evaluate the feasibility of a step-up-and-down topology in the context of an EPS on a spacecraft. To answer the formulated problem and objectives, the findings and insights gained are covered.

The SEPIC was identified as the most suitable step-up-and-down topology in view of an input PV source. The SEPIC exhibits a continuous input current, and a non-inverted output voltage. The large-signal transfer-ratio is the same as a traditional buck-boost, but with positive sign. The SEPIC consists of four passive components, resulting in rather complex system dynamics. One drawback of the SEPIC is the increased stress on the semiconductors, as they must withstand the sum of the input and output voltages and currents.

The efficiency potential of the SEPIC was assessed using a Python-based analytical power loss model and validated through a laboratory prototype. To achieve highest possible efficiency an EPC2304 GaN HEMT was utilised. Through laboratory testing a peak efficiency of 92.4% was measured at a switching frequency of 500 kHz, fulfilling the ripple requirements. Tests at a switching frequency of 250 kHz were also performed, reaching a peak efficiency of 96.8%, however not fulfilling the ripple requirements in that scenario. Both the python-based algorithm and the experimental tests proved that the SEPIC with coupled inductors exhibit a higher efficiency compared to the uncoupled version. The improved efficiency was due to reduced core losses when implemented on a common core, in combination with requiring less total number of turns because of the mutual inductance. To maximise mutual inductance a high coupling factor is desirable in the SEPIC, and any interwinding capacitance is in parallel with either the C_{in}- or C_1 capacitor, thus not raising concern. Moreover, it was found that higher input voltage would shift the point of peak efficiency to higher power levels, without altering the peak efficiency noticeably.

In view of the mechanical constraints of the APR module, a small PCB containing the semiconductors was designed and mounted directly on the side of the mechanical frame for best heat dissipation. In this regard it was found that the EPC2304 GaN HEMT was not suitable for bottom-cooling, resulting in high temperatures in the device, ultimately limiting the maximum power of the SEPIC prototype. Additionally it was found that the output capacitance of 800 pF was excessively high, resulting in excessive losses proving that the thermal design is a crucial part of enabling the SEPIC topology in practice.

Through small-signal modelling it was found that the power stage consists of RHP zeros, indicating that the control-loop can become unstable if not compensated properly. It was found that a type-II compensator could yield adequate control-loop performance reaching a maximum bandwidth of 8.9 kHz. Through closed-loop simulations it was proven that the SEPIC working with peak current-mode control is capable of fulfilling the ECSS standards regarding both static- and transient regulation. However, for the fast switching periods encountered in a GaN-based converter, the parasitic inductance of the current sensing techniques must be treated carefully in practice.

Given the achieved peak efficiency of 96.8%, it is expected that the SEPIC with coupled inductors could surpass 97% efficiency when using bottom-cooled GaN HEMTs with low output capacitance and an optimized switching frequency. Efficiency could be improved further by implementing synchronous transistors. In view of the aforementioned, the SEPIC utilising coupled inductors is concluded to be a suitable step-up-and-down APR topology.

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9 Future Work

This chapter serves to give a perspective on all the different parts of the project, with a focus on aspects that could be interesting to analyse further.

Perhaps the most relevant topic to analyse further is the capability of a SEPIC prototype with an improved thermal performance. This would require developing another version of the switch network PCB, where a bottom-cooled GaN HEMT device is implemented. The interesting things to asses here are how the thermal performance might improve, how it effect the overall system efficiency, and also evaluating if the directly mounting on the module side is an adequate solution. Additionally it could be interesting to asses and compare the performance of a radiation-hardened device.

It could also be very relevant to make a more thorough analysis of the switching frequency, ideally finding an optimal switching frequency resulting in the highest possible efficiency. This would require redesigning the passive components, and assessing at what point the passive components become to large, or when they result in too many losses. To this extent it could be interesting to develop another prototype designed for lower switching frequency, and see how it performs comparably.

Another topic that is important to analyse is the feasibility of synchronous rectification in the SEPIC. As outlined in section 3.4, the SEPIC is possible to implement with a high-side transistor. Here it can be assessed which high-side driving topology is most sufficient in terms of efficiency, reliability, and complexity. Ultimately it is relevant to access if the comprehensive efficiency can be further improved when using a synchronous high-side transistor.

It would also be insightful to asses the practical implementation of peak current-mode control in the SEPIC. This includes assessing the most efficienct current sensing technique in the transistor path, especially in view of the fast switching transients in a GaN-based SEPIC. To this regard it is also relevant to also analyse if GaN HEMTs can be run sufficiently with conventional PWM controllers, or if it requires a new solution. Furthermore, it is important to demonstrate that multiple SEPIC cells can operate in parallel, while regulating the same output bus.

It could also be interesting to analyse how the power loop could be further optimised. In this project a 4-layer PCB was used, where it was attempted to make the power loop path as small as possible, in an attempt to reduce the parasitic power loop inductance. Much research has already been done on the power loop of the half-bridge, however the SEPIC differs, and it could be interesting to determine the optimal solution. This could be achieved with testing different switch network PCB layouts, and evaluating the voltage overshoot and estimated power loop inductance.

Lastly it would be relevant to improve the python-based loss algorithm. An algorithm with better accuracy, could be handy especially in the design phase. To improve the algorithm, it could be relevant to implement temperature dependency, skin effect, dynamic inductances as a function of DC bias, barometric impacts, and even radiation impacts.

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Bibliography

[1] Julia Seibert. The benefits of space exploration and its importance, 2024. https://spaceinsider.tech/2024/03/14/the-benefits-of-space-exploration-and-its-importance/.

[2] European Space Agency. What is electric propulsion? https://www.esa.int/Enabling_Support/Space_Engineering_Technology/What_is_Electric_propulsion.

[3] D. O'Sullivan. Space power electronics - design drivers. *EPE Journal*, Issue 2, 1993.

[4] Hans Jensen and Johnny Laursen. Power conditioning unit for rosetta / mars express. *Space Power*, 2002.

[5] Ferdinando Tonicello. Electrical & electronics background reading, 2021. https://ecss.nl/wp-content/uploads/2021/09/STC_21-P-Electrical-and-Electronic_background_reading.pdf.

[6] ECSS. *Space Engineering - Electrical and electronic*, 2022. ECSS-E-ST-20C Rev.2, 8. april.

[7] Ned Mohan, Tore M. Undeland, and William P. Robbins. *Power Electronics: Converters, Applications, and Design*. John Wiley & Sons, 2nd edition, 2003.

[8] Grant Bonin ad Nathan Orr, Robert E. Zee, and Jeff Cain. Esd triggered solar array failure mechanism. Technical report, UTIAS Space Flight Laboratory and Com Dev Ltd, 2000.

[9] Ira Katz, David B. Snyder, and Ernest A. Robertson. Esd triggered solar array failure mechanism. Technical report, NASA, 2000.

[10] Azur Space GmbH. Space solar cells. https://www.azurspace.com/index.php/en/products/products-space/space-solar-cells.

[11] Hans Jensen and colleagues. Senior electrical engineer. Terma A/S - Space Systems.

[12] Muhammad H. Rashid. *Power Electronics: Devices, Circuits, and Applications*. Pearson, 4th edition, 2014.

[13] Asger B. Jørgensen. Derivation, design and simulation of the single-ended primary-inductor converter (sepic). Technical report, Aalborg University, May 2019.

[14] Robert W. Erickson and Dragan Maksimovic. *Fundamentals of Power Electronics*. Springer, 3rd edition, 2020.

[15] H. Barde, A. Fernández, S. Taylor, K. Stephenson, and M. Schautz. Electrical power systems basics, 2016.

[16] Claudio Adragna. A primer to transformers and coupled inductors modeling. Technical report, STMicroelectronics, 2007.

[17] J. Garcia. Losses in power diodes.

[18] Henry W. Ott. *Electromagnetic Compatibility Engineering*. John Wiley & Sons, 1st edition, 2009.

[19] Alex Lidow, Tony Marini, Stefano Michelis, David Reusch, Robert Strittmatter, and Max Zafrani. Gan in space. EPC Space.

[20] Efficient Power Conversion, https://epc-co.com/epc/products/gan-fets-and-ics/epc2304. *EPC2304: 200 V, 260 A Enhancement Mode GaN Power Transistor*.

[21] Texas Instruments, https://www.ti.com/product/UCC27611. *UCC27611*. Gate driver datasheet and product information.

[22] Vishay, https://www.vishay.com/en/product/87158/. *V30K202 PRODUCT INFORMATION*. Schottky Diode.

[23] Magnetics Inc., https://www.mag-inc.com/Media/Magnetics/Datasheets/0074083A7.pdf. *0074083A7*. Xflux Ultra Toroid Core.

[24] Magnetics Inc., https://www.mag-inc.com/Media/Magnetics/Datasheets/0059050A2.pdf. *0059050A2*. Edge Toroid Core.

[25] TDK, https://product.tdk.com/system/files/dam/doc/product/capacitor/ceramic/mlcc/catalog/mlcc_automotive_midvoltage_en.pdf. *MULTILAYER CERAMIC CHIP CAPACITORS*. CGA Series datasheet.

[26] TDK, https://www.tdk-electronics.tdk.com/inf/20/20/db/fc_2009/B32520_529.pdf. *Metallized Polyester Film Capacitors (MKT)*. B32524 datasheet.

[27] Charles L. Phillips and John M. Parr. *feedback Control Systems*. Pearson Education Inc., 5 edition, 2011.

[28] Texas Instruments, https://www.ti.com/product/UC1843. *UC1843*. PWM controller datasheet and product information.

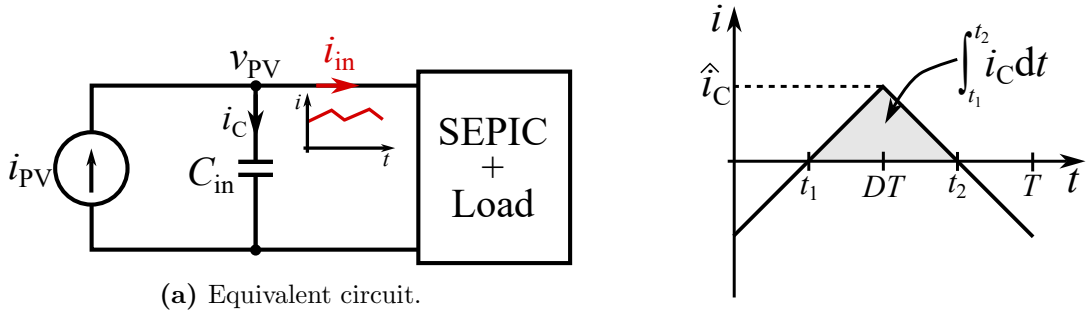
[29] Bainan Sun, Kasper Lüthje Jørgensen, Zhe Zhang, and Michael A.E. Andersen. Research of power loop layout and parasitic inductance in gan transistor implementation. *IEEE Transactions on Industry Applications*, 2021.

[30] Würth Elektronik. Würth elektronik webinar: Using current sense transformers. https://www.youtube.com/watch?v=WUz91I69zWE.

A Additional Modelling

A.1 Input Current Ripple Derivation

The idea is that the input capacitor, C_{in}, act as a decoupling capacitor, that is sinking/sourcing the ripple current. With this assumbtion the PV source will be a constant current. This scenario is illustrated in figure A.1.



(a) Equivalent circuit.

(b) Capacitor current.

Figure A.1 Illustration of the input capacitor decoupling.

Firstly the capacitor equation can be expanded as seen in equation (A.1).

$$i_{\text{c}} = C_{\text{in}} \frac{\text{d}v}{\text{d}t} \quad = \quad \Delta V = \frac{1}{C_{\text{in}}} \int i_{\text{c}} \text{d}t \tag{A.1}$$

As illustrated in figure A.1b the capacitor charge area can be approximated by a triangle. Therefore the relation between the current ripple and the voltage ripple can be derived as presented in equation (A.2).

$$\Delta V_{\text{C}} \approx \frac{1}{C_{\text{in}}} \frac{1}{2} \frac{T}{2} \frac{\Delta I_{\text{in}}}{2} = \frac{\Delta I_{\text{in}} \cdot T}{8 \cdot C_{\text{in}}}$$

$$\Delta I_{\text{in}} \approx 8 \Delta V_{\text{C}} \cdot C_{\text{in}} \cdot f_{\text{sw}} \tag{A.2}$$

Moreover, from equation (A.1) it is observed that the voltage derivative is proportional to the current magnitude. Therefore the input voltage ripple waveform can easiliy be comprehended, resulting in figure A.2.

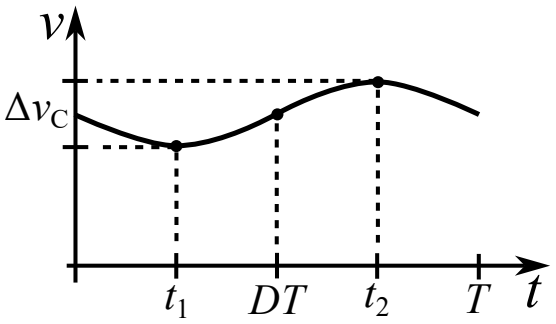
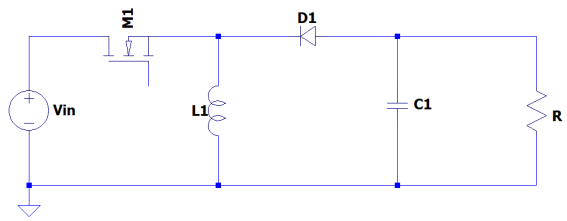


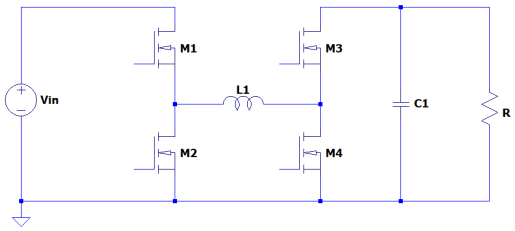
Figure A.2 Input voltage ripple waveform.

A.2 Step-up-and-down Converter Topologies

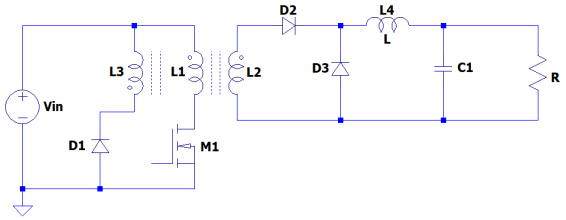
In this section the schematics of the listed step-up-and-down topologies listed in table 2.2 are presented. Tese schematics are shown in figure A.3.



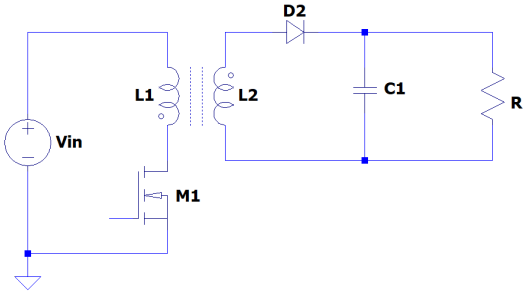
(a) Conventional buck-boost.



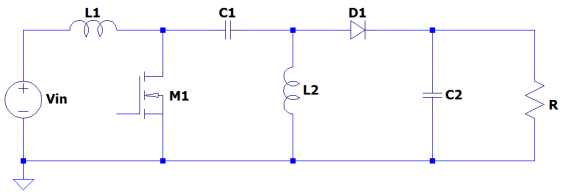
(b) 4-switch buck boost.



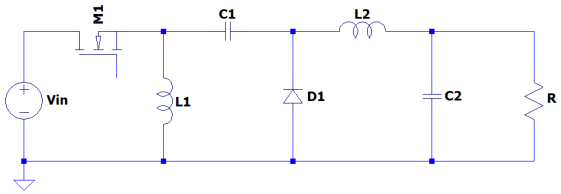
(c) Forward.



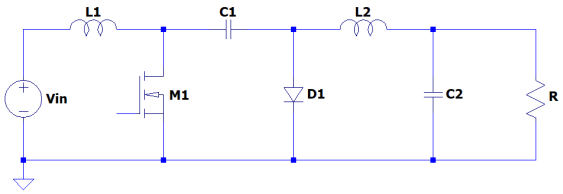
(d) Flyback.



(e) SEPIC.



(f) Zeta.



(g) Cúk.

Figure A.3 Schematics of possible step-up-and-down topologies [14] [12] [7].

Note from figures A.3e and A.3f that the Zeta is simply the inverse of the SEPIC. Thus a synchronous SEPIC is also a bidirectional topology

A.3 SEPIC Inductor Design

As presented in section 2.5, the SEPIC can have the inductors, L_1 and L_2, coupled on the same core. In this section the practical design process of the inductors in the SEPIC is covered. In section 2.3 it was computed that the inductances should be: $L_1 \geq 166.67\,\mu H$ and $L_2 \geq 33.33\,\mu H$ to fulfil the ripple requirements at a switching frequency of 500 kHz.

For L_1 a 0074083A7 toroid core is selected, and for L_2 the smaller 0059050A2 toroid core is used, both

manufactured by Magnetics Inc. For the coupled inductors scenario the same core as for an independent L_1 (the 0074083A7 toroid core) is used. Selection of the specific magnetic cores resulted from a concurrent design approach, balancing module size constraints, saturation limits, copper usage minimisation, and commercial availability. The data of each core is presented in table A.1.

Table A.1 Parameters magnetic cores [23] [24].

Parameter	**0074083A7**	**0059050A2**
Inductance factor, A_L	$82\,\frac{\mathrm{nH}}{\mathrm{turns}^2}$	$56\,\frac{\mathrm{nH}}{\mathrm{turns}^2}$
Initial rel. permeability, μ_i	60	125
Saturation flux density, B_sat	1.6 T	1.5 T
Effective path length, l_e	98.5 mm	31.2 mm
80% DC bias H-field, $H_{80\%}$	90 Oe	55 Oe
50% DC bias H-field, $H_{50\%}$	160 Oe	90 Oe
Outer diameter, OD	40.77 mm	13.46 mm

A.3.1 Design of Coupled Inductors for the SEPIC

For the coupled SEPIC topology the mutual inductance, M, is adding on to the self-inductances. This is given by equation (2.49), where it is observed that the effective inductance is the sum of the self-inductance and the mutual inductance. In the SEPIC, interwinding capacitance is in parallel with the capacitor C_1 or C_in, so tightly coupling the inductors in the SEPIC is a benefit. Tightly coupling of inductor mean that the coupling factor, k, becomes very close to unity. Thus expanding on the definition of the mutual inductance, presented in equation (2.52), results in equation (A.3).

$$M = k\sqrt{L_1 L_2} \approx L_1 = L_2 \tag{A.3}$$

Thus, for a coupling factor near unity, the sum of the self-inductance and mutual inductance, yield that the self-inductance of each winding is doubled. Thus for the coupled SEPIC inductors, each winding should aim for a self-inductance of:

$$L_\mathrm{ref} = \frac{166.67\,\mu\mathrm{H}}{2} = 83.33\,\mu\mathrm{H}$$

The value 166.67 µH is used because L_1 is required to have the largest inductace. Since the volt-sec balance on each inductor is the same in the SEPIC, the turns-ratio of the SEPIC must be unity. This means that the number of turns on the secondary must be the same as the primary, that is: $N = n_1 = n_2$. Effectively yielding that the self-inductance on each winding will be the same, as seen in equation (A.4)

$$L_1 = \frac{\mu \cdot A_\mathrm{c}}{l_\mathrm{e}} \cdot {n_1}^2 = \frac{\mu \cdot A_\mathrm{c}}{l_\mathrm{e}} \cdot {n_2}^2 = L_2 \tag{A.4}$$

The required number of turns are computed with the inductance factor of table A.1 as presented in equation (A.5).

$$N = \sqrt{\frac{L_\mathrm{ref}}{A_\mathrm{L}}} = \sqrt{\frac{\frac{166.67\,\mu\mathrm{H}}{2}}{82\,\frac{\mathrm{nH}}{\mathrm{turns}^2}}} = 31.88 \tag{A.5}$$

Thereby, $\lceil N \rceil = 32$.

The maximum current capability is given as $I_{\mathrm{L1,\,max}} = 14.3\,\mathrm{A}$ and $I_{\mathrm{L2,\,max}} = 10.0\,\mathrm{A}$ in the $V_\mathrm{in} = 35\,\mathrm{V}$ scenario, as given by table 2.3. In a coupled core, the H-field is given by the sum of each winding, as given by equation (2.53). Thereby utilising the effective path length, l_e, the number of turns, N, and the peak currents, $I_{\mathrm{L1,\,max}}$ and $I_{\mathrm{L2,\,max}}$, the H-field at maximum current is computed as presented in equation (A.6).

$$H_{\mathrm{max,\,coupled}} = \frac{32 \cdot 14.3\,\mathrm{A} + 32 \cdot 10.0\,\mathrm{A}}{98.5\,\mathrm{mm}} = 99.2\,\mathrm{Oe} \tag{A.6}$$

Comparing equation (A.6) with the saturation data of table A.1, it is seen that at full current the coupled core will have a little less than 80% of the inductance. Thus validating the design, in view of slight saturation at full current. Using an ampacity of $J = 800\,\frac{\mathrm{A}}{\mathrm{cm}^2}$, the wire diameter must be at least 1.7 mm for the L_1 winding, and at least 1.3 mm for the L_2 winding [12].

A.3.2 Design of Uncoupled Inductors for the SEPIC

For the uncoupled inductors there is next to no mutual inductance, that is $M \approx 0$. Therefore the required number of turns can be computed directly from the the self-inductance based on the inductance factor of each core. This is computed in equations (A.7) and (A.8).

$$N_{\mathrm{L1}} = \sqrt{\frac{166.67\,\mu\mathrm{H}}{82\,\frac{\mathrm{nH}}{\mathrm{turns}^2}}} = 45.1 \tag{A.7}$$

$$N_{\mathrm{L2}} = \sqrt{\frac{33.33\,\mu\mathrm{H}}{52\,\frac{\mathrm{nH}}{\mathrm{turns}^2}}} = 25.32 \tag{A.8}$$

Therefore $\lceil N_{\mathrm{L1}} \rceil = 46$ and $\lceil N_{\mathrm{L2}} \rceil = 26$. The maximum current capability is given as $I_{\mathrm{L1,\,max}} = 14.3\,\mathrm{A}$ and $I_{\mathrm{L2,\,max}} = 10.0\,\mathrm{A}$ in the $V_{\mathrm{in}} = 35\,\mathrm{V}$ scenario, as given by table 2.3. Thus the H-field of each core can be computed as presented in equations (A.9) and (A.10).

$$H_{\mathrm{max,\,L1}} = \frac{46 \cdot 14.3\,\mathrm{A}}{98.5\,\mathrm{mm}} = 83.92\,\mathrm{Oe} \tag{A.9}$$

$$H_{\mathrm{max,\,L2}} = \frac{26 \cdot 10.0\,\mathrm{A}}{13.46\,\mathrm{mm}} = 104.72\,\mathrm{Oe} \tag{A.10}$$

Comparing the results of equations (A.9) and (A.10) to the saturation values in table A.1 it is seen that the maximum H-field at full current for the core of L_1 results in very slight saturation, with less than 10% drop in the inductance. On the other hand it is seen that the maximum H-field at full current for the core of L_2 results in a drop in inductance of more than 50%. This will result in a current ripple amplitude that is doubled. However the ripple on L_2 is not critical at it will be filtered by the output capacitors.

A.3.3 Summary of Designed Inductor Specifications

From the computed values of appendices A.3.1 and A.3.2 the results are summarised in table A.2.

Table A.2 Computed values from the inductor design procedure.

Parameter	**Coupled**		**Uncoupled**	
	1 (L_1)	2 (L_2)	L_1	L_2
Number of turns, N	32	32	46	26
Max H-field, H_{max}	99.2 Oe		83.92 Oe	104.72 Oe
Wire Diameter, D_{wire}	$\geq 1.7\,\mathrm{mm}$	$\geq 1.3\,\mathrm{mm}$	$\geq 1.7\,\mathrm{mm}$	$\geq 1.3\,\mathrm{mm}$

From the values of table A.2, it is clear that the coupled topology required less total number of turns (64 vs 72). This will likely result in higher resistance in the uncoupled version of the SEPIC. Furthermore it is found that at maximum current the L_2 inductor core is driven far out into saturation. This will cause very high current ripple amplitude, which in turn will mean that the hysteresis losses on L_2 will be considerable. On the other hand, the further out into saturation a magnetic material is, the less flux density ripple it will have.

A.3.4 Experimental Evaluation of the Inductors

To evaluate the performance of the inductors, 3 type of tests are performed. Firstly an LCR-meter is used as seen in figure A.4.

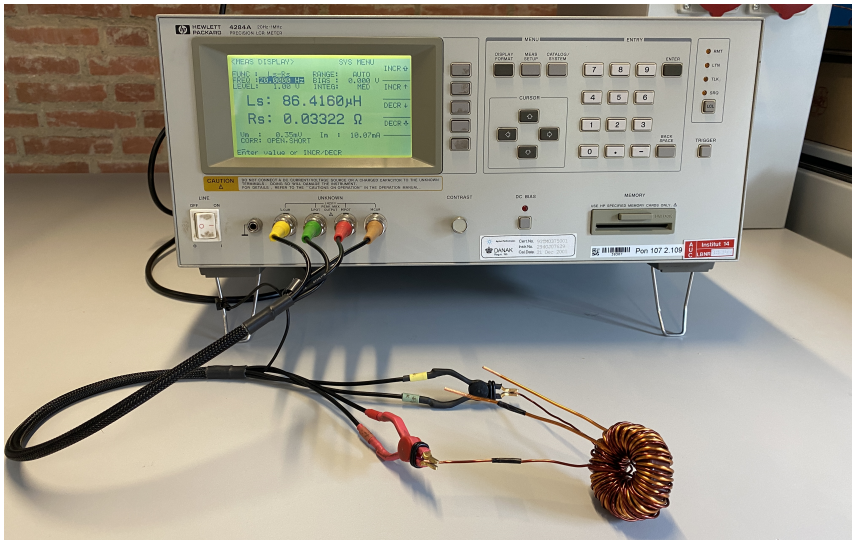
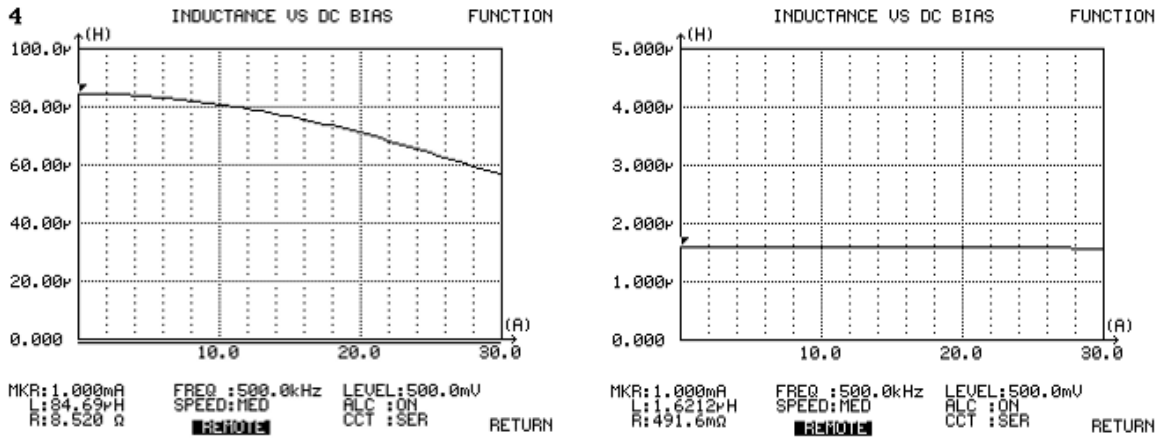


Figure A.4 LCR meter to measure the inductance and series resistance of the coupled inductor.

In figure A.4 the coupled inductor is also observed physically. Secondly a power analyser is also used to measure the DC-bias response of the coupled inductor. The results of evaluating the inductance with an applied DC bias is presented in figure A.5.



(a) Open-circuit secondary.

(b) Short-circuit secondary.

Figure A.5 DC bias curves of the coupled inductor.

In the case of an open-circuit secondary, one will essentially measure the series resistance and self-inductance. When the secondary is short-circuited then the leakage inductance will be measured. This is clear from the equivalen circuit of the coupled inductor, presented in section 2.5.1. From the DC-bias curve in figure A.5a the roll-off is clearly identified in the inductor core. On the other hand the leakage inductance of figure A.5b barely changes as a function of DC current. This makes sense because the magnetic flux path of the leakage is through aim, thus increasing the reluctance considerable, shifting the saturation point to very high H-field value.

Lastly an impedance analyser setup is also used to measure the frequency response of the inductor. The impedance analyser setup is shown in figure A.6.

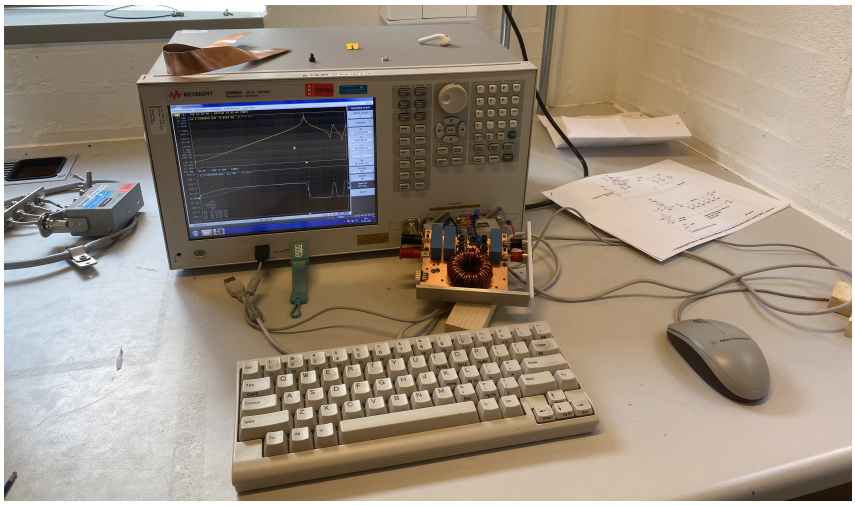
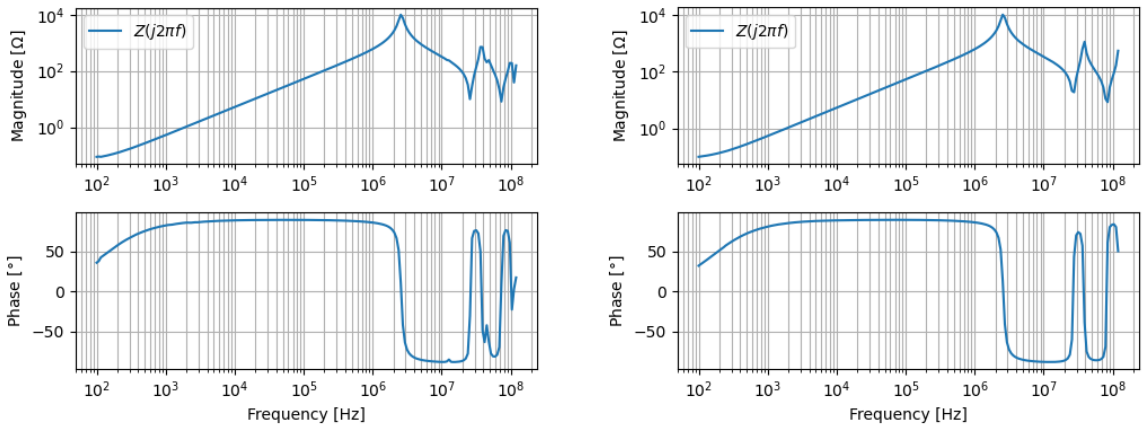


Figure A.6 Impedance analyser used to measure the inductor frequency response.

Using the impedance analyser, the coupled inductor is swept in frequency with open-circuit, and short-circuited secondary. The frequency response of the coupled inductor on the PCB is presented in figure A.7.



(a) Primary with secondary O.C.

(b) Secondary with primary O.C.

Figure A.7 Frequency response of the coupled inductor.

From the frequency response many parameters can be determined. Most importantly from the frequency response it is seen that the resonance peak of the primary and secondary occurs at 2.56 MHz. By combining the results from the LCR-meter, the DC-bias test, and the frequency response, the parameters of the inductors are obtained as presented in table A.3. If the secondary winding is short-circuited, it can be derived from the equivalent circuit, presented in section 2.5.1, that the coupling factor is as presented in equation (A.11).

$$L_{\text{oc}} = L_1 - M + M = L1$$

$$L_{\text{sc}} = (L_1 - M) + M||(L_2 - M) = L_1(1 - k^2)$$

By combining the above:

$$k = \sqrt{1 - \frac{L_{sc}}{L_{oc}}} \tag{A.11}$$

From the open-circuit and shot-circuit inductances of table A.3 it is computed via equation (A.11) that the coupling factor in practice is 0.99.

Table A.3 Measured parameters of the laboratory inductors

Parameter	**Coupled**		**Uncoupled**	
	Prim. (L_1)	Sec. (L_2)	L_1	L_2
Self-inductance, L_{sc}	83.3 µH	86.4 µH	170.4 µH	33.9 µH
Series resistance, R_s	15.5 Ω	33.2 Ω	42.8 Ω	22.32 Ω
Leakage inductance, L_{oc}	1.26 µH	1.62 µH	N/A	N/A
Resonance frequency, f_r	2.56 MHz	2.56 MHz	N/A	N/A

From the values of table A.3, it is observed that the self-inductances yield the reference inductance. This validates that the design procedure was correct.

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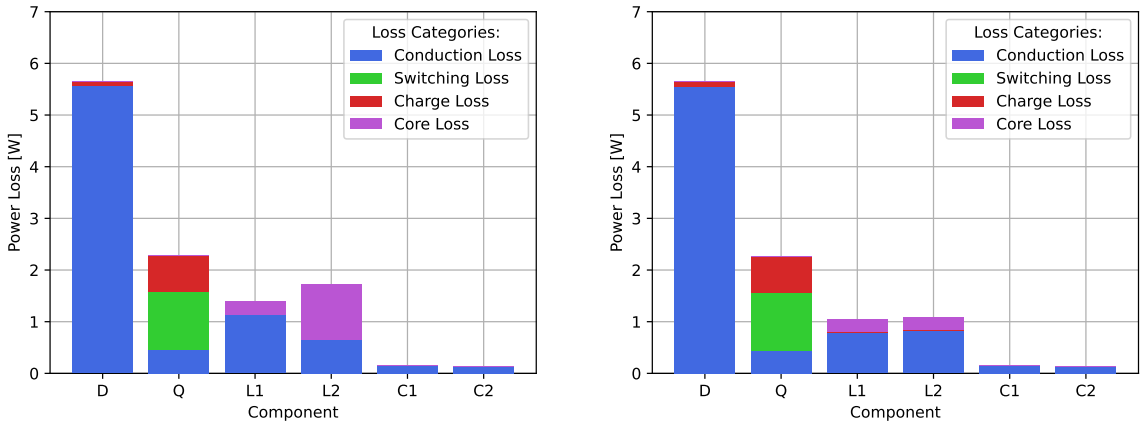
B Additional Efficiency Model Plots

B.1 Estimated Power Loss of the SEPIC at 250 kHz Switching Frequency

In this part of the appendix, the distribution of power losses are presented at $f_{sw} = 250\,\text{kHz}$.

B.1.1 Estimated Power Loss of the SEPIC at 35V Input Voltage

In this scenario the operational parameters are: $V_{in} = 35\,\text{V}$, $f_{sw} = 250\,\text{kHz}$, and $P = 250\,\text{W}$. The distribution of power losses are presented in figure B.1.



(a) Uncoupled SEPIC.

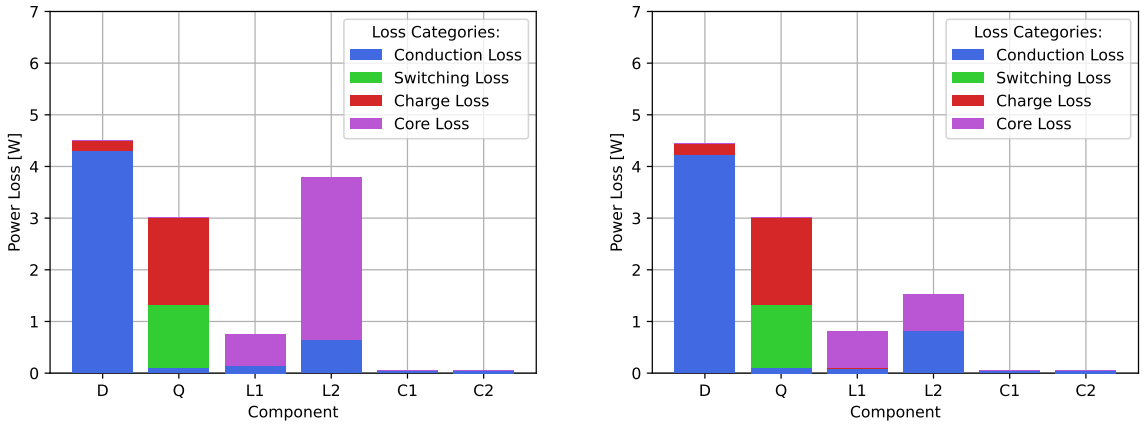
(b) Coupled SEPIC.

Figure B.1 Estimated distribution of power losses an input voltage of $V_{in} = 35\,\text{V}$ and switching frequency of 250 kHz.

The total power losses are 11.33 W and 10.30 W for the uncoupled- and coupled topology, respectively.

B.1.2 Estimated Power Loss of the SEPIC at 100V Input Voltage

In this scenario the operational parameters are: $V_{\text{in}} = 100\,\text{V}$, $f_{\text{sw}} = 250\,\text{kHz}$, and $P = 250\,\text{W}$. The distribution of power losses are presented in figure B.2.



(a) Uncoupled SEPIC. **(b)** Coupled SEPIC.

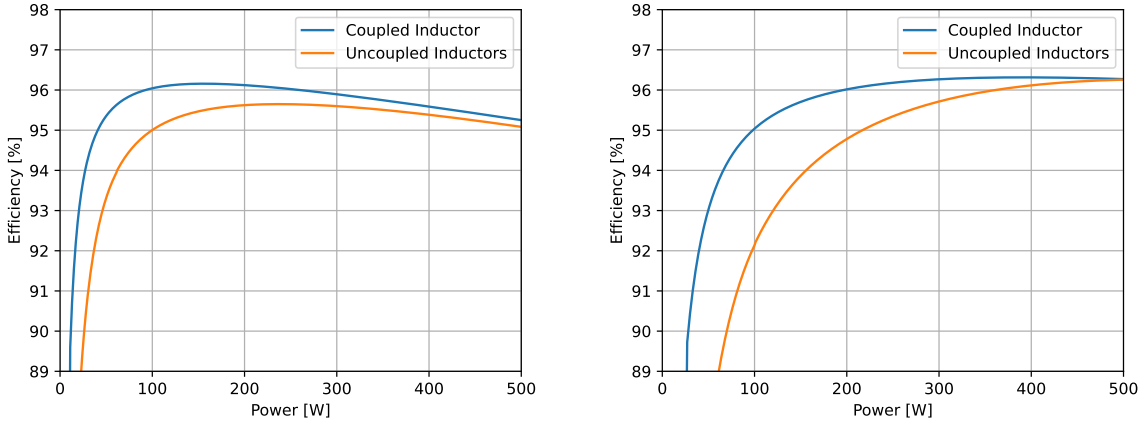
Figure B.2 Estimated distribution of power losses an input voltage of $V_{\text{in}} = 35\,\text{V}$ and switching frequency of 250 kHz.

The total power losses are 12.17 W and 9.89 W for the uncoupled- and coupled topology, respectively.

B.2 Analytical Efficiency Curves of the SEPIC at 250 kHz Switching Frequency

B.2.1 Estimated Efficiency of the SEPIC with Uncoupled- and Coupled Inductors

The efficiency of the SEPIC with a switching frequency of 250 kHz is presented in figure B.3.



(a) $V_{\text{in}} = 35\,\text{V}$ scenario. **(b)** $V_{\text{in}} = 100\,\text{V}$ scenario.

Figure B.3 Efficiency profiles of uncoupled- and coupled versions of the SEPIC with a switching frequency of 250 kHz.

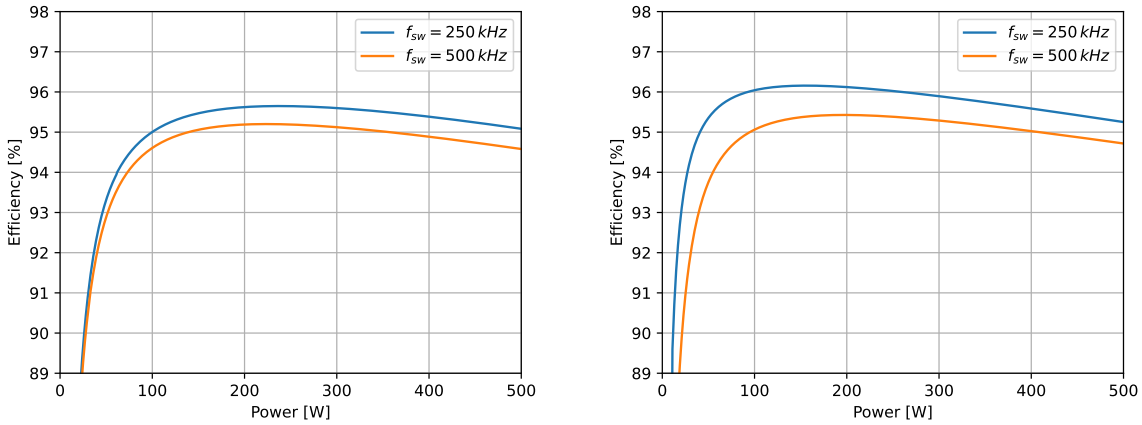
The peak efficiencies and the power at which they occur are summarised in table B.1.

Table B.1 Peak efficiency points on the power curve of the SEPIC with uncoupled- and coupled inductors at a switching frequency of 250 kHz.

Parameter	**Uncoupled**		**Coupled**	
Input voltage, V_{in}	35 V	100 V	35 V	100 V
Peak efficiency, $\hat{\eta}$	95.65%	96.26%	96.16%	96.31%
Power level, P	238 W	500 W	156 W	391 W

B.2.2 Estimated Efficiency of the SEPIC with at Different Switching Frequency

In this subsection the impact of different switching frequency of 250 kHz and 500 kHz is directly compared. The efficiency curve for the SEPIC with uncoupled inductors is presented in figure B.4.



(a) Uncoupled inductors.

(b) Coupled inductors.

Figure B.4 Efficiency profiles of uncoupled- and coupled versions of the SEPIC with a switching frequency of 250 kHz.

The mean efficiency increase across each power level is $0.43\%_{pp}$ and $0.99\%_{pp}$ for the uncoupled- and coupled versions of the SEPIC, respectively. This indicates that the efficiency could perhaps be improved even further by using a lower switching frequency. However, this would require a redesign of the SEPIC component sizes which migh in turn increase other losses.

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C SEPIC Control

C.1 Transfer Function and Pole-Zero Behaviour of the SEPIC Power Stage

This part revolves around the frequency-domain behaviour of the SEPIC. This is evaluated for the uncoupled SEPIC in appendix C.1.1, and for the coupled in appendix C.1.2. Both scenarios consider operational parameters of: $P = 500\,\mathrm{W}$, $V_{\mathrm{in}} = 35\,\mathrm{V}$, and $V_{\mathrm{out}} = 50\,\mathrm{V}$. The resulting responses are computed with the small-signal python script, as presented in appendix F.2.

C.1.1 SEPIC with Uncoupled Inductors

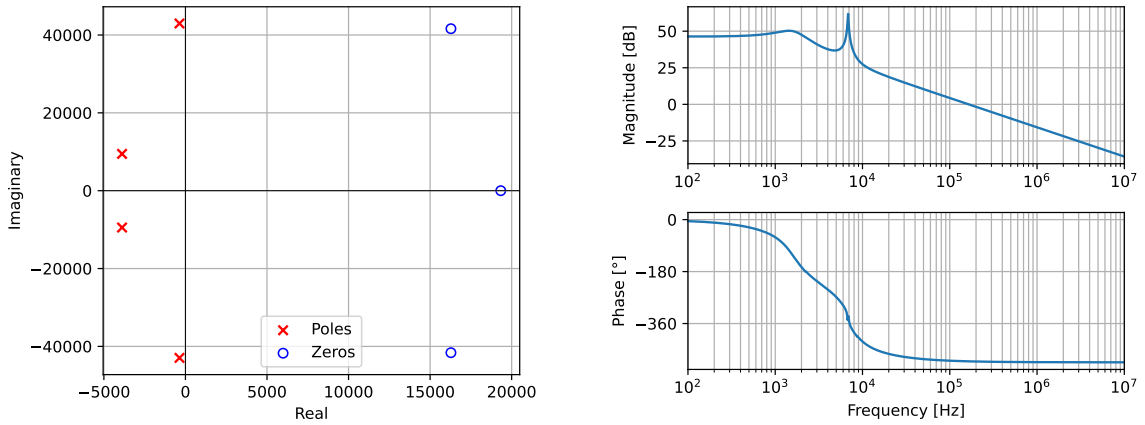
In this subsection the input-to-output transfer functions associated with the uncoupled SEPIC are derived and analysed.

Voltage Mode Control Power Stage

Using the input-to-output state transfer function, presented in equation (4.5), the voltage control plant of the uncoupled SEPIC is derived as equation (C.1).

$$G_{\mathrm{vd}}(s) = \frac{\tilde{v}_{\mathrm{C2}}}{\tilde{d}} = \frac{-1.032 \times 10^{6} s^{3} + 5.355 \times 10^{10} s^{2} - 2.711 \times 10^{15} s + 3.985 \times 10^{19}}{s^{4} + 8500 s^{3} + 1.956 \times 10^{9} s^{2} + 1.442 \times 10^{13} s + 1.93 \times 10^{17}} \tag{C.1}$$

The pole-zero map and the frequency response of equation (C.1) are presented in figure C.1.



(a) Pole-zero map.

(b) Frequency response.

Figure C.1 Frequency domain plots of the Voltage Mode Control Power Stage, from equation (C.1).

The poles and zeros of equation (C.1) are presented in table C.1.

Table C.1 Poles and zeros of equation (C.1)

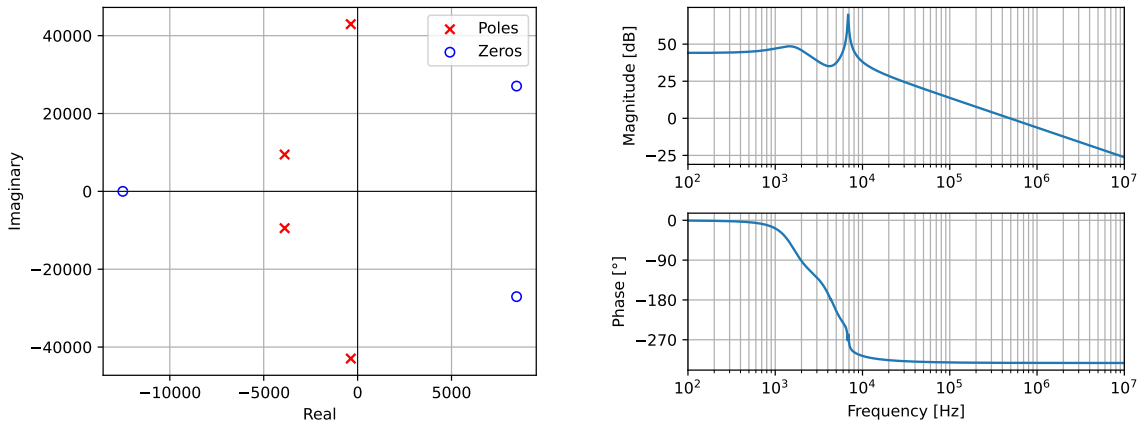
Parameter	Location	Frequency	Angle	Damping
Zero 1	$16.28 \times 10^3 \pm j41.62 \times 10^3$	7.1 kHz	$\pm 68.64°$	0.36
Zero 2	19.33×10^3	3.1 kHz	$0°$	1
Pole 1	$-364.17 \pm j42.96 \times 10^3$	6.8 kHz	$\pm 90.64°$	0.0085
Pole 2	$-3885.73 \pm j9460.28$	1.6 kHz	$\pm 112.33°$	0.38

Current Control Power Stage - Inner loop

Using the input-to-output state transfer function, presented in equation (4.5), the current mode inner control loop plant of the uncoupled SEPIC is derived as equation (C.2).

$$G_{\mathrm{id}}(s) = \frac{\tilde{i}_{\mathrm{L1}} + \tilde{i}_{\mathrm{L2}}}{\tilde{d}} = \frac{3.06 \times 10^6 s^3 - 1.354 \times 10^{10} s^2 + 1.811 \times 10^{15} s + 3.074 \times 10^{19}}{s^4 + 8500 s^3 + 1.956 \times 10^9 s^2 + 1.442 \times 10^{13} s + 1.93 \times 10^{17}} \tag{C.2}$$

The pole-zero map and the frequency response of equation (C.2) are presented in figure C.2.



(a) Pole-zero map.

(b) Frequency response.

Figure C.2 Frequency domain plots of the current-mode control inner-loop power stage, from equation (C.2).

The poles and zeros of equation (C.2) are presented in table C.2.

Table C.2 Poles and zeros of equation (C.2)

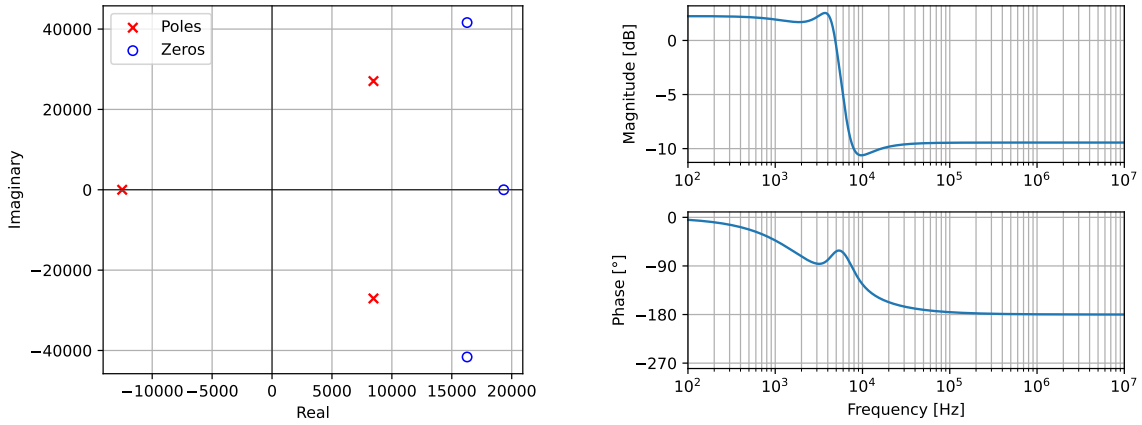
Parameter	Location	Frequency	Angle	Damping
Zero 1	$8.46 \times 10^3 \pm j27.05 \times 10^3$	4.5 kHz	$\pm 72.62°$	0.29
Zero 2	-12.50×10^3	1.99 kHz	$-180°$	1
Pole 1	$-364.17 \pm j42.96 \times 10^3$	6.8 kHz	$\pm 90.64°$	0.0085
Pole 2	$-3885.73 \pm j9460.28$	1.6 kHz	$\pm 112.33°$	0.38

Current Control Power Stage - Outer loop

The outer loop portion of the power stage is derived based on equation (C.1) and equation (C.2) as presented in equation (4.10). Thus it is derived as presented in equation (C.3).

$$G_{\text{vi}}(s) = \frac{G_{\text{vd}}(s)}{G_{\text{id}}(s)} = \frac{\tilde{v}_{\text{C2}}}{\tilde{i}_{\text{L1}} + \tilde{i}_{\text{L2}}} = \frac{-0.337s^3 + 1.75 \times 10^4 s^2 - 8.86 \times 10^8 s + 1.302 \times 10^{13}}{s^3 - 4425s^2 + 5.917 \times 10^8 s + 1.004 \times 10^{13}} \tag{C.3}$$

The pole-zero map and the frequency response of equation (C.3) are presented in figure C.3.



(a) Pole-zero map.

(b) Frequency response.

Figure C.3 Frequency domain plots of the current-mode control outer-loop power stage, from equation (C.3).

The poles and zeros of equation (C.3) are presented in table C.3.

Table C.3 Poles and zeros of equation (C.3)

Parameter	Location	Frequency	Angle	Damping
Zero 1	$16.28 \times 10^3 \pm j41.62 \times 10^3$	7.1 kHz	$\pm 68.64°$	0.36
Zero 2	19.33×10^3	3.1 kHz	$0°$	1
Pole 1	$8.46 \times 10^3 \pm j27.05 \times 10^3$	4.5 kHz	$\pm 72.62°$	0.29
Pole 2	-12.50×10^3	1.99 kHz	$-180°$	1

C.1.2 SEPIC with Uncoupled Inductors

In this subsection the input-to-output transfer functions associated with the coupled SEPIC are derived and analysed.

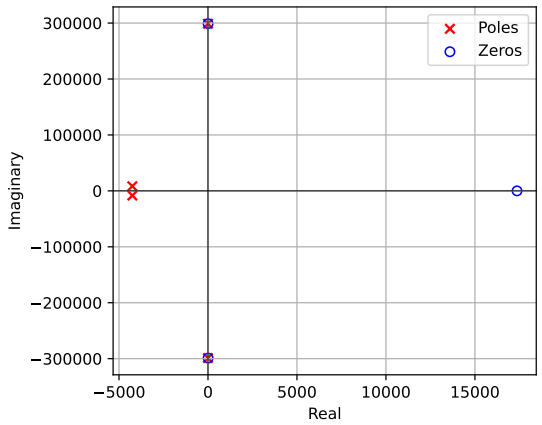
Voltage Mode Control Power Stage

Using the input-to-output state transfer function, presented in equation (4.5), the voltage control plant of the coupled SEPIC is derived as equation (C.4).

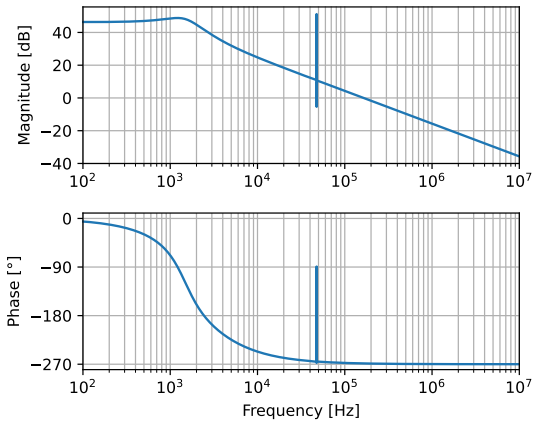
$$G_{\text{vd}}(s) = \frac{\tilde{v}_{\text{C2}}}{\tilde{d}} = \frac{-1.032 \times 10^6 s^3 + 1.394 \times 10^{10} s^2 - 9.223 \times 10^{16} s + 1.602 \times 10^{21}}{s^4 + 8500s^3 + 8.938 \times 10^{10} s^2 + 7.59 \times 10^{14} s + 7.76 \times 10^{18}} \tag{C.4}$$

The pole-zero map and the frequency response of equation (C.4) are presented in figure C.4.

The poles and zeros of equation (C.4) are presented in table C.4.



(a) Pole-zero map.



(b) Frequency response.

Figure C.4 Frequency domain plots of the voltage mode control power stage, from equation (C.4).

Table C.4 Poles and zeros of equation (C.4)

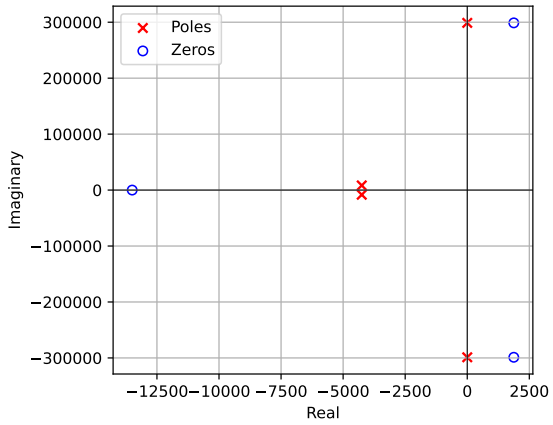
Parameter	Location	Frequency	Angle	Damping
Zero 1	$7.67 \pm j298.94 \times 10^3$	47.56 kHz	$\pm 89.996°$	2.57×10^{-5}
Zero 2	17.37×10^3	2.76 kHz	$0°$	1
Pole 1	$-0.648 \times 10^{-3} \pm j298.83 \times 10^3$	47.56 kHz	$\pm 90.00°$	2.17×10^{-9}
Pole 2	$-4.25 \times 10^3 \pm j8296.14$	1.48 kHz	$\pm 117.12°$	0.456

Current Control Power Stage - Inner loop

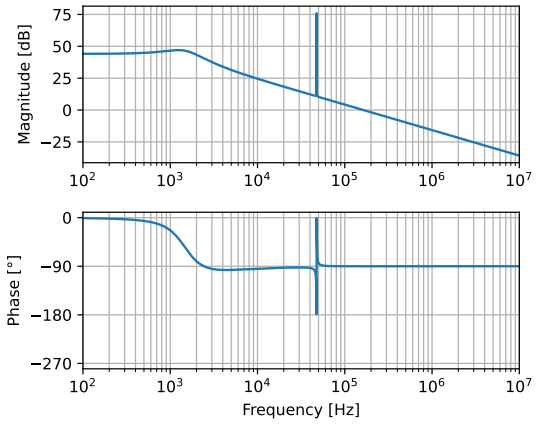
Using the input-to-output state transfer function, presented in equation (4.5), the current mode inner control loop plant of the uncoupled SEPIC is derived as equation (C.5).

$$G_{\mathrm{id}}(s) = \frac{\tilde{i}_{\mathrm{L1}} + \tilde{i}_{\mathrm{L2}}}{\tilde{d}} = \frac{1.03 \times 10^6 s^3 + 9.99 \times 10^9 s^2 + 9.15 \times 10^{16} s + 1.24 \times 10^{21}}{s^4 + 8500 s^3 + 8.938 \times 10^{10} s^2 + 7.59 \times 10^{14} s + 7.76 \times 10^{18}} \tag{C.5}$$

The pole-zero map and the frequency response of equation (C.5) are presented in figure C.5.



(a) Pole-zero map.



(b) Frequency response.

Figure C.5 Frequency domain plots of the current-mode control inner-loop power stage, from equation (C.5).

The poles and zeros of equation (C.5) are presented in table C.5.

Table C.5 Poles and zeros of equation (C.5)

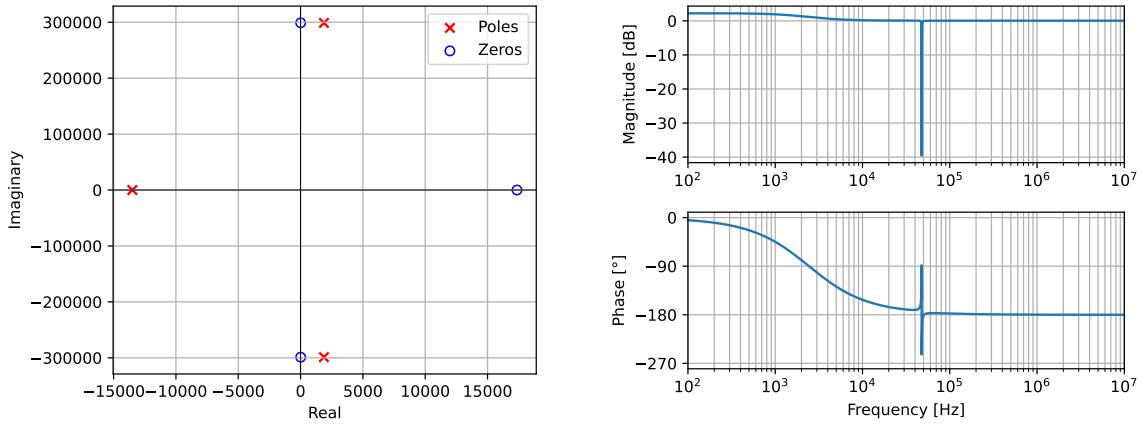
Parameter	Location	Frequency	Angle	Damping
Zero 1	$1.87 \times 10^3 \pm j298.83 \times 10^3$	47.56 kHz	$\pm 89.64°$	6.27×10^{-3}
Zero 2	-13.50×10^3	2.15 kHz	$180°$	1
Pole 1	$-0.629 \times 10^{-3} \pm j298.83 \times 10^3$	47.56 kHz	$\pm 90.00°$	2.10×10^{-9}
Pole 2	$-4.25 \times 10^3 \pm j8296.14$	1.48 kHz	$\pm 117.12°$	0.46

Current Control Power Stage - Outer loop

The outer loop portion of the power stage is derived based on equation (C.4) and equation (C.5) as presented in equation (4.10). Thus it is derived as presented in equation (C.6).

$$G_{\text{vi}}(s) = \frac{G_{\text{vd}}(s)}{G_{\text{id}}(s)} = \frac{\tilde{v}_{\text{C2}}}{\tilde{i}_{\text{L1}} + \tilde{i}_{\text{L2}}} = \frac{-1.007s^3 + 1.75 \times 10^4 s^2 - 9.0 \times 10^{10} s + 1.56 \times 10^{15}}{s^3 - 9748s^2 + 8.925 \times 10^{10} s + 1.21 \times 10^{15}} \tag{C.6}$$

The pole-zero map and the frequency response of equation (C.6) are presented in figure C.6.



(a) Pole-zero map.

(b) Frequency response.

Figure C.6 Frequency domain plots of the current-mode control outer-loop power stage, from equation (C.6).

The poles and zeros of equation (C.6) are presented in table C.6.

Table C.6 Poles and zeros of equation (C.6)

Parameter	Location	Frequency	Angle	Damping
Zero 1	$7.67 \pm j298.94 \times 10^3$	47.58 kHz	$\pm 90.00°$	2.57×10^{-5}
Zero 2	17.37×10^3	2.76 kHz	$0°$	1
Pole 1	$1.87 \times 10^3 \pm j298.83 \times 10^3$	47.56 kHz	$\pm 89.64°$	0.27×10^{-3}
Pole 2	-13.50×10^3	2.15 kHz	$180°$	1

C.2 Current Sense Transformer Design

As outline, to obtain the desirable current sensor gain of $K_{\text{CS}} = 35.7\,\frac{\text{mV}}{\text{A}} = 35.7\,\text{m}\Omega$ a pure resistor would yield excessive losses. When $V_{\text{in}} = 35\,\text{V}$ and $P = 500\,\text{W}$, the transistor current is $I_{\text{DD}} = 18.7\,\text{A}$. In that

case the power loss on the resistor is:

$$P_{\text{sense}} = (18.7\,\text{A})^2 \cdot 35.7\,\text{m}\Omega = 12.4\,\text{W}$$

This is of course not sustainable. Moreover a shunt amplifier is not applicable, because the sensor should be able to sense very fast dynamics, in the range of several MHz. To overcome these issue, it is chosen to utilise a current sense transformer in series with the transistor. The current sense transformer topology is presented in figure C.7.

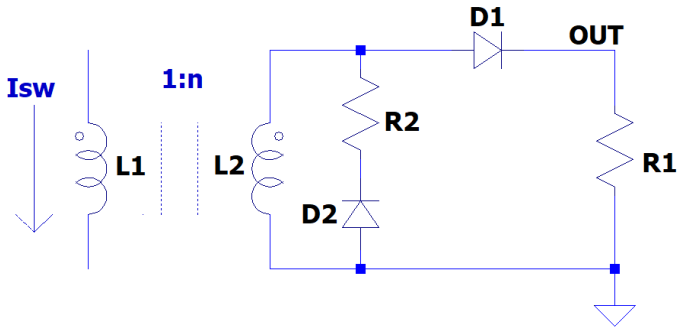


Figure C.7 Current sense transformer schematic [30].

As mentioned in section 4.2, it is desired for the output voltage to yield 1 V when the current is 28 A. Therefore the current transformer is designed for 1 V. It is desired for the maximum power to be 250 mW, therefore the bleeding resistor can be:

$$R_{\text{b}} = \frac{(1\,\text{V})^2}{250\,\text{mW}} = 4\,\Omega$$

This yields a secondary current of:

$$I_{\text{b}} = \frac{1\,\text{V}}{4\,\Omega} = 250\,\text{mA}$$

Based on the primary and secondary currents, the required number of turns can be computed:

$$N_{\text{CT}} = \frac{28\,\text{A}}{250\,\text{mA}} = 112$$

Based on commercial availability a turns-ratio of 125 is considered. Thus through compensation it is found that:

$$I_{\text{b}} = \frac{28\,\text{A}}{125} = 224\,\text{mA}$$

$$R_{\text{b}} = \frac{1\,\text{V}}{224\,\text{mA}} = 4.46\,\Omega$$

To implement a transformer like this in LTspice, it is necessary to specify the inductances. Thus the relation between the primary and secondary inductance is derived:

$$\frac{n_1}{n_2} = \sqrt{\frac{L_1}{L_2}} \qquad = \qquad L_2 = \frac{L_1 {n_2}^2}{{n_1}^2}$$

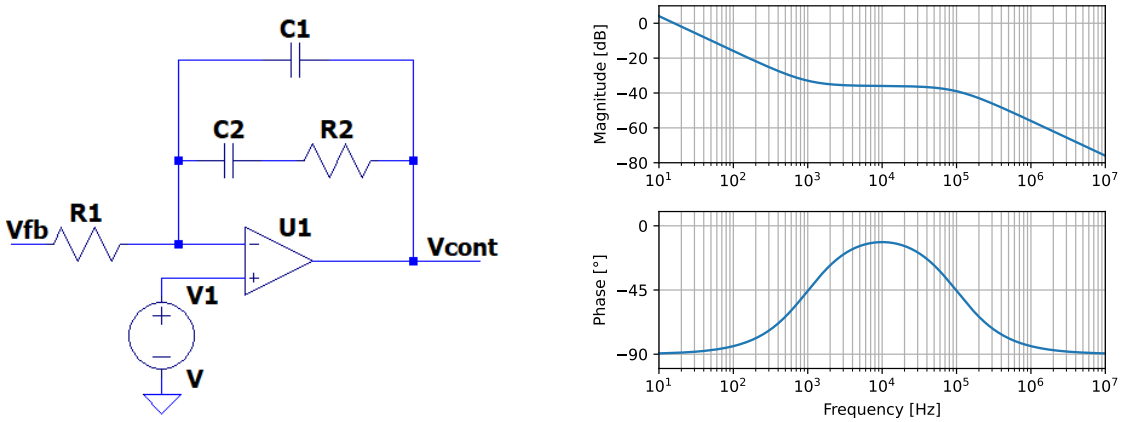
In summary, to yield a current sensor gain of $K_{\text{CS}} = 35.7\,\frac{\text{mV}}{\text{A}}$, the current sense transformer must consist of 125 turns and a burden resistor of 4.46 Ω. For simulations it was found that a reset resistance of 100 Ω was adequate [14] [30].

C.3 Type-II Compensator Design and Realisation

To shape the open-loop transfer function of equation (4.11) and yield adequate open-loop stability margins and closed-loop bandwidth, a type-II compensator is used. The type-II compensator transfer function is presented in equation (4.14), and reviewed below:

$$G_{\mathrm{c}}(s) = K\frac{(s+2\pi f_{\mathrm{z}})}{s(s+2\pi f_{\mathrm{p}})}$$

That is, the type-II compensator consists of a gain, a real zero a pole at origin, and a real pole. To implement this in hardware, and for that matter also SPICE simulations, an operational amplifier with feedback is used. The type-II compensator schematic and the associated frequency response is presented in figure C.8.



(a) Schematic.

(b) Frequency response.

Figure C.8 Type-II compensator.

From the analogue compensator of figure C.8a, the feedback path are two impedances in parallel, thereby the analogue transfer function is derived as presented in equation (C.7).

$$G_{\mathrm{EA}}(s) = -\frac{Z_{\mathrm{f}}(s)}{Z_{\mathrm{i}}(s)} = -\frac{1}{R_1C_1}\frac{s+\frac{1}{R_2C_2}}{s(s+\frac{C_1+C_2}{C_1C_2R_1})} \tag{C.7}$$

Thus by comparing equation (C.7) and equation (4.14) it is derived that:

$$C_1 = \frac{1}{KR_1}$$

$$C_2 = \frac{(\omega_{\mathrm{p}}-\omega_{\mathrm{z}})}{\omega_{\mathrm{z}}}C_1$$

$$R_2 = \frac{C_1+C_2}{C_1C_2\omega_{\mathrm{p}}}$$

Thus the gain, zero-, and pole frequency can all be realised by computing R_1, R_2, C_1, and C_2. For the compensator design in this project it is desired that the bandwidth is a few kilohertz. Therefore ω_{z} and ω_{p} are selected as 1 kHz and 10 kHz, respectively, to provide the phase boost in the target frequency range. Furthermore ω_{p} is set to 10 kHz to attenuate the high frequency content. Then lastly the gain is turned accordingly to achieve the proper bandwidth and stability margins.

C.4 Small-Signal Forced Response

The forced response of the small-signal models are constructed around the equilibrium points, that is:

$$x(t) = X + \tilde{x}(t)$$

where the equilibrium points are those derived in equation (2.24). In the following the forced response to a 10% step in duty cycle is presented for the uncoupled- and coupled versions of the SEPIC. The response is computed using the `ct.forced_response()` function of the control package in Python.

Uncoupled

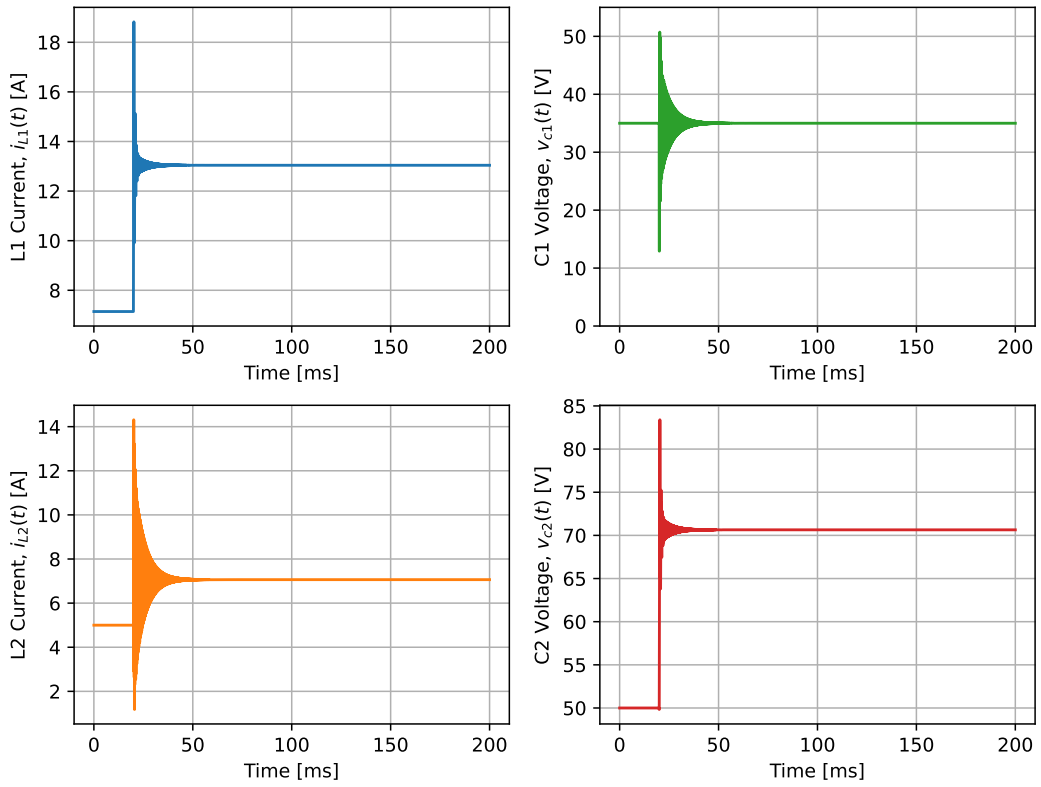


Figure C.9 Forced response of small-signal state-space model of the uncoupled SEPIC topology, to a 10% perturbation in the duty-cycle at 20 ms.

Coupled

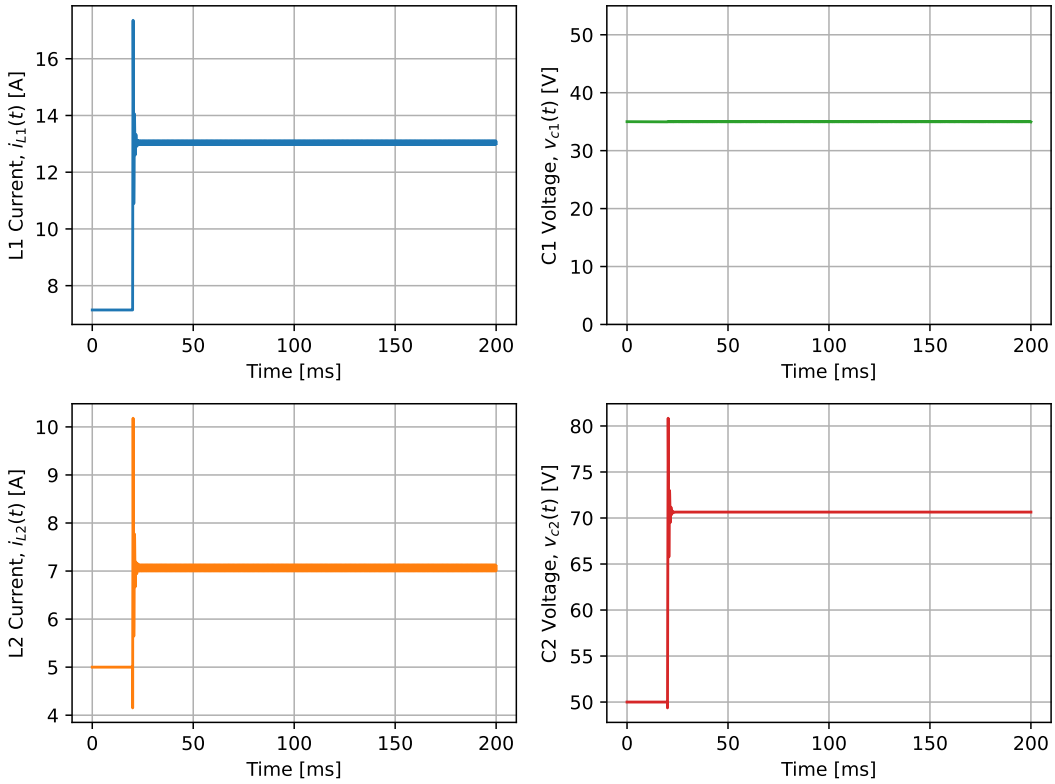


Figure C.10 Forced response of small-signal state-space model of the coupled SEPIC topology, to a 10% perturbation in the duty-cycle at 20 ms.

C.5 Small-Signal Response of the SEPIC Prototype

The small-signal response is attempted to be validated in the lab. This is done by making a step in the control variable, the duty-cycle D. In the lab the input voltage during this test was 20 V, and the step is from 40% to 50%. To compare a small-signal model of the SEPIC with these operational parameters is also computed, using the script of listing F.6. Both responses are of the coupled version of the SEPIC. The laboratory and modelled responses are presented in figure C.11.

Comparing the small-signal model and the laboratory response, it is seen that the laboratory response has much better damping. This is suggesting that the resonances in laboratory are well-damped, perhaps indicating that there s more resistance in the system. Additionally the oscillation frequency of the laboratory response is 1.8 kHz while the model has 2.25 kHz.

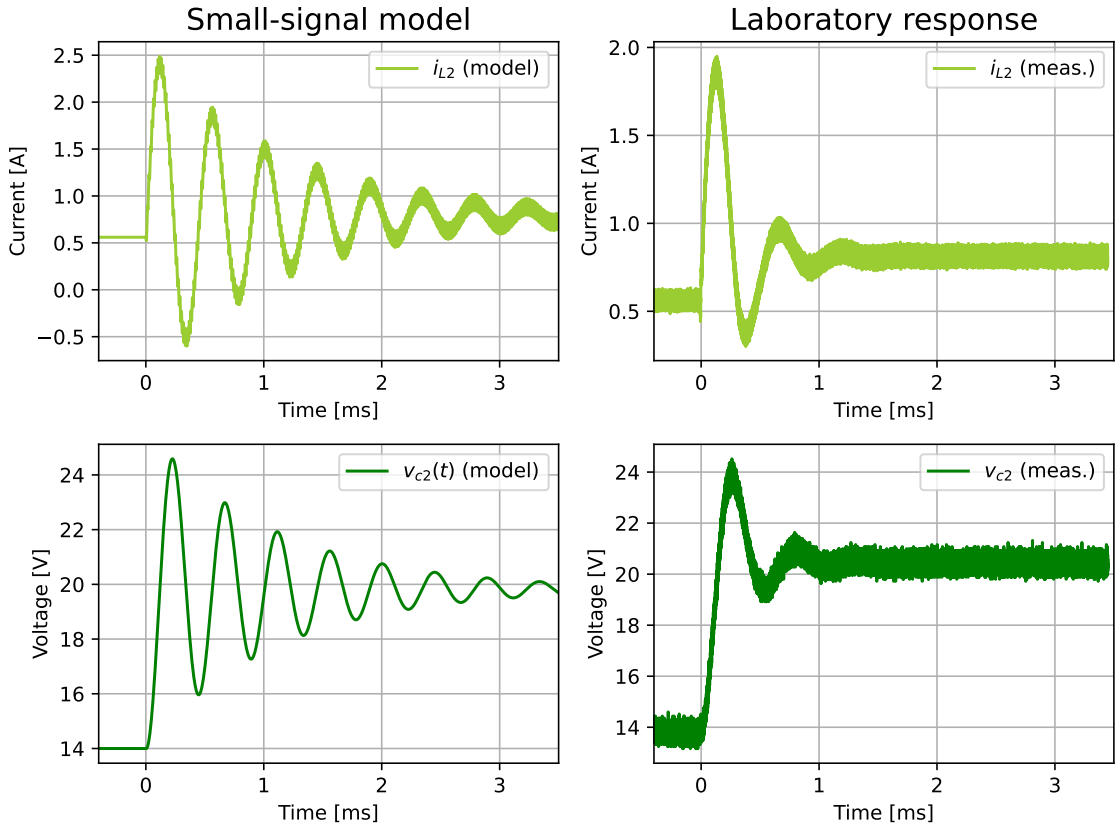


Figure C.11 State response to a 10% step in the duty-cycle, of the laboratory prototype and the small-signal model.

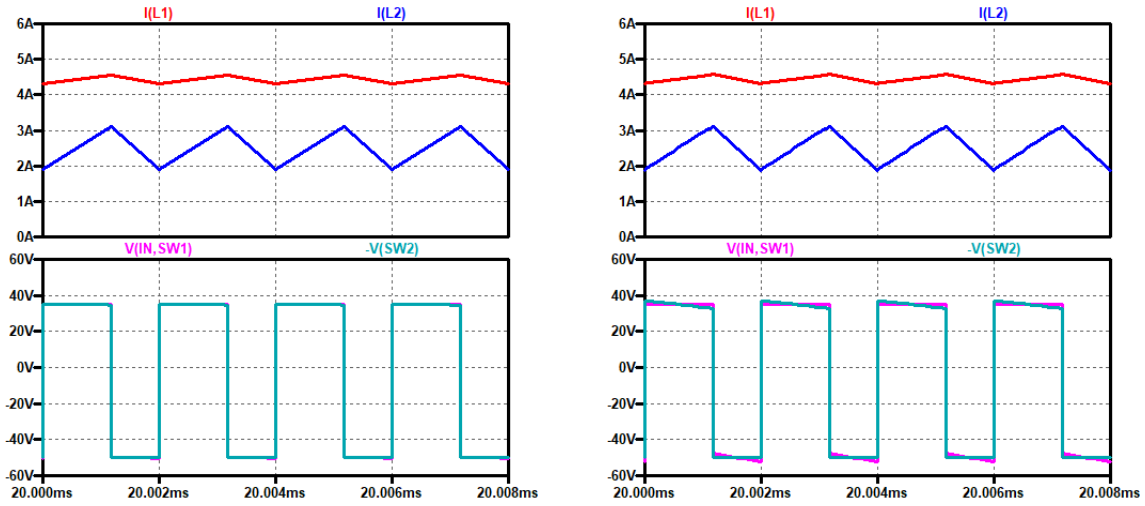
D Additional Simulations

D.1 Evaluation of the C1 Capacitor

In this part it is analysed what influence the voltage ripple on C_1 has on the SEPIC dynamics. For this the open-loop simulation of the SEPIC is used. Both coupled inductors and uncoupled inductors are analysed. The simulations revolve around 1 order of magnitude difference in C_1

D.1.1 Evaluation with Uncoupled Inductors

When the topology has uncoupled inductors, the waveforms on the inductors become as presented in figure D.1.



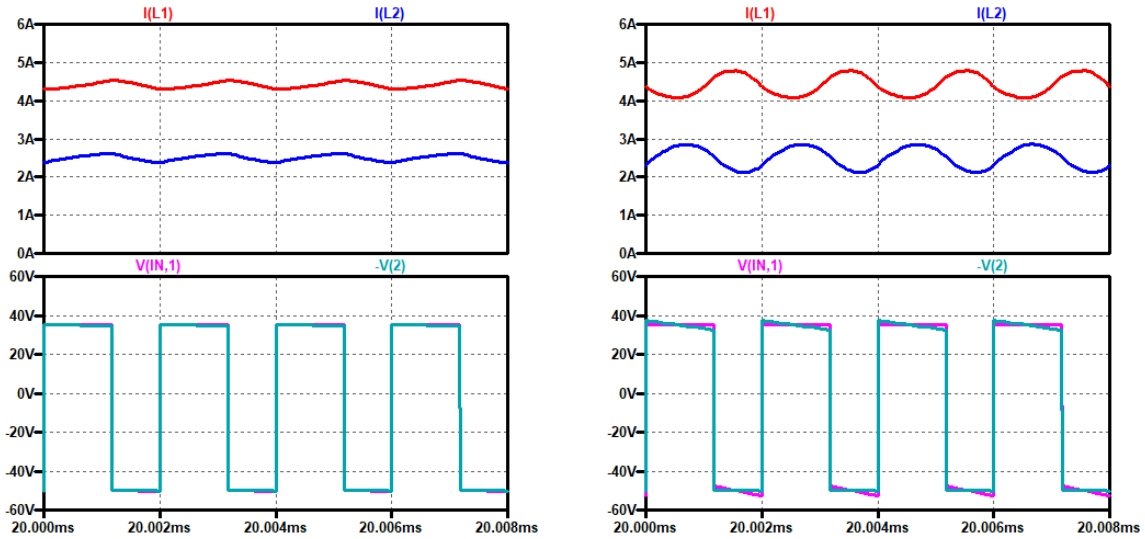
(a) $C_1 = 6.72\,\mu\text{F}$. **(b)** $C_1 = 0.672\,\mu\text{F}$.

Figure D.1 Inductor waveforms subject to different values of C_1.

It is seen that when the capacitance is lowest, the voltage across each inductor no longer overlap that well. This influence does however not seem to make much impact for the uncoupled topology. The impact on the coupled topology is analysed in appendix D.1.2.

D.1.2 Evaluation with Coupled Inductors

When the topology has coupled inductors, the waveforms on the inductors become as presented in figure D.2.



(a) $C_1 = 6.72\,\mu\text{F}$. **(b)** $C_1 = 0.672\,\mu\text{F}$.

Figure D.2 Inductor waveforms subject to different values of C_1.

For the coupled SEPIC topology it is seen that the effect of a lower C_1, results in the inductor current waveforms differing quite abit. This is explained from Faraday's law of induction, which results in equation (2.49), which states that the voltage on the primary and seconary must be exactly equal for an ideal core. However, for a non-ideal core there exists leakage flux. The inductance of the leakage acts as a balance, in which the induced voltage across it must balance the residual voltage. For the leakage inductance to induce a voltage it must draw a current, which explains the reason why the current shape changes. Thus it is clear that for the coupled version of the SEPIC it is essential to have high enough C_1, such that additional currents due to the leakage inductances are minimised.

D.2 Transient Output Voltage Response with High Main Bus Capacitance

In this part the transient response of the SEPIC in closed-loop control is analysed, when the main bus capacitance is 5 mF. As the output capacitance changes the SEPIC power stage transfer function also changes, as given by equation (4.4), Therefore the type-II compensator is also adjusted accordingly. The adjusted compensator is a presented below:

$$G_c(s) = 3.2 \times 10^7 \frac{s + 628.3}{s(s + 188.5 \times 10^3)}$$

yielding GM = 8.52 dB and PM = 61.3°, thus fulfilling the stability criteria of the ECSS standard [6]. With the adjusted compensator, and the 5 mF capacitance, the closed-loop simulation becomes as presented in figure D.3.

Notice that a large capacitance of 5 mF requires alot of charge (250 mC at 50 V), thus the inrush current is possible to reach very high values. However, the peak-current mode control scheme provides inherent current limitation, and thus the controller will keep the inrush current at a reasonable value. This is

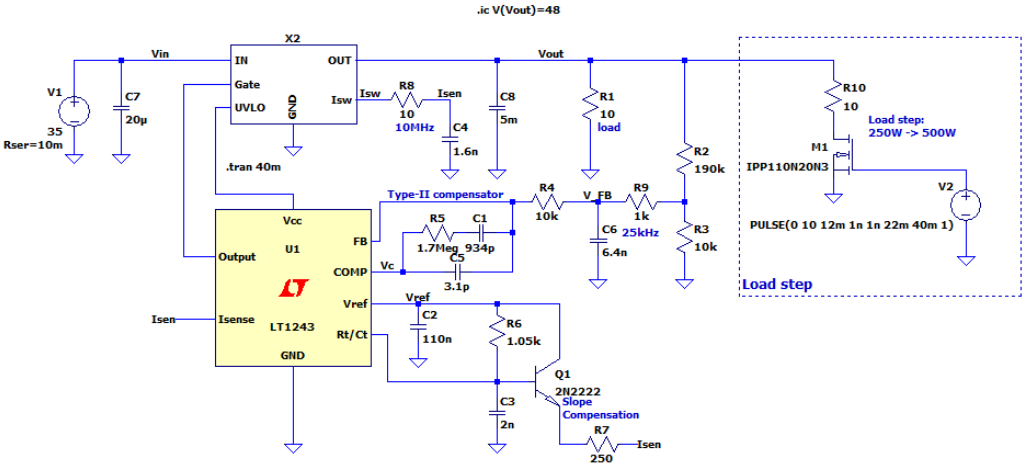


Figure D.3 Closed-loop SEPIC simulation with 5 mF of main bus capacitance and adjusted compensator.

also shown with this simulation. The load step occurs at 12 ms of the simulation time, and the output voltage- and output current response is presented in figure D.4.

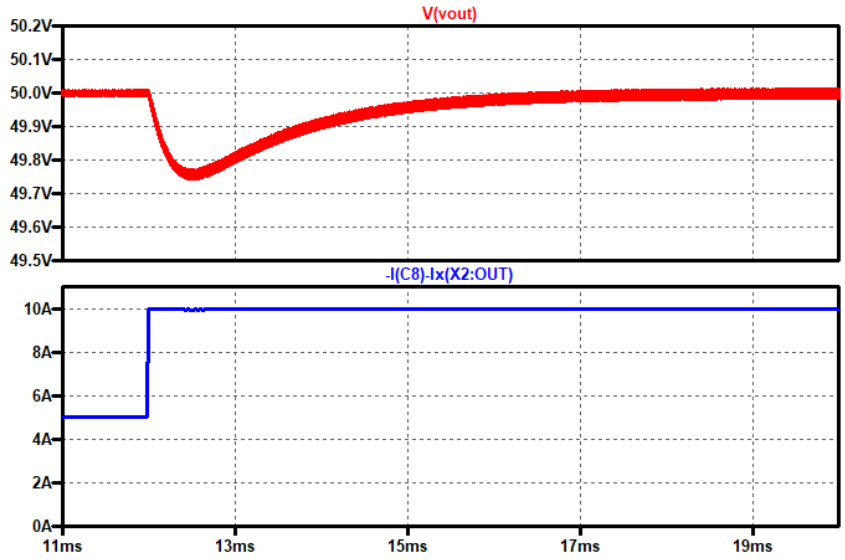


Figure D.4 Output voltage- and output current response of the closed-loop SEPIC simulation for a 50% load step increase.

From the transient main bus voltage of figure D.4 the minimum voltage reaches 49.75 V. This means the voltage transient in this case is just 0.5%, thus fulfilling the ECSS standard, which required a maximum of 1%. The 5 mF capacitance is chosen arbitrarily and may not be a representative value. However, this analysis does prove that the SEPIC can fulfill the transient control-loop requirements of the ECSS standard.

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E Further Laboratory Work

E.1 Additional Waveforms

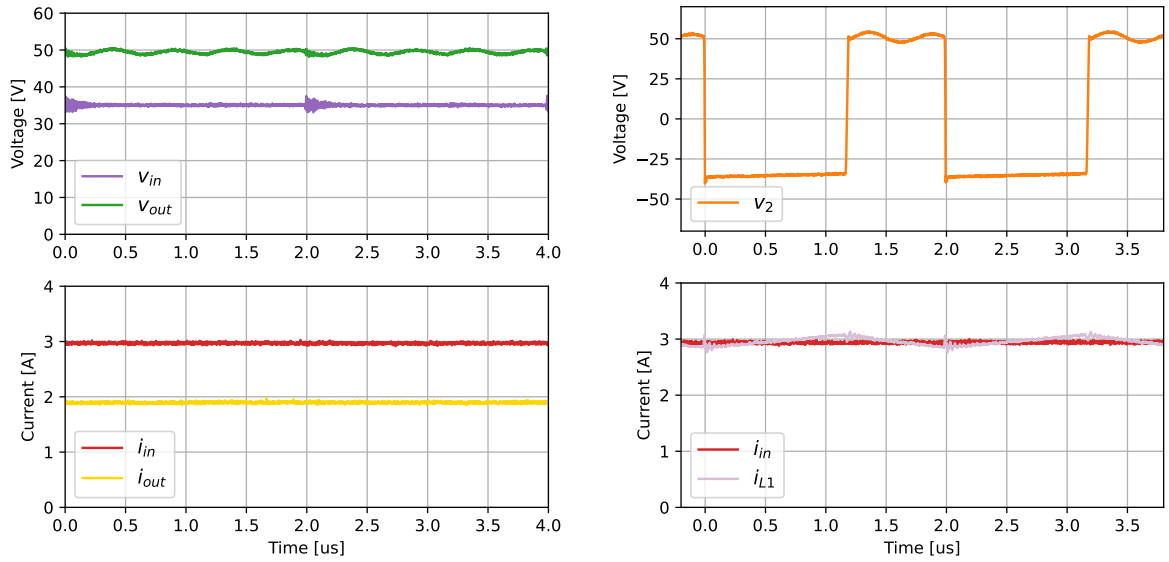
In this part additonal waveforms from the SEPIC prototype are presented.

E.1.1 Extra waveforms of the Uncoupled SEPIC Prototype

In this part of the appendis additional waveforms of the uncoupled SEPIC prototype are covered.

Diode and L1 waveforms with an input voltage of 35V

The waveforms regarding the diode and input of the uncoupled SEPIC with an input voltage of 35 V is presented in figure E.1. Here the voltage at node 2 is presented, which is essentially the voltage across L_2. This is also the voltage at the diode anode.



(a) Input and output waveforms.

(b) Dynamic waveforms.

Figure E.1 Steady-state waveforms of the uncoupled SEPIC prototype with $V_{\text{in}} = 50\,\text{V}$ at $P = 100\,\text{W}$.

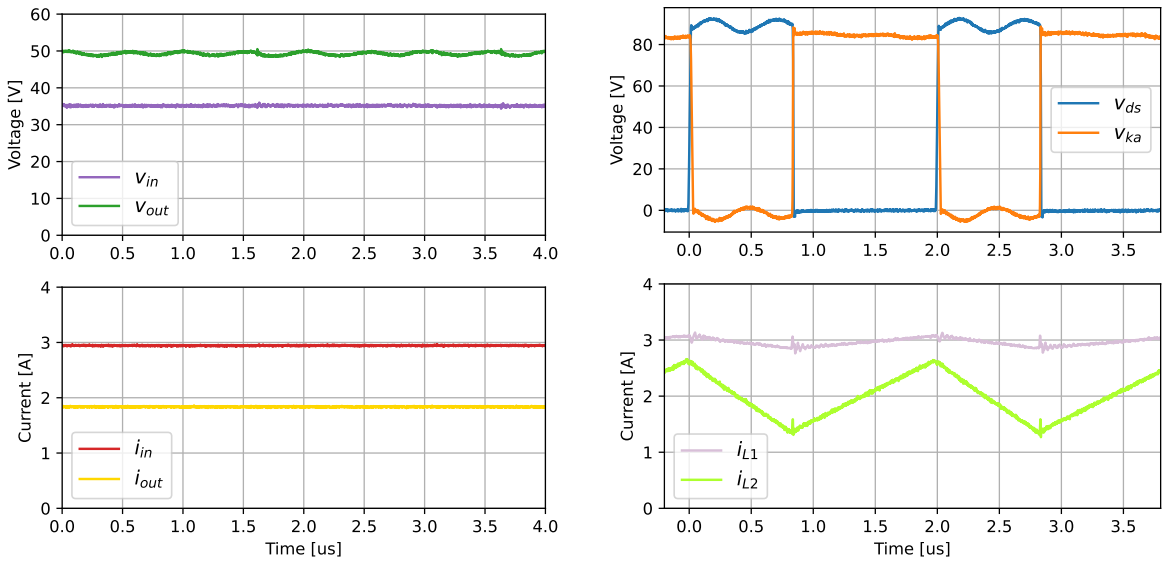
Comprehensive waveform with an input voltage of 35V

By combining the transistor voltage, the node 2 voltage, and the output voltage, the waveforms of figures E.1 and E.4 can be used to construct a complete waveform. The comprehensive waveforms of the SEPIC is presented in figure E.2.

The cathode and anode voltage of the diode are constructed with the relation of equation (2.43). That is:

$$v_{\text{ka}} = -v_{\text{L2}} - v_{\text{out}}$$

Here it is important to note that v_{L2} are measured during two separate tests v_{out}, so they cannot be expected to be synchronised very well. This also means that the v_{ka} waveforms in figure E.2b, should not be taken literally. It should be seen as a reference for when the diode is either ON or OFF. The same waveforms are plotted at 50V below.

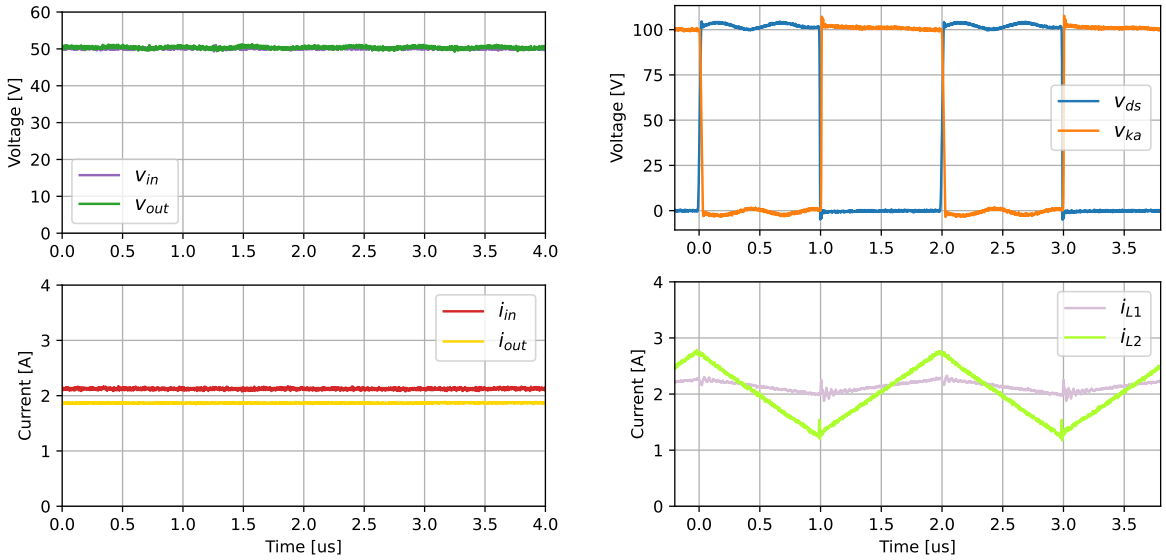


(a) Input and output waveforms. **(b)** Dynamic waveforms.

Figure E.2 Comprehensive waveforms of the uncoupled SEPIC prototype with $V_{\text{in}} = 35\,\text{V}$ at $P = 100\,\text{W}$.

Comprehensive waveform with an input voltage of 50V

The constructed comprehensive waveforms of the SEPIC at 50 V is presented in figure E.3.



(a) Input and output waveforms. **(b)** Dynamic waveforms.

Figure E.3 Steady-state waveforms of the uncoupled SEPIC prototype with $V_{\text{in}} = 50\,\text{V}$ at $P = 100\,\text{W}$.

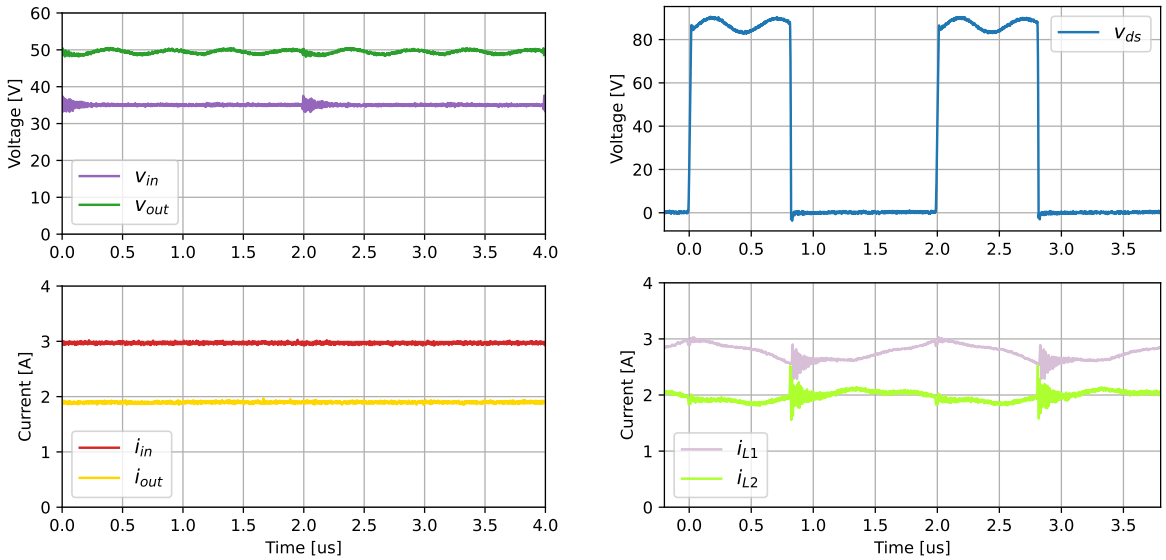
From the waveforms of figure E.3 it is seen that the current and voltages overlap. This is because the duty cycle is about 0.5 when $v_{\text{in}} = v_{\text{out}}$.

E.1.2 Static waveforms of the Coupled SEPIC Prototype

In this part of the appendis additional waveforms of the coupled SEPIC prototype are covered.

Waveforms with an input voltage of 35V

The waveforms of the coupled SEPIC with an input voltage of 35 V is presented in figure E.4.

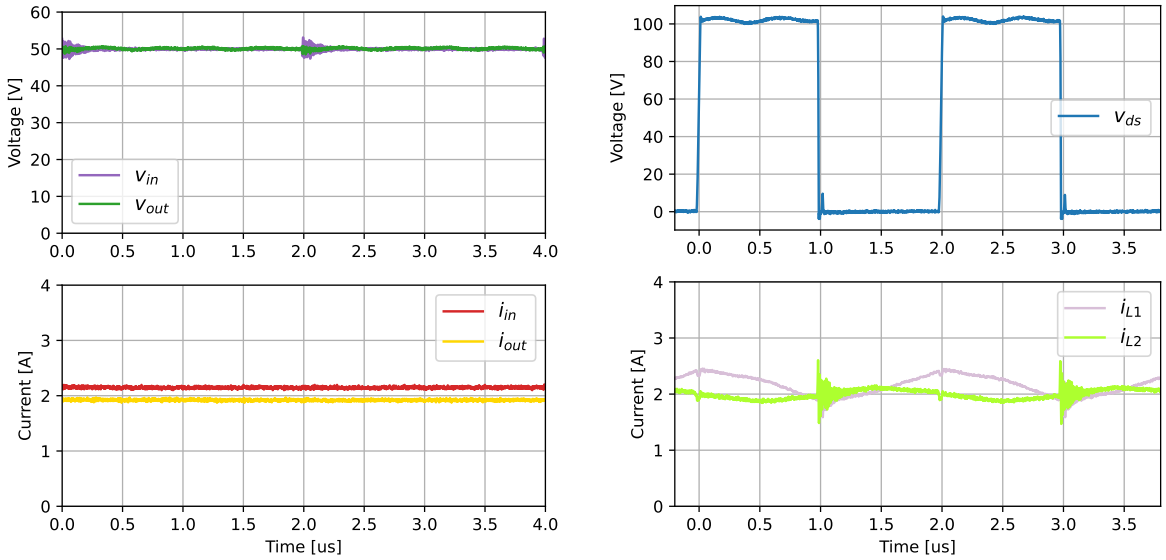


(a) Input and output waveforms. **(b)** Dynamic waveforms.

Figure E.4 Steady-state waveforms of the coupled SEPIC prototype with $V_{\text{in}} = 35\,\text{V}$ at $P = 100\,\text{W}$.

Waveforms with an input voltage of 50V

The waveforms of the coupled SEPIC with an input voltage of 50 V is presented in figure E.5.



(a) Input and output waveforms. **(b)** Dynamic waveforms.

Figure E.5 Steady-state waveforms of the coupled SEPIC prototype with $V_{\text{in}} = 50\,\text{V}$ at $P = 100\,\text{W}$.

From the inductor current in figures E.4b and E.5b it is seen that the current is not zig-zag. This is expected due to the low value of $C_1 = 2.64\,\mu\text{F}$, as described in appendix D.1.2. In comparison to the inductor ripples of figures E.2b and E.3 the ripple amplitudes are also visibly smaller. However, significant noise occurs around the switching event, especially turn on. The 2 MHz oscillation is still present for

the coupled version in both drain-to-source voltage and output voltage. It also appears in the inductor currents.

E.1.3 Drain-to-source Ringing Waveform

A more detailed look of the drain-to-source ringing during a turn off event is presented in figure E.6.

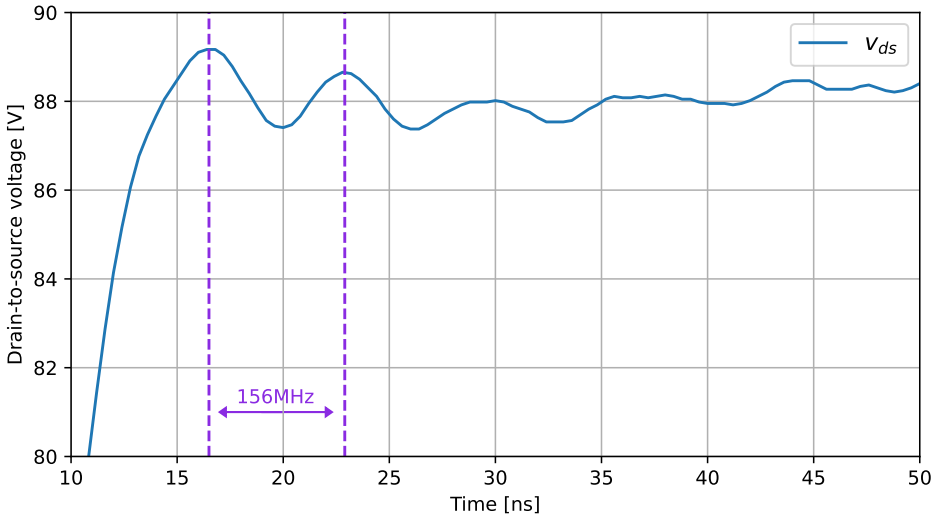


Figure E.6 Zoom in of the transistor drain-to-source voltage during a turn-off event.

It is found that the ringing frequency is $f_0 = 156.25\,\text{MHz}$ and is fairly well damped indicating rather low power loop inductance, but on the other hand perhaps higher resistance. The ringing frequency can be used to estimate the power loop inductance, L_{loop}, as presented in equation (E.1).

$$f_0 = \frac{1}{2\pi\sqrt{L_{\text{loop}} \cdot C_{\text{oss}}}} \tag{E.1}$$

It is assumed that the transistor output capacitance, C_{oss}, is significantly lower than the capacitors of the power loop, refer to figure 6.4, thereby the series capacitance will approach the output capacitance. Using $C_{\text{oss}} = 800\,\text{pF}$ from the datasheet (at 85 V) and $f_0 = 156.25\,\text{MHz}$, it is found that the equivalent power loop inductance must be $L_{\text{loop}} = 1.30\,\text{nH}$. This is a fairly low power loop inductance, suggesting that the power loop design has been effective at minimising parasitic inductance [29].

Furthermore, the rise time is $t_{\text{r}} = 15.6\,\text{ns}$ switching with $5.62\,\frac{\text{V}}{\text{ns}}$. Additionally the mean current in the transistor is $i_{\text{dd}} = i_{\text{in}} + i_{\text{out}}$. Thus with the mean input- and output current of $i_{\text{in}} = 2.94\,\text{A}$ and $i_{\text{out}} = 1.84\,\text{A}$, the output capacitance can be estimated by equation (E.3).

$$i_{\text{dd}} = C_{\text{oss}} \frac{\text{d}v_{\text{ds}}}{\text{d}t} \tag{E.2}$$

$$C_{\text{oss}} \approx \frac{i_{\text{dd}}}{\Delta V_{\text{ds}}/t_{\text{r}}} \tag{E.3}$$

Inserting the parameters, the estimated output capacitance is: $C_{\text{oss}} = 845.6\,\text{pF}$, which is rather close to the specified 800 pF of the EPC2304 datasheet (at 85 V). This further supports the power loop inductance computation.

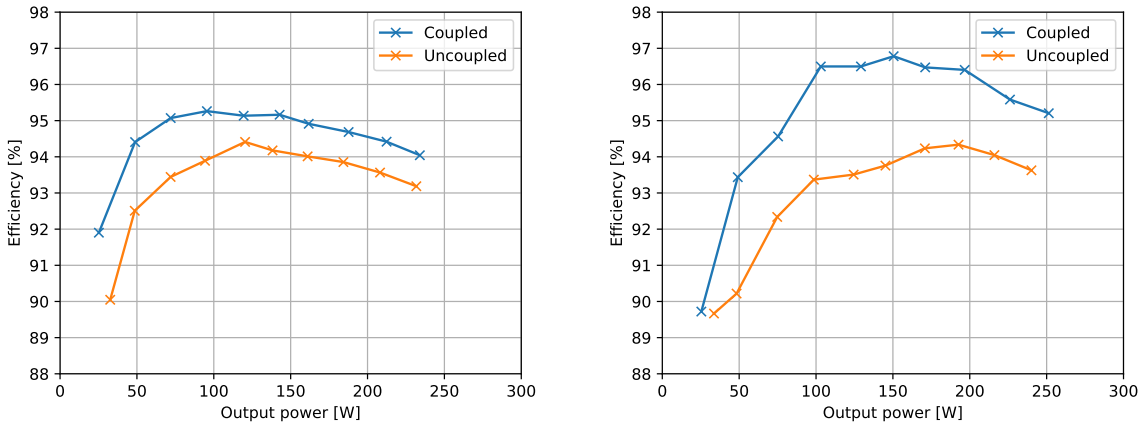
E.2 Additional Efficiency Results

E.2.1 Efficiency Curves with a Switching Frequency of 250 kHz

In this part of the appendix the efficiency curves of the SEPIC protorype operated at a switching frequency of 250 kHz are evaluated.

Impact of Magnetic Coupling on the Efficiency Curve

The efficiency curves of the SEPIC prototype with a switching frequency of 250 kHz is presented in figure E.7.



(a) $V_{\text{in}} = 35\,\text{V}$ scenario.

(b) $V_{\text{in}} = 50\,\text{V}$ scenario.

Figure E.7 Efficiency profiles of uncoupled- and coupled versions of the SEPIC with a switching frequency of 250 kHz.

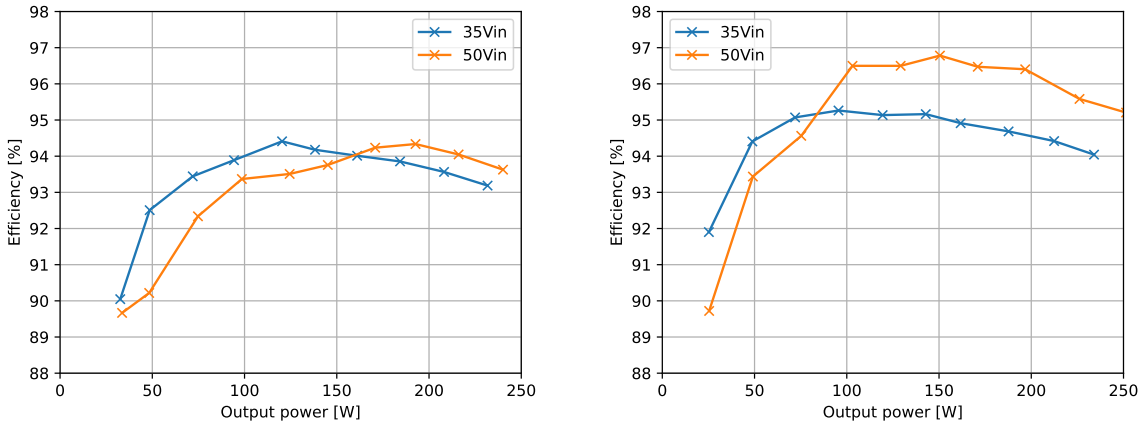
The results of the experimental efficiency curve is summarised in table E.1.

Table E.1 Peak efficiency points on the power curve of the experimental SEPIC prototype with uncoupled- and coupled inductors.

Parameter	**Uncoupled**		**Coupled**	
Input voltage, V_{in}	35 V	50 V	35 V	50 V
Peak efficiency, $\hat{\eta}$	94.4%	94.3%	95.3%	96.8%
Power level, P_{out}	120.3 W	192.7 W	95.5 W	150.5 W

Impact of Input Voltage Magnitude of the Efficiency Curve

The efficiency curves for the SEPIC prototype due to different input voltage level is presented in figure E.8.



(a) Uncoupled inductors scenario.

(b) Coupled inductors scenario.

Figure E.8 Efficiency profiles of the uncoupled- and coupled versions of the SEPIC prototype at different input voltages for a switching frequency of 250 kHz.

F Programming, Algorithms, and Scripts

F.1 SEPIC Python Loss Algorithm

In this appendix the `P_loss_SEPIC()` Python function is presented and described. The full Python function code is presented in listing F.1, and subsequently the rational behind the algorithm is described.

Listing F.1 Python function for coupled SEPIC power losses.

```
def P_loss_SEPIC(P,Vin,Vout,f_sw,coupled_core):
    # init
    D = Vout/(Vin + Vout)
    I_in = P/Vin
    I_out = P/Vout
    I_L1 = I_in
    I_L2 = I_out
    if(coupled_core):
        L2 = L1
        dI_L1 = (Vin*D)/(L1*f_sw)
        dI_L2 = (Vin*D)/(L2*f_sw)
        ESR_L1 = 15.52e-3
        ESR_L2 = 33.2e-3
        N_windings = np.sqrt((L1/2)/AL_L1)
        N_windings = np.ceil(N_windings)
    else:
        L2 = 33.33e-6
        dI_L1 = (Vin*D)/(L1*f_sw)
        dI_L2 = (Vin*D)/(L2*f_sw)
        N_windings_L1 = np.sqrt((L1)/AL_L1)
        N_windings_L1 = np.ceil(N_windings_L1)
        N_windings_L2 = np.sqrt((L2)/AL_L2)
        N_windings_L2 = np.ceil(N_windings_L2)
        ESR_L1 = 15.52e-3 * N_windings_L1/32 # 15.52 mOhm measured in lab for 32 turns
        ESR_L2 = 33.2e-3 * N_windings_L2/32 # 33.2e-3 mOhm measured in lab for 32 turns

    # Conduction loss, Q1
    I_Q1 = (I_L1 + I_L2) * np.sqrt(D) * np.sqrt(1 + (1/3) * ((dI_L1 + dI_L2)/(2*(I_L1 + I_L2))))
    P_cond_Q1 = I_Q1**2 * Rds_on

    # Switching loss, Q1
    T_Qon = Qg_tot/I_gate_on
    T_Qoff = Qg_tot/I_gate_off
    P_Coss_Q1 = 0.5*Coss(Vin+Vout)*((Vin+Vout)**2)*f_sw
    P_turn_on_Q1 = (1/2)*(I_L1 + I_L2)*(Vin+Vout)*(T_Qon)*f_sw
    P_turn_off_Q1 = (1/2)*(I_L1 + I_L2)*(Vin+Vout)*(T_Qoff)*f_sw
    P_SW_Q1 = P_turn_on_Q1 + P_turn_off_Q1 + P_Coss_Q1

    # Driving loss, Q1
    P_drv_Q1 = 2*Qg_tot*V_gate*f_sw

```

```
    # Diode conduction loss
    I_D1 = (I_L1 + I_L2) * np.sqrt(1-D) * np.sqrt(1 + (1/3) * ((dI_L1 + dI_L2)/(2*(I_L1 +
        I_L2)))**2)
    P_cond_D = I_D1 * Vfwd(I_D1)

    # Diode junction capacitance losses
    P_Cj_D = ((Vin+Vout)*Cj(Vin+Vout)*(Vin+Vout))/2 * f_sw

    # Capacitor conduction losses
    I_C1 = np.sqrt(D*(I_out**2) + (1-D)*(I_in**2))
    I_C2 = I_C1
    P_cond_C1 = I_C1**2 * C1_ESR
    P_cond_C2 = I_C2**2 * C2_ESR

    # Inductor conduction losses
    P_cond_L1 = I_L1**2 * ESR_L1
    P_cond_L2 = I_L2**2 * ESR_L2

    # Inductor core losses
    if(coupled_core):
        H_L_max = 0.0125663706 * N_windings*(I_L1+dI_L1/2 + I_L2+dI_L2/2)/l_eff_L1 # Converted
            to Oersted
        H_L_min = 0.0125663706 * N_windings*(I_L1-dI_L1/2 + I_L2-dI_L2/2)/l_eff_L1 # Converted
            to Oersted
        B_L_max = B_curve_ultra(H_L_max)
        B_L_min = B_curve_ultra(H_L_min)
        B_ac_L = (B_L_max-B_L_min)/2
        P_core_L = a_core_L1 * B_ac_L**b_core_L1 * (f_sw*1e-3)**c_core_L1 * vol_core_L1 * 1e-3 #
            multiplies to get mW to W
        P_core_L1 = P_core_L/2
        P_core_L2 = P_core_L/2
    else:
        H_L1_max = 0.0125663706 * N_windings_L1*(I_L1+dI_L1/2)/l_eff_L1 # Converted to Oersted
        H_L1_min= 0.0125663706 * N_windings_L1*(I_L1-dI_L1/2)/l_eff_L1 # Converted to Oersted
        B_L1_max = B_curve_ultra(H_L1_max)
        B_L1_min = B_curve_ultra(H_L1_min)
        B_ac_L1 = (B_L1_max-B_L1_min)/2
        P_core_L1 = a_core_L1 * B_ac_L1**b_core_L1 * (f_sw*1e-3)**c_core_L1 * vol_core_L1 * 1e-3
            # multiplies to get mW to W

        H_L2_max = 0.0125663706 * N_windings_L2*(I_L2+dI_L2/2)/l_eff_L2 # Converted to Oersted
        H_L2_min= 0.0125663706 * N_windings_L2*(I_L2-dI_L2/2)/l_eff_L2 # Converted to Oersted
        B_L2_max = B_curve_edge(H_L2_max)
        B_L2_min = B_curve_edge(H_L2_min)
        B_ac_L2 = (B_L2_max-B_L2_min)/2
        P_core_L2 = a_core_L2 * B_ac_L2**b_core_L2 * (f_sw*1e-3)**c_core_L2 * vol_core_L2 * 1e-3
            # multiplies to get mW to W

    return( P_cond_Q1 + P_cond_D + P_cond_C1+P_cond_C2 + P_cond_L1+P_cond_L2,
           P_SW_Q1 + P_Cj_D,
           P_core_L1+P_core_L2 )
```

The `P_loss_SEPIC()` function has 5 entries: P, Vin, Vout, f_sw, and coupled_core. coupled_core is a

boolean value, determining whether the loss computations is for a coupled SEPIC, or an uncoupled SEPIC.

The initialisiation beginning on line 3 determines the steady-state currents in the system. Then based on the entry of coupled_core, the series resistance and inductance is defined. Note that the resistance of the inductors of like 12 to 13 are determined experimentally as described in appendix A.3.4. This resistance is scaled for the number of turns in the uncoupled versions of likes 24 and 25.

In lines 27 to 40 the transistor conduction and switching losses are computed. Note that the output capacitance is dependent on the drain-to-source voltage. Therefore the function `Coss()` is implemented to capture this non-constant value. This function is described in appendix F.1.1.

In lines 42 to 47 the conduction losses and switching losses of the diode are computed. The conduction losses depend on the forward voltage, which is dependent on the diode current. Therefore a `Vfwd()` funtion is defined based on datasheet values, as described in appendix F.1.2. Similarly, the junction capacitance of the diode. Similarly the junction capacitance is also voltage dependent, hence a voltage dependent function `Cj()` is defined, as described in appendix F.1.3. On lines 49 to 57 the conduction losses of the capacitors and inductors are computed.

Lines 59 to 75 revolve around computing the core losses of the inductors. Based on the winding current and the number of turns, the H-field is computed. With the H-field, the flux density can be obtained from the BH-characteristic. The BH-curve is non-linear due to saturation effects, so a function `B_curve()` is defined, returning the flux density based on the H-field magnitude in Ørsteds. The `B_curve_ultra()` and `B_curve_edge()` are for two different cores, but the approach is the same. The `B_curve()` functions are described in appendix F.1.4.

Finally the `P_loss_SEPIC()` function returns three values. The total conduction losses, the switching losses, and the core losses. For a coupled core, the core loss is split equally on each L_1 and L_2.

F.1.1 `Coss()` Function

To implement the voltage dependence on the output capacitance, data points from the datasheet curves are extracted [20]. These data points are used to interpolate for any voltage in-between, as seen in listing F.2

Listing F.2 `Coss()` function python code.

```
1 from scipy.interpolate import interp1d
2
3 vds_data = np.array([0, 40, 80, 120, 160, 200])
4 Coss_data = np.array([2900, 1100, 800, 600, 600, 600]) # in pF
5
6 Cds_interp = interp1d(vds_data, cds_data, kind='linear', fill_value='extrapolate')
7 def Cds(Vds):
8     return Cds_interp(Vds) * 1e-12 # Convert from pF to F
```

F.1.2 `Vfwd()` Function

To implement the non-constant forward voltage, data points from the diode datasheet are extracted [22]. With these data points a function is generated. This function is then used, as presented in listing F.3.

Listing F.3 `Vfwd()` function.

```
1 def Vfwd(I_D):
2     return 0.537*(I_D**0.138)
```

F.1.3 `Cj()` Function

To implement the voltage dependent junction capacitance, data points from the diode datasheet are extracted [22]. With these data points a function is generated. This function is then used, as presented in listing F.4.

Listing F.4 `Cj()` function.

```
1 def Cj(V_R):
2     return (1130.3*(V_R)**(-0.464))*1e-12
```

F.1.4 `B_curve()` Function

To generate the non-linear BH-curve, the function values are extracted for the relevant core. To ensure that the function is still functional for negative values of H-field, a logic is implemented as presented in listing F.5.

Listing F.5 `B_curve()` function.

```
1  a_core_L1 = 348.97
2  b_core_L1 = 2.015
3  c_core_L1 = 1.237
4  vol_core_L1 = 10.6 # cm3
5  def B_curve_ultra(H_field):
6      if H_field < 0:
7          H_field = abs(H_field)
8          return -((2.335e-2 + 1.000e-2*H_field + 1.774e-4*H_field**2)/(1 + 2.102e-2*H_field +
               1.072e-4*H_field**2))**1.374
9      else:
10         return ((2.335e-2 + 1.000e-2*H_field + 1.774e-4*H_field**2)/(1 + 2.102e-2*H_field +
               1.072e-4*H_field**2))**1.374
```

F.1.5 Shortfalls of the Python-based SEPIC Loss Algorithm

Within the time frame of this project some things have not been implemented in the `P_loss_SEPIC()`. For example per equation (A.4), inductance is dependent on permeability. This the inductance drop when the BH-curve begin to saturate. However in the `P_loss_SEPIC()`, for example in lines 10 and 11, the ripple current is a fixed value independent of the DC current.

Furthermore, the resistance and etc. of components are dependent on temperature. This is also not implemented in the algorithm in any form. All values from datasheets are considered at 25 °C

F.2 Small-signal Model Python Script

For numerical evaluation of the SEPIC small signal model, it is computed in Python. The python script computes the small signal states using equations (4.1) and (4.2). The Python code is presented in listing F.6.

Listing F.6 Python script for computing the SEPIC small-signal model.

```
import numpy as np
import control as ct

coupled = True
if (coupled):
    L1 = 166.67e-6/2
    L2 = L1
    M = 0.99*np.sqrt(L1*L2)
else:
    L1 = 166.67e-6
    L2 = 33.33e-6
    M = 0
C1 = 6.72e-6
C2 = 23.53e-6
R = 5

# Computing equilibrium points:
Vs = 35
Vout = 50
D = Vout/(Vout + Vs)

K = np.array([
    [L1,M,0,0],
    [M,L2,0,0],
    [0,0,C1,0],
    [0,0,0,C2]
])

A1 = np.linalg.inv(K) @ np.array([
    [0,0,0,0],
    [0,0,1,0],
    [0,-1,0,0],
    [0,0,0,-1/R]
])
A2 = np.linalg.inv(K) @ np.array([
    [0,0,-1,-1],
    [0,0,0,-1],
    [1,0,0,0],
    [1,1,0,-1/R]
])
B1 = np.linalg.inv(K) @ np.array([[1],[0],[0],[0]])
B2 = np.linalg.inv(K) @ np.array([[1],[0],[0],[0]])
CC1 = np.identity(4)
CC2 = np.identity(4)

```

```
# State space averaging:
A = A1*D + A2*(1-D)
B = B1*D + B2*(1-D)
C = CC1*D + CC2*(1-D)#np.array([[0,0,0,1]])

# States equilibrium:
X = -np.linalg.inv(A) @ B * Vs
U = Vs

# Computing the small-signal model:
A_ss = A1*D + A2*(1-D)
B_ss = (A1-A2)@X + (B1-B2)*U
C_ss = CC1*D + CC2*(1-D)
D_ss = 0

sys = ct.ss(A_ss,B_ss,C_ss,D_ss)

G_p = ct.ss2tf(sys)

Gvd = G_p[3,0]
Gvd = Gvd.minreal()
print('Gvd =', Gvd)

# Peak current control plant:
G_iswd = G_p[0,0] + G_p[1,0]
G_iswd = G_iswd.minreal()
print('G_iswd =', G_iswd)

# Outer voltage loop:
G_v = Gvd/G_iswd
G_v = G_v.minreal()
print('G_v =', G_v)
```

F.3 Microcontroller Embedded Software

The microcontroller i programmed using C code. The microcontroller is a TMS320F28069M by Texas Instruments. Thus it is coded and flashed through the code composer studio software. The implemented C code is presented in listing F.7. The main user code begins on like 122, everything prior to that is initialisation and configuration of registers.

Listing F.7 C code implemented in the microcontroller.

```
#include "DSP28x_Project.h"
#include "math.h"
#include <stdio.h>

__interrupt void ADC_isr(void);  // Declare interrupt

// PWM variables
float DutyC = 0.588;
float Fsw = 500e3;

// ADC variables
int Vin_RAW = 0;
int Vout_RAW = 0;
int I_L2_RAW = 0;
float Vin = 0;
float Vout = 0;
float I_L2 = 0;
float P_out = 0;

// Fault variables
int Vin_UV = 0;
int Vout_OV = 0;
int I_L2_OC = 0;

// Control variables
int control = 0;
float error = 0;
float error_prev = 0;
float DutyC_prev = 0;
float Vout_ref = 50;

void main(void)
{

    InitSysCtrl();  // TI device support function that initializes the System Control registers
    to a known state.

    // Disable all interrupts when configuring the MCU:
    DINT;           // Disable interrupts globally
    IER = 0x0000;   // Disable interrupts at CPU LEVEL
    IFR = 0x0000;   // Clear all CPU interrupt flags

    // Configuration of GPIO:
    InitGpio();     // TI device support function that initializes the Gpio to a known (default)
     state.
        // Define ePWM1A as an output
```

```
45          EALLOW;                                 // GPIO control registor is protected
46          GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 1; // Set GPIO function (GPIO0 = EPWM1A)
47          GpioCtrlRegs.GPADIR.bit.GPIO0 = 1;  // Set GPIO0 as an output
48          GpioCtrlRegs.GPAPUD.bit.GPIO0 = 1;  // Disable pull-up resistor on GPIO 0 (always
    disable pull-up resistor on an output)
49          EDIS;
50
51      // Configuration of the ePWM module
52          // Time-base submodule configuration
53          EPwm1Regs.TBCTL.bit.CLKDIV = 0;     // TBCLK will not be scaled. That is TBCLK = SYSCLK
54          EPwm1Regs.TBCTL.bit.HSPCLKDIV = 0;  // Like CLKDIV no scale is added to the TBCLK.
55          EPwm1Regs.TBCTL.bit.CTRMODE = 2;    // Up-down-mode
56          EPwm1Regs.TBPRD = 90e6/(2*Fsw);               // Setting the period to 90 CLK cycles.
    f_pwm = SYSCLK/(2*TBPRD)
57
58          // Counter-compare submodule configuration
59          EPwm1Regs.CMPCTL.bit.LOADAMODE = 2; // The CMPA value is loaded either on CTR = 0 or CTR
     = TBPRD
60          EPwm1Regs.CMPA.half.CMPA = DutyC * EPwm1Regs.TBPRD;
61
62          // Action-qualifier submodule configuration
63          EPwm1Regs.AQCTLA.bit.CAU = 1;        // Set PWM1A low at rising compare counter
64          EPwm1Regs.AQCTLA.bit.CAD = 2;        // Set PWM1A high at falling compare counter
65
66          // Dead-band submodule configuration
67          EPwm1Regs.DBCTL.bit.OUT_MODE = 0;   // Dead-band submodule is bypassed
68
69          // Trip-zone submodule configuration
70              // Input voltage sensor
71              EALLOW;
72              EPwm1Regs.TZSEL.bit.OSHT1 = 1;      // TZ1 signal is configured as a one-shot source
     for ePWM1 (Inductor current trip)
73              EPwm1Regs.TZCTL.bit.TZA = 2;        // Any trip-zone signal will force EPWM1A to a
    low state.
74              EDIS;
75
76          // Event-trigger submodule configuration
77          EPwm1Regs.ETSEL.bit.SOCAEN = 1;     // Enable EPWM1 ADC start of conversion mode
78          EPwm1Regs.ETPS.bit.SOCAPRD = 3;     // Trigger SOC pulse every 3rd event
79          EPwm1Regs.ETSEL.bit.SOCASEL = 1;    // SOC pulse is generated at TB counter = 0
80          EPwm1Regs.ETPS.bit.SOCAPRD = 1;     // Generate the SOC flag pulse on 1st events
81
82      // Configuration of the ADC
83      InitAdc();
84      EALLOW;
85      AdcRegs.ADCCTL1.bit.ADCENABLE = 1;          // Enable the ADC module
86      AdcRegs.ADCCTL1.bit.INTPULSEPOS = 1;        // INT pulse generation occurs 1 cycle prior to
    ADC result latching into its result register
87      AdcRegs.ADCCTL2.bit.ADCNONOVERLAP = 1;      // Enable non-overlap mode
88
89          // ADC0
90          AdcRegs.ADCSOC0CTL.bit.TRIGSEL = 5;         // Set SOC trigger source as EPWM1, SOCA
91          AdcRegs.ADCSOC0CTL.bit.CHSEL = 0;           // Channel selection of SOC0. Mapped to
    ADCINA0
```

```
92          AdcRegs.ADCSOC0CTL.bit.ACQPS = 10;          // Set acquisition period to 10 ADCCLK
93
94          // ADC1
95          AdcRegs.ADCSOC1CTL.bit.TRIGSEL = 5;         // Set SOC trigger source as EPWM1, SOCA
96          AdcRegs.ADCSOC1CTL.bit.CHSEL = 8;           // Channel selection of SOC1. Mapped to
    ADCINB0
97          AdcRegs.ADCSOC1CTL.bit.ACQPS = 10;           // Set acquisition period to 10 ADCCLK
98
99          // ADC2
100         AdcRegs.ADCSOC2CTL.bit.TRIGSEL = 5;         // Set SOC trigger source as EPWM1, SOCA
101         AdcRegs.ADCSOC2CTL.bit.CHSEL = 2;           // Channel selection of SOC2. Mapped to
    ADCINA2
102         AdcRegs.ADCSOC2CTL.bit.ACQPS = 10;           // Set acquisition period to 10 ADCCLK
103
104         AdcRegs.INTSEL1N2.bit.INT1E = 1;            // Enable interrupt generation
105         AdcRegs.INTSEL1N2.bit.INT1SEL = 2;          // EOC2 is trigger for ADCINT1
106         AdcRegs.INTSEL1N2.bit.INT1CONT  = 0;        // One shot mode - interrupt must be cleared
     by user before a new one can be received
107
108         AdcRegs.SOCPRICTL.bit.SOCPRIORITY = 3;      // SOC0-SOC2 are set to high priority
109     EDIS;
110
111     // interrupt configuration
112     InitPieCtrl();                              // TI device support function that initializes
    the PIE control registers to a known state.
113     InitPieVectTable();                         // TI device support function that initialize
    the PIE vector table with pointers to the shell Interrupt Service Routines (ISR).
114     EALLOW;
115     PieVectTable.ADCINT1 = &ADC_isr;            // Assign ISR address to ADCINT1 entry in the
    PIE vector table
116     EDIS;
117     PieCtrlRegs.PIEIER1.bit.INTx1 = 1;          // Enable ADCINT1 in the PIE group
118     IER = M_INT1;                               // Enable CPU interrupt line 1
119     EINT;                                       // Enable global interrupt
120     ERTM;                                       // Enable Global realtime interrupt DBGM
121
122     while(1)
123     {
124         // Protection mechanisms
125             if(Vin < 8){           // Input voltage UVLO
126                 EALLOW;
127                 EPwm1Regs.TZFRC.bit.OST = 1;    // Set the trip zone flag through software
128                 EDIS;
129                 Vin_UV = 1;
130             } else if(Vout > 57){   // Output over-voltage protection
131                 EALLOW;
132                 EPwm1Regs.TZFRC.bit.OST = 1;    // Set the trip zone flag through software
133                 EDIS;
134                 Vout_OV = 1;
135             } else if (I_L2 > 15){  // Over-current protection on output
136                 EALLOW;
137                 EPwm1Regs.TZFRC.bit.OST = 1;    // Set the trip zone flag through software
138                 EDIS;
139                 I_L2_OC = 1;
```

```
            } else{
                EALLOW;
                EPwm1Regs.TZCLR.bit.OST = 1;    // Clear the trip zone flag
                EDIS;
                Vin_UV = 0;                     // Status monitoring
                Vout_OV = 0;                    // Status monitoring
                I_L2_OC = 0;                    // Status monitoring
            }

        // Update EPWM registers
        EPwm1Regs.TBPRD = 90e6/(2*Fsw);                     // Update switching frequency
        EPwm1Regs.CMPA.half.CMPA = EPwm1Regs.TBPRD * DutyC; // Update duty cycle

    }
}

__interrupt void ADC_isr(void){

    // Assign the ADC values to variables
    Vin_RAW = AdcResult.ADCRESULT0;
    Vout_RAW = AdcResult.ADCRESULT1;
    I_L2_RAW = AdcResult.ADCRESULT2;

    Vin = (Vin_RAW*32.5)*(3.3/4095.0);
    Vout = (Vout_RAW*32.5)*(3.3/4095.0);
    I_L2 = (I_L2_RAW*20)*(3.3/4095.0);
    P_out = I_L2*Vout;

    if(control){
        error = Vout_ref - Vout;
        DutyC = 1.989e-5*error - 1.869e-5*error_prev + DutyC_prev;

        // Saturation implementation:
        if(DutyC > 0.6){
            DutyC = 0.6;
        }
        if(DutyC < 0.1){
            DutyC = 0.1;
        }

        error_prev = error;
        DutyC_prev = DutyC;
    }

    AdcRegs.ADCINTFLGCLR.bit.ADCINT1 = 1;                   // Clear ADC interrupt flag
    AdcRegs.ADCINTOVFCLR.bit.ADCINT1 = 1;                   // Clear the ADC overflow flag
    PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;                 // Acknowledge this line to receive
    more interrupts
    EPwm1Regs.ETCLR.bit.SOCA = 1;                           // Clear event-trigger flag to
    receive more SOCAs from ePWM module
}
```