DC Fault Performance in MTDC System

Active Fault Clearing by FB-MMC

MSc Thesis
Specialisation in Electric Power Systems and High Voltage Engineering

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Software programs utilized in the report.

1. MATLAB
2. PSCAD

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Abstract:

HVDC technology is a key enabler of large, interconnected power grids with high penetration of renewable energy sources. For a DC fault, the fault current behaviour and interruption capability are significantly influenced by the type of converter used. In line-commutated converter HVDC systems, the converters can rapidly interrupt the fault current. In modular multilevel converter-based HVDC systems, especially those using half-bridge submodules, fault current interruption relies on either AC or DC circuit breakers. DC circuit breakers can interrupt the fault current before the converter blocks; however, they are expensive and come with significant technical complexities. AC circuit breakers operate during the free-wheeling diode conduction phase from the AC side, resulting in relatively long fault clearance and system restoration times. This project focuses on utilising the full-bridge submodule configuration of modular multilevel converters with active fault-clearing capabilities in hybrid point-to-point and multi-terminal systems. Instead of passively blocking the fault current, an enhanced control strategy is employed, utilising the full operational range of the full-bridge.

Table 1: Nomenclature of abbreviations throughout the report.

Nomenclature	
Abbreviation	**Description**
Alternating Current	AC
Arm Average Model	AAM
Capital Expenditures	CAPEX
Circuit Breaker	CB
Circulating Current Suppression Controller	CCSC
Constant Current Control	CCC
Direct Current	DC
Fault Ride Through	FRT
Electromagnetic Transients	EMT
Extinction Angle Control	CEA
Freewheeling diode	FWD
Full Bridge	FB
Grid-forming	GFM
Half Bridge	HB
High Voltage Direct Current	HVDC
hybrid HVDC	hHVDC
Insulated Gate Bipolar Transistor	IGBT
International Electrotechnical Commission	IEC
Line Commutated Converter	LCC
Modular Multi-level Converter	MMC
Multi-terminal DC	MTDC
Overhead Line	OHL
Phase Locked Oscillator	PLO
Phase Locked Loop	PLL
Point of Common Coupling	PCC
Pre-insertion Resistor	PIR
Root Mean Square	RMS
Short Circuit Ratio	SCR
Submodule	SM
Technology Readiness Level	TRL
Voltage Source Converter	VSC

Table 2: Symbols used throughout the report.

Symbols	
Subscript	**Description**
P_{abc}	AC Instantaneous Active Power
P_{ref}	AC Active Power Reference for Outer Controller
I_{A}	AC Current – LCC
$I_{\text{s}\phi}$	AC Current – MMC ϕ for phase *a,b,c*
R_{s}	AC Grid Series Resistance
R_{sp}	AC Grid Parallel Resistance
L_{sp}	AC Grid Parallel Inductance
$R_{\text{s,r}}$	AC Grid Series Resistance-Rectifier Side
$R_{\text{sp,r}}$	AC Grid Parallel Resistance-Rectifier Side
$L_{\text{sp,r}}$	AC Grid Parallel Inductance-Rectifier Side
Q_{abc}	AC Instantaneous Reactive Power
Q_{ref}	Reactive Power Reference for Outer Controller
V_{S}	AC System Voltage RMS L-L
Z_{S}	AC System Impedance
L_{s}	AC System Inductance
$V_{\text{in,ac}}$	AC Voltage – LCC
$V_{\text{s}\phi}$	AC Voltage – MMC for Three Phases ϕ for phase *a,b,c*
$V_{\text{conv}\phi}$	AC Voltage behind arm inductance ϕ for phase *a,b,c*
$V_{\text{abc,ref}}$	AC Voltage Reference for Insertion Indices
C_{arm}	Arm Capacitance – MMC
L_{a}	Arm Inductance – MMC
R_{a}	Arm Resistance – MMC
V_{com}	Commutation Voltage
C_{tl}	Capacitance- Cable
C_{tlo}	Capacitance- OHL
C	Capacitance- MMC SM
i_{d}	Current Controller *d* Component Input Current
i_{q}	Current Controller *q* Component Input Current
$v_{\text{d,ref}}$	Current Controller *d* Component Output Voltage
$v_{\text{q,ref}}$	Current Controller *q* Component Output Voltage
i_{cd}	Circulating Current Suppression Controller *d* Component Input Current
i_{cq}	Circulating Current Suppression Controller *q* Component Input Current
$V_{\text{circ,ref}}$	Circulating Current Voltage Reference for Insertion Indices
$i_{\text{c,abc}}$	Circulating Current
S_{d}	Converter Power Rating
I_{d}	DC Current
P_{d}	DC Power
R_{dc}	DC Side Resistance
L_{d}	DC Smoothing Inductance
$L_{\text{dt,i}}$	DC Terminal Inductance
V_{d}	DC Voltage
$V_{\text{d,ref}}$	DC Voltage Reference for Outer Controller

Table 3: Symbols used throughout the report.

Symbols	
Subscript	**Description**
$V_{\mathrm{d,i}}$	DC Voltage – Inverter
$V_{\mathrm{d,r}}$	DC Voltage – Rectifier
γ	Extinction Advance Angle – LCC
I_{fpu}	Fault Current in pu
K_{SM}	DC Voltage Insertion Ratio
α	Firing Angle – LCC
V_{d0}	Ideal DC Voltage – LCC
β	Ignition Advance Angle – LCC
L_{tl}	Inductance -Cable
L_{tlo}	Inductance -OHL
$V_{\mathrm{s}\phi}$	Instantaneous AC Voltage ϕ for phase *a*,*b*,*c*
V_{circ}	Internal Circulating Voltage
$V_{\mathrm{l}\phi}$	Lower Arm Voltage – MMC ϕ for phase *a*,*b*,*c*
V_{cl}	Lower Arm Capacitance Voltage – MMC
$V_{\mathrm{l}\phi}$	Lower Arm Voltage – MMC ϕ for phase *a*,*b*,*c*
$i_{\mathrm{l}\phi}$	Lower Arm Current – ϕ for phase *a*,*b*,*c*
n_{l}	Lower Arm Insertion Indices – MMC
θ_{PLL}	Phase Locked Loop Angle
N	Number of Submodules
$v_{\mathrm{circ\ d,ref}}$	Out Voltage *d* Component of Circulating Current Suppression Controller
$v_{\mathrm{circ\ q,ref}}$	Out Voltage *q* Component of Circulating Current Suppression Controller
$i_{\mathrm{d,ref}}$	Outer Controller *d* Component Output Current
$i_{\mathrm{q,ref}}$	Outer Controller *q* Component Output Current
R_{tl}	Resistance-Cable and OHL
i_{sm}	Submodule Current
X_{tpu}	Transformer Reactance (pu)
C	Submodule Capacitance
$i_{\mathrm{u}\phi}$	Upper Arm Current – MMC ϕ for phase *a*,*b*,*c*
V_{cu}	Upper Arm Capacitance Voltage – MMC
n_{u}	Upper Arm Insertion Indices – MMC
$V_{\mathrm{u}\phi}$	Upper Arm Voltage – MMC ϕ for phase *a*,*b*,*c* .
K_p	Proportional Gain
K_i	Inegral Gain
R	Resistance
V	Voltage

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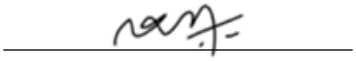
Preface

Aalborg University, May 28, 2025

This report has been developed as part of the master's thesis during the 4th semester of the MSc in Energy Engineering, with a specialisation in *Electric Power Systems and High Voltage Engineering* at Aalborg University. The main objective of the project was to examine DC fault performance in HVDC systems.

The models used in this thesis were developed in PSCAD, while calculations and plotting were performed using MATLAB. LaTeX was used for documenting the project work.

The author would like to thank AAU Energy for providing the resources, guidance, and support necessary throughout the master's studies. The author expresses sincere appreciation to the supervisor, Sanjay Chaudhary, for his valuable support and guidance throughout the thesis work. Gratitude is also extended to the contact persons, Stefan Frendrup Sörensen and Oliver Lukas Headley from Energinet, for their helpful comments and guidance. Lastly, the author wishes to thank fellow students and family for their encouragement and invaluable support throughout this journey.



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Summary

This thesis began by investigating the challenges associated with DC fault management in HVDC systems, particularly as they evolve into multi-terminal configurations. The converter plays a vital role in addressing DC faults in various HVDC systems. *line-commuted converters* (LCC) have excellent DC fault-clearing capabilities. Two configurations of *modular multilevel converters* (MMC)—the *half-bridge* (HB) MMC, which can act as a fault-feeding converter, and the *full-bridge* (HB) MMC, which functions in a fault-blocking capacity—exhibit distinct characteristics. Additionally, the FB module has extended operational capabilities and is capable of inserting negative voltages. This feature is chosen as the final objective of this research into fault-clearing methods. The LCC with FB-MMC forms a hybrid HVDC system that is a technically viable, cost-effective system model. The primary task involved is modelling the three types of converters to simulate DC fault scenarios effectively. Analysing the responses of both FB and HB configurations in blocking mode is essential for identifying the issues that arise during DC faults, which leads to the implementation of the active fault-clearing mode. Thus, modelling includes LCC, MMC-HB and MMC-FB configurations.For modelling and simulation, the EMT software PSCAD was selected. The LCC model is based on the CIGRÉ benchmark, while the MMC models were developed by drawing insights from academic literature and other reference materials. Both HB and FB MMCs were modelled using an arm-average approach, which incorporates blocking circuits in each arm. These circuits differentiate between the two submodule configurations on a fundamental level. A basic point-to-point hybrid HVDC system was developed, including all essential components for system-level DC fault analysis. This study focused on the time required for fault clearing. Initial simulations with the HB configuration assessed fault current characteristics and clearing times. The analysis was then extended to the FB-MMC operating in blocking mode. While the blocking mode quickly interrupts fault currents upon activation, it has drawbacks, including a loss of controllability and the occurrence of voltage transients. These findings underscored the necessity for an actively controlled fault-clearing method. Consequently, active fault clearing using FB-MMCs was implemented, leveraging their capability to generate bidirectional output voltages. The control strategies employed include generating a DC voltage reference to render the fault current zero, as well as implementing a basic arm sum voltage controller to regulate arm voltages and manage arm energy from the AC side, even in the event of DC voltage collapse.

Simulations of active fault clearing in both point-to-point and multi-terminal HVDC systems demonstrated improved performance compared to the blocking mode, particularly in terms of faster fault clearing and reduced voltage transients. The results presented in this thesis suggest that FB-MMCs, with enhanced control strategies, represent a viable and effective solution for managing DC faults in HVDC systems.

Contents

Chapter 1

Introduction

1.1 Motivation and Background

Nowadays, renewable energy is a key player in reducing carbon emissions and is also the cheapest form of energy that meets the growing energy demand. Countries and regions around the world have set ambitious renewable energy targets. For instance, the revised Renewable Energy Directive, adopted in 2023, establishes the European Union's binding renewable energy target for 2030 at a minimum of 42.5 % of total energy consumption. In 2024, 80 % of the growth in global electricity generation came from renewable sources and nuclear power, reflecting progress towards meeting targets [1] [2].

Thus, an unprecedented acceleration in electrification driven by renewable energy sources continues. This change requires a robust and flexible grid that harnesses and balances generation from distant locations across the region without curtailment. *High voltage direct current* (HVDC) technology is increasingly recognised as a vital technological choice in fostering or developing the power grid infrastructure due to its ability to transmit with high voltage and minimal losses over long distances and its enhanced control capabilities [3].

1.2 Development of HVDC Transmission System

The fundamental and widely implemented HVDC system architecture is a point-to-point HVDC link. The advancement of HVDC transmission systems is ongoing and is undoubtedly progressing toward a *multi-terminal DC* (MTDC) system. A MTDC system consists of multiple connections on the DC side [4]. Research continues to investigate how different technological features can be added to address various operational challenges in the HVDC transmission system, layered in three areas of engineering: power transmission, power electronics, and control engineering [5]. Figure 1.1 outlines the conceptual framework of the HVDC system architecture by building blocks from three engineering layers.

The technical challenges in developing an HVDC transmission system are to be addressed based on different key parameters of the building blocks. The *technology readiness level* (TRL) and performance capabilities of various building blocks under these layers differ. For example, for HVDC transmission, the main power electronics converter topologies are *line commutated converter* (LCC) and *voltage source converter- modular multi-level converter* (VSC- MMC). Regarding TRL, the LCC is a widespread, technologically mature building

block, whereas the VSC-MMC with a *full bridge-submodule* (FB-SM) configuration is in the early stages of implementation [6]. The FB-SM indicates a full bridge rectifier configuration of semiconductor switches as a basic module. However, the performance levels of these converters under normal and fault conditions differ, and they need to be deployed as required to leverage their potential benefits.

Figure 1.1 provides a general outline of how the transmission system is structured, highlighting key parameters that influence the selection of building blocks in various engineering layers. However, it does not encompass all the factors that can affect this process. The components may vary in their levels across parameters. Also, the performance at one engineering layer can require or impact specific choices in other layers. Creating an HVDC system architecture necessitates a detailed study of various engineering aspects, with component selection often driven by system requirements related to cost and reliability.

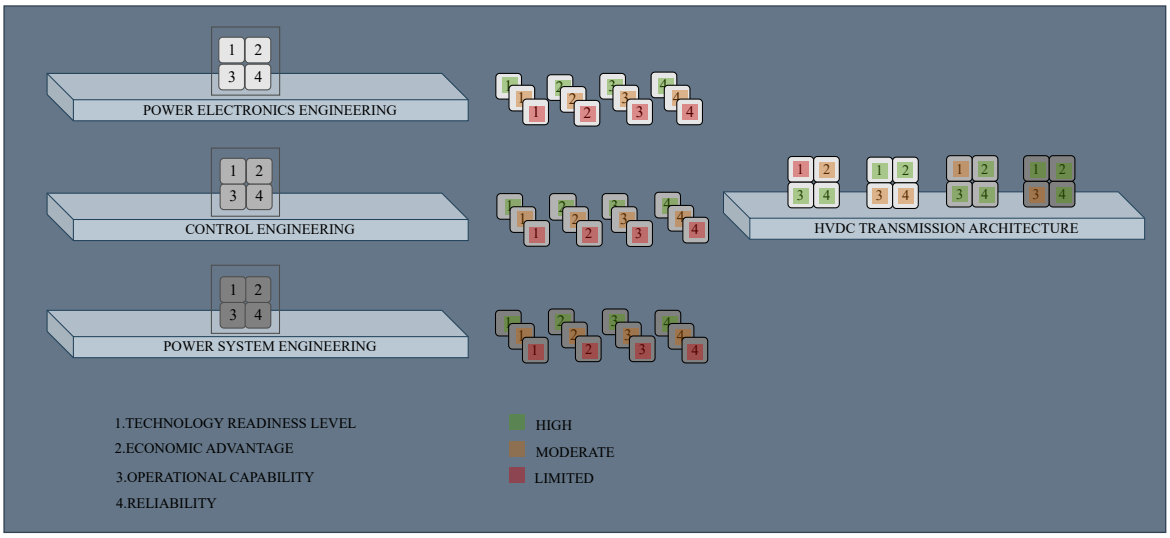


Figure 1.1: HVDC architecture conceptual framework: engineering layers and decision criteria.

Some of the HVDC projects have been implemented or are under implementation, showcasing the evolving diverse HVDC system architectures noted here. The ULTRANET – A-Nord project [7] is groundbreaking for being the first to implement FB-SM MMC technology. Wudongde UHVDC project in China [8] is a three-terminal VSC-LCC hybrid HVDC system. The Caithness-Moray-Shetland project [9] features a five-terminal HVDC configuration, and the project Aquila [10] is an initiative to achieve multiterminal, multi-vendor interoperability.

For a given point-to-point or multi-terminal HVDC system, the converter is one of the primary factors determining various system-level characteristics. Table 1.1 analyses the critical characteristics of two converter technologies and how they behave at the system level [5] [8].

Parameter	**LCC**	**MMC-VSC**
Semiconductor	Thyristor	IGBT
Device level losses	Negligible switching losses Low on state losses	Low switching losses Moderate on state losses
Converter Transformers	Higher Insulation	Standard AC transformers
Transmission medium	No XLPE	Suitable for OHL and Cable
Independent Power Control	No. Q control with statcom	Yes
Rating	Up to 12 GW DC voltage:1100 kV	Up to 5 GW DC voltage:800 kV
AC Fault ride through	Possible	Excellent
DC fault handling	Excellent	Depends on SM topology
Power restoration	No	Yes
Foot Print	Large : Harmonic filters , Reactive compensation	Less : Less filters No reactive compensation
Cost	Less	Higher than LCC
Multiterminal configuration	Feasible with limitation	Any number of terminals

Table 1.1: Comparison of LCC and VSC-MMC.

Different technical challenges in operating HVDC systems are noted in the literature [3] [11] [4] [8]. One of the key performance challenges is the DC side fault performance and protection. Unlike the AC system, the DC system lacks a zero crossing and offers low impedance. Because of this, the fault current's rise time is shorter, and the peak and steady-state fault currents are high [12]. As noted in Table 1.1, the converter behaviour under DC fault events differs significantly. For a point-to-point system with LCC, primarily due to the converter's phase shift reversal and thus the reversal of voltage, the HVDC control mitigates fault transients; consequently, the AC system is rarely affected. For a VSC-MMC-based grid, the DC fault mainly results in power loss between the connected AC grids, depending on the submodule configuration. In the widely implemented *half-bridge submodule* (HB-SM) configuration known as the fault feeding MMC, where the freewheeling diodes continue to feed the fault. This uncontrolled rectifier action necessitates the disconnection of the AC grid by the AC circuit breaker (CB) unless a high-speed DC circuit breaker is implemented. The FB-SM is a fault-blocking converter, capable of providing the voltage at two different polarities. This characteristic produces excellent DC fault behaviour with negligible impact on the AC grid.[13]

In this context, the question arises as to whether the grid can tolerate the loss of a DC link, and this depends on the size of the DC system integrated into the grid. A high-power rating DC link or a multiterminal system is particularly significant compared to the connected AC system. Therefore, when expanding or designing the HVDC system, the chosen converter configuration must be capable of fast recovery from transient faults within the HVDC system or *DC fault ride-through* (DC FRT).

1.3 Problem Summary and Definition

The VSC-MMC is considered state-of-the-art technology due to its operational capabilities, making it a suitable choice for a second converter in a point-to-point system alongside one LCC, as well as for developing a multiterminal system [8] [11]. On the other hand, the HB-SM topology of the VSC-MMC lacks DC FRT capability. In a hybrid point-to-point system, DC fault performance at the VSC side can be improved with FB-SM through the use of an appropriate power converter control [8]. This provides excellent DC fault performance in a hybrid HVDC system, as both converters feature fast fault clearing. For multiterminal systems, various protection strategies have been proposed as research outcomes, although they have not yet been finalised as a grid code. These strategies depend on converter topology, fault clearing time, and available protection equipment [13].

CIGRE TB:739 states *"DC grid protection is a trade-off between cost and availability"* and classifies the protection strategies broadly as follows [14]:

- Non-selective fault clearing
- Partial selective fault clearing
- Full selective fault clearing

Fully selective and partially selective fault clearing require a DCCB, but the costs of DCCBs are relatively high [14]. In this context, applying FB-MMC presents a balanced solution; research proposes actively controlling the voltage reversal in FB-MMC and reducing the fault current rather than blocking the converter.[8] Therefore, this thesis focuses on implementing FB-MMC for DC fault management in hybrid HVDC point-to-point and multiterminal systems.

This project aims to evaluate the performance of hybrid point-to-point and multi-terminal HVDC systems during a DC fault with FB-MMC, with the goal of improving their fault-clearing and thus system restoration time. The emphasis is on devising a control system for active fault clearing that provides a negative voltage during a DC fault, thereby quickly reducing and clearing the fault current without losing the controllability of the converter. The point-to-point hybrid HVDC system has been further developed into multiterminal systems by adding VSC-MMC converters for two reasons: VSC-MMC converters are recognised as the future converter topology [11] for MTDC, and the DC FRT for LCC is not considered a significant technical challenge [5].

1.3.1 Problem Formulation

How can active fault clearing control with FB-MMC improve the DC fault performance of different HVDC system architectures by reducing fault current and enabling fast fault clearing?

Thesis Objectives

To answer the problem formulation, the following objectives are defined:

- Understand converter topologies LCC and VSC-MMC, fundamental principles, and switching actions determining fault-blocking capability. Investigate DC fault characteristics and converter performance during fault conditions.
- Develop VSC-MMC models for both HB and FB submodule configurations, incorporating fault-blocking capability. Implement appropriate control strategies for normal operation and fault conditions to ensure controllability of the FB-MMC during faults.
- Implement a hybrid system combining LCC with two types of MMC SM configurations—HB or FB—in a point-to-point system and develop it further into a multi-terminal system with the FB-MMC configuration.
- Analyse DC fault performance, considering various factors affecting the DC fault behaviour, across the system configurations implemented.

1.4 Limitations and Assumptions

Some limitations and assumptions are made for the project. These limitations are listed below:

- The converter model primarily assesses DC fault performance. The control tuning is based on general control philosophies, and no further detailed tuning has been implemented.
- The DC transmission system is modelled with the necessary components; mechanical disconnector switches are provided as a required minimum. Surge arresters are not included.
- The AC grid connected to the DC system is an aggregated voltage resource with characteristics relevant for DC fault studies.
- The system restoration after a DC system failure in simulation cases is not included in the scope of this study.

1.5 Outline of the Thesis

The organisation of the thesis is as follows.

- **Chapter 2** describes the HVDC system architecture, different converter operation principles and switching states, and also details DC fault characteristics along with converter DC fault performance.

- **Chapter 3** provides details on the modelling of the HVDC system configuration used in this thesis, along with the converters LCC, HB-MMC, and FB-MMC. The MMC converters have been modelled with blocking capability. A general control scheme for the normal mode of operation of converters is provided. The necessary modifications to the control scheme for fault blocking mode and active fault clearing are presented.

- **Chapter 4** explains the simulation of a hybrid system combining LCC with two types of MMC SM configurations—HB or FB—in a point-to-point system, along with steady state operation and DC fault performance.

- **Chapter 5** explains the simulation of a hybrid system combining LCC with FB—MMC in a multiterminal system, along with steady state operation and DC fault performance.

- **Chapter 6** discusses and provides a comparison of the fault clearing process in hHVDC systems with three fault clearing methods: HB-MMC blocking, FB-MMC blocking and FB-MMC active fault clearing.

- **Chapter 7** provides the conclusions of the project work along with recommendations for potential avenues of future research.

Chapter 2

HVDC System Architecture and DC Fault

This chapter provides the theoretical background necessary for understanding HVDC transmission systems, including an introduction to system configurations and the vital components—converters. It also examines DC fault behaviour, with a detailed analysis from the converter perspective. This chapter is organised as follows: Section 2.1 introduces the HVDC system architecture and provides details about the converters, LCC and VSC MMC. Section 2.2 outlines the characteristics, challenges, and potential solutions associated with the hybrid HVDC system, which is the selected architecture for analysing DC fault performance in this thesis. Finally, Section 2.3 discusses the characteristics of DC faults and analyses DC system protection, with a particular focus on converter topology.

2.1 HVDC System Architecture

As introduced in 1, the fundamental and widely implemented HVDC system architecture is a point-to-point HVDC link. This system consists of core building blocks, converters named as rectifiers that convert AC voltage to DC voltage, and inverters that convert DC voltage back to AC. Additional components of the system include the transmission medium, which can be DC cables or overhead lines; converter transformers, DC CB or other DC switches; and inductors that limit fault current rates [6]. Figure 2.1 outlines the different HVDC system configurations from a fundamental level to a DC grid.

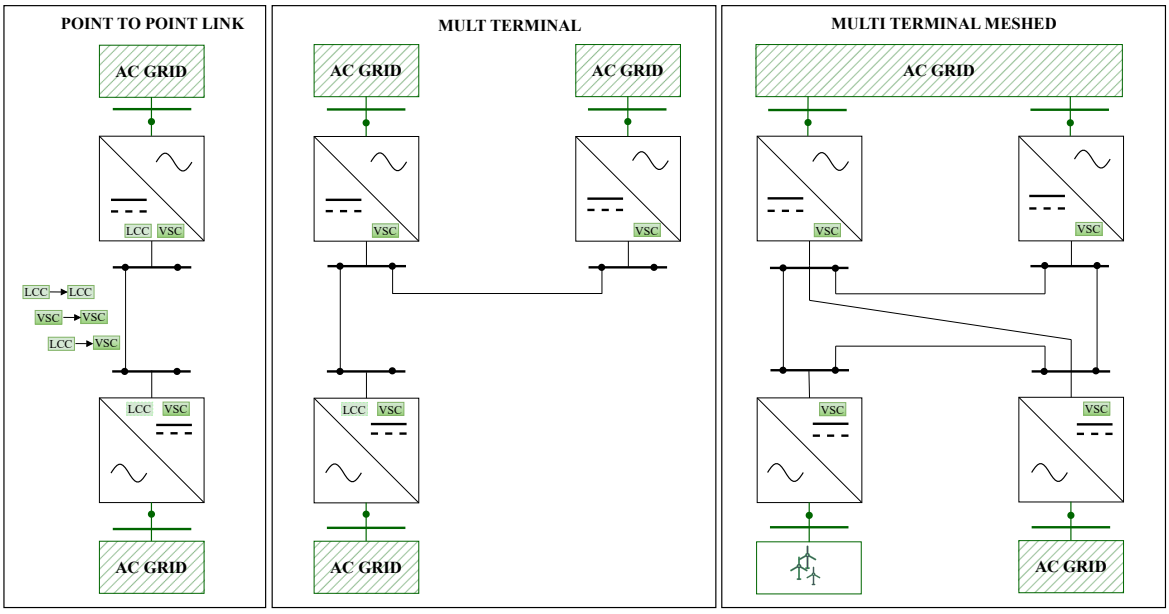


Figure 2.1: Schematic of HVDC system architecture at different levels.

Further expanding the scope from the building blocks to the HVDC transmission at the system level, the system configuration can be broadly classified as follows [5] [15].

- **HVDC Transmission System**: This system, simply referred to as an HVDC transmission system, is a point-to-point link that connects two converters. If the converters consist of LCC and VSC-MMC technologies, the configuration is a hybrid HVDC system. LCC is recommended for rectifier action in a hybrid system with a VSC converter at the inverter side to avoid commutation failure. [8].
- **Mutiterminal HVDC**: This refers to a DC system with more than two terminals connected to a single DC line, however, not including any meshed connections between converters.
- **DC Grid** : This refers to a DC transmission system characterised by more than two terminals, which includes at least one meshed connection between the converters.

The rationale for developing HVDC grids is that they provide an economical solution through resource sharing and increased reliability, as the loss of one line will not lead to a loss of load or resources [14]. The economic advantage of hybrid HVDC systems is that the cost-effectiveness of LCC for high-power transmission can be combined with the upsides of VSC-MMC [8]. Having stated that, the technology readiness for implementing various HVDC systems necessitates a detailed study from the perspective of different engineering layers. As indicated in Chapter 1, the DC fault and DC side protection are significant concerns for the HVDC grid development. For hybrid HVDC, HB SM topology is a bottleneck for DC fault performance. Amidst available technological options, FB-SM is a choice for addressing the DC fault performance challenges. Section 2.3 explains the DC fault and performance through the converter topologies. Before that, the technical background of converter topologies relevant to this project and the hybrid HVDC system architecture will be explained in the following sections.

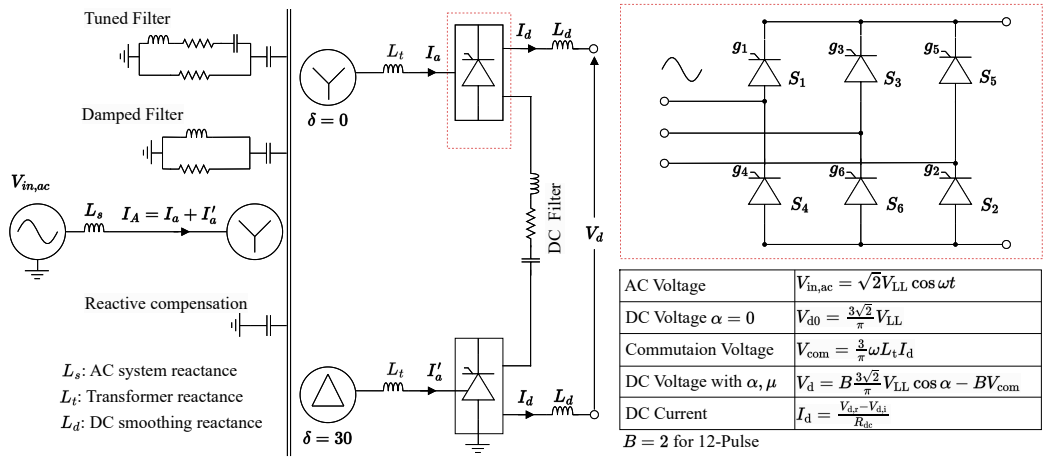
2.1.1 Line Commutated Converter

A six-pulse thyristor, known as the Graetz bridge, is the basic LCC converter topology for three-phase AC-to-DC conversion. A 12-pulse converter is formed with two similar Graets bridges and phase-shifting transformers. It is generally used in the HVDC transmission system with the advantage of reduced harmonics because of a higher number of pulses.[16]

The Graets bridge consists of six thyristors that act as partially controllable diodes fired with a gate current. The firing angle denoted by α decides the point at which the thyristor switch starts to conduct from the zero reference point of voltage: the operation as a rectifier set by the angle 0° - 90° and the inverter by 90° - 180°. An increase in the firing angle of over 90° makes the DC voltage negative, and with the reverse power flow, the inverter mode operation is facilitated.

The LCC, being a half-controlled rectifier, the switching off of one converter or the commutation of thyristor from one circuit to the other happens naturally at zero voltage

crossing. The commutation from one switch to another in a bridge circuit does not occur instantaneously. The AC side transformer inductance causes the thyristor's conduction to continue even if the other alternate valve is fired to commutate. This makes the commutation overlap for a period μ, known as the commutation overlap angle, and results in a commutation voltage drop that reduces the output DC voltage [17]. For the inverter operation, the ignition advance angle $\beta = 180 - \alpha$ and extinction advance angle $\gamma = 180 - \alpha$ are defined .[5]. Figure 2.2 illustrates the components of a 12-pulse LCC system. These include the transformers that provide a 30° phase shift, AC and DC side harmonic filters, and a capacitive bank for reactive power compensation. For ease of reference, a summary of related equations is also provided.



AC Voltage	$V_{\text{in,ac}} = \sqrt{2} V_{\text{LL}} \cos \omega t$
DC Voltage $\alpha = 0$	$V_{\text{d0}} = \frac{3\sqrt{2}}{\pi} V_{\text{LL}}$
Commutaion Voltage	$V_{\text{com}} = \frac{3}{\pi} \omega L_{\text{t}} I_{\text{d}}$
DC Voltage with α, μ	$V_{\text{d}} = B \frac{3\sqrt{2}}{\pi} V_{\text{LL}} \cos \alpha - B V_{\text{com}}$
DC Current	$I_{\text{d}} = \frac{V_{\text{d,r}} - V_{\text{d,i}}}{R_{\text{dc}}}$

$B = 2$ for 12-Pulse

Figure 2.2: 12 Pulse LCC converter topology.

For LCC, the DC voltage depends on the firing angle α, with a 60° phase difference applied for each thyristor in a 6-pulse bridge configuration. The rectifier controls the current in a point-to-point connection with two LCCs, while the inverter regulates the DC voltage. As shown in Figure 2.2, the DC current is a function of the difference in converter voltages and the total DC side resistance R_{dc}. The primary control strategy for the LCC system is power control. Typically, the rectifier operates in *constant current control* (CCC) mode. It is essential to note that as the firing angle exceeds 90° for inverter operation, the duration available before the zero voltage crossing decreases; therefore, it is necessary to maintain a minimum extinction angle. For example, during the commutation from S1 to S3, the extinction and ignition are advanced by β and γ angles from the zero crossing. This indicates the inverter operates under constant *extinction angle control* (CEA) rather than a constant DC voltage control. The CEA control can regulate the rectifier side firing angle α to prevent commutation failure under steady-state conditions [5].

2.1.2 Voltage Source Converter

VSCs are equipped with IGBT switches, which can self-commutate as needed and do not rely on the connected grid. As a result, VSC can control both active and reactive power independently, allowing it to synthesise the voltage with a specific magnitude and

phase angle. This offers higher controllability compared to LCC. Initially, the 2-level VSC was engineered, offering two voltage levels and having a small DC-link capacitor as a short-term energy source. One of the drawbacks of the 2-level VSC is that it operates at high switching frequencies, which results in higher losses and makes it not promising for high-power applications. A breakthrough in HVDC transmission occurred with the introduction of the VSC-MMCs. Hereafter, this converter is referred to simply by MMC in the thesis.

As mentioned in Chapter 1, there are two submodule configurations for MMC: the technologically mature HB-MMC and the newer FB-MMC, which is now commercially available. A HB-MMC-SM can provide only zero and positive cell voltages. Each FB-SM can achieve multiple AC voltage states, including 0, positive and negative cell voltages, which enhances redundancy and allows for negative DC voltage operation. While this added redundancy is not typically required in normal HVDC operation, it can be advantageous during abnormal conditions like DC faults [5]. This section begins by detailing the circuit topology and internal dynamics of the MMC, utilising an average model applicable to HB and FB configurations, except that the arm voltage source can have reverse polarity. Following that, the operation of the FB-MMC is examined in terms of how it differs from the HB-MMC, primarily in its switching sequence.

The MMC is formed by connecting a large number of submodules in series, which are fundamentally 2-level VSCs. This configuration allows multiple DC voltage levels within the converter, thus enabling switching at the submodule level. As a result, the converters operate at lower switching frequencies and reduce losses, making it ideal for high-voltage and high-power applications. The MMC consists of a lower-level control to balance the capacitor voltages by inserting and bypassing SM capacitor voltages, thereby generating the desired output voltage based on the reference from the outer control loop [18]. HB-MMC, with its modular structure having N numbers of SMs, produces $N+1$ voltage levels. The different capacitor voltage balancing methods are described in [18]. Modelling MMC at the SM level leads to $2(N+1)$ state variables, making the computation extensive. Therefore, the averaging principle at the arm level is applied in MMC's modelling and simulation studies, where each arm is aggregated as a controllable voltage source. Examining the Figure 2.3, the circuit relationship of each arm can be written as in Equation (2.1) and Equation (2.2) according to Kirchhoff's law.

$$V_{s\phi} = \frac{V_d}{2} - V_{u\phi} - \left(L_a \frac{d}{dt} + R_a\right) i_{u\phi} \tag{2.1}$$

$$V_{s\phi} = -\frac{V_d}{2} + V_{l\phi} - (L_a \frac{d}{dt} + R_a) i_{l\phi} \tag{2.2}$$

Where V_d denotes the DC pole-to-pole voltage and $V_{s\phi}$ denotes the AC input voltage.The terms $V_{u\phi}$ and $V_{l\phi}$ are the upper and lower arm voltages, respectively. $i_{u\phi}$ and $i_{l\phi}$ are the corresponding arm currents. L_a is the arm inductance which limits the current transients and R_a is the arm resistance accounting for arm conduction losses. From these relations stated, the current and voltages of the upper and lower arms in terms of the AC and DC side voltages can be formulated as in Equation (2.3) and Equation (2.4), respectively. It is important to note that the voltage drop caused by the arm's reactance and resistance

is added to the AC-side voltage to represent the internal AC voltage generated by the converter, denoted as $V_{\text{con}\phi}$.

$$V_{\text{u}\phi} = \frac{V_\text{d}}{2} - V_{\text{con}\phi} \qquad (2.3)$$
$$i_{\text{u}\phi} = \frac{i_{\text{s}\phi}}{2} + \frac{i_\text{d}}{3}$$

$$V_{\text{l}\phi} = \frac{V_\text{d}}{2} + V_{\text{con}\phi} \qquad (2.4)$$
$$i_{\text{l}\phi} = \frac{-i_{\text{l}\phi}}{2} + \frac{i_\text{d}}{3}$$

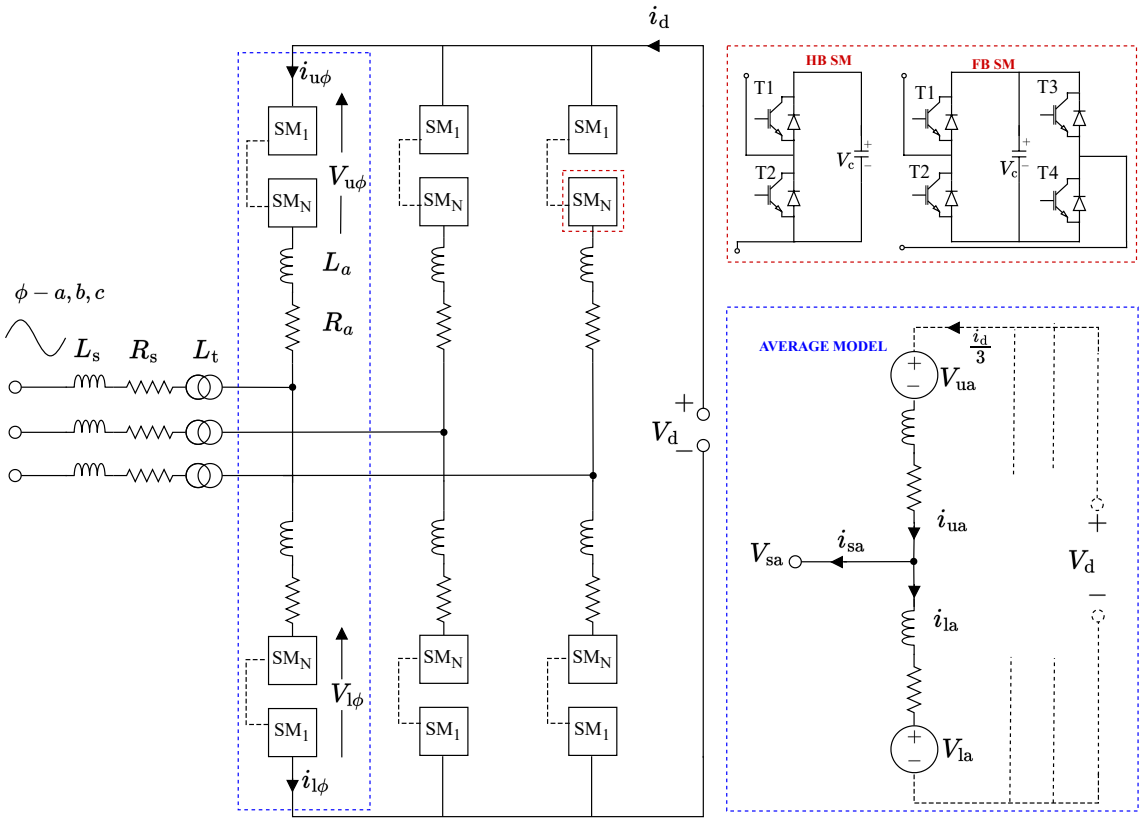


Figure 2.3: MMC topology with average model and submodule.

The capacitor voltage must be balanced across one leg such that the sum of arm voltages in one arm is equal to the DC link voltage V_d. Now, as the arm currents flow, the capacitor is charged, and the expression for the capacitor voltage of either the upper or lower arm is expressed by Equation (2.5) in terms of arm currents and insertion indices.

$$\frac{C}{N}\frac{d}{dt}(V_{\text{c(u,l)}}) = n_{\text{(u,l)}}.i_{\text{(u,l)}\phi} \qquad (2.5)$$

where C is the submodule capacitance and N is the number of submodules. Insertion indices can be defined as the ratio of the number of submodule cells in the ON state to

the total submodules in the arm, or, equivalently, as the ratio of arm voltage available to generate a required output voltage to the total arm voltage possible. Instead of individual capacitor cell switching status, this is expressed as a continuous variable for the average model in terms of the voltages as provided in Equation (2.6) for the upper arm and in Equation (2.7) for the lower arm.

$$n_{\mathrm{u}} = \frac{\frac{V_{\mathrm{d}}}{2} - V_{\mathrm{con}\phi} - V_{\mathrm{circ}}}{V_{\mathrm{d}}} \tag{2.6}$$

$$n_{\mathrm{l}} = \frac{\frac{V_{\mathrm{d}}}{2} + V_{\mathrm{con}\phi} - V_{\mathrm{circ}}}{V_{\mathrm{d}}} \tag{2.7}$$

V_{circ} is the internal voltage driving the circulating current. An internal closed-loop control known as the *circulating current suppression controller* (CCSC) is used in MMCs to eliminate or minimise the circulating current [19].

FB-MMC with Switching State

During each conducting stage, the HB-MMC uses one switch, whereas the FB-MMC uses two switches; this results in higher conduction losses for the FB-MMC. However, FM MMC offers the advantages of fault-tolerant capability with negative voltage during the blocked states and the ability to work in overmodulation [20]. Additionally, [19] mentions that the FB-MMC requires only 50 % of the total DC bus voltage V_d to achieve the same AC output voltage as the HB-SM-based MMC, assuming identical power ratings and the same number of SMs. Consequently, each FB-SM capacitor can have a voltage rating of 75 % of an HB-SM capacitor, and the FB-SM-based MMC exhibits a lower capacitor voltage ripple.

MMC operation consists of inserted, bypassed and blocked switching states at the individual submodule level, which generates the required capacitor voltage in the arm[18]. For brevity, these switching states for HB and FB are presented in Table 2.1 and Table 2.2, with further pictorial illustrations provided in the Appendix A.

Operating Mode	**Conduction**	v_{sm}
Inserted	$D1$ for $i_{sm} > 0$, $T1$ for $i_{sm} < 0$	V_c
Bypassed	$T2$ for $i_{sm} > 0$, $D2$ for $i_{sm} < 0$	0
Blocked	$D1$ for $i_{sm} > 0$,	V_c
Blocked	$D2$ for $i_{sm} < 0$,	0

Table 2.1: HBSM switching states.

Operating Mode	**Conduction**	v_{sm}
Inserted	$D1$ and $D4$ for $i_{sm} > 0$, $T1$ and $T4$ for $i_{sm} < 0$	V_c
Inserted	$T2$ and $T3$ for $i_{sm} > 0$, $D2$ and $D3$ for $i_{sm} < 0$	$-V_c$
Bypassed	$D1$ and $T3$ for $i_{sm} > 0$, $D3$ and $T1$ for $i_{sm} < 0$	0
Bypassed	$T2$ and $D4$ for $i_{sm} > 0$, $T4$ and $D2$ for $i_{sm} < 0$	0
Blocked	$D1$ and $D4$ for $i_{sm} > 0$,	V_c
Blocked	$D2$ and $D3$ for $i_{sm} < 0$,	$-V_c$

Table 2.2: FBSM switching states.

From the switching states shown above, it is noted that from the zero to maximum AC voltage, the DC voltage can be varied from positive to negative using the different capacitor voltage levels. The individual inserted and bypassed states provided here can be replaced by the continuous variable insertion indices for the entire arm in the average model. So, the expression for insertion indices provided by Equation (2.8) and Equation (2.9) can be modified by introducing a variable K_{SM} as follows [5].

$$n_{\mathrm{u}} = \frac{K_{SM}\frac{V_{\mathrm{d}}}{2} - V_{\mathrm{con}\phi} - V_{\mathrm{circ}}}{V_{\mathrm{d}}} \tag{2.8}$$

$$n_{\mathrm{l}} = \frac{K_{SM}\frac{V_{\mathrm{d}}}{2} + V_{\mathrm{con}\phi} - V_{\mathrm{circ}}}{V_{\mathrm{d}}} \tag{2.9}$$

Where $0 < K_{\mathrm{SM}} < 1$ for HB and $-1 < K_{\mathrm{SM}} < 1$ for FB.
In blocking mode, the IGBTs in the half-bridge submodules stop conducting, while the freewheeling antiparallel diodes allow current to flow through the converter. In the FB, two diodes enable current flow through the capacitor cell, resulting in a negative cell voltage that stops the current at the system level through the converter. Also, the extended range of DC voltage insertion ratio for FB-MMC can provide controlled voltage during fault conditions, making it an ideal choice to overcome challenges at the system level during abnormal conditions.

2.2 Hybrid HVDC Transmission System

Hybrid HVDC transmission systems, hereafter abbreviated as *Hybrid HVDC* (hHVDC), when engineered with unidirectional power flow, address the limitations of LCC in reversing power flow and commutation failure at the inverter side, while taking advantage of its low-cost, high-power transmission capabilities [21]. The demand for long-distance, high-power UHVDC transmission in countries like China and India, from remote generation resources, further promotes the use of this hHVDC transmission system [22]. Notable projects, including that hybrid at the system and converter level, can be referred in [23] [8]. For providing the technical background of hHVDC systems, this section is divided into two parts. Section 2.2.1 details the basic configuration of the system, including the transmission components and the converter control philosophy. Section 2.2.2 analyses the performance requirements and limitations, along with a review of FB-MMC as a potential solution.

2.2.1 hHVDC System Configuration and Control

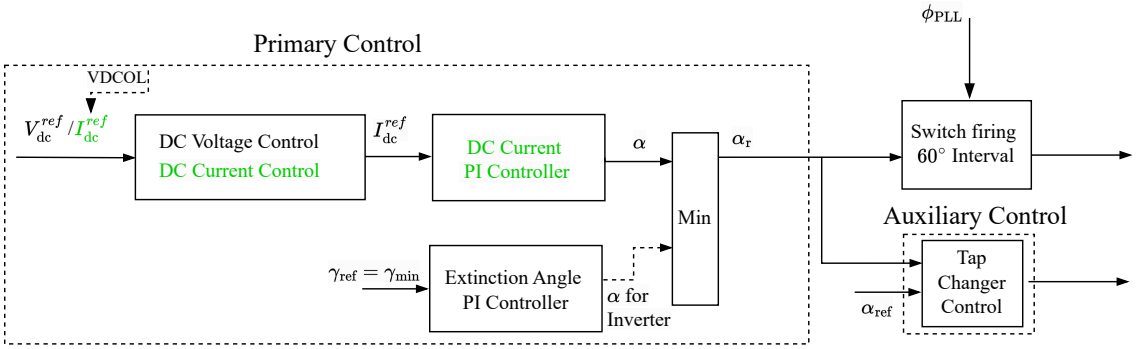
In the HVDC system, the configuration and system components consist of both VSC and LCC at each corresponding side. Unlike the point-to-point systems that use only LCC or VSC, the VSC side of the hybrid system employs a FB-MMC topology to meet performance requirements [8] instead of HB-MMC. Both converter sides are connected to the AC grid through power transformers. The transformers on the LCC side must be

capable of withstanding high harmonic currents and AC and DC voltage stress. In contrast, on the MMC side, stress depends on the connection between the converter, transformer, and AC side filter [24]. On the LCC side, harmonic filters are necessary for both the AC and DC sides, as well as capacitor banks for reactive power compensation. The MMC side has arm-level reactance and pre-insertion resistors to prevent transients during energisation. With unidirectional power flow, the hybrid system can use *overhead lines* (OHL) and cables as transmission mediums. Notably, implemented HVDC projects, such as UHVDC long transmission systems, prefer OHLs [25].

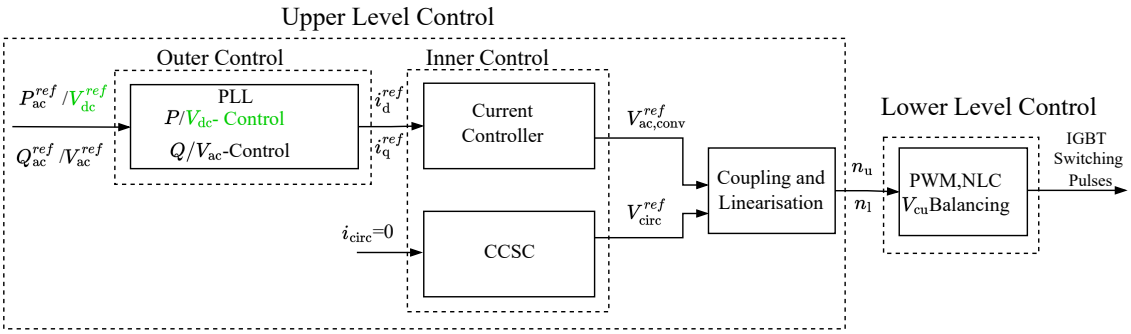
LCC and VSC utilise distinct control strategies, as illustrated in Figure 2.4. The VSC features a faster response time and greater flexibility. Hence, VSC is selected to stabilise the DC voltage in hybrid systems. Meanwhile, the LCC operates in DC current control mode. Hence, the steady state DC current, as noted in Figure 2.2 can be rewritten as follows.

$$I_{\mathrm{d}} = \frac{(B\frac{3\sqrt{2}}{\pi}V_{\mathrm{LL}}\cos\alpha - BV_{\mathrm{com}}) - V_{\mathrm{d}}}{R_{\mathrm{dc}}} \tag{2.10}$$

Reference [25] suggests incorporating additional measures, such as a backup converter station on the VSC side and implementing voltage and current margin control for LCC and VSC, respectively. The DC power or current on the LCC side is regulated through alpha control, which generates a higher DC voltage, taking into account the voltage drop along the transmission line. On the inverter side, the DC voltage is controlled at 1.0 pu.



(a) HVDC Control for LCC: Green for rectifier operation at hybrid system.



(b) HVDC control for VSC: green for inverter operation at hybrid system.

Figure 2.4: Control overview for hybrid HVDC transmission system.

In a hybrid system, the LCC also implements voltage margin control, otherwise known as α limit control. Normally, when there is an active power change in the system, the MMC capacitor either charges or discharges to maintain a stable DC voltage. This ensures the active power is regulated and the DC voltage is maintained. The voltage margin control includes a DC voltage controller at the LCC, which sets maximum and minimum limits for the DC current controller on the LCC side. As a rectifier in the hybrid system, the output of the LCC's DC voltage controller establishes a lower limit for the LCC current controller, maintaining a minimum alpha angle. Similarly, current margin control can be implemented on the MMC side. When the LCC station enters a minimum firing angle control mode and the LCC determines the DC voltage, the VSC station controls the DC current.

2.2.2 hHVDC System Performance and Adaptations

The introduction of the MMC converter, rather than relying exclusively on the LCC-based HVDC transmission system, enhances its performance by utilising the inherent capabilities of the MMC, as noted in the Table 1.1. However, with different power conversion principles of these converters, the performance of the whole hHVDC transmission system faces specific challenges. Here, the performance of hHVDC system is analysed based on its operation range of voltage and current. Fundamentally, the LCC works as a constant current source, and the VSC as a constant voltage source. The LCC offers a DC current range, from a minimum value of 0.1 pu to 1.0 pu, with two-quadrant operation for voltage. For VSC with an HBSM MMC configuration, it can offer a voltage range of 0 to 1.0 pu, although the effective operational range is typically from 0.85 to 1.0 pu with two-quadrant operation for current. While combining the ranges of each results in a highly restricted operating range of single-quadrant operation for both voltage and current. This range supports only the minimum requirement of power regulation and transmission demand during normal operational conditions. However, the FB-SM topology, with its capability to provide reverse polarity voltage, expands the operating region, as illustrated in Figure 2.5.

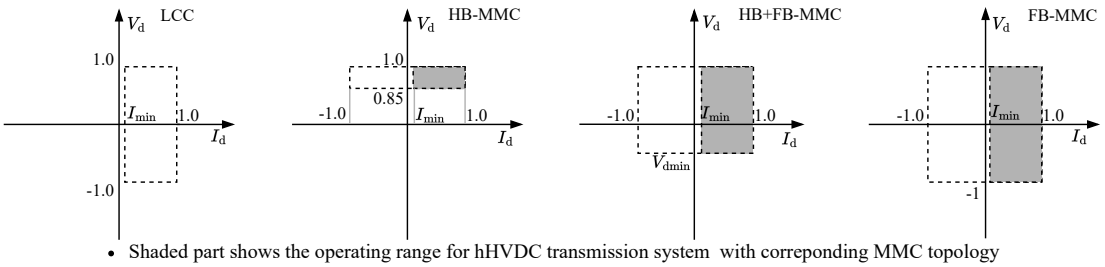


Figure 2.5: V-I operating range for different converter configurations. [8]

MMC FB topology, the complete operating voltage range of the LCC can be utilised. However, the minimum DC current requirement is determined by the LCC side. Multiple research studies have examined the benefits of using FB-SM topology in hHVDC systems.

Table 2.3 below provides an overview of specific performance aspects at the system level.

Characteristic	**HB-SM**	**FB-SM**
Power Flow Reversal [26]	Requires a reversal switch at the DC side; the system needs to stop during transition	Polarity reversal achieved within MMC; enables continuous operation
DC Fault Ride Through (FRT) [26] [8]	Requires AC circuit breaker tripping	Inherently blocks DC faults via reverse voltage
Overvoltage Management [27] [28]	Diode-based ride-through possible in some cases; high insulation needed for diodes and arresters	Higher switch cost, but saving in insulation coordination
Control Capability [8]	Limited control flexibility	Enhanced control functionalities
AC Fault Ride Through [29]	Limited reactive power support; risk of overvoltage during faults	Provides reactive power support; actively reduces DC voltage, offers improved security and stability

Table 2.3: System-Level performance comparison of HB-SM and FB-SM topologies in hHVDC systems.

2.3 DC Fault in HVDC Systems

This section discusses the performance of DC faults in HVDC systems, divided into two parts. Section 2.3.1 examines the short-circuit characteristics, considering various factors affecting this behaviour in relation to the HVDC system and the connected AC grid. Section 2.3.2 introduces general concepts on HVDC system protection from the perspective of converter topologies. The process is highlighted with the difference in fault response of HB and FB MMC topologies.

2.3.1 DC Fault Phenomena

The DC faults, considering the short-circuit faults, can be broadly categorised as pole-to-ground faults and pole-to-pole faults. The DC fault can be analysed as a short circuit of the DC voltage source in an RL circuit. This includes both transient and steady-state components, assuming no protective measures are taken throughout the entire event [30]. The characteristics that make DC fault current difficult to interrupt are well explained in [5]. When the short-circuit behaviour is analysed for HB-MMC, which has inferior short-circuit performance, the short-circuit current can be described in three stages of operation [31] [30] [32]. Upon the occurrence of a fault, the short-circuit current propagates through the transmission medium as a travelling wave. After a very short span of time, the fault current discharges through the transmission medium, specifically through the cable. This

stage, known as capacitive discharging, contributes to the peak value of the short-circuit current. For the MMC, the discharge of capacitance distributed in SMs is limited by the arm inductor. This stage discharges with time. However, IGBT protection measures block it from the circuit when the current reaches a standard threshold of 2 pu for current and 0.8 pu for DC voltage, and the *freewheeling diode* (FWD) starts to conduct. At steady state, the fault on the DC side results in a three-phase short circuit on the AC side. This fault current depends on *short circuit ratio* (SCR) and transformer impedance, and is expressed in per unit pu relative to the nominal DC as follows [5] [32],

$$I_{\text{fpu}} = \frac{4SCR}{\pi(1 + SCR \quad X_{\text{tpu}})} \tag{2.11}$$

$$SCR = \frac{V_{\text{s-LL}}^2}{Z_{\text{s}} P_{\text{d}}} \tag{2.12}$$

Where X_{tpu} is the pu transformer impedance, X_{s} is the AC system impedance, $V_{\text{s-LL}}$ is the AC source line to line voltage and P_{d} is the DC power.

In addition to SCR and transformer impedance, several other factors influence short-circuit current characteristics. These include the HVDC circuit topology (whether it is a monopolar or bipolar structure), earthing principle and grounding impedance, current-limiting reactors in the circuit, and the location of the fault, which are briefed in the Section 3.1 where the modelling of HVDC transmission system is explained. Another important factor that affects short-circuit behaviour is the converter topology. In both LCC and FB-MMC, faults are cleared through converter actions within a short period and are not reliant on the action of the AC CB.

For LCC rectifier operation, the controller determines the firing angle by comparing the reference value with the measured DC current. When a DC fault occurs, the DC line voltage drops, leading to a significant increase in the DC line current. As a result, the LCC operates in inverter mode in response to the control system's commands. The LCC rectifier station rapidly transitions the firing angle from rectifier mode to inverter mode [25], typically within a range of 145 to 165 degrees. The DC fault performance of FB-MMC, along with general DC system protection strategies, is explained in the following section.

2.3.2 Analysing HVDC Systems Protection Through Converter Topology

The primary goal of HVDC system protection is to quickly clear faults and ensure the rapid recovery of the system. This is imperative in multiterminal systems, as they transmit large amounts of power over long distances; power loss can significantly impact system reliability, including the connected AC grid. Chapter 1 stated three protection strategies based on selectivity. The fully selective strategy treats each node or busbar in the HVDC grid as a separate protection zone, with HVDC circuit breakers installed at both ends of each line or connection. However, this approach is not always the preferred option for all HVDC transmission systems in terms of TRL and *capital expenditures* (CAPEX) [14]. FB-MMC as fault-blocking converters are an option for clearing the fault current and restoring

the operation of healthy parts in a faster time frame. Figure 2.6 outlines the DC fault performance of converters in three different options over the timeline from fault inception to system recovery.

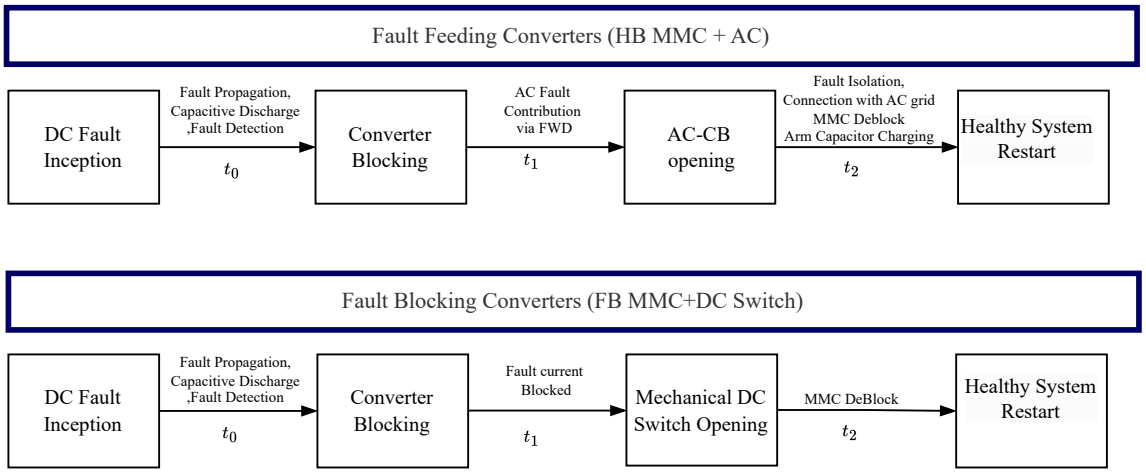


Figure 2.6: DC fault time frame for different MMC configurations.

The time from fault inception to converter blocking by its internal protection system is denoted as t_0. The time frame for fault detection and blocking in the HB-MMC converter ranges from 1.1 ms to several milliseconds, depending on various factors, including converter overcurrent capability, inductance connected to the converter and system configuration [33]. For FB-MMC, the fault can be detected within 0.5 ms [14] and the internal protection decides the t_0. As a general assumption, this time period can be considered to be in a similar range for both converters. The subsequent period, denoted as t_1, is from converter blocking to disconnection of the faulted line, in case of permanent fault or stopping the fault current feeding from the AC circuit to the fault point. This interval is significantly reduced in FB-MMCs because, with its configuration, a reverse voltage through the submodule capacitors is applied at the system level via the antiparallel diodes. So, the fault feeding is stopped. Consequently, the faulted element can be disconnected using a DC mechanical switch for 10–100 ms. However, for HB-MMCs, the AC CB needs to act to interrupt the fault current conducted by the freewheeling diodes, which typically involves an extra 60–80 ms, depending on the AC system's protection strategy. This indicates the fault current is cleared at t_0 for FB-MMC, whereas it is cleared at $t_0 + t_1$ for HB-MMC at the system level, even though the semiconductor switches are protected by blocking.

The DCCB is the choice for faster fault clearing for HB-MMC. The operation with DCCB allows the converter to remain operational without initiating blocking. However, this requires the total fault detection time and DCCB opening time to be less than the converter blocking time. However, this approach introduces high cost, requires a high-speed, selective protection scheme, and depends on reliable communication systems [14]. The third period, which pertains to system recovery after fault clearance, denoted as t_2, can be further minimised if the FB-MMC is designed to ride through the DC fault without blocking and maintaining the controllability. Instead of stopping the converter

switches after fault detection, the change in control action facilitates inserting a negative voltage in the circuit to reduce the fault current to zero. At the same time, a suitable control change is needed to maintain the necessary internal variable of MMC because the AC-DC power balance is lost. This implementation of active fault clearing by FB-MMC is further detailed in Section 3.4.2 as part of modelling the FB-MMC with fault-clearing capability.

2.4 Summary

This chapter begins with a classification of basic HVDC transmission systems and as it develops into multiterminal configurations. The working principles of converters and their fundamental operating concepts and the relevant mathematical equations are presented. A detailed explanation of the hybrid HVDC system architecture is provided, focusing on operational challenges and potential solutions. Finally, the characteristics of DC fault currents are discussed, followed by an analysis of HVDC systems protection strategies using converter topologies, based on findings from recent research publications. This chapter establishes the theoretical foundation for the modelling and simulations presented in the following chapters.

Chapter 3

Modelling

The analysis of DC fault performance in an HVDC transmission system entails converters at the component level and the connected AC and DC systems. This chapter aims to present the modelling of converters and other grid components. As the transmission system is hHVDC, the scope of converter modelling includes the LCC, MMC-HB and FB configurations with blocking capability. The DC transmission system model considers the connection topology between converters and the transmission medium. The study of DC side faults is influenced by the characteristics of the AC system at the *point of common coupling* (PCC) [30]. The AC system modelling will outline the characteristics of the AC system and the connected converter transformers.

The converter modelling is implemented in the EMT software PSCAD, LCC modelling relies on available PSCAD open-source examples, and the MMC model is developed using methodologies derived from research publications. The complete system configuration references PSCAD engineering examples, research publications, and implemented HVDC projects. Initially, Section 3.1 explains the modelling of the DC side transmission system. Following that, Section 3.2 , Section 3.3 and Section 3.4 will detail the modelling of converters LCC, MMC HB and MMC FB, respectively, along with parameters of the connected AC system.

3.1 DC Transmission System

The two general classifications for the DC substation configuration are monopolar and bipolar. The focus of configuration here is monopolar, and the further details of bipolar configuration are not explained. For monopolar configuration, there can be symmetrical and asymmetrical configurations as shown in Figure 3.1. The symmetrical configuration employs two conductors, each with half of the DC voltage rating. For an asymmetrical configuration, a pole conductor has the DC full voltage rating; another conductor is an earth or metallic return. The metallic return is preferred over an earth conductor for environmental reasons and corrosion considerations, and selected for modelling in this thesis [34].

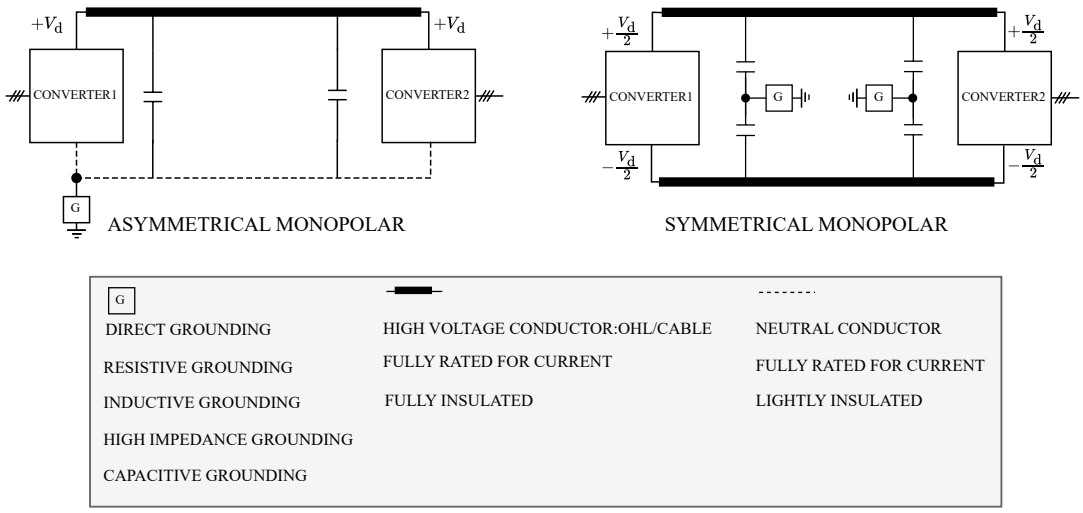


Figure 3.1: Schematic of HVDC substation configurations. [30]

At the converter level, the LCC system consists of two 6-pulse bridges and can be featured as an asymmetric monopolar system with one high-voltage DC conductor and an earth or metallic return. The VSC can be configured as either an asymmetrical or symmetrical monopolar connection. When connecting the two converters—LCC and MMC— for the hybrid system, the asymmetrical monopolar configuration with a metallic return results as the DC side configuration. The return conductor is grounded at a single point.

In selecting the DC voltage level, the insulation requirements of the high-voltage conductor and associated grid components are accounted for [35]. Based on the literature review on the product specification and the HVDC project implementation, a DC voltage level of 500 KV is decided for the high voltage point of the monopolar configuration [36] [37] [38]. The parameters of the DC transmission system are depicted in Table 3.1. The DC cable and OHL are modelled as a π section, and parameters are based on the reference [39].

Parameters	**Symbol**	**Values**
Converter Rating	S_{d}	1000 MVA
DC Voltage	$V_{\mathrm{d,rated}}$	500 KV
DC current	$I_{\mathrm{d,rated}}$	2 KA
Cable , OHL Resistance	R_{tl}	0.011 Ω/km
Cable Capacitance	C_{tl}	0.191 µF/km
OHL Capacitance	C_{tlo}	0.012 µF/km
Cable Inductance	L_{tl}	2.615 mH/km
OHL Inductance	L_{tlo}	0.936 mH/km

Table 3.1: Parameters of DC transmission system.

The asymmetrical monopolar arrangement depicted in Figure 3.1 can be configured as the hHVDC system. This system includes the LCC at the rectifier side and the MMC at the inverter side, as shown in Figure 3.2. The metallic return conductor resistance is

selected as $0.05\,\Omega/\text{km}$ [34]. Regarding the smoothing reactors for the converter, the LCC side is connected with the smoothing reactor as per the CIGRE model[40]. For MMC, the system is configured without a smoothing reactor; however, a terminal reactance denoted as $L_{\text{dt,l}}$ of DC side connection 25 mH is included. [33]. The system is assumed to be solidly grounded, representing the most critical case in terms of fault current magnitude. This point-to-point hHVDC transmission system is the foundation for the modelling and simulation work in the following sections. The MMC exhibit different operational performances depending on whether configured in HB or FB submodules, as discussed in Section 2.2. Therefore, the modelling section includes both configurations, specifically focusing on their performance during DC fault conditions. All associated variables of LCC are denoted with the subscript r for the rectifier operation mode, whereas variables related to the MMC are presented with no subscripts to indicate the operation mode. Additional MMC converters are introduced when the system is extended to an MTDC system. In these cases, the parameters of each MMC are indexed by converter number to differentiate between multiple units as necessary.

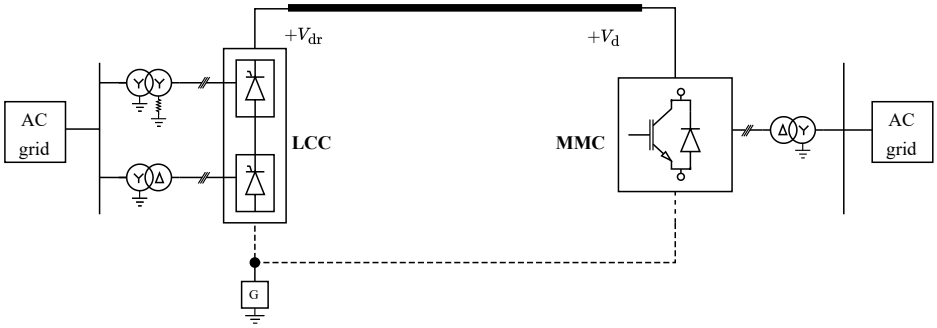


Figure 3.2: Schematic of hHVDC point-to-point system.

3.2 LCC Modelling

The fundamental working principle of the LCC is introduced in Section 2.1.1. The basis for the LCC model is the CIGRE Benchmark model in PSCAD [41] [40]. The primary purpose of the LCC model here is to function as a rectifier in the hHVDC system during normal conditions, while having the capability to withstand DC faults. Therefore, the primary control of the model is set to operate in rectifier mode. The fault-tolerant behaviour of the LCC is due to its inherent high current capability and its ability to operate with phase reversal during DC fault conditions. As such, a control mode selection is implemented to switch to inverter mode during the fault conditions as required.

At the device level, the fundamental component of the LCC system is an integrated converter model, which is available in PSCAD. This model consists of a 6-pulse Graetz converter bridge that can operate as a rectifier or an inverter, an internal *phase-locked oscillator* (PLO), firing and valve-blocking controls, and measurements of firing angle and extinction angle. The internal PLO activates an interpolation algorithm to interpolate all turn-on and turn-off events.[42] In a 12-pulse bridge configuration, two 6-pulse bridges are connected to the AC grid via two transformers that have a phase shift of 30 degrees.

The schematic of the LCC as it connects to the AC power grid, represented by Thevenin's equivalent circuit, is illustrated in Figure 3.3

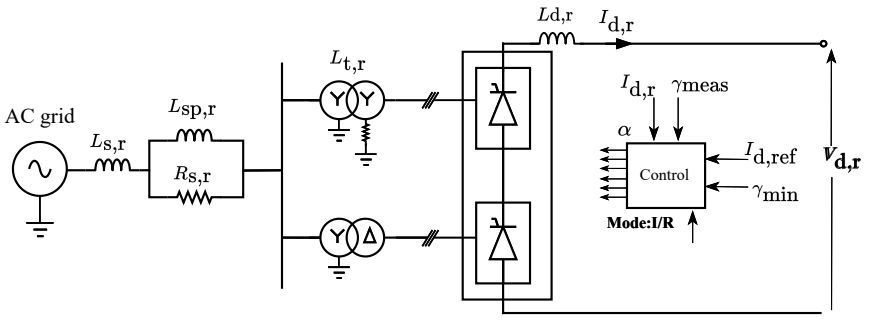


Figure 3.3: Schematic of hHVDC transmission system with LCC at rectifier side.

Certain modifications have been incorporated from the CIGRE Benchmark model to enhance operational performance. The Y/Y transformer is connected to the high-voltage side of the grid for better insulation coordination. The AC system voltage rating has been changed from 345 KV to 220 KV, taking into account the rectifier side generation voltage. The system impedance the R-R/L network has been correspondingly adjusted to reflect this change through the per-unit conversion. Furthermore, the AC system's equivalent impedance has been adjusted to improve the SCR, aiming for a value >5 for a strong system while maintaining the X/R ratio. The values of filters and capacitance for reactive compensation are intact as in the CIGRE model.

This AC system is now to be connected to the DC system through the transformers. Considering the firing angle and commutation overlap, the transformer's voltage rating is decided to provide the necessary AC voltage to meet the DC rated voltage of 250 KV of a 6 pulse rectifier. Table 3.2 presents the system parameters finalised after all modifications. A comprehensive presentation of these changes, as calculations performed in MATLAB, is provided in Appendix B for further review.

Parameters	**Symbol**	**Values**
Apparent Base Power	S_{base}	1000 MVA
AC System Voltage,RMS L-L	$V_{s,r}$	220 KV
AC System Series Resistance	$R_{s,r}$	0.456 Ω
AC System Parallel Resistance	$R_{sp,r}$	878.59 Ω
AC System Parallel Inductance	$L_{sp,r}$	0.018 H
AC System Impedance	Z_s	5.808 Ω
Short Circuit Ratio	SCR	8.334
Effective Short Circuit Ratio	ESCR	8.209
Transformer Leakage Reactance	$X_{t,r}$	0.125 pu
Minimum Extinction Angle	γ_{min}	15°
DC Reactance	$L_{d,r}$	0.5968 H

Table 3.2: Parameters of LCC (rectifier side) for hHVDC transmission system.

The AC side system and the transformer parameters for connecting LCC to the DC side are now established. The following section delves into the control of LCC.

3.2.1 LCC Converter Control

The control of LCC in this model consists of two parts. The primary control for the rectifier is in normal operating conditions, and the secondary control is for inverter operation, which is activated by a change in control mode during abnormal conditions. In both the control modes, the intended output is the firing angle order denoted as α_{order}; however, the PI controller input varies. Figure 3.4 illustrates the control of the LCC in different modes. The measured values of DC current $I_{\text{d,r}}$ and the extinction angle γ are compared with the reference values to generate α_{order}.

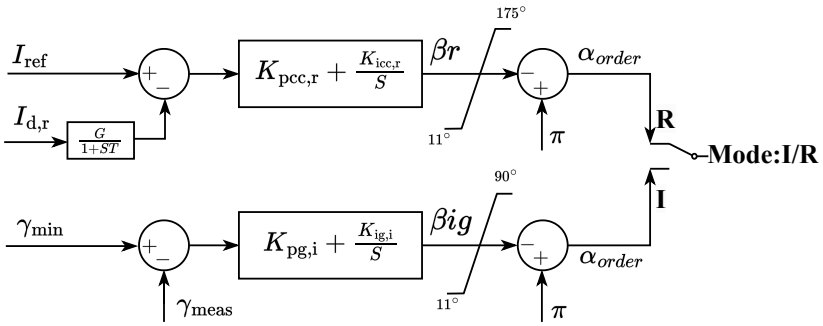


Figure 3.4: Block diagram for LCC control operation in hHVDC system.

Firstly, review the rectifier mode with constant current control,α_{order} is derived from the current measured at the DC rectifier side, compared to the required current order. The current order can be calculated from the required power transfer or set directly through a specified current rating. In this model, the current order is directly provided by a control panel setting, on pu basis of rated DC current denoted as $I_{\text{d, rated}}$ in Table 3.2. In Figure 3.4 I_{ref} denotes the current order, and $I_{\text{d, r}}$ is the measured current on the DC rectifier side. The PI controller, with a proportional gain of $K_{\text{pcc,r}}$ and an integral gain of $K_{\text{icc,r}}$, generates β_r, which is the extinction advance angle for the rectifier. Then the required α_{order}, to align the measured current with the required current order, is calculated as $180 - \beta_{\text{r}}$.

Next, during the DC fault condition, the LCC fault rides through with a rapid phase shift reversal, which is facilitated by the inverter mode of operation. The fault activation triggers the change in the control mode. During the inverter mode of operation, the primary concern is to process the firing of thyristor valves by keeping the minimum ignition advance angle γ_{min} in order to avoid commutation failure. So that input to the current controller is the reference as γ_{min}. The PI controller, with a proportional gain of $K_{\text{pg,i}}$ and an integral gain of $K_{\text{ig,i}}$, generates β_{ig}, which is the extinction advance angle for the inverter mode operation and the firing angle order is calculated as $180 - \beta_{ig}$.

3.3 HB-MMC Modelling

The basic working principle and arm averaging of HB-MMC are described in Section 2.1.2. This section provides a detailed modelling of HB-MMC with *arm average model* (AAM) and the implementation. The section is organised as follows: First, the MMC converter is described as connected to the AC grid. The parameters and components on the AC side are defined in alignment with the converter's rating. Following this, the modelling of the converter is detailed, covering arm averaging, the controller for reference voltages of the insertion indices required for the appropriate arm voltage, as well as the operation of the converter with the blocking circuit.

The MMC converter with the ratings provided in Table 3.1 is connected to the AC system represented by Thevenin's equivalent circuit. The AC grid connection arrangement is similar to that shown for LCC. The AC system voltage is 400 KV, where the higher AC grid voltage is selected. The system impedance parameters have been adjusted from the [43] to account for this voltage and SCR for a strong AC system. Consequently, the transformer voltage rating has been chosen to connect the 400 KV RMS L-L AC voltage with a 500 KV DC link. The calculations performed in MATLAB for these modifications are provided in Appendix C for further review. The final parameters of the AC system are summarised in Table 3.3.

Parameters	Symbol	Values
AC System Voltage,RMS L-L	V_s	400 KV
AC System Series Resistance	R_s	0.852 Ω
AC System Parallel Resistance	R_{sp}	2766.24 Ω
AC System Parallel Inductance	L_{sp}	0.045 H
AC System Impedance	Z_s	14.022 Ω
Short Circuit Ratio	SCR	11.411
Transformer Leakage Reactance	X_t	0.125 pu

Table 3.3: Parameters of MMC (inverter side) for hHVDC transmission system.

3.3.1 AAM and Converter Control

The MMC has a modular structure and high controllability; however, this results in significantly more complex control and internal dynamic behaviour than LCC. The literature review suggests varying levels of detail in modelling MMCs for *electromagnetic transients* (EMT) simulations. The primary objective of the model in this thesis is to assess its performance during DC faults; therefore, the AAM of MMC will be designed with a blocking circuit. This model has been chosen due to its lower computational demands while accurately depicting the DC fault behaviour [18] [5].

The three-phase MMC modelled in PSCAD resembles the three-phase MMC shown in Figure 2.3, with each arm assigned as a subpage in PSCAD. The two key parts of the model are the details of arm average modelling with the blocking circuit, and the control section,

which determines references for the insertion indices for the arm voltage to be generated. Figure 3.5 shows the different parts in this modelling, from measuring grid parameters to generating arm voltage. This controllable arm voltage inserted on the MMC enables the generation of the required output voltage according to the power or DC voltage setpoints. This is an approximation disregarding the switched mode operation of the MMC, which is not necessary to analyse the MMC dynamics as grid-connected [18].

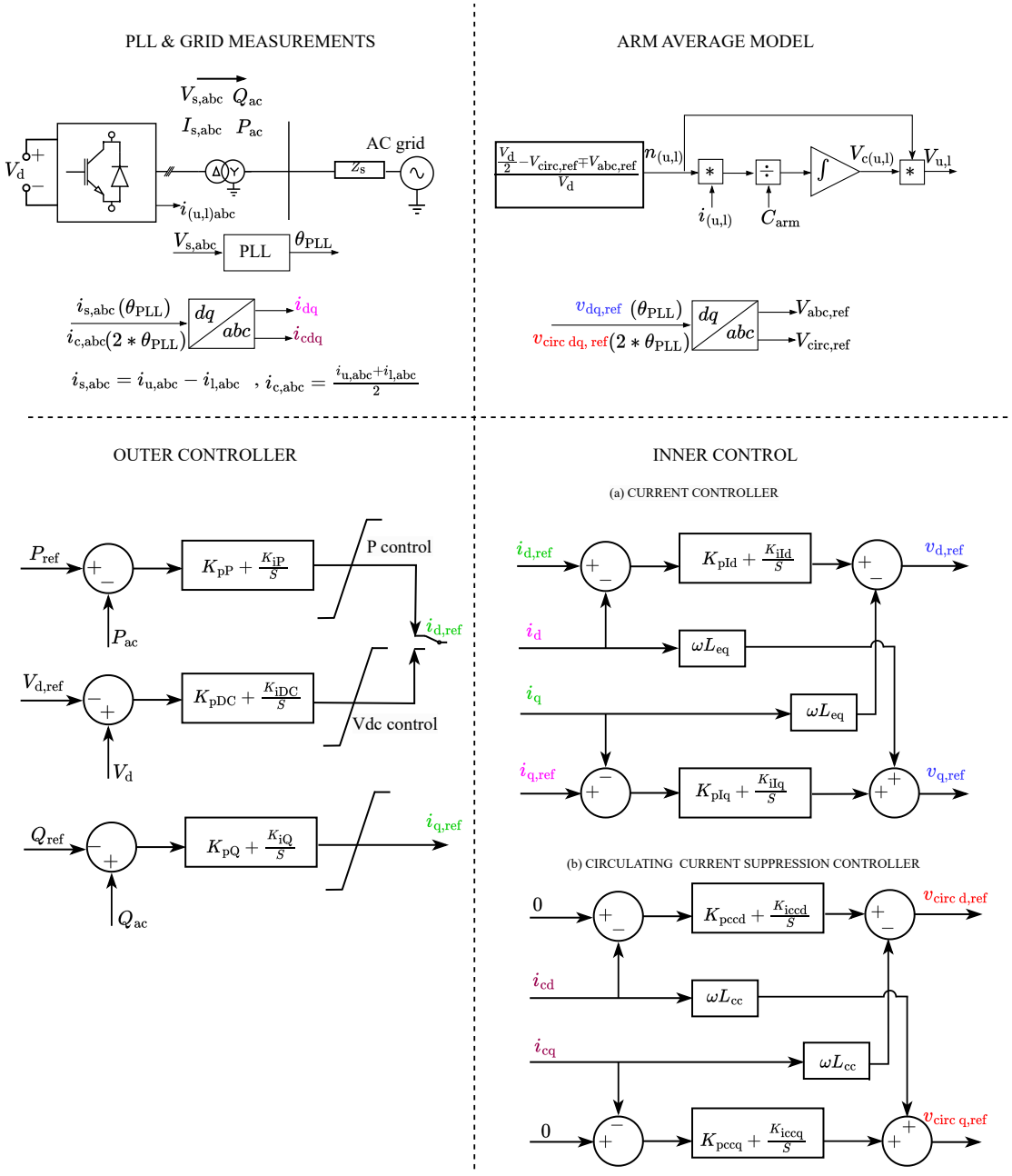


Figure 3.5: The AAM and controller modelling of MMC as connected to AC grid and a DC link.

Starting the modelling from the internal dynamics of the MMC, the arm average modelling is explained first. Each capacitor has a zero or one switching status at the submodule level design, indicating whether its voltage is actively inserted. The AAM simplifies this

using a continuous average summation voltage index, assuming all capacitor voltages are controlled to the same mean value. This index, called the insertion indices, represents the ratio of reference voltages to the ideal arm voltage, the rated DC link voltage. The subpart arm average model in Figure 3.5 illustrates how this is implemented in the model, where the voltage $V_{\mathrm{u,l}}$ is the multiplication of insertion indices and capacitor voltage $V_{\mathrm{c(u,l)}}$ in each arm as explained. The capacitor voltage is decided by integrating the multiplication of arm current $i_{\mathrm{u,l}}$ and the capacitors inserted, which is decided by the insertion indices $n_{\mathrm{u,l}}$. Each arm is connected with an arm inductance of 50 mH and arm resistance 1.07 Ω of values. The arm capacitance of 25 µF is selected [5].

Now, the next phase is how the insertion indices are decided. The relationship between the arm voltage and the AC side voltage and the DC voltage is provided in Equation (2.3) and Equation (2.4) for upper and lower arms, respectively, considering the AAM where each arm voltage is formed by AC and DC voltages. Hence, insertion indices have the AC and DC voltage references. Considering the direct voltage control as the modulation technique, the insertion indices are calculated as the ratio of this reference voltage to the desired mean value of total capacitor voltage that is the DC link voltage V_{d} [18]. The AC voltage reference is taken from the inner current controller, and the circulating current suppression control suppresses the second harmonics in the DC voltage.

The most commonly used vector current control of VSC is implemented for the inner current control. The system quantities are transformed into a rotating reference frame that aligns with the voltage at the point of common coupling. This transformation allows for the independent control of the d and q components in a synchronous reference frame, which is provided by the PLL at the PCC [30]. The *phase locked loop* (PLL) and the measured quantities, including their directions, are shown in the subpart, labelled as PLL and Grid Measurements in the Figure 3.5. The sign conventions of the controller are selected accordingly. The PLL block available in PSCAD is utilised in the model. Since the transformer is configured in a Y/Δ connection, corrections must be accounted for a 30° phase shift, or the voltage reference point must be set to the secondary side of the transformer for PLL. The outer controllers provide the input for the internal current control, and [44] is referred to for this implementation. The active power controller, or DC voltage controller, provides the d component reference denoted as $i_{\mathrm{d,ref}}$ for the inner current controller, while the reactive power controller provides $i_{\mathrm{q,\,ref}}$. In the current controller, the current reference generated by the outer controller is compared with the dq components of the output ac current, as shown in Figure 3.5 in the subpart, labelled as internal control. The PI controller regulates the error in the measured quantities to align with the reference setpoints, generating the reference AC voltage.

A circulating current of twice the fundamental frequency and negative sequence is coupled with the DC current that flows through the upper and lower arms. So the DC current through each arm has two components, the ideal part $\frac{i_{\mathrm{d}}}{3}$ and the circulating current i_{c}. So the circulating current suppression controller is implemented as detailed in [45]. This is shown in the subpart labelled internal control in Figure 3.5. Hence, for the DC part, the reference voltages used for formulating the insertion indices are V_d, the rated DC voltage and $V_{\mathrm{csc,dq}}$, the output of the circulating current suppressing controller.

The HB-MMC modelling for normal operating conditions that works with AAM and the arm voltage determined by the insertion indices, to generate the required output voltage, has been detailed so far. The second part of the model addresses DC fault performance, during which the semiconductor switches are blocked to protect them from fault currents, as explained in the following section.

3.3.2 HB Blocking Circuit

The switching states outlined in Table 2.1 can be referenced for describing the blocking operation of the HB-MMC. When modelling the HB-MMC as AAM with blocking capability, the N submodules can be substituted with an arm voltage source with either a switch T or $D1$ in the pathway and a bypass diode $D2$ antiparallel to this. This is illustrated in Figure 3.6.

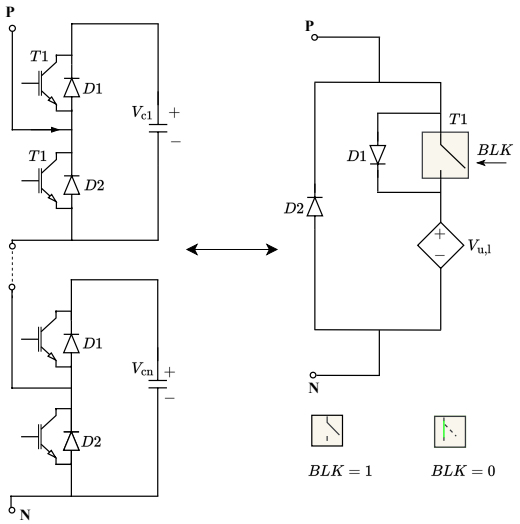


Figure 3.6: Representing the transition from SM to AAM with blocking capability for HB-MMC .

During normal operation, the BLK signal is not activated, and the switch remains in the closed position. This state allows current to circulate through the submodule capacitors in both directions, inserting the arm voltage in the circuit. However, the BLK signal opens the switch in fault conditions, replicating the blocking of semiconductor switches and thus not inserting the arm voltage into the circuit. Consequently, current flow is directed solely through the diodes, determined by the direction of the current [5]. The Figure 3.7 illustrates the flow of current through the diodes $D1$ and $D2$ for different directions.

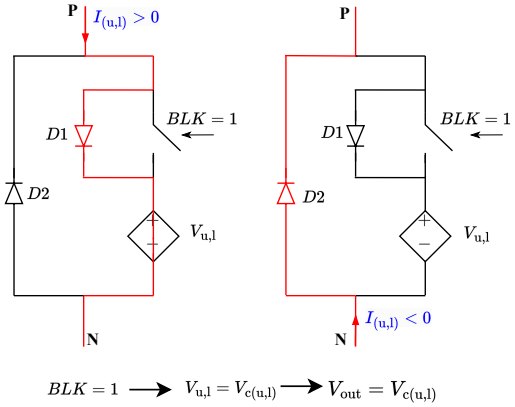


Figure 3.7: Conduction in the HB-MMC arm in blocked state for different current directions.

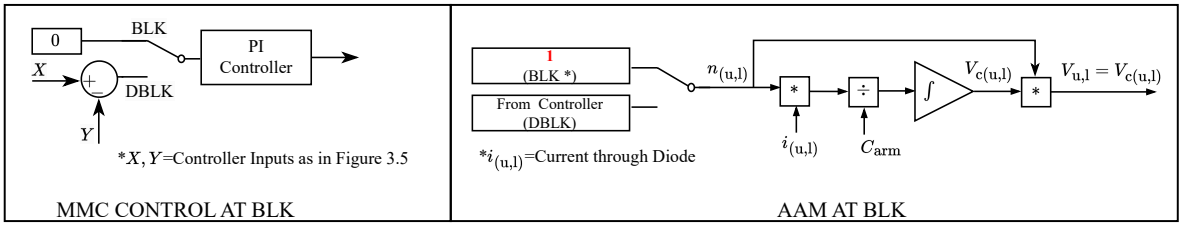


Figure 3.8: HB-MMC AAM and control scheme changes in blocked state.

One important aspect to note in modelling is that after blocking, conduction occurs due to the freewheeling action of diodes. Therefore, changes need to be incorporated into the model regarding the transition of the insertion indices and the application of insertion indices in AAM during blocking mode. As shown in the Figure 3.8, when the *BLK* signal is activated, all controls for the normal operation of the converter are deactivated to avoid further control saturation. Consequently, the insertion indices are set to one, keeping the total arm capacitor voltage as such. The current through diode *D*2 bypasses the arm capacitors and constitutes the flow of fault current. Now, as these six arms are connected in a three-phase circuit, the conduction follows the circuit of a six-pulse diode rectifier, and this results in the AC grid feeding the DC fault point, until the AC CB stops this.

3.4 FB-MMC Modelling

For FB-MMC modelling, the AC system parameters remain the same. Internally, however, the switching circuit differs in FB-MMC. This section presents the modelling approach from that perspective. Like HB-MMC, FB-MMC operates in two modes: normal operating mode and blocking mode. In normal operating mode, the FB cell employs two switches and diodes, as shown in Appendix A, allowing it to output positive voltage from the cells for both positive and negative current directions, as well as negative voltages for both current directions when measured from point P to point N. For normal operating conditions, a positive output voltage from a system perspective is considered here. In the blocking mode of operation, for HB-MMC, only the positive direction of current flows

through the capacitor cell and outputs a positive voltage referenced from P to N. The key functional attribute of FB MM is that current can flow in both directions through the capacitor cells via diodes during blocking mode. Consequently, the cells provide different output voltages when referenced from P to N, depending on the direction of current flow. This output voltage is such that, when added at the system level, it effectively creates an open circuit for the DC current. For this to happen, the capacitor sum voltage should be greater than the AC line-to-line voltage. This characteristic enables the FB-MMC to block DC fault current inherently.

3.4.1 FB Blocking Circuit

As shown in Figure 3.9, the above detailed characteristics are incorporated to model the FB-MMC, with Figure 3.10 showing the output voltages of the model in different current directions. The different sequences of operation of the FB model are summarised as follows,

- A positive voltage path configured by the switches $T1$ and $T4$ parallel to diodes $D1$ and $D4$ connected across the arm capacitors $V_{(u,l)}$, emulates the normal mode of operation. The signal BLK, which is zero in normal conditions, indicates the closed switch. During blocking mode, this path allows positive-directed current flow through the diodes.
- A second current path includes diodes $D2$ and $D3$, also connected across the arm capacitors, which allows negative-directed current flow during the blocking mode. In the PSCAD model, this path is disabled in normal operation using a switch in series with the diodes controlled by the $DBLK$ signal, which is the logical inverse of BLK in simulation.

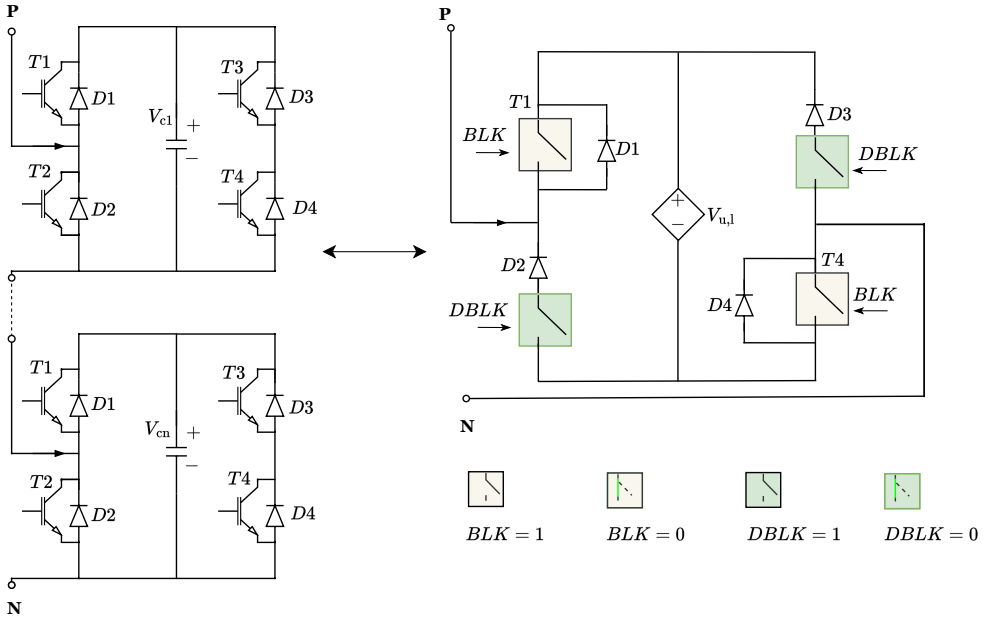


Figure 3.9: Representing the Transition from SM to AAM with blocking capability.

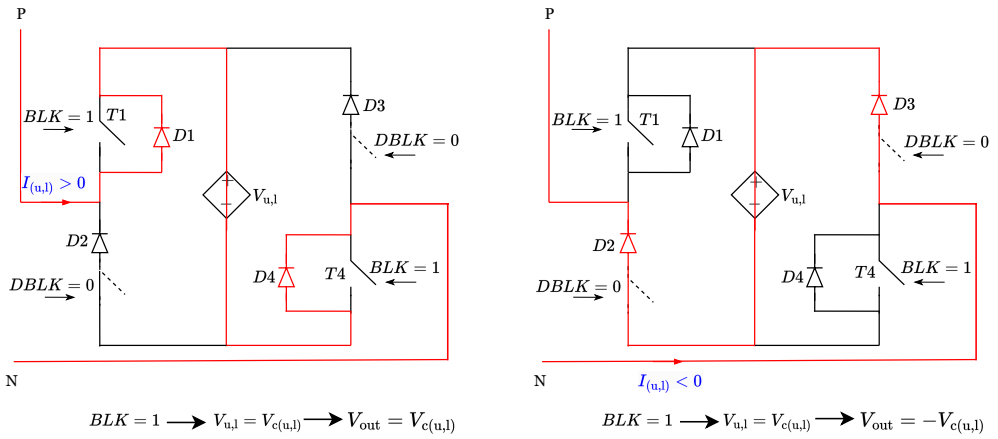


Figure 3.10: Conduction in the HVDC MMC arm in blocked state for different current directions.

Thus, according to the current directions, the fault current is blocked with two different output voltages in the blocking mode.

3.4.2 FB Active Control for DC Fault

Although the FBMMC provides an open circuit during DC faults by blocking the converter, this turns off controllability by blocking all semiconductor switches. With the controls deactivated, the insertion indices are fixed at one, as the current flow through the diode path determines the capacitor charging and voltage. Then, fault blocking is a result of the circuit configuration alone. If the DC fault current can be reduced while maintaining controllability, there are significant advantages: reverse DC polarity during faults can clear arcs quickly, allow for fault recovery without synchronisation and control checks, and minimise disturbances on the AC side and able to provide reactive power support, critical for weak AC grids [46].

The modelling can be implemented in two stages to ensure controllability during fault conditions for FB-MMC. The conduction path remains unchanged as such in normal operating conditions. Control modifications are triggered by the signal FLT in the simulation model, which transitions from 0 to 1 when the fault current reaches a predefined threshold.

- Stage 1: $-1 < K_{\text{SM}} < 1$ This implementation utilises the extended DC voltage insertion ratio of FB SM to insert a negative voltage during the fault condition. The primary principle here is to bring the DC current to zero by the insertion of a negative voltage generated by the controller.
- Stage 2: $i_{\text{d,ref}}$ is from arm sum voltage control, $i_{\text{q,ref}}$ from reactive power controller

  In the second stage, the control is further enhanced by an arm sum voltage controller, which can maintain the arm power balance. During normal operation conditions, the arm voltage is controlled with power balance between the AC and

DC sides. So the insertion indices for the AC voltage part are provided by the outer controllers, and the DC voltage part is calculated with the DC link voltage and CCSC controller. During a DC fault, the DC voltage collapses. This disrupts the power balance between the AC and DC grids, leading to power imbalances in the arms. So, the error in arm voltage is controlled by the AC side active current reference. As part of the outer controller, the active reactive controller can provide $i_{\text{q,ref}}$, which supports the AC grid with reactive power injection during the DC fault.

Figure 3.11 shows the changes implemented additionally in the control system of MMC for enabling active fault clearing with FB-MMC

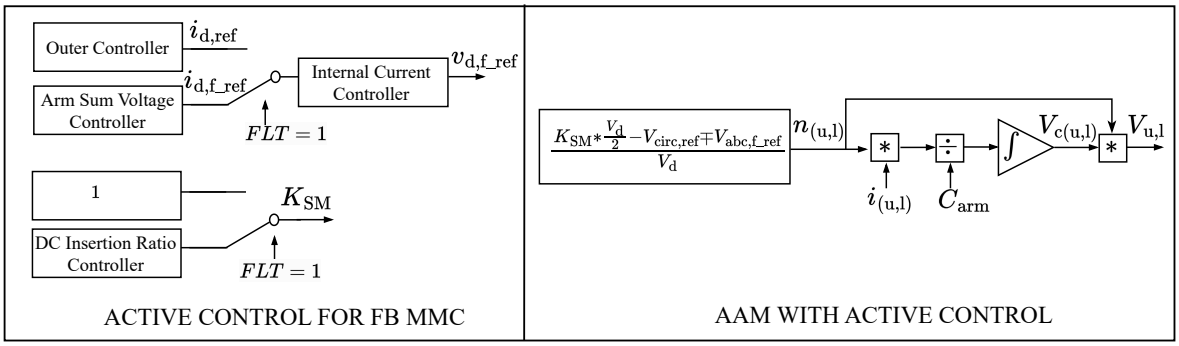


Figure 3.11: FB-MMC AAM and control Scheme changes For active fault clearing.

The DC voltage reference for deciding the insertion indices of DC voltage references during the fault is determined by comparing the DC current to the zero reference and accordingly issuing the appropriate DC insertion ratio, denoted as K_{SM}. Figure 3.12 shows the controller circuit for the DC insertion ratio controller. This indicates that, in the insertion ratio calculation for the DC part, without the CCSC references, limited to 0.5 for HB-MMC, is changed by FBFB-MMCs' extended range. For FB-MMC, this part of the insertion ratio is determined by the DC insertion ratio controller during the fault conditions. In this thesis, the extended range is applied only during fault conditions.

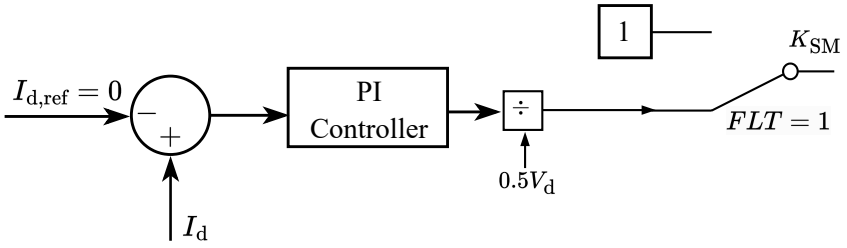


Figure 3.12: DC voltage insertion ratio controller.

As stated before, the arm sum voltage controller determines the d component of the AC voltage reference during a fault, which is determined by the DC voltage controller or the active power controller at an outer level under normal conditions. Figure 3.13 shows the controller circuit.

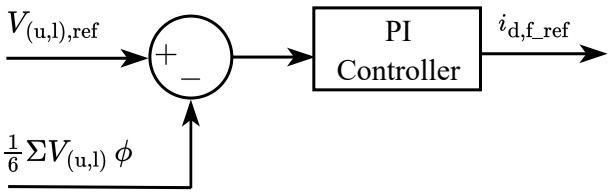


Figure 3.13: Arm sum voltage controller.

The upper and lower arm voltages are 180 degrees out of phase, and their sum approximates a DC voltage V_d as balanced. Thus, the arm voltage reference is kept 5% above V_d to ensure a safe voltage margin.

3.5 Summary

This chapter establishes the DC transmission system configuration, including detailed converter modelling, for DC fault analysis. The developed hHVDC system incorporates essential parameters to evaluate worst-case DC fault scenarios. The LCC converter model changes from the CIGRE benchmark model, and the control scheme for normal and fault conditions is explained. The MMC modelling includes the AAM and a comprehensive control scheme for normal operation. This serves as the foundation for both FB and HB configurations. Emphasis is placed on the arm switching circuit, which features blocking capability, differentiating the two SM configurations. The changes during the blocking mode in AAM for both HB and FB models are presented. By leveraging the extended DC voltage insertion capability of the FB-MMC, an active fault-clearing strategy is implemented, consisting of a DC insertion ratio controller and an arm sum voltage controller. This facilitates the simulation study in the coming chapters for HB-MMC blocking, FB-MMC blocking and FB-MMC active fault clearing.

Chapter 4

Simulation:Point to Point hHVDC Systems

This chapter covers simulations of a point-to-point hHVDC system with two different MMC configurations connected to the LCC. It first analyses the performance with the HB-MMC during normal operation and DC faults. Then, it examines the system with FB-MMC and verifies its inherent DC fault blocking capabilities and then DC fault performance with active fault clearing. The simulation follows the model, methods, parameters and values provided in Chapter 3 for converter and system configuration. Section 4.1 explains the simulation of the HB-MMC configuration, and Section 4.2 explains the simulation of the FB-MMC configuration. Results are presented and discussed in the corresponding sections. Figure 4.1 shows the general schematic of the system configuration employed in the simulation studies, with corresponding references provided for the parameter values.

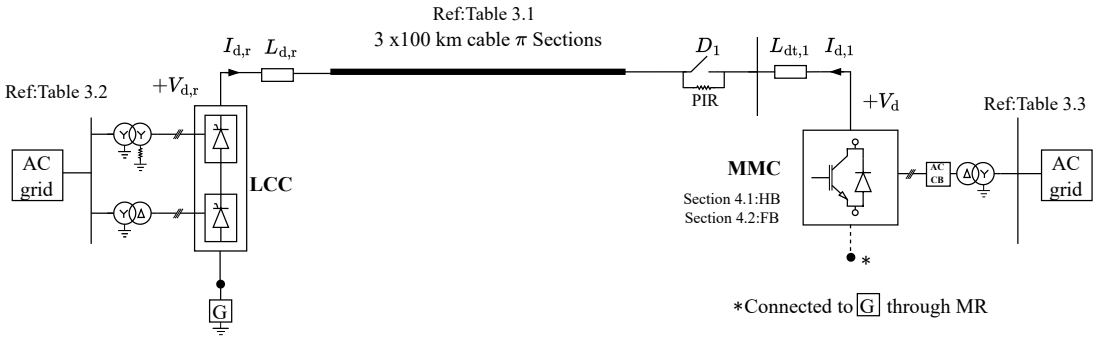


Figure 4.1: Schematic of hHVDC point-to-point system for simulation studies.

4.1 hHVDC Point to Point System with HB MMC

This section details the simulation of a point-to-point hHVDC system where the HB configuration of the MMC converter is employed. The system under study is an asymmetric monopole configuration, described previously in Section 3.1, with the neutral point grounded at the LCC side. The simulation scenarios for the hHVDC system consist of firstly making the converter internal dynamics and control ready to connect to the system, secondly, steady state operation, and finally, the DC fault event, with the corresponding converter and system responses. The threshold for the protection circuit to act is 2 pu. The protection circuit is implemented as a comparison of the DC current with this threshold value. No further delay is implemented for the protection logic to act, indicating the time the DC current reaches the threshold value, the converter protection acts and a uniform comparison across all simulation cases. Thus, the sequence of operations is summarised in the Table 4.1. The transmission line considered is a cable

consisting of three π sections of each 100 km length. All quantities are measured and represented in the pu system for standardised comparison and analysis.

Description	Time [s]	Remarks
MMC Deblock	0.4	Initially charged from AC side
DC Voltage Ramp-up to Rated Value	1.5	Depends on initial capacitive charge
MMC DC Side Switch Closing	2.5	With PIR
LCC Deblocking	2.6	CC control
Active Power Reference Step	3 and 4	0.1 pu step
DC Side Fault Event	5	LCC Phase Reversal, MMC Blocking
AC CB Opening	5.12	DC System disconnected from AC grid

Table 4.1: Sequence of simulation events and timings for the HB-MMC point-to-point hHVDC system.

4.1.1 Deblocking and Steady State Operation

For setting up power transmission in the hHVDC system, the sequence begins with the MMC converter, which establishes the DC voltage reference in this simulation. The DC voltage control mode is selected. Initially, for up to 0.4 s, the MMC is precharged to 450 kV equal to 0.9 pu while connected to the AC grid, and being in the blocked state. This is implemented by setting an initial value for the arm capacitor voltages $V_{c(u,l)}$ in the model. The MMC is deblocked at this stage, continuing in DC voltage control mode to regulate the arm voltage to the rated DC voltage. Once the DC voltage reaches this rated value, a disconnector switch at the DC side, using a circuit breaker in the PSCAD simulation, is closed at 2.5 s, which connects the MMC to the DC transmission cable and the LCC. A *pre-insertion resistor* (PIR) is used to mitigate overvoltage transients during this connection. Subsequently, the LCC is deblocked at 2.6 s, and the rectifier-side DC voltage ramps up to the rated 500 kV, with the PIR remaining in place to complete the charging process. After achieving steady state with rated voltage, the system is verified for active power transmission. The active power references as current order is applied in LCC for 0.1 pu at 3 seconds and increased by another step of 0.1 pu at 4 s. Figure 4.2 and 4.3 illustrates the DC voltage and current profiles at both the LCC and MMC sides during the initial charging period and subsequent steady-state operation, spanning from 0.0 s to 4.5 s.

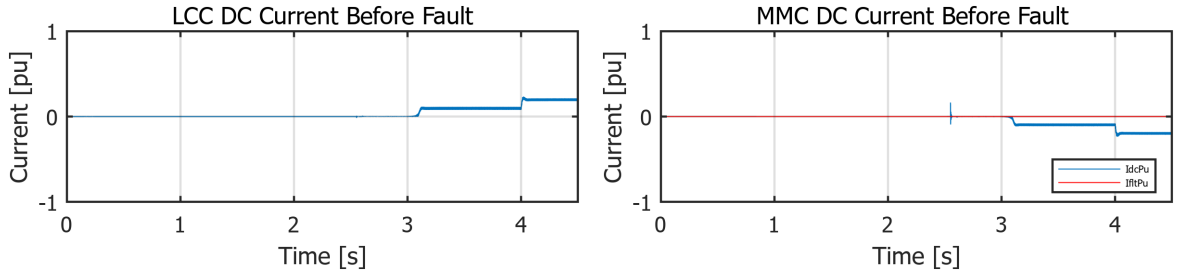


Figure 4.2: LCC and HB-MMC DC current during the charging and steady state operation.

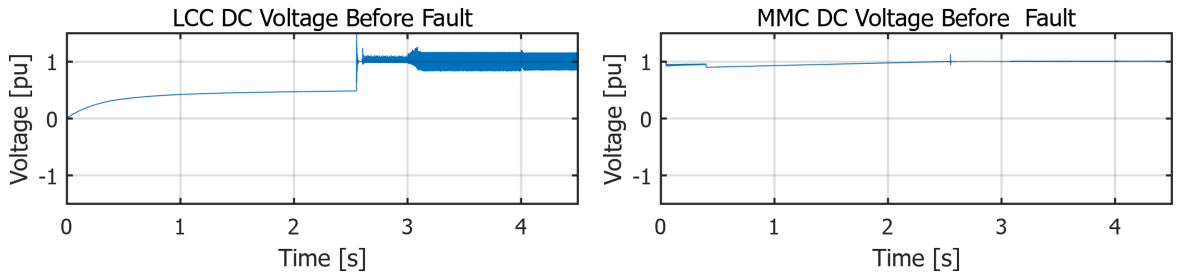


Figure 4.3: LCC and HB-MMC DC voltage during the charging and steady state operation.

Before the DC fault analysis, the characteristics of the arm capacitor voltages $V_{c(u,l)}$ and arm voltage $V_{(u,l)}$ can be observed as shown in Figure 4.4. The voltage builds up from the initial charged value to the rated DC voltage during the initial period. An inrush current occurs at 0.4 s during the deblocking of the MMC. This process continues until the DC voltage reaches the rated value within a few seconds. After this, the current as in Figure 4.5 decays until it stabilises, following the step power reference, which is applied first at 3.0 s from the rectifier side.

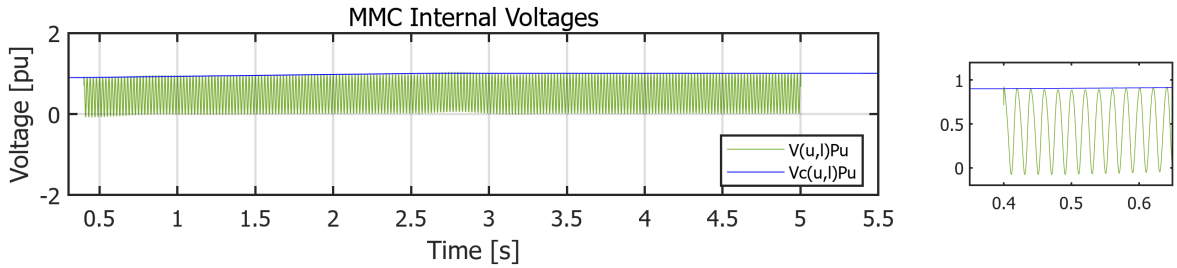


Figure 4.4: HB-MMC arm voltage and capacitor voltage during full sequence of simulation.

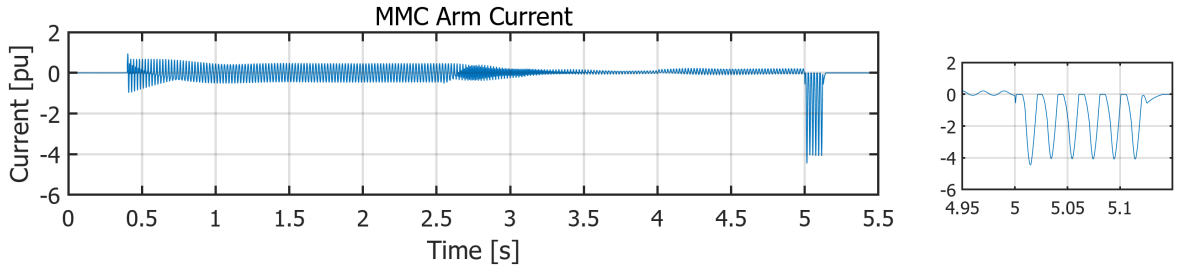


Figure 4.5: HB-MMC arm current during full sequence of simulation.

4.1.2 DC Fault Analysis

The DC fault sequence in the simulation begins at 5.0 s with the application of a solid pole-to-ground fault, as the system is an asymmetrical monopole. This is implemented using the timed fault logic in PSCAD. This section initially compares the DC current of the LCC and MMC sides during a fault. Then, for the MMC converter, the current up to blocking and during the freewheeling action of the diodes are analysed. This is done from the perspective of different factors that affect the current magnitude and rate of rise of the fault. The AC circuit breaker ACCB operation is fixed at 120 ms, considering a slightly

higher time period than AC protection system response times reported in the literature. The threshold value put for converter blocking is 2 pu [5].

The behaviour of the DC fault current and DC voltage for both the MMC and LCC during the fault period can be examined in Figure 4.6 and Figure 4.7 respectively for the SCR value 11.4 and the fault at the MMC converter terminals. Along with the MMC DC current, the fault current measured at the fault point is also plotted, denoted as I_{fltPu}. It is noted that the DC voltage does not return to zero at the fault, which is attributed to the system's use of a metallic return conductor with a resistance of 0.05 Ω/km. This resistance leads to a small voltage buildup due to the ongoing flow of fault current. As a result, there is a potential between the MMC ground terminal and the system ground.

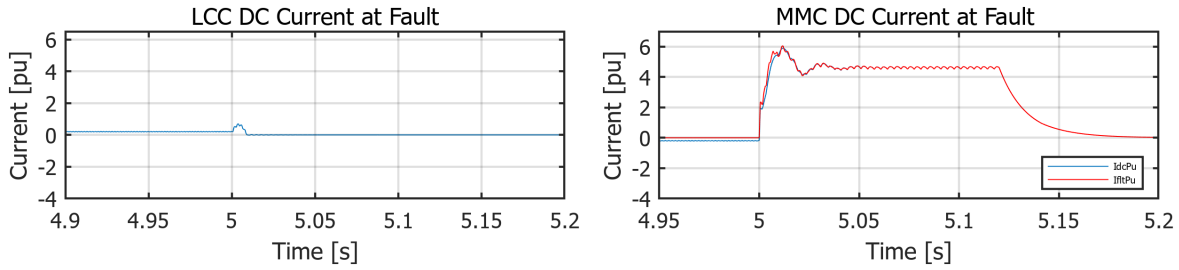


Figure 4.6: LCC and HB MMC DC current for fault at MMC terminals and SCR-11.4 on the MMC AC side.

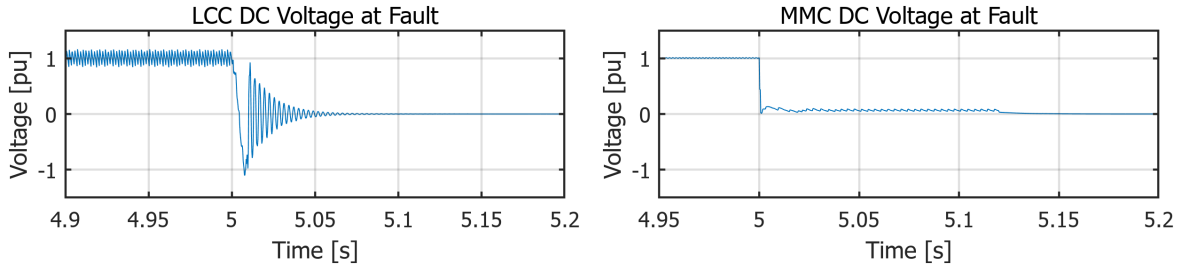


Figure 4.7: LCC and HB MMC DC voltage for fault at MMC terminals and SCR-11.4 on the MMC AC side.

Further, the fault contribution from each converter and performance can be analysed separately. For LCC, a control selection is implemented in the event of a fault. This is implemented as the fault current is detected, the control signal becomes active. Upon fault detection, with a delay of 3 ms, the LCC transitions to inverter mode by reversing the firing angle sequence, resulting in power flow reversal. This action causes the LCC to contribute a negligible fault current, which is rapidly redirected to the AC side, enabling fast fault clearance. The fault current response of LCC shown in Figure 4.6, validates this. For the fault at the point at the MMC converter terminal, the fault current is approximately 0.7 pu. This is also examined without any delay after the fault current detection to signal activation, and the current observed is 0.4 pu. If the fault is at the point at the LCC converter terminal, and the control activation is after the specified delay, the current rises to about 1.1 pu.

Now, examining the MMC DC current, there is a significant amount of fault current in three stages: initially, due to the discharge of its capacitance, which stops at converter

blocking; then, followed by a transient and steady-state current path facilitated by the diode freewheeling action from the AC grid. It is to be noted that the arm voltage follows the arm capacitor voltage during the fault. For a fault at MMC terminals, the transient peak value of the fault current from the MMC side reaches up to 6.05 pu.The steady state current of 4.66 pu flows up to 5.12 s till the AC CB opens at the MMC side. The MMC AC voltage and current drop to zero following AC grid disconnection, as shown in Figure 4.8 and 4.9. This analysis verifies the severity of HB-MMC's DC fault performance compared with the LCC, emphasising the need for alternative measures to improve the DC fault performance of the HVDC system.

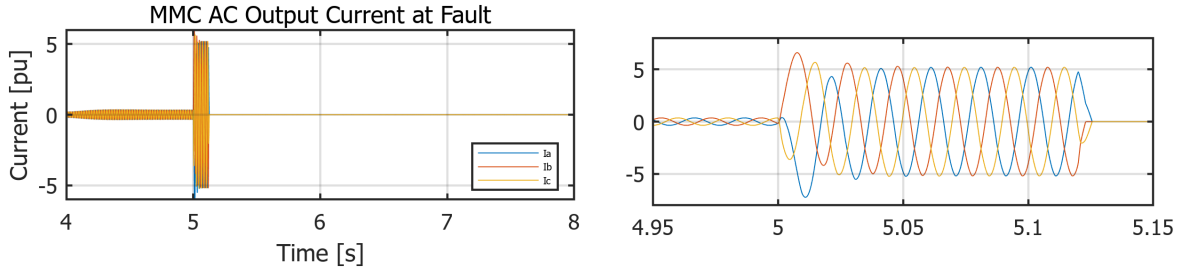


Figure 4.8: MMC AC output current for fault at MMC terminals and SCR-11.4 on the MMC AC side with AC CB operation.

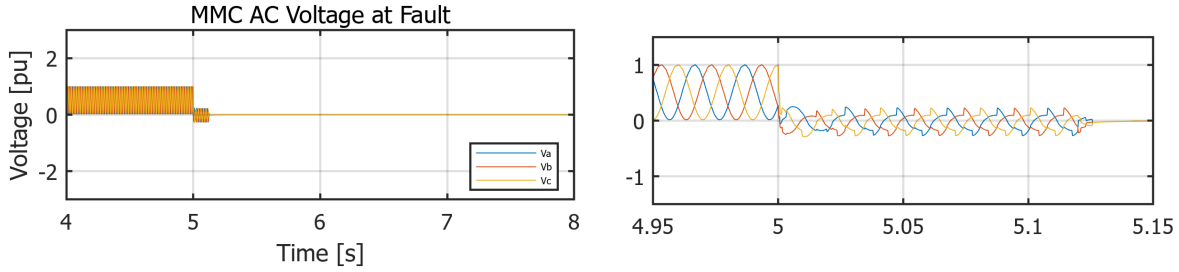


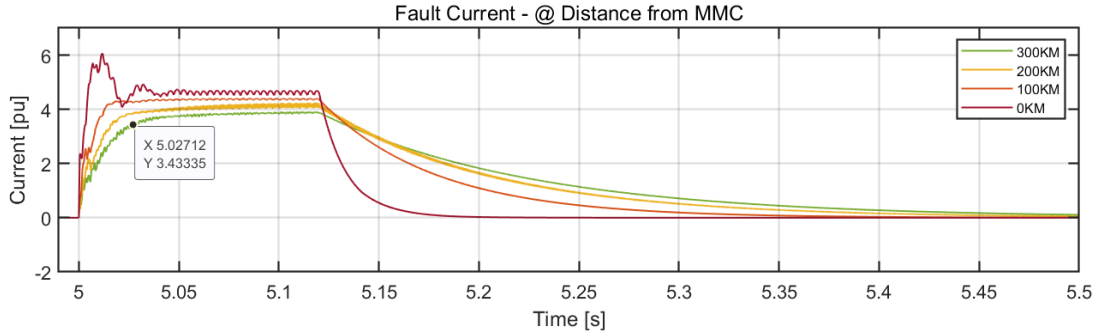
Figure 4.9: MMC AC Output voltage for fault at MMC terminals and SCR-11.4 on the MMC AC side with AC CB operation.

Now, the DC fault performance is analysed for two cases: fault location at a distance from the MMC converter and SCR variation of the connected AC grid of the MMC. A preliminary analysis was conducted to avoid redundant simulations by varying the fault location along the DC transmission line. Based on these results, the most critical fault scenario was identified near the MMC terminal, where subsequent fault cases were simulated at this fault point for varying SCR conditions. Figure 4.10a shows the fault current for different fault locations at varying distances from the MMC converter, simulated at the maximum SCR and Figure 4.10b shows the fault current for varying SCR values on the MMC's AC side, with the fault applied at the MMC converter terminal.

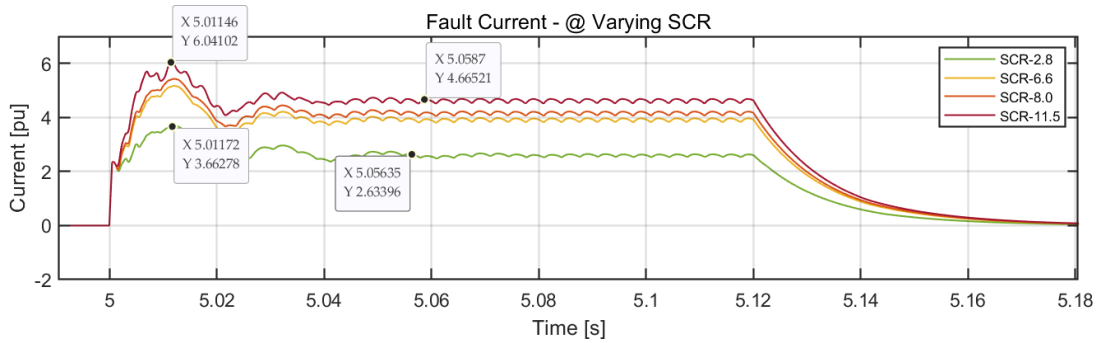
As shown in Figure 4.10a, the peak value of fault current decreases from 6 pu to 3.43 pu when the fault distance increases from 0 km to 300 km, from the MMC converter. It is noted that the transient behaviour is significantly reduced at greater distances. However, during disconnection, the current takes a longer time to discharge. This indicates that the higher inductive reactance associated with a longer distance to the fault point from the

source causes a slower current change rate. For a stronger system with SCR of value 11.4, the peak value of transient fault current is 6.04 pu at the MMC terminal fault, and it is 3.66 pu for a weak system with SCR of value 2.8. Correspondingly, the steady-state value of fault current also decreases for the AC grid with an SCR of a weak system.

The highest severity of fault current—characterised by both a high magnitude and a steep rate of rise—occurs near the MMC terminal in this point-to-point system configuration involving LCC and HB-MMC. The results confirm that SCR and fault location significantly influence the magnitude and rate of rise of the fault current.



(a) Fault current at varying distances to the fault point from the MMC with maximum SCR .



(b) Fault current for varying SCR on MMC AC side with fault point at MMC terminal.

Figure 4.10: Characteristics of fault current for varying fault point distance and SCR values.

4.2 hHVDC Point to Point System with FB-MMC

This section details a point-to-point hHVDC system simulation using the FB-MMC configuration. This simulation verifies the inherent fault-blocking mode of FB-MMC in Section 4.2.1 and analyses the implementation of active fault clearing in Section 4.2.2. The voltage and current profiles during the steady-state operation are not repeated here as that follow the HB-MMC operation.

4.2.1 DC Fault Performance for FB-MMC Blocking

The sequence of operations in the simulation scenarios is the same as the HB-MMC study case, as summarised in Table 4.1, with the change that AC CB operation is not required for fault current clearing. The fault detection and blocking logic is the same as applied for HB-MMC. As a preliminary step, the DC current and voltage behaviour during the fault period is analysed for both MMC and LCC. Figure 4.11 illustrates the DC current profiles of the converters during the fault, while Figure 4.12 shows the corresponding DC voltage waveforms.

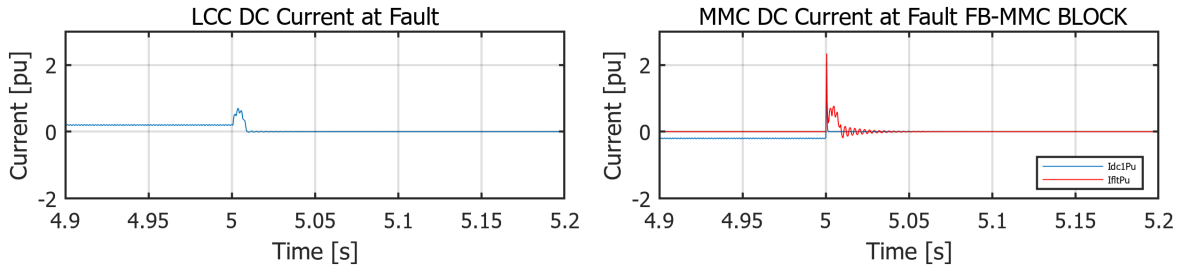


Figure 4.11: LCC and FB-MMC converter DC current during the fault with blocking.

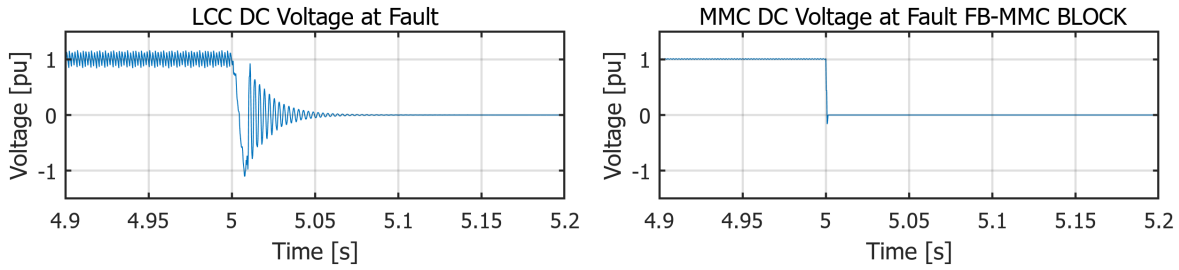


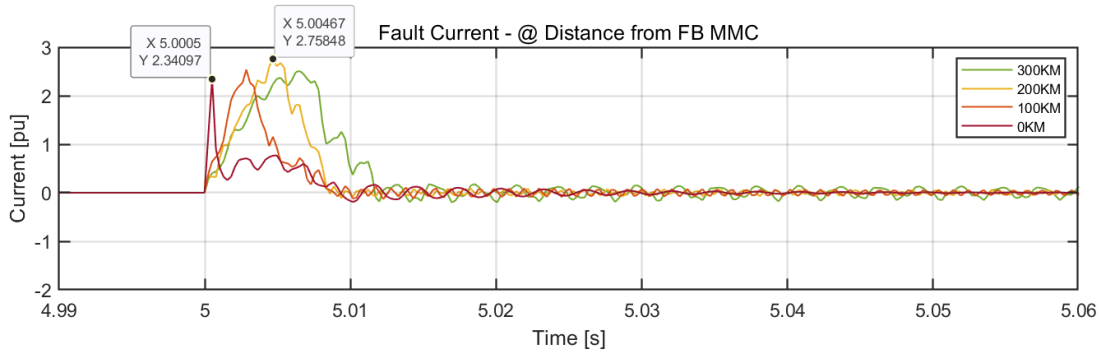
Figure 4.12: LCC and FB-MMC converter DC voltage during the fault with blocking.

As expected, the DC current and voltage during the fault and the clearing process remain unchanged for the LCC, similar to the behaviour observed in the hHVDC system with an HB-MMC. A distinctive response is on the MMC side with the FB configuration now. The DC current reaches a peak of 1.98 pu at 0.4 ms and afterwards the current decays. This is because, as the protection logic detects its threshold value, instantaneous blocking is activated. As a result, the current rapidly drops to zero by approximately 1.2 ms. As previously explained in Section 3.4.1, during blocking in the FB-MMC, the capacitor voltage is applied in opposition to the current direction due to the circuit configuration, effectively suppressing the fault current.

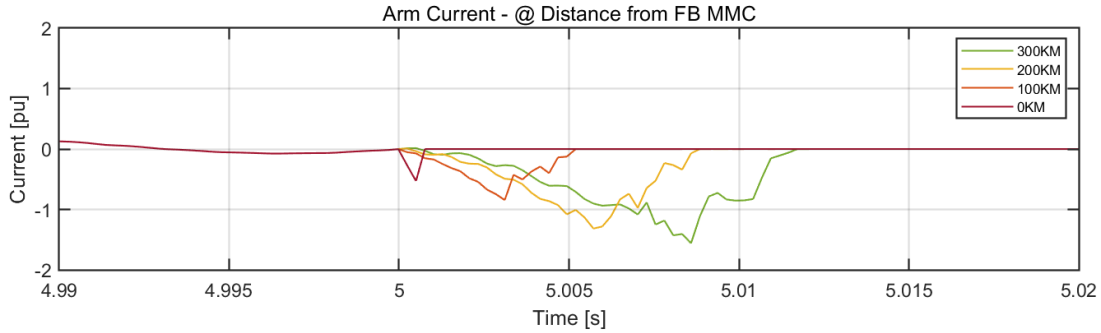
Figure 4.11 also shows the fault current I_{fltPu}, which is measured at the fault point. This current does not decay as fast as the DC current and exhibits oscillations before fully decaying after several milliseconds. This behaviour shows the contribution from the transmission cable to the fault current. During the rising period of the fault current, the arm capacitor voltage also shows a dip due to the discharge of stored energy. As the fault current subsides, the capacitor voltage gradually returns to its initial value. Hence, further analysis was conducted to examine the fault current and arm current for faults

occurring at various distances from the MMC converter.

The arm current and the transmission line conductors contribute to energy exchange during a fault event, increasing the transient fault duration and arm current as the transmission line length increases. Figure 4.13a and Figure 4.13b show the fault current and arm current characteristics, respectively, for variation of the distance to the fault point from the converter. It can be observed that a transient current persists beyond the threshold value, even when the converter is blocked. For comparison with Figure 4.13a, on this discharge period, Figure D.1 in Appendix D presents the corresponding current waveform over the same time interval for the HB-MMC in blocking mode, illustrating its behaviour during the transient period. It is noted that the discharging of the capacitor is minimal compared to FB-MMC.



(a) Fault current at varying distances from the FB-MMC.



(b) Arm current at varying distances from the FB-MMC.

Figure 4.13: Fault current and arm current for varying fault point distance for FB-MMC blocking.

It is also noted that a significantly rippled MMC AC voltage waveform is associated with a fault at an increased transmission line from the MMC to the fault point. Although the HB-MMC also shows increased ripples as the fault point moves further from the converter, the severity of this is comparatively lower than that of FB-MMC blocking. Figure 4.14 illustrates the MMC's AC output voltage during the fault event at the FB-MMC terminal. In Figure 4.15, the AC output voltage during the fault event at a point 200 km away from the FB-MMC converter shows a higher distorted waveform compared to that of the AC voltage for the fault at the converter terminal.

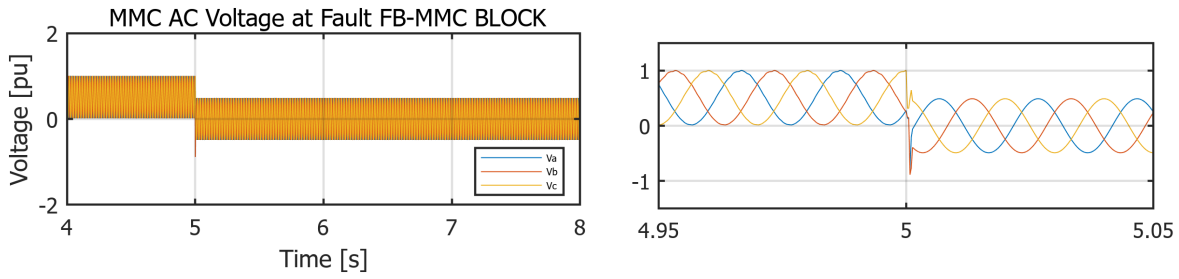


Figure 4.14: AC output voltage during the blocking for a fault at the FB-MMC terminal.

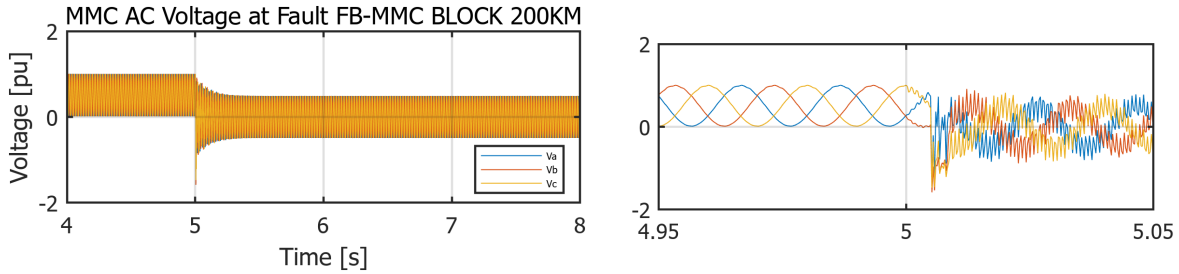


Figure 4.15: AC output voltage during the blocking for a fault at 200 km from the FB-MMC terminal.

The simulation demonstrates the DC fault response of the FB-MMC, showing rapid fault clearance through converter blocking as the capacitors are connected in series through diodes, opposing the current flow from the AC grid. However, as outlined in Section 3.4.2, active fault clearing provides several advantages, as maintaining the controllability of the converter. The following section analyses the performance of the FB-MMC for fast fault clearing while preserving system controllability during the fault event.

4.2.2 DC Fault Performance for FB-MMC Active Fault Clearing

This section presents simulation results of DC fault performance in a point-to-point system employing active fault-clearing with the FB-MMC. Instead of blocking the converter, the control system adjusts the voltage reference signals for insertion indices in response to fault detection. The simulation event sequence and corresponding timings are consistent with those used in the FB-MMC blocking case, and the protection circuit configuration remains the same.

The output of the protection circuit, denoted as FLT, triggers control changes and activates the DC insertion ratio controller, as explained in Section 3.4.2. This controller compares the DC current to a zero reference and generates an output voltage to eliminate the fault current. To ensure a rapid response, the DC insertion ratio controller output must reach a sufficiently negative voltage when the FLT signal is activated. Previous analysis indicates that, with the system configuration analysed so far, the current reaches 2 pu at about 0.28 ms. This duration represents an extremely short period under worst-case scenario assumptions—specifically, that the fault occurs directly at the converter terminal, eliminating any contribution from transmission line inductance, and that the DC terminal inductance is at its minimum assumed value of 25 mH and no

further smoothing reactor added. The insertion of a full negative voltage is not required to clear the fault current; the capacitors also absorb the line inductance energy stored in the inductor during the fault, causing the capacitor overvoltage, which is prominent in the fault at a longer distance from the converter [8].

Considering the same simulation sequence of events applied in FB-MMC blocking mode of operation, a fault is applied at the MMC terminal point at 5 s, and the resulting voltage and current profiles are examined to assess the performance of the system. This analysis focuses on the DC fault current and voltage at the FB-MMC side, as the fault clearing method changed there. Hence, no repetition of LCC-side results is required. An analysis of the general characteristics shows that, similar to the fault blocking mode, the DC current in the FB-MMC decays rapidly, whereas the fault current displays oscillatory behaviour and a slightly delayed reduction.

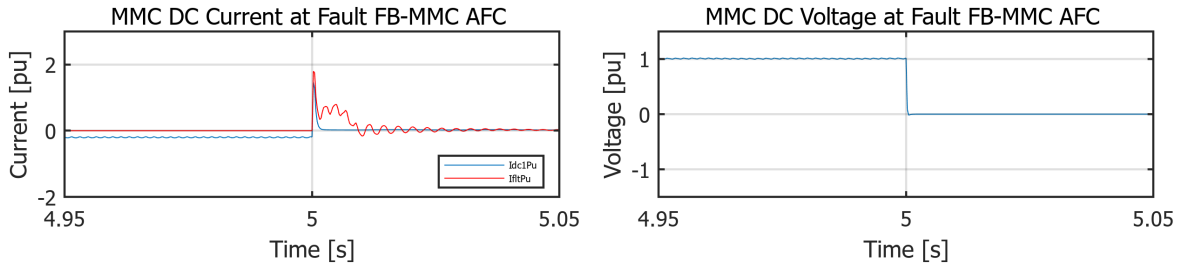


Figure 4.16: DC current and voltage during the fault for MMC, with FB-MMC active fault clearing.

The closer examination of the current in blocking mode and active fault clearing, as shown in Figure 4.17, provides a better understanding of the characteristics of current decay. It is noted that with active fault clearing, the fault current decays to zero faster than the converter blocking. It is understood that the uncontrolled current flow and dissipation of capacitive energy are reduced with active fault clearing.

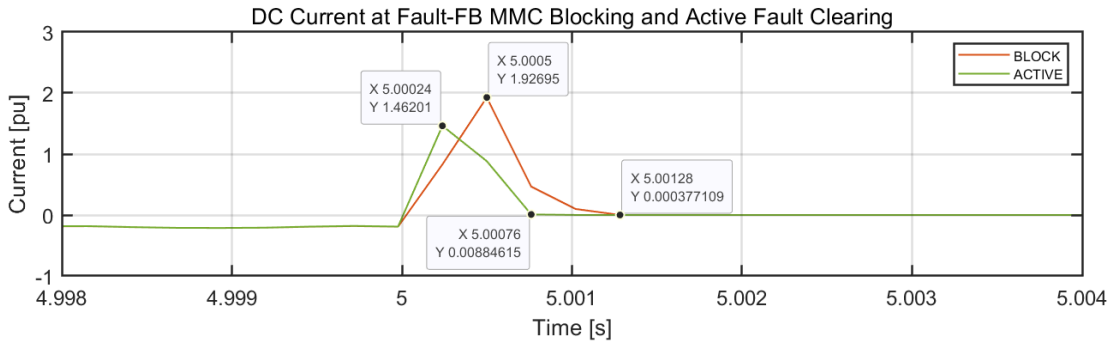


Figure 4.17: Comparison of DC current during fault with FB-MMC blocking and active fault clearing.

For active fault clearing, as the negative voltage is inserted as an output of the DC insertion ratio controller, providing better control for clearing the fault. This is further evident by comparing the parameters and characteristics of the fault at a distance 200 km from the MMC to the fault at the MMC terminal analysed so far in this section.

A comparison of the DC current, DC voltage and the DC insertion ratio of the FB-MMC converter for the fault converter terminal and 200 km away from the terminal is presented here. As active fault clearing is implemented, different DC insertion ratios, as in Figure 4.19, are observed depending on the current characteristics, as in Figure 4.18, when the fault point distance from the source changes. As previously noted, a smaller slope and slower current decay along the transmission line from the converter are attributed to the inductive reactance that is added as the transmission line length increases.

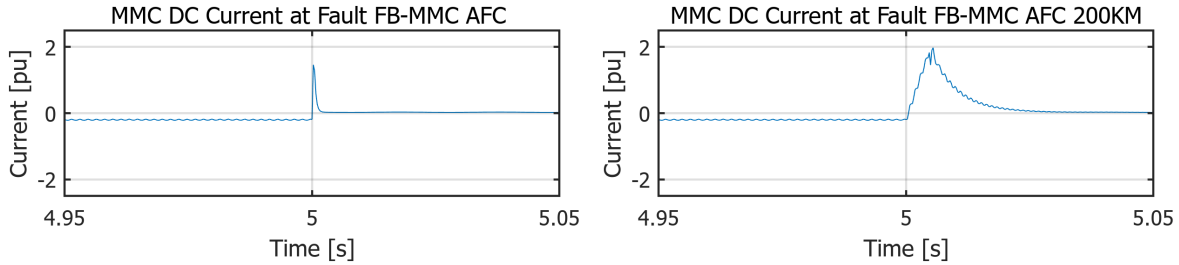


Figure 4.18: The DC current for fault at FB-MMC terminal and 200 km away with active fault clearing.

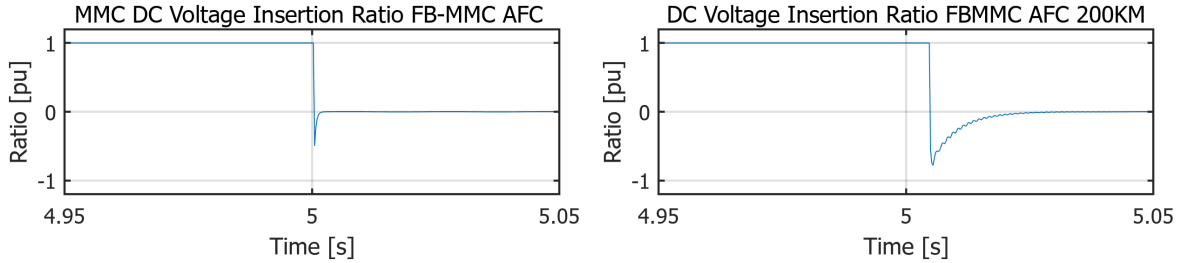


Figure 4.19: The DC voltage insertion ratio for the fault at FB-MMC terminal and 200 km away with active fault clearing.

There is no transient voltage at the DC terminal for a fault at the MMC terminals. However the energy exchange with the transmission medium causes transient voltage in the DC terminal voltages, when the fault is at 200 km away from MMC as shown in Figure 4.20, However, due to the adjustable negative voltage, the DC transient voltage is considerably reduced when an active fault clearing is applied than when a blocking mode of FB-MMC is used. As previously mentioned, the generation of this negative voltage depends on the PI controller within the DC insertion ratio controller. A more detailed tuning and stability analysis of this controller remains an area for further investigation. Figure D.2, provided in the Annexure D, provides a comparison of voltage magnitude for both modes of fault clearing for a fault located 200 km away.

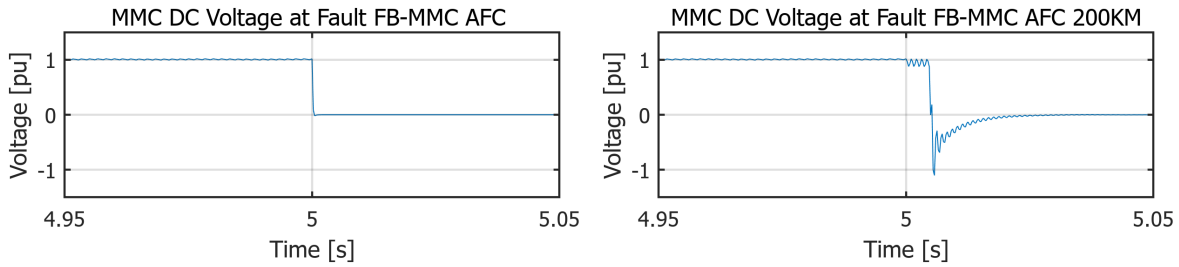


Figure 4.20: The DC voltage for fault at FB-MMC terminal and 200 km away with active fault clearing.

It was previously noted that the converter AC voltage exhibits transient over-voltages with higher ripple during faults, when the converter transitions to blocking mode. The unbalanced arm energy and transmission line energy transfer are prominent as the transmission length increases. Active fault clearing enables reduced ripples, as demonstrated in Figure 4.21, as compared to Figure 4.15 for a fault at 200 km away applying blocking mode. However, a high transient in AC voltage during the control change occurs because the arm sum voltage controller initiates to regulate the arm energy. However, keeping the arm voltage controlled at its rated level is required to provide AC voltage support further, working as a STATCOM.

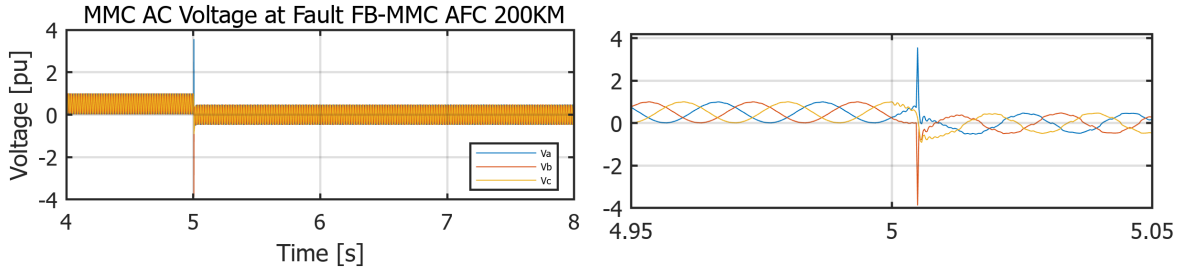


Figure 4.21: FB-MMC converter AC voltage for fault at 200 km away from MMC with active fault clearing.

4.3 Summary

This chapter presented a simulation of a point-to-point hHVDC system utilising both the HB-MMC and FB-MMC configurations. Initially, the characteristics and general performance of the DC fault for the HB-MMC were analysed, noting the long fault-clearing time associated with this configuration. Subsequently, the inherent fault-blocking capability of the FB-MMC configuration was verified, and an improved method for fault clearing, known as active fault clearing, was examined. The advantages of implementing active fault clearing have been demonstrated by the simulations conducted thus far.

Chapter 5

Simulation:Mutiterminal hHVDC Systems

So far in the thesis, the DC fault performance of a point-to-point hHVDC system is analysed for HB-MMC Blocking, FB-MMC blocking and active fault clearing. Further, this chapter analyses the simulation of a three-terminal hHVDC system, an extension of the previously analysed point-to-point system. The additional converter introduced is an MMC, which is suitable for developing a multi-terminal system because of the advantages stated in the Table 1.1. However, since HB-MMC has inferior DC fault performance compared to LCC, this chapter analyses how the FB-MMC active fault clearing described in previous chapters enables fast fault clearing to resume power transfer through the healthy part of the system. This chapter is organised as follows: Section 5.1 will explain the system configuration and control sequence. Section 5.2 will examine the charging process of the MMC and the steady-state operation of the three-terminal system. Finally, Section 5.3 will analyse the DC fault performance of the verified system by applying active fault clearing in the MMC.

5.1 MTDC System Configuration and Simulation Scenario

Figure 5.1 illustrates a schematic representation of the three-terminal MTDC system analysed in this study. The MMC converters are connected to the DC transmission line with disconnector switches and enable the isolation of the faulted line after clearing the fault current in case of a permanent fault. The total length of the transmission cable between the MMCs is 200 km, consisting of two π-sections. In the existing point-to-point hHVDC system discussed throughout the thesis, the LCC and MMC share the same voltage and current ratings, ensuring that their power ratings are identical. All converter ratings are considered equal for the multi-terminal system analysed here, and the two MMCs are assumed to operate in inverter mode. An alternative design could involve two MMCs together, constituting the power rating of the LCC. However, using a higher-rated MMC allows for future system expansion by integrating additional generation resources, where a converter can operate as a rectifier, or a fourth converter can be added. The advantages of the VSC system include its ability to connect to islanded generation sources, such as wind farms and solar parks. LCC is a cost-effective solution for strong grids with generation sources that perform black starts. When connected to islanded sources, those sources need to regulate voltage and frequency independently. An example is the *grid-forming* (GFM) control in wind turbine converters, which helps maintain offshore AC grid stability.

Each MMC converter can operate using one of the outer control loops: AC voltage, DC voltage, active power, or reactive power. Among these, the d-axis controllers— the DC

voltage and active power control—are crucial for MTDC systems, as the DC voltage level depends on the power flow across the network. When combined with droop control, this configuration is referred to as DC grid primary control [47]. For simplicity, and considering only two MMC converters connected in the system, *FB MMC*1 is designated to operate in DC voltage control mode, while *FB MMC*2 is configured for active power control. Further coordinated control can be implemented when expanding the system with a third MMC. For LCC, the constant current control mode is activated. All other individual control and modelling of converters are the same as explained before in Chapter 3.

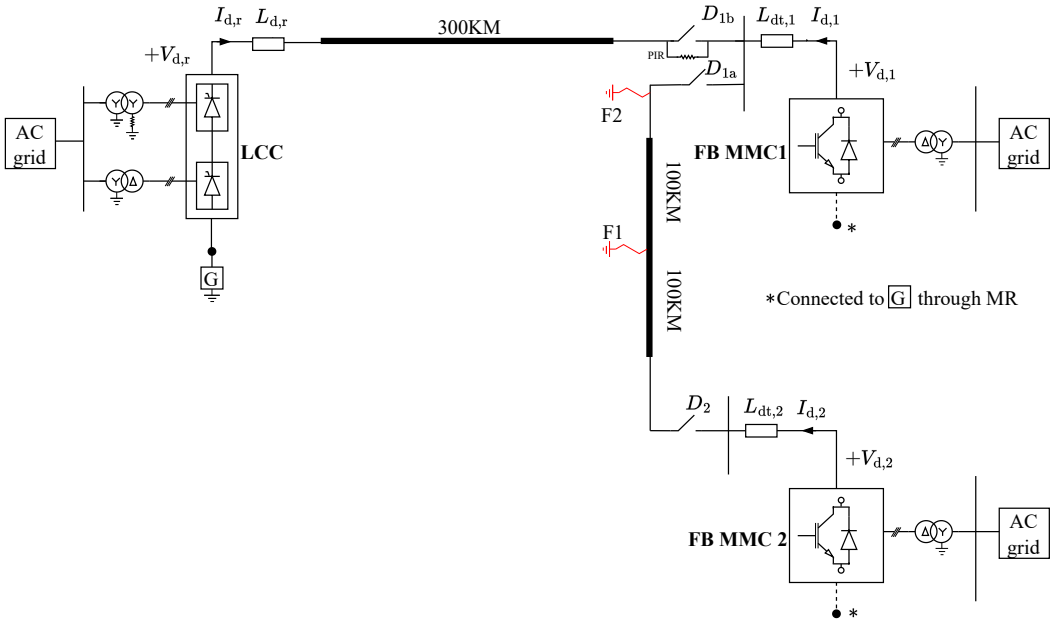


Figure 5.1: Schematic of hHVDC multi-terminal system.

5.2 MTDC system Steady State Operation

The two simulation scenarios before the DC fault are the MMC converter charging and connection to the LCC converter. The simulation sequence up to 5 s explained is for the charging period and steady state operation of the system. Table 5.1 summarises the simulation events with corresponding timing.

Description	Time [s]	Remarks
*FB MMC*1 Deblock, D_{1a} and D_2 Close	0.4	*FB MMC*2 DC side charging
DC Voltage Ramp-up to Rated Value	2.0	Depends on initial charge
D_{1a} Switch Closing	2.5	With PIR
LCC Deblocking	2.6	CC control
Active Power Reference Step at LCC	3	0.2 pu step,LCC to *FB MMC*1
Active Power Reference Step at *FB MMC*2	5	0.1 pu

Table 5.1: Sequence of steady state simulation events and timings for the MTDC hHVDC system.

As a starting procedure, the *FB MMC*1 at DC voltage control mode is deblocked at 0.4 s. The disconnector switches at the DC side for connecting the two MMCs D_{1a} and D_2 are closed at this instant enable the charging of *FB MMC*2 from DC side. The initial capacitance charge at both converters is 0.9 pu. Figure 5.2 shows the DC current for *FB MMC*1 and *FB MMC*2 for the charging period with a large current flow during the initial period and stabilising thereafter.

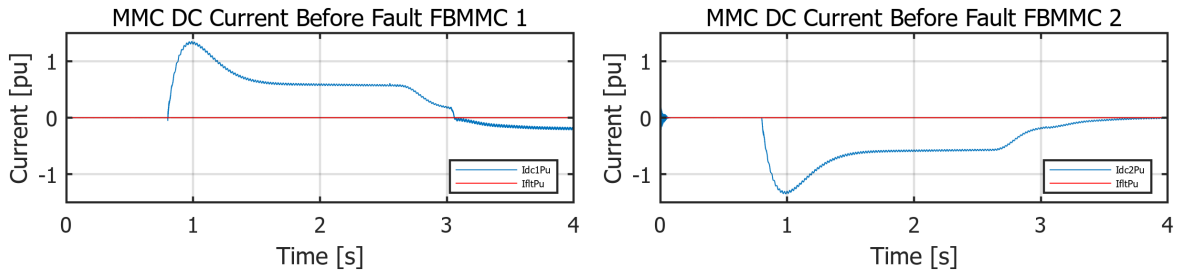


Figure 5.2: FB-MMC DC current during initial charging period, LCC not connected.

At 2.5 s as the *FB MMC*1, which is in DC voltage control mode, ramps up to rated DC voltage, the Switch D_{1b} closes and LCC is connected. The LCC is in current control mode, and the active power dispatch of 0.2 pu from LCC is initiated at 3.0 s. At this point, the power transmission is between *FB MMC*1 and LCC only. The power reference point of *FB MMC*1 remains zero, which is active only at 5.0 s. After this, the power flow is divided between the two MMCs. Figure 5.3 shows the DC current and voltage for *FB MMC*1, the voltage and current profile for *FB MMC*1 and LCC during the steady state operation is included in Annexure E.

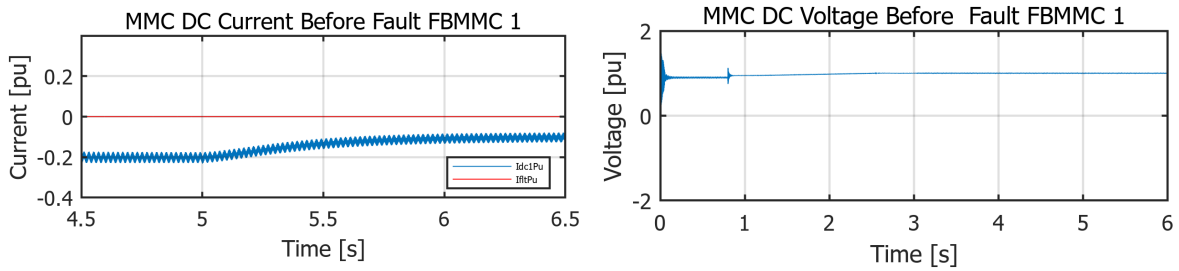


Figure 5.3: *FB MMC*1 DC current and voltage during steady state operation.

5.3 MTDC System DC Fault Performance

This analysis primarily aims to investigate the DC fault behaviour of a three-terminal DC system, with particular emphasis on the variation in fault current contributions from each converter. With minimal fault current contribution, fast fault clearing, and isolation of the faulty line, power transmission in the healthy sections continues. Two fault scenarios were considered to evaluate the system's behaviour under different conditions. The first fault point is located in the middle of the transmission line between the two MMCs, denoted as *F*1, while the second fault point is assigned near *FB MMC*1, denoted as *F*2. By these two fault events, the fault contribution from each MMC for faults occurring at varying

distances from the converter station can be differentiated. Upon detecting DC current that exceeds a predefined threshold, the signal *FLT* is activated. Unlike point-to-point systems with only one MMC converter and LCC, the DC current contribution and the fault current rise rate vary considerably between the MMCs.

The fault detection logic has been modified to ensure uniform application of fault-clearing measures across converters when a fault is detected. The fault propagation and time to reach the threshold for activating the protection circuit vary for each converter and depend on several factors, including the distance to the fault point and system configuration. The higher of the two FB-MMC DC currents is compared to the threshold value, triggering a coordinated fault signal for both converters simultaneously and ensuring consistent protection in the MTDC system.

Once the steady-state power transmission between the three converters is established, a DC fault event is simulated at 7.0 s. The Simulation scenario is stated in Table 5.2. For both fault points, the same time frame of simulation events is considered. Based on the previous simulations, it is evident that the fault contribution from the LCC is minimal. Therefore, the fault event analysed in the developed three-terminal systems is justified between the two MMCs.

Description	**Time [s]**	**Remarks**
DC Side Fault Event	7	LCC phase reversal
D_2 Open at *FB MMC*2	7.02	DC system LCC and *FB MMC*1

Table 5.2: Sequence of fault simulation events and corresponding timings for the MTDC hHVDC system.

Initially, the fault event *F*1 can be analysed. The DC voltage and DC current for the LCC are illustrated in Figure 5.4. This is consistent with the characteristics observed for LCC in previous simulations for point-to-point systems, where the phase reversal following fault detection allows for rapid fault clearing, resulting in minimal fault current contribution. Here, the fault point is farther away from LCC than in the previous cases.

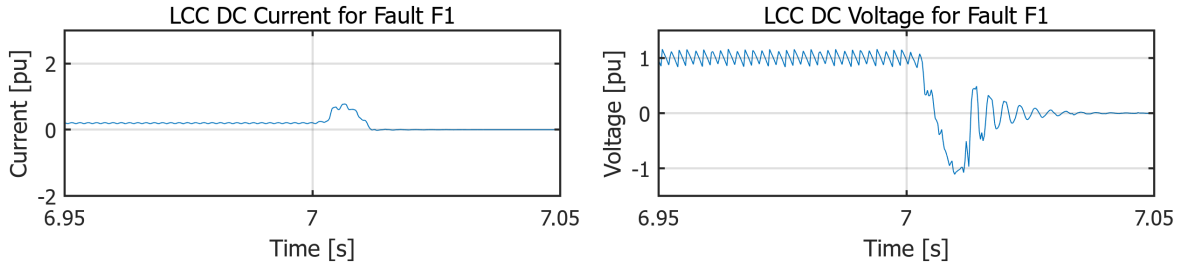


Figure 5.4: LCC DC current and voltage during the fault event *F*1 in MTDC.

For the MMCs, the fault current contribution is higher as shown in Figure 5.5 and Figure 5.6 below.

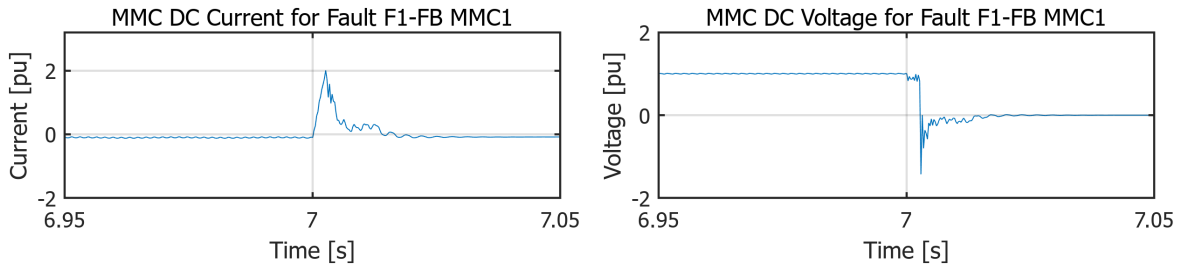


Figure 5.5: *FB MMC*1 DC current and voltage during the fault event at *F*1.

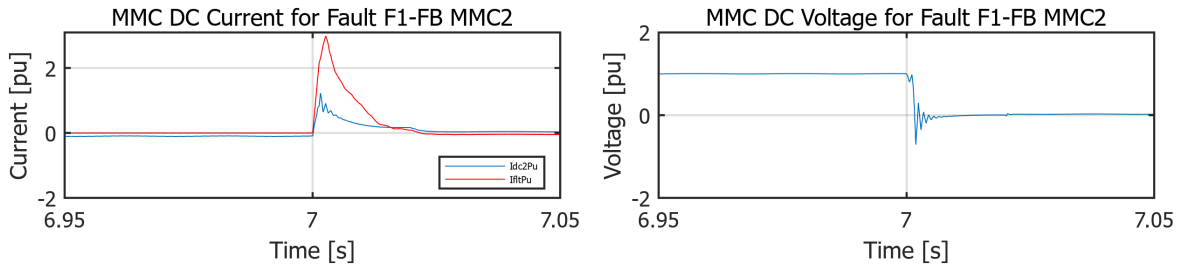


Figure 5.6: *FB MMC*2 DC current and voltage during the fault event at *F*1 .

The converter *FB MMC*1 has a higher fault contribution and also experiences higher DC voltage transients. The DC current from both converters constitutes the total fault current. The profile of DC current for both MMC converters with time to reach peak denoted as t_{p}, and the fault clearing time, denoted as t_{c}, is summarised in Table 5.3 below.

Converter	**Peak Value [pu]**	$t_{\mathrm{p}}\ [s]$	$t_{\mathrm{c}}[s]$
*FB MMC*1	2.007	7.00263	7.0073
*FB MMC*2	1.22	7.00159	7.016

Table 5.3: Fault current contribution *FB MMC*1 and *FB MMC*2 for fault event *F*1.

The time frame for both the rise of the current and the decay of the DC current of the converter varies, though the fault location is at the midpoint of the transmission line. The exact reason for the higher current contribution from *FB MMC*1 requires further investigation. One possible explanation could be variations in the connected DC-side inductances.

The uniform activation of fault-clearing logic in the system and control changes offers the advantage of initiating fault-clearing in the faraway converter early in the rise of its fault current. This early response minimises the contribution of fault current from that MMC. This effect is evident in the simulation of a fault event *F*2, which is at the terminals of converter *FB MMC*1 and far from the other converter. In this scenario, the DC current of *FB MMC*1 reaches the threshold value before that of the distant converter. As a result, the fault-clearing process is triggered earlier, effectively limiting the DC fault current contribution from the distant *FB MMC*2 during the fault event.

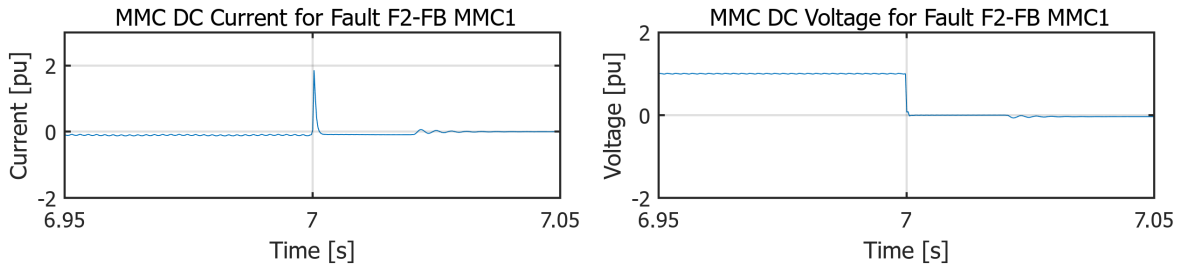


Figure 5.7: *FB MMC*1 DC current and voltage during the fault event *F*2.

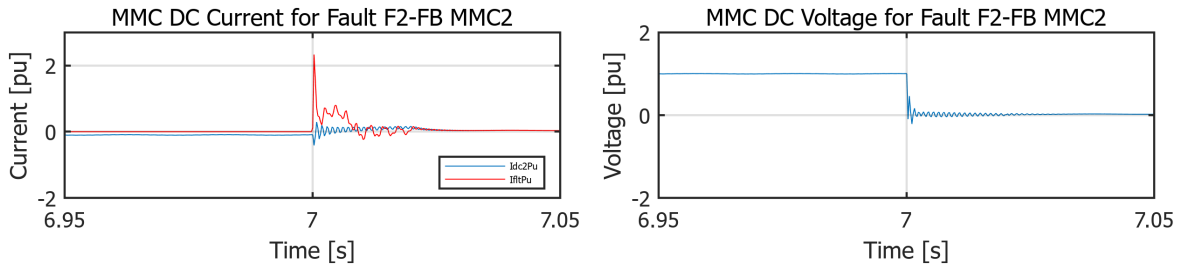


Figure 5.8: *FB MMC*2 DC current and voltage during the fault event *F*2.

It can be noted that the DC current of *FB MMC*1 rises very fast as the fault is at its terminals. This results in an early activation of the fault clearing process in *FB MMC*2, such that the fault contribution is nearly zero as shown in Figure 5.8. In both fault cases, the DC current is cleared to zero in a shorter time frame. For the permanent fault, the faulty line can be isolated from the grid using a mechanical disconnector switch in 10 ms or slightly higher. So, power transmission can continue between *FB MMC*1 and LCC.

5.4 Summary

This chapter analyses the DC fault performance of a three-terminal HVDC system, which extends the analysis conducted for a point-to-point configuration. The fault performance is evaluated based on DC current contribution, fault current rise rate, and the fault-clearing coordination between MMCs for faults occurring at various distances from the converter stations. The analysis demonstrates that uniform application of the fault-clearing process across all converters effectively minimises fault current contributions from distant terminals. Furthermore, the results validate that fast fault-clearing mechanisms enable prompt resumption of power transfer through the healthy sections of the network.

Chapter 6

Discussion

The thesis investigated the capability of the FB-MMC to provide fast fault clearing and examined how additional control changes for active fault clearing can enhance performance during fault conditions while maintaining controllability. The selected HVDC system architecture is a hybrid system where the FB-MMC is essential for improved operational capability, working along with LCC. At the same time, LCC and MMC together provide excellent DC fault performance, considered a technically viable and cost-effective solution in different geographical locations worldwide, taking into account the aspect of the connected generation source.

The thesis begins by outlining the necessary theoretical background to achieve this objective. Section 2.1 provides a brief introduction to HVDC system architecture, leading into a multiterminal DC system. Within this context, Section 2.1.1 details the fundamental principles of LCC converters, while Section 2.1.2 covers the fundamentals of VSC-MMC converters. Section 2.2 outlines the characteristics, challenges, and potential solutions for the hHVDC system, the system configuration followed in this thesis. Since the thesis aims to analyze DC fault performance by selecting a converter configuration, Section 2.3 examines DC faults in two parts: the characteristics of DC faults in Section 2.3.1, and the second part, in Section 2.3.2, focuses on analyzing DC systems protection through converter topology.

Chapter 3 serves as the foundation for the simulation in this thesis. Initially, Section 3.1 explains how the configuration of the DC transmission system is established. Given that the hybrid system comprises both LCC and MMC, an asymmetrical monopolar system is considered. Then, considering the HVDC projects implemented, the high-voltage DC side was selected as 500 KV. Following that, Section 3.2 discusses the modifications made to the existing CIGRE benchmark model for LCC model. Section 3.3 and Section 3.4 describes the HB-MMC modelling and FB-MMC modelling ,respectively.

A three-phase MMC is composed of six arms, each consisting of SM that includes capacitors and semiconductor switches. The modelling is performed by averaging these individual sub-modules. The AAM model and the control scheme for the voltage reference remain consistent for both HB and FB modules. The distinction between the two configurations lies in the switching circuit with blocking capability. Furthermore, with these two sub-module arrangements, three methods have been devised for fault clearing.

- HB-MMC Blocking as detailed in Section 3.3.2
- FB-MMC Blocking as detailed in Section 3.4.1

- FB-MMC Active fault Clearing as detailed in Section 3.4.2

In Chapter 4, the simulation of the hHVDC system is carried out based on the models and methodologies presented in Chapter 3. Initially, a point-to-point hHVDC system is simulated under DC fault conditions. Table 6.1 summarises the peak fault current, the time taken to reach the peak, and the fault-clearing time for MMC, where the fault current contribution is substantial. The active fault-clearing method of FB-MMC demonstrates a reduction in fault-clearing time while maintaining the controllability compared to the other two methods under the same system configuration. This includes the SCR value of 11.4 and a fault applied at the MMC converter terminal. FB-MMC active fault clearing shows better performance in terms of the voltage transient appearing in the event of a fault and blocking mode operation of FB-MMC.

Description	**Peak Fault Current [pu]**	**Time [s]**	**Fault Clearing**	**Time [s]**
HB-MMC Blocking	6.04	0.011	ACCB	0.12
FB-MMC Blocking	1.92	0.0005	By Blocking	0.00128
FB-MMC Active Control	1.46	0.00024	By Controlled Voltage	0.00076

Table 6.1: Time frame for fault clearing across converter fault clearing methods.

A steep rise in fault current, and hence a minimum time to activate the protection circuit, is the result of considering worst-case scenarios. This includes the fault point distance from the converter, eliminating transmission line reactances, a solid ground fault, and minimum reactance connected at the DC side of the system. Furthermore, the protection circuit for the MMC is considered to act instantaneously upon reaching the threshold value. The coordination between a fault detection method and the time for the protection circuit to act is a further area of study not included in this thesis. Additionally, it is essential to note that the peak fault current of the HB-MMC results from the free-wheeling diode action in the AC circuit, underscoring the necessity for a high-rated diode circuit in the converter to withstand this phase.

In Chapter 5, the simulation of the point-to-point hHVDC system is extended to a multiterminal configuration. The focus of the multiterminal system simulation is to analyse the fault contributions from individual converters and evaluate strategies for effectively reducing the total fault current and clearing the fault quickly. The primary approach involves activating the protection circuit to uniformly change the control mode across all converters when any of the converters reaches a threshold value for protection. This strategy proves effective in the current system configuration, as it significantly reduces the fault contribution from distant converters.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

In this thesis, the DC fault performance of both point-to-point and MTDC hHVDC systems is analysed. The study begins with the fundamental principles of converter operation, continues with the configuration of HVDC systems, and examines DC fault performance in relation to these converters. The modelling of converters was developed using PSCAD, with the LCC model utilising the PSCAD CIGRE benchmark model. The modelling of MMC was based on research publications that included HB and FB configurations, adhering to the AAM method, and each configuration included specific arm circuit configurations for enabling the blocking capability. The control scheme for all converter configurations during normal operations is the same. The DC fault performance was analysed for three methods: FB-MMC blocking, HB-MMC blocking, and FB-MMC active fault clearing. Accordingly, the AAM and control scheme were adjusted to accommodate the specific requirements of each operational mode.

During the blocking modes of HB-MMC and FB-MMC, conduction occurs through the diodes, resulting in an insertion index of one. For HB-MMC, the conduction of fault current continues through the freewheeling diodes. In contrast, the FB-MMC features two different paths for current direction across the capacitors, incorporating capacitors into the system circuit to halt fault current immediately upon activation of blocking. For the FB-MMC active fault clearing mode, two additional controllers are activated to adjust the DC and AC voltage references needed to calculate the insertion indices.

The analysis of DC fault performance focused on the time required for fault clearing, as well as the characteristics of fault currents. This is examined for different system characteristics and at different fault points. FB-MMC can clear fault currents through blocking, compared to the HB-MMC. This faster fault-clearing capability can be further enhanced through active fault clearing, maintaining controllability of the converter. This feature is particularly useful when extending to MTDC systems, demonstrating how quick fault clearing can prevent the loss of the entire system.

Based on the results presented from simulations, it can be concluded that the FB-MMC with active fault clearing represents a viable solution for MTDC systems, offering faster DC fault clearing times while being more economically advantageous than the HB-MMC with a DC circuit breaker. As such, the implementation of FB-MMC with active fault clearing in an MTDC system demonstrates the ability to quickly resume operation of the healthy segments, allowing the HVDC system to return to functional status in a shorter time frame.

7.2 Future Work

In this section, some aspects that could be relevant to investigate further, possibly improving the obtained results or yielding further findings, are outlined. However, they were not considered within the scope of this project.

- The active control system, maintaining the controllability, can support the grid with reactive power support during abnormal conditions. This can be checked how the grid code requirements can be met with FB-MMC working as STATCOM during the fault conditions.
- Research to understand how restoration time affects the transient stability of the connected AC systems while FB-MMC is employed. Gaining insights into this relationship can develop the system with FB-MMC to improve the connected AC system stability and reliability.
- There are studies in the literature focusing on the steady-state operation of MTDC systems and coordinated control. This can be further expanded with active fault clearing for more than two MMC converters, how the fault detection and control circuit transitions to be synchronised to ensure the contribution from each converter is minimal, and so optimise fault clearing time.

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A. SM Switching Representations

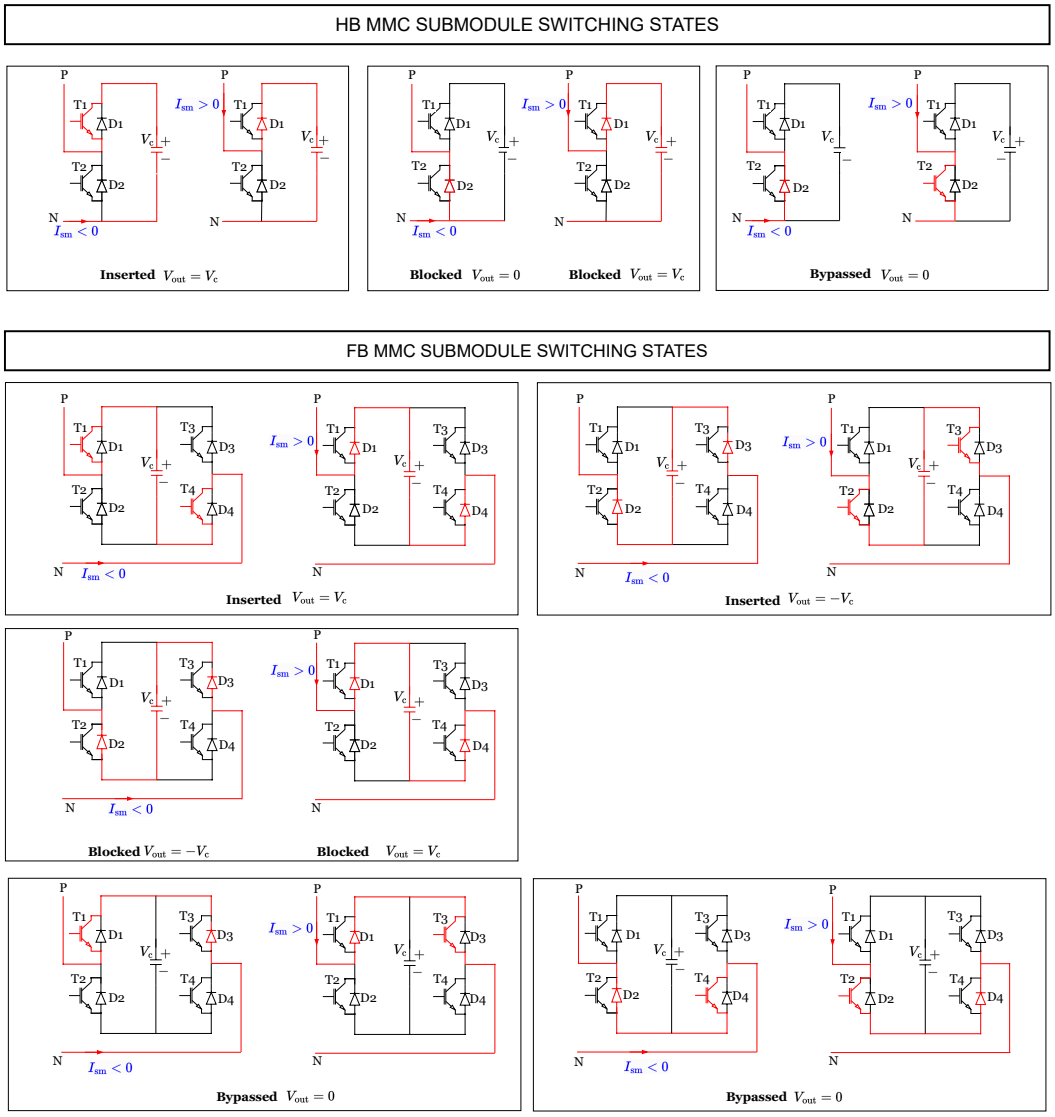

Figure A.1: Switching states of HB and FB MMC configuration-inserted, bypassed, blocked States

B. LCC Parameters

```
% The parameters are referenced from CIGRE Model
% ------------------------------------------------
Vs_r = 345;                                  % AC System Voltage (RMS, L-L) in kV
Rs_r = 1.1211;                               % AC System Series Resistance (Ohms),Rs_r = 3.737 in CIGRE model.
Rsp_r = 2160.633;                            % AC System Parallel Resistance (Ohms)
Lsp_r = 0.0453;                              % AC System Parallel Inductance (H),Lsp_r = 0.151 in CIGRE model.
f = 50;                                      % Frequency (Hz)
Pd = 1000;                                   % Total 12 Pulse Converter Power Rating in MW
f = 50;                                      % Frequency (Hz)
omega=2*pi*f;                                % Angular Frequency (rad/s)
C = 3.342e-6;                                % Reactive Compensation Capacitance (F)
Qc=Vs_r^2/(1/(omega*C));                     % Reactive Compensation in MVar
% ------------------------------------------------
% AC System Impedance Calculation
% ------------------------------------------------
Zs_parallel = (1j * omega * Lsp_r * Rsp_r) / (1j * omega * Lsp_r + Rsp_r); Zs = Zs_parallel + Rs_r;
disp(['AC System Impedance: ',sprintf('%.3f ∠ %.2f°', abs(Zs), angle(Zs) * (180/pi)), ' ohm']);
```

```
AC System Impedance: 14.283 ∠ 85.12° ohm
```

```
% The calculation for new values in Table 3.1
% ------------------------------------------------
Vs_rnew = 220;                               % New AC System Voltage (RMS, L-L) in kV------------
Rs_rnew = Rs_r*Vs_rnew^2/Vs_r^2 ;            % New AC System Series Resistance (Ohms)
Rsp_rnew = Rsp_r*Vs_rnew^2/Vs_r^2 ;          % New AC System Parallel Resistance (Ohms)
Lsp_rnew = Lsp_r*Vs_rnew^2/Vs_r^2 ;          % New AC System Parallel Inductance (H)
disp(['Rs_rnew:', sprintf('%.3f',Rs_rnew),',Lsp_rnew:',sprintf('%.3f',Lsp_rnew) ,' and
Rsp_rnew:',sprintf('%.3f',Rsp_rnew)]);
```

```
Rs_rnew:0.456,Lsp_rnew:0.018 and Rsp_rnew:878.594
```

```
Zs_parallelnew = (1j * omega * Lsp_rnew * Rsp_rnew) / (1j * omega * Lsp_rnew + Rsp_rnew); Zsnew = Zs_parallelnew +
Rs_rnew;
XbyRnew = imag(Zsnew) / real(Zsnew);          %(Recommended 5 < XbyR <20)
disp(['AC System Impedance new: ',sprintf('%.3f ∠ %.2f°', abs(Zsnew), angle(Zsnew) * (180/pi)), ' ohm']);disp(['X/R
ratio: ', sprintf('%.3f', XbyRnew)]);
```

```
AC System Impedance new: 5.808 ∠ 85.12° ohm
X/R ratio: 11.714
```

```
% SCR and ESCR Calculation
% ------------------------------------------------
SCR = Vs_rnew^2 / (abs(Zsnew) * Pd);
ESCR=SCR-Qc/Pd;
disp(['SCR: ', sprintf('%.3f', SCR), ' and ESCR: ', sprintf('%.3f', ESCR)]);
```

```
SCR: 8.334 and ESCR: 8.209
```

```
% Transformer Ratio Estimation
% ------------------------------------------------
Vd0 = 250;                                   % Maximum DC Voltage (kV) for one 6 Pulse
syms Vs_tr2                                  % Transformer Secondary Voltage RMS L_L
eqn = Vd0 == (3*sqrt(2)*Vs_tr2)/pi;          % Voltage Relationship DC to AC
sol = solve(eqn, Vs_tr2); Vs_tr2_approx = vpa(sol);
disp(['Transformer Secondary Voltage for the given DC voltage ,no firing angle: ',sprintf('%.3f',double(Vs_tr2_approx)),'
KV']);
```

```
Transformer Secondary Voltage for the given DC voltage ,no firing angle: 185.120 KV
```

```
% Transformer Inductance
%------------------------------------------------
Xt_r = 0.125;                                % Transformer reactance in pu,0.18 in CIGRE Model
Sbase = 500;                                 % Transformer Base MVA of 6 Pulse Connection
L_tr = (Xt_r*(double(Vs_tr2_approx))^2 /Sbase)/(omega);
disp(['Leakage Inductance: ', sprintf('%.3f', L_tr), ' H']);
```

```
Leakage Inductance: 0.027 H
```

```
%DC Voltage  with commutation drop and firing angle ,and  required AC Voltage
%-------------------------------------------------------------------------------
Rc = (3 * omega * L_tr) / pi;              %Commutation Resistance
Id=Sbase/Vd0;
alpha=15;                                  % Firing Angle
Vd=Vd0*cosd(alpha)-Id*Rc;                  % DC Voltage with commutation and firing angle
syms Vs_tr2_require ;eqn=Vd0==3*sqrt(2)*Vs_tr2_require/pi*cosd(alpha)-Id*Rc;
sol = solve(eqn, Vs_tr2_require);Vs_tr2_require_approx = vpa(sol);
% Based on the connected AC system, the required transformer ratio can be determined using the calculated secondary
voltage.
disp(['Transformer Secondary Voltage for the rated DC voltage with alpha and commutation:',sprintf('%.3f',
double(Vs_tr2_require_approx)),' KV']);
```

```
Transformer Secondary Voltage for the rated DC voltage with alpha and commutation:204.194 KV
```

C. MMC Parameters

```
% The parameters are referenced from PSCAD OPEN Model
% ------------------------------------------------
Vs_r = 240.5;                                % AC System Voltage (RMS, L-L) in kV
Rs_r = 0.88*0.35;                            % AC System Series Resistance (Ohms)
Rsp_r = 1000;                                % AC System Parallel Resistance (Ohms)
Lsp_r = 0.046*0.35;                          % AC System Parallel Inductance (H)
Pd = 1000;                                   % Converter Power Rating in MW
f = 50;                                      % Frequency (Hz)
omega=2*pi*f;                                % Angular Frequency (rad/s)
% ------------------------------------------------
% AC System Impedance Calculation
% ------------------------------------------------
Zs_parallel = (1j * omega * Lsp_r * Rsp_r) / (1j * omega * Lsp_r + Rsp_r); Zs = Zs_parallel + Rs_r;
disp(['AC System Impedance: ',sprintf('%.3f ∠ %.2f°', abs(Zs), angle(Zs) * (180/pi)), ' ohm']);
```

```
AC System Impedance: 5.069 ∠ 86.23° ohm
```

```
% The calculation for new values in Table 3.1
% ------------------------------------------------
Vs_rnew = 400;                               % New AC System Voltage (RMS, L-L) in kV------------
Rs_rnew = Rs_r*Vs_rnew^2/Vs_r^2 ;             % New AC System Series Resistance (Ohms)
Rsp_rnew = Rsp_r*Vs_rnew^2/Vs_r^2 ;           % New AC System Parallel Resistance (Ohms)
Lsp_rnew = Lsp_r*Vs_rnew^2/Vs_r^2 ;           % New AC System Parallel Inductance (H)
disp(['Rs_rnew:', sprintf('%.3f',Rs_rnew),',Lsp_rnew:',sprintf('%.3f',Lsp_rnew) ,' and
Rsp_rnew:',sprintf('%.3f',Rsp_rnew)]);
```

```
Rs_rnew:0.852,Lsp_rnew:0.045 and Rsp_rnew:2766.240
```

```
Zs_parallelnew = (1j * omega * Lsp_rnew * Rsp_rnew) / (1j * omega * Lsp_rnew + Rsp_rnew); Zsnew = Zs_parallelnew +
Rs_rnew;
XbyRnew = imag(Zsnew) / real(Zsnew);          %(Recommended 5 < XbyR <20)
disp(['AC System Impedance new: ',sprintf('%.3f ∠ %.2f°', abs(Zsnew), angle(Zsnew) * (180/pi)), ' ohm']);disp(['X/R
ratio: ', sprintf('%.3f', XbyRnew)]);
```

```
AC System Impedance new: 14.022 ∠ 86.23° ohm
X/R ratio: 15.162
```

```
% SCR and ESCR Calculation
% ------------------------------------------------
SCR = Vs_rnew^2 / (abs(Zsnew) * Pd);
disp(['SCR: ', sprintf('%.3f', SCR)]);
```

```
SCR: 11.411
```

```
% Transformer Ratio Estimation
% ------------------------------------------------
Vd0 = 250;                                   % Maximum DC Voltage (kV) for one Arm
syms Vs_tr2                                  % Transformer Secondary Voltage RMS L_L
eqn = Vd0 == (sqrt(2)*Vs_tr2/sqrt(3));          % Voltage Relationship DC to AC
sol = solve(eqn, Vs_tr2); Vs_tr2_approx = vpa(sol);
% Based on the connected AC system, the required transformer ratio can be determined using the calculated secondary
voltage.
disp(['Maximum Transformer Secondary Voltage for the given DC voltage : ',sprintf('%.3f',double(Vs_tr2_approx)),' KV']);
```

```
Maximum Transformer Secondary Voltage for the given DC voltage : 306.186 KV
```

1

D. Reference Figures for Point to Point hHVDC System

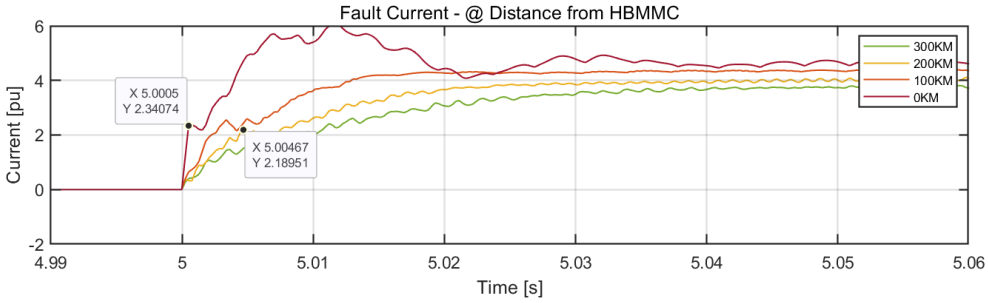

Figure D.1: For comparing HB-MMC blocking initial charging period at the same time frame with that of FB-MMC in Figure 4.13a

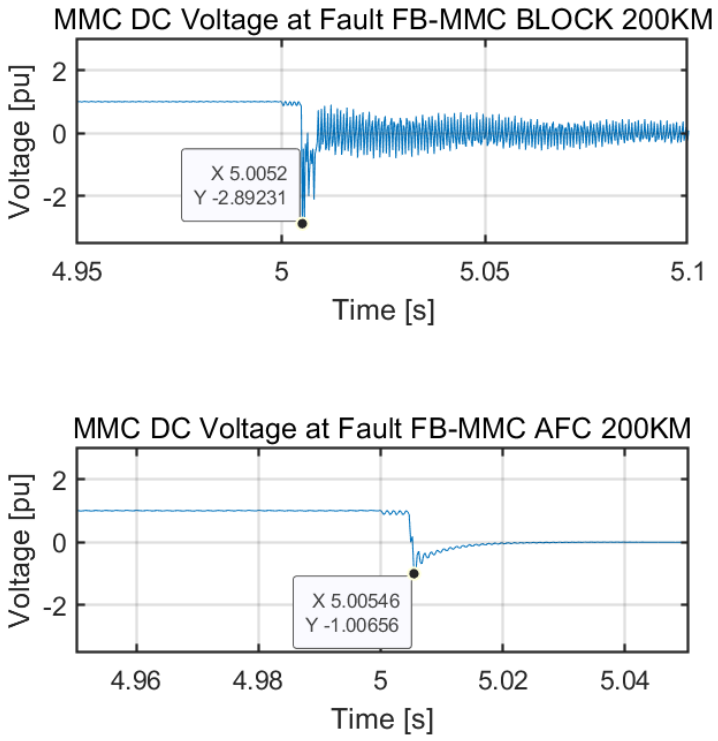

Figure D.2: Comparison of FB MMC DC voltage for fault at 200 km for blocking and active fault clearing

E. Refernce Figures for MTDC System

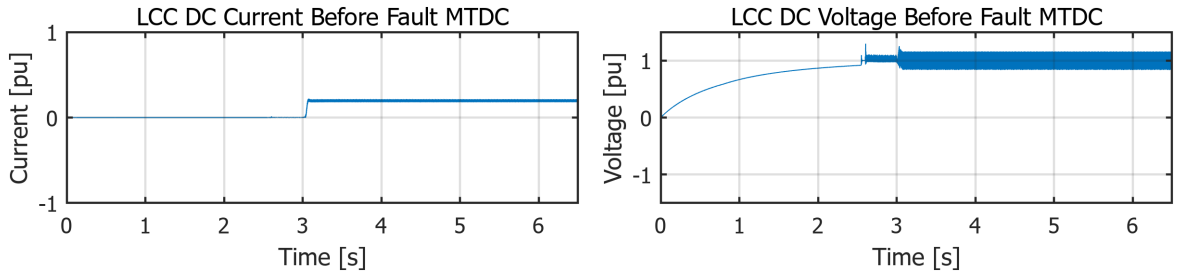

Figure E.1: LCC converter DC current and voltage during steady state operation of MTDC system

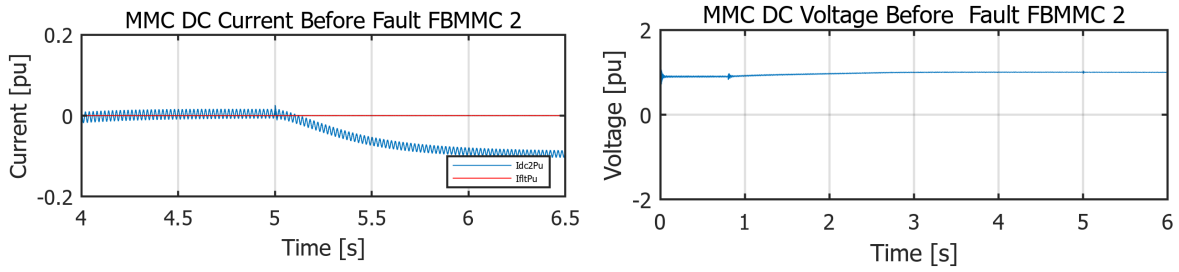

Figure E.2: *FB MMC*2 Converter DC current and voltage during steady state operation of MTDC system