High-Speed Accurate Digital Modeling of Power Electronics Systems

Project Report

PED4-1049/Xu Han

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STUDENT REPORT

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High-Speed Accurate Digital Modeling of Power Electronics Converters with Transient Dynamics

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Abstract:

This report presents a high-speed, high-fidelity simulation framework for power electronic converters that accurately captures MOSFET switching transients within circuit-level models. Leveraging Modified Nodal Analysis (MNA) and companion discretization methods, the framework automatically generates and solves circuit equations, including nonlinear device dynamics. A physics-based MOSFET model incorporates gate-charge behavior, voltage-dependent capacitances, parasitic inductances/resistances, and body-diode reverse recovery, and is validated through double-pulse experiments. To reconcile computational efficiency with waveform detail, a two-stage integration decouples system-level simulation—using ideal switches to identify switching events—from localized, high-resolution transient analyses. This modular approach facilitates rapid, accurate assessment of converter performance.

Contents

Summary

This report presents the development and validation of a high-speed, high-fidelity simulation framework for power electronic converters, with a focus on MOSFET transient behavior and its integration into circuit-level models. The work is motivated by the growing need for accurate yet computationally efficient tools that capture nonlinear dynamics—such as overshoot, reverse recovery, and parasitic effects—that conventional ideal-switch models neglect.

Objectives

Formulate systematic, time-domain circuit equations using Modified Nodal Analysis (MNA) and companion discretization methods.

Develop a physics-informed MOSFET model encapsulating gate dynamics, voltage-dependent capacitances, parasitic inductances/resistances, and body-diode reverse recovery.

Integrate the high-fidelity MOSFET model into system-level simulations via a two-stage framework.

Validate both circuit and device models against MATLAB/Simulink benchmarks and experimental data.

Methodology

Chapter 2 introduces systematic approach to construct mathematical formulation of a circuit and the solution of it, and provides validation.

Chapter 3 details the MOSFET equivalent circuit. Key parameters are extracted from datasheets and curve-fitted. The model is validated using double-pulse tests, showing close agreement between measured and simulated switching waveforms, with minor discrepancies attributed to package inductances.

Chapter 4 proposes a two-stage simulation. This decoupling achieves the speed of ideal-switch simulations while recovering detailed waveforms without re-solving the entire system at nanosecond resolution.

Results Validation

A three-phase inverter example demonstrates that the discretization-based MNA model and explicit model match Simulink benchmarks in waveform fidelity.

MOSFET switching waveforms obtained from double-pulse tests exhibit expected overshoot and ringing patterns that the model faithfully reproduces.

Successful integration of the high-fidelity MOSFET model and the circuit-level simulator, enabling dynamic MOSFET switching transient analysis under realistic operation.

Chapter 1

Introduction

1.1 Background

The global shift toward electrification, renewable energy, and advanced transportation systems has led to the widespread adoption of power electronic converters in applications ranging from electric vehicles and solar inverters to data center power supplies. These converters rely on fast-switching semiconductor devices such as MOSFETs and IGBTs to efficiently transfer and regulate power.

As switching frequencies increase and design margins shrink, accurate modeling of these converters becomes essential. Traditional simulation methods often rely on simplified switch models or idealized components that fail to capture critical transient phenomena, such as electromagnetic interference (EMI), overshoot, reverse recovery, or losses due to parasitics[1].

There is a growing demand for high-fidelity simulation frameworks that can accurately model these phenomena while maintaining computational efficiency. Such frameworks enable virtual prototyping, reduce the need for costly experimental iterations, and accelerate innovation in converter design.

1.2 Problem Statement

Existing commercial circuit simulation software presents a trade-off between accuracy and computational speed. SPICE-based tools can simulate detailed behaviors but are often slow and not suitable for large-scale simulations. Moreover, their accuracy depends heavily on the device models provided by the manufacturers. On the other hand, tools using idealized switch-level models such as PLECS offer fast execution but neglect nonlinear dynamics and parasitic effects critical for modern high-frequency designs.

A simulation framework that balances these requirements, accurately capturing nonlinear and transient behaviors of switching devices while maintaining simulation speed, is

still lacking. Moreover, there is a need for flexible modeling approaches that integrate easily with numerical solvers and support dynamic parameter updates from measurements or experiments.

1.3 Objectives

This project aims to develop a high-speed and accurate digital modeling framework that can capture switching dynamics, for power electronics systems. The key objectives are:

- To introduce a systematic methodology for modeling electrical networks and to formulate time-domain circuit equations suitable for numerical or discretized algebraic solutions.
- To apply a high-fidelity, physics-informed MOSFET model that captures gate dynamics, nonlinear parasitics, and reverse recovery effects.
- To integrate this detailed switch model into converter-level simulations.
- To validate the MOSFET model experimentally and the modeling framework against simulation benchmarks.

1.4 Methodology Overview

1. **Circuit Modeling and Mathematical Formulation**: Systematic formulation of power electronics circuits using MNA and symbolic stamping, allowing flexible inclusion of linear and nonlinear components.
2. **Numerical Solving**: Applying both continuous-time DAE solvers and time-discretized algebraic approaches to compare performance and accuracy.
3. **Switch Modeling**: Development of a detailed MOSFET model incorporating nonlinear capacitive effects, internal resistances, and body diode behavior.
4. **Experimental Validation**: Parameter extraction, and validation of simulated waveforms against measurements.
5. **Simulation and Demonstration**: A working example simulating standard topologies (half-bridge three-phase inverter), compared against simulation benchmarks.

1.5 Outcomes

The main contributions of this work include:

- A general modeling framework for constructing and simulating universal power electronic circuits.
- A high-fidelity half-bridge-configured switching behavioral MOSFET model that accounts for parasitics.
- Executable code integrating circuit-level simulation and high-fidelity MOSFET switching dynamics under steady-state operation along with a demonstration.

1.6 Thesis Organization

The remainder of this thesis is organized as follows:

Chapter 2 introduces the modeling of electrical networks using Modified Nodal Analysis (MNA) and systematic techniques or a direct approach to construct mathematical formulation, and their numerical or analytical solutions, and provides a comparative analysis and validation.

Chapter 3 presents a detailed high-fidelity MOSFET model that captures nonlinear and dynamic behaviors based on physics and experimental characterization.

Chapter 4 describes the integration of the MOSFET model into converter-level simulations.

Chapter 5 concludes the thesis, summarizing key findings.

Chapter 2

Electrical Network Modeling and Simulation

This chapter presents a general framework for modeling electrical networks using Modified Nodal Analysis (MNA) or other methods, with an emphasis on algorithmic construction of system equations and their numerical solution, before demonstrating with an example circuit.

Power electronics circuits usually include nonlinear, time-variant elements and may operate under transient conditions. To simulate these behaviors, circuits must be accurately modeled and mathematically formulated, often into systems of equations suitable for numerical solution.

A typical simulation process involves the following steps:

1. Circuit Representation: The circuit is translated into a schematic graph with nodes and branches, where each branch corresponds to a circuit element.

2. Mathematical Formulation: Applying Kirchhoff's laws, the physical behavior of the circuit is converted into a system of equations, often in the form of Differential-Algebraic Equations (DAEs).

3. Numerical Solution: Solve the DAEs using iterative methods or discretize them into algebraic equations before solving them linearly.

4. Postprocessing: Solution data is visualized to analyze voltages, currents, and other behaviors across the network.

2.1 Modified Nodal Analysis (MNA)

2.1.1 MNA Equation Structure

Modified Nodal Analysis is a well-established algorithm for writing circuit equations systematically. It extends traditional nodal analysis by incorporating current variables for certain elements that cannot be handled with nodal voltages alone, such as voltage sources and inductors[2].

Given a circuit described by a set of devices connected via nodes, MNA produces an equation of the form:

$$\mathbf{C}\,\dot{\mathbf{x}}(t) + \mathbf{G}\,\mathbf{x}(t) + f(x,t) = \mathbf{b}(t) \tag{2.1}$$

Where:

- $\mathbf{x}(\mathbf{t})$ is the vector of unknowns (node voltages and selected branch currents)
- $\mathbf{C}$ is the dynamic capacitance matrix
- $\mathbf{G}$ is the conductance (static) matrix
- $f(x,t)$ is the nonlinear current contribution (e.g., diode or switching behavior)
- $\mathbf{b}(\mathbf{t})$ contains contributions from independent sources.

2.1.2 Stamping Method

The Stamping technique is a systematic approach to construct MNA equations. It incrementally builds the matrices $\mathbf{C}$, $\mathbf{G}$, and vector $\mathbf{b}$ by "stamping" the local effect of each element into the global matrices.

Let i and j denote the indices of the nodes connected to the component. Define:

- $G(i,j)\ +\!= \alpha$ indicates adding α to the (i,j) entry of matrix $\mathbf{G}$.
- $C(i,j)\ +\!= \beta$ indicates adding β to the (i,j) entry of matrix $\mathbf{C}$.

Only stamps for non-ground nodes (i.e. $i,j > 0$). Below lists some examples of component stamping:

Resistor (R)

$I = (V_i - V_j)/R = G(V_i - V_j)$

Stamp:

$$\begin{aligned} G(i,i)\ +\!= G, \quad G(j,j)\ +\!= G \\ G(i,j)\ -\!= G, \quad G(j,i)\ -\!= G \end{aligned}$$

where $G = 1/R$

Independent Voltage Source (V_s)

$V = V_s(t)$, introduce ancillary branch current i_s
Stamp:

$$\begin{aligned} G(i, i_s) &+= 1, \quad G(j, i_s) -= 1 \\ G(i_s, i) &+= 1, \quad G(i_s, j) -= 1 \\ b(i_s) &+= V_s(t) \end{aligned}$$

Capacitor (C)

$I = C \frac{d}{dt}(V_i - V_j)$
Stamp:

$$\begin{aligned} C(i, i) &+= C, \quad C(j, j) += C \\ C(i, j) &-= C, \quad C(j, i) -= C \end{aligned}$$

Inductor (L)

$V = L \frac{dI}{dt}$, introduce current variable i_L
Stamp:

- Add new row/column for i_L

$$\begin{aligned} C(i_L, i_L) &+= L \\ G(i, i_L) &+= 1, \quad G(j, i_L) -= 1 \\ G(i_L, i) &+= 1, \quad G(i_L, j) -= 1 \end{aligned}$$

2.2 Numerical Solutions

The formulated DAEs can be solved numerically using e.g. MATLAB built-in solver ODE15s. ODE15s solver uses variable-step, variable-order methods based on numerical differentiation formulas (NDFs) or Backward Differentiation Formulas (BDFs), suitable for stiff problems. It solves the implicit equations using Newton-Rapeson iteration approach, estimates local error and adjust step size accordingly.

2.3 Discretization-Based Algebraic Formulation

Instead of formulating and solving DAEs directly, an alternation is to discretize the governing differential equations of inductors and capacitors beforehand to convert the circuit into a purely algebraic system.

This method discretizes all derivatives using a fixed time step, effectively eliminating derivatives from the equations and resulting in purely algebraic equations, as shown in equation (2.2).

$$\mathbf{G}\,\mathbf{x}(t) = \mathbf{b}(t) \tag{2.2}$$

The discretized capacitance or inductance will be modeled as companion models, as shown in Figure 2.1, each with an equivalent conductance in parallel with a branch current.

2.3.1 Capacitor Discretization

Applying the Backward Euler discretization to the capacitor current relation:

$$I = C\frac{dV}{dt} \implies i^{(n+1)} = C\frac{v^{(n+1)} - v^{(n)}}{h} = G_C \cdot v^{(n+1)} - I_{eq} \tag{2.3}$$

where $G_C = \frac{C}{h}$, $I_{eq} = G_C \cdot v^{(n)}$, h being the discrete time step.

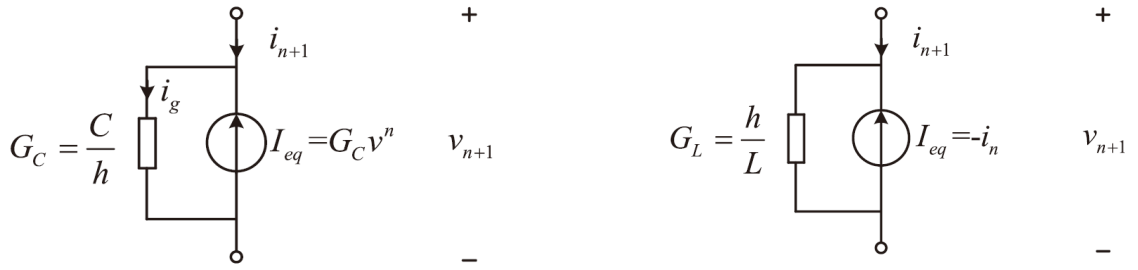
2.3.2 Inductor Discretization

Applying the Backward Euler discretization to the inductor voltage relation:

$$V = L\frac{dI}{dt} \implies v^{(n+1)} = L\frac{i^{(n+1)} - i^{(n)}}{h} \tag{2.4}$$

$$\implies i^{(n+1)} = \frac{h}{L}v^{(n+1)} + i^{(n)} = G_L \cdot v^{(n+1)} - I_{eq} \tag{2.5}$$

where $G_L = \frac{h}{L}$, $I_{eq} = -i^{(n)}$, h being the discrete time step.[3]



(a) Capacitor **(b)** Inductor

Figure 2.1: Companion Model of Capacitor and Inductor[3]

Diode

Diodes are modeled as binary resistors as previously discussed and will be stamped as resistors.

Linear Solution

The algebraic equation can also be solved linearly using Gausse Elimination or LU decouplesentaion method[].

2.4 Implementation

The discretization-based algebraic formulation is selected to represent circuit equations, which are then solved using MATLAB built-in linear methods. The model is developed and implemented using MATLAB scripts.

We leverage the MATLAB Object-Oriented Programming OOP features.

Component Classes

Each device type is implemented as a MATLAB class with methods:

- stampDC(A,b,numNodes): add its DC contribution.
- stampTransient(A,b,dt,prevVoltages,numNodes,branchCurrents): add its dynamic (companion) contributions.

Circuit Class

Holds a list of component objects, counts non-ground nodes (numNodes) and extra branches (numBranches), and implements following methods:

- analyzeTransient(t_end,dt,initialState):
  - For each time step, performs fixed-point iteration:
    1. Stamp all components.
    2. Solve G\b.
    3. Update nonlinear device states and repeat until converged.
  - Records node voltages and branch currents over time.

Netlist Parser

Users supply a table or text netlist; a parser builds component objects and invokes addComponent. This approach provides excellent extensibility, as changing circuit topology does not affect the core code and new types of devices can be added simply by writing new methods.

For more details see Appendix A Code Composition.

2.5 Demonstration and Validation

This section compares various modeling approaches benchmarked with Simulink continuous model and discusses the results on consistency and execution speed. An experimental validation is also included in the end.

A three-phase inverter with RL load is set as an example circuit to be simulated with following models: explicit model, generalized MNA and discretization-based algebraic formulation, and Simulink model.

To simplify the analysis, ideal power switches are used.

2.5.1 Model a: Explicit Model

It is sometimes possible to derive explicit expressions of a certain circuit topology.

For a three-phase half-bridge inverter with ideal switches, whose topology is shown in Figure , the following expressions can be derived based on circuit theories:

$$V_a(i) = V_{\text{in}} \cdot S_1(i), \quad V_b(i) = V_{\text{in}} \cdot S_3(i), \quad V_c(i) = V_{\text{in}} \cdot S_5(i)$$
$$V_O(i) = \frac{V_a(i) + V_b(i) + V_c(i)}{3} = \frac{V_A(i) + V_B(i) + V_C(i)}{3}$$

where V_j stands for phase voltages, i_j stands for phase currents, $j \in \{a, b, c\}$;
$S_x,\ x \in \{1, 3, 5\}$ represents gate functions.

Applying backward Euler discretization

$$V_a(n) - V_A(n) = L\frac{i_a(n) - i_a(n-1)}{\Delta t}$$

we can obtain recursive formulas for the phase currents as

$$i_a(i) = \frac{V_a(i) - V_N(i) + \frac{L}{\Delta t} \cdot i_a(i-1)}{\frac{L}{\Delta t} + R}$$
$$i_b(i) = \frac{V_b(i) - V_N(i) + \frac{L}{\Delta t} \cdot i_b(i-1)}{\frac{L}{\Delta t} + R}$$
$$i_c(i) = -i_a(i) - i_b(i)$$

and phase voltage formulas as

$$V_A(i) - V_N(i) = i_a(i) \cdot R$$
$$V_B(i) - V_N(i) = i_b(i) \cdot R$$
$$V_C(i) - V_N(i) = i_c(i) \cdot R$$

This model uses explicit recursive expressions to compute the value of circuit variables. Therefore it is extremely time efficient but is least flexible.

2.5.2 Model b: Discretization-Based MNA Model

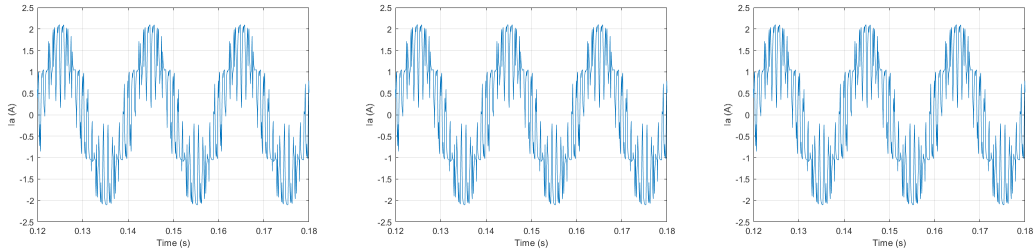
A netlist of the inverter is input to the universal MNA model using discretization methods discussed in the previous sections.

2.5.3 Model c: Benchmark - MATLAB/Simulink Model

MATLAB/Simulink model serves as a benchmark for the simulation. The model is configured as discrete model with a time step of 1e-6s, in consistence with the others.

2.5.4 Simulation Results and Discussion

Figure 2.2 compares the phase-a current waveforms from the three models. Table 2.1 compares their FFT (Fast Fourier Transformation) analysis.



(a) Model a: Explicit **(b)** Model b: MNA **(c)** Model c: Simulink

Figure 2.2: Comparison of Simulated Phase-A Current Waveform

Model	Explicit Model	MNA Model	Benchmark (Simulink)
Fundamental Amplitude	1.5761	1.5765	1.5754
Total Harmonic Distortion	0.2802	0.2805	0.2805

Table 2.1: Frequency Domain Analysis of the Simulation Data

The waveforms look almost identical, and the frequency analysis suggests great agreement of data, proving the validity and accuracy of the proposed models.

Regarding the computational efficiency, the explicit model costs less than 1 seconds, the Simulink model costs less than 10 seconds, while the MNA model costs around 20 seconds, for a simulation period of 0.5 seconds.

It is noticed that execution time of the MNA model does not increase linearly with respect to the total simulation length. So the computational efficiency of the Simulink model surpass that of the MNA model over a certain point. This may require further investigation on the solver.

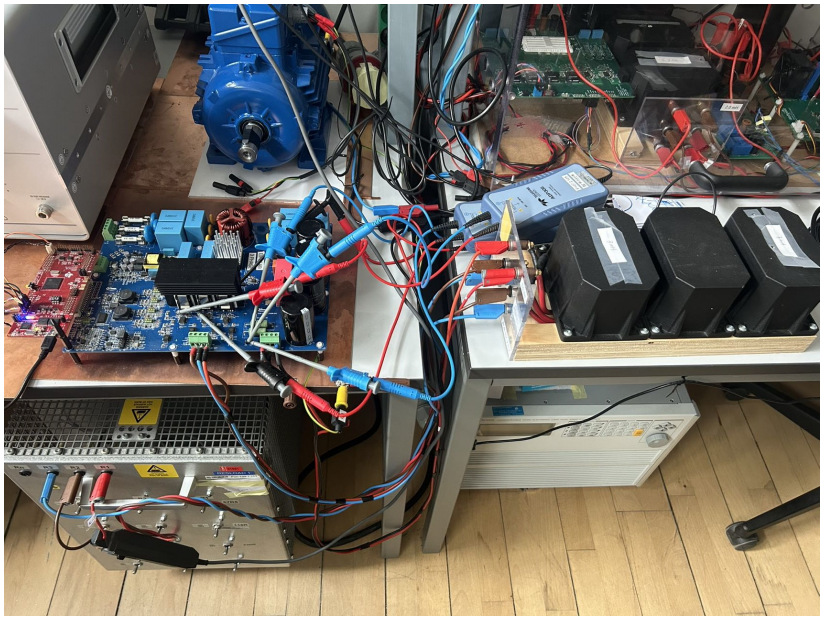


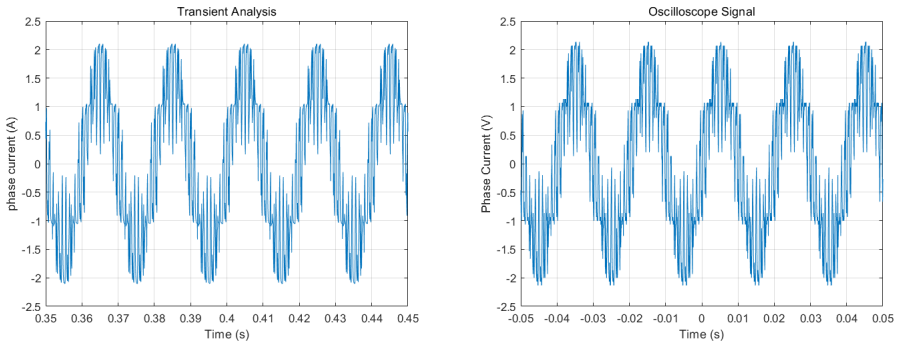
Figure 2.3: Inverter Experimental Setup

2.5.5 Experimental Validation

An additional experimental validation of the inverter circuit is conducted. The experimental setup contains an Infineon evaluation board integrating the circuit and a digital controller, a three-phase inductor in series with resistor loads, and probes and oscilloscopes, as shown in Figure 2.3.

Figure 2.4 illustrates a visual comparison of the simulation (a) and experimental data (b) of the phase-a current waveform.

Results from Figure 2.4 and Table 2.2 proves the fidelity of the model.



(a) simulation **(b)** experiment

Figure 2.4: Comparison of Phase Current Waveform

Model	Simulation (MNA)	Experiment
Fundamental Amplitude	1.5765	1.5433
Total Harmonic Distortion	0.2805	0.2646

Table 2.2: Frequency Domain Analysis of the Experimental Data

Chapter 3

MOSFET Transient Behavior Modeling

3.1 Introduction

Modern power converters operate at high switching frequencies with steep voltage and current transitions. Simplified models of MOSFETs—ideal switches with fixed on/off resistances—fail to capture the detailed transient behavior that critically affects efficiency, electromagnetic interference (EMI), and device stress. In this chapter, we construct a physics-informed high-fidelity MOSFET model suitable for accurate time-domain simulation.

This chapter includes:

- Reviewing MOSFET characteristic and switching dynamics.
- Introducing key parasitic elements.
- Presenting equivalent circuit models.
- Demonstration and validation in a half-bridge configuration.

3.2 Overview of MOSFET Characteristic

A high-fidelity model includes the following elements:

- Gate resistance: R_g
- Gate-source capacitance: $C_{gs}(V)$
- Gate-drain capacitance: $C_{gd}(V)$
- Drain-source capacitance: $C_{ds}(V)$
- Body diode: modeled as a parallel p-n junction with reverse recovery
- Parasitic inductances: L_g, L_s, L_d

Modes of Operation

Let:

- V_{gs}, V_{gd}, V_{ds}: terminal voltages
- V_{th}: gate-source threshold voltage
- K_P: transconductance constant

MOSFETs operate in three regions:

- **Cut-off**: $V_{gs} < V_{th}$; no conduction.
- **Triode (Linear)**: $V_{ds} < V_{gs} - V_{th}$; resistive channel.
- **Saturation**: $V_{ds} \geq V_{gs} - V_{th}$; current limited by gate.

The equivalent circuit of a power MOSFET switch during transitions is presented in Figure 3.1[4][5].

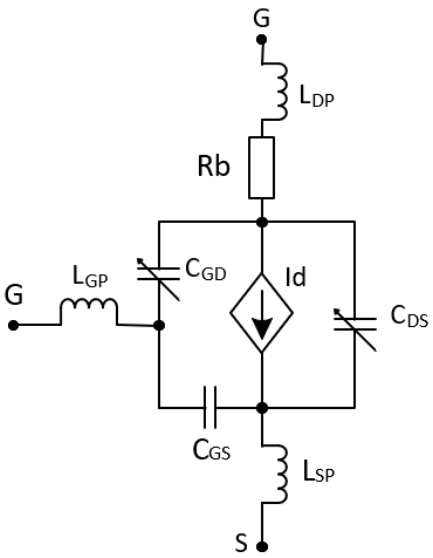


Figure 3.1: MOSFET Equivalent Circuit

Drain current

Drain current (channel current) I_D (I_{ch}) is governed by the following equations.

$$I_D = \begin{cases} 0, & V_{gs} < V_{th} \\ K_P(V_{gs} - V_{th})^2, & V_{gs} \geq V_{th}, \quad V_{gs} < V_{ds} + V_{th} \quad \text{(saturation)} \\ K_P[2(V_{gs} - V_{th})V_{ds} - V_{ds}^2], & V_{gs} \geq V_{th}, \quad V_{gs} \geq V_{ds} + V_{th} \quad \text{(triode)} \end{cases} \tag{3.1}$$

Stray Capacitance

The drain-source capacitance C_{DS} and gate-drain capacitance C_{GD} are modeled as voltage-dependent function using curve fitting techniques.

Body Diode

In a half-bridge configuration, the inactive MOSFET switch can be simplified using a free-wheeling diode model that includes forward current and junction capacitance behavior, as illustrated in Figure 3.2.

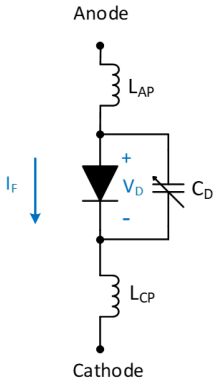


Figure 3.2: Diode Equivalent Circuit

Forward Current Modeling

The forward current I_F is given by:

$$I_F = \frac{V_D - V_{fto}}{R_d} \tag{3.2}$$

where: V_D is the diode forward voltage, V_{fto} is the diode threshold voltage and R_d is the diode on-state resistance.

Capacitance Modeling

The diode junction capacitance C_D is also modeled as a voltage-dependent function obtained by curve-fitting the MOSFET output capacitance C_{oss}.

3.3 High-Fidelity MOSFET Modeling in a Chopper Cell (Half-Bridge) Configuration

The most common application of MOSFET switches is in chopper cell (half-bridge) configurations. Since the switches are complementary in a chopper cell, the inactive MOSFET (soft-switching) can be simplified as a freewheeling diode. The model is demonstrated in Figure 3.3.

3.3.1 Circuit Description

The circuit is of a half bridge configuration and includes:

- A 4-pin MOSFET model with internal voltage-dependent capacitances C_{GS}, C_{GD}, C_{DS} and parasitic inductances and resistances.
- A freewheeling diode with voltage-dependent capacitance C_{D2}.
- A gate drive circuit supplying voltage V_{GG}.
- A main loop (load) circuit.

3.3.2 Mathematical Formulation

Following formula are constructed to describe the chopper circuit, applying relevant circuit laws[4].

$$I_G = C_{GS}\frac{dV_{GS}}{dt} + C_{GD}\left(\frac{dV_{GS}}{dt} - \frac{dV_{DS}}{dt}\right) \tag{3.3}$$

$$V_{GG} = V_{GS} + I_G R_G + L_G\frac{dI_G}{dt} + L_S\left(\frac{dI_D}{dt} + \frac{dI_G}{dt}\right) \tag{3.4}$$

$$I_D = I_{CH} + C_{DS}\frac{dV_{DS}}{dt} + C_{GD}\left(\frac{dV_{DS}}{dt} - \frac{dV_{GS}}{dt}\right) \tag{3.5}$$

$$I_L = I_D + I_F - C_{D2}\frac{dV_{D2}}{dt} \tag{3.6}$$

$$V_{DC} = V_{DS} + (L_C + L_{DP})\frac{dI_D}{dt} + L_S\left(\frac{dI_D}{dt} + \frac{dI_G}{dt}\right) + V_{D2} + I_D(R_P + R_B) \tag{3.7}$$

Therefore, the full MOSFET transient behavior can be described by a set of differential-algebraic equations (DAEs), as follows, and solved using ODE15s or similar numerical

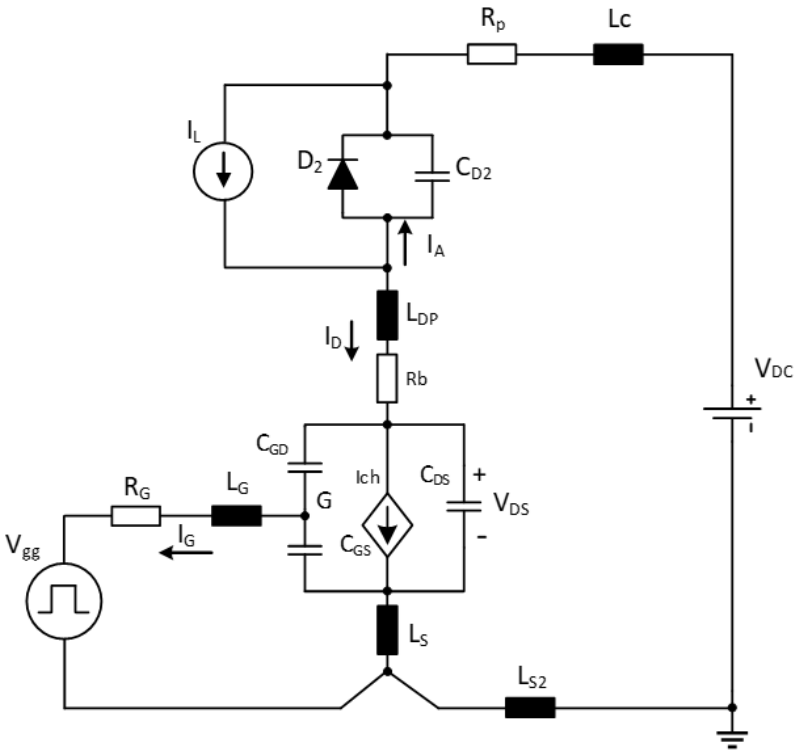


Figure 3.3: Half-Bridge-Configured Circuit Model[4]

solvers as previously described.

$$\frac{dI_d}{dt} = -\frac{L_sV_{gg} - L_sV_{dc} - L_gV_{dc} + L_gV_{ds} + L_gV_{d2} + L_sV_{ds} - L_sV_{gs} + L_sV_{d2} + L_gR_bI_d + L_sR_bI_d - L_sR_gI_g + L_gR_pnI_d + L_sR_pnI_d}{L_gL_s + L_gL_pn + L_pL_sn}$$

$$\frac{dV_{ds}}{dt} = \frac{C_{gd}I_d + C_{gd}I_g + C_{gs}I_d - C_{gd}I_{ch} - C_{gs}I_{ch}}{C_{ds}C_{gd} + C_{ds}C_{gs} + C_{gd}C_{gs}}$$

$$\frac{dI_g}{dt} = \frac{L_sV_{gg} - L_sV_{dc} + L_sV_{ds} - L_sV_{gs} + L_sV_{d2} + L_pV_{gg}n + L_sR_bI_d - L_sR_gI_g - L_pnV_{gs} - L_pR_gnI_g + L_sR_pnI_d}{L_gL_s + L_gL_pn + L_pL_sn}$$

$$\frac{dV_{gs}}{dt} = \frac{C_{ds}I_g + C_{gd}I_d + C_{gd}I_g - C_{gd}I_{ch}}{C_{ds}C_{gd} + C_{ds}C_{gs} + C_{gd}C_{gs}}$$

$$\frac{dV_{d2}}{dt} = \frac{I_f - I_L + I_d}{C_{d2}}$$

3.4 Model Validation

3.4.1 Parameter Sources

There are basically two ways of obtaining parasitic parameters of the MOSFET and body diode:

- Extract parameter from datasheet
- Fit empirical models using curve fitting on measured switching waveforms

In this section a model will be constructed using parameters extracted from the datasheet, and the model will be tested by comparing its simulation results with experiments in half-bridge configuration.

Stray Capacitance

C_{ds}, C_{gd}, and C_{gs} are extracted from the $C - V_{ds}$ curve provided in datasheet. Figure 3.4 shows the curve (a) and the digitization (b) process. This digitized data will be further curve-fitted into a function which can be called when solving ODEs.

Transconductance Constant

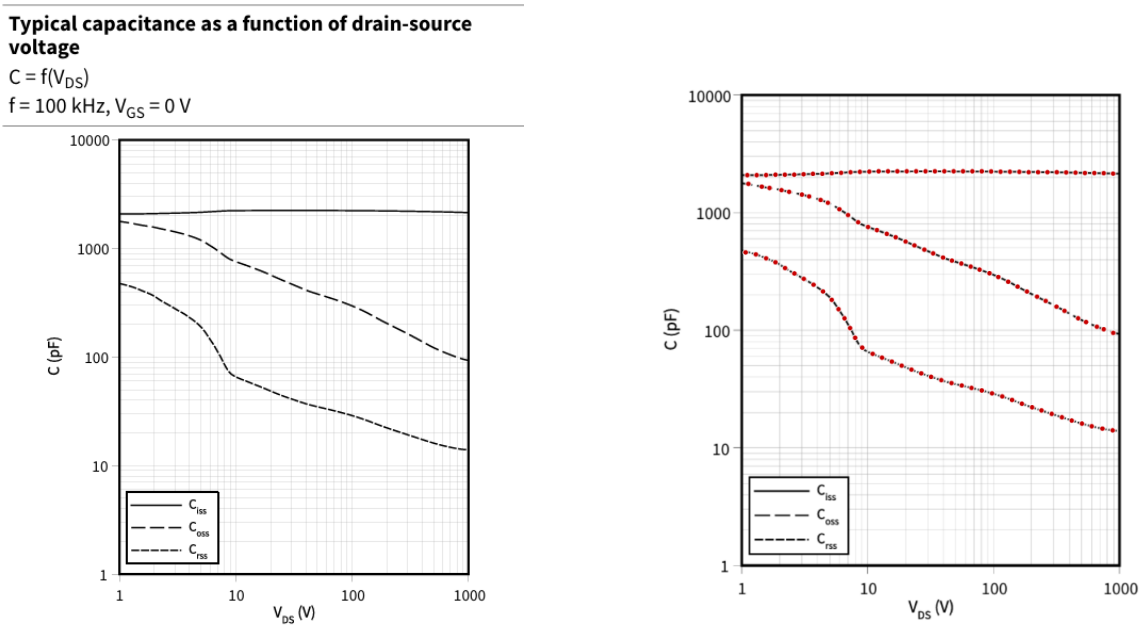
K_p is extracted by curve-fitting the transfer characteristic $I_D - V_{GS}$ provided in datasheet and using equation (3.8).

$$K_P = \frac{I_D}{(V_{gs} - V_{th})^2} \tag{3.8}$$

Spray Inductance

L_s is the common source inductance and L_{DP} is introduced by the drain package. They are usually obtained by experiments. It is in this case estimated as $L_p = 40nH$, $L_{DS} = 0.5nH$.

All other parameters can be read directly from datasheet.



(a) C-V Curve

(b) Digitization

Figure 3.4: Stray Capacitance Extraction

3.4.2 Double Pulse Test

The double pulse test is a widely used experimental method for evaluating the switching characteristics of power semiconductor devices and validating device models under realistic operating conditions.

The test involves applying two consecutive gate pulses to a device under test in a half-bridge or chopper configuration. The first pulse establishes a desired current level in the inductor, while the second pulse initiates a switching transition during which the dynamic parameters are captured.

3.4.3 Typical Switching Behavior

We expect to observe overshoots and oscillations in V_{ds} and I_d due to parasitic inductance and capacitance.

Figure 3.6(a) shows the V_{ds}, I_d, and V_{GS} waveforms in a double pulse test. (b) and (c) provide the zoom-in views of the turn-off and turn-on transitions respectively. For comparison, Figure 3.7 shows the corresponding simulated waveforms by the constructed MOSFET model for turn-off (a) and turn-on (b) transitions. The experimental results show reasonable agreement with the simulation, confirming the validity of the MOSFET model. However, larger oscillations are observed in the experimental data, possibly due to mismatched loop or package inductance and AC impedance.

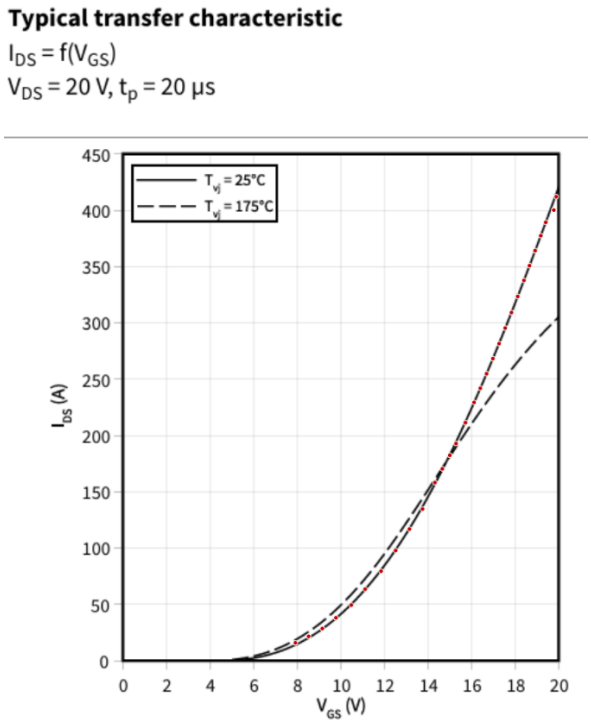
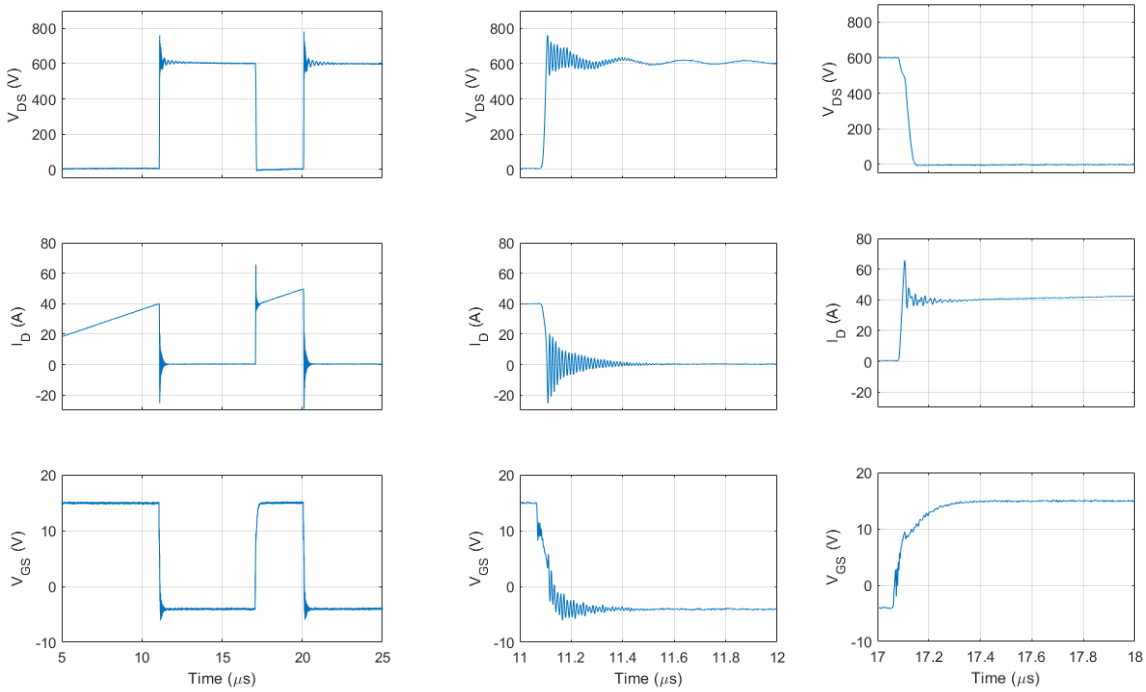
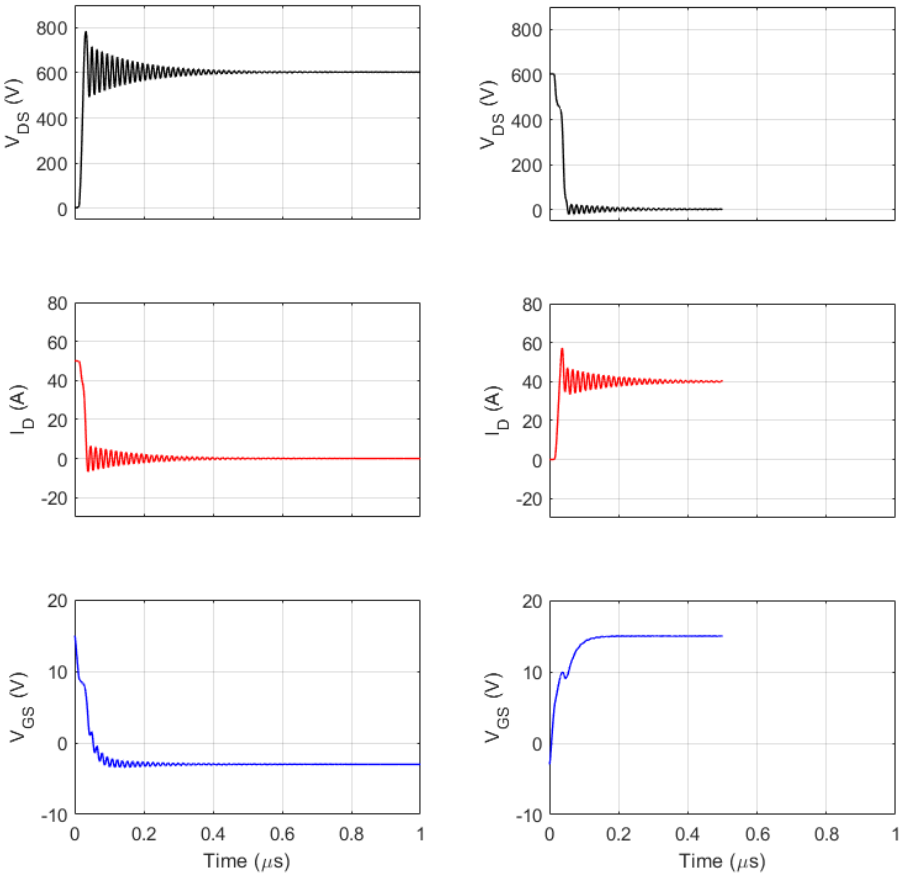


Figure 3.5: Transconductance Extraction



(a) overall **(b)** turn-off **(c)** turn-on

Figure 3.6: Experimental Switching Behavior



(a) turn-off **(b)** turn-on

Figure 3.7: Simulated Switching Behavior

Chapter 4

Integration of the High-Fidelity MOSFET Model

This chapter presented a two-stage integration framework for combining circuit-level simulations with high-fidelity MOSFET transients. By isolating and refining local switching events, the method balances computational speed and accuracy, making it suitable for design and validation for EMI-sensitive applications and loss assessment.

4.1 Two-Stage Simulation Framework

The simulation process is divided into two stages:

1. **Circuit-Level Simulation**
    - Run the circuit simulation using ideal switch models (e.g., binary resistor model).
    - Record all relevant node voltages and branch currents over time.
    - Identify switching instants for each MOSFET from gate signals or current/voltage transitions.
2. **High-Fidelity Switching Transient Simulation**
    - For each identified switching event, extract the pre-transition circuit conditions.
    - Use these values as boundary conditions to initialize the high-fidelity MOSFET model.
    - Simulate the switching event over a short window to recover accurate $V_{DS}(t)$ and $I_D(t)$ waveforms.

4.2 Stage 1: Ideal Switch Simulation

The converter circuit is first modeled using the methods described in Chapter 2, with MOSFETs replaced by ideal switches. Using MNA and time discretization, the circuit is solved over the full time horizon.

Record values of the relevant circuit variables, and each switch's on/off state determined by gate signals.

4.3 Stage 2: High-Fidelity MOSFET Transient Simulation

4.3.1 Switching Condition Determination

The transient MOSFET model discussed in Chapter 3 is developed for the case of complementary conduction of the upper and lower switches in a half-bridge structure. It takes into account the dead time and the reverse recovery current of the diode. Since the modeling simplifies each bridge leg into an active switch and a freewheeling diode, it is necessary not only to determine the switching state of each MOSFET, but also to identify whether it is an active or inactive turn-on/off event.

For the active switch, the corresponding simulation is performed based on its switching state. For the inactive switch, the drain-source voltage (V_{DS}) and drain current (I_D) are obtained by subtracting the results of the complementary switch from the DC bus voltage (V_{DC}) and inductor current (I_L), respectively.

Figure 4.1 illustrates all possible cases with switching conditions marked by the corresponding switches. Below is a flowchart illustrating the simulation process.

4.3.2 Initial Conditions Extraction

- Load current through the inductor or MOSFET.
- Voltage across the MOSFET terminals (drain-source, gate-source).

These variables are used to set the initial conditions for transient simulation.

4.3.3 Local Device Simulation

The extracted conditions serve as inputs to the high-fidelity model described in Chapter 3. A standalone simulation is performed for each switching event using a fine timestep (e.g., nanoseconds). Figure 4.3 demonstrates a single switch V_{DS} waveform during switching transitions. The data was recorded for 0.02 seconds and to avoid over lapping only the transition dynamics are captured.

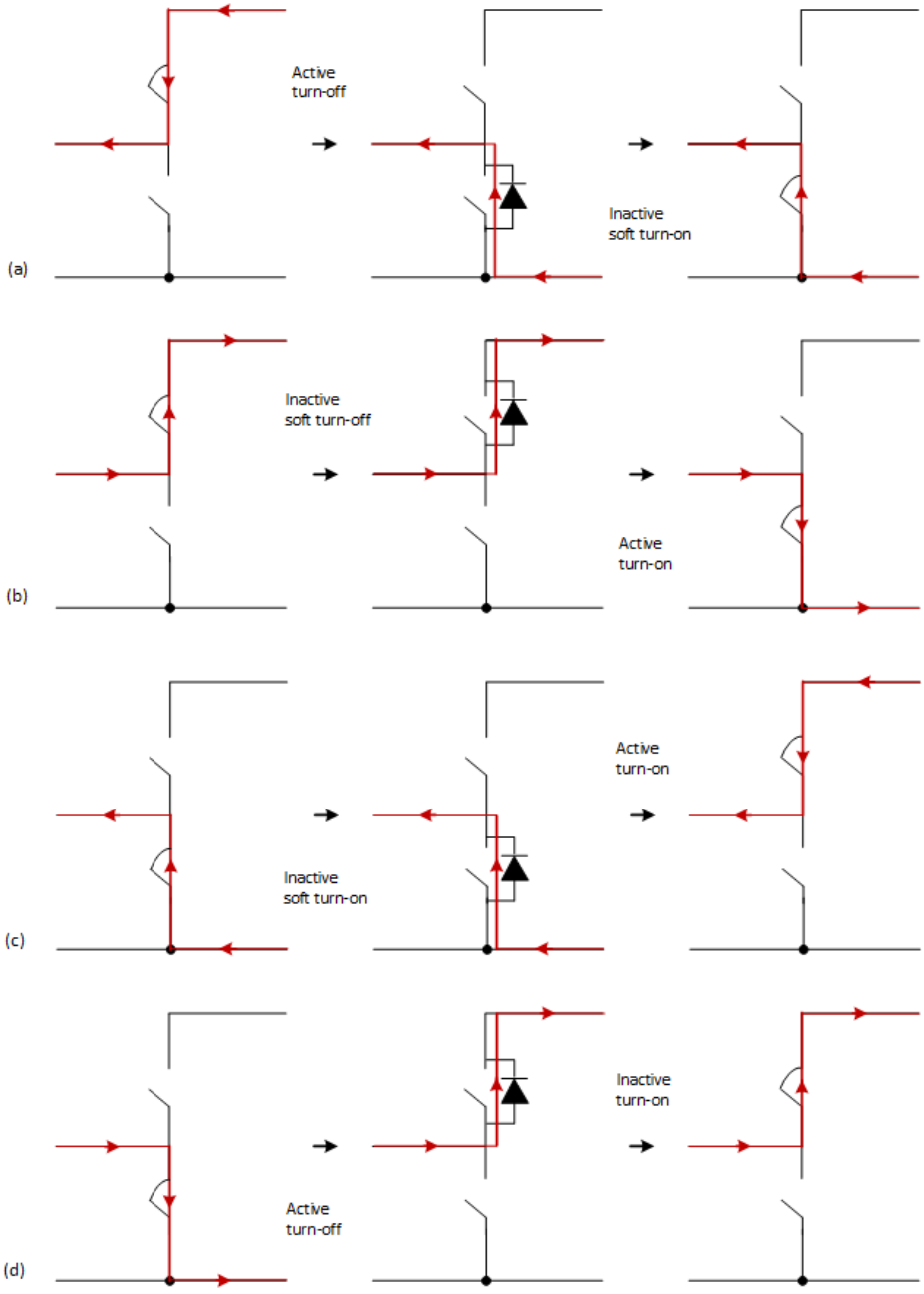


Figure 4.1: Switching Condition Determination

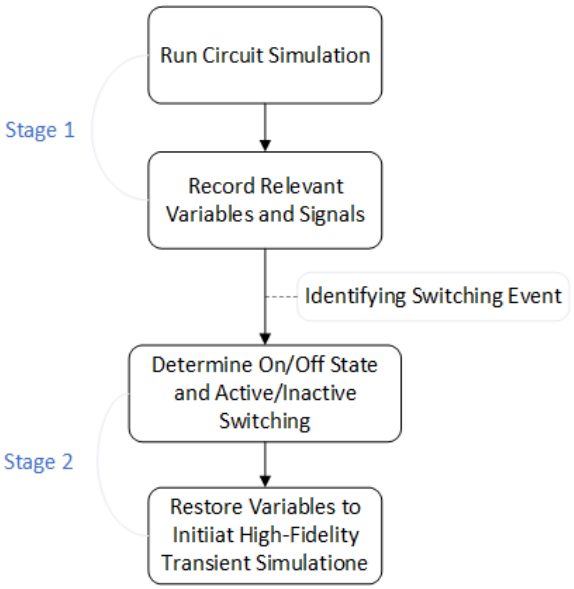


Figure 4.2: Simulation Process Flow Chart

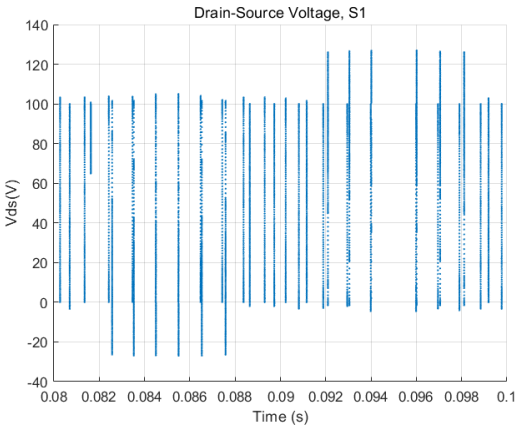


Figure 4.3: V_{DS} during Switching Transition

4.4 Advantages and Limitations

4.4.1 Advantages

- **Speed**: Main simulation runs with fast ideal switches.
- **Accuracy**: Local switching waveforms reflect physical device behavior.
- **Modularity**: Transient modeling is decoupled from circuit topology.

4.4.2 Limitations

- Transient effects do not feed back into main simulation. The two simulations are decoupled.

Chapter 5

Conclusion

5.1 Summary of Contributions

This project has successfully developed a modular simulation framework that balances computational speed and modeling accuracy for power electronic systems:

- Generalized Circuit Modeling: A robust MNA-and-discretization approach enables automatic construction and solution of circuit equations with both linear and nonlinear elements.
- High-Fidelity MOSFET Model: A physics-based device representation captures gate dynamics, parasitic capacitances and inductances, and diode recovery effects, validated by experimental double-pulse tests.
- Two-Stage Integration: The proposed decoupling of system-level and device-level simulations achieves fast execution with ideal switches, then refines switching events locally to recover detailed waveforms without full-system computational burden.

5.2 Key Findings

- The discretization-based MNA model matches traditional continuous and discrete solvers in accuracy but requires further optimization to reduce computation time for long simulations.
- The MOSFET model reproduces critical transient phenomena (overshoot, oscillations) within experimental tolerances, demonstrating its potential for EMI and loss assessments.
- The two-stage framework effectively balancing the computational cost and accuracy, preserving system-level performance metrics while providing device-level insights in a time-efficient manner.

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The high-fidelity MOSFET transient model and corresponding code were originally developed by Peng Xue.

ChatGPT was used for assistance with code generation and debugging, and thesis revision.

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Appendix A

Code and Simulation Files

Due to potential future updates, please visit the GitHub repository below for the latest code:

https://github.com/vectors-1/Digital-Modeling-of-Power-Electronics-System-Circuit-Simulator-