Advanecd Power Cycling test of SiC MOSFET Power Modules

MSc. Thesis

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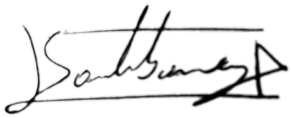

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Abstract:

In recent years, Wide Band Gap devices, such as SiC and GaN, have emerged as a promising technology, showing advantages in efficiency, speed, and thermal dissipation. However, despite their benefits, mass adoption is challenged by the reliability concerns still present in these technologies. Addressing the reliability of SiC MOSFET is crucial for their adoption in industrial applications, and one key methodology to achieve this is power cycling tests. This thesis focuses on how to perform Power Cycling Tests on SiC MOSFET Power Modules by adapting an existing test platform capable of performing DC and AC Power Cycle Tests. The laboratory work is conducted on a test setup at AAU that has been used to perform DC and AC power cycle tests on IGBT modules. An adapter PCB is designed to incorporate half-bridge SiC MOSFET power modules to the test setup, and DC and AC power cycle tests are performed. Problems were detected in relation to the on-state voltage measurement of the switches, and the origin is the faster switching of the MOSFETs causing EMI issues. The test results show differences in the temperature profiles of the DC and AC versions of the power cycling test. Moreover, there are differences in the rate of change of the temperature, showing a more aggressive temperature rise on the DC version. The results of the DC power cycling test show bond wire lift-off is present, and it can be seen on the on-state voltage reading as a fast rises or jumps in voltage.

Summary

In recent years, Wide Band Gap devices, such as SiC and GaN, have emerged as a promising technology, showing advantages in efficiency, speed, and thermal dissipation. These features, among others, position these devices as a promising replacement to traditional Si power semiconductors, especially in military, automotive, and high-demanding industry applications where reliability is fundamental. However, despite their advantages, mass adoption is challenged by the reliability concerns still present in these technologies. Addressing the reliability of SiC MOSFET, and Wide Band Gap devices in general, is crucial for their adoption in industrial applications, and to harness the benefits they offer.

One method to evaluate the reliability of semiconductors is Power Cycling Testing, where repeated heating and cooling is applied to the device, and are appropriate to evaluate degradation related to thermo-mechanical fatigue. The DC Power Cycling Test creates a thermal cycle by applying a DC current and generating conduction losses on the device. It is a well understood method, and its implementation does not involve a switching scheme like SPWM, facilitating the process. This test can apply thermal cycles and trigger the degradation and ageing mentioned before, but it does not represent the switching behaviour of the device, and thus it does not represent its real operation in the field. In contrast, the AC power cycle test is an alternative method where the device switching is involved. This type of test is considered closer to the field operation of the device, and is preferred because of this reason. As this test involve switching, its implementation is more complex, typically requiring a switching algorithm and different topologies, depending on the test conditions.

This thesis focuses on power cycling tests of SiC MOSFET power modules, and it is center around the following problem:

How to perform Power Cycling Tests on SiC MOSFET Power Modules by adapting an existing test platform capable of performing DC and AC Power Cycle Tests

The laboratory work is conducted on a test setup at AAU that has been used to perform DC and AC power cycle tests on IGBT modules.

An adapter PCB is designed to incorporate half-bridge SiC MOSFET power modules to the test setup, and DC and AC power cycle tests are performed. Problems were detected in relation to the on-state voltage measurement of the switches, and the origin is the faster switching of the MOSFETs causing EMI interference. The problem is diagnosed at the communication with the ADC responsible of performing the reading, and possible solutions are explored.

The test results show differences in the temperature profiles of the DC and AC versions of the power cycling test. The waveform of the current and the thermal impedance affect the final temperature profile of the junction temperature. Moreover, there are differences in the rate of change of the temperature, showing a more aggressive temperature rise on the DC version. This

behaviour can deviate from the real life behaviour in some applications like motor drives, where a sinusoidal current creates a slower rise in temperature.

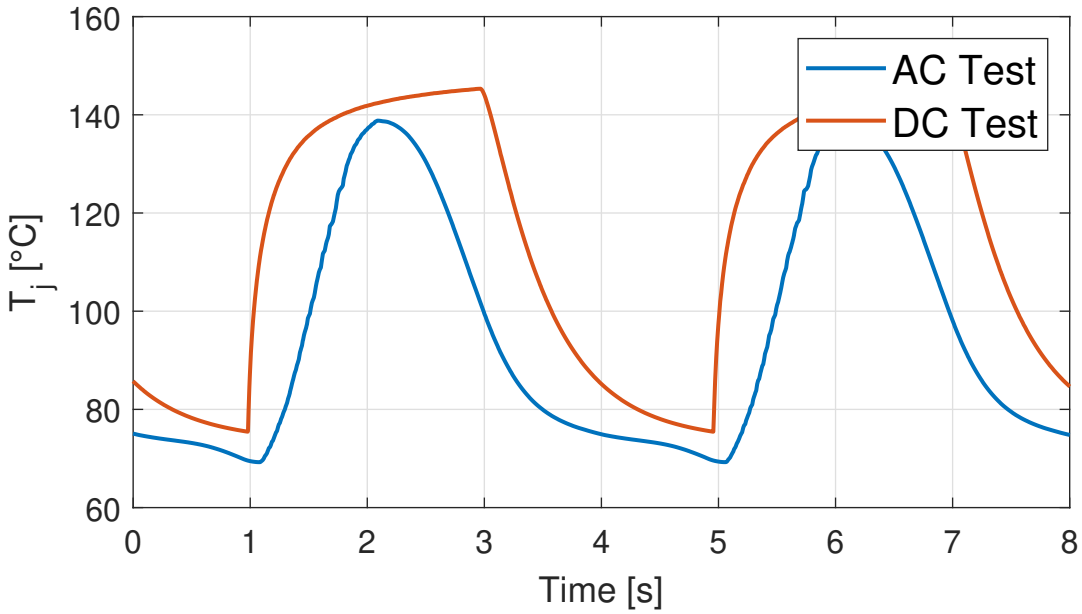


Figure 1 Temperature profile for the AC and DC test.

The results of the DC power cycling test show degradation of the packaging. In particular, bond wire lift-off is present, and it can be seen on the on-state voltage reading as a fast rise and sudden jumps in voltage.

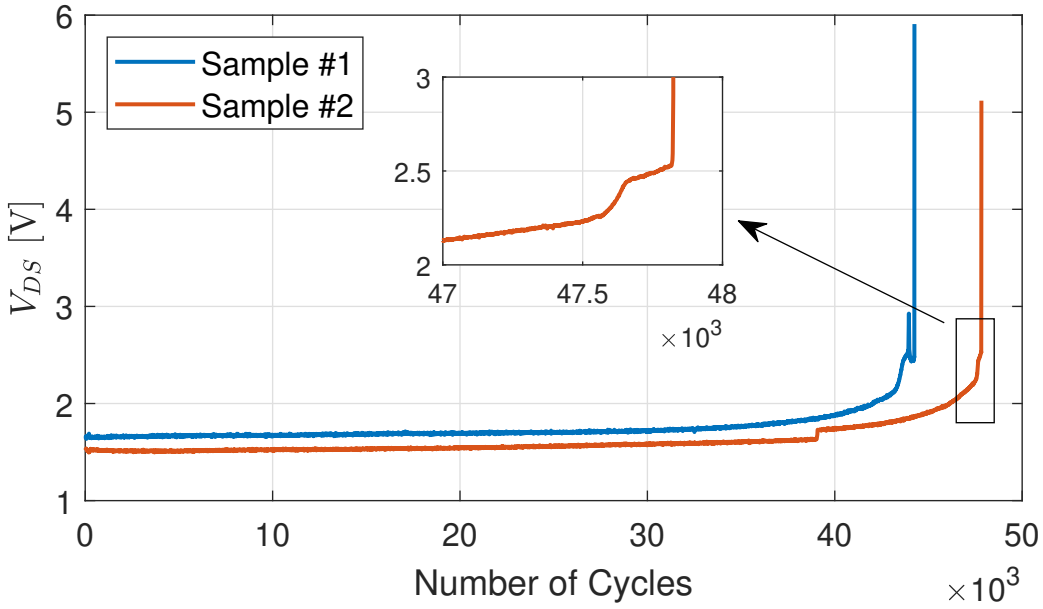


Figure 2 On-state voltage vs. number of cycles for both switches.

Contents

1 Introduction

This chapter introduces power cycling of SiC MOSFETs as the main topic of the thesis. It shows Wide Band Gap devices as a growing technology, and it introduces the problem formulation.

1.1 Power Electronics and Their Applications

Power electronics is a branch of electrical engineering focused on the conversion and control of electrical energy. Semiconductor devices, such as diodes and transistors, are used for this purpose and convert the input energy into a suitable form for the load. They are used in many applications, from tens to hundreds of watts in phone chargers and computer power supplies, to kilowatts in industrial applications and electric vehicles[1].

Power electronics play a critical role in energy infrastructure, industrial automation, transport, and many other areas of society. Inverters are present in electric vehicles, wind power generators, and solar farms, and they transform a DC input voltage into a controllable AC output voltage. Rectifiers are used in electronic equipment to rectify the AC input voltage to a stable DC output.

Wide Band Gap devices have become popular due to their advantages in thermal conductivity and power losses, when compared to Si devices. SiC and GaN are the most mature alternatives to replace Si in the near future[2]. SiC presents a higher breakdown field compared to Si, which allows higher voltage ratings. Its higher thermal conductivity also improves thermal performance. These attributes make SiC suitable to be used in automotive, military applications, and other high-demanding situations where the reliability requirements are high. However, despite their advantages, mass adoption is challenged by the reliability concerns still present in these technology. Addressing the reliability of SiC MOSFET, and Wide Band Gap devices in general, is crucial for their adoption in industrial applications.

1.2 Reliability of SiC MOSFET Power Modules

The most important challenge to reliability of WBG device packaging is fatigue at high temperatures, caused by a mismatch of the coefficient of thermal expansion of the materials used. This induces thermo-mechanical fatigue in solder, substrate, and in the bond wires. Thermal cycling is one of the main causes of failures on WBG devices, both at the chip and packaging level[3].

During operation, condition monitoring is used to detect changes on certain parameters of the semiconductor devices related to their degradation and possible failure. Preventive measurements and maintenance can be done to avoid critical failures or excessive down time[3]. A deep knowledge of the failure mechanisms of the device is required for proper monitoring. Junction temperature and on-state resistance are some of the parameters that can be used to monitor the degradation state of the devices[4]. Accelerated testing is a key method to properly

understand different failure mechanisms and how they manifest.

Accelerated Lifetime Tests are a crucial tool to analyse failure modes and ageing mechanisms, and they are used to evaluate the reliability of products. Power Cycling Tests apply a temperature swing to the device, and are appropriate to evaluate degradation related to CTE mismatch, mainly package-related degradation, such as bond wire lift-off and solder fatigue. The DC Power Cycling Test creates a thermal cycle by applying a DC current and generating conduction losses on the device. It is a well understood method, and its implementation does not involve a switching scheme like SPWM, facilitating the process This test can apply thermal cycles and trigger the degradation mentioned before, but it does not represent the switching behaviour of the device, and thus it does not represent its real operation in the field [5]. In contrast, the AC power cycle test is an alternative method where the device switching is involved. These type of test is considered closer to the field operation of the device, and is preferred because of this reason. As this test involve switching, its implementation is more complex, typically requiring a switching algorithm and different topologies, depending on the test conditions[4].

1.3 Problem Formulation

SiC MOSFETs are one of the key technologies that are enabling better performance and higher efficiency in power electronics applications. Given their importance and their current development, there are key concerns on the reliability and degradation mechanisms of this devices. To investigate this topic, the following problem is formulated:

How to perform Power Cycling Tests on SiC MOSFET Power Modules by adapting an existing test platform capable of performing DC and AC Power Cycle Tests

This problem is further explored by the following objectives:

- Understanding the role of power electronics in electric motor and drive systems.
- Identify the changes needed and upgrade an existing AC power cycling setup designed for IGBTs, so that it can be used for SiC MOSFETs.
- Analyse the test results and compare the behaviour of DC power cycling and AC power cycling.

With the problem statement clearly defined, the next chapter discusses the background needed to understand how SiC MOSFETs operate and how they are tested.

2 Background

This chapter introduces the reliability of SiC MOSFETs as a key concern for their adoption as an alternative to Si devices. The degradation and failure mechanisms are presented, and power cycling is introduced as one of the testing methods used to evaluate the lifetime and reliability of semiconductors. The chapter also exposes the behaviour of MOSFETs, and how their power losses create the thermal stresses that ultimately lead to degradation over their lifetime. It finalises with an introduction of the testing setup available at AAU, which is used during this project.

2.1 Semiconductor Reliability

The reliability of power semiconductors is a key aspect in their adoption, and it is still a concern in industrial applications, as well as in academia. Power semiconductor failure can represent over 50 % of converter failures in industry[6]. It is therefore important to understand and evaluate the reliability of SiC MOSFETs, to inform future designs and improve their performance and longevity, ultimately encouraging their adoption.

The reliability of a product can be defined as *the probability that an item will perform a required function,without failure, under stated conditions for a defined period of time*[7]. Testing is a key part of product development, and reliability testing evaluates that a product or design will operate during its lifetime without failure. Power cycle testing is a key method to asses the reliability of semiconductor devices and to predict their lifetime.

2.1.1 Thermal Cycles and Degradation

During a power cycling test, the device is subject to repeated heating and cooling cycles, through the application of electrical power. The temperature cycle amplitude and the maximum temperature reached are selected to accelerate the degradation that would happen during the device normal operation. The testing process involves constant monitoring of the device temperature and degradation parameters. It is also necessary to define an end of life criteria, to decide when a product fails during testing. A common failure criteria for MOSFETs is an increase of 5 % in the on-state voltage of the semiconductor.

The repeated heating and cooling creates thermo-mechanical stress caused by the thermal expansion of the materials that form the device. As different materials present different coeficcients of thermal expansion, the difference in expansion creates a mechanical stress that leads to material fatigue.

2.2 Failure Mechanisms in SiC MOSFETs

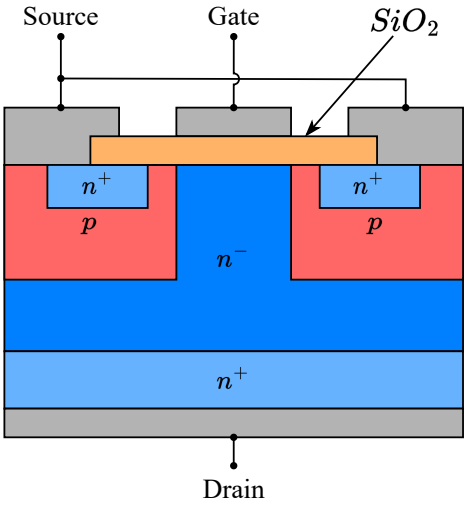
The degradation and failure of SiC MOSFETs manifest in different ways, depending on the origin of the failure. An understanding of the failure mechanisms and how they appear is a key

part of the testing process, as it allows to isolate and study a single failure mechanism during testing. It also allows the monitoring of key parameters that can inform when a device is close to failure, which is helpful in some contexts, for example, in maintenance scheduling.

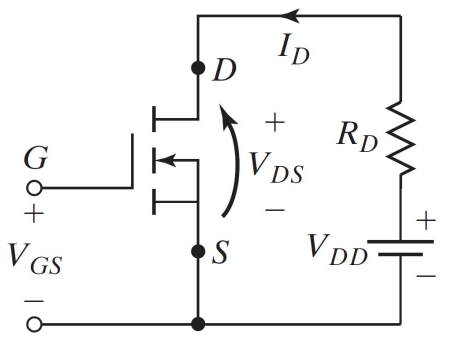
The failures of SiC MOSFETs can be classified in two groups: failures of the electronic chip or die, and failures of the packaging. The MOSFET is constructed as a chip or die, and consists of different layers of semiconductor material. To understand chip failures, the structure and operation of the power MOSFET are explained.

2.2.1 Working principle of the MOSFET

The MOSFET is characterised by the Drain, Source, and Gate terminals. The Drain and Souce are considered the power terminals, while the Gate receives the control signal.



(a) Cross section of an n-channel Power MOSFET



(b) MOSFET symbol in a reference circuit.

Figure 2.1 Construction of a MOSFET and its electrical symbol [8].

The Power MOSFET is constructed in layers of semiconductor material. The Drain terminal is placed at the bottom, after which layers of semiconductor material are placed as shown in Figure 2.9. The Source and the Gate are placed at the top. The Gate is isolated from the Source and the semiconductor layers by an oxide layer (SiO_2). Between the Source and the Drain, there are regions of n-type and p-type semiconductor[8].

When a positive voltage is applied between the Gate and the Source terminals, a channel forms between the Drain and the Source, connecting the n-regions and allowing current to flow. The voltage applied between the Gate and the Source needs to be above the Threshold Voltage for the channel to form. Between the Drain and the Source there is a pn junction, responsible for the voltage blocking capability of the switch, and forming the Body Diode. When a negative voltage is applied between the Drain and the Source, and is greater than the forward bias voltage of the pn junction, this Body Diode section conducts current in the opposite direction (from Source to Drain)[8].

The MOSFET is not an ideal switch, thus, the switching process is not instant and energy is

dissipated each time the switch turns on or off. When an external voltage is applied between the Gate and the Source, the voltage between these terminals raises according to the parasitic capacitance and resistance between them. This behaviour causes a delay from the moment the voltage is applied, and the moment the internal Gate-Source voltage reaches the Threshold voltage. After V_{GS} surpasses V_{Th}, the Drain current I_D raises to the load current, and the Drain-Source voltage V_{DS} drops to the on-state voltage.

When the MOSFET is on, there are conduction losses generated along the current path. These losses are often characterised by the drain-to-source resistance $R_{DS,ON}$, which is a parameter included in the datasheet of MOSFETs. R_{DS_ON} depends on the Gate-Source voltage applied, and can be considered as:

$$R_{DS\_ON} = \frac{1}{2K\left(V_{GS} - V_{Th}\right)} \tag{2.1}$$

where K is a constant that depends on the geometry and material of the MOSFET. This relationship is valid for $0 < V_{DS} < V_{GS} - V_{Th}$ [8]. A higher Gate-Source voltage reduces R_{DS_ON} and the conduction losses.

2.2.2 Chip Failures

Threshold voltage instability refers to the change of the threshold voltage with ageing, caused by gate oxide degradation. A change in the threshold voltage changes the conduction losses during normal operation, since R_{DS_ON} depends on $V_{GS} - V_{Th}$. This can result in higher power losses and higher temperature swings, which accelerates the degradation of the device. The intrinsic body diode of the MOSFET can be subject to degradation when it is used to fly-back the load current. The transient current degrades the switch, increasing the power losses[2].

2.2.3 Packaging Failures

The semiconductor die has to be packaged to protect it from the environment, to provide the necessary electrical connections, and to provide means for heat dissipation, which is often done by mounting the switch to a heatsink. The packaging introduces elements that are also subject to thermal stresses, and can degrade and eventually fail. Thus, it is also relevant to understand how the MOSFET is packaged, and how the packaging can degrade over time.

The packaging of the power chip includes a substrate, solder, a base plate, a heatsink, bond wires, and encapsulation. The materials used have different coefficients of thermal expansion (CTE), and expand and contract at different rates during the temperature cycles present in on-site use. This behaviour results in thermo-machanical fatigue[2].

Repetitive thermal cycles cause mechanical fatigue in bond wires, leading to cracks that can potentially result in lift-off. In the same manner, cracks and voids can form in the solder layers, causing delamination and an increase in thermal resistance. The mismatch of CTEs causes mechanical stress on the ceramic substrate, leading to cracks that worsen the thermal

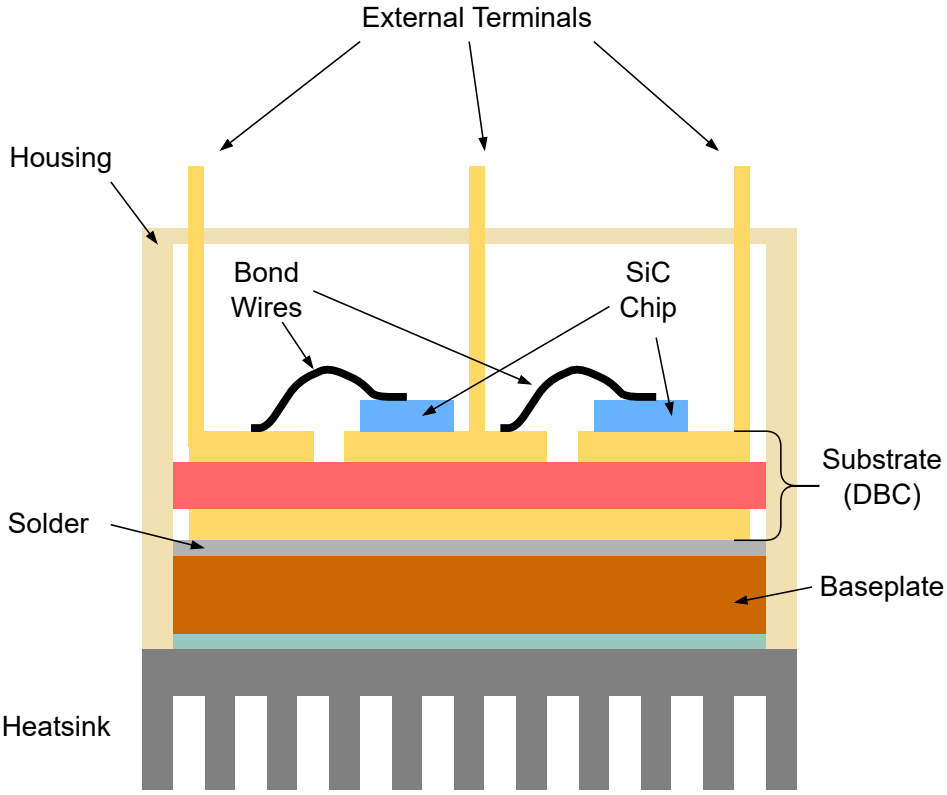


Figure 2.2 Schematic of a power module packaging[2].

conduction of the material.

Degradation of the bond wires results in higher electrical resistance between the Drain and the Source terminals. Since the bond wires connect the Source terminal of the MOSFET die to the rest of the circuit, this manifests in an increase of the on-state resistance. On the other hand, degradation of the solder layer or the ceramic substrate results in an increase in the thermal resistance between the chips and the heatsink. This results in higher temperatures on the chip for the same level of power losses[2][3].

2.3 Power Losses and Thermal Behaviour

As explained in previous sections, the thermal stresses on the device lead to degradation at different levels. This stresses are often produced by the power losses in the device itself, and depend on the operating conditions of the device. It is therefore important to understand how the power losses are generated, and how they relate to the different use cases of the device.

During operation, the MOSFET generates conduction losses and switching losses. The internal resistance between Drain and Source when the switch is conducting ($R_{DS,ON}$) is responsible for the conduction losses:

$$P_{cond} = I^2 \cdot R_{DS\_ON} \tag{2.2}$$

The switching losses account for the energy dissipated in the turn on and tun off processes, and depends on the switching frequency f_{sw}:

$$P_{sw} = (E_{ON} + E_{OFF}) \frac{V}{V_0} \frac{I}{I_0} f_{sw} \tag{2.3}$$

E_{ON} and E_{OFF} are the turn on and turn off energy at a specific voltage V_0 and current I_0, and V and I are the operating voltage and current.

The total power losses P_{Loss} are then the sum of conduction and switching losses, and depend on the current, the voltage, and the switching frequency:

$$P_{Loss} = P_{cond} + P_{sw} = I^2 \cdot R_{DS\_ON} + (E_{ON} + E_{OFF}) \frac{V}{V_0} \frac{I}{I_0} f_{sw} \tag{2.4}$$

When a MOSFET operates with time-changing power losses, its junction temperature does not follow the changes in power immediately. The temperature responds slowly due to the thermal inertia of the device, which comes from its thermal resistance and capacity. Understanding the thermal behaviour of the MOSFET is important to understand the thermal stresses that arise during its field operation and during power cycle testing.

During normal operation, the switch generates heat through its power losses, raising its temperature. The dissipation of this heat through a heatsink can be modelled by an Foster network, as depicted below. This network represents the thermal path of the generated heat, from the junction to the heatsink[9][10].

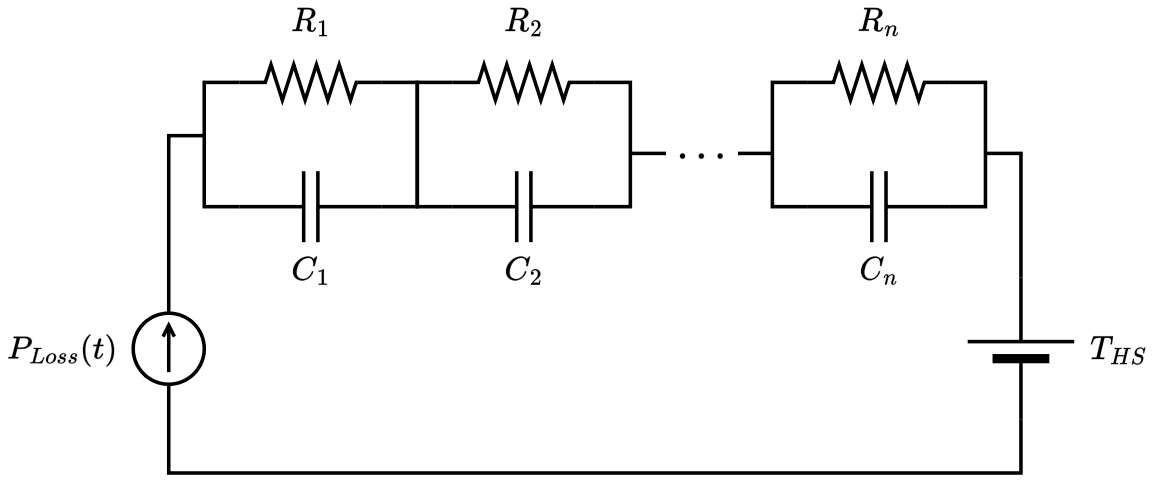


Figure 2.3 Generic Foster network.

The thermal resistance and capacity of the system causes the temperature to respond gradually to fast changes in power losses, and effectively acts as a low-pass filter The junction temperature of the switch can be calculated based on the power losses and the thermal impedance between the junction and the heatink. The thermal impedance between the junction and the heatsink is expressed in Equation 2.5 for a Foster model of n stages[10].

$$Z_{(t)} = \sum_{i=1}^{n} R_i \cdot \left(1 - e^{-t/\tau_i}\right) \tag{2.5}$$

Each stage of the network contributes a thermal resistance R_i and a time constant $\tau_i = R_i C_i$. Experimental data can be fitted to the model by recording the junction temperature response to a step in power losses. The junction temperature $T_j(t)$ can be calculated using the following equation[10]:

$$T_j(t) = T_{HS} + \int_0^t P_{Loss}(\tau) h(t-\tau) d\tau \tag{2.6}$$

where T_{HS} is the heatsink temperature, $P_{Loss}(t)$ is the power loss, and $h(t)$ is the thermal impulse response given by:

$$h(t) = \sum_{i=1}^{n} \frac{R_i}{\tau_i} e^{-t/\tau_i} \tag{2.7}$$

2.4 AAU Laboratory Setup

This project is conducted in a test setup developed at AAU, as part of the X-POWER reliability testing laboratory. In this section, the laboratory setup is introduced, to bring context to the project, and to illustrate the operation and capabilities of the setup.

The laboratory setup consists of two 2-level 3-phase DCAC converters connected in a back-to-back configuration. A simplified schematic of the system is shown in Figure 2.4.

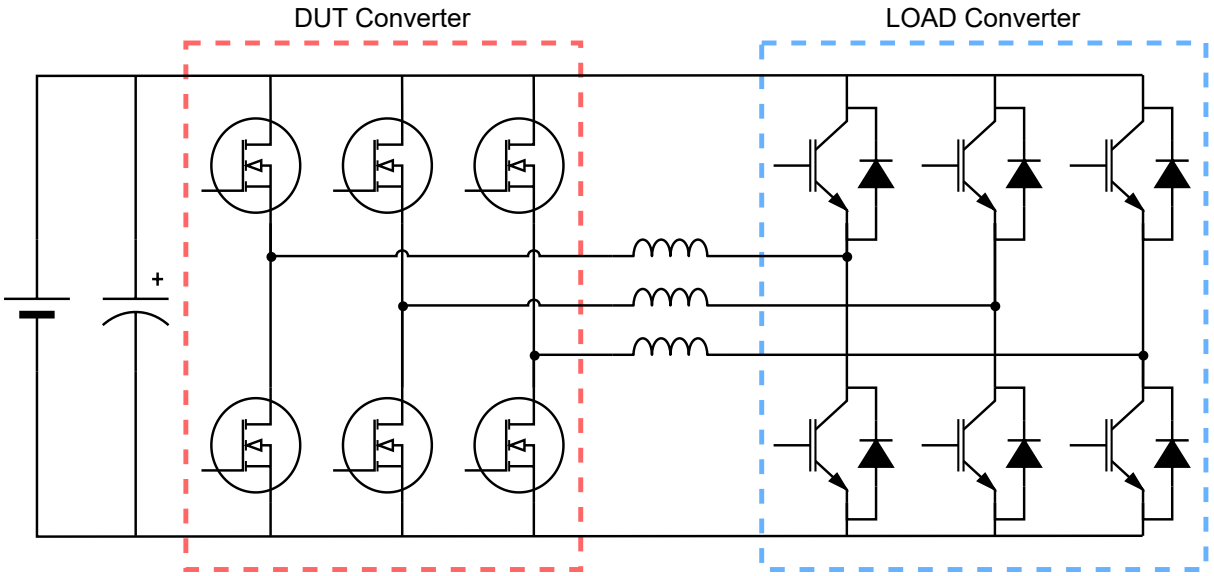


Figure 2.4 Simplified schematic of the two converters in a back-to-back configuration.

The test setup is custom built, and the main sections are two converters: the Load Converter, which consists of Si IGBTs, and the DUT Converter, which consists of the devices under test (DUTs). The DC sides of both converters are connected in parallel and are fed by an adjustable DC power supply. Capacitors are also included in the DC link, and the AC sides are connected by either bus bars or an inductive load, depending on the configuration of the system. This layout can also be analysed as three full bridge inverters, and it is possible to only use one phase to perform a test. Each converter has a separate cooling system, where the DUT heatsink temperature can be adjusted to different setpoints as needed.

The system is constructed in a modular fashion as depicted in Figure 2.5, and consists of different PCBs that are connected together. Two identical Main PCBs, one for each converter, house the gate driver circuits and on-state voltage measurements. The DUT PCB contains the devices that are tested, and it is redesigned based on the specific semiconductors used. The junction temperature of each device is registered by optical fibers, placed directly on top of each semiconductor die. The NI cRIO FPGA system and LabView software control the whole system, including instrument control, converter control, and safety measures. Details of the test setup can be found in [11], where the system has been validated for Si IGBT tests in AC and DC power cycle mode.

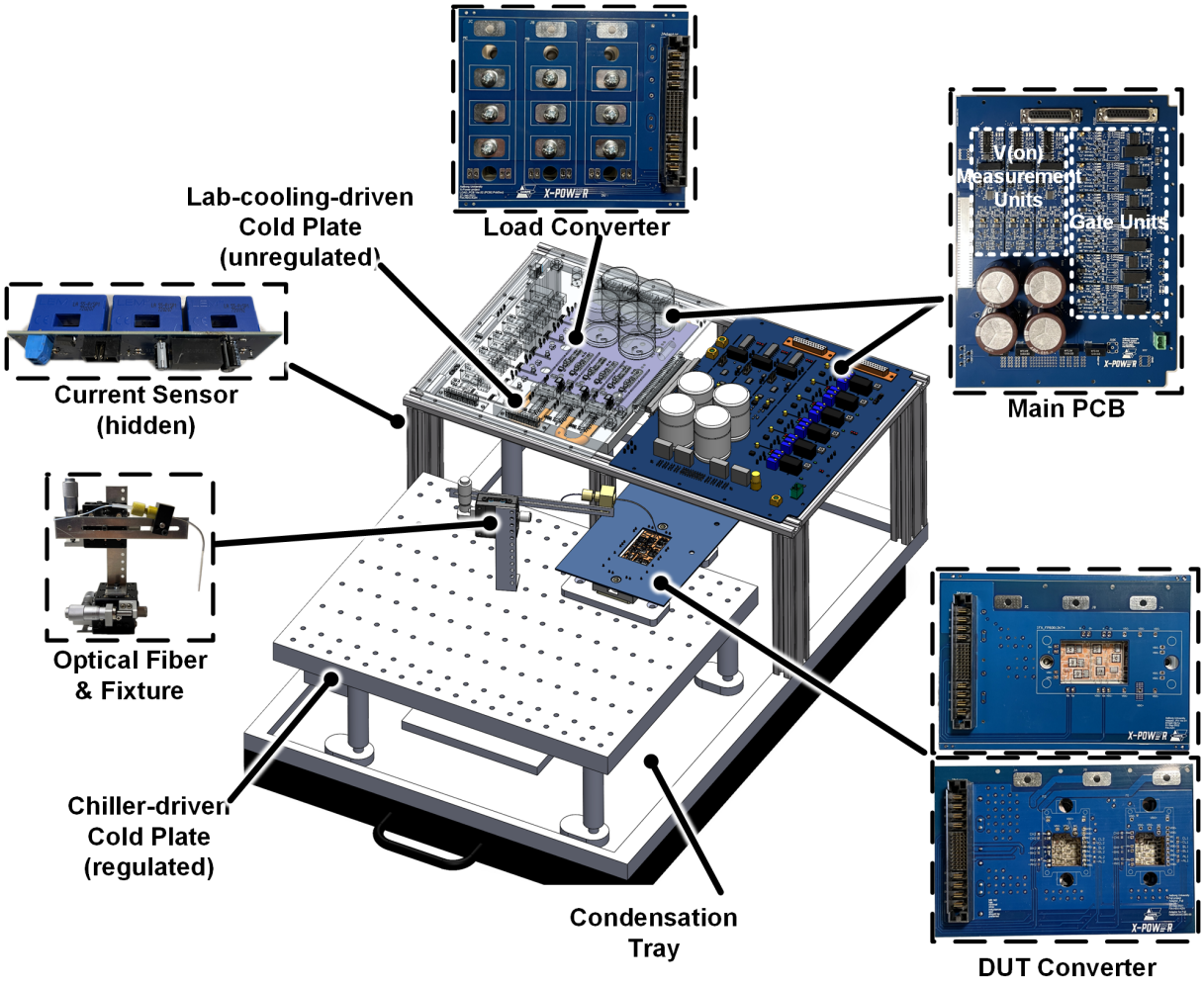


Figure 2.5 Test setup used[11].

2.4.1 Main PCB

The Main PCB is shown in Figure 2.6, and houses six gate driver circuits, one for each of the semiconductor devices of one of the converters. These gate drivers can be adjusted to provide different on and off voltages and accommodate different DUTs. The on-state voltage measurement is implemented by the circuit found in the referenced patent (cite patent). This circuit measures the voltage between the Drain and the Source pins of the high-side switch and the low-side switch, and has been proven to achieve an accuracy on the 10 mV scale. Instrument amplifiers are used to preserve the voltage reading, and one ADC IC circuit is used after the amplifier circuits to read their output voltage. Finally, an optocoupler is placed between the ADC and the NI cRIO interface to provide electrical isolation.

2.4.2 DUT PCB

The DUT PCB is designed to include the devices that will be tested. For this project, three SiC MOSFET half-bridge modules are used to form the 3-phase ACDC converter. The design of the Adapter PCB can be seen in Figure 2.7.

The PCB receives the gate signals from the corresponding Main PCB, and connects the Drain and Source of each switch to the measuring circuits. To record the junction temperature, an optical fiber is placed on the semiconductor die of each switch, and thus a cut-out is included on the PCB on the location of each die. The modules tested are manufactured in a plastic housing filled with gel, and part of the plastic housing is removed to place the optic fibers. The DUTs are attached to a specially design cooling plate, connected to an adjustable cooler that controls and maintains the cooling plate temperature at a fixed value throughout the test.

2.4.3 Adaptation for SiC Testing

The adaptation of the test setup for SiC MOSFET testing involves the following aspects:

1. Gate driver compatibility
2. Measurements required
3. Load capabilities

The gate driver circuits have to be able to operate the SiC MOSFETs successfully, and to the desired conditions, primarily, on and off gate voltages, gate currents, and switching frequency. The setup needs to perform the required measurements during the test, which are the on-state voltage, load current, and junction temperature through the optical fiber. The specific hardware design and integration steps are detailed in Chapter 3. Finally, the test setup has to sustain the required load current needed to achieve the desired test conditions, both in DC and AC power cycling.

2.5 SiC MOSFET Module

The power module used is the SEMIKRON SK40MB120CR03TE1 SiC Half-Bridge Power Module. It presents voltage and current ratings of 1.2 kV and 49 A respectively. The module

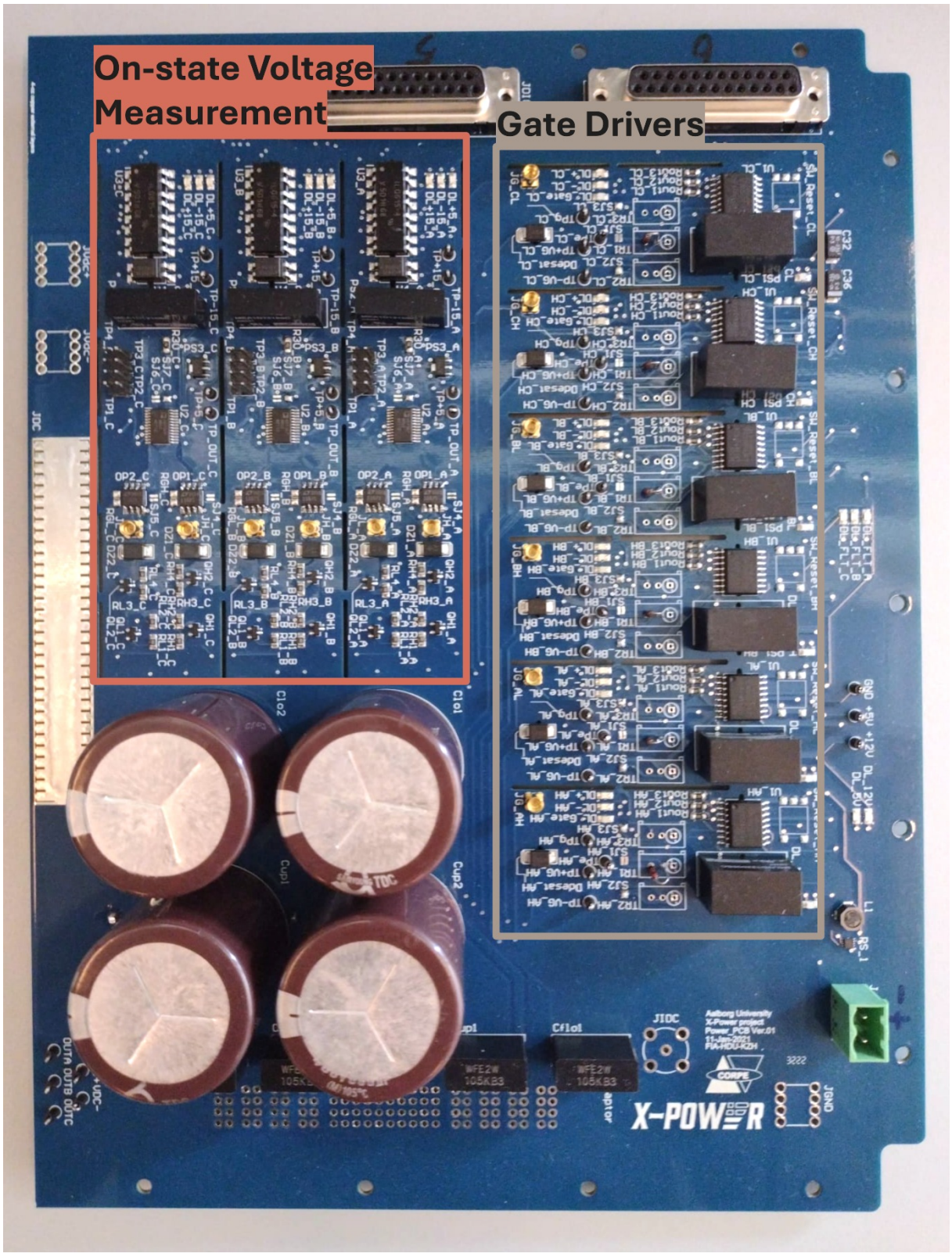


Figure 2.6 Main PCB used in the test setup.

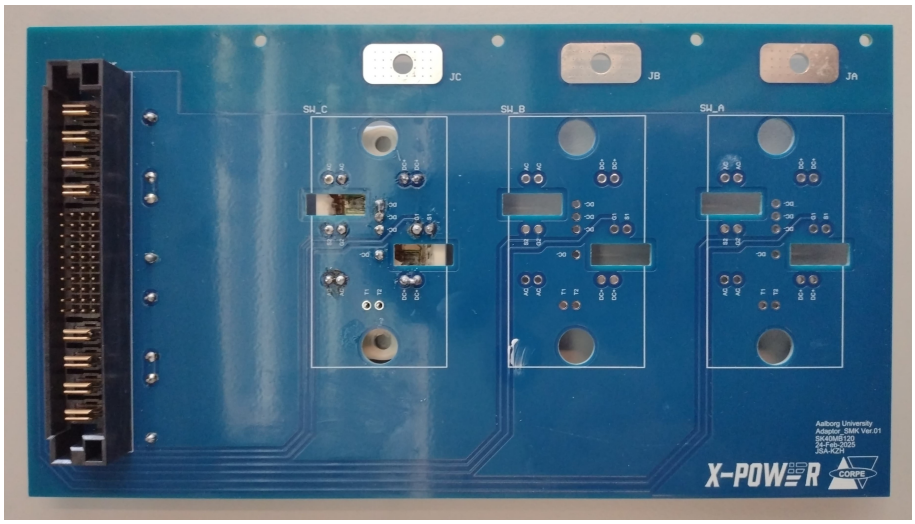
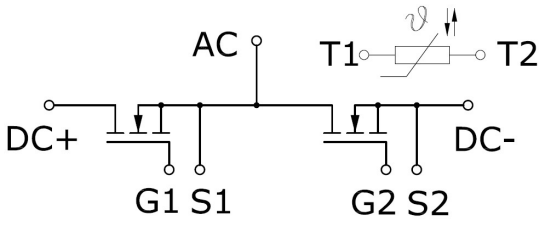


Figure 2.7 Adapter PCB.

includes Kelvin Source pins for each switch and an integrated NTC temperature sensor. The module presents a rising and falling time of 16 ns and 23 ns, respectively, and the recommended turn-off/turn-on gate voltages are −4 V and 15 V.

(a) MOSFET modules used as DUT.



(b) Module schematic, including Kelvin Source pins (S1 and S2), and the NTC temperature sensor.

Figure 2.8 MOSFET module and corresponding schematic showing the connection of the two switches

2.6 Simulation of the System

The testing setup is simulated to evaluate the testing conditions. SEMIKRON provides the thermal library of the Half-Bridge module for PLECS, which includes several look-up tables for different Gate-Source voltages and gate resistors, load currents and DC voltages. This library also includes the thermal network that characterises the thermal response of the module.

2.6.1 DC Power Cycle Test

The DCPC test is simulated using one of the phases of the setup. The circuit considered is shown in Figure 2.10. The goal of the test is to apply a temperature swing dT and a maximum junction temperature $\hat{T}_j$ through the power losses of the device. The coolant temperature is held constant, and therefore, the temperature swing is caused only by the power losses.

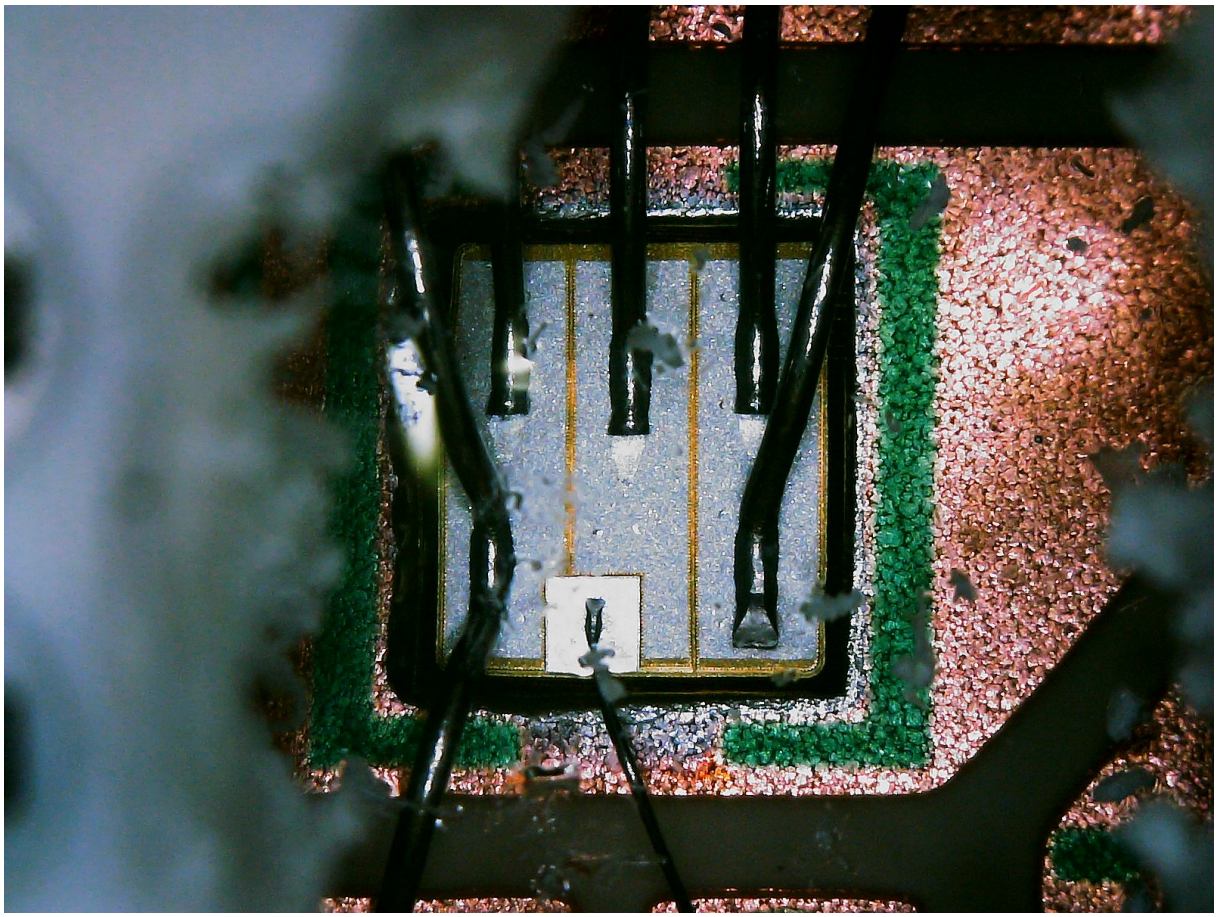


Figure 2.9 Photo of one of the MOSFETs of the power module.

The heatsink temperature is calculated as:

$$T_{HS} = \hat{T}_j - \Delta T \tag{2.8}$$

Since this is a DCPC test, only conduction losses in the semiconductor are considered, and thus, the temperature swing is calculated as:

$$\Delta T = P_{Loss} R_{Th} = I_D^2 R_{DS\_ON} R_{Th} \tag{2.9}$$

where R_{Th} is the thermal resistance between the junction and the heatsink, and R_{DS_ON} is the on-state resistance of the MOSFET. Solving for the Drain current I_D:

$$I_D = \sqrt{\frac{\Delta T}{R_{DS\_ON} R_{Th}}} \tag{2.10}$$

This equation shows that the Drain current depends on the desired temperature swing, the on-state resistance, and the thermal resistance between the junction and the heatsink. This last

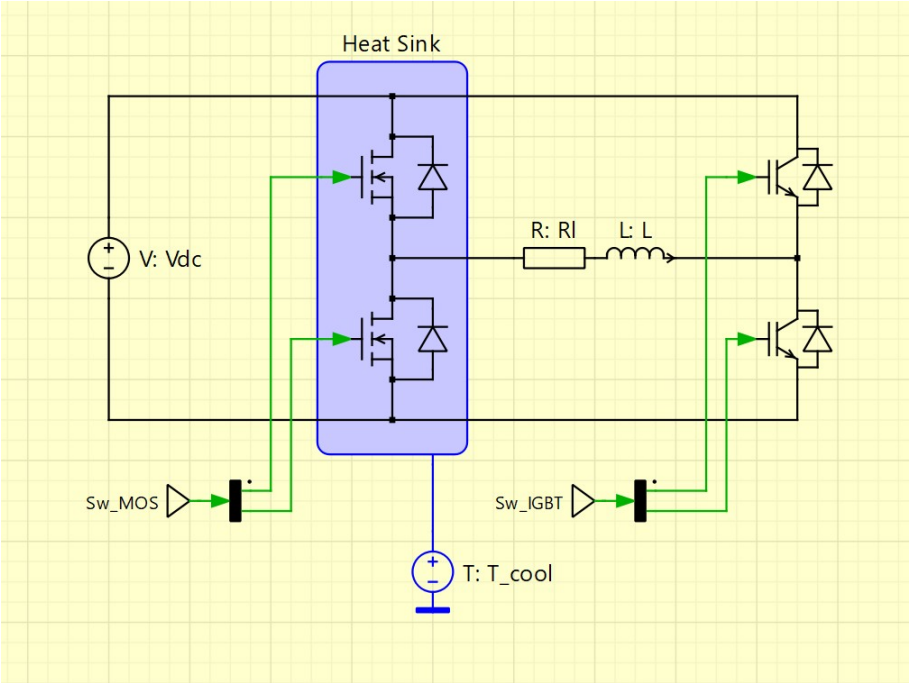


Figure 2.10 Test circuit simulated for the DCPC test.

parameter depends heavily on the specific test setup, specifically on how the device is mounted to the heatsink, and the Thermal Interface Material used.

From this calculations, the heatsink temperature and the load current are adjusted to achieve the desired test conditions in terms of ΔT and $\hat{T}_j$

From the datasheeet of the module, R_{DS_ON} has a value of 50 $m\Omega$, and the thermal resistance is specified as 1.2 K/W when using the SEMIKRON proprietary thermal paste. The necessary load current and heatsink temperature are calculated for a ΔT of 70 K and $\hat{T}_j$ of 150 °C.

$$T_{HS} = \hat{T}_j - \Delta T = 150 - 70 = 80°\text{C} \tag{2.11}$$

$$I_D = \sqrt{\frac{\Delta T}{R_{DS\_ON} R_{Th}}} = \sqrt{\frac{70}{0.050 \cdot 1.02}} \approx 37.05\text{A} \tag{2.12}$$

The calculated load current depends on the thermal resistance between the junction and the heatsink, and the value provided by the manufacturer is used as a first approximation. The thermal paste and mounting method that is used in the laboratory is not the same as the ones used by the manufacturer when characterising the module, therefore, there is high uncertainty on the real thermal resistance of the test setup. Based on this fact, the values calculated above are used as a reference, and fine tuning of the heatsink temperature and load current on the setup itself is needed to obtain a specific ΔT and $\hat{T}_j$

The calculated conditions are used in simulation, where the thermal model of the SiC MOSFETs used is provided by the manufacturer on their website.

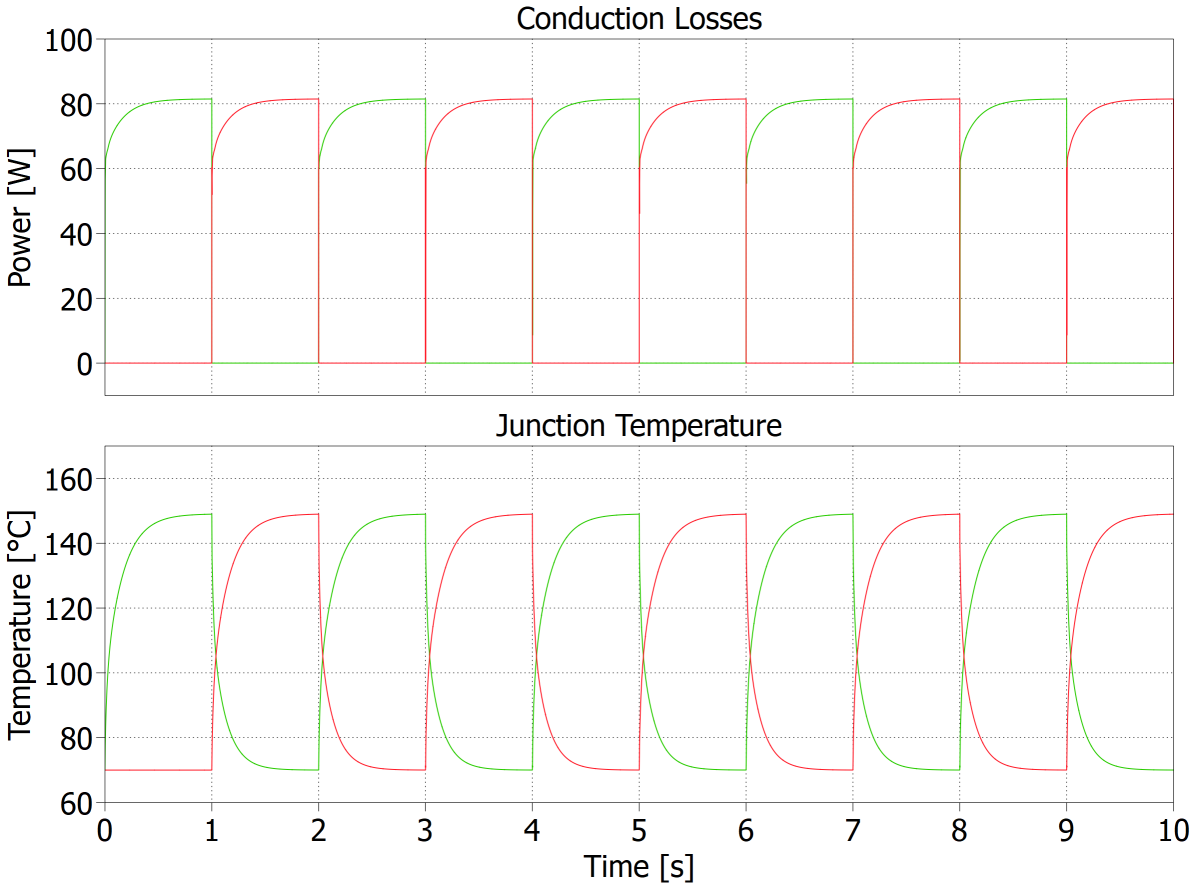


Figure 2.11 Conduction losses and junction temperature for the upper switch (green) and lower switch (red) of the half Bridge module.

The on and off times considered in the simulation are 1 s each, which allows the devices to reach the maximum and minimum temperature. The simulation shows that the desired test conditions are achievable for a current of 40 A, which is within the capabilities of the test setup and is below the maximum current of the SiC module. As explained before, this result assumes the conditions specified by the manufacturer, this is, using their proprietary thermal paste. If a different product is used, the thermal resistance may change, and the load current has to be adjusted accordingly.

In this chapter, the laboratory setup has been introduced, as well as the specific SiC MOSFET module to be tested. The necessary changes to the setup have been identified, and the simulation results show a starting point for the testing conditions. In the next chapter, the changes to the setup are addressed, including the hardware design and validation.

2.6.2 AC Power Cycle Test

In contrast to the previous case, during the AC power cycle test the switching losses also contribute to the device heating. To calculate the device switching losses, the switching energies from the device datasheet are used, following Equation 2.3. A DC-link voltage and peak current

of 400 V and 30 A are considered, respectively, and the switching frequency is 15 kHz.

$$P_{sw} = (E_{ON} + E_{OFF}) \frac{V}{V_0} \frac{I}{I_0} f_{sw} = (0.56 \cdot 10^{-3} + 0.35 \cdot 10^{-3}) \frac{400}{600} \frac{30}{40} 15 \cdot 10^3 = 6.825W \quad (2.13)$$

The conduction losses for the same conditions are 45 W.

The system is simulated in PLECS to evaluate the thermal response of the MOSFET. The peak current is 40 A and the DC-link voltage is 400 V

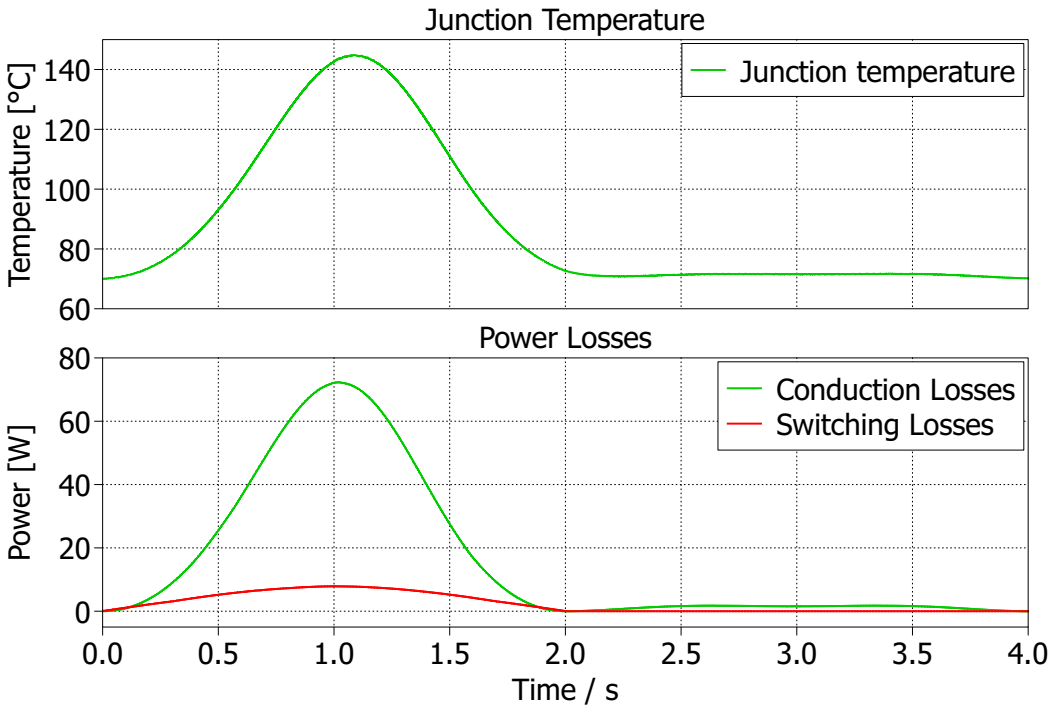


Figure 2.12 Junction temperature and power losses for the AC power cycle test simulation.

The temperature profile differs from the DC case, and a gradual increase and decrease in junction temperature is observed.

The behaviour of the MOSFET has been introduced, along with its failure mechanisms. The test setup has been presented, along with the devices considered for testing. Finally, simulation results of the system show differences between the DC and AC power cycle test in terms of the temperature profile. The next chapter explains the necessary hardware changes to the setup.

3 Changes to Hardware

This chapter discusses the changes to the hardware needed to adapt the test setup for SiC MOSFET testing. As discussed in the previous chapter, the on-state voltage measurement is one of the key variables to evaluate degradation of the device. The changes focus on the adapter PCB that connects the SiC MOSFETs to the rest of the system, and on the limitations and possible improvements to the on-state voltage measurement section.

3.1 Power Module Adapter Board

The modularity of the test setup facilitates the incorporation of new test subjects. To perform the power cycling tests, a new Adapter PCB needs to be designed to connect the SiC MOSFET modules to the setup.

The design of the PCB needs to fulfill some design criteria, both to operate successfully during the test, and to allow the required measurements to be perform throughout the test. Each MOSFET in the module requires a connection to the Gate and the Source for the control signals, a connection to the Drain and the Source for the on-state voltage measurement, and connections for the power inputs and outputs (VDC+, VDC-, and AC OUT terminals).

The modules use a press-fit connection, which require a dedicated tool to apply even and controlled pressure on the PCB during the mounting process. The design of the PCB follows the alternative method of through-hole soldering, and follows the manufacturer guidelines for the module in its application notes [12]. The dimensions used are shown in Figure 3.1.

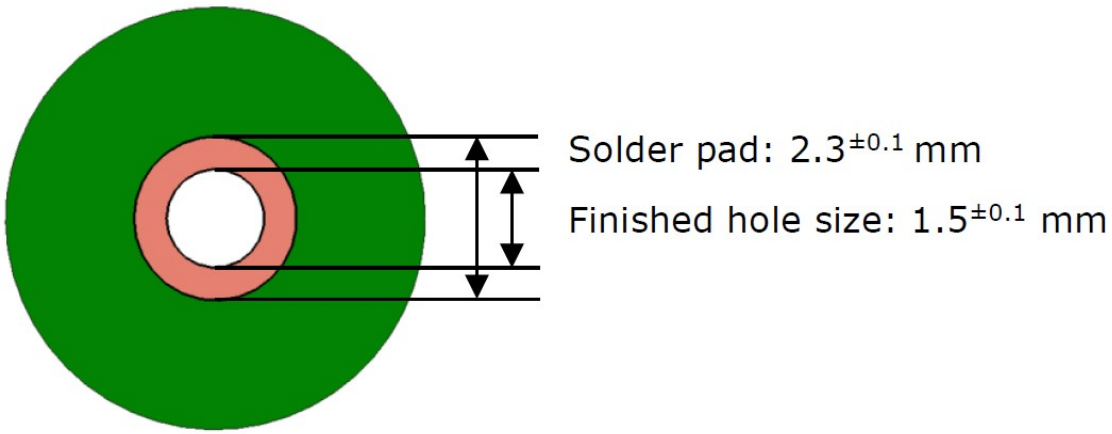


Figure 3.1 Specification of PTH for Press-fit module subject to soldering process[12].

The SAMTEC mixed connector provides a robust connection for the gate signals, the on-state voltage measurement signals, and the VDC+ and VDC- power connections. The AC outputs of the PCB are implemented as screw connections, in the same manner as previous design used in the setup. The design of the PCB incorporates cut-outs placed on the locations of each

MOSFET die, to place the optical fiber responsible of the junction temperature measurement.

The gate signals of each switch are routed maintaining the gate and source tracks as close as possible, placing one track on top of the other using adjacent layers. The power module has several pins for the power signals (DC+, DC- and AC), and the DC+ and DC- signals are connected through copper planes. One cut-out for each die is carefully placed to allow the optical fiber to be installed, while not compromising the mechanical integrity of the adjacent pins.

There are mechanical restrictions that limit the placement of the connector to the Main Board, and the terminals that connect to the AC load. The output terminals are placed to keep enough distance from the aluminium profiles where the system is mounted. The placement of the modules is not restricted in any significant way.

It is worth mentioning that the connection for the gate signals involves the gate and kelvin-source pins of each switch, and the tracks of these connection are routed as close as possible to minimize the loop inductance. The source connection for the V_{on} measurement uses a different track and uses the power-source pins.

The module is screwed to an aluminium block that is fixed to the heatsink, and thermal grease is used as interface. The heatsink is watercooled by an adjustable chiller, that keeps a constant set temperature.

The Adapter PCB is tested by applying the testing conditions of a DC power cycle test, with a current of 30 A, and the testing conditions of an AC power cycle test, with a DC-link voltage of 400 V and a peak current of 30 A. In both cases the DUTs behave correctly, and there are no issues related to the PCB. The placement of the optical fiber can be seen in Figure 3.4.

3.2 Gate Driver

The Main PCB includes 6 gate driver, which can be easily adapted to drive different semiconductors like IGBTs and MOSFETs.

The Infineon EiceDRIVER 1ED020I12-F2 single channel isolated gate driver is the IC implemented in the system. Its gate output signal can switch between $-12\,\mathrm{V}$ and $20\,\mathrm{V}$, depending on its power supply. The power supplies for the gate drivers are adjusted to $-5\,\mathrm{V}$ and $15\,\mathrm{V}$ to properly drive the newly incorporated SiC MOSFETs.

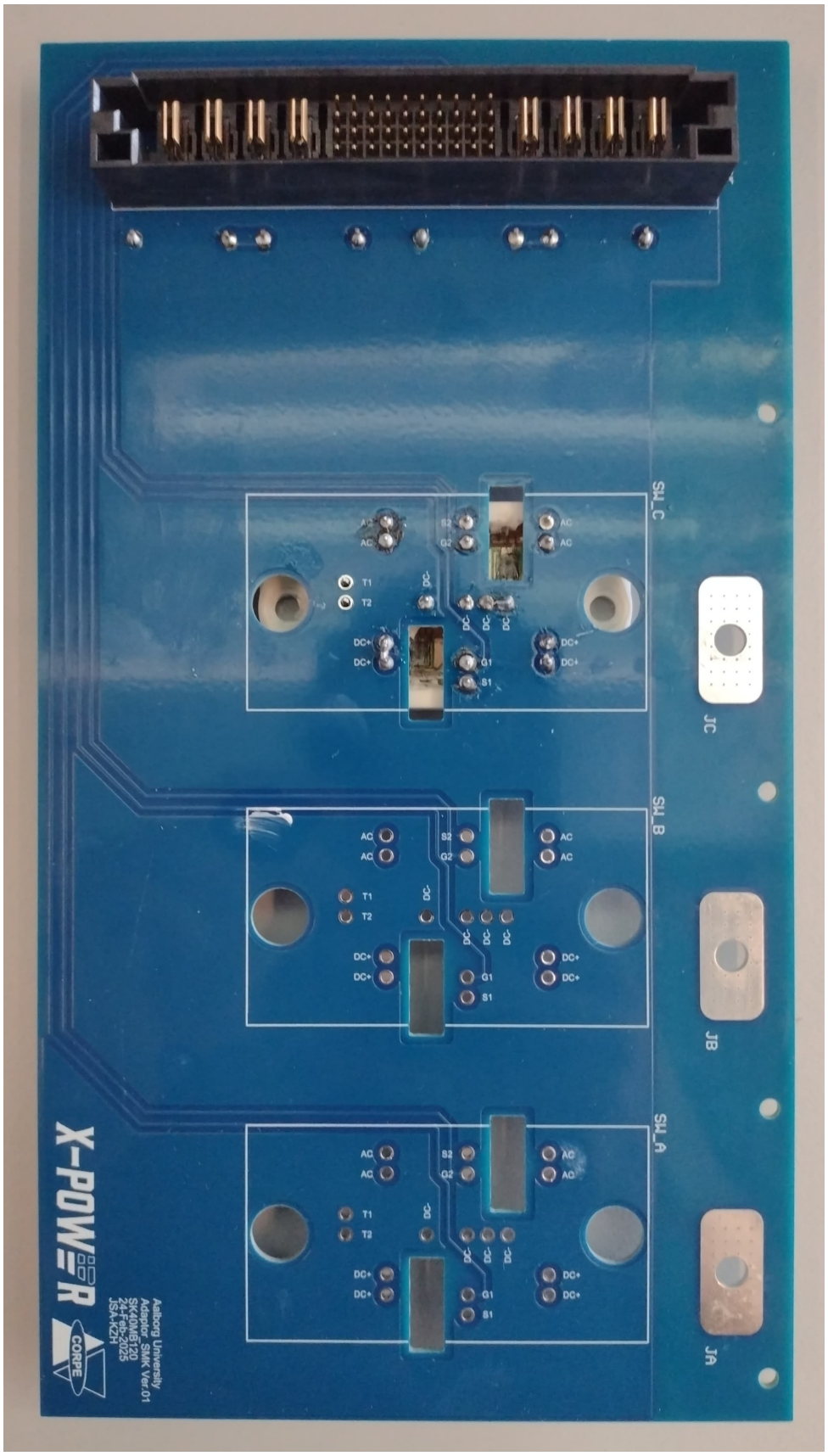


Figure 3.2 Adapter PCB with one Half-Bridge module included. The SAMTEC connector is at the top, and the AC output terminals are placed to the right.

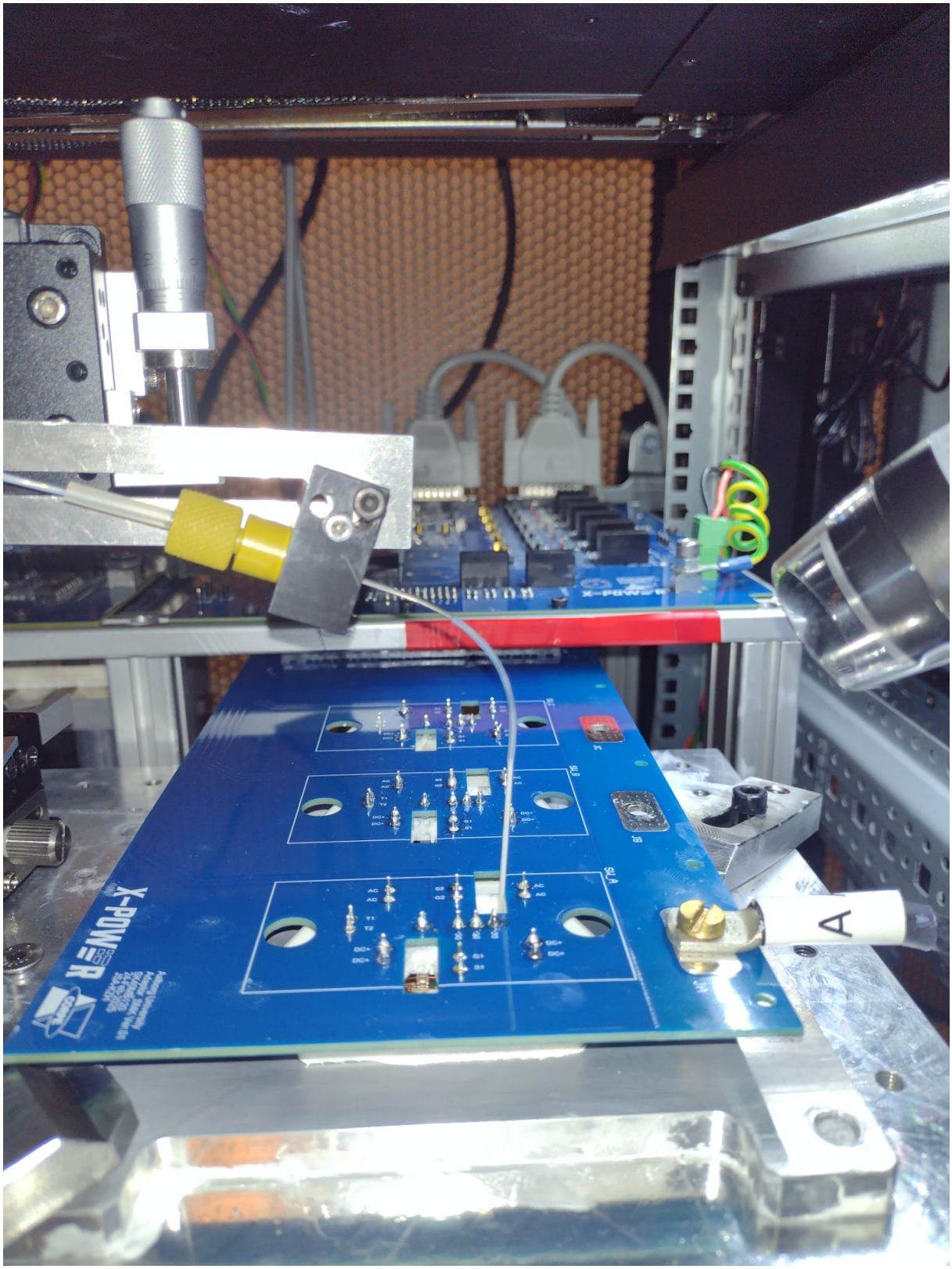


Figure 3.3 Adapter PCB installed in the test setup.

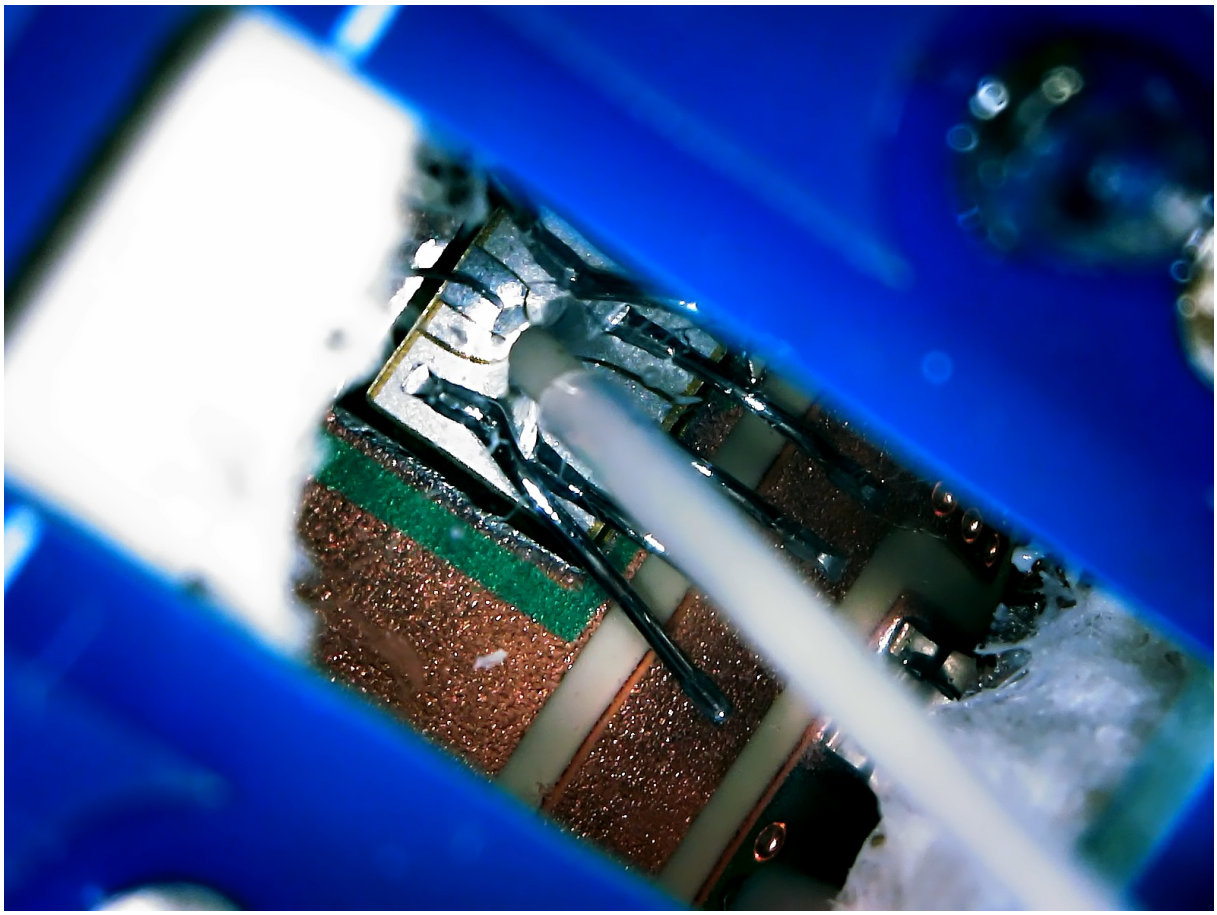


Figure 3.4 Placement of the optical fiber for temperature measurement.

3.3 On-State Voltage Measurement

The on-state voltage of the semiconductor switch is one of the variables used to evaluate degradation, and therefore it is crucial to measure it during the test in a precise and reliable manner. The inclusion of SiC MOSFETs as a test subject introduces changes in the system related to faster switching.

The current on-state voltage measurement solution is illustrated in Figure 3.6. The measurement circuit is shown in Figure 3.5, and is connected to the half-bridge module, and its output is fed to instrumentation amplifiers to maintain signal integrity. The ADC reads both voltages and feeds the data to the NI cRIO through the optocouplers. It is clear that an isolation stage is required, as the GND reference of the ADC and the amplifiers corresponds to the AC output of the module, which reaches the DC-link voltage.

The communication between the ADC and the FPGA is isolated by the optocouplers. These devices use an LED and a phototransistor to communicate a signal between two sides of the circuit without an electrical connection between them. Their response time is a limiting factor for a fast communication with the ADC, and can be a bottleneck when faster readings are required.

The on-state voltage reading presents an erratic behaviour when the ACPC test is attempted.

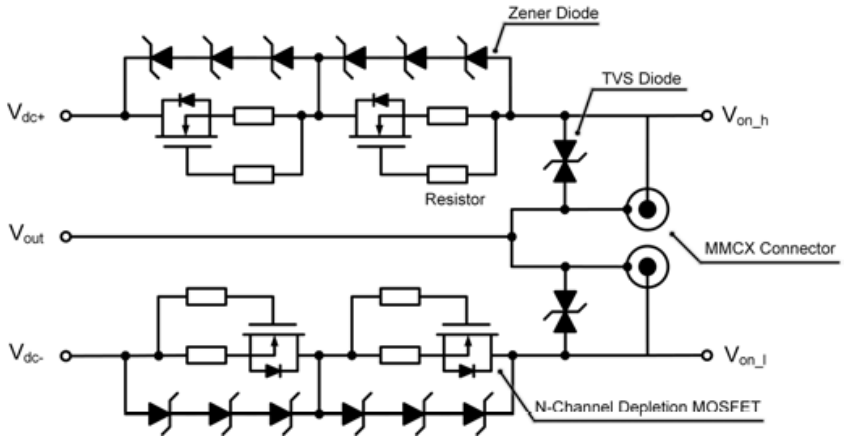


Figure 3.5 Measuring Circuit used in the Main PCB [11]

The voltage reading shows a value of 10 V after the DC-link voltage reaches 300 V. During testing, the analog section of the on-state voltage measurement has been tested, and there are no issues related to either the measuring circuit or the instrumentation amplifier. As the voltage reading corresponds to the maximum reading of the ADC, one possible cause is that the reading of the ADC is performed when the switch is off.

The inclusion of SiC MOSFETs creates a faster rising and falling voltage, which can compromise the communication between the ADC and the NI cRIO FPGA. To understand the problem in more detail, knowledge of the communication between the FPGA and the ADC is needed.

The AD7367 is a dual channel analog-to-digital converter, capable of a throughput data rate of up tu 1 MSPS. The two channels are used to read the on-state voltage of the upper and lower switch of the half-bridge. A serial interface is used to communicate with the ADC, and uses the following communication signals:

- CNVST (conversion start): The falling edge of this signal triggers the ADC sampling and conversion.
- BUSY: This signal goes high during conversion, and falls when the conversion is complete.
- SCLK (serial clock): Clock signal for reading the data.
- ADDR (address): this signal selects which channel to retrieve the data from.
- CS (chip select): Enables the serial interface.
- DOUT (data out): Serial data output.

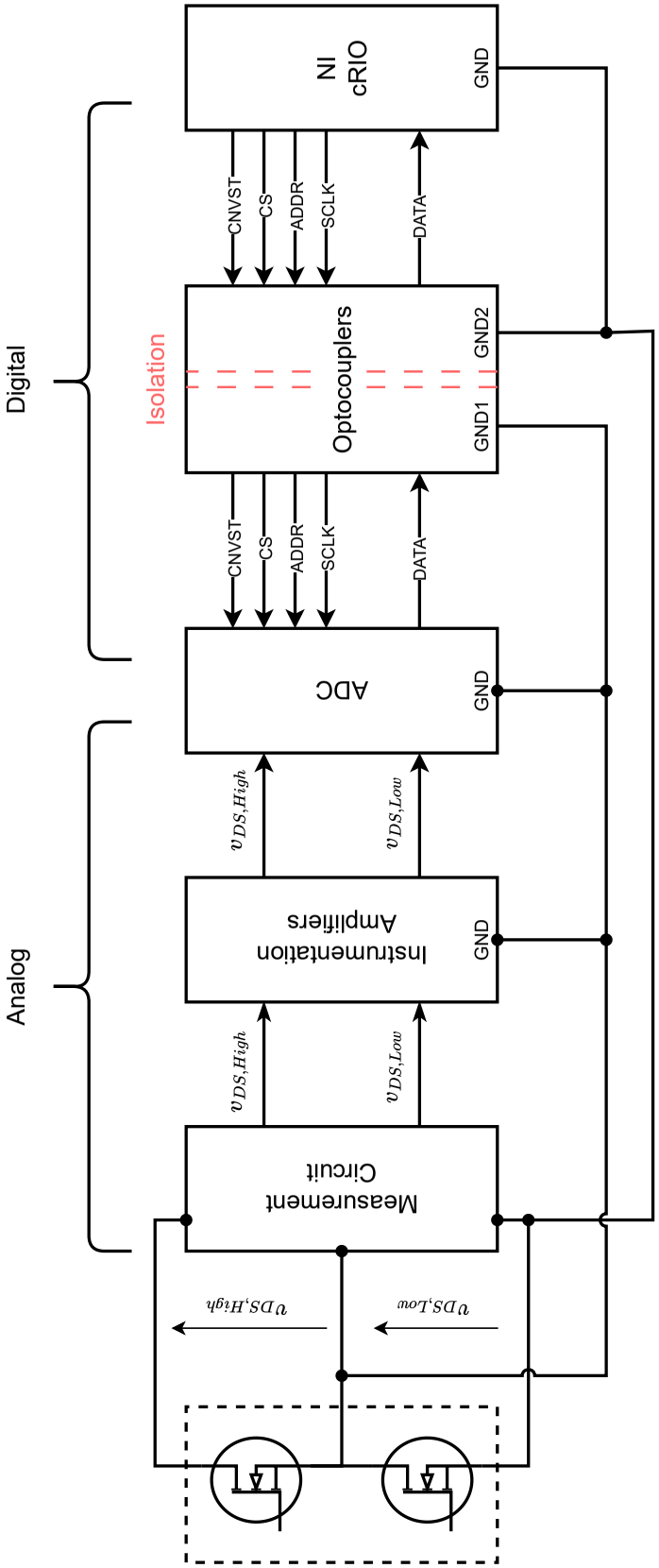


Figure 3.6 On-state voltage measurement sequence.

The communication signals are shown in Figure 3.7. The conversion process begins with the falling edge of the CNVST signal, which is controlled by the FPGA. The signal is held low for a minimum time t_1 of 10 ns. The conversion takes place during $t_{CONVERT}$, and the BUSY signal remains high during this time, which can be up to 680 ns according to the datasheet. After the conversion finishes, the CS signal is pulled low to initiate the serial read operation, where the SCLK signal is used to retrieve the data. A series of 14 clock pulses is send by the FPGA, and the data is read using the DOUT signal, on a MSB first sequence. After the data is read, and a minimum time of t_{QUIET} has passed, the ADC is ready for another sampling and conversion.

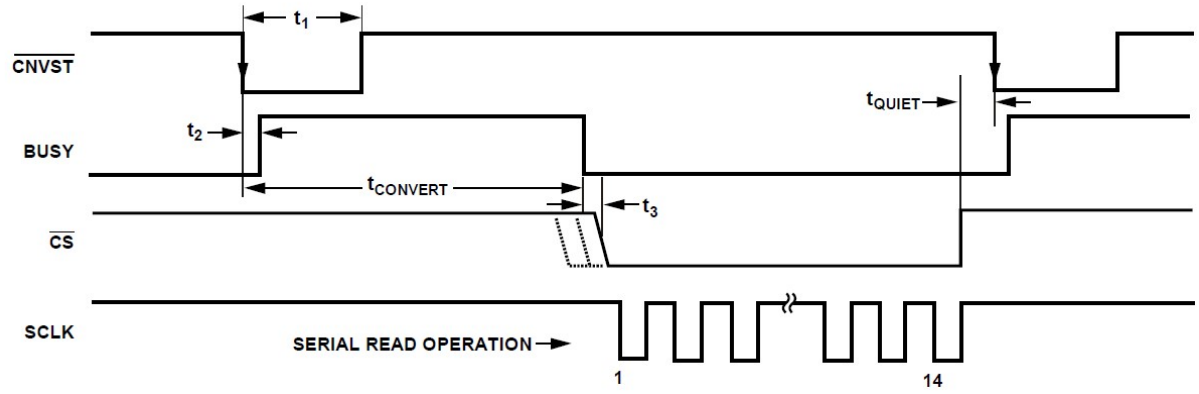


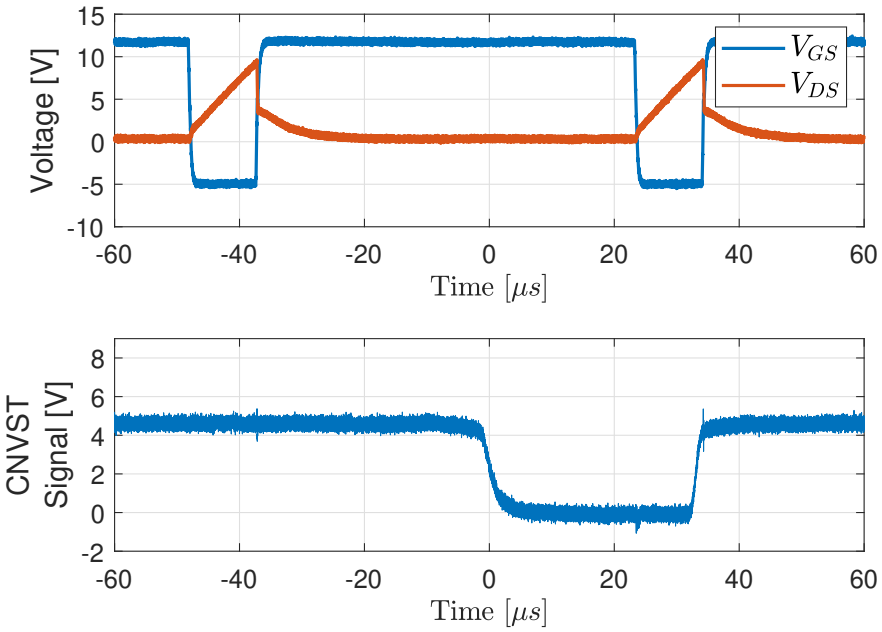
Figure 3.7 Signals during the serial communication of the ADC[13].

The CNVST signal is controlled by the FPGA, and it marks the moment when the ADC samples the signal. Coordination between this signal and the gate signal of the corresponding MOSFET is mandatory to ensure that the ADC samples the voltage when the switch is on. Noise in the signal can trigger a conversion when it is not needed, and read the voltage when the switch is off. The SCLK and DATA signals are responsible for the data reading after the conversion has taken place. The SCLK signal is driven by the FPGA, and consists of 14 pulses at a frequency between 10 kHz and 48 MHz. The DATA line is driven by the ADC, and it outputs the binary data to the FPGA with each pulse of the SCLK signal. The duration of the SCLK pulses determines the time the FPGA takes to read the data from the ADC: faster pulses allow faster readings.

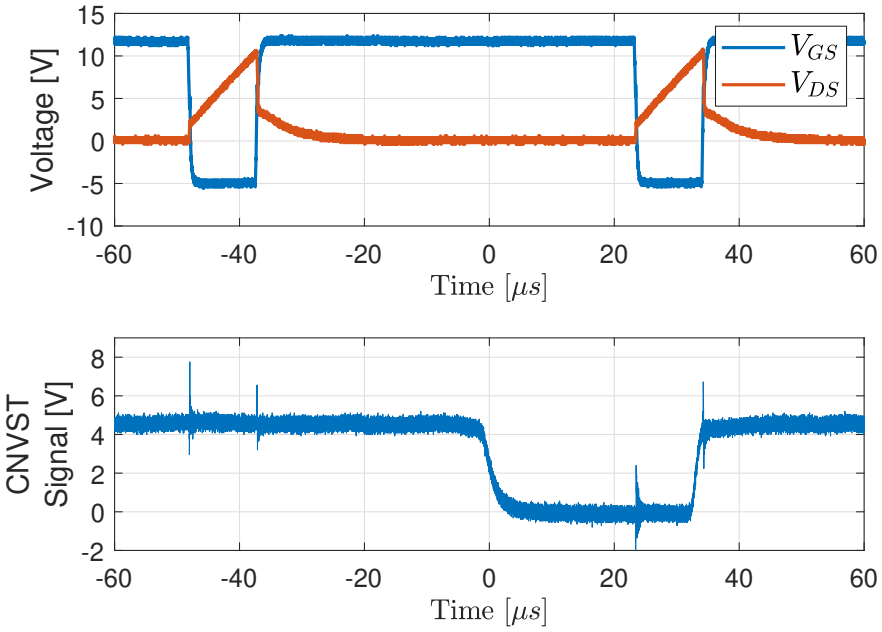
SiC MOSFETs present turn-on and turn-off times lower than their Si counterparts, which allows for higher switching frequencies, and requires a more robust measurement against higher dV/dt. The specific power module considered has a rising time of 16 ns, and when used with a DC-link voltage of 400 V results in a dV/dt of 25 $kV/\mu s$.

To illustrate the interference caused by the switching, the CNVST signal is registered, along with the gate signal and the on-state analog voltage. The CNVST signal is registered near the ADC pin, and the on-state voltage measurement is registered after the measurement circuit. Two cases are recorded, one with a DC-link voltage of 50 V and another with a DC-link voltage of 200 V. The waveforms are presented in Figure X.

The ADC is capable of performing the complete reading process, including sampling and reading, within $1\mu s$. If the process is completed within the on-time of the MOSFET, the switching noise



(a) 50 V on the DC-link



(b) 200 V on the DC-link

Figure 3.8 CNVST signal for two different DC-link values. Gate-Source voltage and Drain-Source voltage includes for reference.

would not happen during the communication between the ADC and the FPGA. In practice, the optocouplers limit the communication speed, and switching happens while the reading process takes place. The optocouplers used present a rise time and fall time of 4.6 μs and 15 μs, respectively. This fact alone highlights the optocoupler as a limiting factor in the reading speed of the whole circuit: several readings of the ADC could be performed during the rise time or fall time of the optocoupler alone.

An alternative to the optocoupler is the digital isolator. It provides faster rise and fall times, allowing faster communication between the FPGA and the ADC. The Skyworks Si8645BD and Si8715BD digital isolators are chosen as a replacement, as they provide the necessary voltage isolation and common mode rejection. Some of the relevant parameters of the optocouplers and digital isolators are presented in Table 3.1.

The optocouplers present a common mode rejection of 5 $kV/\mu s$. In contrast, the chosen digital isolators feature a common mode rejection of 50 $kV/\mu s$. This allows the test setup to operate with a DC-link voltage of up to 800 V with the same rise time of the SiC MOSFET module. Since the setup is rated for 700 V, the digital isolator chosen is deemed sufficient in terms of common mode rejection.

It is also worth mentioning the speed advantage that digital isolators present over optocouplers. As SiC MOSFETs can operate at higher switching frequencies, faster readings are mandatory for AC power cycling.

Table 3.1 Relevant parameters of the optocoupler and the digital isolator.

Parameter	Optocoupler	Digita Isolator
Propagation delay	7.4 μs	8 ns
Common Mode Transient Immunity	5 kV/μs	50 kV/μs
Rise Time	4.6 μs	2.5 ns
Fall Time	15 μs	2.5 ns
Isolation Voltage	4.42 kV	5 kV

Based on the previous discussion, the digital isolator allows a more robust reading when faster SiC MOSFETs are used in place of Si IGBTs. Moreover, they allow faster readings, which is important in high switching frequency operation.

3.4 Digital Isolator PCB

A redesign of the Main PCB to include the digital isolators instead of the optocouplers is the ideal solution, as an integrated design is more compact and can be more robust in noisy environments. As there are many Main PCBs already manufactured and implemented, and considering the time constraint of the project and the cost of remaking the Main PCBs, an alternative method is decided, where and additional small PCB, called Digital Isolator PCB, is added to the Main PCB to replace the optocouplers.

The Digital Isolator Board is designed to use two digital isolator ICs, connecting the ADC communication pins and the NI cRIO FPGA. There are several considerations regarding the design of the Isolator PCB:

- Connection to the Main Board.
- How to power the ICs on the Isolator PCB.
- How to maintain isolation.

As this PCB replaces the optocouplers, the connection to the Main PCB is limited to the SMD pads designed for the optocoupler ICs. The pitch between the SMD pads of the optocouplers is 100 mils (0.1 in), which is the same standard for some PCB connectors on the market. Due to space constraints, the Isolator PCB needs to be placed perpendicular to the Main PCB, and right angle connectors are needed for this purpose.

Existing SMD header connectors for PCB present a distance of 7 mm between the rows of contacts. As the distance between the edges of the pads for the optocoupler IC is around 9 mm, these types of connectors do not reach the contacts to form a strong soldered connection. Single row through hole connectors were found at the student lab at AAU, and have a spacing of 12 mm between the leads when placed against each other. This solution is tested successfully on a damaged Main Board that is no longer in use. The soldered connection provides enough area to provide a solid bond that allows the connection and disconnection of another PCB without stripping the SMD pads or damaging the Main Board. Based on this test, this connection is chosen to be implemented.

The design of the Isolator PCB is restricted by the signals available coming from where the optocoupler were placed. These signals are the communication interface to the ADC, and are split in two sides, the LabView side, where the FPGAs connect, and the ADC side, where the ADC and measuring circuit are present. The isolation between these two sides needs to be preserved.

The digital isolator ICs require a separate 5 V supply on each side. From the Main PCB connection, only one pin providing 5 V is available on the ADC side, thus, a connection to the GND of this side is needed, as well as an extra connection to a separate power supply for the FPGA side.

The Isolator PCB needs enough clearance to fit between the D-Sub connectors and the DCDC converters present in the Main PCB. The maximum span of the PCB is 36 mm. The final design of the Isolator PCB mounted to the Main PCB is shown in Figure 3.9.

3.4.1 Validation of the Digital Isolation PCB

To ensure that the Isolator PCB works properly, the communication signals are measured on the input and output side. One of these readings is shown in Figure 3.10 for the DATA signal.

The outputs signals follow the inputs correctly. The same verification is done for the rest of the signals, and all of them are followed correctly. The FPGA code that handles the reading process is updated with faster reading times, following the recommended times in the datasheet of the ADC. Several tests are conducted to ensure that the communication with the ADC remains functional after the code update. For this purpose, a small voltage is applied between the Drain and the Source of each MOSFET, and this "on-state" voltage reading is performed for values between 1 V and 2 V. During this process, the communication signals at the ADC are monitored using a digital signal probe. The registered signals are shown in Figure 3.11.

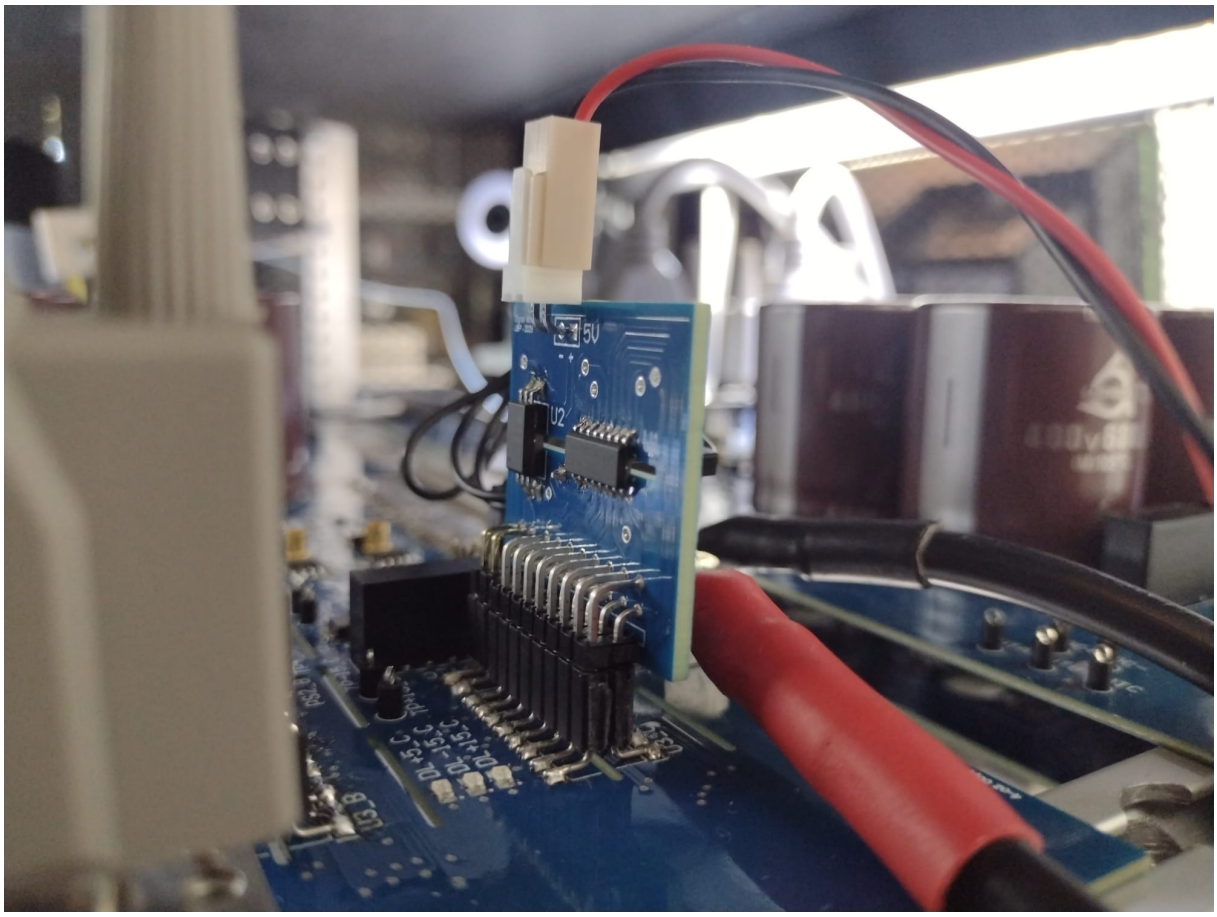


Figure 3.9 Isolator PCB installed in the test setup.

The signals show the expected behavior, and the complete process takes close to 1.2 μs. The readings are successful and show the correct voltage reading for both switches (high side switch and low side switch), and the communication with the ADC and the new code are validated.

To finish the validation of the Isolator PCB, a test is performed in the AC power cycling setup, and voltage and current are applied, in the same manner as a regular ACPC test. The voltage reading of both switches shows erratic behaviour, jumping to 10 V in some occasions. To investigate further, the CNVST signal of the ADC is registered using a differential probe, along with the gate signal and the on-state voltage of the lower switch. The behaviour is registered for a DC-link voltage of 0 V and 200 V, and the results are shown in Figure 3.12.

The trigger pulse of the CNVST signal starts the conversion of the ADC at 0 s. The signal shows a noise spike at the moment the current is switched, and it is possible that this spike triggers the conversion of the ADC.

With the Adapter PCB designed and tested, the next chapter discusses the test results for DC power cycle and AC power cycle. Given the time constraints of the project, the DC and AC power cycle tests are performed with the original optocouplers. The limitations of this setup are addressed in the next chapter.

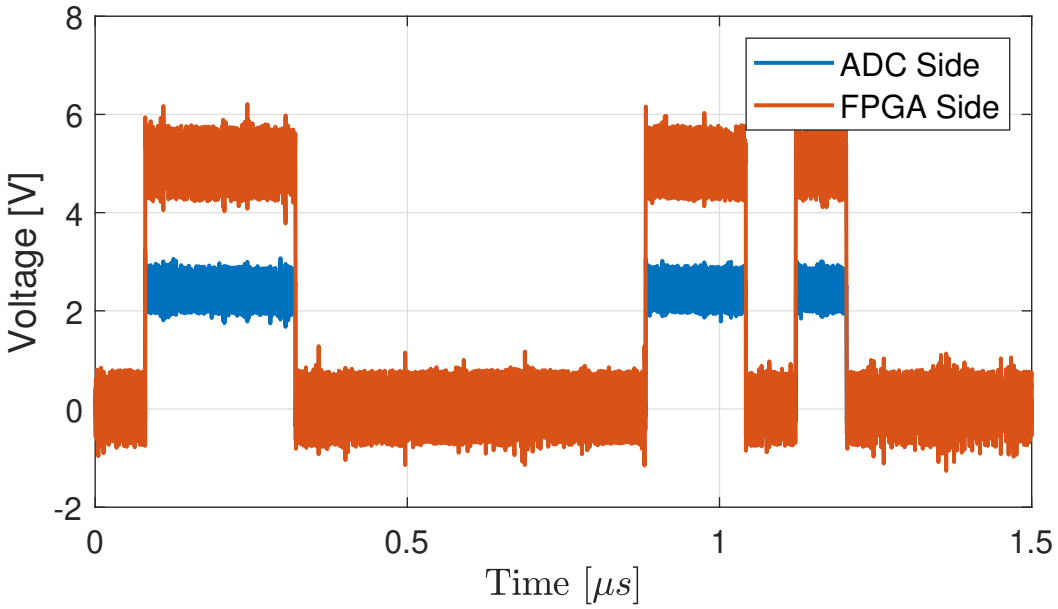


Figure 3.10 Voltage measurement for the DATA signal on both sides of the digital isolator.

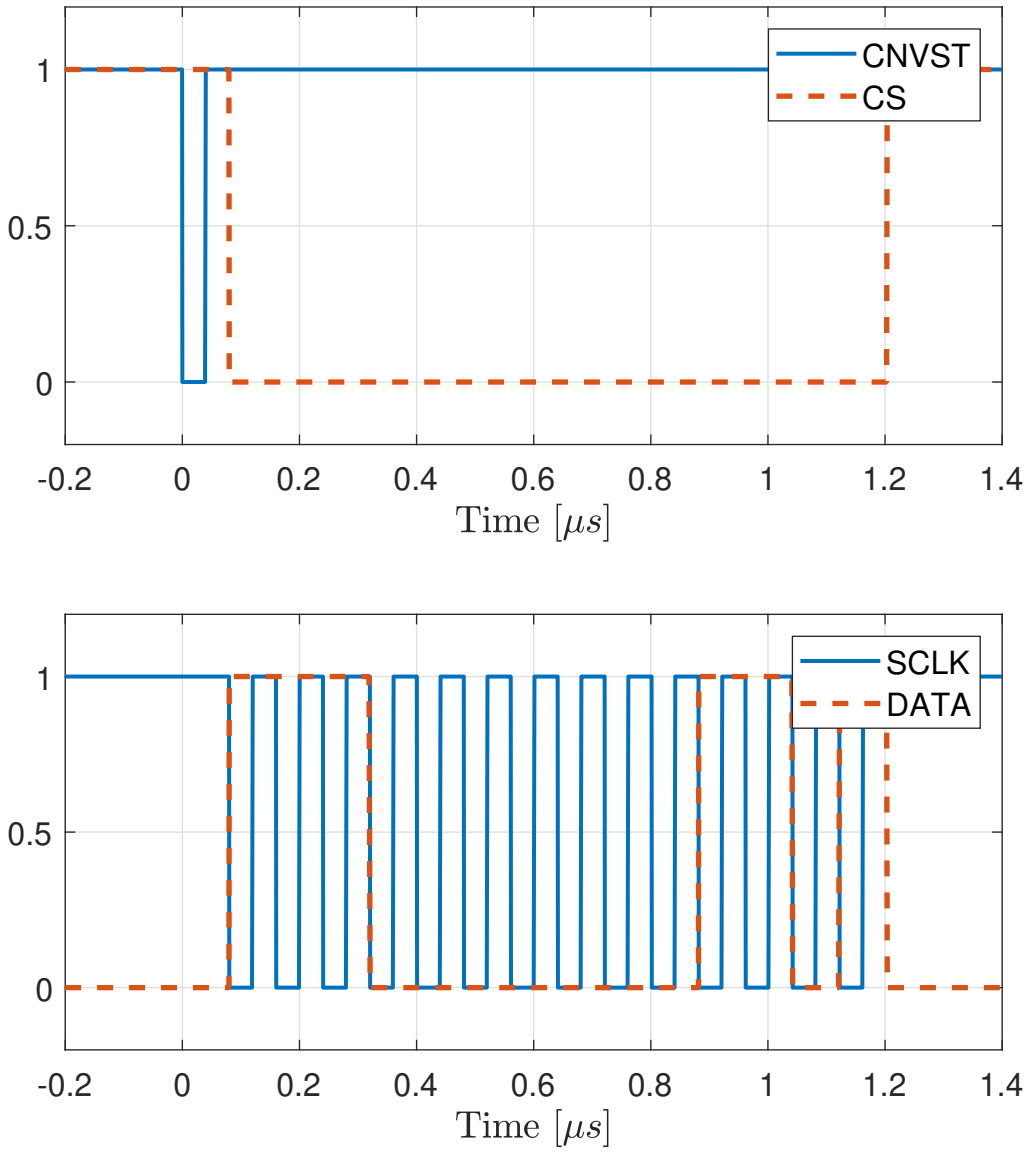
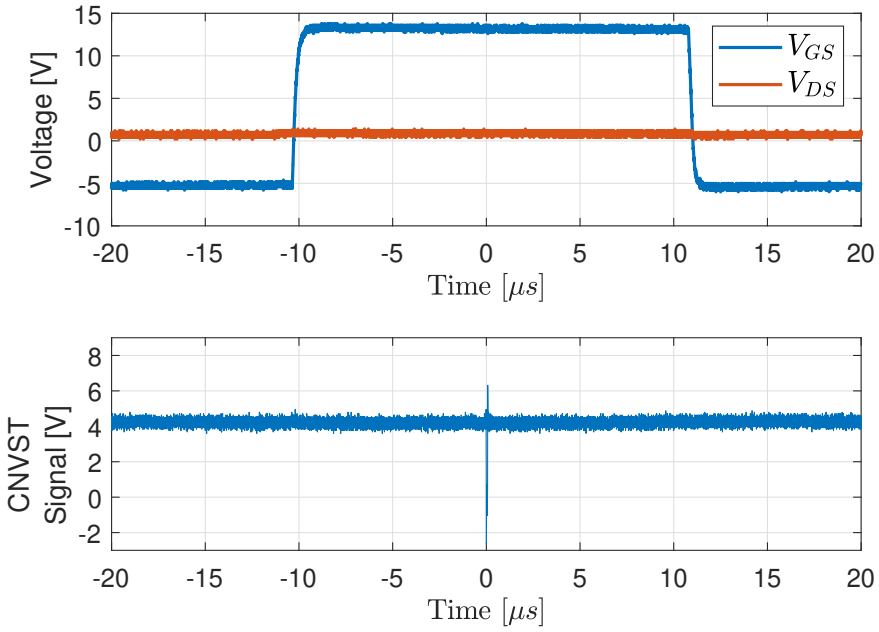
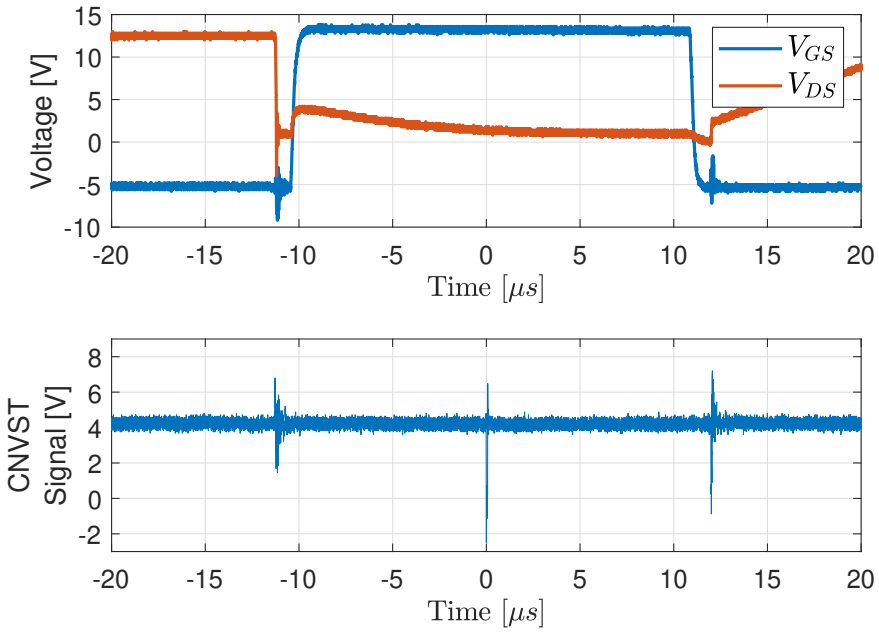


Figure 3.11 Digital signals registered during an ADC reading process, under the updated code and with the Digital Isolator PCB incorporated.



(a) DC-link voltage of 0 V



(b) DC-link voltage of 200 V

Figure 3.12 Signals registered for different DC-link voltages. The FPGA sends the CNVST trigger at $t = 0$

4 Experimental Results and Discussion

This chapter presents and analyses the results of the power cycling tests performed on SiC MOSFETs. Two types of stress tests were conducted: DC power cycling and AC power cycling. The purpose is to compare the degradation behaviour and failure mechanisms observed under different operational stresses. During this chapter, the MOSFET connected between VDC+ and the AC output is referred to as the Upper switch, while the one connected between the AC output and VDC- is called the Lower switch. For both types of tests, only one phase is used at a time, effectively using the setup as a full-bridge inverter.

4.1 DC Power Cycling Test

As explained in previous sections. the DC power cycle test applies a constant current through the device for a set period of time, to raise its temperature and apply the desired thermal stress.

The necessary testing parameters for the DCPC test are calculated before the test is initiated, to verify that the test setup is capable of reaching the desired testing conditions.

The objective of the test is to apply a temperature swing of 70 K and reach a maximum junction temperature of 145 °C. Based on the equations presented in Chapter 2, the testing parameters are calculated as:

$$T_{HS} = \hat{T}_j - \Delta T = 145 - 70 = 75°\text{C} \tag{4.1}$$

$$I_D = \sqrt{\frac{\Delta T}{R_{DS\_ON} R_{Th}}} = \sqrt{\frac{70}{0.050 \cdot 1.02}} \approx 37.05\text{A} \tag{4.2}$$

The calculated test parameters fall within the capabilities of the setup and the MOSFETs, and are the starting point to adjust the power source and the heatsink temperature.

Two samples have been tested. The adapter PCB is installed on the test setup, and the heating and cooling curves of each switch are registered for thermal characterization of sample #1. The thermal resistance between junction and heatsink is extracted for both switches, showing a value of 1.5812 K/W for the upper switch, and 1.5687 K/W for the lower switch.

The load curent calculation is updated with these values to 29.76 A and 29.87 A for the high and low switch, respectively. Both values are still within the capabilities of the testing setup and the MOSFETs.

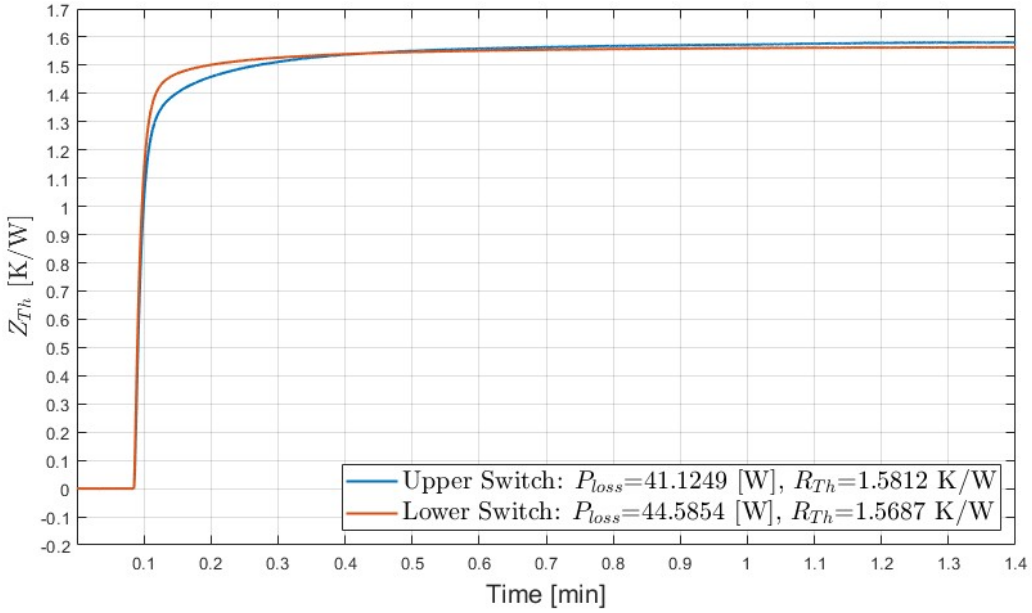


Figure 4.1 Thermal impedance for both switches of Sample #1.

4.1.1 Test Conditions

Two samples are tested until failure. The test conditions are presented in Table 4.1. The test continuously monitored the on-state voltage of each switch, and their maximum and minimum junction temperature. The on-state voltage measurement is done before the device is switched off.

Table 4.1 DC Power Cycling Test Parameters

Parameter	Sample #1	Sample #2
Test Current	30 A	30 A
On/Off Time	2 s / 2 s	2 s / 2 s
Heatsink Temperature	70 °C	63 °C
Initial dT	70 °C	70 °C
Initial max. T_j	145 °C	140 °C

The temperature profile applied to the switches of sample #1 is shown in Figure 4.2. The lower switch shows a higher on-state voltage, higher temperature swing and higher maximum temperature, thus, the test is adjusted to reach the desired testing conditions on this switch.

4.1.2 Test Results Sample #1

The lower switch presents a higher temperature swing and higher maximum temperature, and it stopped conducting before the high side switch. The on-state voltage of both MOSFETs during the test is shown in Figure 4.3. $V_{DS,on}$ exhibited a slow and steady increase over time, accelerating near the end of the test. Near the end of the test, the lower switch shows a sudden peak in on-state voltage.

The temperature swing and maximum junction temperature during the test are shown in Figure 4.4 and Figure 4.5 respectively. Both switches show a steady increase over time, which accelerates

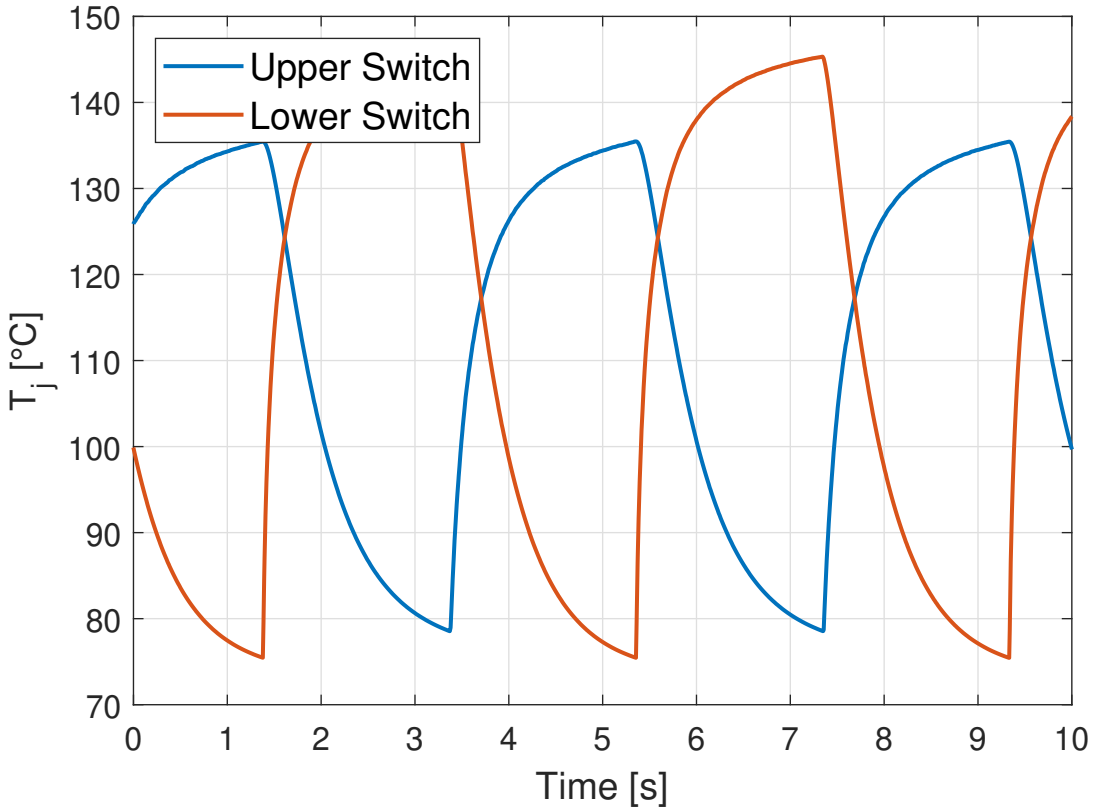


Figure 4.2 Temperature profile during the DC power cycle test.

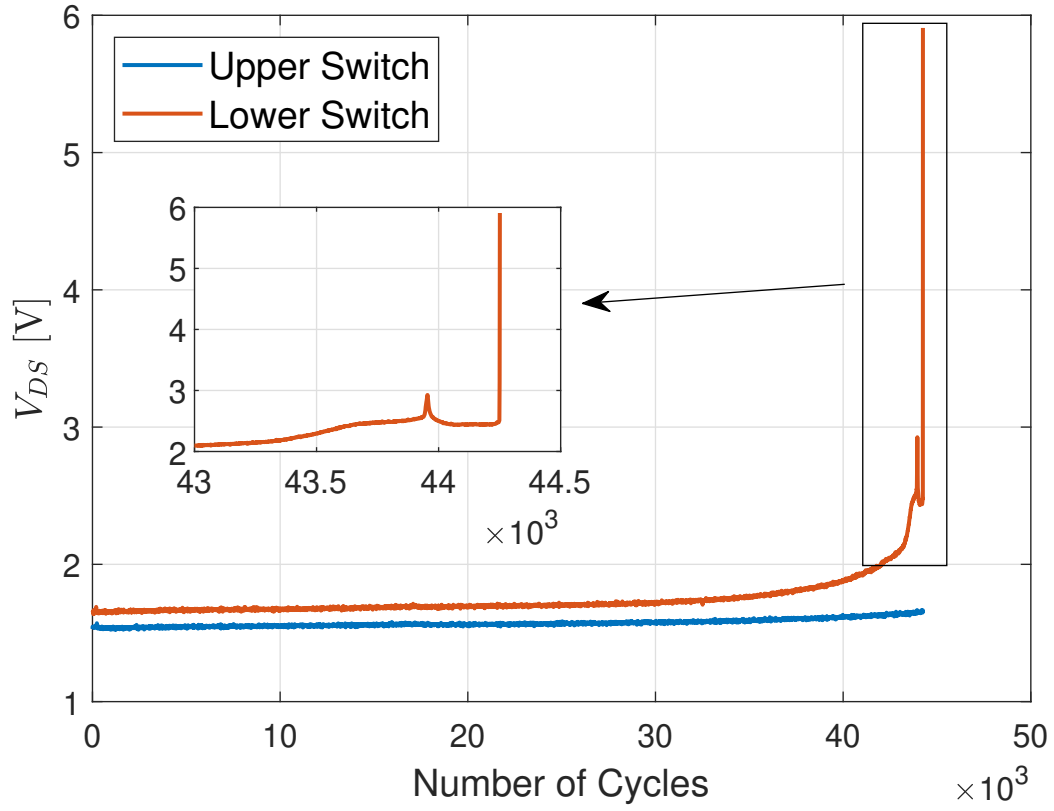


Figure 4.3 On-state voltage vs. number of cycles for both switches.

near the end of the test for the lower switch.

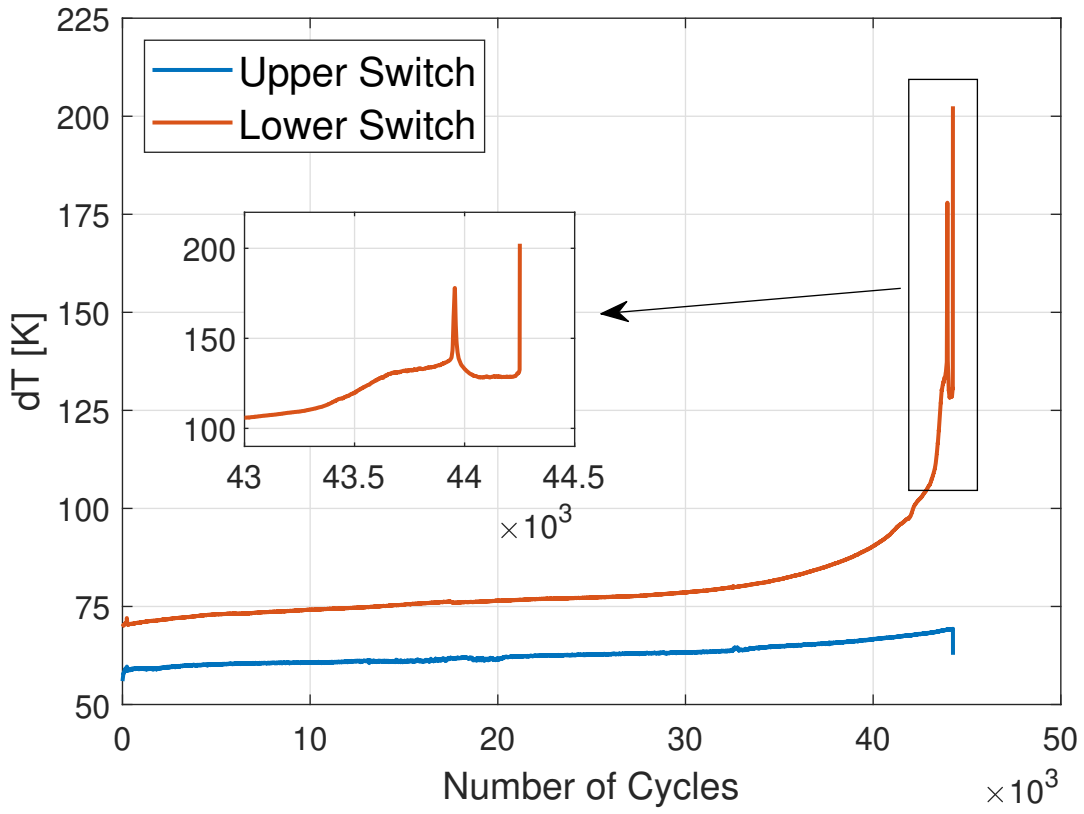


Figure 4.4 Temperature swing dT during the test.

The on-state voltage of the lower switch shows a rapid increase near 43,500 cycles, and a sudden spike near 44,000 cycles. This behaviour shows a possible bond degradation, where the bond wire starts lifting, increasing the contact resistance and the power losses. The sudden spike in voltage could indicate the moment of lift-off, after which there is no longer any contact and the voltage falls close to the level before the lift-off.

To account for the temperature effect on the on-state voltage, a linear trend is obtained from the first 40,000 cycles. The data and linear trend are presented in Figure 4.6.

The linear trend is used to correct the effect of temperature in the on-state voltage readings. The corrected voltage values are given by Equation 4.3, where α is the slope extracted from the linear trend of Figure 4.6, and T_0 is a reference temperature, chosen at 150 °C. $V_{DS,test}$ and $T_{j,max}$ are the on-state voltage and maximum junction temperature registered during the test, respectively

$$V_{DS,corrected} = V_{DS,test} - \alpha(T_{j,max} - T_0) \tag{4.3}$$

The result is shown in Figure 4.7. The previously observed gradual rise in voltage is almost non-existant after correction. An increase in V_{DS} is noticeable shortly after the 43,500 cycle

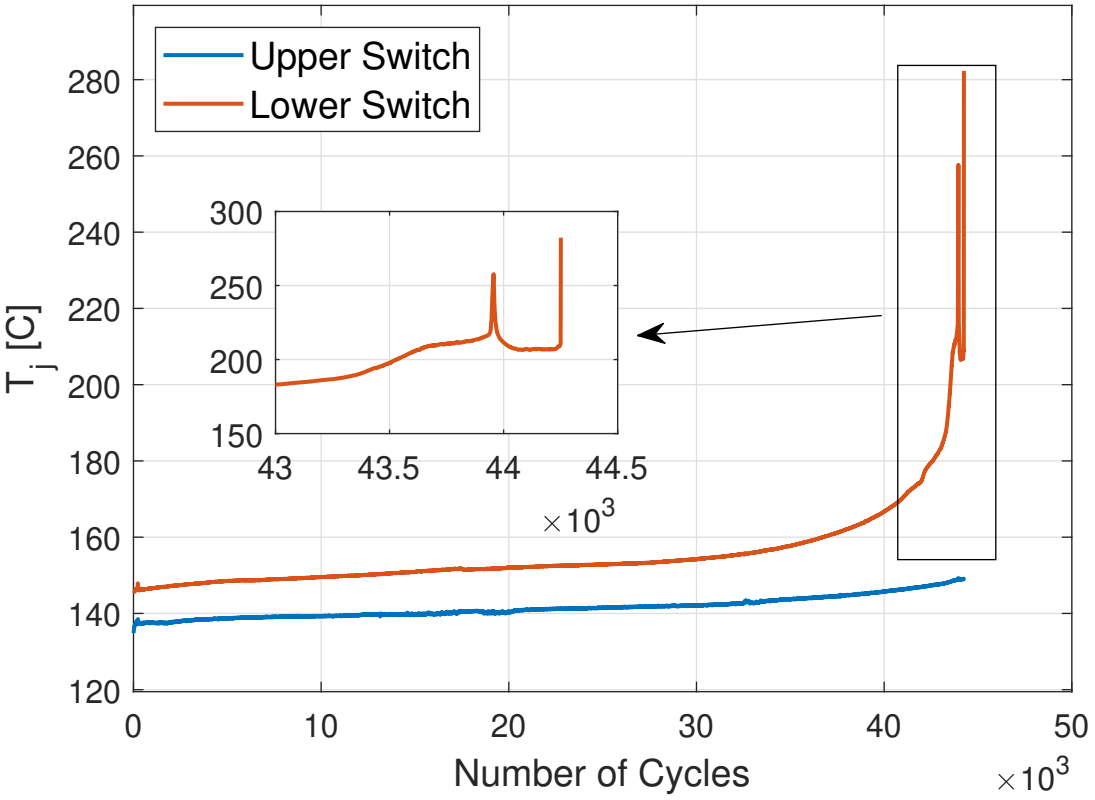


Figure 4.5 Maximum junction temperature during the test.

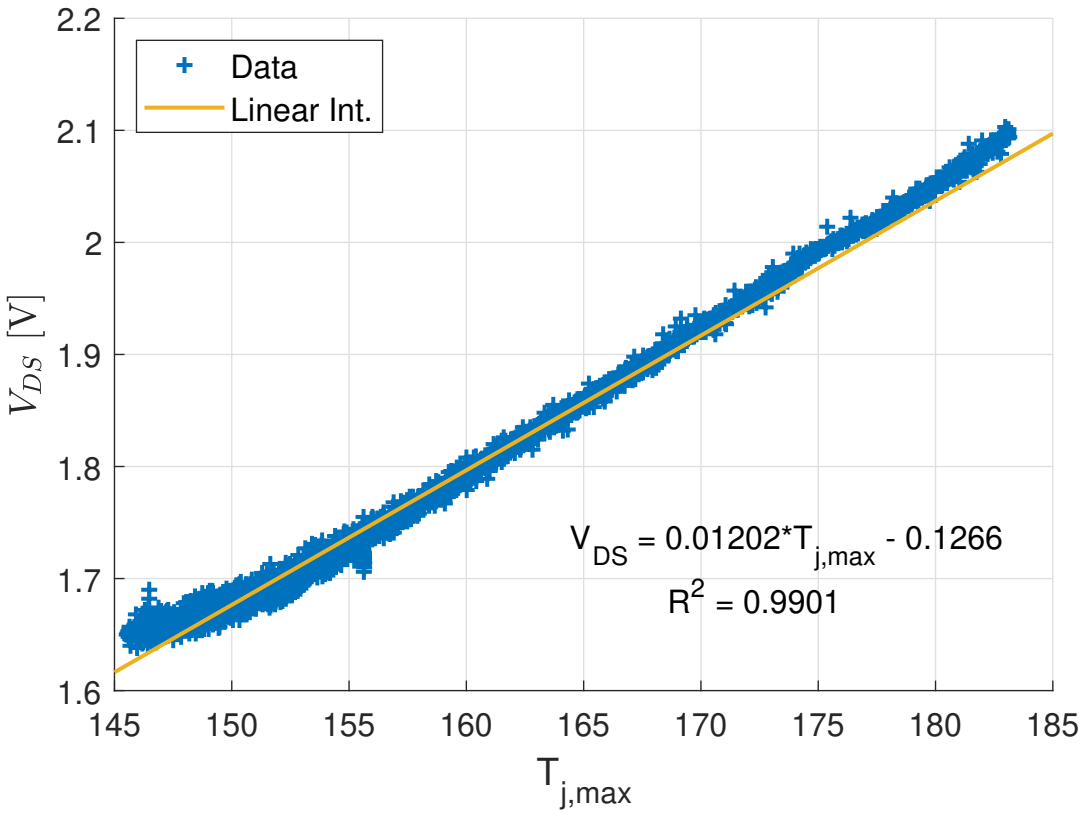


Figure 4.6 On-state voltage vs maximum junction temperature and linear trend.

mark, followed by the spike previously seen in Figure 4.3 and 4.4.

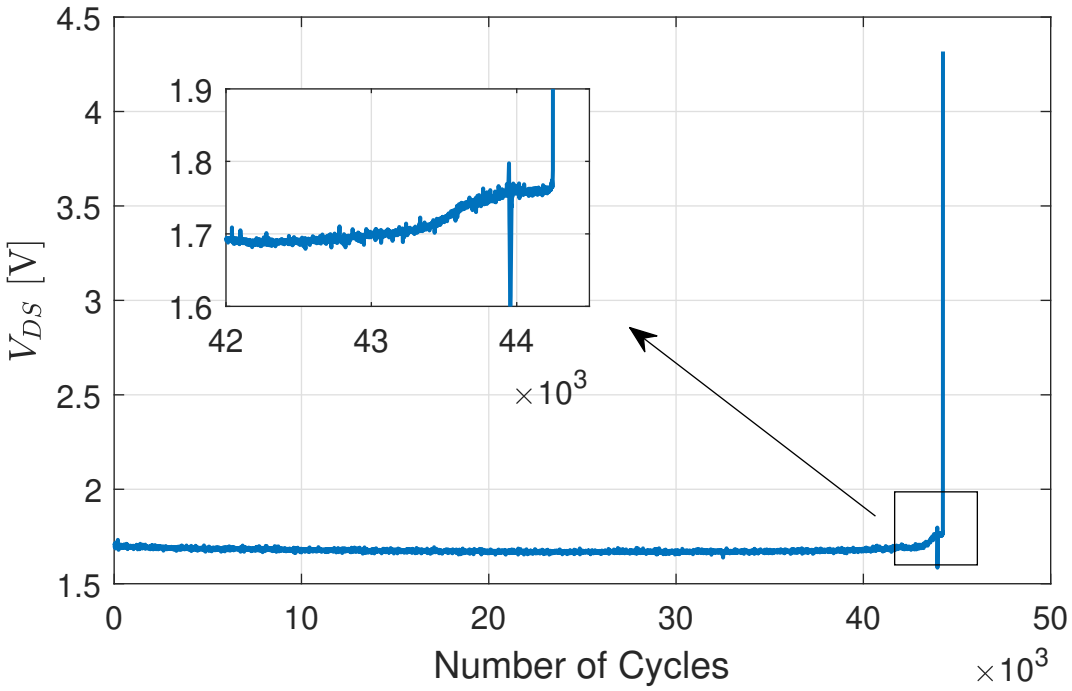


Figure 4.7 On-state voltage of lower switch after temperature correction.

4.1.3 Test results Comparison

The on-state voltage of the two samples is shown in Figure 4.8. Sample #2 shows a clear jumps in voltage, corresponding to bond wire lift-off. Sample #1 was tested with a higher maximum junction temperature and with the same initial dT, and is the first to fail.

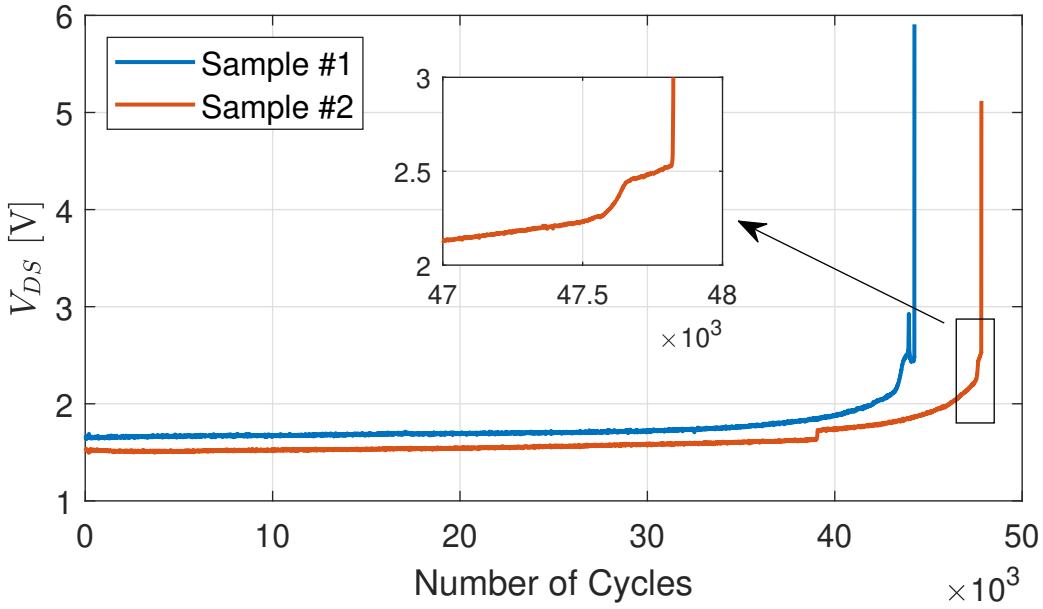


Figure 4.8 On-state voltage for Samples #1 and #2.

The temperature swing is presented in Figure 4.9. For both samples the temperature swing

increases steadily, mostly at the same rate. After around 35.000 cycles Sample #1 starts increasing at an accelerated rate, while Sample #2 increases rapidly after the sudden jump in dT.

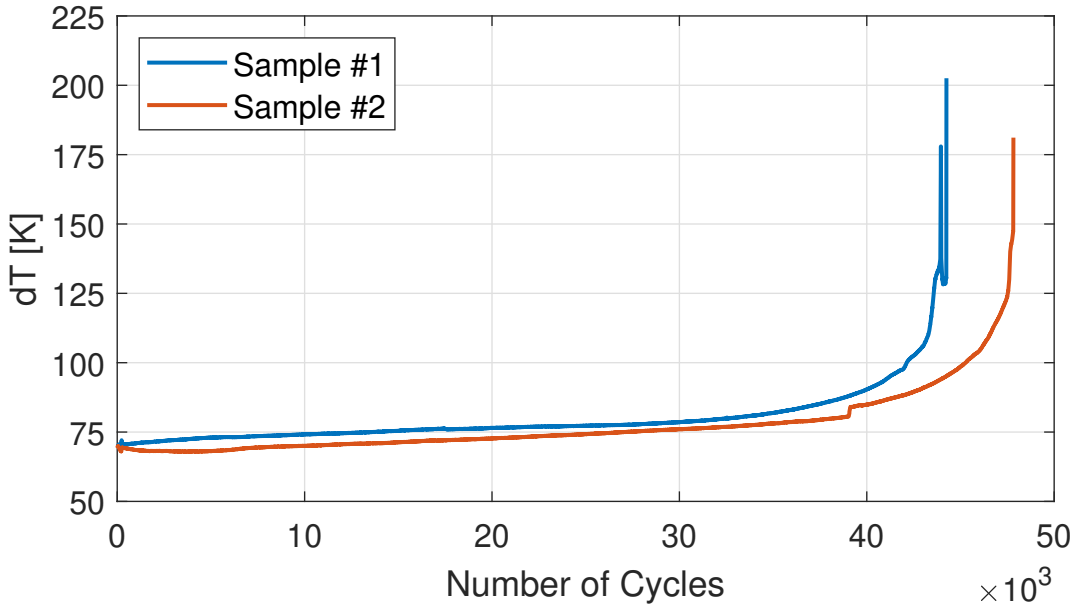


Figure 4.9 Temperature swing for Samples #1 and #2.

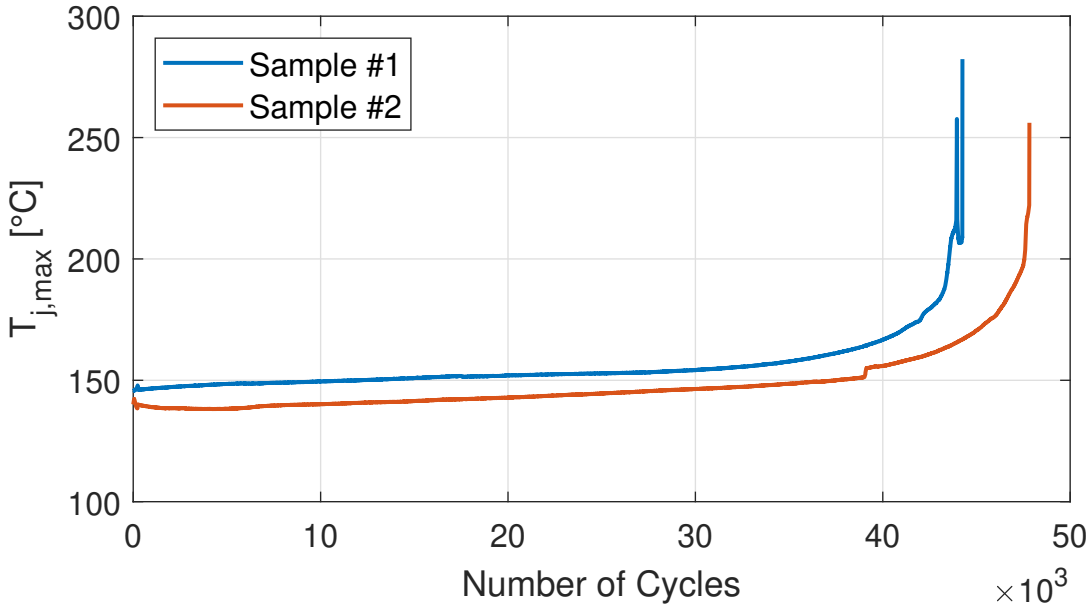


Figure 4.10 Maximum junction temperature for Samples #1 and #2.

4.2 AC Power Cycling Results

The AC power cycle test uses a sinusoidal current to stress the devices under test. The resulting waveforms are presented, however, the test has not finished before this report has been delivered. Nontheless, some comparisons between this case and the DC power cycle test are drawn based on the available data.

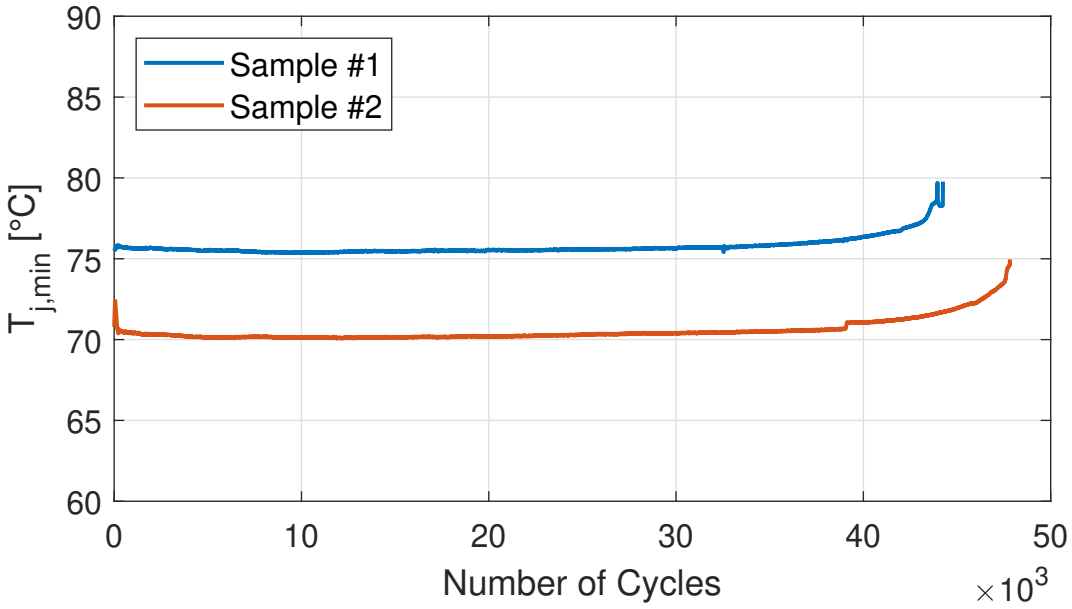


Figure 4.11 Minimum junction temperature for Samples #1 and #2.

4.2.1 Test Conditions

The testing conditions of the AC power cycle are presented in Table 4.2. The on-state voltage is measured at the peak of the current of the corresponding device. The load current is presented in Figure 4.12.

Table 4.2 AC Power Cycling Test Parameters.

Parameter	Value
Peak Phase Current	$\approx$ 30 A
DC-link Voltage	200 V
Modulation Type	Sinusoidal PWM
Switching Frequency	15 kHz
Fundamental Frequency	0.25 Hz
Load resistance	5.6 $m\Omega$
Load inductance	420 μH
Heatsink Temperature	70 °C
Initial dT	70 °C
Initial max. T_j	140 °C

The temperature profile of the upper switch is shown in Figure 4.13. It shows a different shape when compared to the DC power cycle test. The first half of the cycle resembles a sinusoidal shape, while the second half shows a shape similar to an exponential cooling, with some differences near the end of the cycle.

4.3 Comparative Analysis

After the two tests are conducted, the results between the DC and AC version of the power cycle test are compared.

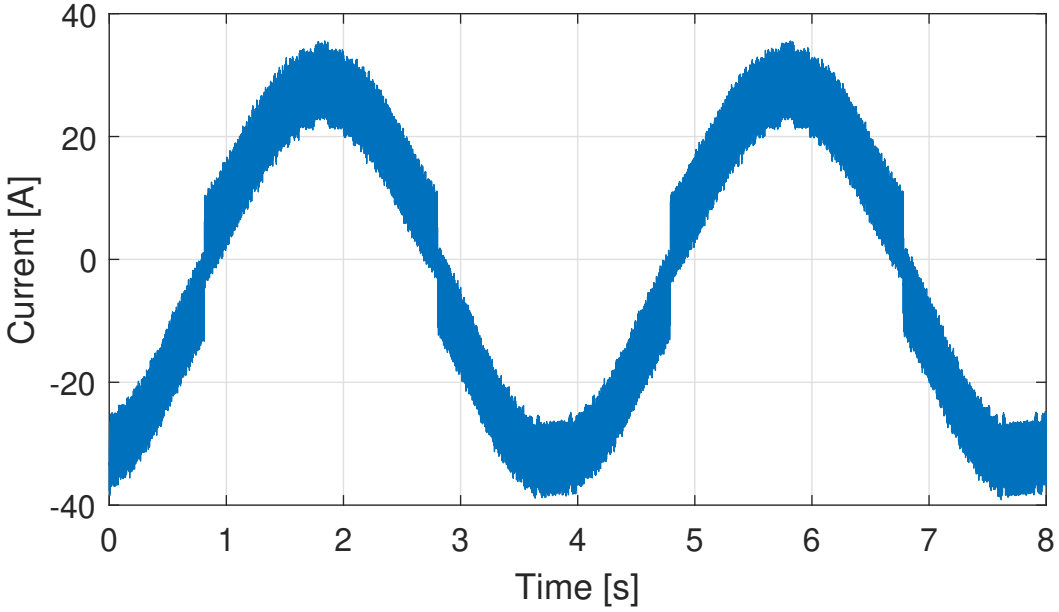


Figure 4.12 Output current during the AC power cycling test.

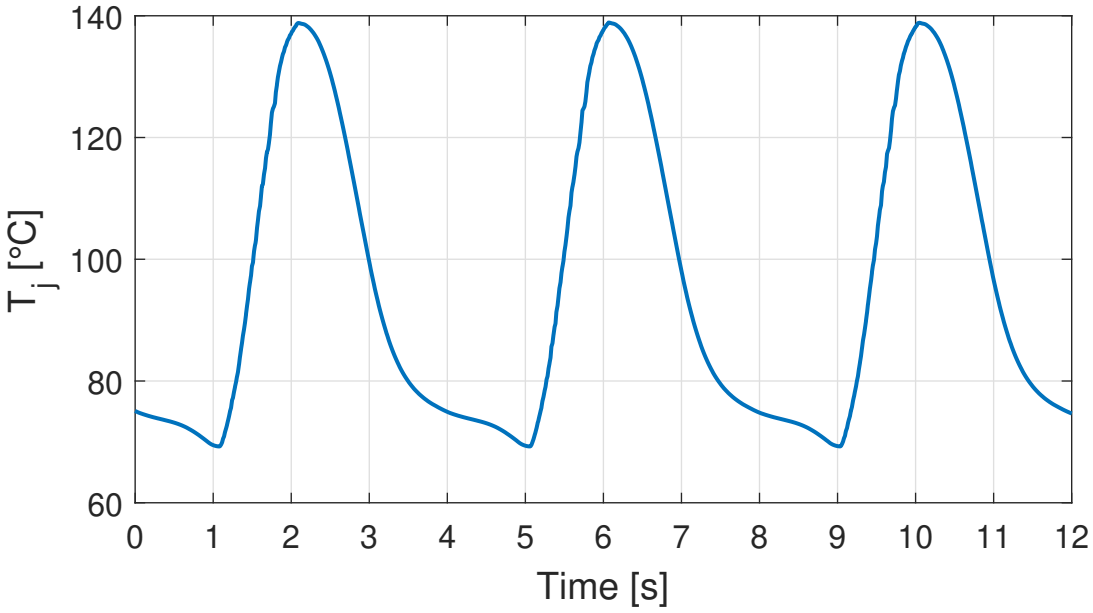


Figure 4.13 Temperature profile of the upper switch during the ACPC test.

4.3.1 Temperature profile

In the DC power cycle test the on/off times are selected to reach the desired temperature swing, and take into account the thermal impedance of the device, from the junction to the heatsink. While the DC version of the test applies a step current, the AC variant uses a sinusoidal current to generate the power losses in the device. Both temperature profile are compared in Figure 4.14. The temperature cycle of the DC version shows a sudden step in temperature at the moment the switch is turned on. In contrast, the increase and decrease in temperature during the AC power cycle is more gradual, especially the decrease during the late half of the cycle.

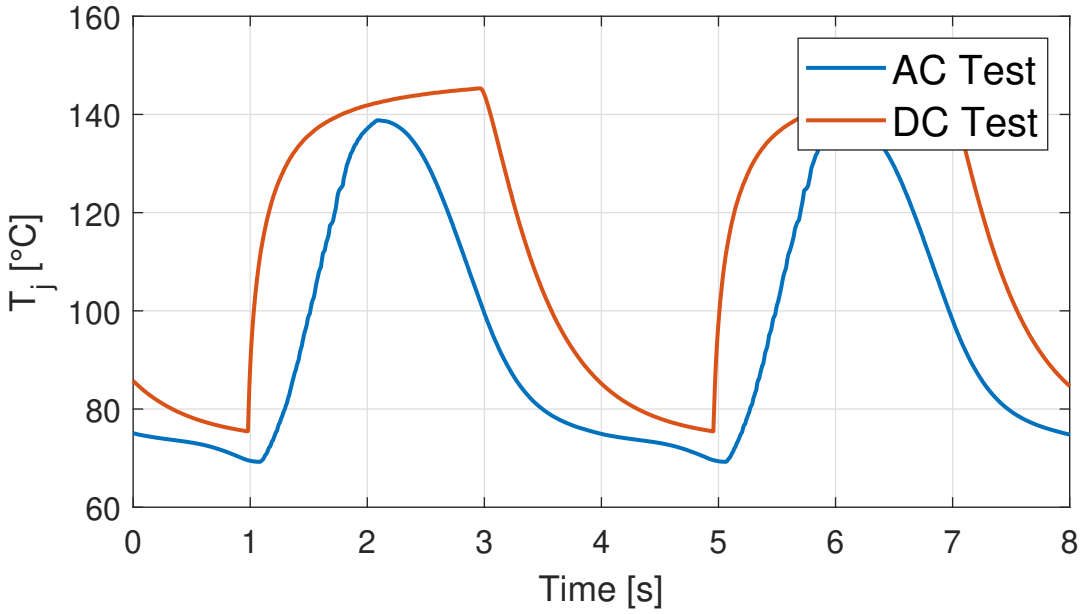


Figure 4.14 Temperature profile for the AC and DC test.

The difference on the shape of the temperature profile is explained by the shape of the current, and the implementation of the PWM modulation. The AC power cycle test applies a sinusoidal current, and therefore, the power losses will follow a similar shape. In contrast, the DC power cycle applies a step in current, and therefore, a step in power losses. As explained in Chapter 2, the resulting temperature profile is a filtered version of the power losses, where faster transients are less noticeable.

For the testing conditions, the fundamental output voltage and current of the DUT are closely in phase. This means that the duty cycle of the upper switch is at its maximum close to the positive peak of the current, and at its minimum close to its negative peak. The conduction losses during one PWM cycle can be considered as follows:

$$P_{Cond} = \frac{1}{T_{sw}} \int_0^{t_{on}} R_{DS,on} \cdot i^2 dt \approx D(t) \cdot R_{DS,on} \cdot i^2(t) \tag{4.4}$$

where T_{sw} is the switching period, $t_{on} = D \cdot T_{sw}$ is the fraction of time the switch is on, $D(t)$ is the duty cycle, and $i(t)$ is the switch current, which is considered as constant during t_{on}. If $D(t)$ and $i(t)$ are in phase, the conduction losses reach a maximum at the maximum of $i(t)$ and a minimum when the current crosses zero. Moreover, conduction losses also occur during the negative part of the current, but to a lesser degree, and the temperature rises accordingly. This highlights a difference of this test when compared to Si IGBT testing in this configuration: the negative part of the output current does not create power losses in the upper IGBT, but it affects the temperature profile for the SiC MOSFET. The theoretical conduction losses for different power factors are shown in Figure 4.15, where the on-state resistance is considered as constant. Two peaks in power losses are present, and they become equal as the power factor reaches 0. In reality, for the second peak the power losses are attenuated by a lower on-state

resistance that decreases with a lower temperature.

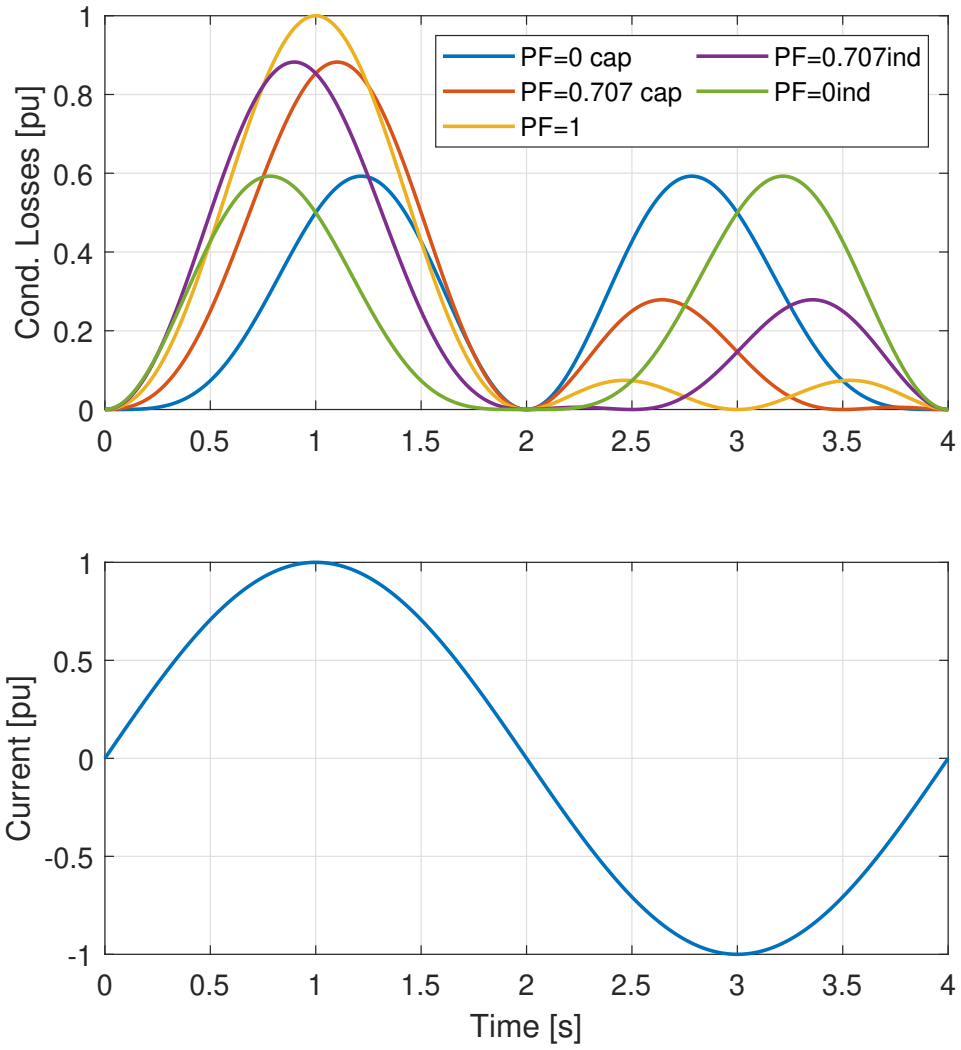


Figure 4.15 Theoretical normalised average conduction losses for different power factors. Current is shown as a reference.

The thermal impedance can limit the temperature swing achieved, and its effect can be more noticeable for higher fundamental frequencies. As explained in Chapter 2, the thermal impedance acts as a filter for the power losses, and higher fundamental frequencies lead to lower temperature swings for the same level of power losses. This effect can limit testing conditions if the maximum achievable current does not result in the desired power losses. An alternative in this case can be to reduce the gate voltage, increasing the on-state resistance, however, this also can deviate from real-life conditions.

After the test results have been reviewed and compared, the next chapter shows the conclusions extracted from tha laboratory work and the test results.

5 Conclusions

In this thesis, power cycling tests of SiC MOSFET have been analysed and conducted. In this chapter, conclusions are presented based on the results of the tests and the laboratory work.

5.1 Test Setup Adaptation

The test setup has been modified from Si IGBT testing to SiC MOSFET testing. One of the challenges discussed in this thesis is the on-state voltage measurement and its implementation in a faster switching environment. The optocouplers previously used do not operate correctly when SiC MOSFETs are tested, resulting in an unreliable measurement. The change to digital isolators presents challenges in its implementation, as a full redesign of the Main Board PCB was not a feasible option within the time frame and budget of the project. The proposed solution shows that an integration of the isolators to the existing Main PCBs is feasible, and data transmission is achieved. EMI issues are present caused by the faster switching introduced by the SiC MOSFETs. In particular, the conversion of the ADC could be triggered unintentionally, which introduces a voltage reading when the switch is off. The solution to this problem involves further testing of the different communication signals of the ADC, and a possible redesign of the Isolator PCB.

One AC power cycle test is conducted with the optocouplers in place, and with a reduced DC-link voltage. The test can be performed to the desired temperature swing, however, the limitation of the DC-link voltage reduces the switching losses, and changes the temperature profile obtained.

5.2 Test Results

DC and AC power cycles were performed for this thesis. However, the AC version did not finish in time for the delivery of this document. Nonetheless, differences in the temperature profile are observed, and confirm the results shown in simulations.

There are differences in the temperature profiles of the DC and AC versions of the power cycling test. The waveform of the current and the thermal impedance affect the final temperature profile of the junction temperature. An increase in the fundamental frequency will highlight the effect of the thermal impedance, reducing the temperature swing for the same current amplitude. The test conditions should take this into account, since the thermal impedance is different for each manufacturer, power module, packaging, etc. Moreover, there are differences in the rate of change of the temperature, showing a more aggressive temperature rise on the DC version. This behaviour deviates from the real life behaviour in some applications like motor drives, where a sinusoidal current creates a slower rise in temperature.

The results of the DC power cycling test show degradation of the packaging. In particular, bond wire lift-off is present, and it can be seen on the on-state voltage reading as a fast rise in voltage

followed by a sudden spike. The AC power cycling test shows a similar result, with a smoother increase in the on-state voltage.

5.3 Future Works

During this thesis, several limitations were encountered, which reduced the scope of the project. This section discusses possible aspects that could be further developed.

A deeper investigation in the timing and communication process between the FPGA and the ADC can confirm if the conversion is properly triggered. The addition of a separate PCB solely dedicated to the on-state voltage measurement can also be a viable option, replacing the voltage measurement section on the Main PCB altogether.

Incorporating the ability to operate the DUT converter with different power factors would allow different test conditions to be analysed. The current control implementation operates with a fixed power factor, determined by the inductive load.

Several DC and AC power cycle test could be perform. Time limitations and laboratory availability reduced the amount of samples that could be tested during the project. More tests to failure can be used to better understand the behaviour of the power modules used, and statistical processes can be used to create lifetime models and quantify the reliability of the modules.

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[12] SEMIKRON. Mounting instruction semitop e1/e2.

[13] Analog Devices. True bipolar input, dual 12-bit/14-bit, 2-channel, simultaneous sampling sar adc ad7366/ad7367.

A Appendix 1

A.1 AC Power Cycle Results

As the AC power cycle test did not finished before this document is delivered, the registered data is presented for illustrative purposes. The data presented was recorded before the device failed.

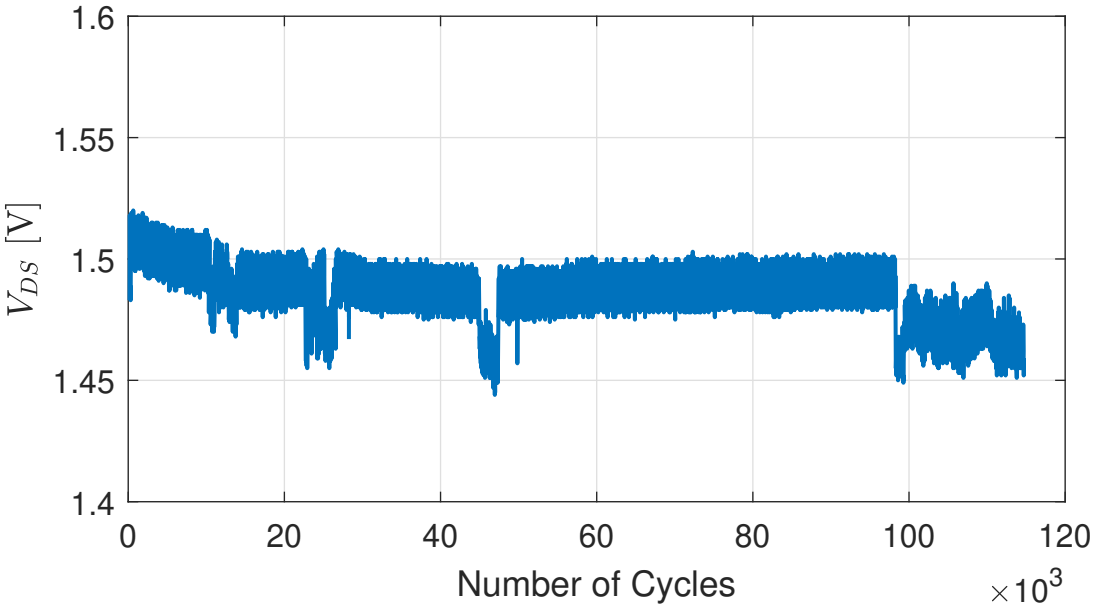

Figure A.1.1 On-state voltage.

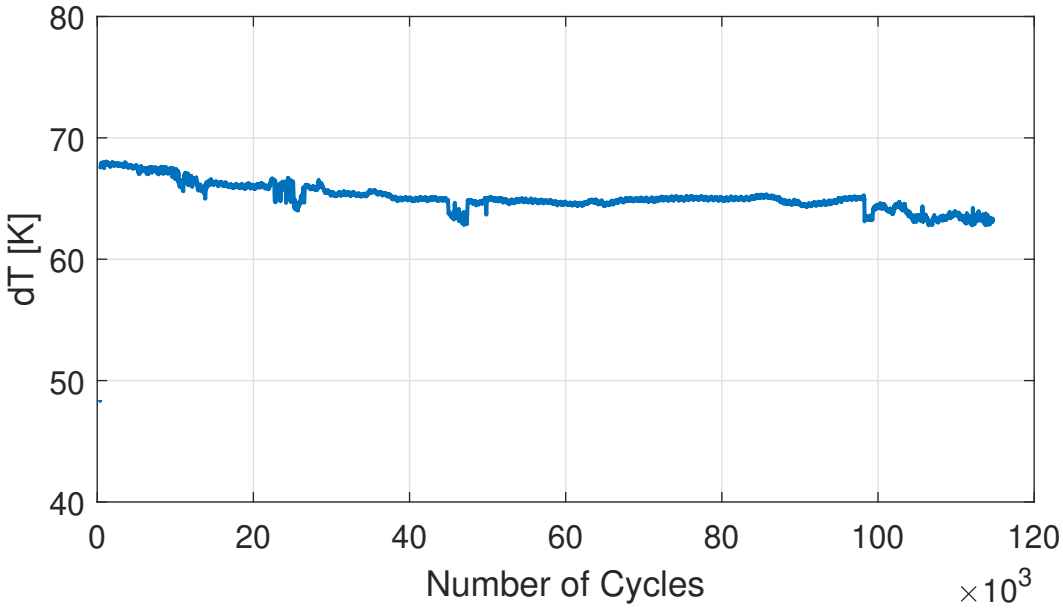

Figure A.1.2 Temperature swing.

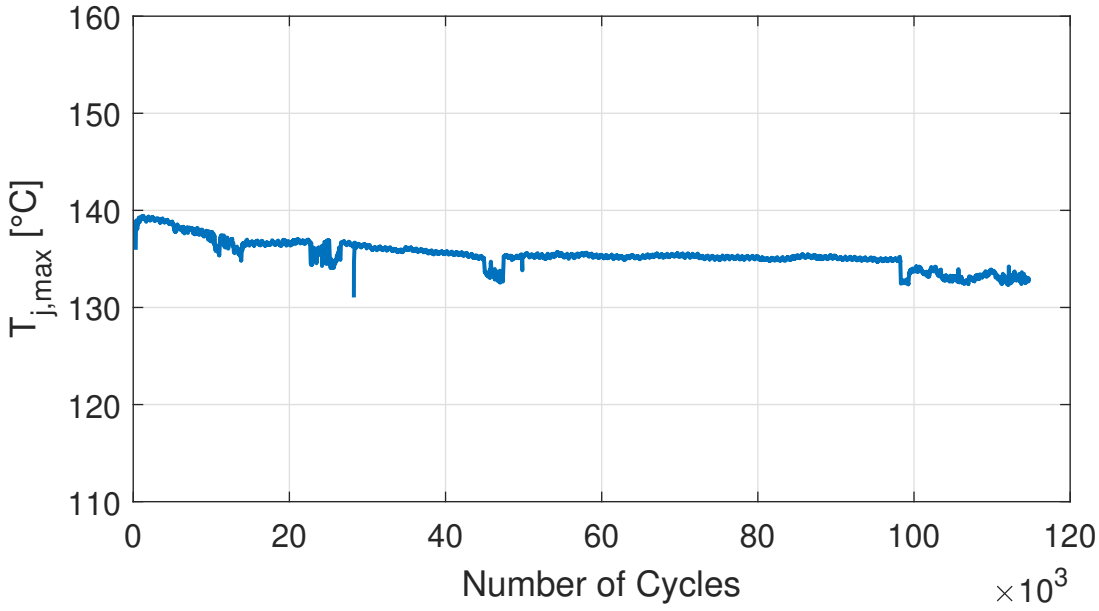

Figure A.1.3 Maximum junction temperature.

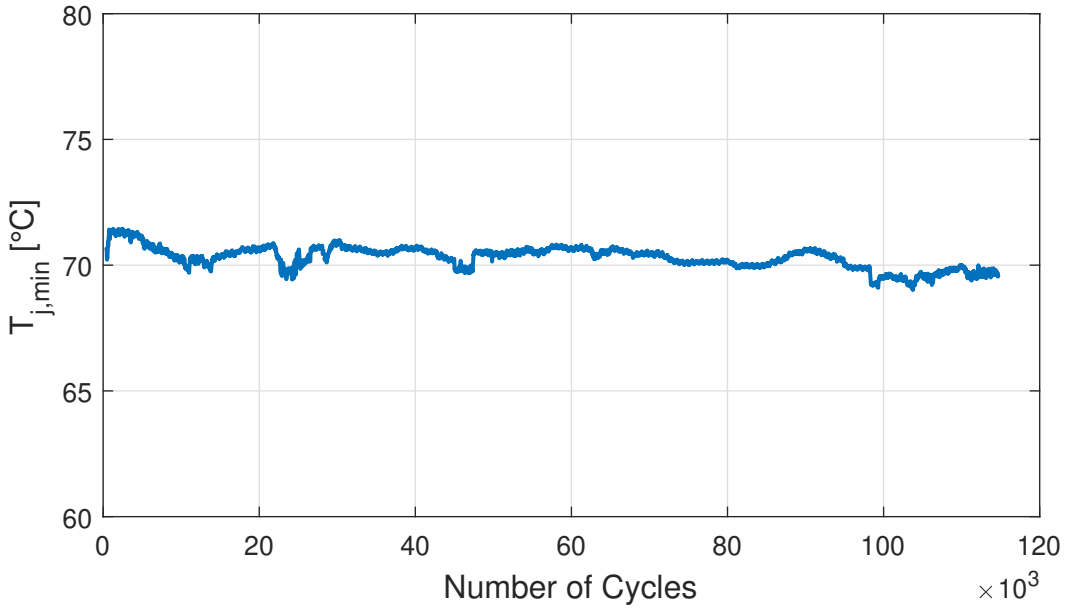

Figure A.1.4 Minimum junction temperature.