Eco Design for Sustainable Power Electronic Converters

Master's Thesis

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Abstract:

Global e-waste is one of the fastest-growing waste streams, with a total of 62 Mt being discarded in 2022 and a projected amount of 82 Mt by 2030. Power electronic converters are not designed with end-of-life dismantling in mind, but instead to reach high efficiency, power density and low cost in production and maintenance which makes them harder to treat when they become e-waste at end-of-life.
In this work, a novel design approach is proposed. The approach is using end-of-life recyclability as a design parameter in a multi-objective optimization algorithm. To enable disassembly and thereby recyclability, several eco-design implementations are developed. These different designs incorporate perforations, as a means to enable the dismantling. Double pulse tests are performed for all designed boards to ensure performance is not compromised. Three-point bending tests are used to estimate the flexural strength of the designs to evaluate the impact of the perforations on the mechanical strength.
The optimization algorithm shows that high values of all the design objectives are achievable in multiple solutions. Differences in the switching energy are witnessed, but these can not directly be tied to the perforations, but appear to be more dependent on component variations. The perforations are estimated to increase the parasitic series inductance of the power loop by 5 pp to 22 pp. The lowest flexural strength is measured to be 21% compared to the conventional non-perforated benchmark design.
Based on these results it is concluded that designs for end-of-life disassembly can be considered as possible solutions for the growing e-waste problem, as the impact on the converters' operation is negligible compared to the ease of disassembly it introduces.

Summary

The global prevalence of e-waste is a growing problem, particularly in the context of the ongoing electrification of consumers' daily lives and the progressive integration of renewable energy sources. In the context of the ongoing climate change, and with the objective of achieving the EU's target of net-zero carbon dioxide emissions by 2050, this issue is of significant concern. The increasing waste stream arising from electronic and power electronic applications and the improper disposal and treatment of e-waste can lead to a depletion of critical natural resources such as rare earth metals. To circumvent the over-exploitation of these critical resources adequate recycling becomes necessary. To combat this increasing problem, this thesis sets out to propose a design approach that can aid in increasing the recyclability of power electronic converters.

As the manufacturers are rarely responsible for the disposal and treatment of electronics and power electronics at their end-of-life, the treatment and recovery of components and materials is accounted to the recycler. Due to directives, such as the Waste from Electronic and Electrical Equipment, instated by the EU, the recyclers have to extract materials from e-waste such as aluminum, iron and copper. They are also responsible for the extraction and treatment of hazardous substances from electronics and power electronic applications, as well as the extraction of rare earth elements.

Although standards and guidelines exist to make the end-of-life treatment easier, most manufacturers do not consider this in the design procedure. They have the freedom, in the design process, to configure their products as their objectives demand it. This translates to a difficult objective for streamlining the dismantling and treatment process at end-of-life. Typically, the designer of power electronic converters has objectives such as power density or efficiency, and cost in mind, when configuring a power electronic converter. However, this approach hardly considers the recyclability of components or materials. Therefore, it leaves room for including an objective such as the recycling rate of each component in the design consideration. By introducing the recyclability design objective, the power electronic converter's design process and objectives can be expanded to make future recyclability feasible. This is done in this thesis to demonstrate how the consideration of the components' recyclability rate affects the other objectives and if this poses drawbacks in terms of efficiency and power density.

This work investigates the introduction of theoretical recyclability in the design process of a specific power electronic converter. Multi-objective optimization is utilized for this analysis. A multi-objective optimization algorithm is developed based on a three-phase half-bridge inverter with an LCL-filter designed for infeed to the grid from a residential-scale PV plant. In this process, the required electrical models for the optimization algorithm are introduced. Switching loss models for three-phase half-bridge inverters and LCL-filters developed in [1] and [2] are utilized and the magnetic design of the LCL-filter is expanded upon. The DC-link capacitance required to handle both fast transients in the switching frequency range and slow unbalances at

fundamental frequency level is presented. The algorithm is developed to sweep a generated component database and calculate the efficiency, power density and recyclability of all the different combinations. Different switching frequencies are swept to obtain all possible design combinations of the components for the use in the three-phase half-bridge inverter. A Pareto optimality algorithm is developed to find the optimal solution out of all the possible combinations generated, followed by an objective-weighting analysis.
As a result of the multi-objective Pareto optimization, it is seen that recyclability goes hand-in-hand with power density but that efficiency is reduced when the other two increase. However, as the efficiency generally is high only a few percentage points are lost in this design parameter, whereas several tenths stand to be lost if power density and recyclability are prioritized less. Based on this it is found that including recyclability in a multi-objective optimization design approach is possible and it shows that a high recyclability does not harm the other design parameters.

Next the recyclability implementation is concerned in a more practical matter. Several different eco-design implementations are developed, which all consist of a conventional converter layout but with different kinds of perforations added on the printed circuit board. Based on these eco-designs, the electrical and mechanical performances are tested to see how the perforations impact the performance.
Double pulse tests are performed at different current levels to investigate the switching performance of the seven developed boards. It is found that the switching energy of the different MOSFETs tested are more dependent on the component variation than on the eco-design implementation. Furthermore, analysis into the oscillations of the turn-off transients are performed to estimate how the inductance varies among the different implementations. Here, it is seen that the inductance is increased when the perforations are introduced. The inductance tends to increase for the same perforation type when the perforations become more frequent on the board, which is to be expected. However, testing the developed converters at different gate resistances results in slightly different inductance values. However, this can also be explained by the change in parasitic capacitance from increasing the speed of the transients. Based on this it is found that the electrical performance is not noticeable impacted by the introduction of the eco-designs.
Specific test boards are designed for mechanical testing in the form of three-point-bending tests. During these tests, the deformation and the force are recorded until a sudden drop in the applied force is measured. This sudden drop indicates failure as the board's structural integrity is compromised. From these results, the flexural strength is calculated and utilized to compare different implementations of the perforations. The tests show that the flexural strength of the boards is significantly reduced. Furthermore, the tests show that with higher perforation percentages, less force is required to result in a fracture of the printed circuit boards. It is seen that perforations based on fewer and wider holes result in higher strength compared to additional narrower holes with the same total perforation percentages. Based on this, it is found that the structural integrity of printed circuit boards is significantly impacted by perforations. Regarding recyclability and the ease of disassembly at the end of life of the application, this is prudent to implement as the proposed eco-design approach enables more efficient and easier disassembly.

Preface

The following software and hardware have been used during the writing of this report:

- Overleaf for text processing.
- Altium Designer for designing the printed circuit boards.
- MathWorks MATLAB for data processing and calculations.
- Plecs for modeling and simulation.
- Code Composer Studio by Texas Instruments
- Drawio for figure composing.
- Microsoft 365 for data processing and sharing.
- Automeris.io for data collection from datasheets

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Reading Guide

The references are made according to the Institute of Electrical and Electronics Engineers (IEEE) citation style and can be found at the end of the report. Figures, tables and equations are referred to as Figure, Table and Equation, respectively (for example, Table 4.2 refers to the second table in the fourth chapter). This report uses the SI units. The thesis contains seven chapters, which are divided into Introduction, State of the Art, Modeling, Problem Solution, Discussion, Conclusion and Future Work. After the bibliography, appendices are attached with additional information, figures, and tables.

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Acronyms

AI Artificial Intelligence.

BNC Bayonet Neill–Concelman.

CCS Code Composer Studio.
CEAP Circular Economy Action Plan.

DC Direct Current.
DfD Design for Disassembly.
DfR Design for Recycling.
DPT Double Pulse Test.
DUT Device Under Test.

e-waste electronic waste.
EMC Electro Magnetic Compatibility.
EMI Electro Magnetic Interference.
EoL End-of-Life.
ePWM enhanced PWM.
ESPR Ecodesign for Sustainable Products Regulation.
ESR Equivalent Series Resistance.
EU European Union.
EV Electric Vehicle.

IC Integrated Circuit.

LED Light Emitting Diode.

MCU Micro Controller Unit.
MLT Mean Length of Turns.
MMCX Micro-Miniature Coaxial Connector.
MOO Multi-Objective Optimization.
MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

PCB Printed Circuit Board.
PEBB Power Electronic Building Blocks.
PEC Power-Electronic Converter.
PV Photovoltaic.

RES Renewable Energy Sources.
RMS Root Mean Square.

SiC Silicon Carbide.
SMD Surface-Mount Devices.
SPWM Sinusoidal Pulse Width Modulation.

TIM Thermal Interface Material.

VSI Voltage Source Inverter.

WEEE Waste from Electrical and Electronic Equipment.

Nomenclature

Symbol	Explanation	Unit
A_1	Inductance factor	$\frac{\text{nH}}{\text{turn}^2}$
A_{Cu}	Total copper winding area	m^2
A_{e}	Effective core area	m^2
A_{p}	Area product	m^4
$A_{\text{q,req}}$	Required area product	m^4
A_{w}	Window area	m^2
$A_{\text{w,e}}$	Window area estimate	m^2
$A_{\text{w,toroid}}$	Window area	m^2
A_{wire}	Total wire cross-sectional area	m^2
B	Magnetic flux density	T
B_{max}	Maximum magnetic flux density	T
$B_{\text{max,fund}}$	Maximum magnetic flux density at fundamental frequency	T
$B_{\text{max,sw}}$	Maximum magnetic flux density at switching frequency	T
B_{pk}	Peak magnetic flux density	T
B_{sat}	Saturation magnetic flux density	T
b	Width	mm
C	Capacitance	F
C	Core dimension	m
C_{DC}	Capacitance of the DC-link Capacitor	F
$C_{\text{DC,slow}}$	Capacitance of the slow DC-link Capacitor	F
C_{DPT}	Required DC-link capacitance	F
D	Duty Cycle	–
D	Core dimension	m
d_{wire}	Diameter of a wire	m
$\frac{di}{dt}$	Infinitesimal change in current over time	$\frac{\text{A}}{\text{s}}$
Δi	Change in current	A
$\frac{\Delta i}{\Delta t}$	Difference in current over a difference in time	$\frac{\text{A}}{\text{s}}$
E	Core Dimension	m
E_{sw}	Switching energy	J
$F(x)$	Cost Function	–
F	Force	N
$f(i)$	Objective Funtion	–
f	Frequency	Hz
f_{fund}	Fundamental frequency	Hz
f_{sw}	Switching frequency	Hz
f_{g}	Grid frequency	Hz
f_{r}	Resonance frequency	Hz
f_{sw}	Switching frequency	Hz
h	Height	mm

Symbol	Explanation	Unit
I	Current	A
I_{ph}	Phase current	A
I_{pk}	Peak current	A
I_{rec}	Reverse recovery current	A
I_{S}	Grid Current	A
I_{test}	Test current	A
J	Current density	$\frac{\text{A}}{\text{m}^2}$
K_{u}	Utilization factor	–
K_{c}	Empirical constant	$\frac{\text{W}}{\text{m}^3}$
k	Duty cycle	–
L	Length	mm
L	Inductance	H
L_{ramp}	Ramping inductance	H
L_{s}	Total series inductance	H
l_{e}	Effecetive magnetic path length	m
l_{wire}	Length of wire	m
M	Core dimension	m
MLT	Mean length of turns	m
M_{max}	Maximum moment	Nm
m_{i}	Modulation index	–
m_{k}	Mass of the k^{th} material	g
m_{tot}	Total mass of the materials comprising the equipment	g
N	Number of turns	–
N_{wire}	Number of wires	–
P_{avg}	Average power loss	W
P_{cond}	Conduction losses	W
$P_{\text{Cu,L}}$	Conduction loss	W
P_{fe}	Power Loss per unit volume	$\frac{\text{W}}{\text{m}^3}$
$P_{\text{fe,fund}}$	Power Loss per unit volume at fundamental frequency	$\frac{\text{W}}{\text{m}^3}$
$P_{\text{fe,sw}}$	Power Loss per unit volume at switching frequency	$\frac{\text{W}}{\text{m}^3}$
P_{max}	Maximum power	W
P_{tot}	Total power loss	W
$P_{\text{unbalanced,max}}$	Maximum expected power imbalance between phases	W
p_{KoolMu}	Power per unit volume for Kool Mu core	$\frac{\text{mW}}{\text{cm}^3}$
p_{NeuFLux}	Power per unit volume for NeuFlux core	$\frac{\text{mW}}{\text{cm}^3}$
p_{N87}	Power per unit volume for N87 core	$\frac{\text{mW}}{\text{cm}^3}$
$p_{\text{Si-Fe}}$	Power per unit volume for Fe Si core	$\frac{\text{mW}}{\text{cm}^3}$
p_{XfLux}	Power per unit volume for Xflux core	$\frac{\text{mW}}{\text{cm}^3}$
R	Resistance	Ω
R_{cyc}	Calculated recycling rate	%
$R_{\text{cyc,k}}$	Recycling rate of the k^{th} material	%
R_{ds}	On-resistance	Ω
$R_{\text{ds,avg}}$	Average on-resistance	Ω
R_{HS}	Heatsink resistance	$\frac{\text{K}}{\text{W}}$
R_{JC}	Junction to case thermal resistance	$\frac{\text{K}}{\text{W}}$
R_{l}	Resistance	Ω
r_{wire}	Resistivity of a wire	Ωm

Symbol	Explanation	Unit
R_{TIM}	Thermal interface material resistance	$\frac{\mathrm{K}}{\mathrm{W}}$
R_0	Calculated recycling rate	Ω
R_1	Calculated recycling rate	%
S	Section modulus	mm^3
T_{A}	Ambient temperature	°C
T_{test}	Test time	s
t_{s}	Settling time	s
V	Voltage	V
V_{cf}	LCL-filters capacitance voltage	V
V_{DC}	DC-voltage	V
V_{ds}	Drain-source voltage	V
V_{gs}	Gate-source voltage	V
$V_{\mathrm{gs,th}}$	Threshold gate-source voltage	V
$V_{\mathrm{gs,miller}}$	Miller plateau gate-source voltage	V
v_{L}	inductor voltage	V
$V_{\mathrm{m,AC}}$	Desired grid voltage based on DC-link voltage and modulation index	V
V_{ph}	Phase voltage	V
V_{o}	Output voltage	V
$\hat{V}_{\mathrm{tri}}$	Triangular voltage	V
$\hat{V}_{\mathrm{ref}}$	reference voltage	V
V_{S}	Grid voltage	V
V_{s}	Source voltage	V
V_{o}	Output voltage	V
W_{a}	Window area	m^2
W_{m}	Energy stored in inductor	J
W_{h}	Window height	m
W_{w}	Window width	m
w_i	Weighting coefficient	–
Z_{b}	Base impedance	Ω
α	Empirical constant	–
β	Empirical constant	–
μ_{r}	Relative permeability	–
μ_0	Vacuum permeability	$\frac{\mathrm{H}}{\mathrm{m}}$
μ_{core}	Core permeability	$\frac{\mathrm{H}}{\mathrm{m}}$
θ	Phase angle	°
φ	Power factor	°
ω_{o}	Angular frequency of the grid	rad/s
ω_{res}	Angular resonance frequency	rad/s
σ_{c}	Compressive strength	MPa
σ_{t}	Tensile strength	MPa
σ_{f}	Flexural strength	MPa

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1 Introduction

This chapter introduces the background of this thesis, by expanding on the current problems of electrical and electronic waste. It gives an overview of current and planned political directives and legislations to combat the challenges. It then reflects how these challenges can be addressed, which ultimately leads to the problem formulation and the objectives for this thesis' and its limitations.

1.1 Motivation

The use of power electronic applications will rise in the following years due to the required electrification for meeting the net-zero emissions goal for 2050. Electrification is seen as a way of decarbonizing different sectors. The use of Power-Electronic Converters (PECs) is required for most of the applications, such as the transportation and energy sectors. This results in a drastic increase in power electronic applications, with a lifetime of these applications typically between 20 to 25 years, meaning that by 2050 the PECs, which are produced today, will reach the end of their lifetime or will be decommissioned by then. [3]
The waste resulting from decommissioned PECs will therefore add to the growing waste stream of electronics.

In 2022, around 62 Mt of electronic waste (e-waste) was produced worldwide, and it is projected that by 2030, around 82 Mt of e-waste will accumulate annually [4]. The increasing amounts of e-waste urge a shift in the economy to a more sustainable and circular approach to handle electric and electronic equipment [5]. Concerns exist regarding the scarcity of critical natural resources and the limited planetary availability of these resources as well as the extraction and consumption of raw materials, water and energy [6].
In line with the energy transition, a shift in the current economy needs to happen in order to avoid the depletion of those critical natural resources. This means that the linear lifetimes of converter systems have to change and therefore, the utilized components must be reused or recycled in various ways to achieve a circular economy. [3]

To enable this economic shift, adequate legislations need to be instated so that manufacturers adopt the proposed shift to a circular economy instead of maintaining the current linear one. Therefore, the European Union (EU) has introduced the Circular Economy Action Plan (CEAP) as one of the key pillars of the European Green Deal, Europe's new agenda for sustainable growth in order to achieve climate neutrality by 2050. The CEAP contains legislative and non-legislative measures, which target product design, promote circular economy processes, encourage sustainable consumption, and aim to ensure that waste is prevented and the resources used are retained within the EU economy for as long as possible [7]. Among the key targets of the CEAP are sectors that use the most resources and where the potential for circularity is high, such as electronics, batteries and vehicles, packaging, plastics, textiles, construction and buildings, food, water and nutrients [7]. Furthermore, it is aimed to empower consumers

through initiatives such as the right to repair, as well as to increase the use of recycled materials, while also making products more recyclable. Yet, the product's reliability ought not to be affected by this increase in recyclability.[7] As a part of the CEAP, the Ecodesign for Sustainable Products Regulation (ESPR) proposes a legislative framework, which sets out targets on how the objectives defined by the CEAP can be realized. It extends eco-design requirements, such as improving product durability, reusability, upgradability and repairability, while also enhancing the possibility of product maintenance and refurbishment. Additionally, the products have to become more efficient and resource-efficient with the increasing use of recycled materials and making products easy to remanufacture and recycle. Furthermore, an objective of the ESPR is to implement a digital product passport, which indicates the product's environmental, sustainable, repairable and recyclable score in a new proposed system. [8]

The possibility of reusing components will reduce the use of resources the most. Recycling components, to obtain the raw materials from which they are made of, requires energy in the extraction and remanufacturing. However, studies show that recycling the raw materials, metals and plastics, will result in energy and emission savings [9][10][11]. Thus, the circular economy can be achieved through different means.
In the current landscape of electronics, the main problem with recycling is that the electronic equipment is difficult to disassemble. As most electronic equipment consists of components soldered or screwed to a Printed Circuit Board (PCB), the reuse of components requires manual removal with several different kinds of tools [5]. Recycling electronics is an even longer process as the products first have to be shredded, followed by many different sorting methods to separate different metals, plastics and other contents. After the materials are separated, each material is then ready to be refined once again and sold to manufacturers to make new products.[12]

To address these End-of-Life (EoL) challenges, the EU implemented the Waste from Electrical and Electronic Equipment (WEEE) directive. This is particularly important because e-waste consists of a complex mixture of materials, some of which are hazardous and can pose significant environmental and health risks if improperly managed. It also focuses on preventing e-waste, mandating proper collection and treatment, and setting targets for the collection, recovery, and recycling of e-waste. The directive also helps EU member states combat illegal e-waste exports by strengthening enforcement mechanisms. One of its key objectives is to promote the efficient use of resources and the recovery of secondary raw materials through reuse, recycling, and other recovery methods [13].

However, even with such regulations in place, achieving efficient recycling remains challenging if products are not designed with EoL disassembly in mind. To circumvent the inherent difficulties of disassembly, the design process itself can be adapted, enabling future dismantling of the PEC after the end of its lifetime. This design philosophy is known as Design for Recycling (DfR) or Design for Disassembly (DfD).
This results in the necessity to consider the eco-design methods, DfR and DfD, when designing a PEC which is to be sold in the EU.

1.2 Power Electronic Applications

As previously mentioned PECs are difficult to repurpose and recycle. As PECs are an integral part of the electrification, the design processes must change to accommodate the CEAP.

The current standard of PEC design is optimized to yield the highest efficiency and/or power density at the lowest cost, depending on the application[14]. Due to this, there is little to no room for the design procedure to take into account the recyclability of the PECs' components. Furthermore, discarded PECs have a high value in terms of functioning components and resources. [6]
This necessitates that the recyclability of PECs has to become an essential part of the design, which the CEAP proposes through lifetime extensions of components and interconnections by giving them multiple life cycles [5]. Thus, enabling further reuse of the components becomes an essential part of the PEC's design.

One way of introducing recyclability of PECs can be incorporated already in the design procedure of the PCB. Some manufacturers are starting to come up with guidelines and practices to make recycling easier. Some of these practices include reducing the number of fasteners or connectors used to hold the electronic equipment connected, making the boards that contain the circuits smaller, meaning they require less material to manufacture, reducing the mixing of materials, and excluding adhesives in the products [15]. With these practices in mind, a designer is able to come up with designs that are easier for recyclers to take apart either for reuse, refurbishment, or recycling.

One way to increase the reusability and recyclability of PECs is to include a modular approach such as Power Electronic Building Blocks (PEBB) in the design phase. The advantage of implementing the PEBB approach is that if one or multiple components fail, they can be replaced by either swapping the faulty components or replace the parts of the PCB with the defective components with intact working ones. This can be done in extensive ways with many levels of modularity in one system while also allowing for upgrading of existing PEC systems with advanced technology [16]. The PEBB approach will, in most cases, result in additional fasteners or connectors. However, repair and refurbishment becomes a possibility and the damaged parts with fasteners can be removed and sent to recycling. This therefore works around the practice. One of the setbacks from the modular approach is that increased interconnections might impact the performance of the equipment in both a mechanical and electrical manner. Furthermore, additional components like the required connectors will add to the required footprint of the PECs, reducing the power density.

Another method, in the design process of the PCB, is to include cut-outs to make future extraction or breaking of component areas easier. This leads to not only a higher component recycling rate, through enhanced sorting, but also allows for intact components to be reused in other or the same applications after the end of the first lifetime. In this design approach, it is desired to lump similar components into the same break-away areas, which might increase the required size of the PCB. Apart from this, the design approach is capable of incorporating the same design practices as normal PCB designs are proposed to follow. One of the clear benefits

to this approach is that it is possible to include it in existing designs without having to change the existing layouts and thus neither the products the altered PCBs go into.

As there is benefits and drawbacks for both approaches, it is decided in this thesis to continue working with the cut-out approach as this appears to be the less investigated approach.

1.3 Problem Formulation

Research into how electronics can be designed today, enabling higher recycling yields, are of great focus. However, less emphasis has been put on power electronics so far. Therefore, an investigation into methods of implementing eco-friendly designs in PECs and these methods' impact on the performance of the PEC itself is crucial. This thesis aims to conduct a investigation of this matter. Furthermore, the investigation will look into the prospect of integrating material recyclability in the design process, to see how the changing the recyclability impacts the efficiency and power density of the system.
This leads to the following problem statement:

Problem Statement

How can power converters be designed for future disassembly at their EoL, while taking into account the optimality trade-offs between recyclability, efficiency and power density?

Objectives:

- Develop and use a multi-objective optimization tool to get an optimal set of specifications regarding efficiency, power density and recyclability for a PEC case study.
- Develop different eco-design implementations enabling disassembly and recyclability of PECs.
- Test the electrical and mechanical performance of the different eco-design implementations to evaluate the possible trade-offs between recyclability and performance.

Limitations:

- Component recyclability is modeled. However, the recyclability of capacitors are not taken into account. The capacitors are chosen based on the smallest viable volume.
- Simple calculations regarding steady-state heatsink requirement.
- No thermal modeling of the used components.
- Conduction in first and third quadrants are assumed to produce the same conduction loss, as the same gate voltage is applied when conducting in both quadrants.
- The magnetic designs are performed without custom air gaps being inserted into cores.

Case Study

The case study of this project is split into two parts. The first part focuses on a component-model-based design approach for a full converter and investigates the optimality trade-offs between efficiency, power density, and recyclability. The second part focuses on how different design implementations, allowing recyclability at EoL, impact the performance of the investigated PEC.

The first part of the case study revolves around the optimization problem. In the optimization problem it is decided to use a common power converter topology as the basis. Many common power converters make use of the half-bridge leg configuration for some, if not all, of their switching devices. This includes half-bridge inverters, full-bridge inverters, t-type inverters, synchronous buck converters, synchronous boost converters, resonant converters, and totem-pole rectifiers. This means that the configuration is used in DC/AC, DC/DC, and AC/DC converters. With this in mind, this thesis sets out to develop and perform an optimization analysis on a PEC in which this configuration is used and implemented to test the performances. Based on this, a three-phase inverter for a residential Photovoltaic (PV) application is investigated.

The second part of the case study is developing and testing different eco-design implementations. These different implementations are based on a half-bridge configuration, as it is the foundation of the inverter. Here, the different designs will have the same dimension constraints, and the implementation of the eco-design aspect will vary.
It is noted that despite this work revolving around the half-bridge topology, the work is translatable to other topologies without any apparent problems.

As the output of the optimization problem is used to analyze how including recyclability as a design objective impacts the different design objectives, the analysis of how the eco-design implementation impacts performance does not have to be carried out on the same PEC. If instead a comparative study is performed, the two analyses' results can be used in tandem to see how a full system is impacted. The output of the optimization analysis is used to the largest possible extent in the comparative study.

2 State of the Art

In order to answer the previously formulated problem statement, this chapter gives an overview of practices in electronic applications, design procedures, and PEC performance testing.
First, some of the common design methodologies for PECs are discussed. Secondly, the procedures implemented in consumer electronics with the intention of increasing the circularity of products are introduced. As a third part, some of the aspects of the circularity design choices for consumer electronics are mirrored in the design of PECs. This is to see what methods might be applicable in this category. As a fourth and last part, the specific case study for this thesis is introduced along with the required testing to see the impact of the circularity design changes on the different performance metrics of a PEC.

2.1 Designing Power Electronic Converters

This section concerns the process surrounding the design of PECs, the desired objectives are reintroduced and discussed, and the most important ones are chosen for this project. Following this, the process of optimization is introduced as a tool for use in the design process.

2.1.1 Design Parameters

Depending on the application, different design aspects or objectives are often considered. The conventional design objectives are mentioned in Section 1.2 and are efficiency, power density and cost.
When designing residential PV inverters, a high efficiency is often the most desirable factor, however, if the cost is too high or the inverter is too large for installation, the consumer will find another more fitting product. For large power-generating plants, the efficiency is very important and the power density and the cost can be weighted lower due to the large power flowing through the inverter, making up for the increased cost. Inverters for drives are used in many different applications such as Electric Vehicle (EV), heavy machinery, and pump drives. Especially when designing an inverter for EV applications, the efficiency and power density are prioritized. This is because the efficiency and power density are directly correlated to the range per charge, where the high power density will result in a decreased weight. For heavy machinery, the power density is of less importance, but the cost and efficiency are more desirable design parameters. For pump drives, almost all combinations are possible depending on residential or industrial applications and also depending on whether the pump is installed below or above ground [17].

As previously mentioned, in this thesis, the cost is not considered. For the design of a residential PV inverter efficiency is highly valued. Power density is also valued, as this directly impacts the required amount of material and from an environmental perspective this is desired to be minimal. Furthermore, a metric evaluating the recyclability objective is also introduced to investigate how the variation in efficiency and power density correlates with the possibility of regaining materials after the ended life of the equipment.

To achieve a design that balances these objectives, the components cannot be selected arbitrarily. Instead, a structured approach is required to systematically evaluate trade-offs and identify the optimal design solution. This is where optimization techniques become valuable. By leveraging an optimization algorithm, the design process can be guided toward the most suitable component selection and system configuration. The following section introduces optimization as a design tool, outlining its advantages over conventional rule-based methods and detailing the steps involved in the optimization process. [14]

2.1.2 Optimization as a Design Tool

When developing PECs, a typical design procedure follows the steps depicted in Figure 2.1. Here, the utilization of an optimization approach offers advantages over rule-based design approaches. [14]

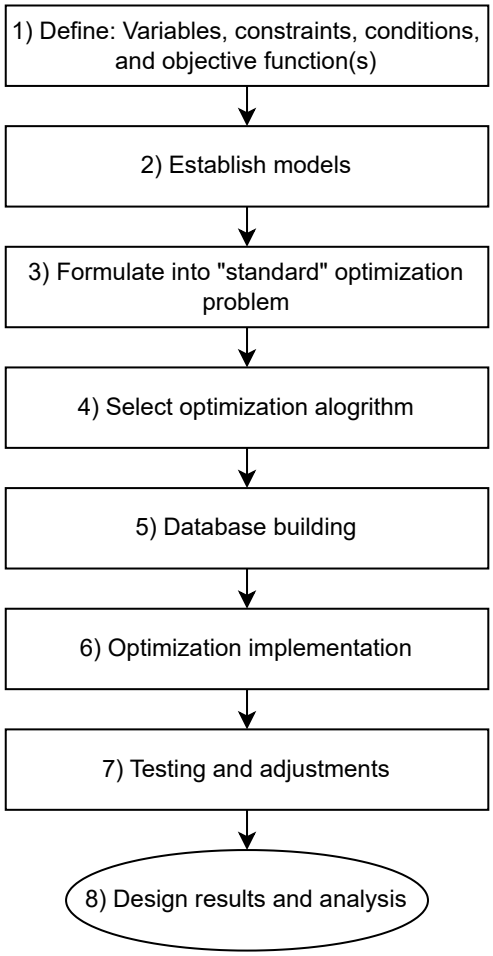


Figure 2.1 Optimization steps. [14].

Depending on the type of application, trade-offs can or must be made in favor of one or more objectives over the other. One method of the optimization approach is to use single-objective optimization while constraining the other objectives. The other method considers multiple objectives and is denoted as Multi-Objective Optimization (MOO) method. [14]
The MOO method includes all objectives and sums them together with weighting coefficients as shown in Equation (2.1). The weighting coefficients w_i are selected, corresponding to the requirements, for example, if efficiency is prioritized, then the weighting coefficient is higher for efficiency than for the other objectives. A cost function $F(x)$ is then defined based on the different objectives. The solution to the MOO maximization problem is then found as the configuration which results in the largest evaluated cost function. This is seen in the equation below: [14]

$$\max F(x) = \sum_{i=1}^{m} w_i \cdot f_i(x) \tag{2.1}$$

$f_{\mathrm{i}}(x)$ is the function of the respective i^{th} part of the total amount, m, of objective functions. Thus, Equation (2.1) is used to find an optimal design solution for a given set of weights.
For analysis, where multiple solutions are of interest, the Pareto front can be applied. This concept logs all possible combinations of design variables in the feasible design space D through the objective function into the feasible performance space P. The Pareto optimal points consist of dominating points only. For the following description it is noted that this thesis works with maximization. Two conditions have to be met for domination. The first is that for a point, f, to be dominating no other point, f^*, in the set has design variables which are larger than f's own. The second is that f has to have at least one design variable which is larger than that of

the same variable of f^*. These two conditions state that f has to be partially bigger than f^* in all objectives, and also that f has to be strictly better than f^* in at least one objective. [14] The conditions are visualized in the equation below:

$$f_i \geq f_i^*, \quad i = 1 : k \tag{2.2}$$

$$f_i > f_i^*, \quad i = 1 : k \tag{2.3}$$

The MOO method in conjunction with the Pareto front is thus applicable to obtain a series of optimal design solutions. The Pareto front is a commonly used tool by PEC designers to obtain an optimal configuration for a specific application [14].
Having covered the theoretical basis for PEC design, the focus now shifts towards the practical considerations in the design process.

2.1.3 Layout Considerations

This section provides an overview of standard design practices and constraints relevant to design of PCBs involved in this study. It outlines general PCB design principles, commonly applied in power electronic converters, while briefly explaining key aspects. Table 2.1 summarizes key clearance requirements for the PCBs, along with the trace widths for signal paths and high-voltage planes.

Table 2.1 Summary of clearance requirements and trace widths for the PCB.

Parameter	Implementation	Distance (if required)
Keep-out	Areas around Direct Current (DC)+ potential	5 mm
Trace width	DC+ plane	As much copper as possible
Trace width	Minimal width for signal traces	0.5 mm
Trace width	Maximal width for logic power supply	2 mm
Distance	Minimum between high-voltage planes	2.6 mm
Distance	Gate driver component spacing	As compact as possible

The key electrical and mechanical design aspects of the prototype PCBs are outlined below. From an electrical perspective, a fundamental consideration is ensuring reliable power delivery to all active components, maintaining stable current and voltage levels. To minimize parasitic inductance and capacitance, the PCB layout is designed to be as compact as possible, keeping the inductance loops formed by components and traces as small as feasible. To prevent crosstalk and electromagnetic interference, it is important to maintain adequate separation between signal and power planes. Signal traces are carefully routed to minimize overlap with power planes, and where connections to the switching devices are required, the trace lengths between the gate driver circuits and the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)s are kept as short as possible. Where signal or power traces are required to cross, they are arranged to do so perpendicularly to reduce coupling effects.

Clearance between traces and planes, with different potentials, must be sized adequately to prevent discharges under operating conditions. It is noted that creepage distances have not been explicitly addressed in this project. In relation to the clearance between high-voltage planes, it is worth noting that a separation of approximately 2.6 mm, such as between the DC+ plane and the

switch-node plane, is sufficient to prevent electrical discharges. Ground planes are designed with as much copper as possible, which improves both current distribution and thermal dissipation, and reduces parasitic inductance. For high-current traces and planes, sufficient current-carrying capacity is ensured through appropriate trace sizing. To further enhance current handling and heat dissipation, vias can be placed strategically to increase the PCB's effective cross-sectional area by utilizing multiple layers of the PCB.
In terms of mechanical aspects, components are spaced to avoid mechanical interference, while keeping trace lengths short to maintain electrical performance. For thermally stressed components such as MOSFETs, heatsink are utilized.

2.2 Sustainability Status in Consumer Electronics

To give an overview of the current landscape of consumer electronics and electrical equipment, this section presents the general status of e-waste, how electrical equipment is recycled and the observed trends for consumer electronics. It also introduces the consumers and political demands for more refurbished products. Furthermore, it introduces a technique used to ease the manufacturing process of electronic and electrical products that make use of PCBs, which can be mirrored into the dismantling process.

2.2.1 Status on E-waste

As elaborated on in Section 1.1 e-waste is a growing problem. In 2022 only 22.3 % of the total global e-waste of 62 Mt, equaling 13.8 Mt, was formally collected and recycled. In this context, formally refers to e-waste being collected through designated collectors, who send it to specialized recycling facilities. It is noted that from the formally worldwide recovered e-waste, the 13.8 Mt, 6 Mt of metals were extracted in an environmentally safe way. However, during this process, around 1 Mt was lost. To achieve higher recycling rates, proper separation and pre-treatment of e-waste is necessary. However, this is not a common practice in global e-waste management. [4]

2.2.2 How Recyclers Disassemble

Recyclers have many tools available for enabling dismantling of e-waste. They have access to a variety of hand tools, such as side-cutters, heat guns, soldering stations, and pliers [18]. Automated machines such as automatic component dismantling machines, granulators and shredders, and electromagnetic separators are also used [18]. Recent development includes Artificial Intelligence (AI)-based disassembly systems that use robots for disassembly [19], [20]. Automated recycling and sorting are only feasible for larger-scale operations, such as larger recycling plants. Whereas AI-based dismantling is currently limited to research and laboratory settings, as the cost of these machines and systems is high. [19] [20] However, a large fraction of the recycling processes nowadays is still performed by manual labor as electronics and power electronics PCBs do not have standardized configurations. [21] [22] Thus, it becomes the recyclers' responsibility to separate hazardous materials and recover components, no matter the degree of difficulty encountered during disassembly. [19] This reflects directly onto the design phase of PECs, where considerate choices in the layout configuration can reduce the amount of time and effort spent during the disassembly. [19]

2.2.3 Movements for Circular Consumer Electronics

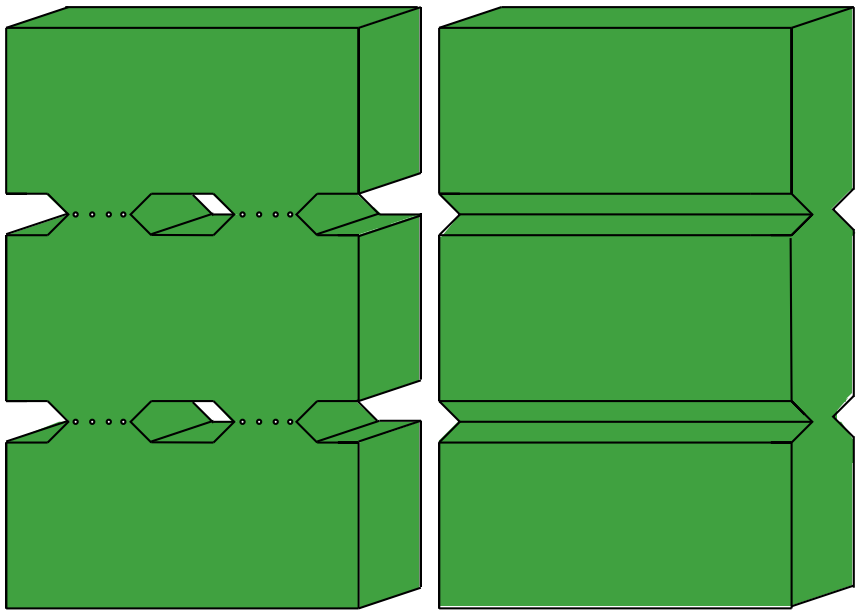
Growing global attention to climate change and sustainability by consumers, alongside political legislation and initiatives, demand technological solutions to promote a more circular economy. This is evident in trends like the rising demand for reusable and refurbished electronic products [23]. However, despite these positive signals, global material circularity has declined, from 9.1 % in 2018 to just 7.2 % in 2023 [23] [24]. Nevertheless, certain initiatives and companies are making tangible progress toward a circular approach in consumer electronics. Manufacturers such as Fairphone, Framework, and Dell Technologies have introduced modular devices and are continuously refining this strategy. Another trend is the increasing global demand for second-hand products. Fueled by rising environmental awareness, many online and physical retailers are now offering both new and refurbished products. [23]

According to the 8th edition of the Barometer issued by Recommerce, which surveyed citizens in 13 European countries, it concluded that almost 46 % of Europeans have already bought a second-hand smartphone. These have either been sold by professional retailers or by private individuals. The survey also shows that the trend of buying second-hand consumer electronics is still growing compared to the previous year, with 43 %. It also concluded that the refurbished smartphones remain an alternative for Europeans. As a matter of fact, around 55 % of citizens declared that they will buy refurbished smartphones in the future. According to a study conducted by Recommerce and McKinsey concluded that the European market for refurbished consumer electronic products can double in size between the years 2023 and 2029. [25]

Furthermore, big companies such as Vinted recently moved from second-hand clothing to also including electronics in 2024. On the other hand, companies such as the French company Back Market connects refurbishers with consumers through its online platform, with the primary traded goods being electronics and electric appliances. Another example of such a company is UK's Curry, employing over 1000 repairers. But also big tech companies like Samsung recognize the potential, offering refurbished smartphones under Samsung's "Certified Re-Newed" program. But also other tech companies like Miele and Dyson are running refurbishing projects in many European countries. [26]

2.2.4 Production Techniques with Potential for use in EoL Treatment

In the manufacturing process of PCBs for electronics, some processes are utilized for separating PCBs into smaller pieces. This is done for big panels of the same individual layouts, multiplied and spread over a larger panel to increase productivity. As these processes are developed for enabling the separation of PCBs without damaging components, it is interesting to see if these can be used at the end of the electronics' lifetime to reduce the amount of e-waste by enabling easier recycling.
Depanelizing techniques and tools are standard methods for mass-producing manufactures. Specific tools and techniques are selected based on the production scale, precision requirements, and mechanical stress tolerances of the components on the PCBs. For small-volume production, depanelizing is often performed manually. This can involve separating the boards along v-grooves or mouse-bite perforations. The two techniques are illustrated in Figure 2.2.



(a) **(b)**

Figure 2.2 Implementation of different breakage lines used for depanelization : a) mouse-bite perforation, b) v-grooves.

A cost-effective and fast method of depanelization for prototypes or smaller batches, consist of snapping the PCB at the breakage line. However, it may introduce mechanical stress that can damage sensitive components near the separation lines or even damage the PCB unintentionally. In medium to high-volume production, manufacturers rely on automated depanelizing machines to separate the boards at the breakage lines. These machines use tools such as: [27]

- Rotary cutters (pizza cutters or v-cutters), for scoring and snapping v-grooved boards.
- Routing/milling machines, which use high-speed spinning bits to cut out PCBs with minimal mechanical stress.
- Laser depanelizing, non-contact method for high precision applications, especially where component density is high.
- Punching or die cutting, suitable for boards with fixed repeatable geometries.

Each of these separation methods can be configured for different widths of cut-outs, such as circular and elongated implementations, denoted as slots, and tolerances, depending on the design of the panel. Selection of the applied methods depends not only on the board design but also on the desired quality and cleanliness of the edges, as well as minimizing strain on components, which is essential for product reliability.[27]

2.3 Implementing Circular Design Choices in PECs

As elaborated in Section 2.3.3, the current standard of designing PECs hardly considers the recyclability at the end of the PEC's lifetime. In order to implement recyclability into the design procedure, a novel approach for the design process is investigated in this thesis.
In this section, the method and trends presented in Section 2.2.4, for making consumer electronics more sustainable, is evaluated for the use in the design of sustainable PECs.

2.3.1 Refurbished, Repurposed and Right to Repair

For consumer electronics, there is a large refurbished market as mentioned in Section 2.2. This can also be the case for power electronics if faulty power electronics are taken in, repaired, and resold at a lower price. One of the reasons this can be possible is that when PECs malfunction, it will often be because of single components malfunctioning. Then depending on the type of failure other components might be damaged but it might also be the case that all other components are left unharmed. For PECs it is often the switching devices and the capacitors which cause failures while other components, such as inductors, remain functioning [28][29]. With this in mind companies, which do refurbishments, can change out these common causes of failures and then resell the otherwise e-waste for a lower price, than a new device, and give the PEC a longer span.

Another option is harvesting functioning components out of broken PECs and repurposing them in other devices. This can be done in tandem with the refurbishment introduced above to avoid putting brand-new components into equipment that might only have a few operating years left. Repurposing can also be performed before failure occurs. For systems that have been worn for some time, it can be an option to downgrade the device to a lower power rating and thus increase the remaining life of the device. This is already done in the power grid with power transformers being relocated to extend the life time and to avoid extended downtime [30].
The economic aspect of doing refurbished or repurposed PECs are not investigated in it self in this work and it might have to be subsidized to be profitable.

When it comes to the right to repair, as part of the legislative approach of the CEAP, the subject of power-generating plants starts to become a gray zone. It is difficult for most consumers to repair their devices while still maintaining the rules and regulations concerning these types of equipment. The main difference between consumer and power electronics is the risk to human life and the impact a fault can have on the surrounding grid. As PECs have a higher power rating than consumer electronics, there is a larger risk of death if an accident occurs involving humans. Therefore, it is assumed in this work that right to repair, for smaller residential-level power plants, can only be realized if PECs start to utilize a PEBB-based design approach where replacement blocks can be purchased.

2.3.2 Mouse-Bite Perforations and V-Grooves

While mouse-bite perforations and v-grooves are primarily used by manufacturers for depanelization, they can also be applied to facilitate the disassembly of PECs at the end of their operational life. In this context, the objective shifts from preserving the integrity of the PCB to using it as a guide for targeted breaking or cutting, thus enabling the efficient separation of components for reuse or recycling. By implementing these methods, the use of tools can be reduced and thereby also the potential exposure to harmful dust particles. PCBs are commonly made out of fiberglass, which releases tiny fiber particles when cut, sanded or drilled. These can cause respiratory issues and skin irritation. The proposed utilization of mouse-bite perforations or v-grooves can significantly reduce the need for tools and thus also the release of dust particles. [31]
This approach proposes integrating perforations into the PCB of a PEC with the explicit aim

of future disassembly. Looking ahead to the EoL, the system can be more easily dismantled by breaking apart grouped sections of the PCB. While still soldered to their respective board sections, these component groups can be sent to specialized recyclers or refurbishers, who can recover some or all of the components for potential second-life applications. Alternatively, the PEC can be shipped to recycling facilities, where the pre-defined perforations will simplify the separation and pre-treatment processes based on material composition. Furthermore, desoldering components on smaller, separated board sections becomes easier due to the reduced thermal mass, particularly in areas where large current-carrying traces or planes are present. By dividing these areas into smaller segments, less heat is required to desolder components because less heat is required to bring the copper to the temperature where the solder becomes liquid, thus improving the efficiency of manual or automated recovery processes.

To make the novel process easier for designers to implement, it is suggested that all electrical traces are to be routed before the perforations are introduced. The proposal is that a designer have to be able to draw a perforation line in the design software and then specify what perforation is desired, followed by what perforation percentage have to be applied. After this, the designer can move or remove the perforations that will compromise the circuit. Altering the circuit by implementing the perforations requires tests to see how the performance is impacted.

2.3.3 Recyclability as a Design Parameter

In order to include recyclability as one of the multi-objective design parameters, it needs to be defined how recyclability can be quantified for in the design. This is done by a literature review to obtain the recycling rates for all used materials. A material database is then generated to include the recyclability of the materials.

A method for calculating the recyclability of electric equipment is to look at its material composition. When the amount of each material comprising the inverter is known, each amount can be multiplied by its recyclability rate to obtain the amounts of materials that can be extracted through a recycling process. All these can be summed and normalized by the total mass of materials to obtain the total recyclability. This is shown in the equation below [32]:

$$R_{\text{cyc}} = \frac{\sum_{\text{k=1}}^{n}(m_k \cdot R_{\text{cyc},k})}{m_{\text{tot}}}, \qquad k = 1 : n \tag{2.4}$$

here R_{cyc} is the calculated recyclability rate of the equipment, n is the number of materials comprising the equipment, m_{k} is the mass of the k^{th} material, $R_{\text{cyc},k}$ is the recyclability rate of the k^{th} material, and m_{tot} is the total mass of the materials comprising the equipment. [32] Recyclability rates differ between sources for the same materials. [33][34]

2.4 Converter Topology and Application

As stated in Section 1.3, many of the commonly used DC/AC, DC/DC, and DC/AC topologies are based on the half-bridge topology. In this section, the choices of topology and switches are determined and the rating of the switches are introduced based on the system requirements.

2.4.1 Three-Phase Inverter

Especially for grid-connected residential Renewable Energy Sources (RES) the three-phase full-bridge Voltage Source Inverter (VSI) is predominantly applied, due to the simplicity of its circuit and control, equal loading of the switching devices, and good overall performance as well as time-proven reliability [14]. This inverter type is from this point referred to as the VSI and it is seen in Figure 2.3.

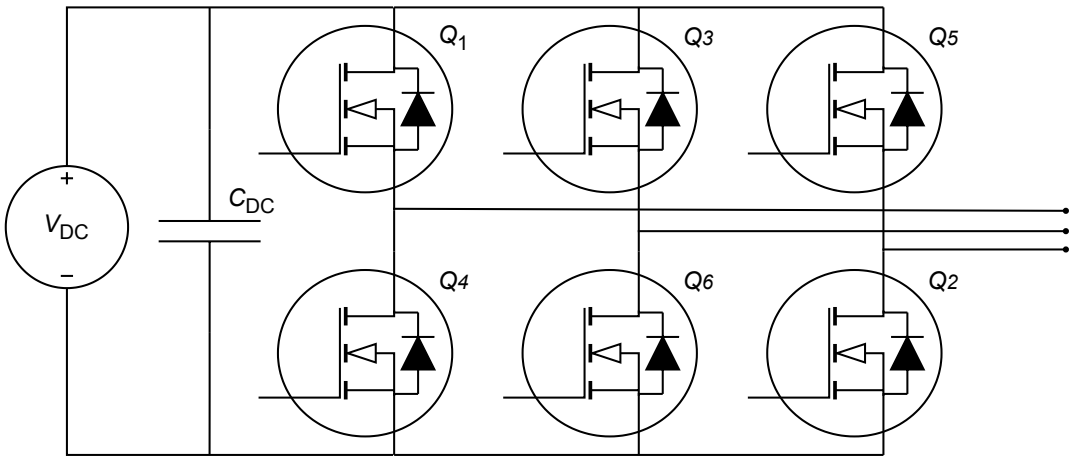


Figure 2.3 Three-phase voltage source inverter.

The purpose of the VSI is to generate the desired output voltage and deliver the required power to the connected loads and feed surplus power to the grid. This sets a requirement for the voltage that the VSI has to generate. In this thesis Sinusoidal Pulse Width Modulation (SPWM) is utilized to operate the VSI.

The VSI is required to be connected to the grid through an intermediate filter to reduce the injected harmonic content. The L-filter offers a simple yet robust attenuation of harmonics and good overall performance. However, the required inductance can become quite large, depending on the application's power rating, as well as poor higher-order harmonic attenuation. The L-filter has an attenuation of $-20\,\frac{\text{dB}}{\text{dec}}$. LCL-filters are often more suitable, in grid-connected applications, for current harmonic attenuation and voltage regulation, as they offer better rejection of high-order switching-frequency harmonics, as they offer an attenuation of $-60\,\frac{\text{dB}}{\text{dec}}$. Another advantage of an LCL-filter is the reduced size of the inductors and capacitors, while achieving superior harmonic attenuation and dynamic performances. However, the LCL-filter also introduces a resonance frequency which needs to be addressed either through physical implementations, such as passive damping, or through measures in the controllers, such as active damping, otherwise, it will lead to instability for the controllers, which will ultimately lead to triggering of protection devices. [14]
Since the LCL-filter offers better rejection of high-frequency harmonics, it is chosen for the remainder of the work in this thesis.

2.4.2 Switching Device Ratings

Based on the requirements for the system, the rating of the switching devices are introduced. All switches in the VSI will experience the same voltage as they share the voltage of the DC-link

capacitor and are switching complementary in each respective leg. Therefore, the voltage rating is based on the required input voltage to the VSI to achieve the desired output voltage. The required input voltage for the VSI is calculated based on Equation 3.2 and increased to 700 V. Thus, multiplying this required voltage by a common safety factor of 1.5 results in 1050 V. The closest common blocking voltage to this, while still remaining larger than required, is 1200 V. The last rating introduced is the current rating. This is based on the continuous current rating of the devices and the calculation is based on the largest current stress in the PEC. Here, the peak phase current is investigated. In this case, with the 10 kW inverter, the phase current is 15 A and thus the conducted current near the peak of the sinusoid is 21 A. It is decided that the safety factor of 1.5 is not required in this instance, as the large current values are only present in shorter intervals. Thus, the requirements for the switches are set up.

Investigated Switching Devices and their Compositions

In this thesis, it is chosen to only investigate Silicon Carbide (SiC) MOSFETs. The choice is based on SiC MOSFETs' generally more desirable properties and despite their generally lower reliability [35]. The switching devices are picked such that they all share the same package type. This choice is primarily for the design simplicity. The chosen package is the TO247-4 and brand-specific variants of this. The chosen switching devices are found in Table 2.2 and their minimum required ratings are introduced in Section 2.4.2.

Table 2.2 Chosen switching devices, for analysis, and their ratings

Device name	Blocking voltage	Continuous-current rating
IMZ120R090M1H	1200V	26A
IMZ120R060M1H	1200V	36A
SCT070W120G3-4AG	1200V	30A
SCT070W120G3-4	1200V	30A
SCTWA40N12G24AG	1200V	33A
SCTWA40N120G2V-4	1200V	36A
SCT040W120G3-4	1200V	40A
SCTWA60N12G2-4AG	1200V	52A

Note that SCT070W120G3-4AG and SCT070W120G3-4 have the same ratings and also share the same electrical parameters and performance when looking through the datasheet. However, a difference is seen in the material composition of the devices and thus the two models are treated separately.

A list of materials present in the larger components of an inverter is to be generated. The inductors and the heatsink compositions are taken into account, as these components are very dependent on the operating points and the chosen switching devices. The capacitors are not taken into account in this work. For simplicity, it is decided to assume that the heatsink only contains aluminum, that the inductor cores are made solely of iron, and that the inductor windings are pure copper. Based on this the recyclability rate list is now generated based on the materials. Where different sources states different recycling rates an interval is given. The list is seen in Table 2.3 below:

Table 2.3 Recycling rates of materials covered in this work. [33][34][36][37]

Material	Recycling rate	Source
Ag/Silver	50-80%	[34][36][37]
Al/Aluminum	42-75%	[34][33][36][37]
Au/Gold	50-95%	[36][34][37]
Cu/Copper	28-60%	[33][34][36][37]
Fe/Iron	50-62%	[36][37][33]
Mg/Magnesium	15-50%	[33][37][36]
Ni/Nickel	43-60%	[33][36][37]
Pb/Lead	50-65%	[36][37]
Sb/Antimony	1-44%	[36][37][33]
Sn/Tin	20-50%<	[37][36]
Ti/Titanium	40-50%<	[36][37]
V/Vanadium	<1-40%	[36][37]

Note that only metals are treated here. In Table 2.3, the placement of the sources in the rightmost column corresponds to the location of their value in the interval in the center column. As seen by this, the different sources are not leaning one way or the other in regard to a generally low or high recyclability. Based on this information, the remainder of this thesis will work with the highest value of each recyclability rate, as it is assumed that a high yield is achievable in the disassembly process.

2.4.3 Performance Testing

It is expected that the introduction of perforations in the PCB will impact the performance of the PEC. The perforations will reduce the rigidity and if they are placed on copper traces or planes, they presumably also impact the electrical performance. Therefore, in the following sections, the testing procedures for testing such impacts on converters and the material they are made from are introduced, which yield insights about how mechanical and electrical performances can be evaluated.

Mechanical Performance Test

To investigate how the mechanical rigidity of the board is impacted by including different perforations, it is desired to see how the flexural strength, σ_f, of a non-perforated design compares to different perforated designs. The reason the flexural strength is a good metric for such an analysis is because it is translatable between different geometries. Thus, a simple geometry can be tested and the results can be projected to other use cases. One method of obtaining the flexural strength is by using the three-point bending test. A force diagram representing this is shown in Figure 2.4 below:

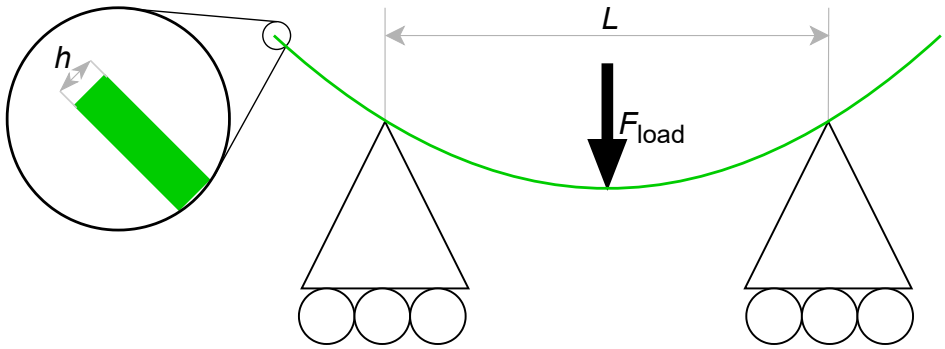


Figure 2.4 Three-point bending test with a PCB specimen.

In the test setup, a roller applies force to the midpoint of a rectangular specimen, which is simply supported by rollers, equidistant from the point where the force is applied. The specimen is positioned so that the center aligns with the top roller, meaning that for the perforated specimens, the perforation line have to be in the center. The top roller is then lowered onto the specimen, increasing the force exerted onto it until fracture. The flexural strength can be derived using the equations below: [38]

$$\sigma_{\mathrm{t}} = \frac{M_{\max}}{S} \tag{2.5}$$

$$\sigma_{\mathrm{c}} = -\frac{M_{\max}}{S} \tag{2.6}$$

Here $M_{\max}$ is the maximum bending moment which is directly proportional to the flexural strength. σ_{c} is the compressive stress and σ_{t} is the tensile stress. The top side of the PCB experiences the compressive stresses and the bottom side is subject to the tensile stress. S is the section modulus, which for a rectangular specimen is obtained by the width, b, of the PCB and the PCB's height, h, as shown in the equation below: [38]

$$S = \frac{b \cdot h^2}{6} \tag{2.7}$$

If the cross section of the PCB is rectangular, which is denoted as a doubly symmetric cross section, then tensile and compressive stresses are equal numerically and can be expressed as: [38]

$$\sigma_{\mathrm{t}} = -\sigma_{\mathrm{c}} = \frac{M_{\max}}{S} \tag{2.8}$$

Therefore, maximum bending moment, $M_{\max}$, is calculated as shown below: [38]

$$M_{\max} = F \cdot \frac{L}{4} \tag{2.9}$$

Here, F is the applied force and L is the distance between the support rollers. Inserting the Equation (2.7) and Equation (2.9) into Equation (2.5) yields:

$$\sigma_{\mathrm{f}} = \frac{6 \cdot F \cdot L}{4 \cdot b \cdot h^2} = \frac{3 \cdot F \cdot L}{2 \cdot b \cdot h^2} \tag{2.10}$$

The flexural strength of each individual perforated specimen can be compared to the benchmark to see the impact of the perforations. FR-4 is a commonly used material for the dielectric layers.

The material consists of woven fiberglass and a flame-retardant epoxy resin. As the dielectric layers are often the thickest layers, they contribute most of the flexural strength. FR-4 exhibits a flexural strength of 413.68 MPa [39]. Thus, the flexural strength of FR-4 serves as the baseline to validate the experimental results and the assessment of the mechanical weakening through perforations. With the introduction of perforations, the PCB experiences greater local stresses at the edges of these introduced perforations, if the PCB is mechanically loaded. This is because the geometry is changing from a uniform cross-section to an irregular one. These points are defined as stress concentrations and they introduce an interruption of the material in the PCB. The applied load can be visualized as a flow through the PCB as shown in Figure 2.5.

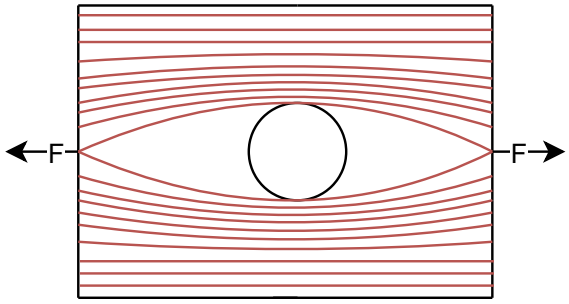


Figure 2.5 Illustration of the stress flow lines in a material under load and with a stress concentration in the middle of the material.

For the stress flow lines to flow around these discontinuities, they have to be compressed in the vicinity of the perforations. Hence, the discontinuities cause the local stress to increase in these areas. As a consequence, the PCB will most likely fail at these stress concentrations under mechanical loading. [38]

Electrical Performance Test

Besides analysis of the mechanical rigidity of the proposed design approach, the electrical performance is of utmost value. Hence, the following sections will elaborate on the electrical testing procedures for the designed PCBs. The electrical tests are performed to ensure that the novel PCB design does not compromise the electrical performance of the equipment. The test, which is performed on all the different test boards, is a Double Pulse Test (DPT). It is performed on the conventional board to investigate if the fundamental PCB design works as desired and as a benchmark for the other boards.

The DPT requires two switching devices, where one is the Device Under Test (DUT) and the other its complementary, a ramping inductor, which is connected to the half-bridge circuit as illustrated in Figure 2.6, and a voltage source.

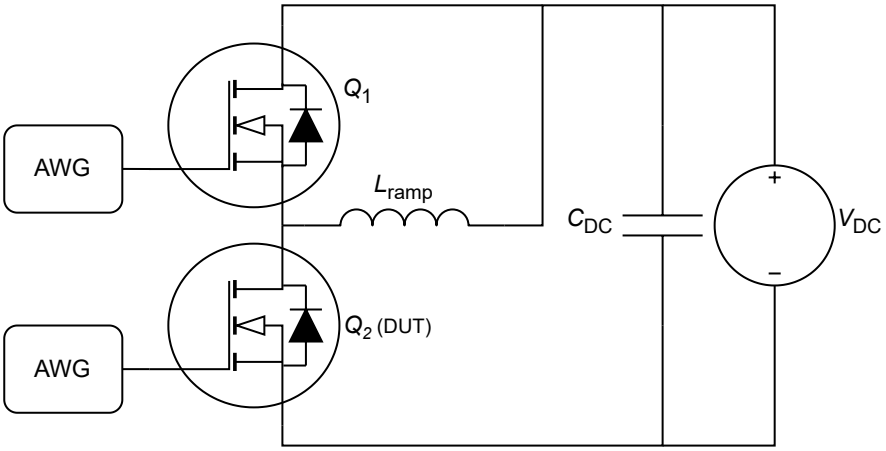


Figure 2.6 Configuration for the DPT test for the conventionally designed half bridge. [40]

The inductor can be connected in parallel to the low-side or high-side switch. The DUT is the switch paralleled with the ramping inductor. It is noted that the switching sequence needs to be implemented according to the configuration of the DPT, meaning the turn-on and turn-off impulses have to be sent to the corresponding switches complementarily.

The DPT consists of three distinct periods, which determine the current level of the test. These periods are depicted in Figure 2.7 along with the current through the DUT.

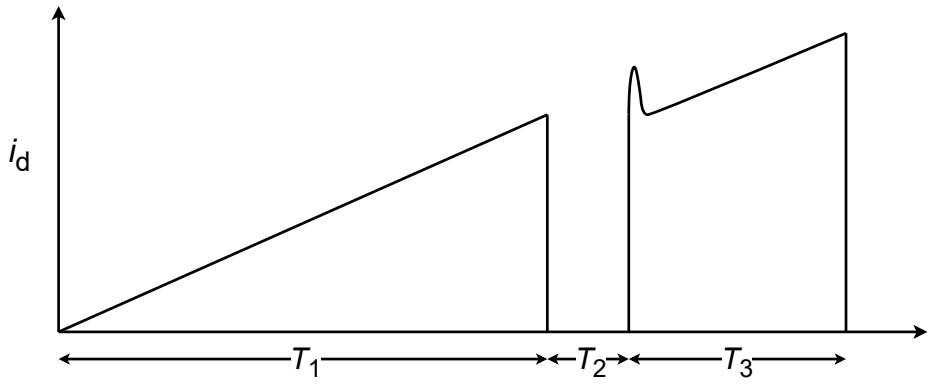


Figure 2.7 Current through the DUT during the DPT. [40]

The first period, T_1, charges the inductor, L_{ramp}, until the desired current level is achieved. This ramping period is dependent on the DC-link voltage, the inductance, and the desired current level, which, when considering an ideal inductor, can be expressed with the following equation:

$$V = \frac{di}{dt} \cdot L \tag{2.11}$$

Since Equation (2.11) considers an infinitesimal time, it can be replaced by a difference in time Δt, which yields the following equation:

$$V = \frac{\Delta i}{\Delta t} \cdot L \tag{2.12}$$

This allows to calculate the ramping period since $t_0 = 0$ and $i_0 = 0$ which, inserted into Equation (2.12) yields:

$$T_{\text{test}} = \frac{I_{\text{test}} L_{\text{ramp}}}{V_{\text{dc}}} \tag{2.13}$$

Here $T_{\text{test}} = T_1$. Hence, the ramping period depends on the parameters on the right side of the Equation (2.13). The following period, T_2, is the freewheeling period of the DUT and the ramped current is allowed to freewheel in the complementary side of the circuit. It is important to consider that the period must not be too long, such that the current level drops under an undesired level, but also not too short either, as the transient behavior of the circuit must settle before the DUT is turned on again.
The last period, T_3, is when the DUT is turned on again. However, the period for T_3 is limited by the maximum current the DUT can handle. Nevertheless, obtaining the full characteristic of the switching transient at the rated current is prudent. [41]

In the DPT, energy is moved from the DC-link capacitors to the ramping inductor. This energy transfer results in a voltage drop over the capacitors, with the voltage drop being dependent on the test current, ramping inductance, DC-link voltage and the capacitance. The calculation for the required DC-link capacitance for a given voltage drop is seen in the equation below: [40]

$$C_{\text{DPT}} \geq \frac{L_{\text{load}} I_{\text{test}}^2}{2V_{\text{dc}}\Delta V_{\text{dc}} - \Delta V_{\text{dc}}^2} \tag{2.14}$$

It is important to maintain the voltage as constant as possible in the DC link, as the voltage directly impacts the transients and losses investigated in the DPT.

It is however, the transition between the periods which are of interest, as this is where the switching events occur. Between T_1 and T_2 the DUT turns off and between T_2 and T_3 it turns on. At these switching events, the switching loss of the device can be found and the circuit behavior can be analyzed. As device characterization is not of interest in this work, the energies and transients are instead used to investigate the impact of introduced circuit alterations such as the perforations. This comparative study is conducted by comparing the switching energies and by analyzing the difference in voltage and current waveforms under the transients. The transients and expected changes are presented in the following.

The transients, which the DUT undergoes at turn-off events, are shown in Figure 2.8, where L_{s} is the total inductance in series with the switching device.

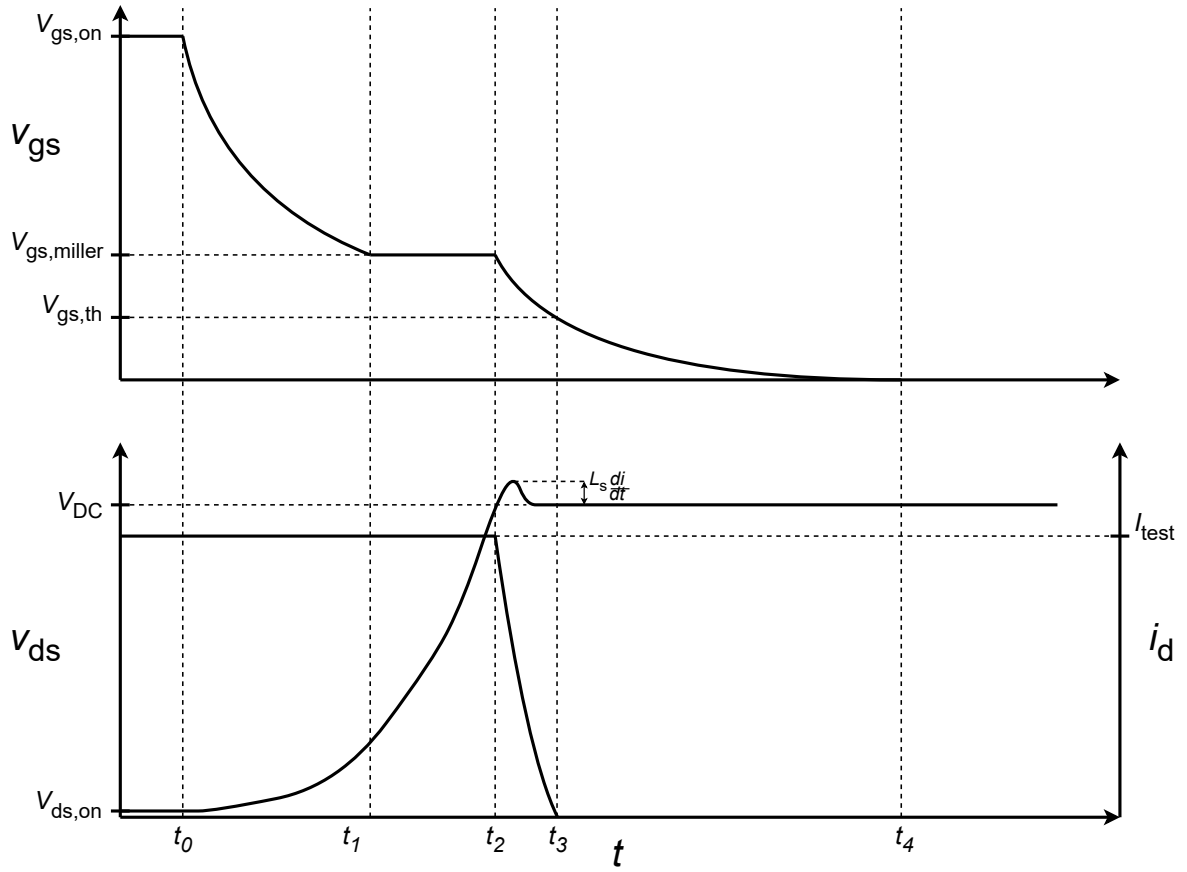


Figure 2.8 Turn-off transient showing DUT gate-source voltage, drain-source voltage, and drain current waveforms. [40]

Before t_0, the gate signal for the device is high. At t_0, the input capacitance is beginning to discharge through the gate resistor and the gate voltage starts to drop. At the same time, the voltage starts to increase over the channel of the DUT. At t_1, the gate voltage reaches the Miller plateau where it remains while the drain-source voltage increases. Then, at t_2, the drain-source voltage reaches the input voltage and the gate-source voltage starts to decrease once again. It is first at t_2 that the drain currents start to decrease. At t_3, the gate-source voltage reaches the threshold value and the current drops to zero. Between t_3 and t_4, the gate-source voltage keeps discharging until it reaches zero at t_4.

In this analysis, the important points are from t_1 to t_3, as this is where the switching energy is dissipated. Furthermore, between t_2 and t_3, the change in parasitic inductance is visible. When the drain-source voltage reaches the DC-link voltage the inductance of the circuit will cause a spike in the voltage due to the experienced change in current which occurs at this instance. This voltage spike can then be used comparatively between different implementations of perforations to see how these change the stray inductance of the power loop of the circuit. Figure 2.9 shows examples of different stray inductances' impact on the overshoot voltage. It is noted that higher series inductance will force the device to turn on faster, as it acts as a current source due to the stored charge. [40]

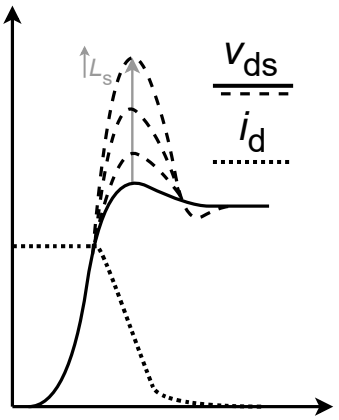


Figure 2.9 Increasing voltage overshoot at turn-off events caused by increasing parasitic stray inductance. [40]

Next, the impacts on the turn-on events are introduced and the transient is shown in Figure 2.10

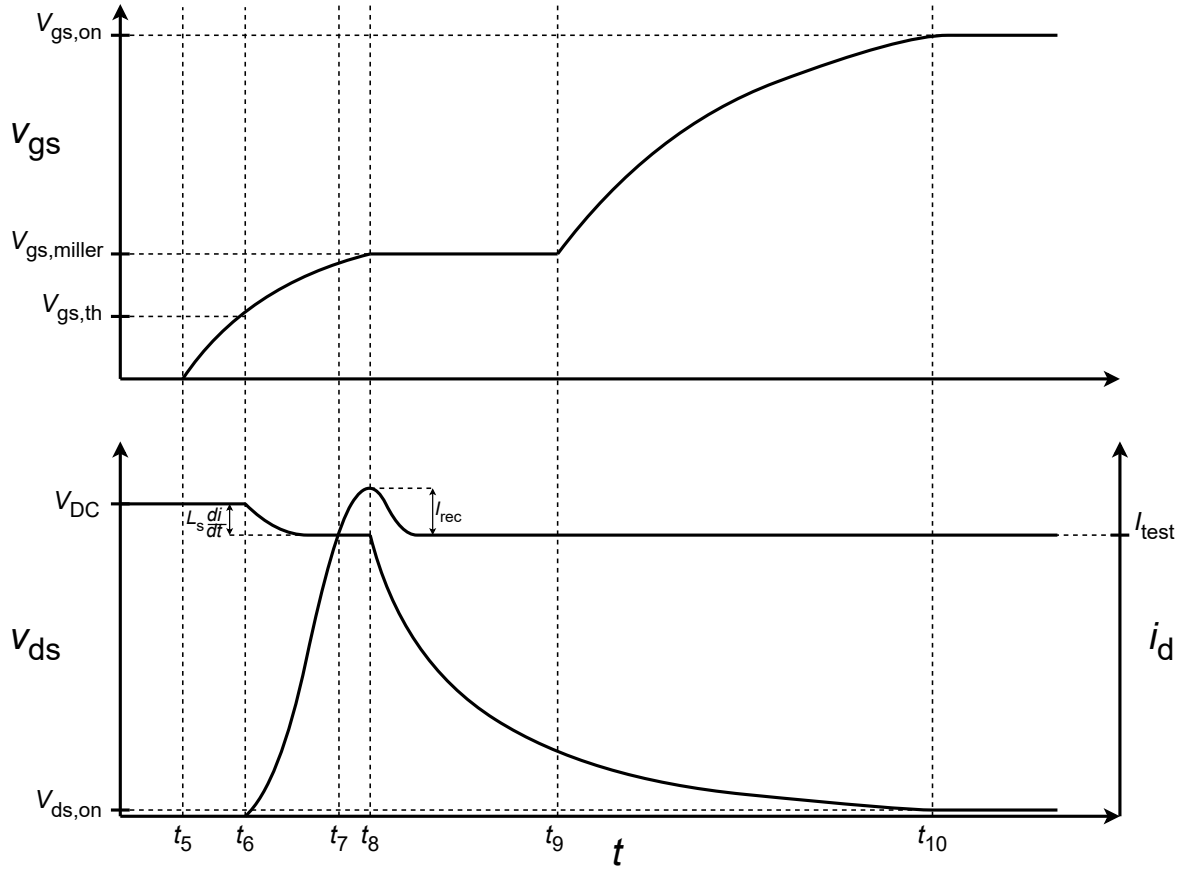


Figure 2.10 Turn-on transient showing DUT gate-source voltage, drain-source voltage, and drain current waveforms. [40]

Here, L_s is again the total series inductance of the power loop and I_{rec} is the reverse-recovery current of the freewheeling diode. Before t_5, the gate signal is low. Then, at t_5, the gate-source voltage starts to increase until it reaches the threshold voltage at t_6. Then at t_6, the current starts to commutate to the DUT's channel. At t_7, the load current is fully commutated to the DUT channel and the reverse-recovery current of the complementary switch's diode is witnessed. Then at t_8, the current reaches its maximum value, being the load current plus the magnitude of the reverse-recovery current. Here, the gate-source voltage stops increasing as the Miller plateau is reached. Then the drain-source voltage starts to drop. At t_9, the change in gate-source voltage decreases, allowing the gate-source voltage to start increasing again. Then at t_{10} the gate-source voltage reaches the final value and the DUT is fully on.

Here, the important analysis is between t_6 and t_{10} for the switching energy. Between t_6 and t_7, the impact of the stray inductance is again seen on the drain-source voltage. The change in current at the start of the commutation will cause a voltage drop over the stray inductance between the DUT and the DC-link capacitors. A larger stray inductance will cause a larger drop in the voltage. Additionally, between t_7 and t_8, the reverse-recovery current is impacted by the capacitance of the complementary diode. An increased capacitance will result in a larger peak current, as it corresponds to a larger charge being stored. It is expected that including perforations in the PCB will not affect the capacitive coupling of the devices much and therefore the main interest is the impact of the stray inductance. Similar to the turn-on transient, L_s affects the switching speed. At turn off, a larger series inductance does however, slow the switching. Thus, an increased inductance will speed up turn-on transients and slow down turn-off transients.

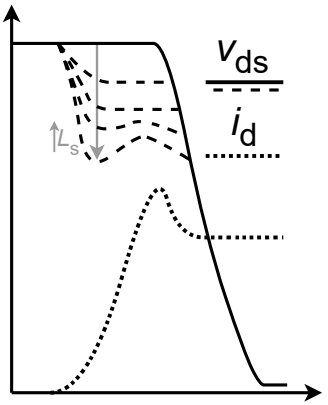


Figure 2.11 Increasing voltage overshoot at turn-on events caused by increasing parasitic stray inductance. [40]

It is noted that changing the gate resistance will have an impact on the switching transients as well. This is because a lower gate resistance will result in an increased di/dt and thus the impact of the stray inductance is increased and the opposite is occurring if the gate resistance is increased.

In this chapter, common principles in PEC design and the decision-supporting design tool in the form of a MOO algorithm are presented. In regard to the optimization tool, the recyclability has been defined as an objective. Practices in the design of circular consumer electronics are also investigated to see if these can be applicable in the design of sustainable PECs. Furthermore, a novel approach for PCB design has been presented. Lastly, the topology was introduced along with the required tests to validate the novel design approach.

3 Modeling

In this chapter, the required models for dimensioning and operating a three-phase inverter as well as generating the optimization algorithm, are introduced. First, the operation of the VSI is introduced with the power loss model used for the MOSFETs in the three-phase inverter. Then, the component models used for calculating the required size of the passive components are introduced along with a heatsink-sizing proposal based on the average losses of the inverter. As a last part, the magnetic-design considerations for the required inductors of the LCL-filter are introduced along with the power-loss models for some suitable core materials.

3.1 Modeling of the Three-Phase Inverter

In this section, the operation modeling of the VSI, required for the implementation in a suitable optimization algorithm, is introduced. First, the SPWM of the VSI is introduced. The second part is a summary of the power loss model for the switches in the inverter as presented in [1] and [2].

3.1.1 Modulation of Three Phase Inverter

When utilizing SPWM, the switches are turned on or off based on a continuous comparison between a carrier waveform, in this case a triangular waveform, $\hat{V}_{\text{tri}}$, and a reference waveform, $\hat{V}_{\text{ref}}$. The triangular waveforms' frequency establishes the inverter's switching frequency. In SPWM, the reference waveform is a sinusoidal wave and the amplitude of this signal is altered depending on the desired voltage generation. Moreover, the frequency of this reference is desired to be the fundamental output frequency of the inverter. The modulation index is defined as: [42]

$$m_{\text{i}} = \frac{\hat{V}_{\text{ref}}}{\hat{V}_{\text{tri}}} \tag{3.1}$$

With $\hat{}$ denoting the amplitude of these waveforms. In intervals, where the value of the reference waveform exceeds the value of the carrier waveform, the switch is turned on, and when the opposite is the case the switch is turned off. The waveform comparison and corresponding pulse train is seen in Figure 3.1.

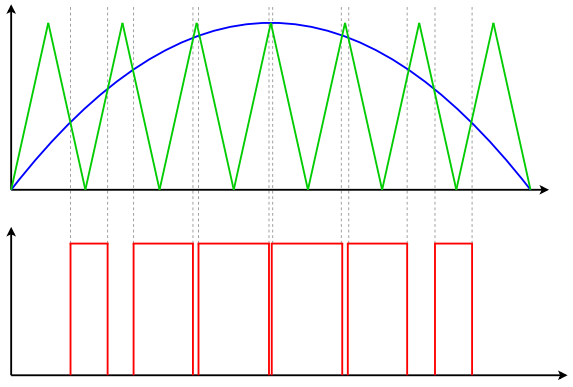


Figure 3.1 Three-phase inverter PWM with gate-driver pulse train.

It is noted that another definition of the modulation index exists, which is in regard to the output and DC-input voltage. Therefore, the peak voltage of the residential grid, 325 V, is used and thus, the required input voltage for the inverter can be calculated. The required input voltage is calculated as two times the desired voltage magnitude divided by a proportionality constant. This proportionality constant is equal to modulation index introduced in Equation (3.1). The calculation of the input voltage is seen in the equation below: [43]

$$V_{\mathrm{DC}} = \frac{2 \cdot V_{\mathrm{m,AC}}}{m_{\mathrm{i}}} \tag{3.2}$$

In SPWM, the modulation index must remain below unity, otherwise the inverter will go into over-modulation, which will cause an increase in the low-order harmonics in the output waveform. Based on this, the minimum required input voltage, assuming ideal components, is 650 V. Due to non-ideality, voltage drops will occur throughout the circuit, and the required dead time also impacts the actual output voltage. Thus, a larger input voltage is required, and it is in this thesis decided that it must be at least 700 V. Furthermore, for the three-phase inverter to output three phases, the switching signals are generated by comparing the same triangular waveform with three sinusoidal reference waveforms, with each sinusoidal waveform being phase shifted by 120° [42].

3.1.2 Power Loss Model for Three-Phase Inverter MOSFETs

This is a summary of the switch power loss model presented in [1] and [2], as this is used in the algorithm. It is noted that the power factor is unity for all of the calculations and that conduction in Q1 and Q3 of the MOSFETs result in the same conduction loss.
The power loss calculations are based on the "On-resistance versus drain current" and "Switching loss versus drain current" charts from the MOSFET's datasheets. These are fitted to a second-order polynomial, and the coefficients are stored in the database. Then, the first step of the power loss model is to calculate the average on-resistance of the switches. As MOSFETs are used in this thesis, the power loss model calculates the average drain-source on-resistance. The coefficients from the datasheets are made into a function of the output current. The model is shown below: [1]

$$i(t) = I_{\mathrm{o}} sin(\omega t) \tag{3.3}$$

$$R_{\mathrm{ds}}(t) = R_0 + R_1 i(t) + R_2 i(t)^2 \tag{3.4}$$

Here R_{ds} is the drain-source resistance, R_0 is the zero-order coefficient of the drain-source polynomial, R_1 is the first-order coefficient, and R_2 is the second-order coefficient. The average drain-source resistance is calculated over half of the fundamental period. The current waveform is generated as a high-resolution vector, which turns R_{ds} into a discrete vector. Thus, the average is achieved by summing all the entries and dividing by the length of the vector, i.e., the number of entries. This is shown below:[1]

$$R_{\mathrm{ds,avg}} = \frac{\sum_{n=1}^{N} R_{\mathrm{ds}}(n)}{N} \tag{3.5}$$

Here N is the number of entries.

Next the Root Mean Square (RMS) current for both the high-side and low-side switch is calculated. This is done based on the modulation of the inverter and the desired output current. SPWM is used to generate all switching instances for the two MOSFETs, in the half-bridge, for half of a fundamental period. Then, based on the switching instances and the desired output waveform, the current at each switching instance is mapped and used for piece-wise integration in the RMS calculation, as seen in the equation below: [1]

$$I = \sqrt{\frac{1}{T} \cdot \sum_{i=1}^{n_{\text{rise,edge}}} \int_{t_{r,i}}^{t_{f,i}} i(t)^2 \, dt} \tag{3.6}$$

With the RMS current obtained, the conduction loss can now be calculated as shown below:

$$P_{\text{cond}} = R_{\text{ds,avg}} I^2 \tag{3.7}$$

The conduction losses are calculated for the high-side and low-side MOSFET independently.

Next, the switching losses are summarized. Here, the currents at the different switching instances are used as well. The currents are used with the switching energy coefficients saved in the database to generate the switching energy at every instance. This is seen in the equation below: [1]

$$E_{\text{sw}}(I_{\text{inst}}) = E_0 + E_1 I_{\text{inst}} + E_2 I_{\text{inst}}^2 \tag{3.8}$$

Here I_{inst} is the vector containing all the instantaneous current values from every turn-on instance, E_{sw} is the total switching energy, E_0 is the zero-order coefficient of the switching energy polynomial, E_1 is the first-order coefficient, and E_2 is the second-order coefficient. It is assumed that the change in current between turn on and turn off is negligible and that the difference averages out over half of the fundamental period. Then the switching power loss is achieved by averaging the energy, by summing all the entries and dividing by the period, and then multiplying by the switching frequency, which is also used in the modulation scheme.
With this, the power loss models for the MOSFETs has been summarized.

3.2 Component Modeling

In this section, the different models used to dimension the VSI's components are introduced. First, the model for the DC-link capacitance is introduced, followed by the output LCL-filter modeling. A thermal network is developed for the heat dissipation of the switching devices through a heatsink to the surrounding air. The dimensioning and design of the different inductors are also introduced. Lastly, the recyclability rate modeling of the inverter is introduced.

3.2.1 DC-Link Capacitance Sizing

For the capacitor dimensioning, two approaches are used in this project. The two approaches are used in tandem to allow better operation the VSI. The first methodology revolves around a balanced use of the inverter in a state where equal power is supplied across the three phases. This approach is based on the capacitors keeping the DC-link voltage stable for fast responses in the span of switching cycles. Here, the capacitors will have enough power to supply or absorb

additional transient energy. The calculation for the fast DC-link capacitance is shown in the equation below: [44]

$$C_{\text{DC,fast}} \geq \frac{P_{\text{max}}}{(V_{\text{DC}}\Delta V \pm \Delta V^2)\, f_{\text{sw}}} \tag{3.9}$$

Here, $C_{\text{DC,fast}}$ is the required capacitance, P_{max} is the maximum power throughput of the inverter, V_{DC} is the DC-link voltage, ΔV is the allowed voltage ripple in the DC link, and f_{sw} is the switching frequency. In the equation, $\pm$ indicates that different transients require either a larger or smaller capacitance to maintain the desired voltage ripple. In this thesis, the term $\pm\Delta V^2$ is neglected as the system is designed to compensate for both a source and load change. Thus, one will not be prioritized over the other.
If either film or ceramic capacitors are selected as the fast capacitors, they can be further used as decoupling capacitors, given that they are placed within close proximity of the drain terminal of the high-side MOSFET due to their very low Equivalent Series Resistance (ESR). [40]

The second approach deals with unbalances where the period is closer in value to that of the fundamental waveform. This approach supplies each phase with sufficient capacitance when the different phases are loaded unevenly. As this requires a larger capacitance, electrolytic capacitors are a good choice due to their high energy density. [40]
The calculation for the slow DC-link capacitance is shown in the equation below:[45]

$$C_{\text{DC,slow}} \geq \frac{P_{\text{unbalance,max}}}{2\pi f_{\text{g}} V_{\text{DC}} \Delta V} \tag{3.10}$$

Here, $C_{\text{DC,slow}}$ is the required capacitance for the slow capacitors, $P_{\text{unbalance,max}}$ is the maximum expected power unbalance between phases, and f_{g} is the grid frequency.
In this thesis, the voltage ripple is set for both approaches to be 10% of the DC-link voltage. The maximum power unbalance is dictated by TR 3.2.1 by Energinet and IEEE standard 929-2000 [46][47]. These regulations state that smaller power plants, such as a residential PV inverter, must be able to operate in a voltage unbalance of 110% to 85% between phases. Thus, the maximum power unbalance occurs when a phase experiences a 15% voltage unbalance while all other phases conduct full phase currents, resulting in a 15% power unbalance. Thus, 15% power unbalance is used for dimensioning the slow DC-link capacitance in this thesis.

3.2.2 Output Filter Design

The components for the LCL-filter for the output of the inverter are designed in this section. As mentioned in Section 2.4, the LCL-filter consists of two inductors with a shunt capacitor in between. The dimensioning of the filter components below was introduced into the power loss model developed in [2] and is based on [48]. The following is a summary of the modeling. The filter capacitance is calculated based on the base impedance of the inverter and the frequency of the grid. The calculation for the filter capacitance is seen in the equation below:

$$Z_{\text{b}} = \frac{V_{\text{ll}}}{P_{\text{n}}} \tag{3.11}$$

$$C_{\text{b}} = \frac{1}{\omega_{\text{g}} \cdot Z_{\text{b}}} \tag{3.12}$$

$$C_{\text{f}} = xC_{\text{b}} \tag{3.13}$$

Here Z_{b} is the base impedance, V_{ll} is the line-to-line output voltage of the inverter, P_{n} is the nominal converter power, C_{b} is the base impedance of the system, ω_{g} is the angular frequency of the grid, and x is the assumed maximum variation in the power factor and is often set to 5% [48]. Next, the inverter-side inductance is calculated. This is calculated based on the input voltage, which the inductor is continuously pulsed with, the switching frequency and the maximum ripple current. The calculation is shown in the equation below:

$$L_1 = \frac{V_{\mathrm{dc}}}{6 f_{\mathrm{sw}} \Delta I_{\mathrm{max}}} \tag{3.14}$$

Next, the grid-side inductor is calculated based on the desired attenuation of the high-order components, the filter capacitance, and the angular switching frequency as shown in the equation below:

$$L_2 = \frac{\sqrt{\frac{1}{k_{\mathrm{a}}^2}} + 1}{C_{\mathrm{f}} \omega_{\mathrm{sw}}^2} \tag{3.15}$$

Here, k_{a} is the desired attenuation, and ω_{sw} being the switching angular frequency. With the filter component models being introduced, the applicability in a concrete system is checked. This check is performed by looking at the resonant frequency of the filter and comparing it to the grid frequency and the switching frequency, This is to ensure that the resonant frequency is inside the range, but not too close to either frequency. First, the resonant frequency is calculated as shown in the equation below:

$$\omega_{\mathrm{res}} = \sqrt{\frac{L_1 + L_2}{L_1 \cdot L_2 \cdot C_{\mathrm{f}}}} \tag{3.16}$$

$$f_{\mathrm{res}} = \frac{\omega_{\mathrm{res}}}{2\pi} \tag{3.17}$$

Here, f_{res} is the resonant frequency, and ω_{res} is the resonant angular frequency. After these calculations, the check is performed to ensure that the resonant frequency is at least one magnitude larger than the grid frequency and that the resonance frequency is less than half of the switching frequency. [48]
Additionally, it is recommended to add damping resistors in series with each of the capacitors. These are added to dampen the oscillations that can occur inside the filter. The damping resistance is calculated as shown below:

$$R_{\mathrm{f}} = \frac{1}{3\omega_{\mathrm{res}} C_{\mathrm{f}}} \tag{3.18}$$

As a new addition to the filter capacitor modeling, the current ripple is considered. As the capacitors experience and help maintain the alternating voltage at the output of the filter, it has to charge and discharge. This results in a current ripple, which is dependent on the voltage of the capacitor and thus this is calculated first. The calculation is presented in the equation below: [14]

$$V_{\mathrm{c,filter}} = \sqrt{V_{\mathrm{o}}^2 + \omega_0^2 L_2^2 I_{\mathrm{o}}^2 - 2\omega_0 L_2 I_{\mathrm{o}} V_{\mathrm{o}} sin(\varphi)} \tag{3.19}$$

Here, $V_{\mathrm{c,filter}}$ is the voltage over the capacitor, V_{o} is the output voltage of the filter, ω_{o} is the angular frequency of the output voltage, which in this case is the same as that of the grid, I_{o}

is the output current, and φ is the phase angle between the output voltage and current. Thus, it is noted that the capacitor voltage is the largest, when the voltage and the current are in phase, and it is the smallest, when the power factor is 0. Next, the current is calculated as the capacitor's impedance divided by the voltage calculated in Equation (3.19) as seen in the equation below:

$$I_{\mathrm{cf}} = \omega_0 C_{\mathrm{filter}} V_{\mathrm{c,filter}} \tag{3.20}$$

This is the current that the capacitor is subject to and thus the filter capacitor has to be at least rated for this current.

3.2.3 Thermal Network

In this thesis, the effects of the thermal swing of the MOSFET chips are not investigated. SiC-MOSFET chips are capable of withstanding very high junction temperatures. However, large stress in the form of high average temperatures with large thermal swings can lower the total lifetime of the devices. [49]
The thermal network, which is used for the modeling in this work, is shown in Figure 3.2

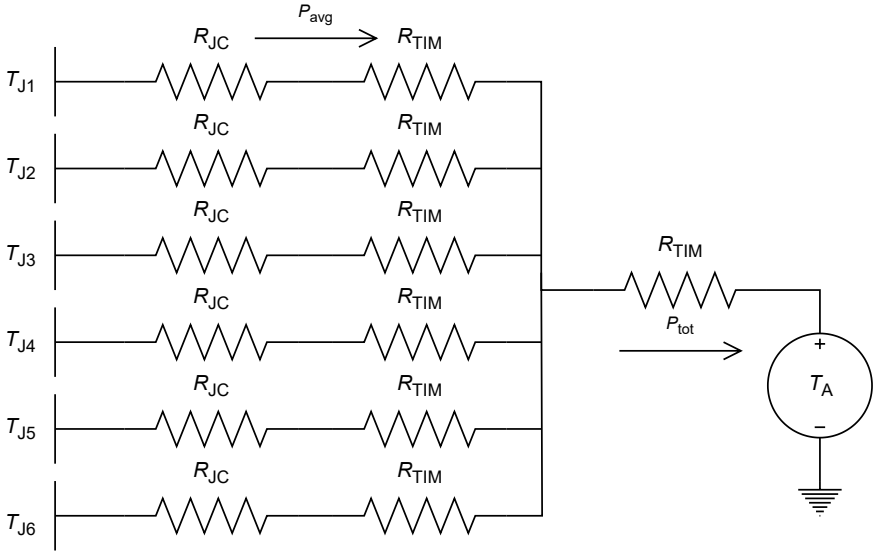


Figure 3.2 Thermal network of three-phase inverter with thermal interface material and heatsink.

This is a steady-state thermal network, as transient thermal capacitance effects are neglected. The assumption is that the average junction temperature of one switch can be estimated as the average power loss of that switch through the thermal resistance from junction to case and through the Thermal Interface Material (TIM), added with the average temperature rise over the heatsink's thermal resistance.
This assumption is based on that the average temperature over the thermal capacitors has to be zero otherwise a constant temperature rise will occur.
Based on this, the model for the junction temperature as is seen below:

$$T_{\mathrm{J1}} = P_{\mathrm{avg}}(R_{\mathrm{JC}} + R_{\mathrm{RIM}}) + P_{\mathrm{tot}} R_{\mathrm{HS}} + T_{\mathrm{A}} \tag{3.21}$$

Here, P_{avg} is calculated as the mean of the power loss for the positive half of the fundamental period and the negative half of the fundamental period. The power loss of the positive half cycle

is calculated as the power loss of the high-side switch, and the power loss for the negative half cycle is calculated as the losses for the low-side switch. Thus, the average power loss is as seen in the equation below:

$$P_{\text{avg}} = \frac{P_{\text{hs}} + P_{\text{hs}}}{2} \tag{3.22}$$

The total power loss is six times the average power loss and thus Equation (3.21) can be rewritten as seen in the equation below:

$$T_{\text{J1}} = P_{\text{avg}}(R_{\text{JC}} + R_{\text{RIM}}) + 6P_{\text{avg}}R_{\text{HS}} + T_{\text{A}} \tag{3.23}$$

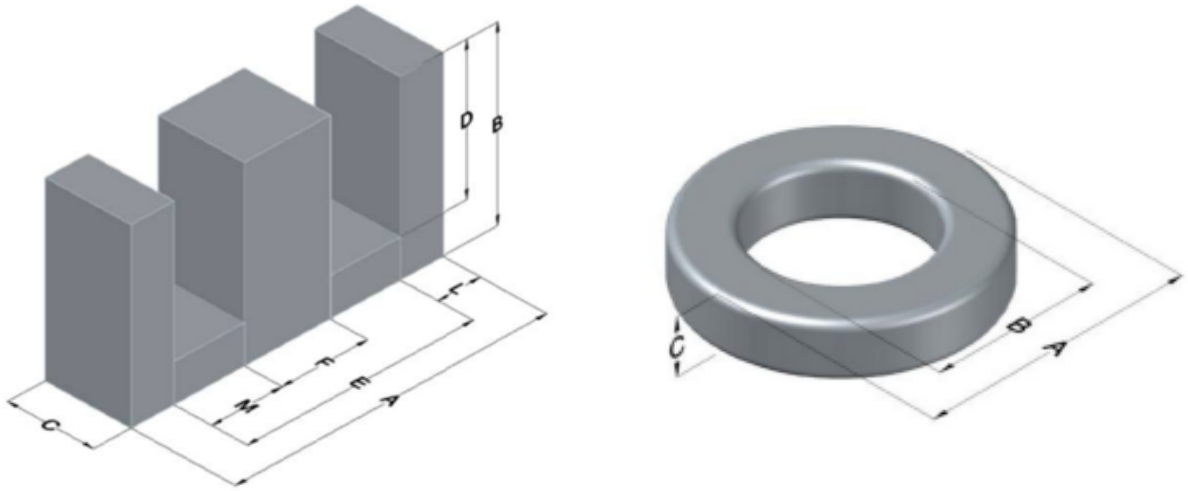
Solving for the thermal resistance of the heatsink results in the equation below:

$$R_{\text{HS}} = \frac{T_{\text{J1}} - T_{\text{A}}}{6P_{\text{avg}}} - \frac{(R_{\text{JC}} + R_{\text{RIM}})}{6} \tag{3.24}$$

With this equation, the maximum thermal resistance of a heatsink, which will keep the average junction temperature at the desired level, can be calculated. The power losses of the MOSFETs are calculated based on the appropriate switching devices in the database, the desired average junction temperature, and the applied TIM.
It is noted that as this calculation results in an average junction temperature, the temperature swing have to be considered such that the maximum temperature does not exceed the maximum allowed for the switching device.

3.2.4 Inductor Dimensioning and Design

This section introduces how to design power inductors with E-cores and toroidal cores. The two core shapes are seen in Figure 3.3 below:



(a) **(b)**

Figure 3.3 Dimension designations for two different core types: a) Designations for E-cores [50], b) Designations for toroidal cores [51].

First, the design procedure is introduced for the E-cores and then afterwards for the toroidal cores.

E-Core Inductors - Area Product Method

The following design methodology is based on [52]. The area product method is a common method for picking cores for use in a power inductor. The method calculates the required area product for a given application. The first thing to do when picking a core for a design is to calculate the number of windings required for the inductor to reach the required inductance with the given core. To do this, the inductance factor, which is normally found in the core's datasheet, and the required inductance are used as seen in the equation below: [52]

$$N(i) = \sqrt{\frac{L_1}{A_\mathrm{l}(i)}} \tag{3.25}$$

Here N is the number of turns, L is the desired inductance, and A_l is the inductance factor. Also, the magnetic flux density is to be calculated based on the application and the chosen core. The magnetic flux density is calculated as the product of the core permeability, number of windings, and the peak current all divided by the effective length of the magnetic field as seen in the equation below [53]:

$$B_\mathrm{pk} = \frac{\mu_\mathrm{r} \cdot \mu_0 \cdot N \cdot I_\mathrm{pk}}{l\mathrm{e}} = \frac{\mu_\mathrm{core} \cdot N \cdot I_\mathrm{pk}}{l\mathrm{e}} \tag{3.26}$$

Next, the required area product is calculated as seen below: [52]

$$A_\mathrm{p,req} = \frac{2W_\mathrm{m}}{K_\mathrm{u} B_\mathrm{pk} J} \tag{3.27}$$

Here, W_m is the energy which is to be stored in the inductor, K_u is the utilization factor, B_pk is the peak magnetic flux density in the core, and J is the current density in the wire(s) making up a winding. The actual area product of a core is given by the product of the window area of the core, where the windings go, and the effective area of the core. This is seen in the equation below: [52]

$$A_\mathrm{p} = A_\mathrm{w} A_\mathrm{e} \tag{3.28}$$

The effective area is often listed by the manufacturer in the datasheet of the core and the window area of the core shape in Figure 3.3a is calculated as shown in the equation below:

$$A_\mathrm{w,E} = W_\mathrm{w} W_\mathrm{h} = 2DM \tag{3.29}$$

The window area and the current density are used to calculate the utilization factor and both are used in Equation 3.27. First, the area of the wire is calculated, then the current density is calculated as the current divided by the wire area. The calculations are seen in the equation below:

$$A_\mathrm{wire} = \pi \frac{d_\mathrm{wire}^2}{4} N_\mathrm{wire} \tag{3.30}$$

$$J = \frac{I}{A_\mathrm{wire}} \tag{3.31}$$

The wire area have to be designed such that the current density is in the range of 6-10 $\mathrm{A/mm^2}$ for windings with a total length of less than 1 m, for wires with a longer total length larger than 1 m the current density is not to exceed 5 $\mathrm{A/mm^2}$. When the wire is designed to reach a desired

current density, the total winding area cross section is to be calculated as the wire diameter multiplied by the number of wires. This is seen below:

$$A_{\mathrm{Cu}} = A_{\mathrm{wire}} N \tag{3.32}$$

With the total winding cross-sectional area calculated, the window utilization area is the ratio of the total winding cross section and the window area, as seen in the equation below: [52]

$$K_{\mathrm{u}} = \frac{A_{\mathrm{Cu}}}{W_{\mathrm{a}}} \tag{3.33}$$

It is noted that a reasonable value for K_{u} coincides in the interval between 0.3-0.7. If the core passes the required area product test, the saturation flux density must be checked. Here, the peak flux density calculated in Equation (3.26) has to be smaller than the saturation flux density of the core material specified by the manufacturer:

$$B_{\mathrm{sat}} > B_{\mathrm{max}} \tag{3.34}$$

If the actual maximum magnetic flux density is less than the saturation flux density for the specific core the core is viable and the inductor can be manufactured. For estimating the required amount of wire to generate the inductor, the Mean Length of Turns (MLT) of the windings is calculated and multiplied by the number of turns. The MLT is based purely on the geometry of the core and does not take the number of windings into account. The MLT for an E-core with dimensions designated as in Figure 3.3a is seen in the equation below: [52]

$$l_{\mathrm{wire}} = N \cdot MLT = N \cdot 2(C + E) \tag{3.35}$$

The length of wire is also used for the conduction loss calculation for the inductor, which is presented in the following.

Toroidal Core Inductors - Area Product Method

The process for designing an inductor with a toroidal core is very similar to that of an E-core-based design. The differences lie in the calculation of the window area and the MLT. The calculations are based on Figure 3.3b and is seen in the equation below: [52]

$$A_{\mathrm{w,toroid}} = \pi \frac{B^2}{4} \tag{3.36}$$

Winding losses

The winding losses are calculated based on the resistivity of copper and the length of the wire calculated with Equation (3.35). With these values, the resistance is calculated which is then multiplied by the conducted RMS current squared to obtain the conduction losses. The equations are presented below:

$$R_{\mathrm{L}}(i) = r_{\mathrm{wire}} \cdot l_{\mathrm{wire}}(i) \tag{3.37}$$

$$P_{\mathrm{Cu,L}}(i) = R_{\mathrm{L}}(i) \cdot I^2 \tag{3.38}$$

Here, R_{L} is the resistance, r_{L} is the resistivity which is dependent on the cross-sectional area of the conductor, and $P_{\mathrm{Cu,L}}$ is the conduction loss. Apart from the conduction losses, the core-loss models are also to be obtained. These are to be modeled in the following.

Core losses

Due to hysteresis, power losses will occur in the cores when subject to an alternating magnetic field. The Steinmetz equation is used for calculating the losses in magnetic cores and many different forms of the equation exist. The variations of the Steinmetz equation are all empirical models where losses are fitted to the model, which enables the loss calculation at other operating points as well. [54] The Steinmetz equation is shown below:

$$P_{\text{fe}} = K_{\text{c}} f^{\alpha} B_{\text{max}}^{\beta} \tag{3.39}$$

Here, P_{fe} is the power loss per unit volume, f is the frequency at which the losses are calculated, B_{max} is the maximum flux density experienced in the core, and K_{c}, α, and β are empirical constants which are found in the datasheet for the magnetic material which the core is made from.

In this thesis, the core loss models are obtained for specific core materials, resulting in different separate models. As the cores are subject to different hysteresis loops, introduced by the different frequencies, these will also be modeled. This is done by calculating the power loss in the core at the fundamental frequency and at the switching frequency at their respective corresponding magnetic flux density. Additionally, higher frequency harmonics will also introduce losses in the cores. However, the amplitudes of the corresponding flux densities are assumed to be so small that they can be neglected without larger impact on the accuracy. The losses at the different frequencies can then be added to approximate the power loss of the core as shown below:

$$P_{\text{fe,tot}} = P_{\text{fe,fund}} + P_{\text{fe,sw}} = K_{\text{c}} \left(f_{\text{fund}}^{\alpha} B_{\text{max,fund}}^{\beta} + f_{\text{sw}}^{\alpha} B_{\text{max,sw}}^{\beta} \right) \tag{3.40}$$

Four of the materials investigated in this work are Neu Flux by KDM, Fe SI by Poco Magnetic, Xflux by Magnetics Inc., and Kool Mu by Magnetics Inc. Common for these core materials is that they are made from iron powder. Iron powder cores are well suited for power applications as they have distributed air pockets throughout the core, which can contain a large amount of magnetic energy without the core saturating. This is also achievable with solid iron cores, ferrite cores, by introducing larger air gaps in the assembly process. However, these large air gaps are subject to large fringing fluxes, which can cause Electro Magnetic Interference (EMI) problems. Thus, as this project does not focus on the EMI/Electro Magnetic Compatibility (EMC) aspect of converter design, it is sensible to choose the option, that will have the least impact on this aspect. One large ferrite core without an air gap is introduced to see if this is picked as well. This is made from N87 by TDK.

As mentioned in Section 3.2.4, two core shapes are used, namely E-cores and toroidal cores. It is appropriate to use different equations for these core shapes despite being made from the same material. In this thesis, different core shapes will not share the same core material however, the developed algorithm is able to include this. It is decided to include more different materials instead. The loss models for the toroidal cores are introduced first. The first material is Neu Flux, here the included power loss model is the same for the materials with the relative permeability of 60, 75, and 90. The model is shown in the equation below:

$$p_{\text{NeuFlux}} = B_{\text{peak}}(i)^{2.15} \cdot (5.101 \cdot f + 0.1561 \cdot f^{1.822}) \tag{3.41}$$

It is seen that this is a different variation than the general Steinmetz Equation presented in (3.39). In this model, the unit of the flux density is kilogauss, the unit for the frequency is

kilohertz and the resulting power per unit volume is in milliwatts per cubic centimeter.
Next is the Fe Si from Poco and this model is for a relative permeability of 60. The model is shown in the equation below:

$$p_{\text{Si-Fe}} = B_{\text{peak}}^{2.295} \cdot (8.884 \cdot f + 0.0625 \cdot f^{1.982}) \tag{3.42}$$

Here the variables and units are the same as in Equation (3.41). The model for N87 is a bit different, it uses the general Steinmetz Equation but it models the power loss per unit mass instead. The model is shown in the equation below:

$$p_{\text{N87}} = 3.48 \cdot 10^{-5} f^{1.635} B_{\text{peak}}^{2.253} \tag{3.43}$$

Here, p_{N87} is the power loss in watts per kilogram. The next material is of the included E-core, Xflux:

$$p_{\text{Xflux,26}} = 379 B_{\text{max}}^{1.995} f^{1.33} p_{\text{Xflux,40,60}} = 441 B_{\text{max}}^{2.16} f^{1.35} \tag{3.44}$$

Lastly, the power loss model for E-cores made from Kool Mu is presented. In this model, the constant K_{c} is dependent on the relative permeability. The models are presented below:

$$p_{\text{KoolMu,14}} = 29.3 B_{\text{max}}^{1.988} f^{1.541} \tag{3.45}$$

$$p_{\text{KoolMu,26,40}} = 32.22 B_{\text{max}}^{1.988} f^{1.541} \tag{3.46}$$

$$p_{\text{KoolMu,60,90}} = 40.27 B_{\text{max}}^{1.988} f^{1.541} \tag{3.47}$$

Here, the power loss $p_{\text{KoolMu,x}}$ is once again in miliwatts per cubic centimeter, and the frequency is in kilohertz, however the flux density is now in tesla.
These power loss models are then evaluated at the different flux densities produced in the different cores at their specific operating points and then multiplied either by the volume of the core or the mass of the core. The iron losses can then be added to the copper losses for the total inductor loss.

With this, all the different required models are introduced and the algorithm can be assembled.

4 Eco-Design Implementation and Testing

This chapter presents the solution strategies, developed to address the problem statement and to meet the objectives outlined in Section 1.3.
First, the chapter elaborates on the MOO algorithm and its implementation, describing how it is applied to investigate the different design objectives. Next, the design process for the PCBs is presented, highlighting how the electrical requirements are integrated with the eco-design considerations. Following this, the results of the DPTs are reported, providing insights into the electrical performance of the developed boards. Finally, the chapter concludes with the presentation of the mechanical test outcomes, which evaluate the flexural strength of the perforated designs and assess the trade-offs introduced by the eco-design.

4.1 Assambly of the Multi-Objective Optimization Algorithm

As mentioned in Section 2.1, multi-objective optimization is a common design tool for PECs as it enables the designer to investigate the benefits and drawbacks of different combinations of the hardware. This section presents the structure of the developed optimization algorithm. The optimization algorithm, which is developed in this thesis, is a continuation of previous work in [1][2]. The previous work has resulted in a power loss model for power semiconductors and filters in inverters, as well as the filter sizing for said applications as summarized in Section 3.2.
A flowchart of the structure in the developed optimization algorithm is seen in Figure 4.1. In the following, the different parts of the algorithm are described accordingly to the order in which they appear in the algorithm including how the parts treat the data presented to them and how the data is moved forward.

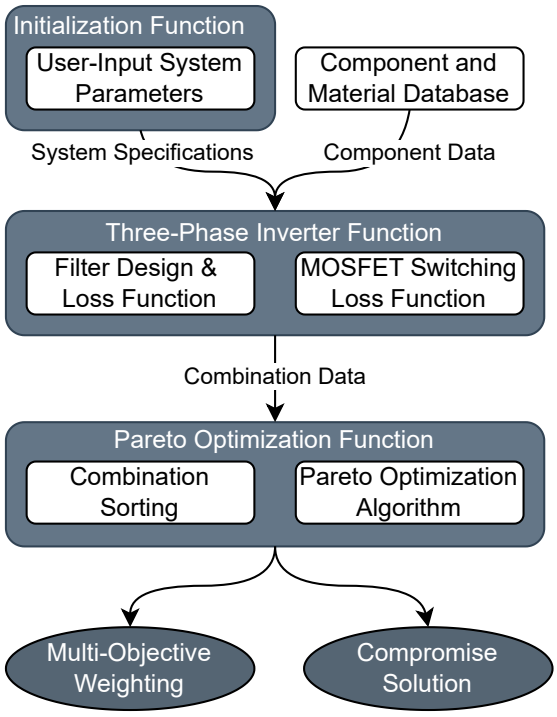


Figure 4.1 Flowchart showing the overall structure of the developed MOO algorithm.

4.1.1 Initialization Function

The first part of the algorithm is the initialization function. The initialization function is the main script where the user inputs the system specifications such as desired output current, DC-link voltage, and desired output voltage. It is also here that the user can alter the weighting coefficients, which are used in the optimization scheme later. The initialization function then calls the three-phase inverter function, which is a separate script doing the primary data generation and handling.

4.1.2 Three-Phase Inverter Function

In the three-phase inverter function, the first operation performed is the definition of the switching-frequency sweep range, followed by defining the thermal-network constants. These are the allowable $T_{\mathrm{J,mean}}$, T_{A}, and the TIM's thermal resistivity, R_{TIM}. Followed by this is the loading of the heatsink database, which is used later. After this, the material recycling rates of Table 2.3 are loaded for later use.
Next, the switch database is loaded and in this application, only the SiC MOSFETs with the TO247-4 package and a voltage rating of 1200 V are used as described in Section 2.4.2. The MOSFETs and their corresponding database entries are found in M. Then the average drain-source on-resistance is calculated for each switch, based on Equation (3.5), and saved for later use.

Next, the data matrix initializations occur, but for this, the two inductor core databases are loaded. This is done as it is required to know the number of cores, the number of switches, and the number of switching frequencies, in order to generate the data matrices. The first matrix being defined is the one containing the most information about the combinations. This is a $n_{\mathrm{SiC}} \cdot n_{\mathrm{Cores}} \cdot n_{\mathrm{fsw}}$ by 23 matrix. The data saved in the matrix' columns are introduced in the following:

- Column 1 contains the switching frequency
- Column 2 the switch-database entry
- Column 3 the losses of the present switch
- Column 4 the required heatsink volume for cooling the switch
- Column 5 the mass of the heatsink
- Column 6 the core number used in this combination
- Column 7 the mass of copper required to make the windings of L_1 at this frequency with this specific core
- Column 8 the volume of the windings
- Column 9 is a saturation and area product check to see if the core is applicable for L_1 (1 if applicable, 0 if not)
- Column 10 contains the required mass of copper to make L_2 with this specific core
- Column 11 is the volume of the windings
- Column 12 is the saturation and area product test check same binary representation as for L_1
- Column 13 is the mass of the specific core
- Column 14 is the volume of the core
- Column 15 is the recyclability rate of L_1 in this specific configuration
- Column 16 is the power loss of L_1
- Column 17 is the recyclability of L_2
- Column 18 is the power loss of L_2
- Column 19 is the entry of the chosen fast DC-link capacitor
- Column 20 is the capacitance of a singular capacitor chosen
- Column 21 is the volume of the capacitor
- Column 22 is the number of the chosen capacitor required in series to handle the voltage
- Column 23 is the number of chosen capacitors required in parallel to meet the capacitance.

It is noted that a lot of redundant data is saved in this matrix. The matrix can be split into three matrices as the switch-dependent columns (1-5), core-dependent columns (6-18), and fast-capacitor columns (19-23) are all independent of each other and only dependent on the switching frequency.

The next matrix is for the applicable MOSFETs. This is a n_{SiC}x3 matrix. The data stored in the columns is given below:

- Column 1 contains the recyclable mass of each switch
- Column 2 contains the total mass of each switch
- Column 3 contains the recyclability rate of each

A matrix is also initialized for saving the required information about the cores. The stored data is listed below:

- Column 1 contains the core-database entry
- Column 2 contains the core mass
- Column 3 contains the core box volume
- Column 4 contains a disassembly factor in column 4

Here, the disassembly factor is used for determining the recyclability rate of the inductor. This is based on that it is easier to disassemble an inductor made from E-cores than one made from a toroidal core.

The final initialization, which is moved between functions, is a vector for the non-changing capacitors. These are the slow DC-link capacitors and the filter capacitors. The data and the corresponding column is shown below:

- Column 1 is the obtained slow DC-link capacitance
- Column 2 is the slow DC-link volume
- Column 3 is the filter capacitance
- Column 4 is the total filter capacitor volume
- Column 5 is the entry of the used electrolytic capacitor in the DC link
- Column 6 is the entry of the used film capacitor in the filter
- Column 7 is the required number of the used electrolytic capacitors in series to reach the desired voltage handling capability
- Column 8 is the required number of the used electrolytic capacitors in parallel to reach the required DC link capacitance
- Column 9 is the required number of the used film capacitors in parallel to reach the required filter capacitance

As all matrices are initialized, the order of the calculations follows below.

The first calculation is for the slow DC-link capacitors. The calculation is shown in Equation (3.10) and remains constant throughout the algorithm. Next, all the capacitors in the database are checked for applicability in the DC link. This is done by first checking how many are required in series to withstand the input voltage and then how many are required in parallel to obtain the required capacitance. If more than two of the specific capacitor is required in series or more

than four of the capacitor is required in parallel, the specific capacitor is removed as an option. Between the remaining capacitors, the total volume is calculated and the combination with the lowest volume is chosen. The five required parameters, as described in the initialization above, are then saved to the non-changing capacitance vector.

Now the program starts sweeping the switching frequency. In every iteration, the new fast DC-link capacitance is calculated based on Equation (3.9). Then the same series and parallel calculations as for the slow DC-link capacitors are performed and the specific capacitor resulting in the smallest total volume is chosen. Then the capacitor entry, volume, capacitance, number in series, and number in parallel are saved in the big data matrix. It is noted, that electrically it might be better to have at least one of these per phase, as it can then be placed close to the high-side drain and act as a decoupling capacitor.

4.1.3 Filter Design Function

Next, the filter function is run every switching-frequency iteration. The calculations are follow the procedure as shown in the filter part of Section 3.2. Once again, the film capacitors in the database are investigated based on the experienced voltage, required capacitance, and also the ripple current. Then the filter inductors are designed followed by the power loss, saturation and area product calculations. This is done for all the cores in the database. All the information is then sent out from the filter function back to the three-phase inverter function. In the three-phase inverter function all the inductor data is then saved in the corresponding locations in the big data matrix and for the first switching-frequency iteration, the filter capacitor data is saved in the non-changing capacitor vector, alongside the slow DC-link capacitor information, as these calculations are independent on the switching frequency.

4.1.4 MOSFET Switching Loss Function

Next, the nested switch loop is entered and the switching loss function is called for each usable switch every switching-frequency iteration. Then, based on the power losses, for each switch, the smallest usable heatsink from the database is chosen, and its corresponding data is saved in the big data matrix. After the entire switching frequency range has been swept, the big data matrix is sent back to the initialization function. Here, it is sent to the optimization function.

4.1.5 Optimization Function

The first operation in the optimization function is the generation of the combination matrix. Each row in this matrix will correspond to a specific combination, unlike the big data matrix. The size of this matrix is the product of all iterated frequencies, number of cores squared, and number of applicable switches by 13, $n_{fsw} n_{cores}^2 n_{switches}$ by 13. Then, every combination is generated based on the different data matrices and vectors. The recyclability is also calculated in this process. Here, it is noted that the inductors' disassembly factor dictates the recycling rate. If the inductor is more difficult to disassemble, due to its core, the lower recycling rate, given in Table 2.3, is used.
After all combinations are generated, all the invalid combinations are deleted. The invalid combinations include the ones where either a core is saturated or its area product is smaller

than the required but it also includes combinations with an impossible heatsink requirement. The impossible heatsink requirement occur when the thermal network model, introduced in Section 3.2 Equation (3.23), requires a negative thermal resistivity to satisfy the model. After this, the remaining combinations are ready for the optimization scheme.

In the optimization scheme, the combinations are checked for domination as described in 2.1 with Equation (2.2) and Equation (2.3). Each of the Pareto optimal points is normalized with the highest value of each objective and then checked in Equation (2.1). This is done to find the Pareto optimal solution, which results in the highest value at the given weighting vector, which is input at the startup. No specific weighting vector is introduced in this work, however the option is implemented for use.

The results from running the algorithm, with the specifications for the case study and a switching frequency range from 10 kHz to 100 kHz, with 1 kHz intervals, are presented in the following.

General Pareto Result Analysis

The Pareto optimal solution are seen in Figure 4.2, Figure 4.3, and Figure 4.4, which are two-dimensional representations of the three-dimensional solution space.

From Figure 4.2, Figure 4.3, and Figure 4.4, it is seen that the efficiency is generally lowered when the other two objectives increase. Therefore, it is also visible that the power density and recyclability generally follow each other. However, exceptions occur when larger heatsinks are required. When the heatsink volume is increased, it is the result of MOSFETs in the Pareto points at higher switching frequencies requiring larger heatsinks. The larger heatsink lowers the power density, but as aluminum is the material with the highest recycling rate, out of the materials from which the large components are made of, there is an increase in the recycling rate of that Pareto point. The most notable result is that all Pareto optimal points use switch number 3.

Switching frequency is the driving factor, the changing components are the responses and the change in objectives are the results. However, the efficiency is also directly impacted by the switching frequency. The different components used at the different Pareto optimal solutions are presented in Appendix E.

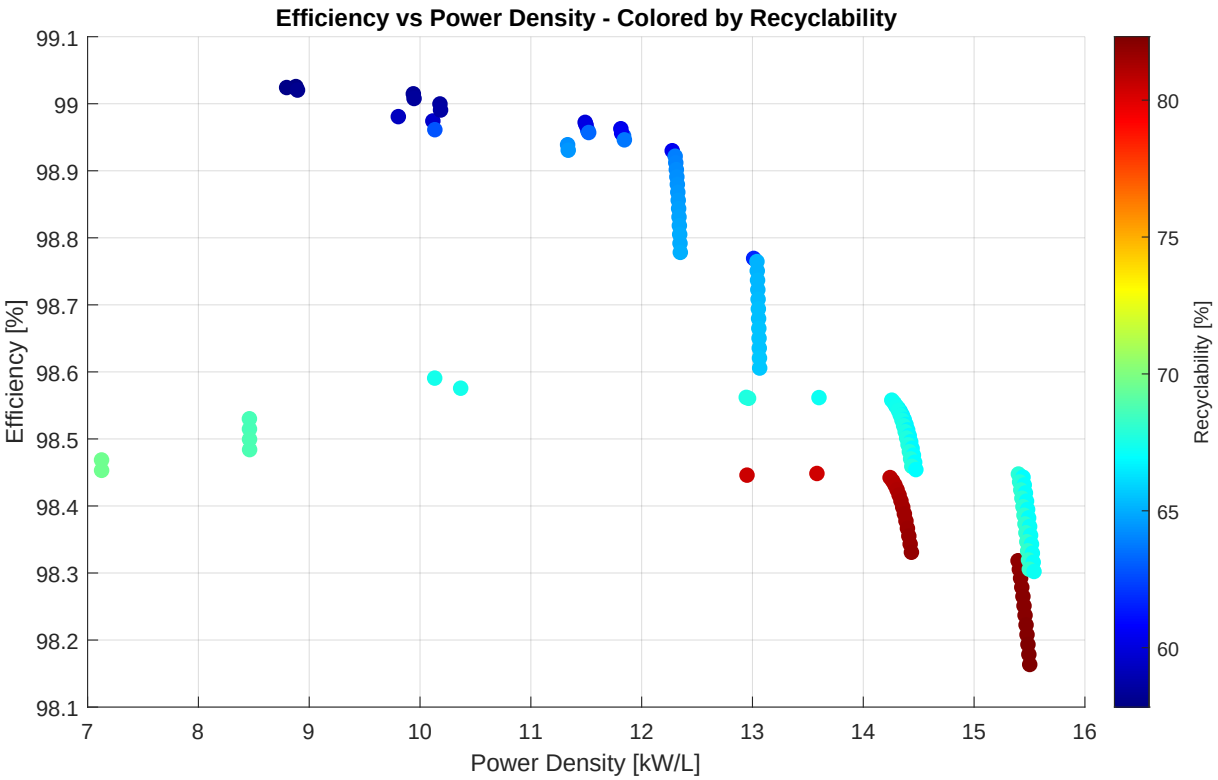


Figure 4.2 2D plot of the Pareto optimal solutions showing efficiency and power density colored by the recyclability.

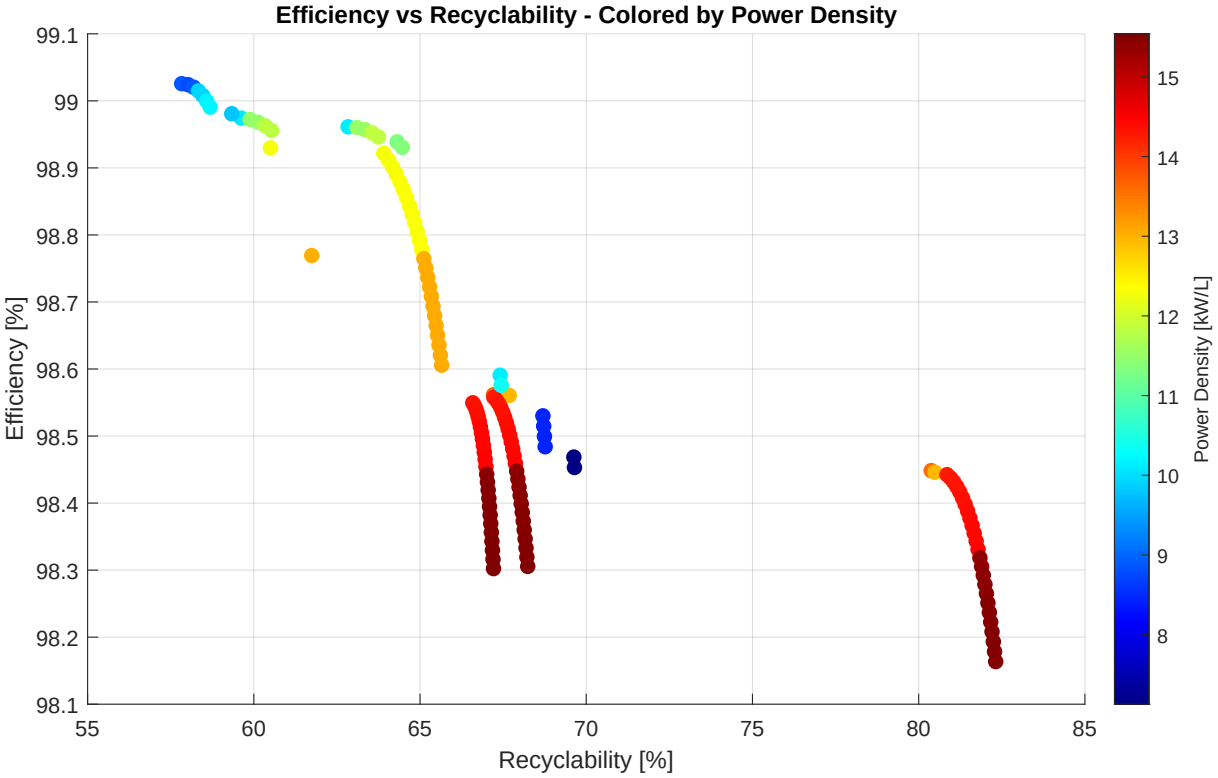


Figure 4.3 2D plot of the Pareto optimal solutions showing efficiency and recyclability colored by the power density.

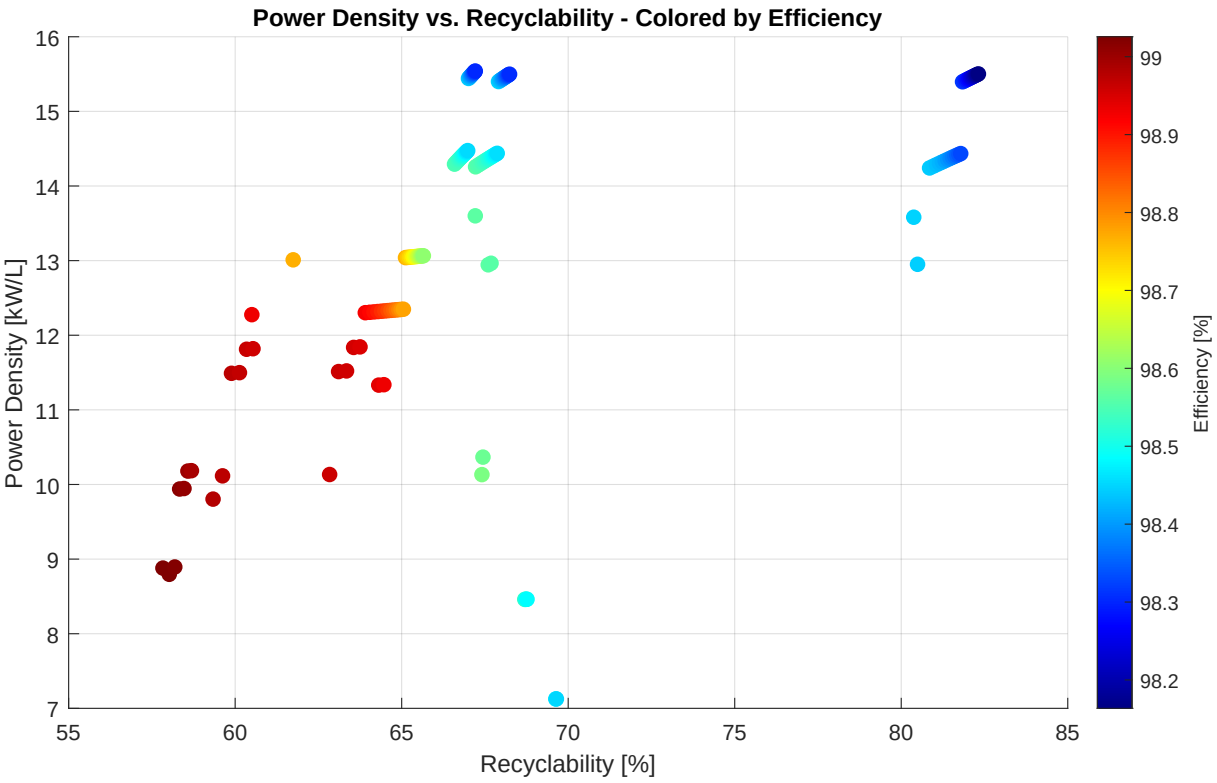


Figure 4.4 2D plot of the Pareto optimal solutions showing power density and recyclability colored by the efficiency.

Compromise Solution

The compromise solution is introduced first. The algorithm informs that combination 30638 results in the compromise solution. Switch 3 from the database, which is SCT070W120G3-4AG by STMicroelectronics, is used in combination 30638. Furthermore, core 16, which is 00K114LE060 by Magnetics Inc., for L_1, and core 14, which is 00X6527E040 by Magnetics Inc., for L_2 are used in this combination. The switching frequency for this combination is 43 kHz. The compromise solution results in an efficiency of 98.16%, a power density of 15.5 kW/L, and a recyclability of 82.32%.

Multi-Objective Optimization with Different Weights

The three objective weights are set to sweep from 0 to 1 with their sum always equaling 1. This is shown in the equation below:

$$w_1 + w_2 + w_3 = 1 \tag{4.1}$$

This results in a binominal coefficient of $\binom{n+k-1}{k-1} = \binom{12}{2}$ resulting in 66 different combinations. However, this does not mean that there have to be 66 unique combinations, each being a respective solution to a weighting vector, but instead that there is 66 unique weighting vectors. As the objectives are normalized with respect to the highest value of each objective, large variations within the objective will result in this objective being prioritized when finding the maximum cost function per weighting vector. To visualize the results, a heatmap is seen in Figure 4.5.

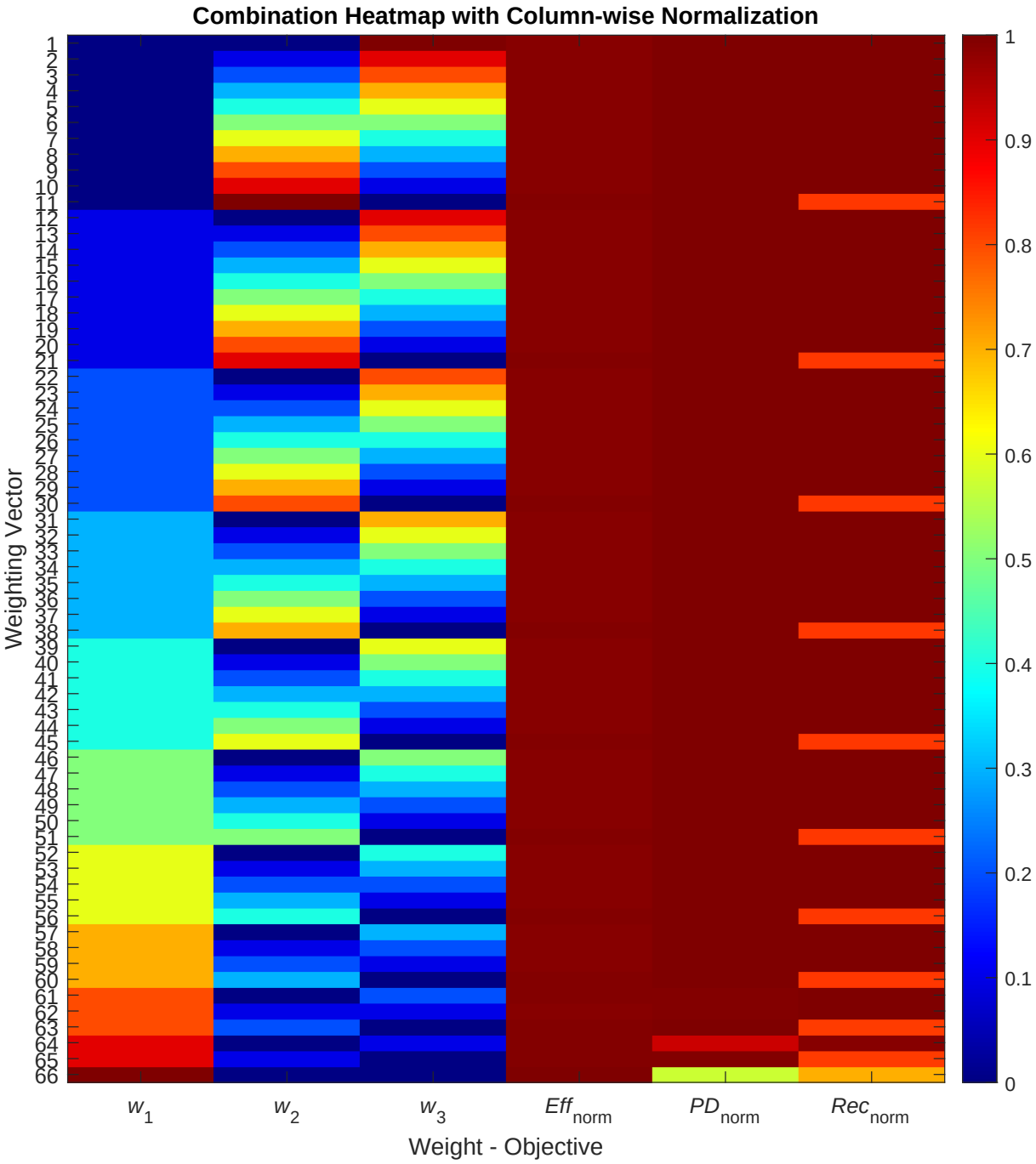


Figure 4.5 Combination heatmap with column-wise normalization with zero as reference.

An alternative heatmap is found in Appendix J. This heatmap does not have zero as the base for the normalization, but instead the lowest value in each column. This enables seeing the relative difference instead of the absolute.

In Figure 4.5, the three left-most columns are the weightings and the change in color indicates the rise in numerical value. The three right-most columns are normalized values of the objectives, resulting in the maximum cost function value at the given weighting vector. The heatmap shows that, regardless of the applied weighting vector, the efficiency remains high. This is primarily because of the small relative change in efficiency, throughout all combinations, being 0.8 pp. It is also seen that the power density is often prioritized, as it has the largest relative difference

between different combinations. The smallest power density is 57.8% of the largest. Generally, the power density has the same color in the heatmap except for two cases. Weighting vector 64, with $w_1 = 0.9$ and $w_3 = 0.1$, the color becomes more orange, but the power density value is still at 92.4% of its maximum. Then, with weighting vector 66, only the efficiency is weighted and this is where the power density drops to 57.1% of its maximum and the recyclability drops to 57.8%. The reason the power density drops when the efficiency is weighted is, as described above at the introduction of the Pareto optimal results, because of the inverse behavior between efficiency and power density. It is also noted that the recyclability is often maintaining a high value, which again stems from a larger relative difference resulting in a maximum difference of 24.5 pp. The occurrence of the different combinations, chosen by the maximization, is shown in Table 4.1 below:

Table 4.1 Occurrence of combinations resulting in maximum cost function, based on the different weighting vectors.

Combination	Occurrence
77	1
13310	1
20222	1
24190	1
25230	1
27278	1
30606	8
30638	52

Here, it is noted that combination 30638 is the compromise solution as introduced earlier. Based on the analysis, it is chosen that the compromise solution is used for the remainder of this work. This combination is, by definition, a good all-round solution and this is also shown when looking at the analysis of the different weighting vectors. Therefore, the compromise solution with these system parameters and based on the component database will make an eco-friendly design, without drawbacks in the prioritized existing design objectives, efficiency and power density.

4.1.6 Components for the Design

The components from the chosen combination are now investigated to see if and how they can be utilized in the eco-design implementation tests. Six electrolytic capacitors of number four in the database are used as the slow part of the DC link. Two are used in series, as the voltage rating is 450 V per device, and to achieve the required capacitance, three of these series connections are used in parallel. This results in a slow capacitance of 330 µF. However, the required capacitance for the DPT might be different from the one for the continuous SPWM operation of the inverter. Instead, the same footprint of the capacitors is used to make the implementation representative of the three-phase inverter design. As introduced in Section 2.4, the required capacitance is based on the inductance, the DC-link voltage and the test current. Thus, the capacitance is determined in the generation of the DPT setup.

Film capacitor number six, from the database, is to be used for the fast DC-link capacitor. Only one is required for the entire VSI and this results in a 7 µF capacitance. However, the algorithm

is not taking the decoupling property into account and thus it is beneficial to add a per-phase recalculation in the algorithm. For the eco-design implementation test boards, it is decided to use one of the 7 µF filter capacitors on each board regardless. The reason for picking this larger than required capacitor, is to see how the designs can be made around larger components, which can make the layout process more difficult.

During the development of this thesis, the SCT070W120G3-4AG SiC MOSFET by STMicroelectronics, chosen in all the Pareto optimal solutions, is not available. Therefore, it is chosen to use the SCTWA40N12G2-4AG SiC MOSFET by STMicroelectronics instead, as they have very similar ratings. However, SCT070W120G3-4AG uses STMicroelectronics' third generation SiC chips, whereas SCTWA40N12G2-4AG uses their second generation. This results in a reduced performance of the used MOSFET, however, with the comparative study testing the MOSFET relative to itself, the impact of the lower generation is negligible.

As the MOSFETs are only subjected to the short pulses of the DPT no continuous power dissipation occurs. Based on this, it is decided that a heatsink is unnecessary. It is therefore assumed that the devices are kept at room temperature and that the small temperature variations in the room will not result in significant deviations.

4.2 PCB Design

This section introduces the PCB design strategy proposed in this thesis, with focus on how eco-design principles are integrated to improve EoL disassembly while reducing mechanical strength but maintain electrical performance. The following subsections cover the layout of a half-bridge converter, followed by the eco-design methodology and the implementation into half-bridge converter PCBs. Lastly, the mechanical test specimens are presented.

The designs are implemented on PCBs configured as half-bridge converters, which serve as the foundation for the electrical performance tests. For the mechanical tests, however, dedicated unpopulated PCBs, without any copper traces or components, are used. These mechanical test specimens are specifically adjusted in size to fit within the testing setup and isolate the mechanical effects to the perforations.

To ensure comparability between designs, the cut-out holes and slots used across all boards are kept at fixed dimensions. Other perforation shapes or sizes are not investigated in this project. Furthermore, this study uses two-layered PCBs for all designs, although the underlying principles and methods can be extended to multilayered boards in future work.

4.2.1 Eco-Design Strategy

A key aspect in the proposed eco-design is the grouping and placement of components by either material type, function, or EoL treatment strategy. By arranging component groups together, the separation and disassembly process at the EoL can be simplified, making the recovery of valuable materials or components more efficient. Similar components, with the same recycling process and composition, is ideally positioned in easily distinguishable zones to minimize the

time, tools, and effort required for disassembly. This is illustrated in Figure 4.6, with the dotted lines being the perforations and the components are grouped as depicted.

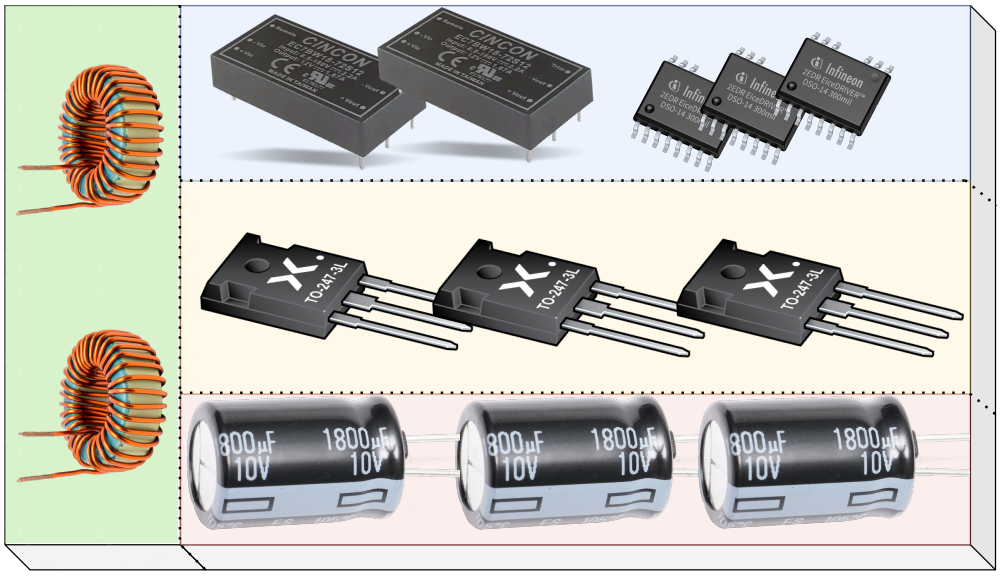


Figure 4.6 Illustration of a possible implementation of perforations on a PCB concerning component groups.

In Figure 4.6, a possible design structure is illustrated with the top part of the PCB being equipped with isolated DC/DC converters and gate driver Integrated Circuits (ICs). The middle part is populated with the switching devices, and the lower part is equipped with capacitors. The size and shape of the perforations, which are used to define the break-away zones, must be selected. Here, the investigated perforations are in the form of circular cut-outs, denoted holes, and elongated cut-outs, denoted slots.

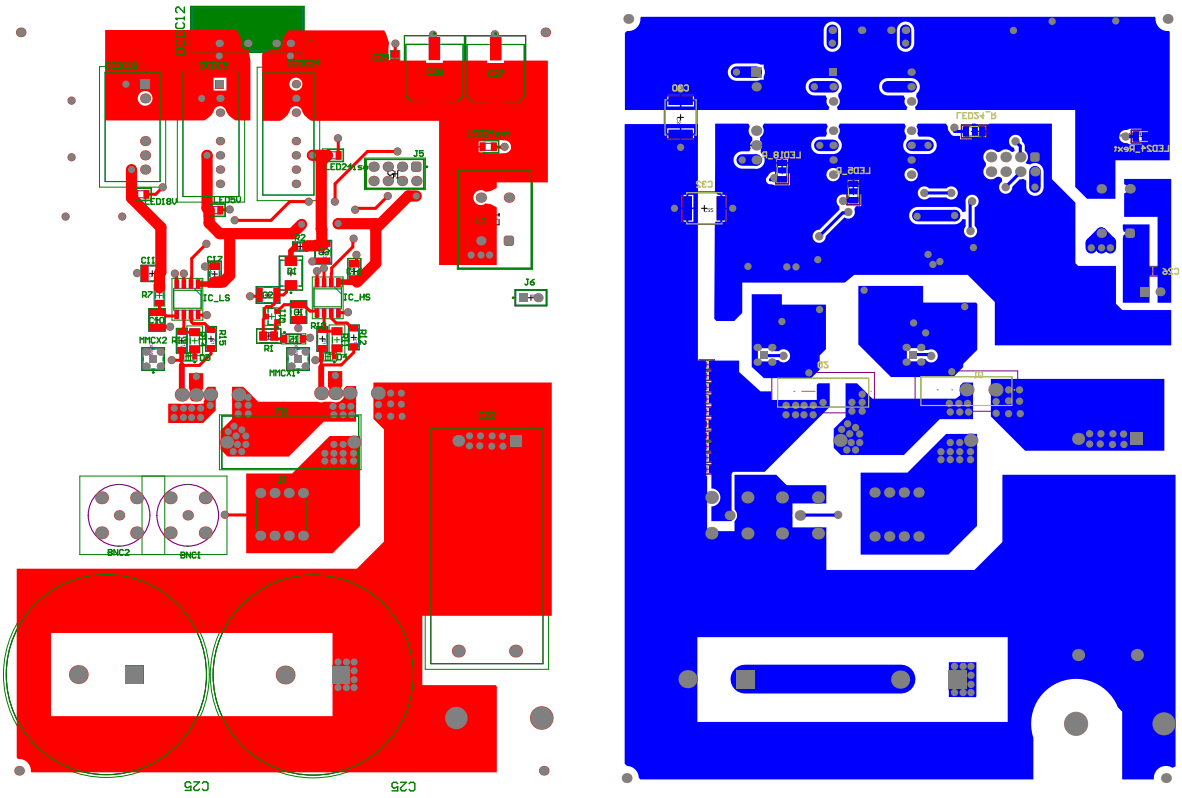
By including the holes and slots, dismantling is simplified as the recyclers can then easier use the breakage lines for guidance and use the different tools at their disposal, introduced in Section 2.2.4. Therefore, it is assumed that the recycler has access to the required tools to enable breaking of the structurally weakened PCBs. Thus, the perforation holes need to be so high in count that an operator can break the PCB. Furthermore, for the slot-based approach, applying the wider perforation type, the usage of tools such as side-cutters and pliers is possible. This thesis investigates, how the flexural strength is impacted by the different implementations and how they compare to a non-perforated design, to quantify how much easier the disassembly becomes. Using the flexural strength as the metric, the analysis is conducted without regard to the different ways a PCB can be dismantled.

4.2.2 Conventional Design as the Comparison Baseline

The design choices and layouts used for the half-bridge converter boards developed for this thesis are described in the following.

Layout and Circuit Considerations

A conventional half-bridge board is designed without any cut-outs. This unmodified board is used as the benchmark, allowing the mechanical and electrical impacts of the perforated designs to be evaluated against a standard reference. Figure 4.7 shows the top and bottom layout of the conventional half-bridge converter board. This layout has been developed according to the common practices outlined in Section 2.1.3. The half-bridge boards have overall dimensions of 105.16 mm in width and 142.24 mm in length.



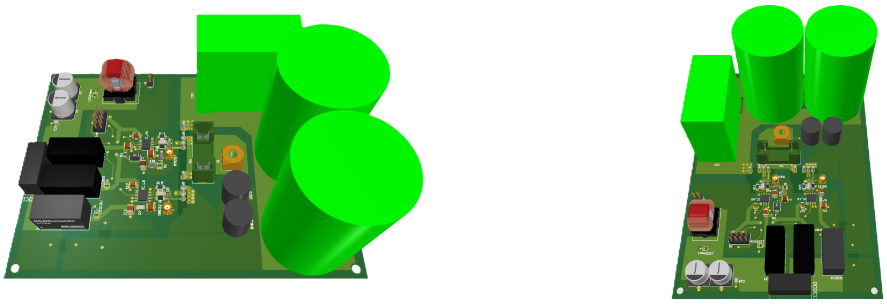
(a) **(b)**

Figure 4.7 PCB with a conventional design strategy: a) top side b) bottom side.

The design procedure is initialized from the top right corner, where the external voltage supply is connected to the PCB. Here, the 24 V is filtered through a common-mode choke inductor, L1, and four filtering capacitors, of which two are electrolytic, C27 and C28, and the other two are ceramic, C26 and C29. All of the filtering components are implemented based on the recommendations from isolated DC/DC converter manufacturers. [55]
The 24 V plane supplies two DC/DC converters, of which one generates 12 V and the other 24 V. The 12 V plane then feeds two additional DC/DC converters, with one producing 5 V and the other 18 V. Furthermore, a film and a ceramic capacitor, C30 and C31, are used to decouple the ground of the external 24 V supply and the power planes ground, while ensuring that the potentials are not allowed to float completely relative to each other. In addition, the ground of the gate driver logic circuit has the option to be decoupled in the same way, by applying the same two capacitors between the logic ground and the power ground, which are named C32 and C33.

The 5 V converter supplies the gate driver ICs. The 18 V DC converter supplies the low-side gate driver IC, denoted as IC_LS. The 24 V DC converter supplies the high-side gate driver IC, denoted IC_HS, through a bootstrap circuit. The gate driver circuits are essential for the operation of the MOSFETs, named Q1 for the high-side and Q2 for the low-side MOSFET, especially on the high side. Because N-channel MOSFETs require a positive gate-to-source voltage to turn on, a bootstrap circuit is used to provide the necessary gate voltage to the high-side MOSFET even when the source potential is elevated higher than the supply. The bootstrap circuit and the gate driving circuit is explained in the following Section 4.2.2. To ensure that the DC/DC converters produce the desired voltages, four Surface-Mount Devices (SMD) Light Emitting Diodes (LEDs) are inserted to indicate if the DC/DC converters receive and produce the appropriate voltage. The connector J5 is the connection point for the external Micro Controller Unit (MCU). Two connections are for the logic-level gate signals, another connection can be used to deliver 5 V to the MCU, yet another is for ground connection, and the remaining four are left unconnected in the schematic, but soldered to ground. The many ground connections are introduced to maintain high signal integrity.

Below the gate driving circuits, the MOSFETs are placed. The MOSFETs' gate terminals are then connected with the gate driving ICs through turn-on and turn-off resistors, named R10 and R11 for the high side and R13 and R14 for the low side. The turn-off gate resistor is furthermore connected to a Schottky diode, which ensures that the branch is not used for turn-on. Thus, the turn-on and turn-off transients can be tuned independently. The high-side switch's drain terminal is connected to the DC+ plane, whereas the low-side switch's source terminal is connected to ground. The source terminal of the high-side switch and the drain terminal of the low-side switch are connected via a power plane on the top and bottom side of the PCB, which is denoted as the switch-node. To improve the switch-node's current capacity, vias are inserted close to the switch terminals and close to the fuse, which left side is connected to these planes. The fuse, denoted as FH, is inserted to ensure that, in the case of an overcurrent occurring, the components are protected. The right side of the fuse connects to the power terminal, J1, where for example, the load inductor during the DPT is connected. It is noted that, similar to the power planes between the switches, the same strategy is selected for the plane between the fuse and power connector, with copper planes on the top and bottom sides to enhance current carrying capacity. Next to the power terminal, the Bayonet Neill–Concelman (BNC) connectors for measurements are placed along 15 shunt resistors for measurements of the DUT current. The right BNC, BNC1, connects to the power plane, whereas the left BNC, BNC2, connects the two ground planes. The last section on the PCB is the DC-link capacitance along with the respective DC-link connectors. Two electrolytic DC-link capacitors, which are named C25, and a film capacitor, C22, is placed very close to the high-side MOSFET. A three-dimensional view of the conventionally designed half-bridge PCB is presented in Figure 4.8 below:



(a) (b)

Figure 4.8 A three-dimensional illustration of the conventionally designed half-bridge converter PCB.

In Appendix H, Section H.9 ref the remaining PCBs are attached. In Appendix ref a complete list of the used components is presented.

Gate-Driving Circuit

The two supplies for the driving side of the gate driver is seen in Figure 4.9.

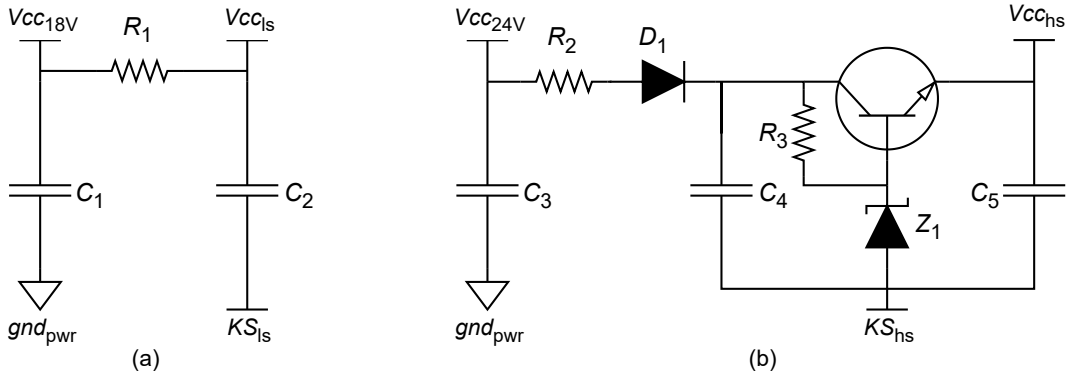


Figure 4.9 Gate driver voltage supplies (a) the low-side supply with decoupling, (b) high-side supply with bootstrap capacitor and emitter follower voltage regulator[56].

The low-side MOSFET's gate driving circuit is supplied by the circuit seen in Figure 4.9a. The input to the low-side gate driver IC is supplied by the decoupling capacitor C_2, this decoupling capacitor is furthermore charged through the resistor R_1 by C_1, which is in parallel to the isolated 18 V DC/DC converter. The high-side MOSFET's gate driving circuit is supplied by the circuit in Figure 4.9b. Here, a bootstrap circuit is used to provide the required gate-source voltage for the high-side MOSFET. It uses the MOSFET's Kelvin-source connection as the reference. This enables the required gate-to-source voltage of 18 V despite a bouncing reference. The bootstrap circuit works as follows. When the high-side MOSFET is turned off and the low-side MOSFET is turned on, the source terminal is pulled close to power ground potential. At this point, the bootstrap capacitor, C_4, is charged by C_3, which is in parallel with the isolated 24 V DC/DC converter, through the diode, D_1. Additionally, D_1 is reverse biased when the Kelvin-source voltage reaches the DC-link voltage. Once charged, C_4 acts as the voltage source when the high-side MOSFET turns on, even though the source potential rises. Additionally, an emitter following voltage regulator, consisting of a bipolar junction transistor Q_1, a resistor R_3, and a zener diode Z_1, ensures that the voltage across C_5 remains close to the zener voltage.

This regulation process, however, only functions effectively if the MOSFET's off-period is long enough for the capacitors to recharge, compensating for the charge drawn during gate operation.

4.2.3 Eco-Design Implementations

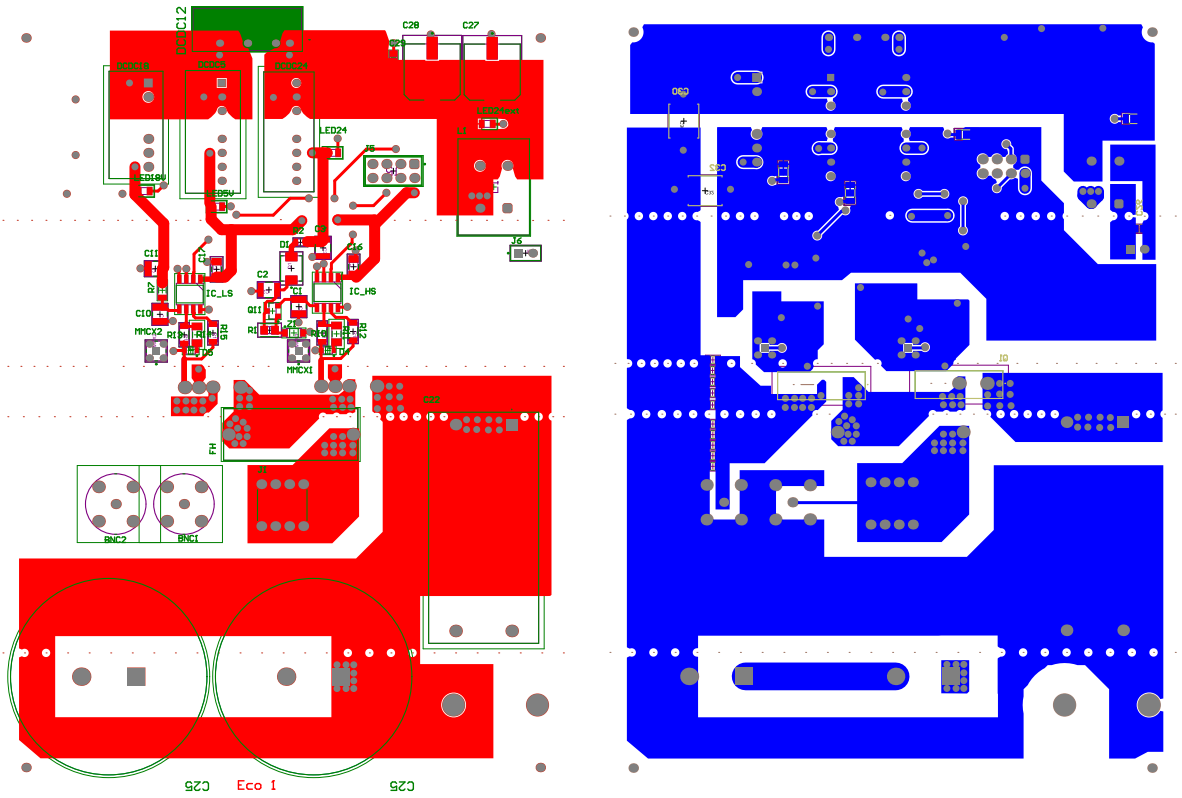
The implemented eco-design layouts are based on the previously presented conventional design. The proposed eco-designs are implemented on each half-bridge PCB with four distinct perforation lines. These lines strategically divide the board into five zones, corresponding to the component groups, enabling easier separation of the sections.

These breakage lines are realized by different cut-outs, which are implemented on the mechanical layer in the design program. Each perforation is placed along a predefined breakage line on the PCB. The spacing between perforations and the perforation count are adjusted based on the desired perforation percentage, which is calculated by multiplying the length of each cut-out by the total count of that perforation and dividing by the width of the board.
To decrease the risk of electrical breakdown, a keep-out area, of 0.25 mm, is set around each cut-out, which increase the local distance between layers. The perforations are aligned in a row to induce a controlled breakage when force is applied.

For the hole-based approach, circular cut-out holes with a diameter of 1 mm are used. This diameter is chosen not to accommodate clipping tools but to ensure that the number of cut-outs reduces the boards' strength strategically and induces a clear breakage. By keeping the hole size constant, the investigation can isolate the effects of varying the perforation percentage without introducing additional variables related to geometry.
The slot dimensions are selected as elongated octagons, with a length of 4.57 mm and a width of 2.54 mm, enabling smaller side-cutters and similar tools to fit in the cut-out. Both perforation types' dimensions are kept consistently across all designed PCBs.

The division into the zones is conducted as described in the following. The first line separates the 24 V external supply and the respective filtering and decoupling components, along with the DC/DC converters from the gate driving circuit. The second perforation line is introduced between the gate driving circuits and the MOSFETs. The third perforation line is introduced between the MOSFETs and the power connection and measuring components as well as the film capacitor. Lastly, the fourth perforation line is introduced to separate the DC-link capacitors. This is illustrated in Figure 4.10, where the four perforation lines separate the described component groups.

This functional zoning is based on the components' functions, but also on their type and composition. The PCBs design contained perforation percentages of 25 and 50% for the hole-based approach. These boards are denoted as "Eco 1" and "Eco 2" and the PCB configuration is presented in Appendix H, Section H.3 and Section H.4. The perforation percentages for the slot-based boards are 25, 50 and 75% and these are denoted as "Eco 3", "Eco 4" and "Eco 5", is presented in Appendix H, Section H.5 and Section H.6 and Section H.7. Furthermore, another board is designed with a combination of the hole- and slot-based approach and with a perforation percentage of 50%. This combination board is denoted as "Eco SnH" on the actual



(a) (b)

Figure 4.10 PCB "Eco 1" with a 25% perforation hole-based design strategy: a) top side b) bottom side.

board, but also referred to as "EcoSH" hereafter. The layout configurations of all half-bridge PCBs are found in Appendix H.
Minor adjustments are made to the trace routing, where necessary, to accommodate the placement of cut-outs and to prevent interference between traces, components and perforations. It is noted that the perforations are placed in close proximity to the MOSFETs, which might make separation by bending or snapping more difficult at EoL.

For the slot-based designs, it is not possible to reach exactly the same perforation percentages as with the hole-based designs without changing the slot dimensions. To keep the comparisons consistent, the slot size is kept fixed across all configurations, and only the number of slots is varied. The selected cut-out configurations are summarized in Table 4.2.

It is noted that the design with 75 % perforation using only holes, denoted with (*), is not implemented. As for this perforation percentage, the required number of holes combined with their keep-out zones leaves no space for copper between the perforations.

4.2.4 Mechanical Test Specimens

The boards used for the mechanical testing are designed as plain PCBs with copper fully covering both the top and bottom surfaces. These boards are not meant for electrical operation but are specifically made to test the mechanical behavior. To match the configuration of the electrical test boards, the mechanical specimens used the same types of perforations and perforation

Table 4.2 Summary of cut-out implementations on the half-bridge boards and mechanical test specimens.

Board Type	Cut-out Type	Number of Cut-outs	Perforation Percentage
Half-Bridge Converter Boards			
	Holes	27	25%
	Holes	53	50%
	Holes*	79	75%
	Slots	6	26%
	Slots	11-12	51%
	Slots	16-18	74%
	Holes and Slots	18, 27, 28, 28 Holes and 6, 6, 5, 6 Slots	49%
Mechanical Test Specimens			
	Holes	15	25%
	Holes	30	50%
	Holes*	45	75%
	Slots	3	23%
	Slots	7	53%
	Slots	10	76%
	Holes and Slots	12 Holes and 4 Slots	50%

percentages. However, each mechanical specimen included only a single perforation line. This setup enabled a direct measurement of the breaking force for each specific perforation pattern. It is assumed that the presence of copper itself has only a minor influence on the breaking force, so the boards are fabricated without the removal of copper to assimilate traces.

To fit the test setup, the mechanical specimens are made narrower than the electrical half-bridge boards, resulting in 60.2 mm in width. Without this change, part of the specimen will extend beyond the rollers, which can lead to multi-dimensional bending and inaccurate test results. By keeping the specimen width within the supports, the test can apply a one-dimensional bending force, yielding accurate data. Across all perforation types, the dimensions of the mechanical test specimens are kept constant to ensure that the results are comparable. These dimensions are summarized in Table 4.3. As shown in Figure 4.11, the mechanical test specimens include

Table 4.3 Test specimen dimensions.

Parameter	Value [mm]
Length	140.2
Width	60.19
Thickness	1.6

only one perforation line. In this example, the board combines holes and slots to achieve a total

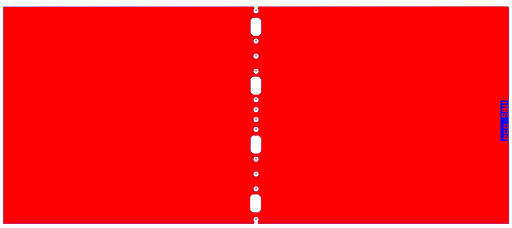


Figure 4.11 Layout of the boards for mechanical testing with 50 % Perforation and a combination of holes and slots.

perforation percentage of 50 %. All mechanical test specimens can be found in Appendix H. To reach this percentage, the holes and slots are placed so that their centers align. However, the spacing between the holes near the center slots is slightly different from that near the outer slots, although within each zone, the distances between cut-outs is kept consistent. For the remaining test specimens, the distance between the cut-outs is kept consistent between each perforation type. In total, six distinct perforation designs are implemented and tested, alongside the conventional (non-perforated) reference design.

With the physical board design described, the next step is to evaluate how these structural modifications affect the electrical behavior of the system. Therefore, the following chapter presents the DPT, which is used to analyze switching behavior, voltage overshoots, and potential parasitic effects across the different perforation designs.

4.3 Performing Double Pulse Test

In this section, the setup for performing the DPTs is introduced, followed by the results from the performed tests. The first part is designing an inductor for the DPT, and choosing DC-link capacitors based on the requirements. The second part is developing the setup for the DPT, followed by the third and last part being the results.

4.3.1 Design of Ramping Inductor

When choosing a ramping inductor it is important to note that the core is likely to experience quite a large magnetic flux density due to the tests requiring high currents. Additionally, a larger inductance results in a longer ramping period but also an increased flux density. Longer ramping periods have both benefits and drawbacks. The benefits are that a simpler DPT program can be used as the time constant of the tests are increased. Another benefit, which is very necessary for half-bridge DPT setups with a low-side DUT and a high-side bootstrap gate driver, is that the low-side switch can be pulsed initially to charge the bootstrap circuit. This is done by turning on the low-side switch for a short interval, giving the bootstrap circuit a small period for charging, followed by a much longer period, in which the inductor can discharge the small current it ramped while the DUT is conducting. This is visualized in Figure 4.12:

The bootstrap sequence also enables the high-side switch to be the DUT. When this is the case, the off-period is not required to be as long, as no current is ramped in the inductor when the inductor is parallel to the low-side switch. The program developed for performing the DPTs in this project is found in Appendix K where Section K.1 describes the main program in detail and Section K.2 contains the full program.
The specific charging periods required for fully charging the bootstrap capacitor can be established iteratively with the final setup. Similarly, the required period of the inductor discharging must also be tuned iteratively.
The drawbacks of large inductors are that the core of the inductor can saturate, and the larger required period can result in a larger power dissipation in the windings. The saturation drawback is circumvented by using an air-core inductor, as it then behaves linearly because there is no core to saturate. The large power dissipation is not a problem unless an extremely high inductance

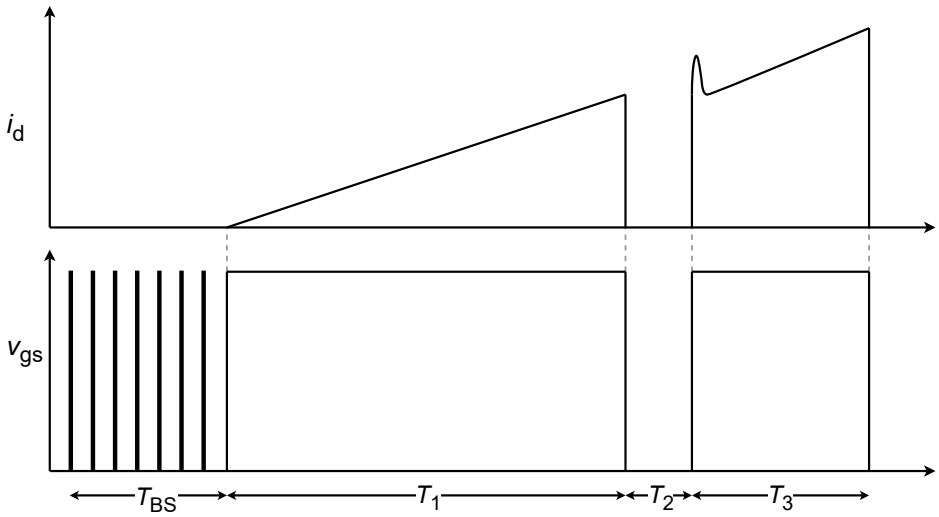
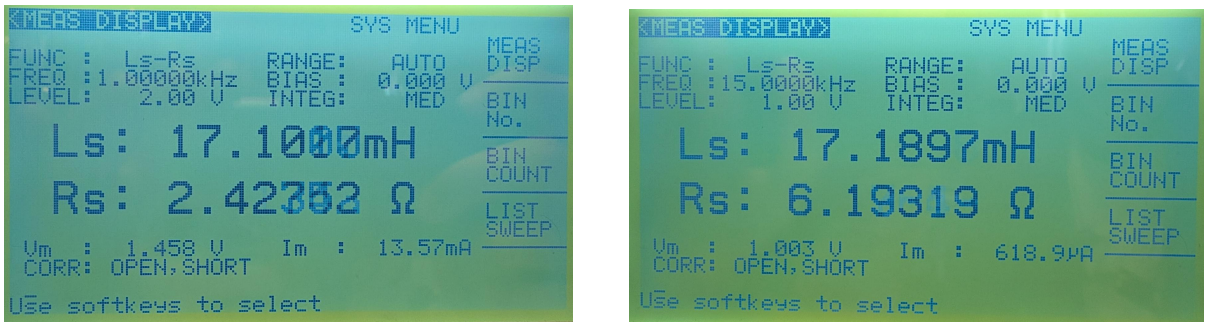


Figure 4.12 Low-side DUT drain-current and gate-voltage waveforms with bootstrap charging pulses preceding the ramping period.

is used or if a very high current is required. An example of the available time during which heat generation occurs in the inductor is given. As the device in this thesis is rated for 33 A and the application only has peak currents of 25 A, a large inductor with 10 mH subject to 700 V will only require 360 µs to reach this desired current based on Equation (2.13). Thus, the dissipated energy is very small.

It is decided to use a cable spool with a length of 200 m and a conductor cross section of 1.5 mm^2 as the air-core inductor. After having connected the required terminals to the cable ends a Hewlett Packard 4284A LCR meter is used to find the series inductance and resistance of the inductor. The measurements where performed at 1 kHz and 15 kHz and are shown in Figure 4.13:



(a) **(b)**

Figure 4.13 Series inductance and resistance measurements with 4284A LCR meter by Hewlett Packard: a) 1 kHz b) 15 kHz

The measurements showed that the inductance remained almost constant with a difference below 1% as the values are between 17.1 mH and 17.2 mH. However, the resistance varied by almost a factor of 3. The varying resistance is of lesser importance. A quick calculation of the conduction loss shows that the inductor can ramp 25 A in 600 µs when subjected to 700 V. The average power loss over the inductor in the ramping period is calculated as half the test current squared multiplied by the resistance. Using 6.2 Ω results in a power loss of 970 W. However, as the period is 600 µs, the energy dissipated only adds to 591 mJ, which is far from enough to raise the temperature of the cable spool. The spool is shown in Figure 4.14:

Figure 4.14 Ramping inductor with air core.

As the inductance and test currents are determined, the DC-link capacitance is calculated based on Equation (2.14). Based on available capacitors in the laboratory it is decided that a 20 V voltage drop is acceptable. With this the capacitance is calculated as seen below:

$$C_{\mathrm{DPT}} \geq \frac{L_{\mathrm{ramp}} I_{\mathrm{test}}^2}{2V_{\mathrm{dc}}\Delta V_{\mathrm{dc}} - \Delta V_{\mathrm{dc}}^2} = \frac{17\ \mathrm{mH} \cdot (25\ \mathrm{A})^2}{2 \cdot 700\ \mathrm{V} \cdot 20\ \mathrm{V} - (20\ \mathrm{V})^2} = 427\ \mu\mathrm{F}$$

Based on this, two 1 mF capacitors, each having a voltage rating of 400 V, are connected in series to achieve a total rating of 500 µF and 800 V. With the ramping inductor and DC-link capacitors, the next part is to set up the necessary measurement instruments before performing the DPT.

4.3.2 Setting up Measurements

When performing the DPT the DUT's drain-source voltage and drain current are used to calculate the power losses but also to evaluate the impact of the parasitics in the switch and in the board. Additionally, the gate-source voltage of both MOSFETs are monitored to ensure that no false turn on occur leading to voltage shoot-through. Additionally, the high-side MOSFET's current can be used along with the switch-node voltage and input voltage to estimate the reverse-recovery loss of the high-side MOSFET when the DUT turns on. The high-side MOSFET current is approximated as the difference in the low-side MOSFET and the load current and the diode voltage is approximated as the difference in input voltage and the switch-mode voltage. However, this is not performed in this work.
To accomplish these different measurements, two oscilloscopes are used with different cables and probes. First, the method for measuring DUT current is introduced.

The DUT current is measured with a resistive shunt between the DUT's source terminal and the power ground. The voltage over the shunt is then also applied over a BNC terminal, which is connected to the oscilloscope with a coaxial cable. To ensure that the signal is transferred properly to the oscilloscope the BNC, coaxial cable, and the termination in the oscilloscope all have to have the same impedance. This is obtainable as the chosen oscilloscope has a 50 Ω termination, which is the common impedance of BNC connectors and coaxial cables. The oscilloscope termination does however limit the voltage which can be applied over the shunt.

The 50 Ω termination does not allow more than 5 V continuous and 8 V pulses to be applied to it. This therefore means that the resistive shunt has to be designed such that the voltage stays sufficiently far from 5 V in the ramping, and under 8 V at transients, to ensure that the oscilloscope is not damaged.
It is decided to create a shunt using SMD resistors of the 1206 package. To reduce the inductance, it is decided that several resistors are to be placed in parallel. This also helps with the heat dissipation, however as stated previously, the DPT period is so short that the dissipation should not be an issue. It is decided that a shunt voltage of 4 V is adequate at the desired maximum current of 25 A, i.e., with the safety factor applied. The resulting required resistance is 160 mΩ, which can be approximated by applying 15 2.4 Ω resistors in parallel. Again as a safety precaution one value lower resistance of 2.2 Ω is picked, resulting in a resistance of 146 mΩ The 50 ohm resistance of the BNC terminal does not impact the equivalent resistance. With this configuration the maximum continuous current through the collective shunt is 5 A before the 1206 packages power rating of 250 mW is met, which is relevant for calibrating the gain for the conversion between the shunt voltage and the DUT current.
The gain, which is used in the conversion between the voltage measured by the oscilloscope and the current through the load, can be slightly different from the value calculated based on the advertised resistance. Thus, a calibration of the gain is appropriate. The difference in the theoretical and actual gain is caused by tolerances in the SMD resistances of 5%. The gain should be approximately 6.82 S. The method for the calibration is presented here. A known current is injected into the ground connection, through the MOSFET and thus also the shunt, and returned through the switch-node connection. The setup for the calibration is shown in Figure 4.15

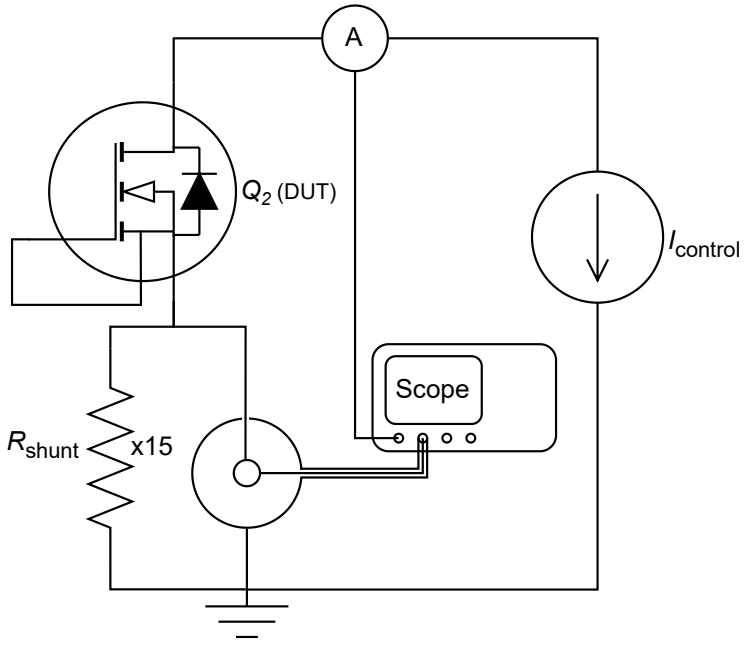


Figure 4.15 Shunt voltage to DUT current gain calibration setup.

The current source is a bench-top power supply which can supply a steady output current of up to 3.3 A. This is only 75% of the current which the created shunt is rated for, however, the resistor started to heat up at higher values due to their close proximity. First, the conventional

design is calibrated. The theoretical gain is applied with the result as seen in Appendix F in Figure F.1a, where the mean values and waveforms are different. A gain of 6.95 S results in two almost identical curves and mean values as seen in Figure F.1b.
The same procedure is performed for each of the boards, resulting in the gains seen in Table 4.4 below:

With the shunts calibrated, the next measurement introduced is for the drain-source voltage.

For measuring the drain-source voltage a LeCroy PPE4KV high-voltage probe, with a bandwidth of 400 MHz, is used. The main reason for this choice, is that this type of probe comes with an adapter to a BNC terminal. Connecting the center conductor of the BNC to the switch node and the sheath to the almost-ground potential before the shunt, allows for measuring the drain-source voltage with the probe without introducing a large inductance loop.
As the drain-source voltage is pulsed by the DC-link voltage, which is up to 700 V under the tests, the BNC terminal is near the limit of its use case. BNC terminals are rated to continuous voltages of 500 V and peak voltages up to 1500 V before dielectric breakdown occur. Thus, the BNC should be applicable for both the DPT but also for continuous SPWM as the RMS voltage of the switch node should be 230 V for grid-connected applications.

The last measurement sent to the main oscilloscope is the load current. The load current is measured with a LeCroy CP030 current probe with a bandwidth of 50 MHz rated for 30 A continuous,50 A peak. It is noted that every time the oscilloscope is turned off and on again, the probe should be degaussed and auto-zeroed to ensure proper measurements.

The measurements sent to the secondary oscilloscope is the gate-source voltages of the MOSFETs. The gate-source voltage is applied over a Micro-Miniature Coaxial Connector (MMCX) terminal and then adapted to a BNC connection, which is then measured with a fast differential probe. The reason a probe is required for the MMCX connection is that the voltage is too great for direct connection into the oscilloscope's 50 Ω termination which will match the impedance of the MMCX and the 1 MΩ can result in signal oscillations due to impedance mismatch. The used differential probes are the DP700 by Micsig with a bandwidth of 100 MHz. This probe has two voltage levels and corresponding attenuation with the first being 70 V(20X) and the second being 70 V(20X). The low-voltage attenuation setting is used here to capture the transients in the gate-source voltage as best as possible.
The setup and the different probe connections are shown in the Figure 4.16.

Table 4.4 Gains to transform the measured voltage into the current through the different shunts.

Board	Conv	Eco1	Eco2	Eco3	Eco4	Eco5	EcoSH
Gain	6.95	7	6.97	6.96	6.98	6.97	6.94

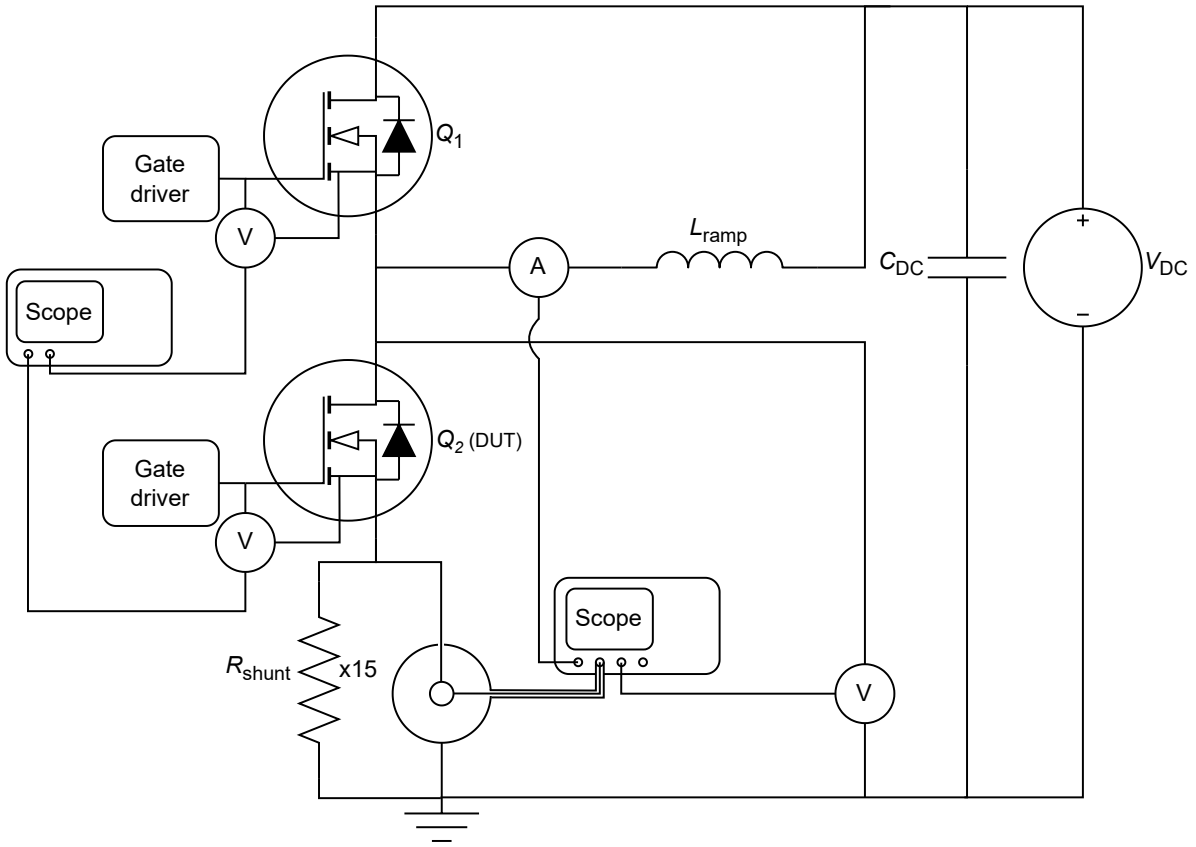


Figure 4.16 Measurement setups for the DPT.

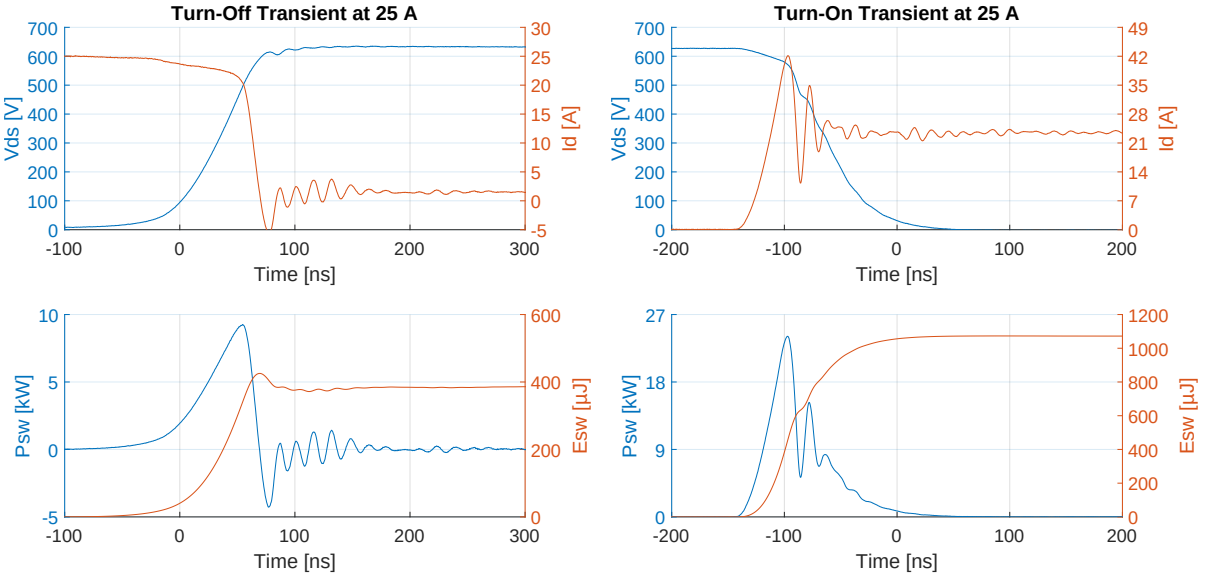
With the DPT setup and program ready the following presents the results from the performed DPTs.

4.3.3 Results

It is decided to test each board at five different current levels, 5 A to 25 A with 5 A intervals. Furthermore, an investigation into how the switching speed impacts the switching performance is conducted. The tests are first performed with a conservative gate resistance of 47 Ω, resulting in a slower switching speed. As mentioned in Section 4.2.2 regarding the gate-driving circuit the turn-off branch is implemented to enable tuning the switching events differently if this is deemed necessary for continuous operation. Thus, the tests are preliminarily performed without the turn-off branch.
First, the conventional design is installed in the setup and tested at the different currents. Figure 4.17 shows the turn-on and turn-off switching events at 25 A.

The voltage waveform during the turn-off transient can be used to estimate the difference in inductance between the boards when the waveform has the overshoot as shown in 2.4. When the overshoot is not present as in Figure 4.17a the second-order response being superimposed on the first-order response can be used. If faster switching is achieved, the first-order response should be faster and this coupled with a larger di/dt might result in the overshoot allowing analysis.

From the turn-on transient it is seen that a very large reverse-recovery current is present. The reverse-recovery of the body diode is listed to be 20 A at a test current of 20 A, a DC-link voltage



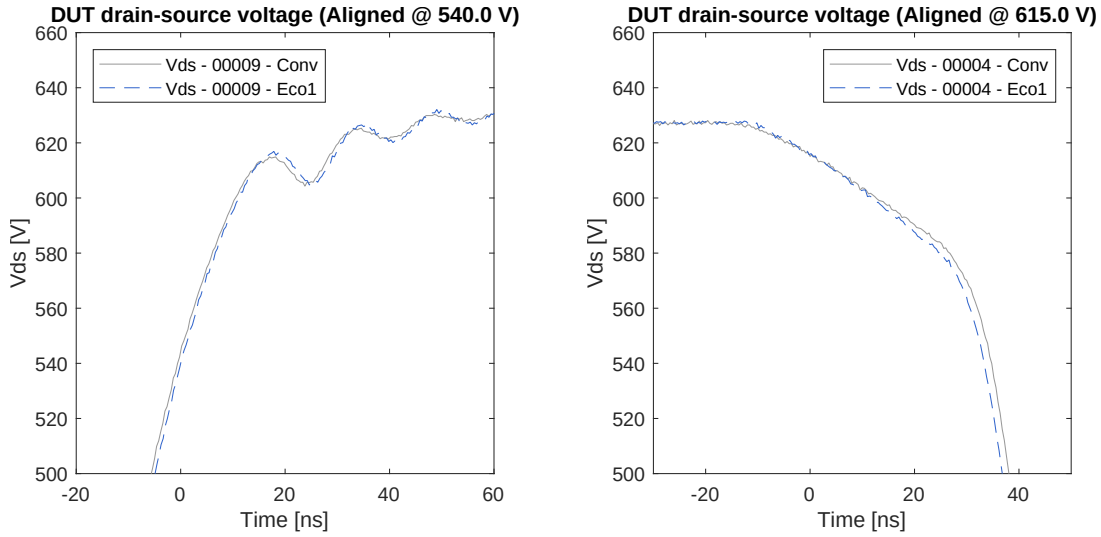
(a) **(b)**

Figure 4.17 DPT on conventional board at 25 A: a) Turn-off instance b) Turn-on instance.

of 800 V, and with a di/dt of 2000 A/µs. In Figure 4.17b, the current peaks at 42 A resulting in a reverse-recovery current of 18.5 A. The di/dt is calculated to be 917 A/µs measured from 10% to 90% of the test current. Thus the reverse-recovery current is almost at the listed at half of the di/dt and 80% of the DC-link voltage. The reason this is of interest is that if the reverse-recovery current becomes too large, the measurement of the drain current will not be possible with the used method. The maximum peak-to-peak voltage which can be measured with the shunt resistor is 8 V. The boards featuring the eco-design implementations are tested next.

The same test suite is performed for each of the eco-design boards. The DPT waveforms for all design implementations tested at 25 A, with a gate resistance of 47 Ω, are shown in Appendix A in Section A.1 for turn-off instances and Section A.2 for turn-on instances. From the eco-design implementations, the same behavior is seen as that of the conventional design. The DPT waveforms of the different eco-design implementations are very similar to the two seen in Figure 4.17. This is especially true for the voltage waveforms. A zoom-in of the waveforms of the conventional design and Eco1 is seen in Figure 4.18.

In Figure 4.18, it is seen that there is some difference between the turn-off waveforms and also in the turn-on waveforms. However, at turn off the largest difference is a few volts, whereas at turn on, it appears to be slightly larger. The issue is that the waveforms do not allow an accurate measurement of the voltage differences. As presented in Section 2.4, the turn-off voltage difference requires an overshoot from the steady-state value for a precise measurement. Similarly, at turn-on instances, a more plateau-like shape is required as it is difficult to determine when the slopes of the voltages change enough for it to be the transition to the next sub-transient. Furthermore, the di/dt is different between the two tests, making a relative comparison imprecise. Zoomed-in plots for comparisons between the conventional- and the eco-design implementations, for test currents from 15 A to 25 A, are seen in Appendix A, Section A.1 to Section A.4. The currents and the di/dts of the different boards are investigated



(a) **(b)**

Figure 4.18 Zoomed-in switching instances for the conventional design and Eco1 at 25A for: (a) Turn-off instance, (b) Turn-on instance.

in the following.

A large reverse-recovery current is present in all of the boards. However, Eco4 has the largest reverse-recovery current, which, apart from being larger, is also slower than the others, resulting in the largest turn-on loss. Furthermore, it is seen that Eco1, Eco5, and EcoSH all have a smaller reverse-recovery current than the conventional design. However, only Eco1 and Eco5 end with a smaller switching loss as EcoSH switches slightly slower. The switching speeds are investigated by looking at the di/dt. The di/dt for the different boards at all the test currents are seen in Table 4.5 below:

Table 4.5 di/dt [A/µs] of all boards at all tested currents with $R_g = 47\,\Omega$.

Current	Conv	Eco1	Eco2	Eco3	Eco4	Eco5	EcoSH
				Turn-on			
5	510	511	469	466	445	467	437
10	674	679	637	640	620	651	589
15	789	797	744	750	720	772	694
20	870	891	829	835	802	861	763
25	917	945	885	890	842	927	818
				Turn-off			
5	34.3	34.0	34.2	34.1	40.1	34.4	34.0
10	91.0	95.0	98.1	101	107	95.0	87.0
15	177	186	213	215	230	180	162
20	331	360	447	439	423	348	298
25	626	601	682	723	681	583	530

It is seen that Eco1 has a higher turn-on di/dt than the conventional design regardless of test current, whereas Eco5 is only faster at 25 A. The remaining boards are all slower at turning on than the conventional. As mentioned in Section 2.4, an increased series inductance results in faster turn-on transients. It does not appear to be the implementation of the holes that strictly dictates these behaviors. This is based on that Eco1 is faster with its 25% perforation, but Eco3

is slower with the same perforation percentage. Eco2 and Eco4, both being 50% perforated, are slower, which is partly due to a larger reverse-recovery current, which is to be expected. However, Eco5, which has the highest perforation is faster, at turn on, than both of the previous mentioned 50% perforations and faster than the conventional design at the highest current. Then, the last 50% board, being EcoSH, being the slowest of all the boards.
At turn-off the results are more nuanced. Referring to Section 2.4, a larger series inductance should slow the turn-off event. Eco1 is slower at 5 A and 25 A, but faster at 10-20 A. Eco2 is slightly slower at 5 A, but otherwise faster. Eco3 is also slower at 5 A, but at least 10% faster for the remaining currents. Eco4 is $10 - 15\%$ faster across the currents. Eco5 is slightly faster except at 25 A. EcoSH is slower than the conventional design at all tested currents.

The differences seen in the comparisons of the turn-on and turn-off instances are difficult to assign to the implementation of the perforations. The tendency described in Section 2.4 makes it appear that the conventional design has the highest series inductance at most of the current tests, when using the di/dt as the switching-speed indicator. With this in mind, variance between used components and PCBs might also be affecting the results. Here, it is important to add that as the same ramping inductor is used in all tests there should not be a variation in the inter-winding capacitance which can affect the current spike at turn-on events.

Another analysis point is the switching losses of the different boards. The switching loss are once again analyzed comparatively to the conventional design. The switching energy waveform is obtained by integrating the power loss waveform at the switching events as seen in Figure 4.17. The switching energy is then noted as the change in the energy curve. When no integration drift occur, the result is the final value of the integration waveform. However, the peak-to-peak value in the switching period can be used to minimize the error from integration drift.
First, the turn-off switching loss of the conventional board is fit to a second-order polynomial. The resulting model is used to minimize the impact of potential mismeasurements as it allows recalculation of the switching loss at a given current level in reference to the other measured values. The model is shown in the equation below:

$$P_{\text{sw,off,conv,R47}} = -0.0200 I_{\text{d}}^2 + 18.6 I_{\text{d}} - 30.0 \tag{4.2}$$

The model gives the power loss in micro joule. Next, the turn-on switching loss model for the conventional board, with a gate resistance of 47 Ω, is shown in the equation below:

$$P_{\text{sw,on,conv,R47}} = -0.0194 I_{\text{d}}^2 + 43.3 I_{\text{d}} + 55.3 \tag{4.3}$$

Similarly, the model presents the losses in micro joule. The two models can be summed to get the total switching energy at a given current:

$$P_{\text{sw,tot,conv,R47}} = -0.0394 I_{\text{d}}^2 + 62.0 I_{\text{d}} + 25.3 \tag{4.4}$$

The coefficients for the switching loss models for all the boards are shown in Table B.1 In Appendix B. For an initial switching loss comparison, the models are plotted side-by-side in Figure 4.19.

From Figure 4.19 it is seen that the DUTs in the different eco-design implementations have very comparable switching losses to the DUT of the conventional board. It is seen that the energy

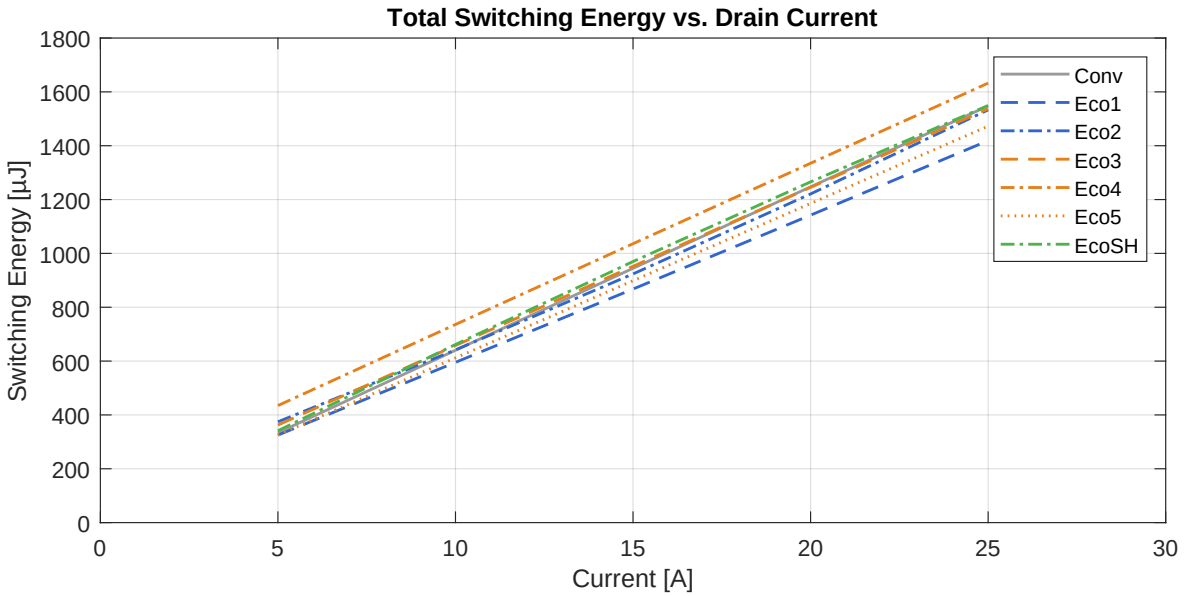


Figure 4.19 Total switching loss models for all designed boards.

curve for the conventional board is in the low-to-middle range of the curves for the most part until the higher currents, where it becomes the second largest at 25 A. The separate turn-on and turn-off energy curves are shown in Appendix B. From the separate curves, the same behavior is seen as described earlier. The conventional design's energy curve for turn off is in the lowest end of the range and at turn on it is in the middle-to-high range.
The general power loss analysis is thus not conclusive in regard to the impact of the eco-design implementation.

To investigate if the uniformity, across the test boards, is caused by a too low di/dt to introduce the voltage spike, as a response to altered parasitic, the gate resistance is approximately halved to a value of 24 Ω. In Appendix A, Section A.3 and Section A.4, the DPT waveforms are presented for all the boards tested with a gate resistance of 24 Ω. The reason a lower gate resistance is not used is that the reverse-recovery current magnitude becomes so large that a higher current will not be readable by the oscilloscope with the present shunt configuration. The reason the reverse-recovery current increases is due to same charge from the diode being discharged in a shorter period due to the increased switching speed. The switching speed is again evaluated by the looking at the di/dt of the tests. The results are presented in Table 4.6.

First, looking at the di/dt at turn on, it is seen that the conventional design is the fastest across all measurements. The same tendencies are witnessed with Eco1 switching almost as fast as the conventional design, and the remaining boards switching slower. Here, Eco4 is generally the slowest, closely followed by EcoSH.
When looking at turn-off the di/dt is again more diverse with Eco1 being slightly slower than the conventional design, Eco2 and Eco3 oscillating between being faster and slower, Eco4 being the fastest, Eco5 being slightly faster at the lower currents but then slow down relatively as the current rises, and finally EcoSH having a much faster first di/dt measurement but then slowing down.
Neither of the switching speed analysis show an impact, which can be directly tied to the implementations of the different eco-designs.

Table 4.6 di/dt [A/µs] of all boards at all tested currents with $R_g = 24\,\Omega$.

Current	Conv	Eco1	Eco2	Eco3	Eco4	Eco5	EcoSH
Turn-on							
5	889	881	817	856	742	831	786
10	1244	1215	1150	1162	1009	1141	1053
15	1405	1399	1286	1294	1162	1306	1182
20	1526	1523	1421	1435	1295	1434	1289
25	1612	1611	1514	1515	1379	1551	1383
Turn-off							
5	58.4	56.7	59.4	59.1	63.3	58.6	75.5
10	141	137	139	140	154	141	137
15	238	235	230	228	259	237	226
20	353	341	369	368	394	347	335
25	554	517	521	516	561	471	474

The average switching energy over the tested current range with the different gate resistances is investigated next. For this analysis the energies measured at all the different current levels are normalized with respect to the energy of the conventional board at the same current. This results in five normalized energies per board for the two different gate resistances. For each gate resistance the average energy per board is calculated over its tested current range. This results in two normalized average switching energies per board, one per tested gate resistance as seen in Figure 4.20.

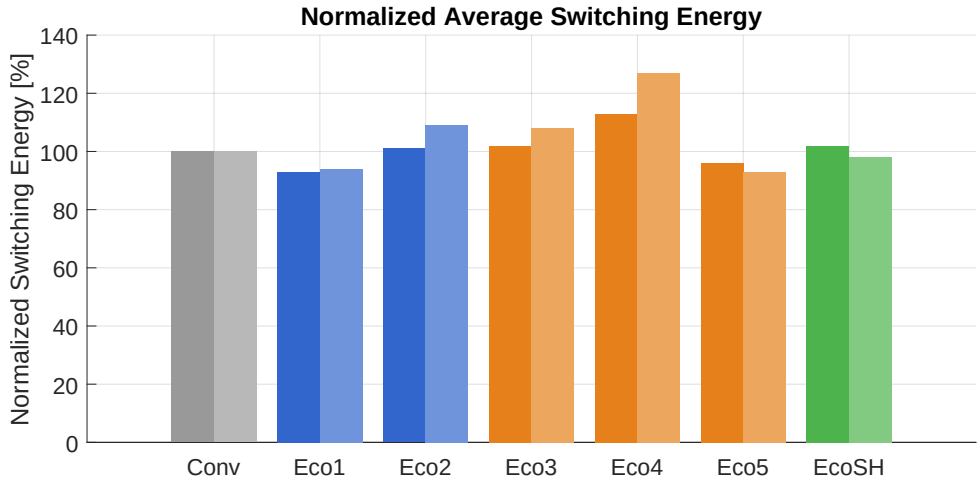


Figure 4.20 Normalized average total switching energy for each board with both tested gate resistances. $R_g = 47\,\Omega$ is the solid infill and $R_g = 24\,\Omega$ is the translucent infill. Lower percentage is better.

The main reason that the total energy is utilized for this comparison is that it automatically becomes a weighted average, compared to analyzing turn-off energies and turn-on energies independently. The reason for this is that the energies might not change with the same ratio when changing the gate resistance and thus a small relative change in the largest energy measured can be more impactful than a large change in the smaller energy measured. From Figure 4.20 it is seen that the total energy of the DUT of EcoSH drops below the 100% mark. EcoSH obtains a relatively lower total energy, with the lower gate resistance, despite that the average normalized value for the individual energies increase. The turn-off energy increases 4 pp from 107% to 111% and for the turn-on energy the increase is 1 pp from 95% to 96%. The reason this result in a

lower average normalized total energy is that the turn-off energy shifts from contributing 29% of the total energy to contributing 20% of the energy making the relatively lower energy less impactful. For Eco5 it is because the average normalized energy drops for both turn on and turn off. The average normalized energy for Eco1, Eco2, Eco3 and Eco4 increase due to the individual contributors increase more relatively to the conventional design.
From the power loss analysis the impact of the perforations are once again not directly apparent. The performance of the boards with the same perforation percentage differ substantially and Eco5 with the largest perforation is one of the best boards along with Eco1 with their DUTs both achieving lower total switching energy than the DUT in the conventional board.

In order to estimate the increased inductance of the different developed boards the method with utilizing the overshoot of first order response of the drain-source voltage is not possible as presented above. Instead the superimposed second-order response is investigated. It is assumed that the second-order response is due to a resonant circuit consisting of an inductor and a capacitor. The resonance frequency of this sub-circuit satisfies the equation below:

$$\omega L = \frac{1}{\omega C} \tag{4.5}$$

Thus, the inductance can be isolated as seen in the equation below:

$$L = \frac{1}{\omega^2 C} = \frac{1}{(2\pi f)^2 C} \tag{4.6}$$

Thus, calculation of the inductance is possible if the capacitance is known. If instead the eco-design board's inductances are normalized with that of the conventional design the equation is as seen below, with Eco1 as the example:

$$\frac{L_{\text{Eco1}}}{L_{\text{Conv}}} = \frac{\frac{1}{(2\pi f_{\text{Eco1}})^2 C_{\text{Eco1}}}}{\frac{1}{(2\pi f_{\text{Conv}})^2 C_{\text{Conv}}}} \tag{4.7}$$

Assuming that the capacitance is approximately the same between the boards, Equation (4.7) reduces to the following:

$$\frac{L_{\text{Eco1}}}{L_{\text{Conv}}} = \left(\frac{f_{\text{Conv}}}{f_{\text{Eco1}}}\right)^2 \tag{4.8}$$

Thus, with Equation (4.8) the relatively normalized inductance can be obtained. Table 4.7 below show the different frequencies of the designed boards and the corresponding normalized inductance:

Table 4.7 Normalized inductance for the different designs with the two tested gate resistances. The plots from which the frequency is read are found in Appendix C

	Conv	Eco1	Eco2	Eco3	Eco4	Eco5	EcoSH
				$R_g = 47\,\Omega$			
f	61.0 MHz	59.5 MHz	55.6 MHz	59.2 MHz	59.5 MHz	58.1 MHz	58.1 MHz
L_{norm}	1.00	1.05	1.20	1.05	1.05	1.10	1.10
				$R_g = 24\,\Omega$			
f	65.8 MHz	64.1 MHz	62.5 MHz	62.5 MHz	61.0 MHz	59.2 MHz	61.0 MHz
L_{norm}	1.00	1.05	1.11	1.11	1.16	1.22	1.16

The difference between these results and the previous power loss and switching speed analysis is that there appears to be definitive evidence that the perforations impact the inductance with the above-mentioned assumptions. Generally, the normalized inductances show that increasing the perforation increases the inductance within the same perforation type. However, the same perforation percentage shows different normalized inductances depending on the perforation type. With a gate resistance of 47 Ω, Eco1 and Eco3 have the same normalized inductance, whereas at 24 Ω there is a 6 pp difference. At 47 Ω Eco2, Eco4 and EcoSH all differ in normalized inductance with Eco4 being 15 pp and 5 pp lower in normalized inductance, respectively, and at 24 Ω Eco2 has the lowest value as Eco4 and EcoSH both have a 5 pp larger normalized inductance. The differences can be assigned to imprecision in the measurement of the period of the oscillations, but also due to smaller capacitance variations occurring at different frequencies.

4.4 Performing Mechanical Strength Tests

This section presents the results of the mechanical testing performed in this thesis to evaluate the impact of perforation patterns on the structural strength of the PCBs. As stated in Section 2.4.3, the perforations are implemented on plain, non-populated PCBs specifically prepared for three-point-bending tests. To ensure consistency, the specimens' perforations are adjusted to match the same percentage of perforation used in the half-bridge designs.

4.4.1 Performing the Three-Point-Bending Test

The test is conducted using a universal testing machine, as shown in Figure 4.21, located at the Department of Materials and Production at Aalborg University. The three-point-bending test is selected since this method concentrates stress along a single axis. This makes it effective for evaluating how localized perforations impact mechanical performance in a controlled and consistent manner. Each perforation configuration is tested on four separate specimens to provide a representative sample, resulting in a total of 28 mechanical test boards.

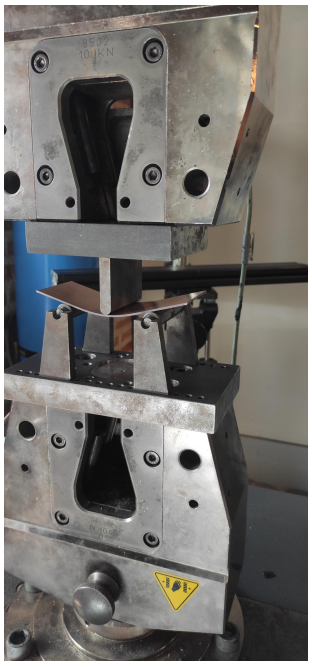


Figure 4.21 Bending test with the Zwick Z100 and one of the test specimens.

During the testing, each specimen is placed on two support rollers, and a loading roller is lowered onto the center of the board until a pre-load force of 2 N is reached. After this is completed, the applied force is gradually increased until the specimen fails. The failure criteria is that the specimens must exhibit a sudden and significant reduction in their ability to oppose the applied force at a certain deflection. This is expected due to the brittle nature of the dielectric material used for PCBs. This sudden decrease in force correlates directly to a fracture of the specimen, although it should be noted that a complete breakage is not necessary. This test method offers simplicity and reproducibility while providing valuable insight into the mechanical performance of the perforated boards under bending.
For each test, the bending force is exerted with a speed of 5 mm per minute. The same speed is applied to all test specimens to ensure consistent testing. Each cut-out configuration is produced so that four specimens are available for testing. During the test, the peak force required to induce failure in each specimen is recorded. The term fracture is used to describe the induced failure. These peak values are used to calculate the flexural strength, following Equation (2.10) introduced in Section 2.4.3.

The main objective of the mechanical test is to determine the force required to fracture the PCB, with focus on how this force, and ultimately the flexural strength σ_f, is influenced by the presence of cut-out holes and slots. It is expected that the introduced perforations will reduce the breaking force.

This forms the basis for the mechanical success criteria of the bending test. It is expected that the measured flexural strength of the unperforated specimen is close to the one known value for FR-4, introduced in Section 2.4, since this is a commonly utilized dielectric for PCBs.

For this thesis, the flexural strength results are normalized relative to the flexural strength of a non-perforated reference board. This normalization ensures that the results are independent of the absolute specimen size, allowing for comparisons across different perforation configurations.

4.4.2 Results from the Bending test

The maximum bending moment is derived from the measured maximum force, along with the known specimen dimensions and the distance between the support rollers. From this, the average force-deflection curve is obtained, and the behavior for each group is shown in Figure 4.22, which depicts the mechanical response before fracture.

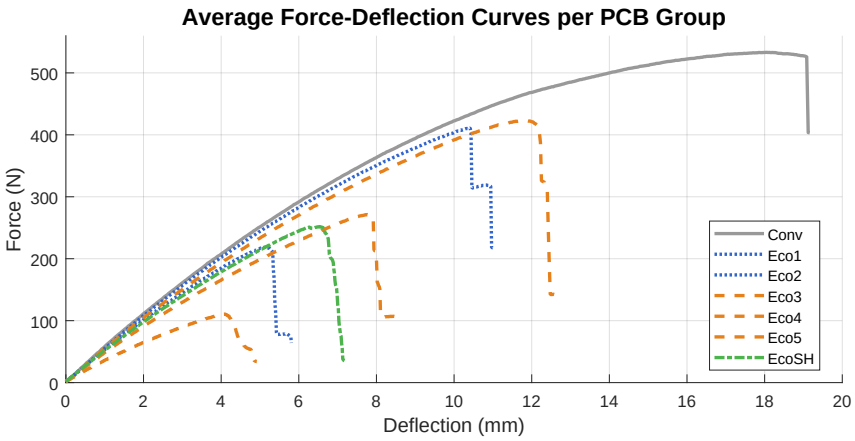


Figure 4.22 Average force-deflection curve for each perforation group.

Figure 4.22 illustrates the average force applied to the breakage line of the specimen during three-point bending. The sudden drop in applied force in each curve marks the point of fracture, which indicates a brittle nature of the material. The exhibited curves have been calculated as the mean of each specimen group, respectively. It is observed that for certain specimens, the fracture did not occur due to the application of a maximum force, but rather a prolonged exertion of force. Cracking sounds indicated the onset of the fracture, with force remaining around a certain value, while the top roller increased the boards' deflection. Furthermore, it is seen in Figure 4.23 that not all specimens broke evenly at the intended breakage line.

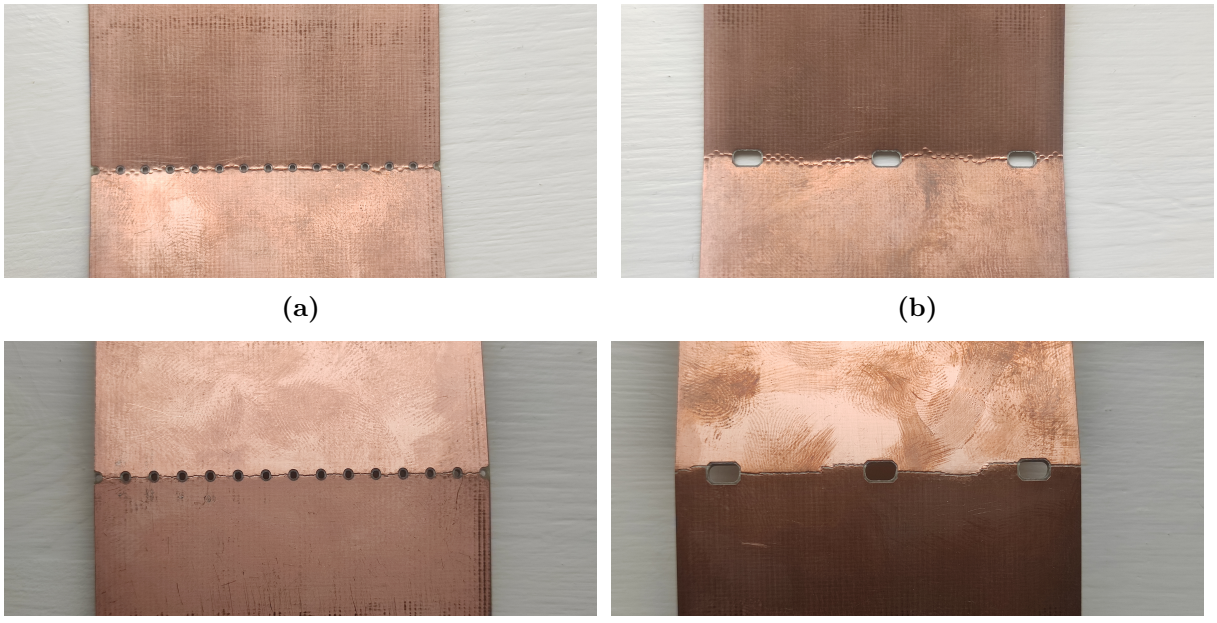


Figure 4.23 Top and bottom side of the specimen "Eco1" and "Eco3" after the three-point-bending test.

Here, Figure 4.23 shows the breakage line after the applied three-point-bending test. The remaining specimens are depicted in Appendix D Section G. It is evident that the hole-based approach yielded a cleaner breakage line in the 25% and 50% perforation configurations. In contrast, the slot-based design resulted in a breakage line that exhibited a more jagged breakage, especially for the specimen with the lowest perforation percentage.

It is calculated that the non-perforated specimens' flexural strength is close to the anticipated one of FR-4. With an average measured flexural strength of 411.1 MPa, the result aligns well with the value of approximately 413 MPa from [39], thereby validating both the test setup and the mechanical behavior of the test specimens. The obtained values are presented in Table 4.8 below:

Table 4.8 Obtained averages for each configuration group.

Specimen	Perforation [%]	Max. Breaking Force in [N]	σ_f in [MPa]	$\sigma_{f,norm}$
Solid	0	534.7	411.1	1
Holes	25	417.9	321.4	0.78
Holes	50	222.2	170.8	0.41
Slots	23	430.2	330.8	0.80
Slots	53	278.7	214.3	0.52
Slots	76	112.8	86.76	0.21
Holes + Slots	50	256.8	197.5	0.48

The normalized flexural strength represented in a bar chart is found in Appendix D in Figure D.1. The test results show that slot-based perforations require a higher breaking force than hole-based perforations at similar perforation percentages. While the perforation percentages for the two sets differ slightly, with 25% for the hole-based design and 23% for the slot-based design, the difference in flexural normalized strength 2 pp. The 50% hole-based design and 53% slot-based design show a bigger difference with a difference of 11 pp, as shown in Table 4.9.

Table 4.9 Deviation in force, calculated as the difference between the slot-based approach and the hole-based approach.

Compared Implementation	Force Difference [N]
25% holes - 23% slots	12.3
50% holes - 53% slots	56.5

It is noted that not all boards originated from the same fabrication batch. This is evident in some test groups, where one of the four specimens displayed a noticeably higher or lower flexural strength compared to the other, which is seen in Appendix D. As seen from Figure D.5, one specimen in the 25 % slot-perforation group required a force of 477 N to break, whereas the rest of the group broke at an average applied force of 414 N. This is, however, the highest observed deviation as shown in Table D.1, which is found in Appendix D.

Another trend is observed for both perforation types. As the perforation percentage increased, the deviation from the average required breaking force decreased. This have to be analyzed further to investigate if this trend is a result of the specimen's origin or due to the perforation geometry itself. Table 4.8 shows that slot perforations result in higher flexural strength of the PCBs than the hole perforations at similar perforation percentages. This difference becomes especially notable for the perforation percentage of 53 % and can be attributed to the remaining material between the slots. As more material is retained between two perforations, the applied force can spread more evenly between them. In contrast, boards with circular holes introduce more frequent geometric discontinuities. These discontinuities act as stress concentrators, where the local stress at the holes' edges can reach up to three times the amount of the applied stress [57].

Moreover, it is observed that the combination of cut-out holes and slots yields a compromise in terms of the required force until breakage occurs. The combination layout exhibits higher flexural strength than the hole implementation, but remains slightly mechanically weaker than the slot-based configuration, even at similar perforation percentages. This suggests that while the inclusion of slots helps preserve structural integrity, the added holes introduce local stress concentrations that reduce the overall mechanical rigidity.

Overall, the findings from the conducted test indicate that the eco-designs can yield a promising trade-off between mechanical rigidity during the PECs' lifetime and efficient and simplified disassembly at the EoL. This suggests that if a clean breakage is intended, then the cut-out hole approach yields better results, but if mechanical rigidity is of priority, then the slot-based approach can be considered.

4.5 Combined Performance Test Results

This section combines the obtained results from the electrical and mechanical tests. Furthermore, it aims to create a metric that can be used to evaluate the overall performance of the proposed design approach in regard to mechanical and electrical results. Therefore, Table 4.10 presents all the relevant information.

Table 4.10 Summary table for the electrical and mechanical tests.

Board	Perforation [%]	E_{norm} [%]	L_{norm}	$\sigma_{\text{f,norm}}$ [%]
		$R_{\text{g}} = 47\,\Omega$		
Conv	0	100	100	100
Eco1	25	93	105	78
Eco2	50	101	120	41
Eco3	23	102	105	80
Eco4	53	113	105	52
Eco5	76	96	110	21
EcoSH	50	102	110	48
		$R_{\text{g}} = 24\,\Omega$		
Conv	0	100	100	100
Eco1	25	94	105	78
Eco2	50	109	111	41
Eco3	23	108	111	80
Eco4	53	127	116	52
Eco5	76	93	122	21
EcoSH	50	98	116	48

The takeaway from Table 4.10 is that the inductance increases when introducing the perforations and the flexural strength decreases. Both of these outcomes are expected. The change in switching energy can however not be directly attributed to the introduction of the perforations, but appears to be more component dependent. This is seen when looking at the normalized inductance is largest the normalized energies are closer to that of the conventional design. This is seen at Eco2 at a gate resistance of $47\,\Omega$ and Eco5 with a gate resistance of $24\,\Omega$.

5 Discussion

This chapter discusses the obtained results of this thesis and the validity of the applied solutions, given the assumptions made in order to obtain the results. The discussion first includes a detailed examination of the MOO algorithm, and afterwards the PCB designs are reflected upon. Then, the designs of the PCBs are discussed as well as the results of the DPTs and the mechanical tests.

5.1 Multi-Objective Optimization Algorithm

Only the metals occurring in the MOSFETs, filter cores and filter windings are investigated in this project. However, more metals might occur in the logic voltage-level components. Furthermore, most of the used components have some kind of plastic housing. Thus, leaving out the plastics from the larger components and the smaller components entirely will make the recycling rate appear better than it is in reality. However, as the smaller components are constant between the different designs in this work, the recycling rate is treated as a relative metric between combinations. The omission of plastic does have an impact, but it is deemed that the omission does not impact the results in a large degree. Most of the components encapsulated in plastics utilize similar amounts of plastic as they often have similar proportions, making the relative comparison remain appropriate. Furthermore, as the the plastic is mostly a sheath around the larger components they contribute a very small percentage of the total volume.

Another omission is in regard to the film capacitors and their recyclability. As the film capacitors are able to vary depending on the frequency, so will the amount of metal and especially plastic, which a chosen capacitor contributes. Therefore, if the plastic recyclability is included in the recyclability parameter, the changing film capacitors can have a large impact on the recycling rate of the system. Once again, the omission is not suspected to skew the results much, as it is mainly the large metal-rich components, such as the filter cores, filter windings and heatsinks, which change the recycling rate due to the generally larger mass.

In the MOO algorithm, the power loss of the capacitors is disregarded. However, as the switching frequency impacts the ripple current in the DC link this nuance in the power loss is not captured. Furthermore, as the film capacitors vary the different capacitors' ESR might have an impact on the final efficiency. The impact of omitting this in the power loss model can shift the different objectives and other optimal points might occur instead. It is however deemed unlikely that this omission skews the results in such a degree that the obtained data is invalid. This is based on that less power generally flows through the capacitors than the remaining large components. However, it is prudent to include a power loss model for all capacitors, considering that the ESR is frequency dependent.

5.2 PCB Design

It is assumed that perforation is an appropriate way to minimize the force required for dismantling, but also that it acts as a guideline for recyclers. It is seen that the perforations act as guides for the breaking itself, but it is also noted that visibly they sectionalize the PCB. It is thus justified that these perforations are superior to silk-screened area-separation as the dismantling can be performed more controlled and reduces the necessity of having to use rotary cutters, which exposes the workers to unhealthy particles when the glass fiber is cut. Thus, the assumption that the dismantling is simplified is justified.

Regarding the gate-driving circuit, it is assumed that the routing, the component selection, the assembly of the components, and the operability of the MOSFETs is adequate. This is seen as both MOSFETs could be switched as desired, as well as the use of either MOSFET as the DUT for DPTs. This implies that the bootstrap circuit for the high-side MOSFET holds the voltage sufficiently long enough for operation. Therefore, the assumption is justified.

In the PCBs design, it is assumed that the connection between the power ground and the logic ground is acceptable. It is seen that, when the ground planes are not connected, the low-side switch's gate-source voltage is not high enough for turn-on. The reason for this is that the two ground planes float too much in relation to each other, despite the capacitor connecting both planes. Thus, the planes have to be connected as the gate-driver circuit does not use an isolated power supply directly. This could have been circumvented by having the DC/DC converter placed such that it uses the Kelvin-source of the low-side as the reference. This results in fewer components for the half-bridge converter, but will require a 18 V DC/DC converter for each phase for the VSI.

For the MOSFETs, it is assumed that the use of a negative gate voltage is not required. The reason for this assumption is, that a negative voltage decreases the risk of false turn on. In this thesis, a Miller clamp is used for the half-bridge converter, as this achieves the same outcome as the negative gate voltage, by pulling the gate voltage below the threshold voltage. However, it is seen that the gate-source voltage during the DPTs exceeded the threshold value, and thus a combination of a negative gate voltage and the Miller clamp is recommended.

5.3 Electrical Results

In the used power loss model, the conduction losses are calculated based on the on-state resistance from drain to source, also known as conduction in the first quadrant (Q1). When the output current is positive, the low-side switch is conducting in the third quadrant (Q3). Then, when the output current is negative, the high-side switch is conducting in Q3 and the low-side switch in Q1. Based on this, the power losses are imprecise if there is a large difference in the on-state resistance between the two quadrants. To investigate this possible difference, the datasheet of the used MOSFET, SCTWA40N12G24AG by STMicroelectronics, is referenced. Looking at the conduction in Q1 and Q3 at the same temperature, it is seen that there is only a very small difference when comparing the similar gate voltages. Furthermore, the larger the current the lower the voltage over the channel is for Q3 compared to Q1. This results in a slightly

more conservative power loss model. Using the on-state resistance of Q3, when appropriate, will however, still increase the accuracy.

In the estimation of the different eco-design implementations' inductances it is assumed that the capacitance is approximately equal between the different boards. The reasoning for this assumption, that the introduction of perforations affect the inductance more than the capacitance of the board, is based on the cross sections affected. The capacitance of the board is dependent on the area of the plates or island, being parallel to each other, on either side of the board and the inductance is dependent on the cross section of the conductor. Thus, the introduction of a perforation line does not impact the total area of the plates much, but it does cut the cross section of the conductor and thus the inductance have to vary more than the capacitance.

5.4 Mechanical Results

While the mechanical test setup is suitable for comparative analysis, it does not fully capture the complete loading conditions encountered in the real world. For example, multi-dimensional or sheer forces, repeated flexing, extended periods of vibrations, edge loading or drop impacts may occur during handling, transportation and installation.

With the mechanical boards being designed solely for the three-point bending test, it is assumed that the flexural strength values translate to the half-bridge configuration with components soldered onto it. As the flexural strength is a metric which is easily translatable between dimensions, the different shapes of the PCBs are not impacting the results. Furthermore, as long as no components or solder are placed over or in the break-guiding line, no difference is expected.

In addition, it is observed during the mechanical testing that the PCB s' flexural strength varied. This variation is further seen to originate from the fabrication sheets, where the specimen depicted a color variation in the fiberglass from the rest of the group whenever a significant difference in flexural strength is measured. This difference is evident as the colors varied from subtle green to translucent green. As the measured forces and thus the averaged flexural strengths are normalized, this will have a smaller impact if the sample size of the mechanical boards is greater.

It is assumed that the fiberglass is the main contributor of the flexural strength, and thus the difference in traces on the actual PCBs and the full copper on the test specimens will result in almost the same flexural strength. This is justified as the copper layer is only 18 µm and thus the fiber glass is the main contributor to the height as the total height 1.6 mm and thus also to the strength of the board. Furthermore, the witnessed fracture response is very brittle which is expected for the glass fiber as a composite material. As copper is a ductile material, the response is different if it is the main strength contributor. Thus, the flexural strength is translatable between the test specimens and the similarly perforated electrical test boards.

6 Conclusion

The developed MOO algorithm is used to investigate the impact of introducing recyclability as a design parameter. A Pareto point analysis shows that the optimal points vary between an efficiency of 99% to 98.2%, a power density of 15.5 kW/L to 7.13 kW/L, and a recyclability between 82.3% and 57.8%. It is noted that these numbers only account for the analyzed part of a full system. With these objectives in mind, it is seen that the efficiency is generally very high, the power density varies substantially and is mainly reduced when the efficiency is highest, and the recyclability mirror the trends of the power density quite well. A normalized objective maximization analysis show that the large variation values in power density and recyclability, results in these parameter being prioritized in most of the objective maximization solutions. The chosen combination for additional investigation in the rest of the case study is the most frequently occurring point in the objective maximization analysis. This combination results in an efficiency of 98.2%, a power density of 15.5 kW/L, and a recyclability of 82.3%. It is noted that in all of the maximization solutions, which only consider efficiency and power density, the efficiency does not surpass 98.4%, so it is not the introduction of recyclability alone, which result in the lowest possible efficiency.

A benchmark design is developed with a conventional design approach. Six different eco-design implementations are designed to facilitate dismantling at EoL. The designs use different perforation lines in the PCB to enable guidance and easier separation of components with different compositions. Two eco-designs using smaller holes, one with 25% perforation and one with 50% perforation, are designed with the same layout as the conventional design. Three eco-designs using elongated holes, one with 25% perforation, one with 50% perforation, and one with 75% perforation, are designed. The last eco-design is a combination of the two different perforation types and has a 50% perforation.
These different eco-design implementations are tested by conducting two distinct test types. The first is a three-point bending test on unpopulated PCBs, as the mechanical test, and the second is a set of DPTs on the developed half-bridge converters, as the electrical test. From the DPT it is obtained that the eco-design implementations impact the inductance of the PCB. The reduction of copper on the PCBs does increase the inductance of the boards, but this increase does not have a significant impact on the switching energies. Moreover, the mechanical test showed that implementing cut-outs reduces the PCBs flexural strength, making it more prone to fracture under applied force, almost linearly. Thus, these findings suggest that the implementation of the proposed eco-design method enables an easier dismantling and sorting at EoL without harming the efficiency of the PEC.

The case study of this thesis revolves around half-bridge converters, as this configuration is one of the most commonly used topologies. The core of this work focuses on the implementation of the proposed eco-design and its impact on the electrical and mechanical performance. From the half-bridge converters and the different tests, it is seen that the eco-design does not impact the performance to a significant extent. It is further seen that the components' own inconsistency

and deviation from the manufacturers' given values affected the performance to a greater extent than the eco-design implementation.

This thesis investigates how PECs can be designed for dismantling at EoL without harming the performance, but also how the different objectives are impacted when recyclability is introduced as a design parameter. Based on the previously stated sub-conclusions, it is deduced that recyclability can be incorporated into the design procedure of PECs as an objective similar to efficiency or power density. It is shown that the recyclability and material minimization in the form of achieving high power density is interconnected. Furthermore, the proposed categorization based on component type and the incorporation of perforation areas in the PEC design facilitate more efficient recycling processes. This approach is not only considered prudent but also imperative to implement in order to combat the growing e-waste problem.

7 Future Work

7.1 Combating Large Reverse Recovery Currents

One of the limiting factors in the performed DPTs in this work is the large reverse-recovery charge of the fast and not very soft body diode of the utilized switch. If a switch with a softer reverse recovery or a smaller reverse-recovery charge is used, the impact of the perforations on the inductances might be more apparent. Furthermore, faster switching is enabled, which will push the di/dt further, resulting in a clearer voltage overshoot. Another solution to the large reverse recovery can be the implementation of an anti-parallel Schottky diode [58]. A SiC Schottky diode can be used to carry most of the charge in the freewheeling period. As the Schottky diode is a majority-carrier device, the current commutation to this device is fast. However, even if current is initially commutating to the non-DUT body diode, it can quickly be handed over to the Schottky diode after the initial transient, until the voltage across the two diodes is even. This will result in most of the current freewheeling in the Schottky diode and then at the turn-on event of the DUT, the reverse-recovery current is limited.

7.2 Reliability and Lifetime Impacts from Perforations

Not all performance metrics of a PEC are considered in this work. Reliability aspects of the proposed eco-design should be investigated before implementing them in a final product. Specifically, vibration tests should be performed to see how the introduced stress concentrations will respond to the induced stress and how large an impact this has on the PCB's lifetime. Another lifetime aspect of the PCB is in regard to delamination of the copper layers. As the perforations also increase the resistance around the perforations, these locations are more prone to higher temperatures. The increased temperature will act as increased thermal cycling of the areas close to the stress concentrations, but also of the copper traces, which might result in the PCB being more prone to delamination, resulting in EoL.

7.3 Introducing Vertical Lines

Repurposing of components is not investigated in this project. However, it is one of the benefits of including the perforations. Furthermore, including vertical perforations in the layout, used in this work, can enable easier desoldering of e.g. film capacitors when the other components on the board are the reasons for EoL. First, breaking the horizontal line and then a vertical line very close to the film capacitor will enable it to be on its own small piece of PCB with a smaller thermal capacity. With the smaller thermal capacity, it can then be sent to another station for desoldering and quality testing, preferably both automated processes. It is therefore recommended that investigations are performed into analysis of perforations in two dimensions and how the smaller PCB pieces impact the ease of desoldering.

7.4 Shear Stress Analysis and Actual Dismantling Tests

Considering that bending or snapping the PCBs is not always a feasible solution, further investigations should analyze the impact of other force applications, such as shear forces, and how perforations affect the ease of disassembly. Shear forces occur when the blades of, for example, a side-cutter is cutting the PCB. The introduced force along the blade's edges causes the material to deform until it eventually breaks. Thus, it is recommended to investigate the impact of shear forces in regards to perforation percentages and types and how this translates to easier disassembly of PECs.

Implementing the proposed eco-design approach into PECs needs to be sufficiently tested before such methods are applied to PECs, especially regarding how recyclers are actually dismantling PECs. Therefore, future testing of eco-design approaches should be conducted in similar ways, which replicate how recycling facilities treat e-waste in order to ensure that the design enables disassembly. Furthermore, other metrics such as the tool accessibility, disassembly time, or the sorting quality can influence the overall recycling yield and are thus to be analyzed as well.

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A DPT Switching Instances

A.1 Turn-Off DPT Instances with $Rg = 47\,\Omega$

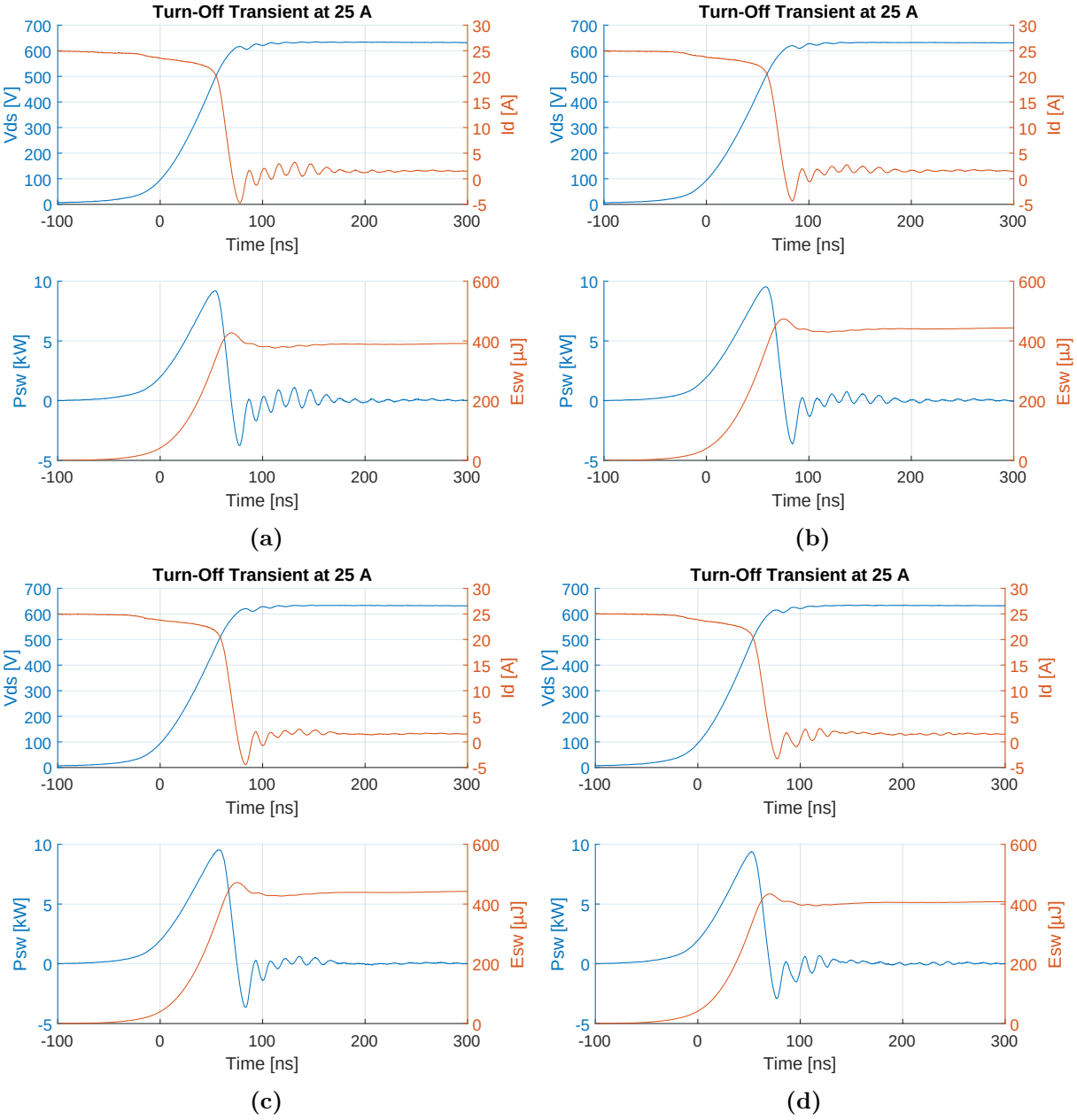


Figure A.1 Turn-off instances at 25 A for board: (a) Eco1 (b) Eco2 (c) Eco3 (d) Eco4.

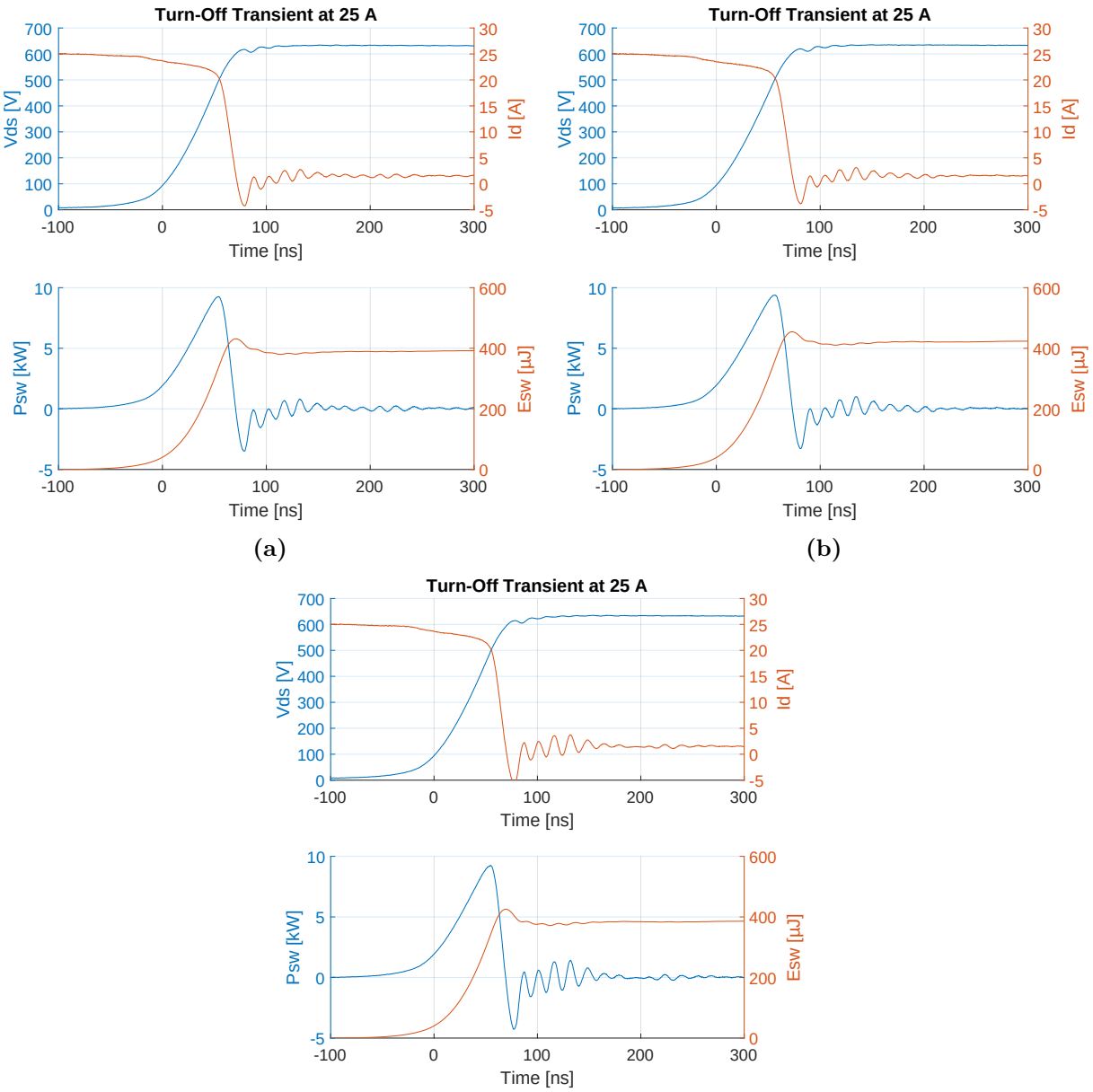


Figure A.2 Turn-off instances at 25 A for board: (a) Eco5 (b) EcoSH (c) Conv.

A.2 Turn-On DPT Instances with $Rg = 47\,\Omega$

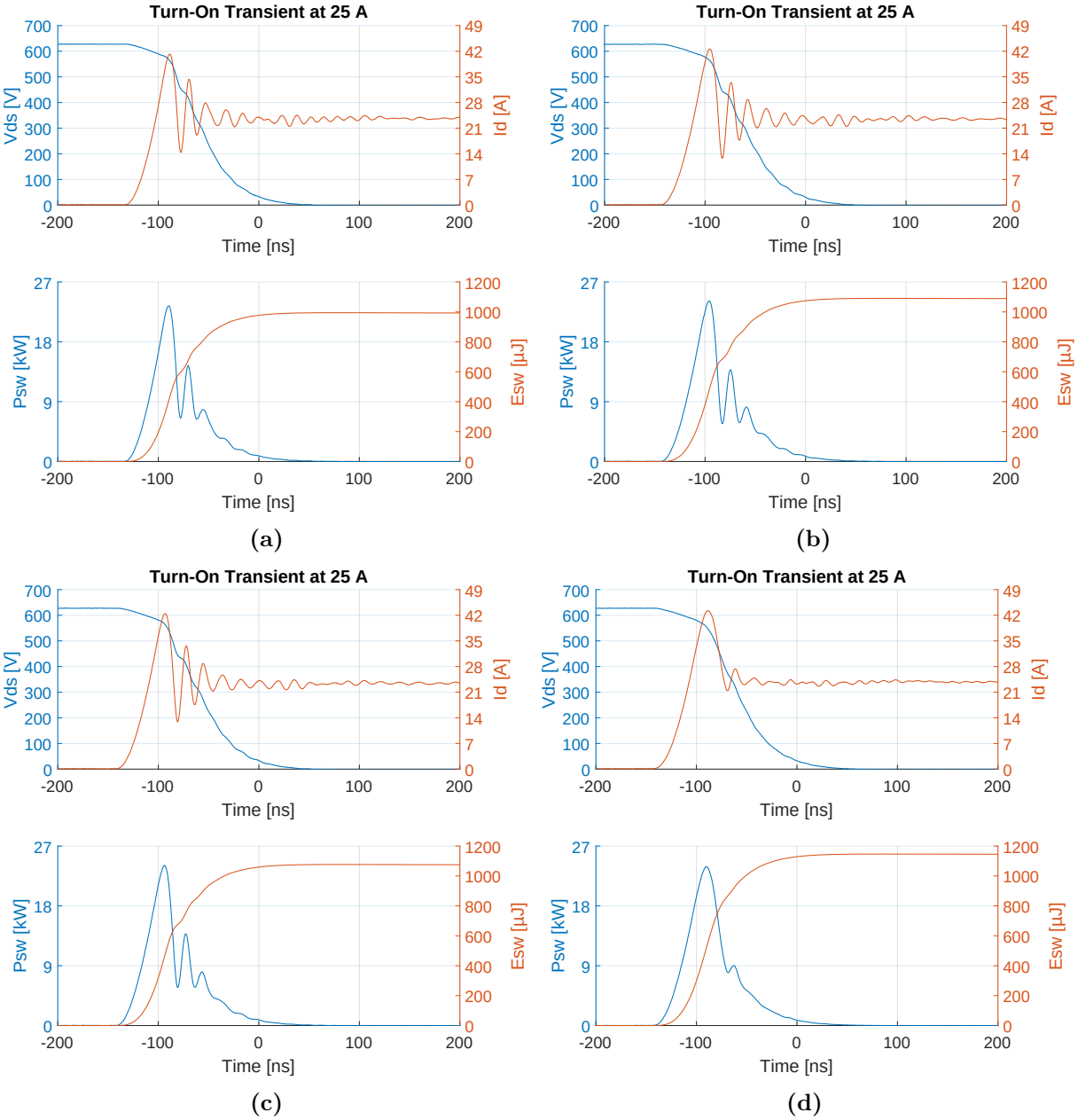


Figure A.3 Turn-on instances at 25 A for board: (a) Eco1 (b) Eco2 (c) Eco3 (d) Eco4.

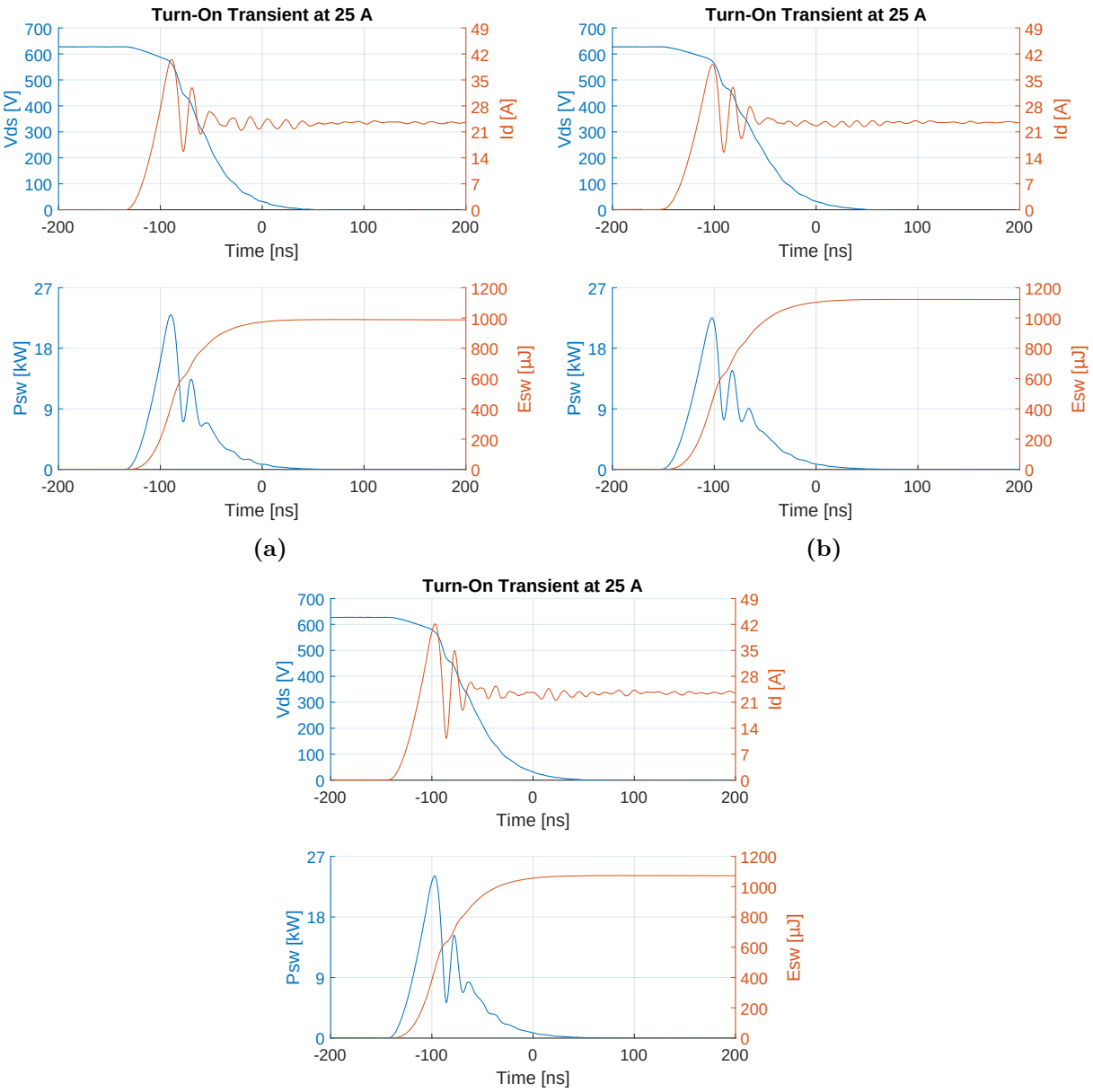


Figure A.4 Turn-on instances at 25 A for board: (a) Eco5 (b) EcoSH (c) Conv.

A.3 Turn-Off DPT Instances with $Rg = 24\,\Omega$

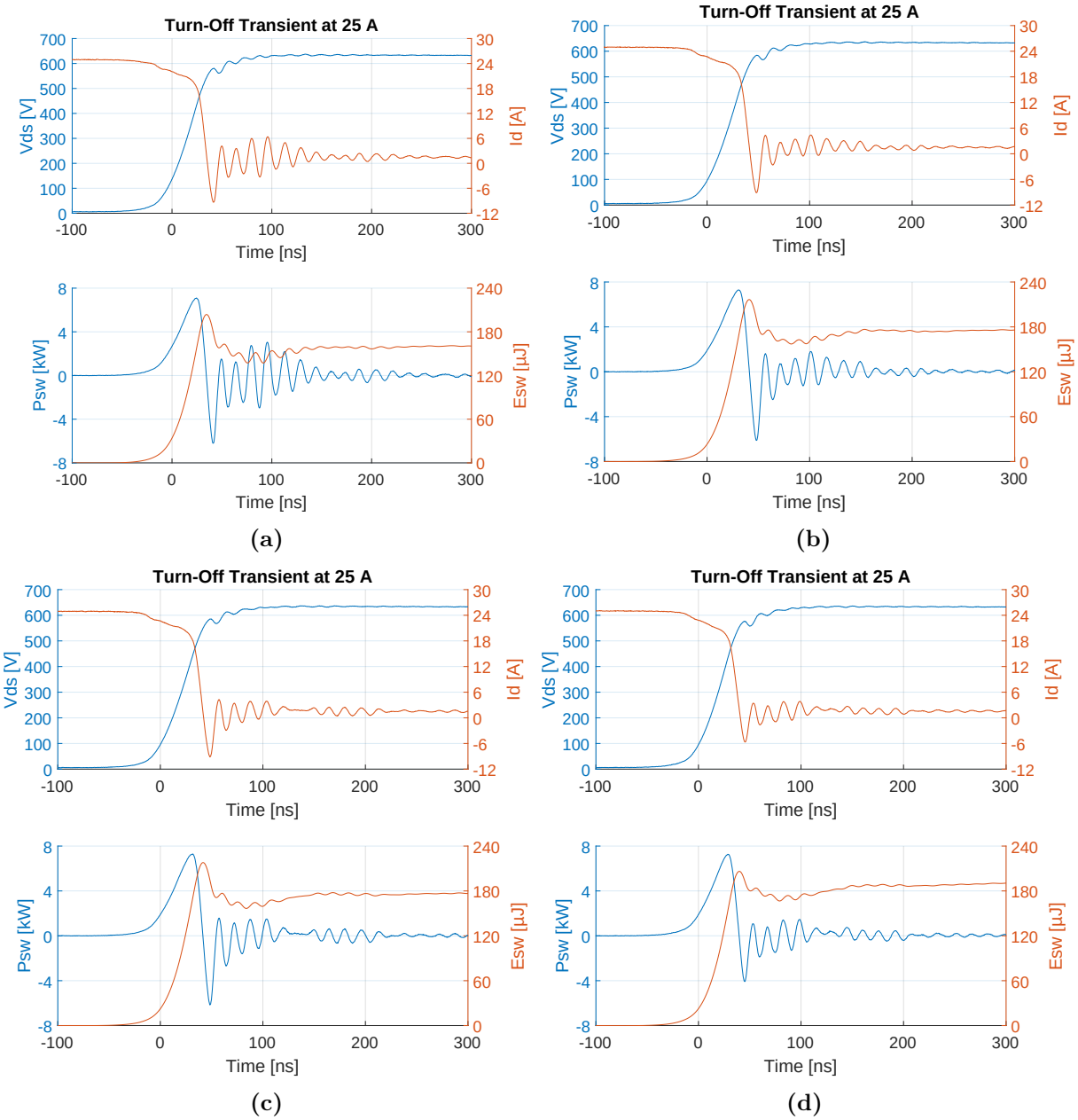


Figure A.5 Turn-off instances at 25 A for board: (a) Eco1 (b) Eco2 (c) Eco3 (d) Eco4.

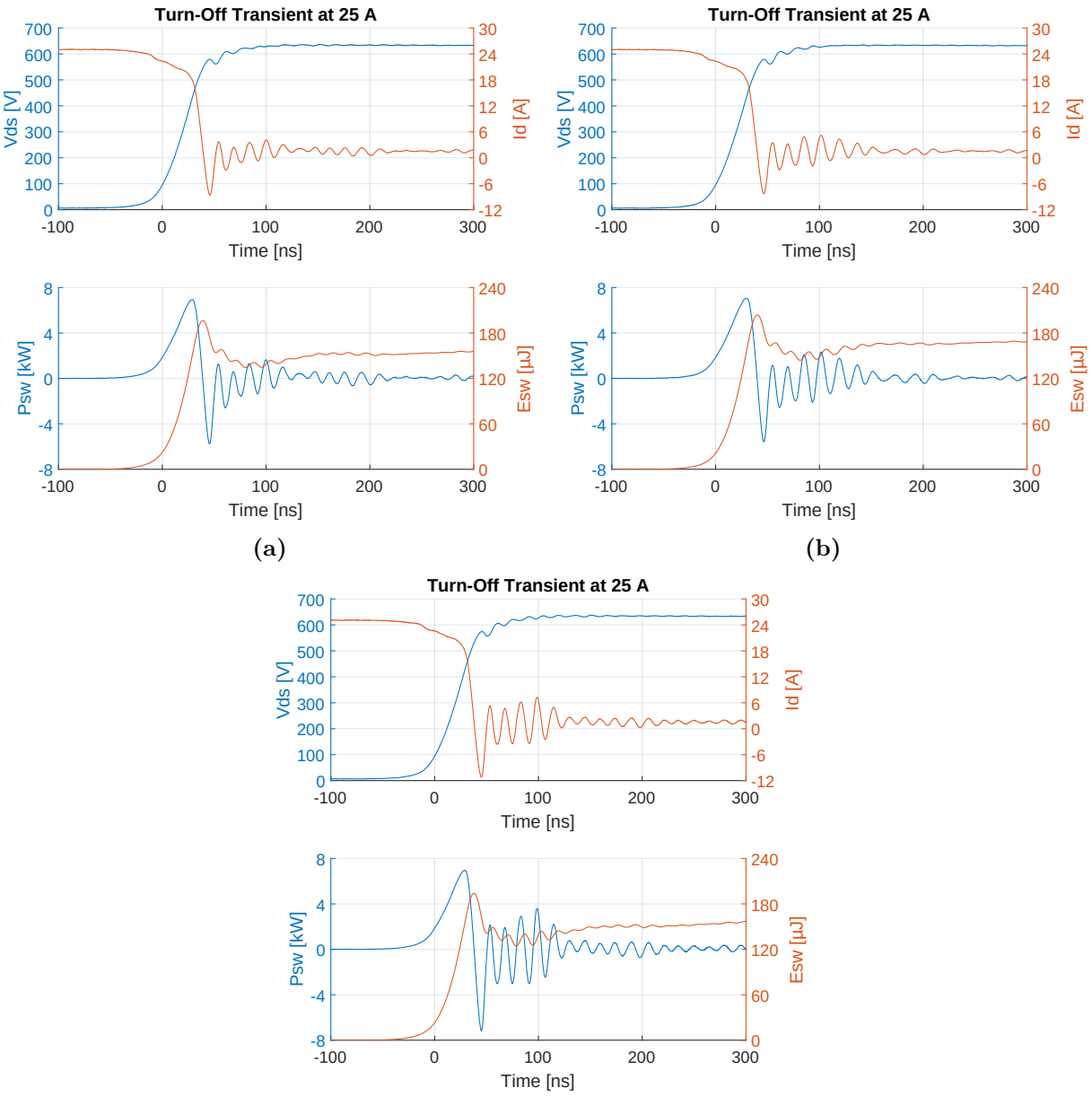


Figure A.6 Turn-off instances at 25 A for board: (a) Eco5 (b) EcoSH (c) Conv.

A.4 Turn-On DPT Instances with $Rg = 24\,\Omega$

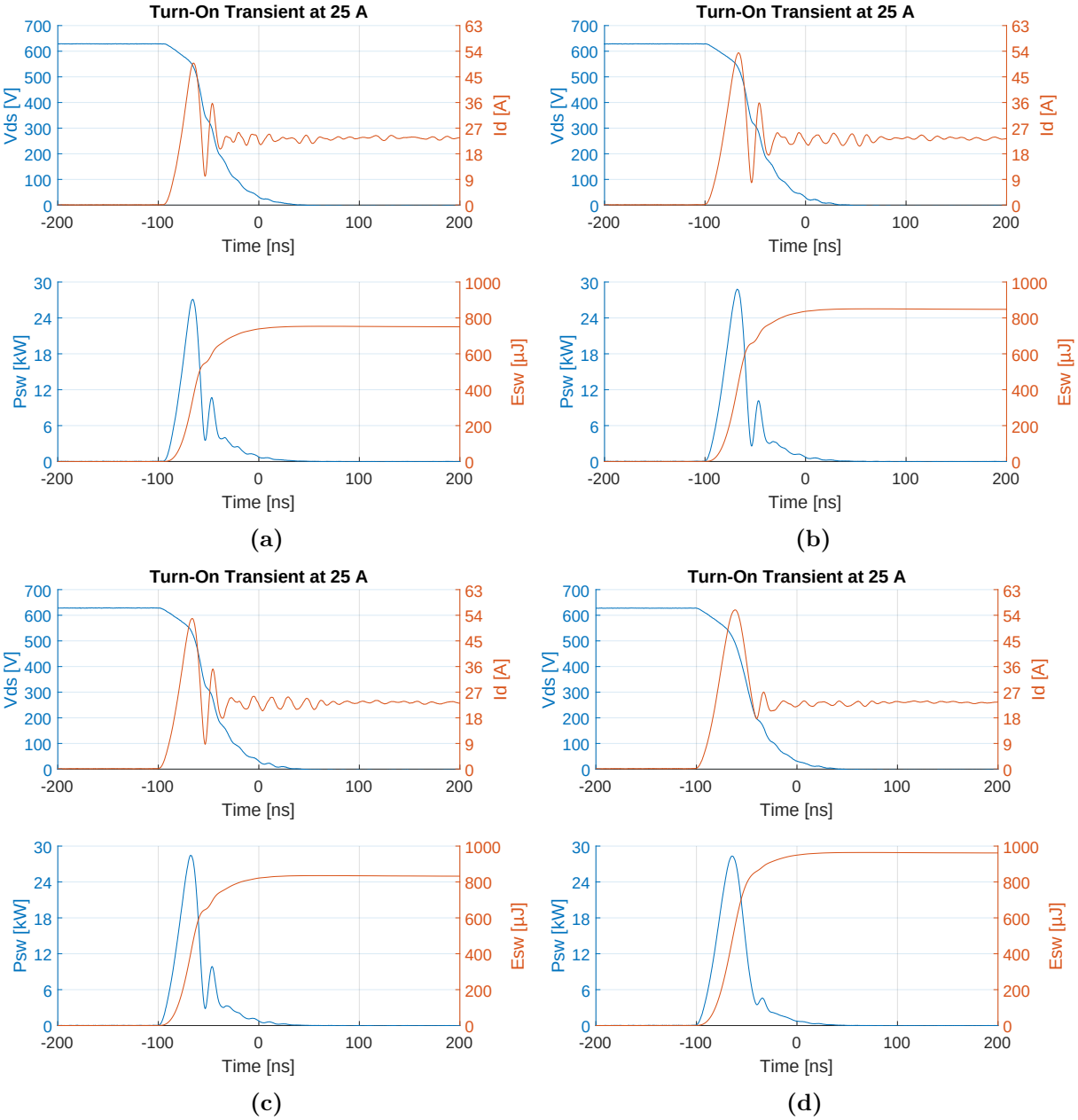


Figure A.7 Turn-on instances at 25 A for board: (a) Eco1 (b) Eco2 (c) Eco3 (d) Eco4.

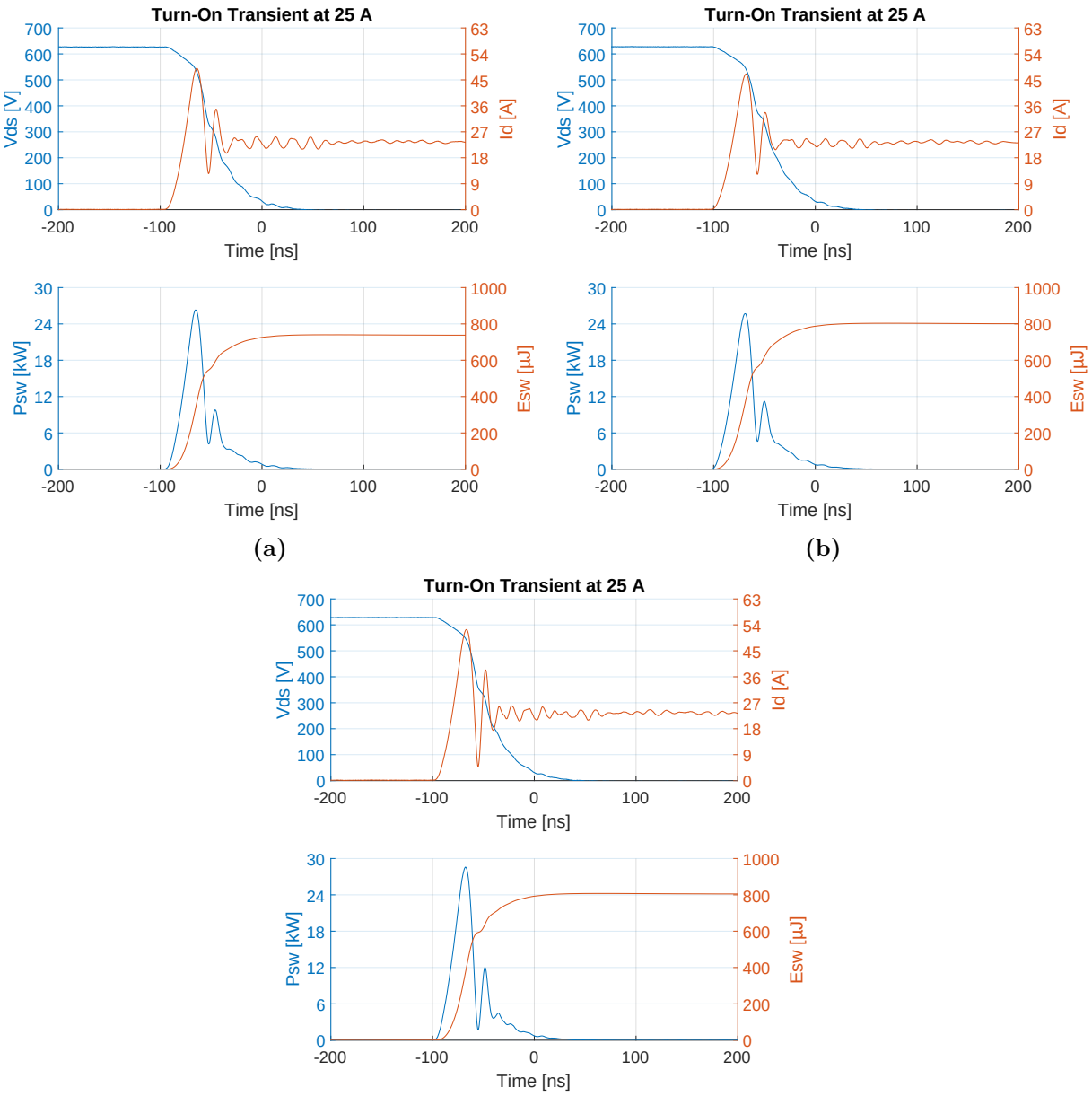
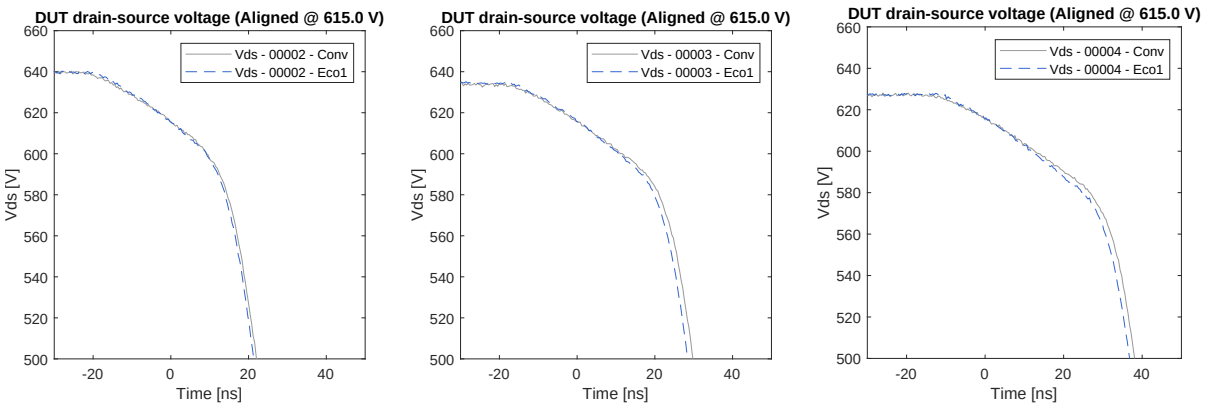


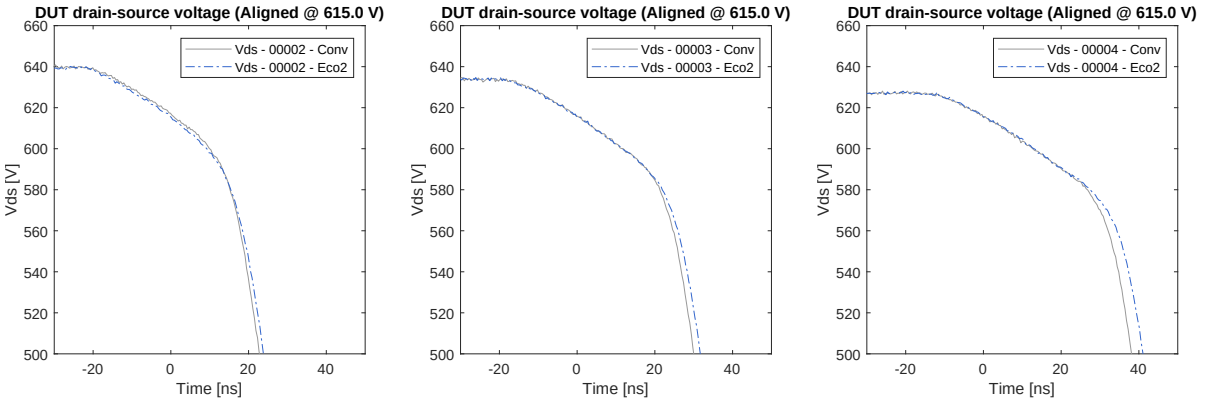
Figure A.8 Turn-on instances at 25 A for board: (a) Eco5, (b) EcoSH, (c) Conv.

A.5 Zoomed in Turn-On DPT Instances with $R_g = 47\,\Omega$



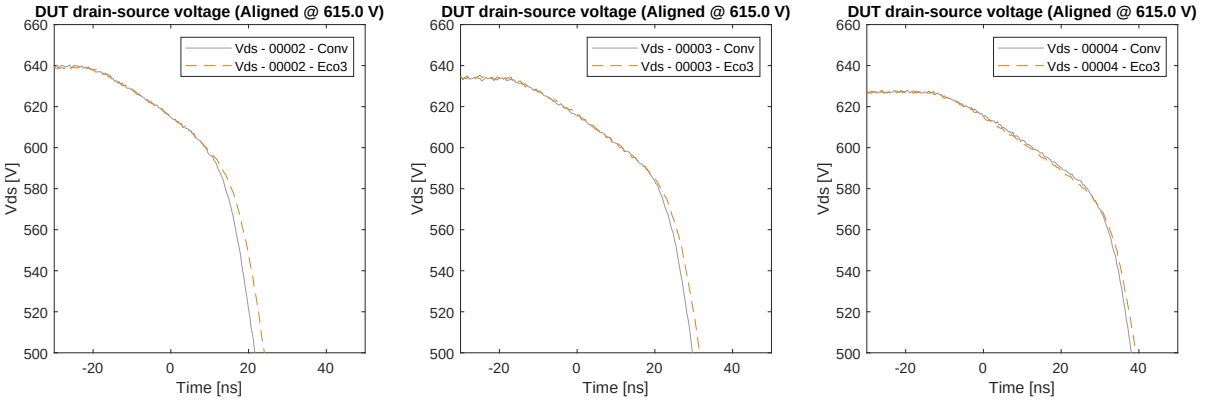
(a) **(b)** **(c)**

Figure A.9 Turn-on instances for Conv and Eco1 at: (a) 15 A, (b) 20 A, (c) 25 A.



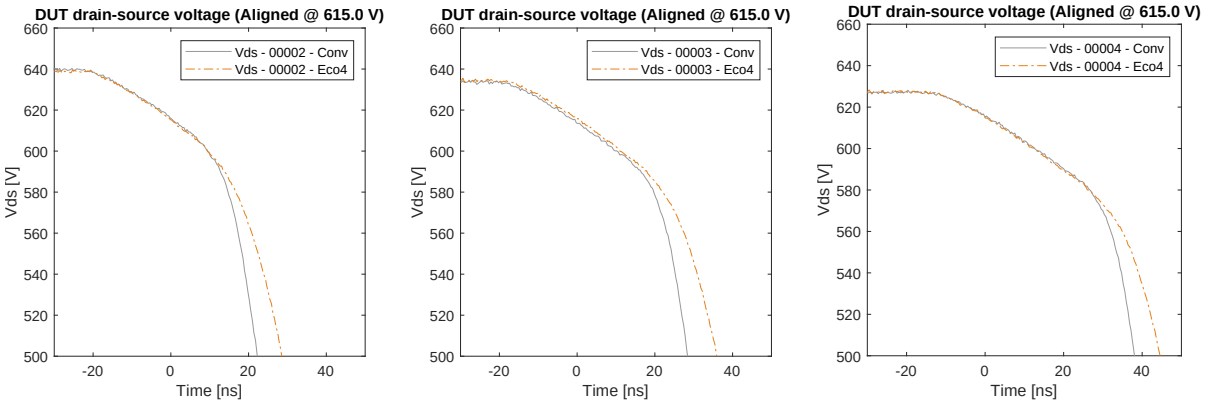
(a) **(b)** **(c)**

Figure A.10 Turn-on instances for Conv and Eco2 at: (a) 15 A, (b) 20 A, (c) 25 A.



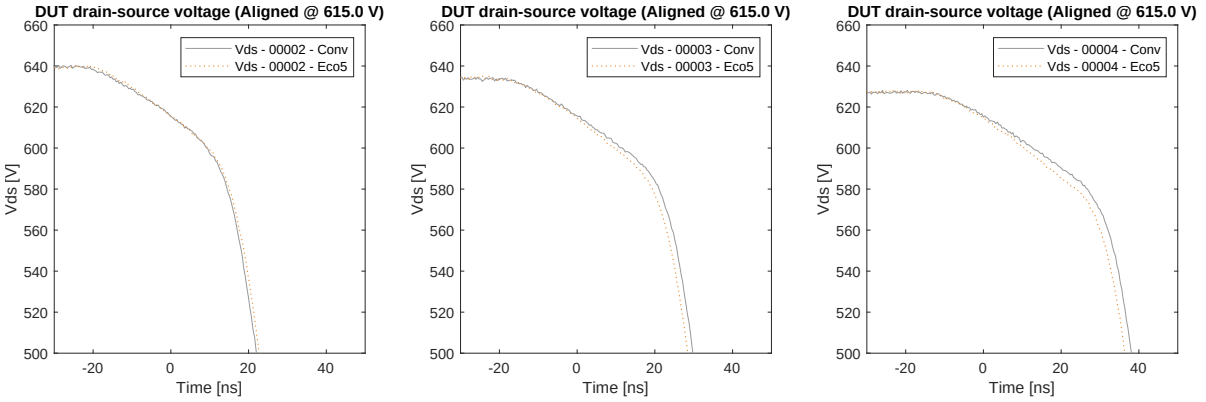
(a) **(b)** **(c)**

Figure A.11 Turn-on instances for Conv and Eco3 at: (a) 15 A, (b) 20 A, (c) 25 A.



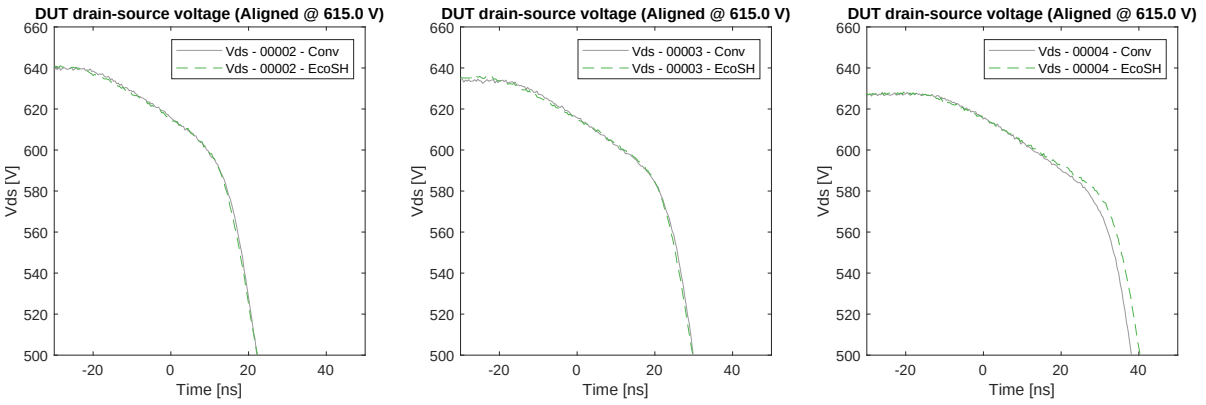
(a) **(b)** **(c)**

Figure A.12 Turn-on instances for Conv and Eco4 at: (a) 15 A, (b) 20 A, (c) 25 A.



(a) **(b)** **(c)**

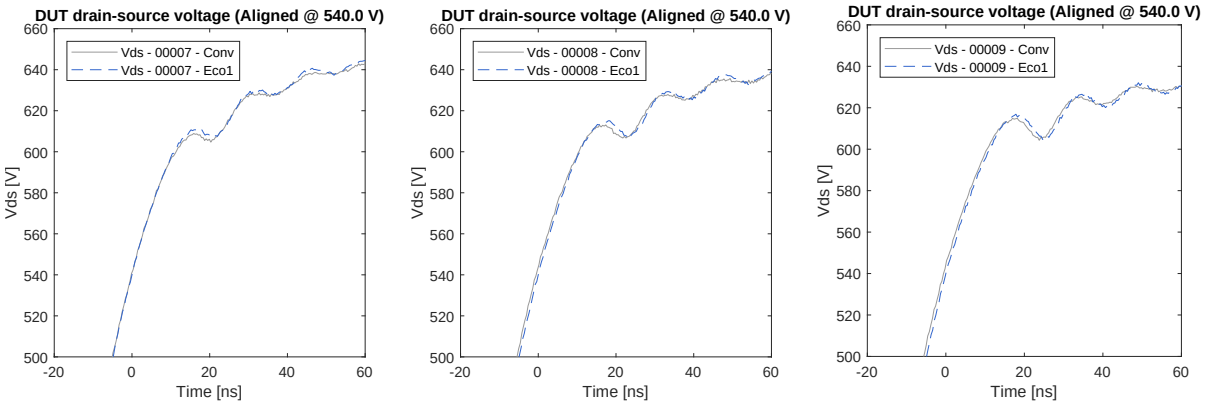
Figure A.13 Turn-on instances for Conv and Eco5 at: (a) 15 A, (b) 20 A, (c) 25 A.



(a) **(b)** **(c)**

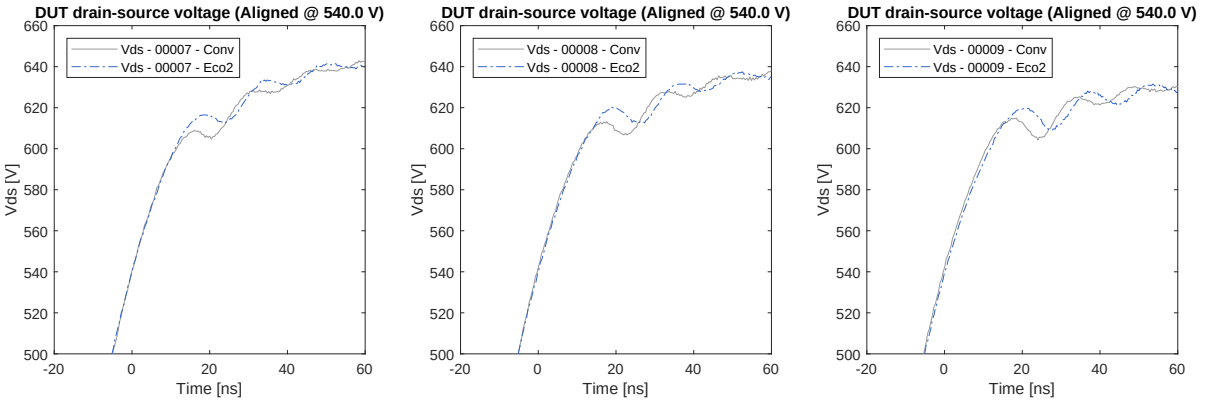
Figure A.14 Turn-on instances for Conv and EcoSH at: (a) 15 A, (b) 20 A, (c) 25 A.

A.6 Zoomed in Turn-Off DPT Instances with $R_g = 47\,\Omega$



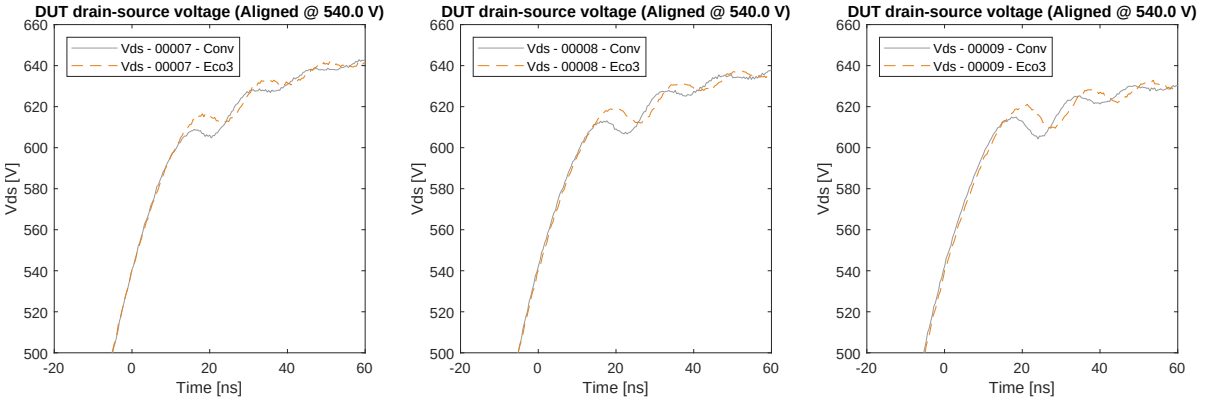
(a) **(b)** **(c)**

Figure A.15 Turn-on instances for Conv and Eco1 at: (a) 15 A, (b) 20 A, (c) 25 A.



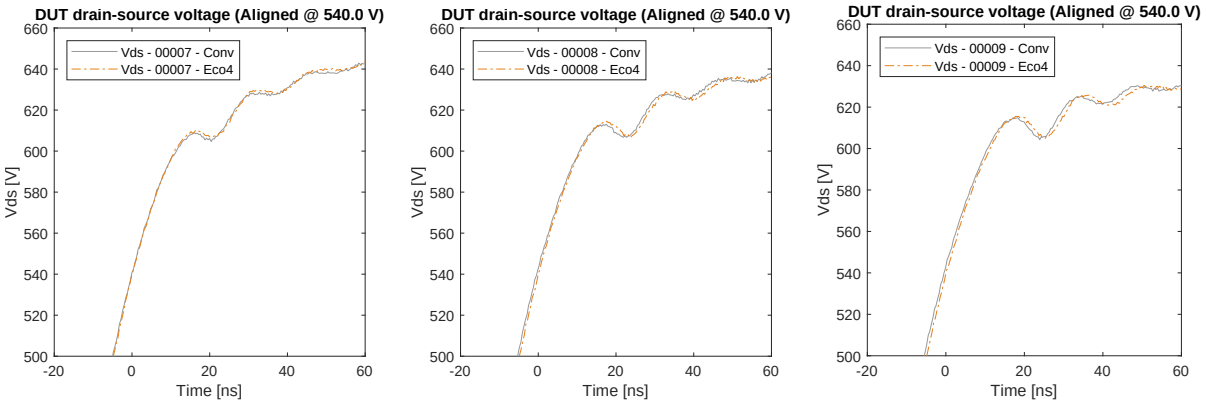
(a) **(b)** **(c)**

Figure A.16 Turn-on instances for Conv and Eco2 at: (a) 15 A, (b) 20 A, (c) 25 A.



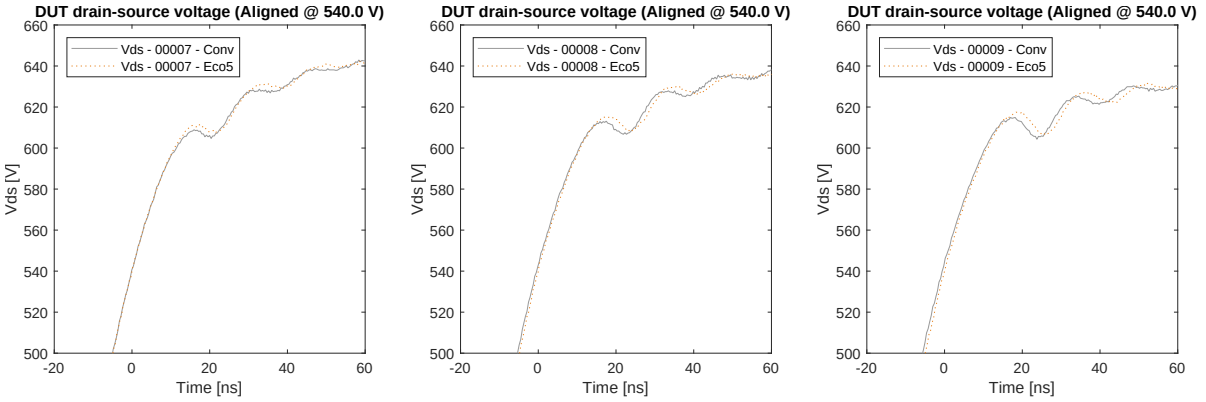
(a) **(b)** **(c)**

Figure A.17 Turn-on instances for Conv and Eco3 at: (a) 15 A, (b) 20 A, (c) 25 A.



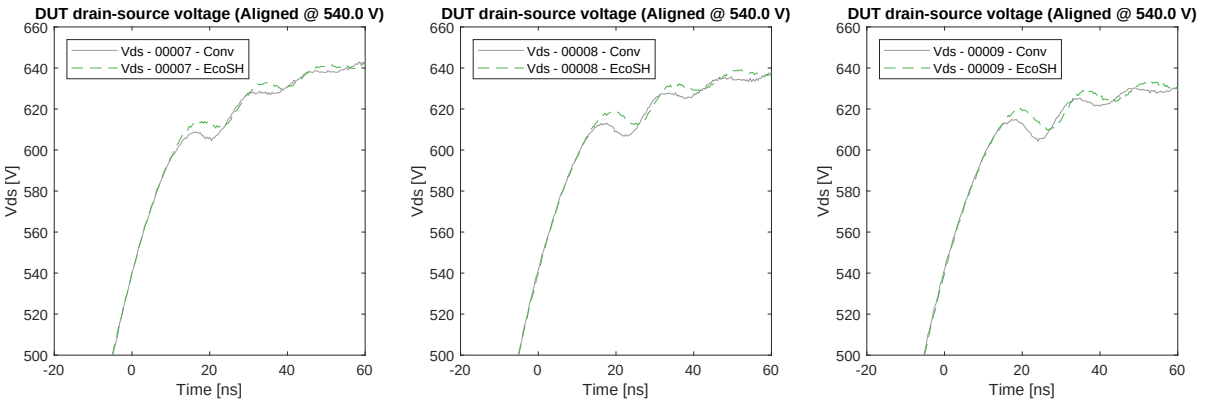
(a) **(b)** **(c)**

Figure A.18 Turn-on instances for Conv and Eco4 at: (a) 15 A, (b) 20 A, (c) 25 A.



(a) **(b)** **(c)**

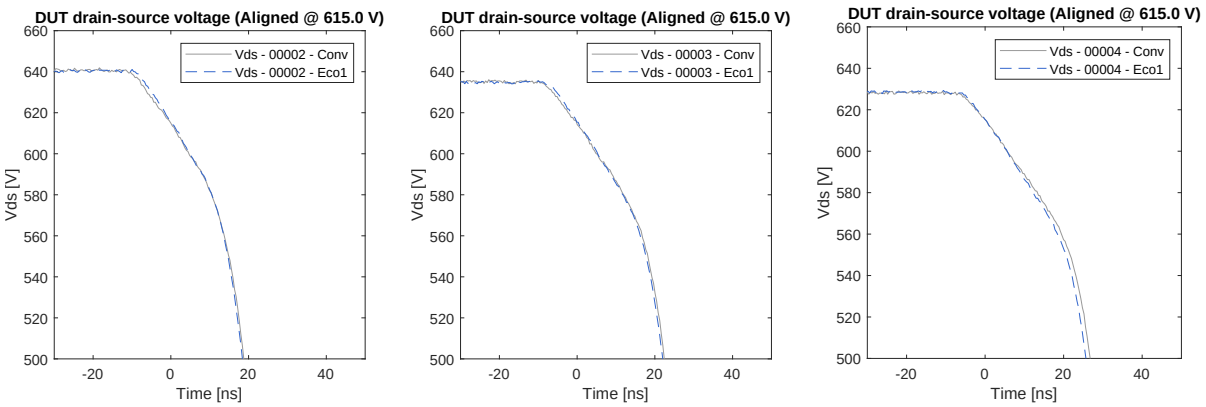
Figure A.19 Turn-on instances for Conv and Eco5 at: (a) 15 A, (b) 20 A, (c) 25 A.



(a) **(b)** **(c)**

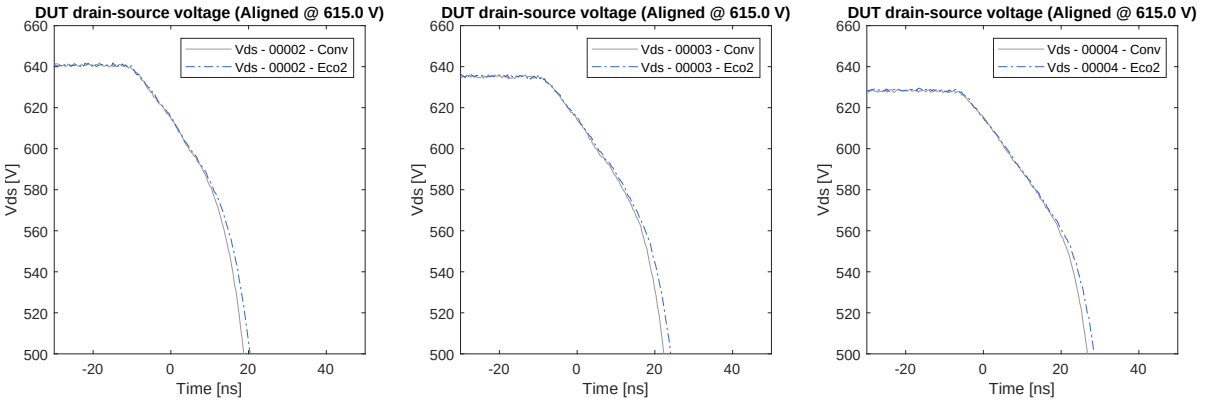
Figure A.20 Turn-off instances for Conv and EcoSH at: (a) 15 A, (b) 20 A, (c) 25 A.

A.7 Zoomed in Turn-On DPT Instances with $R_g = 24\,\Omega$



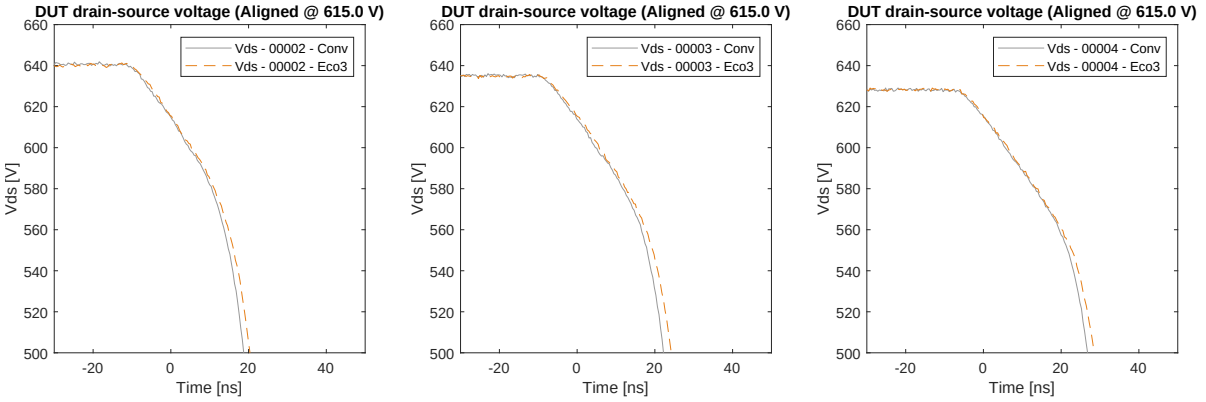
(a) **(b)** **(c)**

Figure A.21 Turn-on instances for Conv and Eco1 at: (a) 15 A, (b) 20 A, (c) 25 A.



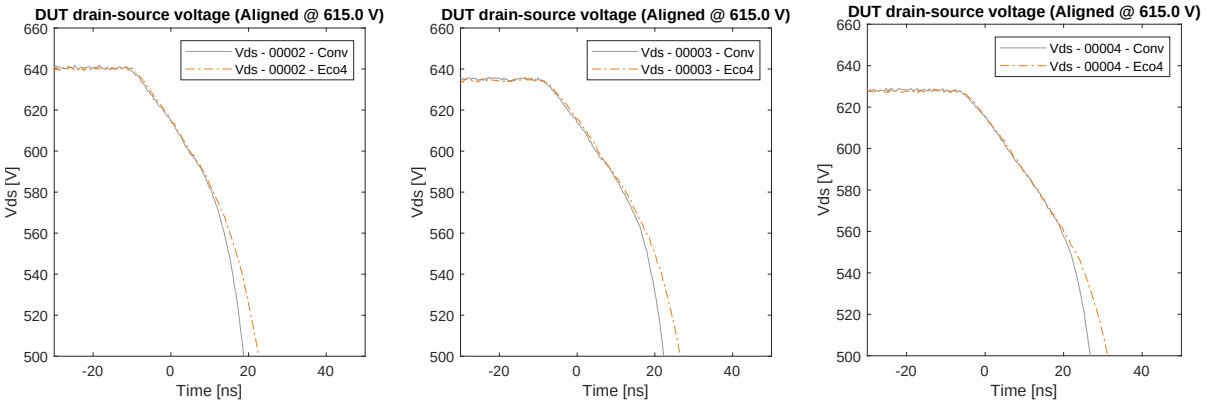
(a) **(b)** **(c)**

Figure A.22 Turn-on instances for Conv and Eco2 at: (a) 15 A, (b) 20 A, (c) 25 A.



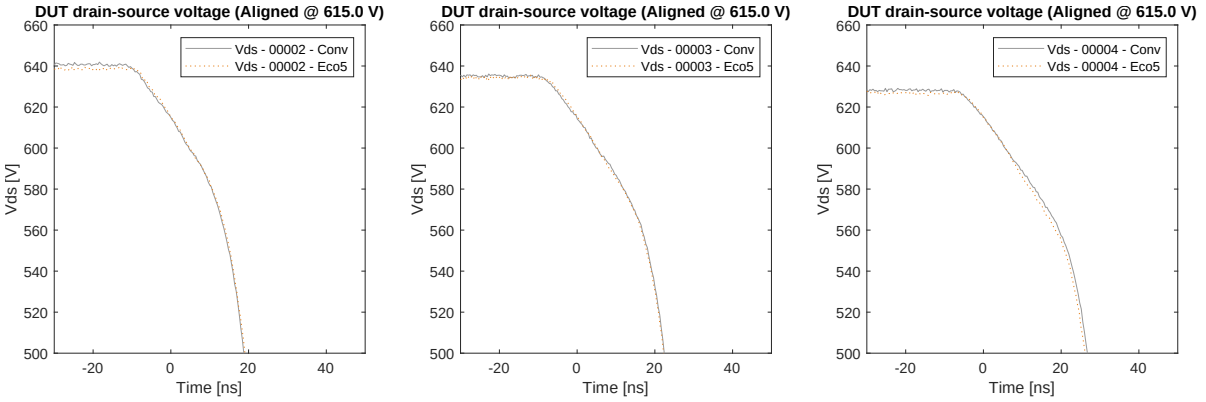
(a) **(b)** **(c)**

Figure A.23 Turn-on instances for Conv and Eco3 at: (a) 15 A, (b) 20 A, (c) 25 A.



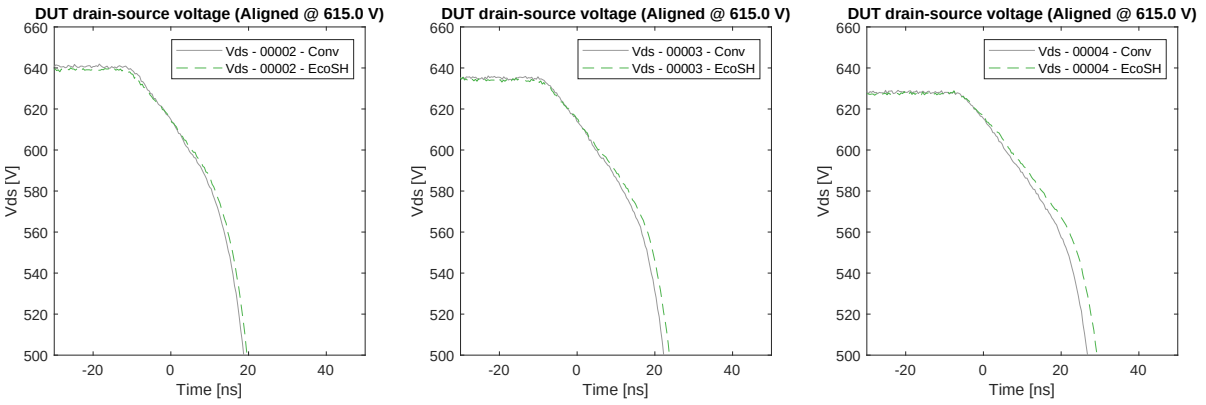
(a) **(b)** **(c)**

Figure A.24 Turn-on instances for Conv and Eco4 at: (a) 15 A, (b) 20 A, (c) 25 A.



(a) **(b)** **(c)**

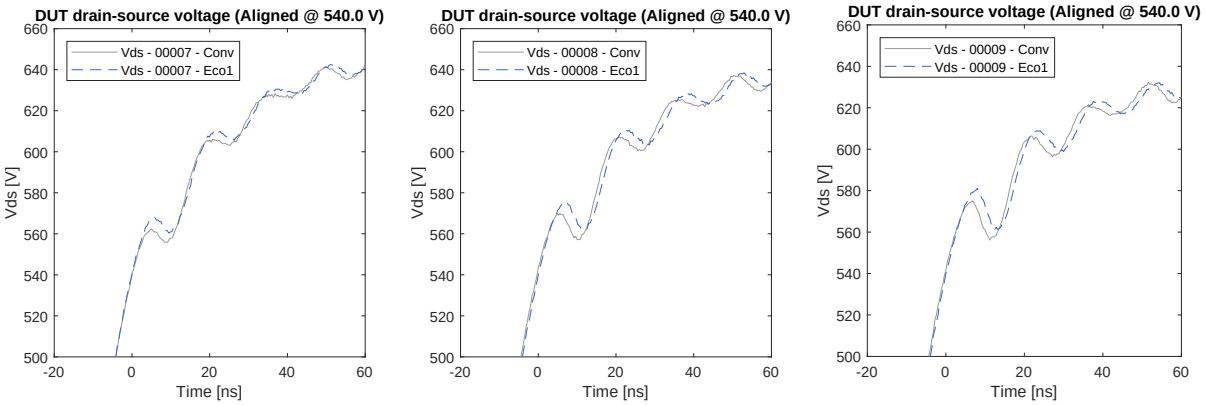
Figure A.25 Turn-on instances for Conv and Eco5 at: (a) 15 A, (b) 20 A, (c) 25 A.



(a) **(b)** **(c)**

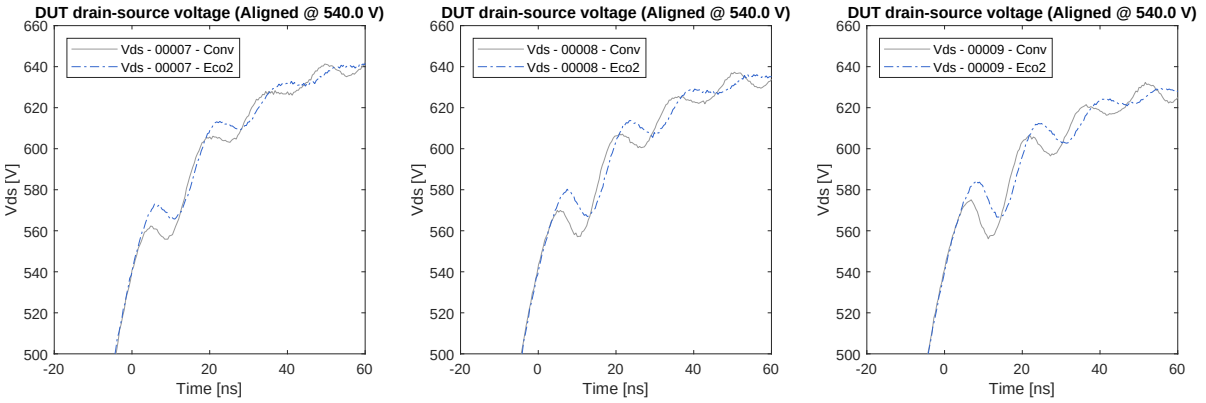
Figure A.26 Turn-on instances for Conv and EcoSH at: (a) 15 A, (b) 20 A, (c) 25 A.

A.8 Zoomed in Turn-Off DPT Instances with $R_g = 24\,\Omega$



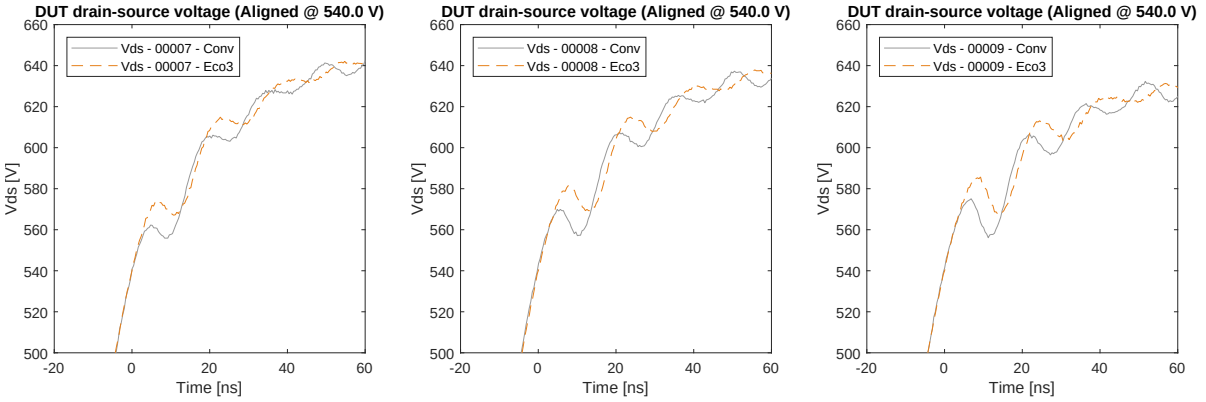
(a) **(b)** **(c)**

Figure A.27 Turn-on instances for Conv and Eco1 at: (a) 15 A, (b) 20 A, (c) 25 A.



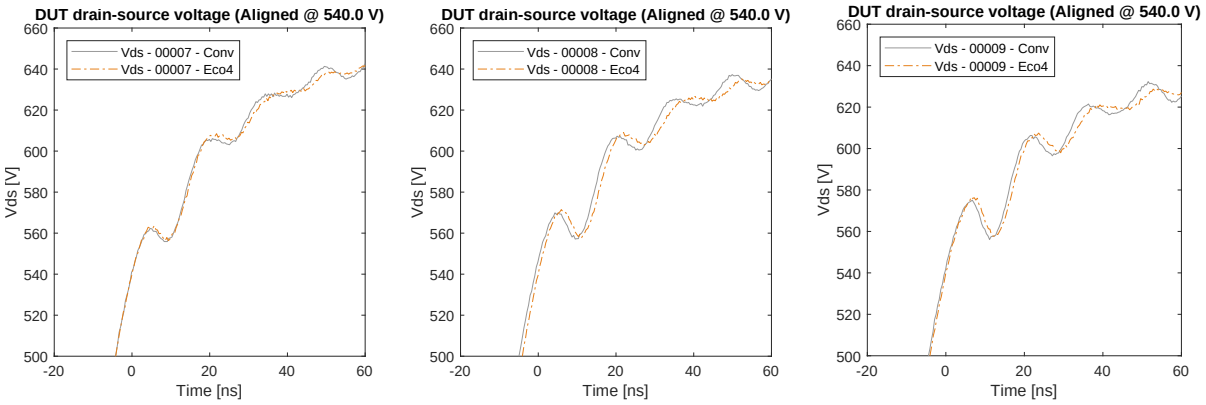
(a) **(b)** **(c)**

Figure A.28 Turn-on instances for Conv and Eco2 at: (a) 15 A, (b) 20 A, (c) 25 A.



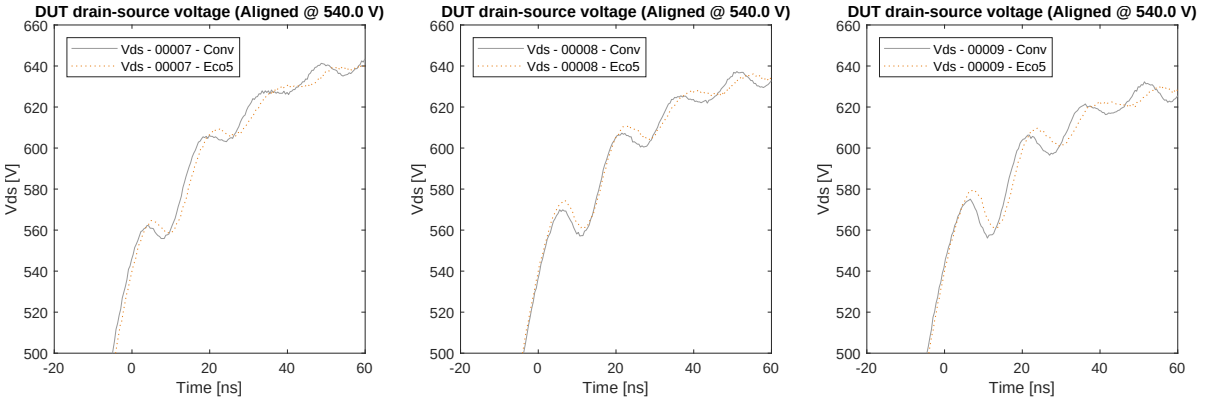
(a) **(b)** **(c)**

Figure A.29 Turn-on instances for Conv and Eco3 at: (a) 15 A, (b) 20 A, (c) 25 A.



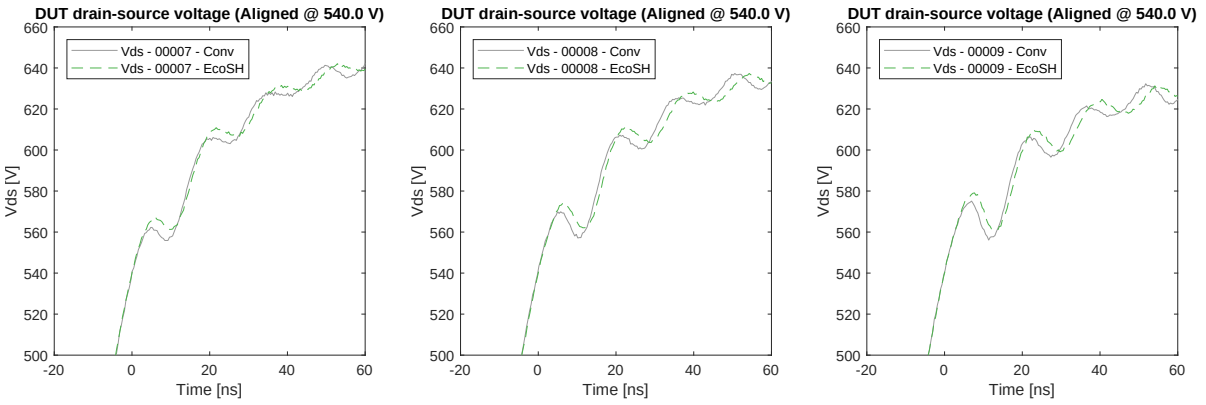
(a) **(b)** **(c)**

Figure A.30 Turn-on instances for Conv and Eco4 at: (a) 15 A, (b) 20 A, (c) 25 A.



(a) **(b)** **(c)**

Figure A.31 Turn-on instances for Conv and Eco5 at: (a) 15 A, (b) 20 A, (c) 25 A.



(a) **(b)** **(c)**

Figure A.32 Turn-off instances for Conv and EcoSH at: (a) 15 A, (b) 20 A, (c) 25 A.

B Energy Curve Models

B.1 Switching Energy Data and Curves with $R_g = 47\,\Omega$

Table B.1 Power loss model coefficients with $R_g = 47\,\Omega$.

Board	Conv	Eco1	Eco2	Eco3	Eco4	Eco5	EcoSH
Total Switching Loss Model							
E2	-0.0394	0.0432	0.301	-0.0234	-0.0243	0.00410	-0.244
E1	61.9	53.4	48.9	59.4	60.6	57.2	67.7
E0	25.3	57.0	123	65.8	132.	39.1	8.87
Turn-Off Switching Loss Model							
E2	-0.0200	-0.0340	0.336	-0.0195	-0.00870	-0.0288	-0.0436
E1	18.6	19.0	8.95	20.2	18.3	19.2	20.5
E0	-30.0	-28.7	32.5	-22.5	-22.7	-33.6	-35.6
Turn-On Switching Loss Model							
E2	-0.01940	0.07630	-0.03500	-0.00390	-0.0156	0.0329	-0.201
E1	43.3	34.4	40.0	39.3	42.3	38.1	47.2
E0	55.3	85.7	90.0	88.3	155	72.7	44.4

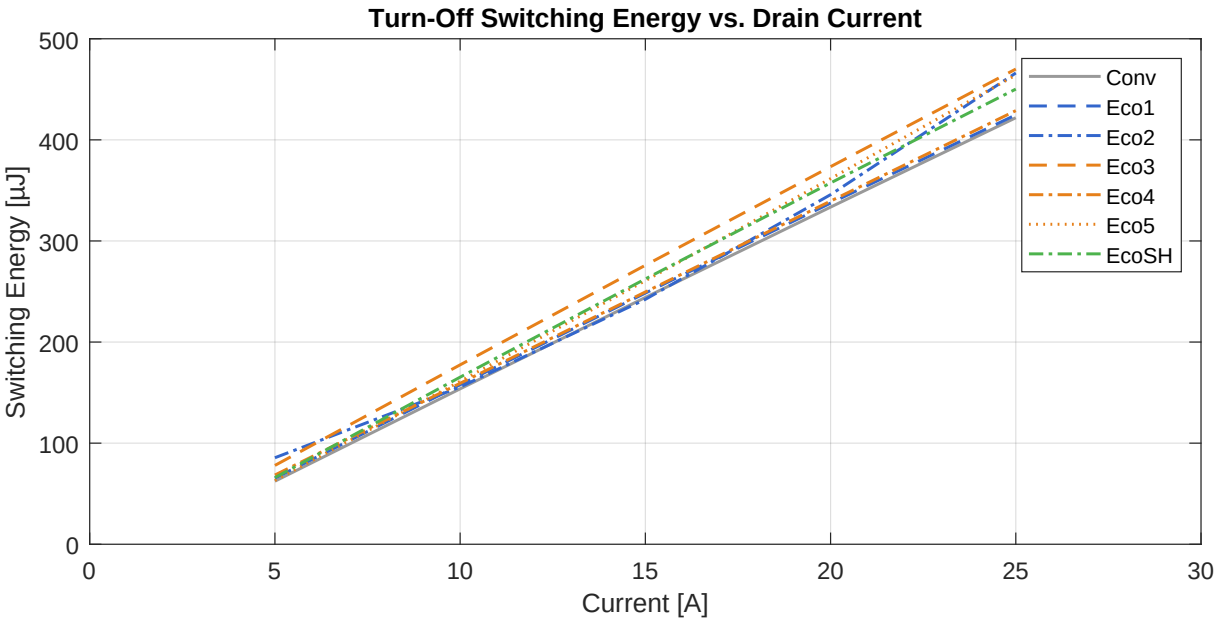


Figure B.1 Turn-off energy curves for all designed and tested boards.

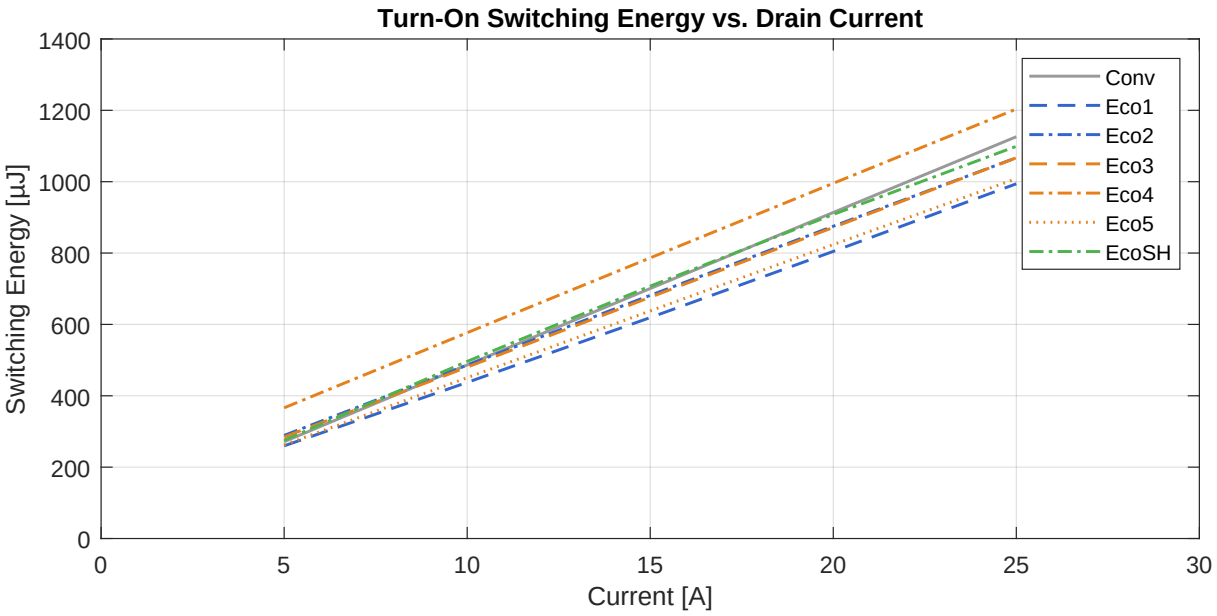


Figure B.2 Turn-on energy curves for all designed and tested boards.

B.2 Switching Energy Data and Curves with $R_g = 24\,\Omega$

Table B.2 Power loss model coefficients with $R_g = 24\,\Omega$.

Board	Conv	Eco1	Eco2	Eco3	Eco4	Eco5	EcoSH
Total Switching Loss Model							
E2	-0.146	-0.0542	-0.130	-0.114	-0.109	-0.0776	0.0275
E1	41.1	37.2	41.7	41.0	41.0	36.7	37.9
E0	101	99.3	143	143	249	98.4	95.3
Turn-Off Switching Loss Model							
E2	0.0134	-0.0023	0.00700	0.00500	0.0107	0.0186	0.00680
E1	8.362	9.32	9.35	9.52	8.93	8.42	9.42
E0	-23.4	-26.7	-21.3	-21.9	-23.6	-26.0	-26.4
Turn-On Switching Loss Model							
E2	-0.159	-0.0519	-0.137	-0.119	-0.119	-0.0962	0.0207
E1	32.8	27.9	32.4	31.5	32.1	28.3	28.5
E0	124	126	164	165	273	124	122

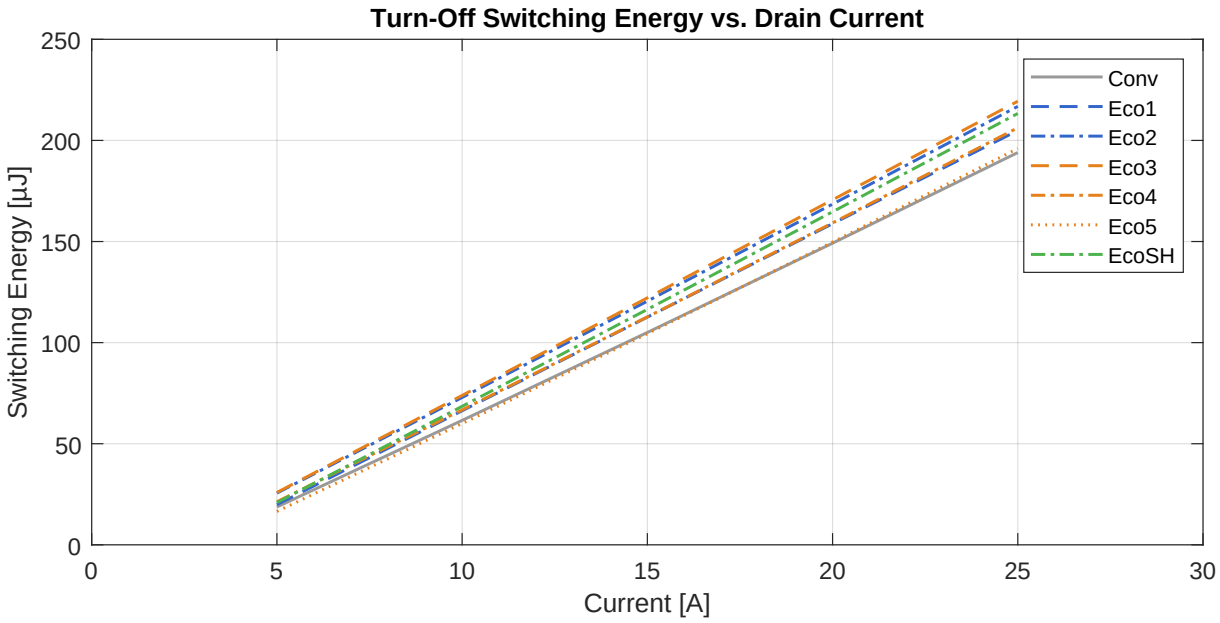


Figure B.3 Turn-off energy curves for all designed and tested boards.

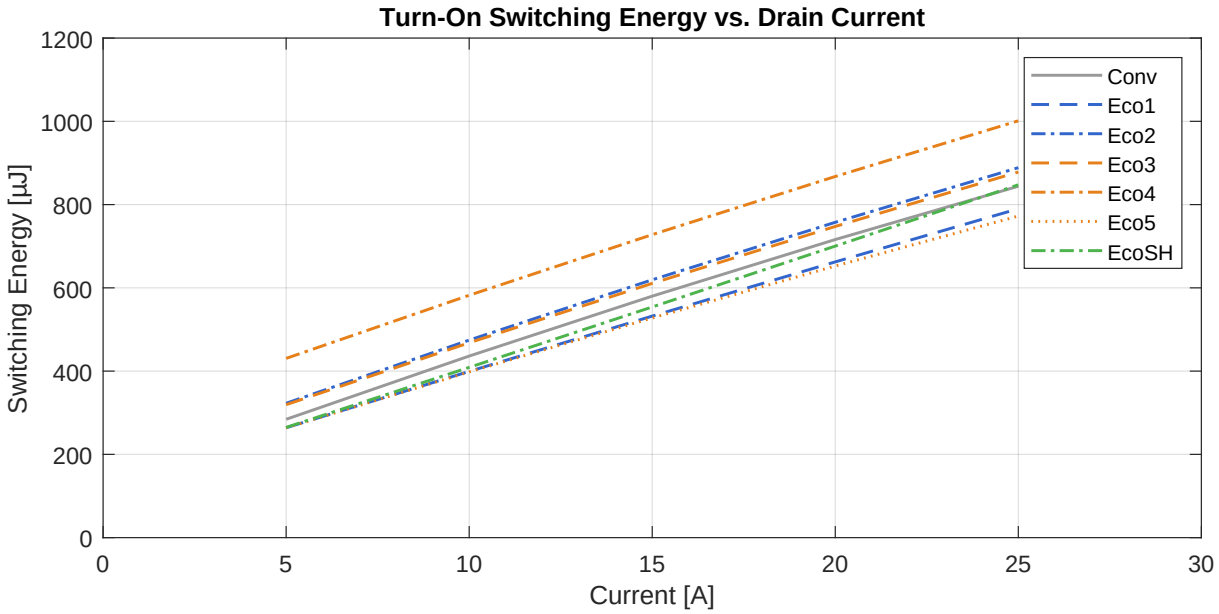


Figure B.4 Turn-on energy curves for all designed and tested boards.

B.3 Separate Average Normalized Total Switching Energies

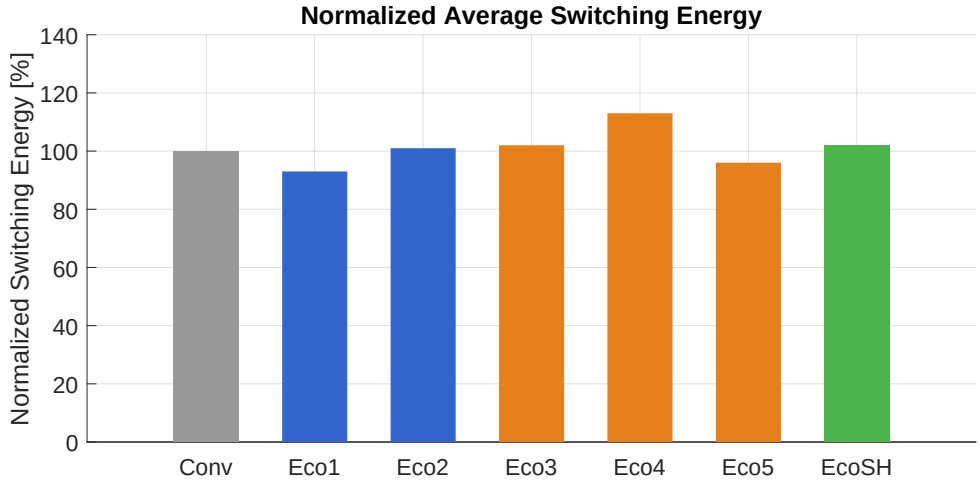


Figure B.5 Normalized average total switching energy for each board with $R_g = 47\,\Omega$.

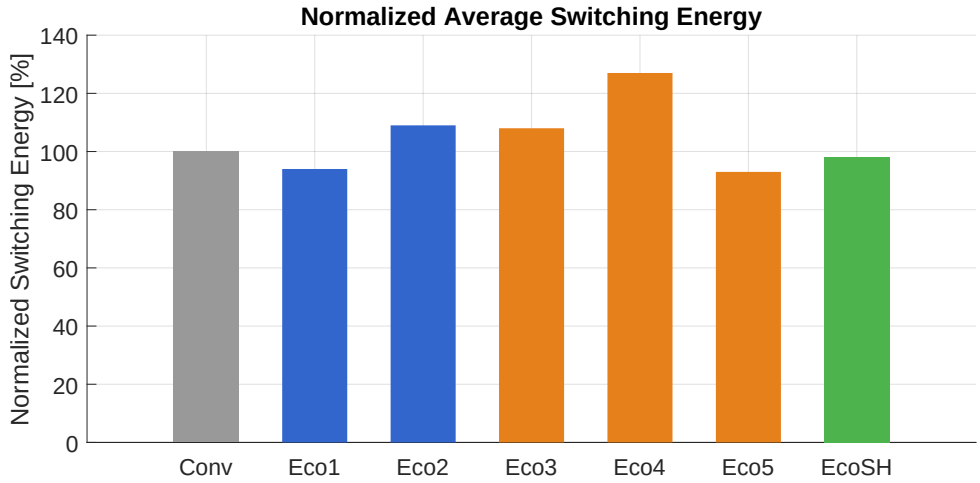


Figure B.6 Normalized total switching energy for each board with $R_g = 24\,\Omega$.

C DPT Second Order Oscillation Frequency Determination

C.1 Turn-Off DPT Oscillations with $R_g = 47\,\Omega$

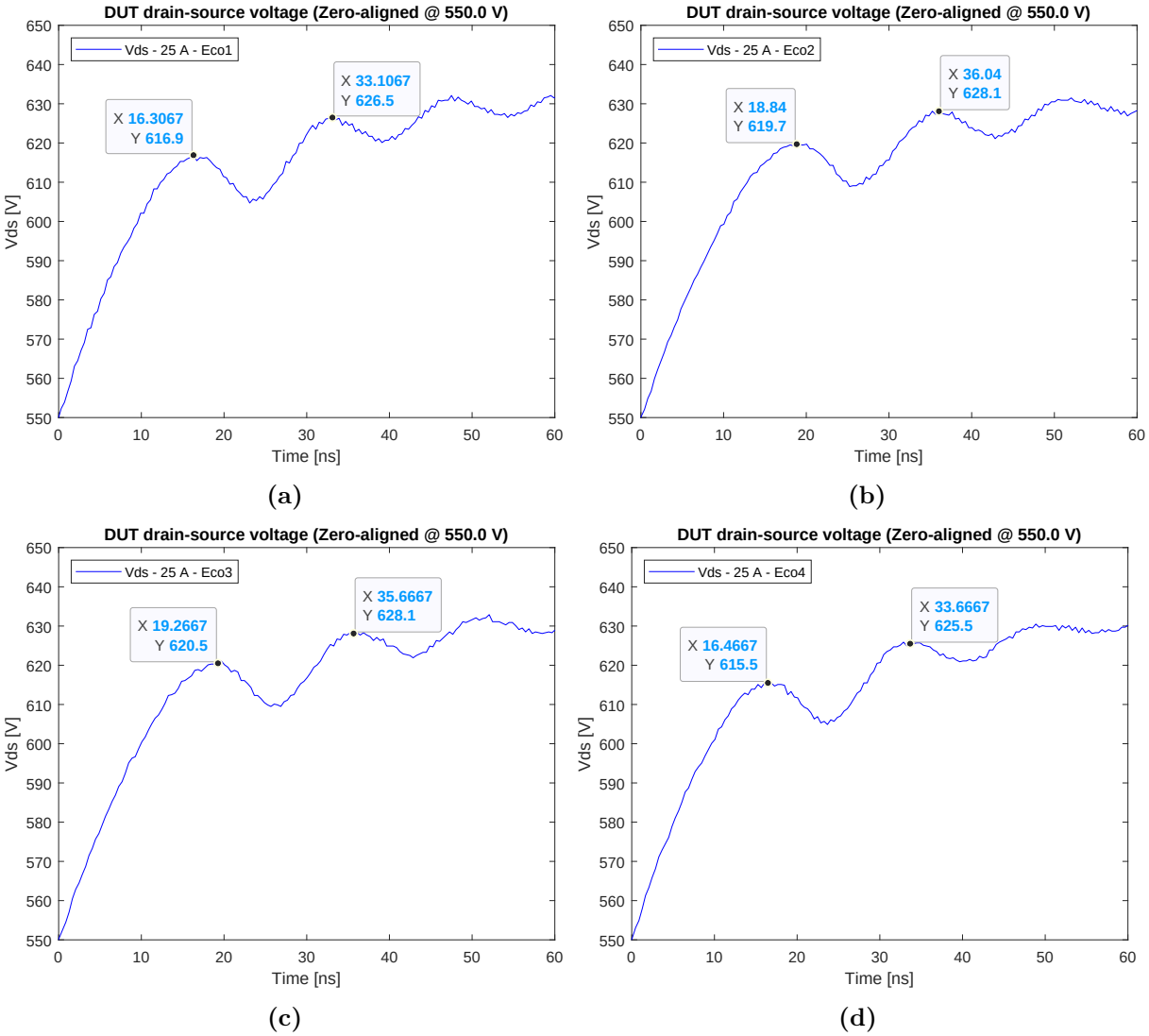


Figure C.1 Turn-off Oscillations at 25 A for board: (a) Eco1 (b) Eco2 (c) Eco3 (d) Eco4.

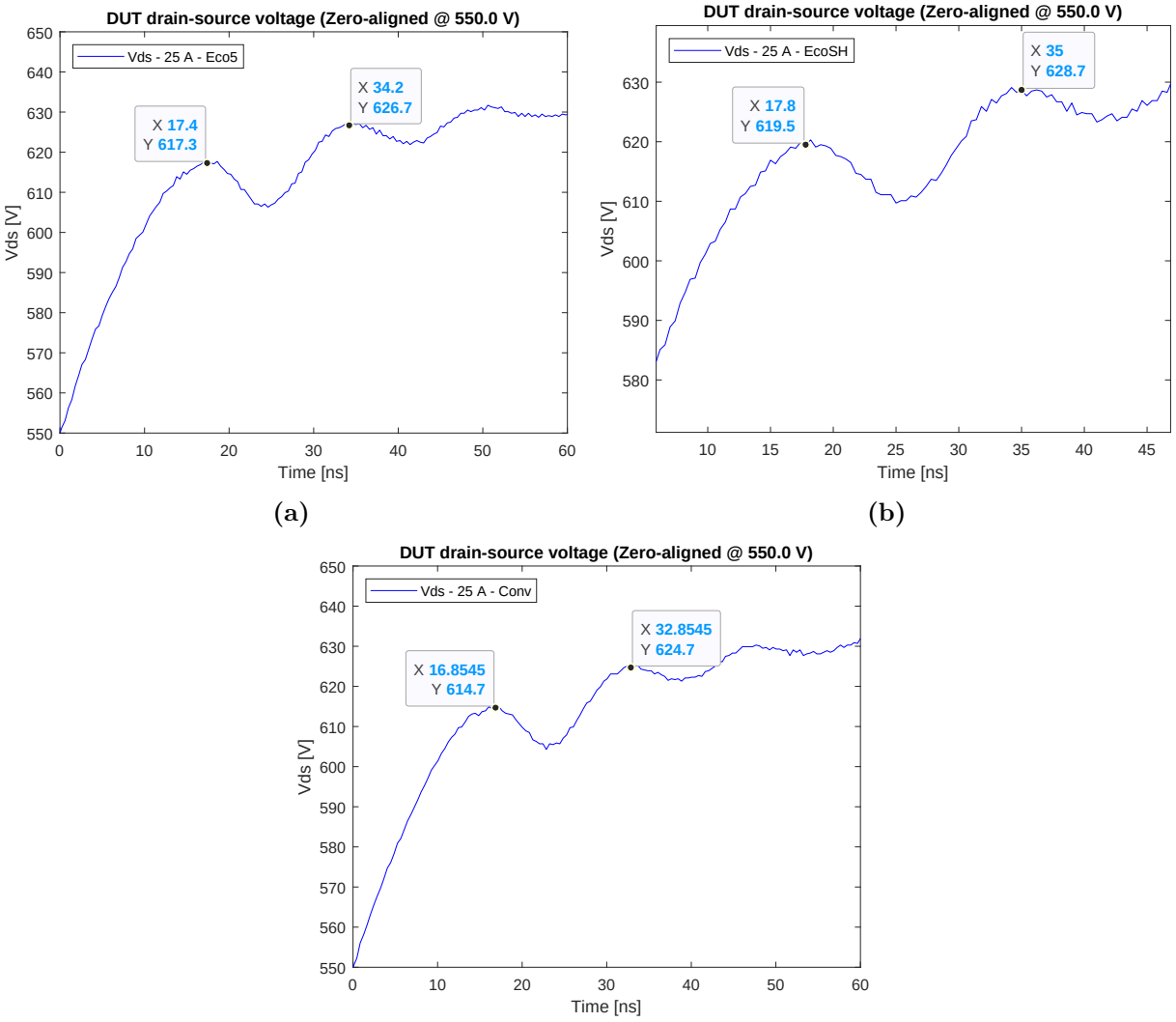


Figure C.2 Turn-off Oscillations at 25 A for board: (a) Eco5 (b) EcoSH (c) Conv

C.2 Turn-Off DPT Oscillations with $Rg = 24\,\Omega$

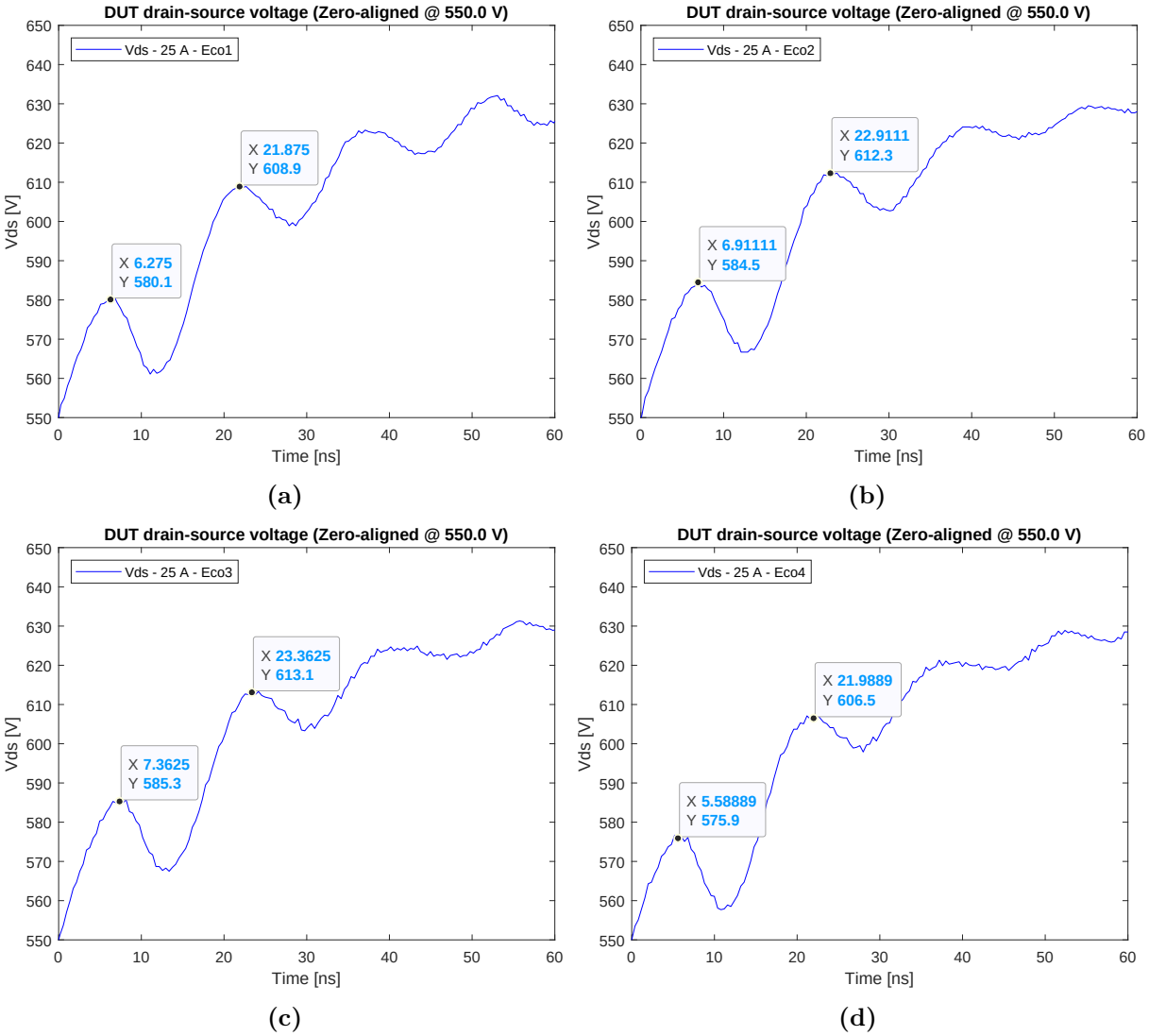


Figure C.3 Turn-off Oscillations at 25 A for board: (a) Eco1 (b) Eco2 (c) Eco3 (d) Eco4.

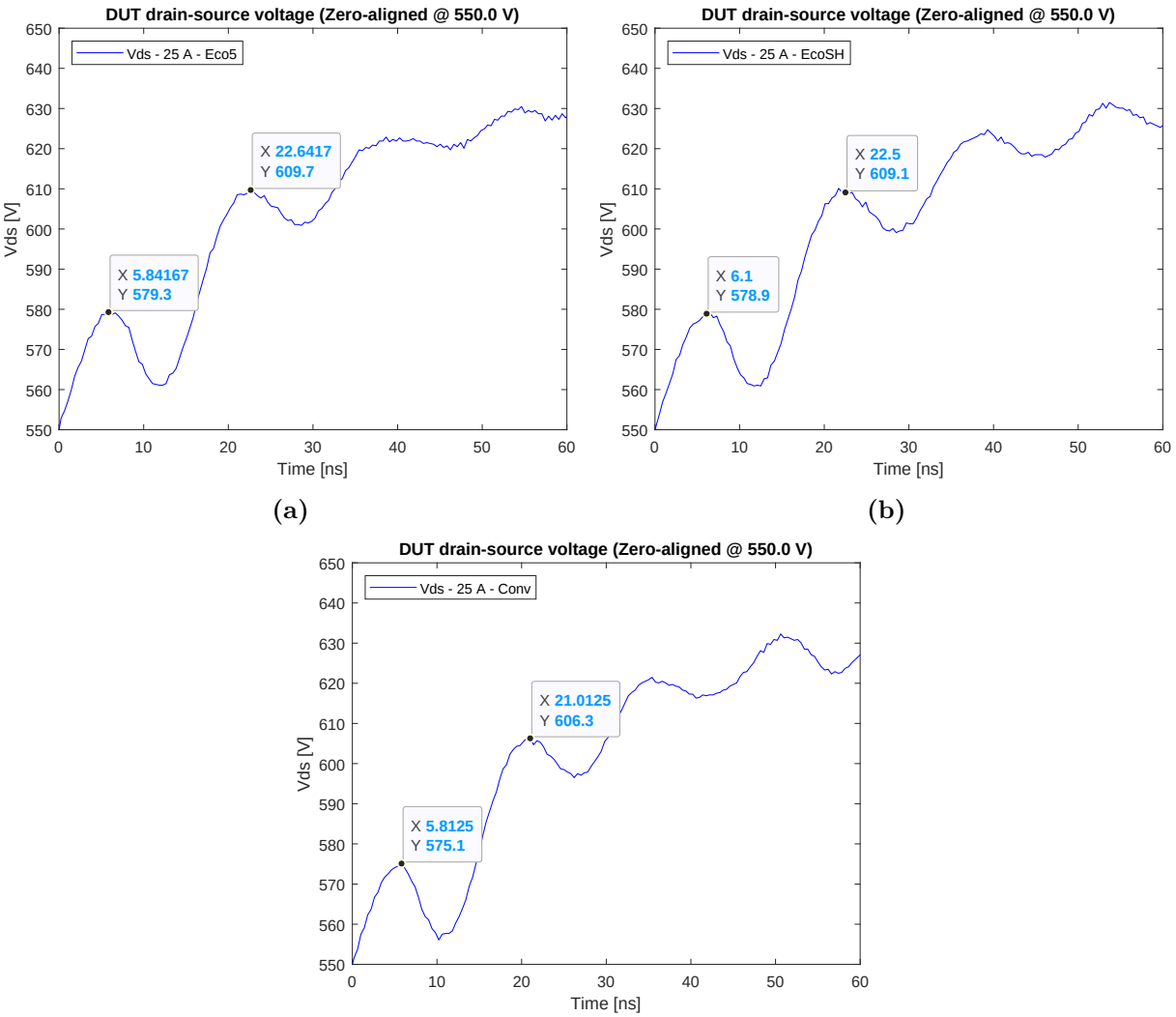


Figure C.4 Turn-off Oscillations at 25 A for board: (a) Eco5 (b) EcoSH (c) Conv.

D Mechanical Testing Results

D.1 Average Flexural Strength

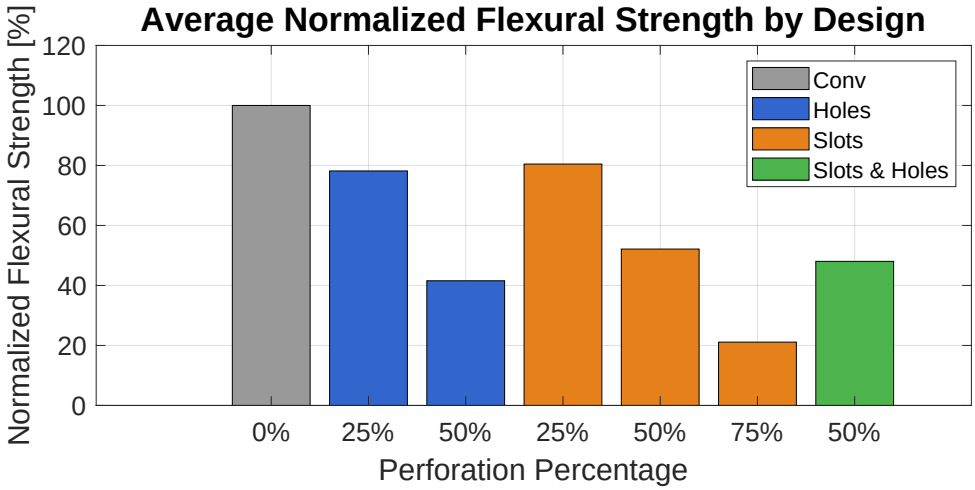


Figure D.1 Normalized flexural strength of the PCBs.

The bar chart presents the average values for each group of the tested boards in a normalized manner. The conventional design, without holes or slots, is used as the reference, and thus it is set to 1. The first two bars to the right of the conventional design in blue color represent the hole perforation implementations with 25 % and 50 % perforation levels, respectively. The 25 % hole configuration retains approximately 78.2 % of the original PCB's flexural strength, while the 50 % implementation shows a more significant reduction to 41.5 %. The decline in normalized flexural strength with increasing perforation percentage can be linked to the accumulated impact of the geometric discontinuities. As the percentage of perforations increases, the structural continuity is increasingly reduced, and thus the overall ability of the board to withstand bending decreases as well. The bars show a steady decline in strength as more material is removed.

The three orange bars in the middle represent the slot perforation at 23 %, 53 %, and 76 %, from left to right. The data indicates that a perforation of 23 % leads to a reduction of the PCB's flexural strength by 20 %, retaining 80 % of its original strength. For the boards with 53 % perforation, the flexural strength is reduced to 52 % of the original value. In the case of 76 % perforation, the remaining strength is only 21 % of the initial value.

Table D.1 Mechanical Test Results for PCB Samples.

Group	Name	$F_{\max}$ [N]	$M_{\max}$ [Nm]	σ_f [MPa]	avg σ_f	$\sigma_{f,\text{group,norm}}$	Deviation
Solid	PCB_conv1	541.99	10704.34	416.75	411.14	1.000	5.30
	PCB_conv2	529.36	10454.59	407.03			
	PCB_conv3	533.31	10503.90	409.99			
	PCB_conv4	534.26	10551.71	410.81			
25% holes	PCB_eco1_1	402.1	7953.68	309.6	321.37	0.782	11.82
	PCB_eco1_2	422.21	8338.70	324.65			
	PCB_eco1_3	430.81	8508.66	331.26			
	PCB_eco1_4	416.06	8217.30	319.92			
50% holes	PCB_eco2_1	219.01	4325.44	168.40	170.87	0.416	7.16
	PCB_eco2_2	232.71	4535.99	178.93			
	PCB_eco2_3	216.72	4280.35	166.65			
	PCB_eco2_4	220.41	4335.18	169.49			
25% slots	PCB_eco3_1	477.88	9438.27	367.46	330.83	0.804	31.83
	PCB_eco3_2	412.06	8175.52	316.82			
	PCB_eco3_3	413.95	8175.67	318.30			
	PCB_eco3_4	417.12	8238.11	320.73			
50% slots	PCB_eco4_1	267.13	5275.86	205.40	214.32	0.521	22.84
	PCB_eco4_2	266.78	5268.32	205.13			
	PCB_eco4_3	268.01	5293.20	206.08			
	PCB_eco4_4	240.75	4816.12	184.87			
75% slots	PCB_eco5_1	109.59	2164.45	84.26	86.77	0.211	8.68
	PCB_eco5_2	105.65	2154.05	83.83			
	PCB_eco5_3	125.75	2483.57	95.69			
	PCB_eco5_4	106.58	2122.42	82.24			
50% slots & holes	PCB_SnH_1	261.16	5157.92	200.82	197.47	0.480	7.40
	PCB_SnH_2	253.43	5005.35	194.87			
	PCB_SnH_3	264.50	5223.83	203.38			
	PCB_SnH_4	248.16	4901.24	190.82			

D.2 Force and Deflection Curves

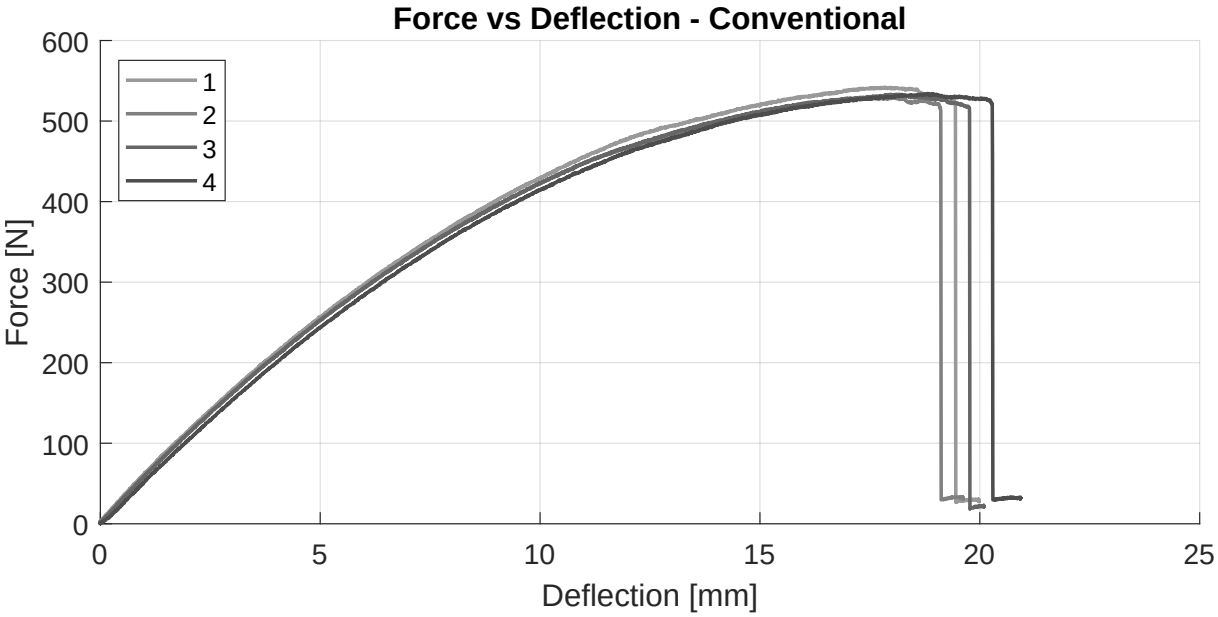


Figure D.2 Illustration of the force over the deflection of the specimen for all "Conventional" specimens.

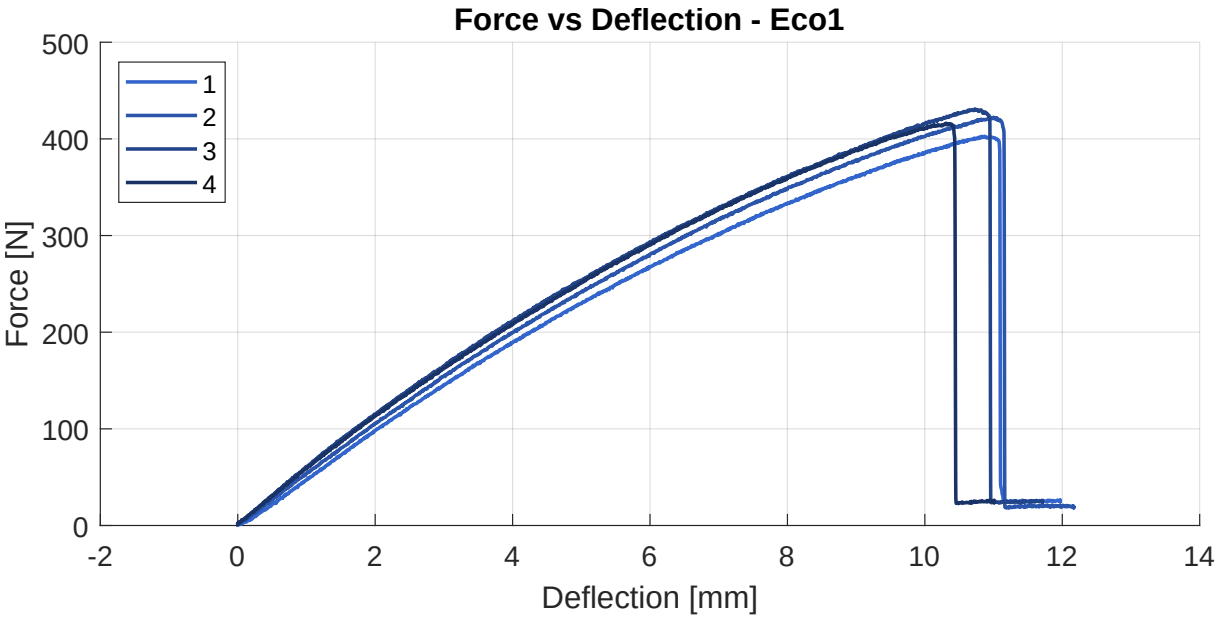


Figure D.3 Illustration of the force over the deflection of the specimen for all "Eco1" specimens.

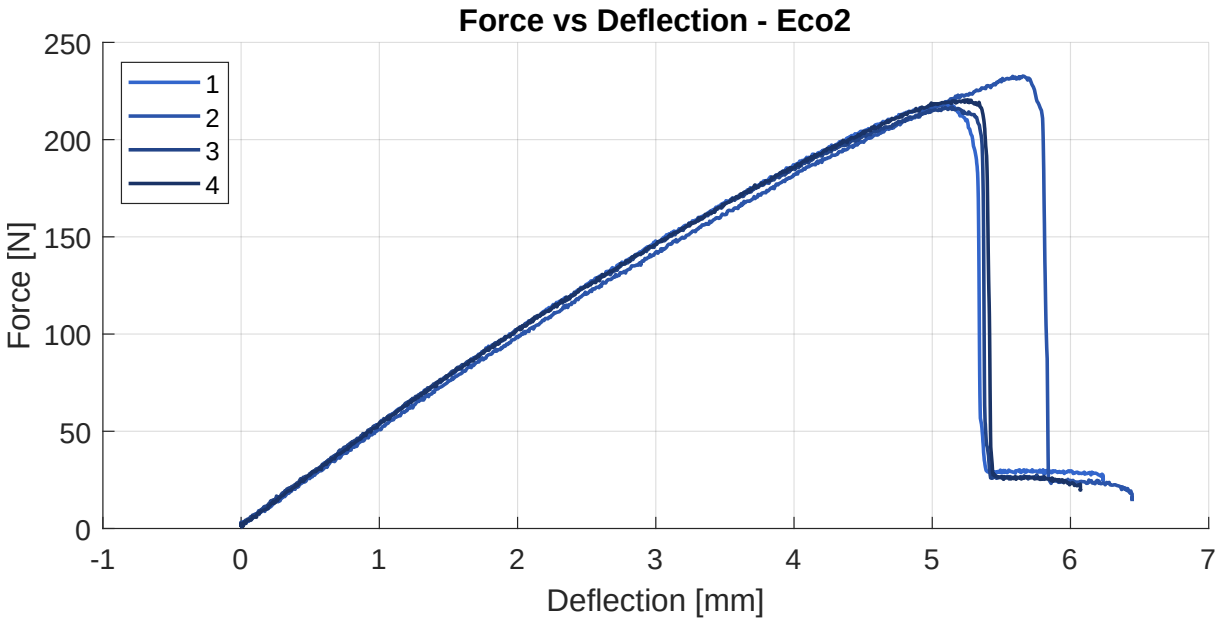


Figure D.4 Illustration of the force over the deflection of the specimen for all "Eco2" specimens.

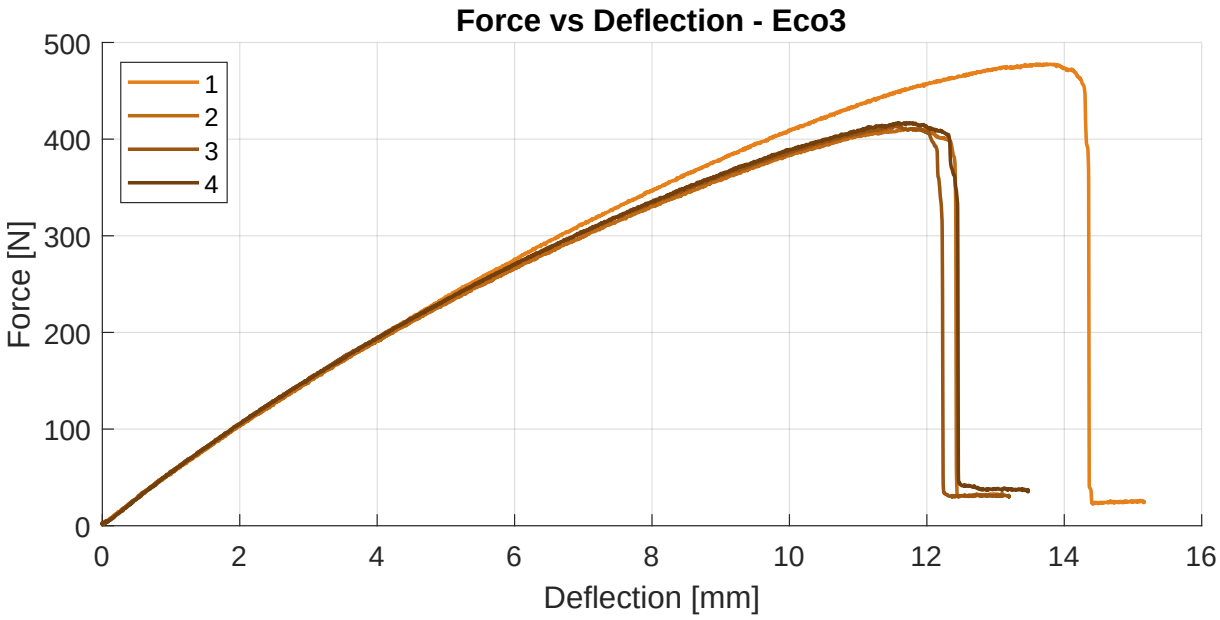


Figure D.5 Illustration of the force over the deflection of the specimen for all "Eco3" specimens.

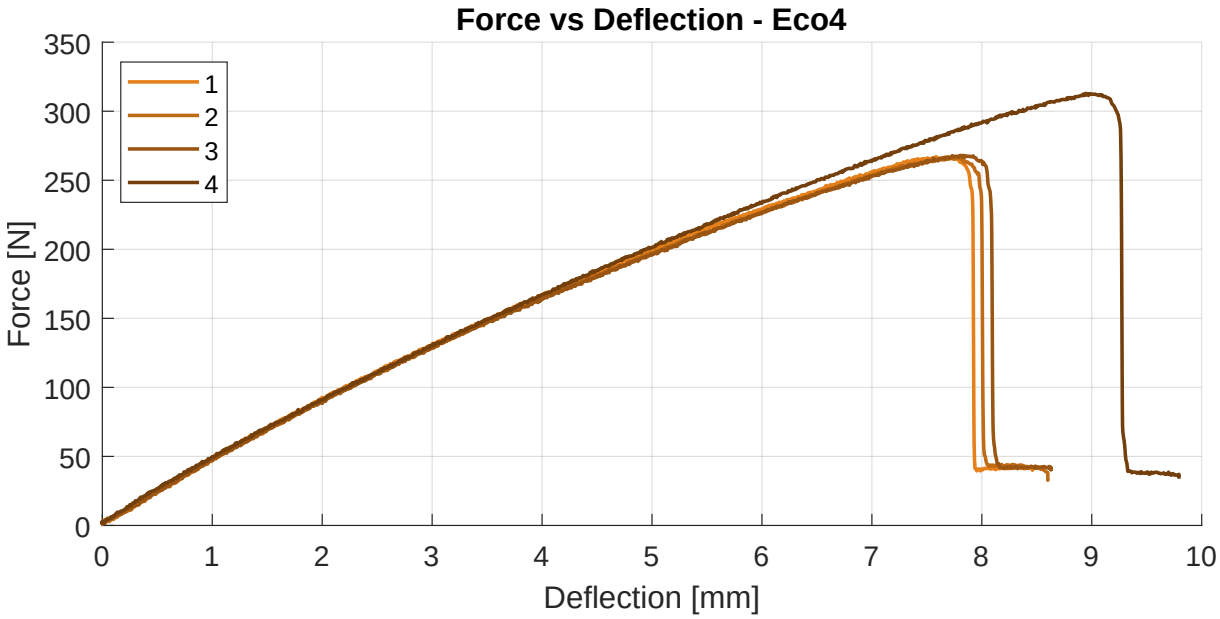


Figure D.6 Illustration of the force over the deflection of the specimen for all "Eco4" specimens.

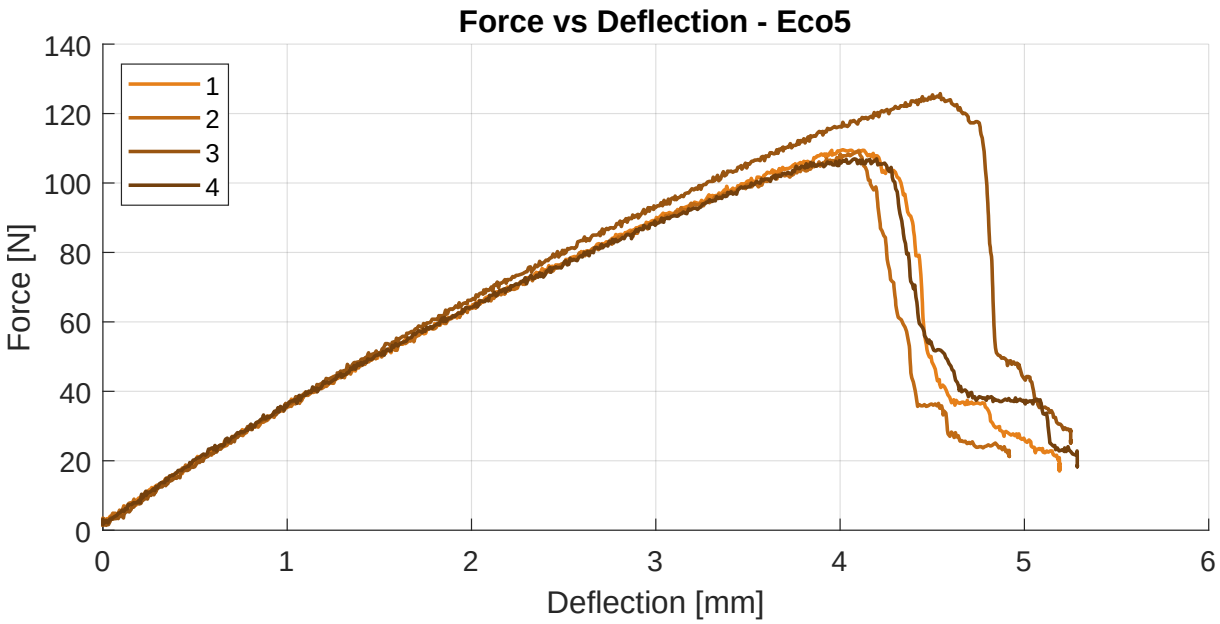


Figure D.7 Illustration of the force over the deflection of the specimen for all "Eco5" specimens.

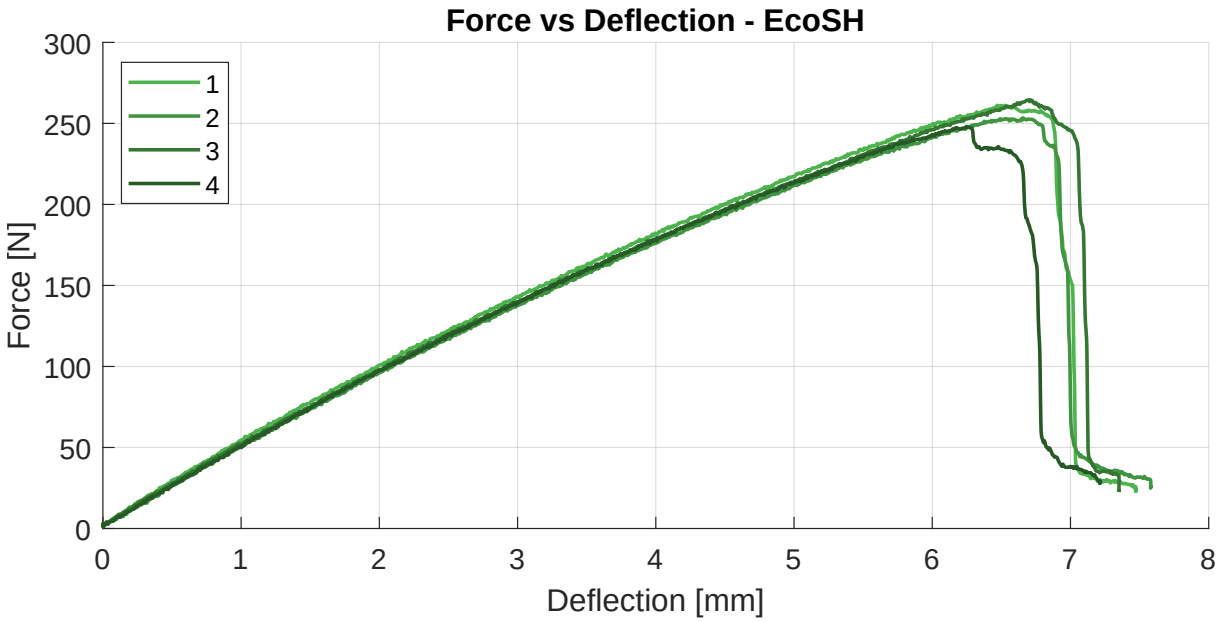


Figure D.8 Illustration of the force over the deflection of the specimen for all "EcoSH" specimens.

E Pareto Point Figures

E.1 Efficiency vs Power Density

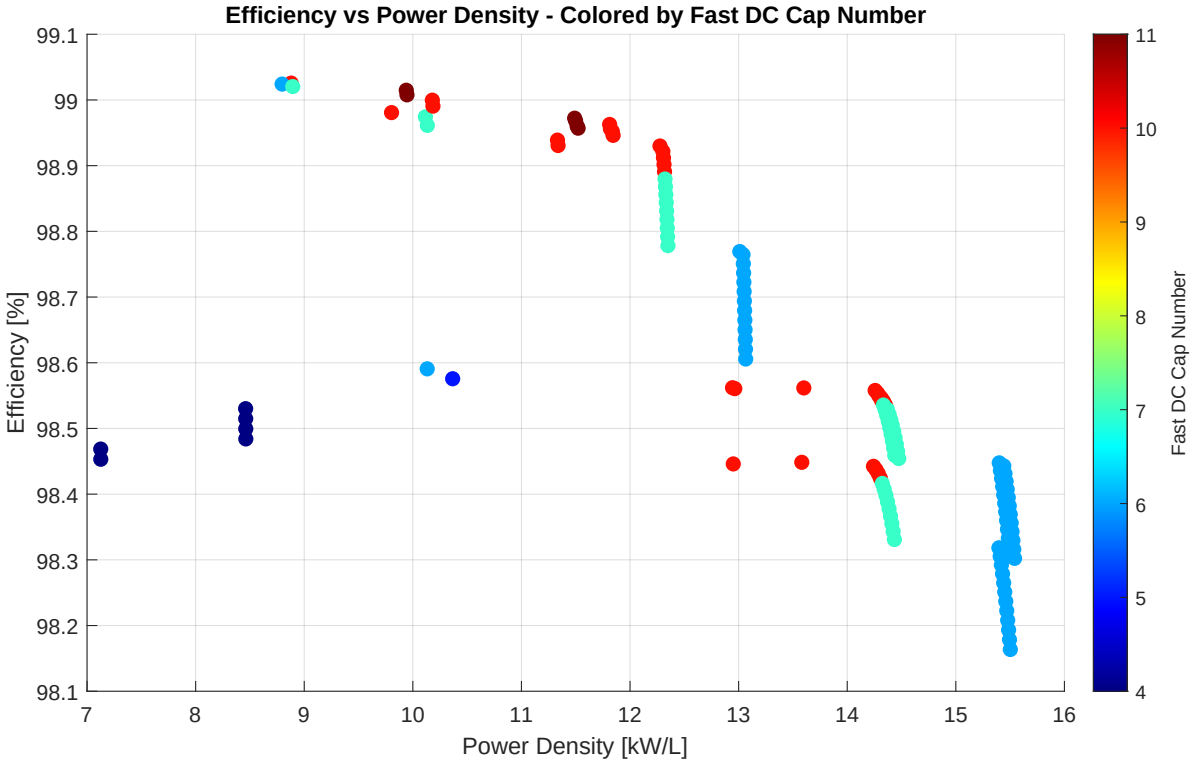


Figure E.1 2D plot of the Pareto optimal solutions showing efficiency and power density colored by the fast DC capacitor database entry.

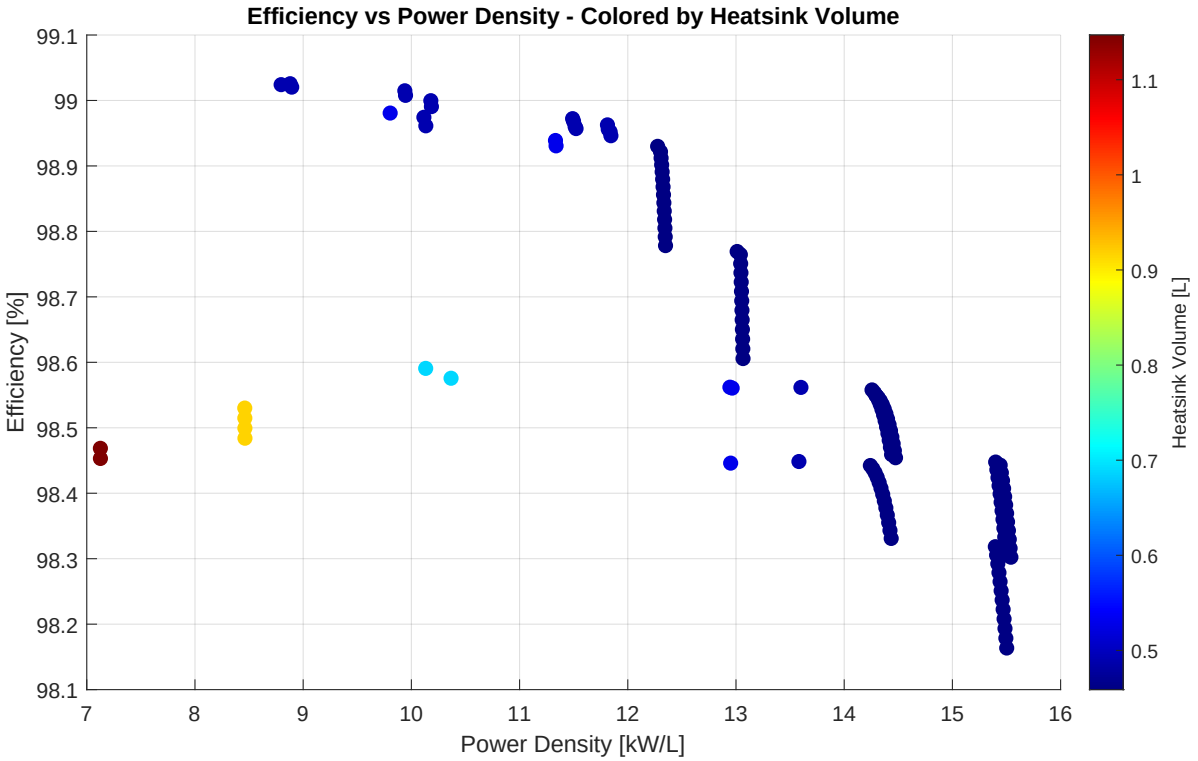


Figure E.2 2D plot of the Pareto optimal solutions showing efficiency and power density colored by the heatsink volume.

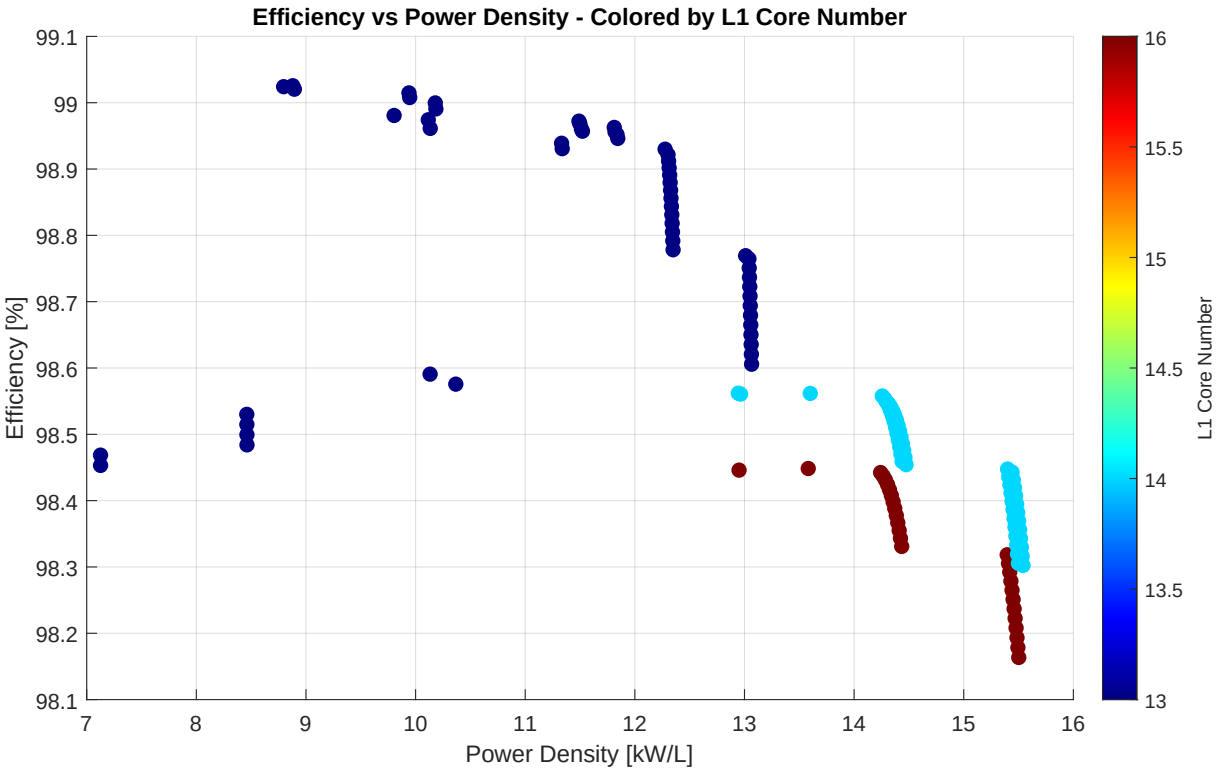


Figure E.3 2D plot of the Pareto optimal solutions showing efficiency and power density colored by entry of the core used for L1.

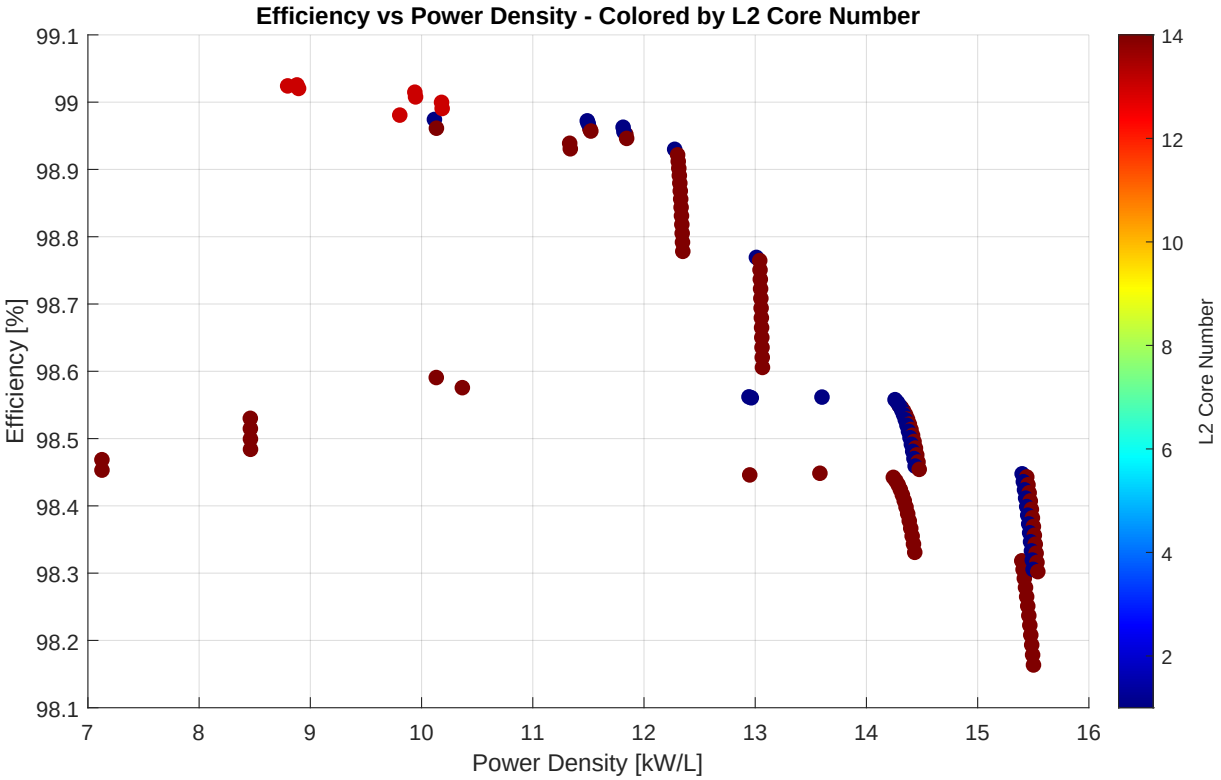


Figure E.4 2D plot of the Pareto optimal solutions showing efficiency and power density colored by entry of the core used for L2

E.2 Efficiency vs Recyclability

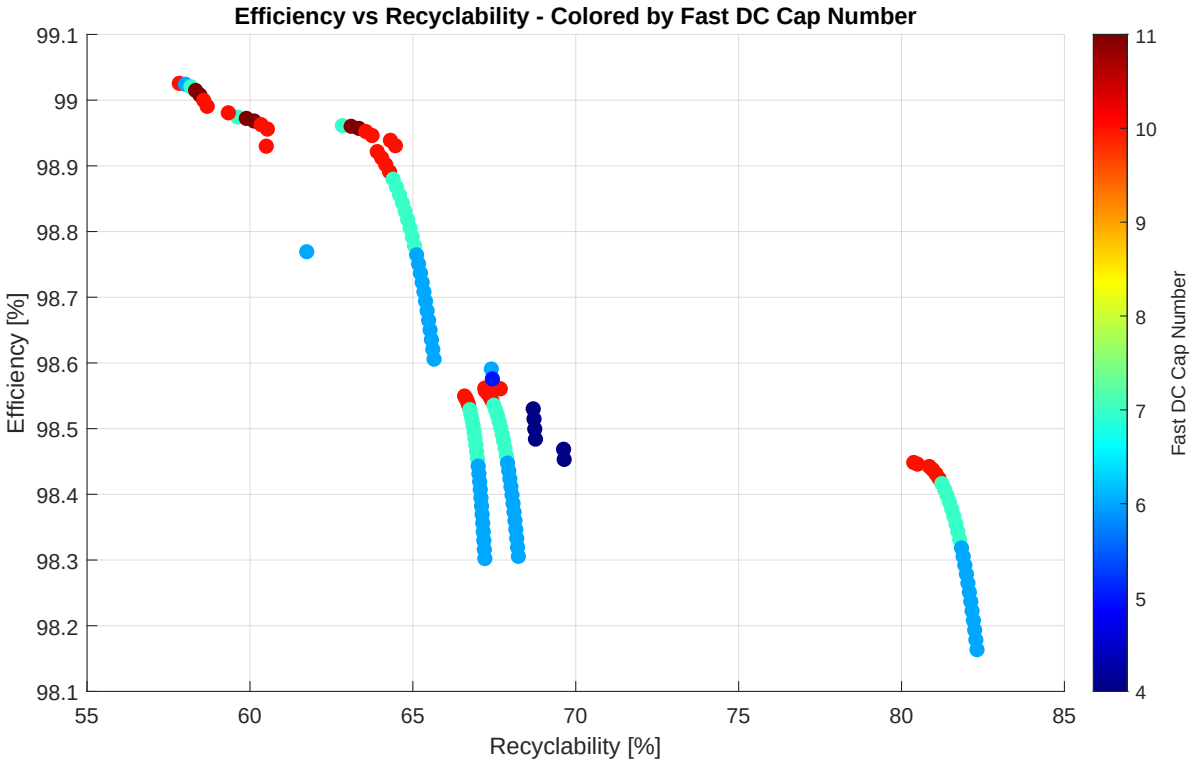


Figure E.5 2D plot of the Pareto optimal solutions showing efficiency and recyclability colored by the fast DC capacitor database entry.

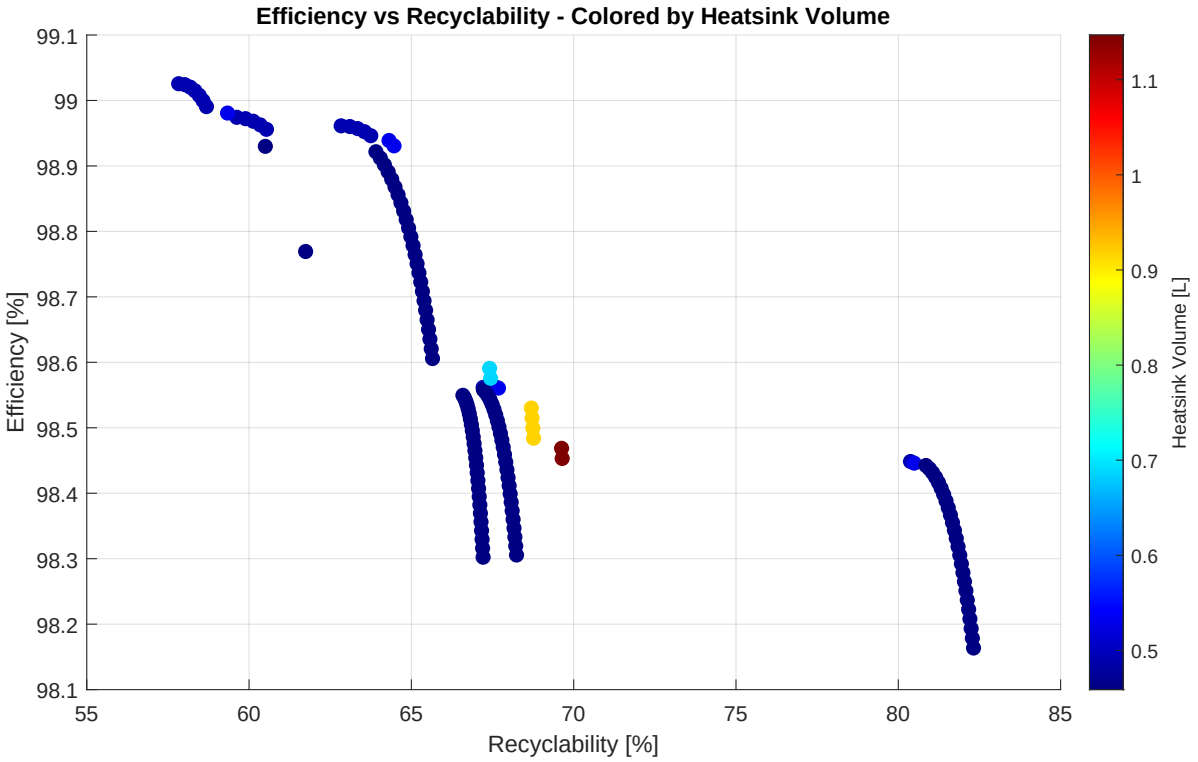


Figure E.6 2D plot of the Pareto optimal solutions showing efficiency and recyclability colored by the heatsink volume.

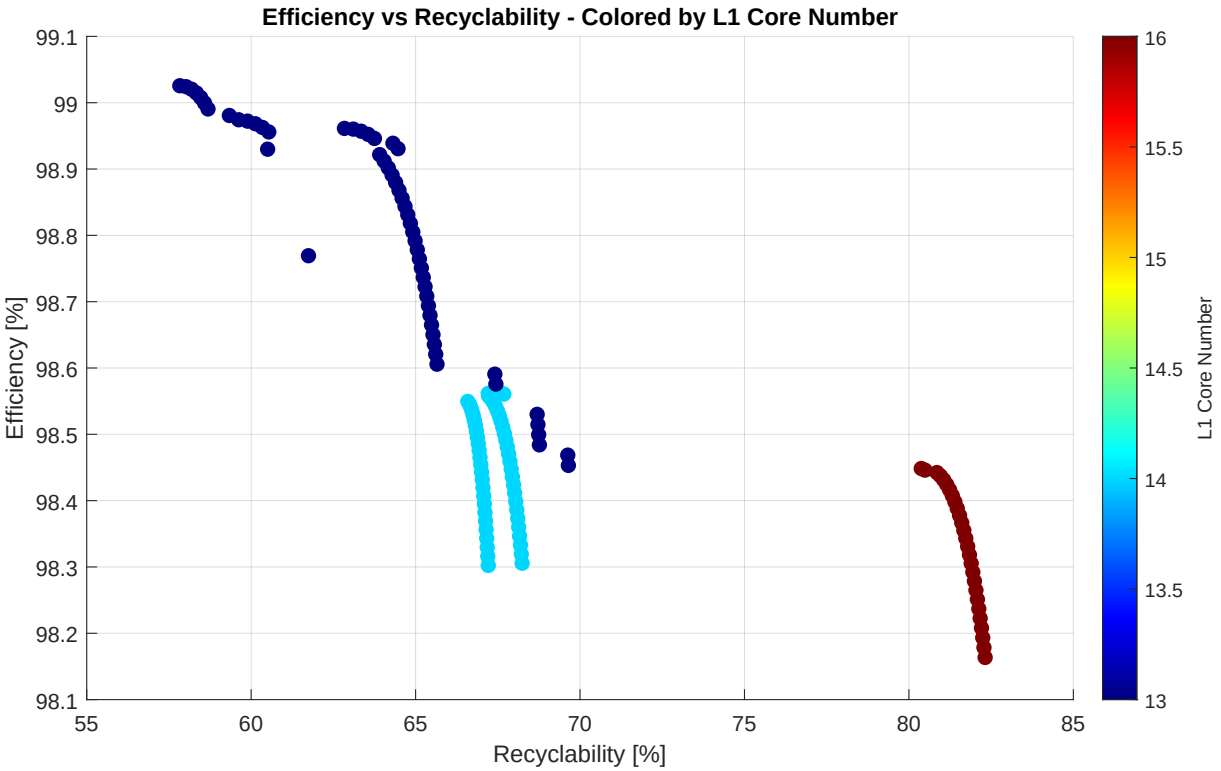


Figure E.7 2D plot of the Pareto optimal solutions showing efficiency and recyclability colored by entry of the core used for L1.

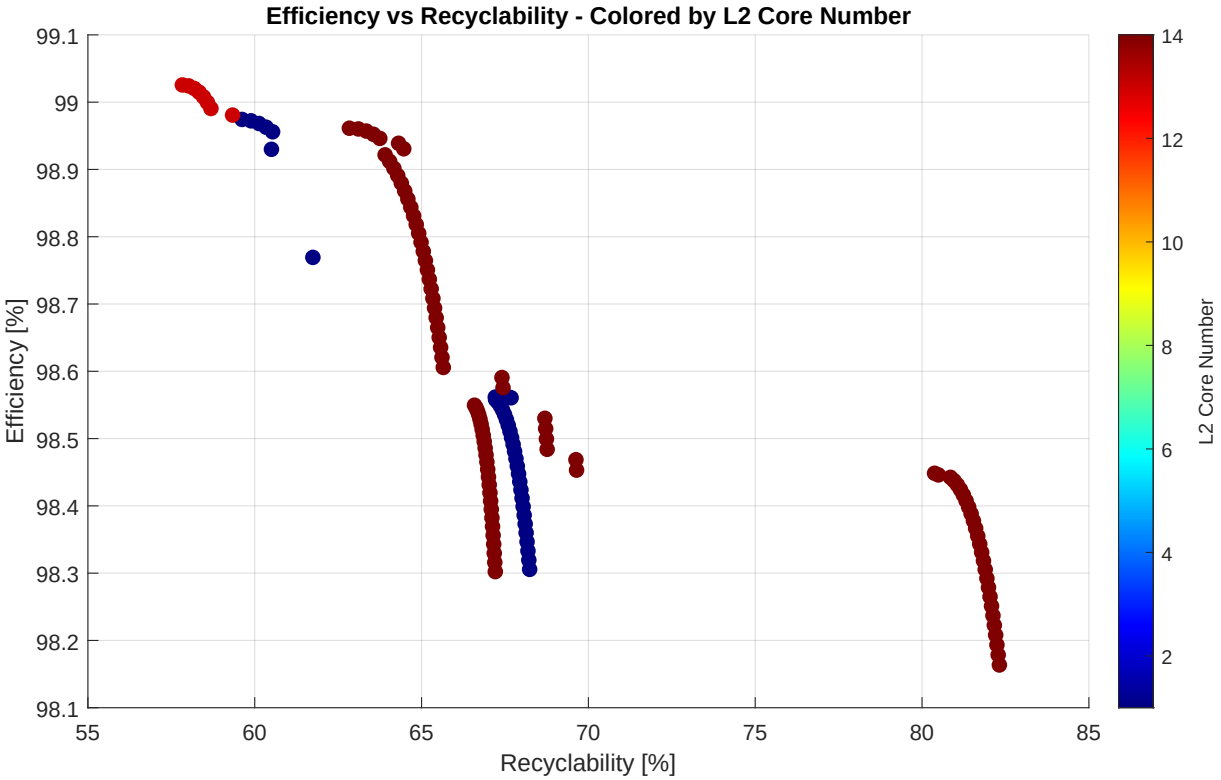


Figure E.8 2D plot of the Pareto optimal solutions showing efficiency and recyclability colored by entry of the core used for L2.

E.3 Power Density vs Recyclability

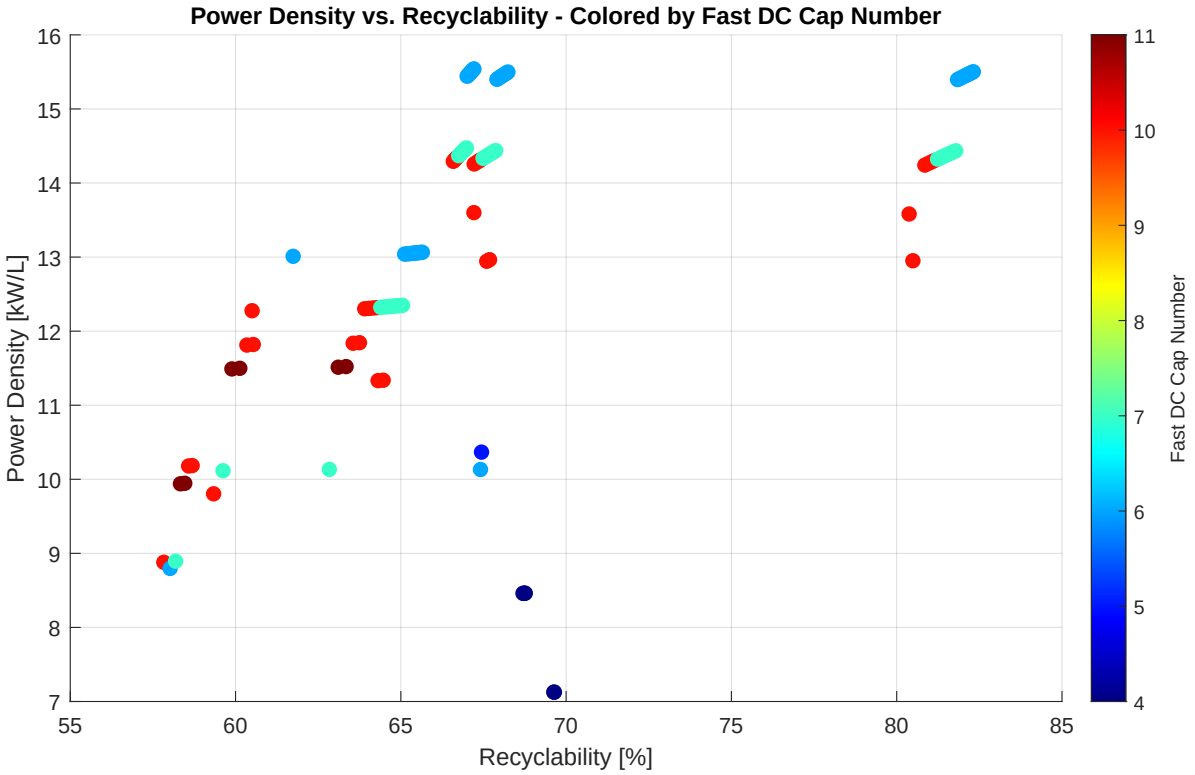


Figure E.9 2D plot of the Pareto optimal solutions showing power density and recyclability colored by the fast DC capacitor database entry.

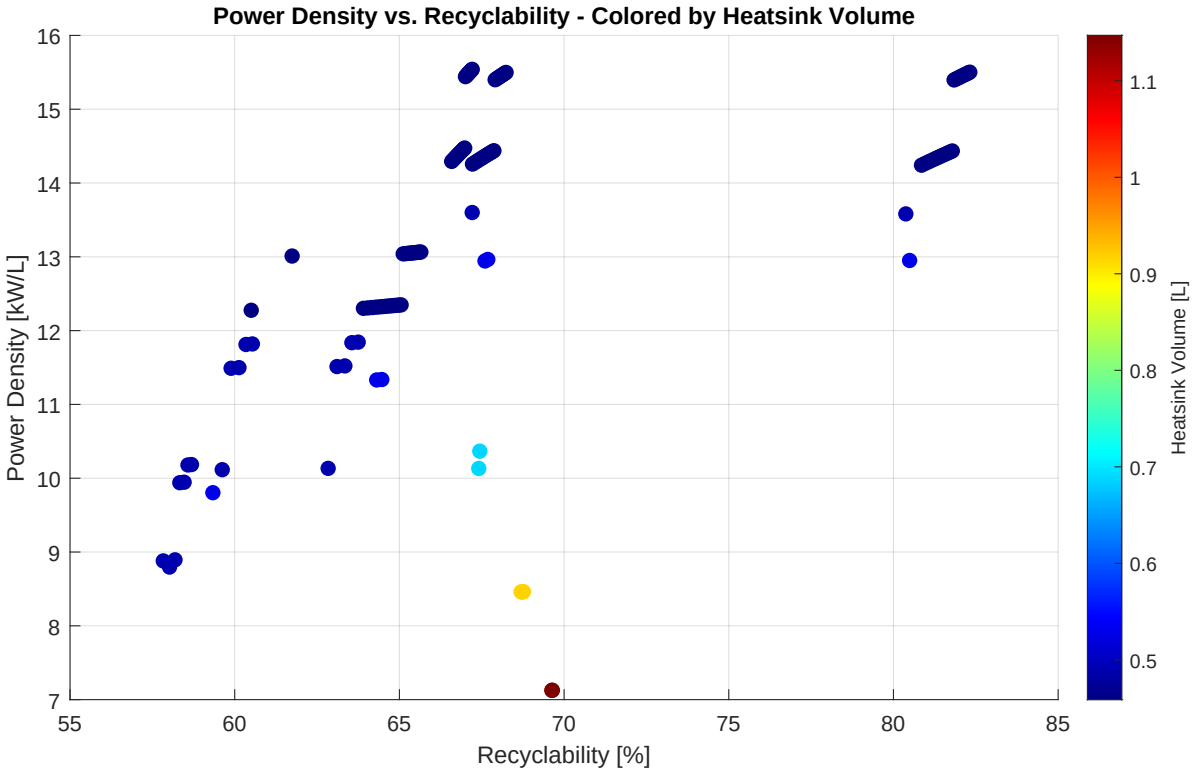


Figure E.10 2D plot of the Pareto optimal solutions showing power density and recyclability colored by the heatsink volume.

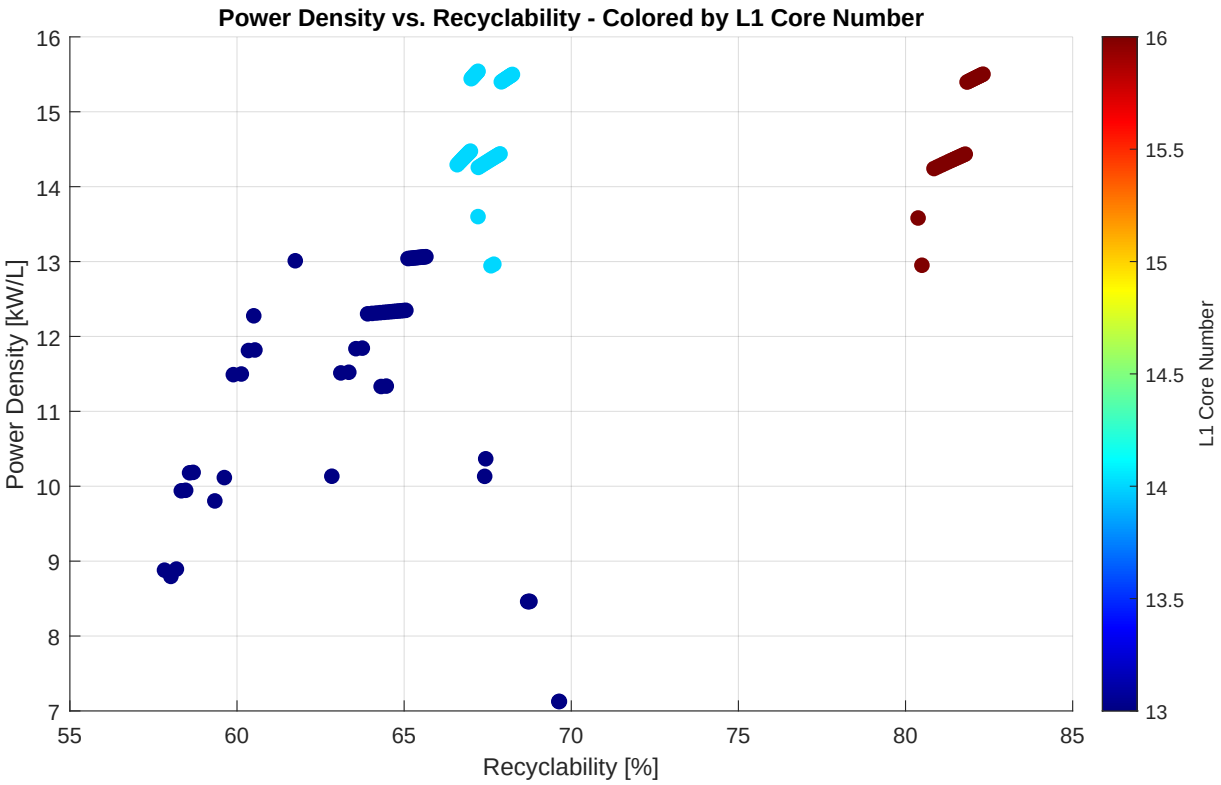


Figure E.11 2D plot of the Pareto optimal solutions showing power density and recyclability colored by entry of the core used for L1.

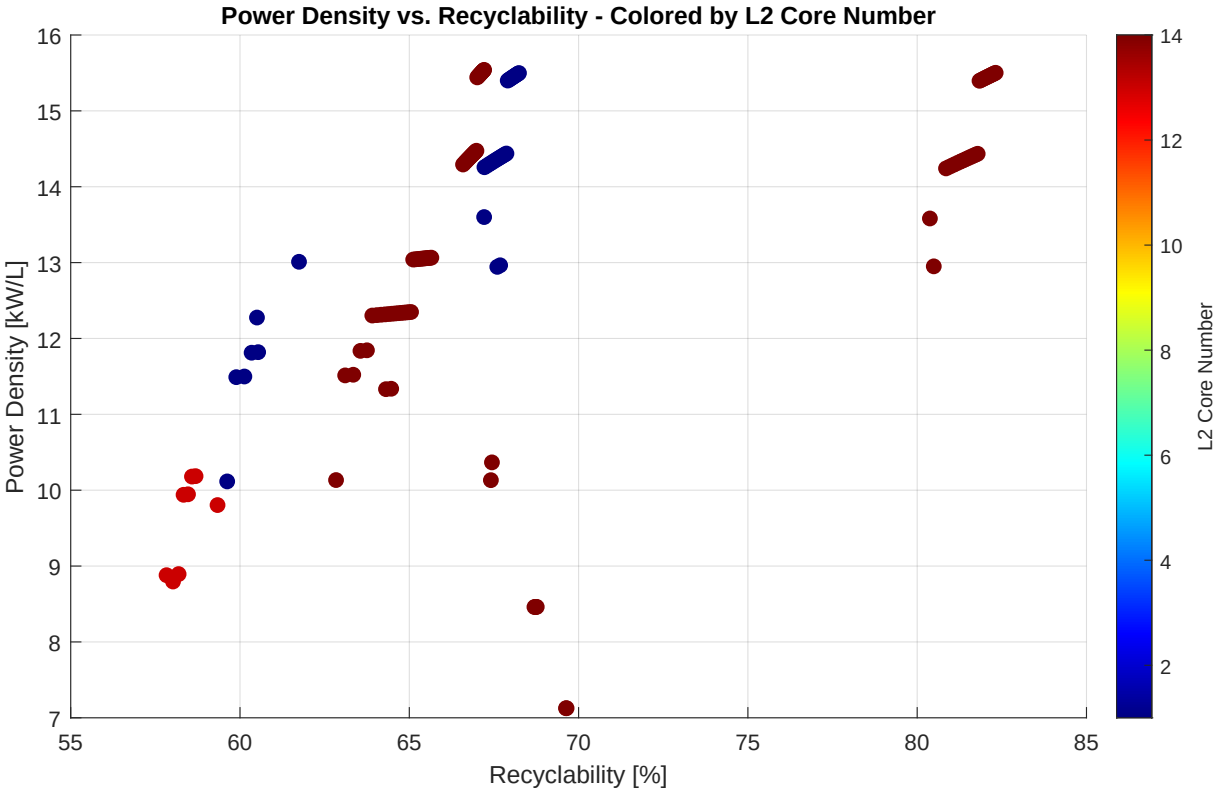
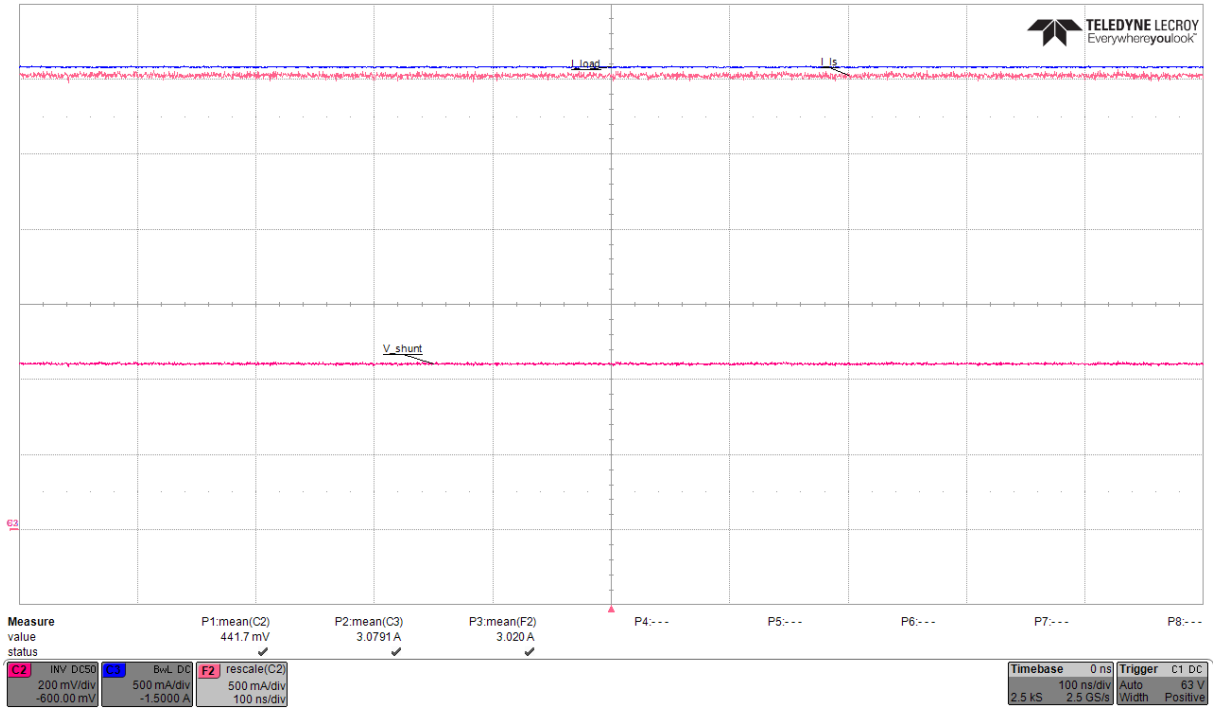
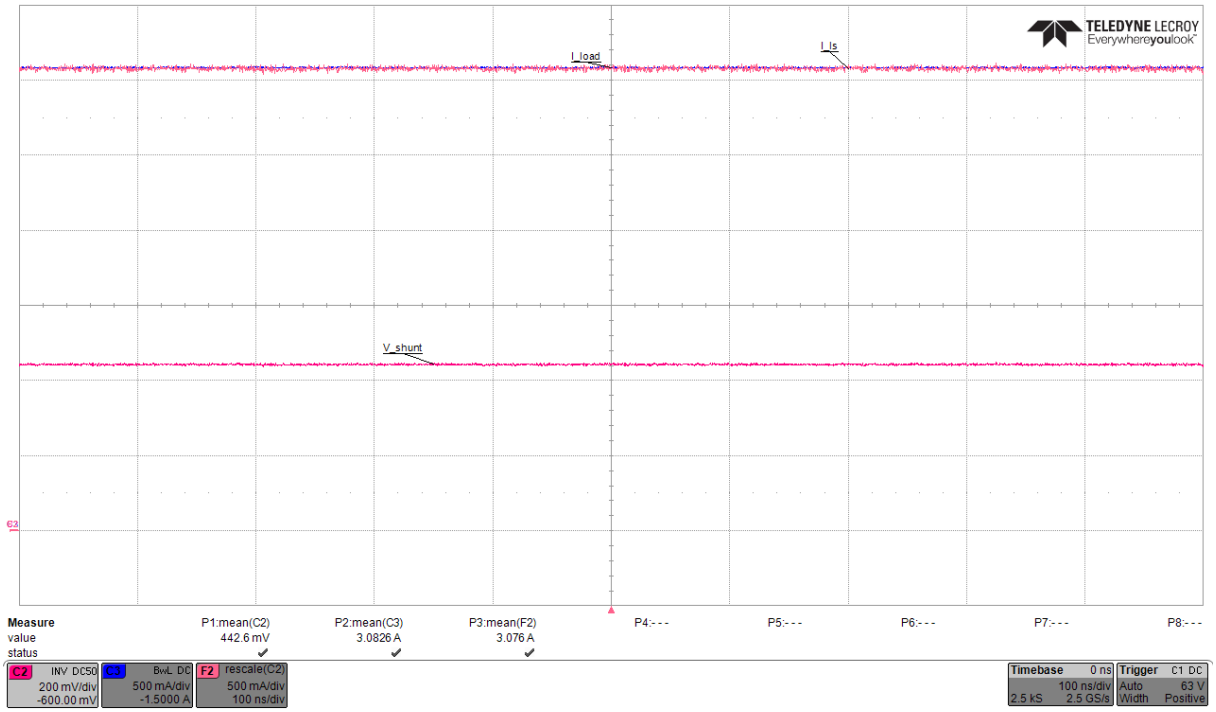


Figure E.12 2D plot of the Pareto optimal solutions showing power density and recyclability colored by entry of the core used for L2.

F Shunt Calibration



(a)



(b)

Figure F.1 DUT current measured by resistive shunt (F2) and current probe (C3): a) Gain of 6.85 S b) Gain 6.95 S

G Specimen after Three-Point-Bending Test

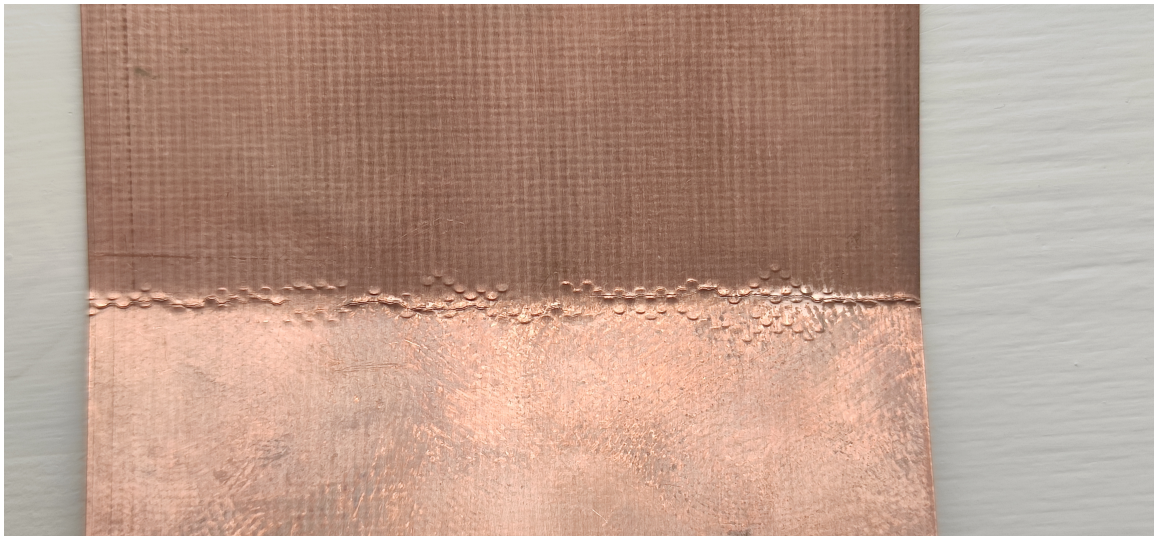


Figure G.1 Top side of the mechanical test specimen "Conv" after the three-point-bending test.

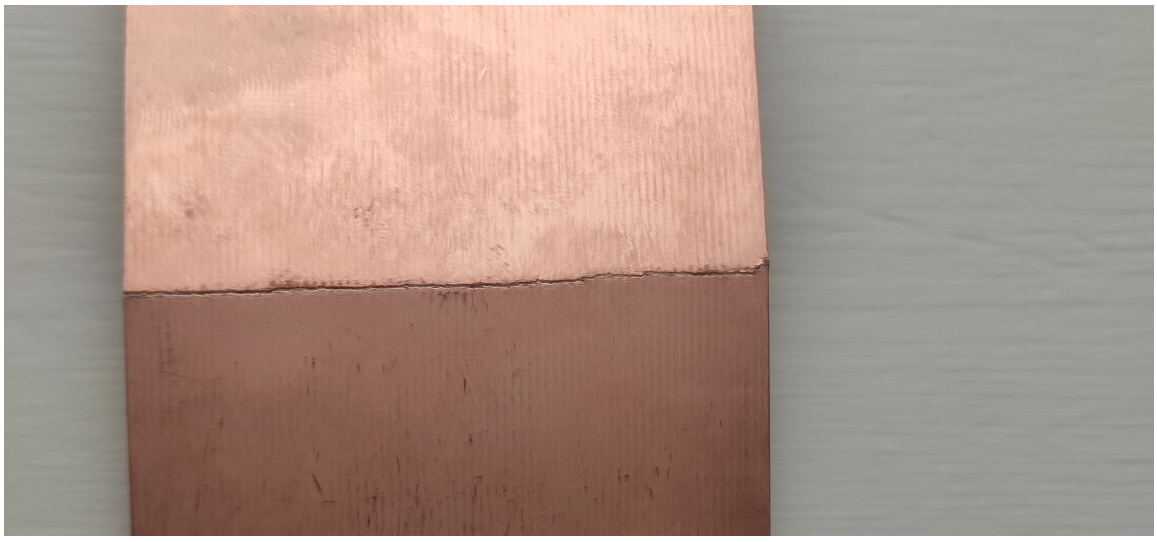


Figure G.2 Bottom side of the mechanical test specimen "Conv" after the three-point-bending test.

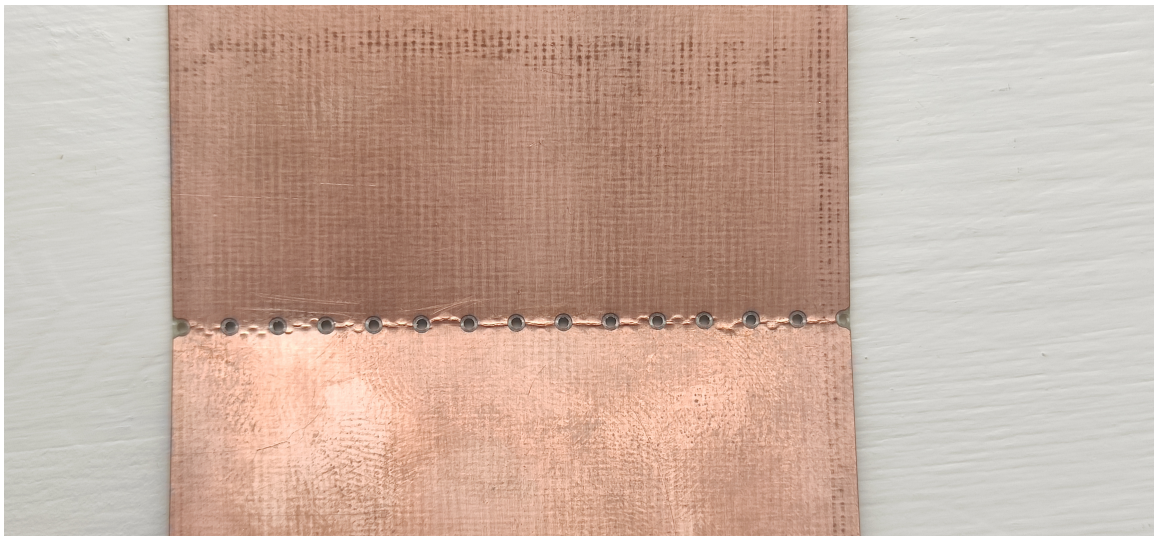


Figure G.3 Top side of the mechanical test specimen "Eco1" after the three-point-bending test.

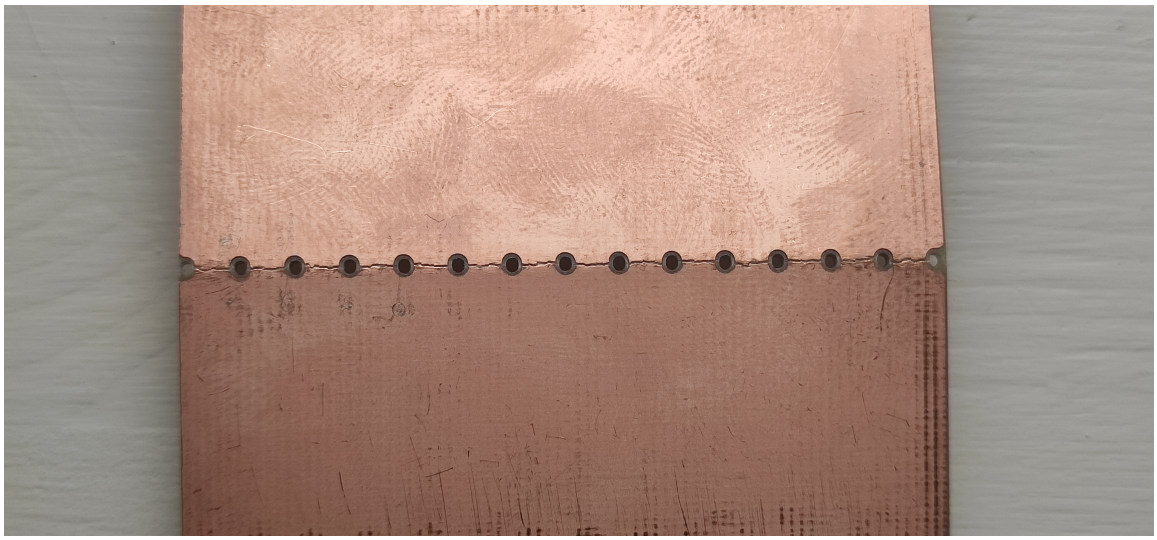


Figure G.4 Bottom side of the mechanical test specimen "Eco1" after the three-point-bending test.

Figure G.5 Top side of the mechanical test specimen "Eco2" after the three-point-bending test.

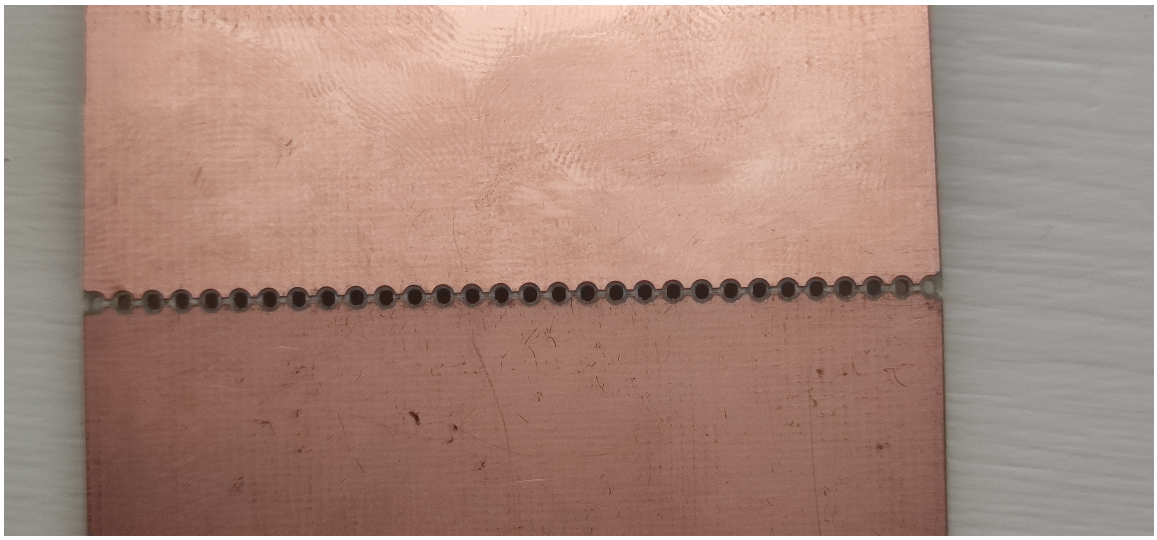


Figure G.6 Bottom side of the mechanical test specimen "Eco2" after the three-point-bending test.

Figure G.7 Top side of the mechanical test specimen "Eco3" after the three-point-bending test.

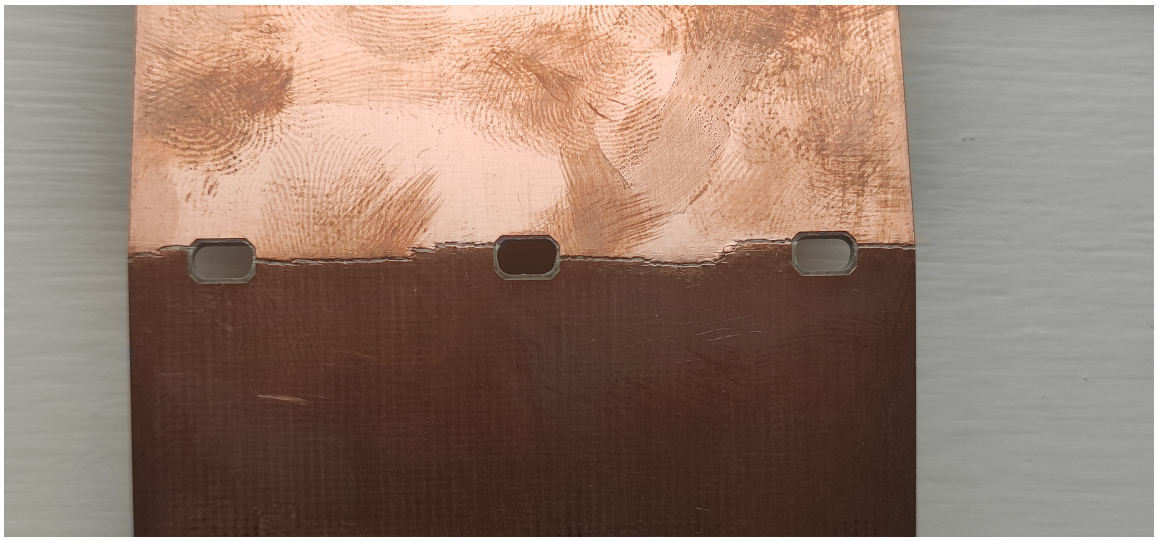


Figure G.8 Bottom side of the mechanical test specimen "Eco3" after the three-point-bending test.

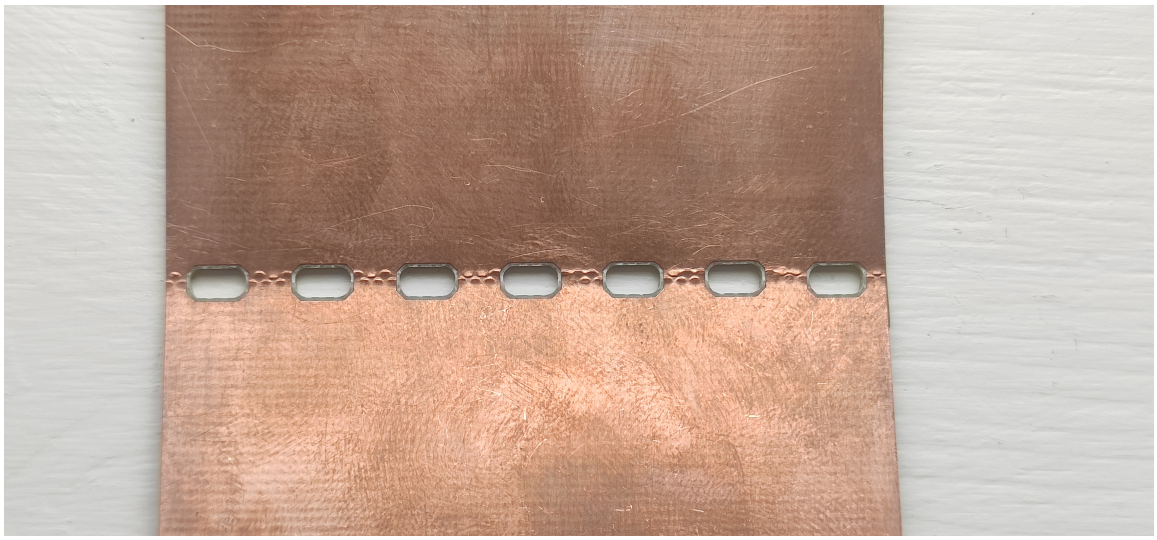


Figure G.9 Top side of the mechanical test specimen "Eco4" after the three-point-bending test.

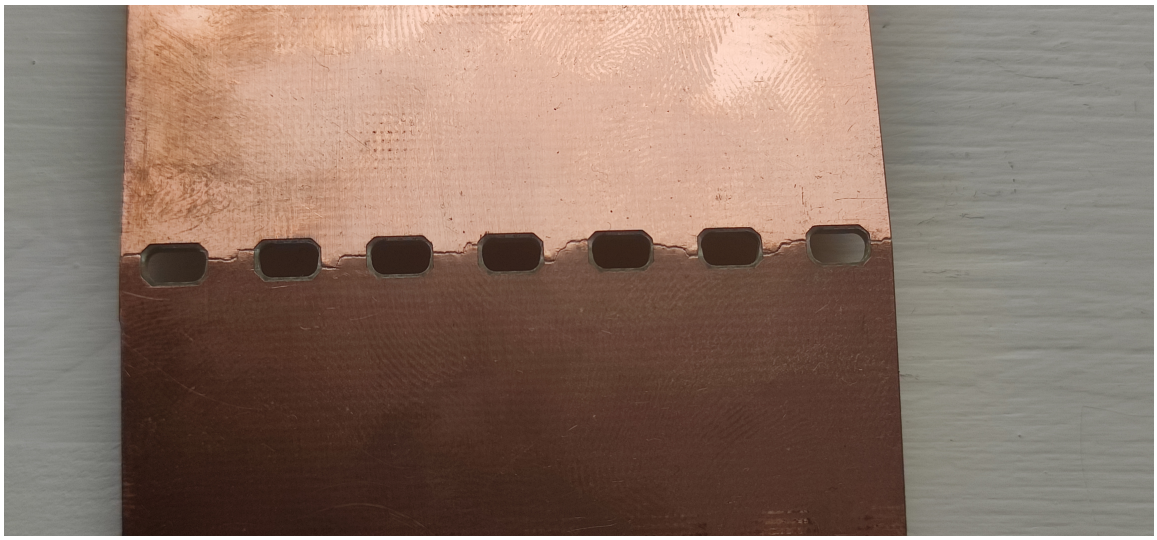


Figure G.10 Bottom side of the mechanical test specimen "Eco4" after the three-point-bending test.

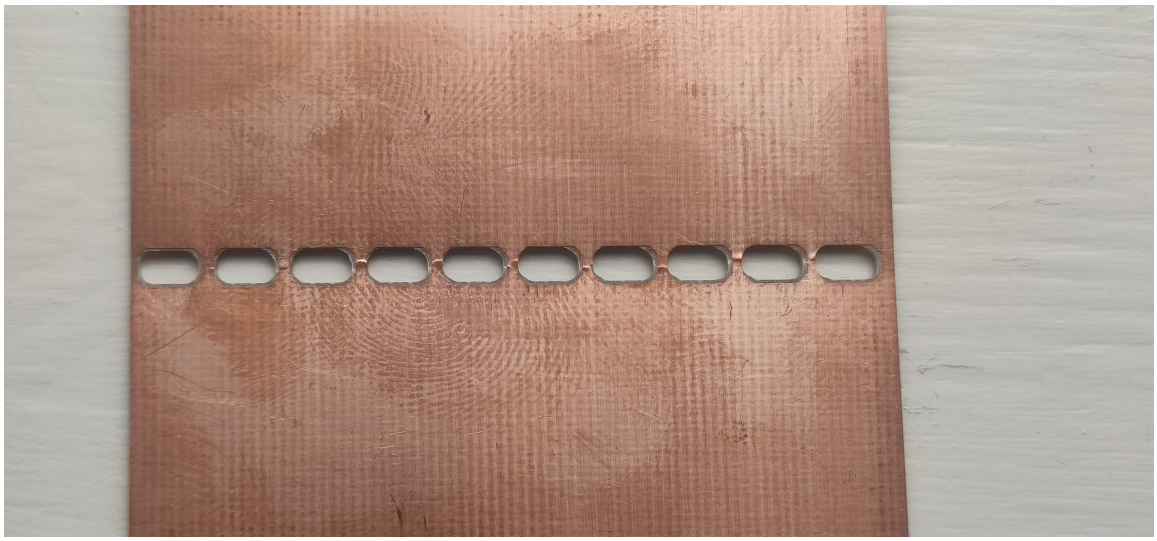


Figure G.11 Top side of the mechanical test specimen "Eco5" after the three-point-bending test.

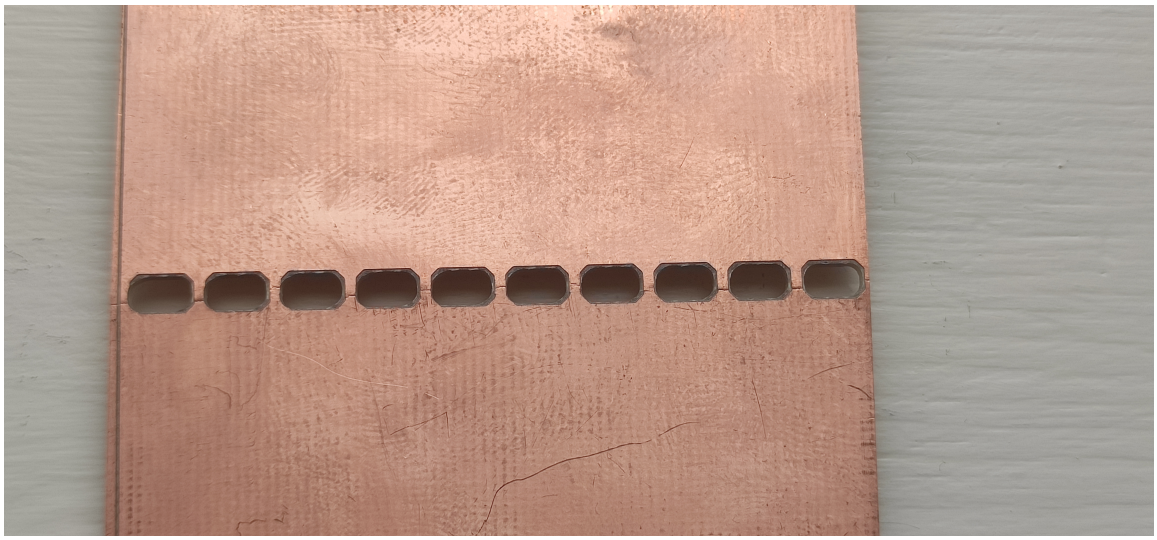


Figure G.12 Bottom side of the mechanical test specimen "Eco5" after the three-point-bending test.

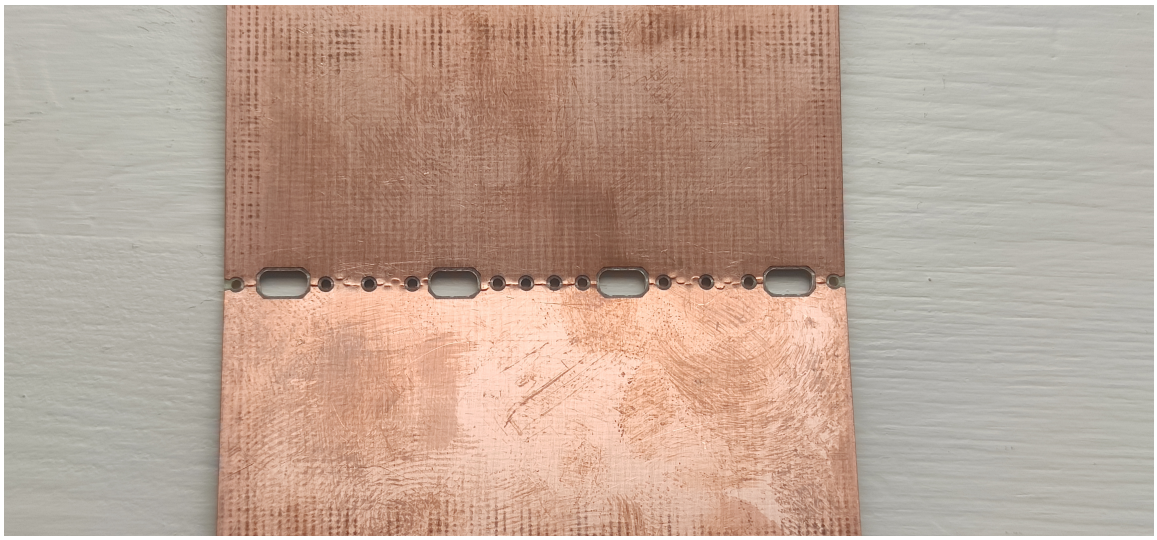


Figure G.13 Top side of the mechanical test specimen "EcoSH" after the three-point-bending test.

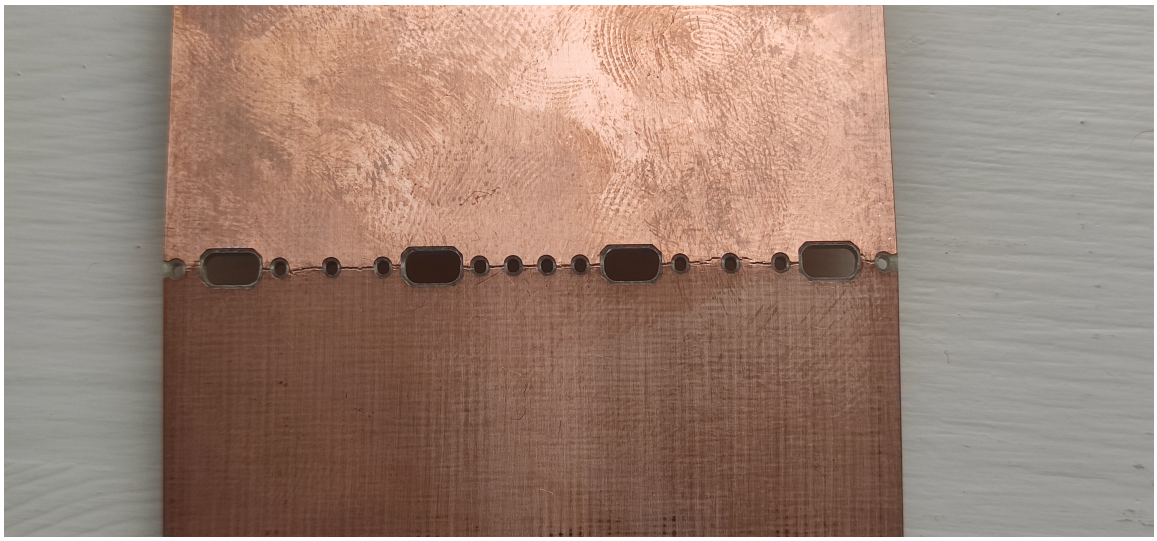


Figure G.14 Bottom side of the mechanical test specimen "EcoSH" after the three-point-bending test.

H PCB Layout Configurations

H.1 Mechanical Specimens

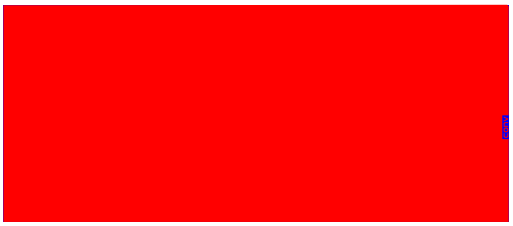


Figure H.1 Layout of the boards for mechanical testing without perforations.

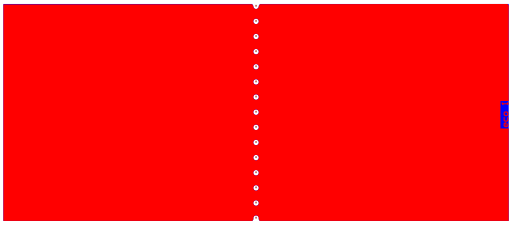


Figure H.2 Layout of the boards for mechanical testing with 25 % perforation holes-based approach.

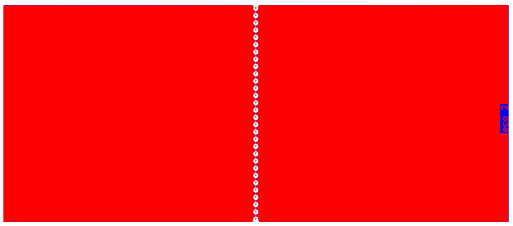


Figure H.3 Layout of the boards for mechanical testing with 50 % perforation holes-based approach.

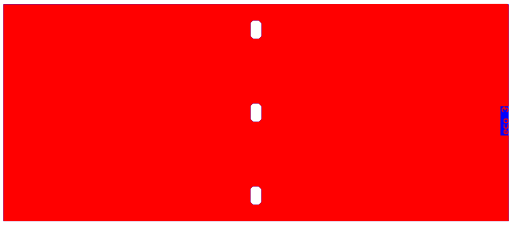


Figure H.4 Layout of the boards for mechanical testing with 25 % perforation slot-based approach.

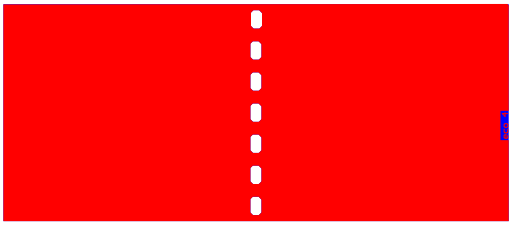


Figure H.5 Layout of the boards for mechanical testing with 50 % perforation holes-based approach.

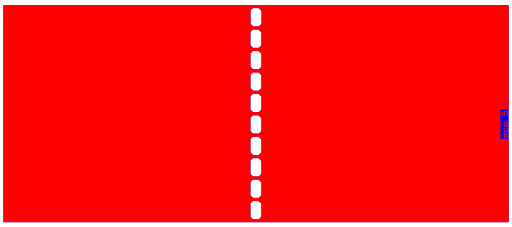


Figure H.6 Layout of the boards for mechanical testing with 75 % perforation slot-based approach.

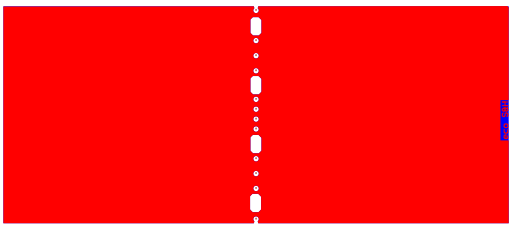


Figure H.7 Layout of the boards for mechanical testing with 50 % perforation and a combination of slot- and hole-based approach.

H.2 Conventional Design

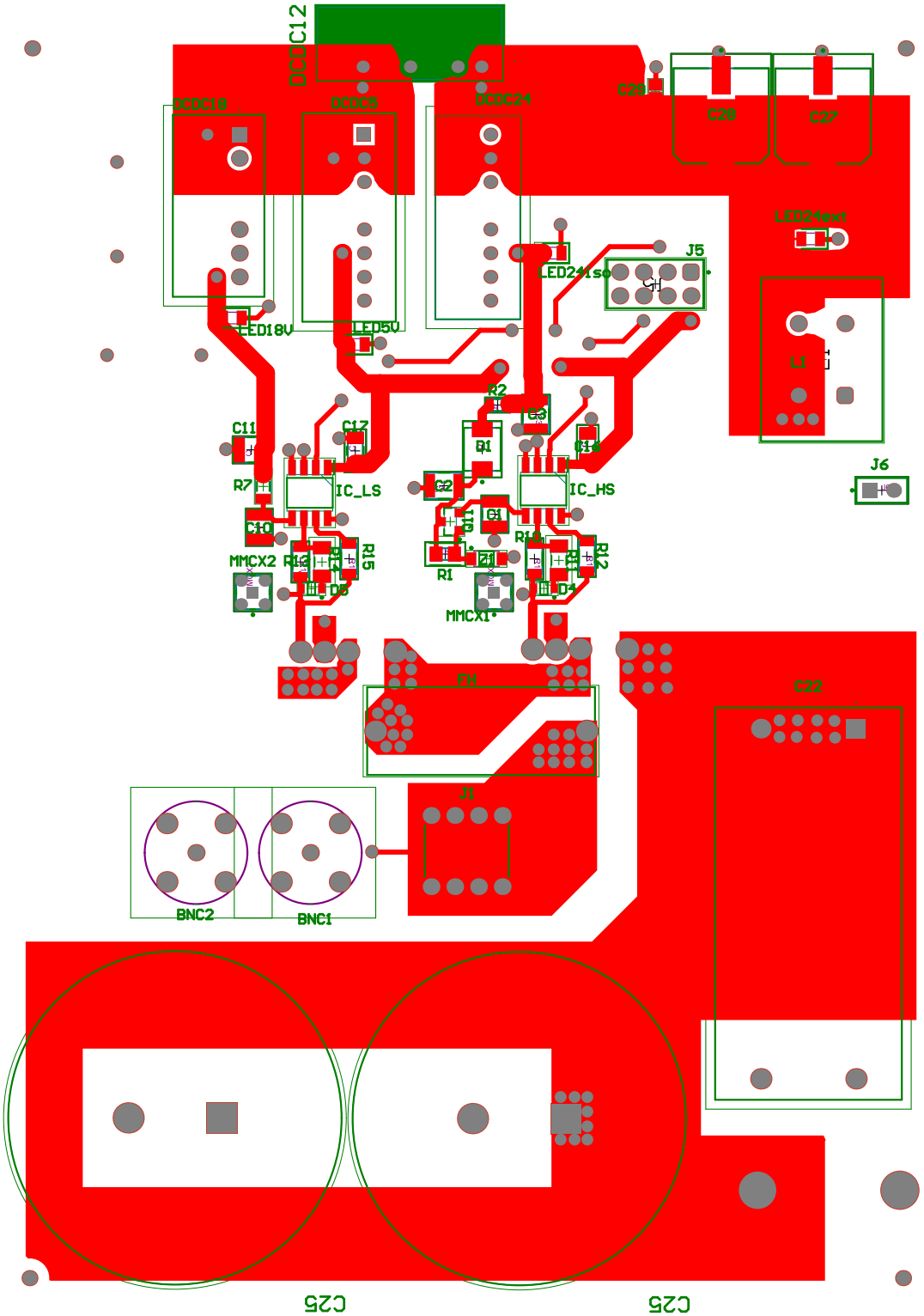


Figure H.8 PCB "Conv" without perforation top side. The board measures 105 mm by 142 mm.

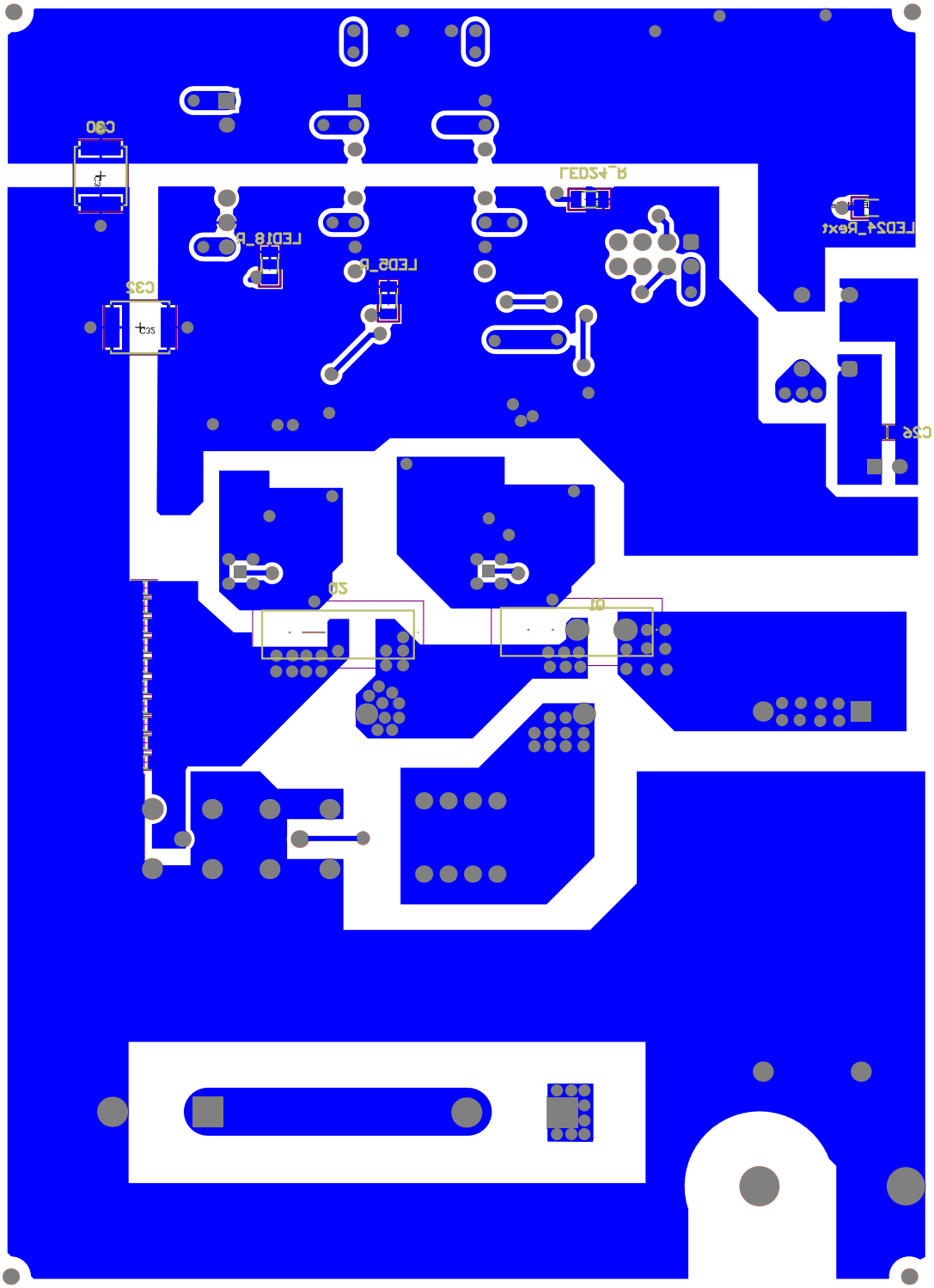


Figure H.9 PCB "Conv" without perforation bottom side. The board measures 105 mm by 142 mm.

H.3 Eco1 Design

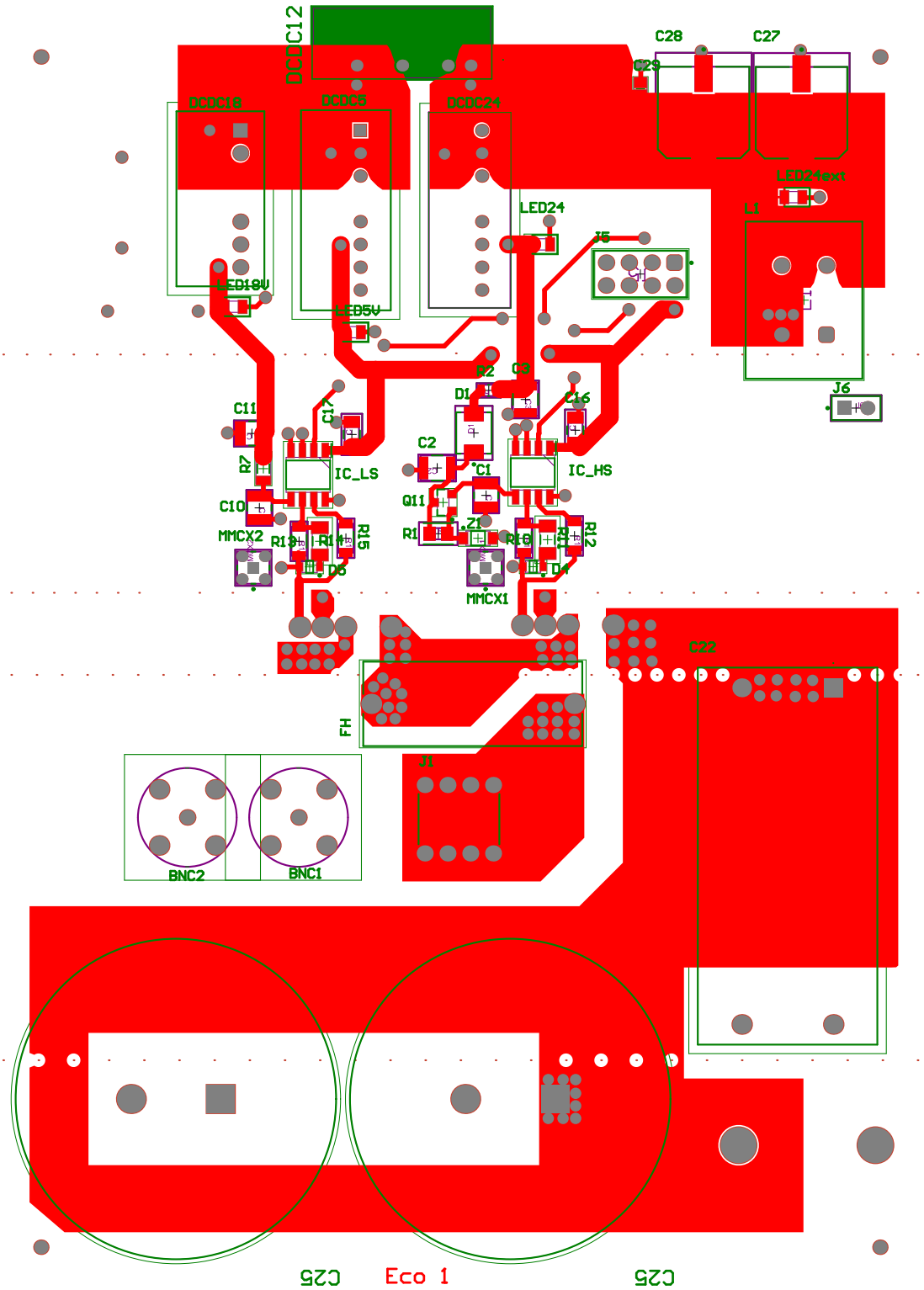


Figure H.10 PCB "Eco1" with a 25% hole-based perforation strategy, top side.

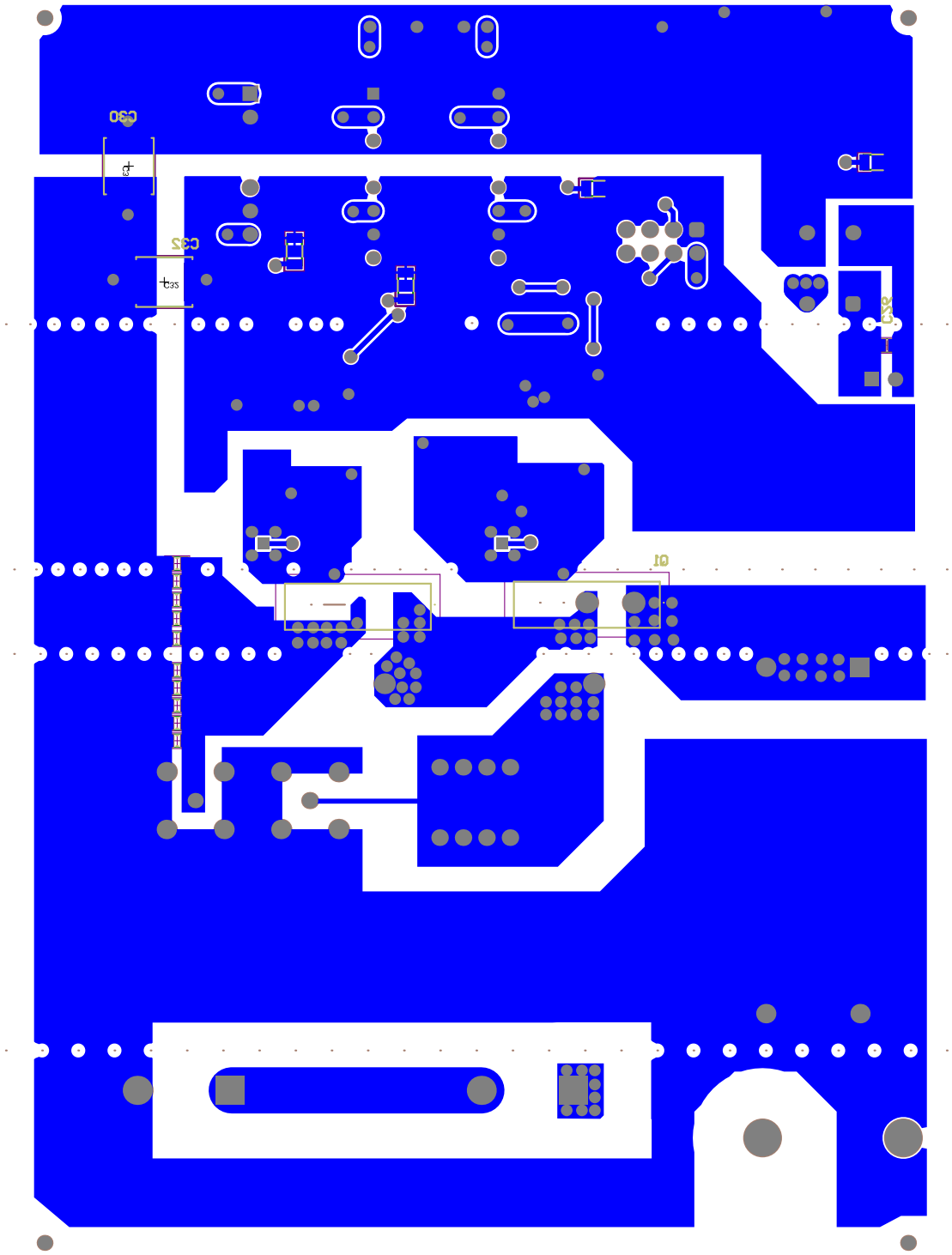


Figure H.11 PCB "Eco1" with a 25% hole-based perforation strategy, bottom side.

H.4 Eco2 Design

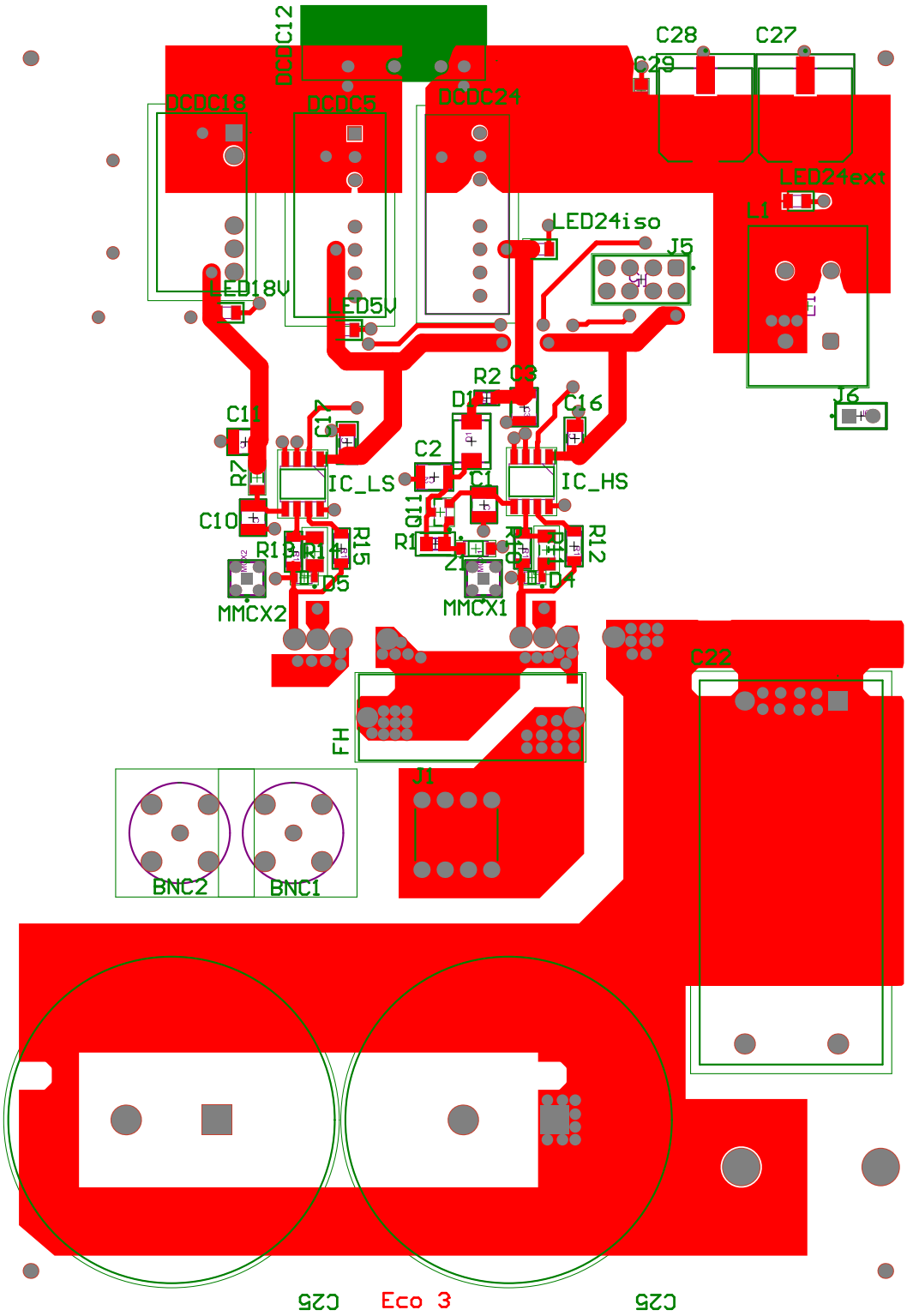


Figure H.12 PCB "Eco2" with a 50% hole-based perforation strategy, top side.

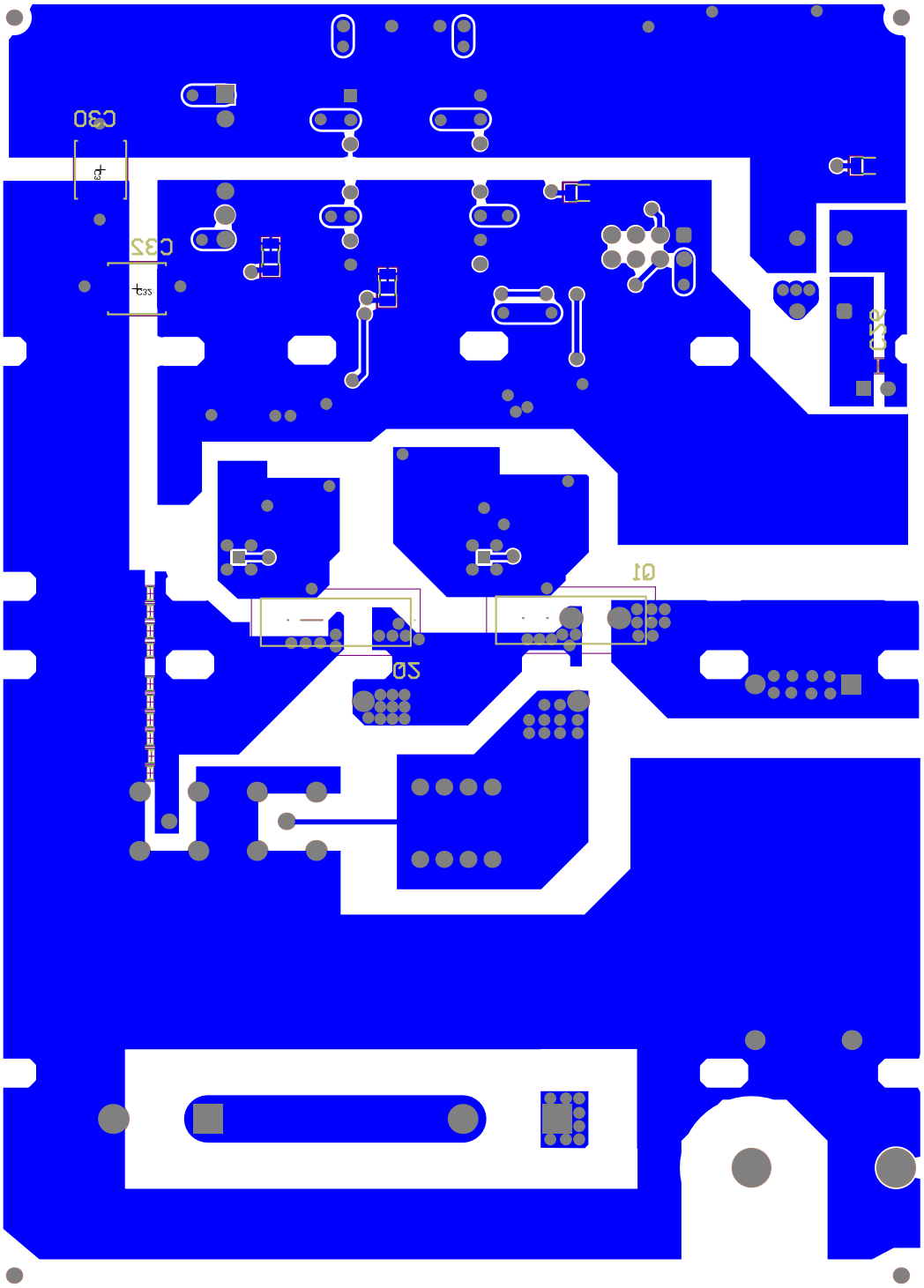


Figure H.13 PCB "Eco2" with a 50% hole-based perforation strategy, bottom side.

H.5 Eco3 Design

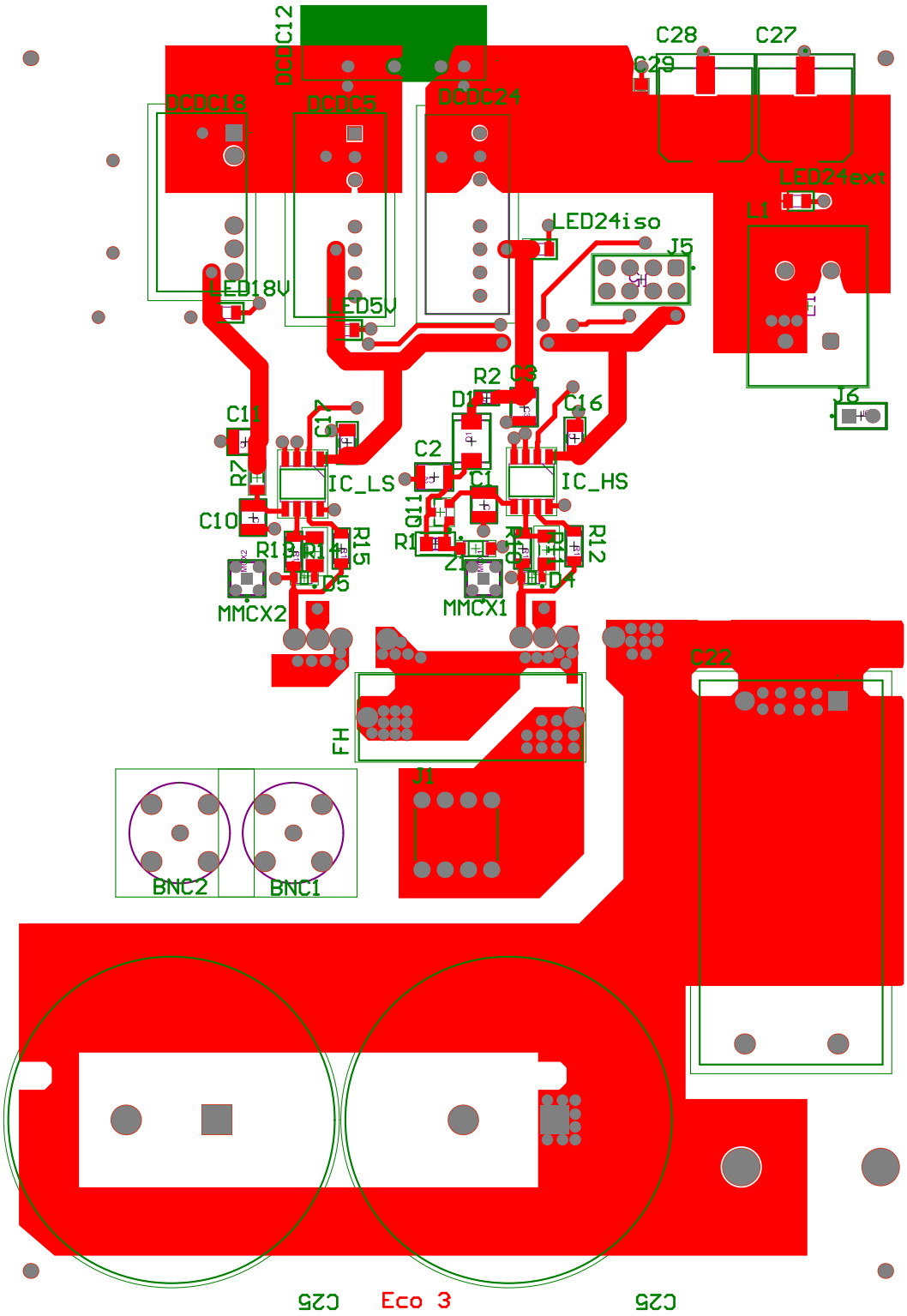


Figure H.14 PCB "Eco3" with a 25% slot-based perforation strategy, top side.

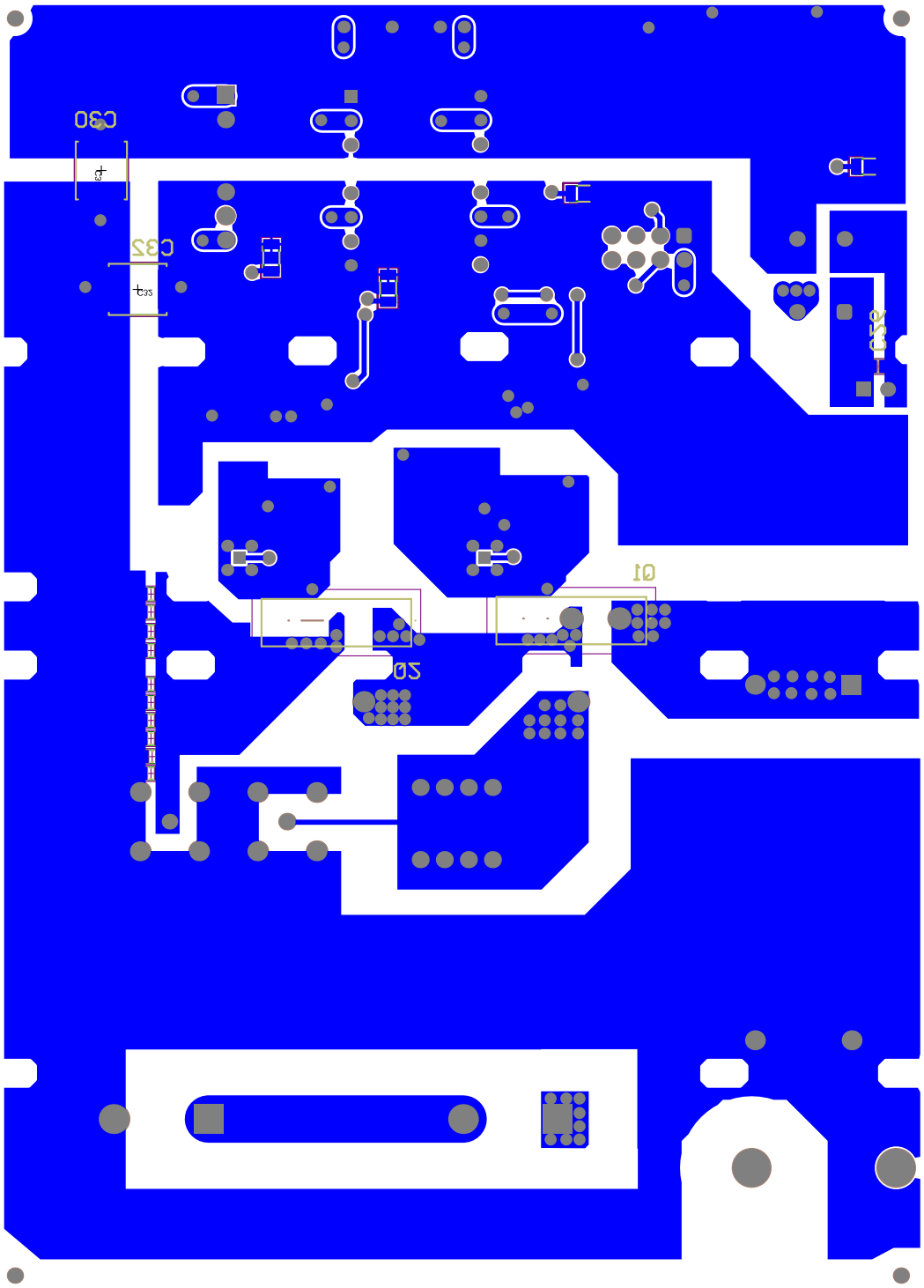


Figure H.15 PCB "Eco3" with a 25% slot-based perforation strategy, bottom side.

H.6 Eco4 Design

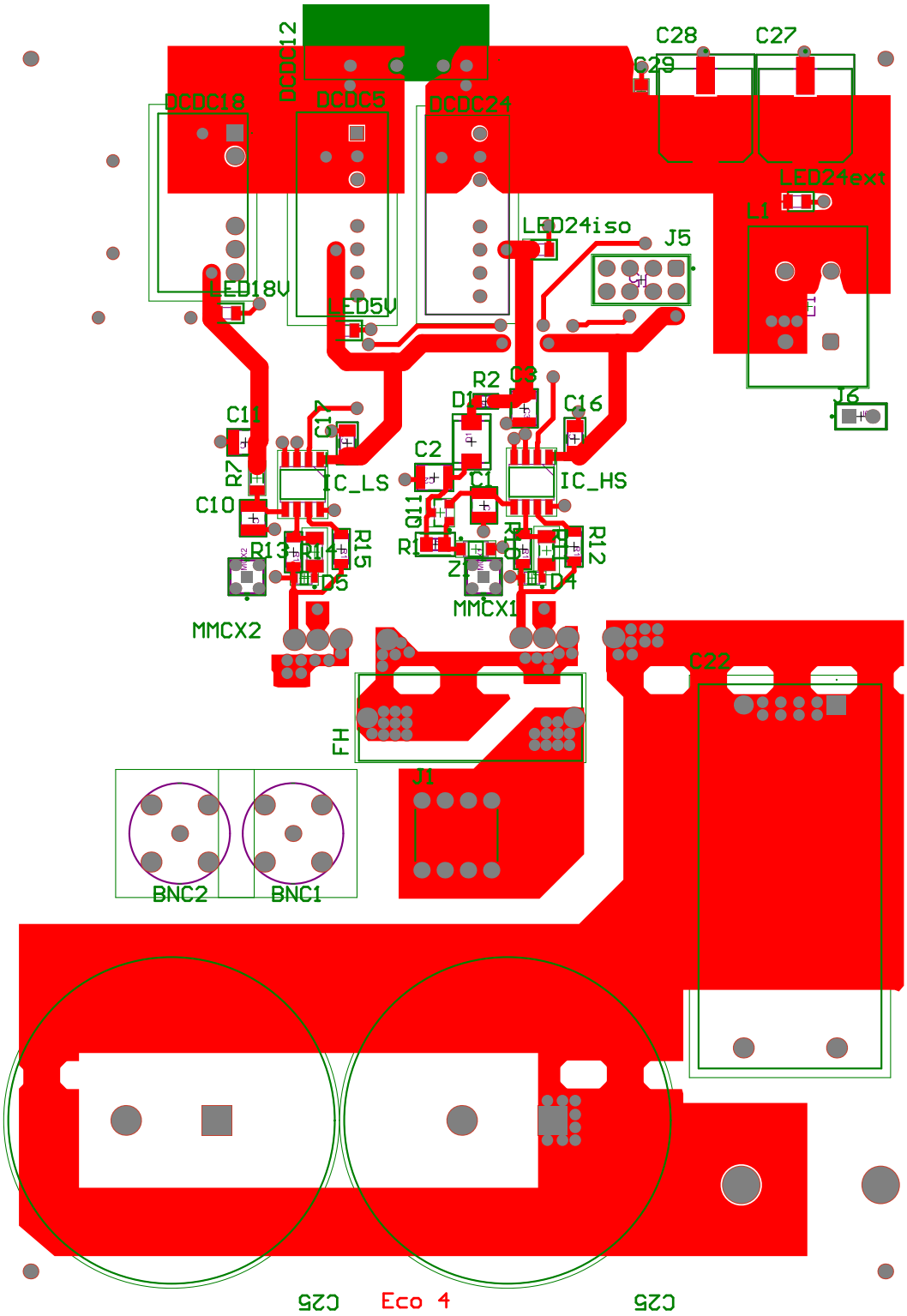


Figure H.16 PCB "Eco4" with a 50% slot-based perforation strategy, top side.

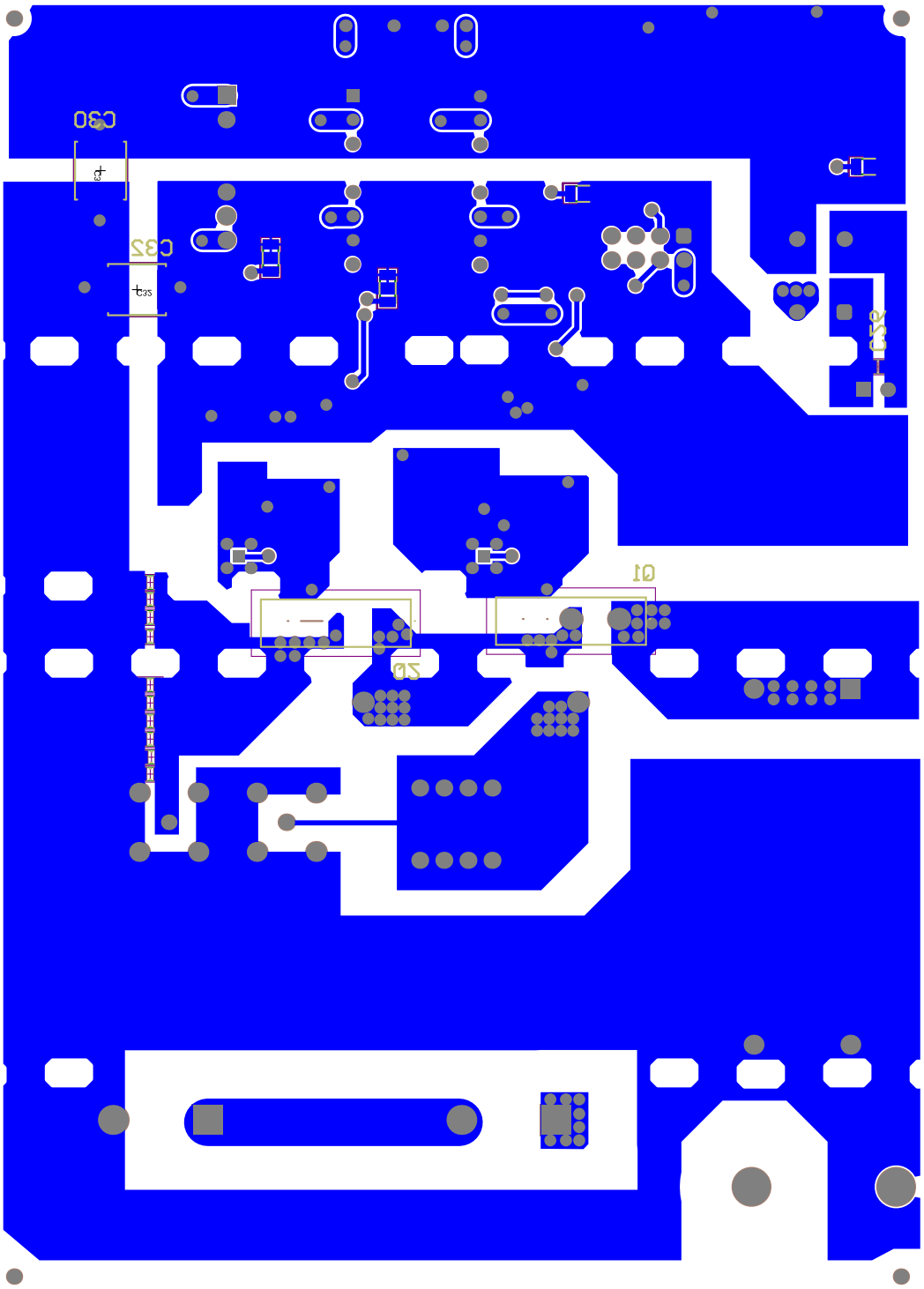


Figure H.17 PCB "Eco4" with a 50% slot-based perforation strategy, bottom side.

H.7 Eco5 Design

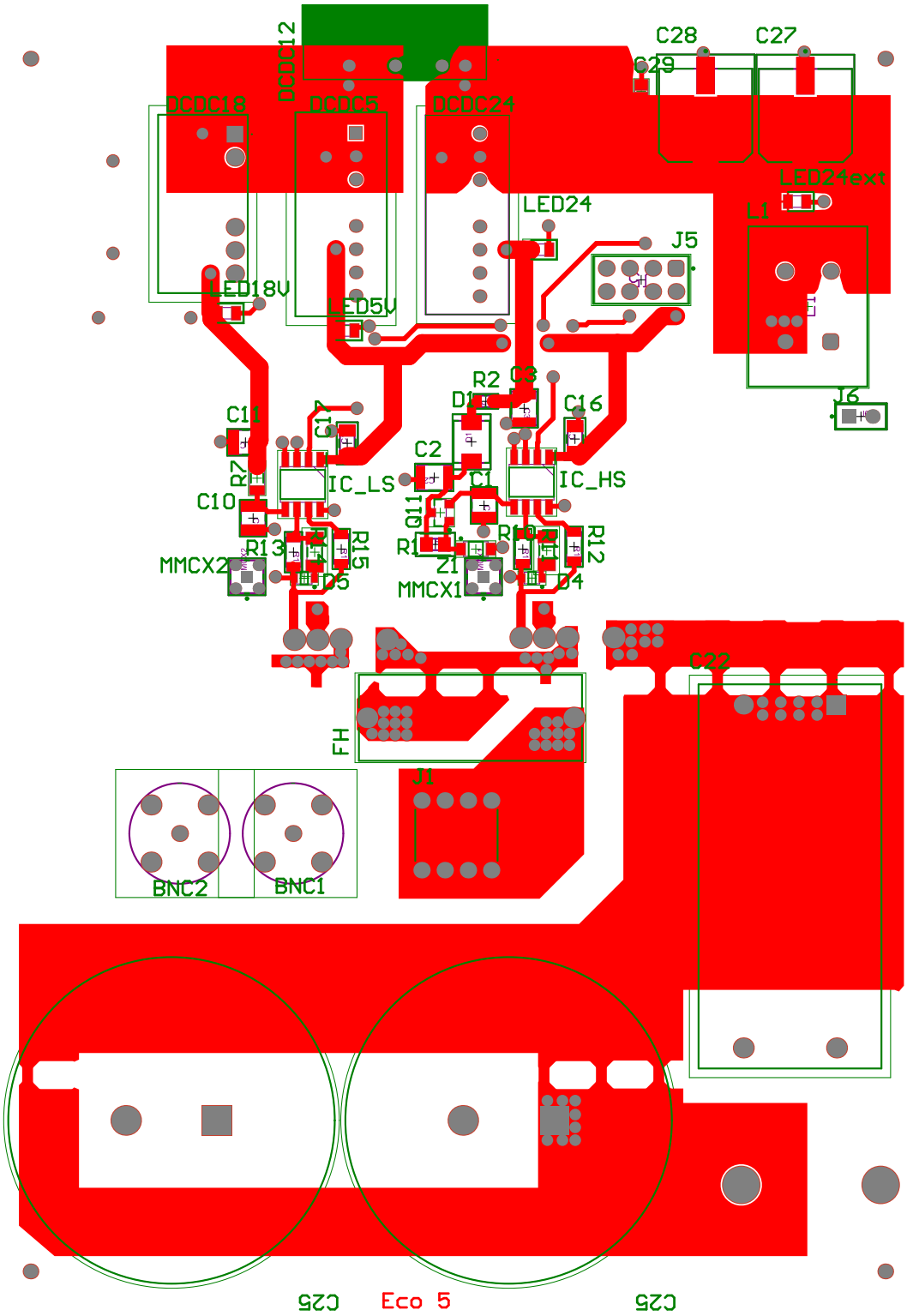


Figure H.18 PCB "Eco5" with a 75% slot-based perforation strategy, top side.

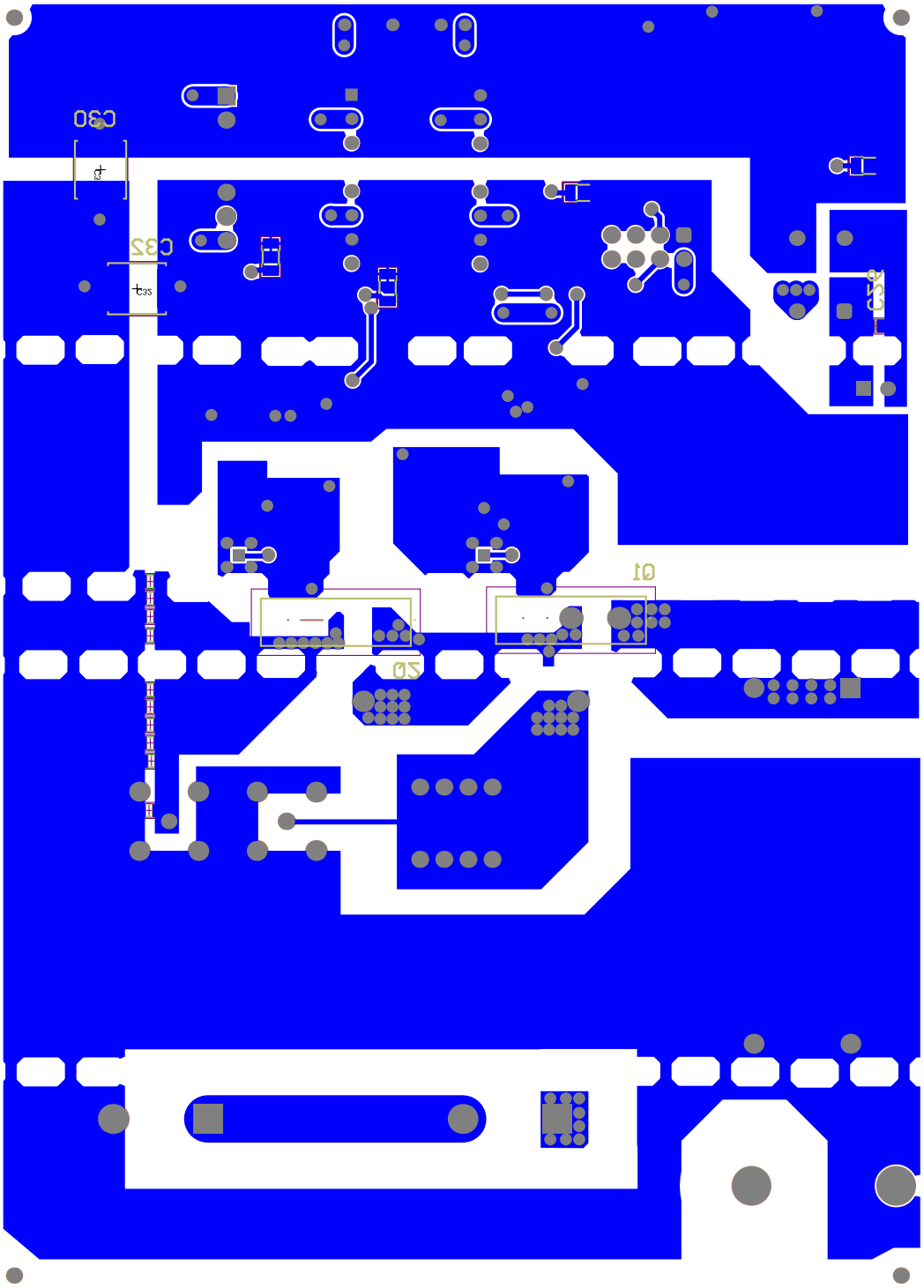


Figure H.19 PCB "Eco5" with a 75% slot-based perforation strategy bottom side.

H.8 EcoSH Design

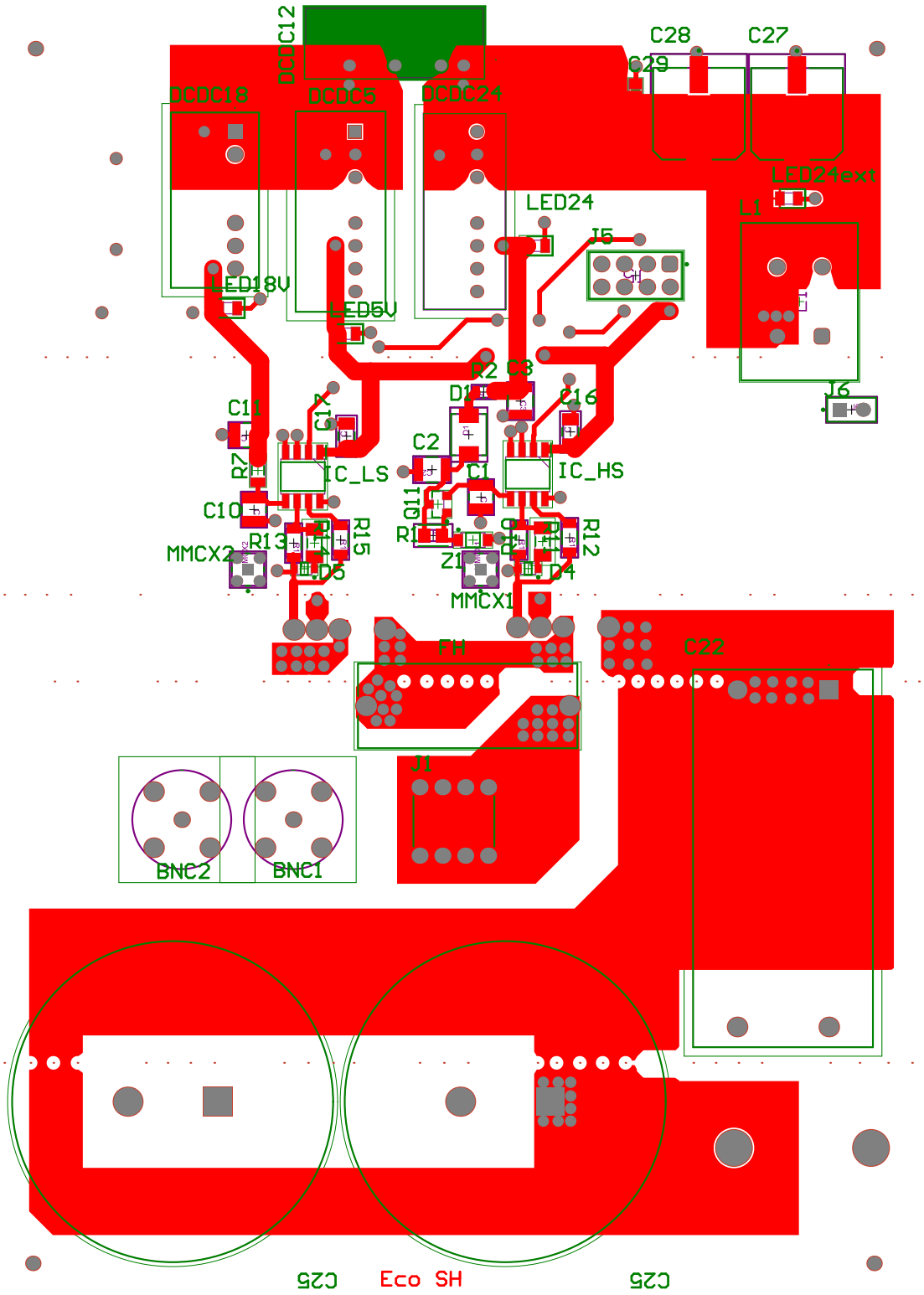


Figure H.20 PCB "EcoSH" with a 50% combined hole and slot-based perforation strategy, top side.

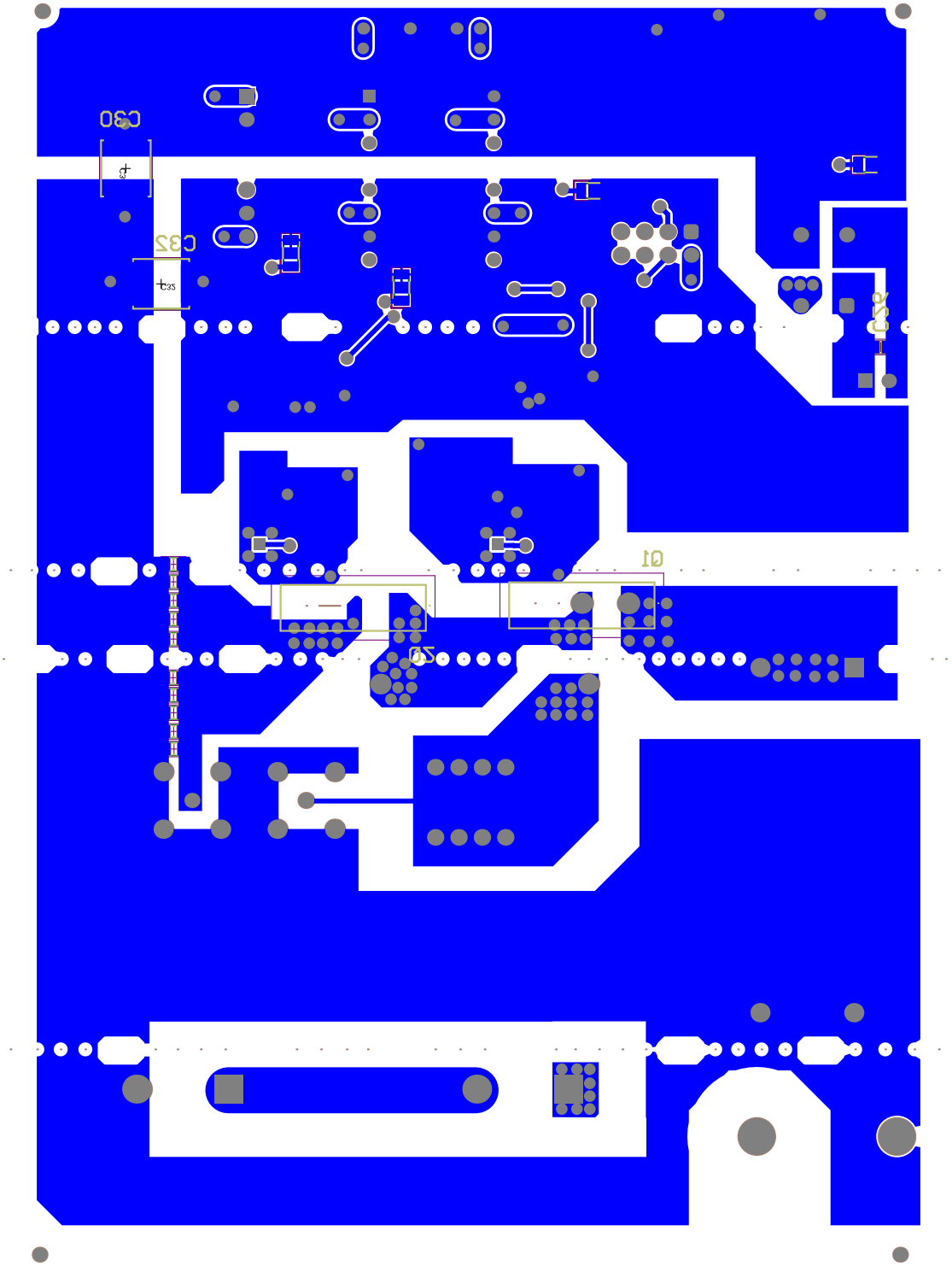
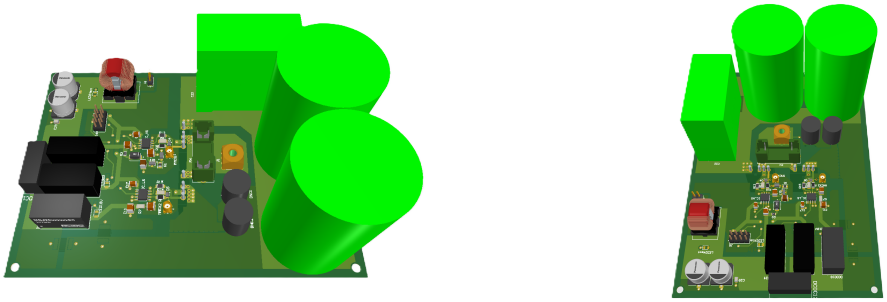


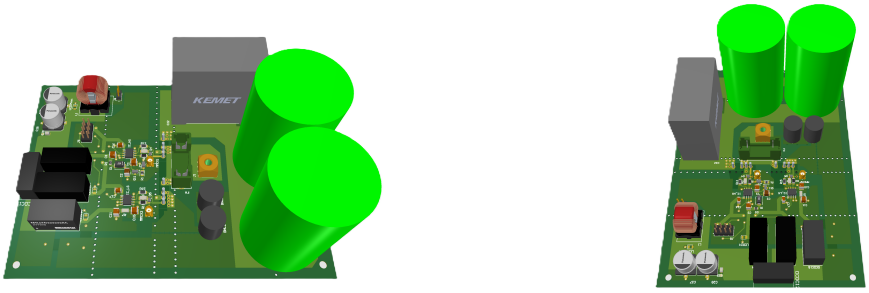
Figure H.21 PCB "EcoSH" with a 50% combined hole and slot-based perforation strategy, bottom side.

H.9 Three-Dimensional Illustration



(a) **(b)**

Figure H.22 A three-dimensional illustration of the conventionally designed half-bridge converter PCB without perforation (Conv).

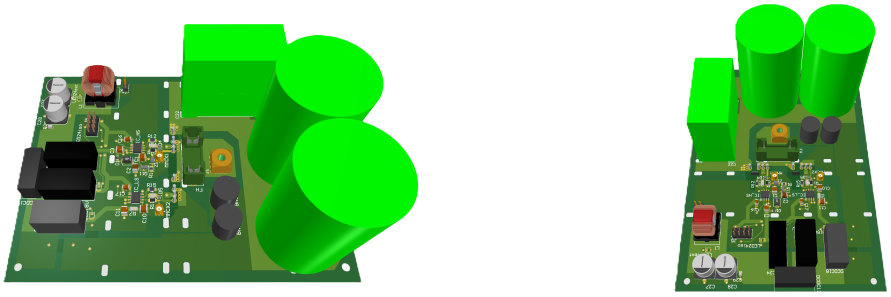


(a) **(b)**

Figure H.23 A three-dimensional illustration of the hole-based designed half-bridge converter PCB with 25% perforation (Eco1).

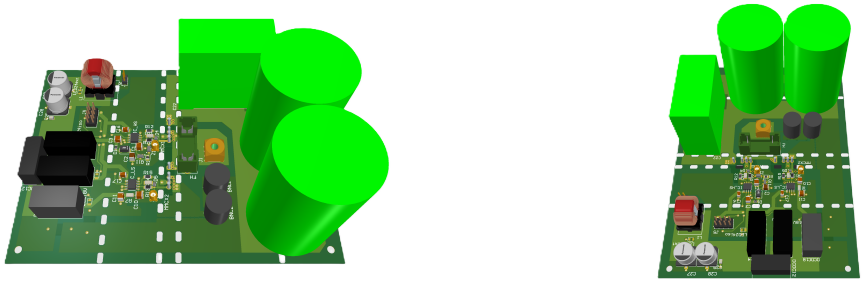
(a) **(b)**

Figure H.24 A three-dimensional illustration of the hole-based designed half-bridge converter PCB with 50% perforation (Eco2).



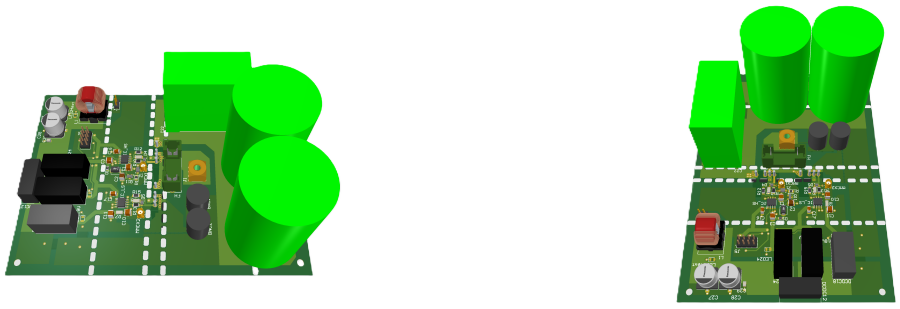
(a) **(b)**

Figure H.25 A three-dimensional illustration of the slot-based designed half-bridge converter PCB with 25% perforation (Eco3).



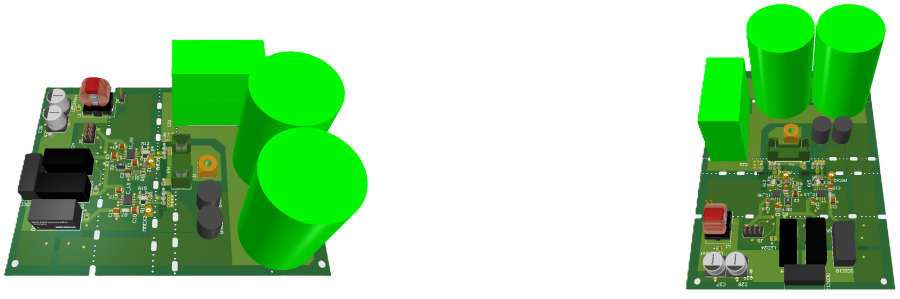
(a) **(b)**

Figure H.26 A three-dimensional illustration of the slot-based designed half-bridge converter PCB with 50% perforation (Eco4).



(a) **(b)**

Figure H.27 A three-dimensional illustration of the slot-based designed half-bridge converter PCB with 75% perforation (Eco5).



(a) **(b)**

Figure H.28 A three-dimensional illustration of the combination of hole- and slot-based half-bridge converter PCB with 50% perforation (EcoSH).

I Component List for Half-Bridge Boards

The table below introduced the components used to generate one half-bridge test board.

Table I.1 Component list for half-bridge test boards.

Designator	Description	Quantity	Manufacturer Part Number
B1, B2	CONN BNC JACK STR 50 OHM	2	304-19-481
C1, C10, C11	CAP CER, 4.7uF, 50V, 1210, X7R	3	C1210C475K5RACTU
C2	CAP CER, 10uF, 50V, 1210, X7R	1	12105C106K4Z2A
C3	CAP CER, 1uF, 50V, 1210, X7R	1	12105C105KAT2A
C16, C17	CAP CER, 4.7uF, 25V, 1206, X7R	2	12063C475KAT2A
C22	CAP FILM, 7µF, 600VAC, RAD	1	C4AUPBW4700M3FJ
C25_1, C25_2	CAP ELEC, 1000uF, 400VDCV, SNAP IN	2	B43601A9108M060
C26, C29	CAP CER, 0.1uF, 50V, 0805, X7R	2	08055C104K4T4A
C27, C28	CAP ELEC, 100uF, 35V, SMD	2	EEE-FC1V101P
C30	CAP CER, 4.7uF, 250VAC, 2220, X7R	1	GA355DR7GF472KW01L
C31	CAP FILM 47pF, 1KVDC, RAD	1	BFC233663473
D1	DIODE GEN PURP 1.2kV 1A SMB	1	STTH112U
D4, D5	Schottky Barrier Diode, SOD-123,	2	MBR0540T1G
DCDC12	24Vin/12Vout DC-DC-Converter	1	TMH 2412S
DCDC18	12Vin/18Vout DC-DC-Converter	1	PUC1218050D2BG
DCDC24	24Vin/24vout DC-DC Converter	1	TEC 3-2415WI
DCDC5	12Vin/5Vout DC-DC Converter	1	TEC 3-2421UI
FH	FUSE 20A, 250VAC	1	B233451
J1	CONN Terminal, Bushing, M4,	1	7460307
L1	INDUC, Common mode choke, 10mH	1	744822110
LED1, LED2, LED3, LED4	LED SMD	4	MP008293
M1, M2	CONN MMCX, 50 OHM	2	135-3701-201
N/A	CONN BANANA Terminal,	2	23.3140-21
Q1, Q2	SiCFET N-CH 1.2KV 33 A TO247-4	2	SCTWA40N12G24AG
Q11	NPN Transistor	1	MMBT2222ALT1G
R1	RES SMD 4.7k OHM, 1/8 W, 0805,	1	RG2012V-472-B-T5
R10, R13	RES SMD 47 OHM, 1/4 W 1206	2	RT1206FRE07200RL
R11, R14	RES SMD 47 OHM, 1/4 W 1206	2	RC1206FR-07100RL
R12, R15	RES SMD 0 OHM, 1/4 W 1206	2	RC1206JR-070RL
R2	RES SMD, 22 OHM, 1/8 W, 0805	1	CRCW080522R0FKEA
R7	RES SMD, 10 OHM, 1/4 W, 1206	1	ERJ-8ENF10R0V
R?	RES SMD 2.2OHM, 1/4 W 1206	15	CRCW08050000Z0EA
U1, U2	IC, Isolated Gate Driver	2	NCD57080ADR2G
Z1	Zener Diode, 19V, 500 mW, SOD-123,	1	MMSZ5249BT1G

J Alternative Combination Heatmap

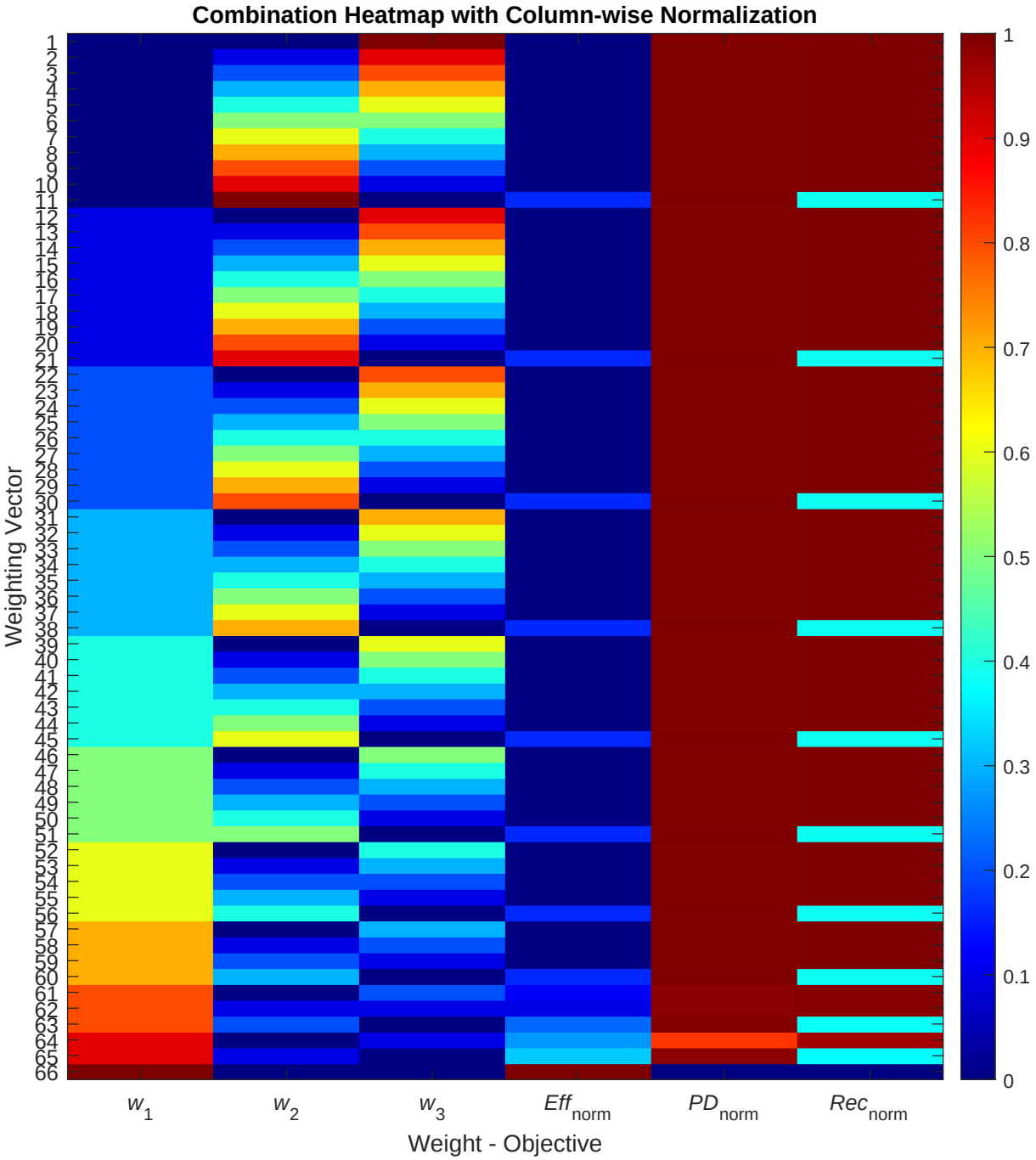


Figure J.1 Combination heatmap with column-wise normalization with lowest column entry as zero-reference.

K DPT Program

K.1 DPT Program Explained

As introduced in Section 2.4 the DPT program has to produce two ramping pulses for the DUT. Additionally, the high-side switch is also turned on in the free-wheeling period between the two pulses. As mentioned the bootstrap design of the converter also requires a bootstrap-charging period before the pulses. Refer to Figure 4.12 for the entire pulse sequence.
To realize the program it is chosen to make a program for a TI LAUNCHXL-F28069M MCU. To do this two enhanced PWM (ePWM) modules are used on the MCU. The reason two modules are used in the DPT program is that it allow for individual control of the switches without making them directly complementary. Doing this allow for both switches to be kept turned off while the program is idling. The switches are controlled with respective integers. These integers are multiplied by the respective reference waveform in the ePWM module, directly controlling when the gate signal is high or low.

The structure of the program has some base settings that should be applied before the program is run. These are the DC-link voltage, Vdc, this should always be at the maximum test voltage to ensure that the ramping time is never too long for an initial test. The inductance, L1, should be matched with the inductance of the used ramping inductor. Furthermore, a low test current tested also has to be input before startup, once again to ensure a small initial ramping test.
At startup, the program calculates the timings, t1, t2, and t3, for the initial test based on the inputs and the system settings using Equation (2.13). The program is then made such that it can be run over and over without shutting down and recompiling the code. This is possible through Code Composer Studio (CCS), which is used for the communication with the MCU, as it allows changing some variables while the program is running. This is also used to allow changes in the DC-link voltage, test currents and boot-strap pulses while the program is idling. The pulse sequence is based on a set of if-loops. The first part of the main loop as presented below:

```
1   if(startA==0){
2       ls_Duty = 0;
3       hs_Duty = 0;
4       }
```

This is the part that keeps the program idling as long as the variable 'startA' is 0. Next, the boot-strap charging part of the loop is shown:

```
1   else if(startA==1 && Ramp==0 && nPulse<=nPulseReq){
2       hs_Duty = 0;
3       if(nPulse%2==0){
4           ls_Duty=1;
5           nPulse++;}
6       else if(nPulse%2!=0){
7           ls_Duty=0;
8           nOff++;
```

```
            if(nOff==nOffReq){
                nPulse++;
                nOff=0;}
            }
        }
```

Here, the main statement check is that the system is still ready to ramp and that the required boot-strap charging pulses has not yet all been fired. The first nested if statement is allowing different lengths for the on-and-off periods in the boot-strap charging sequence. meanwhile, the second nested if-statement allows the reset of number of the off-periods part of the signal and let the system send a new on-period signal. Note that the high-side signal is kept low throughout the boot-strap charging.
When the boot-strap charging sequence is completed the ramping sequence of the program commences as shown below:

```
    else if(startA==1 && Ramp==0 && nPulse>nPulseReq){
        ls_Duty = 1;
        hs_Duty = 0;
        Ramp++;
        n++;
    }
```

Here, there is a statement check to see if the system is out of idle, that the current has not yet been ramped and that the boot-strap sequence has been completed. If this is true, the system starts ramping the inductor current by keeping 'ls_Duty' high and counts that the current has now been ramped for one interrupt period. The system then moves out of this loop as the ramping has begun and onto the last outer statement check of the DPT sequence as seen below:

```
    else if(startA==1 && Ramp==1){
        if(n<=n1){
            n++;
            ls_Duty = 1;
            hs_Duty = 0;
        }
        else if(n1<n && n<=n2 ){
            n++;
            ls_Duty = 0;
            hs_Duty = 1;
        }
        else if(n2<n && n<=n3){
            n++;
            ls_Duty = 1;
            hs_Duty = 0;
        }
        else if(n3<n){
            ls_Duty = 0;
            hs_Duty = 0;
        }
    }
```

The outer statement check ensures that the system is active and that the ramping has begun.

Then the first nested if-loop checks that the desired current is not yet ramped by checking that the number of interrupt cycles are less than the calculated required number of cycles to reach the desired current. Note that the number of interrupt cycles are increased with the term 'n++' When the required interrupt cycles are reached, the next nested loop is activated which turns off the low-side switch by setting 'ls_Duty' low and setting 'hs_Duty' high. This is then the free-wheeling period and it continues until the total number of interrupt cycles have surpassed the sum of the periods for the ramping and free-wheeling periods 'n2'.
When the free-wheeling period is completed the third nested statement becomes true and the switch signals are reversed. This continues until the number of interrupt periods have reached the calculated end value.
When the final number of interrupt periods is reached, the system enters the last nested loop, where it remains in an idle mode until the 'startA' or 'Ramp' variables are reset to zero.

The program can then be rerun by setting the variable 'run' to 1 in CCS. This activates the if-loop shown below:

```
if(run==1){
    run = 0;
    Ramp = 0;
    n = 0;
    nPulse = 0;
    startA = 1;
}
```

Here it is seen that the loop first resets the variables 'run', 'Ramp', 'n', 'nPulse' to zero, and then sets 'startA' to one, which activates the DPT sequence.

While the program is idling, the variables 'Vdc', 'Itest', 'Iend', 'nPulseReq', and 'nOffReq' can be altered. For the changes in 'Vdc', 'Itest', and 'Iend' to take affect, an if-loop checks if the variable 'Recalc' is one. When 'Recalc' is one the system enters the if-loop seen below:

```
if(Recalc==1){
    Recalc = 0;
    t1 = L1*Itest/Vdc;
    n1 = round(t1/Ts);
    t2 = 3*Ts;
    n2 = round((t2/Ts)) + n1;
    t3 = L1*(Itest+1)/Vdc - t1;
    n3 = round((t3/Ts)) + n2;
}
```

The loop first reset the 'Recalc' value and then recalculate the required interrupt cycles based Equation (2.13).

The setup for the ePWM modules and the interrupt service routines are presented in the following section where the full program is shown.

K.2 Full DPT Program

Note that '//' correspond to the line being commented out in CCS

```
//  ###########################################################################
//  #                    PED-1047 - spring semester 2025                      #
//  #       Eco Design for Sustainable Power Electronic Converters            #
//  #      DPT program for HB boards and Eco design implementations           #
//  ###########################################################################

// Connections:
//  - PWM signal for S1 is generated on pin J4.40 (Phase A upper switch)
//  - PWM signal for S2 is generated on pin J4.38 (Phase B upper switch)

// Notes:
//  - System frequency is set to 120 kHz

#include "DSP28x_Project.h"
#include "math.h"

interrupt void ePWM1_isr(void);
interrupt void ePWM2_isr(void);

// Define/Initialize variables:
 float Vdc = 700;
    // Input voltage
 float Fsw = 120e3;
    // Insert switching frequency
 float Fs = 120e3;
    // Sampling frequency
 float Ts = 0;
    // Sampling period. Precalculated at later point in code based on sampling
    frequency
 float L1 = 16e-3;
    // Inverter side inductance TODO correct value
 float ls_Duty = 0;
    // Initial duty cycle ls
 float hs_Duty = 0;
    // Initial duty cycle hs
 float Itest = 4;
    // The current which is desired to be tested at
 float Irated = 5;
    // Maximum current of the lowest rated device
 int startA = 0;
 int Ramp = 0;
 int n = 0;
 float t1 = 0;
 float n1 = 0;
 float t2 = 0;
 float n2 = 0;
 float t3 = 0;
 float n3 = 0;
 int run = 0;
 int nPulse = 0;
 int nPulseReq = 200;
```

```
51 int Recalc = 0;
52 int nOff = 0;
53 int nOffReq = 350;
54
55 void main(){
56     InitSysCtrl();
57         // TI device support function that initializes the System Control registers to
       a known state.
58
59 // Disable all interrupts when configuring the MCU:
60     DINT;
61         // Disable interrupts globally
62     IER = 0x0000;
63         // Disable interrupts at CPU LEVEL
64     IFR = 0x0000;
65         // Clear all CPU interrupt flags
66
67 // Initialization calls
68     InitGpio();
69         // TI device support function that initializes the GPIO to a known (default)
       state.
70
71 // Configuration of ePWM
72     // Setting up the ePWM1 pins:
73         EALLOW;
74             // GPIO control register is protected
75         // S1 - pin J4.40
76         GpioCtrlRegs.GPAPUD.bit.GPIO0 = 1;
77             // Disable pull-up resistor on GPIO 0 (always disable pull-up resistor on
       an output)
78         GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 1;
79             // Set GPIO function (GPIO0 = EPWM1A (pin J4.40))
80         GpioCtrlRegs.GPADIR.bit.GPIO0 = 1;
81             // Configure GPIO0 as an output (output = 1)
82
83         // S4 - pin J4.39
84         GpioCtrlRegs.GPAPUD.bit.GPIO1 = 1;
85             // Disable pull-up resistor on GPIO 1 (always disable pull-up resistor on
       an output)
86         GpioCtrlRegs.GPAMUX1.bit.GPIO1 = 1;
87             // Set GPIO function (GPIO1 = EPWM1B (pin J4.39))
88         GpioCtrlRegs.GPADIR.bit.GPIO1 = 1;
89             // Configure GPIO1 as an output (output = 1)
90         EDIS;
91             // Disable protected register access
92
93
94         // Configuring the ePWM1 time base counter:
95         EPwm1Regs.TBCTL.bit.PRDLD = TB_SHADOW;
96             // Enable shadowing of ePWM1
97         EPwm1Regs.TBCTL.bit.CLKDIV = 0;
98             // No scaling
99         EPwm1Regs.TBCTL.bit.HSPCLKDIV = 0;
100            // No scaling
```

```
101         EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
102             // Up-down-mode
103         EPwm1Regs.TBPRD = 90e6/(2*Fsw);
104             // Time base period set to 45, which for a up-down counter will generate a
    1 MHz PWM frequency
105         EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;
106             // Disable phase synchronization for ePWM1.
107 
108         // Configuring the ePWM1 counter compare:
109         EPwm1Regs.CMPCTL.bit.LOADAMODE = 0;
110             // Load the compare value on CTR = 0
111         EPwm1Regs.CMPCTL.bit.LOADBMODE = 0;
112             // Load the compare value on CTR = 0
113         EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
114             // CMPR registers are shadowed
115         EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
116             // CMPR registers are shadowed
117         EPwm1Regs.CMPA.half.CMPA = 0;
118             // Setting initial duty cycle as 0 (Used to be "EPwm1Regs.TBPRD * DutyA; //
     setting initial duty cycle as DutyA")
119         EPwm1Regs.CMPB = 0;
120             // Setting initial duty cycle as 0
121 
122         // Configuring the action qualifier:
123         EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
124             // Clear state when CTR = CMPA on up count
125         EPwm1Regs.AQCTLA.bit.CAD = AQ_SET;
126             // Set high state when CTR = CMPA on down count
127         EPwm1Regs.AQCTLB.bit.CAU = AQ_CLEAR;
128             // Clear state when CTR = CMPB on up count
129         EPwm1Regs.AQCTLB.bit.CAD = AQ_SET;
130             // Set high state when CTR = CMPB on down count
131         EPwm1Regs.AQCTLB.bit.CAD = AQ_CLEAR;
132             // Set high state when CTR = CMPB on down count
133 
134         // Dead-band for EPWM1B (PWM1B)
135         EPwm1Regs.AQCTLB.bit.CBU = AQ_CLEAR;
136             // Clear output on CMPB up-count
137         EPwm1Regs.AQCTLB.bit.CBD = AQ_SET;
138             // Set output on CMPB down-count
139 
140         // Set the dead-band value
141         EPwm1Regs.DBCTL.bit.OUT_MODE = 3;
142             // Dead-band enabled for both EPWM1A and EPWM1B
143         EPwm1Regs.DBCTL.bit.POLSEL = 2;
144             // Active high complementary (EPWM1B is inverted)
145         EPwm1Regs.DBCTL.bit.IN_MODE = 0;
146             // EPWM1A is the input for the dead-band
147         EPwm1Regs.DBRED = 1000;
148             // Rising edge dead-band count TODO: Adjust as needed
149         EPwm1Regs.DBFED = 1000;
150             // Falling edge dead-band count  TODO: Adjust as needed
151         // Falling edge dead-band count (adjust as needed)
152     // ePWM1 is now set up
```

```
153
154     // Setting up the ePWM2 pins:
155             EALLOW;
156                 // GPIO control register is protected
157             // S3 - pin J4.38
158             GpioCtrlRegs.GPAPUD.bit.GPIO2 = 1;
159                 // Disable pull-up resistor on GPIO2 (always disable pull-up resistor
    on an output)
160             GpioCtrlRegs.GPAMUX1.bit.GPIO2 = 1;
161                 // Set GPIO function (GPIO2 = EPWM2A (pin J4.38))
162             GpioCtrlRegs.GPADIR.bit.GPIO2 = 1;
163                 // Configure GPIO2 as an output (output = 1)
164             EDIS;
165                 // Disable protected register access
166
167             EALLOW;
168                 // GPIO control register is protected
169             // S6 - pin J4.37
170             GpioCtrlRegs.GPAPUD.bit.GPIO3 = 1;
171                 // Disable pull-up resistor on GPIO3 (always disable pull-up resistor
    on an output)
172             GpioCtrlRegs.GPAMUX1.bit.GPIO3 = 1;
173                 // Set GPIO function (GPIO3 = EPWM2B (pin J4.37))
174             GpioCtrlRegs.GPADIR.bit.GPIO3 = 1;
175                 // Configure GPIO3 as an output (output = 1)
176             EDIS;
177                 // Disable protected register access
178
179             // Configuring the ePWM2 time base counter:
180             EPwm2Regs.TBCTL.bit.PRDLD = TB_SHADOW;
181                 // Enable shadowing of ePWM2
182             EPwm2Regs.TBCTL.bit.CLKDIV = 0;
183                 // No scaling
184             EPwm2Regs.TBCTL.bit.HSPCLKDIV = 0;
185                 // No scaling
186             EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
187                 // Up-down-mode
188             EPwm2Regs.TBPRD = 90e6/(2*Fsw);
189                 // Time base period set to 45, which for a up-down counter will
    generate a 1 MHz PWM frequency
190             EPwm2Regs.TBCTL.bit.PHSEN = TB_DISABLE;
191                 // Disable phase synchronization for ePWM2.
192
193             // Configuring the ePWM2 counter compare:
194             EPwm2Regs.CMPCTL.bit.LOADAMODE = 0;
195                 // Load the compare value on CTR = 0
196             EPwm2Regs.CMPCTL.bit.LOADBMODE = 0;
197                 // Load the compare value on CTR = 0
198             EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
199                 // CMPR registers are shadowed
200             EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
201                 // CMPR registers are shadowed
202             EPwm2Regs.CMPA.half.CMPA = 0;
```

```
203                 // Setting initial duty cycle as 0 (Used to be "EPwm2Regs.TBPRD * DutyC
    ; // setting initial duty cycle as DutyC")
204             EPwm2Regs.CMPB = 0;
205                 // Setting initial duty cycle as 0
206
207             // Configuring the action qualifier:
208             EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;
209                 // Clear state when CTR = CMPA on up count
210             EPwm2Regs.AQCTLA.bit.CAD = AQ_SET;
211                 // Set high state when CTR = CMPA on down count
212             EPwm2Regs.AQCTLB.bit.CAU = AQ_CLEAR;
213                 // Clear state when CTR = CMPB on up count
214             EPwm2Regs.AQCTLB.bit.CAD = AQ_SET;
215                 // Set high state when CTR = CMPB on down count
216
217             // Dead-band for EPWM2B (PWM2B)
218             EPwm2Regs.AQCTLB.bit.CBU = AQ_CLEAR;
219                 // Clear output on CMPB up-count
220             EPwm2Regs.AQCTLB.bit.CBD = AQ_SET;
221                 // Set output on CMPB down-count
222
223             // Set the dead-band value
224             EPwm2Regs.DBCTL.bit.OUT_MODE = 3;
225                 // Dead-band enabled for both EPWM2A and EPWM2B
226             EPwm2Regs.DBCTL.bit.POLSEL = 2;
227                 // Active high complementary (EPWM2B is inverted)
228             EPwm2Regs.DBCTL.bit.IN_MODE = 0;
229                 // EPWM2A is the input for the dead-band
230             EPwm2Regs.DBRED = 100;
231                 // Rising edge dead-band count  TODO: Adjust as needed
232             EPwm2Regs.DBFED = 100;
233                 // Falling edge dead-band count  TODO: Adjust as needed
234         // ePWM2 is now set up
235
236
237 // Configure interrupt generation:
238     InitPieCtrl();
239         // TI device support function that initializes the PIE control registers to a
    known state.
240     InitPieVectTable();
241         // TI device support function that initialize the PIE vector table with
    pointers to the shell Interrupt Service Routines (ISR).
242     EALLOW;
243         // The PIE table is protected
244     PieVectTable.EPWM1_INT = &ePWM1_isr;
245         // Call the ISR to the PIE INT table
246     PieVectTable.EPWM2_INT = &ePWM2_isr;
247         // Call the ISR to the PIE INT table
248     EDIS;
249         // Disable protected register access
250     EPwm1Regs.ETSEL.bit.INTEN = 1;
251         // Enable INT
252     EPwm1Regs.ETSEL.bit.INTSEL = ET_CTR_ZERO;
253         // Generate INT on Zero event
```

```
254     EPwm1Regs.ETPS.bit.INTPRD = 1;
255         // Generate INT every x event TODO
256     PieCtrlRegs.PIEIER3.bit.INTx1 = 1;
257         // Enable EPWM1 in the PIE group 3
258     EPwm2Regs.ETSEL.bit.INTEN = 1;
259         // Enable INT
260     EPwm2Regs.ETSEL.bit.INTSEL = ET_CTR_ZERO;
261         // Generate INT on Zero event
262     EPwm2Regs.ETPS.bit.INTPRD = 1;
263         // Generate INT every x event TODO
264     PieCtrlRegs.PIEIER3.bit.INTx2 = 1;
265         // Enable EPWM2 in the PIE group 3
266     IER |= M_INT3;
267         // Enable CPU interrupt line 3
268     EINT;
269         // Enable global interrupt
270     ERTM;
271         // Enable Global realtime interrupt DBGM
272
273
274  // Precompute time intervals
275     Ts = 1/Fs;
276     t1 = L1*Itest/Vdc;
277     n1 = round(t1/Ts);
278     t2 = 3*Ts;
279     n2 = round((t2/Ts)) + n1;
280     t3 = L1*Irated/Vdc - t1;
281     n3 = round((t3/Ts)) + n2;
282
283 // MAIN USER CODE:
284 while(1){}
285
286 }   //############################ main() ends here ############################\\
287
288
289 interrupt void ePWM1_isr(void)
290     // Call the ISR (interrupt service routine). Interrupt occurs, every event, at CTR
        = 0 (to change how many events which need to occur go to the interrupt
        configuration just before main code starts.)
291 {
292     // Update ePWM:
293         EPwm1Regs.TBPRD = 90e6/(2*Fsw);
                    // Enable updating switching frequency
294         EPwm2Regs.TBPRD = EPwm1Regs.TBPRD;
                    // Enable updating switching frequency
295         if(startA==0){
296             ls_Duty = 0;
297             hs_Duty = 0;
298         }
299         else if(startA==1 && Ramp==0 && nPulse<=nPulseReq){
300             hs_Duty = 0;
301             if(nPulse%2==0){
302                 ls_Duty=1;
303                 nPulse++;}
```

```
            else if(nPulse%2!=0){
                ls_Duty=0;
                nOff++;
                if(nOff==nOffReq){
                    nPulse++;
                    nOff=0;}
            }
        }
        else if(startA==1 && Ramp==0 && nPulse>nPulseReq){
            ls_Duty = 1;
            hs_Duty = 0;
            Ramp++;
            n++;
        }
        else if(startA==1 && Ramp==1){
            if(n<=n1){
                n++;
                ls_Duty = 1;
                hs_Duty = 0;
            }
            else if(n1<n && n<=n2 ){
                n++;
                ls_Duty = 0;
                hs_Duty = 1;
            }
            else if(n2<n && n<=n3){
                n++;
                ls_Duty = 1;
                hs_Duty = 0;
            }
            else if(n3<n){
                ls_Duty = 0;
                hs_Duty = 0;
            }
        }

        if(run==1){
                    run = 0;
                    Ramp = 0;
                    n = 0;
                    nPulse = 0;
                    startA = 1;
                }

        if(Recalc==1){
            t1 = L1*Itest/Vdc;
            n1 = round(t1/Ts);
            t2 = 3*Ts;
            n2 = round((t2/Ts)) + n1;
            t3 = L1*(Itest+1)/Vdc - t1;
            n3 = round((t3/Ts)) + n2;
            Recalc = 0;
        }

```

```
358         // Update ePWM:
359         EPwm1Regs.CMPA.half.CMPA = EPwm1Regs.TBPRD * hs_Duty;
                    // Update PWM for S1 (high-side switch)
360         EPwm1Regs.CMPB = EPwm1Regs.TBPRD - EPwm1Regs.CMPA.half.CMPA;
                    // Update complimentary signal
361
362         EPwm2Regs.CMPA.half.CMPA = EPwm2Regs.TBPRD * ls_Duty;
                    // Update PWM for S2 (low-side switch)
363         EPwm2Regs.CMPB = EPwm2Regs.TBPRD - EPwm2Regs.CMPA.half.CMPA;
                    // Update complimentary signal
364
365     // End ePWM interrupt:
366         EPwm1Regs.ETCLR.bit.INT = 1;
367             // Clear event-trigger flag to receive more interrupts ePWM module
368         PieCtrlRegs.PIEACK.bit.ACK3 = 1;
369             // To receive more interrupts from this PIE group, acknowledge this
370
371
372 }
373
374 interrupt void ePWM2_isr(void){
375     // Call the ISR. Interrupt occurs, every event, at CTR = 0
376
377
378
379     // End ePWM2 interrupt:
380         EPwm2Regs.ETCLR.bit.INT = 1;
381             // Clear event-trigger flag to receive more interrupts ePWM module
382         PieCtrlRegs.PIEACK.bit.ACK3 = 1;
383             // To receive more interrupts from this PIE group, acknowledge this
384 }
```

L Complete MOO Algorithm

The following scripts are all made for use in Matlab R2024b. The scripts must be saved in the same folder along with the database which is set up as presented in Appendix M.

L.1 Initialization Script

The following script is the base script, which need to be implemented in a script, which is run by the user. The name of the script is thus not of importance.

```
I = 15; % [A] % Output current in RMS
V_out = 230; % [V] % Output voltage in RMS
V_dc = 700;  % [V] % DC-link voltage
w1_sep = 0.3;
w2_sep = 0.3;
w3_sep = 0.2;
w4_sep = 0.2;
w_sep = [w1_sep w2_sep w3_sep w4_sep];

w1_joint = 0.34;
w2_joint = 0.33;
w3_joint = 0.33;
w_joint = [w1_joint w2_joint w3_joint];

WeightStepSize = 0.1;
P_in = I*V_out*3; % Input power, neglectiong the losses
[nIter,nIterfsw,tPassed_min1,tPassed_sec1,CapDataOutput, ...
    CoreDataOutput,SwitchRecycDataOutput,BigDataMatrix, ...
    nfsw_SiC, nCores,nSiC1200] = EvaluationFunction3pfb(I,V_dc);

%%%%%%%%%% Efficiency, Power density and joint CR Optimization %%%%%%%%%%
[tPassed_min2,tPassed_sec2,results,paretoResults, ...
    MultiObjectiveSolutionEntry,WeightedVector,CompromiseResults] = ...
    ParetoOptimization_JointRecyc(nfsw_SiC,nCores,nSiC1200, ...
    CapDataOutput,CoreDataOutput,SwitchRecycDataOutput, ...
    BigDataMatrix,P_in,w_joint,WeightStepSize);

fprintf(['Using combination %i, which consitst of\n' ...
         'switch %i, core %i for L1, and core %i for\n' ...
         'L2 utilized at fsw = %i kHz results in \n' ...
         'the comprimise solution, which is pareto\n' ...
         'optimal.\n\n'], ...
         CompromiseResults(2,1),CompromiseResults(1,2), ...
         CompromiseResults(1,3),CompromiseResults(1,4), ...
         CompromiseResults(1,1))

fprintf(['Using the weightings, the multi-objective\n' ...
         'optimization algorithm selects pareto point\n' ...
         'number %d, which is combination %i consisting\n' ...
         'of switch %i, core %i for L1, and core %i for\n' ...
         'L2 utilized at fsw = %i kHz.\n\n'], ...
```

```
        MultiObjectiveSolutionEntry, ...
        paretoResults(MultiObjectiveSolutionEntry,1), ...
        results(paretoResults(MultiObjectiveSolutionEntry,1),2), ...
        results(paretoResults(MultiObjectiveSolutionEntry,1),3), ...
        results(paretoResults(MultiObjectiveSolutionEntry,1),4), ...
        results(paretoResults(MultiObjectiveSolutionEntry,1),1))

paretotxt1 ='Combination';      paretotxt2 ='Eff';
paretotxt3 ='Density';          paretotxt4 ='Recyc';
paretotxt5 ='fsw';              paretotxt6 ='Switch';
paretotxt7 ='HS Volume';        paretotxt8 ='L1 Core';
paretotxt9 ='L2 Core';          paretotxt10 ='FastDC';
paretotxt11 ='FastDCseries';    paretotxt12 ='FastDCparal';

paretotxt = {paretotxt1,paretotxt2,paretotxt3,paretotxt4, ...
             paretotxt5,paretotxt6,paretotxt7,paretotxt8, ...
             paretotxt9,paretotxt10,paretotxt11,paretotxt12};
paretoResults;

fprintf(['For the electrolytic capacitors in the DC-link,\n' ...
         'regardles of the combination %i electrolytic\n' ...
         'capacitors is/are used in series and %i is/are\n' ...
         'used in parallel. Number %i in the database is\n' ...
         'used resulting in a capacitance of %.1f mF.\n\n'], ...
         CapDataOutput(1,7), CapDataOutput(1,8), CapDataOutput(1,5), ...
         CapDataOutput(1,1))

fprintf(['For the capacitor in the filter regardles of\n' ...
         'the combination, %i is/are used in parallel.\n' ...
         'Number %i in the database is used resulting\n' ...
         'in a capacitance of %.1f uF.\n\n'], ...
         CapDataOutput(1,9), CapDataOutput(1,6), ...
         CapDataOutput(1,3)*1e3)

%%%% Results and excel document writting %%%%%%
Weighttxt1 ='WeightCoeff1';     Weighttxt2 ='WeightCoeff2';
Weighttxt3 ='WeightCoeff3';     Weighttxt4 ='Combination';
Weighttxt5 ='Efficiency';       Weighttxt6 ='Power Density';
Weighttxt7 ='Recyclability';

Weighttxt = {Weighttxt1,Weighttxt2,Weighttxt3,Weighttxt4, ...
             Weighttxt5,Weighttxt6,Weighttxt7};

WeightedVector;
% ^^ Gives the Pareto points chosen by the multi-objective algorithm
% at the different weigting coefficeints. The first 2-4 coloums consist
% of the weighting coefficients depending on which algorithm is chosen

delete('paretoResults.xlsx')
writecell(paretotxt,'paretoResults.xlsx','Sheet',1)
writematrix(paretoResults,'paretoResults.xlsx','WriteMode',...
    'append','Sheet',1)

writecell(Weighttxt,'paretoResults.xlsx','Sheet',2)
```

```
writematrix(WeightedVector,'paretoResults.xlsx','WriteMode',...
    'append','Sheet',2)

tPassed_sec = tPassed_sec1 + tPassed_sec2
tPassed_min = tPassed_min1 + tPassed_min2
```

L.2 Three-Phase Inverter Evaluation Script

The following script to be called 'EvaluationFunction3pfb.m'.

```
function [nIter,nIterfsw,tPassed_min,tPassed_sec,CapDataOutput,...
    CoreDataOutput,SwitchRecycDataOutput,BigDataMatrix,...
    nfsw_SiC,nCores,nSiC1200] = EvaluationFunction3pfb(I,V_dc)
tic;
tstart = tic;
nIterfsw = 0;
nIter = 0;
syms Rds_on(Isw)
nMod = 3;

%%%%%%%%%%%%%%%%%% System information for the algorithm %%%%%%%%%%%%%%%%%%
    Vds = V_dc;
    Is_rms = I;
    Vs_rms = 230;
    P_in = Is_rms*Vs_rms*3;
    f = 50;
    T_2 = (1/f)/2;
    DeltaV = 0.1;
    DeltaVfast = 0.1;
    deltaV = DeltaV*V_dc;
    deltaVfast = DeltaVfast*V_dc;
    fsw_SiC = 10e3:1e3:100e3; % [Hz]
    nfsw_SiC = length(fsw_SiC);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%% Heatsink stuff %%%%%%%%%%%%%%%%%%%%%%%%%%%%
    %R_V = 200; % cm^3*K/W
    R_TIM = 1.04; % K/W %
    % ^^ TO247-4 (2.1cm^2) and SIL PAD TSP A2000 @100psi (2.19cm^2*K/W)
    T_A = 25; % degC
    T_J = 90; % degC
    DeltaT_JA = T_J-T_A;
    %%% Load heatsink database
    file = 'Database.xlsx';
    % Load Material Recyclability
    HeatSinkDatabase = 'HeatsinkDatabase';
    [HeatSinkDatabase_data, ~] = xlsread(file, HeatSinkDatabase);
    nHeatsinks = length(HeatSinkDatabase_data);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%% Load component switch function coefficients %%%%%%%%%%%%%%%
    file = 'Database.xlsx';
    % Load Material Recyclability
    RecycCoefficients = 'MaterialRecycCoefficients';
```

```
45      [MaterialRecycCoefficients_data, MaterialRecycCoefficients_txt] = ...
46          xlsread(file, RecycCoefficients); %#ok<*XLSRD>
47      nMaterials = width(MaterialRecycCoefficients_data);
48      DensityAlu = 2700; % mg/cm^3 % Density of aluminium
49      for u = 1:nMaterials
50          if strcmpi(MaterialRecycCoefficients_txt(u),'Cu')
51              RecCopper = MaterialRecycCoefficients_data(u);
52          elseif strcmpi(MaterialRecycCoefficients_txt(u),'Fe')
53              RecIron = MaterialRecycCoefficients_data(u);
54          end
55      end
56
57      % Load SiC MOSFET data %
58      SiCFunctionCoefficients = 'MOSFETs 650 TO247';
59      [SiCdata650, SiCtxt650] = xlsread(file, SiCFunctionCoefficients);
60      nSiC650 = height(SiCdata650);
61      nMaterials650 = width(SiCdata650)-7;
62      SiCdata650 = [SiCdata650 zeros(nSiC650,1)];
63      Rds_location650 = width(SiCdata650);
64      t_int = 0:1e-6:T_2; % Used for integrating the resistance
65      is_int = Is_rms * sqrt(2) * sin(2 * pi * f * t_int);
66      % A % ^^Used for integrating the resistance
67      for u = 1:nSiC650
68          R0 = SiCdata650(u,4); R1 = SiCdata650(u,5); R2 = SiCdata650(u,6);
69          Rds_on(Isw) = (R2*Isw^2+R1*Isw+R0)*1e-3;
70          % Ohm % ^^ Drain-source resistance as a function of the current.
71          SiCdata650(u,Rds_location650) = double(sum(Rds_on(is_int)) / ...
72              length(is_int)); % Ohm % Used for conduction loss calculation
73      end
74
75      SiCFunctionCoefficients1200 = 'MOSFETs 1200 TO247-4';
76      [SiCdata1200, SiCtxt1200] = xlsread(file, SiCFunctionCoefficients1200);
77
78      nSiC1200 = height(SiCdata1200); %#ok<*NASGU>
79      nMaterials1200 = width(MaterialRecycCoefficients_data);
80
81      MaterialMatrix = zeros(nSiC1200,nMaterials1200);
82
83      SiCdata1200 = [SiCdata1200 zeros(nSiC1200,1)];
84      Rds_location1200 = width(SiCdata1200);
85
86      SiCdata1200 = [SiCdata1200 zeros(nSiC1200,1)];
87      Recyc_temp2_location1200 = width(SiCdata1200);
88
89      SiCdata1200 = [SiCdata1200 zeros(nSiC1200,1)];
90      MaterialMass_location1200 = width(SiCdata1200);
91
92      SiCdata1200 = [SiCdata1200 zeros(nSiC1200,1)];
93      Recyc_location1200 = width(SiCdata1200);
94
95
96      %%% Load core info to initilize data matrices %%%
97      sheet_name1 = 'Inductor_ToroidalCores';  % Name of the sheet
98      [num_data1, ~] = xlsread(file, sheet_name1);
```

```
99    nCores1 = height(num_data1);
100   sheet_name2 = 'Inductor_ECores';  % Name of the sheet
101   [num_data2, ~] = xlsread(file, sheet_name2);
102   nCores2 = height(num_data2);
103   nCores = nCores1+nCores2;
104   % Initialize big data matrix and core data matrix %
105   BigDataMatrix = zeros(nSiC1200*nCores*nfsw_SiC,23);
106   CoreDataOutput = zeros(nCores,4);
107   SwitchRecycDataOutput = zeros(nSiC1200,3);
108   % M_Cu_filter_matrix = zeros(nCores,nfsw_SiC);
109   M_Fe_filter = [1000*num_data1(:,5);1000*num_data2(:,5)]; % mg %
110   DissFactor = [num_data1(:,12);num_data2(:,15)];
111   % ^^ Mass of the cores read as gram and changed to mg
112   clear num_data1 num_data2
113   for u = 1:nSiC1200
114       R0 = SiCdata1200(u,4);
115       R1 = SiCdata1200(u,5);
116       R2 = SiCdata1200(u,6);
117       Rds_on(Isw) = (R2*Isw^2+R1*Isw+R0)*1e-3; % Ohm
118       % ^^ Drain-source resistance as a function of the switch current.
119       SiCdata1200(u,Rds_location1200) = ...
120           double(sum(Rds_on(is_int))/length(is_int)); % Ohm
121       % ^^ Used for conduction loss calculation
122   end
123   for u = 1:nSiC1200
124       for v = 1:nMaterials1200
125           MaterialMatrix(u,v) = SiCdata1200(u,7+v); % mg %
126       end
127   end
128   for u = 1:nSiC1200
129       Recyc_temp1 = 0; % Initialization and reset
130       Recyc_temp2 = 0; % Initialization and reset
131       MaterialMass_temp = 0; % Initialization and reset
132       Recyc = 0; % Initialization and reset
133       for v = 1:nMaterials1200
134           Recyc_temp1 = MaterialMatrix(u,v)* ...
135               MaterialRecycCoefficients_data(v);
136           % ^^mg % Calculating the amount of recyclable material
137           MaterialMass_temp = MaterialMass_temp+MaterialMatrix(u,v);
138           % ^^mg % Adding the mass of the materials to get the total mass
139           % at the end
140           Recyc_temp2 = Recyc_temp2 + Recyc_temp1;
141       end
142       Recyc = (Recyc_temp2/MaterialMass_temp)*100; % dim %
143       % The recyclability of the device given in percent
144
145       SiCdata1200(u,Recyc_temp2_location1200) = Recyc_temp2;
146       % This is the recyclability of the switching device
147
148       SiCdata1200(u,MaterialMass_location1200) = MaterialMass_temp;
149       % This is the recyclability of the switching device
150
151       SiCdata1200(u,Recyc_location1200) = Recyc;
152       % This is the recyclability of the switching device
```

```
153
154         SwitchRecycDataOutput(u,1) = Recyc_temp2; % Recyclable mass
155         SwitchRecycDataOutput(u,2) = MaterialMass_temp; % Total Mass
156         SwitchRecycDataOutput(u,3) = Recyc; % Recyclability in percent
157     end
158     clear Recyc_temp1 Recyc
159
160 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
161
162 %%% DC-link capacitor calculations %%%
163     C_dc_slow = (1e3*P_in*0.15)/(2*f*V_dc*deltaV);
164     % ^^ mF
165     RippleCurrentMag = C_dc_slow*deltaV*f/1e3;
166
167     % Initialize cap data output vector
168     CapDataOutput = zeros(1,9);
169     % Read electrolytic capacitor data
170     CapElec = 'CapacitorsElectrolytic';
171     [CapElec_data, ~]= xlsread(file, CapElec);
172     nCapElec = height(CapElec_data);
173     CapElec_data = [CapElec_data zeros(nCapElec,3)];
174     n_CapElecSerie_loc = width(CapElec_data)-2;
175     n_CapElecParal_loc = width(CapElec_data)-1;
176     CapElecTotalVol_loc = width(CapElec_data);
177     CapElec_data_temp = CapElec_data;
178
179     CapFilm = 'CapacitorsFilm';
180     [CapFilm_data, ~]= xlsread(file, CapFilm);
181     nCapFilm = height(CapFilm_data);
182     CapFilm_data = [CapFilm_data zeros(nCapFilm,3)];
183     n_CapFilmSerie_loc = width(CapFilm_data)-2;
184     n_CapFilmParal_loc = width(CapFilm_data)-1;
185     CapFilmTotalVol_loc = width(CapFilm_data);
186     CapFilm_data_temp = CapFilm_data;
187     FilmCapacitorDataOutput = zeros(nfsw_SiC*nCapFilm,2);
188
189     %%% Determine required caps in series depending on DC-link voltage and
190     % voltage rating of the caps:
191     k=0;
192     for n = 1:nCapElec
193         k = k+1;
194         if CapElec_data_temp(n,2) < (V_dc+V_dc*0.25)
195             CapElec_data_temp(n,n_CapElecSerie_loc)=2;
196
197         elseif CapElec_data_temp(n,2) > (V_dc+V_dc*0.25)
198             CapElec_data_temp(n,n_CapElecSerie_loc)=1;
199
200         else
201             CapElec_data_temp(n,n_CapElecSerie_loc)=10;
202         end
203     end
204
205     %%% Determine required caps in parallel depending on required
206     % capacitance and capacitance of the caps. Delete if more than 4
```

```
207     % parallel series connections are required:
208     k=0;
209     for n = 1:nCapElec
210         k = k+1;
211         if CapElec_data_temp(k,1)/...
212                 CapElec_data_temp(k,n_CapElecSerie_loc)...
213                 <C_dc_slow/4
214             CapElec_data_temp(k,:)=[];
215             k = k-1;
216         elseif CapElec_data_temp(k,1)/...
217                 CapElec_data_temp(k,n_CapElecSerie_loc)<C_dc_slow/3
218             CapElec_data_temp(k,n_CapElecParal_loc) = 4;
219             CapElec_data_temp(k,CapElecTotalVol_loc) = ...
220                 CapElec_data_temp(k,6) * ...
221                 CapElec_data_temp(k,n_CapElecParal_loc) * ...
222                 CapElec_data_temp(k,n_CapElecSerie_loc);
223         elseif CapElec_data_temp(k,1) / ...
224                 CapElec_data_temp(k,n_CapElecSerie_loc)<C_dc_slow/2
225             CapElec_data_temp(k,n_CapElecParal_loc)=3;
226             CapElec_data_temp(k,CapElecTotalVol_loc) = ...
227                 CapElec_data_temp(k,6) * ...
228                 CapElec_data_temp(k,n_CapElecParal_loc) * ...
229                 CapElec_data_temp(k,n_CapElecSerie_loc);
230         elseif CapElec_data_temp(k,1) / ...
231                 CapElec_data_temp(k,n_CapElecSerie_loc)<C_dc_slow
232             CapElec_data_temp(k,n_CapElecParal_loc)=2;
233             CapElec_data_temp(k,CapElecTotalVol_loc) = ...
234                 CapElec_data_temp(k,6) * ...
235                 CapElec_data_temp(k,n_CapElecParal_loc) * ...
236                 CapElec_data_temp(k,n_CapElecSerie_loc);
237         else
238             CapElec_data_temp(k,n_CapElecParal_loc)=1;
239             CapElec_data_temp(k,CapElecTotalVol_loc) = ...
240                 CapElec_data_temp(k,6) * ...
241                 CapElec_data_temp(k,n_CapElecParal_loc) * ...
242                 CapElec_data_temp(k,n_CapElecSerie_loc);
243         end
244     end
245     CapElec_data = CapElec_data_temp(1,:);
246     if k == 0
247         error(['No DC-link capacitors are usable without having to use' ...
248             ' more than 5 in parallel of them'])
249     end
250     nCapElec = height(CapElec_data_temp);
251     k = 0;
252     for n = 1:nCapElec
253         k = k+1;
254         if CapElec_data_temp(k,7) < ...
255                 RippleCurrentMag / CapElec_data_temp(k,n_CapElecParal_loc)
256             CapElec_data_temp(k,:)=[];
257             k = k-1;
258         end
259     end
260     [CapElec_data, CapElec_entry] = ...
```

```
261         min(CapElec_data_temp(:,CapElecTotalVol_loc));
262
263     CapDataOutput(1,1) = CapElec_data_temp(CapElec_entry,1) * ...
264                 CapElec_data_temp(CapElec_entry,n_CapElecParal_loc) / ...
265                 CapElec_data_temp(CapElec_entry,n_CapElecSerie_loc);
266     % ^^ Saves electrolytic DC-link capacitance in mF
267
268     CapDataOutput(1,2) = CapElec_data_temp(CapElec_entry, ...
269                         CapElecTotalVol_loc)/1e3;
270     % ^^ Saves electrolytic DC-link capacitor volume in litres
271
272     CapDataOutput(1,5) = CapElec_data_temp...
273                         (CapElec_entry,3);
274     % ^^ Capacitor entry in database % dim %
275
276     CapDataOutput(1,7) = CapElec_data_temp...
277                         (CapElec_entry,n_CapElecSerie_loc);
278     % ^^ Series slow caps in DC-link % dim %
279
280     CapDataOutput(1,8) = CapElec_data_temp...
281                         (CapElec_entry,n_CapElecParal_loc);
282     % ^^ Parallel slow caps in DC-link % dim %
283
284 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
285
286 z = 0;
287 %%%%%%%%%%%%%%%%%%%%%%%%%%%% Main loop 1 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
288 for fsw = fsw_SiC
289     z = z+1; % Counting fsw iterations
290     C_dc_fast = 1e3*P_in/((V_dc*deltaVfast-deltaVfast^2/2)*fsw);
291     % ^^ mF
292     %%% Determine required caps in series depending on DC-link voltage and
293     % voltage rating of the caps:
294     k=0;
295     if z == 1
296         CapFilm_data_temp1 = CapFilm_data;
297     end
298     CapFilm_data_temp = CapFilm_data_temp1;
299     for n = 1:nCapFilm
300         k = k+1;
301         if CapFilm_data_temp(n,2) < (V_dc+V_dc*0.25)
302             CapFilm_data_temp(n,n_CapFilmSerie_loc)=2;
303
304         elseif CapFilm_data_temp(n,2) > (V_dc+V_dc*0.25)
305             CapFilm_data_temp(n,n_CapFilmSerie_loc)=1;
306
307         else
308             CapFilm_data_temp(n,n_CapFilmSerie_loc)=1000;
309
310         end
311     end
312
313     %%% Determine required caps in parallel depending on required
314     % capacitance and capacitance of the caps. Delete if more than 4
```

```
315     % parallel series connections are required:
316     k=0;
317     for n = 1:nCapFilm
318         k = k+1;
319         if CapFilm_data_temp(k,1)/...
320                 CapFilm_data_temp(k,n_CapFilmSerie_loc) < ...
321                 C_dc_fast/4
322             CapFilm_data_temp(k,:)=[];
323             k = k-1;
324         elseif CapFilm_data_temp(k,1)/...
325                 CapFilm_data_temp(k,n_CapFilmSerie_loc) < C_dc_fast/3
326             CapFilm_data_temp(k,n_CapFilmParal_loc) = 4;
327             CapFilm_data_temp(k,CapFilmTotalVol_loc) = ...
328                 CapFilm_data_temp(k,8) * ...
329                 CapFilm_data_temp(k,n_CapFilmParal_loc) * ...
330                 CapFilm_data_temp(k,n_CapFilmSerie_loc);
331         elseif CapFilm_data_temp(k,1) / ...
332                 CapFilm_data_temp(k,n_CapFilmSerie_loc) < C_dc_fast/2
333             CapFilm_data_temp(k,n_CapFilmParal_loc)=3;
334             CapFilm_data_temp(k,CapFilmTotalVol_loc) = ...
335                 CapFilm_data_temp(k,8) * ...
336                 CapFilm_data_temp(k,n_CapFilmParal_loc) * ...
337                 CapFilm_data_temp(k,n_CapFilmSerie_loc);
338         elseif CapFilm_data_temp(k,1) / ...
339                 CapFilm_data_temp(k,n_CapFilmSerie_loc) < C_dc_fast
340             CapFilm_data_temp(k,n_CapFilmParal_loc)=2;
341             CapFilm_data_temp(k,CapFilmTotalVol_loc) = ...
342                 CapFilm_data_temp(k,8) * ...
343                 CapFilm_data_temp(k,n_CapFilmParal_loc) * ...
344                 CapFilm_data_temp(k,n_CapFilmSerie_loc);
345         else
346             CapFilm_data_temp(k,n_CapFilmParal_loc)=1;
347             CapFilm_data_temp(k,CapFilmTotalVol_loc) = ...
348                 CapFilm_data_temp(k,8) * ...
349                 CapFilm_data_temp(k,n_CapFilmParal_loc) * ...
350                 CapFilm_data_temp(k,n_CapFilmSerie_loc);
351         end
352     end
353     CapFilm_data = CapFilm_data_temp(:,1);
354     if k == 0
355         error(['No DC-link capacitors are usable without having to use' ...
356             ' more than 5 in parallel of them'])
357     end
358
359     nCapFilm = height(CapFilm_data_temp);
360     k = 0;
361
362     for n = 1:nCapFilm
363         k = k+1;
364         if CapFilm_data_temp(k,6) < ...
365                 RippleCurrentMag/CapFilm_data_temp(k,n_CapFilmParal_loc)
366             CapFilm_data_temp(k,:)=[];
367             k = k-1;
368         end
```

```
    end

    [FastCapacitanceVolume FastCapacitor] = ...
        min(CapFilm_data_temp(:,CapFilmTotalVol_loc));
    FastCapNumber = CapFilm_data_temp(FastCapacitor,4);
    %^^ Number capacitor in databse
    FastCapVolume = FastCapacitanceVolume/1e3;
    % ^^ Total volume of capacitors in series and parallel for fast DC
    % Converting from cm^3 to L
    FastCapCapacitance = CapFilm_data_temp(FastCapacitor,1);
    FastCapSeries = CapFilm_data_temp(FastCapacitor,n_CapFilmSerie_loc);
    FastCapParallel = CapFilm_data_temp(FastCapacitor,n_CapFilmParal_loc);
    % ^^ Actual capacitance per capacitor % mF %
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

    %%% Run filter design and loss function
    [P_filter_L1,P_filter_L2,VolumeFilterCore,FilterCoreName,C_f,...
        M_Cu_filter_L1,M_Cu_filter_L2, VolumeCu_L1, VolumeCu_L2,...
        BsatCheck_L1,BsatCheck_L2,ApCheck_L1,ApCheck_L2, WaCheck_L1, ...
        WaCheck_L2] = LCLFilterDesignFunction(fsw,Is_rms,V_dc,z);

    if z == 1
        % Save filter capacitor info %
        CapDataOutput(1,3) = C_f(1,1); % Filter capacitance % mF %
        CapDataOutput(1,4) = C_f(1,2)/1e3; % Filter cap volume % L %
        CapDataOutput(1,6) = C_f(1,3); % Filter cap number % dim %
        CapDataOutput(1,9) = C_f(1,4); % Parallel caps in filter % dim %
        for i = 1:nCores
            CoreDataOutput(i,1) = i;
        end
        CoreDataOutput(:,2) = M_Fe_filter/1e6;
        % ^^ Save core mass in kg
        CoreDataOutput(:,3) = VolumeFilterCore/1e3;
        % ^^ Save core volume in L
        CoreDataOutput(:,4) = DissFactor;
        % ^^ Save the core disassemblibillity
    end

    for i = 1:nCores
        for j = 1:nSiC1200
            BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,1) = ...
                fsw/1e3; % [kHz]
            BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,6) = (i);
            BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,7) = ...
                M_Cu_filter_L1(i)/1e6; % [kg]
            BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,8) = ...
                VolumeCu_L1(i)/1e6; % [L]
            if BsatCheck_L1(i) == 1 || ApCheck_L1(i) == 1 ...
                    || WaCheck_L1(i) == 1
                BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,9) = 1;
            else
                BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,9) = 0;
            end
            BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,10) = ...
```

```
423                 M_Cu_filter_L2(i)/1e6; % [kg]
424             BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,11) = ...
425                 VolumeCu_L2(i)/1e6; % [L]
426             if BsatCheck_L2(i) == 1 || ApCheck_L2(i) == 1 ...
427                     || WaCheck_L2(i) == 1
428                 BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,12) = 1;
429             else
430                 BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,12) = 0;
431             end
432             BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,13) = ...
433                 CoreDataOutput(BigDataMatrix(i,6),2)/1e6;
434             BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,14) = ...
435                 CoreDataOutput(BigDataMatrix(i,6),3)/1e3;
436             BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,15) = ...
437                 (M_Cu_filter_L1(i)*RecCopper+CoreDataOutput ...
438                 (BigDataMatrix(i,6),2)*RecIron)/ ...
439                 (M_Cu_filter_L1(i)+ ...
440                 CoreDataOutput(BigDataMatrix(i,6),2));
441             BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,16) = ...
442                 P_filter_L1(i);
443             BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,17) = ...
444                 (M_Cu_filter_L2(i)*RecCopper+CoreDataOutput ...
445                 (BigDataMatrix(i,6),2)*RecIron)/ ...
446                 (M_Cu_filter_L2(i)+ ...
447                 CoreDataOutput(BigDataMatrix(i,6),2));
448             BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,18) = ...
449                 P_filter_L2(i);
450             BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,19) = ...
451                 FastCapNumber;
452             BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,20) = ...
453                 FastCapCapacitance;
454             BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,21) = ...
455                 FastCapVolume;
456             BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,22) = ...
457                 FastCapSeries;
458             BigDataMatrix(i+(z-1)*nCores*nSiC1200+(j-1)*nCores,23) = ...
459                 FastCapParallel;
460         end
461     end
462
463     for i = 1:nSiC1200 % This loops the SiC MOSFETs
464         nIter = nIter + 1; %Counting every combination iterations
465         if Vds <= 650*(2/3)
466             E = [SiCdata650(i,1) SiCdata650(i,2) SiCdata650(i,3)];
467             R = [SiCdata650(i,Rds_location650)];
468             R_JC = SiCdata650(i,7);
469             SiCtxt650 = SiCtxt650; %#ok<ASGSL>
470         elseif Vds <= 1200*(2/3)
471             E = [SiCdata1200(i,1) SiCdata1200(i,2) SiCdata1200(i,3)];
472             R = [SiCdata1200(i,Rds_location650)];
473             R_JC = SiCdata1200(i,7);
474             SiCtxt650 = SiCtxt1200;
475         else
476             error(['None of the MOSFETs in the database\n' ...
```

```
                'are rated for this voltage'])
        end

        %%% Run the SPWM switch power loss function %%%
        fprintf('SiC %d, fsw = %.2f kHz, Sinusoidal\n',i, fsw/1000)
        [P_data,P_sw_losses_indv] = SwitchLoss3phaseSiC_SPWM(Is_rms, ...
            V_dc,fsw,f,E(1),E(2),E(3),R(1));
        %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

        %%% Heat sink calculations %%%
        P_loss_hs_switch = P_sw_losses_indv(1,1)+P_sw_losses_indv(1,2);
        P_loss_ls_switch = P_sw_losses_indv(2,1)+P_sw_losses_indv(2,2);
        P_phase_avg = (P_loss_hs_switch + P_loss_ls_switch)/2;
        R_HS = (DeltaT_JA/(6*P_phase_avg))-((R_JC+R_TIM)/6);
        for k = 1:nHeatsinks
            if R_HS>HeatSinkDatabase_data(k,1)
                VolumeHStot = HeatSinkDatabase_data(k,5);
                % ^^ Heatsink volume in litres [L]
                HSnumber = HeatSinkDatabase_data(k,7);
                % ^^ Database entry number of the chosen heatsink
                break
            else
                HSnumber = 1;
                VolumeHStot = 0;
            end
        end
        %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

        for k = 1:nCores
            BigDataMatrix(k+(z-1)*nCores*nSiC1200+(i-1)*nCores,2) = i;
            BigDataMatrix(k+(z-1)*nCores*nSiC1200+(i-1)*nCores,3) = ...
                P_data(1,3);
            BigDataMatrix(k+(z-1)*nCores*nSiC1200+(i-1)*nCores,4) = ...
                VolumeHStot;
            BigDataMatrix(k+(z-1)*nCores*nSiC1200+(i-1)*nCores,5) = ...
                HeatSinkDatabase_data(HSnumber,6);
        end
    end
    nIterfsw = nIterfsw + 1;
end

%%%%%%%%%%%%%%%
tPassed_sec = toc(tstart); % s %
tPassed_min = tPassed_sec/60; % min %

end
```

L.3 LCL-Filter Design and Loss Function

The following script to be called 'LCLFilterDesignFunction.m'.

```
function [P_L_vector_L1,P_L_vector_L2,VolumeCore_vector,FilterName,C_f, ...
M_Cu_filter_L1_vector,M_Cu_filter_L2_vector,VolumeCu_L1_vector, ...
VolumeCu_L2_vector,ApCheck_L1vector,ApCheck_L2vector, ...
BsatCheck_L1vector,BsatCheck_L2vector,WaCheck_L1vector, ...
WaCheck_L2vector] = LCLFilterDesignFunction(fsw,Is_rms,V_dc,z)

%%% Load component data file %%%
file = 'Database.xlsx';        % Specify the file
sheet_name_Toroidal = 'Inductor_ToroidalCores';  % Name of the sheet
[num_dataToriodal, txt_dataToroidal] = ...
    xlsread(file, sheet_name_Toroidal);%#ok<XLSRD>
nDataToroidal = height(num_dataToriodal);
txt_wo_headerToroidal = txt_dataToroidal;
txt_wo_headerToroidal(1,:)=[];
FilterNameToroidal = txt_wo_headerToroidal(:,1);
sheet_name_E = 'Inductor_ECores';  % Name of the sheet
[num_dataE, txt_dataE] = ...
    xlsread(file, sheet_name_E);%#ok<XLSRD>
nDataE = height(num_dataE);
txt_wo_headerE = txt_dataE;
txt_wo_headerE(1,:)=[];
FilterNameE = txt_wo_headerE(:,1);
sheet_name2 = 'CapacitorsFilm';  % Name of the sheet
[cap_data, ~] = xlsread(file, sheet_name2); %#ok<XLSRD>
nCaps = height(cap_data);

Omega = char(937);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%% Constants %%%
V_s = 230; % [V] % Grid RMS phase voltage
I_o = Is_rms; % [A] % Output RMS line current
I_max = I_o * sqrt(2);
E_n = V_s*sqrt(3); % [V] % Nominal grid RMS line-2-line voltage
P_n = 3*V_s*I_o; % [W] % Nominal power per phase
f = 50; % [Hz] % Grid frequency
omega_g = 2*pi*f; % [rad/s] % Angular grid frequency
f_sw = fsw; % [Hz] % Swithing frequency
omega_sw = 2*pi*f_sw; % [rad/s] % Angular switching frequency
x = 0.05; % dim % Power factor variation seen by the grid
k_a = 0.20; % dim % Attenuation factor for the filter
rho_copper = 8.96; % mg/mm^3
Jmax = 6; % Max allow current density in winding conductors [A/mm^2]
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%% Vector and matrix initializations for toroidal cores %%%
BsatCheck_L1vectorToroidal = zeros(nDataToroidal,1);
BsatCheck_L2vectorToroidal = zeros(nDataToroidal,1);
ApCheck_L1vectorToroidal = zeros(nDataToroidal,1);
ApCheck_L2vectorToroidal = zeros(nDataToroidal,1);
WaCheck_L1vectorToroidal = zeros(nDataToroidal,1);
```

```
WaCheck_L2vectorToroidal = zeros(nDataToroidal,1);
P_L_vector_L1Toroidal = zeros(nDataToroidal,1);
P_L_vector_L2Toroidal = zeros(nDataToroidal,1);
VolumeCore_vectorToroidal = zeros(nDataToroidal,1);
VolumeCu_L1_vectorToroidal = zeros(nDataToroidal,1);
VolumeCu_L2_vectorToroidal = zeros(nDataToroidal,1);
M_Cu_filter_L1_vectorToroidal = zeros(nDataToroidal,1);
M_Cu_filter_L2_vectorToroidal = zeros(nDataToroidal,1);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%% Vector and matrix initializations for E-cores %%%
BsatCheck_L1vectorE = zeros(nDataE,1);
BsatCheck_L2vectorE = zeros(nDataE,1);
ApCheck_L1vectorE = zeros(nDataE,1);
ApCheck_L2vectorE = zeros(nDataE,1);
WaCheck_L1vectorE = zeros(nDataE,1);
WaCheck_L2vectorE = zeros(nDataE,1);
P_L_vector_L1E = zeros(nDataE,1);
P_L_vector_L2E = zeros(nDataE,1);
VolumeCore_vectorE = zeros(nDataE,1);
VolumeCu_L1_vectorE = zeros(nDataE,1);
VolumeCu_L2_vectorE = zeros(nDataE,1);
M_Cu_filter_L1_vectorE = zeros(nDataE,1);
M_Cu_filter_L2_vectorE = zeros(nDataE,1);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%% Calculations %%%
Z_b = E_n^2/P_n;
% ^^ Base impedance % [Ohm] %
C_b = 1/(omega_g*Z_b);
% ^^ Base capacitance % [Ohm] %
DeltaImax = 0.1*I_max;
% ^^ Allowed current ripple % [A] %
L_1 = V_dc/(6*f_sw*DeltaImax);
% ^^ Inverter-side filter inductance % [H] %
L1 = L_1*1e3;
% ^^ Inverter-side filter inductance % [mH] %
C_f = x*C_b;
% Filter capacitance % [F] %
L_2 = (sqrt(1/k_a^2)+1)/(C_f*omega_sw^2);
% ^^ Grid-side filter inductance % [H] %
L2 = L_2*1e3;
% ^^ Grid-side filter inductance % [mH] %
omega_res = sqrt((L_1+L_2)/(L_1*L_2*C_f));
% ^^ Angular resonance frequency % [rad/s] %
f_res = omega_res/(2*pi);
% ^^ Resonance frequency % [Hz] %
R_f = 1/(3*omega_res*C_f);
% ^^ Recommended damping resistor % [Ohm] %
lower_check = 10*f<f_res;
% ^^ Lower check, res-freq a magnitude larger than grid frequency
upper_check = f_res<0.5*f_sw;
% ^^ Upper check, res-freq smaller than half switching frequency
if z==1
```

```
106     fprintf('Switching frequency = %.2f kHz\n',fsw/1e3)
107 else
108     fprintf('\n\n\nSwitching frequency = %.2f kHz\n',fsw/1e3)
109 end
110 if lower_check==1 && upper_check ==1
111     fprintf(['Inverter-side inductance = %.2f mH,\n' ...
112         'Filter capacitance = %.2f uF,\n' ...
113         'Grid-side inductance = %.2f uH,\n' ...
114         'Damping resistor = %.2f %s \n'], L1,C_f*1e6,L2*1e3,R_f,Omega)
115 else
116     fprintf('Resonant frequency is causing trouble\n')
117 end
118 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
119 
120 %%% Choosing capacitor %%%
121 V_cf=sqrt(V_s^2+omega_g^2*L_2^2*I_o^2-2*omega_g*L_2*I_o*V_s*sin(pi/2));
122 % ^^ Capacitor voltage % V %
123 
124 C_f_mF = C_f*1e3;
125 k = 0;
126 for i = 1:nCaps
127     k = k+1;
128     if cap_data(k,3) < (V_cf+V_cf*0.25)
129         cap_data(k,:)=[];
130         k = k-1;
131     end
132 end
133 
134 nCap = height(cap_data);
135 cap_data = [cap_data zeros(nCap,3)];
136 n_capParal_loc = width(cap_data)-2;
137 capTotalVol_loc = width(cap_data)-1;
138 I_ripple_loc = width(cap_data);
139 
140 k=0;
141 for n = 1:nCap
142     k = k+1;
143     if cap_data(k,1) < C_f_mF/4
144         cap_data(k,:)=[];
145         k = k-1;
146 
147     elseif cap_data(k,1) < C_f_mF/3
148         cap_data(k,n_capParal_loc) = 4;
149         % ^^ Number of capacitors required in parallel %
150         cap_data(k,capTotalVol_loc) = cap_data(k,5) * ...
151             cap_data(k,n_capParal_loc);
152         % ^^ Total volume % cm^3 %
153         cap_data(k,I_ripple_loc) = omega_g*cap_data(k,1)/1e3*4*V_cf;
154         % ^^ Per cap current ripple RMS % A %
155 
156     elseif cap_data(k,1) < C_f_mF/2
157         cap_data(k,n_capParal_loc) = 3;
158         % ^^ Number of capacitors required in parallel %
159         cap_data(k,capTotalVol_loc) = cap_data(k,5) * ...
```

```
            cap_data(k,n_capParal_loc);
        % ^^ Total volume % cm^3 %
        cap_data(k,I_ripple_loc) = omega_g*cap_data(k,1)/1e3*3*V_cf;
        % ^^ Per cap current ripple RMS % A %

    elseif cap_data(k,1) < C_f_mF
        cap_data(k,n_capParal_loc) = 2;
        % ^^ Number of capacitors required in parallel %
        cap_data(k,capTotalVol_loc) = cap_data(k,5) * ...
            cap_data(k,n_capParal_loc);
        % ^^ Total volume % cm^3 %
        cap_data(k,I_ripple_loc) = omega_g*cap_data(k,1)/1e3*2*V_cf;
        % ^^ Per cap current ripple RMS % A %

    else
        cap_data(k,n_capParal_loc) = 1;
        % ^^ Number of capacitors required in parallel %
        cap_data(k,capTotalVol_loc) = cap_data(k,5) * ...
            cap_data(k,n_capParal_loc);
        % ^^ Total volume % cm^3 %
        cap_data(k,I_ripple_loc) = omega_g*cap_data(k,1)/1e3*V_cf;
        % ^^ Per cap current ripple RMS % A %

    end
end

nCaps = height(cap_data);

k = 0;
for i = 1:nCaps
    k = k+1;
    if cap_data(k,3) < (V_cf+V_cf*0.25) || ...
             cap_data(k,9)/cap_data(k,n_capParal_loc) < ...
             cap_data(k,I_ripple_loc)
        cap_data(k,:)=[];
        k = k-1;
    end
end

[~, cap_entry ] = min(cap_data(:,capTotalVol_loc));
C_f = [cap_data(cap_entry,1), cap_data(cap_entry,capTotalVol_loc), ...
       cap_data(cap_entry,4), cap_data(cap_entry,n_capParal_loc)];
% Saves the capacitors to the output %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%% Design of filter inductors with toroidal cores %%%
for i = 1:nDataToroidal
    %Core Parameters (Datasheet)
    Al = num_dataToriodal(i,1);          % [H/turn]
    ur = num_dataToriodal(i,2);          % Relative permeability
    le = num_dataToriodal(i,3);          % Effective length [m]
    Ve = num_dataToriodal(i,4);          % Effective volume [m^3]
    M = num_dataToriodal(i,5);           % Mass [kg]
    Bsat = num_dataToriodal(i,6);        % Saturation flux density [T]
```

```
    OD = num_dataToriodal(i,9)*1e-3;     % Outer core diamter [m]
    HT = num_dataToriodal(i,10)*1e-3;     % Core height [m]
    ID = num_dataToriodal(i,11)*1e-3;    % Inner core diamter [m]
    % Core calculations
    Kw = 0.5;                          % Window utilization factor
    u_core = ur * 4 * pi * 10^-7;   % Permeability [H/m]
    Aw = pi*(ID^2)/4;                % Window area [m^2]
    Ac = (OD-ID)*HT;
    Ap = Aw*Ac;                        % Area product of core [m^4]
    % Wire Parameters
    Nw = 0;                            % "Initial" number of wires per winding
    J = 100;
    while J>Jmax
        Nw = Nw+1;
        r_L = 10.44;      % Wire resistivity AWG 15 [ohm/km]
        AWG = 15;
        A = 1.65; % mm^2
        Awire = A*Nw;
        J = I_o/Awire;
    end
    J = J*1e6;
    Awire = Awire*1e-6;
    WcoreL1 = (1/2)*L_1*I_max^2;
    WcoreL2 = (1/2)*L_2*I_max^2;

%%% Inductor Conduction Power Loss Calculations %%%
    N_L1 = sqrt(L_1/Al);
    % ^^ Number of turns
    N_L2 = sqrt(L_2/Al);
    % ^^ Number of turns
    Awind_L1 = Awire*N_L1/Kw;
    % ^^ Area in the window which is taken up by the windings L1
    Awind_L2 = Awire*N_L2/Kw;
    % ^^ Area in the window which is taken up by the windings L2
    B_L1 = ( u_core*N_L1*I_max) / le;
    % ^^ Fundamental magnetic flux density inverter inductor [Wb/m^2]
    B_L1r = ( u_core*N_L1*I_max*0.2) / le;
    % ^^ Ripple magnetic flux density inverter inductor [Wb/m^2]
    B_L2 = (u_core*N_L2*I_max) / le;
    % ^^ Fundamental magnetic flux density grid inductor [Wb/m^2]
    B_L2r = (u_core*N_L2*I_max*0.2) / le;
    % ^^ Ripple magnetic flux density grid inductor [Wb/m^2]
    Apreq_L1 = 2*WcoreL1/(B_L1*J*Kw);
    % ^^ Required area product for L1 [m^4]
    Apreq_L2 = 2*WcoreL2/(B_L1*J*Kw);
    % ^^ Required area product for L2 [m^4]
    K = (2*(OD-ID)+2*HT)*1e-3;
    % ^^ Wire length per turn(circumference core) [km/Turn]
    l_L1 = N_L1 * K * Nw;
    % ^^ Wire length inverter inductor [km]
    l_L2 = N_L2 * K * Nw;
    % ^^ Wire length grid inductor [km]
    R_L1 = r_L * l_L1;
    % ^^ Inductor resistance [ohm]
```

```
    R_L2 = r_L * l_L2;
    % ^^ Inductor resistance [ohm]
    Pv_winding_L1 = Is_rms^2*R_L1;
    % ^^ Inductor conduction losses [W]
    Pv_winding_L2 = Is_rms^2*R_L2;
    % ^^ Inductor conduction losses [W]
    V_copper_L1 = (l_L1)*1e6*A;
    % ^^ mm^3
    V_copper_L2 = (l_L2)*1e6*A;
    % ^^ mm^3
    M_copper_L1 = V_copper_L1*rho_copper;
    % ^^ mg
    M_copper_L2 = V_copper_L2*rho_copper;
    % ^^ mg

%%% Checking flux density saturation %%%
    if Bsat < B_L1
            fprintf(['\nCore number %.0f in the database can not ' ...
                'handle the flux density \nat fsw = %d kHz, and ' ...
                'Is_rms = %.1f A. A larger core is required \n' ...
                'at this switching frequency and current for the' ...
                ' inverter-side inductor.\n\n'], i, fsw*1e-3, Is_rms)
    else
            fprintf(['\nWindings for inductor L1 / length of ' ...
                'required wire / wire gauge\nfor core number' ...
                ' %d %s: \n%.2f [dim] / %.2f [m] / %.2f\n'], ...
                i,txt_wo_headerToroidal{i,1},N_L1,l_L1*1e3,AWG)
    end

    if Bsat < B_L2
            fprintf(['\nCore number %.0f in the database can not ' ...
                'handle the flux density \nat fsw = %d kHz, ' ...
                'and Is_rms = %.1f A. A larger core is required \n' ...
                'at this switching frequency and current for the ' ...
                'grid-side inductor.\n\n'], i, fsw*1e-3, Is_rms)
    else
            fprintf(['\nWindings for inductor L2 / length of ' ...
                'required wire / wire gauge \nfor core number ' ...
                '%d %s:\n%.2f [dim] / %.2f[m] / %.2f\n\n'], ...
                i,txt_wo_headerToroidal{i,1},N_L2,l_L2*1e3,AWG)
    end

%%% Chooses the appropriate calculation based on the Material %%%
    if strcmpi(txt_dataToroidal(i+1,9), 'Neu Flux')
            % Use the Pv_NEU function (Magnetic characteristics)
            Pv_function=@(Br,fsw)(Br*10)^2.150*(5.101*(fsw*1e-3) + ...
                0.1561*(fsw*1e-3)^1.822);
            % ^^ Power loss for inverter-side inductor % [mW/cm^3] %
            Pv_function2 = @(B, f) (B*10)^2.150*(5.101*(f*1e-3) + ...
                0.1561*(f*1e-3)^1.822);
            % ^^ Power loss for grid-side inductor % [mW/cm^3] %
            Method = 1;
    elseif strcmpi(txt_dataToroidal(i+1,9), 'FE SI')
            % Use the Pv_FESI function (Magnetic characteristics)
```

```
            Pv_function=@(Br,fsw)(Br*10)^2.295*(8.884*(fsw*1e-3) + ...
                0.0625*(fsw*1e-3)^1.982);
            % ^^ Power loss for inverter-side inductor % [mW/cm^3] %
            Pv_function2 = @(B,f) (B*10)^2.295*(8.884*(f*1e-3)+ ...
                0.0625*(f*1e-3)^1.982);
            % ^^ Power loss for grid-side inductor % [mW/cm^3] %
            Method = 1;
    elseif strcmpi(txt_dataToroidal(i+1,9), 'N87')
            % Use the Pv_N87 function (Magnetic characteristics)
            Pv_function = @(Br,fsw) 3.47816153320305e-05 * ...
                (fsw*1e-3)^1.63492941721237*(Br)^2.25271092818147; ...
                % ^^ Power loss for inverter-side inductor % [W/kg] %
            Pv_function2 = @(B,f) 3.47816153320305e-05* ...
                (f*1e-3)^1.63492941721237*(B)^2.25271092818147;
            % ^^ Power loss for grid-side inductor % [W/kg] %
            Method = 2;
    else
            error('No valid core loss function.');
    end

%%% Calculate Pv using the chosen function %%%
        Pv_L1a = Pv_function(B_L1r, fsw);
        Pv_L1b = Pv_function2(B_L1, f);
        Pv_L1 = Pv_L1a + Pv_L1b;
        % ^^ Loss per effective volume [mW/cm^3]
        Pv_L2a = Pv_function(B_L2r, fsw);
        Pv_L2b = Pv_function2(B_L2, f);
        Pv_L2 = Pv_L2a + Pv_L2b;
        % ^^ Loss per effective volume [mW/cm^3]

    if Method == 1
        Pv_core_L1 = (Pv_L1 * Ve*1e6)*1e-3;    % Core losses [W]
        Pv_core_L2 = (Pv_L2 * Ve*1e6)*1e-3;    % Core losses [W]
    elseif Method == 2
        Pv_core_L1 = (Pv_L1 * M*1e-3);    % Core losses [W]
        Pv_core_L2 = (Pv_L2 * M*1e-3);    % Core losses [W]
    end
    VolumeFilter = ...
        pi*((num_dataToriodal(i,9)/10)^2/4)*num_dataToriodal(i,10)/10;
    % ^^ cm^3 %Core "box" volume

%%% Calculate total inductor loss %%%
    P_L1 = Pv_core_L1 + Pv_winding_L1;
    % ^^ Inverter-side inductor power loss [W]
    P_L2 = Pv_core_L2 + Pv_winding_L2;
    % ^^ Grid-side inductor power loss [W]

%%% Save data for output %%%
    P_L_vector_L1Toroidal(i) = P_L1;
    P_L_vector_L2Toroidal(i) = P_L2;
    VolumeCore_vectorToroidal(i,1) = VolumeFilter;
    VolumeCu_L1_vectorToroidal(i,1) = V_copper_L1;
    VolumeCu_L2_vectorToroidal(i,1) = V_copper_L2;
    M_Cu_filter_L1_vectorToroidal(i,1) = M_copper_L1;
```

```
    M_Cu_filter_L2_vectorToroidal(i,1) = M_copper_L2;
    BsatCheck_L1vectorToroidal(i,1) = Bsat>B_L1;
    BsatCheck_L2vectorToroidal(i,1) = Bsat>B_L2;
    ApCheck_L1vectorToroidal(i,1) = Ap>Apreq_L1;
    ApCheck_L2vectorToroidal(i,1) = Ap>Apreq_L2;
    WaCheck_L1vectorToroidal(i,1) = Aw>Awind_L1;
    WaCheck_L2vectorToroidal(i,1) = Aw>Awind_L2;
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%% Design of filter inductors with E-cores %%%
for i = 1:nDataE
    % Core Parameters (Datasheet)
    Al = num_dataE(i,1);            % [H/turn]
    ur = num_dataE(i,2);            % Relative permeability
    le = num_dataE(i,3);            % Effective length [m]
    Ve = num_dataE(i,4);            % Effective volume [m^3]
    M = num_dataE(i,5);             % Mass [kg]
    Bsat = num_dataE(i,6);          % Saturation flux density [T]
    Ae = num_dataE(i,7);            % Effective core area [m^2]
    Ww = num_dataE(i,9);            % Window width [m]
    Wh = num_dataE(i,10)*2;          % Total window height [m]
    Cpw = num_dataE(i,11);          % Center-post width [m]
    Cw = num_dataE(i,12);           % Core width [m]
    Cl = num_dataE(i,13);           % Core length [m]
    Ch = num_dataE(i,14)*2;         % Total core height [m]
    % Core calculations
    Kw = 0.5;                       % Window utilization factor
    u_core = ur * 4 * pi * 10^-7;   % Permeability [H/m]
    Aw = Ww*Wh;                     % Window area [m^2]
    Ap = Aw*Ae;                     % Area product of core [m^4]
    % Wire Parameters
    Nw = 0;                         % "Initial" number of wires per winding
    J = 100;
    while J>Jmax
        r_L = 10.44;      % Wire resistivity AWG 15 [ohm/km]
        AWG = 15;
        A = 1.65; % mm^2
        Nw = Nw+1;
        Awire = A*Nw;
        J = I_o/Awire;
    end
    J = J*1e6;
    Awire = Awire*1e-6;
    WcoreL1 = (1/2)*L_1*I_max^2;
    WcoreL2 = (1/2)*L_2*I_max^2;

%%% Inductor Conduction Power Loss Calculations %%%
    N_L1 = sqrt(L_1/Al);
    % ^^ Number of turns
    N_L2 = sqrt(L_2/Al);
    % ^^ Number of turns
    Awind_L1 = Awire*N_L1/Kw;
    % ^^ Area in the window which is taken up by the windings L1
```

```
    Awind_L2 = Awire*N_L2/Kw;
    % ^^ Area in the window which is taken up by the windings L2
    B_L1 = ( u_core*N_L1*I_max) / le;
    % ^^ Fundamental magnetic flux density inverter inductor [Wb/m^2]
    B_L1r = ( u_core*N_L1*I_max*0.2) / le;
    % ^^ Ripple magnetic flux density inverter inductor [Wb/m^2]
    B_L2 = (u_core*N_L2*I_max) / le;
    % ^^ Fundamental magnetic flux density grid inductor [Wb/m^2]
    B_L2r = (u_core*N_L2*I_max*0.2) / le;
    % ^^ Ripple magnetic flux density grid inductor [Wb/m^2]
    Apreq_L1 = 2*WcoreL1/(B_L1*J*Kw);
    % ^^ Required area product for L1 [m^4]
    Apreq_L2 = 2*WcoreL2/(B_L1*J*Kw);
    % ^^ Required area product for L2 [m^4]
    K = 2*(Cw+Cpw)*1e-3;
    % ^^ Wire length per turn(circumference core) [km/Turn]
    l_L1 = N_L1 * K * Nw;
    % ^^ Wire length inverter inductor [km]
    l_L2 = N_L2 * K * Nw;
    % ^^ Wire length grid inductor [km]
    R_L1 = r_L * l_L1;
    % ^^ Inductor resistance [ohm]
    R_L2 = r_L * l_L2;
    % ^^ Inductor resistance [ohm]
    Pv_winding_L1 = Is_rms^2*R_L1;
    % ^^ Inductor conduction losses [W]
    Pv_winding_L2 = Is_rms^2*R_L2;
    % ^^ Inductor conduction losses [W]
    V_copper_L1 = (l_L1)*1e6*A;
    % ^^ mm^3
    V_copper_L2 = (l_L2)*1e6*A;
    % ^^ mm^3
    M_copper_L1 = V_copper_L1*rho_copper;
    % ^^ mg
    M_copper_L2 = V_copper_L2*rho_copper;
    % ^^ mg

%%% Checking flux density saturation %%%
    if Bsat < B_L1
            fprintf(['\nE-core number %.0f in the database can not ' ...
                'handle the flux density \nat fsw = %d kHz, and ' ...
                'Is_rms = %.1f A. A larger core is required \n' ...
                'at this switching frequency and current for the' ...
                ' inverter-side inductor.\n\n'], i, fsw*1e-3, Is_rms)
    else
            fprintf(['\nWindings for inductor L1 / length of ' ...
                'required wire / wire gauge\nfor E-core number' ...
                ' %d %s: \n%.2f [dim] / %.2f [m] / %.2f\n'], ...
                i,txt_wo_headerE{i,1},N_L1,l_L1*1e3,AWG)
    end

    if Bsat < B_L2
            fprintf(['\nE-core number %.0f in the database can not ' ...
                'handle the flux density \nat fsw = %d kHz, ' ...
```

```
                'and Is_rms = %.1f A. A larger core is required \n' ...
                'at this switching frequency and current for the ' ...
                'grid-side inductor.\n\n'], i, fsw*1e-3, Is_rms)
    else
            fprintf(['\nWindings for inductor L2 / length of ' ...
                'required wire / wire gauge \nfor E-core number ' ...
                '%d %s:\n%.2f [dim] / %.2f[m] / %.2f\n\n'], ...
                i,txt_wo_headerE{i,1},N_L2,l_L2*1e3,AWG)
    end

%%% Chooses the appropriate calculation based on the Material %%%
    if strcmpi(txt_dataE(i+1,9), 'KoolMU')
        % Use the KoolMU function (Magnetic characteristics)
        if num_dataE(i,2) == 14
            Pv_function = @(Br,fsw) 29.3*(Br)^1.988*(fsw*1e-3)^1.541;
                % ^^ Power loss for high-frequency % [mW/cm^3]%
            Pv_function2 = @(B,f) 29.3*(B)^1.988*(f*1e-3)^1.541;
                % ^^ Power loss for low-frequency % % [mW/cm^3] %
        elseif num_dataE(i,2) == 26
            Pv_function = @(Br,fsw) 32.22*(Br)^1.988*(fsw*1e-3)^1.541;
                % ^^ Power loss for high-frequency % % [mW/cm^3]%
            Pv_function2 = @(B,f) 32.22*(B)^1.988*(f*1e-3)^1.541;
                % ^^ Power loss for low-frequency % [mW/cm^3] %
        elseif num_dataE(i,2) == 40
            Pv_function = @(Br,fsw) 32.22*(Br)^1.988*(fsw*1e-3)^1.541;
                % ^^ Power loss for high-frequency % % [mW/cm^3]%
            Pv_function2 = @(B,f) 32.22*(B)^1.988*(f*1e-3)^1.541;
                % ^^ Power loss for low-frequency % [mW/cm^3] %
        elseif num_dataE(i,2) == 60
            Pv_function = @(Br,fsw) 40.27*(Br)^1.988*(fsw*1e-3)^1.541;
                % ^^ Power loss for high-frequency % % [mW/cm^3]%
            Pv_function2 = @(B,f) 40.27*(B)^1.988*(f*1e-3)^1.541;
                % ^^ Power loss for low-frequency % [mW/cm^3] %
        elseif num_dataE(i,2) == 90
            Pv_function = @(Br,fsw) 40.27*(Br)^1.988*(fsw*1e-3)^1.541;
                % ^^ Power loss for high-frequency % [mW/cm^3]%
            Pv_function2 = @(B,f) 40.27*(B)^1.988*(f*1e-3)^1.541;
                % ^^ Power loss for low-frequency % [mW/cm^3] %
        end
            Method = 1;
    elseif strcmpi(txt_dataE(i+1,9), 'Xflux')
        % Use the KoolMU function (Magnetic characteristics)
        if num_dataE(i,2) == 26
            Pv_function = @(Br,fsw) 379*(Br)^1.995*(fsw*1e-3)^1.33;
                % ^^ Power loss for high-frequency % [mW/cm^3]%
            Pv_function2 = @(B,f) 379*(B)^1.995*(f*1e-3)^1.33;
                % ^^ Power loss for low-frequency % [mW/cm^3] %
        elseif num_dataE(i,2) == 40
            Pv_function = @(Br,fsw) 441*(Br)^2.16*(fsw*1e-3)^1.35;
                % ^^ Power loss for high-frequency % [mW/cm^3]%
            Pv_function2 = @(B,f) 441*(B)^2.16*(f*1e-3)^1.35;
                % ^^ Power loss for low-frequency % [mW/cm^3] %
        elseif num_dataE(i,2) == 60
            Pv_function = @(Br,fsw) 441*(Br)^2.16*(fsw*1e-3)^1.35;
```

```
                % ^^ Power loss for high-frequency % [mW/cm^3]%
            Pv_function2 = @(B,f) 441*(B)^2.16*(f*1e-3)^1.35;
                % ^^ Power loss for low-frequency % [mW/cm^3] %
        end
            Method = 1;
    else
            error('No valid core-loss function.');
    end

%%% Calculate Pv using the chosen function %%%
        Pv_L1a = Pv_function(B_L1r, fsw);
        Pv_L1b = Pv_function2(B_L1, f*10^-3);
        Pv_L1 = Pv_L1a + Pv_L1b;
        % ^^ Loss per effective volume [mW/cm^3]
        Pv_L2a = Pv_function(B_L2r, fsw);
        Pv_L2b = Pv_function2(B_L2, f*10^-3);
        Pv_L2 = Pv_L2a + Pv_L2b;
        % ^^ Loss per effective volume [mW/cm^3]

    if Method == 1
        Pv_core_L1 = (Pv_L1 * Ve*1e6)*1e-3;    % Core losses [W]
        Pv_core_L2 = (Pv_L2 * Ve*1e6)*1e-3;    % Core losses [W]
    end
    VolumeFilter = (Cw/10) * (Cl/10) * (Ch/10);
    % ^^ cm^3 %Core box volume

%%% Calculate total inductor loss %%%
    P_L1 = Pv_core_L1 + Pv_winding_L1;
    % ^^ Inverter-side inductor power loss [W]
    P_L2 = Pv_core_L2 + Pv_winding_L2;
    % ^^ Grid-side inductor power loss [W]

%%% Save data for output %%%
    P_L_vector_L1E(i) = P_L1;
    P_L_vector_L2E(i) = P_L2;
    VolumeCore_vectorE(i,1) = VolumeFilter;
    VolumeCu_L1_vectorE(i,1) = V_copper_L1;
    VolumeCu_L2_vectorE(i,1) = V_copper_L2;
    M_Cu_filter_L1_vectorE(i,1) = M_copper_L1;
    M_Cu_filter_L2_vectorE(i,1) = M_copper_L2;
    BsatCheck_L1vectorE(i,1) = Bsat>B_L1;
    BsatCheck_L2vectorE(i,1) = Bsat>B_L2;
    ApCheck_L1vectorE(i,1) = Ap>Apreq_L1;
    ApCheck_L2vectorE(i,1) = Ap>Apreq_L2;
    WaCheck_L1vectorE(i,1) = Aw>Awind_L1;
    WaCheck_L2vectorE(i,1) = Aw>Awind_L2;
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

P_L_vector_L1 = [P_L_vector_L1Toroidal;P_L_vector_L1E];
P_L_vector_L2 = [P_L_vector_L2Toroidal;P_L_vector_L2E];
VolumeCore_vector = [VolumeCore_vectorToroidal;VolumeCore_vectorE];
FilterName = [FilterNameToroidal;FilterNameE];
VolumeCu_L1_vector = [VolumeCu_L1_vectorToroidal;VolumeCu_L1_vectorE];
```

```
VolumeCu_L2_vector = [VolumeCu_L2_vectorToroidal;VolumeCu_L2_vectorE];
M_Cu_filter_L1_vector = [M_Cu_filter_L1_vectorToroidal;
                         M_Cu_filter_L1_vectorE];
M_Cu_filter_L2_vector = [M_Cu_filter_L2_vectorToroidal;
                         M_Cu_filter_L2_vectorE];
BsatCheck_L1vector = [BsatCheck_L1vectorToroidal;BsatCheck_L1vectorE];
BsatCheck_L2vector = [BsatCheck_L2vectorToroidal;BsatCheck_L2vectorE];
ApCheck_L1vector = [ApCheck_L1vectorToroidal;ApCheck_L1vectorE];
ApCheck_L2vector = [ApCheck_L2vectorToroidal;ApCheck_L2vectorE];
WaCheck_L1vector = [WaCheck_L1vectorToroidal;WaCheck_L1vectorE];
WaCheck_L2vector = [WaCheck_L2vectorToroidal;WaCheck_L2vectorE];
```

L.4 Pareto Optimization Script

The following script to be called 'ParetoOptimization_JointRecyc.m'.

```
function [tPassed_min,tPassed_sec,results,paretoResults, ...
    MultiObjectiveSolutionEntry,WeightedVector,CompResults] = ...
    ParetoOptimization_JointRecyc(nfsw_SiC,nCores,nSiC1200, ...
    CapDataOutput,CoreDataOutput,SwitchRecycDataOutput,...
    BigDataMatrix,P_in,w,WeightStepSize)
tic;
tstart = tic;
nCombs = nfsw_SiC*nCores^2*nSiC1200;
Combinations = zeros(nfsw_SiC*nCores^2*nSiC1200,13);
nObjectives = 3;

file = 'Database.xlsx';
% Load Material Recyclability
RecycCoefficients = 'MaterialRecycCoefficients';
[MaterialRecycCoefficients_data, MaterialRecycCoefficients_txt] = ...
    xlsread(file, RecycCoefficients); %#ok<*XLSRD>
nMaterials = width(MaterialRecycCoefficients_data);
for u = 1:nMaterials
    if strcmpi(MaterialRecycCoefficients_txt(u),'Cu')
        RecCopper = MaterialRecycCoefficients_data(u);
    elseif strcmpi(MaterialRecycCoefficients_txt(u),'Fe')
        RecIron = MaterialRecycCoefficients_data(u);
    elseif strcmpi(MaterialRecycCoefficients_txt(u),'Al')
        RecAlu = MaterialRecycCoefficients_data(u);
    end
end

% Generate pareto front, find utopia point, use euclidain distance from
% utopia point to pareto front to find compromise solution and use this as
% the point

% Pareto front:
% Make a loop which finds the dominating/non-dominated points.
% Generate all combinations
for i = 1:nfsw_SiC
% ^^ Cycles switching frequencies
Number_Cap_DC_fast =  BigDataMatrix(1 + (i-1)*nCores*nSiC1200,19);
Volume_Cap_DC_fast =  BigDataMatrix(1 + (i-1)*nCores*nSiC1200,21);
Series_Cap_DC_fast =  BigDataMatrix(1 + (i-1)*nCores*nSiC1200,22);
Parallel_Cap_DC_fast =  BigDataMatrix(1 + (i-1)*nCores*nSiC1200,23);
    for j = 1:nSiC1200
    % ^^ Cycles all switches
        PowerLossSwitch = BigDataMatrix(...
            1 + (i-1)*nCores*nSiC1200 + (j-1)*nCores,3);
        % ^^ Load switch power loss volume for present combination
        VolumeHS = BigDataMatrix(...
            1 + (i-1)*nCores*nSiC1200 + (j-1)*nCores,4);
        % ^^ Load heatsink volume for present combination

        for k = 1:nCores
        % ^^ Cycles inverter-side inductor core options
```

```
            PowerLossL1 = BigDataMatrix( (i-1)*nCores*nSiC1200 + k,16);
            % ^^ Load power loss of L1 for present combination containing
            % core and wire volumes
            VolumeL1 = BigDataMatrix(...
                (i-1)*nCores*nSiC1200+k,8)+CoreDataOutput(k,3);
            % ^^ Load total volume of L1 for present combination with core
            % and wire volumes

            for l = 1:nCores
            % ^^ Cycles grid-side inductor core options
                PowerLossL2 = BigDataMatrix( (i-1)*nCores*nSiC1200 + l,18);
                % ^^ Load power loss of L2 for present combination
                % containing core and wire volumes

                PowerLoss = PowerLossSwitch + PowerLossL1 + PowerLossL2;
                % ^^ Calculate total power loss for present combination

                Efficiency = 100*(P_in-PowerLoss)/P_in;
                % ^^ Calculate total efficiency for present combination

                VolumeL2 = BigDataMatrix(...
                    (i-1)*nCores*nSiC1200 + k,11) + CoreDataOutput(l,3);
                % ^^ Load total volume of L2 for present combination with
                % core and wire volumes

                Volume = VolumeHS + VolumeL1 + VolumeL2 + ...
                    CapDataOutput(1,2) + CapDataOutput(1,4) + ...
                    Volume_Cap_DC_fast;
                % ^^ Calculate total volume of the present combination

                PD = P_in/Volume;
                % ^^ Calculate power density of the present combination

                AluMass = BigDataMatrix( 1 + (i-1)*nCores*nSiC1200 + ...
                    (j-1)*nCores,5);
                % ^^ Load mass of aluminium (heatsink) of the present
                % combination (caps are not included in current version)

                Ind1Dis = CoreDataOutput(k,4);
                % ^^ Disassmblibility factor of inductor 1

                Ind2Dis = CoreDataOutput(l,4);
                % ^^ Disassmblibility factor of inductor 2

               if Ind1Dis == 0
                    RecycCopperMass1 = ...
                        BigDataMatrix((i-1)*nCores*nSiC1200 + k,7) * 0.28;
                elseif Ind1Dis == 1
                    RecycCopperMass1 = ...
                        BigDataMatrix((i-1)*nCores*nSiC1200 + k,7) * 0.6;
                end
                if Ind2Dis == 0
                    RecycCopperMass2 = ...
                        BigDataMatrix((i-1)*nCores*nSiC1200 + k,10) * 0.28;
```

```
                elseif Ind2Dis == 1
                    RecycCopperMass2 = ...
                        BigDataMatrix((i-1)*nCores*nSiC1200 + k,10) * 0.6;
                end
                RecycCopperMass = RecycCopperMass1+RecycCopperMass2;
                % ^^ Calculate mass of iron of the present combination

                CopperMass = ...
                    BigDataMatrix((i-1)*nCores*nSiC1200 + k,7) + ...
                    BigDataMatrix((i-1)*nCores*nSiC1200 + l,10);
                % ^^ Calculate mass of copper of the present combination

                if Ind1Dis == 0
                    RecycIronMass1 = CoreDataOutput(k,2) * 0.5;
                elseif Ind1Dis == 1
                    RecycIronMass1 = CoreDataOutput(k,2) * 0.62;
                end
                if Ind2Dis == 0
                    RecycIronMass2 = CoreDataOutput(l,2) * 0.5;
                elseif Ind2Dis == 1
                    RecycIronMass2 = CoreDataOutput(k,2) * 0.62;
                end
                RecycIronMass = RecycIronMass1+RecycIronMass2;
                % ^^ Calculate mass of iron of the present combination

                IronMass = CoreDataOutput(k,2) + CoreDataOutput(l,2);
                % ^^ Calculate mass of iron of the present combination

                SwitchMass = SwitchRecycDataOutput(j,2)/1e6;
                % ^^ Load switch mass of the present combination in kg

                BigMass = AluMass + CopperMass + IronMass;
                % ^^Calculate mass of large components in kg:
                % Heatsink and inductors

                TotalMass = SwitchMass + BigMass;
                % ^^ Total mass of all components in kg

                SwitchRecycMass = SwitchRecycDataOutput(j,1)/1e6;
                % ^^ Recyclable mass from small component in kg:
                % Switches

                BigRecycMass = AluMass*RecAlu + ...
                    RecycCopperMass + RecycIronMass;
                % ^^Recyclable mass from large component in kg:
                % Heatsink and inductors

                TotalRecycMass = SwitchRecycMass+BigRecycMass;
                % ^^ Total recyclable mass of all components in kg

                %%% Begin saving data into huge data matrix %%%
                Combinations(1 + (i-1)*nSiC1200*nCores*nCores + ...
                    (j-1)*nCores*nCores + (k-1)*nCores + (l-1),1) = (i+9);
                % ^^ Save switching frequency into huge output matrix
```

```
160
161                 Combinations(1 + (i-1)*nSiC1200*nCores*nCores + ...
162                     (j-1)*nCores*nCores + (k-1)*nCores + (l-1),2) = j;
163                 % ^^ Save switch number into huge output matrix
164
165                 Combinations(1 + (i-1)*nSiC1200*nCores*nCores + ...
166                     (j-1)*nCores*nCores + (k-1)*nCores + (l-1),3)=VolumeHS;
167                 % ^^ Save the heatsink volume at the present combination to
168                 % the huge combination matrix
169
170                 Combinations(1 + (i-1)*nSiC1200*nCores*nCores + ...
171                     (j-1)*nCores*nCores + (k-1)*nCores + (l-1),4) = k;
172                 % ^^ Save core number for L1 into huge output matrix
173
174                 Combinations(1 + (i-1)*nSiC1200*nCores*nCores + ...
175                     (j-1)*nCores*nCores + (k-1)*nCores + (l-1),5) = ...
176                     BigDataMatrix( (i-1)*nCores*nSiC1200 + k,9);
177                 % ^^ Save core saturation check for L1 huge output matrix
178
179                 Combinations(1 + (i-1)*nSiC1200*nCores*nCores + ...
180                     (j-1)*nCores*nCores + (k-1)*nCores + (l-1),6) = l;
181                 % ^^ Save core number for L2 huge output matrix
182
183                 Combinations(1 + (i-1)*nSiC1200*nCores*nCores + ...
184                     (j-1)*nCores*nCores + (k-1)*nCores + (l-1),7) = ...
185                     BigDataMatrix( (i-1)*nCores*nSiC1200 + l,12);
186                 % ^^ Save core saturation check for L2 huge output matrix
187
188                 Combinations(1 + (i-1)*nSiC1200*nCores*nCores + ...
189                     (j-1)*nCores*nCores + (k-1)*nCores + (l-1),8) = ...
190                     Number_Cap_DC_fast;
191                 % ^^ Save the entry of the fast dc-link capacitor used at
192                 % the present combination to the huge combination matrix
193
194                 Combinations(1 + (i-1)*nSiC1200*nCores*nCores + ...
195                     (j-1)*nCores*nCores + (k-1)*nCores + (l-1),9) = ...
196                     Series_Cap_DC_fast;
197                 % ^^ Save the number of the fast dc-link capacitor used in
198                 % series for the present combination
199
200                 Combinations(1 + (i-1)*nSiC1200*nCores*nCores + ...
201                     (j-1)*nCores*nCores + (k-1)*nCores + (l-1),10) = ...
202                     Parallel_Cap_DC_fast;
203                 % ^^ Save the number of the fast dc-link capacitor used in
204                 % parallel for the present combination
205
206                 Combinations(1 + (i-1)*nSiC1200*nCores*nCores + ...
207                     (j-1)*nCores*nCores + (k-1)*nCores + (l-1),11) = ...
208                     Efficiency;
209                 % ^^ Save the efficiency at the present combination to the
210                 % huge combination matrix
211
212                 Combinations(1 + (i-1)*nSiC1200*nCores*nCores + ...
213                     (j-1)*nCores*nCores + (k-1)*nCores + (l-1),12) = PD;
```

```
                % ^^ Save the power density at the present combination to
                % the huge combination matrix

                Combinations(1 + (i-1)*nSiC1200*nCores*nCores + ...
                    (j-1)*nCores*nCores + (k-1)*nCores + (l-1),13) = ...
                    100*TotalRecycMass/TotalMass;
                % ^^ Save the total component recyclability of the present
                % combination to the huge combination matrix

            end
        end
    end
end
Old_nCombs = length(Combinations);
% Combinations
k = 0;
for i = 1:nCombs
    k = k+1;
    if Combinations(k,3) == 0 || Combinations(k,5) == 0 || ...
            Combinations(k,7) == 0
        Combinations(k,:)=[];
        k = k-1;
    end
end
results = Combinations;
HeatsinkVolumes = results(:,3);
results(:,7) = [];
results(:,5) = [];
results(:,3) = [];
New_nCombs = length(results);
% results
nRemoved = Old_nCombs-New_nCombs;
fprintf(['\nNumber of invalid combinations removed = %.2f,\n' ...
    'New amount of combinations = %.2f\n\n'],nRemoved,New_nCombs)

[HighestEff, HighestEffLocation] = max(results(:,8));
[HighestPD, HighestPDLocation] = max(results(:,9));
[HighestRecyc, HighestRecycLocation] = max(results(:,10));

fprintf(['fsw = %.2f kHz, switch %d, and cores %d and\n' ...
    '%d result in highest efficiency.\n' ...
    'This is using the %.2f litre heatsink\n\n'], ...
    results(HighestEffLocation,1),results(HighestEffLocation,2), ...
    results(HighestEffLocation,3),results(HighestEffLocation,4), ...
    HeatsinkVolumes(HighestEffLocation))


fprintf(['fsw = %.2f kHz, switch %d, and cores %d and\n' ...
    '%d result in highest power density.\n' ...
    'This is using the %.2f litre heatsink\n\n'], ...
    results(HighestPDLocation,1),results(HighestPDLocation,2), ...
    results(HighestPDLocation,3),results(HighestPDLocation,4), ...
    HeatsinkVolumes(HighestPDLocation))

```

```
fprintf(['fsw = %.2f kHz, switch %d, and cores %d and\n' ...
    '%d result in highest big component recyclability.\n' ...
    'This is using the %.2f litre heatsink\n\n'], ...
    results(HighestRecycLocation,1),results(HighestRecycLocation,2), ...
    results(HighestRecycLocation,3),results(HighestRecycLocation,4), ...
    HeatsinkVolumes(HighestRecycLocation))

% Find the utopia point
Utopia = [HighestEff,HighestPD,HighestRecyc]

data = [results(:,8),results(:,9),results(:,10)];
% Get the number of points
numPoints = size(data, 1);

% Initialize a logical array to track non-dominated points
paretoMask = true(numPoints, 1);

% Compare each point with all others
for i = 1:numPoints
    for j = 1:numPoints
        if i ~= j
% Domination check:
% partially better all objectives && strictly better at least one objective
            if all(data(j,:) >= data(i,:)) && any(data(j,:) > data(i,:))
                paretoMask(i) = false;  % Mark as dominated
                break;
            end
        end
    end
end

% Extract Pareto-optimal points with their entry numbers
paretoIndices = find(paretoMask); % Get indices of Pareto-optimal points
paretoPoints = data(paretoMask, :); % Get Pareto-optimal points
nPareto = length(paretoPoints);

% Combine entry numbers with Pareto-optimal points
paretoResults = [(paretoIndices), paretoPoints];

%Generate the combination list for the Pareto-optimal points
Comb = [results(paretoResults(:,1),1), results(paretoResults(:,1),2), ...
        results(paretoResults(:,1),3), results(paretoResults(:,1),4)];

% Find the Compromise solution
D_best = 1e9;
for i = 1:nPareto
    D = sqrt((1-paretoPoints(i,1)/Utopia(1,1))^2 + ...
             (1-paretoPoints(i,2)/Utopia(1,2))^2 + ...
             (1-paretoPoints(i,3)/Utopia(1,3))^2);
    if D < D_best
        D_best = D;
        CompEntry = paretoIndices(i);
        CompComb = Comb(i,:);
        CompPoint = paretoResults(i,:);
```

```
    end
end

CompResults = [CompComb;CompPoint];
CompromiseLine = [Utopia(1,2)/1e3 Utopia(1,1)
                  CompResults(2,3)/1e3 CompResults(2,2)];

CompromiseLine3D = [Utopia(1,1) Utopia(1,2)/1e3  Utopia(1,3);
                    CompResults(2,2) CompResults(2,3)/1e3 CompResults(2,4)];

% 3D pareto plot with front %
figure;
scatter3(data(:,3), data(:,2)/1e3, data(:,1), 50, 'r', 'filled');
hold on
scatter3(Utopia(1,3), Utopia(1,2)/1e3, Utopia(1,1), 50, 'g', 'filled');
scatter3(paretoPoints(:,3),paretoPoints(:,2)/1e3,paretoPoints(:,1),...
    80, 'b','filled')

% Create a Pareto front surface using Delaunay triangulation:
if size(paretoPoints, 1) >= 3
    tri = delaunay(paretoPoints(:,3), paretoPoints(:,2)/1e3);
    trisurf(tri,paretoPoints(:,3),paretoPoints(:,2)/1e3, ...
        paretoPoints(:,1),'FaceAlpha',0.5,'EdgeColor','none', ...
        'FaceColor','cyan');
end
plot3(CompromiseLine3D(:,3),CompromiseLine3D(:,2),CompromiseLine3D(:,1))
% Labels and Formatting
zlabel('Efficiency');
ylabel('Power density [kW/L]');
xlabel('Recyclability');
title('Pareto Front');
legend('All Points','Utopia Point', 'Pareto-Optimal Points', ...
    'Pareto Front Surface','Utopia/Compromise Distance');
colormap('cool');
set(gca, 'YDir', 'reverse')
hold off;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% 3D pareto plot with front, only pareto points %
figure;
scatter3(Utopia(1,3), Utopia(1,2)/1e3, Utopia(1,1), 50, 'g', 'filled');
hold on
scatter3(paretoPoints(:,3),paretoPoints(:,2)/1e3,paretoPoints(:,1),...
    80, 'b','filled')

% Create a Pareto front surface using Delaunay triangulation:
if size(paretoPoints, 1) >= 3
    tri = delaunay(paretoPoints(:,3), paretoPoints(:,2)/1e3);
    trisurf(tri,paretoPoints(:,3),paretoPoints(:,2)/1e3, ...
        paretoPoints(:,1),'FaceAlpha',0.5,'EdgeColor','none', ...
        'FaceColor','cyan');
end
plot3(CompromiseLine3D(:,3),CompromiseLine3D(:,2),CompromiseLine3D(:,1))
% Labels and Formatting
```

```
zlabel('Efficiency');
ylabel('Power density [kW/L]');
xlabel('Recyclability');
title('Pareto Front');
legend('All Points','Utopia Point', 'Pareto-Optimal Points', ...
    'Pareto Front Surface','Utopia/Compromise Distance');
colormap('cool');
set(gca, 'YDir', 'reverse')
hold off;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% 3D pareto plot without front %
figure;
scatter3(data(:,3), data(:,2)/1e3, data(:,1), 50, 'r', 'filled');
hold on
scatter3(Utopia(1,3), Utopia(1,2)/1e3, Utopia(1,1), 50, 'g', 'filled');
scatter3(paretoPoints(:,3),paretoPoints(:,2)/1e3,paretoPoints(:,1),...
    80, 'b','filled')
plot3(CompromiseLine3D(:,3),CompromiseLine3D(:,2),CompromiseLine3D(:,1))
% Labels and Formatting
zlabel('Efficiency');
ylabel('Power density [kW/L]');
xlabel('Recyclability');
title('Pareto Front');
legend('All Points','Utopia Point', 'Pareto-Optimal Points', ...
    'Utopia/Compromise Distance');
colormap('cool');
set(gca, 'YDir', 'reverse')
hold off;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% 2D plot with 3D pareto front %
figure
plot(paretoPoints(:,2)/1e3,paretoPoints(:,1),'o-')
hold on
plot(data(:,2)/1e3,data(:,1),'+')
plot(Utopia(1,2)/1e3,Utopia(1,1),'xg')
plot(CompromiseLine(:,1),CompromiseLine(:,2))
title('3D but 2D')
xlabel('Power Density [kW/L]')
ylabel('Efficiency')
hold off
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

NormalizedParetoPoints = [paretoPoints(:,1)/HighestEff ...
    paretoPoints(:,2)/HighestPD paretoPoints(:,3)/HighestRecyc];

Cost = w(1,1)*NormalizedParetoPoints(:,1) + ...
       w(1,2)*NormalizedParetoPoints(:,2) + ...
       w(1,3)*NormalizedParetoPoints(:,3);
[MultiObjectiveSolution, MultiObjectiveSolutionEntry] = max(Cost);

k = 1/WeightStepSize;
% "Ordnet uden tilbagelaegning":
```

```
nWeightStep = ...
      factorial(nObjectives+k-1)/(factorial(k)*(factorial(nObjectives-1)));

SweepEntryVector = zeros(nWeightStep,1);
CostSweep = zeros(nWeightStep,3);
WeightingValueVector = zeros(nWeightStep,3);
i = 0;
for i1 = 0:k
    x1 = i1 * WeightStepSize;
    for i2 = 0:(k - i1)
        x2 = i2 * WeightStepSize;
        x3 = 1 - (x1 + x2);  % Compute x3 directly to ensure sum = 1
        if x3 >= 0  % Ensure non-negative values
                i = i+1;
                [SweepValue, SweepEntry] = max(...
                    x1*NormalizedParetoPoints(:,1) + ...
                    x2*NormalizedParetoPoints(:,2) + ...
                    x3*NormalizedParetoPoints(:,3));
                WeightingValueVector(i,:) = [x1 x2 x3];
                % ^^ Saves the present weightings
                SweepEntryVector(i,:) = paretoIndices(SweepEntry);
                % ^^ Saves the combination number of the chosen pareto
                % point.
                CostSweep(i,:) = NormalizedParetoPoints(SweepEntry,:);
                % ^^ Saves the normalized value of the pareto points
        end
    end
end

paretoResults = [paretoResults(:,1), paretoResults(:,2), ...
    paretoResults(:,3)/1e3, paretoResults(:,4), ...
    Combinations(paretoIndices,1), Combinations(paretoIndices,2), ...
    Combinations(paretoIndices,3), Combinations(paretoIndices,4), ...
    Combinations(paretoIndices,6), Combinations(paretoIndices,8), ...
    Combinations(paretoIndices,9), Combinations(paretoIndices,10)] ;

WeightedVector = [WeightingValueVector ...
                  SweepEntryVector ...
                  CostSweep(:,1)*HighestEff ...
                  (CostSweep(:,2)*HighestPD)/1e3 ...
                  CostSweep(:,3)*HighestRecyc];
    k = 0;
    for n = 1:nWeightStep
        k = k+1;
        if WeightedVector(k,1) == 0 && ...
           WeightedVector(k,2) == 0 && ...
           WeightedVector(k,3) == 0
            WeightedVector(k,:)=[];
            k = k-1;
        end
    end
tPassed_sec = toc(tstart); % s %
tPassed_min = tPassed_sec/60; % min %
end
```

L.5 Three-Phase Inverter Switch Loss Script

The following script to be called 'SwitchLoss3phaseSiC.m'.

```
function [P_data,P_sw_losses_indv] = SwitchLoss3phaseSiC(Is_rms,V_dc,fsw,f,E0,E1,E2,Rds
    )
syms E_sw(I)
E_sw(I) = (E2*I^2+E1*I+E0)*1e-6; % J % Turn-on energies as a function of switch current
    .
P_sw_losses_indv = [0 0 0 0;0 0 0 0;0 0 0 0;0 0 0 0];

%%% "Constants" %%%
omega = 2*pi*f; % rad/s % angular frequency of grid
T = 1/f; % s %Fundamental period
T_2 = T/2; % s % Half the fundamental period
Vs_rms = 230; % V % % Fundamental voltage RMS
Vs_M = Vs_rms*sqrt(2);
Is_M = Is_rms*sqrt(2);
fsample = 1000*fsw; % Hz % Sample frequency
t = 0:(1/fsample):(T_2); % s % Discrete time points
isA = Is_rms * sqrt(2) * sin(2*pi*f*t); % Fundamental current waveform
isB = Is_rms * sqrt(2) * sin(2*pi*f*t + 2*pi/3); % Fundamental current waveform
isC = Is_rms * sqrt(2) * sin(2*pi*f*t - 2*pi/3); % Fundamental current waveform
Rdson_mean = Rds;

%%% Initialize P_tot variables %%
P_turnsw = 0;
P_condsw = 0;
P_condmean = 0;
P_condRMS = 0;
E_cond = 0;

%%% PWM generation %%%
duty_cycle = 0.5; % dim % Duty cycle for the carrier. Desides the shape, 0.5 is
    triangular, 1 is sawtooth
carrier = (sawtooth(2*pi*fsw*t, duty_cycle)+1)/2; % Carrier waveform for MOSFET w. off-
    set
M_i = Vs_M/V_dc; % dim % Modulation index

%%% Power loss calculation based on different carrier- and modulations waves rotated by
     pi %%%
for j = 0:1:5
    if j == 0
        reference = (M_i * sin(2 * pi * f * t ) + 1) / 2; % Sinusoidal modulation
    waveform
        pulse_signal = reference > carrier; % Gate pulse for switch
        rising_edges = find(diff(pulse_signal) == 1); % dim % Discrete turn-on
    instances (vector)                                  (for time domain mulitply by
    sample frequency)
        t_r = rising_edges/fsample;
        falling_edges = find(diff(pulse_signal) == -1); % dim % Discrete turn-off
    instances (vector)                                (for time domain mulitply by sample
    frequency)
        t_f = falling_edges/fsample;
```

```
41        num_rising_edges = length(rising_edges); % dim % Number of rising edges/turn
    ons (vector)
42        num_falling_edges = length(falling_edges); % dim % Number of falling edges/turn
     offs (vector)
43        is_rising_edges(1:num_rising_edges) = isA(rising_edges); % A % Instantaneous
    currents at turn-on instants (vector)
44        is_falling_edges(1:num_falling_edges) = isA(falling_edges); % A % Instantaneous
     currents at turn-off instants (vector)
45    elseif j==1
46        reference = (M_i * sin(2 * pi * f * t ) + 1) / 2; % Sinusoidal modulation
    waveform
47        pulse_signal = reference < carrier; % Gate pulse for switch
48        rising_edges = find(diff(pulse_signal) == 1); % dim % Discrete turn-on
    instances (vector)                                (for time domain mulitply by
    sample frequency)
49        t_r = rising_edges/fsample;
50        falling_edges = find(diff(pulse_signal) == -1); % dim % Discrete turn-off
    instances (vector)                               (for time domain mulitply by sample
    frequency)
51        t_f = falling_edges/fsample;
52        num_rising_edges = length(rising_edges); % dim % Number of rising edges/turn
    ons (vector)
53        num_falling_edges = length(falling_edges); % dim % Number of falling edges/turn
     offs (vector)
54        is_rising_edges(1:num_rising_edges) = isA(rising_edges); % A % Instantaneous
    currents at turn-on instants (vector)
55        is_falling_edges(1:num_falling_edges) = isA(falling_edges); % A % Instantaneous
     currents at turn-off instants (vector)
56    elseif j==2
57        reference = (M_i * sin(2 * pi * f * t + 2*pi/3 ) + 1) / 2; % Sinusoidal
    modulation waveform
58        pulse_signal = reference > carrier; % Gate pulse for switch
59        rising_edges = find(diff(pulse_signal) == 1); % dim % Discrete turn-on
    instances (vector)                                (for time domain mulitply by
    sample frequency)
60        t_r = rising_edges/fsample;
61        falling_edges = find(diff(pulse_signal) == -1); % dim % Discrete turn-off
    instances (vector)                               (for time domain mulitply by sample
    frequency)
62        t_f = falling_edges/fsample;
63        num_rising_edges = length(rising_edges); % dim % Number of rising edges/turn
    ons (vector)
64        num_falling_edges = length(falling_edges); % dim % Number of falling edges/turn
     offs (vector)
65        is_rising_edges(1:num_rising_edges) = isB(rising_edges); % A % Instantaneous
    currents at turn-on instants (vector)
66        is_falling_edges(1:num_falling_edges) = isB(falling_edges); % A % Instantaneous
     currents at turn-off instants (vector)
67    elseif j==3
68        reference = (M_i * sin(2 * pi * f * t + 2*pi/3 ) + 1) / 2; % Sinusoidal
    modulation waveform
69        pulse_signal = reference < carrier; % Gate pulse for switch
70        rising_edges = find(diff(pulse_signal) == 1); % dim % Discrete turn-on
    instances (vector)                                (for time domain mulitply by
```

```
    sample frequency)
71      t_r = rising_edges/fsample;
72      falling_edges = find(diff(pulse_signal) == -1); % dim % Discrete turn-off
    instances (vector)                          (for time domain mulitply by sample
    frequency)
73      t_f = falling_edges/fsample;
74      num_rising_edges = length(rising_edges); % dim % Number of rising edges/turn
    ons (vector)
75      num_falling_edges = length(falling_edges); % dim % Number of falling edges/turn
     offs (vector)
76      is_rising_edges(1:num_rising_edges) = isB(rising_edges); % A % Instantaneous
    currents at turn-on instants (vector)
77      is_falling_edges(1:num_falling_edges) = isB(falling_edges); % A % Instantaneous
     currents at turn-off instants (vector)
78  elseif j==4
79      reference = (M_i * sin(2 * pi * f * t - 2*pi/3 ) + 1) / 2; % Sinusoidal
    modulation waveform
80      pulse_signal = reference > carrier; % Gate pulse for switch
81      rising_edges = find(diff(pulse_signal) == 1); % dim % Discrete turn-on
    instances (vector)                            (for time domain mulitply by
    sample frequency)
82      t_r = rising_edges/fsample;
83      falling_edges = find(diff(pulse_signal) == -1); % dim % Discrete turn-off
    instances (vector)                          (for time domain mulitply by sample
    frequency)
84      t_f = falling_edges/fsample;
85      num_rising_edges = length(rising_edges); % dim % Number of rising edges/turn
    ons (vector)
86      num_falling_edges = length(falling_edges); % dim % Number of falling edges/turn
     offs (vector)
87      is_rising_edges(1:num_rising_edges) = isC(rising_edges); % A % Instantaneous
    currents at turn-on instants (vector)
88      is_falling_edges(1:num_falling_edges) = isC(falling_edges); % A % Instantaneous
     currents at turn-off instants (vector)
89  elseif j==5
90      reference = (M_i * sin(2 * pi * f * t - 2*pi/3 ) + 1) / 2; % Sinusoidal
    modulation waveform
91      pulse_signal = reference < carrier; % Gate pulse for switch
92      rising_edges = find(diff(pulse_signal) == 1); % dim % Discrete turn-on
    instances (vector)                            (for time domain mulitply by
    sample frequency)
93      t_r = rising_edges/fsample;
94      falling_edges = find(diff(pulse_signal) == -1); % dim % Discrete turn-off
    instances (vector)                          (for time domain mulitply by sample
    frequency)
95      t_f = falling_edges/fsample;
96      num_rising_edges = length(rising_edges); % dim % Number of rising edges/turn
    ons (vector)
97      num_falling_edges = length(falling_edges); % dim % Number of falling edges/turn
     offs (vector)
98      is_rising_edges(1:num_rising_edges) = isC(rising_edges); % A % Instantaneous
    currents at turn-on instants (vector)
99      is_falling_edges(1:num_falling_edges) = isC(falling_edges); % A % Instantaneous
     currents at turn-off instants (vector)
```

```
    end

    %%% Switching loss in switch %%%
    E_swhf = double(E_sw(is_rising_edges)); % J % Instantaneous turn-on/off energies (
    vector)
    E_swhf_sum = sum(E_swhf); % J % Total instantaneous turn-on/off energy in specified
     period
    P_turnsw_add = E_swhf_sum/T_2; % W % Total turn-on/off power loss from switching
    P_turnsw = P_turnsw + P_turnsw_add;
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

    %%% Conduction loss in switch %%%
    if t_f(1)<t_r(1) % Initiate Qsw_tot for loop. This takes care of the first pulse if
     the switch is initially on
    % Charge
        %Mean
        Qsw_mean_add = is_falling_edges(1) * t_f(1); % coulomb
        % Qsw_mean = Qsw_mean + Qsw_mean_add;
        Qsw_mean = Qsw_mean_add;
        %RMS
        Qsw_RMS_add = Is_M^2 * ( 2*(t_f(1) -0 )*omega + sin(2*0 *omega) - sin(2*t_f(1)
    *omega) ) / (4*omega);
        % Qsw_RMS = Qsw_RMS + Qsw_RMS_add;
        Qsw_RMS = Qsw_RMS_add;
    else % This takes care of the first pulse if the switch is initially off
        Qsw_mean = 0; % coulomb % mean
        Qsw_RMS = 0; % coulomb^2/s %RMS
    end

    if t_f(1)<t_r(1)
        for i = 1:num_rising_edges-1
        % Charge
            % Mean
            Qsw_mean_add = is_rising_edges(i) * ( (t_f(i+1)-t_r(i))  ); % coulomb
            Qsw_mean = Qsw_mean + Qsw_mean_add; % coulomb
            % Mean
            Qsw_RMS_add = Is_M^2 * ( 2*omega*( (t_f(i+1) - t_r(i))  ) + sin(2*omega*t_r
    (i) ) - sin(2*omega*t_f(i+1) )) / (4*omega);
            Qsw_RMS = Qsw_RMS + Qsw_RMS_add; % coulomb
            %x = x + 1;
        end
    else
        for i = 1:num_rising_edges
        % Charge
            % Mean
            Qsw_mean_add = is_rising_edges(i) * ( (t_f(i)-t_r(i))  ); % coulomb
            Qsw_mean = Qsw_mean+Qsw_mean_add; % coulomb
            % RMS
            Qsw_RMS_add = Is_M^2 * ( 2*omega*( (t_f(i) - t_r(i)) ) + sin(2*omega*t_r(i)
     ) - sin(2*omega*t_f(i) )) / (4*omega);
            Qsw_RMS = Qsw_RMS+Qsw_RMS_add; % coulomb
        end
    end

```

```
148     if t_f(num_falling_edges)<t_r(num_rising_edges) % This takes care of the final
        pulse if the switch ends being turned on
149     % Charge
150         % Mean
151         Qsw_mean_add = is_rising_edges(num_rising_edges) * (T_2-(t_r(num_rising_edges)
        )); % coulomb
152         %Qsw_mean = Qsw_mean+Qsw_mean_add; % coulomb
153         % RMS
154         Qsw_RMS_add = (Is_rms*sqrt(2))^2 * ( 2*omega*(T_2-t_r(num_rising_edges) ) + sin
        (2*t_r(num_rising_edges) *omega) - sin(2*T_2*omega)) / 4*omega;
155         %Qsw_RMS = Qsw_RMS+Qsw_RMS_add; % coulomb
156     else % This takes care of the final pulse if the switch ends being turned off
157     % Charge
158         Qsw_mean_add = 0; % C
159         Qsw_RMS_add = 0; % C
160     end
161
162     Isw_mean = (Qsw_mean+Qsw_mean_add)/T_2; % A % Mean current of switch 1
163     Isw_RMS = sqrt((Qsw_RMS+Qsw_RMS_add)/T_2); % A % RMS current of switch 1
164
165     P_condmean_add = Isw_mean^2*Rdson_mean; % W %
166     P_condmean = P_condmean + P_condmean_add; % W %
167     P_condRMS_add = Isw_RMS^2*Rdson_mean; % W %
168     P_condRMS = P_condRMS + P_condRMS_add; % W %
169
170     P_sw_losses_indv(j+1,1) = P_turnsw_add;
171     P_sw_losses_indv(j+1,2) = P_condRMS_add;
172     P_sw_losses_indv(j+1,3) = Isw_mean;
173     P_sw_losses_indv(j+1,4) = Isw_RMS;
174
175 end
176
177 P_loss_sw = P_turnsw+P_condRMS; % W % Total power loss
178 P_in = Vs_rms*Is_rms;% W % Input power
179 P_out = P_in-P_loss_sw; % W % Total output power
180 eta = P_out/P_in; % dim % Efficiency
181
182 P_data = [P_turnsw P_condRMS P_loss_sw eta];
183 end
```

M Component Databases

To use the database with the multi-objective optimization algorithm located in Appendix L an excel sheet with the name 'Database.xlsx' is to be generated. Each following table is to be put into a respective sheet with the name corresponding to the name in quotation marks in the tables caption. The table, which for the one divided into two parts, has to go into a singular sheet and not two separate ones.

Table M.1 MOSFET database part 1 'MOSFETs 1200 TO247-4'

Name	E0	E1	E2	R0	R1	R2	Rth,JC [°C/W]
IMZ120R090M1H	4.38E+01	1.13E+01	2.03E-01	1.77E-01	4.22E-04	6.33E-05	1.00
IMZ120R060M1H	5.99E+01	1.19E+00	1.16E-01	1.46E-01	-1.10E-03	2.46E-05	0.80
SCT070W120G3-4AG	1.49E+02	7.29E+00	1.92E-01	1.24E-01	-3.48E-04	1.87E-05	0.74
SCT070W120G3-4	1.49E+02	7.29E+00	1.92E-01	1.24E-01	-3.48E-04	1.87E-05	0.74
SCTWA40N12G24AG	1.27E+02	-1.92E+00	5.82E-01	1.55E-01	-1.41E-04	5.46E-05	0.60
SCTWA40N120G2V-4	1.26E+02	-1.74E+00	5.75E-01	1.60E-01	-5.80E-04	6.12E-05	0.63
SCT040W120G3-4	1.76E+02	1.14E+01	1.51E-01	7.81E-02	-4.21E-04	1.34E-05	0.56
SCTWA60N12G2-4AG	2.82E+02	8.62E+00	5.16E-02	9.94E-02	-6.66E-06	1.13E-05	0.45

Table M.2 MOSFET database part 2 - transposed 'MOSFETs 1200 TO247-4'

Ag	2.45E-01	3.14E-01	8.20E-02	1.27E-01	1.44E-01	1.44E-01	1.76E-01	2.17E-01
Al	2.11E+00	3.35E+00	2.74E+01	2.98E+00	1.21E+00	1.21E+00	1.64E+00	3.63E+00
Au	0.00E+00	0.00E+00	6.00E-03	0.00E+00	8.60E-02	8.00E-03	0.00E+00	1.20E-02
Cu	4.11E+03	4.11E+03	4.74E+03	4.75E+03	4.75E+03	4.75E+03	4.75E+03	4.75E+03
Fe	4.12E+00	4.12E+00	4.75E+00	4.78E+00	4.78E+00	4.78E+00	2.19E+00	4.78E+00
Mg	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Ni	1.95E+00	1.95E+00	1.48E+00	2.39E+01	8.30E-02	2.39E+01	1.77E+01	2.39E+01
P	1.23E+00	1.23E+00	9.50E-01	1.44E+00	1.44E+00	1.44E+00	2.61E+00	1.44E+00
Pb	0.00E+00	0.00E+00	1.04E+00	2.40E+00	2.98E+00	2.98E+00	3.32E+00	4.47E+00
Sb	9.80E-02	1.26E-01	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Sn	2.37E+01	2.39E+01	4.32E+01	5.00E-02	4.26E+01	4.26E+01	6.27E+00	4.27E+01
Ti	0.00E+00	0.00E+00	7.00E-03	7.00E-03	1.30E-02	1.30E-02	1.10E-02	1.90E-02
V	0.00E+00	0.00E+00	2.00E-03	2.00E-03	0.00E+00	0.00E+00	3.00E-03	0.00E+00
Manufaturer	Infineon	Infineon	ST Micro	ST Micro	ST Micro	ST Micro	ST Micro	ST Micro

Table M.3 Toroidal core database 'Inductor_ToroidalCores'

Name	Al [H/turn]	μ_r	le [m]	Ve [m^3]	m[g]	B_{sat} [T]	C_{core} [m]	Material	OD[mm]	HT[mm]	ID[mm]	$Diss$	Manufaturer
KNF068-090A	0.000000064	90	0.0414	0.00000096	7.3	1.6	0.02323	Neu Flux	18.03	7.11	9.02	0	KDM
KNF106-090A	0.000000113	90	0.0635	0.00000415	30.3	1.6	0.03758	Neu Flux	27.7	11.99	14.1	0	KDM
KNF106-090A-E18	0.000000182	90	0.0635	0.00000667	48.6	1.6	0.0516	Neu Flux	27.7	19	14.1	0	KDM
KNF290-060A	0.000000206	60	0.1838	0.00009264	669.2	1.6	0.10367	Neu Flux	75.2	36.27	44.07	0	PAIRUI
KNF290-075A	0.000000257	75	0.1838	0.00009264	678.5	1.6	0.10367	Neu Flux	75.2	36.27	44.07	0	PAIRUI
KNF290-090A	0.000000309	90	0.1838	0.00009264	689.7	1.6	0.10367	Neu Flux	75.2	36.27	44.07	0	PAIRUI
NPF168060	0.000000159	60	0.1022	0.000023234	178.3	1.5	0.071	FE SI	44	25.1	23.2	0	POCO
NPF184060	0.000000135	60	0.1074	0.000021373	165.9	1.5	0.06215	FE SI	47.63	18.92	23.32	0	POCO
NPF185060	0.000000086	60	0.1163	0.000015584	122.9	1.5	0.05217	FE SI	47.6	16.13	27.69	0	POCO
NPF200060	0.000000073	60	0.1273	0.000015929	125.1	1.5	0.04945	FE SI	51.69	14.35	30.94	0	POCO
NPF225060	0.000000075	60	0.143	0.00002065	155.5	1.5	0.05212	FE SI	57.15	14.86	34.75	0	POCO
NPF306060	0.000000085	60	0.1961	0.000043523	342.7	1.5	0.06528	FE SI	78.94	17.15	47.96	0	POCO
B64290L0084X087	0.00000288	2200	0.2553	0.00006822	330	0.49	0.0741	N87	104.8	16.5	63.7	0	TDK

Table M.4 E-core database - transposed 'Inductor_ECores'

Name	00X6527E040	00K114LE026	00K114LE060
Al **[H/turn]**	0.00000023	0.000000235	0.000000455
$\mu_{\mathbf{r}}$	40	26	60
le **[m]**	0.147	0.215	0.215
Ve **[m^3]**	0.0000794	0.000262	0.000262
m **[g]**	260	714	742
$B_{\mathbf{sat}}$ **[T]**	1.6	1.6	1.6
Ae **[m^2]**	0.00054	0.00127	0.00127
Material	Xflux	KoolMU	KoolMU
$W_{\mathbf{window}}$ **[m]**	0.01209	0.0222	0.0222
$H_{\mathbf{window}}$ **[m]**	0.0222	0.0286	0.0286
$W_{\mathbf{centerpost}}$ **[m]**	0.01966	0.0351	0.0351
$W_{\mathbf{core}}$ **[m]**	0.027	0.03494	0.03494
$L_{\mathbf{core}}$ **[m]**	0.06515	0.1143	0.1143
$H_{\mathbf{core}}$ **[m]**	0.03151	0.04618	0.04618
Diss	1	1	1
Manufaturer	MagneticsINC	MagneticsINC	MagneticsINC

Table M.5 Film capacitor database 'CapacitorsFilm'

C **[mF]**	$V_{\mathbf{DC}}$ **[V]**	$V_{\mathbf{AC}}$ **[V]**	**Number**	L **[mm]**	W **[mm]**	H **[mm]**	V **[cm^3]**	RC **[A]**	**Name**
0.0016	1200	600	1	42	20	40	33.6	6.5	C4AFBBW4160F3FK
0.0022	1200	600	2	42	28	37	43.512	11.9	C4AFBBW4220T3JK
0.0033	1200	600	3	42	30	45	56.7	15.3	C4AFBBW4330T3LK
0.0047	1200	600	4	42	35	50	73.5	19.5	C4AFBBW4470T3OK
0.005	1200	600	5	57.5	30	45	77.625	12.5	C4AFBBW4500F3MK
0.007	1200	600	6	57.5	35	50	100.625	20.4	C4AFBBW4700T3NK
0.01	1200	600	7	57.5	45	56	144.9	25.5	C4AFBEW5100T3AK
0.011	1200	600	8	57.5	45	65	168.1875	21.6	C4AFBEW5110F3BK
0.012	1200	600	9	57.5	45	65	168.1875	28.3	C4AFBEW5120T3BK
0.015	1000	500	10	57.5	45	56	144.9	21.6	C4AFAEW5150F3AK
0.018	1000	500	11	57.5	45	65	168.1875	24.1	C4AFAEW5180F3BK
0.02	800	400	12	57.5	45	56	144.9	33.3	C4AF3EW5200T3AK
0.0225	800	400	13	57.5	45	65	168.1875	37.4	C4AF3EW5225T3BK
0.028	800	400	14	57.5	45	65	168.1875	26.1	C4AF3EW5280F3BK

Table M.6 Electrolytic capacitor database 'CapacitorsElectrolytic'

C **[mF]**	VDC **[V]**	**Number**	H**[mm]**	D**[mm]**	V**[cm^3]**	RC**[A]**	**Name**
0.022	500	1	25	13	1.05625	0.115	ESH226M500AL4AA
0.15	500	2	45	22	5.445	1.02	ESG157M500AQ5AA
0.18	450	3	45	18	3.645	1.09	450QXW180MEFC18X45
0.22	450	4	50	18	4.05	1.22	450CXW220MEFC18X50
0.47	400	5	50	40	20	7	MAL205356471E3
0.82	450	6	55	35	16.8	3.3	B43652A5827M050
1	450	7	60	30	13.5	3.11	B43659A5108M057
1	400	8	100	40	40	4.05	MAL205356102E3
1.61	475	9	90	35	27.6	4.85	B43657C0168M157
1.71	475	10	95	35	29.1	5.11	B43657C0178M157
1.81	475	12	100	35	30.6	5.36	B43657C0188M157
1.83	450	13	90	35	27.6	5.07	B43657C5188M357
1.94	450	14	95	35	29.1	5.34	B43657C5198M457
2.06	450	15	100	35	30.6	5.62	B43657C5208M657

Table M.7 Recyclability rate database 'MaterialRecycCoefficients'

Ag	**Al**	**Au**	**Cu**	**Fe**	**Mg**	**Ni**	**Pb**	**Sb**	**Sn**	**Ti**	**V**
0.8	0.75	0.95	0.6	0.62	0.5	0.6	0.65	0.44	0.5	0.5	0.4

Table M.8 Heatsink database 'HeatsinkDatabase'

$R_{\mathbf{th}}$ **[K/W]**	W **[mm]**	H **[mm]**	L **[mm]**	V **[L]**	m**[kg]**	**Number**	**Name**
1.61	30	30	100	0.18	0.222057541	1	LAM 3 100 12
1.55	30	30	125	0.2	0.246730602	2	LAM 3 125 12
1.5	30	30	150	0.22	0.271403662	3	LAM 3 150 12
1.06	60.5	30	100	0.26	0.320749782	4	LAM 3 D 100 12
1.02	60.5	30	125	0.28	0.345422842	5	LAM 3 D 125 12
0.98	60.5	30	150	0.3	0.370095902	6	LAM 3 D 150 12
0.48	80.8	40	100	0.49	0.604489974	7	LAM 4 D 100 24
0.45	80.8	40	125	0.53	0.653836094	8	LAM 4 D 125 24
0.2	62	74	100	0.4588	0.566	9	LA 6 100 24
0.175	62	74	150	0.6882	0.849	10	LA 6 150 24
0.15	62	74	200	0.9176	1.132	11	LA 6 200 24
0.125	62	74	250	1.147	1.415	12	LA 6 250 24
0.1	62	74	300	1.3764	1.698	13	LA 6 300 24
0.09	120	120	100	1.44	1.2	14	LA 17 100 24
0.071	120	120	150	2.16	1.8	15	LA 17 150 24
0.06	120	120	200	2.88	2.4	16	LA 17 200 24
0.05625	120	120	250	3.6	3	17	LA 17 250 24
0.0525	120	120	300	4.32	3.6	18	LA 17 300 24