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Fault tolerant distributed control strategy for Modular Multilevel Converter in HVDC applications

Master Thesis

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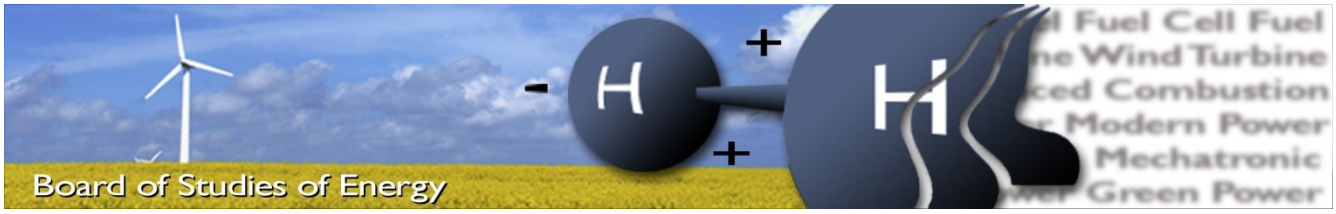

Title: **Fault tolerant distributed control strategy for Modular Multilevel Converter in HVDC applications**

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SYNOPSIS:

The Modular Multilevel Converter (MMC) is a new converter technology which proves to be a good candidate for High Voltage Direct Current (HVDC) transmission systems due to its low losses, modular design, lower filtering requirement and good fault tolerance.

Because of the large number of Sub-Modules (SMs), the classical centralized control strategy becomes is challenging and distributed control is recommended. This will require fast communication and good synchronization.

In this project a SM has been designed, build and experimentally validated to be able to handle fault-tolerant operation and start-up requirement. The communication was build based on real-time Industrial Ethernet protocol and is able to reconfigure on-the-fly during fault operation.

Fault-tolerant operation and start-up procedures have been validate using PSCAD model for realistic test cases.

Copies: [3]
Pages, total: [54]
Appendix: [58]
Supplements: [1 CD]

By signing this document, each member of the group confirms that all group members have participated in the project work, and thereby all members are collectively liable for the contents of the report. Furthermore, all group members confirm that the report does not include plagiarism.

Preface

This report was written as part of the study curriculum requirements for graduation of the Master in Wind Power Systems at Aalborg University. It was carried out by group WPS4-1055, formed by 1 student, between 1st of September 2012 and 13 June 2013.

Acknowledgements

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Without their help I wouldn't be able to finish this project.

Reading Instructions

The references are shown as numbers in square brackets, with detailed information in the Reference Chapter. The format for the equations is (A.B), for table and figure A-B, where A will represent the chapter number and B the position in the chapter.

The chapters are numbered in order and the Appendixes are arranged with letters. Attached to the report, there is enclosed a CD which contains this report in Microsoft Word and Adobe PDF formats, references, simulation files, bill of materials and the Altium files used for the PCB, the source code files for the DSP, TwinCAT server and CPLD.

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Aalborg

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Nomenclature

List of abbreviations

AC Alternating Current

ADC Analog to Digital Converter

APOD Alternative Phase Opposite Disposition

ASIC Application Specific Integrated Circuit

BOOT Bootstrap EtherCAT mode

CAN Controller Area Network

CLK Clock

CPLD Complex Programmable Logic Devices

CS Chip Select

CSC Current Source Converter

DC Direct Current

DC unit Distributed Clock unit

DSP Digital Signal Processor

EEPROM Electrically Erasable Programmable Read-Only Memory

ESC EtherCAT Slave Controller

ESM EtherCAT State Machine

ETG EtherCAT Group

EWEA European Wind Energy Association

FC Flying Capacitor

FPGA Field Programmable Gate Array

GPIO General Purpose Input Output

HS High Side

HVAC High Voltage Alternating Current

HVDC High Voltage Direct Current

IC Integrated Circuit

IGBT Insulated Gate Bipolar Transistor

INIT Initialization state

IP Internet Protocol

IPC Industrial Personal Computer

JTAG Joint Test Action Group

LCC Line Commuted Converter

LED Light Emitting Diode

LS Low Side

MAC Media Access Control

MISO Master Input Slave Output

MMC Modular Multilevel Converter

MOSI Master Output Slave Input

NPC Neutral Point Clamped

OP Operational Mode

PCB Printed Circuit Board

PD Phase Disposition

PDI Process Data Interface

PHY Physical Layer

PLC Programmable Logical Computer

PLL Phase Loop Lock

POD Phase Opposite Disposition

PREOP Pre-Operational Mode

PS Phase Shifted

PWM Pulse Width Modulation

R Read command

RMW Read Multiple Writes commands

RW Read-Write command

SAFEOP Safe-Operational Mode

SM Sub-Module

SPI Serial Peripheral Interface Bus

SPWM Sine Pulse Width Modulation

SVM Space Vector Modulation

TC TwinCAT

VSC Voltage Source Converter

WKC Working Counter

XML Extensible Markup Language

1 Introduction

This chapter presents the motivation and objectives of this project. An overview of the HVDC market and the implementation of the MMC in these applications are shown.

1.1 Background

HVDC has become a more attractive alternative for high power transmissions over long distances by providing lower losses. Compared to similar AC transmission systems, it can deliver more power over long distances, which in term translates in fewer transmission lines and space (Figure 1-1). HVDC also proves to be more flexible in terms of reactive power support and control and can interconnect asynchronous AC networks [1].

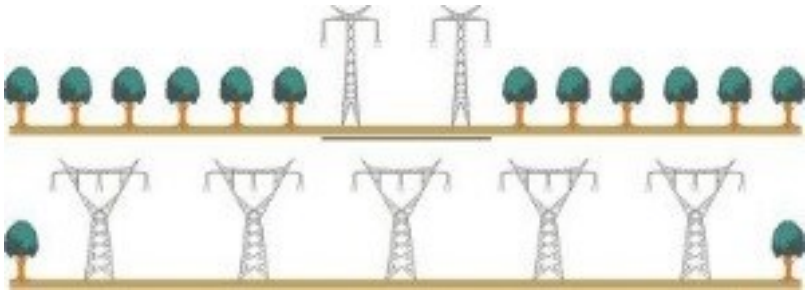

Figure 1-1 - Overhead transmission lines for HVDC compared to AC lines for the same power [2]

HVDC connection can be employed with underground cables, making the installation invisible after the cables are buried. As it only needs two cables, these can be laid next to each other in order to minimize the magnetic field since the currents in the cables pass in opposite directions, cancelling each others effect. In theory, DC cables have no length limit compared to the AC ones, which are limited by the cable capacitance and need intermediate reactive power compensation stations which increase the losses.

One of the main driving force of the HVDC industry in Europe are the offshore wind farms installations, as the European Union has taken the engagement to increase renewable energy capacity in the following year and to minimize the CO_2 emissions[2]. In recent years, thanks to advancements in the research field, the offshore wind installations are dramatically increasing. The European Wind Energy Association (EWEA) forecasts that by 2020 the cumulated offshore capacity will grow up to 50GW (Figure 1-2) from a current value of 5GW [3]. In other parts of the world, the need for power from fast growing economies (China, Brasil, India) and due to the long distances between generation and consumers, HVDC becomes a necessity.

As the wind industry has already matured, most of the good onshore locations for wind farms have already been developed and determined the developers to move to offshore sites. The main reason for this is the available wind resources with higher average wind speeds and yields and the lack of obstacles, making it more reliable. The challenge which comes with this approach is feeding the power generated to the main land AC grid efficient, reliably and cost effective. This can be done with both HVAC and HVDC systems, but as the distance passes 50-100km, the HVDC solution becomes more financially viable [1].

	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
EWEA	3.9	5.3	8.1	10.9	14.0	17.4	21.6	26.7	33.1	40.0
NREAPs	3.7	5.8	9.1	12.4	15.6	20.4	25.8	31.1	36.8	43.3

Figure 1-2 – PROJECTED CUMULATIVE OFFSHORE WIND CAPACITY (EWEA AND NATIONAL RENEWABLE ENERGY ACTION PLANS) [3]

One important aspect in offshore wind farms are the onshore connections. As the costal grids are not often too strong and the offshore farms tend to be large in scale, special attention needs to be given at the point of connection. The strict grid codes have to be met in order to ensure the stability of the grid, but as with any large power generation unit, grid support functions need to be present. A HVDC transmission system could ensure the security and power quality of the connection point by stabilizing irregular power flows which could be generated by the wind turbines, frequency support, voltage and reactive power control, as well as support the possibility of wind park grids energization in low wind speeds. In case of AC grid faults, the wind farms are decoupled from the fault by the DC-link and protected while, at the same time, the HVDC systems can help restore normal operation of the grid [1].

While the first HVDC stations where implemented with two-level thyristor based Current Source Converters (CSCs), the newer tendency is to use Voltage Source Converter (VSC) technology. The MMC or modified versions of it has been the main choice in the industry due to its modularity and high efficiency [1].

1.2 State of the art and motivation

The MMC was introduced by Marquardt and Lesnicar in 2002 [4]. The main idea of the MMC is a series connected Sub-Modules (SMs) with two semiconductors in a half-bridge configuration and a DC capacitor across them. By controlling the states of the SMs' switches, the DC voltage levelsare inserted or by-passed to achieve a high voltage output [5].

Compared to other HVDC technologies, MMC has the simple design and modularity advantages which make the construction and installation of the HVDC connection faster and easier. The modularity also allows for off-the-shelf semiconductor devices with proven reliability and lower bandgap to be used, increasing the reliability of the converter. As it can be scaled in order to suit the power needs, the design time is drastically decreased. In recent years, the trend has been to switch from thyristor based line commutated converter to VSC MMC, due to its high controllability and lower losses [1].

Currently the main developers (ABB, Siemens, Alstom) of HVDC transmission systems offer MMC based solutions, although some small differences in the topology exist in order to improve the controller or to reduce the losses [6].

At the moment, there are different HVDC systems for offshore wind farm in different states of development in the North Sea region.

A state of the art system was developed and given into operation by ABB in the north of Germany in 2009. It was the first HVDC system in Germany and it connects one of the largest and most remote wind parks in the world (BARD Offshore 1) to a station in Diele, mainland Germany (Figure 1-3). It is a +/-150kV 400MW system comprised of an offshore station with an AC collector, 125 km undersea cable, 75 km underground and an onshore station. It connects 80 5MW wind turbines to an onshore 380kV grid[1] .

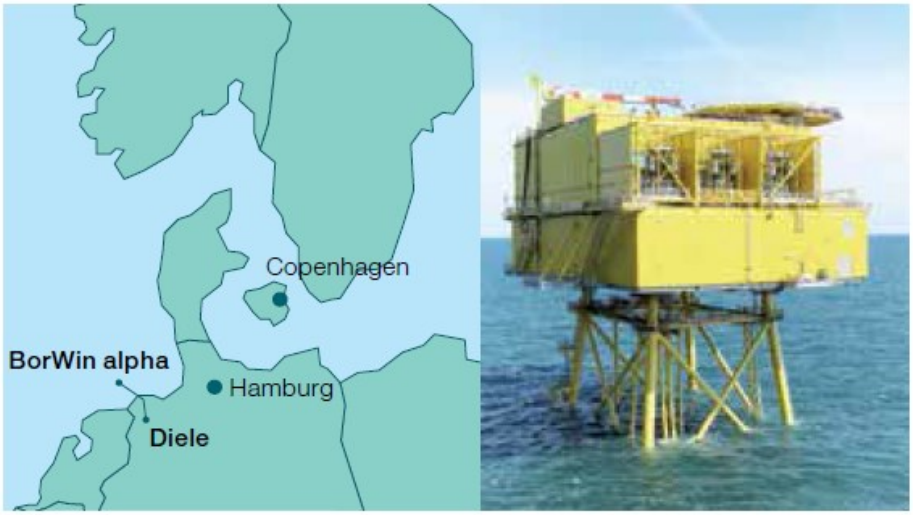

Figure 1-3 BorWin1 HVDC line (left) and offshore platform (right) [1]

A similar application is developed by Siemens for the SylWin1 project (Figure 1-4). This is currently the biggest VSC for offshore applications with 864MW rating, connecting the Dan Tysk wind farm to the german shore. The offshore converter will be installed on a floating platform along with the AC collector and VAr compensator. The +/-320kV DC-link will be connected in Büttel to the 380kV AC grid. The system is expected to be operational in 2014 [7].

Figure 1-4 SylWin1 placement in the north of Germany and the Bremen connection point [7]

One of the main challenges of the MMC is the control strategy (modulation and capacitor balancing). From this point two types of control can be considered:

- The centralized control, where a central controller, based on a sorting algorithm, decides which SM should be inserted at each instance and directly sends the switching signals to the driving circuits of each SM. The central control takes care of the capacitors voltage balancing in the arms. The main disadvantages for this type of control is the complex implementation due to the number and length of the fiber optics needed for control;
- The distributed control, where the control strategy is distributed between a master controller, which takes care of the high level control like circulating current suppression, and a slave controller on each SM which takes care of the modulation and capacitor balancing. The balancing in this case is split between the master and the SM slaves. This type of control allows for a daisy chain connection since the update speeds of the communication can be lowered compared to the centralized one.

1.3 Problem formulation

HVDC converters need to respect grid code requirements like fault ride through, frequency support, voltage support and also to be able to control power flow between the points it connects which translates in fast reactions times.

The distributed control in a MMC proves to be a challenge in terms of communication in order to provide the fast reaction times needed for the balancing of capacitors voltages and grid connection.

The communication in a MMC with a distributed control proves to be a challenge in terms of bandwidth, noise tolerance and update times.

1.4 Objectives

The purpose of this project is to design a control strategy with focus on communication and fault-tolerant operation. A low scale laboratory prototype will be built in order to test the fault redundant control and communication for the distributed control strategy. Also a start-up procedure for the MMC to limit in-rush currents by control will be analysed.

The main objectives of this project are:

- Modeling and analysis of MMC;
- Start-up procedure for distributed control analysis;
- Fault analysis, balancing and reconfiguration implementation;
- High bandwidth fault tolerant communication implementation;
- Low scale prototype design and realization.

1.5 Limitations

Since the main focus of this project is the implementation of a fault tolerant communications and a novel start-up procedure, some limitations have been established. The main limitations of this project are:

- Due to the available equipment and security the laboratory prototype will be a single phased five level MMC (4 SM per arm) with a 400V converter DC link;

- No high-level control strategy will be deeply studied or implemented with the exception of the balancing controller;
- No grid connection will be implemented, and the converter will be designed to follow a simple voltage reference;
- No focus will be placed on the converter output quality (in terms of harmonics) or efficiency.

1.6 Project Outline

At the beginning of the report the motivation and the objectives of this project are presented. After that, in Chapter 2, the theory and calculations for a MMC are discussed and the model for the simulations is presented. Also the modulation and balancing strategies are presented together with the start-up procedure.

Later, in Chapter 3, the communication solution is presented and detailed together with the redundancy and reconfiguration options.

Chapter 4 describes the simulation model in PSCAD and test cases for startup and fault redundancy and reconfiguration

In Appendix A a published paper is attached (ICREPQ13).

Appendix B will present the prototype design. An eight SM, five level small scale MMC was built featuring fast communication, hardware protection design with on the fly reconfiguration. The overview of the development platform is done, after which the sizing and design of the SM PCB is described with the protection mechanism. This chapter will end with an overview of the implemented control on the Digital Signal Processor (DSP) and the Complex Programmable Logic Device (CPLD) together with the hardware validation tests.

In Appendix C the Fortran and C -code for the PSCAD controller is listed.

In Appendix D the Bill of Materials for the SM is presented.

In Appendix E the SM schematic is listed.

In the end, the conclusions regarding the results are presented and analysed and further plans are detailed.

2 Introduction to the modular multilevel converter

This chapter starts with an overview of HVDC converters and afterwards presents the MMC design and dimensioning of components together with different modulation strategies, start-up procedures, fault protection and redundant reconfiguration. Bandwidth and update times requirements for the communication will be analysed.

2.1 Overview

Mainly, there are two technologies available for HVDC:

- Thyristor based line-commutated converters (LCC), which is a well proven technology and was first used in 1954 in Gotland, Sweden [8]. The main disadvantage of this technology is the lack of controllability and grid support capability.

- VSC HVDC, which is a new technology, initially designed for motor drive applications [9-11]. With the advancements made in development of semiconductors, which now can be easily controlled in terms of turn on/off with gate signals, the VSCs have become the standard in HVDC applications. They offer many advantages over the LCC such as: connection of weak (in terms of short circuit power) AC networks, black start possibility, fast control of active and reactive power flow and smaller footprint. Furthermore, in case of reverse power, the VSC does not require to invert the DC link polarity, nor does it require the large AC filters on the output [1, 9, 10, 12].

Since the development of VSC-HVDC, due to advancement in semiconductors, which gave rise to fully controllable devices, the main converter topologies used were two-level or three-level converters. The self-commutated devices, via gate pulses, can be used in VSC with Pulse Width Modulation (PWM) operating at frequencies much higher than the line frequency [13]. It is highly desirable that the PWM frequency to be much higher than the line frequency. However, the maximum frequency at which these devices can operate is determined by the switching losses and heat dissipation of the devices, which are directly related to the power transferred. Other disadvantages which may be caused by the high operating frequencies are: the electromagnetic interferences which can appear and the stresses the transformer insulations have to withstand from the high frequency oscillations which will be present [13].

A basic HVDC system is comprised of two back to back VSCs. The simplest topology which can be used is the two-level three-phase converter, as shown in Figure 2-1. In order to support a high blocking voltage capability and allow for an increased voltage on the DC bus, each switch shown in Figure 2-1 is comprised of series-connected semiconductors (typically IGBTs) with lower ratings. The antiparallel diodes are needed in order to support a four-quadrant operation of the converter. The DC-link capacitors are required in order to ensure the stability of the DC link so that the power flow can be controlled and filter the harmonics which may appear.

By supplying more voltage steps in the output waveform, the harmonics content can be decreased, and as a result, the AC filters dimensions can also be reduced. Figure 2-2 presents the one phase leg of two multilevel converters. Figure 2-2a) shows the diode-clamped neutral-point-clamped converter (NPC) while Figure 2-2b) presents a five-level flying capacitor (FC) converter. By introducing more switches, the switching frequency of each semiconductor can be reduced while keeping the same equivalent switching frequency per leg. This translates to lower switching losses and smaller size for the heatsink while improving the output waveform quality. Also, the voltage blocking requirement for each switch gets reduced [13].

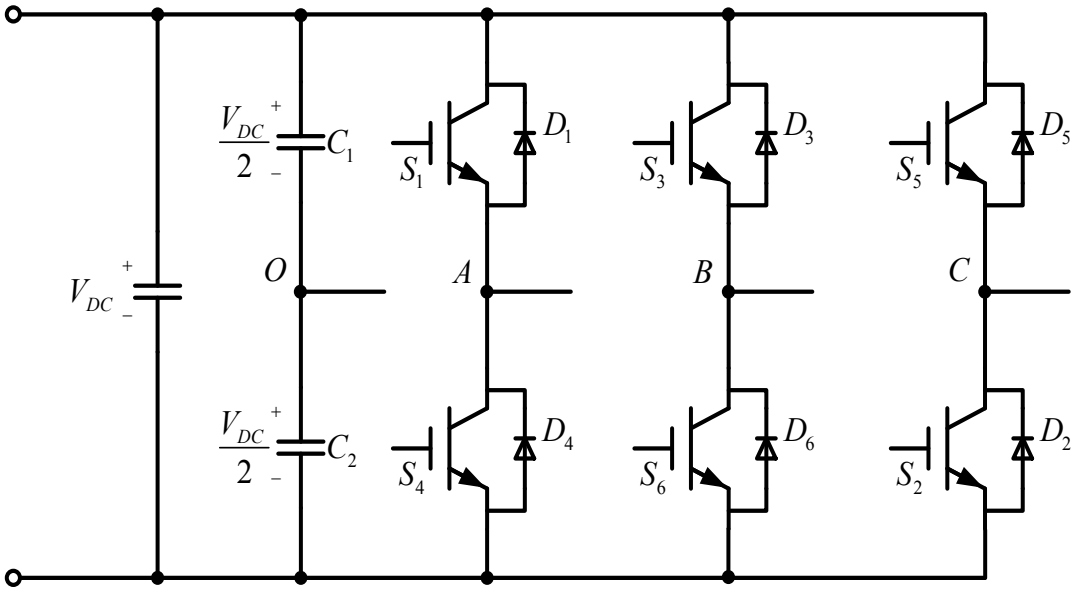

Figure 2-1 Three-phase two-level VSC topology

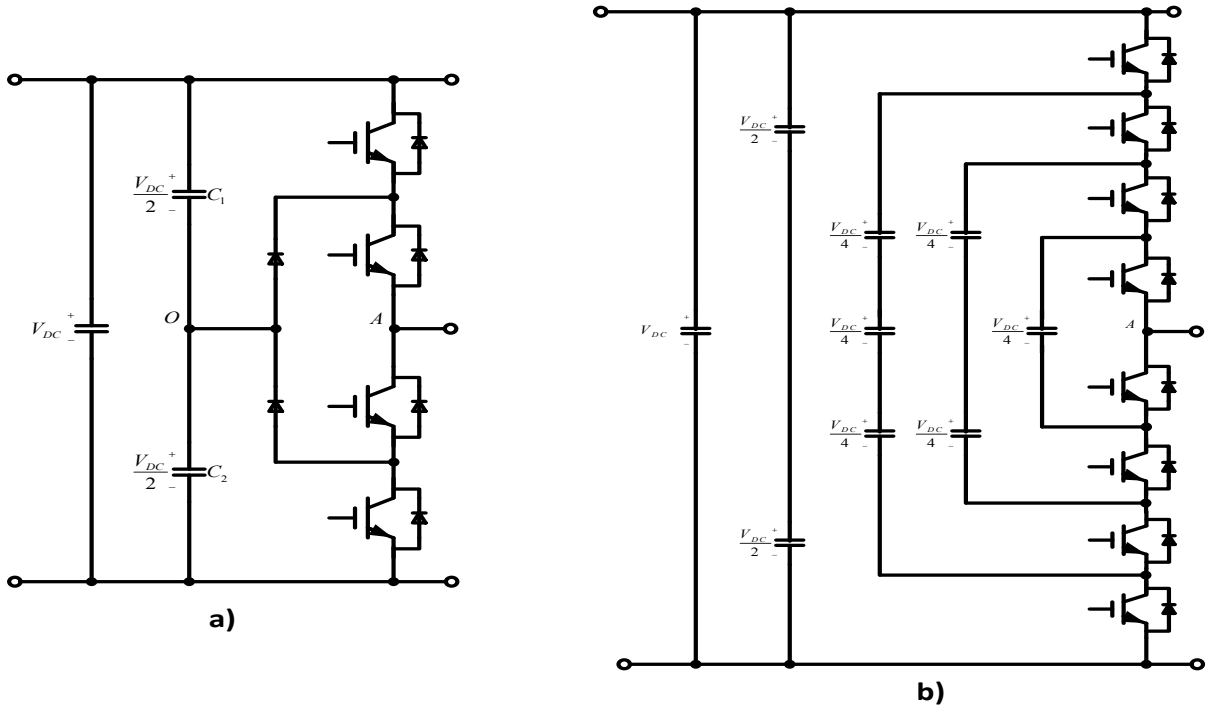

Figure 2-2 a) NPC phase leg; b) Five-level FC phase leg

2.2 Basic Description

Since its introduction in 2002 by Marquart [4], the MMC has proven to be an ideal candidate for HVDC VSC applications [1, 10, 14]. The design characteristic of the MMC is represented by a series connected SMs which consists of semiconductor switches and a capacitor. The main advantage of the MMC over other multilevel topologies includes simpler design which is inherited from the modular construction, making manufacturing and installation faster and easier. Another main benefit from the modular construction is the fault tolerance, since in the case of a switch/capacitor failure the faulty SM can be isolated until it is changed at a scheduled maintenance, allowing for safe operation and at the same time providing a high availability.

The operation of the converted can be isolated at SM level (Figure 2-3). Each switch of the half bridge operates complementary. The SM is considered ON when S1 is conducting and the capacitor is inserted. At this point, the SM participated in the shaping of the output waveforms and the voltage at the terminals will be equal to the capacitor voltage. Depending on the current direction, the capacitor may get charged or discharged. Figure 2-4 shows the current flow and the 4 switches states in the SM, while Table 2-1 summarizes all the possible states of the switches.

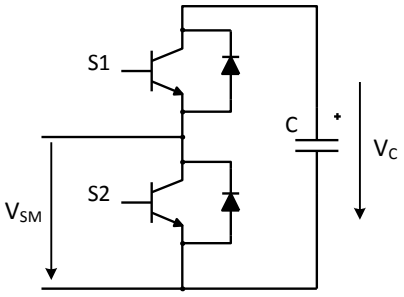

Figure 2-3 - Schematic of a SM [34]

Table 2-1: Switch States of MMC SM [64]

Case	Switch State		SM Terminal Voltage	Current direction	Capacitor Status
	S1	S2			
a	1	0	V_C	(+)	**Charging**
b	0	1	0	(+)	**By-passed**
c	1	0	V_C	(-)	**Discharging**
d	0	1	0	(-)	**By-passed**
-	1	1	**Capacitor Shorted**		
-	0	0	**Open Circuit**		

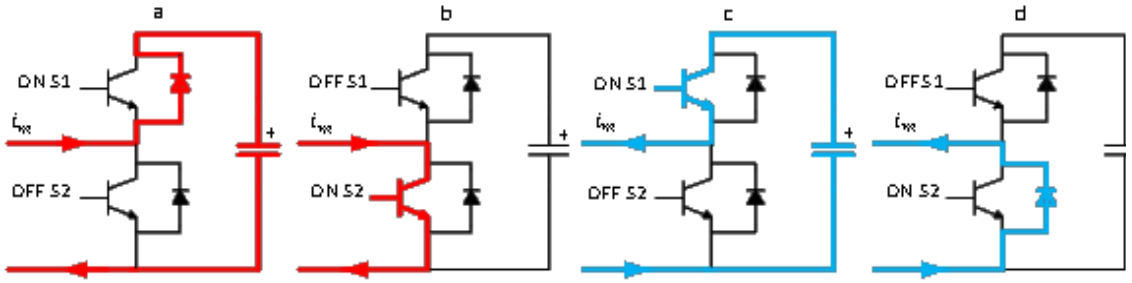

Figure 2-4 - Positive and negative current flow[64]

By controlling the state of each SM, a multilevel output waveform can be obtained. An increased number of voltage levels can be translated in lower harmonics. And, due to smaller amplitude of the voltage steps, the stresses on the devices (dV/dt) can be reduced [5]. Since the voltage steps of the output is directly related to the number of SMs in each arm, AC filters can theoretically be eliminated with a sufficiently large number of SMs [15].

Since each SM has included a capacitor, there is no requirement for a DC-link capacitor as the series connected capacitors can easily replace it. Researches have shown the possibility of operating the MMC with a switching frequency close to the fundamental one, which results into lower losses [7, 16, 17].

Each phase leg of the converter consists of series-connected SMs with a common DC-link (Figure 2-5). The leg is composed of two arms with equal number of SMs and an inductor at the point of connection to the AC terminal. Since the three-phases will be connected to the same DC-link and in real life there will be an unbalance between each phase, balancing currents will rise in each leg which will be suppressed by the inductors. Another major role of the inductors is to suppress high fault currents.

If it is assumed that all the capacitors in the leg are balanced, the voltage across each capacitor can be summarized as:

$$V_C = \frac{V_{dc}}{n} \tag{2.1}$$

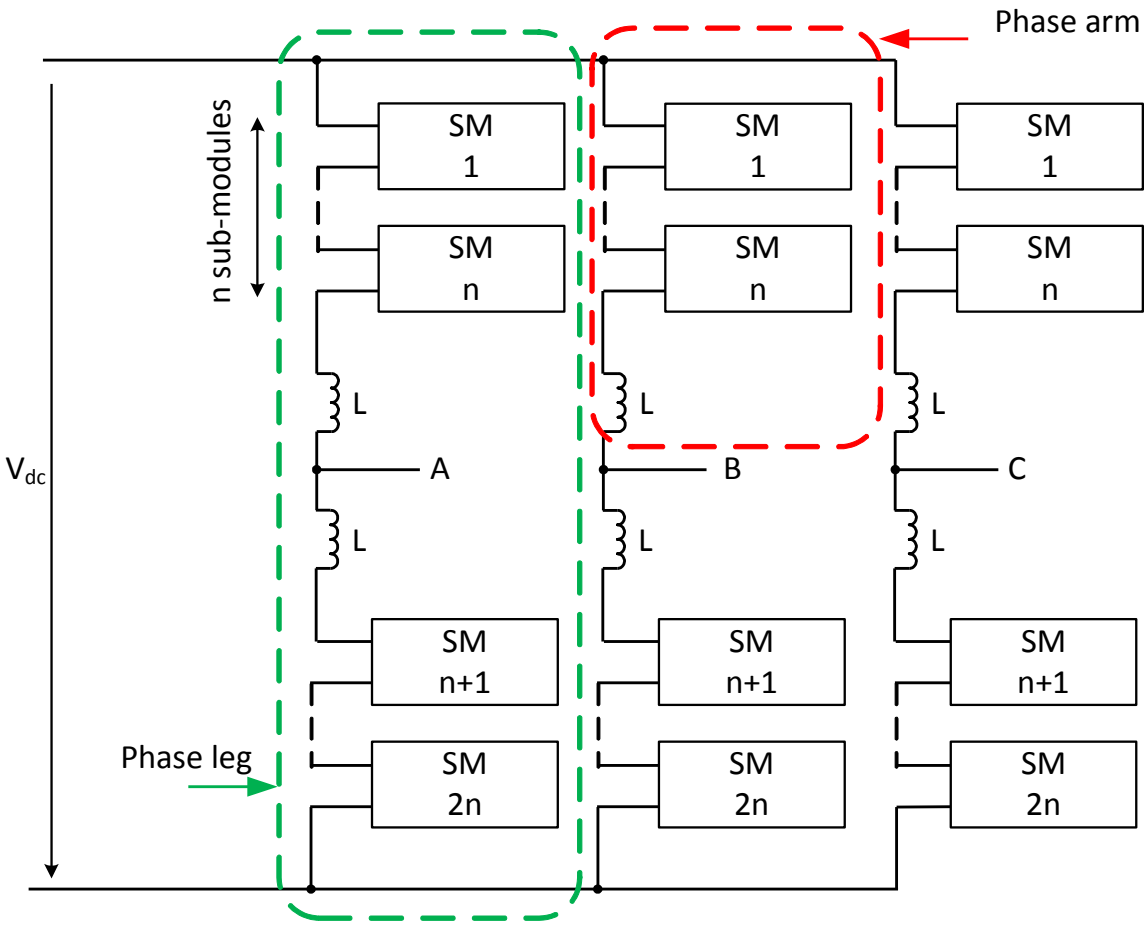

Figure 2-5 - Three-phase MMC topology [18]

where:

V_C - DC link voltage;

n - number of SMs per arm.

The output AC voltage can be summarised as the sum of the SM voltages in each arm. The output voltage (v_m) for each arm can be expressed as:

$$v_m = \frac{V_{dc}}{2} - n_u\left(\frac{V_{dc}}{2n}\right) - L\left(\frac{di_m}{dt}\right) \tag{2.2}$$

$$v_m = -\frac{V_{dc}}{2} + n_l\left(\frac{V_{dc}}{2n}\right) + L\left(\frac{di_m}{dt}\right) \tag{2.3}$$

where:

n_u - number of inserted SMs in the upper arm;

n_l - number of inserted SMs in the lower arm.

According to the above equations, a staircase output voltage can be obtained, by controlling the number of SMs inserted at a certain instance. As the output of each SM can be zero or V_C, and assuming that there are 2n SMs in each leg, by analysing the two equations, it can be notice that at each given time, then number of connected SMs in each leg should be n.

Being a modular converter, makes the MMC easily scalable in terms of power and voltage ratings, while at the same time allowing for a high availability by providing redundant SM in the design, leading to low down-time. As the effective switching frequency is directly proportional to the number of SMs present in the converter, it can get in the range of kHz, while the semiconductors only switch with a few hundred Hz, resulting in low losses [18].

2.3 Converter sizing

The three main components in the design of the converter are the: switching semiconductors, SMs capacitors and arm inductors. In this sub-chapter the main equations needed for the dimensioning of the devices are presented.

The capacitors, when inserted, will behave like voltage dividers, allowing to obtain different steps in the output waveform. For the operation principle of the MMC, it can be noticed that each capacitor has to be rated for the DC-link voltage divided by the number of SMs in the arm, but at the same time considering the voltage ripple and redundancy. One other important selection criterion is the storage capability of the capacitors. As the DC-link capacitor is removed, the converter needs to be able to provide power during transients in the DC-link.

The main criterion to select the arm inductors is the fault current rise rate limitation. Due to the series connections, the inductors can provide protection in case of both external and internal faults, thus preventing damage to the switching devices [9, 19].

2.3.1 Sub-module capacitor sizing

Since the bulky DC-link capacitor is removed by design, the DC-link voltage can be assumed non-constant. Therefore, during transients, the output power must be provided from another source. This means that the SMs capacitors have to be dimensioned in order to be able to pass such transients without disconnecting and also to provide fault-ride-through [4]. Another criterion for the capacitor dimensioning is the DC-link support. Since the DC-link capacitor is replaced by the SMs capacitors, they have to be designed to support the stability of the DC-link and transients during faults. This translates into voltage ripple across the capacitors. The used rule of thumb is to keep the voltage ripple under 10% for good operation conditions. The mainly used dimensioning calculations are presented in [4] and [17]. In [17], Dorn recommends that the total capacitor stored energy to be between 30-40 kJ/MVA for the rated power of the converter, while in [4] Marquardt proposes an analytical expression based on the SM energy ripple, which allows the voltage ripple to be selected.

In order to simplify the analysis, the MMC can be reduced to the model shown in Figure 2-6.

Each arm of the converter can be simplified to a controlled voltage source with a sinusoidal output voltage. The arm current can be split into two parts: $i(t)$ which is the output current of the respective arm and I_C which is the circulating current of the leg and is responsible for charging and discharging the SMs capacitors. Therefore, it can be concluded that, under ideal conditions, the output current is divided equally between the upper and lower arms. The equation of the upper arm current can be written as:

$$i_P(t) = I_C + \frac{1}{2} i(t) = I_C + \frac{1}{2} i_m sin(\omega_N t + \varphi) \tag{2.4}$$

where:

i_m - peak output current;

Figure 2-6 - MMC simplified model [34]

ω_N - output angular frequency;

φ - phase shift between output voltage and current.

Assuming a three-phase system symmetrically loaded, the circulating current in each phase is equal to 1/3 of the DC-link current I_{dc} and can be expressed as:

$$I_C = \frac{1}{3} I_{dc} \tag{2.5}$$

The current modulation index will be:

$$m = \frac{i_m}{2 \cdot I_C} \tag{2.6}$$

By introducing equations (2.5) and (2.6) into (2.4) it results:

$$i_P(t) = \frac{1}{3} I_{dc} \cdot \left(1 + m \cdot sin\left(\omega_N t + \varphi\right)\right) \tag{2.7}$$

From Figure 2-6, the upper arm voltage $v_P(t)$ can be expressed as:

$$v_P(t) = \frac{V_{dc}}{2} - v_N(t) = \frac{V_{dc}}{2} - v_m sin\left(\omega_N t\right) \tag{2.8}$$

where:

v_m - peak line-to-neutral output voltage;

V_{dc} - voltage of the DC link.

and the modulation index k is:

$$k = \frac{2 \cdot v_m}{V_{dc}} \tag{2.9}$$

Substituting equations (2.8) and (2.9) into (2.7):

$$v_P(t) = \frac{V_{dc}}{2} \cdot \left(1 - k \cdot sin\left(\omega_N t\right)\right) \tag{2.10}$$

Then, the active output power of the converter P_{AC} can be represented as:

$$P_{AC} = \frac{3 \cdot v_m \cdot i_m}{\sqrt{2} \cdot \sqrt{2}} cos\varphi = \frac{3 \cdot V_{dc} \cdot I_C}{2} \cdot k \cdot m \cdot cos\varphi = \frac{P_{dc}}{2} \cdot k \cdot m \cdot cos\varphi \tag{2.11}$$

Assuming all components are ideal ($P_{AC} = P_{dc}$), equation (2.11) can be manipulated to express the current modulation index m based on the voltage modulation index k:

$$m = \frac{2}{k \cdot cos\varphi} \tag{2.12}$$

The output power of the upper arm can be obtained from the product of the current (equation (2.7)) and voltage (equation (2.10)) of the upper arm:

$$P_P(\omega_N t) = \frac{V_{dc} \cdot I_{dc}}{6} \cdot \left(1 - k \cdot sin\left(\omega_N t\right)\right) \cdot \left(1 + m \cdot sin\left(\omega_N t + \varphi\right)\right) \tag{2.13}$$

Integrating the above equation over two periods and substituting equation (2.12) gives:

$$\begin{cases} x_1 = -\varphi - arcsin\left(\dfrac{1}{m}\right) \\ x_2 = \pi + arcsin\left(\dfrac{1}{m}\right) - \varphi \end{cases} \tag{2.14}$$

From this, the energy change across the arm can be obtained as:

$$\Delta W_{source}(k) = \frac{2}{3} \cdot \frac{S}{k \cdot \omega_N} \cdot \left(1 - \left(\frac{k \cdot cos\varphi}{2}\right)^2\right)^{\frac{3}{2}} \tag{2.15}$$

where S is the apparent power of the MMC.

Assuming n SMs per arm in the converter, the energy change in one SM can be expressed as:

$$\Delta W_{SM}(k) = \frac{2}{3} \cdot \frac{S}{k \cdot \omega_N \cdot n} \cdot \left(1 - \left(\frac{k \cdot cos\varphi}{2}\right)^2\right)^{\frac{3}{2}} \tag{2.16}$$

If the voltage ripple of the SM capacitor of $\pm\varepsilon$ around the nominal voltage ($V_{SM,nom}$), the energy of the SM can be expressed as:

$$W_C\left(V_{SM,nom}\right) = \frac{1}{2} \cdot C_{SM} \cdot V^2_{SM,nom} = \frac{1}{4 \cdot \varepsilon} \cdot \Delta W_{SM} \tag{2.17}$$

From the above equation, the SM capacitance for the desired voltage ripple is given by:

$$C_{SM} = \frac{\Delta W_{SM}}{2 \cdot \varepsilon \cdot V^2_{SM,nom}} \tag{2.18}$$

2.3.2 Arm inductor sizing

The arm inductors can be dimensioned to limit the fault current rise-rates [19] or the current ripple [20].

2.3.2.1 Fault current rise-rate limitation

Generally, the arm inductors that limit the fault current rise-rate are selected for the most critical case: DC-link short circuit. In order to simplify the analysis, the voltages over the SMs capacitors can be assumed constant. At the time of the fault, the voltage across the inserted capacitors will be equal to V_{dc}. Applying Kirchhoff's voltage law at the output point of the leg, the voltage drop across the upper and lower arm inductors is:

$$L\frac{di_{Pa}}{dt} + L\frac{di_{Na}}{dt} - V_{dc} = 0 \tag{2.19}$$

where:

L - inductance of arm reactors;

i_{Pa} - positive arm current;

i_{Na} - negative arm current.

Considering that, at the instance of the transient, both arm currents can be assumed equal ($i_{Pa} = i_{Na}$), equation (2.19) can be rewritten as:

$$\alpha = \frac{di_{Pa}}{dt} = \frac{di_{Na}}{dt} = \frac{V_{dc}}{2L} \tag{2.20}$$

where α is the rise-rate of the fault current in kA/s. The value of the arm inductor based on the current rise-rate can be obtained by rewriting the above equation:

$$L = \frac{V_{dc}}{2\alpha} \tag{2.21}$$

The current rise-rate has to be chosen so that the semiconductors are able to switch off within their nominal current range in order to avoid damage of the devices and to prevent the discharge of the capacitors. This will allow the removal of the DC-link circuit breakers [9].

2.3.2.2 Current ripple limiting

Considering coupled arm inductors, they will only affect the output current $i(t)$ resulting in a reduced volume of the core. The Kirchhoff's voltage law in this case, at the output of the leg, can be represented as:

$$U_C = u_p + u_n + u_L \tag{2.22}$$

Assuming that the allowable maximum ripple current $\Delta i_{c,\max}$ is not exceeded, the inductance L can be calculated. Deriving the flux linkage from equation (2.22), it results:

$$\psi_L = L\bullet \qquad \bullet \qquad \bullet \qquad _{,n,\max}) \tag{2.23}$$

where:

D_L - duty-cycle across the inductor;

T_a - modulation period;

$u_{Cap,p,\max}$, $u_{Cap,n,\max}$ - maximum capacitor voltage in the upper, respectively lower arm.

According to [20] the maximum current ripple occurs at $D_L = 0.5$. Under normal operations the upper and lower capacitors voltages are equal. Based on this, the inductance equation can be written as:

$$L = \frac{0.25 \bullet}{\Delta i_{C,\max}} \bullet \tag{2.24}$$

2.4 Control topologies

Compared to classical converters, due to its modular design and operation, the MMC allows for two types of control, each with its advantages and disadvantages.

Although both control topologies will be presented, this project will only focus on the distributed one, since that is more demanding in terms of communication bandwidth and update speed.

2.4.1 Centralized Control

The centralized control resembles the classical one, which can be found on every traditional converter. During operation, based on different inputs and measurements, the controller calculates the state of each switch and then sends the gate signals to them. Figure 2-7 illustrates a simple diagram of the control.

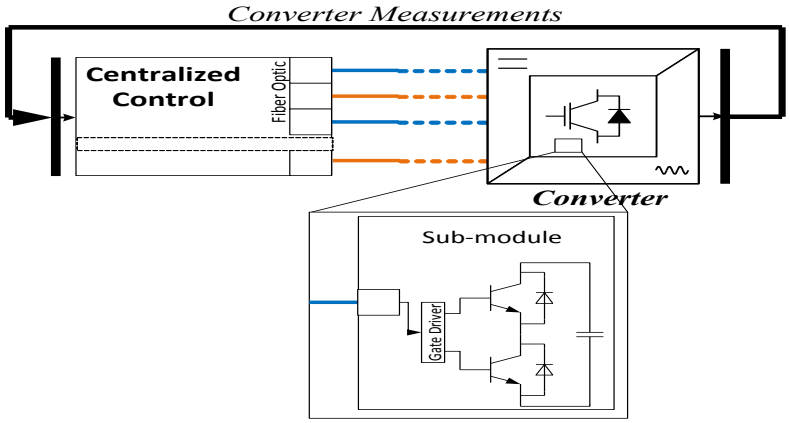

Figure 2-7 – Centralized control and SM diagram

This type of converter allows for a simpler implementation when it comes to control coordination, while at the same time requiring more power from the controller in order to accommodate the large amount of measurements which need to be processed and the large amount of signals which need to be generated. At the same time it requires a large number of communication lines in order to control each SM state and to acquire the measurements. This is typically implemented over fibre optics to accommodate the voltage difference between each board. The measurements generally involve only

SMs voltages. This control can accommodate for longer measurements delays but requires fast transmission for the gate signals.

2.4.2 Distributed Control

The distributed control is an implementation made possible by the modular design. It provides different advantages over the centralized one, but at the same time it comes with some implementation challenges.

In this case, the control is divided between a high level control which takes care of the Phase Lock Loop (PLL), the DC-link support and other high level controls, while at same time performing basic calculations to help in the balancing of the SM and by-pass in case of fault. The modulation and measurements are taken care of by the SM controller.

This allows for a more flexible and modular implementation, facilitating the scaling of the converter at high levels with little to no modification, except an increase in the number of variables in order to account for the additional SMs. Since the calculations are distributed between each SMs, there is no requirement for a high power controller. Figure 2-8 shows a simple diagram of such a control strategy.

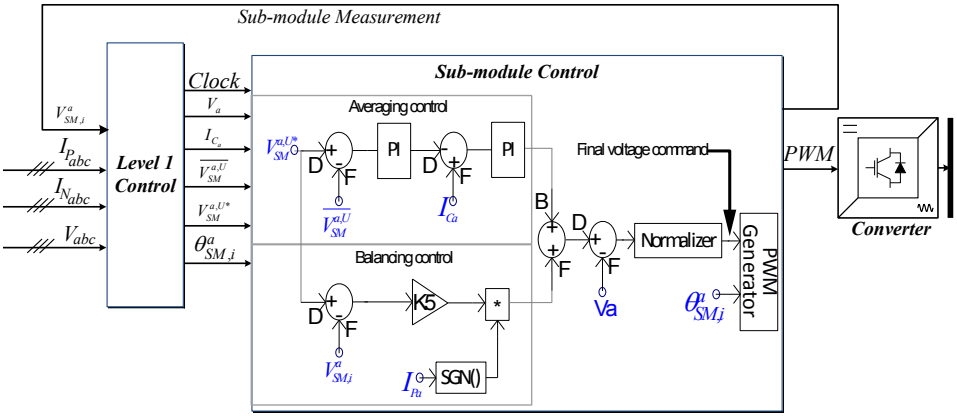

Figure 2-8 – Distributed control and SM diagram [36]

Although the calculation requirements of the central (or master) controller are lowered and the control is simpler to implement, the communication requirements will increase in order to accommodate for the measurements and data needed for the modulation. Since the measurements are generally needed in the control and usually involve more data (voltage/currents/SM state), this type of control requires a faster communication in order to have a good control, but due to the distribution, it should be able to allow for delays in the communication without affecting the switching.

2.5 Modulation strategies

There are three main classic modulation strategies generally used for MMC control: the State Space Vector Modulation (SVM) [21], Duty Cycle and Time Delayed or Sine Pulse-Width Modulation (SPWM) [22]. The SVM and Duty Cycle modulation are only suitable for the centralized control strategy and cannot be used for the distributed one, while the PWM can be accommodated in both control strategies. Although all three modulation strategies will be briefly presented, emphasis will be placed only on the SPWM.

2.5.1 Space Vector Modulation

SVM is basically a PWM algorithm where the switching times are calculated based on the three-phase space vector representation of the AC reference and the inverter switches states [23].

This algorithm uses the stationary α-β frame, where the voltage state-space vector v_s which combines the three-phase variables is defined by the equation:

$$v_s = \frac{2}{3}\left[v_a + a \cdot v_b + a^2 \cdot v_c\right] \tag{2.25}$$

where $\alpha = -(1/2) + \left(j \cdot \sqrt{3}/2\right)$. By inserting in equation (2.25) the outputs of the inverter (v_a, v_b, v_c) for each possible switching state, the inverter state-space vectors can be obtained. A 3^3 (generally the number of possible states of a three-phase convert with N-levels is equal to N^3) state-space vectors of an NPC 3-phased converter is shown in Figure 2-9[23].

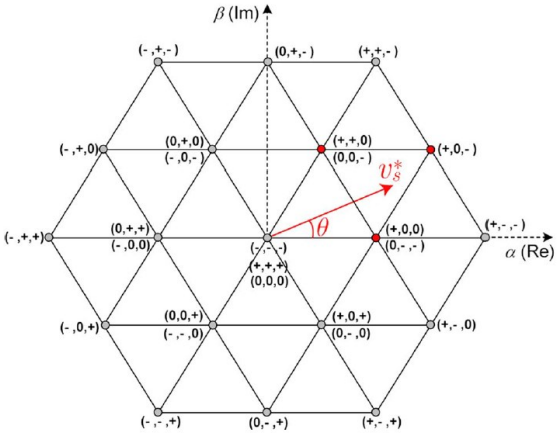

Figure 2-9 – Three-phase three-level converter state-space vectors [23]

In case of the MMC, the state-space vectors will represent the states of the SMs in the upper arms of each phase, while the switches in the other arms will have their states mirrored.

2.5.2 Duty Cycle

This modulation strategy is based on the calculation of the expected voltage output based on the number of SMs in each arm. Considering *n* numbers of SMs in each arm, the arm duty cycle d_{upper} can be calculated using:

$$d_{upper} = \frac{v_m sin\left(\omega_N t\right) - \frac{V_{dc}}{2}}{V_{SM}} \tag{2.26}$$

where V_{SM} is the average voltage of the SMs in the upper arm. As the arm duty cycle is mostly a fractional number, the integer part of the number will represent the number of SMs which will be fully inserted while the sub-unitary number will be the modulation index of another SM.

This modulation scheme is only suited for the centralized control strategy.

2.5.3 Sine Pulse-Width Modulation

As with any multilevel converter over the years there have been many SPWM techniques proposed for driving the MMC. As mentioned before, SPWM can be used for both types of control, but it is the only one suitable for the distributed one. The main idea behind it, is to compare a sine wave, which is the desired output of the converter, to one or more triangular signals specially distributed. When the sine is smaller than the triangular carrier, the output of the PWM module is zero, and vice-versa. Generally the sine wave has the grid frequency while the carrier has a much higher frequency, named

switching frequency. As the number of levels increases, the carriers' frequencies can decrease, in order to limit the switching losses, without affecting the total switching frequency or distorting the output quality.

Among the most important SPWM techniques one can find the Phase Disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposition Disposition (APOD) and Phase Shifted (PS) schemes [24]. For carrier disposition schemes, with n number of SM, n+1 voltage levels can be obtained. For the PD scheme (Figure 2-10a), all the carrier signals are in phase. In the PODs case (Figure 2-10b), the carriers above zero are all in phase, while the ones under zero are in phase to each other and shifted 180˚ in reference to the upper ones. For the APOD (Figure 2-10c) scheme, each carrier is phase shifted by 180˚. The PS scheme (Figure 2-10d) distributes the carrier equally between zero and 2π. This can be done in 2 ways: phase shifting the carriers for the upper arm and using their inverted counterpart for the lower arm, or phase shifting the entire SMs carriers for the whole leg [25-28].

One of the main advantages of the PS scheme is the harmonic content, since they appear only as sidebands centred on the $2 \cdot N \cdot f_s$ frequency in the output voltage, where N is the number of carriers used in the leg and f_s is the frequency of the triangular carriers [29].

Even if the individual carriers' frequency is not very high, the inverter equivalent output voltage frequency is very high. When implementing this type of modulation in a microcontroller, the phase shift of each individual SM in each arm is calculated using the following:

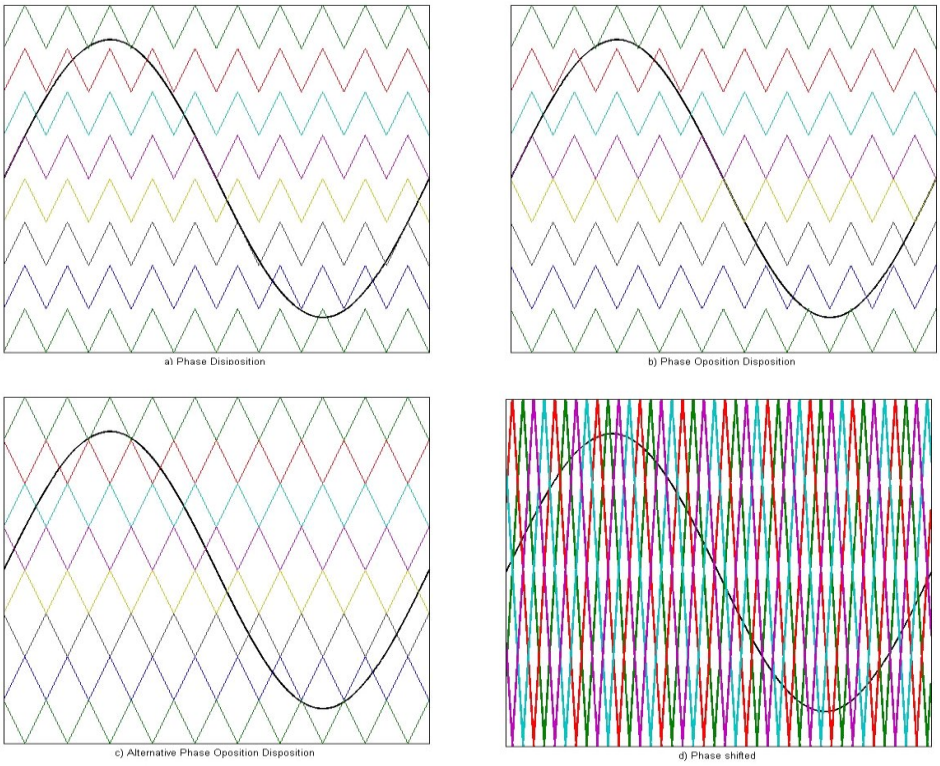

Figure 2-10 – Sine Wave Pulse Width Modulation schemes for 9-level MMC a)Phase Disposition; b) Phase Opposite Disposition; c) Alternative Phase Opposite Disposition; d) Phase Shifted

$$Phase\,Shift\,Time = \left[\frac{(K-1)}{N}\right] \cdot \frac{T_S}{2} \tag{2.27}$$

where:

K – position of SM in the arm;

N – total number of SMs in the arm;

T_S - period of the carrier signals.

Since each SM can be viewed as an insulated DC-source by interleaving their output, the phase voltage is the sum of the output voltages of each SM.

The PS scheme seems the most appropriate modulation strategy to be further implemented, due to its lower harmonics content [29].

2.6 Balancing Strategies

During the operation of the MMC, the SMs capacitors experience an unequal share of the load. This translates in a difference between the voltages of the SMs. This will affect the output voltage of the converter as well as the efficiency and quality of the output. This unbalance, if not controlled, may damage the capacitors in the SMs due to over voltage.

There are several methods to maintain a constant voltage across the capacitors. The two main strategies are presented in the following subchapters.

2.6.1 Sort and Select

This method is described in detail in [30, 31] and will be briefly presented here since it is only suited for centralized control. It is based on the sorting of the SMs and arranging them based on their capacitors voltage. The algorithm then decides which SMs should be in On-state or OFF-state for each cycle based on the current direction. The current flows through each capacitor when the SM is in the ON-state (Figure 2-4). If the current flows in the positive direction the capacitor gets charged and the voltage increases. The capacitor gets discharged and the voltage decreases when the currents flows in the opposite direction. When the SM is OFF, the current will flow through the lower switch without having any impact on the capacitor voltage and charge. The sorting algorithm will switch on the SMs with the lowest voltage when the current flow is positive and the SMs with the highest capacitor voltages when the current flows in the negative direction. The main advantage of this method is that at any time, it ensures a number of *n* SMs in the leg connected across the DC-link. This translates in a smaller arm inductor since the circulating current is smaller [32].

2.6.2 Distributed Balancing Control

A novel balancing strategy for SM capacitor voltages has been proposed in [22, 33]. This is especially suited for the distributed control. It is based on the equally sharing of the arm energy by the capacitors. It uses the PS SPWM modulation strategy, which means that each SM has its own modulation reference (shifted triangular), and because of this, there is no guarantee that at any given type there will be *n* SMs connected across the DC-link. This will require larger arm inductors compared to the Sort and Select Method.

The advantage of this method comes from the higher number of voltage levels that can be obtained, which will result in smaller harmonics content [32].

Considering a three phase converter with the legs connected in parallel to the DC-link as shown in Figure 2-11. Since at any given time the generated voltage outputs of each leg are not equal, circulating currents will appear between individual legs of the converter. Because the converter legs are considered identical, further analysis will be done only on phase a.

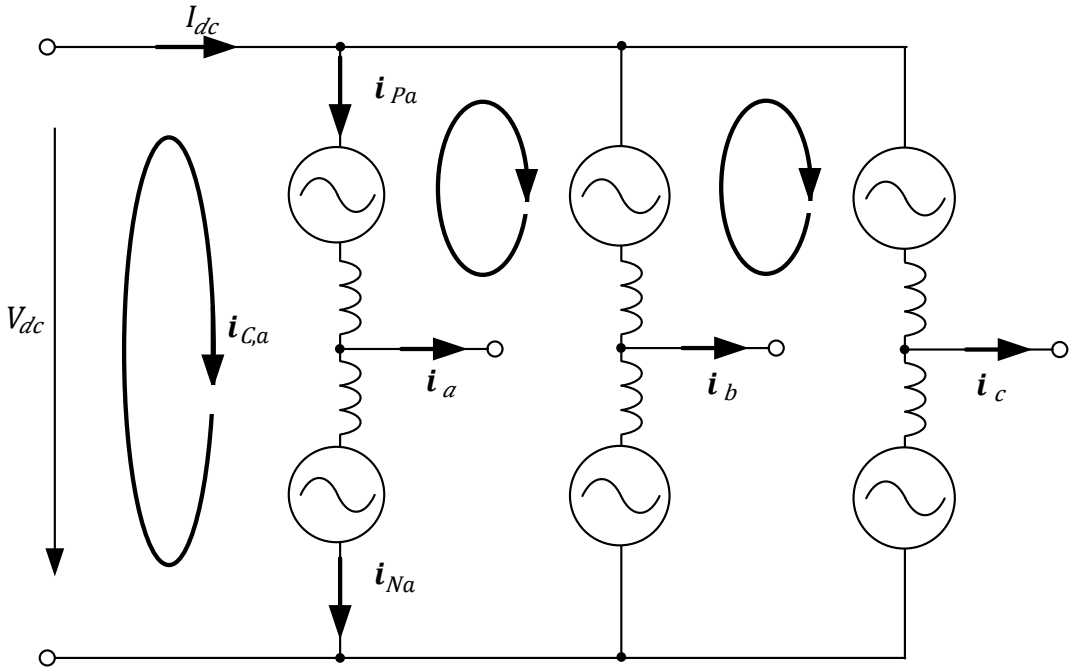

Figure 2-11 – Circulating currents in converter [34]

In Figure 2-11 the positive i_{Pa} and negative i_{Na} arm currents are shown. The circulating current i_{Ca} in the phase a loop represents the mean of the arm current and the output current of the leg is defined as i_a. Due to the symmetry of the upper and lower arms, it is safe to assume that the load current is equally distributed between them. Applying Kirchhoff's current law in node at the output of phase a, the circulating current of the phase can be computed as:

$$i_{Ca} = i_{Pa} - \frac{1}{2} i_a = i_{Na} + \frac{1}{2} i_a = \frac{1}{2}\left(i_{Pa} + i_{Na}\right) \tag{2.28}$$

Observing the equation, it can be noticed that the AC current output does not influence the circulating current i_{Ca}. This circulating current flowing through the legs will influence the arm currents and create unbalance in the capacitors voltages. This can be suppressed by the arm inductors or by controlling the SMs states.

The distributed balancing control is split up into two parts: the averaging controller (or master controller) and the balancing control (or SM controller). The averaging controller is implemented for the entire leg of the converter and will also tolerate operation with faulty SM in the arms. The block representation of the averaging controller is presented in Figure 2-12.
$v_{Cj,ref}$ represents the capacitor voltage reference signal for the entire arm. $v_{Cj,av}$ is the average voltage of all the capacitor in the arm, i^*_{Cj} is the circulating current command, v_{Aj} is the voltage command given by the averaging control and j is the phase index. The average voltage control of the arm capacitors voltages is:

$$v_{Cj,av} = \frac{1}{n}\sum_{i=1}^{n} v_{Cij} \tag{2.29}$$

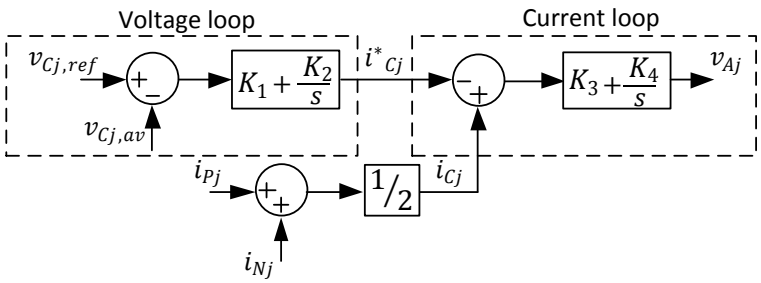

Figure 2-12 – Averaging controller [34]

where *i* represents the position of the SM in the arm. The circulating current reference is expressed as:

$$i^*_{Cj} = K_1\left(v_{Cj,ref} - v_{Cj,av}\right) + K_2\int\left(v_{Cj,ref} - v_{Cj,av}\right) \tag{2.30}$$

where K_1 and K_2 are the gains of the voltage PI controller. While the voltage reference output command of the averaging controller is written as:

$$v_{Aj} = K_3\left(i_{Cj} - i^*_{Cj}\right) + K_4\int\left(i_{Cj} - i^*_{Cj}\right) \tag{2.31}$$

where K_3 and K_4 are the gains of the voltage loop PI controller.

When the reference for the capacitor voltage is bigger than the average voltage, the circulating current command will increase. This will force the circulating current i_{Cj} to follow the command. Based on this $v_{Cj,av}$ will follow the reference $v_{Cj,ref}$ independently of the load current.

The balancing controller which will be implemented on each SM is presented in Figure 2-13.

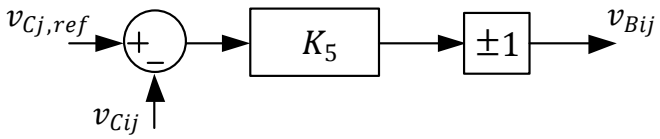

Figure 2-13 – Balancing controller [34]

$\boldsymbol{v_{Cij}}$ is the voltage measured across the i-th SM, $\boldsymbol{K_5}$ is the proportional gain of the controller and $\boldsymbol{v_{Bij}}$ will be the balancing command for the i-th SM. The ±1 multiplier accounts for the direction of the arm current, since this will influence the charging capacitors depending on its direction. When the SM capacitor voltage is lower than its reference ($\boldsymbol{v_{Cj,ref} \geq v_{Cij}}$), the capacitor should be charged. The voltage reference from the balancing control for the upper arm can be expressed as:

$$v_{Bij} = \begin{cases} K_5\left(v_{Cj,ref} - v_{Cij}\right), \left(i_{Pj} > 0\right) \\ -K_5\left(v_{Cj,ref} - v_{Cij}\right), \left(i_{Pj} < 0\right) \end{cases}, for\ i = 1 \div \frac{m}{2} \tag{2.32}$$

And for the lower arm:

$$v_{Bij} = \begin{cases} K_5\left(v_{Cj,ref} - v_{Cij}\right), \left(i_{Nj} > 0\right) \\ -K_5\left(v_{Cj,ref} - v_{Cij}\right), \left(i_{Nj} < 0\right) \end{cases}, for\ i = \frac{m}{2} + 1 \div m \tag{2.33}$$

The final SM reference signal which will be fed into the PWM comparator for the upper and the lower arms can be expressed as:

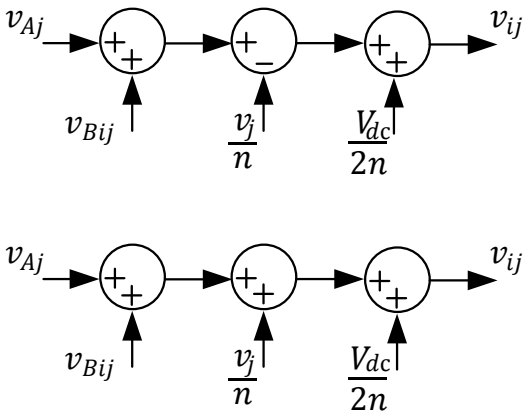

Figure 2-14 – Final SM voltage reference[34]

$$v_{ij} = v_{Aj} + v_{Bij} - \frac{v_j}{n} + \frac{V_{dc}}{2n},\ for\ i = 1 \div \frac{m}{2} \tag{2.34}$$

$$v_{ij} = v_{Aj} + v_{Bij} + \frac{v_j}{n} + \frac{V_{dc}}{2n},\ for\ i = \frac{m}{2} + 1 \div m \tag{2.35}$$

where v_j is the arm AC voltage reference. This is graphically represented in Figure 2-14.

From equations (2.34) and (2.35), it can be observed that the SM reference command is a combination of the averaging and balancing commands with the reference voltage $\boldsymbol{v_{ij,ref}}$ for the SM which can be written for the upper and lower arm as:

$$v_{ij,ref} = -\frac{v_j}{n} + \frac{V_{dc}}{2n} \tag{2.36}$$

$$v_{ij,ref} = \frac{v_j}{n} + \frac{V_{dc}}{2n} \tag{2.37}$$

where $\frac{V_{dc}}{2n}$ is the feed-forward control of the DC link voltage. The SM voltage reference signal (v_{ij}) will be inserted into the PWM block, where it is compared with triangular waveform in order to create the complementary gate signals for the SM transistors. This modulation has proven good characteristics when used with an asynchronous frequency [34].

2.7 In-rush Protection

Because of its construction, the MMC needs to be able to withstand faults without affecting the devices and minimizing the impact of the fault on the energy stored in the capacitors. One of the least desirable faults is the DC-link short-circuit, which might give rise to high in-rush currents [19] which might damage the devices until the DC-link switches can be opened.

In order to be able to handle the in-rush currents which might appear from DC-faults, the converter has to have fast reaction times in order to bypass itself within the safe-operation parameters of the switching devices. This can be done by properly selecting the arm-inductors in order to limit the current rise-rate so that the SM controller has sufficient time to react. By implementing a hardware over-current protection the reaction times of the SMs can be minimized, and coupled with over-dimensioned current handling capabilities for the switches ensures that small transients, like SM failure or change of reference, won't affect the proper operation of the converter by triggering the

protection. Transistor *T* (Figure 2-15) can be used to protect the free-wheeling diodes during such transients.

2.8 Fault tolerance

Since high availability time is very desirable, the MMC is generally designed with redundant SMs. A redundant SM can be defined as a SM which was added as an extra after the calculations for the energy stored was done. It will participate in the modulation although it isn't needed and its main purpose is to compensate, in case one SM will fail.

Because of its design, redundant SMs can be easily added, and their number is decided by the expected failure rate of the devices and the desired maintenance interval. In theory there can be as many redundant SMs as wanted, but they will increase the cost of the converter.

Figure 2-15 shows the implementation of the SMs protection devices in green and the devices which might fail in red.

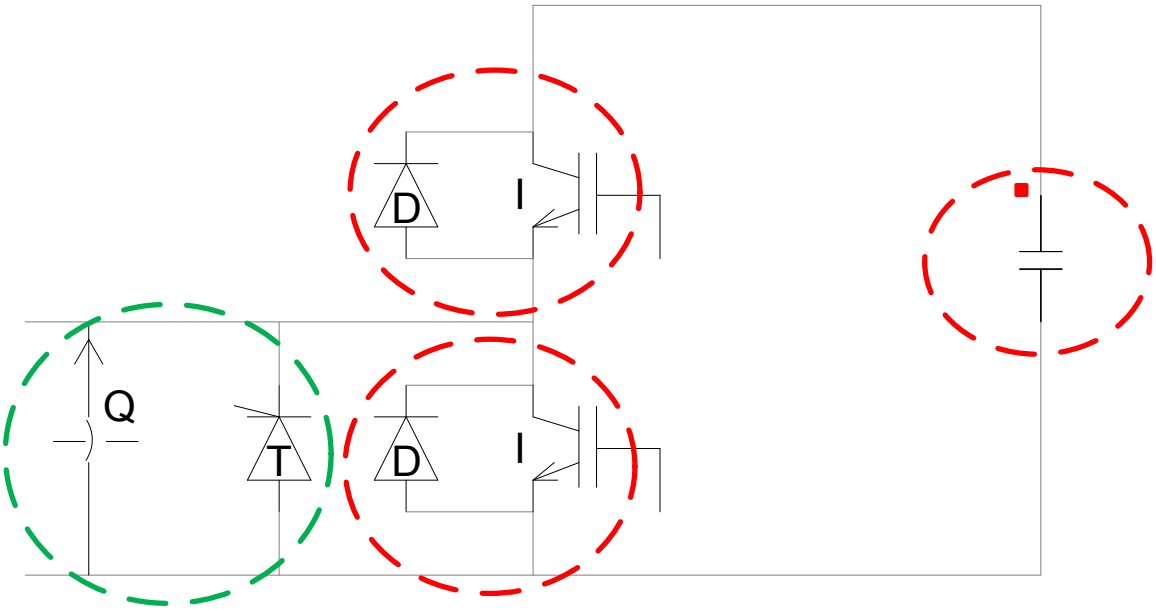

Figure 2-15 – Sub-module elements subjected to failures (red) and required protection

When a SM fails, it is highly desirable to continue operation until it can be replaced during maintenance. A failure might appear from a shorted capacitor, or from a destroyed semiconductor. Some manufacturers implement devices which short-circuit themselves when failed, ensuring that the operation can continue without needing other switches. Others implement a permanent switch *Q* for when the SMs needs to be taken out of the modulation [1, 7].

When a SM is bypassed, it will not participate in the modulation and its capacitor voltage will be neglected. At the same time the reference nominal voltage for the SM in the arm and the phase-shift between their carriers will be adjusted to compensate for its removal and have an equal distribution of the switching across a period. At the same time, from this, it can be concluded that the sub-module capacitors need to be over rated in order to ensure that in case of SM failure the other ones can accommodate for the increased voltage.

2.9 Converter Start-up

One important challenge concerning the MMC is the start-up or energization phase. Although this is an important aspect, it has not been discussed too much in literature and little information about it exists.

Since in the beginning all the capacitors in the converter are discharged, at the instance of the connection to the AC grid, high and fast rising currents will appear in the arms which may stress the SMs switches and capacitors beyond their limits and destroy the converter. An identical situation is experienced after the DC-link is energized and the back-end converter has to be energized from the DC-link.

One start-up procedure suitable for the centralized control is presented in [35]. It is based on the duty-cycle controller with sort and select balancer and will be explained more in the next subchapter.

This project will propose another start-up procedure based on the distributed balancing control and will be presented in subchapter 2.9.2.

Since the energization of the converter can be done from both sides (DC/AC) in an identical fashion, the presented procedures will consider energization from the DC-link. This is done because it is much simpler to illustrate the procedures.

2.9.1 Sort and Select based start-up procedure

In [35], the authors propose a novel start-up scheme based on the sort and select balancing method. Figure 2-16 presents a simplified single phase inverter with six SMs for the explanation. The DC side of the converter is considered energized from a non-controlled rectifier.

The charging procedure can be split into two main stages. First the DC-link is energized and the capacitors are charged to half of their nominal voltage. In the second stage, each SM capacitor is charged to its rated voltage.

In stage 1, the AC switch S1 will be closed and the S2 switch will be opened while all the SMs are inserted. While the DC-link will be charged to its rated value, each SM capacitor will be charged to half of it nominal voltage ($\frac{V_{dc}}{2n}$). The resistors on the AC side will limit the charging currents to a safe value. When the DC-link reaches its rated value, the next stage can start.

In the second stage, both S1 and S2 will be closed. At this point the sum of the SMs voltages are equal to the DC-link voltage and no current flows through the leg. In order to trigger a circulating

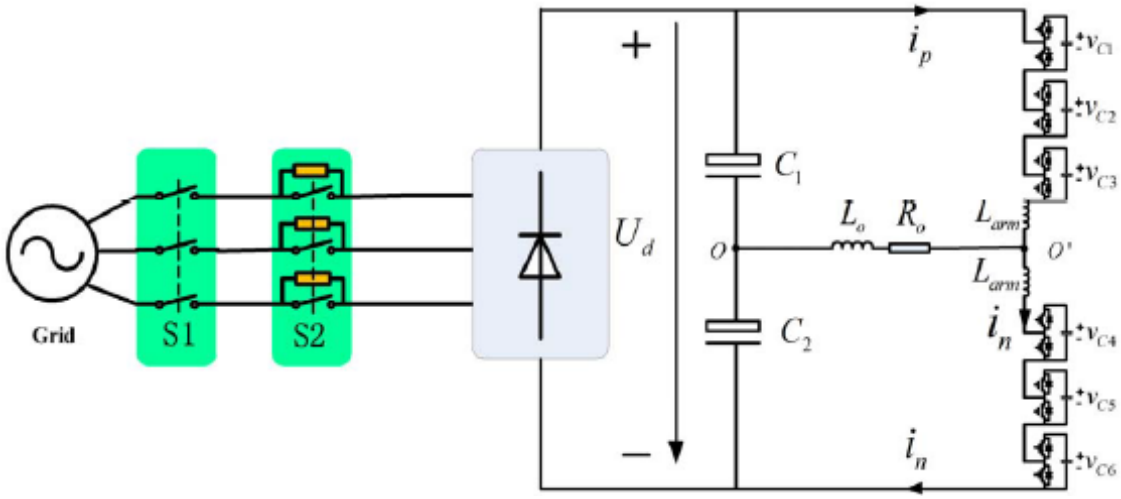

Figure 2-16 – Single phase six-module inverter [35]

current which will charge the capacitors, some SMs need to be by-passed. If the SMs inserted in the upper arm are equal to the lower arm, no voltage difference will appear across the load ($R_0 L_0$) so no load current will flow. For a better explanation, the second stage can be divided into two parts.

In substage 2.1, two SMs in each arm are always connected and the third one is modulated with its nominal switching frequency T_S with a duty cycle varying from 1 to 0 linearly with a slope which guarantees safe operating currents. The state of the modulated SM toggles between inserted and by-passed with each switching period. When the SM is by-passed, the arm current will rise and the inserted SMs will get charged. When it is inserted, the arm currents will decrease. In order to keep the SMs capacitors voltages balanced, the scheme uses the Sort and Select balancing algorithm to decide which modules should be modulating and which should be inserted. This will ensure that all capacitor will get charged as the duty cycle decreases.

In substage 2.2, one SM will be kept by-passed (duty-cycle zero), one will modulate and the third one will be inserted (duty-cycle = 1). This time, the modulating SM will vary its duty cycle linearly from 1 to 0.5. When the duty cycle reaches 0.5 all the capacitors will be charged to $\frac{V_{DC}}{3}$ (since there are three SMs in each arm). The Sort and Select balancing scheme will ensure that the modules are swapped with each other in order to ensure equal voltages.

2.9.2 Novel start-up procedure for distributed control

Since no start-up procedure for distributed control was found in the literature, a start-up procedure had to be investigated in order to allow to safely charge the converter before operation. The distributed start-up procedure uses the balancing method proposed in [22] and later improved in [33].

This procedure is split into two parts. In the first stage, the capacitors will be charged to half their nominal voltage, and in the second, one they will be modulated to their nominal voltage.

As shown in equation (2.18), the capacitance of each SM is designed based on the desired voltage, desired voltage ripple and energy of the SMs. When connecting all the SMs in series, the series equivalent capacitance, assuming *n* SMs in the arm, will be equal to:

$$C_{eq} = \frac{C_{SM}}{2 \cdot n} \tag{2.38}$$

Considering a typical converter which generally has a high number of SMs, the equivalent capacitance will get small.

The procedure will be explained on Figure 2-17. At the beginning of the first stage the converter is disconnected from both the DC-link (S1) and the AC grid (S2). The voltage across the capacitors is zero. Assuming the DC-link charged to its nominal voltage, S1 are closed and all the SM are inserted. Charging in-rush current will appear. This will be a fast-rising current but its peak should be well under the nominal operating current since the equivalent capacitance is small. The first stage stops when the voltage across the capacitors equals half of their rated voltage ($\frac{V_{DC}}{2 \cdot n}$) and there is no current flowing through the arms.

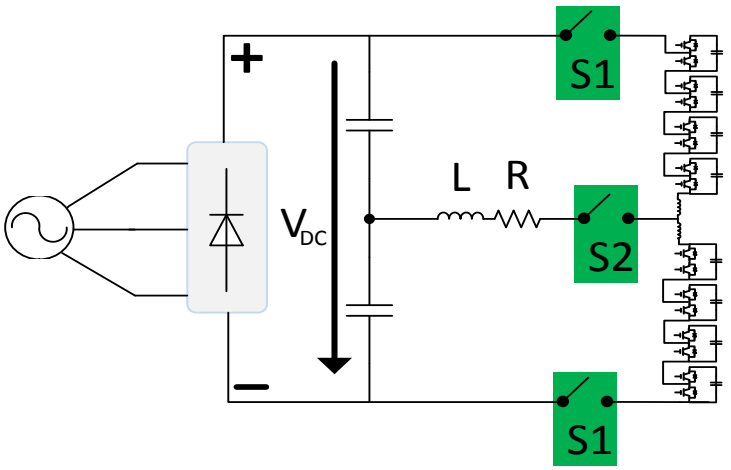

Figure 2-17 – Distributed control start-up converter

In stage 2, the averaging control will be tuned to supress the circulating current. And the voltage reference for the SMs capacitors ($v_{Cj,ref}$) will be increased linearly from $\frac{V_{DC}}{2 \cdot n}$ to their nominal voltage $\frac{V_{DC}}{n}$ with a slow rising slope. The SMs will not follow the reference within the $\pm\varepsilon$ designed characteristic, since the most important part of this stage is suppressing the arms currents (which at this point are only the circulating current) under a manageable value in order not to damage the semiconductors. The arm inductors will also help to supress the circulating currents. This stage will end when the arm SMs capacitors voltages average will be equal to their nominal value $\frac{V_{DC}}{n}$. At this point, the gains of the averaging control will be retuned in order to balance the capacitors within the $\pm\varepsilon$. S2 will be closed and the converter will commence normal operation.

This scheme is suited for the distributed control and will be used in the further implementation. A simulation model and experimental setup will be used in order to show its performance.

2.10 Summary

This chapter has introduced the MMC and described its main operational principles and advantages. In the first part, the calculation methods for the main components (capacitors and inductors) are explained. After that the modulation strategies are presented with their advantages. This is followed by the control types which can be used and the different modulation strategies which are recommended for this converter. Because its operating nature will cause the voltage across the capacitors to derail, two balancing controllers are recommended. At the end, a start-up procedure is described and a novel one, suited for a distributed control topology is proposed.

Based on the conclusions drawn from this part of the project, further work will focus on a MMC with distributed control since this is the most challenging part, but at the same time provides the most modularity. This will be used with the Sine Wave Phase Shifted PWM which appears to be the most efficient for this converter topology. Due to the unbalance which will appear between the SMs capacitors voltages, the distributed balancing controller will be applied and the proposed start-up procedure will be implemented.

3 EtherCAT Communication

The MMC with distributed control, phase shifted modulation and distributed capacitor voltage balancing requires a large bandwidth and fast updates times. For these reasons, an open-source fieldbus fast communication with low jitter will be investigated in this chapter.

3.1 Overview of communication requirements and protocols

On a simple overlook at the data which needs to be exchanged between the high-level controller and the SM controller, at least 14 bytes of data would be required for each SM and 4 bytes for the arm currents measurement for each leg. Table 3-1 summarizes the main variables dimensions which need to be transmitted.

Table 3-1: Variables dimensions for communication

Variable	bytes	Sender
Voltage Reference	2	Master
Sub-modules/arm	2	Master
Position/arm	2	Master
State	1	Master
Voltage command	2	Master
Capacitor Average Voltage	2	Master
Capacitor Voltage	2	SM
State-feedback	1	SM
Positive current	2	-
Negative Current	2	-

The communication can be broken into broadcasts or data for the entire leg and direct addressed data. The master will exchange with the individual SM the: position in the arm, the state requested, and the SM will reply with the capacitor voltage and current state. From the table the data dimension is noted as 6 bytes, but can be considered only 3 bytes since the communication is full duplex. The broadcast can be split into data for each arm which is represented by the number of SM in that arm (2 bytes) and data for the entire leg which is composed of the rest (6 bytes). The master will at the same time read in each leg the circulating currents (4 bytes) but those can also be disregarded in the calculation due to the full-duplex communication. Thus the data exchanged in bytes for a three-phase converter can be computed as:

$$Payload = 3 \cdot \left(\frac{6}{2} \cdot (2 \cdot n) + 6 + 2 \cdot 2 \right) \tag{3.1}$$

Considering 8 modules per leg, a three-phase converter would need 102 bytes of information transmitted from the master to the slaves, without accounting for the returned information. This could be achieved using a low speed communication like Serial Peripheral Interface Bus (SPI), Controller Area Network (CAN) or other types of communication with BUS topology [31]. As the converter size in terms of SM number will increase, the update times would be reduced in order to accommodate for the large data, which will result in a slow reaction time and might not be suited for a HVDC converter.

In order to keep the reaction times short and to accommodate for a large number of sub-modules, the communication could be implanted on a large bandwidth protocol, preferably standardized.

One of the best candidates which presents high bandwidth and fast update times is Industrial Ethernet and will be considered for this project. Currently it can offer speeds of up to Gps, large number of nodes and low cost hardware since it was developed and takes advantage of the well-established Ethernet communication protocol [36]. Compared to traditional Ethernet, which is defined in [37], Industrial Ethernet can guarantee determinism and low jitter with less overhead.

There are different implementations of industrial Ethernet currently on the market, developed for different systems like drives and control applications which require high bandwidth, fast update times and good clock synchronization. As most of the implementations are proprietary and closed source, their interconnection is complicated [36]. There have been a few which have been released as open-source and are widely used in different industrial fields: like EtherCAT and ProfiNet [38, 39]. Since it has shown better performance [40], EtherCAT was chosen as the communication solution for this project.

3.2 Introduction to EtherCAT

EtherCAT is an open-source communication protocol developed by Beckhoff and currently managed by the EtherCAT Group (ETG) [41]. It is implemented on Ethernet and it uses a standard Ethernet frame [37]. It is a fieldbus communication and it uses a Master-Slave configuration, where the Master has to initialize the communication. Both Master and Slaves can be implemented using of-the-shelf Ethernet interfaces: Physical Layer (PHY) and Media Access Controller (MAC). In order to minimize the delays which may appear from the forwarding, the slaves are implemented using hardware like Field Programmable Gate Arrays (FPGAs) and Application Specific Integrated Circuits (ASICs). The Master can be implemented on any off-the-shelf components and there are no special requirements for its communication hardware.

The EtherCAT communication can be described as *on the fly* communication. The communication is started by a master whom sends out an EtherCAT telegram through one of his PHY ports. As it passes through each EtherCAT Slave Controllers (ESC), data is read and written on the fly with little delay time, typically under 500 ns [40]. This is shown in Figure 3-1.

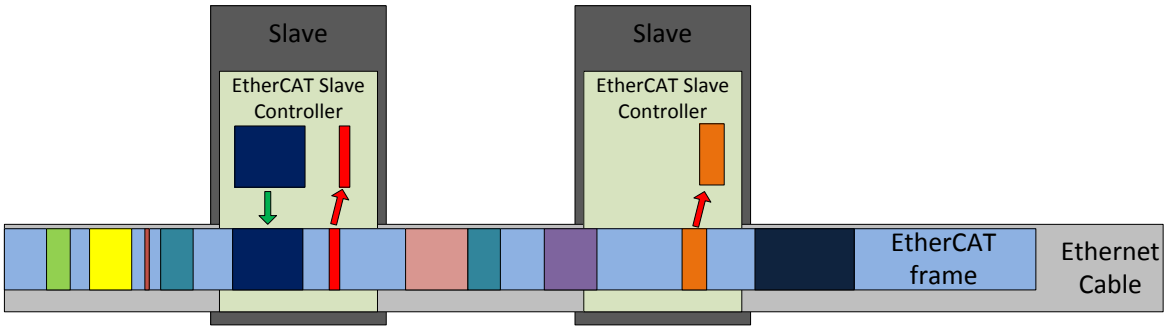

Figure 3-1 – On the fly principle

The EtherCAT frame is implemented on a Standard IEEE802.3 [37] Ethernet frame. Because of this, no special requirements are needed for the master, therefore the standard infrastructure can be used. The EtherCAT frame is registered as an IEEE Ethertype: 88A4h. This defines that the IP stack is not required and the frame overhead can be optimized.

The EtherCAT frame and its integration in the Ethernet frame are shown in Figure 3-2. A standard Ethernet frame can have up to maximum 1498 bytes, but at least 48 bytes of data. This means that if only 2 bytes have to be sent, an Ethernet frame will fill the other 46 bytes with empty bytes in order to respect the standard. An EtherCAT frame uses the same header as an Ethernet one, but it fills the Ethernet data sector with as many datagrams as possible, until the maximum bytes are achieved. This way, the Ethernet standard will be satisfied and, at the same time, the data space will be used more efficiently, by allowing a single frame for multiple devices. This can improve the throughput by lowering the overhead under 10% [40, 42].

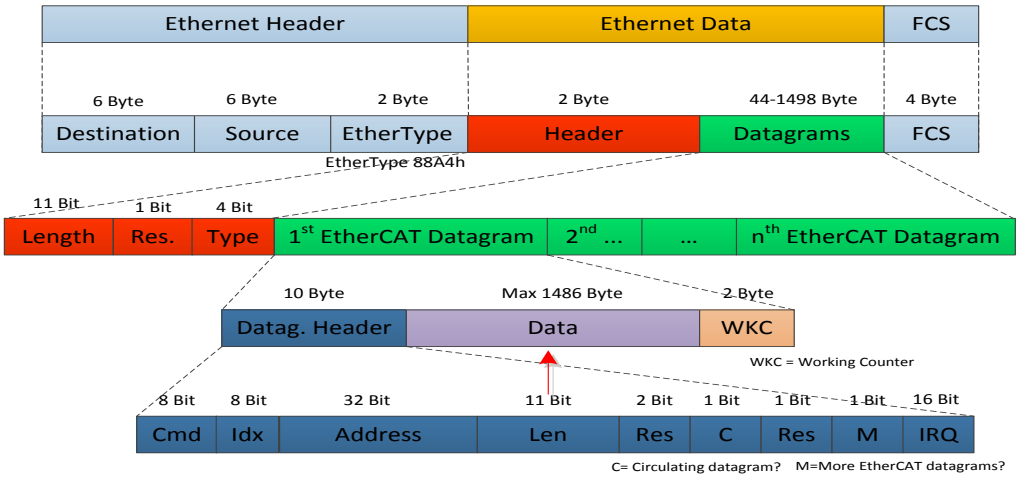

Figure 3-2 – EtherCAT datagram and its integration into an Ethernet frame [36]

An EtherCAT datagram consists of a data header of ten bytes which includes the Command on one byte, the Address of the EtherCAT slave, the Length of the data transported in that datagram, some reserved bits, a circulating datagram Counter and information if the data was split between more datagrams. After the header, the data place is reserved with space up to 1486 bytes and a 2 byte Working Counter (WKC) which is used for fault diagnostics.

3.3 EtherCAT Devices

An EtherCAT network consists of a master and one or more slaves. The master is responsible to initialize the communication and to send telegrams. The exchanged data is considered output if the data starts from the master or input if the data is sent by the slaves.

3.3.1 EtherCAT Master

The EtherCAT master can be implemented on any hardware configuration which has a good and stable power supply without management. This is among the only requirements, since, e.g. in case of a laptop computer, the power management might decrees the power supplied to the central processing unit and increase it for the graphical processing unit. This may affect the communication.

For the Master software, the mostly used solution is TwinCAT (TC) [41]. It natively runs under Windows Operating System and has a small enough footprint to be run on low power computers. It allows different software interfaces, from C++ to Matlab to PLC. It is recommended to run with Intel based network cards with their native drivers, but any card can work with the installation of intermediate drivers. The main advantage of TC is the fast integration of the control code in EtherCAT and the simplified network configuration.

3.3.2 EtherCAT Slaves

Different EtherCAT slaves have been implemented. Among the most used are the ET1100 ASIC ESC [43], and the ET1810/ET1815 FPGAs cores [44, 45]. While the FPGA implementation can be

run and used directly on the FPGA, when using the ET1100, a micro-controller is needed to handle the communication or only simple input/output pins can be used. When used with a micro-controller, the Process Data Interface (PDI) can be set up using either 20 Mhz SPI or 8/16bit synchronous or asynchronous parallel interface.

3.4 Slave addressing

An EtherCAT slave can be address in many ways. If Position addressing is used, the address of the datagram contains an offset which is equal to the negated value of the position of the slave addressed. As the datagram passes though each ESC, the address offset will be increased and the slave which reads zero is addressed. This is normally used only during initial hardware scanning and problems will appear if one of the slave devices is removed during operation, as its datagram will be given to the next slave.

Another way to address the slave is based on the fixed address which is normally given after the hardware scan. This is a safer way of addressing as it is independent form the position of the slave.

Logical addressing can be regarded as a 4Gbytes sized Ethernet frame (fragmented), in which each slave writes and reads from its partition.

3.5 Fault Diagnostic

3.5.1 EtherCAT commands and Working Counter

The EtherCAT master can issue different commands for the slaves to perform when the datagram passes them. These commands can be Read (R), Write (W), Read and Write (RW) and Read Multiple Writes (RMW) which are addressed directly to individual slaves or broadcasted.

In order to verify the proper operation of the communication, before sending a datagram, the master calculates an expected WKC. This will count the number of devices that were successfully addressed by the datagram. The working counter will increase if at least one bit of the access was successfully read/written. The master will compare the expected WKC with the one of the returning datagram in order to evaluate the validity of the communication. Table 3-2 summarizes the operating principles of the working counter. As mentioned earlier, the read/write operations are described as viewed from the master. Further description of all the possible commands can be found in [43].

Table 3-2: Working Counter Operation [43]

Command	Data Type	Increment
Read command	No success	no change
	Successful read	+1
Write command	No success	no change
	Successful write	+1
Read/Write command	No success	no change
	Successful read	+1
	Successful write	+2
	Successful read and write	+3

3.5.2 Frame processing and Circulating Counter

Although the Ethernet frame used for datagram transportations will use MAC and IP addresses, as defined in the standard, they cannot be used for addressing, because the ESC will process the frames

with any MAC or IP addresses. As the MAC is not used in the communication, except to help the master distinguish between the outgoing and incoming frames, an unmanaged switch should not be used in the EtherCAT network since this will normally destroy the frames with invalid MAC addresses.

The ESC can have from one to four ports defined. If a connection is detected on a port, that port will be considered opened by the ESC, unless manually closed by the configuration.

The main port of each ESC is considered port 0 and it should always be used. Depending on how many other ports are opened, the ESC will forward the data from one to the next. The frames are read only when they come from port zero. If a port is closed, the data is automatically forwarded to the next opened port. Table 3-3 summarizes the frame processing order, while Figure 3-3 shows a simplified graphical version of the frame processing.

If a datagram passes through a closed port 0, the circulating counter from Figure 3-2 will be incremented. When a datagram with a circulating counter different than zero passes through a Processing Unit, the data gram is destroyed. This is to ensure that if a physical connection is broken, the datagram will not keep circulating through the separated slaves and cause damage. When the ESC watchdog is not reset by a datagram, the slave devices can go into a safe state in order to protect the system. This is graphically explained in Figure 3-4.

Table 3-3: Frame processing order [43]

Number of Ports	Frame processing order
1	0→EtherCAT Processing Unit→0
2	0→EtherCAT Processing Unit→1 / 1→0
3	0→EtherCAT Processing Unit→1 / 1→2 / 2→0 (log. ports 0,1, and 2) or
	0→EtherCAT Processing Unit→3 / 3→1 / 1→0 (log. ports 0,1, and 3)
4	0→EtherCAT Processing Unit→3 / 3→1 / 1→2 / 2→0

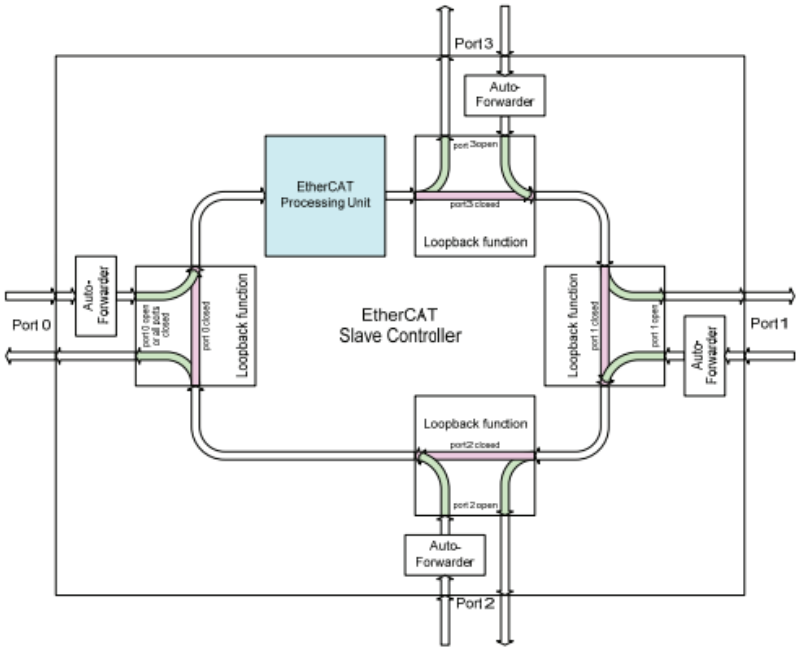

Figure 3-3 – Frame processing [43]

Figure 3-4 – Circulating datagram [43]

3.6 Clock Synchronization and Distributed Clock

Because many control systems require accurate timing, good clock synchronization with low jitter is required. This is implemented in the EtherCAT slaves' hardware in order to ensure low jitter, similar to the IEEE 1588 [46].

The Distributed Clock (DC) unit serves different purposes in the communication process and among the most relevant for this project is the clock synchronization between slaves and synchronous output signals generation [43].

The DC unit enables all the devices in the EtherCAT network to share the same time and be synchronized to each other, which translates into synchronization of the controlled process implemented with EtherCAT. In order to allow the master implementation on off-the-shelf hardware which does not contain a DC unit, the first slave with DC capabilities is chosen as a Master System Clock. This unit is chosen as a reference clock for DC synchronization in the entire network. The Master DC then can calculate the propagation delays in the network, clock drifts and offset needed in the synchronization process [40]. The propagation delay is measured as the delay between the leaving and returning EtherCAT frame in each slave unit and then stamped in the frame in order for the EtherCAT master to calculate the differences between each slave and to compensate for them [40]. This process is illustrated in Figure 3-5. After the clocks are synchronized down to µs, the master will periodically check to ensure that drifts between the clocks are compensated [43].

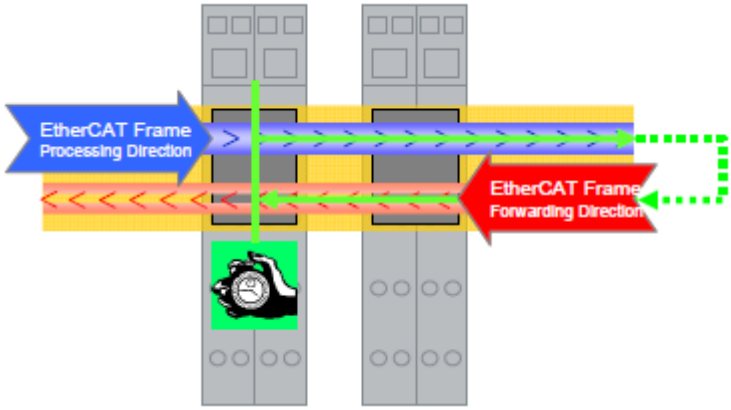

Figure 3-5 – Propagation delay calculation [43]

If the EtherCAT communication is implemented on an ASIC based ESC connected to a microcontroller, two synchronization signals (SYNC0 and SYNC1) can be mapped as interrupt signals to ensure proper synchronization of the clocks. There are different operation modes for the synchronization signals that are described in [43]. The simplest and most suited mode is the SYNC0 synchronization of the readings. The ESCs can be configured to generate the interrupt signal only after all the slaves, which need clock synchronization, have had their data written in the ESC memory and they can read it. This way, the signal will synchronize all the slaves and, at the same time, will inform them that new data is present in the ESC memory for reading. By properly managing the interrupt signal, all slaves' microcontrollers can have their clocks in sync. Figure 3-6 graphically presents the delays in the frame reading and the synchronized interrupt event [43].

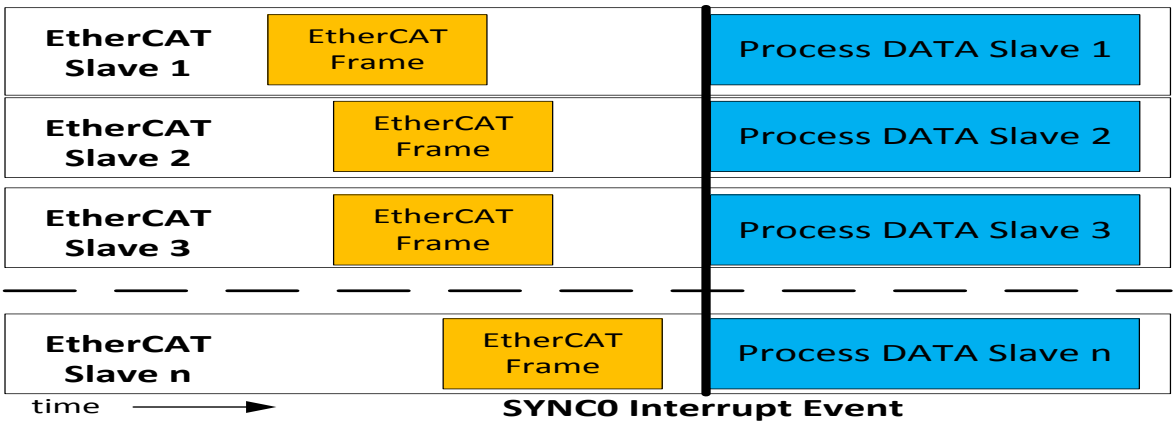

Figure 3-6 – Process synchronization with SYNC0 Interrupt

3.6.1 Communication delay

The communication has to have an update time as fast as possible, but at the same time to be able to transfer the data to all the SM during it. In order to find the most suitable update time, the delay times need to be calculated.

The application overhead on the SPI communication is approximately 50%, and, although SPI is a full-duplex communication, the implementation will use it as a half-duplex. On the 10Mhz SPI connection between the DSP and the ESC the total delay for 14 byte payload will be approximately 22,4 µs. It has to be taken into consideration that although this delay is encountered in every SM, it should be considered only once as all the SM will transfer the data at the same time.

Assuming an 8 SM three-phase MMC with a EtherCAT 100Mbps full-duplex communication with all the SM daisy chained and with the data from Table 3-1, equation (3.1) becomes:

$$Payload = 3 \cdot \left(\frac{6}{2} \cdot 8 + 6 + 2 \cdot 2 \right) = 102\,bytes \tag{3.2}$$

Based on the above payload and a 500 *ns* forwarding delay per ESC, the total delay expected for this configuration, with 10% communication overhead, can be calculated as:

$$delay_{8\,SM} = \frac{payload}{100Mbps} \cdot 1{,}1 + delay_{SPI} + 8 \cdot 500\mu s = \frac{102\,bytes \cdot 8}{100Mbps} \cdot 1{,}1 + 12\mu s \cdot 22.4\mu s = 43.376\mu s \tag{3.3}$$

This value should only be considered for this type of connection. Since a faster SPI communication or a different wiring of the EtherCAT could improve the delay times considerably. For a three-phase converter the delay can be calculated as:

$$delay = \frac{1}{m_{ETC}} \cdot \left(\frac{14\,bytes \cdot 8 \cdot 3 \cdot 2 \cdot n}{EtherCAT\_Band} \cdot 1{,}1 + 2 \cdot n \cdot delay_{ESC} \right) + \frac{14\,bytes \cdot 8}{SPI\_Speed} \cdot 50\% \tag{3.4}$$

where:

m_{ETC} - the number of EtherCAT connections between master and converter (assuming equal distribution of SM per connection);

$EtherCAT\_Band$ - bandwidth of the EtherCAT communication in bps;

$delay_{ESC}$ - delay encountered in the forwarder of each ESC;

SPI_Speed - the frequency of the SPI communication in Hz.

By rearranging equation (3.4), the maximum number of modules which can be addressed in a communication cycle is found as:

$$n = \frac{\left(cycle\_time - \frac{14\,bytes \cdot 8}{SPI\_Speed} \cdot 50\%\right) \cdot m_{ETC} \cdot EtherCAT\_Band}{14\,bytes \cdot 8 \cdot 3 \cdot 2 \cdot 1{,}1 + 2 \cdot delay_{ESC} \cdot EtherCAT\_Band} \tag{3.5}$$

Assuming a converter with a SM switching frequency of 1kHz and one EtherCAT connection per arm ($m_{ETC} = 6$), and an update time of 2kHz (500µs) in order to ensure good response time, the maximum number of SM per leg which can be addressed is obtained as:

$$n = \frac{\left(0.0005 - \frac{14\,bytes \cdot 8}{10^7} \cdot 50\%\right) \cdot 6 \cdot 10^8}{14\,bytes \cdot 8 \cdot 3 \cdot 2 \cdot 1{,}1 + 2 \cdot \left(500 \cdot 10^{-9}\right) \cdot 10^8} = 353.48 \cong 353 \tag{3.6}$$

3.7 SyncManager

The SyncManager is responsible of data exchange between the EtherCAT datagrams and the microcontroller through the SPI communication. There can be up to 16 simultaneous SyncManager channels and two types of SyncManagers: Mailbox type and Buffer type. The mailbox type is generally used for large files and handshake type connections. Since this is not useful for this project, no further details will be given. The buffer type consists of 3 buffer memory areas. This guarantees that the latest data is always available for both sides and that there is always a buffer available for writing. The buffer type is generally used for process data communication. It can be better explained by analysing Figure 3-7. In phase A, the EtherCAT locks memory area 1 by writing the first byte, and keeps it locked until the last byte is written. The microcontroller locks memory area 3 by reading the first byte through the PDI. This should contain the latest available data. In phase B, the EtherCAT ESC finishes the writing procedure and frees up buffer number 1. If another telegram comes in the

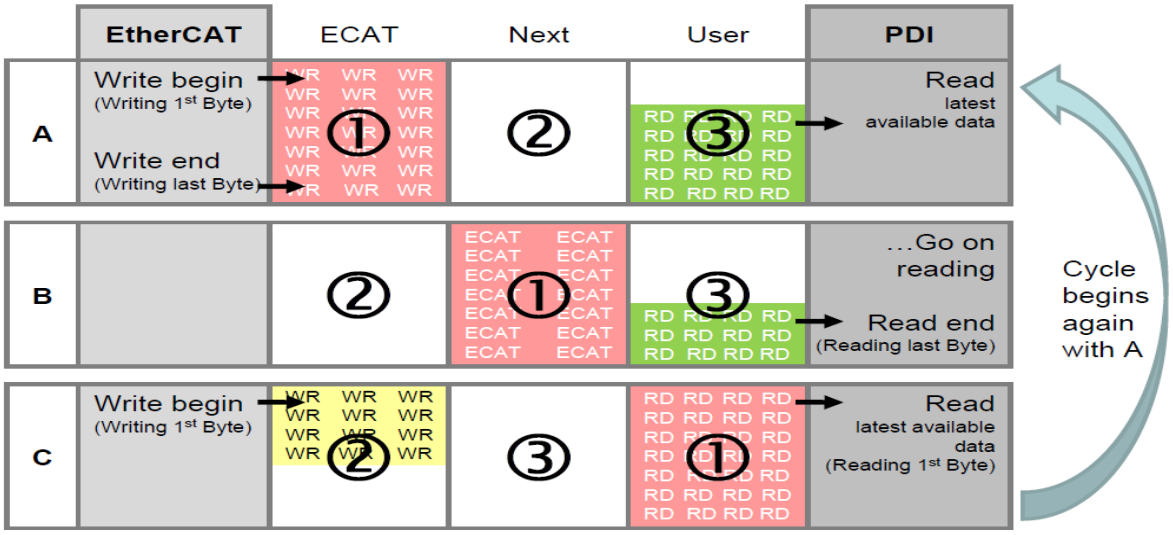

Figure 3-7 – Buffered Type SyncManager Writing [43]

meantime and data needs to be written, it will lock memory area number 2 with the above mentioned procedure. When the microcontroller reads the last byte of buffer 3, it frees it, and then it starts reading buffer 1, which now contains the latest data. The process is then repeated cyclical. There can be cases when either the EtherCAT or the PDI microcontroller will write/read data at a much higher frequency than the other. In this case, the faster one may overwrite one of the buffers in order to ensure latest data [43].

3.8 State Machine

The EtherCAT application layer has implemented 5 possible states for the communication which provide different advantages in control applications. The EtherCAT State Machine (ESM) coordinates the master and slave applications during the initialization and operation. The state change request is initialized by the master and acknowledged by the slave application after the associated operation is executed. The main four states are: INIT, Pre-Operational (PREOP), Safe-Operational (SAFEOP), Operational (OP) and there is another optional state Bootstrap (BOOT). Each state consists of different services, and before a state is changed, all services for the requested state have to be executed and the one for the previous state stopped [43]. Figure 3-8 shows the different states and the possible transition steps from each state to another. Normally, a jump between each state is possible, except for from INIT to Operational. In this case, the state machine has to go through each step.

During the INIT state, no communication takes place on the application layer. When switching from the INIT to PREOP, the EtherCAT master will configure the register of the SyncManager channels for Mailbox communication, initialize the DC clock synchronization, request the PREOP state and wait for confirmation from the slave. During the PREOP state, there will be Mailbox communication in the layer application, but no process data communication takes place. When PREOP to SAFEOP transition is requested, the master configures the process data mapping and checks to ensure that the process data is implemented as it is declared. Furthermore, it configures the SyncManager for the process data communication, requests the SAFEOP state and waits for the confirmation or error code. In the SAFEOP state there will be mailbox communication on the application layer, as well as process data communication, but only inputs (as viewed by the master) are evaluated, while the outputs remain in a safe state. As the SAFEOP to OP state change is requested, the master sends valid outputs data and requests the operational state for which it expects confirmation. During the OP mode, both inputs and outputs are considered valid [43]. Description of all possible states codes and errors are presented in [43] and will not be described here as they are beyond the point of this project.

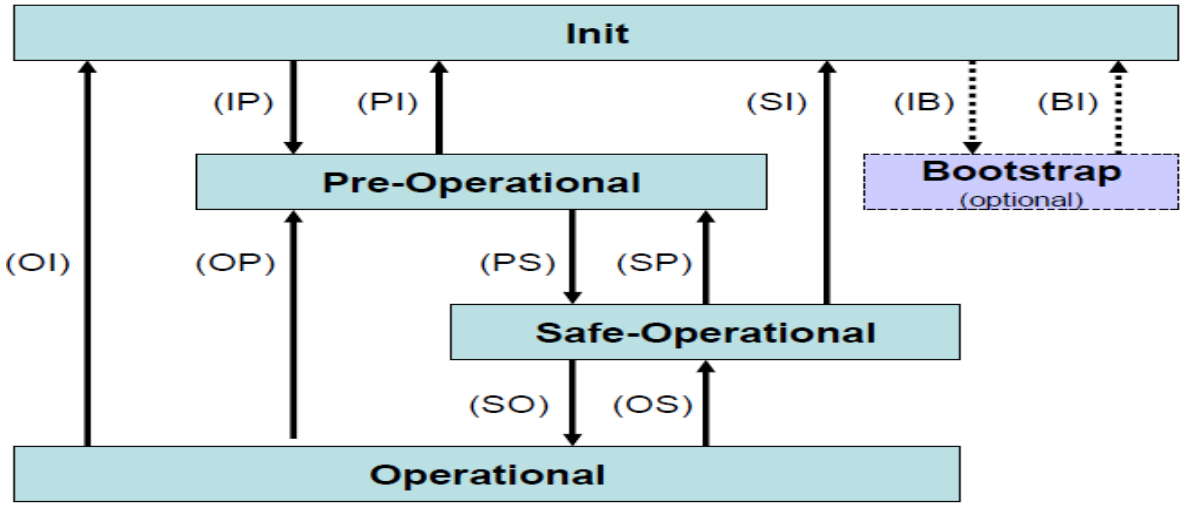

Figure 3-8 – EtherCAT state machine [43]

3.9 Communication redundancy

Communication redundancy is built into the communication protocol in order to support normal operation even when a fault occurs on a physical layer: broken cable, ESC failure on the communication line. Figure 3-9 shows the reconfiguration of the communication. In order to obtain redundancy in the communication, one extra physical network port can be used to make a physical ring in the communication. The same EtherCAT frame will be sent from both port A (blue) and B (orange). Under normal operation, the frame leaving port A will enter though port 0 of each slave, pass through the EtherCAT processing unit and leave through port 1 as shown in Figure 3-3. The slave closest to port A of the Master will be assigned as DC master. The telegram which leaves port B of the master, will enter each slave through port 1 and leaves through the open port 0 without passing through the processing unit. In case the wire will brake, as shown in the lower part of Figure 3-9, the frame which leaves port A, will be redirected back by a closed port 1 and will return through the same port to the master. The frame which leaves on port B, will bypass all the EtherCAT processing units until it will find the closed port 0 of the slave where the line broke. Then it will be forwarded back, and as it returns, it will pass through each of the processing units of the slaves and return to the master though port B. The master will then analyse both working counters of the 2 copies of the frame and will validate the communication unless some slaves got isolated. The newly formed network will have to assign its new master DC for that part of the network [43].

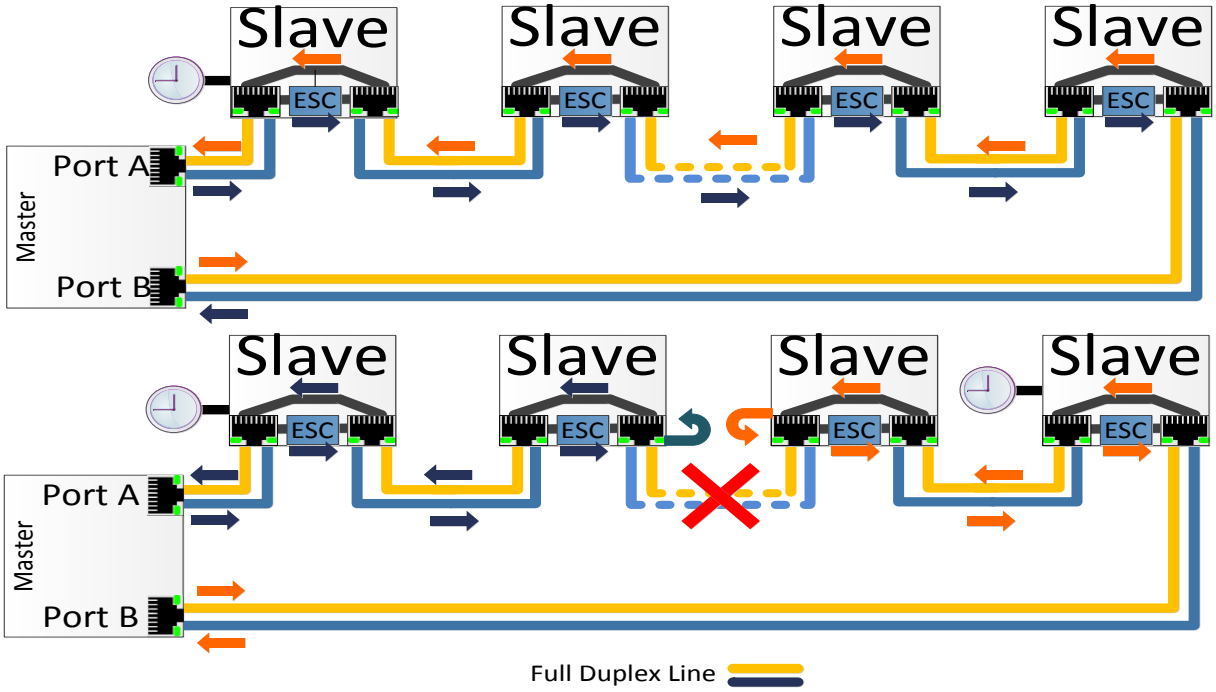

Figure 3-9 – Communication reconfiguration [36]

3.10 Slave description file

Since the standard is open sourced and the EtherCAT masters and slaves can be implemented on different hardware with different purposes, processes and limitations, a simple common mode for interconnection was established for interoperability between devices from different manufacturers. For the interconnection of the EtherCAT slaves with the masters, a simple approach was chosen, based on an XML file which defines the slave. This is also useful as slaves can have different ESCs, PDIs, SyncManagers and process data communication.

The XML file, according to [43], has to contain: the Name and ID of the EtherCAT member, the device type and ESC used, the PDI type used in the connection of the ESC, and especially where the process data is stored in the memory of the ESC. In case the ESC is ASIC based, the master also has to write the configuration into the EEPROM memory of the slave. The rest of the data present in the configuration file is not relevant to this project, and can be consulted in [44].

During the state change of the slaves, the application layer on the slave device microcontroller checks its settings against the settings written by the EtherCAT master in the EEPROM to ensure proper operation, and in case of mismatch, informs the master of the error and goes into a safe state.

3.11 Summary

In this chapter, the Ethernet based, EtherCAT communication was briefly presented with its main characteristics and advantages. It is based on standard Ethernet frames which allows the master implementation with off-the-shelf components and due to its integration in the frame, it can remove much of the overhead present in a standard Ethernet frame, which translates into better data throughput. Hardware based slave implementation allows for low propagation delays and accurate clock synchronization with low jitter.

The communication allows for a large number of SM to be accommodated in short update times. Their number is dependent on the switching frequency desired and the number of SMs which can be connected to one EtherCAT port of the Master.

Thanks to the working counter, the master can easily detect a communication problem and pinpoint to the exact faulty ESC which is highly needed in a control application where such a fault might be catastrophic. At the same time, the ESC can inform, on the application layer, the slave controller about the fault.

The automatic reconfiguration and simple redundancy implementation in case of physical link fault allow the user to be focus on other important aspects.

The circulating counter is another important fault protection, which ensures that if one or more slaves get isolated, they will fall into a safe state after the circulating frames are destroyed and the watchdogs do not get reset.

The machine state allows for different steps to be taken at the initialization of the communication much easier, since they are already implemented in the application layer, making the integration of specific control simpler.

The three buffer mode of the SyncManager allows for the latest data to be available to the slaves and master in case faster update times are used in one of them.

EtherCAT proves to be a suitable solution for a MMC communication. Due to its precise clock synchronization and low jitter, it should allow for a sufficiently fast communication in order for the converter to have fast reaction times. The fault tolerance configuration and different protection mechanisms for fault detection ensure that the SM will go into a safe state in case the communication gets interrupted. The different machine states allow easier integration of the control strategy and synchronization between modules without too much effort.

The description file ensures that all the variables used in the SM microcontroller are recognized by the EtherCAT master and mapped accordingly.

4 Start-up and Fault-tolerant Operation

After the selection of control and the related balancing and start-up scheme, a simulation model was implemented in PSCAD/EMTDC simulation tool. Since no requirements were set, the simulation model parameters were chosen in order to have a simple model, but at the same time to be able to show all the characteristics of the MMC and to be simulated in the laboratory. The MMC model would be a five level single phase converter with 400V DC-link and 1.5kVA rating. This will allow to show the start-up procedure and the fault tolerant operation, which afterward can be tested on a laboratory prototype. The converter will be designed with one redundant sub-module per arm. The design parameters are highlighted in Table 4-1.

Table 4-1: Converter Design Parameters

Number of Sub-module per Arm	4
DC-link Voltage	400 V
Converter Output Power	1,5 kW
Arm inductor	1.6mH
Switching frequency per SM	810 Hz

4.1 Component Selection for Simulation

The detailed explanation behind the converter components selection was presented in sub-chapter 2.3 and here only the main equations will be reviewed.

In order to be able to calculate the capacitance, the output voltage and the power factor are needed. The power factor can be assumed to be 0.9, a traditional approach, as in any AC system there will always be some inductances, and the modulation frequency chosen will be 810, which is an asynchronous frequency. Assuming a modulation index of one, the peak output voltage will be 200V.

4.1.1 Sub-module capacitors

Based on the above assumptions and Table 4-1, the parameters necessary in the capacitance calculations are obtained as:

$$k = \frac{2 \cdot v_m}{V_{dc}} = \frac{2 \cdot 200}{400} \cdot = 1 \tag{4.1}$$

$$\omega_N = 2\pi f = 314.16 rad / s \tag{4.2}$$

Inserting all the values into equation (2.16) and assuming a voltage ripple of $\varepsilon = 0.1$, the necessary energy per capacitor is:

$$\Delta W_{SM}(k) = 2 \cdot \frac{S}{k \cdot \omega_N \cdot n} \cdot \left(1 - \left(\frac{k \cdot cos\varphi}{2}\right)^2\right)^{\frac{3}{2}} == 2 \cdot \frac{1500VA}{1 \cdot 314.16 \cdot 4} \cdot \left(1 - \left(\frac{1 \cdot 0.9}{2}\right)^2\right)^{\frac{3}{2}} = 1.7J \tag{4.3}$$

Consulting [17], the energy per SM can also be calculated as:

$$\Delta W_{SM}(k) = \frac{S}{n} \cdot \frac{40kJ}{10MVA} = \frac{1500VA}{8} \cdot \frac{40kJ}{10MVA} = 7500J \tag{4.4}$$

The second approach is more conservative, and at the same time it allows the converter to store more energy, which in terms will translate to a better handling of faults which might appear.

From equations (4.4) and (2.18) the minimum capacitance for the SM can be found:

$$C_{SM} = \frac{\Delta W_{SM}}{2 \cdot \varepsilon \cdot V^2_{SM,nom}} = \frac{7500J}{2 \cdot 0.1 \cdot (100V)^2} = 3.75mF \tag{4.5}$$

In order to show that the start-up procedure is not influence by the SM capacitance and to allow for the same converter to be implemented in the laboratory, the SM capacitance assumed will be 4.5mF.

4.1.2 Arm inductors

The arm inductors were already selected in the design parameters based on the available inductors for the experimental setup. A 1.6mH arm inductor will limit the fault current rise rate in the leg as:

$$\alpha = \frac{V_{DC}}{2 \cdot L} = \frac{400V}{2 \cdot 1.6mH} = 125kA/s = 125A/ms \tag{4.6}$$

This will be a more than acceptable value for the available protective devices and switching semiconductors available on the market.

4.2 Model description

The 400V DC-link is represented by a ±200 V voltage source with the ground as a middle point reference. The leg of the converter will consist of eight SM with one capacitor and two switching semiconductors with antiparallel diodes. Since PSCAD/EMTDC does not offer a discrete model for Mosfets and all the semiconductor devices are based on an IGBT model, the Mosfet chosen for the laboratory setup will be implemented on an IGBT model. Since the IGBT conduction losses are calculated based on the voltage drop, while the Mosfet is proportional to the drain resistance, the equivalent voltage drop an nominal load (16A) will be assumed.

Table 4-2: Characteristics of simulated switch

On Resistance	110mΩ
Forward Voltage Drop	1.76 V
Diode Resistance	2mΩ
Diode forward voltage drop	1.7V

As mentioned in sub-chapter 2.5.3, phase-shifted triangular carrier PWM will be implemented. The phase shift θ between four SM was obtained from:

$$\theta = \frac{360°}{n} = 90° \tag{4.7}$$

The balancing controller described in sub-chapter 2.6.2 was implemented in the model as a central control, while the averaging part was separated for each arm and the final voltage command for each SM.

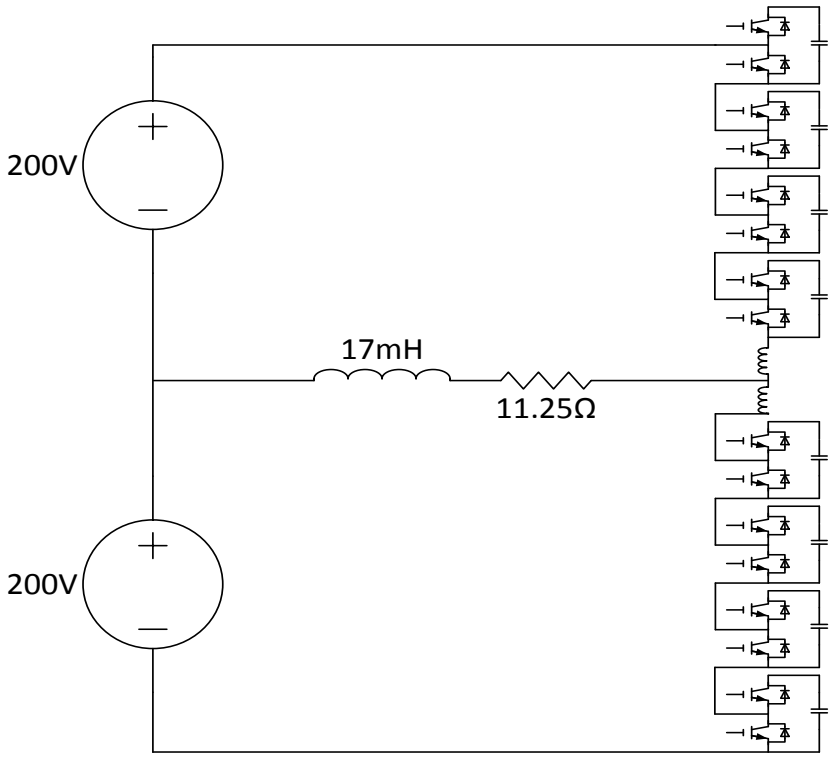

Figure 4-1 – Simulated converter

The converter model is presented in Figure 4-1. First, in order to ensure proper operation, the balancing controller is simulated, including the delays which might appear from the communication between the master and the slaves. In order to accommodate for the communication and errors, a delay of 100µs was introduced to any variable which is exchanged by the master and slave control.

The master control was developed in C programming language and linked to the simulation model using Fortran. The entire code is presented in Appendix C. This was done in order to have a model as close as possible to the laboratory implementation.

The two PIs presented in Figure 2-12 were tuned using the simplex method[47]. Two sets of gains were selected, one for start-up and one for normal operation. Since at the start-up of the converter the most important aspect is the current through the semiconductor devices and the capacitors voltages aren't bounded by the ±10% requirement, the controller was tuned to suppress the circulating currents. After the average of the capacitors arms currents are around their nominal value (100V) and before connecting the converter to the load, the control switches to the second set of gains, which are tuned to minimize the ripple in the capacitors voltages. This will ensure proper operation during the converter start-up and operation. The values for the controllers and their operation point are shown in Table 4-3.

Table 4-3: Chosen controller gains

Converter State	Abbreviation	Description	Value
Start-up	Kp1	Proportional gain of voltage loop control	6,7676 A/V
	Ki1	Integral gain of voltage loop control	14,9714 A/(V s)
	Kp2	Proportional gain of current loop control	11,6418 V/A
	Ki2	Integral gain of current loop control	12,9481 V/(A s)
Operation	Kp1	Proportional gain of voltage loop control	41,8167 A/V
	Ki1	Integral gain of voltage loop control	78,528 A/(V S)
	Kp2	Proportional gain of current loop control	0,03025 V/A
	Ki2	Integral gain of current loop control	59,651 V/(A s)
All	Kp3	Proportional gain of balancing control	2

At first, the converter balancing controller is simulated in order to ensure that it runs as desired. By looking at Figure 4-2 the proper operation can be noticed. The upper and lower capacitors voltages are shown in separate windows, together with their set points. The controller shows good operation. During the simulation the desired modulation index was changed from 1 to 0.6 in order to observe the dynamic behaviour of the controller.

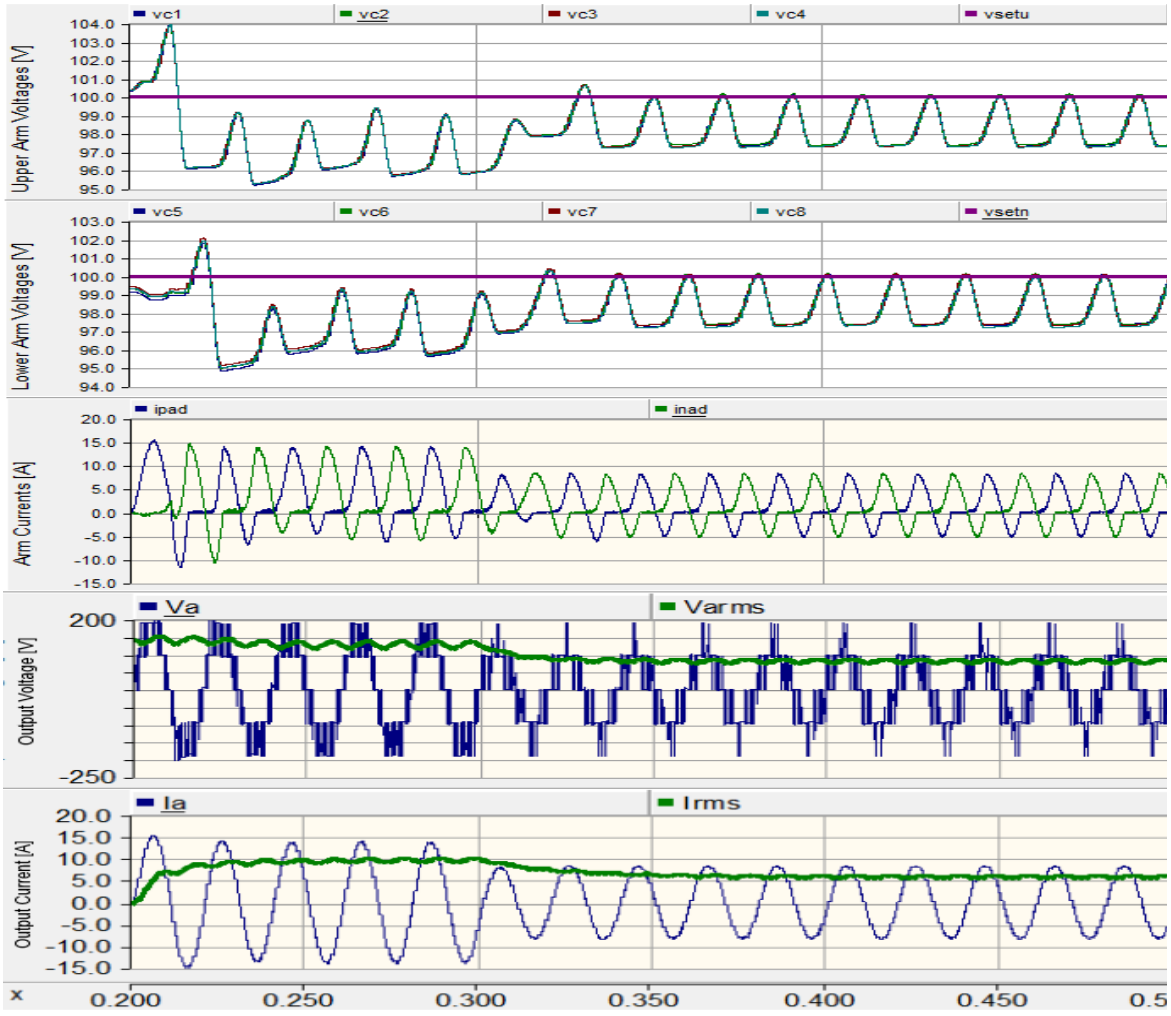

Figure 4-2 – Converter response to modulation index change

4.3 Converter Start-up

The start-up procedure can be split into 2 stages. In the first stage, with the DC-link at nominal voltage, all the capacitors are series connected to the DC-link. The equivalent capacitance will be equal to:

$$C_{eq} = \frac{C_{SM}}{2 \cdot n} = \frac{4500mF}{8} = 562.5mF \tag{4.8}$$

Considering the circuit is not ideal and that the arm inductances will limit the current rise-rate, the currents through the arm will be smaller than the normal operation currents. The first stage is shown in Figure 4-3. The first two windows of the graph show the voltages through the upper, respectively lower arm SM capacitors. The third window shows the arm currents. The first stage ends when the SM capacitors voltages equal to half their nominal voltage, in this case 50V. At this point the Master controller will keep all the SM inserted until the arm currents become zero and prepare for the next stage.

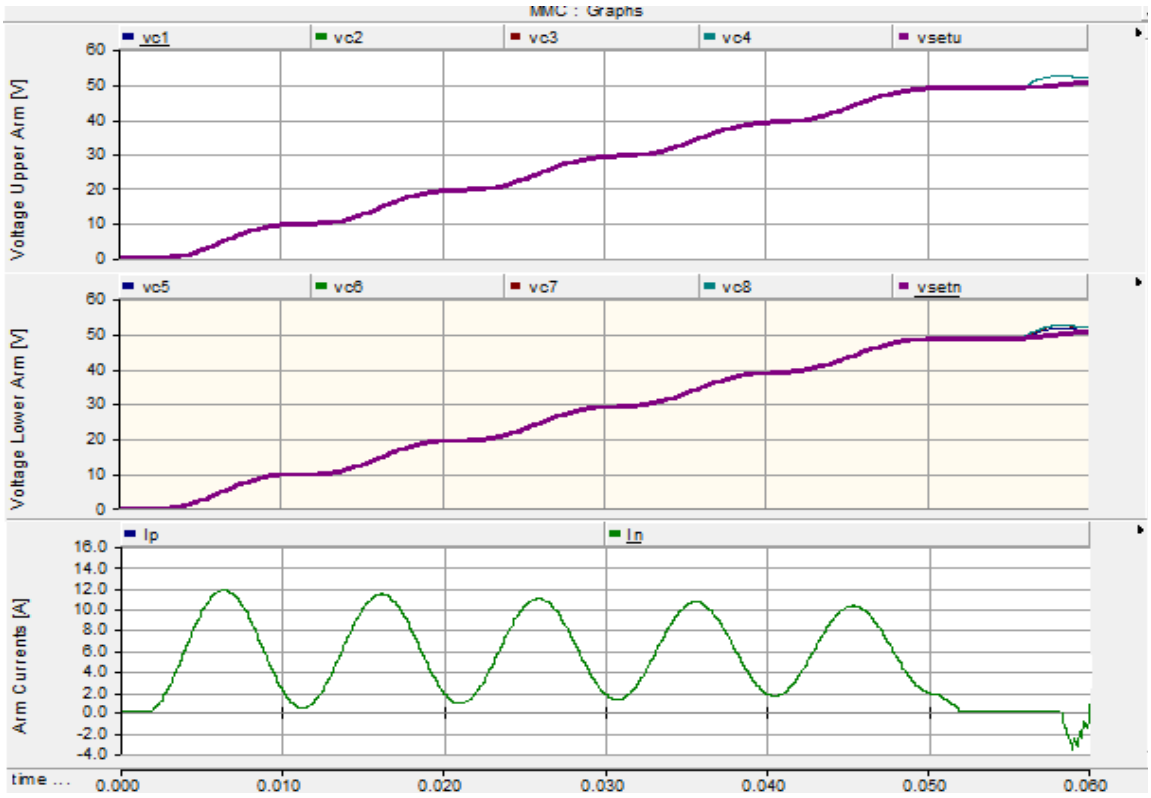

Figure 4-3 – Start-up stage 1

In the second stage of the start-up, the master will use the balancing controller proposed in sub-chapter 2.6.2 to equally charge the SM to their nominal voltage.

At this point the focus will be the circulating current, so the balancing controller is purposely tuned for this. In order to limit the circulating current, the reference SM voltage is varied linearly from 0.5 $V_{cap,nom}$ to $V_{cap,nom}$ with a ramp which guarantees low circulating current. This is shown in Figure 4-4. In the upper two windows the upper arm and lower arm capacitors following their reference voltage are sown. In the lowest window, the currents through the arms are represented. The second stage ends when the capacitors are charged to their nominal voltages, in this case 100V.

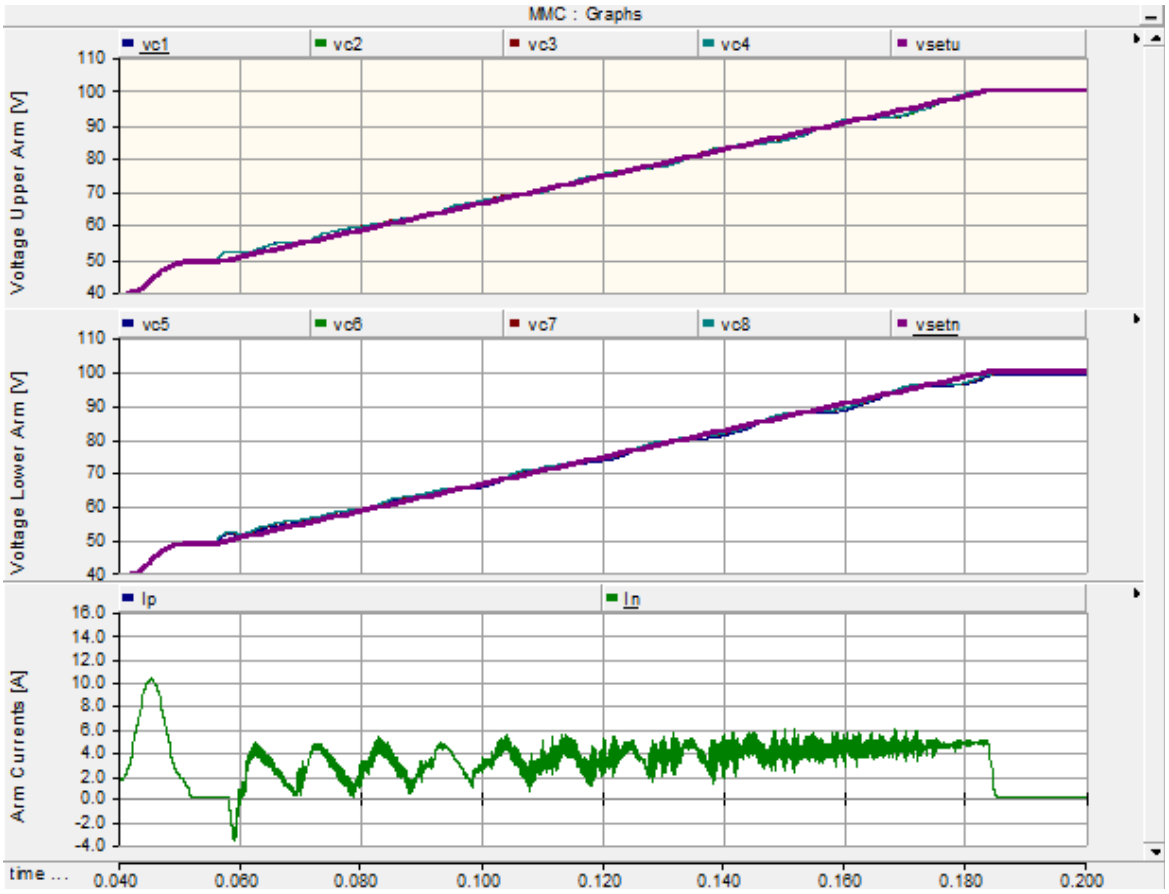

Figure 4-4 – Start-up stage 2

At this point the converter changes the gains of the balancing controller for normal operation and the converter can be connected to the AC load.

4.4 Fault reconfiguration of the converter

The SM failure may damage the semiconductor devices especially when the number of SM in the arm is low, this is because the other SM capacitors need to compensate for the missing voltage. In case of four SM per arm, if one fails, the other three need to accept a 33% increase in capacitance. Sudden increase in voltage will create a rising current in the arm which might damage the switching devices. In order to protect the SM from the inrush current which will appear from the sudden increase in energy distribution in the arm and to eliminate the involvement of the Master control which might react slowly due to delay in communication, each SM will have a protection mechanism included. A non-concomitant SM failure in each arm was simulated in order to show the good operation of the balancing control and the specific MMC tolerance to SM failure. When a SM fails in the arm, an unbalance between the arms energy is created and a fast-rising current will appear in order to balance them. The impact of this is inverse proportional to the number of SM in the arm. In order to protect themselves from this current, the SM are configured to insert their capacitors when the current in the arm rises above a preset threshold, in this case 18A. This will limit the current and at the same time, increase the voltage across the capacitors, helping the SM to rise to their new reference. The results of the simulation are shown in Figure 4-5.

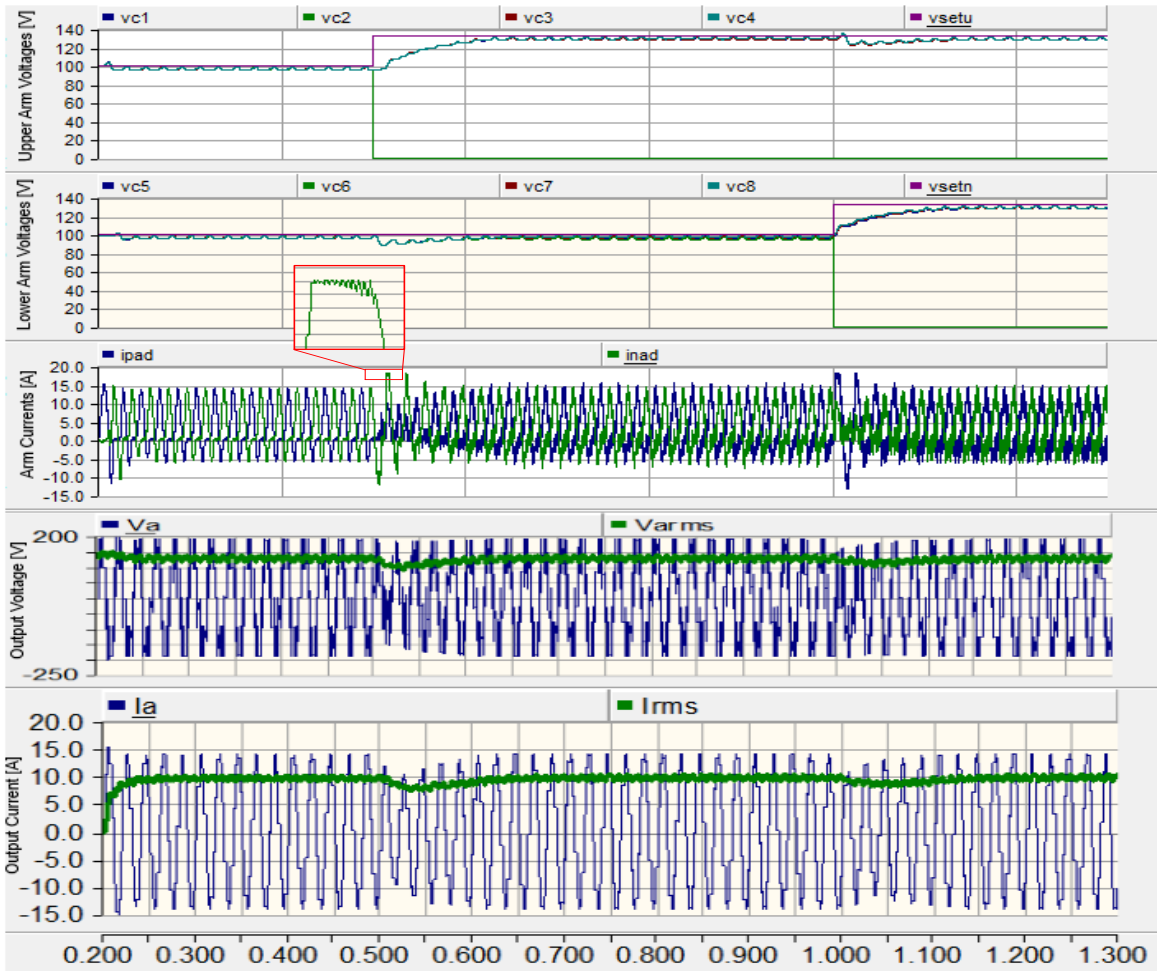

Figure 4-5 – SM failure in each arm

When this occurs, the distribution of the switching in the arm needs to be reconfigured, and the triangular carriers of the SM need to be rearranged to equally cover the entire 2π period. Since the SMs cannot detect if and which one of them has failed, the Master, after it detected the failed SM, will reissue a new phase shift angle to each of the remaining SMs. This will also occur with a delay due to the communication.

At the instance of the failure, the current will increase and the SM will try to limit them. A disturbance will appear from this and from the misdistribution of the carriers. This can also be seen on the outputs of the converter.

4.5 Summary

A model was designed in order to simulate the protections and fault reconfiguration of the MMC. The entire control and balancing algorithm was implemented in C code in order to represent as close as possible the laboratory prototype which will be built.

A novel start-up procedure was introduced and showed good behaviour during the simulation, with arm currents under the nominal ones.

The SM fault reconfiguration was simulated and measures which need to be taken in order in case of a low number of SMs in the arm were investigated.

5 Experimental Results and Redundancy Implementation

In order to validate the simulation from chapter 4 and to show the implementation and efficiency of the EtherCAT communication, a laboratory prototype was designed and built. The SM design and validation is presented in Appendix B.

Due to the unexpected delays encountered in the implementation of the communication on the SM controller, the time schedule got delayed and no experimental results of the converter have been obtained by the time the report had to be delivered. Full experimental result of the converter operations will be later presented in a supplement.

5.1 Experimental Setup

The experimental setup consists of 8 SM single-phased MMC with a total rating of 1.5kVA. The 400V DC-link is provided by a Magna-Power laboratory voltage source and as a load a simple RL circuit is used. The setup will validate the simulations shown in the previous chapter. The master control is implemented on an IPC from Beckhoff. Each arm of the converter will have its own EtherCAT frame and in order to provide communication redundancy, it will have two connections to the master. Together with a daisy chained connection in the arm, this will allow for a fault in one of the cables or communication board without affecting the converter operation. One arm of the MMC prototype is shown in Figure 5-1.

The SM design and validation is presented in Appendix B.

Figure 5-1 – MMC laboratory prototype

5.2 Phase shifted PWM

In order to prove the concept of PSPWM, the modulation algorithm was first implemented on a single digital signal processor (DSP) using 4 PWM channels and is shown in Figure 5-2. Channel 1 (yellow), 2 (green), 3 (purple) and 4 (yellow) show the outputs of each PWM module. The sum of all the channels is shown with red. This is the final expected voltage output of the arm in which it will be implemented.

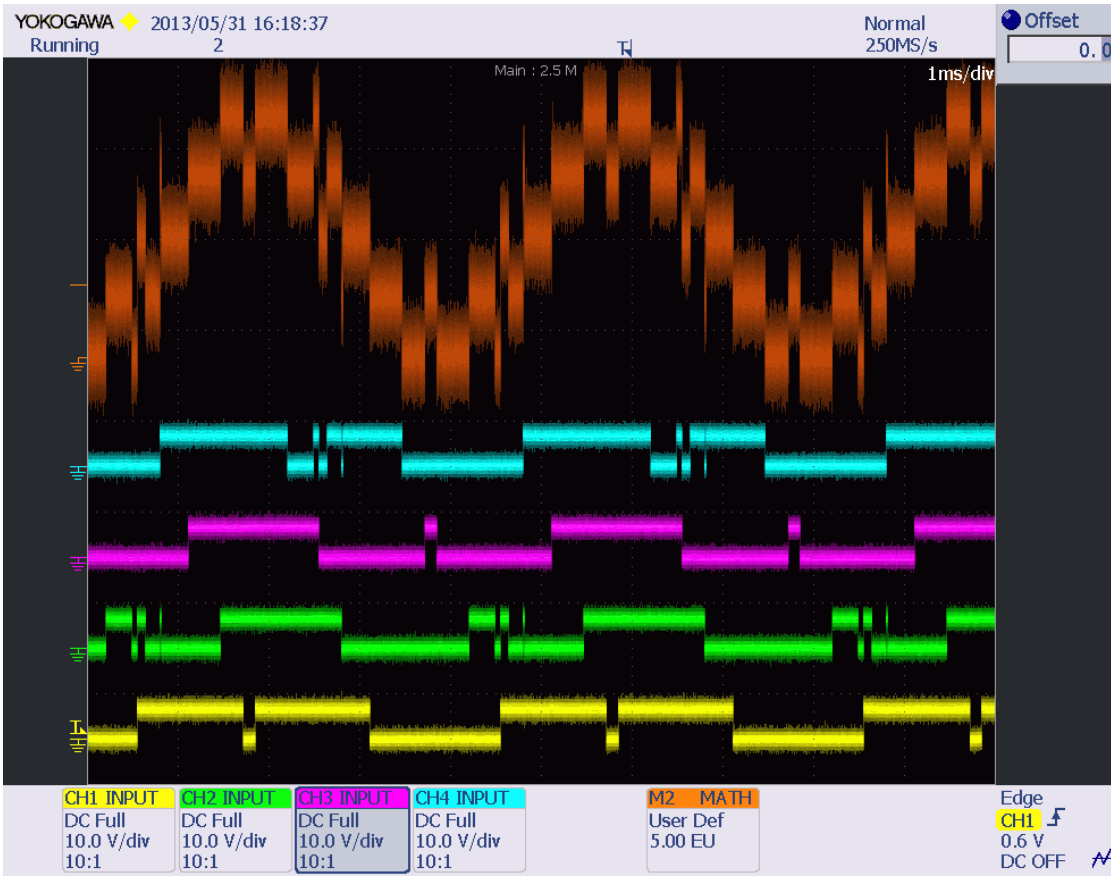

Figure 5-2 – Phase shifted modulation concept

6 Conclusions and Future Work

This chapter will present the conclusions regarding the hardware design of the MMC SM and EtherCAT communication.

During the project work, the communication boards and software was delivered late by the manufacturer and implementation was delayed. In order to understand fully the communication protocol training workshop had to be followed which delayed the implementation even more. Since a communication protocol is difficult to implement and is not part of the main field of energy technology, the sample stacks provided by Beckhoff had to be used. This created even more delays as the stacks were created for a PIC architecture which is different from the one used in the Texas Instruments DSP. As this was a new communication protocol, used for the first time in the department fully understanding the application layer behaviour and the modifications needed for the implementation took more time than initially expected, especially since the support from the manufacturer came late and poor in information. Because of this, the hardware validation of the simulations and the fault and redundancy were not tested. Furthermore the communication, although was operational, due to time limitation wasn't tested at the time of the submission.

6.1 Conclusions regarding the Hardware Implementation

The SM PCB was designed in Altium. The PCB was manufactured by an external company based on the files provided because it had four layers and the Energy Technology department can only produce two layers PCBs. The design featured galvanic insulation between the power and control circuits.

The protection was hardware implemented using a CPLD, providing both flexibility in terms of adjustments and fast reaction times. The 3.3V/5V tolerance makes the CPLD a good choice allowing for mixed voltage design.

The Triac – Relay protection implementation allows for a fast, safe and easy by-pass to the SM in case of failure, allowing the converter to continue operation even with faulty SMs.

The use of insulated half-bridge gate drivers with advanced features such as dead-time protection, undervoltage lock-out and bootstrap operation allowed for a reduction in size and cost, featuring the need of a single power supply for the entire half-bridge. The possibility of currents up to 4A sink/source makes the driving circuit suited for this application.

The hall-effect current measuring IC with filter and built in protection contribute even more to the reduced size, while at the same time allowing for accurate measuring and fast protection.

The SPI EtherCAT piggyback slave implementation using 52 pin header allow for an easier design and at the same time, the slave board can be swapped with other boards in order to allow other communications with the same SM design.

Optical feedback through 8 LEDs allows to easily diagnose and read the state of the communication and operation.

The reduced size is also a consequence of the simple DSP connection through a 32pin header while at the same time providing all the functionalities. It benefits from integrated FLASH and RAM memory with the CPU running at speeds up to 90Mhz. The code inside the DSP is designed to automatically copy itself from flash to RAM during power up in order to provide maximum operating speed and performance.

6.2 Conclusion regarding the start-up and fault tolerance

While the MMC has been a main subject of research lately, the distributed control was never reported from the communication, start-up or fault management point of view.

A novel start-up procedure suited for distributed control was presented and simulated. It proved good behaviour with circulating currents under the nominal operating currents, thus not stressing the converter. The use of the same control and capacitor balancing algorithm with just different gains allows for an easier implementation.

The SM failure and reconfiguration, although described in literature was never deeply investigated. While in a converter with a large number of SM a fault would not prove challenging, as their number is reduced, the energy become dangerous due to the high currents which appear when a SM is disabled.

Since the communication wasn't fully implemented the simulations will be validated only after the delivery of the report.

EtherCAT proves to be a good technology for MMC.

6.3 Future Work

Future work will include full implementation of the communication in the IPC and SM DSP with the definition of all the variable exchange needed.

The simulated start-up procedure and fault management will be tested on the laboratory setup in order to validate them.

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Appendix A – ICREPQ 2013 Paper

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Modular Multilevel Converter Control Strategy with Fault Tolerance

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Abstract. The Modular Multilevel Converter (MMC) technology has recently emerged in VSC-HVDC applications where it demonstrated higher efficiency and fault tolerance compared to the classical 2-level topology. Due to the ability of MMC to connect to HV levels, MMC can be also used in transformerless STATCOM and large wind turbines. In this paper, a control and communication strategy have been developed to accommodate tolerant module failure and capacitor voltage unbalance. A downscaled prototype converter has been built in order to validate and investigate the control strategy, and also test the proposed communication infrastructure based on Industrial Ethernet.

Keywords
MMC, HVDC, Converter, Transformerless wind turbine,

1. Introduction

Wind energy penetration is growing and the size of wind turbines also, especially for offshore applications where turbines in the range of 3-6 MW are now tested [1]. In order to comply with the more demanding grid codes in some countries with high wind power penetration (Denmark, Germany, Spain, UK, etc.) full-scale back-to-back (BTB) converters are more and more used in [2]. The MMC concept appears to be a promising technology recently introduced for high-voltage high power applications, due to the increased efficiency, redundancy provision and high quality voltage output with reduced dv/dt and output filter requirements [3-4]. Due to these advantages, the MMC is being now used by most of the VSC-HVDC manufacturers like ABB (HVDC-Light), Siemens (HVDC-Plus) and Alstom (HVDC-MaxSine) and also in STATCOM applications (Siemens SVC-Plus) and large wind turbines directly connected to MV levels [5].

2. Design and modeling

In the following, we consider an MMC converter applied to a 10 MW/20 kV transformerless wind turbine. The main data is shown in TABLE I.

TABLE I. INITIAL REQUIREMENTS

Description	Abbreviation	Value
DC-link voltage	V_{dc}	36 kV
Output AC RMS voltage	V_{L-L}	20 kV
Rated active power	P_N	10 MW
Power factor	$\cos\varphi$	±0.9
Number of sub-modules per arm	n	13
Sub-module nominal voltage	$V_{SM,nom}$	2.77 kV
Number of voltage levels	-	14

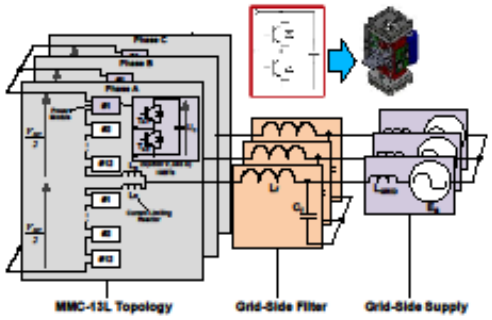


Figure 1: Three Phase MMC for TL Wind Turbine

One redundant sub-module was placed in each arm. This redundant module participates in the operation but in case of failure it can be bypassed and the converter operation can continue with acceptable quality output voltage. The remaining sub-modules are tolerant to the 8% increase of the voltage.

Considering the operation principle of the MMC, each capacitor has to be rated to the DC-link voltage level which is divided by the number of sub-modules in one arm, taking into account safety and redundancy margins. Another aspect that should be taken into account is the storage capability of the capacitor. This means that it has to be able to provide the rated power during transients in the DC link.

Arm inductors have to be selected based on the fault current rise-rate limitation criterion. The inductors are series connected, and this can reduce both internal and external fault currents therefore preventing the damage of the equipment under test [6].

A. CAPACITOR DIMENSIONING

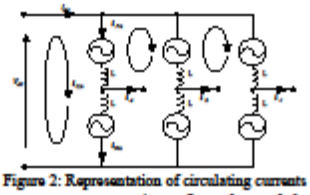


Figure 2: Representation of circulating currents

If the converter arm consists of n sub-modules, the energy change in one sub-module is given by [7]:

$$\Delta W_{source}(k) = \frac{2}{3} \cdot \frac{S}{k \cdot \omega_N \cdot n} \cdot \left(1 - \left(\frac{k \cdot \cos\varphi}{2}\right)^2\right)^{\frac{3}{2}} \quad (1)$$

where S is the apparent power of the converter, k is the voltage modulation index, ω_N is the output angular frequency, n is the number of sub-modules per arm and φ is the output angular frequency.

Assuming that a sub-module capacitor has a relative voltage ripple (±ε) around the nominal voltage for which the capacitor is designed, the energy of the capacitor can be expressed as:

$$W_C\left(V_{SM,nom}\right) = \frac{1}{2} \cdot C_{SM} \cdot V^2_{SM,nom} = \frac{1}{4 \cdot \varepsilon} \cdot \Delta W_{SM} \quad (2)$$

From equation (2), the sub-module capacitance (C_{SM}) at any desired voltage ripple ($0 < \varepsilon < 1$) can be derived as:

$$C_{SM} = \frac{\Delta W_{SM}}{2 \cdot \varepsilon \cdot V^2_{SM,nom}} \quad (3)$$

In case of the designed converter: $C_{SM} = 1\ mF$ (4)

B. ARM INDUCTOR DIMENSIONING

When selecting the arm inductors which limit the fault currents rise-rates, the most critical faults have to be considered; i.e. short circuit between the DC link terminals. In the first instant of fault, the sum of the voltage over the inserted capacitors is equal to the DC link voltage. The voltage drop over the arm inductors, according to Kirchhoff's voltage law, is [8]:

$$L\frac{di_{Pa}}{dt} + L\frac{di_{Na}}{dt} - V_{dc} = 0 \quad (5)$$

where L is the arm inductance, I_{Pa} and I_{Na} are the positive and negative arm currents and V_{dc} is the DC-link voltage. For short transients, both arm currents are assumed to be equal, so equation (5) can be rewritten as [8]:

$$\alpha = \frac{di_{Pa}}{dt} = \frac{di_{Na}}{dt} = \frac{V_{dc}}{2L} \quad (6)$$

Where α is the rise-rate of the fault current in kA/s. Furthermore, in equation (6), the arm inductor depending on the current rise rate can be expressed as:

$$L = \frac{V_{dc}}{2\square} = 0.27mH \quad (7)$$

1. Capacitor Balancing Method

During the operation, sub-module capacitors experience an unequal voltage share due to the operation principal. This affects the output voltage waveform by lowering the efficiency and quality indicators of the converter. There are several possibilities to achieve equal voltage over the arm capacitors without having external voltage sources. This is based on the sorting of the sub-modules by choosing wherever a module has to be in ON-state or OFF-state for each operating cycle [9]. The sorting criteria is based on:

- direction of the arm current;
- capacitor voltage.

The sorting algorithm will switch on the capacitors with the lowest voltages when the current flow is positive and vice versa for negative current. This method ensures that n capacitors in each phase leg are sharing the DC link voltage at all the time. In consequence a smaller arm inductance is required to suppress the circulating currents [10]. This results in balancing currents circulating between the legs as shown in Figure 2. Due to the symmetric structure of the converter, phase A will be used as an example. Figure 2 shows the positive and negative arm currents, i_{Pa} and i_{Na} respectively. The circulating current along the phase A loop i_{Ca} is used to represent the arm current. The load current of the phase A is noted with i_a.

$$L\frac{di_{Pa}}{dt} + L\frac{di_{Na}}{dt} - V_{dc} = 0 \quad (8)$$

Figure 3 presents the implementation of the sub-module

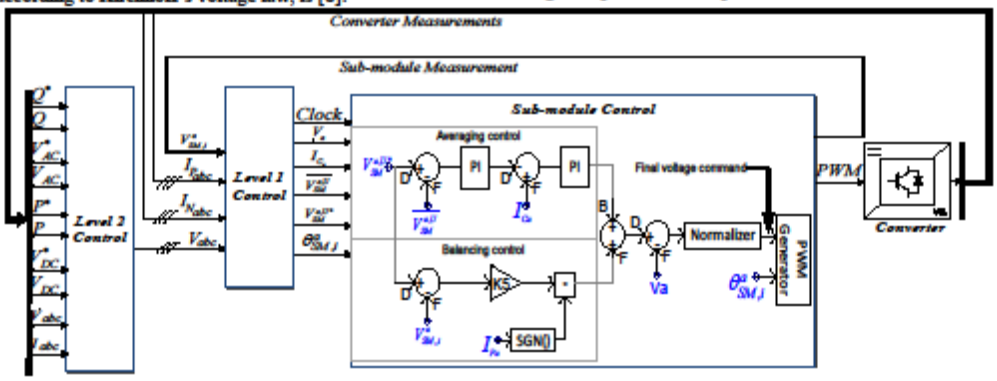


Figure 3: Implementation of converter control with focus on a sub-module control from the upper arm in phase a

balancing control and its integration with the high level control. From the high level 1 control a voltage reference for the entire phase A is given (Va) which will be included in the balancing controller. The balancing controller shown is specific to any sub-module in the upper arms of phase A. The level 1 controller measures the positive ($I_{P_{abc}}$) and the negative ($I_{N_{abc}}$) arms currents, and then send an mean of the phase currents (I_{C_a}) to each sub-module to be used in the averaging controller. The sub-module also receives a capacitor voltage reference ($V_{SM}^{a,U*}$) identical to the entire arm(U=upper arm) in the phase A which needs to be followed and an average of the capacitors voltages ($\overline{V_{SM}^{a,U}}$) in the entire arm of the phase. From the capacitor voltage reference, the balancing controller subtracts its instantaneous value and multiplies it with the sign of the current in the arm, in this case the upper one (I_{P_a}). The signals from the balancing controller are added up together and then normalized before being fed into a PWM generator. The PWM generator receives a phase displacement angle ($\theta_{SM,i}^{a}$) specific to its position in the arm (i) in order to generate the PWM for the sub-module. It can be observed in Figure 4 that the sub-module balancing control forces the sub-module voltages to reach an equal distribution independently on the particular phase shift of the triangular carrier in case of failure and bypassing of one SM with a slight increase in the voltage.

1. Loss Analysis

The current in the devices is spread unequally in a SM; the lower switch and the upper diode conduct a higher amount of current. The average positive and negative arm currents have to be obtained in order to calculate the switching losses. They can be derived analytically and can be confirmed by the simulations. Simulations scenarios show that for different switching frequencies and arm inductors different efficiencies can be achieved (see Table II.). For this case 260 Hz has been selected leading to a high total efficiency of 98.5%

Table II. – Efficiency vs Switching frequency for 10MW/20 kV MMC

			Arm inductor value				Total eff.%
			1 mH	2 mH	3 mH	5 mH	
Switching frequency	260 Hz	Cond. losses, kW	79.56	78.23	77.92	78.70	98.5
		Sw. losses, kW	37.066				
		Total losses, kW	116.6	115.3	114.9	115.6	
	360 Hz	Cond. losses, kW	78.94	77.06	76.99	77.69	98.2
		Sw. losses, kW	51.322				
		Total losses, kW	130.3	128.4	128.3	129.0	

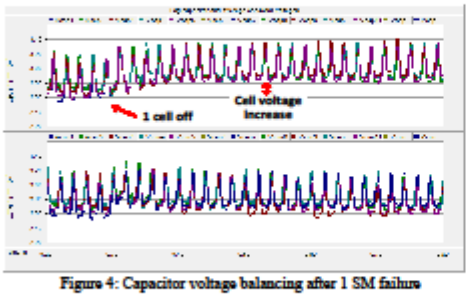


Figure 4: Capacitor voltage balancing after 1 SM failure

2. Distributed control

Figure 5 shows the data exchange between a master and a slave. The master send a global broadcast to the entire converter in terms of: modulation frequency, modulation index, PI controller's gains, operation mode (converter/inverter) and an enable command. This global broadcast will be resent only when one of the values needs to be changed.

A leg broadcast is sent separately to each leg to set the phase number. This value (0-3) will be multiplied with the angle difference between each phase in order to create the 3 sinusoidal references for the PWM. This value will be updated only when it is needed. The circulating currents will be averaged from the measurements done by the master and sent to each slave from the leg in order to be used by the balancing controller.

An arm broadcast is sent with the number of sub-modules from a leg, the phase displacement angle, the reference capacitor voltage and the average from the last update cycle. The phase displacement will be used by the slaves in order to ensure proper distribution of the triangular waves. The capacitors average value will be updated during each cycle, while the other will only be update when reconfiguration is needed.

Finally each sub-module will receive an individual message containing its position in the arm, in order to ensure proper distribution of the modulation.

In turn, each sub-module will communicate each cycle its capacitor voltage, and its status. This will ensure than the communication won't be interrupted and that no sub-module is faulty and disrupt the proper operation.

3. Communication Technology

Industrial Ethernet has been developed and takes advantage of well-established Ethernet [11] (speed up to Gbs, large number of nodes, and low cost hardware). There are different industrial Ethernet implementations available for complex drives systems and other control applications which require high bandwidth, fast updates

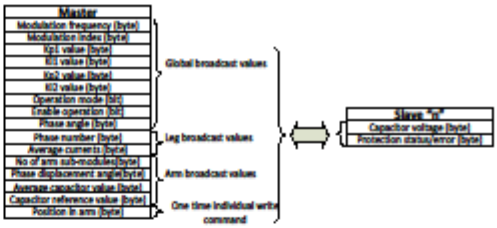


Figure 5: Variable communication

times and good clock synchronization. There are different implementations already on the market, most of them proprietary and hard to interconnect. Some implementations have been released as open source: ProfiNet [12], EtherCAT [13], etc. Due to its better performance [14] for this protocol EtherCAT was chosen as a communication solution.

EtherCAT is an open source protocol currently managed by the EtherCAT Group (ETG) [13]. It uses standard Ethernet frames as defined by IEEE 803.2 [11]. In theory Master and Slave can be implemented by using standard

off the shelf interfaces (PHY and MAC), but in order to improve the package forwarding delays the slaves are implemented on hardware like FPGAs or ASICs. The Master on the other hand can be implemented on any off the shelf hardware, without any special requirements. A typical EtherCAT network consists of at least one master unit and up to a theoretical 65535 slaves. The communication speed is limited to 100Mbps, and although in theory it could go up to gigabit speeds, however, no existing slave hardware can handle that high speed.

At the moment there is a wide variety of master code implementations to suit the needs for the industry. The slave code has been implemented on a large number of FPGAs and ASICs, giving the user flexibility in choosing the optimum solution. A typical EtherCAT telegram and its integration into an Ethernet frame is presented in Figure 6.

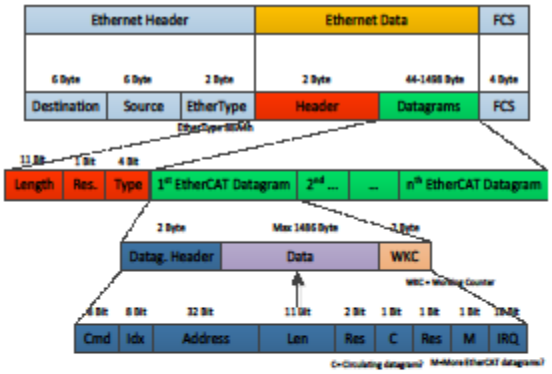


Figure 6 - Ethernet frame with EtherCAT data structure

All the EtherCAT telegrams are initiated by the master. As the telegrams pass thorough the slaves hardware, each slave reads the data addressed to it and writes the requested data in its assigned position inside the telegram. This normally translates in propagation delays under 500ns, depending on the used implementation [14]. More than one slave can be addressed in a telegram. This mechanism provides a better bandwidth usage compared to traditional Ethernet frames, due to the minimum frame size. The communication cycles can be defined in the master, and can be as low as 50 µs. Each cycle can send more than one telegram, and in case the update time is shorter than the time needed for the telegram to travel back, the master program will be signaled and the refresh time will be increased in order to accommodate the traveling time.

To facilitate the communication, each EtherCAT slave controller (ESC) has a 3 buffer memory. This ensures that the latest information will always be present between the telegram and the micro-controller (µC), in case the update times of one of them is faster than the other. As soon as either the EtherCAT processing unit or the µC starts writing the first bit in one of the 3 buffers, that buffer gets locked until the last bit is written. At that point the buffer is available for reading. This is handled automatically by the ESC.

EtherCAT offers its own implementation of IEEE 1588 [15]. The clock synchronization is implemented in the hardware, allowing for an accuracy of below 1µs (mostly determined by the clock source used by the hardware). The slave closest to the master normally is the clock master or reference clock in an EtherCAT network, and because of the use of distributed aligned clocks, they are tolerant to communication faults and delays compared to fully synchronous communication.

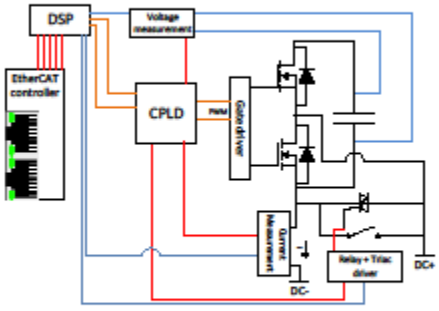


Figure 7 - Sub-module construction
Red: logical signals; blue: analog signals; orange: PWM.

Typical slaves have at least one communication port, but it can be extended up to four, allowing the network to be constructed based on any topology. The telegram is read/written as it passes from port 0 to port 3 by the EtherCAT processing unit and then forwarded to next opened port. In case port 0 is closed, as the telegram passes it, the circulating counter will be increased. If the telegram passes again through a closed port 0, the telegram will be destroyed. This is a safety feature in order to ensure, that in case of a communication failure with the master a telegram will not keep circulating in the ring and possible give erroneous commands to the slaves.

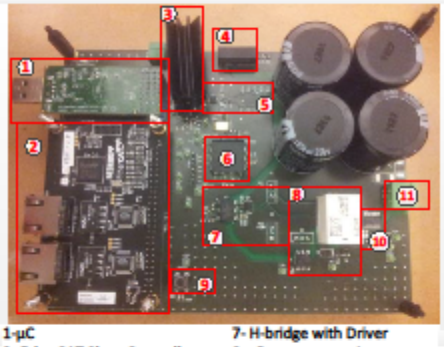
1. Reduced Scale Prototype

For the communication testing a 9 level (16 sub-modules) 10kVA 400Vac single phase MMC is constructed, supplied from a 800V DC-Link. For the control of the converter a distributed controller topology will be used, with phase-shifted triangular carrier pulse width modulation [16]. The master will decide on the modulation frequency, index and phase shift based on the number of modules connected, and the input and output voltages. In order to limit the circulating currents and the unbalance between the sub-modules capacitors, the balancing controller presented in [17] will be used.

It is composed of 8 half-bridge sub-modules per arm. The picture of one sub-module is shown in Figure 8. The used Microcontroller is a Texas Instruments TMDX28069USB. The EtherCAT communication is connected through a piggyback card with an ASIC ET1100 from Beckhoff, which is further connected to the microcontroller via 10MHz SPI bus.

The Half-bridge and capacitors are galvanic isolated from the control part of the board, allowing the high-voltage ground to float as it desires. The power on the high voltage ground is supplied trough a DC/DC converter for the lower Mosfet, while for the higher Mosfet a bootstrap configuration is used. The Driving IC provides insulation of the signals and a dead-time protection of 100us delay.

Figure 7 shows a simplified electrical schematic of the module. The blue wires present analog measurements, the orange lines represent the PWM, the red ones the digital signals while the black ones the power connections. DC+ and DC- are the 2 terminals of the sub-modules. The current is measured on the negative side of the capacitor, and together with the voltage measurement will is used for the balancing controller and modulation. Both measurements will also provide a digital signal for the CPLD when a dangerous situation is present (over-voltage/over-current) in order to trigger the protections. The protection is implemented using a triac and a relay across the connection terminals of the board. In case of



1-µC
2- EtherCAT Slave Controller
3 – 5V Vreg
4 – Insulated DC/DC converter
5 – Voltage measurement
6 -CPLD
7- H-bridge with Driver
8 – Bypass protection
9 – Trigger button
10 – Current measurement
11 – H-bridge connection terminal

Figure 8: Reduced Scale prototype SM

fault the sub-module will be bypassed. The triac provides fast reaction times until the relay which closes slower, will provide a crowbar permanent connection.
In order to synchronize the Microcontrollers, the communication board provides two synchronization signals which can be configured to trigger on all the modules at the same time. These synchronization signals can be used to inform the µC that the communication buffer holds new data. Also it can inform that new communication data should be written in the buffer in order to be read by the passing telegram in the current communication cycle.

1. Fault tolerance

As mentioned before, the MMC should continue proper operation with one or more (based on design) faulty sub-modules. Among the faults which can be handled there are: over-current due to capacitors short circuit, switching devices failure or communication failure.

a. Detection and bypassing of a sub-module in case of short-circuit or over current fault

As described in the previous section, the board has different hardware implemented protections in order to have a fast reaction time. Although dead-time is implemented in the modulation, the driving circuit is designed to not allow shoot-troughs. If one of the Mosfets will get blocked in close position, as soon as the other Mosfet is closed, the capacitors will be short-circuited and the voltage across their terminals will drop very fast.
When the DC-link is short-circuited a high current is generated which might overheat and damage the switching devices. The voltage and current is measured constantly in order to be used for the control, but at the same time also for protection. As soon as the voltage drops under a pre-defined (non-operating) voltage, which means there is a short circuit in the H-bridge, or the current increases over the nominal value for more than 100nS, the CPLD will disable the modulation. The module is bypassed by enabling the triac through an optotriac and by closing the relay. The Triac is used for its fast reaction time, but in order to limit the impact of the bypassed module, a relay will be used to permanently bypass the sub-module.
When the protection is activated, the CPLD will also signal the µC, and at the next communication cycle the master will be informed about the bypassed module. In case the over current protection is triggered on too many modules, the master, will automatically open the circuit breaker on the DC-link, signaling a DC-link short-circuit. All this will normally happen in 2 communication cycles which should take maximum 100 microseconds.
When only one module is bypassed, the master reconfigures the rest of the sub-modules in order to compensate for the by-passed module, while the µC from the by-passed module will try to diagnose the fault and decide if it can still participate in the modulation.

b. Detection and bypassing of sub-module in case of communication fault and online reconfiguration

Unless a message is broadcasted, each slave would normally have a datagram address directly to it. EtherCAT has different communication fault detection mechanism built inside. The most easy to use is the working counter. As the telegram leaves the master it will have a working counter (WKC) equal to "n", where "n" is the number of slaves that telegram is addressed to. Based on the CMD byte, the slave will have to read or write or read and write in that datagram or do nothing. Each time the slaves sees a datagram addressed to it, it will take the WKC and subtract 1 for a write command and 2 for a read command, if the command issued by the master was successful. When the telegram will return to the master, it will look at all the working counters and compare them to the expected values, determining if the communication was or wasn't successful with one or more slaves.
In order to achieve communication redundancy the simpler solution is to use a ring configuration as shown in Figure 9a. While the cable is intact, the same telegram is sent to both ports A and B. The telegram which leaves port A (orange) will pass through the ESC of each sub-module, and will get forwarded to the next opened port until it reaches port B of the master. The same instance of the telegram will leave port B towards port A. As it is not entering in each sub-module on the main port (port zero), it will be directly forwarded to the next opened port until it reaches port A of the master. Normally, he first slave will be chosen as reference clock.

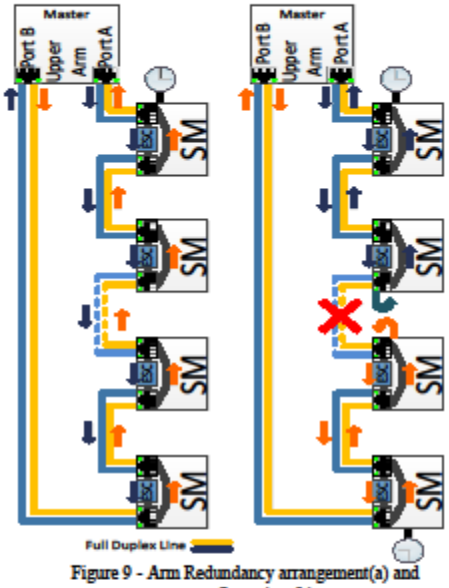


Figure 9 - Arm Redundancy arrangement(a) and reconfiguration (b)

In case of a failure (Figure 9b), the telegram which leaves port A, will be returned by the ESC of the second sub-modules as it noticed that the output port got closed by the broken cable. It will return to the master through the same port (port A). The same telegram left at the same time from port B of the master, it will get to the now closed connection port of the 3rd sub-module, and it will be automatically forwarded to the first open port (back). As it return it will pass through each ESC of the sub-modules. Both instances of the telegram should return at the same time to the master. The master will notice that each telegram has an invalid WKC, but it will try to put the 2 instances together, observing that they are forming a valid telegram. At this point the first sub-module from port B will be designed as a master clock for the newly created ring. This will permit the configuration to continue running without any problems.

The same approach will be taken in case of a sub-module failure. The only difference will be that the master will retry to send the telegram a few times to be sure that the ESC wasn't busy at the moment when the telegram passed. In case one of the sub-modules will be unable to communicate, the master will detect the error for datagram designed for that sub-module, will continue normal operation with the rest of the sub-modules, and will signal the control which sub-module is disconnected. The µC of the affected sub-module will enter into a safe state until communication is restored and will bypass the module in order to allow normal operation of the MMC.

1. Conclusions

MMC topology proves its superiority against 2-level topology in efficiency, reduced filtering requirement and fault tolerant operation. The distribute nature of this converter calls for a distributed control architecture based on real-time communication where the SM carries the capacitor balancing task in an autonomous way. The SMs are switched at very low switching frequency (260 Hz) resulting in very high efficiency. In order to ensure a high apparent switching frequency, all SM are interleaved by providing a shift delay for the carrier. EtherCAT has been showed to be a good candidate for complying with the requirements of real-time control and especially for its ability to provide fault tolerant operation and on-line reconfiguration during SM failure and bypassing. Also it can be designed with redundancy in order to ensure communication optic fiber break tolerance. A reduced scale prototype has been built to validate the control strategy, balancing controller and communication.

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Appendix B – Laboratory implementation of small scale MMC prototype

In order to validate the control strategy, communication, fault tolerance and redundancy a small scale prototype was built in the laboratory. Since the main focus of the project was fast Ethernet based communication with fault tolerance and a scalable SM.

A single-phase MMC with four modules per arm was constructed. Since it was beyond the purpose of this project, the converters output will only have to follow a voltage reference and the load will be a simple RL load.

The SM parameters are summarized in Table B-1.

Table B-1: SM design parameters

Capacitor Nominal Voltage	100V
Sub-module Nominal Current	18A
Switching Frequency	840Hz
Minimum Insulation level for Power Plane	1kV

B.1. EtherCAT Overview

The converter is composed of 8 identical SMs connected to each other through an EtherCAT communication. The high level control is implemented on the EtherCAT Master. The communication is split into two networks for each arm, with redundancy ring connection. The DC-link is generated and supported by a 400V DC laboratory power supply. This value was chosen due to the available laboratory equipment. Due to safety concerns while operating converters with large capacitance, voltages above 60VDC and more than 1A, the entire converter will be placed in a metal cabinet which will be grounded to a protective earth.

High Level control and Master implementation

The Master control (or high level control) is implemented on an Industrial Personal Computer (IPC) developed by Beckhoff. The EtherCAT master software used is TwinCAT 3 from Beckhoff running on a Windows 7 x86 operating system. This is simple and powerful software which allows different integration option for the communication and is running in a Microsoft Visual Studio shell. For this project the high level control will be implemented in C++ and directly integrated into the TwinCAT3 software. Since the converter is designed to be further used with Simulink integration, a more powerful processor was chosen: Intel i5. In order to work seamlessly with the EtherCAT communication an Intel based solution was chosen for the network adapters, as TC was designed to work directly with the adapter, eliminating the need for an intermediate driver which might insert delays. In order to allow for redundancy, 4 network adapters are needed, two for each arm, and extra space is available in order to be able to add more adapters in the future. Figure B-1 shows the EtherCAT master IPC used in the implementation.

Figure B-1 – EtherCAT master Industrial PC [59]

Sub-module implementation

The SMs will be connected using FB1111-0141 from Beckhoff[48]. This is a specially designed development board with an ET1100 ASIC [43] with SPI configured PDI. Although the maximum SPI speed can be up to 20Mhz, it will be limited to 10Mhz since this is the maximum speed of the Digital Signal Processor (DSP) used to implement the SM control. The ASIC has implemented all the advantages of the EtherCAT mentioned in Chapter 3.The piggyback communication board is shown in Figure B-2. All the communication boards have the same dimensions and connection headers, the only difference between them being the ESC and PDI used. Being an add-on board, it conveniently connects to the SM PCB through a 52 pins header. The connection pins are shown in Figure B-3. Pin 10, signals when the ASIC finds the proper configuration in the EEPROM memory. This pin is routed

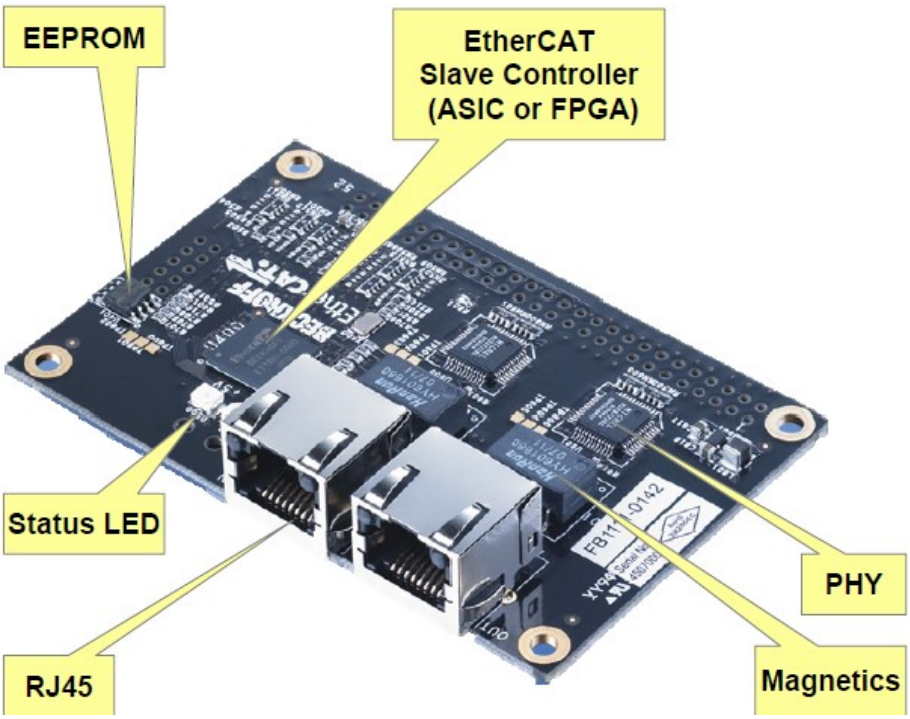


Figure B-2 – FB1111-014x board [44]

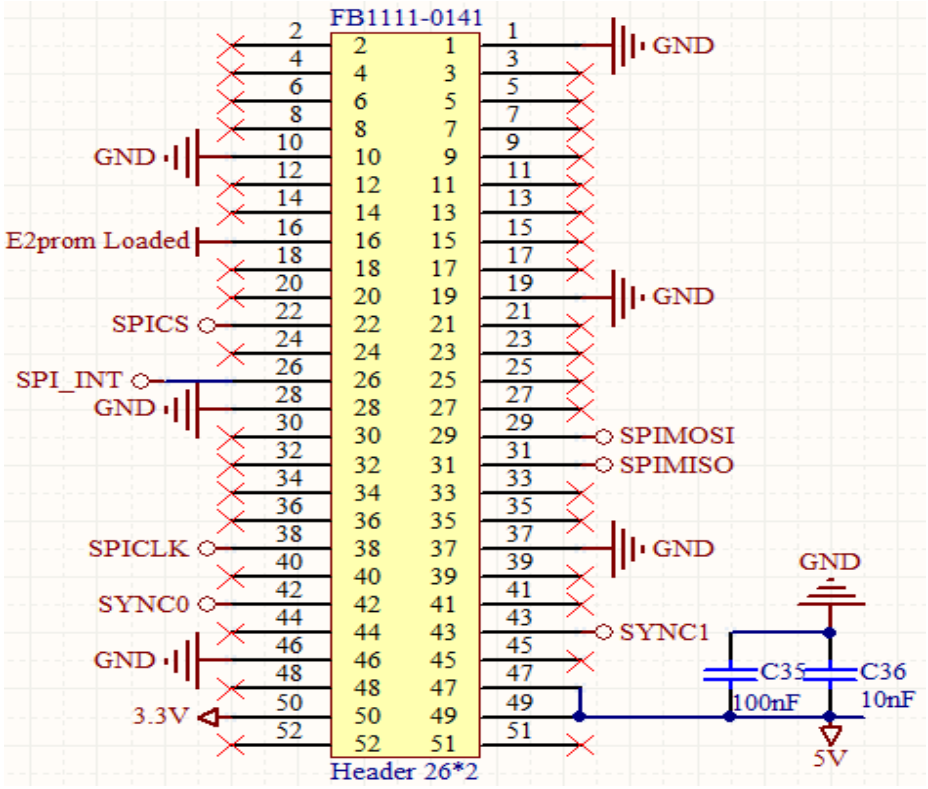


Figure B-3 – Piggyback connection header

to the microcontroller via the Complex Programmable Logical Device (CPLD), in order to visually signal the operation via a Light Emitting Diode (LED) and inform the microcontroller about the State.

The communication SPI pins (MOSI, MISO, CLK) are connected to the hardware SPI pins of the microcontroller. While the Chip Select (CS) pin is connected to a General Purpose Input/Output (GPIO) pin for more flexibility when selecting the ASIC.

This is done in order to suite the SPI configuration of the ET1100. Since the communication should be as fast as possible and the latest data should always be available, no sending/receiving buffer can be used in the SPI implementation. Under normal operation the CS pin gets low before the first bit is transmitted and returns to the idle position after the last bit I transferred or received. This will make the communication unusable, since the first message the ASIC will reply after selection will be the state error (or no error) code. The CS has to be kept low to transmit the other data, otherwise the communication will be stuck into a loop where only the state is read. This can be easily achieved by manipulating the CS line from the software.

The SYNC0 and SPI_INIT interrupt lines are connected directly to the microcontroller interrupt pins. This allow for a fast response when the clocks and applications of the SM need to be synchronized, in the case of SYNC0 output. The SPI_INT is used by the ET1100 when it needs to signal the microcontroller that it has data to transfer. The SYNC1 line is not used in this project, but to allow its implementation in the future without changing the design, it was routed to the CPLD, and when needed, it can connect through this to the microcontroller.

The 5V pins are presented with the decoupling capacitors. The total power consumption should be under 0.5A. The 3.3V is an output from the internal voltage regulator of the piggyback and can output up to 100mA.

B.2. Sub-module overview

The SM board where designed based on the simplified line schematic shown in Figure B-4 and has the following features:

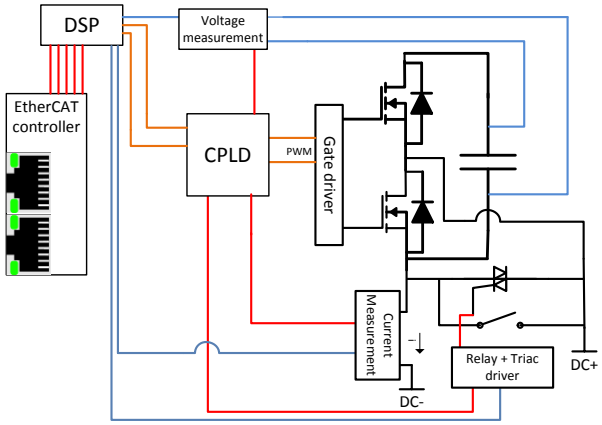


Figure B-4 – Sub-module simplified line schematic[36]

- Plug-in TMS320F28069 control stick;
- 4 layer Printed Circuit Board (PCB);
- Xillinx XC9572XL CPLD based dead-time and protection;
- 100V nominal SM voltage;
- Header for EtherCAT piggyback boards connection with SPI;
- Galvanic insulated half-bridge driving circuit with bootstrap power supply;
- JTAG interface for CPLD;
- Mixed analog and digital design;
- Reduced size;
- In-rush current and SM bypass circuits;
- Hall Effect current sensors.

The schematic can be split into two parts: control and power, which are electrically insulated from each other.

The microcontroller will be connected to the ESC via SPI. It will also be responsible for the PWM signals, for the mosfets driver, which will be generated based on the communicated data and current and voltage measurements. The CPLD will be responsible for generating the dead-time between the 2 PWM signals and also for the protection of the SM based on current and voltage measurements. If any fault is detected, the CPLD will close the protective devices (Relay and TRIAC) and signal the fault to the microcontroller. In the control side, the DSP supplies 1 PWM signal (although 2 are connected) which are a result of the modulation and balancing controllers. The PWM signal is then sent to the CPLD which will insert dead-time and will create the complementary signal for the lower Mosfet. The PWM signals from the outputs are then feed into a half-bridge insulated Mosfet driver which will control the half-bridge of the SM.

As the current direction is needed in the control strategy, the current measurement will be acquired via a Hall Effect sensor. The sensor will transmit an analogue signal to the DSP through the Analogue to Digital Converter (ADC). The same sensor is used for detection of the over-current event as it has this function built in, and the over-current state will be transmitted to the CPLD in order to take the appropriate steps.

The SM capacitors voltage is acquired using a differential operational amplifier. The signal is fed to the DPS via its ADC ports. The same signal is passed through two comparators in order to signal logically to the CPLD if the capacitor voltage is too high, or if the capacitor is short-circuited, in order for the CPLD to try and protect the SM and the entire converter.

As the CPLD is a hardware device, response times are greatly reduced, allowing for fast reacting protections.

B.3. Capacitor and arm inductor selection

The calculations for the capacitors have been shown in chapter 4.1 and since the same converter was built, no extra calculations will be shown.

Figure B-5 – Panasonic Capacitor [49]

In order to have a capacitance per SM of 6mF, four 1.5mF electrolytic aluminium capacitors in parallel are used. The capacitor selected for this application is a 200V 1.5mF Snap-in capacitor from Panasonic. Its main advantage is represented by its small dimensions (30mm diameter, 50mm height) and its high current ripple handling (5.22A) [49].

For the inductor, two 1.6mH laboratory inductors were used.

B.4. Switches

When selecting the switching semiconductors for the MMC one needs to take into consideration the capability of the devices to switch at low switching frequencies. The devices need to be able to switch with low frequency and, at certain points of the start-up procedure, continuously conduct DC voltage. After long consideration the FDL100N50F N-Channel Mosfet from Fairchild with included freewheeling diode was choses (Figure B-6).

Figure B-6 – FDL100N50F TO264 Packaging [50]

This semiconductor presents two important qualities: capability to continuously conduct at the nominal current of the SM and negative thermal coefficient of the freewheeling diode. From Figure B-8 it can be notice, that the Mosfet can continuously conduct DC current of over 20A at 100V and if it is switched faster than 10Hz the drain current can be as high as 100A. In Figure B-8 the body diode forward voltage is plotted against temperature and drain reversed current. The graph shows that if the temperature increases, for the same temperature, the forward voltage will get smaller. This will result in lower heat

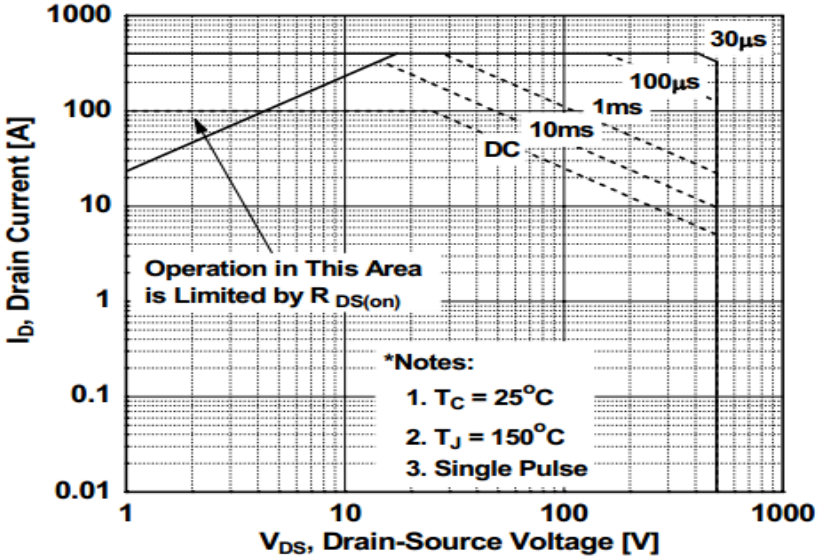


Figure B-7 – FDL100N50F Safe Operation Area [50]

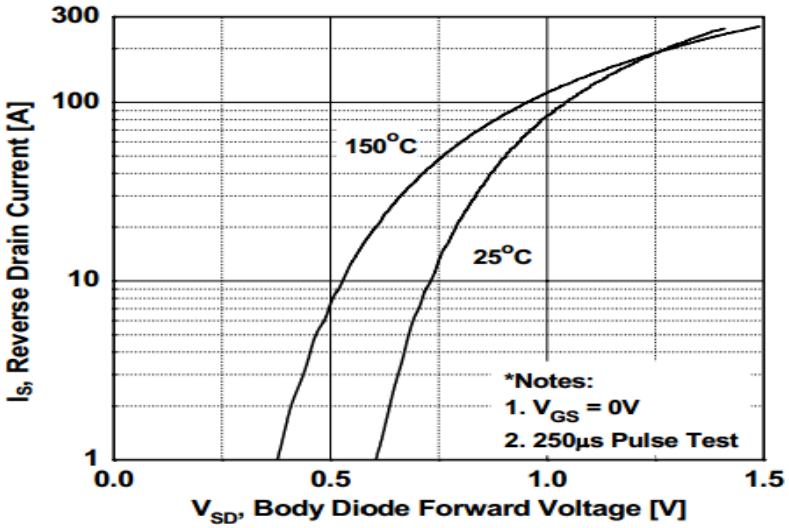


Figure B-8 – Diode Forward Voltage vs. Temperature and Current [50]

dissipation, as the devices cools, the forward voltage will increase. This is called a negative voltage coefficient, since theoretical the diode can cool itself down.

The Mosfet present good ON-resistance, which is typically 43mΩ, and a normalized on resistance against temperature coefficient under 2. Other important aspects of the Mosfet are the low gate charge, which means lower current requirements from the driver and the higher operating temperature (150˚C). The full characteristics of the device can be consulted in [50].

B.5. Gates Driver and Protection

Gates Driver

When choosing a gate driver, different aspects were taken into consideration: built-in insulation, half-bridge driving capability, easy dead-time implementation, driver disable function and possibility to be used in a bootstrap configuration.

The SI82233BB-C-IS Integrated Circuit (IC) from Silicon Laboratories, Figure B-9, was chosen based on its qualities. The IC contains two isolated drivers in the same SOIC16W package. It can support up to 2.5kV potential difference between inputs and outputs and up to 1.5kV between driving outputs. The peak sourcing/sinking currents can be up to 4A with a maximum of 60ns propagation delay. It has two independent inputs for the High Side (HS) and Low Side (LS) of the half-bridge with overlap protection and programmable dead-time protection.

The dead-time and overlap protection prevent the HS and LS signals to be high at the same time. The overlap protection will put both output low while the inputs are overlapping; this is useful in order to protect the Mosfets from short-circuiting the SM capacitors. The dead-time can be

Figure B-9 – Si8233BB-C-IS SOIC16 Packaging [51]

programmed by a single resistance connected to the dead-time pin. If no resistance is placed, the dead-time will be approximately 400 ps. The dead-time resistance (R21) can be calculated as:

$$DT = 10 \cdot RDT \tag{5.1}$$

where:

DT – dead time (ns);

RDT – dead-time programming resistor (kΩ).

The implementation circuit of the driving circuit can be seen in Figure B-10. The PWM_HI and PWM_LO input signals from pins 1 and 2 are the control signals for the half bridge. They should be complementary but since dead-time control was desired, they were implemented with separate inputs. The DIS signal from pin 5 of the IC allows the driving circuit to be disabled by putting both outputs low.

The driver has 3 supply circuits, one on the control side which has a nominal supply voltage of 5V, and two supply circuits on the driving side which have a nominal voltage of 12V. The 12V comes from a MER1S0512SC regulated DC/DC converter with 2kV insulation level and 2W nominal power. The 100nF capacitors are for IC decoupling purposes, while C3, C4 and C4 are for output smoothing from the DC/DC converter. Because of cost consideration, the HS of the driver will be supplied from a bootstrap circuit as shown in Figure B-10. This is connected through a decoupling capacitor to the supply pin of the lower driving circuit of the IC. When the upper Mosfet (Q1) switches on, it will pull the middle point of the half-bridge to a high potential and the 12V power supply will be negative in relation to it. Ignoring the other problems which might appear, there will be no power to keep feed the gate charge. The bootstrap circuit is comprised of a bootstrap capacitor (C25) whose purpose is to supply the driving circuit for the high side while Q1 is conducting and the bootstrap diode (D7) whose purpose is to block the voltage potential which will appear when Q1 is conducting. The operating principle of the circuit is simple: when Q2 is switched on, the bootstrap capacitor gets charged through D1 since its ground is connected via Q2 to the power ground. When Q2 switches of and Q1 switches on, the capacitor will float and its ground will be connected to the high voltage potential, while D1 will protect the supply circuit from this potential. Attention needs to be paid when selecting the bootstrap capacitor, as it needs to be big enough to keep the gate supply constant. The diode has to

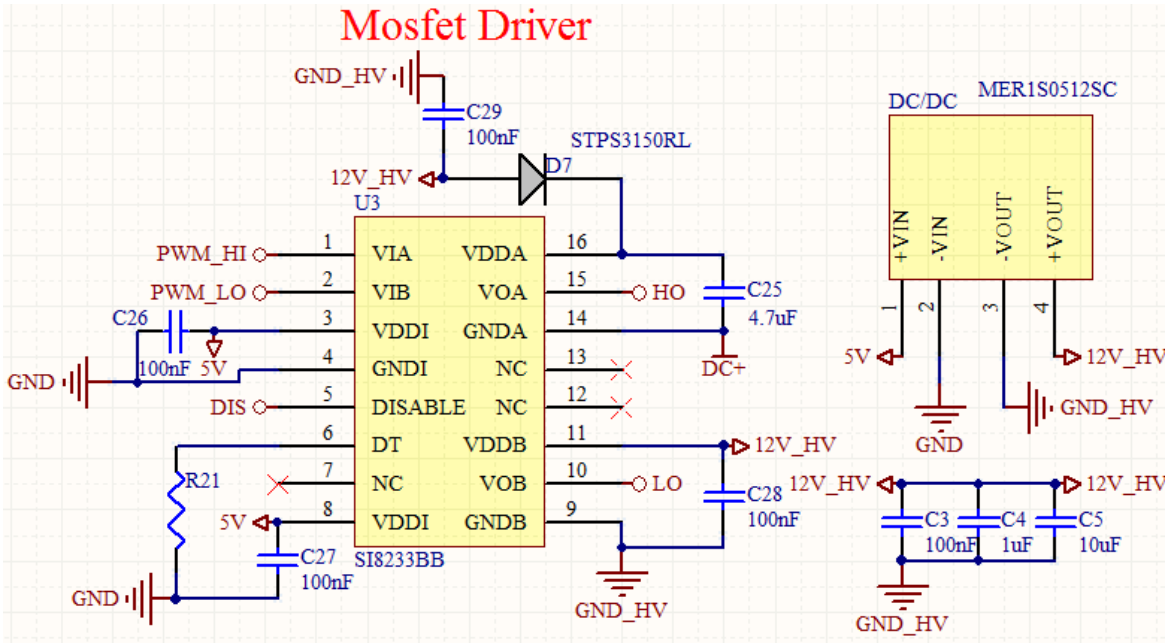


Figure B-10 – Mosfet Driving circuit

be selected in order to block the voltage which might appear across Q1 plus a safety margin of at least 25V in order to accommodate for transients and to consider the voltage across the bootstrap capacitor.

The calculations for the bootstrap circuit are done considering the switching frequency and the gate charge of the Mosfet. By looking in [50], the total gate charge, $Q_{g(tot)}$, is $238\,nC$. After this is obtained, a maximum allowed voltage drop, ΔV_{BST}, for the driving circuit is selected, typically 0.1V.

The minimum capacitor is then calculated as:

$$C_{BST} = \frac{Q_{g(tot)}}{\Delta V_{BST}} = \frac{238nC}{0.1V} = 2380nC \tag{5.2}$$

The rule of thumb is to select a good quality ceramic capacitor with some reserve, usually double the size is a good practice. For this circuit the bootstrap capacitor is a 4.7uF multilayer ceramic capacitor from TDK.

A Schottky diode is generally recommended as the bootstrap diode because of its low forward voltage drop and fast reaction times in order to maximize the power available for the high side Mosfet. In order to support transients, the diode should have higher ratings than the maximum voltage across the half-bridge. At the same time, the diode has to be able to charge the capacitor. For this the average forward current for selecting the diode can be estimated based on a maximum switching frequency ($f_{\max}$) of 2kHz as:

$$I_F = Q_{g(tot)} \cdot f_{\max} = 238nC \cdot 2000Hz = 0.477mA \tag{5.3}$$

Considering the above, the bootstrap diode is S2J from Multicomp. It can handle up to 2A and 600V with a forward voltage of only 1.15V and a recovery time of $2\mu s$.

The driving circuit needs to load the Mosfet gate charge in order to open it, and most of the times a gate resistance needs to be present in order to limit the current. The resistance can be calculated based on the gate charge and the turn-on delay time, $t_{d(on)}$, and turn-on rise time, t_r. The equation for the gate current is then computed:

$$I_{gate} = \frac{Q_{g(tot)}}{t_{d(on)} + t_r} = \frac{238nC}{186ns + 202nS} = 0.6134A \tag{5.4}$$

After this, considering the supply voltage of the driving IC, V_0, and the nominal current gate voltage, V_{GS,I_0}, the gate resistance can be calculated based on the gate current:

$$R_{gate} = \frac{V_0 - V_{GS,I_0}}{I_{gate}} = \frac{12V - 10V}{0.6134A} = 9.34\Omega \tag{5.5}$$

By looking in [51], the gate output source resistance is shown to be 1Ω. This means that the gate resistance should be decreased by 1.

Another rule of thumb when driving a half-bridge in bootstrap configuration is operating the lower switch faster than the upper one in order to avoid ringing in the gate signals. Considering the EMI problems, and ignoring the efficiency, the gate resistances have been selected as 20 Ω for the upper switch and 15 Ω for the lower switch.

Under Voltage Lockout

Under voltage conditions might appear at power up, during operation if a short-circuit condition is present on the supply rail or during shutdown.

The Under Voltage Lockout protection prevents the circuit from functioning with voltages which might be insufficient to put the Mosfet in conduction mode in a safe way. This ensures that when the voltage on the outputs side falls under 8V, the outputs are clamped low until this state passes.

Signal Acquisition

To ensure that the SM operates in its safety region, and in case of fault, to protect the SM and allow the converter to continue operation, different hardware protections are considered. The protections implemented for this design are:

- SM in-rush current protection;
- SM capacitor over-voltage protection;
- SM short-circuit protection.

In order to implement these protections, measurements need to be taken. The SM current is measured using a ACS709LLFTR-35BB hall effect based IC sensor from Allegro Microsystems. The SM capacitors voltage is measured using Analog Devices AD8276ARMZ differential amplifier.

The voltage measurement is passed through both operational amplifiers of STMicroelectronics LM2904DT voltage comparator used in window configurations.

Current acquisition

The Allegro ACS709 current sensor IC is an economical and precise way to measure currents in different application. It offers a small surface mount footprint which makes integration easy. It consists of a good precision linear hall effect sensor with a copper conductive path near the silicon die. When current passes through the copper path an analog output voltage from the sensor tracks its magnetic field generated. The Allegro ACS709, which is shown in Figure B-11, provides the following features [52]:

Figure B-11 – Allegro ACS709 Hall Effect Sensor [52]

- Industry leading noise with 120kHz bandwidth;
- Integrated shield to prevent capacitive coupling;
- Small footprint (QSOP);
- 2.1 kV RMS insulation between current path and IC electronics;
- 1.1mΩ primary conductor resistance;
- User scalable over-current protection with under 2 µs response time;
- ±2% output error;
- Filter pin for output filtering;
- 5V power supply;
- Chopper stabilization;
- Linear proportional output signal.

The current sensor is used as shown in Figure B-12 to measure the SM current on the lower side of the half bridge. Capacitor C32 is for by-passing purposes in order to filter noises which might appear as with any digital circuit. Capacitor C33 is the fault delay setting capacitor. By proper selection of

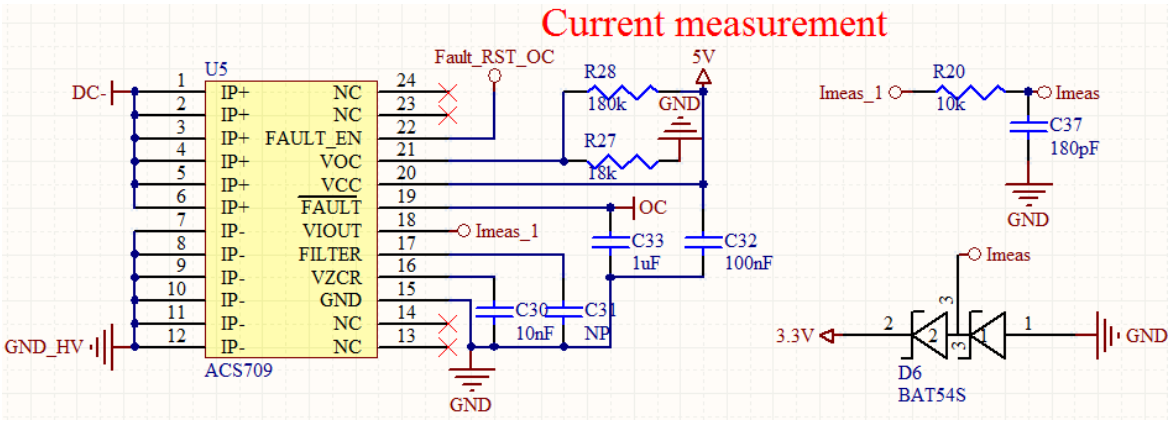


Figure B-12 – Current measuring circuit

this capacitor small timed transients can be ignored. C30 is connected to pin 16 of the IC, which is the voltage reference output pin. This pin is used as a zero current reference, and its output scales with the supply. C31 is not populates, as there is already a filter on the output line. But the footprint is there in case it is needed. This approach was taken because of the distance between the Hall Effect current measurement and the DSP. As with any analog signal it might pick up noise from close by digital signals and due to the inevitable inductance of the tracks, it will get amplified. A simple RC filter was placed close to the input of the DSP to limit that noise. In order to allow its use in a digital protection mechanism, the fault pin (pin 19) will stay high for as long as the current between the IP+ and IP- pins stays within the set limit. When there is an overcurrent this pin will be driven low by an internal transistor. In order to reset it, pin 22 needs to be placed high. Keeping pin 22 always high will keep the internal transistor always on and will render the feature inoperable. Both of the two digital pins are connected to the CPLD in order to allow a simple overcurrent protection [52].

Resistors R27 and R28 are used as a resistive voltage divider and their result is feed to pin 21. This voltage (V_{OC}) will be the reference voltage for the overcurrent fault pin.

The overcurrent voltage reference V_{OC} in mV can be calculated as [52]:

$$V_{OC} = Sens \cdot |I_{OC}| \tag{5.6}$$

where:

Sens – output voltage/current ratio of the IC in mV/A (28mV/A according to [52]);

I_{OC} - desired overcurrent set point in A.

Deciding on 16A maximum allowable current, the voltage reference for the overcurrent circuit can be computed:

$$V_{OC,16A} = 28mV / A \cdot 16A = 448mV \tag{5.7}$$

In order to obtain this voltage, the resistive voltage divider is supplied with 5V and will output:

$$V_{OC} = \frac{R27}{R28 + R27} \cdot V_{Supply} = \frac{18k\Omega}{180k\Omega + 18k\Omega} \cdot 5V = 0.454V \tag{5.8}$$

which is the equivalent of 16.23A, an acceptable error.

The analog current measurement is protected from going over 3.3V or below the ground potential using a dual series small signal Schottky diode in the form of BAT54S from STMicroelectronics.

Voltage acquisition

A good and cost effective solution for voltage measurements is the use of a differential amplifier connected across the SM capacitors through a high resistive impedance. The resistive network is made of two branches, each with 5 series connected resistors ($4 \cdot 560k\Omega + 270k\Omega$). This type of connection ensures that even if one of the resistors fails the control part of the board will not get damaged, although due to the large resistance the current across it will be small.

The differential amplifier chosen for this task is the AD8276 from Analog Devices [53]. The implementation of the AD8276 is shown in Figure B-14. The main criteria for choosing this differential amplifier are[53]:

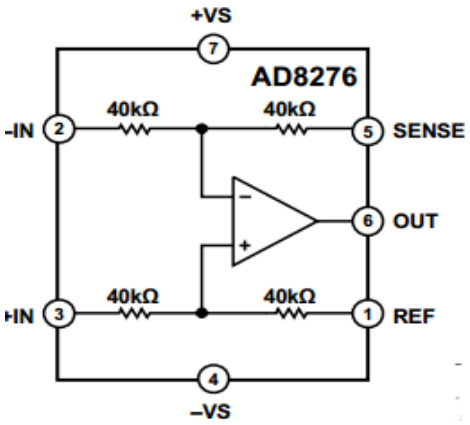


Figure B-13 – AD8276 Functional block [53]

- Wide input range beyond the supplies;
- Good input overvoltage protection;
- 550kHz bandwidth;
- Good common mode voltage rejection: 86dB;
- Single rail supply possibility.

The LT1366 is a special trimmed single differential amplifier supplied from a 5V rail. The supply pin is decoupled by a 0.1µF and 0.01µF capacitors since there is no separated analog power rail.

The inputs of the amplifier are protected from transients across the SM capacitors by two small signal diodes, TS148 from Taiwan Semiconductor. As mentioned earlier the voltage across the capacitors is measured through five series connected resistances with a total resistance of 2.51MΩ. the two 68pF capacitors at the inputs of the amplifier create a RC low pass filter with the resistors. The cut-off frequency of the filter can be calculated as:

$$f_c = \frac{1}{2 \cdot \pi \cdot R \cdot C} = \frac{1}{2 \cdot \pi \cdot 2.51 \cdot 10^6 \cdot 68 \cdot 10^{-12}} = 932.5Hz \tag{5.9}$$

As it can be seen from Figure B-13, the AD8276 has four laser-trimmed on-chip 40$k\Omega$ resistors. These resistors can be used to adjust the gain of the operational amplifier. The transfer function of the amplifier can be derived as in equation (5.10). Under normal operating conditions, the capacitor positive connection (V_Meas in Figure B-14) will have a nominal voltage of 100V in reference to the power ground, GND_HV. This ground under normal operation can swing on the entire range of the DC-link supply (±200V). Equation (5.10) assumes no potential difference between the ground of the power part of the board and the control ground, but the equations transfer function will be the same, independent of the voltage potential. If it will be assumed that the power circuit has a -200V potential compared to the control ground, equation (5.11) shows that the same transfer function applies since the differential amplifier only calculates the difference between the two inputs.

$$V_{out} = \frac{R_{\text{int}ernal,1}}{R_{\text{int}ernal,2} + R_{15} + R_{16} + R_{17} + R_{18} + R_{19}} \cdot (V_{cap} - GND_{HV}) = \frac{40 \cdot 10^3}{2.55 \cdot 10^6} \cdot (100V - 0V) = 1.569V \tag{5.10}$$

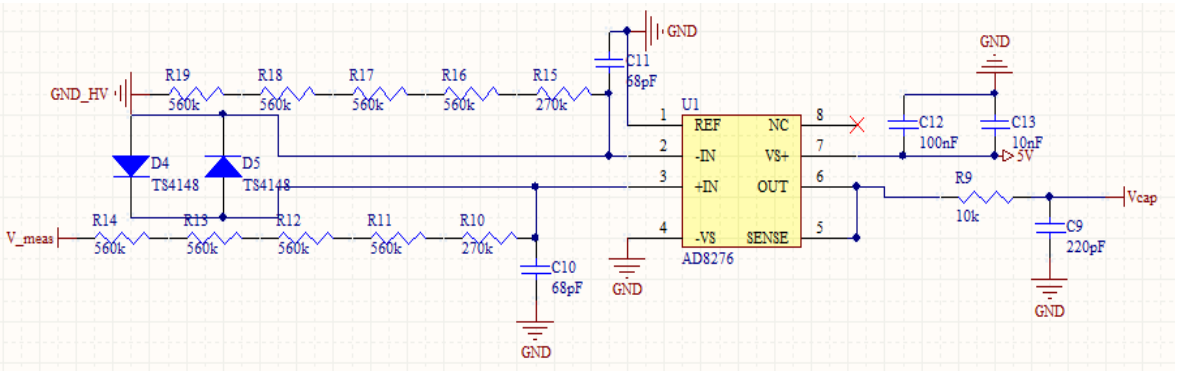


Figure B-14 – Voltage measuring circuit

$$V_{out} = \frac{R_{int,1}}{R_{int,2} + R_{15} + R_{16} + R_{17} + R_{18} + R_{19}} \cdot ((V_{cap} - GND_{HV}) - 200V) = \frac{40 \cdot 10^3}{2.55 \cdot 10^6} \cdot (-100V - 200V) = 1.569V \quad (5.11)$$

The output signal is sent to the ADC of the DSP after it is passed through a RC low pass filter composed of a 10kΩ resistor and a 220pF capacitor. The cut-off frequency of the filter is given by equation (5.12). The filter is placed close to the inputs of the ADC in order to filter the noise which might appear from the close by circuits.

$$f_c = \frac{1}{2 \cdot \pi \cdot R \cdot C} = \frac{1}{2 \cdot \pi \cdot 10 \cdot 10^3 \cdot 220 \cdot 10^{-12}} = 72.343kHz \quad (5.12)$$

Signal processing through comparators

The LM2904DT from STMicroelectronics was chosen as the window comparator due to its features [54]:

- High internal gain;
- Low supply current (typically 500μA at 5V);
- Temperature compensated wide bandwidth.

The voltage signal corresponding to the SM capacitors voltage is passed through two comparators which will be output an active high when the signal is not within the expected limits. The LM2904DT features two comparators in the same IC package, which are connected as in the configuration shown in Figure B-15. The comparator IC is supplied with 5V on pin 8 which is bypassed by a 10*n*F and a 100*n*F capacitor. The analog output from the voltage measurement is fed into the non-inverting input of the A comparator (pin 3) and into the inverting input of the B comparator (pin 6). As the inverting input for comparator A, a 779mV signal is fed from a resistive voltage divider. This would be equal to 49.67V across the SM capacitors and will be used to detect a short-circuit across the capacitors, since under normal operation the voltage should be 100V±10%. The output of comparator A will be fed to the CPLD for protection purposes, and will trigger high when the fault condition will be present. Special care needs to be taken during the start-up procedure, as during the charging procedure the signal needs to be ignored. The non-inverting input of comparator B is supplied with a 2.679V signal from a voltage divider. This will be equal to approximately 171V across the SM capacitors and will be used to detect when the capacitors get overcharged and might reach their maximum allowable voltage since even with one faulty SM in the arm the capacitor voltage should be 133V±10%. The output of comparator B will be fed to the CPLD for protection purposes, and will trigger high when the over-voltage condition is present.

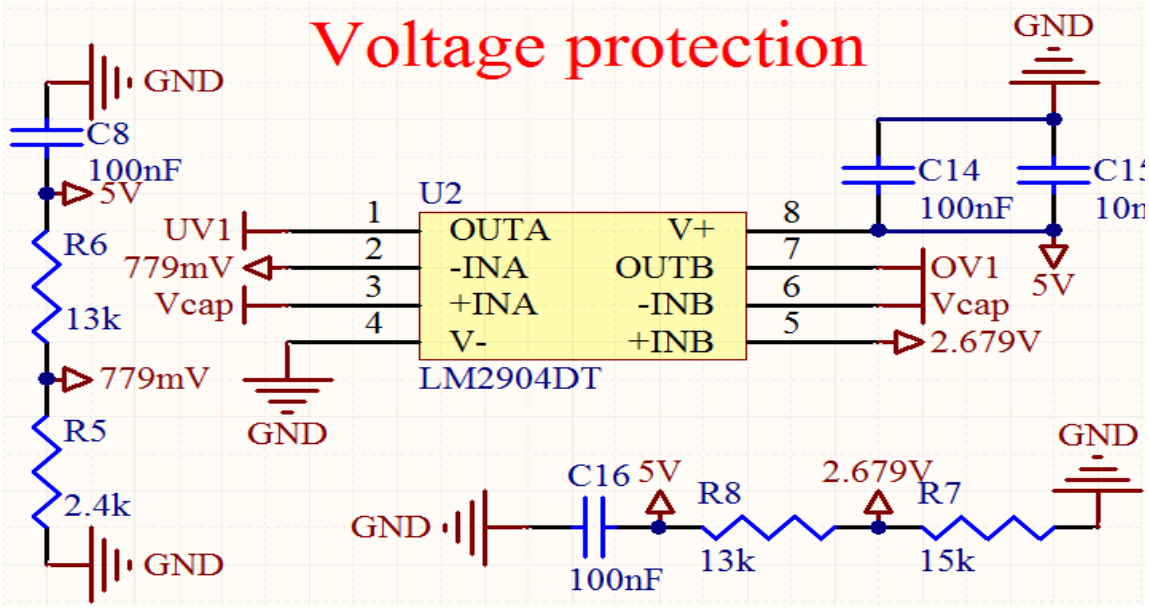


Figure B-15 – Voltage comparators

B.6. Sub-module failure and in-rush current protection

In order to ensure a proper protection of the switching devices and capacitors, the SM was designed with by-pass devices.

In order to protect the devices from faults and allow easy by-pass, two protection devices were implemented which can guarantee fast reaction times and permanent SM by-pass. The protection implementation can be viewed in Figure B-16. For fast reaction times, a Triac is used for its ability to switch independent of the current direction. The Triac is controlled by an Opto-Triac by the CPLD. Since the maximum current output of the CPLD is under 4mA and the LED in the opto-triac requires at least 10mA, a transistor was used connected between the cathode of the LED and the ground, in order to control the LED with the CPLD output. A pull-down resistor is used at the base of the transistor in order to ensure that it will not be turned on by Electro Magnetic Interferences (EMI) since very little current is needed in the base in order to drive 10mA.

Also in order to by-pass the SM permanently with little losses a relay was also included in the design. Since the relay needs a high current on the control side to be driven, a Darlington transistor

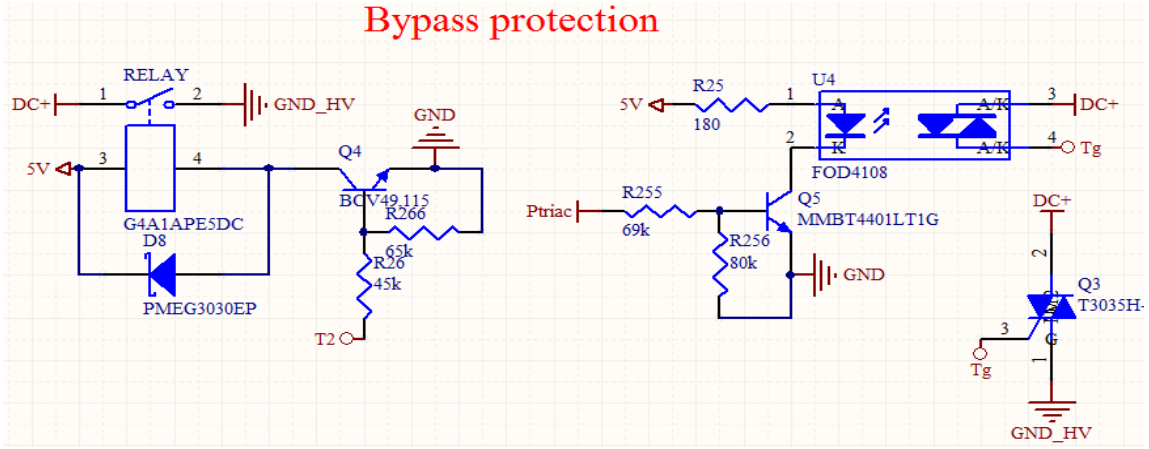


Figure B-16 – Protection & By-pass devices

with a gain of over 10.000 was used. This will allow the CPLD to drive it. An inrush current diode was placed in parallel to the relay, in order to protect the transistor from the high inrush current which will appear at the turn off of the relay, when the magnetic field collapses. As in the other transistor case, a pull-down resistor was used in order to ensure that the relay won't be accidentally turned on.

By design, the converter needs to be able to handle faults without being damaged. The most dangerous fault the converter can encounter is a short-circuit across the DC-link. At the instance of the fault, the current through the arm will increase rapidly, the only think limiting it being the arm inductors. Since the DC-link switches have a slow reaction time, by the time they open, the freewheeling diodes might be permanently damaged.

When a high-inrush current is detected by the current sensor, a fault signal will trigger the protection control in the CPLD, which will turn on the

B.7. Voltage supply

The developed SM PCB is composed of two areas: high voltage floating potential power layer and low voltage, no potential control area. The main supply of the board is 5V and on the control side, there are two power rails, 5V and 3.3V. In order to protect the electronics from fluctuation of the external power supply, over-voltage or inversing polarity of the supply, the circuit in Figure B-17 was used. The socket S1 is supplied from an external power supply, with a supply voltage in the range of $7.5\,V_{DC}$ to $8\,V_{DC}$. Diode D1 is a fast recovery Schottky diode, rated for 30V and 3A. It is placed there to ensure that if accidentally the polarity of the power supply is reversed, it will provide a conductive path and help protect the electronics on the board. Diode D2 is identical to D1 and its purpose is also to protect the board. In case of reverse polarity it will block the reversed voltage and together with D1 will protect the components. Diode D3 is an 8.2V Zener diode from ON SEMICONDUCTORS. In case the input voltage will be higher than 8.2V it will clamp it, and protect the voltage regulator from overheating due to the increased voltage. Although D3 will protect the voltage regulator from high voltages, but should only be used to avoid accidental over-voltages, as it is only rated for 1.5W.

The voltage regulator is an L78S05CV from STMicroelectronics in a TO-220 package. Its main advantages for its selection are [55]:

- Output current up to 2A;
- Thermal overload protection;
- Short circuit protection;
- Internal current limiting;
- Simple implementation with only 2 filtering capacitors.

In case of short-circuit across it pins, the L78S05CV will limit de current until the short circuit

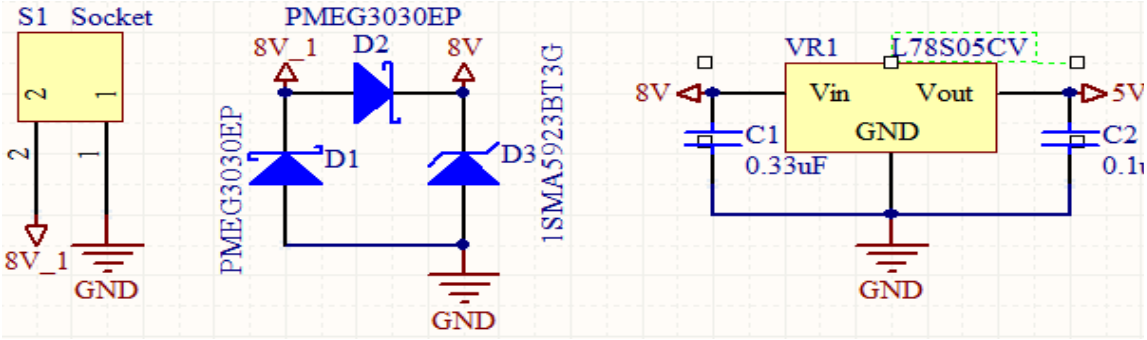


Figure B-17 – Power Supply

state disappears, while at the same time thermally protecting itself.

The CPLD and the muxifier require 3.3V supply. Although there was available space on the PCB for a 3.3V voltage regulator, the internal voltage regulators of the DSP and Piggyback were used. This was done due to the available power of the voltage regulators. The Piggyback can source up to 100mA from the 3.3V regulator can supply up to 100mA. Since each of the voltage regulators had sufficient surplus power to supply their own load and in order to avoid an extra power track on an already dens area of the PCB the 3.3V outputs of the two were not connected. The voltage regulator from the DSP supplies 3.3V to the CPLD and the oscillator. This current should be low, as the DSP only supplies logical signals across the board and its maximum source current is under 4mA. The 3.3V output from the piggyback will supply the LED muxifier.

B.8. Sub-module level Communication

Except for the two PWM lines, of which one is redundant, between the DSP and the CPLD are 6 connection lines used for simple communication between the two.

Two of the lines will be implemented to signal the CPLD the state of the EtherCAT communication, which will also be shown using two of the LEDs.

Two other lines will be used for the protection trigger and acknowledgement.

The fifth line will be used in the start-up procedure and the sixth one will be used in further developments.

The role of the communication lines will be further explained in the CPLD section.

B.9. CPLD and DSP

The low level control algorithm, including sinusoidal and triangular saw tooth signals and the EtherCAT slave code are implemented on a TMS320F28069 DSP based ControlStick from Texas Instruments [56]. The Deadtime and protection management are performed using a CPLD XC9572XL from Xilinx. The ControlStick has a fully embedded form factor shown in Figure B-18, and has the following features:

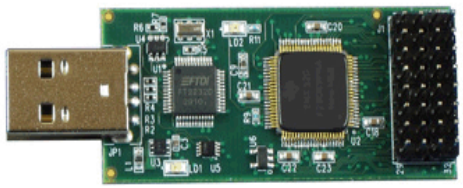


Figure B-18 – Piccolo F28069 ControlStick [56]

ControlStick Features

- Small USB drive like form factor;
- 32pins header for connection;
- Analog and Digital Inputs/Outputs (GPIOs);
- Built in USB JTAG interface;
- 3.3V output;
- 5V supply.

CPU Features:

- High Efficiency 90 MHz, 32 bit Floating point architecture;
- Harvard Bus Architecture;
- 256kB Flash memory and 100kB Random Access Memory (RAM);
- Watchdog Timer Module and three 32-bit Central Processing Unit (CPU);
- 12-bit ADC;
- 16 PWM channels with 8 enhanced PWM (ePWM);

- Two SPI modules;
- Real-time debugging via hardware.

The modulation strategy and the communication are implemented on the DSP based on the simulation model. The PWM is generated using one ePWM module. The analog signals from the capacitors voltage and current measurements are done using two ADC channels.

The connection lines of the Control stick are shown in Figure B-19.

The current measurement is done via channel 7 of the ADC, while the voltage is measured with channel 1.

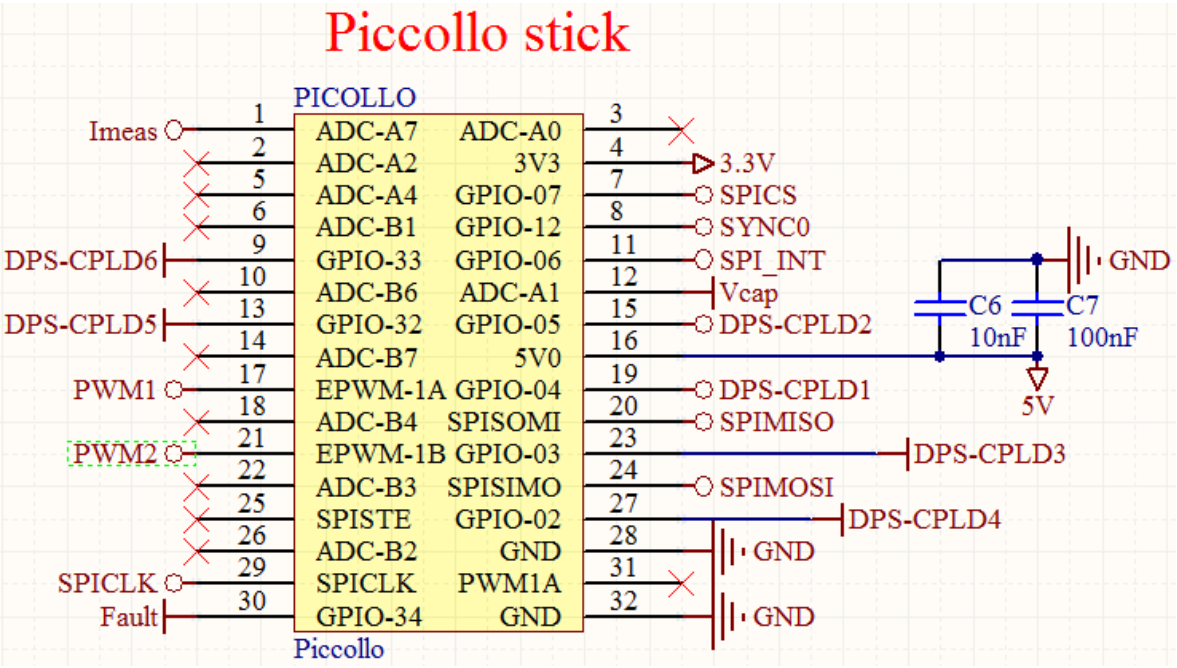


Figure B-19 – ControlStick connection header

On pin 16, power from the board is supplied via the 5V rail after being decoupled with an 10nF and an 100nF capacitors. Pin 4 will supply the 3.3V voltage to the CPLD.

The PWM is generated with the first ePWM module. Although complementary signals can be generated across pins 17 and 21 with deadtime, it was decided that a better approach would be to use a hardware based dead-time based on the signal of only pin 17. Pin 25 will instead be used to enable/disable the modulation, as the state of pin 17 will be transmitted to either the high or low gate inputs for the driver, depending on its logical value.

Pin 9, 13, 19, 21, 24 and 27 are reserved for the communication between the DSP and CPLD.

The SPI communication which is required for the EtherCAT interface is done using the SPI module A, but without using the hardware SPI CS pin (pin25). Instead, for more flexibility and control of the communication the SPI CS will be controlled by the software using the GPIO 7 (pin 7). Pins 8 and 11 are connected to the EtherCAT interrupt lines. This will be used to trigger the necessary procedure in the application layer of the communication.

SPI Implementation

The EtherCAT communication is passed to the DSP from the piggyback via SPI connection. SPI is a synchronous serial data link that operates as full-duplex (communication both ways at the same time). It is implemented as a master/slave communication, where the master device initiates the data exchange. Multiple slave devices can be on the same communication lines, but as it was initially designed, each slave should have a CS pin to inform it when the communication is addressed to him.

The communication lines are:

- CLK – which is the serial clock outputted by the master;
- MOSI – master out, slave input logic signal;
- MISO – master input, slave output logic signal;
- CS – chip select, logic signal to inform the slave when it is addressed.

When the communication starts, the master selects the slave device it wants to address and waits a predetermined amount of time, depending on the slave devices. After that the master will start an oscillating clock signal on the CLK line. During a clock cycle, a full data bit exchange occurs. The master will send a bit on the MOSI line, which will be read by the slave, on one of the clock signal transition and the slave will send a bit on the MISO pin, which the master will read, on the other transition from within clock signal. The transmission can be implemented without one of the two bit transporting lines, but this is not the case of this project.

There are 4 possible clocking schemes, generally named SPI mode 0 to mode 3. In order for the communication to work, both the master and the slave need to use the same mode. This are set by the clock polarity and the clock phase. The Clock polarity sets the active edge of the communication, either rising or falling for the master clock. The clock phase defines if there is a half-cycle delay of the clock. These two can be sued to set up the communication mode. In mode zero, the SPI master transmits on the falling edge of the CLK signal and receives data on the rising edge. In mode 1, the SPI transmits data one half-cycle ahead of the falling edge of the CLK and receives data on the falling edge of it. Mode 2 is defined as transmission of data on the rising edge of the CLK and receiving on the falling edge of it. The last mode transmits data one half-cycle ahead of the rising edge of the clock and receives data on the rising edge [57]. The modes are summarized in Table B-2.

Consulting [43] it was notice that the ET1000 can accept any of the four modes of SPI.

After selecting the SPI mode, the SPI speed needs to be decided. Consulting [57], the equation for the baud rate can be found as:

$$SPIBaudRate = \frac{LSPRCLK}{(SPIBRR + 1)} \tag{5.13}$$

where:

LSPCLK – Low-speed peripheral clock frequency of the device;

SPIBRR = clock divider used to set the SPI Speed.

For the F28069, the default low-speed peripheral clock frequency of the device is set to 22.5 MHz, but it can be changed in the configuration to be up to 90Mhz [56]. Assuming a peripheral clock of 90Mhz, the SPI Baud Rate can be set to 10Mhz (maximum for F28069 [56]) by setting the SPIBRR as:

$$SPIBRR = \frac{SLSPCLK}{SPIBaudRate} - 1 \tag{5.14}$$

Table B-2: SPI Clocking Scheme modes [57]

SPI mode	CLK Scheme	CLK Polarity	CLK Phase
Mode 0	Rising edge without delay	0	0
Mode 1	Rising edge with delay	0	1
Mode 2	Falling edge without delay	1	0
Mode 3	Falling edge with delay	1	1

The Xilinx XC9572XL used in the SM is shown in Figure B-20.

Figure B-20 – XC9572XL CPLD [63]

It presents the following features:

- 72 Macrocells;
- 35Mhz frequency;
- 1600 usable logical gates;
- 34 User definable I/Os;
- 3.3V supply/output with 5V input tolerance.

The tasks of the CPLD are:

- Deadtime management for the half-bridge;
- Stop the modulation in case of fault and by-pass the SM;
- Signal fault status.

When using a half bridge special care needs to be taken in order to avoid shoot through. The deadtime ensures that one Mosfet will have time to close before the other one is opened. The deadtime required delay with a safety margin of 20% can be calculated as:

$$t_{deadtime} = \left[\left(t_{d(OFF),\max} - t_{d(ON),\min}\right) + \left(t_{propagation,\max} - t_{propagation,\min}\right)\right] \cdot 1.2 \quad (5.15)$$

where:

$t_{d(OFF),\max}$ - maximum turn off delay time of the Mosfet;

$t_{d(ON),\min}$ - minimum turn on delay time of the Mosfet;

$t_{propagation,\max}$ - maximum propagation delay of the driving IC;

$t_{propagation,\min}$ - minimum propagation delay of the driving IC.

Since in [51] only the typical values are presented and as explained earlier, the gate resistors are bigger than required; the calculations will not be accurate. One could either calculate the new turn on time based on the new gate resistance or could be found by observing the turn on time of the Mosfets with the new gate resistors using an oscilloscope. In order to implement this, the calculation can be done using equation (5.15), and then the deadtime can be adjusted to ensure a good protection. By consulting [50] and [51] the turn on and of typical delays of the Mosfets and typical and maximum propagation delays can be introduced in equation (5.15) to obtain:

$$t_{deadtime} = \left[\left(202\,ns - 63\,ns\right) + \left(60\,ns - 30\,ns\right)\right] \cdot 1.2 = 202.8\,ns \quad (5.16)$$

Figure B-21 shows the gate signals of the Mosfets in the lower side and the Drain-Source Voltages in the upper side. The plot shows the turn off of the upper side Mosfet and turn on of the lower one. This plot was chosen as the upper Mosfet turn off much more slowly due to the higher gate resistances. This will ensure that there that the Mosfets won't be on at the same time, since the lower Mosfet operates much faster. The approximately deadtime which is short enough to be used is observed to be 3µS, this can't be perfectly tuned due to the frequency of the oscillating crystal used.

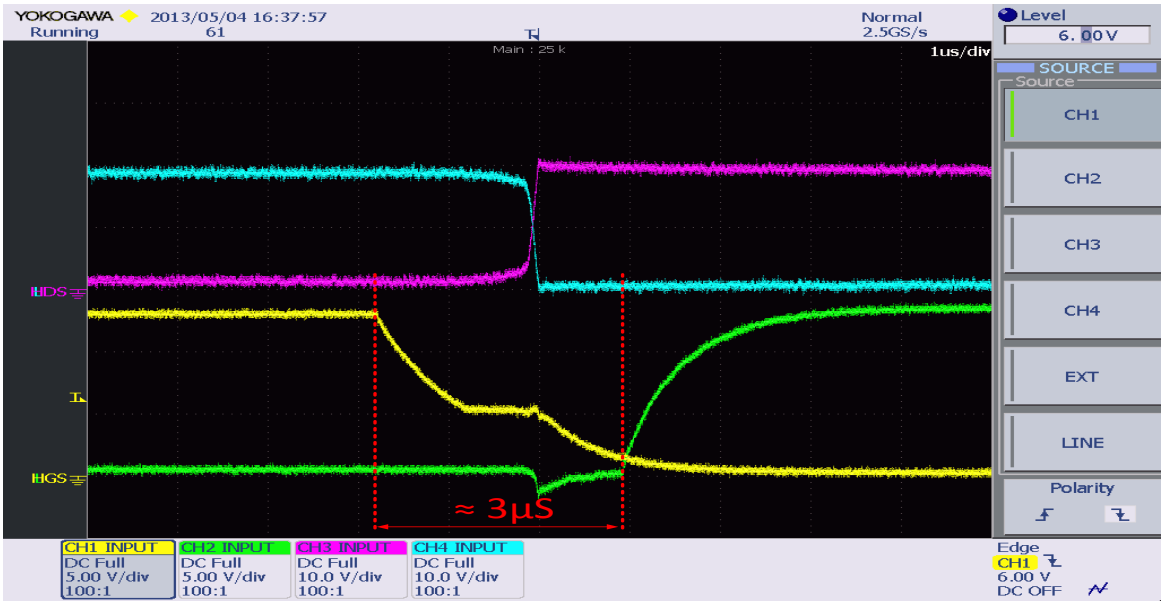


Figure B-21 – Gate signals acquired with oscilloscope. Yellow – Upper Gate Signal; Green – Lower Gate signal; Purple – High Side Drain-Source Voltage; Blue – Lower Side Drain-Voltage.

Different test have been run with the implemented deadtime in order to ensure proper operation. This will be detailed in the hardware validation part.

In order to provide feedback about the SM state, 8 LEDs are connected to the CPLD. Since the distance from the CPLD to the LEDs placement is long and passes through a signal dense area, a demultiplexer was used in order to control the LEDs with only 3 signal lines. The LEDs status are multiplexed in the CPLD and then sent to a CD74AC238 demultiplexer from Texas Instruments [58]. There is one extra LED to show that the SM is powered. Table B-3 shown the functions of the LEDs and their relative position.

The SM design also includes a button which will be used to trigger a fault signal on the SM.

Table B-3: SM LED Signals

LED1	LED2	LED3	LED4	LED5	LED6	LED7	LED8	LED9
GREEN	GREEN	RED	RED	RED	GREEN	GREEN	RED	GREEN
SM normal operation	Initialization	Overcurrent	Overvoltage	SM Trip	E2PROM loaded	EtherCAT Running	EtherCAT Error	SM Power

B.10. EtherCAT Communication

In order to facilitate the EtherCAT implementation with the ET1100 on SPI, Beckhoff provides a slave source code (SSC) generation tool [59]. This allows to easily generate a C code for the application layer which facilitates a simple variable exchange between master and slaves. The hardware dependent part of the code is normally generated for the PIC24 or PIC16 which can be found on Beckhoff EtherCAT development boards. This will have to be adapted to the F28069 DSP since the architecture and hardware control and initialization are different. The tool has many configuration options which are beyond the purpose of this project, and only the most important chosen ones will be discussed. Based on the selections done in the tool, a XML description file will also be created in order to be used with the master and also program the ESC EEPROM memory, so that the process exchange between the ESC and DSP can take place.

In the hardware section, the EL9800_HW switch is set to 1 in order to signal that the ET1100 PDI is set to SPI. The controller architecture switch is set to 32bit in order to optimize the code for it and the ESC access switch to 16bit. In order to use the signalling EtherCAT LEDs, the LED switch will be switch to 1.

In order to simplify the ESC Watchdog reset procedure, the timer switch is set to 1, since this can be implemented easier and much more accurate this way.

In the State Machine section, the bootstrap mode is disabled since it will not be used, and the process data switch is set to 1. This is a safety feature which will ensure that the SM will not switch from SAFEOP to OP mode if the process data exchange wasn't received. In this section also the timeouts of the communication can be set.

In the Synchronization section, the Al_Event switch is set to 1 in order to allow the ESC to use the SPI_INT line to trigger an interrupt in the DSP and at the same time create the interrupt routine in the C program. If this would not be activated, the DSP should pull the even register periodically. This might delay the communication speed if disabled. The DC_SUPPORTED switch will be set to 1, in order to activate the distributed clocks. The ECAT_TIMER switch set to 1 will create the interrupt routine which will allow the DSP to reset the watchdog.

In the Application section, the sample application switch is activated in order to include in the code source a simple 2 variable exchange between the master and the slave. In the process data sub-section the memory addresses and sizes for the input and outputs data in the ESC Memory are defined.

In the mailbox section all the switches are set to zero since the mailbox process will not be used. This way the code and the ESC description files will be simplified.

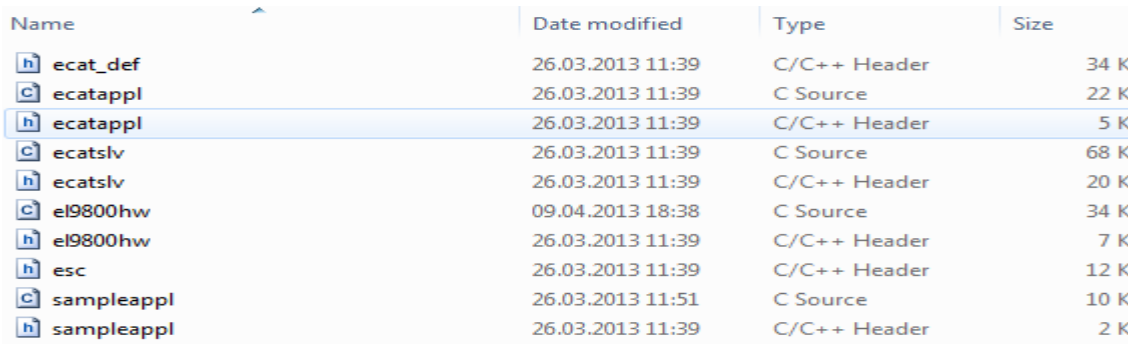
After defining the name of the slave board the SSC can be run to generate the necessary files. The output files from the generator are presented in Figure B-22. The ecat_def file contains all the definitions done in the SSC tool. The ecatappl.c is the main files of the source codes. This file handles all the different functions necessary for the communication. The ecatappl.h is the associated header with the file.

The ecatslv.c, and its header, is used for application interface, state machine and process data interface.

The el9800hw.c, and its header, is the hardware associated file. This handles the hardware initialization and testing and SPI communication.

The sampleappl.c file contains the hardware independent sample application. Here the SSC defined one input and one output variables which are exchanged with the master. Also in this file the different procedures for each state machine change can be defined.

The SPI communication is set for 8 bits per transmission. This means that multiple transmissions



Name	Date modified	Type	Size
ecat_def	26.03.2013 11:39	C/C++ Header	34 K
ecatappl	26.03.2013 11:39	C Source	22 K
ecatappl	26.03.2013 11:39	C/C++ Header	5 K
ecatslv	26.03.2013 11:39	C Source	68 K
ecatslv	26.03.2013 11:39	C/C++ Header	20 K
el9800hw	09.04.2013 18:38	C Source	34 K
el9800hw	26.03.2013 11:39	C/C++ Header	7 K
esc	26.03.2013 11:39	C/C++ Header	12 K
sampleappl	26.03.2013 11:51	C Source	10 K
sampleappl	26.03.2013 11:39	C/C++ Header	2 K

Figure B-22 – Files generated by the SSC for the project

are used for a variable transfer. The DSP will use two functions (one for reading, the other for writing) which split all the data into 8 bits packets. Whenever it want to read or write a variable, it should know the exact memory address where the ESC stores it. The first part of a read or write communication starts with the operation command (read/write) and is followed by the address where the data is stored, the read or write command and the data to be written or will send dump data in order to receive the data from the ESC.

When the SM is powered, the application code will first start initiating the hardware. The clock registers and all the GPIO pins, including the SPI registers, will be set. After this, the DSP will start a SPI communication to verify the SPI settings are correct. A fixed value will be sent on the SPI channel and then read back for confirmation.

After this, the DSP will put the ESC into INIT mode and a clock will trigger the communication very 50ms to reset the watchdog of the ESC. When the masters asks for a state change the DSP initializes the SyncManagers and then cycles waiting for the next state. At his point he will also receive interrupts on the SYNC0 lines to check for new communication data which should have a higher frequency than the timer interrupt. When he receive a request for the SAFEOP state, he checks the ESC for the size of the variables exchanged and then compares then with the ones he has, and if they do not match, he will send an error state back to the master and return to PREOP. If the check proves valid, he will acknowledge the SAFEOP state and continue the communication at the same pace triggered by the SYNC0 interrupt, but will neglect the data received from the master. When the OP state will be requested, he will send and read the data from the master and the main modulation code will be activated.

B.11. Power Tracks sizing

Before building the SM PCB, the current carrying capabilities of the tracks have to be calculated. The maximum current is dependent of the cross-section area of each track. Considering a track copper thickness of 70 µm, a maximum current on the power tracks of 16A and a maximum allowed temperature increase of the PCB track of 30˚C, the track width (w_{track}) in mils can be calculated as[60]:

$$w_{track} = \left(\frac{I}{k \cdot dT^{0.44}} \right)^{1.38} \cdot \frac{1}{h_{copper}} \tag{5.17}$$

where:

h_{copper} - copper thickness in µm;

k – constant for external (0.048) or internal (0.024) traces;

I – current on the track in Amps.

dT – allowed temperature increase over ambient.

Knowing that 1 mil = 0.0254mm, equation (5.17) can be manipulated to find the minimum track width in mm:

$$w_{track} = \left(\frac{I}{k \cdot dT^{0.44}} \right)^{1.38} \cdot \frac{0.0254^2}{h_{copper}} \cdot 1000 \tag{5.18}$$

Inputting all the data into the equations, one gets a minimum of 9.19mm internal trace and 3.53mm for the external one.

B.12. Cooling

In the converter design one important factor to consider is the thermal limitation of the semiconductor devices. The junction temperature of the devices of the switches must never exceed the maximum allowed temperature. Since the power transferred through the devices is considerable, a heatsink must be attached in order to dissipate the heat, which otherwise might destroy the silicon dye. The Fairchild devices have a good thermal performance, with a low on resistance and a big casing size to help dissipate the heat. By consulting [50] the maximum Source On-Resistance ($R_{DS(on)}$) is found to be 0.055Ω at a junction temperature of 25˚C. From Figure B-23 the Normalized On-Resistance coefficient, $K_{R_{DS(on)}}$ for 150˚C is obtained.

It was decided that the best option is to use the same heatsink for both devices, as they share the load uneven and the current through the devices is dependent on the capacitor unbalance. This way the thermal calculations can be done for only one device with the duty cycle of one, since both devices are switching complementary.

First the conduction losses have to be computed as:

$$P_{Conduction} = K_{R_{DS(on)}} \cdot R_{DS(on)} \cdot {I_{DS}}^2 \cdot d \tag{5.19}$$

Inputting all the values in the above equation, the conduction losses are calculated are found as 35.2W.

This are the most important losses in a low switching device, but the switching losses have to also be considered. These losses are dependent on the voltage across the device, the current through the device, the switching frequency and the turn-on and turn-off times of the device. It can be safely assumed that the devices switch on and off at the same rate since the gate capacitances are charged and discharged through the same resistor. A turn on time of 2µs will be taken, based on their gate resistance. The switching frequency will be 1kHz.

With all the values considered, the switching losses are found to be 3.2W, from:

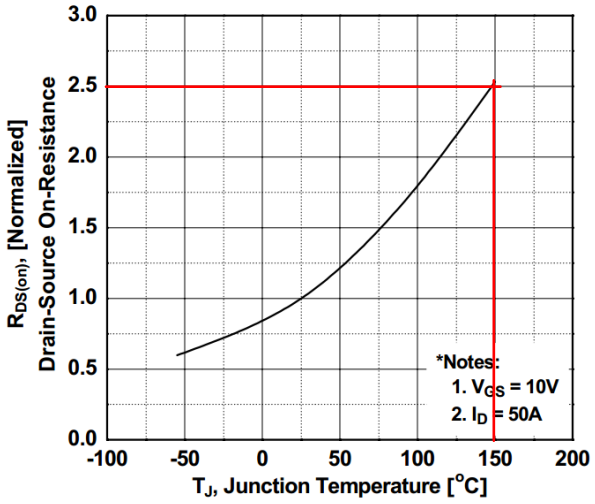


Figure B-23 – On-Resistance Variation vs. Temperature [50]

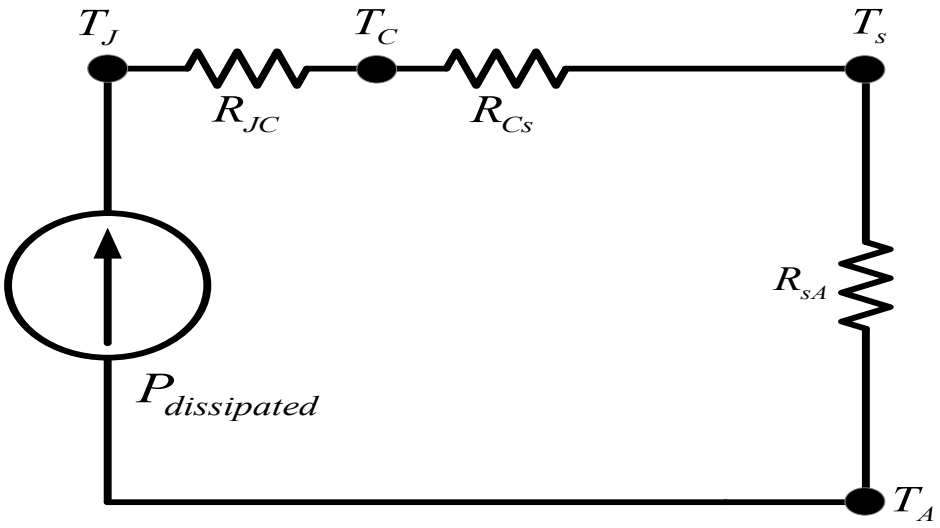


Figure B-24 – Thermal model

$$P_{switching} = \frac{V_{DS} \cdot f_s}{2} \cdot (t_{on} + t_{off}) \cdot I_{DS} \tag{5.20}$$

Thus, the total losses for the devices will be 38.4W:

$$P_{dissipated} = P_{Conduction} + P_{Switching} \tag{5.21}$$

In order to dissipate the heat, a heatsink needs to be attached to the two Mosfets. The dimensions of the heatsink can be calculated based on Figure B-24. T_J represents the junction temperature, T_C is the case temperature, T_s the heatsink temperature, T_A the ambient temperature, R_{JC} the Junction to Case thermal resistance, R_{Cs} the case to heatsink thermal resistance and R_{sA} the sink to ambient temperature. R_{JC} can be obtained by reading the device datasheet as maximum $0.5\,°C/W$. R_{Cs} is given by the bonding agent between the case and the heatsink. For this application, a fiberglass based Silicon insulation pad from Bergquist was used[61]. This pad was chosen since both devices have the drains connected to the case cooling plate. This way the devices can be insulated from each other and at the same time fill the gaps which might appear from small imperfections of the surfaces. The thermal resistance of the pad is $0.45\,°C/W$. The junction temperature, T_J, can be found in the Mosfets documentation as maximum $150\,°C$. For safety it will be assumed $120\,°C$.

Considering an ambient temperature of $25\,°C$, the maximum thermal resistance of the case, R_{sA}, can be calculated as:

$$R_{sA,\max} = \frac{T_J - T_A}{P_{dissipated}} - (R_{Jc} + R_{cA}) \tag{5.22}$$

Putting all the values in the equation, the maximum thermal resistance of the case is computed as $1.97\,°C/W$. For this application, a SK92-50-AL heatsink from Fischer Elektronik was selected[62]. From Figure B-25 the heatsink resistance for a length of 50mm can be found as $1.75\,°C/W$, which is smaller than the necessary one.

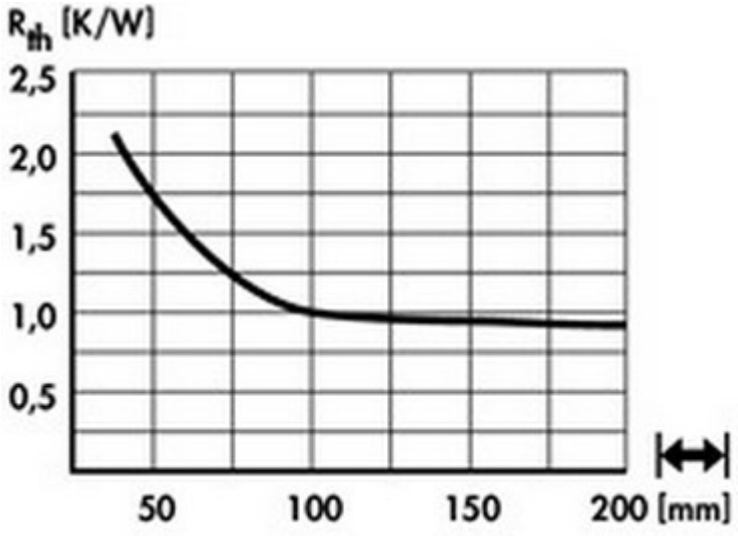


Figure B-25 – SK92 Thermal Resistance vs. length [62]

B.13. Hardware Validation

The SM design presented in this chapter has been built and tested in the laboratory, including the protections.

Dead-time

Before building the entire converter, the SM was tested to ensure proper operation. The dead-time between the half-bridge's switches was tested. The experimental result can be seen in Figure B-26. The yellow line shows the gate-source voltage across the upper Mosfet, the green line shows the gate-source voltage across the lower Mosfet. The purple and blue lines show the Drain-Source voltage for the upper, respectively lower Mosfets. The intersection of the Drain-Source voltages are due to the induction used for the test. The inductance limits the rapid current change and forces the diodes to conduct. The turning on of the diodes can be seen in the gate signals as a ripple.

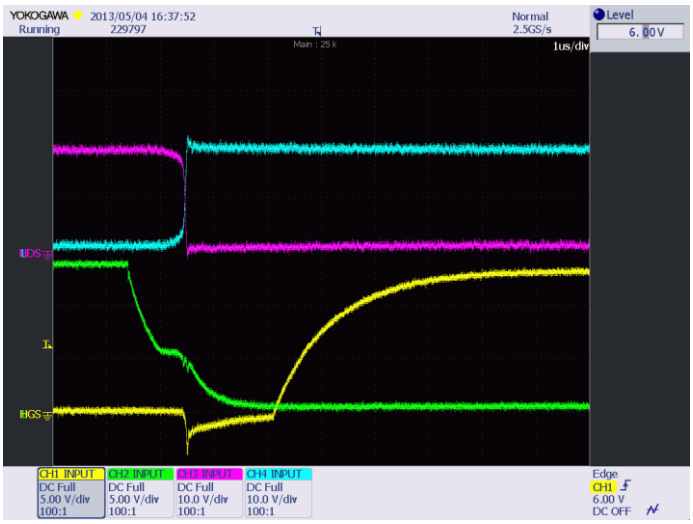


Figure B-26 – Dead-time implementation

Voltage measurements

The differential amplifier transfer ratio was obtained by varying the voltage across the capacitors and measuring the analog output. As with any analog circuit, noise will be present, but the mean ratio of the measurement is 0.015642, as expected based on equations (5.10) and (5.11). Figure B-27 show the measurement ratios and their mean. The biggest ratio appears during the first measurement, when the capacitor should be discharged, but considering it is only 0.04%, it can be ignored.

The current measurements are not required to be exact, since only the current direction needs to be identified. For this, only a basic check was done for this, and it will not be presented as it is not relevant.

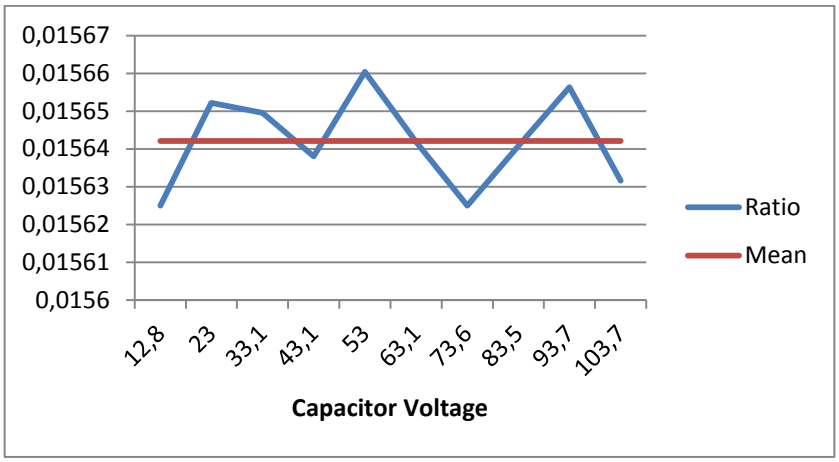


Figure B-27 – Voltage measurement ratio

Thermal Testing

In order to validate the efficiency and correct selection of the SM heatsink, a thermal test was done.

The SM was connected as a half-bridge to a DC laboratory power supply with an RL load. The SM was loaded with currents in steps of approximately 0.5A from 1A to 18.18A. Between each step, sufficient time was elapsed to allow the heatsink's temperature to stabilize. Figure B-29 shows the heatsink temperature in the hottest point plotted along the Power dissipated by the Mosfets and the current through the devices. The test was stopped at 90˚C since the current through the devices was 18A, much bigger than the designed current. Figure B-29 shows the infrared thermal picture of the SM after one hour and forty-five minutes at 18A. The hottest point of the heatsink is 91 ˚C and is marked with red.

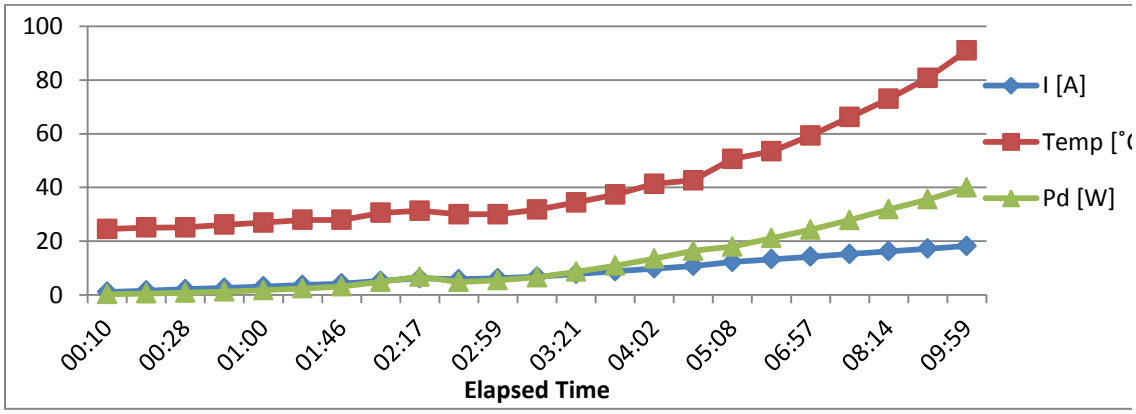


Figure B-28 – Current, Temperature and Power Dissipated

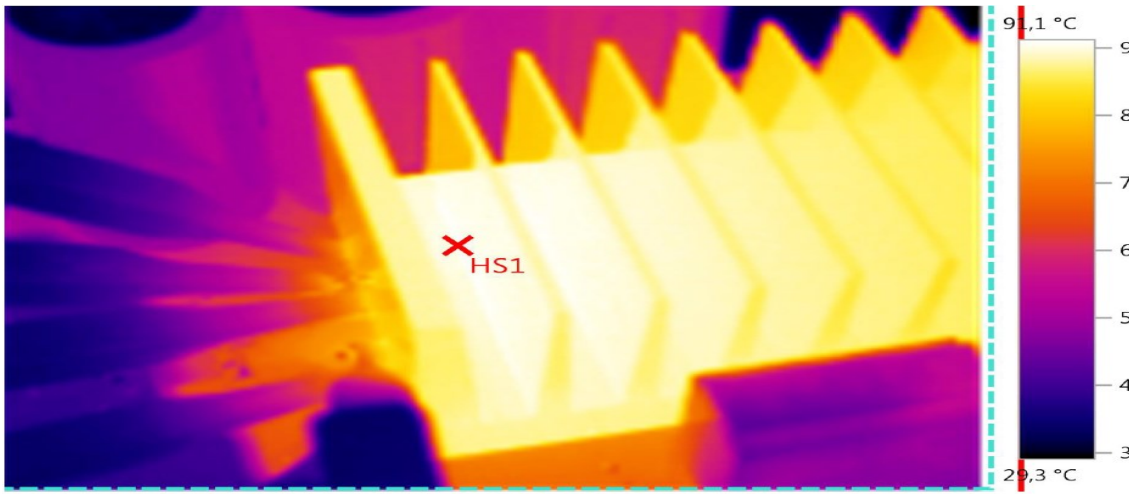


Figure B-29 – Thermal Picture of SM after 1:45hours at 18A

B.14. Summary

In this chapter, the SM prototype design was presented and detailed. The nominal voltage per SM was chosen to be 100V in order to cope with the available laboratory equipment. The maximum current of the SM (same as per arm) was chosen as 16A. The different components of the PCB were presented and their functionality and operation mode described. The driving circuit proved proper operation, as did the bootstrap supply circuit. The dead-time implementation appeared to function as desired, as did the protection devices. The heatsink proved to cool the devices sufficiently for proper operation.

The SM design proved to be correct and to operate as required, validating all the calculations, allowing for the rest of the SM to be built.

Appendix C – Simulation Code for the master control

Fortran subroutine

```
! ****************************************************
!           Subroutine for master control Emanuel-Petre Eni
! ****************************************************



      SUBROUTINE AUX_CBLCK_ONE(I1,I2,TIM,I3,I4,I5,I6,I7,I8,KP1,KP2,KI1,&
      KI2,T0,T1,T2,T3,T4,T5,IP,IN,BAL,VNOM,RAMP,KP11,KP22,KI11,KI22,&
      R,VCU,VCL,VAU,C1U,C2U,C3U,C4U,C1L,C2L,C3L,C4L)
      INCLUDE "nd.h"        ! dimensions
                            ! in the case of EMTDC with Digital Fortran 90
                            ! this file introduces the module NDDE with a array
                            ! E_NDIM which contains all the parameters
                            ! defining sizes of EMTDC matrixes and
                            ! arrays


      INCLUDE "emtstor.h"   ! arrays and indexes: STORx, NSTORx
                            ! in the case of EMTDC with Digital Fortarn 90
                            ! arrays STORx are dimentioning in the follwing way
                            !
                            ! logical - STORL(E_NIDM(27))
                            ! integer - STORI(E_NDIM(28))
                            ! real    - STORF(E_NDIM(29))
                            ! complex - STORC(E_NDIM(30))


      REAL I1,I2,TIM,I3,I4,I5,I6,I7,I8,KP1,KP2,KI1
      REAL KI2,T0,T1,T2,T3,T4,T5,IP,IN,BAL,VNOM,RAMP
      REAL KP11,KP22,KI11,KI22,R,VCU,VCL,VAU,C1U,C2U
      REAL C3U,C4U,C1L,C2L,C3L,C4L
```

```
      CALL TEST_CBLCK_ONE(I1,I2,TIM,I3,I4,I5,I6,I7,I8,KP1,KP2,KI1, &
      KI2,T0,T1,T2,T3,T4,T5,IP,IN,BAL,VNOM,RAMP,&
      KP11,KP22,KI11,KI22,R,VCU,VCL,VAU,C1U,C2U,&
      C3U,C4U,C1L,C2L,C3L,C4L,NSTORF,STORF)



      END
```

C code subroutine

```
    /*/ ****************************************
    Master Control for MMC single phase for 8 SM

    ////////////////////////////////////////
    ////////////////////////////////////////*/
    void test_cblck_one_(double *deb, double *in1, double *in2, double *tim, double
*in3, double *in4, double *in5, double *in6, double *in7, double *in8, double
*kp1,double *kp2,double *ki1,double *ki2, double *t0, double *t1, double *t2, double
*t3, double *t4, double *t5, double *ip, double *in, double *bal, double *vnom, double
*ramp, double *kp11, double *kp22, double *ki11, double *ki22, double *r, double
*vcnu,double *vcnl,double *vau, double *van,double *mu,double *ml,double *c1u, double
*c2u, double *c3u, double *c4u, double *c1l, double *c2l, double *c3l, double *c4l,
int *nstor_f, double stor_f[])
    {
   int stor=30.0; // storage space
   double mod=8.0; // number of modules
   double inputs[8]; //inputs array
   double outputs[8];
   double carriers[7];
   double mud=mod/2.0;

   int i;
   int z=4.0;
   double stg=0.0;
   double rdy=0.0;
   double vlim1=0.0488;
   double vlim2=*vnom;
   double avg=0.0;
   double avgu=0.0;
   double avgl=0.0;
   double timer;
   double vset=*vnom;
   double k1=*kp1;
   double k2=*kp2;
   double k3=*ki1;
   double k4=*ki2;
   double k11=*kp11;
```

```
double k22=*kp22;
double k33=*ki11;
double k44=*ki22;
double rr=*ramp;
double Last_error1=0;
double Last_error2=0;
double Last_error11=0;
double Last_error22=0;
double P1;
double P2;
double I1;
double I2;
double P11;
double P22;
double I11;
double I22;
double last_timer=0;
double dt;
double error1=0;
double error2=0;
double error11=0;
double error22=0;
double Iavg;
double vcu;
double vcl;
double vcn;
double output1;
double output11;
double u=4.0;
double l=4.0;
double fu=0.0;
double fl=0.0;



stg=stor_f[*nstor_f+stor-1];
rdy=stor_f[*nstor_f+stor-2];
timer=stor_f[*nstor_f+stor-3];
Last_error1=stor_f[*nstor_f+stor-5];
Last_error2=stor_f[*nstor_f+stor-6];
last_timer=stor_f[*nstor_f+stor-7];
Last_error11=stor_f[*nstor_f+stor-8];
Last_error22=stor_f[*nstor_f+stor-9];


dt= *tim - last_timer;
Iavg=(*ip + *in)/2;




inputs[0]=*in1;
inputs[1]=*in2;
inputs[2]=*in3;
inputs[3]=*in4;
inputs[4]=*in5;
inputs[5]=*in6;
inputs[6]=*in7;
inputs[7]=*in8;
carriers[0]=*t0;
carriers[1]=*t1;
carriers[2]=*t2;
```

```
carriers[3]=*t3;
carriers[4]=*t0;
carriers[5]=*t4;
carriers[6]=*t5;
carriers[7]=*t0;
*vau=0.0;
*van=0.0;


for(i=0.0;i<mod;i++)

    avg=avg+inputs[i];

avg=avg/mod;
vcn=avg;
vcu=avg;

for(i=0.0;i<mod/2;i++)
{
    if(inputs[i] < (vcu/2))
           fu=fu+1.0;
    avgu=avgu+inputs[i];

}
for(i=4.0;i<mod;i++)
{
    if(inputs[i]<(vcu/2))
           fl+=1.0;
    avgl=avgl+inputs[i];

}
if(fu != 1.0)
{
    vcu=vset;
    avgu=avg;
for(i=0.0;i<mod/2;i++)
    outputs[i]=carriers[i];

}
else
{
    for(i=0.0;i<mod/2;i++)
                  if(inputs[i]>vcu/2)
                  {
                         outputs[i]=carriers[z];
                         z=z+1.0;
                  }
                  vcu=vset*4/3;
                  //avgu=avg*4.0/3.0;
                  u=u-1.0;
                  *deb=z;
}
z=4.0;
if(fl != 1.0)
{
    vcl=vset;
    avgl=avg;
    for(i=4.0;i<mod;i++)
           outputs[i]=carriers[i-4];

}
else
```

```
{
                for(i=4.0;i<mod;i++)
            if(inputs[i]>vcn/2)
                {
                       outputs[i]=carriers[z];
                       z=z+1.0;
                }
                vcl=vset*4.0/3.0;
                l=l-1.0;
                //avgl=4.0/3.0*avg;


}
```

```
if (avg<vlim1 && stg==0.0)
{
    rdy=0.0;
    vset=avg;
    vcu=vset;
    vcl=vcu;

}

if (avg>=vlim1 && stg==0.0)
  {
      stg=1.0;
      timer=*tim;
  }
if (stg==1.0 && *tim-timer>0.005)
{
    if (stg==1.0)
           {
                  rdy=1.0;
                  vcn=vlim1+rr*(*tim-timer-0.005);
                  error1=vcn-avg;
                  P1=error1 * k1;
                  I1=k3 * (error1+Last_error1)*dt;
                  output1=P1+I1;
                  error2=Iavg-output1;
                  P2=error2 * k2;
                  I2=k4 * (error2+Last_error2)*dt;
                  *vau=P2+I2;
                  *van=*vau;
                  vcu=vcn;
                  vcl=vcu;

    }
}
else
    if(stg==1 && *tim-timer<0.005)
    {
           rdy=0.0;
                  vcu=vlim1;
                  vcl=vcu;
```

```
  }
if (stg==1.0 && vcn>=vlim2)
{
    stg=2.0;

}
if (stg==2.0)
{
    rdy=1.0;

                error1=vcn-avg;
                P1=error1 * k11;
                I1=k33 * (error1+Last_error1)*dt;
                output1=P1+I1;
                error2=Iavg-output1;
                P2=error2 * k22;
                I2=k44 * (error2+Last_error2)*dt;
                *vau=P2+I2;

                error11=vcl-avgl;
                P11=error11 * k11;
                I11=k33 * (error11+Last_error11)*dt;
                output11=P11+I11;
                error22=Iavg-output11;
                P22=error22 * k22;
                I22=k44 * (error22+Last_error22)*dt;
                *van=P2+I2;



}

   *vcnu=vcu;
   *vcnl=vcl;




*c1u=outputs[0];
*c2u=outputs[1];
*c3u=outputs[2];
*c4u=outputs[3];
*c1l=outputs[4];
*c2l=outputs[5];
*c3l=outputs[6];
*c4l=outputs[7];
if(*bal ==0.0)
{
rdy=2.0;
}
*mu=u;
*ml=l;
*r =rdy;
// save variables for next run

stor_f[*nstor_f+stor-1]=stg;
stor_f[*nstor_f+stor-2]=rdy;
stor_f[*nstor_f+stor-3]=timer;
stor_f[*nstor_f+stor-5]=error1;
stor_f[*nstor_f+stor-6]=error2;
```

```
   stor_f[*nstor_f+stor-7]=*tim;
   stor_f[*nstor_f+stor-8]=error11;
   stor_f[*nstor_f+stor-9]=error22;

   *nstor_f = *nstor_f + stor; //increase array pointed at the end of routine

   }

   /*****************************************************
   *SM controller By Emanuel-Petre Eni @ AAU
   *****************************************************/

   void sm_ctrl_(double* sin, double* vnom, double* va, double* triang, double* mod,
double* dc, double* ctrl, double* i, double* vcap, double* ovl, double* ocl, double*
kp, double* vcapout, double* error, int* hg, int* lg,double* s)

     {
          int k = 0.0;
          double vb;
          double scaler;
          double fref;

          *vcapout = *vcap;

          //P controller
          *error = *vnom - *vcap;
          if(*i >= 0)
                 k = 1.0;
          else
                 k = -1.0;
          vb = *error * k * *kp;

          //new reference creation
          scaler = *dc / *mod;
          fref = (*va + vb - *sin * scaler) / scaler;
          *s=fref;
          //SM dissabling protection

          if ((*i * *i) > *ocl)
          {
   fref=2.0;
          }



          //external short circuit protection
          if (*vcap > *ovl)
          {
   fref=-1.0;
          }



          //comparator
          if (fref > *triang)
          {
                 *hg=1.0;
                 *lg=0.0;
          }
          else
          {
                 *hg=0.0;
```

```
                *lg=1.0;
        }


        //internal fault protection
        if(*ctrl == 1.0)
                if (*vcap < (*vnom/6))
                {
                        *hg=0.0;
                        *lg=1.0;
                        *error=0.0;
                        *vcapout =0.0;
                }
      if(*ctrl < 1.0)
      {
                        *hg=1.0;
                        *lg=0.0;
                        *error=0.0;
      }

      if(*ctrl == 2.0)
      {
                        if (fref > *sin)
                        {
                                *hg=1.0;
                                *lg=0.0;
                        }
                        else
                       {
                                *hg=0.0;
                                *lg=1.0;
                        }
      }


}


/*****************************
DC-protection function
*****************************/
void dc_prot_(int* trigger, double* cp, double* ip, double* in)
  {
        if(*ip > *cp)
                *trigger=1.0;
        else
                if (*in > *cp)
                        *trigger=1.0;
                else
                        *trigger=0.0;

  }
```

Appendix D – Bill of materials

Description	Designator	Footprint	Quantity	Value	Comment	Order Code	Link (supplier)	Price	Total	Order amount	Total per order
Capacitor	C1	c0805	1	0.33uF	Cap	652-0982	RS	1,76	1,76	11	19,36
Capacitor	C2,C3, C7, C8, C12, C14, C16, C19, C21, C23, C26, C27, C29, C32,C34, C35, Co7	c0805	17	100nF	Cap	648-0979	RS	0,113	1,921	177	20,00
Capacitor	C4, C33	c0805	2	1uF	Cap	653-0490	RS	0,418	0,836	21	8,78
Capacitor	C5	c0805	1	10uF	Cap	691-1161	RS	1,257	1,257	11	13,83
Capacitor	C6, C13, C15, C18, C20, C22, C24, C30, C36, Co6	c0805	10	10nF	Cap	264-4371	RS	0,274	2,74	104	28,50
Capacitor	C9	c0805	1	220pF	Cap	264-4309	RS	0,482	0,482	11	5,30
Capacitor	C10, C11	c0805	2	68pF	Cap	698-4112	RS	3,342	6,684	21	70,18
Capacitor	C17	c0805	1	15nF	Cap	147-443	RS	0,117	0,117	11	1,29
CL43B106KALNNNF	C25	c1812	1	4,7uF	Bootstrap Cap	741-6821	RS	7,458	7,458	11	82,04
Capacitor	C28	C1210_L	1	100nF	Cap	499-7526	RS	3,423	3,423	11	37,65
Capacitor	C31	c0805	1	NP	Cap				0	11	0,00
Capacitor	C37	c0805	1	180pF	Cap	723-6221	RS	0,268	0,268	11	2,95
SM Capacitor	CC1, CC2, CC3, CC4	capacitor 20*50	4	1500uF	EETEE2D152KJ	1828631	Farnell	52,05	208,2	36	1873,80
1206CC103KAT1A	Cd	C1206	1		1206CC103KAT1A	391-090	RS	2,125	2,125	11	23,38
Schottky Diode	D1, D2, D8	SOD-128	3		PMEG3030EP	1829195	Farnell	kr. 2,45	7,35	32	78,40
Zener Diode	D3	sma	1		1SMA5923BT3G	1431145RL	Farnell	kr. 1,50	1,5	11	16,50
Default Diode	D4, D5	C1206	2		TS4148	652-6003	RS	0,224	0,448	21	4,70
Halfbridge IGBT module	D6	SOT-23B_M	1		BAT54SLT1G	9801510	Farnell	0,64	0,64	11	7,04
STPS3150RL	D7	do-214aa	1		MUR120S R5	4085108	Farnell	kr. 2,12	2,12	11	23,32
Module itnerconnection	DC	Socket - DC	1		20020110-H021A01LF	707-5458	RS	kr. 1,94	1,94	11	21,34
MER1S0512SC	DC/DC	'NMK0512SAC	1		NMK0512SAC	1560022	Farnell	59,04	59,04	15	885,60

5988210107F	E2PROM, ECAT, Init, PWR, Run	3.2X1.6X1.1	5		5988210107F	1466000	Farnell	1,39	6,95	52	72,28
5988270107F	EC Err, OC, OV, Trip	3.2X1.6X1.1	4		5988270107F	1465997	Farnell	1,7	6,8	42	71,40
Ethercat Controller	FB1111-0141	Piggiback	1		Header 26*2				0	11	0,00
Header, 6-Pin	Jtag	HDR1X6	1		Header 6				0	11	0,00
Osc	Osc	Osc16	1		7W-35.328MBB-T	1842129RL	Farnell	kr. 5,58	5,58	11	61,38
PICCOLO STICK SOCKET 2X8HEADER X2	PICOLLO	PICOLLO	2		87606-308LF	649-87606-308LF	Mouser	kr. 16,41	32,82	21	344,61
FDL100N50F	Q1,Q2	TO-264	2		FDL100N50F	759-9128	RS	108,35	216,7	21	2275,35
Silicon Bidirectional Triode Thyristor	Q3	TO-220	1		T3035H-6T	1889346	Farnell	kr. 13,01	13,01	11	143,11
darlington-transistors	Q4	sot89	1		BCV49,115	BCV49,115	RS	2,647	2,647	11	29,12
NPN Bipolar Transistor	Q5	SOT-23B_N	1		MMBT4401LT1G	545-0371	RS	0,0336	0,0336	11	0,37
Resistor	R1	J1-0603	1	680	CRG0603F680R	213-2244	RS	0,067	0,067	11	0,74
Resistor	R2, R3, R4, R401, R402, R403, R404, R405	J1-0603	8	220	CR0603-FX-2200ELF	740-8842	RS	0,112	0,896	84	9,41
Resistor	R10, R15	J1-0603	2	270K	CRCW0603270KFKEA	679-0077	RS	0,104	0,208	21	2,18
Resistor	R5	J1-0603	1	2,4k	**ERJP03F2401V**	**721-7371**	RS	0,82	0,82	11	9,02
Resistor	R11, R12, R13, R14, R16, R17, R18, R19	J1-0603	8	560K	CRCW0603560KFKEA	679-0532	Rs	kr. 0,09	0,712	84	7,48
Resistor	R6, R7	J1-0603	2	15k	**ERJP03F1502V**	**721-7432**	RS	0,82	1,64	21	17,22
Resistor	R8	J1-0603	1	13k	**ERJP03F1302V**	**721-7438**	RS	0,82	0,82	11	9,02
Resistor	R9, R20	J1-0603	2	10k	CR0603-FX-1002HLF	740-8808	RS	0,127	0,254	21	2,67
Dead time resistor	R21	J1-0603	1	NP	ERJP14F1500U	721-8090	RS	1,656	1,656	11	18,22
Resistor	R22, R23	14-1210	2	30	ERJP14F30R0U	721-8025	RS	1,656	3,312	21	34,78
Resistor	R24	j1-0603	1	160k	CRCW0603160KFKEA	678-9803	RS	0,112	0,112	11	1,23
Resistor	R25	J1-0603	1	180	CRG0603F180R	213-2171	RS	0,0678	0,0678	11	0,75
Resistor	R26	J1-0603	1	45k	ACPP0603180RBE	668-8328	RS	2,492	2,492	11	27,41
Resistor	R27	J1-0603	1	18k	CRG0603F18K	213-2446	RS	0,067	0,067	11	0,74
Resistor	R28	J1-0603	1	110k	CRCW0603110KFKEA	678-9699	RS	0,104	0,104	11	1,14
Resistor	R31	2512	1	100k	352182KFT	755-1413	RS	1,812	1,812	11	19,93

Resistor	R255, R266	J1-0603	2	69k	CRCW060369K8FKEA	679-0658	RS	0,112	0,224	21	2,35
Resistor	R256	J1-0603	1	80k	CRCW060380K6FKEA	679-0712	RS	0,104	0,104	11	1,14
Single-Pole Single-Throw Relay	RELAY	relay2	1		G4A1APE5DC	2213775	Farnell	22,25	22,25	15	333,75
Halfbridge IGBT module	Reset	Push_Button	1		SK25GB	1550258	Farnell	8,29	8,29	11	91,19
5V power supply board	S1	Socket	1		20020110-C021A01LF	707-5098	RS	kr. 1,79	1,79	11	19,69
Differential comparator 1 input	U1	8msop	1		AD8276	2102536	Farnell	13,43	13,43	11	147,73
LM2904DT	U2	so-8	1		LM2904DT	714-0767	RS	1,752	1,752	11	19,27
Mosfet driver with internal insulation	U3	soic16w	1		SI8233BB-C-IS	753-2113	RS	23,49	23,49	11	258,39
Opto-Triac	U4	DIP6	1		FOD4108	739-4967	RS	50,71	50,71	11	557,81
ACS709	U5	qsop24	1		ACS709	724-8723	RS	32,96	32,96	11	362,56
Muxifier	U6	SOIC16_M	1		SN74LVC138ADRG4	**662-6908**	RS	2,834	2,834	11	31,17
Voltage Regulator	VR1	to-220	1		L78S05CV	714-7780	RS	3,52	3,52	11	38,72
XC9536	XC9536	PLCC-44M	1		XC9536	1193228	Farnell	11,83	11,83	11	130,13
Receptacle MALE	Socket DC	Socket DC	1		20020006-H021B01LF	707-5391	Rs	kr. 5,97	5,966	11	65,63
Receptacle MALE	Socket Power	Socket Power	1		20020004-C021B01LF	707-5032	RS	kr. 5,97	5,966	11	65,63
Heatsink			1		**SK100-75-SA**	**189-8088**	RS	73,9	73,9	3	221,7
Solder paste						321F54210D	Hinonline		0	0	0

Appendix E – Sub-Module Schematic