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Title:	[Thermoel	ectric Modeling of IGBT Modules for Transient Operation]	
Semester:	[10 th Seme	[10 th Semester, February 2013]	
Semester theme:	[Master T	[Master Thesis]	
Project period:	[1 Septem]	[1 September 2012 – 30 May 2013]	
ECTS:		[50]	
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Project group:		[PED4 - 1043]	
		SYNOPSIS: In order to avoid destruction of braking chopper IGBTs, the need of information about instantaneous junction temperature arises. As the operation regime is transient, there is interest of having developed a technique that will allow wind turbine inverter	
Ovidiu Nicolae Faur		manufacturers to limit the number of paralleled transistors as much as possible, while avoiding physical destruction and keeping the ability of fault ride-through for same period of time. This project proposes a novel electro-thermal model for the braking chopper used in wind turbine converters. The thermal model is realized as a ladder network, for better accuracy. Using thermal information provided by it, the model is developed to emulate dynamic changes in collector- emitter voltage drop. A test setup is proposed in order to	
Copies:	[]	reproduce the operating conditions of a braking chopper used in a real field wind turbine application. Electrical	
Pages, total:	[]	devices dimensioning, cooling system design, control and	
Appendix:	[]	control PCB is designed by taking into consideration that	
Supplements:	[1 CD]	the system must be self-protective. As final purpose, a simple and accurate estimator for junction temperature is	

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By signing this document, each member of the group confirms that all group members have participated in the project work, and thereby all members are collectively liable for the contents of the report. Furthermore, all group members confirm that the report does not include plagiarism.

and collector-emitter voltage drop.

realized and presented. The main advantage of the estimator is that it uses only electric measurements – collector current

PREFACE

The present project was conducted by group PED4 -1043 during 9th and 10th Semesters at the Department of Energy Technology from Aalborg University. The work was carried out between the 1st of September 2012 and 30th of May, 2013.

Reading Instructions

The references are shown as numbers between square brackets. Detailed information about the works cited is presented in the References. The numbering of equations is of form (X.Y), where X is the chapter number and Y represents the number of the entry in the chapter. Figures and tables are numbered on the format X-Y, with the same meanings for X and Y.

Lists of figures and tables presented in the report are presented in the beginning, in order to easily find information about the existing data. Also a nomenclature with the used abbreviations is presented in the beginning of the report.

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Aalborg, 30th of May, 2013 Ovidiu Nicolae Faur

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NOMENCLATURE

ADC	Analog to Digital Converter
AC	Alternative Current
DC	Direct Current
DCB	Direct Copper Bond
DUT	Device Under Test
ENTSO-E	The European Network of Transmission System Operators for Electricity
FLIR	Forward Looking Infrared
FRT	Fault Ride Through
HVRT	High Voltage Ride Through
IGBT	Insulated Gate Bipolar Transistor
LVRT	Low Voltage Ride Through
MOS	Metal Oxide Semiconductor
Op-Amp	Operational Amplifier
PCB	Printed Circuit Board
RMS	Root Mean Square
VCE	Collector Emitter Voltage
VLT	Registered Mark for Danfoss Frequency Converter Series

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1. INTRODUCTION

This chapter presents the evolution of the wind energy in Europe, from the point where it was considered only as a negative consumer, to the stage of being an important player on the energy market. The constraints applied to grid connection of wind turbines and their consequences on the inverter topology are reviewed shortly, with a larger focus on voltage regulation. In the following, the need for a braking chopper and thermal monitoring of it is explained. The third and fourth sections present an overview of the failure mechanisms in Insulated Gate Bipolar Transistors (IGBTs) and temperature modelling techniques for power electronics. The chapter ends with a brief outline of the report.

1.1. BACKGROUND

Over the last 30 years, the wind energy sector has evolved from a negligible alternative solution to a major industry. The installed wind power capacity in Europe has grown from 100 [MW] in 1982 to 96.6 [GW] in 2012. The countries with the highest amount of installed wind power are Germany (29.06 [GW]), Spain (21.674 [GW]), France (6.8G [W]), Italy (6.75 [GW]) and United Kingdom (6.54 [GW]). Denmark is the seventh country with respect to the amount of installed wind power, having a total installed wind power of 3.871 [GW]. [3]

1.1.1. TRENDS IN WIND POWER

Presently, wind turbines represent a market share of 6.5% from total energy production in Europe, and it is predicted that it will grow to 14% in 2020 [4]. This growth is justified by both the increase in energy consumption and decommissioning of non-renewable energy production. Figure 1-1 shows the evolution of newly installed power generation capacity per year and the market shares of different adopted solutions, in Europe.



Figure 1-1. Evolution of Energy Production Growth in Europe [5]

The power ratings of wind turbines have also increased drastically, from up to 50 [kW] in 1985 to 7 [MW] in 2009 [6]. In 2012, the world leader in wind turbine manufacturing, Vestas, has designed the 8 [MW] wind turbine dedicated for off-shore and large scale wind power plants [7].

This rapid growth in power ratings has been fuelled by the technological advances. The introduction of variable speed and variable pitch wind turbines with synchronous generators lead to introduction of larger power turbines. After the development of doubly-fed induction generators for wind turbines the viability studies concluded that wind turbines can be developed for up to 20 [MW]. Figure 1-2 presents the general structure of a wind turbine. [3], [4]



Figure 1-2. Wind Turbine Structure [8]

1.1.2. Grid Codes Requirements

The continuous growth of installed wind power led the system operators to impose strict regulations on the wind energy distributed generation units in order to keep in safe limits the operation, stability and security of the grid. Present grid codes require renewable sources to behave as much as possible like conventional power plants from the grid services perspective. Wind power plants are required to provide similar services in terms of grid support, power quality, and dynamic support and avoidance of disconnection during faulty operation. [9]

The European Network of Transmission System Operators for Electricity (ENTSO-E) defined a series of regulations that are applicable to all grid connected generator units, regardless of voltage levels that they are connected to. The plants have the following operation requirements: [10]

- *System management*: production units should perform security analysis for present and forecasted situations, availability analysis in power production and ancillary services, information about temporary limitation, or to perform scheduled actions;
- *Frequency stability*: power plants should provide the necessary control in order to keep the demand and generation in balance;
- *Voltage stability*: network operators have to advise the power production units to supply reactive power in order to keep the voltage profile in balance;
- *System robustness*: power plants have to be robust in case of any perturbation in the power system;

• *System restoration*: after a disturbance the power plant has to restore the voltage after a blackout or to operate in voltage control mode if it is technically feasible.

The typical features that are generally defined in grid codes for wind turbines are: [8]

- Voltage Ride-Through, both for sags (Low Voltage Ride-Through LVRT) and swells (High Voltage Ride Through – HVRT) of different magnitudes are defined, as a demand for WTs to withstand without disconnection for certain periods of time for different magnitudes;
- P and Q limits during fault and recovery;
- Reactive Current Injection for voltage support during fault and recovery;
- Active Power Restoration with limited ramp, during fault recovery.

The standard for voltage stability imposed by the Danish transmission system operator Energinet.dk is presented in the following. The standard refers to wind turbines connected to grid voltage above 100 [kV], and was published by Elkraft System and Eltra in 2004. [1]

As it can be observed in Figure 1-3, a wind turbine must be able to operate without power reduction for small variations in the grid frequency (49.5 [Hz] to 50.5 [Hz] is considered to be the normal operation margins) and for variations of the grid voltage between limits defined as full load upper voltage U_{HF} – for voltages above nominal, and full load under voltage U_{LF} – for voltages below nominal value. Over these limits, the constraints refer to the time necessary to operate without power reduction, and the accepted reductions after the indicated period of time. [1]

The voltage limits are defined for different voltage levels, according to Table 1-1.



Figure 1-3. Dimensioning Voltages and Frequencies for Wind Turbines Connected to Danish Grid [1]

Nominal Voltage,	Lower Voltage	Lower Voltage	Upper Voltage	Upper Voltage
U_N	Limit, U _L	Limit for Full-	Limit for Full-	Limit, U _H
		Load Range, U _{LF}	Load Range, U _{HF}	
400 [kV]	320 [kV]	360 [kV]	420 [kV]	440 [kV]
150 [kV]	135 [kV]	146 [kV]	170 [kV]	180 [kV]
132 [kV]	119 [kV]	125 [kV]	145 [kV]	155 [kV]

Table 1-1. Voltages and Voltage Limits in the Transmission Grid [1]

Another aspect imposed for wind power plants is to remain connected after short circuit faults. Three-phase short circuits for up to 100 [ms], two-phase short circuits of 100 [ms] followed by another short circuit after 300-500 [ms] with a duration of also 100 [ms] and single phase short circuit to earth of 100 [ms] with 300-500 [ms] time between shall be withstood by the wind farms along with its compensation plants. [1]

1.1.3. MOTIVATION

Due to recent renewable power instalments, grid codes have been changed and presently request from energy producers the capability of Fault Ride-Through (FRT). During this transient state, the entire mechanism of a wind turbine is subjected to increased mechanical and electrical stresses.

Given the fact that the electric system presents the highest failure rate in a wind turbine (Figure 1-4), an increased interest is shown in the lifetime expectancy of the power converter involved in the system.



Figure 1-4. Distribution of the average failure rates of the subassemblies in wind turbines [11]

This continuous growth of installed wind power led transmission system operators to consider wind farms as a major player on the energy market, and impose standards similar to conventional power generation units. This means that voltage faults have to be withstood by the turbine, and during short circuit the plant must provide reactive power to the grid. Figure 1-5 presents the FRT demands for such a plant.



Figure 1-5. Voltage vs. Time Profile during FRT [12]

During LVRT, the DC Link voltage of the converter rises due to the excess produced energy that cannot be discharged into the grid. The excess has to be dissipated in order to protect the capacitor bank, thus the converters are equipped with braking choppers, which are switched on if the DC voltage exceeds safety limits.

The IGBT modules used in braking choppers are subjected to transient operations and abnormal current levels. This operation profile subjects the transistors to high stresses that may lead even to destruction of the device, as the temperature in the device can get higher than safe operation limits.

In order to avoid destruction of braking chopper IGBTs, the need of information about instantaneous junction temperature arises. As the operation regime is transient, there is interest of having developed a technique that will allow wind turbine inverter manufacturers to limit the number of paralleled transistors as much as possible, while avoiding physical destruction and keeping the ability of FRT for same period of time.

1.2. OBJECTIVES

In order to understand the influence of IGBT parameters and importance of real time monitoring, a study case will be carried out, in which the main failure mechanisms of IGBTs are illustrated.

The main objective refers to the need of an accurate thermoelectric model that can estimate the instantaneous temperature of the IGBT chip. The model must be able to substitute test systems in order to determine stress limits of DUTs. Therefore, the main objectives in modelling are to:

- Realize thermal loss models for all involved switching devices;
- Realizing a thorough Cauer model of the involved components, based on physics of the devices, in order to simulate the heat flow during operation;
- Realize a thermoelectric model of the system that is able to simulate instantaneous variation of device parameters, such as losses at different temperature levels, dynamic forward voltage drops, and variable heat capacities of involved materials.

The second objective of the project is to design a test setup for single pulse testing of FF1400R17IE4 (1400 [A], 1700 [V]) IGBT power module from Infineon. As the module is meant to operate for short periods of time and high current densities, the design constraints are as following:

- The setup must provide up to 3000 [A] current for 3 [s] in short-circuit operation;
- Due to short time operation, heat-sinks must be dimensioned in order to absorb all dissipated heat;
- The system must be dimensioned in such matter to minimize power consumption and size.

In order to assimilate the state of the art in thermoelectric modelling, a study case on existing modelling techniques for chip temperature estimation during transient operation must be carried out.

1.3. OVERVIEW OF FAILURE MECHANISMS IN POWER MODULES

The continuous development of wind turbine technology led to use of higher power generators as variable speed drives. The energy that the generator produces is converted to the parameters demanded by the grid using VSIs. As the demands in such drives are related to high power handling combined with high switching frequencies, the preferred switching device is the IGBT.

Although the IGBTs are appreciated for their robustness, the excess of electrical and thermal stresses that they are subjected to leads to the failure of the devices. The most important parameters that contribute to the degradation and failure of IGBTs are the ambient temperature variation, chip temperature variation and peak temperature on the chip. The power and thermal cycles that the devices are subjected to, lead to different failure mechanisms. The main failure mechanisms are briefly described in the following.

1.3.1. OPEN CIRCUIT FAILURES

Bond Wire Failures

Approximately 85 [%] of the bond wires contained in IGBT power modules are part of the power circuit of the power poles. This implies their exposure to the temperature swing that appears during operation. The differences in thermal expansion coefficients of different alloys bonded together generate mechanical stresses at connection points. Also, the flexure of the wires is a result of temperature swings, as the material dilates and contracts repeatedly. [13]

As the failure of bond wires cause changes in contact resistance and current distribution, the forward voltage drop is directly affected by these failure mechanisms. This would lead eventually to the destruction of the entire device, because the remaining wires would be subjected to increased stresses due to the higher current density. Because of these properties, the bond wire failures are categorized as open circuit failures.

• Bond wire lift-off

The bond wire lift-off is the most common failure that appears in IGBTs [14]. The lifting is caused by thermal cycling. Cycling can be caused by driver faults or fault-induced rupture of the IGBT, but also appears in normal operation, with only long-term effects. Figure 1-6 shows the physical lift-off of a bond wire in a failed IGBT. [15]



Figure 1-6. Example of Bond wire lifting [16]

• Bond wire heel cracks

The thermal expansion of the wire causes mechanical flexure. This process inflicts fatigue at the inflexion regions of the wires. The plastic deformation of the material leads to appearance of cracks, which propagate in complete rupture of the wire (Figure 1-7).



Figure 1-7. Bonded Wire Failure due to Heel Crack [17]

Solder Layer Failures

Being one of the main failure mechanisms in IGBT chips, the fatigue of the solder layers is a great subject of interest for device breakdown prevention. The solder layer with the higher risk of failure is the one between the ceramic substrate and the base plate of IGBT modules. This is due to the high differences in thermal expansion coefficients of the materials. The large contact area and high temperature swing are also increasing the risk of failure. [13]

During high temperature operation, the recombination in solder alloy leads to formation of voids (Figure 1-8). These voids cause accelerated ageing effects of the device, as the heat dissipation performance of the IGBT is decreasing. This results in higher temperature on the chip and therefore higher stresses on the bond wires and metallization layer. [18] [19]



Figure 1-8. Acoustic Map of Solder Illustrating Voids (Red Stains) in the Material [20]

Emitter Metallization

Thermal cycling of the materials also makes an impact on the Aluminium metallization of the emitter. However, in this case the issue is not related to mechanical stresses generated by thermal expansion. The impure Aluminium metallization reconstructs under power cycling by crystalizing. This leads to appearance of voids and crack propagation points. Those contribute at higher electrical resistance (therefore more heat dissipation) and bond wire cracking and lifting. [13] [21]

1.3.2. SHORT CIRCUIT FAILURE MECHANISMS

Latch Up

Due to the existence of a parasitic thyristor in the power IGBT structure, the devices are susceptible to this type of failure. Figure 1-9 presents the structure of an IGBT. It can be observed that it has the PNPN structure like of a thyristor. The thyristor behaviour is avoided by means of high conductivity on the P-N⁻-P path, thus having, during conduction, the characteristic of the bipolar PNP transistor. For too high values of current, the second P layer can get heavily n doped, and make the device behave like a thyristor. [2]



Figure 1-9. Structure of an Insulated Gate Bipolar Transistor [22]

The problem created by this latch-up is that the device can no longer be controlled through its MOS gate. This leads to device destruction if the latch-up current is not removed immediately. The latch-up is observable during the turn-off of the transistor.

Second Breakdown

During turn-on, the collector-emitter voltage remains at its blocked voltage level until the transistor enters saturation and starts conducting. If the di/dt is very high, the current will continue to rise steeply and therefore the device will be submitted to high current and high voltage simultaneously. This can lead to avalanche and produce a second breakdown voltage of the transistor.

1.3.3. CONCLUSION

The main failures that might appear in an IGBT used as a braking chopper were shortly described. While the bond wire lift-off is most probably to appear only in the case of long term operation, it can be predicted that heel ruptures are a more possible failure for braking chopper IGBTs. This is due to the high current which can induce mechanical forces that bend the wires above their elasticity levels, causing plastic deformation.

Solder voids and solder cracks are also possible failures due to the low melting point of solder and large differences between coefficients of thermal expansion, in comparison with its neighbouring materials.

Although the braking chopper is more exposed to short circuit failures due to the handling of currents larger than guaranteed by the manufacturers, these can be avoided by using slope inductors and properly dimensioned gate resistors.

1.4. OVERVIEW OF THERMAL MODELLING TECHNIQUES FOR IGBT MODULES

Showing that most of the failures in IGBT modules are caused by thermal and electrical induced stresses, the need of temperature estimation tools is justified. The process of temperature estimation is divided in two steps: power loss modelling and thermal modelling.

Power losses can be modelled by considering all its parasitic components in circuits implemented in dedicated tools like Saber and PSpice, or as look-up tables, for matrix manipulation based software programs.

1.4.1. LOSS MODELLING USING EQUIVALENT CIRCUIT

The equivalent circuit of an IGBT with all its parasitic components is presented in Figure 1-10 [23]. This modelling technique presents the advantage of high accuracy and also transient waveform estimation.



Figure 1-10. IGBT Structure and Representation of Parasitic Capacitances [23]

Where:

- C_m Source Metallization Capacitance;
- C_{oxs} Gate Oxide Capacitance (of the source overlap);
- C_{oxd} Gate Oxide Capacitance (of the drain overlap);
- C_{gdj} Gate-Drain Overlap Depletion Capacitance;
- C_{cer} Collector-Emitter Redistribution Capacitance;
- $C_{ebj} + C_{ebd}$ Emitter-Base Depletion Capacitance.

The disadvantage of this circuit is that the parameter extraction is a hard process and requires knowledge about thicknesses of layers. Generally a simpler model which is only based on input capacitance, gate charge and reverse transfer capacitance can be implemented, with the compromise of losing information about the switching waveforms. These capacitances are always available in the datasheets of the device.

1.4.2. LOOK-UP TABLE BASED LOSS MODELLING

Most of the manufacturers offer information about the losses in forms of graphs that illustrate interdependence between the energy consumption during ON- or OFF-switching and collector current at a certain blocked voltage value. The information is presented for more temperature values, in order to get a feeling about their variation while the chip is heating. The reason why they are presented for only one voltage value is that the dependency with respect to blocked voltage is linear.

Output characteristics that illustrate the forward voltage drop dependency on surged current are presented to calculate conduction losses. These characteristics are also presented for more temperature values, in order to have more accurate information about the forward voltage drop.

Inputting this information into look-up tables, the energy consumption during switching or conduction for any scenario can be estimated by means of interpolation.

The disadvantage of the look-up table loss model is that it offers absolutely no information about the switching waveforms. Generally, software that uses this type of model is meant for steady-state simulations and do not have feedback loops to simulate also these influences in the electrical circuit. [24]

1.4.3. 1-D THERMODYNAMIC MODELS

The thermal models with a widespread use are based on implementation of equivalent electrical networks which emulate thermal dynamics. Table 1-2 presents the correspondences between electrical and thermal parameters, needed for this implementation.

Electrical Parameter	Thermal Equivalent
Voltage V [V]	Temperature Difference ΔT [K]
Current I [A]	Heat Flux P [W]
Charge Q [C]	Thermal Energy Q _{th} [J]
Resistance R $[\Omega]$	Thermal Resistance R _{th} [K/W]
Capacitance C [F]	Thermal Capacity C _{th} [J/K]

 Table 1-2. Equivalence of Electrical and Thermal Parameters [2]

The thermal transient is approximated using equation (1.1), having the number of parameters dependent on the desired resolution for the analysis. [25]

$$\Delta T(t) = \sum_{i=1}^{N} T_i * e^{(-\frac{t}{\tau_i})} (1.1)$$

Foster Network

One of the most used types of RC networks is the Foster network, in which RC time constants model the exponential terms of Equation (1.1). The widespread use of it is justified by its simple parameterization and the fact that manufacturers offer information about the thermal resistances and time constants in the datasheets. Figure 1-11 presents a Foster network for one of six cells of an IGBT + Diode half bridge module.



Figure 1-11. Foster Network Representation for Half-Bridge Power Module Cell

The main disadvantage of this model is that it does not recreate the physical nodes along the heat transfer paths, representing only the input and output ports of the modelled thermal equivalent. Therefore, it is not efficient in understanding thoroughly the behaviour of the device, but only an approximate thermal response for a certain heat flux input. [2] [25] [26] [27]

Cauer Network

The Cauer Network represents a closer physical representation of the thermal structure, as the RC cells model each layer of the device. Intermediate thermal resistances can be calculated in order to implement conduction losses through all thermal paths. [2] [25]

Detailed information about calculation and implementation of this type of network is presented in Chapter 3.

The drawback of Cauer network is the complexity of calculations, due to the fact that the time constants depend on all resistors up to that point.

1.4.4. 3-D THERMODYNAMIC MODELLING

Although the Cauer model is a representation of physical layers and thermal transfer paths, it is only a rough approximation of the complex geometry of the layers involved. Lateral heat spreading cannot be modelled through 1-D models.

Finite Element Models

The use of finite element modelling software for thermal applications is very attractive, as it offers accurate information about heat transfer in devices with complex geometry and different materials used.

Using finite element modelling requires advanced mathematical knowledge, as the most important step in the design method is configuring the netlist. Its accuracy must be increased in regions which are of high interest, and where temperature variations are expected to be large. This must be done without extending the netlist to a too large number of nodes, by having comparable density in regions which do not represent such high interest.

Examples of models for finite element analysis are presented in [11], [19] and [28]. The main drawback of this type of model is that it requires large computational power and therefore it cannot be used for steady-state operations or for long pulses.

The finite element simulation is used by manufacturers to determine, using curve fitting, the Foster network parameters.

Finite Difference Modelling

Another accurate method of heat transfer modelling is by realizing Finite Difference models. The Finite Difference Method offers less information about critical points with respect to Finite Element, but it is equivalent for the thermal paths visualization.

The Cauer model can be extended to a finite difference model by dividing layers into sections, as presented in Figure 1-12. The resolution is to be chosen by the designer, but care must be taken, because the dimensions of a section will be kept constant for all involved layers. This may result in models with a large number of nodes which also require large computational power and time, as for the finite element analysis.



Figure 1-12. Extended Cauer Model for a two-layer System [2]

1.4.5. CONCLUSION

Three-dimensional simulations represent an attractive solution for thermal modelling because of the high accuracy and large amount of information they can offer, but their high computational needs do not recommend them for long simulation times.

In order to have a simple model for long simulations or steady-state thermal estimation, manufacturers develop Foster models based on results obtained in finite element analysis. However, these models do not offer information about physical layers.

A more attractive solution, with relatively small computational needs, is the Cauer network topology. Extending a one-dimensional Cauer network in order to estimate heat transfer between layer groups represents an attractive compromise. Such a model can reflect physical nodes in 1-D but also thermal coupling of the layers from an IGBT power module.

1.5. PROJECT OUTLINE

The proposed master thesis focuses over the thermal analysis of braking chopper used in wind turbines to improve the transient stability of the WT during voltage disturbances and provide LVRT capabilities, a requirement mandatory for all grid connected application. The thesis is structured in four chapters.

The first chapter justifies the importance of acquiring thermal information during transient operation of braking chopper IGBTs. In the first part, the subject is introduced by presenting the impact of wind power in present day energy market and the grid connection requirements for wind power plants. In continuing, the problem is defined and the objectives of the study are presented. Moreover, the most important failure mechanisms and the thermal modelling techniques presently used are briefly described.

The second chapter presents the design procedure for a test setup for single pulse short circuit testing of power modules. System dimensioning and choosing of measuring equipment is presented. The chapter ends with the presentation of a protection and data acquisition circuit board designed particularly for the described configuration.

In the third chapter the thermoelectric models realized are described and presented. The first two sections describe the general characteristics of the diodes and IGBTs, characteristics that stand as the basic knowledge for loss modelling. The third and fourth sections present the loss models realized for the two types of power modules used, their thermal models and heat flow theory used for modelling are presented. The chapter ends with a presentation of simulation results which illustrate the functionality of the model.

The fourth chapter summarizes the work presented along this thesis. The main conclusions are deduced based on the results achieved. In the ending, the directions for future work are outlined.

2. Test Setup Design

In this chapter, the designing of a test setup for single pulse short circuit testing of power modules is presented. The design constraints and chosen devices are described in the opening section, followed by a thorough description of the control boards for the setup.

2.1. TEST BENCH REQUIREMENTS

The purpose of the setup is to recreate the functioning conditions for the Device Under Test (DUT) in laboratory, and take advantage of the possibility to monitor the variation of all its thermal and electric parameters. The initial considerations of the setup are explained in the following.

As a braking chopper IGBT, the DUT is subjected to short operation time, between 10s of milliseconds and a maximum of 3 seconds. During this short operation, the transistor is conducting a current larger than nominal. The maximum admitted current is chosen as the "maximum repetitive peak current" given in the datasheet, that is 2800 [A]. Because of its short and sporadic operation profile, a braking chopper is not justifying use of active cooling. A simple Aluminium block will be used as heat-sink, having specified that it can absorb the total dissipated power, which for a maximum of three seconds is maximum 15 [kW].

To minimize the energy waste, the DUT will be subjected to short-circuit testing. Because of this, a new problem arises, given by the risk of too high di/dt. In order to limit the current slope, an inductor must be used before the DUT. As an extra caution, the power is fed through two paralleled IGBTs which will disconnect the DUT in case of overcurrent.

In order to provide the low voltage demanded for short-circuit testing the need for a specially designed step-down transformer appears. The required transformer will lower the voltage from 400 $[V_{ph-ph}]$ to 25 $[V_{ph-ph}]$. The main consideration is to have enough voltage on the second winding to provide the voltage drops over the rectifier, control IGBTs and the DUT; the connection chosen for the transformer is Dd. To avoid the need of a big and expensive transformer, the AC frequency for it is chosen to be 100 [Hz]. This is achieved with a VLT. The use of a VLT also implies the need of a filter after it.

The setup must also record DUT parameters. For this, a current sensor, a forward voltage circuit and a FLIR camera are used. The signals are converted and acquired via a 24-bit ADC converter from National Instruments and LabView.

Figure 2-1 presents the diagram of the setup with all its needed components. Their selection and dimensioning is presented in the following.



Figure 2-1. Block Diagram of Test System for Single Pulse Testing of 1400A IGBT Module

Danfoss VLT

The VLT chosen is model FC302P55K that has a power of 55 [kVA]. As the needed power at 2800 [A] is given by the current through the circuit multiplied with total voltage drop, it can be concluded that the maximum required power for the DC part of the system is of 30 [kW]. To this must be added the reactive power consumed by the transformer. It can be concluded that a 55 [kW] supply is sufficient for the needs of the system. The purpose of the frequency converter is to supply the 100 [Hz] AC voltages for the transformer and reduce the RMS voltage so that it will have the desired DC value.

Transformer

The transformer is specially designed by DanTrafo, following the power requirements given:

- Output phase to phase voltage of 25 [V];
- Continuous RMS current 1500 [A];
- Frequency 100 [Hz].

The main characteristics of the transformer are:

- Turns Ratio N_p/N_s : 81/4;
- Primary winding RMS voltage and current: $V_p = 400[V]$; $I_p = 35.97 [A]$;
- Primary Reactance: $R_1 = 0.0255 [\Omega]; X_{1\sigma} = 0.0383 [\Omega];$
- Secondary winding RMS voltage and current: $V_s = 24.88$ [V]; $I_s = 1531$ [A];
- Secondary Reactance: $R_2 = 0.0001 \ [\Omega]; X_{2\sigma} = 0.0001 \ [\Omega];$
- Nominal operation parameters:

- Output Power: $S_2 = 42558$ [VA];
- Losses: $P_{Cu} = 96.4 [W]; P_{Fe} = 105.8 [W];$
- Efficiency: $\eta = 98.43$ [%];
- Open circuit parameters:
 - Active Losses: $P_{1OC} = 106.5$ [W];
 - Reactive Losses: $Q_{1OC} = 96.84$ [VAr];
 - $\circ \quad \text{Current Factor: } I_0/I_N = 1 \text{ [\%]};$
- Short circuit parameters:
 - Active Losses: $P_{1SC} = 98168$ [W];
 - Reactive Losses: $Q_{1SC} = 4985$ [VAr];
 - Voltage Factor: $V_{SC}/V_N = 14.13$ [%].

The manufacturer also gives the equivalent diagram with the secondary parameters reduced to primary, for nominal load operation at 114.7 [°C], as presented in Figure 2-2. The datasheet is presented in Appendix 1.



Figure 2-2. Equivalent Diagram of 100 Hz 400/25 V Transformer at Nominal Load Operation

Rectifier

The three-phase rectifier is built using the rectifier modules DD540N22K from Infineon. The maximum RMS current through a diode is 900 [A]. The on-state voltage drop for the diode is given by the equation 0.78 [V] + 0.31 [m Ω] * I_F. The datasheet of the module is presented in (Appendix 2).

Protection IGBTs

The two IGBT modules are FF1000R17IE4 from Infineon. This type of module has been chosen by matters of available devices. Due to the high price of power modules, it was lacked of justification to buy new power modules. There are two paralleled IGBTs in order to sustain the current demanded by the DUT without representing a comparable breakdown risk. The cooling system is as for the DUT a simple Aluminium plate. The operation profile of the setup does not justify need of active cooling for any of the devices.

Main characteristics of the FF1000R17IE4 power module are:

- Collector-emitter breakdown voltage: V_{CES} = 1700 [V];
- Continuous collector current: I_C = 1000 [A];
- Repetitive peak collector current: I_{CRM} = 2000 [A];
- Input capacitance: C_{ies} = 81 [nF];
- Reverse transfer capacitance: $C_{res} = 2.6 [nF]$;
- Turn-on delay (1000 [A], 900 [V]): $t_{d on} = 0.6 [\mu s];$
- Rise time (1000 [A], 900 [V]): $t_r = 0.12$ [µs];
- Turn-off delay (1000 [A], 900 [V]): $t_{d off} = 1.25$ [µs];
- Fall time (1000 [A], 900 [V]): $t_f = 0.5 [\mu s];$

The rest of the characteristics of the IGBT and the characteristics of the integrated diode can be found in the datasheet from Appendix 3.

Current slope inductor

The inductor is air coil type and the value of 0.5 [uH] by the need of a slow current slope. For this value, the current rise is of 2 [kA/ms].

FF1400R17IP4 Power Module

This is the device subjected to tests. The used module is open, in order to have the possibility to monitor temperature variations on it.

Its main characteristics are:

- Collector-emitter breakdown voltage: V_{CES} = 1700 [V];
- Continuous collector current: $I_C = 1400 [A];$
- Repetitive peak collector current: I_{CRM} = 2800 [A];
- Input capacitance: C_{ies} = 110 [nF];
- Reverse transfer capacitance: $C_{res} = 3.6 [nF];$
- Turn-on delay (1400 [A], 900 [V]): $t_{d \text{ on}} = 0.88$ [µs];
- Rise time (1400 [A], 900 [V]): $t_r = 0.14$ [µs];
- Turn-off delay (1400 [A], 900 [V]): $t_{d off} = 1.35$ [µs];
- Fall time (1400 [A], 900 [V]): $t_f = 0.77 [\mu s];$

As these are the main characteristics needed for thermal modelling, the rest are not presented here. They can be found in the datasheet from Appendix 4.

Current Sensor

The current measurement is realised using an ABB ES2000S sensor, which has the following characteristics (Appendix 5):

- Measuring range: $I_{Pmax} = \pm 3000 [A];$
- Measuring resistor: $R_M = 0 11 [\Omega];$
- Turn ratio: 1/5000;
- Secondary current at $I_{PN} = 2000 [A]$: $I_S = 400 [mA]$;
- Supply Voltage: $V_{DC} = \pm 24$ [V].

VCE Measurement board

For the voltage measurement, the circuit from Figure 2-3 is the chosen solution. As the blocking voltage is not subject of interest because of short-circuit testing, the forward voltage drop will be measured with a current-source circuit. The op-amp ensures signal continuity, and the circuit is isolated from user through isolation amplifier. This is chosen in order to be able to also use the circuit in high blocking voltage ranges. Entire circuit and layout is presented in Appendix 6.



Figure 2-3. VCE Measuring Circuit Diagram

2.2. DESIGN OF CONTROL AND PROTECTION CIRCUITRY

In order to satisfy the needs of IGBTs control and protection, a PCB was designed having the following needs:

- *Single Voltage Supply:* A 15 V external power supply is used as the single power input of the PCB. This is chosen in order to simplify connection of the device;
- 5 V Logic: The PCB must have a logic implemented on 5 V level, in order to ease the interfacing with gate drivers;

- *Current Sensor Alternative Supply:* The board must include voltage conversion to +/-24 V, in order to supply the current sensor; the power demand is not high, as this represents an alternative supply, that can be used only for short times;
- *Measurement Circuit:* the board must have a circuit for conversion of the measured current to voltage, in order to be used in logic conditioning;
- *Protection Circuit:* the board must cut-off gate signals in case of overcurrent or gate fault detection;
- *Data acquisition:* the board must also acquire the voltage drop from the VCE measuring circuit presented in the previous section.

The block diagram based on which the circuit was realised is presented in Figure 2-4 and explained in the following.



Figure 2-4. Block Diagram of Control PCB

2.2.1. VOLTAGE CONVERSIONS

The 15 [V] supply is used only for gat driver supply. The mains supply has been chosen to be 15 [V] because the three gate drivers require large amount of power compared to the rest of the circuit. It is, therefore, a solution chosen for economic reasons.
The voltage for logic circuitry is provided through a 1 [W] DC/DC converter from TRACO POWER, TMA1505s. The +/- 15 [V] level is provided through a 3 [W] DC/DC converter, TMR 3-1223d, from the same producer. Although, because of the alternative current sensor supply, the +/- 15 [V] converter seems to be too small, it is satisfactory because the short operations of the sensor that can be guaranteed through this supply.

The current is measured through a 12.5 $[\Omega]$ power resistor. In order to limit the measured voltage to a maximum of 10 [V], the measurement is processed through an operational amplifier with factor of 1, and supply of +/- 10 [V].

The supply voltages for op-amp and current sensor are realized through adjustable voltage regulators. Figure 2-5 presents the circuit for voltage conversion. The output voltages are determined by two resistors, one surging current from the output to the adjust port. The ratio between them must be calculated by considering the 1.25 [V] reference at the adjustable port, which is internally regulated. Therefore, the resistors must form a voltage divider that has a 1.25 [V] voltage drop on the resistor that connects output to adjustable pin, and the rest of the voltage drop to the ground level. For the negative voltage regulators, the working principle is the same, only that the voltage reference is internally regulated for -1.25 [V].



Figure 2-5. Voltage Regulators Circuitry

2.2.2. MEASUREMENTS AND OVER CURRENT PROTECTION

The voltage and current measurements are processed through an operational amplifier, as depicted in Figure 2-6. The supply of the op amp is chosen in order to limit the output to a maximum of 10 [V]. This level is chosen by considerations of data acquisition equipment. It can be also observed that the op-amp was configured in a differential mode operation. This is realized for better common-mode rejection. The capacitances and resistances have been chosen by considering that a 10 [kHz] bandwidth can offer a more than sufficient accuracy of the measurements.



Differential Amplifier Measurement Scaling

Figure 2-6. Differential Amplifier Configuration

The current protection is realised with a comparator. When the measured proportional voltage exceeds a certain value, the output of the comparator will be low. In case the current is in normal limits, the output is high. In order to convert the signal to active high, a NAND gate is used. Figure 2-7 presents the implemented circuit.



Figure 2-7. Over current Protection Circuit

2.2.3. GATE SIGNALS CONDITIONING

Due to the single pulse operation of the setup, the control is very simplistic. In order to achieve the pulse, the monostable circuit SN74121N is used. Through two external RC circuits, the pulse width can be varied from 40 [ns] to 28 [s]. The triggering of the monostable is realised through a push button. The signal obtained is used as gate signal for the two paralleled control IGBTs. In order to condition the signal presence of the lack of any gate driver errors or protection triggering, a buffer is used, having the outputs triggered by these active high signals. If one of the errors interrupts normal functioning, the outputs of the specific buffer section will become zero and stop the IGBTs. Figure 2-8 presents the schematic implementation.



Figure 2-8. Gate Signal Conditioning and Pulse Width Diagram

The gate error signals are buffered and OR-ed in order to create the GATE_ERR signal, which is referring to any of them. The buffer has the purpose to change the signals from active low to active high. This is needed because they are used to condition the functioning of a different buffer, as described previously.

The complete design and layout of the PCB is presented in Appendix 8.

2.2.4. PCB VALIDATION

Several simple tests have been carried out on the PCB in order to validate its proper functionality. The logic voltage level is first verified to be 5 [V]. Figure 2-9 depicts the logic voltage on channel 1 of oscilloscope, while channel 2 represents the voltage after the push button (turn-on command). It can be observed that the proper functionality is obtained, having a 5 [V] voltage level for logic devices and 0 [V] gate command before actuation of the push button.



Figure 2-9. 5 [V] Voltage Supply Functionality (channel 1) and Button Output (channel 2) Signals

The proper functionality of the push button is further confirmed by verifying that the actuating of the button is generating a change of the turn-on command from 0 to 5 [V], without having a strong ripple ("ringing") of the command signal. Figure 2-10 shows that the criteria are fulfilled.



Figure 2-10. Push Button Actuation Functionality (Gate Turn-On Command)

The functionality of the gate triggering is further observed. This simple measurement confirms the functioning of the monostable, gate error protection and buffering. Furthermore it assures that the over current protection has the proper logic, allowing gate command when there is no current measurement. Figure 2-11 depicts the proper functionality of the gate triggering. It has to be mentioned that until de submission of this report, the exact dependency of the gate pulse width on the timing circuitry from the monostable has not been determined.



Figure 2-11. Gate Turn-On Control: Command Signal from Push Button (Channel 1) and Gate Command (Channel 2)

The last test depicted here is the functionality of the protection. The test has been carried out for each of the two protections. It has been observed that, for the current protection, a current corresponding to 2.64 [V] voltage drop on the measuring resistor disables the output of the gate buffer. The Gate Error protection has been tested by pulling down one of the error feedbacks. Figure 2-12 depicts the proper functionality of the protection, having the command signal on channel 1 and the gate signal on channel 2.



Figure 2-12. Gate Protection Functionality: Command Signal (Channel 1) and Gate Signal (Channel 2)

3. THERMAL MODELLING

The chapter presents the model realized for transient thermal analysis of the power modules during FRT. In the first two sections, the general characteristics of diodes and IGBTs are presented. Those represent the background for the loss modelling of the devices. Sections 3 and 4 present the realized models for protection power modules and DUT respectively, and device parameters used in modelling. The chapter ends with the presentation of simulation results for different scenarios, and presentation of the temperature estimator which represented a final purpose of the thermoelectric model.

In order to have a more accurate image of the system behaviour, it must be taken into consideration that all the equipment is subjected to thermal stresses, due to the high current used. As a first approximation, it has been considered that the transformer, due to its high volume, has a thermal capacitance large enough to be omitted from thermal modelling.

Therefore, the system before the bridge rectifier can be considered as homogenous. The diodes of the rectifier are modelled simply as having a voltage drop $V_{F} = V_{F(TH)} + R_{ON}*I_{F}$. As the current through the control IGBTs is significant, they must be modelled in order to comprise their nonlinearities.

The importance is justified by the fact that the current and temperature dependent voltage drops affect the voltage to which the DUT will be subjected, therefore also the instantaneous current through it. This results in a nonlinear power flow, which must be also reproduced as in simulations in order to have comparable results. The diode behaviour and IGBT behaviour are presented in continuing.

3.1. GENERAL CHARACTERISTICS OF POWER DIODES

The power diode is basically a PN junction with an added n⁻ epitaxial layer, which is grown on top of the heavily doped n layer. This epitaxial layer is also called drift region, and its thickness determines the breakdown voltage of the device. [22]

The drift region is also important when considering power dissipation. The main voltage drop occurs on this layer of the diode, which has a resistive behaviour. Therefore, it results in a linear dependency of forward voltage drop with respect to the forward bias current. However, due to its small on-state resistance caused by the large amount of excess-carrier injection during conduction, the epitaxial layer has a negative coefficient to the R_{on} with the growth of the current. The ideal characteristic of a power diode is presented in Figure 3-1. [22]



Figure 3-1. Typical I-V characteristic of Power Diodes [22]

The heat generated during operation is sourced by the losses that occur during switching and conduction of the device. These switching and conduction losses can be estimated from switching waveforms as presented in Figure 3-2. In the case of most rectifiers, due to fast turn-on times with respect to switching frequency, the on-switching losses can be neglected. On-state losses represent the product of forward voltage drop and current flowing through device, while off-switching losses are determined by the reverse recovery charge of the diode. [22]



Figure 3-2. Switching Waveforms of Power Diodes [22]

3.2. GENERAL CHARACTERISTICS OF IGBTS

Insulated gate bipolar transistors (IGBT) have been introduced in the 1980s, as an answer to the need of a high power device with fast switching frequency capability. The small on-state losses of the bipolar junction transistors are combined with the voltage controllability of MOSFETs, which yields the need of small gate currents during switching. This results in small switching times and small power dissipation. [23]

The internal structure of an IGBT is presented in Figure 3-3. The feature of the IGBT is the n^+ buffer layer in the punch-through structure. Although the adding of this heavily doped layer reduces the reverse breakdown capability, it is generally preferred due to its capability to reduce the drift region by a factor of 2, as the depletion layer can easily extend across the entire n^- layer, because the heavily doped buffer will prevent the reach of the depletion layer to the p^+ layer. Shortening of the drift region is very useful, as it reduces the conduction losses for the device. [22]



Figure 3-3. Internal Structure of a Punch-Through IGBT [22]

Figure 3-4 presents the output characteristics of the IGBT. It can be observed a similarity to the diode, having a minimum forward voltage drop, and growing linear with the growth of the current. This represents the power loss during conduction.



Figure 3-4. I-V Characteristic of n-channel IGBT [22]

The on-switching waveforms of the IGBT are depicted in Figure 3-5. During the delay time t_d , the input capacitance is charged until the gate-emitter voltage reaches its threshold value. This gate current consumption is negligible in the interest of power dissipation, having only importance on delay-time influences, thus affecting the switching frequency capabilities of the device. [22], [23]

During the rise time, the collector current grows from zero to load current value. The current slope is determined by gate voltage and IGBT transconductance. The collector-emitter voltage starts to drop as soon as the gate voltage reaches the value necessary to support steady-state collector current. As depicted, the voltage drops rapidly in the beginning, during t_{vf1} , and slower during t_{vf2} . This second period of voltage fall is influenced both by the MOS characteristic of the IGBT – as C_{gd} capacitance increases at low drain-source voltages – but also by the PNP transistor portion, which transits the active region slower than MOSFET portion. [22], [23]



Figure 3-5. ON-Switching Waveforms of IGBT [22]

The energy consumption during turn-on can be estimated by considering the $C_{\rm gd}$ variation, as being:

$$E_{ON} = \frac{t_{ri} * I_D * V_D}{2} + \frac{I_D * V_D * t_{vf1}}{2} + \frac{I_D * V_{Cgd} * t_{vf2}}{2}, (3.1) \text{ where:}$$

$$t_{vf1} = R_G * C_{gd1} * \frac{V_D - V_{ON}}{V_{GE} - V_{GE(th)}}, (3.2) \text{ and}$$

$$t_{vf2} = R_G * C_{gd2} * \frac{V_{Cgd} - V_{ON}}{V_{GE} - V_{GE(th)}}$$
(3.3).

The turn-off waveforms of the IGBT are depicted in Figure 3-6. As it can be observed, the current and voltage remain constant until V_{GE} drops below the level required to maintain saturation current. After this period, the collector-emitter voltage rises to blocked voltage, while the collector current remains constant. This MOS characteristic can be also used to determine the rise slope, as the voltage rise is determined by the gate resistor. After the MOS channel turns off, the collector current has a steep descent during the period t_{fi1} , and the freewheeling diode starts conducting. The tail in the current waveform is determined by the carrier excess stored in the drift region. The only way to remove the excess carriers from drift region is by recombination within the transistor. In the case of punch-through IGBTs, the buffer layer acts as a sink for excess holes, and shortens current tail, thus resulting much smaller turn-off time. [22], [23]



Figure 3-6. Turn-Off Waveforms of IGBT [22]

The loss model of an IGBT may be done by considering all parasitic capacitances and material resistances – as described by Allan Hefner in [29]. The model can be implemented in PSpice or Saber. Simpler models are available in Simulink and PLECS, and are based on look-up tables. In this report, the look-up table model from PLECS is used.

3.3. THERMOELECTRIC MODELLING OF THE CONTROL MODULES

Using information provided in the datasheet, the energy loss for each operation case was modelled in PLECS. The model for switching losses is a four-dimensional matrix, having given as input vectors the blocked voltage, forward current and junction temperature, and outputting the energy loss in [mJ]. Figure 3-7 presents the losses that occur during on-switching of the IGBT, while Figure 3-8 depicts the OFF-switching losses. The explicit values are depicted in Table 3-1 and Table 3-2, respectively.



Figure 3-7. Energy Losses for ON-switching of IGBT from FF1000R17IE4 module

Table 3-1. Energy Loss during ON-Switching of FF1000R17IE4 IGBT - Look-Up Table Data

T = 25°	$T = 25^{\circ}C$											
	0 A	200 A	400 A	600 A	800 A	1000 A	1200 A	1400 A	1600 A	1800 A		
0V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ		
900V	0 mJ	66 mJ	100mJ	170mJ	200mJ	265mJ	300mJ	360mJ	500mJ	580mJ		
T = 125	°C											
	0 A	200 A	400 A	600 A	800 A	1000 A	1200 A	1400 A	1600 A	1800 A		
0V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ		
900V	0 mJ	86 mJ	150mJ	220mJ	300mJ	390mJ	500mJ	635mJ	800mJ	1005mJ		
T = 150	°C											
	0 A	200 A	400 A	600 A	800 A	1000 A	1200 A	1400 A	1600 A	1800 A		
0V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ		
900V	0 mJ	90 mJ	160mJ	230mJ	320mJ	415mJ	540mJ	690mJ	860mJ	1090mJ		



Figure 3-8. Energy Loss during OFF-switching of IGBT from FF1000R17IE4 module

Table 3-2 Energy Loss	during OFF-Sy	witching of FF10001	R17IE4 IGBT -	Look-Up Table Data
1 doie 5-2. Lifergy Loss	ouring Or I -5	witching of 11 10001	(1/1L+10D)	LOOK-Op Tuble Data

$T = 25^{\circ}$	$T = 25^{\circ}C$											
	0 A	200 A	400 A	600 A	800 A	1000 A	1200 A	1400 A	1600 A	1800 A		
0V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ		
900V	0 mJ	70 mJ	95 mJ	135mJ	165mJ	200mJ	235mJ	270mJ	305mJ	370mJ		
T = 125	б°С											
	0 A	200 A	400 A	600 A	800 A	1000 A	1200 A	1400 A	1600 A	1800 A		
0V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ		
900V	0 mJ	72 mJ	130mJ	180mJ	240mJ	300mJ	360mJ	420mJ	480mJ	520mJ		
T = 150	°C											
	0 A	200 A	400 A	600 A	800 A	1000 A	1200 A	1400 A	1600 A	1800 A		
0V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ		
900V	0 mJ	90 mJ	150mJ	200mJ	270mJ	335mJ	395mJ	460mJ	515mJ	590mJ		

The conduction losses for the IGBT are given and modelled as transfer characteristics. The forward voltage drop is outputted depending on junction temperature and forward current. Figure 3-9 depicts the implementation in PLECS. The explicit values are shown in Table 3-3.



Figure 3-9. Output Characteristic of the IGBT from FF1000R17IE4 module

	0 A	100A	200A	400A	600A	800A	1000A	1200A	1400A	1600A	1800A
25°	0.8V	1.05V	1.2V	1.4V	1.6V	1.8V	2V	2.2V	2.4V	2.6V	2.8V
125°	0.6V	1V	1.25V	1.55V	1.8V	2.1V	2.35V	2.6V	2.85V	3.1V	3.35V
150°	0.6V	0.97V	1.25V	1.57V	1.85V	2.2V	2.45V	2.75V	3V	3.3V	3.6V

The main drawback of this toolbox is that it is not meant for dynamic simulations. Therefore, the forward voltage drops that occur during operation can be inputted as fixed values. This is a big issue for the system, as the input voltage is very small due to short-circuit testing. [24]

In order to overcome this disadvantage, the circuit has been modified as presented in Figure 3-10. The forward voltage is introduced by a controllable voltage source, to which the input signal is computed by reading the power loss and dividing it by the forward current.

Algebraic loop is broken by inputting the read voltage to a small separate circuit, with only a 1 $[\Omega]$ resistor. The current read is then inputted in the controllable voltage source "V", which simulates the forward voltage drop. This method is chosen because, in order to break the algebraic loops, the signal must be realized as a current controlled voltage source. Figure 3-11 depicts the functionality of the model, as it represents a measured voltage drop over the control transistor.



Figure 3-10. Dynamic Forward Voltage Drop implementation



Figure 3-11. Measured Voltage Drop over FF1000R17IE4 IGBT

The diodes of the module are also modeled considering the losses presented in the datasheet. The switch-on losses do not represent interest, as they are very small compared to reverse recovery, as explained in section 3.1. Figure 3-12 depicts the losses due to reverse recovery. The explicit values are depicted in Table 3-4. It must be noted that the energy losses correspond to negative voltages.



Figure 3-12. Energy Losses during Reverse Recovery of Freewheeling Diode of FF1000R17IE4 Power Module

Table 3-4. Reverse Recovery Energy Consumption of FF1000R17IE4 Diode - Look-Up Table Data

T = 125	$T = 125^{\circ}C$												
	0 A	200 A	400 A	600 A	800 A	1000 A	1200 A	1400 A	1600 A	1800 A			
0V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ			
-900V	0 mJ	90 mJ	125mJ	156mJ	180mJ	205mJ	220mJ	230mJ	237mJ	242mJ			
$T = 150^{\circ}C$													
	0 A	200 A	400 A	600 A	800 A	1000 A	1200 A	1400 A	1600 A	1800 A			
0V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ			
-900V	0 mJ	110mJ	152mJ	192mJ	225mJ	245mJ	266mJ	275mJ	284mJ	290mJ			

Figure 3-13 illustrates the output characteristic of the diode. Table 3-5 depicts the explicit values used. It can be observed that, although there is no difference between the values for 125 [°C] and 150 [°C], there are both inserted. This is done in order to avoid the risk of an erroneous interpolation for temperatures in operation range.



Figure 3-13. Output Characteristic of the Diodes from FF1000R17IE4 Power Module

Table 3-5. Output Characteristic of the FF1000R17IE4 Diode - Look-Up Table Data

	0 A	200A	400A	600A	800A	1000A	1200A	1400A	1600A	1800A	2000A
25°	0.8V	1.2V	1.42V	1.6V	1.75V	1.84V	1.96V	2.1V	2.21V	2.33V	2.44V
125°	0.6V	1.05V	1.4V	1.6V	1.8V	1.95V	2.15V	2.28V	2.42V	2.55V	2.7V
150°	0.6V	1.05V	1.4V	1.6V	1.8V	1.95V	2.15V	2.28V	2.42V	2.55V	2.7V

Because of the interest to study more aspects of the heat transfer inside a power module, but also to have increased accuracy with the model, the transistors have been modelled as a thermal RC ladder network, taking into consideration constructive dimensions and physical characteristics of the materials used. Figure 3-14 presents the structure of the 1000 [A] power module from Infineon.



Figure 3-14. FF1000R17IE4 Power Module

Along with the surfaces of each layer, the thicknesses are necessary in order to calculate thermal resistances and capacitances. The internal structure of a chip from the power module is presented in Figure 3-15. The layers presented are not to scale. The succession of the layers is as it follows: 1 -emitter metallisation, 2 -chip, 3 -solder, 4 -Direct Copper Bond (DCB), 5 -Ceramic bed, 6 -DCB, 7 -solder, 8 -baseplate.



Figure 3-15. Structure of an IGBT Module [30]

Figure 3-16 illustrates a section of the thermal chain. It can be observed that the exact thermal paths are recreated, with only two limitations: the path through air / silicone gel is considered of infinite resistance, and the path through the baseplate between the chips is considered of zero resistance. This is done in order to keep within the model the main heat flow path, to the heat-sink, unharmed. The sequence 1-14 is repeated 12 times, as there are 12 chip pairs in the module, six for each IGBT/diode.





In Figure 3-16, the marked RC components represent the layers as following:

- 1 Metallisation on IGBT chip (Aluminium);
- 2 IGBT Chip (Silicon doped with impurities);
- 3 -Solder (SnAg_{0.5}Zn);

- 4 Metallisation on Diode chip (Aluminium);
- 5 Diode chip (Silicon doped with impurities);
- $6 \text{Solder} (\text{SnAg}_{0.5}\text{Zn});$
- 7 DCB of Group 1 (Copper);
- 8 DCB of Group 2 (Copper);
- 9 Thermal Path Between Groups (through Ceramic);
- 10 Second IGBT Network (see 1, 2, 3);
- 11 Second Diode Network (see 4, 5, 6);
- 12 Ceramic bed half (Al₂O₃);
- 13 DCB (Copper);
- $14 Solder (SnAg_{0.5}Zn);$
- 15 Baseplate (Copper);
- 16 Thermal Paste;

In order to calculate the resistances and capacitances, the dimensions of layers and material properties were needed. The chips may be considered to be pure silicon, as the impurities represent a very small part and do not have a considerable impact on material properties.

Material properties (specific heat capacity and thermal conductivity) for solder are extracted from [31], while the thermal conductivities and mass densities for the rest of materials are extracted from [32]. The heat capacities for Aluminium, Silicon and Copper are considered as well for 300K, and are extracted from [33]. Table 3-6 presents the material properties used:

Layer	Material	Specific Heat Capacity	Thermal Conductivity	Mass Density [Kg/m ³]
LODT	4.1			2700
IGBT	Al	950	250	2700
Metallisation				
Diode	Al	950	250	2700
Metallisation				
IGBT Chip	Si	790	83.6	2329
Diode Chip	Si	790	83.6	2329
IGBT Solder	Sn ₂ Zn ₂ Ag	260	78	7400
Diode Solder	Sn ₂ Zn ₂ Ag	260	78	7400
DCB	Cu	397	386	8960
Ceramic Bed	Al_2O_3	880	18	3690
DCB	Cu	397	386	8960
Solder	Sn ₂ Zn ₂ Ag	260	78	7400
Baseplate	Cu	397	386	8960
Thermal Paste	-	-	16	-
Heat-Sink	Al	950	250	2700

Table 3-6. Material Properties for FF1000R17IE4 Power Module

Layer dimensions are acquired from the Department of Physics and Nanotechnology, and can be found in [28]. The thermal resistance and capacitance are calculated using these dimensions, as it follows:

$$R_{th} = \frac{h}{L*W*k}; (3.4)$$

$$C_{th} = c * \rho * L * W * h (3.5);$$

Where k is the thermal conductivity, c is the specific heat capacity, ρ is the mass density of the material and L, W and h are the physical dimensions as illustrated in Figure 3-17. The specific values are depicted in Table 3-7.



Figure 3-17. Heat Flow Representation through a Material

Table 3-7. Physical Dimensions of Constructive Layers of FF1000R17IP4 Power Module

Layer	Length	Width	Height	Area	Volume
	[mm]	[mm]	[mm]	$[mm^2]$	[mm ³]
IGBT Metallisation	13.6	13.6	$4*10^{-3}$	184.96	0.74
Diode Metallisation	12.7	12.7	$4*10^{-3}$	161.29	0.645
IGBT Chip	13.6	13.6	0.3	184.96	55.49
Diode Chip	12.7	12.7	0.3	161.29	48.39
IGBT Solder	13.6	13.6	0.05	184.96	9.25
Diode Solder	12.7	12.7	0.05	161.29	8.0645
DCB Group 1	CG	CG	0.3	954.51	286.353
DCB Group 2	CG	CG	0.3	667.86	200.358
Ceramic Bed	53	39	0.7	2067	1446.9
DCB	51	37	0.3	1887	566.1
Solder	51	37	0.1	1887	188.7
Baseplate	250	89	3	22250	66750
Thermal Paste	250	89	-	22250	-
Heat-Sink	400	300	30	$12*10^4$	$3.6*10^{6}$

Calculating equations (3.4) and (3.5) for metallization layer of IGBT chip results:

$$R_{th} = \frac{h}{L*W*c} = \frac{4*10^{-6}}{13.6*10^{-3}*13.6*10^{-3}*250} = 86.5*10^{-6} \, [K/W];$$

$$C_{th} = c * \rho * L * W * h = 950 * 2700 * 13.6 * 13.6 * 4 * 10^{-12} = 1.8725 * 10^{-3} [J/_K].$$

The same calculus has been carried out for all involved layers. The resulting values are depicted in Table 3-8.

Layer	Thermal	Thermal
	Capacitance [J/K]	Resistance [K/W]
IGBT Metallisation	$1.8725*10^{-3}$	86.5*10 ⁻⁶
Diode Metallisation	1.654*10 ⁻³	99.2*10 ⁻⁶
IGBT Chip	$102.097*10^{-3}$	19.4*10 ⁻³
Diode Chip	89.033*10 ⁻³	$22.25*10^{-3}$
IGBT Solder	17.797*10 ⁻³	3.466*10 ⁻³
Diode Solder	15.516*10 ⁻³	3.974*10 ⁻³
DCB	2.013686	4.12*10 ⁻⁴
Ceramic Bed	4.698374	18.8*10 ⁻³
DCB	2.013686	4.12*10 ⁻⁴
Solder	0.363059	6.79*10 ⁻⁴
Baseplate	237.43776	5.39*10 ⁻⁴
Thermal Paste	-	$1*10^{-4}$
Heat-Sink	9234	1*10-3

Table 3-8. Calculated Thermal Resistances and Capacitances for FF1000R17IP4 layers

3.4. THERMOELECTRIC MODELLING OF THE DUT

As the device studied is used in a braking chopper, there is no need to model switching losses. The I-V characteristics during conduction are modelled as given in the datasheet of the FF1400R17IP4 power module (Figure 3-18). Table 3-9 presents the explicit data inputted in the look-up table. These represent the source for heat-flow input of the thermal model.



Figure 3-18. I-V Characteristics of FF1400R17IP4 IGBT

T-11. 20	0	C1	- f (1 T	TT1 400D 17TT	1 ICDT	T 1- TT	T-1.1. D-4-
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1 abic 5 7.	Output	Characteristic	or the r	1 1 4001(1/11	T IOD I	LOOK OP	I doit Data

	0 A	200A	400A	600A	800A	1000A	1200A	1400A	1600A	1800A	2000A
25°	0.8V	1.2V	1.42V	1.6V	1.75V	1.84V	1.96V	2.1V	2.21V	2.33V	2.44V
125°	0.6V	1.05V	1.4V	1.6V	1.8V	1.95V	2.15V	2.28V	2.42V	2.55V	2.7V
150°	0.6V	1.05V	1.4V	1.6V	1.8V	1.95V	2.15V	2.28V	2.42V	2.55V	2.7V

Because of the interest to study more aspects of the heat transfer inside a power module, but also to have increased accuracy with the model, the DUT has been modelled as a thermal RC ladder network, taking into consideration constructive dimensions and physical characteristics of the materials used.

The layer thicknesses are similar to those of FF1000R17IE4 power module, but the chips have a different geometry. The dimensions were determined by direct measurement. The construction of the power module is illustrated in Figure 3-19. Table 3-10 presents the measurement results for each constructive layer.

Table 3-10. Physical Dimensions of Constructive Layers of FF1400R17IP4 Power Module

Layer	Length	Width	Height	Area	Volume
	[mm]	[mm]	[mm]	$[mm^2]$	[mm ³]
IGBT Metallisation	15.64	7.15	$4*10^{-3}$	111.83	0.447
Diode Metallisation	16.25	8.1	$4*10^{-3}$	131.625	0.5265
IGBT Chip	17.38	8.45	0.3	146.861	44.06
Diode Chip	18.85	9.27	0.3	174.74	52.422
IGBT Solder	17.38	8.45	0.05	146.861	7.343

Diode Solder	18.85	9.27	0.05	174.74	8.737
DCB Group 1	CG	CG	0.3	954.51	286.353
DCB Group 2	CG	CG	0.3	667.86	200.358
Ceramic Bed	53	43.56	0.7	2309.2	1616.465
DCB	51	41.5	0.3	2116.5	634.95
Solder	51	41.5	0.1	2116.5	211.65
Baseplate	250	89	3	22250	66750
Thermal Paste	250	89	-	22250	-
Heat-Sink	400	300	30	$12*10^4$	$3.6*10^{6}$

It can be noted that the IGBT chips are smaller, but doubled. This construction favours a reduced influence over the current flow through a chip, in case of single chip failures.



Figure 3-19. FF1400R17IP4 Open Module

Figure 3-20 illustrates a section of the thermal chain. It can be observed that the exact thermal paths are recreated, with only two limitations: the path through air / silicone gel is considered of infinite resistance, and the path through the baseplate between the chips is considered of zero resistance. This is done in order to keep within the model the main heat flow path, to the heat-sink, unharmed. The sequence 1-4 is repeated 12 times, as there are 12 chip pairs in the module, six for each IGBT/diode.



Figure 3-20. Thermal model of Device Under Test

In Figure 3-20, the marked RC components represent the layers as following:

- 1 Upper IGBT Network 1;
- 2 Upper IGBT Network 2;
- 3 Upper Diode Network;
- 4 Lower IGBT and Diode.

The values for thermal resistances and capacitances are calculated in the same manner presented in section 3.3. The chips may be considered to be pure silicon, as the impurities represent a very small part and do not have a considerable impact on material properties.

Material properties (specific heat capacity and thermal conductivity) are reminded in Table 3-11:

Layer	Material	Specific Heat	Thermal	Mass Density
		Capacity	Conductivity	$[Kg/m^3]$
		[J/Kg*K]	[W/m*K]	
IGBT	Al	950	250	2700
Metallisation				
Diode	Al	950	250	2700
Metallisation				
IGBT Chip	Si	790	83.6	2329
Diode Chip	Si	790	83.6	2329
IGBT Solder	Sn ₂ Zn ₂ Ag	260	78	7400
Diode Solder	Sn ₂ Zn ₂ Ag	260	78	7400
DCB	Cu	397	386	8960
Ceramic Bed	Al ₂ O ₃	880	18	3690
DCB	Cu	397	386	8960
Solder	Sn ₂ Zn ₂ Ag	260	78	7400
Baseplate	Cu	397	386	8960
Thermal Paste	-	-	16	
Heat-Sink	Al	950	250	2700

Table 3-11. Material Properties for FF1400R17IP4 Power Module

The thermal parameters, calculated using equations (3.4) and (3.5), are depicted in Table 3-12.

Table 3-12. Calculated Thermal Resistances and Capacitances for FF1400R17IP4 layers

Layer	Thermal Capacitance [J/K]	Thermal Resistance [K/W]
IGBT Metallisation	$1.1465*10^{-3}$	$143.074*10^{-6}$
Diode Metallisation	$1.35*10^{-3}$	$121.557*10^{-6}$
IGBT Chip	$81.066*10^{-3}$	24.435*10 ⁻³
Diode Chip	96.452*10 ⁻³	20.536*10 ⁻³
IGBT Solder	$14.128*10^{-3}$	$4.365*10^{-3}$
Diode Solder	16.81*10 ⁻³	$3.6685*10^{-3}$
DCB Group 1	1.0186	$8.142*10^{-4}$
DCB Group 2	0.7127	$11.6372*10^{-4}$
Thermal Coupling of Groups	-	1.5
Ceramic Bed	5.249	$16.84*10^{-3}$
DCB	2.2586	3.67*10 ⁻⁴
Solder	0.363059	$6.79*10^{-4}$
Baseplate	237.43776	$5.39*10^{-4}$
Thermal Paste	-	1*10 ⁻⁴
Heat-Sink	9234	1*10-3

3.5. SIMULATION RESULTS

The above described model was used to estimate chip temperature variations in different scenarios. It is of great interest to know for how long the IGBT can surge currents, for different current values and different ambient temperatures. As the braking chopper has no temperature control, it is necessary to understand its capabilities during FRT for different conditions that may appear inside a nacelle.

The first step is to observe the correlation between the instantaneous current through the DUT and forward voltage drop. Figure 3-21 depicts this variation for 2500 [A] collector current. It can be observed that, although the current stabilizes very fast, the forward voltage drop keeps getting bigger. This is due to its dependency to chip temperature. If comparing the values with those of Appendix 4 it can be observed that the forward voltage drop defined in the datasheet is the same for 2500 [A]. It can be concluded that the dynamic V_{CE} was implemented and scaled correctly and took into consideration all influential factors.





The temperature variation on control IGBTs and DUT is illustrated in Figure 3-22. It can be observed that the temperature on the 1400 [A] IGBT has a slower growth in the beginning, but reaches higher temperature, approximately 150 [°C]. The slower rise is caused by bigger thermal capacitances, but taking full load makes the DUT heat up more than the control IGBTs.



Figure 3-22. Junction Temperature Variation for DUT and Control IGBTs

The heat flow within the IGBT can be observed in Figure 3-23. In the upper graphic, the blue line represents the junction temperature of the active IGBT chip, while the red line is the junction temperature of its associated diode. The lower graph depicts the junction temperature for both IGBT and Diode that are inactive. There is no temperature difference between these two chips because the best path for heat flow is through the baseplate. The heating of inactive branch is also slower because practically the chips are heated by the baseplate, with added delays because the capacitances of all constructive layers.

There can also be remarked that the diode temperature remains considerably lower, as it is not used for freewheeling, and the only source of heat is the heat flow from the IGBT chip. It reaches a temperature of 90 [°C] only by this. The much shorter thermal path is reflected by the temperature difference between diode from active side and components from inactive side. The heat-up difference is of approximately 60 [°C].



Figure 3-23. Junction Temperatures on Chips of the Power Module

After verifying the functionality of the model, it was of great interest to establish a correlation between the measurable parameters – forward voltage drop and collector current – and the junction temperature, as representing the parameter that needs to be estimated. Figure 3-24 depicts their variation in the conditions of 2500 [A] forward current and 21 [°C] ambient temperature.





As these variations show, there is no simple linear relationship between the three involved parameters. Therefore, a more complex approach is considered.

A first step is to correct the input values from the linear range of the output characteristic, in order to fit a straight line (1st order polynomial). By taking the last seven values of V_{CE} , the results obtained are presented in Figure 3-25 – for 25 [°C], Figure 3-26 – for 125 [°C] and Figure 3-27 for 150 [°C].

It can be observed that the corrections applied are relatively small. Another advantage of the line fitting is that it allows reading the offset value of the line, if extended to 0 [A]. These values are: $V_{TH} = 0.995$ [V] for 25 [°C], $V_{TH} = 0.815$ [V] for 125 [°C] and $V_{TH} = 0.76$ [V] for 150 [°C].



Figure 3-25. Curve Fitting of V_{CE} for 25 [C]



Figure 3-26. Curve Fitting of V_{CE} for 125 [C]



Figure 3-27. Curve Fitting of V_{CE} for 150 [C]

Another important parameter extracted is the slope of the curves. They are as following:

$$\begin{split} m_{25^\circ} &= 5.47*10^{-4} \ [V/A]; \\ m_{125^\circ} &= 9.23*10^{-4} \ [V/A]; \\ m_{150^\circ} &= 1.017*10^{-3} \ [V/A]. \end{split}$$

It is necessary to analyse if the variation of the slope and threshold of the linearized output characteristic can be correlated to the temperature variation. It can be easily observed that the slope changes almost linear with the temperature, with a factor of 0.94 [mV/A] / 25 [°C].

The same thing can be said about the threshold value of the linearized characteristics. It can be estimated with good degree of confidence that the threshold decreases with 0.05 [V] for each 25 [°C] increase, having as a beginning point the value of 1 [V] for 25 [°C].

Under these conditions, the three characteristics intersect at the collector current value of 531.915 [A]. The collector-emitter voltage drop for this current is 1.291 [V].

Using the presented information, the logic described in the following is applied to estimate a junction temperature, having as inputs the current and voltage drop. Considering that at a certain collector current, the same voltage drop is inflicted, independent of the temperature, it can be said that:

$$\frac{I_C - 531.915}{V_{CE} - 1.291} = m_{T^\circ};$$

$$\frac{I_C - 531.915}{V_{CE_{25}} - 1.291} = m_{25^\circ};$$

The difference between the slope of the active V_{CE} and the slope for V_{CE} at 25 [°C] can be subjected to the correction factor of 0.94 [mV/A]/[°C]. A temperature correction results from the calculus, which will be added to the 25 [°C] that were initially considered.

The implementation in PLECS is presented in Figure 3-28. Figure 3-29 presents simulation results as comparison between measured and calculated junction temperature. It can be remarked that the difference is of 1.5 [°C], in a precautionary manner. Therefore it can be concluded that a relationship between forward voltage drop and junction temperature has been successfully established using this model.



Figure 3-28. Implementation of Junction Temperature Calculation



Figure 3-29. Measured T_J vs. Calculated T_J – Comparison

The simulations were repeated for the ambient temperature of 90 [°C], because the behaviour in different conditions is of interest, as it is not known the given ambient temperature in which the braking chopper will work. Figure 3-30 depicts the comparison between the junction temperatures of the DUT and control IGBTs. It can be observed that the simulation has been stopped when the temperature on the DUT reached the maximum allowed limit (165 [°C]). This is due to the control implemented, that turns off the control IGBTs in order to avoid destruction of the DUT.

The functionality of the temperature estimator has proven to be better in this case, having the estimated value with 1 [°C] higher than "measured". This is mainly due to the fact that the estimator is constructed using the values for high currents, because the consideration was to have a better accuracy near the maximum allowable temperature. Figure 3-31 depicts this scenario, where the red line depicts the calculated value, and the blue line refers to the measureable temperature.

Some estimation errors may be observed when the system switches off and while the DUT is not conducting current. These may be avoided by filtering the signal through slope limiters, by keeping the allowed slope below a maximum finite number and bigger than zero.



Figure 3-30. Junction Temperature Comparison for $T_{AMB} = 90$ [°C]



Figure 3-31. Junction Temperature Estimator Functionality for $T_{AMB} = 90$ [°C]

4. CONCLUSIONS

4.1. SUMMARY

This research project is focused on the thermal modelling of braking chopper IGBTs used to control the DC link voltage in wind turbine converters, with the purpose of realizing a temperature estimator for transient operation, which can be used as protection against destruction of power modules.

In order to fulfil the task, the process of carrying out this project and thesis report was divided into several tasks.

In the first chapter, general aspects justifying the use of braking choppers were presented. The wind energy trends and grid connection requirements were highlighted, in order to underline the importance of the V_{DC} control. The chapter contained the problem statement and defining of objectives, and ended with an overview on failure mechanisms in power modules and an overview of thermal modelling techniques.

The second chapter was dedicated to the design procedure for a test setup for single pulse short circuit testing of IGBT power modules. The system dimensioning and equipment choosing was presented in the first part. The chapter ended with a presentation of a Control PCB, designed especially for the dimensioned setup.

The third chapter dealt with the thermoelectric modelling of IGBT power modules for transient operation. In the beginning, general characteristics of the device were presented as a starting point and necessary background for loss modelling and temperature estimation. The chapter then described the models realized for the two different power modules presented in the previous chapter. The chapter ended with a presentation of edifying simulation results for the presented models.

4.2. OBJECTIVE FULFILMENT

The main objective of the project was to create a dynamic thermoelectric simulation model for the FF1400R17IP4 IGBT power module that simulates the operating conditions of a braking chopper for wind turbines. A complex ladder diagram that takes into consideration exact dimensions of layers, materials and heat flow paths through the power module was realized and presented. Its accuracy is validated through comparison with the foster network given in the datasheet of the transistor. The model is also extended to implement the dynamic voltage drop of the involved components.

Using the presented model, a simple and accurate estimator for junction temperature has been configured. The use of it is justified by its need of only electrical parameters as input, in order to estimate the instantaneous junction temperature of the analyzed device.

A test setup for single pulse short circuit testing of power modules was designed and presented. The setup has the quality of being self-controlled, based on a monostable and fault protection circuits.

The comparison between simulation results and measurements has not been presented due to the fact that the setup construction was not finished until publishing date of the report.
4.3. FUTURE WORK

The project presented in this report opens attractive directions for continuing this study. At first it should be stated that this thesis was focused on developing a novel thermal model that takes into consideration reciprocal influence of electric and thermal parameters, with the use of limited capability software. Therefore, improvements can be made to the presented models, to depict better the heat flow through a power module and reach a better accuracy.

A second work direction that can be stated is the building of a demonstrator, in order to study the accuracy of the presented models. For this, the second chapter of the thesis stands as a significant guideline, as it presents the complete dimensioning of such a test setup.

Another interesting research direction opened by this thesis is the transient thermal analysis of power modules that work under fast switching frequency and different load profiles. This is attractive especially in the perspective of extending the model with degradation models, and realize lifetime expectancy of devices subjected to stress.

Under the perspective of introduction of compact redundancy using temperature estimators to rebuff the use of a power module right before its destruction, the implementation of the estimators in control logic is wanted in the near future.

Estimators based on 2nd or bigger order curve fitting could be studied for a better accuracy.

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400V / 25V DELTA-DELTA TRANSFORMER DATASHEET





01-28-2013/12:02:54 General Data Seite 3
NOMINAL OPERATIONat Temperature W:38109°C 114.7 and Output Power of Transfor.U:42558 U:42558Output Power on LoadW:38109 W:96.4Output Power of Transfor.W:42558 V:42558Cu LossesW:96.4 Short-Circuit-Volt. cold %:14.13 Instantaneous pow.Fe-Losses activeW:105.8 K:68Instantaneous pow5/95&W:81227 W:81227Efficiency of Transformer %:98.43 dT Fe average Surface%K:75.7 K:76.5dT Gehäuse av.Surface°K:dT secondary°K:72.9
0.037Ω 0.038Ω 398.6U 0.038Ω 0.038Ω 397.3 U −0.39 ° 0.33 × 0.34 × 99.7 × 0.34 × 99.32 ×
1 11.12 Ω 400. U 1502 Ω 28687 Ω 1643 Ω 100 × 13508 × 14773 × 35.97 A 5.549 nF . mH 11.12 Ω 35.97 A 35.70 A
100.7 % 1.025T 100 %
DUTY CYCLE OPERATION at Amb.Temperature °C 40. and Overvoltage 1.00 dT Fe average Surface °K:75.7 dT primary °K:76.5 dT Gehäuse av. Surface °K:. dT secondary °K:73.
NO LOAD OPERATION at Amb.Temperature °C 40. and Overvoltage 1.00 Losses active W:106.5 Losses reactive UAr:96.84 Current factor %:1. Induction T:1.029 dT Fe average Surface °K:50.7 dT primary °K:40.4 dT Gehäuse av. Surface °K: Rezonance frequency kHz:1.3
SHORT-CIRCUIT OPERATION at Amb.Temperature °C 40. and Overvoltage 1.00 Losses active W:98168 Losses reactive UAr:4985. Current factor cold %:707.7 Induction T:.407 dT Fe average Surface °K:7220. dT primary °K:9237. dT Case aver. Surface °K: dT secondary °K:4874.
PRIMARY (Tap:1) 1 2 3 5 6 7 8 Voltage Input/Output U:400. Out. Voltage no load U: Current Input/Output A:35.97 Courrent Input/Output Q: Q: Power factor of load : Current in segment A:35.97 Current in segment A:35.97 Current dencity A/m*2:1.22 Icc-Current cold A:254.5 Io Ioc -Current cold A:254.5 Io -Current main A:3567.1 Inrush Current peak A:567.1 Inrush Current rms A:237.7 Cu-Losses V:48. Resistance cold Q::0255 Reactance Q::0383 Eddy-Current Factor :1.05
SECONDARY 1 2 3 4 5 6 7 8 Output Voltage V:24.88 Output Current A:1531. Out. Voltage no load V:25.06 Sec. Voltage Sec. Voltage V:19.62 Sec. Voltage cold V:19.7 Load on output \$1.000 Icc cold Curcent a:5151. Cu

DIODE POWER MODULE DATASHEET

Ν	÷	 	- D	atenb	latt	: / D	ata sh	eet		ēû	ipe	Ĉ
N Rec	letz-Dioo ctifier Di	den-Modul iode Module		DD540N								
	DD540N											
Elekt	Elektrische Elgenschaften / Electrical properties											
Peri	odische Sj attive peak	e wene / Maxim pitzensperrspan i reverse voltage	nung 86	aues	T _e	-40°C	T _{v[max}	Vr	RM	2000 2400	2200 2600	v
Stol non-	Sepitzensp repetitive	errspannung peak reverse vo	tage		T _{el}	+25°C	T _{v[max}	Ve	EM.	2100 2500	2300 2700	v
Duro	chiaßstrom Imum RMS	-Grenzeffektivw S on-state currer	ert nt					les			900	Α.
Dau aver	ergrenzstr rage on-sta	om ate current			Tc Tc	- 100°C - 95°C		lea	WM		540 573	A A
Stol	Sstrom-Gre	enzwert			T _{el}	- 25 °C, t _i	• = 10 ms • = 10 ms	les	м		16.500 14.000	A A
Gree Pt-va	nziastinteg alue	rai			T _e	- 25 °C, t _r	= 10 ms p = 10 ms	Pt		1	.360.000 980.000	A⁼s A⁼s
Dur on-s	raktenstisk chlaßspan state voltag	nung je	ractenistic v	alues	T _{el}	- T _{vj max} , l _i	F = 1700 A	'	VF	max.	1,48	v
Schi	ieusenspa shold volta	nnung			T _{el}	- T _{vjmax}		'	V _(TO)		0,78	v
Ersa	atzwidersta e resistan	and ce			T _{el}	- T _{vj max}			ſτ		0,31	mΩ
Spe	rrstrom	t			T _{el}	- T _{vjmax} , v	/ _R = V _{RRM}	1	R	max.	40	mA
Isola	ations-Prüf ilation test	spannung voltage			RJ RJ	MS, 1 - 50 MS, 1 - 50	Hz, t = 1 sec Hz, t = 1 min		VISOL		3,6 3,0	k∨ k∨
								I				
Inne	mische Ei erer Wärme	genschaften / 1 ewiderstand	hermal pro	operties	pr	o Modul /	per Module, O = 1	180° sin	Reuc	max.	0,0390	"C/W
then	mai resista	ance, junction to	case		pr pr	o Zweig / o Modul / o Zweig /	per arm, O = 180' per Module, DC per arm, DC	'sin		max. max. max.	0,0780 0,0373 0,0745	-CW
Übe	rgangs-W	armewiderstand			pr	o Modul /	per Module		Reat	max.	0,01	*C/W
Höc	mai resista hstzulässi	ance, case to ne ge Sperrschichtt	emperatur		- pr	0 Zweg /	per aim		T _{vj max}	max.	150	*C
Betr	rebstempe rating temp	ratur perature	e		+				Tcop	-4	40+150	• c
Lag	ertemperal age tempe	tur rature			╈				T _{alg}	- 4	40+150	•c
					<u> </u>							
pre	pared by:	C. Drilling		date of public	ation: (06.05.03						
app	roved by.	M. Leileid		lev	ISION.	1						
BIP AC	/ 95-04-2	21, KA. Rüthe	er	A10	9/95					Seite	e/page	1/9

Ν		Datenbl	att / Data she	eet	Eŭpe	
N Re	letz-Dioden-Modul ctifier Diode Module		DD540N			
Mer	chanische Elgenschaften / Mec näuse, siehe Anlage e. see anner	chanical properties			Sette 3 page 3	
SI-E SI-E	Element mit Druckkontakt				hudr -	
Inne	ere isolation				AIN	
Anz	ugsdrehmoment für mechanisch	e Anschlüsse	Toleranz ±15%	M1	6	Nm
Anz	ugsdrehmoment für elektrische /	Anschlüsse	Toleranz ±10%	M2	12	Nm
Gew	Acht			G	typ. 1500	g
Krie	enstrecke				19	mm
Sch	wingfestigkeit ation resistance		f = 50 Hz		50	m/s²
	2//		file-No.		E 83336	
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Ν	\rightarrow		Date	nblatt	/ Data	sheet	ĒŨ	Öec		
F	Netz-Diode Rectifier Diod	n-Modul de Module		DD	540N					
ſ	Natürliche Kühlung / Natural cooling 1 Modul pro Kühler / 1 module per heatsink Kühler / Heatsink type: KM17 (160W)									
ſ		Ana	alytische Elem Analytical ele	ente des trans ments of trans	ienten Wärmew ient thermal im	viderstandes Z pedance Z _{BICA}	BCA.		1	
	Pos. n	1	2	3	4	5	6	7	1	
	R _{thn} [°C/W]	0,00672	0,0537	0,539					1	
	T _n [s]	2,17	22,4	1130					1	
	Verstärkte Kühlung / Forced cooling 1 Modul pro Kühler / 1 module per heatsink Kühler / Heatrink tyme: KM17 / Parent 4650)									
ľ		An	alytische Elem Analytical ele	ente des trans ments of trans	ienten Wärmew ient thermal im	viderstandes Z pedance Z thca	B CA		1	
	Pos. n	1	2	3	4	5	6	7	1	
	R _{thn} [°C/W]	0,0064	0,0566	0,168					1	
	T _n [s]	4,1	24,7	395					1	
					-	n _{max}	- (-±	1	1	
	Analy	tische Funktion	/ Analytical fun	ction:	2	$L_{\text{thCA}} = \sum_{n=1}^{\infty} I$	R _{thn} [1 -e ⁵	J		
BIP	AC / 95-04-21,	KA. Rüther		A109/95			Seite/	page 5/9		









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- die gemeinsame Durchf
 ührung eines Risiko- und Qualitätsassessments;
 den Abschluss von speziellen Qualitätsicherungsvereinbarungen;
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 ührung von Ma
 ßnahmen zu einer laufenden Produktbeobachtung dringend empfehlen und gegebenenfalls die Beileferung von der Umsetzung solcher Ma
 ßnahmen abh
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- the conclusion of Quality Agreements;
- to establish joint measures of an ongoing product survey, and that we may make delivery depended on the realization of any such measures.

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1000 A 1700 V IGBT POWER MODULE DATASHEET



Technische Information		Infineon								
IGBT-Module IGBT-modules	FF1000R17IE4				حالا	-				
IGBT-Wechselrichter / IGBT Höchstzulässige Werte / Maximur	-inverter n Rated Values									
Kollektor-Emitter-Spenspannung Collector-emitter voltage	T _{vj} = 25*C		VCES		1700		v			
Kollektor-Dauergleichstrom Continuous DC collector current	T _C = 100°C, T _{vi} = 175°C T _C = 25°C, T _{vi} = 175°C		IC nom		1000 1390		A A			
Periodischer Kollektor-Spitzenstrom Repetitive peak collector current	te = 1 ms		ICRM		2000		Α			
Gesamt-Verlustielstung Total power dissipation	T _C = 25°C, T _{vj} = 175°C		Ptot		6,25		ĸw			
Gate-Emitter-Spitzenspannung Gate-emitter peak voltage			VGES		+/-20		۷			
Charakteristische Werte / Charac	teristic Values			min.	typ.	max.				
Kollektor-Emitter-Sättigungsspannung Collector-emitter saturation voltage	Ic = 1000 A, V _{GE} = 15 V Ic = 1000 A, V _{GE} = 15 V Ic = 1000 A, V _{GE} = 15 V	$\begin{array}{l} T_{\nu j} = 25^{\circ}C \\ T_{\nu j} = 125^{\circ}C \\ T_{\nu j} = 150^{\circ}C \end{array}$	V _{CE set}		2,00 2,35 2,45	2,45 2,80	v v v			
Gate-Schweilenspannung Gate threshold voltage	Ic = 36,0 mA, V _{CE} = V _{GE} , T _{vj} = 25°C		VGEm	5,2	5,8	6,4	v			
Gateladung Gate charge	V _{GE} = -15 V +15 V		QG		10,0		μC			
Interner Gatewiderstand Internal gate resistor	T _{vj} = 25°C		R _{Gint}		1,5		Ω			
Eingangskapazität Input capacitance	f = 1 MHz, T _{vj} = 25°C, V _{CE} = 25 V, V _{GE} = 0 V		Cies		81,0		nF			
Rückwirkungskapazität Reverse transfer capacitance	f = 1 MHz, T _{vj} = 25°C, V _{CE} = 25 V, V _{GE} = 0 V		Gree		2,60		nF			
Kollektor-Emitter-Reststrom Collector-emitter cut-off current	V _{CE} = 1700 V, V _{GE} = 0 V, T _{vj} = 25°C		ICES			5,0	mA			
Gate-Emitter-Reststrom Gate-emitter leakage current	V _{CE} = 0 V, V _{GE} = 20 V, T _{vj} = 25°C		IGES			400	nA			
Einschaltverzögerungszeit, induktive Last Turn-on delay time, inductive load	Ic = 1000 A, V _{CE} = 900 V V _{GE} = ±15 V R _{Gen} = 1,2 Ω	T _{vi} = 25°C T _{vi} = 125°C T _{vi} = 150°C	t _{e on}		0,55 0,60 0,60		µs µs µs			
Anstiegszeit, Induktive Last Rise time, Inductive load	Ic = 1000 A, V _{CE} = 900 V V _{GE} = ±15 V R _{Ben} = 1,2 Ω	T _{vj} = 25°C T _{vj} = 125°C T _{vj} = 150°C	ţ,		0,10 0,12 0,12		на ра ра			
Abschaltverzögerungszeit, induktive Last Turn-off delay time, inductive load	Ic = 1000 A, V _{CE} = 900 V V _{GE} = ±15 V R _{Geff} = 1,8 Ω	$\begin{array}{l} T_{vj} = 25^{\circ}C \\ T_{vj} = 125^{\circ}C \\ T_{vj} = 150^{\circ}C \end{array}$	te orr		1,00 1,25 1,30		на На На			
Failzeit, induktive Last Fail time, inductive load	Ic = 1000 A, V _{CE} = 900 V V _{GE} = ±15 V R _{Geff} = 1,8 Ω	$T_{vj} = 25^{\circ}C$ $T_{vj} = 125^{\circ}C$ $T_{vj} = 150^{\circ}C$	t,		0,29 0,50 0,59		µs µs µs			
Einschaltverlustenergie pro Puls Turn-on energy loss per pulse	I _C = 1000 A, V _{CE} = 900 V, L _S = 30 nH V _{GE} = ±15 V, dkdt = 8000 A/μs (T _{v1} =150°C) R _{Gen} = 1,2 Ω	$\begin{array}{l} T_{vj} = 25^{\circ}C \\ T_{vj} = 125^{\circ}C \\ T_{vj} = 150^{\circ}C \end{array}$	Eon		265 390 415		EJ EJ			
Abschaltverlustenergie pro Puls Tum-off energy loss per pulse	$\begin{array}{l} I_{C} = 1000 \; A, \; V_{CE} = 900 \; V, \; L_{8} = 30 \; nH \\ V_{GE} = \pm 15 \; V, \; du/dt = 3000 \; V/\mu s \; (T_{vj} = 150^{\circ} C) \\ R_{Geff} = 1,8 \; \Omega \end{array}$	$\begin{array}{l} T_{vj} = 25^{\circ}C \\ T_{vj} = 125^{\circ}C \\ T_{vj} = 150^{\circ}C \end{array}$	Eott		200 295 330		면 더 더 더			
Kurzschlußverhalten SC data	V _{GE} ≤ 15 V, V _{CC} = 1000 V V _{CEmax} = V _{CES} -L _{sCE} -dl/dt t _P ≤ 10 µs	, T _{vj} = 150°C	lac		4000		A			
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro IGBT / per IGBT		RINC			24,0	KAKW			
Wärmewiderstand, Gehäuse bis Kühikörper Thermal resistance, case to heatsink	pro IGBT / per IGBT λPeste = 1 W/(m-K) / λgreese = 1 W/(m-K)		ReCH		9,00		KANW			
prepared by: TA	date of publication: 2012-03-15									
approved by: PL	revision: 3.2									
	2									

Technische Information / technical information				Infineon						
IGBT-modules FF1000R17IE4				-	-	-				
Diode-Wechselrichter / Dio	de-inverter									
Periodische Spitzensperrspannung Repetitive peak reverse voltage	T _{vj} = 25°C		VRRM		1700		v			
Dauergleichstrom Continuous DC forward current			lF		1000		Α			
Periodischer Spitzenstrom Repetitive peak forward current	te = 1 ms		IFRM		2000		A			
Grenziastintegral Pt - value	V _R = 0 V, t _P = 10 ms, T _{vj} = 125°C		Pt		140		KA3			
Charakteristische Werte / Chara	cteristic Values			min.	typ.	max.				
Durchlassspannung Forward voltage	IF = 1000 A, V _{GE} = 0 V IF = 1000 A, V _{GE} = 0 V IF = 1000 A, V _{GE} = 0 V	T _{v1} = 25°C T _{v1} = 125°C T _{v1} = 150°C	VF		1,85 1,95 1,95	2,25 2,35	V V V			
Rückstromspitze Peak reverse recovery current	IF = 1000 A, - dF/dt = 8000 A/µs (T _{v1} =150°C) VR = 900 V VGE = -15 V	T _{vi} = 25°C T _{vi} = 125°C T _{vi} = 150°C	IRM		1050 1200 1250		AAAA			
Sperrverzögerungsladung Recovered charge	IF = 1000 A, - dF/dt = 8000 A/µ5 (T _{vj} =150°C) VR = 900 V Vac = -15 V	T _{vi} = 25°C T _{vi} = 125°C T _{vi} = 125°C	Q,		245 410 480					
Abschaltenergie pro Puls Reverse recovery energy	IF = 1000 A, - dir/dt = 8000 A/µs (T _{v1} =150°C) VR = 900 V VGE = -15 V	T _{v1} = 25°C T _{v1} = 125°C T _{v1} = 150°C	Erec		115 205 245		m. m. m.			
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro Diode / per diode	-	ReJC			48,0	K/K			
Wärmewiderstand, Gehäuse bis Kühikörpe Thermai resistance, case to heatsink	pro Diode / per diode λPerte = 1 W/(m·K) / λgreese = 1 W/(m·K)		Rech		18,0		K/K			
NTC-Widerstand / NTC-the Charakteristische Werte / Charae Nennwiderstand	rmistor steristic Values		Ras	min.	typ.	max.	kC			
Abwelchung von R100	T _C = 100°C, R ₁₀₀ = 493 Ω		∆R/R	-5		5	%			
Verlustielistung Power dissipation	T _C = 25°C		P25			20,0	mV			
B-Wert B-value	R2 = R25 exp [B25/50(1/T2 - 1/(298,15 K))]		B25/50		3375		к			
B-Wert B-value	R ₂ = R ₂₅ exp [B _{25/80} (1/T ₂ - 1/(298,15 K))]		B25/80		3411		к			
B-Wert B-value	R ₂ = R ₂₅ exp [B _{25/100} (1/T ₂ - 1/(298,15 K))]		B25/100		3433		к			
specification according to the valid application	n note.									
prepared by: TA	date of publication: 2012-03-15									

Technische Information	1	Infl	ine	00		
IGBT-Module IGBT-modules	FF1000R17IE4					
Modul / Module						
Isolations-Prüfspannung Isolation test voltage	RMS, f = 50 Hz, t = 1 min.	VisoL		4,0		kV
Material Modulgrundplatte Material of module baseplate				Cu		
Innere Isolation Internal Isolation				Al ₂ O ₃		
Kriechstrecke Creepage distance	Kontakt - Kühikörper / terminai to heatsinik Kontakt - Kontakt / terminai to terminai			33,0 33,0		mm
Luftstrecke Clearance	Kontakt - Kühikörper / terminai to heatsink Kontakt - Kontakt / terminai to terminai			19,0 19,0		mm
Vergleichszahl der Kriechwegblidung Comperative tracking index		СТІ		> 400		
Wärmewiderstand, Gehäuse bis Kühikörper Thermai resistance, case to heatsink	pro Modul / per module λ _{Pente} = 1 W/(m·K) / λ _{artesta} = 1 W/(m·K)	Rech	min.	typ. 3,00	max.	KAKW
Moduistreuinduktivität Stray inductance module		LICE		10		nH
Modulieltungswiderstand, Anschlüsse - Chij Module lead resistance, terminals - chip	T _C = 25°C, pro Schatter / per switch	RCC'4EE'		0,20		mΩ
Höchstzulässige Spenschichtlemperatur Maximum junction temperature	Wechseirichter, Brems-Chopper / Inverter, Brake-Chopper	T _{vj max}			175	•c
Temperatur im Schaitbetrieb Temperature under switching conditions	Wechselrichter, Brems-Chopper / Inverter, Brake-Chopper	T _{vj os}	-40		150	•C
Lagertemperatur Storage temperature		T _{stp}	-40		150	•c
Anzugsdrehmoment f. Modulmontage Mounting torque for modul mounting	Schraube M5 - Montage gem. gültiger Applikation Note screw M5 - mounting according to valid application note	м	3,00	-	6,00	Nm
Anzugsdrehmoment f. eiektr. Anschlüsse Terminal connection torque	Schraube M4 - Montage gem. gültiger Applikation Note screw M4 - mounting according to valid application note Schraube M6 - Montage gem. gültiger Applikation Note screw M8 - mounting according to valid application note	м	1,8 8,0	-	2,1 10	Nm Nm
Gewicht Weight		G		1200		g
prepared by: TA	date of publication: 2012-03-15					
approved by: PL	revision: 3.2					
	4					











Technische Informatio	n / technical information	Infineon				
IGBT-Module IGBT-modules	FF1000R17IE4					
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Due to technical requirements our prod contact the sales office, which is respo	uct may contain dangerous substances. For information sible for you.	n on the types in question please				
Contact the sales office, which is responsible for you. Should you intend to use the Product in aviation applications, in health or live endangering or life support applications, please notify. Please note, that for any such applications we urgently recommend - to perform joint Risk and Quality Assessments; - the conclusion of Quality Agreements; - to establish joint measures of an ongoing product survey, and that we may make delivery depended on the realization of any such measures.						
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1400 A 1700 V IGBT POWER MODULE DATASHEET



Technische Information / technical information FF1400R17IP4			Infineon					
IGBT-Wechselrichter / IGBT-inverter					ige D nary)ater data	1	
Kolektor-Emitter-Spenspannung	m Rated Values T _{vl} = 25°C		VCES		1700		v	
Kollektor-Dauergleichstrom Continuous DC collector current	T _C = 100°C, T _{vj} = 175°C		IC nom		1400		A	
Periodischer Kollektor-Spitzenstrom Repetitive peak collector current	t⊳ = 1 ms		ICRM		2800		A	
Gesamt-Verlustielstung Total power dissipation	Tc = 25°C, T _{vi} = 175°C		Ptot		9,55		kW	
Gate-Emitter-Spitzenspannung Gate-emitter peak voltage			VGES		+/-20		v	
Charakteristische Werte / Charac	teristic Values			min	turn.	max		
Kollektor-Emitter-Sättigungsspannung Collector-emitter saturation voltage	Ic = 1400 A, V _{GE} = 15 V Ic = 1400 A, V _{GE} = 15 V Ic = 1400 A, V _{GE} = 15 V	$\begin{array}{l} T_{vj} = 25^{\circ}C \\ T_{vj} = 125^{\circ}C \\ T_{vj} = 150^{\circ}C \end{array}$	V _{CE est}		1,75 2,10 2,20	2,20	v v v	
Gate-Schwelienspannung Gate threshold voltage	I _C = 50,0 mA, V _{CE} = V _{GE} , T _{vj} = 25°C		VGEI	5,2	5,8	6,4	v	
Gateladung Gate charge	V _{GE} = -15 V +15 V		QG		13,5		μC	
Interner Gatewiderstand Internal gate resistor	T _{vi} = 25°C		R _{Gint}		1,6		Ω	
Eingangskapazität Input capacitance	f = 1 MHz, T _{vi} = 25°C, V _{CE} = 25 V, V _{GE} = 0 V		Cies		110		nF	
Rückwirkungskapazität Reverse transfer capacitance	f = 1 MHz, T _{vi} = 25°C, V _{CE} = 25 V, V _{GE} = 0 V		C _{res}		3,60		nF	
Kollektor-Emitter-Reststrom Collector-emitter cut-off current	V _{CE} = 1700 V, V _{GE} = 0 V, T _{vj} = 25°C		ICES			5,0	mA	
Gate-Emitter-Reststrom Gate-emitter leakage current	V _{CE} = 0 V, V _{GE} = 20 V, T _{vj} = 25°C		IGES			400	nA	
Einschaftverzögerungszeit, Induktive Last Turn-on delay time, Inductive load	Ic = 1400 A, V _{CE} = 900 V V _{GE} = ±15 V R _{Gen} = 0,47 Ω	T _{vj} = 25°C T _{vj} = 125°C T _{vj} = 150°C	t _{el on}		0,84 0,88 0,89		he he he	
Anstiegszeit, induktive Last Rise time, inductive load	I _C = 1400 A, V _{CE} = 900 V V _{GE} = ±15 V R _{Gen} = 0,47 Ω	T _{vj} = 25°C T _{vj} = 125°C T _{vj} = 150°C	ţ,		0,13 0,14 0,14		au au au	
Abschaltverzögerungszeit, Induktive Last Turn-off delay time, Inductive load	Ic = 1400 A, V _{CE} = 900 V V _{GE} = ±15 V R _{Geff} = 0,68 Ω	$\begin{array}{l} T_{vj} = 25^{\circ}C \\ T_{vj} = 125^{\circ}C \\ T_{vj} = 150^{\circ}C \end{array}$	te orr		1,15 1,35 1,40		µs µs µs	
Failzet, Induktive Last Fail time, Inductive load	Ic = 1400 A, V _{CE} = 900 V V _{GE} = ±15 V R _{Geff} = 0,68 Ω	T _{vj} = 25°C T _{vj} = 125°C T _{vj} = 150°C	t,		0,50 0,77 0,79		µs µs µs	
Einschaltverlustenergie pro Puis Turn-on energy loss per puise	$\begin{array}{l} I_C = 1400 \; \text{A}, \; V_{CE} = 900 \; \text{V}, \; L_8 = 30 \; \text{nH} \\ V_{GE} = \pm 15 \; \text{V}, \; \text{divid} = 9500 \; \text{A/µs} \; (\text{T}_{vl} = 150^{\circ}\text{C}) \\ \text{R}_{\text{Gen}} = 0.47 \; \Omega \end{array}$	$\begin{array}{l} T_{vj} = 25^{\circ}C \\ T_{vj} = 125^{\circ}C \\ T_{vj} = 150^{\circ}C \end{array}$	Eon		340 500 560		222	
Abschältverlustenergie pro Puls Turn-off energy loss per pulse	$\begin{array}{l} I_C = 1400 \; A, \; V_{CE} = 900 \; V, \; L_8 = 30 \; nH \\ V_{GE} = \pm 15 \; V, \; du/dt = 2500 \; V/\mu s \; (T_{vJ} = 150^{\circ} C) \\ R_{Geff} = 0.68 \; \Omega \end{array}$	T _{vi} = 25°C T _{vi} = 125°C T _{vi} = 150°C	Eorr		440 625 650		222	
Kurzschlußverhalten SC data	V _{GE} ≤ 15 V, V _{CC} = 1000 V V _{CEmax} = V _{CES} - L _{sCE} - dl/dt t _P ≤ 10 µs	, T _{vj} = 150°C	lac		5600		A	
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro IGBT / per IGBT		RedC			15,5	KAKW	
Wärmewiderstand, Gehäuse bis Kühikörper Thermal resistance, case to heatsink	pro IGBT / per IGBT λPmte = 1 W/(m·K) / λgreese = 1 W/(m-K)		Rach		11,5		KAKW	
prepared by: TA	date of publication: 2012-04-12							
approved by: PL	revision: 2.4							
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Technische Information / technical information FF1400R17IP4			Infineon					
Diode-Wechselrichter / Dio Höchstzulässige Werte / Maximu	de-inverter m Rated Values	Vor Pre	läuf limi	ige E nary)ater data	1		
Periodische Spitzensperrspannung Repetitive peak reverse voltage	T _{v1} = 25*C	VRRM		1700		v		
Dauergleichstrom Continuous DC forward current		IF		1400		Α		
Periodischer Spitzenstrom Repetitive peak forward current	t⊳ = 1 ms	IFRM		2800		Α		
Grenziastintegral Pt - value	V _R = 0 V, t _P = 10 ms, T _{v1} = 125°C	Pt		200		kAR		
Spitzenveriustielstung Maximum power dissipation	T _{vj} = 125*C	PROM		1400		kW		
Charakteristische Werte / Charac	teristic Values		min.	typ.	max.			
Durchlassspannung Forward voltage	$ \begin{array}{l} {}_{I\!$	VF		1,75 1,80 1,80	2,45	V V V		
Rückstromspitze Peak reverse recovery current	$\begin{array}{l} I_{\rm F} = 1400 \; A_{\rm v} - dI_{\rm F}/dt = 10000 \; A/\mu s \; (T_{\rm vI} = 150^{\circ} C) \; T_{\rm vI} = 25^{\circ} C \\ V_{\rm R} = 900 \; V \\ V_{\rm GE} = -15 \; V \\ \end{array} \\ \begin{array}{l} T_{\rm vI} = 125^{\circ} C \\ T_{\rm vI} = 150^{\circ} C \end{array}$	IRM		1500 1650 1700		A A A		
Sperrverzögerungsladung Recovered charge	IF = 1400 A, - dIF/dt = 10000 A/µs (Tvj=150*C) Tvj = 25*C VR = 900 V V _{GE} = -15 V Tvj = 125*C Tvj = 150*C	Q,		345 585 650		μC μC		
Abschaltenergie pro Puls Reverse recovery energy	IF = 1400 A, - dIF/dt = 10000 A/µs (T _{v1} =150°C) T _{v1} = 25°C VR = 900 V V _{GE} = -15 V T _{v1} = 125°C T _{v1} = 150°C	Erec		195 345 385		m. m.		
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro Diode / per diode	Rinjc			32,5	K/M		
Wärmewiderstand, Gehäuse bis Kühikörper Thermai resistance, case to heatsink	pro Diode / per diode λPerte = 1 W/(m-K) / λgreese = 1 W/(m-K)	Rech		11,5		K/k/		
NTC-Widerstand / NTC-the Charakteristische Werte / Charao	rmistor teristic Values		min.	typ.	max.			
Rated resistance	Tc = 25°C	R25		5,00		kΩ		
Abweichung von R100 Devlation of R100	T _C = 100°C, R ₁₀₀ = 493 Ω	∆R/R	-5		5	%		
Verlustleistung Power dissipation	T _C = 25°C	P25			20,0	mV		
B-Wert B-value	R ₂ = R ₂₅ exp [B _{25/50} (1/T ₂ - 1/(298,15 K))]	B25/50		3375		к		
B-Wert B-value	R ₂ = R ₂₅ exp [B _{25/80} (1/T ₂ - 1/(298,15 K))]	B25/80		3411		к		
B-Wert B-value	R ₂ = R ₂₅ exp [B _{25/100} (1/T ₂ - 1/(298,15 K))]	B25/100		3433		к		
Angapen gemas guilager Application Note. Specification according to the valid applicatio	n note.							
prepared by: TA	date of publication: 2012-04-12							

Technische Information / technical information FF1400R17IP4			Infineon					
Modul / Module	Vorläufige Daten Preliminary data							
Isolations-Prüfspannung Isolation test voltage	RMS, f = 50 Hz, t = 1 min.	VisoL		4,0		kV		
Material Modulgrundplatte Material of module baseplate				Cu				
Innere Isolation Internal Isolation				Al ₂ O ₃				
Kriechstrecke Creepage distance	Kontakt - Kühikörper / terminai to heatsink Kontakt - Kontakt / terminai to terminai			33,0 33,0		mm		
Lufistrecke Clearance	Kontakt - Kühlikörper / terminai to heatsinik Kontakt - Kontakt / terminai to terminai			19,0 19,0		mm		
Vergleichszahl der Kriechwegblidung Comperative tracking Index		СТІ		> 400				
Modulstreuinduktvität		Los	min.	typ. 10	max.	nH		
Stray inductance module Modulieitungswiderstand, Anschlüsse - Chip	Tc = 25°C, pro Schatter / per switch	Recuse		0.20		mΩ		
Höchstzulässige Spertschichttemperatur Maximum lunction temperature	Wechselrichter, Brems-Chopper / Inverter, Brake-Chopper	T _{vj min}		-	175	•c		
Temperatur im Schaltbetrieb	Wechselrichter, Brems-Chopper / Inverter, Brake-Chopper	T _{vj co}	-40		150	•c		
Lagertemperatur Storage temperature		Teta	-40		150	•c		
Anzugsdrehmoment f. Modulmontage Mounting torque for modul mounting	Schraube M5 - Montage gem. güitiger Applikation Note screw M5 - mounting according to valid application note	м	3,00	-	6,00	Nm		
Anzugsdrehmoment f. elektr. Anschlüsse Terminal connection torque	zugsdrehmoment f. elektr. Anschlüsse minal connection forque screw M4 - Montage gen, gültiger Applikation Note screw M4 - mounting according to valid application note		1,8	-	2,1	Nm		
	Schraube M8 - Monfage gem. gültger Appilkation Note screw M8 - mounting according to valid application note	M	8,0	-	10	Nm		
Gewicht Weight		G		1200		g		
prepared by: TA approved by: PL	date of publication: 2012-04-12 revision: 2.4							
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Vorläufige Daten Preliminary data Nutzungsbedingungen Die in diesem Produktiatenbilt enthellenen Daten sind ausschließlich für lichnisch geschüles Fachpersonal bestmitting peurfaltung der Eignung diese Produktes für ihre Anwendung sowie die Beurfellung der Vollstandigsten tor bereitgestellen Produktiaten für diese Anwendung obligg fitnen bzw. Ihren lichnischen Ableilungen. In desem Produktiatenbilt enthelsen dieseing Mechaniae beschriebes. Tür die wie intervertragische Gewährleibung übernehmen. Eine soche Gewährleibung (richel sich ausschließlich nach Matgabe der in jeweitigen Lishrvertrag entheltenen Bestimmungen. Geranten jeglichen Att werden für die Berodukt due desen Eigenschaften seinserfalls fullen somennen. Solfen Sie von um Produktionten allemen beoligen, die über den Inhal diesen Produktionen seinen Sie und den Einzal dasse Produktionen seinen Sie sich die händ diesen Produktionen seinen Sie und den Täss zusändigen Vertiebebärb in Verbindung (seine www.infinson.com, Vertrebäkkontakt). Für interessenten halten wir Application Noles bereit. Aufgrund der fachtleichen Antorderungen Könte umse Produktigeunden die mit zusändigen Vertrebebärb in Verbindung (seine sweithellenen Statuszen enthellenen Statuszen enthellenen Statuszen enthellenen die die Bestellerung von Matgatamen zu ihrer Lunndnen Pro- aussingensensenten. Solfen Sie bestechtigen, das Produkt in Anwendungen der Luffahrt, in gesundheite, vollen das für Ables. Der Klösseg einstelle. Solfen Sie bestechtigen, das Produktion beschnetenente: Begensensentationen Anwendungen der Luffahrt, in gesundheite zusändenen zusändenen vertrebestelle einstellenen alten alten vertrebestellenen derestellenen danalten seisentellenen der der Statuszen einstellenen	Technische Information	/ technical information FF1400R17IP4	Infineon
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De in diesem Produktigenbigt erhaltenen Daten eind ausschließlich für ischnisch geschuftes Fachpersonal bestimmt. Die Beurfaltung der Eignung dieses Produktigen für hirs Anwendung sowie die Beurfaltung der Vollständigkeit der berätgestellten Produktigen für diese Anwendung oblegt finnen bezu. Ihnen technischen Ableilungen. Aussen Produktigen der Benzung diese Thomatiken ableitungen. Eine schlen Gewährstellung (Toffer eine Befarvertrag gehärben ander Benzung der Vollständigkeit der berätgestellten Schlensen Benzung der Benzun	Nutzungsbedingungen		
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ABB ES2000S CURRENT SENSOR DATASHEET



The caracteristics detailed in this leaflet are subject to change without prior notice. Les caractéristiques détaillées dans cette brochure sont susceptibles d'évoluer sans notification préalable.

ABB Entrelec	SENSOR /	Issued: 1995.05.22			
10, Rue Ampère 69680 Chassieu, FRANCE Tel : +33 (0)4 72 22 17 22 Fax : +33 (0)4 72 22 19 35	Commercial reference référence commerciale ES2000S	Order code Référence de commande 1SBT152000R0002	Emis le : Modification : 2 Date : 2003.01.20 Page 2/2		
CHARACTERISTICS	CARACTERISTIQUES				
Nominal primary current (I _{PN})	Courant primaire nominal (I _{PN})	A r.m.s. (A eff.)	: 2000		
Measuring range (I _P max)	Plage de mesure (I _p max)	A peak (A crête)	: ±3000		
Max. measuring resistance (R _M max)	Résistance de mesure max. (R_M 1	παχ) 🖸	: 11 (@I _p max / ±24V (±5%))		
Min. measuring resistance (R _M min)	Résistance de mesure min. (R _M n	uin) 🖸	: 0 (@I _{PN} / ±24V (±5%))		
Not measurable overload	Surcharge non mesurable	A peak (A crête)	:≤20000 (10ms/h)		
Turn ratio (N _P /N _S)	Rapport de transformation $(N_p A)$	Ð	: 1/5000		
Secondary current (I _s) at I_{PN}	Courant secondaire $(I_g) a I_{PN}$ mA		: 400		
Accuracy at I _{PN}	Precision a I _{PN} %		:≤±0.5 (@+25°C)		
Accuracy at I _{PN}	Precision a Im	:≤±1 (-20°C +70°C)			
Offset current (Isa)	Courant résiduel (I ₃₀) mA		:≤±0.25 (@+25°C)		
Linearity	Linearite	96	:≤0.1		
Thermal drift coefficient	Coefficient de dérive thermique	mA/°C	: ≤ 0.01		
Delay time	Temps de retard	μS	:≤1		
di/dt correctly followed	di/dt correctement suivi	A/µs	:≤100		
Bandwidth	Bande passante	kHz	: 0 100 (-1dB)		
No-load consumption current (I_{A0}) (Consumption = $I_{A0} + I_{S}$)	Courant de consommation à vide (Consommation = $I_{A0} + I_S$)	e (I,10) mA	:≤25		
Voltage drop (e)	Tension de déchet (e)	v	:≤1		
Secondary resistance (R _s)	Résistance secondaire (R_{s})	Ω	:≤25 (@+70°C)		
Dieletric strength	Rigidité diélectrique				
Primary / Secondary	Primaire / Secondaire	kVr.m.s. (kV eff.)	: 4 (50Hz, 1min)		
Supply voltage	Tension d'alimentation	V d.c.	: ±15 ±24 (±5%)		
Mass	Masse	Kg	: 1.5		
Operating temperature	Température de service	°C	: -20 +70		
Storage temperature	Température de stockage	°C	: -25 +85		
Temperature of primary conductor in contact with the sensor	Température du conducteur primaire en contact avec le capteur		:≤100		
Particularities	Particularités				

C_ES_7.do



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SCHEMATIC AND LAYOUT FOR VCE MEASUREMENT BOARD





LIST OF MATERIALS FROM PRIMEPACK3 POWER MODULE

Infineon						-	2
Material Conten	t Data Shee	t					
Umbrella Spec	PP3 PrimePACK3	TM .					
Date	2012-09-14			RoHS co	mpllant		YES
Revision	4.0						
Construction element	Material group	Materials	CAS-Nr. If applicable	Average mass [%]*	Sum [%]	Traces	Commenz
chip	inorganic material	silicon	7440-21-3	0,6	0,6		
Base plate and substrate Including metallisation	non noble metal	copper	7440-50-8	50,5	55,2		
	inorganic material	aluminium oxide	1344-28-1	1,6			
	non noble metal	tin	7440-31-5	2,9			
	non noble metal	nickel	7440-02-0			x	
	noble metal	silver	7440-22-4			X	
wire	non noble metal	aluminium	7429-90-5	0,2			
encapsulation	polymers	silicone gel		10,5	10,5		
housing	polymers	Polyamid (PA)		10,5	17,7		classifications: NF F16-101 fine & amola: 12 / F4 CEN/T5 45545: R25: HL3 R24: HL1 R23:-
	inorganic material	antimonypentoxide	1309-64-4	0,7			
	plastics	brominated resin		0,3			
	plastics	chiorinated resin				X	
	inorganic material	silicondioxide / glasfiber		6,2			
lead, finish and plating	non nobie metal	copper	7440-50-8	11,9	16,0		
	terrous metal	steel	11121-90-7	4,1			
	non nobie metal	zinc	7440-66-6			X	
	non nobie metal	nickei	7440-02-0			X	
smd (including thermistors, resistors and shunts)	inorganic material	lead oxide	1317-36-8	0,004	0,004		RoHS compliant
	non noble metal	copper	7440-50-8			X	
	non noble metal	tin	7440-31-5			X	
	noble metal	silver	7440-22-4			X	
deviation	<25%			Sum in total	100.0		

Weight range of product Fluctuation margin

*) related to component weight **) Weight of particular product, see technical product information

portant Remarks:

- This document provides full declaration of all materials present in Infineon products above a threshold of 0,1 % b.w. (1000 ppm).
 Trace concentrations (i.e. < 0,1 % b.w) present in products are marked with an "X" as far as they represent substances-of-concern.
 A list of substances-of-concern can be found at http://www.infineon.com/soc.
 All statements are based on our present knowledge and are subject to change at any time due to technical requirements and development.

<25%

Company	Infineon Technologies
Address	81726 München
Internet	www.infineon.com

SCHEMATIC AND LAYOUT OF CONTROL PCB









