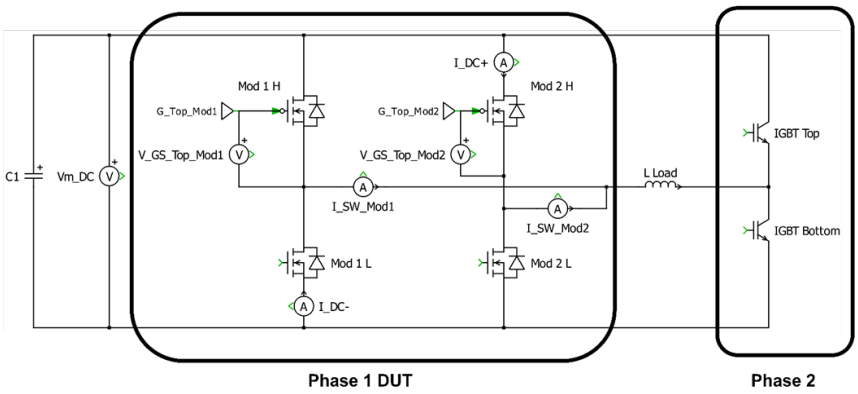
Paralleling of SiC Modules (upto 3) for Mega-Watt application ensuring equal current sharing operation

SiC MOSFET solution for PtX Applications - Industrial Internship at KK Wind Solutions



Project Report - PED3 - 954

Aalborg University, Energy Department
MSc in Power Electronics and Drives 2023-25

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AALBORG UNIVERSITY
STUDENT REPORT

Title:
Paralleling of SiC Modules (upto 3) for Mega-Watt application ensuring equal current sharing operation.

Theme:
SiC MOSFET solution for PtX Applications - Industrial Internship at KK Wind Solutions

Project Period:
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Project Group:
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Participant(s):
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Abstract:

This project focuses on implementing Green Hydrogen technology to reduce fossil fuel dependency. It explores using wide-bandgap (WBG) SiC MOSFETs instead of Si-IGBTs for electrolysers, leveraging their higher power density and switching speeds. The project involves paralleling SiC MOSFET modules and conducting Double Pulse Testing (DPT) on half-bridge configurations to observe current deviations.

The problem is divided into three phases: current ramp-up, current jumps, and freewheeling phases. This project primarily addresses the current ramp-up phase. A FastHenry model simulates the impedance parameters of the switch-node busbar to equalize current sharing among power modules by impedance matching of the conduction paths. Using a new switch-node busbar and load inductor cables, a solution is proposed to ensure current sharing of two modules within tolerance limits during the first pulse.

Further investigations will focus on understanding the turn-on/off characteristics, internal capacitances, and gate driver circuits of the power modules for a potential solution of the other two phases.

Index Terms - "Green Hydrogen, Electrolyzers, Megawatt Power, Wide Band Gap (WBG), SiC MOSFET module, Half-bridge, Double Pulse Testing (DPT), Fast Henry, Power-to-X (PtX)"

Preface

This report has been prepared by PED3-954 as part of the third semester traineeship program of the MSc in Power Electronics and Drives at Aalborg University, in collaboration with KK Wind Solutions. I wish to express profound gratitude to the industrial supervisor, **Bjørn Rannestad** from **KK Wind Solutions**, for his exceptional guidance and support throughout the duration of this project.
I also extend my sincere thanks to our academic supervisor, **Stig Munk-Nielsen** from **Aalborg University**, for his excellent supervision and valuable insights. His expertise and encouragement were instrumental in shaping the direction of this project and ensuring its successful completion.
Additionally, I give my high appreciation to **Anders Eggert Maarbjerg** and **Jakob Iversen Deichgraeber** from **KK Wind Solutions** for their invaluable support during the project progression. Their assistance and collaboration greatly enhanced the quality and outcomes of this research.
The project was undertaken during the fall semester of 2024, spanning from September 2024 to January 2025.

The project investigates the development of an alternative Wide Bandgap (WBG) solution for Power-to-X (PtX) applications by paralleling up to three SiC MOSFET modules. To analyze the power transfer capability exceeding 1 MW, a Double Pulse Testing (DPT) is conducted to observe the switching behavior of Half-bridge modules and to minimize current imbalance within acceptable tolerance limits.

Reading guide

This summary report is separated into chapters which are numbered progressively. These chapters are further separated into sections. The reference method used in this project report is that of the Institute of Electrical and Electronics Engineers (IEEE). Several appendices are attached, including MATLAB scripts, Fast Henry scripts and results. Excel spreadsheet for the testing conducted is attached separately during the project submission.

The following programs have been used during the course of the project:

- Overleaf by WriteLatex Ltd.
- Drawio by JGraph Ltd and draw.io AG
- MATLAB by MathWorks
- Plecs by Plexim GmbH
- LT Spice by Analog Devices
- FastHenry2
- FreeCAD EM Workbench

Aalborg University, January 9, 2025

Shubham

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Nomenclature

Symbol	Explanation	Unit
$V_{GS(th)}$	Threshold Voltage	V
I	Current	A
V	Voltage	V
$R_{DS(on)}$	On-state resistance	Ω
I_{DS} or I_{DN}	Drain-to-source current	A
$C_{DC-link}$	Capacitance of dc-link 2	mF
f_{sw}	Switching Frequency	Hz
L	Inductance	H
V_{GS}	Gate-to-source voltage	V
V_{DS} or V_{DSS}	Drain-to-source voltage	V
$I_{sw-node}$	Switch-node current	A
I_{DRM}	Repetative peak drain current	A
$V_{GS(on)}$	On-state gate voltage	V
$V_{GS(off)}$	Off-state gate voltage	V

Abbreviations

Abbreviation	Explanation
DPT	Double Pulse Test
AC	Alternating Current
DC	Direct Current
PCS	Power Conversion System
FET	Field-effect transistors
IGBT	Insulated-gate bipolar transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PEM	Proton Exchange Membrane
Si	Silicon
SiC	Silicon Carbide
CO2	Carbon Dioxide
WTH	Waste-to-Hydrogen
TES	Total Energy Supply
MSAT	Multi-Step Auto-connected Transformers
WBG	Wide-bandgap
TFC	Total Final Consumption
RE	Renewable Energy
GHG	Green House Gases
MCS	Mega Watt Charging System
IEA	International Energy Agency
IRENA	International Renewable Energy Agency
CCUS	Carbon Capture Utilisation and Storage
WEF	World Economic Forum
AFE	Active Front End
DSO	Digital Signal Oscilloscope
DB	Dead Band
P2X or PtX	Power-to-X
DEA	Danish Energy Agency
kHz	Kilo Hertz
2L-VSC	Two-Level Voltage Source Converter
EV	Electric Vehicle
P2H	Power-to-Hydrogen
CMRR	Common Mode Rejection Ratio
EMI	Electromagnetic Interference
DUT	Device Under Test

Contents

Chapter 1 Introduction

1.1 Motivation

There has been a steady decline of the carbon footprint of Denmark since the 2000's. The country has been one of the early leaders in decarbonisation [1], setting a target for net-zero emissions by 2045 and aiming for 110% emissions reductions by 2050. The country leads in offshore wind, bio-methane and district heating technologies.

The "Energy Statistics 2023" report by the Danish Energy Agency [2] provides a comprehensive overview of Denmark's energy consumption and production for the year. In 2023, Denmark's energy consumption decreased by 2.2%, with significant reductions in coal, natural gas, and oil use, while renewable energy usage increased by 3.0%. Industrial energy use dropped by 4.5%, while household and transport energy consumption rose by 2.0% and 1.6%, respectively.

Renewable energy consumption increased in 2023 as compared to 2022 statistics, also driven by wind, solar energy, biogas, and ambient heat, with renewables making up 82.1% of domestic electricity supply. Despite a decline of over 8% in crude oil and natural gas production, renewable energy production grew by 5.3%, maintaining its majority share.

CO2 emissions from energy consumption fell by 2.1 million tons to 25.8 million tons, continuing a downward trend. The report highlights Denmark's progress in reducing fossil fuel dependence and increasing renewable energy integration, emphasizing the country's commitment to a sustainable energy system and reducing greenhouse gas emissions.

However, the ever-increasing demand for energy to meet final consumption needs still places a significant burden on our dependence on fossil fuels. This dependency on fossil fuels has long posed significant challenges for society, including environmental degradation, economic volatility, and energy security concerns. The combustion of fossil fuels is a major contributor to greenhouse gas emissions, driving climate change and its associated impacts on weather patterns, sea levels, and ecosystems.

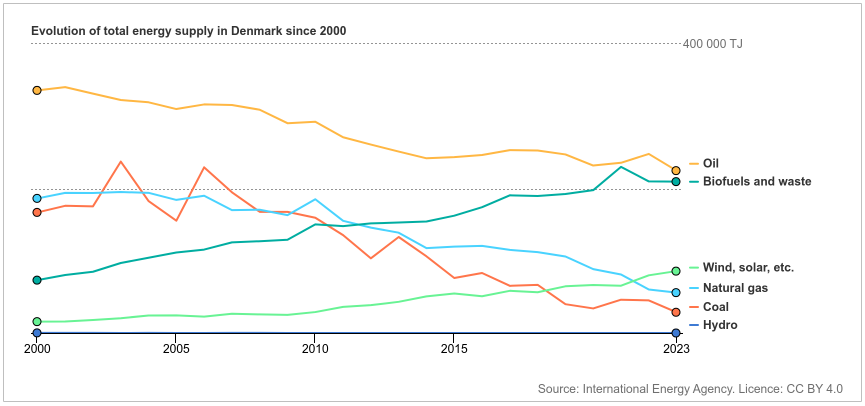
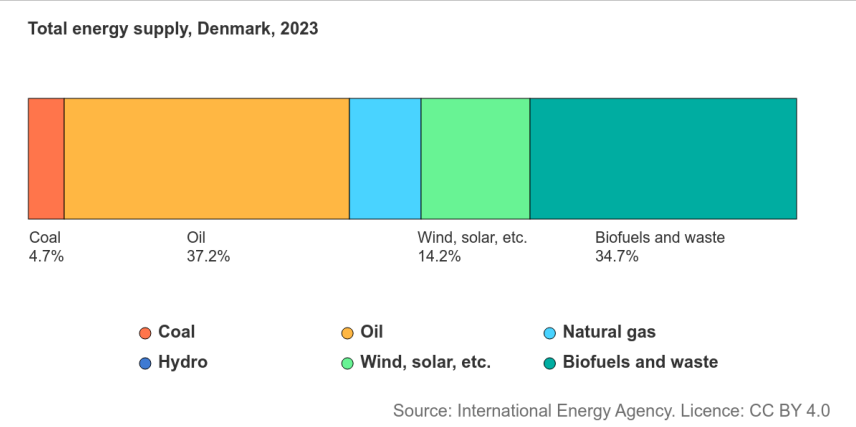


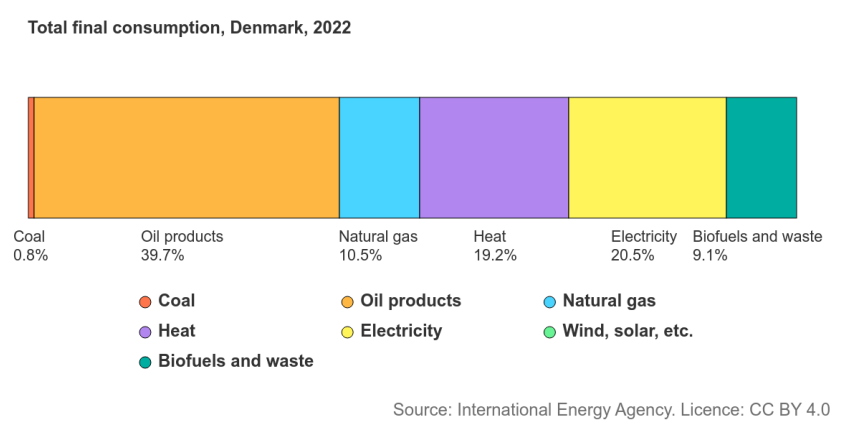
Figure 1.1: Evolution of total energy supply in Denmark
[3]

It can be seen in figure 1.1, within the total energy supply (TES), there has been an

increase in the use of renewable energy resources to meet energy demands. However, a significant portion of 37 % is fulfilled through oil and its products. Refer to figure 1.2a. This percentage is also reflected proportionally in the total final consumption charts as shown in figure 1.2b.



(a) Total Energy Supply - Denmark



(b) Total Final Consumption - Denmark

Figure 1.2: Proportion of Energy Supply and Consumption on renewables and non-renewables [3]

Denmark boasts the highest share of wind electricity among IEA countries, with wind, bio energy, and solar photovoltaic making up over 80% of its electricity mix. Despite impressive advancements in these renewable energy resources, they alone are not yet sufficient to replace conventional energy sources entirely.

The report of the International Energy Agency (IEA) on Denmark's energy mix [1] highlights the country's ambitious goals and achievements in transitioning to renewable energy. Denmark aims for renewables to cover at least half of its total energy consumption by 2030 and to achieve 100% independence from fossil fuels by 2050.

For rapid developments in the decarbonisation segment, the Danish government has begun to tap into the newer fields. Recently, Denmark has expanded its focus to include carbon capture and storage (CCUS) and hydrogen. The Danish Ministry of Climate, Energy and Utilities oversees robust energy and climate governance, ensuring annual policy actions and funding through the Climate Act of 2020.

The report, "Hydrogen needs to replace fossil fuels in industrial applications to meet climate goals" [4], highlights hydrogen's crucial role in replacing natural gas in industries like steel, cement, glass, and chemicals that require high-temperature heat. This transition is vital for decarbonizing these sectors and could create a $1 trillion market. However, 96% of current hydrogen production relies on fossil fuels, necessitating carbon capture and storage (CCUS) to reduce emissions. Producing hydrogen via electrolysis is energy-intensive and requires substantial renewable energy capacity.

The report acknowledges the present cost challenges and poor efficiency of production and emphasizes the need for investment in hydrogen technology and infrastructure, policy support, technological advancements, and increased production capacity. Hydrogen's potential to decarbonize industrial processes makes it essential for achieving net-zero emissions by 2050 and limiting global warming to 2 degrees Celsius. Realizing this potential will require coordinated efforts across technology, policy, and market development.

In summary, while Denmark's renewable energy sources presently are well-developed and play a major role in energy generation, achieving comprehensive decarbonisation requires addressing sectors with high fossil fuel consumption as shown in figure 1.3. Critical attention and innovation are needed in areas such as electricity and heating, transportation (including shipping and aviation and other heavy vehicles). By focusing on these sectors, Denmark can ensure a holistic and sustainable transition to a low-carbon future, aligning all aspects of energy consumption with its ambitious climate goals.

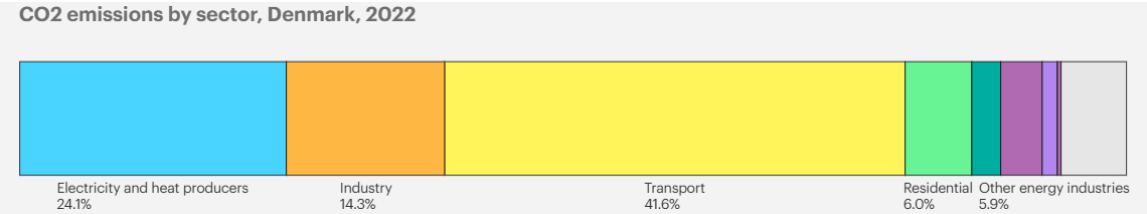


Figure 1.3: CO2 emissions by sector, Denmark, 2022

Battery technology and Hydrogen - Next Step for Energy Goals?

The International Energy Agency (IEA), "Batteries and Hydrogen Technology: Keys for a Clean Energy Future"[5], report underscores the pivotal role of batteries and hydrogen technology in achieving a clean energy future. A diverse portfolio of clean energy technologies is essential to decarbonize all sectors of the economy. Batteries and hydrogen-producing electrolyzers are particularly crucial due to their ability to convert electricity into chemical energy and vice versa.

Lithium-ion batteries have seen significant cost reductions, making them vital for the electrification of transport and the integration of renewable energy sources like wind and solar into the power grid. However, global manufacturing capacity is unevenly distributed, with China leading at approximately 70%, followed by the United States (13%), South Korea (7%), Europe (4%), and Japan (3%). This uneven distribution suggests that

investing further in battery technology in Europe might not be the most strategic move, given the current global landscape.

Green hydrogen, produced through the electrolysis of water using renewable energy sources, is emerging as a key player in the sustainable energy transition. This process emits no CO2, making green hydrogen the most sustainable option compared to grey or blue hydrogen, which are derived from fossil fuels and emit significant carbon dioxide. Green hydrogen's versatility allows it to be used in fuel cells to generate electricity and heat, store renewable energy, and serve as a feedstock for producing chemicals and fuels. It can also help decarbonize hard-to-abate sectors such as shipping, aviation, and heavy industries.

The report highlights the potential for cost reductions in both batteries and hydrogen technologies through mass manufacturing and shared technological advancements. Scaling up electrolyzer production can benefit from the manufacturing experience of batteries, with specialized suppliers like Toray and BASF driving innovation.

Investing in electrolyzer manufacturing presents a significant opportunity for economic growth, creating new demand for clean hydrogen in sectors like transport, iron and steel production, and buildings. Even if new demand does not materialize immediately, electrolyzers can still clean up existing hydrogen supplies in industrial clusters. Policies supporting new hydrogen demand, such as low-carbon fuel standards and purchase subsidies, can further enhance the opportunity for electrolyzers.

For Europe, investing in hydrogen technology could be particularly advantageous. Given the current global distribution of battery manufacturing capacity, Europe might find greater strategic value in focusing on hydrogen. This investment could position it as a leader in green hydrogen production, leveraging its strong renewable energy resources and technological expertise. This focus could also stimulate economic growth, create jobs, and enhance energy security, making hydrogen a key component in Europe's clean energy transition.

The paper "Comparative review of hydrogen and electricity as energy carriers for the energy transition" [6] provides a thorough analysis of the roles of hydrogen and electricity in achieving a sustainable energy future. Hydrogen is highlighted for its high energy density and versatility, making it ideal for long-term storage and heavy-duty transport, despite challenges like high production costs, storage and transportation difficulties, and the need for significant infrastructure investment. Conversely, batteries are praised for their efficiency, established infrastructure, and suitability for direct applications such as residential energy storage and electric vehicles, though they face issues like the intermittency of renewable sources and environmental concerns related to battery disposal. The paper notes that hydrogen shines in applications requiring long-term energy storage and heavy-duty transport, while batteries excel in short-term storage and direct applications. The economic analysis suggests hydrogen's costs are higher, but could decrease with technological advancements and economies of scale. By leveraging the strengths of both, a more resilient and sustainable energy system can be achieved.

This synergy between batteries and hydrogen technologies could accelerate the transition to a sustainable energy system, making them key components in the global effort to meet climate goals.

1.2 Application - Green Hydrogen Production

As inspired from the motivation section, Green hydrogen, represents a transformative solution for our sustainable energy future. According to a report from World Economic Forum (WEF), "Why green hydrogen could play a major role in powering our sustainable future"[7]. As the cleanest form of hydrogen, it emits no carbon dioxide, distinguishing it from grey and blue hydrogen. This innovative energy carrier not only offers a pollution-free alternative but also holds the potential to revolutionize sectors that are difficult to decarbonize, such as heavy industry and long-distance transportation. With the continuous decline in renewable energy costs and advancements in production technologies, green hydrogen is poised to become a cornerstone in the global effort to achieve net-zero emissions and drive the energy transition forward.

Future of green hydrogen

The future of green hydrogen as a key energy source for industrial applications is promising, as highlighted in the paper "Future of Hydrogen as an Alternative Fuel for Next-Generation Industrial Applications; Challenges and Expected Opportunities" [8]. This paper underscores hydrogen's high efficiency, renewability, and zero emissions, making it an excellent alternative to fossil fuels. It discusses advancements in hydrogen technologies across various sectors, including fuel refining, hydrocarbon processing, materials manufacturing, pharmaceuticals, and electronics, while also addressing challenges such as high production costs and the need for significant infrastructure investments. Expected opportunities include the integration of renewable resources and the development of green raw materials, which could drive the widespread adoption of hydrogen in industrial processes.

Similarly, the paper "The Future of Hydrogen: Challenges on Production, Storage, and Applications", [9] provides a comprehensive analysis of hydrogen's potential, discussing various production methods and their environmental impacts. It also highlights significant challenges like high production costs and the need for technological advancements, and examines hydrogen storage methods, evaluating their feasibility, performance, and safety. The paper also compares hydrogen fuel cell vehicle, electric vehicles with battery and gasoline vehicles, and explores applications across sectors such as petroleum refining, chemical production, transportation, and space exploration. It emphasizes the need for continued research, supportive policies, and international collaboration to overcome challenges and fully realize hydrogen's potential as a clean, sustainable energy source. Together, these papers illustrate the critical role green hydrogen could play in the future energy landscape, leveraging its strengths while addressing its challenges through innovation and policy support.

Electrolyzers for Green Hydrogen

Presently, the most common method of producing hydrogen is through electrolysis. Water is broken down into Hydrogen and Oxygen using electricity, and when this electricity is sourced from renewables, the hydrogen produced is termed green hydrogen. They offer a zero-carbon production of hydrogen through its process. The types of electrolyzers used, including alkaline electrolyzers, are the most common and use a liquid alkaline solution, and Proton Exchange Membrane (PEM) electrolyzers, which use a solid polymer electrolyte and are noted for their efficiency and ability to handle variable power inputs from renewable sources.

To support the above argument, The report "CLEAN HYDROGEN PRODUCTION PATHWAYS" can be referred [10] . It provides a thorough examination of various methods for producing clean hydrogen, highlighting their unique benefits, challenges, and readiness levels. The primary techniques discussed include water electrolysis, reforming with carbon capture, methane splitting, biowaste-to-hydrogen, and non-biological waste-to-hydrogen (WTH). Water electrolysis is emphasized for its potential to couple electricity and gas sectors, enhance grid flexibility, and utilize stranded renewable energy. However, it is currently the most expensive pathway, with costs driven by renewable electricity prices and capital expenditures.

In terms of current deployment, water electrolysis is the most common technique, accounting for approximately 50% of the global clean hydrogen production capacity. Reforming with carbon capture follows, representing about 30%, while methane splitting, bio waste-to-hydrogen, and non-biological waste-to-hydrogen collectively make up the remaining 20%.

This distribution reflects the varying stages of technological maturity and economic feasibility of each method, with water electrolysis leading due to its alignment with renewable energy integration despite its higher costs.

The paper "Power Electronics for Green Hydrogen Generation with Focus on Methods, Topologies, and Comparative Analysis" [11] examines power electronic converters essential for optimizing electrolyzer performance in hydrogen production systems. It reviews various electrolyzer types and explores a range of AC-DC and DC-DC converter topologies, including 12-pulse and 20-pulse rectifiers, Multi-Step Auto-connected Transformers (MSAT), and Active Front End (AFE) converters. These innovations aim to reduce harmonic distortions and enhance power quality, addressing challenges inherent in conventional 6-pulse diode bridge rectifiers. The study also investigates DC-DC converters like the Continuous Input Current Non-Isolated Bidirectional Interleaved Buck-Boost Converter and the 3-level buck-boost converter with a coupled inductor. Recent advancements such as the Two-stage ZVT boost converter and multiphase interleaved DC-DC converters are highlighted for their efficiency and reliability.

The article "The Importance of Power Conversion Technologies in the Production of Green Hydrogen" [12], by Infineon highlights the crucial role of power conversion systems (PCS) in green hydrogen production. It emphasizes converting renewable energy inputs into stable electrical outputs for electrolysis. Key AC-DC converter topologies discussed include 12-pulse and 20-pulse rectifiers, Multi-Step Auto-connected Transformers

(MSAT), and Active Front End (AFE) converters, all of which enhance power quality and efficiency.

1.3 Problem Formulation

This section particularly deals with formulating the problem statement. The main advantage of doing that is it clarifies the issue on which the work is implemented, guides the project direction, identifies the stakeholders and beneficiaries, and helps to develop the hypothesis surrounding it [13].

For PtX applications, KK Wind Solutions is developing cutting-edge technology using active switches like IGBTs for both Active Front End converters and DC-DC converters. These components provide better control and efficiency, making them a suitable choice for electrolyzer power supply.

Given the future demand and development of green hydrogen, it is prudent to investigate wide-band gap devices like SiC MOSFETs. This investigation would allow for a suitable comparison on the same topology, highlighting the benefits and challenges of integrating wide-band gap devices. Such a comparative analysis could offer new perspectives and potentially enhance the solutions already developed, paving the way for more efficient green hydrogen production technologies.

For the electrolyzer application, considering their huge power demand, it would require paralleling of these power modules. This poses certain challenges towards current sharing, turn on, turn off mismatch, di/dt, and dv/dt overshoots which would lead to overstressing and lifetime reduction of certain power modules as compared to the others. Therefore, it is necessary to address the problem and investigate a formidable solution for it.

1.3.1 Problem Statement

"Does paralleling of SiC MOSFET power modules (upto 3) for +1 MW electrolyzer application ensure equal current sharing operation?"

1.3.2 Objectives

The objectives of the project are divided into two parts, namely, primary and secondary for the project.

- Primary Objective:

  ◦ Develop a Double Pulse Test (DPT) setup to evaluate the SiC Half-Bridge power modules by assessing each module's switching behavior as well as its dynamic and static characteristics.

  ◦ Introduce a second module to the power stack to investigate current sharing imbalances, and analyze the turn-on and turn-off behaviors of both power modules.

  ◦ Modify the layout of the setup to ensure that the current sharing operation stays within specified tolerance limits.

- **Secondary Objective**:

  ◦ Introduce a third module to the system and ensure the current sharing follows tolerance limits.

  ◦ Investigate more complex behaviors in switching, such as gate driver voltage mismatch, circulating currents, and parasitic impedances in the power stack.

1.3.3 Scope, Constraints, and Assumptions

The project's scope shall be limited to working on a Double Pulse Test (DPT) setup running on power ratings comparable to those of the electrolyzer application. This will enable precise observation of the module's switching behavior under different load conditions.

Based on the results expected from the Double Pulse Testing, there are three major directions to consider in the project. One can look into the setup and layout on the system level which is causing the mismatch in the power power modules, Secondly, it is possible to look into the gate driver and its influence on driving the power modules. And lastly, It might be possible to take a look into the module itself - its layout structure, placement of chips, parasitics impedances of source and gate, coupling effects to get a deeper understanding of the device under test and mitigate the imbalance observed.

Considering this is an industrial project, KK specializes in the converter segment and would have some good insights on the setup modification approach for narrowing down the problem observed. It would be interesting to explore the possibility of focusing on the construction and modification of the DPT setup. Secondly, the power modules and the gate drivers are not its in-house product, and getting detailed information on the structure and design would be difficult and time-consuming as they are proprietary. Also, adhering to the timelines and limited manpower dedicated to the project due to its lower commercial prospect, the pace of decision-making, project planning, and further resource availability are crucial aspects to be taken into consideration.

Given the project's scope, the power modules and gate drivers are treated as ideal components. While their influence on switching behaviors and overall module performance is acknowledged, it is considered negligible for the project's objectives. Nonetheless, their effects are still analyzed within the project's defined parameters.

It is important to note that recommendations for improvements regarding the internal behavior of the module and its gate driver are primarily suggestive for the manufacturer's sake. These pointers should be viewed as indicators for improvement rather than critical issues for this project.

It is assumed that the DC link voltage remains at the same potential for the test duration. The capacitors are assumed to contain the ripple content within grid standards and are not taken into consideration for the project scope. Also, the reactor is considered ideal and its core does not saturate at the operating currents as well as its inductance is assumed to be constant for the test duration.

1.3.4 Limitations

The following limitations are listed below for the scope of the project,

- ***Measurement Limitations***

1. Voltage Measurement with limited bandwidth - The system voltage measurements are done using HVD3206A-6M differential probes from Teledyne LeCroy. These probes offer limited bandwidth upto 120 MHz and any noise observed above this frequency shall be attenuated.
2. For current measurements, Two types of Rogowski probes are used, namely, CWT30R and CWT Ultra Mini (30MHz) from PEM. While the CWT Ultra mini is accurate but is very sensitive to placement and noise in the system. The CWT30R are considered more reliable for measument, however, small fluctuations and noises in the system are attenuated. This might lead to missing skew the results of the waveform analysis. To mitigate the issue both probes are used mounted at different points in the system during measurement for better analysis.

- ***System Limitations***

1. Since, the setup is not grounded at any point, there are chances of measurement errors due to source reference floating on the high side MOSFET.
   Although, the upside is that this avoids the ground loops forming between the baseplate capacitance, cabling parasitic capacitances & other coupling capacitances in the system and the ground.
2. For the alteration of switch node busbar, there are only a few available variants. If the impedance mismatch still persists between the power modules, it has to be mitigated through cable orientation connecting to the reactor unit. Although, it is likely to be resolved, however, due to lack of standard procedure, the results are not repeatable on new setups and might require modifications in the main system.

Chapter 2 State of the Art

2.1 SiC MOSFETs for Power-to-X

Silicon Carbide (SiC) MOSFETs are being explored as an alternative to present state-of-the art Silicon Insulated Gate Bipolar Transistors (Si IGBTs) in Power-to-X (P2X) applications. The papers [14] and [15] discusses the integration of Silicon Carbide (SiC) MOSFET technology in power-to-hydrogen applications offering significant advantages, including a 2-3% efficiency improvement and the ability to operate at switching frequencies in the order of kilo or ten kilo-hertz, compared to 4-5 kHz for traditional Silicon Insulated Gate Bipolar Transistors (Si IGBTs) for MW power transfer. SiC MOSFETs also exhibit better thermal performance, operating at junction temperatures up to 175°C, enhancing system reliability and longevity. These benefits make SiC MOSFETs ideal for compact and efficient AFEs as well as DC-DC converters in hydrogen production. However, their higher initial costs will impede widespread implementation despite their long-term benefits. Additionally, the relative novelty of SiC technology poses challenges related to the availability and maturity of SiC components in the market.

Figure 2.1: SiC MOSFET for Electrolyzer

Why PtX?

As seen from the chapter 1, the move towards production of green hydrogen can be a potentially significant stride towards Denmark's climate goals. The government is investing well in this direction and substantial funds are aided towards development of Electrolyzers.

According to the report from the Danish Energy Agency (DEA),[16] , as a first tender, Denmark has given out six projects for the development of electrolyzers of capacity more than 280 MW with a total budget assigned of 1.25 billion DKK. This is a massive move for achieving the climate neutrality by 2050. The government aims to build 4-6 GW of electrolyzers by 2030, according to a report from offshoreWIND by Adnan Durakovic [17].

The state of green live status is a useful resource, [18] in seeing the on-going developments and potential projects coming up in the PtX segment and the website also shows Denmark's future plans of becoming the world's exporter of PtX products and technologies. [19]

A report from Bio energy International [20], states that the Danish government has secured a significant investment from the Netherlands to advance its Power-to-X (PtX) initiatives. This collaboration involves approximately DKK 1 billion (EUR 134 million) to establish a large-scale PtX plant in Denmark, with a capacity of up to 100 MW. The project aims to produce green hydrogen and other sustainable fuels, supporting Denmark's ambitious climate goals and its strategy to achieve climate neutrality by 2050.

Given the substantial investments, robust government support, and the rapidly expanding market, Power-to-X (PtX) stands out as a strategic and forward-thinking choice for the future. Denmark's commitment to PtX not only aligns with its ambitious climate goals but also positions the country as a global leader in sustainable energy solutions.

Figure 2.2: Hydrogen Power Applications

From a Power Electronics perspective, the market for electrolyzer units presents significant business potential in terms of power supply, conversion, monitoring, and control. With the Danish government's focus on reducing carbon footprints and the rapid advancements in electrolyzer technology, there is a risk that the development of power supply systems and power conversion stages could become bottlenecks for the establishment of these systems.

KK Wind Solutions is addressing this challenge by providing modular power supply systems with integrated solutions, including transformers, rectifiers, cooling, and controls,

offering a comprehensive solution for powering electrolyzer systems. Their systems currently handle up to 6MW of power, scalable to 12MW, and are based on IGBT technology, allowing for the parallel operation of up to four subsystems. KK Wind Solutions has made significant strides in the development of Power-to-X (PtX) solutions. For more detailed information on their scope of work, provided solutions, and market standing, one can visit their PtX webpage [21] . The figure 2.3 shows a block diagram indicating the target area of KK Wind Solutions in the electrolyzer power supply.

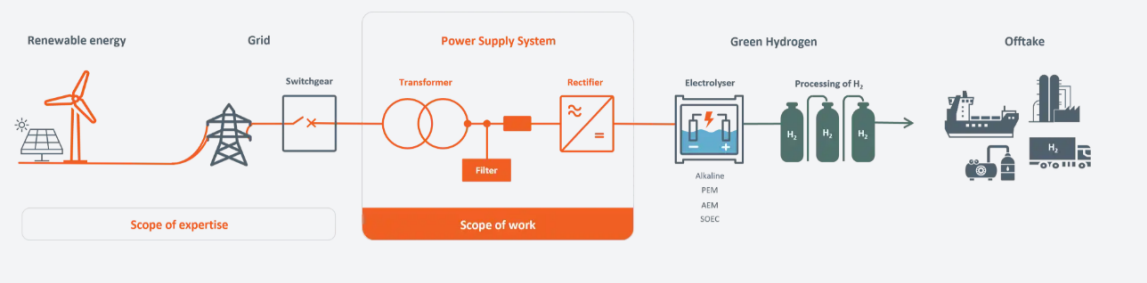


Figure 2.3: Scope of Work [21]

The paper “Overview of Power Electronic Converter Topologies Enabling Large-Scale Hydrogen Production via Water Electrolysis” [14] provides an in-depth analysis of various power electronic converter topologies crucial for large-scale hydrogen production through water electrolysis. It highlights the importance of high-power, high-current AC/DC converters in transforming medium-voltage AC power to a large DC current necessary for hydrogen electrolyzers. The study evaluates different converter topologies, focusing on their performance, efficiency, and cost-effectiveness.

Working with SiC MOSFET technology as part of an alternative for the IGBT solution is the prime focus of this trainee-ship. There are certain merits as well as challenges to the integration of newer technology to the application.

The paper, "SiC-MOSFET or Si-IGBT: Comparison of Design and Key Characteristics of a 690 V Grid-Tied Industrial Two-Level Voltage Source Converter" [22] presents a detailed comparison between Silicon Carbide (SiC) MOSFETs and Silicon (Si) Insulated Gate Bipolar Transistors (IGBTs) in the context of a 190 kVA industrial three-phase two-level voltage source converter (2L-VSC) for 690 V grids. The study evaluates both designs under identical conditions, with switching performed using both IGBTs and SiC MOSFETs, to highlight potential gains and limitations in terms of cost, efficiency, size, and weight. The results indicate that the SiC-based design offers substantial benefits, including an approximately 40% reduction in weight, an 11% reduction in system cost, and improved overall efficiency compared to the Si-based design. This makes SiC MOSFETs a compelling choice for applications requiring high efficiency and power density.

The paper,"Performance Evaluation of High-Power SiC MOSFET Modules in Comparison to Si IGBT Modules" [23], discusses the possibility of replacing the Si-IGBTs in high power applications. A 1700V/325A MOSFET is taken as a reference for analysis for a 100kW application. Although, it is not quite up to speed with the power handling capability required for the electrolyzer application. This paper provides useful insights

looking at the transient behaviour of the devices at high power applications. The device overshoot with current increase, its efficiency, switching behaviour, thermal management and power density have been discussed with results in favour of SiC MOSFETs. This however, is not enough for a significant shift for the Si-IGBT technology. There are many ongoing researches on the SiC technology however, they still are manufactured at a lot higher cost and their long term reliability needs further investigation.

The paper titled "Comparative Assessment of 3.3 kV/400A SiC MOSFET and Si IGBT Power Modules" [24] presents a thorough evaluation of a commercial 3.3 kV/400 A SiC MOSFET power module against a Si IGBT power module in a half-bridge configuration. The study highlights that SiC MOSFETs exhibit a lower forward voltage drop of 1.6 V at 250 A and 1.3 V at 400 A at 300 K, and significantly lower switching losses—7.5 times lower than Si IGBTs at a supply voltage of 2000 V and 300 K. Additionally, SiC MOSFETs maintain consistent switching losses across varying temperatures, unlike Si IGBTs. The paper also explores the short-circuit capabilities of SiC MOSFETs, noting their ability to withstand short-circuit events up to a certain duration before thermal runaway occurs. Despite these advantages, challenges such as higher costs and the need for optimized gate drive circuits remain. Overall, the study concludes towards SiC MOSFETs as a promising alternative for high-power applications.

Power Modules for Electrolyzers

When considering SiC MOSFET power modules for electrolyzer applications, several key factors need to be evaluated: Power levels, voltage and current handling capability etc. These must be carefully assessed to match the specific needs of the electrolyzer system, ensuring compatibility and optimal performance. Aspects like thermal management to ensure better reliability and longevity, overall system efficiency to maximize energy savings, and cost justification are always a good way for selection of power solutions. By carefully examining these aspects, one can leverage the advantages of SiC MOSFET power modules to optimize electrolyzer performance, contributing to more efficient and sustainable hydrogen production.

In accordance with the Power-to-X application targeting the electrolyzer segment. It is important to know the application demands medium-to-high power handling capabilities. Providing a power electronics solution includes a rectifier, for supplying appropriate voltage levels an AC grid input is necessary. A typical example of a medium power electrolyzer with 3MW of power requirement can be taken as a reference moving forward. For such a system a DC link voltage of approximately 1350V with a current demand of more than 2500A. It is crucial to select a device which is capable of handling such power levels. Industrial accepted 3.3 kV modules for traction applications and now newly appointed 2.3 kV modules specifically targeting the PtX and Wind Energy sector are very effective choices for fulfiling the power demands.

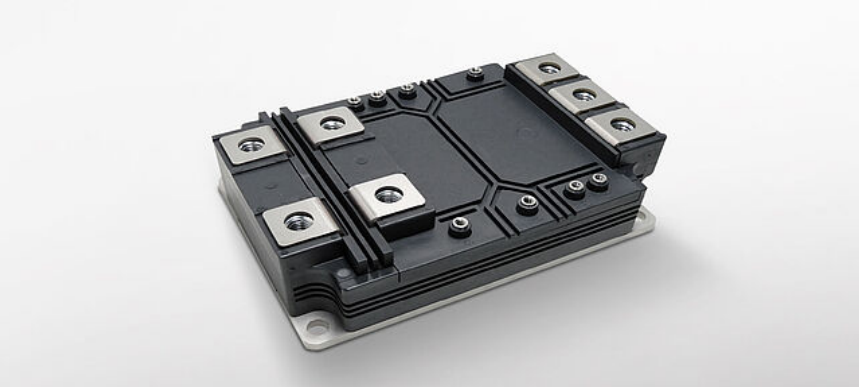


Figure 2.4: Typical SiC Module for Electrolysers

As part of the previous semester project on Mega Watt Charging Systems (MCS), a full bridge inverter power module from Wolfspeed was used. The project was targeted at understanding a Single Active Bridge using a laboratory version for a 10kW application and how the learnings propagated for Megawatt applications for EV charging. Although, the topology as in whole is not adopted in this project, the learnings from power module selection can be used in this project. The voltage overshoots at each turn off instance due to di/dt from the parasitic inductances, the inrush current due to turn on of switches impact greatly on the selection of the modules power levels. This section discusses about the key variables and required margins for selection of a semi-conductor device for our application.

The paper "High-Power Electronic Applications Enabled by Medium Voltage Silicon-Carbide Technology: An Overview" [25] highlights the crucial role of medium voltage silicon-carbide (SiC) semiconductor devices in advancing high-power electronic applications. SiC devices, are preferred over traditional silicon (Si) counterparts due to their enhanced static and dynamic performance characteristics. These include higher switching frequencies in order of tens of kilo hertz, reduced conduction losses, and improved thermal management capabilities. Such attributes make SiC semiconductors particularly suitable for applications demanding high efficiency and reliability, such as renewable energy systems and electric vehicles. The paper notes that SiC MOSFETs, capable of handling voltages up to 1200 V and currents up to 600 A, are especially appropriate for power-to-hydrogen systems, where high power density and efficient energy conversion are essential. This technological advancement facilitates the integration of renewable energy sources with hydrogen production systems, thereby supporting the transition to sustainable energy solutions.

The paper "Application of a Multiphase Interleaved DC-DC Converter for Power-to-Hydrogen Systems" by Pellitteri et al. (2023) [15],explores various topologies and power levels to optimize electrolyzer performance in Power-to-Hydrogen (P2H) systems. The study highlights the use of a multiphase interleaved DC-DC converter, which significantly reduces current ripple and enhances efficiency. This topology is particularly effective for high-current applications, handling up to 1000 A with minimal ripple. Additionally, the paper discusses the full-bridge step-down isolated DC-DC converter, which provides efficient voltage regulation and isolation, crucial for safety and performance. The choice of semiconductors is critical, with Insulated Gate Bipolar Transistors (IGBTs)

preferred for their ability to handle high power levels, typically up to 1200 V and 600 A, and Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) used for their fast switching capabilities and efficiency at lower power levels, often around 600 V and 300 A. These configurations ensure high power density and efficiency, making them ideal for integrating renewable energy sources with hydrogen production systems.

2.2 Paralleling of SiC MOSFETs - Motivation, Benefits, and Challenges

For the electrolyzer application, a single MOSFET module is not completely sufficient enough to provide the necessary power required. However, as stated above, the SiC modules are capable of handling several kilo amps of current, still for megawatt applications, power modules are required to be paralleled for going further up in the current handling capabilities. From the above subsection, "Power Modules for Electrolyzers", an indicative power level can be taken as a base for further investigation. Also, even though, in some cases, it might seem quite possible to extract the amount of power necessary from one module, therefore, the requirement of additional gate drivers, power board integration, additional costs and additional parasitics can be avoided upto a certain power level, it is not recommended considering the efficiency of the power converter, the reliability of the converter for long term use, thermal handling and thermal runaway and redundancy of power devices for long term sustainability of the power converter solution for the electrolyzer application.

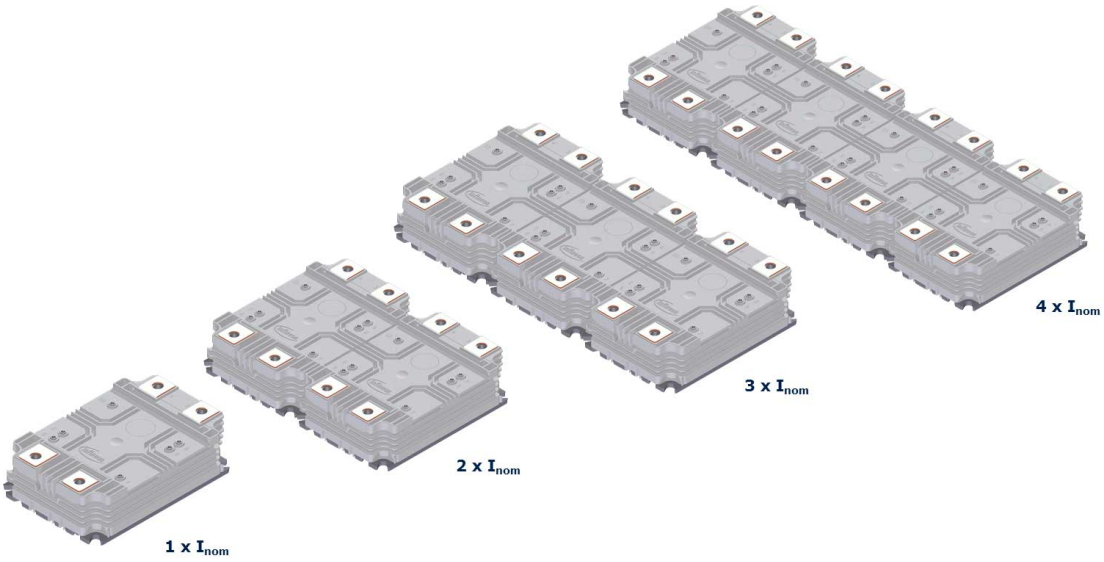


Figure 2.5: Paralleled Power Modules for high current

The paper “Parallel Operation of SiC MOSFETs” [26] by Yuequan Hu and Jianwen Shao provides an in-depth analysis of the challenges and solutions associated with operating Silicon Carbide (SiC) MOSFETs in parallel configurations. SiC MOSFETs are favored for their high efficiency, fast switching speeds, and ability to handle high power densities, making them ideal for applications such as electric vehicle (EV) chargers, server power supplies, and renewable energy systems. However, the parallel operation of these devices

introduces complexities, particularly in ensuring uniform current sharing. The authors identify several critical factors that influence current sharing, including variations in the turn-on threshold voltage, internal gate resistance, and the parasitic inductances inherent in the PCB layout. These factors can lead to imbalanced current distribution, which may affect the overall performance and reliability of the power electronic system.

To address these challenges, the paper presents both experimental results and simulation data to illustrate the effectiveness of various strategies for achieving balanced current sharing. The authors explore techniques such as optimizing the gate drive circuitry, adjusting the layout to minimize parasitic inductances, and selecting MOSFETs with closely matched electrical characteristics. They also discuss the importance of thermal management in maintaining consistent performance across all devices. By implementing these strategies, the paper demonstrates that it is possible to enhance the reliability and efficiency of systems utilizing parallel SiC MOSFETs, thereby unlocking their full potential in high-power applications. This comprehensive study provides valuable insights for engineers and researchers working to optimize the performance of SiC-based power electronics.

The paper titled "Parallel Connection of Silicon Carbide MOSFETs—Challenges, Mechanism, and Solutions" by Helong Li delves into the complexities and solutions associated with the parallel connection of Silicon Carbide (SiC) MOSFETs. One of the primary challenges identified is the issue of current imbalance, which arises due to variations in device characteristics and circuit parameters. This imbalance can lead to some MOSFETs carrying more current than others, resulting in overheating and potential device failure. The high switching speeds of SiC MOSFETs further exacerbate this problem by making the devices more sensitive to parasitic inductances and capacitances in the circuit. Effective thermal management is another critical challenge, as SiC devices operate at higher power densities, necessitating efficient heat dissipation to prevent localized hotspots and ensure device reliability.

To mitigate these challenges, the paper discusses both passive and active strategies. Passive methods include optimizing the PCB layout to minimize parasitic inductance and ensure symmetrical current paths, as well as using closely matched MOSFETs to reduce the likelihood of current imbalance. Active methods involve implementing feedback control systems that dynamically adjust gate drive signals to balance the current distribution among the parallel devices. Additionally, designing gate drive circuits that can compensate for differences in device characteristics and parasitic elements is highlighted as an effective active strategy.

The benefits of successfully addressing these challenges are significant. By achieving balanced current distribution and effective thermal management, the reliability and performance of SiC MOSFETs in high-power applications can be greatly enhanced. This enables the full potential of SiC technology to be realized, offering higher efficiency, faster switching speeds, and better thermal management compared to traditional silicon-based devices. The paper also points to future directions, such as advancements in high-power multi chip SiC module packaging and innovative gate driving techniques, which will further improve the performance and reliability of parallel SiC MOSFET configurations.

These developments are crucial for the continued advancement of power electronics and the broader adoption of SiC technology in various high-power applications.

The document "AN_2009_PL18_2010_105641" by Infineon, titled "Paralleling Power MOSFETs in High Current Applications: Effect of MOSFET Parameter Mismatch on Current and Power Dissipation Imbalance," provides an in-depth analysis of the challenges and solutions associated with paralleling MOSFETs in high current, low voltage applications. It underscores the importance of minimizing conduction resistance R_{DSon} to boost efficiency and lower operating temperatures. The paper identifies critical parameters, such as threshold voltage $V_{GS(th)}$, that significantly influence current sharing among paralleled MOSFETs. Discrepancies in these parameters can lead to uneven current distribution, causing some MOSFETs to dissipate more power and operate at higher temperatures, potentially degrading overall system performance. The document provides a thorough analysis of these imbalances, offering design engineers valuable insights into optimizing power converter designs by considering realistic conditions and parameter variations. It emphasizes the importance of selecting MOSFETs with closely matched parameters, effective thermal management, and implementing circuit design techniques to mitigate the effects of parameter mismatches, ensuring reliable and efficient operation in high current applications.

In summary, the effective paralleling of power MOSFETs is crucial for high current applications, such as electrolyzers and renewable energy systems. Addressing challenges like current imbalance, thermal management, and parameter mismatches through optimized design and careful component selection can significantly enhance the reliability, efficiency, and performance of power electronic systems. These advancements are essential for leveraging the full potential of SiC technology and ensuring long-term sustainability in high-power applications.

2.3 Double Pulse Test Setup

Double Pulse Test is an industry accepted standard for carrying out measurements of switching parameters and evaluating the dynamic behavior of switching modules like MOSFETs and IGBTs. This can be further used to evaluate the energy losses during turn on and turn off intervals as well as the reverse recovery parameters.

For this project, we will also conduct Double Pulse Testing (DPT) on the selected MOSFET modules to observe relevant parameters like current sharing, dynamic and static parameters of the modules and follow appropriate procedures to mitigate the problems seen in the testing. The following section explains the fundamentals of a basic DPT setup and highlights potential pitfalls that could result in inaccurate evaluations of the modules. Our goal is to ensure the setup is uniform and symmetric for all modules, eliminating any imbalances caused by the layout.

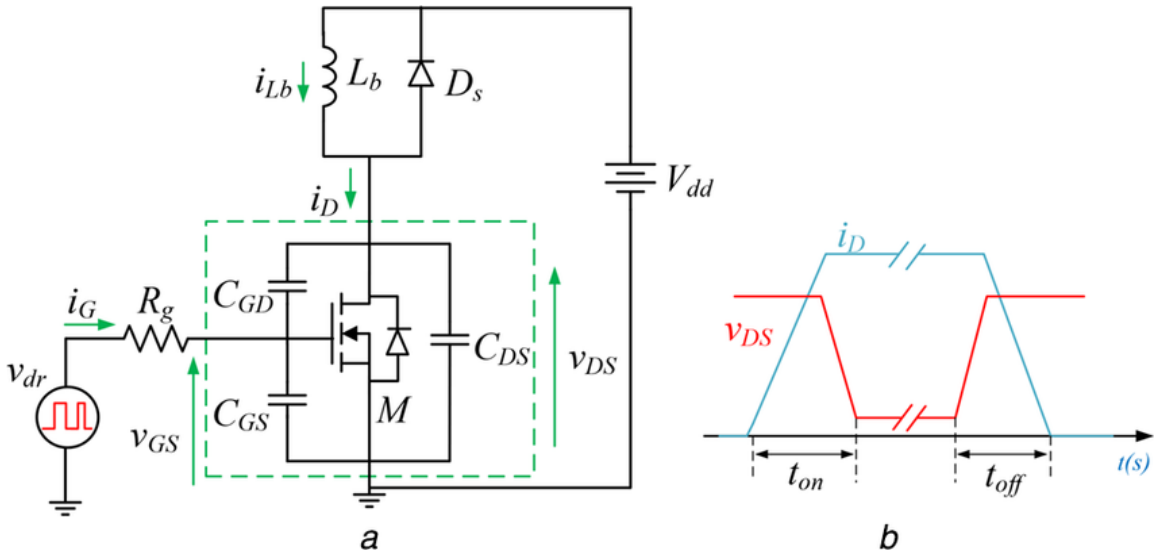


Figure 2.6: Typical DPT Setup for MOSFET evaluation

The paper “Double Pulse Testing: The How, What and Why” by Infineon Technologies [27] provides a comprehensive overview of the double pulse test (DPT) methodology, emphasizing its critical role in evaluating the switching performance of power semiconductors like MOSFETs. It explains that DPT is essential for identifying potential issues early in the design cycle by accurately measuring switching times and waveforms under controlled conditions. The paper details the typical DPT setup, including the use of an H-bridge configuration, and underscores the importance of safety due to the high voltages involved. By following the guidelines provided, engineers can optimize device performance, enhance reliability, and reduce time to market, ultimately improving the robustness of power semiconductor designs.

The paper, "Double pulse test based switching characterization of SiC MOSFET", also shows how DPT is essential for characterizing the switching performance of silicon carbide (SiC) MOSFETs, providing insights into their dynamic behavior under various operating conditions. Accurate voltage probing during DPT is challenging due to the high-speed switching of SiC MOSFETs, which introduces significant electromagnetic interference (EMI) and noise.

To address these challenges, differential voltage probes are commonly used to mitigate common-mode noise and ensure precise measurements. Proper shielding and grounding techniques are also critical to reduce EMI and enhance measurement quality. When selecting voltage probes for DPT, key specifications include high bandwidth (typically in the range of hundreds of MHz) to capture fast switching transients, a high common-mode rejection ratio (CMRR) to minimize noise, and appropriate voltage ratings for both differential and common-mode voltages. High input impedance is also necessary to prevent the probe from loading the circuit under test.

Examples of suitable probes include the Tektronix TDP3500, with a bandwidth of 3.5 GHz and a differential voltage range of ±42 V, and the Keysight N2790A, which offers a bandwidth of 100 MHz and a differential voltage range of ±1.4 kV. These advanced probing techniques and carefully selected probes enable accurate and reliable measure-

ments of SiC MOSFET switching characteristics, crucial for optimizing their performance in power electronics applications.

The paper "Pitfalls and their avoidability in the Double-Pulse Test" by Infineon Technologies [28] provides a detailed analysis of common issues in double-pulse testing and offers strategies to mitigate them. It identifies key pitfalls such as inaccurate measurements due to improper setup, with recommendations to use inductors that do not saturate at peak currents and to maintain di/dt limits between 10 µs and 200 µs to ensure accurate switching times. The paper details the use of an H-bridge configuration for more accurate simulation of real-world conditions and highlights the necessity of using a programmable pulse generator to control switching times precisely. Safety is paramount, with recommendations to enclose high voltage components in protective covers and use warning lights and interlocks to prevent accidents. By following these guidelines, engineers can achieve more reliable and accurate measurements, enhancing the performance and reliability of power semiconductor devices.

Although, there are some approaches which are better suited for wide band gap modules measurement at medium to high voltage ranges, for instance, The paper “Improved Double Pulse Test for Accurate Dynamic Characterization of Medium Voltage SiC Devices” by Infineon Technologies details several key improvements in the design of the double pulse test (DPT) setup to enhance the accuracy of dynamic characterization for medium voltage Silicon Carbide (SiC) devices. One significant improvement is the optimization of the gate drive circuit, which includes precise control of gate resistance to minimize switching losses and improve the fidelity of the switching waveforms. The paper also highlights the use of advanced measurement techniques to reduce electromagnetic interference (EMI), such as shielding and proper grounding of the test setup. Approaches to minimize the impact of parasitic capacitances are also presented in the paper. Additionally, the test circuit design has been refined to ensure consistent thermal conditions, which is crucial for obtaining reliable data on the thermal performance of SiC devices. These enhancements collectively enable more accurate measurement of switching characteristics, such as turn-on and turn-off times, and help in better understanding the behavior of SiC MOSFETs under real-world operating conditions.
While this approach offers significant benefits, it may extend the project timeline and is better suited for future investigations. For the scope of this semester, we will utilize a basic double pulse setup with feasible modifications to support our measurement results.

Chapter 3 System Overview

This chapter deals with the overview of a Power supply solution, its components, and Double Pulse Test setup for the switching modules.

3.1 Power Converter System

The power converter system is used to convert the input voltage of 690 V AC to 1350V DC for making it suitable for Electrolyser operation. For power handling Si-IGBTs are used in parallel operation alongwith reactor and filter capacitors.

Block diagram of the Power Solution

As shown in figure 2.3, the scope of work is defined for the electrolyzer solution provided by KK Wind Solutions. There are several different solutions offered by the company, the block diagram for one of the comprehensive solution is presented below:

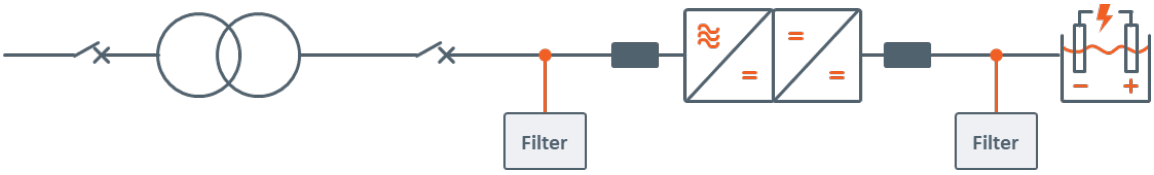


Figure 3.1: Block Diagram - IGBT AFE with DC/DC Converter

Figure 3.1, shows certain circuit breakers before and after the transformer unit to isolate the power converter unit from the grid. The transformer provides the desired voltage level of 690 V feed to the AC-DC converter unit. A second order filter is placed on all the three phases before and after the AC-DC converter unit to inject a cleaner waveform with noise within the approved specifications.

The AC-DC converter stage is also a 3-phase converter with boost capability to produce a DC signal of 1350V. Using the DC-DC buck converter stage the voltage is brought down to be suitable for the electrolyzer unit. Further in the system, a second order filter is setup to reduce the ripple content making it suitable for the electrolyzer unit. An inductive filter is dedicated for each leg of the power stack and certain number of capacitors are charged using each leg of the DC output. A bleeder resistor is added in parallel to the DC capacitors.

Currently, there are four Si-IGBT modules connected in parallel at each stage of power conversion, including the AFE and DC-DC power conversion stages. To incorporate the SiC MOSFET as an alternative solution, the same amount of current or higher shall be handled by the units with current sharing within tolerance limits.

3.2 Double Pulse Test Setup

This section introduces a Double Pulse Test (DPT) Setup prepared in lab for testing the SiC modules.

To emulate a similar setup as shown in section 3.1, and for understanding of the system performance, the DPT setup is made using the same stack arrangement. Here, Phase 1 is kept as a device under test (DUT) with the SiC MOSFET modules while Phase 2 is used

for system testing using IGBT modules (same as the modules in the system) as shown in figure 3.2.

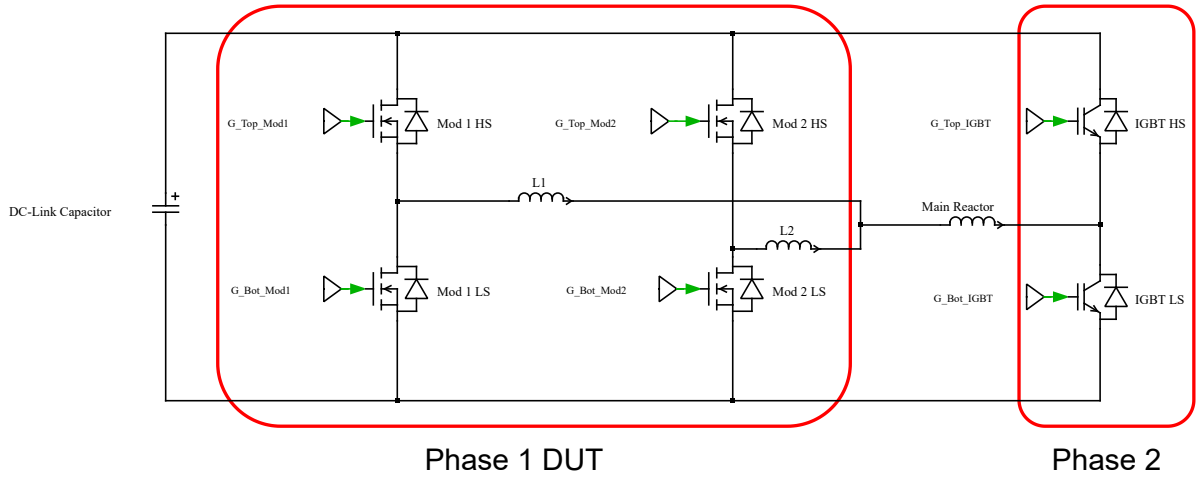


Figure 3.2: Double Pulse Test Setup in Lab

As per the conventional test setup 2.6, there are some modifications done to the setup to carry out testing of both the High-Side MOSFET as well as the Low-Side MOSFET modules. Figure 3.2 provides a single line diagram of the lab setup.

The DC link capacitor kept along-with a bidirectional power supply to carry out dynamic power transfer and to ensure voltage is stable during the testing.

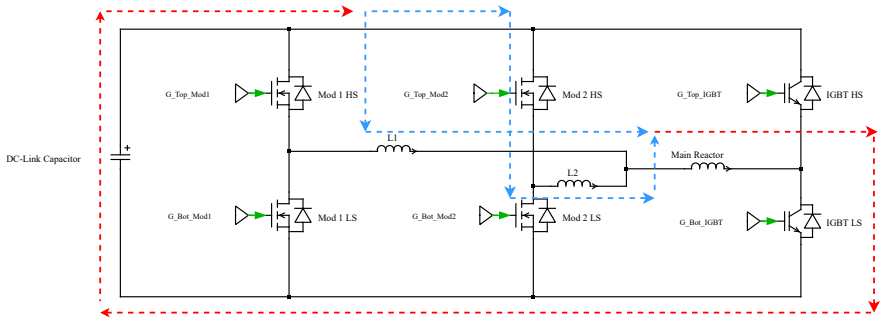
The SiC power modules are tested using this DPT setup. Each SiC power module consists of a half-bridge and are connected in parallel to understand the current sharing among these power modules. Gate-Source voltages, Drain-Source voltages, high side current, low side current and switch node currents are monitored during the testing for both modules. This gives an understanding on the system behavior.

3.2.1 Test Setup Operation

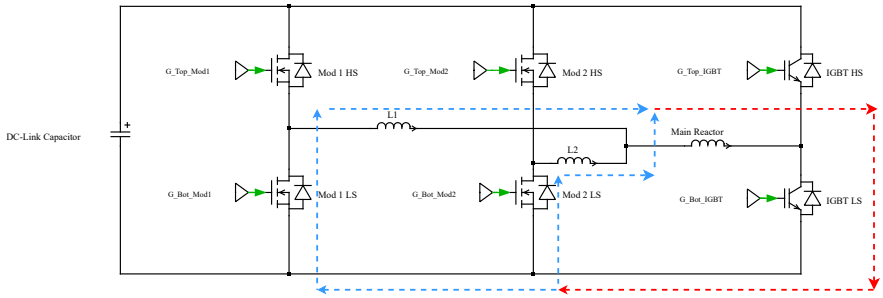
The test setup is developed in such a way that it is sufficient to test both the high side and low side modules. Two half-bridge modules are connected in parallel to observe the dynamic characteristics of each module, current imbalance at different current levels and understand the underlying causes. Following figures 3.3 and 3.4 describes the operation of the setup.

For High Side MOSFET

The figures 3.3a and 3.3b defines the DPT operation carries out for the high side MOSFET testing. The red lines shows the complete current while the blue lines shows the shared current paths respectively.



(a) High Side MOSFET Testing - Active State

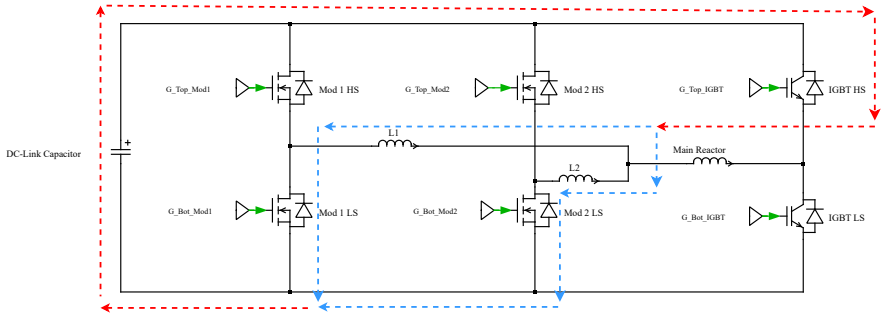


(b) High Side MOSFET Testing - Freewheeling State

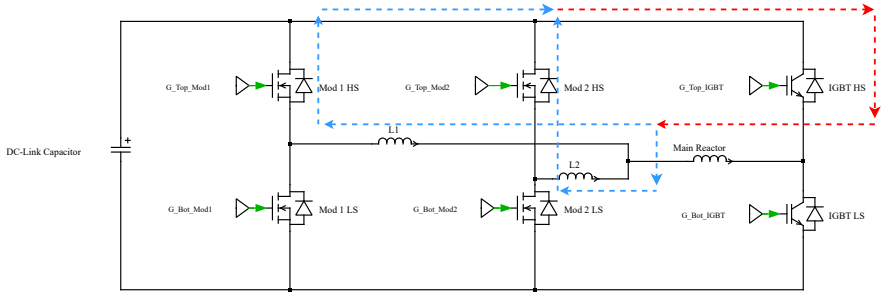
Figure 3.3: High-Side Module Testing using Double Pulse Setup

For Low Side MOSFET

Similarly, the figures 3.4a and 3.4b defines the DPT operation carries out for the low side MOSFET testing. The red lines shows the complete current while the blue lines shows the shared current paths respectively.



(a) Low Side MOSFET Testing - Active State



(b) Low Side MOSFET Testing - Freewheeling State

Figure 3.4: Module Testing using Double Pulse Setup

There are three important times, namely, T1 - First Pulse duration, T2 - Free-wheeling Pulse duration and T3 - Second Pulse duration which controls the MOSFET operation at different current levels and help to test the modules for different power handling capabilities.

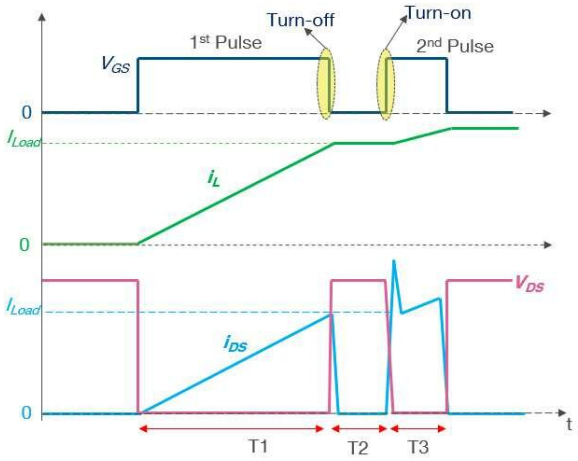


Figure 3.5: Typical behavior of current during double pulse testing

In figure 3.5, the timings T1, T2 and T3 are shown with V_{GS} of the MOSFET under test. During the freewheeling part (T2), the load current through the main inductor is stable and the peak on the i_{DS} at the second pulse (T3) is due to reverse recovery current from diode.

Chapter 4 Modelling

In this chapter, the modeling of the Double Pulse Test (DPT) system components and necessary calculations are done to compute the expected results before going into the system testing.

4.1 Busbar Modelling

To minimize the impact of parasitic impedances in the current imbalance, a new busbar is developed for the switch-node referring to section 7.2. The presently used busbar provides an unbalanced path for the current propagation and the arrangement of the inductor cable also embarks significant impact on the switching behavior of the system due to its mutual inductance effects.

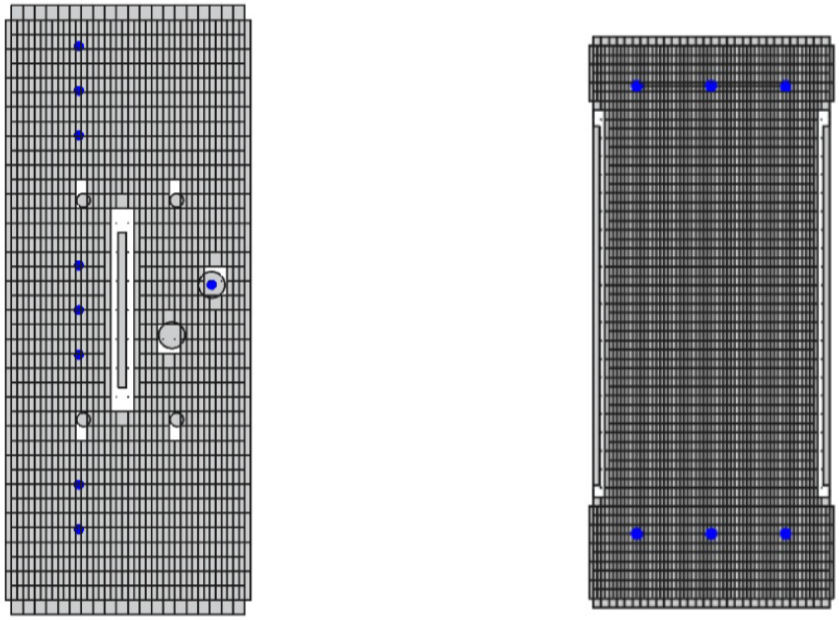
Taking these issues into consideration, a new busbar is modeled to offer equal impedance matching at the switch node, ensuring a more synchronized ramp up phase due to equalized inductances to meet the tolerance requirements as well as the freewheeling phase where the major dependence is on the resistance of the layout.

At the industrial internship, a busbar already designed for a similar IGBT application is available and it gives a good starting point for the modeling and further testing of the system. The image of the busbar can be referred to in figure 7.6. This busbar is sufficient to cater three SiC 100mm MOSFET modules and could be directly connected to the switching node of the modules using flexible busbars.

As shown in figure 4.1a, a rectangular cut is present in the middle of the busbar to equalize the impedance of the shortest path with the other two points of contact. However, initial tests conducted on the busbar using three modules in parallel. However, figure 7.7 shows that the modules are still not sharing equal currents with the middle module (module 2) having the highest di/dt. Therefore, these cutouts in the busbar may not be effective in achieving their intended purpose, as they have not been fully analyzed for direct deployment in the system.

4.1.1 Fast Henry Modeling

To make use of this busbar and see if it can support the function for two atleast two modules with slight modifications, a Fast Henry Model is developed in association with FreeCad tool.
Figure 4.1 below shows the modeled busbars in FreeCad tool,



(a) Switch-Node Busbar **(b)** Braided Busbar

Figure 4.1: Modeled Busbars

For the Switch-Node Busbar shown in figure 4.1a, the blue points are the nodes which are the points of contact with the braided busbar on one end and inductor cable on the other end. The rectangular cutout is provide to equalise the impedances of the middle module with the other two modules on the extreme ends. The smaller holes x4 with diameter 7 mm are for busbar mounting and the larger holes x2 with diameter 13.5mm is for mounting the cable or busbar further to connect to the main inductor.

The Braided Busbar shown in figure 4.1b is connected to the switching node of the SiC MOSFET power module. Since this module offers three points of contact, the busbar nodes are taken as equipotential on the end where the module is connected. The other end nodes represents the connection points of the braided busbar with the switch-node busbar.

From the FASTHENRY analysis, a 3x3 Z-matrix is obtained at different frequency intervals one decade apart. It is possible to make more frequency points but since the impedance values are consistent from 1kHz and up with low variations, it is decided to take 10 kHz frequency as a reference for the matrix values. The Z-matrix consists of self-impedances, meaning from the braided busbar start node to the end of the node port and the mutual impedances originating from the braided busbar themselves and also switch-node busbars.

4.1.2 MATLAB Modeling

The obtained Z-Matrix includes the self and mutual impedances from node port initialization to node port termination. The physical representation of the obtained matrix can be seen in figure 4.2 below:

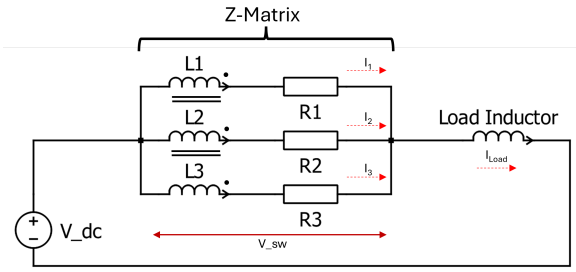


Figure 4.2: MATLAB Model

Since,

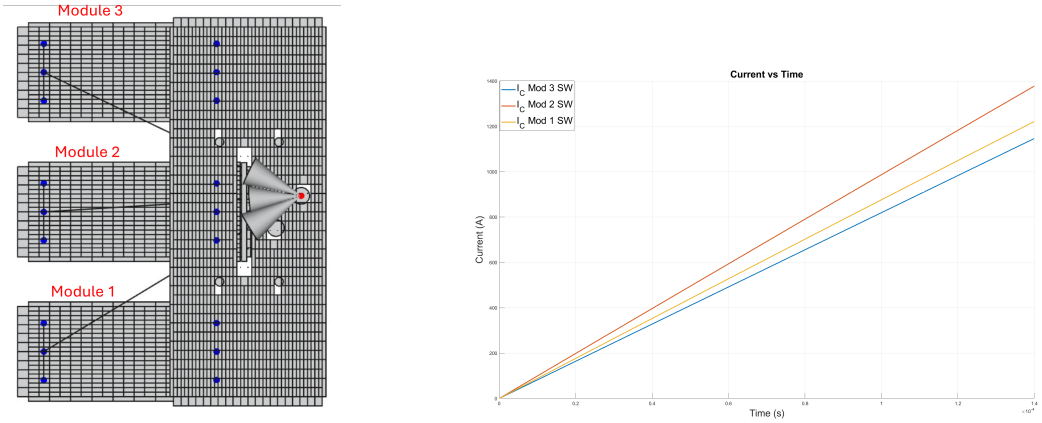
$$I_1 + I_2 + I_3 = I_{\text{Load}} \tag{4.1}$$

and

The voltage, V_{sw}, is consistent across all three nodes connected in parallel. The concept involves injecting V_{sw} into each parallel segment and determining the various current values corresponding to the different impedances of each segment. The simulation emulates the ramp-up phase ensuring that the load current aligns with the measured values. Variations in current values at each time point illustrate differences in slopes, which arise from the diverse impedance values in each segment.

Modeling is done in the following manner,

1. **Braided busbar to Switch-node busbar** - For catering three modules from the braided busbar to the point of cable connection of the switch-node busbar.



(a) Fast Henry Model with three modules

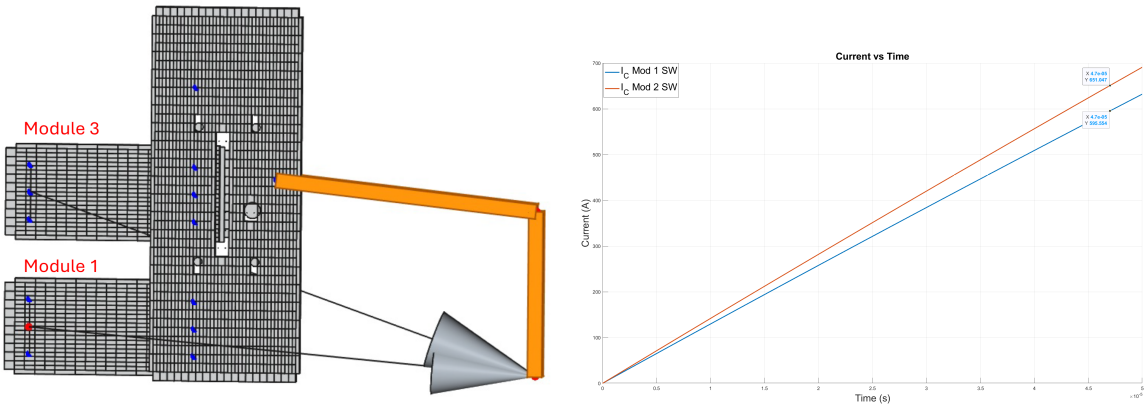
(b) Current Sharing for three modules

Figure 4.3: Modeling of switch-node busbars

The results follow a similar trajectory as the measured values shown in figure 7.7. Seeking the complexity of measurement results, it was decided to first of all move to two modules instead of three to match the ramp up timings. Additionally, the role of inductor cable has to be taken into consideration for better matching the model with the measurement results.

This model with two busbars incorporates the inductor connection cable, connected at specific angle, for matching the impedances better.

2. **Braided busbar to cable end** - For catering two modules from the braided busbar to the point of cable connection of the switch-node busbar.



(a) Fast Henry Model with two modules **(b)** Current Sharing for two modules

Figure 4.4: Modeling of switch-node busbar with cable

The cable connection to the load inductor is taken into consideration while evaluation of the two modules. Skin depth is taken as $4.67e-01\ mm$ considering the frequency of 20 kHz for the 50 μsec ramp up operation.

Comparing the testing results from section 7.3, can be seen in the table below:

Note: The module naming convention is internal for identification. To match the same naming convention, the model is also given the same name for the power module.

Table 4.1: Comparison: Model vs Measurement

Parameter	**Fast Henry Model**	**Measurement Results**	**Deviations (%)**
di/dt (Module 1)	12.7 A/ μsec	12.9 A/ μsec	1.86%
di/dt (Module 3)	13.9 A/ μsec	14.0 A/ μsec	0.84%
Max. Current Module 1 @47us	595.55 A	608.37 A	2.11%
Max. Current Module 3 @47us	651.05 A	658.20 A	1.09%

It can be seen that the model vs the measurement values are well aligned for the first pulse ramp up. There are certain factors for the deviations however, like the voltage injected is not exact to rise the current to the expected values. This will result in over or under current values. Secondly, the expected value of current is calculated as follows:

$$V = L_{\text{load}} \cdot \frac{di}{dt} \tag{4.2}$$

Where, $V = 1350V$(same as measurement value), $L = 1.5 * 34.1 = 51.15\ \mu H$ (from load inductor name plate) and dt is taken as $50\mu sec$ considering the ramp up time.

Here, only the load inductance is considered for di/dt rise, and all the other parasitic inductances are considered negligible. Therefore, it is possible to observe some deviations in the modeled values.

Thirdly, Since the model has certain limitations for instance, it takes course segments in comparision with the actual busbar and each segment considers the same current through itself. It is observed from FASTHENRY computation that though the resistance values increases with increasing segments the inductance value actually decreases with increasing segments and vice-versa. With lower inductance higher current rise shall be observed.

Also, the skin effect is not taken into consideration for the busbars as they are considered as a uniform conductive plane. This will give lower impedance values as compared to the real values.

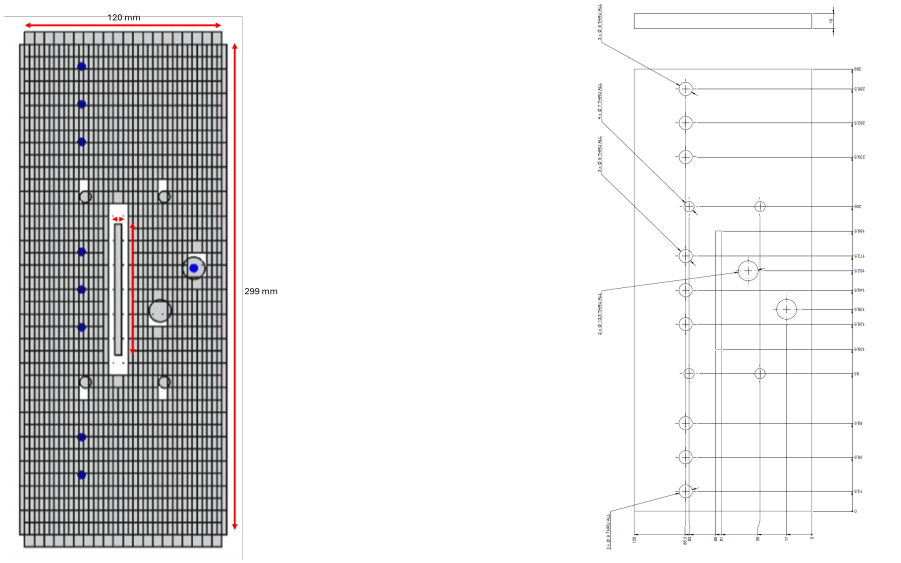
Depending on the weightage of these factors, the impedance values may observe some deviations from the real measurements.

Additionally, It can be seen that the first pulse is $47\mu sec$ instead of $50\mu sec$ due to the dead time introduced by the controller unit for de-saturation protection.

4.2 Sensitivity Analysis

The objective of this section is to observe the change in the Z-Matrix by tweeking the rectangular cut-out in the switch-node busbar. By doing this, the impact on the layout impedance on the hole positioning and size can be known. By iterative computations, it will ensure minimizing the role of external layout causing current imbalances.

Initial dimensions and position of the cutout is defined in the figure 4.5 below:



(a) Switch-node busbar model

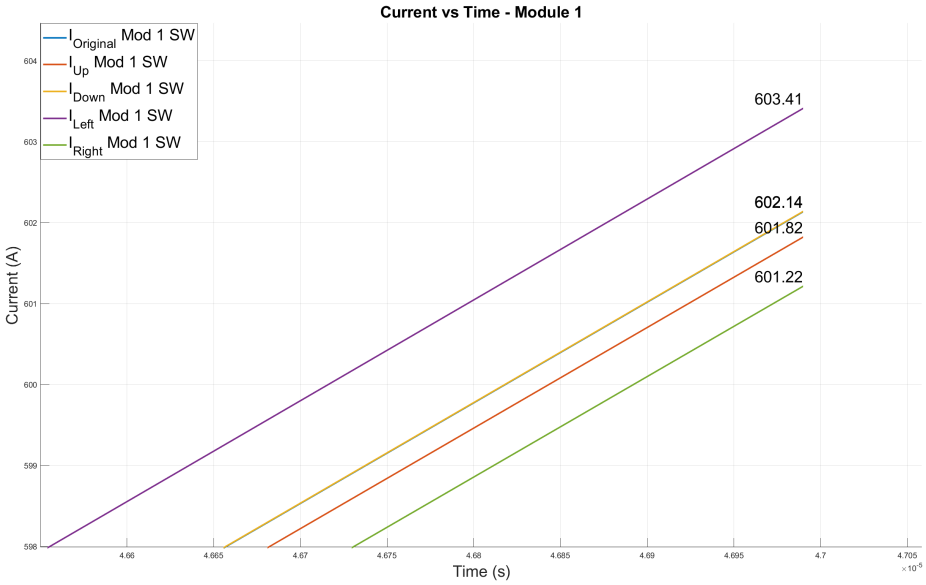
(b) Switch-node busbar dimensions

Figure 4.5: Switch-node busbar - Details

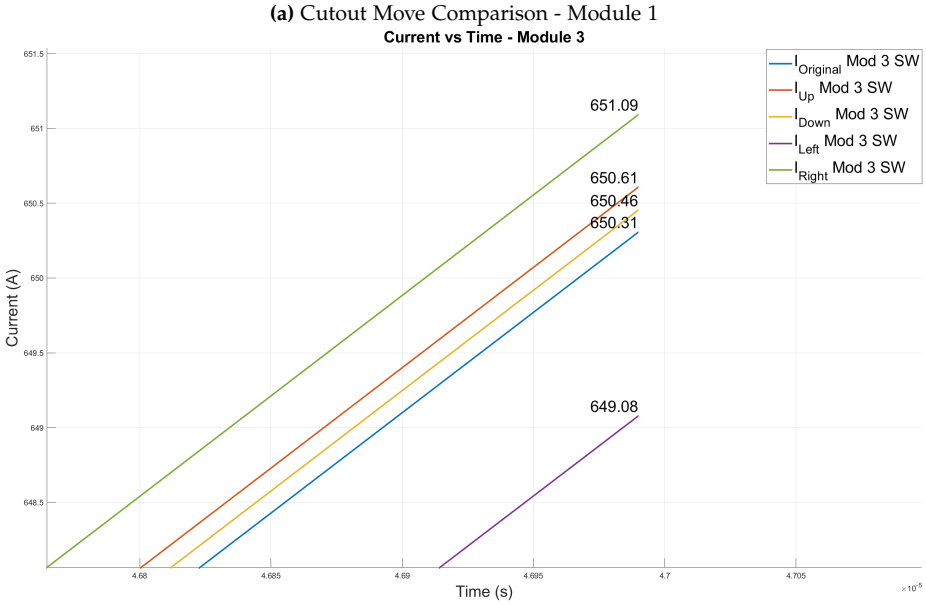
As it can be seen that the cutout dimensions are **80 mm x 4 mm**, and is placed at the position provided in figure 4.5b. As this is a relative analysis, all the other holes in the busbar are removed for simplicity. As due to these holes present, there is a possibility of holes merging upon movement which will lead to incorrect results. The FASTHENRY code can be referenced from the appendix B.3.

4.2.1 Change in cutout position

The cutout is moved in all four directions, namely, up, down, left and right by 10 % cutout length (8 mm) to observe the variation in current ramp up during the first pulse.



(a) Cutout Move Comparison - Module 1



(b) Cutout Move Comparison - Module 3

Figure 4.6: Impact of cutout movement in Switch-node busbar

Table 4.2: Observations - Change in cut-out position - Module 1

Position of Cutout	**Change from original position%**
Module 1	
1. Original Position	$\frac{602.14 - 602.14}{602.14} \times 100 = 0.000\%$ (4.3)
2. Upward Movement - 8mm	$\frac{601.82 - 602.14}{602.14} \times 100 = -0.053\%$ (4.4)
3. Downward Movement - 8mm	$\frac{602.14 - 602.14}{602.14} \times 100 = 0.000\%$ (4.5)
4. Left Movement - 8mm	$\frac{603.41 - 602.14}{602.14} \times 100 = 0.211\%$ (4.6)
5. Right Movement - 8mm	$\frac{601.22 - 602.14}{602.14} \times 100 = -0.153\%$ (4.7)

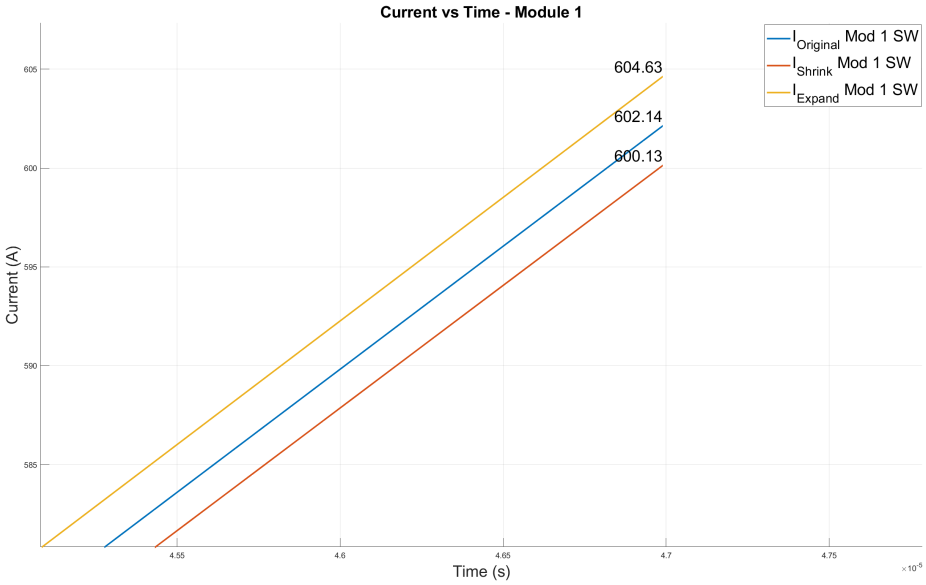
Table 4.3: Observations - Change in cut-out position - Module 3

Position of Cutout	**Change from original position%**
Module 3	
1. Original Position	$\frac{650.31 - 650.31}{650.31} \times 100 = 0.000\%$ (4.8)
2. Upward Movement - 8mm	$\frac{650.61 - 650.31}{650.31} \times 100 = 0.046\%$ (4.9)
3. Downward Movement - 8mm	$\frac{650.46 - 650.31}{650.31} \times 100 = 0.023\%$ (4.10)
4. Left Movement - 8mm	$\frac{649.08 - 650.31}{650.31} \times 100 = -0.189\%$ (4.11)
5. Right Movement - 8mm	$\frac{651.09 - 650.31}{650.31} \times 100 = 0.120\%$ (4.12)

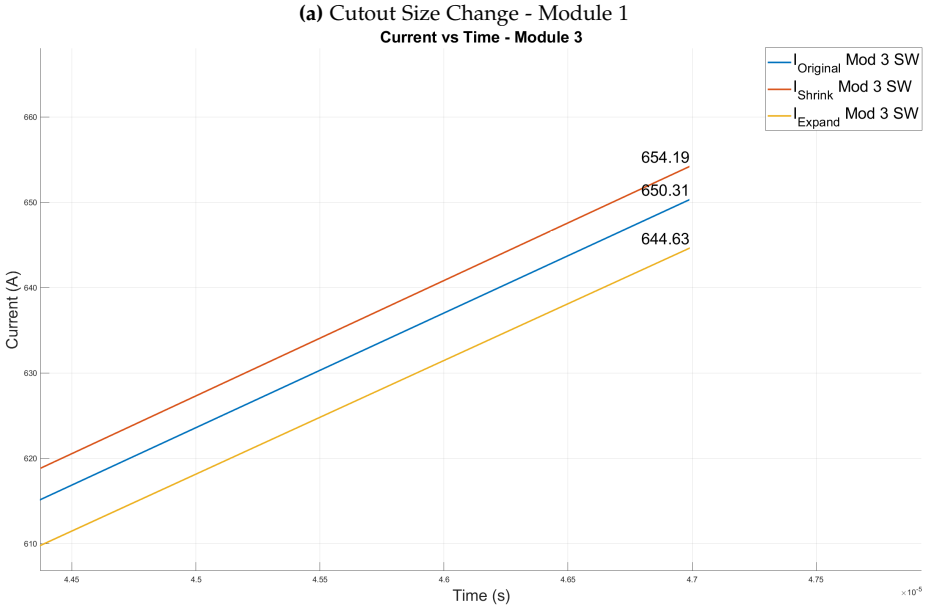
From the observations of tables 4.2 and 4.3, it can be observed that in both module 1 and module 3, the movement from horizontal movement (i.e., left and right) have more impact than the vertical movements (i.e., upward and downward).

4.2.2 Change in cutout size

The cutout is shrinked and expanded by 20 % cutout area to observe the variation in current ramp up during the first pulse. As 10 % shrink was producing same values, probably due to course segments defined in busbars, so it is decided to increase the variation percentage to observe the change. Only the length parameter is changed to match the area of the hole.



(a) Cutout Size Change - Module 1



(b) Cutout Size Change - Module 3

Figure 4.7: Impact of cutout size change in Switch-node busbar

Table 4.4: Observations - Change in cut-out size

Position of Cutout	Change from original position%
Module 1	
1. Original Size - 80 mm x 4 mm	$\frac{602.14 - 602.14}{602.14} \times 100 = 0.000\%$ (4.13)
2. Shrinked Size - 64 mm x 4 mm	$\frac{600.13 - 602.14}{602.14} \times 100 = -0.334\%$ (4.14)
3. Expanded Size - 96 mm x 4 mm	$\frac{604.63 - 602.14}{602.14} \times 100 = 0.414\%$ (4.15)
Module 3	
1. Original Size - 80 mm x 4 mm	$\frac{650.31 - 650.31}{650.31} \times 100 = 0.000\%$ (4.16)
2. Shrinked Size - 64 mm x 4 mm	$\frac{654.19 - 650.31}{650.31} \times 100 = 0.597\%$ (4.17)
3. Expanded Size - 96 mm x 4 mm	$\frac{644.63 - 650.31}{650.31} \times 100 = -0.873\%$ (4.18)

From the observations of table 4.4, it can be observed that in module 1 expanded size has larger impact than the shrinked size. Also, it seems counter-intuitive that with shrinked size the current goes down meaning the inductance value is higher than the original cutout. But since module 1 is placed on the bottom node, the influence of upward movement of hole due to shrinking is more than the influence of shrinking itself.

For Module 3 as well, the impact of expansion is more than the size reduction. Also, here as the module is connected on middle node, the impact of movement is negligible over the influence of size impact.

From the tables 4.2, 4.3 and 4.4, it can be seen that both of them have their influence on the impedances seen by the modules. By automating this process of movement and size-change, the perfect positioning and size of the cut-out can be obtained which will highly reduce the impact of DPT layout on the current imbalances.

Chapter 5 Simulation and Results

5.1 Simulation Description

This section focuses on the simulations for the test setup. This will ensure to have a feel of the system before going into the lab testing.

Firstly, an ideal simulation of the setup was performed in PLECS to get the expected current levels at different timings in the system. The drain-to-source current (I_{DS}) , switch-node current ($I_{sw-node}$), drain-to-source voltage (V_{DS}) and gate voltages (V_{GS}) are measured for each module similar to the way it was done during lab testing. Data for the components involved in the system are taken from datasheet.

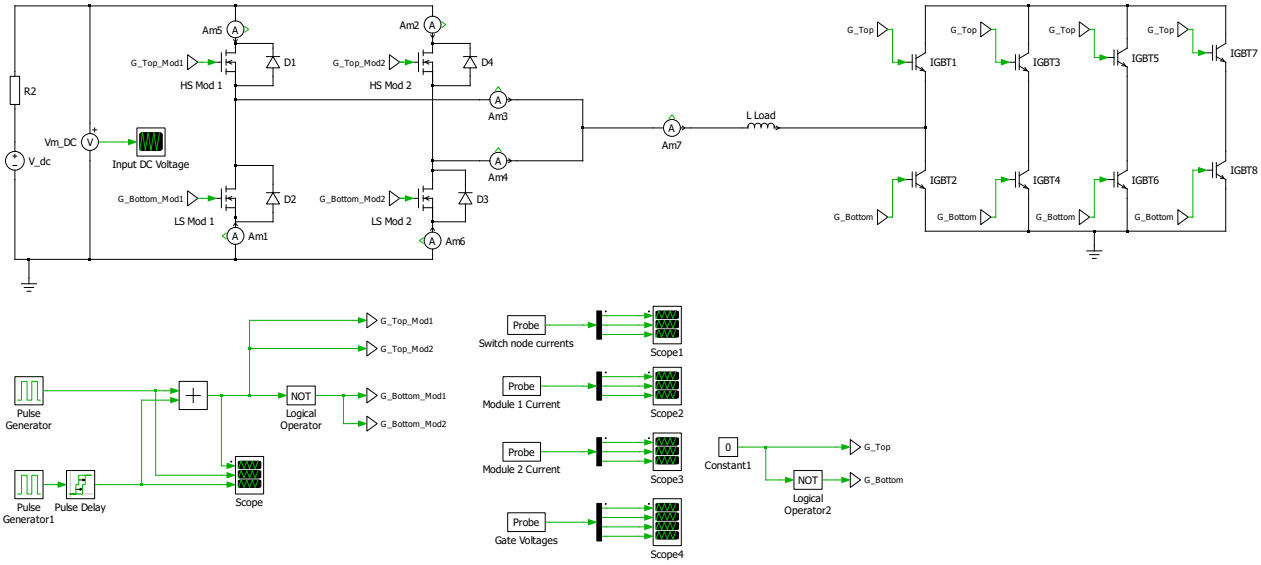


Figure 5.1: PLECS simulation

A SPICE model for the module would be helpful to analyze the system behavior in advance, however, it was not feasible to develop a model taking into consideration the project timeline and limited data availability from the manufacturer for analysis.

As the project focuses more on the layout of the system over the module itself to balance out the imbalances in the current sharing, a simulation on Fast Henry is done of the switchnode busbars which are majorly responsible for the observed behavior as shown in section 7.1. Since, this is an iterative process, two different busbar arrangements were taken into consideration for matching the system impedances as shown in the chapter 7.

5.2 Simulation Results

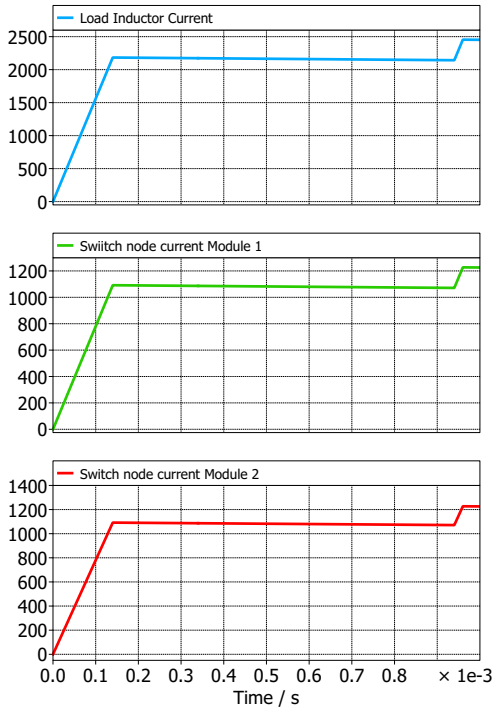
The DPT setup ideal simulation is conducted for the sole purpose of observing the current rise measured at different locations in the setup at different time intervals before conducting the lab experiment.

Similar voltage and current ratings are considered as in the Testing for 2 modules 7.1 to get an idea of the current values to be observed during testing.

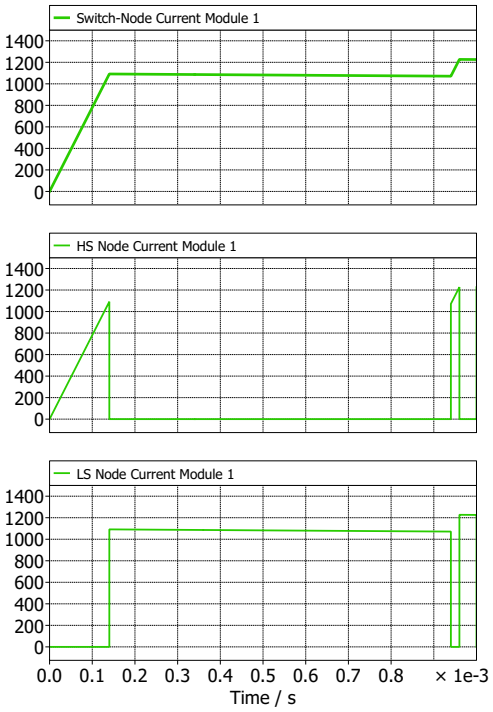
Table 5.1: Simulation Parameters

Parameter	Description
1. DC-Link Voltage	800 V
2. Load Inductor Current	2000 A
3. First Pulse Duration	140 us
4. Free-wheeling Pulse Duration	800 us
5. Second Pulse Duration	20 us

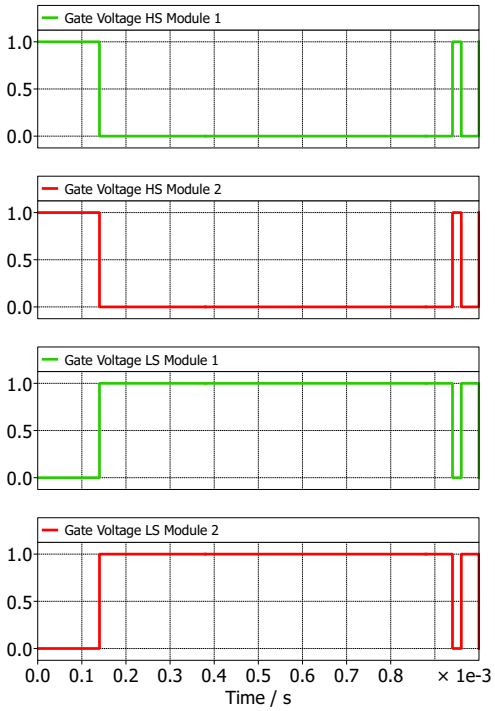
Here are the results from the testing shown in figure 5.2:



(a) Switch node currents for two paralleled modules



(b) Individual module currents



(c) Gate Voltages - Module 1 and Module 2

Figure 5.2: Simulation results for DPT

Chapter 6 Laboratory Setup

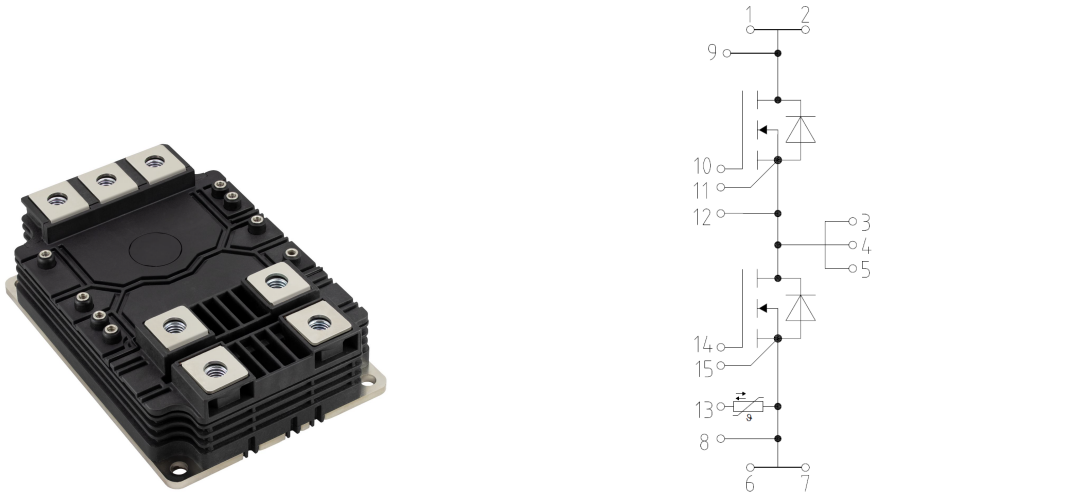
This chapter introduces the hardware setup prepared for the SiC MOSFET modules. As mentioned in section 3.2, the setup was developed similar to the arrangement of power converter AFE as well DC-DC buck converter solution offered by KK Wind Solutions. The setup is operated on rated voltages and current values to emulate the conditions of operation required by the electrolyzer unit.

6.1 DPT Segments

As the system was initially developed to test the Si-IGBT units, it is necessary to add modifications to the setup for accommodating the SiC MOSFET power module testing. In this section, all the segments of the setup will be introduced along with their specifications and usage details.

6.1.1 SiC MOSFET Module

As this module is not available for commercial purposes, the identity of the module cannot be revealed. However, module structure, basic connection details, power ratings, operating voltages and currents are listed below.



(a) 100 mm MOSFET Power Module **(b)** Connection diagram - 100 mm MOSFET Power Module

Figure 6.1: MOSFET Power Module Structure and Connection Diagram

The specifications of MOSFET Module in figure 6.1 are given the table 6.1:

Table 6.1: Specifications - 100mm MOSFET Power Module

Parameter	Symbol	Rating
1. Drain-source voltage	V_{DSS}	2300 V
2. Drain current	I_{DN}	2000 A
3. Repetitive peak drain current	I_{DRM}	4000 A
4. On-state gate voltage	$V_{GS(on)}$	15...18 V
5. Off-state gate voltage	$V_{GS(off)}$	-5 V
Gate Driver Boards	Master Board - 2SILT1200T2A0C−33	Slave Board- 2SMLT0220D2C0PRT−23−SiC

Note: One master gate driver can be used to control upto 4 SiC MOSFET Modules using slave drivers assigned in daisy chain arrangement.

6.1.2 COMIC Board

The COMIC board also known as common-interface board provides an interface between the KK controller unit and the master gate driver of the SiC MOSFET power modules.

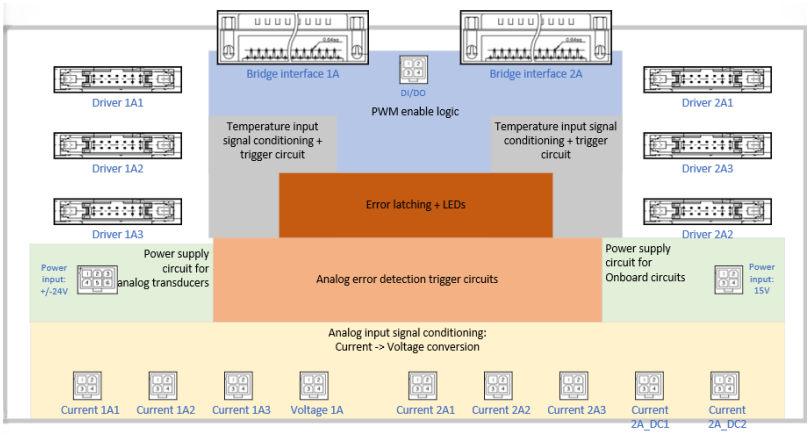


Figure 6.2: COMIC Board

As shown in figure 6.2, the common interface board consists of auxiliary power supplies for the gate driver unit, condition monitoring capability including current, voltage and thermal measurements, and provides gate signals to and carry error or alarm messages from the gate driver to the KK controller unit.

6.1.3 Connecting Board

As the COMIC board is developed to directly interface with the gate driver unit for the IGBT power modules, it is not pin to pin compatible with the SiC MOSFET power module gate driver. For minimizing the modification, a connecting board is developed providing

connection capability of the COMIC board to the Gate driver unit. Figure 6.3, provides a SLD for the connection.

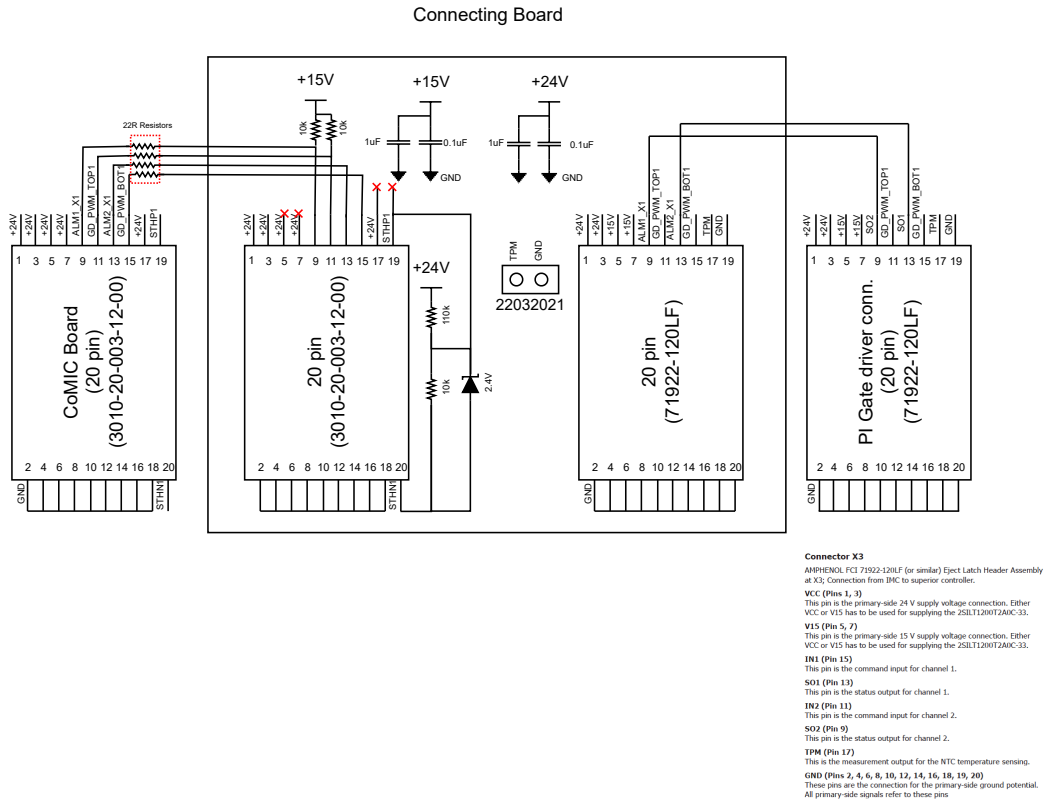


Figure 6.3: Connecting Board for Gate Driver

6.1.4 Load Inductor

The load reactor is a crucial segment of the Double Pulse Testing. It is a 3-phase reactor whose terminals are shorted as shown in figure 6.4. It is required for the ramp up operation and decides the di/dt at an applied voltage across its terminals and for power circulation during free-wheeling operation. The inductance value and current handling capability are the critical features to look into before selecting the inductor.

Figure 6.4: Load Inductor with Name Plate Details

Following are the details of the inductor unit,

Table 6.2: Specifications - Load Inductor

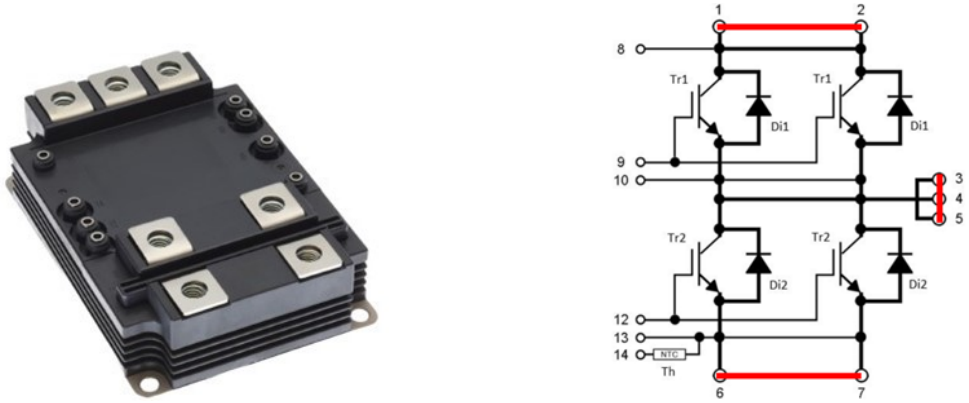
Parameter	Rating
1. Type	3-phase grid reactor
2. Rated Inductance, L	$34 \pm 7\ \mu H$
3. Rated Current, Arms	3227.5 A
4. Peak Load Duration, 3 secs	3873 A (1.2 * Rated Current)

For the initial calculations the lowest values of inductance is taken, that is, 34 μH. As per the connection shown in the figure 6.4, the value for single phase is $L = 1.5 * 34.1 = 51.15$ μH.

The DPT purposes, the inductance and current values are sufficient to get the desired power circulation using the testing software available inside the lab.

6.1.5 Si-IGBT

This module is also not available for commercial purposes, the identity of the module cannot be revealed. However, module structure, basic connection details, power ratings, operating voltages and currents are listed below.



(a) 100 mm IGBT Power Module **(b)** Connection diagram - 100 mm IGBT Power Module

Figure 6.5: IGBT Power Module Structure and Connection Diagram

The specifications of IGBT Power Module in figure 6.1 are given the table 6.1:

Table 6.3: Specifications - 100mm IGBT Power Module

Parameter	Symbol	Rating
1. Collector-emitter voltage	V_{CES}	2000 V
2.Collector current	I_C	1200 A
3. Repetitive peak collector current	I_{CRM}	2400 A
4. Gate-emitter voltage	V_{GES}	$\pm$20 V
5. Collector-emitter saturation voltage	$V_{CE(sat)}$	2.15 V

The DC link capacitor is considered sufficient to stabilize the input voltage during the testing and is considered as a black-box for the system.

6.2 Setup Assembly

This section presents the complete setup with the load inductor. The various system segments are identified in the physical setup.

6.2.1 DPT System Identification

The setup along with the connected load inductor is shown in the figure 6.6 below:

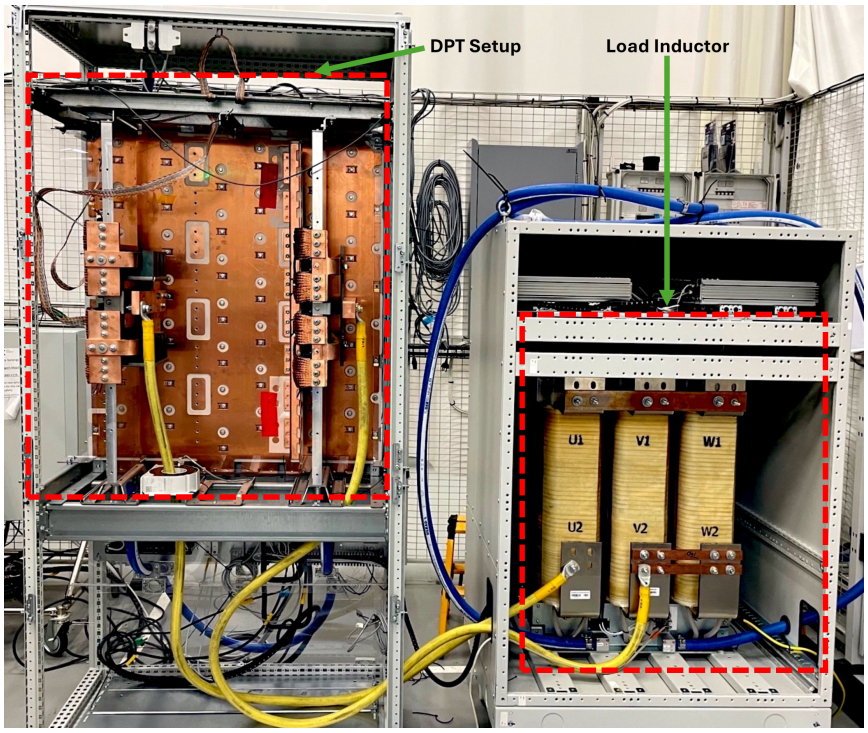


Figure 6.6: Complete DPT Setup with Load Inductor

The figure 6.7 below identifies the components of the DPT setup shown in figure 6.6, it includes, the placement of SIC MOSFET power modules, gate drivers, DC busbars, DC-link capacitors, DUT identification, Testing unit - Phase 2 identification and placement of inductor cable on the switch-node busbar.

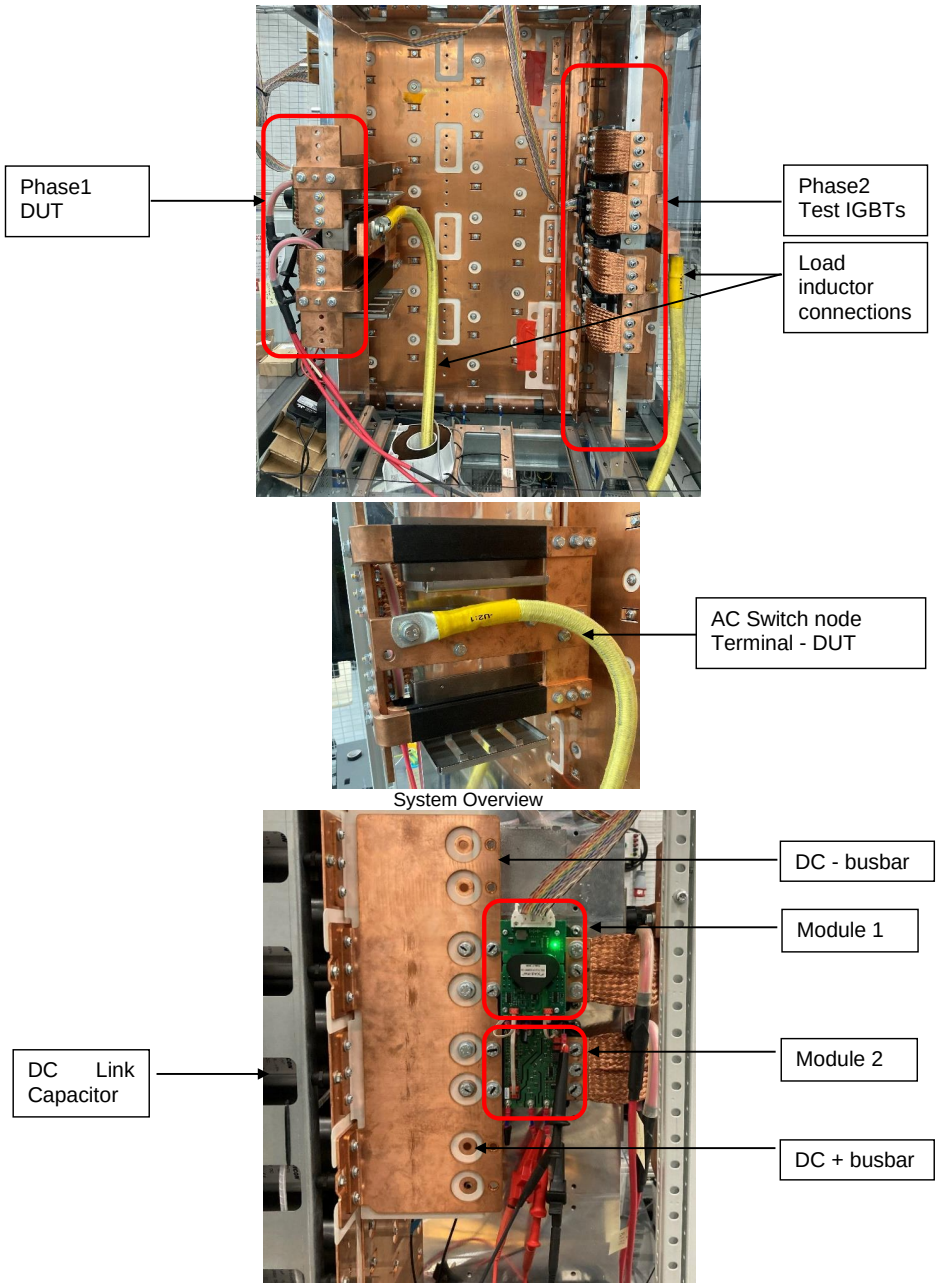


Figure 6.7: DPT Setup Details

6.2.2 DPT Power Cycling

Using the values of the system components, the DPT power cycling can be explained as observed in the measurement results shown in figure 7.2 as follows:

Table 6.4: DPT Power Cycling

Parameter	Rating
1. Input Voltage	800 V
2. Rated Inductance, L	51.15 μH
3. First Pulse Duration	140 us
4. Free-wheeling Pulse Duration	800 us
5. Second Pulse Duration	20 us
6. MOSFET Rdson (2 units connected)	0.94 m Ω (at 25 °C)
6. IGBT Forward Voltage (4 units connected)	1.6 V (at 25 °C) (from datasheet graph)

High Side MOSFET - Active State

The section 3.3a shows the current circulation in the active state, the power cycling analysis is done on the DPT setup.

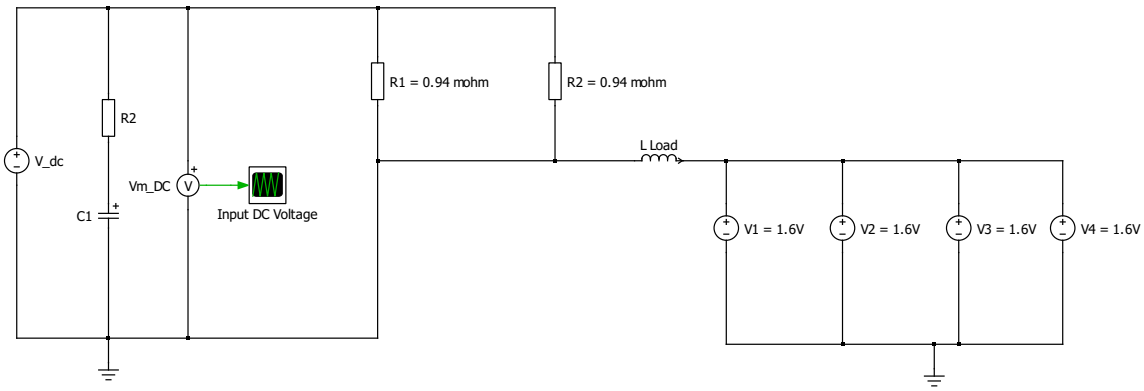


Figure 6.8: HS MOSFET Testing

Considering the values from above table 6.4, for the HS MOSFET active state, following calculations are done for the current levels. Taking 'I' as the current through one MOSFET and considering equal current sharing,

$$V_{DC-link} - R_1 * I - 1.6V = L_{\text{load}} \cdot \frac{(0 - 2 * I)}{(0 - 140)} \tag{6.1}$$

Computing the equation 6.1, gives $I = 1091.2A$ making current through the inductor as $I_L = 2 * I = 2182.4A$.

High Side MOSFET - Free-wheeling State

The section 3.3b shows the current circulation in the free-wheeling state, the power cycling analysis is done on the DPT setup.

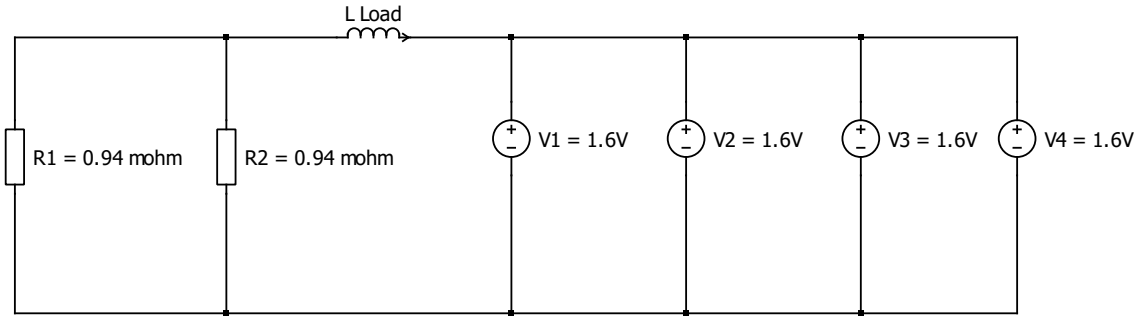


Figure 6.9: Free-Wheeling State

Here, the idea of showing this is to understand the behavior of the system during free-wheeling state. Due to the voltage developed because of the MOSFET and IGBT conduction, the inductor current falls with time.

$$-0.94m * I - 1.6V = V_L \tag{6.2}$$

The equation gives a voltage of $-2.63V$ across the inductor. Therefore, the change in current can be computed using the equation 4.2 gives the current drops from $2182.4A$ to $2141.3A$ for $800\mu s$ time duration.

Chapter 7 Testing and Validation

The chapter 7 focuses on the results obtained from the Double Pulse Testing (DPT) and analysing them for identifying the underlying causes and possibly solving certain issues. It is divided into three major problems observed from the testing and its further analysis.

7.1 System Testing

This section deals with the testing of the two SiC half-bridge modules for power levels sufficient for the application and details the observations of the test.

7.1.1 Testing for 2 modules

There are some initial tests done on individual modules to see the voltage and current handling capabilities of the modules starting from 100V operation to 1350 V operation at different pulse widths. This ensured the power modules are working properly without fail.

Initial Testing - 2 Modules paralleled

An initial test is conducted paralleling two SiC MOSFET half-bridge modules on a Double Pulse Test setup (DPT). As this SiC technology is still in the development phase and has not matured yet, it is important to observe how the system behaves. As shown in section 5.1, an ideal simulation of the setup was done before the test using the DC link capacitor and load inductor values before the test was conducted.

The modules are tested for the following ratings:

Table 7.1: Testing of two Half-bridge modules

Parameter	Rating
1. DC Link Voltage	800V
2. Total current through load inductor	2000 A

To achieve approximate current values, the test was conducted using given timings,

Table 7.2: Test Conditions

Description	Time Duration
1. First Pulse Duration	140 us
2. Free-wheeling Pulse Duration	800 us
3. Second Pulse Duration	20 us

The free-wheeling phase is intentionally kept higher to see the convergence of currents.

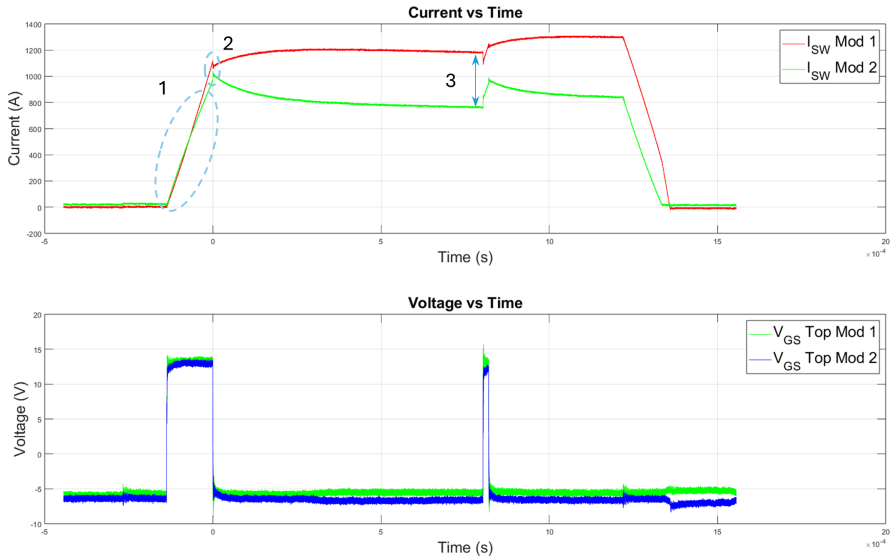


Figure 7.1: Initial Double Pulse Test Observation

As shown in figure 7.1, it can been seen that the initial testing revealed three different segments of problems marked as 1, 2 and 3 in the figure.

1. Firstly, current sharing deviation between the modules is more than 10 % with di/dt of 6.99 A/us and 8.18 A/us of Module 1 and Module 2 respectively. Since both the values observed are above 5 % tolerance limits, it is required to look at the problem in more detail and potentially reduce the deviation.

2. Secondly, current jumps are observed at the turn on of MOSFETs in the lower leg transitioning from the turn off of the MOSFETs in the upper leg. This can be seen as marked 2 in the figure 7.1. These jumps are initially assumed from the imbalance in R_{dson} of the bottom and top legs between both the MOSFET modules.

   Following are the values of R_{dson} observed for testing at 10A of current:

Table 7.3: Rdson Values

SiC Module	**Rdson Top**		**Rdson Bottom**	
	Forward Conduction (mΩ)	**Reverse Conduction** (mΩ)	**Forward Conduction** (mΩ)	**Reverse Conduction** (mΩ)
Module 1	0.94	0.94	1.02	1.02
Module 2	1.03	1.03	0.98	0.98

   This might explain that the current jumps were due this imbalance in Rdson values. However, this is not the case. Firstly, these observations are for 10A and are not applicable for rated power applications. Secondly, due to current imbalance, the temperature will be varying in each MOSFET and will be equalised due to Rd-

son dependance on temperature.

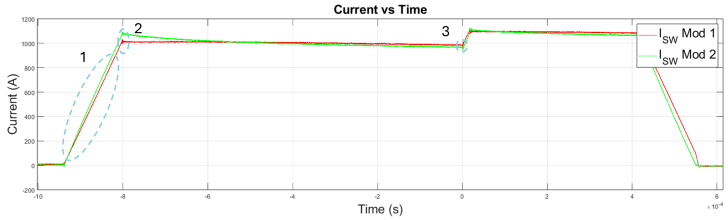
3. Thirdly, It can be seen that during the freewheeling stage, the currents are deviating more than 400A where, this stage is extended longer than the typical duration to see if the current values converge at some point. Since, this was not the case, the problem became interesting to look at. It was decided to delve deeper into the system and further tests were conducted to observe the repeatability of the problem.

Disclaimer: The problem in the 3rd stage was due to a slightly loosened screw on the switching node!! This led to imbalance in resistance between the modules causing huge current deviations.

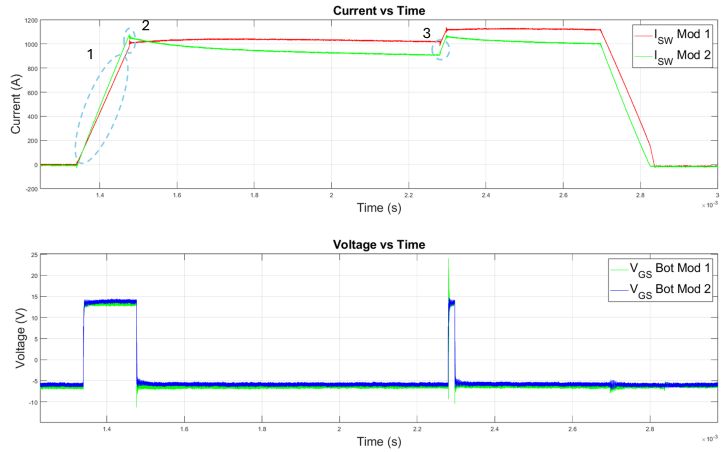
Although, this turned out to be a mistake in the beginning, it was a stepping stone into the project as it instigated to look at the problem critically.

Testing for 2 modules paralleled after setup correction

After validating the setup, the system is again turned on and tested for the same test conditions as in table 7.1. Following are the results of this testing:



(a) Top MOSFET Testing



(b) Bottom MOSFET Testing

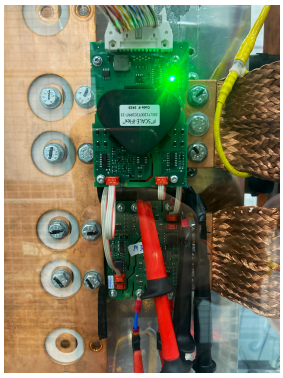
Figure 7.2: Two SiC Module Testing using DPT Setup

From the figure 7.2a, it can be seen that there is an improvement in the test results on all the three segments identified above. With current deviation at commutation (stage 2) less than 10 % with di/dt of 7.36 A/us and 7.77 A/us of Module 1 and Module 2 respectively. Where the third segment (free-wheeling stage) is almost equalised at the end of the pulse duration.

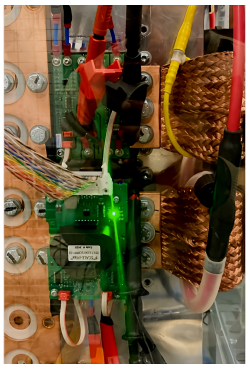
For verifying the behavior, Bottom MOSFET was also test as shown in figure 7.2b. By conducting this test, it was observed that although the first two segments (ramp up stage and commutation stage) are similar to the Top MOSFET results for both the modules, however, segment 3 showed deviations of more than 100A between the modules. Although this value is smaller, but similar behavior is still observed as the initial test results.

To investigate into these switching behaviors, two approaches were proposed:

1. **Gate Driver Swap** - In this method, each module's physical position is kept constant and while the master gate driver was shifted from Module 1 to Module 2 and the observations from both results are shown in figure 7.4.



(a) Module 1 - Master Gate Driver



(b) Module 2 - Master Gate Driver

Figure 7.3: Gate Driver Swap

2. **Module Swap** - In this method, modules themselves are swapped physically and the master gate driver stays on module 1 in both the cases. The observations from both results are shown in figure 7.5.

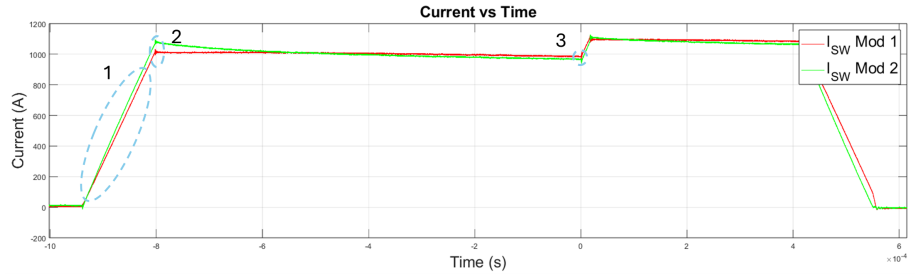
It is understandable that there could be more approaches for the problem at hand. For instance, looking into the gate driver circuit and SiC power module internal structure to understand the problem better. However, As mentioned in segment 1.3, changes in the modules and gate driver are not possible as they are bought out external equipments. Therefore, the above mentioned approaches were deemed appropriate to proceed.

Note: All the tests are done for the same testing conditions as mentioned in 7.1 to make the comparison feasible.

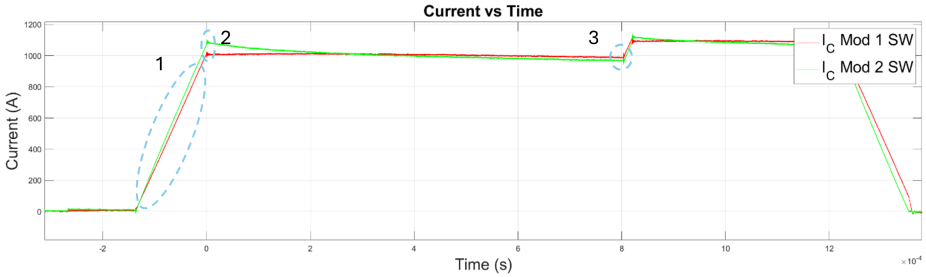
7.1.2 Observations - Investigation Approaches

1. **Gate Driver Swap**

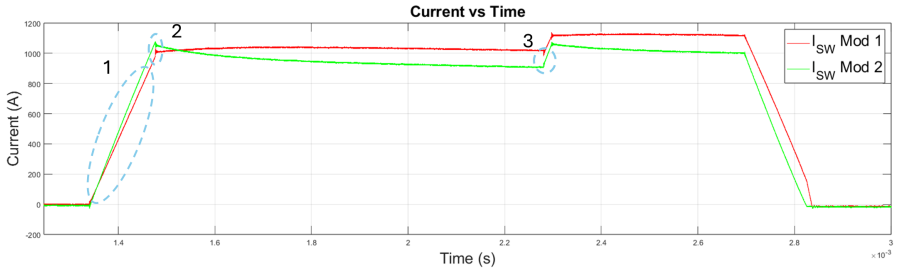
   The following are the results from the gate driver swap:



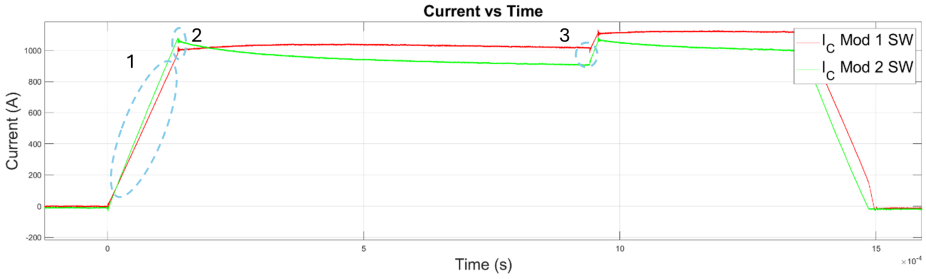
(a) Top MOSFET Test - Master GD on Module 1



(b) Top MOSFET Test - Master GD on Module 2



(c) Bottom MOSFET Test - Master GD on Module 1



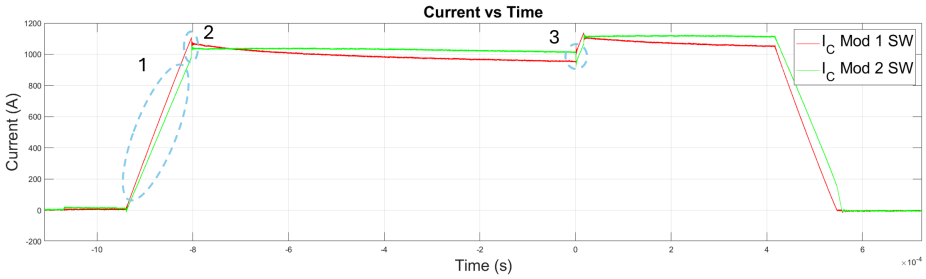
(d) Bottom MOSFET Test - Master GD on Module 2

Figure 7.4: Gate Driver Swap Results

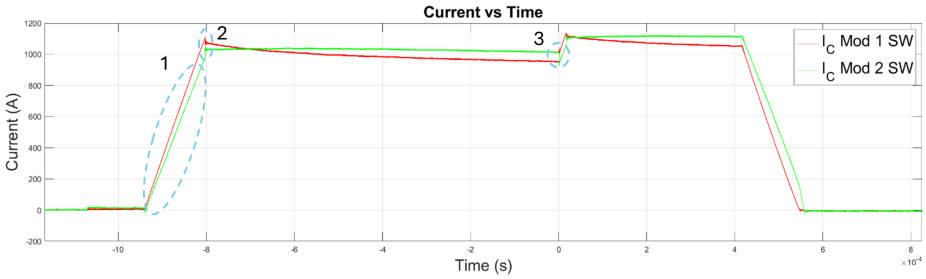
From the figure 7.4, it is concluded that the delay in signal from the master gate driver consequently to the slave gate driver on each module in the daisy chain arrangement does have little to no effect on the system performance. Therefore, it is assumed that the gate driver has negligible impact in obtaining the results observed in the above figure.

2. **Module Swap**

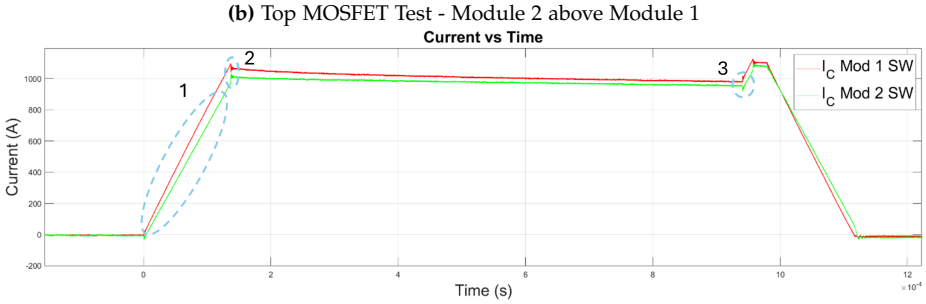
The following are the results from the module swap:



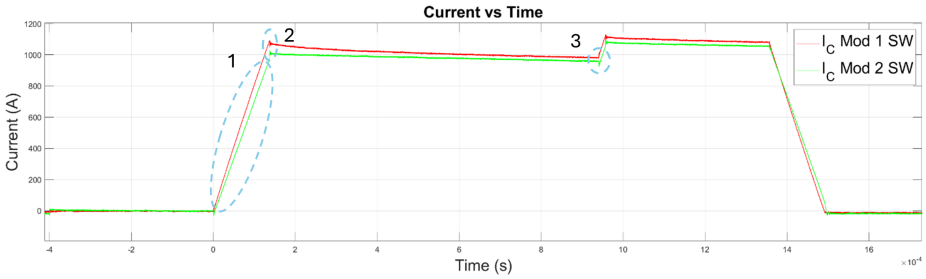
(a) Top MOSFET Test - Module 1 above Module 2



(b) Top MOSFET Test - Module 2 above Module 1



(c) Bottom MOSFET Test - Module 1 above Module 2



(d) Bottom MOSFET Test - Module 2 above Module 1

Figure 7.5: Module Swap Results

From the figure 7.5, it can be interpreted that the behavior of the modules is different based on the position of the module and more closely, the behavior of top MOSFET of module 1 above module 2 arrangement aligns better with the bottom MOSFET behaviour of module 2 above module 1 arrangement. This is similar for the other two cases.

Based on these observations, it is prudent to consider the impact of the DPT setup layout significant and is given higher weightage over the other governing factors. Therefore, in this project, we sought out to investigate and further modify the layout of the system assuming other parameters of the system ideal.

7.2 Decoding Switching Behaviour

From the section 7.1, it is determined that the layout of the DPT system acts as a major contributor in shaping the waveforms as observed, several tests were conducted to determine the dependence of various components in the system.

There are in total 28 tests conducted for the layout, involving different arrangements of - current sensors & inductor cable connections, shorting of both the AC switch node busbars for more balanced current sharing. Since, all the tests cannot be listed in this chapter, only certain tests are written down. However, all the test cases and their results can be referred to the attached excel sheet with the submission.

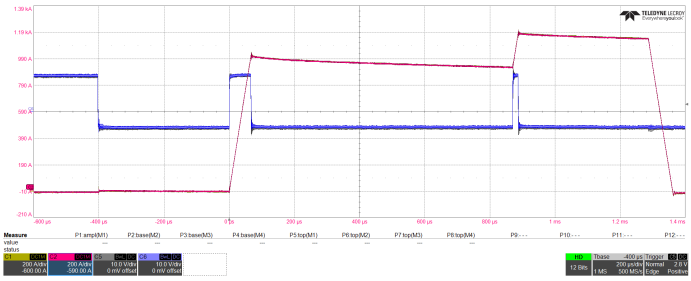
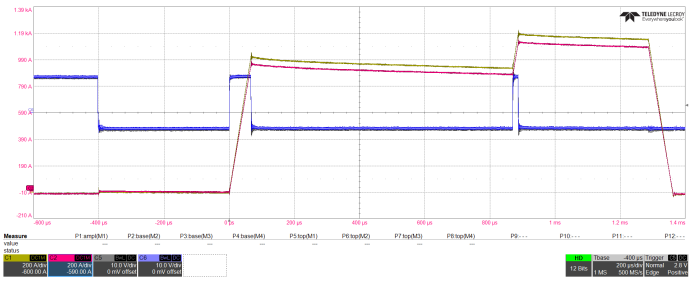
7.2.1 Measurement Devices

Starting with the measurement devices, calibration of the current sensors is done to maintain the authenticity of data observed during measurement. There are several possible problems some of which are,

1. **Zero Error** - There can be a zero error in the Rogowski coils used for measurement and the absolute difference in current values during the test might not be this high.
2. **Improper Placement and Orientation** - If the coil is not correctly positioned around the conductor or aligned with the current flow, it can lead to distorted measurements due to uneven integration of current at different segments of the coil.
3. **Environmental Factors** - External magnetic fields and temperature variations can also impact the accuracy of Rogowski coils as well.

For mitigating the issues with measurement, the coil was tested and the results are listed below:

Table 7.4: Rogowski Coil Testing

Test Description	Active Component	Module Placement	Channels	VDC (V)	Remarks
Test 1- Two rogowski coils on common AC connection and the conductor in center of both sensors.	LS MOSFET	Module 2 above Module 1 below	Ch1 and Ch2 are on common AC	800	Very equal current measurement on both rogowski coils.
					
Test 3 - Two rogowski coils on common AC connection. 1 conductor placed very asymmetrically, as well as the loop of the coil is not completely closed.	LS MOSFET	Module 2 above Module 1 below	Ch1 and Ch2 are on common AC	800	Not so equal current, but the current difference is like different gains. Hence current in one probe is always lower than in the other. No crossing of current waveforms
					

As it can be seen from the table 7.4 that the placement of Rogowski coil is crucial for the tests for accurate results. It is not possible to mitigate the zero error, it would be prudent to consider the zero error in each measurement. However, fortunately there is no zero error in the coils.

7.2.2 DC-Link busbar and IGBT Testing Unit

After testing the Rogowski coils, the inductor was connected between the switch node of the MOSFET module and the DC-link negative at the highest and lowest positions in the busbar using cables. [Refer attached excel file].

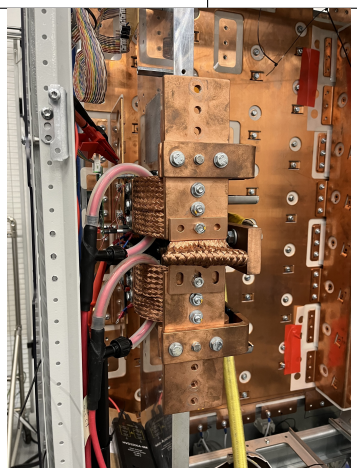
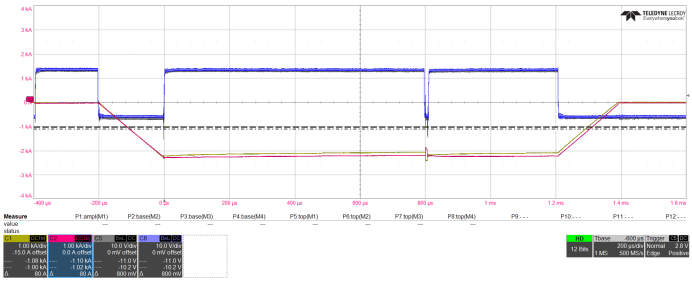
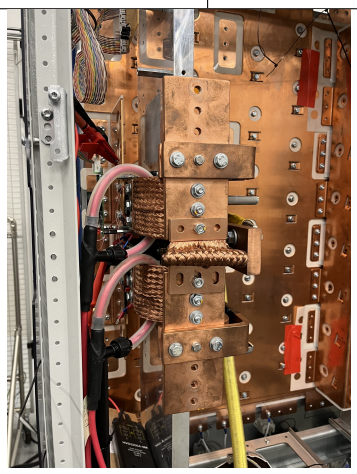
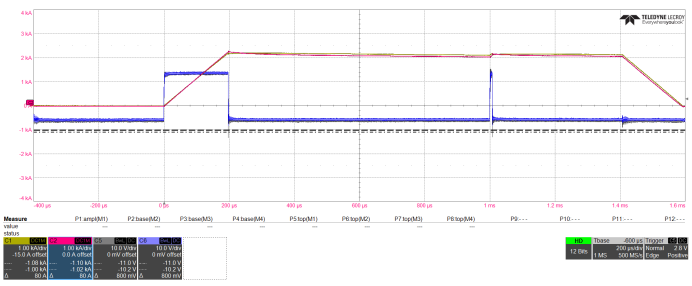
This basically replaced the influence of IGBT testing unit for the current sharing of the SiC MOSFET modules as the module get directly shorted with the DC positive. Along-with this, the influence of DC busbar can also be seen from the testing as the connection was done on different points on the DC-link busbar.

Upon testing the system under these conditions, exactly the same behavior was seen as the Test 6 [Refer attached excel file]. Also the waveform shape is similar to the testing conducted in Module swap as shown in figure 7.5. This makes it clear that the influence of IGBT testing unit as well as the DC link busbar on the DPT is negligible and these components can be considered ideal for the sake of the project.

7.2.3 Switch-Node busbar

As all the tests cannot be shown in this section, only the tests which provided positive results are displayed below:

Table 7.5: Testing Switch Node Busbar

Test Description	Active Component	Module Placement	Channels	VDC (V)	Remarks
Test 17 - Inductor placed on IGBT switch module. Braided busbar placed between module 1 and module 2 in front of test setup. 2000A test	HS MOSFET	Module 2 above Module 1 below	Ch1=below module Ch2=above module	1200	Very good current sharing both in active and freewheeling. A little jump and a little uneven sharing during freewheeling.
					
Test 18 - Inductor placed on IGBT switch module. Flex busbar placed between module 1 and module 2 in front of test setup. 2000A test	LS MOSFET	Module 2 above Module 1 below	Ch1=below module Ch2=above module	1200	Very good current sharing both in active and freewheeling. A little jump and a little uneven sharing during freewheeling.
					

From the results shown in table 7.5, it can be seen that the current sharing is quite synchronized and other segments , for instance, the current jumps as well as the free-wheeling behaviors are improved as well.

This change in waveform behavior demonstrates its high dependence on the switch node busbar. Based on these results, the following takeaways can be noted: Shorting both busbars using a flexible braided busbar balanced the impedance across all modules, as it provided multiple paths for current propagation. If one busbar offers higher impedance, the current can flow through the other busbar, and vice versa. To ensure consistent impedance across the entire busbar, it is essential to develop a single unit busbar. This will help maintain uniform current flow and improve overall performance. Secondly, these tests points towards investigating the influence of inductor cabling as well. The position of the cable in the busbar might impact the impedance seen by the modules due to magnetic coupling.

7.2.4 Inductor Cable on Switch Node busbar

An analysis is carried out by connecting the inductor cable at different positions on the switch node busbar and following are the observations:

Table 7.6: Testing Inductor Cable on Bottom Point of SW Node Busbar

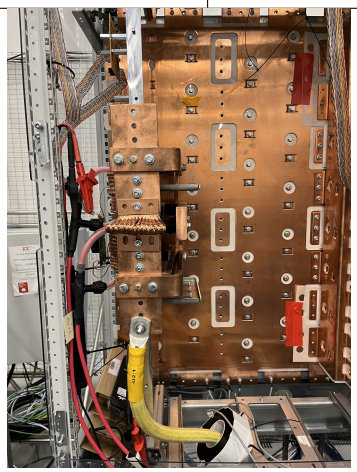
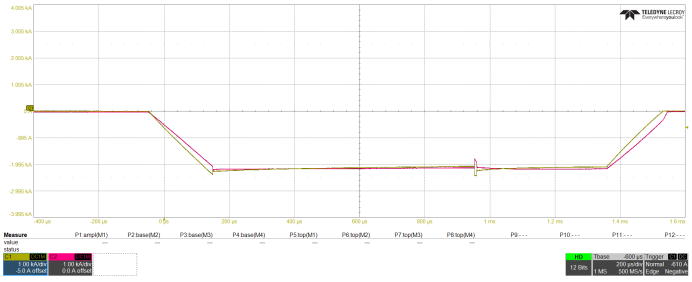
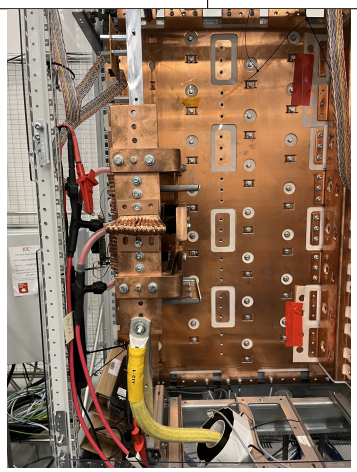
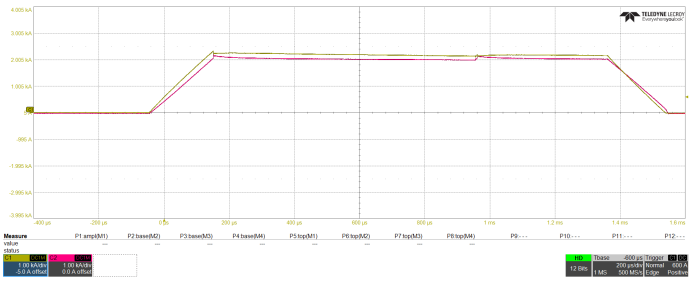
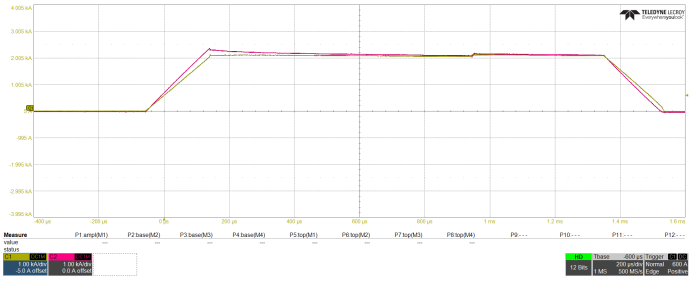
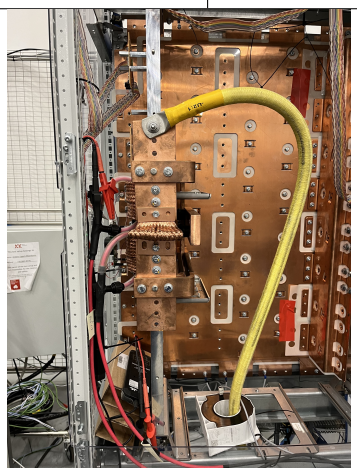
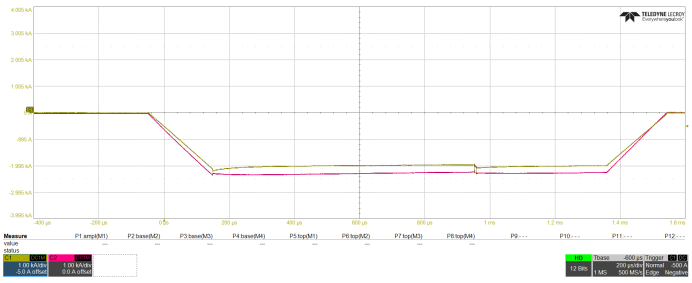
Test Description	Active Component	Module Placement	Channels	VDC (V)	Remarks
Test 25 - Inductor on IGBT switch module. Flex between ac busbars. AC cable connected in AC assembly on switch module lowest part.	HS MOSFET	Module 2 above Module 1 below	Ch1=below module Ch2=above module	1200	Very different ramp up current with highest in module 1 .Freewheeling stage - little difference.
					
Test 26 - Inductor on IGBT switch module. Flex between ac busbars. AC cable connected in AC assembly on switch module lowest part.	LS MOSFET	Module 2 above Module 1 below	Ch1=below module Ch2=above module	1200	Very different active current. Very different freewheeling current. Module 1 has highest current during ramp up.
					

Table 7.7: Testing Inductor Cable on Top point of SW Node Busbar

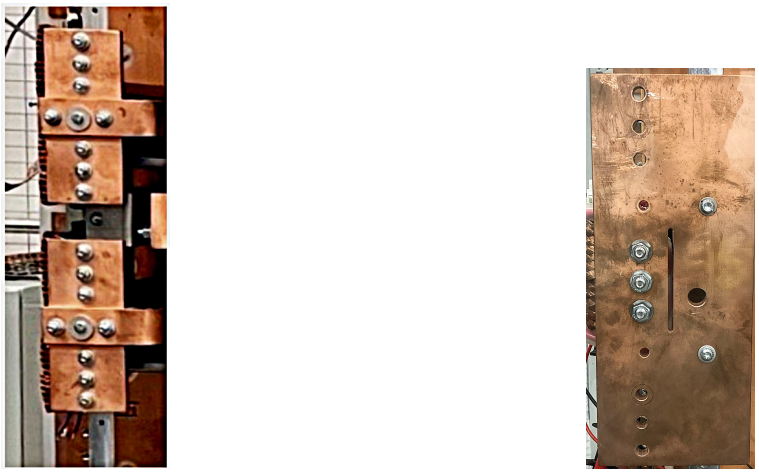
Test Description	Active Component	Module Placement	Channels	VDC (V)	Remarks
Test 27 - Inductor connected on IGBT power module. Flex between ac busbars. Other end of inductor cable connected on switch-node highest point.	HS MOSFET	Module 2 above Module 1 below	Ch1=below module Ch2=above module	1200	Very different active current. Quite equal freewheeling. Module 2 has highest current during ramp up.
					
Test 28 - Inductor connected on IGBT power module. Flex between ac busbars. Other end of inductor cable connected on switch-node highest point.	LS MOSFET	Module 2 above Module 1 below	Ch1=below module Ch2=above module	1200	Very different active current. Very different freewheeling. Module 2 has highest current during ramp up.
					

From tables 7.5, 7.7 and 7.6, it is concluded that these two - Switch node busbar and inductor connection cable - are the most impacting parts, governing the system behavior and should possess higher weightage while developing a solution for the current imbalance.

7.3 Layout Modifications

Building upon the premise established from the previous section, a new switch-node busbar is taken into consideration. As mentioned in the section 4.1, an already available busbar is taken for analysis.

Figure 7.6, shows both the currently used busbar (old busbar) as well as the new busbar taken into consideration.

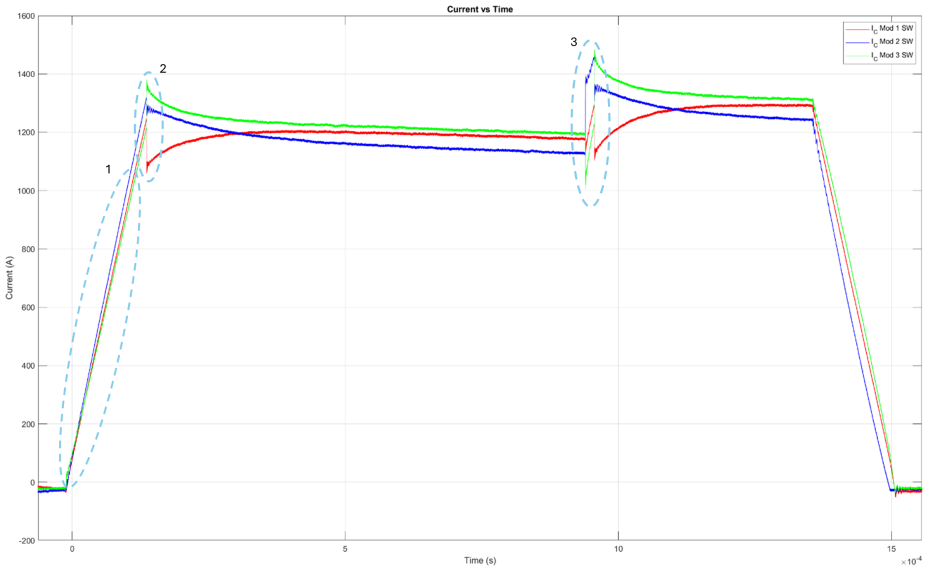


(a) Old Switch-node Busbar **(b)** New Switch-node Busbar

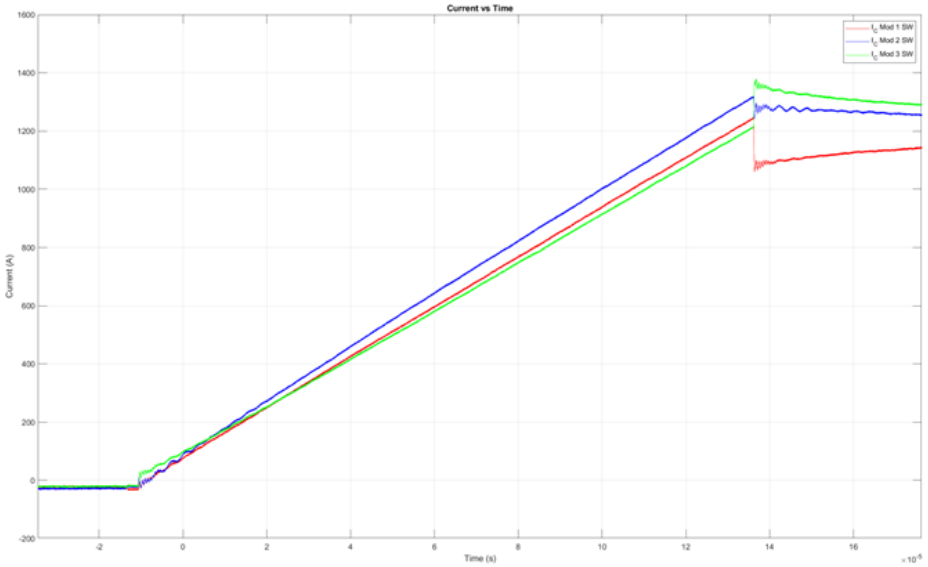
Figure 7.6: Old and New Switch-node Busbars

7.3.1 Testing with Three Power Modules

Three modules were tested on the Double Pulse Test setup using the new busbar, and the following are the results:



(a) DPT on three modules with new busbar



(b) Current Rise Three Modules

Figure 7.7: DPT testing of three modules with new switch-node busbar

As stated in chapter 4 as well, that seeking to the complex nature of these results, it is decided to carry an analysis on the two modules first. It can be seen from the figure 7.7 that the power module 2 (placed on the middle node) has the highest di/dt and the other modules have relatively closer current sharing performance during ramp up phase. Even during the free-wheeling phase, towards, the end the two modules show better current sharing as compared with the power module 2.

7.3.2 Testing with Two Power Modules

The system is setup for testing two SiC MOSFET power modules using the new busbar and the setup is done as shown in figure 7.8.

Figure 7.8: Double Pulse Setup with new busbar

The busbar and cable arrangement is similar to the modeled arrangement shown in figure 4.4a. The testing is carried out on the modules after the FASTHENRY analysis and following are the results of the ramp up stage.

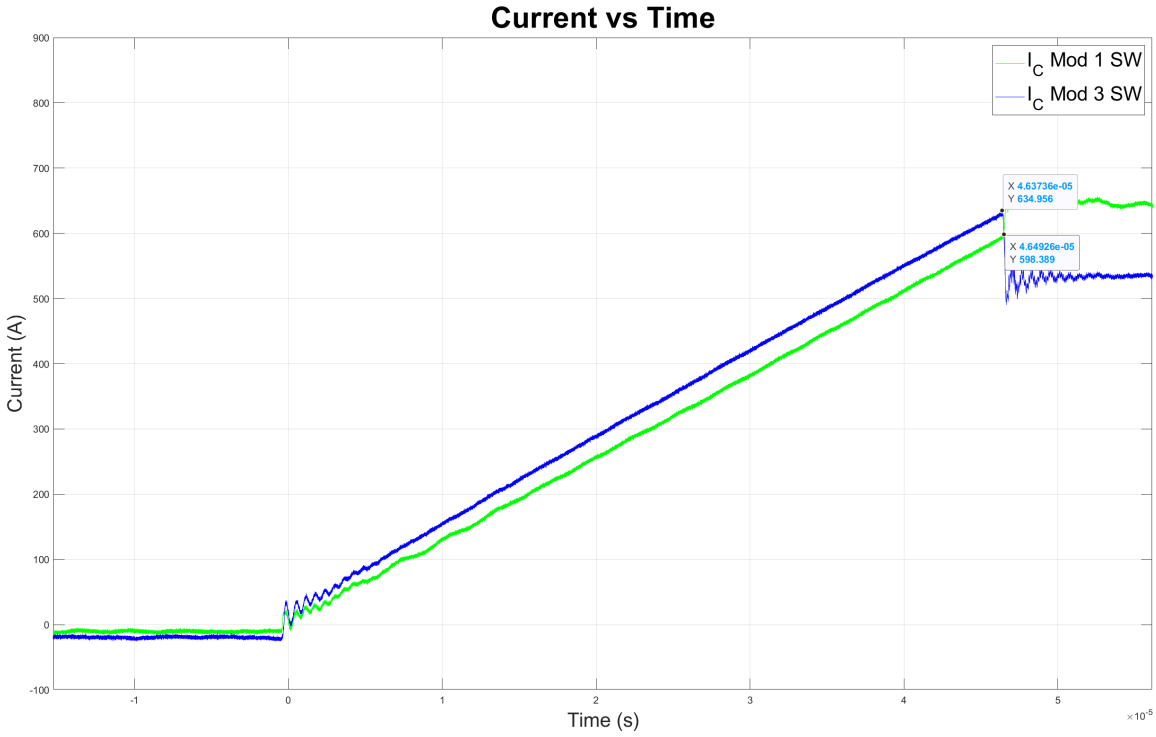


Figure 7.9: Current Rise Two Modules

The comparison of current sharing is already done in table 4.1 and showing low deviations in values of the model and measurements making the model a good reference for further computations.

However, it is necessary to ensure that the exercise yielded absolute results for current sharing. The ideal current is taken as the sum of two peak currents shared by the power modules and divided by 2.

- **Module 1 current -** 608.37A at 47 μsec
- **Module 2 current -** 658.20A at 47 μsec
- **Ideal current value -** 633.29A at 47 μsec and $di/dt = 13.5A/\mu sec$

The below table shares the details of current imbalance of module 1 and module 3,

Table 7.8: Comparison: Module 1 and Module 3 currents

Parameter	**Measurement Results**	**Deviations (%)**
di/dt (Module 1)	12.9 A/ μsec	$\frac{12.9 - 13.5}{13.5} \times 100 = -4.1\%$ (7.1)
di/dt (Module 3)	14.0 A/ μsec	$\frac{14.0 - 13.5}{13.5} \times 100 = 3.7\%$ (7.2)
Max. Current Module 1 @47us	608.37 A	$\frac{608.37 - 633.29}{633.29} \times 100 = -3.9\%$ (7.3)
Max. Current Module 3 @47us	658.20 A	$\frac{658.2 - 633.29}{633.29} \times 100 = 3.9\%$ (7.4)

As concluded from the table above, all the values are below 5% tolerance, the ramp up current is successfully matched. Further analysis on the current jumps and free-wheeling current sharing shall be a part of the future scope of the project.

Chapter 8 Discussion

In this chapter, the impact of limitations and assumptions mentioned in chapter 1 are discussed which may have lead to some inaccuracies in the the results. Some the persistant deviations in the project outcomes might be explained if the components are taken as non-ideal.

8.0.1 Limitations of the DPT Setup

In this section, the limitations of the measurement and setup are discussed and their influence on the results are commented.

Voltage Measurement

Due to the limited CMRR of differential voltage probes HVD3206A-6M, the gate-source signals measurements might not be very accurate. The Micsig MOIP350P with a bandwidth of 350 MHz and a CMRR of 180 dB is yet to arrive. This will ensure higher resolution and accuracy of measurements.

Busbars

The busbars particularly for the switch-node (old busbar) were developed to support interleaving operation for three-phase operation of Si-IGBT modules. To cater the ferrite material, the busbars from the switch-node to the inductor were inevitably longer, offering higher impedances. Also, the point of connection of the inductor cable was not optimal as it caused an imbalance of impedance due to its positioning.

As seen from the results of the old busbars in chapter 7, it became pertinent to replace the busbar overcoming those limitations. Since the replaced busbar was an improvement and solved a lot of problems accustomed with the previous one, due to not fully analyzing it, the busbar shortcomings had to be taken care by specialized cable mounting. Although, it solved the purpose for the project scope, however, this solution is not possible to be standardized as well as might not be repeatable as the positioning is arbitrary. To provide a more sustainable solution, the influence of the cable should be negligible on the module current sharing performance and a more standard connection point like a busbar connection must be provided so that it is scalable and more reliable.

Capacitative Coupling during switching event

The self and mutual inductance caused by the current flow in the switch-node busbar modeling was considered, which helped with the improving the current sharing during ramp up phase highly. However, the capacitative coupling with MOSFET's internal capacitances and the gate driver capacitances have an impact on the turn on and turn off timing. If investigated, it might be a reason for the reverse conduction in one of turned off module while the other module is turning off.

Method of balancing impedances

Since the method of balancing the impedances was using cable was not a standard procedure, it took manual hit-and-trial to reach a close value of impedances in the circuit. This is an inefficient approach as it is time-consuming and might not guarantee success. However, this process can be automated which provides an efficient solution to the problem. This method is further discussed in the chapter 10.

8.0.2 Assumptions

Initially it was assumed that the SiC MOSFET modules are ideal, it is seen from the test results that the behavior has deviations from ideality which are not explained in the project scope. The jumps in the gate voltages observed with increasing current and voltage values demonstrates the need to in-detail investigation of the module towards its maturity and making it production feasible. This switching behavior can instigate de-saturation and might eventually damage the module upon repeated occurance.

For the gate driver, the signal propagates from the Master Gate driver to the Slave Driver, initially the propogation delay is not considered for the project scope, however, this propagation delay in the daisy chain structure might lead to uneven switching events of the modules. This will lead to imbalance in currents and overstressing of one module.

DC-Link voltage is considered to be stable, however, with the change in dynamic voltage due to lower capacitances, it is possible to have a dip in voltage due to highly inductive loads. As a result, the ramp up waveform may not be similar to the simulated values.

8.0.3 SPICE Simultions

The intention was to conduct a SPICE simulation of the setup, however, due to lack of available models of the MOSFET module, the observed behavior after the replacement of new busbar could not be analysed in detail. From the available Z-matrix a model can be formed for the impedances of the busbars, DC-link capacitors and Load inductors are known values and could be directly fed to the model. This would enable better clarity on the observed waveform behavior, like current jumps and free-wheeling current imbalances.

Chapter 9 Conclusion

The project is set out to answer the following problem statement:

"Does paralleling of SiC MOSFET modules (upto 3) for +1 MW electrolyzer application ensure equal current sharing operation?"

To solve the above mentioned problem, Double Pulse Testing (DPT) is conducted on the module and observed phenomenon are analysed. As the SiC technology is still under development, it is pertinent to see current imbalances and other switching issues with the device which are non-existant in the Si-IGBTs due to lower rise and fall times, varied reverse conduction characteristics and die structures.

The main objective of performing DPT was to identify, segregate and individually target the problems in the module current sharing. There are three phases identified, namely, the ramp up, current jumps at MOSFET switchover and the free-wheeling phases. The project direction propagated towards developing a solution for the ramp up current balance. Different segments of the setup are tested for weighting their influence and the switch-node busbar is modified for solving the purpose. From the results of the modeling and testing are well aligned and shows that during the ramp up the current deviation came down to 3.9% for both the power modules 1 and 3, which is within tolerance limits.

Further investigations will focus on understanding the turn-on/off characteristics, internal capacitances, and gate driver circuits of the power modules for a potential solution of the other two phases. With proper procedure, this solution can become scalable and help accelerate the adoption of SiC technology as a potential solution for PtX applications.

Chapter 10 Future Work

This chapter discusses the further developments on the project and its prospective merits.

10.0.1 Impedance matching - Automated

For an efficient solution towards matching the impedances of switch-node busbar, a MATLAB script can be developed integrated with the Fast Henry model. This will ensure MATLAB to iterate the impedance matrix with updated position, shape and size of the cutout in the busbar to make it more uniform for all three modules. It will make the computation time significantly smaller and the accuracy of results will be higher.

10.0.2 Gate Driver Improvement

As a potential solution, the gate driver timings, switching voltages and currents can be studied and potential modifications can be introduced in collaboration with the manufacturer to obtain a more reliable solution. This solution could potentially be unaffected by the noises and prevent false triggering of the modules. Introduction of a miller clamp circuit in the gate driver would potentially lessen the overshoots observed during turn-on.

Potentially different manufacturers can be considered for a driving the modules, this would make sure that to isolate the source-of-trouble segment and provide a better solution.

10.0.3 SiC MOSFET Module

1. **SPICE Model Development** - A SPICE model of the module can be developed from the tests performed in the laboratory so that it is easier to simulate the behavior and expedite the solution methodology. Although, internal capacitances, inductances and resistances are needed to be measured for the model development, which would require higher resolution probes.

2. **Different Manufacturers** - For the Power-to-X segment, the required voltage currently acceptable is 2.3 kV, however, not many manufacturers are producing WBG solutions in this segment. With more manufacturers coming in, a more durable solution with lesser intra-module imbalances could be potentially formed.

10.0.4 Continuous conduction on Load

Instead of performing only a Double Pulse Test (DPT), conducting a full load test would be more beneficial. This approach will enable comprehensive data collection for characterizing both switching and conduction losses. Additionally, it will provide valuable insights into the module's impedance behavior in relation to current and temperature during continuous conduction. Such detailed analysis will lead to more pragmatic and effective solution development in the future.

Bibliography

[1] International Energy Agency, *Denmark - countries & regions*, Accessed: 2024-11-28, 2023. [Online]. Available: https://www.iea.org/countries/denmark.

[2] Danish Energy Agency, *Energy statistics 2023*, Accessed: 2024-11-28, 2023. [Online]. Available: https://ens.dk/sites/ens.dk/files/Statistik/energistatistik_2023.pdf.

[3] International Energy Agency, *Denmark - countries & regions - iea*, Accessed: 2024-12-02, 2023. [Online]. Available: https://www.iea.org/countries/denmark/energy-mix.

[4] Rocky Mountain Institute, "Hydrogen needs to replace fossil fuels in industrial applications to meet climate goals," 2020, Accessed: 2024-12-02. [Online]. Available: https://www.spglobal.com/commodityinsights/en/market-insights/latest-news/electric-power/013020-hydrogen-needs-to-replace-fossil-fuels-in-industrial-applications-to-meet-climate-goals.

[5] International Energy Agency, *Batteries and hydrogen technology: Keys for a clean energy future*, Accessed: 2024-11-28, 2024. [Online]. Available: https://www.iea.org/articles/batteries-and-hydrogen-technology-keys-for-a-clean-energy-future.

[6] M. M. Aba, I. L. Sauer, and N. B. Amado, "Comparative review of hydrogen and electricity as energy carriers for the energy transition," *International Journal of Hydrogen Energy*, vol. 57, pp. 660–678, 2024, ISSN: 0360-3199. DOI: https://doi.org/10.1016/j.ijhydene.2024.01.034. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0360319924000363.

[7] S. C. Ramli, "Why green hydrogen could play a major role in powering our sustainable future," *World Economic Forum*, 2023. [Online]. Available: https://www.weforum.org/stories/2023/12/why-hydrogen-is-the-fuel-of-the-sustainable-future/.

[8] U. Y. Qazi, "Future of hydrogen as an alternative fuel for next-generation industrial applications; challenges and expected opportunities," *Energies*, vol. 15, no. 13, p. 4741, 2022. DOI: 10.3390/en15134741. [Online]. Available: https://www.mdpi.com/1996-1073/15/13/4741.

[9] M. Rasul, M. Hazrat, M. Sattar, M. Jahirul, and M. Shearer, "The future of hydrogen: Challenges on production, storage and applications," *Energy Conversion and Management*, vol. 272, p. 116 326, 2022, ISSN: 0196-8904. DOI: 10.1016/j.enconman.2022.116326. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0196890422011049.

[10] D. F. Matus Muron Grzegorz Pawelec, "Clean hydrogen production pathways," Hydrogen Europe, 2024, Accessed: 2024-12-04. [Online]. Available: https://hydrogeneurope.eu/wp-content/uploads/2024/06/2024_H2E_CleanH2ProductionPathwaysReport.pdf.

[11] A. Hassan, O. Abdel-Rahim, M. Bajaj, and I. Zaitsev, "Power electronics for green hydrogen generation with focus on methods, topologies, and comparative analysis," *Scientific Reports*, vol. 14, no. 1, pp. 1–37, 2024. DOI: 10.1038/s41598-024-76191-6. [Online]. Available: https://www.nature.com/articles/s41598-024-76191-6.

[12] I. Technologies, "The importance of power conversion technologies in the production of green hydrogen," *Infineon Whitepaper*, May 2024, Accessed: 2024-12-04. [Online]. Available: https://www.infineon.com/dgdl/Infineon-The_importance_of_power_conversion_technologies_in_the_production_of_green_hydrogen-Whitepaper-v01_00-EN.pdf?fileId=8ac78c8c8eeb092c018f383f2d1630d5&da=t.

[13] "Iea-trucks." (2013), [Online]. Available: https://ocw.mit.edu/courses/res-tll-004-stem-concept-videos-fall-2013/resources/problem-solving-process/ (visited on 11/27/2023).

[14] M. Chen, S.-F. Chou, F. Blaabjerg, and P. Davari, "Overview of power electronic converter topologies enabling large-scale hydrogen production via water electrolysis," *Applied Sciences*, vol. 12, no. 4, 2022, ISSN: 2076-3417. DOI: 10.3390/app12041906. [Online]. Available: https://www.mdpi.com/2076-3417/12/4/1906.

[15] F. Pellitteri, N. Campagna, R. Inguanta, and R. Miceli, "Application of a multiphase interleaved dc-dc converter for power-to-hydrogen systems," in *2023 IEEE 17th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, 2023, pp. 1–6. DOI: 10.1109/CPE-POWERENG58103.2023.10227382.

[16] T. D. E. Agency, "The first ptx tender in denmark has been determined: Six projects will establish electrolysis capacity on more than 280 mw," Danish Energy Agency, Tech. Rep., 2023. [Online]. Available: https://ens.dk/en/press/first-ptx-tender-denmark-has-been-determined-six-projects-will-establish-electrolysis-capacity.

[17] A. Durakovic. "Denmark accelerates power-to-x push with dkk 1.25 billion subsidy scheme." (2022), [Online]. Available: https://www.offshorewind.biz/2022/03/15/denmark-accelerates-power-to-x-push-with-dkk-1-25-billion-subsidy-scheme/.

[18] S. of Green, *Green experience together*. [Online]. Available: https://live.stateofgreen.com/green-together/#/denmark/2309.

[19] S. of Green, "New strategy accelerates denmark's power-to-x ambitions," State of Green, Tech. Rep., 2022. [Online]. Available: https://stateofgreen.com/en/news/new-strategy-kick-starts-denmark-production-of-green-hydrogen-and-e-fuels/.

[20] A. Sherrard, "Danish government secures major power-to-x investment from the netherlands," Bioenergy International, Tech. Rep., 2020. [Online]. Available: https://bioenergyinternational.com/danish-government-secures-major-power-to-x-investment-from-the-netherlands/.

[21] K. W. S. A/S, *Power-to-x*. [Online]. Available: https://www.kkwindsolutions.com/industries/power-to-x.

[22] C. D. Fuentes, M. Müller, S. Bernet, and S. Kouro, "Sic-mosfet or si-igbt: Comparison of design and key characteristics of a 690 v grid-tied industrial two-level voltage source converter," *Energies*, vol. 14, no. 11, 2021, ISSN: 1996-1073. DOI: 10.3390/en14113054. [Online]. Available: https://www.mdpi.com/1996-1073/14/11/3054.

[23] L. Zhang, X. Yuan, X. Wu, C. Shi, J. Zhang, and Y. Zhang, "Performance evaluation of high-power sic mosfet modules in comparison to si igbt modules," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1181–1196, 2019. DOI: 10.1109/TPEL.2018.2834345.

[24] C. Ionita, M. Nawaz, K. Ilves, and F. Iannuzzo, "Comparative assessment of 3.3kv/400a sic mosfet and si igbt power modules," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 1343–1349. DOI: 10.1109/ECCE.2017.8095946.

[25] M. R. Nielsen, S. Deng, A. B. Mirza, *et al.*, "High-power electronic applications enabled by medium voltage silicon-carbide technology: An overview," *IEEE Transactions on Power Electronics*, pp. 1–26, 2024. DOI: 10.1109/TPEL.2024.3442483.

[26] Y. Hu and J. Shao, "Parallel operation of sic mosfets," in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1–5.

[27] I. Technologies, "Double pulse testing: The how, what and why," *Infineon Technologies White Paper*, 2023. [Online]. Available: https://www.infineon.com/double-pulse-testing.

[28] N. Foerster, D. Urbaneck, B. Kohlhepp, D. Kuebrich, O. Wallscheid, and F. Schafmeister, "Pitfalls and their avoidability in the double-pulse test," in *PCIM Europe 2024; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2024, pp. 3232–3241. DOI: 10.30420/566262457.

Appendix A FASTHENRY Functions

A.1 For Three modules - Braided busbar to Switch-node busbar

```
* FastHenry input file created using FreeCAD's ElectroMagnetic Workbench
* See http://www.freecad.org, http://www.fastfieldsolvers.com and ...
    http://epc-co.com

.units mm

.default sigma=58000.0 nhinc=1 nwinc=1 rh=2 rw=2

* Nodes
NFHNode-BN01 x=36.5 y=85.3 z=0.0
NFHNode-BN02 x=59.5 y=85.3 z=0.0
NFHNode-BN00 x=13.5 y=85.3 z=0.0
NFHNode-MN00 x=126.5 y=85.3 z=0.0
NFHNode-MN01 x=149.5 y=85.3 z=0.0
NFHNode-MN02 x=172.5 y=85.3 z=0.0
NFHNode-TN00 x=239.5 y=85.3 z=0.0
NFHNode-TN01 x=262.5 y=85.3 z=0.0
NFHNode-TN02 x=285.5 y=85.3 z=0.0
NFHNode-BN10 x=13.5 y=85.3 z=10.0
NFHNode-BN11 x=36.5 y=85.3 z=10.0
NFHNode-BN12 x=59.5 y=85.3 z=10.0
NFHNode-BRBN00 x=13.5 y=224.8 z=10.0
NFHNode-BRBN01 x=36.5 y=224.8 z=10.0
NFHNode-BRBN02 x=59.5 y=224.8 z=10.0
NFHNode-MN10 x=126.5 y=85.3 z=10.0
NFHNode-MN11 x=149.5 y=85.3 z=10.0
NFHNode-MN12 x=172.5 y=85.3 z=10.0
NFHNode_BRMN02 x=172.5 y=224.8 z=10.0
NFHNode-BRMN01 x=149.5 y=224.8 z=10.0
NFHNode-BRMN00 x=126.5 y=224.8 z=10.0
NFHNode-BRTN02 x=285.5 y=224.8 z=10.0
NFHNode-BRTN01 x=262.5 y=224.8 z=10.0
NFHNode-BRTN00 x=239.5 y=224.8 z=10.0
NFHNode-TN12 x=285.5 y=85.3 z=10.0
NFHNode-TN11 x=262.5 y=85.3 z=10.0
NFHNode-TN10 x=239.5 y=85.3 z=10.0
NFHNode-InductorExitNode x=136.5 y=17.0 z=0.0

* Planes
GFHPlane x1=0.0 y1=0.0 z1=5.0 x2=299.0 y2=0.0 z2=5.0
+         x3=299.0 y3=120.0 z3=5.0
+         thick=10.0 seg1=20 seg2=20
+         NFHNode-MN00p (126.5,85.3,0.0)
+         NFHNode-MN02p (172.5,85.3,0.0)
+         NFHNode-MN01p (149.5,85.3,0.0)
+         NFHNode-TN00p (239.5,85.3,0.0)
+         NFHNode-TN01p (262.5,85.3,0.0)
+         NFHNode-TN02p (285.5,85.3,0.0)
+         NFHNode-BN01p (36.5,85.3,0.0)
+         NFHNode-BN02p (59.5,85.3,0.0)
+         NFHNode-BN00p (13.5,85.3,0.0)
+         NFHNode-InductorExitNodep (136.5,17.0,0.0)
+         hole rect (109.5,61.0,0.0,189.5,65.0,0.0)

```

```
+         hole circle (93.0,35.0,0.0,3.5)
+         hole circle (206.0,35.0,0.0,3.5)
+         hole circle (93.0,83.0,0.0,3.5)
+         hole circle (206.0,83.0,0.0,3.5)

+         hole circle (162.5,37.5,0.0,6.75)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-MN00 NFHNode-MN00p
.equiv NFHNode-MN02 NFHNode-MN02p
.equiv NFHNode-MN01 NFHNode-MN01p
.equiv NFHNode-TN00 NFHNode-TN00p
.equiv NFHNode-TN01 NFHNode-TN01p
.equiv NFHNode-TN02 NFHNode-TN02p
.equiv NFHNode-BN01 NFHNode-BN01p
.equiv NFHNode-BN02 NFHNode-BN02p
.equiv NFHNode-BN00 NFHNode-BN00p
.equiv NFHNode-InductorExitNode NFHNode-InductorExitNodep

GFHPlane001 x1=0.0 y1=66.3 z1=13.0 x2=73.0 y2=66.3 z2=13.0
+         x3=73.0 y3=237.3 z3=13.0
+         thick=6.0 seg1=10 seg2=10
+         NFHNode-BN10p (13.5,85.3,10.0)
+         NFHNode-BN11p (36.5,85.3,10.0)
+         NFHNode-BN12p (59.5,85.3,10.0)
+         NFHNode-BRBN00p (13.5,224.8,10.0)
+         NFHNode-BRBN01p (36.5,224.8,10.0)
+         NFHNode-BRBN02p (59.5,224.8,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-BN10 NFHNode-BN10p
.equiv NFHNode-BN11 NFHNode-BN11p
.equiv NFHNode-BN12 NFHNode-BN12p
.equiv NFHNode-BRBN00 NFHNode-BRBN00p
.equiv NFHNode-BRBN01 NFHNode-BRBN01p
.equiv NFHNode-BRBN02 NFHNode-BRBN02p

GFHPlane002 x1=113.0 y1=66.3 z1=13.0 x2=186.0 y2=66.3 z2=13.0
+         x3=186.0 y3=237.3 z3=13.0
+         thick=6.0 seg1=10 seg2=10
+         NFHNode-MN10p (126.5,85.3,10.0)
+         NFHNode-MN11p (149.5,85.3,10.0)
+         NFHNode-MN12p (172.5,85.3,10.0)
+         NFHNode-BRMN01p (149.5,224.8,10.0)
+         NFHNode-BRMN00p (126.5,224.8,10.0)
+         NFHNode_BRMN02p (172.5,224.8,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-MN10 NFHNode-MN10p
.equiv NFHNode-MN11 NFHNode-MN11p
.equiv NFHNode-MN12 NFHNode-MN12p
.equiv NFHNode-BRMN01 NFHNode-BRMN01p
.equiv NFHNode-BRMN00 NFHNode-BRMN00p
.equiv NFHNode_BRMN02 NFHNode_BRMN02p

GFHPlane003 x1=226.0 y1=66.3 z1=13.0 x2=299.0 y2=66.3 z2=13.0
+         x3=299.0 y3=237.3 z3=13.0
+         thick=6.0 seg1=10 seg2=10
```

```
+          NFHNode-BRTN02p (285.5,224.8,10.0)
+          NFHNode-BRTN01p (262.5,224.8,10.0)
+          NFHNode-BRTN00p (239.5,224.8,10.0)
+          NFHNode-TN12p (285.5,85.3,10.0)
+          NFHNode-TN11p (262.5,85.3,10.0)
+          NFHNode-TN10p (239.5,85.3,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-BRTN02 NFHNode-BRTN02p
.equiv NFHNode-BRTN01 NFHNode-BRTN01p
.equiv NFHNode-BRTN00 NFHNode-BRTN00p
.equiv NFHNode-TN12 NFHNode-TN12p
.equiv NFHNode-TN11 NFHNode-TN11p
.equiv NFHNode-TN10 NFHNode-TN10p


* Node shorts
.equiv NFHNode-BN10 NFHNode-BN00
.equiv NFHNode-BN11 NFHNode-BN01
.equiv NFHNode-BN12 NFHNode-BN02
.equiv NFHNode-BRBN00 NFHNode-BRBN01
.equiv NFHNode-BRBN01 NFHNode-BRBN02
.equiv NFHNode-MN00 NFHNode-MN10
.equiv NFHNode-MN11 NFHNode-MN01
.equiv NFHNode-MN02 NFHNode-MN12
.equiv NFHNode_BRMN02 NFHNode-BRMN00
.equiv NFHNode-BRMN00 NFHNode-BRMN01
.equiv NFHNode-BRTN02 NFHNode-BRTN01
.equiv NFHNode-BRTN01 NFHNode-BRTN00
.equiv NFHNode-TN10 NFHNode-TN00
.equiv NFHNode-TN01 NFHNode-TN11
.equiv NFHNode-TN12 NFHNode-TN02

* Ports
.external NFHNode-InductorExitNode NFHNode-BRBN01
.external NFHNode-InductorExitNode NFHNode-BRMN01
.external NFHNode-InductorExitNode NFHNode-BRTN01

.freq fmin=1.0 fmax=100000.0 ndec=1.0

.end
```

A.2 For Two modules - Braided busbar to Cable End

```
    * FastHenry input file created using FreeCAD's ElectroMagnetic Workbench
* See http://www.freecad.org, http://www.fastfieldsolvers.com and ...
    http://epc-co.com

.units mm

.default sigma=58000.0 nhinc=1 nwinc=1 rh=2 rw=2

* Nodes
NFHNode-BN01 x=36.5 y=85.3 z=0.0
NFHNode-BN02 x=59.5 y=85.3 z=0.0
NFHNode-BN00 x=13.5 y=85.3 z=0.0
```

```
12 NFHNode-MN00 x=126.5 y=85.3 z=0.0
13 NFHNode-MN01 x=149.5 y=85.3 z=0.0
14 NFHNode-MN02 x=172.5 y=85.3 z=0.0
15 NFHNode-TN00 x=239.5 y=85.3 z=0.0
16 NFHNode-TN01 x=262.5 y=85.3 z=0.0
17 NFHNode-TN02 x=285.5 y=85.3 z=0.0
18 NFHNode-BN10 x=13.5 y=85.3 z=10.0
19 NFHNode-BN11 x=36.5 y=85.3 z=10.0
20 NFHNode-BN12 x=59.5 y=85.3 z=10.0
21 NFHNode-BRBN00 x=13.5 y=224.8 z=10.0
22 NFHNode-BRBN01 x=36.5 y=224.8 z=10.0
23 NFHNode-BRBN02 x=59.5 y=224.8 z=10.0
24 NFHNode-MN10 x=126.5 y=85.3 z=10.0
25 NFHNode-MN11 x=149.5 y=85.3 z=10.0
26 NFHNode-MN12 x=172.5 y=85.3 z=10.0
27 NFHNode_BRMN02 x=172.5 y=224.8 z=10.0
28 NFHNode-BRMN01 x=149.5 y=224.8 z=10.0
29 NFHNode-BRMN00 x=126.5 y=224.8 z=10.0
30 NFHNode-BRTN02 x=285.5 y=224.8 z=10.0
31 NFHNode-BRTN01 x=262.5 y=224.8 z=10.0
32 NFHNode-BRTN00 x=239.5 y=224.8 z=10.0
33 NFHNode-TN12 x=285.5 y=85.3 z=10.0
34 NFHNode-TN11 x=262.5 y=85.3 z=10.0
35 NFHNode-TN10 x=239.5 y=85.3 z=10.0
36 NFHNode-InductorExitNode x=136.5 y=17.0 z=0.0
37
38 * Planes
39 GFHPlane x1=0.0 y1=0.0 z1=0.0 x2=299.0 y2=0.0 z2=0.0
40 +         x3=299.0 y3=120.0 z3=0.0
41 +         thick=10.0 seg1=30 seg2=30
42 +         NFHNode-MN00p (126.5,85.3,0.0)
43 +         NFHNode-MN02p (172.5,85.3,0.0)
44 +         NFHNode-MN01p (149.5,85.3,0.0)
45 +         NFHNode-TN00p (239.5,85.3,0.0)
46 +         NFHNode-TN01p (262.5,85.3,0.0)
47 +         NFHNode-TN02p (285.5,85.3,0.0)
48 +         NFHNode-BN01p (36.5,85.3,0.0)
49 +         NFHNode-BN02p (59.5,85.3,0.0)
50 +         NFHNode-BN00p (13.5,85.3,0.0)
51 +         NFHNode-InductorExitNodep (136.5,17.0,0.0)
52 +         hole rect (109.5,61.0,0.0,189.5,65.0,0.0)
53
54 +         hole circle (93.0,35.0,0.0,3.5)
55 +         hole circle (206.0,35.0,0.0,3.5)
56 +         hole circle (93.0,83.0,0.0,3.5)
57 +         hole circle (206.0,83.0,0.0,3.5)
58 +         hole circle (162.5,37.5,0.0,6.75)
59
60 * Connecting internal plane nodes to actual nodes
61 .equiv NFHNode-MN00 NFHNode-MN00p
62 .equiv NFHNode-MN02 NFHNode-MN02p
63 .equiv NFHNode-MN01 NFHNode-MN01p
64 .equiv NFHNode-TN00 NFHNode-TN00p
65 .equiv NFHNode-TN01 NFHNode-TN01p
66 .equiv NFHNode-TN02 NFHNode-TN02p
67 .equiv NFHNode-BN01 NFHNode-BN01p
68 .equiv NFHNode-BN02 NFHNode-BN02p
69 .equiv NFHNode-BN00 NFHNode-BN00p
```

```
.equiv NFHNode-InductorExitNode NFHNode-InductorExitNodep

GFHPlane001 x1=0.0 y1=70 z1=10.0 x2=73.0 y2=70 z2=10.0
+         x3=73.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-BN10p (13.5,85.3,10.0)
+         NFHNode-BN11p (36.5,85.3,10.0)
+         NFHNode-BN12p (59.5,85.3,10.0)
+         NFHNode-BRBN00p (13.5,224.8,10.0)
+         NFHNode-BRBN01p (36.5,224.8,10.0)
+         NFHNode-BRBN02p (59.5,224.8,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-BN10 NFHNode-BN10p
.equiv NFHNode-BN11 NFHNode-BN11p
.equiv NFHNode-BN12 NFHNode-BN12p
.equiv NFHNode-BRBN00 NFHNode-BRBN00p
.equiv NFHNode-BRBN01 NFHNode-BRBN01p
.equiv NFHNode-BRBN02 NFHNode-BRBN02p

GFHPlane002 x1=113.0 y1=70 z1=10.0 x2=186.0 y2=70 z2=10.0
+         x3=186.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-MN10p (126.5,85.3,10.0)
+         NFHNode-MN11p (149.5,85.3,10.0)
+         NFHNode-MN12p (172.5,85.3,10.0)
+         NFHNode-BRMN01p (149.5,224.8,10.0)
+         NFHNode-BRMN00p (126.5,224.8,10.0)
+         NFHNode_BRMN02p (172.5,224.8,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-MN10 NFHNode-MN10p
.equiv NFHNode-MN11 NFHNode-MN11p
.equiv NFHNode-MN12 NFHNode-MN12p
.equiv NFHNode-BRMN01 NFHNode-BRMN01p
.equiv NFHNode-BRMN00 NFHNode-BRMN00p
.equiv NFHNode_BRMN02 NFHNode_BRMN02p

GFHPlane003 x1=226.0 y1=70 z1=10.0 x2=299.0 y2=70 z2=10.0
+         x3=299.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-BRTN02p (285.5,224.8,10.0)
+         NFHNode-BRTN01p (262.5,224.8,10.0)
+         NFHNode-BRTN00p (239.5,224.8,10.0)
+         NFHNode-TN12p (285.5,85.3,10.0)
+         NFHNode-TN11p (262.5,85.3,10.0)
+         NFHNode-TN10p (239.5,85.3,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-BRTN02 NFHNode-BRTN02p
.equiv NFHNode-BRTN01 NFHNode-BRTN01p
.equiv NFHNode-BRTN00 NFHNode-BRTN00p
.equiv NFHNode-TN12 NFHNode-TN12p
.equiv NFHNode-TN11 NFHNode-TN11p
.equiv NFHNode-TN10 NFHNode-TN10p


* Nodes Angle kept -5 degrees Distance - 220mm from connection point
```

```
128 NFHNode x=197.80  y=-194.29 z=0.0
129 NFHNode001 x=136.5 y=17.0 z=0.0
130 NFHNode002 x=299.0 y=-194.29 z=0.0
131 NFHNode003 x=197.80  y=-194.29 z=0.0
132
133 * Segments from paths
134 EFHPath0 NFHNode001 NFHNode w=16.0 h=15.0 sigma=58000.0 nhinc=5 nwinc=5 ...
        rh=5 rw=5
135 EFHPath0010 NFHNode003 NFHNode002 w=16.0 h=15.0 sigma=58000.0 nhinc=5 ...
        nwinc=5 rh=5 rw=5
136
137 .equiv NFHNode-InductorExitNode NFHNode001
138 .equiv NFHNode NFHNode003
139
140
141 * Node shorts
142 .equiv NFHNode-BN10 NFHNode-BN00
143 .equiv NFHNode-BN11 NFHNode-BN01
144 .equiv NFHNode-BN12 NFHNode-BN02
145 .equiv NFHNode-BRBN00 NFHNode-BRBN01
146 .equiv NFHNode-BRBN01 NFHNode-BRBN02
147 .equiv NFHNode-MN00 NFHNode-MN10
148 .equiv NFHNode-MN11 NFHNode-MN01
149 .equiv NFHNode-MN02 NFHNode-MN12
150 .equiv NFHNode_BRMN02 NFHNode-BRMN00
151 .equiv NFHNode-BRMN00 NFHNode-BRMN01
152 .equiv NFHNode-BRTN02 NFHNode-BRTN01
153 .equiv NFHNode-BRTN01 NFHNode-BRTN00
154 .equiv NFHNode-TN10 NFHNode-TN00
155 .equiv NFHNode-TN01 NFHNode-TN11
156 .equiv NFHNode-TN12 NFHNode-TN02
157
158 * Ports
159 *.external NFHNode002 NFHNode-BRBN01
160 .external NFHNode002 NFHNode-BRMN01
161 .external NFHNode002 NFHNode-BRTN01
162
163 .freq fmin=1.0 fmax=100000.0 ndec=1.0
164
165 .end
```

A.3 Sensitivity Analysis

A.3.1 Moving the Cutout

1. **Upwards**

```
1      * FastHenry input file created using FreeCAD's ElectroMagnetic ...
           Workbench
2  * See http://www.freecad.org, http://www.fastfieldsolvers.com and ...
       http://epc-co.com
3
4  .units mm
5
6  .default sigma=58000.0 nhinc=1 nwinc=1 rh=2 rw=2
7
8  * Nodes
```

```
NFHNode-BN01 x=36.5 y=85.3 z=0.0
NFHNode-BN02 x=59.5 y=85.3 z=0.0
NFHNode-BN00 x=13.5 y=85.3 z=0.0
NFHNode-MN00 x=126.5 y=85.3 z=0.0
NFHNode-MN01 x=149.5 y=85.3 z=0.0
NFHNode-MN02 x=172.5 y=85.3 z=0.0
NFHNode-TN00 x=239.5 y=85.3 z=0.0
NFHNode-TN01 x=262.5 y=85.3 z=0.0
NFHNode-TN02 x=285.5 y=85.3 z=0.0
NFHNode-BN10 x=13.5 y=85.3 z=10.0
NFHNode-BN11 x=36.5 y=85.3 z=10.0
NFHNode-BN12 x=59.5 y=85.3 z=10.0
NFHNode-BRBN00 x=13.5 y=224.8 z=10.0
NFHNode-BRBN01 x=36.5 y=224.8 z=10.0
NFHNode-BRBN02 x=59.5 y=224.8 z=10.0
NFHNode-MN10 x=126.5 y=85.3 z=10.0
NFHNode-MN11 x=149.5 y=85.3 z=10.0
NFHNode-MN12 x=172.5 y=85.3 z=10.0
NFHNode_BRMN02 x=172.5 y=224.8 z=10.0
NFHNode-BRMN01 x=149.5 y=224.8 z=10.0
NFHNode-BRMN00 x=126.5 y=224.8 z=10.0
NFHNode-BRTN02 x=285.5 y=224.8 z=10.0
NFHNode-BRTN01 x=262.5 y=224.8 z=10.0
NFHNode-BRTN00 x=239.5 y=224.8 z=10.0
NFHNode-TN12 x=285.5 y=85.3 z=10.0
NFHNode-TN11 x=262.5 y=85.3 z=10.0
NFHNode-TN10 x=239.5 y=85.3 z=10.0
NFHNode-InductorExitNode x=136.5 y=17.0 z=0.0

* Planes
GFHPlane x1=0.0 y1=0.0 z1=0.0 x2=299.0 y2=0.0 z2=0.0
+         x3=299.0 y3=120.0 z3=0.0
+         thick=10.0 seg1=30 seg2=30
+         NFHNode-MN00p (126.5,85.3,0.0)
+         NFHNode-MN02p (172.5,85.3,0.0)
+         NFHNode-MN01p (149.5,85.3,0.0)
+         NFHNode-TN00p (239.5,85.3,0.0)
+         NFHNode-TN01p (262.5,85.3,0.0)
+         NFHNode-TN02p (285.5,85.3,0.0)
+         NFHNode-BN01p (36.5,85.3,0.0)
+         NFHNode-BN02p (59.5,85.3,0.0)
+         NFHNode-BN00p (13.5,85.3,0.0)
+         NFHNode-InductorExitNodep (136.5,17.0,0.0)
+         hole rect (117.5,61.0,0.0,197.5,65.0,0.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-MN00 NFHNode-MN00p
.equiv NFHNode-MN02 NFHNode-MN02p
.equiv NFHNode-MN01 NFHNode-MN01p
.equiv NFHNode-TN00 NFHNode-TN00p
.equiv NFHNode-TN01 NFHNode-TN01p
.equiv NFHNode-TN02 NFHNode-TN02p
.equiv NFHNode-BN01 NFHNode-BN01p
.equiv NFHNode-BN02 NFHNode-BN02p
.equiv NFHNode-BN00 NFHNode-BN00p
.equiv NFHNode-InductorExitNode NFHNode-InductorExitNodep

GFHPlane001 x1=0.0 y1=70 z1=10.0 x2=73.0 y2=70 z2=10.0
```

```
+         x3=73.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-BN10p (13.5,85.3,10.0)
+         NFHNode-BN11p (36.5,85.3,10.0)
+         NFHNode-BN12p (59.5,85.3,10.0)
+         NFHNode-BRBN00p (13.5,224.8,10.0)
+         NFHNode-BRBN01p (36.5,224.8,10.0)
+         NFHNode-BRBN02p (59.5,224.8,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-BN10 NFHNode-BN10p
.equiv NFHNode-BN11 NFHNode-BN11p
.equiv NFHNode-BN12 NFHNode-BN12p
.equiv NFHNode-BRBN00 NFHNode-BRBN00p
.equiv NFHNode-BRBN01 NFHNode-BRBN01p
.equiv NFHNode-BRBN02 NFHNode-BRBN02p

GFHPlane002 x1=113.0 y1=70 z1=10.0 x2=186.0 y2=70 z2=10.0
+         x3=186.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-MN10p (126.5,85.3,10.0)
+         NFHNode-MN11p (149.5,85.3,10.0)
+         NFHNode-MN12p (172.5,85.3,10.0)
+         NFHNode-BRMN01p (149.5,224.8,10.0)
+         NFHNode-BRMN00p (126.5,224.8,10.0)
+         NFHNode_BRMN02p (172.5,224.8,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-MN10 NFHNode-MN10p
.equiv NFHNode-MN11 NFHNode-MN11p
.equiv NFHNode-MN12 NFHNode-MN12p
.equiv NFHNode-BRMN01 NFHNode-BRMN01p
.equiv NFHNode-BRMN00 NFHNode-BRMN00p
.equiv NFHNode_BRMN02 NFHNode_BRMN02p

GFHPlane003 x1=226.0 y1=70 z1=10.0 x2=299.0 y2=70 z2=10.0
+         x3=299.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-BRTN02p (285.5,224.8,10.0)
+         NFHNode-BRTN01p (262.5,224.8,10.0)
+         NFHNode-BRTN00p (239.5,224.8,10.0)
+         NFHNode-TN12p (285.5,85.3,10.0)
+         NFHNode-TN11p (262.5,85.3,10.0)
+         NFHNode-TN10p (239.5,85.3,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-BRTN02 NFHNode-BRTN02p
.equiv NFHNode-BRTN01 NFHNode-BRTN01p
.equiv NFHNode-BRTN00 NFHNode-BRTN00p
.equiv NFHNode-TN12 NFHNode-TN12p
.equiv NFHNode-TN11 NFHNode-TN11p
.equiv NFHNode-TN10 NFHNode-TN10p


* Nodes Angle kept -5 degrees Distance - 220mm from connection point
NFHNode x=197.80  y=-194.29 z=0.0
NFHNode001 x=136.5 y=17.0 z=0.0
NFHNode002 x=299.0 y=-194.29 z=0.0
```

```
125 NFHNode003 x=197.80  y=-194.29 z=0.0
126
127 * Segments from paths
128 EFHPath0 NFHNode001 NFHNode w=16.0 h=15.0 sigma=58000.0 nhinc=5 ...
        nwinc=5 rh=5 rw=5
129 EFHPath0010 NFHNode003 NFHNode002 w=16.0 h=15.0 sigma=58000.0 ...
        nhinc=5 nwinc=5 rh=5 rw=5
130
131 .equiv NFHNode-InductorExitNode NFHNode001
132 .equiv NFHNode NFHNode003
133
134
135 * Node shorts
136 .equiv NFHNode-BN10 NFHNode-BN00
137 .equiv NFHNode-BN11 NFHNode-BN01
138 .equiv NFHNode-BN12 NFHNode-BN02
139 .equiv NFHNode-BRBN00 NFHNode-BRBN01
140 .equiv NFHNode-BRBN01 NFHNode-BRBN02
141 .equiv NFHNode-MN00 NFHNode-MN10
142 .equiv NFHNode-MN11 NFHNode-MN01
143 .equiv NFHNode-MN02 NFHNode-MN12
144 .equiv NFHNode_BRMN02 NFHNode-BRMN00
145 .equiv NFHNode-BRMN00 NFHNode-BRMN01
146 .equiv NFHNode-BRTN02 NFHNode-BRTN01
147 .equiv NFHNode-BRTN01 NFHNode-BRTN00
148 .equiv NFHNode-TN10 NFHNode-TN00
149 .equiv NFHNode-TN01 NFHNode-TN11
150 .equiv NFHNode-TN12 NFHNode-TN02
151
152 * Ports
153 *.external NFHNode002 NFHNode-BRBN01
154 .external NFHNode002 NFHNode-BRMN01
155 .external NFHNode002 NFHNode-BRTN01
156
157 .freq fmin=1.0 fmax=100000.0 ndec=1.0
158
159 .end
160
161 .freq fmin=1.0 fmax=100000.0 ndec=1.0
162
163 .end
```

2. **Downwards**

```
1  * FastHenry input file created using FreeCAD's ElectroMagnetic ...
       Workbench
2  * See http://www.freecad.org, http://www.fastfieldsolvers.com and ...
       http://epc-co.com
3
4  .units mm
5
6  .default sigma=58000.0 nhinc=1 nwinc=1 rh=2 rw=2
7
8  * Nodes
9  NFHNode-BN01 x=36.5 y=85.3 z=0.0
10 NFHNode-BN02 x=59.5 y=85.3 z=0.0
11 NFHNode-BN00 x=13.5 y=85.3 z=0.0
```

```
12 NFHNode-MN00 x=126.5 y=85.3 z=0.0
13 NFHNode-MN01 x=149.5 y=85.3 z=0.0
14 NFHNode-MN02 x=172.5 y=85.3 z=0.0
15 NFHNode-TN00 x=239.5 y=85.3 z=0.0
16 NFHNode-TN01 x=262.5 y=85.3 z=0.0
17 NFHNode-TN02 x=285.5 y=85.3 z=0.0
18 NFHNode-BN10 x=13.5 y=85.3 z=10.0
19 NFHNode-BN11 x=36.5 y=85.3 z=10.0
20 NFHNode-BN12 x=59.5 y=85.3 z=10.0
21 NFHNode-BRBN00 x=13.5 y=224.8 z=10.0
22 NFHNode-BRBN01 x=36.5 y=224.8 z=10.0
23 NFHNode-BRBN02 x=59.5 y=224.8 z=10.0
24 NFHNode-MN10 x=126.5 y=85.3 z=10.0
25 NFHNode-MN11 x=149.5 y=85.3 z=10.0
26 NFHNode-MN12 x=172.5 y=85.3 z=10.0
27 NFHNode_BRMN02 x=172.5 y=224.8 z=10.0
28 NFHNode-BRMN01 x=149.5 y=224.8 z=10.0
29 NFHNode-BRMN00 x=126.5 y=224.8 z=10.0
30 NFHNode-BRTN02 x=285.5 y=224.8 z=10.0
31 NFHNode-BRTN01 x=262.5 y=224.8 z=10.0
32 NFHNode-BRTN00 x=239.5 y=224.8 z=10.0
33 NFHNode-TN12 x=285.5 y=85.3 z=10.0
34 NFHNode-TN11 x=262.5 y=85.3 z=10.0
35 NFHNode-TN10 x=239.5 y=85.3 z=10.0
36 NFHNode-InductorExitNode x=136.5 y=17.0 z=0.0
37
38 * Planes
39 GFHPlane x1=0.0 y1=0.0 z1=0.0 x2=299.0 y2=0.0 z2=0.0
40 +         x3=299.0 y3=120.0 z3=0.0
41 +         thick=10.0 seg1=30 seg2=30
42 +         NFHNode-MN00p (126.5,85.3,0.0)
43 +         NFHNode-MN02p (172.5,85.3,0.0)
44 +         NFHNode-MN01p (149.5,85.3,0.0)
45 +         NFHNode-TN00p (239.5,85.3,0.0)
46 +         NFHNode-TN01p (262.5,85.3,0.0)
47 +         NFHNode-TN02p (285.5,85.3,0.0)
48 +         NFHNode-BN01p (36.5,85.3,0.0)
49 +         NFHNode-BN02p (59.5,85.3,0.0)
50 +         NFHNode-BN00p (13.5,85.3,0.0)
51 +         NFHNode-InductorExitNodep (136.5,17.0,0.0)
52 +         hole rect (101.5,61.0,0.0,181.5,65.0,0.0)
53
54 * Connecting internal plane nodes to actual nodes
55 .equiv NFHNode-MN00 NFHNode-MN00p
56 .equiv NFHNode-MN02 NFHNode-MN02p
57 .equiv NFHNode-MN01 NFHNode-MN01p
58 .equiv NFHNode-TN00 NFHNode-TN00p
59 .equiv NFHNode-TN01 NFHNode-TN01p
60 .equiv NFHNode-TN02 NFHNode-TN02p
61 .equiv NFHNode-BN01 NFHNode-BN01p
62 .equiv NFHNode-BN02 NFHNode-BN02p
63 .equiv NFHNode-BN00 NFHNode-BN00p
64 .equiv NFHNode-InductorExitNode NFHNode-InductorExitNodep
65
66 GFHPlane001 x1=0.0 y1=70 z1=10.0 x2=73.0 y2=70 z2=10.0
67 +         x3=73.0 y3=241 z3=10.0
68 +         thick=6.0 seg1=20 seg2=20
69 +         NFHNode-BN10p (13.5,85.3,10.0)
```

```
+         NFHNode-BN11p (36.5,85.3,10.0)
+         NFHNode-BN12p (59.5,85.3,10.0)
+         NFHNode-BRBN00p (13.5,224.8,10.0)
+         NFHNode-BRBN01p (36.5,224.8,10.0)
+         NFHNode-BRBN02p (59.5,224.8,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-BN10 NFHNode-BN10p
.equiv NFHNode-BN11 NFHNode-BN11p
.equiv NFHNode-BN12 NFHNode-BN12p
.equiv NFHNode-BRBN00 NFHNode-BRBN00p
.equiv NFHNode-BRBN01 NFHNode-BRBN01p
.equiv NFHNode-BRBN02 NFHNode-BRBN02p

GFHPlane002 x1=113.0 y1=70 z1=10.0 x2=186.0 y2=70 z2=10.0
+         x3=186.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-MN10p (126.5,85.3,10.0)
+         NFHNode-MN11p (149.5,85.3,10.0)
+         NFHNode-MN12p (172.5,85.3,10.0)
+         NFHNode-BRMN01p (149.5,224.8,10.0)
+         NFHNode-BRMN00p (126.5,224.8,10.0)
+         NFHNode_BRMN02p (172.5,224.8,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-MN10 NFHNode-MN10p
.equiv NFHNode-MN11 NFHNode-MN11p
.equiv NFHNode-MN12 NFHNode-MN12p
.equiv NFHNode-BRMN01 NFHNode-BRMN01p
.equiv NFHNode-BRMN00 NFHNode-BRMN00p
.equiv NFHNode_BRMN02 NFHNode_BRMN02p

GFHPlane003 x1=226.0 y1=70 z1=10.0 x2=299.0 y2=70 z2=10.0
+         x3=299.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-BRTN02p (285.5,224.8,10.0)
+         NFHNode-BRTN01p (262.5,224.8,10.0)
+         NFHNode-BRTN00p (239.5,224.8,10.0)
+         NFHNode-TN12p (285.5,85.3,10.0)
+         NFHNode-TN11p (262.5,85.3,10.0)
+         NFHNode-TN10p (239.5,85.3,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-BRTN02 NFHNode-BRTN02p
.equiv NFHNode-BRTN01 NFHNode-BRTN01p
.equiv NFHNode-BRTN00 NFHNode-BRTN00p
.equiv NFHNode-TN12 NFHNode-TN12p
.equiv NFHNode-TN11 NFHNode-TN11p
.equiv NFHNode-TN10 NFHNode-TN10p


* Nodes Angle kept -5 degrees Distance - 220mm from connection point
NFHNode x=197.80  y=-194.29 z=0.0
NFHNode001 x=136.5 y=17.0 z=0.0
NFHNode002 x=299.0 y=-194.29 z=0.0
NFHNode003 x=197.80  y=-194.29 z=0.0

* Segments from paths
```

```
EFHPath0 NFHNode001 NFHNode w=16.0 h=15.0 sigma=58000.0 nhinc=5 ...
    nwinc=5 rh=5 rw=5
EFHPath0010 NFHNode003 NFHNode002 w=16.0 h=15.0 sigma=58000.0 ...
    nhinc=5 nwinc=5 rh=5 rw=5

.equiv NFHNode-InductorExitNode NFHNode001
.equiv NFHNode NFHNode003


* Node shorts
.equiv NFHNode-BN10 NFHNode-BN00
.equiv NFHNode-BN11 NFHNode-BN01
.equiv NFHNode-BN12 NFHNode-BN02
.equiv NFHNode-BRBN00 NFHNode-BRBN01
.equiv NFHNode-BRBN01 NFHNode-BRBN02
.equiv NFHNode-MN00 NFHNode-MN10
.equiv NFHNode-MN11 NFHNode-MN01
.equiv NFHNode-MN02 NFHNode-MN12
.equiv NFHNode_BRMN02 NFHNode-BRMN00
.equiv NFHNode-BRMN00 NFHNode-BRMN01
.equiv NFHNode-BRTN02 NFHNode-BRTN01
.equiv NFHNode-BRTN01 NFHNode-BRTN00
.equiv NFHNode-TN10 NFHNode-TN00
.equiv NFHNode-TN01 NFHNode-TN11
.equiv NFHNode-TN12 NFHNode-TN02

* Ports
*.external NFHNode002 NFHNode-BRBN01
.external NFHNode002 NFHNode-BRMN01
.external NFHNode002 NFHNode-BRTN01

.freq fmin=1.0 fmax=100000.0 ndec=1.0

.end

.freq fmin=1.0 fmax=100000.0 ndec=1.0

.end
```

3. **Left**

```
* FastHenry input file created using FreeCAD's ElectroMagnetic ...
    Workbench
* See http://www.freecad.org, http://www.fastfieldsolvers.com and ...
    http://epc-co.com

.units mm

.default sigma=58000.0 nhinc=1 nwinc=1 rh=2 rw=2

* Nodes
NFHNode-BN01 x=36.5 y=85.3 z=0.0
NFHNode-BN02 x=59.5 y=85.3 z=0.0
NFHNode-BN00 x=13.5 y=85.3 z=0.0
NFHNode-MN00 x=126.5 y=85.3 z=0.0
NFHNode-MN01 x=149.5 y=85.3 z=0.0
NFHNode-MN02 x=172.5 y=85.3 z=0.0
```

```
NFHNode-TN00 x=239.5 y=85.3 z=0.0
NFHNode-TN01 x=262.5 y=85.3 z=0.0
NFHNode-TN02 x=285.5 y=85.3 z=0.0
NFHNode-BN10 x=13.5 y=85.3 z=10.0
NFHNode-BN11 x=36.5 y=85.3 z=10.0
NFHNode-BN12 x=59.5 y=85.3 z=10.0
NFHNode-BRBN00 x=13.5 y=224.8 z=10.0
NFHNode-BRBN01 x=36.5 y=224.8 z=10.0
NFHNode-BRBN02 x=59.5 y=224.8 z=10.0
NFHNode-MN10 x=126.5 y=85.3 z=10.0
NFHNode-MN11 x=149.5 y=85.3 z=10.0
NFHNode-MN12 x=172.5 y=85.3 z=10.0
NFHNode_BRMN02 x=172.5 y=224.8 z=10.0
NFHNode-BRMN01 x=149.5 y=224.8 z=10.0
NFHNode-BRMN00 x=126.5 y=224.8 z=10.0
NFHNode-BRTN02 x=285.5 y=224.8 z=10.0
NFHNode-BRTN01 x=262.5 y=224.8 z=10.0
NFHNode-BRTN00 x=239.5 y=224.8 z=10.0
NFHNode-TN12 x=285.5 y=85.3 z=10.0
NFHNode-TN11 x=262.5 y=85.3 z=10.0
NFHNode-TN10 x=239.5 y=85.3 z=10.0
NFHNode-InductorExitNode x=136.5 y=17.0 z=0.0

* Planes
GFHPlane x1=0.0 y1=0.0 z1=0.0 x2=299.0 y2=0.0 z2=0.0
+         x3=299.0 y3=120.0 z3=0.0
+         thick=10.0 seg1=30 seg2=30
+         NFHNode-MN00p (126.5,85.3,0.0)
+         NFHNode-MN02p (172.5,85.3,0.0)
+         NFHNode-MN01p (149.5,85.3,0.0)
+         NFHNode-TN00p (239.5,85.3,0.0)
+         NFHNode-TN01p (262.5,85.3,0.0)
+         NFHNode-TN02p (285.5,85.3,0.0)
+         NFHNode-BN01p (36.5,85.3,0.0)
+         NFHNode-BN02p (59.5,85.3,0.0)
+         NFHNode-BN00p (13.5,85.3,0.0)
+         NFHNode-InductorExitNodep (136.5,17.0,0.0)
+         hole rect (109.5,69.0,0.0,189.5,73.0,0.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-MN00 NFHNode-MN00p
.equiv NFHNode-MN02 NFHNode-MN02p
.equiv NFHNode-MN01 NFHNode-MN01p
.equiv NFHNode-TN00 NFHNode-TN00p
.equiv NFHNode-TN01 NFHNode-TN01p
.equiv NFHNode-TN02 NFHNode-TN02p
.equiv NFHNode-BN01 NFHNode-BN01p
.equiv NFHNode-BN02 NFHNode-BN02p
.equiv NFHNode-BN00 NFHNode-BN00p
.equiv NFHNode-InductorExitNode NFHNode-InductorExitNodep

GFHPlane001 x1=0.0 y1=70 z1=10.0 x2=73.0 y2=70 z2=10.0
+         x3=73.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-BN10p (13.5,85.3,10.0)
+         NFHNode-BN11p (36.5,85.3,10.0)
+         NFHNode-BN12p (59.5,85.3,10.0)
+         NFHNode-BRBN00p (13.5,224.8,10.0)
```

```
+         NFHNode-BRBN01p (36.5,224.8,10.0)
+         NFHNode-BRBN02p (59.5,224.8,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-BN10 NFHNode-BN10p
.equiv NFHNode-BN11 NFHNode-BN11p
.equiv NFHNode-BN12 NFHNode-BN12p
.equiv NFHNode-BRBN00 NFHNode-BRBN00p
.equiv NFHNode-BRBN01 NFHNode-BRBN01p
.equiv NFHNode-BRBN02 NFHNode-BRBN02p

GFHPlane002 x1=113.0 y1=70 z1=10.0 x2=186.0 y2=70 z2=10.0
+         x3=186.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-MN10p (126.5,85.3,10.0)
+         NFHNode-MN11p (149.5,85.3,10.0)
+         NFHNode-MN12p (172.5,85.3,10.0)
+         NFHNode-BRMN01p (149.5,224.8,10.0)
+         NFHNode-BRMN00p (126.5,224.8,10.0)
+         NFHNode_BRMN02p (172.5,224.8,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-MN10 NFHNode-MN10p
.equiv NFHNode-MN11 NFHNode-MN11p
.equiv NFHNode-MN12 NFHNode-MN12p
.equiv NFHNode-BRMN01 NFHNode-BRMN01p
.equiv NFHNode-BRMN00 NFHNode-BRMN00p
.equiv NFHNode_BRMN02 NFHNode_BRMN02p

GFHPlane003 x1=226.0 y1=70 z1=10.0 x2=299.0 y2=70 z2=10.0
+         x3=299.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-BRTN02p (285.5,224.8,10.0)
+         NFHNode-BRTN01p (262.5,224.8,10.0)
+         NFHNode-BRTN00p (239.5,224.8,10.0)
+         NFHNode-TN12p (285.5,85.3,10.0)
+         NFHNode-TN11p (262.5,85.3,10.0)
+         NFHNode-TN10p (239.5,85.3,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-BRTN02 NFHNode-BRTN02p
.equiv NFHNode-BRTN01 NFHNode-BRTN01p
.equiv NFHNode-BRTN00 NFHNode-BRTN00p
.equiv NFHNode-TN12 NFHNode-TN12p
.equiv NFHNode-TN11 NFHNode-TN11p
.equiv NFHNode-TN10 NFHNode-TN10p


* Nodes Angle kept -5 degrees Distance - 220mm from connection point
NFHNode x=197.80  y=-194.29 z=0.0
NFHNode001 x=136.5 y=17.0 z=0.0
NFHNode002 x=299.0 y=-194.29 z=0.0
NFHNode003 x=197.80  y=-194.29 z=0.0

* Segments from paths
EFHPath0 NFHNode001 NFHNode w=16.0 h=15.0 sigma=58000.0 nhinc=5 ...
    nwinc=5 rh=5 rw=5
EFHPath0010 NFHNode003 NFHNode002 w=16.0 h=15.0 sigma=58000.0 ...
```

```
      nhinc=5 nwinc=5 rh=5 rw=5
130
131 .equiv NFHNode-InductorExitNode NFHNode001
132 .equiv NFHNode NFHNode003
133
134
135 * Node shorts
136 .equiv NFHNode-BN10 NFHNode-BN00
137 .equiv NFHNode-BN11 NFHNode-BN01
138 .equiv NFHNode-BN12 NFHNode-BN02
139 .equiv NFHNode-BRBN00 NFHNode-BRBN01
140 .equiv NFHNode-BRBN01 NFHNode-BRBN02
141 .equiv NFHNode-MN00 NFHNode-MN10
142 .equiv NFHNode-MN11 NFHNode-MN01
143 .equiv NFHNode-MN02 NFHNode-MN12
144 .equiv NFHNode_BRMN02 NFHNode-BRMN00
145 .equiv NFHNode-BRMN00 NFHNode-BRMN01
146 .equiv NFHNode-BRTN02 NFHNode-BRTN01
147 .equiv NFHNode-BRTN01 NFHNode-BRTN00
148 .equiv NFHNode-TN10 NFHNode-TN00
149 .equiv NFHNode-TN01 NFHNode-TN11
150 .equiv NFHNode-TN12 NFHNode-TN02
151
152 * Ports
153 *.external NFHNode002 NFHNode-BRBN01
154 .external NFHNode002 NFHNode-BRMN01
155 .external NFHNode002 NFHNode-BRTN01
156
157 .freq fmin=1.0 fmax=100000.0 ndec=1.0
158
159 .end
160
161 .freq fmin=1.0 fmax=100000.0 ndec=1.0
162
163 .end
```

4. **Right**

```
1  * FastHenry input file created using FreeCAD's ElectroMagnetic ...
       Workbench
2  * See http://www.freecad.org, http://www.fastfieldsolvers.com and ...
       http://epc-co.com
3
4  .units mm
5
6  .default sigma=58000.0 nhinc=1 nwinc=1 rh=2 rw=2
7
8  * Nodes
9  NFHNode-BN01 x=36.5 y=85.3 z=0.0
10 NFHNode-BN02 x=59.5 y=85.3 z=0.0
11 NFHNode-BN00 x=13.5 y=85.3 z=0.0
12 NFHNode-MN00 x=126.5 y=85.3 z=0.0
13 NFHNode-MN01 x=149.5 y=85.3 z=0.0
14 NFHNode-MN02 x=172.5 y=85.3 z=0.0
15 NFHNode-TN00 x=239.5 y=85.3 z=0.0
16 NFHNode-TN01 x=262.5 y=85.3 z=0.0
17 NFHNode-TN02 x=285.5 y=85.3 z=0.0
```

```
NFHNode-BN10 x=13.5 y=85.3 z=10.0
NFHNode-BN11 x=36.5 y=85.3 z=10.0
NFHNode-BN12 x=59.5 y=85.3 z=10.0
NFHNode-BRBN00 x=13.5 y=224.8 z=10.0
NFHNode-BRBN01 x=36.5 y=224.8 z=10.0
NFHNode-BRBN02 x=59.5 y=224.8 z=10.0
NFHNode-MN10 x=126.5 y=85.3 z=10.0
NFHNode-MN11 x=149.5 y=85.3 z=10.0
NFHNode-MN12 x=172.5 y=85.3 z=10.0
NFHNode_BRMN02 x=172.5 y=224.8 z=10.0
NFHNode-BRMN01 x=149.5 y=224.8 z=10.0
NFHNode-BRMN00 x=126.5 y=224.8 z=10.0
NFHNode-BRTN02 x=285.5 y=224.8 z=10.0
NFHNode-BRTN01 x=262.5 y=224.8 z=10.0
NFHNode-BRTN00 x=239.5 y=224.8 z=10.0
NFHNode-TN12 x=285.5 y=85.3 z=10.0
NFHNode-TN11 x=262.5 y=85.3 z=10.0
NFHNode-TN10 x=239.5 y=85.3 z=10.0
NFHNode-InductorExitNode x=136.5 y=17.0 z=0.0

* Planes
GFHPlane x1=0.0 y1=0.0 z1=0.0 x2=299.0 y2=0.0 z2=0.0
+         x3=299.0 y3=120.0 z3=0.0
+         thick=10.0 seg1=30 seg2=30
+         NFHNode-MN00p (126.5,85.3,0.0)
+         NFHNode-MN02p (172.5,85.3,0.0)
+         NFHNode-MN01p (149.5,85.3,0.0)
+         NFHNode-TN00p (239.5,85.3,0.0)
+         NFHNode-TN01p (262.5,85.3,0.0)
+         NFHNode-TN02p (285.5,85.3,0.0)
+         NFHNode-BN01p (36.5,85.3,0.0)
+         NFHNode-BN02p (59.5,85.3,0.0)
+         NFHNode-BN00p (13.5,85.3,0.0)
+         NFHNode-InductorExitNodep (136.5,17.0,0.0)
+         hole rect (109.5,53.0,0.0,189.5,57.0,0.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-MN00 NFHNode-MN00p
.equiv NFHNode-MN02 NFHNode-MN02p
.equiv NFHNode-MN01 NFHNode-MN01p
.equiv NFHNode-TN00 NFHNode-TN00p
.equiv NFHNode-TN01 NFHNode-TN01p
.equiv NFHNode-TN02 NFHNode-TN02p
.equiv NFHNode-BN01 NFHNode-BN01p
.equiv NFHNode-BN02 NFHNode-BN02p
.equiv NFHNode-BN00 NFHNode-BN00p
.equiv NFHNode-InductorExitNode NFHNode-InductorExitNodep

GFHPlane001 x1=0.0 y1=70 z1=10.0 x2=73.0 y2=70 z2=10.0
+         x3=73.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-BN10p (13.5,85.3,10.0)
+         NFHNode-BN11p (36.5,85.3,10.0)
+         NFHNode-BN12p (59.5,85.3,10.0)
+         NFHNode-BRBN00p (13.5,224.8,10.0)
+         NFHNode-BRBN01p (36.5,224.8,10.0)
+         NFHNode-BRBN02p (59.5,224.8,10.0)

```

```
76 * Connecting internal plane nodes to actual nodes
77 .equiv NFHNode-BN10 NFHNode-BN10p
78 .equiv NFHNode-BN11 NFHNode-BN11p
79 .equiv NFHNode-BN12 NFHNode-BN12p
80 .equiv NFHNode-BRBN00 NFHNode-BRBN00p
81 .equiv NFHNode-BRBN01 NFHNode-BRBN01p
82 .equiv NFHNode-BRBN02 NFHNode-BRBN02p
83
84 GFHPlane002 x1=113.0 y1=70 z1=10.0 x2=186.0 y2=70 z2=10.0
85 +         x3=186.0 y3=241 z3=10.0
86 +         thick=6.0 seg1=20 seg2=20
87 +         NFHNode-MN10p (126.5,85.3,10.0)
88 +         NFHNode-MN11p (149.5,85.3,10.0)
89 +         NFHNode-MN12p (172.5,85.3,10.0)
90 +         NFHNode-BRMN01p (149.5,224.8,10.0)
91 +         NFHNode-BRMN00p (126.5,224.8,10.0)
92 +         NFHNode_BRMN02p (172.5,224.8,10.0)
93
94 * Connecting internal plane nodes to actual nodes
95 .equiv NFHNode-MN10 NFHNode-MN10p
96 .equiv NFHNode-MN11 NFHNode-MN11p
97 .equiv NFHNode-MN12 NFHNode-MN12p
98 .equiv NFHNode-BRMN01 NFHNode-BRMN01p
99 .equiv NFHNode-BRMN00 NFHNode-BRMN00p
100 .equiv NFHNode_BRMN02 NFHNode_BRMN02p
101
102 GFHPlane003 x1=226.0 y1=70 z1=10.0 x2=299.0 y2=70 z2=10.0
103 +         x3=299.0 y3=241 z3=10.0
104 +         thick=6.0 seg1=20 seg2=20
105 +         NFHNode-BRTN02p (285.5,224.8,10.0)
106 +         NFHNode-BRTN01p (262.5,224.8,10.0)
107 +         NFHNode-BRTN00p (239.5,224.8,10.0)
108 +         NFHNode-TN12p (285.5,85.3,10.0)
109 +         NFHNode-TN11p (262.5,85.3,10.0)
110 +         NFHNode-TN10p (239.5,85.3,10.0)
111
112 * Connecting internal plane nodes to actual nodes
113 .equiv NFHNode-BRTN02 NFHNode-BRTN02p
114 .equiv NFHNode-BRTN01 NFHNode-BRTN01p
115 .equiv NFHNode-BRTN00 NFHNode-BRTN00p
116 .equiv NFHNode-TN12 NFHNode-TN12p
117 .equiv NFHNode-TN11 NFHNode-TN11p
118 .equiv NFHNode-TN10 NFHNode-TN10p
119
120
121 * Nodes Angle kept -5 degrees Distance - 220mm from connection point
122 NFHNode x=197.80  y=-194.29 z=0.0
123 NFHNode001 x=136.5 y=17.0 z=0.0
124 NFHNode002 x=299.0 y=-194.29 z=0.0
125 NFHNode003 x=197.80  y=-194.29 z=0.0
126
127 * Segments from paths
128 EFHPath0 NFHNode001 NFHNode w=16.0 h=15.0 sigma=58000.0 nhinc=5 ...
       nwinc=5 rh=5 rw=5
129 EFHPath0010 NFHNode003 NFHNode002 w=16.0 h=15.0 sigma=58000.0 ...
       nhinc=5 nwinc=5 rh=5 rw=5
130
131 .equiv NFHNode-InductorExitNode NFHNode001
```

```
.equiv NFHNode NFHNode003


* Node shorts
.equiv NFHNode-BN10 NFHNode-BN00
.equiv NFHNode-BN11 NFHNode-BN01
.equiv NFHNode-BN12 NFHNode-BN02
.equiv NFHNode-BRBN00 NFHNode-BRBN01
.equiv NFHNode-BRBN01 NFHNode-BRBN02
.equiv NFHNode-MN00 NFHNode-MN10
.equiv NFHNode-MN11 NFHNode-MN01
.equiv NFHNode-MN02 NFHNode-MN12
.equiv NFHNode_BRMN02 NFHNode-BRMN00
.equiv NFHNode-BRMN00 NFHNode-BRMN01
.equiv NFHNode-BRTN02 NFHNode-BRTN01
.equiv NFHNode-BRTN01 NFHNode-BRTN00
.equiv NFHNode-TN10 NFHNode-TN00
.equiv NFHNode-TN01 NFHNode-TN11
.equiv NFHNode-TN12 NFHNode-TN02

* Ports
*.external NFHNode002 NFHNode-BRBN01
.external NFHNode002 NFHNode-BRMN01
.external NFHNode002 NFHNode-BRTN01

.freq fmin=1.0 fmax=100000.0 ndec=1.0

.end

.freq fmin=1.0 fmax=100000.0 ndec=1.0

.end
```

A.3.2 Changing the Size of Cutout

1. **Shrink 20%**

```
* FastHenry input file created using FreeCAD's ElectroMagnetic ...
    Workbench
* See http://www.freecad.org, http://www.fastfieldsolvers.com and ...
    http://epc-co.com

.units mm

.default sigma=58000.0 nhinc=1 nwinc=1 rh=2 rw=2

* Nodes
NFHNode-BN01 x=36.5 y=85.3 z=0.0
NFHNode-BN02 x=59.5 y=85.3 z=0.0
NFHNode-BN00 x=13.5 y=85.3 z=0.0
NFHNode-MN00 x=126.5 y=85.3 z=0.0
NFHNode-MN01 x=149.5 y=85.3 z=0.0
NFHNode-MN02 x=172.5 y=85.3 z=0.0
NFHNode-TN00 x=239.5 y=85.3 z=0.0
NFHNode-TN01 x=262.5 y=85.3 z=0.0
NFHNode-TN02 x=285.5 y=85.3 z=0.0
NFHNode-BN10 x=13.5 y=85.3 z=10.0
```

```
NFHNode-BN11 x=36.5 y=85.3 z=10.0
NFHNode-BN12 x=59.5 y=85.3 z=10.0
NFHNode-BRBN00 x=13.5 y=224.8 z=10.0
NFHNode-BRBN01 x=36.5 y=224.8 z=10.0
NFHNode-BRBN02 x=59.5 y=224.8 z=10.0
NFHNode-MN10 x=126.5 y=85.3 z=10.0
NFHNode-MN11 x=149.5 y=85.3 z=10.0
NFHNode-MN12 x=172.5 y=85.3 z=10.0
NFHNode_BRMN02 x=172.5 y=224.8 z=10.0
NFHNode-BRMN01 x=149.5 y=224.8 z=10.0
NFHNode-BRMN00 x=126.5 y=224.8 z=10.0
NFHNode-BRTN02 x=285.5 y=224.8 z=10.0
NFHNode-BRTN01 x=262.5 y=224.8 z=10.0
NFHNode-BRTN00 x=239.5 y=224.8 z=10.0
NFHNode-TN12 x=285.5 y=85.3 z=10.0
NFHNode-TN11 x=262.5 y=85.3 z=10.0
NFHNode-TN10 x=239.5 y=85.3 z=10.0
NFHNode-InductorExitNode x=136.5 y=17.0 z=0.0

* Planes
GFHPlane x1=0.0 y1=0.0 z1=0.0 x2=299.0 y2=0.0 z2=0.0
+         x3=299.0 y3=120.0 z3=0.0
+         thick=10.0 seg1=30 seg2=30
+         NFHNode-MN00p (126.5,85.3,0.0)
+         NFHNode-MN02p (172.5,85.3,0.0)
+         NFHNode-MN01p (149.5,85.3,0.0)
+         NFHNode-TN00p (239.5,85.3,0.0)
+         NFHNode-TN01p (262.5,85.3,0.0)
+         NFHNode-TN02p (285.5,85.3,0.0)
+         NFHNode-BN01p (36.5,85.3,0.0)
+         NFHNode-BN02p (59.5,85.3,0.0)
+         NFHNode-BN00p (13.5,85.3,0.0)
+         NFHNode-InductorExitNodep (136.5,17.0,0.0)
+         hole rect (125.5,61.0,0.0,173.5,65.0,0.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-MN00 NFHNode-MN00p
.equiv NFHNode-MN02 NFHNode-MN02p
.equiv NFHNode-MN01 NFHNode-MN01p
.equiv NFHNode-TN00 NFHNode-TN00p
.equiv NFHNode-TN01 NFHNode-TN01p
.equiv NFHNode-TN02 NFHNode-TN02p
.equiv NFHNode-BN01 NFHNode-BN01p
.equiv NFHNode-BN02 NFHNode-BN02p
.equiv NFHNode-BN00 NFHNode-BN00p
.equiv NFHNode-InductorExitNode NFHNode-InductorExitNodep

GFHPlane001 x1=0.0 y1=70 z1=10.0 x2=73.0 y2=70 z2=10.0
+         x3=73.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-BN10p (13.5,85.3,10.0)
+         NFHNode-BN11p (36.5,85.3,10.0)
+         NFHNode-BN12p (59.5,85.3,10.0)
+         NFHNode-BRBN00p (13.5,224.8,10.0)
+         NFHNode-BRBN01p (36.5,224.8,10.0)
+         NFHNode-BRBN02p (59.5,224.8,10.0)

* Connecting internal plane nodes to actual nodes
```

```
77 .equiv NFHNode-BN10 NFHNode-BN10p
78 .equiv NFHNode-BN11 NFHNode-BN11p
79 .equiv NFHNode-BN12 NFHNode-BN12p
80 .equiv NFHNode-BRBN00 NFHNode-BRBN00p
81 .equiv NFHNode-BRBN01 NFHNode-BRBN01p
82 .equiv NFHNode-BRBN02 NFHNode-BRBN02p
83
84 GFHPlane002 x1=113.0 y1=70 z1=10.0 x2=186.0 y2=70 z2=10.0
85 +         x3=186.0 y3=241 z3=10.0
86 +         thick=6.0 seg1=20 seg2=20
87 +         NFHNode-MN10p (126.5,85.3,10.0)
88 +         NFHNode-MN11p (149.5,85.3,10.0)
89 +         NFHNode-MN12p (172.5,85.3,10.0)
90 +         NFHNode-BRMN01p (149.5,224.8,10.0)
91 +         NFHNode-BRMN00p (126.5,224.8,10.0)
92 +         NFHNode_BRMN02p (172.5,224.8,10.0)
93
94 * Connecting internal plane nodes to actual nodes
95 .equiv NFHNode-MN10 NFHNode-MN10p
96 .equiv NFHNode-MN11 NFHNode-MN11p
97 .equiv NFHNode-MN12 NFHNode-MN12p
98 .equiv NFHNode-BRMN01 NFHNode-BRMN01p
99 .equiv NFHNode-BRMN00 NFHNode-BRMN00p
100 .equiv NFHNode_BRMN02 NFHNode_BRMN02p
101
102 GFHPlane003 x1=226.0 y1=70 z1=10.0 x2=299.0 y2=70 z2=10.0
103 +         x3=299.0 y3=241 z3=10.0
104 +         thick=6.0 seg1=20 seg2=20
105 +         NFHNode-BRTN02p (285.5,224.8,10.0)
106 +         NFHNode-BRTN01p (262.5,224.8,10.0)
107 +         NFHNode-BRTN00p (239.5,224.8,10.0)
108 +         NFHNode-TN12p (285.5,85.3,10.0)
109 +         NFHNode-TN11p (262.5,85.3,10.0)
110 +         NFHNode-TN10p (239.5,85.3,10.0)
111
112 * Connecting internal plane nodes to actual nodes
113 .equiv NFHNode-BRTN02 NFHNode-BRTN02p
114 .equiv NFHNode-BRTN01 NFHNode-BRTN01p
115 .equiv NFHNode-BRTN00 NFHNode-BRTN00p
116 .equiv NFHNode-TN12 NFHNode-TN12p
117 .equiv NFHNode-TN11 NFHNode-TN11p
118 .equiv NFHNode-TN10 NFHNode-TN10p
119
120
121 * Nodes Angle kept -5 degrees Distance - 220mm from connection point
122 NFHNode x=197.80  y=-194.29 z=0.0
123 NFHNode001 x=136.5 y=17.0 z=0.0
124 NFHNode002 x=299.0 y=-194.29 z=0.0
125 NFHNode003 x=197.80  y=-194.29 z=0.0
126
127 * Segments from paths
128 EFHPath0 NFHNode001 NFHNode w=16.0 h=15.0 sigma=58000.0 nhinc=5 ...
        nwinc=5 rh=5 rw=5
129 EFHPath0010 NFHNode003 NFHNode002 w=16.0 h=15.0 sigma=58000.0 ...
        nhinc=5 nwinc=5 rh=5 rw=5
130
131 .equiv NFHNode-InductorExitNode NFHNode001
132 .equiv NFHNode NFHNode003
```

```
133
134
135 * Node shorts
136 .equiv NFHNode-BN10 NFHNode-BN00
137 .equiv NFHNode-BN11 NFHNode-BN01
138 .equiv NFHNode-BN12 NFHNode-BN02
139 .equiv NFHNode-BRBN00 NFHNode-BRBN01
140 .equiv NFHNode-BRBN01 NFHNode-BRBN02
141 .equiv NFHNode-MN00 NFHNode-MN10
142 .equiv NFHNode-MN11 NFHNode-MN01
143 .equiv NFHNode-MN02 NFHNode-MN12
144 .equiv NFHNode_BRMN02 NFHNode-BRMN00
145 .equiv NFHNode-BRMN00 NFHNode-BRMN01
146 .equiv NFHNode-BRTN02 NFHNode-BRTN01
147 .equiv NFHNode-BRTN01 NFHNode-BRTN00
148 .equiv NFHNode-TN10 NFHNode-TN00
149 .equiv NFHNode-TN01 NFHNode-TN11
150 .equiv NFHNode-TN12 NFHNode-TN02
151
152 * Ports
153 *.external NFHNode002 NFHNode-BRBN01
154 .external NFHNode002 NFHNode-BRMN01
155 .external NFHNode002 NFHNode-BRTN01
156
157 .freq fmin=1.0 fmax=100000.0 ndec=1.0
158
159 .end
160
161 .freq fmin=1.0 fmax=100000.0 ndec=1.0
162
163 .end
```

2. **Expand 20%**

```
1     * FastHenry input file created using FreeCAD's ElectroMagnetic ...
          Workbench
2 * See http://www.freecad.org, http://www.fastfieldsolvers.com and ...
      http://epc-co.com
3
4 .units mm
5
6 .default sigma=58000.0 nhinc=1 nwinc=1 rh=2 rw=2
7
8 * Nodes
9 NFHNode-BN01 x=36.5 y=85.3 z=0.0
10 NFHNode-BN02 x=59.5 y=85.3 z=0.0
11 NFHNode-BN00 x=13.5 y=85.3 z=0.0
12 NFHNode-MN00 x=126.5 y=85.3 z=0.0
13 NFHNode-MN01 x=149.5 y=85.3 z=0.0
14 NFHNode-MN02 x=172.5 y=85.3 z=0.0
15 NFHNode-TN00 x=239.5 y=85.3 z=0.0
16 NFHNode-TN01 x=262.5 y=85.3 z=0.0
17 NFHNode-TN02 x=285.5 y=85.3 z=0.0
18 NFHNode-BN10 x=13.5 y=85.3 z=10.0
19 NFHNode-BN11 x=36.5 y=85.3 z=10.0
20 NFHNode-BN12 x=59.5 y=85.3 z=10.0
21 NFHNode-BRBN00 x=13.5 y=224.8 z=10.0
```

```
NFHNode-BRBN01 x=36.5 y=224.8 z=10.0
NFHNode-BRBN02 x=59.5 y=224.8 z=10.0
NFHNode-MN10 x=126.5 y=85.3 z=10.0
NFHNode-MN11 x=149.5 y=85.3 z=10.0
NFHNode-MN12 x=172.5 y=85.3 z=10.0
NFHNode_BRMN02 x=172.5 y=224.8 z=10.0
NFHNode-BRMN01 x=149.5 y=224.8 z=10.0
NFHNode-BRMN00 x=126.5 y=224.8 z=10.0
NFHNode-BRTN02 x=285.5 y=224.8 z=10.0
NFHNode-BRTN01 x=262.5 y=224.8 z=10.0
NFHNode-BRTN00 x=239.5 y=224.8 z=10.0
NFHNode-TN12 x=285.5 y=85.3 z=10.0
NFHNode-TN11 x=262.5 y=85.3 z=10.0
NFHNode-TN10 x=239.5 y=85.3 z=10.0
NFHNode-InductorExitNode x=136.5 y=17.0 z=0.0

* Planes
GFHPlane x1=0.0 y1=0.0 z1=0.0 x2=299.0 y2=0.0 z2=0.0
+         x3=299.0 y3=120.0 z3=0.0
+         thick=10.0 seg1=30 seg2=30
+         NFHNode-MN00p (126.5,85.3,0.0)
+         NFHNode-MN02p (172.5,85.3,0.0)
+         NFHNode-MN01p (149.5,85.3,0.0)
+         NFHNode-TN00p (239.5,85.3,0.0)
+         NFHNode-TN01p (262.5,85.3,0.0)
+         NFHNode-TN02p (285.5,85.3,0.0)
+         NFHNode-BN01p (36.5,85.3,0.0)
+         NFHNode-BN02p (59.5,85.3,0.0)
+         NFHNode-BN00p (13.5,85.3,0.0)
+         NFHNode-InductorExitNodep (136.5,17.0,0.0)
+         hole rect (93.5,61.0,0.0,205.5,65.0,0.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-MN00 NFHNode-MN00p
.equiv NFHNode-MN02 NFHNode-MN02p
.equiv NFHNode-MN01 NFHNode-MN01p
.equiv NFHNode-TN00 NFHNode-TN00p
.equiv NFHNode-TN01 NFHNode-TN01p
.equiv NFHNode-TN02 NFHNode-TN02p
.equiv NFHNode-BN01 NFHNode-BN01p
.equiv NFHNode-BN02 NFHNode-BN02p
.equiv NFHNode-BN00 NFHNode-BN00p
.equiv NFHNode-InductorExitNode NFHNode-InductorExitNodep

GFHPlane001 x1=0.0 y1=70 z1=10.0 x2=73.0 y2=70 z2=10.0
+         x3=73.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-BN10p (13.5,85.3,10.0)
+         NFHNode-BN11p (36.5,85.3,10.0)
+         NFHNode-BN12p (59.5,85.3,10.0)
+         NFHNode-BRBN00p (13.5,224.8,10.0)
+         NFHNode-BRBN01p (36.5,224.8,10.0)
+         NFHNode-BRBN02p (59.5,224.8,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-BN10 NFHNode-BN10p
.equiv NFHNode-BN11 NFHNode-BN11p
.equiv NFHNode-BN12 NFHNode-BN12p
```

```
.equiv NFHNode-BRBN00 NFHNode-BRBN00p
.equiv NFHNode-BRBN01 NFHNode-BRBN01p
.equiv NFHNode-BRBN02 NFHNode-BRBN02p

GFHPlane002 x1=113.0 y1=70 z1=10.0 x2=186.0 y2=70 z2=10.0
+         x3=186.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-MN10p (126.5,85.3,10.0)
+         NFHNode-MN11p (149.5,85.3,10.0)
+         NFHNode-MN12p (172.5,85.3,10.0)
+         NFHNode-BRMN01p (149.5,224.8,10.0)
+         NFHNode-BRMN00p (126.5,224.8,10.0)
+         NFHNode_BRMN02p (172.5,224.8,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-MN10 NFHNode-MN10p
.equiv NFHNode-MN11 NFHNode-MN11p
.equiv NFHNode-MN12 NFHNode-MN12p
.equiv NFHNode-BRMN01 NFHNode-BRMN01p
.equiv NFHNode-BRMN00 NFHNode-BRMN00p
.equiv NFHNode_BRMN02 NFHNode_BRMN02p

GFHPlane003 x1=226.0 y1=70 z1=10.0 x2=299.0 y2=70 z2=10.0
+         x3=299.0 y3=241 z3=10.0
+         thick=6.0 seg1=20 seg2=20
+         NFHNode-BRTN02p (285.5,224.8,10.0)
+         NFHNode-BRTN01p (262.5,224.8,10.0)
+         NFHNode-BRTN00p (239.5,224.8,10.0)
+         NFHNode-TN12p (285.5,85.3,10.0)
+         NFHNode-TN11p (262.5,85.3,10.0)
+         NFHNode-TN10p (239.5,85.3,10.0)

* Connecting internal plane nodes to actual nodes
.equiv NFHNode-BRTN02 NFHNode-BRTN02p
.equiv NFHNode-BRTN01 NFHNode-BRTN01p
.equiv NFHNode-BRTN00 NFHNode-BRTN00p
.equiv NFHNode-TN12 NFHNode-TN12p
.equiv NFHNode-TN11 NFHNode-TN11p
.equiv NFHNode-TN10 NFHNode-TN10p


* Nodes Angle kept -5 degrees Distance - 220mm from connection point
NFHNode x=197.80  y=-194.29 z=0.0
NFHNode001 x=136.5 y=17.0 z=0.0
NFHNode002 x=299.0 y=-194.29 z=0.0
NFHNode003 x=197.80  y=-194.29 z=0.0

* Segments from paths
EFHPath0 NFHNode001 NFHNode w=16.0 h=15.0 sigma=58000.0 nhinc=5 ...
    nwinc=5 rh=5 rw=5
EFHPath0010 NFHNode003 NFHNode002 w=16.0 h=15.0 sigma=58000.0 ...
    nhinc=5 nwinc=5 rh=5 rw=5

.equiv NFHNode-InductorExitNode NFHNode001
.equiv NFHNode NFHNode003


* Node shorts
```

```
.equiv NFHNode-BN10 NFHNode-BN00
.equiv NFHNode-BN11 NFHNode-BN01
.equiv NFHNode-BN12 NFHNode-BN02
.equiv NFHNode-BRBN00 NFHNode-BRBN01
.equiv NFHNode-BRBN01 NFHNode-BRBN02
.equiv NFHNode-MN00 NFHNode-MN10
.equiv NFHNode-MN11 NFHNode-MN01
.equiv NFHNode-MN02 NFHNode-MN12
.equiv NFHNode_BRMN02 NFHNode-BRMN00
.equiv NFHNode-BRMN00 NFHNode-BRMN01
.equiv NFHNode-BRTN02 NFHNode-BRTN01
.equiv NFHNode-BRTN01 NFHNode-BRTN00
.equiv NFHNode-TN10 NFHNode-TN00
.equiv NFHNode-TN01 NFHNode-TN11
.equiv NFHNode-TN12 NFHNode-TN02

* Ports
*.external NFHNode002 NFHNode-BRBN01
.external NFHNode002 NFHNode-BRMN01
.external NFHNode002 NFHNode-BRTN01

.freq fmin=1.0 fmax=100000.0 ndec=1.0

.end

.freq fmin=1.0 fmax=100000.0 ndec=1.0

.end
```

Appendix B MATLAB Modeling

B.1 For Three Modules - Braided busbar to Switch-node busbar

```
    clear all; close all; clc;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
For 3 modules
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% R+jL matrix
Z = [
    1.88243e-05+8.71687e-08j, 2.60905e-06+4.54501e-08j, ...
        -2.10004e-06+2.94145e-08j;
    2.63583e-06+4.54263e-08j, 1.39901e-05+7.61139e-08j, ...
        3.28564e-06+4.78651e-08j;
    2.12278e-06+2.94601e-08j, 3.30947e-06+4.78694e-08j, ...
        2.00821e-05+9.19479e-08j
];

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Frequency Domain Evaluation
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Z_100k = real(Z) + 2*pi*100e3*imag(Z)*1j;

V = ones(3,1) * 1;
Z_inv = inv(Z);
Z_100k_inv = inv(Z_100k);
I = Z_100k_inv * V;
imag_inv = inv(imag(Z));

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Time Domain Evaluation
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

% Time domain
dt = 0.01e-6;
nmax = round(140e-6 / dt);
time = dt * (0:(nmax-1));
ii = zeros(3, nmax);
L = 51.15e-6;
V = 1350;
t = 140e-6;
expected_I = V * t / L;

x = 0;

for n = 2:nmax
    vtot = (1 + x) * ones(3, 1);
    current_sum = sum(ii(:, n-1));

    if current_sum < round(expected_I)
        vr = real(Z) * ii(:, n-1);
        vl = vtot - vr;
        ii(:, n) = ii(:, n-1) + imag_inv * dt * vl;
        x = x + 0.1;
    else
        break;
```

```
    end
end

fprintf('Voltage value: %.2f\n', vtot(1));

figure(1);
hold on;
plot(time, ii(1,:), 'LineWidth', 2, 'LineStyle', '-');
plot(time, ii(2,:), 'LineWidth', 2, 'LineStyle', '-');
plot(time, ii(3,:), 'LineWidth', 2, 'LineStyle', '-');
title('Current vs Time');
xlabel('Time (s)', 'FontSize', 20);
ylabel('Current (A)', 'FontSize', 20);
legend('I_{C} Mod 3 SW', 'I_{C} Mod 2 SW', 'I_{C} Mod 1 SW', 'FontSize', ...
    20);
grid on;
zoom on;

figure(2);
hold on;
plot(time, sum(ii, 1), 'LineWidth', 2, 'LineStyle', '-');
grid on;
zoom on;
```

B.2 For Two Modules - Braided busbar to Cable End

```

clear all; clc; close all;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
For 2 modules with cable
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% R+jL matrix
Z = [
    30.00038425+3.03239e-07j 0.000367798+2.65365e-07j
    10.000367814+2.65374e-07j 0.000384893+3.06779e-07j
];
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Frequency Domain Evaluation
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

Z_100k = real(Z) + 2*pi*100e3*imag(Z)*1j;
V = ones(2,1)*1;
Z_inv = inv(Z);
Z_100k_inv = inv(Z_100k);
I = Z_100k_inv*V;
imag_inv = inv(imag(Z));

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
Time Domain Evaluation
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

dt = 0.01e-6;
nmax = round(50e-6/dt);
time = dt*(0:(nmax-1));
ii = zeros(2,nmax);
L = 51.15e-6;
```

```
V_expected = 1350;
t = 50e-6;
expected_I = V_expected*t/L;
x = 0;

for n = 2:nmax
    vtot = (1 + x) * ones(2, nmax);
    current_sum = sum(ii(1, nmax) + ii(2, nmax));
    if current_sum < round(expected_I)
        for n = 2:nmax
            vr(:, n) = real(Z) * ii(:, n-1);
            vl(:, n) = vtot(:, n) - vr(:, n);
            ii(:, n) = ii(:, n-1) + (imag_inv) * dt * vl(:, n);
        end
        x = x + 0.1;
    else
        break;
    end
end

fprintf('Voltage value: %.2f\n', vtot);

figure(3);
hold on;
plot(time, ii(2,:), 'LineWidth', 2, 'LineStyle', '-'); % Solid line with ...
    increased weight
plot(time, ii(1,:), 'LineWidth', 2, 'LineStyle', '-'); % Solid line with ...
    increased weight
title('Current vs Time');
xlabel('Time (s)');
ylabel('Current (A)');
legend('I_{C} Mod 1 SW', 'I_{C} Mod 3 SW');
grid on;
zoom on;
xlabel('Time (s)', 'FontSize', 20); % Increase x-label font size
ylabel('Current (A)', 'FontSize', 20); % Increase y-label font size
lgd = legend('I_{C} Mod 1 SW', 'I_{C} Mod 2 SW', 'I_{C} Mod 3 SW');
set(lgd, 'FontSize', 20); % Increase legend font size

figure(4);
hold on;
plot(time, ii(1,:) + ii(2,:), 'LineWidth', 2, 'LineStyle', '-'); % Solid ...
    line with increased weight
grid on;
zoom on;
```

B.3 Sensitivity Analysis

B.3.1 Moving the Cutout

```
clear all;clc;close all;

\%R+jL matrix Zoriginal = [ \%Row 0: 0.000382018+3.02062e-07j ...
    0.000365211+2.64017e-07j \%Row 1: 0.000365228+2.64026e-07j ...
    0.000381617+3.05137e-07j ];

```

```
5  Zup = [ \%Row 0: Module 3 0.000382125+3.0204e-07j ...
       0.000365338+2.64021e-07j \%Row 1: Module 1 0.000365358+2.6403e-07j ...
       0.000381749+3.05153e-07j ];
6
7  Zdown = [ \%Row 0: 0.000381766+3.02027e-07j 0.000365002+2.63988e-07j ...
       \%Row 1: 0.000365015+2.63995e-07j 0.000381443+3.05111e-07j ];
8
9  Zleft = [\%Row 0: 0.000382065+3.02148e-07j 0.000365063+2.63983e-07j ...
       \%Row 1: 0.000365079+2.63992e-07j 0.000381428+3.05072e-07j ];
10
11 Zright = [ \%Row 0: 0.000382095+3.02027e-07j 0.000365416+2.64059e-07j ...
       \%Row 1: 0.000365437+2.64067e-07j 0.000381865+3.05206e-07j ];
12
13 \%Inverse Evaluation imag\textit{inv}original = inv(imag(Zoriginal)); ...
       imag\textit{inv}up = inv(imag(Zup)); imag\textit{inv}down = ...
       inv(imag(Zdown)); imag\textit{inv}left = inv(imag(Zleft)); ...
       imag\textit{inv}right = inv(imag(Zright));
14
15 \%Time domain dt=0.01e-6; nmax = round(47e-6/dt); time=dt*(0:(nmax-1));
16
17 \%Defining system parameters L = 51.15e-6; V\textit{expected = 1350; t = ...
       47e-6; expected}I = V\_expected*t/L;
18
19 \% Initialinzing current and voltage values i\textit{1 =zeros(2,nmax); ...
       i}2 =zeros(2,nmax); i\textit{3 =zeros(2,nmax); i}4 =zeros(2,nmax); ...
       i\_5 =zeros(2,nmax);
20
21 x1=0; x2=0; x3=0; x4=0; x5=0;
22
23 \%% Zoriginal Current Ramp up for n = 2:nmax vtot\textit{orginal = (1 + ...
       x1) * ones(2, nmax); current}sum\textit{1 = sum(i}1(1, nmax) + ...
       i\_1(2, nmax));
24
25 \begin{verbatim}
26 if current_sum_1 < round(expected_I) for n = 2:nmax vr_1(:, n) = ...
       real(Zoriginal) * i_1(:, n-1); vl_1(:, n) = vtot_orginal(:, n) - ...
       vr_1(:, n); i_1(:, n) = i_1(:, n-1) + (imag_inv_original) * dt * ...
       vl_1(:, n); end x1 = x1 + 0.1; else break; end
27 \end{verbatim}
28
29 end
30
31 \%% Zup Current Ramp up for n = 2:nmax vtot\textit{up = (1 + x2) * ...
       ones(2, nmax); current}sum\textit{2 = sum(i}2(1, nmax) + i\_2(2, nmax));
32
33 \begin{verbatim}
34 if current_sum_2 < round(expected_I) for n = 2:nmax vr_2(:, n) = ...
       real(Zup) * i_2(:, n-1); vl_2(:, n) = vtot_up(:, n) - vr_2(:, n); ...
       i_2(:, n) = i_2(:, n-1) + (imag_inv_up) * dt * vl_2(:, n); end x2 = ...
       x2 + 0.1; else break; end
35 \end{verbatim}
36
37 end
38
39 \%% Zdown Current Ramp up for n = 2:nmax vtot\textit{down = (1 + x3) * ...
       ones(2, nmax); current}sum\textit{3 = sum(i}3(1, nmax) + i\_3(2, nmax));
40
41 \begin{verbatim}
```

```
42 if current_sum_3 < round(expected_I) for n = 2:nmax vr_3(:, n) = ...
       real(Zdown) * i_3(:, n-1); vl_3(:, n) = vtot_down(:, n) - vr_3(:, n); ...
       i_3(:, n) = i_3(:, n-1) + (imag_inv_down) * dt * vl_3(:, n); end x3 = ...
       x3 + 0.1; else break; end
43 \end{verbatim}
44
45 end
46
47 \%% Zleft Current Ramp up for n = 2:nmax vtot\textit{left = (1 + x4) * ...
       ones(2, nmax); current}sum\textit{4 = sum(i}4(1, nmax) + i\_4(2, nmax));
48
49 \begin{verbatim}
50 if current_sum_4 < round(expected_I) for n = 2:nmax vr_4(:, n) = ...
       real(Zleft) * i_4(:, n-1); vl_4(:, n) = vtot_left(:, n) - vr_4(:, n); ...
       i_4(:, n) = i_4(:, n-1) + (imag_inv_left) * dt * vl_4(:, n); end x4 = ...
       x4 + 0.1; else break; end
51 \end{verbatim}
52
53 end
54
55 \%% Zright Current Ramp up for n = 2:nmax vtot\textit{right = (1 + x5) * ...
       ones(2, nmax); current}sum\textit{5 = sum(i}5(1, nmax) + i\_5(2, nmax));
56
57 \begin{verbatim}
58 if current_sum_5 < round(expected_I) for n = 2:nmax vr_5(:, n) = ...
       real(Zright) * i_5(:, n-1); vl_5(:, n) = vtot_right(:, n) - vr_5(:, ...
       n); i_5(:, n) = i_5(:, n-1) + (imag_inv_right) * dt * vl_5(:, n); end ...
       x5 = x5 + 0.1; else break; end
59 \end{verbatim}
60
61 end
62
63 \%% Plotting obtained results fprintf('Voltage value: ...
       \%.2f\textbackslash{}n', vtot\textit{orginal); fprintf('Voltage ...
       value: \%.2f\textbackslash{}n', vtot}up); fprintf('Voltage value: ...
       \%.2f\textbackslash{}n', vtot\textit{down); fprintf('Voltage value: ...
       \%.2f\textbackslash{}n', vtot}left); fprintf('Voltage value: ...
       \%.2f\textbackslash{}n', vtot\_right);
64
65 figure(1); \%Plot current for Module 1 hold on; plot(time, ...
       i\textit{1(2,:), 'LineWidth', 2, 'LineStyle', '-'); \% Plot Original ...
       Current - Mod 1 plot(time, i}2(2,:), 'LineWidth', 2, 'LineStyle', ...
       '-'); \% Plot Down Current - Mod 1 plot(time, i\textit{3(2,:), ...
       'LineWidth', 2, 'LineStyle', '-'); \% Plot Original Current - Mod 1 ...
       plot(time, i}4(2,:), 'LineWidth', 2, 'LineStyle', '-'); \% Plot Down ...
       Current - Mod 1 plot(time, i\textit{5(2,:), 'LineWidth', 2, ...
       'LineStyle', '-'); \% Plot Down Current - Mod 1 title('Current vs ...
       Time - Module 1', 'FontSize',20); xlabel('Time (s)','FontSize',20); ...
       ylabel('Current (A)','FontSize',20); legend('I}\{Original\} Mod 1 ...
       SW', 'I\textit{\{Up\} Mod 1 SW','I}\{Down\} Mod 1 ...
       SW','I\textit{\{Left\} Mod 1 SW','I}\{Right\} Mod 1 ...
       SW','FontSize',20); grid on; zoom on;
66
67 \% Add value of current at the last point of measurement text(time(end), ...
       i\textit{1(2,end), sprintf('\%.2f', i}1(2,end)), 'VerticalAlignment', ...
       'bottom', 'HorizontalAlignment', 'right', 'FontSize', 20); ...
       text(time(end), i\textit{2(2,end), sprintf('\%.2f', i}2(2,end)), ...
       'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
```

```
    'FontSize', 20); text(time(end), i\textit{3(2,end), sprintf('\%.2f', ...
    i}3(2,end)), 'VerticalAlignment', 'bottom', 'HorizontalAlignment', ...
    'right', 'FontSize
68
69  text(time(end), i_1(2,end)), 'VerticalAlignment', 'bottom', ...
        'HorizontalAlignment', 'right', 'FontSize', 20);
70  text(time(end), i_2(2,end)), sprintf('%.2f', i_2(2,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
71  text(time(end), i_3(2,end)), sprintf('%.2f', i_3(2,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
72  text(time(end), i_4(2,end)), sprintf('%.2f', i_4(2,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
73  text(time(end), i_5(2,end)), sprintf('%.2f', i_5(2,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
74
75  figure(2);
76  %Plot current for Module 3
77  hold on;
78  plot(time, i_1(1,:), 'LineWidth', 2, 'LineStyle', '-'); % Plot Original ...
        Current - Mod 1
79  plot(time, i_2(1,:), 'LineWidth', 2, 'LineStyle', '-'); % Plot Down ...
        Current - Mod 1
80  plot(time, i_3(1,:), 'LineWidth', 2, 'LineStyle', '-'); % Plot Original ...
        Current - Mod 1
81  plot(time, i_4(1,:), 'LineWidth', 2, 'LineStyle', '-'); % Plot Down ...
        Current - Mod 1
82  plot(time, i_5(1,:), 'LineWidth', 2, 'LineStyle', '-'); % Plot Down ...
        Current - Mod 1
83  title('Current vs Time - Module 3', 'FontSize',20);
84  xlabel('Time (s)','FontSize',20);
85  ylabel('Current (A)','FontSize',20);
86  legend('I_{Original} Mod 3 SW', 'I_{Up} Mod 3 SW','I_{Down} Mod 3 ...
        SW','I_{Left} Mod 3 SW','I_{Right} Mod 3 SW','FontSize',20);
87  grid on;
88  zoom on;
89
90  % Add value of current at the last point of measurement
91  text(time(end), i_1(1,end), sprintf('%.2f', i_1(1,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
92  text(time(end), i_2(1,end), sprintf('%.2f', i_2(1,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
93  text(time(end), i_3(1,end), sprintf('%.2f', i_3(1,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
94  text(time(end), i_4(1,end), sprintf('%.2f', i_4(1,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
95  text(time(end), i_5(1,end), sprintf('%.2f', i_5(1,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
```

B.3.2 Changing size of the Cutout

```
1
2  clear all;clc;close all;
3
4  %R+jL matrix
5  Zoriginal_size = [ %Row 0: Module 3
6      0.000382018+3.02062e-07j 0.000365211+2.64017e-07j
7    %Row 1: Module 1
8    0.000365228+2.64026e-07j 0.000381617+3.05137e-07j
9  ];
10
11 Z_shrink =   [
12       %Row 0:
13       0.000380844+3.01451e-07j 0.000364423+2.63627e-07j
14   %Row 1:
15   0.000364441+2.63632e-07j 0.000381078+3.04882e-07j
16     ];
17
18 Z_expand = [  %Row 0:
19     0.000383507+3.03043e-07j 0.00036627+2.64707e-07j
20   %Row 1:
21   0.000366278+2.64714e-07j 0.000382384+3.05625e-07j
22 ];
23
24 %Inverse Evaluation
25 imag_inv_original_size = inv(imag(Zoriginal_size));
26 imag_inv_shrink = inv(imag(Z_shrink));
27 imag_inv_expand = inv(imag(Z_expand));
28
29 %Time domain
30 dt=0.01e-6;
31 nmax = round(47e-6/dt);
32 time=dt*(0:(nmax-1));
33
34 %Defining system parameters
35 L = 51.15e-6;
36 V_expected = 1350;
37 t = 47e-6;
38 expected_I = V_expected*t/L;
39
40 % Initialinzing current and voltage values
41 i_1 =zeros(2,nmax);
42 i_2 =zeros(2,nmax);
43 i_3 =zeros(2,nmax);
44
45 x1=0;
46 x2=0;
47 x3=0;
48
49 %% Zoriginal Current Ramp up
50 for n = 2:nmax
51     vtot_orginal = (1 + x1) * ones(2, nmax);
52     current_sum_1 = sum(i_1(1, nmax) + i_1(2, nmax));
53
54     if current_sum_1 < round(expected_I)
55         for n = 2:nmax
```

```
56              vr_1(:, n) = real(Zoriginal_size) * i_1(:, n-1);
57              vl_1(:, n) = vtot_orginal(:, n) - vr_1(:, n);
58              i_1(:, n) = i_1(:, n-1) + (imag_inv_original_size) * dt * ...
                    vl_1(:, n);
59          end
60          x1 = x1 + 0.1;
61      else
62          break;
63      end
64  end
65
66  %% Zshrink Current Ramp up
67  for n = 2:nmax
68      vtot_shrink = (1 + x2) * ones(2, nmax);
69      current_sum_2 = sum(i_2(1, nmax) + i_2(2, nmax));
70
71      if current_sum_2 < round(expected_I)
72          for n = 2:nmax
73              vr_2(:, n) = real(Z_shrink) * i_2(:, n-1);
74              vl_2(:, n) = vtot_shrink(:, n) - vr_2(:, n);
75              i_2(:, n) = i_2(:, n-1) + (imag_inv_shrink) * dt * vl_2(:, n);
76          end
77          x2 = x2 + 0.1;
78      else
79          break;
80      end
81  end
82
83  %% Zexpand Current Ramp up
84  for n = 2:nmax
85      vtot_expand = (1 + x3) * ones(2, nmax);
86      current_sum_3 = sum(i_3(1, nmax) + i_3(2, nmax));
87
88      if current_sum_3 < round(expected_I)
89          for n = 2:nmax
90              vr_3(:, n) = real(Z_expand) * i_3(:, n-1);
91              vl_3(:, n) = vtot_expand(:, n) - vr_3(:, n);
92              i_3(:, n) = i_3(:, n-1) + (imag_inv_expand) * dt * vl_3(:, n);
93          end
94          x3 = x3 + 0.1;
95      else
96          break;
97      end
98  end
99
100 %% Plotting obtained results
101 fprintf('Voltage value: %.2f\n', vtot_orginal);
102 fprintf('Voltage value: %.2f\n', vtot_shrink);
103 fprintf('Voltage value: %.2f\n', vtot_expand);
104
105 figure(1);
106 %Plot current for Module 1
107 hold on;
108 plot(time, i_1(2,:), 'LineWidth', 2, 'LineStyle', '-'); % Plot Original ...
        Current - Mod 1
109 plot(time, i_2(2,:), 'LineWidth', 2, 'LineStyle', '-'); % Plot Down ...
        Current - Mod 1
```

```
110 plot(time, i_3(2,:), 'LineWidth', 2, 'LineStyle', '-'); % Plot Original ...
        Current - Mod 1
111 title('Current vs Time - Module 1', 'FontSize',20);
112 xlabel('Time (s)','FontSize',20);
113 ylabel('Current (A)','FontSize',20);
114 legend('I_{Original} Mod 1 SW', 'I_{Shrink} Mod 1 SW','I_{Expand} Mod 1 ...
        SW','FontSize',20);
115 grid on;
116 zoom on;
117
118 % Add value of current at the last point of measurement
119 text(time(end), i_1(2,end), sprintf('%.2f', i_1(2,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
120 text(time(end), i_2(2,end), sprintf('%.2f', i_2(2,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
121 text(time(end), i_3(2,end), sprintf('%.2f', i_3(2,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
122
123 figure(2);
124 %Plot current for Module 3
125 hold on;
126 plot(time, i_1(1,:), 'LineWidth', 2, 'LineStyle', '-'); % Plot Original ...
        Current - Mod 1
127 plot(time, i_2(1,:), 'LineWidth', 2, 'LineStyle', '-'); % Plot Down ...
        Current - Mod 1
128 plot(time, i_3(1,:), 'LineWidth', 2, 'LineStyle', '-'); % Plot Original ...
        Current - Mod 1
129
130 title('Current vs Time - Module 3', 'FontSize',20);
131 xlabel('Time (s)','FontSize',20);
132 ylabel('Current (A)','FontSize',20);
133 legend('I_{Original} Mod 3 SW', 'I_{Shrink} Mod 3 SW','I_{Expand} Mod 3 ...
        SW','FontSize',20);
134 grid on;
135 zoom on;
136
137 % Add value of current at the last point of measurement
138 text(time(end), i_1(1,end), sprintf('%.2f', i_1(1,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
139 text(time(end), i_2(1,end), sprintf('%.2f', i_2(1,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
140 text(time(end), i_3(1,end), sprintf('%.2f', i_3(1,end)), ...
        'VerticalAlignment', 'bottom', 'HorizontalAlignment', 'right', ...
        'FontSize', 20);
```