Development and Analysis of Modular Multilevel Converter Integrated with Battery Storage for Grid Support

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Abstract:

This thesis investigates grid support using battery energy storage systems. Initially, a problem analysis is conducted to understand various converters, energy storage systems, and control algorithms used in grid support. The focus then shifts to Modular Multilevel Converters (MMC) integrated with second-life batteries in each submodule via bidirectional buck-boost converters. Dynamic modeling of the MMC for output current control and circulating currents is developed, accompanied by electrical circuit simulations. Various control algorithms, including output current control, active/reactive power control, circulating current suppression, and balancing strategies, are analyzed and implemented. A small-signal model of the bidirectional buck-boost converter is derived, and controllers are tuned for a constant current and constant voltage protocol for battery charging and discharging. Second-life batteries are examined, and an electrical equivalent model is defined, with parameters identified based on the state of charge and charge-discharge cycles to simulate aging processes. Integration of batteries into the MMC is performed, with preliminary analyses showing that battery-integrated MMCs can assist with active power supply and demand regulation. Finally, further research aspects are identified to enhance system model accuracy and simulation fidelity.

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Preface

This project was created by master students of the group APEL4-2-24 attending Aalborg University, Esbjerg. Anytime in the project the terms "we", "our" or "the group" is used, they refer to the student group listed below.

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Chapter 1

Introduction

1.1 Grid Challenges

As the demand and integration of renewable energy systems is increasing, the industry is presented with new challenges. Demand fluctuation, the intermittent nature of renewable power generation, and the essential need for efficient energy storage solutions. One promising approach to maintaining the quality and reliability of the power system under these conditions is through the integration of Energy Storage Systems (ESS), with a particular focus on Battery Energy Storage Systems (BESS). BESSs are gaining attention due to the ongoing electrification of transportation and their potential to provide vital grid services, including load leveling, peak shaving, and facilitating the integration of renewable energy sources [1, 2].

1.2 Battery Energy Storage System

Batteries play a critical role in modern grid infrastructure, offering a flexible and scalable solution to energy storage challenges. As the grid transitions towards a more sustainable and renewable-centric model, the importance of battery storage is increasingly recognized. However, this surge in battery usage brings to the forefront the issue of battery waste and the environmental implications of battery production, usage, and disposal. Addressing these concerns is crucial for the sustainable growth of battery storage solutions and their continued role in enhancing grid stability and renewable energy integration.

Chapter 2

Problem Analysis

2.1 Grid Support Applications

As the use of renewable energy sources grows, the challenge of managing their inherently variable energy output becomes crucial. These renewable sources can produce differing amounts of electricity depending on the time of the day, making it essential to constantly balance electricity generation with consumption to ensure a stable power grid. This has brought grid support into focus as a key issue. Terms like flexibility and resilience are encompassed withing the grid support topic. Flexibility refers to the ability of power systems to adapt to changes and manage variations in electricity demand and supply, particularly from renewable sources. Resilience, on the other hand, is the power system's capacity to withstand and recover from disruptions, ensuring continuous and reliable service [3]. Some of the techniques used for grid support includes, peak shaving, voltage and frequency regulation and energy arbitrage.

As the electricity demand fluctuates throughout the day and the number of end-users rises, ensuring the grid's capacity to meet peak demands becomes crucial for its efficient and reliable operation. The growth in peak load presents challenges, including potential power outages and the escalating costs associated with electricity generation and transmission [4]. Traditional methods to manage peak demand involve cycling in conventional power plants, such as coal or gas power plants [5]. However, these facilities are burdened with high Operation and Maintenance (O&M) costs, substantial fuel consumption, and significant carbon dioxide emissions [4].

2.1.1 Peak Shaving

In response to these challenges, peak shaving is becoming an important area of research. Peak shaving is a technique that is used to level out the increased peaks in electricity use, that occurs when there is an increased demand of power by industrial and commercial consumers. By reducing peak electricity demand, the strain on the grid is lessened,

leading to lower operational costs and enhanced system reliability. Implementing peak shaving benefits grid operators by improving power quality, promoting efficient power utilization, enabling cost reductions, and facilitating the integration of renewable energy sources. End-users also gain through reduced electricity costs [4, 6, 7].

Research into peak shaving strategies includes exploring ESS, vehicle-to-grid (V2G) technologies, and Demand Side Management (DSM). ESS, in particular, offers promising potential for peak shaving by storing energy during off-peak times for use during peak periods. This approach not only mitigates the need for high-demand power generation but also contributes to overall electricity cost reductions. Various ESS technologies, such as BESS and Second-Life Battery Energy Storage Systems (SLBESS), are under consideration [4].

2.1.2 Voltage and Frequency Regulation

Renewable energy sources are designed to supply power to the grid within a specified voltage and frequency, and cease to produce power when exceeding these specified limits. These limits are country specific. Transmission System Operators (TSOs) develop Grid Codes (GCs) [8]. These are necessary to integrate and adopt renewable energy systems. As the technology advances, the GCs are constantly updated. The requirements set by the GC typically focus on a single active feature at any given time. These requirements encompass the following:

- Reduction of the active power for over - frequency and increase of the active power for under - frequency as a response to frequency variation.
- In static grid support, the power generator must adhere to adjustable reactive power settings. This involves maintaining either a constant power factor (PF) or reactive power (Q), where Q changes based on grid voltage variations, denoted as Q(v). The PF can vary according to the active power operation, represented as cosϕ (P).
- Dynamic grid support, such as low and high voltage ride-through capabilities, requires the power generator to supply reactive current according to a specific voltage transient curve.

The compliance with relevant GCs are mandatory [9]. To keep the renewable energy systems running within the specified limits, techniques for voltage and frequency regulation are employed. Voltage regulation ensures the voltage supplied to end-users remains within a predetermined range, mitigating fluctuations in electricity demand or generation. This regulation is critical for the protection of electrical appliances and the maintenance of consistent power quality. Frequency regulation, in contrast, aims to balance electricity generation and consumption across the grid, maintaining the system frequency at a standard value, typically 50 or 60 Hz, depending on the geographical

region. These mechanisms are essential for the stability and efficiency of the electrical supply system, ensuring reliable and safe electricity distribution. For the implementation of voltage and frequency regulation, ESS can be used. In [9], two methods for the power control, P(f) and combined P(f) - Q(v) are reviewed. The P(f) active power control method, that is responsive to line frequency variations. This method works by automatically adjusting the power flow direction of the ESS converters in response to frequency changes. Active power adjustment works by either injecting power into the grid (if the frequency is below a specified threshold) or absorb power from the grid (if the frequency is above a specified threshold), this way stabilizing the grid's frequency. As renewables are inherently a variable source of energy, the P(f) strategy offers flexibility, meaning that the ESS converters can dynamically transition from receiving power to generating power or vice versa. The P(f) - Q(v) power control strategy adds to the active power control method P(f), by including a reactive power control component Q(v). The added reactive power control component Q(v) focuses on reactive power control in regards to voltage fluctuations. By modulating reactive power it aims to maintain the voltage levels within a specific threshold. This control method can be implemented both in single - phase and three - phase distributed ESS converters without the need for communication protocols with the TSO.

2.1.3 Energy Arbitrage

Energy arbitrage refers to the practise of utilizing the energy price market, by purchasing, storing and selling energy based on the demand of it. Not only does this technique provide a financial benefit to the energy storage operators, it is used for grid support applications, by balancing the supply and demand on the grid. For the storage of energy, ESS are of interest. As previously mentioned, ESS are applicable for a wide range of grid support applications, however, energy arbitrage offers the largest profit opportunity for ESS [7, 10].

2.2 Batteries for Grid Support

Mentioned in Section 2.1 were the grid support applications, which emphasized the use of ESS. There are many different ESS for grid support. They come in different forms of energy storage such as mechanical, thermal, electrical, chemical or electrochemical [7, 11]. Emphasis is put on the electrochemical type of energy storage, particularly Li-ion, due to the potential re-usability for second-life applications.

2.2.1 Electrochemical Energy Storage

Electrochemical energy storage for grid support is a fast growing and diverse sector which is crucial for grid-connected system stability, reliability and safety. Electrochemical energy storage involve conversion of electrical energy into chemical energy for storage and back into electrical energy whenever needed. There are many different types of chemistries and systems used in electrochemical batteries all with different characteristics, advantages and applications. For example, Li-ion batteries store energy through movement of lithium ions between anode and cathode during charge and discharge cycles. They are known for high energy density and long life cycle. Li-ion batteries are used in portable electronics, electric vehicles and grid support applications such as peak shaving, load leveling and renewable energy integration. Lead-Acid batteries, one of the oldest types of rechargeable batteries, store energy through chemical reactions between lead, lead dioxide and sulfuric acid. They are known for high power capacity, low cost and robustness. Other forms of electrochemical energy storage, such as flow or solid-state batteries, are getting more attention both in research and industry. Flow batteries differ from conventional batteries by storing chemical energy in external tanks and convert it to electricity in electrochemical cells which allows for energy capacity decoupling from power capacity meaning increasing size of tanks can increase energy capacity independently of power output. Such type of batteries are useful for long-duration energy storage such as renewable energy integration and grid stabilization over several hours or days. Solid-state batteries are interesting due to the fact that they replace the liquid or gel electrolytes with solid material. They promise higher energy densities, improved safety and longer lifespans. While still mostly in development phase, solid-state batteries are expected to revolutionize electric vehicle industry and portable electronics due to improved performance and safety features [7].

2.2.2 SLBs in Grid-Support Applications

Electric vehicle (EV) batteries typically retain about 80% of their capacity at the end of their primary vehicular use, a point defined by the US Advanced Battery Consortium (USABC) as a 20% loss in capacity or power density at an 80% depth of discharge (DOD)

[7, 12]. This residual capacity, while not suitable for vehicular propulsion, is quite adequate for stationary energy storage systems. Research suggests that the daily transportation needs of American drivers could be met with batteries that have as little as 30% of their original capacity, indicating that the USABC's 80% threshold may have more significant implications for plug-in hybrid electric vehicles.

The transition of EV batteries to their "second life" occurs either due to capacity degradation or when the vehicle's service life ends before the battery's. These second-life batteries, which offer a cost-effective alternative to new ones, are influenced by factors such as cost, environmental impact, and aging. Despite the increasing use of lithium-ion batteries in EVs and their advantages over lead-acid batteries, particularly in high-capacity applications, the recycling process for lithium-ion is less mature and more complex. Recycling costs are high because materials like lithium, which make up only 2-7% of the battery's weight, are five times more expensive to recycle than to source new, and cobalt recycling may soon be unnecessary due to advances in battery technology.

The expected lifespan of EV battery packs is about 8 years. Analyzing the market's offerings, the average capacity (34.21 kWh), and the number of batteries from 2018 (165,410 units), projections indicate that around 4526.94 MWh will be available from second-life batteries by 2026. It is estimated that by 2040 around 3.4 million kilograms of lithium-ion EV battery cells could enter the waste stream [13].

For energy storage, a used Nissan Leaf battery, for example, can retain 80% of its initial energy, equating to about 15 kWh suitable for low C-rate applications for years. Projections state that by 2028, 548 GWh of battery capacity from used EV batteries will be globally available, with China accounting for approximately 240 GWh [13].

Current projects exploring the use of second-life batteries are largely research-based, with universities and companies investigating energy storage solutions using repurposed EV batteries. These endeavors highlight the nascent stage of second-life battery systems and their potential for broader application.

However, the lack of formal regulations and standards for second-life battery applications poses challenges, as does the lack of universal standards in the EV industry, such as for charging technologies.

Table 2.1: Notable second-life battery projects [14]

Joint Ventures	Description	Location
Daimler GETEC/ the mobility house remondis /EnBW	Battery storage unit with a total capacity of 13 MWh using degraded EV batteries from Daimler EV models	Luenen, Germany
BMW/PG&E	18-month pilot project to demonstrate EV smart charging and optimization grid efficiency with participation of 100 BMW i3 owners	San Francisco, USA
Nissan Sumitoto (4R Energy)/Green charge network	System (600 kWh/400 kWh): 16 Nissan Leaf LIBs regulate energy from a solar plant	Osaka, Japan
BMW/Vattenfall/Bosch	2,600 battery modules from 100 electric cars, and provides 2MW of output and 2.8 MWh of capacity	Hamburg, Germany
Renault/Connected Energy Ltd	"E-STOR": on-grid providing energy storage that prevents power grid overload and balances supply and demand	United Kingdom, Europe
Mitsubishi/PSA EDF/ Forsee Power/ MMC	Bi-directional battery energy consumption optimization from retired batteries	Paris, France
General Motors/ ABB	5 Chevrolet Volt LIBs, 74 kW solar array & two 2 kW wind turbines to power a General Motors office building site	USA

Evaluation methods for SLBs

The initial step in developing SLBESS is the careful dismantling of used battery packs, a process that is crucial due to the variety of individual cells and configurations used by different EV manufacturers [12, 13].

After disassembly, the individual cells are tested to evaluate their suitability for second-life usage. A battery pack's performance is limited by the cell with the lowest capacity, making it vital to assess and group cells by voltage, capacity, and State of Health (SOH) for uniformity in the second-life packs.

The evaluation starts with a visual inspection to remove any cells with obvious physical damage. Cells passing this phase undergo voltage checks, and those meeting criteria proceed to SOH evaluation. Battery testing often includes cycling studies, where cells undergo repeated charge and discharge cycles in a controlled setting to observe changes in capacity, voltage, SOH, and physical integrity.

For instance, a high-power cycling test can significantly reduce cell capacity and efficiency, as evidenced by a 68% capacity loss and a 12% efficiency drop after 75 cycles, often accompanied by physical deformation. Conversely, low-power cycling shows no apparent adverse effects.

Battery tests, such as pulse power tests, capacity tests, Open Circuit Voltage (OCV) vs. State of Charge (SOC) tests, impedance tests, and hybrid pulse power tests, serve to delineate battery characteristics during cycling and help determine model parameters like time-domain parameters through extended tests.

Acknowledging the importance of remaining capacity for batteries in the second-life

phase is essential for meaningful re-manufacturing contributions. For instance, a study involving over 100 EVs leased to the public collected data over 27 months to analyze usage and charging patterns. Post-first-life analysis revealed that the second-life span varies based on previous usage patterns.

Aging experiments demonstrate that the battery's ability to charge and discharge diminishes over time due to capacity fade. This illustrates that second-life expectancy is variable and contingent on past and anticipated use patterns.

Through such assessments, cells can be sorted by capacity and color-coded for streamlined integration into SLBESS: green for cells above 80% capacity, and other colors like blue for 80%, violet for 60%, yellow for 40%, and red for below 20%, indicating unsuitability for use.

Cost of SLBs

The cost of SLBESS is influenced by production expenses and service margins. Key cost contributors identified by Sandia National Laboratory include the acquisition of SLBs, labor, overhead, and materials for packaging. Figures in their report detail these expenses and manufacturing costs for different SLB sectors.

It has been explored how SLBESS module size impacts cost, considering cell fault rates and the expense of acquiring used batteries for modules up to 24 kWh. Higher fault rates lead to lower purchase costs but higher production expenses due to increased testing. Conversely, a fault rate of 0.01% results in the lowest costs, approximately $30/kWh for modules between 8-24 kWh [13].

Application of SLBs based on area

SLBs are utilized across residential, commercial, and industrial areas due to their varied applications.

Residential Use: SLBs cater to residential electricity demands that fluctuate throughout the day, mainly for heating. Integration with renewable energy systems like solar PV meets daytime needs, but evening peaks, when PV is inactive, require energy storage solutions. SLBs, with their lower costs, offer a feasible option. They typically need 3-4 kWh for load following and 25 kWh for backup, with discharges above 50% DoD.

Commercial Use: Commercial electricity demand surpasses residential, peaking near midday, making evening demand shifting less critical. Dependence on variable PV output prompts the need for storage solutions. For load following, 75-100 kWh SLBs are adequate, while peak shaving requires larger capacities of 3000-4000 kWh. Reconditioned batteries like the Nissan Leaf, with 70% capacity, are used for peak shaving but are less likely for commercial peak shaving due to the high number of batteries required unless used in DSM strategies. For load following, 4-6 reconditioned batteries suffice, suitable in high solar irradiance areas.

Industrial Use: Industrial demand is significantly higher, with midday peaks coinciding with maximum PV output. Large storage capacities of up to 100,000 kWh are necessary for load leveling, making the use of reconditioned batteries impractical due to the sheer number required. Renewable firming in the industrial sector needs less capacity, between 1000 to 10,000 kWh. While peak shaving needs parallel commercial requirements, transmission stabilization is not suitable for reconditioned batteries due to the high power bursts exceeding their C-rate.

Applications of SLBs based on usage

As EV adoption grows, the availability of batteries in their second life is expected to increase. These SLBs can be repurposed and assembled into large packs with megawatt-hour capacities, making them suitable for use in stationary grid applications [7, 12, 13]. These grid applications include, but are not limited to the previously mentioned grid support applications, such as peak shaving, voltage and frequency regulation and energy arbitrage.

Impact of SLBESS

With the rise of renewable energy sources (RES), ESS are crucial for addressing RES intermittencies and providing grid services. However, the high cost of new ESS is a concern. SLBESS offer a cost-effective solution, capable of performing grid duties at approximately 31.71% the cost of new ESS [13]. This affordability is key to increasing RES integration and providing operators with economical options for reliable service.

The high cost of EV batteries significantly raises EV prices. The SLBESS industry can add value to used EV batteries, potentially increasing their resale value and lowering the purchase price of new EVs. Nissan's battery takeback or leasing system exemplifies this approach, aiming to boost EV adoption and support greener transportation. The second-life value of a Leaf battery, estimated at $3,040 out of a total $15,000, highlights the potential for cost savings, although early-generation EV owners may not benefit directly as new battery prices could drop by up to 70% [13].

SLBESS plays a crucial role in environmental conservation and energy efficiency. Without reuse, an estimated 63% of EV batteries would become waste by 2040, wasting energy and resources. Reusing these batteries reduces landfill waste and maximizes the use of the energy invested in their production. Studies indicate that SLB application could cut gross energy demand and global warming potential by 15-70%, improve battery use through better recycling, and significantly reduce CO2 emissions. For instance, SLB-supported renewable penetration could yield 15 TWh of energy annually by 2050 in California and halve CO2 emissions, effectively doubling the GHG emission reduction compared to converting conventional vehicles to electric ones.

2.3 Power Converters for Battery Connection to the Grid

Due to intermittency of renewable energy sources, BESS plays a crucial role to ensure reliability when solar and wind power sources are connected to the grid. In the recent years, there has been a significant increase in BESS deployment worldwide despite many challenges such installations poses. To meet medium voltage (MV) grid voltage requirements, electrochemical cells which are usually in the range of 3-4V/cell must be connected in series. In many cases, series connection is not sufficient to reach required grid voltages, thus necessitating additional DC/DC converters to step-up the voltage. Inclusion of a DC/DC converter also allows dc-link voltage to be controlled which would ultimately allow for reduced number of cells in series. In practice, grid connected batteries comprises a battery pack, DC/DC stage, DC/AC stage where converter topologies can be either transformer based or transformerless. This section analyses differences between transformer-based and transformerless interfaces for integration of BESS to the grid. Converter topologies for different interfaces are discussed as well, and comparative study is selected for some of the converter topologies[7].

2.3.1 Low-Frequency Transformer-Based Interface

The most common approach for BESS integration into the grid includes battery unit, which is composed of cells, modules and packs, where series and parallel combination of cells form modules and modules form packs. Such method treats battery as one unit but it causes issues due to weakest sub-unit limiting the power of the entire string. To mitigate faults in batteries, extend operational life and maximize energy usability, battery management systems (BMS) are necessary to monitor and adjust SOC and SOH of each sub-unit. In BESS applications, a grid-connected inverter utilises a transformer to step-up voltage from hundreds of volts to medium voltage of tens of kilovolts. This allows for a parallel connection of multiple batteries and inverters at low-voltage DC (LVDC) bus for large-scale systems with power ratings of tens of megawatts. For connection to the higher voltage levels such as 66kV and above, additional transformer stage might be needed. Two-level DC-AC converter might require a bulky, lossy and expensive step-up transformer for medium-voltage grid connection. Figure 2.1 shows a typical battery connection to the grid using transformer based converter. There are other converter topologies for BESS applications such as three-level netural-point clamped (NPC) converter, active NPC converter, three-level flying capacitor converter and also five-level converters being proposed. These other topologies feature more complex modulation techniques and control design as compared to traditional two-level converter, however it offers advantages in increasing output voltage magnitude, improving performance, although with a trade-off between harmonic performance, mechanical complexity and installed power [7].

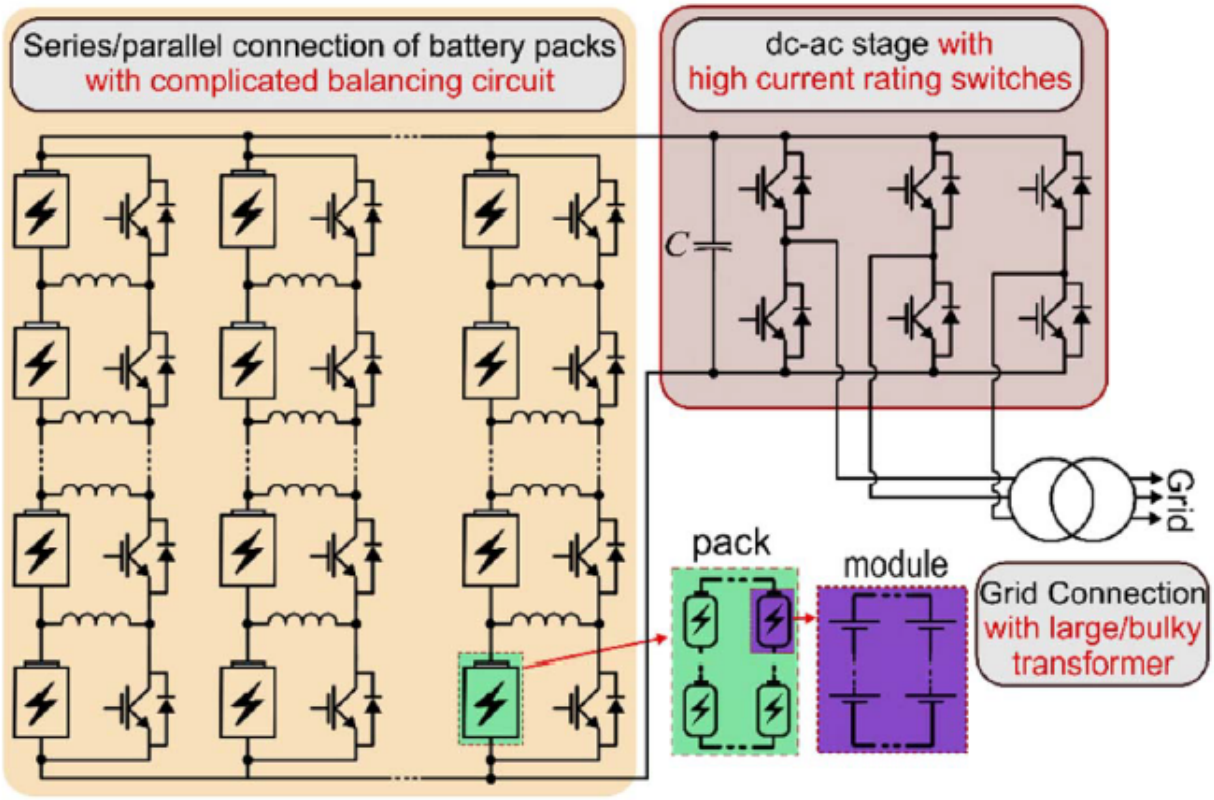

Figure 2.1: Battery unit connected to the grid through 2-level VSC and step-up transformer [7]

2.3.2 Transformerless Interface

One of the main drawbacks of line-frequency transformers is that they are bulky, lossy and costly. To avoid transformers, directly connected utility-scale BESS solutions have been developed. Series connection of semiconductors utilizes two or three level converters for medium voltage grid connections. It involves multiple power semiconductors in series due to limited voltage rating leading to design and construction challenges while at the same time requires low switching frequency to minimize losses. Another approach to achieve transformerless MV grid connection is by using series connection of submodules via modular converters. Two main types of modular converters are cascaded H-bridge converter (CHB) and modular multilevel converter (MMC). Cascaded H-bridge converter consists of multiple H-bridge cells in series per phase which allows distribution of battery modules across cells to boost LV to MV without transformers. Such topology allows power flow regulation for connected battery modules. A diagram of CHB is shown in Figure 2.2. Modular multilevel converter utilizes half-bridge submodules connected in series per phase allowing flexible utility-scale BESS integration. Such topology allows direct or distributed connection of storage elements to the MV DC-link. Centralized

battery connection requires long cables while distributed approach is more feasible for BESS applications. A diagram of MMC in centralised and distributed connections is shown in Figure 2.3. While MMC is considered to have higher complexity, cost as well as requirement for double switching device for the same voltage level as compared to CHB, MMC's integration into HVDC transmission, motor drives and grid support offers additional functions and value. [7]

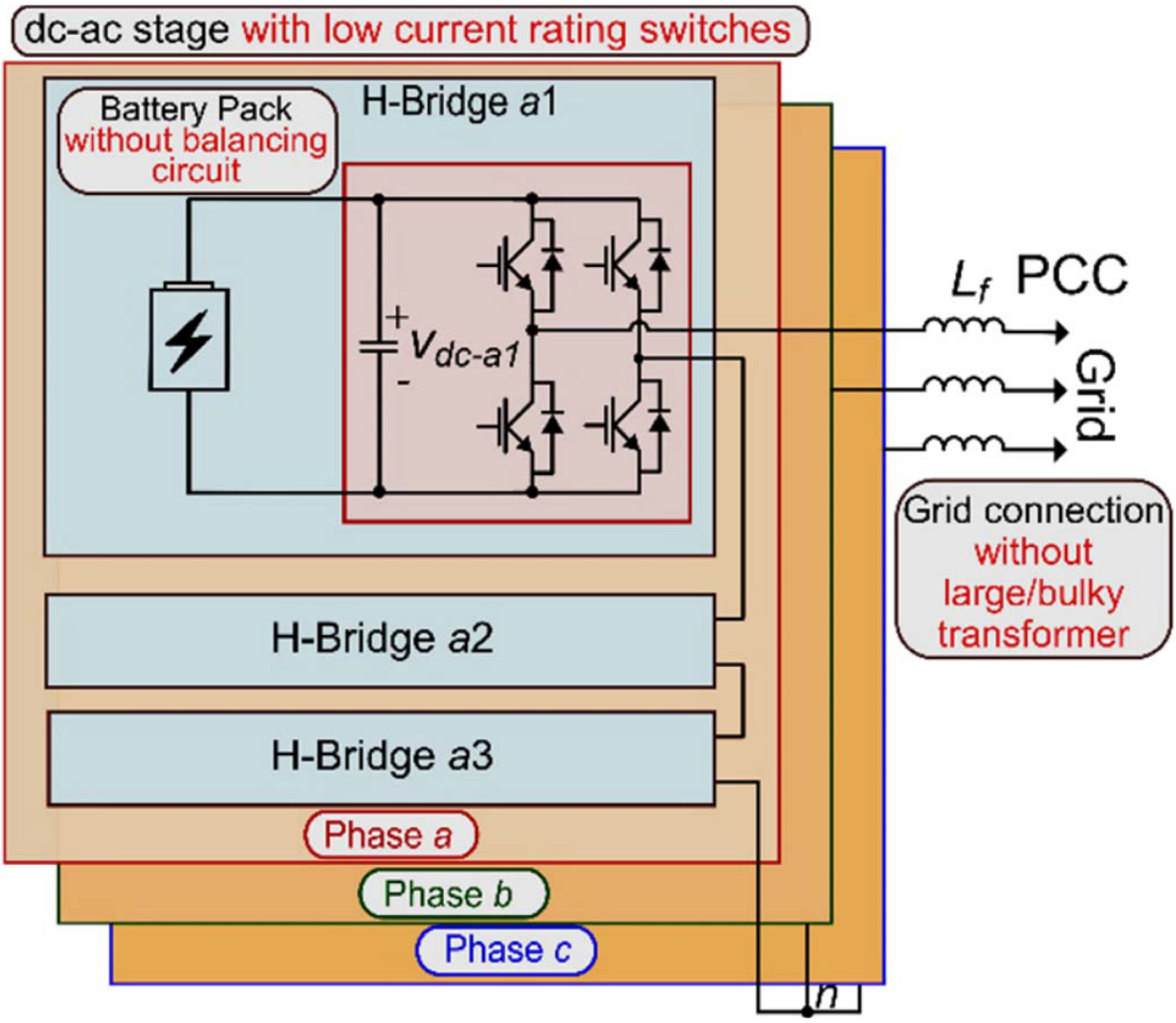

Figure 2.2: Cascaded H-bridge converter [7]

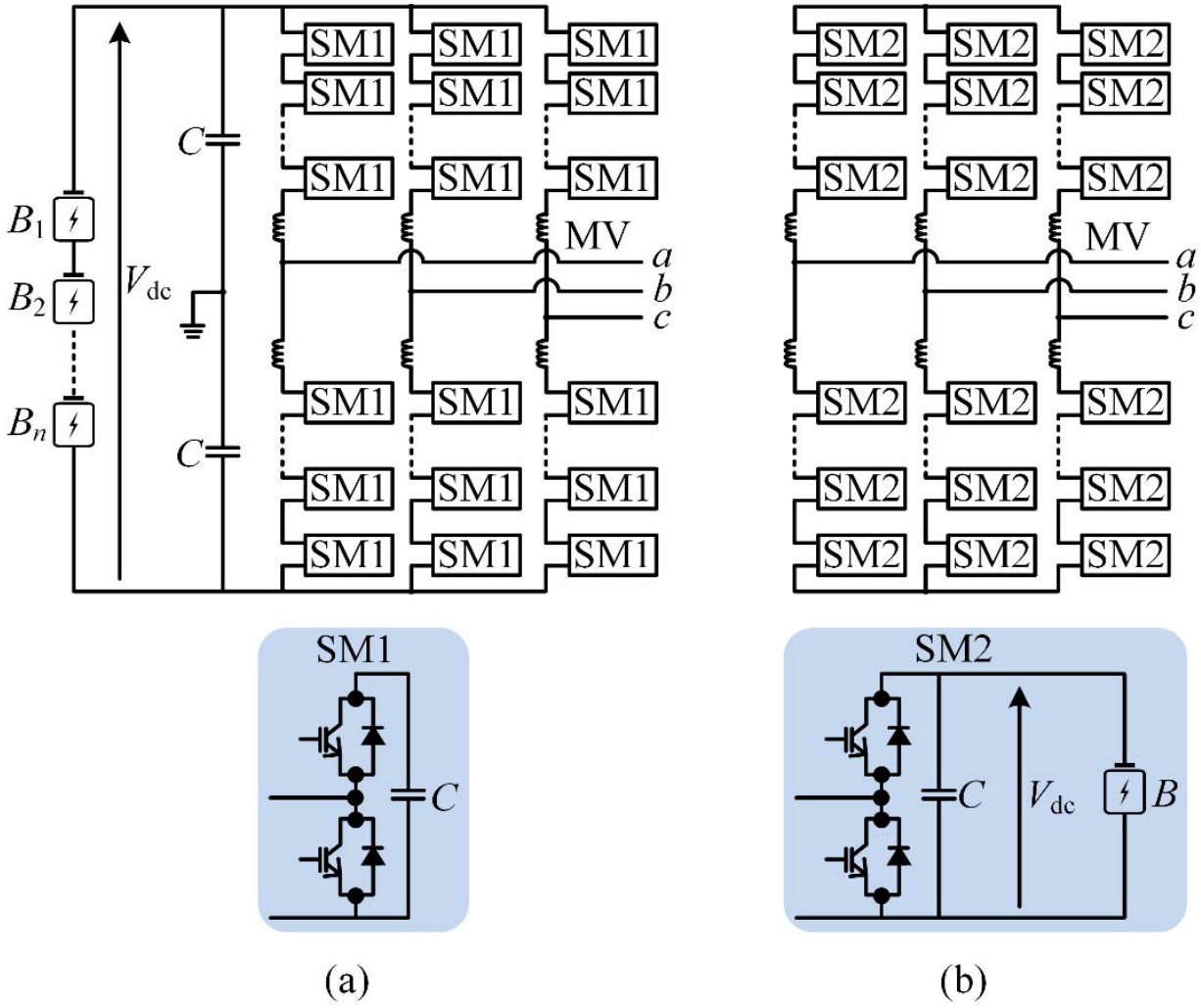

Figure 2.3: Modular multilevel converter. Diagram (a) shows centralized battery connection. Diagram (b) shows distributed battery connection [7]

2.3.3 Solid-State Transformer

Even though transformerless topologies has advantages of size and weight reduction, they lack galvanic isolation which presents safety and leakage current problems. Solid state transformers (SST) operate at higher frequencies in order to reduce core size and weight but introduces additional expenses and losses of frequency converters. There are four main SST categories, which are based on DC-link capacitor placement. Type A category is considered to be without DC decoupling capacitors, they are lightweight, low-cost but lacks reactive power support and renewable integration capability. Type B category includes LVDC capacitor for reactive power control and battery connection, however is limited in HV applications. Type C category features HVDC capacitor which

is suitable for HV applications however it poses challenges for battery integration. Finally, type D category consists of both HVDC and LVDC capacitors offering comprehensive control functions but is more complex and costly. Typically, type D is preferred for field applications due to its extensive capabilities. For the battery storage systems, focus on DC-DC section of the SST is the most important part. This DC-DC converter provides isolation and dc voltage boosting to connect a LV battery bank to the DC-link of grid connected DC-AC inverters. A diagram of different types of solid-state transformers is shown in Figure 2.4.

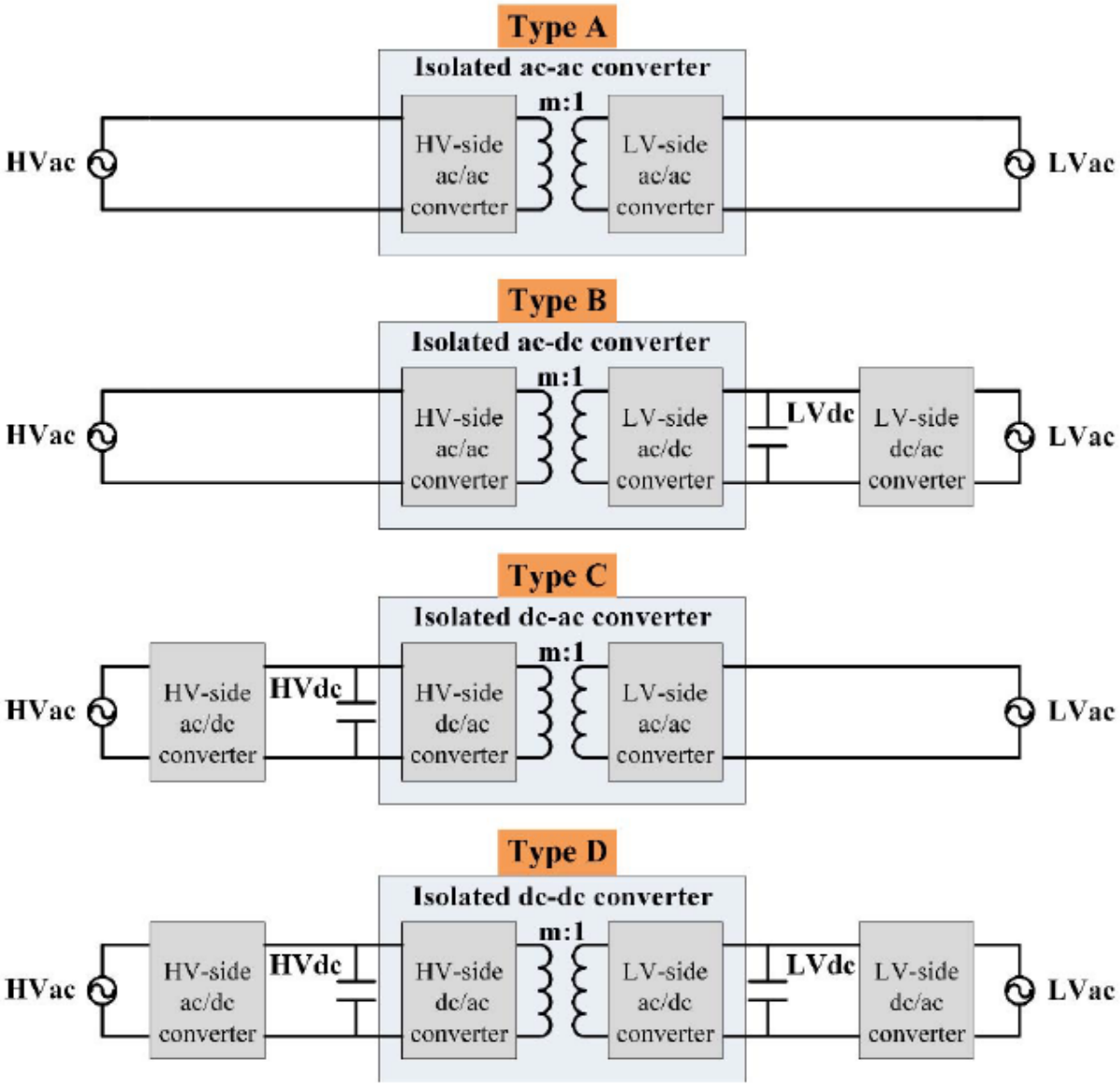

Figure 2.4: Representation of different SST types [7]

2.3.4 Converter Topologies with transformers

The most common two-level converters for DC/AC stage of BESS include voltage source converter (VSC), Z-source inverter (ZSI), and quasi-Z-source inverter (qZSI). For grid connection, they are usually deployed with low-pass filters, such as LC or LCL filters, to attenuate injected harmonic components and a transformer to step-up voltage from low voltage to medium voltage. VSC enables battery to connect either directly to the

DC/AC stage capacitor or through a DC/DC stage. However, it can only operate as buck converter, thus limiting output voltage to be lower than DC voltage. Also, it requires additional dead-time between switching of power semiconductors, which results in distorted output waveform. ZSI and qZSI have the ability to overcome the limitations of VSC by using an additional network with inductors and capacitors which enables operation in boost mode. They are preferred for integrating renewable energy sources with batteries without needing an additional DC/DC converter, thus reducing semiconductor number. However, VSC is often chosen due to its simplicity. Figure 2.5 shows a diagram of a typical connection of the battery to the grid using most common converters, filter and transformer. More advanced topologies such as NPC converter is another widely used topology for BESS, due to its increased output voltage magnitude capabilities as well as harmonic performance, thus resulting in lower filter requirements by clamping DC-bus with NPC diodes. ANPC and flying capacitor converter topologies use capacitors and additional switches for voltage clamping, thus resulting in a better capacitor voltage balancing and switching state redundancies, however at the same time increasing semiconductor count and ultimately system cost. Figure 2.6 shows a diagram of a more advanced converter topologies for battery connection to the grid. It can be seen that using more advanced topologies might result in lower filtering requirements thus passive filter is not present in the diagram. Five-level NPC converters can further enhance the output voltage waveform where in some applications, it can even eliminate the need for a transformer, allowing for a direct connection to the MV grid [7].

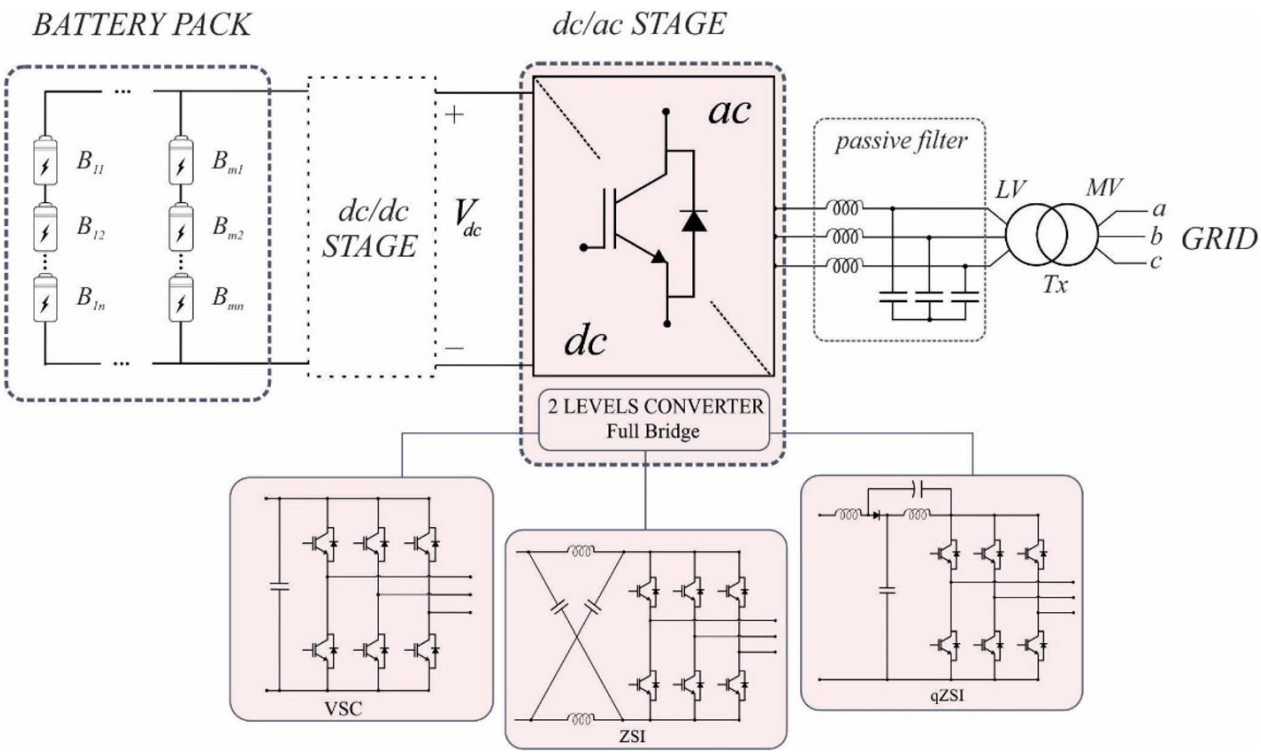

Figure 2.5: Most common converter topologies and components for battery connection to the grid using transformer [15]

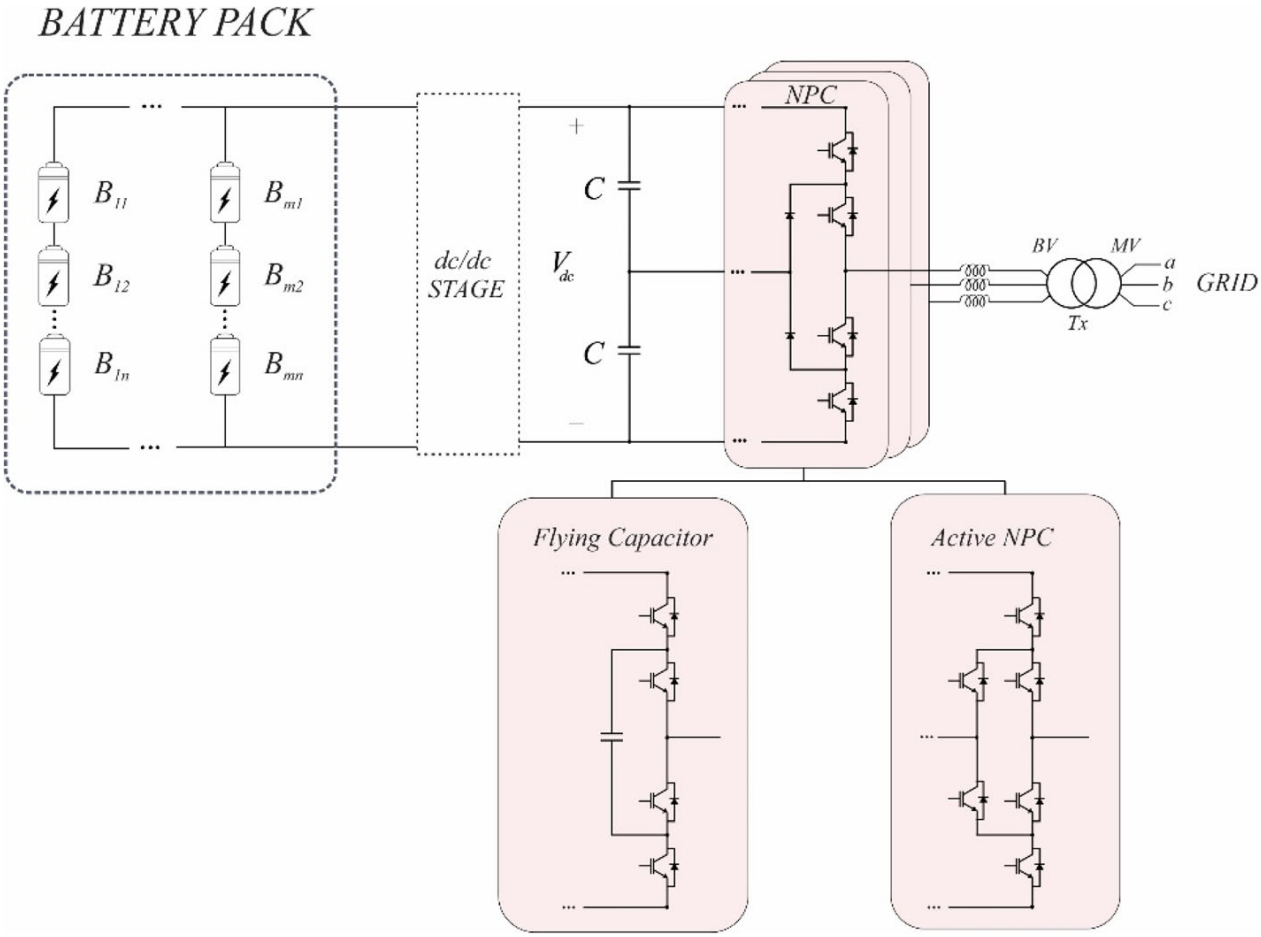

Figure 2.6: More advanced converter topologies and components for battery connection to the grid using transformer [15]

2.3.5 Transformerless Topologies

Topologies such as two-level converter can be directly connected to the MV grid by using series-connected IGBTs to block high voltages. However, this creates issues such as increased complexity in gate drive circuits for synchronization and more complex converter design with more series switches. Also, design requires low switching frequency to limit losses which results in increased filtering requirements. Figure 2.7 shows a diagram of a 2-level VSC with series connected semiconductor switches.

Multilevel topologies such as CHB and MMC are preferred in recent BESS research due to lower loses, easier SOC management, modularity and scalability. CHB are designed using series-connected single-phase H-bridge converters per phase. They can be configured in star or delta configurations. Figure 2.8 shows a diagram of a CHB converter on star and delta connections. Star configuration is less expensive while delta

configuration offers better dynamics for grid unbalances. CHB allows for a direct MV grid connection without transformers, where battery's power flow is managed using each H-bridge. CHB has advantages such as low voltage switches, modularity, fault tolerance, low frequency switching, and high quality of output voltage waveform. In star configuration, energy balancing is achieved through zero-sequence voltage whereas for delta it is achieved by using zero-sequence current.[15]

MMC is composed of series-connected single-phase copper or bridge inverter cells, which allows active power support, flexible SOC control and battery flexibility. Possible transformer for galvanic isolation may increase safety by reducing risks of metallic conduction.

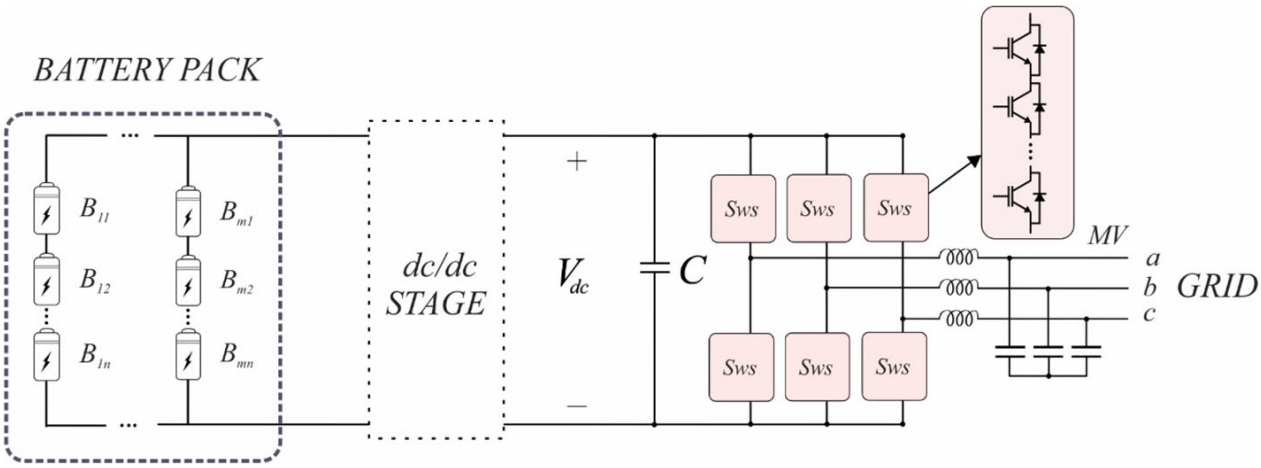

Figure 2.7: Diagram of 2-level VSC with series connected semiconductor switches [15]

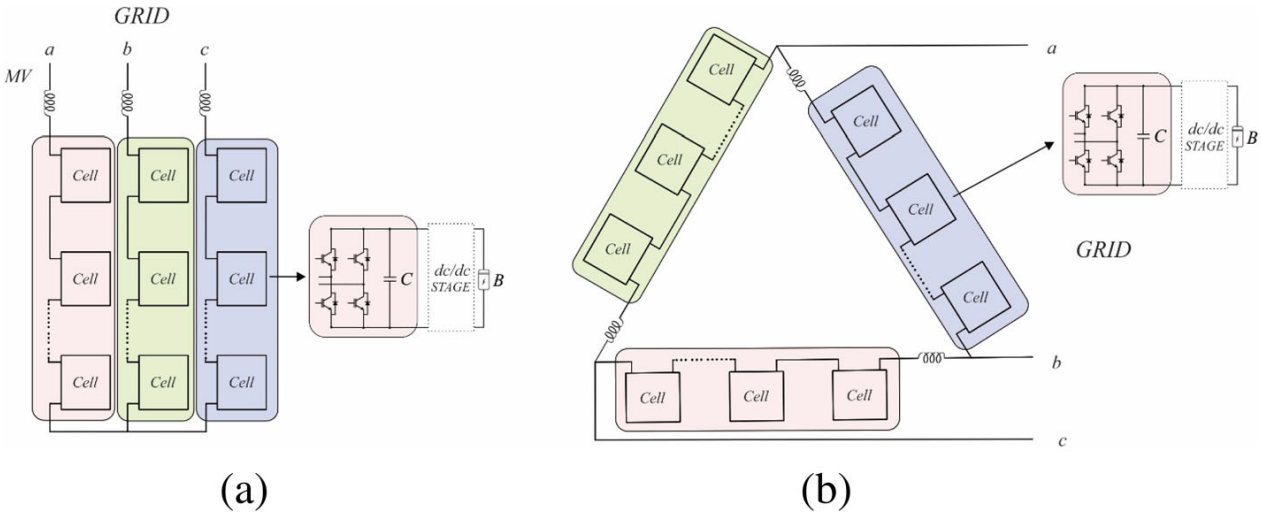

Figure 2.8: (a) CHB in star configuration, (b) CHB in delta configuration [15]

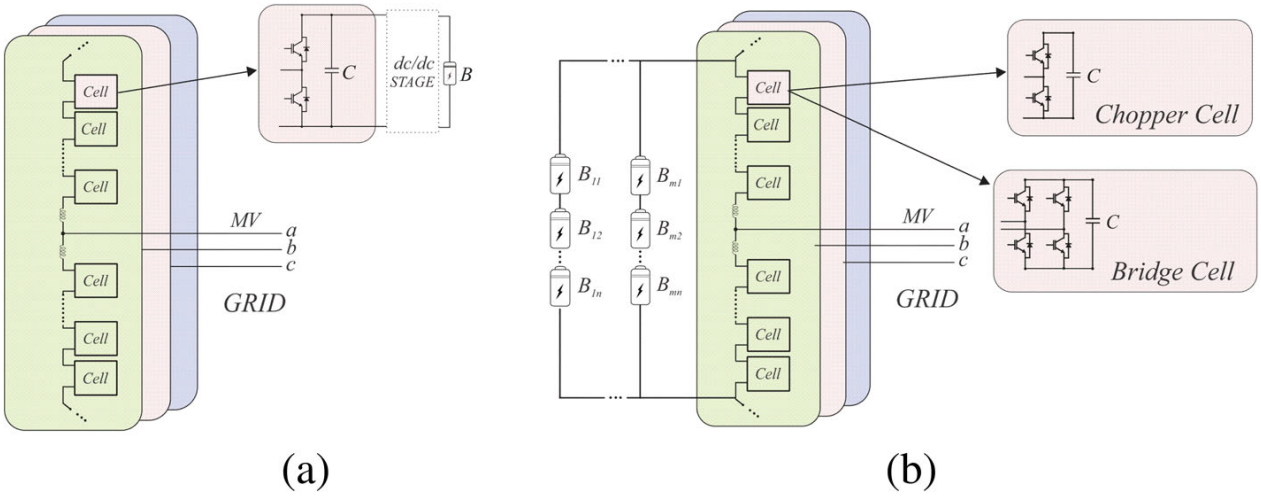

Figure 2.9: MMC with (a) dispositions of batteries in cells, (b) disposition of batteries in DC-link [15]

2.3.6 Comparison of different topologies - A Case Study [15]

Xavier et. al conducted a case study on power converter topologies applied to BESSs. The selected topologies analysed in a case study of 1 MVA BESS integration to the grid are as follows:

- Two-level Voltage Source Converter with transformer (2 L + Tx)
- Three-level Neutral-Point Clamped with transformer (3 L + Tx)
- Modular Multilevel Converter (MMC)
- MMC with insulation grid transformer (MMC + ITx)

The simulation has been performed in PLECS software with parameters defined in [15]. For two-level and three-level converters, battery packs have been configured as four 600V / 500 Ah battery packs in parallel. For MMC, battery pack has been configured as 600V / 10 Ah. In all cases, arrangement of packs are designed to meet 600V for each converter or cell and total power of 1MW. For all topologies, DC/DC stage has been omitted, all topologies are connected to 13.8kV/60Hz grid. Two-level and three-level topologies use transformer to step up from 380V to grid level, whereas MMC is directly connected to 13.8kV grid without transformer. Also, MMC with galvanic isolation transformer of ration 1:1 is included.

The results of the simulation are shown in Figures 2.10-2.12. From Figure 2.10 it can be seen that for varying power levels, MMC shows the lowest power losses whereas three-level converter with transformer shows the highest losses. Also, MMC with direct connection is more efficient than MMC with transformer due to transformer losses. Two-level with transformer shows higher efficiency than three-level with transformer above

0.4 pu of injected power but lower at minimal power levels. However, all topologies exceed 94% efficiency. Figure 2.12 demonstrates power loss distribution across different areas at nominal power. It can be seen that for two-level with transformer, significant losses are in transformer and semiconductor operation. For three-level with transformer, highest losses are identified during semiconductor conduction. Also, significant losses are noticed in transformer and inductor filter. For MMC topology, most of the losses are present in conduction and arm inductor meanwhile switching losses are insignificant. Finally, for MMC with transformer, majority of losses appear in transformer while other losses appear in conduction and arm inductor as in MMC only case. This signifies the transformer impact on the overall power efficiency of the system. Additionally, Table 2.2 shows comparison of the selected topologies in terms of total harmonic distortion (THD), DC-link capacitor and inductor energy storage requirements, different component counts as well as fault tolerance capabilities. From the table it can be seen that MMC has the best THD performance whereas three-level with transformer has the worst performance. However, in all topologies THD is below 5% which is often used as reference for THD limits for grid connected systems. Energy storage in passive components affects converter volume and cost, with MMC needing higher capacitor energy storage but less inductor energy compared to 2 L and 3 L. In terms of the component count, number of semiconductors is significantly smaller for both two-level and three-level converters as compared to MMC. The number of current sensors for two-level and three-level converters is 3, where one sensor is placed for each phase. Furthermore, 4 voltage sensors are required, where 1 is used to measure DC-link voltage and 3 to measure the AC line voltages. The current sensors for MMC are also used to measure arm currents of each phase thus resulting in twice as many current sensors as compared to the two-level and three-level topologies. Number of voltage sensors for MMC is the same as for other two presented topologies. Finally, it has been noted that two-level and three-level converter topologies do not have fault tolerance capabilities whereas MMC has due to its modular nature of submodules.

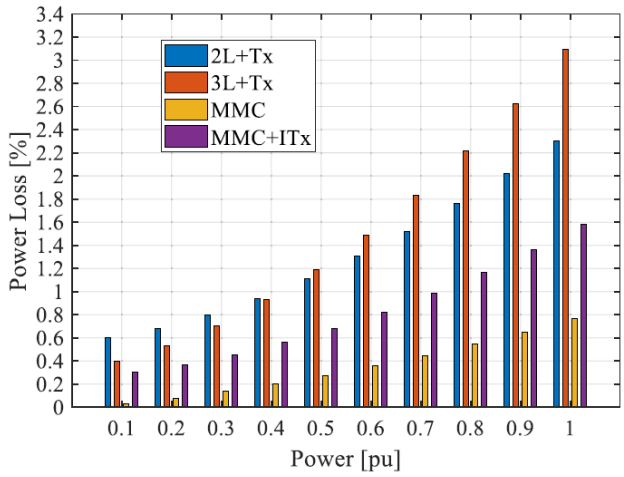

Figure 2.10: Comparison of power losses for each converter topology at different power levels [15]

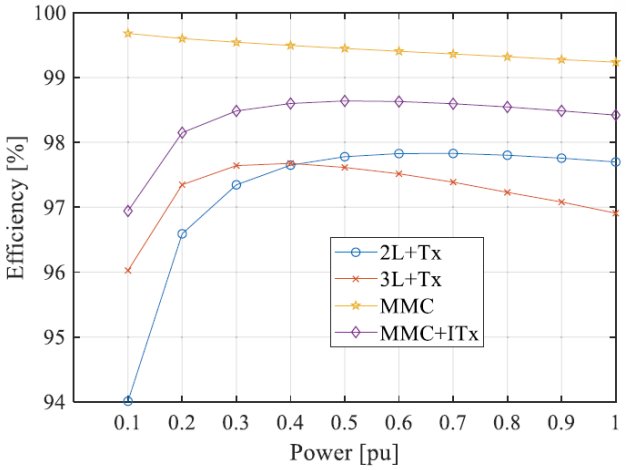

Figure 2.11: Efficiency for each converter topology at different power levels [15]

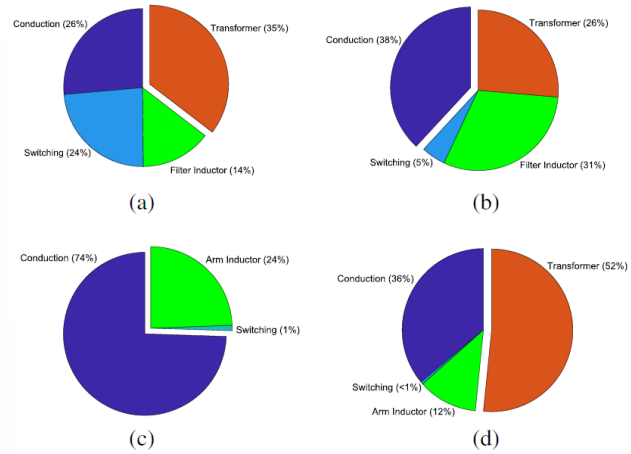

Figure 2.12: Detailing of losses between conduction, switching, inductor and transformer at nominal power (1 pu) (a) 2 L+Tx, (b) 3 L+Tx, (c) MMC, (d) MMC +ITx [15]

Table 2.2: Comparison of 2 L + Tx, 3 L + Tx, MMC and MMC + ITx [15]

Comparison	2 L + Tx	3 L + Tx	MMC	MMC + ITx
Efficiency at rated power (%)	97.70	96.91	99.23	98.42
THD at rated power (%)	2.52	3.48	0.87	0.87
Capacitor Energy Storage (J)	4000	4000	40,000	40,000
Inductor Energy Storage (J)	360	1050	45.5	45.5
Number of IGBTs	6	12	432	432
Number of Diodes	6	18	432	432
Number of Control Loops	3	3	12	12
Number of Current Sensors	3	3	6	6
Number of Voltage Sensors	4	4	4	4
Fault Tolerance	No	No	Yes	Yes

2.4 Grid Requirements and Standards

2.4.1 BESS Grid Codes and Standards

Regulatory frameworks impose few types of requirements for grid-connected inverters to aid the electrical grid during emergencies and transient processes. Primarily, these standards focus on ensuring that inverters contribute effectively to grid stability through two critical support mechanisms: frequency and voltage regulation [7].

Voltage Support

To maintain grid voltage stability at the Point of Common Coupling (PCC), regulations require that BESS inverters either inject or absorb reactive power, contingent upon the prevailing grid voltage conditions. There are a variety of different standards that have different volt-VAR [Q(V)] requirements, these standards being: AS 4777.2, TOR R4, IEEE 1547, VDE 4105, CEI 0-21, TR 3.2.2. Based on these standards, it is evident that when the voltage at the PCC falls below the nominal range, the BESS must inject some amount of reactive power into the grid, to assist in elevating the PCC voltage. If the voltage exceeds the nominal range, the inverter must absorb a certain quantity of reactive power, to facilitate the reduction of voltage at the PCC. Different standards, provide significant variation in dead band parameters. Some standards, such as TR 3.2.2 and IEEE 1547 category A, have no dead band, requiring frequent inverter response. Others have larger dead bands, limiting response activation. VDE 4105 and IEEE 1547 category B feature narrow dead bands for easier activation but demand significant reactive power capability from inverters [7].

Frequency Support

BESS inverters play a crucial role in maintaining grid frequency stability during disturbances, with various standards delineating specific actions in response to frequency alterations. Initially, upon detecting a drop in frequency, inverters are programmed to halt charging operations. Should the frequency decrease beyond a predefined threshold, the inverters then begin to inject active power into the grid, guided by a droop curve, that is different for different standards. This curve dictates the rate at which power is added in relation to the frequency drop, ensuring a balanced response to the disturbance. In scenarios where the frequency continues to fall, inverters augment their output to reach nominal power levels, maintaining this output until the frequency returns to a stable state. This operational strategy is critical in mitigating the impact of frequency dips and aiding in the fast recovery of the grid's equilibrium. Measures to prevent potential instability post-recovery are implemented. A specified hysteresis period is employed post-frequency normalization. During this interval, inverters continue to deliver maximum power output before gradually reverting to standard operational modes. This delay ensures the grid's stability is firmly re-established before any reduction in support occurs. Moreover, during the transition back to normalcy, inverters are required to adhere to a designated power ramp rate. This requirement ensures a smooth and controlled adjustment from maximum output back to regular charging or operational states, thereby minimizing any risk of re-instigating instability within the grid [7].

2.4.2 Regulatory Framework of SLBs

As of currently, a significant problem regarding the industrial application of SLBs is the lack of any up-to-date regulations of SLBs [12]. Currently, the most applicable directive for batteries is EU Directive 2006/66/EC. As of December 2020, EU Commission has released a proposal, which provides improvements over the definitions and management standards of EVs. The proposal includes the specifications on the required documentation to prove proper management of the battery lifecycle. Another point stated in the proposal is the introduction of "battery passports". The passport should detail the types of degradation the battery experienced in its initial usage and evaluate its SOH for potential second-life uses. Additionally, the passport needs to be refreshed with updated parameters each time the battery undergoes repair or repurposing. This introduction of the "battery passport" would essentially mean that the standards related to first-life batteries would be applicable to second-life batteries. Batteries are classified under UN Category 9 as dangerous goods, as subjected under certain uncontrolled environmental conditions or mishandled during transportation, they are thermally and electrically unstable. Present in the UN 38.3 there are specific test procedures that are used for Li cells and batteries. SLBs are required to go through Test T.1-T.7, which includes altitude simulation tests, rapid thermal cycling and storage at low temperature, vibration, shock and external short circuits, and overcharging. Currently, the only norm that provides the definition on the amount of testing required for SLBs to be installed in new products is the UL 1974 [16]. However, the aforementioned standard does not include the definition of suitable SOH and Remaining Useful Life (RUL) estimation methods. A more general standard regarding SLBs is the IEC 63330 [17], which includes templates for data on repurposing products, but lacks the details about practical procedures. Another standard, the IEC 62660 [18] offers reference electrical tests for batteries, although not specifically designed to be for SLBs. The EU Directive proposal aims to address and overcome barriers that limit the interoperability between FLBs and SLBs. While the proposal attempts to address these challenges, significant issues remain. These include the transferability of Extended Producer Responsibility (EPR) and the eco-design of FLBs.

2.5 Conclusion

Integration of RES is critical for a more sustainable energy generation, however it comes with the challenge of balancing electricity generation and consumption due to the inherent variability. To address some of the issues, grid support applications, such as peak shaving, voltage and frequency regulation and energy arbitrage are available, mainly facilitated by ESS. There are a number of different ESS technologies: mechanical, thermal, electrical, chemical and electrochemical storage, each offering unique advantages and disadvantages. The repurposing of SLBs could present a cost-effective and environmentally sustainable option for grid stability, addressing battery waste management challenges.

For the integration of the ESS into the grid, power converters are used. A comparative study of various converter topologies is conducted, looking at 2 L + Tx, 3 L + Tx, MMC and MMC + ITx. Analyzing the results, MMC gives the best efficiency, THD and fault tolerant capabilities, although being more complex in design and control. Lastly, the regulatory frameworks for BESS integration to grid and SLBs have been examined. These are essential for ensuring effective contribution of energy storage solutions to grid stability.

Chapter 3

Task Statement

Scope of Project

The aim of this project is to design, model, and analyze an MMC system integrated with first-life battery storage, focusing on its application in grid support. The goal is to establish a foundational simulation environment that captures the intricate dynamics of MMCs and battery interactions, paving the way for future exploration into incorporating SLBs for sustainable grid solutions. The project will cover the development of the models and control strategies with the grid support functionalities in the simulated environments of MATLAB/Simulink and PLECS.

Objectives

1. Literature Review and Gap Analysis:
    - Conduct a comprehensive review of existing MMC technologies with battery connected systems, battery modelling, different control layers as well as different control methods used for each layer.
    - Identify research gaps in the integration of MMCs with battery storage for grid support applications.
2. Real-life application analysis
    - Define the project requirements in terms of applications (may need further research of MMC+Bat applications)
    - Define power requirements, grid requirements (select specific point of grid (i.e. somewhere in Denmark with known grid voltages, supply/demand quantities, required support requirements (based on regulations))
3. System Design and Modeling:

- Conduct a literature review on modelling and integration of MMC and battery systems.
- Determine the sizing of the components.
- Design a detailed model of an MMC integrated with first-life battery storage, focusing on distributed battery connection to each submodule.
- Design a model of battery module using electrical equivalent circuit (EEC) method.
- This includes simulation of electrical equivalent models as well as linear or non-linear models in different formulations.
- Validate developed linear or non-linear models in different formulations with the simulation of EEC model.

4. Control System Development:

   - Conduct a literature review on control of MMC and battery storage connected systems.
   - Design and simulate control layers associated to MMC and batteries.
   - Develop control strategies for battery charge/discharge management within the MMC.

5. Grid Support Analysis:

   - Conduct a literature review on control for specific grid support functionalities.
   - Determine grid support control algorithms and active/reactive power requirements.
   - Analyze the capability of the MMC integrated with battery storage in providing grid support, focusing on some selected grid support functionalities.
   - Focus on the development of control algorithms for grid support functionalities such as voltage regulation, frequency stabilization, and peak shaving.

Delimitations

Following aspects of the proposed problem will not be analysed in this project due to the limited scope and time constraints. Following aspects should be considered as a future work based on the work done in this report:

- Detailed modeling and analysis of SLBs integration into MMCs, focusing on aging and deterioration impacts.

- Expansion of the simulation model to include diverse grid support functionalities and broader application scenarios.
- Policy and regulatory analysis for the integration of SLBs in grid support systems, addressing standards and compliance issues.
- Perform a cost comparison between first-life and potential second-life battery integration within the MMC system for specified grid support applications.
- Evaluate the economic viability and potential savings associated with SLBs integration.

Chapter 4

Modeling

In this chapter, we first present an in-depth explanation and modeling of the MMC. Subsequently, we detail the individual design and modeling of the submodule's components. The submodule consists of a half-bridge on the MMC side and a bidirectional DC-DC converter that interfaces a battery pack with the MMC side. Finally, we describe the modeling of the battery pack using a second-order Thevenin model. Additionally, parameter identification process for the battery is conducted, taking into account the degradation of internal resistance, RC network parameters, and capacity.

4.1 Modeling of MMC

A Modular Multilevel Converter (MMC) is a type of power converter that is especially suited for high-voltage and high-power applications, such as HVDC power transmission and medium-to-high voltage motor drives. MMCs are favored for their modularity, scalability, and efficiency. In this section, the an explanation of the MMC functions, structure and operation will be presented.

4.1.1 Structure of MMC

MMC is comprised of several main components. At the core of the converter are submodules which create a voltage across its terminals equal to that of the fraction of DC voltage. The fraction of DC voltage on the terminals of the submodule will be proportional to the number of submodules connected in series. Series combination of submodules are switched in specific patterns to synthesize and generate output waveform. Generally, MMC consists of 3 phases, also called legs, and each leg has upper and lower arms. Each arm consists of series connected submodules and inductor. The main purpose of inductor for each arm is to limit current rate and suppress some of the other currents apparent in the converter. Such configuration gives total of 6 strings of submodules which are related to phases a, b, c each with upper and lower arms [19].

Submodules

The core component of MMC are submodules which enables MMC to become modular. A submodule is a simple DC-AC power conversion circuit consisting of IGBTs and DC capacitors. There exists a variety of different configurations of submodules. Some of the different submodule configurations are listed in the Table 4.1. The table shows different characteristics for half-bridge, full-bridge, flying-capacitor, cascaded half-bridge as well as double clamp submodule configurations. The simplest of them all is half-bridge configuration. It consists of 2 semiconductor power switches and a capacitor [20, 21].

Table 4.1: Comparison of MMC submodules [21]

Performance Index	**HB-SM**	**FB-SM**	**FC-SM**	**CH-SM**	**CD-SM**
No. of output voltage levels	2	3	3	3	4
Max. blocking voltage of SM	v_C	v_C	$2v_C$	$2v_C$	$2v_C$
Max. No. of DC capacitors normalized to v_C	1	1	3	2	2
No. of devices normalized to v_C	2	4	4	4	7
Max. No. of devices in conduction path	1	2	2	2	3
Power losses	Low	Moderate	Moderate	Moderate	High
Bipolar operation	No	Yes	No	No	Yes
SM design complexity	Low	Low	High	Low	High
SM control complexity	Low	Low	High	Low	Low
DC fault blocking	No	Yes	No	No	Yes

Simple circuit equivalent of half-bridge submodule is shown in Figure 4.1.

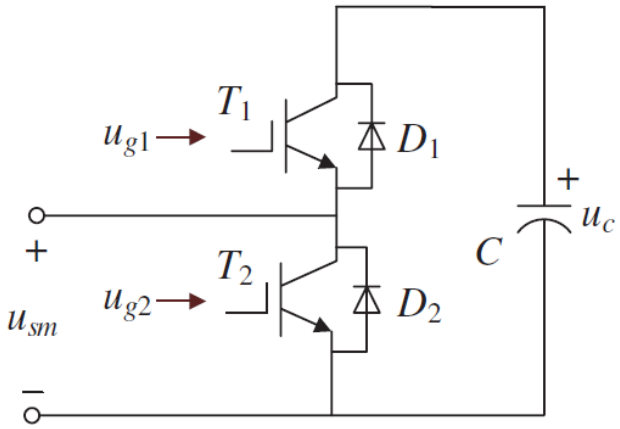

Figure 4.1: Example half-bridge submodule configuration

The output of the submodule u_{sm} is determined by the activation of upper and lower switches of the half-bridge. The submodule output voltage can either be equal to the

capacitors voltage or zero. In other words, submodule can be inserted or bypassed depending on the activation of half-bridge switches. Additionally, depending on the current direcionality, the capacitor will get charged or discharged thus its voltage varies depending on the current direction. In HB-SM configuration, switches are turned in complementary logic. If u_{g1} is turned on, then u_{g2} will be in off state. In such way, when u_{g1} is in conduction mode, the submodule will be inserted, and when u_{g1} is in off mode, then u_{g2} conducts and capacitor is bypassed. Using this assumption, submodule voltage can by synthesized as[22]:

$$u_{sm} = S \cdot u_c \tag{4.1}$$

where S can be either 1 or 0 which refers to capacitor being inserted or bypassed. Considering direction of the current and states of S, there can be 4 total operation modes.

$$S = \begin{cases} 1, & \text{if } u_{g_1} \text{ is high-level and } u_{g_2} \text{ is low-level} \\ 0, & \text{if } u_{g_1} \text{ is low-level and } u_{g_2} \text{ is high-level} \end{cases} \tag{4.2}$$

Mode	S	i_{arm}	**Circuit state**	**SM state**	T_1	T_2	u_{sm}	C	u_c
1	1	> 0	Inserted	On	On	Off	u_c	Charged	Increased
2	1	< 0	Inserted	On	On	Off	u_c	Discharged	Reduced
3	0	> 0	Bypassed	Off	Off	On	0	Bypassed	Unchanged
4	0	< 0	Bypassed	Off	Off	On	0	Bypassed	Unchanged

Table 4.2: Modes of operation for a submodule in a MMC [21]

Mode 1 (normal operation): When $S = 1$ and $i_{arm} > 0$, the T_1 is turned on, the T_2 is turned off, the SM is inserted into the arm circuit, the SM state is on, and the SM output voltage u_{sm} is equal to the SM capacitor voltage u_c. In this case, the SM capacitor C is charged by i_{arm}, and the capacitor voltage u_c is increased.

Mode 2 (normal operation): When $S = 1$ and $i_{arm} < 0$, the T_1 is turned on, the T_2 is turned off, the SM is inserted into the arm circuit, the SM state is on, and the SM output voltage u_{sm} is equal to the SM capacitor voltage u_c. In this case, the SM capacitor C is discharged by i_{arm}, and the capacitor voltage u_c is reduced.

Mode 3 (normal operation): When $S = 0$ and $i_{arm} > 0$, the T_1 is turned off, the T_2 is turned on, the SM is bypassed from the arm circuit, the SM state is off, and the SM output voltage u_{sm} is equal to 0. In this case, the SM capacitor C is bypassed, and the capacitor voltage u_c is unchanged.

Mode 4 (normal operation): When $S = 0$ and $i_{arm} < 0$, the T_1 is turned off, the T_2 is turned on, the SM is bypassed from the arm circuit, the SM state is off, and the SM output voltage u_{sm} is equal to 0. In this case, the SM capacitor C is bypassed, and the capacitor voltage u_c is unchanged.

Once submodule is configured and operation of switches is defined, individual HB-SMs can be connected in series to form strings of submodules. Forming SMs into strings and adjusting their turn-on/turn-off times allows to synthesize multiple voltage levels required to generate signals such as 3-phase AC waveforms.

4.1.2 Voltage Addition

So far we have defined that each SM can generate voltage either zero or equal to its capacitor voltage. Capacitor voltage is determined by the number of the submodules per arm as well as DC link voltage. Each leg is connected in parallel to the DC link which means that voltage across each leg will be equal to the DC link. However, DC link is often split in 2 which creates a floating point and gives $V_{dc}/2$ for upper and for lower arms. Thereby, in ideal conditions voltage across the capacitors for all submodules in the same arm should be:

$$V_{sm} = V_{dc}/N \tag{4.3}$$

If capacitor voltages in the submodules of arms are balanced, then activating series sub-modules would result in addition of the capacitor voltages thereby synthesizing a voltage output equal to the number of active submodules. Figure 4.2 shows an example of stepped voltage synthesis using 4 submodules in series.

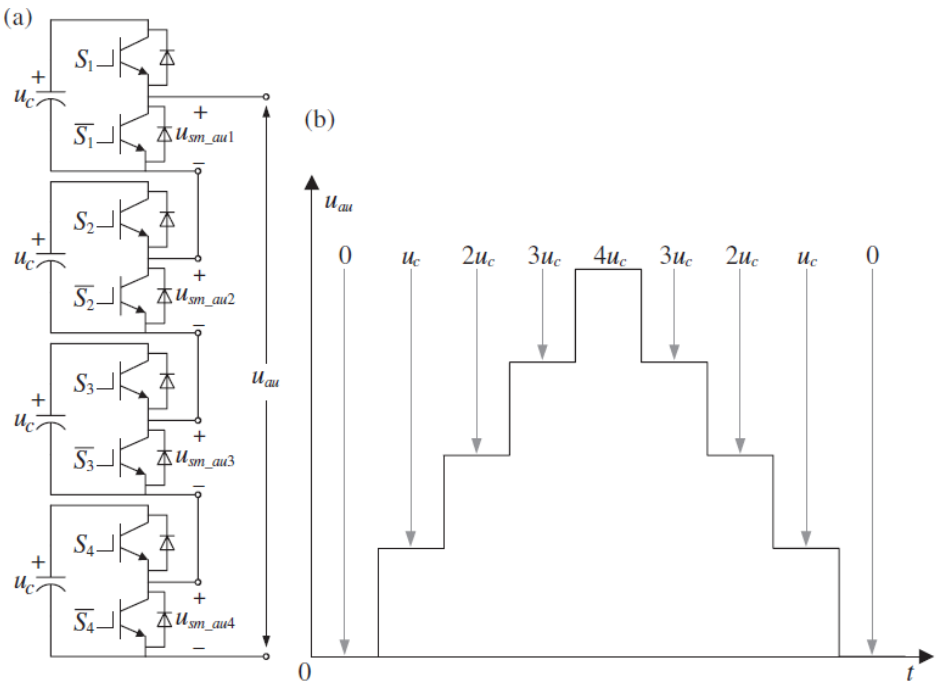

Figure 4.2: Stepped Voltage Synthesis [21]

It can be seen that by adjusting the active time of the submodules, a waveform similar to a sine wave can be synthesized [21]. This simple relation gives rise for a definition of arm voltage as:

$$u_{xy} = \sum_{i=1}^{N} u_{sm\_xyi} = \sum_{i=1}^{N} \left(S_{xyi} \cdot u_c \right) = n_{on} \cdot u_c \tag{4.4}$$

$$n_{on} = \sum_{i=1}^{N} S_{xyi} \tag{4.5}$$

where x - phases a,b,c; y - upper and lower arms; N - number of modules per arm.

To ensure that voltage across the submodules in both arms equals DC link voltage, upper and lower arms must work in a complementary manner. For this reason, N number of switches will be active at all times per leg in total.

$$V_{dc} = \sum_{i=1}^{n} S_{xui} V_{sm} + \sum_{i=1}^{m} S_{xli} V_{sm} \tag{4.6}$$

where n - number of active SMs in upper arm; m - number of active SMs in lower arm.

To synthesize sinusoidal waveform, submodules are being switched on and off during specific time triggers which are defined using modulators. There are numerous modulators capable of driving multilevel converters, each with its own advantages and disadvantages. Use of modulator allows to translate desired reference voltage on the output terminals of the converter into logic signals to turn different switches on/off for specific periods of time that are computed by modulators. More about modulators will be presented in the upcoming sections. However, before discussion about modulation, it is important to understand and define dynamic parameters of the system, thus following is analysis on component selection for MMC.

4.1.3 Component Selection

Power Device Voltage Rating

Each submodule consists of 2 power devices. During conduction mode, power devices experience voltage stress. For HB-SMs, voltage stress across power devices is shown in Table 4.3. It can be seen that the maximum voltage stress power devices experience are up to the voltage of the capacitor voltage u_c. Considering that for safe operation power devices should have some margins around operating point, it is suggested to choose power devices that can handle 1.5-2 times capacitor voltage u_c. Therefore, if capacitors are selected to operate at 1kV, power switches should be able to handle up to 2kV of voltage across them [23].

					Power device voltage stress			
Mode	S	i_{arm}	T_1	T_2	u_{T_1}	u_{D_1}	u_{T_2}	u_{D_2}
1	1	> 0	On	Off	0	0	u_c	u_c
2	1	< 0	On	Off	0	0	u_c	u_c
3	0	> 0	Off	On	u_c	u_c	0	0
4	0	< 0	Off	On	u_c	u_c	0	0

Table 4.3: Power device voltage stress in different operation modes of MMC [23]

Power Device Current Rating

Under normal operation conditions, power devices experience current flowing through them. Current running through all power devices in the same arm will be the same because of series connected SMs. For this reason, the current that flows through power devices is equal to arm current. A summary of the current stress levels for power devices is shown in Table 4.4. It can be seen that the current stress is equal to arm current for all power devices during different conduction modes [23].

					Power device current stress			
Mode	S	i_{arm}	T_1	T_2	i_{T_1}	i_{D_1}	i_{T_2}	i_{D_2}
1	1	> 0	On	Off	0	i_{arm}	0	0
2	1	< 0	On	Off	i_{arm}	0	0	0
3	0	> 0	Off	On	0	0	i_{arm}	0
4	0	< 0	Off	On	0	0	0	i_{arm}

Table 4.4: Power device voltage stress in different operation modes of MMC [23]

By taking one fundamental cycle of arm current, two cycles can be determined. One cycle refers to period when T_2 or D_1 is conducting and the other period is when T_1 or D_2 is conducting. By taking root mean square (RMS) values of current for those specific periods, we can determine the current stresses components will experience.

Figure 4.3 shows upper arm current of phase a during one fundamental cycle.

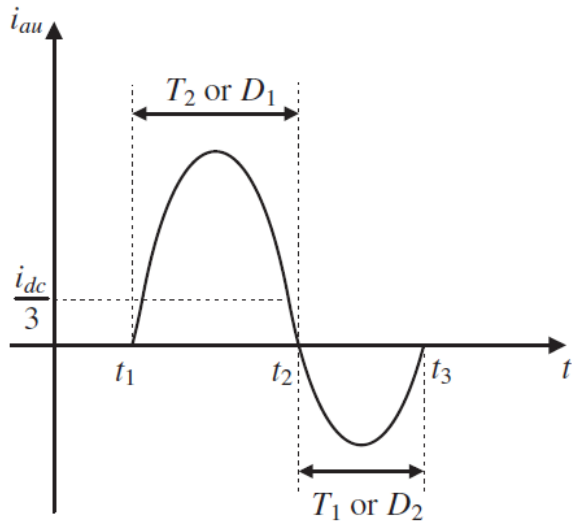

Figure 4.3: Arm Current Waveform [23]

From this information, it is possible to derive RMS currents for components as follows:

$$I_{rms\_T_1} = \sqrt{\frac{1}{T_f}\int_{t_2}^{t_3} S_{aui}^2 i_{au}^2 \, dt} \tag{4.7}$$

$$I_{rms\_T_2} = \sqrt{\frac{1}{T_f}\int_{t_1}^{t_2} (1 - S_{aui})^2 i_{au}^2 \, dt} \tag{4.8}$$

$$I_{rms\_D_1} = \sqrt{\frac{1}{T_f}\int_{t_1}^{t_2} S_{aui}^2 i_{au}^2 \, dt} \tag{4.9}$$

$$I_{rms\_D_2} = \sqrt{\frac{1}{T_f}\int_{t_2}^{t_3} (1 - S_{aui})^2 i_{au}^2 \, dt} \tag{4.10}$$

Since current rating must have margins, it is suggested to select 1.5-2 times of RMS current flowing through power devices.

Capacitor Rating

Capacitor voltage contains DC component and fluctuation component under normal operating conditions [23]. SMs capacitor voltage can be expressed as:

$$u_c = U_c + \Delta u_c \tag{4.11}$$

Where $U_c = \frac{V_{dc}}{N}$ and Δu_c is fluctuation component. The fluctuation ratio of capacitor voltage can be expressed as:

$$\varepsilon = \frac{max|\Delta u_c|}{U_c} \tag{4.12}$$

During fluctuation of voltage, energy in the arm and submodules is also fluctuating. This fluctuation must be balanced through one fundamental cycle of instantaneous power of arm. Assuming arm energy reaches its minimum and maximum at t_1 and t_2 respectively, the largest change of capacitor energy ΔQ_{max} during one fundamental cycle T_f can be obtained as [23]:

$$\Delta Q_{\max} = Q_{\max} - Q_{\min} = \frac{1}{n}\int_{t_1}^{t_2} |p_{au}|\, dt = \frac{2S_N}{3mn\omega}\left[1 - \left(\frac{m\cos\theta}{2}\right)^2\right]^{3/2} \tag{4.13}$$

where ΔQ_{min} and ΔQ_{max} are the minimum and maximum capacitor energy respectively; S_N is rated apparent power of the MMC and m is modulation index. Furthermore, maximum and minimum capacitor energy of SM: Q_{max} and Q_{min} can be expressed as[23]:

$$\begin{cases} Q_{\max} = \dfrac{1}{2}C\left[U_c \cdot (1+\varepsilon)\right]^2 \\ Q_{\min} = \dfrac{1}{2}C\left[U_c \cdot (1-\varepsilon)\right]^2 \end{cases} \tag{4.14}$$

Furthermore, following expression for fluctuation ratio of capacitor voltage is derived [23]:

$$\varepsilon = \frac{1}{3mn\omega C U_c^2} S_N \left[1 - \left(\frac{m\cos\theta}{2}\right)^2\right]^{3/2} \tag{4.15}$$

One of the considerations when selecting SM's capacitance is to ensure that ratio of capacitor fluctuation ϵ is less than maximum allowed voltage fluctuation ϵ_{max} which is normally selected within 5% to 10%. If $\cos\theta = 1$, and $m = 1$, then ϵ reaches its maximum as [23]:

$$\varepsilon_{max} = \frac{1}{3} \cdot \frac{S_N}{n\omega C U_c^2} \tag{4.16}$$

Finally, capacitor of SM can be sized according to the following expression [23]:

$$C \geq \frac{1}{3} \cdot \frac{S_N}{n\omega U_c^2 \varepsilon_{max}} \tag{4.17}$$

Arm Inductor Rating

The sizing of the arm inductor in the operation of MMC is related to a several crucial roles: current limiting, arm current ripple filtering, balancing of the currents shared between submodules, energy storage and many more. A distinctive function of arm inductor in MMC is limiting of the DC-side short-circuit fault current rise rate. DC-side mathematical model of MMC can be expressed as [23]:

$$u_{ju} + u_{jl} + \left(L_s \frac{di_{ju}}{dt} + L_s \frac{di_{jl}}{dt} \right) = 0 \tag{4.18}$$

where $\frac{di_{ju}}{dt}$ and $\frac{di_{jl}}{dt}$ are upper and lower arm fault current rise rates in phase j. The upper and lower arm currents are supposed to be equal, because after a short period of the fault, most of the arm current is the transient component, thus [23]:

$$i_{ju} = i_{jl} \tag{4.19}$$

Therefore, $\frac{di_{ju}}{dt}$ and $\frac{di_{jl}}{dt}$ are supposed to be equal as:

$$\frac{di_{ju}}{dt} = \frac{di_{jl}}{dt} = \lambda \tag{4.20}$$

Using Equations 4.18, 4.19 and 4.20, fault current rise rate λ can be derived as [23]:

$$\lambda = \frac{V_{dc}}{2L_s} \tag{4.21}$$

Finally, to limit DC-side short-circuit fault current rise rate, arm inductor L_s can be chosen as [23]:

$$L_s \geq \frac{V_{dc}}{2\lambda_{max}} \tag{4.22}$$

where λ_{max} is maximum allowed fault current rise rate.

4.1.4 Dynamic Modelling of MMC

Modelling and analysis of dynamic behaviour of MMCs is a crucial step, especially when it comes to control design. MMCs are composed of numerous different components thus it contains various dynamics. The two major dynamic aspects that must be addressed are converter output voltage and current dynamics as well as circulating current dynamics which appear due to imbalances between phases, arms and submodules.

Figure 4.4 shows a schematic diagram of MMC consisting of three phase legs, one for each phase of the three-phase AC system.

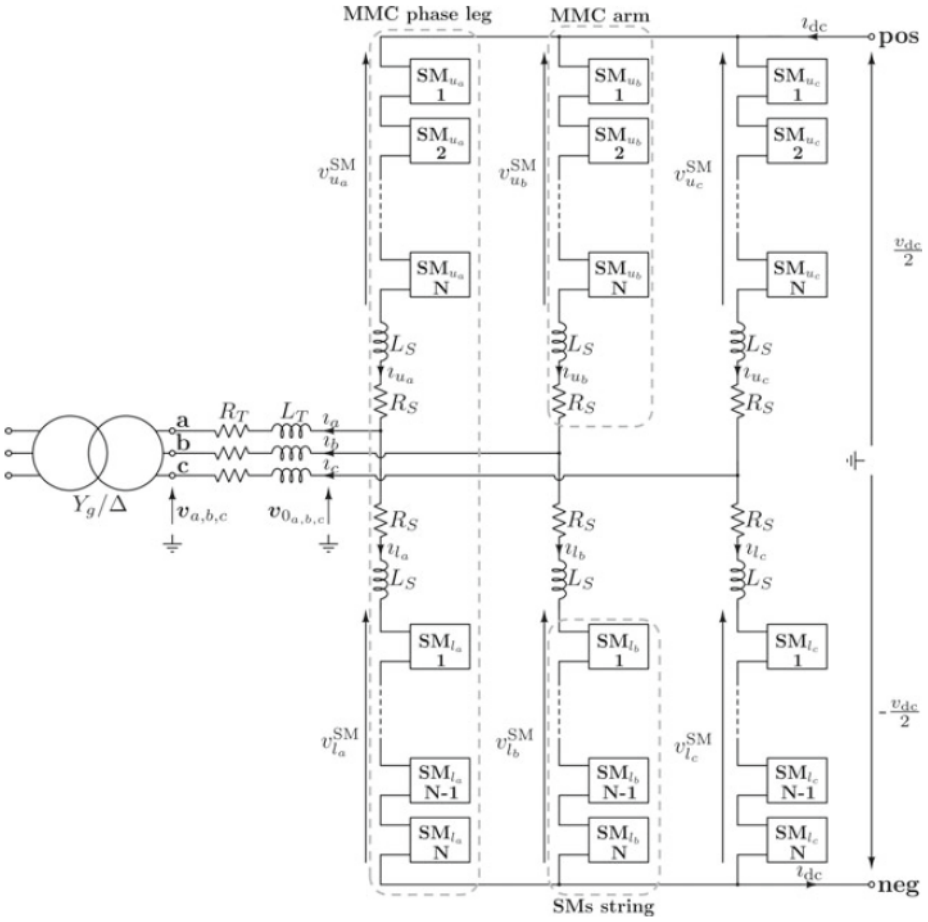

Figure 4.4: Circuit diagram of grid connected MMC [21]

Each phase leg is composed of two arms (upper and lower). Each arm contains N number of SMs, connected in series within each arm. Additionally, each arm has an inductor (L_S) and a resistor (R_S) to filter out high-frequency components and limit fault current. The schematic shows the connections from the three-phase generator (Y_g/Δ) to the MMC through a series of resistors (R_T) and inductors (L_T). The AC side voltages are $v_{a,b,c}$ and the DC side voltage is v_{dc}. The voltages $u_{a,b,c}$ are the AC side voltages after passing through the transformer, while $v_{0a,b,c}$ are the voltages after the transformer before entering the MMC phase legs. The voltages $v_{SM_{ua}}, v_{SM_{ub}}, v_{SM_{uc}}$ and $v_{SM_{la}}, v_{SM_{lb}}, v_{SM_{lc}}$ represent the voltages across the upper and lower sub-modules of each arm, respectively. The DC link is divided into two parts with $v_{dc}/2$ across each part, and the positive and negative DC bus bars are labeled as "pos" and "neg", respectively [24].

Submodule Mathematical Model

The relationship between the i-th SM's capacitor current i_{caui} and arm current i_{au} can be expressed as:

$$\dot{i}_{caui} = S_{aui} \cdot i_{au} \tag{4.23}$$

The relationship between SM's output voltage u_{sm_aui} and SM's capacitor voltage u_{caui} can be expressed as:

$$u_{sm\_aui} = S_{aui} \cdot u_{caui} \tag{4.24}$$

According to the Volt Ampere characteristic of the capacitor from Figure **??**, the voltage u_{caui} imposed on the SM's capacitor can be expressed as:

$$u_{caui} = \frac{1}{C}\int i_{caui}dt = \frac{1}{C}\int (S_{aui} \cdot i_{au})dt \tag{4.25}$$

Finally, the SM's output voltage u_{sm_uai} can be rewritten as:

$$u_{sm\_uai} = \frac{S_{aui}}{C}\int (S_{aui} \cdot i_{au})dt \tag{4.26}$$

Arm Mathematical Model

To simplify analysis of MMC dynamics, submodule strings for each arm are treated as controllable AC voltage sources. Figure 4.5 shows decoupled DC-side circuit, where v_{xu} and v_{xl} are upper and lower arm voltages for phases a, b and c, the same way i_{xu} and i_{xl} are upper and lower arm currents and i_{xi} and v_{xi} are inverter output currents and voltages respectively [24, 25].

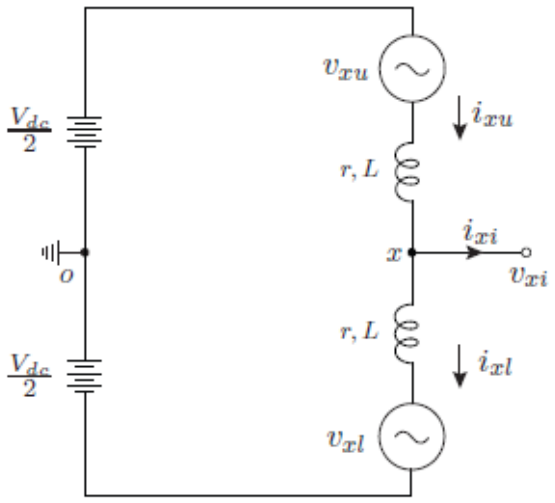

Figure 4.5: Decoupled DC side circuit representation [25]

To further simplify the analysis, linear transformations are defined to relate upper and lower arms with output and circulating currents and voltages [25]:

$$v_{xi} = \frac{v_{xl} - v_{xu}}{2} \tag{4.27}$$

$$v_{xc} = \frac{v_{xl} + v_{xu}}{2} \tag{4.28}$$

$$i_{xi} = i_{xl} - i_{xu} \tag{4.29}$$

$$i_{xc} = \frac{i_{xl} + i_{xu}}{2} \tag{4.30}$$

Where i_{xi} are the AC side currents, v_{xi} is inner emf (electromotive force) of each phase leg driving these currents. Additionally, i_{xi} are average currents of each phase leg, whereas v_{xi} are voltages driving these currents. Also, i_{xi} contains currents circulating between the phase legs and v_{xi} contains voltages driving these circulating currents. The inverse of transformations can be expressed as [25]:

$$v_{xu} = v_{xc} - v_{xi} \tag{4.31}$$

$$v_{xl} = v_{xc} + v_{xi} \tag{4.32}$$

$$i_{xu} = i_{xc} + \frac{i_{xi}}{2} \tag{4.33}$$

$$i_{xl} = i_{xc} - \frac{i_{xi}}{2} \tag{4.34}$$

Furthermore, assuming balanced DC side current, upper and lower arm currents can be expressed as [25]:

$$i_{xu} = \frac{1}{3} i_{dc} + i_{xc} + \frac{i_{xi}}{2} \tag{4.35}$$

$$i_{xl} = \frac{1}{3} i_{dc} + i_{xc} - \frac{i_{xi}}{2} \tag{4.36}$$

Assuming DC bus is balanced, upper and lower arm voltage dynamics are given as [25]:

$$v_{xu} = \frac{V_{dc}}{2} - v_{xi} - L\frac{di_{xu}}{dt} - r\, i_{xu} \tag{4.37}$$

$$v_{xl} = \frac{V_{dc}}{2} + v_{xi} - L\frac{di_{xl}}{dt} - r\, i_{xl} \tag{4.38}$$

MMC Output Current Model

Rearranging Equations 4.37 and 4.38, gives following expression for output voltage [26]:

$$v_{xo} = \underbrace{\frac{1}{2}\left(v_{xl} - v_{xu}\right)}_{v_{xi}} - \frac{1}{2}R_S i_{xi} - \frac{1}{2}L_S \frac{di_{xi}}{dt}, \tag{4.39}$$

Additionally, grid voltage can be expressed as[26]:

$$v_{xg} = -R_T i_{xi} - L_T \frac{di_{xi}}{dt} - v_{o,x} \tag{4.40}$$

By combining equations for inverter output voltage and grid voltage, following expression can be derived [26]:

$$v_{xg} = \underbrace{\frac{1}{2}\left(v_{xl} - v_{xu}\right)}_{v_{xi}} - (R_T + \frac{1}{2}R_S)i_{xi} - (L_T + \frac{1}{2}L_S)\frac{di_{xi}}{dt}, \tag{4.41}$$

Finally, by applying park transformation, equations describing MMC current dynamics can be described in direct quadrature form as [26]:

$$v_{id} - v_{gd} = \left(L_T + \frac{L_S}{2}\right)\frac{di_{id}}{dt} + \left(R_T + \frac{R_S}{2}\right)i_{id} + \left(L_T + \frac{L_S}{2}\right)\omega\, i_{iq} \tag{4.42}$$

$$v_{iq} - v_{gq} = \left(L_T + \frac{L_S}{2}\right)\frac{di_{iq}}{dt} + \left(R_T + \frac{R_S}{2}\right)i_{iq} + \left(L_T + \frac{L_S}{2}\right)\omega\, i_{id} \tag{4.43}$$

By applying Laplace transform to Equations 4.42 and 4.43 a block diagram shown in Figure 4.6 can be made, which depicts relationship between the converter voltage and its output current.

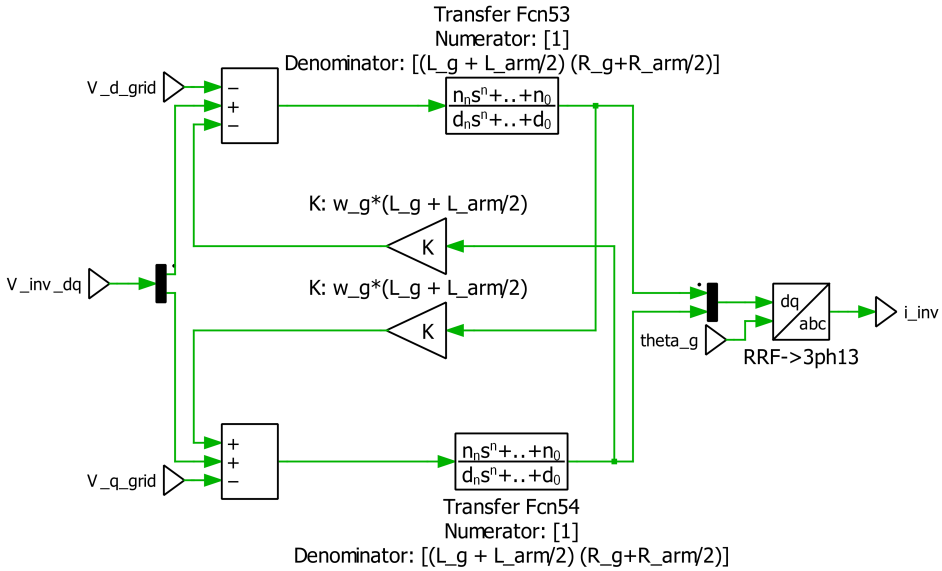

Figure 4.6: Upper Arm Current Transfer Function

Circulating Current Model

Arm current consists of DC-bus current i_{dc}, AC circulating current i_{xc}, and AC output current i_{xi}. Adding upper and lower arm currents gives common-mode current flowing through each leg as [27, 28]:

$$i_{xc} = \frac{1}{3} i_{dc} + i_{xc} \tag{4.44}$$

Furthermore, common-mode current component is given by [27, 28]

$$2L_s \frac{di_{xcc}}{dt} + 2R_s\, i_{xcc} = V_{dc} - (v_{xu} + v_{xl}) \tag{4.45}$$

Finally, circulating current model can be defined as [27, 28]:

$$L_s \frac{di_{xc}}{dt} + R_s\, i_{xc} = \frac{V_{dc}}{2} - \frac{1}{2}(v_{xu} + v_{xl}) - R_s \frac{i_{dc}}{3} \tag{4.46}$$

Considering that DC-bus current i_{dc} represents average power delivered by DC source and to simplify analysis, term $R_s \frac{i_{dc}}{3}$ is neglected which gives simplified model of the circulating currents [27, 28]:

$$L_s \frac{di_{xc}}{dt} + R_s\, i_{xc} = \underbrace{\frac{V_{dc}}{2} - \frac{1}{2}(v_{xu} + v_{xl})}_{v_{xcc}} \tag{4.47}$$

Furthermore, three-phase circulating currents can be transformed into two dc components in double line frequency, negative-sequence rotational frame as [27, 28]:

$$\begin{bmatrix} v_{\text{ccd}} \\ v_{\text{ccq}} \end{bmatrix} = L_0 \frac{d}{dt} \begin{bmatrix} i_{ccd} \\ i_{ccq} \end{bmatrix} + \begin{bmatrix} 0 & -2\omega_0 L_0 \\ 2\omega_0 L_0 & 0 \end{bmatrix} \begin{bmatrix} i_{ccd} \\ i_{ccq} \end{bmatrix} + R_0 \begin{bmatrix} i_{ccd} \\ i_{ccq} \end{bmatrix} \tag{4.48}$$

Following Laplace transformation the same as for MMC output current, the transfer function model with cross-coupling terms for circulating current model can be defined as shown in Figure 4.7

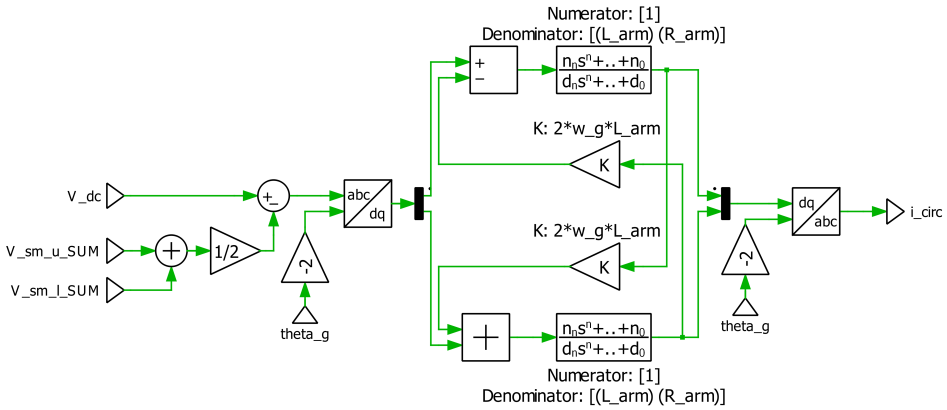

Figure 4.7: Lower Arm Current (Circulating Current) Transfer Function

4.1.5 Modulation

In order to convert arm voltage reference signal to gate signals of each submodule for MMC, modulator must be created. There are two main categories of modulators for MMCs: carrier based and nearest level modulators. Carrier based modulators are also know as PWM where carrier and reference signals are compared to determine the logic switching of the gates. There are many extensions of PWM modulators and two most common are phase-disposition PWM (PD-PWM) and phase-shifted PWM (PS-PWM). Nearest level modulators are different from PWM modulators because it does not have a carrier wave but instead uses a combination of voltages that are closest to the reference wave. All methods can be extended and there exists a broad research on the selection and differences between different modulators. The main characteristics of the basic modulators are listed in Table 4.5. It can be seen that carrier wave based modulators are more suitable for MMCs with lower number of SMs whereas nearest level modulation is more suitable for MMCs with large number of SMs [27, 29].

Modulation scheme	Characteristics
PD-PWM	• High switching frequency modulation • Unevenly distributed pulses • Suitable for MMCs with not so many SMs per arm
PS-PWM	• High switching frequency modulation • Evenly distributed pulses • Suitable for MMCs with not so many SMs per arm
NLM	• Low switching frequency modulation • Easy for implementation • Suitable for MMCs with large number of SMs per arm

Table 4.5: Comparison of Different Modulation Schemes for MMC

PS-PWM

The PS-PWM is suitable for the MMC with not so many SMs per arm. For the MMC with n SMs per arm, it is realized by applying n number of identical triangular carriers which are phase shifted by the same angle. The carrier is between -1 and 1. Through the comparison between the carriers and the reference signal y, the PS-PWM is achieved [27, 29].

Figure 4.8 illustrates the implementation principle of PS-PWM ($n = 5$) for the MMC with n SMs per arm.

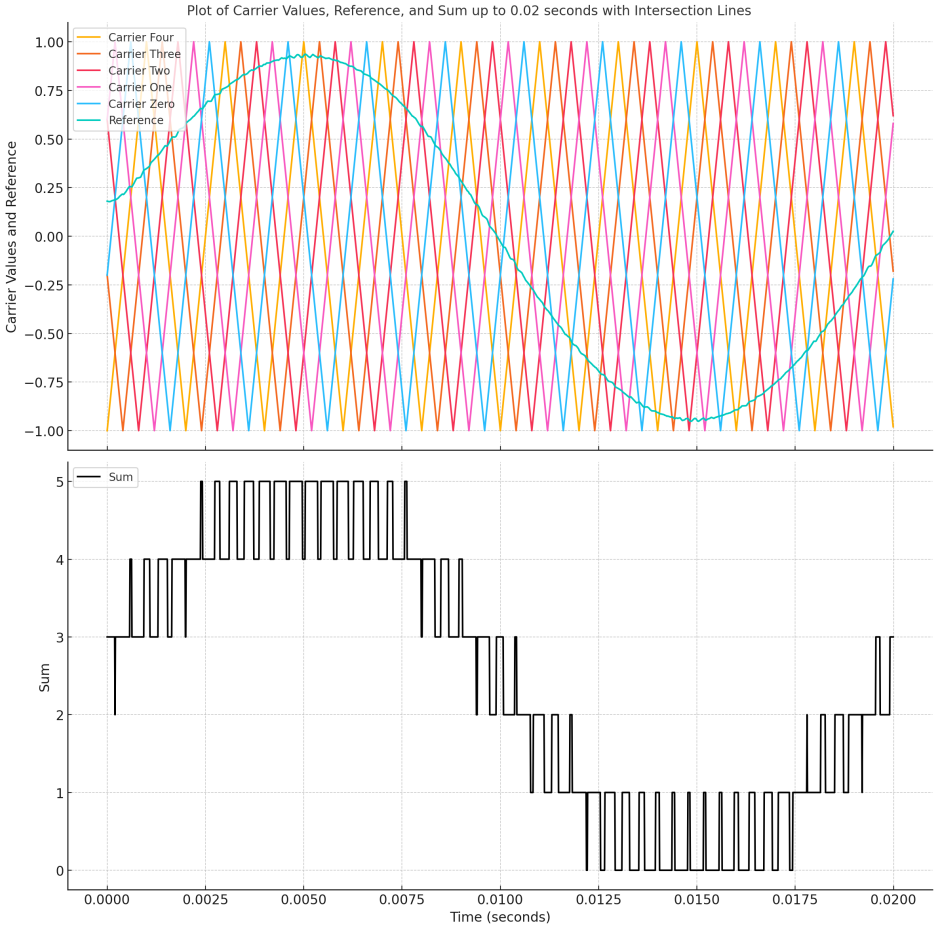

Figure 4.8: PS-PWM Modulation

The carriers are all with the same carrier frequency f_s = 500Hz. The phase angle between two adjacent carriers of is denoted as $\Delta\theta$. Generally, the $\Delta\theta$ is:

$$\Delta\theta = \frac{2\pi}{n} \tag{4.49}$$

The reference signal y is compared with the carriers to generate the pulses as follows:

- The pulse is 1 if the reference y is more than the carrier
- The pulse is 0 if the reference y is less than the carrier

The total number n_{on} of the SMs to be inserted into each arm at each instant can be expressed as the sum of pulses Sp_n, as [27, 29]:

$$n_{on} = \sum_{i=1}^{n} Sp_i \tag{4.50}$$

4.1.6 Electrical Circuit and Transfer Function Validation

To validate defined models, electrical circuit model as well as transfer function models have been developed on Simulink/PLECS environment. The parameters selected for simulation are shown in Table 4.6.

Parameter	Value
Capacitance of Submodule, C_{SM}	5×10^{-4}
Inductance of Arm, L_{arm}	1×10^{-2}
Resistance of Arm, R_{arm}	1×10^{-2}
AC Voltage, V_{ac}	2000
Grid Resistance, R_g	10
Grid Inductance, L_g	1×10^{-3}
Frequency of Submodule, F_{SM}	2000
DC Resistance, R_{dc}	0.01
DC Voltage, V_{dc}	5000
Number of Submodules, N	5
Total Capacitance, C_{tot}	$\frac{C_{SM}}{5}$
Initial State of Charge, SOC_{init}	0.5
Sampling Frequency, F_s	100000
Equivalent Inductance, L_{eq}	$L_g + \frac{L_{arm}}{2}$
Equivalent Resistance, R_{eq}	$R_g + \frac{R_{arm}}{2}$

Table 4.6: System Parameters

Figure 4.9 shows comparison of MMC output current for derived transfer function and designed electrical equivalent models. It can be clearly seen that transfer function model follows electrical equivalent precisely. This proves that transfer function model describes output current dynamics of MMC accurately. However, by looking at a zoomed-in Figure 4.10, it can be seen that output current models has a slight deviation, which are due to harmonic components present in the electrical model but not in the transfer function.

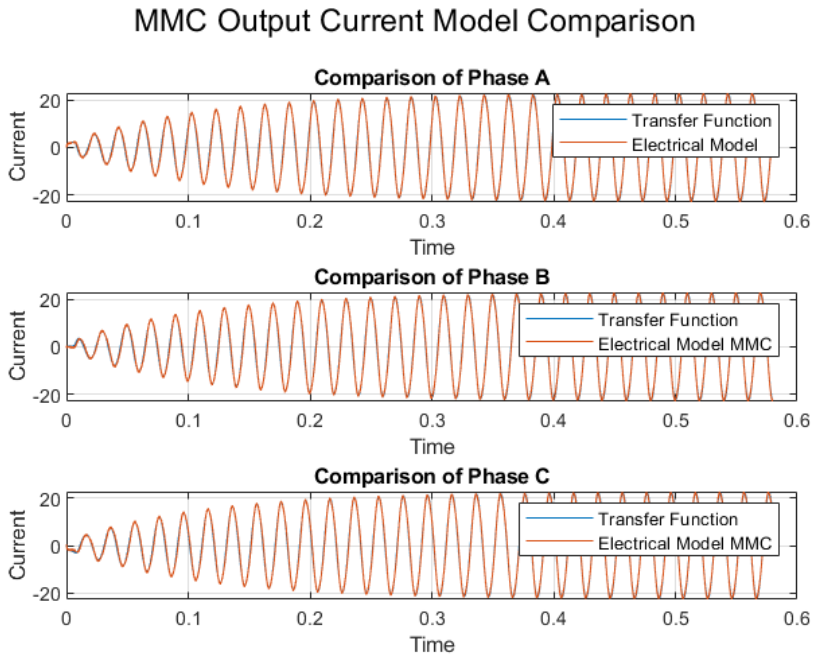

Figure 4.9: MMC Output Current Model Comparison

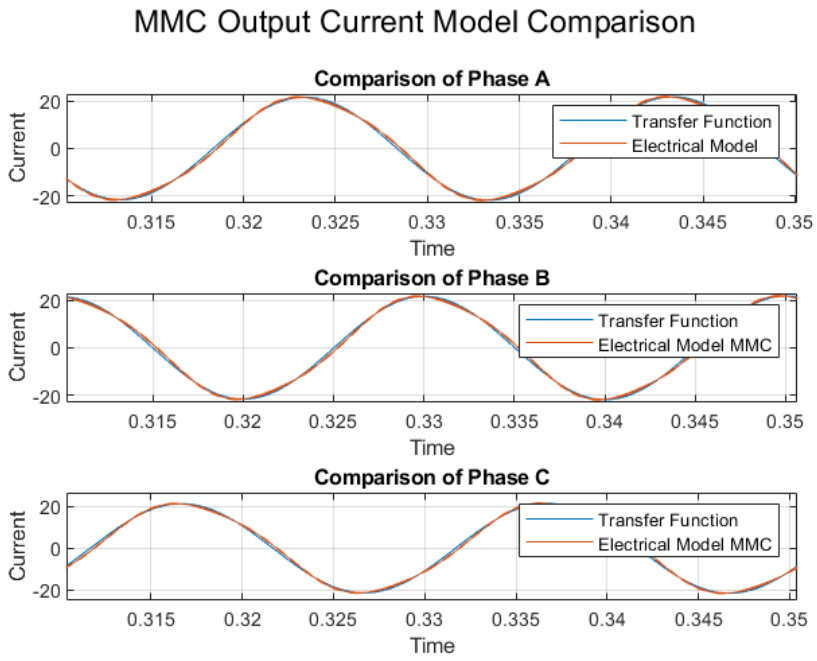

Figure 4.10: MMC Output Current Model Comparison (zoomed in)

Figure 4.11 shows comparison of MMC circulating current for derived transfer function and designed electrical equivalent models. It can be clearly seen that transfer function model follows electrical equivalent precisely, although there are some transient present in the transfer function model at the beginning of the simulation. Nonetheless, this proves that transfer function model describes circulating current dynamics of MMC accurately. Figure 4.12 shows a close up of Figure 4.11, which clearly shows that the transfer function represents the electrical model correctly.

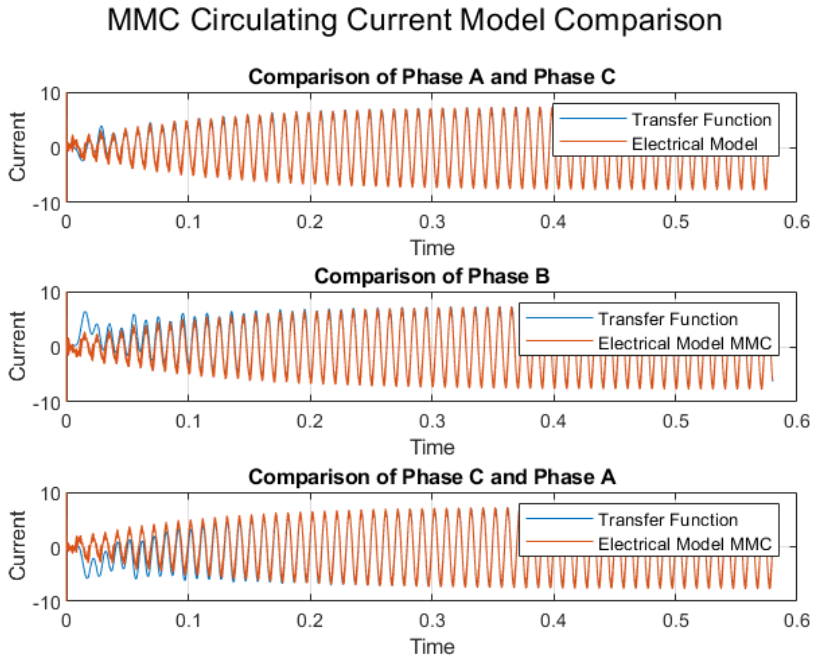

Figure 4.11: MMC Circulating Current Model Comparison

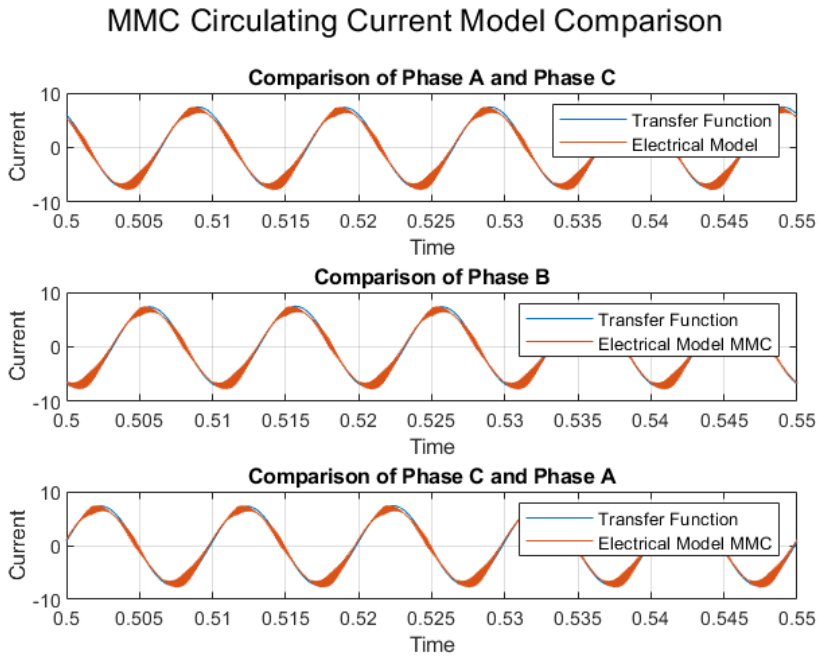

Figure 4.12: MMC Circulating Current Model Comparison (zoomed in)

Furthermore, by applying inverse linear transformations relating output current and circulating current with upper and lower arm currents, a transfer function model defined in Figure 4.13 has been derived. The comparison of the response between transfer function and electrical model measurements are shown in Figures 4.14 and 4.15. It can be seen from the figures that the models indeed match with a slight deviation due as seen for output current and circulating current models separately.

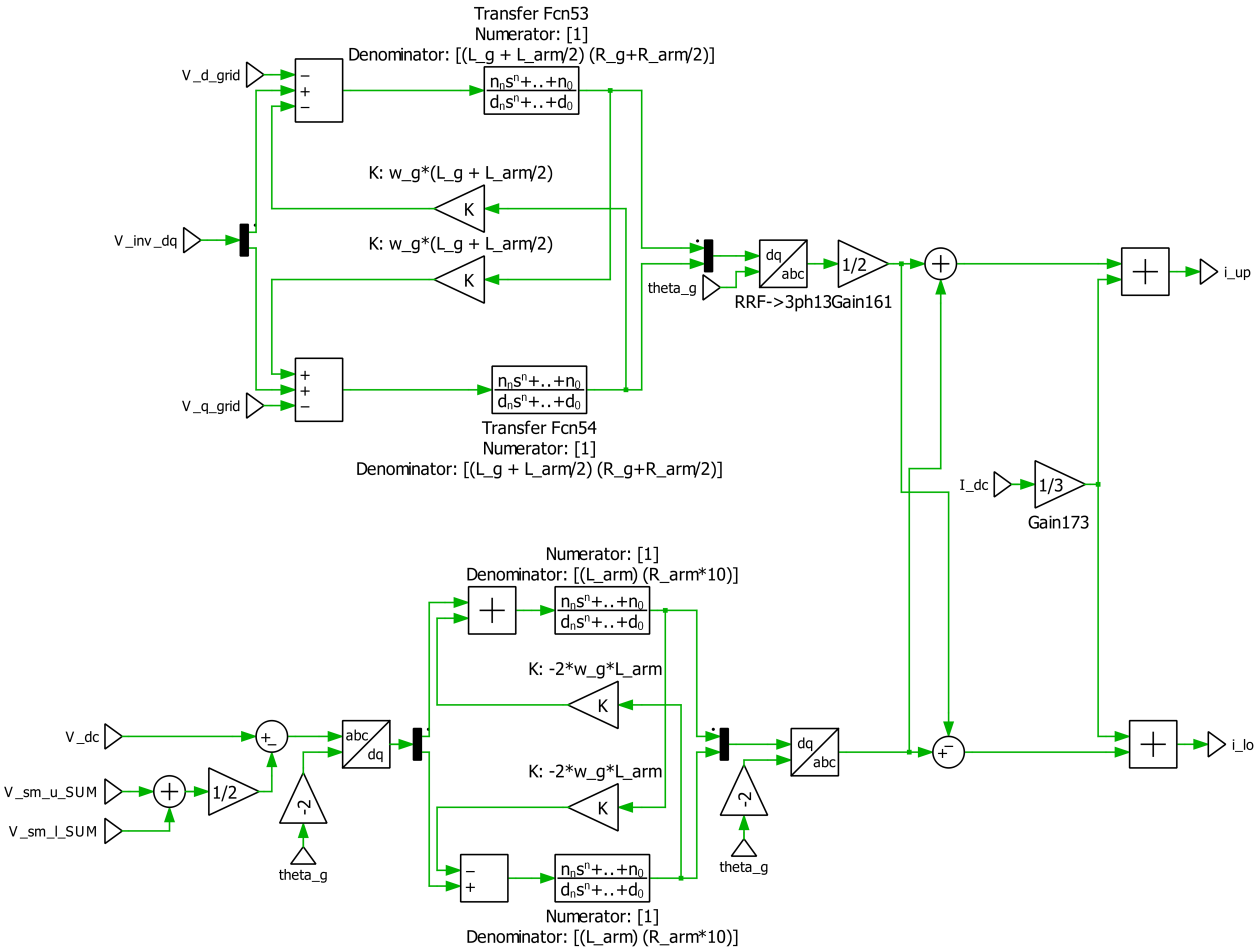

Figure 4.13: Transfer function model for upper and lower arm currents

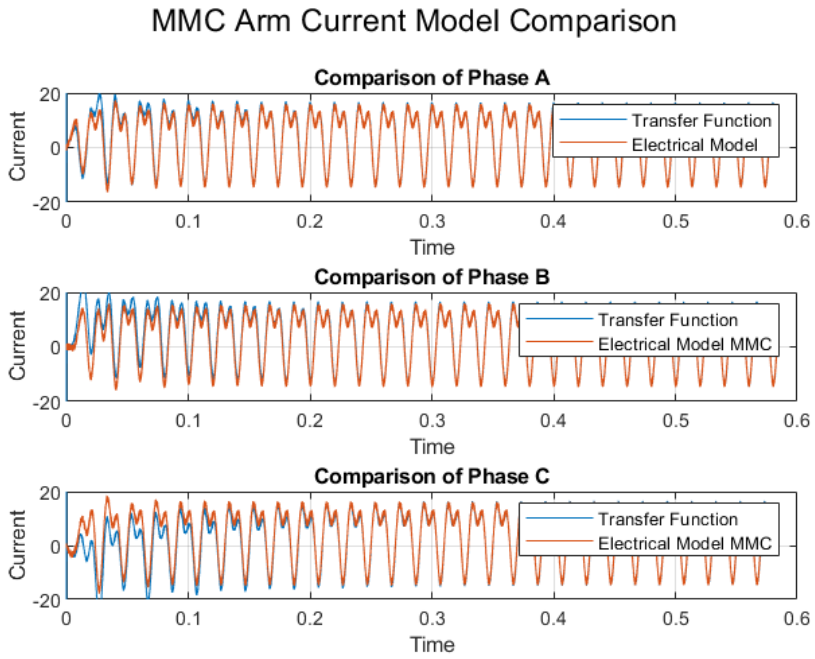

Figure 4.14: MMC Arm Current Model Comparison

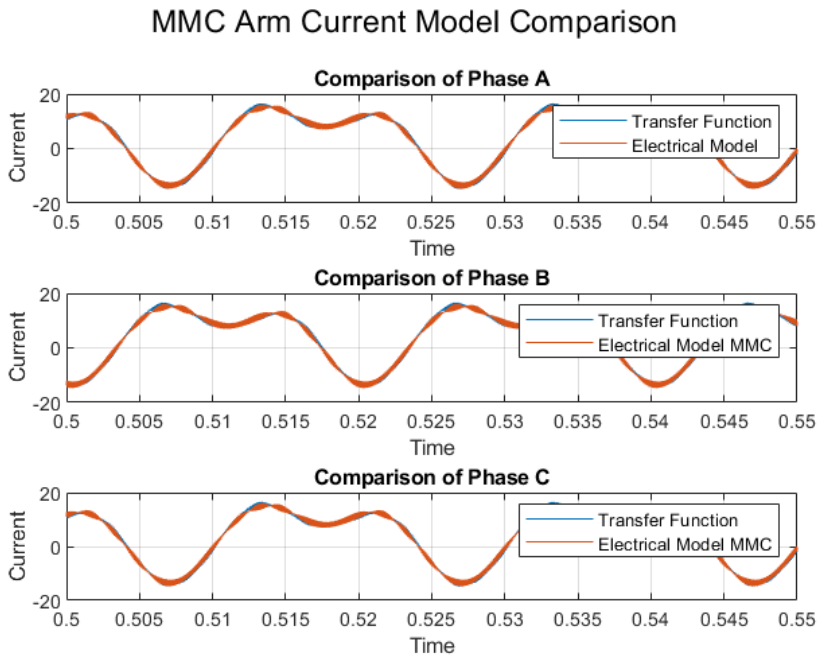

Figure 4.15: MMC Arm Current Model Comparison (zoomed in)

Lastly, there was an attempt at defining MMC output voltage as well as voltages driving circulating currents by incorporating submodule capacitor dynamics to obtain upper and lower arm voltages. The model is defined in Figure 4.16. However, it can be seen from Figure 4.17, such model did not yield satisfactory results. While the transfer function model exhibit some similarity to the electrical model, it can be clearly seen that transfer function is lagging as well as saturates at 0 and does not go below 0 volts which is not the case for electrical model. Further investigation might be required to determine how to obtain upper and lower arm voltages from upper and lower arms currents.

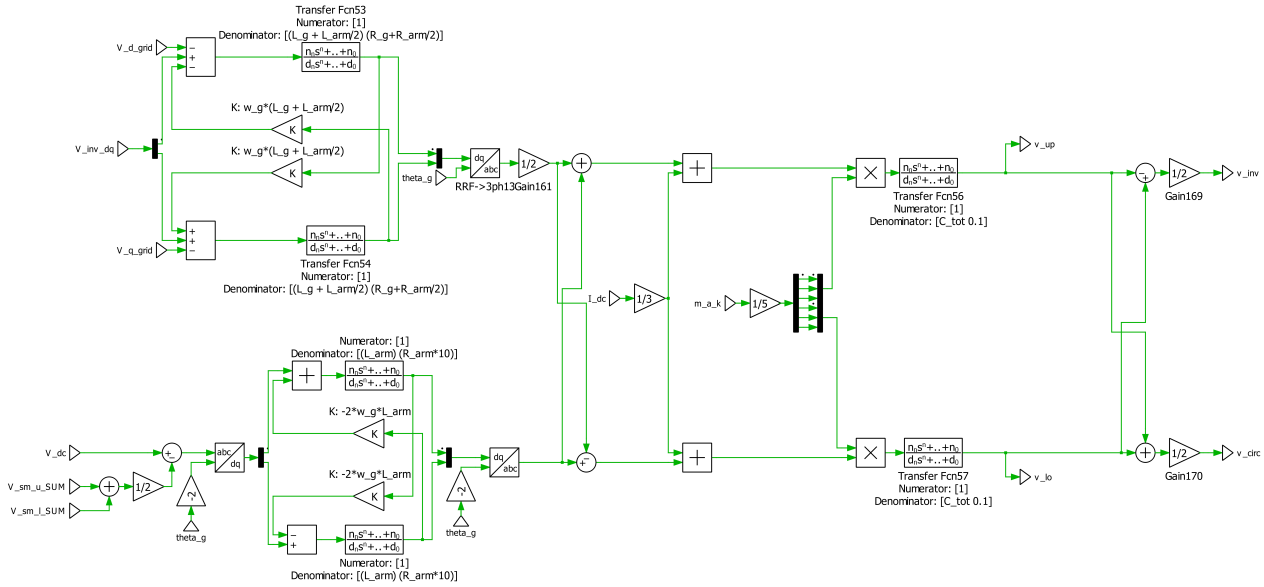

Figure 4.16: Transfer function model with added submodule capacitor dynamics

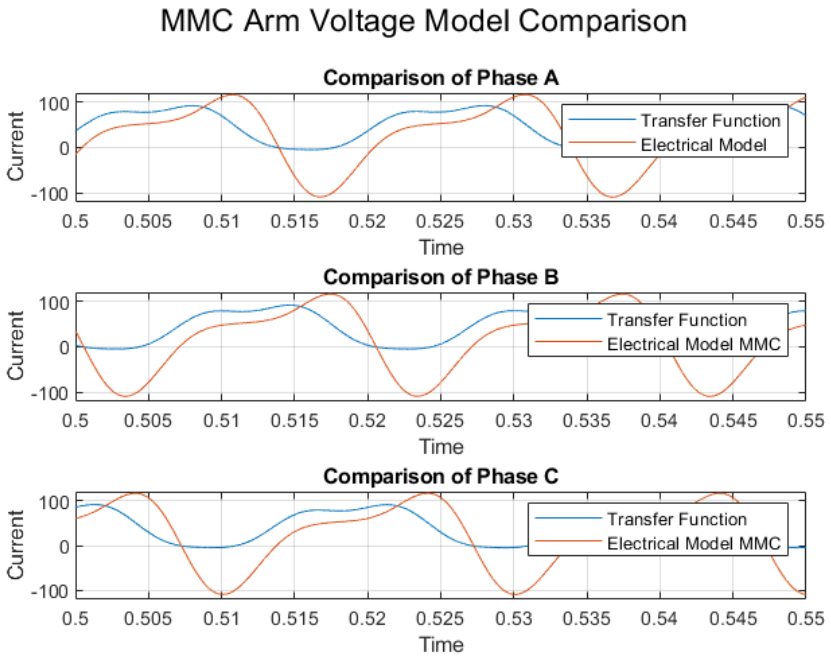

Figure 4.17: MMC Arm Voltage Model Comparison

After the development and validation of the open loop models, it is now appropriate to proceed with the control design. Next chapter will focus on the different layers and requirements for the control of MMC.

4.2 Modelling of Submodules

As mentioned previously, the general types of MMC submodules includes that of half-bridge or full-bridge topologies. In the case, where battery is utilized within a submodule, a different type of submodule is used, shown in Figure 4.18

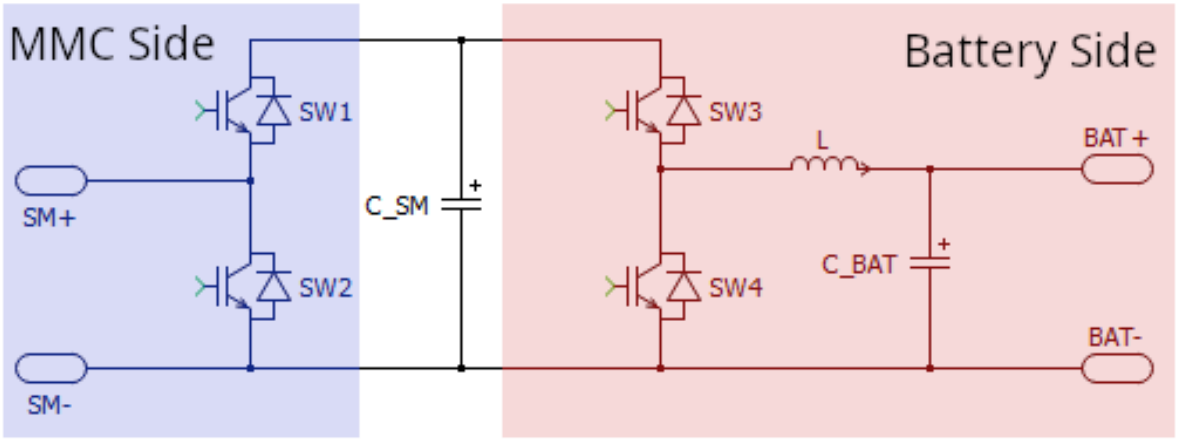

Figure 4.18: Modified submodule with battery integration

The presented submodule type consists of: MMC side half-bridge and a bidirectional DC-DC buck-boost converter used for interfacing between the MMC side capacitor and the battery pack [30, 31]. The chosen structure of the submodule allows for the decoupling of the battery side and MMC side through C_{SM} when employing appropriate control, thus preventing ripples flowing into the battery, which harm and reduce the performance of the battery. Furthermore, the use of the bidirectional DC-DC converter allows for the charging and discharging of the battery.

4.2.1 Battery Side Bidirectional DC-DC Buck-Boost Converter

Presented in Figure 4.19 is a diagram of a non-isolated bidirectional DC-DC buck-boost converter.

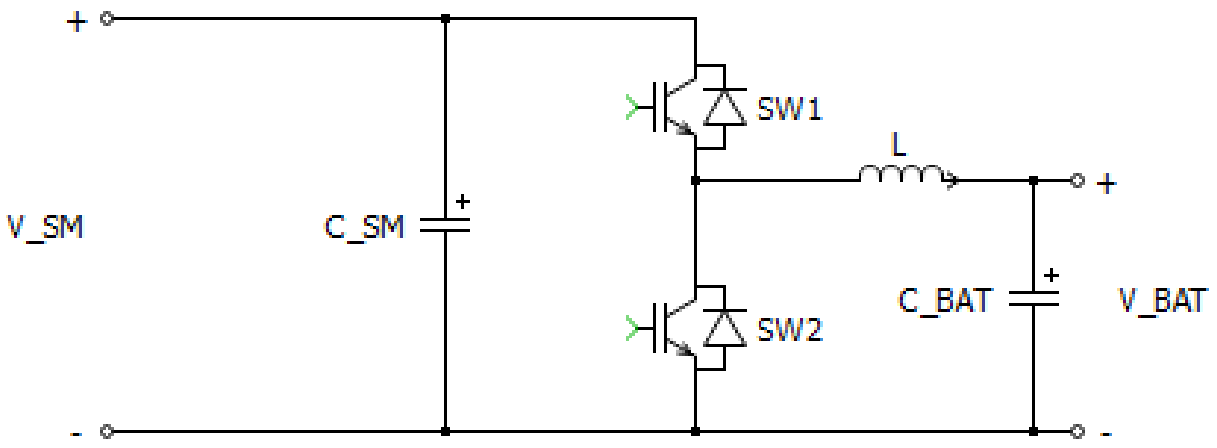

Figure 4.19: Battery Side DC/DC Buck-Boost Converter

The high-side voltage, represented as V_{SM} is the voltage across the C_{SM} (MMC side). The low-side voltage, represented as V_{BAT} is the battery voltage (battery side). In regards to the passive components, the inductor L serves as an energy storage, where it stores energy in one switching cycle and releases it during another. Other than that, it serves current smoothing function and limits the current rate of change. The capacitors purpose is to ensure a constant DC voltage and reduce the ripple at each of the outputs. The choice of switches is determined based on application, most commonly used ones are MOSFETs or IGBTs. The converter is designed as a combination of two fundamental DC-DC converter topologies - buck and boost, presented in Figures 4.20 and 4.21.

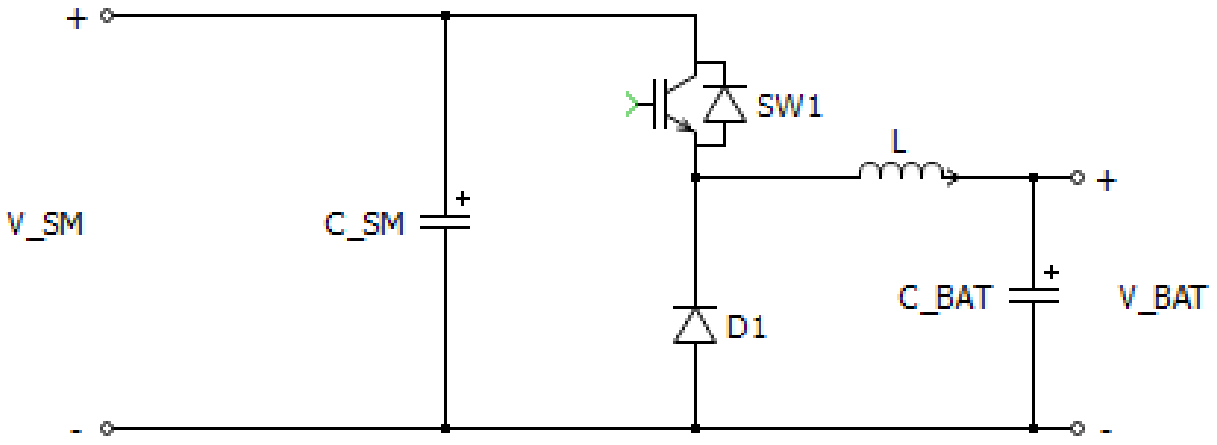

Figure 4.20: DC-DC Buck Converter

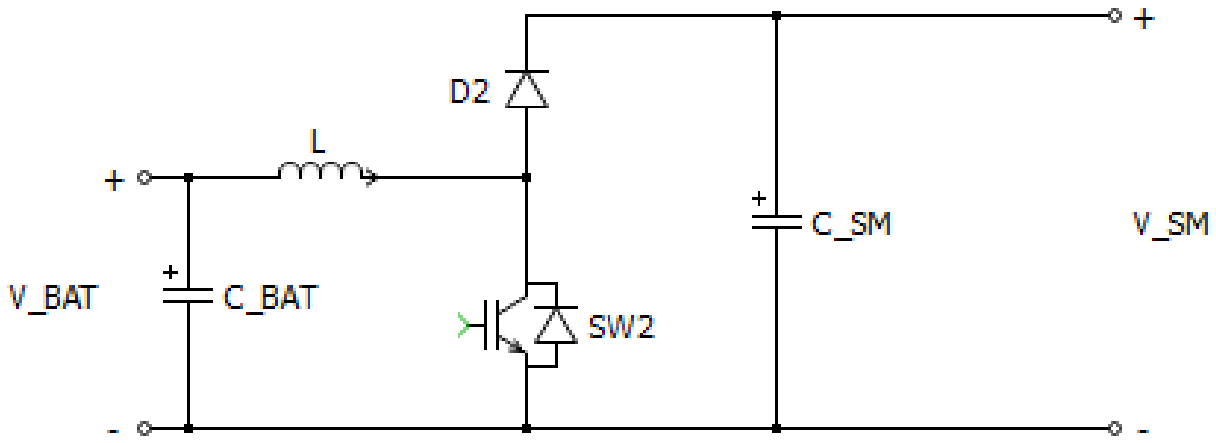

Figure 4.21: DC-DC Boost Converter

4.2.2 Converter Design

The combined circuit would allow the converter to work in both buck and boost modes, thus allowing the change in the direction of the current depending on which mode it is operating in. For the operation in buck mode, switch SW_1 is receiving the PWM signal and SW_2 acts as a diode, and for the operation in boost mode it is the opposite. In the application of battery charging and discharging, the buck operating mode would be used for battery charging - stepping down voltage from the MMC side to the appropriate voltage for the battery. For discharging, boost operating mode would be in use, stepping up the voltage of the battery to the required voltage appropriate to the DC link voltage.

4.2.3 Modualation

For the modulation of the bidirectional DC-DC converter, triangular PWM modulation has been used. The modulation logic for the converter can be seen in Figure 4.22.

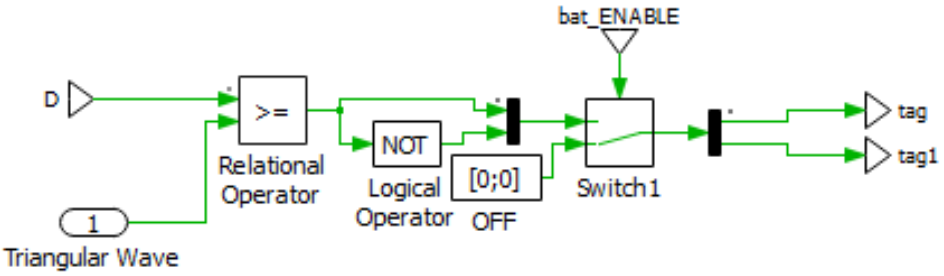

Figure 4.22: Modulation logic for the DC-DC converter

Duty cycle D is the control input, which is generated from the DC-DC converters controllers, presented in Section 5.0.3. It acts as a threshold for the comparator, which compares the duty cycle with the generated triangular wave. The triangular wave is generated at 10kHz. This frequency is the DC-DC converters switching frequency, f_s. The comparator outputs a binary PWM signal for the switches. When the triangular wave value is lower or equal to the value of the duty cycle, the generated PWM signal is a high (1), which signals the switch to close. When the PWM signal is a low (0), the switch is open. Figure 4.23 showcases the generation of the PWM signal with duty cycle of 0.4.

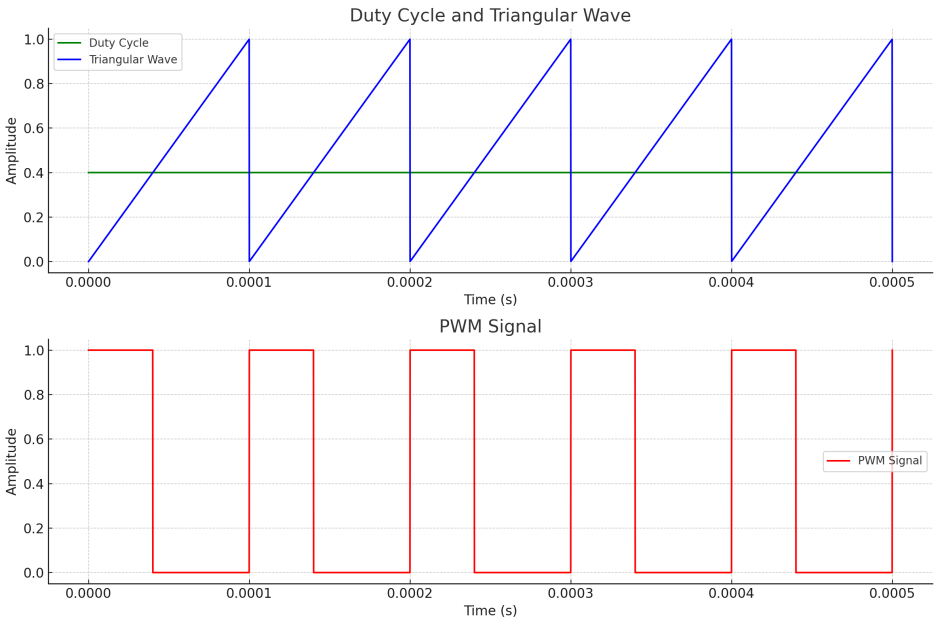

Figure 4.23: Modulation Waveform (Duty Cycle 0.4)

The logical operator is utilized to make sure that only one switch is conducting at a time, to avoid cases where both or neither of the switches are closed. The battery enable logic acts as an ON/OFF switch for the DC-DC converter, the logic is further explained in Chapter 5, Section 5.0.3.

4.2.4 Component Selection

In order for the DC-DC converter to operate correctly and efficiently, it is important to consider the aspect of component selection. As mentioned previously, the DC-DC converter contains two switches, and inductor and a battery side capacitor. Firstly, the selection of suitable switches is analyzed. The two most common semiconductors are - MOSFET and IGBT. MOSFETs main use case concerns high frequency, low voltage switching applications (below 600V). IGBTs on the other hand are utilized mainly for

medium to high power applications with voltages over 1000V, low frequencies (below 20kHz) [32]. It provides better thermal range than MOSFETs and provides a higher output power. As the application in this project will be dealing with medium-high power, the selected switches for the DC-DC converter are IGBTs. The selection of passive components are calculated based on the respective mode that the converter is in, however few considerations should be made:

- Components are considered ideal, meaning that ESR of components are neglected.
- The value of the inductor should be chosen such, that the converter always operates in CCM.

Component Selection (Buck) [33]

To calculate the maximum duty cycle the following equation is used:

$$D_{Buck} = \frac{V_{BAT}}{V_{SM_{max}} \cdot \eta} \tag{4.51}$$

Here η represents the efficiency of the the converter. In this case the converter is considered to be ideal, therefore the efficiency is equal to 1. Nominal voltage of the battery $V_{BAT_{max}}$ is $\approx$ 602V. Maximum submodule voltage V_{SM} is equal to 1000V

$$D_{Buck} = \frac{602V}{1000V} = 0.602 \tag{4.52}$$

As we are selecting the inductor value based on the inductor current ripple, the equation to calculate the inductor current ripple is given below. A good estimation for ΔI_L is 20% of the output current:

$$\Delta I_L = 0.2 \cdot I_{o_{max}} \tag{4.53}$$

The selected maximum output current is equal to 5A.

$$\Delta I_L = 0.2 \cdot 5A = 1A \tag{4.54}$$

Having the inductor current ripple, the minimum inductor value can be calculated by:

$$L_{Buck_{min}} = \frac{V_{BAT} \cdot (V_{SM} - V_{BAT})}{\Delta I_L \cdot f_s \cdot V_{SM}} \tag{4.55}$$

Using the values, we are able to calculate the minimum inductor value:

$$L_{Buck_{min}} = \frac{602V \cdot (1000V - 602V)}{1A \cdot 10kHz \cdot 1000V} \approx 24mH \tag{4.56}$$

To calculate the minimum capacitor value $C_{BAT_{min}}$ for the battery side, following equation is used:

$$C_{BAT_{min}} = \frac{\Delta I_L}{8 \cdot f_s \cdot \Delta V_{BAT}} \tag{4.57}$$

Where ΔV_{BAT} is the desired voltage ripple over C_{BAT}. The selected ΔV_{BAT} in this case is 1%.

Using the values, the minimum capacitor value $C_{BAT_{min}}$ is calculated to be:

$$C_{BAT_{min}} = \frac{1A}{8 \cdot 10kHz \cdot 6.02V} \approx 2.08\mu F \tag{4.58}$$

Component Selection (Boost) [34]

To calculate the duty cycle for minimum (fully discharged) battery voltage ($V_{BAT_{min}}$) the following equation is used:

$$D_{Boost} = 1 - \frac{V_{BAT_{min}} \cdot \eta}{V_{SM}} \tag{4.59}$$

As the converter is considered ideal in this case, the efficiency η is equal to 1. The minimum battery voltage is $\approx$ 568V. The nominal submodule voltage is equal to 1000V. Using the values, duty cycle can be calculated as:

$$D_{Boost} = 1 - \frac{568V}{1000V} = 0.432 \tag{4.60}$$

The equation to calculate the estimated inductor current ripple, considering the ripple current is 20% of the output current is as follows:

$$\Delta I_L = \frac{(0.2 \cdot I_{o_{max}}) \cdot V_{SM}}{V_{BAT}} \tag{4.61}$$

Using the values, the calculation for the inductor ripple current is made as:

$$\Delta I_L = \frac{(0.2 \cdot 5A) \cdot 1000V}{602V} \approx 1.67A \tag{4.62}$$

Then the calculation for the minimum inductor value can be found by utilizing the following equation:

$$L_{Boost_{min}} = \frac{V_{BAT} \cdot (V_{SM} - V_{BAT})}{\Delta I_L \cdot f_s \cdot V_{SM}} \tag{4.63}$$

Calculating the minimum inductor value, gives:

$$L_{Boost_{min}} = \frac{602V \cdot (1000V - 602V)}{1.67A \cdot 10kHz \cdot 1000V} \approx 14mH \tag{4.64}$$

The inductor value selected is the one with the higher inductance as it should be able to work in CCM for both buck and boost modes. The parameters used for the bidirectional DC-DC converter are presented in Table 4.7.

Parameter	Value
Capacitor C_{BAT}	5µF
Selected Inductor L	50mH
Nominal Voltage V_{SM}	1000V
Nominal Voltage V_{BAT}	602V
Duty Cycle D_{Buck}	0.602
Duty Cycle D_{Boost}	0.432
Resistive Load (Boost) R	333Ω
Resistive Load (Buck) R_{BAT}	130Ω

Table 4.7: Final bidirectional DC-DC converter parameters

4.2.5 Mathematical Modeling

For the design of controllers and performing stability analysis, the mathematical model of electrical dynamics for the buck and boost converters are derived. The process that is followed is the same for both converters. Firstly, the appropriate state equations are derived using the EECs for when the switch is ON and OFF [35].

Buck mode modeling

When the converter is in buck mode, SW_2 is modeled as a diode and SW_1 is controlled using PWM with duty cycle D. The converters operation can be split into two sub intervals - one for when SW_1 is closed and one for when SW_1 is open. The equivalent circuits for when SW_1 is closed and open are shown in Figures 4.24 and 4.25 respectively. These circuits have been derived from Figure 4.20, note that the capacitor C_{SM} has been removed from the EECs, as it is not needed for the state-space derivation. The states variable vector and the input vector for the buck converter are:

$$\mathbf{x} = \begin{bmatrix} i_L \\ v_{CBAT} \end{bmatrix} \mathbf{u} = \begin{bmatrix} v_{SM} \end{bmatrix} \tag{4.65}$$

Where i_L is the current over the inductor and v_{CBAT} is the output capacitor voltage, input is v_{SM}. The general form of state-space representation contains the system matrix (A), input matrix (B), output matrix (C) and the feed-forward matrix (D).

$$\begin{aligned} \dot{\mathbf{x}} &= A\mathbf{x} + B\mathbf{u} \\ \mathbf{y} &= C\mathbf{x} + D\mathbf{u} \end{aligned} \tag{4.66}$$

To find the state equations of the buck mode, KVL and KCL are carried out in cases when the SW_1 is closed and open.

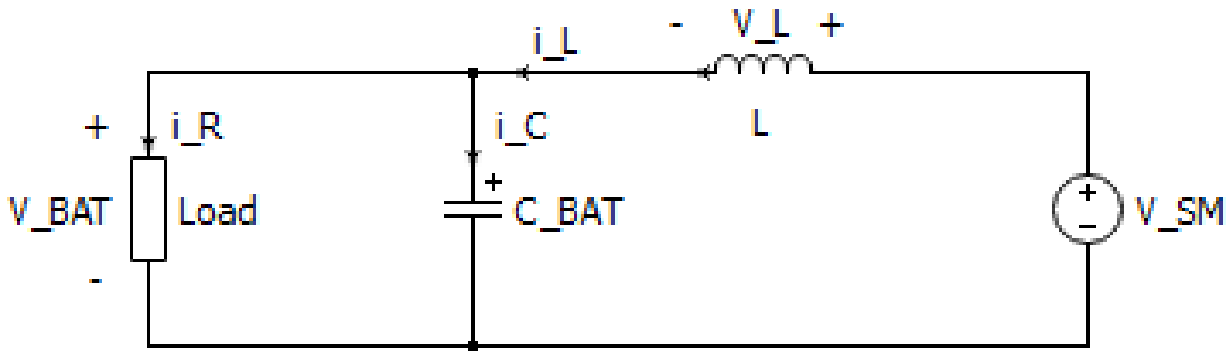

Figure 4.24: EEC of Buck Converter when SW_1 is closed

Applying KVL to circuit in Figure 4.24, yields the following:

$$-v_{SM} + v_L + v_{CBAT} = 0 \rightarrow v_{SM} = v_L + v_{CBAT} \tag{4.67}$$

We can then express v_L as:

$$v_L = L \cdot \frac{di_L}{dt} \tag{4.68}$$

Returning to Equation 4.67, the derivative of the state variable i_L can be expressed as:

$$\frac{di_L}{dt} = \frac{v_{SM} - v_{CBAT}}{L} \tag{4.69}$$

Performing KCL on the circuit yields the following equation:

$$i_L - i_C - i_R = 0 \rightarrow i_R = i_L - i_C \tag{4.70}$$

Expressing i_C as:

$$i_C = C_{BAT} \cdot \frac{dv_{CBAT}}{dt} \tag{4.71}$$

From Ohm's Law, we can say that i_R is:

$$i_R = \frac{v_{CBAT}}{R} \tag{4.72}$$

Returning to Equation 4.70, the derivative of the state variable v_{CBAT} can be expressed as:

$$\frac{dv_{CBAT}}{dt} = \frac{i_L}{C_{BAT}} - \frac{v_{SM}}{R \cdot C_{BAT}} \tag{4.73}$$

Having obtained the state equations, they can be combined to form the state-space representation for when the SW_1 is closed:

$$\begin{aligned}\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_{CBAT}}{dt} \end{bmatrix} = A_{Buck_1}\mathbf{x} + B_{Buck_1}\mathbf{u} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C_{BAT}} & -\frac{1}{R \cdot C_{BAT}} \end{bmatrix} \begin{bmatrix} i_L \\ v_{CBAT} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{SM} \\ y = C_{Buck_1}\mathbf{x} + D_{Buck_1} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_{CBAT} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_{SM}\end{aligned} \tag{4.74}$$

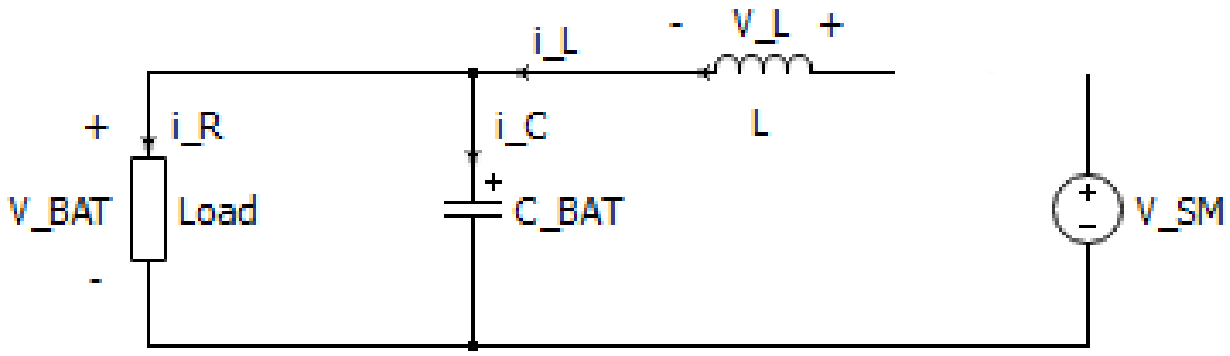

Figure 4.25: EEC of Buck Converter when SW_1 is open

Conducting same procedure on the circuit when SW_1 is open, yields us with the following state equations:

$$\frac{di_L}{dt} = -\frac{v_{CBAT}}{L} \tag{4.75}$$

$$\frac{dv_{CBAT}}{dt} = \frac{i_L}{C_{BAT}} - \frac{v_{CBAT}}{R \cdot C_{BAT}} \tag{4.76}$$

These equations again can be combined to form the state-space representation for when SW_1 is open:

$$\begin{aligned}\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_{CBAT}}{dt} \end{bmatrix} = A_{Buck_2}\mathbf{x} + B_{Buck_2}\mathbf{u} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C_{BAT}} & -\frac{1}{R \cdot C_{BAT}} \end{bmatrix} \begin{bmatrix} i_L \\ v_{CBAT} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_{SM} \\ y = C_{Buck_2}\mathbf{x} + D_{Buck_2} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_{CBAT} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_{SM}\end{aligned} \tag{4.77}$$

State-Space Averaging

Having the state-space representations of when the SW_1 is closed and open in Equations 4.74 and 4.77 respectively, state-space averaging technique can be applied, allowing us to

obtain a simplified model of the converter that averages the effects of switching over one switching period. Since the duty cycle D consists of ON and OFF operations over Ts, averaged matrices can combine state equations for both ON and OFF operation. Therefore, the averaged matrices can be expressed in the following form:

$$\begin{aligned} A_{Buck_{avg}} &= A_{Buck_1} \cdot D + A_{Buck_2} \cdot (1-D) \\ B_{Buck_{avg}} &= B_{Buck_1} \cdot D + B_{Buck_2} \cdot (1-D) \\ C_{Buck_{avg}} &= C_{Buck_1} \cdot D + C_{Buck_2} \cdot (1-D) \\ D_{Buck_{avg}} &= D_{Buck_1} \cdot D + D_{Buck_2} \cdot (1-D) \end{aligned} \tag{4.78}$$

Using the Equations 4.74, 4.77 and 4.78, we obtain the averaged matrices $A_{Buck_{avg}}$, $B_{Buck_{avg}}$, $C_{Buck_{avg}}$ and $D_{Buck_{avg}}$:

$$A_{Buck_{avg}} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C_{BAT}} & -\frac{1}{R \cdot C_{BAT}} \end{bmatrix} \tag{4.79}$$

$$B_{Buck_{avg}} = \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix} \tag{4.80}$$

$$C_{Buck_{avg}} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{4.81}$$

$$D_{Buck_{avg}} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{4.82}$$

All combined, the following averaged state-space representation is obtained:

$$\begin{aligned} \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_{CBAT}}{dt} \end{bmatrix} &= \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C_{BAT}} & -\frac{1}{R \cdot C_{BAT}} \end{bmatrix} \begin{bmatrix} i_L \\ v_{CBAT} \end{bmatrix} + \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix} v_{SM} \\ y &= \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_{CBAT} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_{SM} \end{aligned} \tag{4.83}$$

For further analysis, small-signal model is derived using linearization. Linearization of the averaged state-space model presented in Equation 4.83 is done. Linearization can be done by constructing a small-signal AC model, and the linearized model with perturbations can be expressed by the following representation:

$$\begin{aligned} \tilde{\mathbf{x}} &= A\tilde{\mathbf{x}} + B\tilde{\mathbf{u}} + M\tilde{\mathbf{d}} \\ \tilde{\mathbf{y}} &= C\tilde{\mathbf{x}} + D\tilde{\mathbf{u}} + N\tilde{\mathbf{d}} \end{aligned} \tag{4.84}$$

Where the vector coefficients M and N of input $\tilde{d}$ are:

$$\begin{aligned} M &= (A_{Buck_1} - A_{Buck_2}) \cdot X + (B_{Buck_1} - B_{Buck_2}) \cdot u \\ N &= (C_{Buck_1} - C_{Buck_2}) \cdot X + (D_{Buck_1} - D_{Buck_2}) \cdot u \end{aligned} \tag{4.85}$$

The X in the equations represent the DC gain and is expressed as:

$$X = -A_{Buck}^{-1} Bu \tag{4.86}$$

Calculating M and N coefficients, yields the following state-spaces:

$$M_{Buck} = \begin{bmatrix} -\frac{V_{BAT}}{L \cdot (D-1)} \\ 0 \end{bmatrix} \tag{4.87}$$

$$N_{Buck} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{4.88}$$

For simplification the inputs $\tilde{u}$ and $\tilde{d}$ can be joined together. The linearized state-space model with perturbations can be expressed as:

$$\begin{aligned} \begin{bmatrix} \frac{d\tilde{i_L}}{dt} \\ \frac{dv_{CBAT}}{dt} \end{bmatrix} &= \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C_{BAT}} & -\frac{1}{R \cdot C_{BAT}} \end{bmatrix} \begin{bmatrix} \tilde{i_L} \\ \tilde{v_{CBAT}} \end{bmatrix} + \begin{bmatrix} \frac{D}{L} & -\frac{V_{BAT}}{L \cdot (D-1)} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \tilde{u} \\ \tilde{d} \end{bmatrix} \\ y &= \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \tilde{i_L} \\ \tilde{v_{CBAT}} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \tilde{u} \\ \tilde{d} \end{bmatrix} \end{aligned} \tag{4.89}$$

For purposes of model validation and control, the transfer function of DC-DC converter in buck mode are derived by using the state-space to transfer function formula:

$$\frac{Y(s)}{X(s)} = C_{Buck}(sI - A_{Buck}^{-1}) B_{Buck} \tag{4.90}$$

By using the formula, we acquire the transfer functions, that showcase the relationship between the state variables and the inputs, therefore we get a total of 4 transfer functions.

$$\frac{\tilde{I_L}}{\tilde{V_{SM}}} = \frac{12.04s + 1.852 \cdot 10^4}{s^2 + 1538s + 4 \cdot 10^6} \tag{4.91}$$

$$\frac{\tilde{V_{CBAT}}}{\tilde{V_{SM}}} = \frac{2.408 \cdot 10^6}{s^2 + 1538s + 4 \cdot 10^6} \tag{4.92}$$

$$\frac{\tilde{I_L}}{\tilde{d}} = \frac{2000s + 3.077 \cdot 10^7}{s^2 + 1538s + 4 \cdot 10^6} \tag{4.93}$$

$$\frac{\tilde{V_{CBAT}}}{\tilde{d}} = \frac{4 \cdot 10^9}{s^2 + 1538s + 4 \cdot 10^6} \tag{4.94}$$

The open-loop dynamics of the systems transfer functions $\frac{\tilde{I_L}}{\tilde{d}}$ and $\frac{\tilde{V_{SM}}}{\tilde{I_L}}$ can be seen in Figure 4.26.

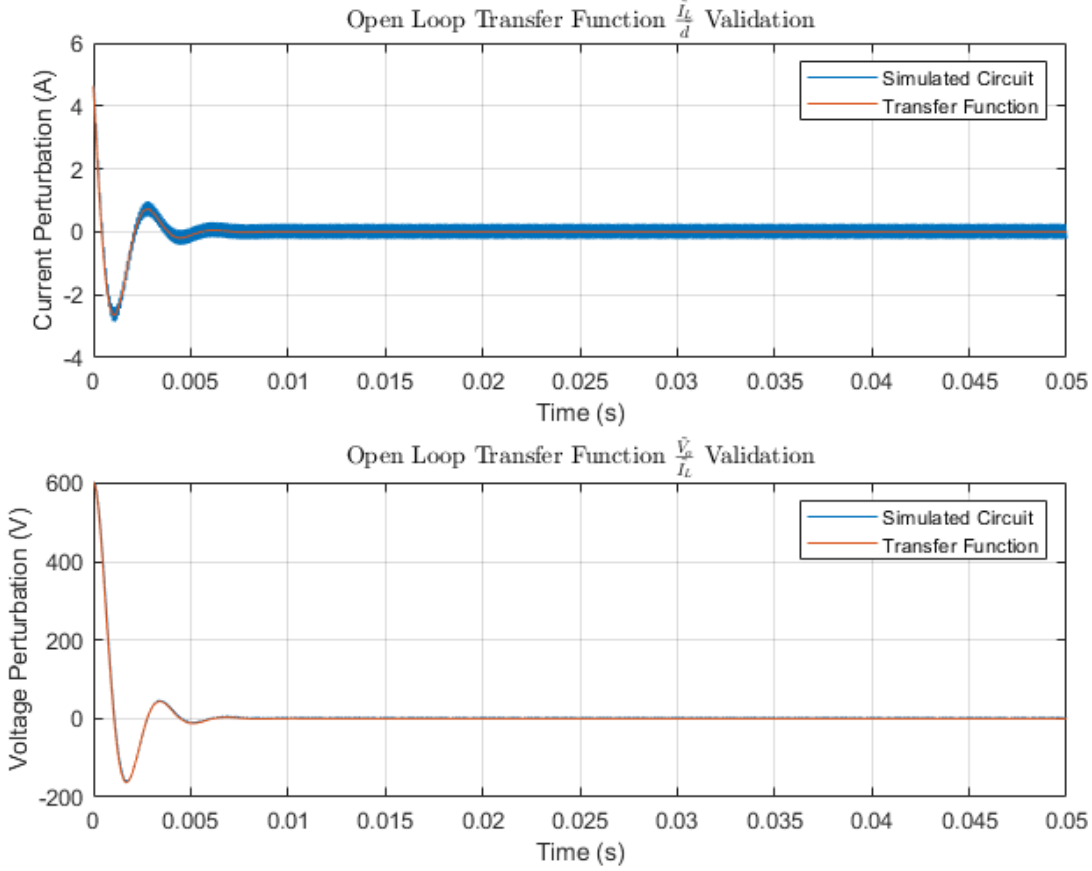

Figure 4.26: Open-loop buck mode transfer function validation

From the figure it is visible that the transfer function correctly represents the simulated electrical circuit of the DC-DC buck converter. Having the open-loop representations, stability analysis and controller design can be done. Pole-zero maps for the validated transfer functions are presented in Figures 4.27 and 4.28

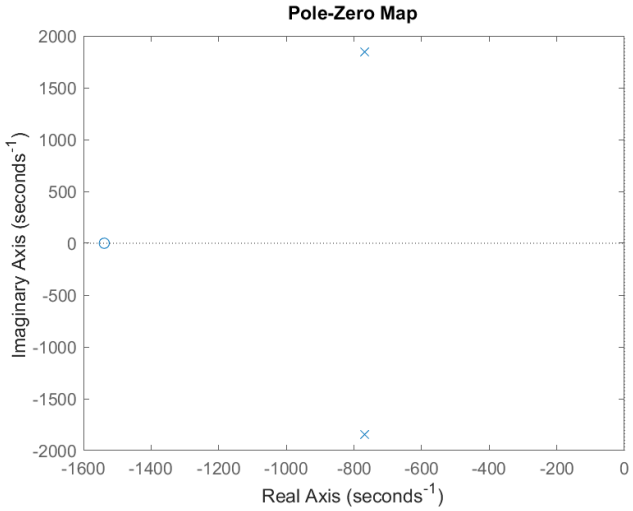

Figure 4.27: Pole-zero map of $\frac{\tilde{I}_L}{\tilde{d}}$

From the pole-zero map, it can be said that the system is stable and exhibits a fast response, due to the poles being far from the origin.

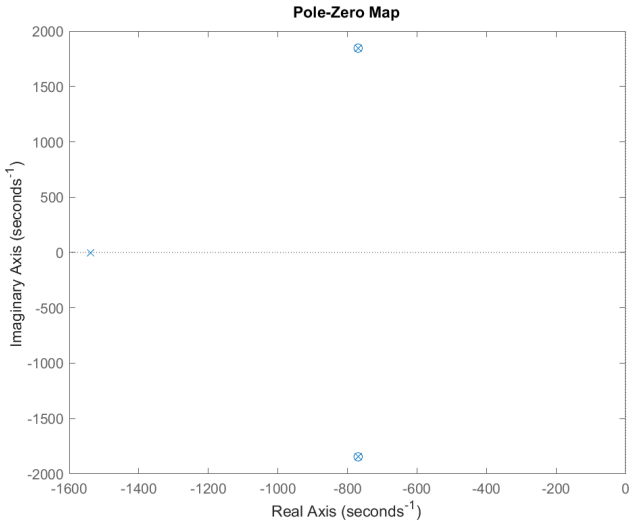

Figure 4.28: Pole-zero map of $\frac{\tilde{V_{SM}}}{\tilde{I_L}}$

The pole-zero map for $\frac{\tilde{V_{SM}}}{\tilde{I_L}}$ as well proves the stability and fast response of the system. Furthermore, pole-zero cancellations occur, which indicate that some transient behaviours of the system may not be visible in the output response. The control utilized for the bidirectional DC-DC converter is presented in Chapter 5.

Boost mode modeling

The modeling of the boost mode follows a similar process to that of the buck mode. When the converter is in boost mode the SW_1 is modeled as a diode and SW_2 is controlled using PWM with duty cycle D visible in Figure 4.21. For the boost mode, the voltage V_{BAT} does not act as a constant voltage source, it acts as a variable voltage source depending on the battery's SOC. The EEC of the boost mode when SW_2 is closed can be seen in Figure 4.29 and when SW_2 is open can be seen in Figure 4.30. The state variable vector and the input vector for the boost mode can be expressed as:

$$\mathbf{x} = \begin{bmatrix} i_L \\ v_{CSM} \end{bmatrix} \mathbf{u} = \begin{bmatrix} v_{BAT} \end{bmatrix} \tag{4.95}$$

The computation of the state equations for the boost mode follows the same process as it does for the buck mode. KVL and KCL are applied for cases when the SW_2 is closed and open.

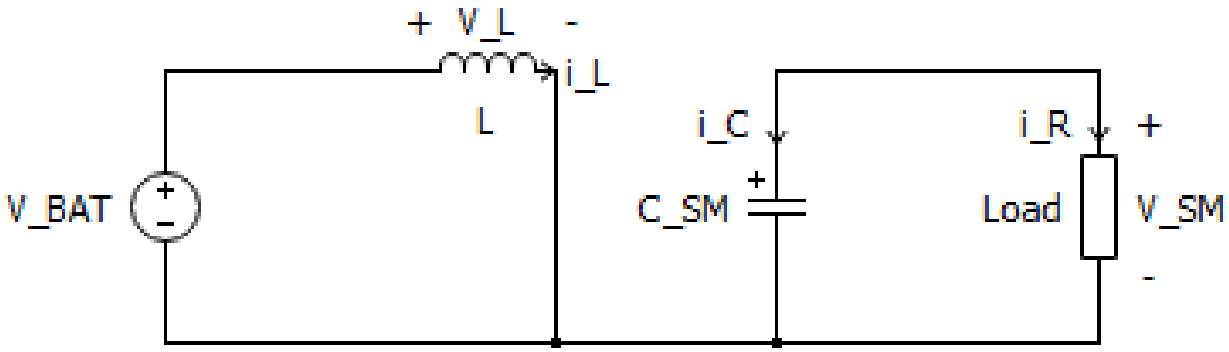

Figure 4.29: EEC of Boost Converter when SW_2 is closed

Applying KVL to circuit in Figure 4.29, yields the equations:

$$v_{BAT} = v_L \tag{4.96}$$

v_L can then be expressed as:

$$v_L = L \cdot \frac{di_L}{dt} \tag{4.97}$$

The equation for $\frac{di_L}{dt}$ can then be solved as:

$$\frac{di_L}{dt} = \frac{v_{BAT}}{L} \tag{4.98}$$

Performing KCL for the loop gives the following expression:

$$i_C = -i_R \tag{4.99}$$

Using Ohms Law and substituting the capacitor current, yields Equation 4.101:

$$C_{SM} \cdot \frac{dv_{CSM}}{dt} = -\frac{v_{CSM}}{R} \tag{4.100}$$

The equation for $\frac{dv_{CSM}}{dt}$ can then be solved as:

$$\frac{dv_{CSM}}{dt} = -\frac{v_{CSM}}{R \cdot C_{SM}} \tag{4.101}$$

Using the derived equations, the state-space representation for when the SW_2 is closed can be formed:

$$\begin{aligned} \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_{CSM}}{dt} \end{bmatrix} &= A_{Boost_1}\mathbf{x} + B_{Boost_1}\mathbf{u} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R \cdot C_{SM}} \end{bmatrix} \begin{bmatrix} i_L \\ v_{CSM} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{BAT} \\ y &= C_{Boost_1}\mathbf{x} + D_{Boost_1} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_{CSM} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} v_{BAT} \end{aligned} \tag{4.102}$$

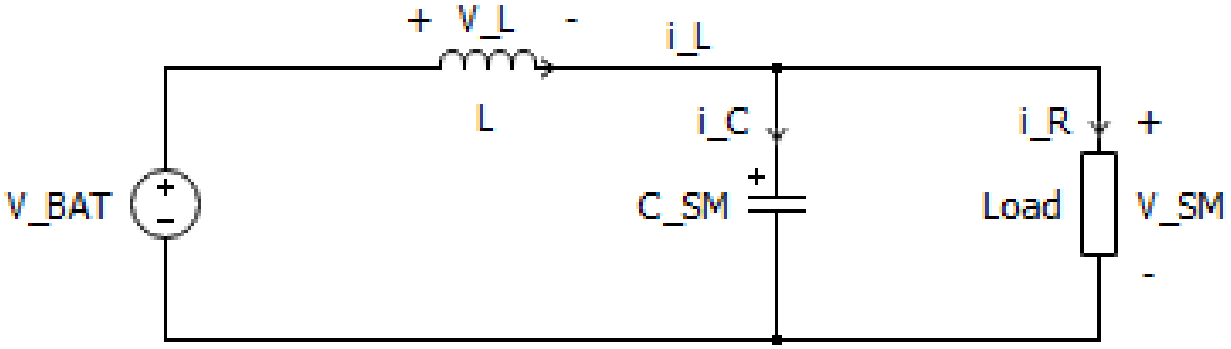

Figure 4.30: EEC of Boost Converter when SW_2 is open

Conducting both KVL and KCL and following the same derivation process for the circuit in Figure 4.30 gives us the state equations for $\frac{di_L}{dt}$ and $\frac{dv_{CSM}}{dt}$:

$$\frac{di_L}{dt} = \frac{v_{BAT} - v_{CSM}}{L} \tag{4.103}$$

$$\frac{dv_{CSM}}{dt} = \frac{i_L}{C_{SM}} - \frac{v_{CSM}}{R \cdot C_{SM}} \tag{4.104}$$

Using the Equations 4.103 and 4.104, state-space representation for when SW_2 is open can be formed.

$$\begin{aligned}\begin{bmatrix}\frac{di_L}{dt}\\ \frac{dv_{CSM}}{dt}\end{bmatrix} = A_{Boost_2}\mathbf{x} + B_{Boost_2}\mathbf{u} = \begin{bmatrix}0 & -\frac{1}{L}\\ \frac{1}{C_{SM}} & -\frac{1}{R\cdot C_{SM}}\end{bmatrix}\begin{bmatrix}i_L\\ v_{CSM}\end{bmatrix} + \begin{bmatrix}\frac{1}{L}\\ 0\end{bmatrix} v_{BAT}\\ y = C_{Boost_2}\mathbf{x} + D_{Boost_2} = \begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}\begin{bmatrix}i_L\\ v_{CSM}\end{bmatrix} + \begin{bmatrix}0\\ 0\end{bmatrix} v_{BAT}\end{aligned} \tag{4.105}$$

State-Space Averaging

The state-space averaging method works in the same principle as it was done in the buck mode. The averaged matrices for the boost mode can be expressed in the following form:

$$\begin{aligned}A_{Boost_{avg}} &= A_{Boost_1}\cdot D + A_{Boost_2}\cdot(1-D)\\ B_{Boost_{avg}} &= B_{Boost_1}\cdot D + B_{Boost_2}\cdot(1-D)\\ C_{Boost_{avg}} &= C_{Boost_1}\cdot D + C_{Boost_2}\cdot(1-D)\\ D_{Boost_{avg}} &= D_{Boost_1}\cdot D + D_{Boost_2}\cdot(1-D)\end{aligned} \tag{4.106}$$

Utilizing Equations 4.102, 4.105 and 4.106, averaged matrices $A_{Boost_{avg}}$, $B_{Boost_{avg}}$, $C_{Boost_{avg}}$, $D_{Boost_{avg}}$ are derived:

$$A_{Boost_{avg}} = \begin{bmatrix}0 & -\frac{1}{L}\\ \frac{1}{C_{SM}} & -\frac{1}{R\cdot C_{SM}}\end{bmatrix} \tag{4.107}$$

$$B_{Boost_{avg}} = \begin{bmatrix}\frac{D}{L}\\ 0\end{bmatrix} \tag{4.108}$$

$$C_{Boost_{avg}} = \begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix} \tag{4.109}$$

$$D_{Boost_{avg}} = \begin{bmatrix}0\\ 0\end{bmatrix} \tag{4.110}$$

The state-space representation is the following:

$$\begin{aligned}\begin{bmatrix}\frac{di_L}{dt}\\ \frac{dv_{CSM}}{dt}\end{bmatrix} = \begin{bmatrix}0 & -\frac{1}{L}\\ \frac{1}{C_{SM}} & -\frac{1}{R\cdot C_{SM}}\end{bmatrix}\begin{bmatrix}i_L\\ v_{CSM}\end{bmatrix} + \begin{bmatrix}\frac{D}{L}\\ 0\end{bmatrix} v_{BAT}\\ y = \begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}\begin{bmatrix}i_L\\ v_{CSM}\end{bmatrix} + \begin{bmatrix}0\\ 0\end{bmatrix} v_{BAT}\end{aligned} \tag{4.111}$$

As with the buck mode modeling, small-signal AC model is constructed and the M and N coefficients are calculated to be:

$$M_{Boost} = \begin{bmatrix}-\frac{V_{BAT}}{L\cdot(D-1)}\\ -\frac{V_{BAT}}{C_{SM}\cdot R\cdot(D-1)^2}\end{bmatrix} \tag{4.112}$$

$$N_{Boost} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{4.113}$$

Final linearized state-space is represented by:

$$\begin{aligned} \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_{CSM}}{dt} \end{bmatrix} &= \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C_{SM}} & -\frac{1}{R \cdot C_{SM}} \end{bmatrix} \begin{bmatrix} i_L \\ v_{CSM} \end{bmatrix} + \begin{bmatrix} \frac{D}{L} & -\frac{V_{BAT}}{L \cdot (D-1)} \\ 0 & -\frac{V_{BAT}}{C_{SM} \cdot R \cdot (D-1)^2} \end{bmatrix} \begin{bmatrix} \tilde{u} \\ \tilde{d} \end{bmatrix} \\ y &= \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ v_{CSM} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \tilde{u} \\ \tilde{d} \end{bmatrix} \end{aligned} \tag{4.114}$$

For purposes of model validation and control, the transfer function of DC-DC converter in boost mode are derived by using the state-space to transfer function formula:

$$\frac{Y(s)}{X(s)} = C_{Boost}(sI - A_{Boost}^{-1})B_{Boost} \tag{4.115}$$

By using the formula, we acquire the transfer functions, that showcase the relationship between the state variables and the inputs, therefore we get a total of 4 transfer functions.

$$\frac{\tilde{I_L}}{\tilde{V_{BAT}}} = \frac{20s + 1.2 \cdot 10^4}{s^2 + 600.6s + 1.29 \cdot 10^6} \tag{4.116}$$

$$\frac{\tilde{V_{CSM}}}{\tilde{V_{BAT}}} = \frac{2.272 \cdot 10^6}{s^2 + 600.6s + 1.29 \cdot 10^6} \tag{4.117}$$

$$\frac{\tilde{I_L}}{\tilde{d}} = \frac{2.113 \cdot 10^4 s + 2.538 \cdot 10^7}{s^2 + 600.6s + 1.29 \cdot 10^6} \tag{4.118}$$

$$\frac{\tilde{V_{CSM}}}{\tilde{d}} = \frac{-1.117 \cdot 10^6 s + 2.4 \cdot 10^9}{s^2 + 600.6s + 1.29 \cdot 10^6} \tag{4.119}$$

The open-loop dynamics of the systems transfer functions $\frac{\tilde{I_L}}{\tilde{d}}$ and $\frac{\tilde{V_{BAT}}}{\tilde{I_L}}$ can be seen in Figure 4.31.

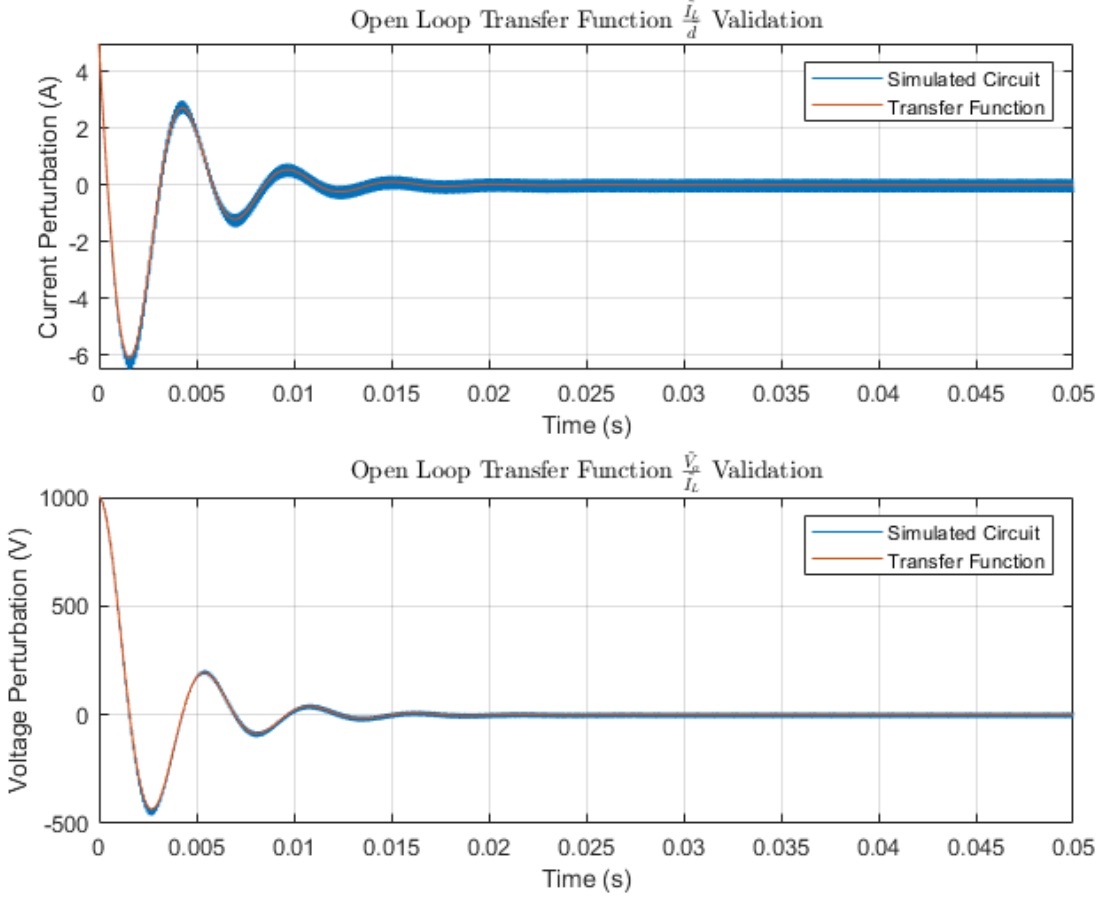

Figure 4.31: Open-loop boost mode transfer function validation

From the open-loop validation, it can be seen that the transfer functions represent the simulated electrical circuit accurately. As with the buck converter, pole-zero maps have been computed for the boost converter. Figures 4.32 and 4.33 represents the pole-zero maps for transfer function $\frac{\tilde{I}_L}{\tilde{d}}$ and $\frac{\tilde{V_{BAT}}}{\tilde{I}_L}$ respectively.

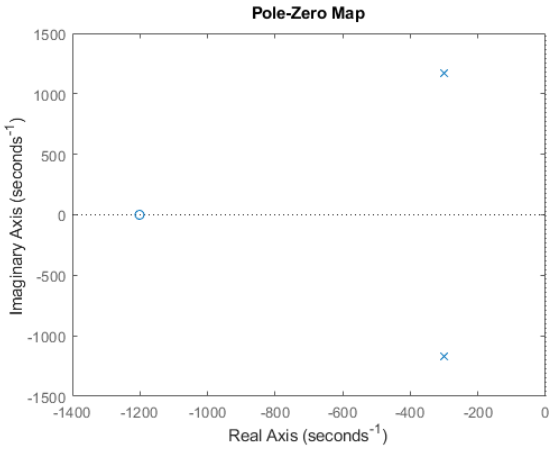

Figure 4.32: Pole-zero map of $\frac{\tilde{I_L}}{\tilde{d}}$

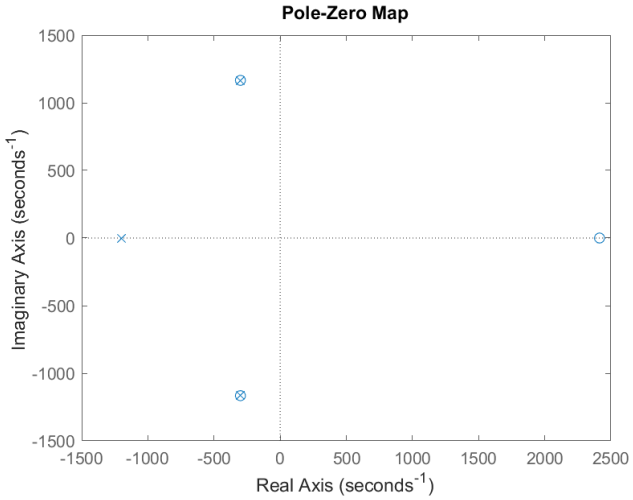

Figure 4.33: Pole-zero map of $\frac{\tilde{V_{BAT}}}{\tilde{I_L}}$

Both transfer function exhibit similar behaviour to that of the buck converter's transfer functions, with a slower response, due to the poles being closer to the origin than that of the buck converter. However, analyzing the pole-zero map in Figure 4.28, it can be seen that the system has a zero on the right-half plane. This indicates a non-minimum phase system, which causes an initial undershoot. To reduce the effect of the undershoot, the control should be designed to respond more slowly.

4.3 Battery Modeling

Battery modeling is crucial for the implementation of the charging/discharging characteristics, SOC estimation, real-time simulation, therefore allowing for a more thorough simulation of the whole system and validation of the bidirectional DC-DC converters CCCV control scheme. Considering that the simulation of the system is complex and computationally heavy, it is important to choose such battery model that would represent the battery accurately and would not be too computationally heavy [36]. To cover the projects topic of utilizing SLBs, comparison between new Li-ion batteries and second-life Li-ion batteries is conducted. The temperature is considered to be constant, therefore the modeling of temperature effects on the battery is omitted.

4.3.1 Li-ion Battery

For the first tests, a healthy Li-ion battery pack has been utilized for each SM of the MMC. Analysis has been performed during battery pack charging/discharging. For the second tests, same procedure has been conducted utilizing a second-life Li-ion battery pack. Parameter estimation for the healthy battery has been conducted using simulated data. To determine the parameters for the second-life battery, it has been assumed to use degradation dynamics of internal resistance R_0 and capacitance Q, acquired from a publicly available dataset [37].

4.3.2 Thevenin Model

The chosen method to model the the Li-ion battery to be used in the complete simulation was using the Equivalent Circuit Model (ECM), specifically a second order Thevenin model [38–40]. This model simplifies the complex internal processes of the battery into an equivalent circuit consisting of easily understandable electrical components. The main components of the Thevenin model include an open-circuit voltage source (E_{OCV}), internal resistance (R_0) and RC networks, consisting of resistance (R_n) and capacitance (C_{pn}). The simulation of the model can be seen in Figure 4.34.

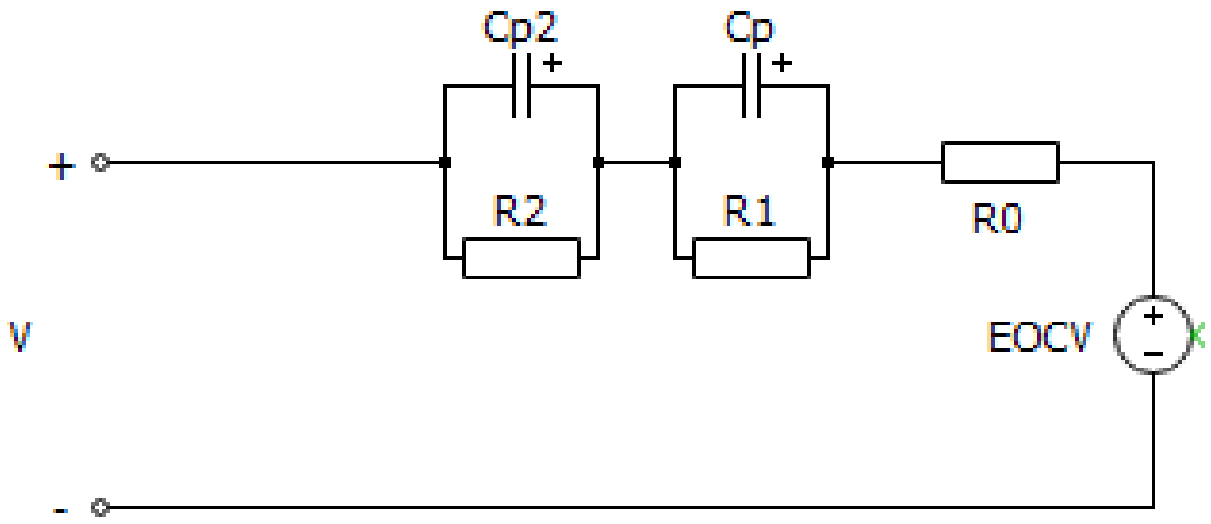

Figure 4.34: Second-order Thevenin model in PLECS

RC network

Two RC networks in the battery model are used to showcase the transient response of the battery. Each of the RC networks consists of resistance R_n and capacitance C_{pn}. Incorporating these components allows the battery model to more closely represent real-life cells behaviour, due to the effects of diffusion voltage and delayed voltage response, that happens because of the electrochemical processes within the battery.

Coulomb counting

For the approximation of SOC, Coulomb Counting method has been used. It works by calculating total amount of charge passing in or out of the battery and integrating the current over time. The calculation is expressed in Equation 4.120.

$$\mathrm{SOC}(t) = \mathrm{SOC}(t_0) + \frac{1}{C}\int_{t_0}^{t} I(t)\,dt \tag{4.120}$$

This method is implemented in the existing PLECS simulation of the battery. The circuit with the added coulomb counting method is presented in Figure 4.35.

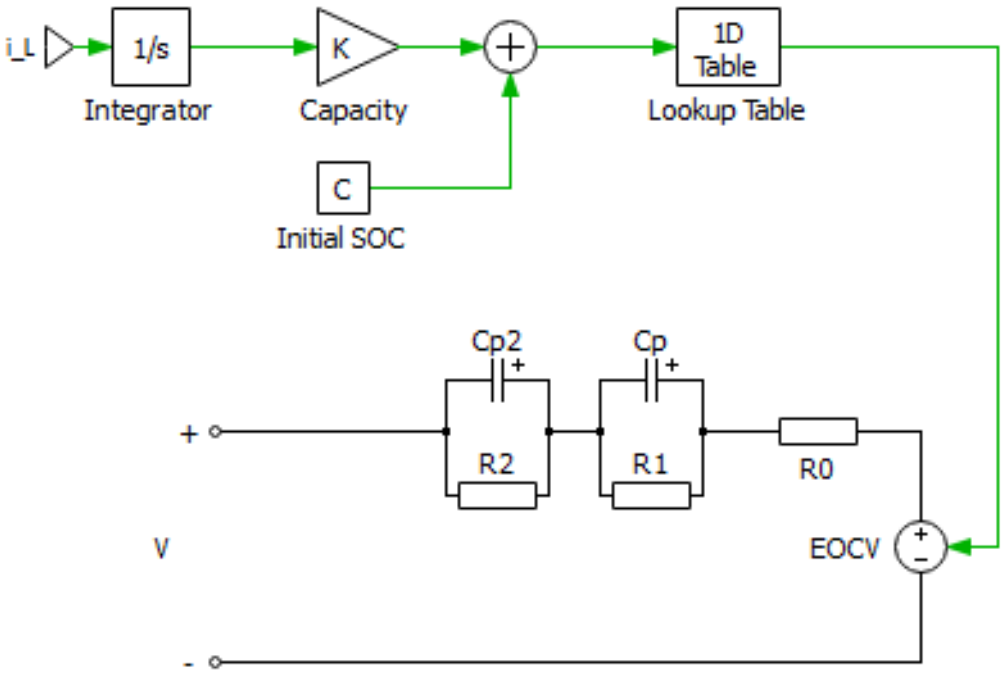

Figure 4.35: Battery model with coulomb counting in PLECS

From Figure 4.35 it is visible that there is an inclusion of a lookup table. The lookup tables maps the SOC to the OCV of the battery. As the relationship of the SOC and OCV is non-linear, it is important to include the lookup table to accurately represent the battery's behaviour.

Degradation profile

For modeling the second-life Li-ion battery, it has been chosen to use a degradation profile to determine the battery's parameters at certain cycle number. As real-life battery data was not available, a degradation profile of internal resistance and capacity has been used for the simulation of the battery data for our case. The degradation profile has been computed by using the data provided in [37]. The chosen data used for fitting is the one that most closely represents the normal operation of the battery, meaning the charging and discharging currents are within the battery's specifications. Using this data two separate polynomial functions are fitted, one representing the change of internal resistance parameter R_0 over cycles and the other representing battery's capacitance Q change over cycles.

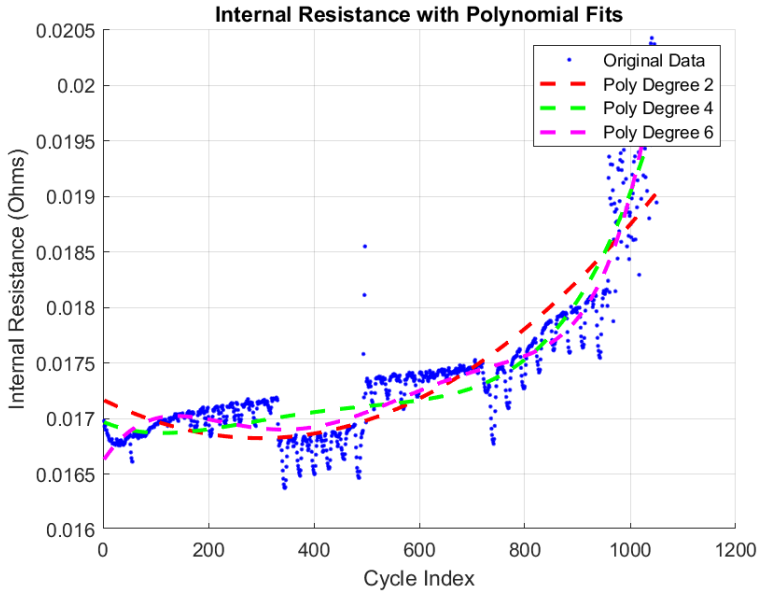

Figure 4.36: Degradation of R_0 with polynomial fits

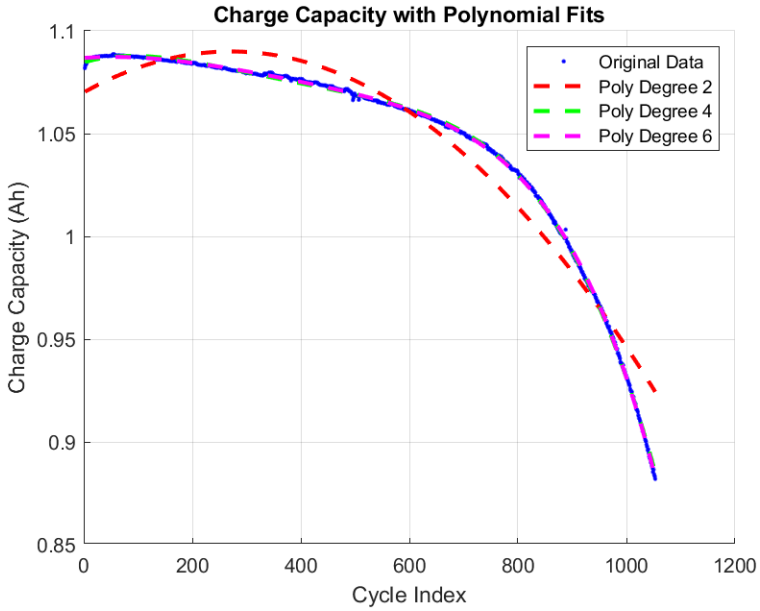

Figure 4.37: Degradation of Q with polynomial fits

The polynomials that were chosen to be used is of 4^{th} order, as there is not a big improvement over the 6^{th} order polynomials. For the degradation profiles to be used in the simulation it has to be normalized so that it represents change of the parameter values from initial parameter value in percentages.

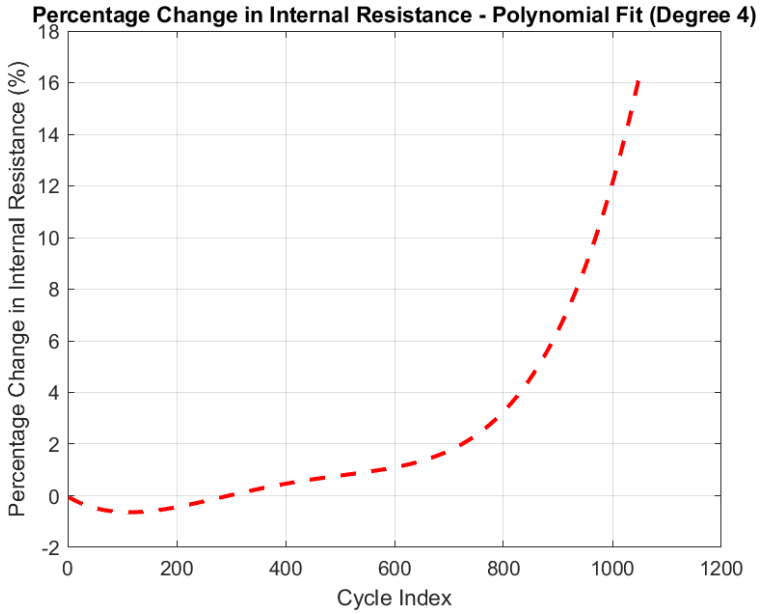

Figure 4.38: Degradation Profile of R_0, 4^{th} order polynomial fit

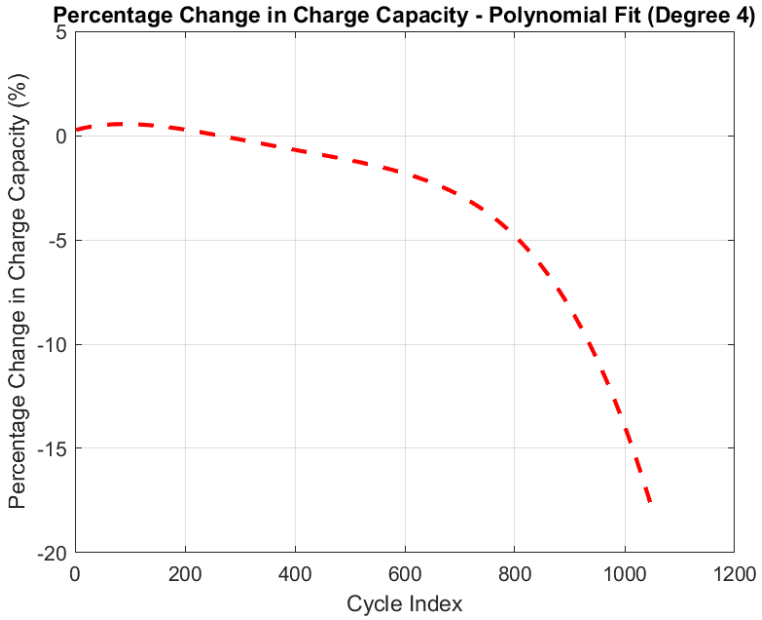

Figure 4.39: Degradation Profile of Q, 4^{th} order polynomial fit

From Figures 4.38 and 4.39 we can see that at end-life the battery's R_0 increases by around 16% and the battery's capacity decreases by around 17%. As the experimental data of the battery test consists of 1052 cycles, it has been decided to scale both how much the parameters degrade, as well as the cycle number, for the use in simulation. The

degradation of the parameters has been increased by 2.5x and the cycle number has been scaled to 40 cycles, fitting the same degradation profile over shorter number of cycles. Figures 4.40 and 4.41 show the scaling of R_0 and Q respectively.

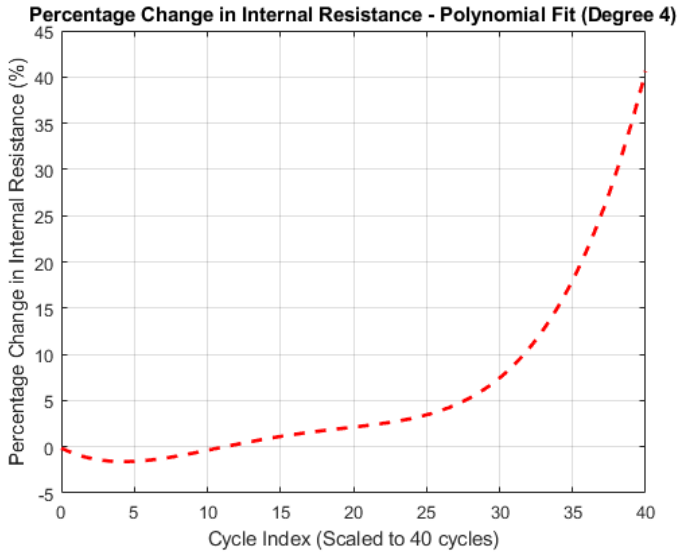

Figure 4.40: Degradation Profile of R_0, 4^{th} order polynomial fit (Scaled)

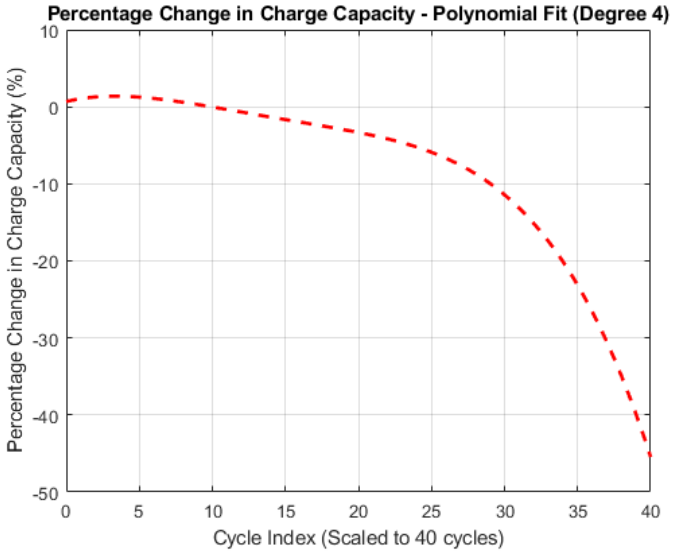

Figure 4.41: Degradation Profile of Q, 4^{th} order polynomial fit (Scaled)

Scaling these degradation profiles allows for accelerated collection of simulation data. Furthermore, scaling the degradation of the parameters allows for a wider range of

change of the parameters, and larger parameter selection at different SOH. For second-life batteries, the useful SOH range is around 80% - 60% [41]. For simplicity, we assume the degradation profile of R_0 for the RC network resistances R_1 and R_2 and no degradation profile for parameters C_p and C_{p2}.

Data acquisition for parameter identification

For this project, the data used for parameter identification was simulated to represent a real-life battery cell. The data collected from the simulation includes V_{OCV}, I and SOC. Pulse charge and discharge test simulation is conducted over a set number of cycles, which is defined to be 40 cycles. The process of the battery test can be explained by the flowchart in Figure 4.42 and the simulation environment can be seen in Figure 4.43.

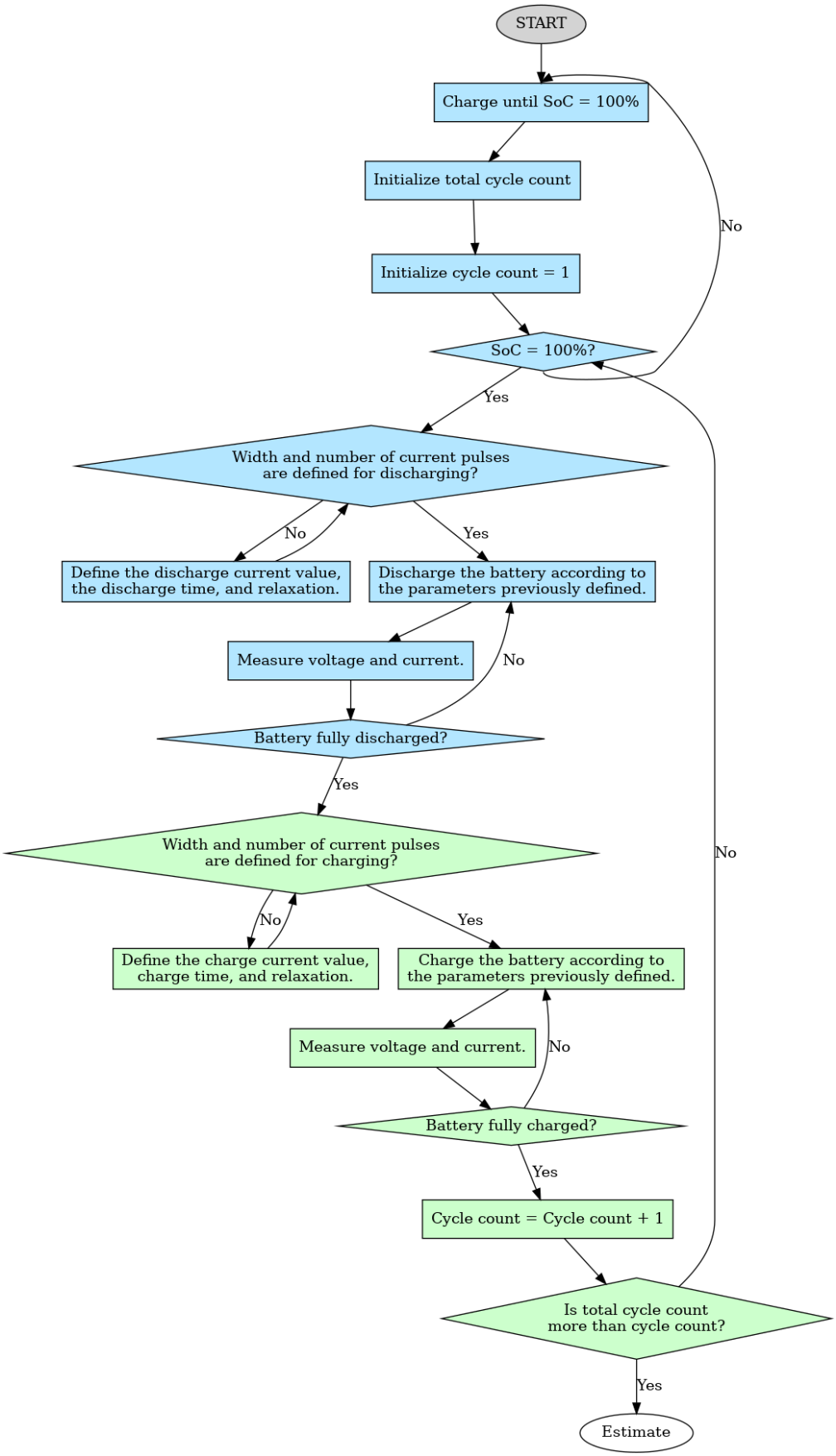

Figure 4.42: Flowchart of the data acquisition process

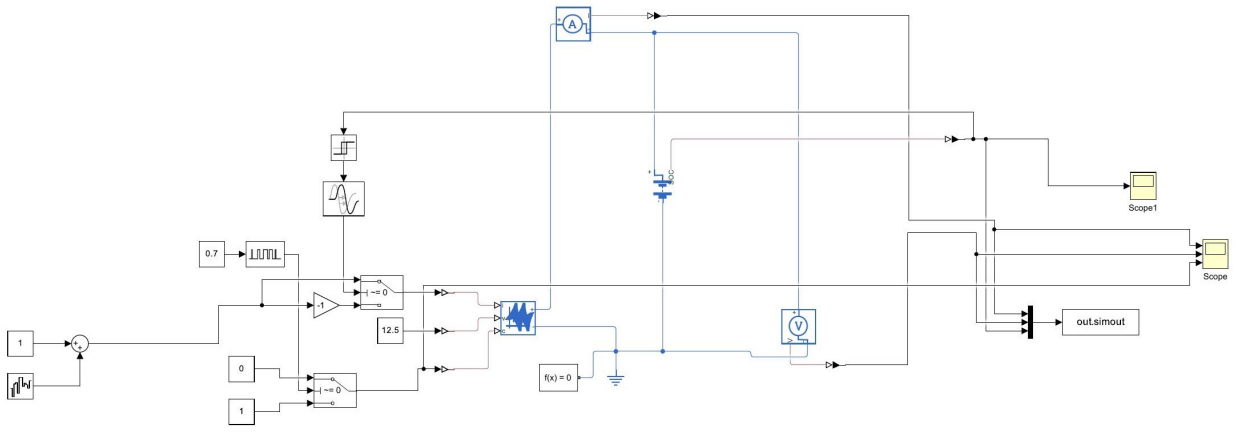

Figure 4.43: Battery Testing Environment Simulation

At the start of the data acquisition, it is made sure that the battery starts at 100% SOC, then the total cycle count is initialized based on the simulation run time. The battery is discharged at 1A with some additional small variations added from the random noise block. The width and number of current pulses are defined using the PWM block and a constant value block that acts as duty cycle. The PWM is set to have period of 600s, meaning that the current pulse width is 180s. The cycler block essentially acts as a galvanostat, providing a set current to the battery, depending on the PWM signal. The relay and transport delay blocks are used to reduce the simulation errors at SOC points of 100% and 0%. As the simulation runs and the cycle number increases, it can be observed that the current pulse width decreases. This could be explained by the degradation of the battery's capacitance Q, causing the battery to fully charge and discharge faster. After every pulse the battery is in a 'rest period' until the next pulse. One cycle can be defined as a full discharge and a full charge, which can be seen in Figure 4.44. The data acquisition process continues until it reaches the defined total cycle count.

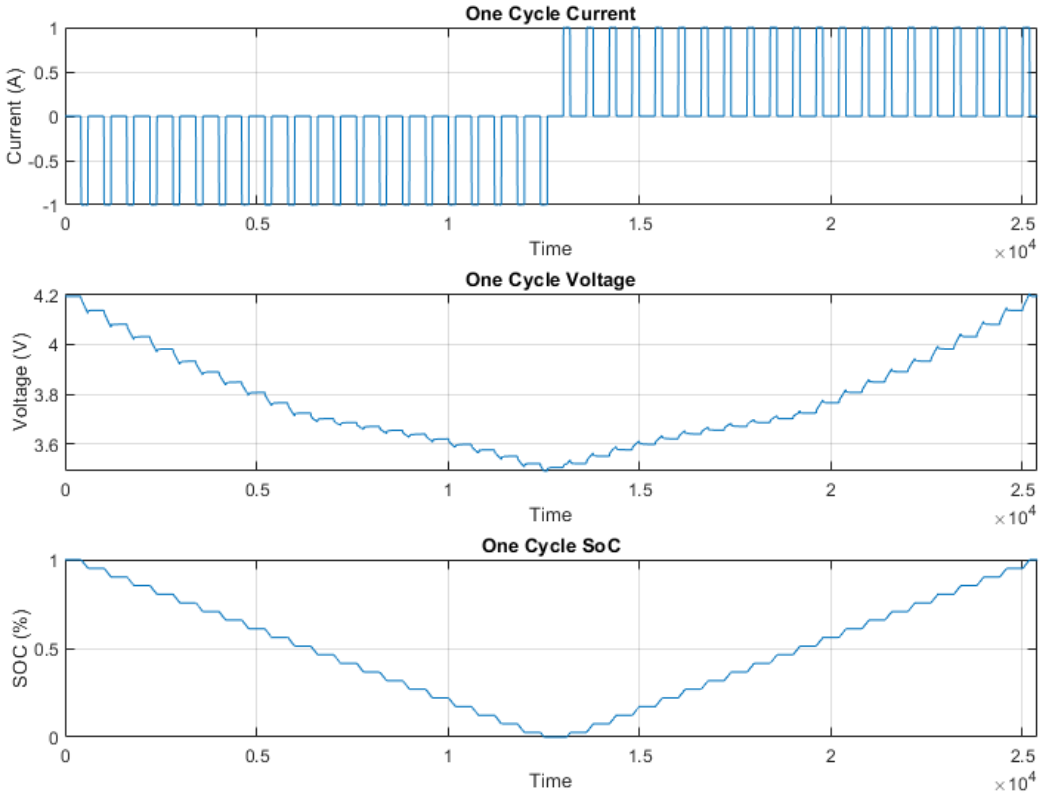

Figure 4.44: Current, Terminal Voltage and SOC over one cycle

It should be noted, that as the data has been collected through simulation, the pulse charge and discharge test does not reflect the time it would take to conduct this test in real-life. The parameters of the battery used for simulation are provided in Table 4.8.

Parameter	Value
Nominal Voltage	3.71V
Min - Max Voltage	3.49 - 4.19V
Charge - Discharge Current	1A
Capacity	1Ah

Table 4.8: Simulated battery parameters

Parameter identification

There are various methods used for obtaining battery model parameters, such as by using Unscented Kalman Filter, Genetic Algorithm, Particle Swarm Optimization [42,

43]. For the thesis it has been decided to use parameter identification based on the Layering Technique [44–46]. The parameter identification is done for internal resistance of the battery R_0, and identification of RC parameters V_1, V_2, τ_1 and τ_2. A MATLAB code has been created for the identification of the parameters. Functions from Optimization Toolbox have been used for the fitting [47]. The high-level flowchart of the code can be seen in Figure 4.45.

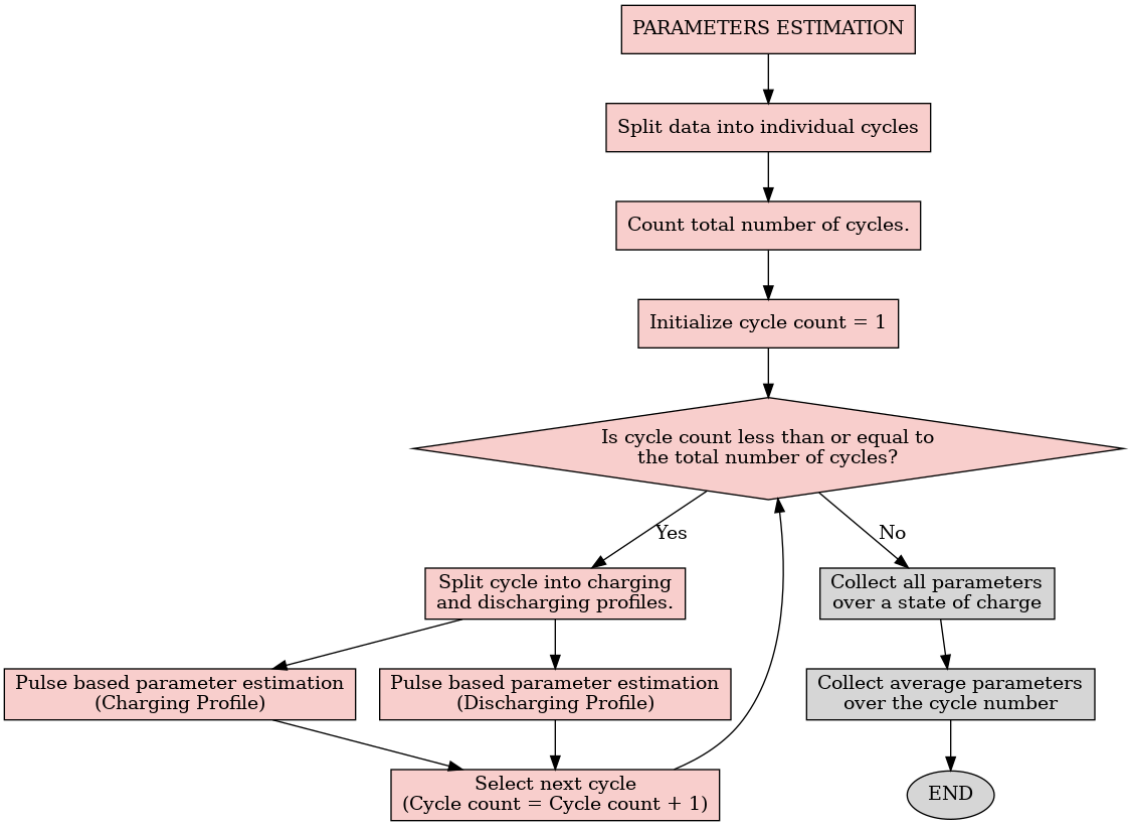

Figure 4.45: Parameter Identification Flowchart

The collected data is first split into individual cycles. After the splitting is finished, the total number of cycles is counted and the first cycle is initialized. The code checks if the cycle count is less than or equal to the counted total cycles, if the logic is positive, it continues into the next part of the code, where the cycles are then split into separate charging and discharging profiles. In Figure 4.46, the the parameter estimation of the discharging profile flowchart can be seen.

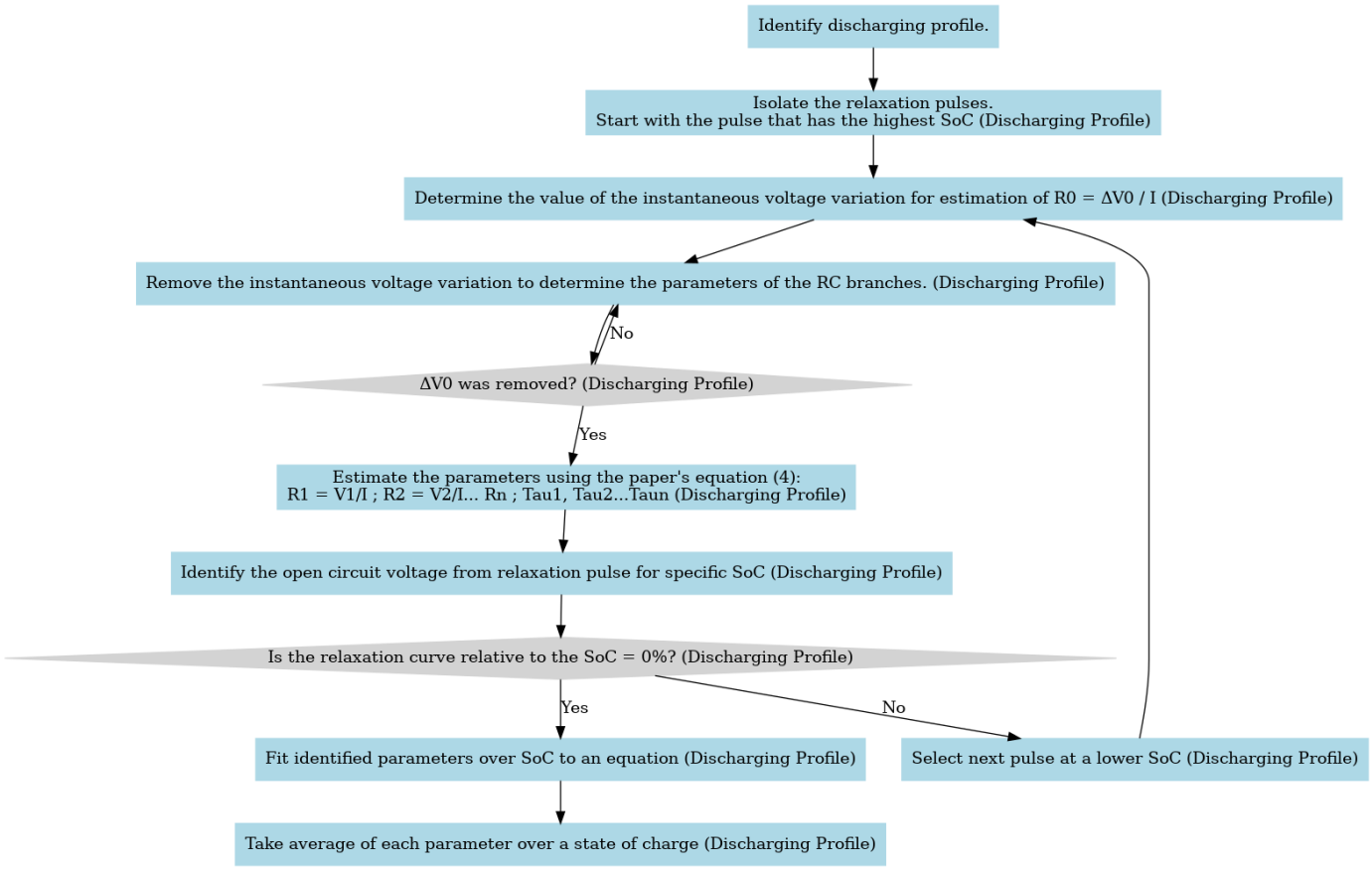

Figure 4.46: Discharging Profile Parameter Estimation Flowchart

First step in the code, is to identify the discharging profile. The V_{OCV}, I and SOC plot of the discharging profile can be seen in Figure 4.47.

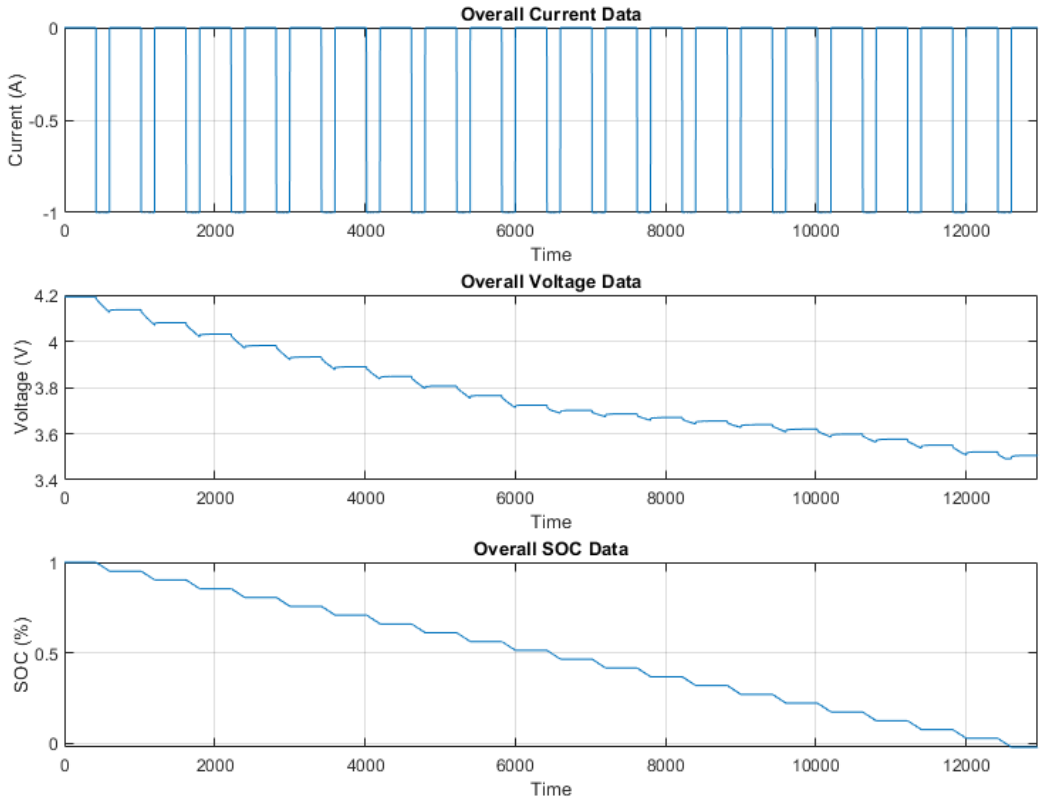

Figure 4.47: Discharge Profile of the collected data

From this data, the algorithm then isolates individual resting pulse periods from the whole profile. The resting pulses provide important information about V_{OCV} and the battery's dynamics at given SOC points. Figure 4.48, provides a closer look of the resting pulse V_{OCV} and I.

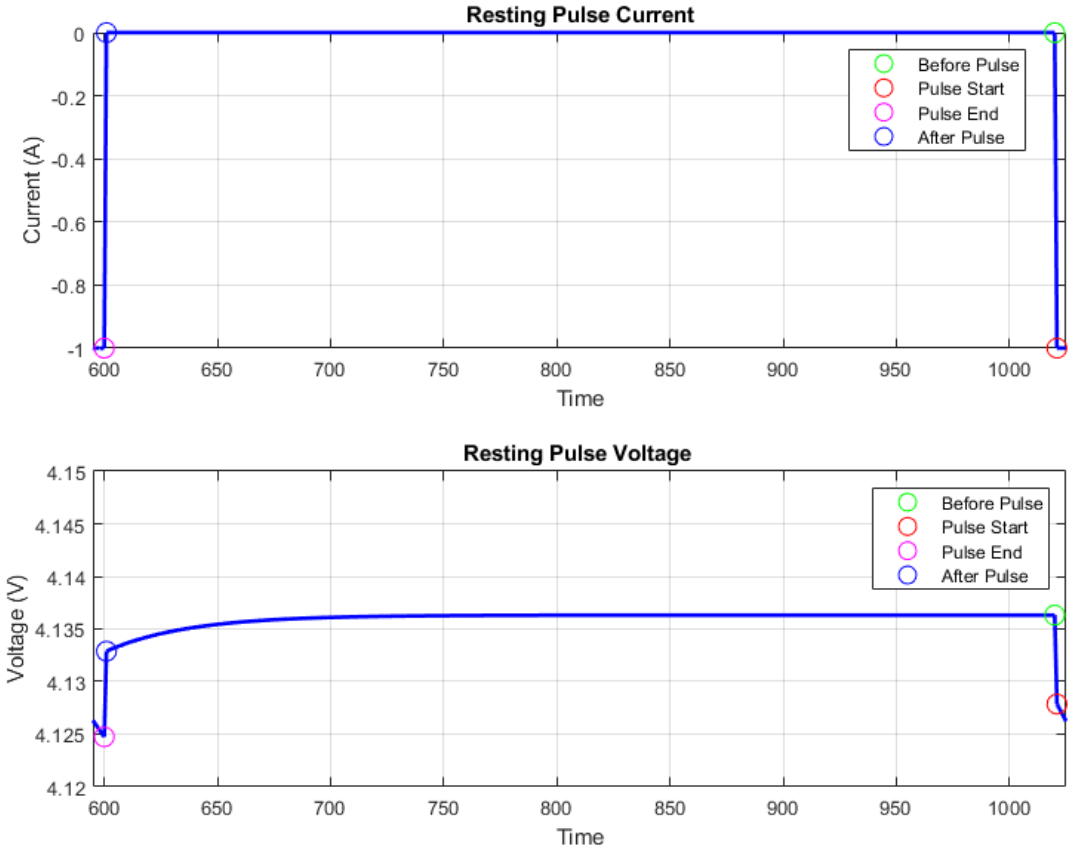

Figure 4.48: Individual Resting Pulse V_{OCV} and I

The code then determines different points of the pulse, these being $before\_pulse\_start$, $pulse\_start$, $pulse\_end$ and $after\_pulse\_end$. The resting period shows how the battery's V_{OCV} reacts after the current I pulse has ended. It provides us information on how parameters R_0, V_1, V_2, τ_1 and τ_2 affects the dynamics of the battery. The instantaneous responses, shown in Figure 4.49 is caused by internal resistance R_0, which is he opposition to the flow of current within the battery. This resistance causes a voltage drop that is proportional to the current flowing through the battery.

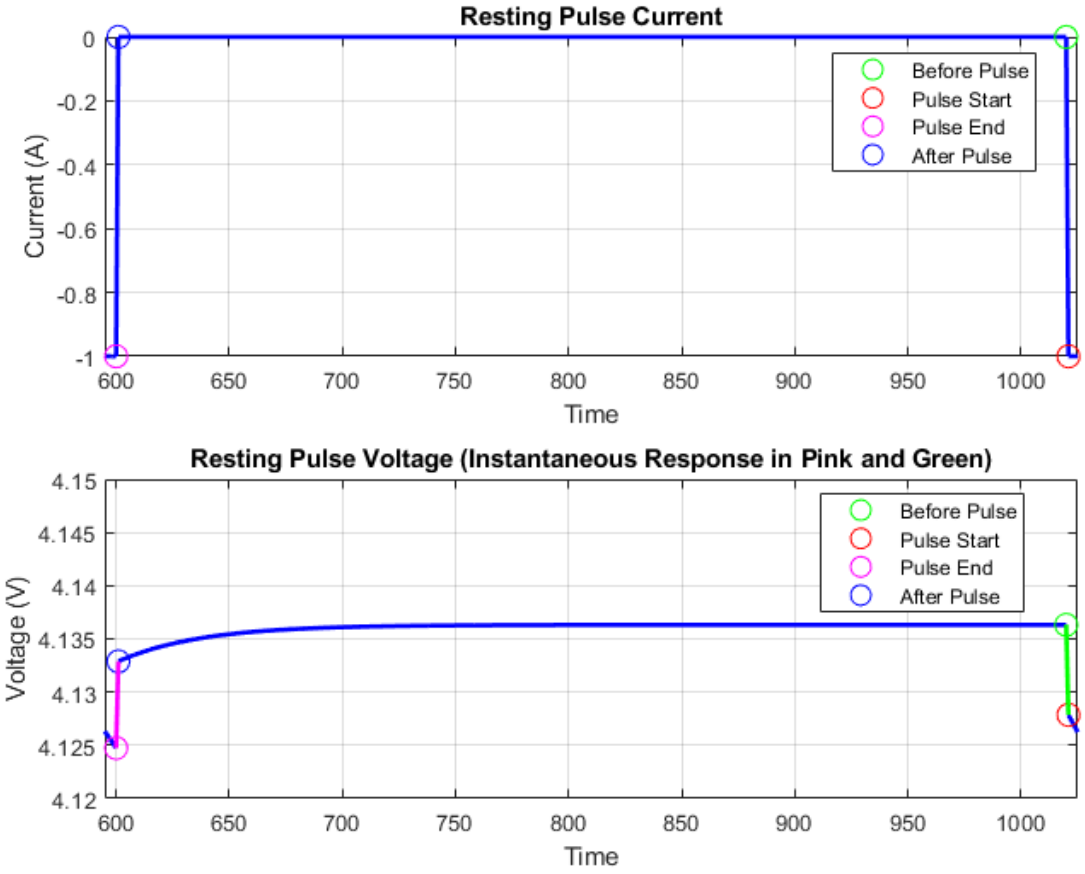

Figure 4.49: Individual Resting Pulse V_{OCV} and I (Instantaneous Response Highlighted)

The estimation of R_0 is done by computing:

$$R_0 = \frac{\Delta V}{I} \tag{4.121}$$

The computation is done at every SOC point for every cycle. Identifying R_0 across the cycles, allows us to use the values for modeling the second-life Li-ion, as well as validating the degradation profile. After the computation of R_0, the ΔV_0 is removed. This is done to isolate the transient response of the V_{OCV}, which is used for RC network parameter identification. Therefore, by isolating this response, the fitting of the RC network parameters is not influenced or skewed by the instantaneous response, represented by R_0. The transient response can be seen in Figure 4.50.

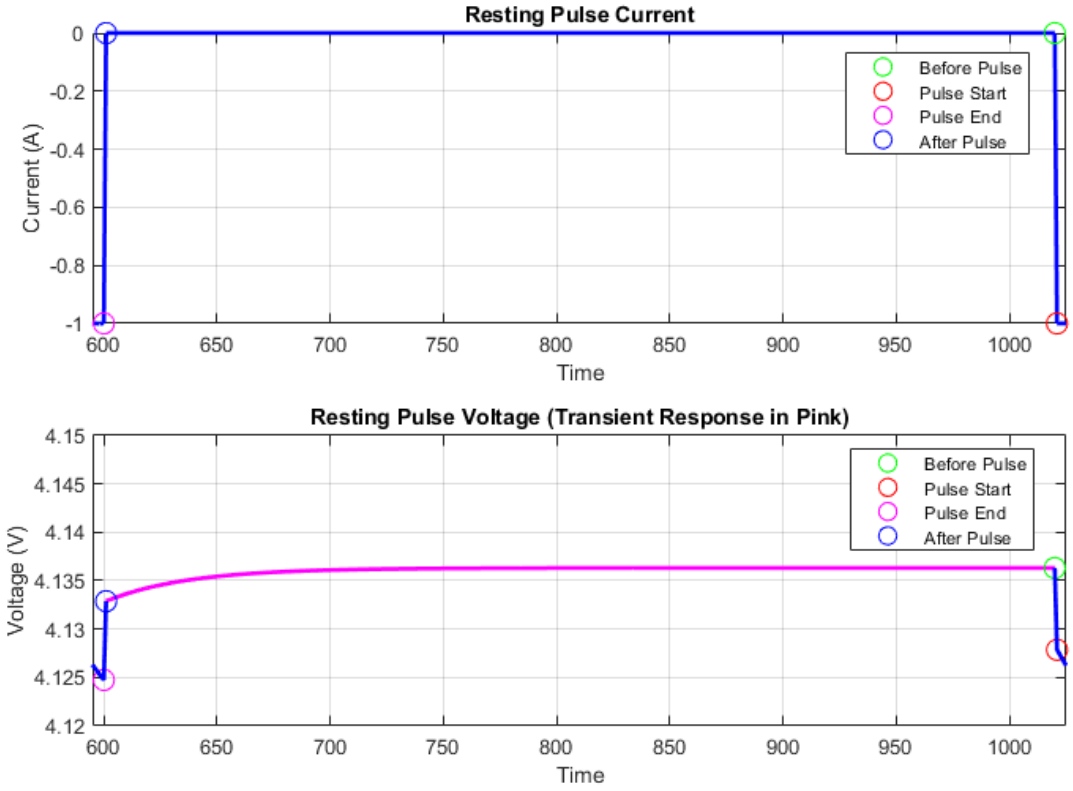

Figure 4.50: Individual Resting Pulse V_{OCV} and I (Transient Response Highlighted)

Fitting of the parameters V_1, V_2, τ_1 and τ_2 is done using an exponential function, presented in Equation 4.122.

$$V(t) = V_1 \cdot (1 - e^{\frac{-t}{\tau_1}}) + V_2 \cdot (1 - e^{\frac{-t}{\tau_2}}) \tag{4.122}$$

For the successful fitting of the transient response curves, the bounds for V_1 and V_2 had to be chosen carefully. Setting the V_1 and V_2 bounds to be $\frac{\Delta V_1}{2}$ and $\frac{\Delta V_2}{2}$ respectively does not provide us with sufficient fitting of the curves, this could indicate that the bounds set are too constrained, potentially causing the solutions to get stuck in local minima. However, adding additional buffer to the bounds allows for the model to be fitted more accurately and allows the solutions to navigate towards an optimal global minima. In Figure 4.51, the bound selection is shown.

$$\Delta V_{RC_{sum}} = (\Delta V_{RC_1} \pm \Delta V_{RC_1}\%) + (\Delta V_{RC_2} \mp \Delta V_{RC_2}\%)$$

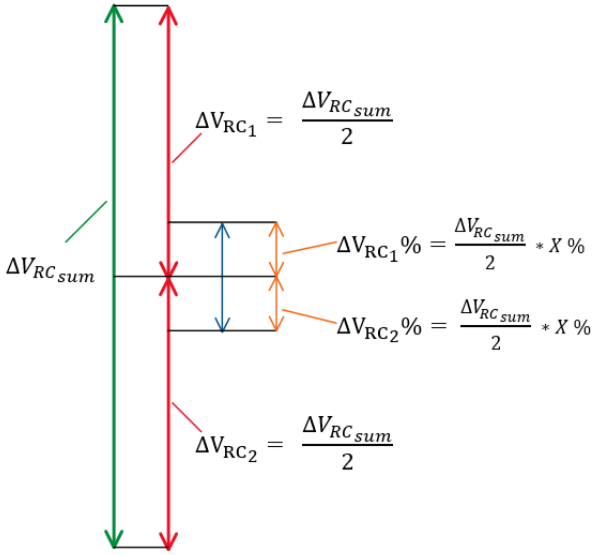

Figure 4.51: ΔV_{RC_1} and ΔV_{RC_2} lower bound selection

Where $\Delta V_{RC_{sum}}$ represents the total voltage change that occurs during the resting period (transient response). The voltage contributions from the RC components are represented by ΔV_{RC_1} and ΔV_{RC_2}. The sum of these two components would be equal to $\Delta V_{RC_{sum}}$. $\Delta V_{RC_1}\%$ and $\Delta V_{RC_2}\%$ represent the additional percentage buffer. Figure 4.52 shows the fitting for the transient response data of the battery.

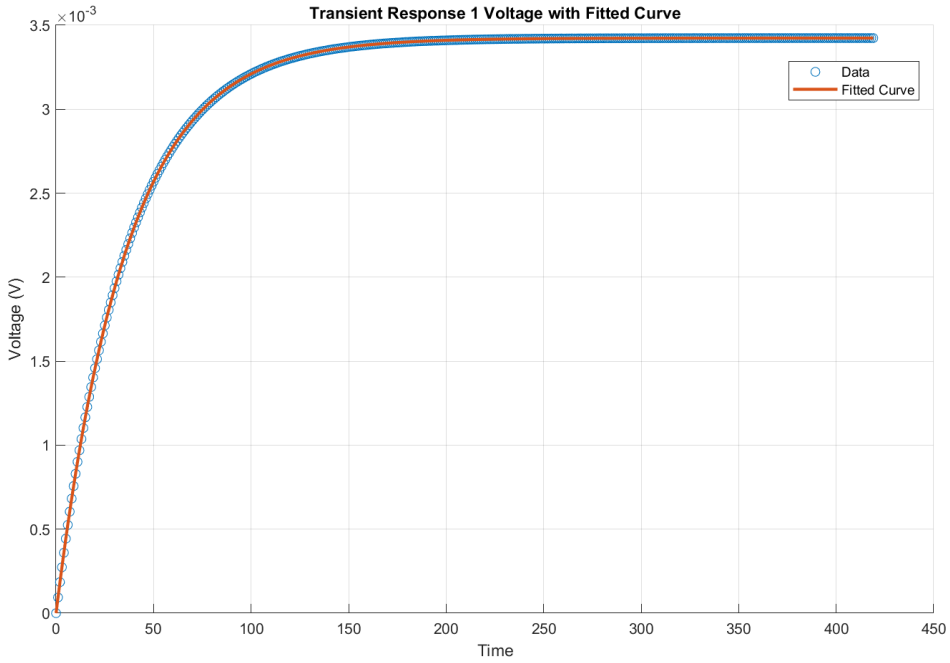

Figure 4.52: Curve Fitting of the 2-RC Transient Response

It can be seen that the data has been fitted accurately, meaning that the selected function, bounds and the RC network count is sufficient. Parameters V_1, V_2, τ_1 and τ_2 are fitted for each resting pulse, for specific SoC points at each cycle. For the parameters to be used in a Thevenin model, they should be represented as passive components R_1, R_2, C_p and C_{p2}. By using the following Equations 4.123 and 4.124, these component values are calculated.

$$R_1 = \frac{V_1}{I} \quad \text{and} \quad R_2 = \frac{V_2}{I} \tag{4.123}$$

$$C_p = \frac{\tau_1}{R_1} \quad \text{and} \quad C_{p2} = \frac{\tau_2}{R_2} \tag{4.124}$$

Figure 4.53 shows the surface plot of the R_0 resistance across different SoC points over the total amount of cycles.

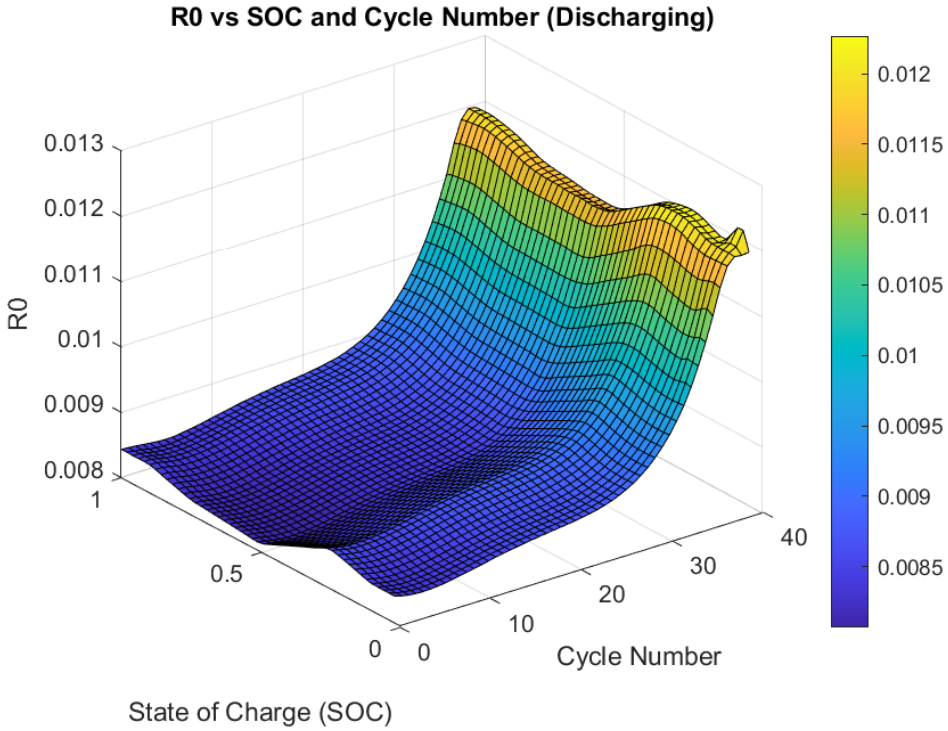

Figure 4.53: R_0 parameter over SoC and Cycle Number (Discharging)

It is clear from the plot that the parameter R_0 degrades following a similar degradation profile shown in Figure 4.36. For a more clear view of identified R_0 degradation, the actual degradation profile is overlaid, which can be seen in Figure 4.54

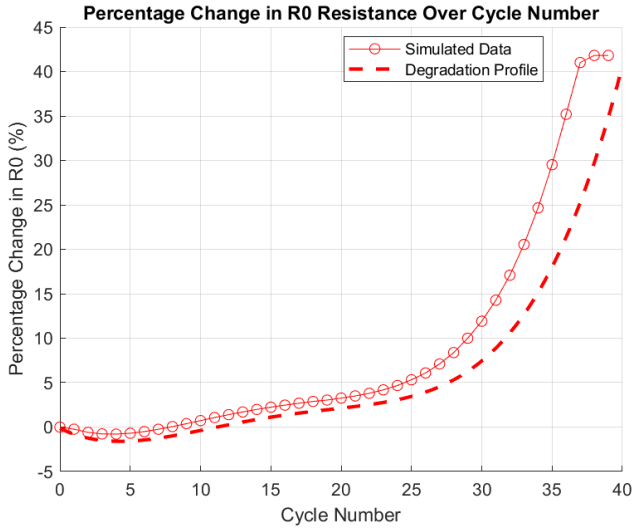

Figure 4.54: Comparison of identified R_0 degradation with the degradation profile

It can be seen that the degradation of the parameter R_0 does not exactly follow the degradation profile. This could be caused by the way the simulation data is collected and the cycling algorithm. As the current pulse width and number of pulses are not identical to the degradation experimental data.

Figures 4.55, 4.56, 4.57 and 4.58 represent the RC parameter change across different SoC points over the total number of cycles.

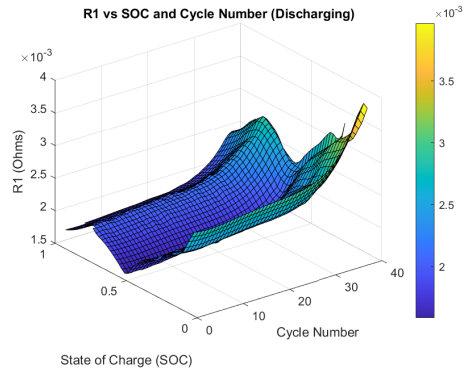

Figure 4.55: R_1 parameter over SoC and Cycle Number (Discharging)

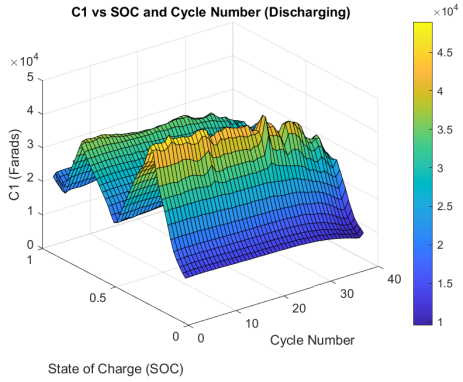

Figure 4.56: C_p parameter over SoC and Cycle Number (Discharging)

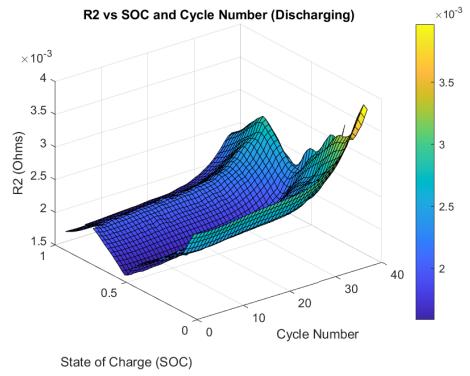

Figure 4.57: R_2 parameter over SoC and Cycle Number (Discharging)

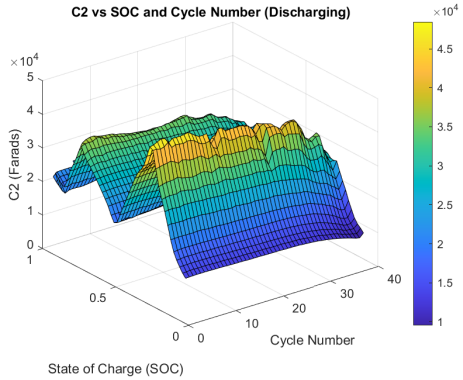

Figure 4.58: C_{p2} parameter over SoC and Cycle Number (Discharging)

By analyzing these plots we can extract the parameters to be used for the battery scaling, presented in the next sub section.

The procedure for the charging profile follows a similar algorithm, therefore it has been decided to not describe it further in this section. The figures for the charging profile can be seen in Appendix C. Furthermore, the parameters estimated from both discharging and charging profiles match, therefore no further analysis has been done for the charging profile.

Scaling

Scaling could be done by calculating the component value changes based on series and parallel connections of the individual batteries [48, 49]. For the project, it has been decided to use 600V / 5A battery packs within the submodules of the MMC. As the individual cells used in simulation have a nominal voltage of 3.71V and the capacity is 1Ah, calculations for series and parallel connections are made. Equation 4.125 shows the calculation to determine the number of cells required to be connected in series. To determine the amount of parallel strings needed, Equation 4.126 is used.

$$N_s = \frac{600V}{3.71V} \approx 162 \; cells \tag{4.125}$$

$$N_p = \frac{5A}{1A} = 5 \; cell \; strings \tag{4.126}$$

It can be seen from the calculations, that it is required to connect 162 cells in series, and have 5 parallel strings to obtain a battery pack that is rated for 600V / 5A. Equation 4.127, is used to calculate the total amount of cells required for such battery pack.

$$N_{tot} = N_s \cdot N_p = 820 \; cells \tag{4.127}$$

To scale the identified parameters, Equations 4.128 and 4.129 can be used.

$$R_{0_{pack}} = \frac{162 \cdot R_0}{5} \quad ; \quad R_{1_{pack}} = \frac{162 \cdot R_1}{5} \quad ; \quad R_{2_{pack}} = \frac{162 \cdot R_2}{5} \tag{4.128}$$

$$C_{p_{pack}} = \frac{C_p \cdot 5}{162} \quad ; \quad C_{p2_{pack}} = \frac{C_{p2} \cdot 5}{162} \tag{4.129}$$

Parameter extraction for main simulation

Having all the parameters identified and scaled, they can be extracted and used in the main simulation, where a Thevenin model is utilized within each of the submodules of the MMC. Technically, as the parameters are identified across 40 SOC points and over 40 cycles, variable components could be used in the Thevenin model. This approach could enable a more detailed simulation with parameters changing across different SOC points and cycles. However, due to the main simulation already being complex and having limited runtime, such in-depth simulation is not possible. Having this constraint, it has been decided to extract the parameters only at 50% SOC point. In MATLAB, the parameters for the 50% SOC point have been isolated over the 40 cycles, giving us a 1x40 array, where the row represent the parameter value at 50% SOC point and the column represents the cycle number. Extracting parameters in such way lets us to easily change the parameters within the main simulation. This allows us to split the simulation into two cases, test with healthy batteries (parameters at cycle 1) and test with second-life batteries (parameters at cycles ranging between 20-35).

4.4 Submodule Model

The PLECS model, representing a single MMC submodule can be seen in Figure 4.59. The model is comprised of three circuits, these being the MMC-side half-bridge, explained in Section 4.1.1, the bidirectional DC-DC converter, explained in Section 4.2.1 and the Thevenin model of the battery pack, explained in Section 4.3.

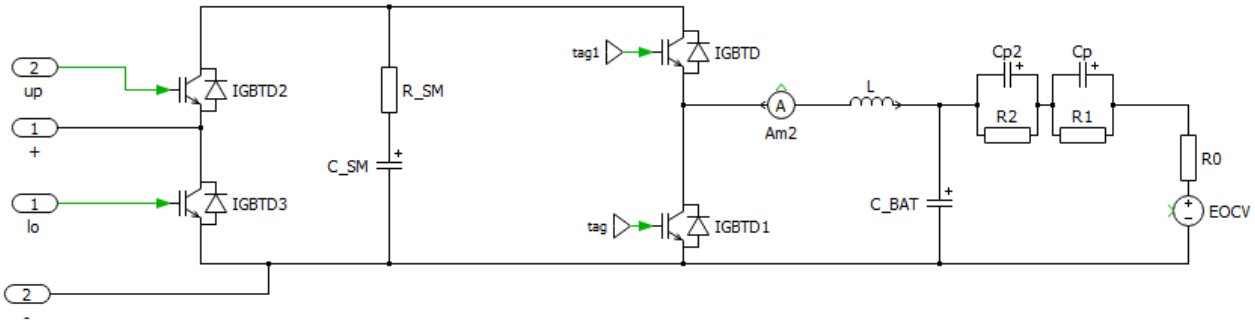

Figure 4.59: Submodule simulation in PLECS

Chapter 5

Control

In this chapter control of the system is defined. The chapter is distributed into 4 sections: definition of overall control layers, MMC control, battery charge/discharge control and finally battery control for MMC integration.

5.0.1 Definition of Control Layers

The control layers of MMC are upper and lower level control layers. The lower control layer associated with the modulation techniques, circulating current suppression and capacitor voltage balancing. The upper control layer is responsible for MMC output current control, active/reactive power control, AC voltage as well as DC voltage control and other control methodologies related to generating the reference value for the MMC output current controller.

Battery control layer is mainly a separate layer from MMC layers. Battery control layer is responsible for output current and voltage regulation, constant-current constant-voltage protocol for battery charging/discharging as well as other mechanisms to ensure the protection of the battery operation.

The layer of battery control for MMC integration is associated with control mechanisms that use the information from both battery side and MMC side. Methods such as SOC balancing among phases/arms/submodules as well as capacitor voltage feed-forward compensation for battery current hold a crucial role to ensure safe and correct operation of battery integrated MMC system.

Additionally, considering that the scope of the project is integration of SLBs into MMC, which encompasses numerous different systems and controllers, only manual controller tuning is applied to all of the controllers mentioned in this chapter. There should be further investigation on optimal controller gain selection to enhance the system performance, however, due to time constraints, manually selected controller gains are assumed to be sufficient for initial stage of the control system development. After the successful integration of different control layers, the focus should be given to finding

optimal control gains for system performance enhancement.

5.0.2 Control of Modular Multilevel Converter

Output Current Control

Current control in MMCs is crucial for regulating the power flow, maintaining voltage stability, and ensuring overall system operates within its desired performance specifications. The voltages and currents of MMC are time-varying variables, which can be difficult to control. To simplify analysis and control, time-varying variables in stationary abc frame can be transformed to DC variables in synchronous dq reference frame. The dq reference frame is a rotating frame aligned with the grid voltage vector. Direct axis (d component) represents real power or active component whereas quadrature axis (q component) represents reactive power or reactive component. The transformation of abc frame to dq frame allows the usage of linear control methods such as PI controllers. PI controllers can be developed for each current component. The control laws for d and q components of current can be expressed as [23]:

$$v_d^* = K_{p,d}(i_d^* - i_d) + K_{i,d}\int (i_d^* - i_d)\,dt - \omega\left(L_T + \frac{L_S}{2}\right) i_q \tag{5.1}$$

$$v_q^* = K_{p,q}(i_q^* - i_q) + K_{i,q}\int (i_q^* - i_q)\,dt + \omega\left(L_T + \frac{L_S}{2}\right) i_d \tag{5.2}$$

Current controller in dq frame is shown in Figure 5.1. It can be seen that controller consists of PID controllers with cross-coupling and feedforward terms. The selection of controller gains is shown in Table 5.2. Controllers gains were selected to ensure fast tracking with no steady-state error and minimal overshoot. Reference tracking performance of output current control is shown in Figure 5.2. It can be seen that controller is capable of tracking reference with no steady-state error with only a slight overshoot. Furthermore, dashed lines indicate the interaction between d and q components during the control sequence. When d component has a change in reference, not only the signal for d component changes but also the q component signal experiences a slight over/under-shoot. Nonetheless, both controllers are capable of tracking reference with no steady-state error.

Parameter	Gain
$K_{p,d}$	0.001
$K_{p,q}$	0.001
$K_{i,d}$	1000
$K_{i,q}$	1000

Table 5.1: Proportional and integral gains for dq controller

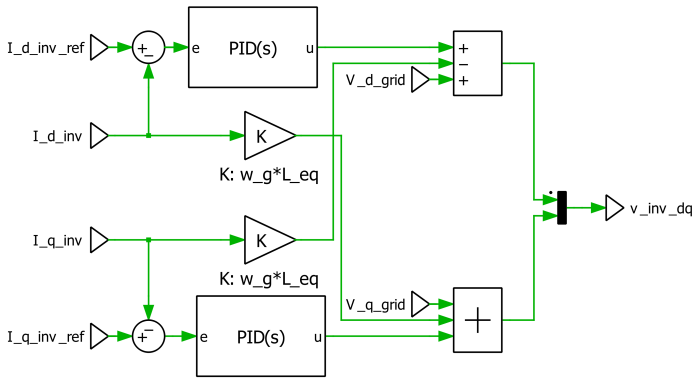

Figure 5.1: Output current controller in dq-frame with cross-coupling and feedforward terms.

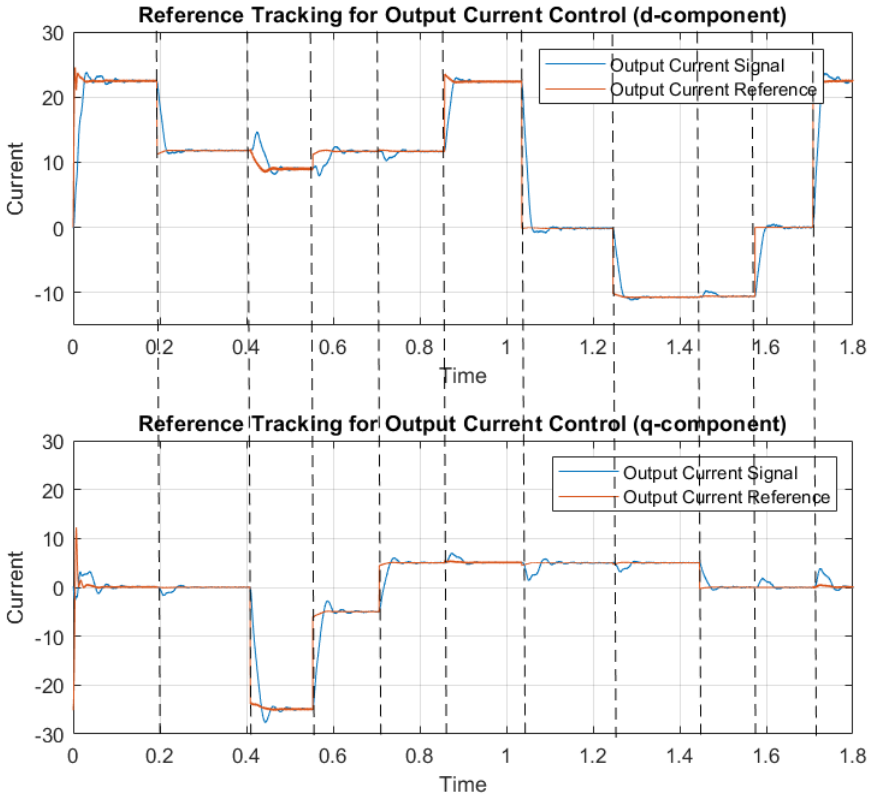

Figure 5.2: Output current controller performance for reference tracking. Upper graph shows d-component, lower graph shows q-component and dashed lines indicate the interaction between d and q components.

Circulating Current Control

Circulating currents in MMCs appear between upper and lower arms of phase legs and do not flow to the AC network. These currents appear due to voltage difference among the phase legs and may contain negative sequence components with frequencies twice of fundamental frequency. Circulating currents cause increased power losses in the converter and additional ripples in the SM capacitor voltages, which ultimately affects converters' performance and lifetime [50].

The arm inductor is capable of suppressing circulating currents to a certain degree, however, to fully eliminate circulating currents, an active regulator is required. Considering that circulating currents are dominated by second-order harmonics, the suppression is mainly designed for this frequency component. PR controllers are widely used for control of specific frequency components. For practical implementation, quasi-PR (QPR) can be used due to its wider bandwidth as compared to PR controller [51].

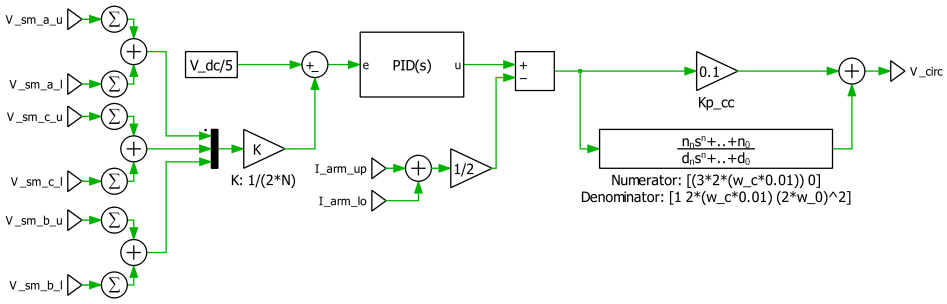

Figure 5.3: Circulating current suppression control diagram

$$G_{\text{cir}}(s) = K_{\text{cirp}} + \frac{2K_{\text{cirh}}\omega_c s}{s^2 + 2\omega_c s + (2\omega_0)^2} \tag{5.3}$$

where K_{cirp} and K_{cirh} are the proportional and integral coefficients of the QPR controller, ω_c and $2\omega_0$ denote the cut-off and resonant angular frequency. The introduced cut-off frequency can prevent a loss of sensitivity in the QPR controller when the frequency shifts, and the shift should be limited to a range of $\Delta f = 2\%$. The selection of controller gains can be seen in Table 5.2

Parameter	Gain
K_{cirp}	0.1
K_{cirh}	3
ω_c	628.3185*0.01
ω_0	314.1593

Table 5.2: PR controller gains with fundamental and cutoff frequencies

Furthermore, from linear transformations for MMCs, circulating currents can be obtain by using upper and lower arm currents $I_{arm,up}$ and $I_{arm,low}$ which provide the signal to be suppressed to the controller. The reference signal for circulating current controller is generated using average phase leg voltage balancing controller. Figure 5.3 shows circulating current controller with average phase leg voltage balancing. Outer loop controller takes the desired capacitor DC voltage as reference and compares it with the average capacitor voltage. This helps with balancing voltages between phase legs thus reducing the circulating currents due to voltage imbalances between phase legs. Average capacitor voltage for leg voltage balancing is defined as [52]:

$$\overline{u_{Ck}} = \frac{1}{2N}\left(\sum_{i=1}^{N} u_{Cki} + \sum_{j=N+1}^{2N} u_{Ckj}\right) \tag{5.4}$$

where i refers to upper arm submodules, j refers to lower arm submodules, k refers to phases abc and N refers to the total number of submodules per arm. The obtained average capacitor voltage is compared with desired capacitor voltage and error signal is fed into a simple PID controller. The output of the PI controller is compared with the circulating currents and the error is fed into QPR controller which generates voltage which is combined with the MMC current controller output to suppress circulating currents.

Parameter	Gain
K_p	5
K_i	-20

Table 5.3: PI controller gains for phase leg average capacitor balancing

Figure 5.4 shows the performance of circulating current controller. It can be clearly seen that circulating current controller is capable of suppressing second order negative frequency harmonic components originating due to circulating currents. However, DC offset still remains present in the measurement. Further investigation of additional control algorithms might be required to reduce DC component of the circulating currents.

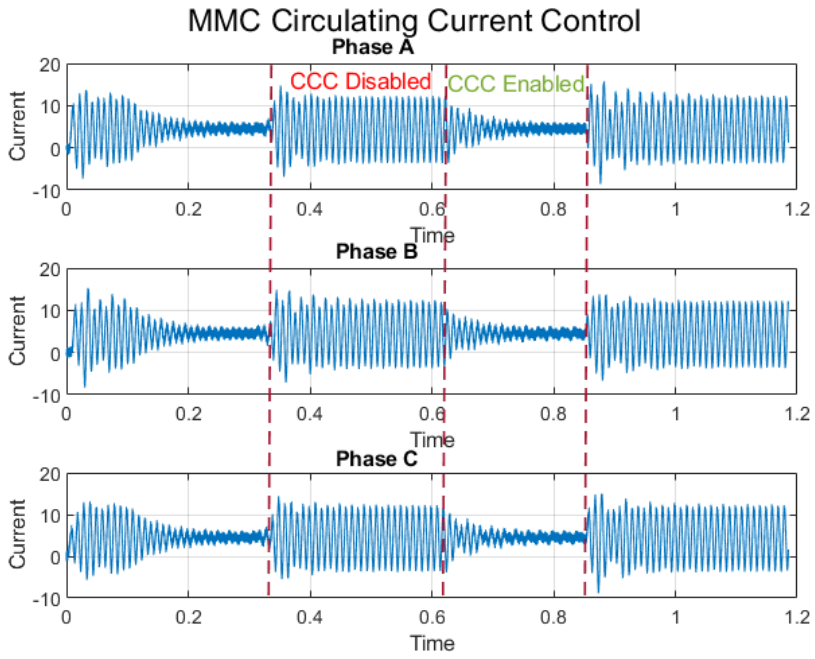

Figure 5.4: Circulating currents in each phase when circulating current controller is disabled and enabled.

Considering that circulating current and output current controllers has been implemented successfully, further investigation is on active/reactive power control.

Active/Reactive Power Control

PQ control in the d-q (rotating) reference frame is a method used to control the active/reactive power of a grid-connected converter. The control is based on the measurement of the voltage and current in the d-q reference frame. The active and reactive power are then calculated using the following equations [29]:

$$P = \frac{3}{2}(v_d i_d + v_q i_q) \tag{5.5}$$

$$Q = \frac{3}{2}(v_q i_d - v_d i_q) \tag{5.6}$$

where v_d and v_q are the d and q components of the voltage, and i_d and i_q are the d and q components of the current.

This means that by controlling the d-axis current, the active power can be controlled, and by controlling the q-axis current, the reactive power can be controlled. To implement PQ control in the d-q reference frame, a current controller is used to regulate the

converter current in the d-q reference frame. Then the active and reactive power command signals are translated into d and q components of the reference current, using the following matrix:

$$\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} = \frac{1}{v_d^2 + v_q^2} \begin{bmatrix} v_d & v_q \\ v_q & -v_d \end{bmatrix} \begin{bmatrix} \frac{2}{3}P^* \\ \frac{2}{3}Q^* \end{bmatrix} \tag{5.7}$$

where P^* and Q^* are the desired active and reactive power references. It is worth noting that the voltage and current components in the synchronous d-q frame or stationary $\alpha\beta$ frame should be properly filtered before they can be manipulated in the active and reactive power formulas.

Figure 5.5 shows block diagram for P/Q control. It takes voltages as inputs, P/Q as references and provides a current signal, which is used as reference for MMC output current controller. This method is straightforward and simple for direct P/Q control. Figure 5.6 shows reference tracking for P/Q controller. It can be seen that generated reference current accurately matches measured and reference powers. Additionally, it can be observed that there is a an interaction between active and reactive during the reference change. This is mainly due to the interactions in the output current controller, which acts as inner loop of the control.

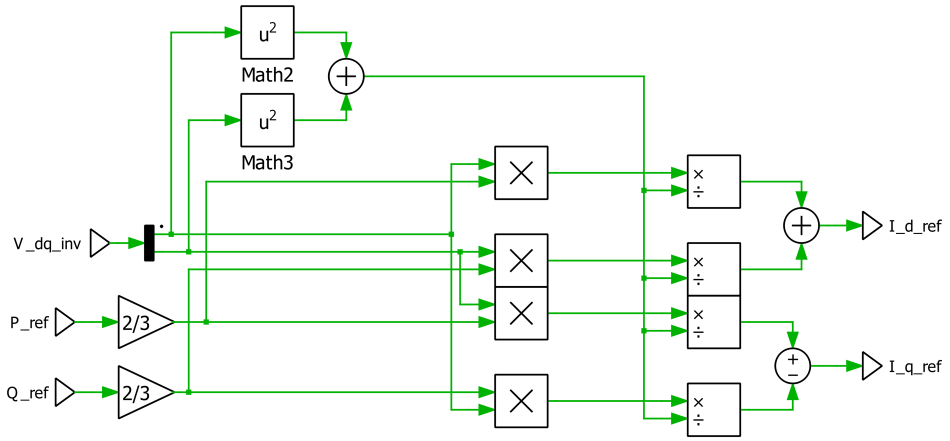

Figure 5.5: Block diagram of instantaneous P/Q controller

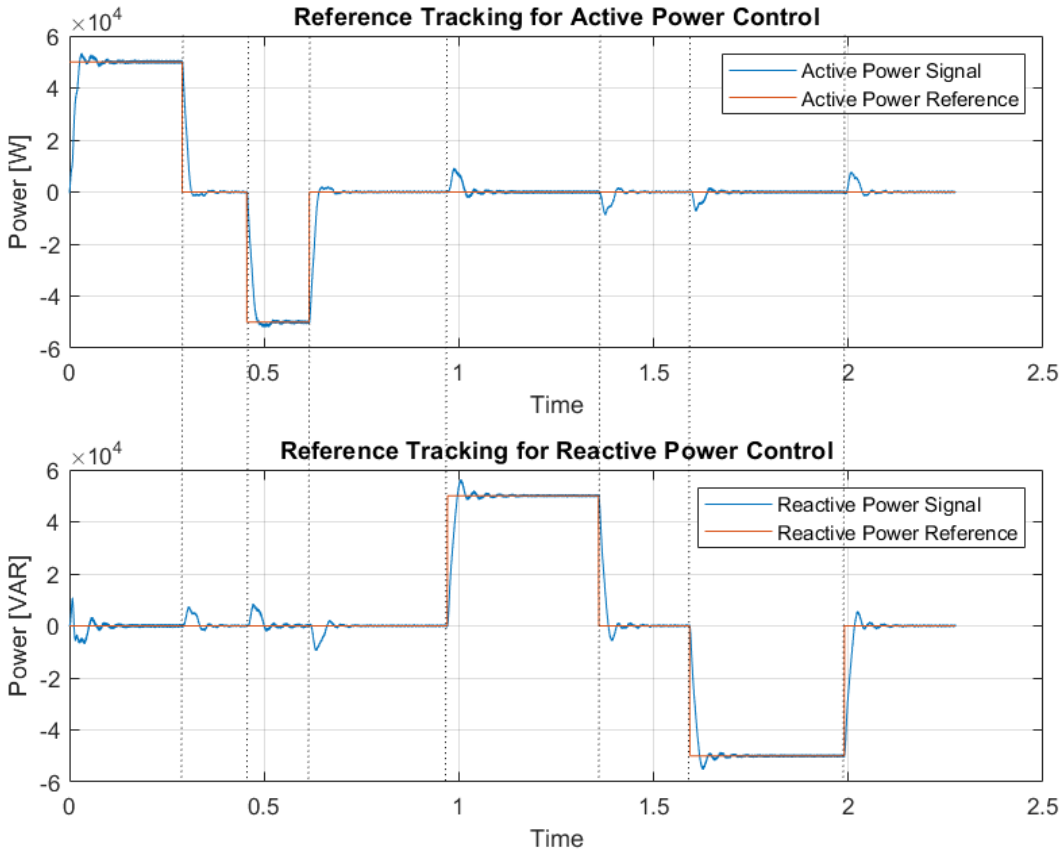

Figure 5.6: Active and reactive power reference following

Considering that sufficiently accurate power control has been achieved for the MMC, next step is to investigate battery integration into submodules. Before batteries can be combined with MMC, first battery converter control and charging/discharging protocols must be understood and designed. For this reason, next section focus on the analysis and development of the battery converter control.

5.0.3 Battery Charge/Discharge Control

High-level Overview

A high-level representation of the cascaded DC-DC control structure can be seen in Figure 5.7. It is comprised of two PID controllers, one responsible for generating $\tilde{I_L}$ reference, this being the outer voltage loop controller and the other responsible for the generation of the $\tilde{d}$ reference, this being the inner current loop controller. The controllers have been tuned using the MATLAB function *pidtune* using the buck converter transfer functions,

shown in Chapter 4, Section 4.2.1. Based on testing, adjustments have been made to the P gain of the inner current control and P gain of the outer voltage control.

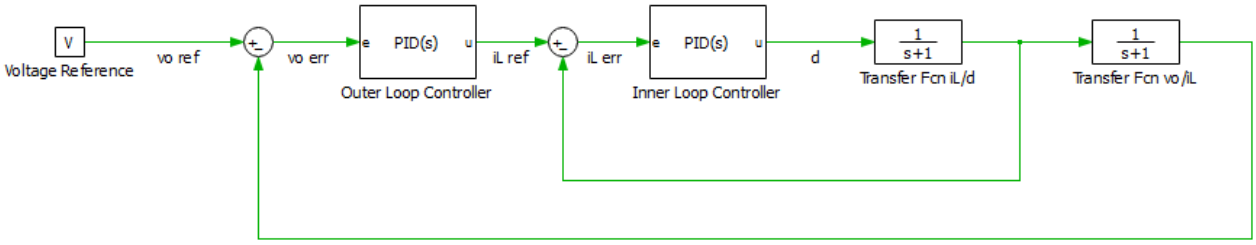

Figure 5.7: DC-DC converter cascaded control scheme

The tuned PID parameters for both inner and outer controllers can be seen in Table 5.4.

Parameter	Gain
$K_{p_{\text{inner}}}$	0.072
$K_{i_{\text{inner}}}$	92.73
$K_{d_{\text{inner}}}$	$1.38 \cdot 10^{-7}$
$K_{p_{\text{outer}}}$	0.0043
$K_{i_{\text{outer}}}$	7.88
$K_{d_{\text{outer}}}$	$9.2 \cdot 10^{-7}$

Table 5.4: Inner and outer PID controller gains

Battery Enable/Disable Logic

The logic to determine whether the battery should be connected to the MMC-side half-bridge for charging or discharging can be seen in Figure 5.8. The upper part of the logic is responsible for the detection of whether the battery is charging. It checks if the battery's SoC is within the range of 9.9% and 100%. If it is true, a logical 1 is outputted from the respective logic gate. Next check in the logic is responsible for detecting whether the reference current set is less than 0 (negative sign current in the battery represents the charging of the battery). If both the SoC and the reference current statements are true, the battery is enabled and the reference is set to charging, which is used for the controller logic, seen in Figure 5.10. A similar logic flow is used for the battery discharging detection. It is checked whether the SoC is above 10% and whether the reference current is larger than 0. If both of those statements are true, the battery is enabled and the reference is set to discharging. In cases where the reference current is set to 0 and the battery is either fully charged or discharged to the threshold, the battery is then disconnected from the MMC-side half-bridge.

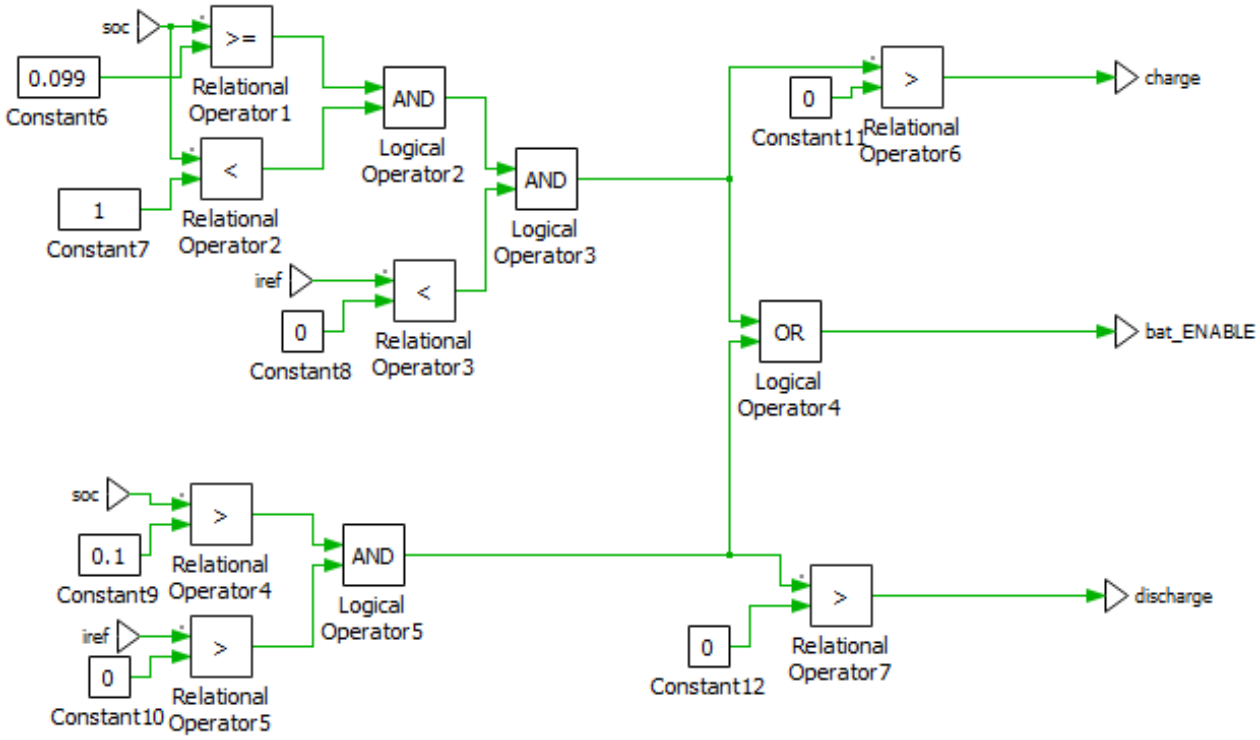

Figure 5.8: Battery Enable/Disable Logic

Figure 5.9 showcases the test performed to determine the working of the logic structure.

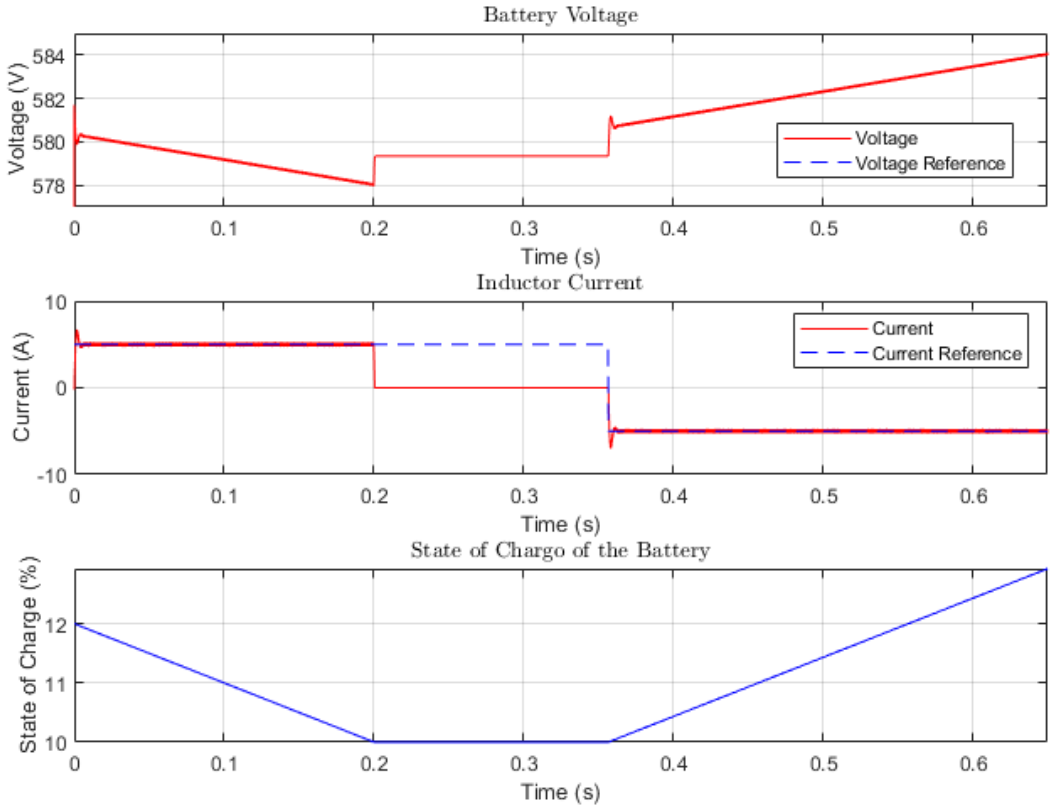

Figure 5.9: Voltage, Current and SoC plots for battery enable/disable logic

The conducted test starts at 12% with a discharging current of 5A. As mentioned in the before, once the battery discharges to 10%, the DC-DC converter is disconnected from the battery. It can be seen that at t≈0.2s the battery SoC reaches 10% and the flow of power to the battery is disrupted, indicating that the logic works as intended. Furthermore, once the reference current is set to -5A for charging, the logic enables the modulation for the DC-DC converter, and the battery starts charging.

CC/CV Control

The control of the bidirectional DC-DC converter is comprised of an inner current controller and an outer voltage controller. The CC-CV method for battery charging has been utilized as the control scheme, and is commonly used for battery charging/discharging purposes [53, 54]. CC-CV refers to the charging and discharging of the battery in two modes, Constant Current and Constant Voltage. In CC mode, a fixed constant current is provided to charge the battery. As the battery charges, the V_{OCV} of the battery slowly rises. Once the V_{OCV} reaches a set voltage level, the charging switches to CV mode,

where the battery is charged with the set voltage level maintained and the current is reduced until the battery reaches full charge [54]. Figure 5.10 shows the control logic of the CC-CV for the bidirectional DC-DC converter in the simulation.

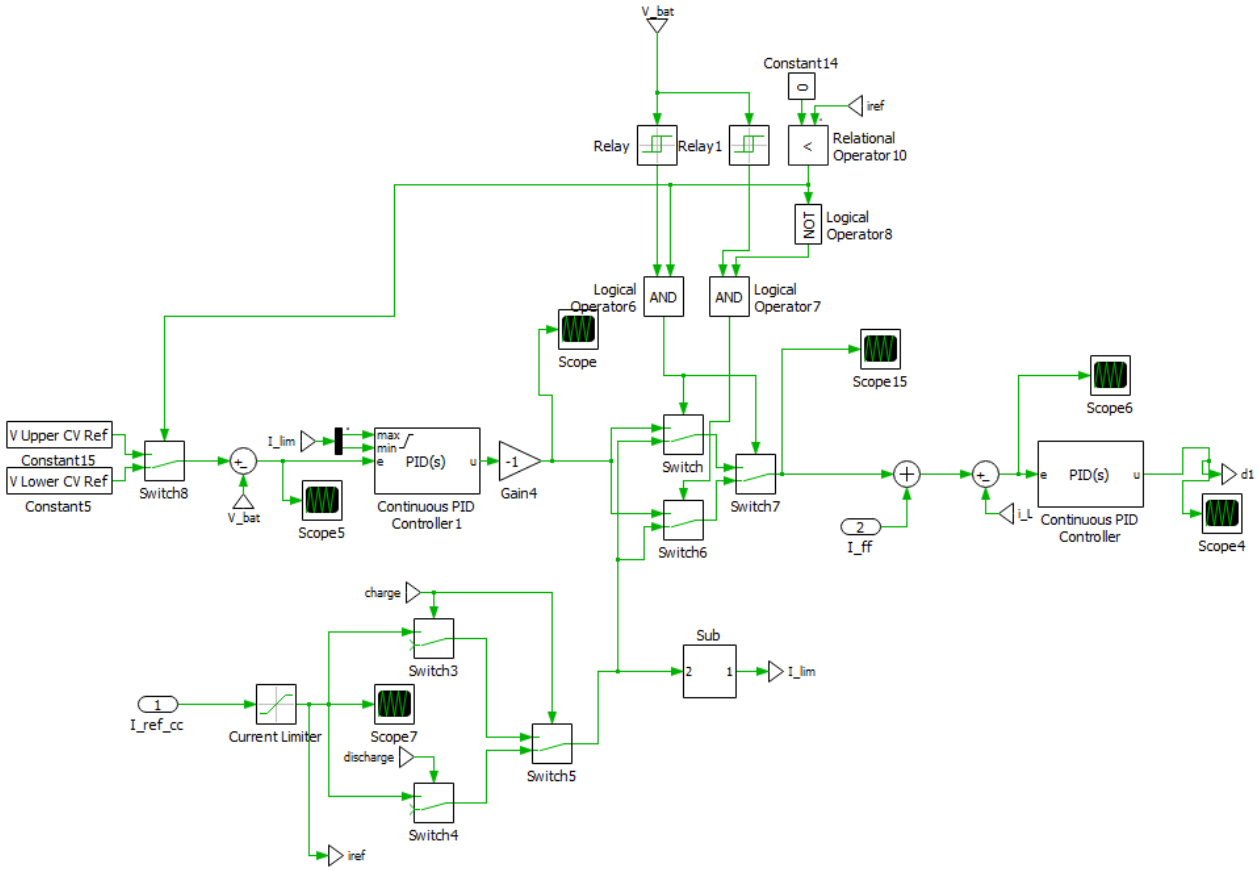

Figure 5.10: CC-CV Control

The control logic allows for the controllers to work both in battery charge and discharge modes (Buck and Boost), without requiring two separate control schemes [53]. For this control scheme, positive current is considered discharging current and negative current is considered charging current. Depending on the measured voltage of the battery, the controller either starts in CC or CV modes. To determine which mode is used for the battery charging and discharging, the controller has a relay. The relay checks whether the battery voltage is within the set threshold of *V Upper CV Ref* or *V Lower CV Ref*. Furthermore, it checks the current reference, to determine which voltage reference should be used. If the battery voltage is not within these thresholds, the controller operates in CC mode. Otherwise, the controller operates in CV mode. The inner current controller takes in the current error, which is calculated from the difference between the reference current and the measured current. The output of the controller is duty cycle,

which is then applied to the DC-DC converters switches. As the duty cycle can only be from 0 to 1, saturation is applied to the current controller. When the controller operates in CV mode, the reference current is generated by the outer voltage controller. The outer voltage controller should be tuned such that it is slower compared to the inner current controller. Figure 5.11, showcases the charging of the battery in CC/CV modes and discharging in CC mode.

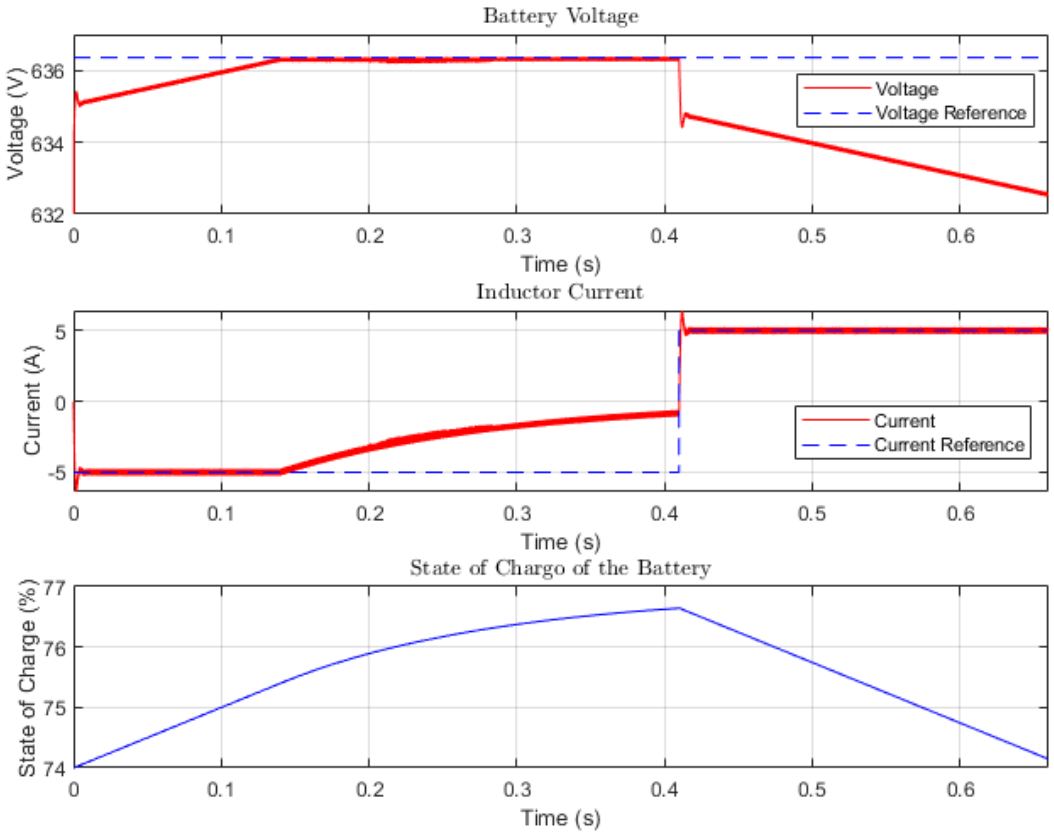

Figure 5.11: Voltage, Current and SoC plots of the CC/CV control

The conducted test starts at 74% SoC, with CC mode enabled, with current reference set to -5A. Current follows the current reference, while the battery voltage slowly rises. At t≈0.15s, the battery voltage reaches the set *V Upper CV Ref* of 636.31V and CV mode is activated, which causes the current to ramp up and the battery voltage to follow the set reference. At t≈0.4s, the current reference is set to 5A, which causes a sharp drop in battery voltage from 636.31V to 634V and a sharp increase in the current. The controller then operates in CC mode, while discharging the battery. Based on this test it can be concluded that the CC/CV control works. Considering this, few improvements to be

made to the control would include a more thorough tuning procedure, to increase the ramp of the current while the controller is operating in CV mode.

Healthy and Second-life battery charging/discharging comparison

A comparison test has been conducted to compare the performance of CC/CV control based on battery parameters at 100% SoH and 70% SoH, which can be seen in Figure 5.12.

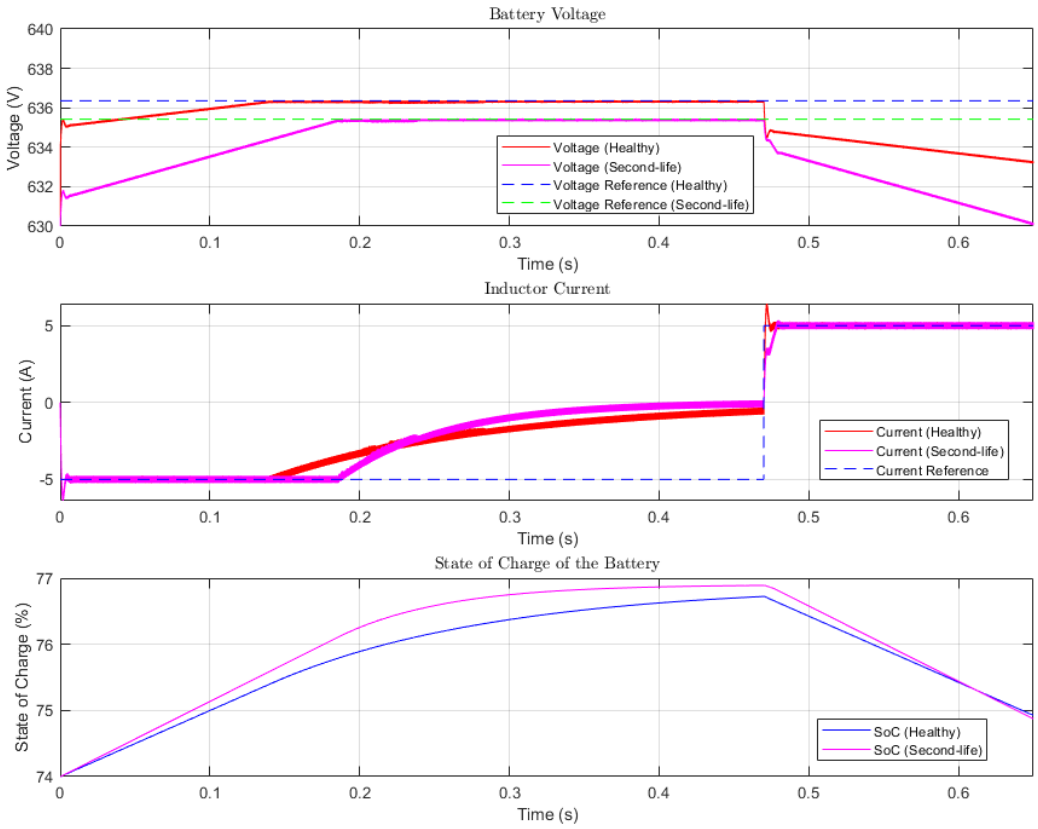

Figure 5.12: Battery Voltage, Current and SoC comparison at 100% and 70% SoC

The healthy battery responds as expected, compared to the results from the previous section. There are no visible disturbances when changing the CC/CV mode and during discharge. The current responds fast according to the reference with minimal overshoot. When looking at the second-life battery test, it is visible that the results differ compared to the healthy battery. Firstly, the battery voltage slope for charging is larger. This increase can be explained by the degradation of internal resistance. During discharge, the current

response to set references shows some disturbances, which could also be explained by the degradation of the internal resistance. Furthermore, there are visible disturbances in the battery voltage, potentially indicating degradation of the electrode materials, which are modeled by the RC network parameters. Lastly, differences in SOC can be seen. It indicates the degradation of the capacity, causing the battery to charge up and discharge faster.

5.0.4 Battery integration into MMC SMs

As discussed before, each SM of MMC has bi-directional DC/DC converter integrated to enable battery power control. Battery power distribution can be described similar to the capacitor voltage, where battery power is defined for individual submodules $P_{b_{kji}}$, battery power per arm $P_{b_{kj}}$, battery power per leg P_{b_k} and finally total battery power for MMC P_b [30].

$$P_{b_{kj}} = \sum_{i=1}^{N} P_{b_{kji}} \tag{5.8}$$

$$P_{b_k} = \sum_{j}^{p,n} \sum_{i=1}^{N} P_{b_{kji}} \tag{5.9}$$

$$P_b = \sum_{k}^{a,b,c} \sum_{j}^{p,n} \sum_{i=1}^{N} P_{b_{kji}} \tag{5.10}$$

Using this definition, battery power influence on the AC and DC sides of MMC can be defined using following expression [30]:

$$P_{ac} = P_{dc} - \sum_{k}^{a,b,c} \sum_{j}^{p,n} \sum_{i=1}^{N} P_{b_{kji}} \tag{5.11}$$

where P_{ac} and P_{dc} are total active powers of the AC and DC side, respectively, while $P_{b_{kji}}$ is the battery power of individual SM. To compensate or absorb power fluctuations of the AC or DC side of the MMC-BESS, the individual battery would discharge when $P_{b_{kji}} < 0$ and vice versa. According to this consideration, there are six different operation modes [30]:

Rectifier operation ($P_{AC} < 0$):

1. Mode I: $P_{AC} = P_{DC} \Rightarrow P_{Bat} = 0$ (idle);
2. Mode II: $|P_{AC}| > |P_{DC}| \Rightarrow P_{Bat} > 0$ (charging);
3. Mode III: $|P_{AC}| < |P_{DC}| \Rightarrow P_{Bat} < 0$ (discharging);

Inverter operation ($P_{AC} > 0$):

1. Mode IV: $|P_{AC}| < |P_{DC}| \Rightarrow P_{Bat} > 0$ (charging);
2. Mode V: $|P_{AC}| > |P_{DC}| \Rightarrow P_{Bat} < 0$ (discharging);
3. Mode VI: $P_{AC} = P_{DC} \Rightarrow P_{Bat} = 0$ (idle).

Battery current reference calculation based on desired total power delivery

In previous section on battery converter control design, it has been decided to use outer loop for battery voltage control and inner loop for current control due to CC-CV protocol. Current reference can be obtained from desired power reference simply by using following expression:

$$I^*_{b_{kji}} = \frac{\frac{P_b}{6N}}{V_{b_{kji}}} \tag{5.12}$$

where $I^*_{b_{kji}}$ is reference current for each individual battery, P_b is desired power delivered from/to the battery and $V_{b_{kji}}$ is voltage of each individual battery. Such calculation is shown in Figure 5.13

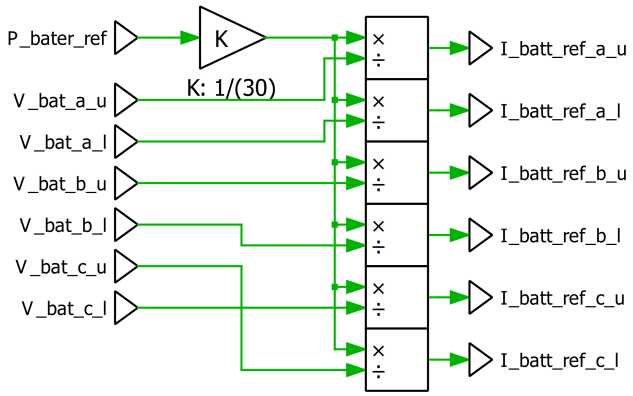

Figure 5.13: Reference current calculation for each battery controller

Battery SOC equalization among phases, arms and submodules

An important function of battery connected MMC system is SOC equalization. The structure of SOC equalization is divided into three sections: balancing among phases, between upper and lower arms, and among SMs within one arm [30]. The definition of SOC for individual battery in terms of power is:

$$\mathrm{SOC}_{kji}(t) = \mathrm{SOC}_{kji}(t_0) + \frac{1}{E_{b,kji}} \int_{t_0}^{t} P_{b_{kji}}\, dt \tag{5.13}$$

where $P_{b_{kji}}$ is individual battery power and $E_{b_{kji}}$ is nominal energy of individual battery given by battery voltage and its capacity. The required power regulation is achieved through closed-loop controls of average SOC for each balancing section. The same as for power, SOC for different sections is calculating by summing SOC among different sections which gives following expressions [30]:

$$SOC_{b_{kj}} = \sum_{i=1}^{N} SOC_{b_{kji}} \tag{5.14}$$

$$SOC_{b_k} = \sum_{j}^{p,n} \sum_{i=1}^{N} SOC_{b_{kji}} \tag{5.15}$$

$$SOC_b = \sum_{k}^{a,b,c} \sum_{j}^{p,n} \sum_{i=1}^{N} SOC_{b_{kji}} \tag{5.16}$$

where battery SOC per submodule is $SOC_{b_{kji}}$, battery SOC per arm $SOC_{b_{kj}}$, battery power per leg SOC_{b_k} and finally total battery SOC for MMC SOC_b. Furthermore, average SOC values are used as a reference for different controllers and can be described as:

$$\overline{SOC_{b_{kj}}} = \frac{1}{N} \sum_{i=1}^{N} SOC_{b_{kji}} \tag{5.17}$$

$$\overline{SOC_{b_k}} = \frac{1}{2} \sum_{j}^{p,n} \sum_{i=1}^{N} SOC_{b_{kji}} \tag{5.18}$$

$$\overline{SOC_b} = \frac{1}{3} \sum_{k}^{a,b,c} \sum_{j}^{p,n} \sum_{i=1}^{N} SOC_{b_{kji}} \tag{5.19}$$

where average battery SOC per arm is $\overline{SOC_{b_{kj}}}$, battery average SOC per leg is $\overline{SOC_{b_k}}$ and finally total average battery SOC for MMC is $\overline{SOC_b}$ [30].

Having averaged SOC values for different SOC balancing sections, following control laws can be defined [30]:

$$\Delta P_{b_k} = K_{ph}(\overline{SOC_b} - SOC_{b_k}) \tag{5.20}$$

$$\Delta P_{b_{kj}} = K_{arm}(\overline{SOC_{b_k}} - SOC_{b_{kj}}) \tag{5.21}$$

$$\Delta P_{b_{kji}} = K_{SM}(\overline{SOC_{b_{kj}}} - SOC_{b_{kji}}) \tag{5.22}$$

where delta SOC per phase is ΔP_{b_k}, battery delta SOC per arm is $\Delta P_{b_{kj}}$ and finally delta SOC for for each submodule within arm is $\Delta P_{b_{kji}}$. Figures 5.14, 5.15 and 5.16 shows block diagrams for SOC balancing between phases, arms and submodules, respectively.

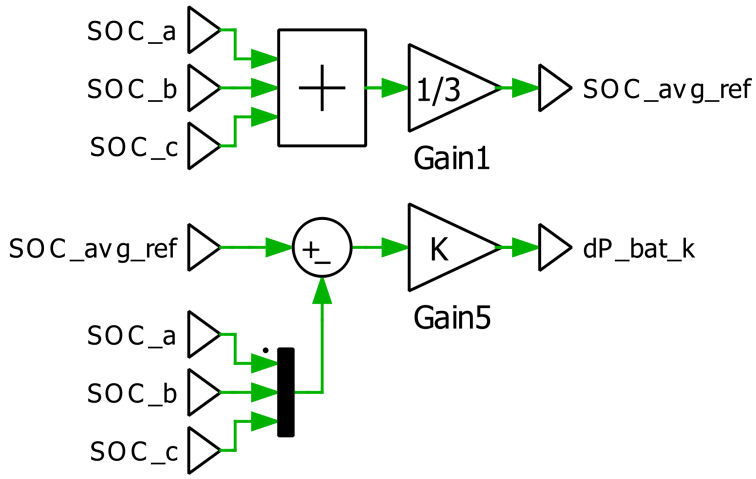

Figure 5.14: SOC averaging and delta power for phase SOC balancing within total SOC

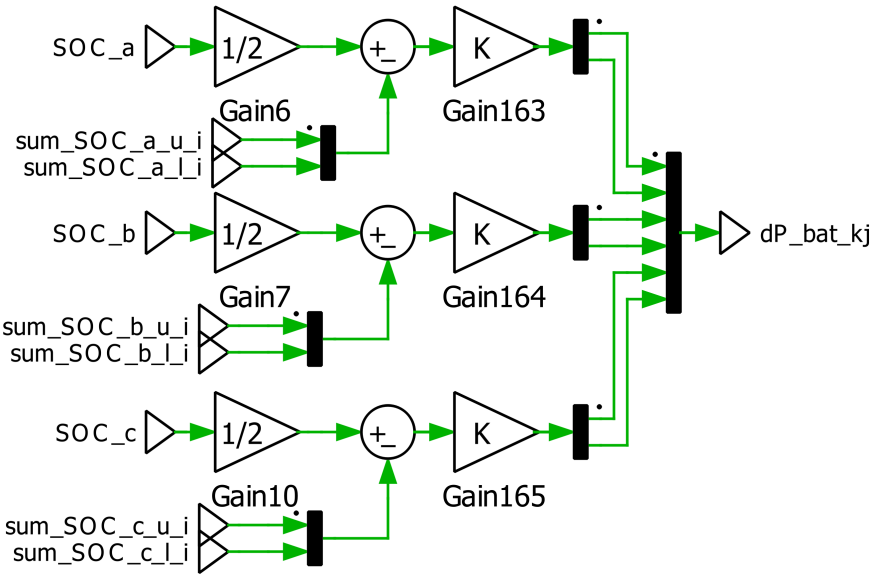

Figure 5.15: Delta power control for arm SOC balancing within phase SOC

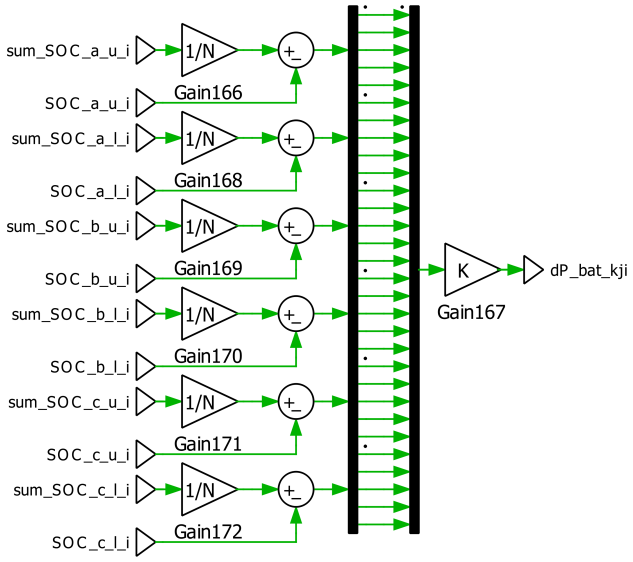

Figure 5.16: Delta power control for submodule SOC balancing within arm SOC

Considering that battery converter operates in CCCV mode where voltage reference is battery voltage and not SM capacitor voltage, SOC balancing is achieved through current feedforward for each individual submodule. Feedforward component for each battery current controller is defined as:

$$I_{ff\_kji} = \frac{1}{v_{b\_kji}} \left(-\frac{\Delta P_{b\_k}}{2N} - \frac{\Delta P_{b\_kj}}{N} - \Delta P_{b\_kji} \right) \tag{5.23}$$

Block diagram of feedforward component calculation is shown in Figure 5.17.

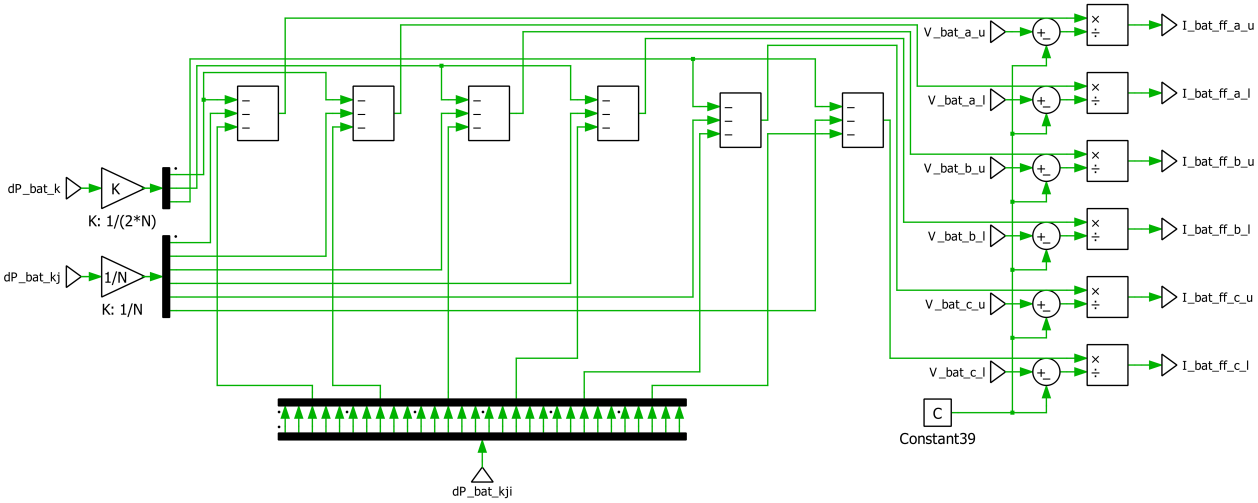

Figure 5.17: Block diagram of current feedforward component calculation for battery SOC balancing

Each obtained current feedforward component is added to each individual battery inner current controller to adjust the reference current which results in adjusted SOC. The placement of feedforward is shown in Figure 5.18. It is shown that feedforward component is added to the reference signal of current controller for each individual battery.

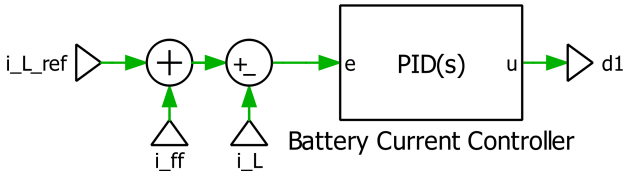

Figure 5.18: Current feedforward component placement in battery current controller for battery SOC balancing

Battery integrated MMC power delivery in discharging mode

Figure 5.19 shows power distribution in AC side, DC side and battery during the discharging period. Following the notation for power direction described in the beginning of the chapter, it can be seen that AC power is positive, thus MMC is operating in inverter mode feeding the power into AC grid. Furthermore, as the batteries are discharging, it reduces required power from DC grid thus supporting it. It follows that in discharging mode $P_{AC} > P_{DC}$.

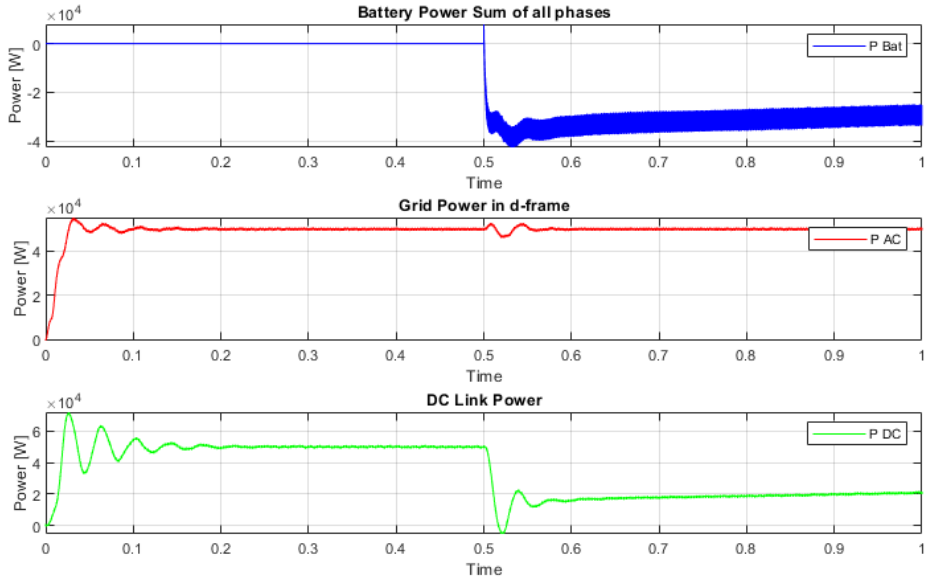

Figure 5.19: Active power change during discharging of the battery

Furthermore, Figure 5.20 shows submodule capacitor voltage. It can be seen that capacitor voltage ripple increases because power is delivered to the submodules. This is expected as increased current in capacitor leads to larger voltage.

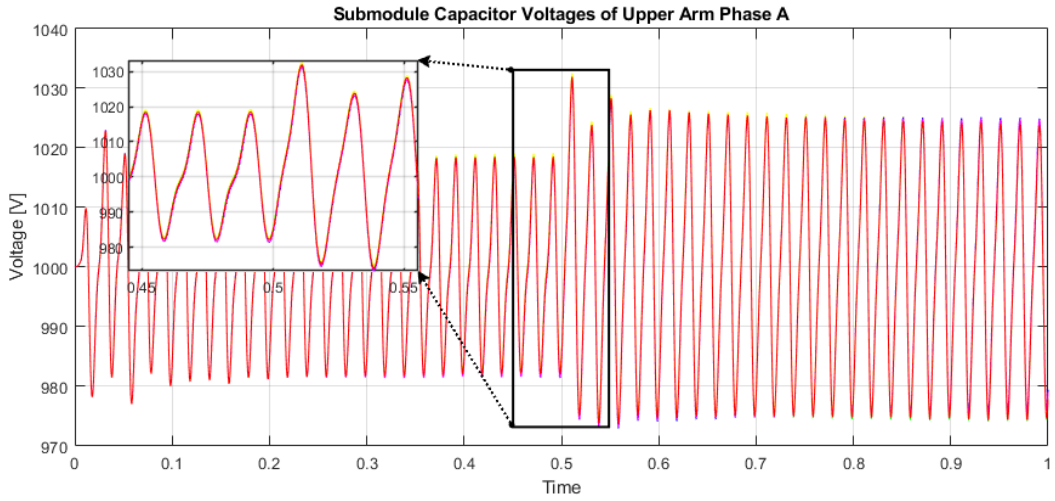

Figure 5.20: Submodule Capacitor Voltage for Upper Arm Phase A (discharging)

Additionally, Figure 5.21 shows battery currents for each submodule in upper arm of phase A. It can be seen that there is an oscillation present together with the DC component. This oscillation appears due to the capacitor voltage oscillating on the high-side of

the DC/DC converter. Further investigation must be done to suppress these oscillations. Nonetheless, it can be observed that all currents within arm are of similar size with some slight variations due to parameter aging.

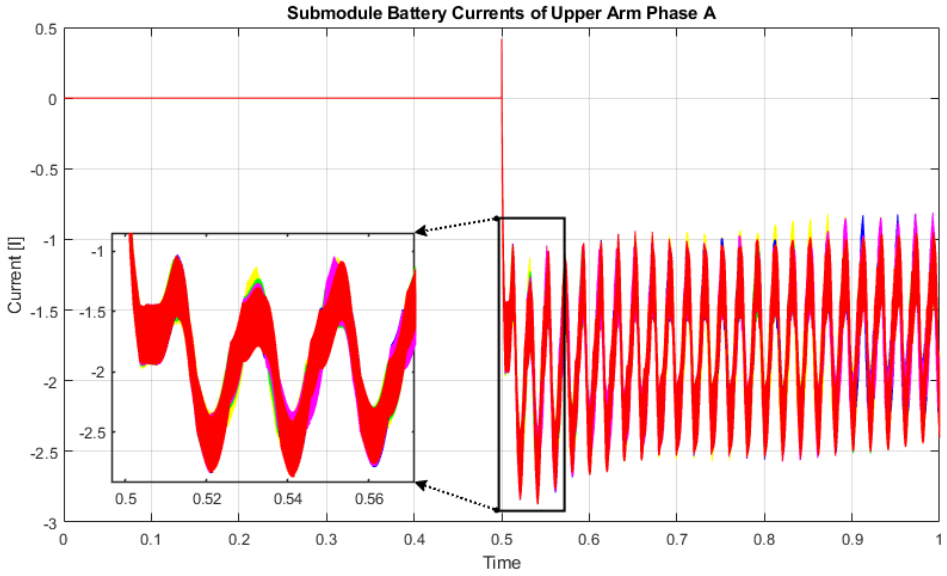

Figure 5.21: Battery Currents Upper Arm Phase a (discharging)

Lastly, Figures 5.22, 5.23 and 5.24 show power delta required for balanced SOC among phases, arms and submodules, respectively. It can be seen from the magnitude of the delta powers that all SOCs are indeed balanced. However, longer simulation might be needed to observe the effects of the balancing over longer period of time.

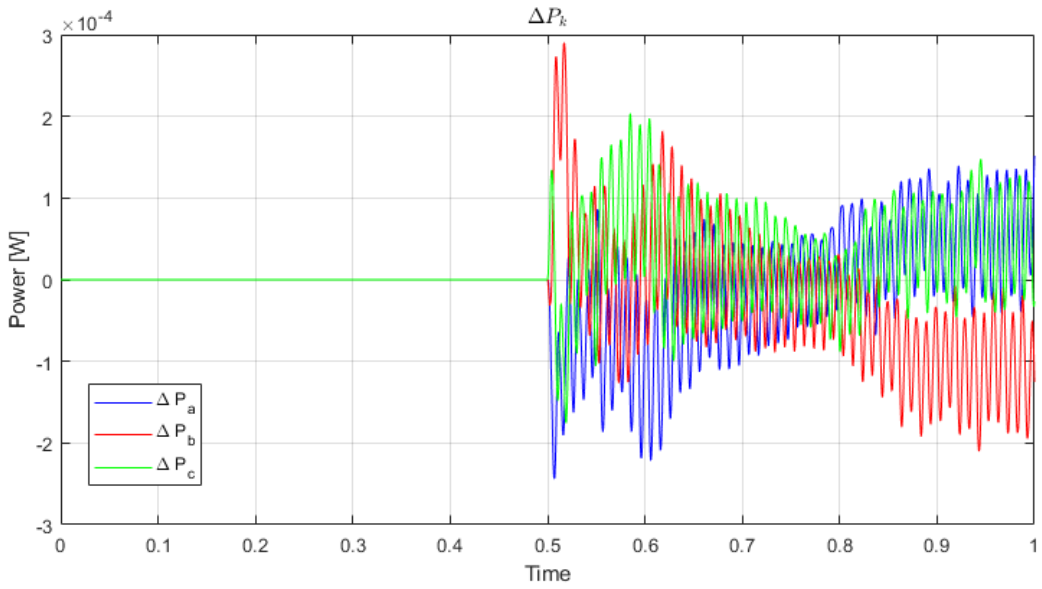

Figure 5.22: ΔP_k (discharging)

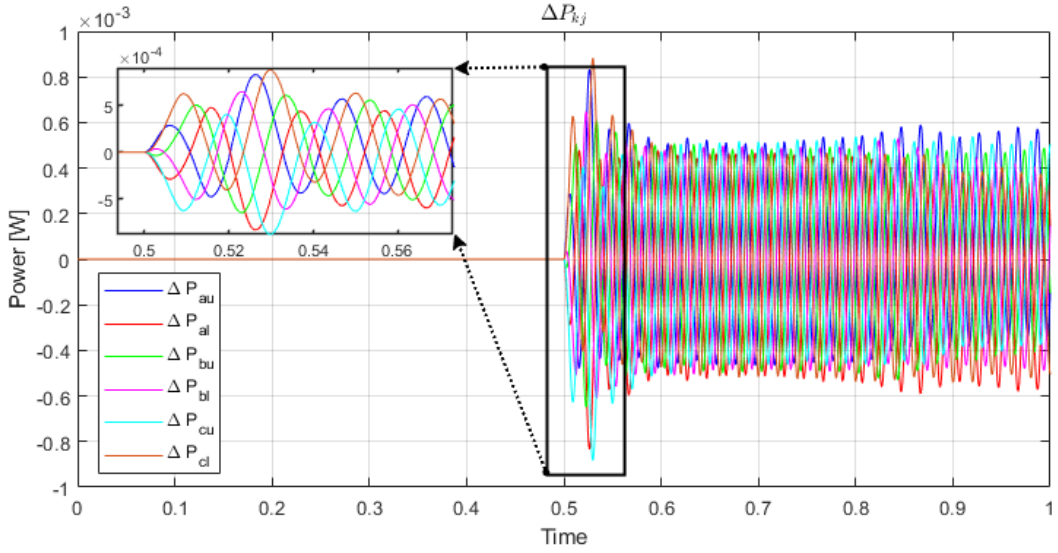

Figure 5.23: ΔP_{kj} (discharging)

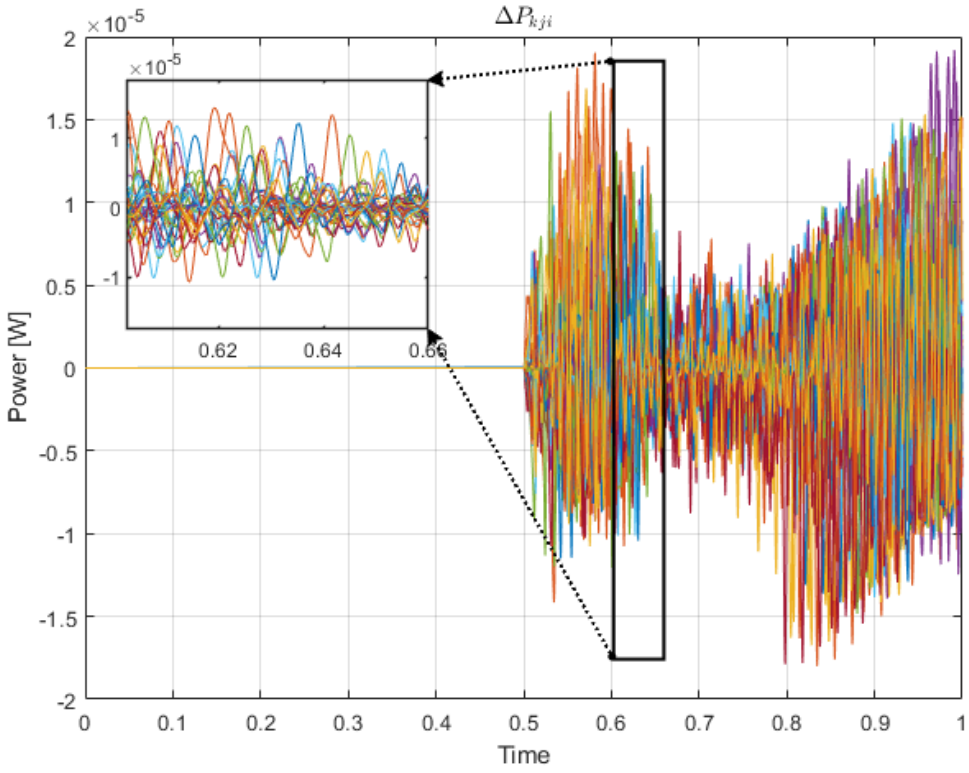

Figure 5.24: ΔP_{kji} (discharging)

Battery integrated MMC power delivery in charging mode

Figure 5.25 shows power distribution in AC side, DC side and battery during the charging period. Following the notation for power direction, it can be seen that AC power is positive, thus MMC is operating in inverter mode feeding the power into AC grid. Furthermore, as the batteries are charging, it increases required power from DC grid thus allowing surplus energy to be utilised for later use. It follows that in charging mode $P_{AC} < P_{DC}$.

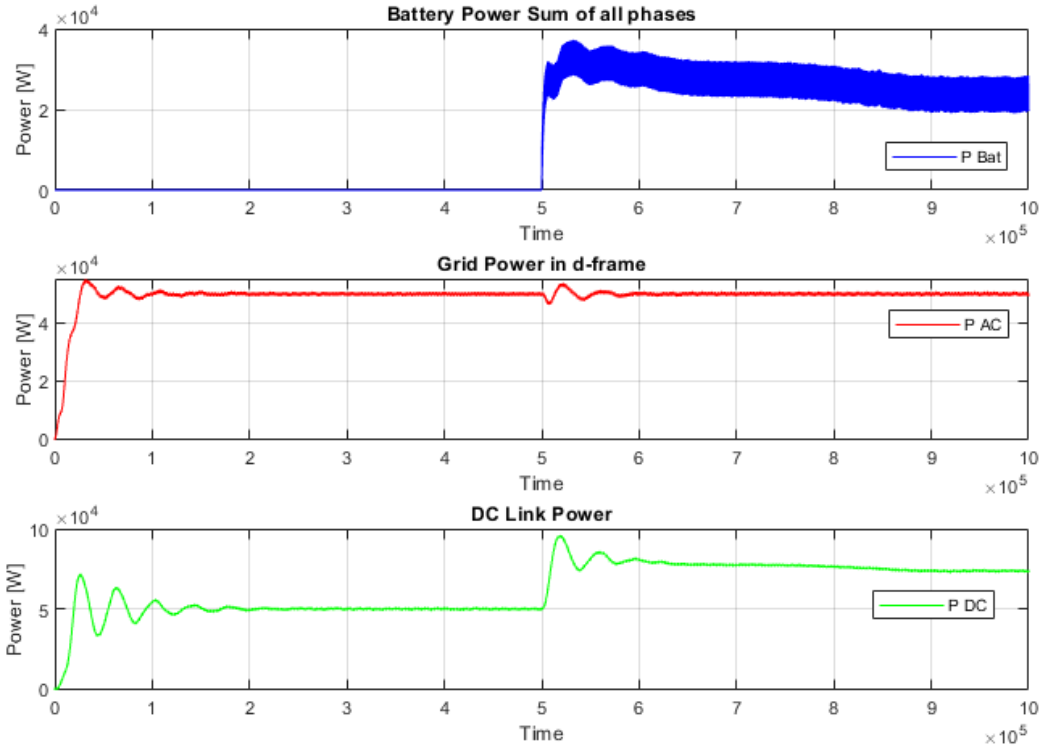

Figure 5.25: Active power change during charging of the battery

Furthermore, Figure 5.26 shows submodule capacitor voltage. It can be seen that capacitor voltage ripple reduces because power is delivered from the capacitors to the batteries . This is expected as reduced current in capacitor leads to lower voltage.

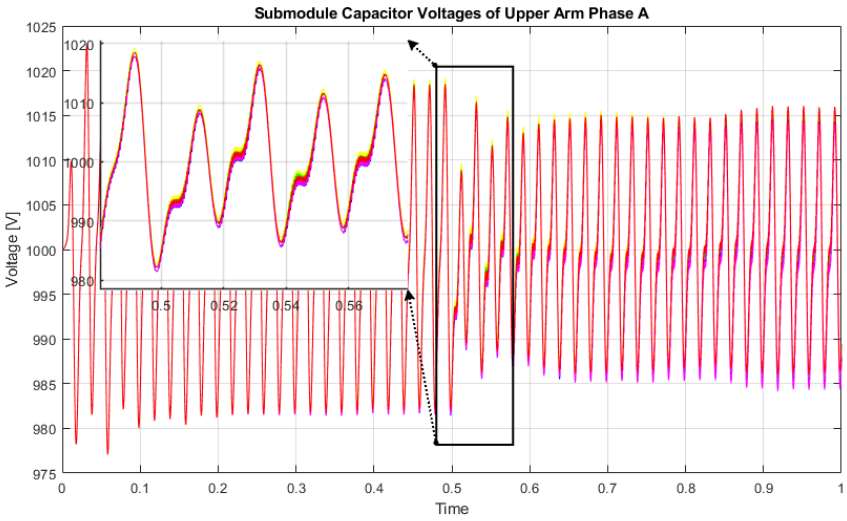

Figure 5.26: Submodule Capacitor Voltages Upper Arm Phase a (charging)

Additionally, Figure 5.27 shows battery currents for each submodule in upper arm of phase A. It can be seen that there is an oscillation present together with the DC component. This oscillation appears due to the capacitor voltage oscillating on the high-side of the DC/DC converter. Also, compared to the current in discharging mode, oscillations appear to be lower. This is mainly due to reduced capacitor voltage oscillations. Further investigation must be done to suppress these oscillations. Nonetheless, it can be observed that all currents within arm are of similar size with some slight variations due to parameter aging.

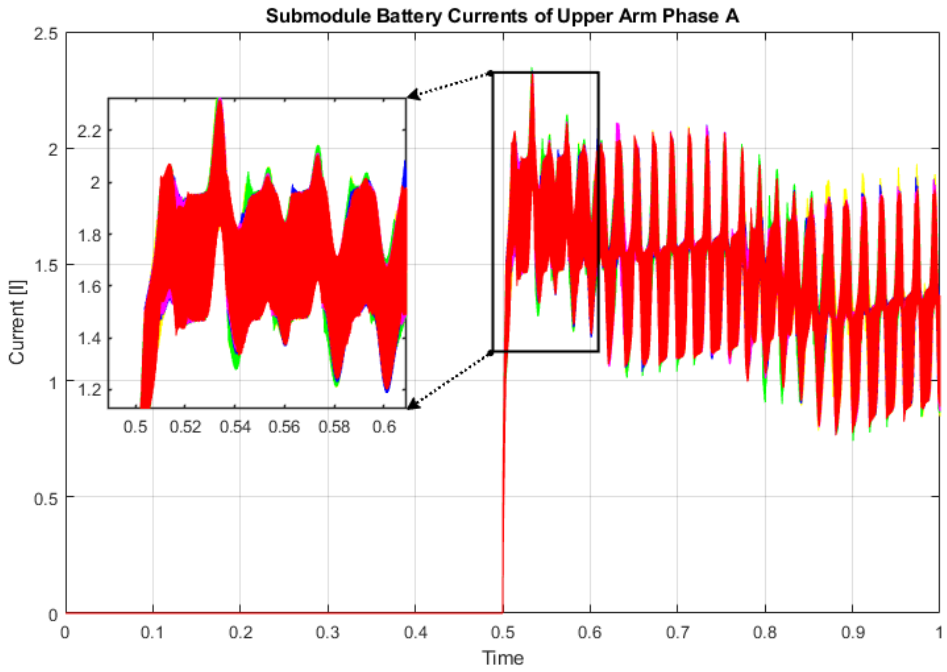

Figure 5.27: Battery Currents Upper Arm Phase a (charging)

Lastly, Figures 5.28, 5.29 and 5.30 show power delta required for balanced SOC among phases, arms and submodules, respectively. It can be seen from the magnitude of the delta powers that all SOCs are indeed balanced. However, longer simulation might be needed to observe the effects of the balancing over longer period of time.

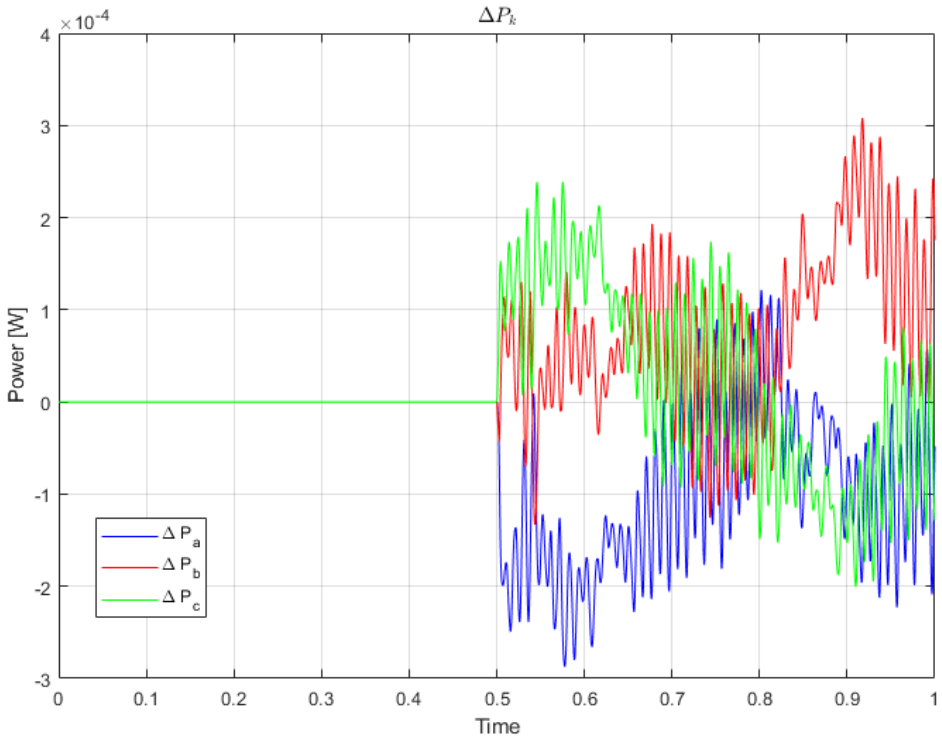

Figure 5.28: ΔP_k (charging)

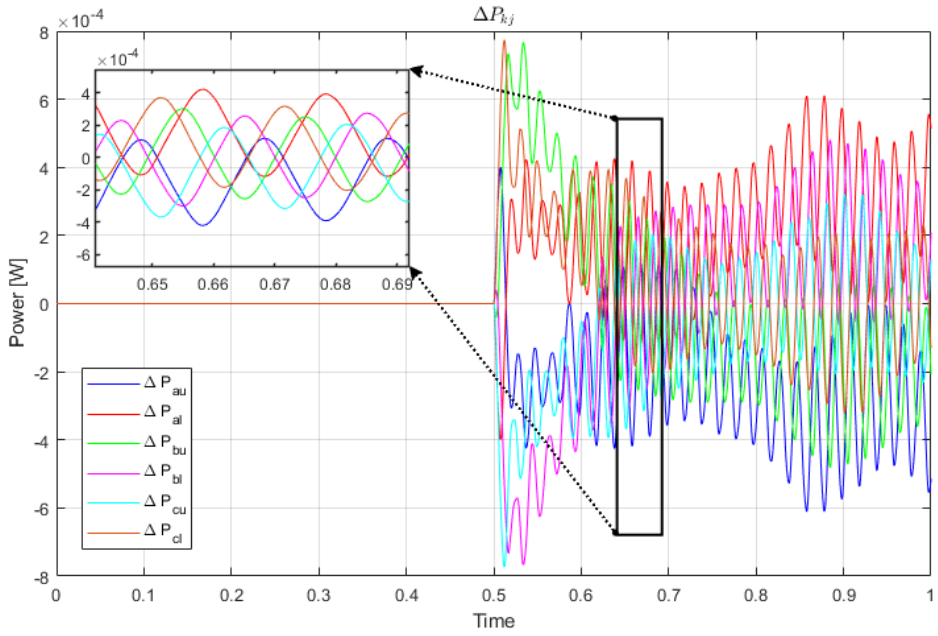

Figure 5.29: ΔP_{kj} (charging)

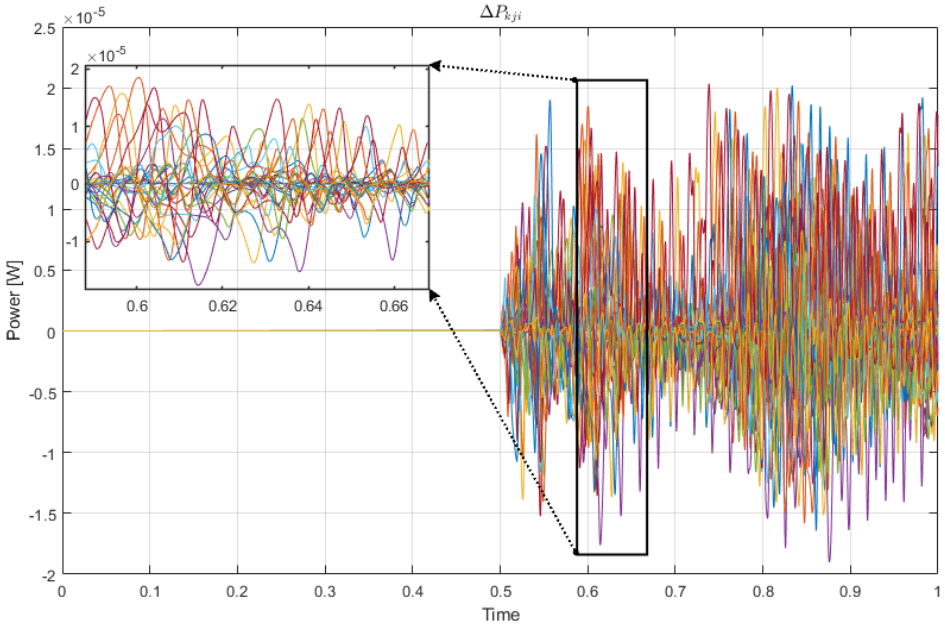

Figure 5.30: ΔP_{kji} (charging)

Chapter 6

Discussion

First Objective: Literature Review and Gap Analysis

- **Conduct a comprehensive review of existing MMC technologies with battery-connected systems, battery modeling, different control layers, and control methods for each layer.**
  - We successfully conducted a thorough review of MMC technologies, battery modeling, and various control layers. Additionally, we discussed the application of MMCs for grid support.
  - However, we did not fully implement grid support functionalities, particularly active power regulation and compensation in terms of supply and demand, as we focused more on the supply aspect.

Second Objective: Real-Life Application Analysis

- **Define project requirements in terms of applications, power requirements, grid requirements, and select a specific point of the grid (e.g., in Denmark) with non-grid voltages, supply, and demand.**
  - We have not defined the power requirements or specific connection requirements for a point on the Danish grid. This task remains for future work to optimize and apply the MMC system more specifically.

Third Objective: System Design and Modeling

- **Conduct a literature review on the modeling and integration of MMC and battery systems.**
  - This task has been completed.

- **Determine the sizing of the components.**
  - While we have addressed this to some extent, further investigation is needed to select more optimal components, which could be a separate project.
- **Design a detailed model of an MMC integrated with first-life battery storage.**
  - We have completed this to some extent, but the model remains theoretical as it was based on simulations. Further investigation with real batteries or battery modules and real data is necessary.
- **Conduct a review on the control of MMC and battery storage-connected systems.**
  - This task has been completed.
- **Design and simulate control layers associated with MMC and batteries.**
  - This task has been completed.
- **Develop control strategies for battery charge and discharge management within the MMC.**
  - This has been done to a certain extent but could be expanded further.
- **Conduct a literature review on control for specific grid support functionalities.**
  - This task has been completed.
- **Determine grid support control algorithms and active/reactive power requirements.**
  - This task has not been fully completed. Only a simple active power control has been implemented.
- **Analyze the capability of MMC integrated with battery storage for providing grid support, focusing on selected functionalities.**
  - This has been done only for active power sharing.
- **Develop control algorithms for grid support functionalities such as voltage regulation, frequency stabilization, and peak shaving.**
  - This task has not been completed and could be a focus for further research.

Delimitations and Future Work

- **Detailed modeling and analysis of second-life battery integration into MMCs, focusing on aging and deterioration impacts.**
  - This has been partially addressed.
- **Expand the simulation model to include diverse grid support functionalities and broader application scenarios.**
  - This task has not been completed.
- **Policy and regulatory analysis for integration of grid support systems, addressing standards and compliance issues.**
  - This task has not been completed.
- **Perform a cost comparison between first-life and potential second-life battery integration.**
  - This task has not been completed.
- **Evaluate the economic viability and potential savings associated with battery integration.**
  - This task has not been completed, though it was recognized as beyond the current scope.

6.1 Future Work

This section will discuss further improvements and additions that can be made in addition to the research done in this thesis.

6.1.1 Optimization of the models and simulation

All the models used for the simulation during this thesis were based on electrical circuits, which proved to be cumbersome when performing the testing. To efficiently perform all the tests, cloud based computing could be beneficial allowing for more computing power to be used. Furthermore, utilizing properly derived transfer functions of the system would allow for a less computationally heavy testing.

6.1.2 Battery parameter identification using experimental battery pack data

For the thesis, the battery experimental data has been simulated, which does not fully reflect the real-life battery testing. For a more appropriate battery parameter identification, real-life battery pack charge/discharge tests could be conducted.

6.1.3 More in-depth controller tuning

The control tuning in this thesis has been done manually by trial and error and observation of the responses of the associated control signals however to further improve the performance of the overall system a more methodological tuning approach for different controllers must be conducted.

6.1.4 Real-life experiments

A crucial step in the design of the battery connected MMC system is the physical implementation and testing of the performance and control of the system thus one of the important future works would be to build an actual MMC system with integrated batteries which then could be used to evaluate actual performance as well as obtain real-life data, which could then be used to understand the impacts of modeled static and dynamic aspects of the overall system.

6.1.5 Battery current ripple reduction

As was seen from the figures of the battery currents when charging and discharging into the MMC it has been observed that based on the proposed topologies and control structures there was a fluctuation in the battery current. In order to preserve the battery lifetime it is important to ensure that batteries are charged and discharged at DC currents with as little ripples and oscillations as possible so further analysis of battery current fluctuation reduction would definitely improve the overall performance and longevity of the system.

6.1.6 FLBs and SLBs comparison for a larger period time in operation

Due to hardware limitations and the model computational complexity the simulation was limited to only one second which limited the observations of the impacts of SLBs in such a system, therefore further research and investigations should be done to simulate the system for a longer period of time preferably for multiple cycles of battery charge/discharge to observe how second-life batteries and the degradation profiles actually affect the stability and performance of the battery integrated MMC.

Chapter 7

Conclusion

This thesis concludes with a detailed exploration of integrating battery systems into power grids to enhance support functionalities. Initially, the problem analysis focused on the need for ESS integration. Furthermore, the use of second-life batteries and various techniques for grid support, along with different converter topologies and an overview of ESS. Upon further investigation, MMC with battery pack integrated into each submodule utilizing bidirectional DC-DC converters as an interface between battery packs and MMC has been chosen. This approach was selected due to the modularity of MMCs, the potential for redundant submodules, and the ease of replacing submodules with significantly degraded batteries. This modularity simplifies maintenance and supports the integration of second-life batteries for grid applications. After defining the problem, a list of goals was established. The thesis discusses the achieved goals and outlines future work for the ones that have not been achieved. Key contributions of this thesis include the modeling and control of the MMC with bidirectional buck-boost converters integrated into each submodule. A dq current controller for MMC output current and a circulating current controller for phase voltage balancing were developed. For the bidirectional DC-DC converter, both current and voltage control were developed, alongside a CCCV protocol to ensure proper battery operation. Regarding the battery parameters, a simulation to extract data has been conducted by utilizing charge/discharge pulse test. Furthermore, a degradation profile has been used as an addition to the simulation of the battery test to include the aging of battery parameters over cycles. The simulated data has been used to identify the parameters for the Thevenin model of the battery, which was used within the submodules for the MMC simulation. Lastly, the simulation results indicate that batteries integrated into each submodule can indeed support active power supply to the grid in both charging and discharging modes. However, further investigation is necessary due to the complexity of the system and simulation. Despite these challenges, we strongly believe that future electrification requires modular, redundant, safe, and efficient solutions.

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Appendix A

List of Abbreviations

Appendix B

List of Abbreviations

AC Alternating Current

ACC Automatic Cruise Control

ANPC Active Neutral-Point Clamped

AS Australian Standard

BESS Battery Energy Storage System

BMS Battery Management System

CC Constant Current

CCCV Constant Current Constant Voltage

CD Capacity Degradation

CEI Comitato Elettrotecnico Italiano (Italian Electrotechnical Committee)

CHB Cascaded H-Bridge

DC Direct Current

DOD Depth of Discharge

DR Demand Response

DSM Demand Side Management

EDF Électricité de France

EEC Equivalent Electrical Circuit

ESS Energy Storage System

EU European Union

EV Electric Vehicle

GC Grid Code

GHG Greenhouse Gas

HV High Voltage

HVDC High Voltage Direct Current

IEC International Electrotechnical Commission

IEEE Institute of Electrical and Electronics Engineers

IGBT Insulated-Gate Bipolar Transistor

KCL Kirchhoff's Current Law

KVL Kirchhoff's Voltage Law

LC Inductor-Capacitor

LCL Inductor-Capacitor-Inductor

LV Low Voltage

LVDC Low Voltage Direct Current

MMC Modular Multilevel Converter

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

MV Medium Voltage

NPC Neutral-Point Clamped

OCV Open Circuit Voltage

PCC Point of Common Coupling

PF Power Factor

PS Phase Shift

PSA Peugeot Société Anonyme (Peugeot S.A.)

PV Photovoltaic

PWM Pulse Width Modulation

RES Renewable Energy Source

RMS Root Mean Square

SAE Society of Automotive Engineers

SLB Second-Life Battery

SMES Superconducting Magnetic Energy Storage

SOC State of Charge

SOH State of Health

SST Solid State Transformer

THD Total Harmonic Distortion

TSO Transmission System Operator

UL Underwriters Laboratories

UN United Nations

USABC United States Advanced Battery Consortium

VSC Voltage Source Converter

ZSI Z-Source Inverter

Appendix C

Battery Charging

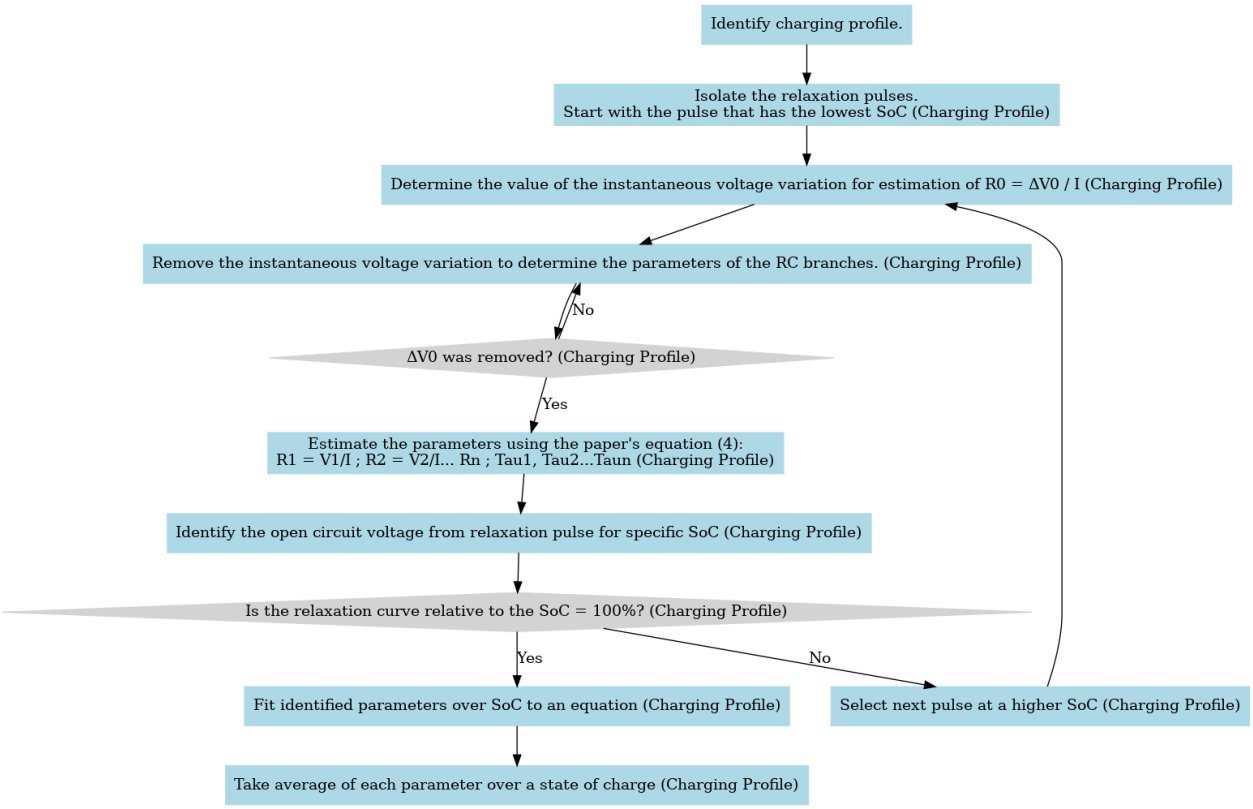

Figure C.1: Charging Profile Parameter Estimation Flowchart

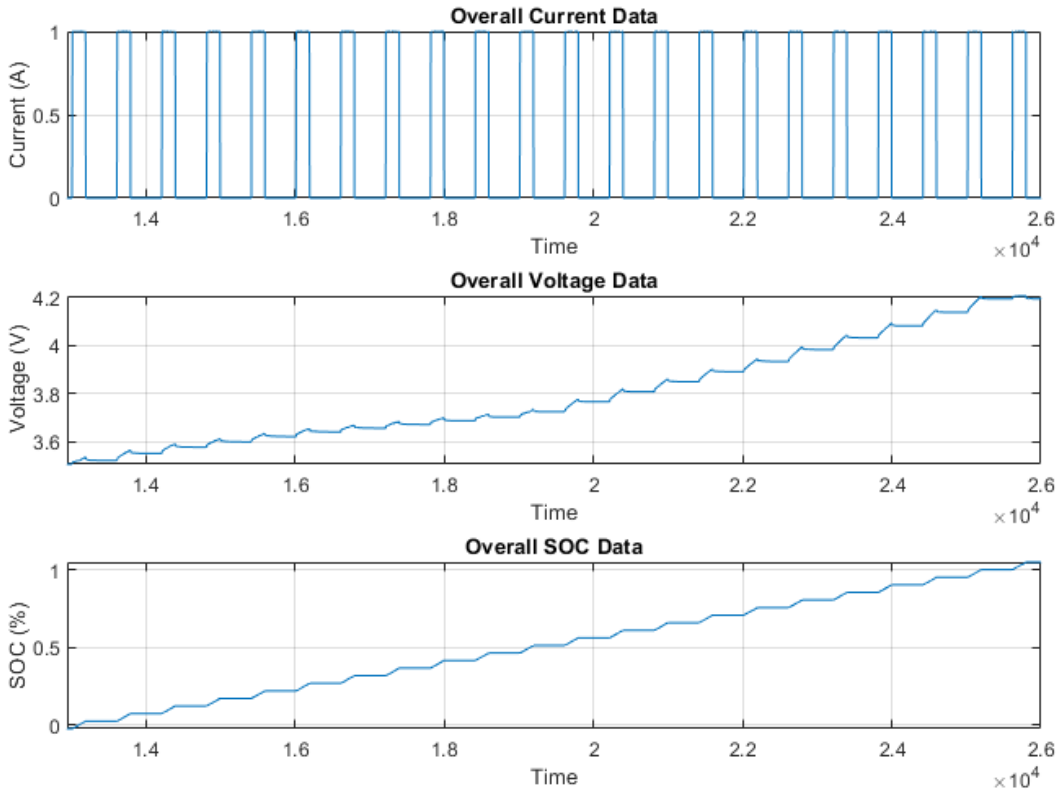

Figure C.2: Charge Profile of the collected data

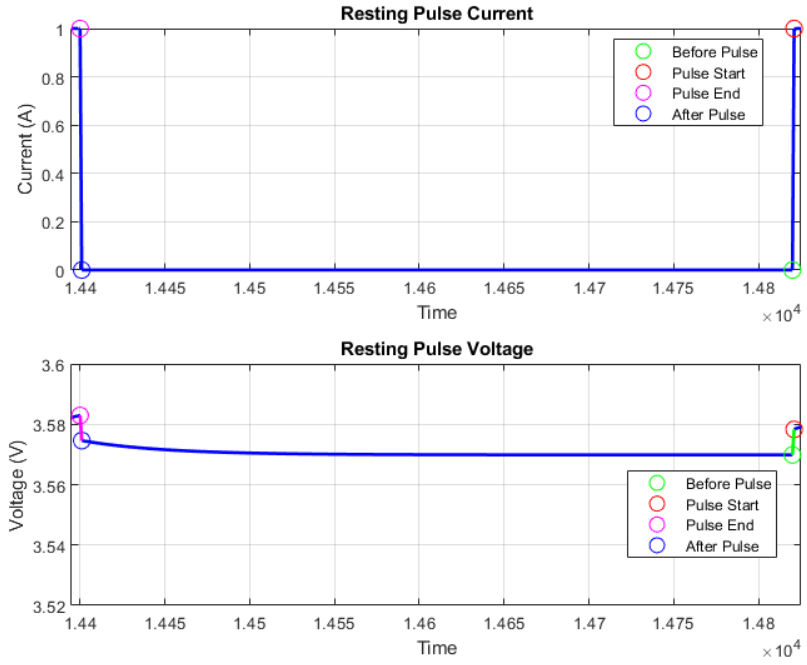

Figure C.3: Individual Resting Pulse V_{OCV} and I (Instantaneous Response Highlighted)

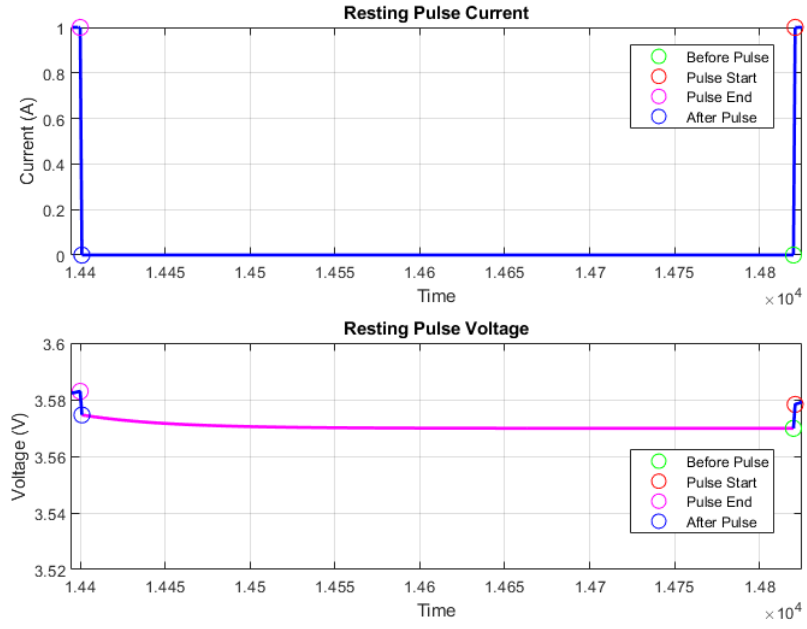

Figure C.4: Individual Resting Pulse V_{OCV} and I (Transient Response Highlighted)

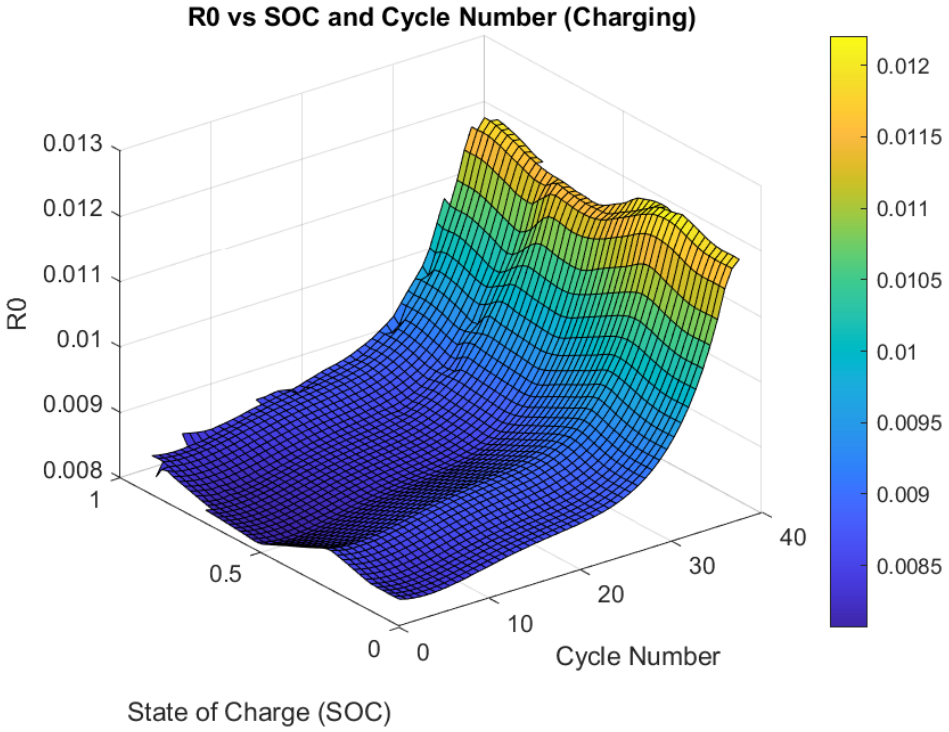

Figure C.5: R_0 parameter over SoC and Cycle Number (Charging)

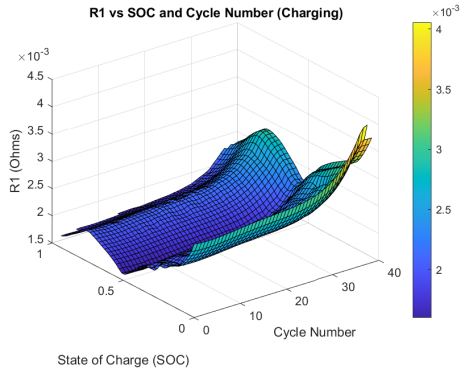

Figure C.6: R_1 parameter over SoC and Cycle Number (Charging)

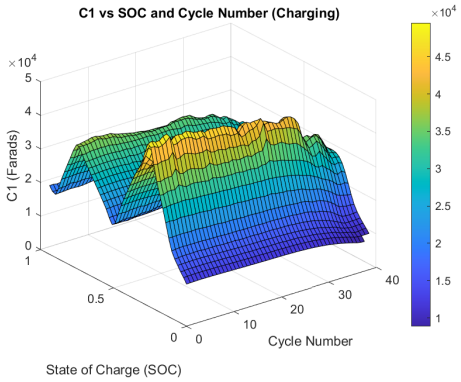

Figure C.7: C_1 parameter over SoC and Cycle Number (Charging)

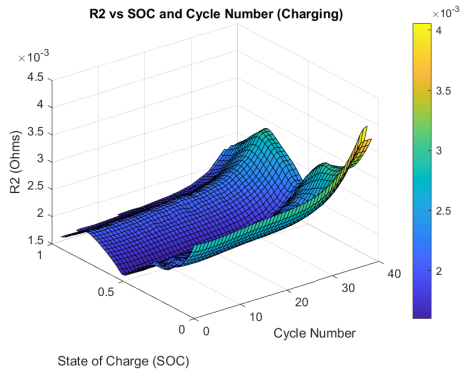

Figure C.8: R_2 parameter over SoC and Cycle Number (Charging)

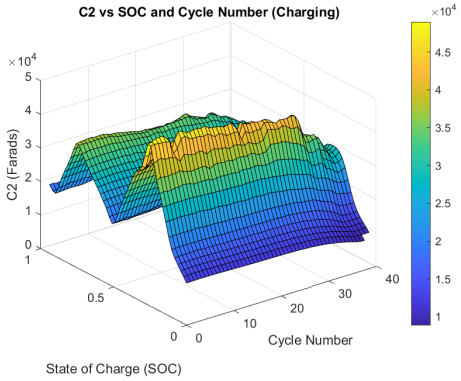

Figure C.9: C_2 parameter over SoC and Cycle Number (Charging)