# Using a Variable Capacitor as a Voltage Actuator

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STUDENT REPORT

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**Abstract:**

Gate drivers are a ubiquitous component in power electronics, and is therefore subject to much research. An fairly unexplored topic is using a variable capacitor as a gate driver. This project analyses and designs a variable capacitor for use as a gate driver. The idea is successfully tested using a basic plate capacitor, which is used to turn on a GaNFET by rapidly removing the dielectric material. This experiment, along with simulation studies give insight into a possible design. Using these insights, a variable capacitor is designed. The capacitor consists of two PCBs, with one being spun around an axis by a motor. This spinning causes the capacitance to change. The capacitance is measured using a voltage divider, and it is found to deviate slightly from expectations. The variable capacitor is inserted into an electrical circuit and it is found that a variable voltage can be achieved over a load similar to the gate of a FET. The predicted voltages do not correspond with many of the measured voltages. When the load is exchanged for a GaNFET, the variable capacitor can successfully regulate turn on and turn off. Instability is seen in the gate and drain voltages of the GaNFET. It is concluded that the variable capacitor can be used to regulate a voltage, but it is not suitable for use as a gate driver. To finish, some ideas are given for future work with this idea.

# Synopsis

Gate drivers are a staple of power electronics. These gate drivers are mostly standard components which seek to maintain a voltage at the gate of a FET. An idea was had to use a drastically different structure for driving the gate by using a changing capacitance. A component was found which could change its capacitance, but was found unsuitable through testing. Therefore, it was decided that the idea should be tested properly. Mathematical analysis was done on the definition of capacitance, if both the charges, voltage and capacitance was allowed to change, both in the steady state and dynamically. It was found that if the charges remain constant, the ratio of the initial capacitance to the final capacitance corresponded to the ratio of the voltages before and after the capacitance change. This concept is called the Capacitance Change Ratio, or CCR. The analysis did confirm the idea that a changing capacitance should lead to a changing voltage, and a proof of concept experiment was set up to test this. A very simple plate capacitor was made from two aluminium plates, some wood and a piece of plexiglass. The analysis suggested that if the capacitor was charged to a voltage with the plexiglass in between the aluminium plates, the voltage could be increased temporarily by ripping the plexiglass out from in between the plates. The experiment was conducted, successfully turning on a GaNFET. The experimental data showed that the gate voltage was erratic and not suitable for periodic activation. It was therefore decided that a variable capacitor should be designed for periodic switching of the GaNFET. To ascertain the important parameters in such a system, a simulation study was made in Simulink. This study found that the leakage currents played a major role in the behaviour of the circuit, and that an approximately $10\,\mathrm{M\Omega}$ leakage resistor was found to still have an impact on the functioning of the system. It was shown that the rate of change of capacitance did not have an impact on the behaviour of the voltage, other than how fast the steady state was reached.

In designing the variable capacitor, a parameter must be chosen as the variable. To do this, a simple model for a plate capacitor was analysed, and it was found that there were three different parameters which could be changed: the relative permittivity, the distance between the plates and the area. Varying the relative permittivity and the distance was discarded, and a variation of the effective area was chosen in stead. The effective area is defined as the overlap between two plates in the x-y plane. It was then chosen that the electrically connected contacts should remain stationary, which lead to the a design consisting of three plates. Two plates are stationary and a third plate is moving above them, creating a capacitive bridge between the two plates. If the plate is then not overlapping both plate beneath it, the capacitance will be much smaller than if it is overlapping. It was chosen that the voltage should plateau at a high and low voltage, and the capacitance is designed to do so as well. The plates were created using PCBs and the method for moving them was chosen to be rotational. A support structure was designed to hold the PCBs and the motor chosen for rotating one of the PCBs. The support structure was designed with a calibration mechanism to allow for precise adjustment of the distance between

the plates. Initial testing of the device showed that the plates were not completely flush, and that the structure warped due to temperature changes. It was therefore chosen that the device should be calibrated once, and all tests should be done quickly afterwards.

The device was then tested electrically. A method was constructed for measuring the capacitance by spinning the rotor slowly and using a capacitive voltage divider to calculate the unknown capacitance of the device. The capacitance generally follows the designed structure, but did contain some both high, and low frequency deviations. These deviations were concluded to be a consequence of the mechanical system, and were deemed of acceptable. It was further found that the current caused by a rapid change in capacitance could have an effect on the capacitance measurement, but at the low speeds the measurement was done at this current was negligible.

A circuit was set up and the variable capacitor was tested in situ, as a way of changing the voltage. The circuit consists of a power supply, the variable capacitor, a DC-blocking capacitor, a zener diode and a load capacitor. It was found that with the zener diode implemented, the voltage initially did not fit expectations, but considering the non-linear behaviour of the diode the voltage could be predicted using the CCR. With the zener diode removed, the voltage was consistently much higher than expected. The load was then exchanged with a GaNFET, and the circuit was tested. It was found that the variable capacitor could turn on the GaNFET, but also that it introduced an instability of the gate and drain voltages in some situations. The origin of this instability is unknown.

With the device tested, some attempts at iterating on the design was made, along with testing some specific weird phenomena found in the system. The device was concluded functional, but not suitable for driving a FET. Suggestions are given for possible future work on such a device, including a more rigid dynamic analysis along with analysis of how inductances affect the system, more robust measurement methods and experimenting with different capacitance variation functions.

# Preface

This project is written by a $4^{th}$ semester master student, Henrik Hansen, studying Energy (Mechatronic Control Engineering) at Aalborg University. It is written in the period 1. February to 31. May 2024, under supervision of Szymon Michal Bęczkowski. I would like to extend thanks to both my supervisors for their guidance during the project, and my fellow students for helping me keep sane. Furthermore i would like to, in no particular order, thank Claus Leth Bak, Asger Bjørn Jørgensen, Per Johansen, Elias Vagn Hansen and Paweł Kubulus for their patience in answering my many questions, and Henrik Nielsen for the extraordinary amount of help in designing and building the physical device.

During the making of this project, the following programs have been used:

- Overleaf LaTeX— For text processing and layout of this report
- MathWorks MATLAB — For calculations, modeling, simulation, data processing and many of the graphs
- Draw.io (app.diagrams.net) — For drawing circuit diagrams
- Altium — For designing the experimental PCB

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# Contents

# Introduction 1

When implementing a Field Effect Transistor, or FET, in a circuit, it is often necessary to similarly include a gate driver. These devices ensure that the gate is charged or discharged such that the FET either does or does not conduct. They do this by providing a current which is pumped into the gate in order to charge it to a specific voltage. When it reaches this voltage the FET turns on. To turn off the FET, a channel is opened from the gate to ground, discharging the gate. These are standard components which can be found in many different configurations, but almost all work on the same principles, using two small FETs in a push-pull configuration.
But what if the same function could be achieved in a different way? What if a single variable capacitor was used instead? Changing the capacitance of a charged capacitor will, in theory, change the voltage.

This idea formed by considering the Murata *LXRW19v201-058* tuning capacitor. This device is a physically tiny 1.3 x 0.9 mm variable capacitor with the ability to change the capacitance from 200 pF to 100 pF by applying 0–5 V on a separate input terminal[1]. This is an extremely attractive gate drive solution, as it is driven by logic voltage, is able to fit almost anywhere and, on top of it all, should be more efficient. Further, it could allow for easy programming of different voltage waveforms, allowing for more advanced control of the gate.
The device was therefore procured and tested, with the test board shown in Figure 1.1. While initial testing seemed promising, the device did not behave as expected. There is practically no information about what is physically happening in the device, so debugging was therefore a difficult process. Further looking into the device in the Questions and Answers related to it, a direct connection from the tuning terminals to the output terminals seemed to exist, which would impact the desired functioning significantly [2]. These factors hindered the testing of the initial idea, but the general idea stuck:

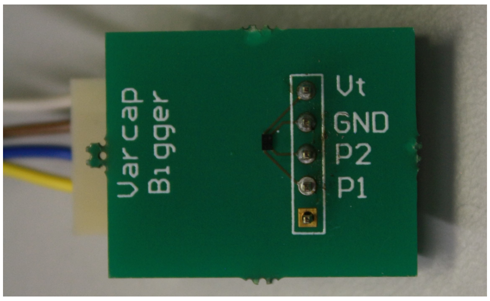


***Figure 1.1:*** The variable capacitor procured from Murata soldered to a printed circuit board.

*Can a variable capacitor be used to drive the gate of a FET, and what are the limitations of this technology?*

# Problem Analysis 2

The idea of using a changing capacitance to drive a voltage is initially a simple concept, but some mathematical rigor will shine a proper light on the applications and limitations.

Therefore, in order for proper analysis of the proposed idea, a mathematical model for changing the capacitance in a system has to be derived. There are two classes of model which are often used in mathematical modelling of physical systems, namely dynamic and static. In the case of the capacitor, both models can spring from the same source: the definition of capacitance. Capacitance of a two conductor configuration is defined as the charges accumulated in each conductor as a result of a voltage difference, as shown in Equation 2.1.

$$C = \frac{Q}{V} \tag{2.1}$$

This value is only dependent on the geometry of the two conductors and the permittivity of the insulating material [3, p.225-226]. Assuming charge to be constant, a relation describing the change in voltage for a change in capacitance in the steady state can be derived. This is the ratio described in Equation 2.2.

$$\frac{C_1}{C_2} = \frac{V_2}{V_1} \tag{2.2}$$

Equation 2.2 only holds if the system only consists of a single capacitor. While this is not truly representative of many useful systems, it does give insight into a fundamental analysis technique which can be used for variable capacitors. The ratio of the voltage change is equal to the ratio of the capacitance change. This ratio is an important tool, and is named the Capacitance Change Ratio, or CCR. The equation shows that decreasing the capacitance of the system will increase the voltage, and vice versa. In most systems there is not only a single capacitive effect. One way of modelling multiple capacitances can be done by changing the equation to include a 'DC-capacitance', which does not change. A DC-capacitance here describes a capacitance which is parametrically static, ie. that the capacitance doesn't change with time. Modeling the voltage rise this was is shown in Equation 2.3.

$$\frac{C_1 + C_{DC}}{C_2 + C_{DC}} = \frac{V_2}{V_1} \tag{2.3}$$

This equation reveals that the CCR for a system with multiple capacitive effects will always be smaller. The effect of the 'DC-capacitance' can be mitigated, however, by increasing the values of $C_1$ and $C_2$. If the ratio of $C_1$ and $C_2$ is kept the same, the resulting voltage rise or fall will only be minimally affected by the peripheral capacitances in the system. Equation 2.3 is a fundamental tool in analysing systems with a voltage change due to a changing capacitance.

The definition given in Equation 2.1 can be extended to describe the dynamics associated with a changing capacitance by taking its derivative with respect to time. Rearranging the equation such that only Q is on the left-hand side and taking the derivative yields Equation 2.4.

$$\dot{Q} = C\dot{V} + V\dot{C} \tag{2.4}$$

Dot notation is used for derivatives with respect to time. This equation can be useful for determining the flow of charges, ie. current, in the system, and how this affects the voltage. It can be rearranged to describe the changing voltage, shown in Equation 2.5.

$$\dot{V} = \frac{1}{C}(\dot{Q} - V \cdot \dot{C}) \tag{2.5}$$

This equation fits with what is expected for a variable capacitor. If the electrical current is positive, the voltage is expected to increase, and if the capacitance increases, the voltage is expected to decrease as per Equation 2.2.
A fascinating consequence of changing the capacitance of a capacitor, is that the stored electrical energy will also change[4, p.134-136]. This energy change is directly proportional to the change in capacitance. This is not of direct consequence in the analysis or design of the system, but is an intriguing facet.

## 2.1 Testing the Idea

From Equation 2.3, it can be seen that the capacitance of the system should be low compared to the variable capacitor, in order for the CCR to remain high. The load voltage variation should also be kept low, in order to require as low a biasing voltage as possible, making the design more accessible. One example of a system which operate in such conditions is a gate driver for FETs. If a GaNFET is used, the voltages are often low and the input capacitance is quite low as well. The initial idea of using the variable capacitance, then, happens to be a very appropriate test case. It does seem that some considerations must be made regarding the electrical circuit in order for an implementation to be successful.

### 2.1.1 Experimental Gate Driver Circuit

As was discussed previously the voltage change of the variable capacitor is directly related to the the initial voltage of the capacitor. This means that the capacitor will have to be charged, and a voltage of 0 V over the capacitor is not feasible. Further, it means that a higher bias-voltage on the capacitor will lead to a larger voltage change. The problem here, is that most FETs are not capable of handling more than 7–25 V. Therefore, a the circuit is designed around a DC-blocking capacitor. This allows for virtually any bias on the capacitor while also allowing for both negative and positive voltages on the gate signal. This circuit was originally designed by Paweł Kubulus, with additions from Szymon Bęczkowski. The experimental circuit is presented in Figure 2.1. The circuit is split up into four parts; Power supply, Variable Capacitor, Voltage Acclimation and Load. The power supply consists of a voltage supply and a diode. If the variable capacitor is connected directly to the voltage source, the changing capacitance will simply result

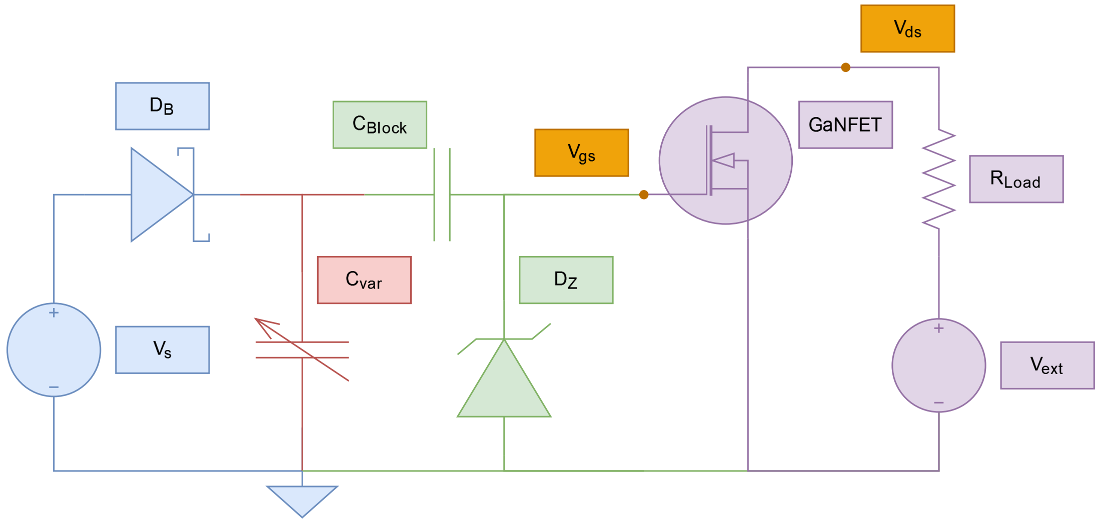


***Figure 2.1:*** The initial circuit used for simulation and experimentation. The points labeled $V_{gs}$ and $V_{ds}$ show where the voltage is measured. The blue colored parts are the Power supply, the red colored parts are the Variable Capacitor, the green colored parts are Voltage Acclimation and the purple colored parts is the Load.

in a current between the source and capacitor [4, p.135]. A diode is implemented to stop this from happening. If a PIN diode is used for this task, the phenomenon of reverse current will be present in the system. This means that for the diode to properly turn off, the depletion layer must be recharged. This uses valuable current, which is needed elsewhere in the system. Therefore, the diode implemented is a schottky diode, as the reverse recovery current is negligible. The specific diode used is a BAT85. The voltage acclimation consists of the DC-blocking capacitor and a zener diode. While it should be possible to predict the maximal and minimal voltages with some accuracy, a zener diode is implemented as a protection strategy for the gate of the GaNFET, in case the voltages should rise above or fall below safe limits. The specific zener diode used is a BZX79C6V2.

The load can consist of different elements, but as the circuit will function as a gate driver, a FET is chosen as the load. The chosen FET is a *GS-065-004-1-L* from GaN Systems. This has an almost constant input capacitance of 26 pF and a typical threshold voltage of 1.7 V. The load resistor is chosen as 100 Ω and the load voltage is chosen as 10 V. One would be forgiven for thinking that the DC-blocking capacitance in the voltage acclimation needs to be chosen carefully, in order to balance some peculiar trade-off. If the capacitance is so sensitive to changes that a difference of only a couple of picofarads is significant, surely the capacitance implemented in the voltage acclimation must need to be chosen with great care. This is, however, not the case. In fact, the larger the capacitance is chosen to be, the better. This rather unintuitive fact is a consequence of the circuit layout, which places the capacitance of the voltage acclimation in series with the load capacitance. Since the resulting capacitance of two capacitors connected in series can never be higher than the smallest of the two capacitors, the capacitance 'seen' from the variable capacitor can never be higher than the smallest capacitance. But if that is the case, then why not pick the DC-blocking capacitor to be incredibly small? By the same principle, the capacitance which the variable capacitor sees will become basically non-existent, and the CCR will be unaffected by the load. While this is true, the two capacitances also act as a voltage divider, and the higher capacitance will experience less voltage. This means that as the DC-blocking capacitance lowers, the voltage over the load lowers as well. For these reasons, it is most effective to pick a relatively high capacitance in the filter. This just leaves choosing the variable capacitor.

### 2.1.2 Improvising a Variable Capacitor

As the Murata *LXRW19v201-058* was unfortunately not deemed a viable candidate for testing, an alternative must be chosen. While there are many different types of variable capacitors on the market, there are only few which are workable. These few consist mainly of different types of microphones. Each viable type does come with caveats with the electret microphones very often being built with a pre-amplifier, and condenser microphones being very expensive. It was therefore chosen, that a plate capacitor should be quickly built as a proof of concept. Not much analysis was done, as this was simply a test to see if the idea could be put into practice. To design the capacitor, a parameter needs to be chosen to be variable. It was chosen that the capacitor should take the form of a plate capacitor, and looking at the equation for a plate capacitor, presented in Equation 2.6, there are three parameters to choose between.

$$C_{plate} = \frac{\epsilon_0 \epsilon_r A}{d} \tag{2.6}$$

This can either be the area A, the distance $d$ or the relative permittivity $\epsilon_r$, as the vacuum permittivity is seemingly a fixed parameter inherent to our universe. The parameter chosen to be variable was the relative permittivity, as this can easily be set up. The capacitor then consists of two aluminium plates, held in place by two wooden blocks. A piece of plexiglass, acting as a dielectric material, is inserted in between the two plates, which can then be ripped out from between them. This will lower the capacitance, which should cause an increase in the voltage over the capacitor. A picture of the constructed capacitor is shown in Figure 2.2.

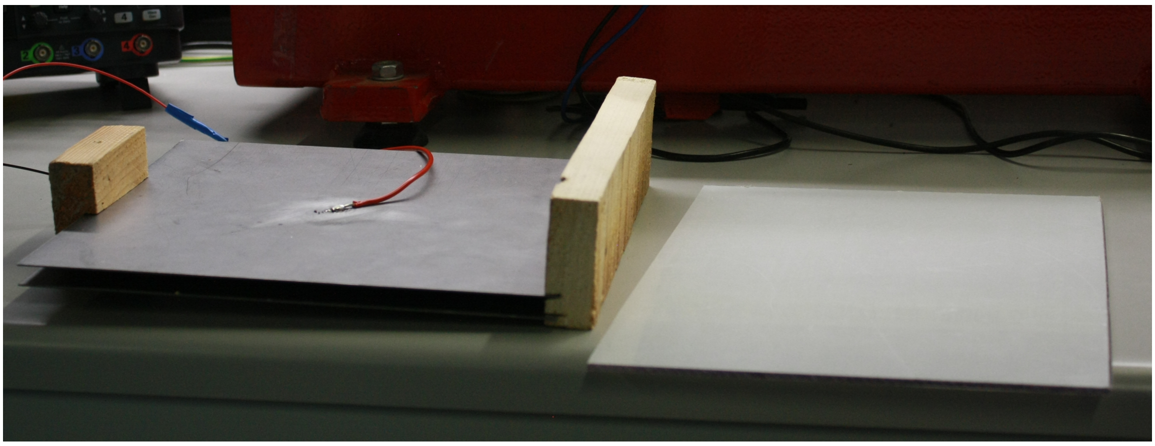

***Figure 2.2:*** The IVaCaT. On the left are the plates which are charged. On the right is the dielectric plate which is ripped from in between the plates, to change the capacitance.

The capacitor consists of two aluminium plates with a wire soldered to each. The plates are separated by two pieces of wood, and a piece of plexiglass is inserted between them. This device is dubbed the 'Improvised Variable Capacitor from Trash', or IVaCaT. The specific increase in voltage is practically unpredictable, as the change and rate of change of capacitance depends on the specific motion of the moving dielectric. This motion is not constricted by anything other than the person moving it, and ensuring a repeatable, fast motion made by an untrained person is difficult. The circuit shown in Figure 2.1 is created on a breadboard, with a DC-blocking capacitor chosen to be 100 nF and a *BZX79-C6V2* zener diode, which should limit the gate voltage to 6.2 V.

The experiment is conducted and the gate-source and drain-source voltages are shown in Figure 2.3.

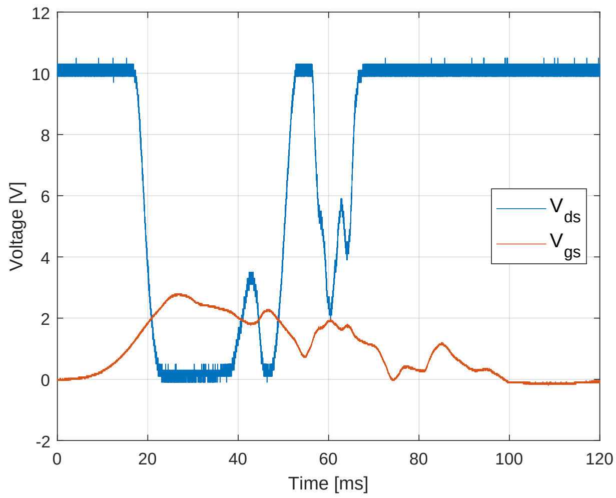


***Figure 2.3:*** The voltages of the GaNFET during the experiment using the IVaCaT.

The figure shows a turn-on of the GaNFET. It is difficult to say specifically when the plexiglass starts moving, but the gate voltage starts to increase at approximately 10 ms. It then increases until it hits the plateau voltage where the GaNFET starts to conduct. This conductive period lasts for about 12 ms. After this, the gate voltage becomes erratic, leading the drain voltage to become erratic as well. Furthermore, performing the experiment confirms the rather obvious notion that this specific implementation is not suitable for periodic switching.
The experiment shows that it is possible to both change the voltage over a capacitor by changing the capacitance, and to use this changing voltage to turn on a GaNFET. It successfully demonstrates that the idea presented in the introduction has merit, but also shows that it is not necessarily trivial to implement.

### 2.1.3 Simulation Study

As a further test of the viability of the idea, a simulation model was constructed to ascertain the importance of various parameters in the system. The simulation software chosen is Simscape, as the effects of a varying capacitance can be simulated directly. The circuit shown in Figure 2.1 is constructed in the software, with the GaNFET being estimated as a series capacitor and resistor in parallel with a leakage resistor. The capacitor is set to 26 pF and the series resistor is set to 4 Ω mimicking the characteristics of the GaNFET gate. The load leakage resistor is initially set to be 10 MΩ. The variable capacitor is estimated to have a leakage resistance of

1 MΩ. The diodes are modeled as ideal diodes, the zener with a breakdown voltage of 7 V and the DC-blocking capacitor is chosen to be 100 pF. The simulation model is shown in Figure 2.4. The capacitance is chosen to be a bounded triangle wave, to mimic the time it would realistically

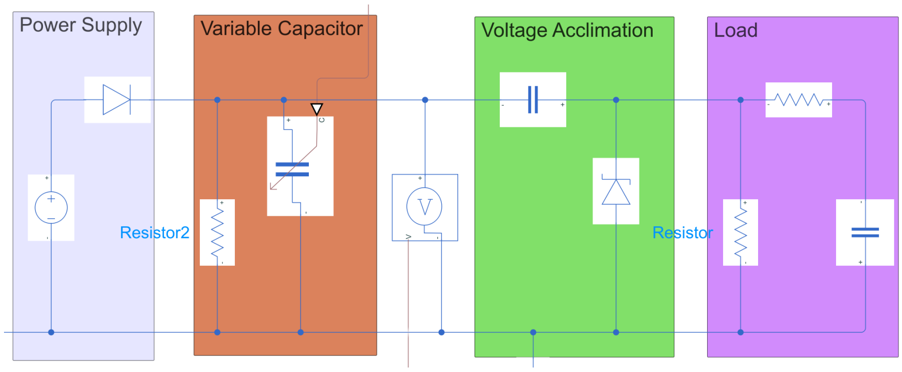


***Figure 2.4:*** The initial circuit as constructed in Simulink.

take to change the capacitance. The values vary from 25–50 nF, with a frequency of 25 Hz. Running the simulation reveals some interesting things about the circuit. Firstly, the leakage resistance seems to have a big impact on the functioning of the system, both for the variable capacitor and for the load. This can be seen in the comparison of the capacitance change and the voltage over the variable capacitor, graphed in Figure 2.5. The capacitance change is much

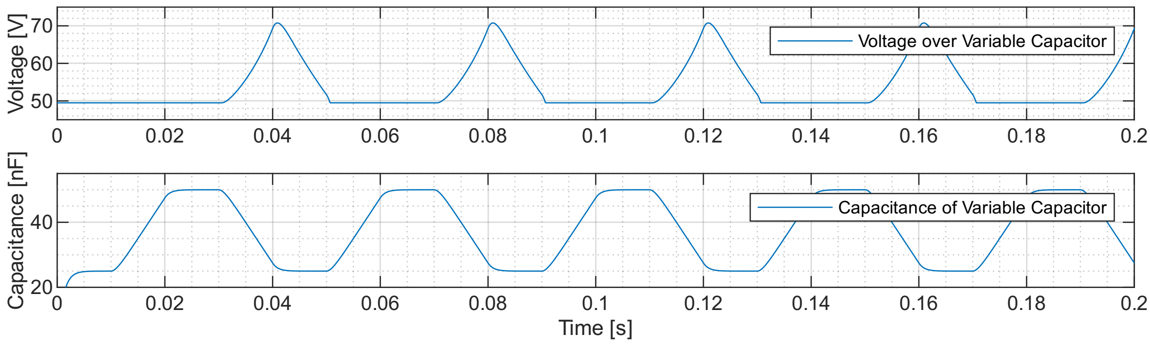


***Figure 2.5:*** The capacitance of the variable capacitor, and the voltage over the variable capacitor.

larger than the load capacitance, and the voltage is therefore assumed to increase until it reaches double the biasing voltage of 49.5 V. The voltage reaches just above 70 V before dropping rapidly back to the biasing voltage level. All of this happens before the capacitance increase, which is what should drive the voltage to a lower value. This is likely due to the leakage current, even when the leakage resistor is at 1 MΩ. It is then natural to conclude that this is also the reason for the voltage not reaching 100 V. As the current pushed into the system by the variable capacitor is pulling the voltage higher, the leakage current is dragging the voltage down, leading to a lower overall voltage. This is confirmed if the leakage resistance of the variable capacitor is set to 10 MΩ. Graphs showing the capacitance and voltage of the variable capacitor is shown in Figure 2.6. As the leakage resistance increases, the rate of voltage change goes down. This is an obvious, but important, result, as it illustrates the size of what a 'low' resistance is. This again shows that while the concept works, successfully implementing a device which operates in the expected manner is not a trivial matter. Finally, the concept of the CCR was introduced in at

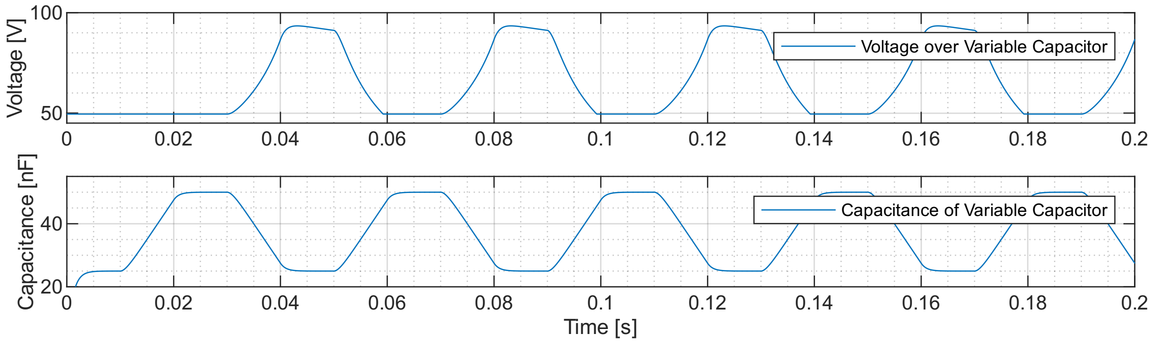


***Figure 2.6:*** The capacitance of the variable capacitor, and the voltage over the variable capacitor. Here the leakage resistance over the variable capacitor is increased tenfold.

the start of the chapter. If this is to be used as an analysis method, it should be tested in a sterile environment. If it cannot succeed here, it is unlikely to succeed in the physical world. To test its feasibility, the circuit is modified to have a 1 pF load and no leakage currents. The zener diode is also removed and the input voltage is increased to 50.5 V to negate the forward voltage drop of the power supply diode. The capacitance is then varied as before, but at with a less smooth waveform. The voltage is expected to follow an exponential path from 50 V to 100 V, and then return to 50 V. The results of the simulation are graphed in Figure 2.7. The voltage

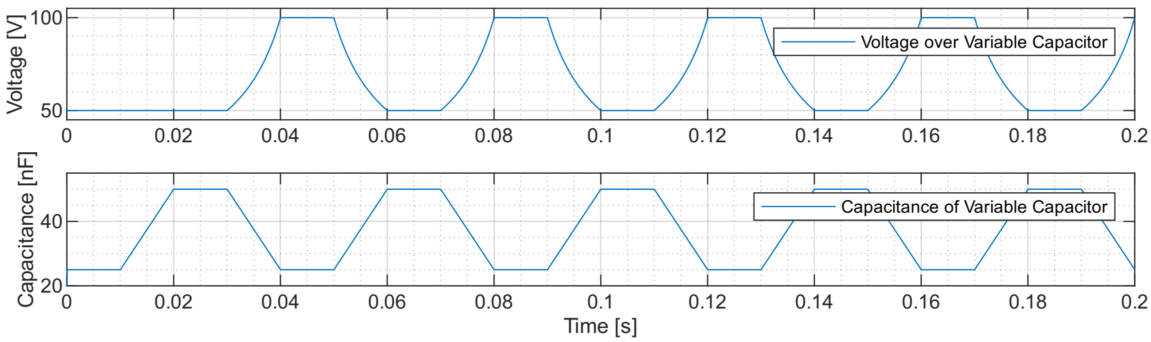


***Figure 2.7:*** The capacitance of the variable capacitor, and the voltage over the variable capacitor. Here the leakage current is set as close to zero as is viable.

follows the expected path, which is a good sign for the CCR to be a useful tool. A final tests can be conducted, where the capacitance change occurs over a much shorter time span. This should push a much larger current through the system, but for a shorter period of time, and the resulting voltage should stay the same. The results for this test is plotted in Figure 2.8. The only difference between the outputs of the two previous experiments is the time it takes for the voltage to reach 100 V. This is a good sign, and indicates that the CCR is a usable tool in the analysis of these systems.

So, armed with tools for analysis, an indication that the concept is viable and an interest in exploring this technology further, the idea must be formalized.

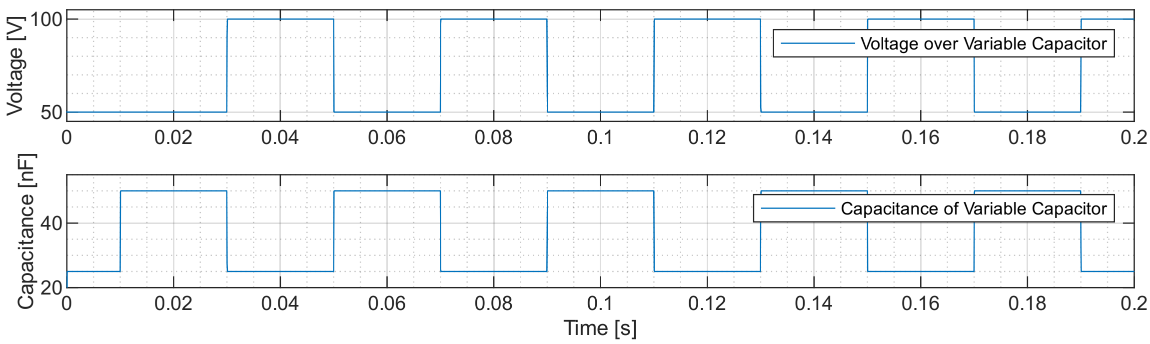


***Figure 2.8:*** The capacitance of the variable capacitor, and the voltage over the variable capacitor. Here the leakage current is set as close to zero as is viable, and the capacitance changes rapidly.

# Problem Statement 3

*How can an actuator be constructed, which can change a voltage by changing the capacitance, and is it useful as a gate driver?*

Answering the problem statement involves accomplishing the following objectives:

- Designing a variable capacitor, including the mechanism for capacitance variation and auxiliary support components
- Constructing the variable capacitor
- Experimentally validate the functioning of the constructed capacitor

## 3.1 Project Scope and Reading Guide

This project will focus on designing, testing and exploring the specifics of a single variable capacitor. While the concept of the variable capacitor has been known for a long time, they have mostly seen use in extremely high voltage applications[5], as various sensors[6] or as low power energy harvesting devices[7, p.7]. Their use in more commonly approachable scenarios are limited to demonstrations of electrostatic concepts.
The project is, as a consequence of this, an exploration into the design and use of such a device. With only very few existing guidelines and analysis techniques, an investigative attitude is necessary, and very much a guiding force in this project.
The structure of this project is then much like the branches of a tree. Experiments may lead to interesting discoveries which are explored as they are uncovered.
With this attitude steering the project, it should also be mentioned that not everything can be explored in equal depth. The design and implementation of various capacitors is, for instance, not a point of focus, as it would take a lot of time. Similarly, the implementation of a constructed variable capacitor into several different 'cases' is not viable. Again, the time spend here is too great compared to the potential output of following this branch. This project is a proof of concept and not made to construct a fully commercially viable product.
The focus is therefore on the design, parametrisation and implementation of a single variable capacitor, with the potential for some iterations on the design to be made.

# 4 Designing the Variable Capacitor

In this chapter, the process of designing a variable capacitor is presented. This means that everything from choosing how to actually vary the capacitance and figuring out the general structure of the device, to presenting the specific design specifications and drawings.

## 4.1 General Structure of the Variable Capacitor

In order to vary the capacitance of a device, the elements which can be varied must be identified. In general, capacitance depends on only two factors, namely the geometry of the conductor configuration, and the permittivity of the material between the conductors [3, p.226]. To gain a more tangible sense of what this actually means, the simplified model of a plate capacitor is again used as an example. Equation 4.1 shows this simple model for a parallel plate capacitor.

$$C_{plate} = \frac{\kappa \cdot \epsilon_0 \cdot A}{d} \tag{4.1}$$

Here, A describes the area of the parallel plates, d describes the distance between them, $\epsilon_0$ denotes vacuum permittivity and $\kappa$ describes the relative permittivity of the material between the plates [3, p.228]. Both the area and the distance then describes the dominant geometry of the capacitor. This model is simplified so that fringing fields are neglected, which also means that the only relevant permittivity is the permittivity of the material directly in between the capacitor plates. While this model does not fully describe the capacitance of this configuration, it serves as a useful tool in identifying what can be changed. As the vacuum permittivity is a physical constant, there are 3 variables which can be changed in this model: the relative permittivity, the distance between the plates, and the area of the plates.

### 4.1.1 Choosing the Variable Parameter

Now that some tangible variables have been identified, the next step is to choose which to vary. Even though the design process could offer more flexibility if several variables are allowed to change simultaneously, the increased complexity of design and construction could extend the time before a finished product is available, significantly. Therefore, in order to simplify the design, it is chosen that only a single variable is to be varied.

### Varying the Relative Permittivity

Varying the relative permittivity can be done in several ways. One way it can be done is by changing the material between the plates. For instance, as was done in Section 2.1.2, if a plate capacitor is constructed with the gap between the plates being filled by a sheet of plexiglass this construction will have some capacitance $C_0$. If the capacitor is charged to 1 V, and the plexiglass is then removed, the voltage will rise. The equation describing the steady state rise in voltage can be derived from Equation 2.2 and Equation 4.1, resulting in Equation 4.2.

$$V_2 = V_1 \cdot \epsilon_{r plexiglass} \tag{4.2}$$

Numerically, as the relative permittivity of plexiglass is 3.4 [3, p.470], the voltage will rise to 3.4 V.
Practical implementation of such a device carries with it some difficulties. Filling out the whole cavity between two plates with a material is effectively impossible. This means that the material filling out the remaining space between the plates modifies the resulting capacitance change, likely decreasing the effective relative permittivity[4, p.134]. This can be solved by using a fluid as a dielectric and moving a solid through this fluid, but then the problem of actually containing the fluid arises. While changing the dielectric serves as a useful tool for demonstration of the effects of a changing capacitance, it is substantially more difficult to implement properly. It is therefore not chosen as the varying parameter.

### Varying the Distance

Varying the distance between the plates needs to be treated slightly differently from the other parameters. Varying either the relative permittivity or the area will change the capacitance linearly, but the distance between the plates has an inverse relation to the capacitance. This means that an absolute change in distance between the plates will have a greater effect on the capacitance the closer the plates end up being.
To demonstrate, a capacitor which varies distance is designed. The CCR is chosen to be 4 and the minimal capacitance should be 1 nF. The area is chosen as 0.100 $m^2$. Equation 4.1 is solved for d, and this is used to calculate the two distances. For this configuration, the maximum distance should be 885 µm and the minimum should be 221 µm. So by changing the distance by only 664 µm the capacitance can be varied from 1–4 nF, and if the plate is moved only 44.3 µm more, the ratio is changed from 4 to 5. While this is the greatest strength of varying the distance, it is also its greatest challenge. The distance needed to increase the CCR from 4 to 5 could be covered by the plate flexing. As the capacitance is to change periodically, a periodically varying force from the periodic movement could induce this flexing and greatly change the actual CCR from the predicted one. This is further complicated by the challenges which arise from actually moving a plate such small distances in a fast, repeatable manner. The distance could be increased while holding the capacitance at a similar value by increasing the size of the area, but there is also a practical limit to how big the plate and surrounding movement mechanism can be made. For these reasons the distance is not chosen as the varying parameter.

#### Varying the Area

As it was chosen that the variable parameter should be neither varying the relative permittivity, nor the distance, varying the area is selected by process of elimination. But varying the physical, actual area of the two plates is an effectively impossible task. A alternative method of achieving something similar is therefore chosen. Instead of varying the area, the 'Effective Area' is chosen in its stead. If fringing fields are neglected, the overlap of two non-contacting conductive plates in the x-y plane will directly correspond relate to the capacitance. Varying how much the plates overlap is then as easy as moving one of the plates relative to the other. An illustration of this is presented in Figure 4.1.

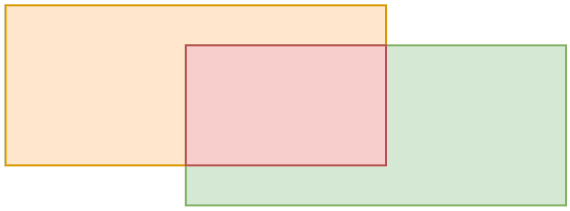

***Figure 4.1:*** The area shaded red is what is described as the effective area.

It is important to emphasize that this is only truly correct if fringing fields do not exist. The definition implies that if there is no overlap, the capacitance between the plates is zero, which is simply not true. But if the size of the overlap is much greater than the distance between the plates, the assumption will hold in the same way that the common model for a plate capacitor holds. As the parameter which is to be varied is chosen, the mechanism for how to vary this is investigated next.

## 4.2 Designing the Variation Mechanism

The parameter which has been chosen to be varied is the effective area. On the journey to a fully fledged design, however, some further choices must be made to put further restrictions on the design. One such choice is that none of the live terminals should be moving. The reasons for choosing this is twofold. Firstly, electrically connecting a rotating and stationary body is significantly more complicated than electrically connecting two stationary bodies. In order to do this, a special connector is needed, which complicates the design. Secondly, having a constantly moving live contact can become dangerous in case of a structural failure, or rapid unscheduled disassembly. For these reasons, the live contacts are chosen to be stationary. Furthermore, the variation mechanism needs to be designed with periodic motions in mind.

### 4.2.1 Designing the Capacitive Connection

The fact that both electrical contacts are to be kept stationary introduces a problem, since changing the effective area will require the movement of at least one plate. This can be solved by constructing two variable capacitors in series with one another. If a circuit is constructed with two parallel conductive plates lying on the same plane, a conductive plate placed above these two will act as a capacitive connective node between the two parallel plates. This is better illustrated graphically. Two figures are provided; a side view of a possible implementation in Figure 4.2 and a circuit diagram of the possible implementation in Figure 4.3.

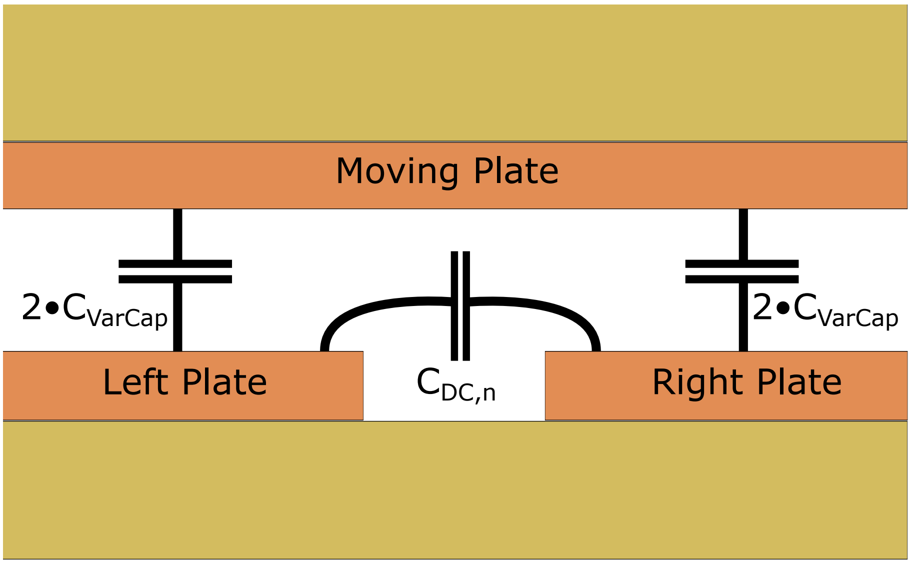


***Figure 4.2:*** Two conductive parallel plates on the bottom serve as the contacts of the circuit. The plate on the top is moved such that it overlaps more or less of the plates below, changing the effective area which changes the capacitance. A circuit representing the situation is shown in Figure 4.3.

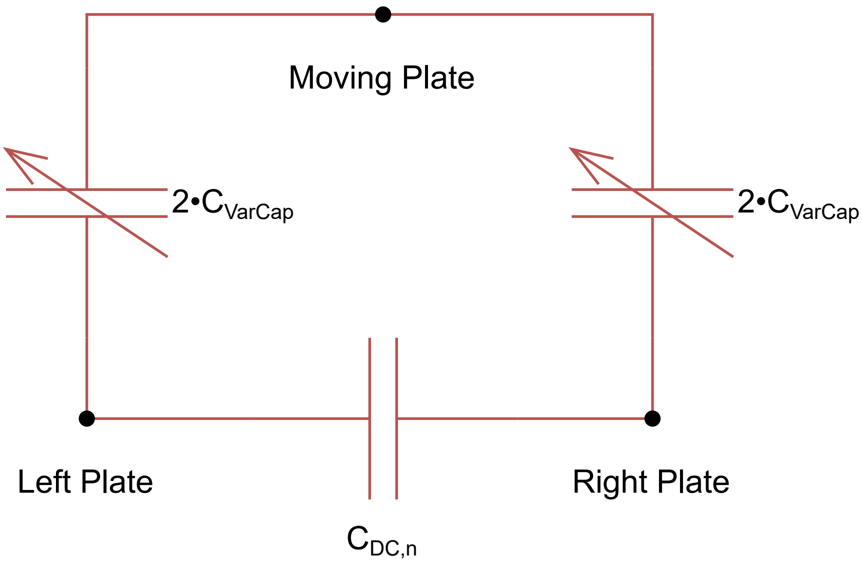


***Figure 4.3:*** A circuit model of the situation presented in Figure 4.2.

In this implementation strategy, the 'Left Plate' and 'Right Plate' represent the live terminals connected to the circuit. These terminals each have a capacitive coupling to the moving plate, which acts as a 'bridge' between them. If the 'Moving plate' is then moved either left or right, the effective area of the plates will change, thereby changing the capacitance connecting either terminal to it. This configuration is then able to change the capacitance of the system continuously. Apart from the capacitance from each of the stationary plates to the moving plate,

there exists several unwanted DC-capacitances, represented in the figure as $C_{DC,n}$. Here, the n signifies that there are many more than the one drawn in the figure, however the capacitance between the plates will most likely account for a significant contribution to this value. While the ability for the live terminals to be stationary is achieved in this configuration, it does come at a cost. The maximum capacitance is at best one fourth of the value of an equivalently two-plate capacitor. Firstly, as the variable capacitances are connected in series in the circuit, the capacitance will be halved. Secondly, the area used by the moving plate needs to be split, at least, in half for left and right plates, as they are not allowed to touch. More distance between the two plates will also decrease the DC-capacitance. The potential maximal capacitance, and therefore the CCR, is therefore lowered by using this configuration. This tradeoff is deemed acceptable.
A positive consequence of this type of design is that an electrical connection does not have to be made between a stationary and a moving body. While these are possible to make and are used in tehcnologies such as DC-motors, they carry with them an increase in design complexity. This type of technology is called a 'Slip Ring'[8]. Mechanically connecting slip rings are prone to wear and tear, and excluding this from the design, eases the design process and removes a point of failure in the system.

### 4.2.2 Moving the Plates

There are two general ways of moving the 'Moving Plate', either linearly, or rotationally. When making this choice, the fact that a periodic output voltage is desired needs to be taken into account. It forces the motion to take a periodic form as well, and this is achieved differently with the different types of motion.

A linear movement of the top plate can be done by sliding the plate over the two bottom plates as shown in Figure 4.4 (a). This type of movement could see the plate moving back and forth along the axis of the arrow sinusoidally. This would lead to the effective area to increase and decrease sinusoidally as well. To achieve this, the speed, acceleration, jerk, etc. of the plate will need to be constantly varying.

A rotational movement of the plate could be done by spinning the plate around a suitably placed axis, as shown in Figure 4.4 (b). One upside of this is that the rotational motion innately achieves the requirement that the motion should be periodic.

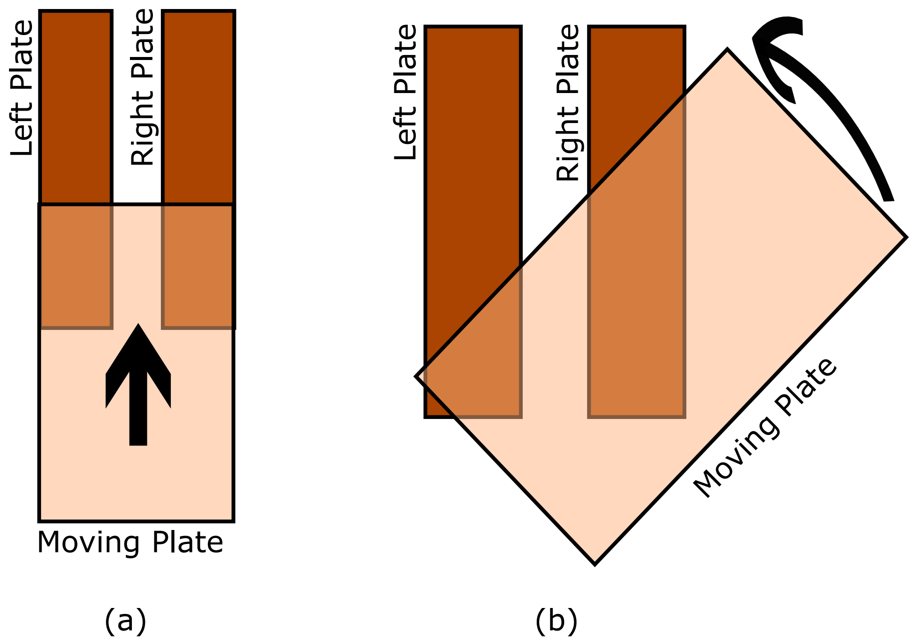


***Figure 4.4:*** Two different ways of moving the 'Moving Plate' relative to the left and right plate. The arrows each signify the direction of movement for the 'Moving Plate' in their respective configuration.

While both ways of moving the plates have upsides and downsides, rotational movement is chosen. This is due to the fact that rotational motors are readily available, and only a minimal amount of support is required to counteract the forces associated with this type of motion. While the speed or torque of any motor can be augmented with the use of gears, this is not utilized here, in order to simplify the design process.

## 4.3 Designing the Conductive Plates

The conductive plates have so far been depicted as two parallel plates of an arbitrary thickness being some distance apart, with another plate placed over them. In this section, these loose definitions are brought to heel, and the design of the plates is considered. This design process can be approached in a number of different ways. A numerical solver could be configured to solve the Maxwell-Heaviside equations for several geometries. These geometries could then be optimised such that a potentially more well known design could be constructed, possibly leading to a more robust device. In order to set up such a solver, however, its functionality must be verified against a known system, and it can take a long time to construct a simulation which can be trusted. Therefore, in the interest of time, this path is not chosen.
As the device is meant as a proof of concept, the design is considered in a more practical sense. The two parallel plates are both stationary, and can therefore be connected mechanically by a non-conductive plate. This setup can be fairly easily achieved by using a printed circuit board, or PCB, which is true for the moving plate as well. Therefore two PCBs are constructed, one with the two parallel plates dubbed the 'stator' and one with the moving plate dubbed the 'rotor'. The PCBs have a maximum size of 160 mm times 260 mm, with a minimum clearance of 0.2 mm between traces.

### 4.3.1 Desired Capacitance Variation

One of the main factors to consider when designing how the plates are to be shaped and placed, is how the desired capacitance variation looks. The ideal gate voltage is shaped like a square wave with somewhat smoothed corners. Achieving this requires a near infinite rate of change of capacitance, which is somewhat difficult to achieve. But a more realistic goal can be extracted from this.

The voltage of the gate driver seeks to be low for some time, followed by a rise in voltage to some value, which is maintained for some other time, concluded by a return to the low voltage. As long as the periods of transition in between the voltage plateaus do not contain voltages which exceed the maximum safe gate voltage, it is not of great importance how it looks. This is a simplification, of course, but it holds well enough if the transition is smooth and does not include high frequency steps or changes. From this the rough shape of the capacitance variation function can be learned. A plateau of capacitance, followed by some smooth transition into another plateau, and then a smooth transition into the first capacitance plateau. A representation of this function is shown in Figure 4.5.

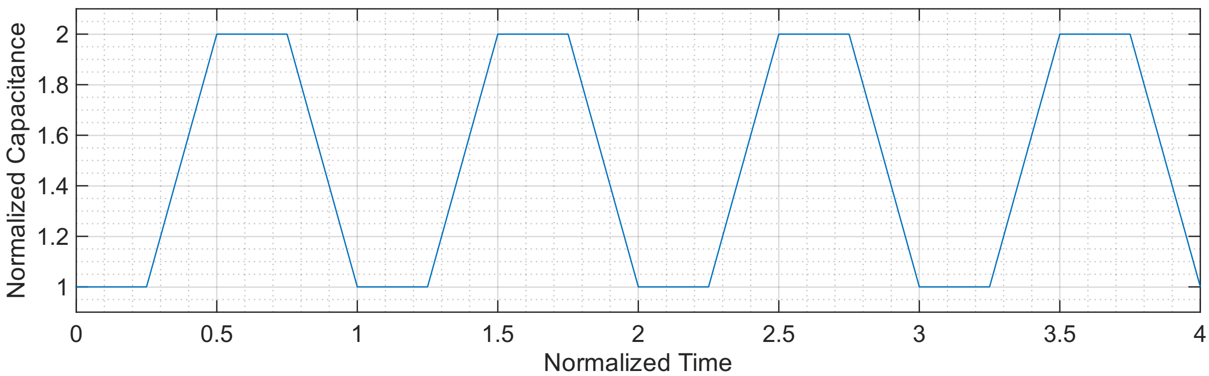


***Figure 4.5:*** The desired capacitance variation function.

This means that moving plate, should be not just as wide as the two stationary contacts, but rather it should be some amount wider to allow for the capacitance to plateau at a high value. Further, it also means that there should be some time period where the moving plate does not overlap both the stationary contacts, to allow for the capacitance to plateau at a lower value. The ratio between these two amounts will then determine a 'duty cycle'. With the period of the capacitance variation described, it is time to look at how a design of the plates might achieve this.

### 4.3.2 The Spokewheel

The rotational actuator is chosen to be a brushed DC-motor, due to its ease of operation. The selected motor is a King Right 7152 as it had the highest speed of the readily available motors. This motor has a rated speed of 3000 rpm, which corresponds to 50 Hz. This is a rather low frequency when it comes to switching a GaNFET, so a trick is borrowed from the design of many electrical motors. In some electrical motors, the concept of 'pole pairs' is used to increase the electrical frequency while keeping the mechanical frequency the same. The same trick can be used here with the two parallel stationary contacts acting as the pole pair, here being dubbed a 'spoke'. If two spokes are placed, one at 0° and one at 180°, the moving plate will overlap both contacts twice per rotation. This doubles the electrical frequency, and if the moving plate is equally designed with a matching plate shifted by 180°, the total area of overlap should not change. This means that the rate of change of capacitance can be increase while keeping the capacitance the same by increasing the number of spokes. The relation between the electrical and mechanical frequency is the given in Equation 4.3 and looks much the same as for an electrical motor.

$$\omega_e = Spokes \cdot \omega_m \tag{4.3}$$

Here, $\omega_e$ represents the frequency of the electrical system, ie. the capacitance change, $\omega_m$ represents the mechanical frequency of the motor and *Spokes* is the number of spokes in the design. This is a powerful tool, but as the saying goes, 'there is no free lunch' and the increase in the amount of spokes will actually decrease the possible overlap area. The drawing in Figure 4.6 has been made to illustrate why this is happening. Due to the resemblance of the proposed design to spokes in a wheel, the design is dubbed the 'Spokewheel'.

***Figure 4.6:*** An illustration of how increasing the width decreases the possible overlap area. The figure shows two PCBs made in Altium, with one being overlaid on the other, such that a direct comparison can be made

The illustration shows that an increase in the width of a plate will increase the area where the plates overlap. It is shown here for width, but the concept is equivalent for an increase in the amount of spokes. This is unacceptable, as the area where the plates overlap can not lead to a change in the capacitance, as the effective area will remain constant. The radius of the circle where this happens can approximately be calculated by considering the sum of the widths of each spoke on the rotor and adding those together. This is then approximately the circumference of a circle, and using this value, the radius of this circle can be found. The reason for using the rotor traces is that these are going to be wider that the combined width of the stationary plates to create the capacitance plateau at a high capacitance. The radius of this circle describes the distance from the center of the rotor, where the rotor plate will intersect with its neighbours, and no variation of overlap will occur. This then effectively corresponds to lost area of the plate capacitor.

### Estimating Capacitance

If the capacitance is estimated, a graph describing the amount of capacitance for a given amount of spokes can be constructed, which can aid in picking the number of spokes. The shape of the spokes has an effect on how to choose this, as the spokes could be made from the area between two non-parallel lines, instead of a single rectangular plate. This can be achieved by essentially 'transforming' the cartesian coordinates to polar coordinates. The angles of the edges of the plates can then be made to ensure that the area of the plates remain fixed, and that a specific rotational 'distance' can be set. This would allow for a design targeting a specific duty cycle. Although this is possible, it would make the design significantly more complex, and the potential gain for a proof of concept design is slim. Straight plates, as shown in Figure 4.4 are therefore used. As described in Section 4.2 the capacitance can be modeled as two capacitors in series. If each sub-capacitor is then modeled as a basic plate capacitor, the total capacitance can be calculated from this.

Doing this requires defining the size of the individual plates. The maximal length can be found from the length from the middle of the PCB to the shortest edge. This is of course shortened by the radius of the previously discussed circle where no capacitance variation can take place. The radius is defined by the width of the rotor plates, which is defined by the width of the stator plates. A ratio of the width of the rotor and stator plates which forces a specific duty cycle can be found, but this is not a necessary design criteria and will only serve to complicate the design further. It is therefore chosen that the rotor plate should be twice as wide as the the sum of the widths of the two stator plates and the gap between them. This is show mathematically in Equation 4.4 with $w_R$, $w_S$ and $w_G$ being the width of the rotor plate, the width of the stator plate and the gap between the stator plates respectively.

$$\frac{w_R}{w_S + w_G} = 2 \tag{4.4}$$

This means that only the width of the gap and the stator plates must be chosen. A larger gap between the stator plates will decrease the unchanging capacitance between the plates, but it will also decrease the area used for creating a capacitance. As the stator plates are perpendicular to each other, and the height of a PCB trace is very small compared to the width, the width of the gap is chosen to be small, specifically 0.4 mm. The choice to make this gap small, will also affect the leakage current, with a smaller gap decreasing the leakage resistance.

The width of the stator plates can be chosen in many ways, and the smaller they are, the more can fit on the board and the higher the electrical frequency will be. For smaller traces, the assumption that the fringing fields are negligible become less and less valid. This can lead to unexpected couplings which may decrease the capacitance variation. It is therefore chosen that the width of the stator traces should be much wider that the chosen gap width, specifically 5 mm.

With these measurements the rotor trace width can be calculated to be 20.8 mm. The radius can then be calculated as in Equation 4.5.

$$Rad_{min} = Ceiling\left(\frac{Spokes \cdot w_R}{2\pi} \cdot 1.1\right) \tag{4.5}$$

Here, the Ceiling function rounds the distance up to the nearest mm. The reason for the radius being rounded up to the nearest mm is to minimize the risk that the PCB will contain manufacturing errors. The reason for the radius being increased slightly is to ensure that there is space for screws to attach the PCB to some mount. The calculated distance can then be used in the estimation of the capacitance.
The equation used for estimating the capacitance is given in Equation 4.6

$$C_{est-max} = \frac{1}{2} \cdot \text{Number of Spokes} \cdot \epsilon_0 \cdot \frac{w_R \cdot (Rad_{max} - Rad_{min})}{2 \cdot \text{Distance}} \tag{4.6}$$

For this estimation, the distance between the rotor and stator plates, named 'Distance' in the equation, is assumed to be 0.5 mm. $Rad_{max}$ represents the distance from the middle of the PCB to the nearest edge. The reason for the capacitance estimate being halved is that the two capacitances are in series, which for two equally big capacitances ends up halving the total capacitance.
Using Equation 4.6 and varying the Number of Spokes from 3 to 20 produces a set of capacitance estimates, which are shown in Figure 4.7.

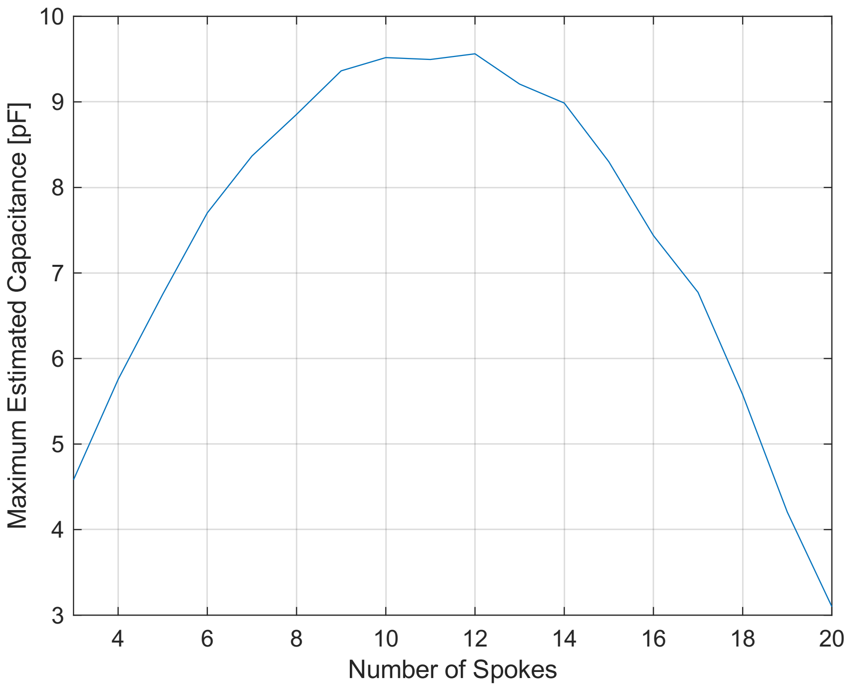


***Figure 4.7:*** The estimated capacitance depending on the number of spokes, calculated using Equation 4.6.

The figure shows a undeniable trend, with the optimal amount of traces being between 10 and 12. An even amount of traces will assure discreet rotational symmetry around the axis of rotation, and is therefore a desirable trait. While choosing 12 spokes would result in a slightly faster

electrical frequency, 10 spokes will result in fewer potential points of failure. The amount of spokes is therefore chosen to be 10.
To sum up, the chosen plate parameters are presented in Table 4.3.2.

| Rotor Plate Width | Stator Plate Width | Distance Between Stator Plates |
|---|---|---|
| 20.8 mm | 5 mm | 0.4 mm |

A quick comment should be made about the amplitude of the capacitance. This capacitance is somewhat lower than the what is ideal. As discussed in Chapter 2, the variation in capacitance should be much higher than the unchanging capacitance, to ensure the highest CCR. The expected load capacitance in the system is approximately 30 pF. Using this, a calculation can be made to predict the performance of the variable capacitor. In the best case, the variable capacitor will vary between 0–9.52 pF. The resulting CCR with the expected load is then 1.32. This means that to achieve a voltage change of 10 V, the variable capacitor will have to be biased at 31.5 V. This is an easily achievable voltage with the available laboratory gear. Even if the CCR ends up being half of the calculated value, a sufficient voltage change should be achievable.

#### Placing the Plates on the PCB

With the amount of spokes determined, along with the dimensions of the plates making up the spokes, the PCB can be properly designed. A method for finding the coordinates of the start and end points of the traces on the PCB is to use a rotation matrix. This matrix will transform a set of coordinates by rotating them around a chosen point, which is perfect for making a discreetly rotationally symmetric structure such as this. The matrix for a 2 dimensional rotation is given in Equation 4.7.

$$\begin{bmatrix} x' \\ y' \end{bmatrix} = \begin{bmatrix} Cos(\theta_{spoke}) & -Sin(\theta_{spoke}) \\ Sin(\theta_{spoke}) & Cos(\theta_{spoke}) \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix} \tag{4.7}$$

A set of coordinates $x$ and $y$ are to be chosen as the starting point of each of the rotor plates. These are determined from a the previously chosen widths and calculated radií. The angle $\theta_{spoke}$, is then calculated by dividing the circle into an amount of pieces equal to the chosen number of spokes, and multiplying by the number of spoke to be placed. The rotation matrix then calculates $x$' and $y$', which are the coordinates rotated by the angle $\theta_{spoke}$ around the origin, which is placed at the middle of the PCB. This is used to calculate all but the starting set of coordinates.

### 4.3.3 Attaching the PCBs

The faces of the two PCBs are going to be very close to each other. This is an issue as it is necessary for some attachment point, between the stator PCB and whatever structure is holding it, to exist. The same issue also exists for the rotor PCB. Any height on the attachment points is a hard limit on the minimum distance between the plates, so this should be minimized or avoided. As the width of the moving plate is larger than the combined width of the two plates on the stator, the radius of the circle where overlap between the contacts exist is going to be

smaller than the radius of the circle on the rotor. This means that a hole can be cut in the middle of the rotor without affecting the capacitance. Within the radius of this hole the height restriction is much less strict. If a set of bolts can be made to fit within this radius, the stator can be attached without impacting the minimum distance between the plates.
The PCB is a rectangle, but the desired structure of the plates is circular. This means that while the area where the capacitance is varied, a circumscribed rectangle is also present around this area. If it is removed from the stator, it can be used for the attachment points of the rotor without affecting the minimum distance. An illustration of the attachment points can be seen in Figure 4.8.

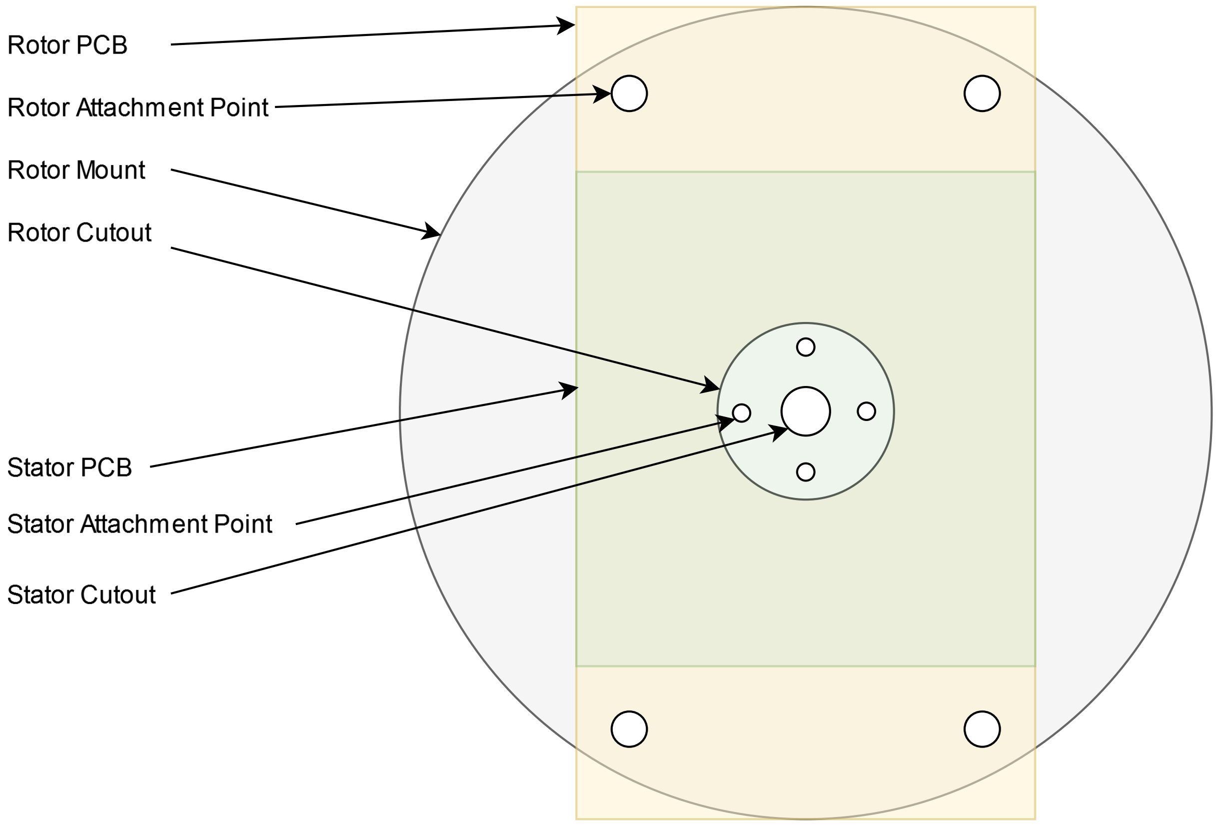


***Figure 4.8:*** How both the rotor and stator PCB are attached to the support structure.

With the full specifications of the PCBs being decided, the PCBs are created. The soldered PCB is shown in Figure 4.9. A thin line of copper is added from the plates going nearer the hole, to ease the attachment of the wires. Magnet wire is used, which is a copper wire enveloped by a thin layer of isolation. A slight variation of color is used to distinguish which 'group' each wire is in. The five holes in the center are the previously described attachment points of the stator. The rotor is made likewise, but no wires are soldered to it.

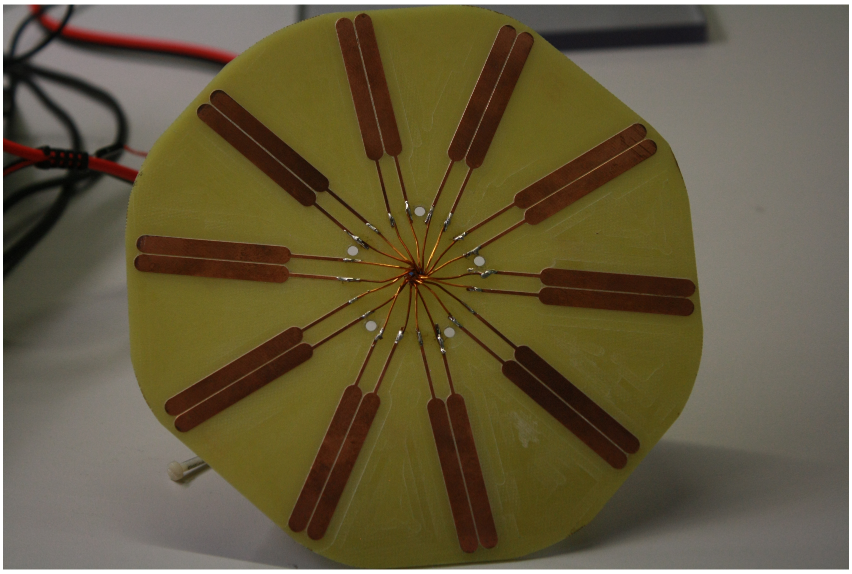

***Figure 4.9:*** The constructed stator PCB.

## 4.4 Designing the Support Structure

The PCBs have been designed, the motor has been chosen and attachment points have been specified. To finalize the design, the structure holding everything together must also be designed. The structure should hold the motor and allow for obstacle free rotation of the rotor, relative to a fixed stator. Further, the structure should allow for changing the distance between the PCBs and fixing it at some value, allowing for calibration of the capacitance values.
The orientation of the PCBs is not of great importance, as long as it remains fixed during operation. It is therefore chosen that they will be oriented perpendicular to the ground. For ease of implementation a pre-built stand with a set of rails is chosen as the basis for the design, as it will allow for the distance to be varied in one direction, while keeping it constant in all others. What needs to be designed is then mostly already defined by the requirements of the PCBs with only a few specifics needing to be chosen.

### 4.4.1 Mounting Structure

The chosen motor needs to be fixed in place even during operation, so as to reduce potential changes in distance as much as possible. As the PCBs are to be mounted vertically and the mechanism fastening the support structure to the rails is horizontal, the support structure will consist of two plates joined at a 90° angle relative to each other. The motor and PCB will be attached a distance up along the vertical plate, at least 160 mm above the rails, to ensure the rotor will not make contact with the rails. To fit the rails, and for ease of construction, it is chosen that all four plates will be 200 mm by 200 mm. The structure holding the motor and rotor will be separated from the structure holding the stator, to allow for a varying distance between them. The support structure must be able to handle vibrations caused by the motor, while moving as little as possible, along with holding pu the motor itself. Analysing, designing and testing this is a gigantic project in and of itself, so some assumptions must be made in this case. It is chosen that thick metal plates are to be used as they are much better at resisting vibrations compared to, ie. plastics [9, p.1110]. The available materials were then either 10 mm aluminium or 10 mm stainless steel. Stainless steel generally has a greater modulus of elasticity than aluminium, making it better at resisting vibrations, but it also has a higher density [10, p.817]. The higher density would increase the weight, which could make calibration of the distance between the structures significantly more difficult. Aluminium plates are therefore chosen. To further strengthen the structures resistance to vibration, meaning decreasing the deflection distance caused by vibration, a triangular structure is attached between the vertical and horizontal plate. The general structure so far is shown in Figure 4.10.

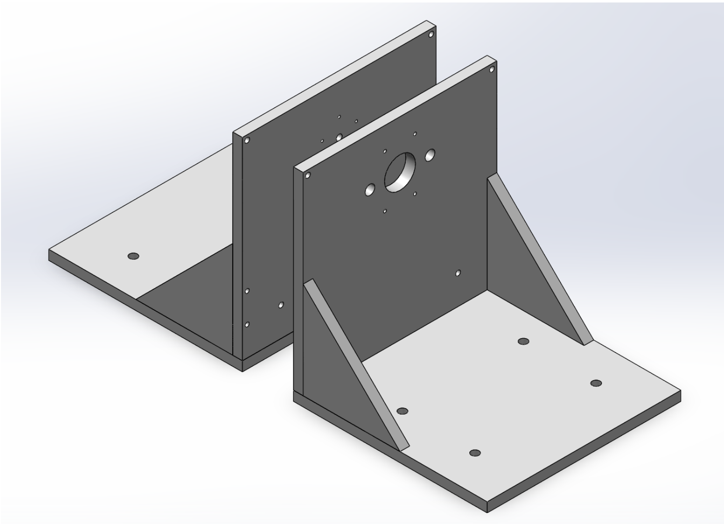

***Figure 4.10:*** A 3D CAD drawing of the support structure.

### 4.4.2 Calibration Mechanism

A set of four 8 mm holes are drilled into the horizontal plate, to allow for the fastening of bolts to the rails. This ensures that when a position is chosen for each support structure, it can fixed. Moving the two structures into position is done with an 'Organic Multifuntional Actuator', or OMA, shown in Figure 4.11. This actuator is not precise down to the necessary distances, and a calibration aid is therefore implemented. A set of four holes is drilled into the vertical plates, two at the top corners and two placed more centrally and much lower. These holes are sized and threaded to fit an M5 bolt. The bolt then acts as the calibration aid, by effectively working as an input gain. Due to the threads, one full rotation of the bolt will correspond to a specific distance traveled. This distance is often quite low, even for very large bolts. The M5 bolts chosen for this task will travel 0.8 mm for each full rotation, making it much easier to adjust very small distances [10, p.412-416]. The procedure is then, that the OMA is used to bring the two structures fairly close. The bolts are then turned until contact is made with the opposing structure. The bolts can then be slowly turned, while force is applied to the support structure, to fine tune the distance between the plates.

***Figure 4.11:*** A picture of the OMA, commonly reffered to as a 'hand'.

### Attaching the Rotor to the Motor

A mechanical coupling was provided to attach the motor axle to the rotor PCB. Coupling is made such that a set screw fastens it to the axle, and four holes at 40 mm from the axle are present such that *something*, here being the rotor PCB, can be attached. This is, however, not far enough from the center, as the attachment points on the rotor are placed 85 mm from the center. A coupling between the mechanical coupling and rotor PCB is therefore designed. It is chosen to be made from 10 mm thick plexiglass. Plexiglass was chosen, as it is a lightweight, non-conductive material. This adds only a small amount to the weight of the whole structure, while also helps to electrically isolate the rotor PCB and motor.

## 4.5 The Delta-Capacitor

With everything designed, the only thing remaining is to put the variable capacitor together. As the stated function of the device is to dynamically change the capacitance, and use this change in the system, the device is dubbed the Delta-Capacitor. It will be referred to as either the device, the variable capacitor or the delta-capacitor from now on. The construction of the sub-components, along with the assembly of the device, is done by the workshop at AAU Energy. A picture of the variable capacitor is shown in Figure 4.12. In the picture the stator can be seen attached to one part of the support structure with nylon screws. The motor and rotor attached to the other part of the support structure. A plastic guard has been put around the rotor as a safety precaution. The bolt going through the top right corner is part of the calibration mechanism described in Section 4.4.2. A picture showing the fastening mechanism is shown in Figure 4.13. The four bolts on the horizontal plate are fastened or loosened to allow for movement along the rails. The hex key inserted into the top left right is used for this. The four bolts in the vertical

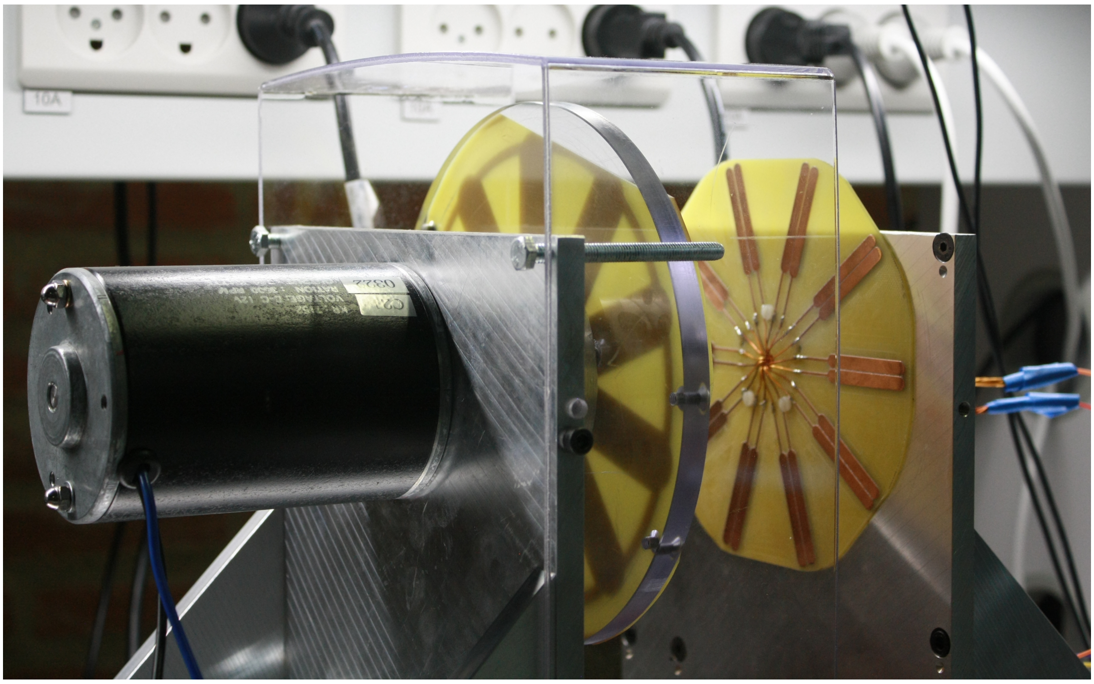

***Figure 4.12:*** A view of the assembled delta-capacitor.

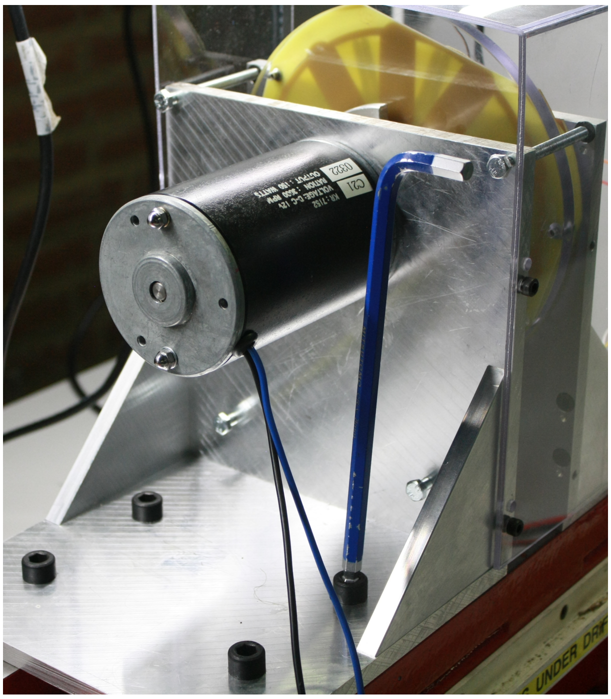

***Figure 4.13:*** A picture showing the fastening mechanism.

plate is the aforementioned calibration mechanism. A picture showing the rotor is displayed in Figure 4.14.

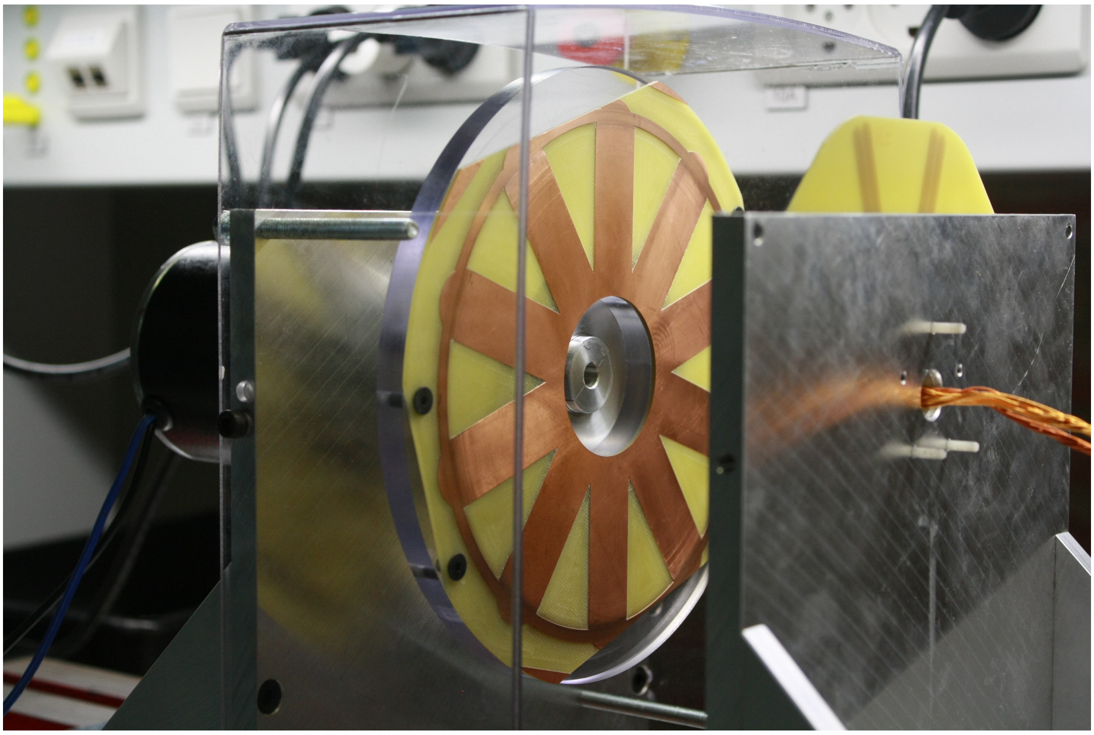

***Figure 4.14:*** A picture showing the attached rotor.

The rotor can be seen with the cutout in the middle, allowing room for the attachment of the stator. The two black bolts on the left on the rotor, along with a corresponding pair on the opposite side, attach the rotor PCB to the plexiglass plate. With the device assembled it can be tested.

**Mechanical Challenges**

During the initial testing of the delta-capacitor, a few issues were noticed. Firstly, the rotor has a slight wobble to it, which affects the minimum achievable distance between the plates somewhat. Secondly, as the structure is made mainly from metal, the structure has a tendency to warp and flex during the day. Therefore, the testing is done as quickly as possible after calibration is completed. Thirdly, the motor draws a lot of power, approximately 12 W. This can be due to several factors, including the friction internally in the motor, and air resistance. The air resistance might be a big part of this power draw, as when the two plates are put so close together, the boundary layers of the air will start to interact and affect the torque on the motor significantly. Some of this power is also used for the changing of the capacitance parameter.

# Evaluating the Delta-Capacitor 5

## 5.1 Analysis of Capacitance

In order to validate the change of capacitance in the physical device, an experiment needs to be conducted. This experiment can take many forms, but should give insight into the absolute capacitance of the system and how it changes over a cycle.
This can be done either discreetly or continuously. If the discreet approach is taken, measurements are done at specific angles for a whole cycle. These results are then compiled together, such that the capacitance profile can be constructed.
This approach requires precise control over the angle of the rotor, while simultaneously requiring having knowledge of said angle. As the motor implemented in the device is a DC-motor not equipped with an encoder, angle control is not easily achieved. The angle could be adjusted by hand, but the permanent magnets in the motor will impart a force on the rotor, which will decrease the accuracy and repeatability of the experiment. These factors make this approach infeasible, and it is therefore not chosen.
The continuous approach is forced as a result, leaving only the method of calculating the actual capacitance to be chosen.
One way of doing this is providing a voltage input consisting of white noise, and measuring the current of the system. The measured current can then be transformed to the frequency domain using the Fourier transform, which will provide the frequency response of the system; the bode plot. This method can be used to glean a very broad system response with both the capacitance and inductance of the device being theoretically calculable. The method is, however, reliant on being able to generate a relatively high current over a wide range of frequencies, such that the response is able to be measured. As the measurements are to be made continuously, more advanced techniques are also needed for transforming the signal into the frequency domain, as the frequency response now varies with time. While it is possible using the field of analysis called time-frequency analysis, the methods available introduce complications into the analysis.
Another way of extracting the necessary information is by constructing a capacitive voltage divider, and measuring the output voltage. This approach requires putting two capacitors in series, applying a voltage at a specified frequency and measuring the voltage over one of the capacitors. If the frequency of the voltage is much greater than the frequency of change of capacitance, the measurements can be performed close to continuously. Using this method, the specific frequency where the capacitance is measured can also be chosen. Furthermore, it is simple to setup, simple to measure and it is easy to modify the critical parameters of the experiment.
Due to the simple and modular nature of the capacitive voltage divider, it is chosen as the form

of the experiment.

## 5.2 Capacitance Measurement

A circuit representing the voltage divider is shown in Figure 5.1. The circuit consists of several elements, namely two impedances, an AC voltage source and a measured output voltage. The input voltage is applied by the AC-source and the measured voltage in between the two impedances is affected by the relation of these impedances. Knowing how the relation between the impedances affect the measured voltage allows for the measurement of the unknown capacitance. While a perfect capacitive voltage divider only includes capacitors, a more general voltage divider, which include resistive effects, is shown in the figure.

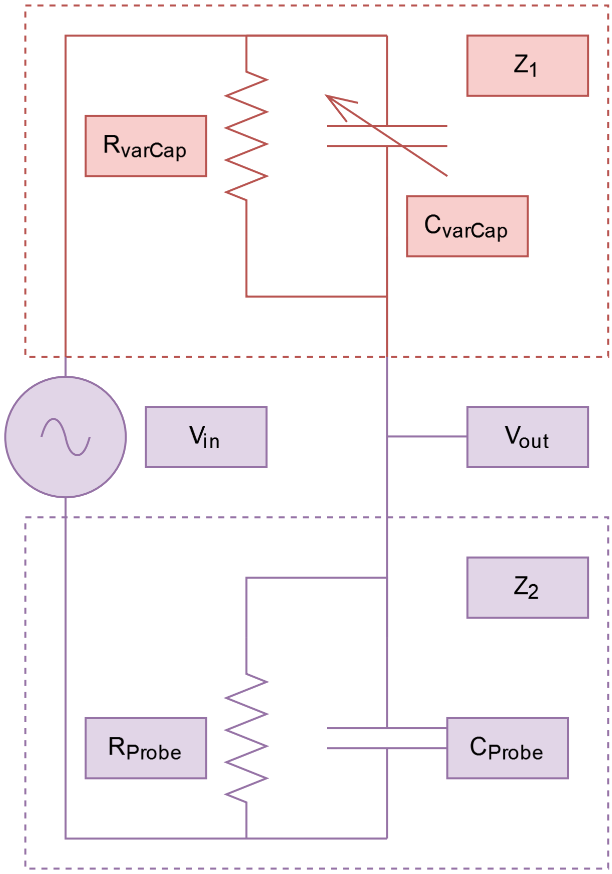


***Figure 5.1:*** A capacitive voltage divider used to measure the unknown capacitance of the delta-capacitor.

This method relies on the one capacitor having known parameters, in order for the calculation of the unknown capacitance to be accurate. The implementation of this known capacitor proved to be somewhat difficult, as the capacitance of the probe ended up being a significant part of the capacitance of the system. This would mean that the capacitance and resistance of the probe should be included in the calculation of the unknown capacitance. To reduce the complexity of calculations, it was then decided that the probe was to take the place of the known capacitor. The electrical parameters of the probe are given in Table 5.1. In the ideal voltage divider, both devices are purely capacitive, and the ratio of the voltage over each is simply equal to the ratio of the two capacitances. In the physical world, however, the resistance of the capacitors will affect this ratio, and it is therefore necessary to know these parameters. This holds true for both the known capacitor, and the unknown capacitor. Therefore, the resistance of the designed capacitor must be found.

To calculate the resistance a Keysight B2902A Precision Source/Measure Unit, or PSMU, is used. The PSMU is able to act as both a source and measurement platform, where in this specific case

| Input Capacitance | Parallel Resistance |
|---|---|
| 23.47 pF | 13.04 MΩ |

***Table 5.1:*** A table of the probe parameters.

it is used as a voltage source, while both the current and voltage at the terminals are being measured. This is done for multiple voltage levels with and multiple different rotor positions, to explore whether there exists some non-linearity or parameter change. The measurements are averaged over a period of two seconds, both to ensure that the capacitive effects have minimal impact on the current, and to reduce the impact of noise. Using Ohm's law, the resistance can be calculated from the measurements. The calculated resistance varied with voltage, is shown in Figure 5.2.

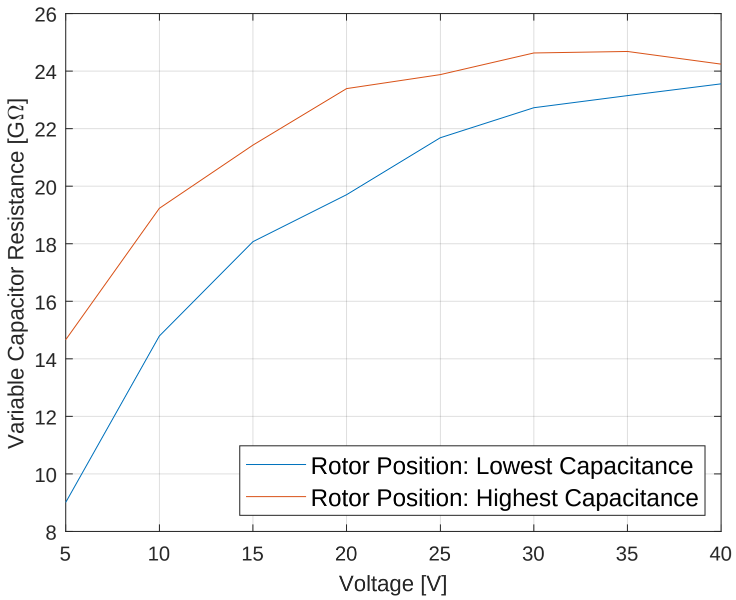


***Figure 5.2:*** Calculated resistance, as a function of voltage over the delta-capacitor, in Gigaohms. Two rotor positions are shown, one where the capacitance is expected to be at its peak, and one where it is expected to be at its lowest.

The resistance is seen to vary with the voltage over the delta-capacitor. This is likely due to some constantly present additional leakage current in the system. The highest measured current in the experiment is approximately 1.7 nA, so what would normally be a small leakage current in other systems is very visible here. With a higher voltage, the resistances does seem to converge on a value. While there is some difference in the measured values between rotor positions, it is minuscule compared to the magnitude of the measured resistances, and can therefore be neglected. The resistance value of the delta-capacitor is therefore calculated as the mean of the two resistances measured at 40 v, which is 23.9 GΩ Now, the equation for finding the unknown capacitance is constructed.
The equation derives from the general equation of a voltage divider, shown in Equation 5.1 [11, p.48].

$$\frac{V_{out}}{V_{in}} = \frac{Z_2}{Z_1 + Z_2} \tag{5.1}$$

With $V_{in}$ and $V_{out}$ being represented by a complex valued number on the polar form in the steady state: $|V|e^{j\cdot\theta}$, with $\theta$ being the phase of the waveform and $j = \sqrt{-1}$. The expressions for $Z_1$ and $Z_2$, shown in Equation 5.2 and 5.3 respectively, are inserted into Equation 5.1, and the equation is solved for the unknown capacitance. The expressions for $Z_1$ and $Z_2$ are shown in Equation

5.2 and 5.3.

$$Z_1 = \frac{1}{-j \cdot C_{varCap} \cdot \omega_{test} + \frac{1}{R_{varCap}}} \tag{5.2}$$

$$Z_1 = \frac{1}{-j \cdot C_{probe} \cdot \omega_{test} + \frac{1}{R_{probe}}} \tag{5.3}$$

Here $\omega_{test} = 2\pi \cdot f_{test}$ is the frequency of the voltage. The equation for the unknown capacitance is then given in Equation 5.4.

$$C_{varCap} = -imag\left(\left(\left(\frac{\frac{|V_{in}|}{|V_{out}|}e^{j\cdot\theta}}{-j \cdot \omega_{test} + \frac{1}{R_{probe}}} - \frac{1}{-j \cdot \omega_{test} + \frac{1}{R_{probe}}}\right)^{-1} - \frac{1}{R_{varCap}}\right)\frac{1}{j \cdot \omega_{test}}\right) \tag{5.4}$$

One of the wonderful things about this equation is the fact that as the voltage are only needed as a ratio of each other, the scaling is irrelevant. As such it does not matter whether the voltages are given in peak to peak values, rms values or other representations. Therefore, peak to peak values are used, as a new representative voltage value can be measured every half cycle of the input voltage. The *imag* operator means taking the imaginary part of the number, and is necessary due to errors in the estimation of the phase between the two signals.The input voltage is applied at 500 Hz, while the rotor is spinning slowly relative to the frequency of this voltage at approximately 550 mHz. Using the measured input and output voltage along with the known parameters the capacitance is calculated, and shown in Figure 5.3.

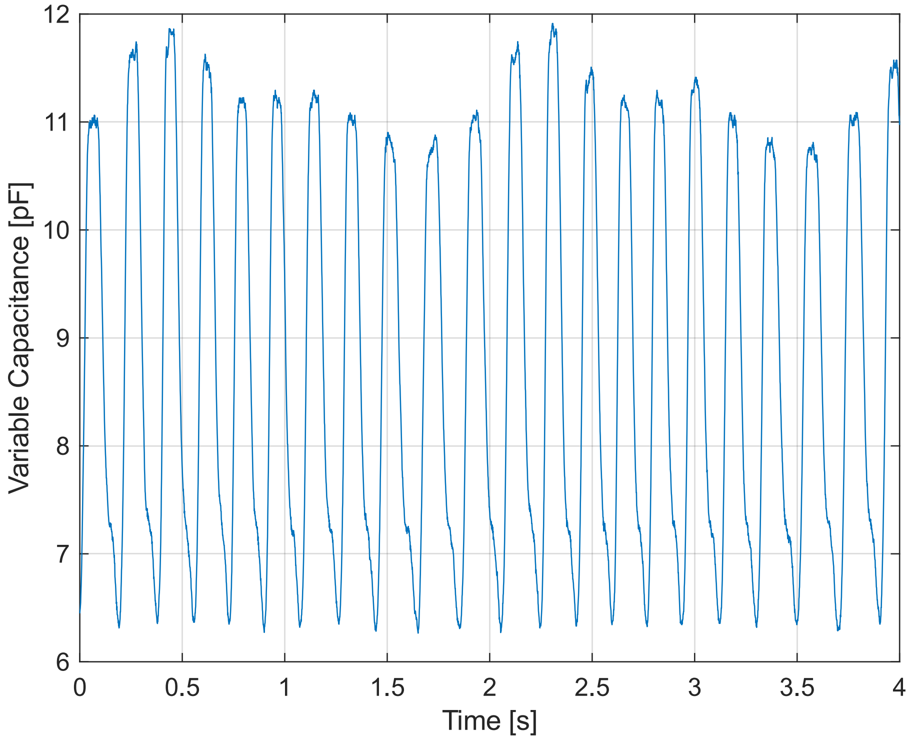


***Figure 5.3:*** Calculated capacitance of the delta-capacitor as a function of time. Several capacitance cycles are seen on the plot, with some variation in the calculated capacitance between them.

The capacitance values generally follow the expected trajectory, with deviations in multiple different time scales. First, a slow deviation can be seen on the amplitude of the capacitance, which changes from about 11.9 pF to 10.8 pF. This is accompanied by a faster deviation in each of the valleys of the capacitance curve. Here, as the capacitance falls, there seems to be a period where the rate of change of capacitance is lessened. These two phenomena are now discussed.

### 5.2.1 Fast Deviation

The occurrence of a 'bump' in the capacitance curve is unexpected. To better see the deviation, Figure 5.3 has been reconstructed with a focus on the data from 2–2.5 s. This is shown in Figure 5.4.

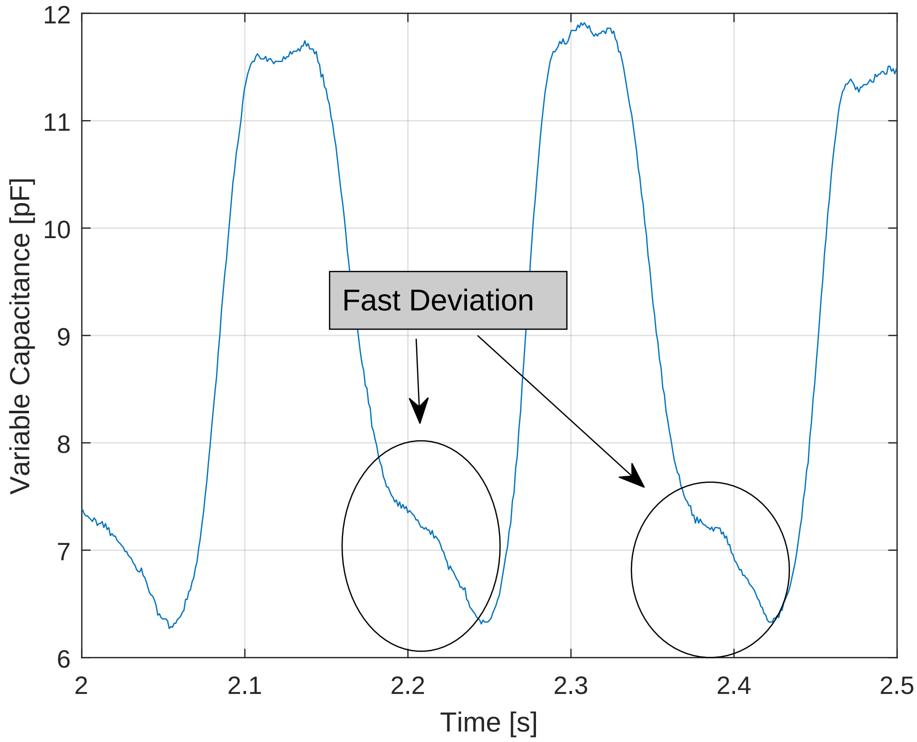


***Figure 5.4:*** Calculated capacitance of the delta-capacitor as a function of time. Only a few capacitance cycles are shown, and focus has been put on the fast deviations.

It is not unthinkable that the capacitance does not completely stop changing while the plate moves during the full overlap of the contacts, due to fringing fields. What is truly strange, however, it that this only happens when the capacitance goes from high to low, and not vice versa. The PCBs are designed to be non-chiral, and the capacitance values should therefore be symmetrical around the midpoints of rotation, ie. where the midpoint of the rotor trace is directly above the midpoint of the two stator contact traces. The presence of this asymmetry, or artifact, indicates several different things possibly occurring. It could stem from electrical noise, as it is occurring at the same frequency as the change in capacitance and not the angular frequency of the motor. The artifact could also stem from a mismatch in the rotational axis and the midpoint of one of the PCBs.

The source of the artifact can be determined by changing the rotational direction of the motor. If the source is electrical, it would retain its 'position' on the downward slope of the capacitance no matter the rotational direction. Yet, if its source is mechanical it could change position when the direction is changed. Therefore, the experiment is repeated with the rotational direction changed to ascertain the source of the artifact. Due to the friction in the motor being different for different directions of rotation, it is almost impossible to maintain the same speed in both experiments. The capacitance is therefore varied slightly faster in this experiment at approximately 775 mHz, which also serves to test if frequency of the deviation is variable. The calculated capacitance values from this experiment is shown in Figure 5.5.

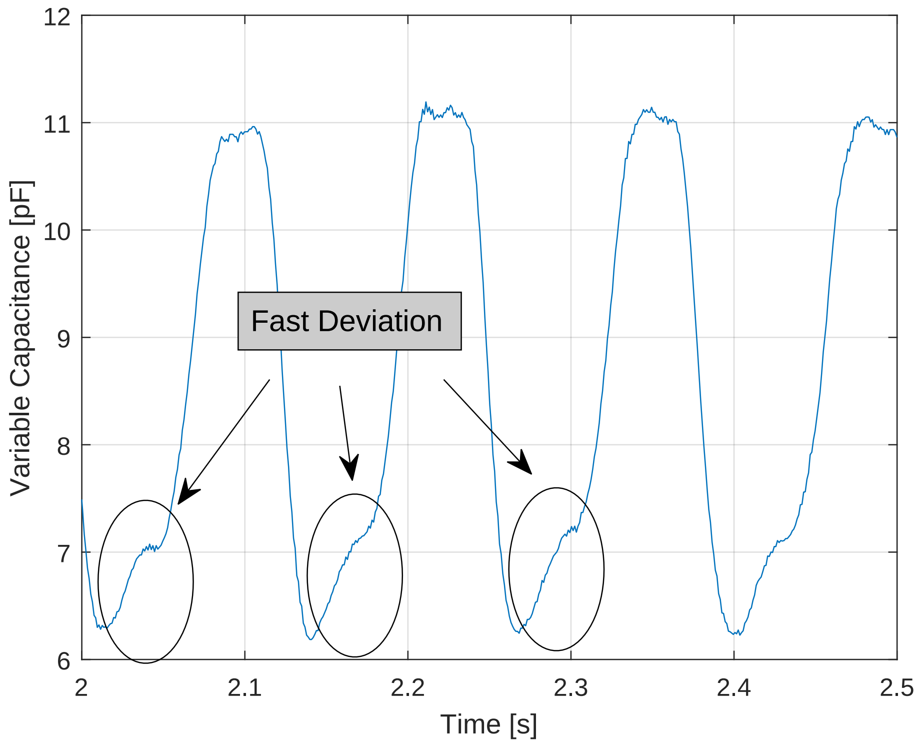


***Figure 5.5:*** Calculated capacitance of the delta-capacitor as a function of time. The rotational direction is reversed relative to the experimental capacitance shown in Figure 5.3. The fast artifacts have changed 'position', indicating a mechanical asymmetry.

Several things of note can be found from the presented plot. Firstly, the previously discussed artifact has changed 'position' in the period, meaning that the source is most likely not electrical. The fact that the frequency of the artifact changed with the changing mechanical speed indicates that it does not originate externally from the device. This leaves few options, including the previously discussed idea that one of the PCBs is not centered on the rotational axis. Even while this is an unexpected phenomenon, it will not significantly affect the functioning of the device.

### 5.2.2 Slow Deviation

Slow oscillations of the capacitance values are present in both the initial calculation of the changing capacitance and in the experiment conducted to explore the fast deviations. These deviations seem to impact the magnitude of the capacitance significantly, with the maximum capacitance in the initial experiment varying from about 11.9 pF to 10.8 pF. Furthermore, these variations also seem to have a periodicity to them. If a line is drawn between the peaks of the capacitance, as is done in Figure 5.6, a structure can be seen.

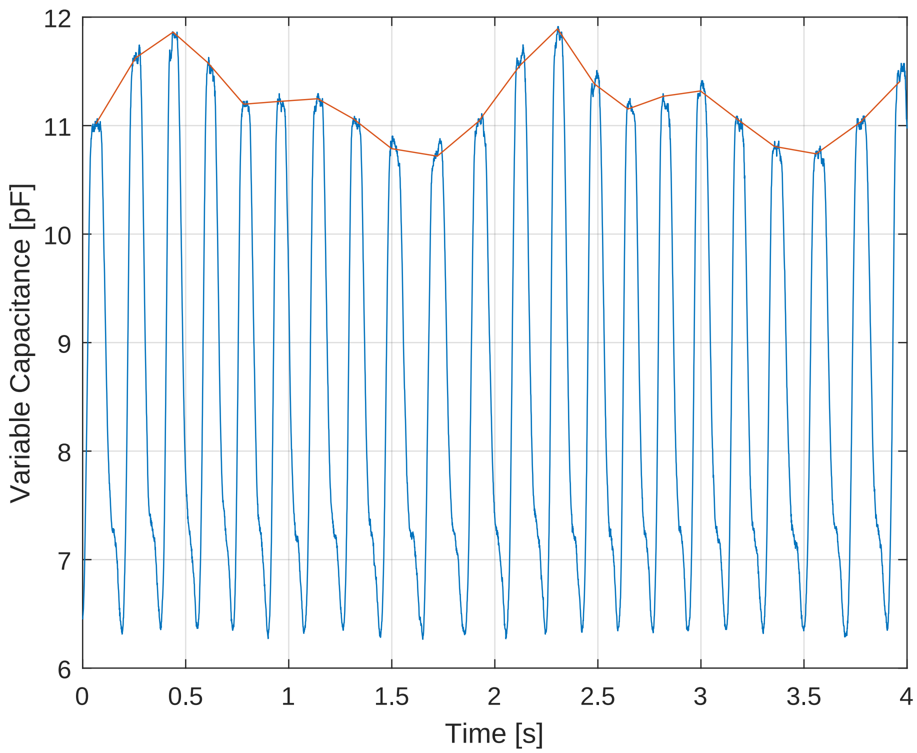


***Figure 5.6:*** Figure 5.5 recreated and augmented with a line along the peaks of the capacitance. A periodic component of the slow deviation is apparent.

The frequency of this structure seems to be low, possibly around 0.5–2 Hz, and the structure itself resembles a signal with some significant harmonic content. While a proper test can be conducted in order to correctly identify the frequency of the deviation, it is not necessary to get an idea of what is happening in the system. The signal is periodic, and changes frequency with the frequency of the motor and is much slower than the frequency of capacitance change. This all points to an asymmetry in the axle of the motor, or in the coupling between axle and rotor. If it were an externally originating disturbance, the frequency of it would most likely not be related to the system, and if it were an electrical disturbance, the frequency would match the electrical frequency. If it were an error on some part of the rotor or stator the discrete rotational symmetry would effectively 'average' it out, leading to a steadily different capacitance. The deviation must therefore be caused by something affecting the entire system at once. This could be a defect in the motor causing the axle oscillate in the direction coinciding with the rotational axis, causing the distance to vary over time.
One way to think about this, is as a common mode failure, rather than a differential mode failure. In a differential mode failure on the distance, one side of the rotor might be pushed closer by 0.1 mm, which would increase the capacitance for that part of the capacitor. But as the rotor is stiff, the other side will be drawn away by equally as much, leading to a decrease in capacitance for that part of the rotor. But this action is paired, and so would happen equally for every period of the capacitance. If, however, the distance of all the traces are changed simultaneously, the failure is now common mode. Here, the capacitance for every part of the rotor will change compared to the previous configuration leading to an overall different capacitance. If this is then due to a structural failure related to the axle, it would make sense for it to be happening at the

frequency of rotation, or a harmonic thereof. The electrical frequency will always be 10 times higher than the rotational frequency due to the design of the PCBs. If the amount of peaks of capacitance between the two peaks of the slowly varying signal is counted, it comes out to 11 over a period of 1.87 s. The frequency of the slow deviation is then calculated to be 588 mHz which is very close to the frequency of the motor. Considering the uncertainty coupled with the frequency measurement method, it can be concluded that the frequency of the slow deviation is likely the same as the mechanical frequency of the motor.

### 5.2.3 Non-ideal Voltage Divider

On the journey to exploring the deviations, an experiment was conducted where the voltage measurements were taken when the device was driven at a higher speed. The idea was to show that the frequency of the deviations were correlated with the frequency of rotation. This, however, did not go to plan, as the calculated capacitances were consistently lower than in previous experiments. The calculated capacitances are shown in Figure 5.7.

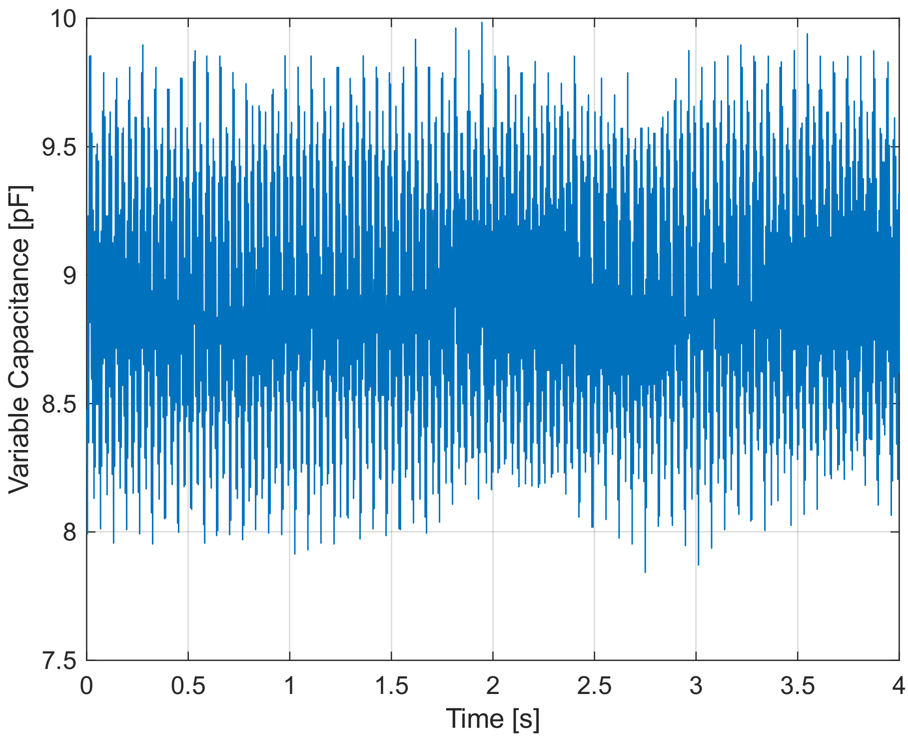


***Figure 5.7:*** Capacitance measurement done at a higher rotor speed.

As the only thing changed was the speed of the rotor, this must be related to the source of the problem. One thing which does change with the changing rotor speed is the speed of change of the capacitance.

As shown in Equation 2.4, recreated here in Equation 5.5, the current through the capacitor is not only dependent on the capacitance as usual, but also on the change of capacitance.

$$\dot{Q} = C\dot{V} + V\dot{C} \tag{5.5}$$

This current will then have to be considered when deriving the model of the voltage divider. This is done in Equation 5.6.

$$V_{out} = \left( \frac{V_{in}}{Z_1 + Z_2} + (V_{in} - V_{out}) \cdot \dot{C}_{VarCap} \right) \cdot Z_2 \tag{5.6}$$

If the current is then to be affected, the $(V_{in} - V_{out}) \cdot \dot{C}_{VarCap}$ term will have to be of a comparable magnitude to the current in the circuit as a result of the voltage divider.
A very rough calculation can be done using a worst case assumption of the current generated due to the changing capacitance. If the capacitance in Figure 5.4 is assumed to be close to correctly measured, the average $\frac{d}{dt}C$ during the fall from 11.8 pF to 7.47 pF can be used for calculations, calculated to be $-95.21\,\frac{\text{pF}}{\text{s}}$. The absolute worst case scenario is this value multiplied by the highest voltage in over the capacitor, here exaggerated to be 10 V. The minimal current as a consequence of the voltage divider can be calculated to be $27.74 - 199.7 \cdot j$ nA, and the maximal current as a consequence of the changing capacitance is calculated to be 0.952 nA. While a direct comparison between these two numbers is not possible, it is clear that at these rotor speeds, the current as a result of a changing capacitance is relatively low. It is, however, not so low that spinning the rotor maybe 50 times faster would not be detectable. It is therefore concluded that this effect is due to the increased rate of change of capacitance. It can also be concluded that at the speeds of the previous experiments, the capacitance should be only minimally affected by this.

### 5.2.4 Fulfilling Operating Requirements

While the deviations are not inconsequential, they are inherent to the construction of the specific device, and can therefore not be mitigated. This changes the expected functioning of the device slightly, but the data predicts a lowest CCR of 1.141 with a load of capacitance of 26 pF. This means that the bias voltage required to reach the threshold voltage of 1.7 V is 12.1 V. The device should therefore be able to function as expected.

## 5.3 Experimental Circuit: 33 pF Load

To experimentally verify the working of the device in conjunction with an external load, the circuit shown in Figure 5.8 in is set up. This experiment is set up on a solderless breadboard, as was done in the experiment on the IVaCaT described in Section 2.1.2. The reason for this is that there are still unknowns in the choice of components, circuit layout and possibly beyond. In these situations it is therefore prudent to use a flexible design for the experiments, as it will limit the time spent redesigning and bugfixing PCBs. While using a solderless breadboard will introduce parasitic elements, these can be mitigated by proper arrangement of the components. Measuring the leakage resistance of the breadboard it is 15.5 GΩ. The capacitance measured between two twisted wires connected to adjacent terminals on the breadboard is at 7.5 pF. This is quite high, but if the wires are placed further from each other, the capacitance quickly drops to 0.38 pF, which is more acceptable. Therefore, when constructing the circuits, care is taken to arrange the components to lower the capacitive coupling.

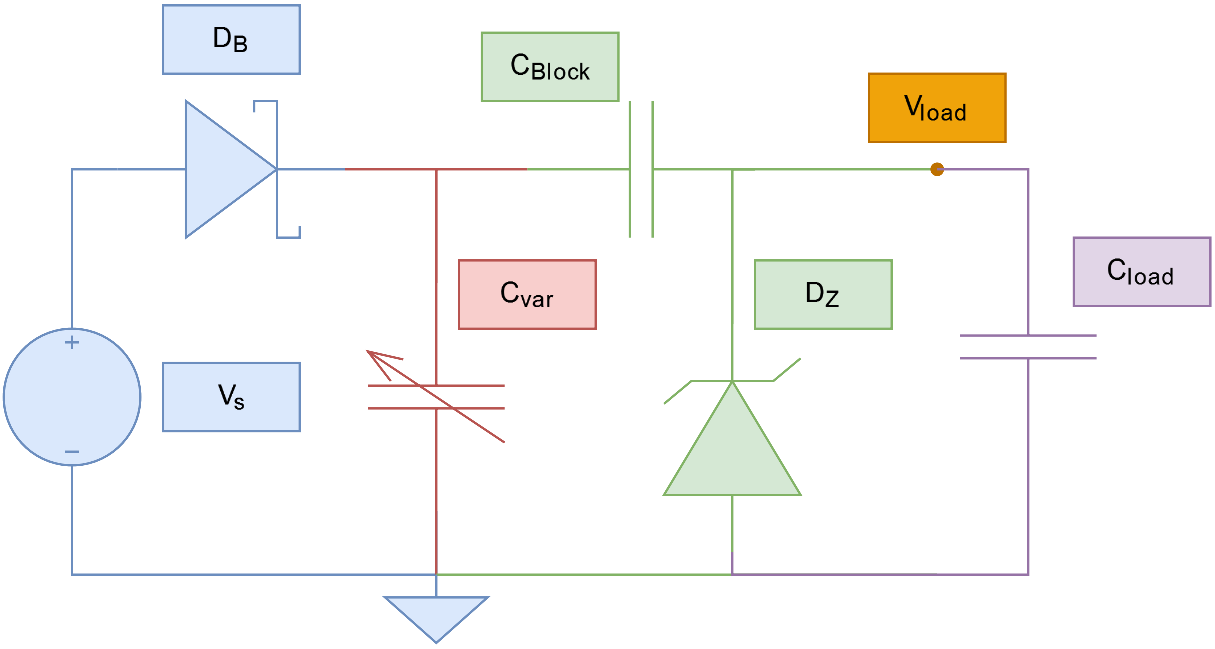


***Figure 5.8:*** The initial circuit used for simulation and experimentation. The point labeled $V_{load}$ show where the voltage is measured.

The experiment is used to test several things, which are listed here:

1. Does the measured load voltage correspond with the predicted voltage?
2. Does the zener diode affect the performance of the device?
3. Is there any unexpected behaviour of the voltage?

First, a load is selected as a 33 pF ceramic capacitor. This is selected because it mimics the capacitance of the chosen GaNFET closely. The biasing voltage over the delta-capacitor is chosen as 63 V. This results in an expected maximum CCR of 1.115 which would correspond to a voltage increase of 7.30 V. This is, however, unverifiable as the mere act of measuring the voltage introduces a parallel capacitance, which lowers the CCR. The actual expected CCR is then 1.0726, leading to a voltage increase of 4.58 V.

### 5.3.1 Experiments With Zener Diode

With the zener diode implemented in the system, the voltage waveform is then expected to go from a negative voltage equal to the forward voltage of the diode, up to half the calculated voltage increase, ie. from 0.7–2.3 V. Due to the specific nature of the capacitance variation, which was explored extensively in Section 5.1, the voltage is also not expected to vary equally every cycle. Instead, it is expected that the voltage peak will vary in amplitude over several capacitance cycles. The blocking capacitor is the same 100 nF capacitor used in the experiment on the IVaCaT. A section of the experimental data is plotted in Figure 5.9.

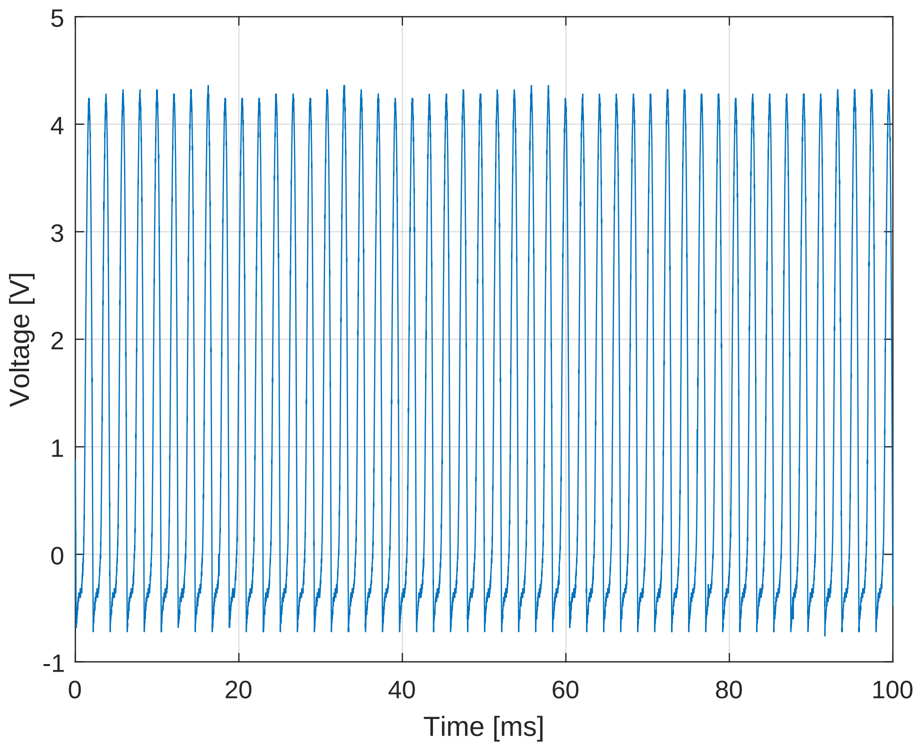


***Figure 5.9:*** The measured voltage over the 33 pF load capacitor with a zener diode implemented. The peak voltage is seen to vary as expected, but the measured amplitude is higher than expected.

The voltage peaks are seen to vary between 4.28 V and 4.36 V. This is significantly higher than the predicted voltage of 2.3 V, which is a surprise, but a welcome one. To gain more insight into the dynamics of the voltage, a smaller section of time is shown in Figure 5.10.

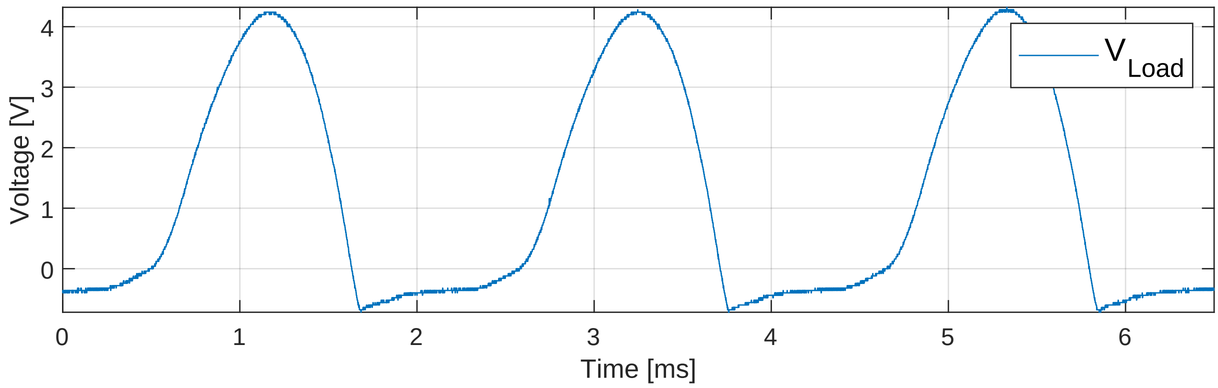


***Figure 5.10:*** The same data as in Figure5.9, bu a smaller section of time is graphed.

The discrepancy between the measured and predicted voltage can arise from several different factors. The capacitance measured in Section 5.1 could be off, which could be a consequence of noisy measurements, or that the speed of the rotor has a bigger than expected impact on the capacitance measurement. The rotor could also be charged, somehow. The rotor being charged would mean that the voltage applied over each of the two 'sub-capacitors' making up the delta-capacitor is different from expected. This can affect the output voltage significantly. In order

to ensure that the rotor is not charged, it is shorted to ground for small amount of time before all tests, however, so this explanation is unlikely. Another explanation is that the prediction method used is inherently faulty. Using the CCR relies on the charges being equal in the system before and after the capacitance change, but this is not necessarily true.
One idea, which can explain this added voltage is related to the presence of the zener diode. This diode 'disturbs' the function of the DC-blocking capacitor, by limiting the load voltage to its forward voltage. When voltage then rises again, due to the capacitance change, the voltage will rise by 4.58 V, no matter the voltage of the load. As the load voltage was limited to approximately zero, it will then rise to approximately 4.58 V, rather than the expected 2.3 V. This is concluded to be the most likely reason for the discrepancy.
To gain more insight into the system, more experiments are conducted.

### 5.3.2 Experiment Without Zener Diode

In the following experiment the zener diode has been removed from the previously described setup. This is done in order to test the scope of the impact the zener diode has on the system. The peak to peak voltage is expected to be of a somewhat greater magnitude, as the zener diode will have introduced an amount of capacitance. The voltage is also not limited to −0.7 V, and the voltage waveform is expected to be more symmetric around 0 V. The previously discussed effect of the zener diode should, however, now be lessened, and the peak voltage is expected to be lower. The experimental waveform is plotted in Figure 5.11.

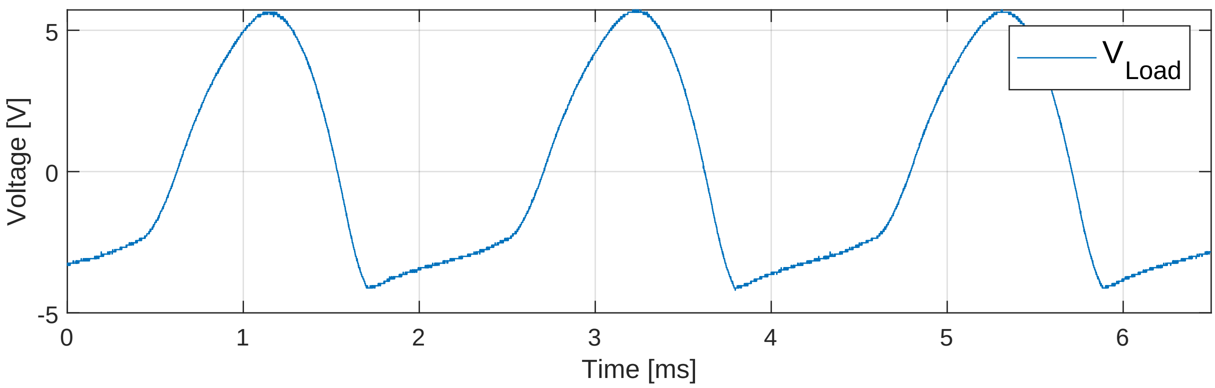


***Figure 5.11:*** The measured voltage over the 33 pF load capacitor with no zener diode implemented. The peak voltage is seen to vary as expected, but the measured amplitude is higher than expected.

The anticipated increase in the amplitude did occur, but to a much greater extent than anticipated. The minimum voltage did move further away from zero, as predicted, but the negative amplitude does not match the positive amplitude. This can be explained by the presence of the diode between the voltage source and the delta.capacitor. As the voltage goes down, charges lost to leakage currents will inevitably have lowered the voltage over the delta-capacitor, and if this voltage is lower than the forward voltage of the schottky diode and the voltage source, the diode will begin conducting.

From these experiments, several observations can be made. First, the presence of the zener diode has an impact on the voltage output of the device, in several ways. One way is by limiting the negative voltage, causing an increase in the output voltage. The other is by changing the amplitude of the voltage peaks implying that the capacitance of the zener diode is significant enough to be detectable. It is, however, not significant enough to substantially impair the functioning of the circuit.
Second, the measured voltage does not correspond to the predicted voltage. This implies that either the capacitance is measured incorrectly, the voltage is measured incorrectly or that the prediction method is insufficient. This could also mean that there are other phenomena at play, which affect the measured voltage, like the one introduced by the zener diode. Thirdly, the voltage in the system does change, both periodically and at a sufficient level to turn on the GaNFET.

## 5.4 Experimental Circuit: GaNFET Load

With the previous circuit tested, and deemed functional, it is modified such that it incorporates the GaNFET and a power loop. The following experiments seek to determine if the delta-capacitor can be used to turn on the GaNFET. In this circuit, there are ways of verifying the functionality of the circuit without measuring directly on the capacitive load. This can be used to identify whether the act of measuring the output voltage has an impact on the self-same voltage. The experimental circuit is shown in Figure 5.12. The things which are investigated

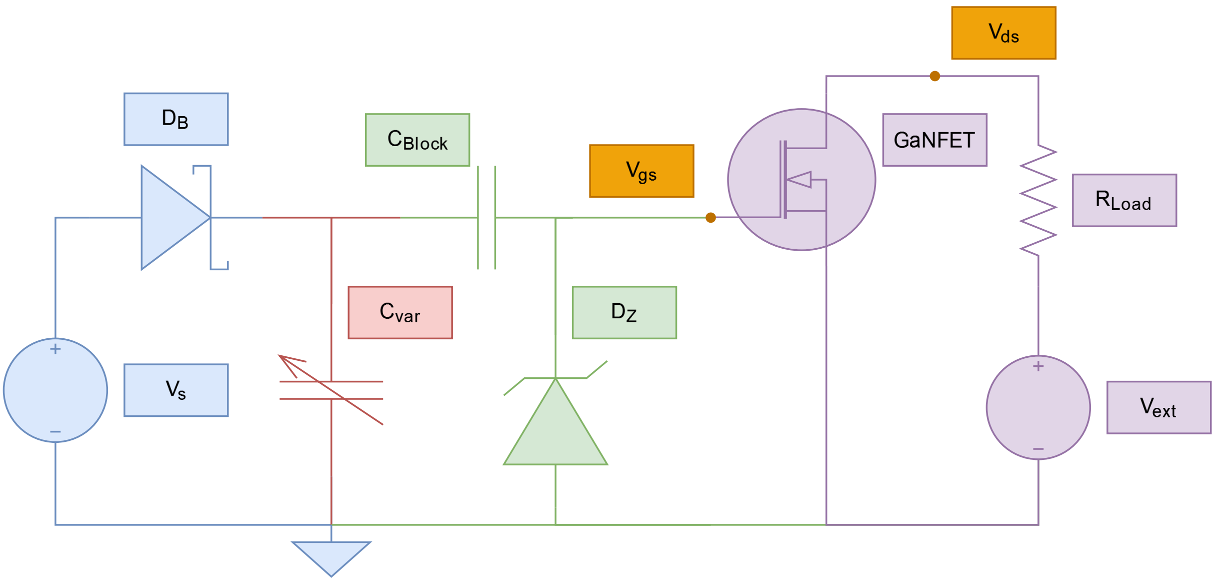


***Figure 5.12:*** The circuit used for experimentation. The points labeled $V_{gs}$ and $V_{ds}$ show where the voltages can be measured.

through the experiments are listed below:

1. Can the designed variable capacitor and circuit be used to drive the gate of the GaNFET?
2. Does measuring the output voltage of the variable capacitor affect the output voltage?

For these experiments, a 100 nF DC-blocking capacitor is implemented, and the load of the power loop is chosen to be a 100 Ω resistor.

### 5.4.1 Experiment Without Zener Diode

The first experiment, is done without the zener diode implemented. It is expected that the gate voltage will peak at a value comparable to the experiments on the 33 pF capacitive load, ie. approximately 5.8 V. This would mean that the GaNFET turns on, which is therefore expected. The experimental waveforms are shown in Figure 5.13.

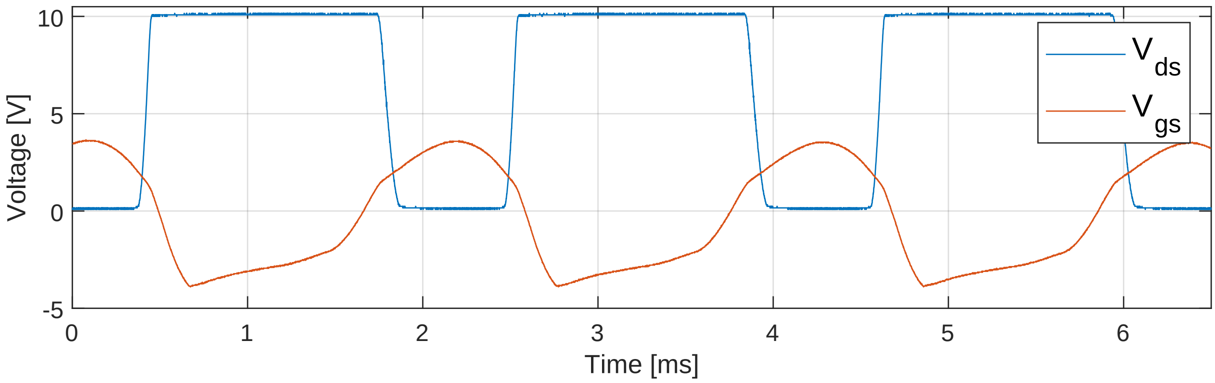


***Figure 5.13:*** The measured voltages over the GaNFET with no zener diode implemented.

Several things can be noted from the presented graph. Most pleasingly, the drain-source voltage indicates that the GaNFET successfully turns on and off periodically. This is a major success, as it proves that the idea of using a variable capacitor as a periodic gate driver is possible.
The switching waveform looks generally as it does in the preceding experiments. The amplitude is, however, decreased compared to the experiment presented in Figure 5.11. This is odd, as the input capacitance of the GaNFET, which goes from approximately 26–30 pF, is comparable to the load in the previous experiment, being 33 pF. This again indicates that there are unmodeled phenomena in the system.
While the technical details of the switching is not the focus, they are presented here in order to evaluate the specifically designed variable capacitors performance as a gate driver. The rise time of $V_{ds}$ is defined as the time from 10% of the high steady state value, compared to the low steady state value, to reaching 90% of the high steady state value. In this case, the rise time is 52.8 µs, going from 1–9 V. This is incredibly slow. It should be kept in mind that the GaNFET was not chosen for its attributes as a high speed switching device, but rather because it has a low input capacitance. Even then, this rise time will lead to the switching losses quickly rising to unmanageable levels, if implemented in a system with any significant load current.
The rise time of $V_{gs}$ is defined slightly differently than for $V_{ds}$, due to the lack of well defined on and off voltages. The rise time is therefore defined to go from 0 V to 90% of the maximal voltage. The rise time for $V_{gs}$ is then 395 µs, which is much slower than the rise time for $V_{ds}$. This is hampered by the fact that the gate voltage never truly reaches a steady state voltage, reaching a maximum value of 3.7 V. This can have an effect on the conduction losses, as they

are proportional to the gate voltage. While this is not a problem with the currents in this specific experiment, it does not inspire confidence in the ability for the delta-capacitor to function properly as a gate driver.

### 5.4.2 Experiment With Zener Diode

In order to examine the effect of having a zener diode in the system, the experiment is conducted with it implemented. Just as in the experiments in Section 5.3, the zener diode is expected to increase the capacitive load, thereby decreasing the amplitude of the gate voltage. It is also expected that the voltage will not go lower than the forward voltage drop of the zener diode. The experimental waveforms are graphed in Figure 5.14.

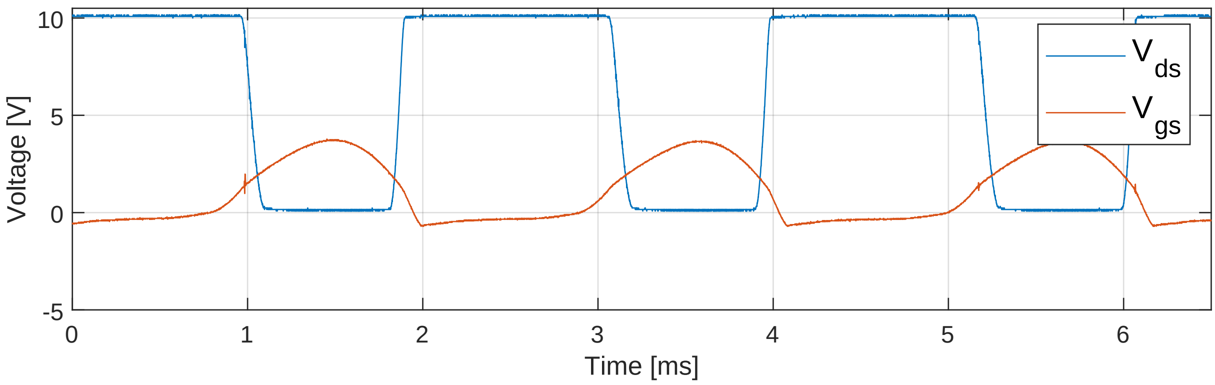


***Figure 5.14:*** The measured voltages over the GaNFET with the zener diode implemented.

While the GaNFET still turns on, the system is, as always, full of surprises. The rise time for $V_{ds}$ remains unchanged at 52.8 µs and the rise time for $V_{gs}$ is increased to 518 µs. While the increase in rise time for the gate voltage is expected, an accompanying increase was also expected in the rise time of $V_{ds}$. The fact that there is a difference in change here, indicates that the system dynamics related to the miller plateau is less affected by a change in the DC-capacitance. Another surprise, is the fact that the maximum measured gate voltage has *increased* to 3.94 V. The experiments conducted in Section 5.3 indicate that the prediction methods are not capable of predicting a correct voltage, or that the measured variable capacitance is incorrect, but that the general predictions about the system dynamics hold. This means that if the DC-capacitance is increased, the voltage variation is expected to decrease, which does not happen here. This can be modified, if the amount of charges in the system is not constant, which is likely what happened here. As the gate voltage slips below the forward voltage of the zener diode, will start conducting, leading to a flow of charges from ground into the system. While this might seem a satisfactory explanation, it does not clarify why the voltage amplitude drops when the zener diode is implemented in the experiments with the 33 pF load. The reason for this increase in voltage is therefore still unknown.

The eagle eyed viewer will have spotted the last surprise offered up by this experiment. To make it clear, a zoomed in view of a turn on transient is presented in Figure 5.15.

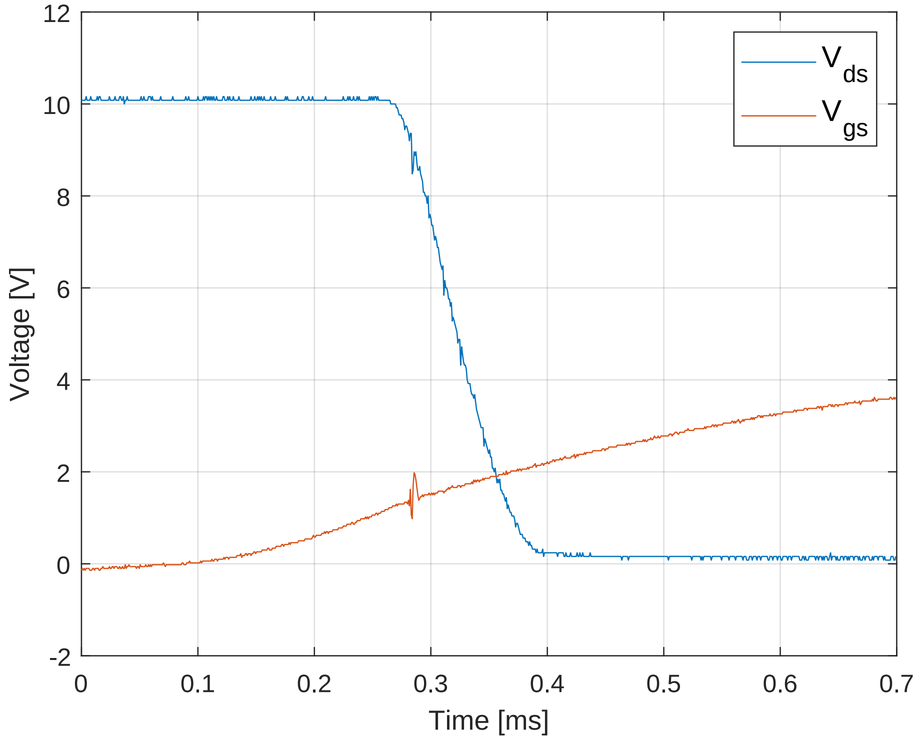


***Figure 5.15:*** A zoomed in view of the measured voltages over the GaNFET with no zener diode implemented. A small region of high frequency noise can be observed.

The graph shows that during the turn on transient, there is a small period of time where some high frequency noise can be detected. This noise affects both $V_{gs}$ and $V_{ds}$ and can be spotted on many, but not all, of the turn on transients and sometimes also on the turn off transients. It is never present outside of these transients, which indicates that this is not an externally generated noise, but rather an effect which originates in the system. As it happens during the switching transients it could very well be caused by the miller plateau. For now, the existence of these artifacts is simply noted, as they do not seem to significantly affect the circuit.

### 5.4.3 Experiments Without Measuring Gate Voltage

Finally, an experiment is conducted where the only measured voltage is the drain-source voltage. This is done to see the extent of the impact of the probe. To protect the gate of the GaNFET, the zener is re-implemented in the system. The experimental waveform is shown in Figure 5.16.

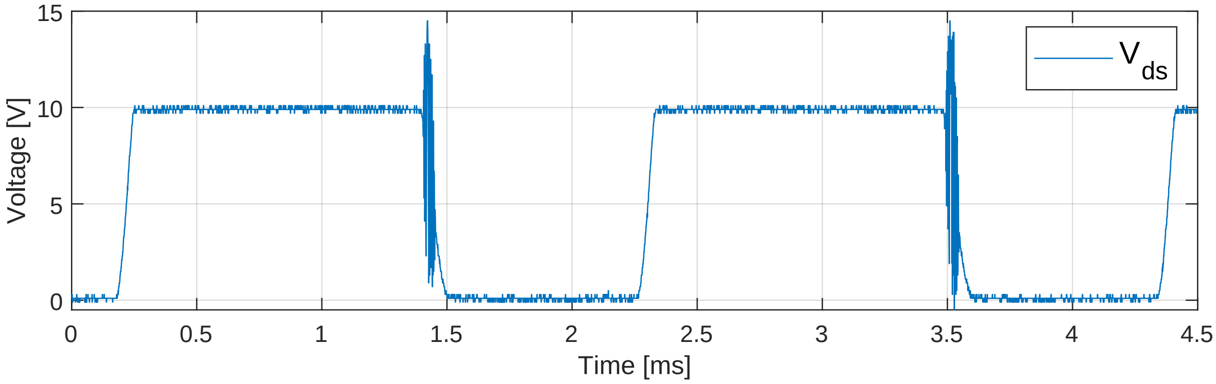


***Figure 5.16:*** The experimental waveform of $V_{ds}$ for the system without measuring $V_{gs}$. Periods of high frequency noise is seen during the turn on transients.

The graph shows that the noise seen in the previous experiment is back, but at a much higher intensity. Focusing on the goal of the experiment, which was to determine the impact of probing the gate voltage, the rise time can be determined to be 48.8 µs, which is faster. This is the expected outcome, as removing the probe will also remove the additional capacitance introduced by the probe.

While not much more can be gleaned from this line of investigation, another door of discovery has swung wide open. A zoomed in view of the noise is shown in Figure 5.17. Here, the perpetrator

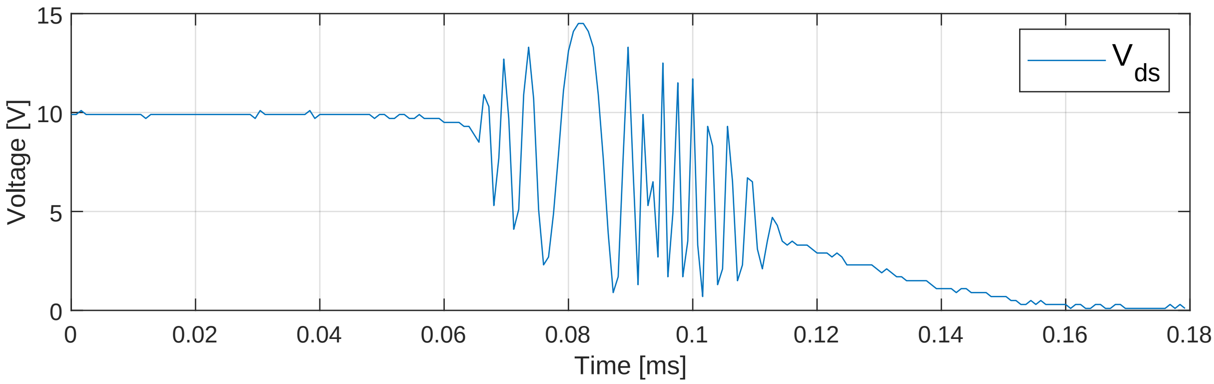


***Figure 5.17:*** A zoomed in view of the periods of high frequency noise is seen during the turn on transients.

of the noise reveals itself as an instability in the system. The voltage peaks can be seen to follow the characteristic exponential increase, before the system stabilises and settles down once more. Fascinatingly, the frequency of the instability seems to change, starting at a high value, then lowering until the system becomes stable again, and then increasing before settling fully. Such instabilities are not unheard of, but mostly occur in circuits with parallel configured FETs [12]. The reason for the change in frequency of the instability is likely due to the parameters of the GaNFET changing during a switching transient.

This is an incredibly interesting phenomenon which additionally serves to strengthen notion that the delta-capacitor does not serve well as a gate driver. While it does function to turn on the GaNFET, the gate voltage never reaches a steady value. The rise times for the drain-source voltage is also slow, which will introduce a large amount of switching losses. While these are problems which might be fixed in various ways, the question remains: Is driving the gate of a FET the proper application for a periodically varying capacitor?

# Iteration and Exploration 6

As the experiments conducted in the previous chapter indicate that the delta-capacitor is not suited for use as a gate driver, an attempt is made to improve the design. In this chapter then, different iterations on the design of the delta-capacitor are investigated, along with the presentation of some curious findings.

## 6.1 Iteration of Delta-Capacitor

While the designed capacitor functions well enough to turn on the GaNFET, iterating on the device can provide valuable insight into the design process.

### 6.1.1 Increasing the Resistance

As shown in Section 2.1.3 keeping the leakage current in the circuit low is crucial. As was briefly discussed in Section 4.3.2, the gap between the stator plates was chosen small even though this could decrease the leakage resistance and increase the DC-capacitance. This was done to increase the area available for creating an overlap, which should lead to an increase in the change of capacitance. If a line is cut in between the plates, it should increase the leakage resistance dramatically, decrease the DC-capacitance and decrease the capacitance variation. This is therefore tested by cutting a away the material of the PCB, and measuring the parameters of the variable capacitor once more. Figure 6.1 shows a picture of the new stator. Initially, the

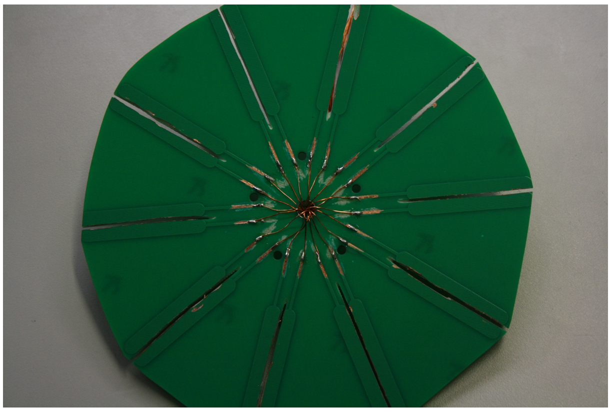

***Figure 6.1:*** A picture of the new stator. The stator is modified by cutting away the material between the stator plates.

resistance is measured and compared to the resistance of the old stator. This is done in the same manner as for the resistance measurement for the old stator, and the results are shown in Figure 6.2. The same trend can be seen for both resistances, so the resistance is again assumed

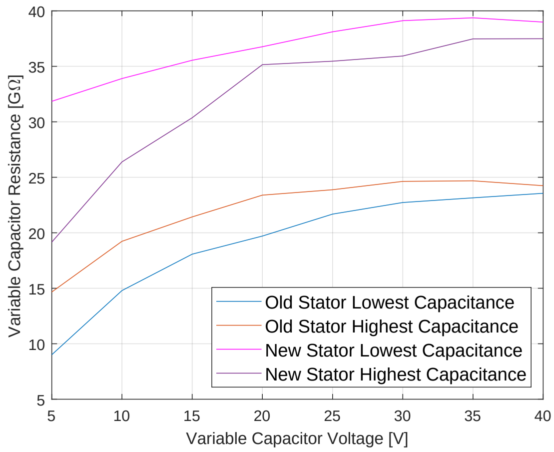


***Figure 6.2:*** The a comparison of the leakage resistance of the two stators.

to be an average of the final two values. This means that the new stator has a leakage resistance of 38.2 GΩ, compared to 23.9 GΩ for the old stator. This is an increase, but also knowing the changes to the capacitance will help to evaluate how worthwhile this increase is. A capacitance measurement is therefore conducted, just as was done for the old stator. The results are shown in Figure 6.3.

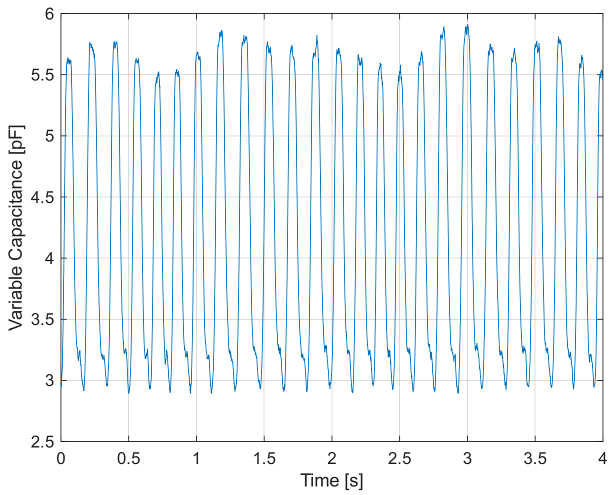


***Figure 6.3:*** The capacitance measurement for the new stator.

The new stator has its minimum capacitance approximately cut in half, from the old capacitances being at around 6.4 pF, to now being 2.9 pF. This comes along with the amount of capacitance variation also being approximately cut in half, from the old variation of 5.6 pF to the new being 3.0 pF. The relative decrease in both maximum and minimum values seem to be a coincidence. A thing to note is the persistence the fast deviations discussed in Section 5.2.1, even when changing the stator. This indicates that the error in alignment is on the rotor, or that the error is equal on two different stators by chance. Considering this, is is concluded that the error is mosty likely on the rotor.
It is difficult to predict the voltages in the system, so an experiment is conducted on the experimental circuit, with the GaNFET as a load and the zener diode implemented. The resulting

waveforms are shown in Figure 6.4.

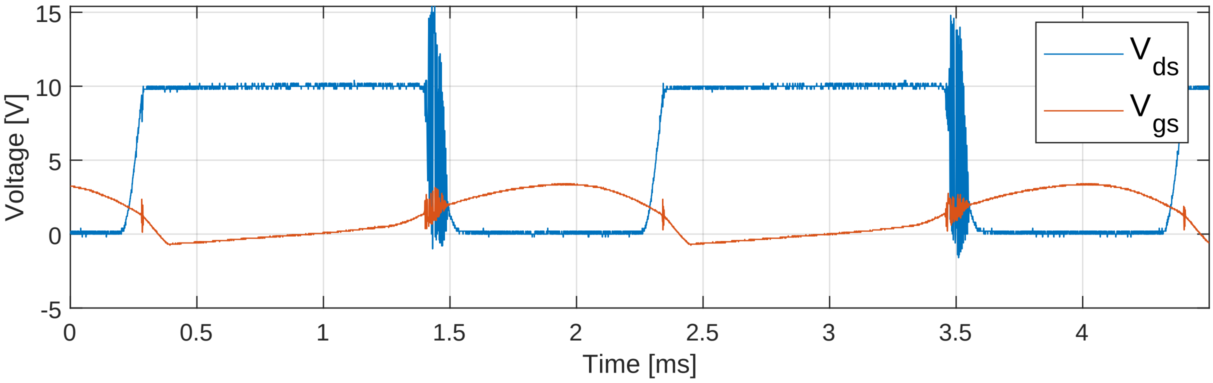


***Figure 6.4:*** The gate and drain voltages of the GaNFET with the new stator.

The instability again rears its ugly head, as it seems a now permanent fixture in the circuit. This could be due to a fault in the GaNFET brought at some stage, but its origin is unknown. What can be seen, however, is that the gate voltage is slightly lower compared to the experiment shown in Figure 5.14. The sub-zero voltages have taken on a different shape, as the voltage now no longer plateaus. Rather, it exhibits a steady rise, even above 0 V. This is strange, as the increased leakage resistance should keep the voltage at the same level for longer.
These results point to the specific implementation having an undesired effect on the system. While the increase in leakage resistance was achieved, it did not seem to have a noticeable effect on the system. The effects which were noticeable, seems to work in opposition to the increased resistance.

### 6.1.2 Increasing the Distance from Support Structure

A way to potentially decrease the DC-capacitance, is to increase the distance of the stator plates to the support structure. The support structure is made of aluminium, and is grounded to power earth for all experiments. It therefore provides a inconvenient path to ground from the plates on the stator, potentially increasing the DC-capacitance. If this distance can be increased, the DC-capacitance might be decreased. However, the material used to increase the distance can potentially increase the capacitance. If the relative permittivity is high enough, it will work against the increase in distance. The distance increase necessary for this to not happen can be calculated by assuming the area to be constant. The relative increase in capacitance can be calculated by Equation 6.1.

$$C_{rel} = \frac{\epsilon_{r2} \cdot d_{min}}{\epsilon_{r1} \cdot (d_{min} + d_{increase})} \tag{6.1}$$

As long as the ratio in Equation 6.1 is kept below 1, the DC-capacitance should decrease. Using a 10 mm sheet of plexiglass as a spacer, and assuming the PCB to be roughly 1 mm thick, the relative increase in capacitance will be 0.31. This means that the minimum capacitance should be roughly a third of what is was before, meaning a decrease from 6.4 pF to 2.0 pF. This is, however, if just the capacitance from the plate to the ground of the support structure is considered. The plates will also couple to each other, and the increase in this coupling is difficult to predict.

Therefore, what can be said with some degree of certainty is that the minimum capacitance of the system will be different.
The spacer is constructed and inserted into the system. Capacitance measurements are done to ascertain the effect of this change. The measurements are shown in Figure 6.5.

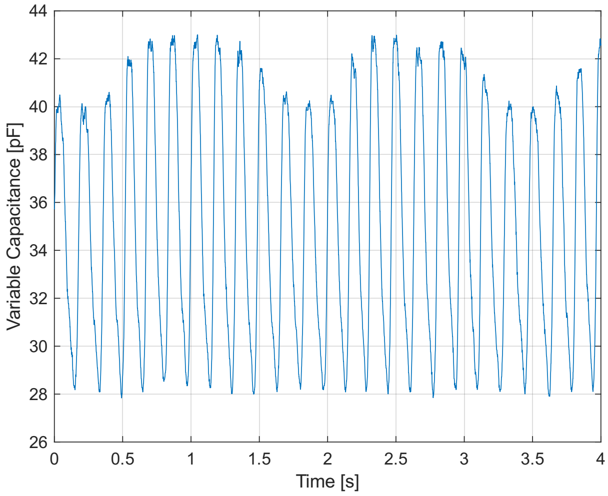


***Figure 6.5:*** The capacitance measurement of the system with the spacer included.

The prediction that the capacitance values were going to be different was correct. It is, however, very different in multiple ways. Firstly, the minimum value has increased from 6.4 pF to approximately 28 pF. This is a big increase, but the possibility of this happening was discussed. What was wholly unexpected was the fact that the capacitance increase was also affected by this change. This implies that the change in capacitance is not only reliant on the change in geometry, but also on the fixed geometry. Whatever the reason for the sudden increase in capacitance, it should change the voltage waveform. The experimental data for this is plotted in Figure 6.6.

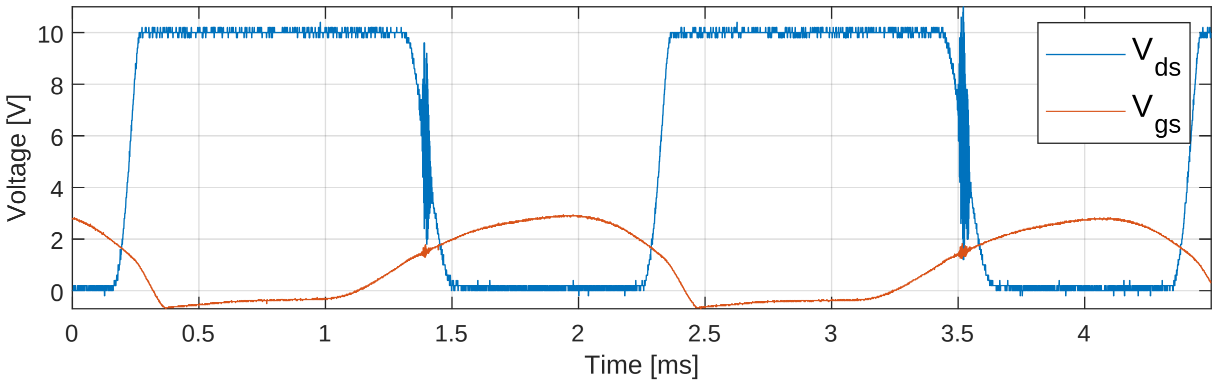


***Figure 6.6:*** Measurements of the gate and drain voltages in the system with the spacer included.

This experiment is performed with the zener diode. The instability is present, accompanied by an insubstantial increase in the voltage on the gate. This can mean one of two things. Either, the measurement technique is wrong and the measured capacitances do not accurately reflect the capacitances in the system, or the charge dynamics in the GaNFET or zener diode affect the system significantly.

## 6.2 Exploration of Weird Phenomena

While testing the delta-capacitor, several experiments were conducted which does not fit into any single category, other than 'exploration through direct experimentation'. Two of these experiments are presented here, to allow for some appreciation of how weird this device truly is.

### 6.2.1 Grounding the Stator

In Section 4.2.1 it was decided that both electrical contacts should remain stationary. While this choice directed much of the design, a copper ring was left at the outer perimeter of the rotor, to allow for a temporary connection. In this experiment, this ring is connected to ground, which should, in theory, increase the capacitance variation. This is because the electrical structure is then no longer two capacitors in series, but rather just a single capacitor. The capacitance variation is then, in the best case, doubled. Due to the previously mentioned problems with estimating the voltage amplitude, this is not done in this experiment. Rather, this experiment is simply done to see if the voltage does actually rise. The experiment is performed on the circuit seen in Figure 5.12, and the experimental data for the gate voltage is plotted in Figure 6.7.

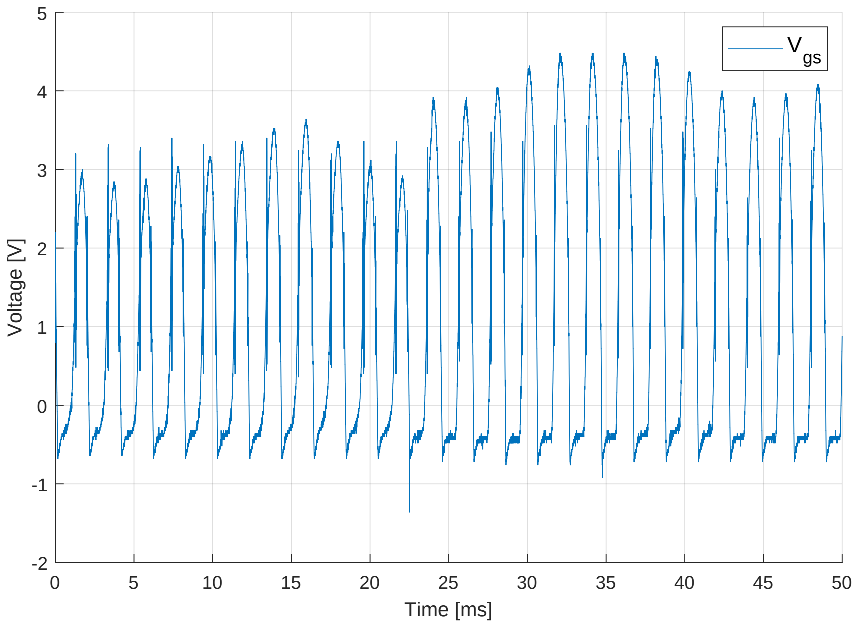


***Figure 6.7:*** Measurements of the gate voltage in the experiment. The wire is applied after approximately 22 ms, after which the amplitude of the voltage jumps approximately 1 V. The high frequency signals are caused by the ever present instability.

The experimental data clearly shows a marked increase in the gate voltage, which jumps by approximately 1 V in amplitude. What is even more remarkable can be seen with a zoomed in view presented in Figure 6.8.

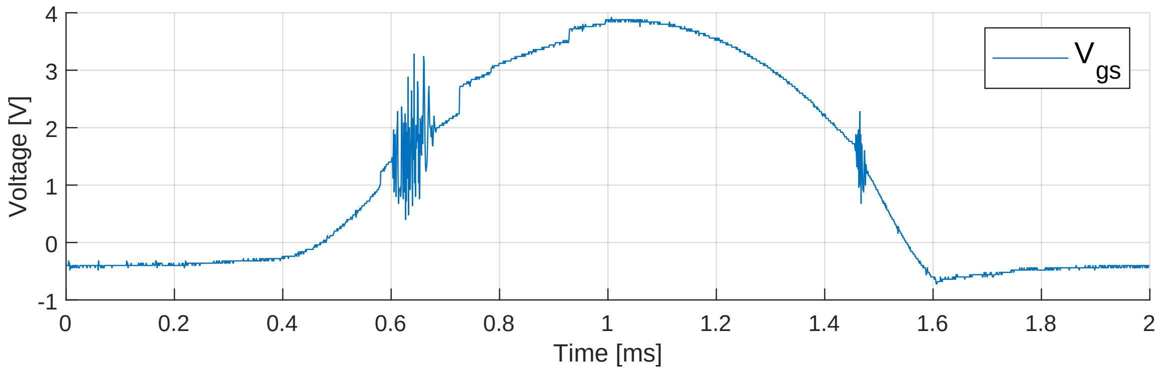


***Figure 6.8:*** A zoomed in view of the measurements of the gate voltage in the experiment. The voltage is seen to jump near instantaneously when the wire is applied.

The voltage can be seen to jump several times in the graph. This is most likely due to the wire being applied with the OMA introduced in Section 4.4.2, which will have introduced some inaccuracy during this process. When the voltage jumps, however, it is near happens nearly instantaneously with seemingly no overshoot. This shows that a much higher frequency of capacitance change is possible. While no doubt was ever had about this being the case, it is always good to confirm such obvious ideas.

### 6.2.2 Touching the Rotor

A phenomenon which was discovered by accident is that if the plexiglass of the rotor is touched during operation, the output voltage can be changed. Furthermore, this effect seems to change depending on the where, and for how long, the rotor is touched. What is meant by touched is shown in Figure 6.9.

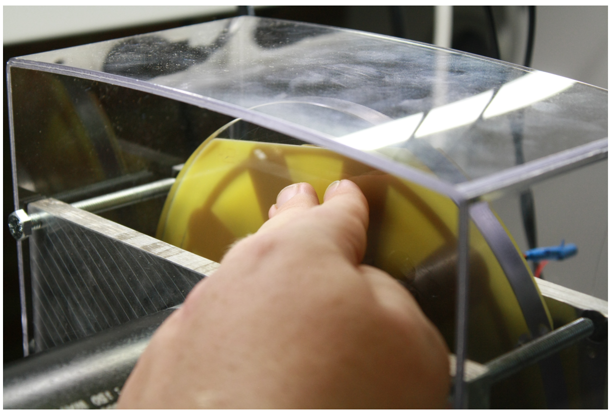

***Figure 6.9:*** Experimental procedure for the following experiment, with the OMA sub-actuator 2 and 3 being applied while the rotor is spinning. These sub-actuators are also known as 'fingers'.

The experiment is done on the circuit shown in Figure 5.12. As this experiment can produce several different, unpredictable results, several waveforms are shown. The first waveform is shown in Figure 6.10.

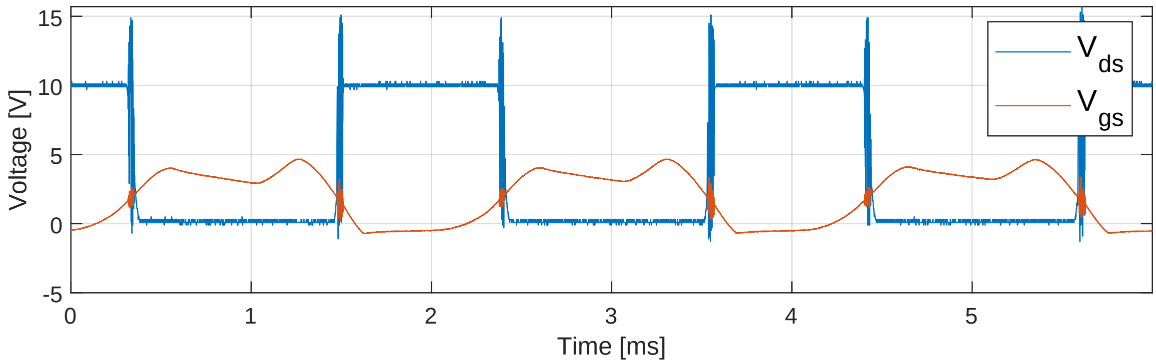


***Figure 6.10:*** Data from the experiment.

The gate voltages seem to be of a higher amplitude compared to any of the experiments done with the GaNFET as a load in Section 5.4. This implies that some charges are either being deposited on the rotor, or the OMA. After approximately 1 minute of running the system undisturbed, the voltages were once again measured. This data is shown in Figure 6.11.

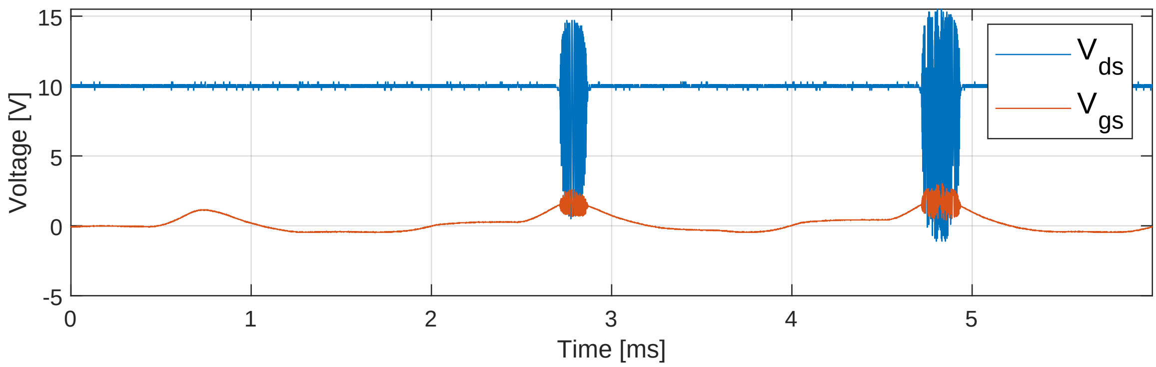


***Figure 6.11:*** Data from the experiment after approximately 1 minute had passed.

After some time has passed, the gate voltage is then lower than before, which again implies that the rotor was charged somehow. Bizzarely, the voltage is lower than for all previous experiments with the GaNFET load, even though the biasing voltage was kept constant. For this to occur, the rotor must have been charged negatively to a degree which 'overpowered' the biasing voltage applied externally. This will then invert the output voltage. If the rotor is then slowly discharged, this overpowering effect will then mean less and less, which means the signal will slowly flip back to its original state. This entails the voltages being very low at some points, which seems to have been caught here. If this is the case, it means that when applying the fingers, electrons are deposited on the rotor. One further observation which supports this analysis is that the shape of the voltage is different. The relation between the on and off time seems to be flipped, as the GaNFET was previously off for longer than it was on. This is flipped in Figure 6.10.
To test whether the rotor is actually charged, the experiment is run with the bias voltage set to 0 V and the rotor is charged by applying the fingers. If the rotor is charged, it should be able to successfully turn the GaNFET on and off, even with no external voltage. The experimental data can be seen in Figure 6.12.

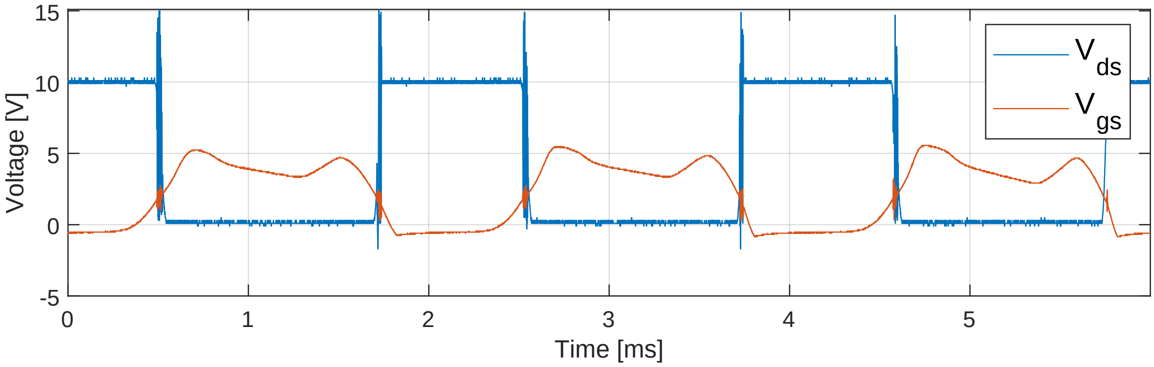


***Figure 6.12:*** Data from the experiment with no bias voltage applied.

The graph shows the GaNFET being turned on, even with no bias voltage. This heavily indicates that the rotor is in fact being charged, which opens up a possible future design. If the biasing voltage is not necessary, the rotor could be permanently charged by being made of electret. This could simplify the design significantly, however analysis and testing would have to be done to confirm the long term viability of such a configuration.

# Conclusion 7

In this project, a variable capacitor is designed for use as a voltage actuator. The specific use case was chosen to be a gate driver. This was done to answer the following problem statement:

*How can an actuator be constructed, which can change a voltage by changing the capacitance, and in which situations can it be useful?*

In order to answer the problem statement, the following objectives were set:

- Designing a variable capacitor, including the mechanism for capacitance variation and auxiliary support components
- Constructing the variable capacitor
- Experimentally validate the functioning of the constructed capacitor

These objectives will be considered first, followed by a general consideration of the problem statement.

## Designing and Constructing the Variable Capacitor

A variable capacitor was indeed designed. Decisions were made in order to simplify the design, such as working with straight plates or using a direct coupling between the motor and rotor. These decisions have had an impact on the functioning of the device, but have not served to undermine the core principles. Said more plainly, the decisions only affected the 'polish' of the design. The final design ended up being much larger than the variable capacitor from Murata. This makes it a significantly less attractive option as a gate drive. The fact that the capacitance is not designed to be directly controllable also supports this notion. The constructed device suffered from several problems including warping due to temperature changes, and the rotor being misaligned on several axes, cause unwanted capacitance variations and limiting the smallest distance between the plates. While this design is functional, it is not optimal, and there exist many avenues of improvement.

## Evaluating the Variable Capacitor

The capacitor was evaluated, and found to be able to change a voltage. The specific voltage output waveforms were dependent on the prescence of a zener diode, with the voltage level rising significantly without the zener diode implemented. The voltage was not able to be predicted correctly with the methods proposed in Chapter 2. The voltage prediction could be corrected by considering the zener diode more directly in the analysis, but this only worked when the zener diode was implemented in the circuit. When the zener diode was not implemented, the voltage could not be correctly predicted. This indicates that the measured capacitance was incorrect and that the measurement method needs revision. The models derived in Chapter 2 generally predict system behaviour. Therefore, it is concluded that the measurement and prediction methods are not satisfactory.

### How can an actuator be constructed, which can change a voltage by changing the capacitance, and is it useful as a gate driver?

An actuator, namely the delta-capacitor, was constructed, which uses changing capacitance to control the voltage. This actuator was used to control the voltage of a gate driver. The voltage is not directly controllable, due to the energy being discharged relatively quickly from the device and the fact that the capacitance variation function is static. The actuator is also very large, and must be made to a high degree of precision for accurate predictions of the performance to be possible. It is therefore concluded that the delta-capacitor can change a voltage in a system, but it is not suitable for driving the gate of a FET.

## 7.1 Future Work

While the core concepts of this technology is used successfully, there are many ways of improving several facets of it. In this section, some of them are listed. While the CCR might generally be useful, it needs an accurate measurement of the capacitance to be correct. Therefore, focus should be put on attaining accurate capacitance measurements at any capacitance level, be it low or high. More confidence in the measurements will give more confidence in the evaluation of the performance of the prediction methods. In this endeavour, advanced system identification techniques, such as Kalman filters, can come in handy.

The prediction methods seem to be somewhat viable in the steady state, but the dynamic model was not explored. Having a easily usable dynamic model would help in identifying successful methods for improving the design. Whether the design is pertaining to the variable capacitor or the circuit surrounding it, a dynamic model is a valuable tool.

With a dynamical model, the effect of inductances in the system could be explored. These effects have been neglected in this project, but could possible serve to both help and hinder. With the capacitance change working effectively as a current source, a correctly placed inductance might increase the voltage over the variable capacitor, while keeping the bias voltage at the same value. Similarly, stray inductances in the system might significantly hurt system performance.

The previously proposed idea of using a permanently charged rotor should also be analysed and explored. This has the potential to remove a complicated and expensive part from the system, significantly simplifying the construction.

Experimentation focused on making different capacitance variation functions should be done. While this seems simple enough, fringing fields are often neglected in analysis of capacitance, and they may have a significant impact on the shape of this function. Therefore, a wide variety of diverse functions should be explored, to fully test how big of an impact these fringing fields can have.

Finally, using a variable capacitor as a part of a closed loop control of a voltage might be possible with the use of a properly designed system which support it. As describing the current is done by an inherently non-linear equation, the controller will need to account for this. Standard linearization methods, such as using taylor approximations, might not be viable in this case, as the capacitance, current and voltage are strongly coupled. Therefore, more advanced non-linear control methods could be employed to handle a problem such as this. Feedback linearization is a good candidate for this, along with using certain adaptive control strategies. Due to the difference in time scales which often exist between mechanical and electrical systems, closed loop control will not lend itself well to attenuating noise, but rather as a regulator for slower phenomena. As the changing capacitance acts as a funky current source, such a system might also be used as a means of pushing a lot of current into a system.

While analysis and design of systems and devices which take advantage of changing capacitances is a challenge, it has a lot of potential as an idea. It is therefore suggested that more work should be put into investigating the usability of changing a reactive parameter as an actuator.

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