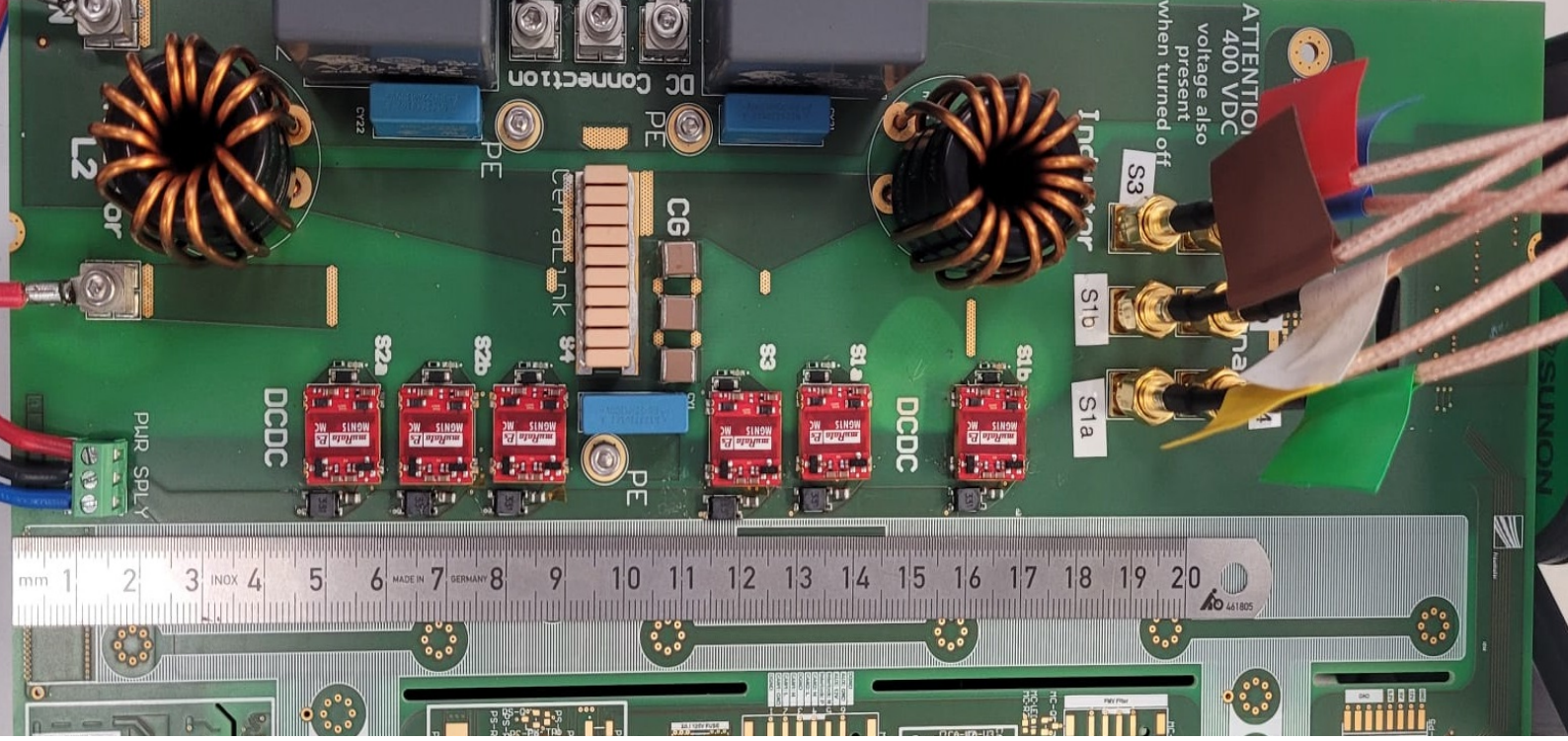

Design and Assembly of a Novel Topology Concept for Bidirectional Grid Connecting Inverters Employing 600V Four Quadrant GaN Semiconductors

Power Electronics and Drives

Department of Energy, PED4-1048, 05-2024

David Levi Ng

STUDENT REPORT

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Abstract:

In this thesis an inverter prototype which enables bidirectional grid connection with a single stage, proposed by Eckart Hoene in context of the EnerConnect project by Fraunhofer Institute Reliability and Microintegration (IZM) is designed, assembled and commissioned. The theoretical foundation of Gallium Nitride (GaN) switches, the flying capacitor principle and the fundamental function of the novel topology are investigated and documented. Instead of the proposed topology, a simplified version with bidirectional devices substituted by two conventional anti-serial GaN switches, no flying capacitor and only GaN High Electron Mobility Transistor (HEMT) devices instead of additional Metal Oxide Semiconductor Field-Effect Transistors (MOSFET)s is designed and assembled. The static control principle and the function of the simplified proposed topology is then verified in Direct Current (DC)/DC laboratory experiments.

Instructions for reading

Relevant literature used for this project includes textbooks, scientific publications, journal articles and data-sheets. Sources are cited throughout the report in the citation style proposed by the Institute of Electrical and Electronics Engineers (IEEE). A list of literature used in this report is presented in the bibliography. Tables and figures are numbered according to chapters and are listed in the provided lists. All symbols, constants and abbreviations used in the report are listed in the nomenclature.

When writing this thesis the following software was used:

- LaTeX and Overleaf - Report Writing
- Portunus - Modelling and Circuit Simulation
- Altium Designer - Printed Circuit Board (PCB) Design
- Matlab - Data Processing
- FLIR Thermal Studio - Temperature Monitoring
- Mendeley - Bibliography Organisation
- Inkscape - Vector Graphics

Preface

This report was written by project group PED4-1048, whose only member is a student of Aalborg University in the spring semester of 2024 from February 2024 to June 2024. During this time period he is doing an internship at the external organisation Fraunhofer IZM in Berlin, Germany. The student expresses gratitude for the cooperation, consulting and support received from colleagues, friends, family and partner throughout the project.

Technical discussions within the Power Electronics research group of Eckhart Hoene were very helpful in expanding my knowledge. I am thankful for the insights, advice and guidance provided by my supervisor at Fraunhofer IZM Stefan Hoffmann. Last but not least, I want to acknowledge the role of my parents and girlfriend whose emotional succour I could always rely on.

David Levi Ng

Aalborg University, May 29, 2024

Contents

List of Abbreviations

2DEG Two-Dimensional Electron Gas

AC Alternating Current

AlGaN Aluminum-GaN

BMBF German Federal Ministry of Education and Research

CAD Computer Aided Design

CAN Controller Area Network

DC Direct Current

DUT Device Under Test

EMI Electro-Magnetic Interference

EMC Electro-Magnetic Compatibility

ESD Electronic System Design

ESS Energy Storage System

EV Electric Vehicle

FOM Figures of Merit

GaN Gallium Nitride

HEMT High Electron Mobility Transistor

IC Integrated Circuit

IEEE Institute of Electrical and Electronics Engineers

IGBT Insulated Gate Bipolar Transistor

IPCC International Panel on Climate Change

IZM Institute Reliability and Microintegration

MBDS Monolithic Bidirectional Switch

MOSFET Metal Oxide Semiconductor Field-Effect Transistors

NASA National Aeronautics and Space Administration

NPC Neutral Point Clamped

OBC On Board Charger

PCB Printed Circuit Board

PE Protected Earth

PV Photovoltaic

PWM Pulse-Width Modulation

SiC Silicon Carbide

SIIT System Integration and Interconnection Technologies

UN United Nations

UPS Uninterruptible Power Supply

WBG Wide Band Gap

1 Introduction

Long term variations in global weather patterns and temperature are commonly described as climate change. A rise in average earth surface temperature has severe consequences on ecosystems in forms of heat waves, drought, floods, famine, lethal storms and other disasters. In January 2024 the average of the past 12-months time period was over 1.5°C above the preindustrial benchmark value [1], failing a goal of the United Nations (UN) Paris Agreement and showing the increased need for action [2]. Therefore, the International Panel on Climate Change (IPCC) concludes that climate change is an immediate threat to planetary health while the window of opportunity to secure a liveable and sustainable future is rapidly closing [3]. The UN speaks of an emergency and states that solving this problem is one of the most difficult challenges faced by humanity [4]. National Aeronautics and Space Administration (NASA) finds that human activity, primarily the burning of fossil fuels, has fundamentally increased the concentration of greenhouse gases which are responsible for warming of the planet [5].

The transition from fossil fuel as primary energy source to sustainable green electric power in every aspect of society such as private households, industry and mobility is the single solution to address the climate emergency [6]. Solar and wind energies are the only two truly renewable energy sources available which have potential to meet 100% load satisfaction globally [7], [8]. Core inherent differences in their nature of operation compared to conventional fossil fuel based power plants, are a decentralized production and intermittent nature. This means that the energy generation is not by a single large power plant but instead spread out to many, distributed small plants and strongly impacted by fluctuating factors such as wind speed and solar irradiance. In order to maintain core qualities of the electric power supply grid such as reliability, stability and quality, the role of Energy Storage System (ESS) becomes vital to maintain grid balance [9]. To overcome the challenge of a green transition in the energy sector in an economically and sufficiently fast manner, it is without alternative to utilize existing grid infrastructure and minimize investment costs.

A forecast for the year 2050 made at the European Conference on Power Electronics and Applications (EPE ECCE) in Aalborg 2023 estimates a total of $100.000\ GW$ of installed converter power with a lifetime of 20 years which means $5000\ GW$ to be replaced each year [10]. These conditions lead to a large need of power electronic converters which bidirectionally connect DC ESS with the Alternating Current (AC) grid at a high efficiency level, especially for low power application between $1\ kW$ to $100\ kW$. Given the immense quantity of converter power which is mostly expected in low power applications, it is necessary to produce highly efficient converters in an automated production at low production and resource cost. Novel bidirectional GaN monolithic semiconductors with four-quadrant properties offer new possibilities to achieve this goal by lowering absolute number of chips required for the same total of installed converter power, conserving resources and reducing costs to achieve a sustainable and reliable

future power grid [11].

1.1 Fraunhofer Institute and Research Project EnerConnect

The Fraunhofer Society is a German research facility of over 30.000 employees working at 76 institutes spread over Germany which focus on different fields of applied science since 1949. The Fraunhofer principle is to prioritize key future-relevant technologies and resemble a link between academia and industry to exhilarate the innovation process. Fraunhofer has an annual research budget of more than EUR 3.0 billion of which more than two third of the income is earned by industry contracts and the remaining third is financed via government grants to support research [12]. Fraunhofer IZM is a research institute with 430 employees in Berlin, Germany, and specializes in high performance packaging of power electronics since 1993. In 2023 IZM has an annual budget of almost EUR 40 million of which over 40% results from industry contracts. The department System Integration and Interconnection Technologies (SIIT) engineers and produces individual highly integrated electronic systems for industry partners in different application fields such as medical, automobile, aviation and communication. Current projects of the research group power electronics include EnerConnect which is patronized by the German Federal Ministry of Education and Research (BMBF) within the funding program ForMikro 2.0. On the one hand side, the BMBF is responsible for the legislation in regards to extracurricular education, vocational training and promotion of education. Furthermore, the BMBF provides funding for research in all areas of science, support of the next generation of young scientists as well as international exchange with a total budget of EUR 20 billion in 2022 [13]. The program ForMikro 2.0 is within the subgroup funding for electronics and electronic systems which is financed with a total of EUR 283 million. The objective of ForMikro 2.0 is similar to the Fraunhofer principle as it is stated that the target is to strengthen the innovative power by acceleration of the knowledge transfer between research academia and commercial industry application [14].

Specifically, the topic of EnerConnect is to investigate the potential of possible topologies relying on monolithic bidirectional GaN semiconductors for low power grid connection of ESS. The project EnerConnect has a budget of EUR 400.000, started in February of 2024 and is set to a duration of four years until February 2028. Conventionally, power electronic topologies to connect ESS with the three-phase power grid consist of a boost and a buck stage. This results in the energy to pass through two conversion stages reducing the efficiency as well as the dependence on an increased number of devices for two stages instead of one. In these conventional topologies power electronics often operate at a higher voltage level than required resulting in higher switching losses. With the development of bidirectional devices, single stage buck-boost topologies become commercially interesting as the novel devices reduce the semiconductor area by factor four. EnerConnect has the objective to find an answer to the question whether there will be a paradigm shift in topologies for grid applications due to development of novel GaN semiconductors. Therefore, it is investigated if concepts utilizing monolithic bidirectional switches are attractive in regards to complexity of control, efficiency, competitive costs and size of magnetic components and Electro-Magnetic Compatibility (EMC) filters. Single stage con-

version reduces the power losses between grid and battery as less transistors are conducting the current. This results in the fundamental research question of the project EnerConnect: is it possible to reach 99% efficiency between grid and battery?

1.2 Project Scope

The work of this thesis is embedded in the project EnerConnect and uses resources and the laboratory facilities of Fraunhofer IZM. This thesis starts simultaneously with the framework project and has a duration of four months until 31.05.2024. The main objective of this thesis is to develop and assemble a prototype which enables grid connection with a single stage, proposed by Eckart Hoene in context of the EnerConnect project by Fraunhofer IZM [15]. The theoretical foundation of GaN switches, flying capacitor principle and design criteria are documented. Instead of the proposed topology, a simplified version with bidirectional devices substituted by two conventional anti-serial GaN switches, no flying capacitor and only GaN HEMT devices instead of additional MOSFETs is designed and assembled. The static control principle and the function of the simplified proposed topology is then investigated in DC/DC laboratory experiments. The objective of the thesis is summarized:

Research task:

> Design, parameterization, assembly, and commissioning of a single stage, buck-boost AC/DC converter for grid connection of DC energy systems.

To achieve the research task, the proposed converter topology is first evaluated in the simulation environment Portunus to investigate the function [16]. The required blocking voltages of the semiconductors are identified. Inductive and capacitive components are parameterized. The commutation loop is investigated to design a low inductive switching topology. A PCB including the gate driver circuits for the active elements of the topology is then designed with the program Altium Designer [17]. The PCB and the components are ordered and assembled in the power electronic laboratory of Fraunhofer IZM. DC/DC experiments are defined to validate the simulation results and document the behaviour of the topology in terms of power loss. The findings are protocolled and evaluated to serve as a foundation to enable further research within the EnerConnect project.

1.2.1 Project Limitations

Simplification to the topology are made and the objectives of the project are limited.

- The project excludes the design of the inductances and Electro-Magnetic Interference (EMI) filter.
- In a first practical setup a design of a single stage buck-boost topology is done without flying capacitor and bidirectional GaN switches.
- As bidirectional GaN switches are not expected to be available at the beginning of the project EnerConnect, they may be replaced by an anti-serial connection of substitute

switches which are to be replaced once bidirectional switches are available during the course of the project.

- The design layout enables connection for measurement units and connection of a closed loop controller, though the control is not within the scope of this thesis.

1.2.2 Project Structure

The structure of the thesis is as follows:
In Chapter 1 the thesis is is motivated and placed into context within the frame project and background of involved institutions.

In Chapter 2, conventional two stage grid connecting converter systems and the novel single stage topology are compared. The fundamental theory of flying capacitor in power converters and monolithic bidirectional GaN switches is introduced, an overview of the dual gate GaN Monolithic Bidirectional Switch (MBDS) is given and the operating principle is explained.

In Chapter 3, the simulation findings of the proposed topology are shown. This includes the operation modes, the modulation index, the commutating switches for each operation mode and the blocked voltage for the switches. A simulation of full sine operation is shown.

Chapter 4 focuses on the design and layout of the topology. The gate driver circuit and the commutation loop are presented along with the components used to assemble the inverter. A first approach to the experiments is described.

In Chapter 5, the laboratory work is described and the experimental results are shown. The experiments are categorized and individually presented.

Chapter 6 discusses the results and draws a conclusion of the project based on the research question formulated. An outlook of possible future work based on this project and the continuation within EnerConnect is assessed.

2 Fundamental Theory

In this Chapter the fundamental theory of existing two stage topologies for grid connection of ESS is given. Additionally, the single stage topology investigated in this master thesis is presented and explained. As the presented concept relies on dual gate bidirectional GaN devices and a flying capacitor topology, these are individually introduced. In this project the bidirectional GaN transistors are substituted.

2.1 Conventional Two Stage Grid Connecting Topology

In order to bidirectionally connect a three phase AC grid to a DC ESS the inverter needs to be able to transform all voltage levels of the three sinusoidal phases to the steady DC value. This task becomes harder when the DC value is variable as in battery applications. Recent state of the art publications on bidirectional grid interface converters connecting ESS rely on two power conversion stages [18],[19].

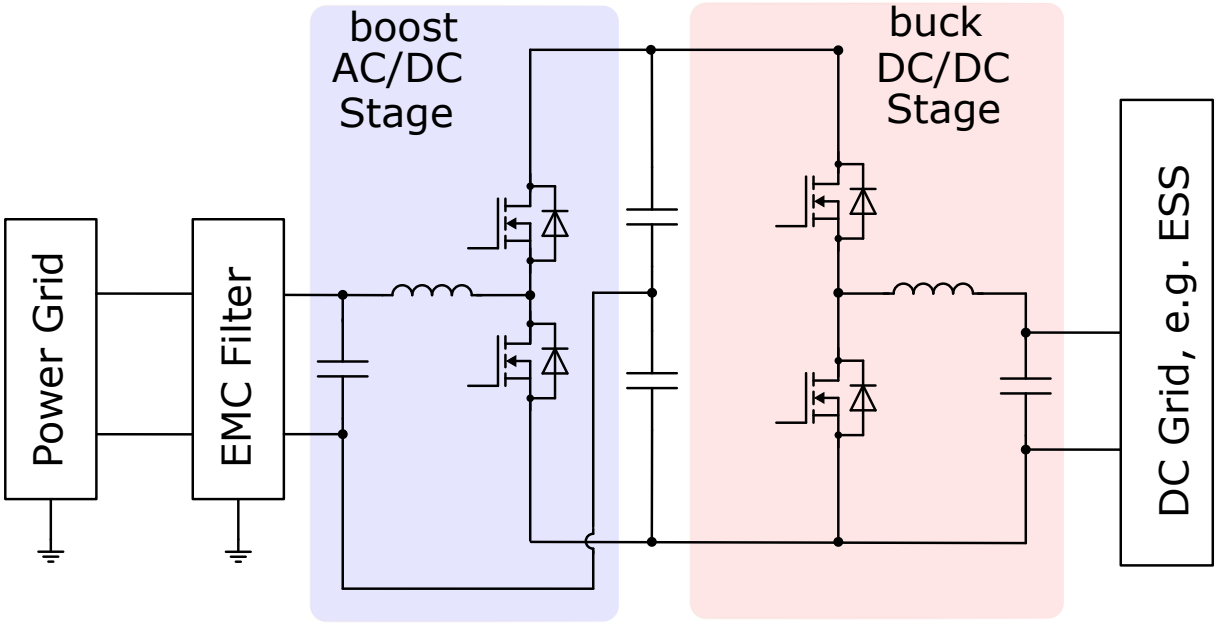

Figure 2.1: Conventional Topology of Dual Stage Grid Connecting Converter.

Figure 2.1 shows an exemplary, simple conventional bidirectional grid interface converter which consists of an AC/DC stage and a DC/DC stage with a shared DC-link [20]. Possible applications for this topology include Uninterruptible Power Supply (UPS), stationary battery systems, fuel cells, Photovoltaic (PV) systems or Electric Vehicle (EV) charging. In Figure 2.1 an arbitrary ESS is connected to the DC-side of the topology and an EMC Filter is connected between the power grid and the AC-side. A simple DC/DC boost converter is displayed in Figure 2.1, however different DC/DC converter topologies can be used depending on the application. The

chosen topology is critical for charging and discharging battery ESSs, has effects on the battery roundtrip efficiency and has impact on the battery lifetime [21]. This stage delivers maximum power to the DC-link capacitance and assures stability of the voltage level. The DC-link capacitor enhances the voltage stability and reduces the fluctuation on the AC output, increasing the power quality [22]. In the second stage, an AC/DC inverter system converts the DC-link voltage to AC power by generation of a sinusoidal AC output with controllable frequency and amplitude. For a power conversion system, the DC input voltage level of a single-phase inverter should be greater than the peak voltage of the inverter's line-to-line AC output voltage. According to this rule, the DC-link capacitance must be chosen sufficiently large enough to decrease the DC-link voltage ripple, which has impact on the output power quality. A simple AC/DC half bridge inverter is displayed in Figure 2.1, however different AC/DC inverter topologies such as full bridge or Neutral Point Clamped (NPC) topologies can be used depending on the application. The semiconductor switching devices for each stage are selected based on the specific design criteria of a system, e.g. switching speed and power capacity. As a rule of thumb, MOSFET switches are chosen for applications with lower power capacity at fast switching speed which results in good output power quality, whereas Insulated Gate Bipolar Transistor (IGBT) switches are used for higher power capacity with medium switching speed [23]. The control strategy used in the bidirectional buck boost converter system has impact on the overall efficiency [24].

With novel Wide Band Gap (WBG) semiconductors available additional factors such as cost have impact on the decision on a switching device material. The topology displayed in Figure 2.1 does not include galvanic isolation, however depending on the regulations of each country grid connected systems galvanic isolation may be mandatory [25]. Usually, this galvanic isolation is realized through an additional transformer stage which reduces the efficiency of grid connected systems. For example, in Spain and Germany galvanic isolation is not used if other technological solutions are employed to separate the electrical grid and the ESS. This decreases the installation complexity, weight, cost, used resources and size of the whole system and increases the total efficiency by 2% [26]. On the other hand, in Italy and the United Kingdom it is a requirement to realize galvanic isolation either by a high-frequency transformer on the DC side or by a low-frequency step-up transformer on the AC side. Due to weight, size and cost problems, line frequency transformers are usually removed when designing a new grid connecting system. However, high-frequency transformers require numerous power stages, which decrease efficiency and raise the costs [27]. Efficiency investigations of a grid interface AC/DC converter show that for a PV battery ESS highest efficiencies of 95.98 % and 95.55% in the charging and discharging modes, respectively, at full-load operation can be achieved [28]. Other publications show, that a full-bridge bidirectional DC/DC converter for battery charging and discharging, has a maximal efficiency of of 96.0% during battery charging and 96.9% during discharging [29]. Analogous to excluding a transformer stage for galvanic isolation increases the efficiency, combining the buck and boost stages to a single stage may increase the efficiency.

2.2 Non-Mirrored Buck Boost Flying Capacitor Three Level Converter

The power electronic topology which is investigated along the project EnerConnect is shown in Figure 2.2. The circuit is first proposed by S. Coday [30] and modified by E. Hoene for the application of decentralized grid connection of ESS. The circuit contains a grid capacitance C_G, an intermediate DC-link capacitance C_{DClink}, two DC capacitances on the side of the ESS C_{DC1}, C_{DC2} and a flying capacitor C_{fly}. The semiconductors used in this topology include four conventional MOSFET switches and two bidirectional blocking GaN switches. Two inductances, one on each polarity of the DC branches, are essential to the functionality of the circuit.

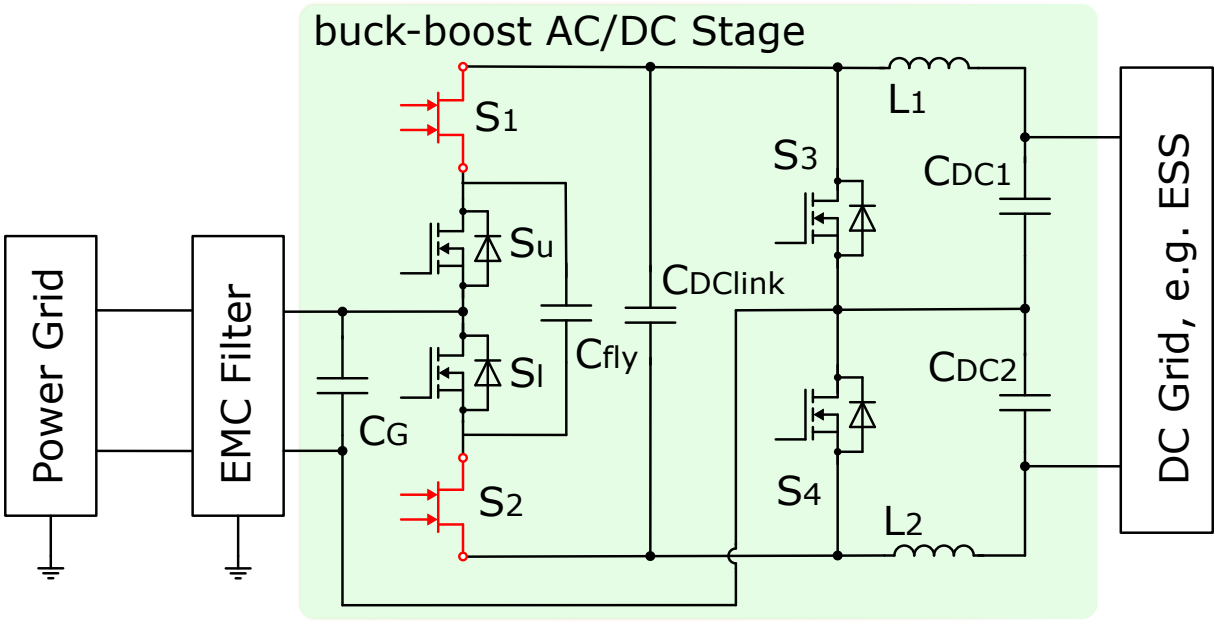

Figure 2.2: Proposed Topology of the Single Stage Grid Connecting Converter.

The grid interface is based on a flying capacitor topology realizing a multilevel structure which shifts the expense for inductive parts to the capacitances to save costs for energy storage. Because the limitation of available bidirectional GaN semiconductors is not expected to exceed $600\ V$ for several years to come, a grid application circuit needs to be realized as three level topology, also because additional levels would increase the complexity, reducing the attractiveness for a commercial realisation. The outer switches on the AC grid side are bidirectional monolithic GaN switches with a maximum blocking voltage of $600\ V$. The switches S_3 and S_2 are Silicon Carbide (SiC) WBG semiconductors with a maximum blocking voltage of $1200\ V$. The switches connecting the flying capacitor S_u and S_l are also SiC WBG semiconductors but with a maximum blocking voltage of $600\ V$. A peculiarity of this topology is that semiconductors are only on one side of the inductances by connecting the inductors on the positive and negative branch of the DC side respectively and capacitances connecting them on either side. Due to the MOSFET switches connecting the potentials to the neutral point the desired buck-boost functionality can be achieved. A drawback of this topology is that two coils are required which increases the complexity and increases the losses as they both absorb the voltage time area. In this Chapter the fundamental theory of the monolithic bidirectional GaN semi-

conductors and the flying capacitor topology principle are presented. An in-depth analysis of the function of the topology displayed in Figure 2.2 is done in Chapter 3.

2.2.1 Lateral Dual Gate Monolithic Bidirectional GaN Semiconductor

GaN is a promising material for power semiconductors because of their wide band gap and resulting high electric field strength, resulting in high power density and reduced size [31]. Because the realization of reliable GaN transistors on cheap silicon substrate instead of expensive exotic substrate materials, GaN transistors have far surpassed state of the art silicon transistors in terms of all relevant Figures of Merit (FOM) [32]. The FOM of a semiconductor device represents an important quality as it pertains to its performance limits. When comparing the performances of switching power devices using their FOMs has become ubiquitous practice in power semiconductor and power electronics industries [33]. The properties of a GaN device are based on the charge of the Aluminum-GaN (AlGaN)-GaN junction which attracts electrons from the surrounding material creating a highly conductive, Two-Dimensional Electron Gas (2DEG). Electrons need a large amount of energy to leave the 2DEG and therefore can be considered to only move in the parallel plane of the junction resulting in a purely lateral device. Furthermore, the 2DEG channel is inherently current bidirectional. To obtain bipolar voltage blocking two gate terminals are added onto the AlGaN substrate which control the conductivity of the channel to its closer drain/source terminal. The polarization discontinuity between p-GaN and the AlGaN layer below create a negative charge driving the device in blocking state and results in a normally-off GaN device [34]. There also exist normally-on devices.

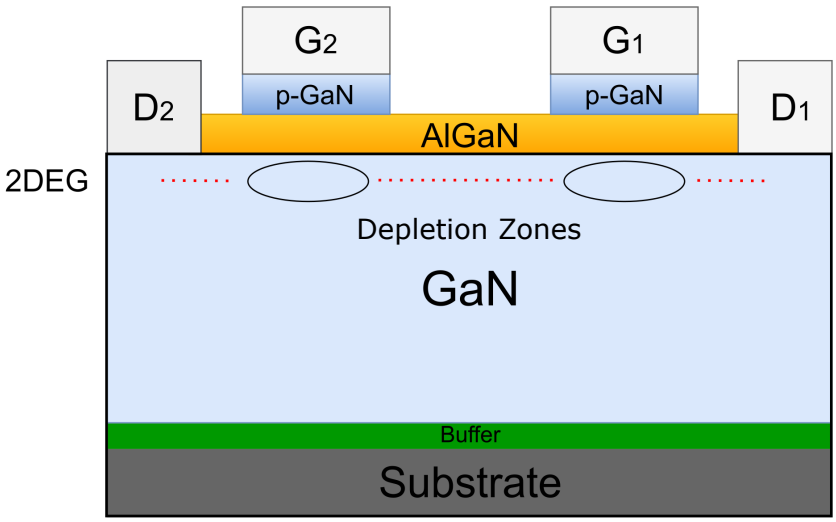

Figure 2.3: Schematic of Normally-Off Dual Gate GaN Device [31].

Current state of the art GaN devices are usually lateral HEMT transistors with very good conduction and switching capabilities. However, the lateral structure limits their maximum blocking voltage to a maximum of 600 V [35]. The basic structure of the device shown in Figure 2.3 can be operated in four different modes. Figure 2.4 displays the possible switching states depending on the two gate signals of a single bidirectional GaN switch.

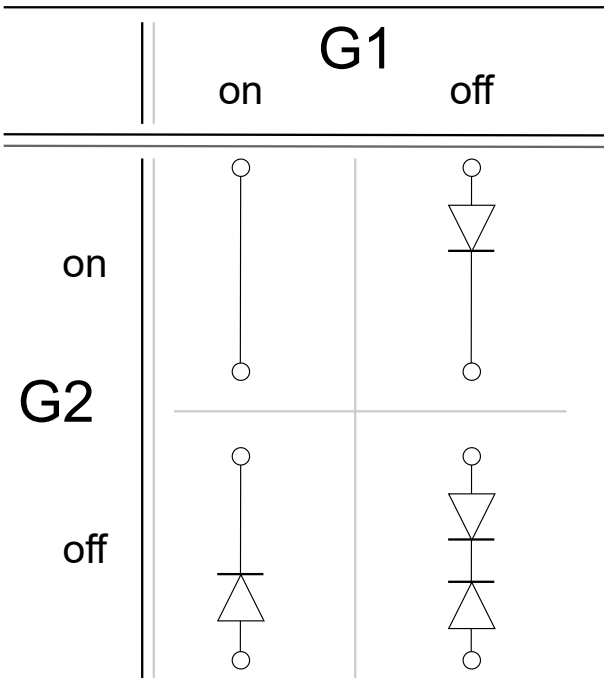

Figure 2.4: Possible Switching States depending on Gate Signals of GaN Switch.

When both gates are off, i.e. low gate voltages are applied, the GaN chip behaves like an open switch. When there is a sufficient voltage applied to gate G_1 the GaN chip behaves like a diode conducting current from pin D_2 to the pin D_1. When a sufficient gate voltage is applied to G_2 the diode is inverted, conducting from pin D_1 to D_2. When both gates are on, i.e. high voltage is applied, the GaN device behaves like a closed switch with reduced conduction losses than in diode mode.

2.2.2 Multilevel Topology Flying Capacitor

Multilevel inverters are of interest for the power electronic industry because of reduction of voltage stress on the semiconductors, reduction of EMI, increment of efficiency, and reduction of dv/dt ratio [36].
The flying capacitor topology was first introduced in 1992 and is able to reduce costs for semiconductors and give a multi-level output with a high output frequency and low dynamic losses [37]. The principle of the flying capacitor is that they provide an offset to the output and thereby add additional voltage levels by usage of high frequency capacitors. Figure 2.5 displays the general topology of the inverter.

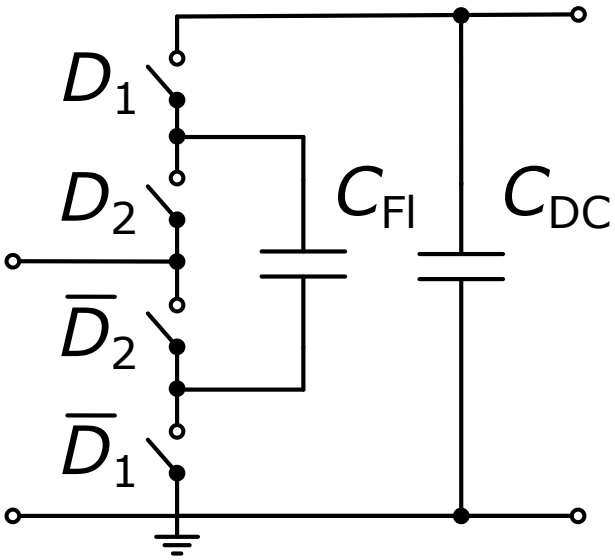

Figure 2.5: Schematic of a Three-Level Flying Capacitor Inverter.

It consists of a DC-link input capacitor C_{DC}, the flying capacitor C_{Fl} and four semiconductor switches. Relatively to the earth, the flying capacitors potential floats which is utilized to create an additional voltage level resulting from the addition or subtraction of the voltage across the capacitance. If the two outer switches are active at the same time, the DC-link and the flying capacitor are shorted which may lead to destruction of semiconductors. If the two inner switches are both in on-state, the flying capacitor is shorted and discharged. Therefore, the switches are labeled D_1 and $\overline{D_1}$ as well as D_2 and $\overline{D_2}$. In the case of a three-level topology, the average voltage of the flying capacitor typically is set to half of the DC-link voltage. The resulting operation modes are displayed in Figure 2.6.

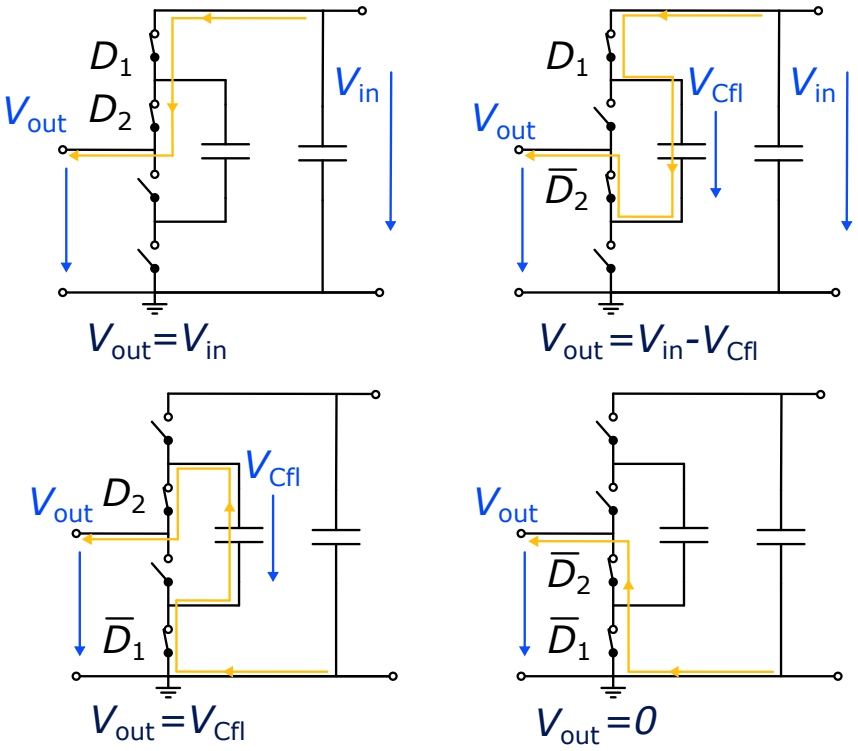

Figure 2.6: Four Operation Modes of the Flying Capacitor Topology.

When operating the three-level flying capacitor inverter, four different modes of operation are possible. The main advantages of utilizing a flying capacitor topology are lower semiconductor voltages and resulting reduced power loss as well as lower voltage and current ripple. This leads to enhanced power quality and reduced size of output filters because of lowered EMI emissions [38].

2.2.3 Substitute Bidirectional Switches

Because bidirectional monolithic GaN semiconductors are limited in their availability even for research, it is decided to supplement the bidirectional switches with two conventional unidirectional HEMT GaN semiconductors arranged in an anti-serial configuration. A bidirectional transistor can be modulated by connecting two unidirectional semiconductors [39]. However, connecting two or more discrete transistors increases the parasitic stray inductance which may lead to overvoltage and oscillation during the switching transients. Furthermore, in this configuration the current conducts through two devices connected in series which results in an increment of the conduction power losses and of the physical size [40]. Hereby, the functionality of the concept as well as the gate driver circuit can be tested before the availability of the bidirectional devices. Once the bidirectional GaN switches are available, they can then simply replace the anti-serial configuration and operate with the same gate driver circuit. The blocking voltage of bidirectional switches is not expected to exceed $600\ V$ which suggests to have an identical blocking voltage and technology of the substitute switches. Therefore, unidirectional $600\ V$ GaN devices from the same manufacturer Infineon are chosen.

3 Simulative Analysis

As introduced in Chapter 1, the availability of dual gate MBDS may lead to a paradigm shift in the industry in terms of converter topologies for grid interfaces. The main objective of this project is to investigate the topology employing novel bidirectional GaN switches shown in Section 2.2 and assemble a prototype to understand its function and compare it to conventional two stage grid-interfaces. Therefore, in this chapter the topology is investigated in a simulation environment to derive the function of the topology. First the fundamental function of a simplified topology is derived. Therefore, the modulation index for a power transfer less operation is derived. The commutating switches for the four operation phases are determined. Afterwards, each operation phase is investigated in regards to the voltage each switch has to block as this has direct impact on the power losses. Finally, the commutation path as well as a closer investigation of the power loss is shown.

The simulation is carried out in Portunus which is a software developed by adapted solutions. It is characterized by combining powerful numeric algorithms and interfaces for programming, automatisation as well as data import and data export. Portunus offers different possibilities of how to describe a system and is suitable for a variety of applications in the fields of electrical energy, power electronics, thermal calculations, magnetic properties and control. Different physical domains such as electrical and thermal are interlinked. Because it has a relatively small user base compared to more publicly known tools like e.g. MATLAB Simulink, the customer support is faster and is able to offer a direct link to the software developers. This leads to it being the preferred software at Fraunhofer IZM.

3.1 Fundamental Function of Inverter Topology

In order to understand the principle of the converter topology proposed in Section 2.2, it is first simplified to a more general circuit excluding the flying capacitor and the associated two MOSFET switches. Furthermore, all semiconductors are replaced by ideal switches, resulting in the following schematic displayed in Figure 3.1. In Figure 3.1 the capacitor C_G is the grid side capacitance and C_{DC} represents the DC-link capacitance, E_G is resembles the AC grid side and E_1 as well as E_2 are the DC side of the ESS. There are two inductances L_1 and L_2 connected to the positive as well as the negative branch of the DC side. On the DC side, the voltage across each source E_1 and E_2 has the same value $V_{DC}/2 = V_1$. To investigate the most fundamental cases, the voltage across E_G for a fixed time is considered a DC voltage V_G with a defined orientation. As the simplified topology still represents the grid connecting inverter introduced in Section 2.2, certain attributes and resulting constrains remain. The circuit is modulated in the simulation environment Portunus and investigated regarding possible operation modes, the blocked voltage across the active semiconductor switches and power loss.

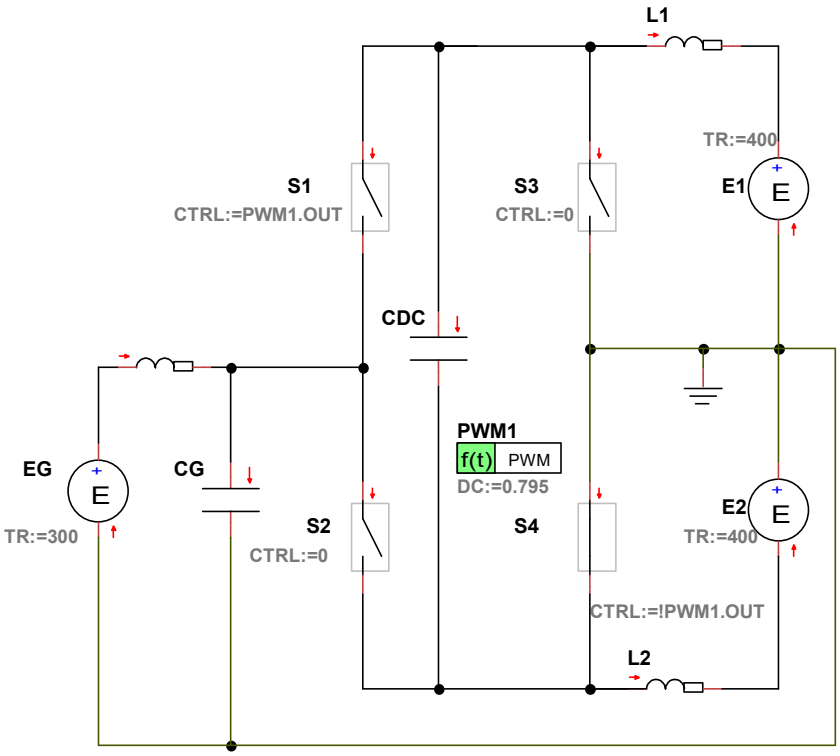

Figure 3.1: Simplified Topology Modulated in Portunus.

The modulated circuit is displayed in Figure 3.1. Depending on the operation mode, the ideal voltage source representing the instantaneous grid voltage E_G is set. It is assumed that for a very short time period, the AC voltage can be simplified to a steady DC value. The sinusoidal AC voltage can then be considered as a sum of DC voltages. An additional inductance is added on the grid side for filtering purpose. Depending on the operation case, a different pair of switches are commutating. The ideal switches S_1 and S_2 represent bidirectional GaN switches which may block a positive or negative voltage. The maximum blocking capability of the monolithic bidirectional switches S_1 and S_2 is limited to $600\ V$. However, when operating semiconductors there should be a sufficient margin to avoid failure and possible destruction of the chip, therefore the voltage of S_1 and S_2 during operation is limited to $500\ V$. The ideal switches S_3 and S_4 represent MOSFET switches which include a body diode intrinsic to the device structure. Therefore, the switches S_3 or S_4 are not capable of blocking a negative voltage and commutation strategies depending on this property are not suited for this topology. Additionally, operating states in which the switches of one leg are both on, for example S_1 and S_2 or S_3 and S_4 result in discharge of the capacitance C. Therefore, these modes result in faults and these switching states are not possible in an error free operation. These two conditions are summarized in Equation 3.1.

$$\begin{aligned} |V_{S1,S2}| &< 500V \\ V_{S3,S4} &> 0V \end{aligned} \tag{3.1}$$

An inverter connecting an AC grid to a DC ESS, has are eight different operation cases depending on the polarity of the voltage V_G, the absolute value of V_G, the battery voltage V_{DC} and application as battery charger or grid stabiliser. These operation phases can be differentiated by buck or boost operation from the AC to the DC side, the polarity of the grid voltage V_G and the direction of power flow. In Figure 3.2 the four fundamental modes $M_{1..4}$ are displayed depending on the DC voltage V_{DC} and the grid voltage V_G. These modes are independent from the direction of power flow and represent the different phases to connect a constant DC to a sinusoidal AC.

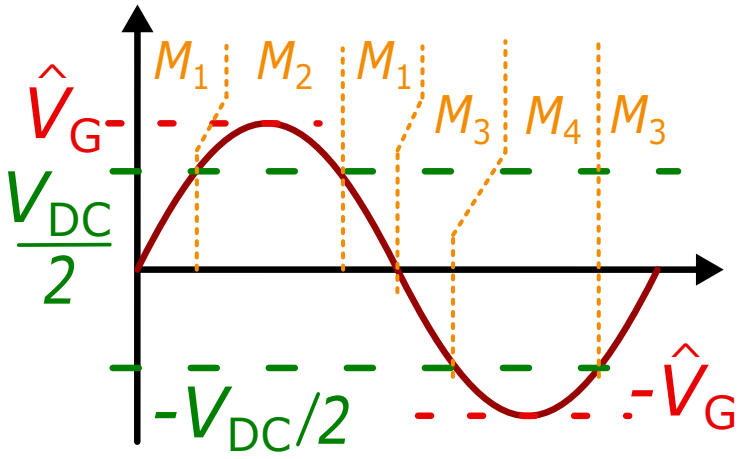

Figure 3.2: Four Different Operation Modes During a Full Sine Phase.

It can be seen that the modulation starts with M_1, representing the boost case of a positive grid voltage until the grid voltage exceeds half of the DC voltage $V_G > V_{DC}/2$. For this duration, the second phase M_2 is active until it switches back to the first mode M_1 when the grid voltage is smaller than half of the DC voltage but still larger than zero $0 < V_G < V_{DC}/2$. In the negative half wave the principle is identically for the modes M_3 and M_4. The conditions for the different modes $M_{1..4}$ are summarized in Equation 3.2.

$$\begin{aligned} M_1 &:= 0 < V_G < V_{DC}/2 \\ M_2 &:= V_{DC}/2 < V_G \\ M_3 &:= -V_{DC}/2 < V_G < 0 \\ M_4 &:= V_G < -V_{DC}/2 \end{aligned} \tag{3.2}$$

Simulation of the four different phases of commutation for all possible pairs of commutating switches lead to the results presented in Table 3.1. Other switch configurations result in violations of the previously mentioned conditions or in higher blocking voltages which is undesirable due to the additional stress on the semiconductors. The active switches in each operation phase were obtained via simulation after the determination of the modulation index but for better understanding the results are shown before the derivation of the modulation index. In order to connect an AC sine to a DC ESS four commutation modes need to be applied. They result from either bucking or boosting a positive or negative grid voltage V_G to the corresponding battery voltage V_{DC}.

Table 3.1: Commutating Switches in Different Operation Phases and Voltage Conditions.

	$V_G > 0$	$V_G < 0$
Boost $\|V_G\| < V_{DC}/2$	M1: S_1/S_4	M3: S_2/S_3
Buck $\|V_G\| > V_{DC}/2$	M2: S_1/S_3	M4: S_2/S_4

For an operation phase of boosting a positive grid voltage V_G to a larger DC voltage V_1, the switches S_1 and S_4 are active. When boosting a negative grid voltage V_G to a larger DC voltage V_1, the switches S_2 and S_3 are commutating. For an operation phase of bucking a positive grid voltage V_G to a smaller DC voltage V_1, the switches S_1 and S_3 are active. For the remaining case of bucking a negative grid voltage V_G to a smaller DC voltage V_1, the switches S_2 and S_4 are commutating.

In Subsection 3.3, these operation modes are investigated in regards to the blocked voltage across the semiconductors. However, first the calculation done to determine the duty cycle for each operation phase is presented. The direction of power flow can be set by increasing or decreasing the duty cycle which is also known as modulation index. This result in eight different operation modes as each of the four modes displayed in Table 3.1 can be operated for battery charging or grid stabilization depending on the direction of power flow. For clarification all possible operation variants are shown in Table 3.2.

Table 3.2: All Possible Operation Modes when Bidirectionally Connecting an AC Grid to DC ESS.

	$V_G > 0$	$V_G < 0$
Battery charging AC to DC		
Boost $\|V_G\| < V_{DC}/2$	$M1_a$	$M3_a$
Buck $\|V_G\| > V_{DC}/2$	$M2_a$	$M4_a$
Grid stabilization DC to AC		
Boost $\|V_G\| < V_{DC}/2$	$M1_b$	$M3_b$
Buck $\|V_G\| > V_{DC}/2$	$M2_b$	$M4_b$

3.1.1 Determination of Duty Cycle

The modulation index m is used to control the power flow from AC to DC or in the opposite direction. When the modulation index is exactly the calculated value resulting from the formula shown in Table 3.3, there is no power flow. Instead AC side and DC side are connected without power exchange. By increasing or decreasing the modulation index by a small percentage, a power flow in the desired direction can be achieved. Therefore, it is essential to determine the formula of the modulation index depending on the topology. In order to calculate the modulation index m, the display of the circuit is modified so the commutating switches resemble a conventional half bridge converter topology. The resulting circuit is shown in Figure 3.3.

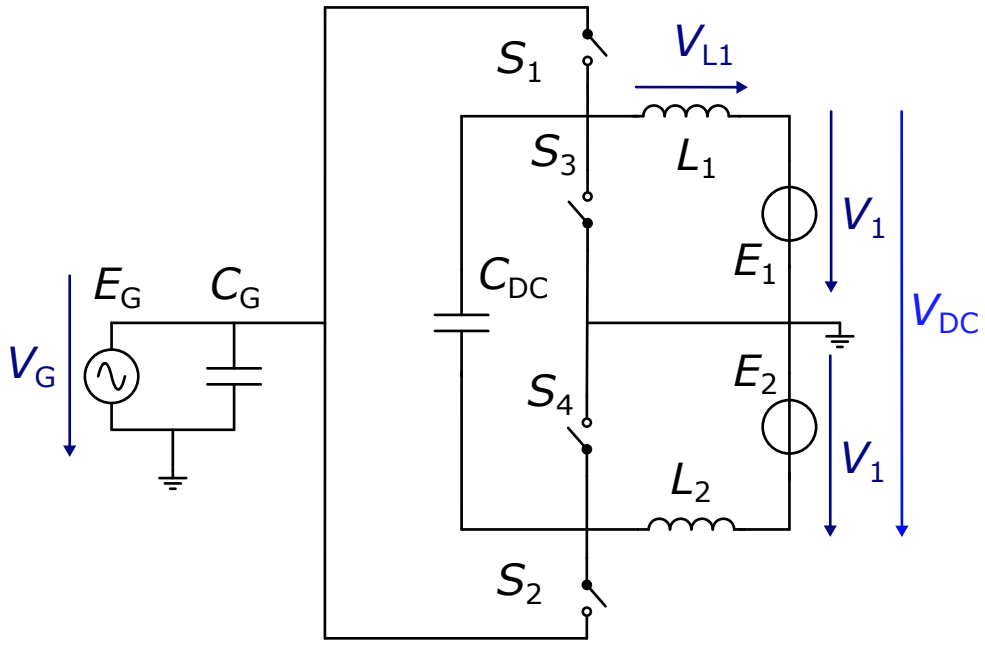

Figure 3.3: Simplified Topology in Conventional Half Bridge Configuration.

The switches S_1 and S_2 are rotated and placed opposite to S_3 and S_4 respectively, thereby resembling a half bridge of a buck converter with the input side E_G and the output side resembled by E_1 and E_2. Furthermore it can be seen that both DC sources have the same voltage value V_1 which is half of the voltage V_{DC}, also displayed in Equation 3.3.

$$V_1 = V_{DC}/2 \tag{3.3}$$

The duty cycle m of two commutating switches S_i and S_j is defined as the time period in which the switch S_i is active t_{Si} divided by the total time period of commutation T_s which is the inverse of the switching frequency f_s. S_i is inverse to S_j, meaning that it is in on state whenever S_i is off which can also be described mathematically as $S_i = \overline{S_j}$. Consequently, the remaining time per switching period is the time t_{Sj} during which the switch S_j is active, assuming that the dead time is negligible. Therefore, the time period t_{Si} in which switch S_i is active is in relation to t_{Sj} and T_s. By definition, the modulation index m can only be between 0 and 1 while the cases of 0 or 1 represent the the situation with no commutation because one of the switches is active for the entire switching period.

$$\begin{aligned} T_s &= \frac{1}{f_s} \\ m &= t_{Si}/T_s \\ t_{Si} &= T_s - t_{Sj} \\ 0 &\leq m \leq 1 \end{aligned} \tag{3.4}$$

In Table 3.3 it is shown how to change the modulation index to achieve a desired power flow. A power flow from the AC grid to the DC side represents charging of the ESS. An opposite direction of power transfer resembles the case of the ESS stabilizing the AC power grid. A modulation index of m_0 is the balanced case in which no power transmission is achieved.

Table 3.3: Power Flow for Variation of Modulation Index in Different Operation Modes.

	Modulation Index m_0	AC to DC	DC to AC
AC Boost $\lvert V_G \rvert < V_{DC}/2$	$\frac{V_{DC}/2}{V_{DC} - \lvert V_G \rvert}$	$m < m_0$	$m_0 < m$
AC Buck $\lvert V_G \rvert > V_{DC}/2$	$\frac{V_{DC}/2}{\lvert V_G \rvert}$	$m_0 < m$	$m < m_0$

In the following Subsections 3.1.2 and 3.1.3, the derivation of the results displayed in Table 3.3 is shown.

3.1.2 Modulation Index for Buck Mode Operation

For the case of bucking a positive grid side voltage V_G, S_1 and S_3 are commutating, therefore the switches S_2 and S_4 are permanently off during this operation mode. The modulation index m_0 is calculated from the circuits shown in Figure 3.4.

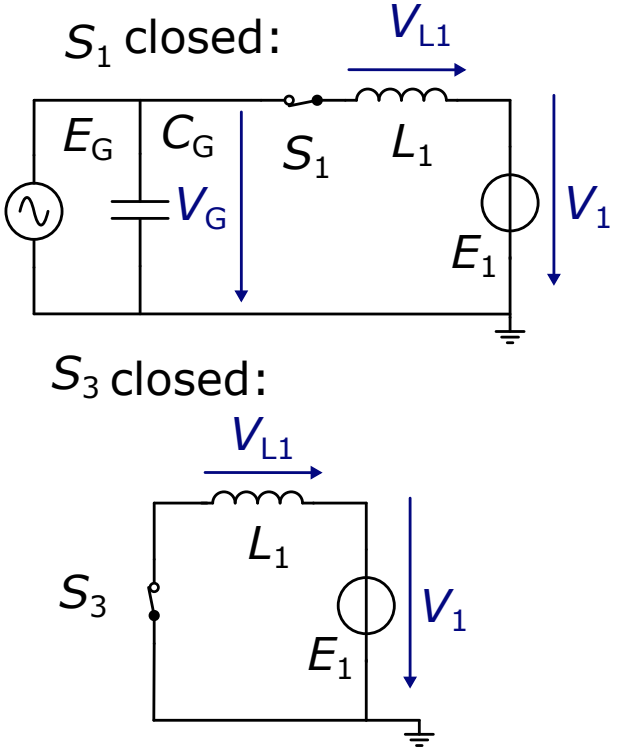

Figure 3.4: Resulting Circuits for Commutation Modes during Buck Operation.

The voltage time area across an inductance averages to zero over a full switching period T_s. For the inductance L_1 this is expressed in Equation 3.5.

$$0 = m_0 \cdot V_{L1}(t_{S1}) + (1 - m_0) \cdot V_{L1}(t_{S3}) \tag{3.5}$$

Here, $V_{L1}(t_{S1})$ represents the voltage across the inductance L_1 over the time period t_{S1}, the time period during which the switch S_1 is active. Similarly, the time period t_{S3} represents the duration of S_3 being active. According to Kirchhoff's second law, the directed sum of the voltages around any closed loop is zero [41]. Applying Kirchhoff's second law to the either case, S_1 on and S_3 off and vice versa leads to Equation 3.6.

$$\begin{aligned} V_{L1}(t_{S1}) &= V_G - V_1 \\ V_{L1}(t_{S3}) &= -V_1 \\ V_1 &= V_{DC}/2 \end{aligned} \tag{3.6}$$

By inserting Equation 3.6 into Equation 3.5 and simplifying, the modulation index m is expressed by Equation 3.7.

$$m_0 = \frac{V_{DC}/2}{V_G} \tag{3.7}$$

For the analogous case of bucking a negative grid voltage V_G by commutation of the switches S_2 and S_4, the calculation shows that the voltage V_1 across the source E_2 is to be divided by the negative grid voltage V_G to obtain the modulation index m_0, similar to the positive case. To resemble both cases with a single formula, Equation 3.7 is modified so that V_1 is divided by the absolute value of V_G as shown in Equation 3.8.

$$m_0 = \frac{V_{DC}/2}{|V_G|} \tag{3.8}$$

3.1.3 Modulation Index for Boost Mode Operation

For the case of boosting a positive grid voltage V_G, S_1 and S_4 are commutating while the switches S_2 and S_3 are permanently off during this operation mode. The resulting circuit for S_4 is displayed in Figure 3.5, the circuit resulting from switch S_1 being closed is shown in Figure 3.4.

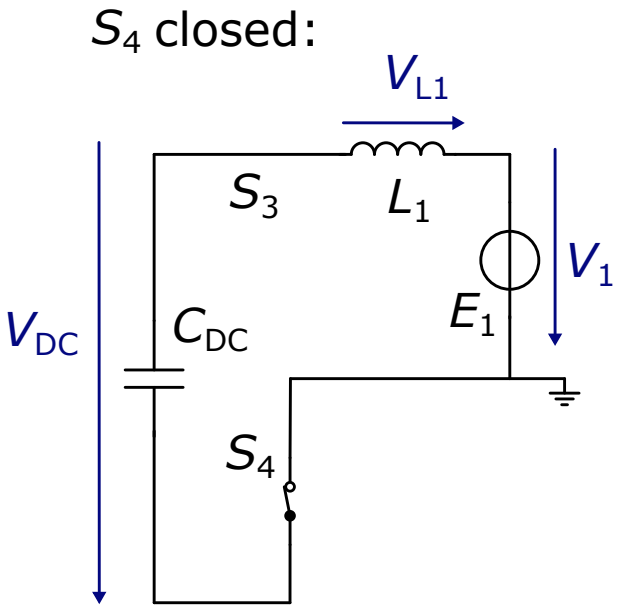

Figure 3.5: Resulting Circuits for Commutation Modes during Boost Operation.

The approach to calculate the modulation index is the same as in Subsection 3.1.2, the voltage time area of a coil is zero for a full switching period. It can be seen from the circuits in Figure 3.5, that in the boost case the capacitance C_{DC} is part of the mesh. The DC sources E_1 and E_2 have the same value V_1 which results in the voltage across the capacitance V_C to be $2 \cdot V_1 = V_{DC}$. As before, Kirchhoff's second law is applied to obtain the values for the voltages across the inductance L_1 for either time period t_{S1} and t_{S4}. The calculation of the modulation index m for the boost cases is shown in Equation 3.9.

$$\begin{aligned} 0 &= m_0 \cdot V_{L1}(t_{S1}) + (1 - m_0) \cdot V_{L1}(t_{S4}) \\ V_{L1}(t_{S1}) &= V_G - V_1 \\ V_{L1}(t_{S4}) &= V_C - V_1 \\ m_0 &= \frac{V_C - V_1}{V_C - |V_G|} \\ &= \frac{V_{DC}/2}{V_{DC} - |V_G|} \end{aligned} \tag{3.9}$$

The calculation off the modulation index m_0 for the boost operation of a negative grid voltage V_G is analogous. In this operation case S_2 and S_3 are commutating and the calculation result in an identical modulation index m_0.

3.2 Commutation Phases and Low Inductance Layout

The term commutation cell was developed by H. Foch and describes the basic structure of a power electronic circuit which determines the switching properties [42]. High power density and compactness are increasing in importance for power electronic systems. Especially, in high frequency applications special attention needs to be paid to parasitic inductances as it is often the bottleneck limiting switching speed and causing power loss [43]. This includes the parasitic inductances arising from the spatial construction, i.e. the physical implementation of the circuitry. The commutation cell is defined as the mesh in which the current during a commutation is changing conduction direction due to the switching event. With an analytical approach the commutation loop can be optimized in regards to a low inductance layout in regards to the geometric area spanned by this commutation mesh [44]. To optimize the PCB layout, the main commutation mesh area is minimised in the design since the spanned area is directly proportional to the parasitic inductances of the commutation cell [45]. Therefore, the circuit elements which are responsible for the parasitic inductances should be arranged with as little distance to one another as possible. In order to determine the commutation cell of an arbitrary topology, the conduction path before and after the commutation is drawn in the schematic. The parts of the meshes which are not overlapping compose the commutation cell. This is done for the topology investigated in this thesis.

3.2.1 Commutation for Buck Case of Positive Grid Voltage

In order to better understand the commutation for the buck case of a positive grid voltage, the circuit displayed in Figure 3.1 is further investigated. As shown in Table 3.1, the commutating

switches for this operation case are S_1 and S_3. The switches S_2 and S_4 are permanently off during this mode. The conducting current in the switches, the DC capacitor, the grid capacitor and the inductances L_1 and L_2 are measured during the commutation events. Furthermore, the power flow as well as the capacitors voltages are measured. The modulation index is increased by 1% to achieve a power flow from the grid to the DC side. This resembles an application in which the ESS is charged by the power grid. The measurements obtained by simulation are shown in Figure 3.6.

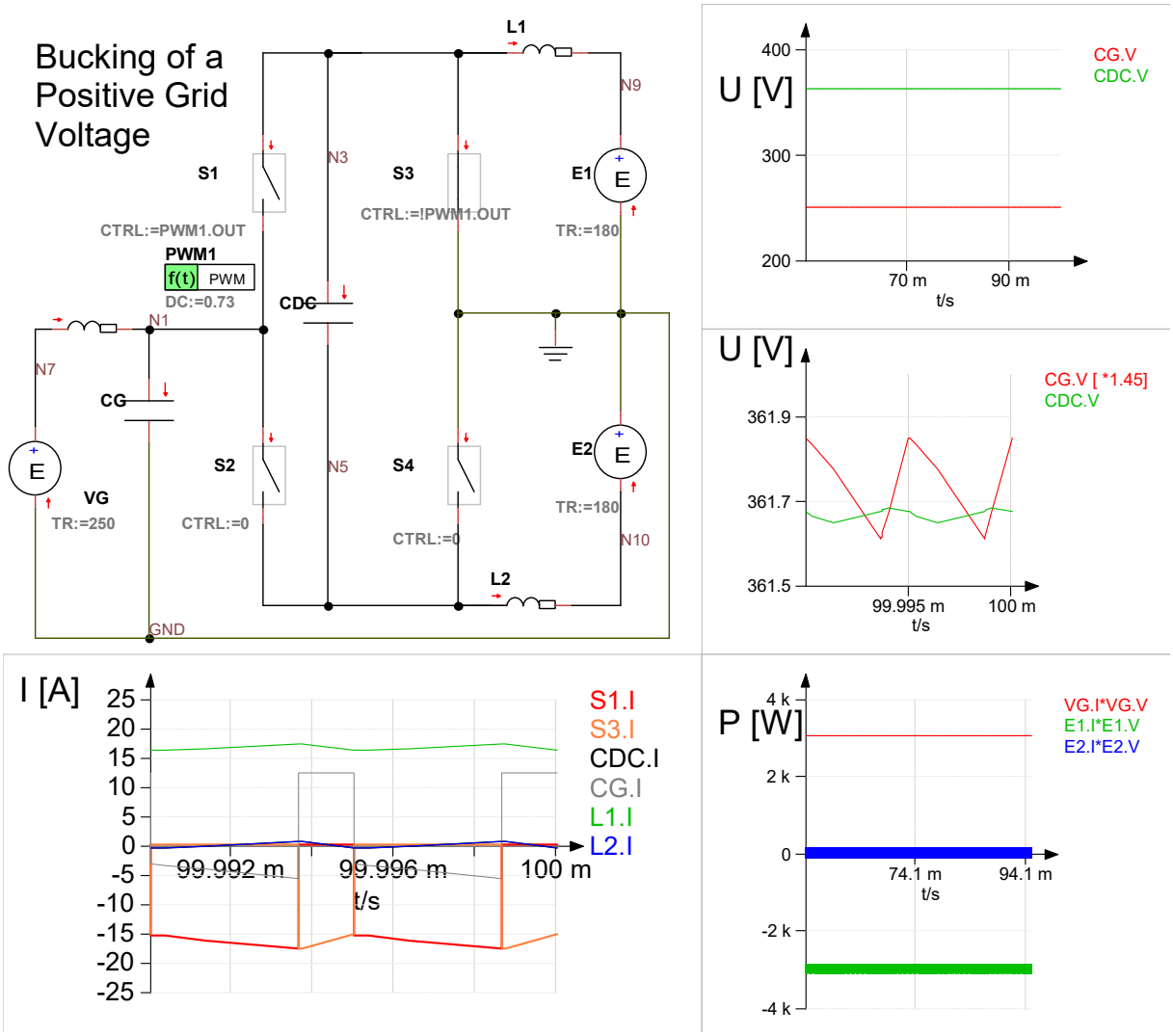

Figure 3.6: Simulation of Buck Case for Positive Grid Voltage with Power Flow into the Grid.

In this DC/DC simulation the grid voltage is set to $V_G = 250V$ and the DC voltage is set to $V_{DC} = 360V$. This simulation resembles an operation in mode M_2 depicted in Figure 3.2. In this mode the sinusoidal grid voltage V_G is positive and larger than the positive DC voltage $V_DC/2$ and thus needs to be bucked to connect the grid and the ESS. Both capacitances have an approximately constant voltage throughout the commutation phases. Assuming the transients have subsided, in the initial moment of a commutation the grid capacitance is charged to $C_G = 250V$ and the DC capacitance is charged to $C_{DC} = 360V$. The current through the

inductors L_1 and L_2 is nearly constant, too. The current i_{L1} ripples around $16A$ while the current i_{L2} ripples around $0A$. Charging and discharging of the DC-link capacitance C_{DC} is not synchronous to the commutation of the switches S_1 and S_3. Charging and discharging of the grid capacitance C_G is synchronous to the commutation of the switches S_1 and S_3.

When the switch S_1 is closed, the grid capacitance C_G discharges. The current through both inductances L_1 and L_2 increases. The ripple current through inductance L_2 changes polarity. As this current i_{L2} is identical to the current through the DC-link capacitance $CDC.I$, the capacitance C_{DC} charges and discharges during the commutation phase in which S_1 is closed. This can be seen in Figure 3.6 in the voltage plot of the capacitances CG and CDC but also in the current plot which shows the current of the grid capacitance $CG.I$ being negative. The current splits into both paths and conducts through both inductances L_1 and L_2 to the DC side.

When the switches commute and S_3 conducts while S_1 is open, the grid capacitance C_G is charged. The current through both inductances L_1 and L_2 decreases. The ripple current through inductance L_2 changes polarity. As this current i_{L2} is identical to the current through the DC-link capacitance $CDC.I$, the capacitance C_{DC} charges and discharges during the commutation phase in which S_3 is closed. This can be seen in Figure 3.9 in the voltage plot of the capacitances CG and CDC but also in the current plot which shows the current of the grid capacitance $CG.I$ being positive. positive. The current splits into two paths and conducts through both inductances L_1 and L_2 to the DC side. This is behavior is illustrated in Figure 3.7 for the two cases of S_1 or S_3 being the conducting switch.

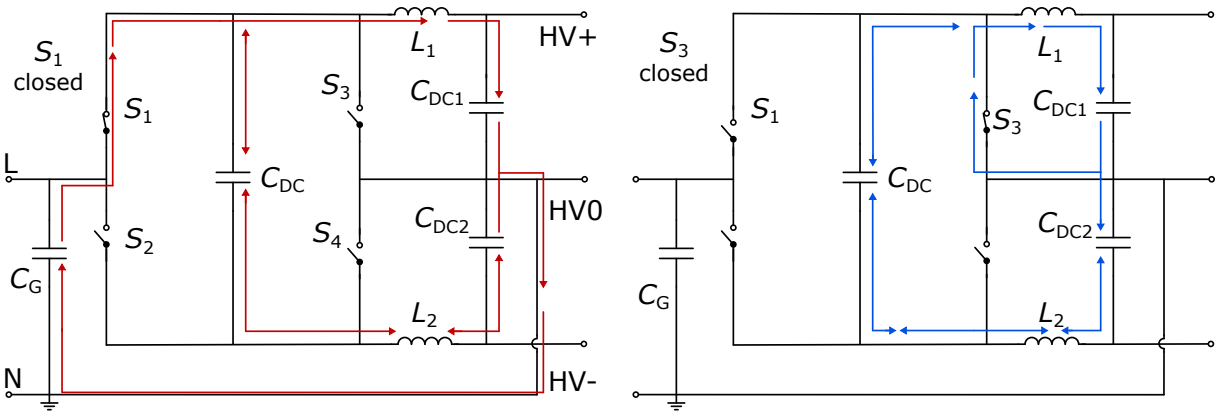

Figure 3.7: Current Direction and Path for Commutation Phases in Buck Case of Positive Grid Voltage.

This is valid for a power flow from the AC grid side to the DC ESS side or in other words a modulation index larger than m_0 described in Equation 3.8. This can also be seen in Figure 3.9 which shows that the power of the grid side has a positive value of approximately $3kW$ and the positive DC side power being approximately the negative value of the grid side $-3kW$. Furthermore it can be seen that there is an additional power flow from the negative DC side oscillating around zero. In case the power flow is from the ESS into the AC grid, the all currents conduct towards the opposite directions and consequently the charging and discharging of the capacitances is inverted.

Commutation Loop Buck Operation

In order to determine the commutation loop, the change of current di/dt in the measurements of Figure 3.6 is visualized in Figure 3.8. Both inductances are conducting current which can be separated according to the superposition principle and investigated individually.

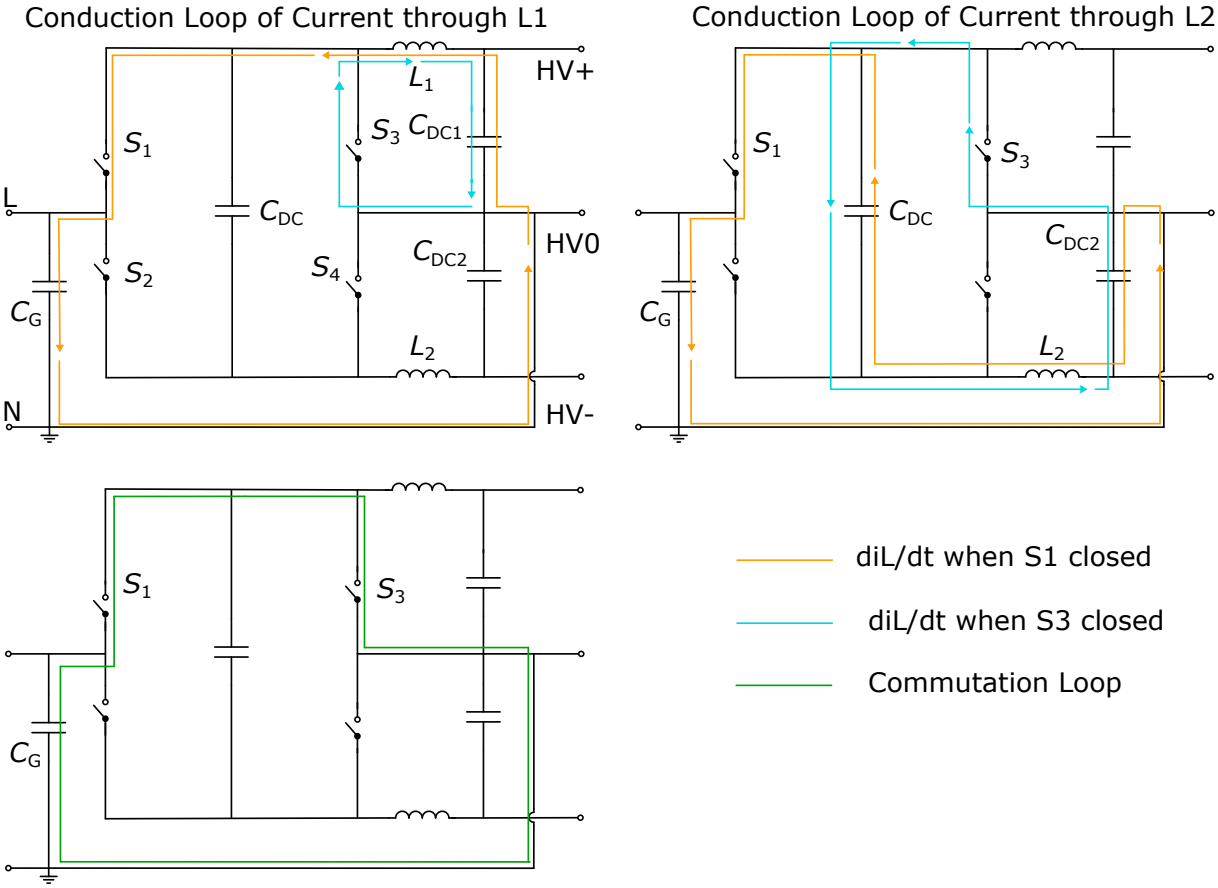

Figure 3.8: Commutation Loop for Buck Case of a Positive Grid Voltage.

In Figure 3.9 it can be seen that the change in current di/dt through both inductances L_1 and L_2 is negative for the switch S_1 being active. When S_4 is active, the change in current di/dt through both inductances L_1 and L_2 is positive. Similarly, the change in current di/dt through the capacitances and the switches is determined and visualized in Figure 3.8. Only the branches of the circuit in which the change in current di/dt is in the identical direction are part of the commutation loop. It can be seen that the switches S_1 and S_4 as well as the capacitances C_G and C_{DC} are part of the commutation loop. For a power flow of the opposite direction, the polarity of change in current di/dt is switched which results into the same commutation cell. The commutation mesh for the boost case of a negative grid voltage V_G is analogous over the switch S_2.

3.2.2 Commutation for Boost Case of Positive Grid Voltage

In order to better understand the commutation for the boost case of a positive grid voltage, the circuit displayed in Figure 3.1 is further investigated. As shown in Table 3.1, the commutating

switches for this operation case are S_1 and S_4. The switches S_2 and S_3 are permanently off during this mode. The conducting current in the switches, the DC capacitor, the grid capacitor and the inductances L_1 and L_2 are measured during the commutation events. Furthermore, the power flow as well as the capacitors voltages are measured. The modulation index is reduced by 0.5% to achieve a power flow from the grid to the DC side. This resembles an application in which the ESS is charged by the power grid. The measurements obtained by simulation are shown in Figure 3.9.

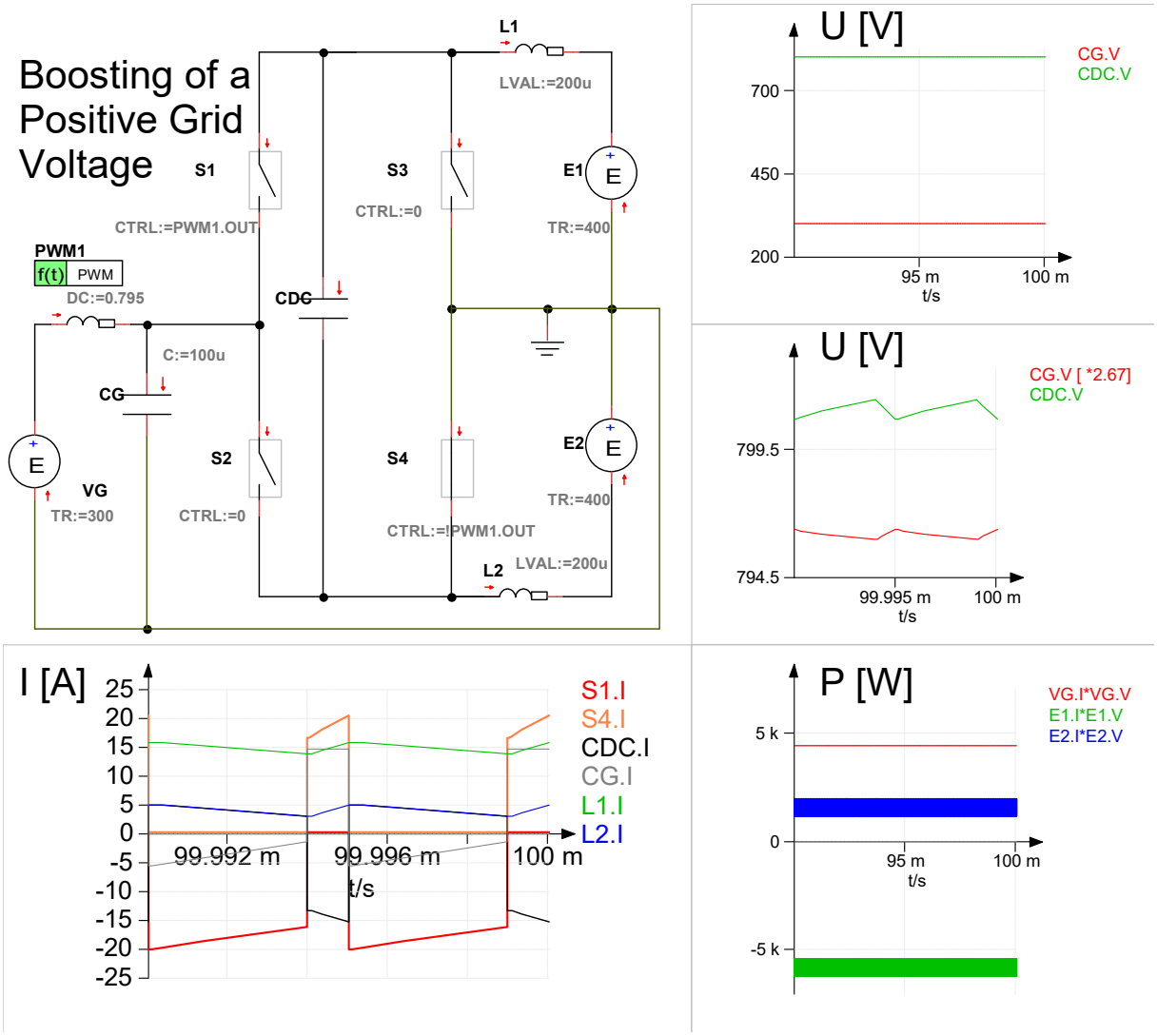

Figure 3.9: Simulation of Boost Case for Positive Grid Voltage with Power Flow into the Grid.

In this DC/DC simulation the grid voltage is set to $V_G = 300V$ and the DC voltage is set to $V_{DC} = 800V$. This simulation resembles an operation in mode M_1 depicted in Figure 3.2. In this mode the sinusoidal grid voltage V_G is positive but lower than the positive DC voltage $V_DC/2$ and thus needs to be boosted to connect the grid and the ESS. Both capacitances have an approximately constant voltage throughout the commutation phases. Assuming the transients have subsided, in the initial moment of a commutation the grid capacitance is charged to $C_G = 300V$ and the DC capacitance is charged to $C_{DC} = 800V$. The current through the in-

ductors L_1 and L_2 is nearly constant, too. The current i_{L1} ripples around $15A$ while the current i_{L2} ripples around $5A$. Charging and discharging of the grid capacitance C_G and the DC-link capacitance C_{DC} is synchronous to the commutation of the switches S_1 and S_4.

When the switch S_1 is closed, the DC-link capacitor C_{DC} is charged while the grid capacitance C_G discharges. The current through both inductances L_1 and L_2 decreases. This can be seen in Figure 3.9 in the voltage plot of the capacitances CG and CDC but also in the current plot which shows the current of the DC capacitance $CDC.I$ being positive while the current of the grid capacitance $CG.I$ being negative. The current splits into both paths and conducts through both inductances L_1 and L_2 to the DC side.

When the switches commute and S_4 conducts while S_1 is open, the DC-link capacitor C_{DC} discharges while the grid capacitance C_G is charged. The current through both inductances L_1 and L_2 is positive and increases. This can be seen in Figure 3.9 in the voltage plot of the capacitances CG and CDC but also in the current plot which shows the current of the DC capacitance $CDC.I$ being negative and the current of the grid capacitance $CG.I$ being positive. The current splits into two paths and conducts through both inductances L_1 and L_2 to the DC side. The direction and the path of the conducting currents is illustrated in Figure 3.10 for the two cases of S_1 or S_4 being the conducting switch.

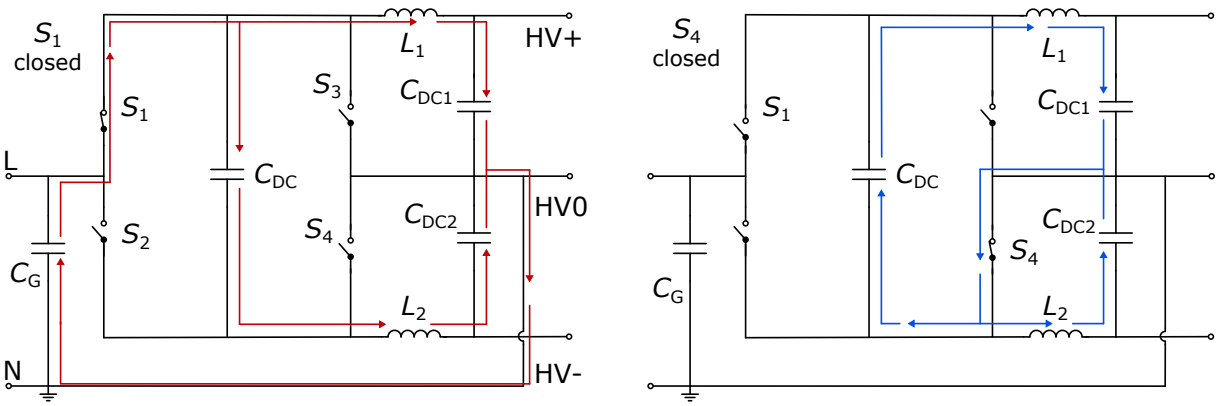

Figure 3.10: Current Direction and Path for Commutation Phases in Boost Case of Positive Grid Voltage.

This is valid for a power flow from the AC grid side to the DC ESS side or in other words a modulation index smaller than m_0 described in Equation 3.9. This can also be seen in Figure 3.9 which shows that the power of the grid side has a positive value of approximately $5kW$ and the positive DC side power being approximately the negative value of the grid side $-5kW$. Furthermore it can be seen that there is an additional positive power flow from the negative DC side. In case the power flow is from the ESS into the AC grid, the all currents conduct towards the opposite directions and consequently the charging and discharging of the capacitances is inverted.

Commutation Loop Boost Operation

In order to determine the commutation loop, the change of current di/dt of the measurements of Figure 3.9 is visualized in Figure 3.11. Both inductances are conducting current which can be separated according to the superposition principle and investigated individually.

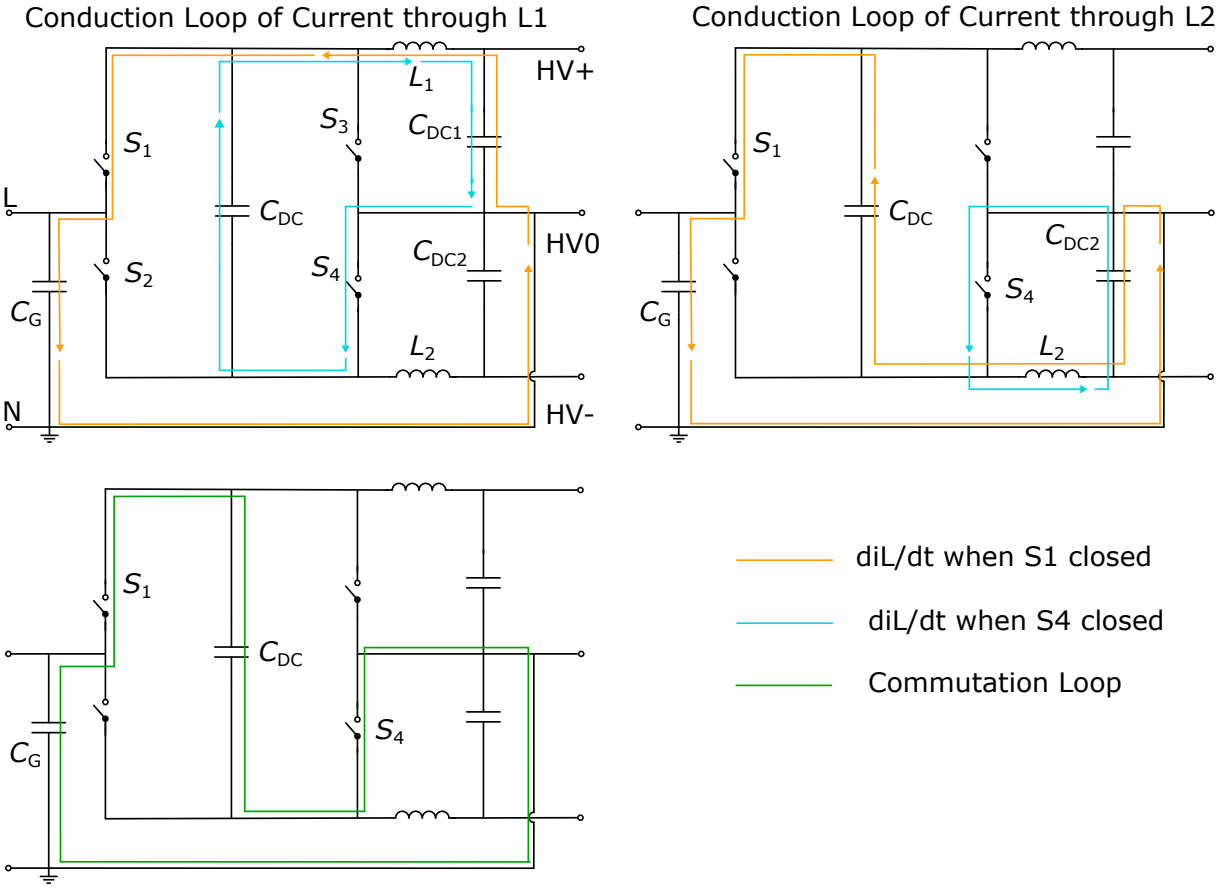

Figure 3.11: Commutation Loop for Boost Case of a Positive Grid Voltage.

In Figure 3.9 it can be seen that the change in current di/dt through both inductances L_1 and L_2 is negative for the switch S_1 being active. When S_4 is active, the change in current through both inductances diL_1/dt and diL_2/dt is positive. Similarly, the change in current di/dt through the capacitances and the switches is determined and visualized in Figure 3.11. Only the branches of the circuit in which the current conducts only in one of each switching states are part of the commutation loop. It can be seen that the switches S_1 and S_4 as well as the capacitances C_G and C_{DC} are part of the commutation loop. For a power flow of the opposite direction, the polarity of change in current di/dt is switched which results into the same commutation cell.

The commutation mesh for the boost case of a negative grid voltage V_G is analogous over the switch S_2 and S_3.

3.3 Blocking Voltages in Operation Modes

After calculation of the modulation index, the properties of the eight operating modes $M_1a, .., M_4a$ and $M_1b, .., M_4b$ displayed in Table 3.2 are further investigated. The eight modes of operation are bucking and boosting of positive and negative grid voltage with power flow in either direction. All eight operation modes are required when connecting a sinusoidal AC grid to a steady DC ESS, assuming that the peak of the AC voltage $V_{\hat{G}}$ is larger than the battery voltage V_{DC}. In order to better understand the functionality of the topology, a DC/DC simulation of the eight operating modes is done.

3.3.1 Bucking of a Positive Grid Voltage

In order to buck a grid voltage of $V_G = 250V$ to a DC voltage of $V_1 = 180V$ the switches S_1 and S_3 are commutating while S_2 and S_4 are permanently turned off. The modulation index m is calculated as shown in Section 3.1.2. When the modulation index is decreased, the topology achieves a power flow into the AC grid while increasing the modulation index results in a power flow from the AC grid to the DC ESS. In the simulation, the modulation index is increased by 0.1%. The resulting voltages across the ideal switches are shown in Figure 3.12.

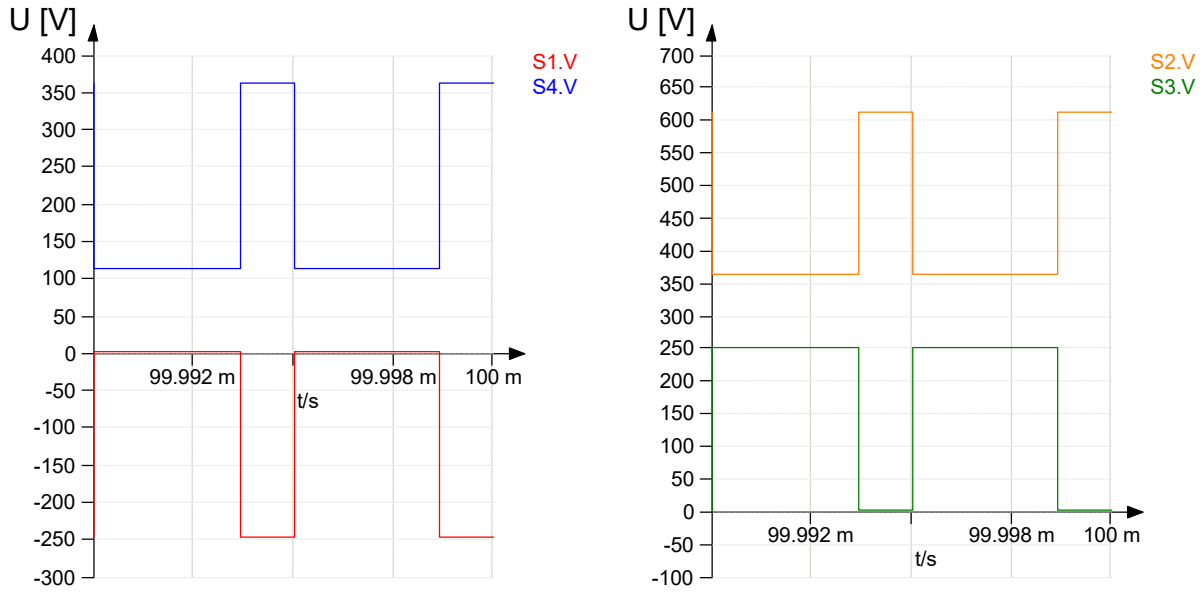

Figure 3.12: Blocked Voltages of Ideal Switches S1, S2, S3 and S4 in Case of Bucking a Positive Grid Voltage.

It can be seen from Figure 3.13, that the voltage across S_1 is either 0 or $-|V_G|$. The voltage across S_2 switches between $V_{DC} + |V_G|$ and V_{DC}. The voltage across S_3 is alternating between 0 and $|V_G|$. The voltage across S_4 is switching from $V_{DC} - |V_G|$ to V_{DC} The voltage across the inductors L_1 and L_2 are identical which results in the same ripple current.

Further simulations with varying grid side and DC side voltages to investigate the DC-DC properties of the topology show, that in case of the DC voltage V_{DC} being smaller than the AC voltage V_G, the switches S_3 and S_4 need to block a negative voltage. This would violate the

condition set in Equation 3.1 and results in the rule displayed in Equation 3.10.

$$\left|\hat{V_G}\right| < V_{DC} \tag{3.10}$$

3.3.2 Boosting of a Positive Grid Voltage

In order to boost a grid voltage of $V_G = 300V$ to a DC voltage of $V_1 = 400V$ the switches S_1 and S_4 are commutating while S_2 and S_3 are permanently turned off. The modulation index m_0 is calculated as shown in Section 3.1.3. When the modulation index is increased, the topology achieves a power flow into the AC grid while decreasing the modulation index results in a power flow into the opposite direction from the AC grid to the DC ESS. In the simulation, the modulation index is reduced by 0.5%. The resulting voltages across the ideal switches in the simulation are shown in Figure 3.1.

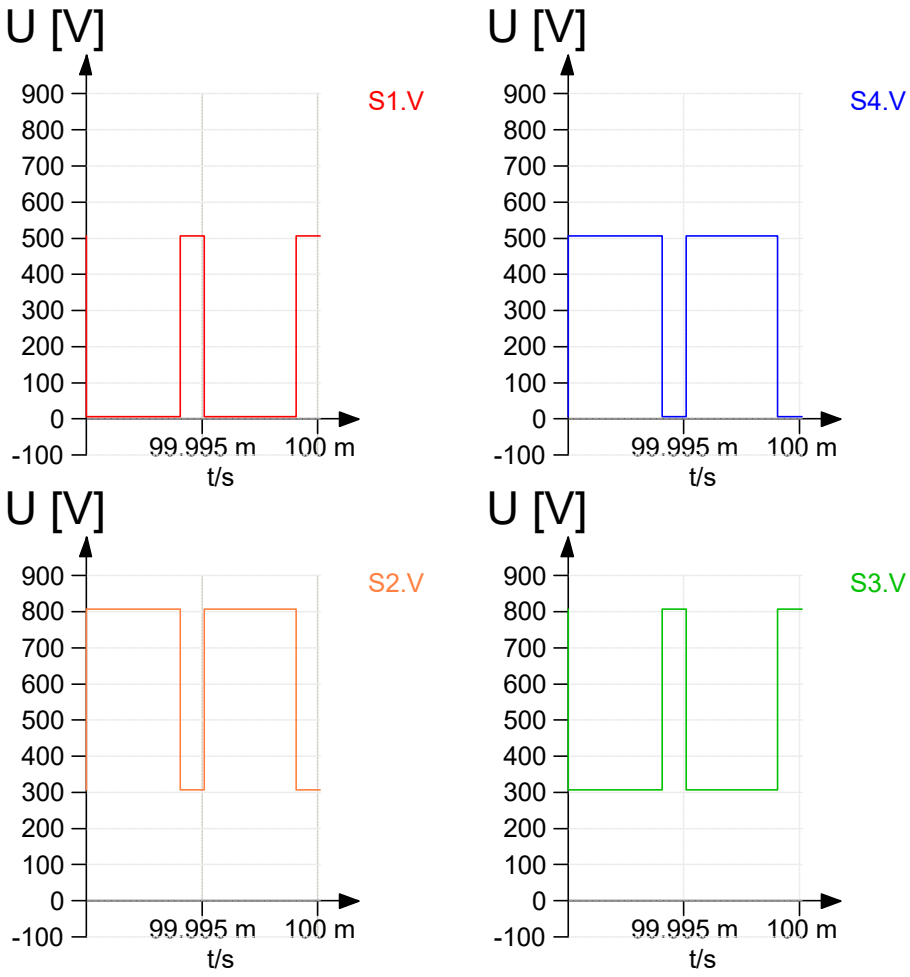

Figure 3.13: Blocked Voltages of Ideal Switches S1, S2, S3 and S4 in Case of Boosting a Positive Grid Voltage.

It can be seen from Figure 3.13, that the voltage across S_1 is either 0 or $V_{DC} - |V_G|$. The voltage across S_2 and S_3 switches between V_{DC} and V_G. The voltage across S_4 alternates from 0 to $V_{DC} - |V_G|$. The voltage across the inductors L_1 and L_2 are identical which results in the same ripple current. The results are summarized in Subsection 2.2.3.

3.3.3 Summary of Switches Blocking Voltages

Simulations of the buck and boost case for a negative grid voltage V_G yield the same values of blocking voltages for the respective other switch, S_1 to S_2, S_3 to S_4 and vice versa. The results of all four individual simulation cases are summarized in the following Table 3.4.

Table 3.4: Switch Voltages and Modulation Index of Different Operation Modes.

	Voltage of S_1 and S_2	Voltage of S_3 and S_4	Modulation Index
Boost	0 & $V_{DC} - \lvert V_G \rvert$	0 & $V_{DC} - \lvert V_G \rvert$	$\underline{V_{DC}/2}$
$\lvert V_G \rvert < V_{DC}/2$	V_{DC} & $+\lvert V_G \rvert$	V_{DC} & $+\lvert V_G \rvert$	$V_{DC} - \lvert V_G \rvert$
Buck	0 & $-\lvert V_G \rvert$	0 & $+\lvert V_G \rvert$	$\underline{V_{DC}/2}$
$\lvert V_G \rvert > V_{DC}/2$	$V_{DC} + \lvert V_G \rvert$ & V_{DC}	V_{DC} & $V_{DC} - \lvert V_G \rvert$	$\lvert V_G \rvert$

As seen in Table 3.4, in the buck case the switches S_1 and S_2 need to block between the negative value of the voltage $|V_G|$ as well as the positive voltage $V_{DC} + |V_G|$. Hence, the transistors S_1 and S_2 need to have bidirectional voltage blocking properties. The switches S_3 and S_4 need to block between a minimum voltage of $0V$ and a maximum voltage of V_{DC}. In the boost case the switches S_1 and S_2 need to block between a minimum voltage of $0V$ and the positive voltage V_{DC}. The switches S_3 and S_4 need to block between a minimum voltage of $0V$ and a maximum voltage of V_{DC}. These voltage boundaries are critical when assembling a physical inverter as the components, especially the semiconductors, have maximum voltage blocking capabilities which limit the voltages V_G and V_{DC}. This is elaborated in Section 4.3.

3.4 Full Sine Wave Simulation

The preceding findings are now brought together in simulation of a full sine wave. Therefore, the switches S_1 and S_2 are now modulated as bidirectional switches by anti serial connection of two switches which results in S_{1a}, S_{1b}, S_{2a} and S_{2b}. They are extended with an internal body diode and output capacitances of $C_{oss} = 500pF$. The dead time between commutation is taken into account.

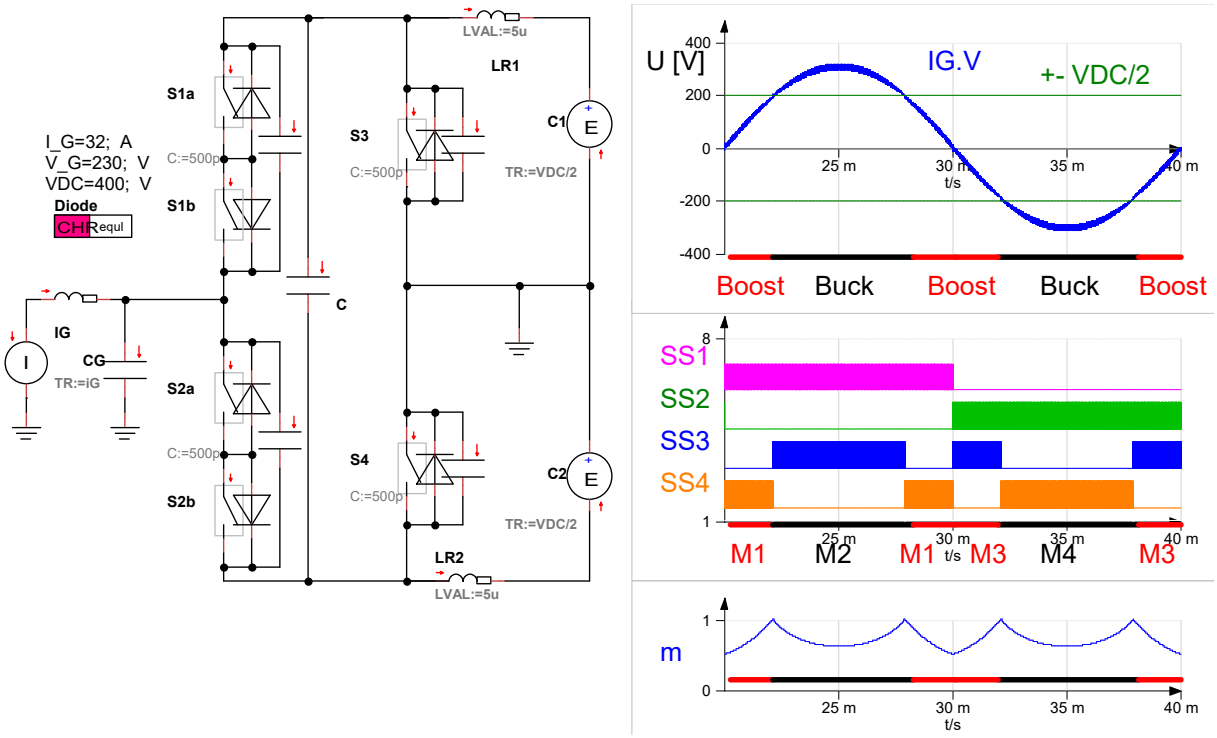

Figure 3.14: Simulation of Full Sine Wave.

Figure 3.14 shows the simulation in Portunus and the results. A sine period is divided in boost and buck operation depending on the grid voltage and DC side voltage as described in Section 3.1 and shown in Figure 3.2. The four operation modes $M_1, .., M_4$ are displayed in Figure 3.14. The active switches in each phase can be seen as they are displayed in Table 3.1. The course of the modulation index m for a grid to ESS coupling without power flow is displayed as it is shown in Section 3.1.3 and Section 3.1.2. It can be seen that the duty cycle does not fall below 50% for the switches S_1 and S_2. Reason for this is that other values for m would lead to blocking voltages of the switches with undesired polarity. Therefore, the maximum AC voltage depends on the DC voltage $VG_{max} = V_{DC}$. The mean of the modulation index is $m_{mean} = 0.714$.

4 Design and Assembly of Topology

This chapter begins with an introduction of the design tool Altium Designer used in this project to design the PCB. The gate driver circuit and its function is shown. The components used in the design and assembly of the prototype are presented.

4.1 Altium Designer Project Structure

Altium Designer is a Electronic System Design (ESD) program released in 2005 to develop PCBs. ESD is a subarea of Computer Aided Design (CAD) which focuses on electrical engineering rather than mechanical construction. The major functions of Altium are circuit implementation in so called schematics and PCB layout design based on the schematic. The layout design can be extended to three dimensional modelling by importing or creating 3D models of the specific components, often offered by the manufacturers. Each electrical component is represented by a symbol in the schematic, a footprint for the 2D PCB layout design and a 3D model mainly for illustration purpose. The footprint resembles the actual physical component and the connections to the top layer of the PCB. A helpful feature of the program is the function of visualising the electrical potential of the component connectors, illustrating which net they are connected to according to the previously designed schematic.

Modular design is a useful technique in PCB design because it enables easy understanding of complex contexts as it promotes clarity and interconnection of different units. All modular circuits may be designed on a dedicated schematic in Altium and then be unified in a main schematic which includes the sub-schematics. Taking advantage of this function, clarity can be improved. The PCB layout of this thesis is based on a previously existing On Board Charger (OBC) project of Fraunhofer IZM designed by Oleg Zeiter [46]. This simplifies the process of setting up the fundamental properties such as layer functions and labeling. The topology of the active power circuit is fully designed from scratch while other modules such as the Controller Area Network (CAN) unit, the connection to the control unit, the measurement units and the power supply unit are adopted. Thereby, in later stages of the EnerConnect project the Altium project design files which are created over the course of this thesis may be altered and reused to a large extend, e.g. when implementing closed-loop control. The required space and the required circuit units themselves are already existing and located on the PCB and only need to be connected to the high power circuit, therefore reducing work as a design is reused. This is modular approach is illustrated in Figure 4.1.

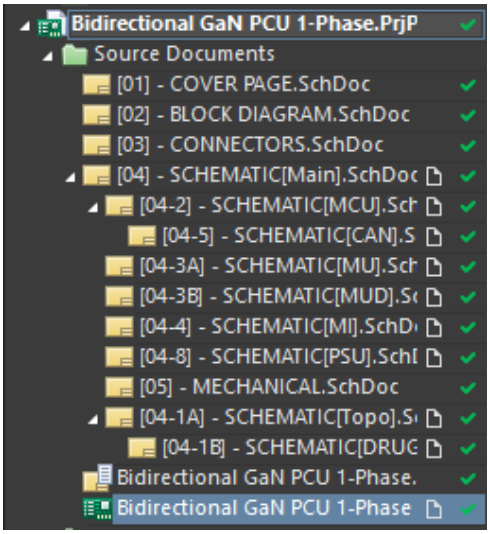

Figure 4.1: Modular Design Approach in the Altium Project.

Figure 4.1 shows the typical structure of an Altium project file at Fraunhofer IZM. It can be seen that the project includes a cover page, a block diagram, connectors and the main schematic. The main schematic is composed of multiple other schematics which each represent a unit, e.g. the gate driver unit. The sub-schematics can be embedded in the main file and also interchanged conveniently between projects to reduce development time. For file sharing and simultaneous development in the same project, Altium project can easily be shared with GitLab [47]. GitHub enables convenient administration of repositories which contain the project files. Functions such as branching or merging different repositories can be of use in the development phases of multiple projects in a group with multiple engineers. Repositories can be cloned and saved locally which is also described as "pull request". After local changes are made, the updated version can be "pushed" and shared. An advantage of GitHub is the automated version control by continuously pushing and pulling the repositories throughout the project phase.

4.1.1 Implementation of Topology

When implementing the simplified topology of the single phase, single stage AC-DC inverter to experimentally investigate the properties and feasibility of the proposed novel topology, the circuit and the associated components need to be implemented in Altium. Figure 4.2 displays the schematic of the circuit introduced in Figure 3.1 in Chapter 3 implemented in Altium. It is vertically mirrored as the DC side and AC side are interchanged.

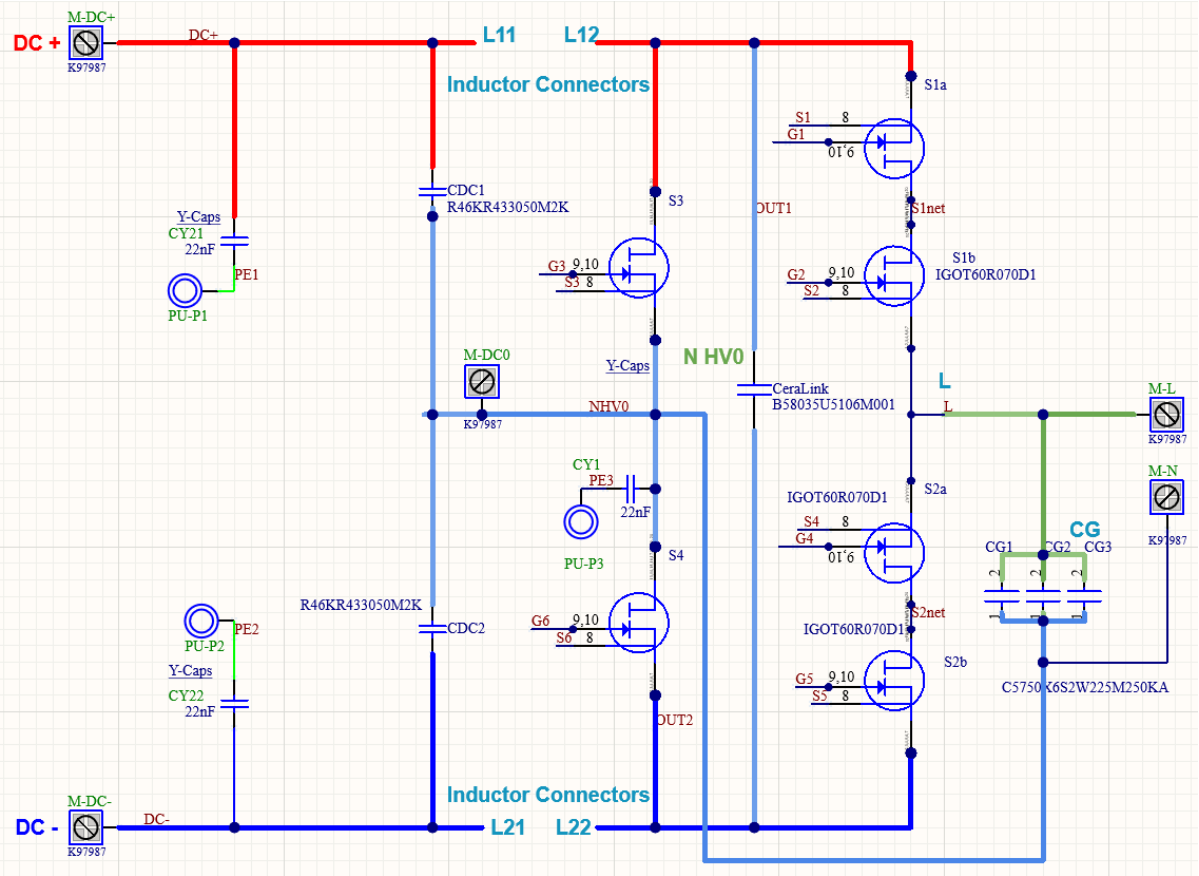

Figure 4.2: Schematic of the Altium Project.

In Figure 4.2 the previously ideal switches S_1 and S_2 are realized by the anti-serial configuration of two unidirectional switches S_{1a} and S_{1b} as well as S_{2a} and S_{2b} respectively as described in Section 2.2.3. The Circuit shows the GaN HEMT devices, the capacitances, connection for voltage sources on the DC and AC side as well as space for the inductors. Furthermore filtering capacitances and connections to the Protected Earth (PE) are integrated. Each component consists of a symbol as well as a footprint which are uploaded in the Fraunhofer IZM cloud so they can be used throughout the projects. It is important that the layer stack of all component models is consistent and identical to the layer stack of the PCB. Otherwise errors in layout phase or the production files may arise.

4.1.2 Proposed Low Inductive Commutation Cell

After the circuit and the associated components are implemented, the layout of the physical PCB employing the circuit is done. The parasitic inductance caused by the layout of the circuit is to be minimized to optimize performance. Therefore, the area spanned by the commutation mesh is minimized. This is achieved by the following topology displayed in Figure 4.3.

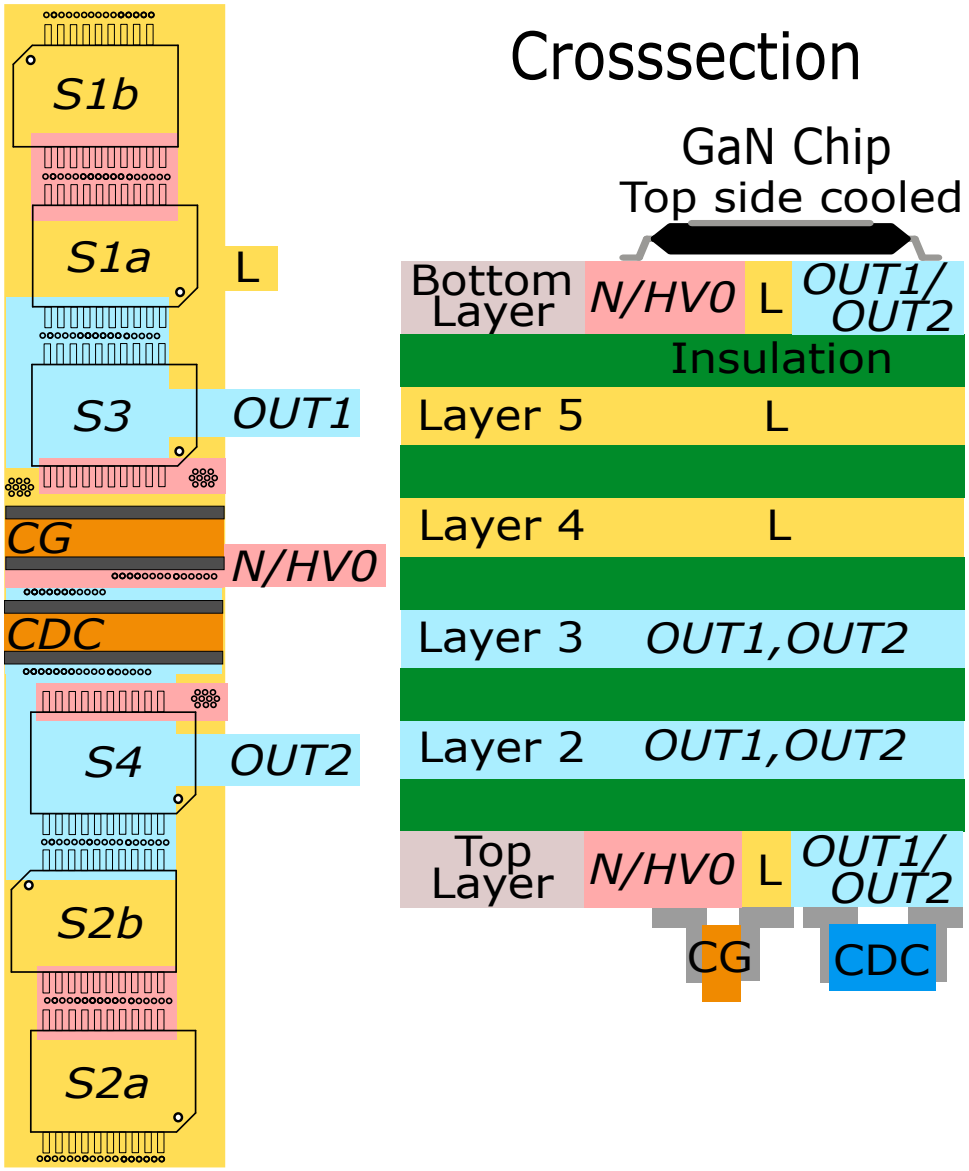

Figure 4.3: Proposed Low Inductive Commutation Cell.

All transistors are connected to the same side but to different potentials labeled $L, OUT1, OUT2$ and $N/HV0$ which are on top of each other in the layer stack. The according potential is connected to the side of the transistors with vias. Because there is no commutation between the switches S_1 and S_2, they are placed with maximum distance to one another. The forward conductor and the pertaining return path are placed as close to one another as possible resulting in a multi layer topology. The capacitances C_G and C_{DC} are on the opposing side as the semiconductors to minimize distance and to not interfere with the heatsink of the semiconductors. A connection between the top side and the bottom side of a PCB is realized with a via. A via is realized by plating small drilled hole through the full layer stack with conducting material such as copper to enable an electrical connection through the PCB including the insulating layers. In favour of visualisation, the switches S_3 and S_4 have a rather large distance while in the actual layout they can be placed closer to one another. However, the vias connecting the layers need to fit between the connections to the respective switches and capacitors. The areas labeled $OUT1$

and $OUT2$ describe potentials which heavily change their voltage value. Capacitive coupling between these unsteady potentials and the other, more steady nets need to be kept as low as possible to reduce EMI. This contradicts the premise to minimize the parasitic inductance. To solve the problem with a compromise, two adjacent layers can be used for either potential to decrease the width of the copper tracks without reduction of the current carrying capability. The capacitances are placed on the top layer $Layer_1$. OUT_1 and OUT_2 are placed on the layers $Layer_2$ and $Layer_3$, the calm net L is on layers $Layer_4$ and $Layer_5$.
All layers of the Altium design are shown in detail in Appendix A.

4.1.3 GaN HEMT and Gate Driver Circuit

To reduce the total effort it is decided to supplement the remaining MOSFET switches with the same GaN devices so that only one gate driver circuit needs to be designed and implemented on the PCB. The unidirectional GaN transistors used in this project are manufactured by Infineon and distributed under the label IGOT60R070D1 [48]. They are characterized by a rated maximum blocking voltage of $V_{DS} = 600V$, an on-state resistance of $R_{DS,on} = 70m\Omega$ and a maximum rated current of $I_D = 60A$.

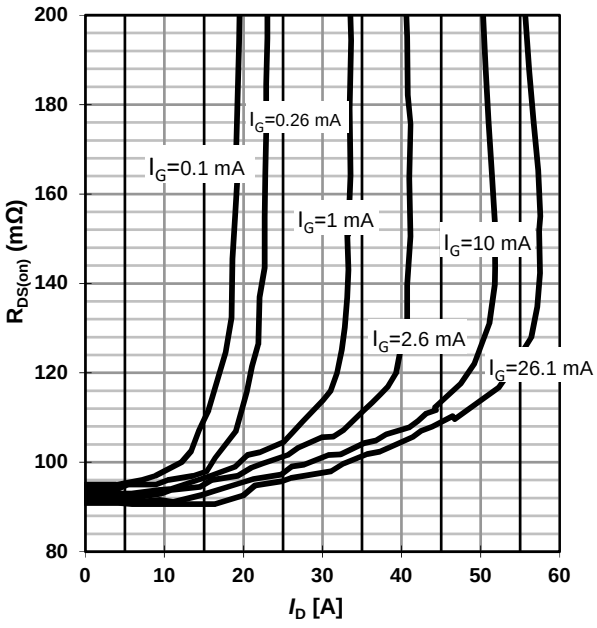

Figure 4.4: Drain Source Resistance of Transistor depending on Drain Current for different Gate Currents [48].

Figure 4.4 shows the dependency of the drain source resistance $R_{DS,on}$ on the drain current I_D for different gate currents I_G. It can be seen that the GaN devices are gate injecting transistors which means that they rely on a steady gate current of up to $I_G = 26mA$ to have a low on state resistance $R_{DS,on}$.

The drive circuit implemented in the design and prototype is suitable for the GaN switch and proposed by Infineon in the application note 201702 PL52 012 [32]. The Integrated Circuit (IC) proposed by the application note is also manufactured by Infineon as part of the 1EDI Compact

series and distributed under the label 1EDI20N12AF [49]. It is characterized by an output current of $I_{out} = 4A$ and a propagation delay of $t_{prop} = 120ns$. The IC is the core unit of the gate driver circuit. It consists of an input side which receives the Pulse-Width Modulation (PWM) signal and is powered by a $5\ V$ voltage source and an output side connected to the gate of the GaN semiconductor via auxiliary circuitry. This output side is powered with a $12\ V$ isolated voltage source. This DC/DC converter is manufactured by Murata and distributed under the name MGN1S1212MC as part of the MGN1 Series. It has a rated power of $1\ W$, $12\ V$ input, $12\ V$ output voltage and an output current of $83\ mA$ [50]. The components are summarized in Table 4.1. The gate driver IC and the auxiliary circuitry and the isolated DC/DC converter is shown in Figure 4.5.

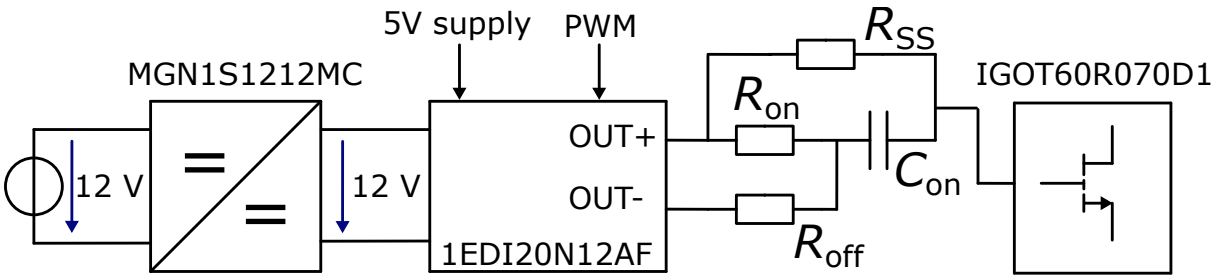

Figure 4.5: Schematic of Gate Driver Circuit.

To drive the transistor, the input capacitance of the transistor C_{iss} needs to be charged and discharged. The higher the gate current I_G to recharge the gate capacitance, the faster the switching transients. Therefore, the target of this circuitry is to provide large peak gate currents to turn the transistor on and off fast at a sufficient steady-state gate current I_{SS} to minimize the on state resistance $R_{DS,on}$ as seen in Figure 4.4. To understand the gate driver circuit it is helpful to simply it which is shown in Figure 4.6.

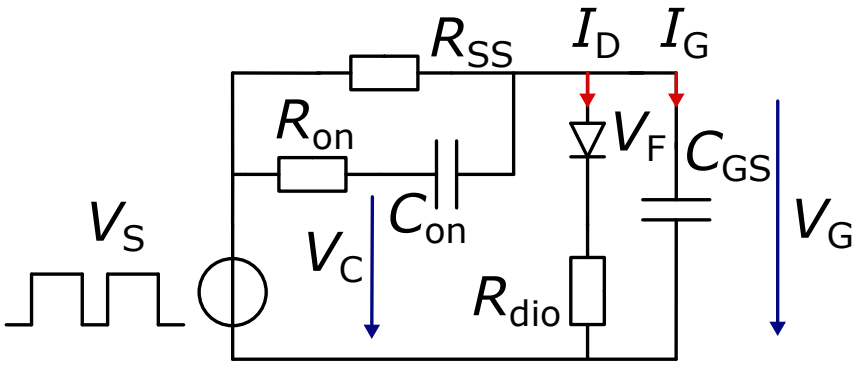

Figure 4.6: Simplified Circuit of the Gate Driver.

In the simplified version the transistor is replaced by a constant capacitance $C_{GS} = 2nF$ in parallel to an ideal diode which has a forward voltage of $3.5V$ and a serial resistance of $R_{dio} = 3\Omega$. This diode represents the internal gate diode of the transistor which is inherent to the structure of the device. A voltage source switching between GND and V_S is connected which represents the step PWM signal to be applied on the gate of the transistor. The capacitance C_{on} is a coupling capacitance and together with the resistor R_{on} these two components represent

the low impedance AC path. A high ohmic resistor $R_{SS} = 500\Omega$ represents the DC path. The circuit is simulated in Portunus and the results are shown in Figure 4.7 and Figure 4.8. In this example, the capacitances C_{GS} and C_{on} are equal. Before the PWM signal rises, the capacitances C_{GS} and C_{on} are both uncharged. V_F is the forward voltage of the internal gate diode which origins from the transistor structure. When the voltage source V_S turns on, the capacitances are both charged until the diode forward voltage $V_F = 3.5V$ is reached and the internal body diode starts conducting a current I_D. The value of the forward voltage $V_F = 3.5V$ is found in the application note [32]. The gate charging current I_G in the parallel branch can be described by Equation 4.1.

$$I_G(t) = \frac{V_S - V_C(t)}{R_{on}} \tag{4.1}$$

Without any diode current I_D the charge in both capacitances are equal. As soon as the diode forward voltage is reached and the diode starts conducting, the gate voltage is clamped to $V_G = 3.5V$ which corresponds to a voltage $V_{Con} = 7V$. The capacitance C_{on} is further charged until $V_C = V_S$ if $V_S > 2 \cdot V_G$. However, if V_S is not large enough, the gate voltage V_G is charged via the capacitive path while the remaining gate charge is provided by the resistor R_{SS}. This behaviour is shown in Figure 4.7.

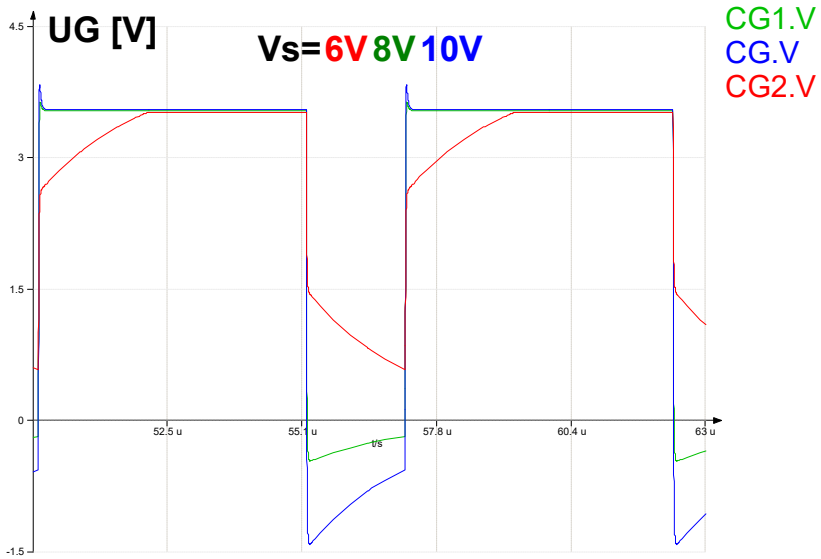

Figure 4.7: Gate Voltage of the Gate Driver Circuit Simulation.

As shown in Figure 4.7 when the source voltage $V_S = 6V$ is too low to fully charge the capacitance C_G via the fast path. The gate voltage V_G instantly rises to $3V$ and is then slowly charged to $3.5V$ via the resistor R_{SS}. Otherwise, if the potential V_S exceeds $7V$, the charge of the capacitance C_G happens faster via the opposing path which can be seen as instantaneous rise of the gate voltage V_G.

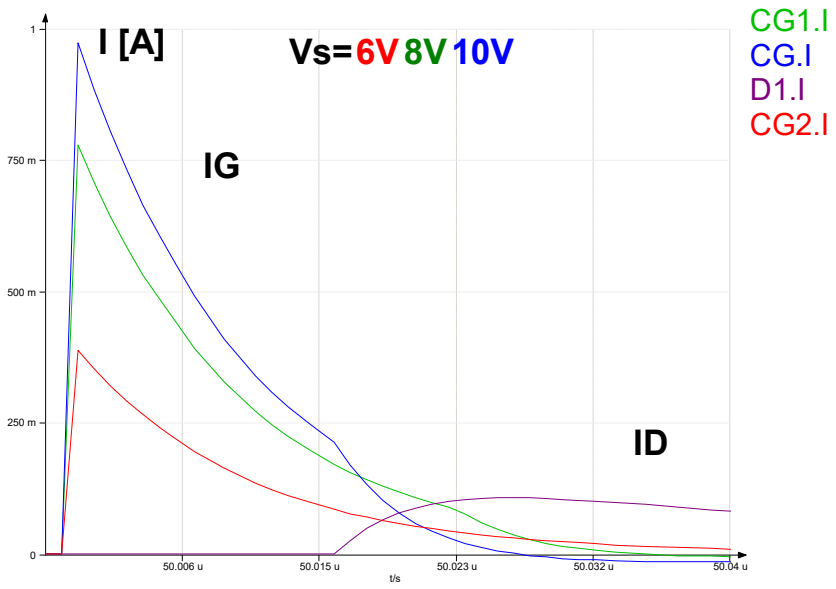

Figure 4.8: Simulation of Gate Driver Gate Current Duringn Switch On.

Figure 4.8 shows the gate current I_G and the diode current I_D. It can be seen that the peak of the gate current I_G is voltage dependent. A large gate current I_G is desirable to reload the transistors input capacitance.

The goal of the gate driver circuit is to provide large peak currents for turn on and turn off at a small steady state current. A fixed gate driver impedance $R_{ss} = R_{on}$ leads to a low ratio between the steady state current and the peak current. In order to obtain a high ratio between the currents, a significant difference in resistance during the transients and the steady on-state is required. This could be achieved by using two separate different driver stages for transients and steady-state with different impedance values and/or supply voltage. However, this results in high hardware effort because integrated drivers for this purpose do not exist. Therefore, Infineon recommends use of the gate-drive concept presented in this section. Here the Ron of the classic drive concept is substituted by an RC network that provides two parallel paths. The small resistor R_{on} is coupled to the gate with the capacitance C_{on} and a much larger resistor R_{ss} provides a direct path. Hereby, the transient current is defined by resistance R_{on}, while R_{ss} determines the steady-state diode current. By a shift of the capacitor C_{on} negative gate-drive levels values can be achieved.

4.2 Assembly of Printed Circuit Board

The circuit is designed on a PCB and ordered from a supplier. The components are ordered separately. The component, the fabricator, the distribution name and if necessary the value is summarized in Table 4.1.

Table 4.1: Components Assembled on the PCB.

Component	Fabricator	Distribution Name	Value
GaN Transistors	Infineon	IGOT60R070D1	-
Gate Driver IC	Infineon	1EDI20N12AF	-
DC/DC Converter	Murata	MGN1S1212MC	$12V/12V$
Grid Capacitance	TDK	C5750X6S2W225M	$2.2\mu F$
DC Capacitance commutation mesh	TDK Ceralink	B58035U5106M001	$10\mu F$
DC-link Capacitance	KEMET	R46KR433050M2K	$3.3\mu F$
Filtering Y-Capacitance	TDK	B32022A3223M189	$22nF$
Inductance $N = 14$ $dCu = 1.8mm$	Kool Mu	3x77351A7	$30\mu H$

The assembly of the PCB is done in the power electronics laboratory of the Fraunhofer IZM. The soldering is done per hand in order so that testing and debugging can be done accompanying. For soldering, a heat plate is used in combination with a hot air soldering as well as a conventional soldering iron. Soldering paste is used as well as solder wire. For debugging purpose, a Tomlov digital microscope is used as well as a FLUKE Multimeter.

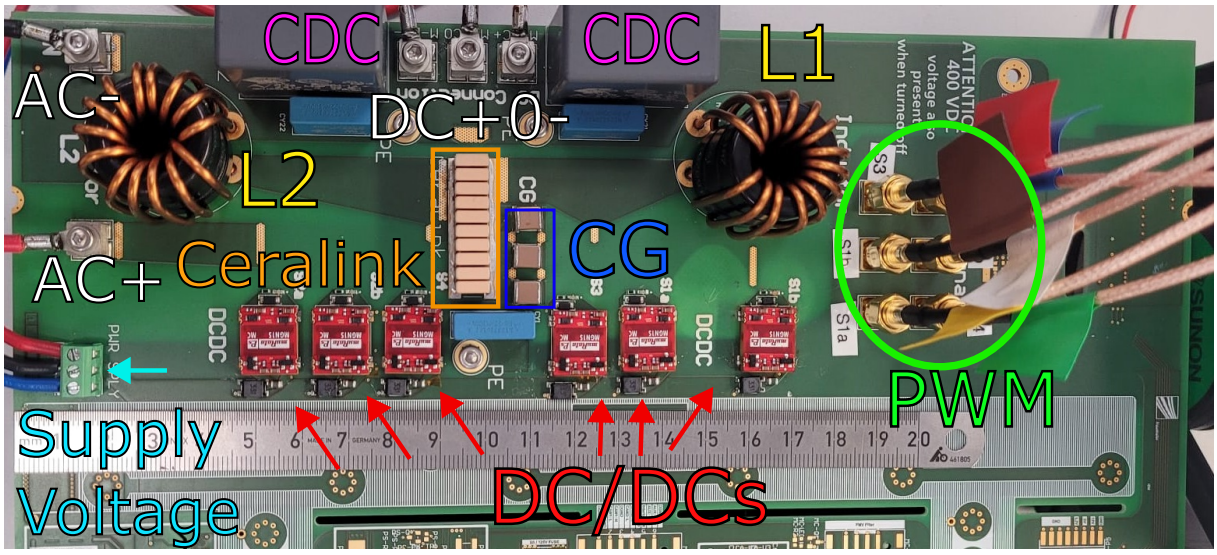

Figure 4.9: Top View of the Device Under Test.

Figure 4.9 shows the top side of the designed and assembled PCB. The connectors of the AC side cables and the DC side are shown. The DC side includes the positive, negative and neutral connection. The DC-link capacitors, the Ceralink capacitance and the grid capacitances are shown. A Ceralink capacitance is used in the commutation loop because of the high current carrying capacity. While other capacitors nominal capacitance is reduced at higher voltages, Ceralink products remain with low impedance. The inductances can be seen as well as the DC/DC

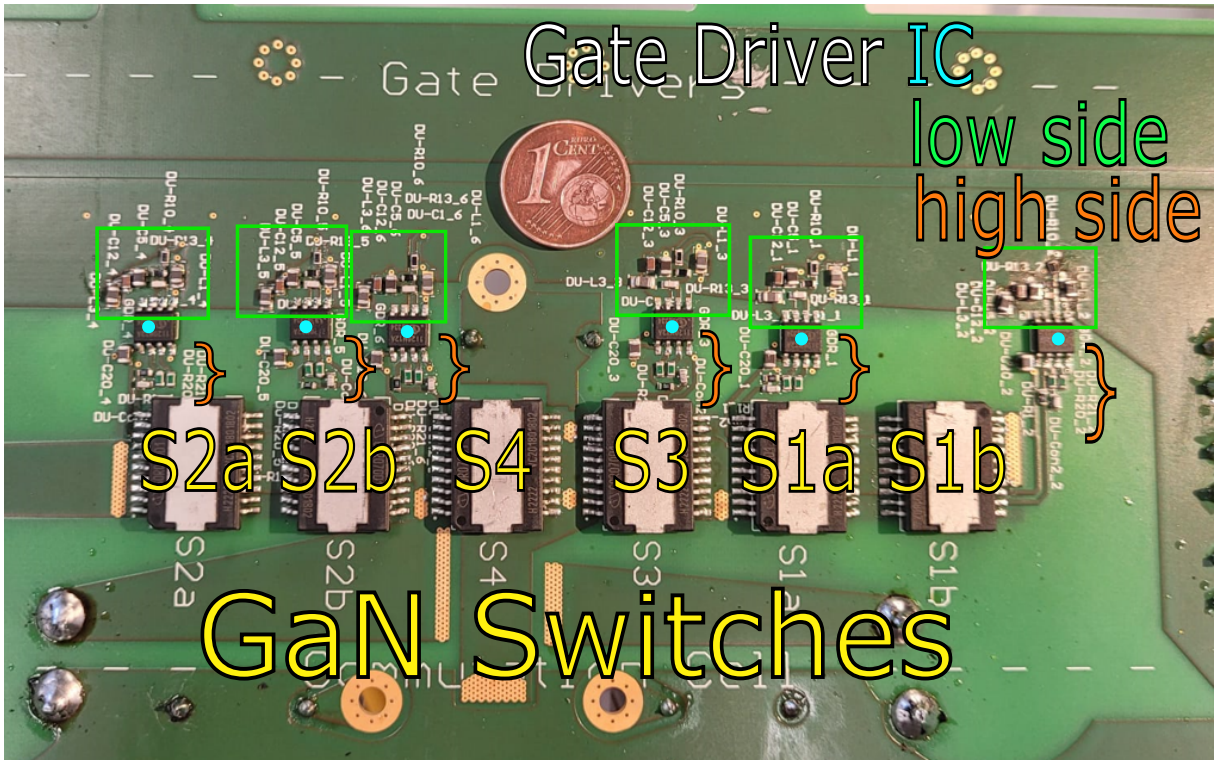

Figure 4.10: Bottom View of the Device Under Test.

Figure 4.10 shows the bottom side of the designed and assembled PCB. The actual assembly process included testing and debugging experiments which are not further elaborated in this thesis.

4.3 Nominal Operating Points of DC-DC Experiment

The designed single phase grid connecting inverter is to be tested for efficiency and functionality. Thereby, the commutation principle applied in simulations can be verified or refuted. The experiments are conducted in the power electronic laboratory of the Fraunhofer IZM under safety precautions. The nominal operating points for the DC-DC experiment are chosen so all commutation modes $M_1, .., M_4$ displayed in Table 3.1 are investigated. As the rated blocking voltage of the physical GaN transistors modulated by the ideal switches S_1 and S_2 is $600\ V$, another condition for the voltages V_G and V_{DC} is set. Additional to the condition described with Equation 3.10, Table 3.4 show that the maximum blocking voltage for the switches S_1 and S_2 is $V_{DC} + |V_G|$. This condition is shown in Equation 4.2.

$$\left|\hat{V_G}\right| + V_{DC} < 600V \tag{4.2}$$

The AC grid voltage V_G can not to be a conventional $230\ V$ rms grid as described in the international standard norm IEC 60038 [51]. This standard grid varies from positive to negative peak voltages of $\sqrt{2} \cdot 230V = 325V$. The first condition described in Equation 3.10 describes that $V_G < V_{DC}$ which would mean $325V < V_{DC}$. However, this results in a direct violation of the second condition described in Equation 4.2. In order to fulfill both rules and investigate the

inverter employing $600\ V$ blocking GaN switches S_1 and $S2$ as well as unidirectional blocking switches S_3 and S_4, the grid voltage V_G is lowered so it has a maximum peak voltage of $\left|\hat{V_G}\right| = 200V$. The DC-voltage can then be set to $V_{DC} = 300V$ resulting in a maximum blocking voltage of $\left|\hat{V_G}\right| + V_{DC} = 500V$ while also fulfilling Equation 3.10. The chosen nominal operating points for the experiments are displayed in Table 4.2

Table 4.2: Nominal Operating Points for DC-DC Experiments.

	V_G	V_{DC}
Boost $0 < V_G$	$100V$	$300V$
Buck $0 < V_G$	$200V$	$300V$
Boost $V_G < 0$	$-100V$	$300V$
Buck $V_G < 0$	$-200V$	$300V$

Voltage sources are used to generate the DC side voltage V_{DC} while the AC side voltage V_G is measured across a resistive load. The PWM signals are generated with a signal generator and applied to the input of the gate drivers IC via coaxial cables and the PCB's SMA connectors. The PWM signals for have a dead time of $t_{dead} = 70ns$ for all experiments conducted. The power dissipation is measured and the efficiency determined.

5 Laboratory Setup and Experimental Results

In this section the setup in the Fraunhofer IZM power laboratory in which the experiments are conducted is described. First, the test to verify the functionality of the gate circuits is described. Then, the low power experiment in which the blocking voltage of the transistors is measured and compared to the simulations is performed. Afterwards, the connection of the heat sink to the transistors and the following high power experiment for efficiency measurement is presented. In Figure 5.1 a schematic of the conducted experiments is shown.

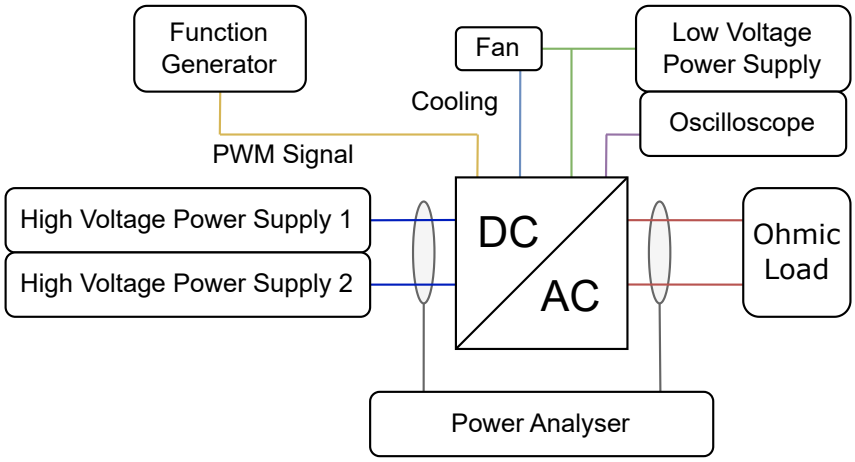

Figure 5.1: Schematic of the Experiments.

An Agilent 33522A function generator is used to apply the PWM signals with a frequencies from 70 kHz to 210 kHz to the IC of the gate driver circuit. A Rohde and Schwarz tripple power supply 7042-5 is used to apply the supply voltage for the low side $V_{S1} = 5\ V$ and the high side $V_{S2}) = 12\ V$ of the IC and the gate driver circuit. Another low voltage power supply is used to power the fan which is used for cooling of the heat sink during the efficiency measurement experiments. A Tektronix MSO58 mixed signal oscilloscope with PMK Bumblebee high voltage differential probes is used to measure the waveform of the gate voltage V_{GS} and the drain source voltage V_{DS}. Two Delta Electronica bidirectional power supplies SM500-CP-90 and SM1500-CP-30 provide the input voltage and power to the DC side of the inverter. An electric load with six phases of each 15 Ω resistance is connected to the output of the AC side of the inverter as variable passive load. A ZES Zimmer precision power analyser LMG671 is used to measure the input voltage V_{in}, input current I_{in} as well as the output voltage V_{out} and the output current I_{out}. The Device Under Test (DUT) is in a protective plastic box as safety measure in case of explosion and against touch.

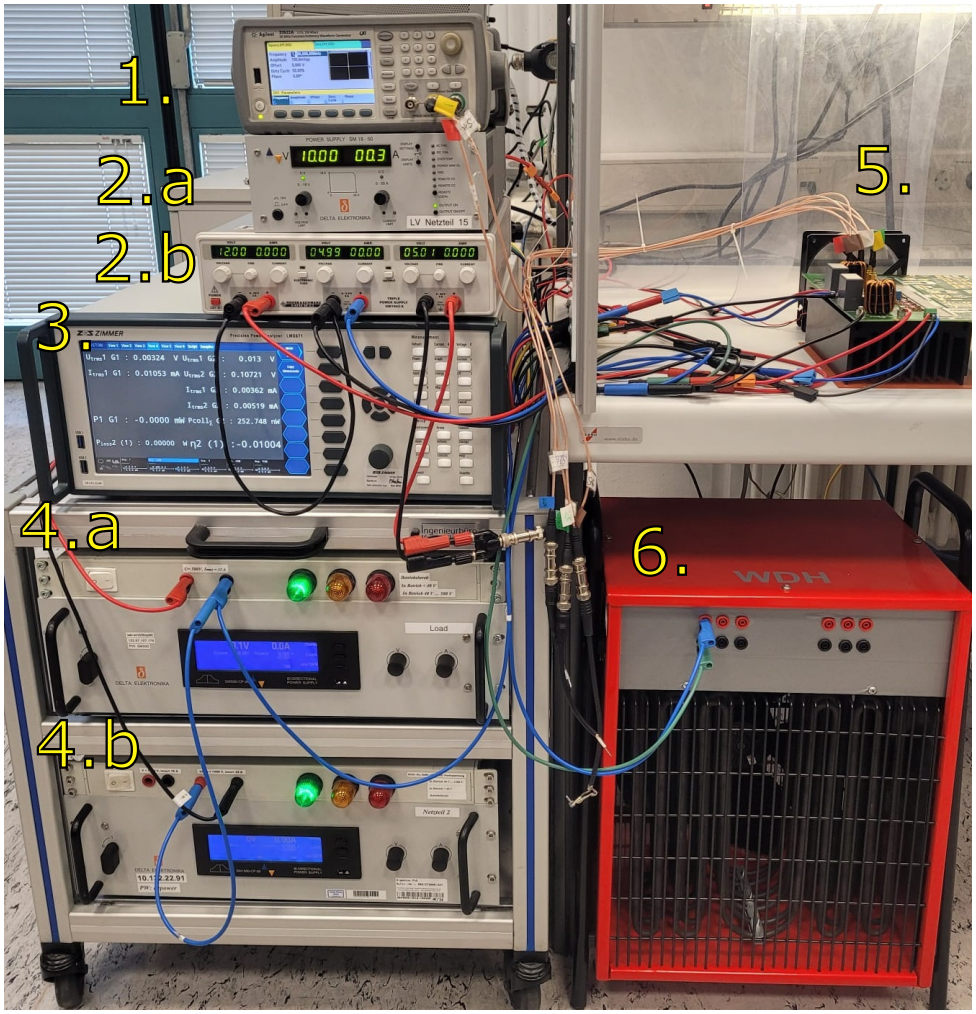

Figure 5.2: Experimental Setup. 1. PWM Generator. 2. Low Voltage Power Supplies. 3. Power Analyser. 4. High Voltage Power Supplies. 5. Device Under Test. 6. Ohmic Load.

Figure 5.2 shows the DUT with the high voltage sources, the power analyzer, the low voltage sources, the load and the function generator. The door of the plastic box used for protection is opened.

5.1 Verification of the Gate Driver Circuit

In order to verify the proper functionality of the gate driver circuit, an experiment to measure the gate source voltage V_{GS} of two switches resulting from a PWM signal is conducted.

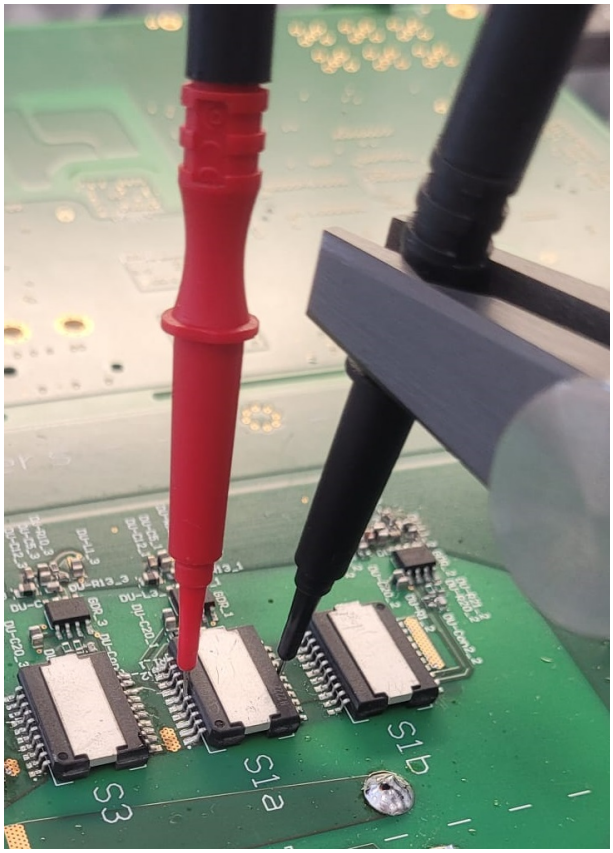

Figure 5.3: Gate Voltage Experiment of the Assembled Inverter.

Figure 5.3 shows the connection of the differential probes with mechanical arms to the transistors to measure the gate voltages V_{GS}.

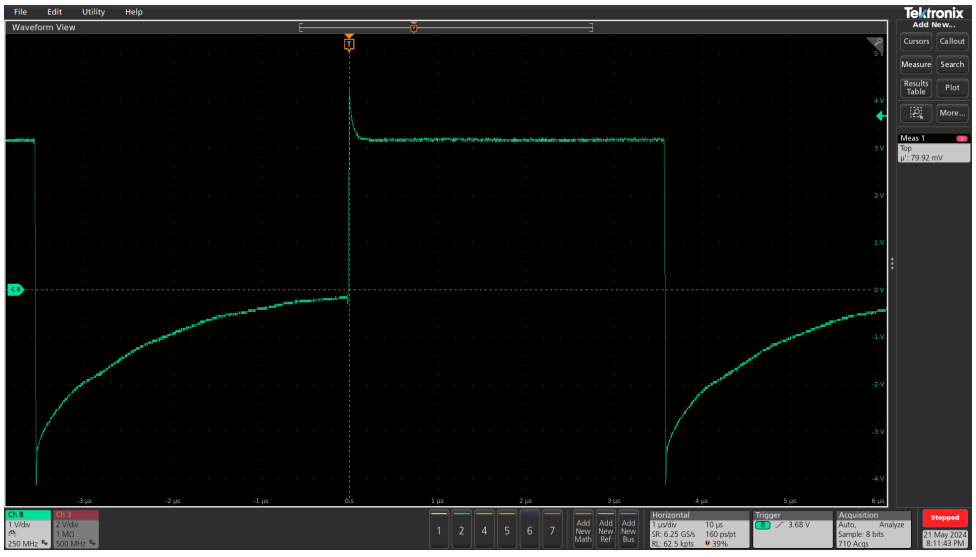

Figure 5.4: Gate Voltage Measurement of the Assembled Inverter.

Figure 5.4 displays the gate voltage measurement of a GaN transistor. The flat of the measured gate voltage $V_G = 3.2\ V$. Simulations in Section 4.1.3 suggest that the flat of the measured gate

voltage should be $V_G = 3.5\ V$. Reasons for a differing gate voltage may be a differing forward voltage of the transistors gate diode in the physical device from the application note value [49].

5.2 Low Power Transistor Voltage Experiment

To verify the simulation results of the novel inverter topology regarding the blocking voltages described Section 3.3.3, an experiment to measure the drain source voltage V_{DS} across the GaN transistors during operation is done. A schematic of the laboratory setup is shown in Figure 5.1. A photograph of the experimental setup is shown in Figure 5.2.

Table 5.1: Power Analyser Measurement for Boosting of a DC Input with a Passive Load.

$V_{AC} =$	$71.80\ V$	$V_{DC1} =$	$49.48\ V$
		$V_{DC2} =$	$49.9\ V$
$I_G =$	$4.75\ V$	$I_{DC1} =$	$7.14\ A$
		$I_{DC2} =$	$1.6\ mA$
$P_G =$	$340.975\ W$	$P_{DC} =$	$353.144\ W$
$P_{loss} =$	$12.17\ W$	$\eta =$	0.9655

Table 5.1 shows the input and output currents, voltages and power measurement. The power flow is from DC to AC, the DC voltage is boosted from $V_{DC1} = 49.48\ V$ to a grid side voltage of $V_{AC} = 71.8\ V$. The power loss $P_{loss} = 12.17\ W$ at an input power of $P_{DC} = 352.144\ W$ results in an efficiency of $\eta = 0.9655$.

The drain source voltage V_{DC} of the transistors is measured with the oscilloscope and differential probes as displayed in Figure 5.3. The measurement results are shown in Figure 5.5.

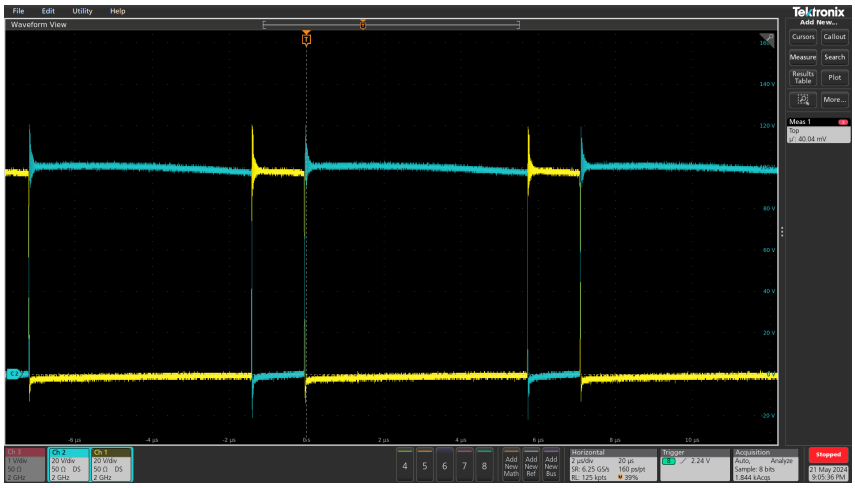

Figure 5.5: Measured Blocked Voltages of Switches S1b and S4 when Boosting a DC Voltage.

It can be seen that the blocked voltage is between 0 and $V_G = 100\ V$ as expected from the simulation results of Table 3.4. There are some oscillations during turn on and turn off. Figure

5.6 shows an enlarged section of the measurements to investigate the turn on and turn off oscillations.

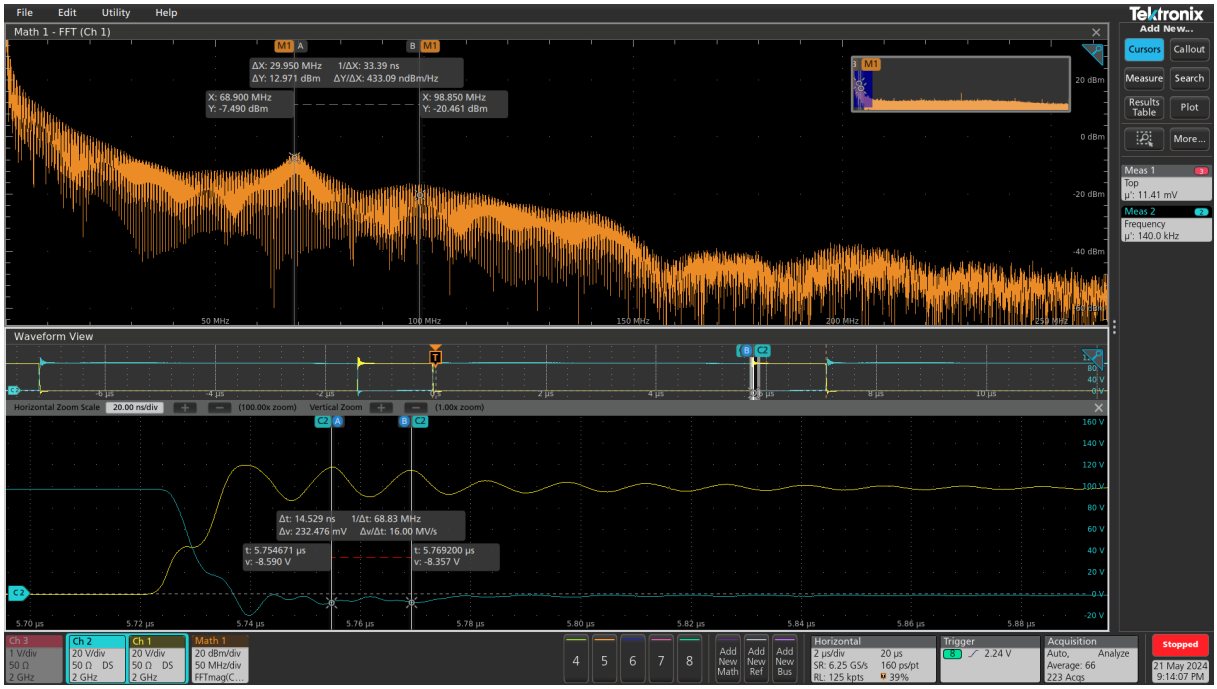

Figure 5.6: Enlarged Section of the Oscillations and Fourier Analysis.

It can be seen from Figure 5.6, that the oscillations have a frequency of roughly 69 MHz. A Fourier analysis of the measured oscillation displayed show, that the frequency of the oscillation is 69 MHz. The spectrum of high frequency components may result from the other capacitances on the board such as the first and second DC capacitances or the filtering Y-capacitance. It is assumed that the oscillation results from the parasitic induction of the commutation loop and the transistors parasitic output capacitance C_{oss}. To further investigate this, a simulation simulation including the parasitic inductance of the commutation loop and the output capacitance C_{oss} is done and shown in Figure 5.7. The Portunus simulation includes the voltage dependency of the transistor output capacitances. Because the commutation mesh includes multiple transistors, multiple output capacitances need to be recharged and also effect the parasitic resonant circuit with the commutation loop inductance.

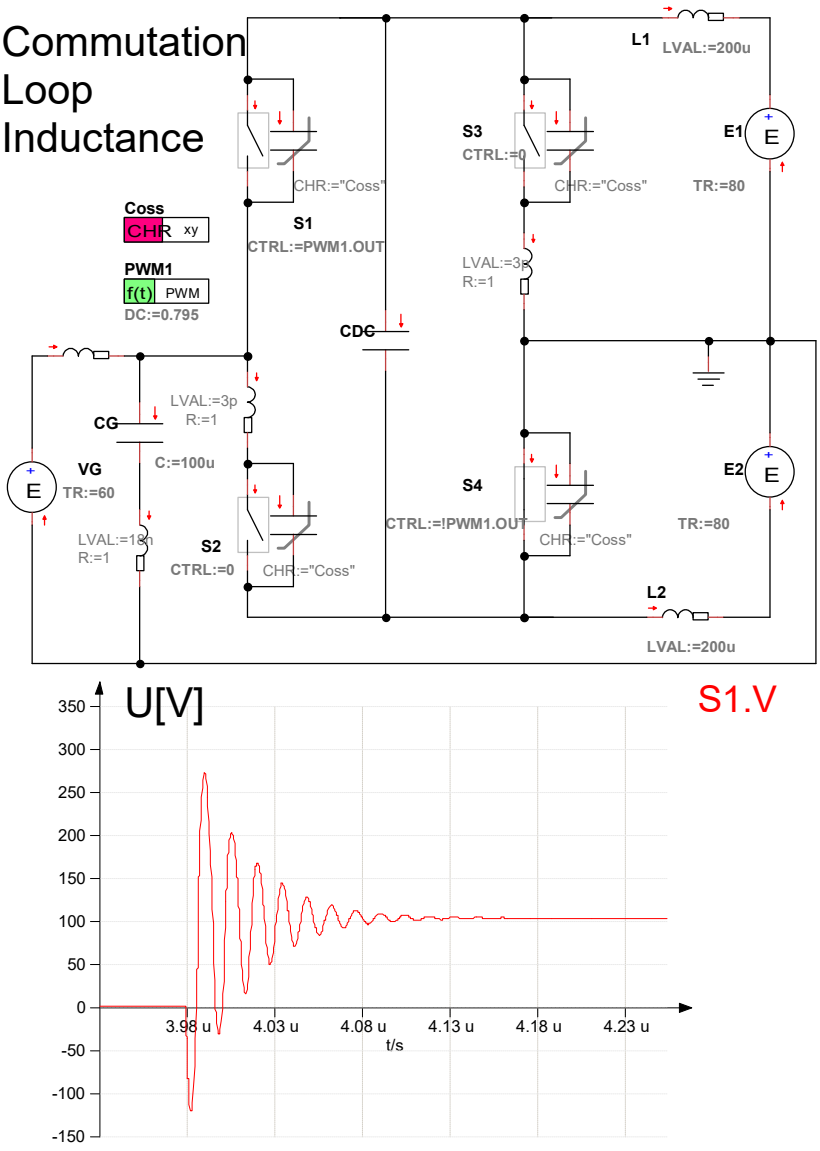

Figure 5.7: Simulation to Determine the Conduction Loop Inductance.

The voltage across switch S_1 is measured and displayed. It can be seen that that the simulated voltage is oscillating. The value for the parasitic inductance of the commutation loop is alternated until the frequency of the simulated voltage matches the oscillation of $68.9\ MHz$ obtained by experiment. It is found that for a commutation loop inductance of $L_{loop} = 18\ nH$, the frequencies are matching.

The peak of the oscillation determines the highest operating voltage because the transistors limited blocking voltage. The blocking voltage across the transistor with the highest voltage stress S_3 is measured in the case of boosting a DC voltage of $V_{DC}/2 = 110\ V$.

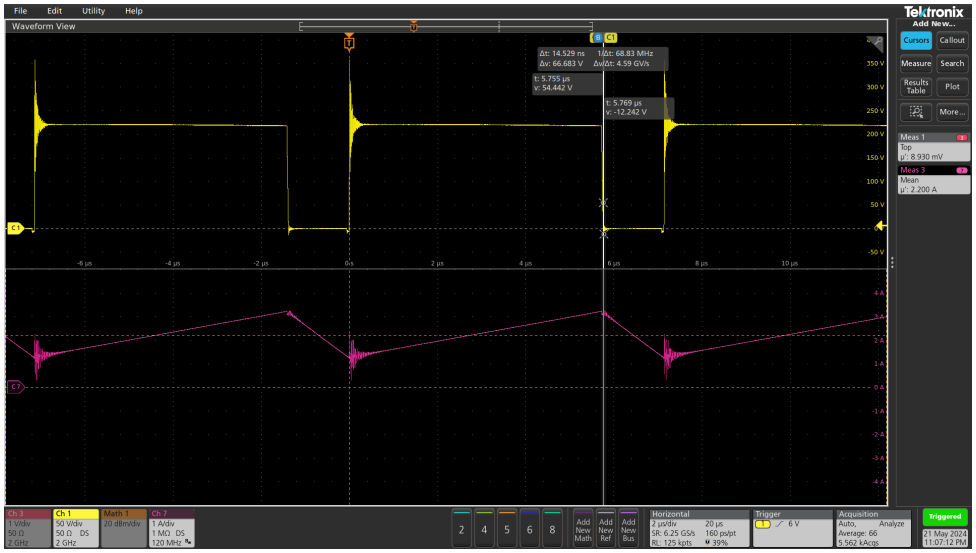

Figure 5.8: Voltage Overshoot for Transistor with Highest Voltage Stress.

Figure 5.8 shows the blocking voltage and the current through an inductance. The current is measured with a current clamp and visualized on the oscilloscope. It matches the simulation. During the switch on moment there are oscillations in the current as well as in the voltage. It can be seen that the peak of the overshoot voltage is approximately $350\ V$ which is roughly factor 1.5 of the steady state blocking voltage. Therefore, the operating points chosen in Section 4.3 are not suitable as they may lead to destruction of the transistors due to the overvoltage spikes caused by oscillation. Sudden increment or turn off of the DC voltage may lead to destruction, too. With a different gate driver circuit connecting the IC to the gate of the transistor, the overvoltage may be reduced.

5.3 High Power Efficiency Experiment

Typically, the efficiency of a bidirectional grid connecting inverter is power dependent [52]. Therefore, in order to determine the optimal working point with highest efficiency a range of measurements are taken with increasing total power P_{tot}. In order to deal with the power dissipation in form of heat, specifically the transistors junction temperature, a heat sink is connected to the GaN semiconductors. The experimental setup is similar to the experiment described in Section 5.2. Figure 5.9 displays the side profile of the DUT with the heat sink attached.

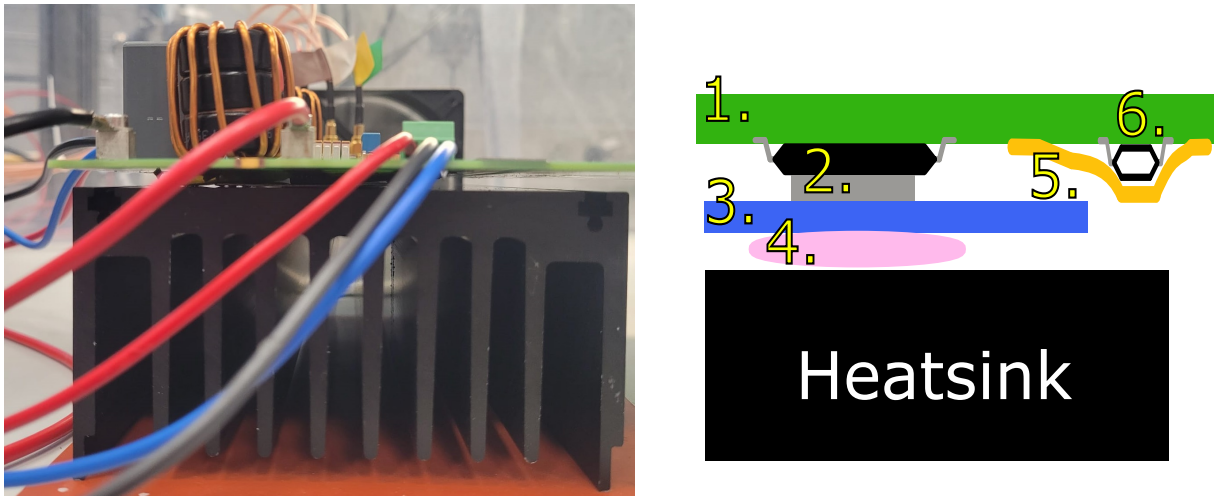

Figure 5.9: Side Profile of the Device Under Test. 1. PCB. 2. Transistor with Device Heatsink. 3. Graphite Foil. 4. Heatpaste. 5. Kapton Foil. 6. Surrounding Example Gate Driver IC.

The heatsink of the chip has the transistors source potential. Therefore, it needs to be electrically isolated from the heatsink which serves as PE potential. A heat conducting graphite foil is connected to the transistor's heat sinks with the adhesive side. The adhesive side of the graphite foil is tested beforehand and a dielectric strength of $4\ kV$ is determined. Kapton, an electrically isolating, heat resistant polyimide film is used to isolate the circuitry on the PCB surrounding the transistors against possible accidental connection to the PE potential which extends to the opposite side of the graphite foil. Additionally, heat conducting paste is used between the aluminium heatsink and the graphite foil to ensure that there is no air gap between graphite foil and heatsink. The heatsink is connected to the PCB by five screws to press the board and the heatsink together. A fan is used to create an air stream which cools the heatsink during the experiment. A FLIR thermal camera is used to monitor the temperature of the transistors. Figure 5.10 shows the thermal image captured by the camera.

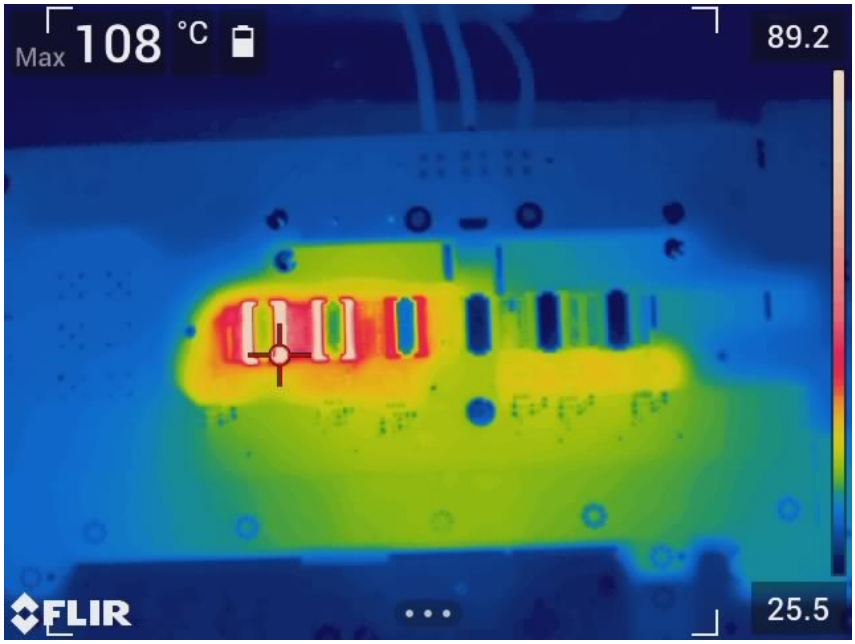

Figure 5.10: Heat Monitoring of Thermal Camera.

It can be seen from Figure 5.10 that the temperature of the transistor package is at $108° \, C$. This is captured at an operating point with a power loss of $P_{loss} = 32.54 \, W$. The maximum junction temperature allowed to the data sheet is $150° \, C$. As the transistors are located between heatsink and PCB they can not be measured directly when the heatsink is connected. The heat conduction through the PCB is very low which leads to an imprecise monitoring of the transistors temperature when measuring the opposite side of the PCB. In operation modes with significant power loss this leads to overheating and destruction of the GaN device [53]. When this occurs, the damaged transistors are exchanged.

All efficiency experiments are done with a DC voltage of $V_{DC} = 160 \, V$ which is either bucked or boosted to the resistive load connected to the AC side. For all efficiency measurements the dead time in the PWM signals is set to $t_{dead} = 70 \, ns$ which is verified with an oscilloscope.

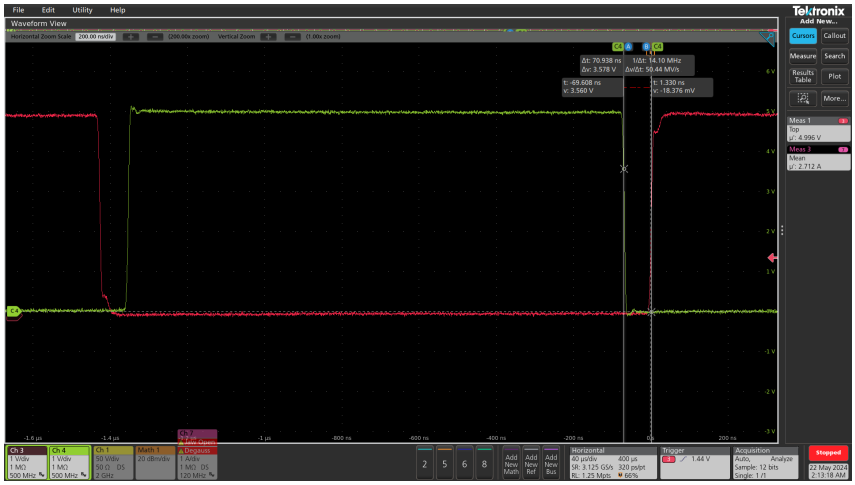

Figure 5.11: Verification of Dead Time between PWM Signals.

Figure 5.11 shows the dead time between the two PWM signals of approximately $t_{dead} = 70\ ns$. The dead time is important to assure that the commuting switches are at no time both turned on. This is crucial because it would lead to a short circuit and destruction of the transistors.

The effect on the efficiency of a change in load current, switching frequency f_{sw} and a change in modulation index m are investigated. The load current is set by alternating the resistance of the load in a range from $90\ \Omega$ to $5\ \Omega$. This is done by different serial and parallel connection of six $15\ \Omega$ phases of the resistive load. All load resistances applied to the AC side of the inverter during the experiments are shown in Table 5.2.

Table 5.2: Different Load Values in Efficiency Experiments.

Load Resistance $R_L[\Omega]$	90	60	45	30	22.5	18	15	11.25	10	7.5	5

Different switching frequencies in the range from $210\ kHz$ to $70\ kHz$ are investigated as well as an increment of the modulation index m from approximately 64% to 80%. For simplicity the modulation index m in this chapter is treated as percentage. The operating points investigated are summarized in Table 5.3.

Table 5.3: Frequency, Duty Cycle and Phase Shift in Efficiency Experiments.

Switch Frequency $f_{sw}[kHz]$	Duty Cycle m	Phase Shift [°]
210	80:17	66.4
140	80:18	126
140	64:34	68.3
105	80:18.5	126.7
105	64:34.5	69.1
70	64:35	127.5

The input power P_{in}, the power loss P_{loss}, the load current I_L and the efficiency η is measured. The experiment is done for the boost and the buck case of a positive DC current.

5.3.1 Efficiency Measurement of Boost Experiment

Figure 5.12 shows the measurement results for the boost case of a positive DC voltage. The highest total power transmitted during this experiment is $P_{tot} = 995\ W$ for a switching frequency of $f_{sw} = 70\ kHz$, a modulation index of $m = 64 : 35$ and a current of $I_L = 7.975\ A$. In this operation point the efficiency is the lowest. The highest efficiency $\eta = 98.689\%$ is achieved for a switching frequency of $f_{sw} = 140\ kHz$, a modulation index of $m = 80 : 18$ and a current of $I_L = 2.171\ A$. It can be seen that an increment in modulation index has a higher impact on the efficiency than a change in switching frequency. For a low modulation index, the effect of the an increment in switching frequency is more significant. For a high modulation index, an increment in switching frequency has little effect.

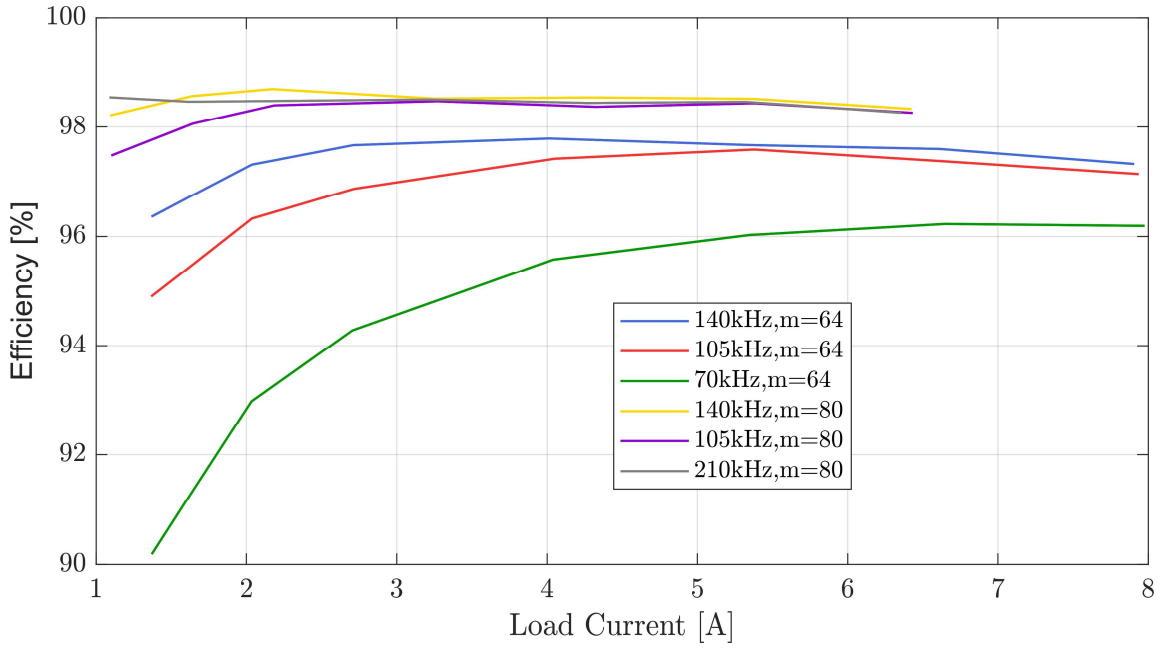

Figure 5.12: Inverter Efficiency of Boost Experiment.

Figure 5.13 shows that the efficiency for all operating conditions does not follow a quadratic function with a single global maxima but instead has multiple local maxima. The results obtained by experiment show atypical properties of the inverter. It is unusual for the efficiency load curve of an inverter to have multiple maxima.

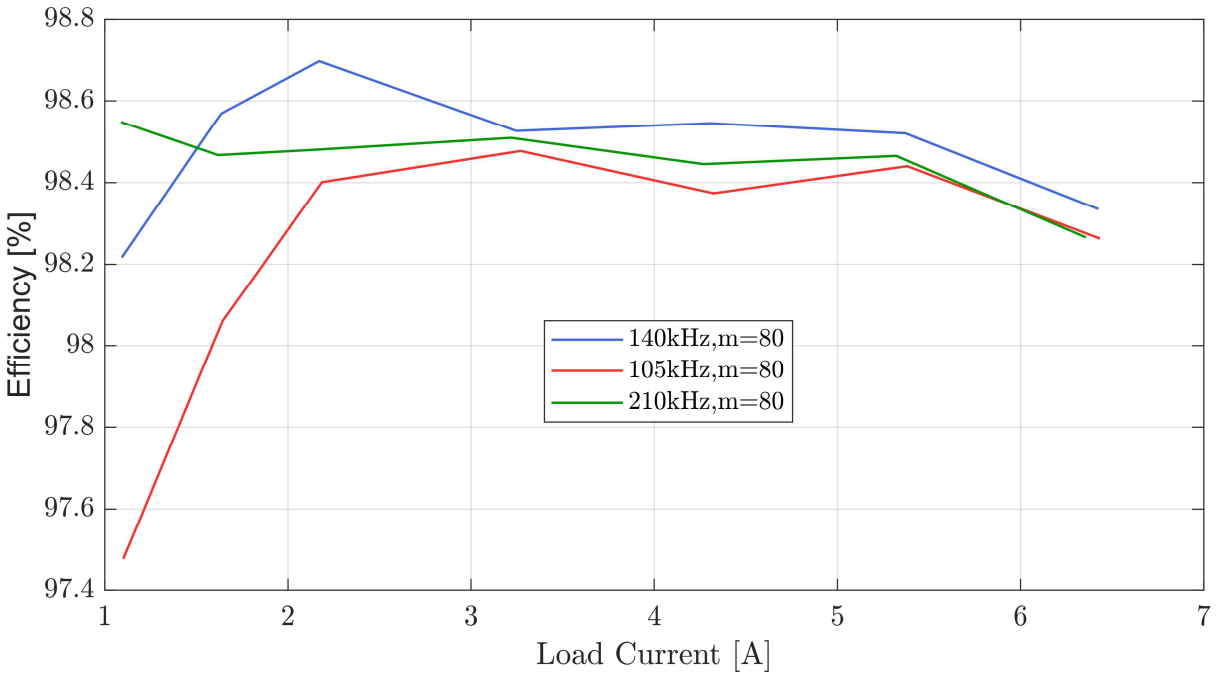

Figure 5.13: Zoom on Inverter Efficiency of Boost Experiment.

5.3.2 Efficiency Measurement of Buck Experiment

Figure 5.14 shows the measurement results for the buck case of a positive DC voltage. The highest total power transmitted during this experiment is $P_{tot} = 54.6\ W$ for a switching frequency of $f_{sw} = 105\ kHz$, a modulation index of $m = 64 : 34.5$ and a current of $I_L = 8.663\ A$. In this operation point the efficiency is the lowest. The highest efficiency $\eta = 97.858\%$ is achieved for a switching frequency of $f_{sw} = 140\ kHz$, a modulation index of $m = 80 : 18$ and a current of $I_L = 2.024\ A$. It can be seen that an increment in modulation index has a higher impact on the efficiency than a change in switching frequency. For a low modulation index, the effect of the an increment in switching frequency is more significant. For a high modulation index, an increment in switching frequency has little effect. The results obtained by experiment show atypical properties of the inverter.

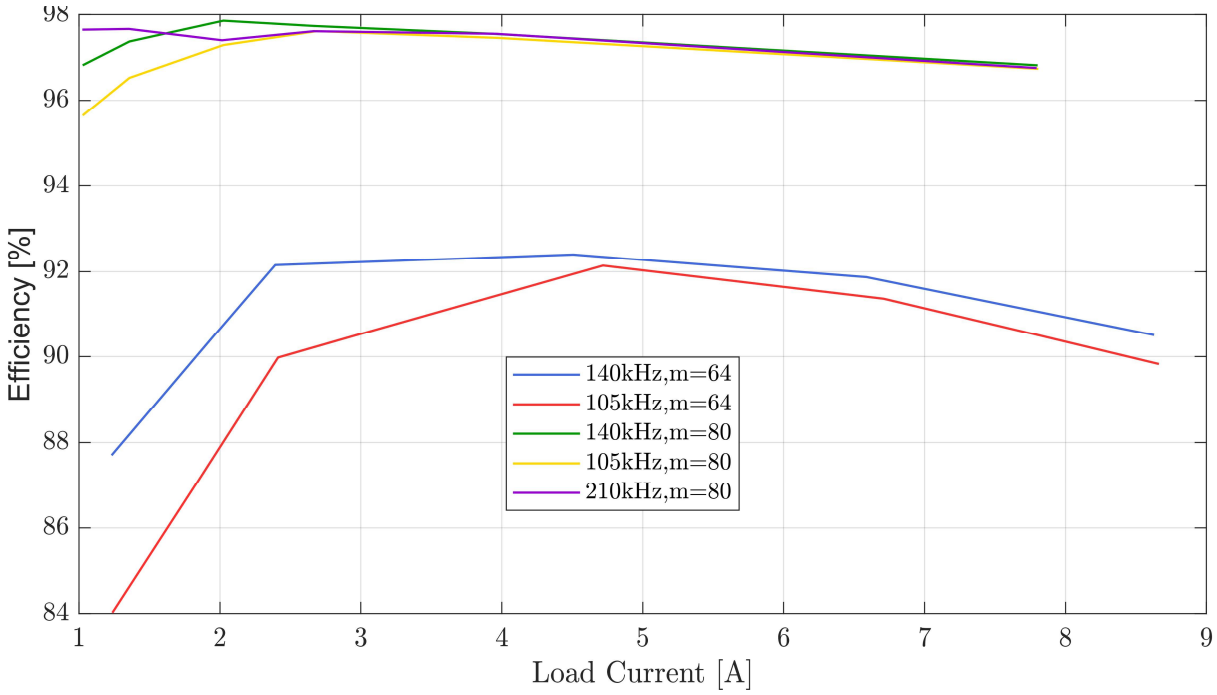

Figure 5.14: Inverter Efficiency of Buck Experiment.

Figure 5.15 shows that the efficiency for an operation at 240 kHz does not follow a quadratic function with a single global maxima but instead has two local maxima. The results obtained by experiment show atypical properties of the inverter. It is unusual for the efficiency load curve of an inverter to have multiple maxima.

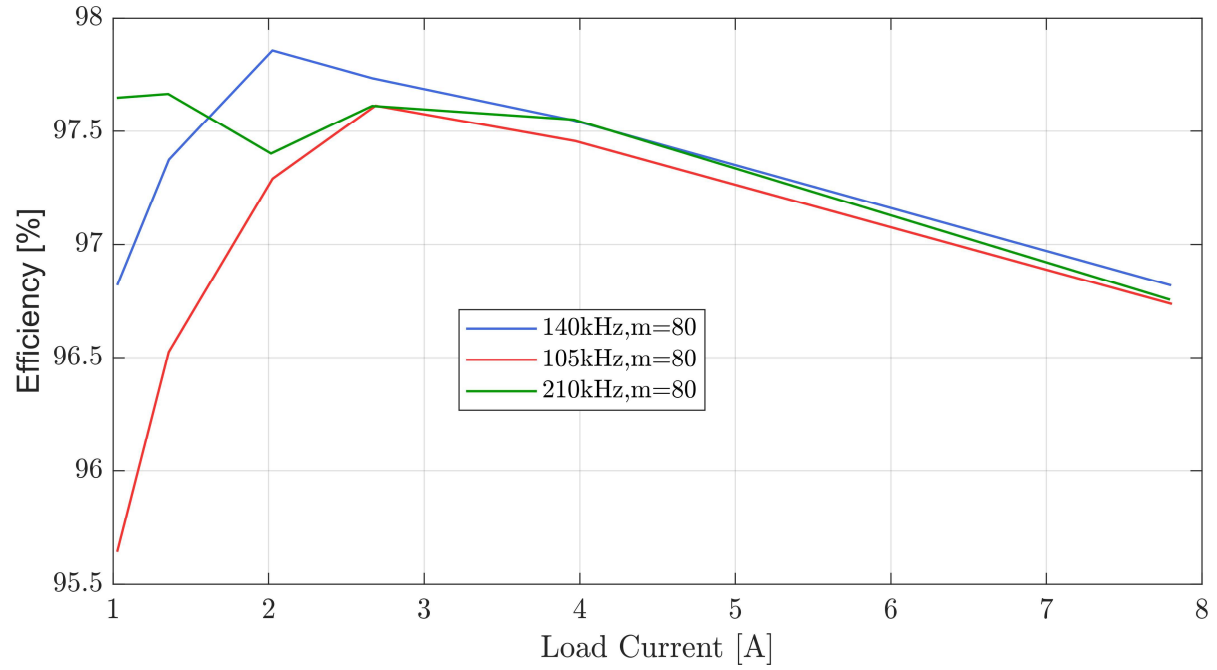

Figure 5.15: Zoom on Inverter Efficiency of Buck Experiment.

For a load current of $I_L = 2.666\ A$ an operation at 105 kHz as well as 240 kHz lead to an

efficiency of $\eta = 97.613$ which suggests that there are two effects of power loss which counteract one another as twice the switching loss is compensated. Similarly for an operation at a load current of $I_L = 3.961\ A$ yields an efficiency of $\eta = 97.552$ for operating frequencies of both $140\ kHz$ and $210\ kHz$.

5.3.3 New Inductance and Effect of Higher DC Voltage

It is suspected that the atypical efficiency curves with multiple maxima as well as low efficiency origins from the losses of the inductances L_1 and L_2. Therefore they are replaced by new inductors with twice the number of windings and thus factor four increased inductance. A smaller wire is used which has a higher resistance, increasing the conductive power loss. Furthermore, the effect of a higher DC voltage is investigated. Further experiments which the same DC voltage of $V_{DC}/2 = 80\ V$ are conducted with alternating modulation indices $m_i = [95, 80, 64, 55]$ and the same switching frequency of $f_{sw} = 140\ kHz$. The dead time is again always the same with $t_{dead} = 70\ ns$. The efficiency measurement for the boost case is shown in Figure 5.16.

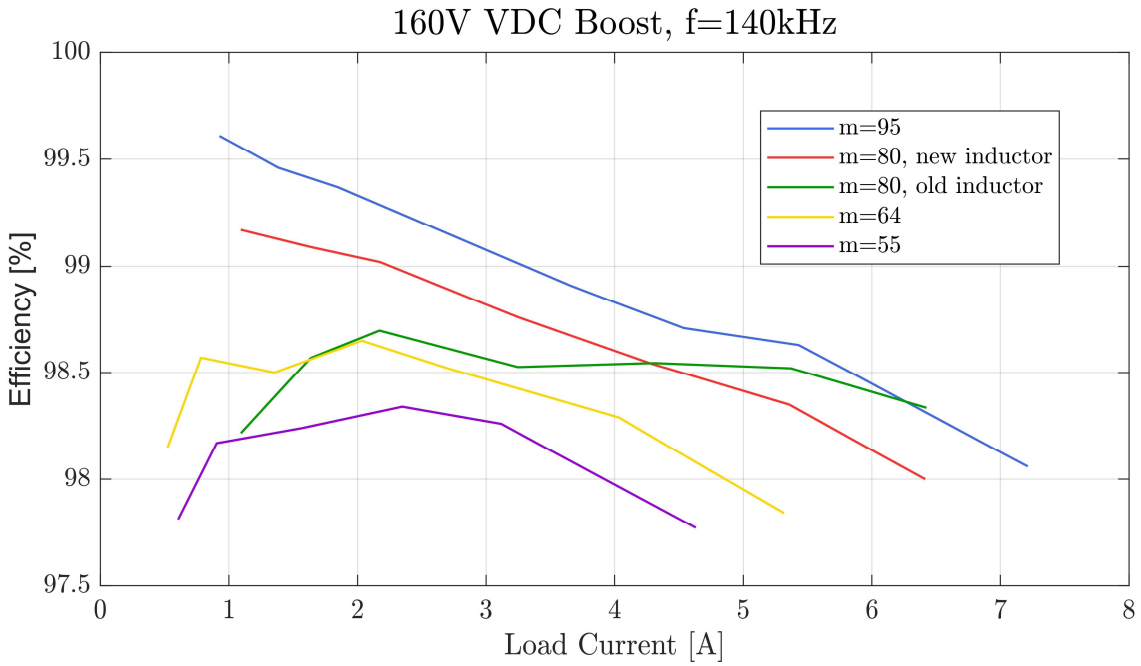

Figure 5.16: Inverter Efficiency of DC Boost Experiment With New Inductors.

The efficiency measurement for the buck case is shown in Figure 5.17.

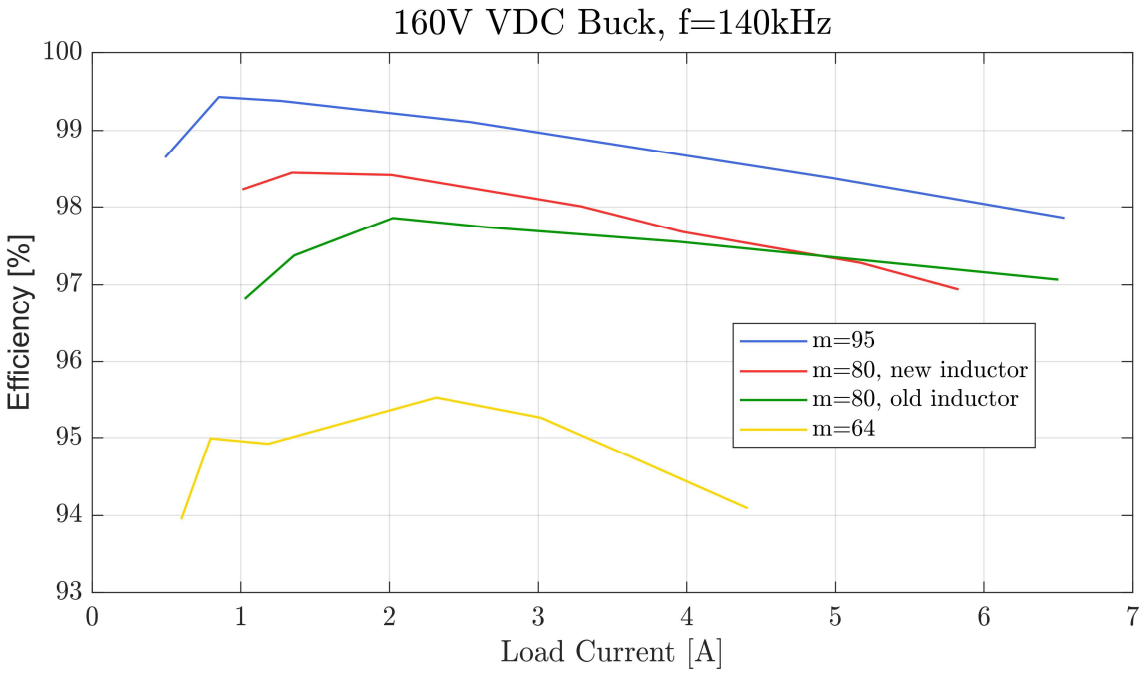

Figure 5.17: Inverter Efficiency of DC Buck Experiment With New Inductors.

It can be seen from Figure 5.16 that the new inductors have better performance at low currents but worse at higher currents. The efficiency for the relevant values of the modulation index are between 97.5% and 99.6%. For lower currents, the new inductors have an decreased ripple current which has a positive effect on the efficiency as it reduces the switched currents which contribute to switching power loss. For higher currents, this results from the increased resistance from the smaller wire cross section and the quadratic current dependency of the conductive switching loss. The highest efficiency is measured at the highest modulation index of $m = 95 : 3$ with a phase shift of $14°$, a load current of $I_L = 0.9265\ A$ and $\eta = 99.61\%$. It can be seen that the efficiency increases for a higher modulation index when all other parameters stay the same. It can be seen from Figure 5.17 that effect of the new inductors are verified. The efficiency for the relevant values of the modulation index is lower than 94%. Therefore, the inverter has worse performance when bucking a DC voltage than when boosting a DC voltage.

To investigate the effect of the DC voltage value, the same experiments are conducted at twice the DC voltage. The efficiency measurement for the boost case is shown in Figure 5.18.

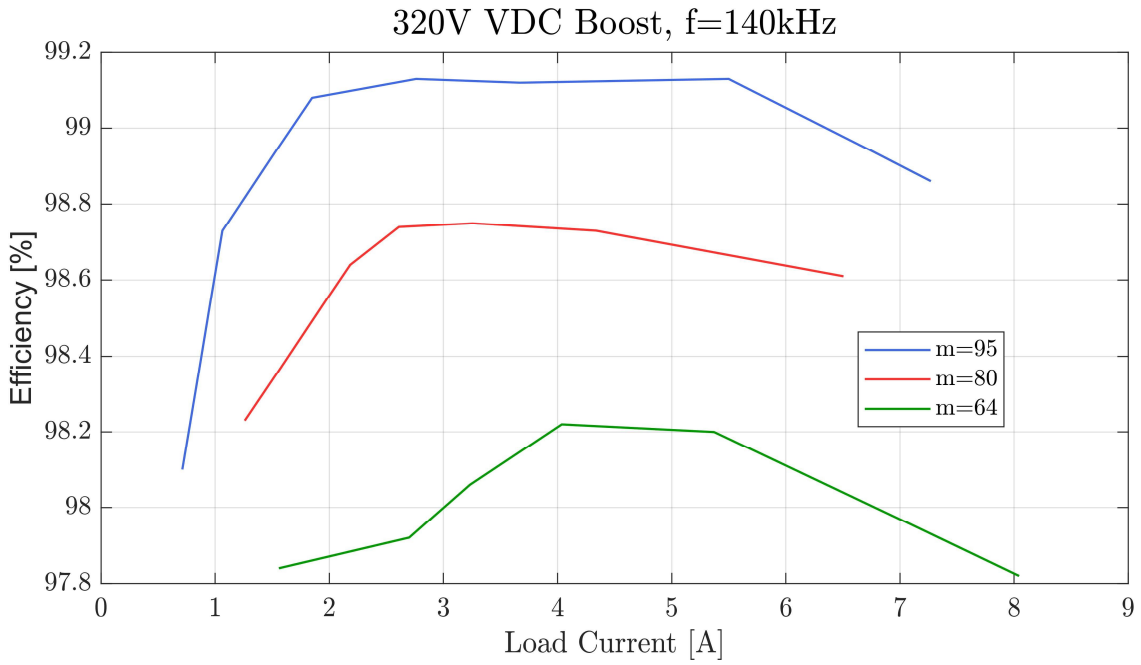

Figure 5.18: Inverter Efficiency of DC Boost Experiment with New Inductors.

The efficiency measurement for the buck case is shown in Figure 5.19.

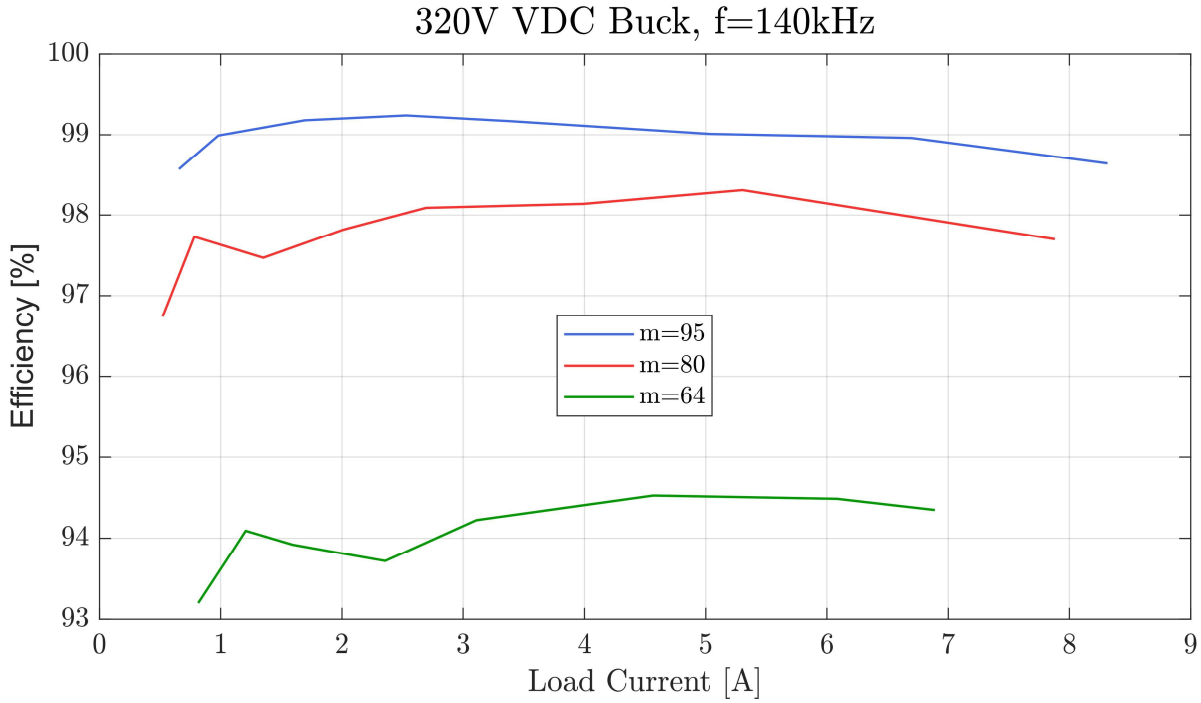

Figure 5.19: Inverter Efficiency of DC Buck Experiment with New Inductors.

It can be seen that a higher DC voltage leads to slightly lowered efficiency.

5.3.4 AC to DC Power Flow Experiments

In a final experiment, two working points of the inverter are tested with reverse power flow from the AC side to the DC side. A boost and a buck working point are set at the same DC voltage as in previous experiments. This means that a third power source is connected to the AC side and set so the desired DC voltage is reached. The power sources on the DC side are used to set the DC voltage and limit the current which enables swiping through all operation points without relying on a resistive load. This includes the PWM signal, specifically the dead time of $t_{dead} = 70\ ns$ and the modulation index m.

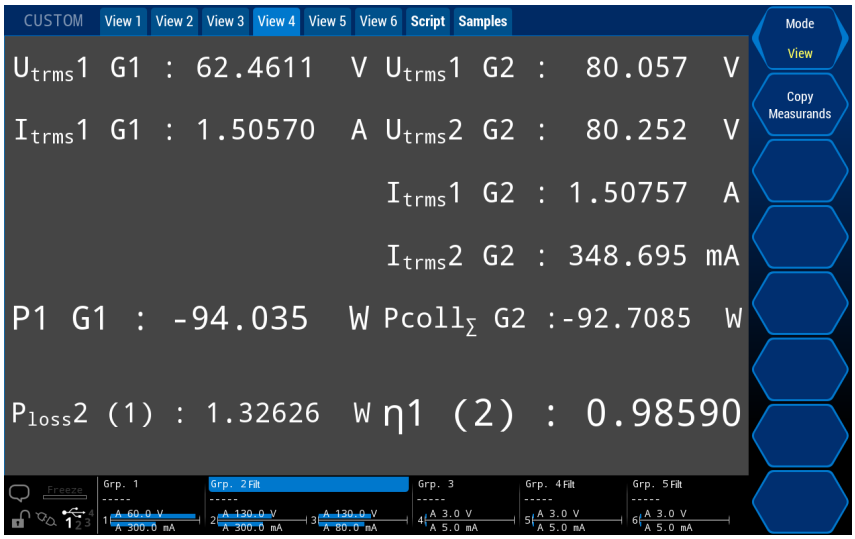

Figure 5.20: Inverter Efficiency of AC Boost Experiment with New Inductors.

Figure 5.20 shows the power analyser measurement of the AC boost experiment. The efficiency is very similar to value obtained in the same working point during the DC buck experiment.

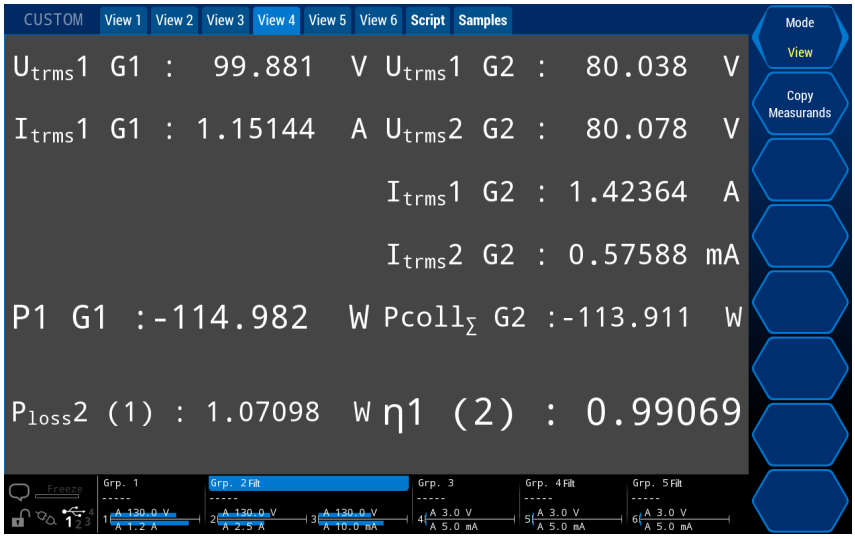

Figure 5.21: Inverter Efficiency of AC Buck Experiment with New Inductors.

Figure 5.21 shows the power analyser measurement of the AC buck experiment. The efficiency

is very similar to value obtained in the same working point during the DC boost experiment.

5.3.5 Summary of Inverter Properties

At this point the inverter is not able to bidirectionally connect an AC grid to a DC ESS. It is only able to operate certain DC to DC working points. Based on the experimental results and observations, the inverter specifications are summarized in Table 5.4.

Table 5.4: Properties of Assembled Bidirectional Single Stage Grid Connecting Power Converter.

Property	Rated Values
Input Power	$P_{in} = 200\ W$
Nominal DC Voltage	$V_{DC,nom} = 160\ V$
DC Voltage	$V_{DC,max} = 320\ V$
Maximum Efficiency	$\eta = 99.689$
Switching Frequency	$f_{sw} = 140\ kHz$

The properties displayed in Table 5.4 result from observations and represent a first estimation of the inverter properties. A significant power loss of more than $P_{loss} = 20\ W$ for an extended time leads to thermal destruction of the inverter even through an installed heatsink. A worst case efficiency of $\eta = 0.9$ is assumed and results in a rated input power of $P_{in} = 200\ W$. An improved method to cool the GaN switch packages is likely to increase this value. The best efficiency is recorded at a DC voltage of $V_{DC,nom} = 160\ V$. Operation at a working point of bucking a DC voltage of $V_{DC} = 400\ V$ to a grid voltage of $V_{AC} = 150\ V$ leads to destruction of the GaN transistors. A sufficient margin to avoid destruction results in a rated voltage of $V_{DC,max} = 320\ V$. As only the working points presented in Table 5.3 are investigated at a DC voltage of $180\ V$ and $360\ V$, it is possible that higher efficiencies are achievable at other operating points. Similar, lower and higher switching frequencies than the rated switching frequency are possible but $140\ kHz$ show the best performance because at high switching frequencies the switching losses increase and at low switching frequencies the magnetic coil losses caused by the ripple current increase.

6 Discussion, Conclusion and Future Work

In the final chapter of this thesis the results and the project are discussed. A conclusion based on the results and the insights gained during the thesis work is drawn and an outlook for possible future work based on this project is given.

6.1 Discussion

In this section the project, the project and the experimental results are further interpreted and discussed. Suggestions are made which may help to avoid challenges or simplify processes encountered in the course of this thesis.

Bidirectional Single Stage Inverter

The experiments show that the four quadrant switches enables bidirectional power flow with both boost and buck operation with a single stage inverter topology. Theoretically, the inverter is suitable for bidirectional connection of AC grid and DC ESS. The experiments show that the there is a significant difference in efficiency between DC buck operation and DC boost operation. When boosting a DC voltage the inverter show worse performance than in the case of bucking a DC voltage. Reason for this is possibly a current conducting between the DC sources which is observed in experiment and can also be seen in simulation as shown in Section 3.2.2 Figure 3.9. This leads to a need for larger electrolytic capacitors on the DC side and lower system power density.

Atypical Efficiency Curve

The results show that the dependency of efficiency on switching frequency is relatively low. This leads to the assumption that the switching loss of the GaN transistors are low because switching losses are linear frequency dependent. The effect of change when varying the duty cycle is typical as for a higher modulation index, the efficiency increases. Reason for this is that the target side voltage is higher than the source side which leads to an increased total output power and therefore reduced impact of the constant losses.
The experiment results show local maxima of the inverter efficiency curves. The total power loss of the inverter can be seen as sum of switching, conduction and inductive losses. The switching loss is linearly frequency dependent. Conduction loss of the inverter is quadratic load current dependent. The conduction losses are expected to reduce significantly when the bidirectional GaN transistors replace the two anti serial unidirectional switches. This is because the drain source resistance is reduced as each switch in series adds up to the total value. Part of inductance losses result from the core of the coils absorbing the voltage time area. These inductive core losses are constant. The temperature effect on the power electronic system which impacts the efficiency is not taken into account.

When the inductances are replaced with coils with twice the number of windings but smaller wire cross section, this results in factor four higher inductance value and higher resistance. This in turn results in lower conduction losses at low currents because the current ripple is reduced by the higher inductance. However, higher conduction losses at higher currents result from the resistance increment. At low load currents the impact of the constant losses is dominant. At high load currents the quadratic current dependent conduction losses become dominant. This explains the general shape of the efficiency graphs with one maxima. Another extreme local point can be explained by switching losses. For low currents, the DC component of one of the two inductances is zero and only the current ripple is present which causes soft switching. At higher currents the DC component of the inductance current becomes larger than zero which results in hard switching and thus switching power loss increment.

Transistors Blocking Voltage

Actual grid applications such as OBC systems or ESS for grid stabilization or in end consumer households require higher blocking capabilities than achieved with the assembled inverter due to the limited blocking capability of the GaN devices. Therefore, the designed and assembled inverter is merely of investigative research interest. Higher blocking capabilities of monolithic bidirectional switches are currently a hot topic of research because the improvement is of high importance for the transition to Power Electronics 4.0 which describes the innovative step to a new generation of power electronic devices [54]. Innovation can be expected either by utilization of GaN sapphire substrate technologies [55], mature SiC technologies such as super junction [56] or ultra-WBG materials such as diamond [57]. Until significant progress in regards to the blocking voltage is made or a different solution such as the flying capacitor approach is investigated and proven, a commercial product of the topology is unlikely.

Inductance of Commutation Loop and Overshoot Voltage

The overshoot voltage observed in Section 5.2 likely results from the parasitic inductance of the commutation loop. Because of the efforts made to design a low inductance commutation mesh, an parasitic inductance of approximately $L_{loop} = 18\ nH$ is achieved. The simulation made in Section 5.2 is an approximation because the inductance is along the entire system and not concentrated in a single component. A more accurate way to determine the parasitic inductance is a 3D field simulation of the system which is more complex and more time intensive. The number of components involved in the commutation contribute to an increment in parasitic inductance value. In order to reduce the overshoot voltage, it is possible to either increase the gate driver circuit resistance R_{on} or decrease the size of the capacitor C_{on}. This measure slows down the dv/dt of gate capacitance discharge and recharge which reduces the overshoot. However, this leads to an increment of switching losses. An optimal trade off between higher achievable operating voltages and increased switching losses can be done with a suitable model. Another approach to reduce the parasitic inductance resembles the usage of embedded transistor packages.

Measuring Connectors

It is useful to include dedicated measuring points to prototype topologies during the layout phase. Thereby, the testing and commissioning phase is simplified as voltages can be measured by connecting to the measurement points instead of directly at the transistor with manual. Connection points dedicated for measuring are easier than using differential probes to measure the transistor pins directly. Additional connectors also enable a double pulse test which requires certain connecting points to the topology.

Assembly of PCB

Delamination describes the detachment of layers in material composites such as a PCB [58]. This phenomenon may occur because of excessive heat. The PCB designed in this project has areas with six layers of copper next to areas without any copper layers. Copper transports the heat efficiently due to its conductive properties. When assembling the surface mounted devices, the PCB or more precise, the copper pads need to be heated to solder the electrical components to it. In areas with a lot of copper, more energy is required to sufficiently heat the component's pads. In areas with little copper, the same heat energy is to much as there is not enough heat conducting material consequently the PCB layers becoming to hot and resulting in delamination. Delamination has impact on the electrical properties as the insulating and conducting layers are no longer directly connected to one another but air is between them. Therefore, if delamination occurs, the PCB has a defect and unpredictable properties which may cause unpredicted behaviour or even dangerous errors.

Figure 6.1: Delamination on the Printed Circuit Board.

Figure 6.1 shows the delamination on the PCB fabricated during the assembly. Delamination and the general quality of the contact between components and the PCB pads can be improved with the process of the fabrication line. Fraunhofer IZM offers the possibility to automatically micro dispense solder paste onto the PCB by jetting technology. This increases the accuracy and the amount of solder paste dispensed. Only the placement of the components needs to be done by hand which reduces the sources of errors. Afterwards, the PCB can be baked at optimum temperature to precisely heat up the solder to an ideal temperature. Hereby the soldering process is almost fully automated. Automatising of applying solder paste and heating increases the accuracy and enhance the connection of the solder points which has impact on the resistance and thus the power loss and efficiency. There is sufficient material to assemble a prototype with this method.

6.2 Conclusion

A conclusion is made regarding the project, the designed and assembled DUT and the performed experiments. The scope of this thesis described in Section 1.2, to design, parameterize, assemble, and commission a single stage, buck-boost inverter is fulfilled. The commutation loop inverter design has relatively low inductance at $L_{loop} = 18\ nH$. The knowledge gained through experiment validates the properties of the inverter based on simulation as presented in Chapter 3. This includes the derivation of the modulation index m, the commuting switches for each operation mode $M_1, .., M_4$, the required blocking capabilities of the switches as well as

the fundamental ability of the novel inverter to connect an AC grid to a DC ESS with a single stage only. No conclusion of the total inverter efficiency can be made as it is operated in DC to DC only and there exist no power loss model of the system at this point. The commissioned inverter is a simplified version of the topology suggested by Eckart Hoene as it does not include the flying capacitor concept. This leads to the prototype being unable to be utilized in real world application for grid connection of DC energy systems. Reasons for this is the insufficient blocking capability of the transistors but also the undeveloped control algorithm for AC to DC operation. A possible application after further improvement may be balcony solar panels as they generate relatively low DC voltage of $50\ W$.

The investigated novel inverter topology requires further analysis. The research work within the EnerConnect project represents fundamental research in the process of finding innovative solutions to the upcoming challenges of power electronics. This work serves as introduction to the topology in simulation, layout design, PCB assembly and provides a first insights to operating the topology. When exploring methods to increase efficiency in grid connection of ESS with bidirectional AC to DC inverters employing four quadrant GaN devices, this thesis resembles a first fundamental investigation.

6.3 Future Work

In this section possibilities for future work based on this project is given. The project EnerConnect is funded until 2028. The master thesis of Technical University Berlin student Nahyun Lee focuses on the closed loop control of the bidirectional grid coupling inverter presented in this thesis. A feasibility investigation of the presented inverter for balcony PV application may be of interest.

Power Loss Composition

In order to explain the atypical efficiency curve of the inverter, several measurements can be taken. The switching loss of the GaN transistors utilized in the inverter assembly can be tested with a double pulse experiment. Thereby, the switching loss during operation can be derived. The conduction loss of the inverter can be simulated and thereby estimated. The power loss properties of the magnetic core can be approximated in simulation. To estimate the inverter properties regarding the efficiency in full sine operation, further simulation of the power losses needs to be done. Using the efficiency measurements an inverter power loss model can be created. Possibly further measurement points need to be taken to make the model more accurate. Afterwards, an optimisation of the system can be done. The inductances, the switching frequency and the EMI filter as well as the parasitic resistance of the system represent degrees of freedom for this optimization. Thereby a better understanding of the inverter and a possible application case can be defined well-founded.

Flying Capacitor Approach

The concept of enabling the $600\ V$ rated blocking voltage GaN switches in in this topology to fulfill the conditions required in AC grid to high DC voltage application such as automotive OBC or other ESS by utilization of a flying capacitor concept is neither proven nor refuted at this moment. Future work may investigate the flying capacitor integration to the proposed topology and the feasibility of the solution.

Closed Loop Operation with Varying Grid Side

The end of the line goal of grid connecting inverters are fully stable systems which can control the amount and direction of power flow in real time while emitting low EMI. During this project only DC to DC operation was investigated. The next step when further exploring this topology, could be research of the AC to DC operation of a $50\ Hz$ sine connected to the DC side. Simulative investigations have shown that the transition between operating modes such as boost and buck operation requires precise control of the commuting switches to ensure smooth operation. Master student Nahyun Lee is writing a thesis about the closed loop control of this topology within the frame of the EnerConnect project and expanding the insights about the inverter.

Different Topologies

During the EnerConnect project time frame further topologies will be investigated and may be compared to the inverter topology shown in this thesis. Advantages and disadvantages of these topologies can then be explored to make a decision on which inverter topology is most promising when approaching the goal of 99% between grid and ESS. Topologies which may be compared include a 3-level Neutral Point Clamped 2 topology [59].

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A PCB Layers in Altium Design Layout

In the appendix all layers of the Altium design are shown in detail. The six layers of the PCB are designed during this thesis. They are optimized for a low inductance commutation loop. The PCB design features a control interface which connects to the transistors. Additionally, the control unit can be accessed via a CAN interface. Furthermore, a DC voltage measurement unit, an AC current measurement unit and a power supply unit for the control interface and the measurement units are designed on the PCB. However, these units are not assembled and not connected.
Figure A.1 shows the 3D top side view of the PCB design.
Figure A.2 shows the 3D bottom side view of the PCB design.
Figure A.3 shows all layers of the PCB design.
Figure A.4 shows the top layer of the PCB design.
Figure A.5 shows the second layer of the PCB design.
Figure A.6 shows the third layer of the PCB design.
Figure A.7 shows the fourth layer of the PCB design.
Figure A.8 shows the fifth layer of the PCB design.
Figure A.9 shows the bottom layer of the PCB design.

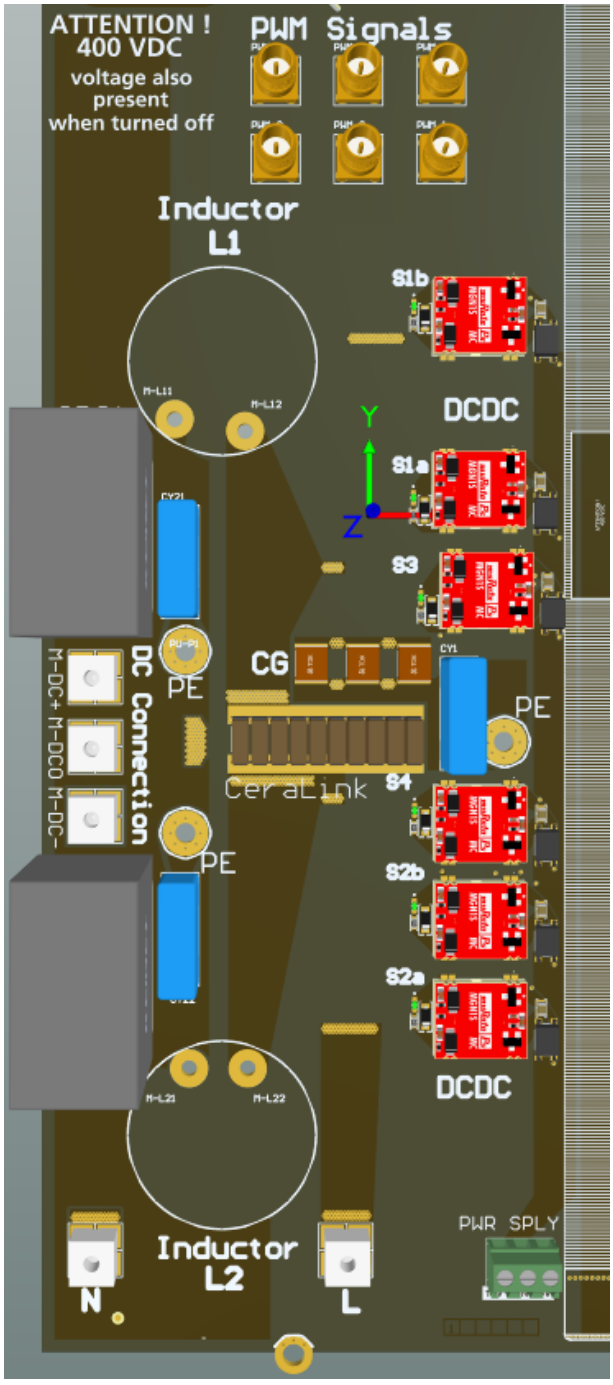

Figure A.1: 3D Top View of the PCB Design.

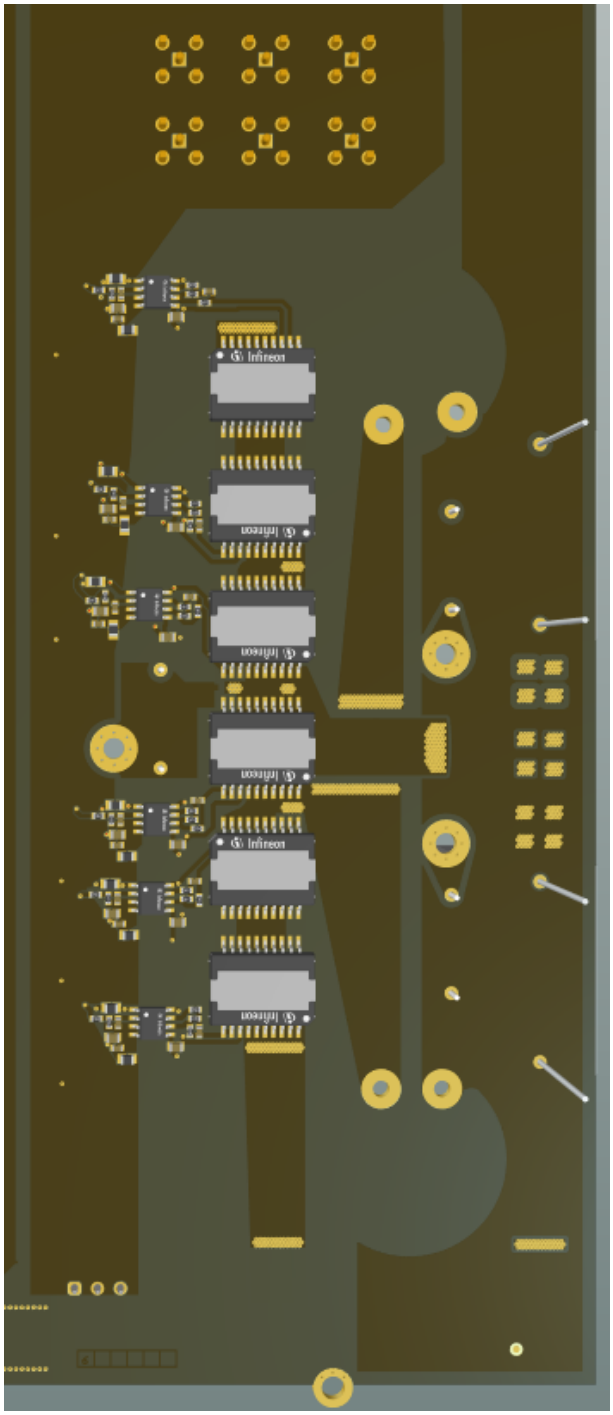

Figure A.2: 3D Bottom View of the PCB Design.

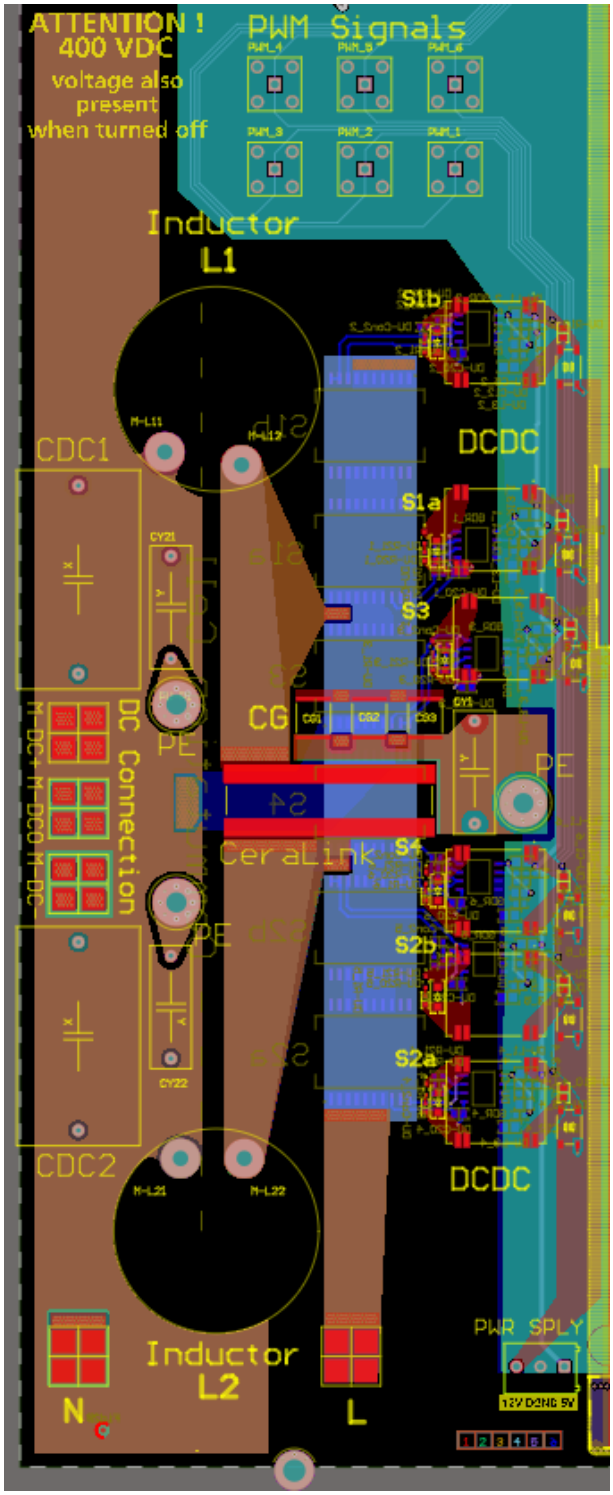

Figure A.3: All Layers of the PCB Design.

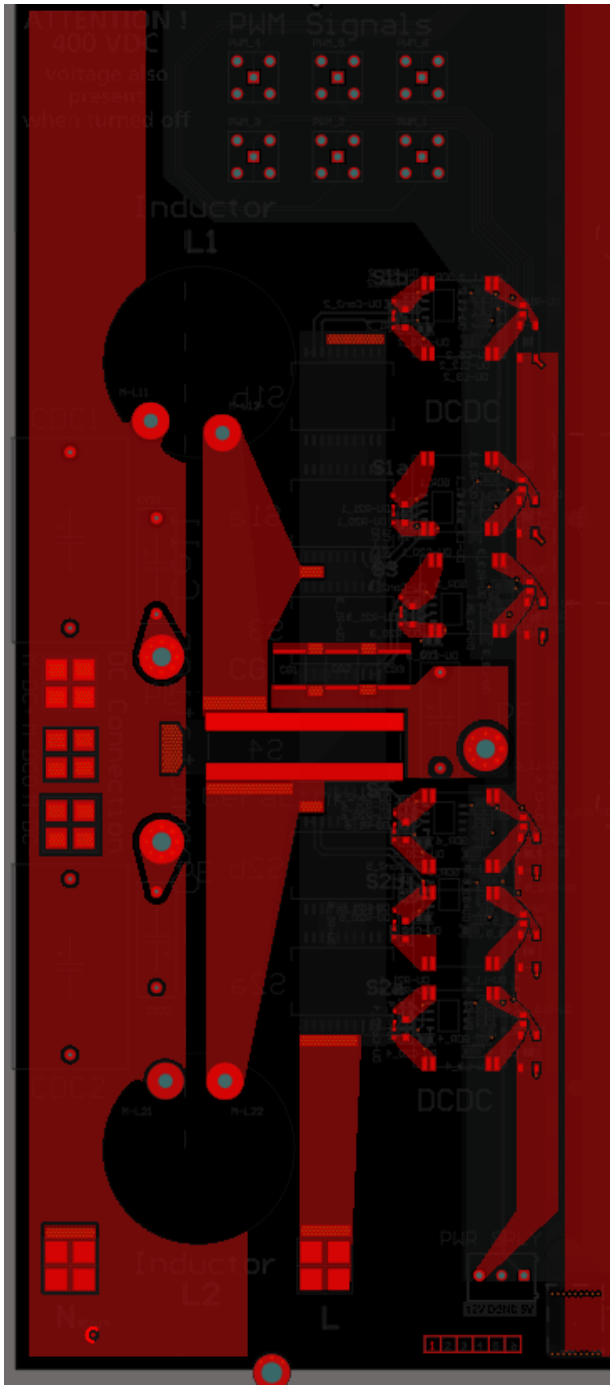

Figure A.4: Top Layer of the PCB Design.

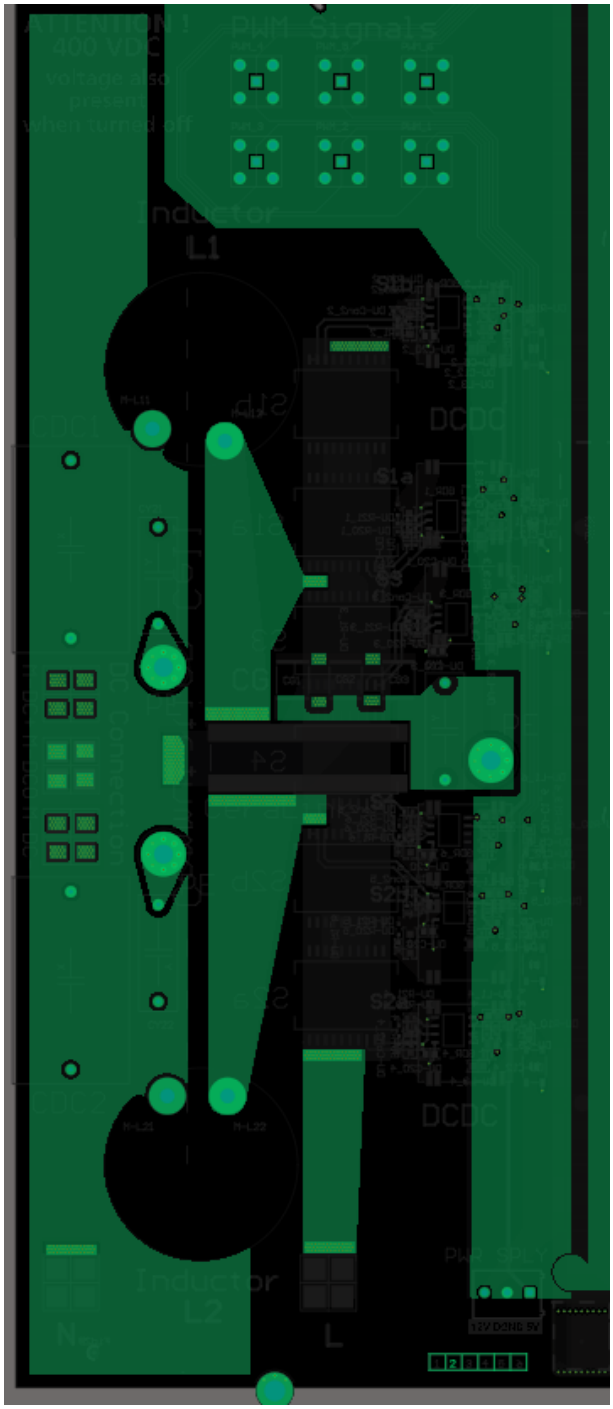

Figure A.5: Second Layer of the PCB Design.

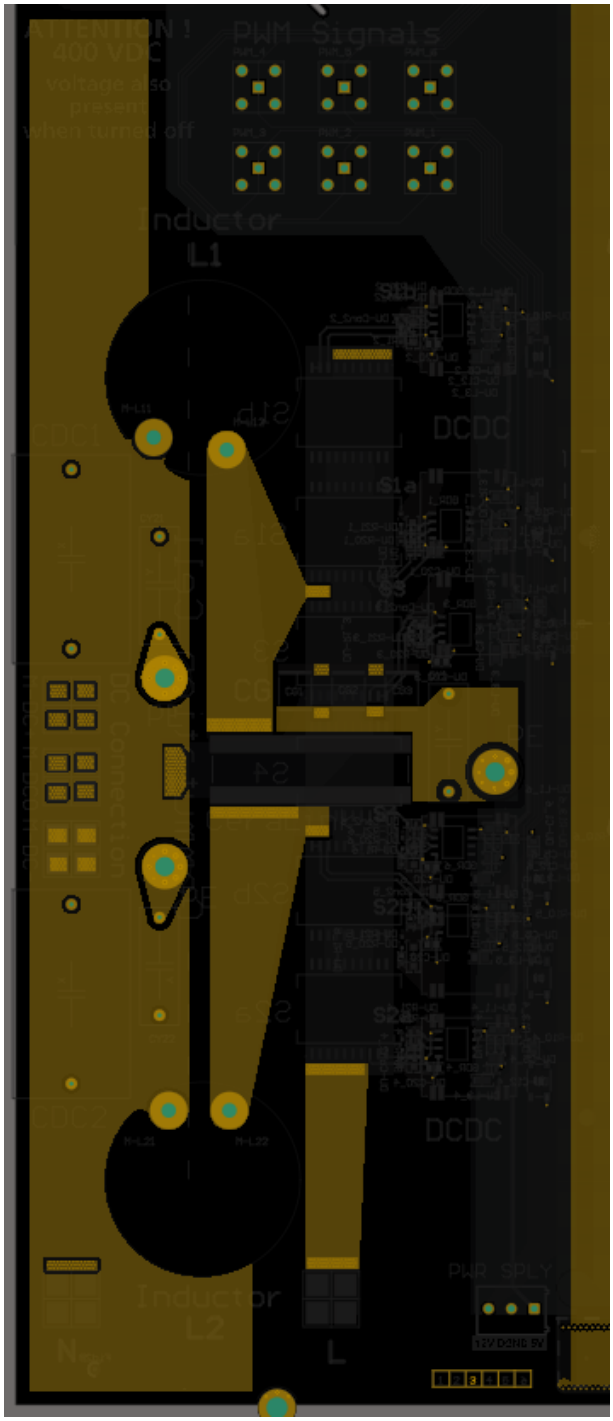

Figure A.6: Third Layer of the PCB Design.

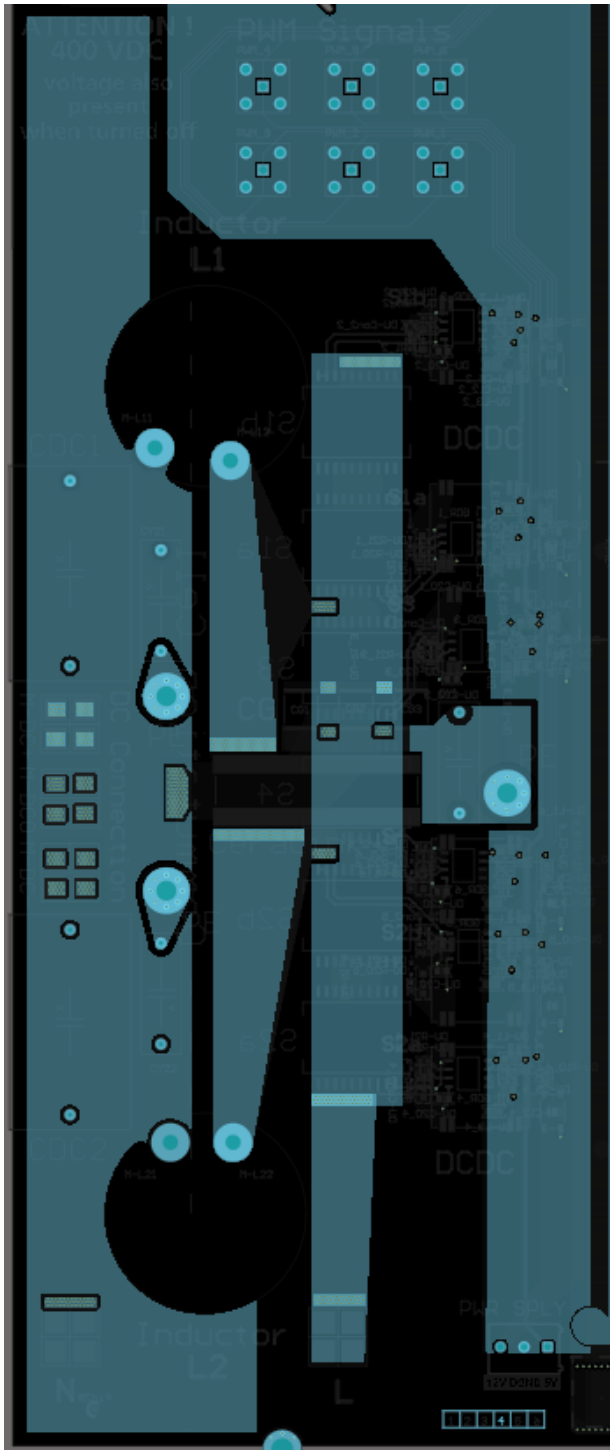

Figure A.7: Fourth Layer of the PCB Design.

Figure A.8: Fifth Layer of the PCB Design.

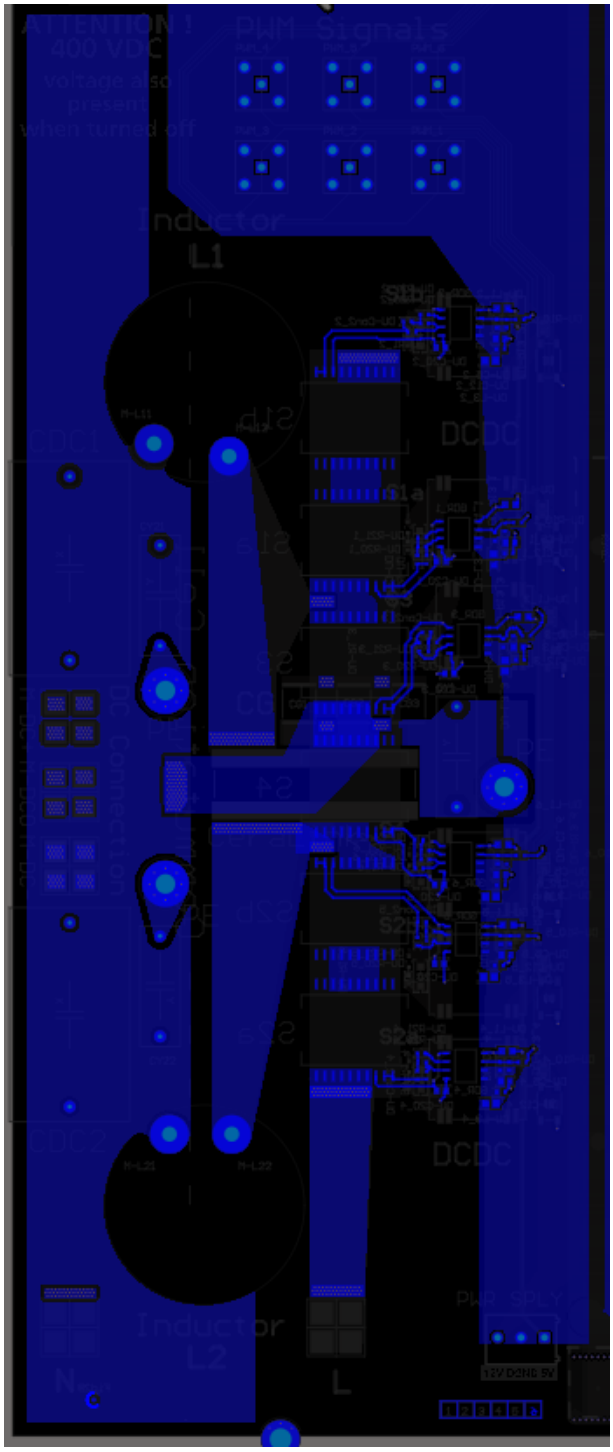

Figure A.9: Bottom Layer of the PCB Design.