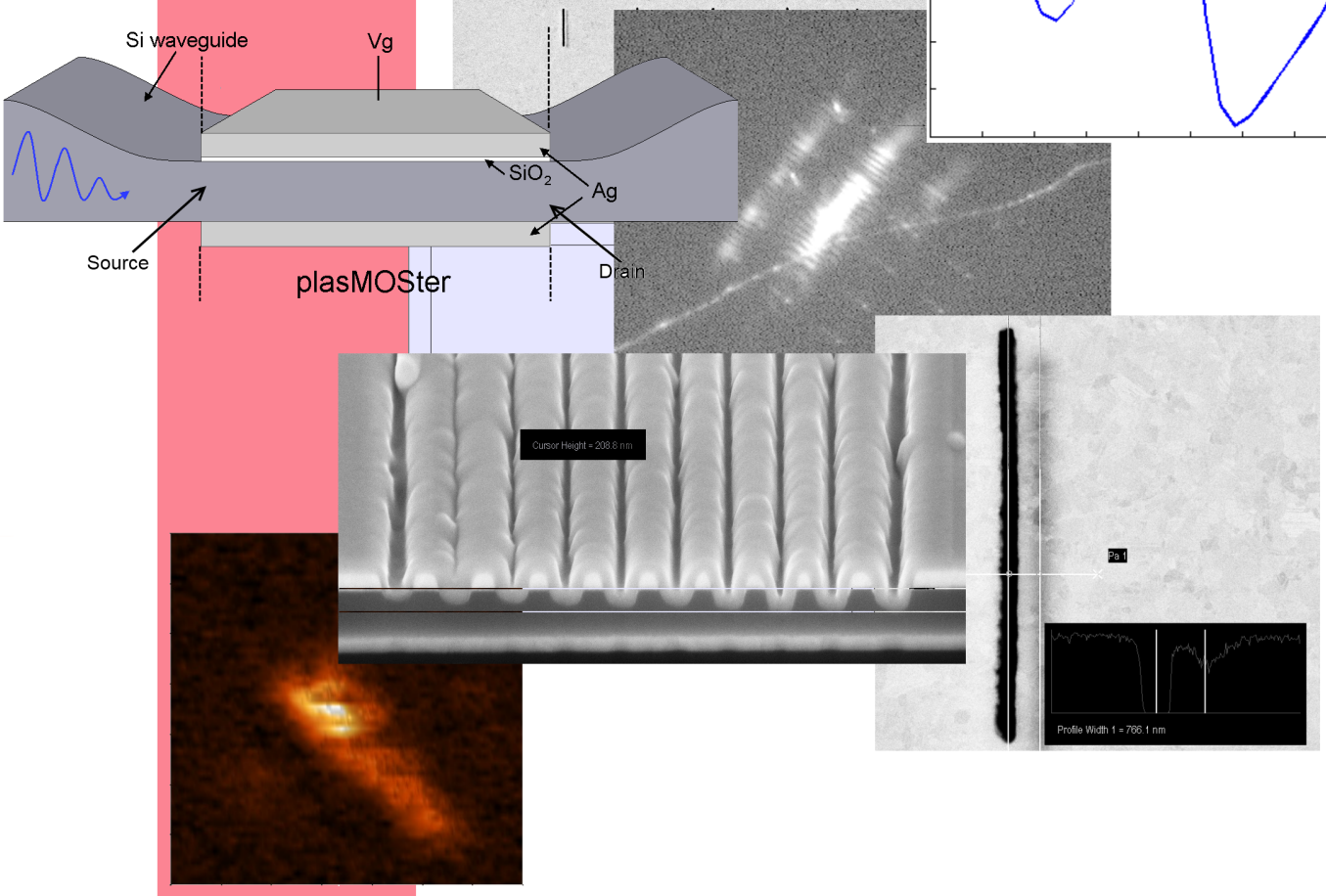
VLSI ready plasMOSter. Design, fabrication and characterisation



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Synopsis:

This thesis presents a novel approach to fabrication of plasMOSter devices with focus on Very Large Scale Integration. A plasMOSter is based on propagating surface plasmons and is an electro-optical transistor that uses an electric signal to control the transmission of near infrared light through it. The design of the device is based on photonic dispersion engineering of the plasMOSter structure and finite element analysis of its operation. The layers that constitute the plasMOSter is here deposited solely using e-beam deposition. The wave guide in this design is low density *a-Si* which is examined using ellipsometry. Finally, NSOM and IR microscopy are used to verify simulation results of the structural dependence of the output.

Preface

This master thesis is composed in the period from the 15th of January to the 14th of June 2012 during my 4th semester in the Nanophysics and -materials program at Institute for Physics and Nanotechnology at Aalborg University.

The subject of the thesis is *VLSI ready plasMOSter. Design, fabrication and characterisation.* Since data from the various fabrication steps were needed in order to properly treat the device theoretically and provide optimum structure parameters, devices were fabricated without knowledge of optimum structure. Unfortunately, a key device in the fabrication process went out-of-order after the first series and was not repaired in time to make a run with optimum parameters. However, the experimental data extracted from the first fabrication run showed tendencies that are prerequisite for functionality of plasMOSters.

The project which started as a crazy idea and ended as a slightly less crazy one, greatly benefited from the kind aid of some noteworthy persons to whom I owe my thanks. A thanks to Peter Kjaer Kristensen for sharing his insight and great advice and without whom the fabrication would never had gone so smoothly.
A thank you, to Giulio Biaggi for valuable discussions and for teaching me the ways of the NSOM.
And a big thank you to Tobias Holmgaard for spending hours on hours introducing me to Focused Ion Beam lithography and his seemingly endless patience in doing so, that goes well beyond the call of duty.

Contents

1 Introduction

In 1965 Gordon E. Moore in a paper for Electronics Magazine noted that the complexity of integrated circuits increased by a factor of two per year and estimated that it would continue to do so for at least ten years[21]. Moore overestimated the progress of technology, but greatly underestimated how long the industry was able to keep alive what was later to be known as Moore's law. In 1975 Moore revisited his statement from ten years earlier and changed his prediction to be a doubling in transistors per integrated circuit to be doubled every two years[20].
Today Moore is also known as one of the founders of Intel$^{\mathbf{TM}}$ who is keeping his law alive at least until 2015, where they have announced they will be producing components with half-pitch width[1] of $10nm$[8, 24]. We are quickly approaching a natural limit for scaling down the size of components to ideally a single atom transistor. Furthermore, at such small scale, effects like propagation delay and parasitic capacitance which always exists between two wires, becomes more profound as the wires are packed closer[5]. So the big question is: What happens next?

Modern fiber optics is already widely used for long range communication since it is far superior to electronics in terms of bandwidth, speed and loss. Computational devices are based on electronics so optical signals are converted before they are used in computation. An obvious next step would of course be to replace electronic components with optical ones. This is by no means a simple task. Where on-chip optical communication would eliminate the previously described problems that constitute the interconnect-bottleneck, it does suffer from some disadvantages on the microscopical scale.
Electronic components as those being used today have the advantage over photonic computers that the individual components can be made in the low end of the nanoscale, where with photonics scaling is limited, not so much because its hard to make the components small, but due to restrictions like the diffraction limit. This limit is of course based on the wavelength of light used and using shorter wavelengths would allow for smaller structures. However, modern communication and microchip technology is build up around silicon which has high absorption of visible and shorter wavelengths. So, any attempt to fundamentally change the operating mechanisms that govern signal processing should preferably be compatable with modern silicon technology.
The diffraction limit can be beaten though, using plasmonics. Plasmonics is a rapidly growing field based on squeezing light into structures much smaller than the wavelength. Introducing plasmonics allows for some or all of the optical communication to take place below the diffraction limit. Since plasmons are essentially collective movement of charge, plasmonics has some of the same speed issues as electronics.

[1] The distance from the centre of the gate to the centre of the source and drain of the transistor in question.

Therefore, plasmonics are not supposed to replace electronics or compete with photonics, but instead act as a bridge between the two. When talking plasmonics, surface plasmon polaritons(SPP) are usually what is refered to. Surface plasmons are plasmons localised near the surface of a metal. Over the past years, the scientiffic and engineering community has produced several breakthroughs in coupling light in and out of SPPs. Of course this is interesting in terms of "all optical" communication and signal processing, but considering photo diodes and subwavelenght lasers the foundation is laid for mixing optical and electrical communication and signal processing on a very compact scale using plasmonics. Here a device is presented, that bridges the gap between optics and electronics in signal processing acting like an AND gate performing the Boolean operation $A \cdot B$. Where the classic transistor takes in two electrical signals and the photonic transistors takes in two optical signals, the plasmonster here presented performs its logical operation on both an optical and an electronic signal, producing an optical output. The device here presented resembles a MOSFET both in structure and operation. The basic operation of both devices is illustrated on Figure 1.1.

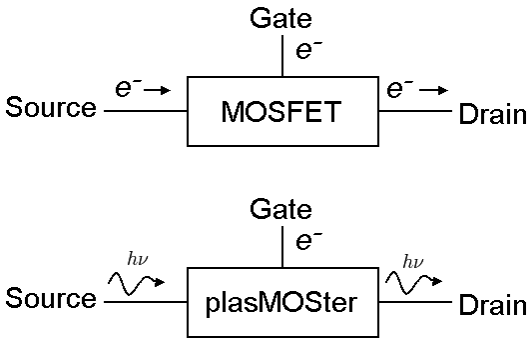


Figure 1.1: *Similarities between a MOSFET and a plasMOSter. The MOSFET modulates an electronic signal going from source to drain using a second electronic signal.*
The plasMOSter uses an electronic signal to modulate an optical signal.

As the name indicates, the plasMOSter is based on a Metal Oxide Semiconductor(MOS) capacitor, just like a MOSFET. The plasMOSter is essentially a multimode waveguide that is designed in a way so the modes interfere destructively at the output so no light is transmitted. Like in a MOSFET, a gate bias causes charge carriers to accumulate near the semiconductor/oxide boundary. An increase in charge carrier concentration results in a higher electrical conductivity, which in a MOSFET, allows for easy passage of charge carriers. For optical signals, an increase in conductivity has the opposite effect especially for near infrared wavelengths where absorption increases with conductivity. In a plasMOSter, two propagating modes are present, a photonic and plasmonic(i.e. as propagating surface plasmons). The plasmonic mode is localised at the metal interfaces and are not affected much by the increase in conductivity. The photonic mode on the other hand has most of its field in the semiconductor and is therefore damped much more than the plasmonic when increased conductivity is induced in the semiconductor. By shutting off one of the modes like this, modes no longer cancels eachother at the output and a higher nonzero output is generated. The operation principle of plasMOSter fabricated in this project is illustrated on Figure 1.2

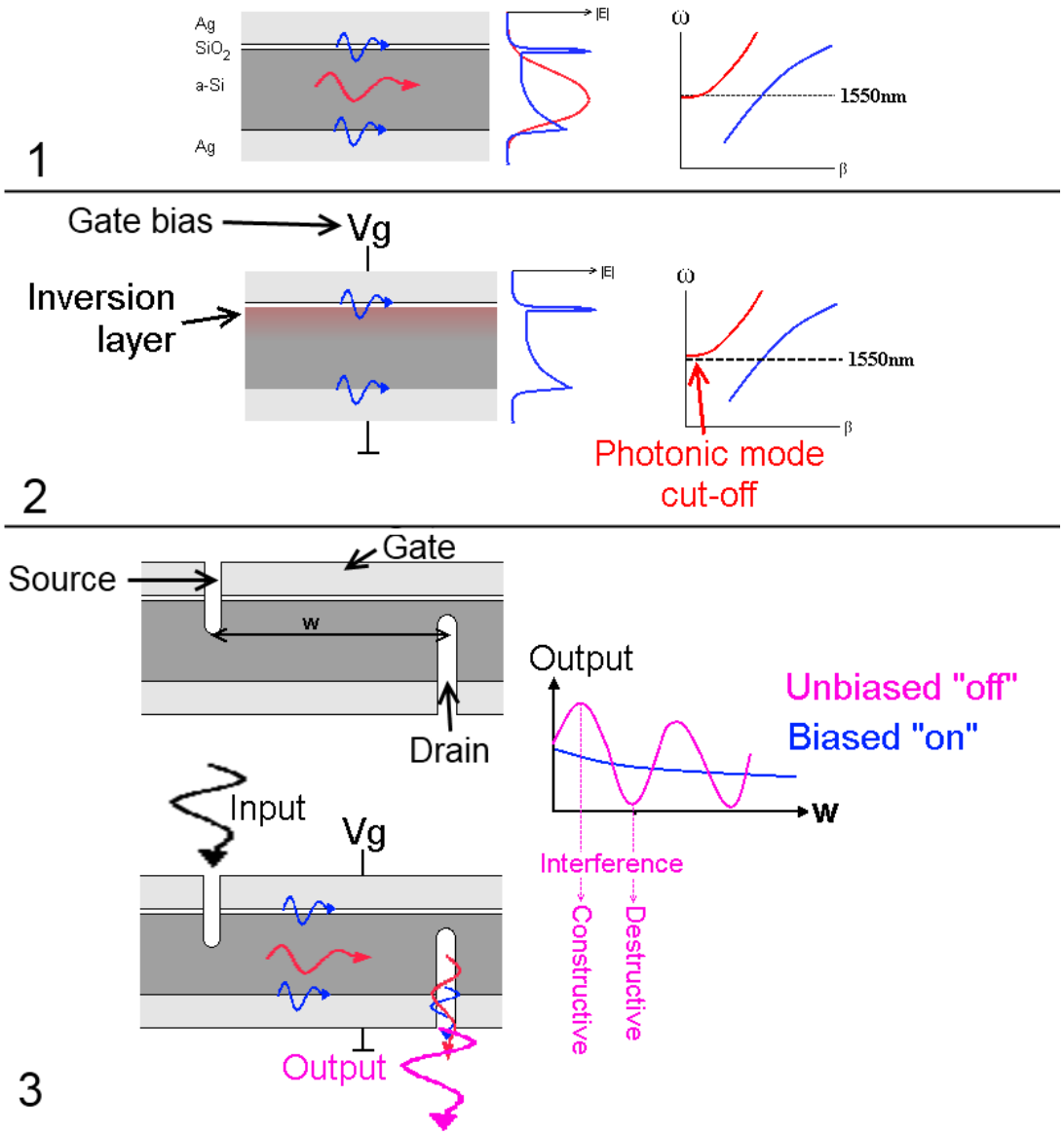


Figure 1.2: *Conceptual sketch of the plasMOSter and its mode of operation.*

1: *The plasMOSter layer stack which supports a propagating plasmonic**(blue)** and a photonic**(red)** mode. To the right of the layer stack, electric field distributions for the two modes are shown along with a photonic dispersion relation for the stack that shows how the photonic mode is just short of being unsupported by the structure for light with a wavelength of* 1550*nm.*

2: *The same layer stack except a positive bias is applied at the top metal layer. Just like in a MOSFET conductivity is increased significantly at the semiconductor/oxide interface. This inversion layer disrupts the photonic mode(red) more than the plasmonic(blue) since the photonic mode has a larger proportion of its field located at the inversion layer relative to the plasmonic mode which is localised at the metal interfaces.*

3: *Slits are etched on both sides of the layer stack with an individual distance* ***w****, representing a source and a drain. Light enters the device via the source slit, it then propagates to the drain slit as a photonic and a plasmonic mode at different speeds. At the drain both modes couple out and interfere constructively or destructively depending on the distance* ***w****.* ***w*** *is chosen so it causes destrucive interference. This means, that unless one of the modes are shut off the device will produce no output. As is was seen, this can be done by applying a gate bias, so the device will only produce a non-zero output if the device is supplied light at the source and a bias at the gate.*

However, to be a viable alternative to similar electronic or optical components, the plasMOSter should be easily implementable with other components on a large scale. The layered structure on Figure 1.2 can be deployed on any flat surface on any scale as will be shown later, but the source and drain design used here is more problematic. On an integrated circuit the light wont be coupled in and out perpendicularly as is the case here, but horizontally. In such a design, the *a-Si* wave guide will be connected directly to the wave guide, carrying the signal and the destructive interference will come from matching the length of the silver slabs as seen on Figure 1.3 instead of the two slits on Figure 1.2.

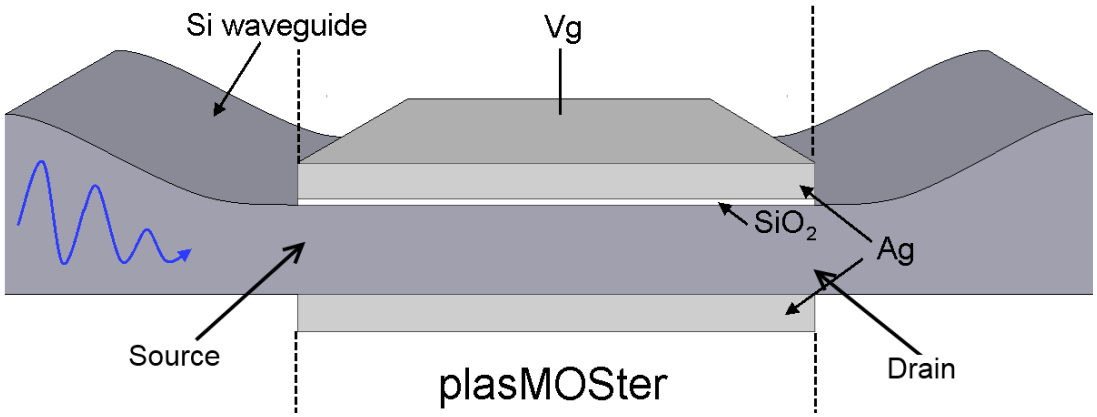


Figure 1.3: *PlasMOSter implemented onto a silicon wave guide as suggested by [5]. The design here works much like the one on Figure 1.2 except destructive interference at the output is determined by the finite width of the silver slabs. The wave guide is thicker outside the plasMOSter than inside, since the confinement of light in the plasMOSter which is essential to its operation, leads to high loss.*

The idea of using a MOS like structure for plasmonic modulation is not original, and has in fact been attempted elsewhere[5], but in that study, the silicon wave guide was crystalline and the fabrication was based on a non-scalable SOI process in which the substrate was removed locally to add the bottom conducting layer. This approach would be hard to implement in an integrated circuit fabrication process, where every process ideally takes place on one side of the substrate wafer. That being said, the plasMOSter fabricated here would benefit from the refractive and conductive properties of crystalline silicon as will be seen later.

2 PlasMOSter fabrication

In this study, the metal / insulator / semiconductor / metal stack was made using e-beam deposition. The source and drain slits were milled with Focused Ion Beam(FIB) and the silicon substrate was replaced with a stabilising layer of SU8 2100 photo resist on the opposite side of the layer stack. A chart describing the five steps in the process can be seen on Figure 2.1.

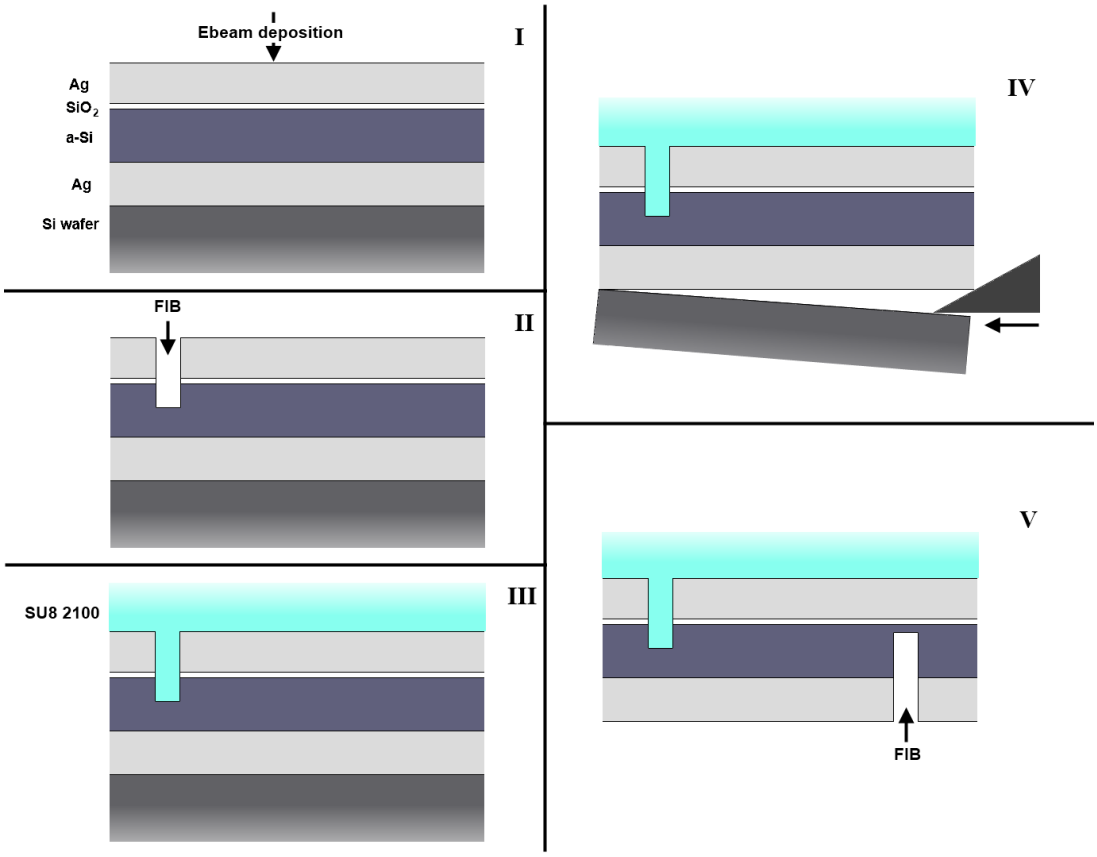


Figure 2.1: *Diagram of the different fabrication steps for producing a plasMOSter.* ***I****: E-beam sputtering is used to deposit a layer stack consisting of a silver, a-Si, SiO_2 and a silver layer on a silicon wafer piece.* ***II****: FIB is used to mill the source slit through the silver, SiO_2 and into the silicon layer.* ***III****: A thick layer of SU8 2100 is applied to act as stabilising layer instead of the silicon wafer.* ***IV****: The silicon wafer is broken off to gain access to the drain side of the plasMOSter.* ***V****: Finally, FIB is used to mill the drain slit.*

In this project e-beam sputter deposition was chosen over CVD to deposit silicon. E-beam deposition produces amorphous silicon and CVD may produce both amorphous and polycrystalline silicon. A CVD deposition on a silver surface would pollute the machinery which is unfavourable. In a laboratory setting this is problematic since it is used for various purposes. In a production setting such a machine would be

dedicated to fulfil that specific job.

2.1 E-beam deposition

The first step is building the layer stack on a silicon wafer. This can in principle be done in number of ways, each with their advantages and disadvantages. An important prerequisite, as already mentioned, to make this device viable is to be able to fabricate it using only scalable techniques. For deposition this include various CVD processes, RF, DC and e-beam deposition. The materials here considered are silver, silicon dioxide and doped silicon. Crystalline silicon deposition is somewhat difficult to obtain through scalable techniques, but allotropic forms might work just as well. Both amorphous*(a-Si)* and poly crystalline silicon can be obtained with CVD and amorphous silicon can furthermore be deposited using e-beam or RF deposition techniques.
Here, e-beam deposition was used for all layers. A CRYOFOX™ 600 Explorer was used which employs enough crucibles to make the entire layer structure in a single run. First, samples were prepared for characterisation of the properties of *a-Si*. *200nm* silver was deposited on a silicon wafer at a rate of *1 Å/s* . A layer of Boron doped *a-Si* was deposited on the silver layer at the same deposition rate and finally a layer of SiO_2 deposited at a rate of *1nm/s*. The *a-Si* thickness was monitored during the process using a built-in thickness monitor, based on the resonance frequency of a quartz crystal subject to the same deposition as the sample. The thickness is calculated through the change in resonance frequency, density of the sputtered material and the acoustic impedance or Z-value.
It is here worth noting that SiO_2 is an insulator and therefore relatively difficult to deposit using e-beam deposition. SiO_2 is not melted in the crucible as silver and silicon is but is evaporated directly from solid phase. This allows for electrons to accumulate on the surface which disrupts the process due to Coulomb repulsion. Sputter rate and therefore thickness is difficult to control. However, $20nm \pm 4nm$ was consistently obtained. The difficulties with SiO_2 could have been avoided by using RF sputter deposition instead. This was attempted, but an unresolved short circuit in the deposition chamber prevented its use.

The resulting stack was examined with ellipsometry and SEM. The ellipsometry was done after deposition of SiO_2 which act as a sealing layer preventing the *a-Si* from coming into contact with air. The *a-Si* from e-beam deposition is suspected of having an open structure with low density which would make it possible for air to form oxides far into the layer. Both ellipsometry and tilt corrected SEM measurements of *a-Si* suggested a layer thickness of $\sim 420nm$. An SEM scan of a cross section of the layer stack can be seen on Figure 2.2

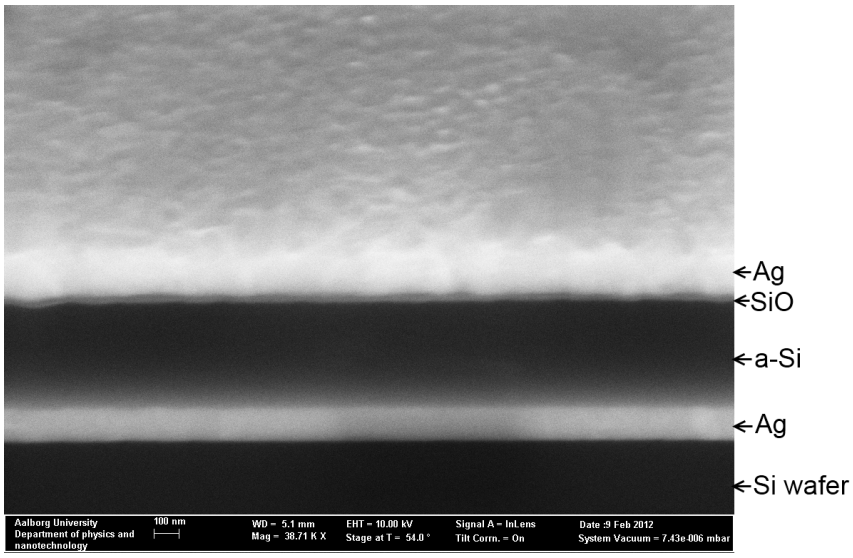


Figure 2.2: *SEM scan with tilt correction of a cross section of the layer stack that make up the plasMOSter. A thing of importance to notice here is the roughness at the SiO_2 / silver interface at the top. This is an unfortunate feature since surface plasmon propagation will certainly be hindered by this.*

2.2 Properties of E-beam sputtered a-Si

The *Ag / a-Si / SiO_2* stack was analysed using ellipsometric spectroscopy at VIS+IR wavelengths. The refractive properties of SiO_2 were taken to be well known but with unknown thickness. The *a-Si* thickness and properties waere unknown so the ellipsometric data was used to fit the *a-Si* to the Tauc-Lorentz model[10]. The Tauc-Lorentz model uses 5 parameters to describe the complex permitivity. One of the Tauc-Lorentz parameters is the band gap, which for *a-Si* is expected to be around $1.5eV$[4]. With the addition of a layer of SiO_2 with unknown thickness the fitting becomes a near impossible task, so the measurements were carried out at three angles to provide enough data for the fit. The SiO_2 layer was fitted to be $\sim 18nm$ even though $10nm$ was attempted in the deposition. This is likely due to the previously mentioned difficulties with e-beam deposition of SiO_2 and too long feedback-delay between the thickness measuring and the shut-off mechanism in the instrument.

The Tauc-Lorentz model allowed for a good fit to the experimental data as can be seen on Figure 2.3 where the fit is plotted along with the raw data. The fitted data suggest a *band gap* around $1.40eV$ and the refractive index can be seen on Figure 2.4.

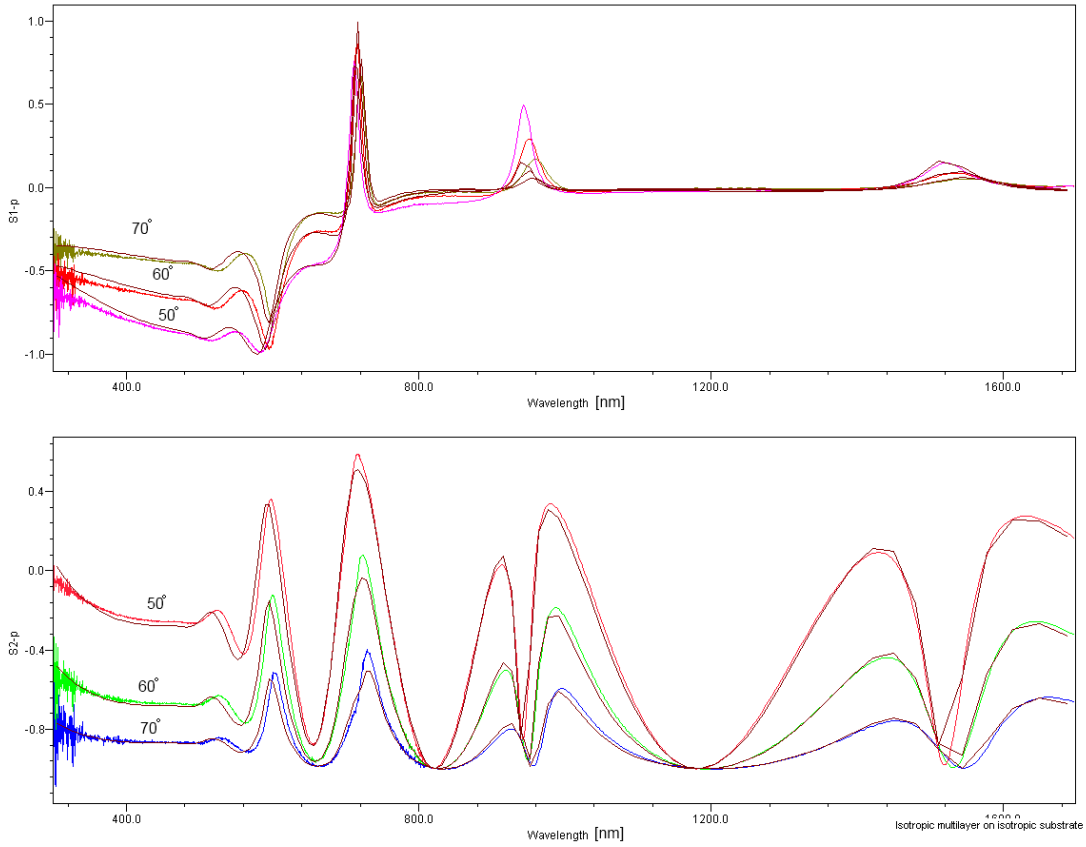


Figure 2.3: *Tauc-Lorentz fit(brown) and raw ellipsometry data* Ψ*(top) and* Δ*(bottom) at angles* 50°, 60° *and* 70°

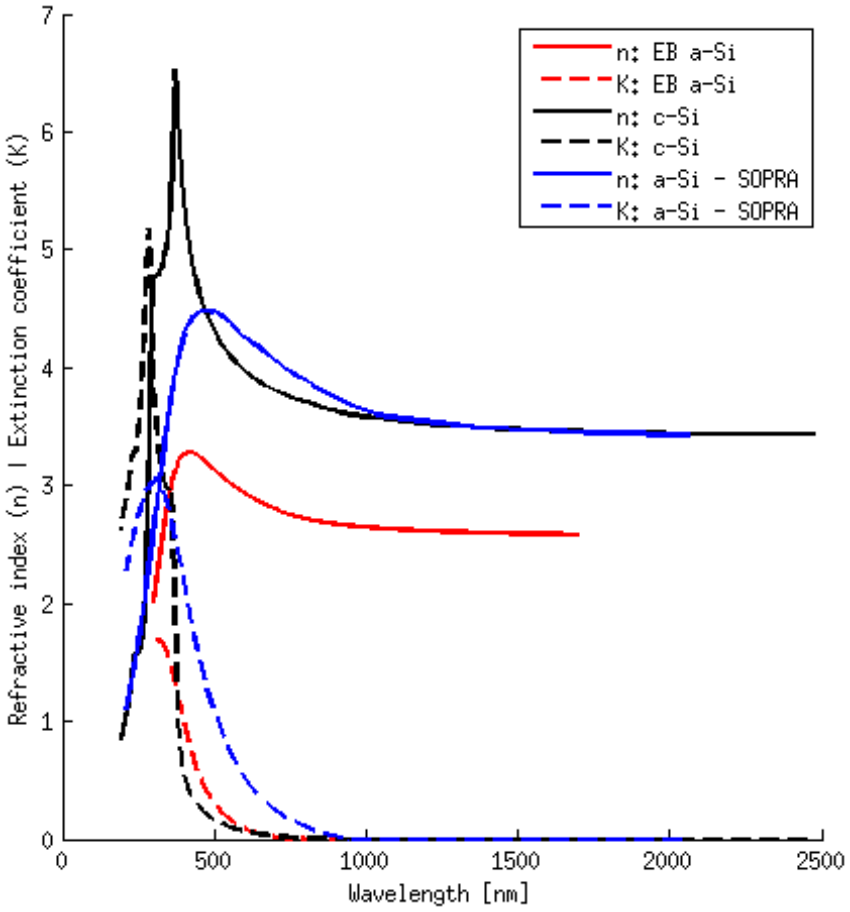


Figure 2.4: *Refractive index(solid) and extinction coefficient(dashed) of e-beam sputtered a-Si(red), crystalline Si(black) and a-Si according to SOPRA [22](blue).*
It is clear that the a-Si here produced has a much lower refractive index than the other allotropes of Si.

As can be seen on the figure, the refractive index of e-beam sputtered *a-Si* is much lower than that produced with CVD. It should here be mentioned that, the *a-Si* thickness provided by the e-beam evaporator was inconsistent with that obtained with ellipsometry. Notice also that the refractive index curve follows the same tendencies as that of CVD produced *a-Si*. It is therefore likely that the uniform shift down in refractive index is due to the e-beam sputtered *a-Si* being *less dense*. This also explains why the thickness measuring device did not put out the correct thickness as it was provided the wrong density.

However, higher refractive index is achievable with e-beam deposition. By pumping the deposition chamber for several days, the deposition process became much more stable and by using a lower deposition rate $< 1\text{Å}/s$ the refractive index became significantly higher without changing the band gap; see Figure 2.5.

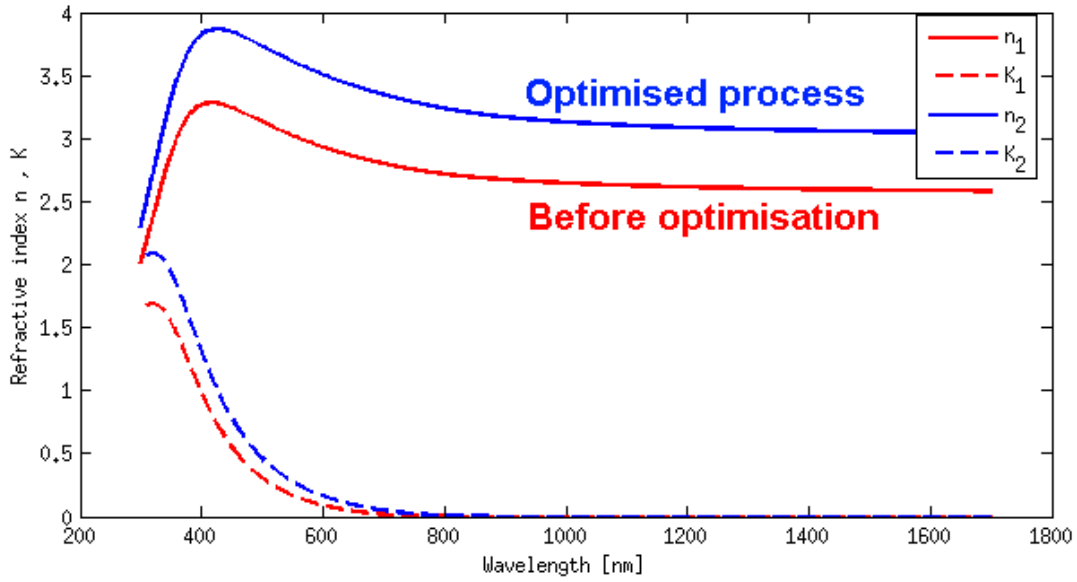


Figure 2.5: *Refractive index and extinction coefficients for a-Si produced under different conditions. Through careful deposition, the refractive index is raised by 0.5 with no significant increase in absorption for 1550nm radiation.*

These deposition parameters were not explored until after the plasmonic device had been fabricated and therefore the *a-Si* used in the rest of the study was of the low index type, shown on Figure 2.4.

2.3 Focused Ion Beam

Structures like the ones in this study are on a size scale that has been used by the micro processor industry for a long time. On a large scale, the source slits would be fabricated using projected photo lithography and eg. Reactive Ion Etching(RIE). Especially the photo lithography step is an expensive one. However, as long as the desired structure can be produced in a scalable way, we are not compromising with scalability by choosing another technique for this particular study. In this study, Focused Ion Beam(FIB) is used. In many ways it resembles SEM since it uses a similar design where the electron source is replaced by a Gallium ion source. The main difference is, that FIB is destructive in nature. FIB produces very narrow channels by default as seen on Figure 2.6

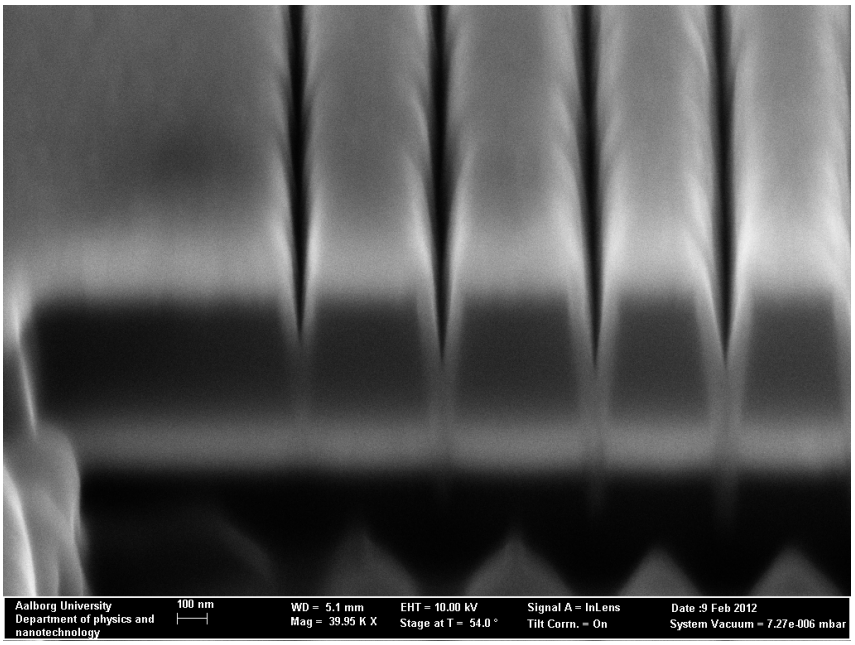


Figure 2.6: *Tilt corrected SEM scan of a cross section showing four slits that have been milled into the Ag/a-Si/SiO_2/Ag structure using FIB at different doses. The bright areas in the top and bottom of the picture are the silver layers*

It should be noticed that redeposition of material occurs durign FIB scans. On Figure 2.6 it is seen how silver from the top layer was redeposited onto the trench walls in the *a-Si* layer during FIB milling. This is of course unwanted, since silver is virtually impenetrable to IR radiation, and the redeposited silver along with the narrow slit will prevent light from entering the *a-Si* wave guide layer. This was fixed by bringing the FIB slightly out of focus, thereby widening the peak exposure spot. Redeposition into the trench was significantly lowered this way and the trench became more trapezoid in its shape. An SEM scan of a cross section can be seen on 2.7.

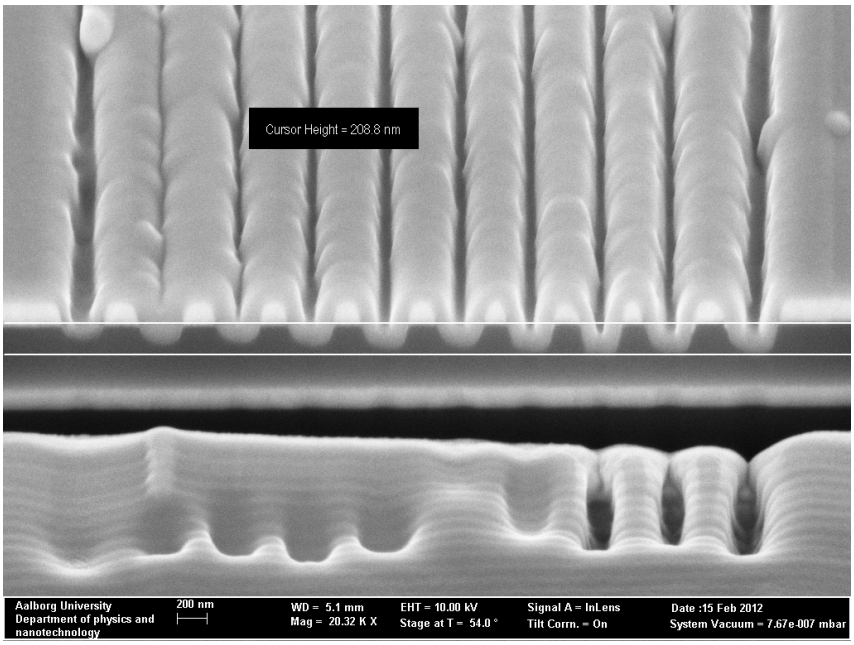


Figure 2.7: *Tilt corrected SEM scan of the layer stack with trenches milled with out-of-focus FIB at different exposures. The structure was covered in a thin layer of platinum to enhance contrast. Exposure settings for the trench second from right were chosen for the plasMOSter source slits due to its depth, width and shape.*

With the parameters in place, source slits were made and the result can be seen on Figure 2.8

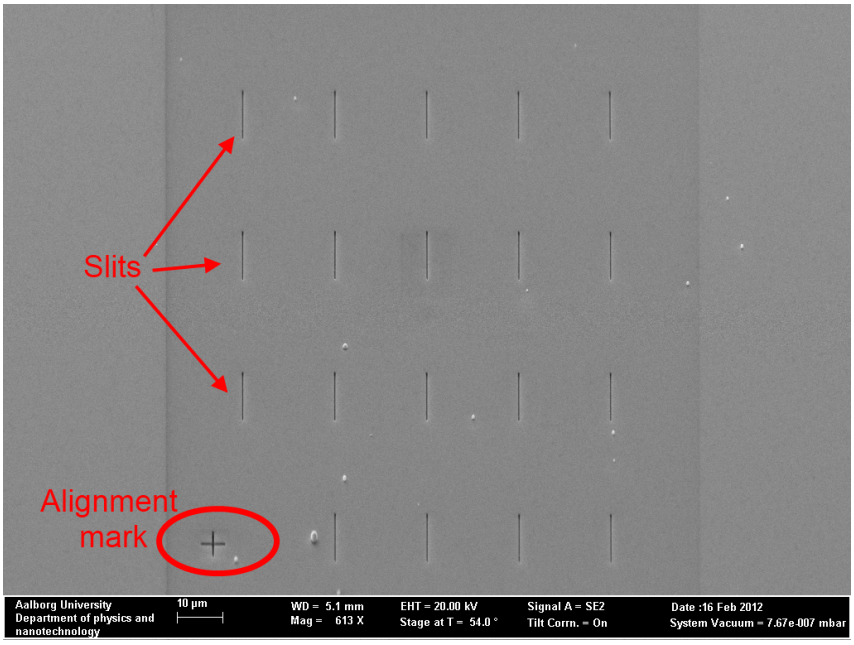


Figure 2.8: *SEM scan of one of four source slit arrays. The cross to the lower left is an alignment mark that is milled all the way through the layer stack and into the silicon wafer. The slits are* $10\mu m$ *long and are placed* $20\mu m$ *apart in bot directions. Four arrays like these were made* $1mm$ *apart using different exposure times.*

The drain slits were made in a similar fashion. After source slits were made the layer stack was peeled off the silicon wafer and turned around revealing the drain side of the stack. Unfortunately the peel-off had damaged the sample and only two of the four arrays remained somewhat intact. An overview showing the two remaining arrays on the damaged sample can be seen on Figure 2.9

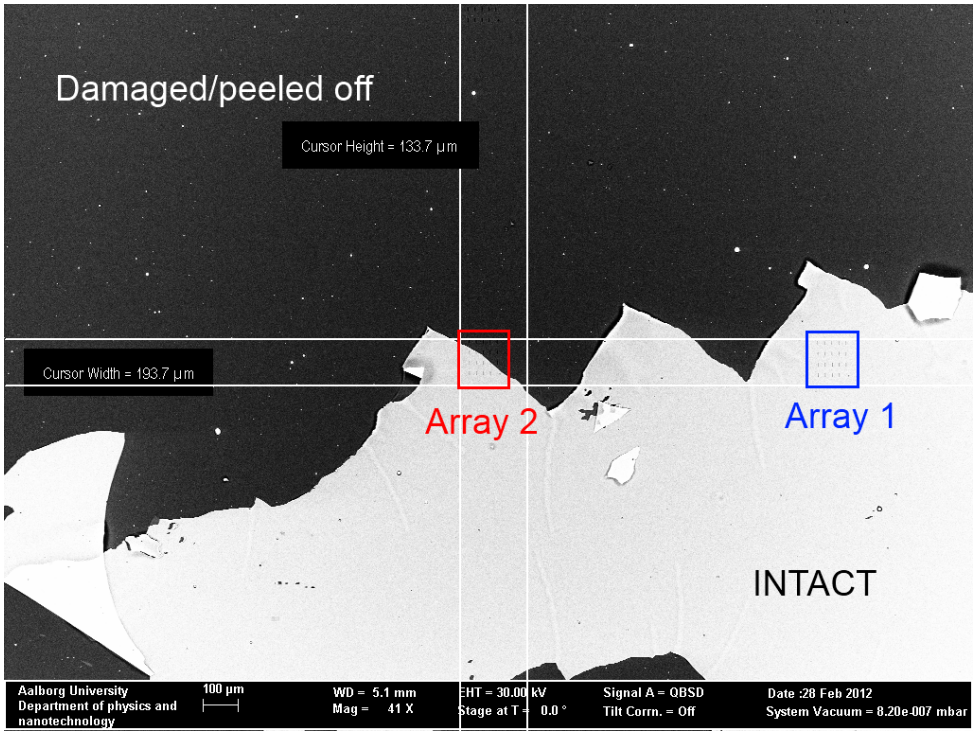
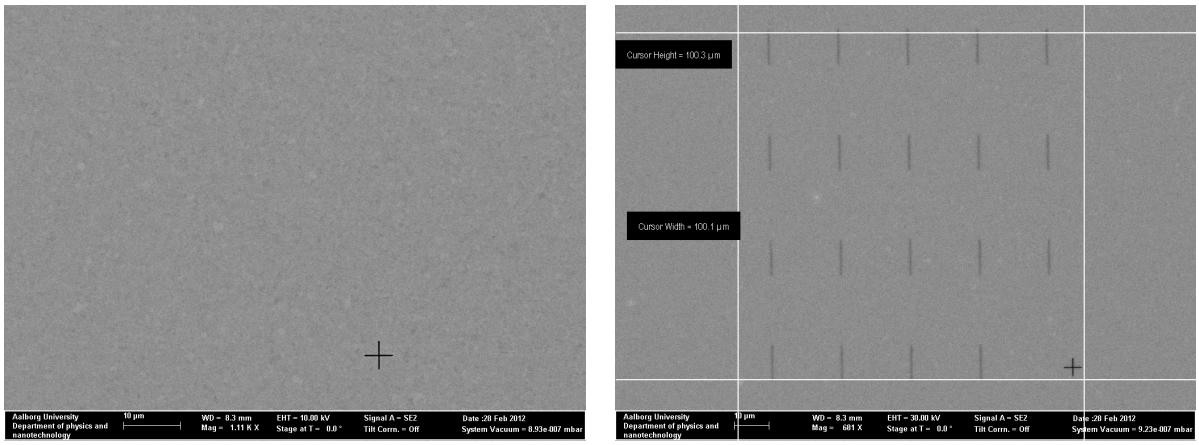


Figure 2.9: *SEM scan using a back-scatter detector showing an overview of the drain side of the sample after peel-off. The bright area is where the silver layer is intact. The array in the centre of the scan is only partially intact whereas the array to the far right is completely intact.*

The cross in Figure 2.8 was made as an alignment mark. As it is milled through all layers it should be visible from the other side. However, it is possible to detect the source slits from the drain side with the SEM. By turning up the acceleration voltage, the electrons penetrate deeper into the sample and can in fact visualise the underlying structure. This effect can be seen on Figure 2.10.



(a) (b)

Figure 2.10: *SEM scans of the array area, demonstrating the difference between acceleration energies of* ***a)*** $10keV$ *and* ***b)*** $30keV$.

A vital part in all lithography productions that have more than one step is aligning mask and structure. Here the structure is the source slits made visible by turning up the acceleration voltage of the SEM. The mask is defined by software, so alignment becomes a matter of providing the software with points of reference from which it can operate. Here, alignment marks like the cross highlighted on Figure 2.8 were placed around the sample with $2mm$ between them. These served to align the angle of the sample. The alignment cross at the array shown on Figure 2.8 served to align the drain array with the underlying source array since each source slit is defined by it position relative to the alignment cross.
The drain slits were then made with varying distance from the source slits and with slightly longer exposure. In the FIB setup used here, the sample had to be tilted in order to perform FIB milling. This caused the sample to slowly drift. The drift was reduced by aligning the sample and then leave it for two days allowing it to settle and then realign. The resulting arrays can be seen on Figure 2.11 and 2.12.

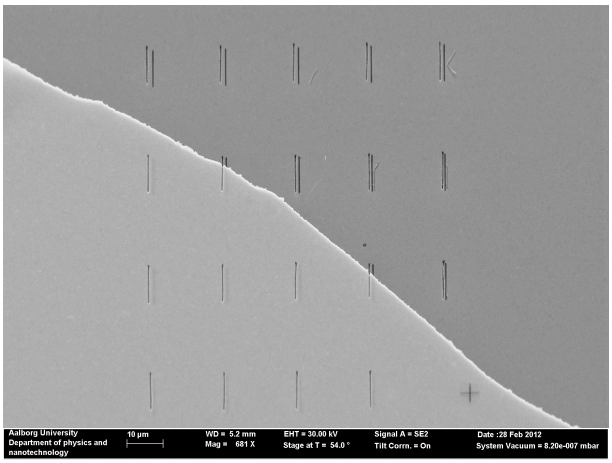


Figure 2.11: *SEM scan of the partially destroyed array. The top right area has no silver layer, and maybe no a-Si layer either. This could however not be conclusively confirmed with Energy-dispersive X-ray spectroscopy(EDX), which was attempted. In the upper right part of the scan where the silver is removed, the source slits are clearly seen as vague lines with varying distance to the drain slits.*

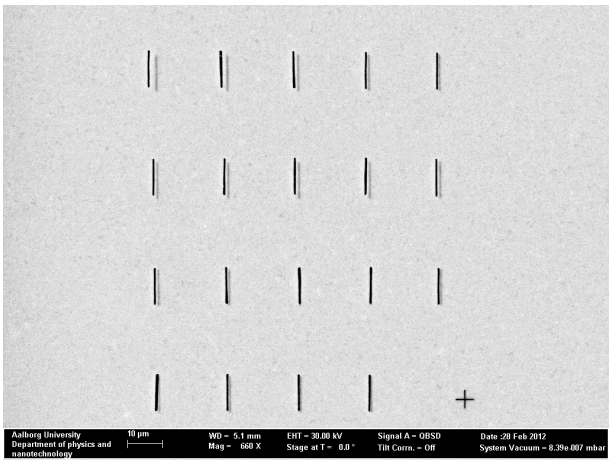


Figure 2.12: *SEM scan of the intact array. Back-scatter detector is here used as it better reveals the underlying source array compared to Figure 2.11. The source-drain distances are the same as those used for the array on Figure 2.11*

The final source-drain distances were determined through inspection of the SEM scans after the slits were made, since the drift made it difficult to create an entire array of drain slits with a predetermined distance to the underlying source slits. On Figure 2.13, a close-up, used for source-drain distance determination, can be seen.

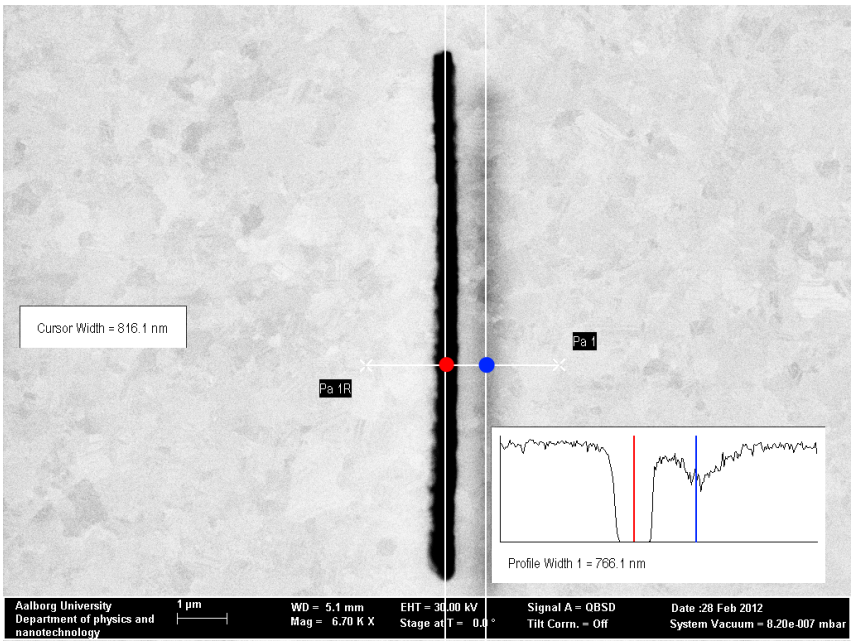


Figure 2.13: *SEM scan using back-scatter detector, showing a close-up of a drain slit with the location of the underlying source slit clearly visible to its right. The inset shows scan signal across the two slits and was used to estimate their relative spacing.*

2.4 Ultra thick resist

Clearly, the drain slit should be made during the deposition of the metal/semiconductor layers. Ways to achieve this in a scalable way will be discussed later. In this study, the layers were peeled off the silicon wafer mechanically. The layer structure is less than a micron thick so this was achieved by applying a very strong IR transparent material to the source side of the layer structure.

Here, a thick layer of SU8 2100 photo resist was used. This is a very viscous negative resist normally used in MEMS, which can produce thermally and chemically stable films with thickness's around $300\mu m$. At that point, source slits had been produced using FIB. These slits were very narrow and to avoid unpredictable behaviour, like light scattering, due to partial filling of the source slits, a layer using a diluted version of the SU8 2100 was used initially. After the sample had been prepared with an adhesion promoter; hexamethyldisilazane(HMDS), the sample was spin-coated with the diluted resist which should provide good filling of the source slits. After soft baking for 1 minute the sample was exposed to UV-light for 1 minute. The resulting resist was post exposure baked to reduce stress and the thickness was measured to be $2-3\mu m$.

The SU8 2100 was spin-coated onto the first layer at $1500rpm$. The sample was soft baked for 90 minutes at $95°C$. Because the wafer piece was $5\times 5mm^2$ the resist formed a dome shaped liquid drop during pre bake. This is unwanted, since a light signal will experience different angles of incidence across the wafer. This was solved in the exposure step where the sample was place face down on a glass plate while the resist was still warm from the soft bake. As the resist solidified it obtained a uniform thickness where

it was in contact with the glass plate. The sample was then exposed to UV light for a total energy amount of $500 mJ/cm^2$, measured on the sample side of the glass, over 10 minutes. Finally the sample was baked for 10 minutes at $95°C$ for 10 minutes to reduce stress. The resulting resist had a thickness of $\sim 0.5mm$ where it had been in contact with the glass.

2.5 Peel-off

To make the drain side accessible for the FIB, the silicon wafer must be removed at the slits. Initially *KOH* was used to make an anisotropic etch through the entire wafer leaving only a silicon frame for stabilisation. Unfortunately, this process is very slow at room temperature and may take days. Bobble formation further slows down the process giving rise to an uneven etch, so extensive stirring is needed. Turning up the heat, increases the etch rate significantly, but also the formation of bobbles. This method was approached in several ways, but the fragile layer stack was damaged every time, either by the powerful stirring, surface tension of the bobbles or heat induced stress. This approach was therefore eventually abandoned and the layer stack was instead mechanically cleaved off the silicon wafer. This *peel-off* was done as illustrated on Figure 2.1:***IV*** by driving a scalpel in between the ultra thick resist and the silicon wafer at the edge of the sample. From Figure 2.2 it is clear that the silicon wafer/silver is clearly the smoothest interface in the layer stack which is probably why it has the weakest adhesion, and hence is most likely to let go compared to the remaining interfaces.

3 Dispersion engineering and optimum structure simulation

3.1 Layer stack with engineered photonic dispersion

The design process essentially follows five steps, which are visualised in Figure 3.1.

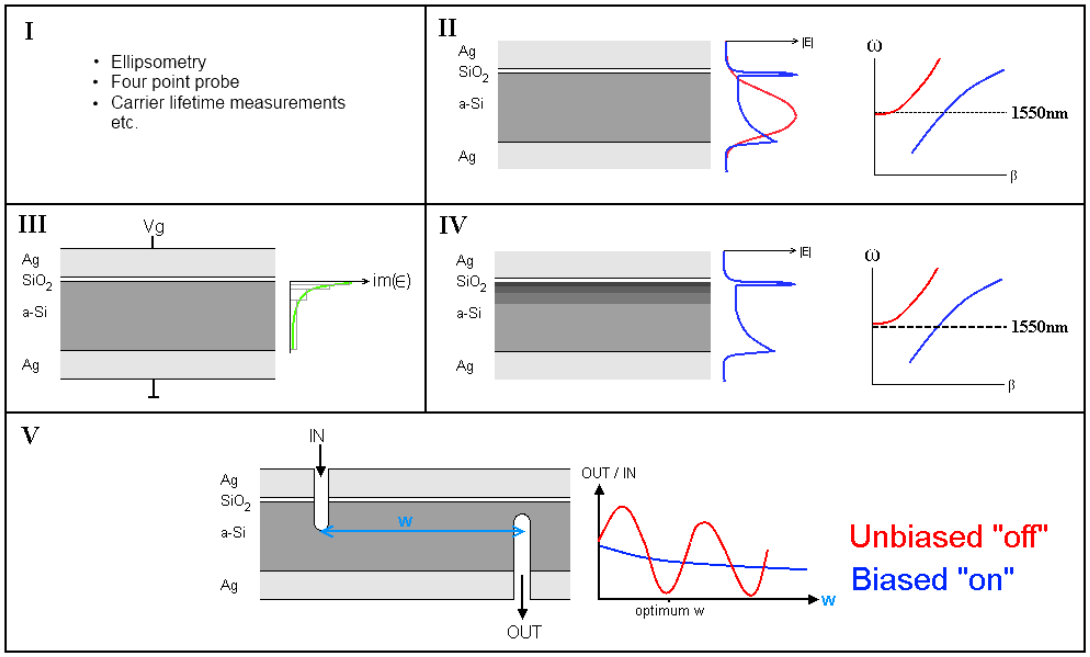


Figure 3.1: *Conceptual outline of the five steps in the design process.* ***(I)****: Material properties are obtained experimentally or through theoretical approaches.* ***(II)****: Photonic dispersion calculations are used to find the optimum thickness for the layers.* ***(III)****: Complex permittivity profile is calculated for an applied gate bias. The complex permittivity profile is split up into intervals of average permittivities.* ***(IV)****: The intervals from step (III) are turned into layers and of constant permittivity representing the refractive index profile for the system under an applied gate bias. Photonic dispersion is calculated to confirm that the photonic mode indeed goes into cut-off where it is no longer supported.* ***(V)****: A 2D model with appropiate source and drain slits is created and the ratio between output and input light intensity is calculated for various slit separation widths. The optimum separation width is a width that produces destructive interference between the photonic and plasmonic mode.*

First the material properties for the materials used must be obtained experimentally or through calculations. Next, photonic dispersions are calculated for the layered metal/oxide/semiconductor/metal structure. The metals are taken to be semi-infinite and only the two remaining layer thickness's need to

be optimised. 1550*nm* radiation is effectively screened for silver slabs thicker than 100*nm* so semiinfinite slabs should be a good approximation since the fabricated plasMOSters have a silver thickness of $\sim 200nm$. The optimisation criterion is a structure that supports a plasmonic and a photonic mode and where the photonic mode is close to cut-off for the operation wavelength. Step three is to use the structure from step two to calculate the electron and hole concentration profiles across the semiconductor with a gate bias applied, which is then used to calculate a new complex permittivity profile for the semiconductor which varies across the structure. The new permittivity profile is then turned into representative layers of constant permittivity. These layers of constant permittivity then represent the semiconductor with a gate bias applied. A photonic dispersion is then calculated to confirm that the increased light absorption causes the photonic mode to go into cut-off. Fourth step is to calculate the ratio between input and output light intensity r_{io} as a function of source-drain slit separation width. The optimum width is the width that produces the highest difference in r_{io} when the plasMOSter is switched between on and off.
The final structure dimension is thus obtained and the device should be fabricated with the thickness's from step two and the source-drain separation from step 4. There is one important thing to beware of though. The shape and depth of the slits influences how the photonic and plasmonic modes interfere at the drain and should be optimised as well. Since the source and drain slits are quite narrow it may be necessary to figure out which shapes and depths can be produced with the fabrication process, and then run the simulations for optimisation of source-drain separation using these.

Photonic dispersions

The photonic and plasmonic modes of interest are electrical and magnetical field component distributions, that are solutions to a wave equation. Here, that equation is the Helmholtz equation which is derived from Maxwell's equations.
The derivation of the Helmholtz equation and the field component equations to be solved can be found in appendix A on page 53. If the coordinate system is chosen so that z is normal to the layers and x is the direction of propagation then only transverse magnetic(TM) modes allow for propagating surface plasmon modes[16]. The TM mode wave equation is given as

$$\frac{\partial^2 H_y}{\partial z^2} + \left(k_0^2 \varepsilon - \beta^2\right) H_y = 0 \tag{3.1}$$

which provides H_y for waves propagating in the x-direction on the general form

$$H_{yi} = A e^{i\beta x} e^{k_i z} \pm B e^{i\beta x} e^{-k_i z} \tag{3.2}$$

which is a superposition of two solutions to equation (3.1), where $k_i^2 = \beta^2 - k_0^2 \varepsilon_i$, and i is a layer index. The $\pm$ indicates a symmetric and an antisymmetric solution. Equation (3.2) can be combined with the

remaining TM component equations

$$E_x = \frac{-i}{\omega\varepsilon\varepsilon_0}\frac{\partial H_y}{\partial z} \tag{3.3}$$

$$E_z = \frac{-\beta}{\omega\varepsilon\varepsilon_0}H_y \tag{3.4}$$

to yield

$$E_{xi} = \frac{-ik_i}{\omega\varepsilon\varepsilon_0}\left(Ae^{i\beta x}e^{k_i z} \mp Be^{i\beta x}e^{-k_i z}\right) \tag{3.5}$$

$$E_{zi} = \frac{-\beta}{\omega\varepsilon\varepsilon_0}\left(Ae^{i\beta x}e^{k_i z} \pm Be^{i\beta x}e^{-k_i z}\right) \tag{3.6}$$

which must be evaluated in each layer interface using continuity of D_z and E_x. Furthermore, only modes confined to the wave guide are of interest, so all fields are taken to be evanescent in the metals. This means A is zero for the top metal layer and B is zero in the bottom metal layer. Matching the field component equations at the boundaries gives a linear system of homogeneous equations. Solving such a sytem for the coefficients A and B can be done by simple substitution. For a metal-insulator/semiconductor/metal structure, an analytic expression is obtainable for the β and ω relation. With the addition of an additional layer, as in the plasMOSter, an extra two equations and coefficients are introduced and an analytical expression is hardly obtainable. Instead the system of equations can be evaluated in a numerical way. First, the system of linear homogeneous equations is reformulated as a matrix problem

$$\bar{\bar{M}}\bar{x} = 0 \tag{3.7}$$

where $\bar{\bar{M}}$ is a $n \times n$ matrix with complex entries and $\bar{x}$ is a vector of length n containing the coefficients A_i and B_i. Since we are not interested in the trivial solution $\bar{x} = \bar{0}$ the determinant $\det(\bar{\bar{M}}) = 0$. The determinant is calculated for an interval of complex valued β. The resulting determinants are complex valued and most likely nonzero. Since both the imaginary and real part of the determinant must be zero, one can use a Newton-Raphson based algorithm or plot out the contours at zero for the imaginary and real parts of the determinants against the real and imaginary parts of β. A plot like this can be seen on Figure 3.2 where the β we are looking for are the intersections of the real and imaginary contours of the determinant, which can be directly determined through examination of the plot.

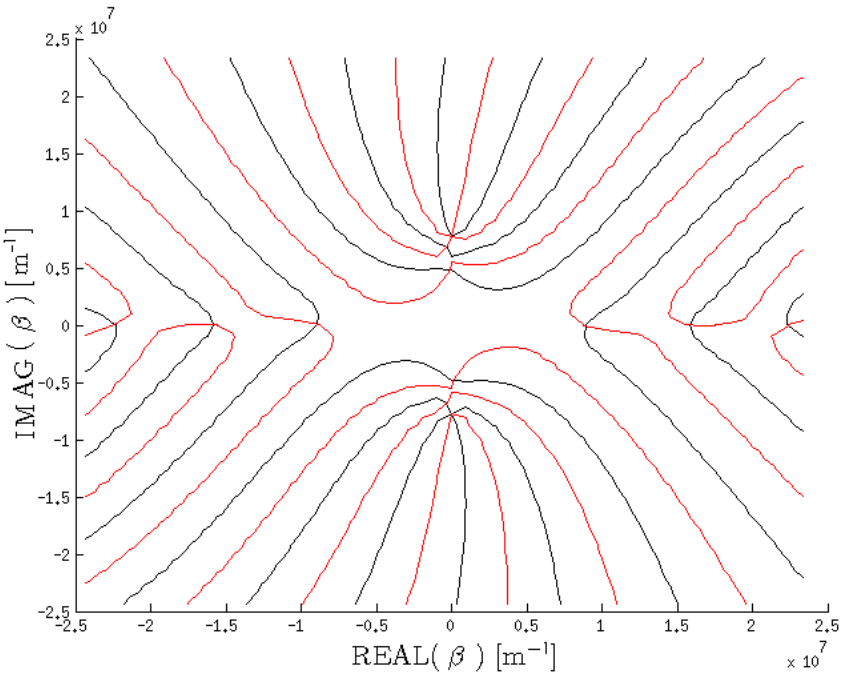


Figure 3.2: *Contour plot at zero for a plasMOSter structure. The curves are the real**(black)** and imaginary**(red)** part of the determinant. The real and imaginary parts of* β *can be directly determined through inspection of the intersections.*

To be able to plot the fields we need the coefficients contained in $\bar{x}$. To determine the coefficients contained in $\bar{x}$ we must find the null space for $\bar{\bar{M}}$. This can be done through singular value decomposition(SVD). The Singular Value Decomposition Theorem tells us that[14]

Let A be an $m \times n$ matrix with rank r. Then there exists an $m \times n$ matrix Σ

$$\Sigma = \begin{pmatrix} D & 0 \\ 0 & 0 \end{pmatrix} \tag{3.8}$$

for which the diagonal entries in D are the first r singular values of A, $\sigma_1 \geq \sigma_2 \geq ... \geq \sigma_r \geq 0$, and there exist an $m \times m$ orthogonal matrix U and an $n \times n$ orthogonal matrix V such that

$$A = U\Sigma V^T \tag{3.9}$$

D presented here is an $r \times r$ diagonal matrix, which means that if A is an $m \times m$ matrix then the zero matrices do not appear and $\Sigma = D$. The diagonal entries of D are the eigenvalues $\sqrt{eig(A^T A)}$ in descending order.

The columns of V are called the *right singular vectors* of A and the columns of V which correspond to zero singular values form an orthonormal basis for the null space of A. Since the β we find requires $\bar{\bar{M}}$ to be singular through the condition $\det(\bar{\bar{M}}) = 0$ and the singular values of Σ are sorted so the zero singular

value is at the end, the null space basis vector is simply the last column vector in V if $\bar{\bar{M}}$ is a square matrix. The entries in the null space vector corresponds to the coefficients A and B in (3.5) and (3.6) for each layer.

In the plasMOSter design there are 3 boundaries each imposing a boundary condition on both A and B, leading to six equations and six coefficients A and B. The corresponding matrix $\bar{\bar{M}}$ is then a 6×6 matrix with complex entries.

For accurate results, one must sweep over large number of real and imaginary values of β, computing the complex determinant in each case. If the purpose is to compute photonic dispersions, as is the case with the structural optimisation of the plasMOSter, the calculations must be carried out for a range of structural parameters and preferably wavelengths. The scripting and computation time then quickly scales beyond a reasonable time scale. A photonic dispersion relation of a plasMOSter structure with an a-Si layer of *400nm* and SiO_2 layer of *20nm* can be seen on Figure 3.3

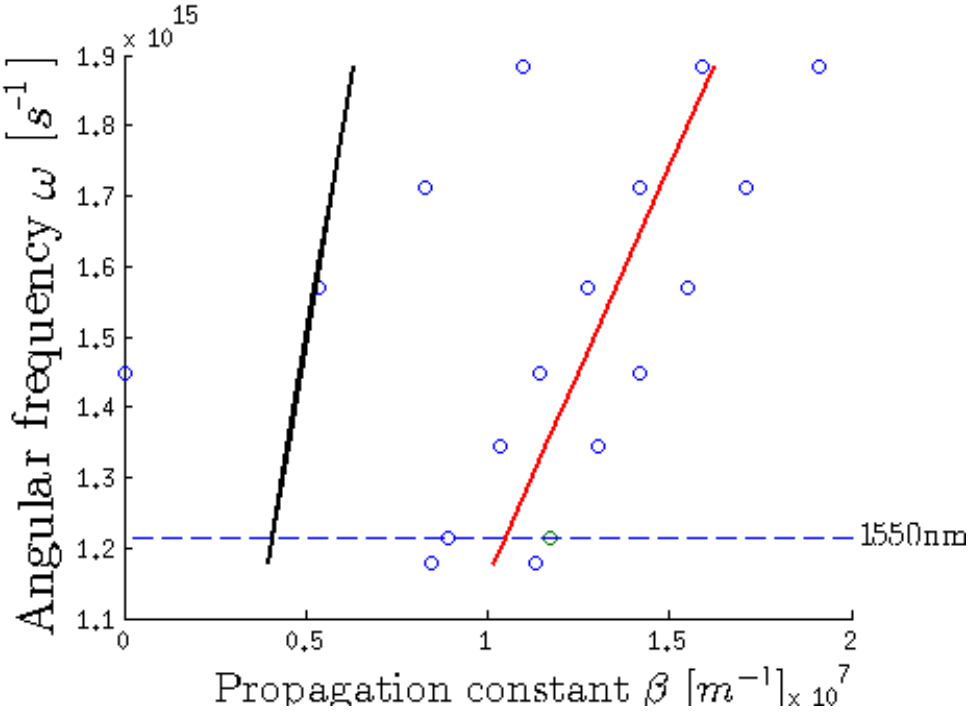


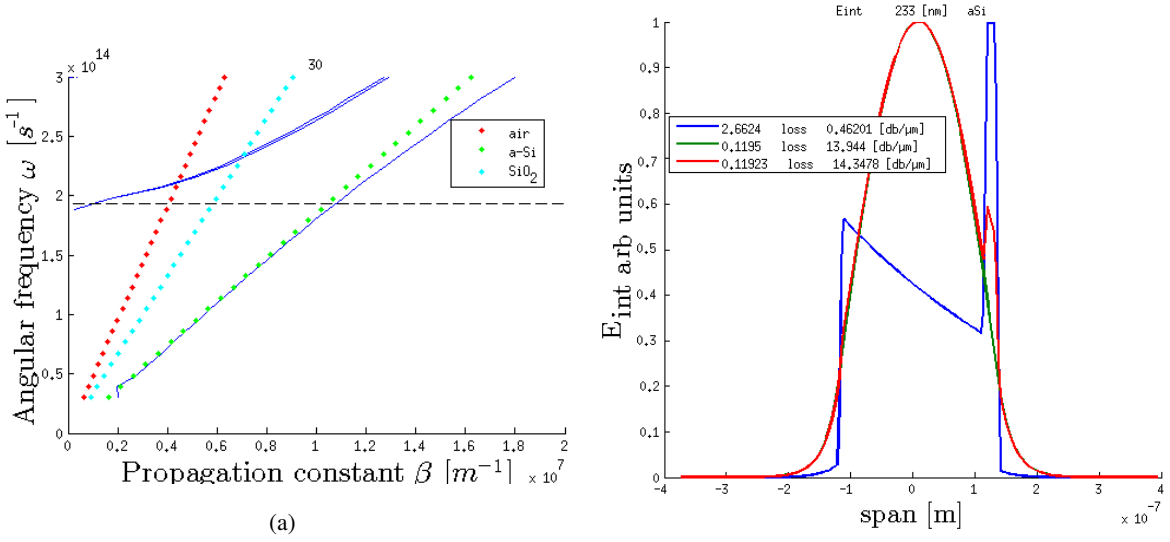
Figure 3.3: *Example of a photonic dispersion relation for TM-modes in a plasMOSter structure of 400nm a-Si, 20nm SiO_2 between two layers of gold. The values were found using inspection of plots like in figure 3.2. The black line is the vacuum light-line and the red line is the light line for a-Si. The dotted line indicates a wavelength 1550nm.*

It is clear that this makes up for a slow optimization process, but viable nevertheless. Unfortunately this becomes increasingly difficult as the response to a gate bias is needed. Even if the refractive index profile of a biased plasMOSter is divided into discrete layers, since each additional layer adds two coefficients and two boundary conditions that needs to be solved for.

Therefore, we must abandon this approach. An alternative approach, that is not so sensitive to the addition of layers is *finite element analysis*. This approach divides the structure into a finite element mesh,

where properties varies linearly between the grid points. This makes this type of analysis insensitive to property variations, but using a mesh dense enough to properly imitate, for instance exponential behaviour, is crucial. Fortunately, several sofware interfaces have been developed to perform finite element analysis in various application areas. In this project two such programmes have been used; Lumerical MODE for photonic dispersion simulations and COMSOL Multiphysics 4.2 for computation of refractive index under applied bias and 2D simulations of the plasMOSter performance.

The idea here is to engineer the plasMOSter so the plasmonic modes are only weakly affected compared to the photonic modes when an electric bias is applied. This amounts to producing a photonic dispersion relation plot like in picture *II* on Figure 3.1 on page 19, where the photonic mode is just short of being disallowed. Lumerical MODE™solutions were scripted to compute photonic dispersion relations for a number of *a-Si* thicknesses. The thickness of SiO_2 was kept at 20*nm* throughout the project for the experimental reasons given on page 6. The metal layers are silver which is taken to be semi-infinite and Perfectly Matched Layers(PML) are used to absorb fields propagating further than *200nm* into the silver layers. This is a safe assumption since we are dealing with infrared wavelengths in silver. The calculated photonic dispersion relations for a selected *a-Si* thickness of *233nm* can be seen on Figure 3.4.



(a) (b)

Figure 3.4: *Photonic dispersion relation* ***(a)*** *and normalised electric field profile* ***(b)*** *for a plasMOSter using silver cladding, 20nm SiO_2 and 233nm a-Si.*
As seen on ***(a)*** *the a-Si wave guide thickness is chosen so that the photonic mode is very close to cut-off for 1550nm light, which is also why the loss is so significant for these modes on figure* ***(b)****.*

As the field distribution in Figure 3.4 shows, the majority of the field for the photonic mode lies in the *a-Si* layer. This means that this mode will be more sensitive to changes to the refractive of this layer than the plasmonic mode, also depicted in Figure 3.4.

3.2 Electron-hole dispersion simulation

The idea here is to locally alter the refractive index of the silicon in a MOS structure. Applying a bias to the metal changes the conductivity by creating an inversion channel in the semiconductor at the insulator interface. This local change in conductivity can be several orders of magnitude higher than that of the bulk semiconductor. Needless to say, this will have a noticeable effect on the frequency dependent permittivity $\varepsilon(\omega)$ through[23]

$$\varepsilon(\omega) = \varepsilon' + \frac{i\sigma_0}{\omega} \tag{3.10}$$

where ε_0 is the vacuum permittivity, ε' is the real part of the permittivity and σ_0 is the DC conductivity. Since the material in question is a semiconductor, the charge carriers can be both holes and electrons. σ_0 therefore depends on both the local concentration of holes (p) and electrons (n) and their respective mobilities μ_h and μ_e.

$$\sigma_0 = q(n\mu_e + p\mu_h) \tag{3.11}$$

where q is the elementary charge and the mobilities depends on the effective mass m^* and lifetime of the respective charge carrier through the relation

$$\mu = \frac{q\tau}{m^*} \tag{3.12}$$

So to describe the change in refractive index $\tilde{n} = \sqrt{\varepsilon}$ we need values for electron and hole lifetime, effective masses and concentrations. For crystalline materials, this would normally include calculation of the of the electronic dispersion and through that the effective mass components for electrons in the conduction band E_c and holes in the valence band E_v, using[11]

$$\frac{1}{m^*_{\mu\mathbf{v}}} = \frac{1}{\hbar}\frac{d^2E_{c,v}}{dk_\mu dk_\mathbf{v}} \tag{3.13}$$

where μ, $\mathbf{v}$ are Carteisan coordinates, that takes into account that effective masses are often anisotropic for crystalline materials.

3.2.1 Electronic dispersion

If the material in consideration is amorphous this otherwise comprehensible task becomes very tricky. Instead of using a small unit cell, one has to use a huge supercell, where the atomic structure is determined using ab initio molecular dynamics(MD) or Monte Carlo(MC) techniques. The ab initio MD approach starts with liquid silicon and then allows it to cool into its amorphous structure. In this type of MD simulation the ionic forces are derived directly from DFT calculations of the electronic ground state at each time-step[26][3]. Still the problem is by no means simple and computational cost of increasing the number of atoms in the super cell is high. Furthermore, since time stepping is computational costly the simulated liquid is usually condensed to its amorphous state in a matter of picoseconds. Going from approx. $1800K$ to $300K$ in that short period of time may cause the atoms to arrange in an unstable conformation. Sometimes this problem is addressed by simulating several reheating and cooling allowing the structure to settle in more stable conformations.[26] When a satisfactory configuration is obtained, the physical properties can be extracted.
Alternatively, electronic properties can be obtained experimentally. The carrier lifetimes can be obtained by measuring how the transmittance of infra-red changes as another chopped light source excites charge carriers at different chopping frequencies[7]. Here the absorption coefficient of the semiconductor responds to an increase in conductivity (like in equation (3.10)) caused by excitation of charge carriers i.e. photoconductivity. When excitation light is on, the transmittance decreases to a certain level and when the chopper shots off the excitation light, the transmittance drops to its initial level at a rate determined by its charge carrier lifetime. The spectrometer measures the average intensity, which now depends on the chopping frequency and carrier lifetime. It will for instance be lowered if the carrier lifetime is short since transmittance will drop faster during "dark" periods.
Later an alternative PLASMONSTER device design will be proposed based on the current one except it will be modulated by a UV signal instead of an electric one, much like in this photoconductivity experiment.
However, neither the described theoretical or experimental approaches on amorphous silicon are within the scope of this particular project, and the values for carrier lifetime used in the simulations has been found elsewhere[28].

3.2.2 Charge carrier distributions

Next step is to calculate the charge carrier distributions in the MOS structure.
The particles of interest are holes and electrons. The study of their behaviour under an applied electrostatic bias is governed by three coupled equations. First the Poisson equation

$$\nabla^2\psi(\vec{r}) = -\frac{\rho(\vec{r})}{\varepsilon\varepsilon_0} \tag{3.14}$$

which describes the relationship between the electric potential $\psi(\vec{r})$ and charge density ρ. The charge density depends on electron, hole and ionized impurity concentrations and takes the form

$$\rho = e(p - n + N) \tag{3.15}$$

Where p is the positive charge due to holes, n is the negative charge due to electrons and $N = N_d - N_a$ is the charge contribution from ionised donors N_d and acceptors N_a. The variables of course depend on their position in space like equation (3.14). The notation has been left out in most of the chapter for simplicity. In a moderately doped semiconductor at room temperature, it can safely be assumed that the concentrations of ionised donors and acceptors are the concentrations of the impurities themselves, since the ionisation energies are low compared to the thermal energy.

In equilibrium there is no net charge and from equation (3.15) it follows that

$$N = n_0 - p_0 \tag{3.16}$$

When an electric potential is present, the energy bands are bend accordingly and the concentrations are affected as

$$n = n_0 e^{\frac{e\psi}{k_B T}} \tag{3.17}$$

$$p = p_0 e^{-\frac{e\psi}{k_B T}} \tag{3.18}$$

Equations (3.14), (3.17) and (3.18) are the governing equations and can be collected into a single expression

$$\nabla^2\psi = -\frac{e}{\varepsilon\varepsilon_0}\left[p_0\left(e^{-\frac{\psi}{k_B T}} - 1\right) - n_0\left(e^{\frac{\psi}{k_B T}} - 1\right)\right] \tag{3.19}$$

In the MOS, or more correctly metal-oxide-semicondoctor-metal structure here considered, the Shottky barrier at the metal/semiconductor interface provides an influential boundary condition which has to be considered.

Carrier statistics

In an intrinsic semiconductor at ambient temperatures, assuming spheric parabolic bands and that the Fermi distribution can be approximated to a Boltzmann distributiion, the electron and hole concentrations

are given by the general expressions

$$n = \bar{N}_c e^{\beta(E_F - E_C)} \tag{3.20}$$

$$p = \bar{N}_v e^{\beta(E_V - E_F)} \tag{3.21}$$

where $\beta = \frac{1}{k_B T}$, E_c and E_v are the energies of the conduction and valence band edges respectively, E_F is the Fermi level and $\bar{N}_c$ and $\bar{N}_v$ are effective density-of-states which are weighted summations over all states in the respective band and depends on the effective mass at the band edges

$$\bar{N}_c = 2\left(\frac{m_c^* k_B T}{2\pi\hbar^2}\right)^{3/2} \tag{3.22}$$

$$\bar{N}_v = 2\left(\frac{m_v^* k_B T}{2\pi\hbar^2}\right)^{3/2} \tag{3.23}$$

In an intrinsic semiconductor, every electron excited into the conduction band leaves a hole in the valence band, hence the concentrations equate and

$$n = p = n_i \tag{3.24}$$

$$\Downarrow$$

$$\bar{N}_c e^{\beta(E_{Fi} - E_C)} = \bar{N}_v e^{\beta(E_V - E_{Fi})} \tag{3.25}$$

$$\Downarrow$$

$$E_{Fi} = E_V + \frac{1}{2}E_g + \frac{3}{4}k_B T \log\left(\frac{m_v^*}{m_c^*}\right) \tag{3.26}$$

where E_{Fi} is the Fermi level for the intrinsic semiconductor and $E_g = E_C - E_V$. This shows that for an intrinsic semiconductor the Fermi level stays the same at all temperatures if $m_v^* = m_c^*$.
In extrinsic semiconductors the concentrations (3.20), (3.21) can be used in a modified form[1] multiplying by $e^{E_{Fi} - E_{Fi}}$

$$n = \bar{N}_c e^{\beta(E_F + E_{Fi} - E_{Fi} - E_C)} = n_i e^{\beta(E_F - E_{Fi})} \tag{3.27}$$

$$p = \bar{N}_v e^{\beta(E_V + E_{Fi} - E_{Fi} - E_F)} = n_i e^{\beta(E_{Fi} - E_F)} \tag{3.28}$$

In the semiconductor at thermal equilibrium far from interfaces the electric potential $\psi(\vec{r}) = 0$ the equilibrium electron and hole concentrations n_0 and p_0 can be expressed as[1]

$$n = \frac{1}{2}\left[N + \sqrt{N^2 + 4n_i^2}\right] \tag{3.29}$$

$$p = \frac{1}{2}\left[-N + \sqrt{N^2 + 4n_i^2}\right] \tag{3.30}$$

Using $N = N_d - N_a$, again assuming all impurities are ionised. These expressions are particularly useful in compensated semiconductors. However, in this study the semiconductor is an e-beam sputtered layer of Boron p-doped a-Si, which is assumed to have the same acceptor impurity concentration as the p-type silicon used as sputter substrate.

Heterostructures

When dealing with heterostructures with different electron affinities, it is often a good idea to introduce a reference point for the electric potential. The potential reference here chosen is the vacuum level. When an electric potential is present the bands are bent including the vacuum level which is shifted by $-e\psi$ as seen of figure 3.5.

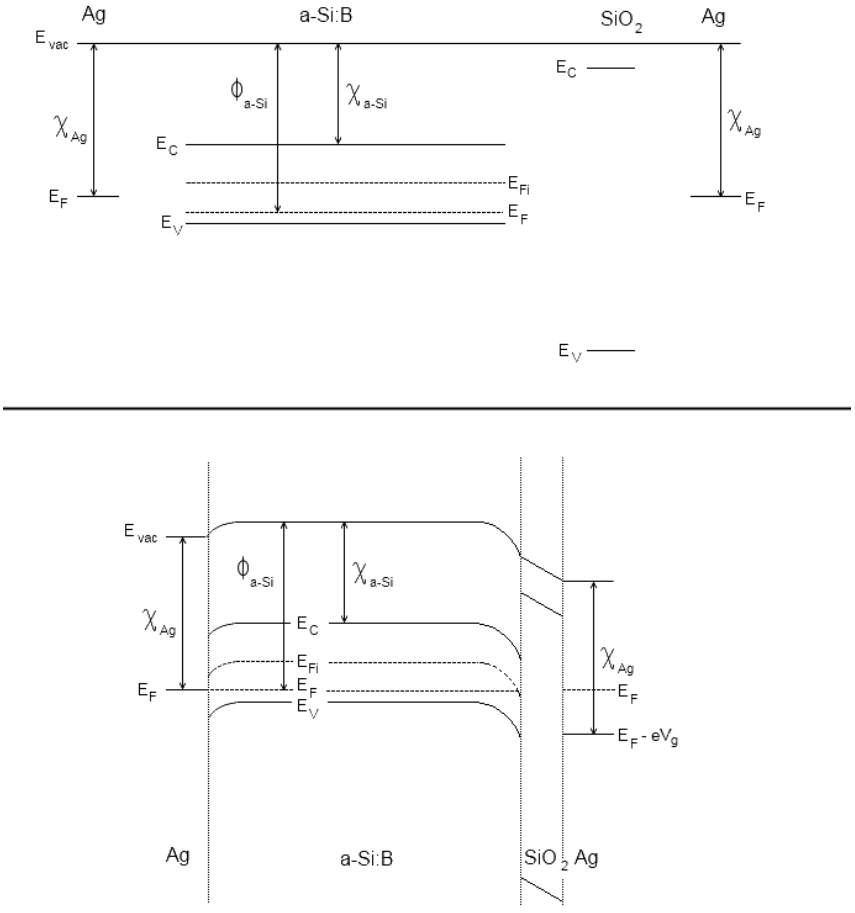


Figure 3.5: *Energy bands in the plasMOSter as the layers of different materials are brought together. In the top diagram the materials are far apart and no potentials are build up. In the bottom diagram, the layers are brought together, an electric bias has been applied at the gate electrode to the right and enough time has passed so that thermal the system is in thermal equilibrium. Several factors influence the bottom picture such as Boron concentration, gate potential and thickness of the oxide and a-Si*

Here we might want to consider the extrinsic semiconductor as an intrinsic semiconductor subjected to an innate bias ψ. If we assume the intrinsic Fermi level is in the middle of the band gap then the energy difference $E_F - E_{Fi}$ in equation (3.27) and (3.27) becomes

$$E_F - E_{Fi} = e\psi + \chi + \frac{E_g}{2} \tag{3.31}$$

Which of course has to produce the correct carrier concentrations at thermal equilibrium and no applied bias. So, by combining (3.31) with (3.27) and (3.29) we obtain an expression for the innate potential

$$\begin{aligned} \frac{1}{2}\left[N + \sqrt{N^2 + 4n_i^2}\right] &= n_i e^{\beta\left(e\psi + \chi + \frac{E_g}{2}\right)} \\ &\Updownarrow \\ e\psi &= -\chi - \frac{E_g}{2} + k_B T \log\left(\frac{\frac{N}{2} + \sqrt{\frac{N^2}{4} + n_i^2}}{n_i}\right) \end{aligned} \tag{3.32}$$

Which is the difference between the Fermi level and the vacuum level. At the interface between a semiconductor and a metal, a Shottky barrier arises. Depending on whether the semiconductor is n or p-type the bands in the semiconductor will bend up or down respectively due to charge carrier migration between the materials. In a metal, the continuum of energy levels causes any excited electrons to quickly decay to the Fermi level. When in contact with a semiconductor, the interface acts as an effective recombination site for the semiconductor and the law of mass action is valid. Furthermore, we assume zero charge at the interface and equation (3.32) for the potential and equations (3.29) and (3.30) for the concentrations provides the boundary conditions given that no electric potential is applied to the metal, which in our there is not.

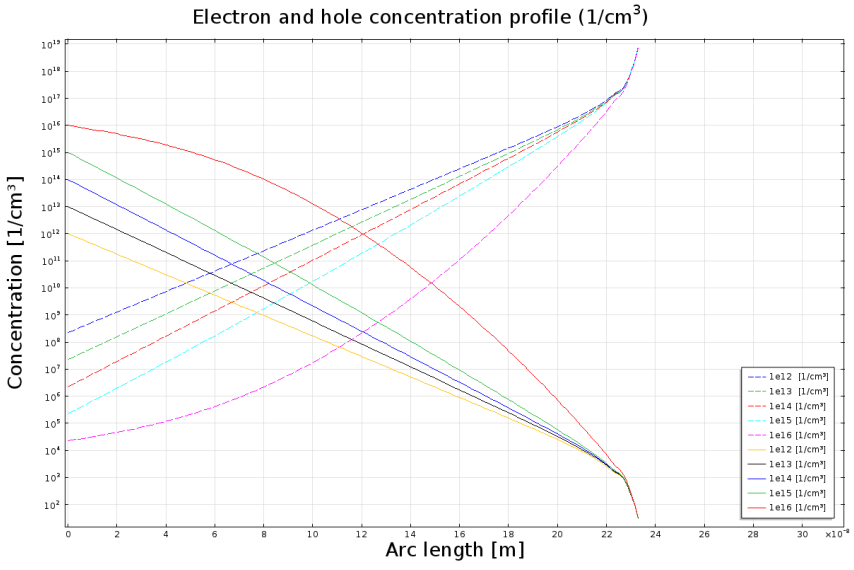


Figure 3.6: *Electron(dotted lines) and hole(solid lines) distributions for different boron concentrations of the a-Si layer. Boron concentrations are indicated by the legend.*

A conductivity profile is then calculated using equation (3.11) and can be seen on Figure 3.7. Values for mobilities of electrons and holes in amorphous silicon were found elsewhere as $\mu_e \sim 5 \cdot cm^2/s \cdot V$ [6] and $\mu_h \sim 6.1 \cdot 10^{-4} cm^2/s \cdot V$[15, 19], both orders of magnitude lower than the mobilities of crystalline silicon, which is expected since the high amount of defects reduces carrier lifetime substantially.

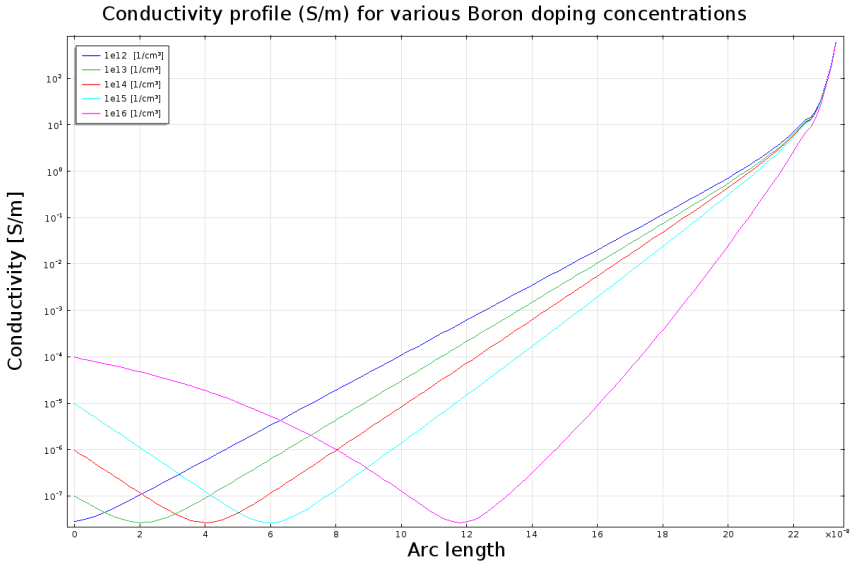


Figure 3.7: *Conductivity profile for different Boron concentrations of 240nm e-beam sputtered a-Si. The a-Si used in the experiments has a Boron concentration of* $1 \cdot 10^{12} cm^{-1}$.

In the table on Figure 3.8 the conductivity profile from Figure 3.7 is converted into representative layers of various thickness and conductivity. This set of layers defines a new complex permittivity distribution using equation (3.10) which is used instead of the original *a-Si* layer permittivity to simulate the behaviour of the plasMOSter under applied bias.

Layer thickness [nm]	Conductivity σ_0 [S/m]
3	437.33
12	33.12
17	4.18
26	0.40
175	0.004

Figure 3.8: *Thickness and conductivity of 5 successive layers which will replace the unbiased a-Si layer. The conductivity is approximated to zero since conductivities in that range has no noteworthy effect for 1550nm light.*

These conductivities are obviously quite low due to the low carrier lifetime in *a-Si*. They are however, significantly higher than that of intrinsic *a-Si* which is around $\sigma_0 = 10^{-11} S/cm$ [15]

3.3 Simulation of biased plasMOSter

First, the photonic dispersion calculations are repeated with the new *a-Si* layer stack to obtain knowledge of the modes for the biased plasMOSter. The results of these calculations can be seen on Figure 3.9

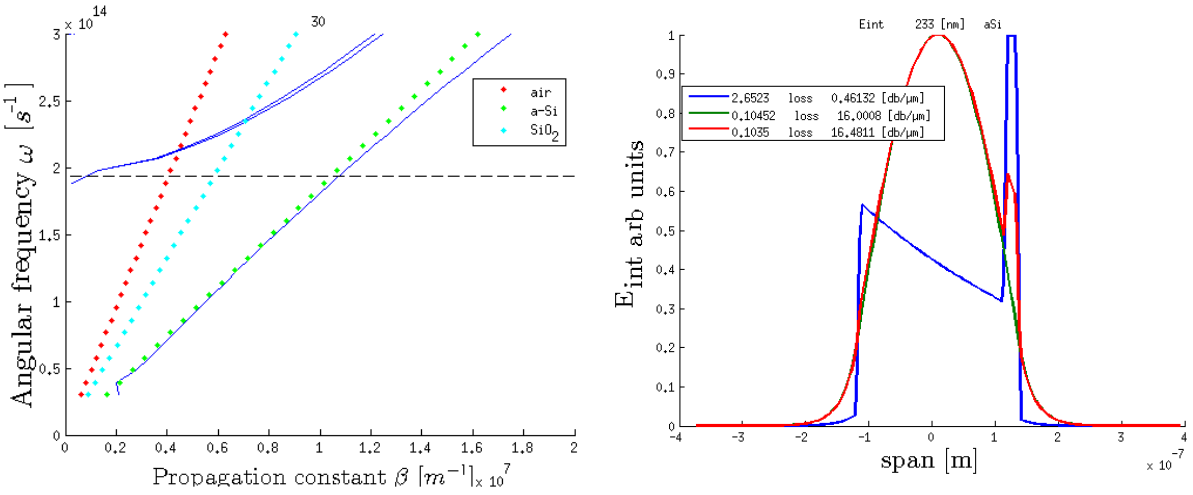


Figure 3.9: *Photonic dispersion relation* ***(a)*** *and normalised electric field profile* ***(b)*** *for the same configuration as on Figure 3.4 except a gate bias of 1V is applied here. The result is an increase in absorption of the photonic mode and only a negligible change for the plasmonic mode.*

It is clear that the change in index is small. This is due, in no small part, to the low mobility of *a-Si*. Obvious fixes to this includes applying a higher bias, enhancing the carrier mobility or using a different material. Solutions to this problem will be discussed later.

Regardless, the structure of the plasMOSter is a complex one and the modulation produced might be sufficient.

With the infomation about the slit shapes and thickness of the various layers in the test plasMOSter, we should first try to recreate the data available before predicting the effect of applying a gate bias. Here COMSOL™ Multiphysics 4.2 is used employing the RF module and frequency analysis. The simulation domains can be seen on Figure 3.10

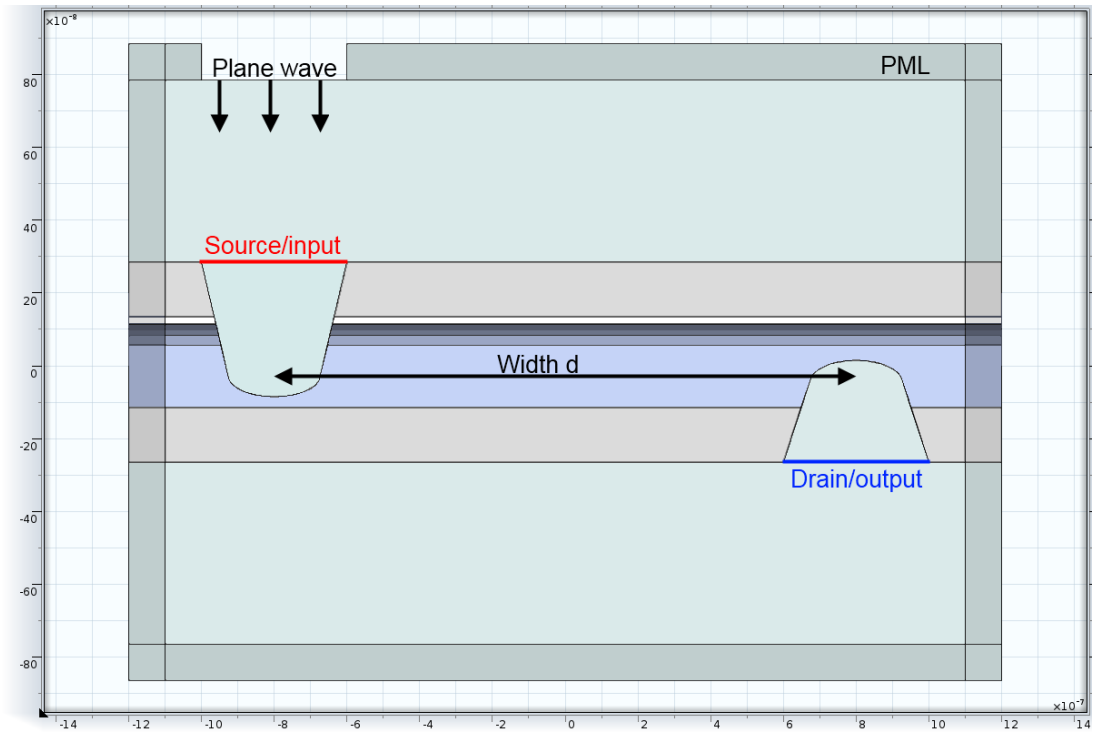


Figure 3.10: *The simulation box used for finite element analysis of optimisation of source-drain distance d. The wave guide layer is replaced by a set of five layers with conductivities from table 3.8. The input here is a plane wave with a wavelength of 1550nm. The gray toned edge domains are perfectly matched layers(PML) which absorbs all incoming radiation from media with the same refractive index as the PML.*

The *a-Si* permittivity profile was defined using the table on Figure 3.8 and equation (3.10). With conductivity of all the layers set to zero, which is approximately true for the unbiased case, steady state was computed for a sweep over source-drain separation distance. The figure of merit for the device was chosen to be the normalised average power intensity in the y-direction for the drain output boundary highlighted on Figure 3.10.

On Figure 3.11 simulation results are plotted showing modulation for a sweep over source-drain distance.

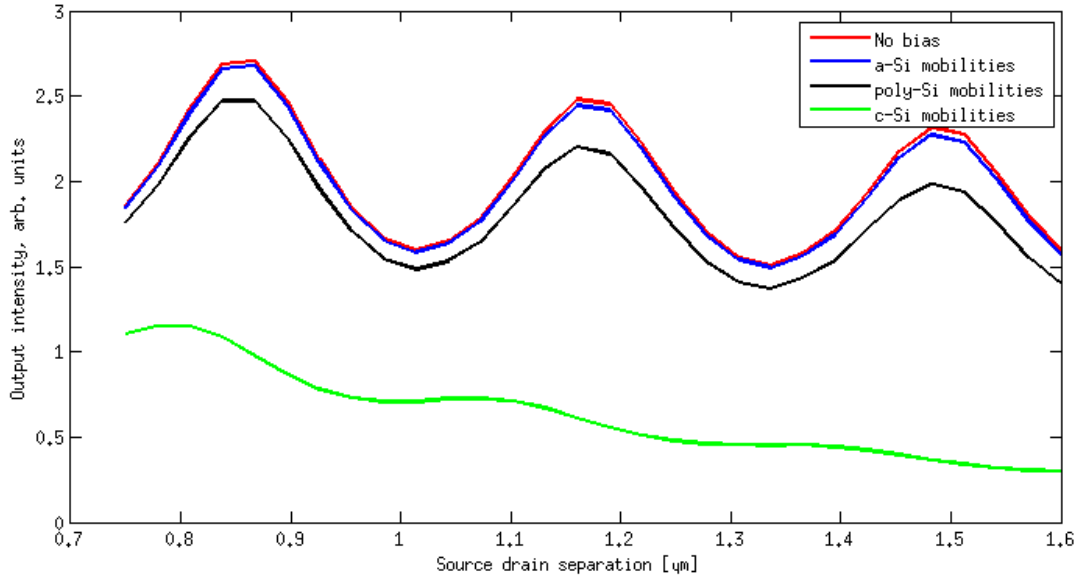


Figure 3.11: *Output intensity for various sweeps.The output values are absolute values of time averaged energy dissipation in y-direction, integrated over the drain output boundary highlighted on Figure 3.10. In the unbiased case**(red)** minima(destructive interference) and maxima(constructive interference) are clearly distinguishable. However due to the low carrier mobility of a-Si, the photonic mode is not damped enough over the separation span of this set of simulations to produce a significant difference between "on"**(blue)** and "off"**(red)** states. Since polycrystaline silicon(poly-Si is a viable alternative with carrier mobilities, magnitudes higher than that of a-Si, a plot**(black)** is seen where poly-Si mobilities are used in the biased simulation, and shows a more effective dampening of one mode resulting in less profound interference. Finally, the mobilities for crystalline silicon**(green)**, which are even higher, are explored as well.*

It is clear that the carrier mobilities of *a-Si* hinders proper operation of the device. Of course higher gate bias would help by increasing the charge carrier concentration and hence the conductivity. Using high voltages in integrated circuitry results in other problems and is an unwanted trade-off if the problem can be solved by a change in design. Means to achieve this goal will be discussed later.

The plot on Figure 3.11 also reveals that further enhancement of the plasmonic mode relative to the photonic mode is needed. Ideally, the plasmonic and photonic modes should each transport half of the field each, so that destructive interference would lead to complete annihilation of the field at the drain. According to the design of the plasMOSter, the photonic mode is most sensitive to the modulation and it is therefore most likely the photonic mode we see are being damped on Figure 3.11 as the conductivity increases with various mobilities. For mobilities similar to those for crystalline silicon it is seen, that the output intensity plot approaches the exponentially decaying profile expected of a single mode in a lossy medium. Since the design these calculations are based upon, have pushed the *a-Si* thickness to a point where the photonic mode is close to cut-off, if the thickness is further decreased, the photonic mode will no longer be supported. Thinner layers can be used if the material has a higher refractive index. Poly-*Si* has both higher carrier mobility and refractive index. Considerations regarding use of poly-*Si* instead of amorphous will be discussed later.

Another aspect of the plasMOSter operation that should be considered is reflected radiation from within the structure. On Figure 3.12 results for simulated input power is plotted. The values are time averaged energy dissipation through the source boundaryhighlighted on Figure 3.10. The values are integrated over the boundary, assuming infinity in the third direction. Just like before, the analysis is carried out for a number of different source-drain separation widths. The approach is identical to that used to produce the plot on Figure 3.11 and yields units of intensity.

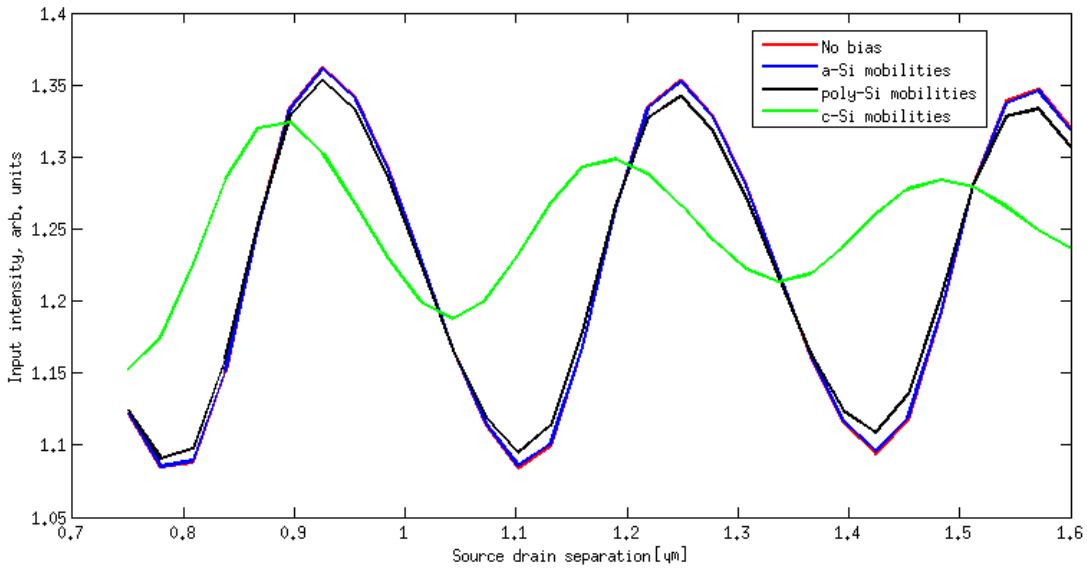


Figure 3.12: *Input intensity for various sweeps. The data points are absolute values of time averaged energy dissipation in y-direction, integrated over the source input boundary highlighted on Figure 3.10. It is clear that the dominating contribution is the input from the plane wave source, but minima are observed with* $\sim$ *20% lower values than the maxima.*

Since nothing is changed in how the source recieves its input, the lower input intensity must be due to energy dissipation out of the source slit. The only influential geometric parameter changed is the source-drain distance, so the sinusoidal like features of the plots is likely a resonance effect meaning light is being reflected by the drain/air interface. This suggests, that up to 20% higher output can be acchieved if reflection from the drain slit is reduced, e.g. through proper design of the shape or by applying an antireflective coating.

4 Device characterisation

The first goal is to establish an optimum source-drain distance, that is a distance between the source and drain slits that leads to destructive interference between the guided modes. This was approached in two ways, both using a $7mW$, $1550nm$ wavelength laser focused down to a $10\mu m$ spot as input on the source slit.

First, Near field Scanning Optical Microscopy(NSOM) was attempted, but proved too invasive and the probe damaged the structure before useful data could be obtained. Instead an infrared camera was used to photograph each drain slit with the laser focused on the source slit.

4.1 NSOM imaging

In near field scanning optical microscopy, an optical fiber performs a raster scan, much like a cantilever in an AFM. Since this fiber comes in close contact to the surface is capable of probing the near-field of a sample. The NSOM setup used here can be seen on Figure 4.1.

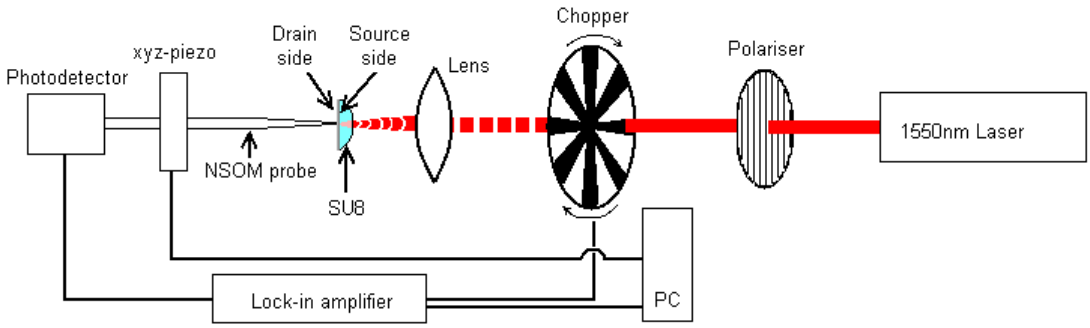
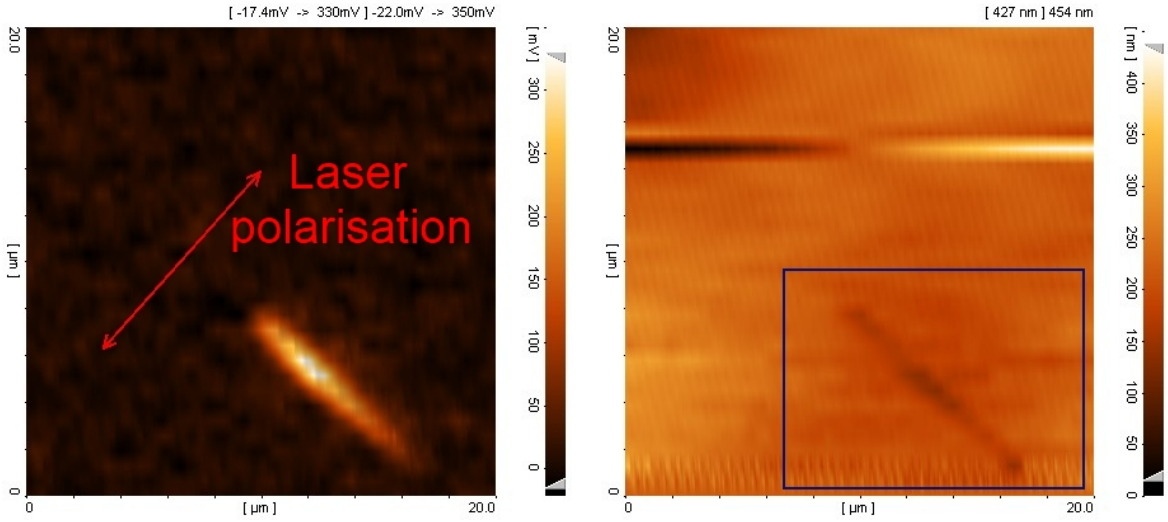


Figure 4.1: *Conceptual diagram of the NSOM setup.*

Here we are interested in measuring the average intensity of light that exits the drain slits while $1550nm$ light is incident on the source slits. A way to do this is to scan each slit using the same scan parameters each time. The results can then be evaluated by integrating the signal over each plot. This will give a comparable value for each device representing its abillity to transmit radiation. The measurements were made with the polarisation of the incident laser perpendicular to the source slits, as it allows for maximum amount of light to enter.

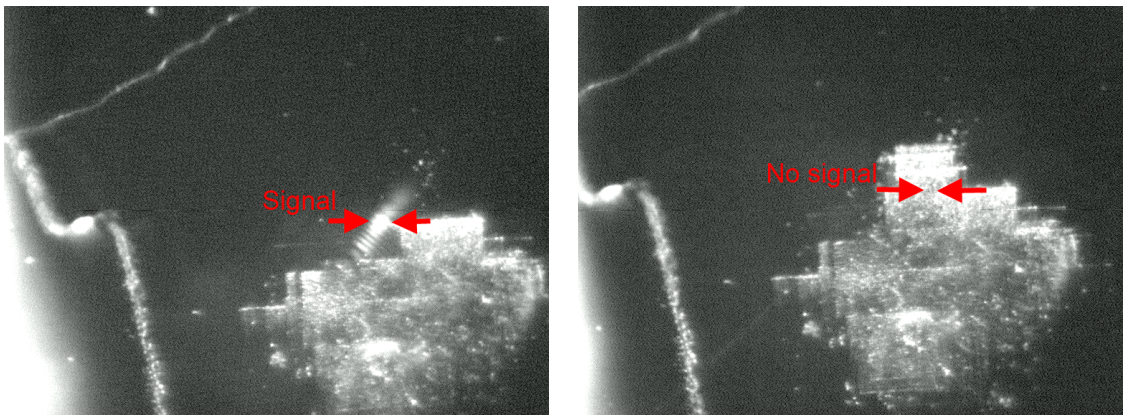
That light in fact passes through the plasMOSter can be seen on the NSOM image on Figure 4.2



(a) (b)

Figure 4.2: *NSOM **(a)** and topographical image **(b)** of a slit from the intact array from before damage became too severe. Laser polarisation is indicated on **(a)** by the red arrow.*

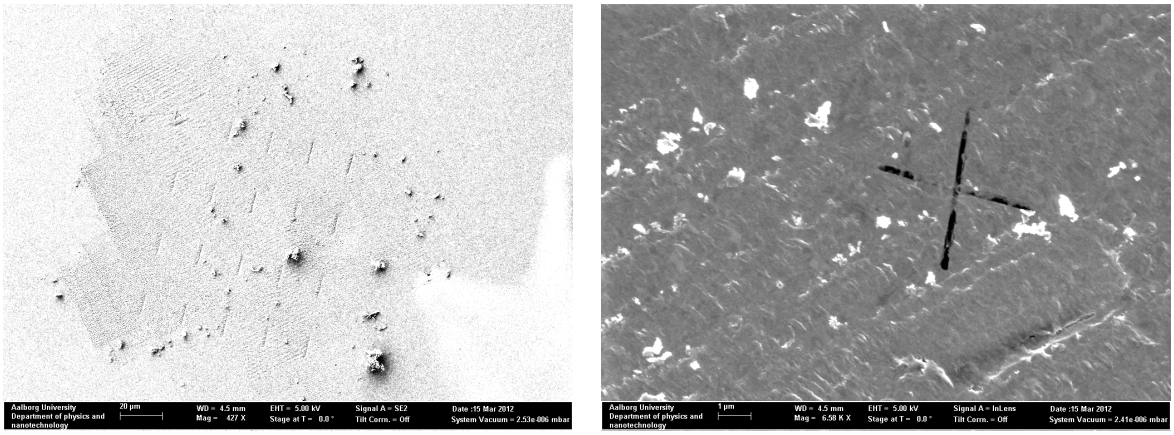
However, several scans were involved in the process of properly aligning the probe to a slit. It was here noticed that as a slit was scanned several times, the signal disappeared. The force applied is only a few nano Newtons and NSOM is generally not considered an invasive procedure especially not on a metal surface like silver. Still, as can be seen on Figure 4.3 IR pictures of the surface revealed some alteration of the surface from scanning and even shows how scanning a particular drain slit makes it unable to transmit.



(a) (b)

Figure 4.3: *IR pictures of the array that were intact after peel-off. Here, surface structures are visible since light from a light bulb is incident on the side facing the camera. At the same time, an IR laser is fixed and focused onto a single source slit from behind the sample. Scattered light from rectangular areas are from previous NSOM scans. On **(a)** a functioning drain slit is found outside the scanned area. On **(b)** that area has been scanned several times and the radiation is no longer transmitted.*

Since the procedure needed several scans of the same area to properly align probe and sample, the resulting scans would not be comparable. On the topography scans the slits were still visible and no destruction could be seen. However, SEM images seen on Figure 4.4 shows how the surface has been scratched by the probe.



(a) (b)

Figure 4.4: *SEM scans of* ***(a):*** *Overview and* ***(b):*** *Alignment cross, showing significant damage as a result of scanning the silver surface with an glass probe.*

Furthermore, significant topography deformation was observed in form of wrinkles, during prolonged scans of the same area. As opposed to the scratches, these wrinkles were much larger than than the tip of the probe and can be seen as circular dips in topography height $> 100nm$ on Figure 4.5.

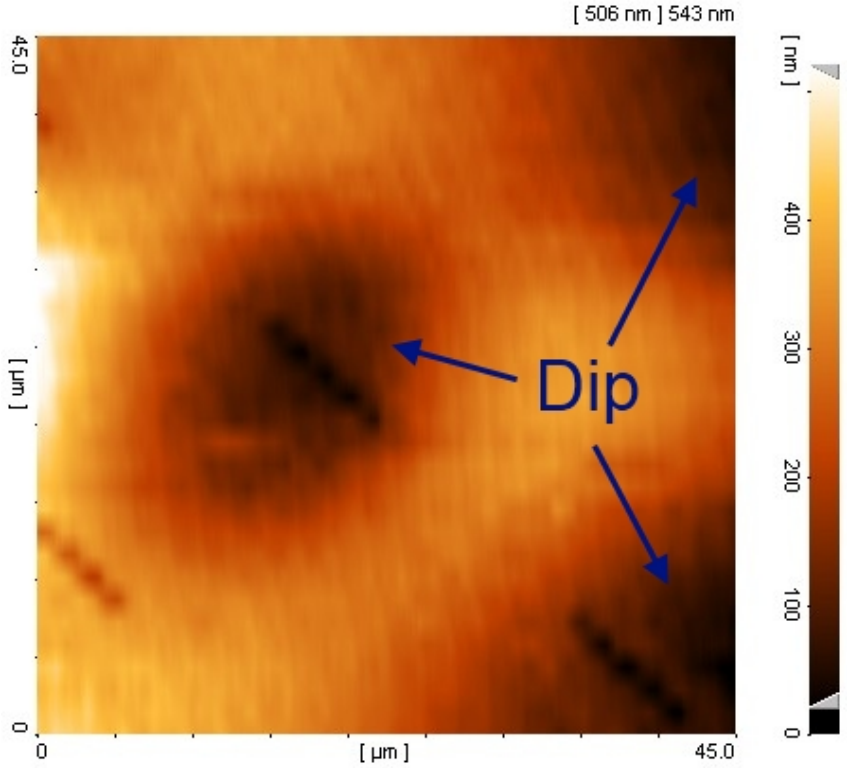
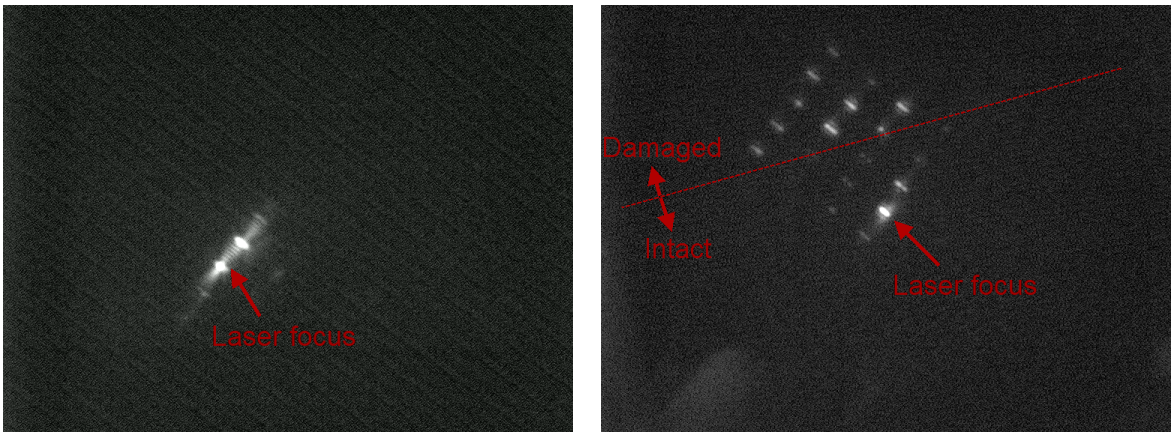


Figure 4.5: *Topography showing wrinkles with depths* $> 100nm$ *which may have partially induced the loss of signal over time.*

It is not unlikely that these wrinkles are the product of either stress in the layer stack or in the polymer substrate. Since it developed over time it could have been thermally induced. Silver absorbs IR radiation and has a high heat conductivity. However, this layer of silver is sandwiched between a layer of amorphous silicon and a polymer neither of which dissipates heat well. The laser may only produce $7mW$ ($\sim 2mW$ hits the sample since the signal is polarised and chopped), but the energy is concentrated on a spot $\sim 10\mu m$ in diameter, making the local intensity fairly high. With slow heat dissipation, heat builds up and may induce stress in the polymer, resulting in the wrinkles seen on Figure 4.5. Obviously this would not be as much of a problem in an integrated optical circuit as the substrate will most likely be something crystalline like a silicon wafer.
Bottom line, for this particular device design, NSOM seems too invasive to say anything conclusive and ended up destroying more than $2/3$ of slits left intact after peel-off. Therefore, an alternative approach was attempted using only an IR sensitive camera.

4.2 IR pixel analysis

Output radiation from the plasMOSter arrays were high enough to be clearly detectable with an IR camera. IR pictures of both arrays can be seen on Figure 4.6



(a) (b)

Figure 4.6: *IR images of* ***(a):*** *the array NSOM was performed on, taken before the array was damaged and* ***(b):*** *the array partially damaged from peel-off where the dotted line separates intact(lower) from damaged(upper) slits. Both images were taken with laser incident on the source side and focus point indicated by arrows.*

The goal here was to obtain a measure of how much radiation each device transmits relative to each other. This was done here by first reducing exposure time for the camera to a level, where it does not reach saturation at any of the slits. Then, the laser spot was placed on each slit individually and pictures were taken. The pictures were taken in an RGB format and imported to MATLAB®. Since the pictures are black and white, the difference in RGB values remains the same regardless of intensity. This means that intensity can be evaluated by using just one value. The NSOM scan seen on Figure 4.7 from the destroyed array had revealed, that the output radiation was concentrated at the slit ends. This is also vaguely seen on Figure 4.6**(a)** and **(b)**, but is confirmed through closer examination.

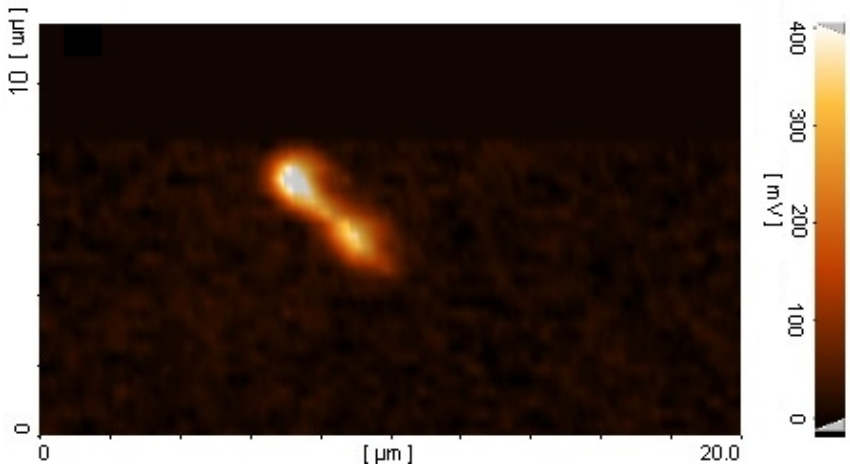


Figure 4.7: *NSOM image of a single slit, showing how fields are concentrated at the ends.*

As seen on Figure 4.6 **(b)** only *eight* slits were left undamaged after peel-off. For each slit picture, the highest value of green in the bottom half of the slit was interpreted as an intensity representative value.

SEM scans like the one shown on Figure 2.13 taken for each slit were used to associate each intensity reading with a source-drain distance. These values are plotted together with simulation results on Figure 4.8

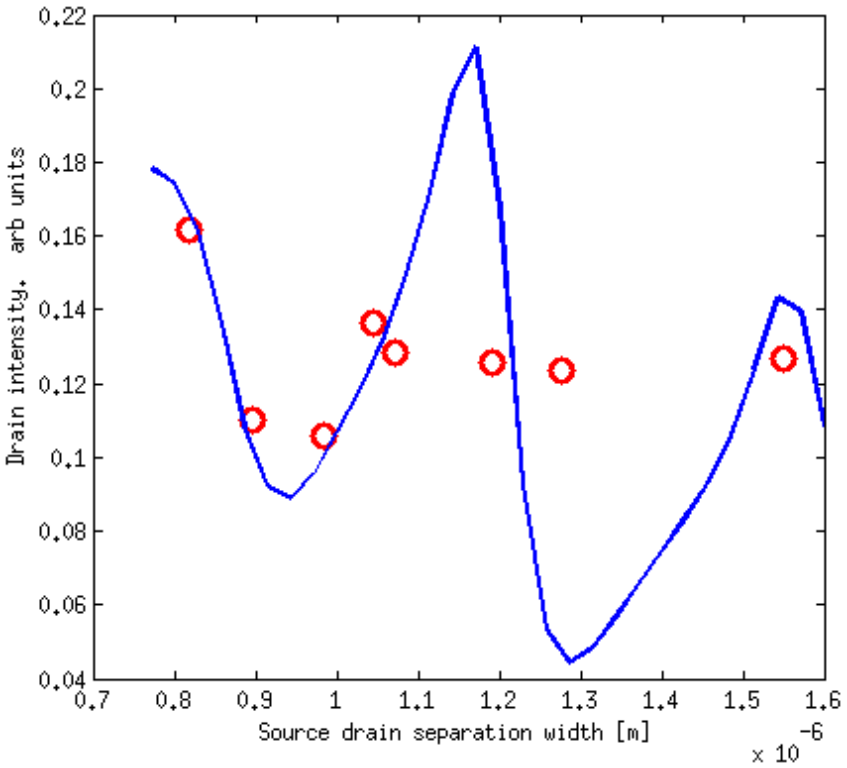


Figure 4.8: *Transmitted light intensity plotted against source-drain separation width. Red circles are measured data, analysed using the IR pixel analysis technique, and the blue line is the simulation result for a 400nm a-Si wave guide using the same approach as in section 3.3 on page 32.*

It is clear that the amount of data points available are insufficient and data is needed at some key points to be able to say anything conclusive.

5 Discussion

5.1 e-beam sputtered *a-Si*

Amorphous silicon proved to be a poor choice as wave guide material in the plasMOSter due to its low carrier mobilities and refractive index. The low refractive index compared to alternatives like crystalline and polycrystalline silicon, means that the layer must be made thicker in order to support the photonic mode. This is a problem not so much that the dimensions increase but more because roughness that arise during deposition of material is amplified as more material is sputtered on, as is evident on Figure 2.2 on page 7, where it is clear that the smooth surface of the silicon wafer is not transferred to the top layers. This provides a problem for the plasmonic modes propagating along these interfaces as their propagation is very sensitive to roughness[12, 13]. Scattering of plasmons are difficult to account for and results in higher loss for the plasmons. The ideal material is therefore a material with a high refractive index, low absorption of near infrared light and high carrier mobility. Without changing the overall mechanisms and fabrication too much this is achievable in at least two ways: Laser annealing of the *a-Si* layer or replacing the *a-Si* with a layer of poly-*Si*. One note of importance here though. Hydrogenation of *a-Si* does improve carrier properties but studies have shown that hydrogenated *a-Si* is photodegradable called the Staebler-Wronski effect[25], which of course rules it out as viable wave guide material.

5.1.1 Laser annealing

Recrystallisation of materials through annealing is widely used. The process relies on applying enough energy for bonds to break, allowing atoms to relocate and form bonds in a conformation that is more crystalline. The energy can be supplied as heat, which is a scalable method but requires the material to be heated to temperatures approaching the melting point for bonds to break. For silicon that means heating well above $1000^{\circ}K$[17]. Furthermore, if oxygen is present, it will rapidly oxidise the material. High temperature is unfavourable in heterostructures as it induces strain on the interfaces, and in this case one of the other materials is silver which will melt around $1300^{\circ}K$.
Another method is laser annealing[27, 18] where the energy is delivered by an excimer laser. This method can produce poly-*Si* with grain sizes $> 100nm$. This enables mobilities orders of magnitude larger than that of *a-Si*[18], but since the layer thickness needed is also just a few hundred nanometers, this is not a viable option. Fortunately, the grain size can be varied by controlling the laser intensity and one should consider a trade-off between favourable carrier properties and small grain sizes. Unfortunately, the method is not scalable and the laser or a series of laser would have to scan the areas where annealing is needed.

5.1.2 Using poly-*Si*

Instead of attempting to crystallise *a-Si*, poly-*Si* can be deposited using LPCVD which produces grain sizes around 60*nm*[17] which should not scatter the 1550*nm* light much. The LPCVD deposition approach has some obvious advantages over the laborious annealing process described above. Furthermore, poly-*Si* has been used as a gate contact material for MOSFETs in the industry[2] for many years, so the deposition on large scale is well implemented.
One disadvantage with LPCVD of poly-*Si* is that it takes place at $\sim 900^{\circ}$ so lift-off is not an option. Instead, the entire wafer is covered and photolithography is used to define the structure and the unwanted poly-*Si* is etched away.
Using poly-*Si* is an important upgrade for the plasMOSter, not only because it provides higher carrier mobilities but also because a more confined wave guide will be more sensitive to the electrical field modulation. This is because a larger portion of the photonic mode will be situated at the poly-Si/SiO_2 interface as the poly-*Si* layer becomes thinner, but only if the SiO_2 layer thickness is kept constant.
The implementation of poly-*Si* into a plasMOSter design can be found in the following section.

5.2 Fabrication on large scale

One of the main challenges proposed in this project was to not attempt any structure that can not be fabricated with the VLSI technology of today. It is clear that the methods for the material depositions are easily scalable. However, techniques that are not mass production friendly have also been used here. Still, no structure have been attempted where the technique for making it could not be replaced by a VLSI technique. For instance the FIB milling of source and drain slits, would be replaced by projection UV lithography and RIE. Since, the slits are a couple of hundred nanometers across, the lithography technology is long out-dated[8, 24] and thus easily achievable.
Additionally, the plasMOSter would not be transferred to another material as was the case in this study where it was done to facilitate characterisation. In today's VLSI, communication does not take place across the substrate and the plasMOSter should be able to return outputs on the same side as it takes in its input. So, using source and drain slits might not even be the way to go. The design seen on Figure 1.3 accomplishes just that. In that design, the plasMOSter is an integrated part of the wave guide and returns its output in the same plane as it takes its input. Some difficulty lies in realising a 3D structure like that with planar techniques, but on Figure 5.1 a series of fabrication steps are suggested.

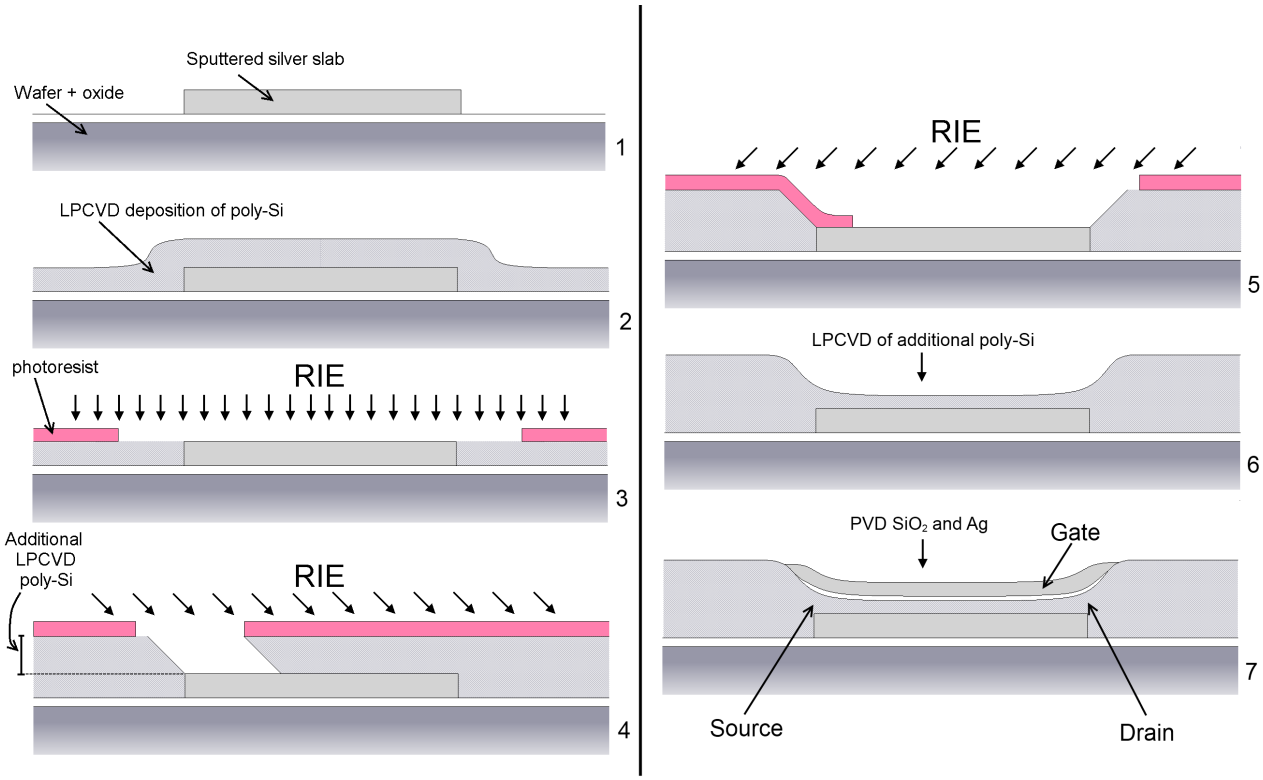


Figure 5.1: *Suggested fabrication steps for realisation of integrated plasMOSter using optical lithography methods. Intermediate steps with application of photo resist and exposure are left out.* ***(1):*** *A wafer is oxidised with a thick oxide and the bottom silver slab is made using e-beam or DC sputtering and lift-off.* ***(2):*** *LPCVD is used to deposit a layer of poly-Si with same thickness as the silver slab.* ***(3):*** *RIE is used to remove the poly-Si at the silver slab.* ***(4):*** *A thick layer of poly-Si is applied and RIE is used at a 45° angle.* ***(5):*** *A new photo resist is applied and again exposed asymmetrically around the silver slab so as to produce a 45° angle on the right side.* ***(6):*** *A layer of poly-Si is applied with thickness corresponding to the desired thickness of the plaMOSter wave guide layer.* ***(7):*** *Finally SiO_2 and the silver gate contact is applied using e-beam or a combination of RF and DC sputtering, in a lift-off process.*

The steps 4 and 5 on Figure 5.1 could be replaced by an isotropic *KOH* etch, but RIE is chosen here since it provides better etching control.

As mentioned earlier, this design differs slightly in its operating mechanism from the one with source and drain slits. With the slits, the output intensity due to interference was determined mainly by the distance between the source and drain, but in this VLSI design the output intensity is determined mainly by the length of the silver slabs.

It should be noted that the VLSI design uses poly-*Si* as wave guide. Here the wave guide is fabricated as a part of the steps seen on Figure 5.1. The strong confinement of light in the plasMOSter causes high loss of the photonic modes since a large proportion of the field is forced to propagate in the metal which has high absorption. Therefore, the wave guide should obviously be larger than the poly-*Si* layer in the plasMOSter since the main job of the wave guide is to guide light between components fast and without loss.

It should also be noted that the substrate used here is a silicon wafer which has a refractive index similar to that of poly-*Si*. If caution is not taken in making the oxide layer separating them thick enough, light will couple from the poly-*Si* to the silicon through evanescent fields.

5.3 Pixel analysis

As is seen on Figures 4.4 (a) and (b) NSOM damaged most of the samples. At this point, the FIB went out-of-order so a second batch could not be fabricated. So to reduce the chance of destroying the few structures that were left unharmed, a completely non-invasive method was needed. Since the long exposure to the laser was under suspecion of contributing to degeneration of the layered structure, the method needed to be one where the exposure time was kept short. Taking a picture with a camera accomplished just that.
The highest value was used instead of e.g. an average over a larger area, since slits placed between other slits produced standing waves between them, as seen on Figure 4.6. Averaging over an entire slit would give lower readings for slits at the edge of the array, since they only have neighbouring slits to one side. By comparison, highest value readings of intensity seems more representative.

5.4 Optically modulated plasMONster

If the vision is all-optical signal manipulation, then the induced conductivity of the plasMOSter needs to be optically triggered. This can be accomplished in at least two ways. An optical signal can be converted into an electrical signal using an integrated photovoltaic(PV) device connected to the gate contact. This is indeed possible, but means that the PV has to be produced which adds additional steps to the fabrication. Futhermore, the transport of electrons is slow compared to light. The ideal case would be modulation using a light signal which would fundamentally change the operating mechanism of the plasMOSter. This could be achieved with photoconductivity where simple excitation of electrons in the valence band into the conduction band increases charge carrier concentration and hence absorption. The device would no longer need the SiO_2 layer and should instead be classified as a plasMONster. This is a twin edged blade however. For the device to work at high operation speeds it must be able to quickly turn on and off. For the plasMONster, "on" means that the conductivity is raised to a level where the photonic mode is dampened enough so that the output can be considered a logic "1". The device is considered in "off" mode when the conductivity drops to a sufficiently low level. Fast switching between on and off relies on two competing properties of the active material.
Photoconductivity is induced by radiation with energy matching the bandgap, but the material must obviously be chosen so that the communication wavelength is *not* capable of exciting charge carriers. This means the device will work with two different wavelengths an excitation and a transmission wavelength. There are three things to consider here. The rate of excitation, dissipation of excitation radiation and how

to apply the excitation light. The rate of excitation of course depends on the intensity of excitation radiation but since that should be kept as low as possible the material should be carefully chosen to effectively produce charge carriers. This first of all means choosing a direct bandgap material instead of silicon. This will enhance charge carrier generation and will solve the problem of excitation light dissipating into the wave guide causing increased absorption outside the device. With a device design like that on Figure 5.1 the light can be coupled in from the side of the plasMOSter, parallel to the substrate. If it is assumed that the communication wave length used is in the near-IR and the excitation is in the ultraviolet, then light excitation light could also be applied from a vertical direction, that is, perpendicular to the top metal layer. This means that the top layer should be able to allow UV light to pass through and prevent near-IR from escaping while at the same time maintaining a silver layer that supports plasmonic modes. This can be done by replacing the top silver layer with a 1D band pass filter[9] which is a simple modification of the fabrication process as the top silver layer is simply replaced by alternating layers of silver and SiO_2 with predetermined thickness's effectively blocking propagation of one wave length while allowing passage of another. Since the layers are silver and SiO_2 they can be deposited in a single run much like the layer stack in this project was fabricated.

6 Conclusion

In this project, various aspects of a plasMOSter design is explored. The plasMOSter is an electro-optical transistor that uses an electric signal to control the transmission of near infrared light through it. A main focus throughout the project has been to fabricate and design the device in a manner that is ready for very large scale integration.

The device is based on a layer stack containing silver, amorphous silicon and SiO_2, which are all deposited using e-beam sputter deposition. This means the fabrication is independent of substrate material and can in principle be placed on any flat surface. The amorphous silicon deposited using this technique showed properties that differ from those of amorphous silicon produced using CVD techniques. Ellipsometry revealed an overall lower refractive index, but it was showed that changes in deposition parameters allowed for higher refractive index to be obtained. Focused ion beam(FIB) was used to mill source and drain holes. The FIB was used out-of-focus to obtain more rectangular cross-sections.

The design of the plasMOSter relies on photonic dispersion engineering which was approached in two ways. Singular value decomposition of a homogeneous equation system representing various field components and boundary conditions proved ineffective and the remaining dispersion engineering was carried out using finite-difference analysis software.

7 References

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A Photonic dispersions in layered structures

When analysing which photonic modes are supported by a given structure, Maxwells equations provides a good starting point. Optical modes are configurations of electrical and magnetic fields that solves certain wave equations. To such expressions the following two relations from Maxwells equations are used

$$\nabla \times \mathbf{E} = -\frac{\partial \mathbf{B}}{\partial t} \tag{A.1}$$

$$\nabla \times \mathbf{H} = \mathbf{J_{ext}} + \frac{\partial \mathbf{D}}{\partial t} \tag{A.2}$$

Where

$$\mathbf{D} = \varepsilon_0 \mathbf{E} + \mathbf{P} \tag{A.3}$$

$$\mathbf{H} = \mu_0^{-1} \mathbf{B} - \mathbf{M} \tag{A.4}$$

Which for isotropic and nonmagnetic materials reduces to

$$\mathbf{D} = \varepsilon_0 \varepsilon \mathbf{E} \tag{A.5}$$

$$\mathbf{B} = \mu_0 \mu \mathbf{H} \tag{A.6}$$

Taking the curl of (A.1) assuming isotropic nonmagnetic materials gives

$$\nabla \times \nabla \times \mathbf{E} = -\nabla \times \frac{\partial \mathbf{B}}{\partial t} \tag{A.7}$$

Inserting (A.6) and using (A.2) remembering that $\mathbf{J_{ext}} = \mathbf{0}$ gives rise to

$$\nabla \times \nabla \times \mathbf{E} \quad = \quad -\mu_0 \frac{\partial^2 \mathbf{D}}{\partial t^2} \tag{A.8}$$

using $\nabla \times \nabla \times = -\nabla^2 + \nabla\nabla\cdot$ and the assumption of no external charge $\nabla \cdot \mathbf{D} = \mathbf{0}$ we get the widely used wave equation

$$\nabla^2 \mathbf{E} - \frac{\varepsilon}{c^2} \frac{\partial^2 \mathbf{E}}{\partial t^2} = 0 \tag{A.9}$$

For confined propagating waves we assume the fields take a time harmonic form i.e. $\mathbf{E}(\mathbf{r},t) = \mathbf{E}(\mathbf{r})e^{-i\omega t}$ and we arrive at the Helmholtz equation

$$\nabla^2 \mathbf{E} + k_0^2 \varepsilon \mathbf{E} = 0 \tag{A.10}$$

where $k_0 = \frac{\omega}{c}$.

Throughout this project the structures we have been dealing with are essentially one dimensional. That is, material properties, like permitivity, changes in one direction only $\varepsilon = \varepsilon(z)$. Now, let us place the coordinate system so that the z-direction is normal to the material interfaces and the waves propagate in the x-direction. This way, we can express the spatial component of the electric field as $\mathbf{E}(x,y,z) = \mathbf{E}(z)e^{i\beta x}$ where $\beta = k_x$ is the propagation constant component in the direction of propation. Evaluating equation (A.11) using this form of the electric field yields

$$\frac{\partial^2 \mathbf{E}}{\partial z^2} + (k_0^2 \varepsilon - \beta^2)\mathbf{E} = 0 \tag{A.11}$$

A similar expression can be found for the magnetic field following the same route as here, but for these expressions to be of any use, we need to obtain expressions for the componennts of these fields. This is easily done by once again considering equations (A.1) and (A.2) e.g.

$$\nabla \times \mathbf{E} \quad = \quad -\frac{\partial \mathbf{B}}{\partial t} \tag{A.12}$$

$$\Updownarrow$$

$$\left(\frac{\partial E_z}{\partial y} - \frac{\partial E_y}{\partial z}\right)\hat{\mathbf{x}} + \left(\frac{\partial E_x}{\partial z} - \frac{\partial E_z}{\partial x}\right)\hat{\mathbf{y}} + \left(\frac{\partial E_y}{\partial x} - \frac{\partial E_x}{\partial y}\right)\hat{\mathbf{z}} \quad = \quad -\left(\frac{\partial B_x}{\partial t}\hat{\mathbf{x}} + \frac{\partial B_y}{\partial t}\hat{\mathbf{y}} + \frac{\partial B_z}{\partial t}\hat{\mathbf{z}}\right) \tag{A.13}$$

and

$$\nabla \times \mathbf{H} \quad = \quad \frac{\partial \mathbf{D}}{\partial t} \tag{A.14}$$

$$\Updownarrow$$

$$\left(\frac{\partial H_z}{\partial y} - \frac{\partial H_y}{\partial z}\right)\hat{\mathbf{x}} + \left(\frac{\partial H_x}{\partial z} - \frac{\partial H_z}{\partial x}\right)\hat{\mathbf{y}} + \left(\frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y}\right)\hat{\mathbf{z}} \quad = \quad \left(\frac{\partial D_x}{\partial t}\hat{\mathbf{x}} + \frac{\partial D_y}{\partial t}\hat{\mathbf{y}} + \frac{\partial D_z}{\partial t}\hat{\mathbf{z}}\right)$$

(A.15)

Remembering that there is homogeneity in the y-direction $\left(\frac{\partial}{\partial y}=0\right)$ along with equation (A.3) and (A.4) and noticing that $\left(\frac{\partial}{\partial x}=i\beta\right)$ and $\left(\frac{\partial}{\partial t}=-i\omega\right)$ these six equations turns out to be

$$\frac{\partial E_y}{\partial z} = -i\omega\mu_0 H_x \tag{A.16}$$

$$\frac{\partial E_y}{\partial z} - i\beta E_z = -i\omega\mu_0 H_y \tag{A.17}$$

$$i\beta E_y = i\omega\mu_0 H_z \tag{A.18}$$

$$\frac{\partial H_y}{\partial z} = i\varepsilon\varepsilon_0\omega E_x \tag{A.19}$$

$$\frac{\partial H_x}{\partial z} - i\beta H_z = -i\varepsilon\varepsilon_0\omega E_y \tag{A.20}$$

$$i\beta H_y = -i\varepsilon\varepsilon_0\omega E_z \tag{A.21}$$

This system allows for two sets of selfconsistent solutions. One set describes the transverse electric (TE) modes i.e. only the components H_x, H_z and E_y are nonzero. The other set contains the transverse magnetic modes(TM) where only the components E_x, E_z and H_y are nonzero.
For the TE modes the components E_x and E_z are zero and the wave equation becomes

$$\frac{\partial^2 E_y}{\partial z^2} + \left(k_0^2\varepsilon - \beta^2\right) E_y = 0 \tag{A.22}$$

with the component equations

$$H_x = \frac{i}{\omega\mu_0}\frac{\partial E_y}{\partial z} \tag{A.23}$$

$$H_z = \frac{\beta}{\omega\mu_0} E_y \tag{A.24}$$

For the TM modes the wave equation is

$$\frac{\partial^2 H_y}{\partial z^2} + \left(k_0^2\varepsilon - \beta^2\right) H_y = 0 \tag{A.25}$$

and the nonzero electric field components are

$$E_x = \frac{-i}{\omega\varepsilon\varepsilon_0}\frac{\partial H_y}{\partial z} \tag{A.26}$$

$$E_z = \frac{-\beta}{\omega\varepsilon\varepsilon_0} H_y \tag{A.27}$$

For a layered structure these fields must be solved for each layer using continuity of $H_y,\ H_x,\ B_z,\ E_x,\ E_y$ and D_z to match the fields at the boundaries.