Impact of Short-circuit events on Lifetime Expectancy of SiC MOSFETs

Giovanni Martello

AAU Energy, PED4-1040, 2024-02

Master's Project

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The Silicon Carbide (SiC) is a "new" material that offers very high performance, but the lifetime of components (in this case SiC MOSFET) are not sufficient and is shorter than the Silicon (Si) counterparts. The power cycling test is the best and the main way to extract the lifetime of a component. It can be performed in AC or DC mode, in this project the focus is on the DC mode. For the components made with Silicon Carbide (SiC) the expected lifetime is not reaching the theoretical value, due to problems during the manufacturing procedure and to the not clear failure mechanisms. This project aims to find if the lifetime of a SiC MOSFET, at which a no destructive stress has been performed (in this case the stress is a short-circuit with energy below the critical value), lays between the life time of a no damage component and a damage component. The power cycling are performed in a AC machine, adapted to work in DC mode, to do that a load adaptor has been developed.

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Contents

Preface

The author would firstly like to thank the Master thesis' supervisor Francesco Iannuzzo, professor at Aalborg University, for all his patience, kindness and guidance. Further, thanks to Ariya Sangwongwanich, associated professor at AAU and Kaichen Zhang, PhD student at AAU's Department of Energy Technology, for all their support and multilateral contribution throughout the entire project period. Additionally, the author would like to thank all him friends (international and italian) for the wonderful moments spent together during this beautiful experience.

Aalborg University, January 4, 2024

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Chapter 1

Introduction

The world electric demand is continuing to grow over time. In the past 20 years the electric requests markedly increased, for they are set to slightly grow by than 2% this year (2023) [13]. Nowadays, compared to the past, there is more awareness about the source of electric energy. In fig.1.1, the renewable energies (yellow bar) markedly increased during the years, furthermore, after COVID-19 (which started in 2020 and finished in 2022), they became the most important sources of electricity in Europe, while the coal (light blue bar), gas (dark blue bar), nuclear (light green) and other non-renewables (dark green) significantly dipped. [13] The graph 1.1 of the article [13] shows that the global trend is moving into a more eco-friendly position, and here the task of power electronics starts; new power devices will lead not only to enormous energy savings but also to conservation of fossil fuels and reduced environmental pollution. Eco-friendly means also to not waste energy, thus to be more efficient. Electric energy is regulated and converted, so that the power can be supplied to the loads in the best form; in general, the efficiency of power electronics is limited by the performance of semiconductor devices, capacitors, inductors and packaging. The power electronics (PE) is based on a material that could be considered "the father of the modern electronic": the Silicon. However, nowadays new materials that have even better characteristics than the Silicon have been studied.
The new studied materials for PE are: SiC (Silicon Carbide) and GaN (Gallium nitride).
The initial studies for this types of material have stared in the twentieth century [18], and are still continuing nowadays; compound semiconductors have established unique positions in PE applications where Si devices cannot exhibit good performance because of the inherent material properties. These devices will also find applications in efficient high-voltage DC power transmission lines, while for automotive applications the use of new materials will considerably reduce electricity loss during vehicle operation.

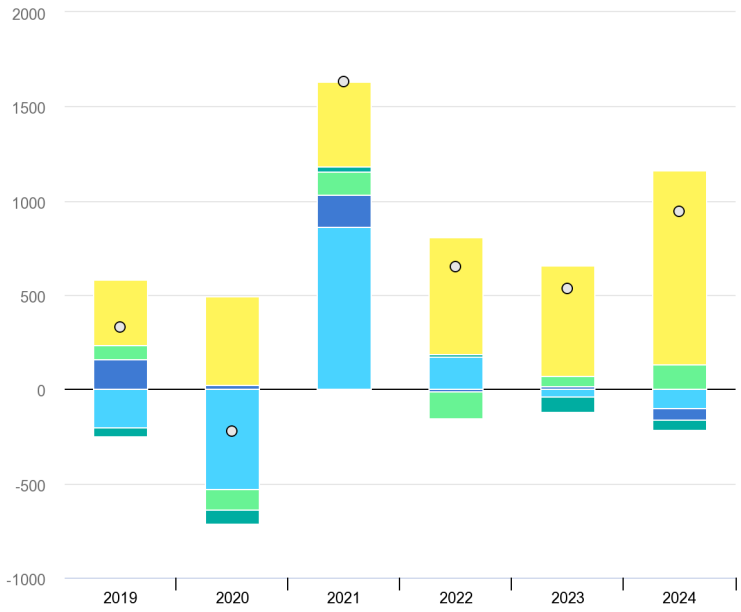


Figure 1.1: Year-on-year global change in electricity generation by source, 2019-2024.
Legend: the renewable energies (yellow bar), coal (light blue bar), gas (dark blue bar), nuclear (light green) and other non-renewable (dark green). [13]

The first electronics components created with SiC have been released in the early 1990s [18] and then the first commercial diode based on this new material has been commercialised in 2001 [10]. A very intuitive graph that allows to understand the developing of the SiC over the years is reported in fig. 1.2. Before 2006 the tech-

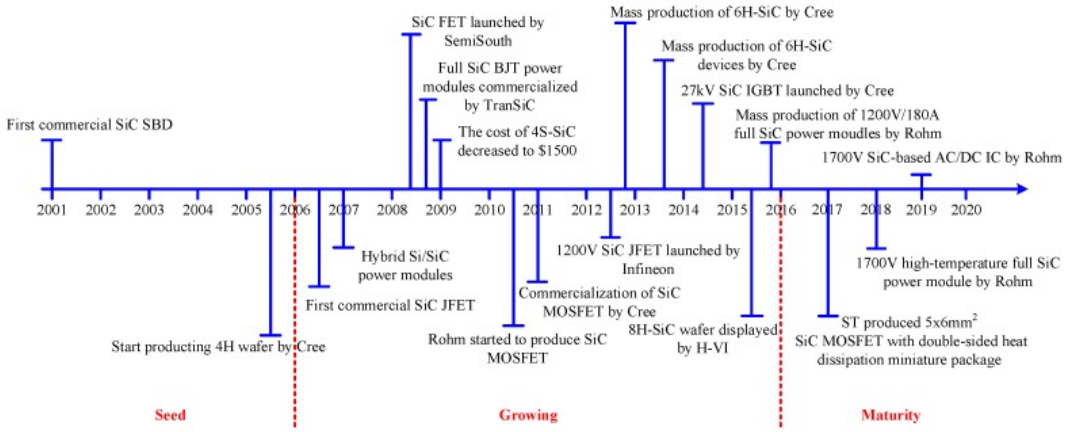


Figure 1.2: The milestones of the development process of SiC power electronic devices. [10].

nology wasn't ready to provide a very reliable and functional component made of SiC, but throughout the years the quality and the study increased to allow a good development of new components.Between 2006 and 2016, SiC technology started to grow significantly and successful results were obtained. After 2016, SiC technology was considered ready and mature [10]. The market value of SiC in 2022 was equal to 843.9 USD millions [14] and it is expected to continue growing in the next years, with a exponential trend, as shown in fig. 1.3. Furthermore, in 1.3 are reported

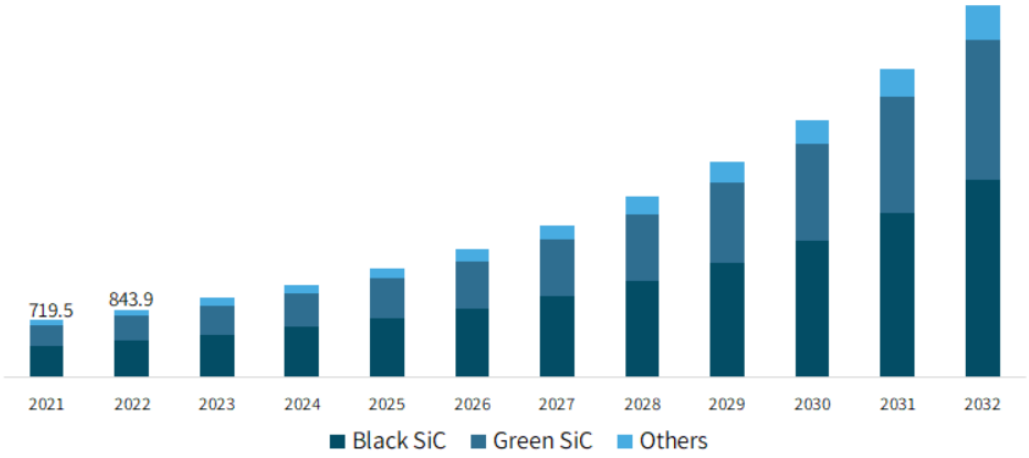


Figure 1.3: Global silicon carbide market size [Millions of USD] and its forecasted . [14].

two different categories of SiC: the green and the black SiC; green silicon carbide is basically the same as black silicon carbide, only the raw material and manufacturing process are different, the green product is translucent, hardness and purity is better than black silicon carbide [14].

To allow a better interpretation about the quality and differences between Si and SiC, in fig.1.4 are reported few of the most important parameters that show those differences. As can be seen all the characteristics are much higher in SiC compared to Si, an important aspect that deserves a small focus is the thermal conductivity ($\frac{W}{cmC^{\circ}}$); the high value of this parameter (even more than GaN thermal conductivity [21]) indicates that the SiC devices are the perfect subjects to handle high power because they are able to conduce in most efficient way the heat power; in addition, a related parameter is the junction temperature, which will be lower and therefore less subject to thermal stress. [9].

The future of electronics will be based on new materials (SiC and GaN), which, as it has been said, they have better characteristics compared to the "old" material (Si). Taking into account the world trend that is moving towards being more eco-friendly, the life-time of the components has a crucial role into this aspect, just think

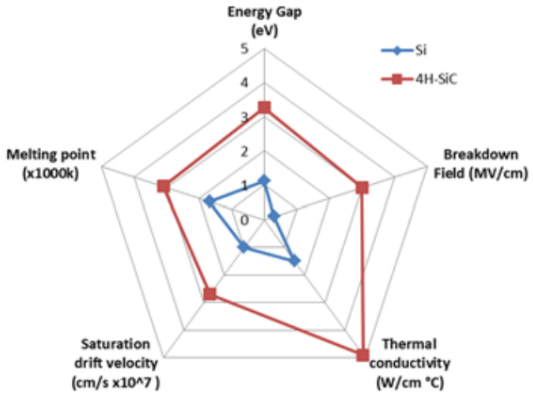


Figure 1.4: Comparison between Si and SiC material, based on their characteristic [25].

of how many electronic components are present in every devices and a component failure can lead to the device being discarded. Thus developing a more reliable electronics allow to produce less wastes, therefore important aspect that has to be taken into account is the reliability of these new components made with compound materials. The devices made by Si are well-known and their failure mechanisms as well, thus the knowledge of them also in the SiC and GaN devices, must to be examined in depth to guarantee the expected performance and their theoretical life-time[2] .
The goal of the electronics of the future is to be able to unleash the enormous potential that new materials hold for the world.

1.1 Purpose of the Project

The purpose of this project is investigate the impact of Short-circuit events on Lifetime Expectancy of SiC MOSFETs, it is a ECPE (European Center for Power Electronics) project. The AAU University will collaborate with IRT Saint Exupéry, Technological Research Institute (Toulouse University). The project aim to investigate the effect of SC on the SiC Mosfet life-time. From previous studies has been seen [6] that there is a so-called critical energy (E_{CRIT}) where the device under test is irreversibly damaged. In the past many other tests at reduced durations (Design-of-experiment approach) has been performed to investigate at which percentage of E_{CRIT} there is an observable drift of measurable parameters. Some results found by IRT are:

- V_{TH} doesn't change up 50%E_{CRIT}.
- I_{gss} doesn't change up to 90%E_{CRIT}.

However, some aspects of SiC Mosfet behaviour have lacks of knowledge about

1. Whether a device subject to a short-circuit event below 100%E_{CRIT}, i.e., damaged but still complaining with specs, reaches anyway up to the same expected life.
2. Whether a device subject to a short-circuit event below50%E_{CRIT}, i.e., with no detectable damage on any of the measurable device parameters, reaches anyway up to the same expected life.

The selected components are provided by STmicroelectronics, and the component is a 1200 V, 30 A SiC Mosfet, having a static typical drain-source on-resistance equal to 64 mΩ: **SCT070W120G3AG**.
Initially, the SC time-to-failure ($t_{SC_{Failure}}$) will be investigated and the critical energy (E_{CRIT}) identified for the given part number. Tests will be performed in the range of 50% to 70% blocking voltage. Afterward, three batches will be prepared. The samples belonging to the first one will not be subject to short circuit. The samples belonging to the second one will be subject to repetitive short circuit at damaged conditions (point 1 above) and, finally, the ones belonging to the third one will be subject to repetitive short circuit at no detectable damage conditions (point 2 above). Next step will be to power-cycle the samples belonging to the three batches. In fig. 1.5 is showed the expected results. in terms of VDS,ON degradation during power-cycling tests.

The procedure tasks of this project are the following: 1)IRT Saint-Exupery will be in charge of the short-circuit tests and post-failure analyses; 2) AAU will be in charge of the power-cycling testing [19]; 3) Electrical characterization will be considered by both research units.

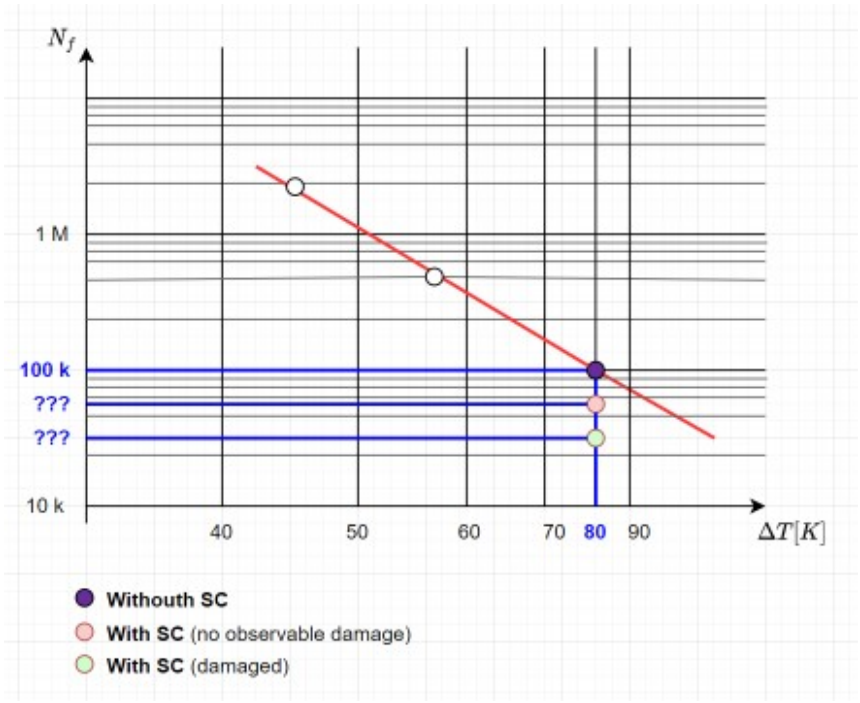


Figure 1.5: Expected results of the study case expressed in number of failure over temperature difference.

Final step is extrapolate a low to correlate the number of cycles and the SC energy.

1.2 Limitations

The power cycling (PC) test takes a lot of time to be performed; the expected time for the culmination of the ISLE project is around 1 year. Therefore in the following thesis will be addressed just some parts of its. Furthermore, during the analysis particular attention should be paid to distinguishing between the effects of V_{th} increase and the one related to metallization degradation; then the stress tests will be conducted on a substantial number of samples for each family, this due the mismatching of the component parameters introduced during the manufacturer process. Another aspect that should be taken into account is the lack of availability of the equipment, this has led some delays in the developing of the project, because a pre-existing equipment has been adapted to perform the test.

1.3 Thesis Outline

To summarize, the points addressed in this master thesis work follow. The thesis consist in four parts:

1. An overview about SiC's Technology and about the physical parameters of the material and of components created with it. Furthermore, a focus about some of the parameters that characterise the components is needed to figure out who are more interesting for our analysis.

2. The characterisation procedure to extrapolate the parameters responses of the components, to do that a dedicated equipment will be used, it is the Keysight B1506A.

3. Explanation about Power Cycling, which are the parameters sampled and how.

4. Final consideration regarding the results.

Chapter 2

SiC Technology

Silicon is used and it has been used in very wide number of applications, but due its characteristics has a quite important limitations, thus in past new materials have been studied. The component made with new material, like SiC and GaN, are defined as high electron mobility transistors (HEMT) due to their capability to allow a higher velocity for electrons that pass through them. To give an simple example of the incredible advantages that these new materials can bring into the electronic world, is reported in [27] an example of application. As reported in article [27], if a withstand voltage of 5000V is to be obtained, the Si power device with a substrate material doped with $2.5 \times 10^{13}\,\mathrm{cm}^{-}3$ requires a drift layer thickness of 0.5 mm and an area resistance of $10\,\frac{\Omega}{\mathrm{cm}^2}$, while the SiC MOSFET with a drift layer doped with a concentration of $2 \times 10^{15}\,\mathrm{cm}^{-}3$ only requires a thickness of 0.05 mm and an area resistance of $0.02\,\frac{\Omega}{\mathrm{cm}^2}$. SiC power devices allow the use of thinner drift regions to maintain higher blocking voltages, significantly reducing forward voltage drop and conduction losses.

To figure-out which material between Si and SiC is the best for the power application in table 2.1 are listed some physical & electric parameters, with a carrier density equal to $10 \times 10^{16}\,\mathrm{cm}^{-3}$ at room temperature. Since the saturated drift velocity of electrons in 4H-SiC is twice the value of Si, SiC devices are able to reach higher switching speeds with lower power dissipated. One more aspect to takes into account is the internal breakdown field, in tab 2.1 can be seen that the breakdown field in 4H-SiC is three times higher than Si, that means the dimension of the chip could be smaller and it allows to operate at higher voltages. A correlated aspect to high breakdown electric field inside the SiC components is the reliability of the oxide. SiC based devices have a native insulator, as well as the Si components, the silicon dioxide (SiO_2). It is an amorphous material used in microsystems as a dielectric to isolate various electronic elements. Thin films of oxide are easily grown or deposited on silicon wafers using a variety of techniques[20].
Up to now a quick overview about the relevant parameters have been accounted,

Physical characteristic	Si	4H-SiC
Bandgap energy (eV)	1.12	3.26
Breakdown field parallel to *c-axis* (MV/cm)	0.3	2.8
Electron mobility parallel to *c-axis* at 300 K ($cm^2/V \times$ sec)	1000	1200
Relative dielectric constant	11.8	10
Thermal conductivity ($W/cm \times K$)	1.4–1.5	3.3–4.9
Electron Saturated Drift Velocity (10×10^7 cm/s)	1	2.2

Table 2.1: Overview of the material properties of Si and 4H-SiC.[18] [7]

now a brief focus on what are the real qualities that bring SiC to the top of the market is needed. SiC is an exceptional wide bandgap semiconductor, in the sense that control of both n- and p-type doping over a wide range is relatively easy. As is listed in tab. 2.1 4H-SiC has a very high bandgap value, just to be precise the band gap is the distance expressed in eV from the conduction band to valance band, the effective densities of states in the conduction band N_C and valence band N_V can be calculated and for this material at room temperature they are $1.8 \times 10^{19}\,\mathrm{cm}^{-3}$ and $2.1 \times 10^{19}\,\mathrm{cm}^{-3}$, respectively. These two values are important as they allow to estimate whether the material will be degenerate when heavy impurity doping is performed. Knowing these two parameter the intrinsic carrier concentration can be extracted by eq. 2.1.

$$ni = \sqrt{N_C N_V} \exp\left(-\frac{E_g}{2kT}\right) \tag{2.1}$$

At room temperature its value is $5 \times 10^{-9}\,\mathrm{cm}^{-3}$ (for the silicon the intrinsic concentration is $1 \times 10^{10}\,\mathrm{cm}^{-3}$), this result is due the larger band gap. This is the main reason why SiC electronic devices can operate at high temperatures with low leakage current [18].
Another important parameter is the *mobility*, the formulas used to calculate the values for electrons and holes mobility in 4H-SiC is reported in eq. 2.2 and 2.3.

$$\mu_{e^-} = \frac{1020}{1 + \left(\frac{N_A + N_D}{1.8E17}\right)^{0.6}} \tag{2.2}$$

$$\mu_{h^+} = \frac{118}{1 + \left(\frac{N_A + N_D}{2.2E18}\right)^{0.7}} \tag{2.3}$$

Along the c-axis in the crystallographic structure of the 4H-SiC, the mobility for electrons is approximately 1200 $\frac{\mathrm{cm}^2}{\mathrm{V}\times\mathrm{sec}}$ and for the holes is 120 $\frac{\mathrm{cm}^2}{\mathrm{V}\times\mathrm{sec}}$ at room temperature, this is one of the major reasons why 4H-SiC is the most attractive polytype for vertical power devices fabricated on SiC[0001] wafers. At high temperature, the

doping dependence of mobility becomes small, because the influence of impurity scattering decreases. In general, the temperature dependence of mobility is discussed by using a relationship of $\mu \sim T^{-n}$ [18].
A further parameter that markedly bring SiC as the most suitable compound material to produce power electronic components is the *Breakdown electric field*. At the moment when a very high electric field is applied to a p-n junction or Schottky barrier in the reverse-bias, the leakage current increases generating electron–hole pairs and the junction ultimately breaks down. Exist two different braking mechanism and they occur in two distinct situations, one is the *avalanche breakdown* and the second is the *tunnelling breakdown*. The breakdown field for 4H-SiC is 2.8 MV/cm which is approximately nine times bigger than the breakdown field of Si 0.3 MV/cm, at the same value of doping. Into a junction with a lightly-doped region, avalanche breakdown is predominant, this is the case for most power devices[1]. In his case the carriers can gain enough energy to excite electron hole pairs and the generation of e/h pairs is multiplied inside the space charge region of a junction, this condition can lead to breakdown. The critical voltage that cause the breakdown in a Schottky barrier diodes or a one side p-n junction is expressed by eq.2.4.

$$V_B = \frac{E_B X_{BD}}{2} = \frac{\epsilon_s E_B^2}{2qN_D} \tag{2.4}$$

Where E_B is the critical electric filed straight, ϵ_s is the dielectric constant of the material, q is the charge of electron in free space and the N_D is the concentration of the impurities (donor concentration) introduced into the semiconductor. Moreover, for a given V_B, SiC power devices could be made thinner than the Si devices. The minimum width of the Drift (W) region is in general limited by the need to contain the entire depletion region which extends with the applied blocking voltage[1]. When the doping density is increased, the width of the space-charge region becomes small and the distance for carriers to be accelerated becomes short. Furthermore, the mobility is reduced in highly doped materials because of enhanced impurity scattering. These are the reasons why the critical electric field strength apparently increases with increasing doping. From the literature can be seen that this characteristic of hexagonal SiC polytypes is the main reason why SiC is very attractive for power device applications [18].
Owing to the high critical field strength and high electron mobility along the c-axis, 4H-SiC exhibits a significantly higher qualities and properties than other SiC polytypes. This is a another reason why 4H-SiC has been almost exclusively employed for power device applications.
A parameter that is sure to be reported is the *Thermal Conductivity*, that indicates how fast is the rate of transfer of heat generated inside the component. This parameter in 4H-SiC is almost three times larger than Si, so for power components it is so relevant and it's understandable why SiC is used to produce power de-

vices, because having higher thermal conductivity value enables a reduction of the thermal resistance of the semiconductor device, that means a larger capability to handle with high current and high voltage without entering dangerous operating zones.

2.1 Structure of MOSFET and developing

During the years even more typologies of mosfes have been developed, in fig. 2.2 is shown the base structure of a n-mosfet based on SiC (to be precise, the base structure of a Si mosfet is the same). The entire structure is grounded on a SiC substrate layer which has been doped by elements belonging to the third group, they have just three valence electrons (Silicon and silicon carbide atoms have 4 valence electrons), thus the introduction of these elements into the crystal reticle of SiC creates free spaces, they are called holes, in which electrons can go and stand there. Instead the parts indicated with n are created introducing into the SiC crystals elements belonging to the fifth group, they have 5 valence electrons. To resume, the conduction of a current in p doped area is related to the movement of the holes, instead in a n doped area the current is created from the movement of electrons (electrons in this type of mosfet are the majority carriers). The majority carriers are the most relevant causes for the current in a mosfet components [18]. The base structure of a planar mosfet is reported in fig.2.2, as can be seen three terminals are present (plus one that is put equal to reference ground): Gate, Source and Drain. Appling well-known levels of voltage between these terminals a current is allowed to pass through the component, or better a depletion region is formed and after that an inversion layer can be created between the drain and source, it allows a current to flow.

In this chapter and in this work the goal is not to address the differences between the structures of different mosfet typologies and their functionality but a small overview is needed to show the advantaged and the differences between the normal structure of the mosfet and the power mosfet. As said above, applying the correct value of voltage between the pins, the component can be controlled to perform and behave in different mode. Exist three district main working area for the mosfet, the linear, saturation and off region. They are extractable and capable from the characteristic curve that link I_D over V_{DS}, un example for that is reported in fig.2.1.

During the year companies developed new structure of for the mosfet to achieve even better characteristics than before; for the SiC power mosfet, as have been reported above, the preferable conduction direction is along the c-axis, so the configuration of the components are changed, The n+ drainage area is no longer on the upper surface and the current exits the inversion channel and flows first hori-

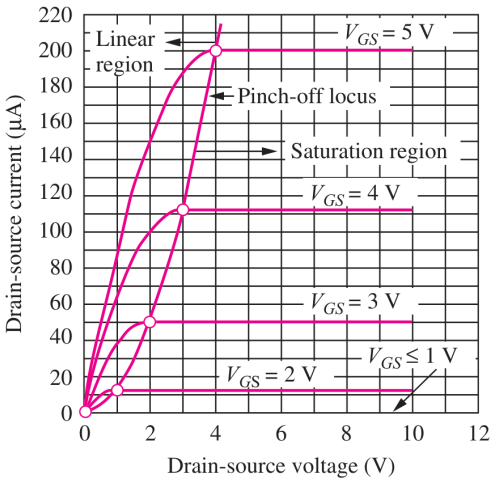


Figure 2.1: I_D over V_{DS} characteristic of a generic ideal Mosfet, in which are reported the interesting areas. [3]

zontally and then vertically through the lightly doped n-drainage region to the n+ substrate, which acts as the drain terminal. As shown in fig.2.3 two main structure has been developed, the planar one and trench one, but they are known as DMOSFET and UMOSFET, respectively. DMOSFET because the n+ source and p base regions are formed by diffusion of n-type and p-type impurities through the same mask opening, whereas the UMOSFET derives from the U-shaped geometry. The power mosfet incorporates the basic mosfet structure on a thick, lightly-doped n-type epilayer on an n+ substrate.

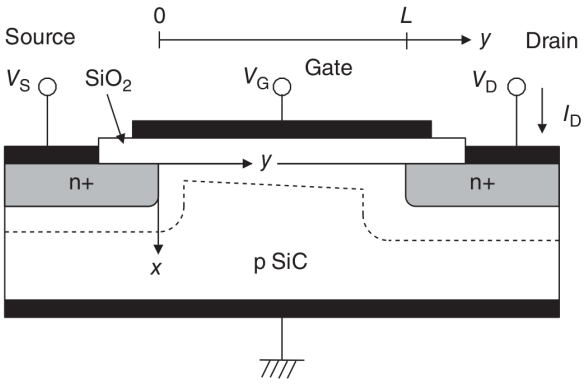
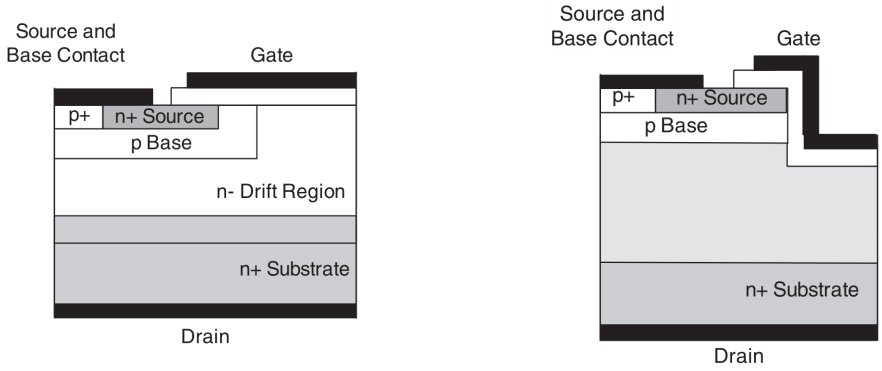


Figure 2.2: SiC base n channel mosfet structure. [18]



(a) Planar base power mosfet

(b) Trench base power mosfet

Figure 2.3: Two different structure of a power SiC mosfet [18].

2.2 Physical & Electric Parameters of a SiC Mosfet

A focus to the most important parameters of SiC Mosfet is needed to figure out better which are the most significant for this study cases and also in a general one, because the pertinent physical and electric quantities analysed during the characterization, or during a study case, of a component are basically the same; however sometimes some parameters are more important than other.
To understand the quality of a component exist a very wide range of parameters, that, as been said above, allow to extrapolate the functionality characteristic: below a list of electrical and physic parameters are reported:

- R_{DS}: The resistance seen between the Drain and the source.
- V_{TH}: The threshold voltage correspond to the gate-source voltage at which a significant drain current starts to flow.
- $V_{DS_{ON}}$&$V_{DS_{OFF}}$: The drain-source voltage is the potential difference measured between the drain and the source pins.
- S_iC/S_iO_2 *Defects*: The interface between the semiconductor and the insulator can have some defects that modify the functionality of the component.
- *Junction Temperature*: The T_J is the junction temperature of the SiC die.
- *Gate oxide Reliability*: The reliability of the gate oxide is related the manufactured quality of the insulator layer inside the component.

In order to provide a broader overview of the effects that each of these parameters can have during the operation of a SiC Mosfet, a brief description of each is needed. Thus below has been reported, for each item cited above, a description about its behaviour in a SiC Mosfet.

R_{DS} The resistance seen between the drain and the source in a Mosfet is the union of few small resistance that are present inside the semiconductor chip and also the resistance of the connection from the chip to the case (in some cases this resistances are neglected because very small). The n+ drain is no longer at the surface, and instead the current exits the inversion channel and flows vertically through the lightly-doped n-drift region to the n+ substrate, which acts as the drain terminal. Consequently, the on-resistance of the power MOSFET is the sum of the on resistance of the fet channel plus the on resistance of the drain drift region and the substrate. As reported before exist two main topologies of power mosfet, the planar and the trench configuration, that mean there will be some differences between the R_{DS} of them. Below in fig.2.4 and fig.2.5 are shown the main contribution of each layer on the total resistance in the two difference structure. For the planar power mosfet

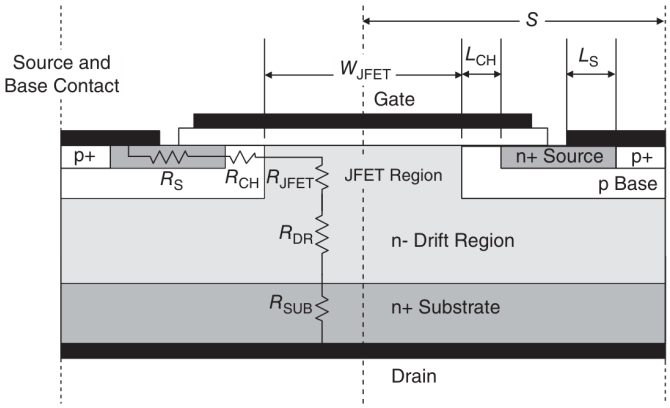


Figure 2.4: Internal resistance inside a power DMOSFET [18].

the resistance seen between drain and source is defined by the equation 2.5, follow [18]:

$$R_{ON_{SP}} = R_{CH,SP} + R_{DR,SP} + W \times S \times (R_S + R_{JFET} + R_{SUB}) \tag{2.5}$$

Here R_S represents the resistance of the source contact and the n+ source region, R_{JFET} is the resistance of the vertical JFET gated by the grounded p base regions, and R_{SUB} is the resistance of the substrate and its ohmic contact. And W and S are the width and half-pitch of the cell. For the trench power mosfet the effect of the JFET region has been deleted, so it is reasonable thinking that the total resistance in lower than planar one [18].

V_{TH} The threshold voltage of the mosfet is the lowest level of tension that up to that the current starts to flow through the drain and source. Another way

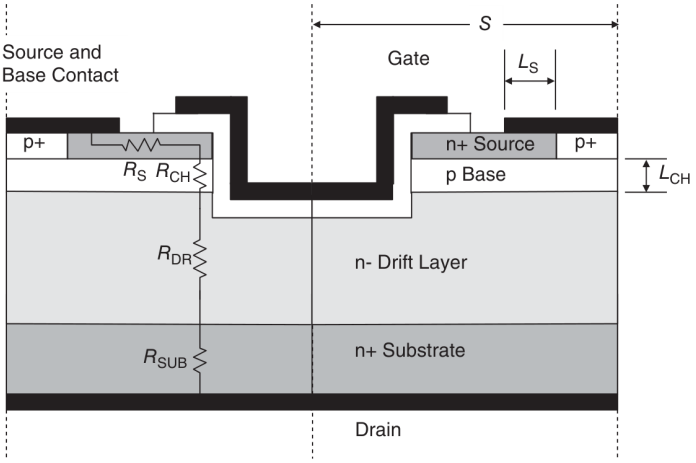


Figure 2.5: Internal resistance inside a power UMOSFET [18].

to define it as the a voltage applied to the metal electrode to enter in strong inversion and when the surface of a semiconductor enters in strong inversion condition, the surface potential is equal to twice the bulk potential. The V_{TH} in a SiC mosfet is affected by trapping phenomenon [12] and when the junction temperature of the component increase the intrinsic carrier density rise and this bring a decreasing of the V_{TH} in relation with the temperature. If the temperature stress is continuing during the time, the SiC mosfet degrades due the accumulated electrons trapped in the gate oxide and the V_{TH} increases [30].

V_{DS} The voltage across the drain and the source in a Mosfet is called V_{DS} and it can be distinguished in two: $V_{DS_{ON}}$&$V_{DS_{OFF}}$ during the t_{on} and t_{off} time respectively. The value of the voltage indicated as $V_{DS_{ON}}$ is defined by the current that pass through the channel and the relative resistance during that interval of time, $R_{DS_{ON}}$. The value of those resistance has been defined above and it has a strongly dependence by the controlling voltage (V_{GS}) and the threshold voltage V_{TH}. The value of the voltage indicated as $V_{DS_{OFF}}$ is affected by some parameters, as V_{GS} and from the conduction of the body diode. Because in the SiC mosfet the channel is not completely closed with $V_{GS} = 0V$ [30] and this bring some changes in the behaviour of its. This aspect is well addressed in chapter 4.

S_iC/S_iO_2 ***Defects*** The defects in the gate oxide and in the interface between the semiconductor and the insulator are basically: mobile ionic charges, oxide trapped charges, fixed oxide charges, S_iC/S_iO_2 interface traps and near interface oxide traps. To have a better interpretation, in fig. 2.6 is reported a

small image found in an article of literature [28] that show the differences between the different defects. The fixed charge is correlated with the oxidation process. The oxide trapped charges can be induced by ionising radiation and avalanche injection. The interface traps and near interface oxide traps can be attributed to structural defects. [28] The threshold voltage are mainly affected by the interface and near interface oxide traps and that bring a faster degradation of the SiC mosfet.

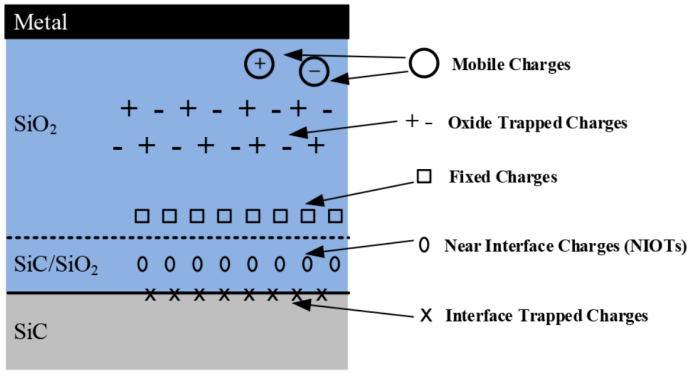


Figure 2.6: Simplified schematic diagram with reported main defects in the SiC mosfet [28].

Junction Temperature The theoretical working junction temperature in the SiC mosfet is quite higher than the Si mosfet counterpart. Furthermore, the higher thermal conductivity enables a reduction of the thermal resistance of the semiconductor device, that means a larger capability to handle with high current and high voltage without entering dangerous operating zones; but due to the structural defects and the problem during the manufacturing, the theoretical working temperature is not reached yet.

Gate oxide Reliability High level of temperature can induce broking mechanism of the silicon dioxide. This bring a creating of a conductive path between the gate and source. The I_G increases and the V_{GS} dips to zero [8]. The reliability of the gate oxide in a SiC component is affected by different factors:
the density of interface traps is very high because of the presence of carbon atoms during the thermal oxidation of SiC and defects formed during the process. The density of charged interface defects and interface states in S_iC/S_iO_2 structures is still quite high and these are the possible root reason for the reliability and ruggedness of SiC mosfet.
The tunnelling effects are more present in the S_iC/S_iO_2 than in the S_i/S_iO_2, due to the small energy band offset between the semiconductor and the oxide. Furthermore, the SiC components have a higher tunnelling current with

the same value of electric field; when the temperature increase the effective barrier height in the interface between the S_iC/S_iO_2 dips.
At the end the higher critical electric field allowed by SiC material, may cause failures inside the gate oxide [28].

To resume wide bandgap materials power electronic components are faster, smaller, more efficient and more reliable than their Si-based counterparts; furthermore, they permit the operation of devices at higher voltages, temperatures, and frequencies, making it possible to reduce volume and weight in a wide range of applications. SiC has highest thermal conductivity compared than Si, indicating that SiC devices can operate at higher power densities, that means SiC components produce much lower heat and thus the temperature will rise much more slowly. Wide bandgap devices can operate at a voltage 10 times higher than Si-based power devices, because of their higher maximum electric field and operating temperatures of well over 300°C, twice the maximum operating temperature of Si-based devices. [9] Thus the components manufactured with SiC look like the best compromise to handle high power.

2.3 Expected SC effects

According to the reported literature, discrete SiC mosfet devices can withstand an SC event for a shorter time than the Si components counterparts [28] and this can be see from the fig.2.7 . The main reason is that their much smaller chip size and larger power density than Si components. Thus, the SC issues of SiC mosfet needs to be addressed for further performance improvement and to do that the failure mechanism has to be studied. Self-heating of the mosfet due to the short-circuit event is the most influential parameter, this processes is related to the increase of the device temperature, since temperature influences a multitude of physical quantities of any semiconductor [8]. When a SC events occur the drain current first rise up and then dips as the device temperature increases, due to the negative thermal coefficient. Furthermore, the threshold voltage of the MOSFET decreases. The level of the drain current is strictly related to the applied gate voltage from the relation [18]:

$$I_D = \mu_N C_{OX} \frac{W}{L} \left[(V_{GS} - V_{TH})\, V_{DS} - \frac{1}{2} V_{DS}^2 \right] \tag{2.6}$$

Thus, higher is the gate voltage higher is the current peak during the SC event.

However from the literature [28] can be distinguished two different failure mode for the SiC mosfet due to short circuit:

- Gate terminal shorted with the source and the PN junction is the remains blocking capability. The main key factor for this type of failure is the V_{GS} value.

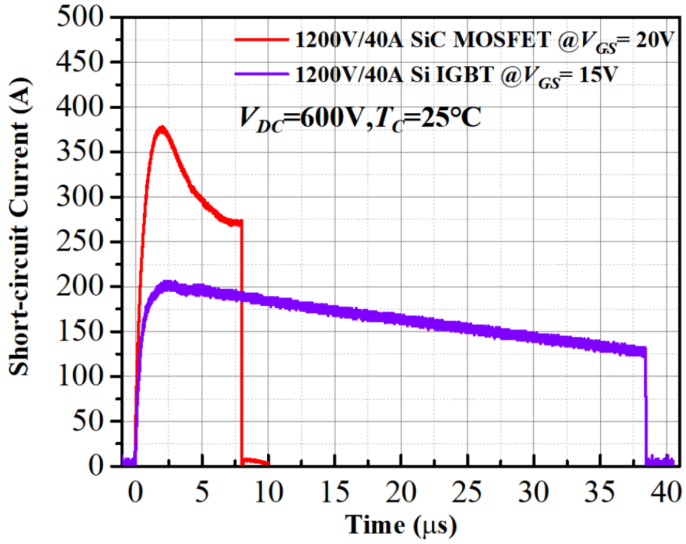


Figure 2.7: SC current comparison of the $1200V$ / $40A$ SiC MOSFET and $1200V$ / $40A$ Si IGBT under $V_{DS} = 600V$ and $T_C = 25C^{\circ}$[28]

- All three terminals of the component are shorted, this case is recognized as thermal runaway. The main key factor for this failure is the bus voltage value.

Therefore, when a SC event is applied to a SiC mosfet, great care must be taken not to break the component under test.

Chapter 3

Device Characterization

The characterisation of a component consists in extracting its parameters. A SiC MOSFET or every electronic component has an enormous number of physical quantities that can be measured; as reported in chapter 2, section2.2 some parameters are linked with others, furthermore it exists a very close connection between them; obviously there will be some parameters more affected than others and some that will be independent. Thus, one of the first step in a project is to figure out which of them are relevant, fortunately in chapter 2 they are already pointed. It is important to bear in mind that, when talking about an integrated semiconductor component, one expects its parameters to be strongly interrelated, considering that the device is constructed into a single piece of semiconductor. This last sentence has been largely discussed and analysed considering the effect using a new semiconductor material that allows the construction of new components using even smaller quantities of semiconductor, see chapter 2.
However, the choice of the important parameters has been taken in advance, as reported in 2.2. In this chapter the focus is to report the measurement evaluated before the stressing procedure (stressing means DC power cycling); in chapter 1 all the three different study cases have been expounded; a small recall of them is mandatory, thus the three families of components that will be evaluated are:

No Short circuit : This family is the one that did not get stressed, it means the components belonging to it have characterised directly out from the manufacturer. Thus, they did not receive any stressing procedure (like SC and PC), the expected behaviour should match with the data provided by manufacturer on the data-sheet; it is important to bear in mind that due to the mismatch and variation of the parameters, there will probably be some variation, but this fact has been taken into account previously. For that reason, several components will be characterized.

Short circuited with damage : SiC mosfet are especially susceptible to damage as

a result of short-circuiting events due to their fast switching speeds and very low on-state resistance. As reported in [22], the current passing through a SiC mosfet during a short circuit event can exceed 10x the nominal rating with 10-20 microseconds after turn-on. In this case the parameters extracted by the analyser after short-circuit event will not match with those extracted by the components at which the SC haven't been performed.

Short circuited without visible damage : In this batch the SC has been performed but below the critic energy (E_C), that value has been extracted in in a step before. Thus, the curves expected behaviour should be the same, or better, should be in the range of the variation found in the first case, for the component at which the SC was not performed.

The equipment used for the study and for extrapolation and derivation of the parameters and curves is a dedicated analyser, the owner company of the project and the seller is the Keysight; the device is the Keysight B1505A. It is a single-box solution with the capability to characterize high-power devices from the pico-ampere level up to several hundred ampere, as well as for the voltage. All the features are available and reported in [16]. The components have been characterized are SCT070W120G3AG from STMicroelectronics, since they are power components is reasonable thinking the package is also made to handle for high power level of voltage and current; since they are designed to have a blocking voltage equal to $1200V$ and constant current entering thought the drain equal to $30A$ at 25°, it's understandable that the construction of the container in which the DIE are arranged, has to be consistent with the power level. The following components are provided in two different power packages: TO-247 *3 pins* and TO-247 *4 pins*. The main difference between them is the number of pins, to be precise in the *4 pins* the source contact is divided in two, or better, the source contact has two pins, one used for the power connection, so current flows out of this pin and in from the drain, and the another one is the sense connection, as known as kelvin source, this pin is used to have a very clean and precise measure of the source potential because the kelvin source is arranged closer to the DIE than the power source pin. Furthermore, the *4 pins* introduces a higher efficiency in the switching losses, as reported in [24], due the gate voltage relevant effects, because the gate voltage affects also the R_{ON}. In fig. 3.1 it can be seen the structural difference between the two configurations, the increasing of the efficiency in the *4 pins* can be explained looking at the right-hand figure and observing that using the kelvin source as reference to control and to apply the gate signal, the parasitic inductance coming from the source power pin has been neglected, so that the V_{GS} needed to turn-on (or better, to enter in the inversion layer) the component is lower because the voltage across the stray inductance is not present.

The Keysight B1505A Power Device Analyzer has a very well defined measure-

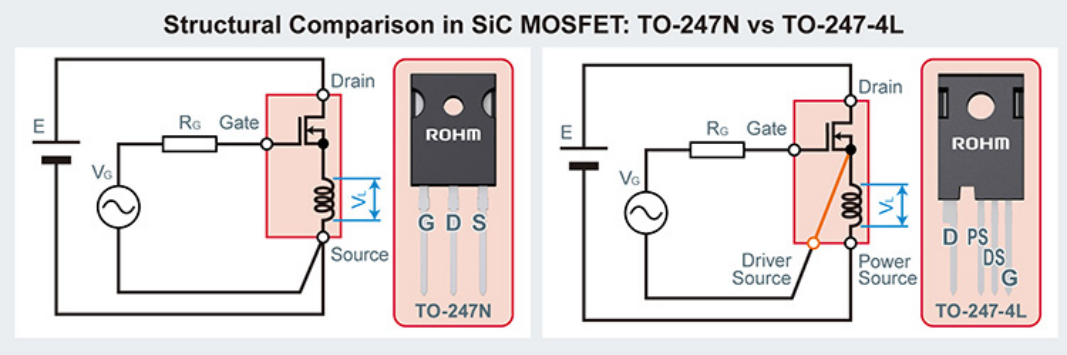


Figure 3.1: Structural differences between TO-247 *3 pins* and TO-247 *4 pins* [24] .

ment procedure and also the connections are pre-set, but to be able to measure a real component another equipment is needed, that creates the connection between the B1505A and the DUT (device under test). The mid component is the N1265A Ultra high current expander/fixture which contains the current expander to enable $500A$ output and measurement, and contains the selector to switch the measurement resource connected to the DUT.
The measurement chain is reported in the graph 3.2 and as can be seen, between the DUT and the N1265A there is an adaptor, which is needed just to create a well-done connection between the DUT and the cable coming out from the expander. The final data come out from the B1505A and they can be used in several different ways, in our case the interest measurements are: I_D/V_D, I_D/V_G, $I_{G_{SS}}$ and $I_{D_{SS}}$. However, the N1256A was designed in such a way as to separate the power and sensing connections. As can be see in fig.3.3, every pin of the DUT has two possible connections, one for the force and one for the sense (except the gate, it still have two cable, this for apply a gate signal with a modifiable reference point). In this case is reported a n-mosfet in a TO-247/4 package, where the sense pin for the source is the kelvin source, so at the end in total, to perform the measurements that we need, 6 connections are needed; it is important to bear in mind that the same number of connections is required also with TO247/3 package.

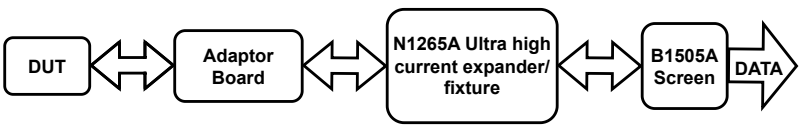


Figure 3.2: Flow chart of measurement chain using Keysight products.

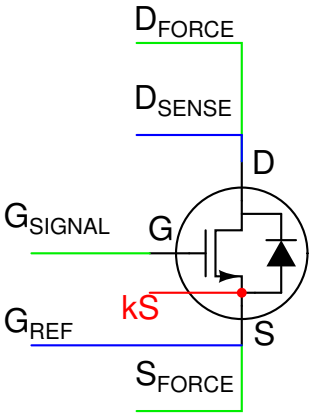


Figure 3.3: Division of power and sense connection in a mosfet with package TO247 4 pins.

An additional difficulty introduced in this project was the lack of an adaptor board for the TO247/4, therefore a new adaptor board has been designed following the guideline provided by Keysight in [17]. The crucial step was to create a board that fit with the required packages (TO247/3 and TO247/4) and that allowed to perform correctly the measurements, thus creating, as mentioned above, the connection for the force and sense cable. To address the problem about the two different packages a new footprint has been developed, it was to be allowed to install in the same adaptor two different components (not at the same time) with mounting structure markedly different, thus a 5 pins foot print has been extrapolated through superposition of the pins. The following footprint is reported in fig. 3.4 and the in the upper side are indicated the enumeration of the pins for the package TO247/3 and in the lower side for the TO247/4.

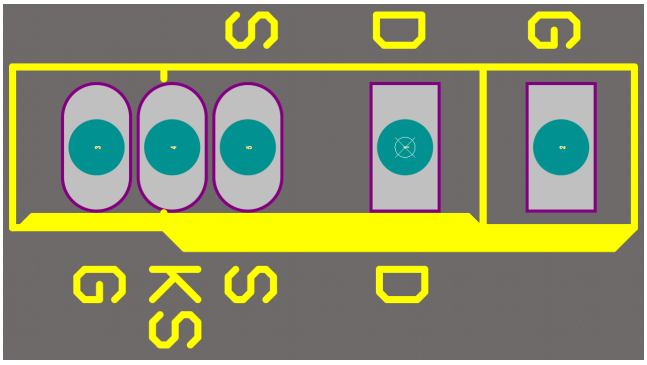


Figure 3.4: Footprint for installation of TO247/3 an TO247/4.

This approach was also adopted for the next phase, the DC power cycle, but

this is better detailed in the chapter.4. The hole and the pads are oversized to make installation and disassembly easier, but in the final project it is added also the dedicated socket, that allows an easier installation without the use of solder. The final project and a picture in which are reported all the connections and the DUT in a real case are reported in fig.3.5 and fig.3.6, respectively. In fig. 3.5 the 5 pins footprint can be pointed and it is on the right-hand side of the board, instead in the center there is the socket adaptor. One thing can be highlighted and it's that for the gate, there is just one connector, this because the gate in the mosfet should absorb a very small current, so the force and the sense connections has been merged. In

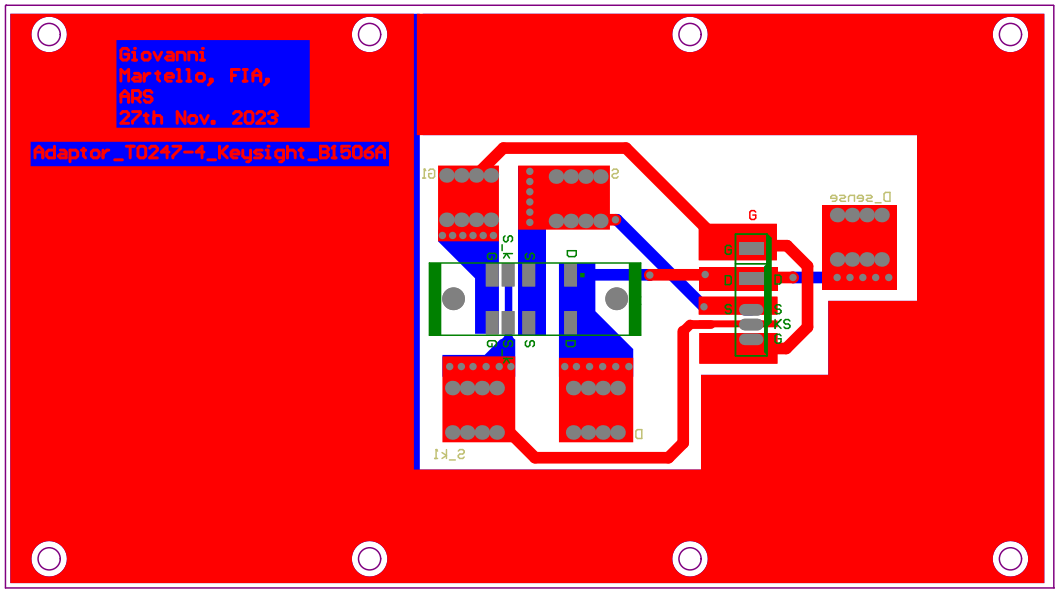


Figure 3.5: PCB board of adaptor, here is highlighted the top layer.

fig.3.6 the DUT can be seen on the left-hand side of the board and the connections, the red connector are used to indicated the high side, that means the drain, the black for the low side, so the source, and the last one, the yellow is used for the gate control.

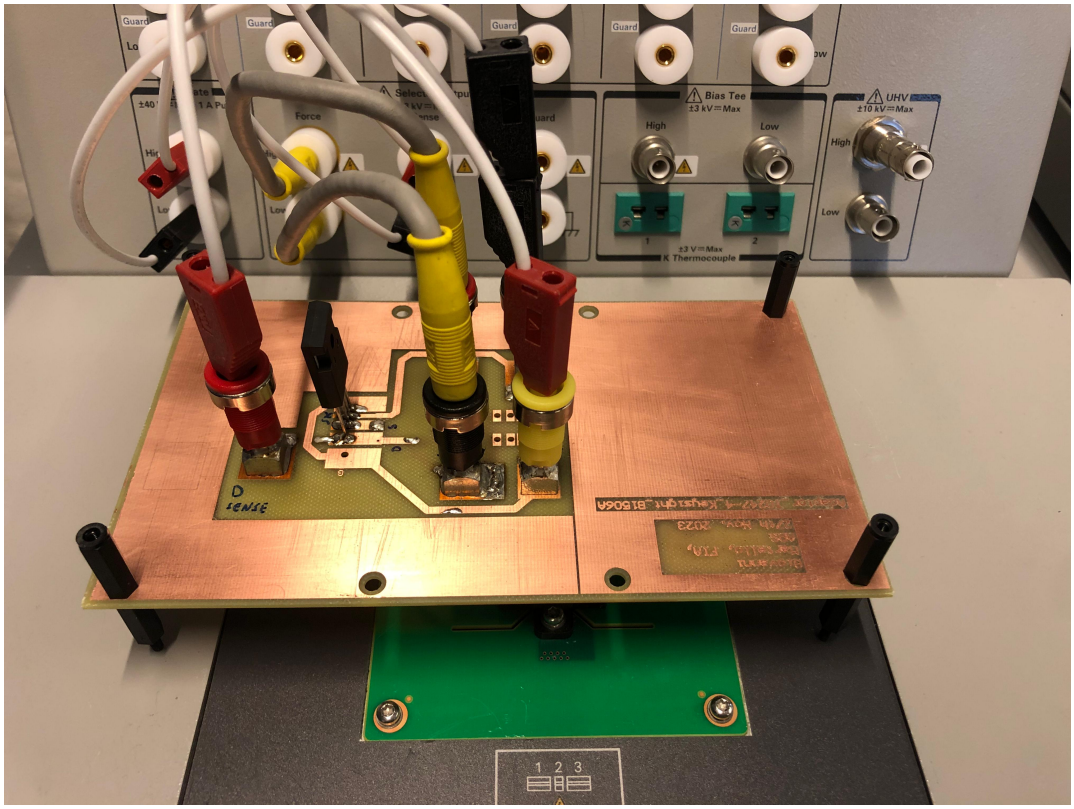


Figure 3.6: Picture of DUT and adaptor board connected to the analyser.

3.1 Measurements of interest

During the characterization of components several measurements can be performed. The measurement chain using the Keysight's product are able to extract a lot of information from a DUT, but in this project just of them are needed and relevant. The curves of interest are: I_D/V_{DS}, I_D/V_{GS}, $I_{D_{SS}}$ and $I_{G_{SS}}$. A short explanation about the circuit connection used to extract the correct curve in each measurements is useful to understand how the measurement has been performed. Below are reported a short description of each different circuit used:

I_D/V_{DS} During the extrapolation of the following curve, the focus is to check the behaviour of the component under different values of gate voltage, the measurement circuit carried out by Keysight B1505A is reported in fig. 3.7. As reported in blue, the gate and the drain voltage are steeped up and down during the measurement. To address in a complete way this quantification of the component, the working procedure is explained: the voltage V_{DS} is setted to start from an well defined value up to the maximum set value, this sweep

has been performed for every prearranged gate voltage, because also the V_{GS} is changed and as can be see in fig. 3.11 the curve I_D/V_{DS} has been plotted at 8 different gate voltages. Thus for every value of gate voltage, the drain voltage is swept, from the minimum up to the maximum value and at the meantime time the current of the drain is sampled. The reason for changing the gate voltage is to extract a graph to recognise the saturation and linear working region of the mosfet. Furthermore, it is interesting to analyse the behaviour of the mosfet in the presence of a high current at different gate voltage.

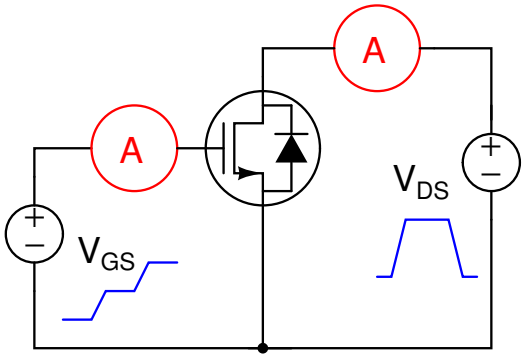


Figure 3.7: Conceptual electric schematic to measure the value of interest, for I_D/V_{DS} graph.

I_D/V_{GS} This curve in the most part of the cases is plotted to extract the threshold voltage of the mosfet. It is the value of the voltage at which significant current starts to flow through channel, or it is the voltage applied to the metal electrode to enter in strong inversion and when the surface of a semiconductor enters in strong inversion condition, the surface potential is equal to twice the bulk potential. The tipical way to measure the V_{TH} is short together the gate and drain, but in this case Keysight decided to perform in a different way, so that a new connections weren't needed, as reported in [16], both gate and drain voltage sweep at the same potential by synchronizing two SMUs. Then in order to decide what the V_{TH} is, it is sufficient to decide for which drain current the threshold voltage is considered to have been reached. To compare the results extracted by measurements with the data obtained from the data-sheet of manufacturer the same drain current should be taken into account, however this aspect is addressed in the section 3.2. The simplified schematic measurements chain used to extrapolate the V_{TH} is reported in fig.3.8, the dotted line indicates the hide connection created internally in the B1505A [16].

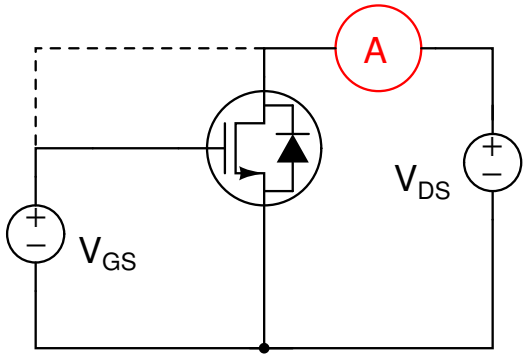


Figure 3.8: Conceptual electric schematic to measure the value of interest, for I_D/V_{GS} graph.

$I_{D_{SS}}$ The leakage current that occurs when a voltage is applied across drain and source with gate and source short-circuited is defined as $I_{D_{SS}}$. As in the previous points a simplified electric measurement is displayed below, it can be see in fig.3.9. The ideally value of leakage current in a mosfet should be equal to zero ampere, but every real component has non-idealities characteristic and one of these is the gate leakage current. Considering that the voltage applied on the gate is markedly below the threshold voltage, the channel is not formed, so no electrons should be able to pass through the channel, because the transistor is in sub-threshold region, or weak-inversion region.

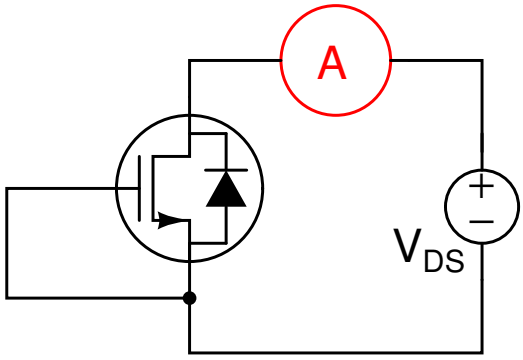


Figure 3.9: Conceptual electric schematic to measure the value of interest, for $I_{D_{SS}}$ graph.

$I_{G_{SS}}$ The leakage current that occurs when the specified voltage is applied across gate and source with drain and source short-circuited is defined as $I_{G_{SS}}$. Low oxide thickness with high electric fields results in electrons tunnelling from the substrate to the gate and from the gate to the substrate through the gate oxide, resulting in gate oxide tunnelling current.

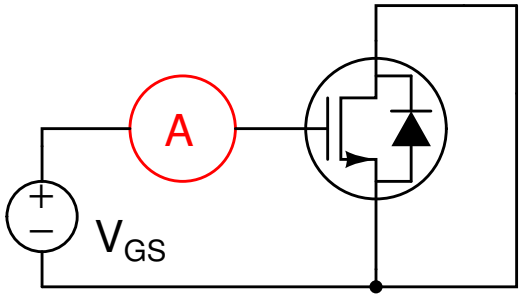


Figure 3.10: Conceptual electric schematic to measure the value of interest, for $I_{G_{SS}}$ graph.

3.2 Parameter of three different batches

3.2.1 Not short circuited

Considering that the following project is in collaboration with another university the timing of proceeding can be slow and has some delays due to the distance and the several appointment of the supervisors. For that reason up to now has been analysed just the virgin sample, those one that no stresses have been applied. The results, as discussed above, are extracted with the analyser provided by Keysight, in each graph are reported two different curve and each of those correspond to one sample.
The trans-characteristic of the mosfet is showed in fig. 3.11, and as can be seen increasing the gate voltage, the drain current markedly surges for the same value of the drain voltage, this can be explained by the equation of the current of the mosfet, that it has a linear dependency from V_{TH} and V_{GS}. In the fig.3.12 are reported the curves that allow to extract the value of V_{TH} and the two threshold voltage have a slightly difference between them, but this is normal, because their values are between the range indicated by the manufacturer. The values of the threshold voltage in the two different cases are reported in tab.3.1, the range of the V_{TH} can be sees in [26]. It is important to bear in mind that the value of V_{TH} has been measured at one specified drain current, thus to be consistent with the comparison between the manufacturer data and the extrapolated one, the drain current has been set equal to that one indicated in the data-sheet, so $I_D = 1\,\text{mA}$. It exists way more different typologies to measure the threshold voltage in a mosfet, but to be still consistent with the specification of the manufacturer, during the test (PC) the drain and source are shorted together and the current at which the threshold voltage is reached is $I_D = 1\,\text{mA}$. However this part is addressed in a more focus way below.

Now a short description of the single graphs extracted with curve analyser Keysight 1505A is addressed, first of all the graph 3.11

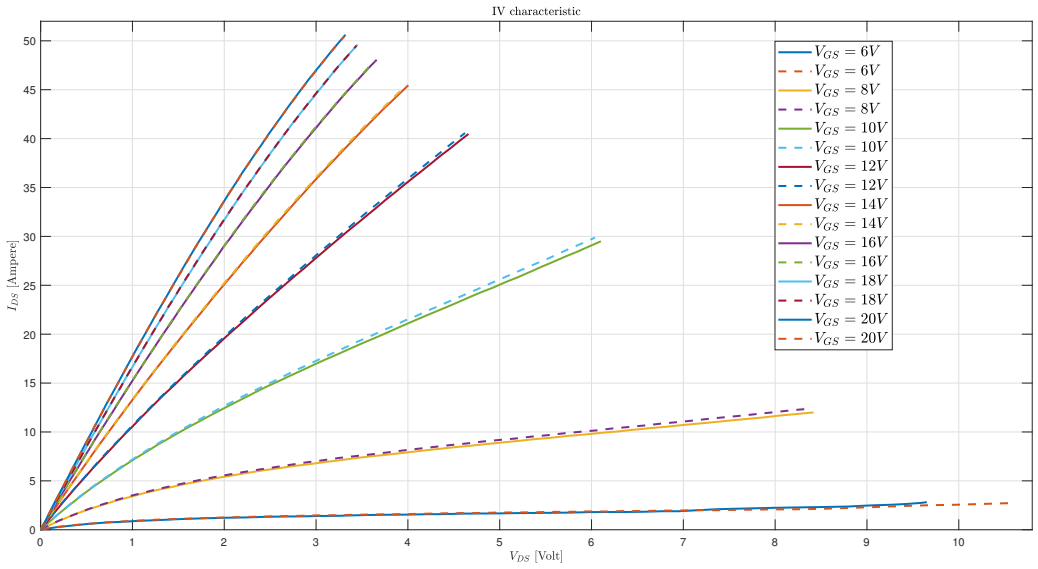


Figure 3.11: I_D over V_{DS} characteristic of DUT. Continous line is for sample one and dotted line for sample two.

	Threshold voltage
Sample 1	2.7330 V
Sample 2	2.7179 V

Table 3.1: Values of threshold voltage of the two virgin samples reported in fig3.12, the reference current is $I_D = 1\,\text{mA}$.

3.2.2 Short circuited with damages

Waiting for samples and results from the partner university.

3.2.3 Short circuited without visible damages

Waiting for samples and results from the partner university.

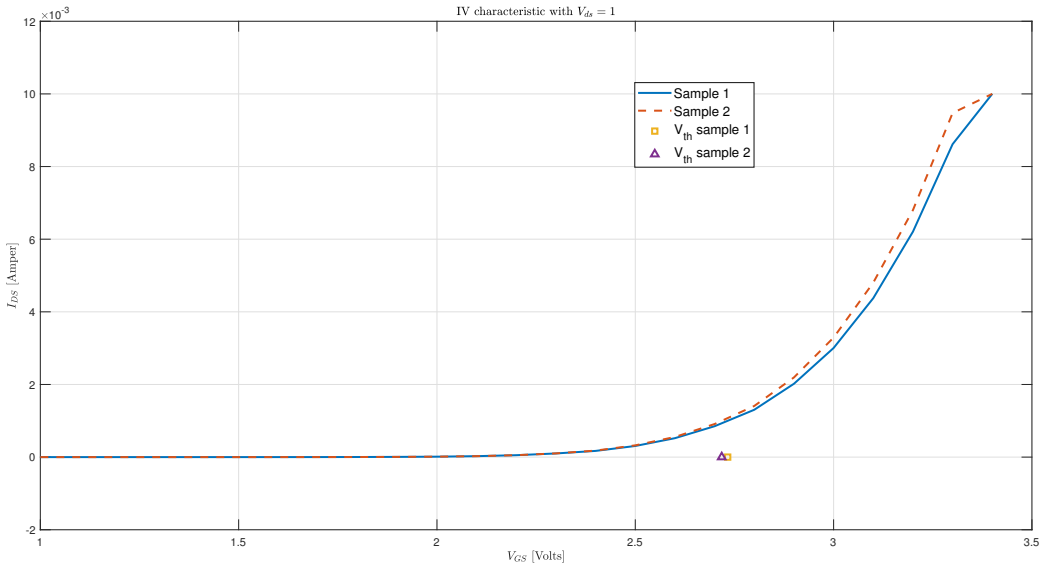


Figure 3.12: I_D / V_{GS} curves in which the V_{TH} are reported curve.

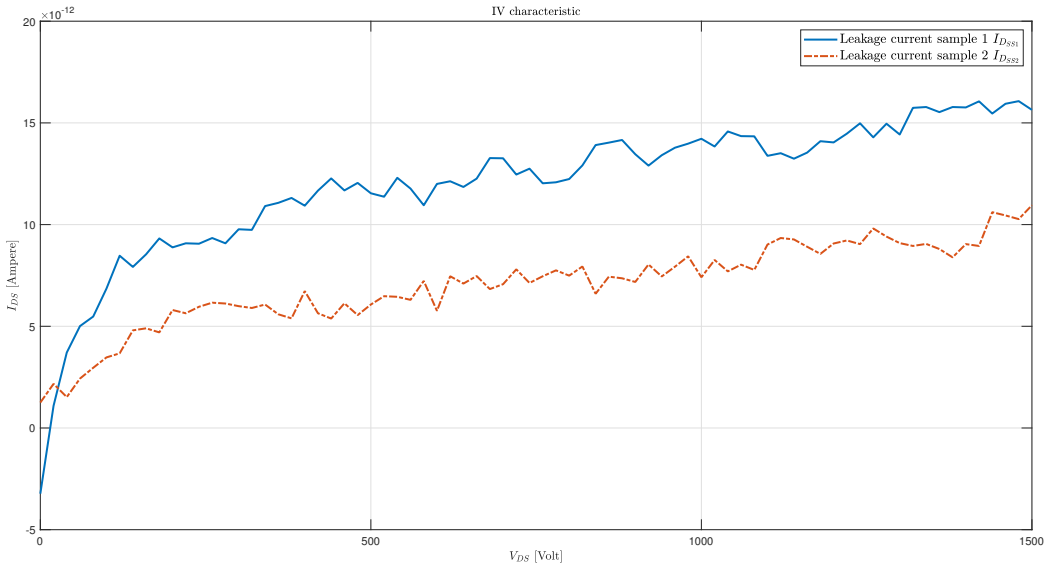


Figure 3.13: Leakage current curves on the drain.

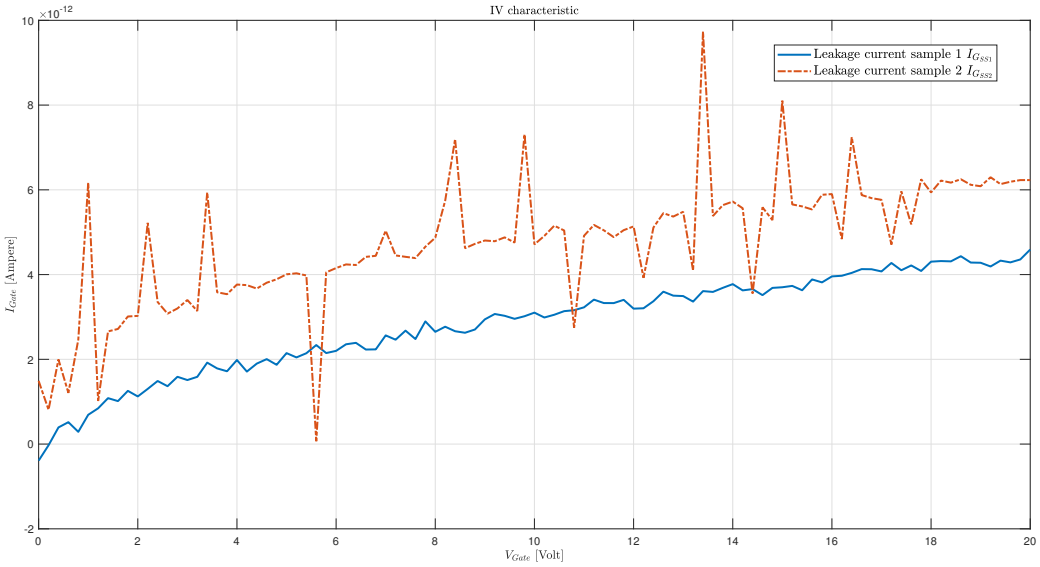


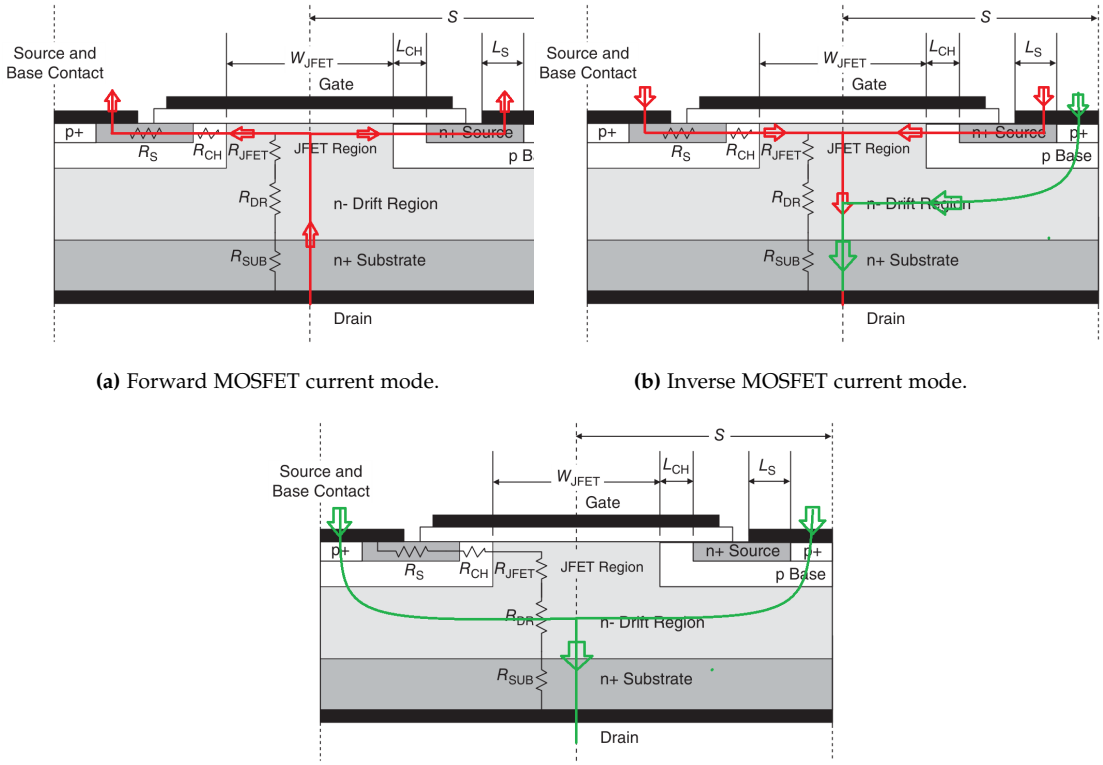
Figure 3.14: Leakage current curves on the gate.

Chapter 4

DC Power Cycling

According to a recent survey, the power semiconductor failures account for more than half of the total failures in dc–dc converters in industry [30]. As mentioned in the previous chapters, the reliability of power semiconductor devices is important as the device failures can lead to power converter malfunctions or power interruptions, which are not desirable in industry because of the penalties of maintenance cost, operation cost, and safety concerns. Thus a way to evaluate the reliability of them is so important. The classic way to extrapolate the life time of a power device is perform the Power Cycling test, that is the most important reliability test in of power electronics, normally with DC injection in conduction mode [4]. For the power device with a single conduction mode (single conduction mode means that the current has a single path in which flows, instead into the mosfet exist more than one current paths and they depend in which state the component is; furthermore the presence of body diode add a further path for the current), as IGBT, diode, the knowledge about the procedure of the test is well know. Whereas due to the unique characteristics of the MOSFET cell structure, there are three conduction modes, namely forward MOSFET mode, reverse MOSFET mode and body diode mode [4]. The different characteristics under different conduction modes lead to different PC methods, and the failure mechanisms and lifespans may vary. However, the standard of PC method for mosfet is not clearly defined, and it is mentioned that the body diode mode can be used to simplify the test process. Therefore, a precise and accurate study about the reliability of the power semiconductor device is needed, especially for the emerging silicon carbide SiC MOSFET since limited field data are available regarding its reliability [30].

As reported in literature [4] exist three different working zone for power mosfet, the forward mode, the inverse mode and the body diode mode. In the fig. 4.1 are reported te three cases mentioned above, taking into account them, it is reasonable think that the current passing through the mosfet has different behave in those three cases, so the conduction paths changes. In the most of the cases, in the direct



(a) Forward MOSFET current mode.

(b) Inverse MOSFET current mode.

(c) Body diode MOSFET current mode.

Figure 4.1: Three different path of the current during working modes.

conduction of the mosfet is in the forward voltage, thus the current flows from the drain to the source, see fig4.1a. When the mosfet is turned off, that means $V_{DS} < V_{GS} - V_{TH}$ and $V_{GS} < V_{TH}$, the only possible way for the current to pass through the mosfet is from the body diode an parasitic structure of the power mosfet, which can be used as a freewheeling during switching; so the current can flow just if enter from the source and go out from the drain. This case is reported in fig.4.1c. When power mosfet working in the reverse mode (reverse mode means the mosfet is kept turn on but the current has inverse direction), the load current may also flow from the source through the PN junction to the drain, as shown by the dashed line in fig.4.1b. At this time, the mosfet device works in a combination mode of forward mode and body diode mode.

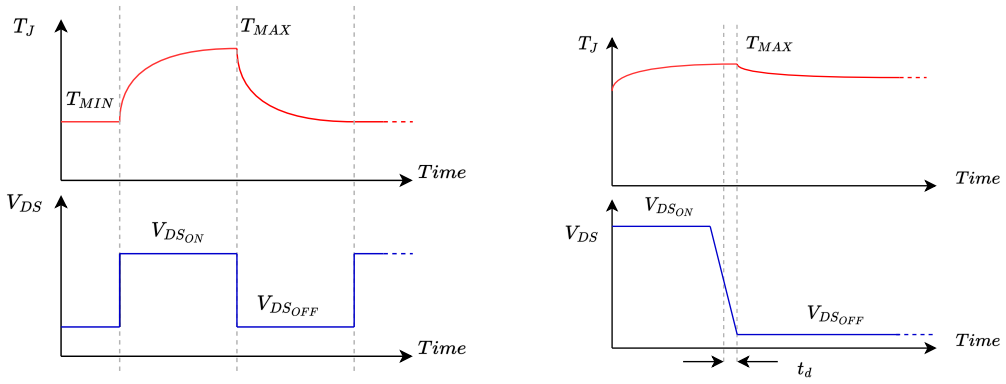
Some research as reported in [12] has observed how is difficult to find a temperature sensitive electrical parameter: TESP. An overview, about which is the best indirect way to measure the junction temperature, is needed. In the tap.4.1 are listed the possible approach to extract the junction temperature and their issues.

$R_{DS_{ON}}$ can not be the TESP for the PC, because its value has a strong depen-

Parameters	Possible issues
$R_{DS_{ON}}$	Trapping e^- in gate-channel, degradation chip metallizations, lift-off bonding wires.
V_{TH}	Trapping e^- inside the gate-channel and oxide defects
V_{SD}	Channel not completely close (a calibration is needed)

Table 4.1: Principal issues about a reliable TESP parameter.

dence with the temperature, and it is not stable, due the trapping into the gate-channel and the degradation of the metallization. Same reason can be addressed for use the threshold voltage, the trapping phenomenon is strong enough to make the V_{TH} unstable and unreliable, furthermore one of the main problem on the SiC MOSFET is the instability of the threshold voltage, so it can not be used as TESP. The last possibility is use the inner body diode that is present inside the structure of the MOSFET, one example of its is reported in fig.4.1c, but in contrary to a Si MOSFET, the SiC MOSFET gate-channel at $V_{GS} = 0\,\text{V}$ is not completely close, thus some part of the current can pass through the channel [12]; but this inconvenience can be solved applying a negative voltage to the gate to be sure that the channel is completely close; the negative value can be found extracting the calibration curve of the body diode, applying a negative voltage in the gate and forcing a small current pass through the inner diode, all of that is made during a sweep of temperature; this procedure have to be performed at different negative value of gate voltage, as long as the curve doesn't change anymore (same crossing point and slope). A good example of that can be see in [12]. The calibration curve is used also to extract the thermal coefficient of the body diode inside the SiC MOSFET, it is needed to calculate the temperature of the junction, that can be calculated starting from the V_{SD} which is sampled in very precise moments during the course of power cycling, to be precise the voltage of the body diode can be divided in two different parts, the V_{SD} *hot* and the V_{SD} *cold*, these nomenclatures are defined in this way to recall the status of the junction, or better, the temperature of its. As shown in fig.4.2a the junction has a maximum and minimum value, indicated as T_{MAX} and T_{MIN}, respectively; these two values are in correspondence with the V_{DS} (or V_{SD}) and as can be seen at the end of on-state of the MOSFET, the maximum temperature is reached and then it start to decrease. The temperature trend is exponential due the thermal impedance of the junction, that can be schematized in a equivalent RC (Resistance-Capacitance) electric model. The T_{MIN} can be any desirable value, it can be the ambient temperature or the temperature of a cooling plate set before the experiment, to have an appropriate temperature swing (as in this case study). The sampling of T_{MAX} occur when the MOSFET is entering in the off state, because here in that point the load current stops to flow, so that the maximum temperature is reached; thus using the body diode to measure the temperature, the off state



(a) Diagram of different phases of the thermal characterization.

(b) Zoom in the commutation moment for the V_{DS} and junction temperature.

Figure 4.2: Waveforms of the drain to source voltage and the junction temperature.

of the MOSFET is the only possible way to perform the measurement; the current that pass through the MOSFET is just a small current that turn on the body diode and this happens just during the $V_{DS_{OFF}}$ as said, then the voltage in the *hot* point is sampled after a way short delay time asfet that the MOSFET starts to enter in the off state.

In the fig.4.2b the following approach is clearly illustrated. The same procedure of sampling the temperature can be applied for the T_{MIN}, in this case the procedure is easier, because the MOSFET is in the off state and the body diode is still turn on, thus a very accurate timing as on the T_{MAX} is not needed, the sufficient thing is measure the voltage slightly before the MOSFET is turned on, so to be sure that the temperature of the junction has reached the minimum level. Once the two temperature have been sampled the temperature of the junction can be calculated using the formula 4.1 extracted from [5].

$$-(V_{DS}^{hot} - V_{DS}^{cold}) = k \times (T_J^{hot} - T_J^{cold}) \tag{4.1}$$

It's important to bear in mind that the figure4.2 report just ad ideal behaviour of the V_{DS} because in the real world, the drain voltage is different, it is not constant during the cooling, it has a slope and the voltage across the body diode when the junction is hot is different than the voltage when the junction is cold, otherwise the temperature measurement would not be possible.
Furthermore the PC test aims to find the life time of a component, the criterion used for assessing the end of lifetime is the increase in the forward voltage drop V_{DS} by 5% measured at load current. Once the drain to source voltage goes above this value the component is considered damaged and the test stops. [11]. The

cycling of the test has been set to have a current load on the DUTs equal to the nominal continuos current allowed by the component an it is modulated to have a $t_{ON} = 2\,\text{sec}$ and $t_{OFF} = 2\,\text{sec}$, thus a square wave current load with a duty cycle equal to $\delta = 0.5$ [19].

Schematic The circuit deigned for the developing of this project is reported in fig.4.3 and as can be see the circuit presents 6 MOSFET, 4 low power DC current source and one high power DC current source. The schematic circuit has been manufactured on a PCB board, but this aspect has precisely discussed below in the following next paragraph. First of all, can be seen that the circuit is composed

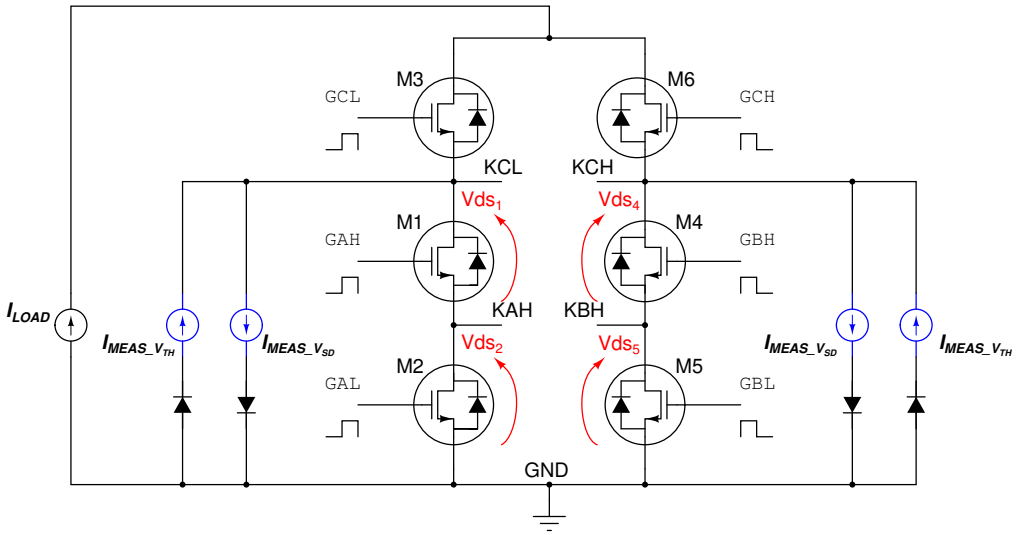


Figure 4.3: Electrical scheme of the entire measurement system adopted for the power cycling test.

by two different legs, in this case we can call them differently to distinguish them, the left leg are defined as *phase A* instead the right leg is the *phase B*. Each leg is made up of three MOSFET, for the the *phase A* the MOSFET are $M_{1,2,3}$ and for the *phase B* are $M_{4,5,6}$; the upper one is the control MOSFET, or better, is the MOSFET that is used to control the flow of the load current, its task is to open the circuit to stops the high level current in a well defined instant; the M_3 and M_6 are not DUT, they are not involved in the PC, the goal of this project is not perform PC also on M_3 and M_6, so they must have a current ranking a quite larger then the other 4 MOSFET ($M_{1,2.4,5}$), but this aspect are addressed in a more specific way later. The

DUT (device under test) in this project are, as could be guessed, $M_{1,2.4,5}$, they have a current ranking lower than the external switching ($M_{3,6}$).
The left leg and the right leg to allow a good functionality and to extract good results, have to be controlled in a very precise way; when the *phase A* turn on the *phase B* should turn off, thus they have to be controlled in phase opposition, that means the signals that controls the components are shifted by 180° from each other. This can be appreciated also in the fig. 4.3, because in the gate pins of each MOSFET are reported the control signals and in the left leg when the gate signals are low, the gate signals in the right leg are high. Since the power load of this circuit is a DC current load, care must be paid to the timing that is applied to gate signals; because the current load, that is a current generator, it needs lo have always a close circuit to works properly, thus throughout the control of the two phases particular attention has to be taken. A way to overcome this possible problem is to temporize the gate signal of each legs to have a overlapping, in fig.4.4 is reported the theoretical behaviour of the gate signals and as can be see the overlapping between the two signals are set equal to 50 µ sec, in this way the current load find always a close circuit, so that its functionality is ensured. However this waveforms are the-

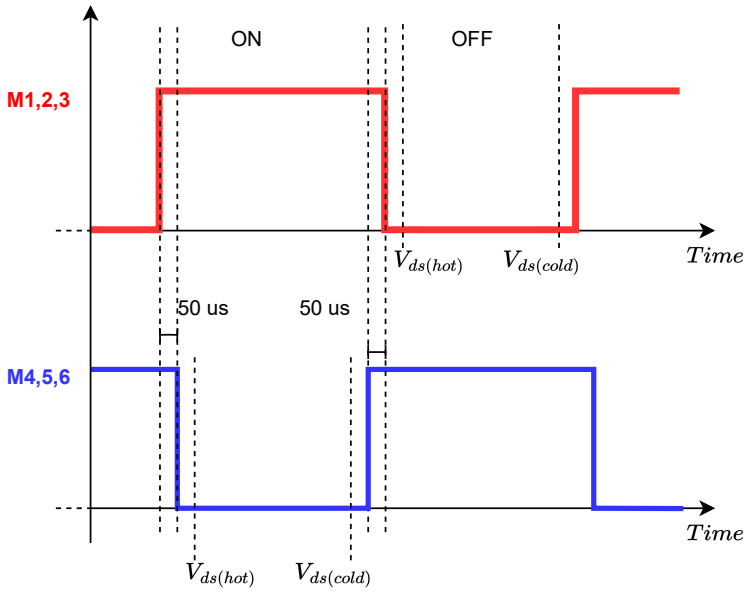


Figure 4.4: Gate signals with current overlapping.

oretical, then when the physical circuit are explained and this timing is accounted; furthermore in fig,4.4 are indicated the instant at which the V_{DS} are sampled to extrapolate the junction temperature. As reported in the graphs in fig.4.2, the junction temperature has two levels, T_{MAX} and T_{MIN}, but there's a proper moment

to measure the the V_{DS} across the body diode and it is when the load current is interrupted and through the MOSFET just flows the small inverse current, named $I_{MEAS_{V_{sd}}}$, but this aspect of the functionality is well addressed after this chapter.
As is highlighted in the schematic in fig.4.3, the value that are sampled are the V_{DS}, during the functioning the values across the drain to source are sampled by an ADC located in the main board. These sample point are fixed in the board, and them can not be changed during the functioning of the circuit; they have also an another purpose; during the measuring of the threshold voltage they don't need any change because thanks to the configuration adopted in the board, the same sample points are used to measure V_{DS} and V_{TH}, but this particular aspect are described later. Now can be just addressed the presence of the small DC current generator named $I_{MEAS_{V_{TH}}}$, it is present on the board just to be allow the measuring of the threshold voltage; however the V_{TH} can not be measured using the connections indicated in the fig. 4.3, the gate and the drain should be connected together and a small current has to be pushed into the drain, ar reported in fig.4.7, but this aspect is well addressed in the next part.
To resume the *principle of operation* of the DC-PC a short overview of the main board functionality is needed, this can be easier of interpretation looking the waveforms in fig.4.4. The two legs are controlled in a complementary way, when the *phase A* is high, the *phase B*B is low, but a short overlapping is needed to ensure a path for the current provided by the load, because the DC-PC test has as a load a constant DC power current generator that push a high level current into the DUT ("high level" is relative to the DUTc, the current has to be higher enough to stress the component, so that to rise its junction temperature). For now let's focus just to one phase: let's assume that the circuit is at steady state, when the MOSFET M_3 (M_1 and M_2 as well) turn-on the current load starts to flow also through the the phase A because before was flowing in phase B, but just for a small time interval the load current are flowing in the two legs, and this is due the overlapping introduced in the control signal. After this small interval of time in which the two legs are conducting in the same moment, the M_6 (M_4 and M_5 as well) opens so all the load current flows thought the phase A, and from this moment due to the high level of the current the junction temperature T_J of the DUTs start to rise. In the meantime, the small current generator $I_{MEAS_{V_{SD}}}$ is still working (the $I_{MEAS_{V_{TH}}}$ are used in a different situation). Once the signal gate on phase A changes from high to low, the highest junction temperature has been reached and the load current are not present anymore and the only possible current that flow through the DUT is the inverse current provided by $I_{MEAS_{V_{SD}}}$ that can exist due the presence of the body diode inside the MOSFET, and the V_{DS} is sampled (that is negative) in this instant the drain to source voltage is referred to maximum temperature of the junction. The small current is the only current that flows in the phase A during the t_{OFF} time, and at the end of this time the sampled voltage V_{DS} is referred to the minimum

junction temperature, furthermore at the end of this span the phase B is turned on and after a short overlapping time the phase A is turned off and the cycle repeats.

The flowchart that explains the experimental chain of the DC power cycling is reported in fig.4.5, the entire system is controlled by PC which enable the control and sensing program inside a FPGA (field gate programmable array), then the main is supplied by an external voltage source that gives the needed power to turn on all the components on the primary board. All the control signal signal are delivered from the FPGA to the main board and its task is transform the control signals into a consistent signals to govern the adaptor, furthermore it is important to take in mind that the main has two different tasks, one is delivers the control signal and the second one is to transform the signal extracted by the DUT and send them to the FPGA. After the main board there is the adaptor board, that its task is provide the connections to control the DUTs and the external switches, moreover it is used to sample the electrical informations coming from them. The adaptor board, since the system has been changed to works in DC mode, has a direct connection with a DC current supply, that provide the needed current to stress the DUTs. All the DUTs and the external switches are placed on a cooling plate to control the minimum operating temperature of the devices.

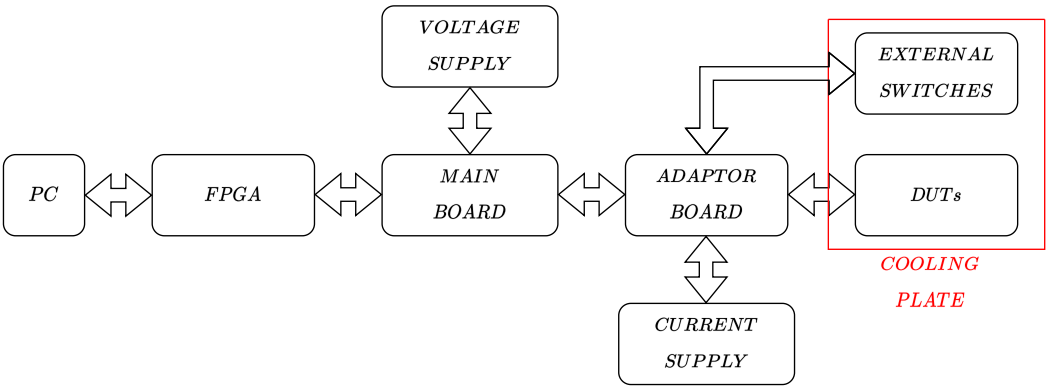


Figure 4.5: Flowchart of the entire DC power cycling system.

4.1 Measurements and parameters of interest

During this PC test the load current is always on and the DUT is in on/off control mode to generate a certain junction temperature swing. An milliampere-level current is constantly flowing through the device and is used to determine the maximum junction temperature when the high load current is removed from the DUT

by interdiction of its. The temperature of the junction is a way interesting because high temperature within the material has a degrading effect on it and this leads to premature failure of the component. In this test, and in general power cycling test, the relevant and interesting value that have to taken under control are the junction temperature T_J, the drain voltage in each component V_{DS}, the gate signal or better the applied gate voltage V_{GS} and the drain current that pass through the DUT I_D. The circuit configuration for measure the V_{DS} in the reported in fig.4.6, this circuit is the same for the phase A and B and this is the configuration during the t_{OFF} time. As reported in fig.4.2 and equation 4.1, the junction temperature is extracted from the value of the drain to source voltage. An important parameter in the SiC MOS-

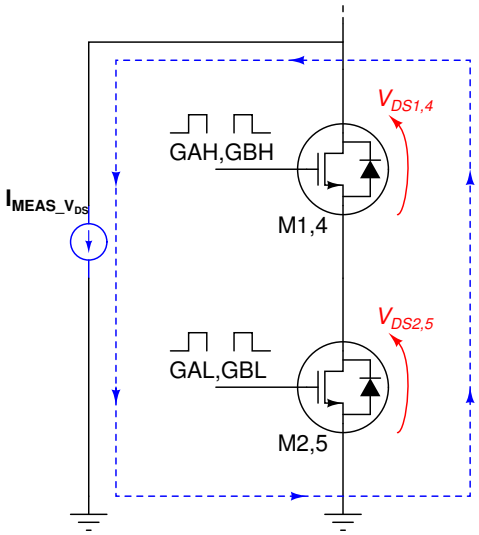


Figure 4.6: Circuit configuration for the measure of the diode forward voltage. The current direction is indicated with the blue arrows.

FET is the threshold voltage, its value is unstable due to the trapping of electrons in the channel and in the oxide, as reported in literature [15], [18], [28], [29], [23]. The circuit configuration that allows to measure the V_TH is reported in fig.4.7, as can be see the drain and the gate are at the same potential and a small DC current $I_{MEAS_{V_{TH}}}$ are pushed into the drain pins of the MOSFET, it is important to bear in mind that the following measure can be performed when the power cycling is not running, because the configuration of the circuit has to be changed and the current source has be turned on. The necessary changes to be made to the circuit are addressed in the next subsection. The configuration of the circuit has been selected to be consistent with that one used in the data-sheet by the manufacturer [26] just to be able to compare the results and also because the standard to measure the theshold voltage is well defined as can be see in [29]. Since the gate and the drain

are shorted together the sample point didn't change, thus it possible measures the V_{GS} using the same measuring setup of the V_{DS}.

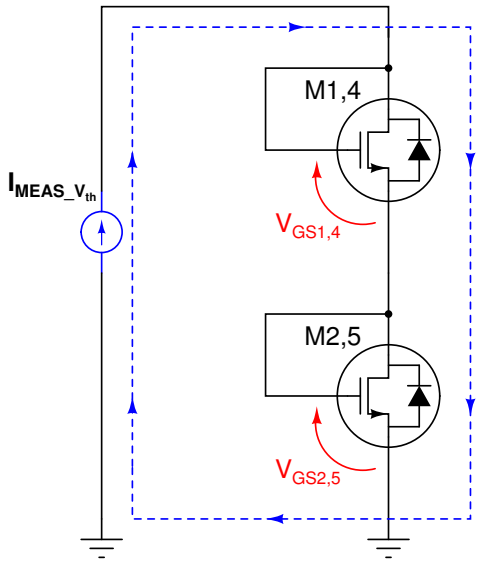


Figure 4.7: Circuit configuration for the threshold voltage measurement. The current direction is indicated with the blue arrows.

4.2 Adaptations of equipment

In the market exist a lot of DC power cycle machines, in which all the needed features are embedded inside them. For this project the commercial DC power cycling equipment has not been used due to the luck of availability, thus a solution has been found: adapt a AC power machine to work in DC mode. This choice brought some troubles in the project developing, but the main point that deserves attention is the needed to adapt the main board to work as a DC power cycling board with DUTs that use the TO247 package, to be precise the TO247 *3 pins* and TO247 *4 pins*. The main characteristics required for the adaptor are:

A Possibilities to perform DC power cycling in to different packages of TO247: TO247 *3 pins* and TO247 *4 pins*.

B Embed a DC current source in the board to measure the V_{DS}, so to use an indirect temperature measurement: the body diode inside the SiC MOSFET.

C Embed a DC current source to measure the V_{TH} during well defined moments throughout DC power cycling, to do that physical changes in the circuit was needed.

D Allows parameters of interest during the DC power cycle to be measured intelligently: measuring qualities with the lowest possible noise and highest possible accuracy.

A short explanation follows for each point addressed above:

A To overcome this particular request a new footprint has been developed, as reported in chapter 3 a 5 pins footprint is explained, in fig.3.4 it is reported. This footprint allows to install in the adaptor devices that has different TO247 packages: TO247 *3 pins* and TO247 *4 pins*.

B The DC current source to measure the V_{DS} is developed and placed in the adaptor board is reported in fig.4.8. The upper component **LT3092** is used to create the current that is needed to measure the voltage across the MOSFET during the t_{OFF} and from that, calculates the temperature, as described by the eq.4.1. The following component has been selected for its good linearity with the temperature, since the adaptor board is arranged above the cooling plate and for its output current (maximum 200 mA but minimum 300 µA). The current was set equal to 20 mA to be sure that the voltage across the was as high as possible to be measured. Furthermore the diode D2 in the left-hand side of the schematic has been positioned so that the current can only flow in one direction, as reported in fig.4.6. To allow the correct operation of the current source, a minimum voltage across its has to be ensured, for that reason a voltage equal to -12 V is applied; taking into account that the current must flow out from the DUTs and the point at which the current source is connected can arrive around 4 V. The complete circuit can be see in the appendix A in fig.A.2.

C For the DC current source used to measure the V_{TH} a dedicated chip has been used, the **LM334**, it can be see in the bottom side on fig.4.8. It was chose because it has a programmable range (from 1 µA up to 10 mA) that fits with the needed current. Changing the passive component that are connected to the LM334 the output current can be changed; in the first step the current was set equal to 10 µA but to be consistent with the data-sheet of the producer [26] it should be rose up to 1 mA. Here the diode D4 has been placed for the same reason of before, so that the current can only flow in the desired direction; in this case the current must flow in the circuit, as reported in fig.4.7. Here since the current must flow in the circuit the voltage across the regulator must be applied in a different way, now the voltage is 12 V, and as can be see in the schematic in fig.4.8 a jumper is present and trough its the desired voltage can be changed; changing the jumper position the required DC current source is activated.

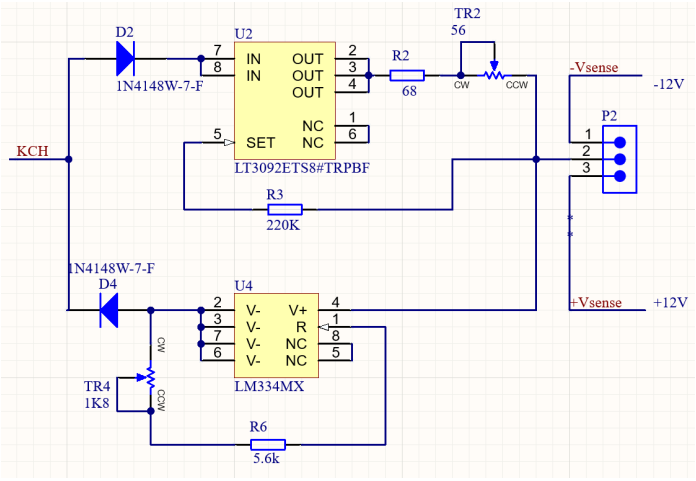


Figure 4.8: Real electric schematic configuration adopter for the current sources.

D The aspect concerning the measuring and the transport of the information of interest is quite important. Since the frequency of working for the system is not high ($t_{ON} = t_{OFF} = 2\,\text{sec}$) the problem of the stray inductance and capacitance is not largely predominant, but still the circuit rooting presents some attentions about that. Looking the fig.4.3 in which are indicated the name of the nodes of interest in the circuit, they are the upper side of the DUTs (KCH and KCL)component, the central point (KAH and KBH) and le lower side(GND); they are the sample point of the circuit. Taking in mind them and looking the fig.4.9, the same name are reported to highlight the routs reported in the image 4.3. This has been made to show which was the approach to ensure a very precise measurement mode and to minimize the stray inductance of the circuit. An anticipation of the adaptor board design is that it is composed by 4 layers, the two external layers are made to conduct the high current and the inner are used for the signals; but as can be see in fig. 4.9, the measuring routs has been developed in the two closer layer, to be precise, using the top (first) and the second layer, so that the distance between the copper routs is smaller. Then to improve the robustness against noise the routing has been carried out in this way, knowing that the left leg has at the upper side KCL, the center is KAH and the low side is GND, a good approach is to route the upper and lower side as closer as possible and them should be surrounded by the central node, this should be done for all the length od the routs and split them as close the the starting and final point as possible, so that the voltage drop is the same along the length of the tracks.

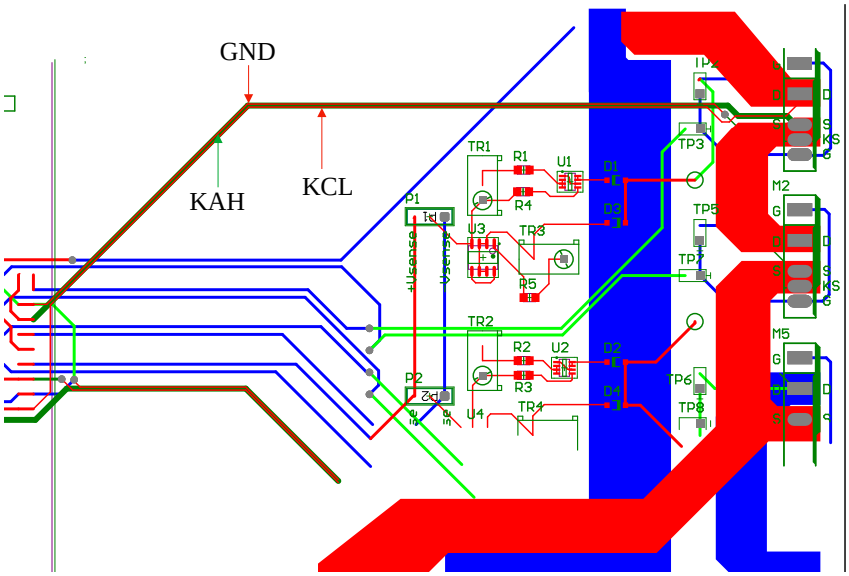


Figure 4.9: Enlargement of PCB board with tracks of interest highlighted.

4.2.1 Adaptor

The adaptor board, as reported above, should have some features that have to take into account during the developing. In fig.4.10 is reported the final version of the adaptor and to figure out better which are the interesting parts a simplified diagram is shows in fig.4.11. In the left-hand side of the board can be found the SAMTEC® connector which has been adopted to be consistent with the type connectors used in the main board, it has 40 pins dedicated for the low power connections (located in the central part of the connector) and 8 pins for the high power connections (located in the lateral part of the connector, in this case are not used). The low power pins are used for the gate signals of the gate control of the devices, for the sample connections (test points) and to supply the current source. In the central part are present the 2 symmetrical circuit: the current source; the upper one provide the current for the left leg (*phase A*) and the lower one for the right leg (*phase B*) and in the left-hand side of the both current source circuit are present 3 linear pins header connectors, that has mentioned before they are used to select which current generator has be to be used. The resistor trimmers (blue components) are used to precisely set the current value of each source, this procedure are made during the debugging of the board.
The power line in the bottom side of the figure, is the connectors used to connect

the external DC current load to the circuit, they are two large pads on which the power cable are secured trough a dedicated clips.
The external switches are in the outer parts of the board, in the top and in the bottom side; they are the M_3 and M_6 MOSFET reported in fig.4.3.
Last but not least, in the right-hand side of the board are located the DUTs, the SiC MOSFET under test; as mentioned before it has been used the 5 pins footprint developed during the case study, which it allows to connect two different packages TO247 *3 pins* and TO247 *4 pins*; the holes of its have a larger size than the normal one indicated by the manufacturer, to allow a easier change of components.
The entire board has been designed to have 4 layers:

- The two external layers, the bottom and the top layer are primary used to conduct the high power current, thus their thickness are higher than the internal ones, and they are equal to 105 µm (or expressed with quantity of copper on a surface 3 $ounces/foot^2$).
- The inner layers are primary used for the control signal, thus for the signal connections and they have thickness equal to 35 µm (or expressed with quantity of copper on a surface 1 $ounces/foot^2$).

The power paths have been made larger enough to support the high DC level current provided by the external DC current supply.

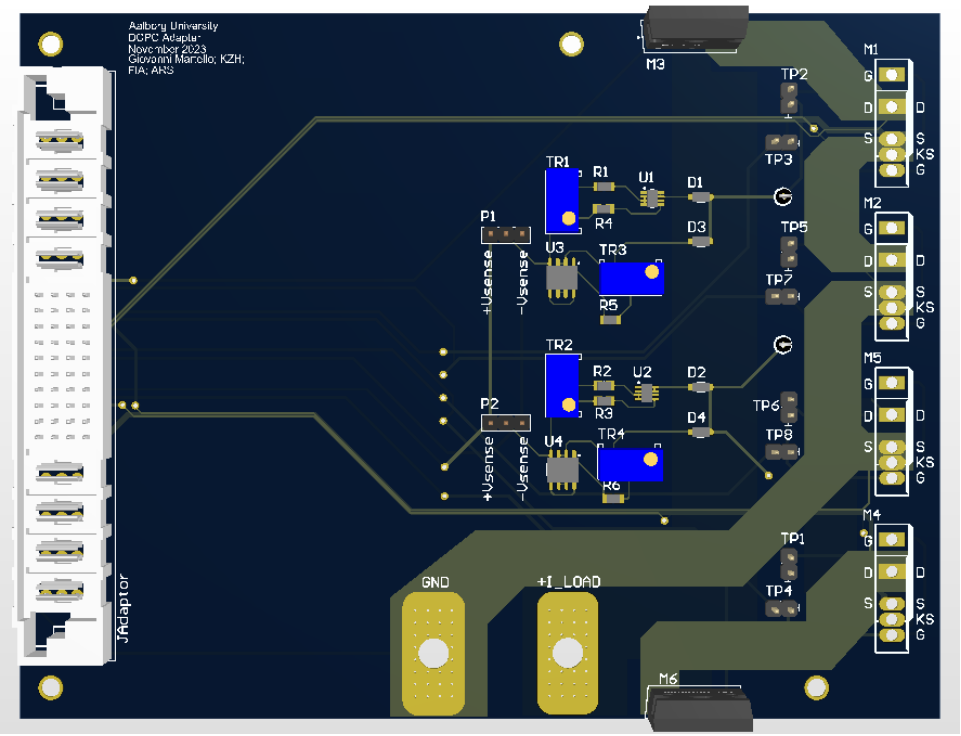


Figure 4.10: PCB adaptor board.

4.3 Results and waveforms

The first step of the project was the debugging of the board and it takes a very important place in the entire project progress. First of all, the entire number of connections has been checked using a tester, this to guarantee that all the electric tracks were made in the correct way and there were no issues and errors during the manufacturing process of the board. Then the embedded current source has been tested and some issues rose up: there was a current loop created within the current source circuit, so to solve that in each circuit just one chip has been left to isolate every possible issues; doing that the single current source works properly. Then the board has been populated with the DUTs and the external switches and mounted to the cooling plate with a sidpad to isolate the iron plate with the back of the DUTs, and connected to the main board(see fig.A.1); in this step for each legs just the current source dedicated for the V_{DS} measurements and the jumper to short-circuit drain and gate disconnected. The gate signal coming from the control and sampled by a oscilloscope are reported in fig.4.12, as can be see the gate voltage are between $-3\,\mathrm{V}$ and $12\,\mathrm{V}$ and they are correct, as expected. Then the overlapping of the gate signal has been checked to be sure that the timing was correctly set and

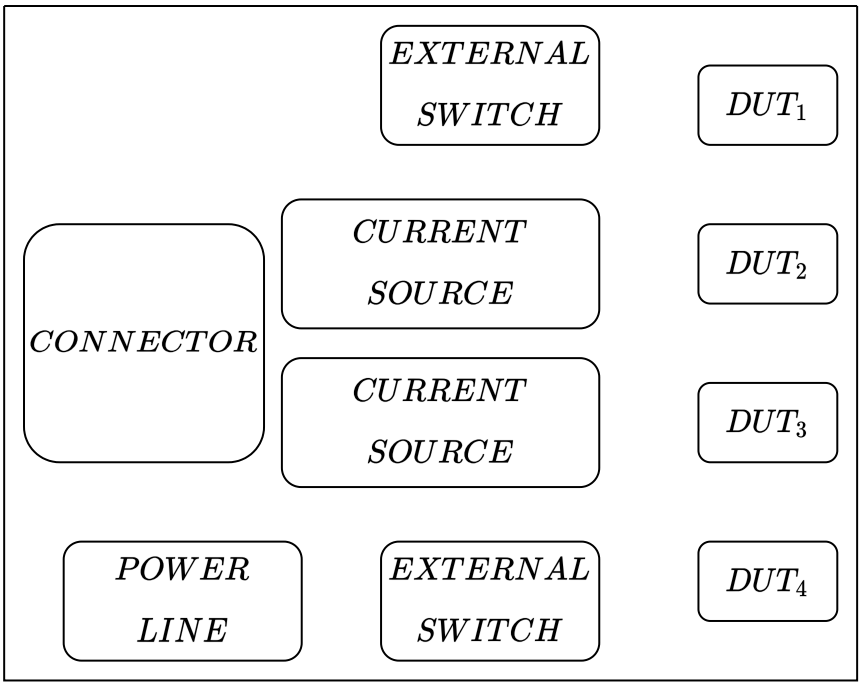


Figure 4.11: Schematic of the PCB adaptor board.

this has been reported in fig. 4.13, as can be see from the cursors it is correct and it is equal to 50 µsec. All the other parameters and the wave forms are are being developed with the debugging of the board.

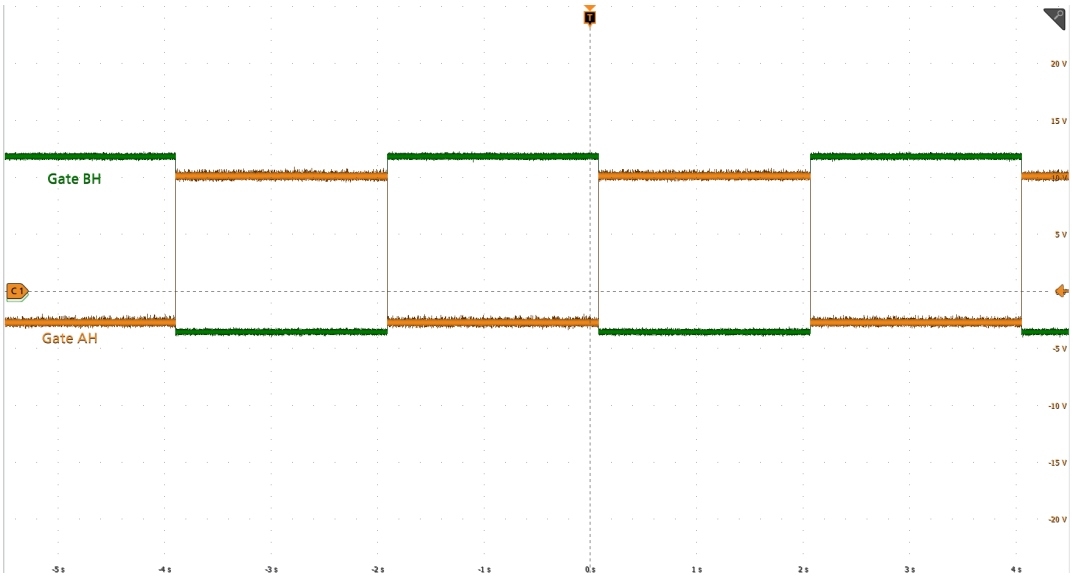


Figure 4.12: Gate signal sampled on the PCB board with an oscilloscope. The BH signal is coming from the right leg and AH from the left peg of the circuit

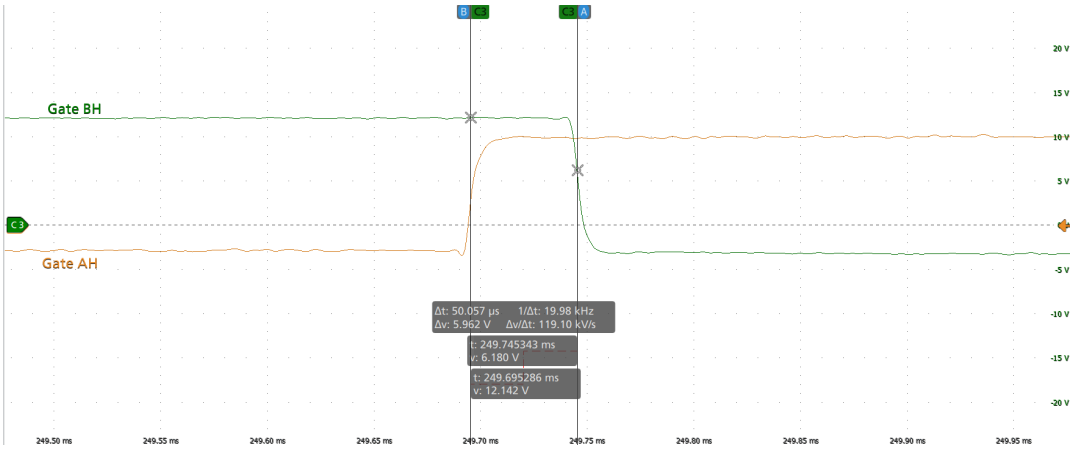


Figure 4.13: Zoom of the gate signal in which the overlapping is highlighted.

Chapter 5

Conclusions

The present project is a part of a larger project funded by ECPE, in which Aalborg University (AAU) aims to implement power cycling. The objective of this project is to try to find the lifetime of a SiC MOSFET component that has been stressed with a short circuit having energy below the critical energy E_C. It is expected that this component has no change in its parameters, but that its lifetime lies between the lifetime of a component to which no stress test has been carried out and a component which has been stressed to the point of changing parameters (i.e. damaged). The expected duration of the study is around one year, so this report shows up to the initial step of that. Furthermore, the lack of availability of the equipments brings one more difficulty in the project, to overcome the problem a AC power cycling machine has been adapted to work in DC mode. To do that, a new adapter has been developed, which allows to measure the V_{DS} during the t_{OFF} and the V_{TH} thanks to a current sources embedded in the board; furthermore, it allows to mount two different types of TO247 packaging (*TO247 3 pins* and *TO247 3 pins*). Up to now, the board is still in the debugging phase. The next step is to make the board functional, so that the DC power cycling tests can start. When the entire measurement and testing chain is ready, the ability of Aalborg University to carry out DC power cycling testing will rise, and this will make it possible to carry out more tests at the same time for a larger number of companies that required these type of test for their components.

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Appendix A

Appendix

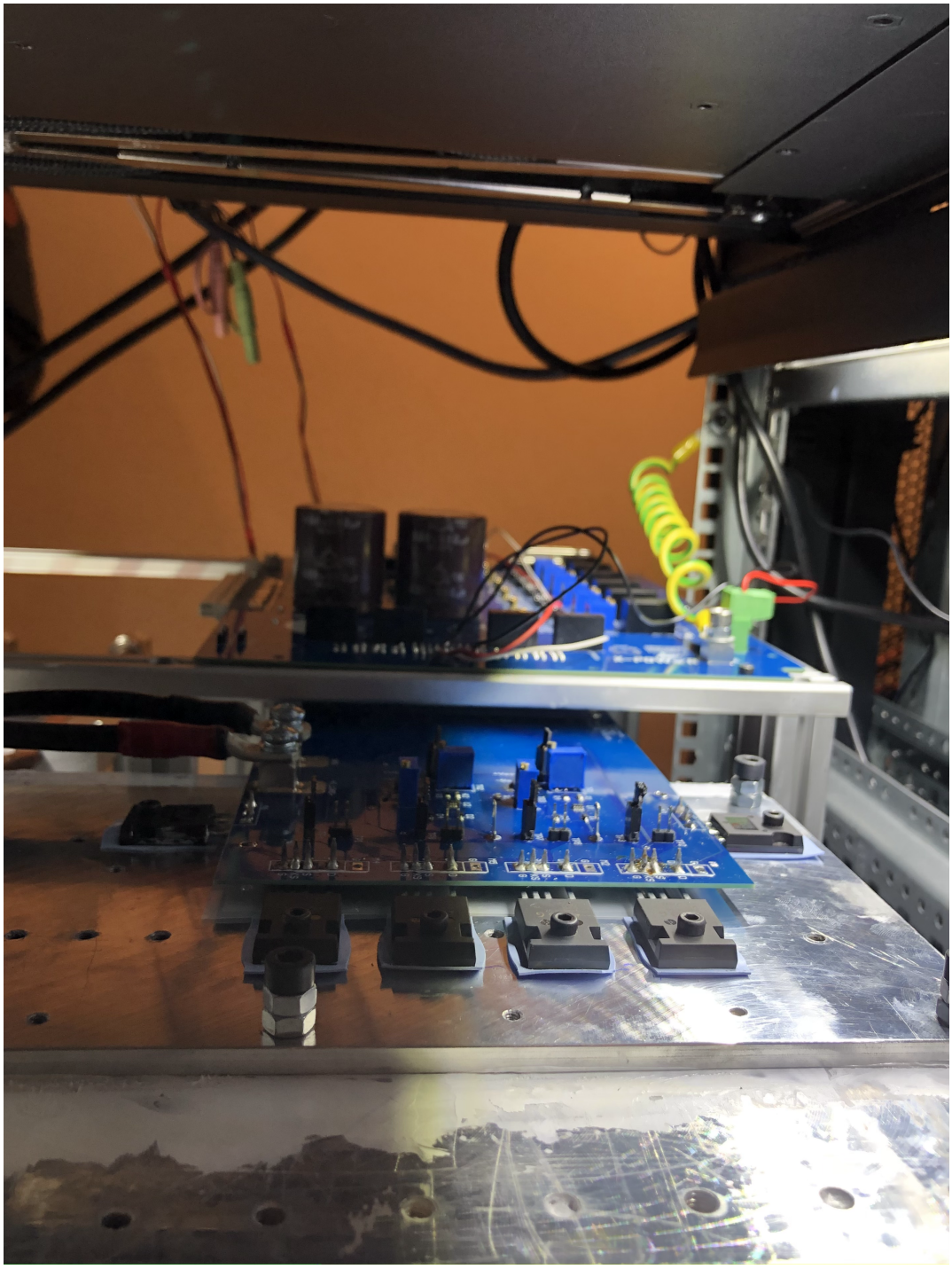

Figure A.1: Picture of the real setup.

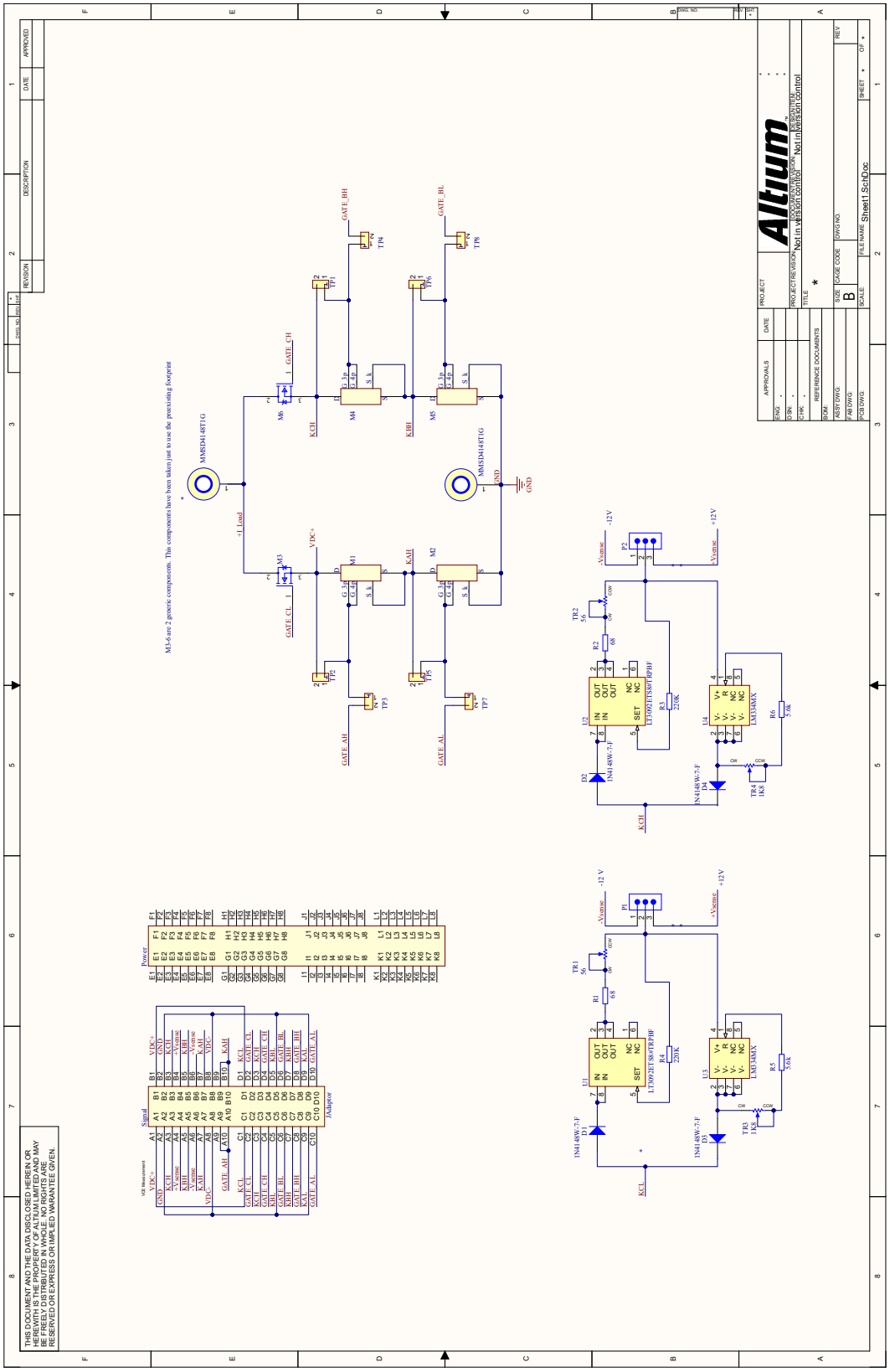

Figure A.2: Total schematic circuit of the PCB adaptor board.