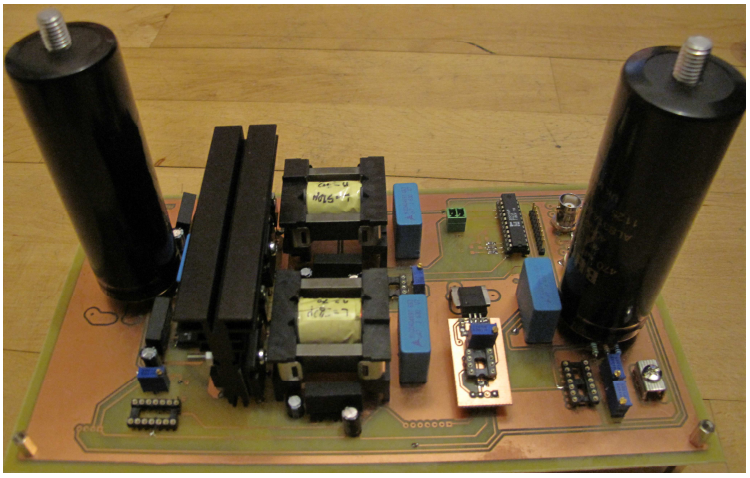
High Efficiency Residential Photovoltaic system

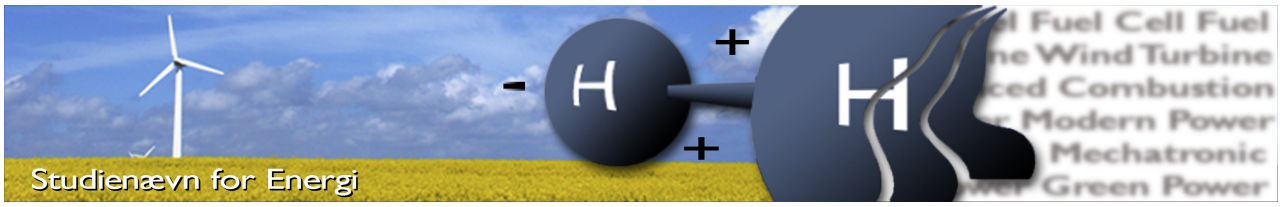


AALBORG UNIVERSITET

Master of Science in Energy Technology

10^{th} Semester, fall 2011, Group PED4-1040

Department of Energy Technology, Aalborg University



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Supervisor:	Tamas Kerekes
Co-supervisors:	Remus Teodorescu and Pedro Rodriguez
Project group:	PED4-1040

Cam Pham

Abstract:

In this report a novel high efficiency topology has been proposed, which is using low voltage switches and manage bidirectional power flow in 700V applications.
A methodology has been established to perform analytic calculations of power losses.
A thermal model in Plecs has been created to predict the losses.
As the result, the simulation confirms the analytical calculations, the worst case efficiency is 97% at 3 kW in boost mode and 98.3% in buck mode.
The converter has been designed and built. Due to time constraint the verification of high efficiency is postponed to after the report submit.

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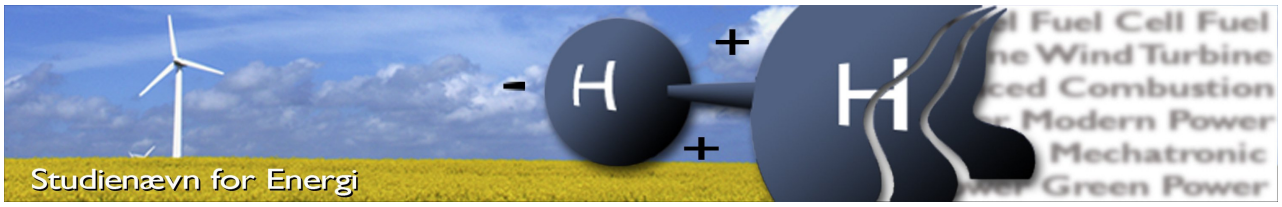

Titel:	Høj virkningsgrad solcelleanlæg til boliger
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Bi-vejleder:	Remus Teodorescu og Pedro Rodriguez
Projektgruppe:	PED4-1040

Cam Pham

SYNOPSIS:

En ny højvirkningsgrad topologi er blev foreslået i denne rapport, som kan anvende med lav spænding elektronisk kontakter og håndtere tovejs effekt flow i 700 Vs applikationer.

En metodologi er etableret til at fortage analytisk beregninger af effekttab.

En termisk model er blev fremstillet i Plecs til at forudsige tab.

Resultatet er, at simulering bekræfter de analytisk beregninger, hvor værst tænkelig virkningsgrad er 97% ved 3 kW i boost tilstand og 98.3% i buck tilstand.

Omformer er blev designet og bygget. På grund af tidsbegræsning, verifikation af højvirkningsgrad er udskudt til efter rapport aflevering.

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Preface

The project report on a dual phases bidirectional DC-DC converter. It has been written by group PED4-1040 at the Department of Energy Technology at Aalborg University. It was conducted during the 1^{st} of September to 1^{st} of Febuary 2012.

The target groups of this report are the fellow student in the department and for those who has the intrested in power electronic.

Literature references are given in [] and they can be found in bibliography at the end of this report, e.g. [1] is the number one in the reference list. Equations are numbered in format (x.y) and figures are numbered in format Figure x.y, where x is the chapter number and y is the number of the item.

The enclosed CD-ROM contains the project written in Adobe PDF format and the simulation files. All the simulations used in this project were performed in MATLAB/SIMULINK 32-bit.

I would like to thanks my supervisors Tamas Kerekes, Remus Teodorescu and Pedro Rodriguez for the contructive comments an idea. A special thank to Cristian Nicolae from the 9^{th} semester who has helped me when I need most. At last, thanks to my wife Nga thi Thuy Nguyen, my daugther Lyly Cam Tien Pham and my son Isaac An Pham for being a part of me. Thuong 2 con va em nhieu. Cam Pham.

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Chapter 1

Introduction

1.1 Background

To slow down the climate change and reduce the carbondioxide emmision caused by human activity, worldwide goverments work on a common goal - to reduce carbondioxide emmision.

The goal of the Danish energy policy in year 2020 for power system is; 50 percents of power production is to be generated from renewable sources, mainly from wind power. The ambition is to become independent of fossil fuels in the year 2050 [1]. To overcome challenges like; fluctuating production from wind power and the extra load from Electric vehicles (EVs) in the future, huge imbalancing of generation and demand etc., worldwide researchers believe that Smart Grids can be the solution. The infrastructure of a Smart Grid can be seen in Figure 1.1. It can be seen, besides the primary substainable generations and storages, the end users have also similiar facilities, all connected in a network.

Figure 1.1: The infrastructure of a Smart Grid, where generations and loads are connected in a network, that operates in parallel with utility grid [1].

Among different renewable energy sources that can be connected to the grid, one which is expanding fast worldwide is the Photovotaic (PV) technology [6]. PV panels are discrete and often installed at place like rooftop, some are also a part of modern architecture. Statisticly, the price of PV modules has been reduced by half for every seven years since 1980s [7]. To increase the interest of PV in Denmark, the incentive at the moment for the residential installation up to 6 kW is; to store the energy in the grid, this means for every kWh to the grid can be used again within a year[citation: ens.dk] for free, this is a saving of a little bit more than 2 kr/kWh. This incentive is not permanent, but the storage concept can also be realized with batteries. This smart PV solution with storage is called Smart PV for the rest of the report and in the next subchapter will introduced why Smart PV is economically attractive.

1.1.1 Smart PV

The main goal of a Smart PV is to promote the use of a classical grid connected PV. In this way the importances of the inverter are moved from a simple power conversion unit into an essential component of grid infrastructure.
Beside the functionalities of grid connected PV, further can be achieved: reactive power compensation, energy storage and smart grid interaction[8]. Through communication with the distribution system operator (DSO), the smart PV inverters can ease the grid imbalances.
According to IMS Research (see Figure 1.2), Smart PV inverters will take over in 2014 and grow from 20% of the market in 2010 up to almost 60% in 2015 (27GW).

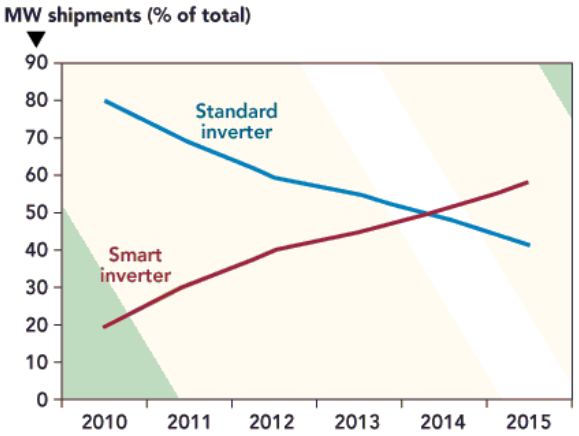


Figure 1.2: The world market for standard and smart inverters[2]

To highlight the benefits of Smart PV, the following case study is based on PV generation from the $1.8\ kW$ system in Green Power Lab at AAU, the shown case is from July 2008. More detailed analysis can also be found in [9]. From the economic point of view, it is more fair to analyze in the case of Spot price; where energy is payed hourly, electricity tranding is available and storing energy

"in the grid" is no longer valid.

1.1.1.1 Electricity price

For a household with a consumption of $4000\ kWh$ per year, the average unit price of electricity is $1.98\ Kr./kWh$. This is included tariffs, subscription ect. and is distributed as shown in the pie chart below.

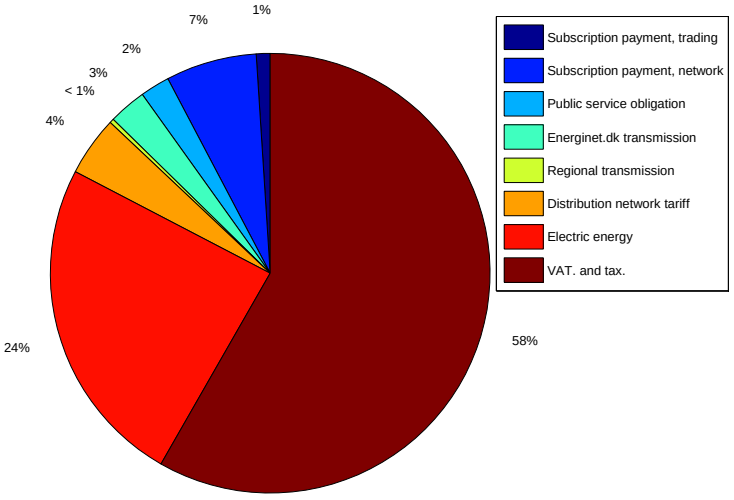


Figure 1.3: The sharing of unit price for private consumer with 4000 kWh per year[3].

It can be seen that the average Spot price of electric energy is only a quater of the totalt price, by in house generation of the consumed electricity the dominate part of electricity can be cut away and only few small subscription fees plus their tax. remain.
Electricity price dependeds on generation and demand. Due to the consumption pattern and the fluctuation in mostly wind power, Spot price is different from hour to hour but has a 24-hours cycle as consumption, based on the estimation of the two mentioned, the price is given 24 hours ahead. Figure 1.4 shows the plot of 24-hours average Spot price of electricity in July. The average Spot price during the day is $0.492\ Kr./kWh$ and swings more than double from $0.266\ Kr./kWh$ at $4AM$ till $0.664\ Kr./kWh$ at $11\ AM$.

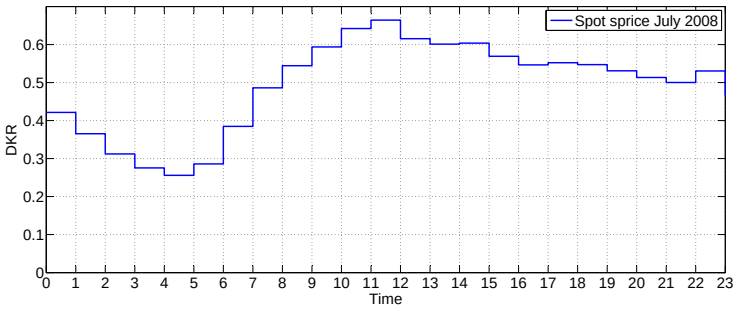


Figure 1.4: 24-hours average of electricity energy Spot price in July.

1.1.1.2 Residential consumption and PV generation

The 24-hours average electricity energy consumption of a resisdential house in DK for July was $25.65\ kWh$ and is distributed as plotted in Figure 1.5 with the green solid line. The minimun consumption was $0.45\ kWh$ and was between 2 and 3 AM. The maximun was $1.73\ kWh$ and was between 9 and 10 AM. Based on the mentioned unit price, this cost $51.79\ Kr$ per day.

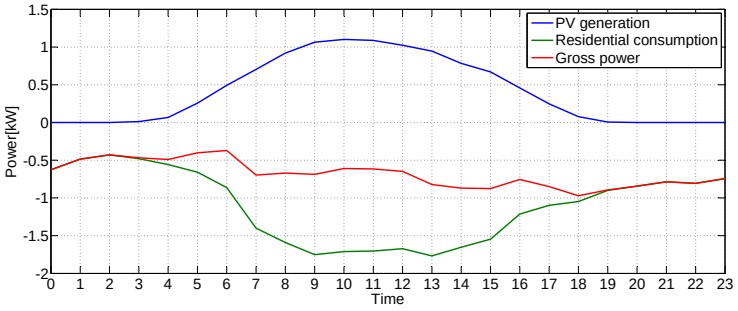


Figure 1.5: 24-hours average of electricity energy consumption and PV generation in July.

Based on the data from the $1.8\ kW$ PV setup from the Green Power lab, a 24-hours average power generation in July is plotted in Figure 1.5 with blue solid line. The average sunny hour in July was 9 hours and due to different in irradiance and temperature the average of peak energy generation from a $1.8\ kW$ PV setup was only $1.1\ kWh$ and was between 11 and 12 AM. The total production was $9.92\ kWh$ per day. PV generation has the advantage, that the distribution of generation pattern is to a certain degree similiar to the consumption pattern. The solid red line in Figure 1.5 show the difference between generation and demand, where gross power is more steady, which confirms this correlation.

From the gross power plot in Figure 1.5, it is obvious that $1.8\ kW$ PV system is too small for residental households, but what if the setup is doubled to $3.6\ kW$ PV installation?
Figure 1.6 show the power curve for this scenario, where PV generation has been scaled by a factor of two.

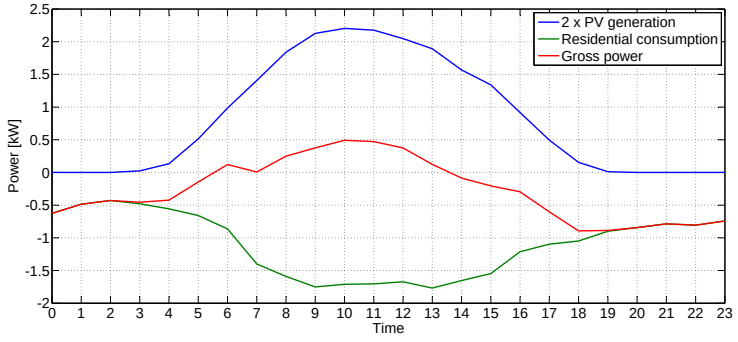


Figure 1.6: 24-hours average of electricity energy consumption and doubled PV generation scenario.

From the macroscopic/day scale the imbalance between generation and demand is minus 5.81

kWh, but on microscopic/hour scale, the power imbalance was piecewise positive and was 1.99 kWh, which means more generation than demand. This gives two possiblities, either sell it to Spot price or store the surplus energy.

Although Spot price during these positive imbalance hours is more than the average; 0.492 $Kr./kWh$ (see Figure 1.4), but the revenue from selling this surplus energy is not enough to cover the cost of buying 1 kWh from the grid.
Having a storage does give rise to additional cost, but it does also gives the opportunity to trading with the electricity energy. Electric energy can be bought when the price is lowest and sold when it is highest, according to Spot price in Figure 1.4, this gives almost 250% in profit, which can reduce payback time. Processing the energy through a high efficiency converter is very important, because this affects the profit directly.

1.1.1.3 Smart PV configuration

A potential residential PV installation with battery storage in the future could be like shown in Figure 1.7, where storage is used to store surplus energy from PV panels or trading energy based on the price information from Nordpool.

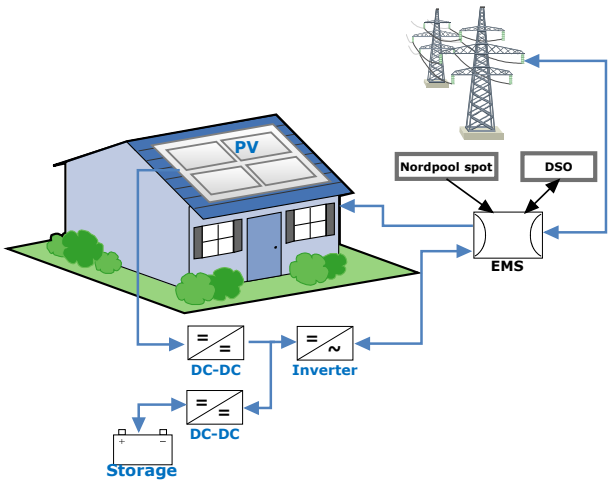


Figure 1.7: A potential PV installation with battery storage for Smart Grid solution with energy management system.

Due to the difference in voltage level of PV panels and the battery bank, each are shown with its own converter, in practice those can be of similiar topology. An inverter will be used to switch the common DC link voltage to grid voltage, an Energy Management System (EMS) will communicate with the Smart Grid and enable an economic and secure electricity supply.

1.2 Problem formulation

To maximize the economic benefit and reduce the payback time of the system, a energy efficient system is required. Based on that the problem is formulated as:

Design a high efficiency bidirectional DC-DC converter for battery storage

The requirements for this converter are:

- 3 kW.
- Common DC link voltage is 700V for grid connected.
- Target efficiency ¿ 95 at nominal power%.
- Criteria for the battery is based on Saft Synerion 48 E lithium-ion module, see more in Table 1.1

Table 1.1: Eletrical parameters of Saft Synerion 48 E[5].

Parameter	Value	Note
Voltage [V]	48	Norminal
Energy [Wh]	2200	
Voltage window [V]	42 to 56	
Discharge current [A]	40	Nominal
Charge current [A]	14	Norminal
Peak power [W]	1440	30 sec. at 20 ° C

1.3 Project limitations

Designing a converter is an iterative process and since the focus is to demonstrate a bidirectional DC-DC converter with high efficiency, the first task is to analyze the power losses during power processing. Based on that the topology which is most suited to fulfill the target efficiency will be designed.
Due to time and resouces contraints, some further limitations are needed, those are:

- Switching with high frequency to reduce size of magnetic components.

- Operate in continuous-current conduction mode to reduce the losses.
- Minimum power output is 300 W.
- Using of eigth battery modules to reduces the convertion ratio and losses.
- Charging control of the battery bank is not addressed.
- The test will be carried out in the lab with a power supply and programmmable load.

The milestones of the project are listed below:

- Acquire knowlegde of high efficiency converter.
- Analyze losses.
- Design and build a bidirectional DC-DC converter with high efficiency ($> 95\%$).
- Implement the control in the DSP TMS320F28335.

1.4 Report outline

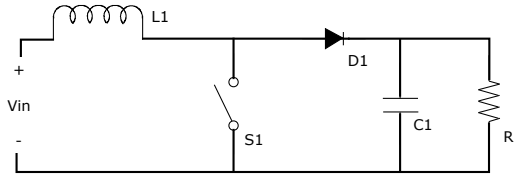
Until now, the motivation has been mentioned. The problem formulation is formulated and the limitation is presented.
In Chapter 2, a novel high efficiency bidirectional converter topology, which is using low voltage switches in 700 V applications, is presented.
In Chapter 3, results from the thermal modeling in Plecs are presented.
In Chapter 4, the design and build of the converter.
Chapter 5 concludes the work which has been done.
Appendix provide the necessary materials for understanding the decision and realisation, which have been moved to have the flow in the report

Chapter 2

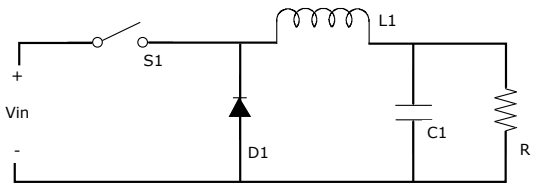
Bi-directional DC-DC converters for batteries

DC-DC converters are used to convert the unregulated DC input into a controlled DC output at a desired voltage level. They are also referred as DC-choppers and can be considered as a DC equivalent to an AC transformer with a continuously variable turn ratio. Like a transformer, it can be used to step-down or step-up a DC voltage. Two converters can be recognized as the basic converter topologies, namely; the boost converter and the buck converter[10].

Charger and discharger the energy to/from the batteries requires a converter with bidirectional power flow. A simple boost is shown in Figure 2.1(a) and the buck topology in Figure 2.1(b) support only unidirectional power flow, this is due to the diode in the boost topology and the potential different between input and output in the buck.



(a) The classical boost converter.



(b) The classical buck converter.

Figure 2.1: The boost and the buck converter.

Bidirectional power flow can obtain by back-to-back connected two unidirectional converters. From Figure 2.1 each converter can be indentified to have an inductor ($L1$), a controlled switch ($S1$), a diode ($D1$), a filter capacitor ($C1$) and a load (R). Thus some components can be utilised for both topologies, if back-to-back connected is realised.

In Figure 2.2, a capacitor ($C1$) is added to filter/stabilise the input voltage and the diode ($D1$) is replaced with the MOSFET ($S2$), where the intrinsic body diode is oriented in the same direction as the rectify diode. See the circuit from left to right, this is a boost converter, where the body diode of the MOSFET ($S2$) is replaced the rectify diode ($D1$). Because of the MOSFET ($S2$), this boost converter is able to perform active rectification; by turn on this MOSFET. This can reduce the losses during rectify period, which is not possible with a simple boost converter as shown in Figure 2.1(a).

Swap around the source and the load from Figure 2.2 and see the circuit from right to left, this is indeed a buck converter; where $C2$ is now the input filter capacitor, the freewheeling diode ($D1$) is replaced with the intrinsic body diode of the MOSFET ($S1$), $L1$ and $C1$ form a low pass filter. By replade freewheeling diode with a MOSFET, this converter can perform active freewheeling and thus reduce the losses during freewheeling period.

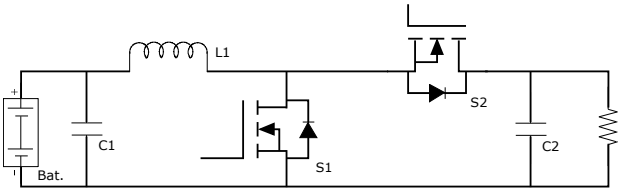


Figure 2.2: The proposed bidirectional DC-DC converter for batteries.

Table 2.1 sums up the properties of the mentioned converters.

Table 2.1: Properties of the converters.

	Power flow	Conversion	Number of components	Active rectifify	Active freewheeling
Boost	Unidirectional	Step up	4	No	No
Buck	Unidirectional	Step down	4	No	No
Proposed	Bidirectional	Step up/down	5	Yes	Yes

Beside the differences of properties highlighted in Table 2.1, the proposed converter is the same as the basic boost and the buck under respected mode. Thus the transfer ratio for the boost converter under continuous-current conduction mode (CCM) is still valid and is as expressed in Equation 2.1 and as Equation 2.2 for the buck converter, where D is the percentage of on-time also known as duty cycle.

$$V_{out_{boost}} = \frac{V_{in}}{1-D} \qquad [V] \tag{2.1}$$

$$V_{out_{buck}} = V_{in} \cdot D \qquad [V] \tag{2.2}$$

By CCM means, the inductor current never reach zero, this is sketched for a boost converter in Figure 2.3 with arbitrary values.

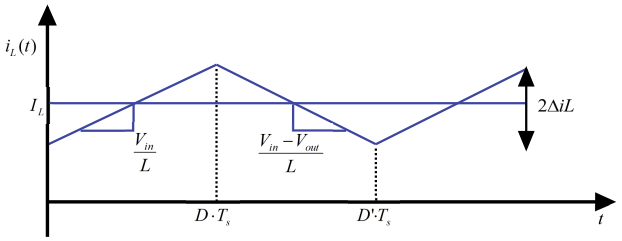


Figure 2.3: Waveform of the inductor current over a switching cycle (T_s.

In order to maintain to operate in CCM, the inductor value can be deduced from Figure 2.3 to be:

$$L_{boost} = \frac{V_{in}}{2 \cdot \Delta iL} \cdot T_s \qquad [H] \tag{2.3}$$

Similiar can be done for the buck converter or find in litterature(s)[11] to be:

$$L_{buck} = \frac{V_{in} - V_{out}}{2 \cdot \Delta iL} \cdot T_s \qquad [H] \tag{2.4}$$

It is desired to keep the current ripple small and thus operate in CCM, because the peak current is not differ to much from the average, thus reduce the rated current of the inductor and semiconductors. This can reduce the size, cost and efficiency.

2.1 Dual phases bidirectional split converter

The idea of merger the boost and the buck; boost-buck converter, to obtain bidirectional converter for charge and dicharge the batteries has been introduced in the previous section. Based on this merged converter, this section justify the design of a converter, which can fullfil the target efficiency best, thus this converter design will be modelled and build to validate the high efficiency.
To have high efficiency is by means reduce the losses, this tool is introduced in Appendix A.

2.1.1 Select of semiconductors

To have low losses, based on the analysing in Appendix A, a MOSFET with low Drain-Source on-resistance ($R_{DS_{on}}$) is needed to reduce the conduction loss, at the same time this MOSFET must

have low input capacitance to reduce the switching loss.

The DC link voltage is $700V$ and a safety margin should be added for the require MOSFET. Compound of silicon and carbon have give a material (SiC; silicon carbide) which has pushed the limit of blocking voltage and other advantages to semiconductors. SiC MOSFETs at $1200V$ is commercial avaiable, which can be used to realise the boost-buck converter, but the price is extremely high.

Alternative is using Super junction CoolMOS^{TM}. The arguments when CoolMOS is presented are: The on-resistance of MOSFETs are normally increased with higher blocking voltage, but in Super junction CoolMOS devices this "silicon limit" is overcome, where the square-law dependency between blocking voltage and on-resistance is amended and a very low $R_{DS_{on}} \cdot Q_g$ gives low conduction, driving and switching losses [12]. .

CoolMOS C3 series is avaiable up to $900V$, but the switching charateristics are not suited for fast switching. Furthermore they are only tested to 600V, which cannot guarantee anything at $700V$.

One way to overcome this challenge is by split the $700V$ DC link into two parts; one for $+350V$ the other for $-350V$ and use $600V/650V$ devices as shown in Figure 2.4.

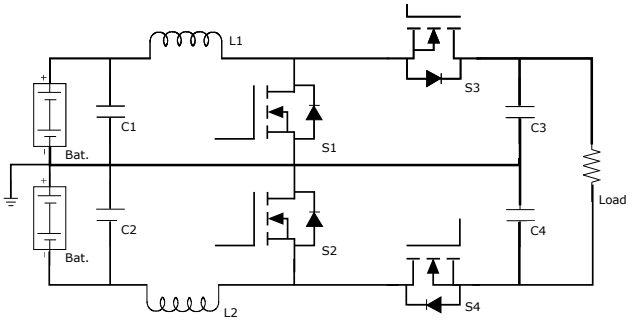


Figure 2.4: The bidirectional split converter(BSC), where lower blocking voltage switches are utilised.

The split converter has an internal common reference, but the DC link voltage will be the connect between $+350V$ and $-350V$, thus $700V$ can be obtained.
Super junction CoolMOS^{TM} below $700V$ ($650V$) exist in larger number, one of the most attractive series is the latest generation, CFD2; where the fast body diode is integrated. The advantage of choosing a integrated fast body diode is not only reduce the switching loss, but also enable active rectify and freewheeling, which can increase the efficiency as mentioned in the beginning of the chapter.

Due to problem with purchase of IPx65R110CFD[13] and other CDF2 devices, which are not avaiable at RS components or Farnell or Mouser or Digikey. The selected device is from an earlier generation; CP series. IPW60R099CP [4], which has similiar specifications, except the built-in fast body diode.

To eliminate the drawback from the slow body diode in the selected device, a SiC schottky diode (SCS120AG)[14] is added in serie with MOSFET to block the body diode and another SiC schottky barrier diode is connected in parallel with the MOSFET and blocking diode, to takeover the functionality of the body diode. The connection of this modification of the CP device can be seen in

Figure 2.5.

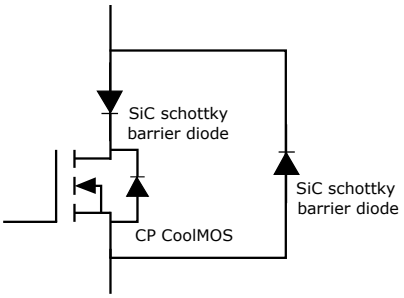


Figure 2.5: Modification of CP device with two SiC diodes to block the slow body diode and improve the switching charateristics.

SiC diodes is well known for theirs extremely fast reverse recovery time due to extremely low recovery charge and this extends the switching frequency limit of hard switching. The limitation of this modification as shown in Figure 2.5 is; this cannot perform active rectify/freewheeling due to the block diode. Furthermore should be mentioned, that add-on with SiC diodes will increase the total price of components, but the modification is an engineering necessity to fulfill the target efficiency and overcome the problem with purchase of CFD2 devices.
To summarise the devices which are mentioned above, some of the most importance characteristics behind the decision of the switch are shown in Table 2.2. The table is shown for the modified IPW60R099CP, instead of the IPW60R099CP. Some of the values can be read out directly from the datasheets while others have to be computed as the case of the modified CP. Be to fair, the devices have approximate the same current capability.

Table 2.2: Comparision of parameters between 1200 V SiC MOSFET with IPW65R110CFD and the modified CP device.

Characteristic	CMF10120D[15]	IPW65R110CFD (IPW60R099CP + SCS120AG)	Modified	Note
V_{DS}	$1200V$	$650V$	$600V$	
$R_{DS_{on}}$	220 $m\Omega$ @ $I_D = 10A$	110 $m\Omega$ @ $I_D = 12.7A$	110 $m\Omega$ @ $I_D = 18A$	Max. @ $T_j = 25°C$
Q_g	$47nC$ @ $V_{DD} = 800V$, $I_D = 10A$	$118nC$ @ $V_{DD} = 480V$, $I_D = 19.1A$	$60nC$ @ $V_{DD} = 400C$, $I_D = 19A$	Typ. @ $V_{GS} = 10V$
C_{iss}	$1000pF$	$3240pF$	$2800pF$	$V_{DD} = 175V$
C_{oss}	$100pF$	$90pF$	$130pF + 110pF = 240pF$	$V_{DD} = 175V$
C_{rss}	$10pF$	$10pF$	$2.2pF$	$V_{DD} = 175V$
V_F	$3.5V$ @ $I_F = 5A$	$0.9V$ @ $I_F = 19.1A$	$1.5V$ @ $I_F = 20A$	Typ. @ $T_j = 25°C$
t_{rr}	$138ns$ @ $I_F = 10A$, $\frac{diF}{dt} = 100A/\mu s$	$150ns$ @ $I_F = 19.1A$, $\frac{diF}{dt} = 100A/\mu s$	$19ns$ @ $I_F = 20A$, $\frac{diF}{dt} = 380A/\mu s$	Typ. @ $V_R = 400V$
Q_{rr}	$94nC$ @ $I_F = 10A$, $\frac{diF}{dt} = 100A/\mu s$	$800nC$ @ $I_F = 19.1A$, $\frac{diF}{dt} = 100A/\mu s$	$35nC$ @ $I_F = 20A$, $\frac{diF}{dt} = 380A/\mu s$	Typ. @ $V_R = 400V$

The characteristics in Table 2.2 are important regarding to power losses performance, which are detailed in Appendix A.

2.1.2 Boost and filter inductor

Inductor design is very challenges, beside obtain the require inductance, it all started with select the proper core, choose the operation point so the maximum flux density must not saturate the core, limit the ac flux density so the core losses is acceptable, choose the right wire so winding losses is acceptable low and so on. Those design steps can be seen in Appendix B.

Design inductor with high saturation flux density core material reduces the airgab, number of turns and the physical core size. Reduce the number of turns will decrease winding losses, which is an important factor of this converter. Due to problem with purchase high saturation flux density core, as consequence a Ferrite core is used. The used ETD39 N87 core from Epcos is saturated around $0.4T$ at $25°C$, where Kool Mu goes to around $1.5T$. As the consequence, the stored energy is divided into two and realise the BSC with two interleaved boost-buck. To reduce the winding loss, the inductance is reduce to a half ($800uH$) and the frequency is doubled ($200kHz$).

Based on the equations (in theory) in Appendix B a $1.6mH$ inductor can still be obtained on the same core, by double the number of turns and increase the four double the airgab to almost $6mm$. Whenever the ETD39 core can handle for power density in practice is another question and $6mm$ airgab is quite large (which contribute to EMI problems).
To reduce the influence of $200kHz$ switching on losses, litz wire with $2/3$ of skin depth is used.

2.1.3 Interleaved dual phases bidirection split converter

In total this interleaved dual phases bidirectional split converter (IDPBSC) has four inductors; two in $+350V$ and two in $-350V$ as shown in Figure 2.6.

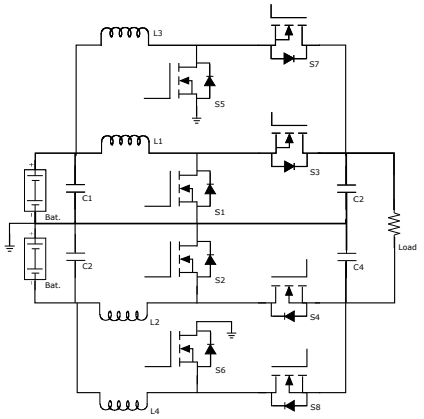


Figure 2.6: Interleaved dual phases bidirectional split interleaved converter (IDPBSC).

As the advantage compare to BSC the current in IDPBSC is reduced by a factor of two, but switching frequency, number of semiconductors and inductors are doubled.

The question is, which converter fulfill the target efficiency best?

To answer this question, based on the analytic calculation (from Appendix A) losses is calculated for the boost mode, where $V_{in} = 168V$ and the duty cycle $D = 0.52$. Table 2.3 presents the power losses from the Boost-buck, BSC and IDPBSC. As a comment to the table, active rectify is not addressed, because the BSC and IDPBSC is calculated with the modified CP, where this function is not possible. Furthermore series resistance in the boost inductor in case of Boost-buck and BSC is assumed to be the double (because double inductance compare to IDPBSC). The MATHCAD file used to generate the table can find in the attached CD.

Table 2.3: Power losses in Boost-buck, BSC and IDPBSC.

Converter type	P_{losses} MOSFET	P_{losses} Diode	P_{losses} Inductor	P_{losses} Total	Efficiency
Boost-Buck with CMF10120D	$35W$	$19.2W$	$47.5W$	$101.6W$	96.613%
BSC with modified CP	$2 \cdot 19.3W$	$2 \cdot 3.8W$	$2 \cdot 47.5W$	$141.1W$	95.297%
IDPBSC with modified CP	$4 \cdot 13.6W$	$8 \cdot 2.4W$	$4 \cdot 5.94$	$97.4W$	96.766%

From Figure 2.3 it can be seen, that the power losses in IDPBSC is lowest ($97.4W$), next is the Boost-buck which differ 4 W and last the BSC with $141W$. It should be mentioned, that the power losses in the inductor for the case of Boost-buck and BSC, is under the assumption of the same core can be used, but the airgab is $6mm$ and can caused serious electromagnetic interference. All the converters above fulfill the efficiency target, but the IDPBSC show the best result. Based on the mentioned comments, the IDPBSC will be modelled and build to verify the target efficiency.

Chapter 3

Thermal modelling with PLECS

In the previous chapter the analytic calculation has shown, that the IDPBSC has the highest efficiency. In this chapter the IDPBSC is modelled in boost and buck mode with lowest input voltage; $\pm 168V$ and highest input voltage; $\pm 224V$, where the load varies discrete from $300W$ to $3000W$ and the efficiency at the egde of operation point will be recorded.

Based on the datasheets of the semiconductors and the application note[16] the loosses look up tables for PLECs are constructed. For correction the reverse recovery energy is substracted from the turn-on energy loss of the MOSFET, because the body diode of the MOSFET is blocked by the blocking diode. This energy is calculated as:

$$E_{Qrr} = \frac{1}{4} \cdot Q_{rr} \cdot V_{rr} \qquad [J] \tag{3.1}$$

The reverse recovery charge can be read out from the datasheet.

3.1 Modelling of the boost part of the converter

In Figure 3.1 a screen is shown the modelled converter in boost mode. A thermal heat sink is overlap the semiconductor devices and by using Plecs probe, conduction and switching losses can be read out. By using the provided losses averaging model from my supervisor, the power losses can be read out.

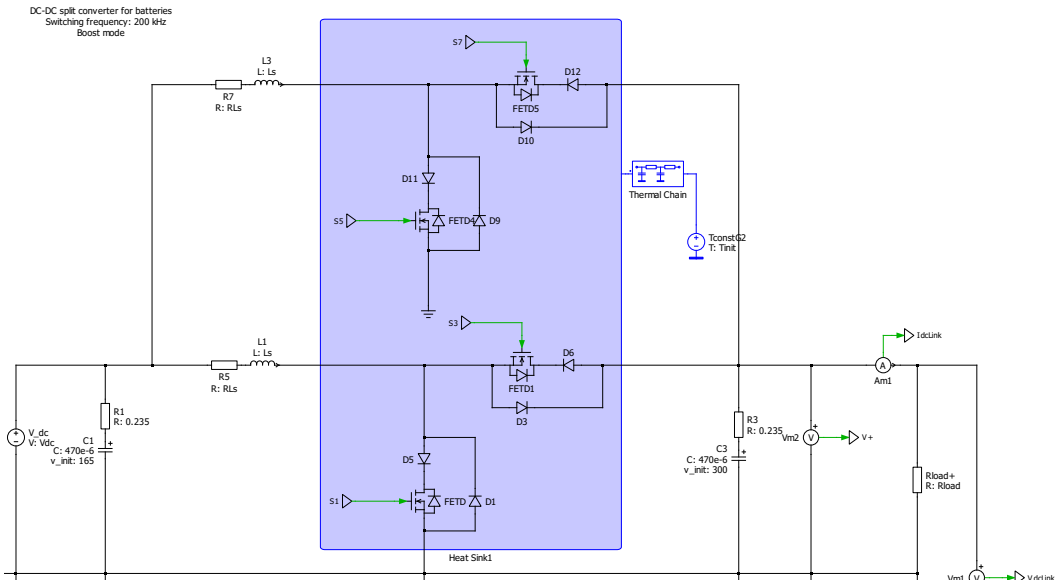


Figure 3.1: Screen dump in PLECS of the modelled IDPBSC in boost mode.

Due to some transients in the converter, as shown in Figure 3.2 in boost mode at nominal load. The power losses will first read out, when the converter seem to be stable.
Power losses is modelled and read out, but the power losses in the inductor is calculated as series resistance (0.349Ω) time the average current square.
The efficiency plot for the converter in boost mode is plot in Figure 3.2. The lowest efficiency is obtained when the input voltage is lowest and at nominal power. It is 97.06% in the simulation and the analytic calculation in the previuos chapter shows 96.76 which only differ by 0.3%. The explaination must be, since the added power lower of inductor is the same (calculated value), this show that the formular used in the anaylitic calculation is not differ so much from how Plecs uses to compute the losses.

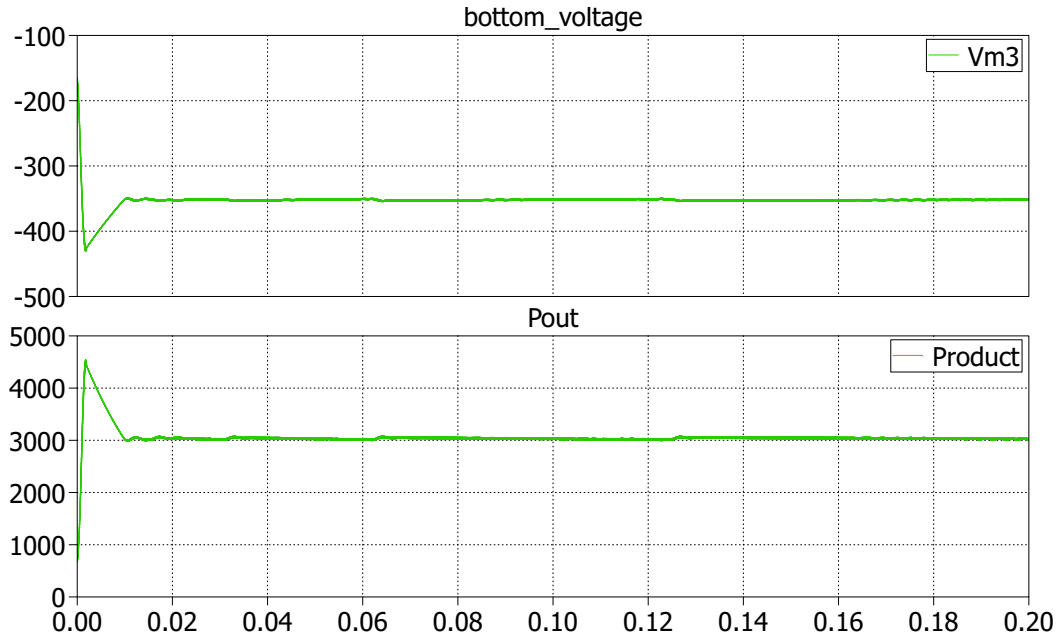


Figure 3.2: The transient in the modelled converter.

The efficiency is decreasing with increase power output, this make sense because the current is, thus power losses must increase as well.

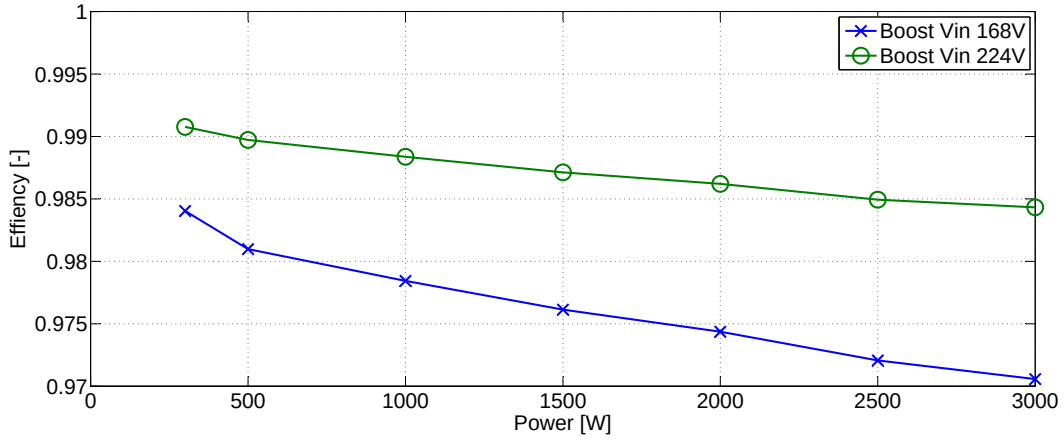


Figure 3.3: Efficiency plot in boost mode where solid blue line is for $V_{in} = 168$ and the solid green line is $V_{in} = 224$.

According to Figure 3.2, the highest efficiency is obtained with highest at lowest power demanding and is more than 99%.

3.2 Modelling of the buck part of converter

Similiar is done for the buck converter and the efficiency is plotted in Figure 3.4. No analytic calculations have been done, thus it cannot compare. The lowest efficiency is obtained with the lowest input voltage and is 97.5%. The highest efficiency is 99.3% and was reached with $224V$ in the input. Although the efficiency is really flat between $1kW - 3kW$.

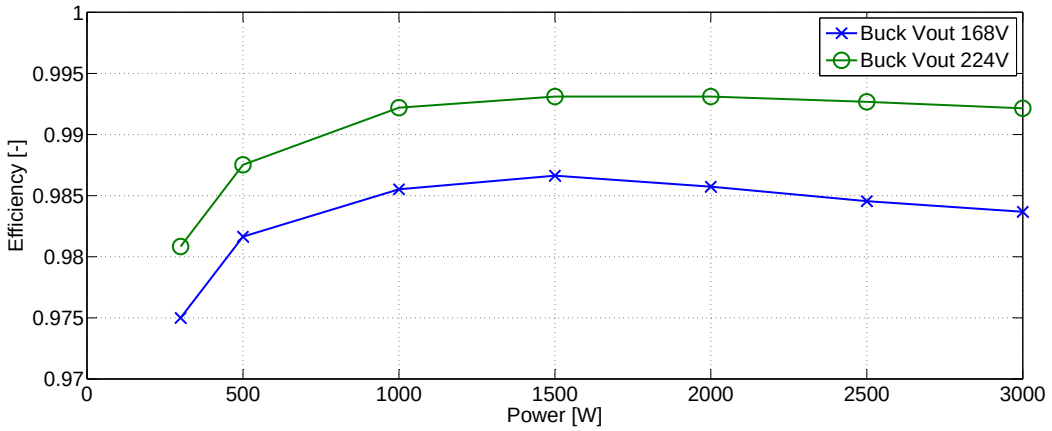


Figure 3.4: Efficiency plot in buck mode where solid blue line is for $V_{out} = 168$ and the solid green line is $V_{out} = 224$.

To summerise, in this chapter a thermal model has been create in PLECs/SIMULINK. The result from the simulation has confirmed the analytical calculation, which gives the confident of the target efficiency can be obtain. The next chapter will be about the pratical design og the converter.

Chapter 4

Converter design and practical results

Modelling the IDPBSC in previous chapter has justified analytic calculation of the efficiency. In this chapter the practical design of converter is addressed.
The schematic can be found in Appendix **??**.

4.1 Miscellaneous circuits

4.1.1 Sensing circuit

To monitor the voltage at the input and output for regulation, two voltage sensing circuits are implemented. The battery voltage is downscaled with R8 and R9, through the buffer (U2A) the signal will be send to the DSP. Furthermore the upper and lower threshold are detected by the comperators build around U1A and U1B to perform a hardware shutdown (U26 and U27).
Similiar is done for the DC Link voltage and formed around U1C and U2B, where the voltage scaling (R21 and R23) is different.

4.1.2 Current sensing

Four current sensing circuit is implemented; two for the battery input and two for the DC link. The signal will be send to DSP for monitoring and perform power calculation of the converter. As in the voltage sensing, the current sensing signal is also send to a onboard hardware protection (U26 and U27).

All four sensing circuit is identical, the one belongs to battery input $+350V$ is explained here. To reduce the power losses a hall effect-based linear current sensor IC with $100\mu\Omega$ current conductor is selected (ACS758[17]). This device is bidirectional and the sensitivity is $40mV/A$. At zero current this gives $2.5V$. Through U3A and the R29 and R28, the signal is amplified to $100mV/A$.

A voltage divide (R25 and R30) is implement so the voltage will never go more than 3V and this signal is send to the DSP. The downscaled signal is also used for hardware detection (U3C and R37) to perform a hardware shutdown (U26 and U27).

4.1.3 Gate drive

A small gate resistor will charge the input capacitance to the threshold voltage faster and thus reduce the transient time during switching, but to have control of dv/dt and di/dt, gate resistor value is recommend in the application note for CP CoolMOS[16]. For $dv/dt < 50V/nS$ the recommend gate resistor should not be lower than 15Ω. Beside the built-in 1.3Ω gate resistor, an external 33Ω is used during switch on and through a diode two parallel 33Ω will be used during switch off. The total gate resistance is approximate 10 times more than specified in datasheet for switch on and 5 times more during switch off, thus similiar scaling can expect for total switch on time (turn on delay + rise time) and switch off time (turn off + fall time), this gives $150ns$ and $325ns$ respectively.

To switch on the MOSFET in $150ns$, the gate charge (Q_g) of $80nC$ has to be pumped in, this gives a peak current of:

$$i_{gate_{peak}} = \frac{80 \cdot 10^{-9}}{150 \cdot 10^{-9}} = 0.54 \qquad [A] \tag{4.1}$$

To improve the immunity during switch off, the gate driver is feeded with $\pm 12V$.
The power losses in the gate driver can be calculated as[18]:

$$P_{gate} = V_{gs} \cdot Q_g \cdot f_{switching} = 24 \cdot 80 \cdot 10^{-9} \cdot 200 \cdot 10^3 = 0.348 \qquad [W] \tag{4.2}$$

Based on Equation 4.1 and 4.2 and $2.5A_{peak}$ gate driver (HCNW3120[19]) is selected.

4.1.4 Output filter capacitor

Beside fulfill the DC voltage (with some margin) the capacitor has to fulfill the current ripple from the converter. The maximun current ripple is equal the peak current of the boost inductor. In this converter it is 4.65, thus a margin should be added. The maximum current ripple that the selected electrolyt capacitor can handle can be calculated as[20]:

$$I_{rippel} = \sqrt{\frac{f \cdot a^2 \cdot b^2}{100 \cdot (b^2 - a^2) + (f \cdot a^2)}} \qquad [A] \tag{4.3}$$

where:
a is current ripple at 100 Hz
b is current ripple at 10 kHz and
f is frequency in Hz
This gives $7.39A$ for $200kHz$.

4.2 Protection

To keep the converter operating, all possible scenario that could kill the converter should be addressed and a solution should be implement to prevent it happens, this is called protection in this report. Inrush current control and short circuit current limiting is not mentioned here, because the converter will be feeded from power supply.

4.2.1 Gate and drive protection

To protect the gate drive circuit from any spike, which might enter from drain dv/dt, it is recommend to use ferrie beads[16].Furthermore a bidirectional TVS is added over gate-source to supress any possible transient, which exceed the maximum gate-source voltage.

4.2.2 Heat sink

In order to keep the semiconductor within the maximum allowed temperature, the generated heat must be take away, either active or passive. An electrical analog of the thermal process is shown in Figure 4.1.

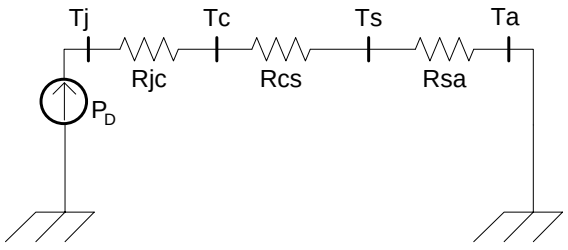


Figure 4.1: Electrical analog of the thermal process.

In the figure above, P_D is the heat source, T_j is the junction temperature, T_c is the case temperature, T_s is the heatsink temperature, T_a is the ambient temperature, R_{jc} is the junction to case thermal resistance, R_{cs} is the case to heat sink resistance and R_{sa} is the heat sink to ambient resistance.
The maximum allowable power dissipation is [21]:

$$P_D = \frac{T_{jmax} - T_a}{R_{ja}} \qquad [W] \tag{4.4}$$

Thus R_{ja} must be:

$$R_{ja} < \frac{T_{jmax} - T_a}{P_D} \qquad [K/W] \tag{4.5}$$

There are two heat sinks on the converter, one for the positive and the other for the negative. All 12 semiconductors will share the same heat sink, thus the heat sink should selected based on the worst

case power dissipation. Based on Table 2.3, the MOSFET dissipate most; $13.6W$.
Assume the $T_a = 50°C$. $T_{jmax} = 150°C$ and thus R_{ja} is:

$$R_{ja} < \frac{150 - 50}{13.6} = 7.35 \qquad [K/W] \tag{4.6}$$

From Figure 4.1, $R_{ja} = 7.35K/W$ is included R_{jc} of $0.5K/W$ from the datasheet and $1K/W$ for the thermal insulation pad. Themal selected heat sink is of type PR118/94/SE/M3[22] which has $3.2K/W$.

4.2.3 Thermal sensing

In the prototype two temperature sensors; LM35[23] (U28 and U29) are implemented, one for each heat sink. The potentiometer R81 determine the threshold temperature to trigger the hardware shutdown.

4.2.4 Onboard protection

To handle the hardware shutdown, a programmable electrical erasable logic (PEEL) device is used to form the protection hardware. The PEEL22CV10[24] up to 22 inputs and ten outputs. The benefite of programmable gives the flexibility, if something have to be addon or modify. Beside the mentioned hardware shutdown above, this onboard protection prevents gate signals to perform cross conduction of switches.

4.3 Practical works

After running the first PCB (version 1), some problems are observed. In Figure fig:ringningboost a $20MHz$ oscillation occurs and die out after $140ns$, this was measured with a current $50MHz$ current probe. The reverse recovery time of the SiC diode should be around $20nS$. Furthermore the turn off time is too slow, the gate resistor was 33Ω, thus this suspect a high Drain-Source parasitic capacitance.

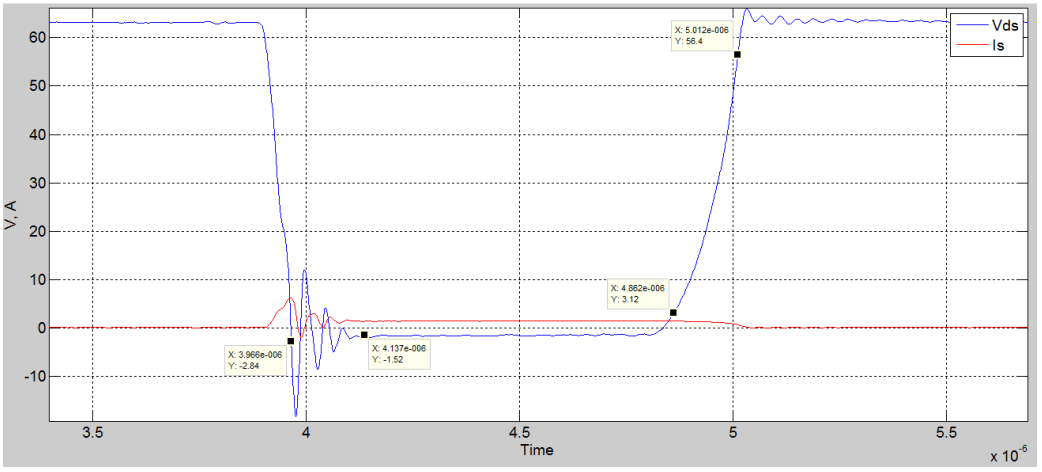


Figure 4.2: Observed problem in boost mode; 140ns oscillation and too slow turn off time.

In buck mode, the problem is shown in Figure 4.3 when RC snubber is not connected; a ringing of twice the input voltage occured, this must come from parasitic inductances and together with parasitic capacitance resonate.

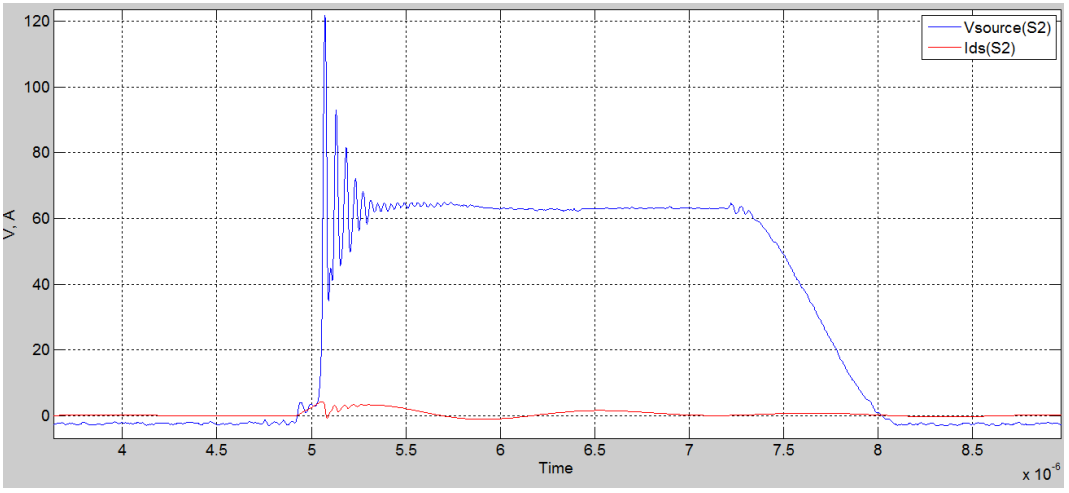


Figure 4.3: Observed problem in buck mode without RC snubber; high voltage ringing and slow turn off time.

These problem consider to be more than what cut and repair of the PCB trace can solve, so another PCB (version 2) is built, but time could not allow to run version 2 and carry out the results. This work is expected to continuous after the report submit.
Some of the improvement in version 2 is mentioned here.

4.3.1 PCB routing strategy

A good routing layout is an essential part of the converter design as this can improve the practical performance of converter, especially in high frequency hard switching. Trace width should at least

fulfill IPC-2221 standard[25]. The strategies which have been used in version 2 of the PCB are:

Avoid routing gate, source and drain PCB track in parallel as much as possible, because this will increase (parasitic) capacitances.

Keep the gate drive and its components close to the gate and use wide trace to avoid parasitic inductances. This helps by using SMD components.

Use the identical layout for the two phases.

Use wide and short commutation path to reduce parasitic inductance.

Use start grounding so high current circulation is no affect small signal circuit.

Some of the applied strategy can be seen in Figure 4.4 and the

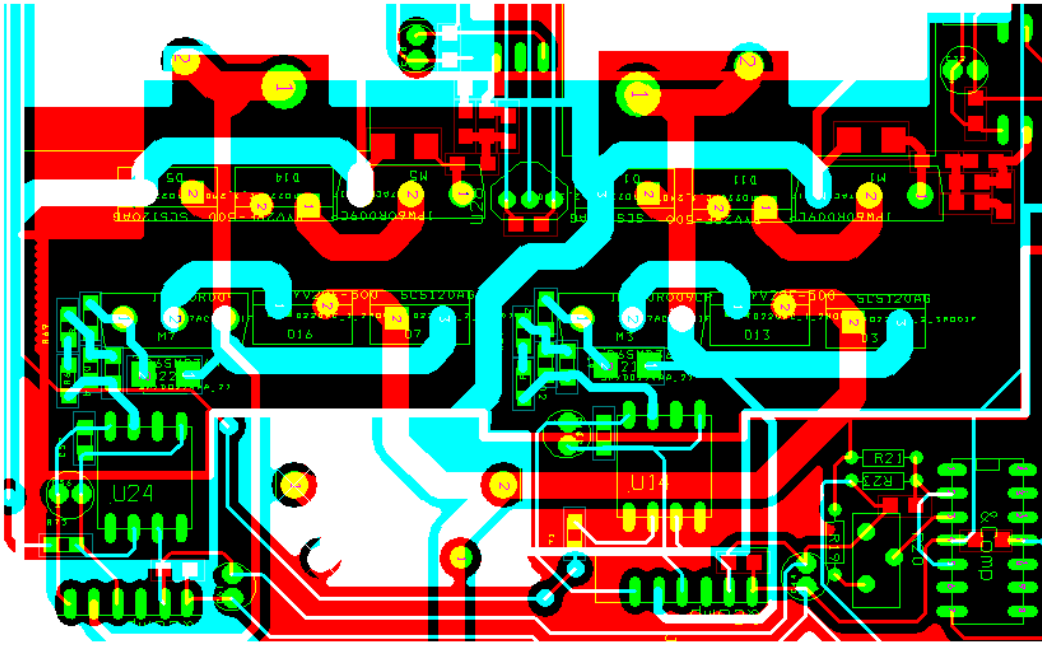


Figure 4.4: Section of PCB traces in version 2. where some routing strategies is visible.

4.3.2 Efficiency report

The setup to be carry on for testing the efficiency is shown below. This will be perform in openloop, where to interlead signal from from function generators is feeded the converter and the efficiency will be recorded at the same point as the losses modelling.

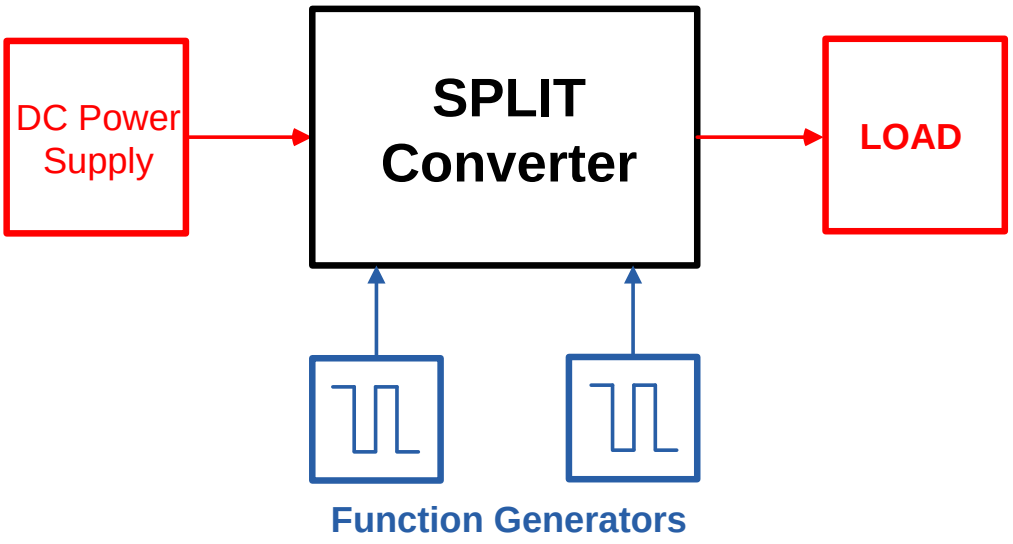


Figure 4.5: The sketch of laboratory setup for testing efficiency.

More to come...

Chapter 5

Conclusion and future work

In this report a novel high efficiency topology has been proposed, which can used low voltage switches and manage bidirectional power flow. Due to the challenge of purchase, a modification of switching device and topology is necessary in order to reach the high efficiency target. A methodology has been established to perform an analytic calculation of power losses. A thermal model in Plecs has been created to predict the losses. As the result, the simulation confirms the analytical calculations, the worst case efficiency is 97% at nominal power in boost mode and 98.3 in buck mode. Taken into account of the obtained results, the converter has been designed and built to validate the simulation model. Due to time constraint the practical work has been postponed to after the report submit.

5.1 Future work

Beside verify the efficiency the control implementation with DSP can be done. Furthermore it can be integrated in PV applications and perform field test. Improvement of the efficiency can be done by using a high saturation flux density core or using other switches technology to perform active rectify/freewheeling.

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Appendix A

Methodology

During the power convertion of a converter, the input current has to flow through semiconductors, inductor, filtering ect. before it is avaiable at the output. None of components are ideal, thus some energy has been lost in each component. This appendix provides an analytic tool to estimate some related losses of this converter. Power losses increases with the increased current and the high current path in this converter is through semiconductors devices and boost/filter inductor.

A.1 Losses in the converter

A.1.1 Losses in semiconductors

Power losses in any components can be divided in three groups [26]:

- Conduction related losses; P_c.
- Switching related losses; P_{sw}.
- Blocking/leakage losses P_l.

The conduction losses are represented by the energy lost in the device during the on-state.
The switching losses represent the energy losses which occur during the finite switching transient, as the operating state of the switch is changed from on(off) to off(on).
The blocking losses is normal considered to be very small and can be neglected.
Thus the power losses can be approximated as:

$$P_{losses} \approx P_c + P_{sw} \qquad [W] \tag{A.1}$$

A.1.1.1 MOSFETs

Conduction loss in MOSFETs[26]
The conduction loss in a MOSFET can be determined by using the Drain-Source on-resistance ($R_{DS_{on}}$) and the current through the device. The on-resistance is depended on Gate-Source voltage (V_{GS}), Drain current (I_D) and junction temperature (T_j).
V_{GS} is usually fixed, so the conduction loss of the MOSFETs can be computed as:

$$P_{c_{MOSFET}} = R_{DS_{on}}(T_j) \cdot I^2_{D_{on}} \qquad [W] \tag{A.2}$$

MOSFETs are positive temperature coefficient devices thereby the conduction loss is also increasing with temperature. To take the temperature into account, Equation A.3 can be used.

$$R_{DS_{on}}(T_j) = R_{DS_{onMax.}}(25°C) \cdot (1 + \frac{\alpha}{100})^{T_j - 25°C} \qquad [\Omega] \tag{A.3}$$

where:
$R_{DS_{onMax.}}(25°C)$ *is the maximun value at* $25°C$
T_j *is the junction temperature of the operation point and*
α *is the slope between* $R_{DS_{onMax.}}(25°C)$ *and* T_j.

The $R_{DS_{on}}$ as function of temperature can be found in datasheet as shown for the case of IPW60R099CP in Figure A.1, where the manufacture has plotted the typical and the maximun variation in the same plot.

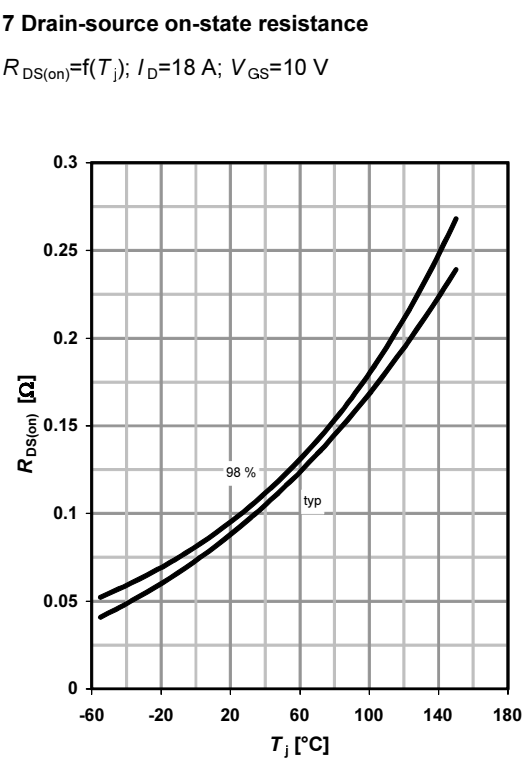

Figure A.1: $R_{DS_{on}}$ as function of junction temperature for IPW60R099CP[4].

Instead of Equation A.3, an estimation can also be used by read out the worst case junction temperature for this device, this is shown in Figure A.2 for different Gate-Source voltage (V_{GS}) at $150°C$.

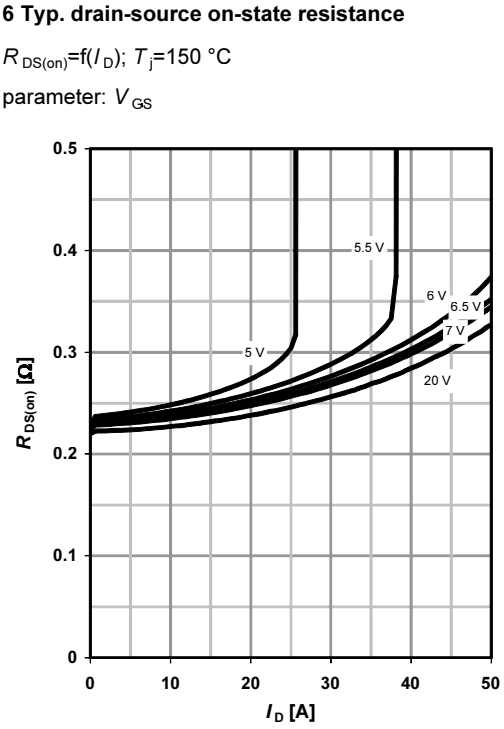

Figure A.2: $R_{DS_{on}}$ charateristic for IPW60R099CP[4] at $150°C$.

Switching loss in MOSFETs[26][16]

Due to parasitic capacitance in the MOSFET; Gate-Source (C_{gs}), Gate-Drain (C_{gd} or C_{rss}) and Drain-Source (C_{ds}), the switching dynamics are governed by charging and discharging those capacitors through the gate resistor (R_g).
The switch-on waveform of the MOSFET is sketch in Figure A.3. Where V_{DD} is the applied DC bus voltage, I_D is the Drain current and I_F is the forward current of the body diode.

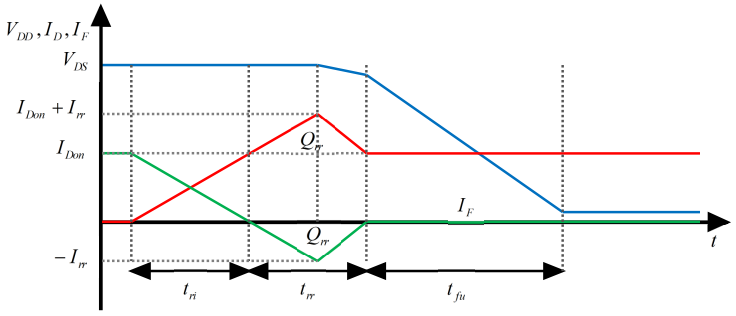

Figure A.3: Switch-on waveform of the MOSFET.

Through the gate resistor, the input capacitance ($C_{iss} = C_{gd} + C_{gs}$) is charged to the gate driver

voltage (V_{gs}). Once the voltage at the gate (V_{gate}) reachs V_{platue} the output current will rise to $I_{D_{on}}$ and the current of the body diode is decreased, while voltage over Drain-Source is remained at DC link voltage. This current rise time is called t_{ri}.
To switch off the diode, the stored minority carriers have to be removed, this is done during the reverse recovery time (t_{rr}). The MOSFET will absorb this recovery current and thus gives further loss. After the reverse recovery time the Drain-Source voltage decrease from DC link voltage toward the on voltage ($V_{DS} = I_{D_{on}} \cdot R_{DS_{on}}$), this time periode is called voltage fall-time (t_{fu}) and is governed by the output capacitance (C_{ds}). The energy losses during switch-on are the sum of losses during the mentioned time constants and can be computed as:

$$E_{MOSFET_{on}} = V_{DD} \cdot (I_{D_{on}}) \cdot \frac{t_{ri} + t_{fu}}{2} + Q_{rr} \cdot V_{DD} \qquad [J] \tag{A.4}$$

The waveform during MOSFET switch-off is sketched in Figure A.4. The gate drive will discharge C_{iss} through R_g. Once V_{gate} drops to V_{platue}, V_{DS} start rise to V_{DD}. This voltage rise time t_{ru} is determined as:

$$t_{ru} = \frac{R_g \cdot C_{rss} \cdot V_{DD}}{V_{platue} - V_{gs_{off}}} \qquad [s] \tag{A.5}$$

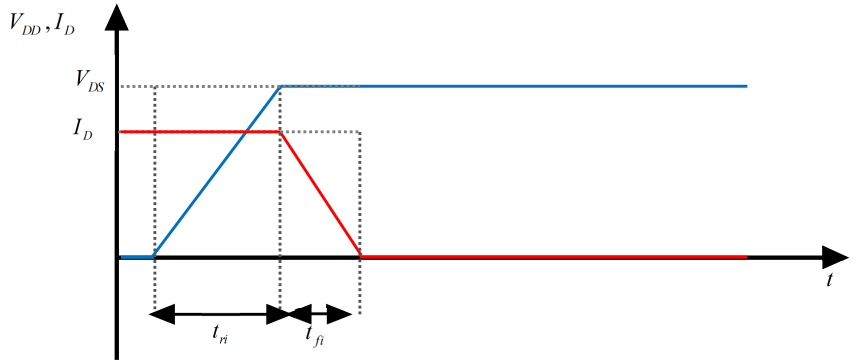

Figure A.4: Switch-off waveform of the MOSFET.

Once $V_{DS} = V_{DD}$, V_{platue} drops further due to dicharge of C_{iss} through R_g and in the mean time $I_{D_{on}}$ drops down to zero. This current fall time (t_{fi}) is computed as:

$$t_{fi} = R_g \cdot C_{iss} \cdot ln \frac{V_{platue} - V_{gs_{off}}}{V_{th} - V_{gs_{off}}} \qquad [s] \tag{A.6}$$

Both the threshold voltage (V_{th}) and the platue voltage (V_{platue}) is specified in the datasheet.

The energy losses during switch-off can be found as:

$$E_{MOSFET_{off}} = V_{DS_{off}} \cdot (i_{D_{off}}) \cdot \frac{t_{ru} + t_{fi}}{2} \qquad [J] \tag{A.7}$$

The power loss during switching can be expressed as:

$$P_{sw_{MOSFET}} = (E_{MOSFET_{on}} + E_{MOSFET_{off}}) \cdot f_{sw} \qquad [W] \tag{A.8}$$

As the summary, to have low losses, the MOSFET should have low $R_{DS_{on}}$, low input capacitance and low reverse recovery energy. Low $R_{DS_{on}}$ gives low conduction loss, low input capacitance to reduce switching transient duration and thus switching loss and low reverse recovery energy, because this is an addition loss to the switching losses.

A.1.1.2 Diodes

[26] The conduction losses of the diode can be approximated by two terms, the average current through a DC source represents the diode voltage at zero current and another source which is depended on the dynamic resistance and the rms current through the diode, thus it can be expressed as:

$$P_{c_{Diode}} = V_{D0} \cdot I_{Fav} + R_D \cdot I^2_{Frms} \qquad [W] \tag{A.9}$$

Theo zero curren voltage source and the dynamic resistance can be read out from the datasheet as shown in Figure A.5 for the body diode of the IPW60R099CP device.

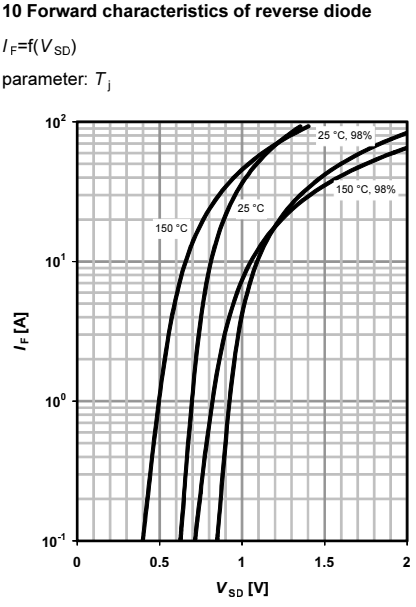

Figure A.5: Diode forward charateristics.

The energy loss during switching the diode is dominated by the turn-on energy (reverse recovery energy) and can be found as:

$$E_{sw_{Diode}} = \frac{1}{4} \cdot Q_{rr} \cdot V_{Drr} \qquad [W] \tag{A.10}$$

where:
V_{Drr} is the peak voltage during reverse recovery and
Q_{rr} is the recovery charge.

A.1.2 Losses in the inductor

Two type of losses are usually addressed in inductor design, they are: winding losses and core losses. Operate the converter in continuous-current mode operation with especially with small current ripple (fraction of the full load), core losses can be neglected because only small part of B-H loop is utilised.
The winding losses can be divided into two part; low frequency and the high frequency.
The low frequency loss is copper loss due to DC resistance (R_dc) in the conductor, which is[11]:

$$R = \rho \cdot \frac{l_b}{A_w} \qquad [\Omega] \tag{A.11}$$

where:
ρ is the resistivity,
l_b is the lenght and
A_w is the bare cross section.

The high frequency loss is due to eddy current and causes skin and proximity effect.
Skin effect is governed by the eddy current which oppose the primary ac flux in the conductor, as the result, current density is not uniform distributed, but rather more concentrate on the surface than the center of the conductor. Skin depth expresses the penetration depth and is:

$$\sigma = \sqrt{\frac{\rho}{\pi \cdot \mu 0 \cdot f}} \qquad [m] \tag{A.12}$$

where:
ρ is the resistivity in Ωm and
f is frequency in Hz.

As seen from Equation A.11, thicker conductor gives lower R_{dc} due to larger bare cross section, but on the other hand if skin depth from Equation A.12 is not taken in to account, only fraction of the conductor is utilised and the ac resistance (R_{ac}) can be dominated. The relationship between dc

and ac resistance is as[27]:

$$\frac{R_{ac}}{R_{ac}} = \frac{\pi \cdot r^2}{\pi \cdot r^2 - \pi \cdot (r - \sigma)^2} \qquad [-] \tag{A.13}$$

where:
r *is radius of the conductor.*

One way to overcome this challenge is by using multi stands wire also known as Litz wire. Litz wire is multiple thin insulated copper wires which are bundled together, thus larger cross section area can obtain without violate the penetration depth.
The proximity effect is similiar to skin effect, but coupled between the layers. By using Litz wire, this loss can maitain low and not adresse here.

A.1.3 Others losses in the converter

Beside the power losses in the inductor and semiconductors during power processing, other losses exist like in gate driver, filter capacitors and other type of circuits. Most of them are relative small and can neglected, but one should be mentioned which can not be determined in forehand is the snubber.
Due to parasitic inductance and capacitor caused by the phycial layout, energy can be stored in the layout and create voltage transient during turn-off the switch, which gives more switching loss than expected and the transient can be dangerous high and kill semiconductors. Snubber can be used reduce the stress of semiconductor by either passive dissipate the energy or active recovery this energy so the voltage limit can be fulfilled. It should also be mentioned that snubber is also used to mimigate the EMI emission, but emission is not required for the prototype. As mentioned in Chapter 1, design converter is an iterative process, so the first iteration is used simple passive and aim for a good PCB layout, some used layout tips can be found in [16].

Appendix B

Inductor design step by step

The operation voltage window of eight series connected battery modules is $336 - 448V$. From Equation 2.1, the duty cycle of the boost converter can be expressed as:

$$D_{boost} = 1 - \frac{V_{out_{boost}}}{V_{in}} \qquad [-] \tag{B.1}$$

Thus step up to $700V$, the duty cycle window; $D = 0.36 - 0.52$. The nominal output current at $3kW$ is:

$$I_{DC_{link}} = \frac{P_{DC_{link}}}{V_{DC_{link}}} = \frac{3000}{700} = 4.29 \qquad [A] \tag{B.2}$$

If the power converter is lossless, then the average input current at nominal power will be:

$$I_{L_{boost}} = \frac{I_{DC_{link}}}{0.52} = 8.25 \qquad [A] \tag{B.3}$$

Similiar can be done for the buck converter by using Equation 2.2, the duty cycle of the buck converter is:

$$D_{buck} = \frac{V_{in}}{V_{out_{buck}}} \qquad [-] \tag{B.4}$$

Hence the window of duty cycle for the step down; $D0.48 - 0.64$.
The highest output current at $3kW$ of the buck converter is:

$$I_{L_{buck}} = \frac{P_{DC_{bat.}}}{V_{DC_{bat.}}} = \frac{3000}{336} = 8.93 \qquad [A] \tag{B.5}$$

B.1 Inductor design

$$V_{DClink} = 700[V] \tag{B.6}$$

$$f_{sw} = 200 \cdot 10^3[Hz] \tag{B.7}$$

$$T_{sw} = \frac{1}{f_{sw}} = 5 \cdot 10^{-}6[s] \tag{B.8}$$

$$P_{min} = 300[W] \tag{B.9}$$

$$P_{max} = 3000[W] \tag{B.10}$$

$$R_{load_{min}} = \frac{V_{DClink}^2}{P_{min}} = 1633[\Omega] \tag{B.11}$$

$$R_{load_{max}} = \frac{V_{DClink}^2}{P_{max}} = 163.33[\Omega] \tag{B.12}$$

$$V_{bat_{min}} = 4 \cdot 42 = 168[V] \tag{B.13}$$

$$V_{bat_{max}} = 4 \cdot 56 = 224[V] \tag{B.14}$$

$$V_{out} = \frac{V_{DClink}}{2}[V] \tag{B.15}$$

$$D_{min} = 1 - \frac{V_{bat_{max}}}{V_{out}} = 0.36[V] \tag{B.16}$$

$$D_{max} = 1 - \frac{V_{bat_{min}}}{V_{out}} = 0.52[V] \tag{B.17}$$

To ensure CCM in dual phases split; $I > \Delta iL$:

$$L_{min} = \frac{D_{max} \cdot (1 - D_{max})^2 \cdot R_{load_{min}} \cdot T_{sw}}{2} = 489.2\mu H \qquad [H] \tag{B.18}$$

$$L_{max} = \frac{D_{min} \cdot (1 - D_{min})^2 \cdot R_{load_{min}} \cdot T_{sw}}{2} = 602.1\mu H \qquad [H] \tag{B.19}$$

$$\Delta iL_{min} = \frac{V_{bat_{max}}}{2 \cdot L_{max}} \cdot D_{min} \cdot T_{sw} = 0.335 \qquad [A] \tag{B.20}$$

$$\Delta iL_{max} = \frac{V_{bat_{min}}}{2 \cdot L_{max}} \cdot D_{max} \cdot T_{sw} = 0.363 \qquad [A] \tag{B.21}$$

$$K = 1 - \frac{2 \cdot L_{max}}{R_{load_{min}} \cdot T_{sw}} = 0.147 \qquad [-] \tag{B.22}$$

$$K_{crit.} = D_{max} \cdot (1 - D_{max})^2 = 0.12 \qquad [-] \tag{B.23}$$

$$I_{load_{min}} = \frac{P_{min}}{V_{DC_{link}}} = 0.67 \qquad [A] \tag{B.24}$$

$$I_{load_{max}} = \frac{P_{max}}{V_{DC_{link}}} = 4.286 \qquad [A] \tag{B.25}$$

$$I_{Ldc_{min}} = \frac{I_{load_{min}}}{1 - D_{min}} = 0.67 \qquad [A] \tag{B.26}$$

$$I_{Ldc_{max}} = \frac{I_{load_{min}}}{1 - D_{max}} = 8.929 \qquad [A] \tag{B.27}$$

$$I_{L_{min}} = I_{Ldc_{min}} - \Delta iL_{min} = 0.335 \qquad [A] \tag{B.28}$$

$$I_{L_{max}} = I_{Ldc_{max}} - \Delta iL_{max} = 9.291 \qquad [A] \tag{B.29}$$

Design from [11]:

Constraint 1: Maximum flux density

$$I_{max} = \frac{I_{L_{max}}}{2} = 4.646 \qquad [A] \tag{B.30}$$

$$B_{max} = 0.34 \qquad [T] \tag{B.31}$$

$$\mu_0 = 4 \cdot \pi \cdot 10^{-7} \tag{B.32}$$

$$n \cdot I_{max} = B_{max} \cdot \frac{l_g}{\mu_0} \qquad [-] \tag{B.33}$$

Constraint 2: Inductance

$$L_{boost} = \frac{\mu_0 \cdot A_c \cdot n^2}{l_g} \qquad [H] \tag{B.34}$$

Constraint 3: Winding area

$$K_u \cdot W_a \geq n \cdot A_w \tag{B.35}$$

K_u has been estimated by first wound the number of turns and estimate the windows fill factor (K_u). Estimate to be 0.3.

Constraint 4: Winding resistance

$\rho cu_{25} = 1.724 \cdot 10^{-6} \qquad [\Omega - m]$

$\rho cu_{100} = 2.3 \cdot 10^{-6} \qquad [\Omega - m]$

The geometric data of the core is specified by the manufacture.

ETD34:

$A_c = 0.97$

$MLT = 6$

$$l_g = \frac{\mu_0 \cdot L_{boost} \cdot I_{max}^2}{B_{max}^2 \cdot A_c} \qquad [m] \tag{B.36}$$

$$n = \frac{\cdot L_{boost} \cdot I_{max}}{B_{max}^2 \cdot A_c} \cdot 10^4 \qquad [m] \tag{B.37}$$

$A_w = 2.513 \cdot 10^{-3} \qquad [cm^2]$

resitance = $\rho \cdot \frac{n \cdot MLT}{A_w} = 0.349\ K_g \geq \frac{\rho \cdot L_{boost}^2 \cdot I_{max}^2}{B_{max}^2 \dot{r}esistance \cdot K_u} = 0.111$ This justify that ETD34 can be used.

Appendix C

Schematics of the converter

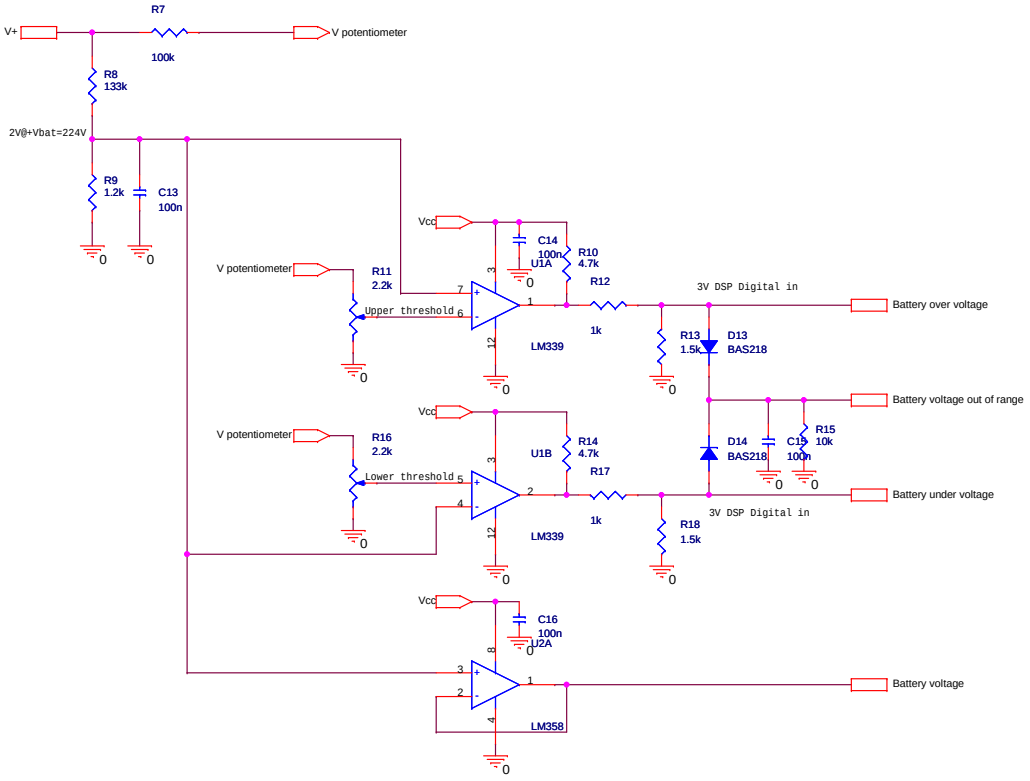

Figure C.1: Battery sensing circuit.

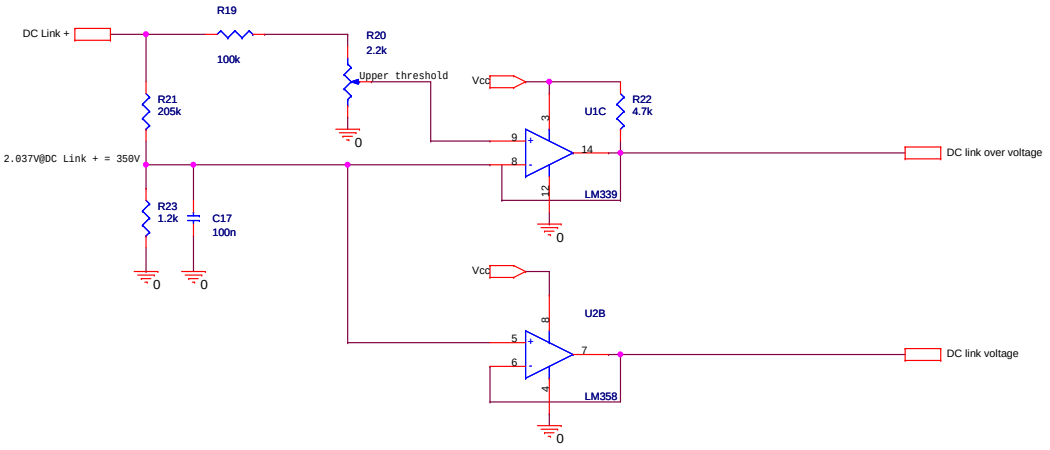

Figure C.2: DC link sensing circuit.

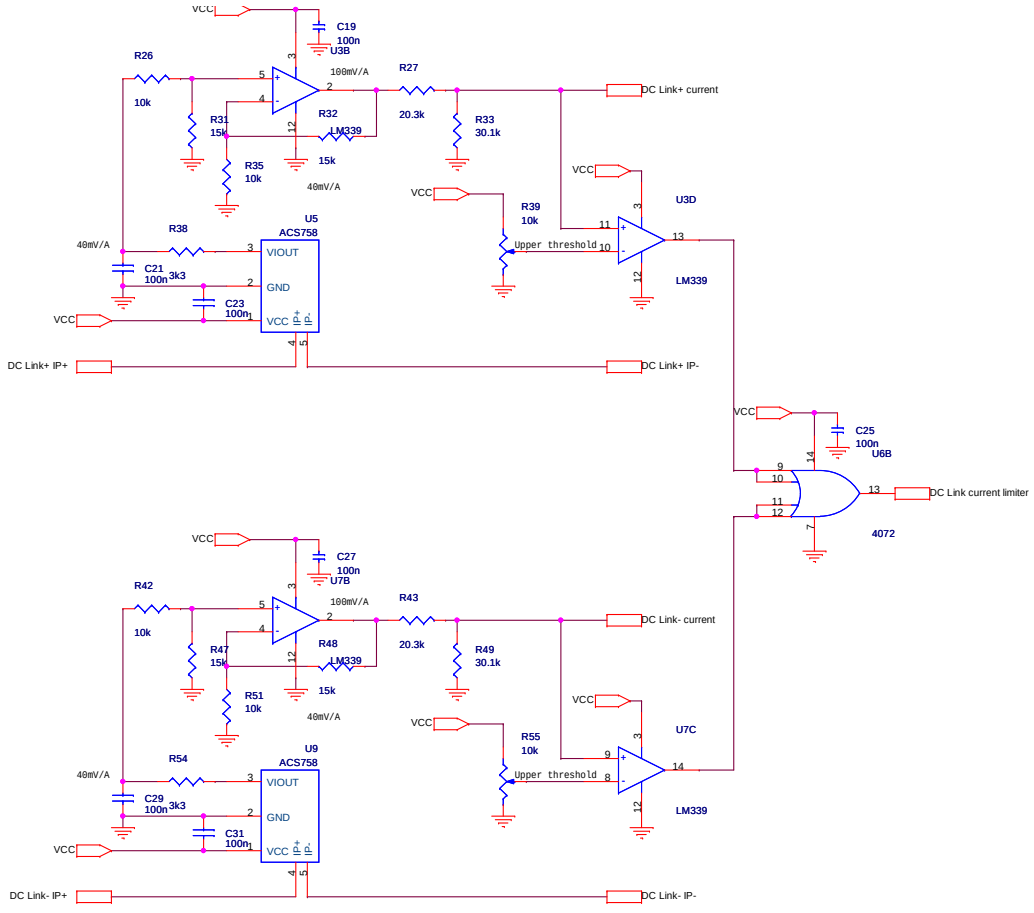

Figure C.3: Current sensing circuit.

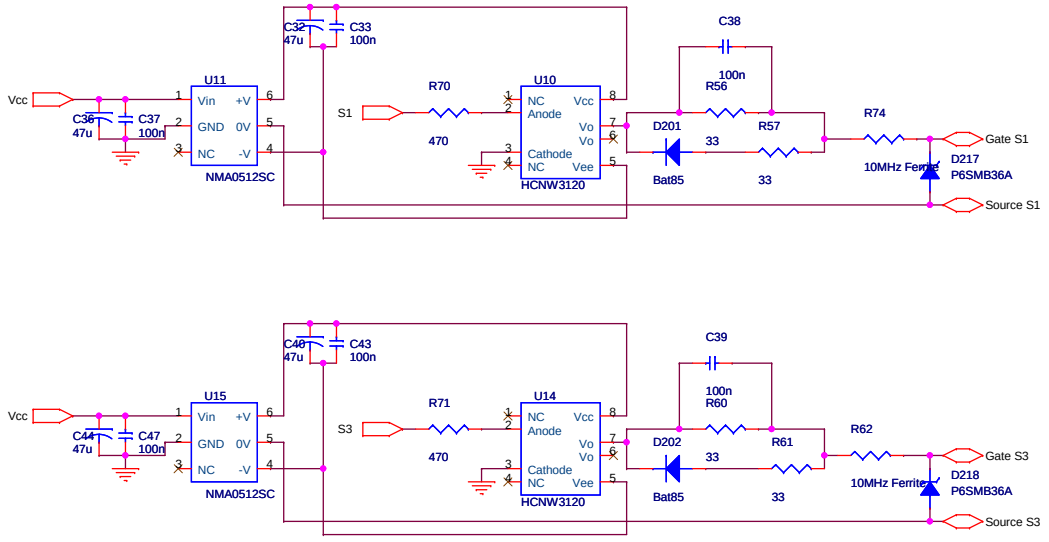

Figure C.4: Gate drives .

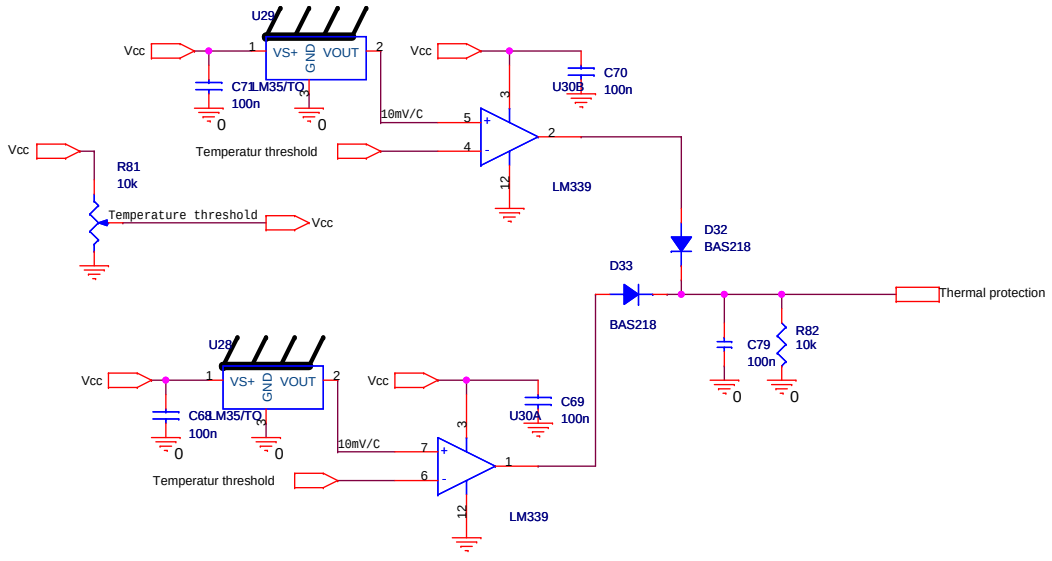

Figure C.5: Thermal sensing circuit.

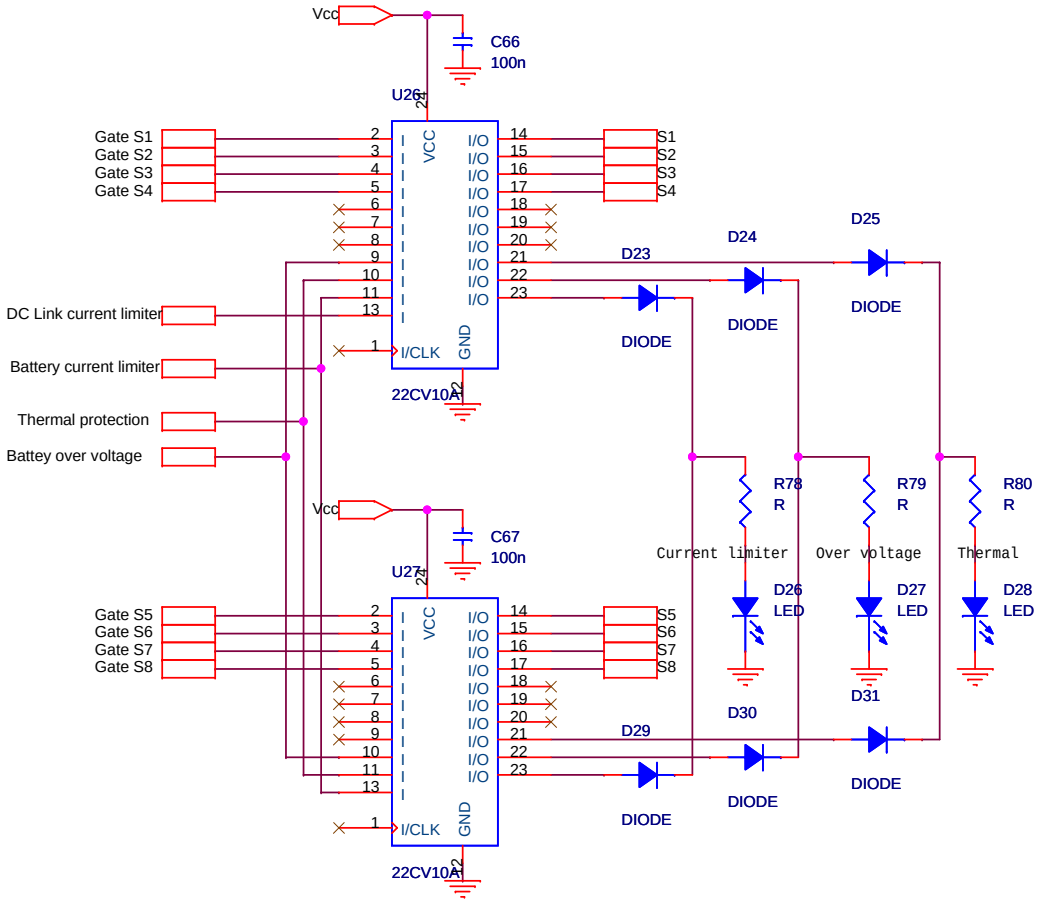

Figure C.6: On board programmable protection circuit.