High-Power Density PFC Converter Design with SiC-based Power Module

MSc Thesis, with specialisation in Power Electronics and Drives

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Department of Energy Technology, PED4-1041, 11-2023

Software programs utilized in the report.

1. MATLAB
2. PLECS
3. Altium Designer
4. Code Composer Studio
5. Visio

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http://www.energy.aau.dk

AALBORG UNIVERSITY
STUDENT REPORT

Title:
High-Power Density PFC Converter Design with SiC-based Power Module

Theme:
Design of interleaved boost converter for PFC applications

Project Period:
4th Semester 2023

Project Group:
PED4-1041

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Supervisor(s):
Pooya Davari

Copies: Unlimited

Page Numbers: 95

Date of Completion:
November 3, 2023

Abstract:

With the escalating adoption of electric vehicles worldwide, the demand for efficient charging solutions has become paramount. Power factor correction (PFC) technology, known for its high power factor and minimal input current harmonic distortion, has gained prominence in the quest for advanced charging systems. This project delves into the intricate design and optimisation of an interleaved PFC converter employing SiC MOSFET module with 3 integrated boost legs. The ability of the interleaving technique to maintain acceptable efficiency across a wide range of output powers via phase-shedding management is a major advantage. The design and optimisation of the boost inductor and EMI filter under such operating conditions to increase power density, however, has not been thoroughly investigated. As a result, the primary goal of this study is to investigate various aspects impacting the performance of a single phase three stage interleaved PFC converter to maximise its power density.

Table 1: Nomenclature of abbreviations throughout the report.

Nomenclature	
Abbreviation	**Description**
Alternating Current	AC
American Wire Gauge	AWG
Average Current Mode Control	ACMC
Boundary Conduction Mode	BCM
Common mode	CM
Continuous Conduction Mode	CCM
Differential mode	DM
Digital Signal Processor	DSP
Direct Current	DC
Discontinuous Conduction Mode	DCM
Electric Vehicle	EV
Electromagnetic Interference	EMI
Equivalent Series Inductance	ESL
Equivalent Series Resistance	ESR
Integrated Circuit	IC
International Electrotechnical Commission	IEC
Line Impedance Stabilization Network	LISN
Metal Oxide Semiconductor Field Effect Transistor	MOSFET
Power Factor	PF
Power Factor Correction	PFC
Printed Circuit Board	PCB
Pulse-Width Modulation	PWM
Quasi-continuous Conduction Mode	QCM
Quasi-peak	QP
Root Mean Square	RMS
Silicon	Si
Silicon Carbide	SiC
Small Signal Model	SSM
Surface Mount Device	SMD
Total Harmonic Distortion	THD
Wide Band Gap	WBG

Table 2: Symbols used throughout the report.

Symbols	
Subscript	**Description**
A	Area
C	Capacitance
I	Current
d	Derivative
D	Duty cycle
f	Frequency
K_p, K_i	Gain
H	Height or Magnetic field strength depending on context
L	Inductance or Length
s	Laplace operator
N	Number of turns or layers or cores
T	Period or Temperature
P	Power
R	Resistance
t	Time
$G(s)$	Transfer function
V	Voltage or Volume
W	Width

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Preface

Aalborg University, November 3, 2023

This report has been developed as part of the Master's Thesis during the 4th semester of MSc in Energy Engineering in the specialisation of *Power Electronic and Drives* at Aalborg University. The main objective of the project was to design a *High-Power Density PFC Converter with SiC-based Power Module*. LaTeX is used for documenting the project work and simulations are carried out in PLECS and MATLAB. The hardware prototyping of the PFC converter is developed in Altium Designer.

The prerequisites for reading the report are a certain knowledge of mathematics, physics, circuit analysis theory and power electronics.

I extend my heartfelt gratitude to my supervisor, Pooya Davari for his unwavering support and invaluable guidance throughout the entire semester. His input has been instrumental in the successful development of this project, providing me with the expertise and knowledge I needed. Moreover, I want to extend my heartfelt gratitude to my significant other, family, friends, and fellow members in the EMI/EMC in Power Electronics research group for their constant presence and unwavering support.

Reading instructions

In this project, the Vancouver method is used for referencing which means that after every section the reference will be listed as [1, 2, 3, etc.]. All references are sorted as they appear in the report and will be included in the bibliography at the end of the report.

The project contains figures and tables, which are numbered by the chapters. Hence, the first figure in Chapter 1 has number 1.1 and the following figure has number 1.2, etc. The symbols in the nomenclature are listed in alphabetical order.

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Contents

Chapter 1
Introduction

1.1 Motivation and Background

The emerging technology of Electric Vehicles (EV) has contributed to a shift towards more sustainable transportation options and has the potential to significantly reduce greenhouse gas emissions and improve air quality. Longer driving ranges and faster charging times, brought about by improvements in battery technology, have made EVs more practical for both longer trips and everyday use. Given the rapid increase in the market presence of EVs with higher battery capacity, the establishment of a fast and efficient charging infrastructure is deemed necessary [1].

EV charging systems rely significantly on the role played by power electronic converters. The road map for power electronics R&D in EVs for the next 20 years demands huge increase in the desired characteristics of on-board chargers to encompass high efficiency, high power density, high reliability, and low cost[2]. Moreover, ensuring that Total Harmonic Distortion (THD) resulting from EV chargers remains below 5% is imperative to mitigate power quality issues and ensuring the extraction of maximum real power by drawing grid current at a high Power Factor (PF)[1].

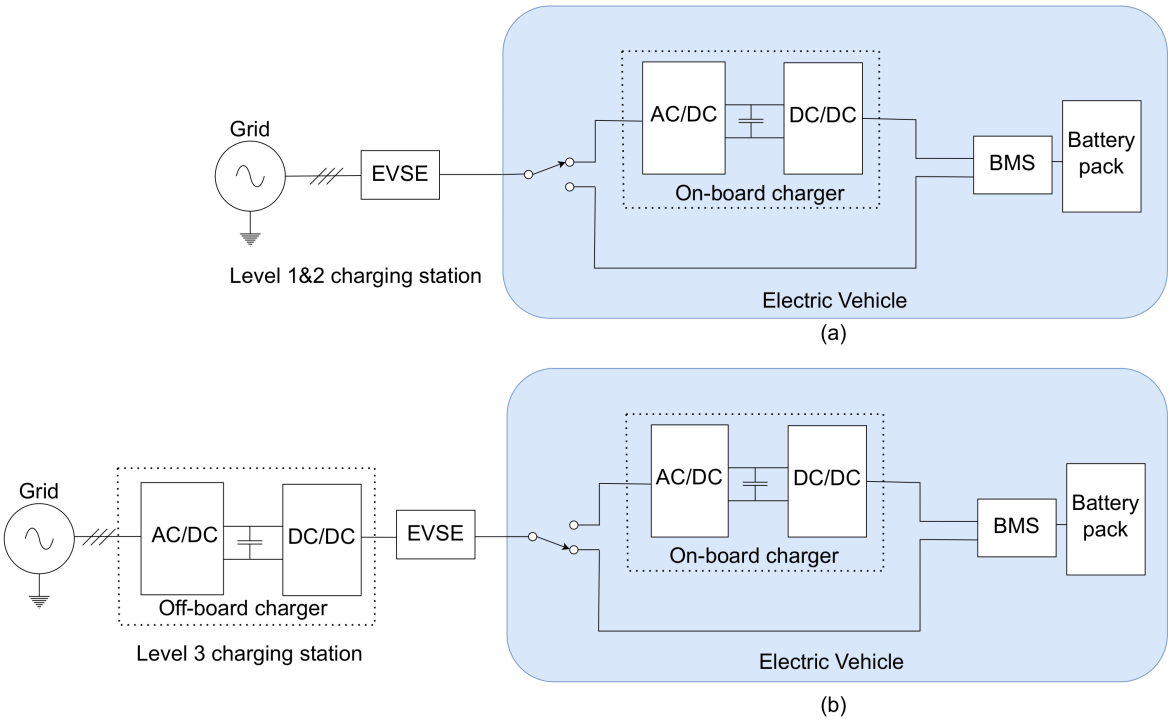


Figure 1.1: Level 1, 2 and 3 charging infrastructure in Electric vehicles.

EV chargers can be categorised as either on-board chargers or off-board chargers. On-board electric vehicle chargers refer to chargers that are installed within the vehicle

itself, while off-board chargers pertain to those that are not integrated into the vehicle and are typically situated at a charging station or at the user's residence. On-board chargers fall under the domain of AC charging, typically designated as Level 1 or Level 2 charging. DC charging, on the other hand, is employed for off-board chargers, specifically classified as Level 3 charging. Off-board DC fast chargers are directly linked to the EV battery through BMS, bypassing the on-board charger as shown in Figure 1.1

Due to various contributing factors, there is an increasing focus on the quality of the power that any electronic equipment absorbs from the utility grid. In the case of most of the mains-connected power electronic systems, in order to convert the grid's AC voltage to the DC voltage needed for electronics, a rectification is required. The EV charger also has an AC/DC converter to establish the required DC link voltage for the subsequent DC/DC converter to function. Conventionally the rectification is done using a diode bridge rectifier with an output capacitor. Due to the non-sinusoidal nature of the line current drawn in the conventional rectification, there is very high harmonic content in the AC line current which leads to adverse effects on the grid. Some of the undesirable effects on the grid are grid voltage distortion, efficiency reduction, the requirement for higher current rating for connection to the grid, and damage to connected electronic equipment due to harmonics [3]. Countries around the globe are implementing strict regulations to restrict the level of harmonic distortion produced by electronic devices connected to the power grid. This is being achieved through the establishment of international standards for harmonics like IEC-61000-3-2, IEC-61000-3-12 [4]. In order to meet the standards, to improve the power factor, and also to regulate the DC link voltage in the AC/DC converter, Power Factor Correction (PFC) circuits are employed.

Power Factor (PF) is an important measure in electrical device design because it represents the ratio of energy a device can supply at its output to the total energy it absorbs from the input power source. It relates the active power (P) and the apparent power (S) as shown in the Equation (1.1) [3].

$$PF = \frac{P}{S} = \frac{V_{1,rms} \cdot I_{1,rms} \cdot \cos(\phi)}{V_{rms} \cdot I_{rms}} \tag{1.1}$$

If the input voltage is taken to be ideally sinusoidal without any harmonics, then the RMS of the input voltage can be taken equal to the RMS of the first harmonics ($V_{rms} = V_{1,rms}$). The equation for PF can be made simpler to the product of two terms: displacement power factor (k_{DPF}) and distortion power factor (k_D).

$$k_{DPF} = \cos(\phi) \quad ; \quad k_D = \frac{I_{1,rms}}{I_{rms}} \tag{1.2}$$

The phase difference between the fundamental voltage and current is described by k_{DPF}, whereas k_D accounts for the current harmonics present in the input RMS current (I_{rms}). k_D is related to the Total Harmonic Distortion (THD) which is the amount of distortion present in the line current by the following relation.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_{1,rms}} \rightarrow k_D = \frac{1}{\sqrt{1 + (THD)^2}} \tag{1.3}$$

Thus the PF can be expressed in terms of THD and k_{DPF} as in Equation (1.4) [3].

$$PF = k_D \cdot k_{DPF} = \frac{1}{\sqrt{1+(THD)^2}} \cdot \cos(\phi) \tag{1.4}$$

The ideal situation for any electric system is achieved when the power factor is unity. This is when the input current does not have any harmonics ($THD = 0$) and is in phase with the input voltage ($(\phi = 0)$ or $\cos(\phi) = 1$). As the unity power factor is not achieved in practical situations, PFC circuits are implemented to achieve a power factor higher than 0.99.

Power factor correction (PFC) can be accomplished using passive or active approaches. In passive PFC, inductance is added between the diode bridge and the DC link capacitor before the DC/DC stage. Although this method is simple and inexpensive, its effectiveness is limited, and maintaining acceptable PFC performance across a wide operating range (such as 85 V RMS to 265 V RMS) can be difficult [5].

On the other hand, active PFC employs a PWM converter between the diode bridge and the isolated DC/DC converter. Even though this method is more complicated, it provides better power factor performance with minimum degradation across a wide operating range. Various converter topologies have been used over the years for active PFC, each with its own set of advantages and disadvantages. The boost converter is the most extensively used topology for active power factor correction today (Figure 1.2)[5]. Boost converters are most commonly used because the input is connected to the power supply continuously via the inductor (L_b). This means that the current does not experience significant di/dt, allowing the input current to be readily shaped by controlling the switching device (S_b) and obtaining low THD [6].

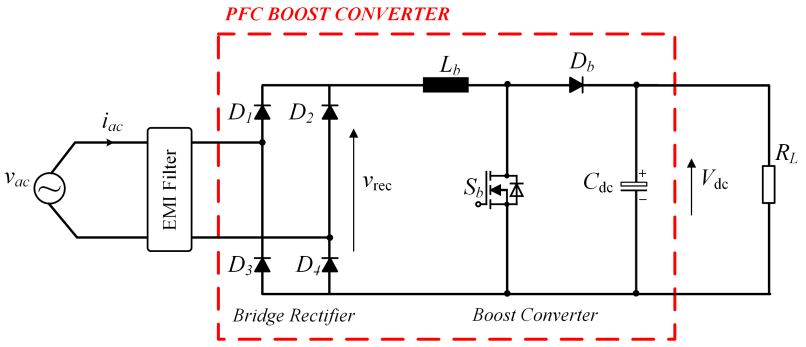


Figure 1.2: AC-DC rectification using single-phase boost PFC converter.

Recently, with the widespread adoption of PFC converters in applications like EVs and heating, ventilation, and air conditioning (HVAC) systems, there has been an increased demand for higher power capabilities. Operating a conventional single-switch PFC at higher power levels can potentially reduce its efficiency. This has led to the implementation of interleaving techniques to maintain efficiency during high-power operations. One of the main advantages of an interleaved configuration is its ability to achieve acceptable efficiency across a wide range of output power through phase-shedding control. However, the design and optimization of EMI filters under such operating conditions have not been

fully explored.

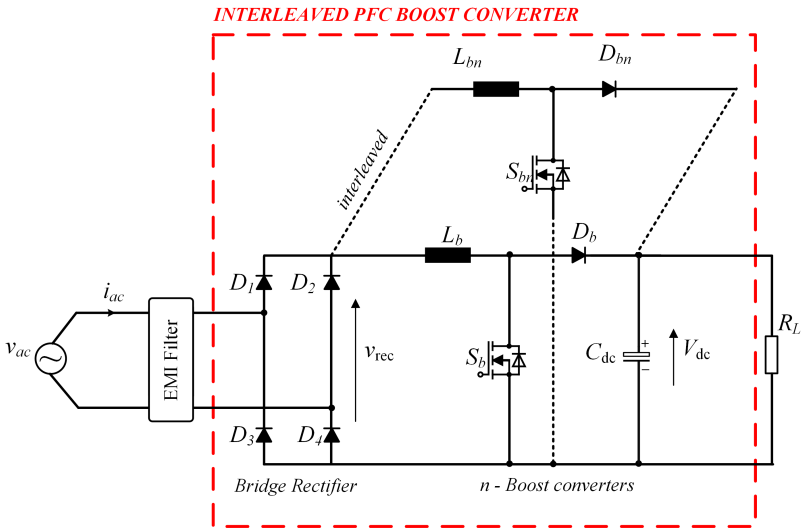


Figure 1.3: AC-DC rectification using n-channel interleaved PFC boost converter.

1.2 Influencing factors on PFC converter performance

A PFC converter (Single-phase with a single-switch boost topology) can be operated in various modes. Traditionally, Continuous Conduction Mode (CCM) was favored for PFC converters because it required less effort in designing EMI filters. However, due to the ongoing need to increase system power density and limitations in the operating speed of Silicon (Si) power switches, these converters have been pushed towards operating in Discontinuous Conduction Mode (DCM). While DCM operation can lead to a smaller boost inductor size and lower control complexity, it demands more effort in designing the EMI filter. Also, QCM which stands for quasi-continuous conduction mode, describes a current waveform that encompasses intervals operating in both DCM and CCM. The inductor current ripple undergoes a gradual change as it shifts from pure DCM to CCM. Even if a PFC converter is designed to primarily operate in CCM, under conditions of low line input voltages or low output power levels, the inductor current tends to transition towards DCM near zero crossings of the line voltage. This shift from CCM to DCM occurs when the output power level decreases, and it is guided by the QCM mode of operation. Operating the boost inductor in this mode allows for the advantages of both current modes mentioned earlier to be combined. The critical conduction mode or Boundary Conduction Mode (BCM) in which the switching frequency is not fixed is not discussed in this study [7].

It's worth noting that the high switching capability of the new Wide-Band Gap (WBG) power devices allows for the possibility of reverting back to CCM mode for PFC systems while still reducing the size of the boost inductor. In this project, the SiC MOSFET Module SK45MLET12SCp from SEMIKRON is evaluated. It has three separated boost legs in a very compact solution making it an ideal choice for implementing interleaved PFC.

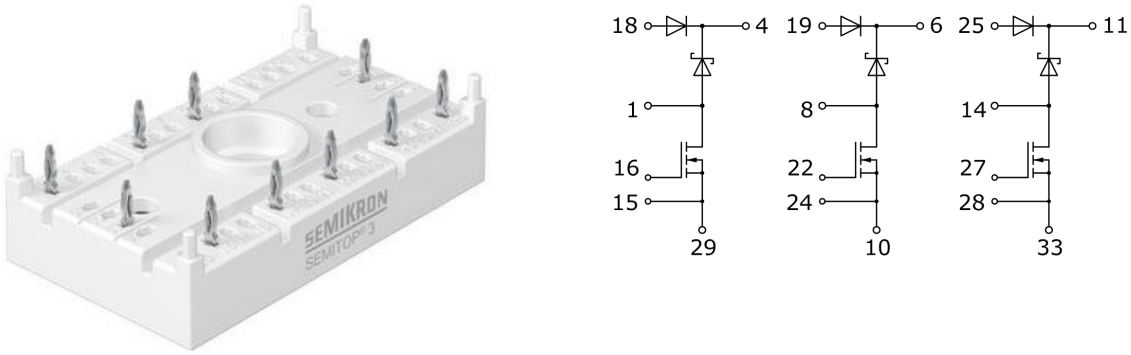


Figure 1.4: SiC MOSFET Module from Semikron.

Although these devices can significantly increase the power density of the converter, they may not always be the ultimate solution due to various application requirements, such as cost-effectiveness. The other influencing factors like maintaining efficiency using phase shedding, choosing proper semiconductor technology, the complexity of control, size of the components, varying of switching frequency, and the optimal number of EMI input filters all play crucial roles in optimising a PFC rectifier.

1.3 Scope of the project

The aim of this project is to assess various factors that impact the performance of the PFC rectifier, with the aim of optimising its power density. Additionally, the project will explore the impact of QCM current operation, in conjunction with the established CCM and DCM modes. There will also be an emphasis on devising an intelligent control system that selects appropriate modulation methods based on prevailing output power conditions. Furthermore, due to the continual growth in power capability requirement, the benefits of interleaving parallel boost cells will be examined. This project will benefit from SiC MOSFET Module SK45MLET12SCp from SEMIKRON, which integrates three interleaved boost cells in the same package, seeking to maximise power density.

1.3.1 Problem statement

Analyzing the impact of current modulation, interleaving, switching frequency, phase shedding, phase shifting as well as optimisation of the boost inductor and EMI filter on the design of a single-phase PFC boost converter, with the aim of attaining high performance and power density.

1.3.2 Objective

- Magnetic component sizing and design considering different current modulation techniques and different magnetic materials.
- EMI filter design and sizing considering single-switch and interleaved topologies based on CISPR 11 standards.
- Optimising converter performance with respect to utilized modulation techniques, component sizing, EMI performance, efficiency, and switching frequency.
- Practical implementation and measurement of SiC-based, 7 kW single phase interleaved PFC converter.

1.4 Specification

The normal household single phase supply has outlets with a maximum rated power of 7360 W with I_{rms} = 32 A and V_{rms} = 230 V. The specification of the PFC boost converter is finalised considering designing for the application of an onboard charger with a maximum output power rating of 7360 W.

Parameter	Notation	Value
Nominal input RMS voltage	$V_{in,rms}$	230 V AC
AC line input frequency	f_{line}	50 Hz
Switching frequency	f_{sw}	20 - 30 kHz
Nominal output voltage	V_o	400 V DC
Output power range	P_o	1000 - 7360 W
Nominal output current	I_o	18.4 A
Nominal input current	$I_{in,rms}$	32 A
Maximum voltage ripple	$\Delta V_{o,pk-pk}$	10 V
Hold-up time	t_{hold}	16.6 ms @ $V_o = 340$ V
Power factor at rated power	PF	>0.99

Table 1.1: Specifications of 7.36 kW PFC interleaved converter.

1.5 Outline of the thesis

The organisation of the thesis is as follows.

- **Chapter 2** focuses on the design of the interleaved boost converter. The passive component values are designed for three current conduction modulation techniques. The current controller and voltage controller are designed and finally, the designed parameters are verified with simulation.
- **Chapter 3** offers a comprehensive exploration of inductor design, encompassing an examination of various core types and a determination of the core that minimizes volume while meeting specified design criteria. Additionally, the chapter delves into the simulation of the steady-state behavior of a PFC converter using MATLAB scripts.
- **Chapter 4** firstly introduces the differential-mode EMI filter design based on EMI noise simulations. The second part of the chapter discusses the loss modeling of various components in the PFC converter.
- **Chapter 5** is about assessing and enhancing the overall performance of the interleaved PFC converter by performing additional theoretical and simulation analyses. Optimisation of the three-stage interleaved PFC is pursued with the aim of improving power density, efficiency, and EMI performance.
- **Chapter 6** pertains to the hardware design of a single-phase three-stage interleaved PFC boost converter. It covers the sizing of components, selected devices, and PCB design of the converter. The chapter concludes with discussions on the hardware test results and validation of the simulation results.

- In **Chapter 7** the conclusions of the project work are provided along with recommendations for potential avenues of future research.

Chapter 2
Design of Interleaved PFC Boost Converter

In this chapter, the design of the 3-stage interleaved boost converter in CCM, DCM and QCM is carried out. It involves determining the values of passive components (boost inductance and output capacitor). The mathematical model of the system under study is obtained and the procedure for current and voltage controller design is discussed. Finally, the validity of the designed parameters is confirmed through closed loop simulation.

2.1 Interleaved PFC boost converter

A Single phase three stage interleaved PFC boost converter is shown in the Figure 2.1. The three interleaved stages share the input current. This sharing of input current helps reduce the size and rating of individual devices in the interleaved stages when compared to the non-interleaved case. The three stages are controlled with PWM signals conventionally with a phase shift of 120°. This phase shifting helps in input current ripple cancellation. The input current ripple cancellation effect for n = 1,2,3,4 interleaved stages operating in CCM is shown in Figure 2.2 with the help of the plot of normalized input current ripple K_{cr} as a function of duty cycle. K_{cr} is the factor obtained by dividing the net ripple produced by interleaving n channels with the amplitude of the single channel ripple ($\Delta I_L / \Delta I_{L1}$) [8].

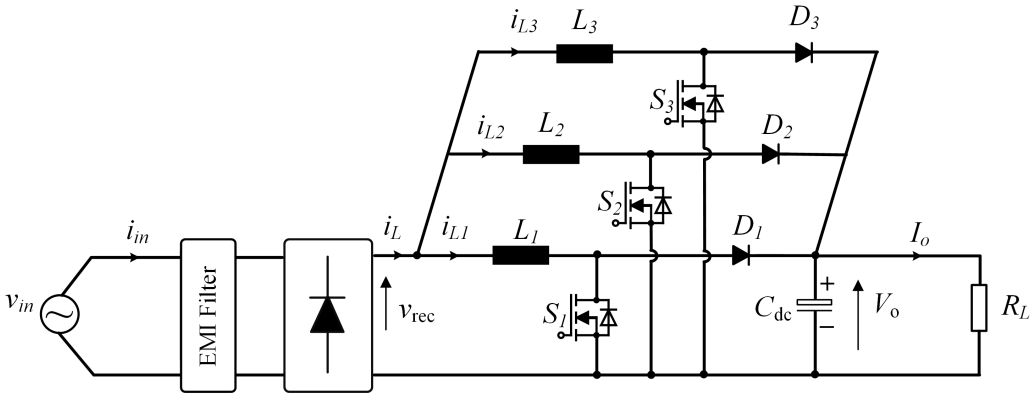


Figure 2.1: Single phase Three stage interleaved PFC boost converter diagram.

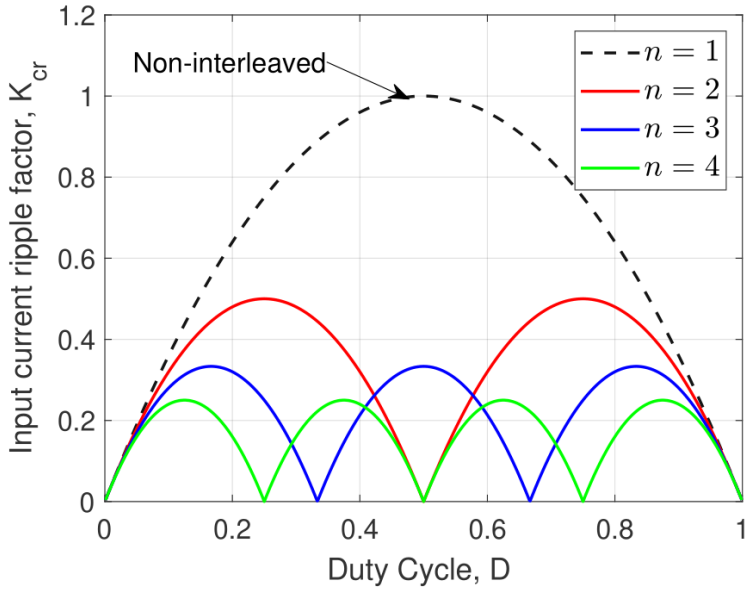


Figure 2.2: Normalized input current ripple K_{cr} as a function of duty cycle for n = 1,2,3,4 interleaved stages operating in CCM [7, 8].

2.2 Boost inductor design

One of the two main passive components of the PFC boost converter is the boost inductor and the other is the output capacitor. The performance of the PFC converter is dependent on these components. The design of the boost inductor is dependent on various factors like the current conduction mode (CCM, DCM, or QCM), switching frequency, input voltage range, output voltage, maximum inductor current ripple, and other factors [7].

The specification of the converter in Table 1.1 is used to calculate the parameters required for the calculation of boost inductance. For an output power of P_o = 7.36 kW, an output voltage of V_o = 400 V, an input line RMS voltage of $V_{in,rms}$ = 230 V, and considering an efficiency η of 100 %, the input current RMS $I_{in,rms}$ is calculated as

$$I_{in,rms} = \frac{P_o}{\eta \cdot V_{in,rms}} = 32\,\text{A} \tag{2.1}$$

Also from the RMS values of the input voltage and current, the peak values are calculated to be $V_{in,pk}$ = 325.27 V and $I_{in,pk}$ = 45.25 A.

2.2.1 Design for CCM operation

In CCM operation the inductor current does not fall to zero throughout the switching cycle as shown in the Figure 2.3. The design is based on the percentage ripple factor k_{ripple} which relates the average inductor current $i_{L,avg}$ to the peak-to-peak inductor current $\Delta i_{L,\text{max}}$ at a specific point, given as Equation (2.2). The choice of the ripple factor (k_{ripple}) in theory, has to be carefully chosen for CCM operation because it will affect the power losses, the requirement for the EMI filter, and the volume of the boost inductance [9, 10].

$$\Delta i_{L,\text{max}} = k_{\text{ripple}} \cdot i_{L,avg} \tag{2.2}$$

In the design, the specific point at which k_{ripple} is defined is taken as the point where the maximum ripple current occurs, which is at a duty cycle of 0.5. The output-input voltage relation of a boost converter is used to get the $V_{\text{in},0.5}$ when the duty ratio (D) is 0.5,

$$\frac{V_o}{V_{\text{in}}} = \frac{1}{1-D} \quad \rightarrow \quad V_{\text{in},0.5} = \frac{V_o}{2} \tag{2.3}$$

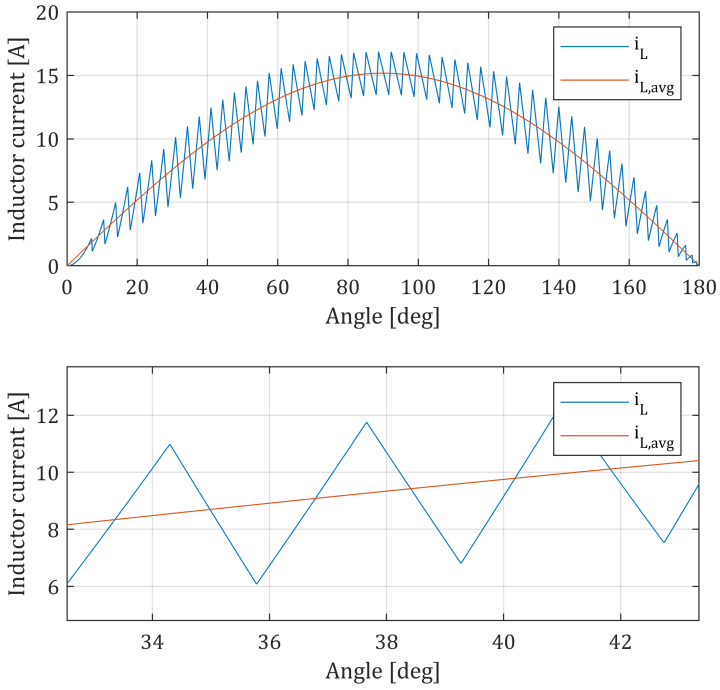


Figure 2.3: Top: The inductor current and its average in CCM.
Bottom: Zoomed in view at angle $\theta = 38°$.

Now the angle at which V_{in} is equal to $V_{\text{in},0.5}$ can be found by substituting the Equation (2.3) in the equation for line input voltage, $V_{in} = V_{in,pk} \cdot \sin(\theta)$. For V_o= 400 V and $V_{in,pk}$ = 325.27 V, the resulting angle θ_d is found to be 38° from Equation (2.4).

$$\theta_d = sin^{-1}\left(\frac{V_o}{2 \cdot V_{in,pk}}\right) \tag{2.4}$$

In an interleaved PFC boost converter, the rectified input current is divided among each interleaved boost inductor. Therefore, the average current in each inductor is divided by the number of interleaving stages (n_{stage}).

$$i_{L,avg} = \frac{|i_{in}|}{n_{stage}} = \frac{\left|I_{in,pk} \cdot \sin(\theta)\right|}{n_{stage}} \tag{2.5}$$

Substituting θ_d from Equation (2.4) in Equation (2.5) the average inductor current at D = 0.5 can be calculated as,

$$i_{L,avg,0.5} = \frac{I_{in,pk} \cdot V_o}{2 \cdot V_{in,pk} \cdot n_{stage}} \tag{2.6}$$

This calculated $i_{L,avg,0.5}$ can be used in the Equation (2.2) to get the $\Delta i_{L,max,CCM}$ for a chosen value of k_{ripple}.

$$\Delta i_{L,\mathrm{max},CCM} = \frac{k_{ripple} \cdot I_{in,pk} \cdot V_o}{2 \cdot V_{in,pk} \cdot n_{stage}} \tag{2.7}$$

Now when the power switch in the boost converter is conducting, the line voltage is applied across the inductor for a time period of $D \cdot T_{sw}$, where T_{sw} is the switching time period (inverse of the switching frequency, f_{sw}). Thus substituting $v_L = V_{\mathrm{in},0.5}$, $di_L = \Delta i_{L,\mathrm{max},CCM}$ and $dt = D \cdot T_{sw}$ in the fundamental voltage equation of an inductor as shown in Equation (2.8).

$$v_L = L \cdot \frac{di_L}{dt} \tag{2.8}$$

we get the minimum value of inductance that can keep the PFC in CCM as given by Equation (2.9).

$$L_{CCM} \geqslant \frac{V_o}{4 \cdot \Delta i_{L,max,CCM} \cdot f_{sw}} \tag{2.9}$$

The generalized formula for CCM of an interleaved PFC boost converter with k_{ripple} defined at duty ratio of 0.5 is derived by substituting Equation (2.7) in Equation (2.9) and is given by Equation (2.10).

$$L_{CCM} \geqslant \frac{V_{in,pk} \cdot n_{stage}}{2 \cdot I_{in,pk} \cdot f_{sw} \cdot k_{ripple}} \tag{2.10}$$

2.2.2 Design for DCM operation

In the case of DCM, the inductor current always touches zero in every switching cycle as seen in the Figure 2.4:Top. The current will remain at zero during some part of the switching cycle as seen in the Figure 2.4:Bottom. It can be also seen in the Figure 2.4: Middle, that the current is in the boundary of switching to CCM at $\theta = 90^\circ$. At this instant, the Δi_L is twice the $i_{L,avg}$. In order to maintain the PFC in DCM and prevent it from transitioning into CCM, the design of the inductance is based on this boundary. The boundary at which DCM shifts to CCM is denoted as angle α in this work. At $\theta = \alpha = 90^\circ$ the duty cycle D is calculated as,

$$\frac{V_o}{V_{\mathrm{in}}} = \frac{1}{1-D} \quad \rightarrow \quad D = 1 - \frac{V_{\mathrm{in,pk}} \cdot \sin(90^\circ)}{V_o} \tag{2.11}$$

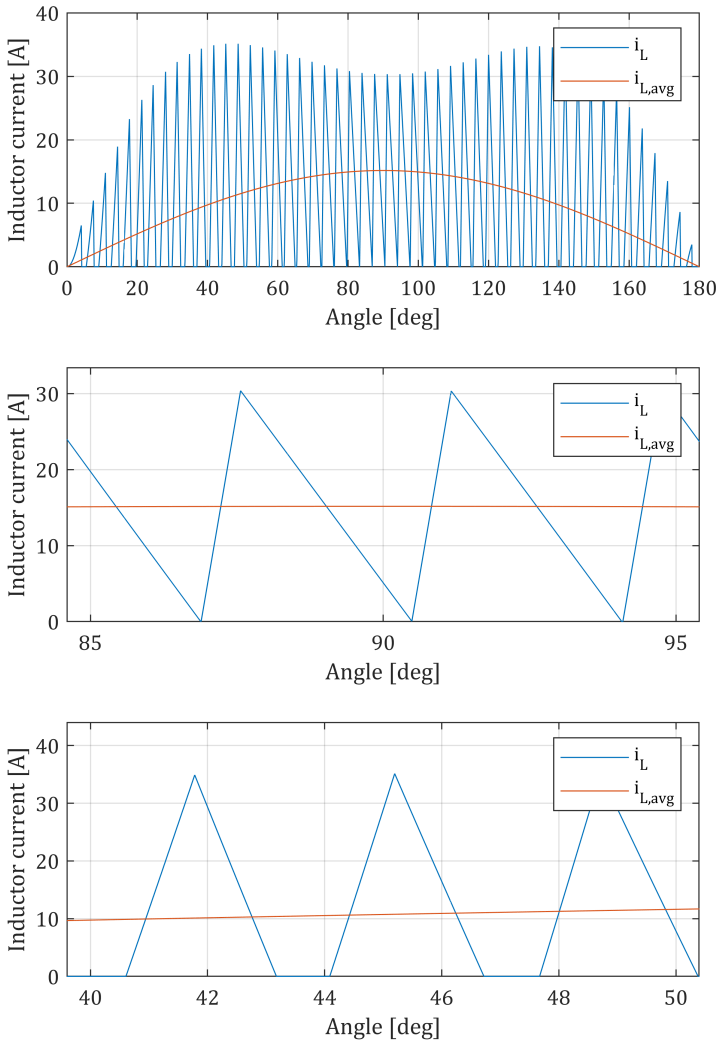


Figure 2.4: Top: The inductor current and its average in DCM.
Middle: Zoomed in view around angle $\theta = 90°$ which is the value of α.
Bottom: Zoomed in view around angle $\theta = 45°$ to show discontinuous operation.

The peak-to-peak inductor current at $\theta = 90°$ is given by,

$$\Delta i_{L,DCM} = \frac{2 \cdot I_{in,pk}}{n_{stage}} \tag{2.12}$$

When the power switch in the boost converter is conducting around $\theta = 90°$, the line voltage, $V_{\text{in,90}} = V_{\text{in,pk}} \cdot \sin(90°)$ is applied across the inductor for a time period of $D \cdot T_{sw}$. Thus substituting $v_L = V_{\text{in,90}}$, $di_L = \Delta i_L$ and $dt = D \cdot T_{sw}$ in Equation (2.8), the inductance is calculated as in Equation (2.13).

$$L_{DCM} = \frac{V_{in,pk} \cdot n_{stage} \left(1 - \frac{V_{\text{in,pk}} \cdot \sin(90°)}{V_o}\right)}{2 \cdot I_{in,pk} \cdot f_{sw}} \tag{2.13}$$

2.2.3 Design for QCM operation

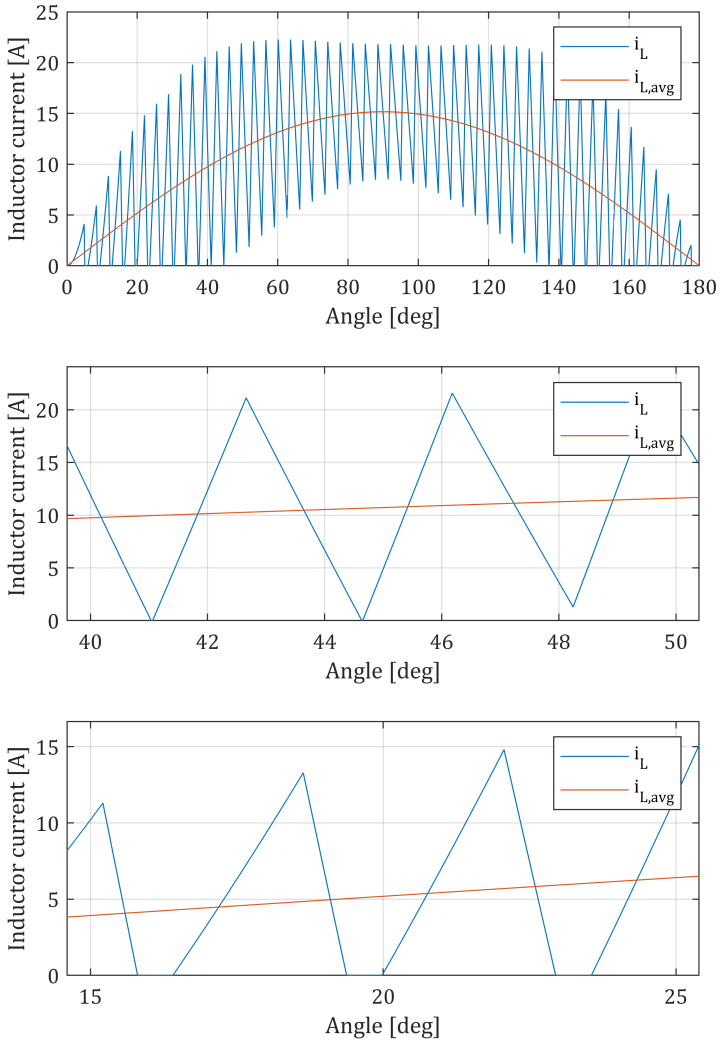


Figure 2.5: Top: The inductor current and its average in QCM.
Middle: Zoomed in view around angle $\theta = 45°$ which is the value of α.
Bottom: Zoomed in view around angle $\theta = 20°$ to show discontinuous operation.

Quasi-continuous Conduction Mode is when the boost converter conducts in DCM for the switching cycles till a defined angle α (as shown in Figure 2.5 where $\alpha = 45°$) and then conducts in CCM. It is a mixed conduction mode and combines the benefits of both CCM and DCM. The angle at which the conduction mode changes from DCM to CCM which is denoted as α is a design parameter for the inductance.
At $\theta = \alpha$ the duty cycle D is calculated as,

$$\frac{V_o}{V_{\text{in}}} = \frac{1}{1-D} \quad \rightarrow \quad D = 1 - \frac{V_{\text{in,pk}} \cdot \sin(\alpha)}{V_o} \tag{2.14}$$

The peak-to-peak inductor current at $\theta = \alpha$ is twice the average inductor current at that

point and is given by,

$$\Delta i_{L,QCM} = \frac{2 \cdot I_{in,pk} \cdot \sin(\alpha)}{n_{stage}} \tag{2.15}$$

When the power switch in the boost converter is conducting around $\theta = \alpha$, the line voltage, $V_{\text{in},\alpha} = V_{\text{in,pk}} \cdot \sin(\alpha)$ is applied across the inductor for a time period of $D \cdot T_{sw}$. Thus substituting $v_L = V_{\text{in},\alpha}$, $di_L = \Delta i_{L,QCM}$ and $dt = D \cdot T_{sw}$ in Equation (2.8), the inductance is calculated as in Equation (2.16).

$$L_{QCM} = \frac{V_{in,pk} \cdot n_{stage} \left(1 - \frac{V_{\text{in,pk}} \cdot \sin(\alpha)}{V_o}\right)}{2 \cdot I_{in,pk} \cdot f_{sw}} \tag{2.16}$$

2.2.4 Summary of Inductance Design

The summary of design equations for the boost inductance in the interleaved PFC converter is given in Table 2.1. The Design Point (DP) is the point where the peak-to-peak inductor current is designed. It can be seen that different values of inductance can be obtained for CCM at a design point of $D = 0.5$ by varying the value of k_{ripple}. In the case of QCM, different inductance values can be obtained by varying the boundary angle (α) at which the conduction mode switches from DCM to CCM. DCM is obtained when the angle α is set to 90°. It is observed that for all the conduction modes the peak-to-peak inductor current ripple is inversely proportional to the number of stages of interleaving (n_{stage}). This also impacts the value of the inductance, as the inductance value is proportional to n_{stage}.

Mode	**CCM**	**QCM (for DCM, $\alpha = 90°$)**
Design Point (DP)	$D = 0.5$	α
Boundary angle from DCM to CCM (α)	0°	α
Ripple factor (k_{ripple})	k_{ripple}	2
Angle at DP (θ_{DP})	$\sin^{-1}\left(\frac{V_o}{2 \cdot V_{in,pk}}\right)$	α
Inductor voltage at DP ($v_{L,DP} = V_{in,pk} \cdot \sin(\theta_{DP})$)	$\frac{V_o}{2}$	$V_{in,pk} \cdot \sin(\alpha)$
Duty cycle at DP ($D_{DP} = 1 - \frac{V_{in,pk} \cdot \sin(\theta_{DP})}{V_o}$)	0.5	$1 - \frac{V_{in,pk} \cdot \sin(\alpha)}{V_o}$
Peak-to-peak inductor current at DP ($\Delta i_{L,DP} = \frac{k_{ripple} \cdot I_{in,pk} \cdot \sin(\theta_{DP})}{n_{stage}}$)	$\frac{k_{ripple} \cdot I_{in,pk} \cdot V_o}{2 \cdot V_{in,pk} \cdot n_{stage}}$	$\frac{2 \cdot I_{in,pk} \cdot \sin(\alpha)}{n_{stage}}$
Inductance value ($L = \frac{v_{L,DP} \cdot D_{DP}}{\Delta i_{L,DP} \cdot f_{sw}}$)	$\frac{V_{in,pk} \cdot n_{stage}}{2 \cdot I_{in,pk} \cdot f_{sw} \cdot k_{ripple}}$	$\frac{V_{in,pk} \cdot n_{stage}\left(1 - \frac{V_{\text{in,pk}} \cdot \sin(\alpha)}{V_o}\right)}{2 \cdot I_{in,pk} \cdot f_{sw}}$

Table 2.1: Summary of design equations for boost inductance of interleaved PFC converter.

2.3 Output capacitor design

On the basis of the specifications in Table 1.1, the output bulk capacitor, C_{dc} in Figure 2.1 is sized in this section. Design specifications include the hold-up time (t_{hold}) and output voltage ripple (ΔV_o). Numerous technical notes [6, 11] demonstrate the derivation of t_{hold} beginning with the capacitor's energy equation. The instantaneous output voltage at the start of the line outage will be determined by the hold-up time, which is typically measured in milliseconds, and this will influence the requirements for the capacitor value. Maximum output capacitor value from Equations (2.17) and (2.18) is chosen as required the output capacitor value [7].

$$C_{dc} \geqslant \frac{2 \cdot P_o \cdot t_{\text{hold}}}{V_o^2 - V_{o.\,\text{min}}^2} \tag{2.17}$$

$$C_{dc} \geqslant \frac{P_o}{2 \cdot \pi \cdot f_{\text{line}} \cdot \Delta V_o \cdot V_o} \tag{2.18}$$

Here t_{hold} is the hold-up time (16.6 ms) and P_o is the rated output power (7.36 kW). V_o is the output DC voltage (400 V), ΔV_o is the maximum permitted output voltage ripple (10 V), and $V_{o,min}$ is the minimum output voltage (340 V). f_{line} is the fundamental grid frequency (50 Hz). These parameters are substituted in Equations (2.17) and (2.18) and the maximum value from them is selected.

$$C_{dc} = \max(5.5\,\text{mF}, 5.86\,\text{mF}) \quad \rightarrow \quad C_{dc} = 5.86\,\text{mF} \tag{2.19}$$

2.4 Small-signal model of the boost converter

The Small-Signal Model (SSM) of a converter is typically derived using state-space averaging. The SSM provides a time-invariant representation under specific operating conditions, simplifying the controller design [3]. It is still possible to estimate the controller's parameters using the SSM even while the input to the PFC boost converter varies sinusoidally. This is possible because the converter operates with a slowly shifting operating point, resulting in only minor variations in electrical variables within one switching period, owing to the fact that the switching frequency (f_{sw}) is higher than the line frequency (f_{line}) [7, 12]. In interleaved PFC converters, each channel has an independent control due to the presence of a switching device in each channel. Consequently, an individual controller is employed for each channel, and only the SSM of a single boost converter is necessary for controller design. Equation (2.20) presents the general expression for the state-space equations, where $x(t) = \begin{bmatrix} i_L(t) & v_C(t) \end{bmatrix}^T$ are the state variables, $y(t)$ is the output signal and $u(t)$ is the input signal.

$$\begin{aligned} K \cdot \dot{x}(t) &= A \cdot x(t) + B \cdot u(t) \\ y(t) &= C \cdot x(t) + E \cdot u(t) \end{aligned} \tag{2.20}$$

The schematic diagram in Figure 2.6 represents an ideal non-synchronous boost converter. In this analysis, the power switch and diode are taken to be ideal, neglecting any parasitic components to simplify the analysis. The converter operates in two modes under CCM: Mode 1 when the switch S conducts, and Mode 2 when the diode D conducts current. These modes are illustrated in Figures 2.7a and 2.7b, respectively.

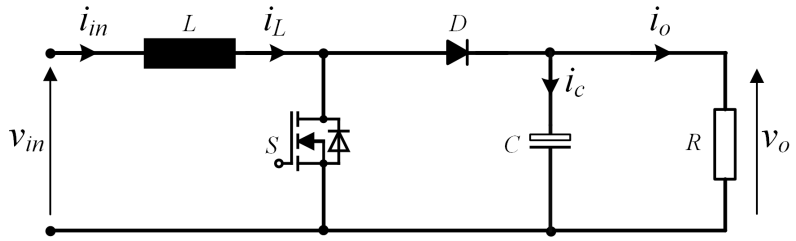
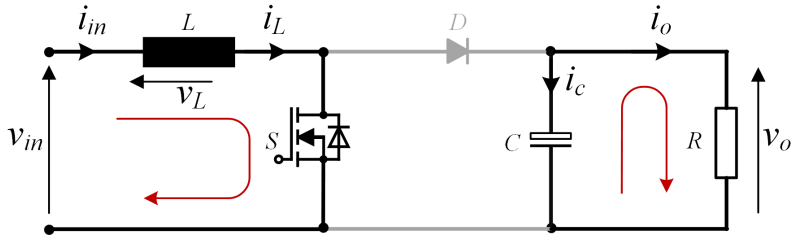
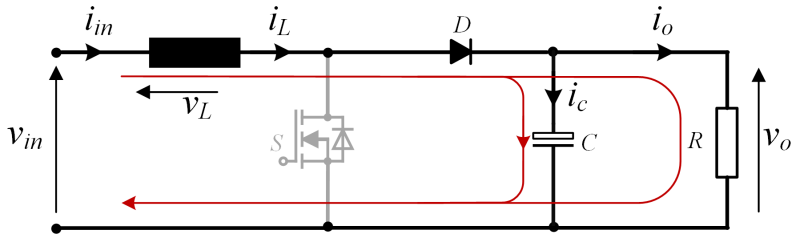


Figure 2.6: Electrical circuit diagram of an ideal non-synchronous boost converter.



(a) Mode 1, Switch S is conducting current.



(b) Mode 2, Diode D is conducting current.

Figure 2.7: Different modes of operation in CCM of a Boost converter.

By examining the circuits, it is possible to derive the state equations for each mode of operation from the formulae for inductor voltage and capacitor current provided in Equation (2.21).

$$v_L(t) = L \cdot \frac{di_L(t)}{dt} \quad ; \quad i_c(t) = C \cdot \frac{dv_c(t)}{dt} \tag{2.21}$$

The state equation for Mode 1 is as shown in Equation (2.22)

$$\underbrace{\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}}_{K} \cdot \frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & -1/R \end{bmatrix}}_{A_1} \cdot \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 1 \\ 0 \end{bmatrix}}_{B_1} \cdot [v_{in}(t)] \tag{2.22}$$

The state equation for Mode 2 is as shown in Equation (2.23)

$$\underbrace{\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}}_{K} \cdot \frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & -1 \\ 1 & -1/R \end{bmatrix}}_{A_2} \cdot \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 1 \\ 0 \end{bmatrix}}_{B_2} \cdot [v_{in}(t)] \tag{2.23}$$

By performing an average of the state-space equations over a single switching period, the averaged state matrices A and B can be determined. The equilibrium operating point X

(where $x(t) = 0$) is represented in Equation (2.24). From this equation, the voltage and current gain ratios of the boost converter are derived as shown:

$$X = -A^{-1} \cdot B \cdot U \quad \rightarrow \quad \frac{V_o}{V_{\text{in}}} = \frac{1}{1-D} \quad ; \quad \frac{I_o}{I_{in}} = 1 - D \tag{2.24}$$

The small signal linear model is then achieved by imposing small AC perturbations around the equilibrium point. The SSM of a boost converter is calculated using the equation shown in Equation (2.25).

$$K \cdot \dot{\hat{x}}(t) = A \cdot \hat{x}(t) + B \cdot \hat{u}(t) + [(A_1 - A_2) \cdot X + (B_1 - B_2) \cdot U] \cdot \hat{d}(t) \tag{2.25}$$

The SSM of the boost converter is obtained in Equation (2.26) by substituting the state-space matrices in the previous calculation.[3, 7]

$$\begin{aligned} \hat{v}_L(t) &= L \cdot \frac{d\hat{i}_L(t)}{dt} = -D \cdot \hat{v}_o(t) + \hat{v}_{in}(t) + V_o \cdot \hat{d}(t) \\ \hat{i}_c(t) &= C \cdot \frac{d\hat{v}_c(t)}{dt} = (1-D) \cdot \hat{i}_L(t) - \frac{\hat{v}_o(t)}{R} + \hat{v}_{in}(t) - I_L \cdot \hat{d}(t) \end{aligned} \tag{2.26}$$

To derive the transfer functions (TF) necessary for controller design, the small signal model (SSM) is represented in the frequency domain. The control-to-output voltage transfer function, $G_{vd}(s)$, and the control-to-inductor current transfer function, $G_{id}(s)$, are obtained by setting $\hat{u}(s)$ = 0, as demonstrated in Equation (2.28).

$$x(\hat{s}) = (sI - A)^{-1} \cdot B \cdot u(\hat{s}) + (sI - A)^{-1} \cdot [(A_1 - A_2) \cdot X + (B_1 - B_2) \cdot U] \cdot d(\hat{s}) \tag{2.27}$$

$$G_{vd}(s) = \left.\frac{\hat{v}_o(s)}{\hat{d}(s)}\right|_{\hat{u}(s)=0} \quad ; \quad G_{id}(s) = \left.\frac{\hat{i_L}(s)}{\hat{d}(s)}\right|_{\hat{u}(s)=0} \tag{2.28}$$

For the design of current controller, $G_{id}(s)$ is used. Now for designing the voltage controller $G_{vi}(s)$ is obtained from Equation (2.28) by dividing.

$$G_{vi}(s) = \frac{\hat{v}_o(s)}{\hat{i_L}(s)} = \frac{G_{vd}(s)}{G_{id}(s)} \tag{2.29}$$

The obtained transfer functions after substituting $D^{'} = 1 - D$ are shown in Equation (2.30)

$$\begin{aligned} G_{vd}(s) &= \frac{D'V_o}{LC} \cdot \frac{1 - \frac{I_L \cdot L}{V_o D'} \cdot s}{s^2 + \frac{1}{RC} \cdot s + \frac{D'^2}{LC}} \\ G_{id}(s) &= \frac{V_o}{L} \cdot \frac{s + \frac{1}{RC} + \frac{I_L D'}{V_o C}}{s^2 + \frac{1}{RC} \cdot s + \frac{D'^2}{LC}} \\ G_{vi}(s) &= \frac{D'}{C} \cdot \frac{1 - \frac{I_L \cdot L}{V_o \cdot D'} \cdot s}{s + \frac{1}{RC} + \frac{I_L D'}{V_0 C}} \end{aligned} \tag{2.30}$$

2.5 Controller structure for interleaved PFC boost converter

A PFC controller's primary objectives are precise output voltage regulation and low line current distortion (high PF). Because of its excellent dynamic performance, resilience, and simplicity, Average Current Mode Control (ACMC) is one of the most often used control systems to accomplish this goal [7, 13]. The ACMC approach seeks to control the average inductor current in proportion to the rectified input voltage. As a result of this regulation, the line current will follow a sinusoidal pattern and remain in sync with the line voltage. Five feedback signals must be monitored in order to execute the cascaded digital controller. These include the inductor currents for three interleaved stages (i_{L1}, i_{L2} , i_{L3}), the output voltage (V_o), the AC line to neutral voltage (v_{ac}).

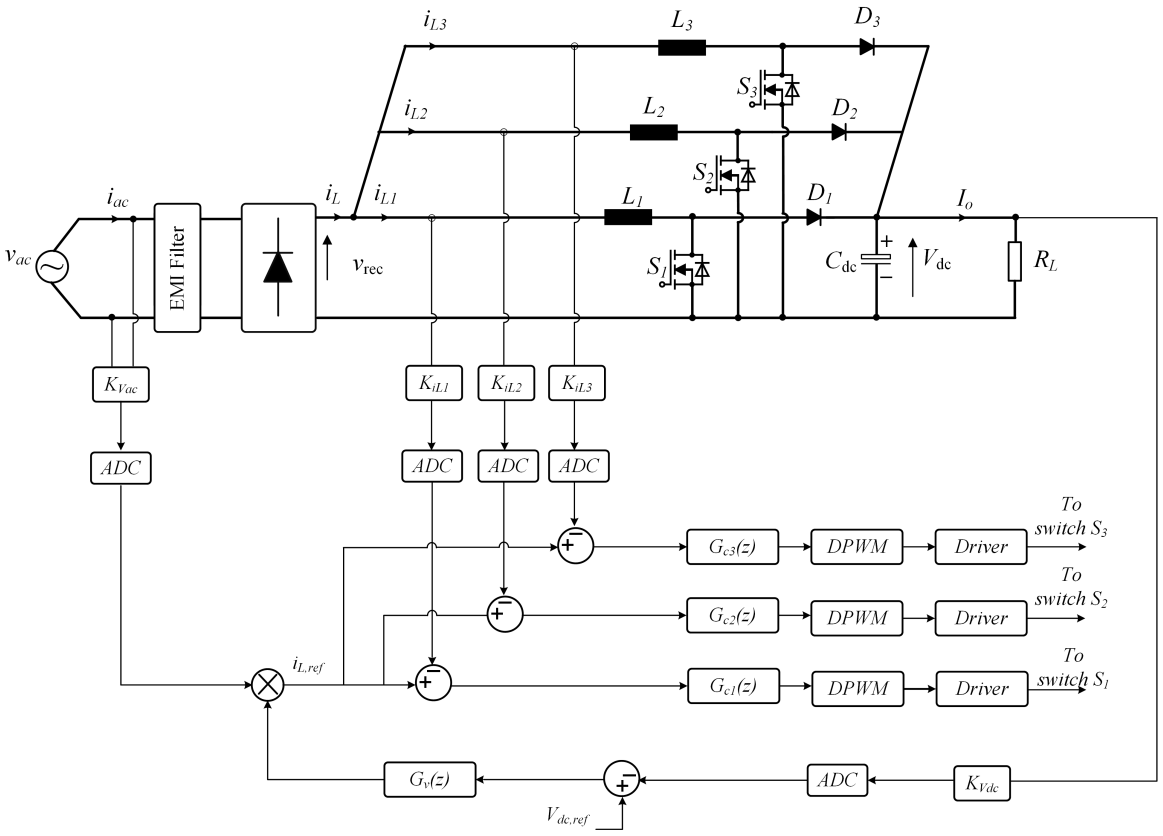


Figure 2.8: Controller diagram for three stages interleaved PFC boost converter.

There are three high bandwidth inner current control loops to regulate the input current and make it follow the same shape of the input AC voltage. The outer low bandwidth voltage control loop is to regulate the DC link voltage. The output voltage is sensed and compared with the reference value to generate the error which is passed to the outer voltage controller to generate the reference value for the inner current controllers. In order for the current in the inductor to follow the input voltage in phase, the reference value for the current controller is calculated by multiplying the output of the voltage control loop by the rectified sensed input voltage.

The current controller $G_{c1}(s)$ (same for all three stages) and voltage controller $G_v(s)$ are

designed after getting the bode plot of the open loop transfer function with the help of small signal transfer function and then applying frequency response analysis.

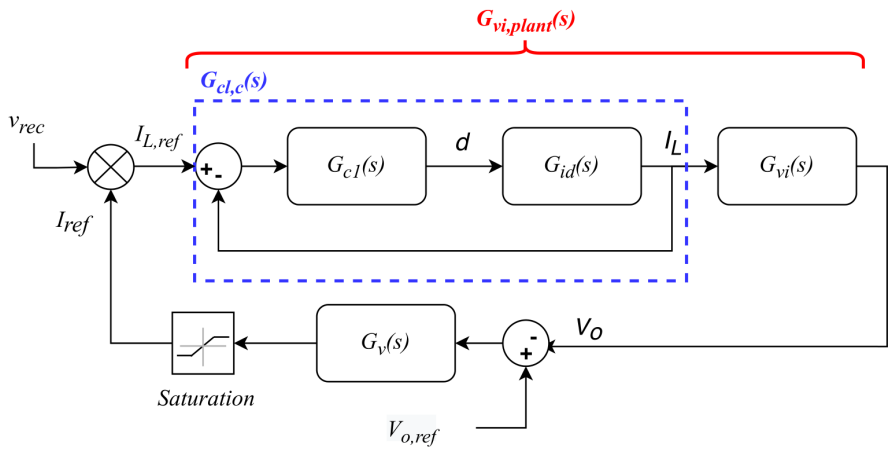


Figure 2.9: Block diagram of the cascaded controller showing the current and voltage loops [7].

2.6 Simulation results

In this section, initially, the PFC boost inductor is designed for CCM, QCM, and DCM with the help of Table 2.1, and then simulation results are presented to verify if the designed parameters are met.

Mode	CCM	QCM	DCM
Design Point (DP)	$D = 0.5$	$\alpha = 45°$	$\alpha = 90°$
Boundary angle from DCM to CCM (α)	0°	45°	90°
Ripple factor (k_{ripple})	0.4	2	2
Angle at DP (θ_{DP})	38°	45°	90°
Inductor voltage at DP $(v_{L,DP} = V_{in,pk} \cdot \sin(\theta_{DP}))$	200 V	230 V	325.27 V
Duty cycle at DP $\left(D_{DP} = 1 - \frac{V_{in,pk} \cdot \sin(\theta_{DP})}{V_o}\right)$	0.5	0.425	01868
Peak to peak inductor current at DP $\left(\Delta i_{L,DP} = \frac{k_{ripple} \cdot I_{in,pk} \cdot \sin(\theta_{DP})}{n_{stage}}\right)$	3.71 A	21.33 A	30.17A
Inductance value $\left(L = \frac{v_{L,DP} \cdot D_{DP}}{\Delta i_{L,DP} \cdot f_{sw}}\right)$	1348 μH	229 μH	100 μH

Table 2.2: Summary of designed parameters for boost inductance of interleaved PFC converter for P_o = 7360 W, V_o = 400 V, $V_{in,rms}$ = 230 V and F_{sw} = 20 kHz.

2.6.1 CCM operation

Simulation for CCM operation is conducted in PLECS for rated power conditions (Table 1.1) with the designed inductance, $L_{CCM} = 1348\ \mu H$ in (Table 2.2) and capacitance ($C_{dc} = 5.65\,\text{mF}$) for three stages interleaved PFC boost converter with a conventional phase shift of 120°. The results are as shown in Figure 2.10. The peak-to-peak inductor current ($\Delta i_{L,DP}$) at design point $D = 0.5$ is verified from the theoretical calculation in Table 2.2. $D = 0.5$ is the design point at which the value of the angular displacement θ is 38° and the corresponding time in the simulation is 1.0021 s. The $\Delta i_{L,DP}$ value in the Table 2.2) 3.71 A is matching closely to the $\Delta i_{L,DP}$ value in the simulation 3.76 A (calculated as 11.438 A - 7.678 A). The effect of interleaving (ripple cancellation) is seen in the plot for $i_{L,sum}$.

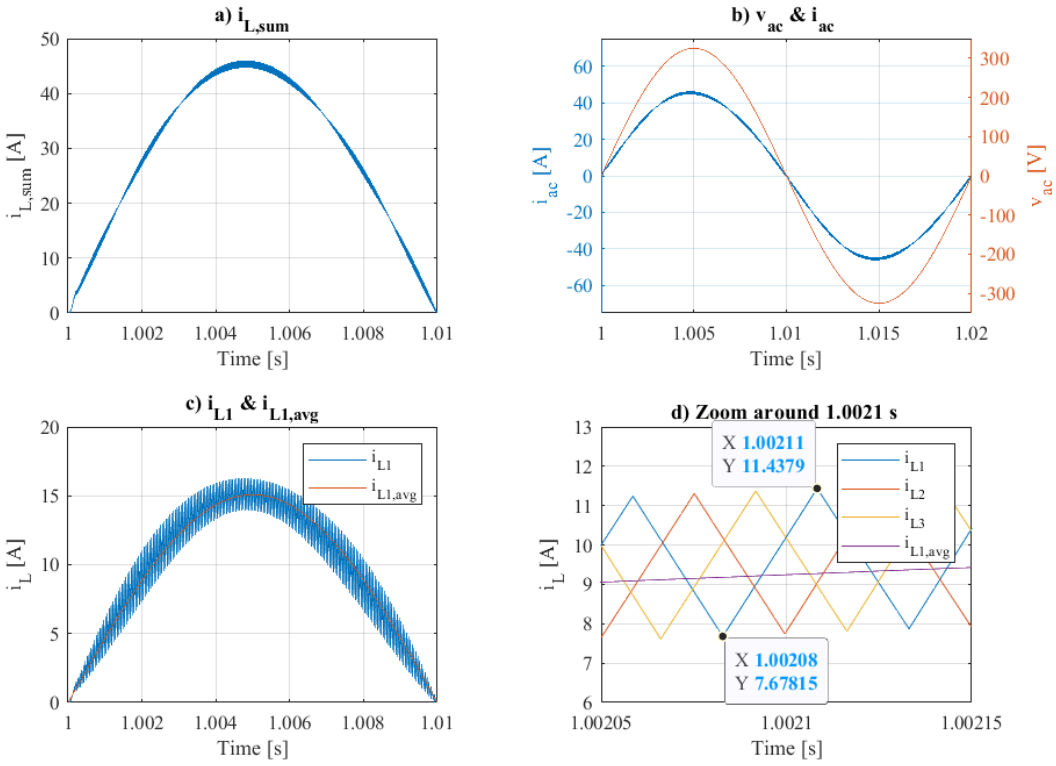


Figure 2.10: CCM operation waveforms with $L_{CCM} = 1348\ \mu H$ (a) Sum of inductor currents $i_{L,sum}$ =i_{L1} + i_{L2} +i_{L3}. (b) AC input voltage and AC input current waveform. (c) Inductor current i_{L1} for one half cycle. (d) Detailed view of all three inductor currents at $\theta = 38°$.

2.6.2 DCM operation

Simulation for QCM operation is conducted in PLECS for rated power conditions (Table 1.1) with the designed inductance, $L_{DCM} = 100\mu H$ in (Table 2.2) and capacitance ($C_{dc} = 5.65\,\text{mF}$) for three stages interleaved PFC boost converter with a conventional phase shift of 120°. The results are as shown in Figure 2.11. The peak-to-peak inductor current ($\Delta i_{L,DP}$) at design point $\alpha = 90°$ is verified from the theoretical calculation in Table 2.2. $\alpha = 45°$ is the design point at which the current changes from DCM to CCM and the corresponding time in the simulation is 1.005 s. The $\Delta i_{L,DP}$ value in the Table 2.2) 30.17 A is matching closely to the $\Delta i_{L,DP}$ value in the simulation 30.22 A. The effect of

interleaving (ripple cancellation) is seen in the plot for $i_{L,sum}$.

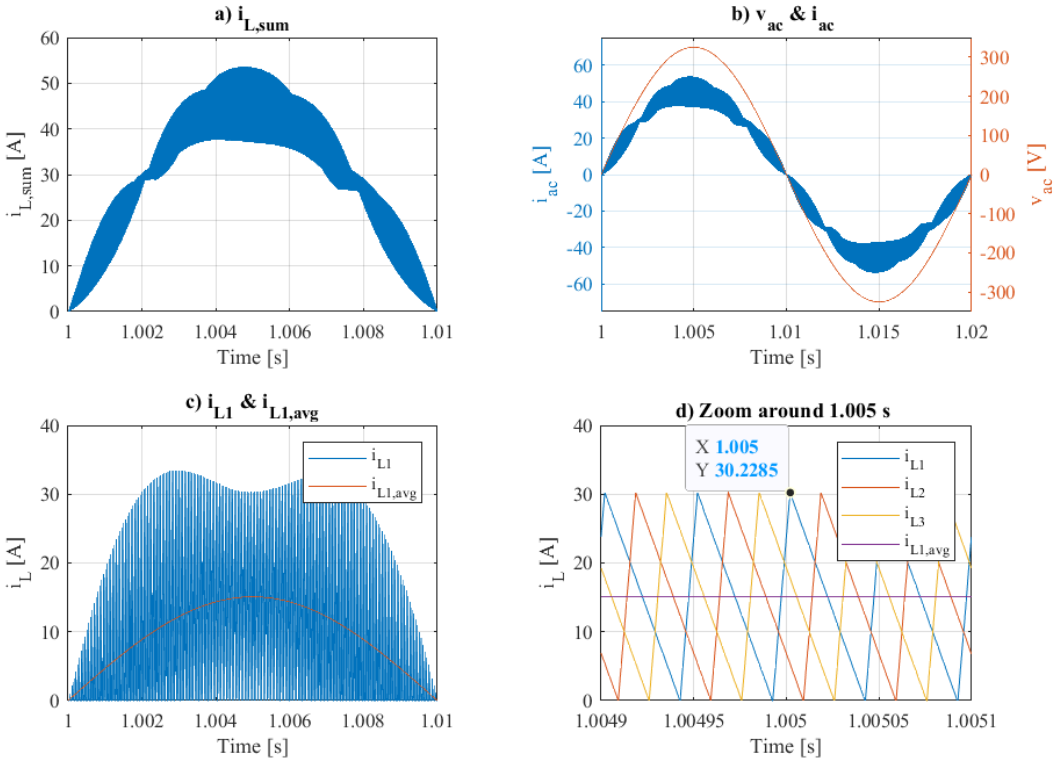


Figure 2.11: DCM operation waveforms with $L_{DCM} = 100\ \mu H$ (a) Sum of inductor currents $i_{L,sum}$ =i_{L1} + i_{L2} +i_{L3}. (b) AC input voltage and AC input current waveform. (c) Inductor current i_{L1} for one half cycle. (d) Detailed view of all three inductor currents at $\theta = 90°$.

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2.6.3 QCM operation

Simulation for QCM operation is conducted in PLECS for rated power conditions (Table 1.1) with the designed inductance, $L_{QCM} = 229\mu H$ in (Table 2.2) and capacitance ($C_{dc} = 5.65\,\text{mF}$) for three stage interleaved PFC boost converter with a conventional phase shift of 120°. The results are as shown in Figure 2.12. The peak-to-peak inductor current ($\Delta i_{L,DP}$) at design point $\alpha = 45°$ is verified from the theoretical calculation in Table 2.2. $\alpha = 45°$ is the design point at which the current changes from DCM to CCM and the corresponding time in the simulation is 1.0025 s. The $\Delta i_{L,DP}$ value in the Table 2.2) 21.33 A is matching closely to the $\Delta i_{L,DP}$ value in the simulation 21.305 A. The effect of interleaving (ripple cancellation) is seen in the plot for $i_{L,sum}$.

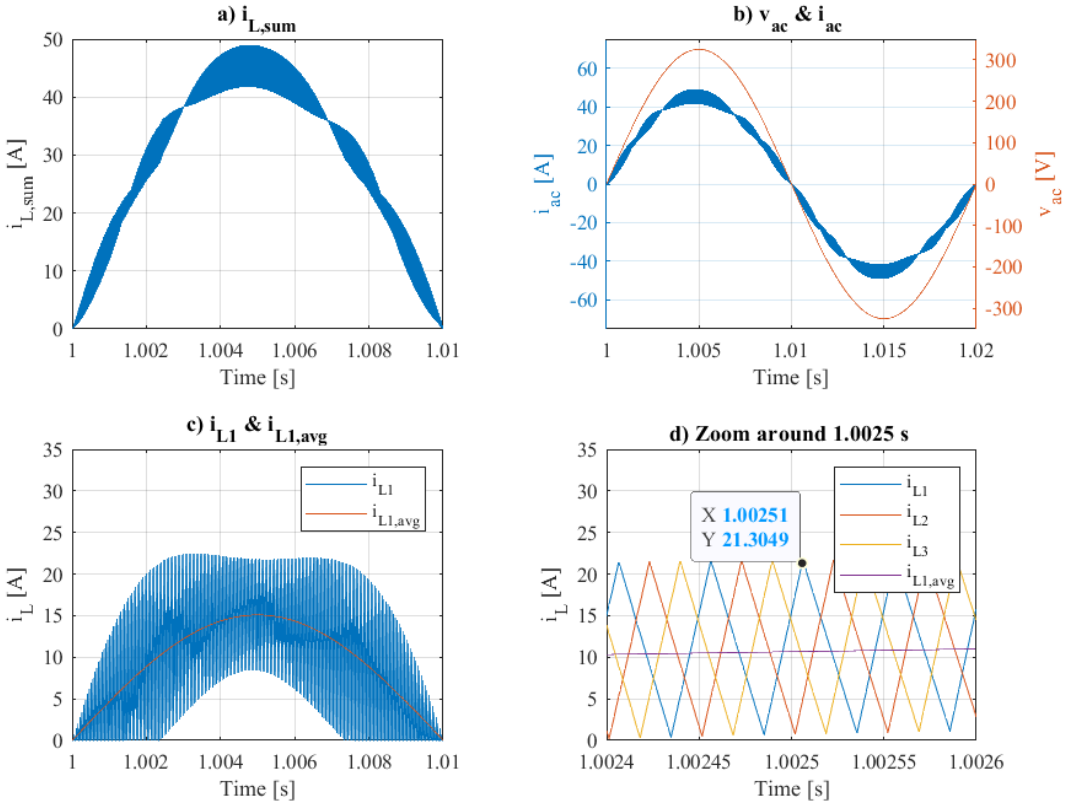

Figure 2.12: QCM operation waveforms with $L_{QCM} = 229\ \mu H$ (a) Sum of inductor currents $i_{L,sum}$ =i_{L1} + i_{L2} +i_{L3}. (b) AC input voltage and AC input current waveform. (c) Inductor current i_{L1} for one half cycle. (d) Detailed view of all three inductor currents at $\theta = 45°$.

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Table 2.3 presents a comparison between numerically calculated $\Delta i_{L,DP}$ values and those obtained from simulations.The power factor measured for all three modulation techniques is higher than 0.99. It is evident that the discrepancy between numerical and simulated results is not substantial. This affirms the validity of the obtained inductance values for all three current modulation techniques discussed in this chapter. It can be noted that CCM exhibits the least inductor current ripple, while DCM displays the highest. A lower current ripple necessitates a higher inductance, leading to an increase in boost inductor volume but a reduction in the size of the EMI filter. Conversely, accepting a higher current ripple allows for a smaller inductance, but this results in an increase in the volume of the EMI filter. Simulation results for QCM fall between these extremes, making it an intriguing current modulation technique for further analysis [7].

Mode	CCM	QCM	DCM
Inductance value	1348 μH	229 μH	100μH
Design Point (DP)	$D = 0.5$	$\alpha = 45^\circ$	$\alpha = 90^\circ$
Angle at DP (θ_{DP})	38°	45°	90°
Time at DP	1.0021 s	1.0025 s	1.005 s
Peak to peak inductor current at DP (numerical)	3.71 A	21.33 A	30.17A
Peak to peak inductor current at DP (simulation)	3.76 A	21.305 A	30.22 A

Table 2.3: Summary of comparison of numerical and simulated values peak to peak inductor current for interleaved PFC converter for P_o = 7360 W, V_o = 400 V, $V_{in,rms}$ = 230 V and F_{sw} = 20 kHz.

Chapter 3
GUI for Inductor Design and Volume Optimisation

This chapter provides a comprehensive outline of the inductor design process, taking into account various core types and identifying the core with the smallest volume that meets the necessary design parameters. A Graphical User Interface (GUI) to design the inductor and optimise for the least volume is also presented. It also delves into the discussion of the steady-state simulation of the PFC converter using a MATLAB script.

3.1 Cores under consideration for design of inductor

The design of the boost inductor is based on the database of toroidal powder cores from Magnetics. The powder core materials produced by Magnetics for toroidal cores, include Kool Mμ (sendust), MPP (molypermalloy), Kool Mμ MAX, Kool Mμ Hf, Edge, High Flux, XFlux. These distributed air gap cores are widely used in power inductor applications. High resistivity, little hysteresis and eddy current losses, and impressive inductance stability under both DC and AC situations are just a few benefits of the powder core materials offered by Magnetics that stand out. These materials undergo pressing without organic binders, preventing thermal ageing [14, 15].

Each of the seven materials finds application in various scenarios, and each has its unique advantages. To achieve the lowest loss inductor, it is advisable to utilize Kool Mμ Hf and MPP materials, given their exceptional track record of minimising core losses. In designs where space efficiency is paramount, particularly in situations dominated by DC bias, the preferable choices would be Edge and High Flux due to their remarkable flux capacity. In instances where cost considerations weigh heavily, XFlux can serve as a more budget-friendly alternative to High Flux, granted that the compromise in terms of higher core losses and somewhat restricted permeability availability is deemed acceptable. Both Kool Mμ and Kool Mμ MAX stand out as cost-effective options, providing excellent DC bias performance under current loading conditions [14, 15].

3.2 Inductor design

The main parameters required for designing the inductor are

- Inductance (L_{design}) required with DC bias.
- The design current (I_{design}) at which the inductance with DC bias is required.
- The RMS value of current (I_{rms}) to determine the required wire size.
- Other factors like maximum winding factor allowed, single layer or multi layer, number of stacked cores (N_C), temperature rise allowed, and switching frequency.

Once these parameters are in hand, the different steps involved in the inductance design for a selected core with inductance factor A_L in nH/T^2 are as follows:

1. Selection of required core.
   There are about 1000 different toroidal cores available from magnetics in different sizes, permeability, and materials. Each core has its own geometric and magnetic properties which are provided in the datasheet of the respective cores.

2. Calculate the required AWG of the copper wire required from the wire table with the help of I_{rms} and the current density allowed ($500A/cm^2$ is considered in this project).

3. Find out the maximum possible single-layer winding N_p with the selected wire size for the core, from the winding table in the datasheet.

4. Take initial value of inductance $L_0 = L_{design}$.

5. Calculate the required number of windings N_r with the value of L_0 in μH, A_L in nH/T^2 and N_c (number of stacked cores) known.

$$N_r = \sqrt{\frac{L_0 \cdot 10^3}{A_L \cdot N_c}} \tag{3.1}$$

6. The magnetic field strength or bias in Oersteds is found with the formula,

$$H = \frac{4\pi \cdot N_r \cdot I_{design}}{l_e} \tag{3.2}$$

   where l_e is the magnetic path length in (mm) of the core.

7. From the Permeability vs. DC Bias curves for the core selected, determine the rolloff percentage of initial permeability (%μ) for the previously calculated bias level (H).

$$\%\mu = \frac{1}{(a + bH^c)} \tag{3.3}$$

8. Multiply the required inductance L_0 by the %μ to find the inductance L_{biased} with bias current applied.

9. If the L_{biased} is significantly lower than the L_{design} due to biasing, find new L_0 by dividing old value of L_0 by %μ and iterate steps 5-9 till the L_{biased} is close to the L_{design} at the required biased condition.

10. The final number of turns N_r must be equal to or lower than the maximum number of possible windings N_p if it is a single layer winding. For a multi layer winding the main limitation is meeting the maximum winding factor. If this condition is not met, a different core is chosen.

The above procedure for designing the inductance is implemented as a GUI using MATLAB App Designer. The example of L_{QCM} = 229 μH is taken for demonstration.

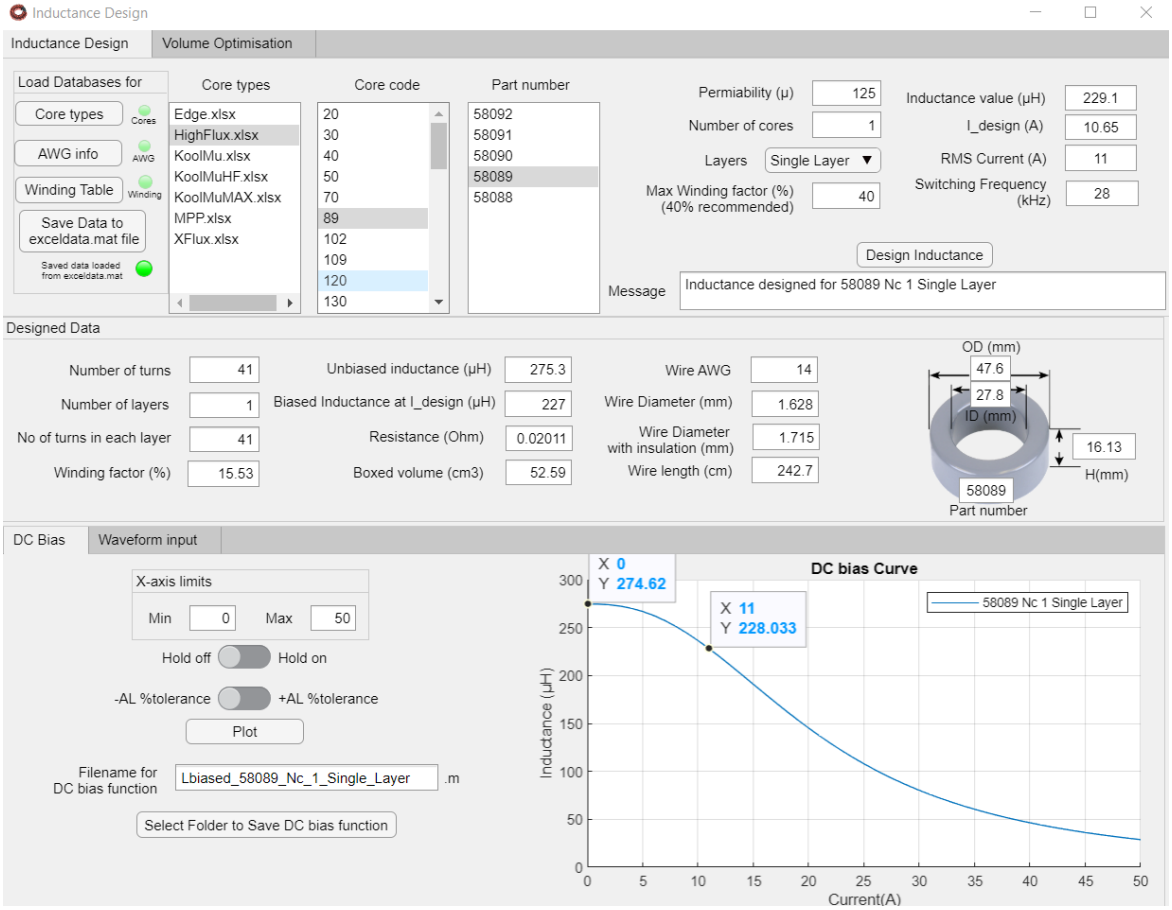


Figure 3.1: Inductance designed for QCM operation for L_{QCM} = 229 μH.

The inductance value drops as the current increases due to the biasing of the core. The current through inductor as seen in Figure 2.12 varies from 0 A to 21.3 A around the design point α = 45°. So if the inductance value changes with the current, the QCM operation may not be maintained if we wind the inductance for L_{QCM} = 229 μH at I_{design} = 0 A. Thus to make sure that the QCM operation is maintained as designed, the I_{design} value is taken to be 10.65 A (half of 21.3 A). It can be seen in the numerically modeled DC bias curve plot in the Figure 3.1 that, with -A_L tolerance the unbiased inductance at 0 A is 274.62 μH and at 11 A it is 228 μH as designed. The inductance is wound at the lab and tested using the power choke tester DPG to verify the calculations. The results are as shown in the Figure 3.2. It can be seen that the actual measurement and the numerical model are comparable and thus the design procedure is verified to be okay. The slight difference in the plots can be attributed to the change in A_L as given by the % tolerance in the datasheet for the core of size 89 in Figure D.1.

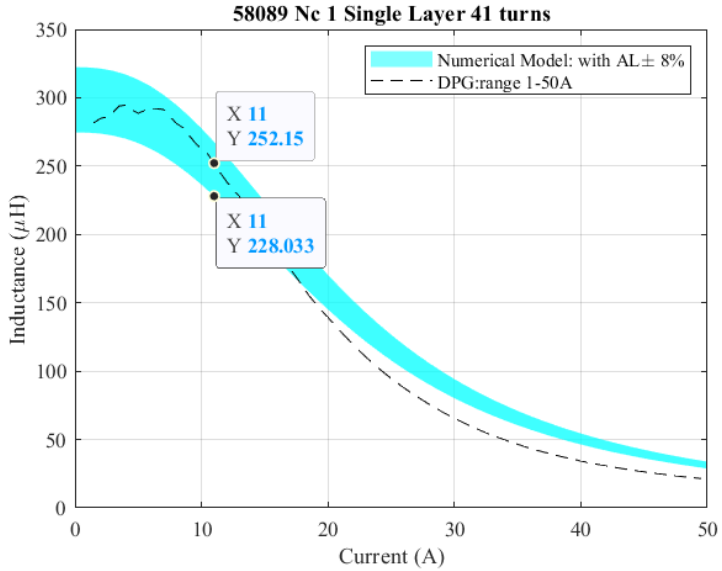


Figure 3.2: Numerical model and DPG result comparison for L_{QCM} = 229 μH at I_{design} =10.65 A.

There are about 1000 different toroidal cores available from magnetics in different sizes, permeability, and materials. Choosing the right core for the specific application and requirements needs to be optimised. The second tab of the GUI is designed to perform volume optimisation to find the cores with minimum volume for each of the materials. The code, when provided with the required data, computes and designs inductance with all the cores in the database. Feasible results are then compared to identify the cores with the minimum volume for each material.

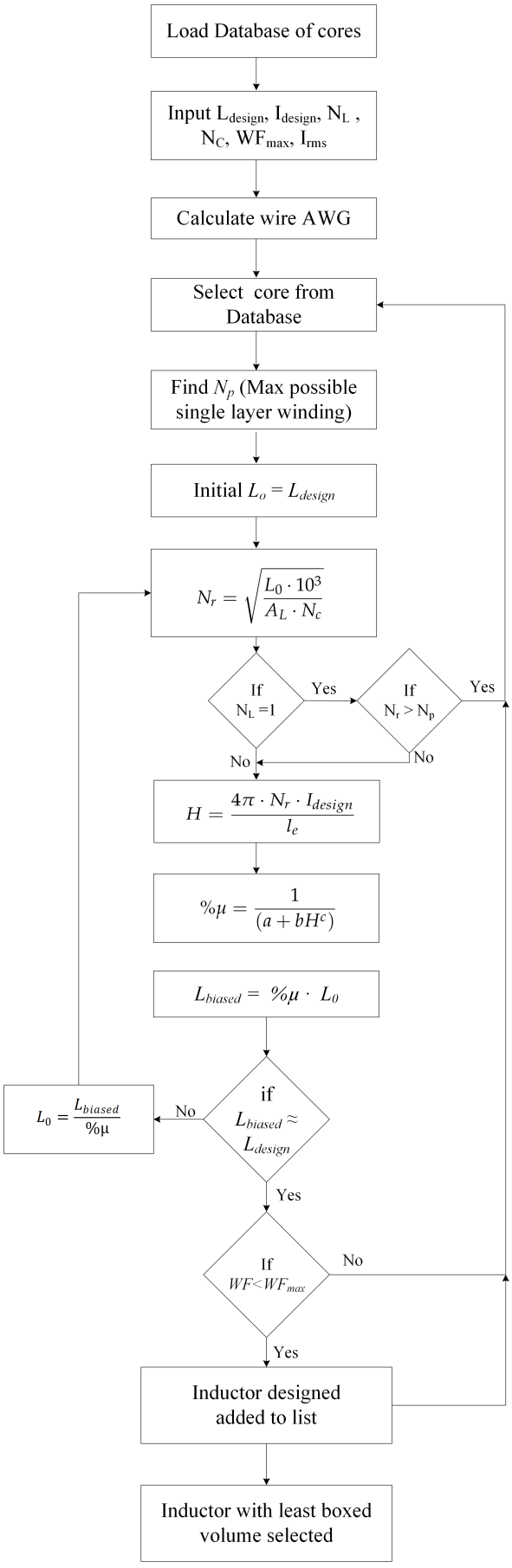
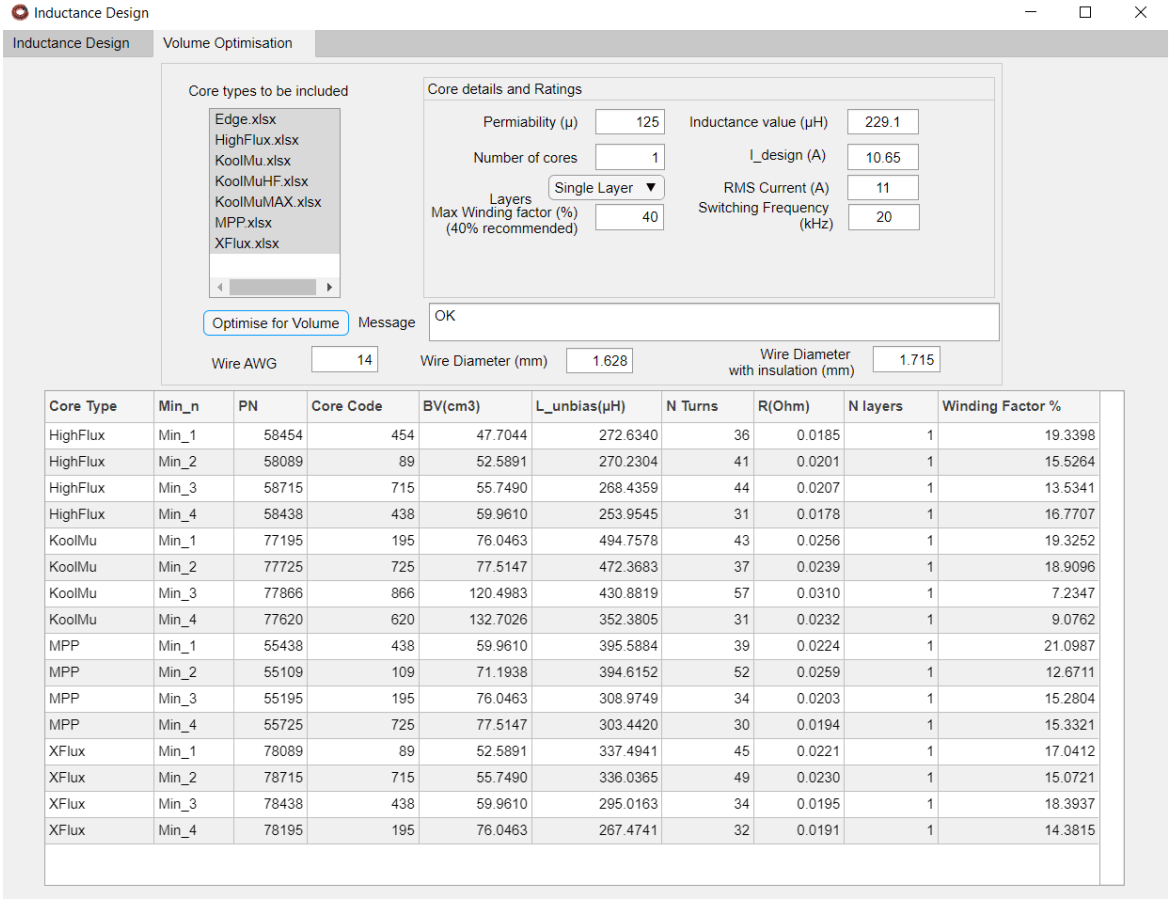


Figure 3.3: Flow chart for finding inductor with least boxed volume.



Core Type	Min_n	PN	Core Code	BV(cm3)	L_unbias(μH)	N Turns	R(Ohm)	N layers	Winding Factor %
HighFlux	Min_1	58454	454	47.7044	272.6340	36	0.0185	1	19.3398
HighFlux	Min_2	58089	89	52.5891	270.2304	41	0.0201	1	15.5264
HighFlux	Min_3	58715	715	55.7490	268.4359	44	0.0207	1	13.5341
HighFlux	Min_4	58438	438	59.9610	253.9545	31	0.0178	1	16.7707
KoolMu	Min_1	77195	195	76.0463	494.7578	43	0.0256	1	19.3252
KoolMu	Min_2	77725	725	77.5147	472.3683	37	0.0239	1	18.9096
KoolMu	Min_3	77866	866	120.4983	430.8819	57	0.0310	1	7.2347
KoolMu	Min_4	77620	620	132.7026	352.3805	31	0.0232	1	9.0762
MPP	Min_1	55438	438	59.9610	395.5884	39	0.0224	1	21.0987
MPP	Min_2	55109	109	71.1938	394.6152	52	0.0259	1	12.6711
MPP	Min_3	55195	195	76.0463	308.9749	34	0.0203	1	15.2804
MPP	Min_4	55725	725	77.5147	303.4420	30	0.0194	1	15.3321
XFlux	Min_1	78089	89	52.5891	337.4941	45	0.0221	1	17.0412
XFlux	Min_2	78715	715	55.7490	336.0365	49	0.0230	1	15.0721
XFlux	Min_3	78438	438	59.9610	295.0163	34	0.0195	1	18.3937
XFlux	Min_4	78195	195	76.0463	267.4741	32	0.0191	1	14.3815

Figure 3.4: Volume optimisation for QCM operation for L_{QCM} = 229 μH.

It can be seen in Figure 3.4 that the 58089 core of High Flux (designed in Figure 3.1) has the second minimum boxed volume of 52.589 cm^3.

Other cores are also designed to see if all of the DC bias curves meet at the design point of L_{QCM} = 229 μH at I_{design} =10.65 A and to see which has better DC bias performance. The DC bias curves of High Flux 58089 (Min_2), Kool Mu 77195 (Min_1), MPP 55438 (Min_1), and XFlux 78089 (Min_1) are compared in Figure 3.5. High Flux 58089 (Min_2) is chosen over High Flux 58454 (Min_1) because they were comparable and more importantly 58089 core was readily available in the lab to be wound physically and test with DPG power choke tester.

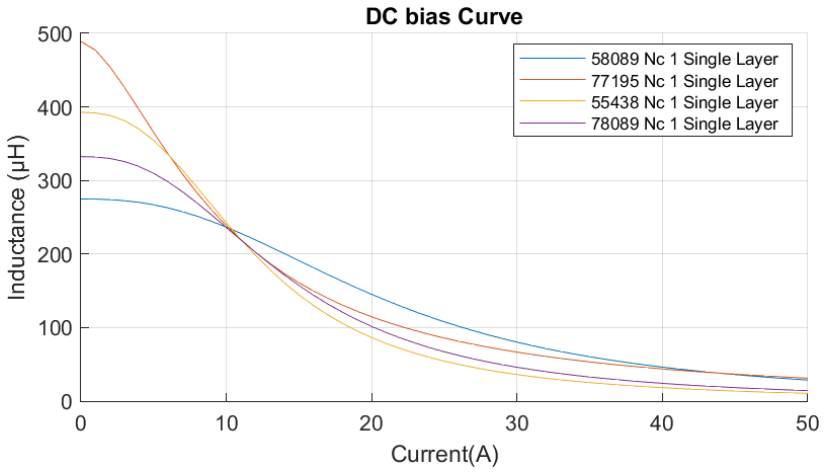


Figure 3.5: Different possible designs for L_{QCM} = 229 μH at I_{design} =10.65 A.

As depicted in Figure 3.5, High Flux core 58089 has better DC bias performance among the ones compared. The unbiased inductance is minimum for High Flux core and demonstrates less saturation when compared to the other cores at higher current values.

3.3 MATLAB code to incorporate DC biasing of inductance

In the previous subsection, it is demonstrated that inductance changes with biasing. This effect is not considered in the PLECS simulation. To address this, a MATLAB script is written to simulate the PFC boost converter in steady state, taking into account the DC biasing of the inductor. Additionally, steady-state current waveforms of the PFC boost converter can be utilised for further optimisations. In PLECS, the waveforms need to be saved each time after the simulation reaches steady state. This process can be time-consuming, especially for complex simulations, and it can significantly slow down any optimisation algorithm that relies on data from the steady state. Hence, the implementation of the PFC boost converter in MATLAB is of great importance.

The simulation previously conducted in PLECS which does not consider the effect of DC biasing for L_{QCM} = 229 μH as shown in Figure 2.12, is repeated using a MATLAB script. The resulting waveform without the effect of DC bias is displayed in Figure 3.6. The results are matching for both simulations.

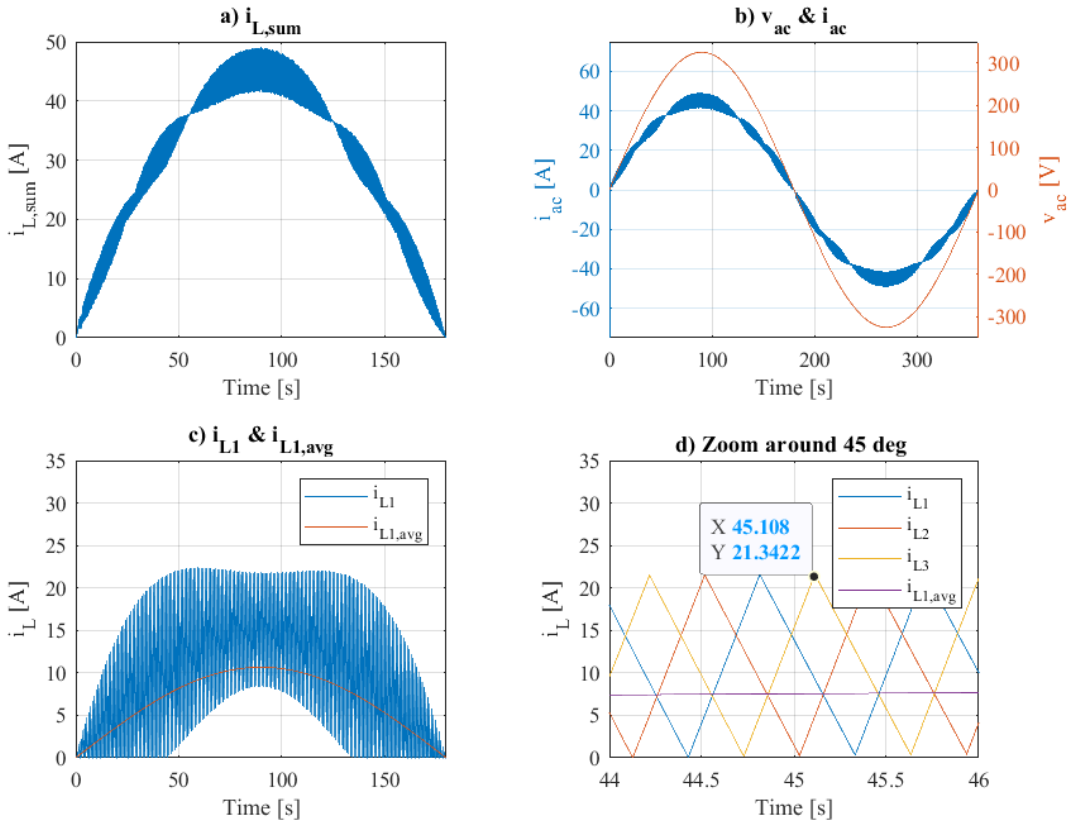


Figure 3.6: QCM operation waveforms in MATLAB with L_{QCM}= 229μH, no biasing (a) Sum of inductor currents $i_{L,sum}$ =i_{L1} + i_{L2} + i_{L3}. (b) AC input voltage and AC input current waveform. (c) Inductor current i_{L1} for one half cycle. (d) Detailed view of all three inductor currents at $\theta = 45°$.

Now, the DC bias of the inductor is incorporated into the simulation after designing the inductance for L_{QCM} = 229 μH at I_{design} =10.65 A. In Figure 3.6, it is shown that without considering the DC bias effect in the simulation, the α angle is 45°, and the peak-to-peak current ripple is 21.4 A. However, in the case of the simulation with the biasing effect included, the α angle is 50°, and the peak-to-peak current ripple is 27.62 A. This change in ripple and angle is due to biasing.

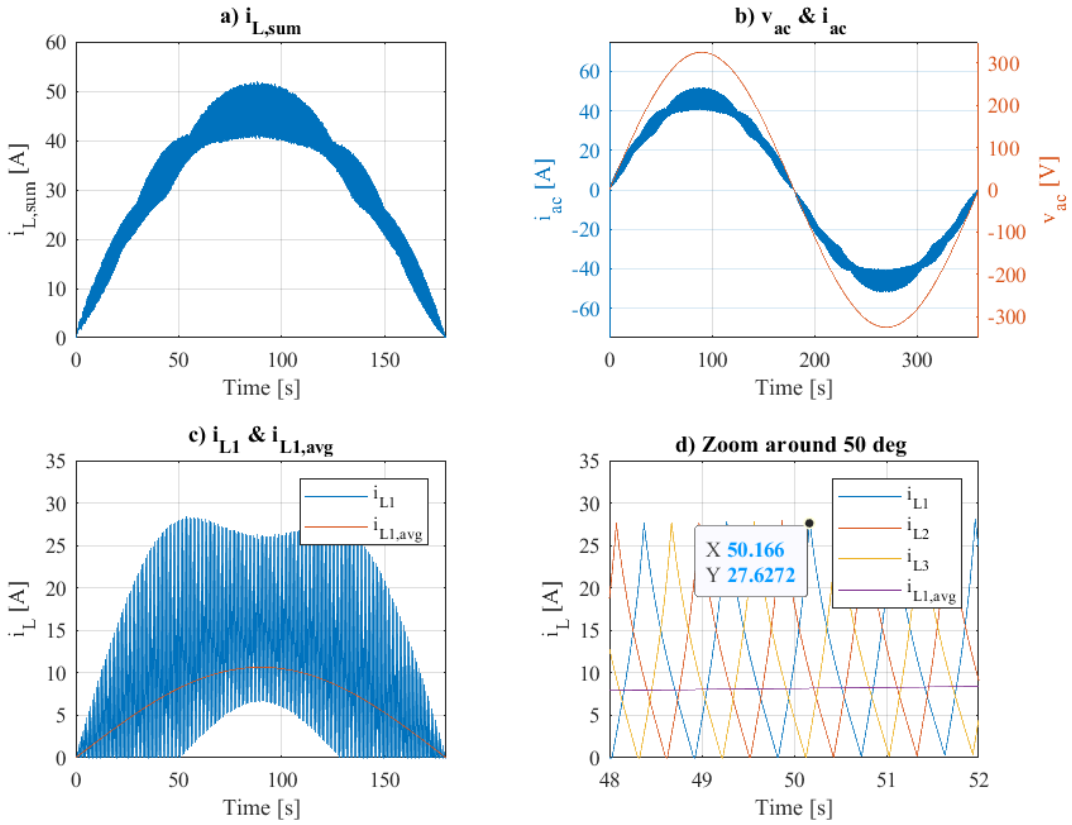


Figure 3.7: QCM operation waveforms in MATLAB with L_{QCM}= 229μH at I_{design} =10.65 A (biasing effect included) (a) Sum of inductor currents $i_{L,sum}$ =i_{L1} + i_{L2} + i_{L3}. (b) AC input voltage and AC input current waveform. (c) Inductor current i_{L1} for one half cycle. (d) Detailed view of all three inductor currents at $\theta = 50°$.

Chapter 4
Differential Mode EMI Filter Design and Loss modelling

The first section of this chapter introduces the design of the differential-mode (DM) EMI filter. The EMI noise measurement and simulations are discussed to understand how the EMI noise can be predicted at the simulation level. The second part of the chapter focuses on the discussion of modeling losses in various components of the PFC converter.

4.1 Differential mode EMI filter Design

Power electronic converters with high frequency switched currents like Switched-Mode Power Supplies (SMPS) generate high-frequency conducted emissions, necessitating the design of an EMI filter to meet regulatory standards and protect the mains from these emissions. EMI filter is a necessary part of the PFC converter as well. When designing the input EMI filter, two primary sources of noise must be considered: differential-mode (DM) and common-mode (CM) noise. EMII noise originates from the presence of parasitic elements within a circuit, such as Equivalent Series Inductance (ESL) or Equivalent Series Resistance (ESR), stray capacitances as well as due to high-frequency switching.

The differential-mode refers to signals or noise that flow in opposite directions in a pair of lines. In a single phase system, DM noise flows between the phase and neutral lines. This type of noise can directly impact sensitive circuit components, and the grid leading to a degradation in system performance. Noise can also be conducted from any line in the system towards the ground. This specific kind of noise is referred to as CM noise. The key distinction is that CM noise propagates in the same direction through all lines before reaching the ground. Sensitive analog and digital circuits are affected more by the CM noise. Given that the DM filter significantly influences the size of the EMI filter, this project's primary focus will be on mitigating DM noise, thereby achieving maximum power density. A DM EMI filter can have up to n_f filter stages. Figure 4.1 shows the PFC boost converter with two LC filter stages.

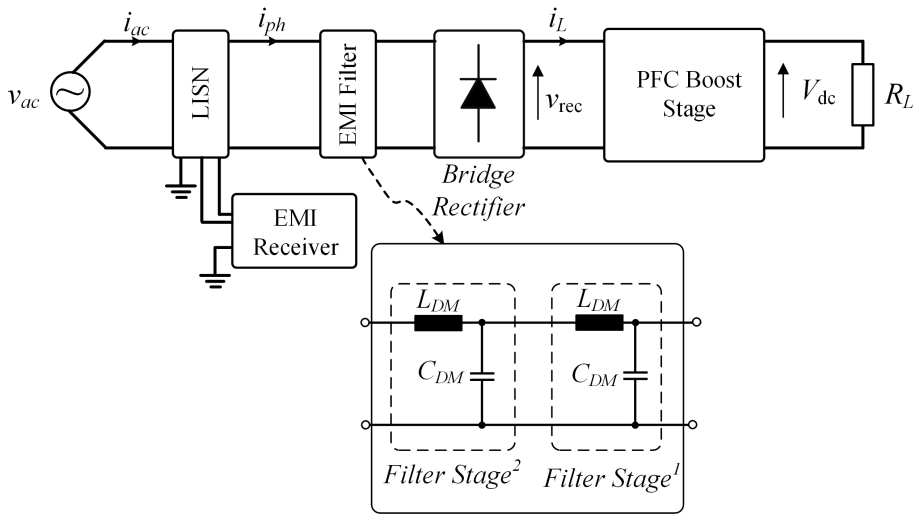


Figure 4.1: Single phase PFC boost converter including the EMI filter at the input.

There are various EMC standards that define the acceptable levels of electromagnetic emissions and the susceptibility of electronic and electrical devices or systems to electromagnetic interference. These standards ensure that devices and systems can function correctly without causing or being affected by electromagnetic interference. EMC standards are classified based on their application.

Based on the frequency range noise limit in CISPR standard is categorized into band A and band B. Band A extends from 9 kHz to 150 kHz and band B covers the range from from 150 kHz to 30 MHz as shown in Figure 4.2. Different limits and measurement methods may apply to emissions within these bands. Band B represents the frequency range for which regulatory compliance is mandatory, while Band A pertains to a frequency range where only specific products are subject to regulation as defined by the standard. Within band B of CISPR 11, limit lines are defined separately for residential areas and industrial areas. These two areas are represented by two classes of limits: class A represents the industrial environment; class B defines the limits for residential areas which have a more stringent limit. In this work, CISPR 11 for class B on the Band B is the focus of consideration.

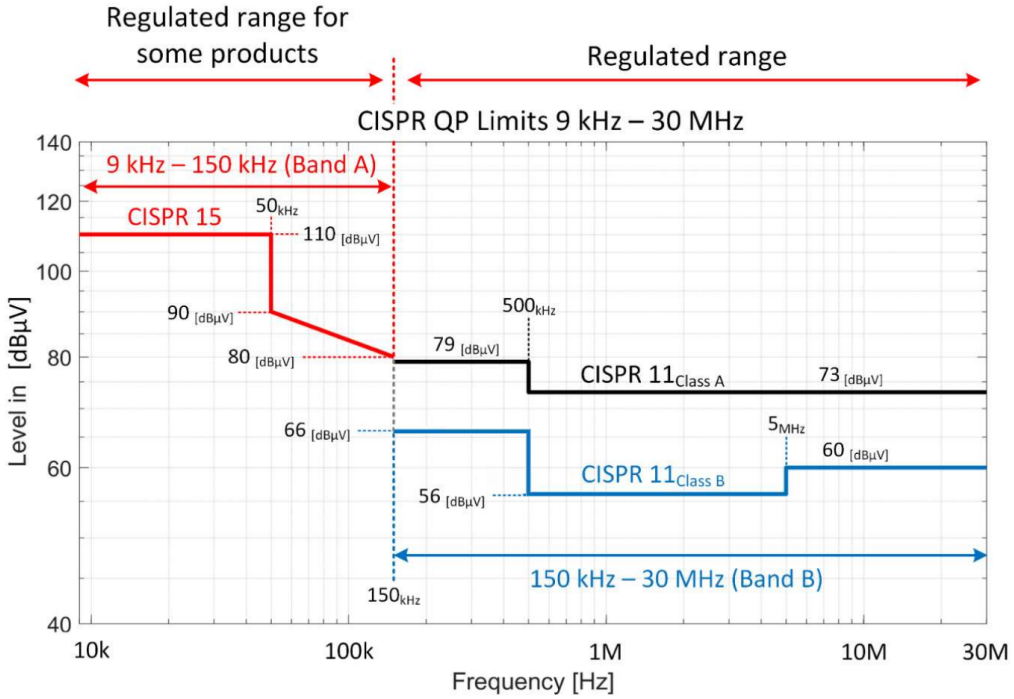


Figure 4.2: CISPR Quasi-Peak (QP) limits for 9 kHz - 30 MHz frequency range [16].

4.1.1 Differential mode EMI noise measurement

Conducted mode emission is measured using an EMI receiver along with LISN as shown in the Figure 4.1. Modeling LISN and the EMI receiver virtually helps optimize the filter during the design phase and aids in the early identification of issues [16].

Line Impedance Stabilization Network - LISN

A Line Impedance Stabilization Network (LISN), alternatively referred to as an Artificial Mains Network (AMN) in the latest IEC standards, is used for conducted emission testing. It facilitates the decoupling of the mains power supply and the high-frequency emissions generated by the power converter. Additionally, it establishes a fixed impedance for both line and ground currents, ensuring that measurements can be consistently replicated [16]. The LISN is positioned between the AC power source and the PFC converter with the purpose of creating a predictable impedance profile across the desired frequency range. To ensure impedance mismatch, the LISN provides a low-impedance path on the mains side while maintaining a high-impedance path from the load to the ground. The voltage drop across the LISN resistor is utilized to measure the conducted noise voltage $U_{meas}(t)$ [7].

EMI Receiver

EMI receivers function similarly to high-frequency spectrum analyzers, in accordance with CISPR 11 specifications. A simplified model of EMI receiver proposed in [16] is considered for the modeling. The LISN output voltage is translated from the time domain, $U_{meas}(t)$, to the frequency domain, $U_{meas}(f)$, through Fourier analysis in the EMI receiver. The spectrum of measured voltage, $U_{meas}(f)$, is then passed through a bandpass

filter known as the Resolution Band Filter (RBW). Depending on the frequency band of interest, bandwidth of the bandpass filter will change. In the CISPR 11 standard, it is defined as RBW = 9kHz for Band B. The output signal from the RBW filter is processed using a quasi-peak detector. The quasi-peak EMI emission can be predicted using Equation (4.1). This approach may result in a slightly oversized filter for certain frequency ranges. Nonetheless, taking into account component variations, measurement errors, and uncertainties in the modeling process, this can also offer advantages in the filter design process.

$$U_{QP,\max}\left(f_{sweep}\right)\left[dB\mu V\right] = 20 \cdot \log\left[\frac{1}{1\mu V}\sum_{f=f_{sweep}-RBW/2}^{f=f_{sweep}+RBW/2} U_{meas}(f)\right] \tag{4.1}$$

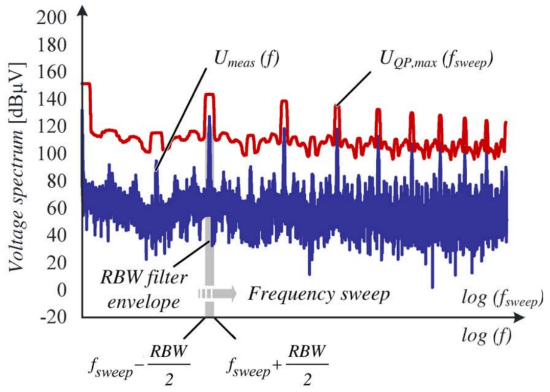


Figure 4.3: CISPR Quasi-Peak (QP) limits for 9 kHz - 30 MHz frequency range [9].

4.1.2 DM filter design

To meet the requirements of the CISPR 11 standard, it is necessary to place a DM filter at the input of the PFC converter. This filter should be capable of providing an attenuation of $Att_{req,LC}$ at frequency f_D. The attenuation, Att_{LC}, provided by a filter with n_f stage is calculated as per Equation (4.2). This estimation is applicable for higher frequencies ($f > 150kHz$) [17].

$$Att_{LC} = \frac{1}{\left(2 \cdot \pi \cdot f_D\right)^{2n_f} \cdot L_{DM}^{n_f} \cdot C_{DM}^{n_f}} \geqslant Att_{req,LC}(f_D) \tag{4.2}$$

Here L_{DM} and C_{DM} of each stage are chosen to have the same values. This design choice results in a filter with minimal volume.

Selecting design frequency

The design frequency, denoted as f_D, plays a significant role in determining both the overall filter volume and the choice of the number of filter stages to be deployed. f_D is chosen as the first multiple of the switching frequency within the frequency range of Band B (150 kHz - 30 MHz). Consequently, if the switching frequency (f_{sw}) is greater than or equal to 150 kHz, f_D will align with f_{sw}. However, if f_{sw} is less than 150 kHz,

the calculation of the design frequency for an n_{stage} interleaved PFC converter follows a specific procedure.

$$f_D = m \cdot n_{stage} \cdot f_{sw}, \text{ where } m = \text{ceil}\left(\frac{150\text{kHz}}{n_{stage} \cdot f_{sw}}\right) \tag{4.3}$$

For a switching frequency of f_{sw} =20 kHz, and number of interleaved boost cells n_{stage} = 3, the factor of m computes to 3. The design frequency is then determined as f_D = 180 kHz, which corresponds to the ninth multiple of the switching frequency.

Calculating required attenuation

The required attenuation in dB at f_D is computed by subtracting the CISPR standard limit at f_D from the quasi-peak value of the original noise without a filter at f_D, then adding some margin of 6 dB, as depicted in Equation (4.4).

$$Att_{req,db}(f_D) = U_{QP,\max}(f_D)[dB\mu V] - CISPR_{Limit}(f_D)[dB\mu V] + Margin[dB] \tag{4.4}$$

$$Att_{req,LC}(f_D) = 10^{\left(-Att_{req,db}(f_D)/20\right)} \tag{4.5}$$

Finding filter cut-off frequency

Equation (4.6) provides the cut-off frequency (f_c) for the DM EMI filter.

$$f_c = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{DM} \cdot C_{DM}}} \tag{4.6}$$

It is a useful indicator of filter size because it can be observed that the filter cut-off frequency decreases with increasing values of $L_{DM} \cdot C_{DM}$. Low cut-off filter frequency implies a larger filter since higher capacitance and inductance values imply larger components. To lower the filter volume, an EMI filter with a high cut-off frequency is desired [7, 17].

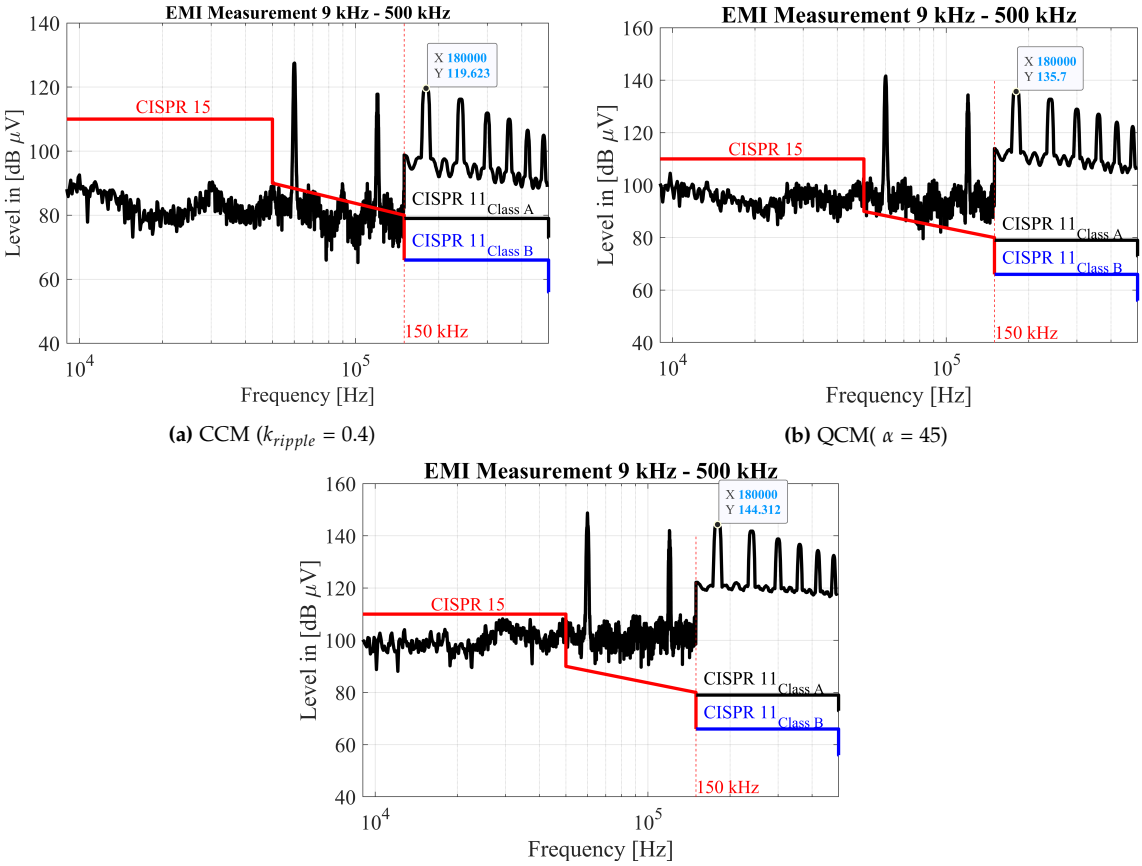
$$Att_{req,LC}(f_D) = \frac{1}{(2 \cdot \pi \cdot f_D)^{2n_f} \cdot L_{DM}^{n_f} \cdot C_{DM}^{n_f}} \tag{4.7}$$

The filter cut-off frequency for n_f stage EMI filter can be determined by first obtaining the product ($L_{DM} \cdot C_{DM}$) using equation Equation (4.7), followed by equation Equation (4.6) to get,

$$f_c = f_D \cdot \sqrt[2n_f]{Att_{req,LC}(f_D)} \tag{4.8}$$

4.1.3 Comparison of EMI measurement in CCM, QCM, and DCM

The simulation is conducted for CCM, QCM, and DCM which was designed in Table 2.1 in accordance with the specifications outlined in Table 1.1, using the MATLAB script. Subsequently, the EMI noise was measured utilising the model designed for LISN and EMI receiver. The results of EMI noise simulation results are presented in Figure 4.4.



(a) CCM (k_{ripple} = 0.4)

(b) QCM(α = 45)

(c) DCM (α = 90)

Figure 4.4: EMI simulation measurment results for CCM, QCM and DCM operation of thre stage interleaved converter at the rated conditions, f_{sw} = 20 kHz.

In Figure 4.4, it is evident that the filter design frequency f_D is 180 kHz in all the three modulation technique as expected from Equation (4.3). Notably, the quasi-peak at f_D for DCM reaches the highest value at 144.37 dBμV, followed by QCM at 135.7 dBμV, and the lowest for CCM at 119.62 dBμV. The filter cut-off frequency f_c for a two-stage EMI filter has been computed and is tabulated in Table 4.1.

4.1.4 Filter component size

In this subsection,the emphasis lies in designing the filter with the smallest possible volume. The filter cut-off frequency f_c can be translated to boxed volume by optimizing the values of the filter inductor L_{DM} and capacitor C_{DM} for the least volume. For an EMI filter with n_f stages, the total volume V_{DM} of the EMI filter is determined by Equation (4.9) [17].

$$V_{DM} = n_f \cdot V_L + n_f \cdot V_C \rightarrow \min \tag{4.9}$$

where V_L and V_C are given by,

$$\begin{aligned} V_L &= k_{L1} \cdot L_{DM} \cdot I_{in,pk}^2 + k_{L2} \cdot L_{DM} + k_{L3} \cdot I_{in,pk} \\ V_C &= k_{C1} \cdot C \cdot U_{in,pk}^2 + k_{C2} \end{aligned} \tag{4.10}$$

The inductance L_{DM} and capacitance C_{DM} are interrelated through the filter cutoff frequency by Equation (4.6). Consequently, L_{DM} can be substituted in terms of C_{DM} in

Equation (4.9).

$$\begin{aligned} V_{DM} &= b \cdot L_{DM} + c + d \cdot C_{DM} + e \\ \rightarrow V_{DM} &= b \cdot \frac{a}{C_{DM}} + c + d \cdot C_{DM} + e \end{aligned} \tag{4.11}$$

where the coefficients a,b,c,d, and e are as defined in Equation (4.12).

$$\begin{aligned} a &= L_{DM} \cdot C_{DM} = \frac{1}{(2\pi \cdot f_D)^2 \cdot \sqrt[n_f]{Att_{req,LC}(f_D)}} \\ b &= n_f \cdot \left(k_{L1} \cdot I_{in,pk}^2 + k_{L2}\right) \\ c &= n_f \cdot k_{L3} \cdot I_{in,pk} \\ d &= n_f \cdot \left(k_{C1} \cdot U_{in,pk}^2\right) \\ e &= n_f \cdot k_{C2} \end{aligned} \tag{4.12}$$

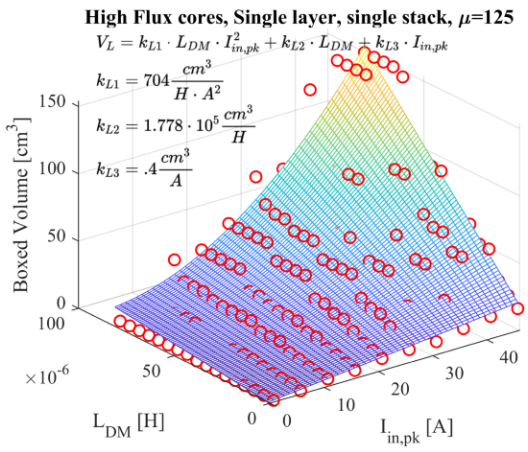
Then by differentiation of Equation (4.11) with respect to C_{DM} to minimize the volume and equating the result with zero,

$$\frac{\partial V_{DM}}{\partial C_{DM}} = 0, \tag{4.13}$$

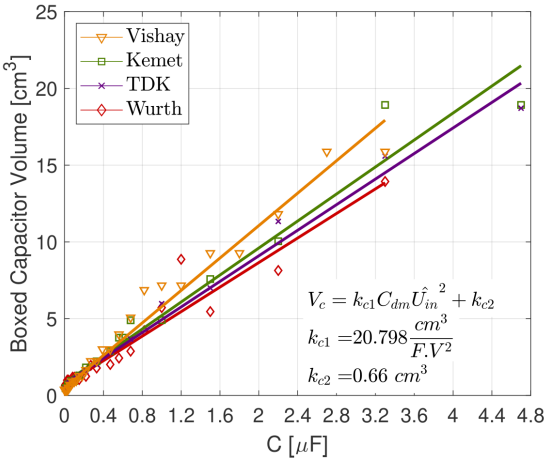
we get the equations for L_{DM} and C_{DM} in Equation (4.14).

$$\begin{aligned} C_{DM} &= \sqrt{\frac{a \cdot b}{d}}, \\ L_{DM} &= \sqrt{\frac{a \cdot d}{b}}. \end{aligned} \tag{4.14}$$

The values of V_L and V_C in Equation (4.10) are approximated through plots shown in the Figure 4.5. Specifically, Figure 4.5a is generated using a MATLAB script from the developed GUI. This script determines the core with the least volume for a set of currents and inductances.



(a) Inductor boxed-volume approximation for DM filter inductances using High Flux Magnetics toroid cores in dependence on the inductance value.



(b) Metallized Polypropylene (MKP) Class X2 capacitors (305, 310 V RMS) volume approximation for DM filter capacitors. [7]

Figure 4.5: Inductor boxed volume and capacitor volume approximation for DM filter.

The optimum number of filter stages for f_D = 180kHz is plotted in the Figure 4.6. For a required attenuation within the range of 40 dB < $Att_{req,db}$ < 80 dB, two filter stages yield to minimum filter volume. On the other hand, for a required attenuation within the range of 80 dB < $Att_{req,db}$ < 140 dB, three filter stages result in the minimum filter volume.

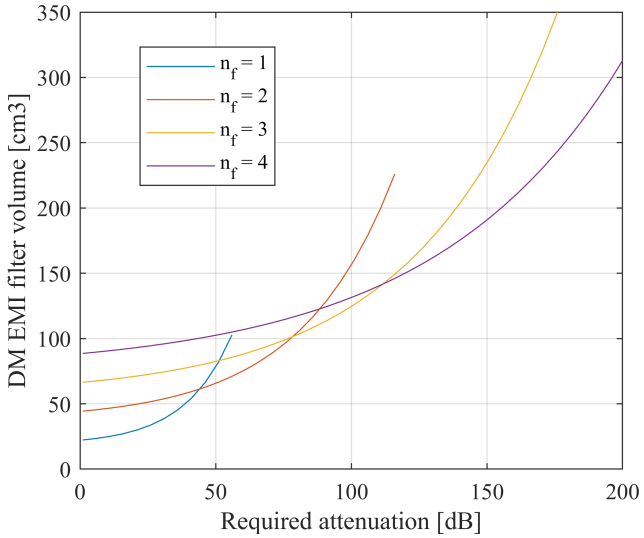


Figure 4.6: Total DM EMI filter boxed volume as a function of the required attenuation for different number of filter stages, for f_D = 180 kHz,$I_{in,pk}$ = 45A, $U_{in,pk}$ = 325 A.

4.2 Loss modelling

Loss calculation of the different passive and active components is necessary for optimizing the PFC converter for high power density while ensuring minimal compromise on efficiency. This section provides an explanation of how the losses in semiconductor components, boost inductor, and output capacitor are computed.

4.2.1 Core loss and copper loss of boost inductor

To further optimise the selection of boost inductor, it is essential to compute the inductor losses, which comprise both core loss P_{core} and copper loss P_{cu}. The copper loss P_{cu} primarily arises from the resistive loss $P_{cu,dc}$, through the winding inductance. additionally, there is a minor portion of eddy current loss $P_{cu,edd}$ due to skin and proximity effect which is not taken into account in this analysis [18].

$$P_{cu,dc} = I_L^2 \cdot R_{L,dc} \tag{4.15}$$

where I_L is the RMS current through the inductor and $R_{L,dc}$ is the DC resistance of the winding calculated from Equation (4.16).

$$R_{L,dc} = \rho_{cu} \cdot l_{cu} / A_{cu} \tag{4.16}$$

The datasheet for cores from core manufacturers [15] provides core loss density curves in the form of Steinmetz equation,

$$P_{core,v} = k \left(B_{pk}\right)^a \left(f_{sw}\right)^b \tag{4.17}$$

where $P_{core,v}$ is the time average power loss per unit volume. This equation is only valid for sinusoidal current waveforms. For a more accurate estimation, in cases involving non-sinusoidal switched waveforms of current, improved Generalized Steinmetz Equation (iGSE) is employed.

$$P_{core,v} = k_i \cdot f_{sw} \cdot \Delta B^{(a-b)} \sum_j \left(\frac{U_{Ldc,j}}{N \cdot A_e} \right)^b \Delta t_j \tag{4.18}$$

where N denotes the number of turns, $U_{Ldc,j}$ is the voltage across the inductor during a switching time interval of Δt_j. From this the inductor core loss P_{core} can be computed using Equation (4.19) [18, 19].

$$P_{core} = l_e \cdot A_e \cdot N_c \cdot P_{core,v} \tag{4.19}$$

4.2.2 Output capacitor loss

The output capacitor C_{dc}, designed in Section 2.3, has a voltage and current ripple with twice the frequency of line voltage, (2*f_{line}). The ripple component of the diode current is filtered in the output capacitor, as it offers a lower impedance compared to the load [20]. The power loss in the output capacitor, with an effective series resistance (ESR) and the RMS of the current passing through the capacitor ($I_{Co.rms}$), is calculated using Equation (4.20).

$$P_{Cdc} = {I_{Cdc,rms}}^2 \cdot ESR \tag{4.20}$$

Where ESR is calculated using Equation (4.21) in which DF is the dissipation factor ($tan\delta$) and $I_{Cdc,rms}$ is calculated using Equation (4.22) [21].

$$ESR = \frac{DF}{2 \cdot \pi \cdot (2 \cdot f_{line}) \cdot C_{dc}} \tag{4.21}$$

$$I_{Cdc,rms} = \sqrt{\frac{8 \cdot \sqrt{2} \cdot {P_o}^2}{3 \cdot \pi \cdot V_{in,rms} \cdot V_o} - \frac{{P_o}^2}{{V_o}^2}} \tag{4.22}$$

4.2.3 Semiconductor losses

The method employed in this project for calculating the semiconductor losses is based on a lookup table approach. This is because the simulation conducted in PLECS and the steady state waveform generated using MATLAB scripts rely on the ideal switch concept.

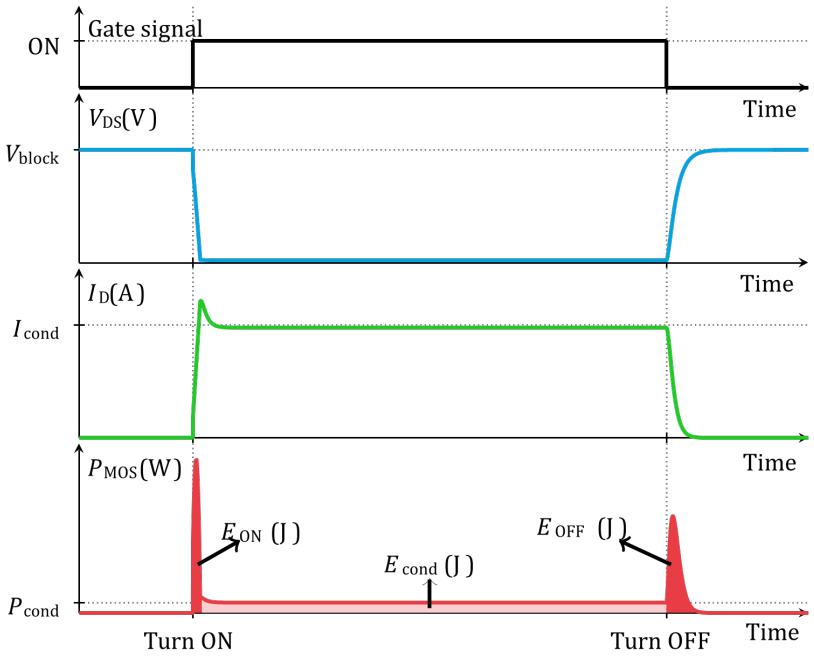


Figure 4.7: Switching and conduction losses in semiconductor devices[22].

The conventional method of computing the losses using the simulated waveform of the current and voltage across the device requires an accurate physical device model and calibrated model parameters, which can be challenging to obtain. Additionally, this method is time-consuming due to the necessity of using a small time step to resolve switching transients. To maintain simulation speed while still conducting loss analysis, an alternative approach for calculating switching losses is adopted, a concept that is currently utilised in PLECS[22].

The turn-on and turn-off transients are compressed on the time axis to an indefinitely short interval in order to employ the ideal switch approach for thermal simulations. The pulse must be infinitely high in order to preserve the switching losses (which correspond to the areas E_{ON} and E_{OFF} in Figure 4.7. The resulting energy pulse is referred to as a "Dirac pulse" and the pulse's weighting factor corresponds to the switching loss of one switching transition. Figure 4.8 depicts a comparison of the two methods, with the lower image representing the method employed in this project. The method for calculating the weighting factor of the energy pulse (impulse magnitude) is detailed in the following paragraph.

A lookup table is used to determine the energy loss for each switching occurrence. The switching voltage V_{block} prior to the switching event, the junction temperature, and the current I_{cond} following the switching event are all described as functions of losses in this lookup table. The lookup table only contains a finite number of data points, but simulations can produce nearly any result for current or voltage. In these circumstances, the two closest neighbors in the lookup table are used to build a linear interpolation.

Because the product of voltage and current is constantly known, calculating conduction losses during a simulation is easier. A forward conduction characteristic, where the on-

state voltage is presented as a function of current, is used to represent the conduction losses in a 2D lookup table. The instantaneous conduction loss in Watts is calculated at each simulation step by looking up the voltage for a specific current and junction temperature, and then multiplying that result by the current.

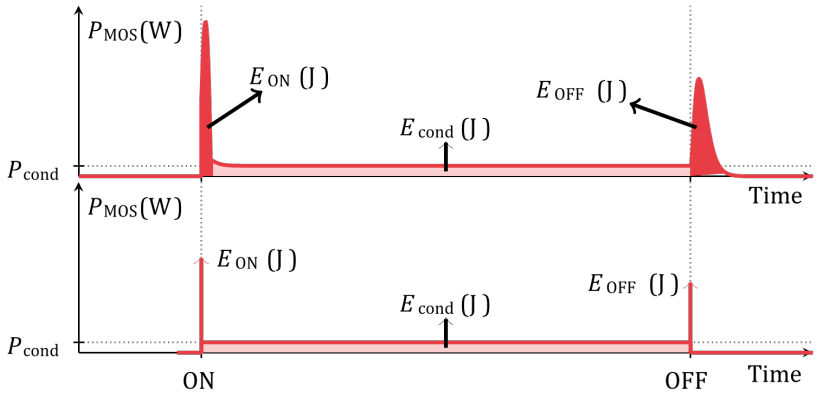


Figure 4.8: Conventional (top) and Dirac pulse (bottom) approach for calculating switching loss in semiconductor devices[22].

Once the instantaneous conduction loss and the weighting factor of the energy pulse (impulse magnitude) during turn on and off is obtained from the lookup table, the following procedure in Figure 4.9 is performed to get the total losses for the semiconductor device.

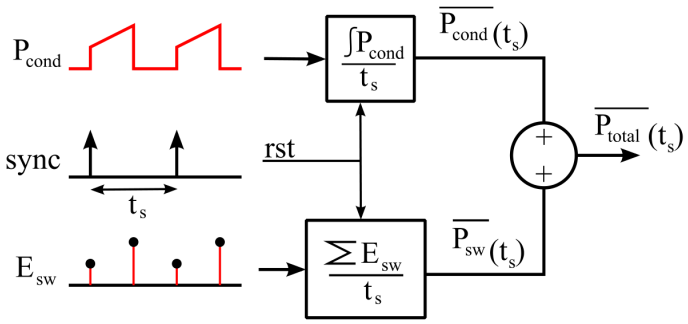
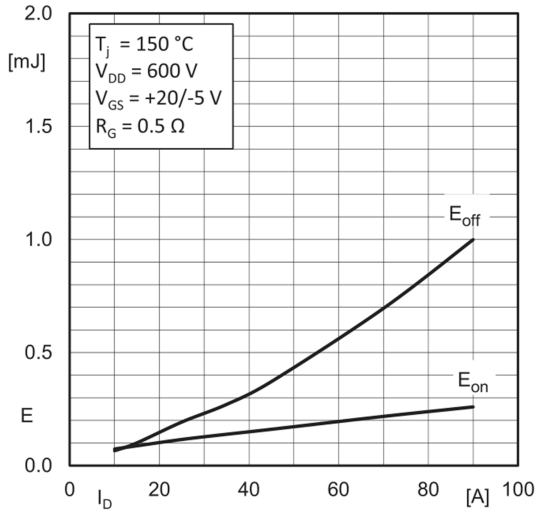


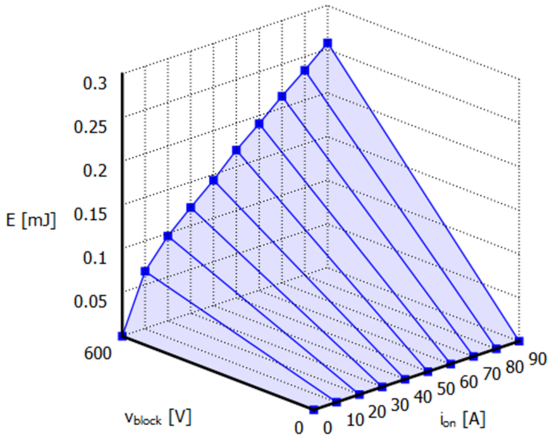
Figure 4.9: Switching and conduction losses calculation in semiconductor devices[22].

The various semiconductor losses in the PFC boost converter are

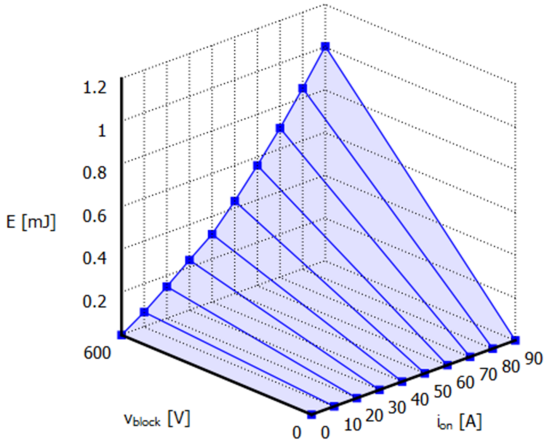
1. $P_{sw,module}$ - the switching loss of SiC MOSFET Module (SK45MLET12SCp), which is calculated from Figure 4.10 by getting the required turn-on and turn-off energy.



(a) E_{ON} [mJ],E_{OFF} [mJ] – I_D [A] modelled in Datasheet



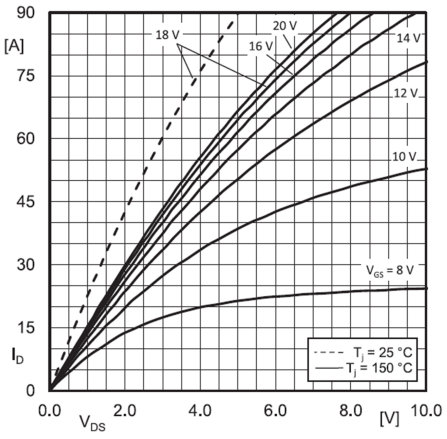
(b) E_{ON} [mJ] – I_D [A] modelled in PLECS



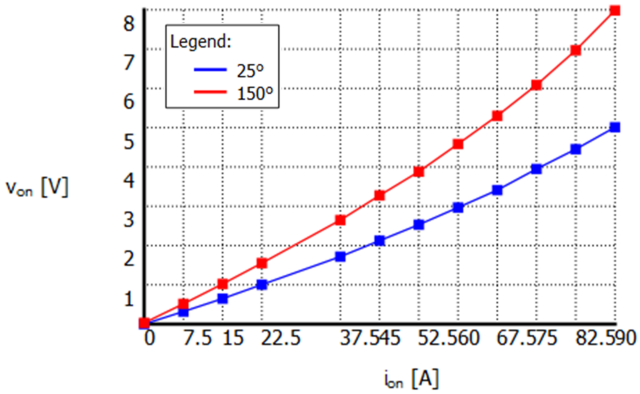
(c) E_{OFF} [mJ] – I_D [A] modelled in PLECS

Figure 4.10: (a) Turn on and Turn off energy for SK45MLET12SCp Module from SEMIKRON (b) Turn on energy modelled in PLECS (c) Turn off energy modelled in PLECS.

2. $P_{cond,MOS}$ - conduction loss of the MOSFET in SK45MLET12SCp,
which is calculated by getting the corresponding drain source voltage across the MOSFET for the current through the MOSFET with the help of graphs in Figure 4.11.



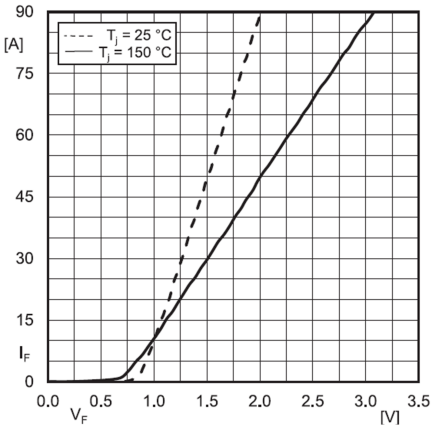
(a) V_{DS} [V]– I_D [A] modelled in Datasheet



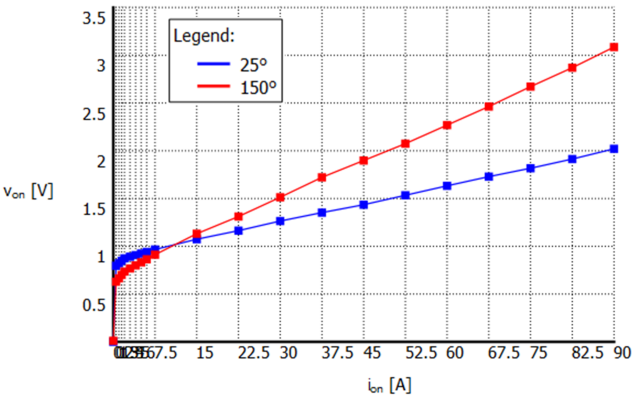
(b) V_{DS} [V]– I_D [A] modelled in PLECS for a gate voltage of 18V

Figure 4.11: Forward output characteristics of MOSFET in SK45MLET12SCp Module, used for computing conduction losses.

3. $P_{cond,diode}$ - conduction loss of the boost diode in SK45MLET12SCp, which is calculated by getting the corresponding forward voltage drop across the diode for the current through the diode with the help of graphs in Figure 4.12.



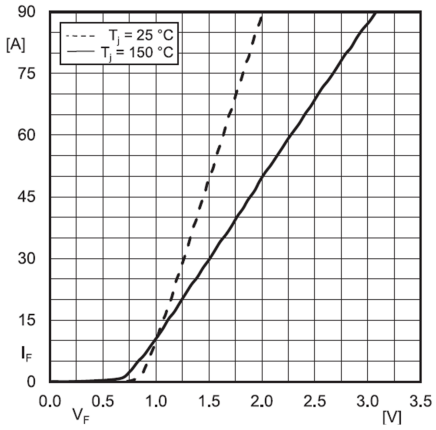
(a) V_F [V]– I_F [A] modelled in Datasheet



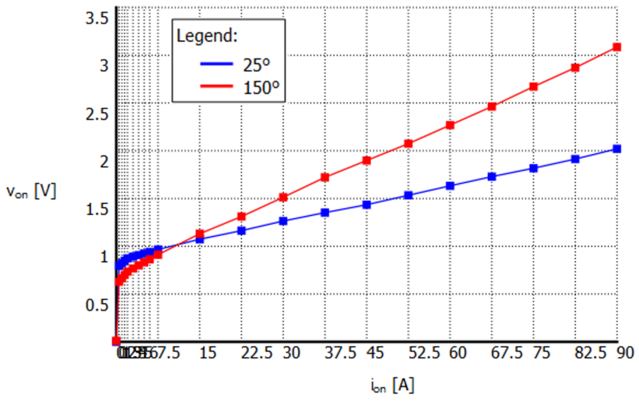
(b) V_F [V]– I_F [A] modelled in PLECS

Figure 4.12: Forward output characteristics of boost diode in SK45MLET12SCp Module, used for computing conduction losses.

4. $P_{cond,bridge}$ - conduction loss of the diodes in the GBJ5010 bridge rectifier, which is calculated by getting the corresponding forward voltage drop across the diode for the current through the diode with the help of graphs in Figure 4.13.



(a) V_F [V]– I_F [A] modelled in Datasheet



(b) V_F [V]– I_F [A] modelled in PLECS

Figure 4.13: Forward output characteristics of diode in GBJ5010 bridge rectifier module, used for computing conduction losses.

4.2.4 Losses and efficiency comparison for CCM, QCM, and DCM

The simulation is conducted for CCM, QCM, and DCM which was designed in Table 2.1, using the MATLAB script after designing the boost inductor and optimising it for the least volume. The average loss in each component is calculated, which is summed up to obtain the average total loss $P_{loss,tot}$ in one line cycle of input voltage. Efficiency (η) is then calculated as,

$$\eta = \frac{P_o}{P_o + P_{loss,tot}} \tag{4.23}$$

The results are then tabulated in Table 4.1. The boxed volume of the boost inductor is the largest for CCM since the inductance value is higher due to less ripple of the inductor current. The effect of the current ripple is also seen in the core loss, which is highest for DCM where the ripple is maximum. Copper loss is higher for CCM due to the increased winding resistance resulting from higher inductance and number of turns. Switching loss is highest for DCM. Although DCM mode benefits from zero current turn-on for the MOSFET, the turn-off is not at zero current, and the current during turn-off in DCM is larger compared to other modes due to the high ripple. This leads to higher turn-off energy in DCM, resulting in slightly higher switching losses. Conduction losses of diodes and MOSFETs are highest for DCM. CCM exhibits the highest efficiency. The EMI filter volume is highest for DCM (since DCM has the lowest f_c). Therefore, even though design for DCM gives less volume for boost inductor, its efficiency is lower, and the filter volume is higher. This indicates that the selection of modulation technique and its parameters, such as k_{ripple} for CCM and α for QCM, need further optimization to find the right balance between boost inductor volume, efficiency, and EMI filter volume.

Mode	CCM	QCM	DCM
Inductance value, L [μH]	1350	229	100
Current at which L is designed, I_{design} [A]	11.13	10.65	15
Core with minimum volume	58778	58089	58254
Number of turns	65	41	29
Boxed Volume of one inductor [cm^3]	209	52	38
Core loss, boost inductors, P_{core} [W]	6	43	56
Copper loss, boost inductors, $P_{cu,dc}$ [W]	19	8	9
Output capacitor loss, P_{Cdc} [W]	21	21	21
Switching loss, SiC Module, $P_{sw,module}$ [W]	4	5	6
Cond. loss, MOSFETs, $P_{cond,MOS}$ [W]	5	6	13
Cond. loss, boost diodes, $P_{cond,diode}$ [W]	20	20	22
Cond. loss, bridge diodes, $P_{cond,bridge}$ [W]	58	59	67
Total losses, $P_{loss,tot}$ [W]	133	162	193
Efficiency, η [%]	98.23	97.85	97.44
EMI noise simulation results			
Filter design frequency f_D [kHz]	180	180	180
Quasi peak at f_D, $U_{QP,\max}(f_D)$ [dBμV]	119	136	144
Attenuation required at f_D, $Att_{req,db}(f_D)$ [dB]	59	76	144
Filter cut-off frequency, f_c [kHz]	32	20	16

Table 4.1: Summary of comparison of losses and efficiency and EMI simulation results for three stages interleaved PFC converter for P_o = 7360 W, V_o = 400 V, $V_{in,rms}$ = 230 V and f_{sw} = 20 kHz.

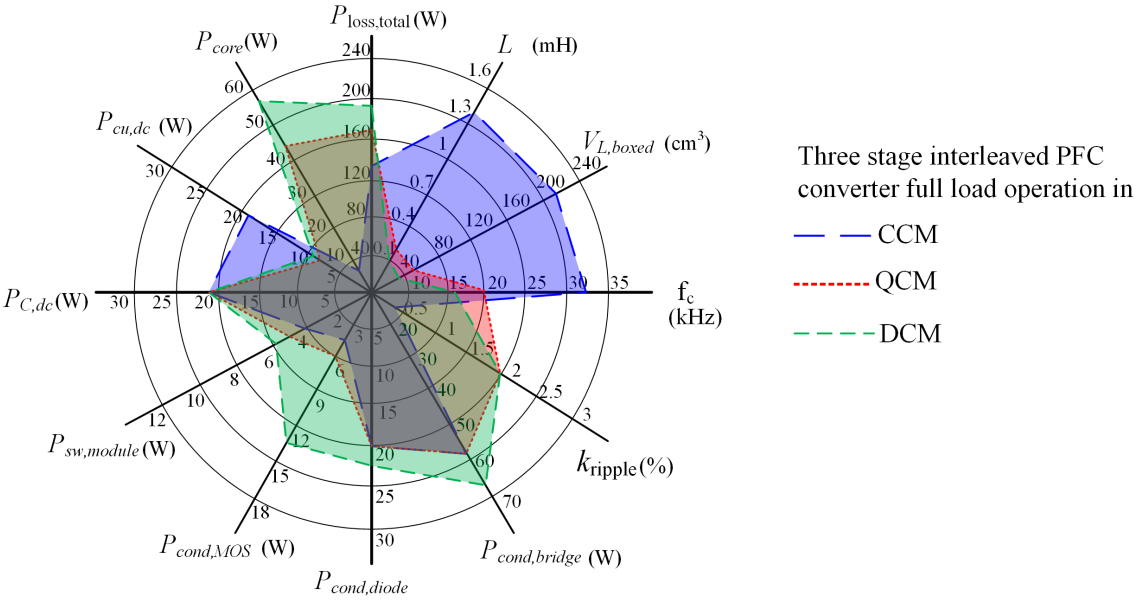


Figure 4.14: Summary of comparison of losses and efficiency and EMI simulation results for three stages interleaved PFC converter for P_o = 7360 W, V_o = 400 V, $V_{in,rms}$ = 230 V and f_{sw} = 20 kHz for CCM(k_{ripple} = .4), QCM (α = 45°) and DCM (α = 90°).

Chapter 5
Optimisation of Interleaved Boost PFC

In order to evaluate and optimise the overall performance of the interleaved PFC converter, additional theoretical and simulation analyses are conducted. Optimisation of a three stage interleaved PFC is performed to improve the power density, efficiency, and EMC performance. This optimisation process involves analysing the following influential factors:

- Current modulation techniques (CCM, QCM and DCM).
- Optimum k_{ripple} for CCM and α for QCM.
- Phase shedding of interleaved stages.
- Phase shift control of interleaved stages.
- Switching frequency variation.

5.1 Optimum core selection for boost inductor

The different parameters taken into account for optimising the boost inductor core for improving the power density, efficiency, and EMC performance of the interleaved PFC converter are,

- Type of the core (Toroidal cores from Magnetics of the type Kool Mμ, MPP, Kool Mμ MAX, Kool Mμ HF, Edge, High Flux, and XFlux are considered)
- Number of layers of winding (N_L).
- Number of stacked cores (N_C).
- Permeability (μ) of the core (μ= 60 and 125 is considered).
- Ripple factor of the current (k_{ripple}) for CCM operation.
- Boundary angle (α) for QCM.

The mentioned parameters are varied, and the consequent outcomes, including boost inductor volume, total losses, and EMI filter cut-off frequency, are assessed for each combination. This meticulous evaluation process aids in identifying the most optimal configuration.

5.1.1 Selection of optimum core for CCM by varying ripple factor

In this section, the ripple factor of the current k_{ripple} for CCM operation is varied to obtain different values of inductance for the boost inductor. Subsequently, these inductors are designed with different possible core configurations, permeabilities, and materials and the core with least volume is selected for each k_{ripple} in each configuration.

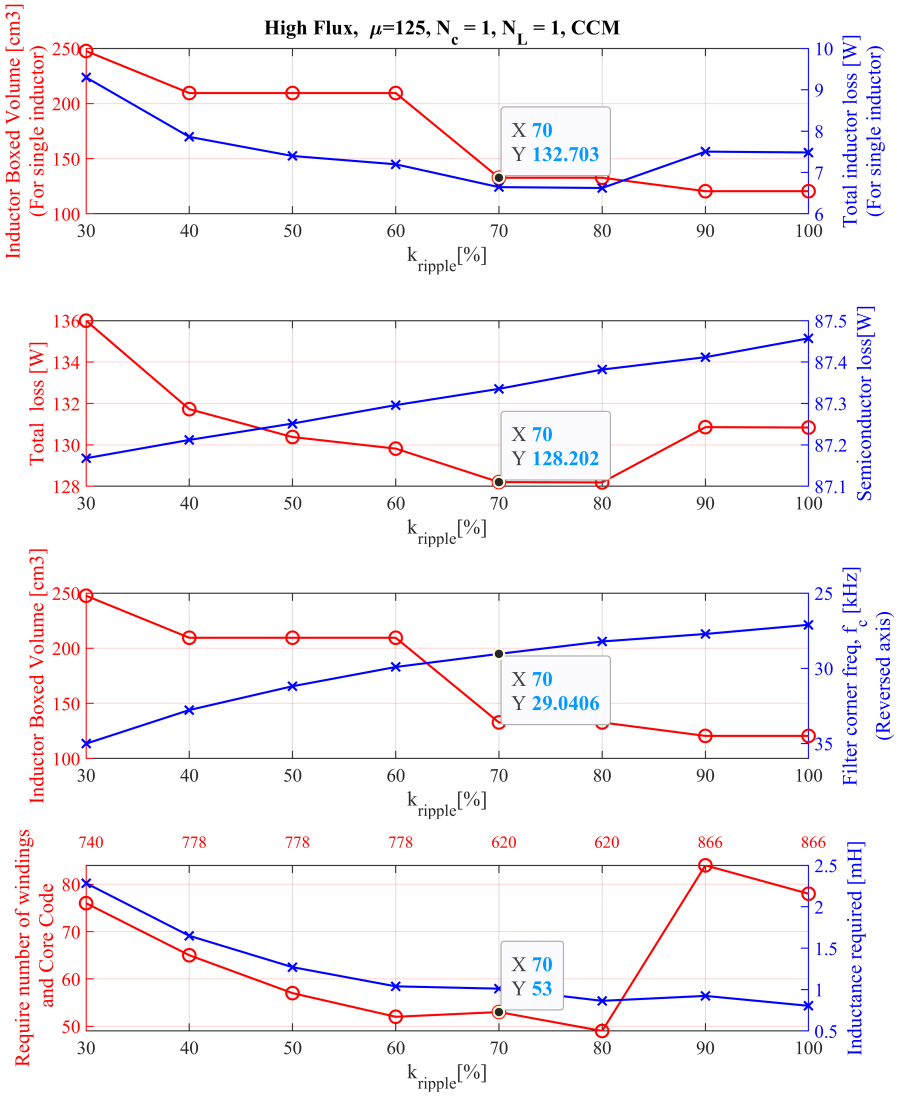


Figure 5.1: Variation of boost inductor volume, total losses, inductor losses, filter cut-off frequency with k_{ripple} for CCM operation for High flux cores with N_C=1, N_L=1, μ=125.

A specific core configuration is depicted in Figure 5.1. This figure illustrates the variation of boost inductor volume, total losses, inductor losses, and filter cut-off frequency with k_{ripple} for CCM operation for High flux cores with N_C=1, N_L=1, μ=125. The steps that are implemented in MATLAB script to get this required plot are,

1. The core configuration under consideration is chosen.
2. For a k_{ripple} starting from 10%, the inductance value is calculated for CCM operation using Equation (2.10). The value of I_{design} is chosen as the maximum current at the design point of $D = 0.5$.
3. The boost Inductor is designed for every possible core with the chosen configuration as explained in Section 3.2.

4. The core that yields the minimum volume for the calculated inductance is selected.

5. Utilising the selected boost inductor design, simulation is conducted using MATLAB script developed to obtain steady-state current and voltage waveforms for the three stage interleaved boost converter.

6. Core loss and copper loss of the inductor, semiconductor losses, and capacitor losses are calculated as explained in Section 4.2. The total loss under full load condition is calculated.

7. EMI measurement and filter cut-off frequency calculation are performed as explained in Section 4.1.1

8. The value of k_{ripple} is incremented and steps from 2 to 8 is repeated until k_{ripple} reaches 100%.

It is evident that the boxed volume of a single inductor decreases with an increase in k_{ripple}. This is attributed to the fact that the required inductance value decreases as k_{ripple} increases. The total inductor loss exhibits an initial decrease, followed by reaching a minimum value, and subsequently increases. This behaviour arises from the fact that the core loss initially decreases with an increase in ripple current until they reach a minimum, while copper losses exhibit an increasing trend. The filter corner frequency decreases with an increase in k_{ripple}. In the graph, it is plotted on a reversed axis for comparison with the boxed volume of inductors. The larger the value of f_c, the smaller the volume. The optimum point selected in Figure 5.1 is k_{ripple} = 70. At this point, both total losses and volume are at their minimum, despite the EMI filter corner frequency being lower. Therefore, core 620 is chosen as the optimum result are for this configuration.

Similar analysis and selection of optimum core are carried out for each core configuration by varying k_{ripple}. The results are tabulated in Table 5.1 for single layer winding and Table 5.2 for multi layer winding. Where V_b is the boxed volume of a single inductor, P_L is the sum of copper and core loss of a single inductor, P_{tot} is the total loss of the PFC converter, f_c is the EMI filter cut-off frequency, N_C is the number of stacked cores, μ is the permeability of the core, and N_r is the number of windings.

SINGLE LAYER									
μ	N_C	Material	k_{ripple} [%]	V_b $[cm^3]$	P_L [W]	P_{tot} [W}	f_c [kHz]	Core code	N_r
60	1	Kool Mμ	80	247	8.93	135	28	740	73
		Kool Mμ MAX	80	209	8.26	133	28	778	66
		XFlux	80	209	12.8	146	28	778	61
		High Flux	60	247	9.32	136	30	337	71
		MPP	60	579	10.26	139	29	337	82
60	2	Kool Mμ	50	393	12	145	31	778	61
		KoolMuMAX	50	393	13.3	148	31	778	57
		XFlux	40	393	22.62	176	32	778	61
		High Flux	40	393	14	150	32	778	61
		MPP	40	393	12	144	33	778	65
125	1	Kool Mμ	80	247	9.53	138	31	102	99
		High Flux	70	132	6	128	29	620	53
		MPP	70	209	7.53	131	29	778	63
125	2	Kool Mμ	70	248	10.75	141	31	620	53
		XFlux	80	143	21	173	28	725	40
		High Flux	40	215	13	148	32	866	83
		MPP	40	393	13	149	32	778	49

Table 5.1: The optimum selected parameters for each core configuration in CCM for single layer winding.

The optimum core configuration in the Table 5.1 for a single layer is the High Flux core "58620" with μ=125 and N_C=1 since it has the least volume and losses. The filter cut-off frequency does not vary much for each configuration.

MULTI LAYER									
μ	N_C	Material	k_{ripple} [%]	V_b $[cm^3]$	P_L [W]	P_{tot} [W}	f_c [kHz]	Core code	N_r
60	1	Kool Mμ	70	166	9.4	137	29	620	99
		Kool Mμ MAX	60	166	8.54	133	29	866	89
		XFlux	60	125	11.8	144	30	109	159
		High Flux	60	125	10	138	31	109	145
		MPP	60	166	9.3	136	30.4	320	99
60	2	Kool Mμ	70	171	10	139	29	195	79
		KoolMuMAX	60	158	12.38	146	29	715	120
		XFlux	60	121	15	153	30	89	87
		High Flux	60	121	12	144	29	89	86
		MPP	60	171	9.7	138	30.83	195	77
125	1	Kool Mμ	60	257	9.48	138	32	778	91
		High Flux	60	129	7	130	31	866	78
		MPP	50	257	10	140	34	778	97
125	2	Kool Mμ	50	296	11	143	33	620	69
		XFlux	80	138	15	154	31	438	64
		High Flux	50	138	12	144	32	438	60
		MPP	70	248	10	140	31	620	45

Table 5.2: The optimum selected parameters for each core configuration in CCM for Multi layer winding.

The optimum core configuration in the Table 5.2 for multi layer is the High Flux core "58866 "with μ=125 and N_C=1 , since it is one among those with the least volume and losses. The filter cut-off frequency does not vary much for each configuration. Other cores with smaller boxed volume are not selected due to higher inductor losses associated with them Additionally, in other cores, ones with double stacked configuration tends to be more costly, and the high frequency behavior of single stack is better as demonstrated in Section 5.2.

Now when the optimum selection from single layer and multi layer is to be performed, High Flux core "58620" with μ=125 and N_C=1, k_{ripple} = 70%, single layer is the most optimum choice as it has better high-frequency behavior than the multi-layer option. Also, other parameters like losses and filter cut-off frequency are almost the same. The chosen optimum design of the inductance is shown in Figure 5.2

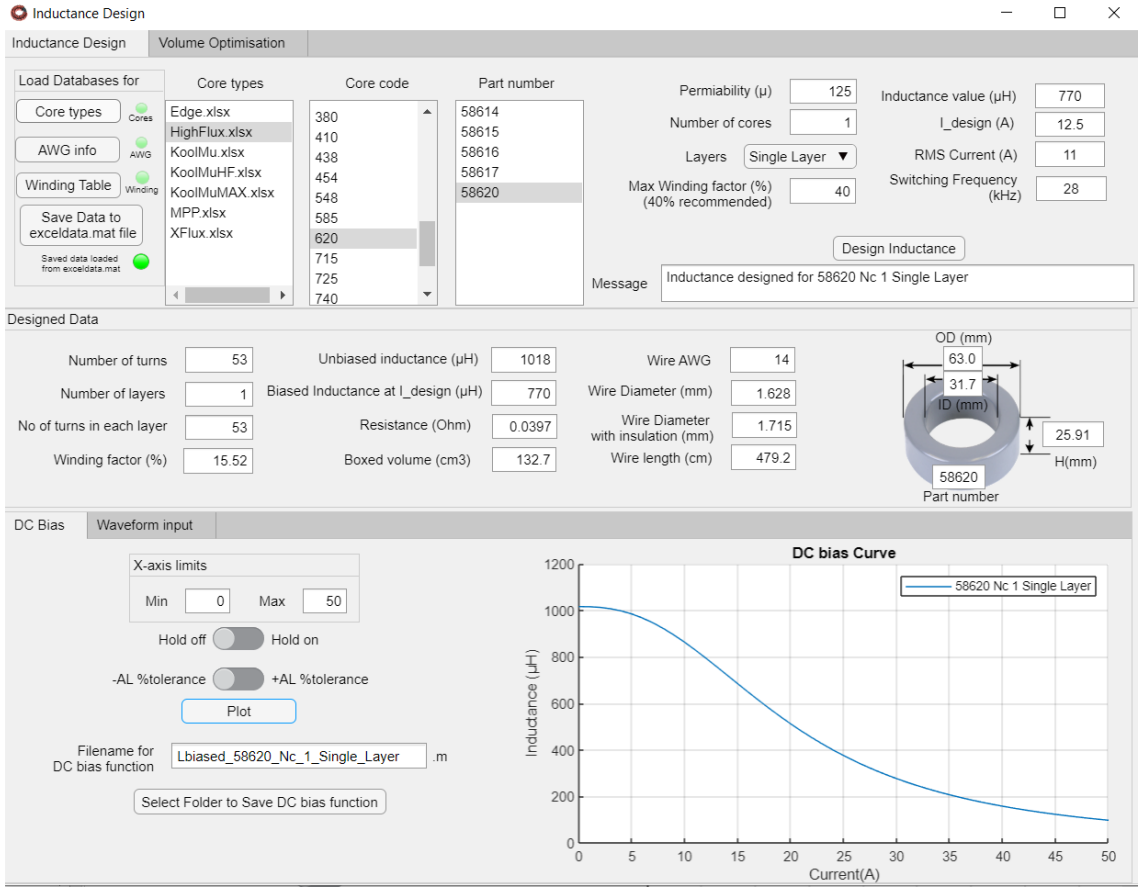


Figure 5.2: The optimised design for boost inductor in CCM operation for a three stage interleaved converter with specs in Table 1.1 .

5.1.2 Selection of optimum core for QCM by varying boundary angle

In this section the boundary angle α at which conduction mode changes from DCM to CCM in a QCM operation, is varied to get different values of inductances. These inductances are designed with different possible core configurations, permeability, and materials. The procedure for optimisation is the same as in the Section 5.1.1, the only differences being, α is changed instead of k_{ripple} to get different inductances and I_{design} is taken as half of the peak to peak inductor current at the design point α. A specific core configuration is shown in Figure 5.3. Here variation of boost inductor volume, total losses, inductor losses, and filter cut-off frequency with α for QCM operation for High flux cores with N_C=1, N_L=1, μ=125 is shown.

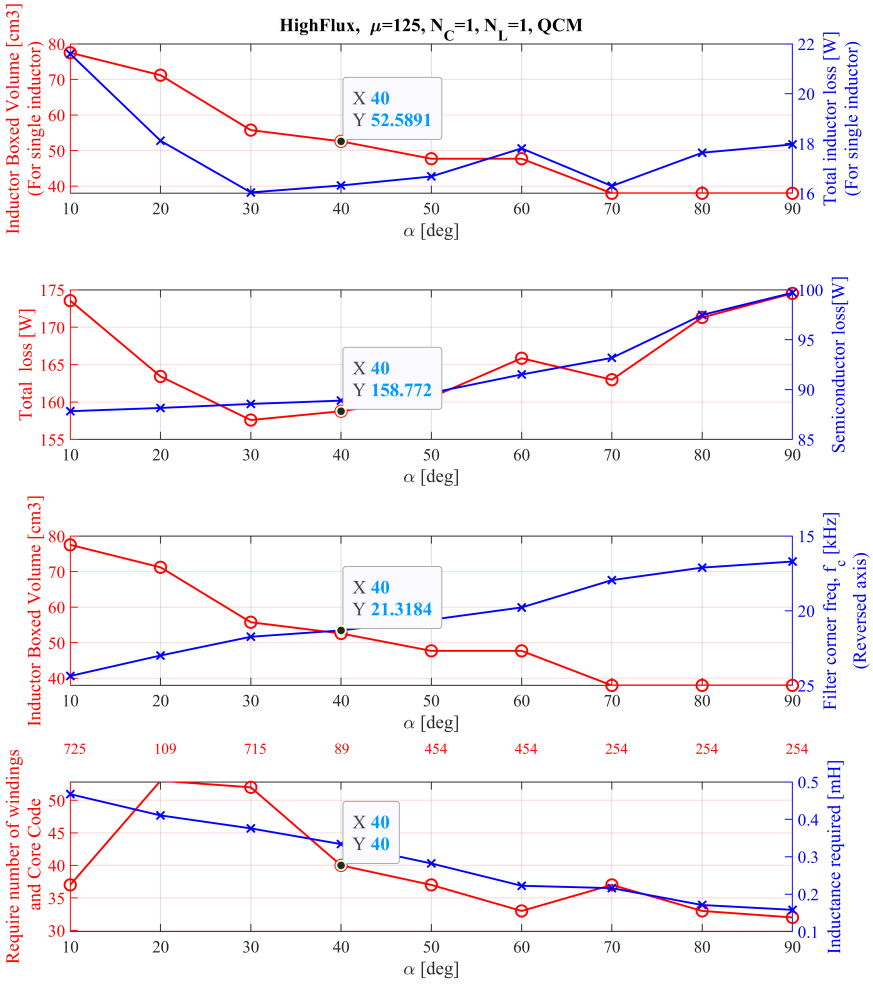


Figure 5.3: Variation of boost inductor volume, total losses, inductor losses, filter cut-off frequency with α for QCM operation for High flux cores with N_C=1, N_L=1, μ=125.

The observed trend indicates that the inductor boxed volume for a single inductor decreases as the α increases. This is attributed to the reduced requirement for inductance as α is raised. The total loss decreases initially, reaches a minimum value, and then increases. The optimum point selected in Figure 5.1 is α = 40. This selection is made after a thorough consideration of factors including inductor volume, total loss, and filter cut-off frequency. Consequently, the High Flux core 58089, featuring parameters μ=125 , N_C=1 and N_L=1, is determined to be the most suitable choice for this configuration.

Similar analysis and selection of optimum core is carried out for each core configuration by varying α and the results are summarised in Table 5.3 for single layer winding and Table 5.4 for multi layer winding.

SINGLE LAYER									
μ	N_c	Material	α [deg]	V_b $[cm^3]$	P_L [W]	P_{tot} [W}	f_c kHz	Core code	N_r
60	1	Kool Mμ	60	77	8	136	20	725	39
		Kool Mμ MAX	50	77	9.6	139	21	725	39
		XFlux	50	71	23.8	182	21	109	56
		High Flux	50	71	13.3	151	22	109	57
		MPP	50	77	8	135	21	725	40
60	2	Kool Mμ	40	99	17	162	21	715	52
		Kool Mμ MAX	40	86	25	186	22	454	39
		Kool Mμ HF	60	68	14	157	20	254	39
		XFlux	40	71	86	325	22	454	37
		High Flux	40	87	39	229	22	454	37
		Edge	60	68	38	229	21	254	33
		MPP	40	95	20	171	22	89	44
125	1	Kool Mμ	60	77	8	135	21	725	38
		XFlux	40	60	19	166	20	715	38
		High Flux	40	52.6	16	159	21	89	40
		MPP	20	71	9.5	141	20	109	58
125	2	Kool Mμ	50	87	17	164	22	89	39
		XFlux	20	68	62	295	21	254	37
		High Flux	50	43	51	266	19	324	34
		MPP	20	68	27	193	20	254	39

Table 5.3: The optimum selected parameters for each core configuration in QCM for single layer winding.

The optimum cores in the Table 5.3 for single layer are High Flux core "58089" with parameters μ=125 and N_C=1 and High Flux core "58324" with parameters μ=125 and N_C=2. Upon comparison, it is evident that High Flux core "58089" with N_C=1 exhibits lower total loss and a higher cut-off frequency, despite having a larger boxed volume compared to High Flux core "58324" with two stacked cores. In addition to this, utilising two stacked cores increases the cost.

The optimum core in the Table 5.4 for multi layer configuration is the same as in the case with the single layer, which is High Flux core "58089" with μ=125.

MULTI LAYER									
μ	N_c	Material	α [deg]	V_b $[cm^3]$	P_L [W]	P_{tot} [W}	f_c kHz	Core code	N_r
60	1	Kool Mμ	60	65	7.5	134	20	454	64
		Kool Mμ MAX	60	53	8.5	137	19	254	65
		Kool Mμ HF	70	53	7	134	18	254	66
		XFlux	30	53	12	146	21	254	69
		High Flux	30	53	9	136	22	254	70
		Edge	30	53	8	132	22	254	67
		MPP	10	65	8	134	20	454	69
60	2	Kool Mμ	10	89	14	154	22	254	58
		Kool Mμ MAX	40	59	20	172	21	324	63
		Kool Mμ HF	60	59	14	156	20	324	58
		XFlux	20	59	35	216	23	324	63
		High Flux	50	49	28	197	20	585	63
		Edge	40	49	21	174	21	585	64
		MPP	70	59	17	163	19	324	63
125	1	Kool Mμ	60	78	8	135	21	725	38
		XFlux	40	60	19	167	21	438	38
		High Flux	40	52.6	16	159	21	89	40
		MPP	20	71	9.5	141	20	109	58
125	2	Kool Mμ	50	87	17	164	22	454	39
		XFlux	20	68	62	295	21	254	37
		High Flux	20	68	46	248	23	254	36
		MPP	20	68	27	193	20	254	39

Table 5.4: The optimum selected parameters for each core configuration in QCM for multi layer winding.

To observe the effect of high frequency model in EMI noise simulation and EMI filter design for the optimally selected cores in single layer, multi layer, single stacked, and multi stacked configurations for QCM operation, a case study is presented in the next section.

5.2 Case study: Comparison of high frequency model, DC bias curves, and EMI simulation

The inductor can be wound in different configurations to achieve the same design parameters. These configurations involve various combinations of the number of winding layers(N_L) and the number of stacked cores (N_C). A specific design parameter has been chosen for this case study, which can be used to effectively compare the optimised configurations discussed in the previous section. The inductor is designed with different configurations using the optimised cores from the previous section (58089 and 58324) to achieve the same design parameter inductance L_{design} of 200 μH at an I_{design} of 9A as shown in Figure 5.4.

- Case 1: 58089 single layer 1 stack (N_L = 1, N_C = 1).
- Case 2: 58324 single layer 2 stack (N_L = 1, N_C = 2).
- Case 3: 58324 multi layer 1 stack(N_L = 2, N_C = 1).

In Case 1, the number of turns of windings (N_r) after design in is 36 turns, which is similar to the 40 turns in the optimised core 58089). In Case 2. N_r is 32 turns, similar to 34 turns the two stack optimised core of 58324. The multi layer winding in Case 3 has an N_r of 51 turns, with 28 turns in the inner layer and 23 turns in the outer layer.

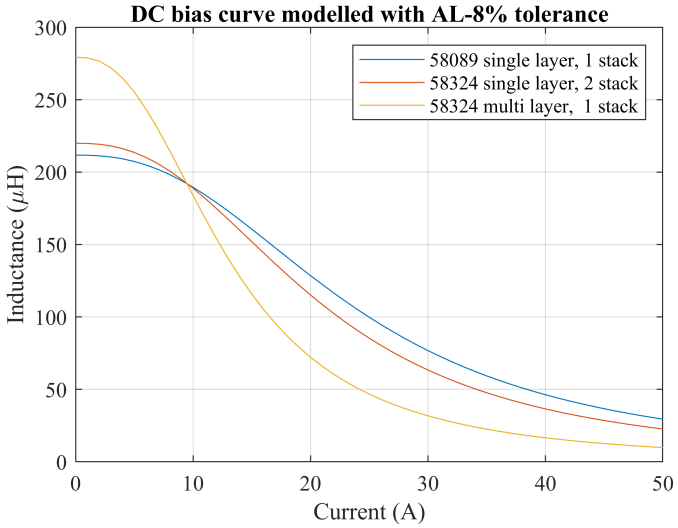


Figure 5.4: Comparison of DC bias curves, numerically modelled for the three cases.

The DC bias curves of three cases numerically modelled for A_L-8% are compared in Figure 5.4. It can be observed that in all three cases, the DC bias curve passes through the design point of L_{design} of 200 μH at an I_{design} of 9 A. This result has been verified through measurements using the DPG power choke tester, as depicted in Figure 5.6.

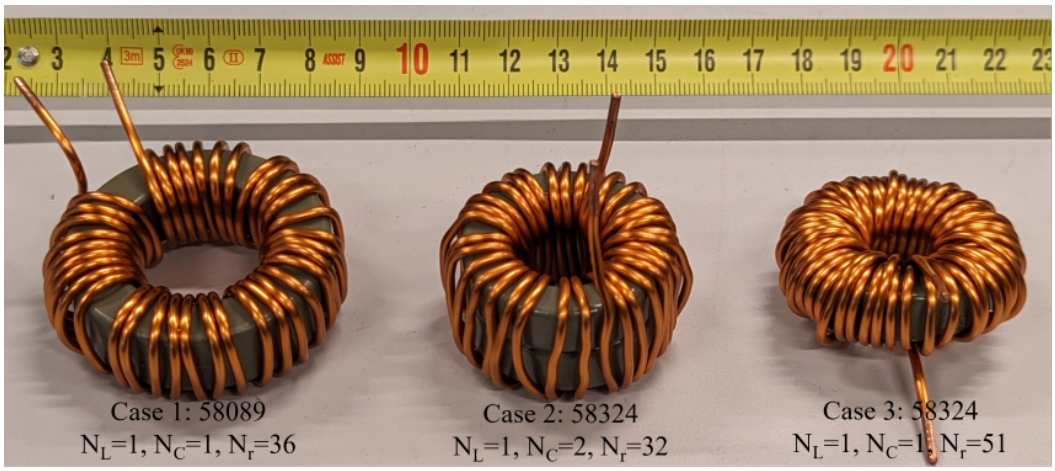


Figure 5.5: Inductors tested with high frequency impedance analyser and power choke tester.

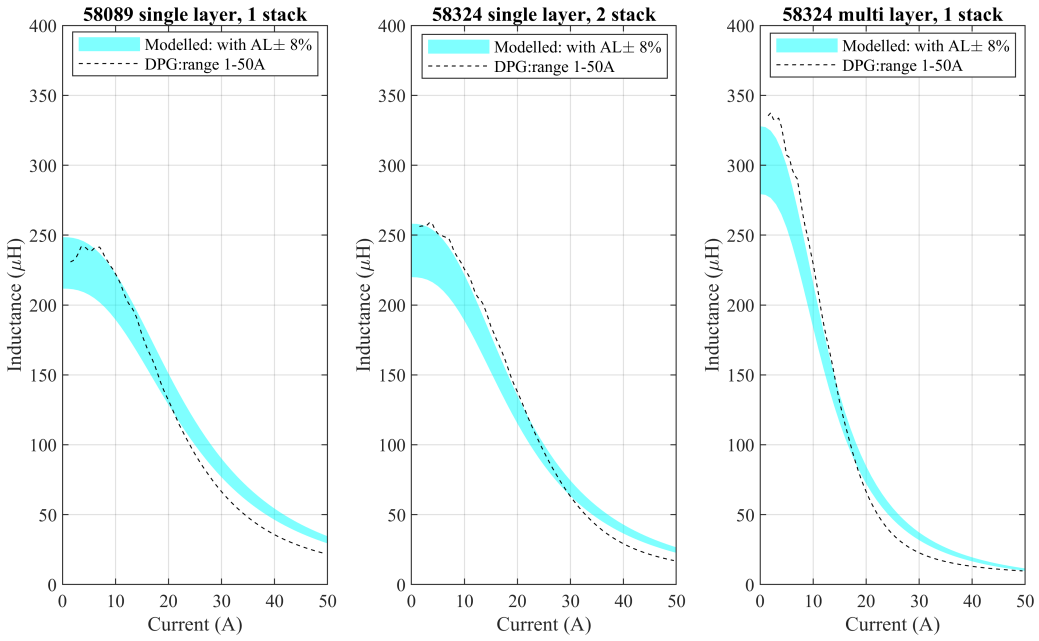


Figure 5.6: Comparison of DC bias curves from DPG and numerically modelled curves for the three cases.

The high frequency modelling of the toroidal core inductor is depicted in Figure 5.7, where L represents the inductance, C_p is the parasitic capacitance, R_s is the equivalent series resistance, and R_p is the resistance of the core. The high frequency impedance for the three cases was extracted using a series impedance analyzer and DC bias unit from Wayne Kerr Electronics(Figure D.2). The result with 9A DC bias is shown in Figure 5.8.

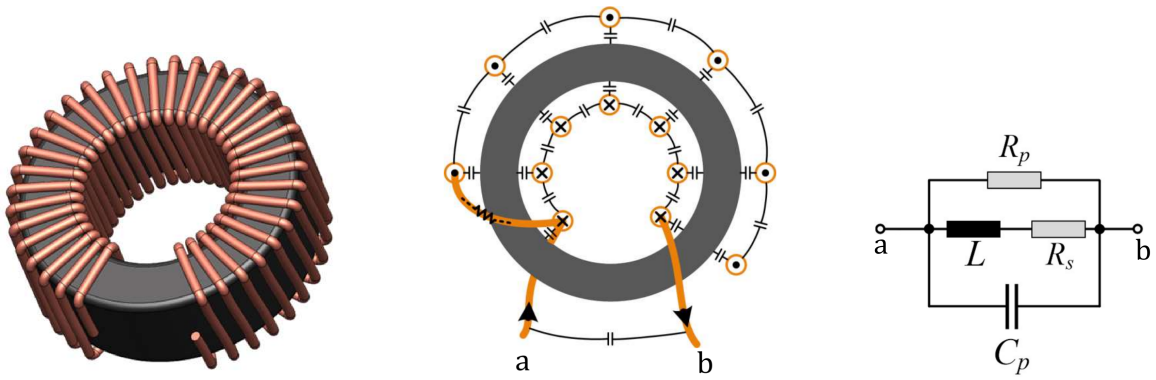


Figure 5.7: Modeling of a physical inductor with an equivalent circuit.

These inductors are modeled with the equivalent circuit for high frequency using the impedance curves for 0 A bias and 9 A bias. The high frequency model is tabulated in Table 5.5.

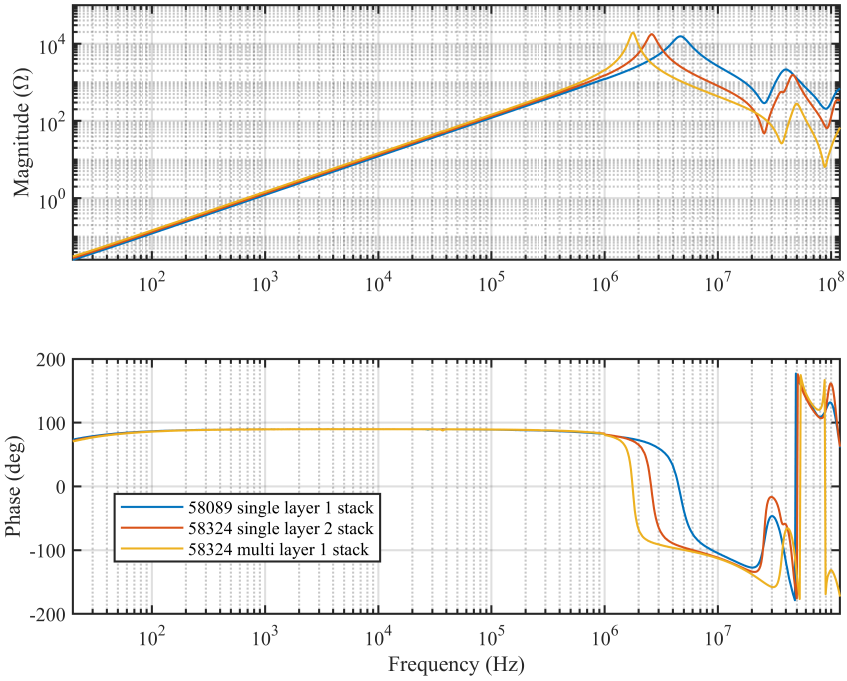


Figure 5.8: The high frequency impedance curve of the three cases with 9A DC bias measured with impedance analyzer and DC bias unit from Wayne Kerr Electronics.

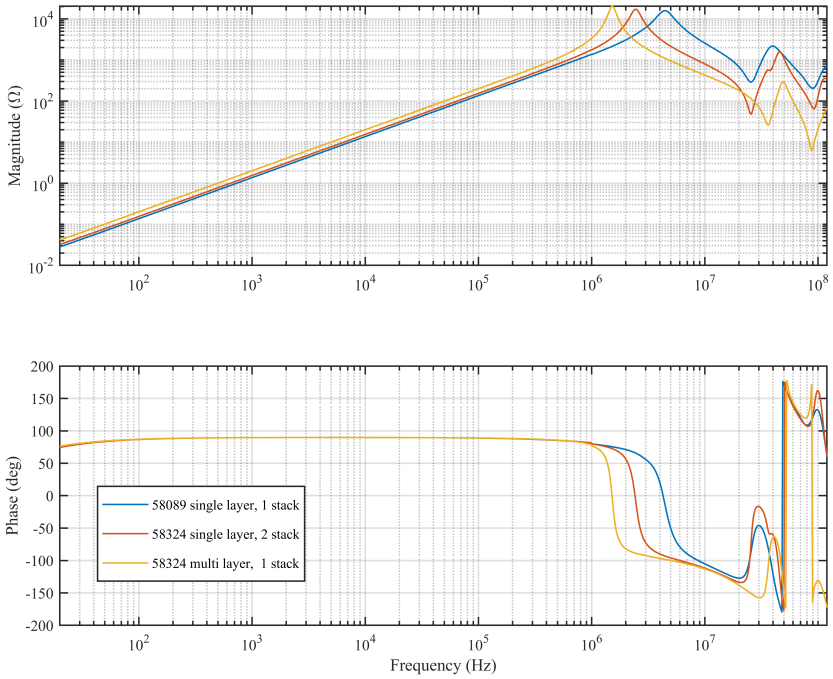


Figure 5.9: The high frequency impedance curve of the three cases with 0A DC bias measured with impedance analyzer and DC bias unit from Wayne Kerr Electronics.

Case	Case 1	Case 2	Case 3
Inductance value, L_{design} $[\mu H]$	200	200	200
I_{design} [A]	9	9	9
Core chosen	58089	58324	58324
Number of layers	1	1	2
Number of cores	1	2	1
Number of turns	36	32	51
Unbiased inductance $[\mu H]$	212	220	280
Boxed Volume $[cm^3]$	52.6	43.4	37
First positive peak $[MHz]$	4.71	2.62	1.77
High frequency model with 0 A bias			
L $[\mu H]$	216.4	245.4	318
C_p $[pF\}$	5.94	16.8	34.5
R_s $[m\Omega]$	.96	1.3	1.5
R_p $[k\Omega]$	15.85	17.15	20.47
High frequency model with 9 A bias			
L $[\mu H]$	192.35	211.6	231.3
C_p $[pF\}$	5.94	17.42	34.77
R_s $[m\Omega]$	1.1	1.5	1.9
R_p $[k\Omega]$	15.5	17.6	19.32

Table 5.5: Comparison of high frequency model of three cases.

It can be observed that in Case 1, which involves a 58089 core with a single layer and one stack, the minimum value for C_p is achieved. In Case 2, where a 58324 core with a single layer and two stacks is used, C_p is three times greater than that of Case 1. In Case 3, employing a 58324 core with a multi-layer and one stack, C_p is six times larger than that of Case 1. This trend is also evident in the impedance analyzer waveform presented in Figure 5.8, where the first positive peak for Case 1 occurs at 4.71 MHz, while for Case 2 and Case 3, it appears at lower frequencies.

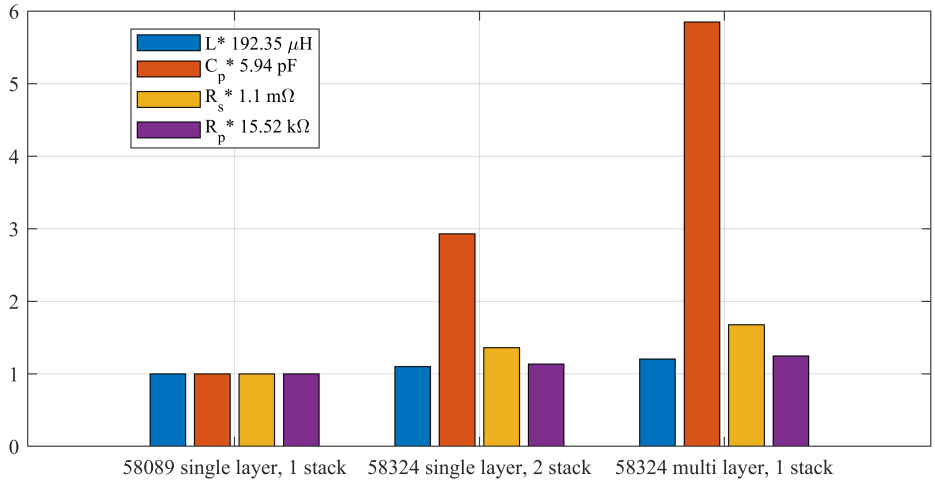


Figure 5.10: Comparison of parameters (L, C_p, R_s and R_p) of high frequency model of inductors from 3 cases.

This observation demonstrates that, despite the reduction in volume for Case 2 and Case 3, their high-frequency behavior is inferior to that of Case 1. It is evident that the inductance values modeled at 0A, based on the data from the impedance analyzer, match the unbiased inductance. Additionally, the inductance values modeled at 9A align with the designed inductance at I_{design}.

5.2.1 EMI simulation at full load

The boost inductors designed in all three cases are simulated using a MATLAB script. Subsequently, EMI noise simulations were conducted after incorporating the high frequency model of the inductors, and the results are shown in Figure 5.11. The resonant frequencies of the inductors observed in Figure 5.8 are also visible in the EMI simulation. It is evident that the high frequency performance of Case 1, with a single layer and single stack of 58089, is better, whereas Case 3 with a multi-layer, and single stack is worse. This establishes that reducing parasitic capacitance can lead to a reduction in EMI noise level at high frequencies [23].

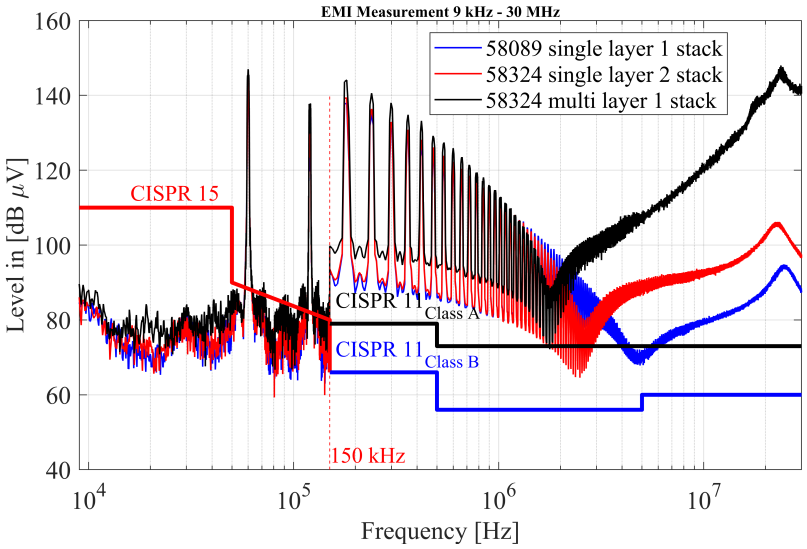


Figure 5.11: Conducted emissions in the range 9 kHz - 30 MHz for three stage interleaved PFC converter including high frequency model of boost inductout, without EMI filter, operating in QCM at full load (7360 W), 20kHZ switching frequency.

EMI filter is designed to meet CISPR 11 Class B standards and EMI simulation is performed again with the effect of connecting EMI filter considered. The results are in Figure 5.12.

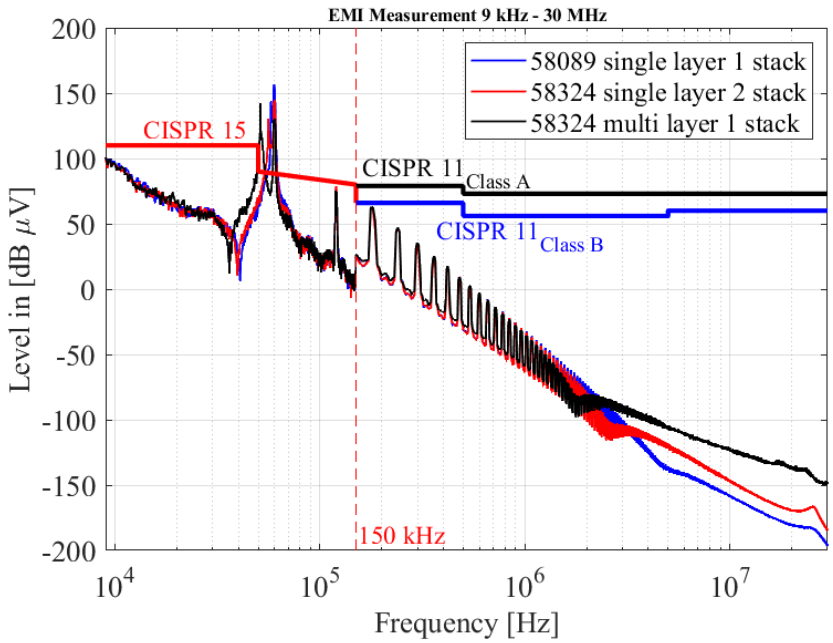


Figure 5.12: Conducted emissions in the range 9 kHz - 30 MHz for three stage interleaved PFC converter with EMI filter, operating in QCM at full load (7360 W), 20kHZ switching frequency.

This case study benefitted in selecting the single layer single stack configuration for further study in the case of QCM operation. Thus the optimum inductor for QCM operation is selected as with 40 turns of winding in single layer on single stacked High Flux core 58089.

5.3 Phase shedding with different phase shifts and switching frequency

The phase shedding technique is employed to enhance the efficiency of multiphase converters like interleaved PFCs, which consist of n_{stage} units operating in parallel. This method involves disconnecting specific units when the load decreases beyond a certain threshold, and it can be reversed by reintroducing units when the load rises.[24]. However, to achieve the least EMI filter volume and reduce EMI noise, the switching frequency and the phase shift (β) between the operation of interleaved stages of the boost converter must be selected carefully.

The phase shift of operation between the stages in an interleaved boost converter is conventionally selected as $360/n_{stage}$. However, conventional interleaving does not guarantee a reduction in the size of the DM EMI filter. Its effectiveness heavily relies on the switching frequency (f_{sw}) chosen, which defines the design frequency (f_D) for the EMI filter within the permitted range of 150 kHz to 30 MHz. With conventional interleaving control methods, a non-interleaved topology may have the same (f_D) as an interleaved one, resulting in no visible advantage in terms of minimising EMI filter size.

The order of harmonic of the switching frequency which gets canceled for different phase shifts (β) between the interleaved stages is summarised in Table 5.6.

No. of stages of interleaving n_stage	Phase shift (β) between interleaved stages	Order of harmonics which gets cancelled
2	180°	1, 3, 5, 7, 9, 11, ...
	90°	2, 6, 10, 14, 18, 20, ...
	45°	4, 12, 20, 28, ...
3	120°	1, 2, 4, 5, 7, 8, ...
	40°	3, 6, 12, 15, 21,24, ...

Table 5.6: The order of harmonic of the switching frequency which gets cancelled for different phase shifts and number of interleaved stages.

Range of fsw (kHz) $\frac{150}{n} \leq f_{sw} < \frac{150}{n-1}$	First occurring harmonic of f_{sw} after 150 kHz (n)	β_{opt} **for** n_{stage}**=2**	β_{opt} **for** n_{stage}**=3**
$150 \leq f_{\text{sw}} < \infty$	1	180°	120°
$75 \leq f_{\text{sw}} < 150$	2	90°	120°
$50 \leq f_{\text{sw}} < 75$	3	180°	40°
$37.5 \leq f_{\text{sw}} < 50$	4	45°	120°
$30 \leq f_{\text{sw}} < 37.5$	5	180°	120°
$25 \leq f_{\text{sw}} < 30$	6	90°	40°
$21.4 \leq f_{\text{sw}} < 25$	7	180°	120°
$18.75 \leq f_{\text{sw}} < 21.4$	8	180°	120°

Table 5.7: The order of harmonic of switching frequency which appears firstly after 150 kHz and the optimum phase shifts for various range of switching frequencies.

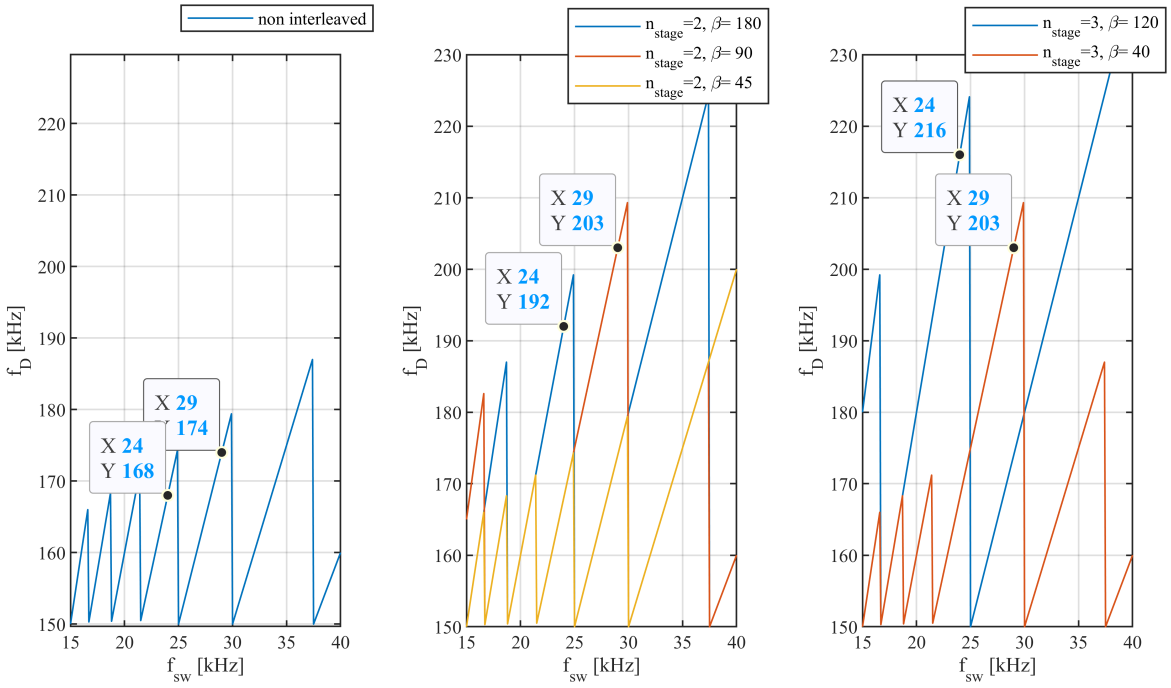
When designing the EMI filter for band B, the design frequency (f_D) for the EMI filter is selected as the first peak of the EMI measurement within the range of 150 kHz to 30 MHz. This frequency is n^{th} harmonic of the switching frequency f_{sw}, depending on the range of frequency, as summarised in the second column of Table 5.7.

If the switching frequency is in the range ($25 \leq f_{\text{sw}} < 30$), for example, 28 kHz, then 6th harmonic is the first peak appearing after 150kHz. When choosing a conventional phase shift, 6th harmonic is not cancelled in two stage and three stage interleaved converters. However, in the case of an unconventional phase shift of 90° for two stage interleaved and 40° for three stage interleaved, the 6th harmonic gets cancelled. Thus the first appearing peak in the EMI noise measurement will be the 7th harmonic which means the f_D is higher and consequently, the EMI filter volume can be reduced. With the data from Table 5.6 the optimum selection of phase shift (β) can be made for each switching frequency range so that the order of harmonic of the switching frequency first appearing after 150kHz cancels. This is summarized in Table 5.7.

From Equation (4.8), the relation between f_c and f_D is given as,

$$f_c = f_D \cdot \sqrt[2n_f]{Att_{req,LC}(f_D)} \tag{5.1}$$

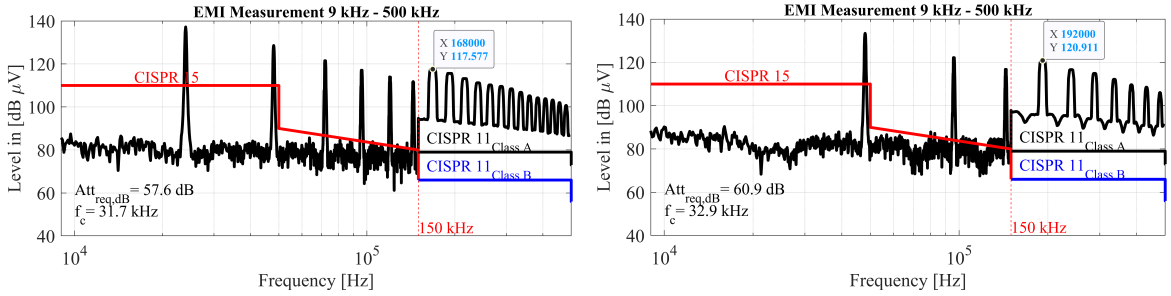
Now the filter design frequency f_D is computed for the range of switching frequencies of the interest and plotted to get a tentative idea of how f_c will vary for different phase shifts, interleaving and switching frequency.[25].



(a) n_{stage} = 1 **(b)** n_{stage} = 2 **(c)** n_{stage} = 3

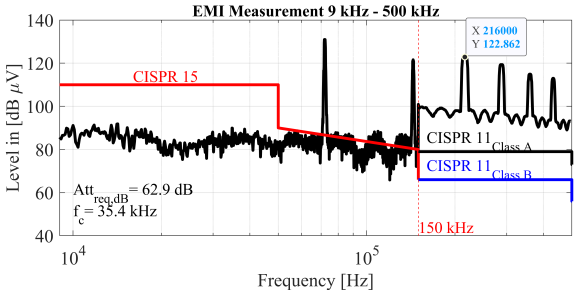
Figure 5.13: Variation of f_D for different stages of interleaving, phase shifts and switching frequency.

In the frequency range of 20 kHz to 30 kHz, the peak for f_D occurs at 24 kHz and 29 kHz, considering only integer values for switching frequency. As shown in Figure 5.13, it is evident that the optimum phase shift for $n_{stage} = 3$ is $\beta = 120°$, operating at a f_{sw} of 24 kHz, to achieve the highest f_D of 216 kHz. Meanwhile, the optimum phase shift for $n_{stage} = 2$ is $\beta = 90°$, operating at a f_{sw} of 29 kHz, yielding the highest f_D of 203 kHz. To confirm these computations and to check whether the trend for f_c follows the trend for f_D, EMI simulations were conducted for these frequencies, to compute the actual f_c from the values of f_D and $Att_{req,LC}(f_D)$ obtained from the EMI measurement. In the next section, phase shedding of CCM is performed at 24 kHz to determine the maximum power level of operation for each stage of interleaving.



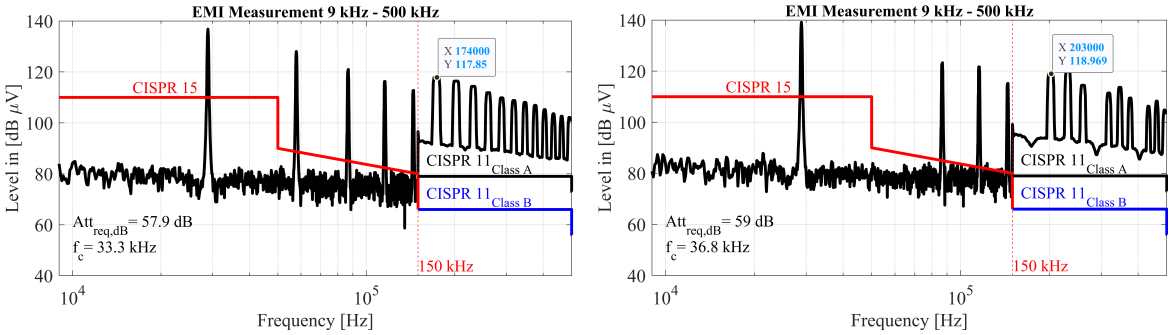
(a) n_{stage} = 1, P_o = 2208 W

(b) n_{stage} = 2, β= 180°, P_o = 3680 W



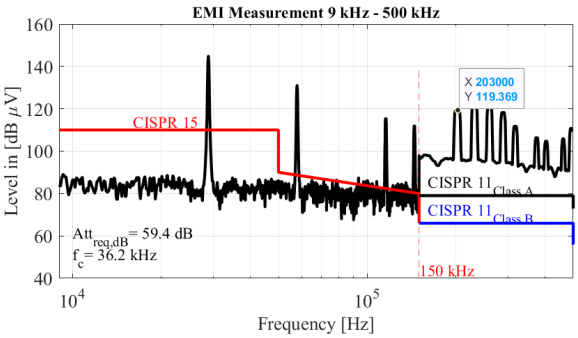
(c) n_{stage} = 3, β= 120°, P_o = 7360 W

Figure 5.14: EMI measurement results with the optimum core selected for CCM operation, High Flux core "58620" with μ=125 , N_C=1 and N_r =53 at f_{sw} = 24 kHz, conventional phase shift.



(a) n_{stage} = 1, P_o = 2060 W

(b) n_{stage} = 2, β= 90°, P_o = 3680 W



(c) n_{stage} = 3, β= 40°, P_o = 7360 W

Figure 5.15: EMI measurement results with the optimum core selected for CCM operation, High Flux core "58620" with μ=125 and N_C=1, N_r =53 at f_{sw} = 2 kHz, non conventional phase shift of β= 90° for n_{stage} = 29 and β= 40° for n_{stage} = 3.

The first quasi-peak which appears in the band B at f_D in Figures 5.14 and 5.15 matches with the corresponding f_D which was predicted in Figure 5.13. The cancellation of

harmonics for different phase shifts and different stages of interleaving given in Table 5.6 is also demonstrated using the EMI simulation results.

5.3.1 Phase shedding in CCM for the selected core

The optimum core selected for CCM operation is the High Flux core "58620" with μ=125 and N_C=1, N_r =53. The simulation is conducted with this inductor for different power levels within a specified range with n_{stage} = 1,2,3 for f_{sw} = 24 kHz with conventional phase shift. The total loss and efficiency are calculated. The filter design frequency, f_D is determined from EMI measurements, and a DM EMI filter is designed to achieve the least volume for the calculated cut-off frequency.

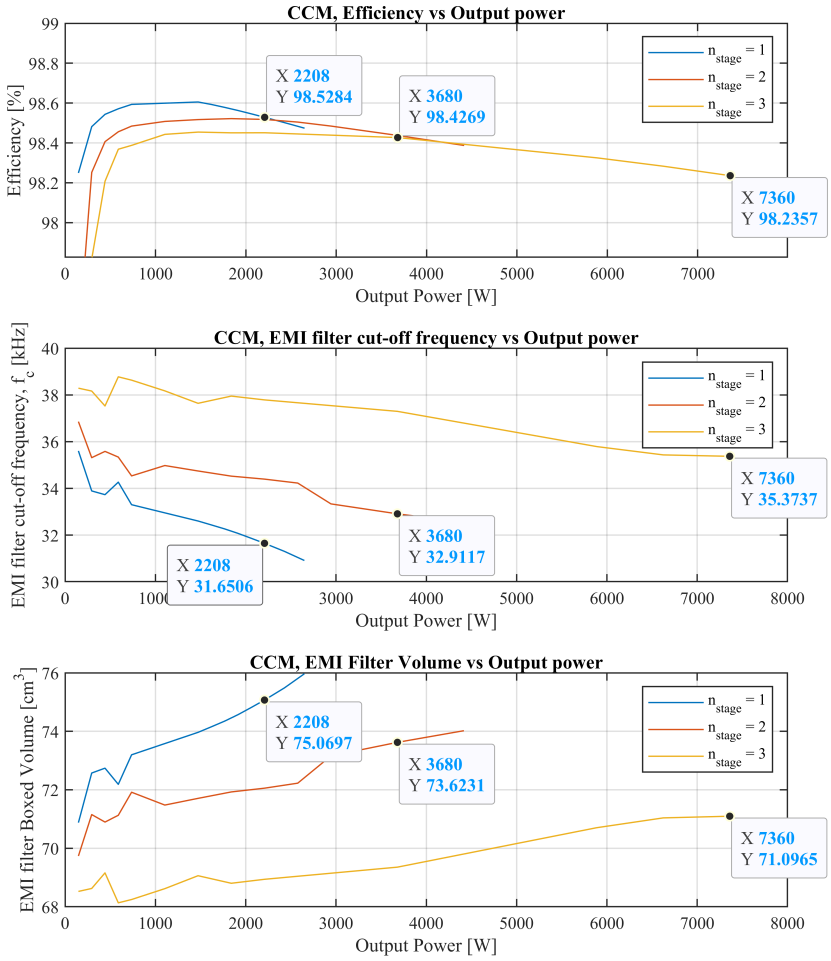


Figure 5.16: Phase shedding operation with the optimum core selected for CCM operation, High Flux core "58620" with μ=125 and N_C=1, N_r =53 at f_{sw} = 24 kHz, conventional phase shift.

It is shown that phase shedding operation can improve the efficiency of the converter by shedding the interleaved units when the load decreases. At full load, all three stages run, when the load drops below 3680W, the number of interleavings can be reduced to two, and below 2208 W, single stage operation yields better efficiency. However, a drawback of phase shedding is that the EMI noise for two stage interleaved and one stage interleaved

operation is higher. Therefore, the EMI filter design should be carried out with respect to the cut-off frequency f_c = 31.6 kHz at a power level of 2208W with single stage operation. This results in an EMI filter volume of 75 cm^3.

The simulation is conducted for different power levels within a specified range with n_{stage} = 1,2,3 for f_{sw} = 29 kHz, using a non-conventional phase shift of β= 90° for n_{stage} = 2 and β= 40° for n_{stage} = 3. The total loss and efficiency are calculated.

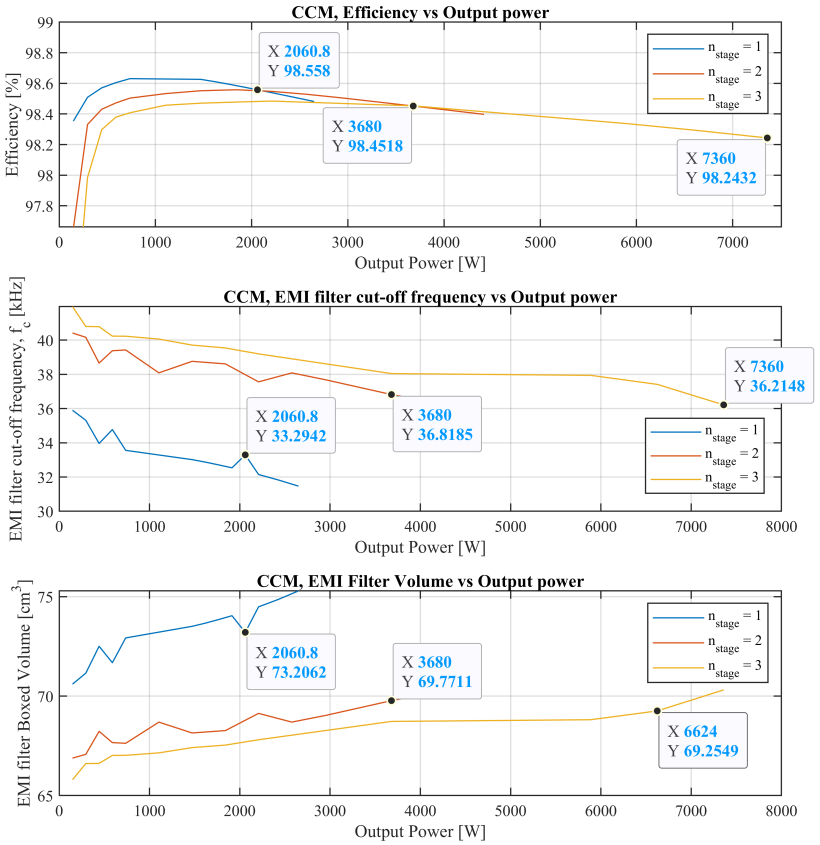


Figure 5.17: Phase shedding operation with the optimum core selected for CCM operation, High Flux core "58620" with μ=125 and N_C=1, N_r =53 at f_{sw} = 29 kHz, non conventional phase shift of β= 90° for n_{stage} = 2 and β= 40° for n_{stage} = 3.

When comparing Figures 5.16 and 5.17, it becomes evident that phase shedding operation with non-conventional phase shifts at fsw = 29 kHz is more beneficial. This is due to the fact that, for non-conventional phase shift, EMI filter cutoff frequency (f_c = 31.6 kHz) for the single stage at the change over point (P_o = 2060) is higher than in the conventional phaseshifting case. This results in a lower filter volume of 73 cm^3. Additionally, the cut-off frequency curves of two and three stage interleaved conditions are closer to each other. Thus, when phase shedding is implemented, the EMI noise level with two stages is not as high as in the conventional phase shift case.

5.3.2 Phase shedding in QCM for the selected core

The optimum core selected for QCM operation is High Flux core "58089" with μ=125, N_C=1 and N_r =40, at an operating point α = 40° at full load for a f_{sw} of 20 kHz. To determine the optimum switching frequency, phase shift, and power levels for phase shedding, simulations are conducted for a different range of power levels with n_{stage} = 1,2,3 for f_{sw} = 24 kHz with conventional phase shift, and 29 kHz with non-conventional phase shifts as in the case of CCM.

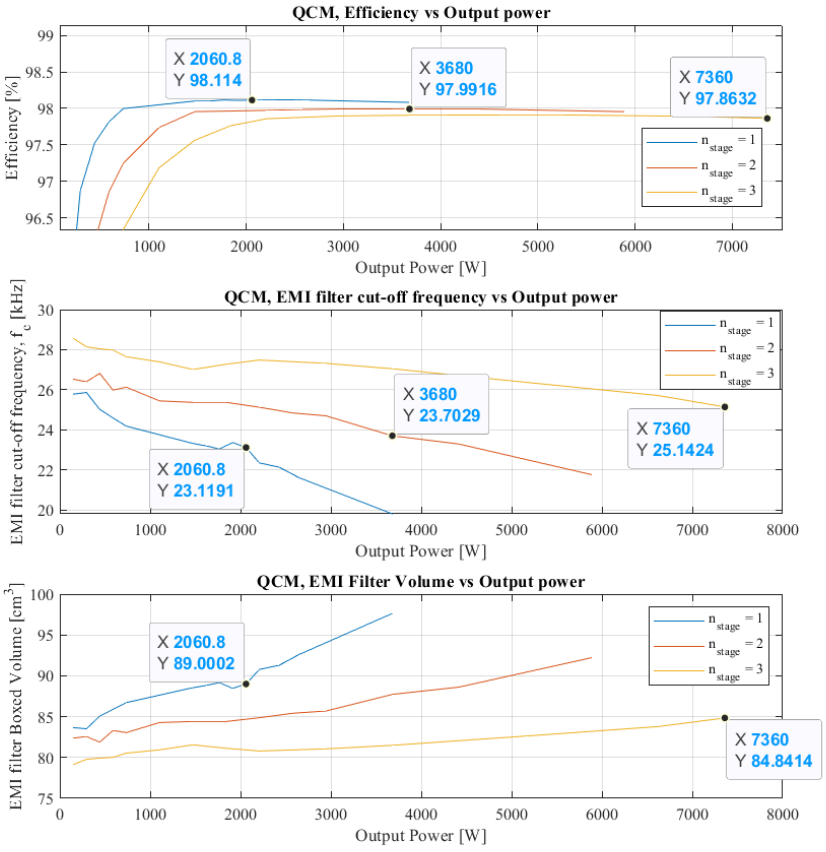


Figure 5.18: Phase shedding operation with the optimum core selected for QCM operation, High Flux core "58089" with μ=125, N_C=1 and N_r = 40 at f_{sw} = 24 kHz, conventional phase shift.

Comparing the phase shedding operation in CCM, it is noticeable that the plots for one and two stages do not intersect below the three-stage plot at higher power levels. This can be attributed to the higher core loss in the case of QCM.

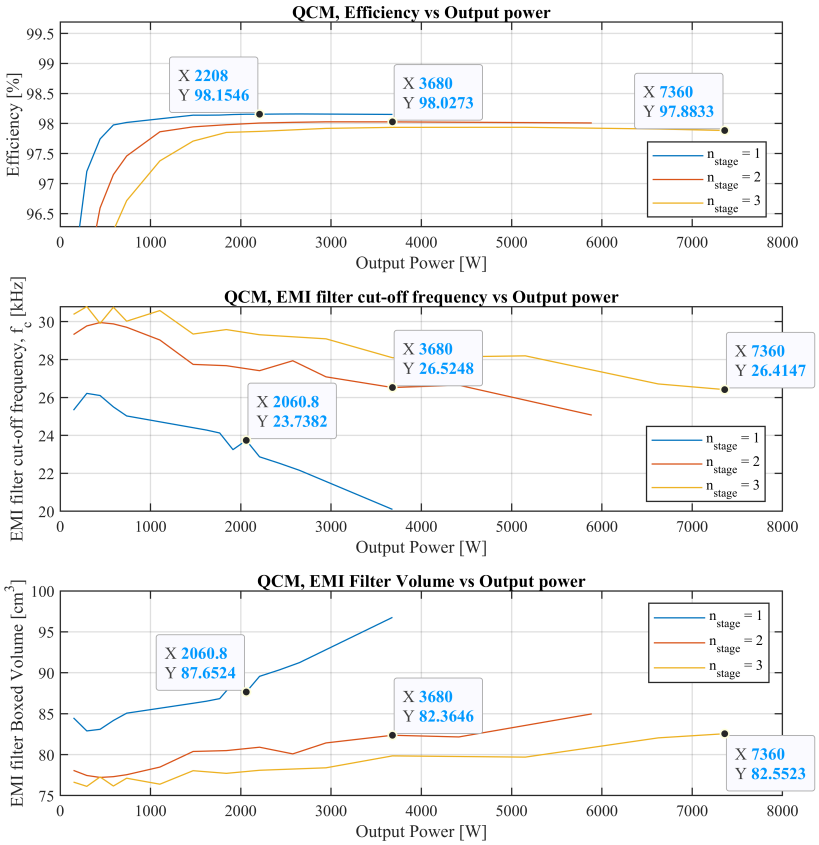


Figure 5.19: Phase shedding operation with the optimum core selected for QCM operation, High Flux core "58089" with μ=125 N_C=1 and N_r = 40 at f_{sw} = 29 kHz, non conventional phase shift of β= 90° for n_{stage} = 2 and β= 40° for n_{stage} = 3.

On comparing Figures 5.18 and 5.19 the phase shedding operation for QCM, non-conventional phase shifts at fsw = 29 kHz is more beneficial. This is because for non-conventional phase shift, EMI filter cutoff frequency (f_c = 31.6 kHz) for single stage at change over point (P_o = 2060) is higher than the conventional phase shifting case. This results in lower filter volume of 87.6 cm^3. Also, the cut-off frequency curve of two and three stage interleaved condition is closer to each other. Thus when phase shedding is implemented, the EMI noise level with two stages is not as high as in conventional phase shift.

In this chapter, in Section 5.1, the optimum boost inductor, and DM EMI filter are designed with respect to high power density, efficiency and EMC performance for both CCM and QCM operations. The optimised design for CCM utilises a High Flux core "58620" with μ=125 and N_C=1, N_r =53, and a single layer, resulting in a total boxed volume of inductors equal to 396 cm^3. For QCM operation, the optimised design employs a High Flux core "58089" with μ=125 and N_C=1, N_r =40, and a single layer, resulting in a total boxed volume of inductors equal to 158 cm^3. A case study is conducted in Section 5.2 to demonstrate the effect of parasitic capacitance on high frequency noise. Case 1, with a single layer winding, exhibits lower noise levels when compared to Case 3, which employs a multi-

layer winding. In Section 5.3, phase shedding technique is examined to determine the best switching frequency, phase shift, and EMI filter design. The final results are tabulated in Table 5.8.

Modulation technique	**CCM**	**QCM**
Boost inductor core	High Flux 58620	High Flux 58089
Number of cores, N_C	1	1
Number of layers, N_L	1	1
Number of turns, N_r	53	40
Unbiased boost inductance [μH]	1020	260
Optimum switching frequency, f_{sw} [kHz]	29	29
Total boxed volume for 3 boost inductors [cm^3]	396	158
Optimum Phase shift for interleaving , β [deg]	90° for $n_{stage} = 2$ 40° for $n_{stage} = 3$	90° for $n_{stage} = 2$ 40° for $n_{stage} = 3$
Total losses at full load [W]	132	159
Efficiency at full load, μ [%]	98.2	97.8
EMI filter cut off frequency, f_c [kHz]	33.3	23.7
EMI filter volume [cm^3]	73	88
DM filter inductance, L_{DM} [μH]	6	8
DM filter capacitance, C_{DM} [μF]	4	6
Total volume of converter [$cm^3] (approximated by adding volume of each device)	1650	1400
Power Density [kW//dm^3]	4.5	5.2

Table 5.8: Summary of comparison of losses and efficiency and EMI simulation results CCM and QCM operation for three stages interleaved PFC converter for P_o = 7360 W, V_o = 400 V, $V_{in,rms}$ = 230 V and f_{sw} = 29 kHz.

The utilisation of the QCM technique, as opposed to the CCM method, results in a notable decrease in total boost inductor volume, approximately 60%. The increase in EMI filter volume for QCM over CCM is not significant. This enhancement positively impacts the power density of the converter when operating in QCM mode, without significantly compromising the overall efficiency of the converter, as illustrated in Table 5.8. The analysis of the interleaved PFC boost converter underscores the potential benefits of integrating QCM modulation, which include a substantial reduction of 60% in the size of the boost inductor and a 16% increase in the power density of the PFC converter from 4.5 kW/dm^3 to 5.2 kW/dm^3.

Chapter 6
Hardware Implementation and Validation

This chapter provides a comprehensive overview of the hardware design for a single phase three stage interleaved PFC boost converter. It encompasses the determination of component specifications, the selection of appropriate devices, and the design of the converter's PCB. The chapter concludes with a discussion of experimental results and the validation of simulations.

6.1 PCB Design

A four layered PCB has been designed for the 3 stage interleaved boost converter. This section presents brief analysis of the key components chosen for the design, which includes the MOSFET module, bridge rectifier, sensors, and capacitors. Additionally, this section delves into the primary factors taken into account during the PCB design process and provides a visual representation of the three-dimensional layout of the PCB.

6.1.1 Power Semiconductor devices

The primary power semiconductor devices required to implement a PFC converter include MOSFETs and diodes in the boost converter, a bypass diode for inrush current protection, and diodes in the bridge rectifier. In order to achieve maximum power density, the SiC MOSFET Module SK45MLET12SCp from SEMIKRON is examined in this project. It contains three distinct boost legs in a relatively compact package, making it an excellent candidate for implementing interleaved PFC. It has an ultra-low inductance design, SiC 1200V planar MOSFETs, Schottky FWDs and by-pass rectifier diodes [26]. It is slightly overrated for the application, but given that this is a laboratory prototype, it justifies having a higher-rated device for added safety margin and flexibility for testing. Moreover, since the component comes in a module packaging, it is very compact, and one of the project objectives is to evaluate the use of the module for interleaving. The bridge rectifier chosen is GBJ5010 from Panjit Semiconductor. It is a glass passivated bridge rectifier with 4 diodes with a maximum average forward current rating of 50A when attached to a heat sink. This component is well-suited for integration onto printed circuit boards. The Maximum Repetitive Peak Reverse Voltage of the device is 1000V [27].

The isolated gate driver (CGD15SG00D2) tailored for 900V and 1200V SiC MOSFETs from Wolfspeed is used to drive the MOSFET module. It has a integrated isolated power supply, Gate driver output voltage = +15 V (max) / -3.3 V (min), High Creepage (9mm) clearance between logic side and power side[28]. Three such drivers are used. The block diagram for the gate driver is in Figure 6.1.

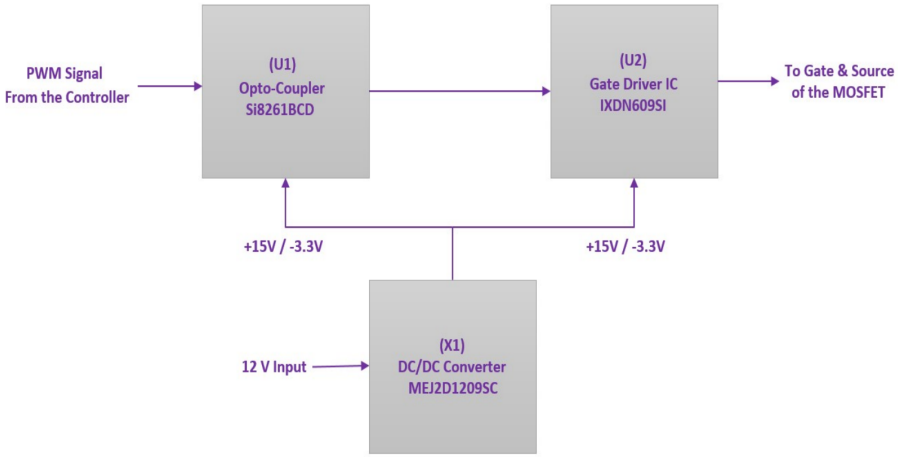


Figure 6.1: Block diagram of CGD15SG00D2 gate driver board [28].

6.1.2 Capacitors Selection

Electrolytic capacitors find widespread application as output filters in power converters, to reduce DC bus oscillations due to their high energy storage capacity. However, it is worth noting, that they have high ESR and ESL, resulting in an inferior performance at higher frequencies. In contrast, Film capacitors, are recommended for noise attenuation owing to their naturally higher energy density. Electrolytic capacitors, on the other hand, excel in low-frequency applications. To harness the advantages of both capacitor types, it is common practice to connect electrolytic and film capacitors in parallel to achieve the required DC-link capacitance. This combination produces low impedance across a wide frequency range while also providing significant capacitance for energy storage. To get the required capacitance value for the design, 10 Aluminium Electrolytic Capacitors of value 560 μF, and a voltage rating of 450 V from Würth Elektronik are connected in parallel. In addition to this, a 50 μF film capacitor is placed in parallel.

6.1.3 DSP as controller and its programming

For the implementation of control in the machine emulator, a controller is essential. The controller chosen is the Digital Signal processor (DSP) TMS320F280049C from the C2000 family by Texas Instruments (TI). This DSP boasts a high-efficiency 32-bit CPU, offering a cost-effective solution for both the device and the overall system. It operates at speeds of up to 100 MHz, with a flash memory capacity of up to 256 KB and a RAM capacity of up to 100 KB. Additionally, it features up to 18 Enhanced Pulse Width Modulation (ePWM) modules and a 12-bit ADC equipped with dual sample-and-hold capability across 16 channels [29]. In order to program the microcontroller effectively, a compatible platform for interaction is essential. Microcontrollers manufactured by TI are typically programmed using C/C++ code, with platforms like Code Composer Studio (CCS). However, using CCS can introduce complexities, particularly in manually translating the control algorithm into C code. This may lead to an increased likelihood of errors, subsequently prolonging the debugging process as one seeks for faults in either the C code or the control strategy. To address this challenge, the Target Support Package in PLECS for TI C2000 Code Generation proves invaluable. This tool employs embedded coder technology to seamlessly convert the control algorithm from PLECS and automatically generate concise C code for the DSP.

Utilizing the embedded coder not only reduces the time-to-market but also enhances the code's serviceability [30].

6.1.4 Current and voltage sensors

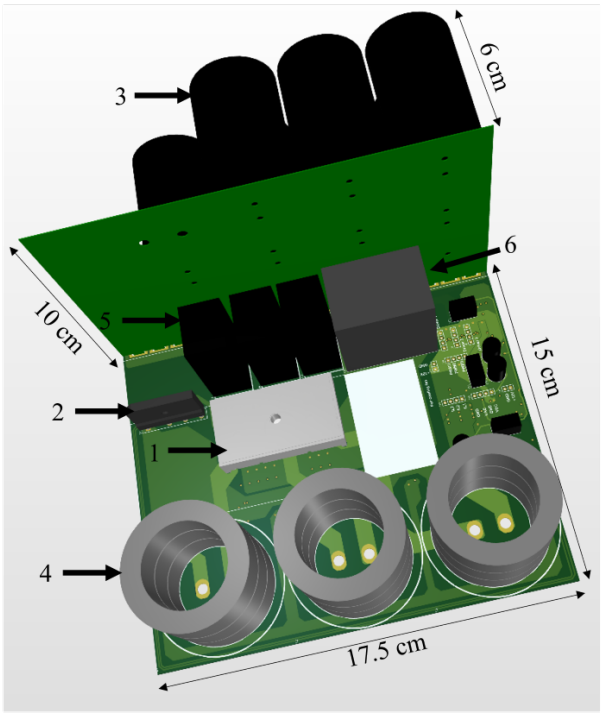
The ADC (Analog-to-Digital Converter) integrated into the TI DSP has a limited sensing range, it is specifically designed to capture voltage signals within the 0 to 3 volt range. To accommodate this, the sensing circuits are employed to transform both the measured voltage and current into a compatible range of 0 to 3 volts for accurate ADC readings. In ensuring proper system control, it is crucial to consider the characteristics of the feedback signal waveform. This encompasses factors such as amplitude, phase-angle, and phase sequence, all of which significantly influence the control process. Care is also taken to use isolated sensor circuits.

The current sensor used to measure the inductor currents is ACS725LLCTR-40AB-T from Allegro MicroSystems. Its small package is ideal for space-constrained applications. The device consists of a precise, low-offset, linear Hall sensor circuit. When current flows through the copper conduction path in the sensor, it generates a magnetic field which is sensed by the integrated Hall IC and converted into a proportional voltage. The current is sensed differentially to reject common-mode fields, improving accuracy in magnetically noisy environments[31]. It operates with a 3.3V supply and has a sensitivity of 33 mV/A. The schematic for the current sensor circuit is given in Figure A.5. To enhance the frequency response, it is advisable to incorporate an RC filter by connecting it between the ground and the output voltage signal. Additionally, for safeguarding the DSP against over-voltage scenarios, it is wise to consider the inclusion of a 3V zener diode.

The output DC voltage is measured using NSI1311DSWVR from NOVOSENSE Microelectronics. The NSI1311DSWVR is an isolation amplifier known for its capacitance isolation technology, ensuring complete separation between the input and output. This component is specifically engineered to accommodate single-ended input signals within the range of 0.1V to 2V. Additionally, the high input impedance characteristic of the NSI1311DSWVR renders it well-suited for seamless integration with high voltage resistive dividers or other sources of voltage signals featuring elevated output impedance.[32]. The DC voltage is first passed through a resistive divider to scale down a voltage of 450V to 1.5V. This scaled-down voltage is then passed through the isolation amplifier, and a signal conditioning circuit is employed to finally transform the initial 450V to 2.98V, which can be safely connected to DSP through an RC filter and 3V zener diode as shown in Figure A.6.

The AC input voltage of the PFC is measured using the AMC1301DWVR sensor from Texas Instruments. The AMC1301 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. The input AC voltage of the PFC is first passed through a resistive voltage divider to scale from ± 400 V to ± 250 mV which is dropped across a shunt resistor. The input of the AMC1301 is optimized for direct connection to shunt resistors or other low voltage-level signal sources. The sensor output is then passed through a conditioning circuit designed to get a voltage of range 0 to 3 V. This is connected to DSP

through an RC filter and zener diode as shown in Figure A.7.



	Device
1	SiC MOSFET module
2	Bridge Rectifier
3	DC link Capacitor
4	Boost inductor
5	Gate driver
6	Film Capacitor

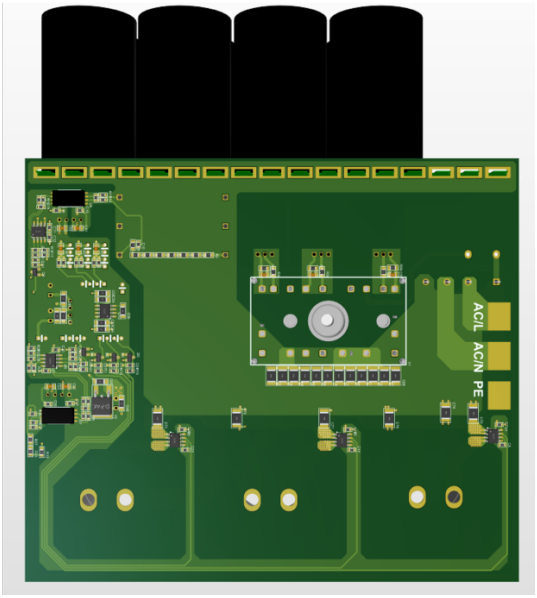


Figure 6.2: Top and bottom view of the PCB for 7.36 kW three stage interleaved boost PFC converter.

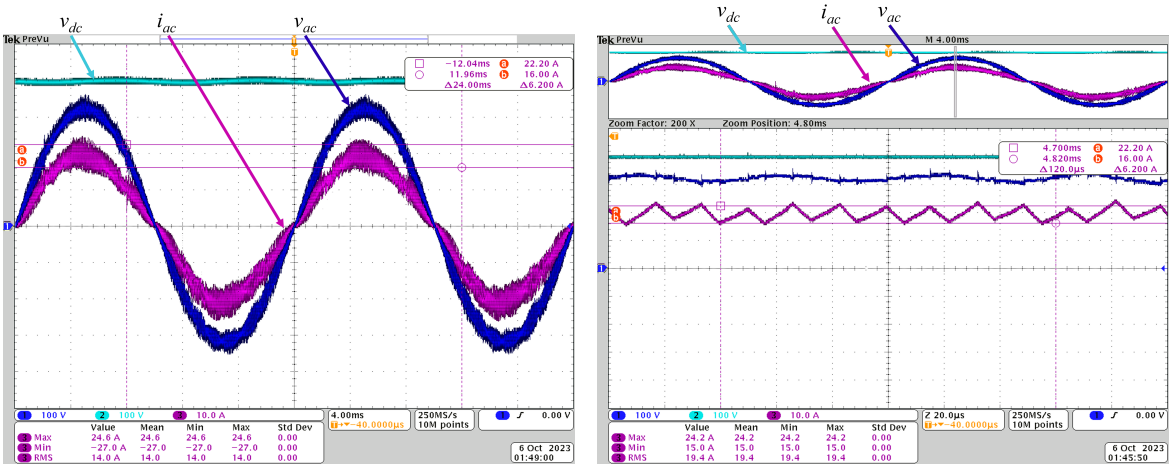
6.1.5 PCB layout

It is critical to design a PCB to reduce EMI while boosting power density to ensure that the converter operates reliably and efficiently. Some of the design considerations are discussed in this section. Multi-layer PCB with separate power and ground planes is used to provide a low-impedance return path for high-frequency signals. Track inductance is reduced by making the tracks as wide and as short as possible. Connecting power ground (PGND) and control ground (GND) at a single point to avoid interference. Using multiple ground vias to connect different layers of the PCB, ensuring a low-impedance ground

path. Keeping lines of hot and cold parts of the circuit separated to avoid cross-talk. Separating different interference levels by placing the components carefully. Use of SMD components wherever possible to reduce the lead parasitic capacitance. Reducing ground loops and minimizing the area of any loops. Placing decoupling capacitors close to the power pins of integrated circuits to provide local energy storage and stabilize the power supply. Implement proper thermal vias and heatsinking techniques to dissipate heat generated by high-power components. The top and bottom view of the PCB designed for 7.36 kW three stage interleaved boost PFC converter is given in Figure 6.2. Since this is a prototype and was designed before the final volume of inductor and EMI filter are obtained, enough space is given for the components. However the final power density is calculated in Table 5.8 by adding the volume of each components.

6.2 Test results and validation

This section presents the test results of the experiments conducted to validate the designed three stage interleaved PFC boost converter. The boost inductor chosen for the converter is the one optimized for QCM operation. (High Flux core 59089, μ=125, N_C =1, N_r =40, L_0 = 260 μH). The operation of the converter for different stages of interleaving at different power levels is tested with the conventional phase shift technique at a switching frequency of 20kHz. The highest power level examined is 3140 W for three stage interleaved converter. Operating at frequencies higher than 20 kHz could not be achieved using PLECS auto-code generation. All the required calculations in the control loop have to be executed within the sampling time. the Sampling frequency is set as twice the switching frequency. When switching frequency is set above 20 kHz, the control loop calculations did not complete, resulting in unstable control. For 20 kHz and below, the calculations were getting executed properly. Thus the results shown are with a switching frequency of 20 kHz.



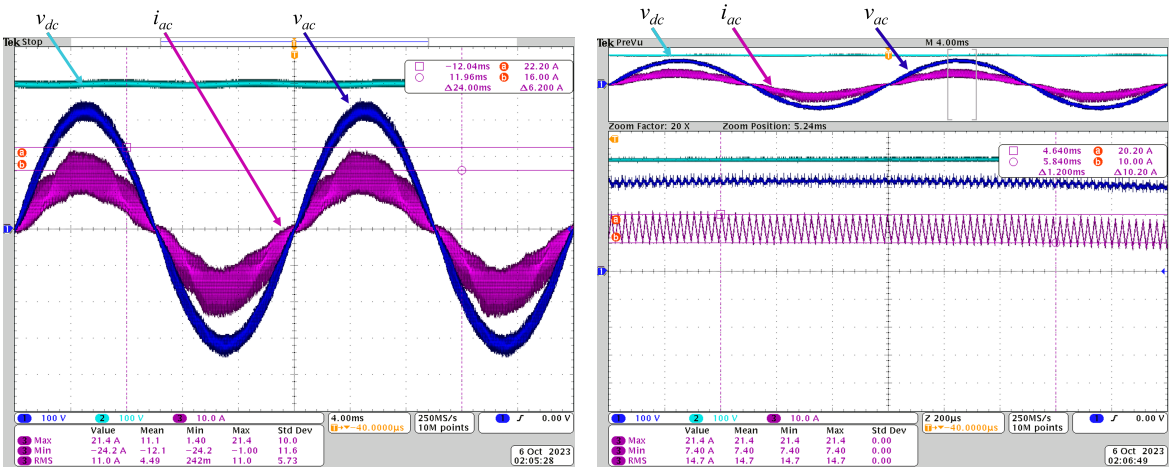
(a) Waveforms for 40 ms

(b) Zoomed in view

Figure 6.3: Experimental results for three stage interleaved PFC converter operating with a resistive load of 51 Ω at V_o =400 V (P_o = 3140 W) showing input line voltage v_{ac} (dark blue), line current i_{ac} (pink) and output voltage v_{dc} (light blue) waveforms.

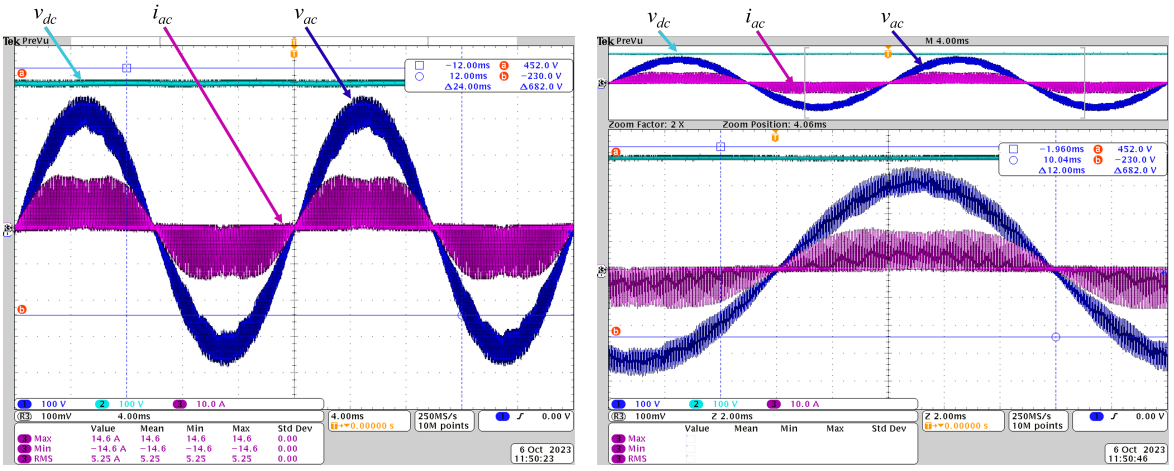
The experimental results are compared with simulation results and the shape of the waveform and peak-to-peak value of currents are verified to be similar. This is shown in

Figure C.2. It can be seen that the input AC current is sinusoidal and follows the input AC voltage in phase. The ripples get cancelled in three stage and two stage interleaved converter. The percentage of current ripple when compared with the input current average value is less for three stage interleaved as expected. The experimental results
5 demonstrate that interleaving many boost cells considerably reduces the overall input current ripple, resulting in high PF and low THD.



(a) Waveforms for 40 ms **(b)** Zoomed in view

Figure 6.4: Experimental results for two stage interleaved PFC converter operating with a resistive load of 65 Ω, V_o =400 V (P_o = 2460 W) showing input line voltage v_{ac} (dark blue), line current i_{ac} (pink) and output voltage v_{dc} (light blue) waveforms.



(a) Waveforms for 40 ms **(b)** Zoomed in view

Figure 6.5: Experimental results for non-interleaved PFC converter operating with a resistive load of 153, V_o =400 V Ω (P_o = 1045 W) showing input line voltage v_{ac} (dark blue), line current i_{ac} (pink) and output voltage v_{dc} (light blue) waveforms

Chapter 7
Conclusion and Future Work

7.1 Conclusion

Achieving high power density in converters is crucial to the advancement of numerous sectors and technologies, resulting in more efficient, compact, and sustainable systems. In this project, the emphasis is on analysing the effects of different current modulation techniques, interleaving, switching frequency variation, phase shedding, phase shifting, and optimisation of the boost inductor and EMI filter on the design of a single-phase PFC boost converter to achieve high performance and power density. The optimisation of these influencing factors requires the proper design of the inductor, fast, accurate, and easily accessible simulation of PFC, computation of losses of various components in PFC, EMI noise prediction, and EMI filter design.

The operation of the PFC converter with different modulation techniques (CCM, QCM, DCM) affects the component sizing, efficiency, and EMI filter requirements. The inductance value for the boost inductor is designed for each mode, and the design basis of achieving the required ripple at the desired angle is validated through simulation for each mode. The process of designing the physical inductor is thoroughly studied. The data of various types of cores provided by the core manufacturer Magnetics is used to design a GUI with an algorithm of designing the inductance required and identifying the core which gives the least boxed volume for each configuration. The algorithm behind this tool is one of the crucial part in further optimisations carried out in the project.

In order to quickly achieve the simulated steady state waveforms of PFC, including the effect of DC biasing, a MATLAB script based simulation of the PFC is created. The simulation results from this code are compared and verified with PLECS. This code can simulate more close to practical waveform through the inductor since it incorporates the modeled DC biasing of the inductor using the GUI. It has faster computational and access time of steady state waveform compared to running the simulation in PLECS and extracting steady-state waveforms from it to use in optimisation algorithm.

The virtual measurement of EMI noise is addressed by modeling LISN and EMI receiver. The steady state waveform of the current in the PFC is utilised to simulate the quasi peaks of EMI measurement. The DM EMI filter is design based on the noise measurements, and the filter values are computed for least volume. Achieving the optimal filter volume requires volumetric information about inductors, which has been modeled using the developed GUI.

Improved iGSE is employed to compute the core loss of the inductor in boost PFC, using the steady state current waveform. The loss modeling of semiconductor devices is perfomed by extracting relevant information from their datasheet. This model, combined with the steady-state waveforms of current and voltage across the components, is used to

determine the average loss. This approach aids in predicting the total loss of the converter and, consequently, its efficiency.

With the proper inductor design, simulated waveform corresponding to the designed inductor, losses of components, and the design of the EMI filter in hand, optimisation is performed to find the best inductor core configuration for operation in CCM and QCM modes. The optimised inductor designed for CCM is with single stack High Flux core 58620 with 53 number of turns. Optimisation for QCM gave two results- one with single stack and other with two stacks. High frequency measurement tests were conducted on these configurations along with a multi layer case to understand the effect of parasitic capacitance on EMI noise at very high frequencies. It is found that single-stack, single-layer cores provided better EMI performance at higher frequencies with the added advantage of reduced cost. Therefore, the single stack High flux core 58089 with 40 number of turns is chosen as optimum for QCM operation.

Once the optimised inductor with the least volume, losses, and better EMC performance is selected, to further reduce the EMI filter volume and increase the efficiency, the effect of phase shedding with different phase shifts and switching frequency is studied. Over the range of considered switching frequencies (20 kHz to 30 kHz), non conventional phase shift operations with $\beta = 40^\circ$ for three stage interleaving and $\beta = 90^\circ$ for two stage interleaving gave the best efficiency and EMI performance at a switching frequency of 29 kHz.

In the final comparison, the optimized design in CCM and QCM is considered. When QCM modulation is employed instead of CCM modulation, there is a reduction in the overall boost inductor volume by approximately 60%. The increase in EMI filter volume from CCM to QCM is not substantial due to the optimisations employed. This improvement positively impacts the PFC converter's power density with an increase of around 16% when operating in QCM mode, without significantly compromising the converter's overall efficiency and EMI performance.

7.2 Future Work

In this section, potential areas for future research are recommended to enhance or address objectives that fall beyond the scope of the current thesis. Various scenarios, which, due to time constraints within the semester, were not explored, are put forth as follows:

- Although the main objectives of the project have been met, work is still left to be done related to hardware testing, which could be considered interesting to do as a continuation of the project in the future.

- Prototyping for the DM EMI filter was not conducted in this project. To comprehensively assess the performance of the PFC converter, and to complement the design of EMI filter components, it is essential to consider PCB prototyping for the input filter. Measurement of conducted emission from the prototype is also left as a future work

- The performance of a combination of stacked cores with different types can be

investigated to determine whether it offers any advantages or improvements in the design.

- Frequency dithering can be used to improve the EMI performance of the converter. The fundamental idea behind frequency dithering is to vary the switching frequency within a defined range, as opposed to maintaining a constant switching frequency. This variation in switching frequency can modify the noise emission spectrum which can lead to better EMI performance.
- With the implementation of advanced thermal design and more efficient cooling methods, the full potential of the SiC module can be thoroughly investigated. This design can be scaled to accommodate higher power levels. Moreover, the integration of the designed single phase PFC converter as phase modules within a three phase PFC converter system presents a viable avenue for future exploration. A simulation of this concept has been conducted and is briefed in Appendix E for reference.

Bibliography

[1] M. Safayatullah, M. T. Elrais, S. Ghosh, R. Rezaii, and I. Batarseh, "A comprehensive review of power converter topologies and control methods for electric vehicle fast charging applications", *IEEE Access*, vol. 10, pp. 40 753–40 793, 2022. DOI: 10.1109/ACCESS.2022.3166935.

[2] F. Blaabjerg, H. Wang, I. Vernica, B. Liu, and P. Davari, "Reliability of power electronic systems for ev/hev applications", *Proceedings of the IEEE*, vol. 109, no. 6, pp. 1060–1076, 2021. DOI: 10.1109/JPROC.2020.3031041.

[3] R. W. Erickson and D. Maksimović, "Power and harmonics in nonsinusoidal systems", in *Fundamentals of Power Electronics*. Springer US, 2001, pp. 589–607, ISBN: 978-0-306-48048-5. DOI: 10.1007/0-306-48048-4_16. [Online]. Available: https://doi.org/10.1007/0-306-48048-4_16.

[4] International Electrotechnical Commission, *Iec 61000-3:2022 ser series, electromagnetic compatibility (emc) - part 3: Limit - all parts*. [Online]. Available: https://webstore.iec.ch/publication/62426, (Accessed: 01/06/2023).

[5] B. McDonald and B. Lough, "Power factor correction (pfc) circuit basics", *Texas Instruments Power Supply Design Seminar*, 2020. [Online]. Available: https://www.ti.com/seclit/ml/slup390/slup390.pdf.

[6] S. A. Rahman, F. Stückler, and K. Siu, "Pfc boost converter design guide", *Infineon Technologies AG*, 2016. [Online]. Available: https://www.infineon.com/dgdl/InfineonApplicationNote_PFCCCMBoostConverterDesignGuide-AN-v02_00-EN.pdf?fileId=5546d4624a56eed8014a62c75a923b05.

[7] E. R. Arenaza and M. M. Boghiu, "Design and performance analysis of high power density pfc converter", *Aalborg University*, 2020. [Online]. Available: https://projekter.aau.dk/projekter/files/334072520/FINAL_Design_and_performance_analysis_of_high_power_density_PFC_converter.pdf.

[8] M. O Loughlin, "An interleaving pfc pre-regulator for high-power converters", *Texas Instruments*, 2015. [Online]. Available: https://www.ti.com/lit/wp/slua746/slua746.pdf.

[9] T. Nussbaumer, K. Raggl, and J. W. Kolar, "Design guidelines for interleaved single-phase boost pfc circuits", *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2559–2573, 2009. DOI: 10.1109/TIE.2009.2020073.

[10] K. Raggl, T. Nussbaumer, G. Doerig, J. Biela, and J. W. Kolar, "Comprehensive design and optimization of a high-power-density single-phase boost pfc", *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2574–2587, 2009. DOI: 10.1109/TIE.2009.2020074.

[11] STMicroelectronics, "Power supply hold-up time", 2007. [Online]. Available: https://www.st.com/resource/en/technical_note/tn0024-power-supply-holdup-time-stmicroelectronics.pdf.

[12] K. D. Gusseme, D. Van de Sype, A. Van den Bossche, and J. Melkebeek, "Digitally controlled boost power-factor-correction converters operating in both continuous and discontinuous conduction mode", *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 88–97, 2005. DOI: 10.1109/TIE.2004.841133.

[13] J. Schönberger, "Modeling a pfc controller using plecs", *Plexim GmbH*, [Online]. Available: https://www.plexim.com/sites/default/files/plecs_pfc.pdf.

[14] Magnetics, *Powder cores*. [Online]. Available: https://www.mag-inc.com/products/powder-cores, (Accessed: 01/06/2023).

[15] Magnetics, *2020 magnetics powder core catalog*. [Online]. Available: https://www.mag-inc.com/Media/Magnetics/File-Library/Product%20Literature/Powder%20Core%20Literature/Magnetics-Powder-Core-Catalog-2020.pdf?ext=.pdf, (Accessed: 01/08/2023).

[16] P. Davari, F. Blaabjerg, E. Hoene, and F. Zare, "Improving 9-150 khz emi performance of single-phase pfc rectifier", in *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*, 2018, pp. 1–6.

[17] K. Raggl, T. Nussbaumer, and J. Kolar, "Model based optimization of emc input filters", in *2008 11th Workshop on Control and Modeling for Power Electronics*, 2008, pp. 1–6. DOI: 10.1109/COMPEL.2008.4634683.

[18] P. Davari, Y. Yang, F. Zare, and F. Blaabjerg, "A review of electronic inductor technique for power factor correction in three-phase adjustable speed drives", in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–8. DOI: 10.1109/ECCE.2016.7854767.

[19] J. Muhlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Core losses under the dc bias condition based on steinmetz parameters", *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 953–963, 2012. DOI: 10.1109/TPEL.2011.2160971.

[20] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power electronics: converters, applications, and design*. John wiley & sons, 2003.

[21] S. A. Rahman and N. Fontana, "Coolsic totem-pole pfc design guide and power loss modeling", *Infineon Technologies AG*, 2023. [Online]. Available: https://www-blue.infineon.com/dgdl/Infineon-Application_note_CoolSiC_Totem_Pole_PFC_Design_and_Power_Loss_Modeling-ApplicationNotes-v01_00-EN.pdf?fileId=8ac78c8c85ecb34701865a064ec24076.

[22] PLEXIM, *Thermal simulation*, 2022. [Online]. Available: https://www.plexim.com/products/plecs/thermal, (Accessed: 18/11/2023).

[23] J. C. Hernandez, L. P. Petersen, and M. A. E. Andersen, "Low capacitive inductors for fast switching devices in active power factor correction applications", in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, 2014, pp. 3352–3357. DOI: 10.1109/IPEC.2014.6870168.

[24] Y.-C. Chen, J.-D. Hsu, Y.-A. Ang, and T.-Y. Yang, "A new phase shedding scheme for improved transient behavior of interleaved boost pfc converters", in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 1916–1919. DOI: 10.1109/APEC.2014.6803567.

[25] C. Wang, M. Xu, F. C. Lee, and B. Lu, "Emi study for the interleaved multi-channel pfc", in *2007 IEEE Power Electronics Specialists Conference*, 2007, pp. 1336–1342. DOI: 10.1109/PESC.2007.4342188.

[26] Semikron Danfoss, *Sk45mlet12scp datasheet*. [Online]. Available: https://www.semikron-danfoss.com/dl/service-support/downloads/download/semikron-datasheet-sk45mlet12scp-24919661.pdf, (Accessed: 01/08/2023).

[27] Panjit Semiconductor, *Gbj5010 datasheet*. [Online]. Available: https://www.mouser.dk/datasheet/2/1057/GBJ5010-2949708.pdf, (Accessed: 01/08/2023).

[28] Wolfspeed, *Cgd15sg00d2 gate driver board for 3rd generation silicon carbide mosfets datasheet*. [Online]. Available: https://assets.wolfspeed.com/uploads/2020/12/CPWR-AN21.pdf, (Accessed: 01/08/2023).

[29] T. Instruments, *Tms320f280049c real-time microcontrollers*. [Online]. Available: https://www.ti.com/lit/ug/spruii7b/spruii7b.pdf, (Accessed: 17/10/2023).

[30] J. Allmeling, *Automatic code generation for embedded microcontrollers*, 2021. [Online]. Available: https://eepower.com/technical-articles/automatic-code-generation-for-embedded-microcontrollers/#, (Accessed: 18/10/2023).

[31] Allegro microsystems, *Acs725 datasheet*, 2021. [Online]. Available: https://www.allegromicro.com/-/media/files/datasheets/acs725-datasheet.pdf, (Accessed: 18/10/2023).

[32] Novosense Microelectronics, *Nsi1311dswvr datasheet*, 2021. [Online]. Available: https://www.novosns.com/Public/Uploads/uploadfile3/files/20220729/NSI1311_DatasheetRev1.5_EN.pdf, (Accessed: 18/10/2023).

Appendix A
PCB schematic

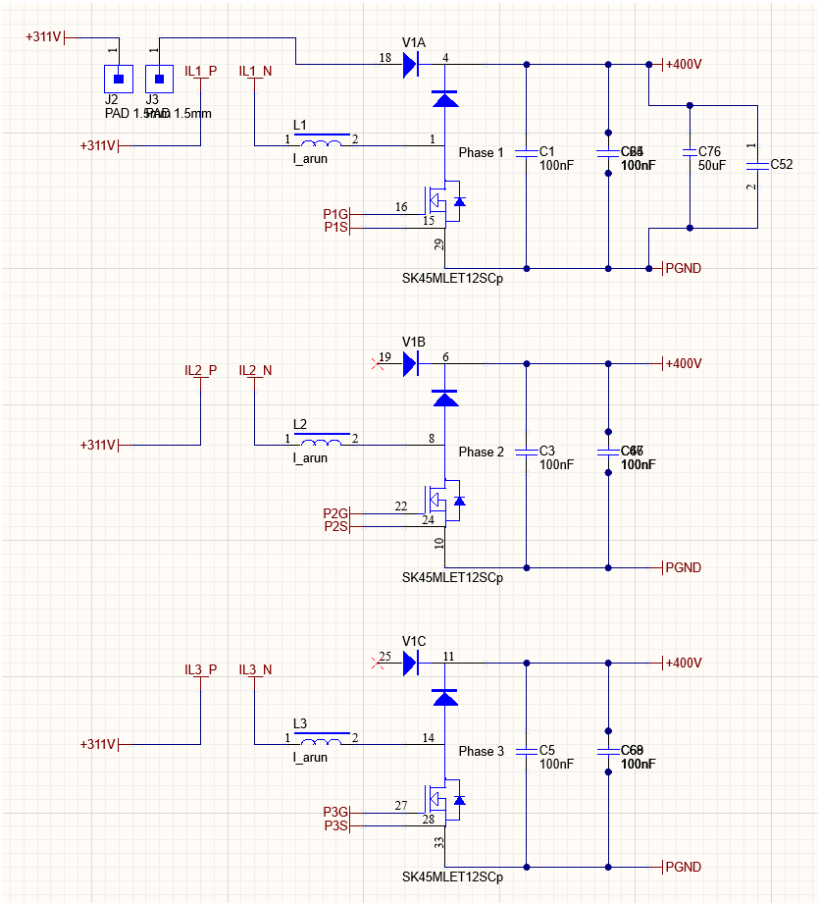


Figure A.1: Schematic of the interleaved boost converter of PFC

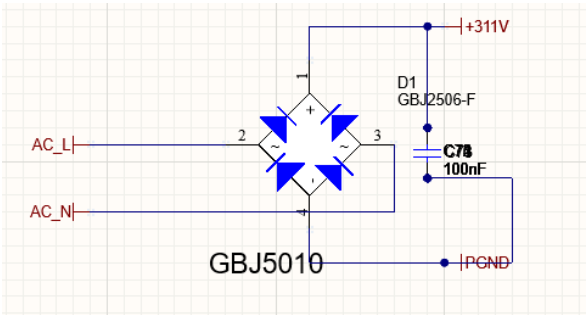


Figure A.2: Bridge rectifier in the PFC

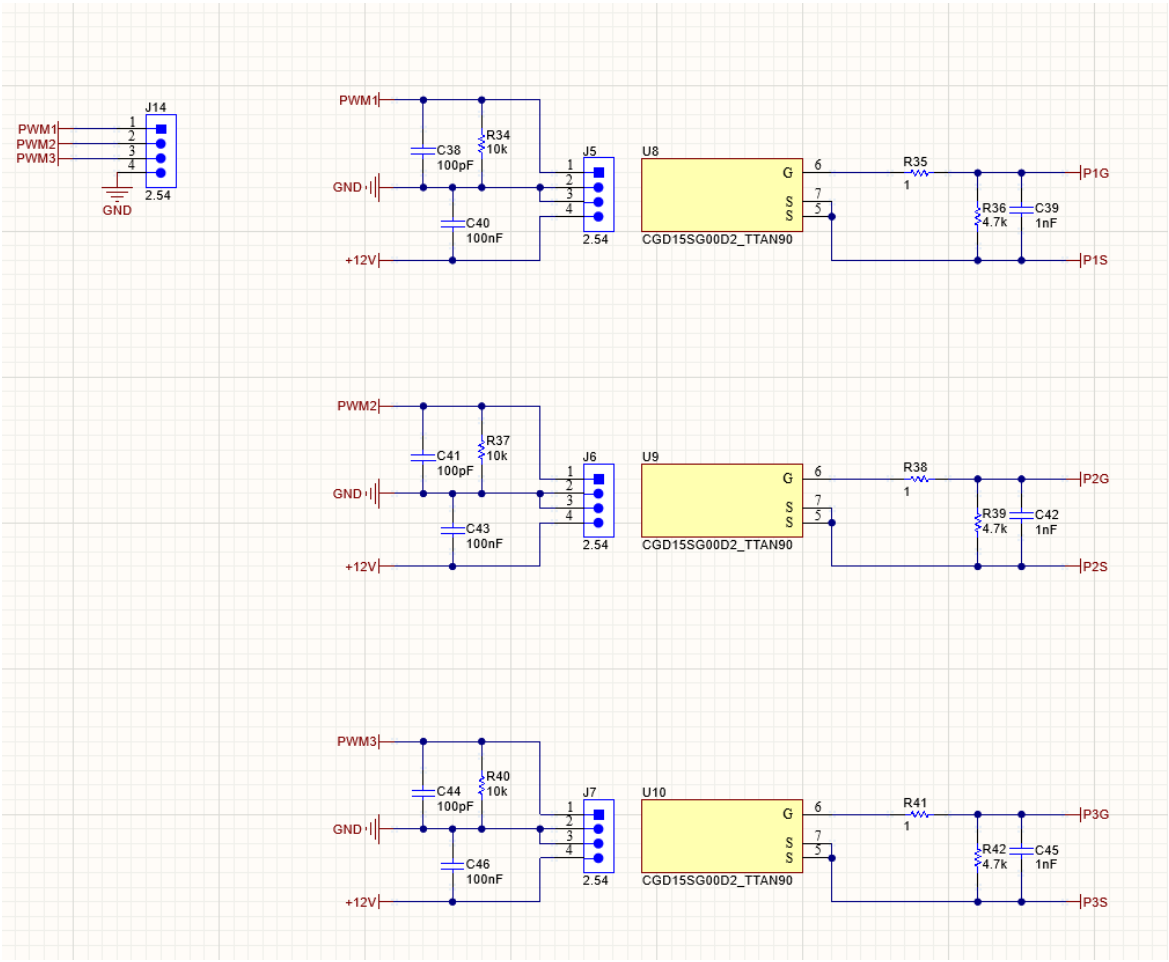


Figure A.3: Gate driving circuit

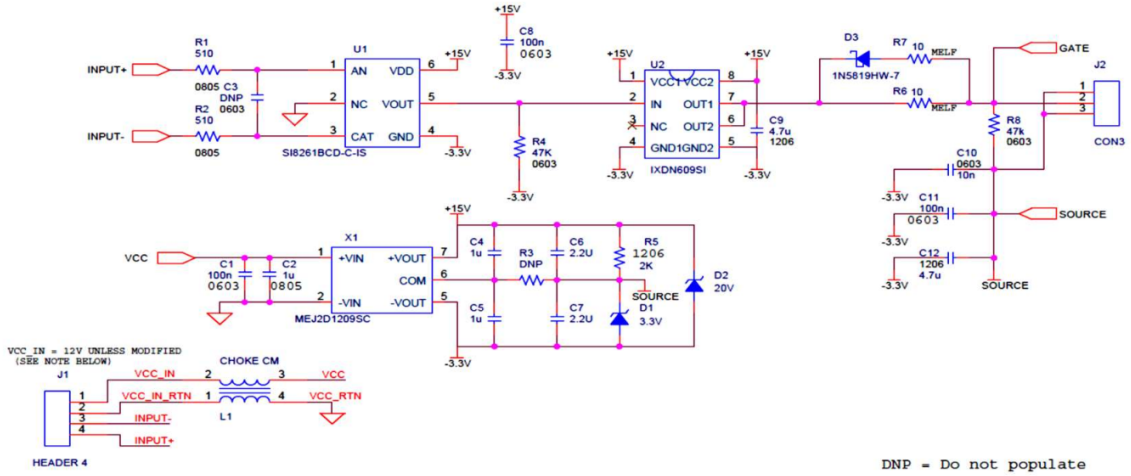


Figure A.4: Schematic of CGD15SG00D2 Gate driver board [28]

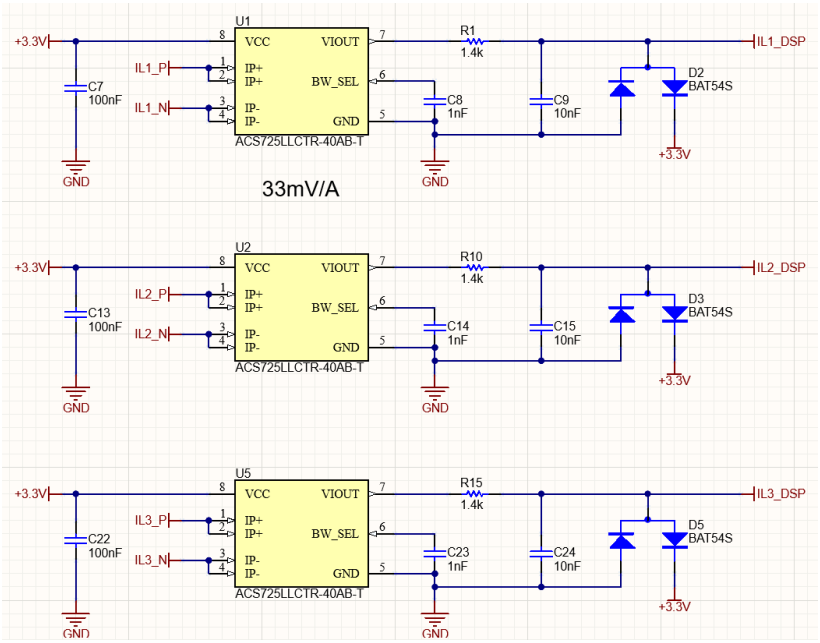


Figure A.5: Schematic for current sensor circuit for measuring current through boost inductor.

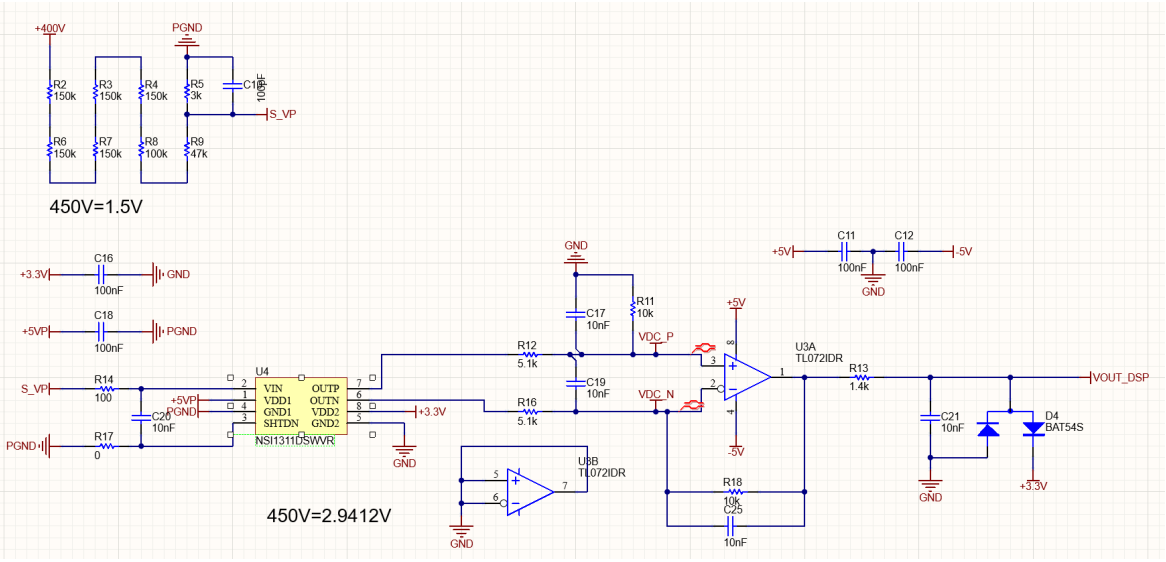


Figure A.6: Schematic for DC voltage sensing circuit for measuring output voltage of PFC.

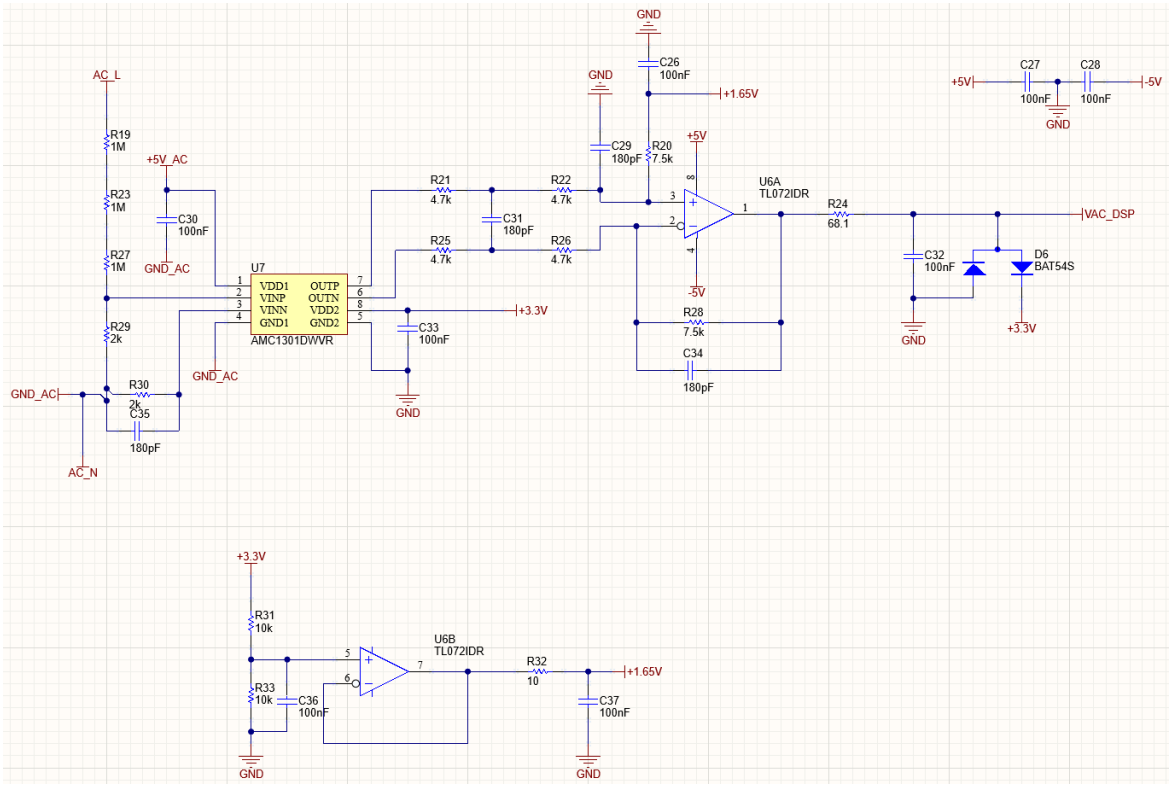


Figure A.7: Schematic for AC voltage sensing circuit for measuring input AC voltage of PFC.

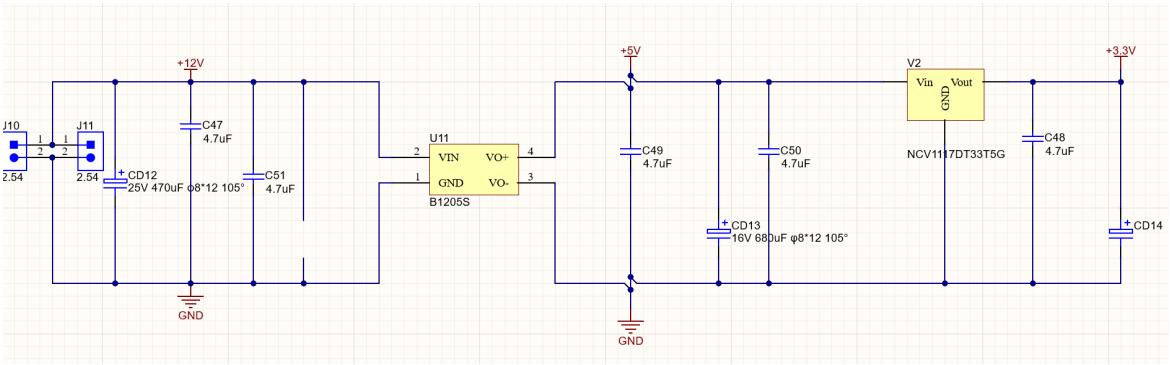


Figure A.8: Schematic for auxiliary power supplies required for gate driver and sensing circuits.

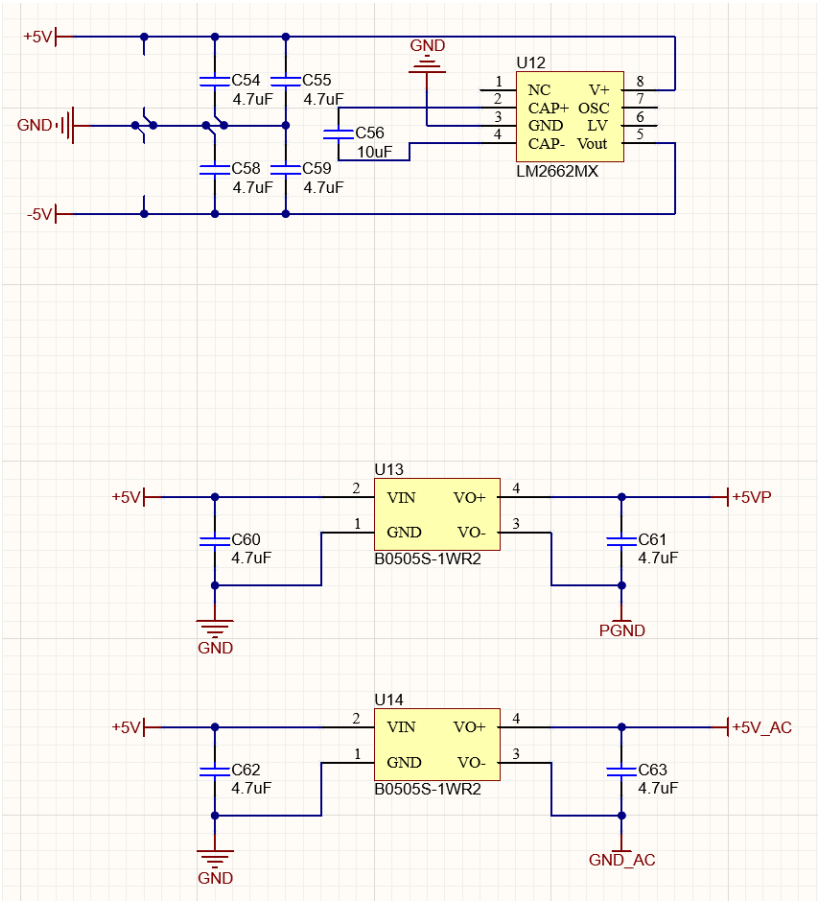


Figure A.9: Schematic for auxiliary power supplies required for gate driver and sensing circuits.

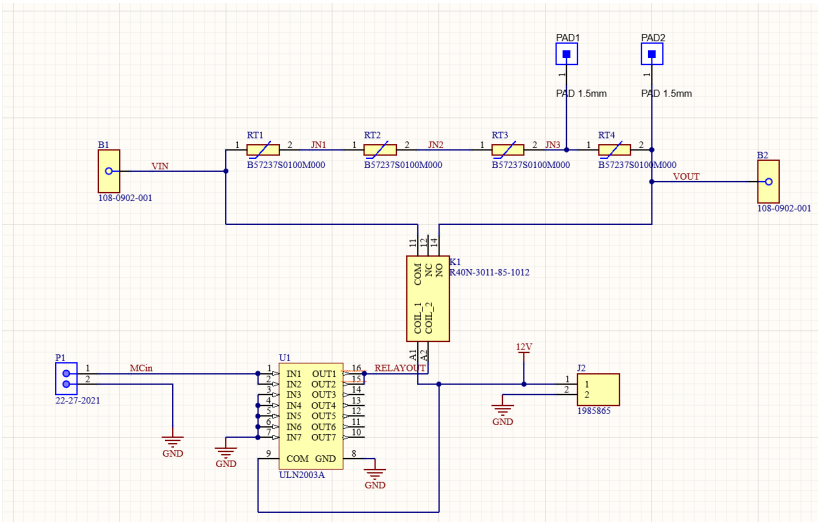
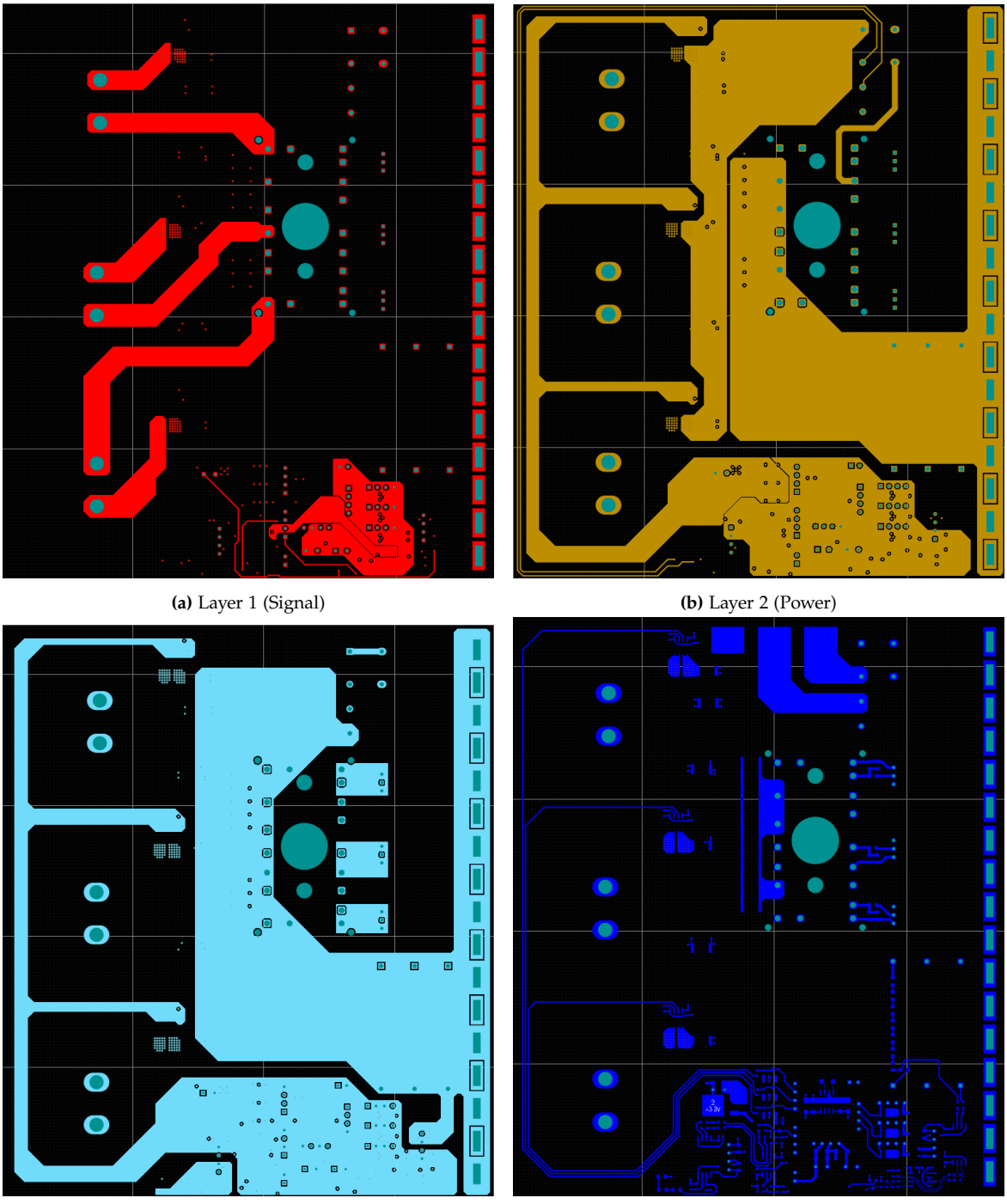


Figure A.10: Schematic for inrush current protection with NTC resistor and relay.

Appendix B
PCB layout



(a) Layer 1 (Signal)

(b) Layer 2 (Power)

(c) Layer 3 (Ground)

(d) Layer 4 (Signal)

Figure B.1: PCB layout of the PFC

Appendix C
Experimental setup

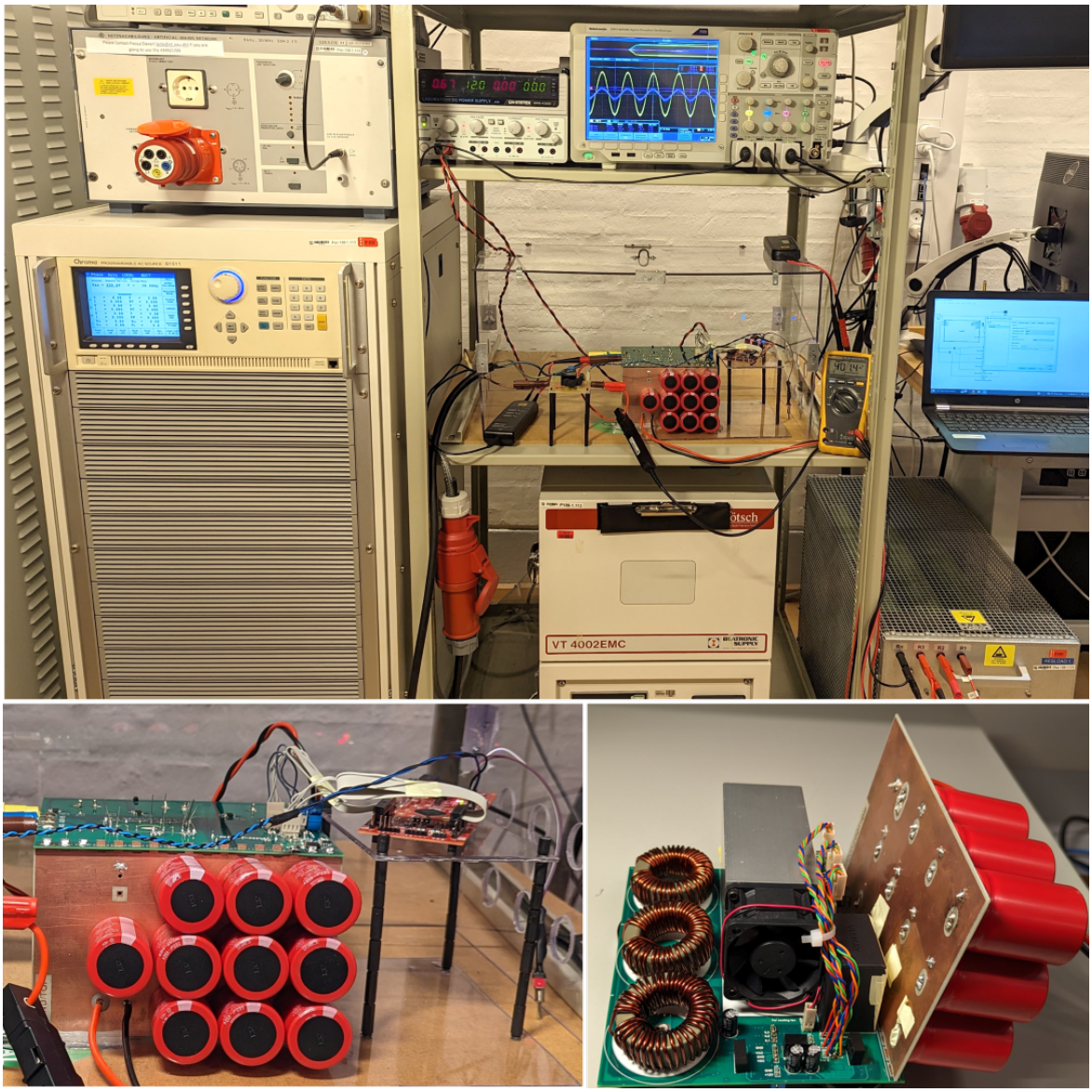
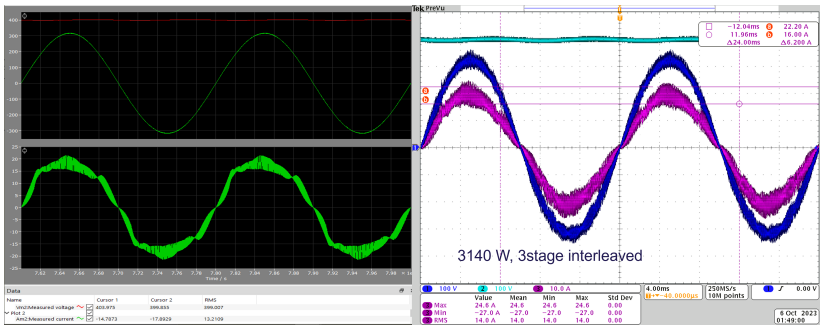
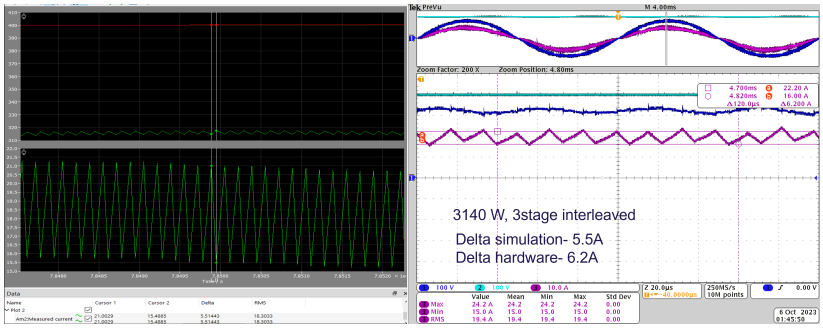


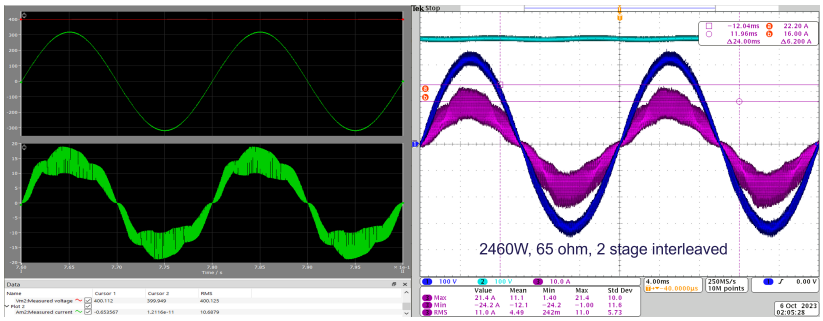
Figure C.1: Experimental setup for testing the single phase three stage interleaved boost converter



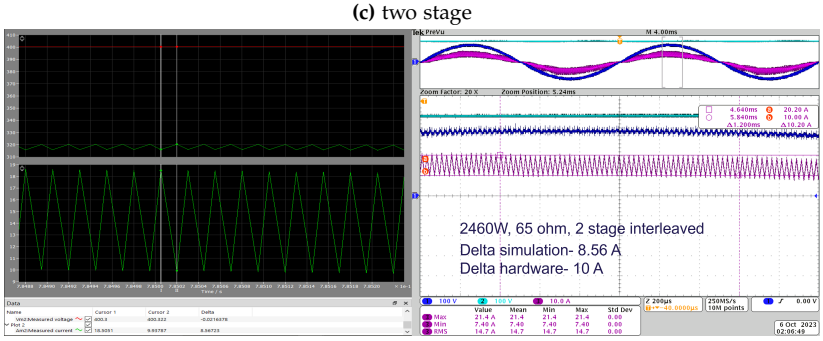
(a) three stage



(b) three stage zoomed



(c) two stage



(d) two stage zoom

Figure C.2: Comparison of hardware results with simulation results for three stage and two stage interleaved operation

Mode	CCM	QCM	% change
Inductor volume [cm^3]	396	158	-60.101
EMI filter volume [cm^3]	73	78	6.849315
Heat sink volume [cm^3]	250		
Semicondoctor devices volume	30		
Gate driver volume [cm^3]	60		
Capacitor volume [cm^3]	840		
Total Volume [cm^3]	1649	1416	-14.1298
Output power [W]	7360	7360	
Power density [kW/dm3]	4.463311	5.19774	16.4548

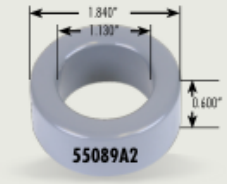
Table C.1: Power density calcultaion

Appendix D
Boost inductor design

Core Data

46.7 mm OD

Core Dimensions	OD	ID	HT
Before Finish (nominal)	46.74 mm/1.840 in	28.70 mm/1.130 in	15.24 mm/0.600 in
After Finish (limits)	47.63 mm/1.875 in	27.89 mm/1.098 in	16.13 mm/0.635 in



Permeability (μ)	A_L ± 8%	Part Number						
		Kool Mμ®	Kool Mμ® MAX	Kool Mμ® Hf	XFlux®	High Flux	Edge®	MPP
14	20	77092	79092	-	-	58092	-	55092
19	27	-	79079	-	78079	-	-	-
26	37	77091	79091	-	78091	58091	-	55091
40	57	77095	79095	-	78095	-	-	-
60	86	77090	79090	-	78090	58090	-	55090
75	107	77094	-	-	78094	-	-	-
90	128	77093	-	-	78093	-	-	-
125	178	77089	-	-	78089	58089	-	55089
147	210	-	-	-	-	58088	-	55088
160	228	-	-	-	-	-	-	55087
173	246	-	-	-	-	-	-	55082
200	285	-	-	-	-	-	-	55086
300	427	-	-	-	-	-	-	55084

Physical and Magnetic Parameters	
Window Area	610 mm^2
Cross Section (A_e)	134 mm^2
Path Length (L_e)	116 mm
Effective Volume (V_e)	15,600 mm^3
Area Product	81,800 mm^4

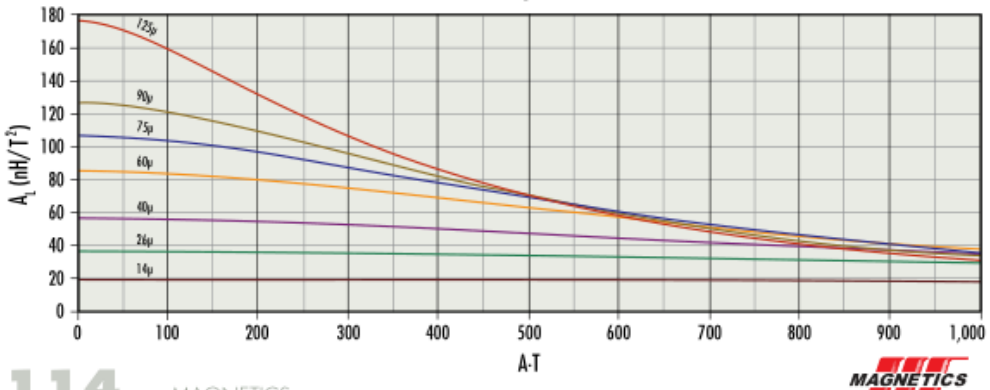
Wound Coil Dimensions*		
40% Winding Factor	OD	52.0 mm
	HT	24.9 mm
Completely Full Window	Max OD	66.3 mm
	Max HT	39.8 mm

Surface Area*	
Unwound Core	6,100 mm^2
40% Winding Factor	9,800 mm^2

Winding Turn Length*	
Winding Factor	Length/Turn (mm)
0%	52.0
20%	59.1
25%	61.0
30%	62.2
35%	64.5
40%	66.4
45%	68.2
50%	70.4
60%	74.7
70%	79.5

* See Toroid Winding pg. 19

Kool Mμ A_L vs. DC Bias



MAGNETICS

Figure D.1: Datasheet of 89 size core from Magnetics[15].

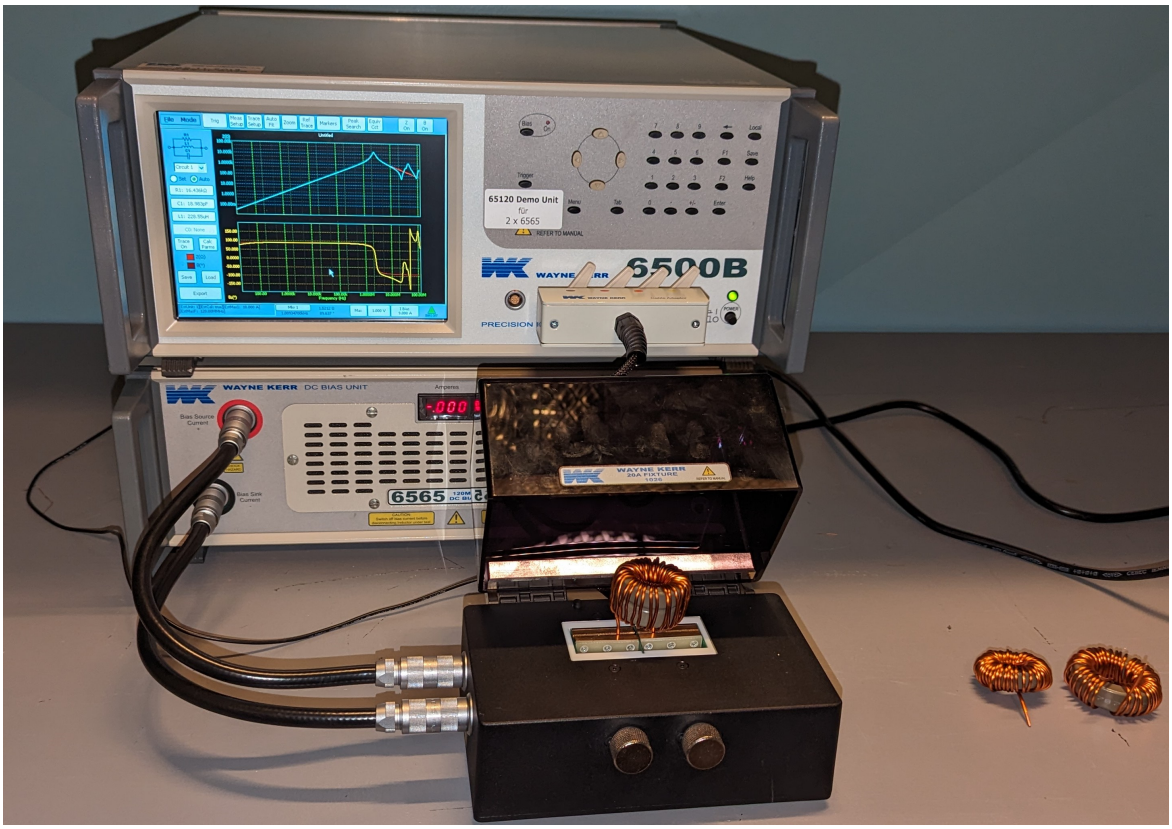


Figure D.2: High frequency testing of inductor using Wayne 6500B impedance analyser.

Appendix E
Three phase three stage interleaved boost PFC converter

The use of the designed single phase three stage interleaved PFC as phase modules for three phase three stage interleaved PFC is explored by doing simulation in PLECS. The topology used is as in the snap shot of PLECS simulation in Figure E.1

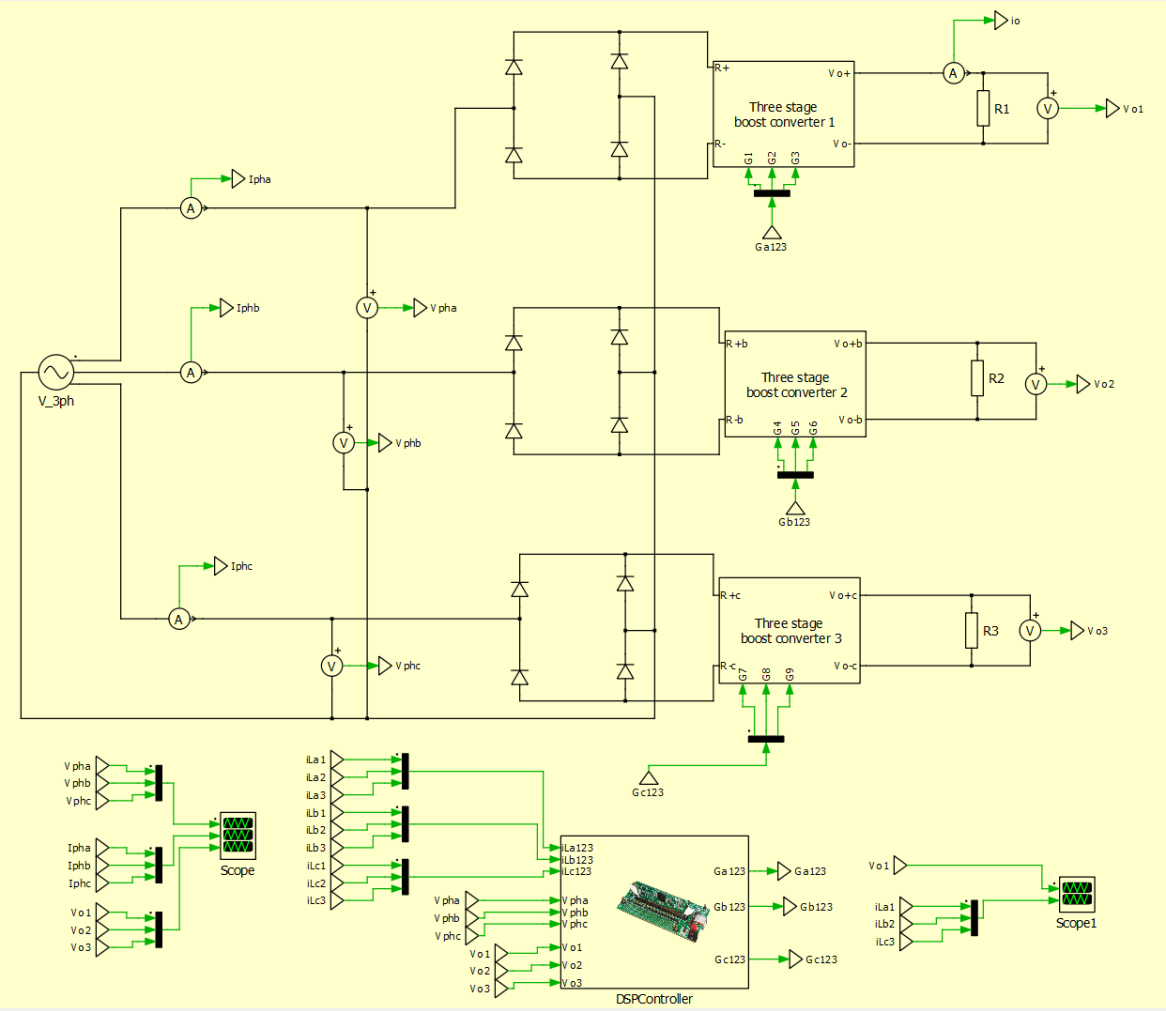


Figure E.1: PLECS simulation for three phase three stage interleaved boost PFC.

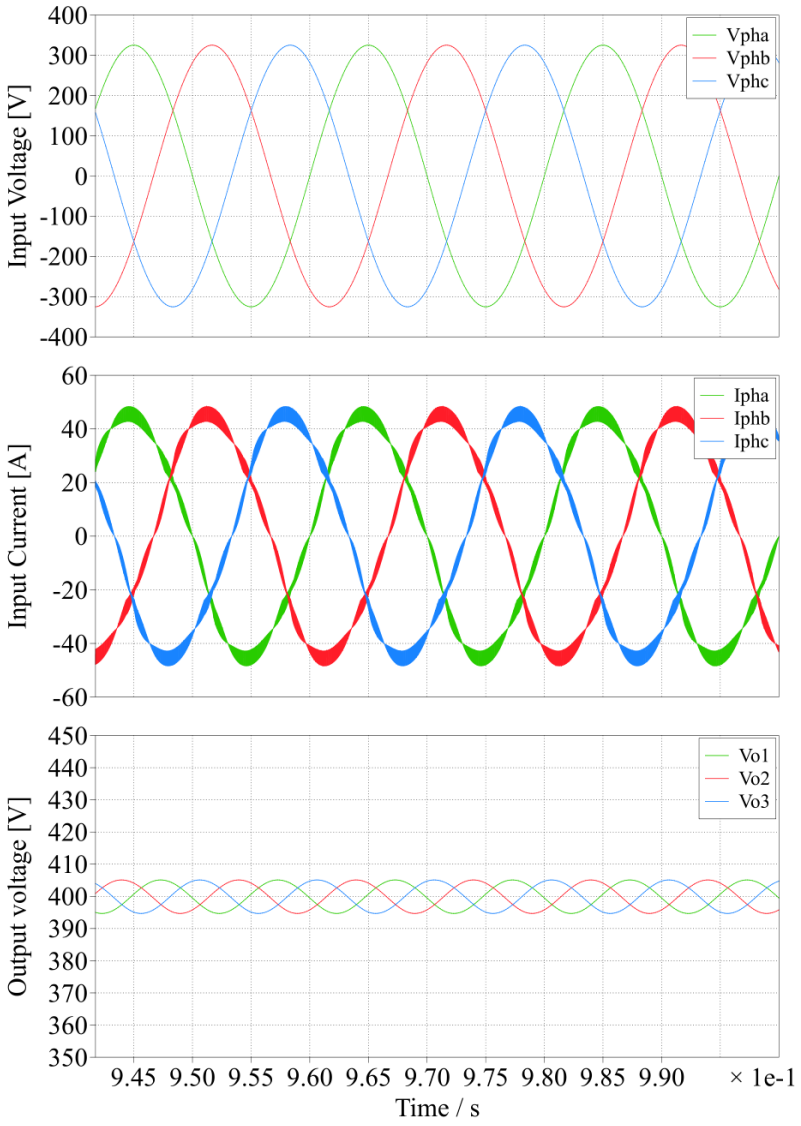


Figure E.2: Simulation result for three phase three stage interleaved boost PFC.