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Mitigation of Common-Mode and Circulating Currents in Power Supplies for Power-to-X Applications

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Mitigation of Common-Mode and Circulating Currents in Power Supplies for Power-to-X Applications

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Abstract:

Emphasis on the production of green hydrogen through Power-to-X (PtX) and the electrolysis process has strengthened significantly in the past decade. This has led to increased research activity on power supplies used for electrolyzer stacks. This thesis aims to propose a solution for the problems of common-mode and circulating currents associated with an infrastructure having multiple electrolyzer stacks. The proposed solution incorporates a simple topology consisting of an AC/DC rectifier with a non-isolated full bridge DC/DC converter. Multiple control schemes suitable for implementation namely Feedforward, PI, and PI+Feedforward are explored. A scaled-down version is developed in simulation and as a hardware setup to simulate the operations and challenges associated with a real system. The control strategies are systematically explored and implemented on the hardware setup. The simulated results obtained at each stage are used as a reference for validation of the results obtained with the hardware setup. Although the simulations show promising results for the applied control scheme, the hardware results only partially conform to them. The inconsistencies between the simulated and measured results are discussed and the positive trends are highlighted.

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Summary

In the last decade, focus towards Power-to-X technologies has increased significantly. As the demand for hydrogen production continuously increases, the power supplies for electrolyzers are becoming center of attention. In the first chapter of this thesis, the State-of-the-Art is thoroughly explained, highlighting existing challenges relevant to power supplies dedicated for hydrogen production that lead to the formulation of the problem statement and objectives.

The second chapter covers background concepts relevant to the project and provides a detailed description of the hardware setup and the selected components. Design considerations, limitations, and supporting diagrams are included. A system overview is also presented through a block diagram, outlining individual components such as the AC power supply, isolation transformer, Rectifier and Inverter solution, and the Auxiliary board for measurements, protection, and control. The chapter further discusses the development of the PCB to accommodate auxiliary circuits and the microcontroller interface.

The importance of modeling the system in a simulation environment is emphasized for feedback on performance and safety during hardware implementation. The chapter explains the cause of common-mode components, the stages of a DC/DC converter control development to mitigate these components, and presents simulation results and observations. The tools used for modeling and simulations are LTspice and PLECS, each with its specific advantages.

The hardware setup and its features are described, including the debugging process, validation of measurement circuits, and safety functions. The chapter concludes with the presentation of conducted measurements to establish the validity of the control approach, discussing inconsistencies and solutions encountered during the operation of the system.

Resume

Igennem det sidste årti har der været et øget fokus på Power-to-X-teknologier. Eftersom efterspørgslen efter brintproduktion stiger konstant så er strømforsyningerne til elektrolysatorer også kommet under et øget fokus. I det første kapitel af denne afhandling er ”State-of-the-Art” grundigt gennemgået og eksisterende udfordringer, der er relevante for strømforsyninger dedikeret til brintproduktion, er identificeret. Udfordringerne har ført til udarbejdelsen af problemformuleringen og dens målsætninger.

Det andet kapitel omhandler baggrundsbegreber, der er relevante for projektet og giver en detaljeret beskrivelse af hardwareopsætningen og de valgte komponenter. Designovervejelser, begrænsninger og understøttende diagrammer er inkluderet. En systemoversigt præsenteres også gennem et blokdiagram, der skitserer individuelle komponenter såsom AC-strømforsyningen, isolationstransformer, ensretter- og inverter-løsning, og hjælpekortet til målinger, beskyttelse, og kontrol. Kapitlet diskuterer yderligere udviklingen af PCB’et til at rumme ekstra kredsløb og mikrocontrollergrænsefladen.

Vigtigheden af at modellere systemet i et simuleringsmiljø understreges i forhold til ydeevne og sikkerhed under hardwareimplementering. Kapitlet forklarer årsagen bag ”common-mode” strøm-komponenterne og stadierne for en DC/DC konverter kontrol til at minimere disse komponenter og præsenterer simuleringsresultater og observationer. De anvendte værktøjer til modellering og simuleringer er LTspice og PLECS, hver med sine specifikke fordele.

Hardwareopsætningen og dens funktioner er beskrevet, inklusive fejlretningsprocessen, validering af målekredsløb og sikkerhedsfunktioner. Kapitlet afsluttes med præsentation af udførte målinger for at fastslå validiteten af kontrolmetoden, diskutere inkonsistente tendenser og løsninger, man støder på under driften af systemet.

Preface

This document presents a Master of Science Thesis completed during the spring semester of 2022 at Aalborg University's Department of Energy. The thesis falls under the specialization program in Power Electronics and Drives. It was carried out from February to May 2022, and it corresponds to a workload of 30 ECTS points for each student involved.

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I, Angelos, would like to express my gratitude to my family, my fellow students and friends for their support and guidance during this remarkable journey in Denmark. This experience would not have been the same without you by my side.

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List of Abbreviations

Abbreviation:	Description:
AC	Alternating Current
ADC	Analog-To-Digital Converter
AMR	Anisotropic magnetoresistance
CMRR	Common-Mode Rejection Ratio
DAC	Digital Analog Converter
DC	Direct current
DSP	Digital Signal Processor
FFT	Fast Fourier Transformation
GMR	Giant Magnetoresistance
HFR	High Frequency Resistance
MCU	Microcontroller Unit
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
P2H	Power-to-Hydrogen
PCB	Printed Circuit Board
PE	Protective Earth
PEM	Polymer Electrolyte Membrane
PtX	Power-to-X
PWM	Pulse Width Modulation
SMD	Surface-Mount Device

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Chapter 1

Introduction

This chapter aims to introduce the reader to the broad concept of Power-to-X and narrows it down to the focus area of the present work which is power supplies used in hydrogen production. Further, the State-of-the-Art is explained in detail, and existing challenges are located. These challenges lead to formulating a problem and certain objectives are defined to address it. Finally, the methods and processes along with limitations are presented.

1.1 Power-to-X

Since the past decade, the world has been in constant pursuit of "Green" sources of energy in order to reduce the heavy dependency on non-renewable fossil fuels and the carbon footprint of human existence to make the planet sustainable. As the demand for energy has been ever-increasing with industrialisation and urbanisation, more emphasis is being placed on the possibility to have this demand met through clean energy sources. Efforts are being made on multiple fronts to have more sustainable solutions in day-to-day lives of humans and one such focus area is called PtX, where 'X' could be gaseous and liquid fuels, heat, mobility, etc. The goal of PtX is to convert and/or store electrical energy generated through renewable sources such as solar and wind in order to reuse it as a clean source of energy. In Power-to-Heat (P2Heat) and Power-to-Mobility (P2M), surplus renewable electrical energy is directly used as the source of power to produce heat and for charging Electric Vehicles (EV). The P2Heat process is brought about by using electrical heating methods and heat pumps to direct heat where it is needed. P2M offers charging of EVs through renewable energy where the energy stored in the batteries can then be utilised to support the Grid during peak periods if the vehicle is not in use.

The biggest area of interest in PtX has been in the production of green fuels using renewable electrical energy, as per [1]. Today, various processes and technologies are being investigated to develop highly efficient systems that carry out the conversion of electrical energy to fuels. The advantage of converting electrical energy to fuel is the ease of storage and transportation of fuel which would increase the usage of the available renewable source. Hydrogen is considered an important fuel which is also used for the production of other gaseous and liquid fuels. As per [2], till the year 2020, less than 1% of the total hydrogen production around the world was being produced through renewable electrical energy. [3] talks about plans to install pipelines in Denmark for the transportation green hydrogen from the locations of production to various parts of the country and to Germany. Thus, Power-to-Hydrogen has become one of the most important areas of PtX and is illustrated in Figure 1.1.

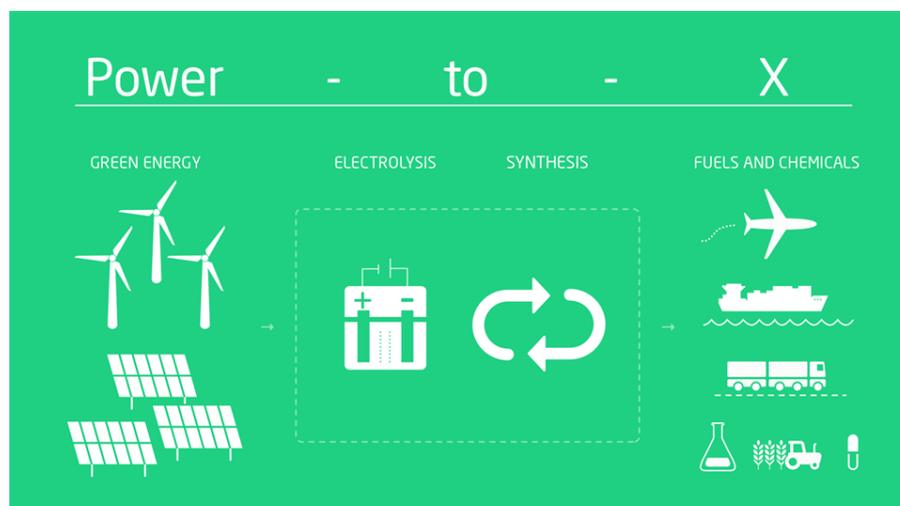


Figure 1.1: Power-to-Hydrogen process and end applications [4]

1.1.1 Power-to-Hydrogen

P2H is the process of converting renewable electrical energy into gaseous energy carriers such as hydrogen and methane. The hydrogen produced through P2H can be directly injected in the natural gas grid or used as fuel for transport, heating and various industrial processes. For these processes, it can go through further steps to be synthesised into more complex green fuels such as methanol, kerosene and ammonia [5].

The process of P2H primarily involves splitting of water using electricity to produce hydrogen and oxygen through the technique called Electrolysis. The device performing the process of electrolysis is called as an Electrolyzer. The electrolyzer consists of negatively charged cathode and positively charged anode which are separated using a membrane called separator. An important component in an electrolyzer is the electrolyte since pure water lacks a large number of ions required for the conduction of current in the electrolysis process.

The working principle of the electrolyzer is such that when a current flows through it, each electrode (anode and cathode) attracts ions of the opposite charge. Through the introduction of electrons at the cathode and their removal at the anode, the desired products can be removed from the electrolyte at the electrode, based on their physical state of existence. The two commonly used electrolysis technologies are alkaline electrolysis and PEM electrolysis.

In the alkaline electrolysis process, the electrodes are immersed in an aqueous solution of caustic potash (KOH) or caustic soda (NaOH) as electrolytes with OH^- atoms being the charge carriers. When a DC current is applied to the electrodes, the water molecules split and dissociate into hydrogen at the cathode and oxygen at the anode. The PEM electrolyzers use a solid specialty plastic material as an electrolyte. In a PEM electrolyzer, with a flow of DC current, water reacts at the anode to form oxygen and positively charged hydrogen ions (protons) [6]. The hydrogen ions flow selectively through the PEM and towards the cathode where they combine with the electrons to form hydrogen gas which are shown in Figure A.9 and Figure A.10.

1.1.2 Trends and On-going Activities in Power-to-X

Various studies conducted over the past few years show that PtX is being looked at more and more as a solution to enabling the availability of green fuels moving forwards. With the push for clean energy gaining traction in almost all industries, hydrogen has seen a great demand as a source of green energy and this has been backed by the possibility of large-scale production of green hydrogen through multiple electrolysis processes as explained above. An increasing number of countries are formulating plans to set up PtX farms of large capacities in order to tackle problems arising due to pollution and the resulting climate change. In [7], the Danish government's strategy for PtX has been explained in detail with a list of existing and upcoming projects throughout the country. It can be observed that the oldest existing PtX plant has a capacity of 1.2 MW while one of the upcoming projects is expected to reach up to 1 GW. The trend for the growth of capacity is similar in Europe, as observed in Figure 1.2 from [8].

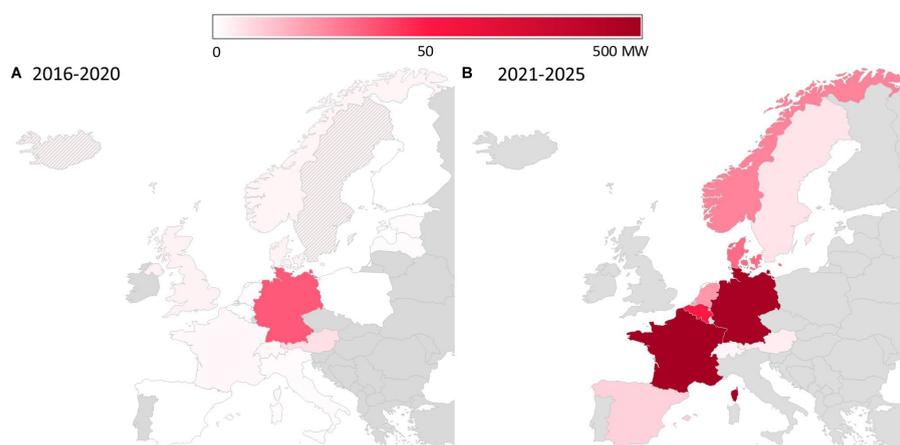


Figure 1.2: Capacities of PtX plants for existing and proposed projects across Europe

Across the world, many large PtX projects are being undertaken to scale up the green hydrogen production to the GW levels to power regions around the farms with renewable energy. [9] describes in great detail, a 1 GW PtX farm project that is forecast to be completed by the year 2028. The European Union aims to have 40 GW of electrolyzer capacity installed by 2030 and the Hydrohub Innovation Program is one of the projects contributing towards the achievement of this goal. In an online article, [10], the news of a project to build a 1.5 GW plant has been covered. [11] talks about the many projects being planned in Latin America with the highlight being one in Uruguay which is planned to have a production capacity of 2 GW and expected to start producing green fuels like e-jet fuel, methanol and ammonia from the year 2026.

Due to increasing plant capacities, the need for electrolyzer units with higher power levels has also followed with a particular interest in Alkaline and PEM electrolysis technologies. Out of the two, PEM has been a topic of greater interest due to its faster response time and higher efficiency which enables better control of hydrogen production. [12] talks about the characteristics of PEM electrolyzers in comparison with the alkaline type. Along with increasing capacities of the PtX plants, there are also possibilities being explored about having Energy Islands where electricity is produced from solar and wind farms which is mainly fed to PtX

farms for producing hydrogen with only the surplus energy being directed to the utility grid. Such a concept has also been highlighted in [7].

Many organisations around the world have been actively involved in developing alkaline and PEM based electrolyzer stacks with power in the magnitude of hundreds of kW for alkaline electrolyzers and up to a few MW with PEM technology. This development has also placed a huge demand on electric power supplies of the same and higher power range as the electrolyzer stacks since they can be used for unit electrolyzer stacks as well as for PtX farms where many hundreds of electrolyzer stacks could be deployed for generation of hydrogen at a large scale. In the implementation of large PtX farms, the efficiency of the power supplies would play a big role in the overall system efficiency since the power levels could be about hundreds of MW. As would be explained further, the power supplies are also one of the crucial components determining the performance parameters of the electrolysis process.

1.2 Power Supply for Electrolyzers : Considerations and Requirements

In order to achieve higher production rates, multiple cells are connected in what would be called an electrolyzer stack. As a next step, multiple stacks can connect in multiple configurations, several in series, in parallel or both combined. The required current and voltage for these configurations vary from tens to thousands of amperes and from a few to hundreds of volts [13]. The selection of a proper power supply depends on these voltage and current demands and the given electrolyzer application. For example, an installation connected to the AC grid requires a rectification stage while an installation coupled to a photovoltaic park does not. However, different power converter topologies can affect in different ways the system's performance. To this, there is a series of requirements and specifications that need to be taken into consideration before the selection of the adequate power supply, some of which are mentioned in [13] and below.

- System efficiency [14], [15], [16]
- Control of the DC current
- The system's interaction with the grid [17], [13] [18]
- Current fluctuation [19]
- Cost and Reliability

As energy consumption constitutes the highest part of the cost of the produced hydrogen by water electrolysis, achieving high efficiencies is crucial. Different power converter topologies have different efficiencies based on their operating characteristics. Switching-mode converters include switching losses in comparison with line-frequency diode rectifiers. Furthermore, the quality of the output current plays a significant role in the electrolyzer's efficiency. In [14], the current supplied by a transistor based power supply leads to a 10% better efficiency than that of a current supplied by a thyristor based one. That is because, although the average current was maintained in both cases the same, in the thyristor based supply, the low frequency switching

generates low frequency and large-amplitude harmonics in the output current and voltage which is very difficult to be filtered in practice. In a more generic way, in [15] the impact of the current fluctuation on the efficiency of an alkaline electrolyzer was investigated by imposing different types of AC current components on the supplied DC current. The presented results show that any deviation from purely DC current causes an efficiency decrease. Specifically the offset, the frequency and the ripple factors are the parameters that affect the efficiency. According to [16], similar results were reached in the case of PEM electrolyzers. To this, both the power supply topology and the quality of its produced current should be taken into consideration.

The system's interaction with the grid is a parameter that should not be ignored. In [17], the power quality and reactive power on the AC side of an alkaline electrolyzer was investigated for the case of a thyristor based power supply. The result is that for different loads the reactive power has very high values and the power factor is low. To mitigate this issue, modern transistor rectifiers can be utilized. Recognizing that electrolyzers can be configured as smart dynamic loads, [18] discusses power converter topologies and their control scheme to enable electricity grid services. Controlling the active and reactive power requires a controllable power supply for the electrolyzer system. At the same time, input current harmonics injected in the AC power supply must meet the international standards and requirements such as IEEE 519-2014 [13].

Apart from its impact on efficiency, the current ripple is linked with degradation phenomena in the electrolyzers. In [19], three different typical power converter current waveforms (triangular, sinusoidal and constant) were applied to PEM electrolyzers in order to measure the impact of the current ripple on their durability. Specifically, four cases were characterized after a 3000 hour operation. These are, a triangular current ripple of 10 kHz, a triangular current ripple of 1 kHz, a sinusoidal current of 300 Hz and a constant current. The study concludes that in the case of the triangular current of 10 kHz, the degradation is the most significant and that the HFR of the electrolyzer experiences the highest increase.

In order to manage the hydrogen production, controlling the current that is fed to the electrolyzer is essential. A simple diode rectifier connected directly to an electrolyzer does not give this possibility. On the other hand, in a thyristor based rectifier, by controlling the firing angle, the output voltage and current can be controlled. Another way to achieve controlled DC power to the electrolyzers is by using IGBT or MOSFET based AFE as the rectifier. Diode, AFE and thyristor based rectifiers could be used independently as shown in Figure 1.3a to supply an electrolyzer stack or they can be combined with DC/DC converters that allow further controllability to the current as depicted in Figure 1.3b.

The cost and reliability play also a key role in the selection of the power supply. Thyristor designs exist since decades in the electrolyzer business and not only do they offer the highest current density but also low cost and a degree of controllability. Systems with few components in the rectifier (as also in total) are considered more robust and cost effective. For that reason, rectifiers based on diodes and thyristor are still dominating the market at high power applications.

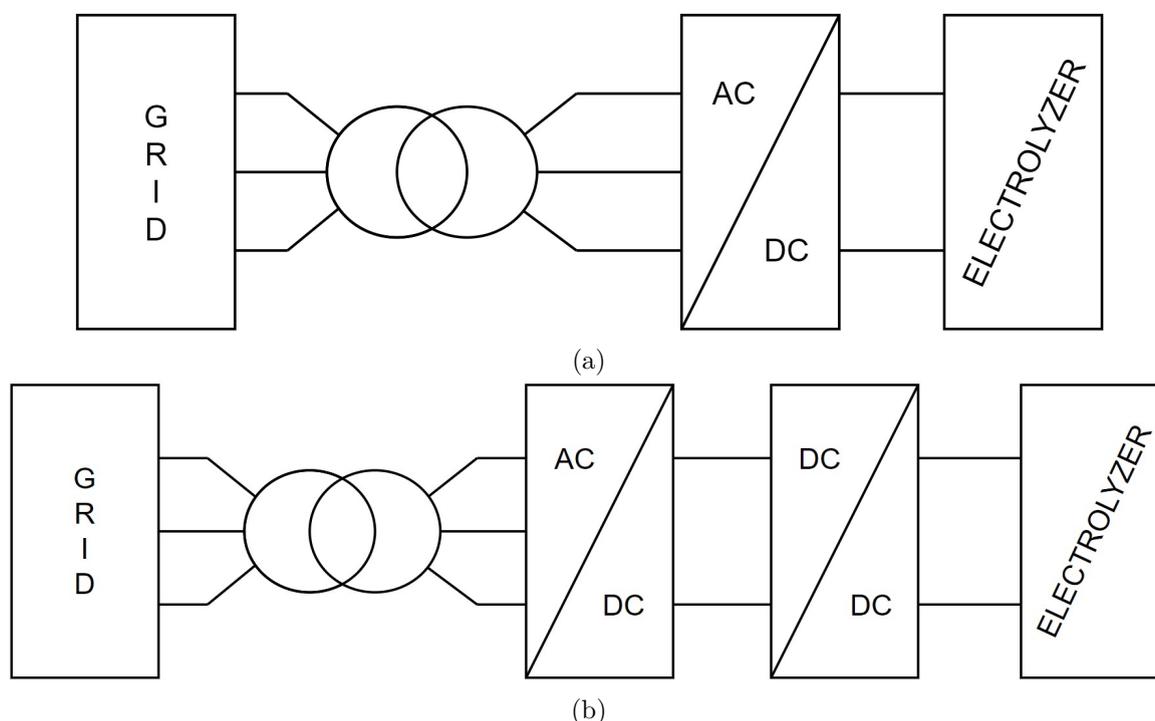


Figure 1.3: (a) Power supply that utilizes a single controlled AC/DC stage (Thyristor based rectifier or an AFE), (b) Power supply that utilizes a controlled/uncontrolled (diode based rectifier) AC/DC stage and a DC chopper

Finally, the choice of a specific architecture/converter topology is motivated by balancing the cost of the system, the degree of control over it and the redundancy to meet the needs of the application. High redundancy and degree of control leads to higher performances but also higher costs [20].

1.3 State of the Art

As discussed in Section 1.1.2, the green transition is leading to the creation of big and different types of hydrogen production plants. Such a project is the One-GigaWatt Green-Hydrogen Plant project which is described in [9]. The authors present the plant's technical overview where a modular design method is apparent. According to this modular design, several electrolyzer stacks are connected together into groups. As it can be seen in Figure 1.4, each group is supplied by a power block that consists of a MV transformer and a rectifier. In the described setup, each transformer-rectifier power block has a 40 MW capability and it is connected to four stacks of PEM electrolyzers of 10 MW each or two stacks of alkaline electrolyzers of 20 MW each. The two alkaline stacks are connected in series while the PEM stacks are connected as two parallel strings where each string consists of two stacks in series (series-parallel configuration as per [20]). Given the advantages of this modular concept, similar and more architectures of connected stacks are introduced in similar projects and are proposed in the literature.

In its technical report, [21], a manufacturer of power supplies for electrolyzers presents the

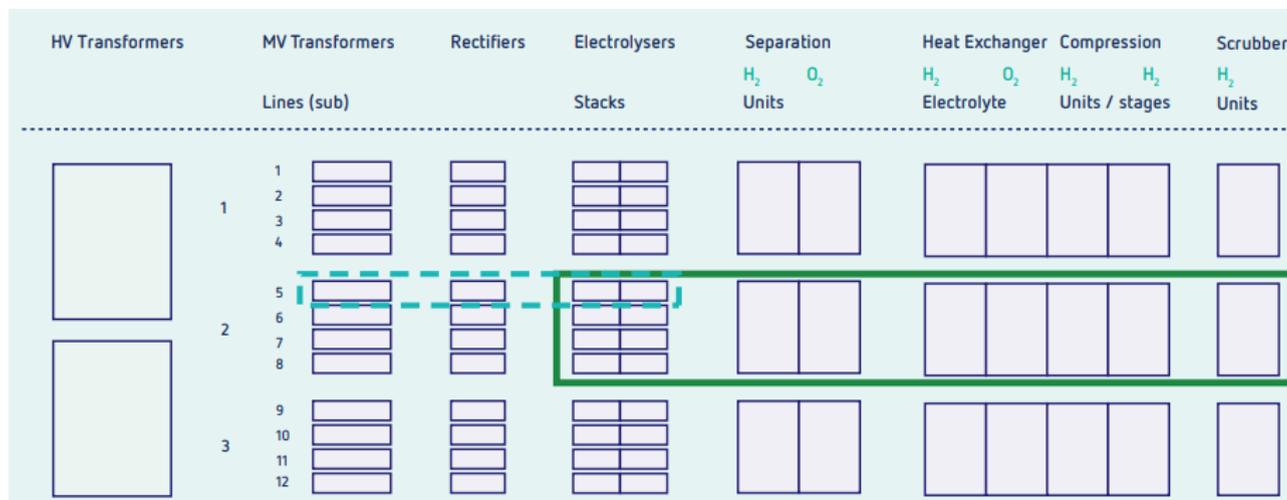


Figure 1.4: Part of the modular layout proposed for the One-GigaWattGreen-Hydrogen Plant project of [9].

configuration of two stacks connected in series and supplied by two thyristor-based AC/DC converters as per Figure 1.5. It can be observed that in series connection of two stacks, their common point is grounded while the transformer in this setup is not.

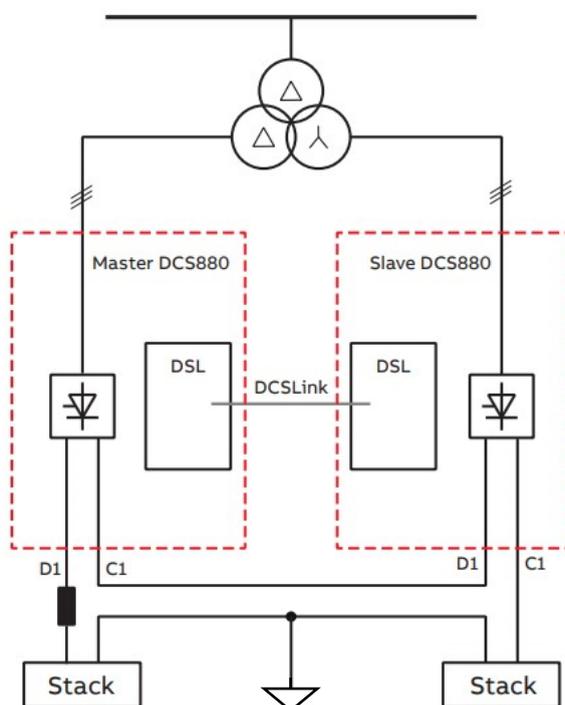


Figure 1.5: Thyristor-based power supply for two electrolyzer stacks connected in series [21]

In case the transformer was grounded, the existence of both, the grounded common point in the electrolyzers and the grounded neutral in the transformer would introduce the issue of

common-mode currents flowing through the formed ground loop as highlighted with red dashed lines in Figure 1.6.

From the power supply considerations mentioned in Section 1.2, such currents are considered harmful both in terms of efficiency and degradation of the electrolyzers.

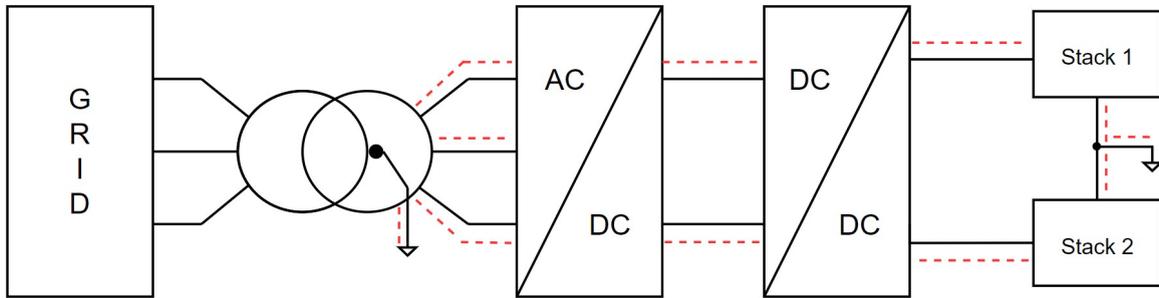


Figure 1.6: Formation of ground loops due to earthed transformer and electrolyzer stacks

The degradation of an electrolyzer stack impacts several of its characteristics and it is reflected in its equivalent resistance and internal voltage. This causes an imbalance in the voltage drop across each stack of Figure 1.6.

In order to meet the requirement of controlling the DC current and voltage across each stack, the aforementioned case of series-parallel configuration, should not simply be connected as two parallel connected strings to one power supply. A way to achieve the parallel connection that enables the voltage control along the series of stacks is the one depicted in Figure 1.7 that incorporates one DC/DC stage per series of stacks. In this case, however, the issue of imbalances is further extended. Supposing unequally degraded stacks, the nodes $M1$ and $M2$ could be under different potentials and therefore an additional circulating current could flow between the parallel stacks. This circulating current is depicted by blue dashed lines in Figure 1.7.

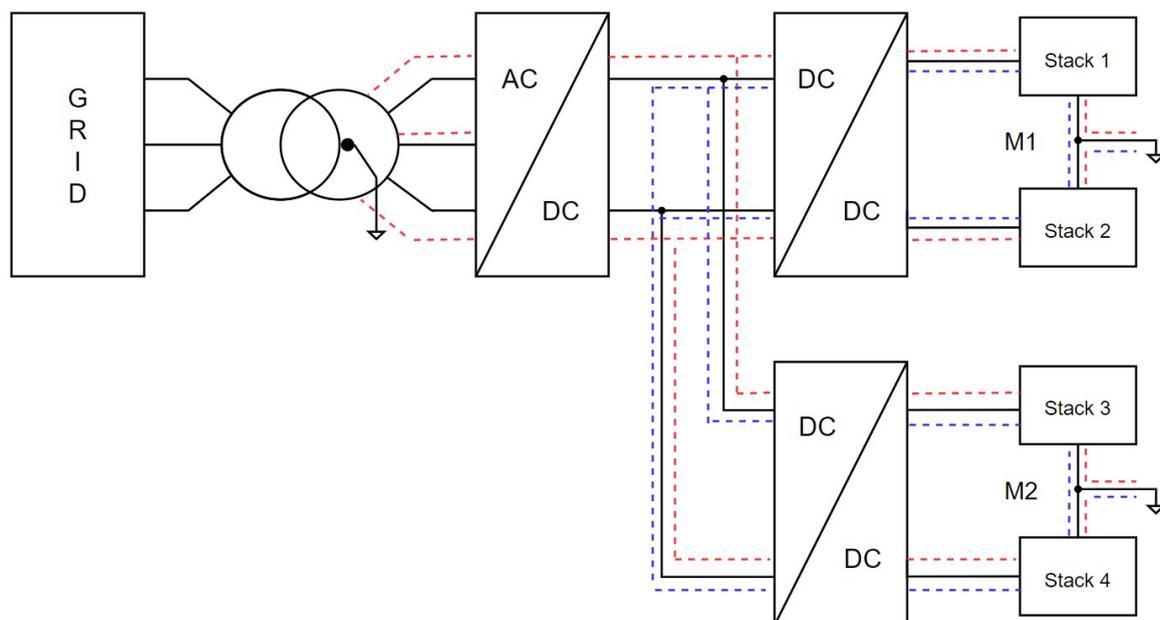


Figure 1.7: Formation of circulating current loops and ground loops in the parallel configuration of stacks

To tackle this issue, the converters of [18] incorporate galvanic isolation. However, this approach would only add in cost, losses and volume of the power supply.

1.4 Problem Formulation

As described in the above sections, for the system shown in Figure 1.7, the following problems exist:

- Common-mode currents: flow of common-mode currents through ground loops formed due to the presence of common-mode voltage at points $M1$ and $M2$.
- Circulating currents: flow of circulating currents between paralleled stacks through ground loops due to the imbalance of voltages across the stacks.

These circulating currents are capable of deteriorating the electrolyzer's overall performance. The decrease in its expected lifetime, the degradation phenomena, the reduced efficiency and the subsequent increased operating costs constitute important reasons into the direction of minimizing the presence of these currents.

Both the circulating currents and the common-mode currents can be minimized by controlling $M1$ and $M2$ to be equal to each other and equal to the earth potential. This can be attributed to the control of each paralleled system's midpoint by its respective DC/DC converter. This implies that if the midpoint of each system is controlled to a value equal to the earth potential then all the midpoints of the paralleled systems will be equal to each other. This means that the problems mentioned above can be merged into the problem of controlling

the midpoint of one system.

1.5 Project Objectives

The goal of this project can be formulated as finding a solution to control the midpoint of one system while maintaining the desired DC current through the stacks.

An important step to achieving the goals of the project is to define the scope and objectives which set the target milestones and success criteria.

These objectives are defined as the following:

- Finding a DC/DC converter topology that achieves the goals of the project with a simplistic design and low component count
- Developing a control scheme for the differential and common-mode current through the stacks and ground loop for the single system of Figure 1.6
- Developing a simulation model for the validation of the control scheme
- Implementing and validating the simulation results on a hardware setup
- Documentation of results

1.6 Methodology

Given the limited available time of four months to complete the master thesis project, it is important to follow structured processes and methods that would lead to successfully meeting the predefined objectives on time. In addition to the time constraints, there are component and laboratory constraints. Aiming to meet these constraints, as a first step, the described system will be simplified to an equivalent system of lower power, reduced complexity and higher development feasibility. This topology should be less complicated in terms of simulation, hardware development and testing but yet reliable and representative of the original system.

For the management and implementation of the project, the parallel approach of simulation and hardware development tasks of Figure 1.8 is followed. According to this, the completion of simulations and hardware development are planned to converge at the same time, leading to the testing phase. The simulation tools that will be used are LTspice and PLECS, and the averaging method shall be applied during development of the control scheme wherever needed to simplify the system analysis and to solve control problems algebraically. To save time on the hardware development, components that are available in the university will be preferred. Furthermore, in situations where a choice between 'Make v/s Buy' is required to be made, preference would be given to the solution that can be implemented with all the required functionalities in the shortest time. An attempt would be made to maintain high level of consistency between the simulation cases carried out and the experiments and validation performed on the hardware setup in the laboratory. The processes of modelling and simulation, hardware development including the problems faced and debugging, and finally, the results obtained through laboratory

tests and relevant observations shall constitute the documentation for the submission of this thesis.

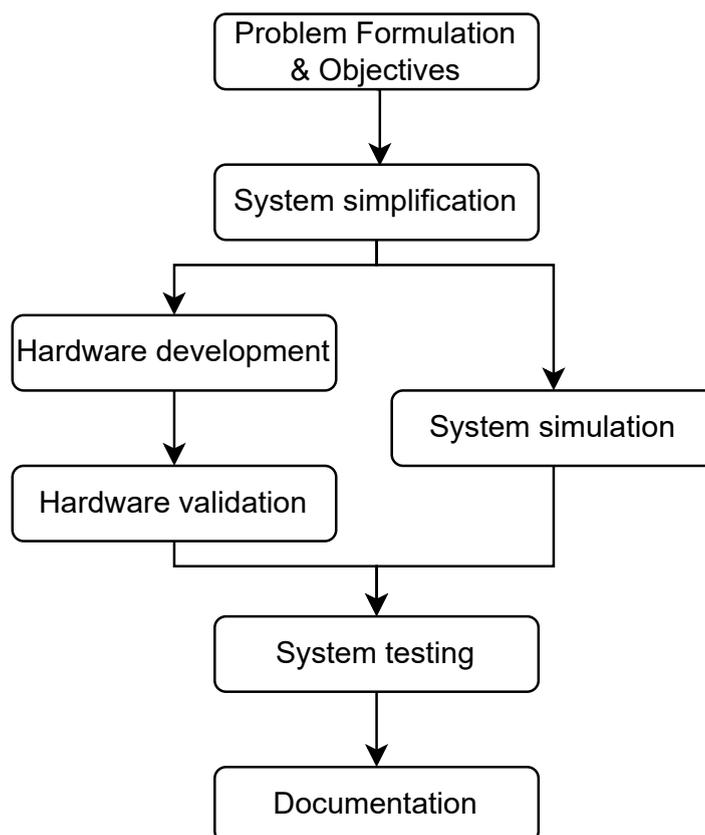


Figure 1.8: Flowchart of thesis tasks management.

1.7 Limitations

The scope of the project has been defined based on the constraints highlighted above in Section 1.6. Considering the aim of the project and time, the focus areas considered for investigation and implementation have been narrowed down to the following:

- The diode rectifier is considered as the AC/DC throughout the project due to its simplicity and availability.
- The implemented system has been based upon the TN-S system of earthing but the hardware setup will not use the main PE connection as will be explained later.
- Based on the problem formulation, focus throughout the project would be on working with a single system of DC/DC converter and load as shown in Figure 1.6.
- The switching frequency ripple component on the load current shall not be addressed through the control strategies as it can be independently handled by sizing filter components appropriately.

Chapter 2

Theoretical Background and System Description

In this chapter, are explained the background of topics that would be used throughout the project and in context of the report. The concepts are also relevant for a better understanding of the system that is aimed to be built for the hardware setup which has also been described in detail in the second half of this chapter. Also, the various design considerations and limitations with regard to the components and equipment used in the laboratory along with supporting equations, diagrams and flowcharts are included.

2.1 Theoretical Background

2.1.1 Electrolyzer Model

The electrolyzers are part of a larger electrical ecosystem that could include the grid, photovoltaics, wind farms and conventional power plants. Additionally, as mentioned in Section 1.2 they are supplied by different AC/DC and DC/DC converters to manage their operation. Therefore, obtaining an accurate electrical model of them that could be used for simulation purposes would be useful to predict their behavior under different conditions (static and dynamic).

A model for a single cell, reproduced from [22], is presented in Figure 2.1. The reversible potential, V_{rev} , corresponds to the minimum required voltage for the water electrolysis to be initiated. The ohmic resistances R_c and R_a refer the conductivity of the anode and cathode electrodes. R_{mem} and R_{ele} represent the ohmic resistance of the membrane and the electrolyte respectively. Finally, the combination of a current source and a capacitor refers to the activation over-potential. This is an extra electric potential required for the chemical reaction which occurs on the interface between electrodes and the electrolyte to cross an energy obstacle [23].

For stacks of multiple cells, considering that all the cells have similar physical performance and behavior the stack's total voltage is considered equal to the single cell voltage of Figure 2.1 multiplied by the number of cells.

In Figure 2.2 the current-voltage characteristic of a cell can be seen. In the steady-state and for currents higher than 2 A, the cell and stack's behavior is ohmic. For that reason, in the frame of this project, the electrolyzer stacks will be modelled as resistors both in simulations and the hardware setup.

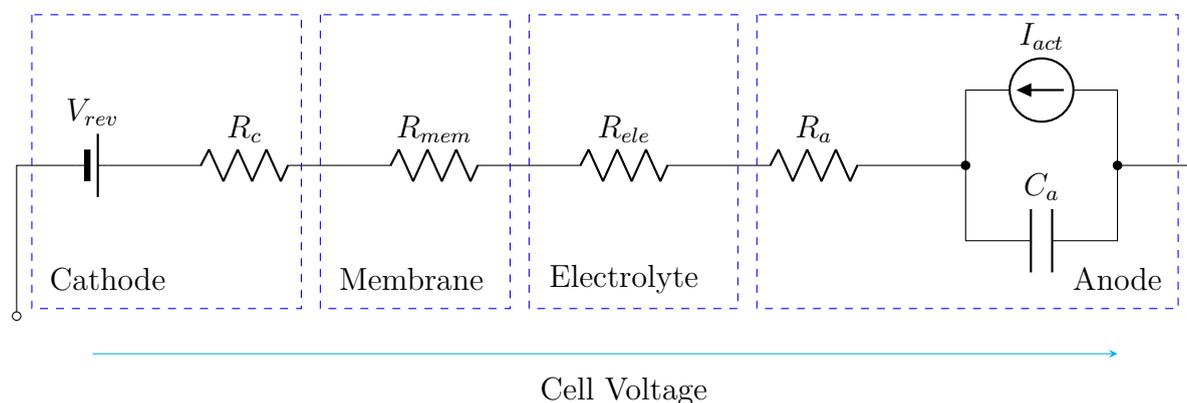


Figure 2.1: Simplified cell model as per [22] – others propose R//C instead

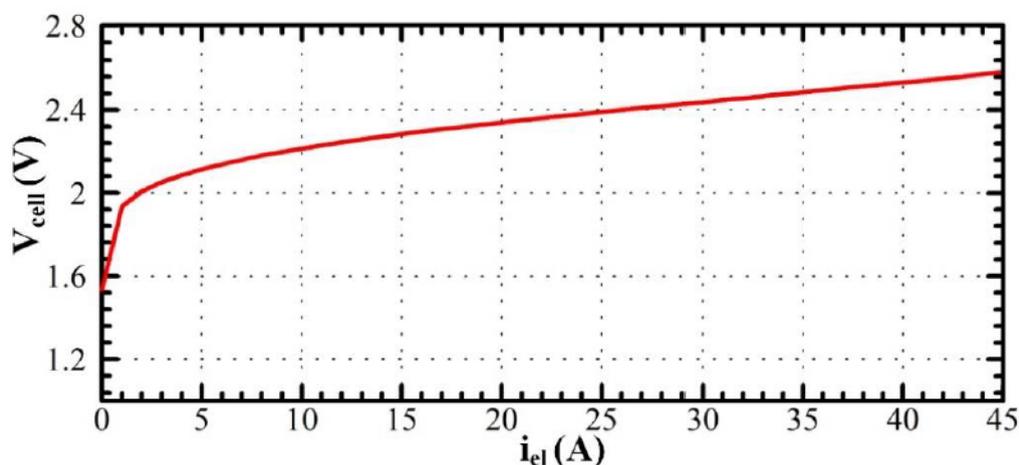


Figure 2.2: Voltage–current characteristic of the employed cell in [22].

The total ohmic resistance of a single cell is typically quantified by the high frequency resistance, R_{HFR} , which can be accessed via electrochemical impedance spectroscopy [24]. As mentioned in Section 1.2, the degradation effects result to a higher resistance and therefore in this project the degradation effect will be modeled in the simulations and laboratory measurements by changing the load resistance by a percentage of 10-20%.

2.1.2 Earthing Systems

Specific parts of a power system or an electrical power supply and load system are earthed with the purpose of safety or for specific functional requirements. An equipment can be earthed to prevent accidents and risks related to the operator of the equipment where the equipment is not earthed directly but has a connection to the earth conductor through a Residual Current Device (RCD). The RCD detects a fault and breaks the circuit, thereby preventing the operator from getting an electrical shock. Some equipment could also be earthed for functional requirements where the earth conductor is used as the return path for the high currents flowing through the equipment. Earthing is used for protection purposes where it provides a sink for high currents

that are not caused due to electrical faults. For example, during a lightning strike, the earthing of a system located close-by would prevent the high build up of charge from reaching an appliance by diverting the excess current to earth.

The international standard IEC 60364 defines three earthing arrangements - TN, TT and IT where the first letter indicates the connection between earth and power supply equipment (transformer or generator) and the second letter indicates the connection between earth and the electrical device being supplied. The 'T' stands for direct connection to Terra/Earth, the 'I' stands for insulated from earth and the 'N' stands for Neutral where the earth connection is provided as a part of the distribution network in different combinations with the Neutral connection.

The TN system of earthing is widely used for power distribution networks in Europe and in this system, the star point (Neutral) of the three phase supply is connected to earth and the device that is being supplied is connected to earth through this point. The TN system has the following three variants which are shown in Figure 2.3:

- **TN-S** system is an arrangement where the Neutral (N) and Protective Earth (PE) are connected at the transformer's star point to earth but have separate conductors for the device
- **TN-C** system is where the Neutral (N) and the Protective earth (PE) are combined in the same conductor which is connected to the supply star point and the earth
- **TN-C-S** system is where the Protective earth (PE) and Neutral (N) are combined in the same conductor between the substation and the site, which is connected to the star point of the supply and the earth but is then split into separate N and PE lines

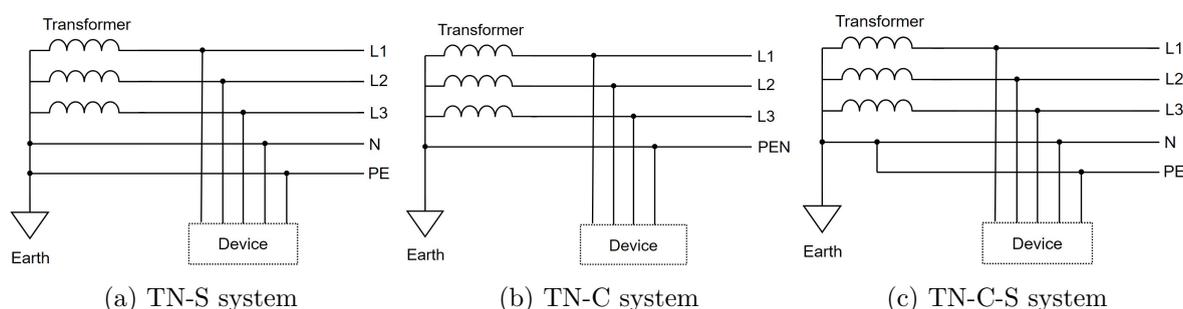


Figure 2.3: TN systems

Out of these variants, predominantly the TN-S system is used for industrial installations which states that the transformer star point or Neutral (N) should be earthed as well as the consuming electrical device. Thus, throughout this project for simulations and hardware, the secondary of the transformer shall be with its neutral point connected to earth.

2.2 System Description

The overview of the system that is to be implemented is shown as a block diagram in Figure 2.4 where individual components are highlighted and named. As can be seen, the system consists of the 3-phase AC power supply of 400 V line-line from the grid followed by a 1:1 isolation transformer which has its Neutral terminal earthed as per TN-S system explained earlier. An integrated Rectifier + Inverter solution (EVAL board) was found in the market with suitable ratings and this would form the power stage of the hardware setup. The Auxiliary board houses the systems such as measurements, protection and control with the help of sensors and a microcontroller. The load, as explained in Section 2.1.1, shall be resistive banks with their midpoint earthed, again in adherence to Figure 1.5. Each of these individual components are explained further in depth in this chapter and Chapter 4.

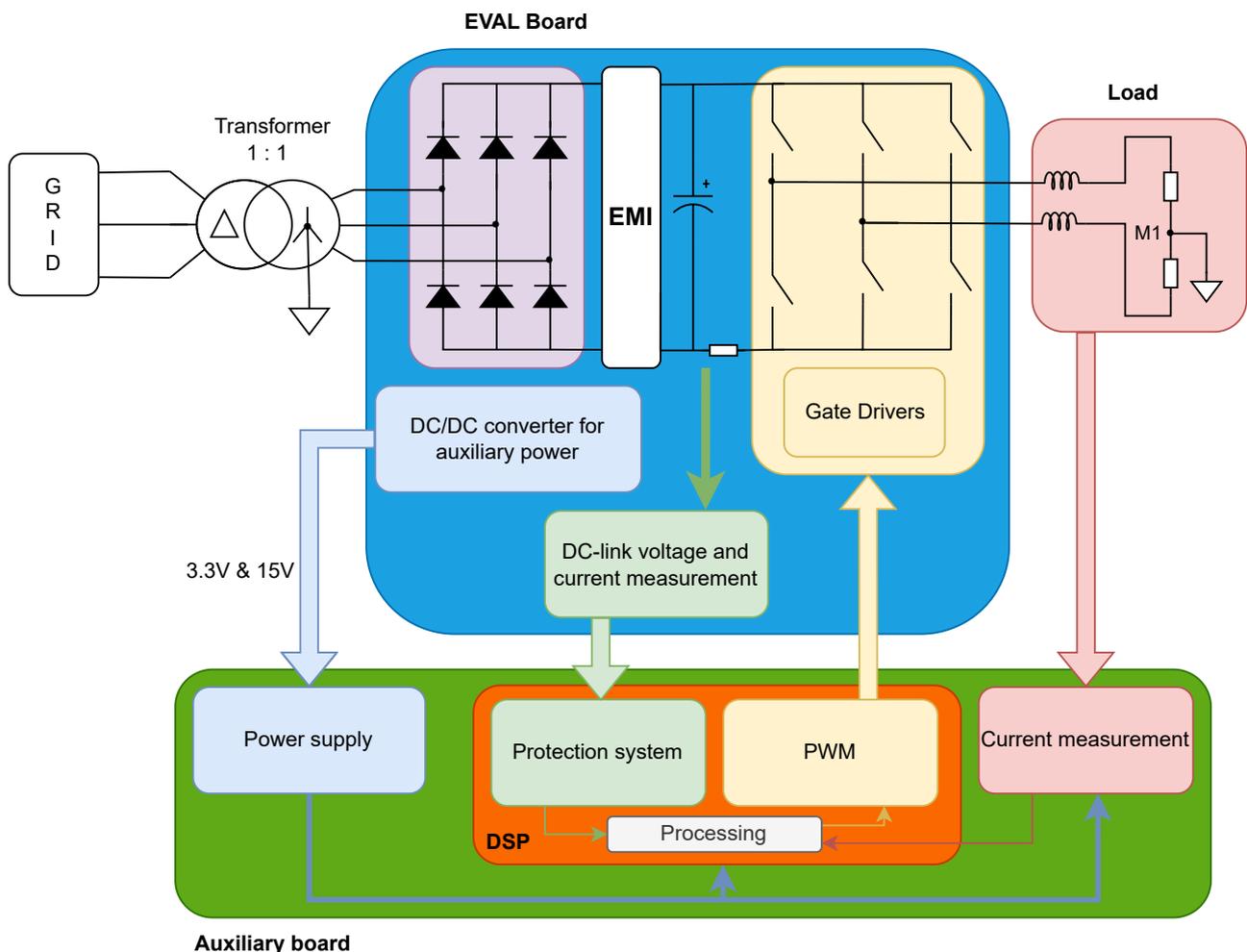
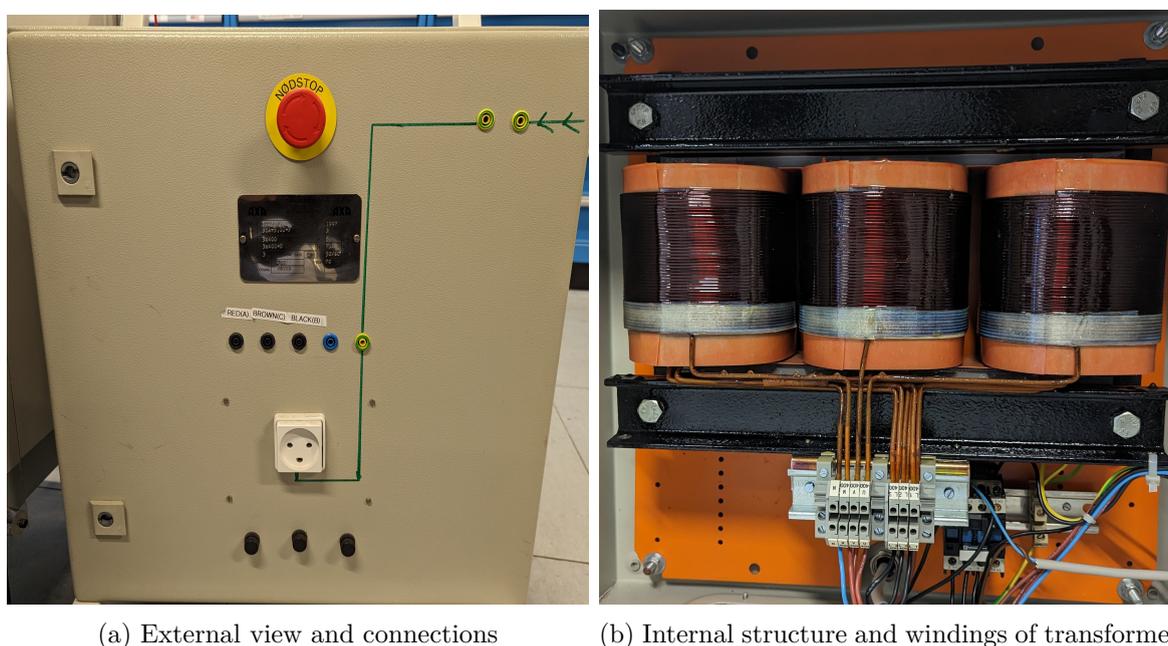


Figure 2.4: System block diagram

A PCB was made to accommodate the auxiliary circuits and microcontroller to be interfaced with the evaluation board which would be explained later in Chapter 4.

2.2.1 Transformer

In the real application a transformer is required to step down the medium voltage to low voltage. Additionally, it provides galvanic isolation from the rest of the system. In the present work, the three phase transformer of ?? is deployed for this purpose. It is a Delta-Star transformer rated at 5 kV A, 400 V, 7.2 A and a ratio of one. For the simulations to be as accurate as possible, a model of the transformer is needed. However, as the electrical characteristics were not provided, various tests were performed to estimate the transformer's parameters. The copper resistance was estimated by applying a DC voltage on its primary and secondary winding and were found to be 1.5Ω for the primary and 0.6Ω for the secondary. The leakage and magnetizing inductances were found through the Short-Circuit Test and the Open-Circuit Test by following the steps described in [25]. The leakage and magnetising inductances on the primary side obtained through these tests are 3.25 mH and 17 H respectively. As the transformer has a Delta-Star combination, the ratio of number of windings per phase is $\frac{1}{\sqrt{3}}$, which gives the leakage inductance on the secondary side to be 1.08 mH.



(a) External view and connections

(b) Internal structure and windings of transformer

Figure 2.5: External and internal views of transformer

Finally, establishing the reliability of the estimated transformer's parameters is an important step for the simulation results to be accurate. For this, a comparison between the simulated values in LTspice and the measured values of the primary and secondary line voltages (V_{ab} and V_{RS}) and line current (I_a) was conducted. The setup included the transformer, a diode rectifier and a resistive load of $10\Omega/40\Omega$. The simulated and measured values for both cases are gathered in Table 2.1 and the resulting percentage error is computed. As the operating voltages and currents are beyond 100 V line-line where the error is considered acceptable, the transformer's parameters will be used for the simulation model in Chapter 3. The percentage error is calculated as follows:

$$\%error V_{RS} = 100 \cdot (V_{RS}^{sim} - V_{RS}^{meas}) / V_{RS}^{meas}$$

$$\%error I_a = 100 \cdot (I_a^{sim} - I_a^{meas}) / I_a^{meas}$$

Table 2.1: Comparison between the simulation and the measured values of the line-voltage (on the secondary of the transformer, V_{RS}) and current in the case of different primary line voltages V_{ab}

	V_{ab}	V_{RS}	I_a	% error V_{RS}	% error I_a
Simulation result	30 V	27.67 V	2.67 A	7%	16%
	50 V	46 V	4.56 A	7%	20%
	75 V	69 V	6.89 A	6%	4%
	100 V	97.7 V	2.58 A	0.3%	1%
	150 V	146.6 V	3.9 A	0.2%	2%
	200 V	195 V	5.2 A	0.5%	4%
Measurement result	30 V	25.7 V	2.3 A		
	50 V	42.8 V	3.8 A		
	75 V	65 V	6.6 V		
	100 V	98 V	2.55 V		
	150 V	147 V	3.8 V		
	200 V	196 V	5 V		

2.2.2 Power Stage

The power stage of the system consists of an AC/DC rectifier, an EMI filter, the DC-link and a three phase inverter as shown in Figure 2.4. Since the main objectives of the project were to develop a control scheme which could be implemented on hardware as soon as possible, a decision was made to use an integrated hardware system with AC/DC rectifier and the DC/DC converter rated for the power level of 5 kW, similar to the transformer. After consideration of available hardware options, the EVAL-M1-IM828-A from Infineon was selected as the power stage. The EVAL-M1-IM828-A is an evaluation board intended for application of motor drives, capable of operating at 320 - 480 V_{AC} rms and rated for up to 8 kW[26]. It also provides the flexibility of controlling each MOSFET of the inverter stage with a separate PWM input which is very useful for the present application where one or two half bridges of the inverter would be used as a DC/DC converter depending on the topology. Alongside these, the evaluation board comes with a common-mode and differential filter as well as basic measurements and a fan-based forced cooling arrangement. The evaluation board is shown below in Figure 2.6.

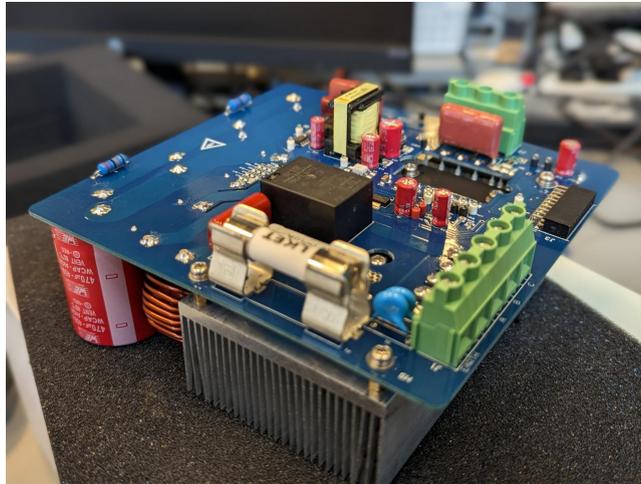


Figure 2.6: Evaluation board EVAL-M1-IM828-A from Infineon [26]

Following are the features offered by the evaluation board that would be used in the project:

- 2 or 4 out of 6 PWMs for control of MOSFETs
- Isolated dual output DC/DC converter stepping down from DC-link voltage to 15 V and 3.3 V for powering the microcontroller and auxiliary circuit
- DC-link voltage measurement
- DC-link current measurement for protection
- Built-in cooling system with fan

2.2.2.1 Inverter

The inverter is implemented on EVAL-M1-IM828-A using CIPOS Maxi which is a three phase bridge inverter module with SiC MOSFETs and integrated gate driver. The module accepts six 3.3 V PWMs and provides three phase outputs swinging between the DC-link voltage and Ground. The negative DC-link rail is considered as the Ground for the evaluation board and all the voltages are referenced to this Ground including the auxiliary circuit voltages. The gate driver uses the bootstrap technique with external capacitors to drive the high side MOSFETs. Further, the inverter module has protective features such as the Gate Kill bit which shuts down the gate drivers in the event of a fault, the ITRIP for overcurrent protection which activates if the drain current exceeds 34 A and analog output VTH to measure the temperature of the module.

2.2.2.2 DC-link Voltage and Current Measurement

The DC-link voltage measurement is provided by the evaluation board through a voltage divider network as shown in Figure 2.7.

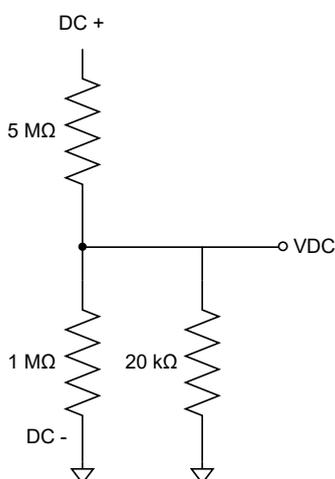


Figure 2.7: DC-link voltage measurement on evaluation board

The measured voltage VDC is given by,

$$VDC = V_{DC-Bus} \cdot \frac{1 \text{ M}\Omega || 20 \text{ k}\Omega}{(1 \text{ M}\Omega || 20 \text{ k}\Omega) + 5 \text{ M}\Omega} \quad (2.1)$$

$$VDC = V_{DC-Bus} \cdot 0.003944 \quad (2.2)$$

The signal VDC varies between 0 V and 2.13 V for DC-link voltage of 0 to 540 V respectively which can be read by the ADC of the micro-controller.

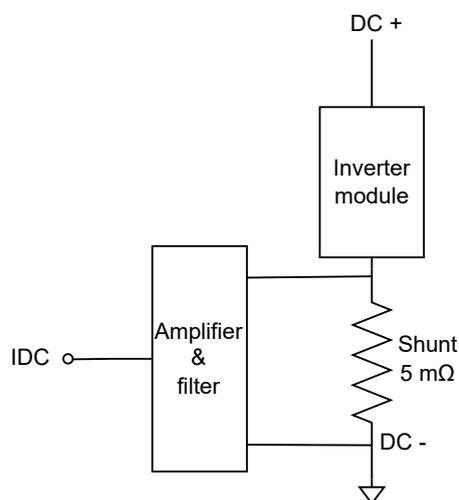


Figure 2.8: DC-link current measurement on evaluation board

The current is measured by means of two parallel shunt resistors of 10 mΩ each, connected between the Source pin of all the MOSFETs on the low side of the three phases and the

negative rail of the DC-Bus. The voltage drop on the shunt resistors is filtered and amplified by a differential amplifier on the evaluation board as per Figure 2.8 and [26]. The signal is amplified by a factor of 13.26 and the total measurement system has a sensitivity of 66.3 mV/A while maintaining an offset 0.6 V for sensing negative currents.

2.2.3 Stack Resistor

As explained in Section 2.1.1, it was decided to use resistors as load in the simulation model and hardware setup to represent the electrolyzers. For the hardware setup, however, with the transformer that is used, there is a limitation of power to 5 kV A which indirectly restricts us to a range of values for the resistors which are used as load. The values for the resistors were chosen as shown in Table 2.2.

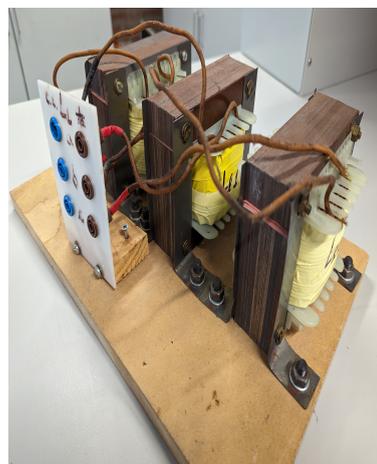
Table 2.2: Sizing of load resistors

Assumed power factor of the diode rectifier	0.95
Total maximum usable power	$0.95 \cdot 5000 = 4.75 \text{ kW}$
Maximum AC input voltage	400 V line-line
Maximum DC-Bus voltage	$400 \cdot 1.35 = 540 \text{ V}$
Maximum DC-link current	$4750/540 = 8.79 \text{ A}$
Maximum differential load voltage	540 V (with 100% duty cycle)
Load resistance with two serially connected resistors (with 100% duty cycle)	$540/8.79 = 62 \Omega$

Thus, based on the above calculations, it was decided to use two variable resistors of up to 32Ω and rated for $> 9 \text{ A}$. The resistors used for the hardware setup provide resistance of up to 40Ω and are rated for 10 A, shown in Figure 2.9a. With a variable resistance, another possibility to control the power level of the system becomes available along with the possibility to emulate electrolyzer degradation, as explained in Section 2.1.1.



(a) Resistor



(b) Inductor

Figure 2.9: Resistor and inductor used for hardware setup

2.2.4 Inductors

In order to filter the switching frequency ripple that would be present in the load current, two inductors were placed in series between the half bridges and the resistive loads. As the switching frequency was decided to be 10 kHz, a ripple of 10% on the maximum DC current (9 A) was considered as the design parameter. The total value of inductance required to limit the ripple at 10% is obtained as shown below:

$$v_L = L \cdot \frac{di}{dt} \quad (2.3)$$

where v_L is the total voltage across the inductors, di is the ripple current and dt is the switching period

$$L = \frac{v_L \cdot dt}{di} = \frac{540 \cdot 0.1 \cdot 10^{-3}}{900 \cdot 10^{-3}} = 60 \text{ mH} \quad (2.4)$$

The total voltage seen across the two inductors is chosen to be 540 V since in the worst case, the entire DC-link voltage which is limited by the AC supply voltage, might appear across the load. As this 60 mH is shared by two series inductors, each inductor should have a value of 30 mH. However, the highest value of inductance available in the laboratory was 15 mH. A trade-off between higher ripple content and faster implementation was encountered and it was decided to use the available inductors for the hardware setup.

2.2.5 Load Current Measurement

Establishing a reliable current measuring method is essential for the control methods that are proposed later on. The source [27] gathers some key current sensing principles and applied technologies. Out of these, the most commonly used techniques for this kind of applications are presented and their performance is compared in Table 2.3. It should be mentioned that the technological progress is advancing fast leading to compact, small size and accurate sensors and therefore part of the following data may need to be updated. However, the final selection of a current transducer is based on the requirements of the presented application which include the DC capability, a reasonable accuracy and measuring range, the availability in the market and a simple assembly process. The galvanic isolation is also an important factor as it will become apparent in the next chapters.

Table 2.3: Current Sensing Performance, reproduced from [27].

	Bandwidth	DC capability	Accuracy	Isolation	Range
Shunt resistor	kHz-MHz	Yes	0.1 - 2 %	No	mA-A
Rogowski coil	kHz-MHz	No	0.2 - 5 %	Yes	A-MA
Current Transformer	kHz-MHz	No	0.1 - 1 %	Yes	A - kA
Hall effect	kHz	Yes	0.5 - 5 %	Yes	A - kA
Fluxgate	kHz	Yes	0.001 - 0.5 %	Yes	mA - kA
AMR	kHz	Yes	0.5 - 2 %	Yes	A
GMR	kHz	Yes	1 - 10 %	Yes	mA - kA

Even though fluxgate sensors have many advantages they are a potential source of noise and therefore will not be further discussed. As the Rogowski coil sensors are bulky, difficult to implement, expensive and they do not have the DC capability, they will not be further discussed either. Similarly the current transformer and the shunt resistor that operates based on Ohm's law are rejected due to the one's DC incapability and the other's lack of isolation. The GMR sensors are based on a technology that is still under development and for that reason they will not be used in the scope of this thesis. The AMR technology is excluded from the discussion as it requires special care on creating the tracks above the sensor. The only technology that serves the specified requirements in the Hall-effect and therefore it's basic theory will be presented.

Hall Effect

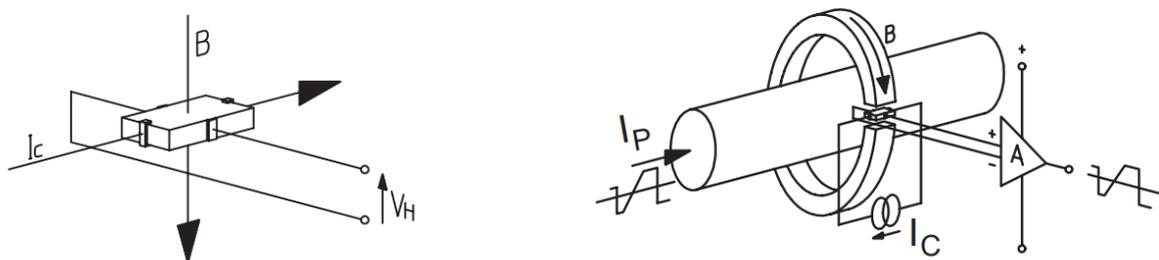
One of the most popular techniques employing the magnetic field is the Hall effect. Hall effect sensors are met in several technologies such as the open-loop and the closed-loop. The Hall effect is created by Lorentz forces, which act on charges moving through a magnetic field. A thin sheet of conducting material is traversed lengthwise by a control current, I_C , as per Section 2.2.5. The mobile charge carriers of this current are affected as the external magnetic flux, B , generates a Lorentz force, perpendicular to the direction of current flow. The resulting deflection of current causes more charge carriers to be located at one edge of the sheet, creating a potential difference referred to as the Hall voltage, V_H , [28]. This arrangement is described in Equation (2.5).

$$V_H = \frac{K}{d} \cdot I_c \cdot B + V_{OH} \quad (2.5)$$

where K is the Hall constant of the conducting material, d is the thickness of the sheet, and V_{OH} is the offset voltage of the Hall generator in the absence of an external field.

The current to be measured creates a magnetic field around it which is concentrated by the magnetic core. A hall generator positioned in a gap of the core, as shown in Figure 2.10 senses the magnetic flux density, while a control current I_c is fed to the hall generator. As the magnetic flux density is proportional to the primary current and the hall voltage proportional to the magnetic flux density, the output of the Hall generator is proportional to the primary current, plus the Hall offset voltage. At last, the hall voltage signal goes through a differential voltage amplification by electronics built into the current sensor. Open-loop current transducers amplify the Hall generator voltage to provide an output voltage [28].

The approach of the closed loop transducers is different resulting in a higher bandwidth but more information regarding the open loop and closed loop Hall effect can be found in [28].



(a) Representation of the electrical parameters of the Hall effect [28].

(b) Conversion of the primary current into an output voltage [28].

Figure 2.10: Open-loop and Closed-loop configurations.

Finally, the selected current transducer utilizes the open loop technology, it is incorporated on the auxiliary board and it is the product GO 10-SME/SP3 of LEM. Its current measuring range is from -25 A to 25 A and it has a sensitivity of 50 mV/A , [29].

2.2.6 Microcontroller

To achieve the objectives of this work a control scheme needs to be developed. The implementation of this control scheme in the hardware requires a MCU that provides the corresponding pulses to the gates of the MOSFETs and permits the interaction with the system. For this purpose the STM32F446-ARM Nucleo development board was selected and it is shown in Figure 2.11. It uses the STM32F446RET6 microcontroller which is an ARM Cortex M4 processor that can operate with frequencies up to 180 MHz and has a range of features that can be found in [30]. Apart from the prior experience with this specific board, it was selected because of the existence of STM32CubeIDE. STM32CubeIDE is an all-in-one multi-OS development tool, which is part of the STM32Cube software ecosystem. It is an advanced C/C++ development platform with peripheral configuration, code generation, code compilation and debug features for STM32 micro-controllers and microprocessors [31]. This software tool gives to the user the possibility to create a project, configure graphically the microcontroller and assign pins to peripherals while all the initialization code will be automatically generated. For this project, the useful peripherals of the micro-controller are the Timers and the ADC.

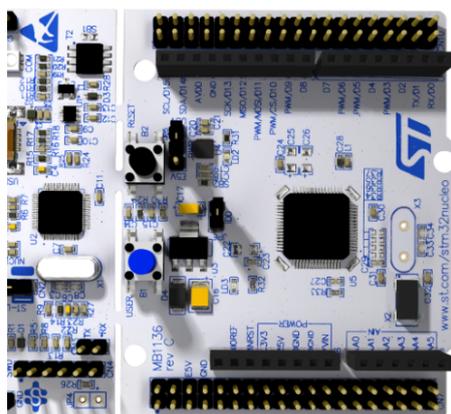


Figure 2.11: STM32F446-ARM Nucleo development board

2.2.6.1 Timer Peripheral

Fundamentally, Timers are pulse counters and given a fixed frequency incoming pulses, counting becomes a timing function. Although they have several features, they will be used for the purpose of PWM generation and triggering interrupts.

Once the Timer is initiated, the timer's value begin to increment at a rate that is specified by the Central Processing Unit (CPU) clock and prescalers. At specified moments, when this counter's value reaches a specified one, the timer can trigger an interrupt on which the program will handle a part of the user's code. In the user's part of the code, the micro-controller senses some signals through and based on a control scheme that is described in Chapter 3, two duty cycle reference signals, one for each leg, are generated.

As the system employs only two legs of the three-phase inverter, four gate signals are needed. The Timer peripheral of the micro-controller has several channels assigned to PWM generation and therefore, four channels with complementary PWM outputs and with programmable dead time are used. The generation of pulses in the gates of the MOSFETS is based on the comparison between the reference signals and the carrier signal which is the counter signal. When the reference signal has a higher value than that of the carrier, the PWM channels of the micro-controller are active for the high side MOSFET of each leg. At the same time the lower MOSFET of the leg is receiving a complementary signal and thus does not conduct. Between these two signals, a dead time of 500 ns is applied to make sure that shoot-through events are avoided. The switching frequency is set at 10 kHz. In Figure 2.12, the carrier signal, the reference signal and the instances of the triggered interrupts are shown in a more graphical way.

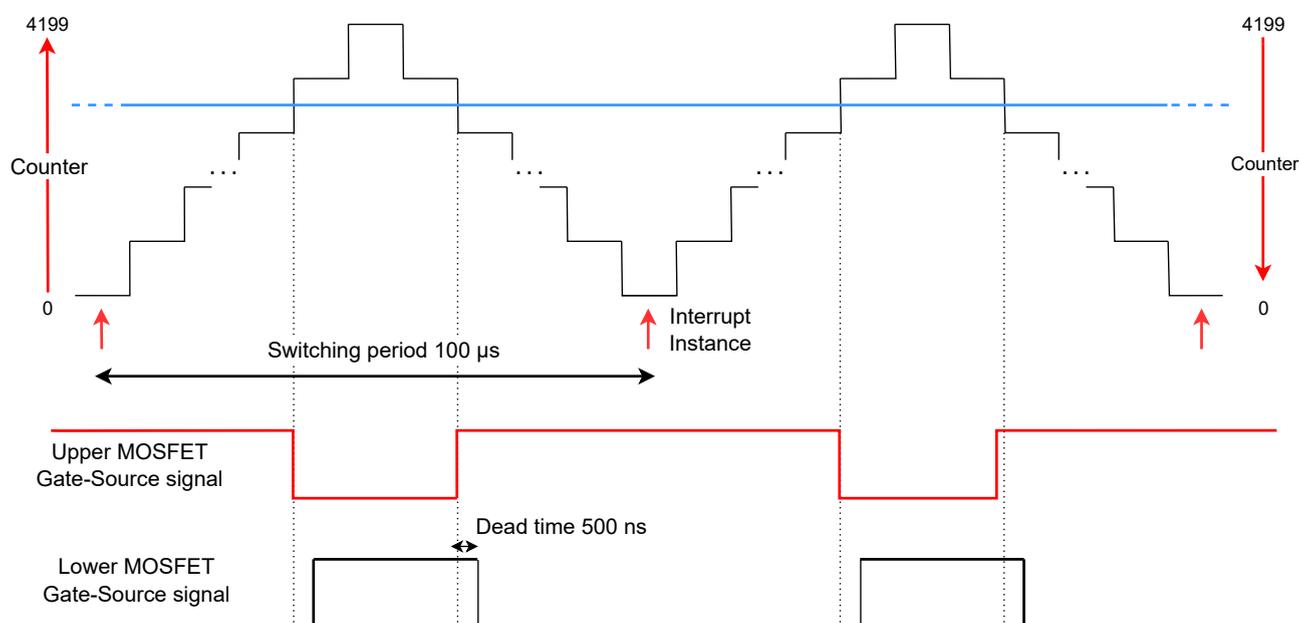


Figure 2.12: Timer scheme and PWM generation

2.2.6.2 ADC Peripheral

As mentioned earlier, there are four signals that need to be sensed by the micro-controller. This is achieved by using four ports of the micro-controller as ADC. For the conversion to be as accurate as possible the ADC resolution is set at 12-bits. This means that the input voltage in the ADC can be perceived in the digital range of 0 to 4095. As the range of the analog values that can be detected ranges from 0 to 3.3 V, the micro-controller is able to detect changes in its input voltage of 8.056 mV.

Additionally, the conversions generally demand a specific time to be completed and based on the application this time can be of significant importance. For example, to measure the single phase instantaneous electrical power, the current and voltage signals should be sampled and converted at the same time. For that reason there are several ADC modes that can be used and are further discussed in [32].

For this application, it is important measuring the currents that flow through the resistors as close as possible in time. Additionally, it is important that all four measurements are completed during the 100 μs of one period. This is important so that there is one interrupt per switching period and the new duty cycle value is estimated before the new switching period starts. Based on these two requirements, the four samplings and conversions are performed consecutively, requiring a total time of 62 μs as highlighted in Figure 4.3.

2.2.6.3 Micro-controller Functions and Operation

Finally, a flow chart of the way that the micro-controller operates can be seen in Figure 2.13.

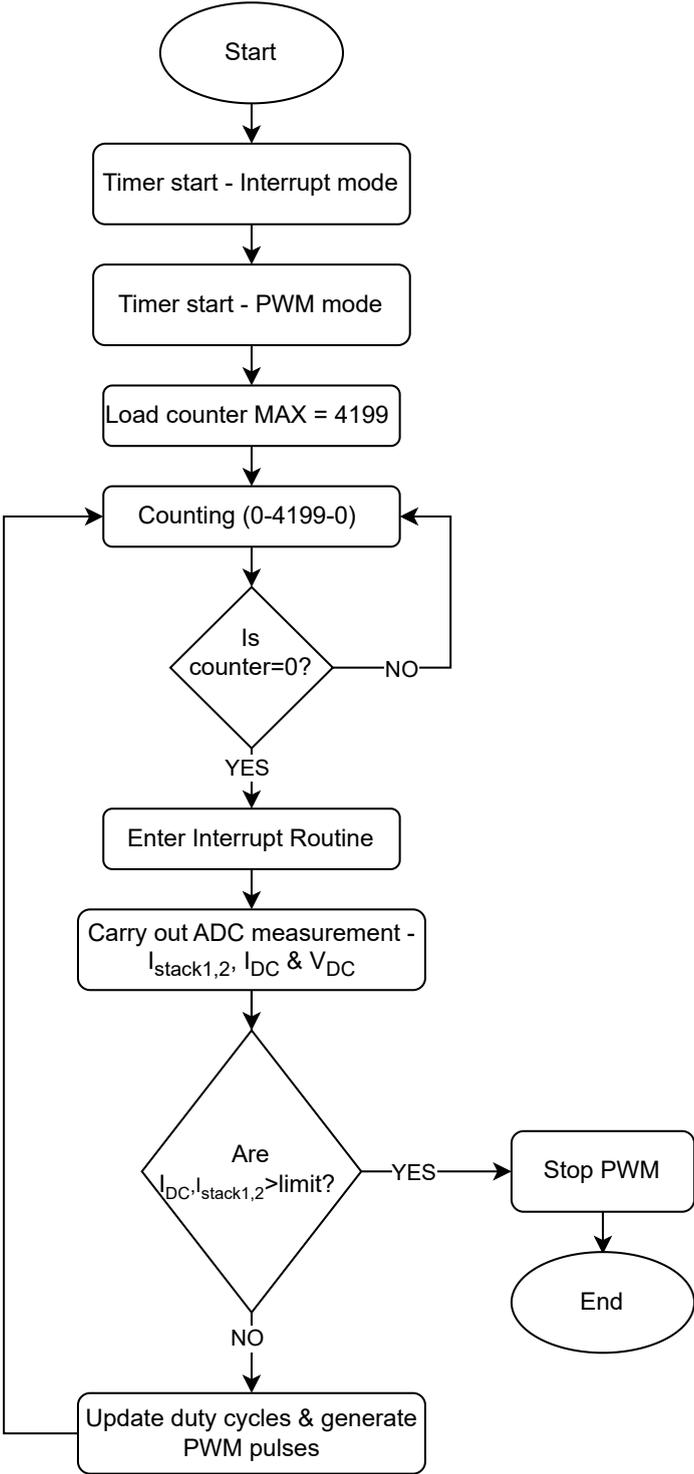


Figure 2.13: Flow chart of the micro-controller operation

Chapter 3

System modelling and Simulations

Modelling of the project's system in a simulation environment is an important step towards implementing the system on hardware. It provides important feedback on system performance and parameters which help in maintaining the safety of the equipment and personnel during hardware implementation.

In this chapter, the cause of the common-mode components is outlined and the stages of development of the DC/DC converter control are explained. Besides these, supporting simulation results and observations that led to the final stage are added. The approach used to develop the control of the DC/DC converter has also been specified for each topology and relevant waveforms are included for better illustration of the results.

The tools utilised for modelling and simulations are LTspice and PLECS. LTspice is used extensively for simulating device-level performances and circuit operations. The SPICE simulation environment is especially useful and accurate for the transient response of devices and systems. On the other hand, PLECS is more system-oriented with ease of development of control, electrical, thermal systems and prediction of performances. As such, on some occasions, PLECS might ignore certain transient behavioural responses at the device level to generate faster and more representative results at the system level.

3.1 Origin of Common-Mode Voltage

Introduced in Section 1.4, the common-mode current was one of the problems that the project aimed to solve in the power supply setup. In order to eliminate the common-mode current through the stacks which would lead to their degradation and affect hydrogen production, it is required to find the cause of the common-mode voltage that leads to the flow of this current. Thus, a simple 6-pulse diode rectifier model is simulated without the DC/DC converter to observe the voltages and currents with a load of two resistors representing the electrolyzer stacks connected in series and their midpoint earthed. Throughout this chapter, these resistors are named *Rstack1* and *Rstack2* in all the simulation models.

The model used for simulation is shown in Figure 3.1 which is developed to reflect the hardware equipment used in the lab setup. This includes the three phase transformer modelled according to Section 2.2.1 with the Neutral of the secondary side of the transformer and the common point of the stack resistors connected to the earth, based on the TN-S system of earthing. The resistances, *Rcom*, *RT-PE* in the ground loop represent the wire resistance of the lab setup and their values are representative.

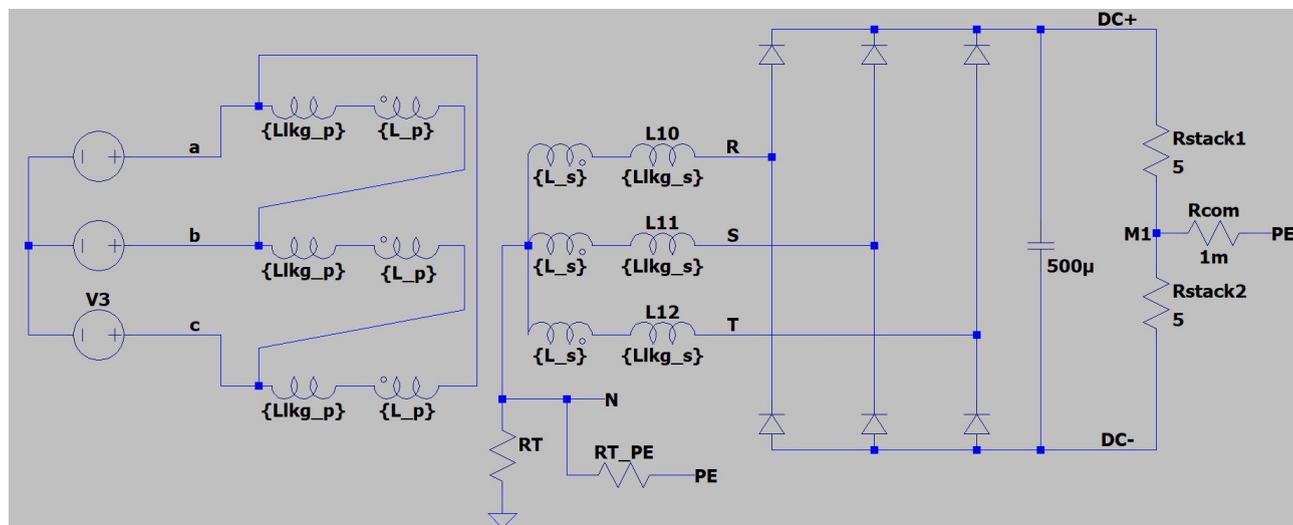


Figure 3.1: Rectifier system with serially connected stacks earthed at common point as load

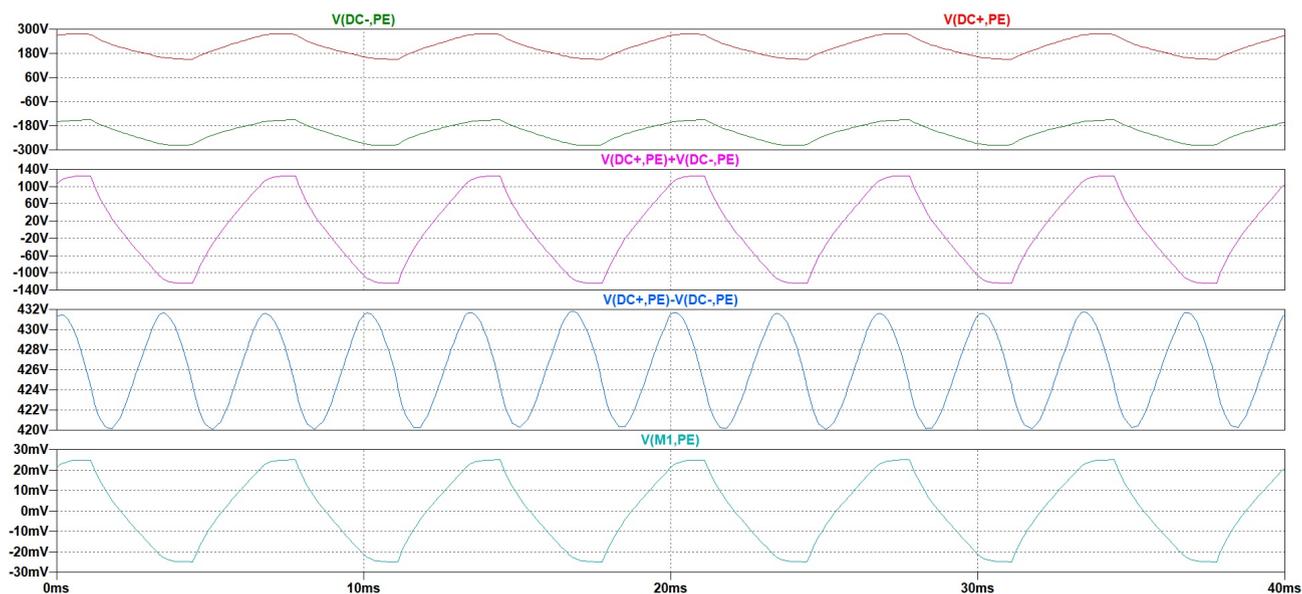


Figure 3.2: Differential and common-mode voltages in the rectifier system

It can be observed in Figure 3.2 that the differential-mode DC-link voltage between points $DC+$ and $DC-$, $V(DC+, PE) - V(DC-, PE)$ (plotted in blue) that appears across the load has the characteristic waveform of a 6-pulse diode rectifier with a 300 Hz ripple. The voltages at points $DC+$ and $DC-$, however, are at positive and negative potential with respect to earth, equal to half of the DC-link voltage on either side of zero. These voltages give rise to the common-mode AC voltage $V(M1, PE)$ with a frequency of 150 Hz at the midpoint of the stacks, $M1$ with respect to earth. This common-mode voltage is directly proportional to $V(DC+, PE) + V(DC-, PE)$ (plotted in magenta) which indicates the following:

$$\begin{aligned}
 V(DC+, PE) + V(DC-, PE) &\rightarrow \text{Common-mode voltage} \\
 V(DC+, PE) - V(DC-, PE) &\rightarrow \text{Differential-mode voltage}
 \end{aligned}$$

Based on this finding, it is inferred that the common-mode voltage, $V(M1, PE)$ originates in the connection between the point M1 and earth (PE). In case this connection is absent, there would only be a differential voltage across the load.

Hence, further focus was placed on finding a suitable DC/DC converter topology and developing a control scheme that would aim at controlling the common-mode voltage and thereby the current which is explained in detail in the following sections.

3.2 Buck Converter as DC/DC Stage

As the simplest step-down DC/DC converter, the Buck converter was implemented as the DC/DC stage to control the voltage and the current seen by the electrolyzer stacks. The simulation model of the system with two electrolyzer stacks is as shown in Figure 3.3.

For a Buck converter, the main control parameter is the duty cycle (D) of the switch ($S1$ in the model). The average output voltage over a full switching period seen by the load is given by $V_{out} = D \cdot V_{DC-Bus}$ which is controlled by varying the duty cycle between 0 and 1.

3.2.1 Simulation Model and Results

As mentioned in Section 2.1.2, when an equipment is earthed, the connection goes through a Residual Current Device (RCD) which detects current on the earth connection and breaks the circuit. In order to avoid tripping of this device in the laboratory, it was decided that the midpoint of the two load resistors will just be connected to the star point or Neutral of the transformer's secondary side. Since the purpose of simulating the system was to aid the hardware implementation, to keep the systems consistent in the simulation model and the laboratory setup, the point $M1$ is connected to the neutral of the transformer's secondary side in Figure 3.3.

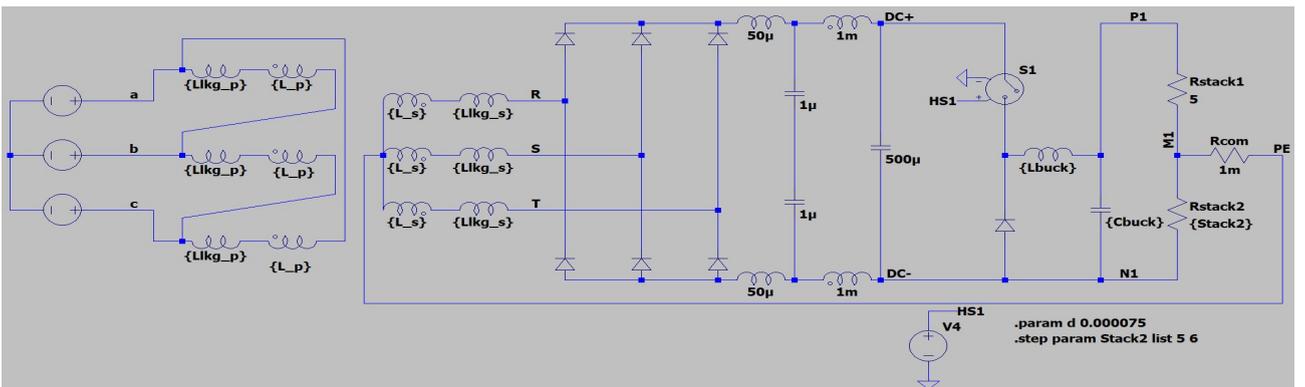


Figure 3.3: Simulation model with Buck converter as DC/DC stage supplying two series-connected electrolyzer stacks

Based on the simulations carried out, it was observed that the Buck converter suffers from a major drawback that the load (in this case, the two in series connected resistances) and the converter itself are referenced to the same point i.e. point $N1$ (which is at the same potential as $DC-$). However, since $DC-$ is always at -270 V with respect to earth, the point $N1$ is also at a lower potential compared to earth. This allows a continuous flow of common-mode current with a DC offset through the ground loop and R_{com} in the model. The non-uniform degradation of the electrolyzer stacks contributes further to this issue since the potential difference of common point $M1$ is a function of the two resistances. This behaviour can be seen through waveforms obtained by simulating the system by stepping R_{stack2} with $5\ \Omega$ and $6\ \Omega$ in Figure 3.4, where the DC offset of the common-mode current reduces with the increase in the resistance of R_{stack2} .

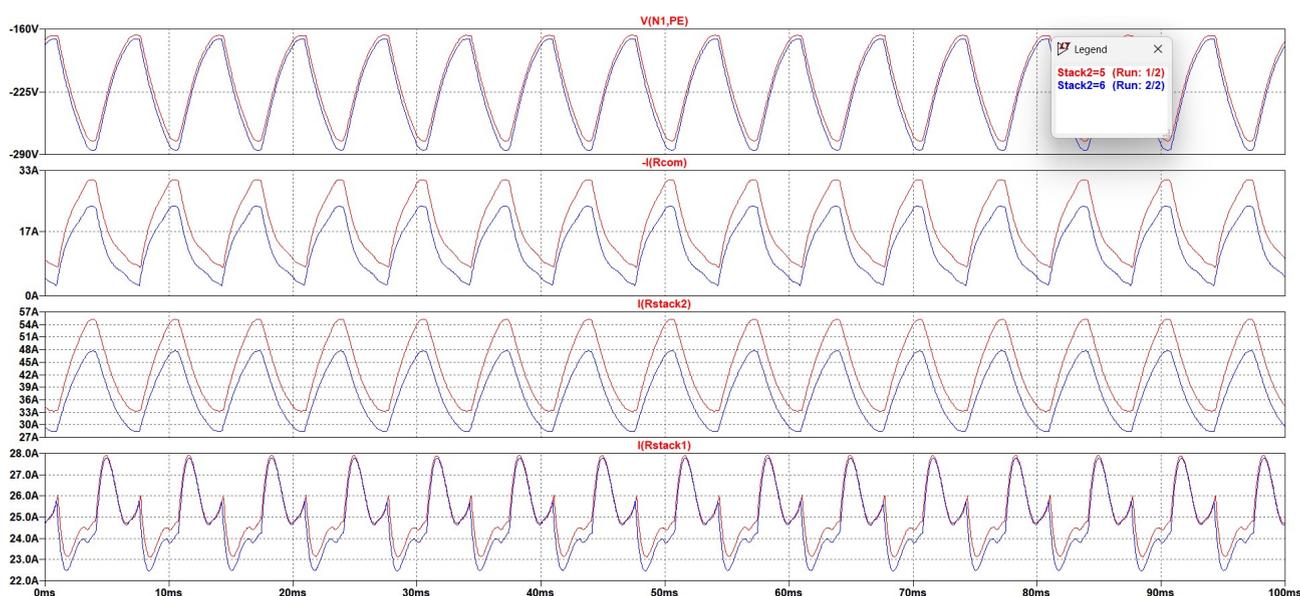


Figure 3.4: Results for single Buck converter system with stepped R_{stack2}

3.2.2 Limitations

Based on the primary reason that the load's reference voltage (point $N1$) with respect to earth cannot be controlled along with above results and observations for single Buck converter system, it could be concluded that the common-mode and circulating currents cannot be avoided using the Buck converter topology for the DC/DC stage.

3.3 Full Bridge Converter as DC/DC Stage

Based on the limitations of the Buck converter, the full bridge topology with four active switches as per Figure 3.5 is considered to be investigated with the electrolyzer stacks connected between the outputs of the two half bridges.

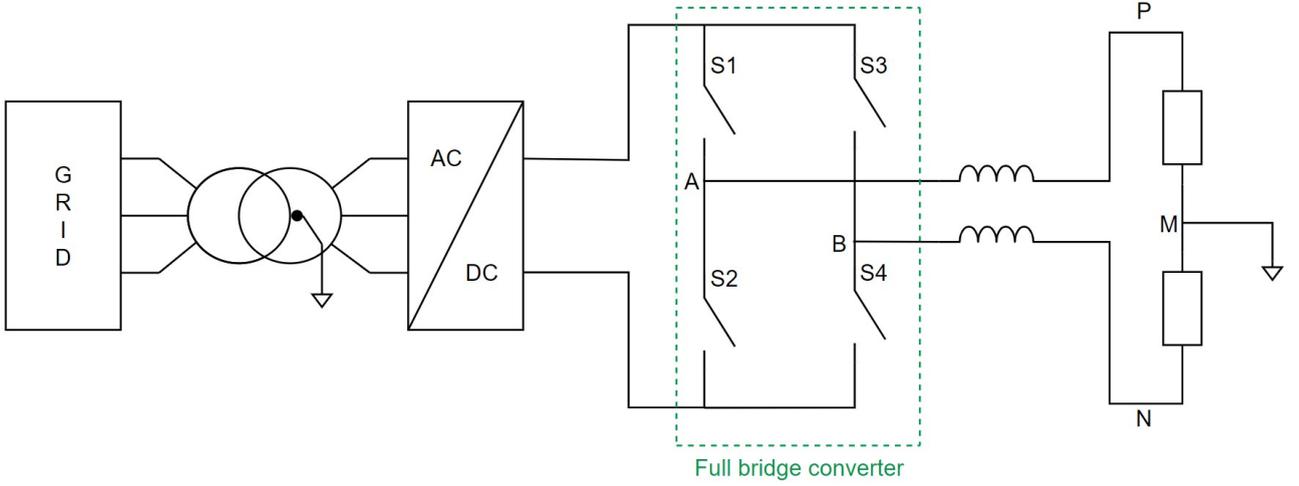


Figure 3.5: Overview of system with Full bridge as DC/DC stage

3.3.1 Operating Principle

The full bridge topology features two half bridges, which are used to provide a controlled differential voltage across the load as shown in Figure 3.5. The potential at P is generated by controlling the duty cycles of switches $S1$ (dA) and $S2$ such that $D_{S2} = 1 - dA$. Similarly, the potential at N is generated by controlling the duty cycles of switches $S3$ (dB) and $S4$ in complementary manner. In this way, the P and N components of the differential load voltage will be aimed to be controlled in such a way that the resultant effect successfully cancels the common-mode voltage at midpoint M . The differential voltage across the load, V_{PN} is given by,

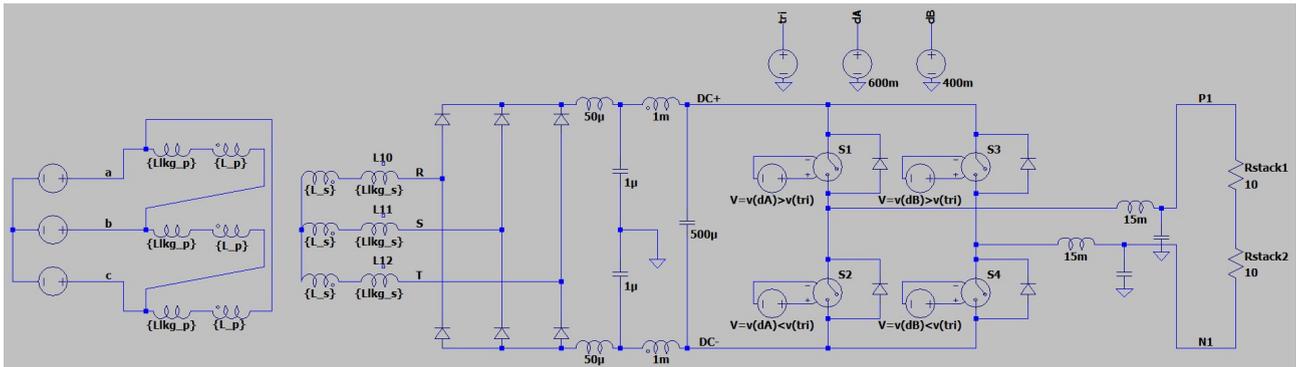
$$V_{PN} = dA \cdot V_{DC-Bus} - dB \cdot V_{DC-Bus} \quad (3.1)$$

where $dA \cdot V_{DC-Bus}$ is the average voltage at point A and $dB \cdot V_{DC-Bus}$ is the average voltage at point B with respect to the negative rail of the DC-Bus.

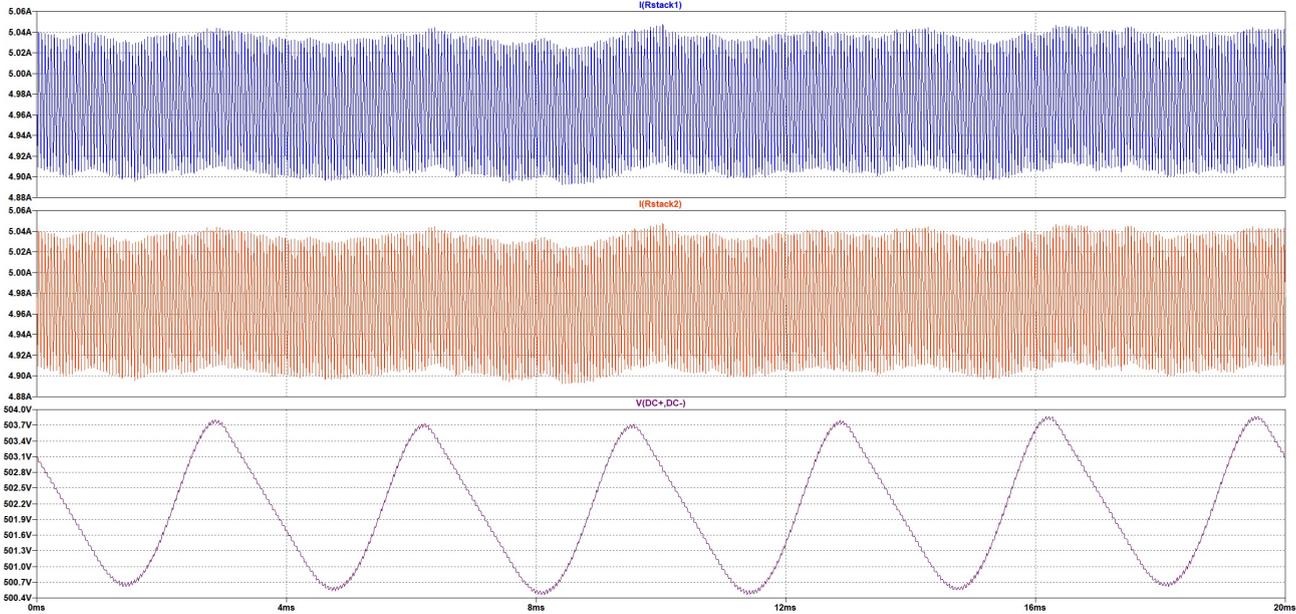
As a first step, simulations were carried out with the midpoint of the resistors not connected to the neutral of the transformer and fixed duty cycles for legs A and B to validate the operation of the full bridge converter. The model and the results are shown in Figure 3.6 and Figure 3.7. The duty cycles for legs A and B , dA and dB , for this simulation were kept to 0.6 and 0.4, respectively as seen in Figure 3.6a. The supply line voltages for the simulation is 400 V. The two resistors in this case were kept set to the same values of 10Ω to have a current of 5 A and it can be observed in Figure 3.6b that the system behaves as a simple DC/DC converter connected to a resistive load since the same current flows through R_{stack1} and R_{stack2} . Equation (3.1) can also be verified through Figure 3.6b as follows:

$$V_{DC-link} = 502 \text{ V}$$

$$I_{Rstack1} = I_{Rstack2} = \frac{0.6 \cdot 502 - 0.4 \cdot 502}{10 + 10} = 5.02 \text{ A}$$



(a) Simulation model



(b) Load currents and DC-link voltage

Figure 3.6: Simulation model and results of full bridge DC/DC converter with midpoint of the load not connected to neutral of the transformer

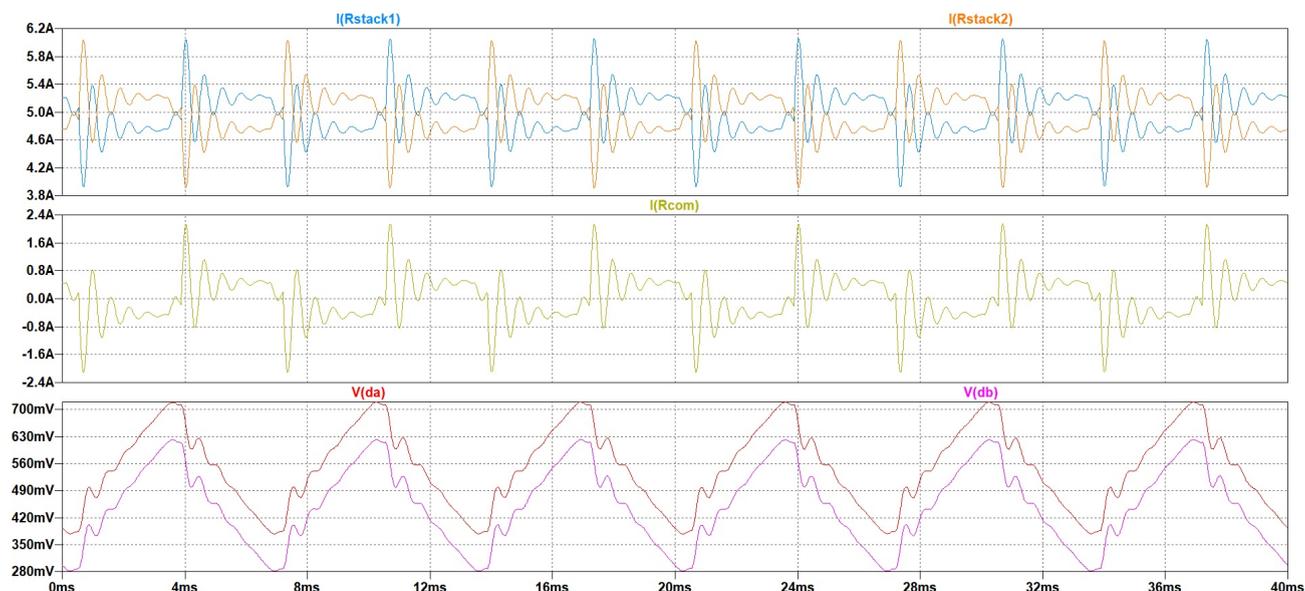


Figure 3.7: AC line currents for model shown in Figure 3.6a

Figure 3.7 shows the line currents for the simulation model. Each half cycle of 50 Hz of the line currents is divided into two pulses due to the presence of leakage inductance on the phases of the transformer, as also explained in [33]. Once the operation of the full bridge DC/DC converter was verified, the midpoint $M1$ was connected to the Neutral of the transformer to verify the common-mode voltage $V(M1, PE)$ shown in Figure 3.9.

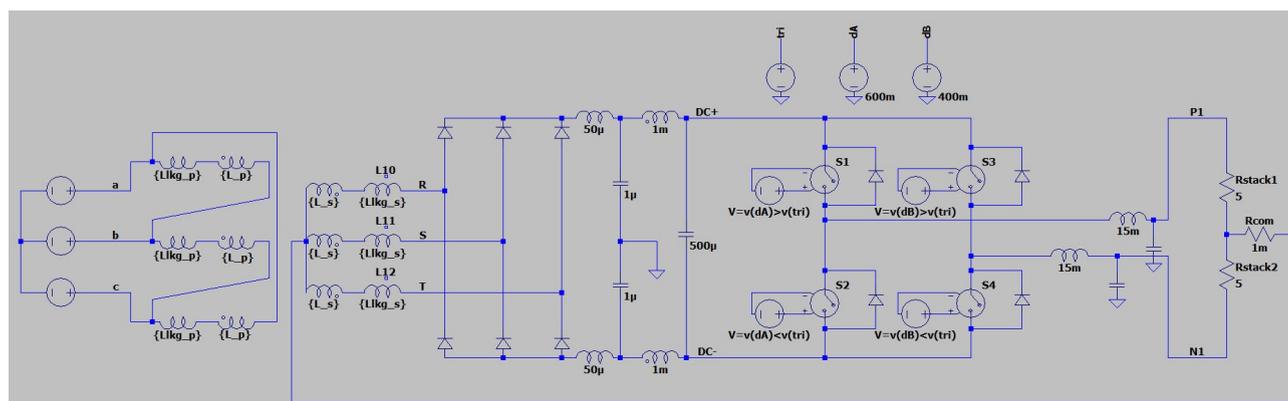
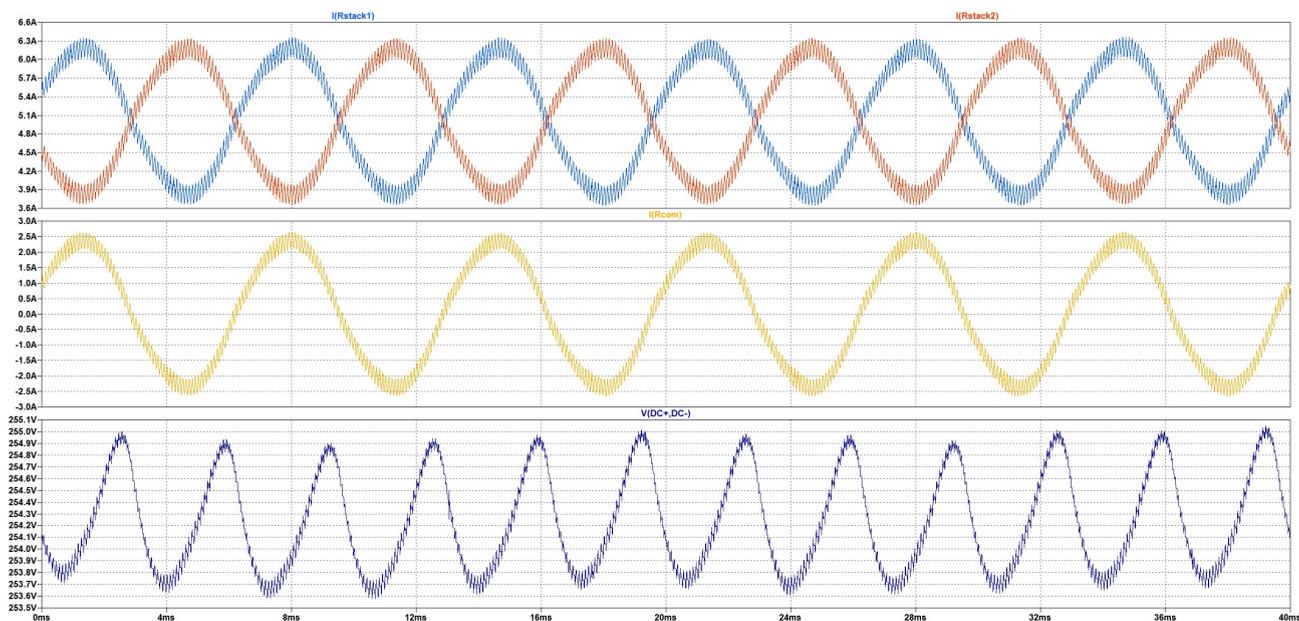
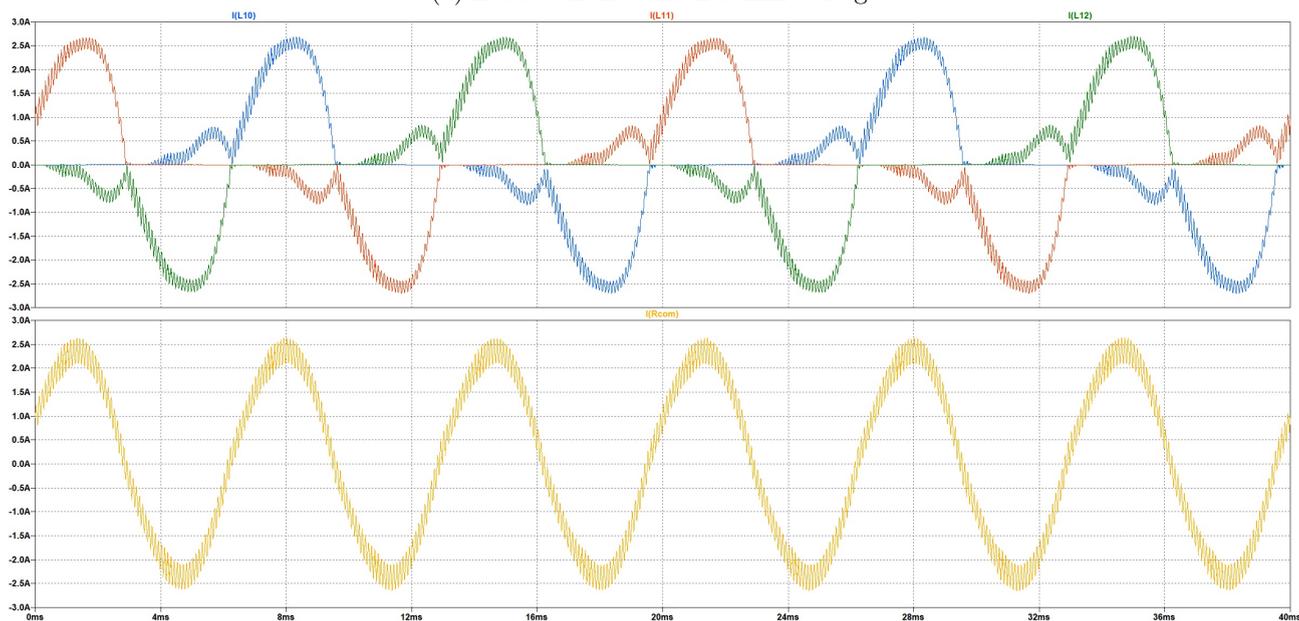


Figure 3.8: Simulation model with $M1$ connected to Neutral



(a) Load currents and DC-link voltage

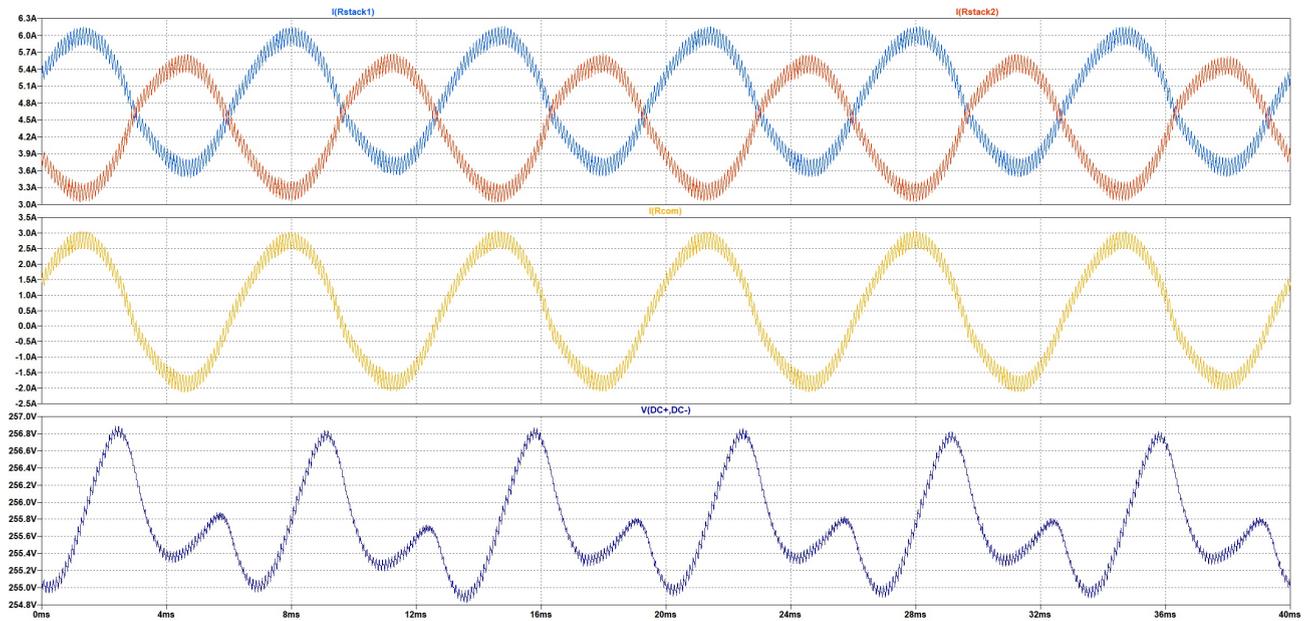


(b) AC line currents and common-mode current

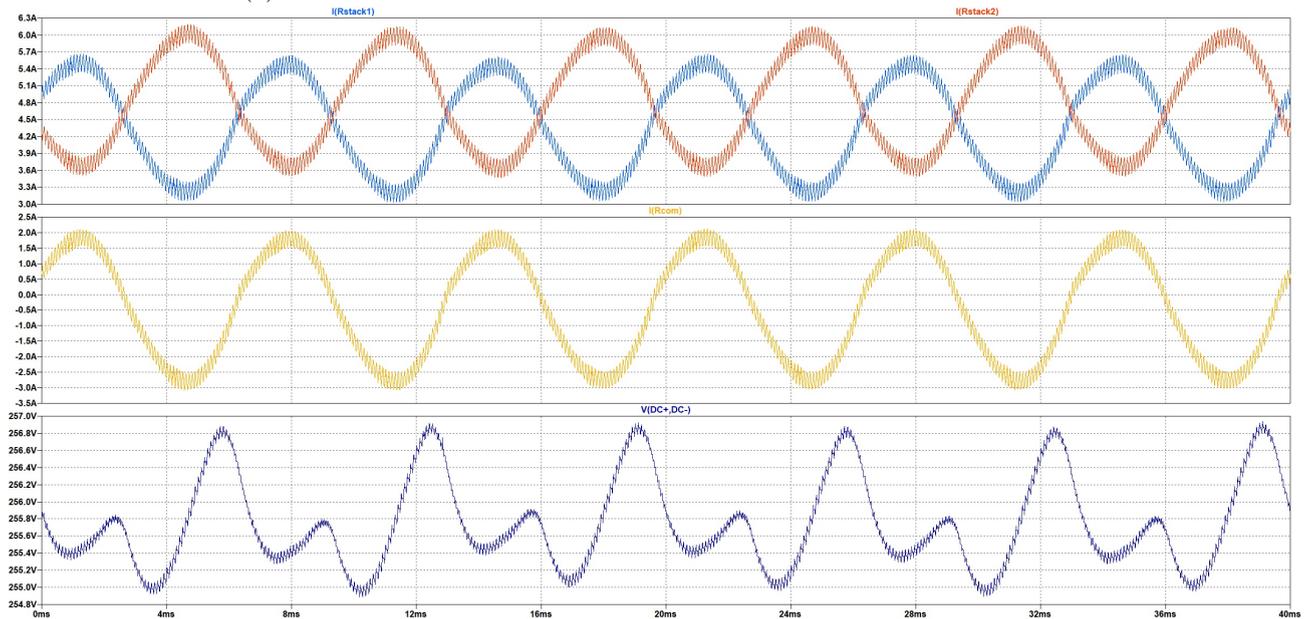
Figure 3.9: Simulation results for model shown in Figure 3.8

Figure 3.9a shows the common-mode current flowing through R_{com} with a frequency of 150 Hz. The flow of the common-mode current also changed the nature of the stack currents and AC line currents. The DC offset of the currents flowing through R_{stack1} and R_{stack2} represents the differential-mode current which is based on the voltage across points $P1$ and $N1$. These are dependent on the duty cycles applied to each half bridge of the DC/DC converter. The AC components of the stack currents which are equal and opposite, as seen in Figure 3.9a, suggest that the common-mode current flows from the rectifier through the positive and negative rails of

the DC-link to point $M1$ through both the resistors. Additionally, in comparison with the results of the Buck converter shown in Figure 3.4, the common-mode current has an average value very close to 0 A which is due to the control of potential at point $N1$. Further, to analyse the effects of unequal resistances on the common-mode and line currents, two simulations were carried out with $R_{stack1} = 5$ and $R_{stack2} = 6$ in the first case and $R_{stack1} = 6$ and $R_{stack2} = 5$ in the second. The results obtained through these simulations are shown in Figure 3.10.



(a) Load currents and common-mode current with $R_{stack1} < R_{stack2}$

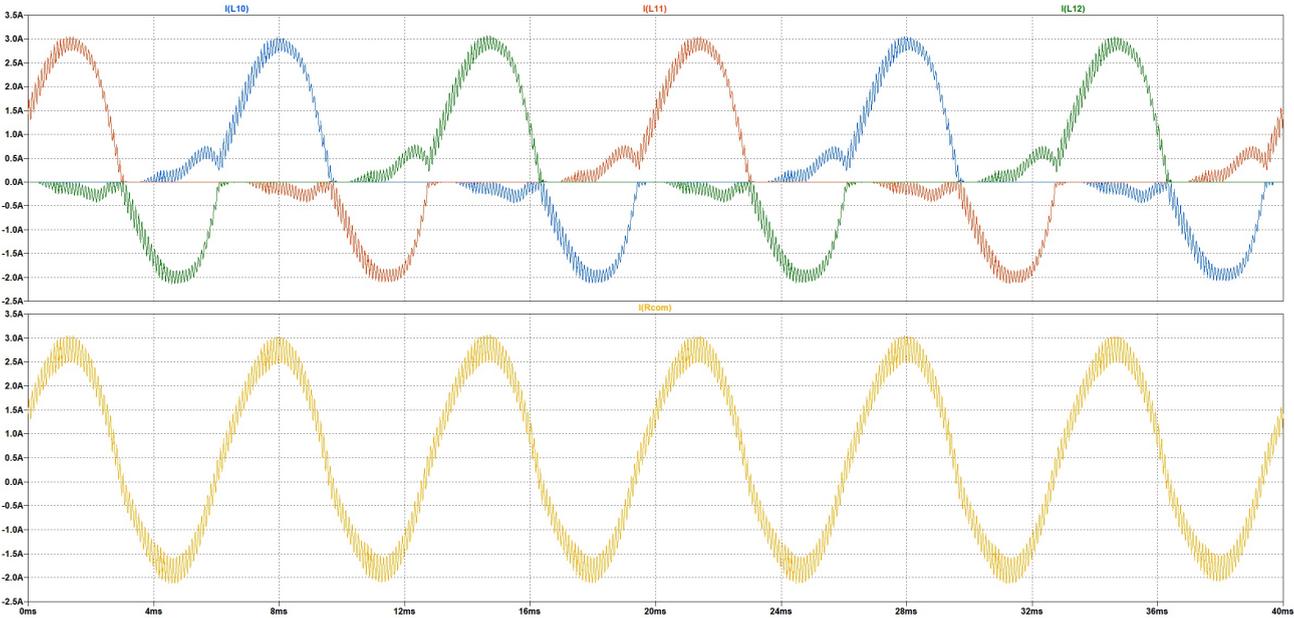


(b) Load currents and common-mode current with $R_{stack1} > R_{stack2}$

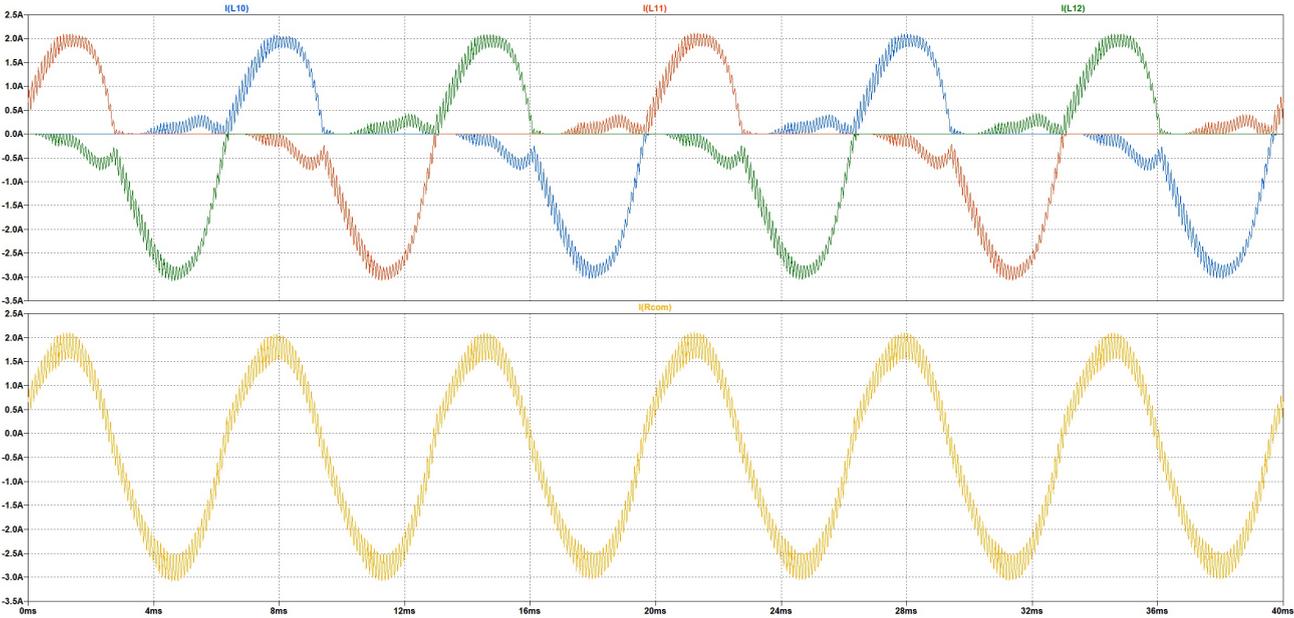
Figure 3.10: Load currents and common-mode current for unequal stack resistances

When the resistances on either side of point $M1$ are unequal, the common-mode current gets a DC average due to the voltage divider formed by the two stack resistors at point $M1$, as explained previously in the Buck converter simulation. This is also reflected by the difference between the DC offsets of the stack currents being equal to the DC offset of the common-mode current through R_{com} .

The DC offset in the common-mode current is also carried into the line currents as shown in Figure 3.11.



(a) AC line currents and common-mode current with $R_{stack1} < R_{stack2}$



(b) AC line currents and common-mode current with $R_{stack1} > R_{stack2}$

Figure 3.11: Line currents for unequal stack resistances

By applying Kirchoff's Voltage Law (KVL) to the branches of Figure 3.12, the below equations are obtained:

$$V_{com} = V_{DC-} - V(P1, DC-) + I_{Rstack1} \cdot R_{stack1} \quad (3.2)$$

$$V_{com} = V_{DC-} - V(N1, DC-) - I_{Rstack2} \cdot R_{stack2} \quad (3.3)$$

Additionally, given the control that is applied on each leg, the following equations stand true as explained in Section 3.3.1:

$$V(P1, DC-) = dA \cdot V(DC+, DC-) \quad (3.4)$$

$$V(N1, DC-) = dB \cdot V(DC+, DC-) \quad (3.5)$$

Two different conditions for dA and dB can be assumed.

$$d_A, d_B = \begin{cases} constant \\ variable \end{cases} \quad (3.6)$$

In the case that both are constant, the currents $I_{Rstack1}$ and $I_{Rstack2}$ have a DC component and an AC component of 150 Hz which due to V_{COM} . Therefore, if the target is to achieve constant currents the control parameters of the two legs dA and dB should not be constant.

By substituting Equation (3.4) and Equation (3.5) into Equation (3.2) and Equation (3.3) the resultant equations are:

$$dA = \frac{V_{DC-} - V_{com} + I_{Rstack1} \cdot R_{stack1}}{V(DC+, DC-)} \quad (3.7)$$

$$dB = \frac{V_{DC-} - V_{com} - I_{Rstack2} \cdot R_{stack2}}{V(DC+, DC-)} \quad (3.8)$$

By forcing the current values to be constants and equal to I_{diff} in Equation (3.7) and Equation (3.8), dA and dB are now varying in accordance to the opposite of V_{COM} which is the only element of these equations with an AC component. Try to interpret the above equations, one would say that the formulated control parameters, dA and dB , that are applied in the two legs of the DC/DC converter, generate the opposite effect of V_{COM} . Specifically, it is generated in such a manner to be present in both legs and cancel the flow of common-mode currents from both R_{stack1} and R_{stack2} .

As these equations for duty cycles are open-loop, they produce the desired differential-mode current, I_{diff} for the specific values of R_{stack1} and R_{stack2} that they are computed for. The challenge, however, was to compute V_{com} correctly. Initially, the equations', Equation (3.7), Equation (3.8), effectiveness is verified by developing a simulation model as per Figure 3.13 based on the average circuit. The computation of V_{com} was developed in the following stages

with the aim of reaching a final stage that could be implemented on hardware in the laboratory setup.

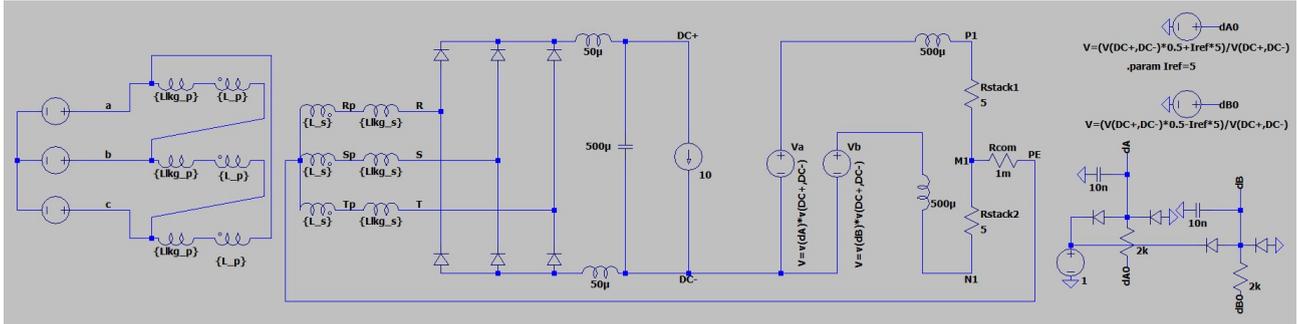


Figure 3.13: Simulation model of average circuit

$$V_{com} = K \cdot V(M1, PE) :$$

As the first option, the voltage across points $M1$ and PE which is the generated common-mode voltage itself, was chosen as the term to be subtracted. However, the voltage represented by the term V_{com} in Equation (3.7) and Equation (3.8) is practically in the mV range and has insignificant magnitude in comparison with the other components that are usually in the range of tens of Volts. Thus, a gain associated with this term would need to be introduced. As such, multiple following options were tested to recreate the most suitable V_{com} . The voltage was applied with different values of gain to observe the effect of increasing magnitude of V_{com} .

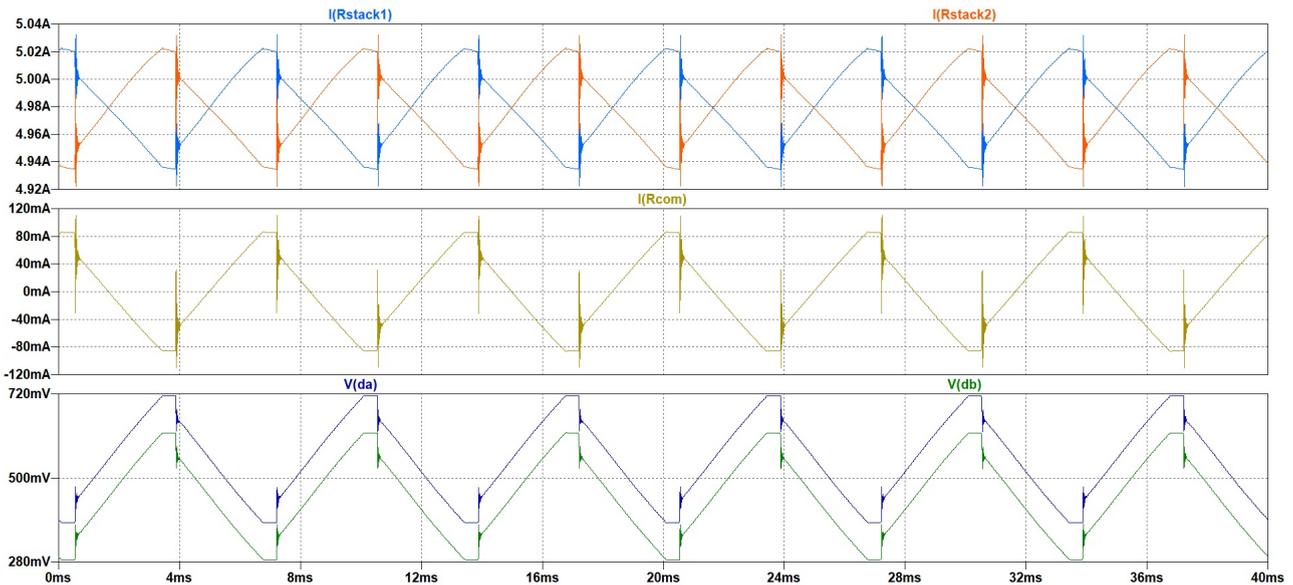


Figure 3.14: Stack currents and duty cycles with $V_{com} = V(M1, PE) * K$; where $K = 10^6$

Figure 3.15 shows that as the gain increases, the amplitude of the common-mode current reduces. The rms values of the current were 3.8 A, 503 mA and 52 mA for increasing values

of K . Although this option works as expected in the simulation environment, it was not a feasible solution to be implemented on hardware since the generated common-mode voltage was of the order of nV which could be difficult to measure and process. Hence, an alternate option, explained further, was sought which was computable through measurement on the lab setup.

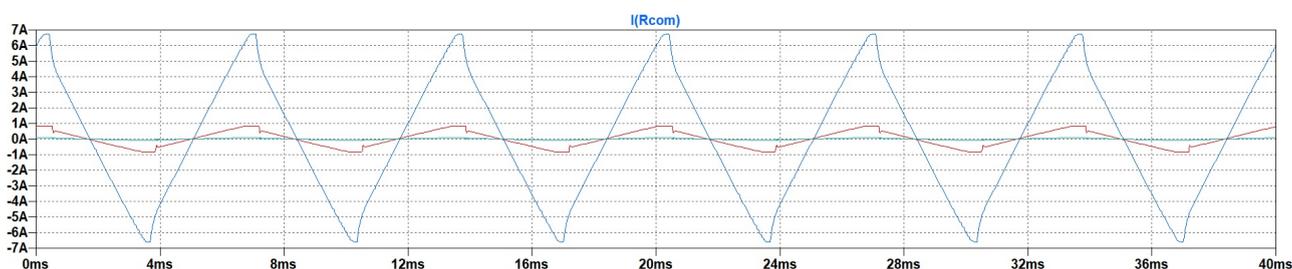


Figure 3.15: Common-mode currents with $V_{com} = V(M1, PE) * K$; where $K = 10^4$ (blue), 10^5 (red) and 10^6 (cyan)

$$V_{com} = K \cdot R_{com} \cdot (I_{Rstack1} - I_{Rstack2}) :$$

As mentioned in the beginning of this chapter, having a closed-loop control of the DC/DC converter for regulation of the stack currents is an objective of the project. Hence, making use of the parallelly measured quantities of the stack currents, $I_{Rstack1}$ and $I_{Rstack2}$, equations for dA and dB were formed where the term for V_{com} was substituted by the difference in these stack currents. The simulation results for the product of $K \cdot R_{com} = 1$ applied to the difference of the stack currents for computing the common-mode voltage are shown in Figure 3.16.

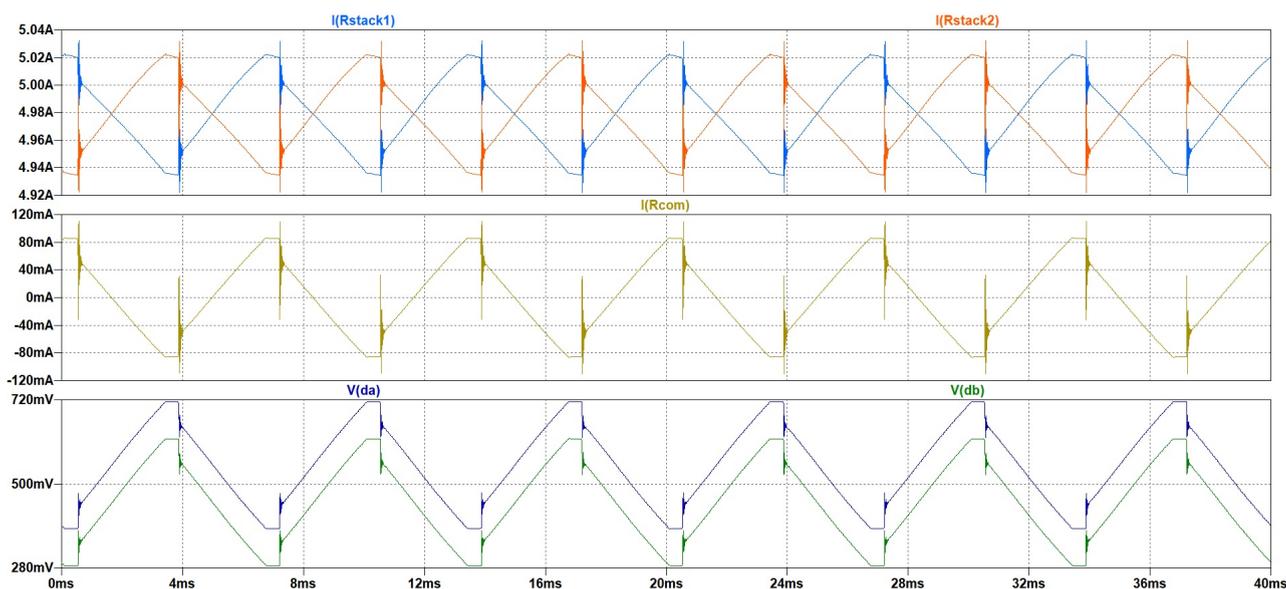


Figure 3.16: Differential-mode, common-mode currents and duty cycles with $V_{com} = K \cdot R_{com} \cdot (I_{Rstack1} - I_{Rstack2})$

The average value of the common-mode current with this gain was 42 nA and the RMS was

52 mA which could further be optimised for the right value of gain for the switching model. The biggest advantage of using the difference of the stack currents for computing the feedforward term for reducing the common-mode voltage was its feasibility of implementation on hardware. Although, prior to that, the equations were applied to the switching model to observe its performance and effects of different values of gain when the feedforward control is used with the high frequency switching component.

3.4.2 Switching Model with Feedforward Control

Due to the ease of development of the control system with simpler functional blocks, the switched model was implemented on PLECS. The transformer was modelled by a three phase voltage source and leakage inductances for simpler and faster implementation. The model implemented on PLECS and its simulation results are shown in Figure 3.17 and Figure 3.18, respectively. This simulation was carried out for a reference differential-mode current of 5 A through the stacks and a product $K \cdot R_{com} = 100$ for the feedforward component. It is important to note the different resistances of R_{stack1} and R_{stack2} and their reflections in the gain blocks applied to the reference current on the control side.

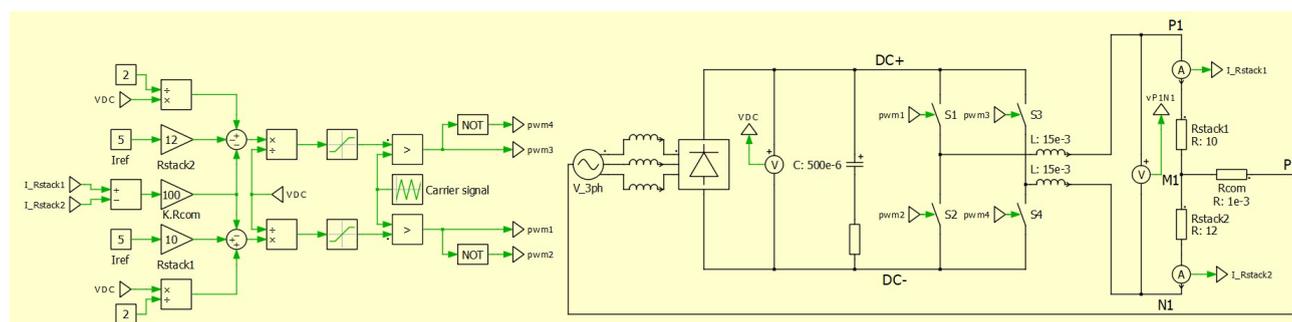


Figure 3.17: PLECS simulation model for switched circuit with open-loop feedforward controller

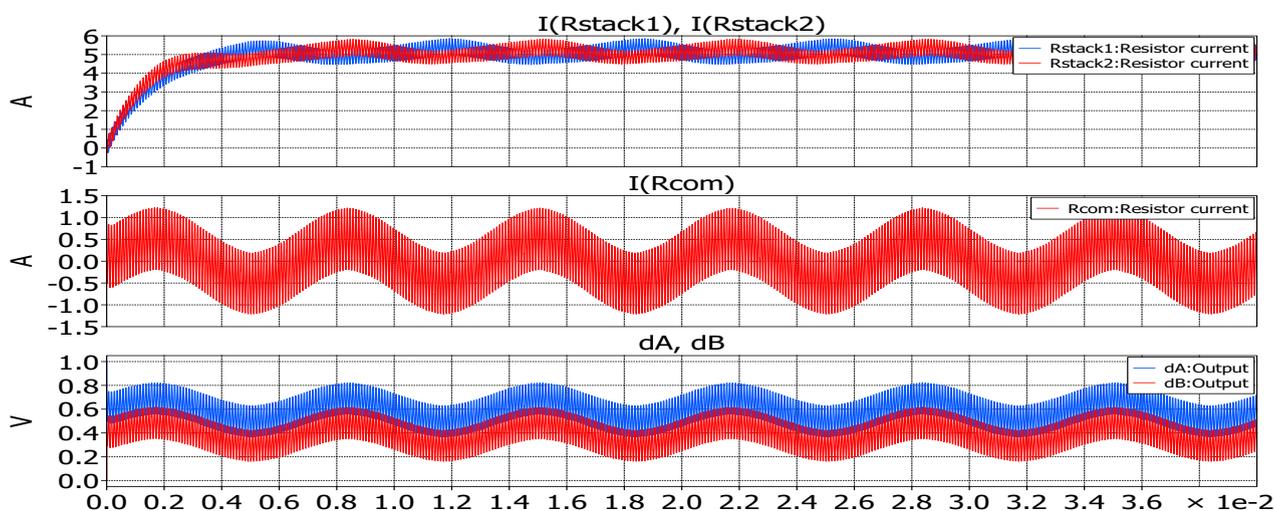
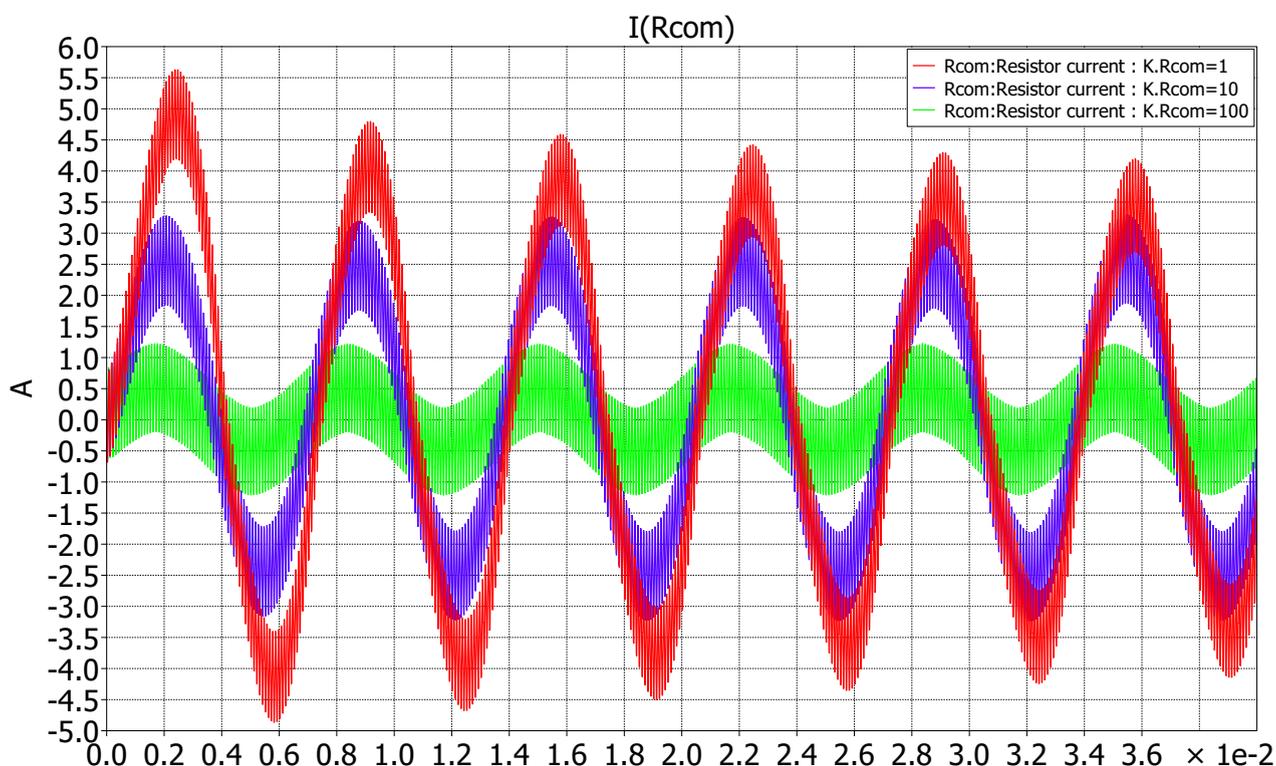


Figure 3.18: Stack currents, common-mode current and duty cycles with open-loop feedforward controller for unequal stack resistances; $K \cdot R_{com} = 100$

Figure 3.19: Common-mode current $I(R_{com})$ for different values of $K \cdot R_{com}$ Table 3.1: Variation of I_{com} rms with product $K \cdot R_{com}$ for feedforward controller

$K \cdot R_{com}$	I_{com} rms
1	2.5 A
10	1.9 A
100	0.58 A

In Figure 3.18, it can be seen that the stack currents reach the target reference current of 5 A despite the different resistances, however with the 150 Hz common-mode current present. The amplitude of the common-mode component varies inversely with the value of $K \cdot R_{com}$ which can be seen in Figure 3.19 and Table 3.1. The Fourier spectrum of I_{com} shown in Figure A.3 confirms that the 150 Hz is the most dominant of the lower order harmonics present. Although the feedforward control approach shows promise for solving the problems highlighted in Chapter 1, it has a few drawbacks for the implemented system. For the simulation model, the system's stability was lost for gain values beyond 250 which could be due to the dominance of the V_{com} component in the equations of the duty cycles. Another drawback of the control system was its inability to maintain the average current flowing through R_{stack1} and R_{stack2} for varying resistances. To regulate this current, it becomes necessary to update the value of the resistances in the control equations governing the duty cycles. Failure to do so results in the average currents through the stacks not being equal to the reference current. This phenomenon can be seen in the Figure A.8. Thus, the feedforward control could address the

issue of controlling the common-mode component but it does not cater to all the requirements of the project. A decision was hence made to assess the performance of the classical PI controller which is a feedback type controller, perfectly suited for situations with dynamically varying system parameters.

3.5 PI Controller

The PI controller was implemented in the simulation model on PLECS which is shown in Figure 3.20. The difference between the reference current of 5 A and the measured currents through R_{stack1} and R_{stack2} are passed through individual PI controllers. Each PI controller independently generates one of the duty cycles, dA and dB which provides a good degree of control for each stack resistor. The PI controller was also implemented for different values of R_{stack1} and R_{stack2} as can be seen in the figure below.

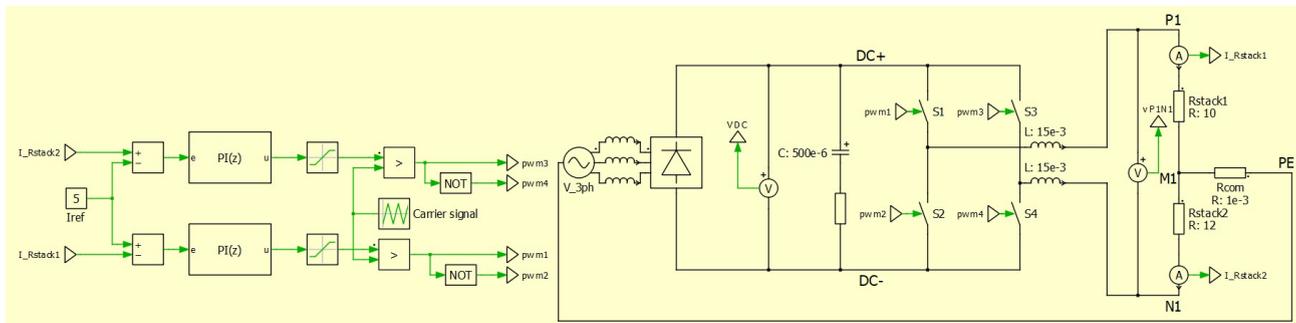


Figure 3.20: Simulation model with PI controller for unequal stack resistances

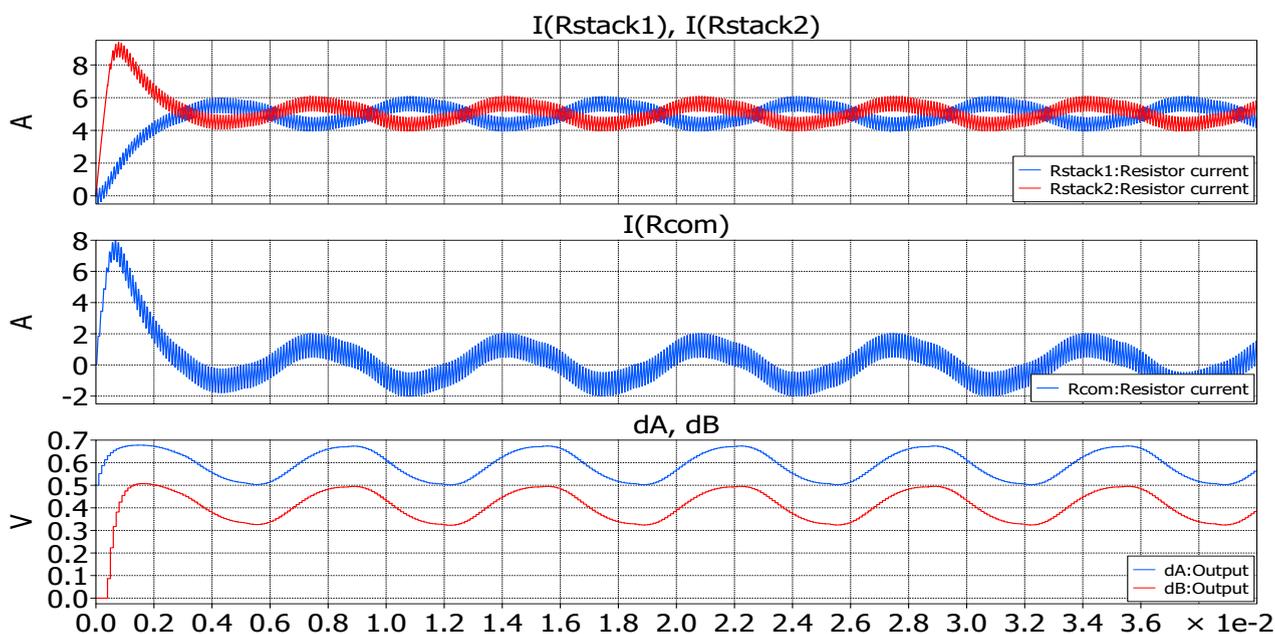


Figure 3.21: Differential-mode, common-mode currents and duty cycles with PI controller for unequal stack resistances; $K_P=0.1$, $K_I=100$

Figure 3.21 shows the stack currents, common-mode currents and duty cycles generated using the PI controller with K_P and K_I values equal to 0.1 and 100, respectively. The average differential-mode current through the stack resistances is equal to the reference current of 5 A and this is obtained without changing any of the parameters of the controller.

Thus, the objective of using the PI controller to respond to the changing values of resistances was met perfectly. However, even though the common-mode current did not possess a DC offset, it still had a considerably large AC rms value of 1 A with the existing values of K_P and K_I . Thus, these values were changed to obtain three different combinations with the aim to observe the trend of change in the common-mode current. These combinations and the resulting rms values of I_{com} are listed in Table 3.2 and shown in Figure 3.22.

Table 3.2: Variation of I_{com} rms with control parameters K_P and K_I for PI controller

K_P	K_I	I_{com} rms
0.1	100	1 A
0.1	1000	0.53 A
0.5	1000	0.52 A

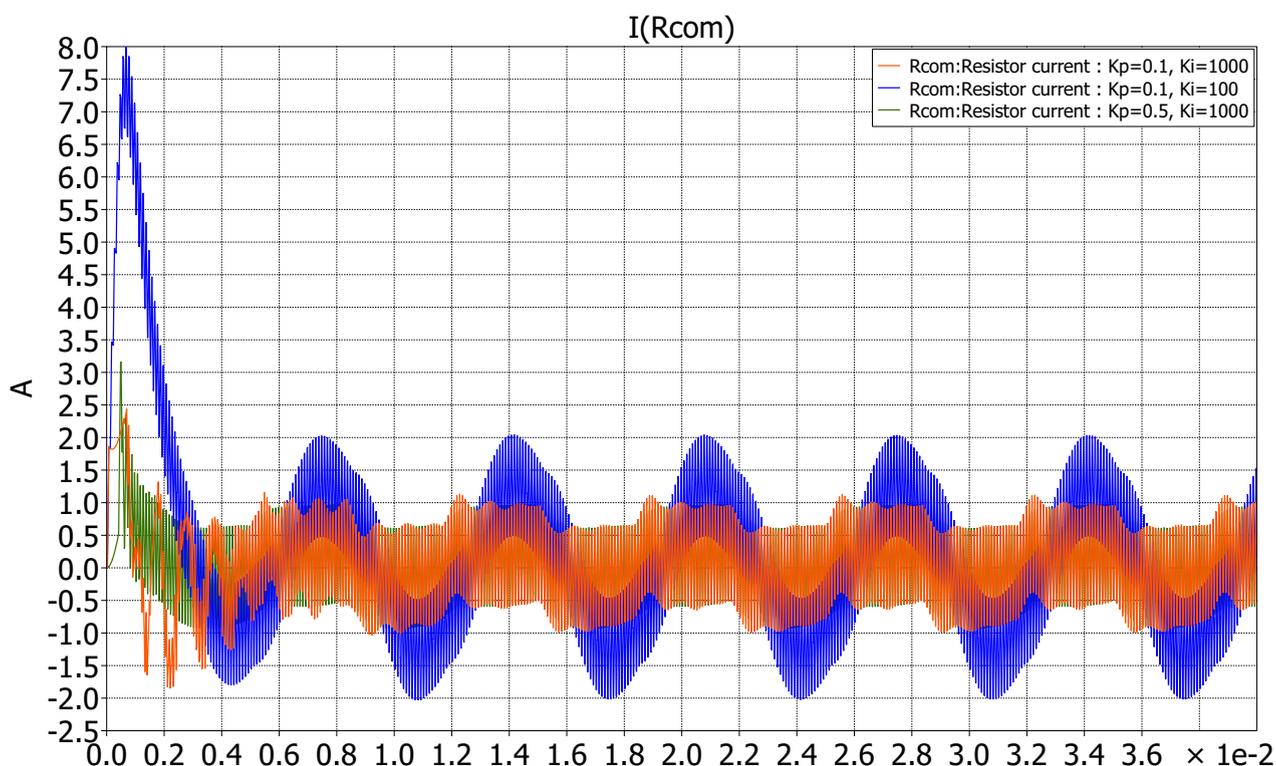


Figure 3.22: Stack currents, common-mode current and duty cycles with open-loop feedforward controller for equal stack resistances

Based on the above observations, it can be said that the values of the control parameters affect the behaviour of the common-mode current flowing through the system. The rms value of I_{com} had a 50% reduction by increasing the K_I by a factor of 10 but with harmonics of multiples of 150 Hz. These components are attenuated to some extent by increasing the K_P by a factor of 5 although the 150 Hz component remained dominant. The comparison of the Fourier analysis for the results with K_P values 0.1 and 0.5 can be seen in Figure A.4. Since an increase in K_P resulted in reduction of the higher order harmonics, a further increase was attempted, although this resulted in the system becoming unstable. On the basis of these preliminary observations, it could be understood that the PI controller can handle changing plant parameters very well and can also affect the common-mode current to some extent. However, as the system aims to have both these requirements met through a single control scheme, PI controller also could not be considered as the solution for the presented problem.

Out of the two investigated control strategies, both show promise with regard to certain aspects of the problems that are addressed in the project. With the feedforward strategy, there is a high degree of reduction in the amplitude and therefore, the rms value of the common-mode current. On the other hand, the PI controller offers the advantage of having control of the differential-mode current in a dynamically varying environment. As a next step, a combination of these controllers was implemented where the PI controller would cater to the regulation of differential-mode component of the stack currents and the feedforward controller would regulate

the common-mode component of the stack currents.

3.6 PI + Feedforward Controller

In this control scheme, the PI controller uses the error in the reference and the measured values of stack currents and generates an output to reduce the error with the reference differential-mode current. On the other hand, the feedforward controller computes the difference between the two stack currents which results in the common-mode current I_{com} . From this output of the PI controller, the output of the feedforward controller multiplied by a product $K \cdot R_{com}$ is subtracted and filtered to generate the duty cycle. Each half bridge has its own controller (PI + feedforward) for better control of the individual stack current. The control block diagram for this is shown in Figure 3.23.

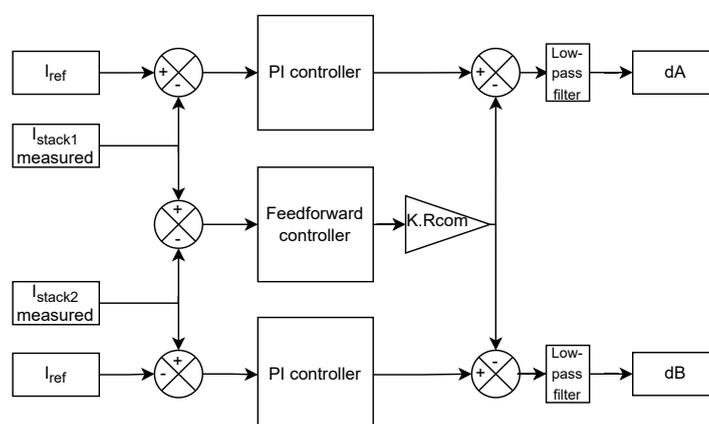


Figure 3.23: Block diagram of PI+feedforward controller

The PI + feedforward controller was implemented on LTspice due to very long simulation times on PLECS and the model is shown in Figure 3.24. Simulations were carried out for different values of the PI controller parameters K_P and K_I which predominantly control the differential-mode component of stack currents. After a few iterations, for the values of 5 and 1 for K_P and K_I respectively, the desired response of the system for controlling the differential-mode current was obtained. Once this was achieved, the value of product $K \cdot R_{com}$ for the feedforward component was varied to reduce the amplitude of the common-mode current, I_{com} .

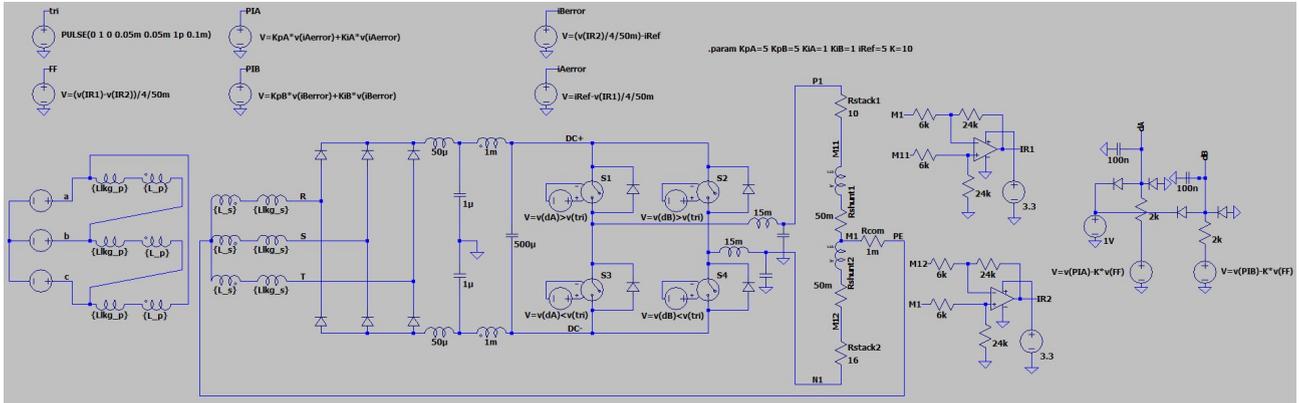


Figure 3.24: Simulation model with PI + Feedforward controller for unequal stack resistances and $K \cdot R_{com} = 10$

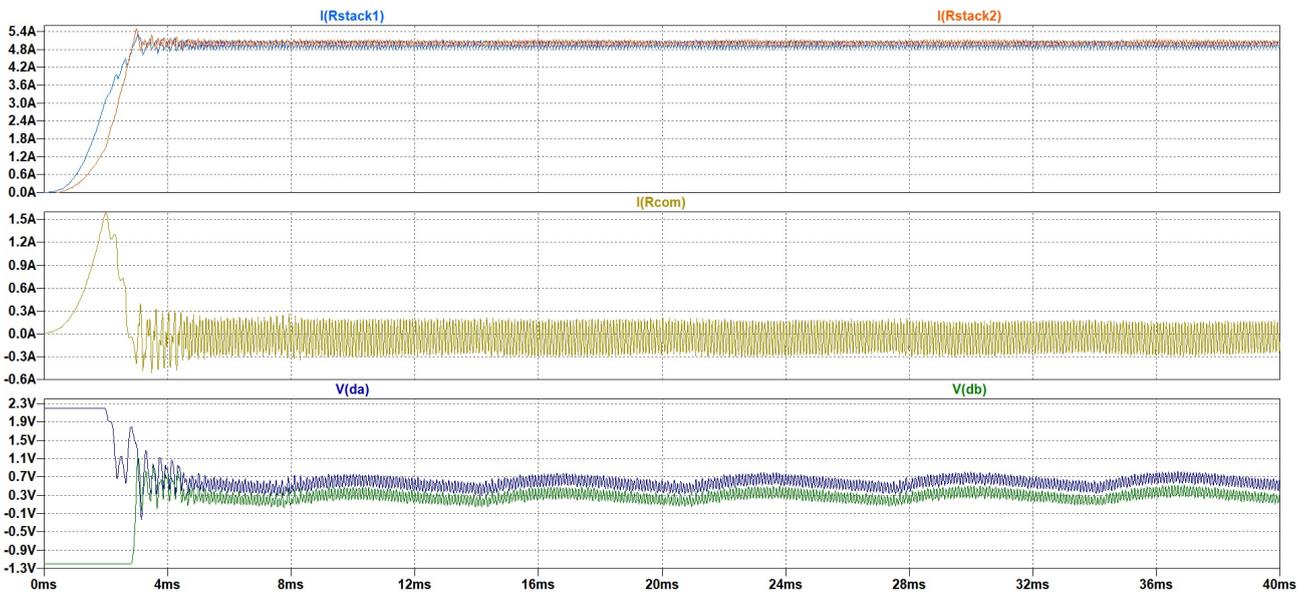


Figure 3.25: Differential-mode, common-mode currents and duty cycles with PI + Feedforward controller for unequal stack resistances and $K \cdot R_{com} = 10$

Table 3.3: Variation of I_{com} rms with feedforward gain $K \cdot R_{com}$ for PI + Feedforward controller

$K \cdot R_{com}$	I_{com} rms
1	0.3 A
5	0.16 A
10	0.11 A

The results of the simulation with $K \cdot R_{com}$ set to 5 are shown in Figure 3.25. It can be seen that the stack currents quickly settle to the desired value of 5 A due to the PI controller. The common-mode current is observed to be mainly having only the switching frequency component

and no 150 Hz component is present. The Fourier spectrum of I_{com} can be found in Figure A.5. For fixed values of K_P and K_I , the variation of $K \cdot R_{com}$ and its effects can be seen in Table 3.3. Due to time constraints, the controller could not be further optimised, however, on the basis of these values, it can be considered that the PI + feedforward controller might be successfully able to address the challenges of controlling the differential-mode as well as common-mode current in the given system. These simulation cases were then applied to the hardware setup developed parallelly in the laboratory and the observations and findings from the lab are explained in the next chapter.

Chapter 4

Implementation and Results

This chapter presents the hardware setup and its features that were developed as part of this thesis. The steps that were followed towards debugging the auxiliary board and validating the operation of the measurement circuits and safety functions are also explained in this chapter. Finally, with consistency to the simulation cases of Chapter 3, the conducted measurements are presented to establish the validity of the control's approach and the inconsistencies are discussed. During this process, difficulties were encountered and solutions were required to operate the system.

4.1 Implemented Setup

The hardware setup implemented in the laboratory is as shown in Figure 4.1. The figure highlights the auto-transformer which is used to vary the input line voltage to the isolation transformer and is rated for 7kV A. The isolation transformer has been explained in detail in Section 2.2.1 and is functionally used for isolation from the grid and to provide the PE connection for the midpoint of the resistors. As mentioned previously in Section 3.2.1, the PE connection is implemented locally which is referenced to the Neutral (N) of the isolation transformer.

Highlighted in red is the protective cabinet made up of wooden and acrylic sheets. This cabinet provides the necessary protection to the operators of the setup and access to see and work on the hardware enclosed within it. Housed within the cabinet are the Auxiliary Board, the EVAL Board, the load inductors and the measurement probes. The Auxiliary Board is a PCB that was made to contain all the control system elements as one solution. The EVAL Board is the power stage of the implemented setup consisting of the AC/DC rectifier and the DC/DC converter and has been explained in Section 2.2.2. It takes the 3-phase AC input from the isolation transformer and provides controlled DC power the load resistors. The switched DC voltage from the EVAL Board is filtered by the inductors which are placed in series between the output of the EVAL Board and the resistors. Each inductor has a value of 15 mH. The resistors $R1$ and $R2$ are used to represent the electrolyzer stacks as explained previously and their midpoint is connected to the Neutral terminal of the isolation transformer.

The measurement of all the voltage points was carried out using differential voltage probes P5200 from Tektronix which can measure differential-mode voltages up to 1300 V and common-mode voltages up to ± 1000 V. For measurement of common-mode and resistor currents, the current probes TCP0030 and TCP202 from Tektronix were utilised. These current probes have a bandwidth of 120 MHz and can measure currents up to 30 A in positive and negative directions. All the measurements were observed on two different digital oscilloscopes - Tektronix

DPO2014 and KEYSIGHT DSOX1204G having bandwidth of 100 MHz and 70 MHz respectively. The input AC line voltage from the auto-transformer and the total DC voltage across the resistors were monitored using digital multimeters shown in Figure 4.1.

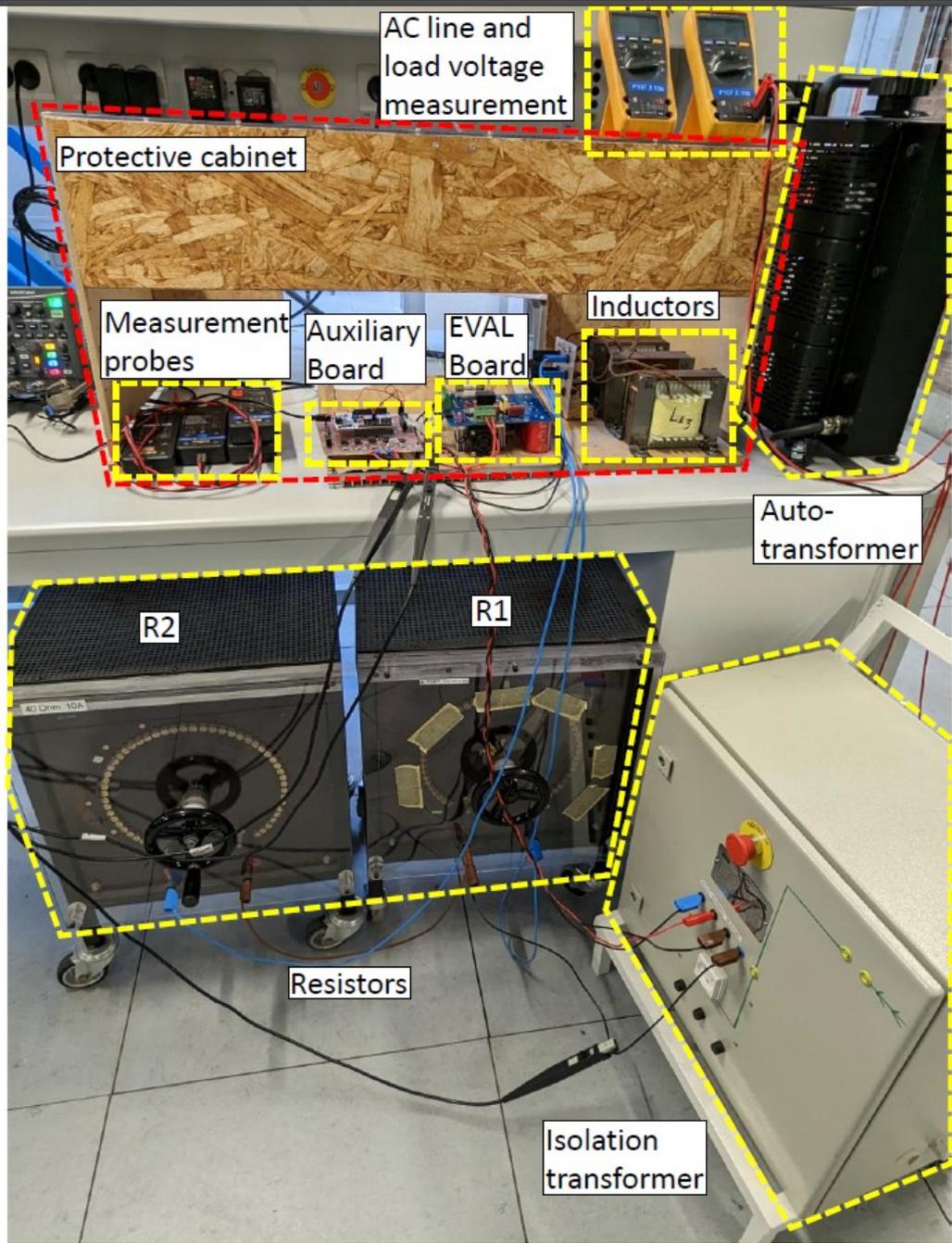


Figure 4.1: Laboratory setup

4.2 Auxiliary Board

In Section 4.1 was highlighted the auxiliary PCB that was designed to accommodate all the functions that were not included in the evaluation board EVAL-M1-IM828-A. It is a two-layer board that was designed using the software Altium Designer and fabricated locally in the university using the student's laboratory PCB Computerised Numerical Control (CNC) machine. Its top layer can be seen in Figure 4.2 with highlighted the areas of interest.

The STM32 micro-controller (6) is connected via two connectors on the auxiliary board. The connectors (2,3) enable the interface between the micro-controller and the power stage board. They include pins dedicated for the PWM signals, the DC-link voltage and DC-link current measurement signals, two power level buses and the ground. There are two such connectors in order to permit the operation of two parallel systems as per Figure 1.7. Similarly to the EVAL-M1-IM828-A all the auxiliary board's functions are referenced to the DC-link negative rail. On the auxiliary PCB are placed all the load current measurement circuits (1). They are five in total, two per system plus a reserve one and each consists of a SMD current transducer, two filtering capacitors, a differential amplifier circuit with SMD resistors and an operational amplifier. For the case of the bottom current measurement circuit, the current enters the board through the ring terminals C9 of Figure 4.2 and then flows through the LEM current transducer U6 before exiting the board from the ring terminal C10. This current measurement topology is further explained in Section 4.4.

As per the auxiliary board power supply, it was mentioned previously that two power levels and a ground are provided to the auxiliary board through EVAL-M1-IM828-A. One is at 3.3 V and is meant to power the micro-controller and the current transducers. The other is at 15 V and with the help of the DC/DC converter (4) it is stepped down to 5 V to supply the operational amplifiers. The STM32-NUCLEO board has two different possible ways to be supplied. The first is at 5 V through the USB connector of the host computer and the second via an external source at 3.3 V or 5 V or 7 V-12 V. However, when the DSP board is supplied externally, the USB can be used for communication, programming and debugging only when it is supplied by 5 V or 7 V-12 V. To this, the NUCLEO board is supplied at 5 V by the linear voltage regulator indicated as (5) in Figure 4.2.

4.3 Protection Circuit

As mentioned in Section 2.2.2, the evaluation board integrates a topology that measures the DC-link current on the negative rail of the DC-Bus as shown in Figure 2.8.

The output signal of this circuit is directed to an ADC port of the micro-controller. There it is converted to its real current value based on Equation (4.1) and by using a conditional statement it is compared with the maximum permitted value. In case it exceeds the maximum allowed value, the PWM generation is programmed to stop. As there are two $10\text{ m}\Omega$ resistors in parallel, the value of shunt resistor R_{Shunt} in Equation (4.1) is $5\text{ m}\Omega$. The parameter V_{offset} holds a value of 0.6 V while the gain G is 13.26 .

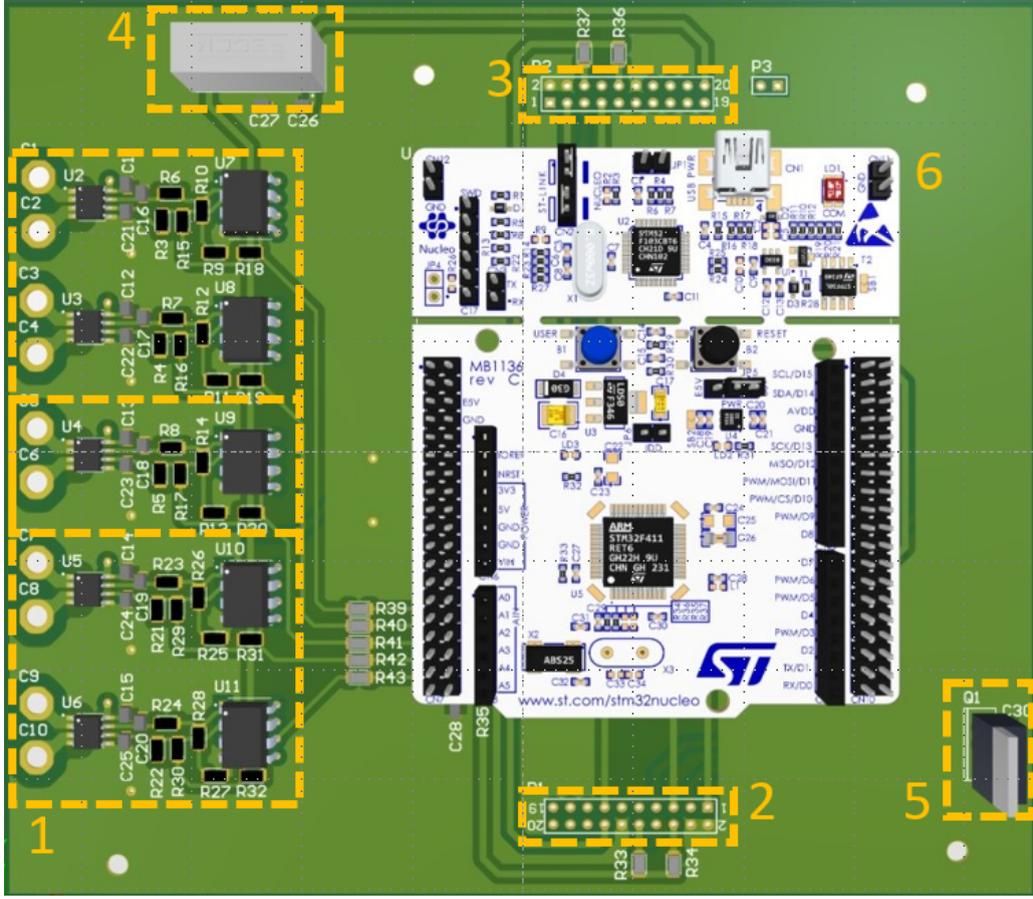


Figure 4.2: Auxiliary board's top layer. Different implemented circuits and components are highlighted.

$$I_{load} = (V_{ADC} - V_{offset}) \cdot \frac{1}{G} \cdot \frac{1}{R_{Shunt}} \quad (4.1)$$

As the safety function is a priority, it is the first to be tested in the system. While in fixed duty cycle conditions, the current flows through the negative rail of the DC bus when the switches S1 and S4 of Figure 3.5 conduct. In Figure 4.3a can be seen the PWM signals that are applied on S1 and S4 while in Figure 4.3b can be seen the equivalent current signal that is sensed by the ADC of the micro-controller as retrieved by the oscilloscope. In the time intervals that both switches are ON, the output of the dedicated current sensing amplifier is having an approximate value of 5 A. The offset that appears in the protection current signal can be attributed to the oscilloscope channel's own offset. The large spikes on the signal appear exactly in the moments of the switching events and they are followed by an oscillation period. These oscillations when captured by the ADC they are able to trigger the system's shut-down function even if the current flowing in the negative DC-rail has not reached its critical value. The red color signal of Figure 4.3b shows the duration of the total ADC conversion that occurs during the interrupt in the micro-controller. It can be seen that the protection current can be captured only once per switching period. In total, for the case of the fixed duty cycle conditions, the function of

the topology is considered acceptable.

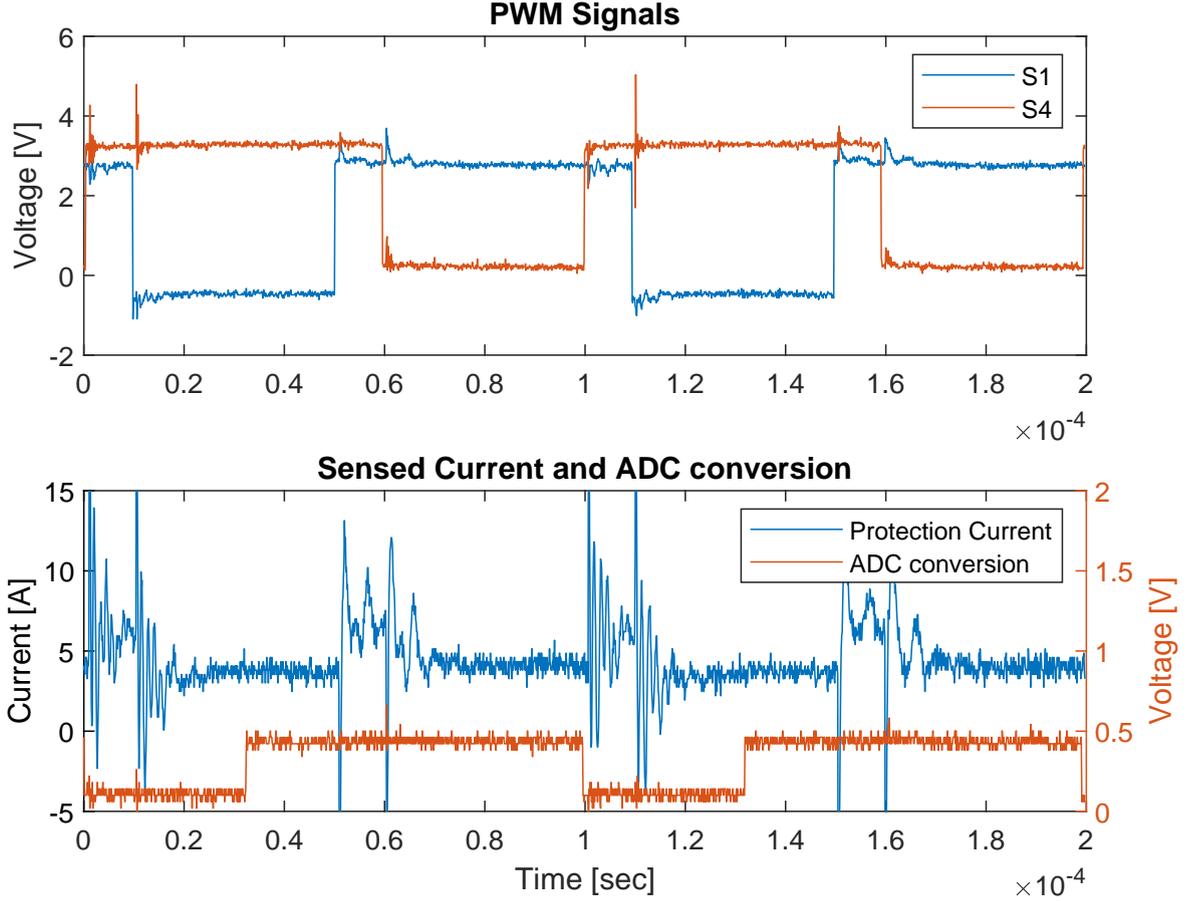


Figure 4.3: (a) PWM signals of S1 and S4 (b) DC-link current measurement on EVAL-board

4.4 Current Measurement

The topology that is incorporated on the auxiliary board for the current measurements is shown in Figure 4.4. The incorporated current transducer is the product GO 10-SME/SP3 from LEM and it operates based on the Hall Effect. It has a current measuring range from -25 A to 25 A and a sensitivity of 50 mV/A , [29]. Its output voltage is referenced to the potential V_{Ref} . The differential signal $V_{out} - V_{Ref}$, contains the information of the current value and is given as an input to a differential amplifier circuit. Based on the superposition theorem, the transfer function of the differential amplifier topology is given by Equation (4.2). To reach a high CMRR, according to [34], the impedances of the two branches of the differential amplifier need to be matched as good as possible and therefore $R_a = R_b$ and $R_c = R_d$.

$$V_{ADC} = \frac{R_c}{R_a} \cdot (V_{out} - V_{ref}) = G \cdot (V_{out} - V_{ref}) \quad (4.2)$$

$$R_a = R_b = 10 \text{ k}\Omega \quad R_c = R_d = 44 \text{ k}\Omega$$

As the output of this differential amplifier is fed to the ADC of the micro-controller that has a range of 0 V to 3.3 V the gain of this circuit needs to be selected accordingly. By selecting the previous values of the resistors, a gain, G , of 4.4 is applied to the output of the current sensor. Given that, the range of 0 A to 15 A should be measured.

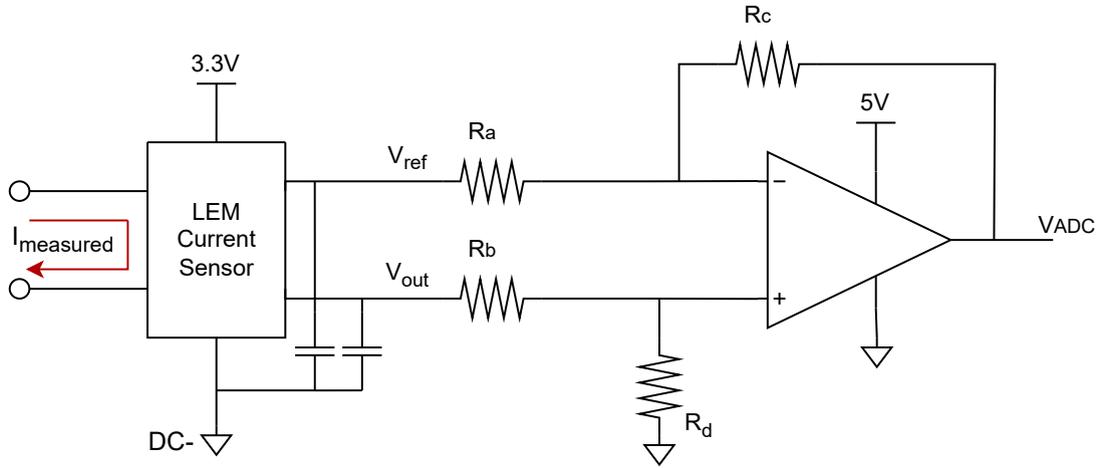


Figure 4.4: Load current measurement topology

During the debugging process, an offset of 760 mV, V_{offset} was observed on the output signal V_{ADC} of the differential amplifier under zero current. This offset voltage corresponds to an offset current, I_{offset} of 3.45 A. Additionally, under zero current, the signal $V_{out} - V_{ref}$ has a negative value of almost -130 mV. As long as the input of the op-amp is negative, its output V_{ADC} remains clamped at the offset of 760 mV. Although it was not possible to track the origins of the -130 mV, it was observed that its value decreases as the current increases by a rate of 50 mV/A (sensor sensitivity). Once the signal $V_{out} - V_{ref}$ that is applied on the input of the op-amp becomes positive, V_{ADC} starts changing properly. That means that the measuring topology of Figure 4.4 is not capable of sensing currents below 2.6 A. Although this is not the desired performance it was considered acceptable due to the fact that the operating currents in the rest of the experiments exceed 2.6 A. In total, knowing the voltage V_{ADC} of Figure 4.4 the current through the load resistors can be estimated in the micro-controller based on the Equation (4.3).

$$I_{load} = (V_{ADC} - V_{offset}) \cdot \frac{1}{G} \cdot \frac{1}{50 \text{ mV/A}} + I_{offset} \quad (4.3)$$

4.5 Measurements

The measurements carried out in the lab are based on the sequence introduced in Chapter 3 to have consistency between the simulation cases and laboratory experiments. After one particular experiment which is later explained in Section 4.5.3 and shown in Figure 4.10, a suspicion arose about the legitimacy of the measurement of the common-mode current, I_{COM} . This suspicion was further amplified by observing all the other measurements that had already been carried out for the hardware setup and presented ahead in this section. To confirm this error in measurement, a DC test was carried out using three probes previously measuring I_{R1} (with Probe 1), I_{R2} (with Probe 2) and I_{COM} (with Probe 3). During the test, at 0 A, the oscilloscope channels measuring through the probes had the following offsets:

Probe 1: -140 mA, Probe 2: -190 mA and Probe 3: 139 mA.

Figure A.7 shows the measurement for a test current of 2 A. Table 4.1 shows the results of the DC test after subtracting the offsets and presents the error. The error was calculated as follows:

$$Error = \frac{(I_{Probe1} + I_{Probe2})/2}{I_{Probe3}}$$

Test current	I_{Probe1}	I_{Probe2}	I_{Probe3}	Error
0.5 A	0.458 A	0.462 A	0.311 A	1.47
1 A	0.9 A	0.886 A	0.601 A	1.48
1.5 A	1.35 A	1.37 A	0.961 A	1.43
2 A	1.88 A	1.91 A	1.28 A	1.47

Table 4.1: Results of DC test carried out for confirmation of measurement error for I_{COM}

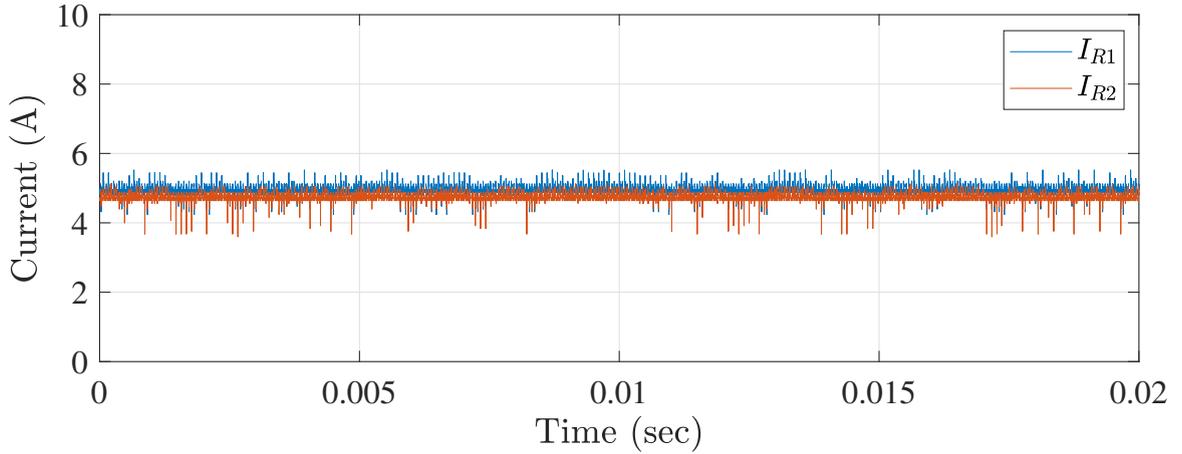
As can be seen in the table, a gain of $1/1.46$ is present on every measurement done by Probe 3. Hence, the results presented further in this section with respect to I_{COM} are reduced by a factor of 1.46. Therefore, the results pertaining to I_{COM} are not compared based on their absolute values with those obtained in the simulations. Instead, they are compared relatively with other measurement results and the trends have been highlighted further.

4.5.1 Open-loop Measurements

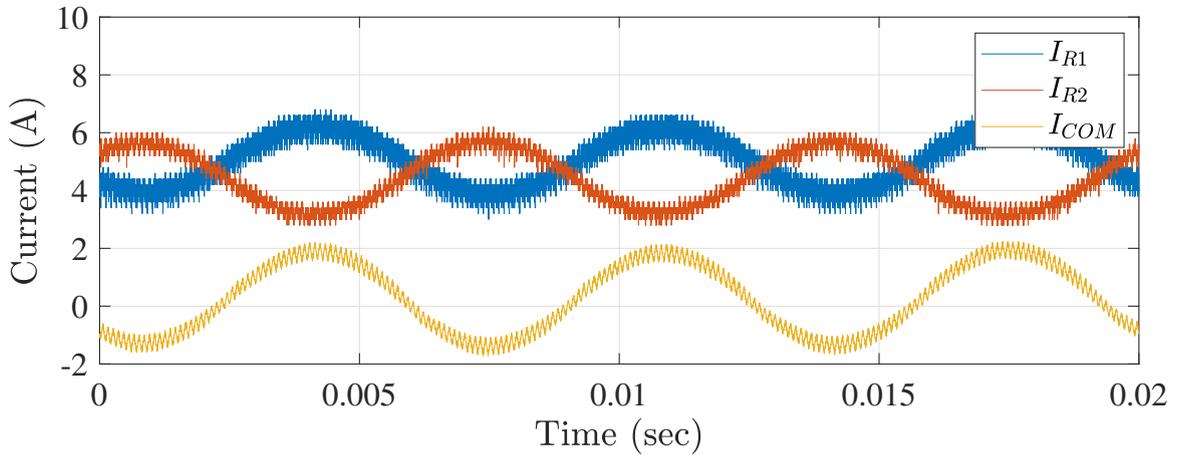
Before implementing any type of control, the system is operated at open-loop conditions. The purpose of these measurements is to prove the operation of the converter and to prove the alignment of the measurement results with the simulations in a safer environment. Therefore, the duty cycles are set at 60% and 40% respectively with a dead time of 500 ns as firstly used in Section 3.3.1.

As mentioned in Section 3.2.1 to avoid triggering the laboratory's safety sensors by forcing current flow through the earth system, the transformer's neutral point is connected to the

midpoint of the load resistors. This way, the common-mode current can be also measured permitting a better interpretation of the data. By doing so and by keeping the resistors to a value of $5\ \Omega$ each, the load currents I_{R1} , I_{R2} and the common-mode current I_{COM} were measured and are presented in Figure 4.5b. This measurement was executed by increasing the input AC voltage up to the point that the $V_{P,N}$ voltage reached 50 V. By comparing it with Figure 4.5a, can be noticed the expected 150 Hz frequency due to the introduced common-mode path. The selected 10 kHz switching frequency is superimposed on all the signals. The 10 kHz ripple is close to 0.5 A peak-peak. In Figure 4.5b, the average value of both load currents is expected to be 5 A. However it is 5.058 A and 4.418 A and 0.276 A for I_{R1} , I_{R2} and I_{COM} respectively. This difference is partly attributed to the different offsets that different channels of the oscilloscope might experience. This offset is revealed in the difference of I_{R1} and I_{R2} when the midpoint is not connected to the neutral which is 220 mA. The above results are gathered in table Table 4.3. Additionally, due to the low precision of the load resistors and small differences in the DC link voltage, the final value of the currents might slightly vary leading to a small DC component in I_{COM} .



(a)



(b)

Figure 4.5: Load currents I_{R1} , I_{R2} and common-mode current I_{COM} with load resistors at $R_1 = R_2 = 5\ \Omega$ for the cases of (a) Midpoint M1 floating, (b) Midpoint M1 connected to transformer's neutral

Table 4.2: Average currents corresponding to the data of Figure 4.5b

	$R_1 = R_2 = 5 \Omega$		
	I_{R1}	I_{R2}	I_{Rcom}
Average Current	5.058 A	4.418 A	0.276 A

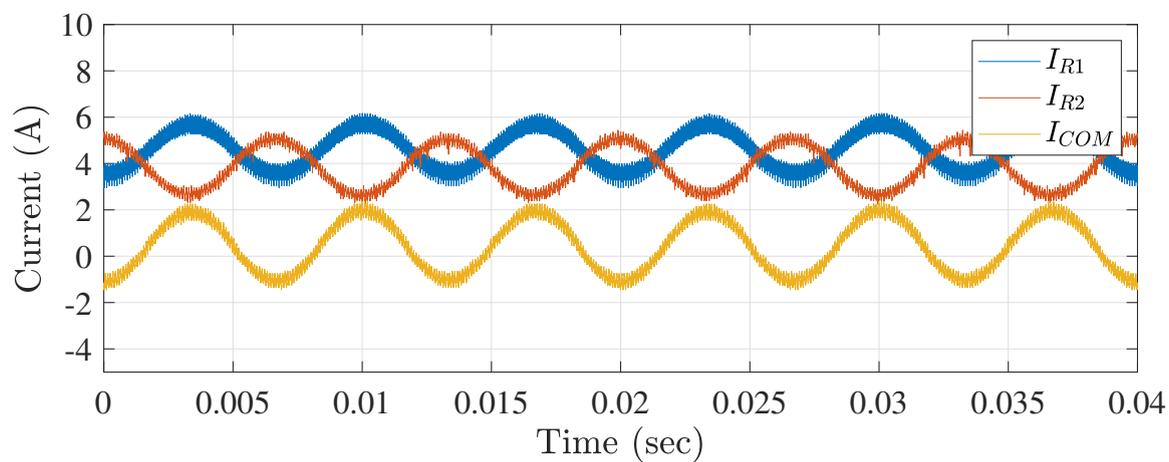
As a next step, the load imbalance is introduced. The resistors are changed to the following values and the same measurements are repeated.

$$(a) \quad R_1 = 5 \Omega \quad R_2 = 5.9 \Omega$$

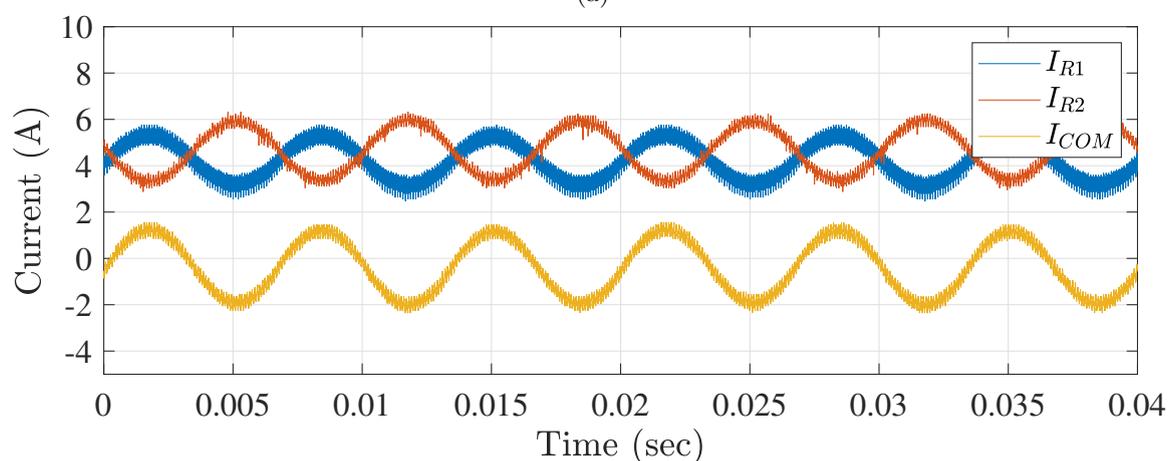
$$(b) \quad R_1 = 6 \Omega \quad R_2 = 5 \Omega$$

It can be seen in Table 4.3 that although the 150 Hz component is maintained the average values of the measured currents are different. This behavior is one of the main problems that is tried to be addressed in this thesis and it can be explained by the equivalent average circuit Figure 3.12. Specifically, when $R_1 > R_2$ the average current flowing through R_1 is smaller than that of R_2 . The opposite occurs when $R_1 < R_2$. As expected a positive or negative offset, depending on the ratio of R_1/R_2 appears on the common mode current I_{COM} as seen in Table 4.3.

The effects of the asymmetry of the load resistors are mirrored in the three-phase currents flowing through the secondary of the transformer as shown in Figure 4.7. The transformer currents are measured and depicted for three different cases. In the first case, Figure 4.7a, the load midpoint is not connected to the neutral of the transformer. The discontinuity of the line currents due to the leakage inductance is also visible. Based on the simulation results of Figure 3.7 there is an inconsistency as per the nature of the line currents. While in simulation results the two pulses are of the same amplitude, the measured currents have a smaller and a larger peak. In general though, the measured and simulated values are close to each other. This inconsistency is though not present in the case of Figure 4.7b where the load resistors have the same value and the midpoint is connected to the transformer's neutral. Similarly, the results of Figure 4.7c are similar to the simulated ones. It should be mentioned that while in Figure 4.7a for each positive current there is a negative current that corresponds to the return path, in the cases of Figure 4.7b and Figure 4.7c that is no longer the case. Instead the return path for these cases is through the transformer neutral-load midpoint connection.



(a)

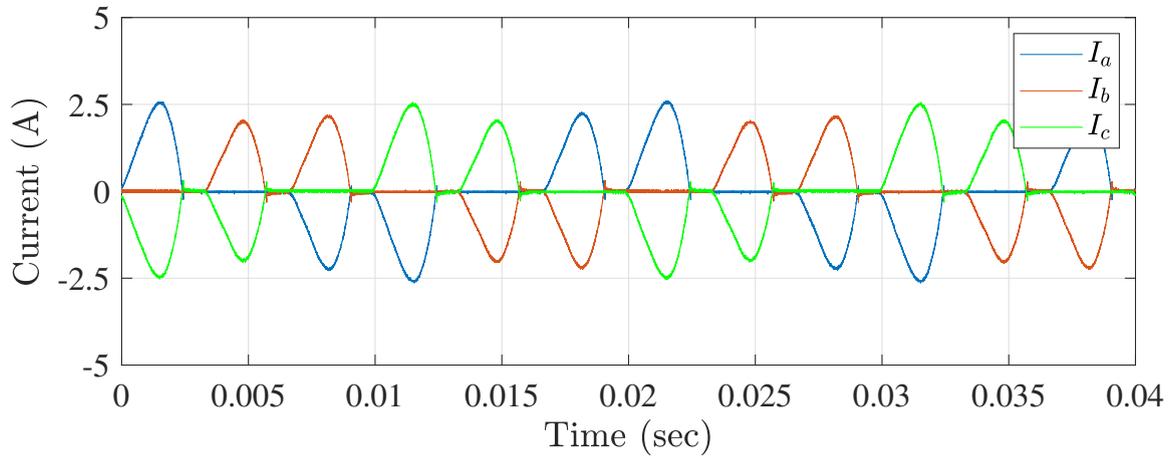


(b)

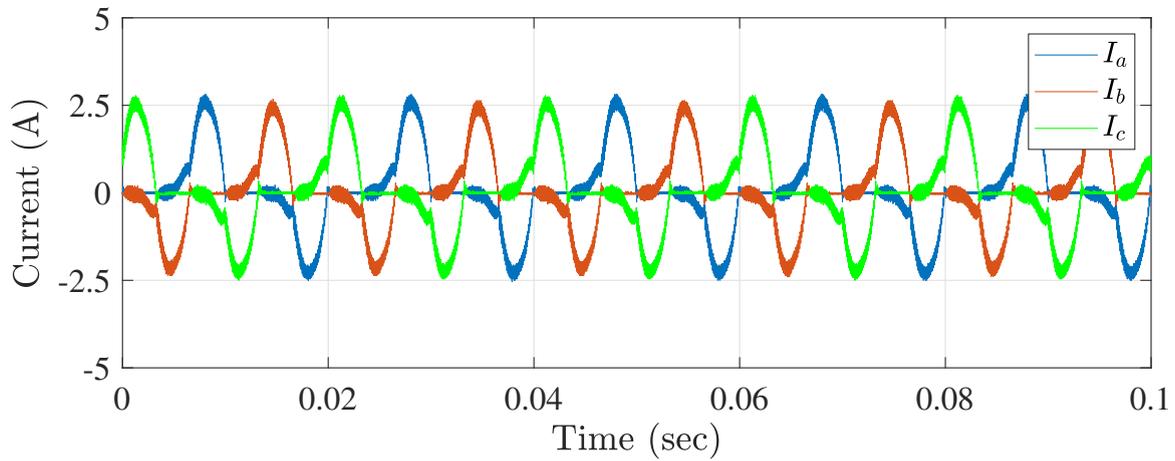
Figure 4.6: Load currents I_{R1} , I_{R2} and I_{COM} for two cases of unequal load resistors (a) $R_1 = 5 \Omega$ and $R_2 = 6.1 \Omega$, (b) $R_1 = 6.1 \Omega$ and $R_2 = 5 \Omega$

Table 4.3: Average currents corresponding to the data of Figure 4.6b

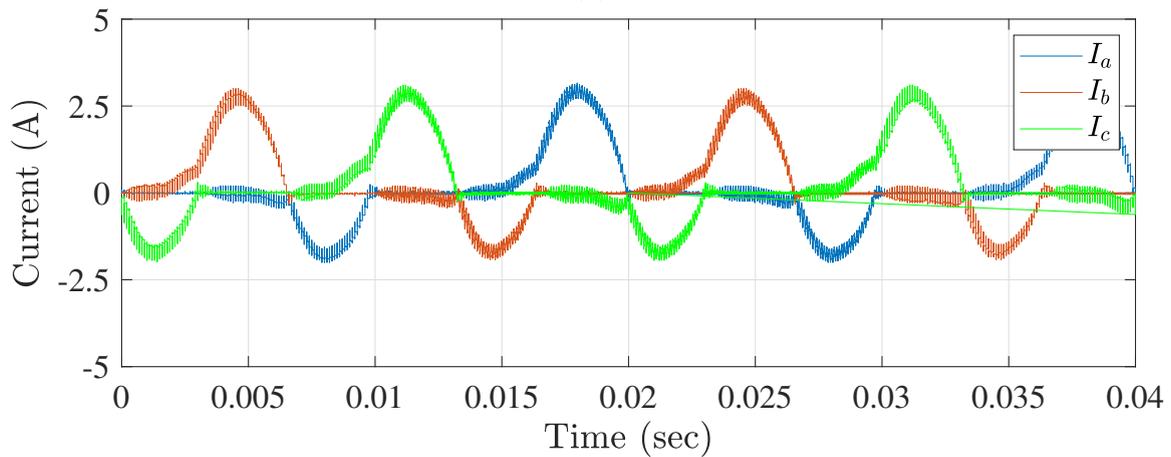
	$R_1 = 6.1 \Omega$ and $R_2 = 5 \Omega$			$R_1 = 5 \Omega$ and $R_2 = 6.1 \Omega$		
	I_{R1}	I_{R2}	I_{Rcom}	I_{R1}	I_{R2}	I_{Rcom}
Average Current	4.317 A	4.661 A	-0.377 A	4.710 A	3.853 A	0.439 A
RMS Current	-	-	1.205 A	-	-	1.177 A



(a)



(b)



(c)

Figure 4.7: (a) The three line currents when the load midpoint (M1) is floating and $R_1 = R_2$, (b) The three line currents when the load midpoint (M1) is connected to the transformer's neutral and $R_1 = R_2$, $I_{COM-mean} = 0.125$ A (c) The three line currents when the load midpoint (M1) is connected to the transformer's neutral and $R_1 \neq R_2$, $I_{COM-mean} = 0.416$ A

4.5.2 Feed Forward Control

In the previous section, the proper operation of the system has been established. Having identified the presence of the 150 Hz and the inequality of the load currents for different load resistors as the main problems to be addressed, in the following measurements are presented the results of the feed-forward control.

These results are divided in two parts of three measurements each. In the first part the load resistors are equal while in the second they are not. For all the measurements, the software is programmed based on Equation (3.7) and Equation (3.8) that were extracted from the average model to determine the duty cycles for the two legs. The DC-link voltage is measured by the voltage divider topology described in Section 2.2.2.2. The V_{DC-} variable is equal to half of the DC-link voltage and the resistor values are inserted in the code as selected in the hardware setup. At this point, it should be mentioned that the resolution of the ADC measurement that corresponds to the DC-link voltage is incapable of tracking its 300 Hz component. As current parameters, I_{R1} , I_{R2} are given in the code the desired output current values. Having obtained through the ADC the two load currents, I_{R1} and I_{R2} , the common-mode voltage in both equations is estimated as:

$$k \cdot V_{COM} = k \cdot R_{COM} \cdot (I_{R1} - I_{R2})$$

where R_{COM} as per Figure 3.17 represents the equivalent resistance of the connection to the neutral of the transformer and the midpoint of the loads. The factor k is amplifying the effect of V_{COM} in the equations. In each part of the results, three different products $k \cdot R_{COM}$ (1, 10, 100) are applied and the currents I_{R1} , I_{R2} and I_{COM} are measured. The AC input voltage is now set to its highest value 380 V line-line and the current reference is set to 5 A. The resistors for the two cases are:

$$(a) \quad R_1 = 10 \Omega \quad R_2 = 10 \Omega \quad \& \quad (b) \quad R_1 = 10 \Omega \quad R_2 = 12 \Omega$$

The retrieved waveforms of the first case can be seen in Figure 4.8 while the ones of the second case can be seen in Figure 4.9. At the same time the average and RMS values of these waveforms are gathered in the tables Table 4.6 and Table 4.5. In both cases by controlling the product $k \cdot R_{COM}$ it can be seen that the ripple of 150 Hz is reduced. This is visible in the reducing trend of the RMS value of I_{RCOM} in the aforementioned tables. Specifically, by changing the product $k \cdot R_{COM}$ from 1 to 100 the RMS value of I_{RCOM} is reduced from 1.385 A to 0.437 A. Although a direct comparison of the simulation results with the measured results for the I_{COM} would not be sensible, the trend is similar which consists a promising behavior that should be further explored. In the case that $R_1 \neq R_2$, the average currents that flow through the load resistors, I_{R1} and I_{R2} are closer to each other than in the case of the open loop control as seen in Table 4.3. By employing a DAC port of the micro-controller it was attempted to measure the duty cycle signal of the first leg of the converter for reasons of comparison with Figure 3.18. Although the measured waveform, Figure A.6, was similar to the simulated there is high noise content. Therefore this type of control not only presents promising results towards reducing the current ripple but is also maintaining the load currents close to the desired values. However,

when the load resistors change, due to possible degradation effects, a sophisticated feature that can estimate this change is needed in order to update the duty cycles. This is something that is not manageable in this setup and therefore the PI control is proposed.

Table 4.4: Average currents corresponding to the data of Figure 4.8

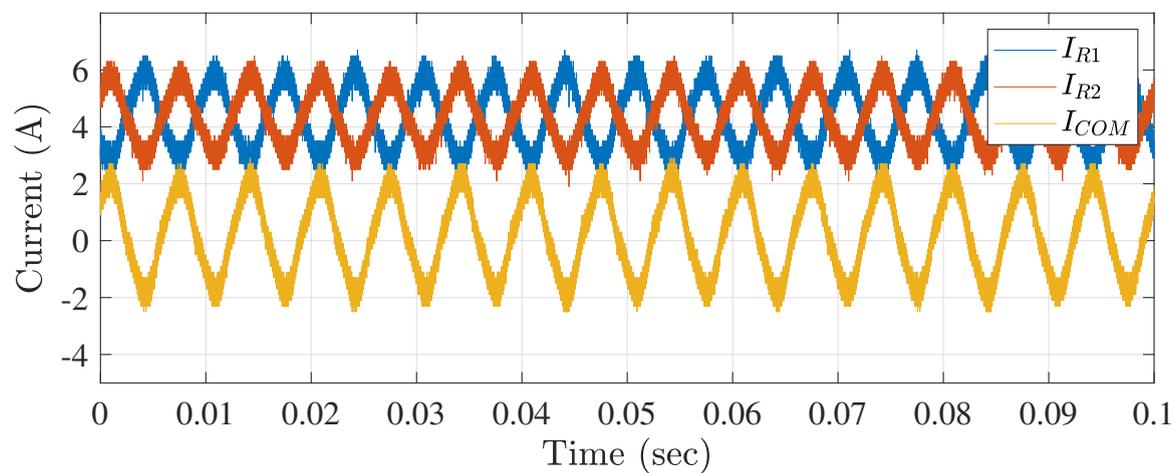
$$R_1 = R_2 = 10\Omega$$

	$k \cdot R_{com} = 1$			$k \cdot R_{com} = 10$			$k \cdot R_{com} = 100$		
	I_{R1}	I_{R2}	I_{Rcom}	I_{R1}	I_{R2}	I_{Rcom}	I_{R1}	I_{R2}	I_{Rcom}
Average Current	4.369 A	4.373 A	0.166 A	4.457 A	4.269 A	-0.015 A	4.571 A	4.194 A	-0.015 A
rms Current	-	-	1.385 A	-	-	1.271 A	-	-	0.432 A

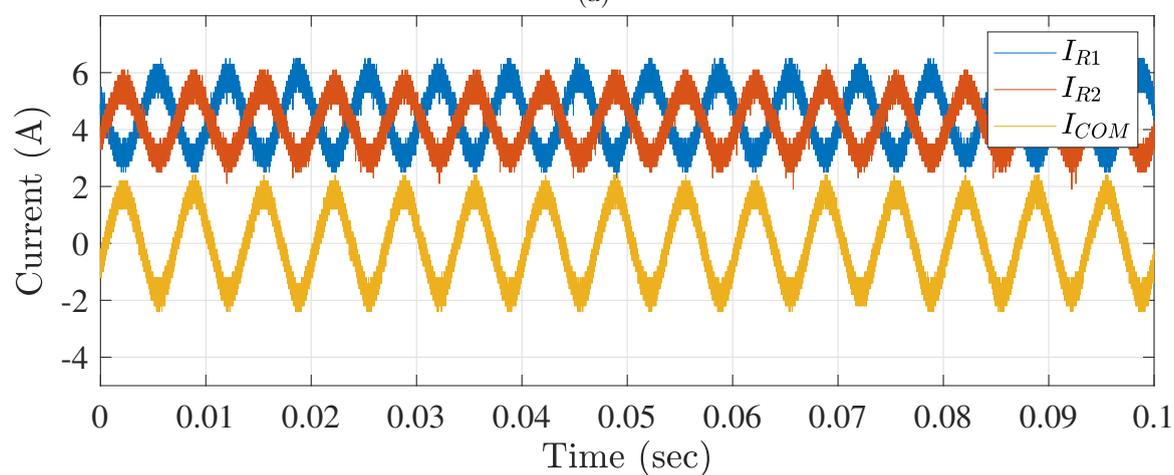
Table 4.5: Average currents corresponding to the data of Figure 4.9

$$R_1 = 10\Omega \quad \text{and} \quad R_2 = 12\Omega$$

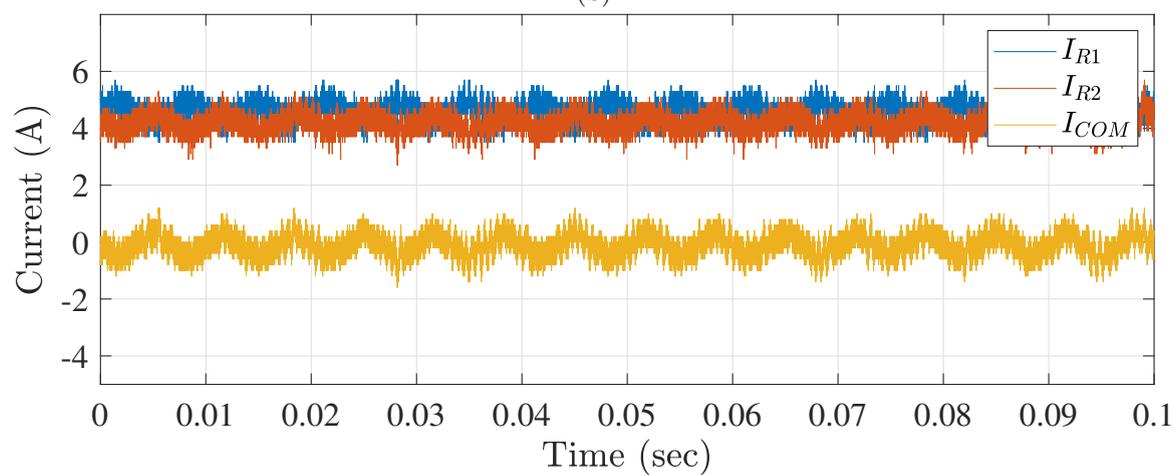
	$k \cdot R_{com} = 1$			$k \cdot R_{com} = 10$			$k \cdot R_{com} = 100$		
	I_{R1}	I_{R2}	I_{Rcom}	I_{R1}	I_{R2}	I_{Rcom}	I_{R1}	I_{R2}	I_{Rcom}
Average Current	4.481 A	4.382 A	0.072 A	4.577 A	4.277 A	-0.066 A	4.630 A	4.277 A	-0.118 A
rms Current	-	-	1.526 A	-	-	1.329 A	-	-	0.437 A



(a)

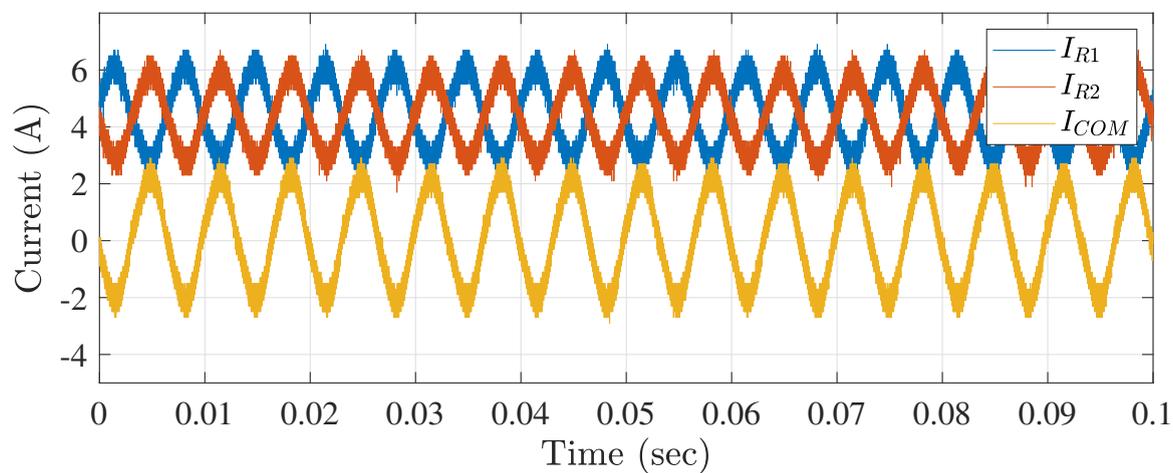


(b)

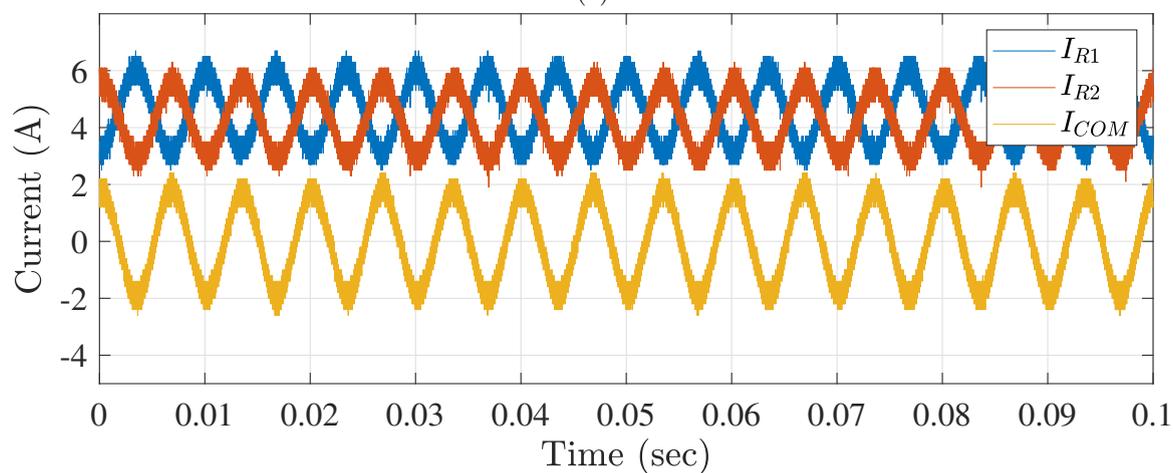


(c)

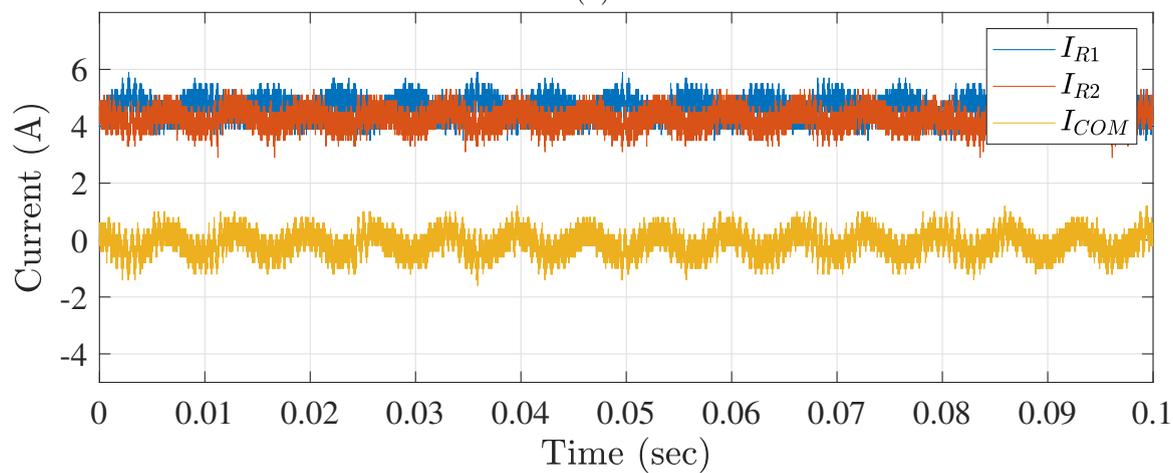
Figure 4.8: Load currents I_{R1} , I_{R2} and common-mode current I_{COM} for $R_1 = R_2 = 10\ \Omega$ for different $k \cdot R_{COM}$ values, (a) $k \cdot R_{COM} = 1\ \Omega$, (b) $k \cdot R_{COM} = 10\ \Omega$, (c) $k \cdot R_{COM} = 100\ \Omega$



(a)



(b)



(c)

Figure 4.9: Load currents I_{R1} , I_{R2} and common-mode current I_{COM} for $R_1 = 10 \Omega$ and $R_2 = 12 \Omega$ for different $k \cdot R_{COM}$ values, (a) $k \cdot R_{COM} = 1 \Omega$, (b) $k \cdot R_{COM} = 10 \Omega$, (c) $k \cdot R_{COM} = 100 \Omega$

4.5.3 PI Control

The next measurement that was conducted was the one of the PI control. Based on the promising simulation results of Figure 3.21, the current reference for the two resistors was set to 5 A, the proportional parameter k_p was set to 0.1 and the integral parameter k_i to the value of 100. When the setup was powered though, the system would not behave as expected. Instead of reaching the reference current value, as it is shown in Figure 4.10, I_{R1} appears to be zero, meaning that the current flows only through one load resistor and specifically the bottom one with a direction as per Figure 4.11. The fact that the switch S3 is constantly turned off indicates that the control variable that contains the information for the duty cycle of the second leg is always below zero. Worth mentioning that the sum of currents in node M1, based on the measurements, is not zero which indicates the existence of an error in the measuring process. This error was described earlier in this section.

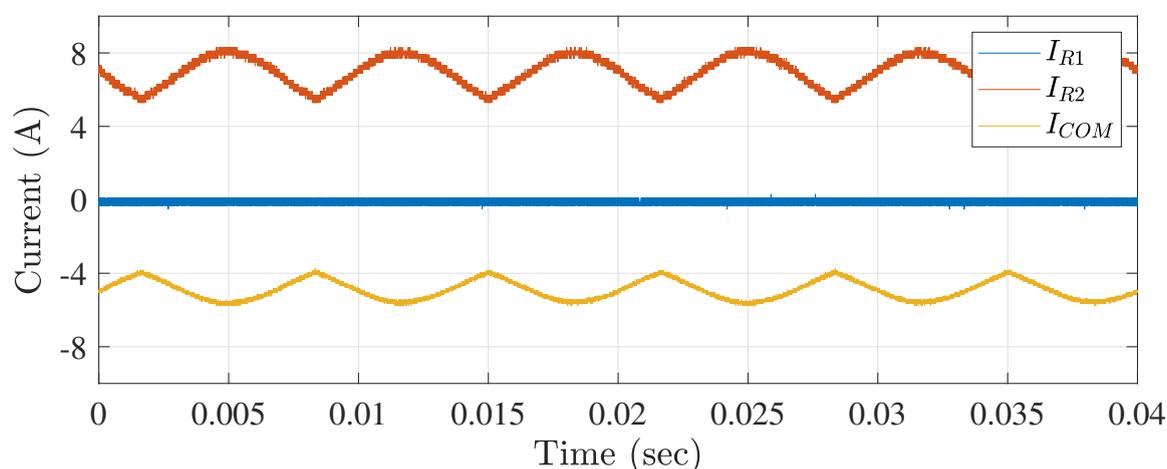


Figure 4.10: Load currents I_{R1} , I_{R2} and common mode current I_{COM} for $R_1 = R_2 = 10\ \Omega$ and $k_p = 0.1$, $k_i = 100$

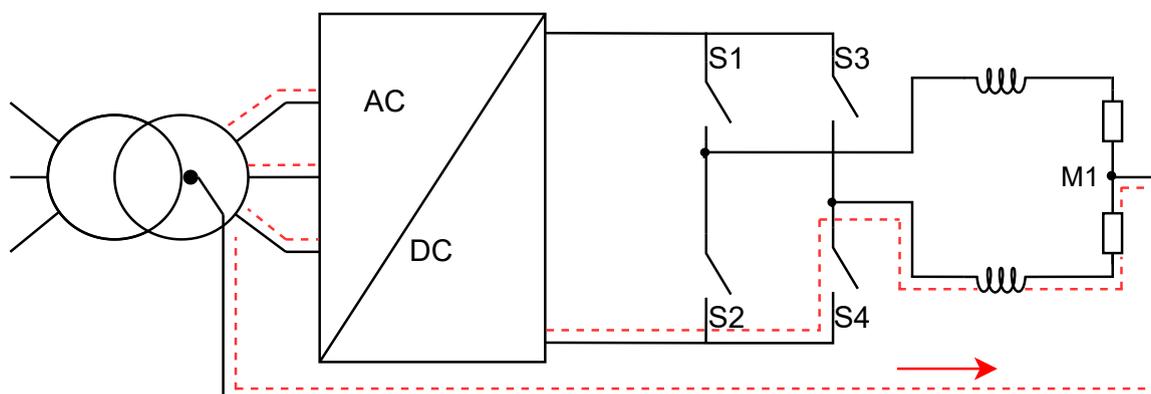


Figure 4.11: Resultant current flow when applying directly the PI control without any prior control stage.

As a first step to overcome this issue, the values k_i and k_p were changed to values that would cause a slower response. However this approach did not solve this behavior. As a second step,

the program was adjusted in such a way, to start by a constant duty cycle of 60% and 40% respectively for each leg and 10sec later to switch to the PI control. This approach generated the results of Figure 4.12a for the case $R_1 = R_2 = 10\Omega$. It can be seen that although the flowing currents are close to the reference values, their shape and frequency is different than the simulated one in Section 3.5. In the simulated waveforms is apparent a DC value of 5 A on which the previously mentioned frequencies of 150 Hz and 10 kHz are superimposed. Instead the measured results do not include the 10 kHz component which means that the converter's legs do not switch at the carrier signal's frequency but there is present an overmodulation. By applying the FFT method, the measured signal appears to have a 150 Hz, 225 Hz, 300 Hz, 450 Hz and so on components as shown in Figure A.2. The load currents have a ripple of 5.2 A which is unacceptable for an average current of 4.6 A. The PWM signals for both the legs (switches S1,S3) can be seen in Figure A.1. By applying different k_i and k_p parameters, the waveforms of Figure 4.12b were retrieved. However, the results were not adequate.

As a last attempt to operate the system with the PI control, the open-loop stage prior to the PI was removed. The system was once again operated with $k_p = 0.01$ and $k_i = 2000$ and the measured waveforms can be seen in Figure 4.12c. Contrary to the previous result, the 150 Hz component is present, while the 10 kHz component is not. A steady-state error is present, as the average values of the currents differ from the reference of 5 A. As this measurement has similarities to the simulated results, it is believed that further calibration of the k_p and k_i parameters could improve the system's behavior. However, when the measurement was repeated, one of the switches was burnt and the system became inoperational.

In total, although in simulations the PI control's performance is promising, applying it on hardware brought to the surface several inconsistencies. A more systematic execution and better calibration of the PI's parameters could significantly improve its behavior. Due to the PI controller's strong influence, the results obtained for PI+Feedforward showed similar behaviour as the PI. This can be seen in Figure A.11.

Table 4.6: Average and rms currents corresponding to the data of Figure 4.8

		$R_1 = R_2 = 10\Omega$								
		$k_p = 1 \quad k_i = 100$			$k_p = 0.01 \quad k_i = 2000$			$k_p = 0.01 \quad k_i = 2000$		
		I_{R1}	I_{R2}	I_{Rcom}	I_{R1}	I_{R2}	I_{Rcom}	I_{R1}	I_{R2}	I_{Rcom}
Average Current		4.609 A	4.635 A	0.049 A	4.696 A	4.673 A	0.113 A	5.901 A	6.772 A	-0.258 A
rms Current		-	-	1.097 A	-	-	1.147 A	-	-	1.031 A

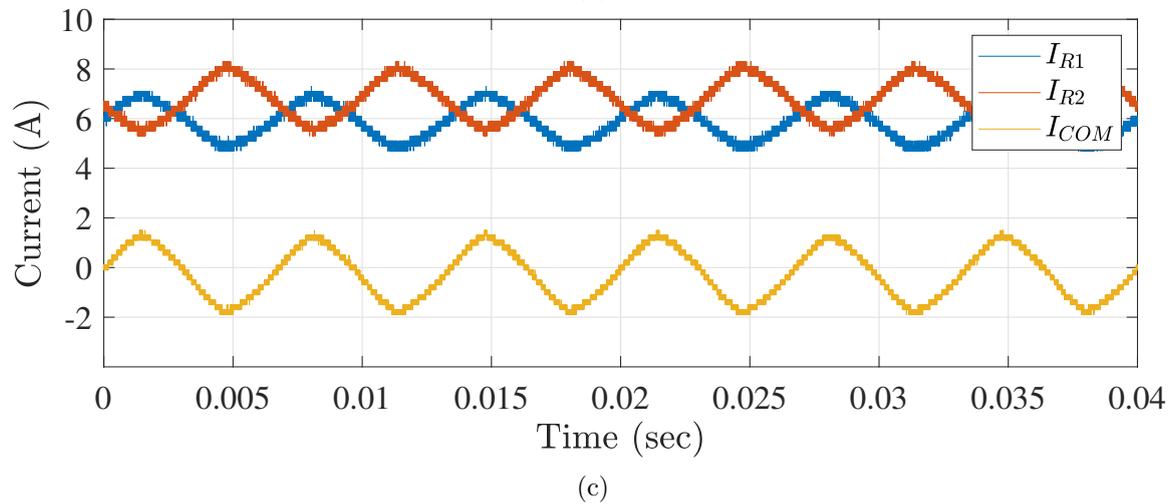
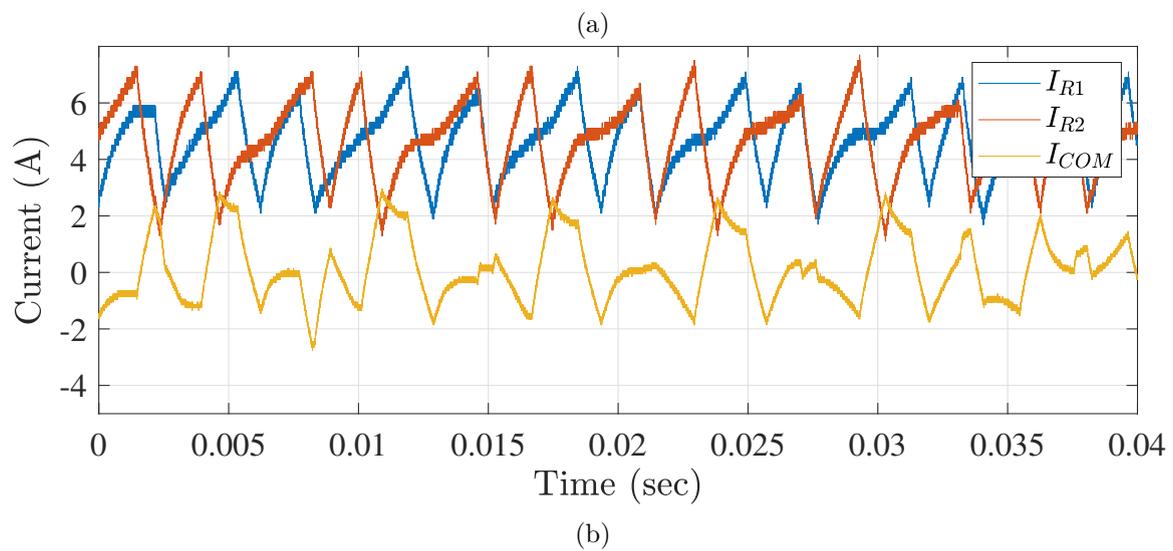
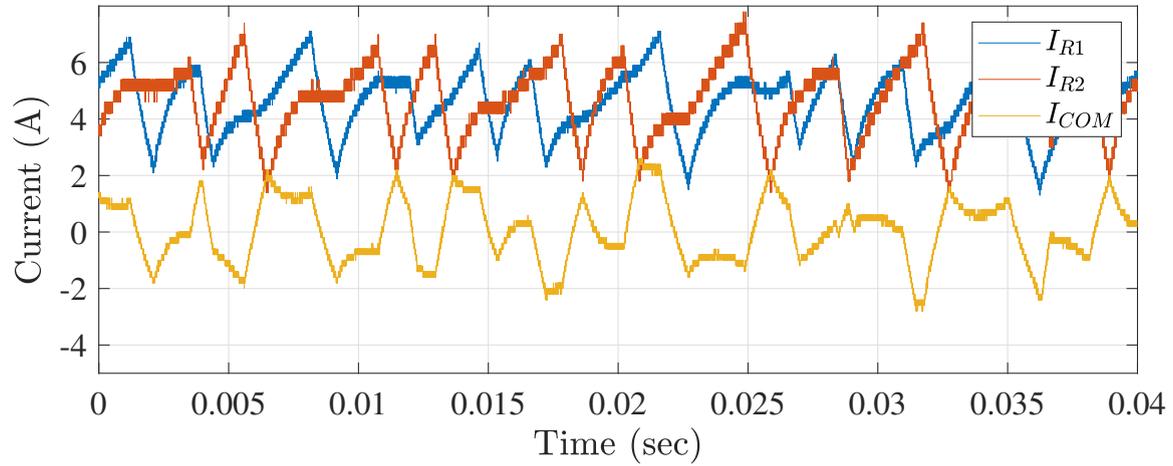


Figure 4.12: Load currents I_{R1} , I_{R2} and common mode current I_{COM} for $R_1 = R_2 = 10\ \Omega$ and different values of k_i and k_p , (a) $k_i = 100$, $k_p = 1$, (b) $k_i = 2000$, $k_p = 0.01$, (c) $k_i = 2000$, $k_p = 0.01$, without open-loop pre-stage

Chapter 5

Conclusion

This thesis addressed the problem of common-mode and circulating currents in modern electrolyzer systems, which have adverse effects on their lifetime, efficiency, and proper operation. In this regard, a simplified yet representative system of an electrolyzer power supply topology was implemented. This topology consists of a diode rectifier AC/DC stage and a full bridge DC/DC converter.

Through simulations, the origins of the problem were located and different control strategies were applied to the DC/DC converter to investigate their impact on the common-mode current. The initial control strategy was the Feedforward approach, which is based on removing the common-mode component before its generation in the system. The limitations with respect to this control scheme lie in its dependency on the varying equivalent load's resistance. The second control strategy is based on a PI controller, which has the capability to follow a current reference value independent of parameter variation.

The simulation results indicate the potential of both control techniques to address and minimize the common-mode voltage individually. However, the Feedforward approach was incapable of maintaining the desired DC current when the electrolyzer's equivalent resistance changed, and the PI controller was unable to cancel the 150 Hz component. As a result, a combination of both control strategies, namely the PI + Feedforward controller, was explored and showed remarkable potential in simulations. Specifically, in the simulated cases, the common ripple on the load current was reduced to 4 % of the reference value.

To further evaluate the above control strategies, a hardware setup was developed in the laboratory. After establishing the safe operation of the setup, the aforementioned control strategies were applied in hardware. The performance of the Feedforward control was successfully validated, achieving a reduction of the common-mode current by 320 % by adjusting the influence of the common-mode voltage in the applicable duty cycle signals.

However, in the case of the PI controller, the measured results did not meet the expected performance and it further led to the failure of the EVAL board. This influenced the hardware implementation of the PI + Feedforward control scheme, which also did not yield the expected results.

Although it was not possible to successfully achieve all the goals of this thesis, strong indications exist that similar results to those obtained in simulations can be achieved in hardware. Further analysis and experiments are necessary to characterize the proposed control technique as successful.

Chapter 6

Future Scope

In this chapter, several suggestions for future work are proposed, aimed at further exploring and improving the behavior of the Feedforward, the PI and the PI+Feedforward control techniques. A more comprehensive investigation can be conducted on the Feedforward control, including a thorough mapping of values that minimize the common-mode current and the development of techniques for on-line tracking of changes in the load resistors. Such a capability could help update in an automatic way the duty cycle signals and improve the Feedforward's control performance.

Additionally, estimating the system's transfer function and implementing a more systematic calibration of the control parameters for the PI controller would contribute to the extraction of safer conclusions regarding its behavior. Given the previous, the successful implementation of the PI + Feedforward control would be the natural outcome.

Regarding the hardware tests aspect, it is proposed to investigate the factors that led to the improper operation of the PI control in the laboratory, resulting partly to the destruction of one evaluation board. Identifying and understanding these reasons will facilitate the enhancement of the hardware setup and prevent similar issues in the future.

Once a reliable control approach has been established and validated, the next crucial step is to investigate the feasibility and benefits of paralleling the two systems. This investigation will explore the potential advantages of the control schemes by combining multiple systems, paving the way for further optimization and scalability in the design of the power supply setup.

These future directions hold great promise for advancing the field and addressing the challenges identified in the present study, ultimately contributing to the development of more efficient and reliable power supply solutions for hydrogen production in large-scale installations.

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Appendix A

Supplementary Material

This appendix contains all the supplementary drawings, screenshots and photos that might indirectly support findings and explanations of the previous chapters.

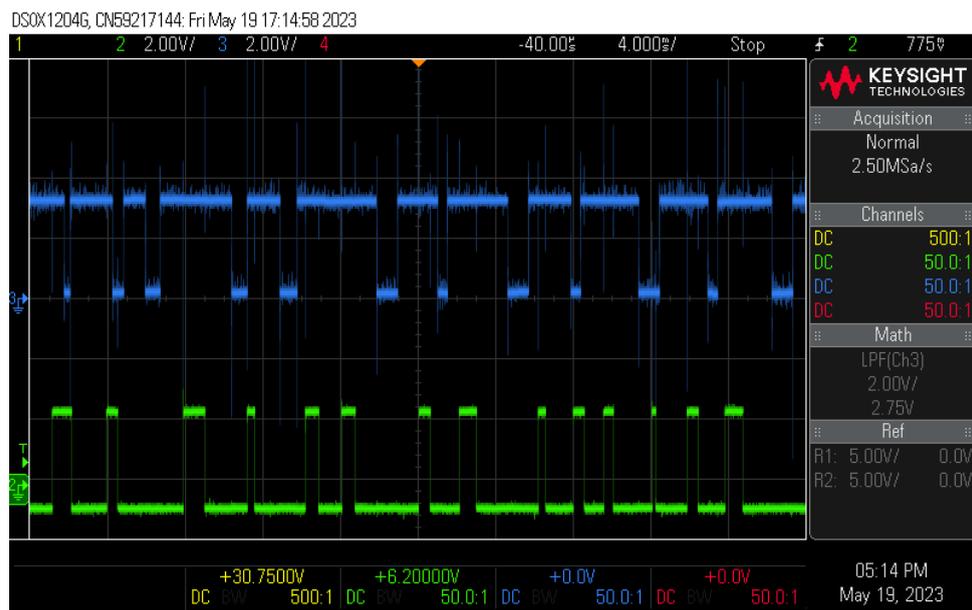


Figure A.1: Gate pulses for S1 and S3 in the case of the PI control. It can be seen that the switches do not operate at the carrier signal's 10 kHz switching frequency.

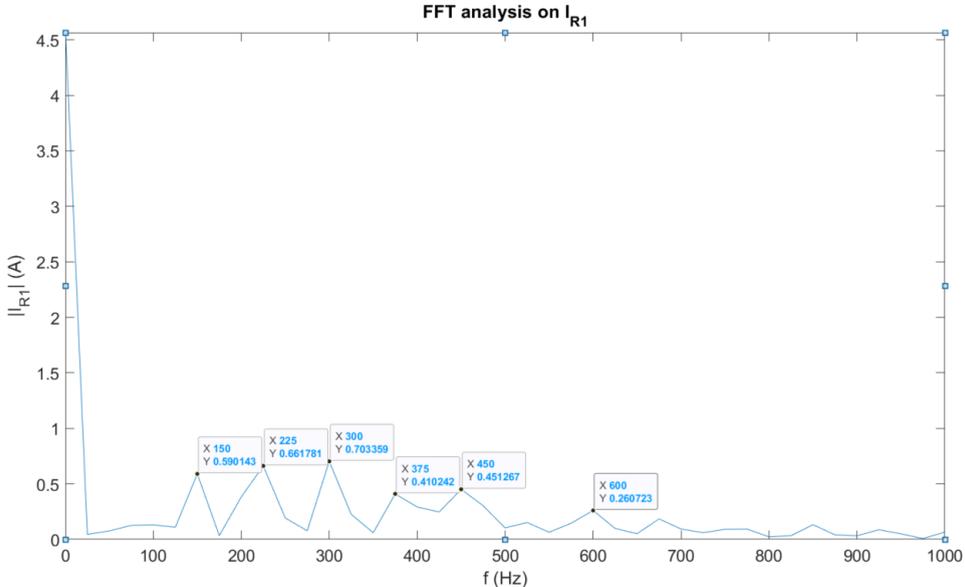


Figure A.2: FFT of Figure A.1. Significant frequency content at not expected frequencies.

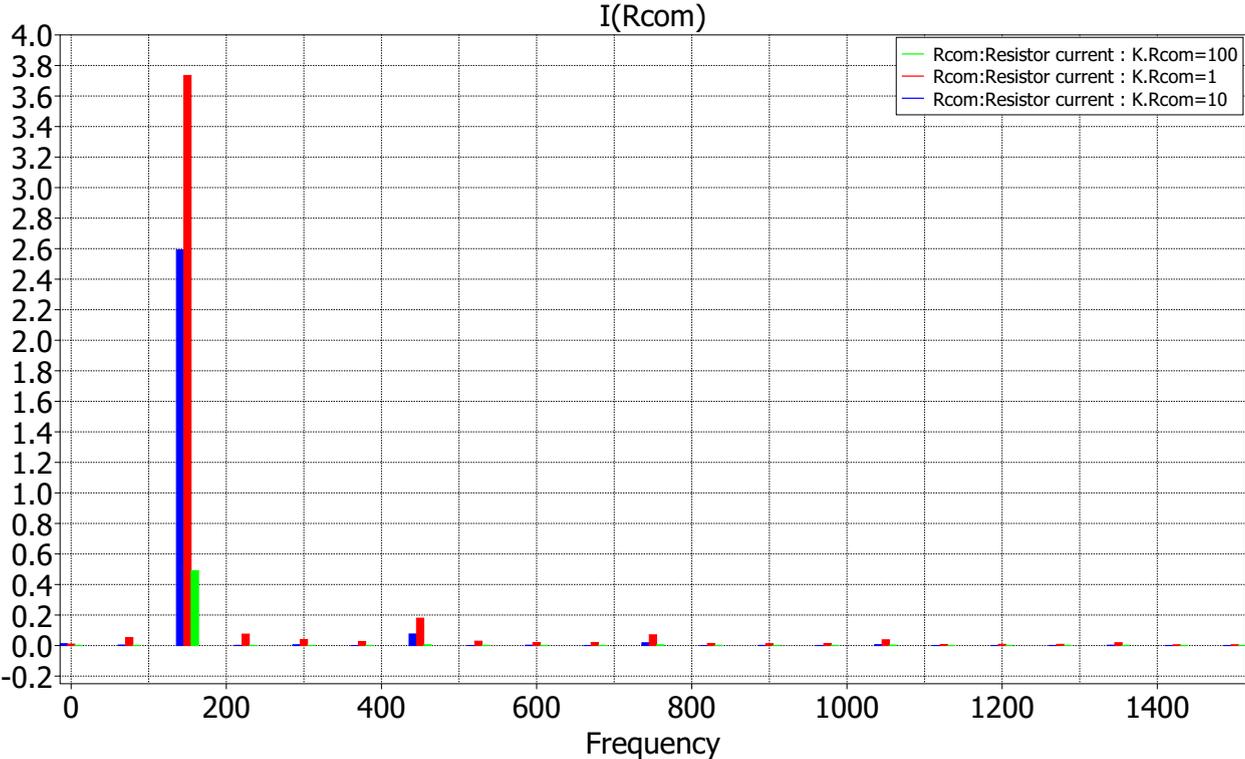


Figure A.3: Fourier spectrum of common-mode current I_{com} with feedforward controller showing a reduction in the magnitude of 150 Hz component

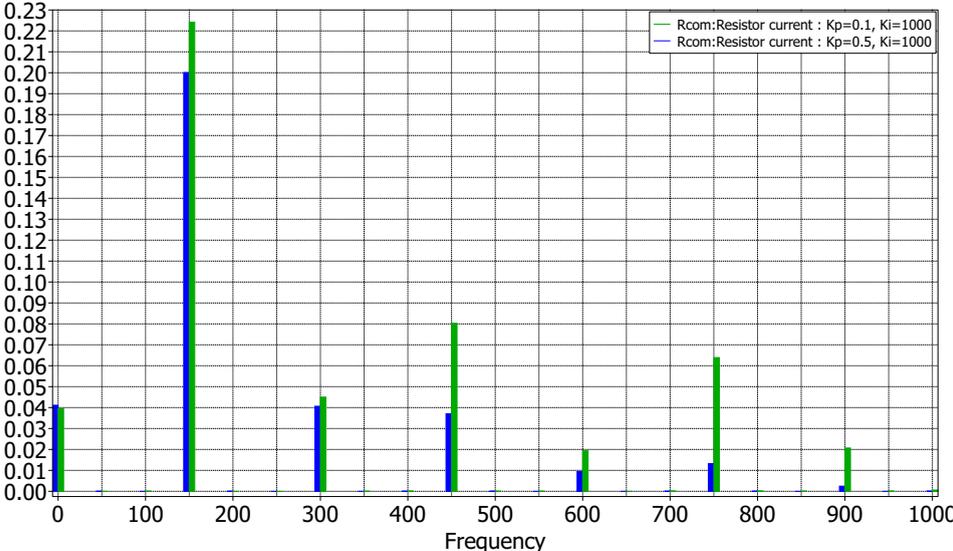


Figure A.4: Fourier spectrum of common-mode current I_{com} with PI controller showing presence of unwanted harmonics

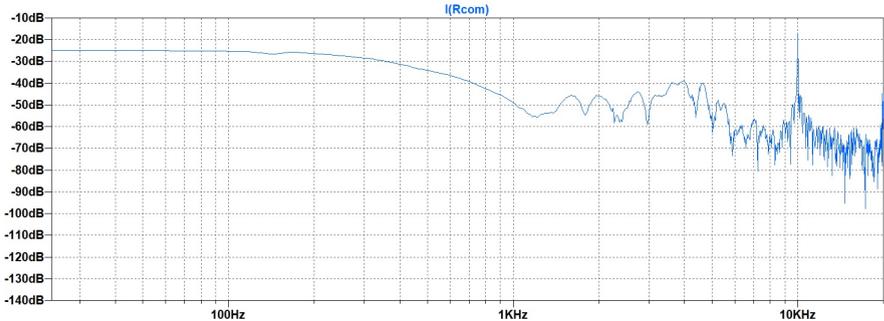


Figure A.5: Fourier spectrum of common-mode current I_{com} with PI+feedforward controller showing minimisation of 150 Hz component

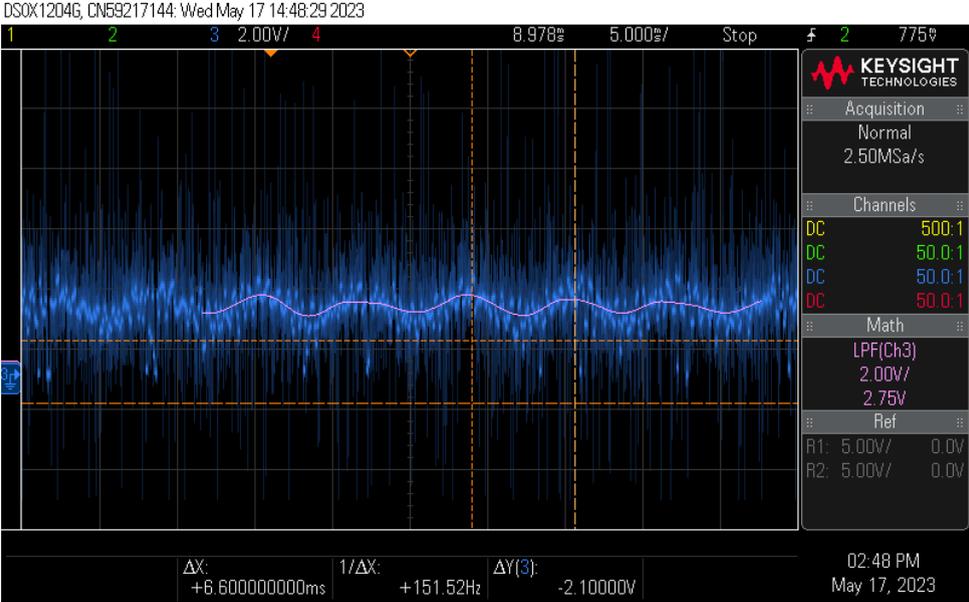


Figure A.6: Duty cycle signal retrieved using the DAC of the micro-controller for the case of Feedforward control.

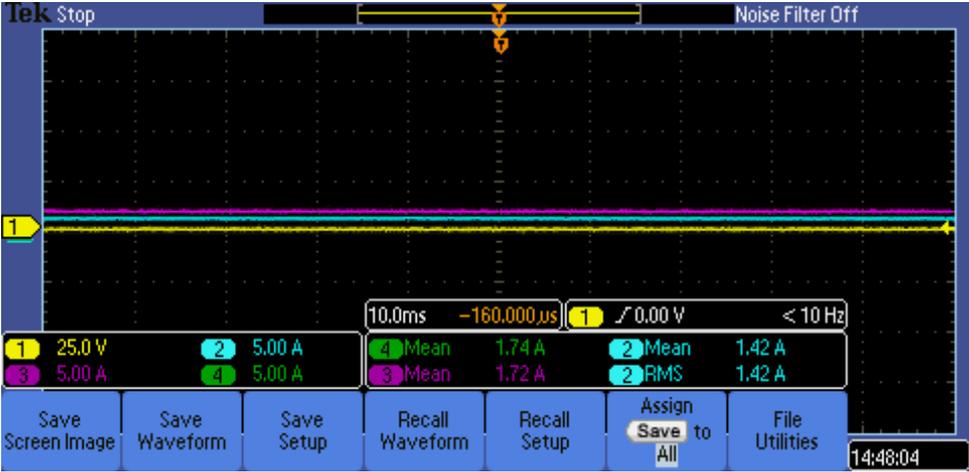


Figure A.7: Current measurement for the DC test to confirm error

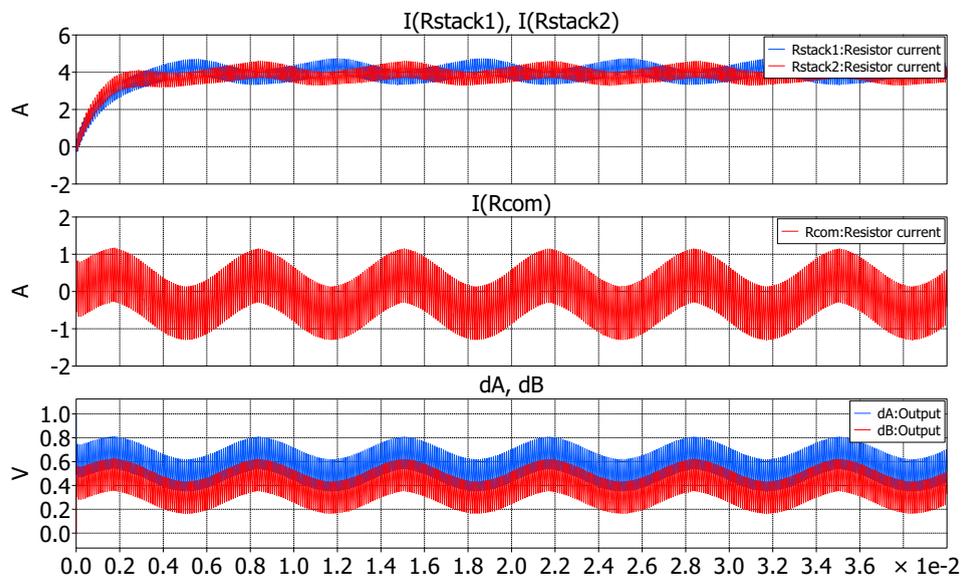


Figure A.8: Simulation results with feedforward controller with I_{ref} as 5 A; the value of R_{stack2} was kept to $16\ \Omega$ while the equation for dA uses 10

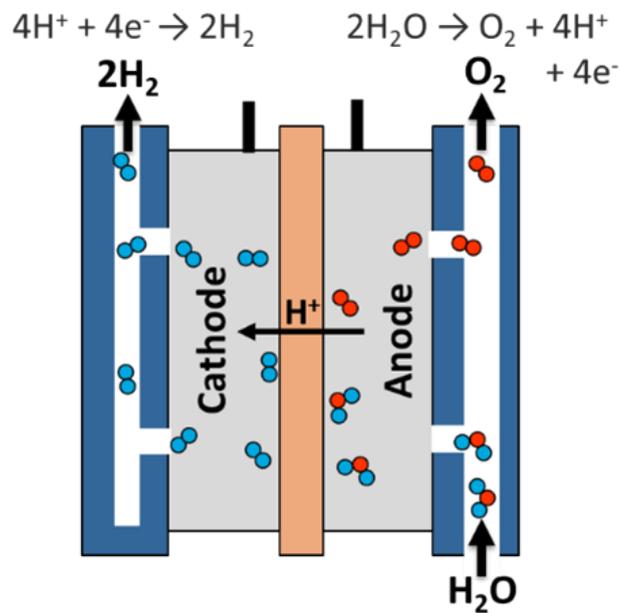


Figure A.9: PEM electrolysis process

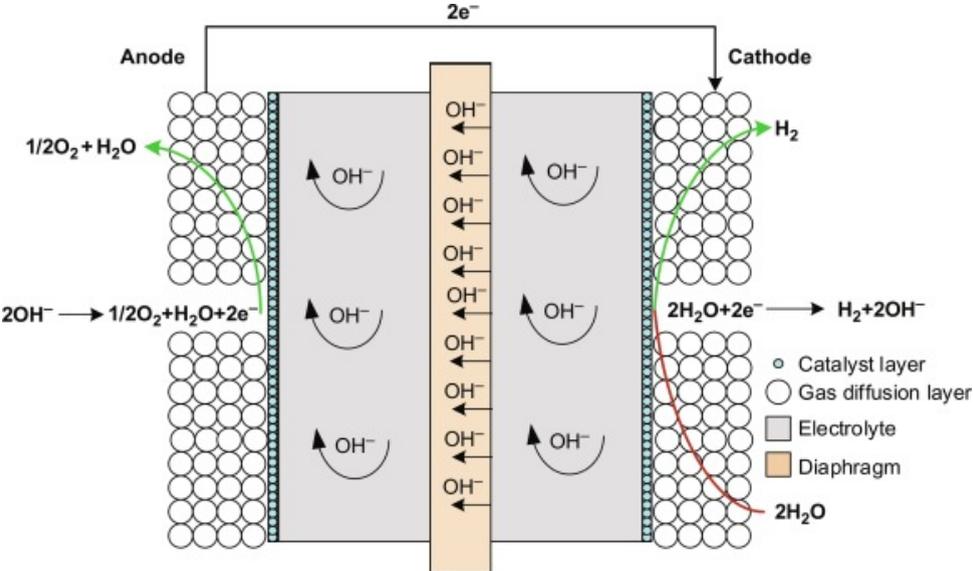


Figure A.10: Alkaline electrolysis process

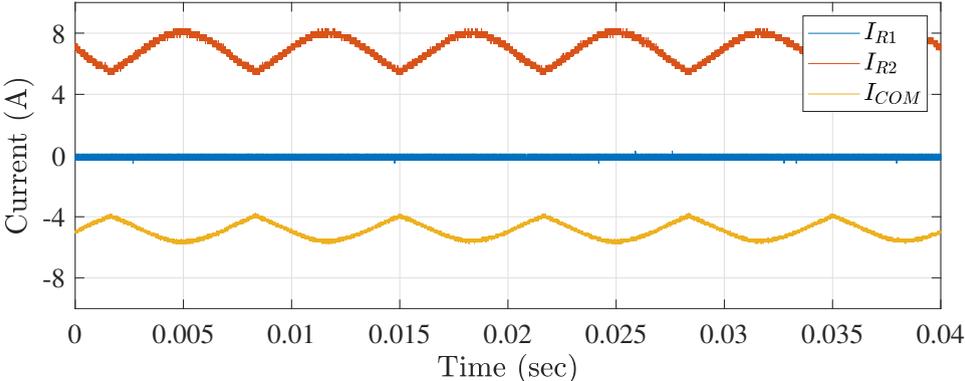


Figure A.11: PI + Feedforward control measurement