Master of Energy Engineering - Master thesis

A Generalized Double Pulse Test With Potential Short Circuit Protection For SiC-MOSFET's

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Abstract:

This project investigates a generalized double pulse test to characterize a MOSFET's switching losses. This is achieved by designing an inductor and capacitor that charge to the specific voltages and currents in a given time. From the double pulse test, the voltage and current under "turn off" and "turn on" are measured and used to calculate the switching losses. After developing the double pulse test in the laboratory, LT-spice has been chosen to model the double pulse test in simulation and to compare such simulation to the laboratory test. Subsequently, the switching losses are compared under different voltages and currents to test for the general part of the double pulse test. Lastly, the LT-spice simulation also demonstrates possible short-circuit protection for a double pulse test setup. Investigating the short circuit protection shows that a crowbar can protect a MOSFET under testing. Overall, this project illustrates that the MOSFET switching losses can be extracted using the designed generalized double pulse test, and that a crowbar can protect the MOSFET.

Preface

This master thesis is prepared by Steffen Peters, a student in the Master's program *Power Electronic and Drives* in Energy Engineering at Aalborg University. *Semiconductor power loss* is the overall theme of the project.

The prerequisites for reading the report require a certain knowledge of mathematics, physics, circuit analysis theory and power electronics.

The supervisors offered a lot of useful advice and feedback during the project work. The supervisors' guidance and assistance at each stage has paved the way for this thesis.

Reading instructions:

In this project, the Vancouver method is used for referencing, which means that after every section the reference will be listed as [1, 2, 3, etc.]. All references are sorted as they appear in the report and will be included in the bibliography at the end of the report. Books are specified with author, title, edition, and publisher. Websites are specified with author, title, year, link, and visit date.

The project contains figures, which are numbered by the chapter, hence the first figure in Chapter 1 has number 1.1 and the following figure has number 1.2, etc.
The symbols and the abbreviation in the nomenclature are listed in alphabetical order.

Aalborg University,
June 1, 2023

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Nomenclature

Abbreviations

DPT	Double Pulse Test
DSP	Digital Signal Processor
KCL	Kirchhoffs current law
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
SC	Short Circuit
SiC	Silicon-Carbide
WBG	Wide-Bandgap

Symbols

+	More doping
−	Less doping
Δ	Differences
μ	micro
μ_0	Permittivity
Ω	Ohm
ω	radians per second
A	Ampere
A_c	cross-sectional area
C	Capacitor
c	Specific heat
CH	Channel
D	Diameter
D	Drain
E	Energy
F	Farad
G	Gate

H	Henry
I	Current
k	kilo
L	Inductor
m	Volume
N	Number of windings
n	Electrons
off	off
on	on
P	Holes
p	Parallel
R	Resistor
S	Source
s	Seconds
sp	Series parasitic
T	Temperature
t	time
t_1	specifics time
V	Voltage
W	winding width

1 Introduction

When manufacturing semiconductors, silicon has been the preferred material for designing and implementing transistors. With advancements in semiconductor materials, this preference is shifting to compound materials such as Silicon-Carbide (SiC) and Gallium-Nitrate. Over time, these changes in material lead to superior characteristics resulting in optimized and efficient devices. [1], [2] When shifting from silicon Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)s to SiC MOSFETs, the device's physical size decreases. This reduction in size is due to the increased distance between the valence band and the conduction band, which is the reason it is named Wide-bandgap (WBG). Another change when switching to WBG is the increased operating Switching frequency, as SiC has a higher Drift velocity. [1], [3] Shifting from silicon to SiC has advantages and disadvantages, as shown in table 1.

Advantages	Disadvantages
Higher breakdown voltage	Cost of material
Higher thermal stability	Cost device
Compact packaging	Cost of packaging
Reduced Volume	Low channel mobility
Cost of passive components	Threshold voltage 40 % deviation
Same insulator as Silicon	Change of circuit topology
Higher switching frequency	New gate drivers required

Table 1: Advantages and Disadvantages of SiC [4]–[6].

As shown from the disadvantages in table 1, solving these disadvantages will result in SiC becoming the go-to solution. These disadvantages will reduce as time passes due innovations in SiC technology, allowing the manufacturer to reduce the manufacturing cost and the other disadvantages. [7]
With the increasing use of SiC MOSFETs, characterization concerning its switching loss and conduction loss is becoming more critical, as every joule saved will reduce the energy losses and thereby reduce the emissions produced. Such reduction is especially important considering the increase in the use of power converters and their use of SiC MOSFETs.

It is possible to use a power converter to characterize the device. Though, it would be expensive and time-consuming as it requires building a specific power converter to characterize one device. Therefore using a method for early characterization is considered. Double pulse testing (DPT) is a widely accepted method for it. The circuit of the DPT is shown in figure 1.1. The DPT simulates the working inside a power converter through two pulses. By regulating the pulse width and the amplitude of the pulses, measurement under any voltage and current ratings is possible. With the measuring results, the switching losses are calculated for the MOSFET. These switching loss calculations can subsequently be used in a power converter design to define the converter's efficiency. [8], [9]

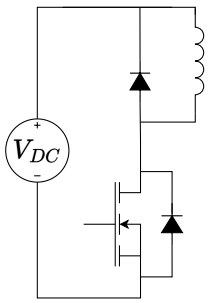


Figure 1.1: Simplified double pulse test.

For the DPT, there are four steps:

1. The MOSFET is turned on long enough for the inductor to charge to the defined current.
2. When the inductor is charged, the MOSFET will be turned off, and the turn-off losses will be measured.
3. There is a defined break time until the MOSFET is turned-on.
4. The MOSFET is turned on again to measure the turn-on loss.

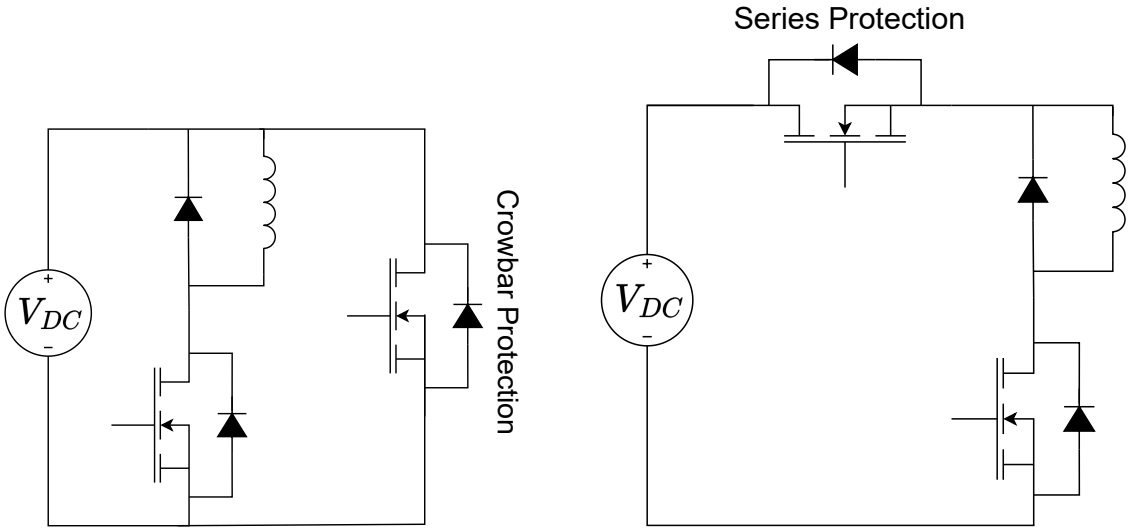
The pulses must be as short as possible to prevent temperature change in the MOSFET and long enough to account for the dead time and transients. [8]–[11]
With faster switching and altered device properties, the new iterations of testing Sic MOSFETs will require an adjustment in DPT. As mentioned by [10], the DPT and its working principles are fully explored for silicon and SiC MOSFETs under 1 kV. Even though it is fully understood, there are no standards regarding the setup of a DPT.

The MOSFETs tested with DPT are often prototype MOSFETs, and there may only exist one, so the production of extra MOSFETs would be expensive and time-consuming. Therefore protection of the MOSFET against short circuits and, thereby, device failure should be considered. [8]
When designing protection schemes for SiC MOSFETs, requirements change compared to silicon devices. These requirements are[12]:

- Smaller chip area and higher current density result in lower Short Circuit (SC) withstanding.
- Leakage current after 5 µs means a shorter response time for protection is required.
- Higher gate bias results in a larger SC.

These requirements mean that it is crucial to have fast protection to protect against the points mentioned above. There are three possible solutions for the problems: the protection is in series with the MOSFET, the other is in parallel, and lastly, desaturation protection by switching the MOSFET itself to the off state.
Shown in figure 1.2 is the series protection and the parallel protection, also called crowbar protection. The first protection scheme is the series protection scheme that works by

measuring the current, and if it detects a SC or over current, it will trip a switch between the power supply and the SiC MOSFET, thereby clearing the fault. The second scheme is Parallel protection which works by causing an intently short circuit, thereby giving a lower impedance pass and clearing the SC. [9], [13], [14]



(a) Turn-off switching losses **(b)** Turn-on switching losses

Figure 1.2: Switching losses of real-world with 30 Ω gate Resistance.

The series protection can use a fuse or an electrical fuse. The fuse disconnects the MOSFET from the power supply when a current exceeds its limits, destroying the fuse. When using a fuse, switching to an electrical fuse has its advantages, such as a faster turn-on time and is easier to reset because it is not required to replace the fuse because the electrical fuse is nothing more than a semiconductor that switches from the on-state to the off-state when an SC is detected. When an SC occurs, all the energy in the capacitor flows through the electrical fuse.This energy flow might destroy an electrical fuse, as it does not have sufficient blocking capability. Adding more than one electrical fuse in a series improves the voltage-blocking capability. [15]
The second protection is crowbar protection shown in fig. 1.2a. The device is required to have a lower impedance than the branch where the SC occurs. Then when the SC occurs, the switch closes, and the energy can flow through. When using the crowbar protection, a series fuse is often triggered from the intentional SC, thereby disconnecting the MOSFET from the power supply. [16]
Triggering the semiconductor in the series and crowbar protection requires some detection. The most common detection method is to detect the voltage drop of drain to source of the device [17].
The third possibility of protection is to use the device itself, which is called the desaturation technique. The desaturation functions by using the MOSFETs IV curve. When considering a MOSFETS IV characteristic, the fault occurs in the saturation region. After that, the

protection switches the MOSFET off before it stops to withstand the SC [18], [19].

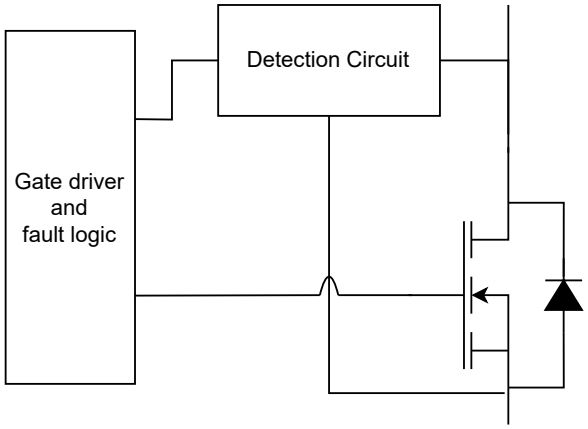


Figure 1.3: Desaturation SC protection.

1.1 Case study - SiC MOSFET DPT

Testing of MOSFET is a crucial step in the specification of the dynamic performance of the device. Each newly developed MOSFET requires testing. Therefore, the DPT must be consistent in the testing of these devices. Developing a fixed storable setup is considered.
The DPT setup should not be limited to one device, as this would reduce the idea of a reusable setup. To increase the use of the test bench, the DPT should test different MOSFETs between 100 V and 600 V., thereby being a test bench with a wide range of use. The test bench sizing is important, as using wrong sizing could mean it could only be used on one specific module.
When testing MOSFETs, there is the risk of fault which could destroy the MOSFET. Considering the price of the SiC MOSFETs, one destroyed module could be a significant loss of revenue. Therefore, it is crucial to know what the protection is for and how it protects. In this case, a short circuit fault will be considered, and prospective protection will be explored. When considering short circuit protection, there are multiple possibilities to implement it. For this reason, the best protection scheme is chosen.
As protection is one part that requires consideration when buying a test bench, some research is required to get the matching test bench. The current producers of DPT test benches include Keysight PD1500A and Tektronix AFG31000. These producers do not offer device protection and focus on a discrete package. This project, in contrast, focuses on the module package.

1.1.1 Problem statement

How can a SiC MOSFET be tested at different voltages and currents using a generic DPT and thereby extract the switching losses and investigate how to protect against short circuit faults?

1.1.2 Objectives

The Primary objectives for solving the problem statement are:

1. Analysis of used components and system.
2. Design of the components.
3. LT-spice model of the Half Bridge.
4. Design/use of measuring/capturing devices.
5. Ideal simulation of the DPT.
6. Non-ideal simulation of the DPT.
7. Extract switching losses.
8. Short circuit test.
9. Short circuit protection test.

1.1.3 Limitations

Limiting the project is crucial to solving the problem statement in time. The following are the limitations of the project:

1. In-depth analysis of the short circuit behaviour of MOSFET.
2. Only the electric behaviour of the MOSFET is analysed.
3. Voltage drop of the capacitor should only be 20 volt.
4. The simulation is made from the laboratory DPT.
5. MOSFET may only have a temperature rise of 1°.
6. SC is only explored in simulation, for safety and because of time constrains.
7. The SC is only added but not explored in depth.
8. The DPT is only run at ambient temperate.

2 Operation and working principle

This section explains the different components of the DPT, how they work, and the DPT itself. After it explains the DPT, the short circuit event and the protection is also explained.

2.1 MOSFET working principle

Understanding the MOSFET working principle is essential for the DPT, as without, the results can not be verified. Therefore, it is first required to look at what happens in a switching event, which is the main part of the DPT, as it is where it extracts the switching loss.
For the MOSFET to switch in a switching event, the MOSFET requires to move the charge in the stray capacitance. The switching events are analyzed. For this, it requires having an equivalent circuit that can explain the switching behavior [20].
Figure 2.1 given from [20] shows the cross-section of a MOSFET with its different doped regions. By examining the cross-section, the different parasitic capacitances are the charge build-up between the different intrinsic regions.

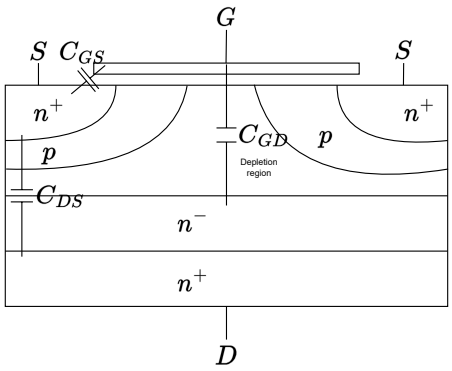


Figure 2.1: Origin off the capacitance.

Considering figure 2.2 it is possible to arrive at the equivalent circuit of the SiC MOSFET with its parasitic capacitance. This equivalent circuit is used to describe the switching event in detail by splitting it into four switching events as mentioned by [20]–[22].

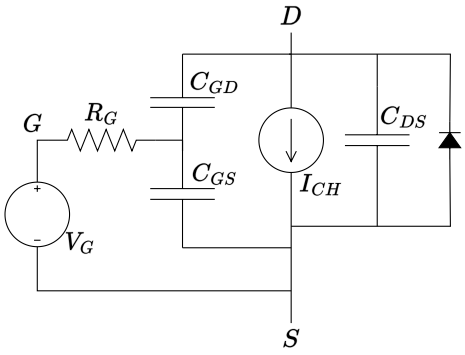


Figure 2.2: MOSFET active region equivalent circuit.

Shown in fig. 2.3 is the first turn-on event where red arrows and the red path indicate the current flow.

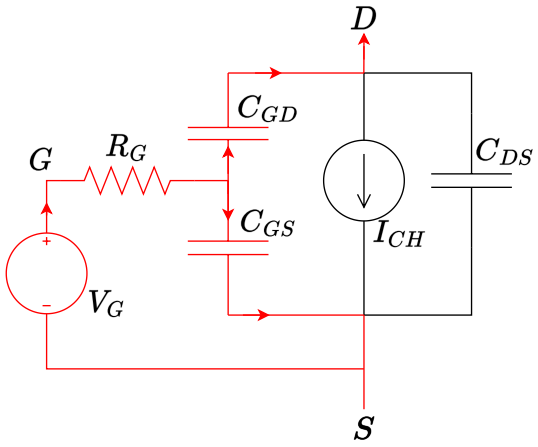


Figure 2.3: MOSFET first turn-on event.

Before the first turn-on event, no current is running through i_D as V_{th} has yet to be reached. V_{DS} has its full potential as there is no current flowing through i_D. First, voltage V_{GS} is applied because $V_{GS} < V_{th}$ in the first turn-on event, and there is no current flow through i_D. This event continues until the gate voltage reaches the threshold voltage. Simultaneously, the current I_G decreases with the capacitors' charge. Using Kirchhoff's Current Law (KCL) on the circuit in fig. 2.3, it is possible to arrive at the equation for the gate current eq. (1).

$$I_G = I_{GS} + I_{GD} \tag{1}$$

Considering that the gate current depends on the current over the capacitors, and the current ocer the capacitor is given by eq. (2).

$$I_C = C\frac{dV_C}{dt} \tag{2}$$

Where the voltage equation is given as eq. (3).

$$V_{DS} = V_{GS} - V_{GD} \tag{3}$$

Because there is no change in voltage over V_{DS} in the first switching phase. The voltage change is over the capacitors C_{GS} and C_{GD}, considering this eq. (1) can be rewritten as eq. (4).

$$I_G = (C_{GS} + C_{GD})\frac{dV_{GS}}{dt} \tag{4}$$

The last part of this missing equation is I_G, which is current over the resistor.

$$I_G = \frac{V_G - V_{GS}}{R_g} \tag{5}$$

With the equations, the current and voltage waveforms in fig. 2.7 in the t_{Delay} phase is described.

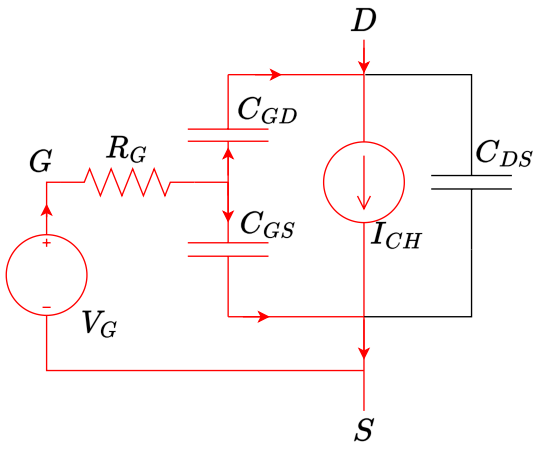


Figure 2.4: MOSFET second turn-on event.

The second turn-on event starts when the gate voltage reaches the threshold current. After reaching the threshold, the current starts to flow through the channel and is defined by eq. (6). The current flow in the circuit is shown in fig. 2.4.

$$I_{CH} = I_{GD} + I_D \tag{6}$$

While the current starts flowing through the channel, V_{DS} is kept constant as there is no space for the charge in V_{DS} to dissipate.
The third Turn-on event starts after the current I_D has reached its maximum value as shown in fig. 2.7. In this stage, the voltage V_{DS} falls to zero because the charge in C_{DS} is first dissipated after I_D has reached its nominal value, then adding its own charge to I_D which is the reason for the current going over its nominal value and then falling again. Shown in fig. 2.5 is the current flow in the third turn-on event. All three capacitances have a current flowing through them; using KCL makes it possible to arrive at eq. (7).

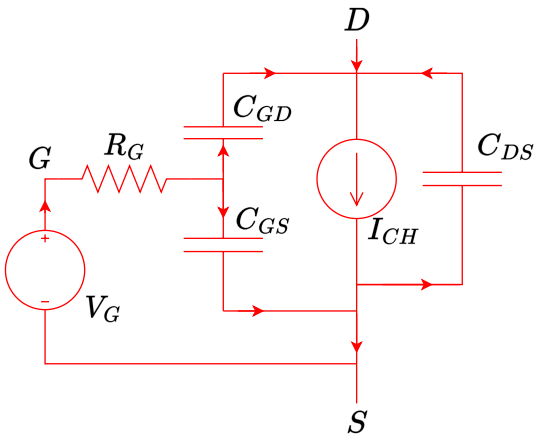


Figure 2.5: MOSFET third turn-on event

$$I_{CH} = I_{GD} + i_D + i_{DS} \tag{7}$$

In this stage, the capacitance's C_{GD} and C_{DS} are delivering the current resulting in eq. (7). Because the increase in V_G, due to I_G continuing to run through C_{GS} and thereby increasing V_G, it increases I_{CH} which means it comes from C_{GD} and C_{DS} still having charge. Because eq. (1) an increasing C_{GD} results in a decrease in C_{GS}.

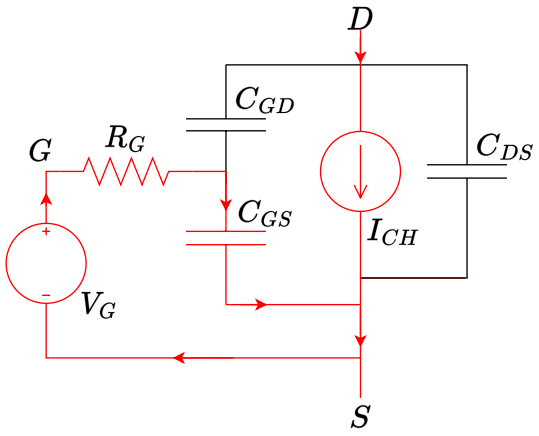


Figure 2.6: MOSFET Forth turn-on event.

The fourth turn-on event starts when the voltage is below the threshold voltage and the MOSFET transitions from the saturation to the Triode region shown in fig. 2.8. In this phase, the current flowing through C_{DS} and C_{GD} becomes close to zero and is therefore not considered. This results in the gate current flowing only through C_{GS} arriving at eq. (8).

$$I_{gs} = \frac{V_g - V_{gs}}{R_g} \tag{8}$$

and the channel is conducting the current, thus arriving at eq. (9).

$$I_{CH} = I_D \tag{9}$$

Considering these switching events the energy loss can then be calculated by integrating the Power over time [23].

$$E_{on} = \int_0^{t_1} V_D S(t) \cdot i_D(t)\, dt \tag{10}$$

$$E_{off} = \int_0^{t_1} V_D S(t) \cdot i_D(t)\, dt \tag{11}$$

The switching waveform for the explained switching event is shown in fig. 2.7.

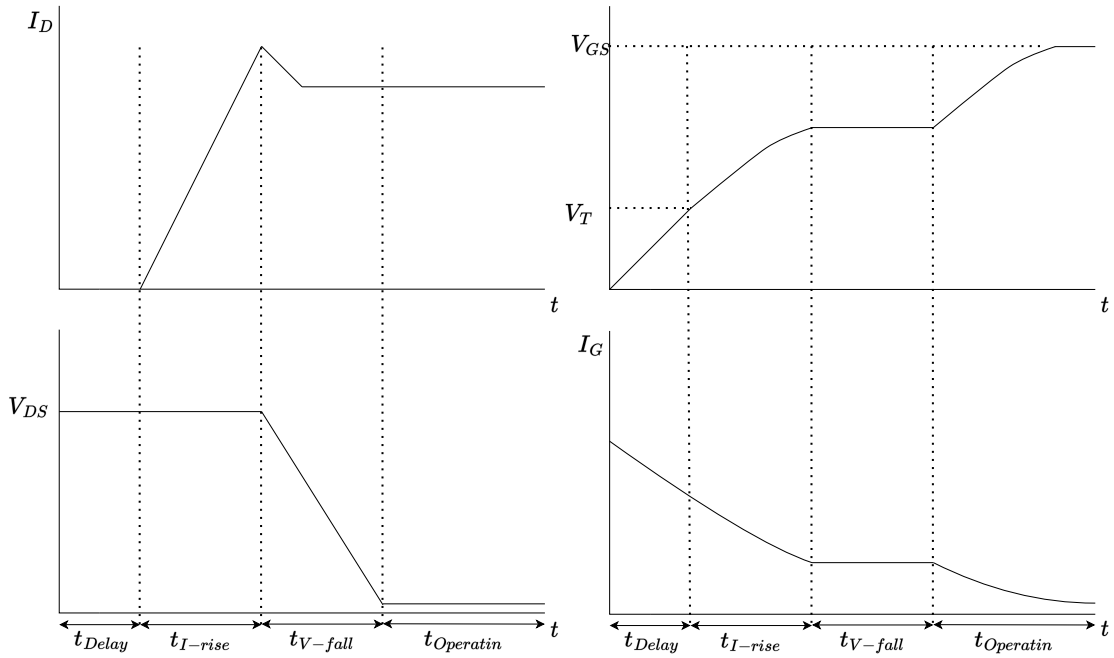


Figure 2.7: MOSFET turn on waveform.

Shown in fig. 2.8 is the IV characteristic of the MOSFET, which defines the output voltage and current at different gate voltages.

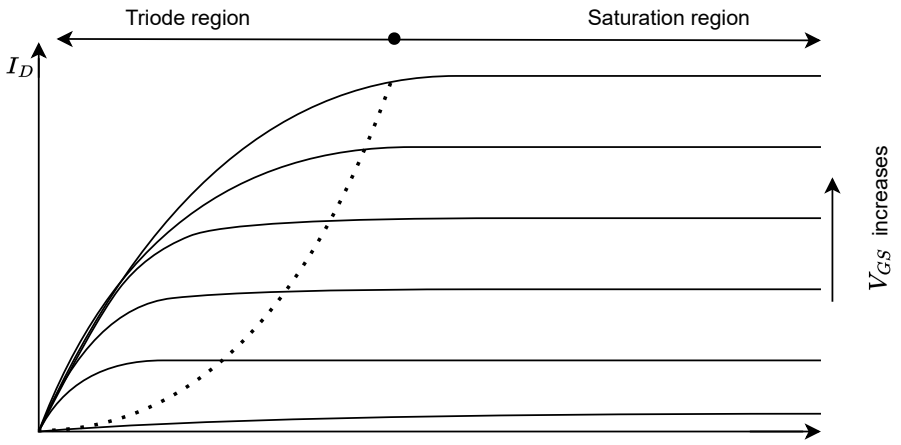


Figure 2.8: MOSFET IV caracteristic.

2.2 Double pulse test operating working principle

After the MOSFET is analyzed, the current and Voltage in the DPT stages are explained and shown in the following. First, the capacitors charge to the required voltage level. After that, the MOSFET is turned on, thereby charging the inductor as shown by the red current path in fig. 2.9. The charging of the inductor depends on the MOSFET device. When reaching the desired current, the MOSFET turns off. From this turn-off event, the losses are calculated. [24]

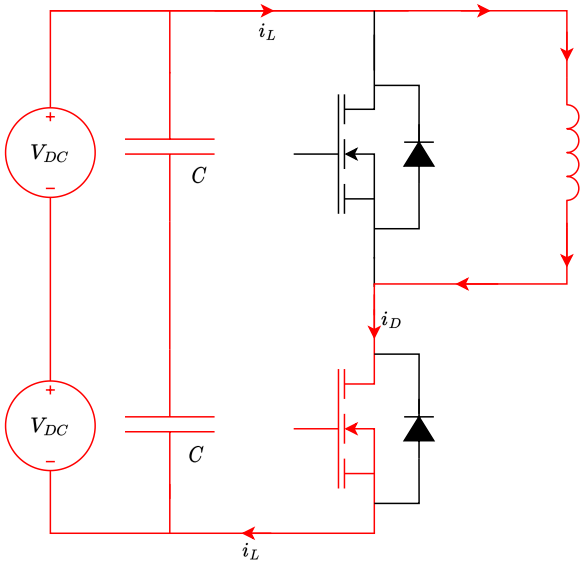


Figure 2.9: DPT current flow under first turn on.

In the second stage, the current circulates through the freewheeling diode and will reduce because of the losses in the diode and the inductor. The circulating current is indicated by the red arrows in fig. 2.10. This stage must be long enough to account for the switching time of the MOSFET and the dead time introduced by the gate driver and DSP. Time is

crucial in this stage. The longer the break lasts, the bigger the losses become, resulting in testing the MOSFET at a different current level than defined. [24]

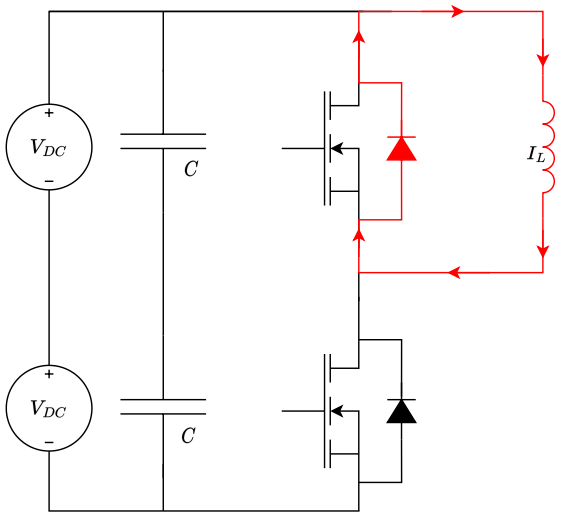


Figure 2.10: DPT current flow under freewheeling period.

In the third stage of the DPT, the current flows from the inductor through the MOSFET and back to the capacitor as shown in fig. 2.12. In this stage, the current starts at the inductor's charged current minus the current lost to losses as the defined current has been circulating through the inductor. [24]

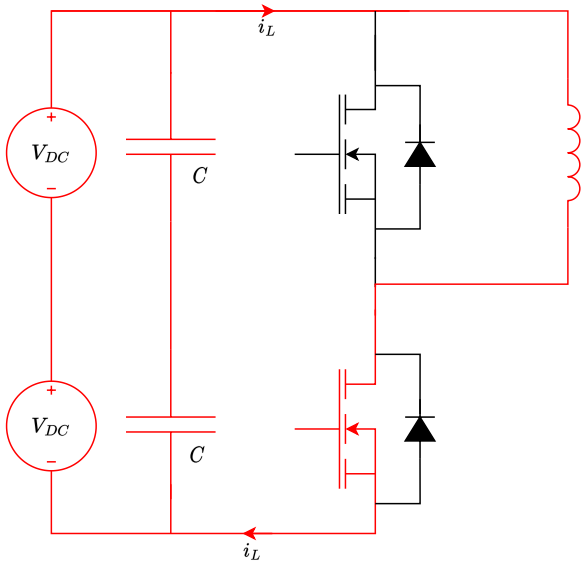


Figure 2.11: DPT current flow under second turn on.

After the last stage, the MOSFET turns off, and the energy dissipates. The voltage and current waveforms are shown in fig. 2.12.

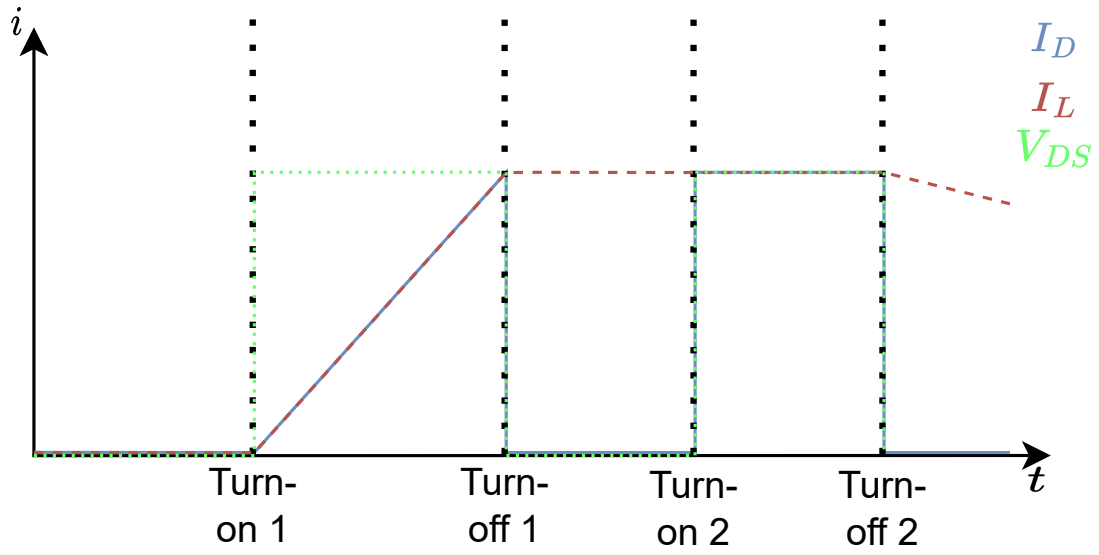


Figure 2.12: DPT current and voltage under first turn on, freewheeling period and second turn-on.

Following the analysis of the DPT, the different components of the DPT is analysed.

2.3 Voltage source

Under the operation of the DPT, the voltage source has little-to-no influence as the capacitor works as the power source. Because the DPT is in the microseconds, the voltage source can not react to the turn on and off of the MOSFET. Therefore the main part of the Voltage source is to charge the capacitor. This results in a pre-start-up time before the DPT. Because the capacitor cannot charge instantly, the time for charging the capacitor and the time the voltage source requires before the test, should be known to have the required amount of energy in the capacitor. After charging the capacitor, the DPT is executed.

2.4 Inductor sizing

The right inductor size is required to keep the MOSFET temperature consistent throughout the DPT. Using an inductor with an inductance that is too high results in exceeding the MOSFETs temperature limitation when sweeping the MOSFET at different currents. When choosing an inductor that is too small it will result in the DPT not having enough energy or dissipating too much energy in the Break operation of the DPT. The first requirement is to define the energy dissipated in the MOSFET and thereby limit the temperature rise of the MOSFET to 1°. To do this, the Heat Capacity equation eq. (12) given by [25] is used.

$$E = m \cdot c \cdot \Delta T \tag{12}$$

Considering eq. (12), the maximum on-time of the MOSFET under first turn on is calculated by its conduction loss eq. (13) given by [23].

$$E = \int_0^{t_1} V_{DS}(t) \cdot I_D(t)\, dt \tag{13}$$

As the voltage drop over V_{DS} is unknown, eq. (13) is rewritten with Ohm's law to make it dependable on the on-state resistance and the current through it; this is possible as the temperature rise of the MOSFET should be maximum 1°, to keep the measurement consistent, as increasing the temperature changes the results.

$$E = \int_0^{t_1} R_{on} \cdot I_D^2(t)\, dt \tag{14}$$

Defining I_D and t_1 is accomplished by fig. 2.13 which shows that I_D is increasing under first turn-on.

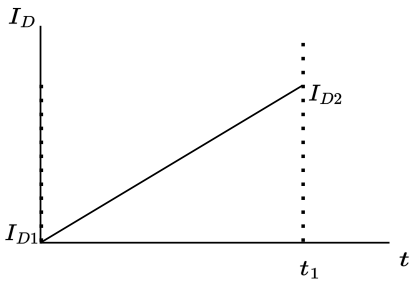


Figure 2.13: Expected I_D under first turn on.

Then eq. (15) is defined by two known points, with unknown time.

$$I_D(t) = I_{D1} - \frac{I_{D1} - I_{D2}}{t_1} t \tag{15}$$

Substituting eq. (15) into eq. (14) gives eq. (16)

$$E = \int_0^{t_1} R_{on} \cdot (I_{D1} - \frac{I_{D1} - I_{D2}}{t_1} t)^2\, dt \tag{16}$$

The integral is then solved, and eq. (17) is achieved.

$$E = R_{on} \cdot \frac{1}{3} I_{D2}^2 \cdot t_1 \tag{17}$$

Rewriting eq. (17) and eq. (12) to have the maximum on time results in eq. (18) when considering that $I_{D1} = 0$ and $I_{D2} = I_L$.

$$t_1 = \frac{m \cdot c \cdot \Delta T}{R_{on} \cdot \frac{1}{3} I_L^2} \tag{18}$$

Lastly, for calculating the inductor, its voltage equation is given in eq. (19) by [26].

$$v = L\frac{dI_L}{dt} \tag{19}$$

Considering that the inductor starts at time zero and that the inductor is not charged at the time, the equation is rewritten as:

$$v = L\frac{I_L}{t_1} \tag{20}$$

For finding the right inductor size, eq. (20) is substituted into it eq. (18), and finally, L is isolated.

$$L = \frac{m \cdot c \cdot \Delta T}{\frac{1}{3}R_{on} \cdot I_L^3} \cdot V \tag{21}$$

It is possible to calculate the inductor value considering the maximum allowed temperature change of the MOSFET. Because there are more constraints when choosing the inductor, it is required also to take them into account.
The other constraint that influences the inductor selection is the DSP. The DSP can only delay the signal for a pre-defined amount of time. If the DPT is run at different current amplitudes, the DSP must turn off the first puls when it reaches the required current.

2.5 Capacitor sizing

The capacitor must act as a fast energy source, because the power supply can only supply a limited current in the given time [8]. Therefore, it requires the capacitor to deliver all the energy in the DPT and be the correct size. If the capacitor is too small, it will run out of energy before the DPT reaches the current of the inductor. Though if it is too large, there will be problems, in the case of a fault, as a larger fault current would occur
To calculate the correct size inductor: First, the total energy in the system is required in order to calculate the inductor size.

$$E_{tot} = E_{inductor} + E_{MOSFETloss} \tag{22}$$

The total energy required is the energy required to charge the inductor and the energy lost to heat in the MOSFET. To calculate the energy in the inductor eq. (23) from[26] is used.

$$E_{inductor} = \frac{1}{2}L \cdot I^2 \tag{23}$$

The other important equation is to calculate the energy in the capacitor eq. (24).

$$E = \frac{1}{2}C \cdot V^2 \tag{24}$$

When using eq. (24) to calculate the capacitor, it would result in the capacitor total discharge, which would lower the DC bus voltage to zero; therefore eq. (24) is redefined with a maximum voltage difference eq. (25).

$$\Delta E = \frac{1}{2}C \cdot V_1^2 - \frac{1}{2}C \cdot V_2^2 \tag{25}$$

Next eq. (25) is simplified to eq. (26).

$$\Delta E = \frac{1}{2}C \cdot (V_1^2 - V_2^2) \tag{26}$$

For calculating the capacitor eqs. (17), (22), (23) and (26) are combined and finally C is isolated.

$$C = \frac{R_{on} \cdot \frac{1}{3}I_L^2 \cdot t_1 + \frac{1}{2}L \cdot I_L^2}{V_1^2 - V_2^2} \tag{27}$$

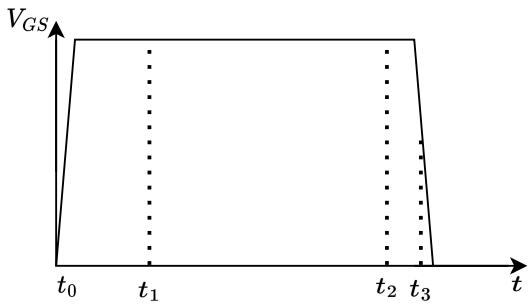
Where the voltage difference should be 20 V for the range of 100 V to 1000V, and after that can increase to 200 V and so on.

2.6 Freewheeling diode

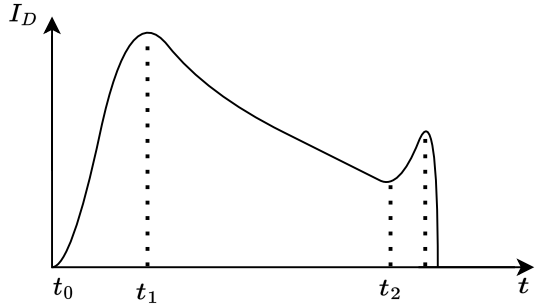
A freewheeling diode keeps the inductor's current constant under the DPT turn-off operation. If the freewheeling diode is not present, it results in voltage stress on the MOSFET when it switches from conduction to blocking; this could destroy it. Using the freewheeling diode creates a path for the current in the inductor to protect the MOSFET. [27] Through introducing the freewheeling diode, loss is introduced in the alternate part, this will result in a reduction of the current for the turn-on loss test.

2.7 Short circuit event

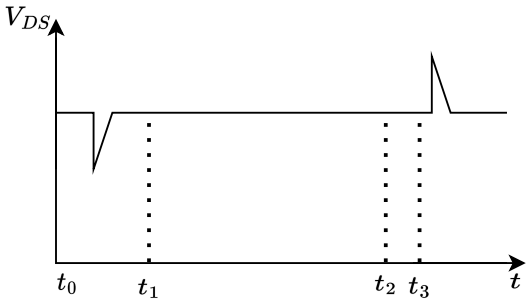
As mentioned in the introduction, three types of short circuit protection exist. Understanding short circuit protection requires looking at a short circuit event and understanding it. Shown in fig. 2.14 is an SC fault under hard switching. First, the device is off before t_0 where it turns on. The current over I_D increases when the device conducts. The device will be heating up rapidly during this increase, which could destroy it. Under this event, the voltage is stained at V_{DC} as the device's resistance increases. After I_D has reached its maximum, the current decreases because of the increased resistance and decreased channel mobility. Before the turn off of the device after t_3 and the falling off of the current to zero, there is an increase in current as the temperature of the device increases. [19], [28]



(a) Short circuit voltage over V_{GS}.



(b) Short circuit current over I_D.



(c) Short circuit voltage over V_{DS}.

Figure 2.14: Short circuit event voltage and current curves under event.

As power is voltage times current, the energy of the event is acquired by integrating from t_1 to t_3; this results in eq. (28).

$$E_C = \int_{t_1}^{t_3} V_{DS} I_D \, dt \tag{28}$$

2.8 Short circuit protection

First; to decide the right SC protection a choice is taken between the three protection schemes.

Part to compare	Series	Crowbar	Desaturation
Component between module	Yes	No	No
Redesign gate driver	No	No	Yes
Connection and disconnection	No	Yes	No
Can fail	No	Yes	Yes
Ease of implementation	Medium	Easy	Hard

Table 2: Comparison of best protection.

Table 2 argues that Parallel protection is best for this DPT as it has its ease of implementation and does not have any wire length and thereby inductance. However, the problem with using parallel protection is that it is required to use Insulated gate bipolar transistor(IGBT) or Thyristors that can deal with the short circuit current higher than the nominal current,

thereby making the module more expensive. As mentioned by [16], thyristors are used for their reliability and longer lifetime when typically developing crowbar protection. The switching time and the current rise time are the drawbacks when using thyristors. There are two possibilities to reduce the thyristor switching time: reduce the detection time of the fault or reduce the time it takes for the thyristor to switch, as reducing the detection time requires in-depth knowledge about the circuit parameters every time. The IGBT is used as it reduces the switching time, since this is not dependent on the other circuit parameters. As mentioned by [16], using an IGBT will result in the fault current falling to zero right after the IGBT reaches its on-state, and thereby the fault energy is equal to the power from the fault until the switching of the IGBT.

3 Double pulse test setup

A DPT is implemented in the laboratory to test the theories mentioned in section 2.

3.1 Digital signal processor

First, the control, to switch the MOSFET is implemented. The tool chosen to control the MOSFET is a microcontroller. Because the microcontroller works in the discrete domain, it has a fixed time interval for charging the inductor, and it is required to know the time interval the microcontroller is running at to design the right size inductor later. For choosing the right microcontroller, there are several companies to choose from, like Atmel, Texas Instruments, Intel, and many more. As the DPT only requires the microcontroller to control the MOSFETs, only an output port is required, so it is possible to turn it on and off. The other important factor for the microcontroller is the processing time, so it is possible to define the on-time and off-time of the device, and the delay. [29] Shown on fig. 3.1 is the microcontroller to control the MOSFET; it is a digital signal processor (DSP) from Texas Instruments. The DSP is the TMS320F28379D [30] which has the following specifications:

- 32-bit CPU
- 512KB (256KW) or 1MB (512KW) of flash
- Two internal zero-pin 10-MHz oscillators
- 24 PWM channels with enhanced features

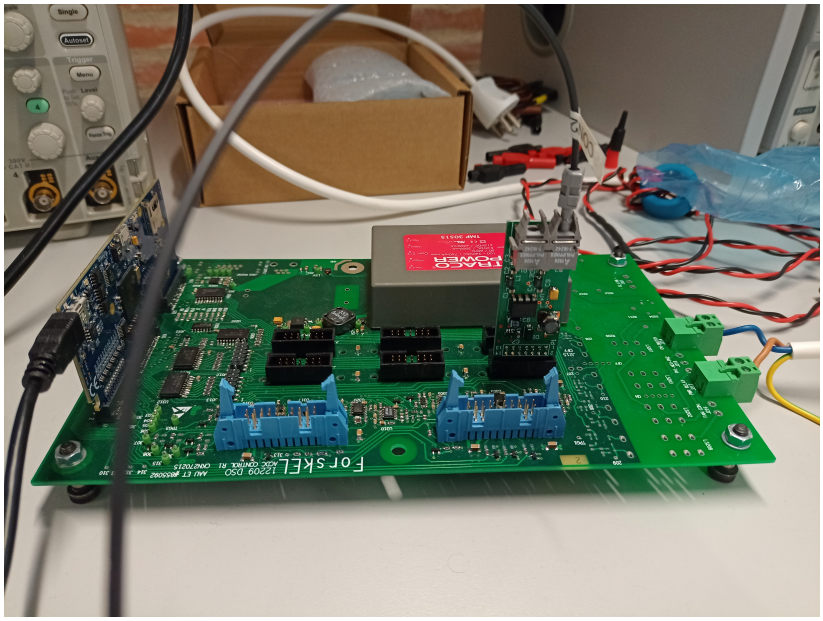


Figure 3.1: Microcontroller board do provide electrical isolation.

The DSP is coded in Code composer studio to use one output channel. This output channel connects to the MOSFET driver through the board shown in fig. 3.1. The board is for controlling six MOSFETs as the DPT only uses one MOSFET while the rest is kept empty. The

figure also shows an optocoupler that transforms the signal from electrical to light, thereby providing electrical isolation.

3.2 MOSFET gate driver

A gate driver is required to switch the MOSFET with a DSP, as the DSP cannot deliver the voltage and current to switch the MOSFET. The gate driver shown in fig. 3.2 was developed and implemented in [31].

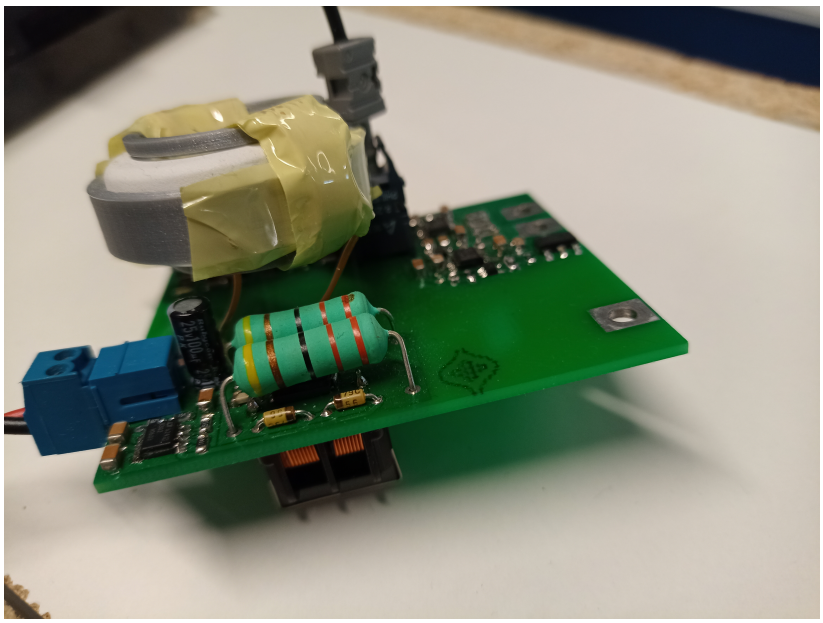


Figure 3.2: MOSFET gate driver.

This driver is developed for the range above 1000V but can also be used below that range as long as the gate voltages match the MOSFETs gate voltage requirements. The gate driver connects via the gate and the source terminal.

3.3 Inductor design

For designing the inductor, limiting factors are taken into account. These limiting factors are maximum energy through the MOSFET and sufficient ampere per seconds rating for the inductor, so the microcontroller can turn off at the right time. For the first constraint, eq. (21) was used to calculate the maximum energy value the inductor may have from the limitations mentioned in section 1.1.3. To use the equation table 3 is used to show the values inserted for the variables.
By using eq. (21) and table 3 the value of the inductor is calculated.

$$0.0014H = \frac{0.10533g \cdot 0.69\frac{J}{g \cdot K} \cdot 1K}{\frac{1}{3}0.011\Omega \cdot 200A^3} \cdot 600V$$

The inductor is calculated to 0.0014 H. If the inductor is not larger than the calculated

Name	Variable	Value
Maximum voltage	V	600V
Maximum current	I_L	200A
On-state resistance	R_{on}	0.011Ω
Maximum temperature rise	ΔT	1K
Specific heat	c	0.69 $\frac{J}{g \cdot K}$
Mass	m	0.10533g
Time to reach maximum current	t_1	$20e^6 s$

Table 3: Values to calculate inductor.

value, it will not heat the device more than 1 degree when charged to the maximum current. After that, to design is influenced by the microcontroller that could only send a switching signal at one-microsecond intervals. Therefore the amps per second should be 10 A/s. Using this, it is possible to accurately calculate the inductor value by using eq. (19).

$$60 \cdot 10^{-6} H = 600V \cdot \frac{20 \cdot 10^{-6} s}{200A}$$

This calculates the final inductor value to $60 \cdot 10^{-6}$H. With the inductor calculated, it is required to build the physical inductor. For the physical inductor, it is chosen to use an air core inductor as it is possible to design one in time as well as there are no problems with the saturation of the core.
Designing the physical inductor [32] is used. The equation uses the width, diameter of the coil, number of turns as well as permeability of air to calculate the inductor size.

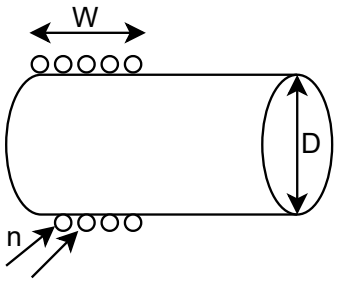


Figure 3.3: Inductor design [32].

Shown in fig. 3.3 are the specifications of the parameters used to arive at eq. (29).

$$L = \frac{\mu_0 A_c N^2}{W(1 + 0.9(D/2W)} + \frac{\mu_0 N D}{3} \tag{29}$$

where:

$$A_c = \frac{\pi D}{4} \tag{30}$$

With these equations, the physical inductor is designed and implemented.

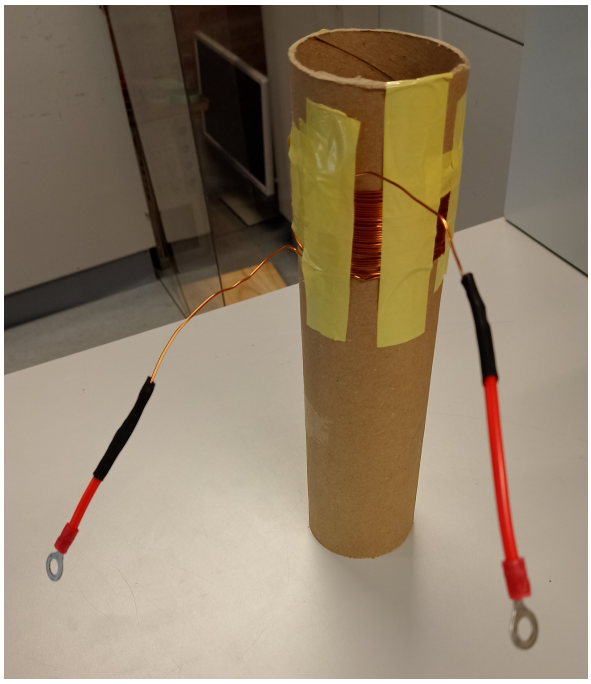


Figure 3.4: The implemented low voltage inductor.

Figure 3.4 shows the designed and implemented inductor. The inductor is made of a paper roll where an insulated copper wire is spun around, and then fixed with electrical tape.

Dimension	Value	Unit
Inductor value	60	µH
Width	50	mm
Diameter	60	mm
Number of turns	36	

Table 4: Inductor parameters.

To verify if the inductor is 60μH, the parasitic circuit model of the inductor shown in fig. 3.5 is used [33], [34].

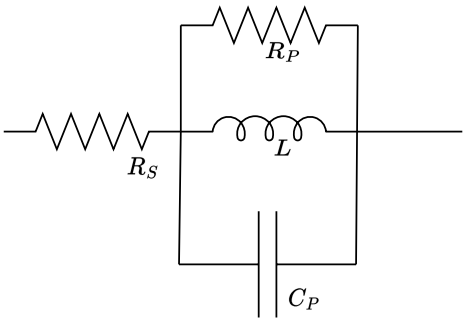


Figure 3.5: inductor equivalent circuit [33].

By using the parasitic circuit model, it is possible to calculate the impedance with eq. (31), derived from the parasitic equivalent circuit by finding the impedance of the total circuit;

for the inductor and capacitor, their reactance model is used.

$$|Z| = R_s + \frac{1j \cdot \omega \cdot L \cdot R_p}{1j \cdot \omega \cdot L + (1 - \omega^2 \cdot L \cdot Cp) \cdot Rp} \tag{31}$$

The measured impedance and the calculated inductance are shown in fig. 3.6.

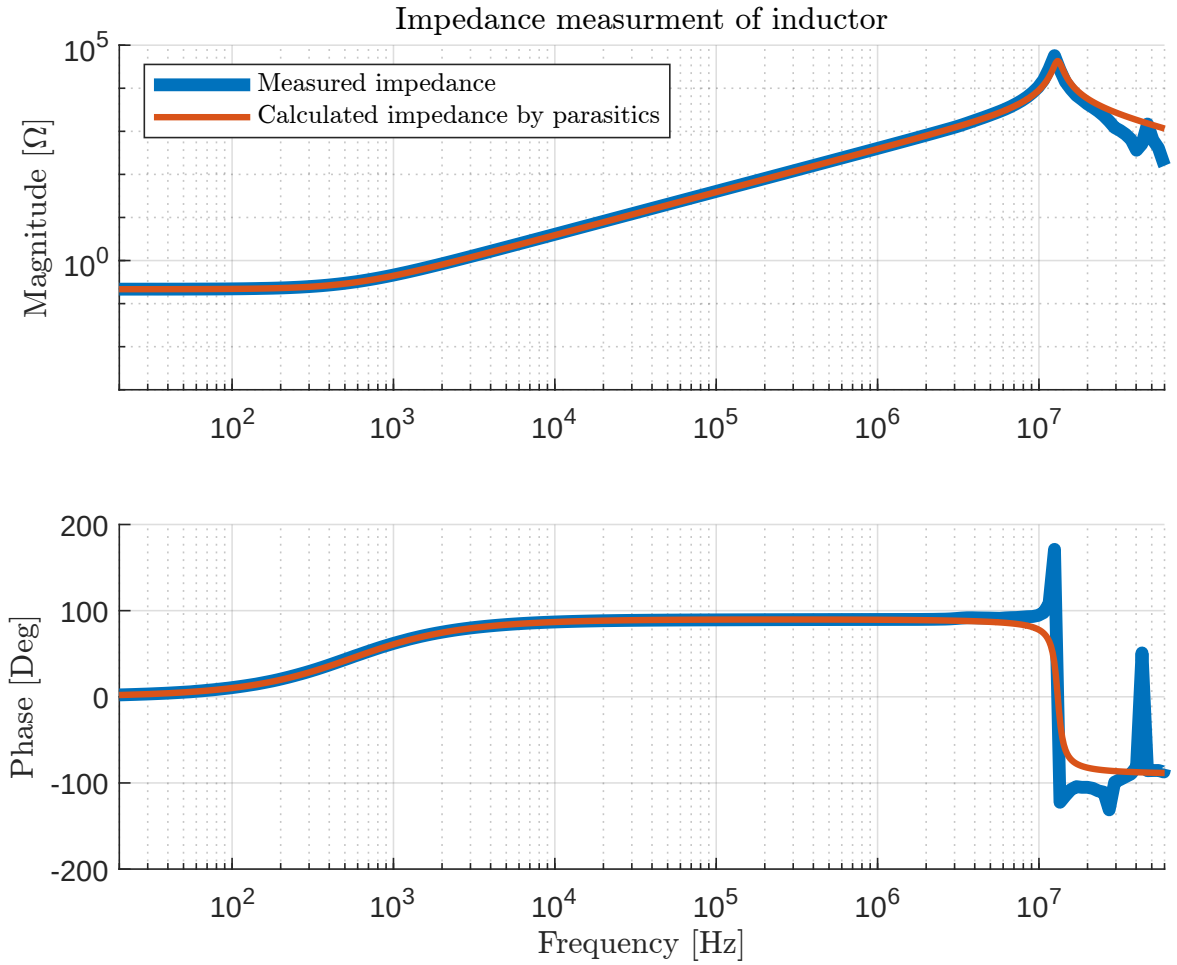


Figure 3.6: inductor impedance and phase.

To find the values for the calculated impedance, eq. (31) is used. The values are changed until both curves match and thereby getting the parasitic values when both curves match. The final parasitic values are presented in table 5.

Parasitc component	Value
Inductance	$61.7\mu H$
Parallel parasitic capacitance	2.4 pF
Series parasitic resistance	216mΩ
Parallel parasitic resistance	43kΩ

Table 5: Inductor electrical parameters.

When comparing the measured impedance with the calculated, the impedance matches until 20 MHz. After that, the measuring requires a better impedance analyzer. To get the

measured and the calculated impedance to match it, a higher order system is required than the second order.

3.4 Capacitor design

From the inductor, the capacitor is designed. First, eq. (27) is used to calculate the capacitor to 50 µF.

$$50 \cdot 10^{-6} = \frac{0.011\Omega \cdot \frac{1}{3}200A^2 \cdot 20 \cdot 10^{-6} + \frac{1}{2}60 \cdot 10^{-6} \cdot 200^2}{600V^2 - 580V^2} \tag{32}$$

Shown in fig. 3.7 is the capacitor bank that is used.

Figure 3.7: Capacitor bank.

The capacitor comprises four capacitors, two 50 µF in series and then two in parallel to make up the capacitor as shown in fig. 3.8. After that, the capacitors are connected to three busbars.

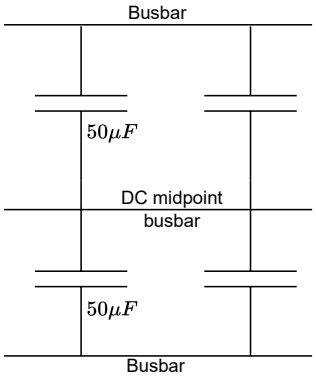


Figure 3.8: Capacitor schematic.

To verify if the capacitor is 50μF, the parasitic circuit model of the capacitor shown is fig. 3.9 [33].

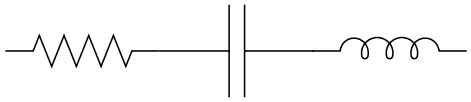


Figure 3.9: Capacitor with parasitic components [35].

By using the parasitic circuit model, it is possible to calculate the impedance with eq. (33), derived from the parasitic equivalent circuit by finding the impedance of the total circuit; for the inductor and capacitor, their reactance model is used.

$$|Z| = R_s p + 1j\omega \cdot L_s + \frac{1}{1j\omega \cdot C} \tag{33}$$

The result of the impedance measurement and the calculated impedance is shown in fig. 3.10.

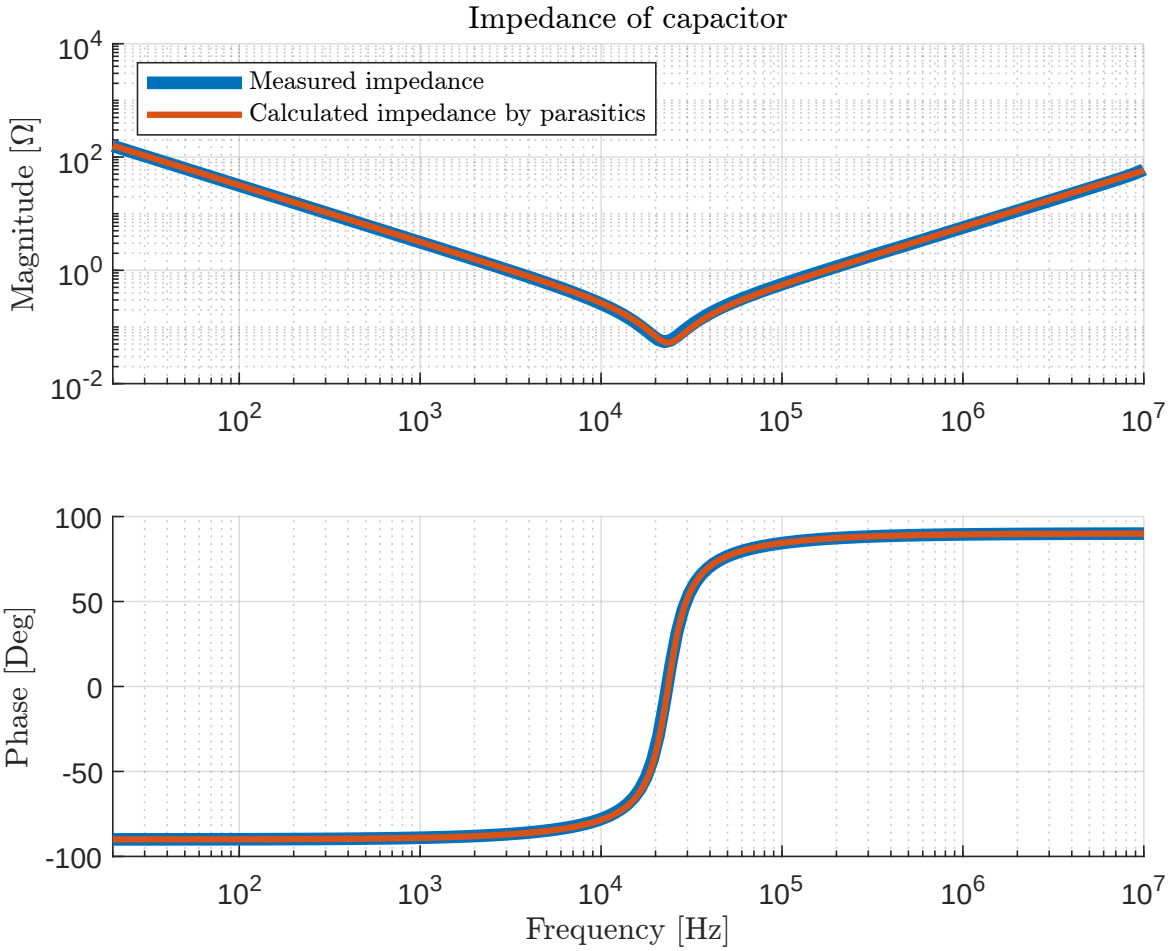


Figure 3.10: Capacitor impedance and phase.

To find the values for the calculated impedance, eq. (33) is used. The values are changed until both curves match and thereby getting the parasitic values when both curves match. The final parasitic values are presented in table 6.

Component	Value
Capacitance	$50\mu F$
Series parasitic resistance	$57m\Omega$
Series parasitic inductance	920 nH

Table 6: Capacitor parasitic component.

3.5 Measuring instruments

For measuring V_{GS}, V_{DS}, and I_D, an oscilloscope is required to log and measure the response of the system. For this, it is chosen to use the Tektronix dpo 2014 shown in fig. 3.11.

Figure 3.11: Oscilloscope used for measuring [36].

Parameters	Value
Bandwith	100 MHz
Channels	4
Sample rates	1 GS/s
Record length	1 M points
Capture rate	5,000 waveforms/s

Table 7: Tektronix dpo 2014 stats [36].

From the datasheet [36], the specifications of the oscilloscope is given:
When choosing the oscilloscope, it is crucial to consider the limitation of the measuring capability. Choosing an oscilloscope with low bandwidth would result in the wrong measurements due to the 3DB limit [37].

3.5.1 Current probe

To measure the I_D current. The Pearson current monitor model 2878 is used.

Figure 3.12: Current probe used to measure I_D [38].

Parameters	Value
Sensitivity	0.1 V/A
Output resistance	50 Ω
Maximum peak current	$400A$
Maximum rms current	$10\ A$
Useable rise time	$5\ ns$
Current time product	$4\ mAs$
Low Bandwidth	$30\ Hz$
High Bandwidth	$70\ MHz$
I/f figure	$0.025\ A/Hz$

Table 8: Pearson current monitor model 2878 stats [38].

The sensor works by measuring the magnetic field in the wire also called the hall effect [39]. Another essential part to consider is the current time product. The current time product limits the measuring capacities of the current sensor. If the current time product of the signal is over the specified current time product, another sensor should be chosen.

3.5.2 Passive voltage probe

For Measuring the V_{GS} voltage, a differential voltage probe, as shown in fig. 3.13 is used.

Figure 3.13: passive voltage probe used to measure V_{GS} [40].

Parameters	Value
Bandwidth	50 MHz
Rise time	7 ns
Input resistance	10 MΩ
Input capacitance	12 pF
Propagation delay	6.1 ns
Maximum input voltage	300 VRMS

Table 9: Passive voltage probe parameters [40].

The passive voltage probe has the required specifications for this measurement as the V_{GS} voltage is between -5 and 20 volts, table 9 shows the specifications. There it is shown that the bandwidth is 50 MHz which satisfies the 3 DB criteria mentioned before; also, the voltage rating of 300 V is not exceeded.

3.5.3 Differential voltage probe

A differential voltage probe is required to measure the V_{DS} Voltage. The differential voltage

Figure 3.14: Differential voltage probe used to measure V_{DS}.

Parameters	Value
Bandwidth	25 MHz
Rise time	14 ns
Input resistance	8 MΩ
Input capacitance	3.5 pF
Propagation delay	6.1 ns
Maximum input voltage	1300 VRMS

Table 10: Differential voltage probe parameters [41].

probe has the required specifications for this measurement as the V_{DS} voltage is between 0 and 600 volts, table 10 shows the specifications. There it is shown that the bandwidth is 25 MHz which satisfies the 3 DB criteria mentioned before; also, the maximum voltage range is not exceeded.

3.6 MOSFET module

The DPT requires a MOSFET to test. The BSM180D12P2E002 MOSFET by Rhom semiconductors is the right choice, because it is in the discrete package and is a half-bridge which makes it possible to use the second MOSFET body diode as the freewheeling diode and it has the voltage requirements as shown in table 11.

Figure 3.15: MOSFET module.

Parameter	Value
Drain source voltage	1200kV
Gate-source voltage+	20V
Gate-source voltage-	-6V
Drain current	200A

Table 11: MOSFET specifications [42].

To understand the MOSFET's structure, the module's circuit diagram is shown in fig. 3.16.

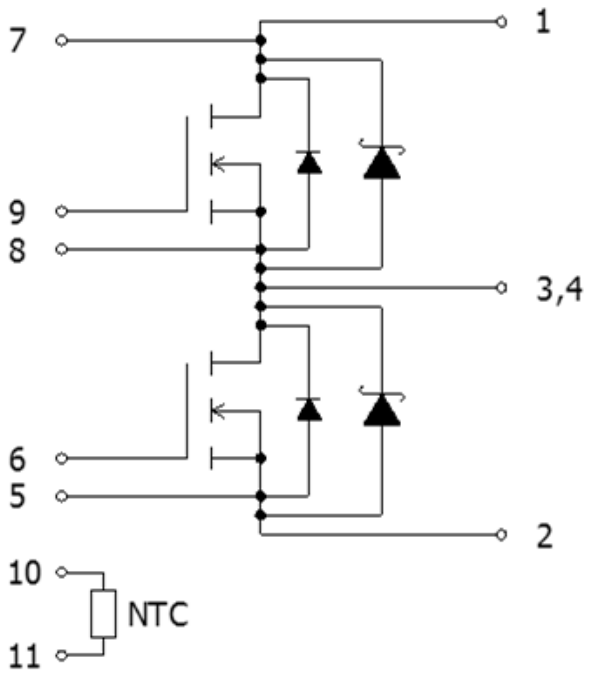


Figure 3.16: MOSFET module circuit diagram [42].

When using the module, the low-side MOSFET is measured. The inductor is connected over terminals 1 and 3, and the capacitor is connected over 1 and 2. Lastly, to control the MOSFETs, the high side MOSFET is shorted between 9 and 8 to reduce the risk of an accidental turn-on, then the gate driver is connected over 6 and 5 where 6 is the gate and 5 the drain.

3.7 Experimental setup

Combining each part of the design, measurement and control, results in the final setup are shown in fig. 3.17. On the left side is the MOSFET With the inductor and measuring equipment while on the right side is the inductor that is shorted.

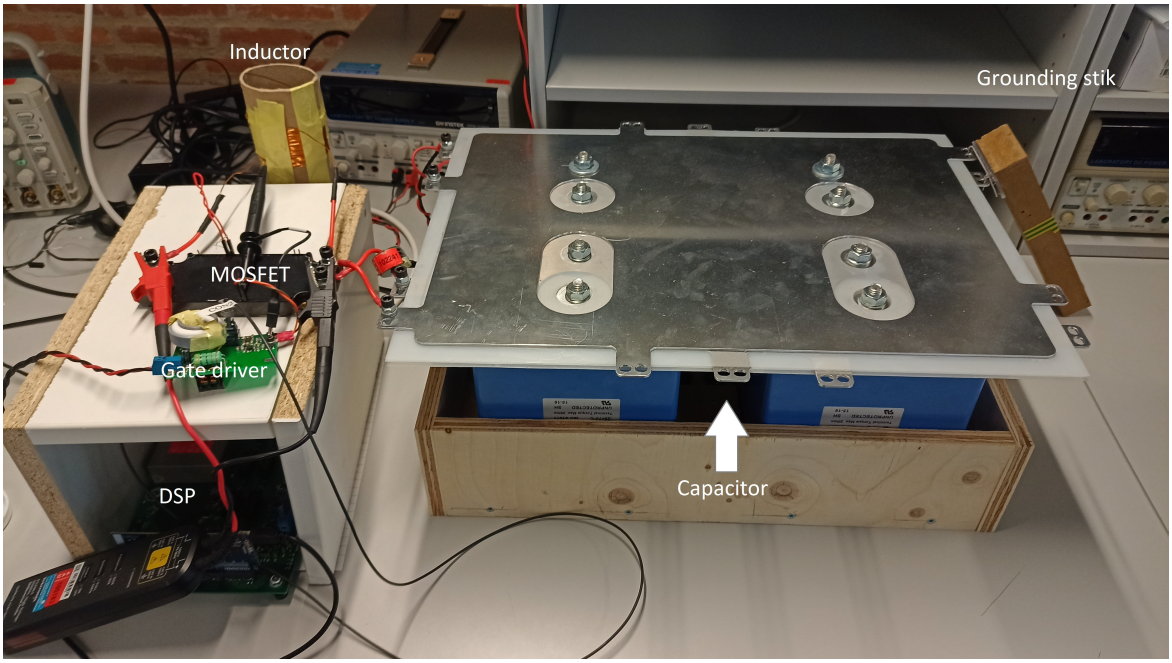


Figure 3.17: Completed DPT setup.

Executing a DPT requires four steps. First, remove the grounding stick from the conductor. Second, putting a protective cover over the DPT setup protects it against accidental touch by covering it with a Plexiglas cover, making it safe to operate. Third, the voltage turns on to the chosen level. Finally, for starting a DPT, a computer is connected to the microcontroller to control it via the coding environment's debug mode. There the time length of the first pulse of the DPT is changed, corresponding to the charging of the inductor. Then a signal switches the MOSFET with the defined setup, and the oscilloscope measures the signal. After that, the data is saved on a portable data storage device and exported to MATLAB for calculating the switching losses.
The DPT is run at 100V, 200V, 300V, 400V, 500V, and 600V; for each voltage, the inductor is charged from 20A to 200A, increasing with 20A per step. Lastly, the test testing for the different voltages repeats with 10, 20, and 30-ohm gate resistance. Through this, switching loss extraction under different conditions is possible.

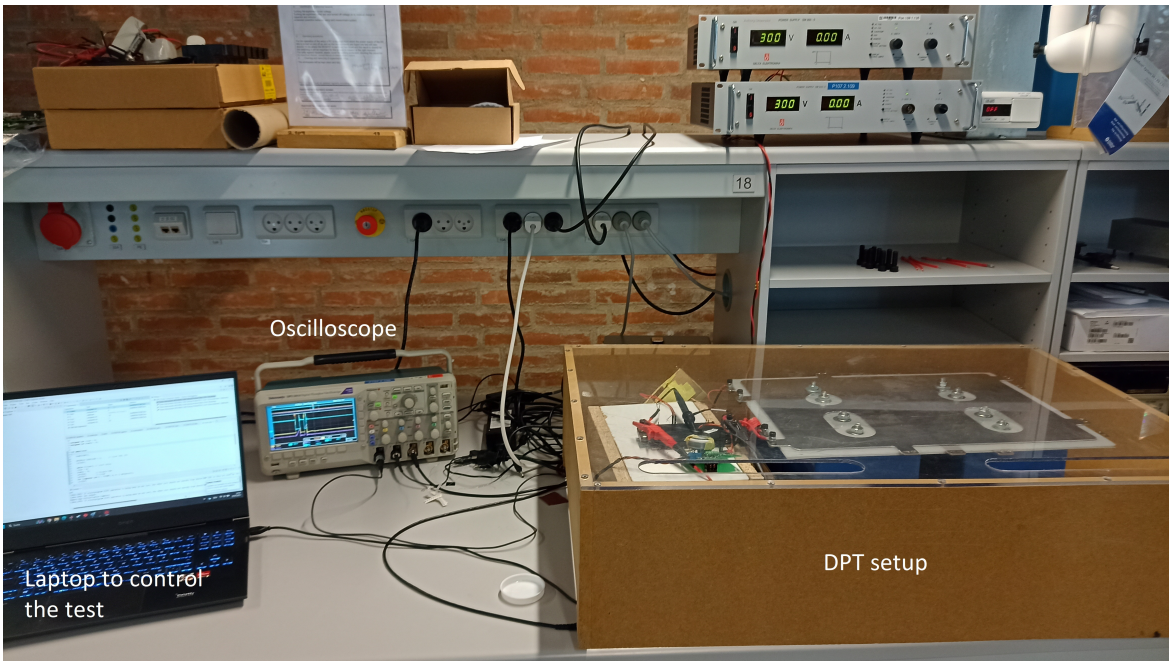


Figure 3.18: Complete DPT setup with measuring and computer.

3.8 Testing of DPT setup

After the DSP implementation, a test shows if it functioning as expected.

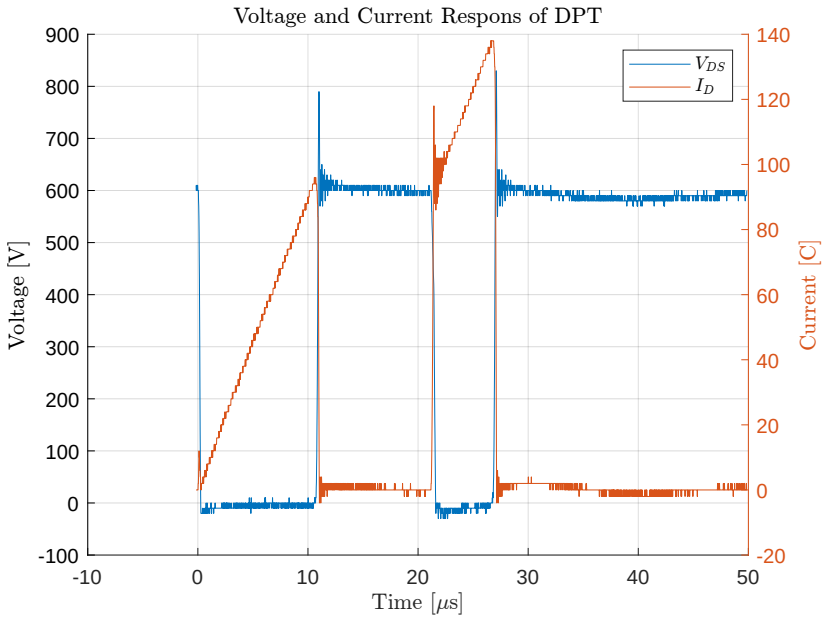
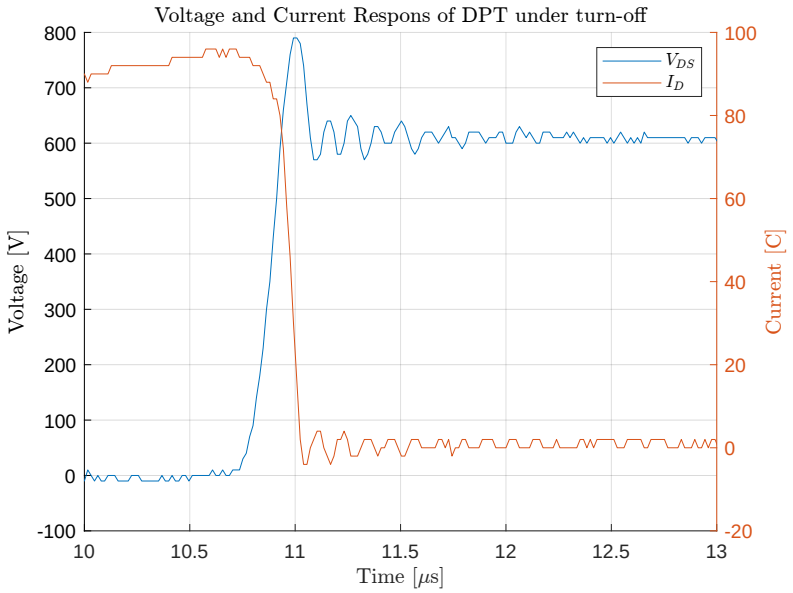


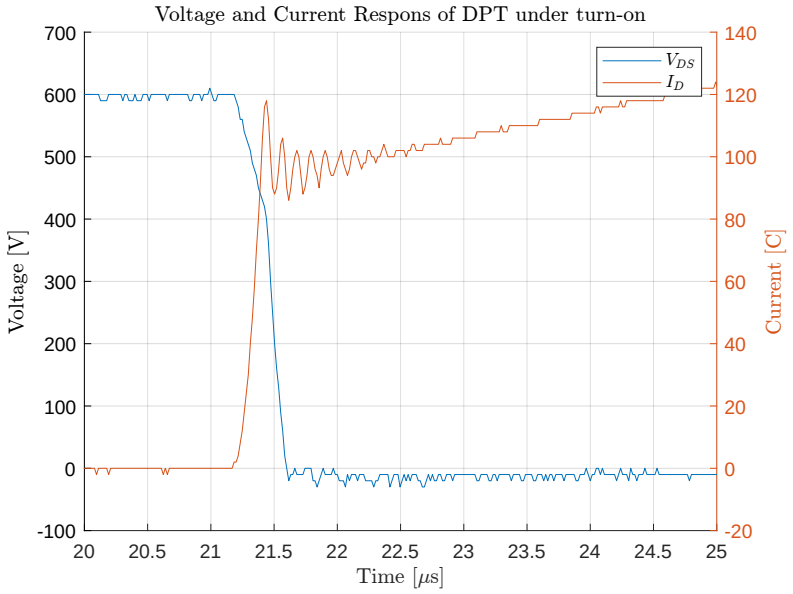
Figure 3.19: Current and voltage response of DPT laboratory test.

Shown on fig. 3.19 is a full DPT. It shows that the first puls are around 10 μs, which is around the time required to achieve a current of 100 A. Then there is a break until the transient stop, and the second turn-on starts after 10μs. lastly, it turns on and then turns off after 5μs From the DPT, a closer view is taken at the turn-on and the turn-off, which is

shown in fig. 3.20.



(a) Turn-off event of MOSFET.



(b) Turn-on event of MOSFET.

Figure 3.20: Turn on and turn off event of MOSFET.

Shown in the switching events is that oscillations arrive from the inductances in the system and the device's switching. Next, it shows the theory matches with the shown waveform where the current starts rising first, and then the voltage starts falling, as in theory.

4 Double pulse test simulation

After implementing the DPT in the laboratory, the DPT is simulated to show the DPT modeling. LTspice is the choice to simulate the circuit because it can simulate the real-world behavior of different components.

4.1 Ideal double pulse test

First, an ideal simulation is developed to test the standard idea of a DPT. Figure 4.1 shows the ideal simulation of the system; it includes the power supply, capacitors inductor, MOSFET, as well as a power supply to switch the MOSFET.

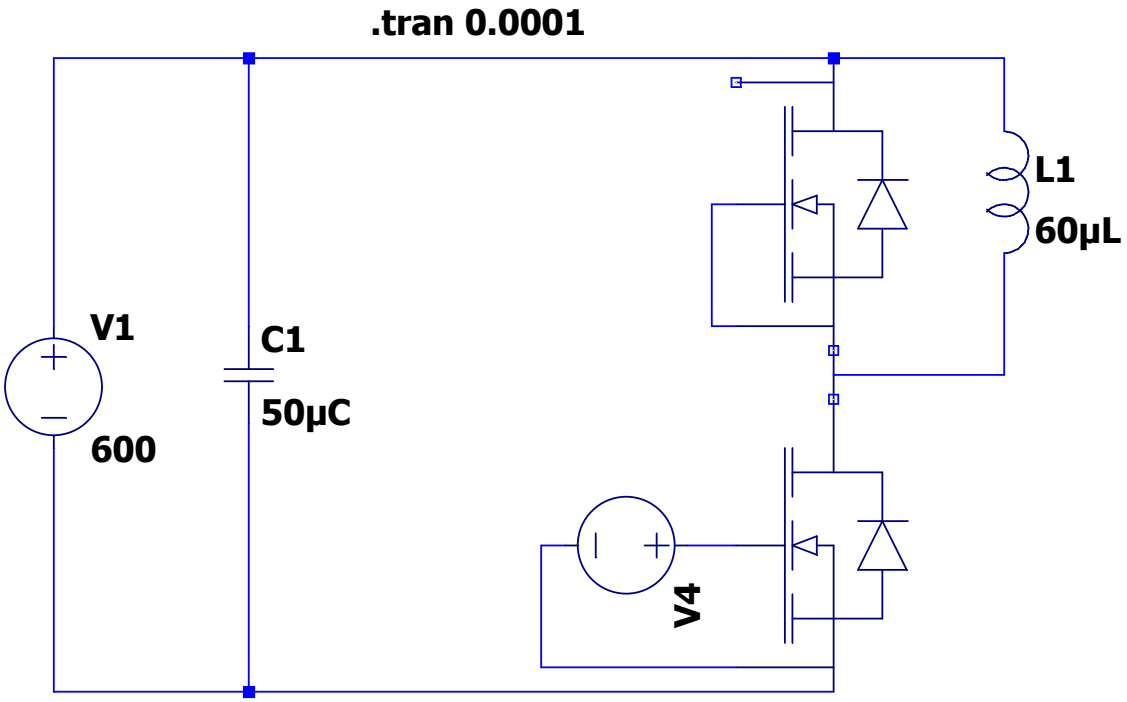


Figure 4.1: Simulation with the basic DPT test setup.

The simulation switching loss requires the specific model of the BSM180D12P2E002 MOSFET. Because Rohm supplies the MOSFET spice model, it is as simple as importing it into LTspice and connecting the terminals as required. To optimize the simulation, sweeping the different currents for one voltage level is automated using the STEP function of LTspice. After a simulation test, the results are saved in a .txt file for MatLab to calculate the losses.

4.2 Parasitic inductance's and non-ideal components double pulse test

A second simulation is made with the parasitic components of the inductor, capacitor, and wires to simulate a DPT as close as possible to real-world situations. This simulation is

then used to compare the simulation and real-world while preparing for the Short circuit protection simulation, as it should be as close to the real world as possible.

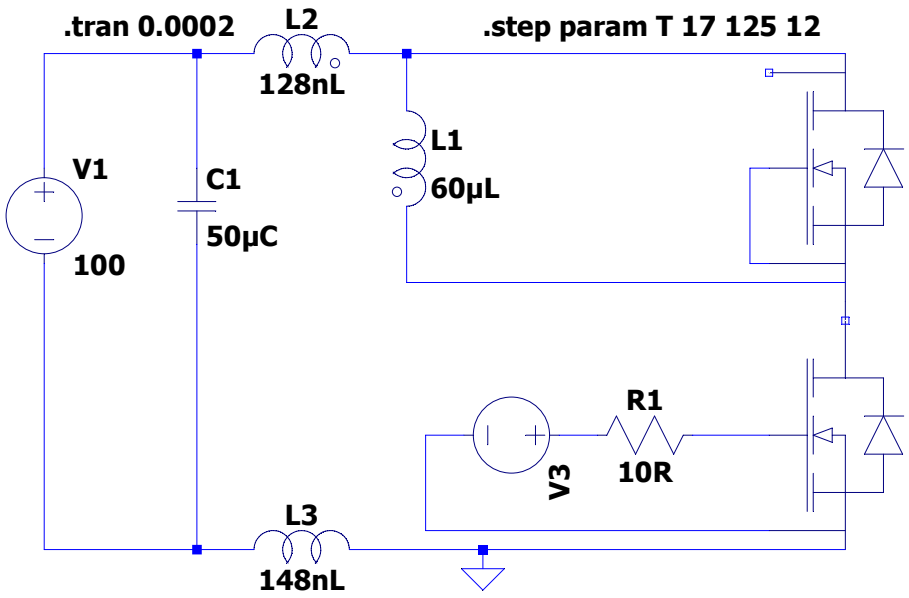


Figure 4.2: Simulation with the non-ideal components and parasitic components.

When comparing the non-ideal simulation to the ideal simulation, the difference is that inductors L2 and L3 simulate the wires connecting the MOSFET to the capacitor, and the simulation includes the parasitic of the inductor and capacitor from the impedance measurement.

5 Results

This section presents the results of the ideal simulation, non-ideal simulation, and Laboratory test.

5.1 Switching loss calculation

For calculating the switching losses, the Voltage over V_{DS} and V_{GS} are measured. While measuring the voltage, the current over I_D is also measured. Figure 5.1 shows these measurements.

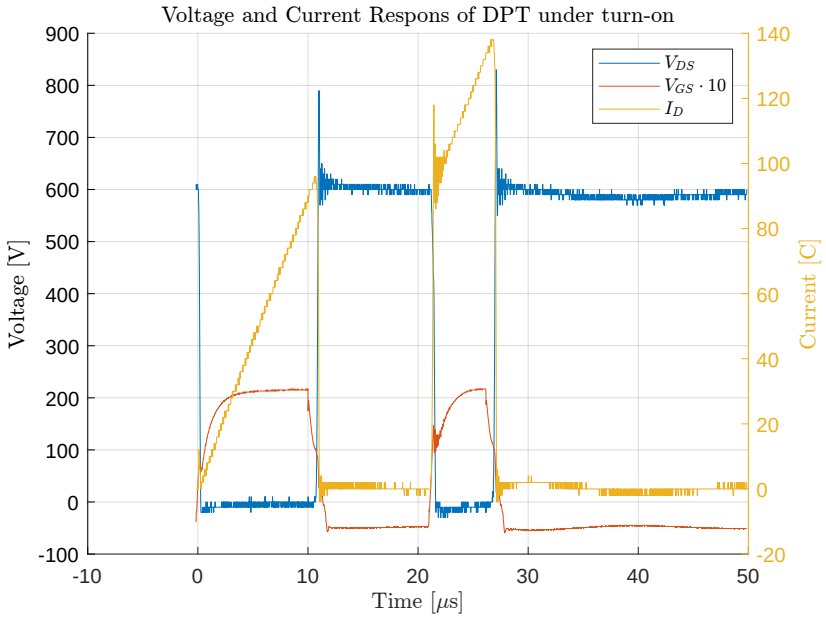


Figure 5.1: Representation of measured current and voltage.

The first step in calculating the switching losses, is calculating the power by multiplying the voltage and the current, resulting in fig. 5.2. The figure shows four power peaks where each corresponds to a switching event. It uses the second peak for calculating the turn-off switching losses, and for calculating the turn-on losses it uses the third peak.

After calculating the power in MatLab, it must calculate the energy by integrating the turn-off and turn-on peaks separately. The power is integrated by finding the start and end of the power peak. Therefore, the power peaks split into turn-on and turn-off. Then the start and the end of the switching event are defined; MatLab defines the on and off events by real-world time, thereby giving a rough estimate of the switching event. Then to enhance accuracy, it is decided to start the integration from zero, before the power peak, until six zero crossing are reached, corresponding to three transients after the power peak. MatLab then calculates the energy once the limits are defined by using cumtrapz.

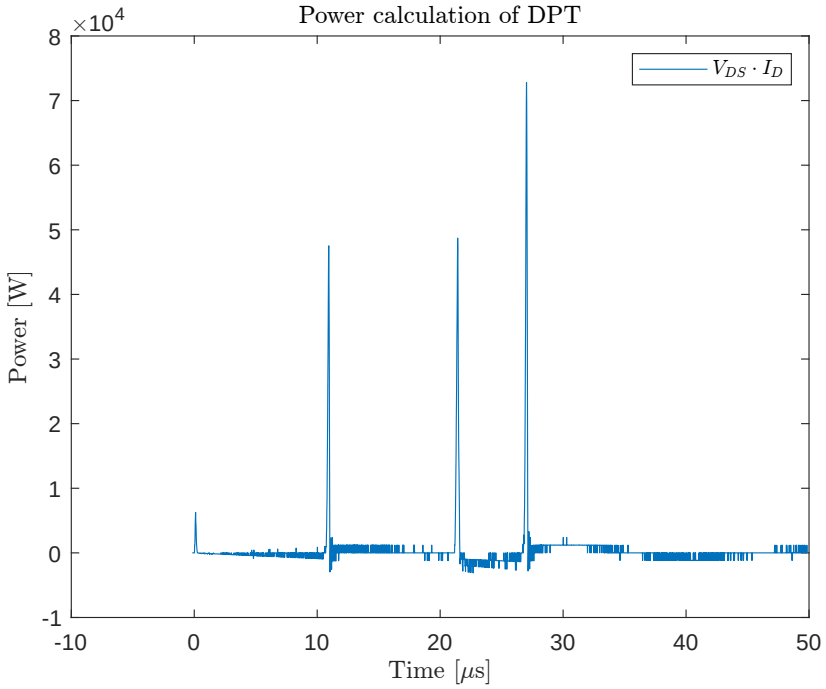


Figure 5.2: Representation of Power calculated in DPT.

Shown in fig. 5.3 is the turn off switching event and the part of the switching event that is to be integrated.

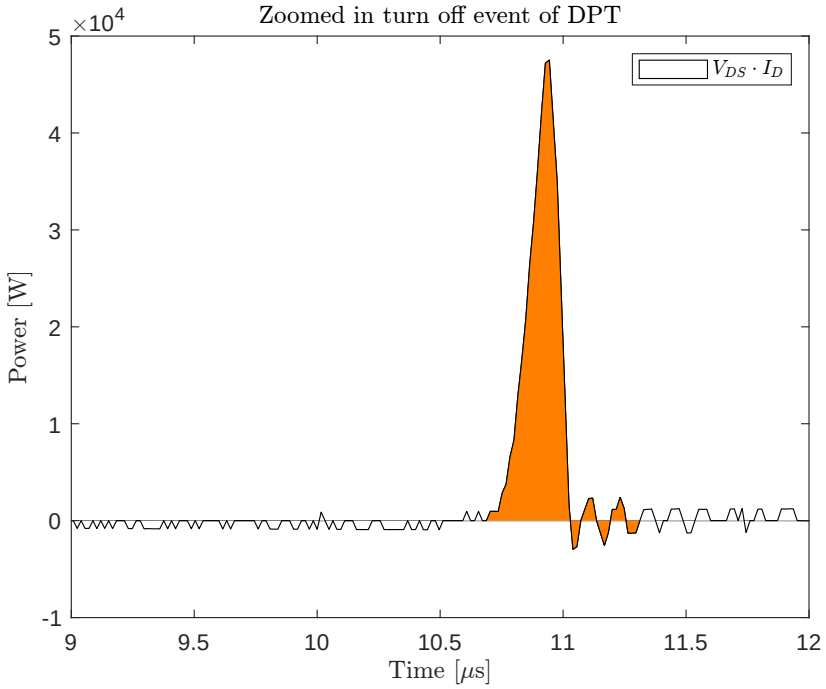


Figure 5.3: Zoomed in look at turn-off switching event.

As mentioned before, using the MatLab cumtrapz function can integrate the power and get the energy shown in fig. 5.4.

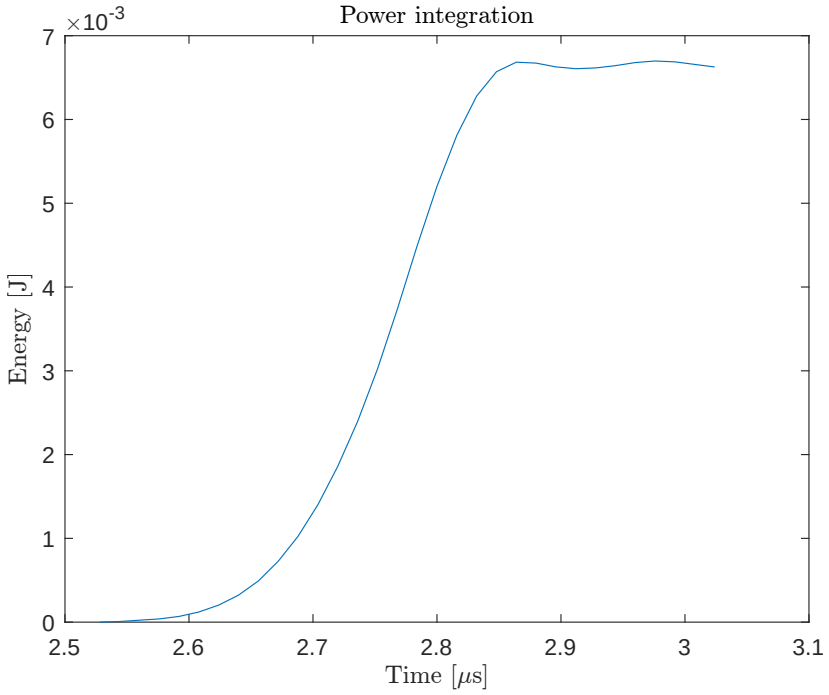
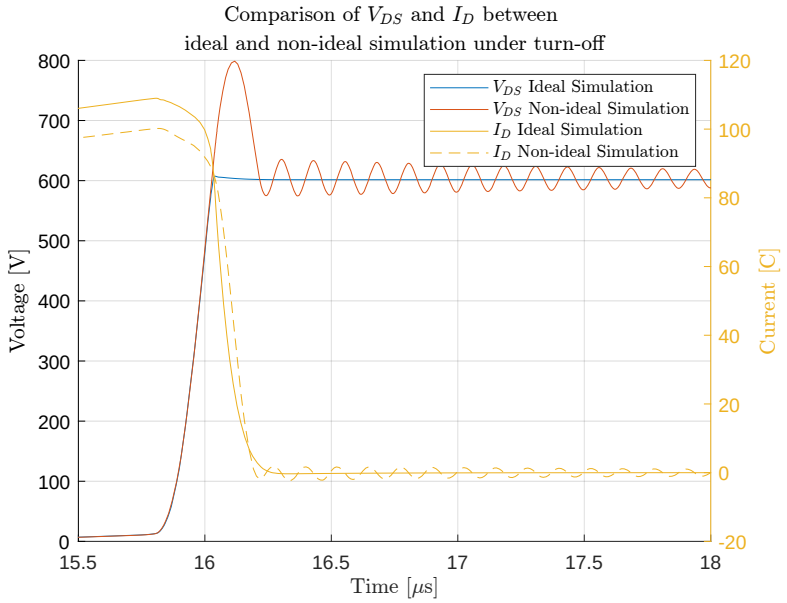


Figure 5.4: Integrating of the power calculation.

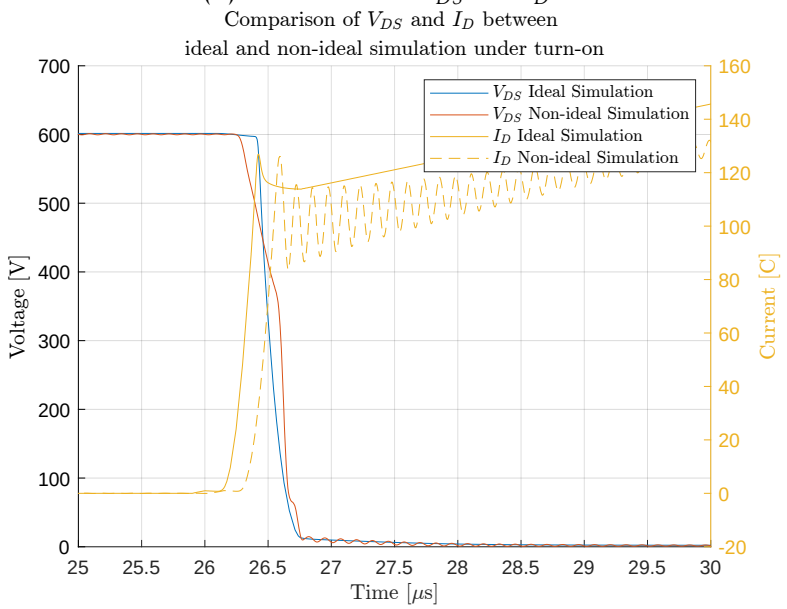
After the power integration, the last value of the integration is the energy switching loss.

5.2 Comparison between simulation and real-world at the same gate resistance

First, the simulations and laboratory results are compared to show that simulation matches the implemented DPT.
Figure 5.5a shows the comparison of V_{DS} and I_D between the ideal simulation and the non-ideal simulation. The figure clearly shows no transients on V_{DS} because there are no parasitic inductances. Also, I_D is lower in the non-ideal simulation due to the parasitic resistance in the DPT. Then, it shows that V_{DS} and I_D have the same rise/fall time for the turn-off event.
Considering the turn-on event shown in fig. 5.5b, it is shown that there is a difference in the V_{DS} between the simulations this is because of the inductors parasitic components. The other difference is on I_D, where the current is lower due to the lower current in the turn-off event and the parasitic resistances in the non-ideal simulation.
Figure 5.5b also shows the current spike on I_D in the ideal and non-ideal simulation, though, in the non-ideal simulation, the current spike is not as predominant because of the transient oscillations because of the wire parasitics.



(a) Turn-off event V_{DS} and I_D.

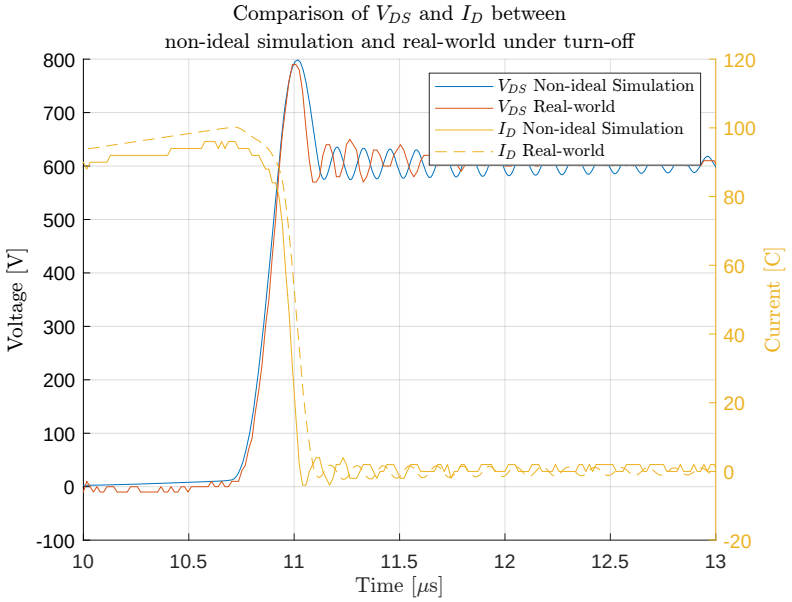


(b) Turn-on event V_{DS} and I_D.

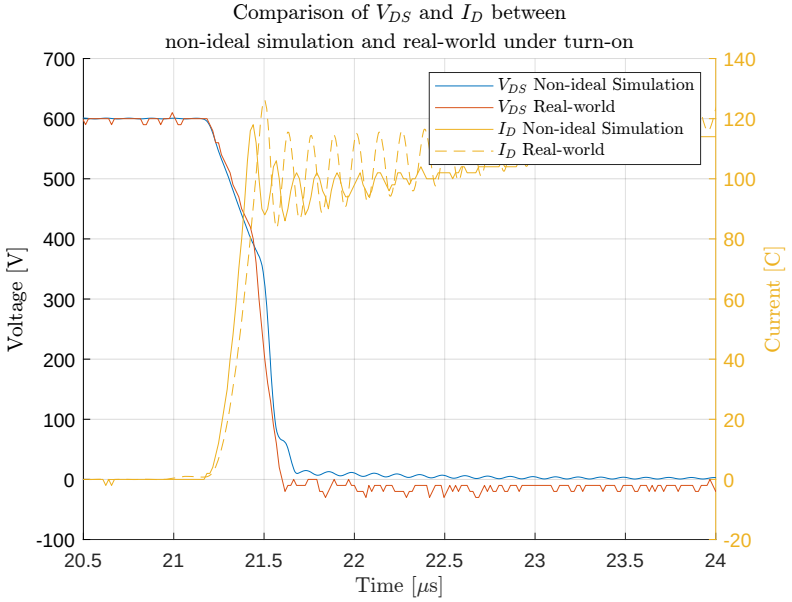
Figure 5.5: Comparison of V_{DS} and I_D between ideal and non-ideal simulation.

Next, the non-ideal simulation is compared with the real-world implementation of the DPT. Figure 5.6a compares the turn-off event. The difference between them is higher parasitic resistance in the real world, and the first transient has a different wavelength due to using parasitic components, that match the real world entirely, as it is impossible to have the exact resolution in a simulation. It means that the simulation is close but still missing the last one percent, which could be solved by using a higher-order inductor and capacitor model or having more decimal points on the parasitic values in the circuit. When comparing the turn-on event shown in fig. 5.6b, there are different I_D currents. The current difference comes from the turn-off event as well as the simulations resistance due to the skin effect,

which increases the resistance in the real world resulting in the current transients.



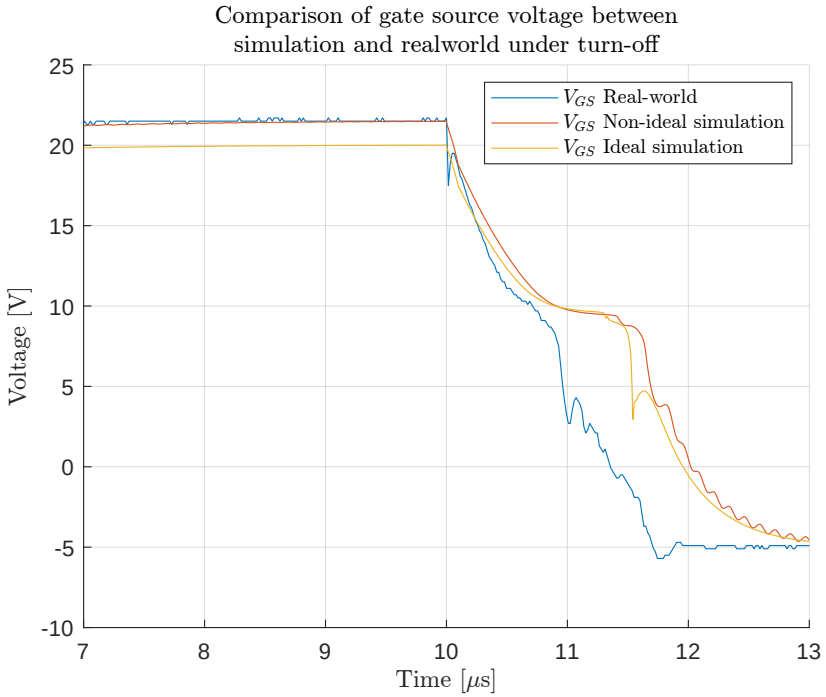
(a) Turn-off event Voltage and current.



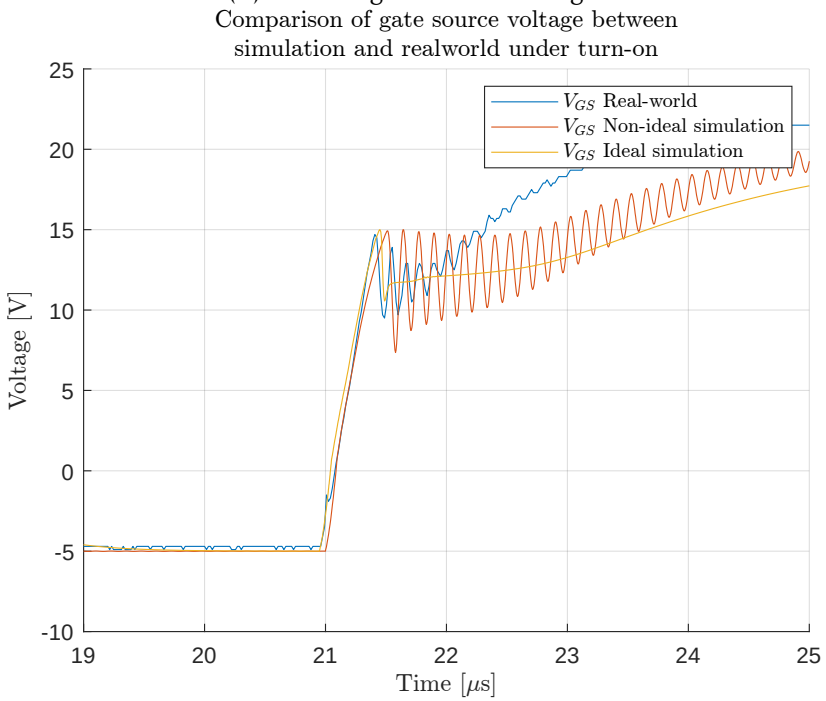
(b) Turn-on event Voltage and current.

Figure 5.6: Comparison of V_{DS} and I_D between non-ideal simulation and real-world.

After comparing V_{DS} and I_D, Figure 5.6 shows V_{GS}. When comparing the different gate-source voltages, it shows that the first part matches both turn-on and turn-off events thoroughly and that only the last part is different between the simulation and the real-world, because the gate driver is considered an ideal voltage source with a gate resistor in the simulation connected without wires. In the turn-off, the difference comes from an active miller clamp which gives a lower discharge impedance in the circuit; in the turn-on, the difference comes from a bypass capacitor which makes the voltage rise faster.



(a) Turn off gate-source voltage.



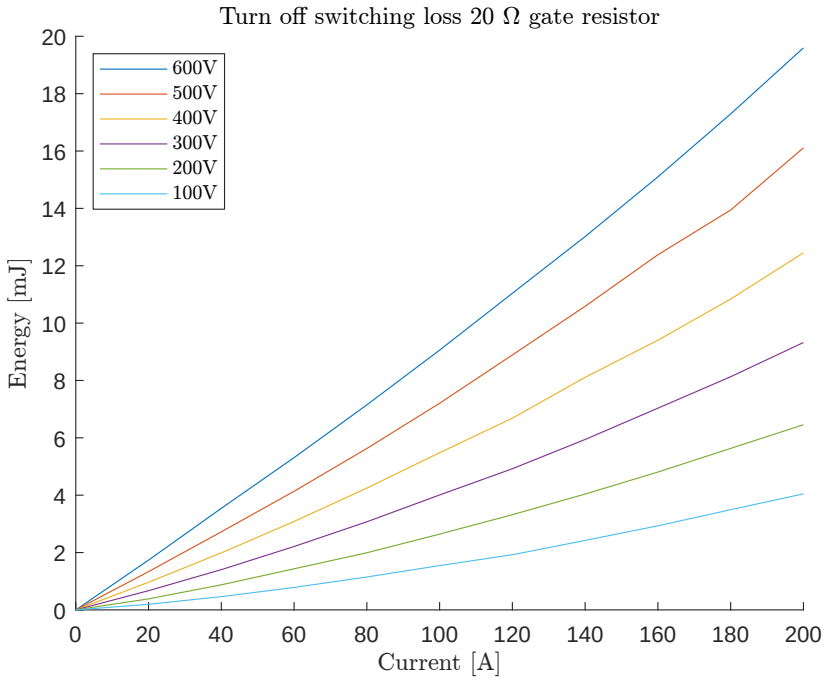
(b) Turn-on gate-source voltage.

Figure 5.7: Comparison of gate source voltage between simulation and realworld.

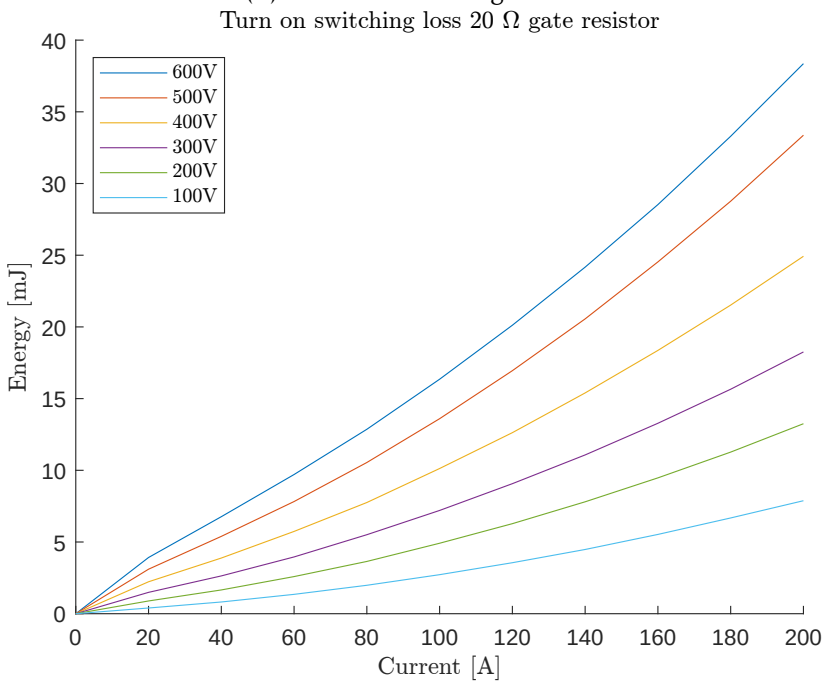
5.3 Switching loss result at 20 Ohm gate resistance

After comparing the switching event itself, the different switching losses are calculated and shown in figs. 5.8 to 5.10. First is the ideal simulation that shows how the switching loss increases with higher voltage and current. It can also be seen that the losses increase with

the same multiplier and the turn-on losses are higher than the turn-off losses.



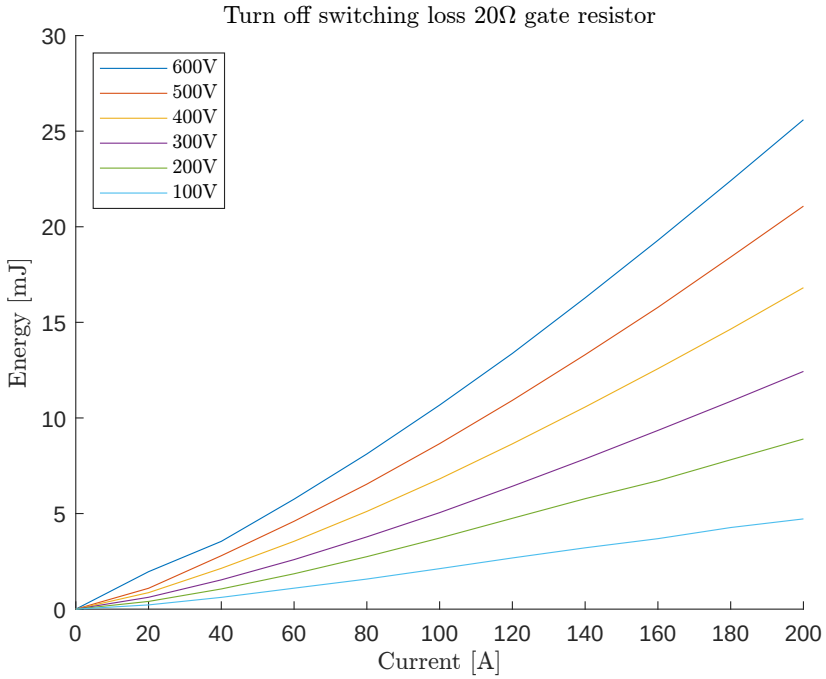
(a) Turn-off switching losses.



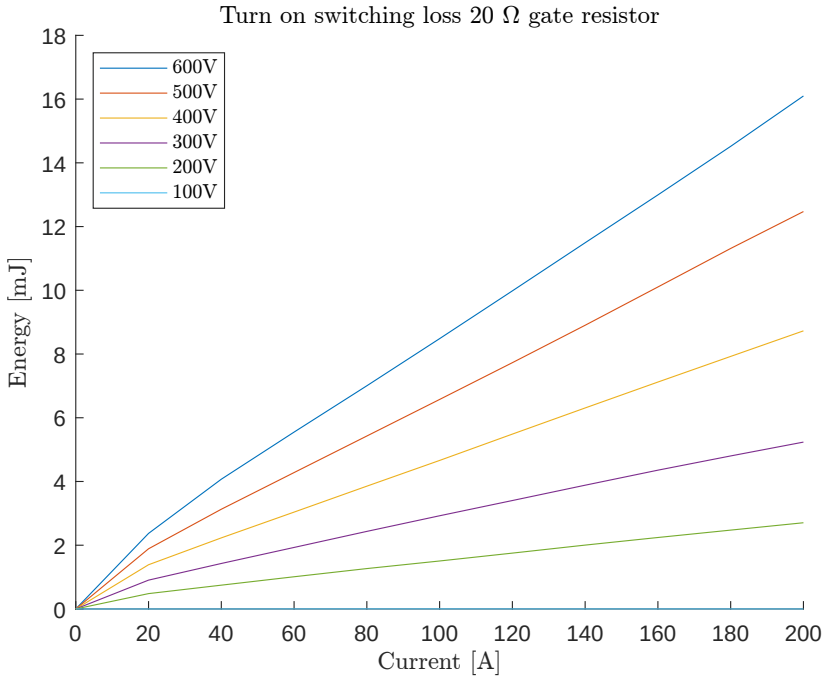
(b) Turn-on switching losses.

Figure 5.8: Switching losses of ideal simulation with 20 Ω gate Resistances.

Next is the non-ideal simulation shown in fig. 5.9 where the turn-off losses are lower than in the ideal simulation, which is due to lower current from the parasitic resistances in the system. The turn-on losses shown in fig. 5.9b are at the same size as the turn-off loss because of the higher parasitic losses in the system, as well as the introduction of the transients.



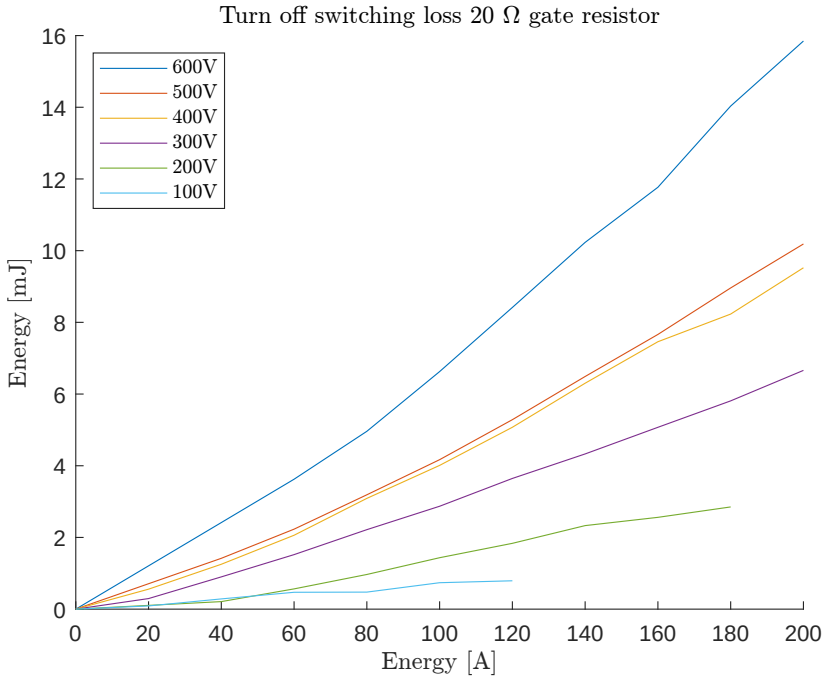
(a) Turn-off switching losses.



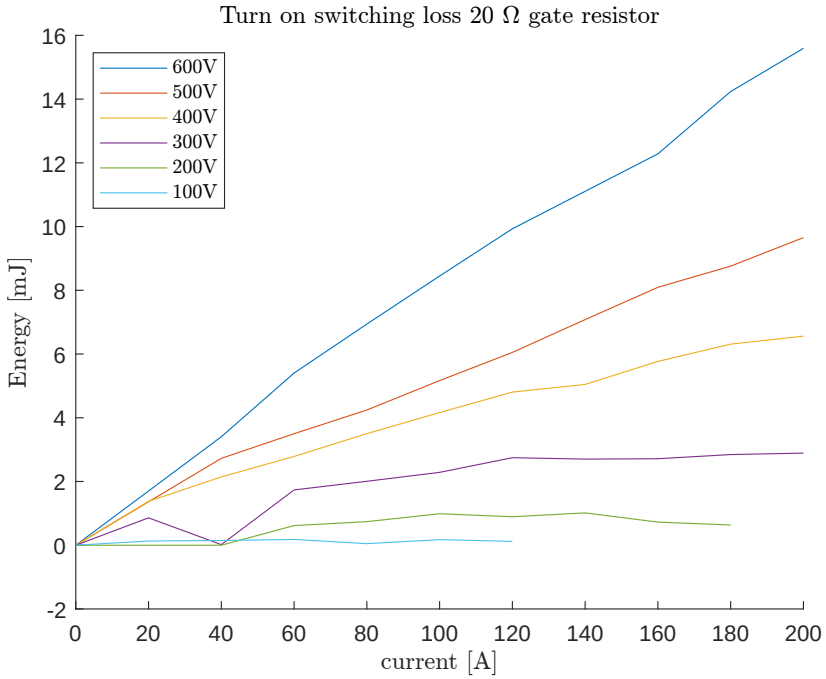
(b) Turn-on switching losses.

Figure 5.9: Switching losses of non-ideal simulation with 20 Ω gate Resistances.

Then comparing the non-ideal switching losses to the real-world shown in fig. 5.10, it is shown that the 500 V measurement matches with the 400 V measurement, which is due to the limitation of the microcontroller that can only do switches at one-microsecond intervals. This means that the current will be lower than the target and, thereby, the losses.
However, for 100V and 200V, the energy calculations stop because the capacitor is used as



(a) Turn-off switching losses Laboratory.



(b) Turn-on switching losses Laboratory.

Figure 5.10: Switching losses of real-world with 20 Ω gate Resistances.

a voltage source for the DPT, and in the mentioned range, the capacitor is completely discharged when reaching above 120A. Considering the general look of the switching losses, it shows that the losses are close to those of the non-ideal in the turn-off and turn-on events. However, they are lower in the real world when compared to the non-ideal simulation because the capacitor is not the energy source in the non-ideal simulation.

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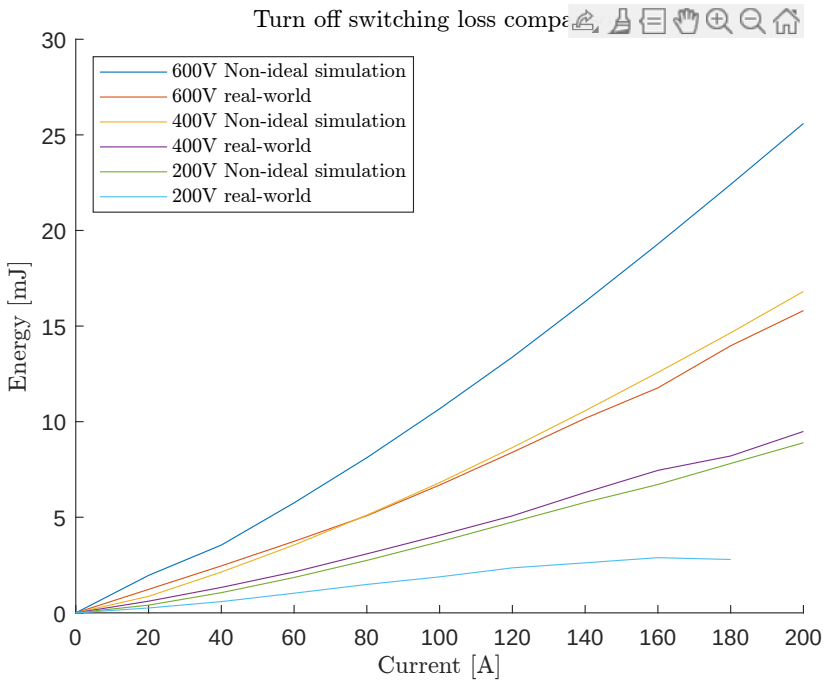
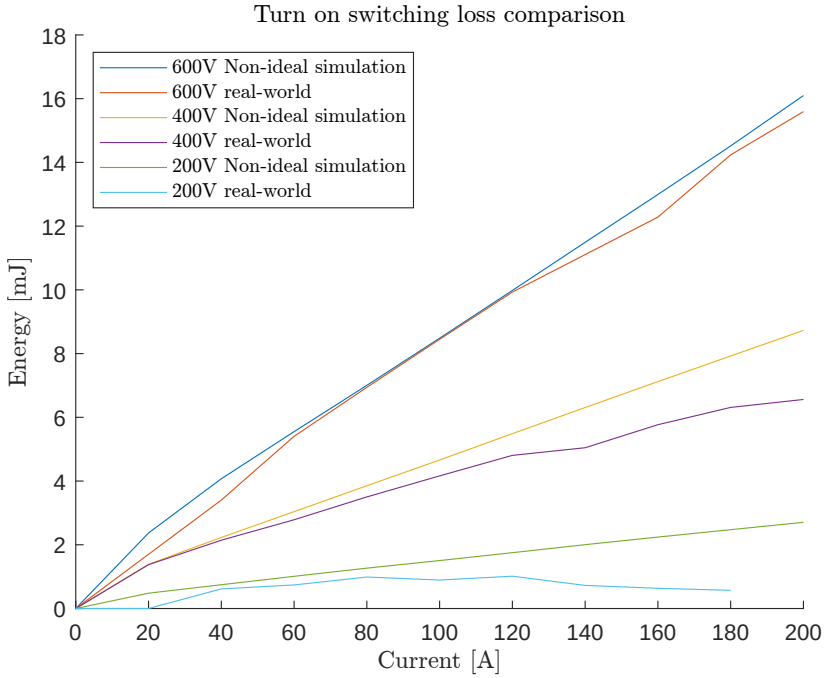


(a) Turn-off switching loss comparison.



(b) Turn-on switching loss comparison.

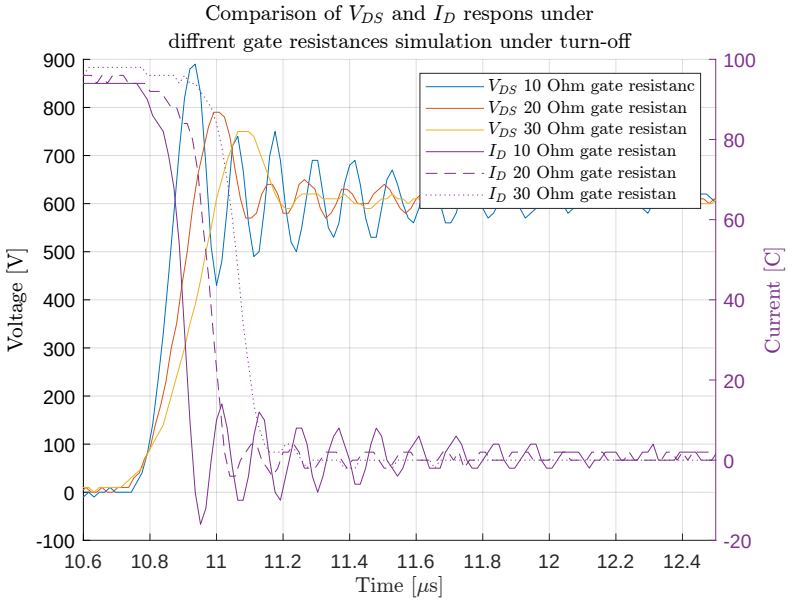
Figure 5.11: Switching losses of real-world with 20 Ω gate resistances compared with non-ideal simulation with 20 Ω gate resistances.

Lastly, fig. 5.11 shows a comparison between simulation and real-world. For the turn-off, the non-ideal switching losses are higher due to the switch of timing and the higher voltage in the system because the capacitor does not have a voltage drop. When then looking at the

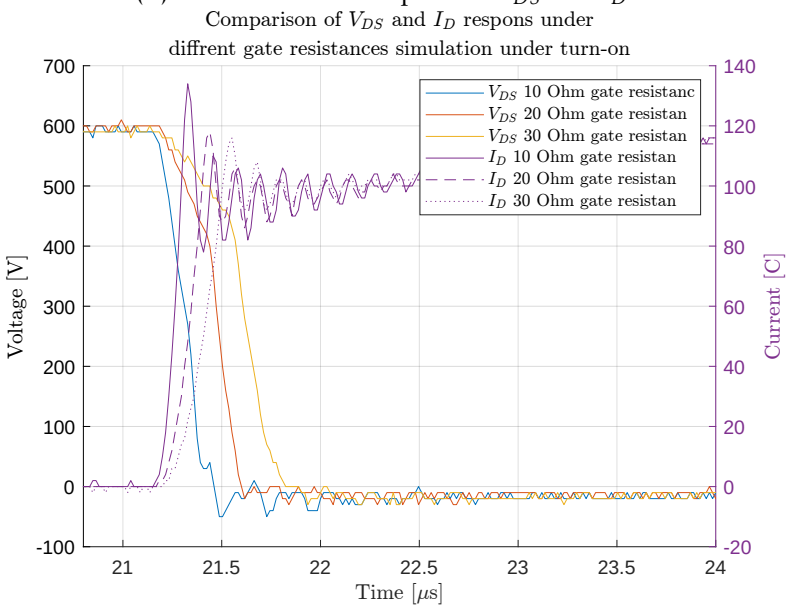
turn-on, it is shown that they have the same looses for 600 V, but it is reduced after 120 A for 400 V, and 200 V, which is due to the capacitor voltage.

5.4 Comparison between simulation and real-world at different gate resistances

When comparing V_{DS} and I_D at different gate voltages, it is shown that there is a clear difference shown in fig. 5.12.



(a) Turn-off event comparison V_{DS} and I_D.

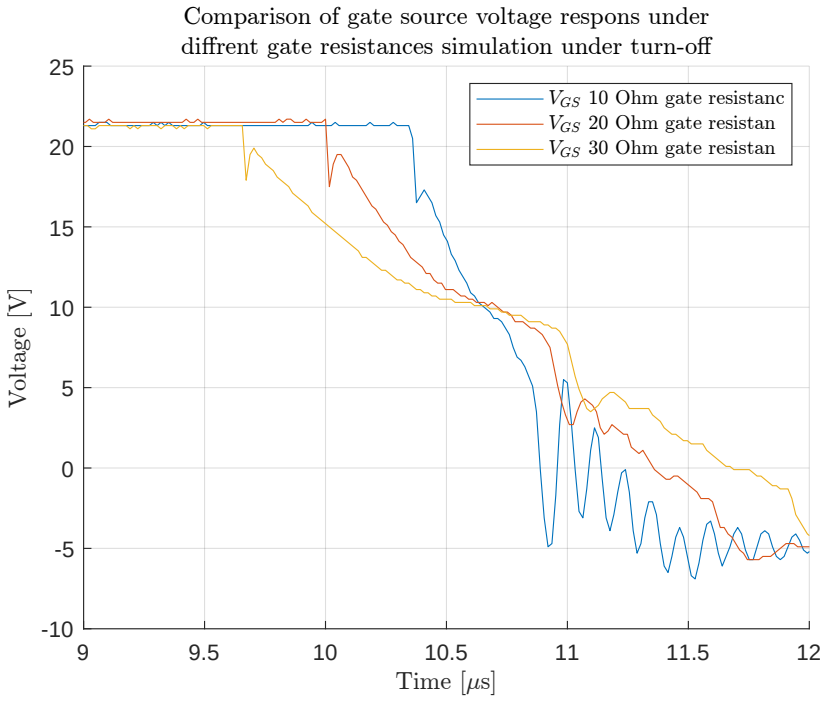


(b) Turn-on event comparison V_{DS} and I_D.

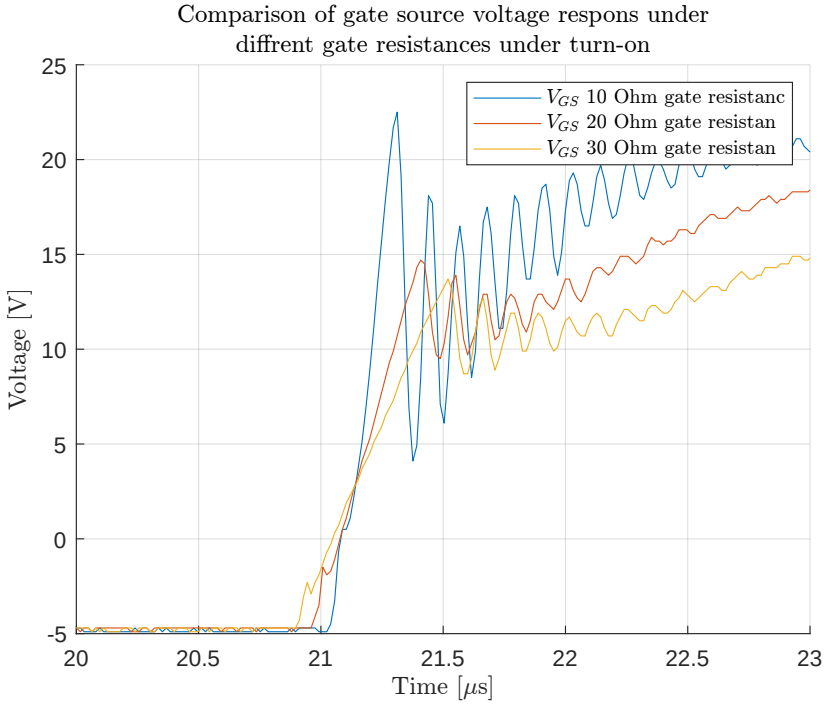
Figure 5.12: Comparison of V_{DS} and I_D under different gate resistances in real-world.

The difference is that when going from 20 Ω to 30 Ω gate resistance, the turn-off time and the turn-on time increase. When going from 20 Ω to 10 Ω the turn-on time reduces. This

is due to the gate voltage reaching the turn-on state faster. After showing V_{DS} and I_D, V_{GS} is shown.



(a) Turn-off event V_{GS}.



(b) Turn-on event V_{GS}.

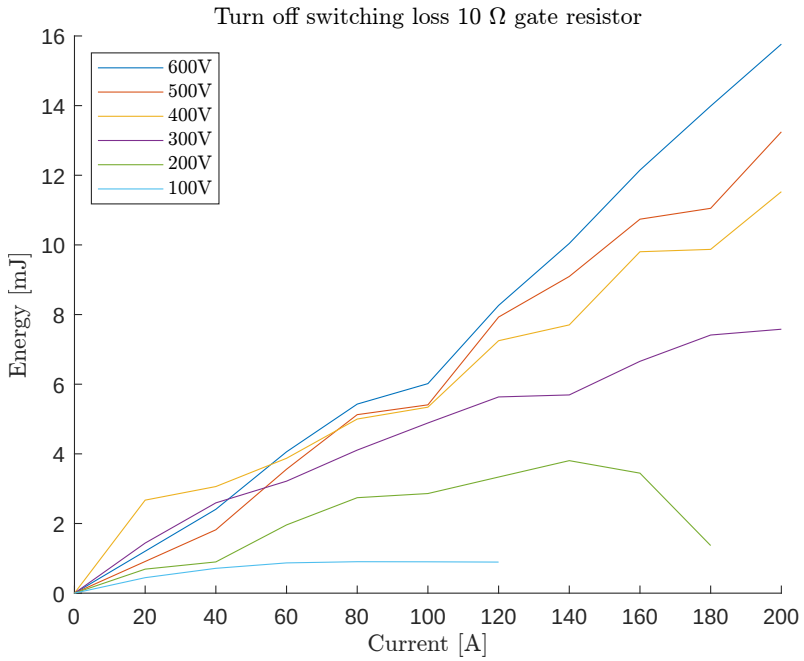
Figure 5.13: Comparison of gate voltage with different gate resistances in real-world.

The gate voltage is falling slower at 30 Ω compared to 10 Ω gate resistance. Figure 5.13 shows that there are more transients on the lowest gate resistor test; this is due to the

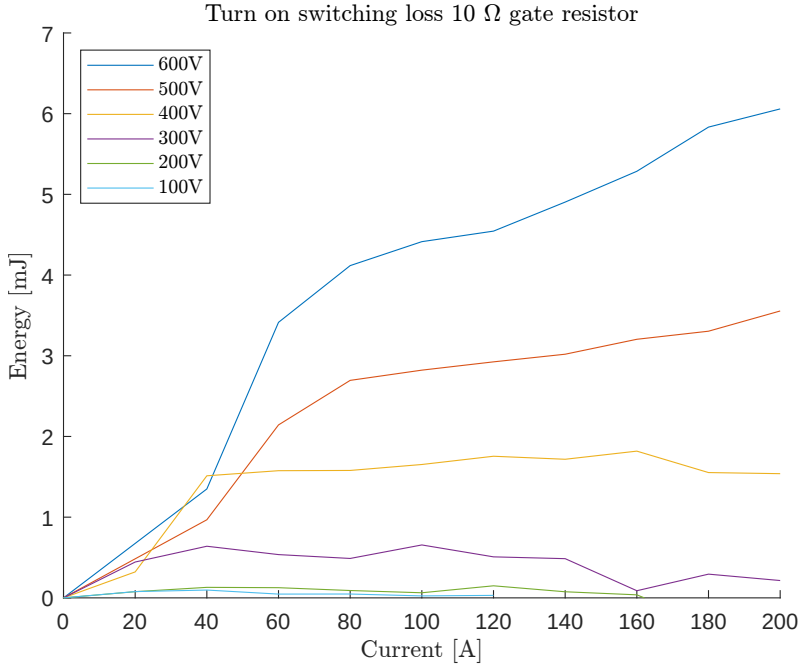
reduced resistance dampening the oscillations.

5.5 Energy calculated at different gate resistors

Section 5.4 shows that switching time depends on the gate resistor.



(a) Turn-off switching losses.

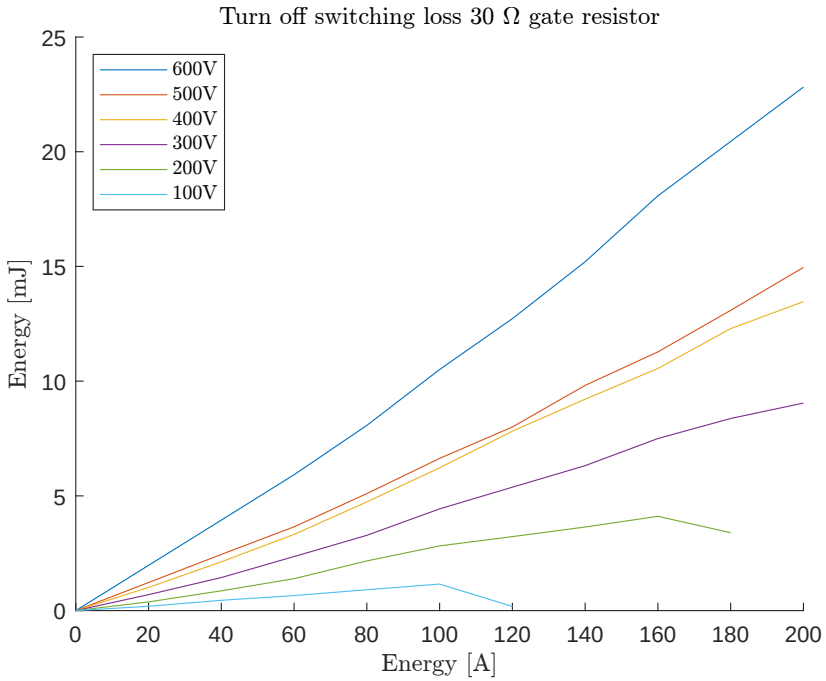


(b) Turn-on switching losses.

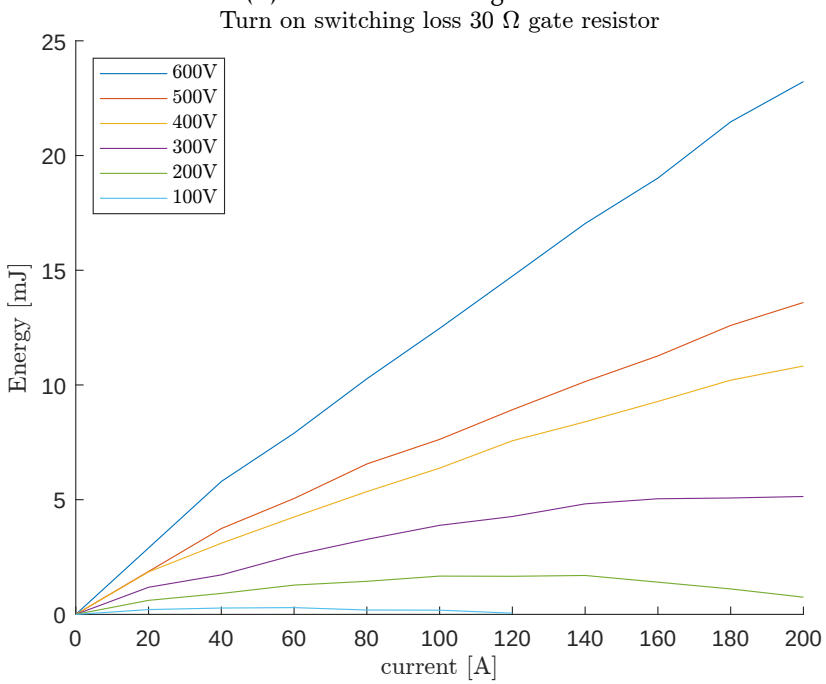
Figure 5.14: Switching losses of real-world with 10 Ω gate Resistance.

It is also shown that if the switching time decreases, better probes are required to increase

the number of samples that are measured.
In comparison, increasing the gate resistance, increases the switching losses as shown in fig. 5.15.



(a) Turn-off switching losses.



(b) Turn-on switching losses.

Figure 5.15: Switching losses of real-world with 30 Ω gate Resistance.

5.6 Device characterization

For characterization, there are two defining factors. First, the switching losses and then the conduction losses. Figure 5.10 shows the Switching losses. It is shown that the energy loss is different for every voltage between 100V to 600V and for the different gate voltages. When considering 20 volts as the standard, the energy loss will reduce when reducing the gate resistance, as well as the voltage and current, and the opposite is true for increasing voltage, current, and gate resistance.
An IV curve of the MOSFET is made in an IV analyzer to find the conduction loss, and the results in fig. 5.16 are obtained. The conduction losses can be calculated by ohms law by finding the on-state resistance for the different gate voltages.

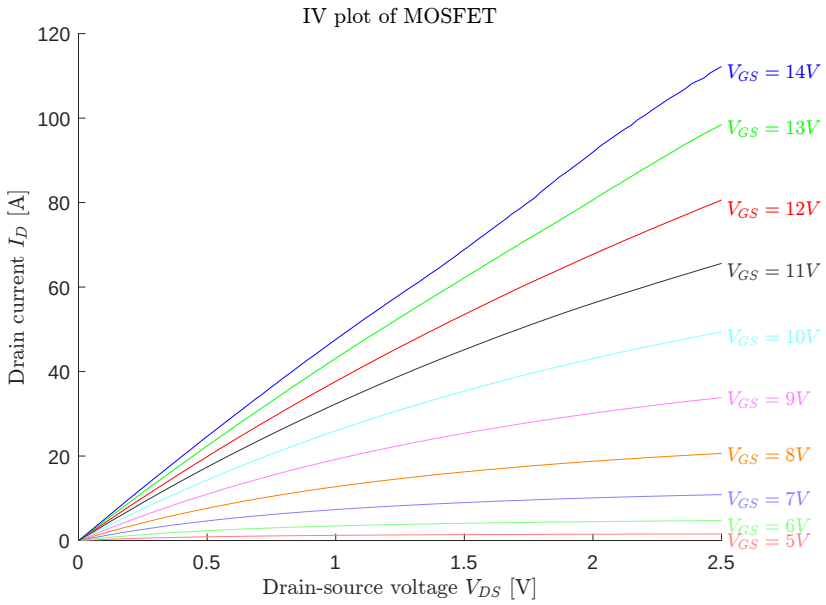


Figure 5.16: IV curve of MOSFET.

6 Short circuit protection

After calculating the switching losses, a look is taken at the prospective short circuit protection.

6.1 Short circuit protection

For implementing the crowbar, the non-ideal simulation is used, there an ideal IGBT is added in parallel with the capacitor to draw the current. The protection device's specifications are important for using a crowbar because the device is required to turn on faster than the break downtime of the MOSFET, or else, the protection would not protect the circuit. As there is no final short circuit protection scheme, there is no short circuit detection, but rather, the protection device turns on after the detection time. Shown in fig. 6.1 is the simulation of the protection of the MOSFET via an ideal insulated gate bipolar transistor corresponding to the NPN transistor in the figure.

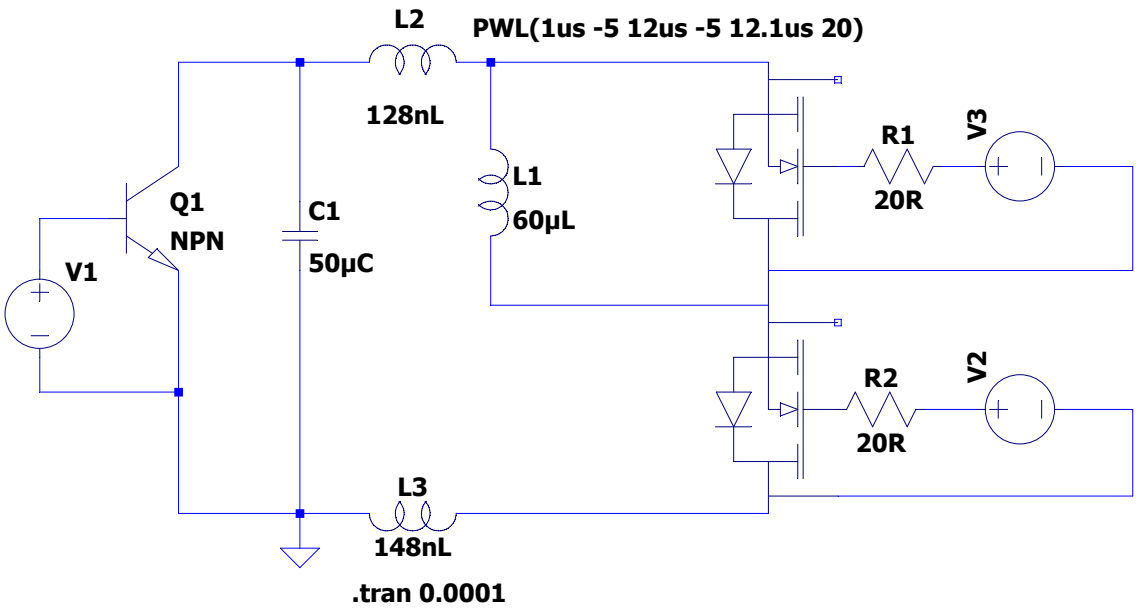


Figure 6.1: Simulation of short circuit with prospective protection.

First, to test the prospective short circuit protection, a short circuit is created by simultaneously turning the high side and low side MOSFET on. After two microseconds, the crowbar turns on, clearing the fault.

6.2 Short circuit fault protection

The following shows the prospective short circuit protection response simulation and a short circuit to compare the protection that can reduce the short circuit current and thereby protect the device from failure. First, in fig. 6.2 is a short circuit produced by turning on the high side MOSFET after the low side MOSFET turns on. From the voltage and current

response, it shows that the current is rising while the voltage will drop until it reaches zero and the capacitor discharges. It will result in currents exceeding the MOSFETs I_D current rating, thereby damaging the device.

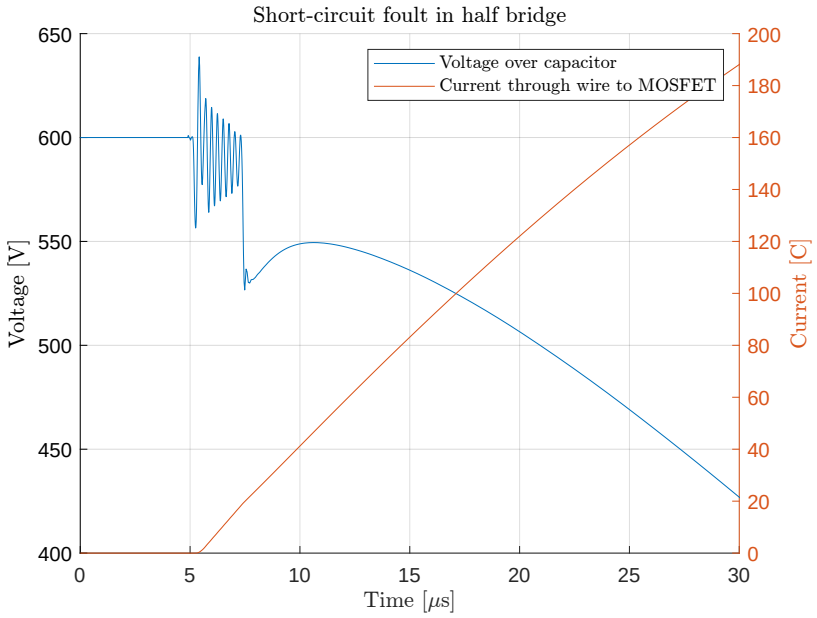


Figure 6.2: Fault produced by turn on of high side MOSFET.

Short circuit protection is implemented as a crowbar that works as a low-impedance path to protect the MOSFET. The result for this simulation is shown in fig. 6.3.

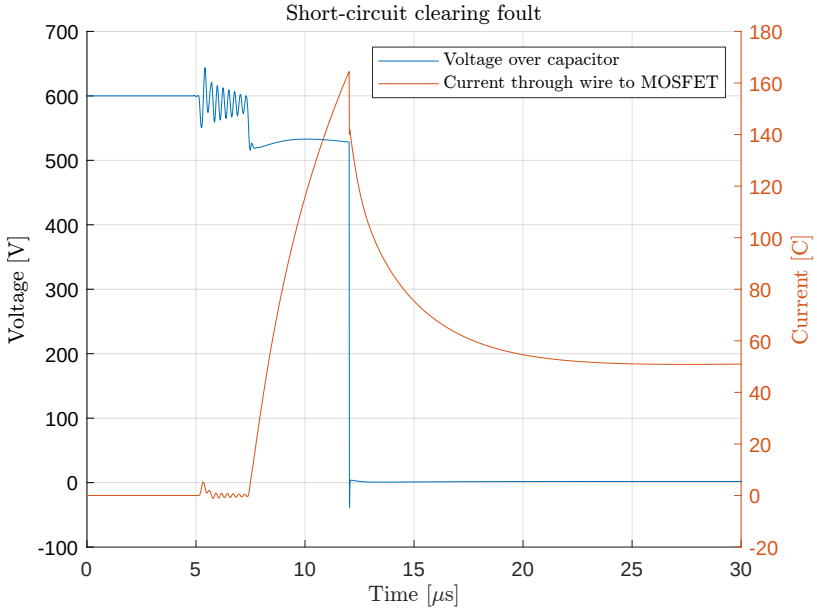


Figure 6.3: Fault cleared that was produced by turn on of high side MOSFET.

As shown, after introducing the fault, the current rises. After 12 microseconds, the protection device activities drop the voltage to zero, and the current is no longer rising but falling. It is decided to use a voltage source as a gate driver for the IGBT to activate the device. As

the timing of the fault is known, it is decided to turn the IGBT on after 2 microseconds by changing the V1 voltage from 0 to 20, thereby turning the device on and achieving short circuit protection. Figure 6.3 shows that the current rises exponentially when the short circuit is created, then the crowbar turns on, pulling the current back down. Figure 6.4 shows the voltage over the crowbar and the current running through it; the voltage goes to zero while the current increases until the capacitor is discharged.

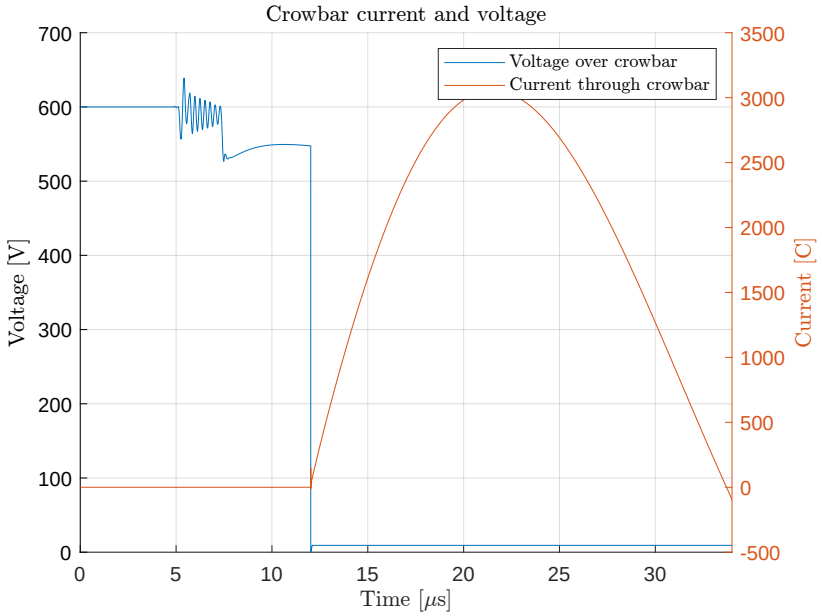


Figure 6.4: Current and voltage through crowbar.

7 Discussion

Because of the limitations, different factors are ignored or reduced, which is discussed in the following. After that, the results for the DPT and the comparison are discussed. Finally, the prospective shorts circuit is discussed.

First, the DPT is executed at ambient temperature, which means that the switching results are extracted at ambient temperature. To use the results requires the MOSFET to be at the ambient temperature all the time, as increasing the temperature will render the result useless because the temperature of a MOSFET either reduces the switching losses or increase them. Ther after the DPT was allowed only to have a temperature rise of 1 degree, which is fulfilled through the inductors charging time per second.

Next, the voltage drop over the capacitor was chosen to be 20 volts, though the results showed that the voltage drop increases with the different voltages used. This is shown to the extreme in the 100 Volt test, where there is a voltage drop of 100% as the capacitor is fully discharged. The same is shown of the 200 volts when reaching above 180 amperes.

Then the simulation is modeled from the DPT implemented in the lab. As shown, the parts that were implemented from the laboratory were the capacitor and inductor parasitic models as well as the inductor parasitics. When shown the result are shown that there were differences in the results which result from these differences that the capacitor does not have a voltage drop as well as the gate driver is ideal and does not include the active miller clamp or a bypass which results in different turn-off turn-on characteristics .

Through the comparison of the simulation with the laboratory implementation, it is shown that both of them match well enough to say that they are working correctly. It should be considered to add more parasitic components to make it better. One problem with this is, though, that there are parts that can not be accounted for. One of these is when the MOSFET is turned off and on. This is because the Microcontroller will send a signal to switch the MOSFET, and the oscilloscope will then measure it; now, it is questionable if two probes are measuring at the same time or if they have a time delay, thereby changing the result.

The ideal simulation gives the results under ideal situations only considering the losses of the MOSFET. In the ideal simulation, the result is as expected, where the turn-off losses are lower than the turn-on losses. As the ideal simulation does not have any resistance losses in the system, it is the expected result. It means that the DPT should arrive at the result as the ideal simulation if the DPT is optimized to remove as much of the parasitics and resistances as possible, as well as not having a voltage drop over the capacitor, which is impossible.

As the world is not ideal, the non-ideal simulator is considered the one to compare, and

when comparing those two, they match closely in the current and voltage, thereby showing that the DPT is designed acceptable.

When then looking at the general use of the DPT, it shows it can be considered to have achieved it as it is possible to use the DPT in the Range of 300 V to 600 V though it is essential to state that if special voltages are chosen more time is required to have the right timing for currents, this discusses how much sense it makes to have a general DPT as 300 V differences are not a relatively limited spread, though it gives a good overview on how to make a general test with the equations described in section 2.

Lastly, the short circuit protection is discussed as the short circuit protection is only implemented with an ideal switch ignoring all losses and parasitic elements. To have a better simulation should be chosen to use an IGBT that has an LTspice model to make the simulation better. However, at the same time, it gives a rough idea that it is possible to use the crowbar as protection and that it is fast enough to protect the MOSFET. It can then be expanded upon. At the same time, it shows that the crowbar is a good choice as the voltage goes to zero instantly, and it reduces the current. Then considering that the current through the crowbar is 10 to 20 times higher than the maximum current through the inductor, it requires an expensive IGBT that can tolerate 4 kA current running through it. To add protection, the DPT only makes sense if the MOSFET is non expendable or more expensive than implementing a crowbar.

8 Conclusions

A generic DPT is implemented in the laboratory, and the switching losses of a MOSFET have been extracted. Subsequently, the DPT is modeled in LT-spice, and a prospective crowbar is investigated.

By implementing the DPT, an equation is derived for the inductor to keep the MOSFET below 1 degree. Next, an equation is derived to design the capacitor as a power source. These are general equations for modeling a DPT and keeping the MOSFET below a specific temperature. From these equations, an inductor and capacitor are built accordingly. The impedance is then used to test whether the components are modeled correctly and to find their parasitic components. The results are compared after developing the test setup and modeling it in LT spice. This DPT showed that it can test the MOSFET at different voltages and currents with some limitations because of the capacitor voltage drop.

Using the test results from the DPT in MatLab, it is then possible to extract the switching losses based on the turn-on or turn-off event for the different voltages and currents. The DPT shows that it is possible to extract the switching losses in simulation, simulation with parasitic, and in the laboratory. The generic element of the DPT is shown through testing the MOSFET at different voltages and currents.

Through this, it is clear that testing a SiC MOSFET with a generic DPT requires the right size inductor, capacitor, and a versatile micro-controller to control the exact switching time of the DPT. The testing additionally requires the right measuring equipment to measure faster or slower switching times. Sizing these allows the DPT's use on different voltages, as shown. Considering this, it is concluded that a generic DPT is developed to extract the switching losses of a MOSFET.

After the DPT, this project investigated how to protect against short circuit faults. Under the investigation, three solutions are found: series, desaturation, or crowbar protection. From those, the crowbar protection is then implemented in simulation because of its ease of adding it to the DPT. The crowbar only sits in parallel and can, therefore, be added and taken off as required. Through this, it is then shown that the crowbar is a possible protection against short circuit faults as it is fast, easy to implement, and only requires a IGBT and the corresponding detection and gate circuits.

In general, this project has shown that the DPT can extract the switching losses at different voltages and currents, while the MOSFET is protected against short circuit faults. This, in turn, offers an opportunity to standardize the DPT setup and streamline the extractions of switching losses. Consequently, precise energy losses in power converters and preventions of device destruction under fault are realistic possibilities for the future.

9 Future investigation

As a project is defined by its boundary, there are always future investigations that can increase the prospective scope of the project. In this project, the problem specification defines the boundary and the due date's time limit.

One of the major aspects that should be looked into is the short-circuit protection. This project has demonstrated that the protection is feasible. The next step is to choose how the protection circuit should protect and how fast. This step is paramount, because it is first possible to properly define the protection afterwards. After all, defining protection is only protects to salvage the module, to see why the MOSFET failed, is which differs from the protection required to save the device from damage. From this, the right protection semiconductor can be chosen, and the detection circuit is found because some detection methods are faster than others.

A second aspect that should be investigated further relates to is optimizing the DPT regarding noise reduction, Such optimization is done by reducing the wire length between the capacitor and the MOSFET. The other part of being optimized is to use a gate driver specifically designed for the MOSFET. A MOSFET-designed gate driver can be mounted on the MOSFET and thereby reduce the wire between the gate driver and the MOSFET.

Since this project had a limited budget, only one MOSFET was chosen to test the DPT at different voltages. To show if the DPT works on different MOSFETS, the DPT should be tested with different MOSFETs. Here it would be crucial to choose some MOSFETs that have different voltage and current ratings to show how many different MOSFETs it works with.

One could also consider optimizing the inductor to reach exactly 60 μH and optimizing the inductor windings to have the same spacing between them and build the inductor on a more permanent structure. The DPT can also be tested with different types of capacitors to show how a different capacitor can influence the test.

Lastly, the DPT could be implemented on a PCB, thereby making it into a permanent setup that can be used again and again. By using a printed circuit board, it will also be possible to optimize the DPT in regards to wire length, harmonics, and safety. Subsequently, one could also consider going from a voltage level below 1000 to the range of 1000 to 10000 voltage to increase the standardization of the DPT.

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