DEPARTMENT OF ENERGY TECHNOLOGY
AALBORG UNIVERSITY

# Grid connected voltage source inverter control under unbalanced and distorted grid conditions

Wind power systems final semester project

Bizhan Neishabouri

Department of Energy Technology, WPS4, 2023

Masters thesis

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The programs that are used in this short technical report are: MATLAB®, Simulink® PLECS®

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**Abstract:**

Wind turbine systems are one of the main energy generation technologies in the journey of electricity infrastructures transition towards renewable energies. Conventional power plants' substitution by wind turbines in the grid requires the wind turbine's grid side inverter robustness against voltage distortion in the grid. These distortions can be because of transmission line impedance unbalance or other equipment in the grid causing synchronization or grid connection problems. This project analyzes the importance of filtering the voltage distortion using existing solutions, for instance, MSRF-PLL. The theory, conducted and simulated case studies, and experimental results to analyze the stability and performance of the controller are analyzed to address the MSRF-PLLs capability in maintaining grid connection during distorted grid voltage conditions.

# Preface

This project is conducted individually as the final semester project at Aalborg University as a part of the Wind Power Systems master program. The theme of this semester is *Final semester in wind power systems*, and the title of this project is *Grid connected voltage source inverter control under unbalanced and distorted grid conditions*.

I would like to thank the supervisors *Sanjay Chaudhary* and *Gibran David Agundis Tinajero* for guidance and help during the thesis.

## Readers guide

Figures and tables in the report are numbered according to the respective chapter. In this way, the first figure in Chapter 2 has the number 2.1, the second number 2.2, and so on. Explanatory text is found under the given figures and tables. Figures without reference are made by the student.

On page **v**, a Table of Contents is given. When viewing this report as a PDF, hyperlinks in the table of contents will allow fast navigation to the desired sections. Additionally, a table of figures is found on page **ix** in order to find the actual place of the figure quickly.

The bibliography can be found on the last page, and is sorted after their order of appearance in the text. All the appendices can be found after the bibliography, which is labeled with letters.

If a source is used to cite a specific piece of information, the source will appear before the period [source no.]. If a source is used in general in the entire paragraph, it will appear after the period at the end of the paragraph. [source no.]

Aalborg University, June 2, 2023

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# Nomenclature

## Acronyms

| | |
|---|---|
| AC | Alternating Current |
| CCAD | Capacitor Current Active Damping |
| DC | Direct Current |
| DG | Decenteralized generation |
| DSO | Distribution System Operator |
| DSRF | Dual Synchronous Reference Frame |
| EV | Electric Vehicle |
| FACTS | Flexable AC Transmission System |
| FRT | Fault Ride Through |
| GC | Grid Codes |
| GCVSI | Grid Connected voltage source inverter |
| IEC | International Electrotechnical Commission |
| IGBT | Insulated Gate Bipolar Transistor |
| LTI | Linear Time Invariant |
| MSRF | Multiple Synchronous Reference Frame |
| PCC | Point of Common Coupling |
| PI | Proportional Integral |
| PLL | Phase Locked Loop |
| PV | Photovoltaic |
| PWM | Pulse Width Modulation |
| RES | Renewable Energy Source |
| STATCOM | Static Synchronous Compensator |
| SVM | Space Vector Modulation |
| THD | Total Harmonic Distortion |
| TSO | Transmission System Operator |
| VSC | Voltage Source Converter |
| VSI | Voltage Source Inverter |
| VOC | Voltage Oriented Control |
| VUF | Voltage Unbalance Factor |
| WPP | Wind Power Plant |
| WT | Wind Turbine |
| WTS | Wind Turbine System |
| ZOH | Zero Order Hold |

# Variables

| Symbol | Description | Unit |
|---|---|---|
| C | Capacitance | F |
| $\hat{E}$ | Generated Voltage | V |
| f | Frequency | Hz |
| I | Current | A |
| L | Inductance | H |
| P | Active Power | W |
| Q | Reactive Power | VAr |
| S | Apparent Power | VA |
| t | Time | s |
| v | Voltage | V |
| $\omega$ | Angular Velocity | Rad/s |

# Contents

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# Chapter 1

# Introduction

*This chapter introduces the general scope of the project in three sections; Motivation 1.1, State of the art (SOA) 1.2, and Problem formulation 1.3. The Motivation highlights why the subject is interesting to be looked into. The state-of-the-art explains the latest developments in different subjects that the project is looking into. The problem statement section is about framing the specific subject from the state of the art in different subsections.*

## 1.1 Motivation

The evolution of electrical infrastructures all over the world is highly affected by the transition towards renewable energy production and utilization. The integration of renewable energy sources (RES) is important due to environmental concerns and shortages in traditional resources because of excessive use, increase in demand, and political reasons. These reasons motivate achieving fully renewable-based electrical infrastructures, as is aimed by the European Union until 2050. [2]

The integration of RES units into power systems must be done carefully, in multiple steps, and over time. This is done so manufacturers, power system operators, and consumers have to adapt to this process. The multiple steps in power systems evolution are explained in the following list. [3]

1. In the first step, the power system architecture is changing towards utilizing decentralized generation (DG) units. A DG-based power system can handle the challenge of geographic and location limits of integrating RES units. However, this causes more complicity, uncertainty, and less reliability of system operation. [1, 4]

2. The complexity of a DG-based power system is due to high dynamics in the balance of production and demand, although RES units are perfectly utilized. Therefore, the whole infrastructure of the system must evolve, for example using wind turbine systems (WTS), combined heat and electricity systems,

PV-STATCOM, etc. These additional technologies are utilized to help DG-based power systems handle the high dynamics in power balance and reduce operational complexity in the second step [4, 5, 3].

3. In the third step, the challenge of uncertainty in power systems is about when to expect the dynamics happening when the dynamics for the main source of energy in RES units are also unknown. The solution purposed by the industry is for the power systems in big regions to cooperate in power transition, as a super grid to reduce this uncertainty. [2, 3]

4. In the last step, the challenge of reliability is to have standards, making sure if a RES unit is integrated, what regulations are needed, and when. The grid codes were introduced by TSOs and DSOs so they can achieve reliable dispatch when RES units guarantee supply security and the design specifics are clear for manufacturers that RES units need to comply with. [6]

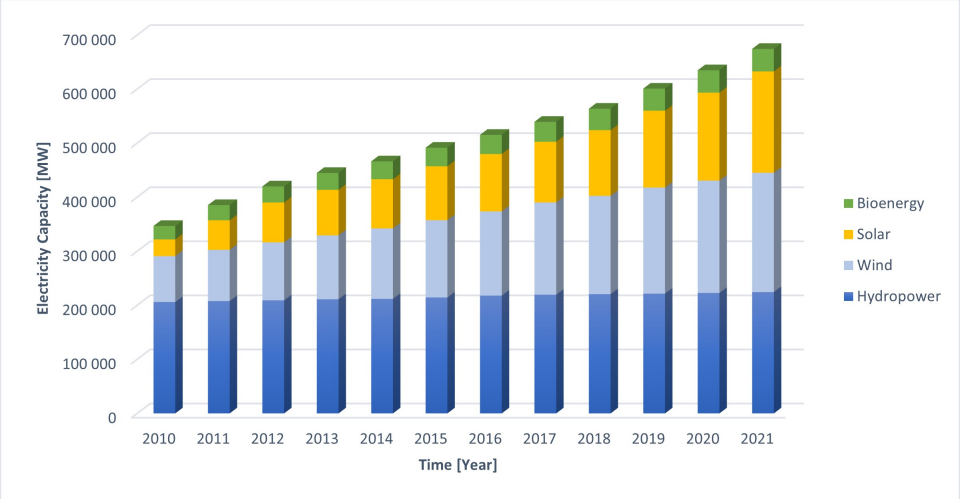


**Figure 1.1:** Europian trending renewable integration [1]

Figure 1.1 shows that the integration of RES increased by a factor of two from 2011 to 2021 in Europe. By using a variety of generation technologies and improvement equipment, European grids successfully were able to help the system maintain high dynamics. The interconnection with neighboring grids assisted with worst-case uncertainties and adopting specific grid codes clarified the criteria for reliable regulation. [2, 3]

Research also investigated, cases like photovoltaic (PV) generation unit integration in California were turned out to be not successful. Although PV units are feasible geographically, not enough equipment to support the grid for dynamics, isolation of the grid from neighbor regions, and no revisions in grid codes resulted

in disconnecting a high portion of PV capacity due to severe losses in the network. [3]

Meanwhile, the RES technology manufacturers aimed to achieve the security of supply. The challenge of supply security, because of the fluctuating main energy source of RES units, is resolved by implementing power electronic converters as an active intelligent interface between RES generation and load or grid. The term active means a controller is needed so the device act on the input based on the command to obtain the desired output. This means in the end, proper control design is important, so reliability and quality can be ensured by RES units. [7]

One of the advanced RES technologies with much potential to develop further in Denmark is wind power. The wind turbine industry is pretty advanced and can further utilize on a multi-gigawatt scale with current commercial technologies. With current technologies, countries like Denmark successfully achieved fulfilling 25% of the country's demand in 2010 to 47% in 2019, only with wind power. By selling and storing excess electricity, buying or using the stored energy, wind power systems are reliably integrated into the grid. [8]

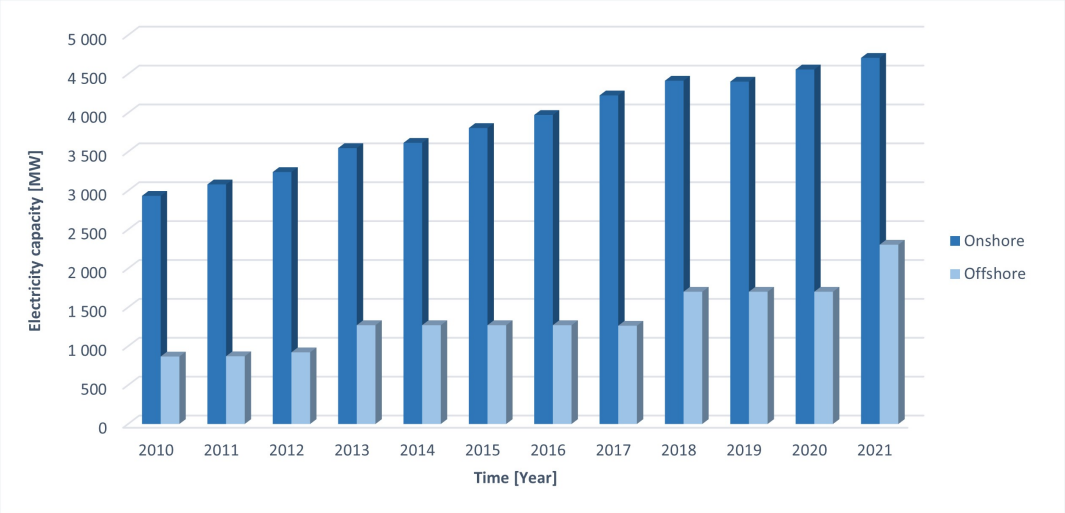


**Figure 1.2:** Denmark's electricity capacity by wind turbine systems [1]

With further advances in power electronics control technologies, as wind power systems integrate more into the grid they will be able to provide more services to the grid. Even in new researches, the capabilities of wind turbines are investigated in theory, highlighting the possible role of wind turbines in the near future, supporting new technologies like nuclear fusion, in the transition towards 100% renewable energy generation on a global scale. In the next section 1.2, these new technologies will be introduced, providing a background for further analysis of the control aspects of converters used for grid integration of wind turbines. [8, 9, 10]

## 1.2 State of the art

### 1.2.1 Grid codes for wind turbines integration

The importance of grid codes in utilizing converters in wind power integration is to make the expected design requirements clear for manufacturers. The integration of wind generation units can be on a residential scale with a single wind turbine or can be on a large scale for example a gigawatt wind farm. The energy harvesting system can be manufactured with different generators and interconnection can be standalone or connected to a network. The equipment and interconnections of the converter have different power ratings and voltage inputs. [11]

When the TSOs or DSOs declare the integration and requirements, the manufacturers are able to use the grid codes to utilize converters and controls compatible with the technologies that they have. Therefore, TSOs and DSOs specified the grid codes for grid integration of wind power plants with different scales. The grid codes are specific for different plant categories based on their power rating and voltage levels, delivered by ENSTO-E European standards and Nordic grid codes as requirements for generation (NC-RFG). The plant categories to be utilized by manufacturers are shown in table 1.1. [12]

**Table 1.1:** Plant categories based on rated power and voltage [12]

| Plant category | Rated Power | Voltage Level |
|---|---|---|
| A1 | $\leq$ 11 kW | <1kV |
| A2 | 11 kW <S $\leq$ 50 kW | <1 kV |
| B | 50 kW <S $\leq$ 1.5 MW | <1 kV |
| C | 1.5 MW <S $\leq$ 25 MW | <100 kV |
| D | S >25 MW | >100 kV |

The connections to voltages less than 1 kV are considered low voltage connections, more common in distribution systems and residential plants. The voltage levels higher than 1 kV are in medium and high voltage applications in wind power plants and wind farms. The grid codes require that the converter control maintains the quality of supply and services in regular or abnormal interconnection conditions. When the scale and purpose of the integration are clear, the choice of device and control configuration is to be done. [6]

### 1.2.2 Power converters in wind turbine systems

There are four main types of wind turbine systems technologies introduced. The type 1 wind turbine system, also known as the Danish concept, and type 2 wind turbine system had limited capabilities for control and therefore were replaced

by type 3 and type 4 wind turbine systems. With advancements in power electronic converter technologies, type 4 wind turbine systems are the most common topology used for wind energy conversion systems in large megawatt-scale wind turbines. Type 3 topology is becoming less common in large scales because of the sensitivity of the generator to disturbance of the load/grid-connected side. The generic configuration of the type 4 wind turbine system is shown in figure 1.3. [6, 8, 13]

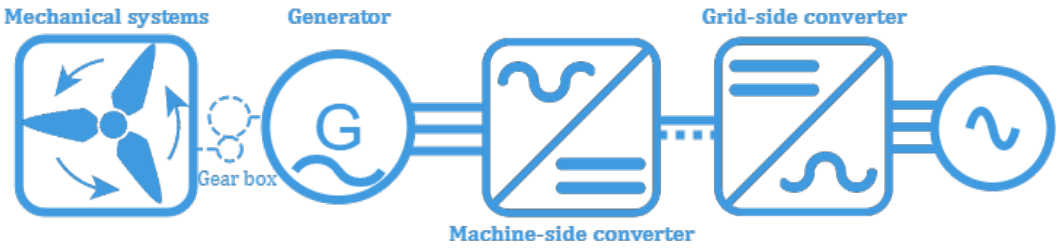


**Figure 1.3:** Type 4 wind turbine energy harvesting system schematics

In the type 4 wind turbine systems, after the mechanical system is connected to the generator, there is a full-scale power converter topology to fully isolate the generator output from the load or grid side. This topology uses AC to DC to AC conversion in two stages, using two converters that are connected back-to-back with their DC link. The first converter controls the generator dynamics and mainly manages power flow from the generator into the DC link. The second converter controls the DC into AC output to the load and the DC link voltage. [8, 13]

The grid or load interaction of the type 4 WTS is managed by the grid side inverter, which is a DC-to-AC converter controlled as an active voltage source. The topologies introduced for grid voltage source inverters for high-power WTS are single-cell high-power multi-level converters or multi-cell medium-power parallel-connected converters. The main difference in utilizing control techniques is the generation of switching signals. Therefore, to control the dynamics of grid or load interconnection, a control layout used in one can be used in other topologies. [6, 13]

### 1.2.3 Control layout of grid side inverter

In the first step, of designing the controller, an average model of the inverter and plant will be used and the effect of the modulator will be neglected. This is done to simplify the controller design, while still including the modulator in the physical system. This makes configuring two loops in cascade, managing both DC input and AC output by generating a command based on the reference provided by the previous loop. [6, 13]

In the second step, since designing this cascade controller is difficult, by designing the outer loop to be slower in generating reference for the inner loop, two tasks can be processed in two decoupled cascaded loops. Considering these three steps, a generical visualization of VSI is shown in figure 1.4. [6, 13]

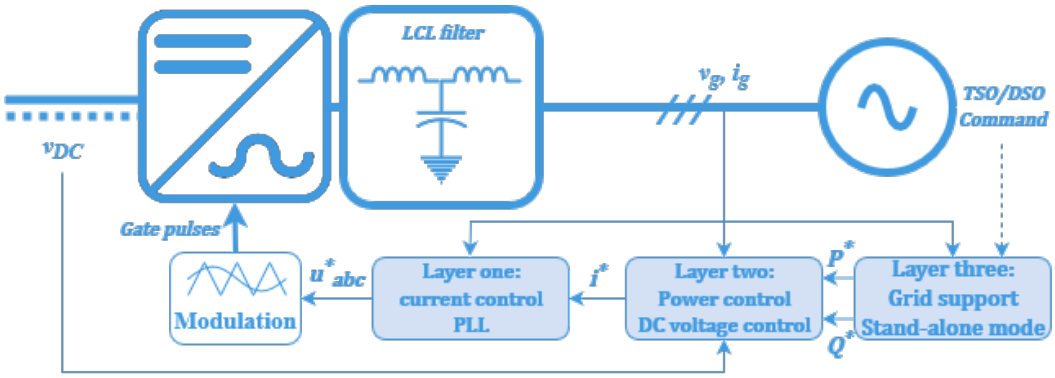


**Figure 1.4:** Controller layout of Grid-connected voltage source inverter

The outer loop controls the active and reactive power directly, or indirectly by controlling the DC link voltage, or both. The inner loop controls the power conditioning on the converter's AC power or current output by managing the voltage output. The cascade structure provides the reference value for the next inner control loop. Additional loops can be included to make additional regulations and the outputs can be decided to aim different operations. The VSI can operate to be connected to the main grid, stand-alone loads, or microgrids. When connected to the main grid, the VSI controller can be designed to provide the grid with additional services and support. [6, 13]

## 1.3 Problem Statement

More integration of WPP into the grids is done with large offshore WPPs to compensate for the presence of traditional plants. VSI, the means to grid interaction, and its controller usually located in the onshore substation, is sensitive to distortions at the PCC. For this, the industry had to do more adjustments to mitigate fault ride through, supply, service, and support delivery standards. [13]

The sensitivity to voltage distortion is due to the controller's configuration, so-called voltage-oriented control (VOC). The distortion from the grid affecting the GCVSI controller performance is not only limited to disturbing the service control and regulation or FRT but also affects the quality of the supply. The distortions can affect the controller dynamics and stability, causing the disconnection of plants and loss of capacity. Two of the common distortions affecting the power quality on the grid side are unbalanced voltage profiles and harmonics at PCC. [12]

In the traditional power system unbalanced transmission line impedance, unbalanced loading, electromagnetic equipment, switching equipment, and power factor correction equipment were mainly the sources that caused the distortions. The power electronic devices integrated into the power system are also one of the reasons for these distortions, and the more they appear in the power system, the more distortions will be introduced. [14]

These voltage distortions cause increased losses, conductor heating, insulation stress, malfunctioning protection controllers, and reduced equipment efficiency and lifetime. Moreover, it causes synchronization problems in the phase-locked loop (PLL), distorting the dynamic and stability of the WTS controller when operating in grid-connected mode, which is the main focus of this project. [15]

### 1.3.1 Main Objectives:

The integration of WTS into the grid requires the industry to perform adjustments in GCVSI controllers so they are immune to the distortions. Considering the standards and solutions provided by TSO, DSO, and manufacturers, this project will be

***Analyze the solutions of the industry for operating the grid-connected voltage source inverter of wind turbine systems, under distorted grid conditions.***

This analysis can be performed in the following chapters in multiple stages including:

- Introducing the theory of the unbalanced signal and harmonic waveform.
- Looking into the grid codes to understand the limits of emissions in the system and use them as criteria to verify the modeling.
- Model and simulate an existing system of GCVSI and controller to confirm the theory and solutions.
- Validate the simulations on an experimental setup.

### 1.3.2 Project Considerations

The three-step analysis includes theory, simulation, and experiment and will consider some limits in each step to mainly focus on the main objective.

- In the upcoming chapters when explaining the theory:
    1. From all ENSTO-E and Nordic grid codes, only the requirements for harmonics and unbalanced voltage (IEC-50610 and IEC-16000-3) will be looked into and used as criteria. The requirements for FRT, grid support, and protection will not be investigated.

2. The modeled and experimented system will be a scaled-down 2L-VSI system. This layout, as mentioned exists and has the same configuration for all types of DC/AC inverters. Even in large-scale modular multilevel converters in the onshore power station of wind farms, the main control layout is the same and as it was mentioned in 1.2.3 with additional loops for sub-modules control, etc.
3. The main solution introduced and analyzed is the MSRF-PLL structure and its capability to prevent distortion affecting the controller dynamics.

- When modeling and simulating:

1. The data used will be for a 380 V and scaled-down VSI has a rating of 2.2 kVA. This is done to speed up the analysis when experimenting and will not make a difference in the analysis of the controller. The difference will be in the amount of mitigation required for this voltage and scale.
2. The modeled circuit will be using a constant DC source as input therefore, the level two control will be implemented to provide current reference directly from power reference and voltage.
3. During the modeling, additional assessment is done including stability analysis of the controller and further improving the system with capacitor current feedback active damping (CCAD). This is done because of the unexpected setup instability problem in the lab which is the modeled and simulated system.
4. The simulation investigates the capability of the MSRF-PLL in maintaining the system stability by filtering out the distortions so the inverter remains connected. The other capabilities, power delivery and quality, are only mentioned to highlight the system's need for additional compensation solutions. The analysis only covers distortions robustness for connection and not compensation for quality.

### 1.3.3 Methodology

In order to fulfill the main objectives of the project different methods in the analysis of problems, modeling, and software utilizing is been used.

- The methods of analysis are:

1. Three-step theory, simulation, and experimentation of aspects.
2. Using the standards as evaluation criteria during each step.

3. Applying the methods of implementation in each step to the next one. The simulation and modeling will be based on theory and experiments based on simulation.
4. The conclusions will be confirmed on each step based on the next. The results from the theory will be confirmed by simulation and then by experiment.

- The scientific methods are:
  1. Reference frame transformations to be used in controller synchronization and analysis of unbalanced signals.
  2. Fourier transform and series are used for the analysis of harmonics.
  3. Classical linear PI-based control theory is used for controller design.
  4. Zero-pole placement and time domain analysis is used to analyze the stability and tuning of the controller.
- The used software is:
  1. Simulink is used to implement controller layout in both simulation and experiment.
  2. PLECS is used to perform Fourier analysis and monitoring during simulation.
  3. The dSPACE control desk is used for interfacing and monitoring in experiments.

## 1.4 Conclusion

This chapter introduced the generic topic of the project and the big scope in section 1.1. The concepts related to the topic introduced in 1.2 will be explained in more detail in 2. The methods, 1.3.3, are used in 3, 4, and 5 to theorize, and buildup the concepts while considerations 1.3.2 are applied step by step to achieve an analysis of 1.3.1.

# Chapter 2

# Power quality, VSC control and Evaluation criteria

*First, the specific grid codes required for connection quality and the theory behind them will be introduced. This will be used as evaluation criteria in the next chapter to validate any simulation, the results that will be achieved, and the conclusion that will be made. The second step will be sections about topics regarding the theory of unbalanced three-phase voltage and harmonic emitted voltage waveform. Finally, concepts in SOA including details about GCVSI and its control will be introduced. These sections will be used to introduce the system architecture to be modeled, simulated, and experimented with.*

## 2.1 Grid codes for power quality

The NC-RFG for WPP, which are above 11 kW connected to a high voltage grid, is more strict and requires specific agreements. Based on the guidelines, the calculated margin for unbalanced connection and harmonic emission includes more parameters and tighter constraints that WPP control has to comply with. The limits indicating power quality for grid connection are based on IEC/TR 16000-3-6, IEC/TR 16000-3-7, DS/EN 16000-3-11, and DS/EN 16000-3-12. [16, 17, 18]

Because simulation and experimenting with a large-scale system are out of scope due to the lack of data and equipment, a scaled-down system will be chosen. Because of unbalanced single-phase loadings, emerging electric vehicle (EV) chargers, and residential PVs, voltage unbalance and harmonic emissions in low-voltage distribution grids exist, introducing the same challenges and harms. This means grid codes, DS/EN 50160 NC-RFG based on IEC 16000-3-2 standards, containing the same context but with scaled limits exist plus the same applied configuration for improving the controller. [19, 20]

Since the objective is to analyze the effects of distortion on the GCVSI controller and the same configuration can be applied for any scale, the method of analysis

can be validated using criteria for the scaled-down system. The standards for a scaled-down system can be used based on DS/EN 50160 NC-RFG, based on IEC 16000-3-2 limits for power quality shown in table 2.1. [21, 22]

**Table 2.1:** EN 50610 limits for voltage distortions [21]

| Distortion | EN 50610 limit |
|---|---|
| Voltage Imbalance (VUF) | 2 % |
| Total Harmonic Distortion (THD) | 8 % |
| Even harmonics | n = 2 : 2 %<br>n = 4 : 1 %<br>n = 6 - 24 : 0.5 % |
| Odd harmonics<br>(Multiples of 3) | n = 3 : 5 %<br>n = 9 : 1.5 %<br>n = 15 and 21 : 0.5 % |
| Odd harmonics<br>(Not multiples of 3) | n = 5 : 6 %<br>n = 7 : 5 %<br>n = 11 : 3.5 %<br>n = 13 : 3 %<br>n = 17 : 2 %<br>n = 19, 23 and 25 : 1.5 % |

The voltage unbalance factor means the negative sequence per positive sequence of voltage can exceed up to 2%. It can be seen that the limit for emission increases by the order of the harmonic. [22]

## 2.2 Unbalanced voltage waveform

A general way to understand the unbalanced voltage condition is to compare it to a balanced voltage waveform. This method will break down the three-phase unbalanced voltage vector into balanced components so the difference between the actually balanced vector and additional vectors is able to be distinguished. The tool to perform the analysis is using Lyon transform to map the voltage vector from the phase domain to the sequence domain like equation 2.1. [23]

$$\begin{bmatrix} v^+ \\ v^- \\ v^0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} \tag{2.1}$$

$v^+$, $v^-$, and $v^0$ are called positive, negative, and zero sequence components of the inspected voltage vector, respectively. $v_A$, $v_B$, and $v_C$ are the phasors of the

phase-to-neutral voltages in the phase domain, and parameter $a = e^{j2\pi/3}$, is the phase axis location coefficient. [23]

Equation 2.1 is the main formula for calculating the unbalanced component and it is the method to calculate the sequences in theory and simulation. Moreover, it is needed to calculate the parameter so-called voltage unbalance factor (VUF) calculated in the equation 2.2 which is further used for calculating the limit in evaluation criteria. [23]

$$VUF = \frac{v^-}{v^+} \times 100 \tag{2.2}$$

## 2.3 Voltage harmonic distortion

The main equation of the Fourier transform, decompose a signal into a DC component and the AC harmonic component as it is shown in equation 2.3. [19, 14]

$$v(t) = a_0 + \sum_{n=1}^{\infty}(a_n \cos\frac{2\pi nt}{T} + b_n \sin\frac{2\pi nt}{T}) \tag{2.3}$$

$v(t)$ is the main voltage waveform, $a_0$ is the DC offset component meaning how much the mean value of the signal is shifted. The formula decomposes the $v(t)$ into two periodic terms, $a_n$ is the amplitude for cosine-shaped harmonics, and $b_n$ is the amplitude of sinusoidal harmonics. The parameter $n$ is a natural number, indicating the order of harmonic as the $n^{th}$ multiple of the fundamental frequency. [14]

The parameters $a_n$ can be calculated using equation 2.3 to calculate the parameter called total harmonic distortion (THD). This parameter is used in grid code with a margin, indicating the limit of harmonic emission in voltage waveform to comply with grid connection criteria. THD can be calculated using equation 2.4. [24, 21]

$$THD = \sqrt{\frac{\sum_{n=2}^{\infty} a_n^2}{a_1^2}} \tag{2.4}$$

In this equation, the parameter $v_n$ is the amplitude of the $n-th$ order harmonic, $v_1$ is the amplitude of the fundamental voltage, and THD is obtained in percent. The calculation of harmonic magnitudes and THD can be performed using PLECS software which is used for both simulation and experimentation. [21]

## 2.4 Grid side inverter topology

The scaled-down converter chosen to analyze the control of GCVSI is a two-level voltage source inverter (2L-VSI). A Schematic of a grid-connected 2L-VSI is shown in figure 2.1. [9]

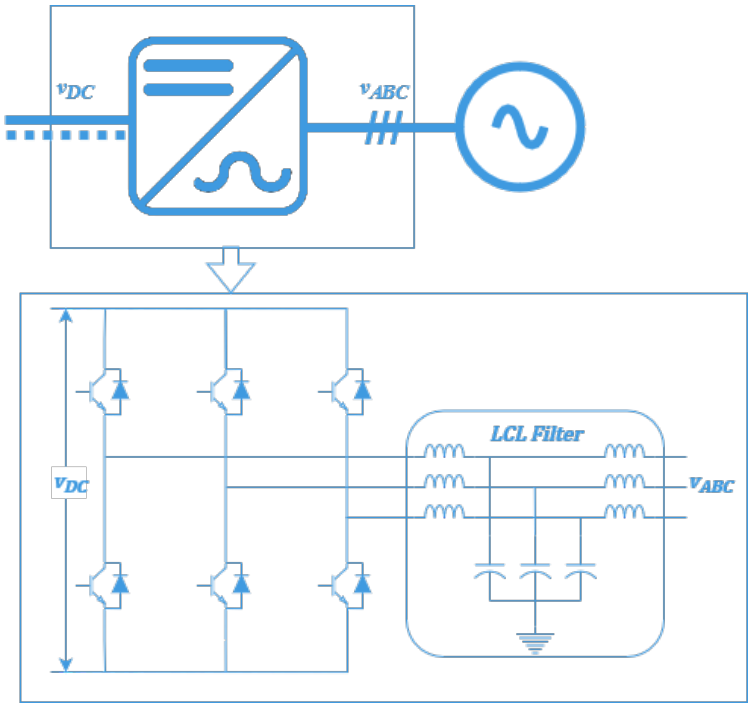


**Figure 2.1:** Structure of a two-level voltage source inverter

There are six switches in total in a 2L-VSI, two per leg and one on each arm without a neutral point. The ratings of the inverter and its filter are shown in table 2.2. [25, 26]

**Table 2.2:** Grid-connected inverter circuit properties

| Parameter | Value | Ratings [pu] |
|---|---|---|
| Nominal power (S) | 2.2 kVA | 1 |
| DC voltage (vdc) | 690 V | $2.125 \cdot \sqrt{\frac{2}{3}}$ |
| AC voltage ($v_{l2l.rms}$) | 380 V | 1 |
| Converter side inductance ($L_1$) | 1.8 mH | 0.0086 |
| Grid side inductance ($L_2$) | 1.8 mH | 0.0086 |
| Filter capacitance ($C_{\Delta.connected}$) | 9 $\mu F$ | 0.00013 |
| Sampling frequency | 10 kHz | - |

The choice of parameters is based on the experimental setup where the choice for switching frequency is equal to the IGBTs switching frequency. [7]

## 2.5 Control structure of inverter

The options for modulation techniques include square wave modulation, sinusoidal pulse width modulation (SPWM), and space vector modulation (SVM). The most common ones are SPWM and SVM where in this project for simplicity and more focus on controller layout. The SPWM technique generates the switching commands by synthesizing the duty cycle using a carrier. When the carrier is larger than the duty cycle, the upper switch is on; when it is less, the lower switch is on. [25]

After the choice of the modulator, the controller architecture is to be decided loop by loop. Primarily, the converter and sensors will be modeled as an ideal unity gain and only the modulator will be considered in the diagram. Secondly, the effect of the capacitor in the plant can be neglected due to the identical behavior of LCL and L filters at 50 Hz. Moreover, since one of the most utilized controllers is the PI controller, Clark transform is used to transform three-phase signals to DC. [7, 25]

To utilize Park transform, an additional loop, called the phase-locked loop (PLL), is needed to extract the instantaneous phase-angle of three-phase signals. Finally, although the transfer function of the sensors, modulator, and actuator is considered a unity gain, their delay affects a real system. This delay is modeled by a unit delay and a zero-order-hold (ZOH) in "z domain" and can be modeled using Pade approximation to "s domain".[7, 25, 27]

Considering all the conditions above, the standard layout of the current controller is represented in figure 2.2.

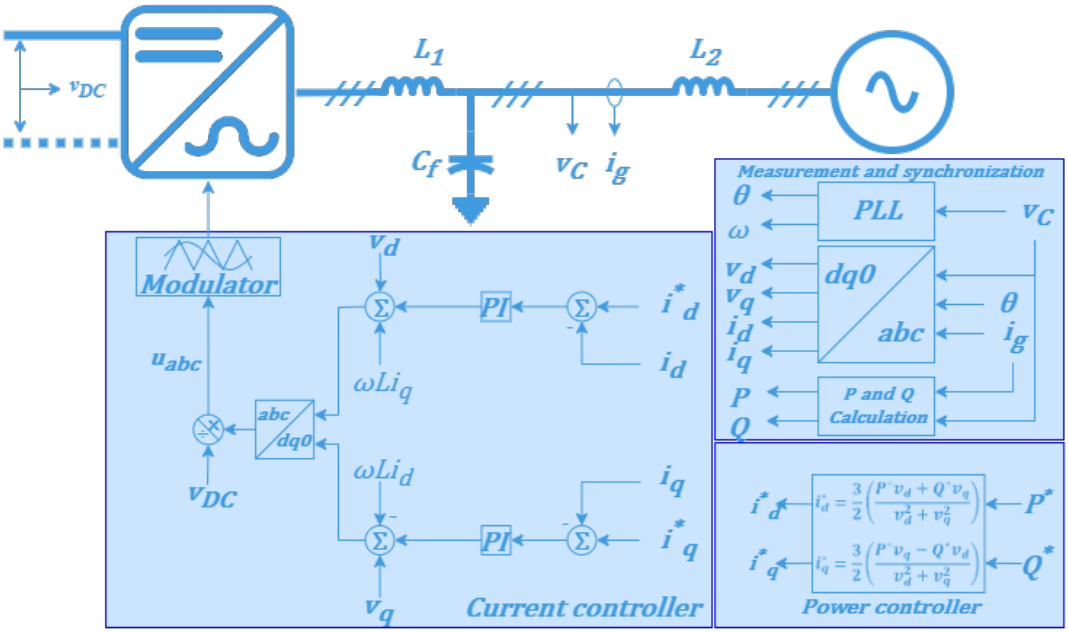


**Figure 2.2:** Controller layout of grid-connected VSI

The reference currents are provided from the second layer of control. The PLL, extracting the phase angle to synchronize the controller, and the feed-forward stage are implemented to enhance dynamic response and disturbance rejection. However, if the feed-forward term, contains oscillations, it will disturb the dynamic and stability of the controller. Therefore, the capability of the controller to prevent distortion affecting this stage is needed. [7]

In order to obtain the references, the instantaneous three-phase power theory can be used. If the reference power is known the current references can be obtained using equation 2.5 and 2.6. [7]

$$i_d^* = \frac{2}{3}\frac{P^* v_d + Q^* v_q}{v_d^2 + v_q^2} \tag{2.5}$$

$$i_q^* = \frac{2}{3}\frac{P^* v_q - Q^* v_d}{v_d^2 + v_q^2} \tag{2.6}$$

Since the modeled system considered a constant voltage source as a DC supply, there is no need for a DC voltage controller in the second level and the power controller can use algebraic equations, 2.5 and 2.6, to provide current references. The configuration for adjusting the distortion is done in the current control level and the main focus will be designing this control layer. [7, 25]

### 2.5.1 Grid synchronization using PLL

The layout of the additional loop needed for synchronization by extracting the phase angle of a three-phase signal, as known as PLL, is shown in figure 2.3. [7]

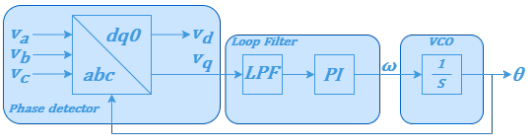


**Figure 2.3:** Structure of PLL

The standard PLL shown in figure 2.3 is made of three stages. The phase detection stage includes Park transform which transforms input to DC. The loop filter stage includes the PI controller eliminating the error between frames and the last stage. [25]

Theoretically, when a balanced three-phase input is changed to constant components using Park transform, the output will be the $d$ component equal to the magnitude of three voltage signals and the $q$ component is zero. This is the basic principle of the PLLs phase detector, shown in equation 2.7. [7]

$$v_{dq0} = [T_{dq0}] \times v_{abc} \tag{2.7}$$

where $[T_{dq0}]$ is the transformation matrix and $v_{abc}$ is a pure sinusoidal three phase signal that $v_a = v_{mag} \sin\theta$, $v_b = v_{mag} \sin(\theta - \frac{2\pi}{3})$ and $v_c = v_{mag} \sin(\theta + \frac{2\pi}{3})$. $v_{mag}$ is the magnitude of the voltage vector and $v_{dq0}$ will be obtained $v_d = v_{mag}$, $v_q = 0$ and $v_0 = 0$ which are DC values and can be processed in the controller. [7]

If there is a difference in the magnitude of the phase voltages, an oscillating time-dependent term will appear in the generated $d$ and $q$ output, making them oscillatory too. Considering a sinusoidal three-phase voltage with $VUF = \epsilon$ based on standards, according to equation 2.2 has a positive sequence of $v_{Mag}$ and a negative sequence of $\epsilon$.[23]

The unbalance three-phase component can be modeled with a three-phase sinusoidal rotating in the opposite direction of the positive sequence. Therefore, The oscillatory terms can be shown in the equation 2.8. [7, 28]

$$\begin{bmatrix} v^d \\ v^q \\ v^0 \end{bmatrix} = [T_{dq0}] \times \begin{bmatrix} v_{mag} \cdot \sin\theta + \epsilon \cdot \sin(\theta + \phi) \\ v_{mag} \cdot \sin(\theta - \frac{2\pi}{3}) + \epsilon \cdot \sin(\theta + \frac{2\pi}{3} + \phi) \\ v_{mag} \cdot \sin(\theta + \frac{2\pi}{3}) + \epsilon \cdot \sin(\theta - \frac{2\pi}{3} + \phi) \end{bmatrix} = \begin{bmatrix} v_{mag} - \epsilon \cdot \cos 2\theta + \phi \\ \epsilon \cdot \sin 2\theta + \phi \\ 0 \end{bmatrix} \tag{2.8}$$

In equation 2.8, $\epsilon$ is the magnitude of the negative sequence, and $\phi$ is the phase of the negative sequence. The initial phase of $v_b^-$ is $+\frac{2\pi}{3}$ and $v_c^-$ is $-\frac{2\pi}{3}$, indicating the negative rotation. It can also be seen that the $d$ and $q$ components are

not constants and their value oscillates. These oscillatory terms appear as components rotating with a speed of double the synchronous frame speed going through the controller into the duty cycles and this is how unbalanced voltage makes the controller malfunction.

An easy way to prevent this is to add another loop in the phase-detector stage to extract the negative sequence component. This can be done by using the same concept to extract a three-phase signal's positive and negative sequence to decouple two rotating reference frames [25]. There are different concepts for improving phase detectors introduced in [7], [29] and chapter 39 of [25]. The multi-synchronous reference frame (MSRF) is used in this project since it is the most straightforward, easy to implement, and modular concept. The idea of decoupling sequences is used by first transforming the input voltage to the stationary frame using equation 2.9, then extracting and subtracting the negative sequence as equation 2.9 [30].

$$v_{\alpha\beta0} = [T_{\alpha\beta0}] \times v_{abc} = v^{+}_{\alpha\beta0} + v^{-}_{\alpha\beta0} \tag{2.9}$$

The parameter $v_{\alpha\beta0}$ is the input voltage vector in stationary frame, $v^{+}_{\alpha\beta0}$ is the positive sequence component of input and $v^{-}_{\alpha\beta0}$ is the negative sequence of it. To calculate them, the $v_{\alpha\beta0}$ is transformed into $v_{dq0}$ in two rotating frames, one aligned with $+\theta$ and the other one to $-\theta$, then reverse transformed using the same rotating frame to stationary frame, obtaining the sequences of $v_{\alpha\beta0}$ in the following equations. [30]

$$v^{\pm}_{\alpha\beta0} = [T^{-1}_{dq0}] \times ([T_{dq0}] \times (v_{\alpha\beta0} - v^{\mp}_{\alpha\beta0})) \tag{2.10}$$

Primarily, it is important to consider that calculation of each sequence requires the other one to be calculated before. There is a constant error in the calculation because $v_{\alpha\beta0}$ containing both sequences, appears in the cross-pre-calculation stage. The parameters $v^{'+}_{\alpha\beta0} = v_{\alpha\beta0} - v^{-}_{\alpha\beta0}$ and $v^{'-}_{\alpha\beta0} = v_{\alpha\beta0} - v^{+}_{\alpha\beta0}$ are introduced to distinguish the terms containing this error and the main decoupled term. [30, 28]

Secondly, as was shown in the equation 2.8, when rotating frames are aligned to one of the sequence components, the presence of the other sequence will cause oscillatory terms. This oscillatory term rotates at double the speed of the frame and will remain in the transformed vector when transforming from a stationary to a rotating frame and vice versa. [30, 28]

In order to lower these two errors from $v^{'+}_{\alpha\beta0}$ and $v^{'-}_{\alpha\beta0}$ to calculate the actual positive and negative sequences, a low pass filter is needed to interface the two Clark transform section. With these considerations, The structure of the decoupled phase-detection is implemented and shown in figure 2.4. [28]

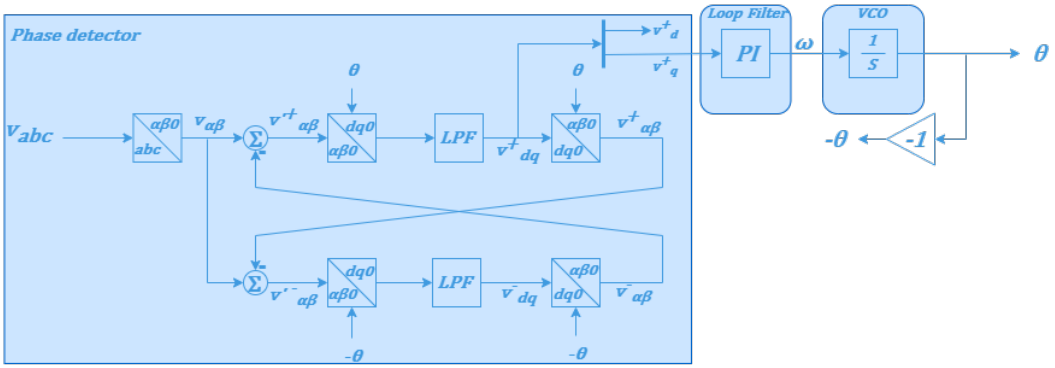


**Figure 2.4:** DSRF-PLL structure

It can be seen that the new phase-detection stage can decouple the frequency of the fundamental and negative sequence. If the loop filter input is set to extract $v^{+}_{dq0}$, the phase angles for both sequences can be obtained. The structure is known as a double synchronous reference frame PLL (DSRF-PLL) which is one of the existing architectures with a phase detector able to decouple the sequences. [25]

### 2.5.2 Selective harmonic filtering using MSRF-PLL

Harmonic terms can still affect the DSRF-PLL phase detector. Harmonics appear in the voltage of each phase as additional sinusoids with an angular speed of $\omega_n = n \cdot \omega$ and phase of $\varphi$ [25]. In theory, when the phase detector of SRF-PLL is experiencing the presence of $n^{th}$ order harmonic with the magnitude of $h$ in an input, the $v_{dq0}$ obtained to be used in the controller can be calculated using equation 2.7. [7]

$$\begin{bmatrix} v^d \\ v^q \\ v^0 \end{bmatrix} = [T_{dq0}] \times \begin{bmatrix} v_{mag} \cdot \sin\theta + h \cdot \sin(n\theta + \varphi) \\ v_{mag} \cdot \sin(\theta - \frac{2\pi}{3}) + h \cdot \sin(n\theta - \frac{2\pi}{3} + \varphi) \\ v_{mag} \cdot \sin(\theta - \frac{2\pi}{3}) + h \cdot \sin(n\theta + \frac{2\pi}{3} + \varphi) \end{bmatrix} = \begin{bmatrix} v_{mag} - h \cdot \cos((n-1) \cdot \theta + \varphi) \\ h \cdot \sin((n-1) \cdot \theta + \varphi) \\ 0 \end{bmatrix} \tag{2.11}$$

where can be seen the appearing oscillating terms are not rotating at $\omega = 200 \times \pi$ but their angular speed is multiple of $n-1$ where $n$ is the harmonic order. The decoupling and filtering stages of the DSRF-PLL phase detector cannot filter out these terms since they are tuned to the fundamental frequency of the input. [7]

In order to exclude the oscillations from the higher frequencies, the similar concept from 2.4 can be used to extract the desired components and subtract them to obtain the fundamental [30]. For start, the general version of equation 2.9 can be written as

$$v_{\alpha\beta0} = [T_{\alpha\beta0}] \times v_{abc} = v_{\alpha\beta0}^{1+} + v_{\alpha\beta0}^{h1} + v_{\alpha\beta0}^{h2} + \cdots + v_{\alpha\beta0}^{hn} + v_{\alpha\beta0}^{-1} + v_{\alpha\beta0}^{-h1} + \cdots + v_{\alpha\beta0}^{-hn} \tag{2.12}$$

where in addition to unbalance, there are harmonic emissions in both sequences. This is the third consideration for improving the phase detector in order to extract harmonics, in unbalanced conditions, harmonics will affect both sequences appearing as two terms of $v_{\alpha\beta0}^{hn+}$ and $v_{\alpha\beta0}^{hn-}$. [30]

The same concept of the DSRF-PLL phase detector can be advantageous as it can be expanded to extract and subtract harmonic and unbalanced terms to obtain the fundamental positive sequence component [30]. Therefore, in a similar first step, a specific harmonic term can be calculated by subtracting the rest from the main input [30]. To obtain an individual term, for instance, $k^{th}$ order harmonic in both sequences, two reference frames with the speed of $\pm\omega_{hk} = \pm k \cdot \omega_{\pm1}$ are used to extract $\pm k^{th}$ components of $v_{\alpha\beta0}$ as $v_{dq0}^{hk\pm}$. By inverse transforming $v_{dq0}^{hm\pm}$ to stationary frame, $v_{\alpha\beta0}^{hm\pm}$ can be obtained as [28]

$$v_{\alpha\beta0}^{hk+} = [T_{dq0}^{-1}] \times ([T_{dq0}] \times (v_{\alpha\beta0} - (\sum_{1}^{n\neq k} v_{\alpha\beta0}^{hm+} + \sum_{-n}^{-1} v_{\alpha\beta0}^{hm-})) \tag{2.13}$$

$$v_{\alpha\beta0}^{hk-} = [T_{dq0}^{-1}] \times ([T_{dq0}] \times (v_{\alpha\beta0} - (\sum_{1}^{n} v_{\alpha\beta0}^{hm+} + \sum_{-n\neq-k}^{-1} v_{\alpha\beta0}^{hm-})) \tag{2.14}$$

where similar considerations for filtering out the errors from the Clark transformation and cross-calculation section are needed. Additional parameters terms containing the error of input and cross calculation introduced as [28]

$$v_{\alpha\beta0}^{'hk+} = v_{\alpha\beta0} - (\sum_{1}^{n\neq k} v_{\alpha\beta0}^{hm+} + \sum_{-n}^{-1} v_{\alpha\beta0}^{hm-}) \tag{2.15}$$

$$v_{\alpha\beta0}^{'hk-} = v_{\alpha\beta0} - (\sum_{1}^{n} v_{\alpha\beta0}^{hm+} + \sum_{-n\neq-k}^{-1} v_{\alpha\beta0}^{hm-}) \tag{2.16}$$

that will be transformed and filtered to obtain $v_{\alpha\beta0}^{hk\pm}$. The phase detector of DSRF now can be expended as shown in figure 2.5. [30]

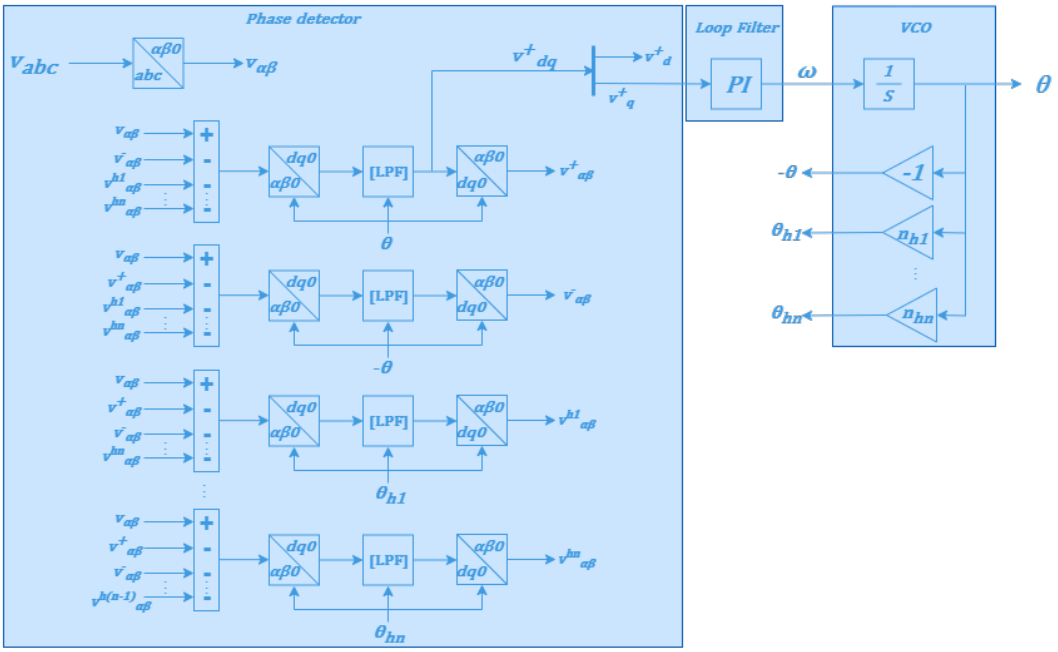


**Figure 2.5:** MSRF-PLL structure

In the new architecture, similar loops including cross subtractions and filters are added to eliminate harmonics in both sequences. The loop filter input is set on the loop calculating the fundamental positive sequence and phase angle for the fundamental positive sequence and other harmonics in sequences can be obtained accordingly. Since more than two reference frames are involved in extracting and filtering components, the improved concept is known as multiple synchronous reference frame PLL (MSRF-PLL). The filters for each loop are tuned with cutoff frequency according to the target harmonic frequency to be extracted. [30, 29, 28]

The MSRF-PLL structure has the advantage of being easy to implement, straightforward theory, and modularity. These advantages made this structure the suitable PLL structure to choose from.

## 2.6 Conclusion

This chapter introduced the different aspects of the project in theory which will be used in chapter 3 to simulate, evaluate and analyze. Section 2.1 is used for evaluating and modeling the distortions, and section 2.4 and 2.5 include the theory of the systems and subsystems to be simulated plus addressing the part of the system that can be affected by distortion.

# Chapter 3

# Controller and modeling validation

*In this chapter, the subjects in the previous one, theory, and evaluation criteria 2 will be validated by comparing the results from the calculation and the simulation. In the first section, the modeled layout of the controller will be evaluated focusing on the current controller and PLLs configuration for none distorted conditions. The second section will focus on the effect of modeled grid distortion on PLLs specifically.*

## 3.1 Current controller configuration

The design procedure starts with introducing the basic diagram of the system and considerations in section 2.5. The configured diagram for the current controller tuning is represented in 3.1. [25]

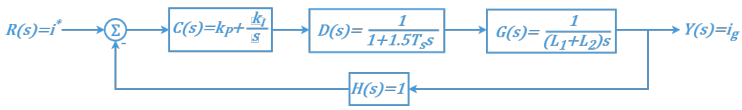


**Figure 3.1:** Current controller system diagram design

The controller transfer function for the PI controller is $C(s) = k_P + \frac{k_I}{s}$, where $k_P$ is the proportional gain and $k_I$ is the integrator gain. The first-order delay and ZOH are modeled as 1.5 times the sample time using the Pade approximation, represented as $D_s = \frac{1}{1+1.5T_s s}$ where $T_s$ is the sample time. Finally, a simplified transfer function of the filter is used which will be $G_s = \frac{1}{Ls}$ where $L$ is the inductor value. $i_s^*$ is the transferred reference current and $i_s$ is the sensed output current. [7, 27]

The general design criteria with a damping ratio= $\frac{1}{\sqrt{2}}$ and an overshoot of 5%. The frequency response of the system for design criteria is shown in figure 3.2.[27]

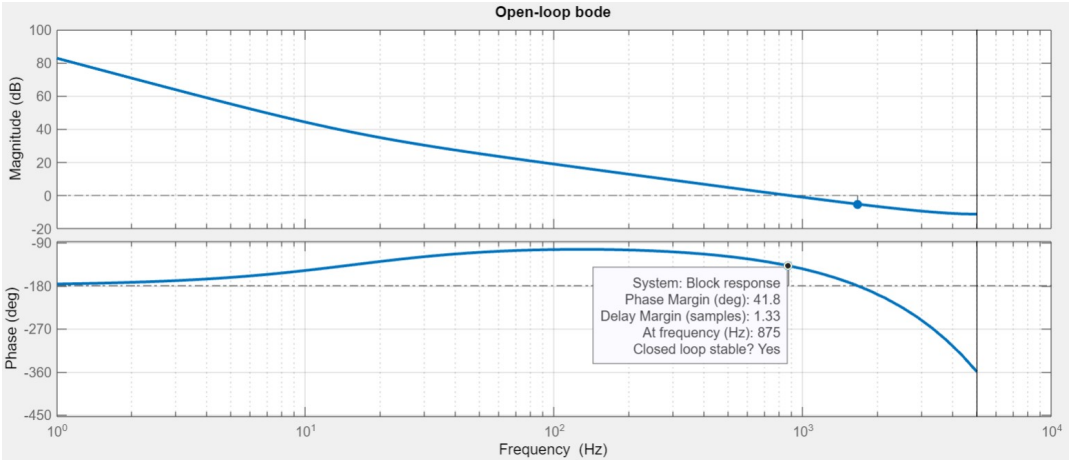


**Figure 3.2:** Current controller bode

The bode diagram represents the open loop system response, the bandwidth of the system can be seen at magnitudes zero crossing, $875Hz$, and the phase of the system at the point will be the phase margin, 42 deg. [27]

The tuned PI is discretized so it is easier to implement in the controller, considering the digital signal processor operates with a sampling rate of $0.1ms$. The tuned controller, $G_{PI} = 20 + \frac{0.1}{z-1}$, requires additional considerations to ensure the safety and stability of the design.

### 3.1.1 Controller stability analysis

In order to perform the stability analysis, a detailed model of the system is required which includes the capacitor in the diagram, shown in figure 3.3. [27]

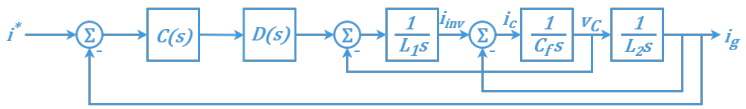


**Figure 3.3:** Detailed current controller with LCL filter

The figure demonstrates the effect of capacitor current, $i_C$ and to analyze the transient behavior of the controller, the frequency response of the system is shown in figure 3.4.

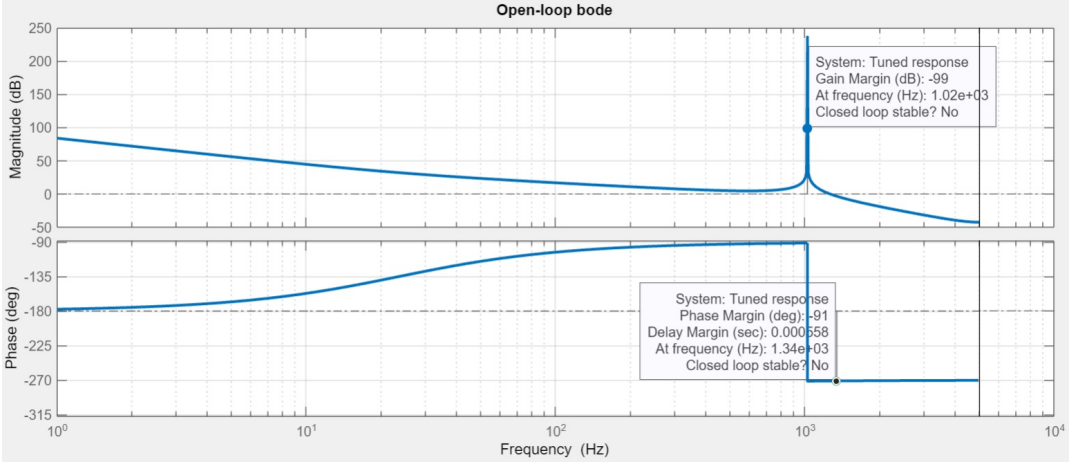


**Figure 3.4:** Open loop bode plot of the current controller

The open loop bode plot in figure 3.4 shows the peak of magnitude appearing at the resonance frequency of LCL filter, $f_r = \frac{1}{2\pi}\sqrt{\frac{1}{C_f}(\frac{1}{L_1}+\frac{1}{L_2})} = 1020.97Hz$. Generally, the loop is unstable at this resonant frequency, giving the system a negative phase jump that crosses $-180\,\text{deg}$. The effect of this additional pole is more obvious using the root-locust of the discrete closed-loop system in figure 3.5. [27, 7]

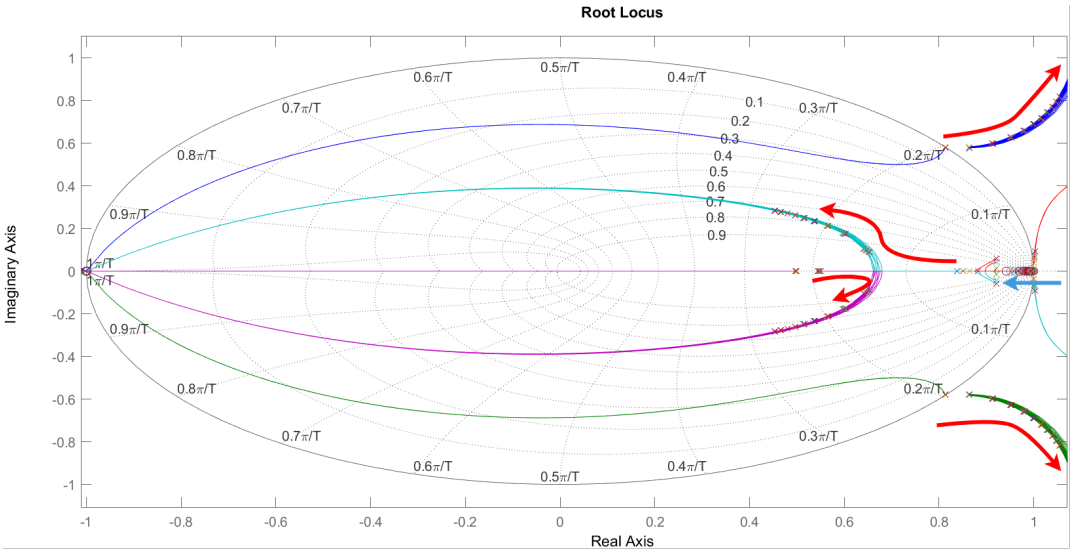


**Figure 3.5:** Close loop root-locust of the current controller

Figure 3.5 is made in a way that the poles and zeroes are plotted in groups for different proportional and integral gains. An increase in the proportional gain moves the group of poles along the loci towards zeros at $[1, 0]$ and $[-1, 0]$. The integral gain tightens the loci so the groups of poles are becoming closer to the

unity circle's stability margin and moving the zero at $[1, 0]$ towards the center. For better observation, the effect of the increase of each individual gain is also shown in the zero pole map in figure 3.6 and 3.7. [27]

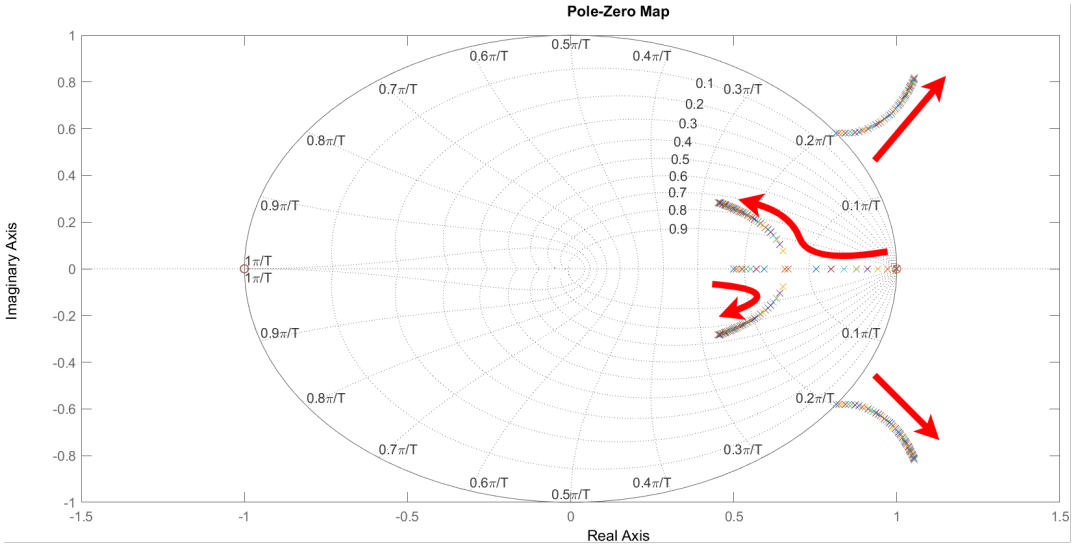


**Figure 3.6:** Close loop zero pole map with constant $k_I$ and varying $k_P$

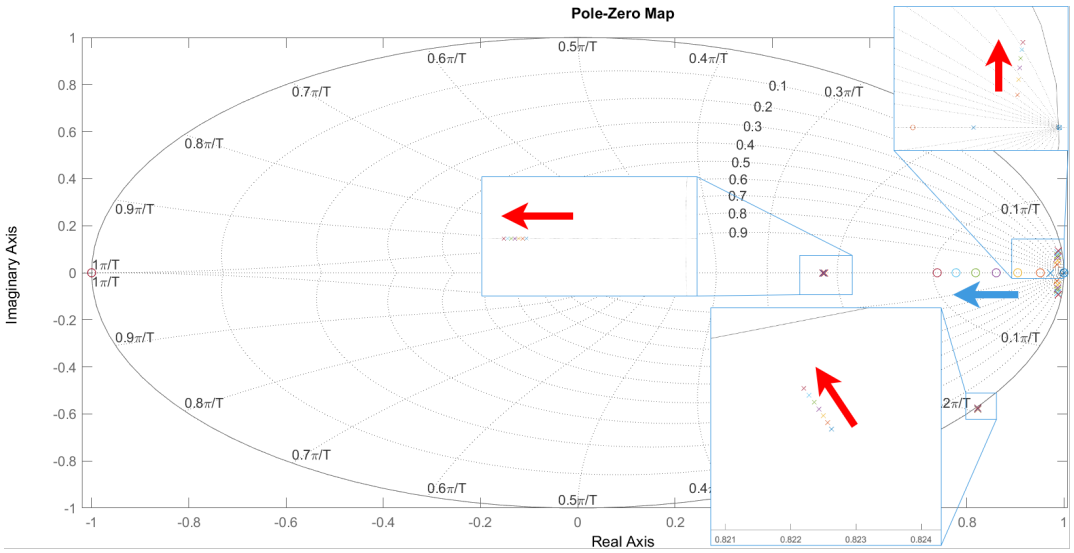


**Figure 3.7:** Close loop zero pole map with constant $k_P$ and varying $k_I$

By comparing figure 3.6 and 3.7, it can be seen that the proportional gain moves the poles (red arrows) along the loci while the integrator gain affects the poles less and moves the zero (blue arrows) towards the origin. Considering this and the

loci path in figure 3.5, the poles move around and away from the unity circle. This analysis shows that for all the values for $k_P$ and $k_I$, the system will become unstable during startup transient, and therefore, additional considerations are needed. [25, 31]

### 3.1.2 Capacitor current feedback active damping

In order to resolve the system stability challenge, damping the resonance peak is the necessary approach. These methods introduced in [7], chapters 8 and 38 in [25], and [27] are known as active or passive damping methods. Since the system of choice includes sensors to measure both inverter side and grid side current, a very simple and straightforward method of damping, the so-called capacitor current feedback active damping (CCAD) method, is chosen. Implementation of the capacitor current feedback active damping is shown in figure 3.8. [7]

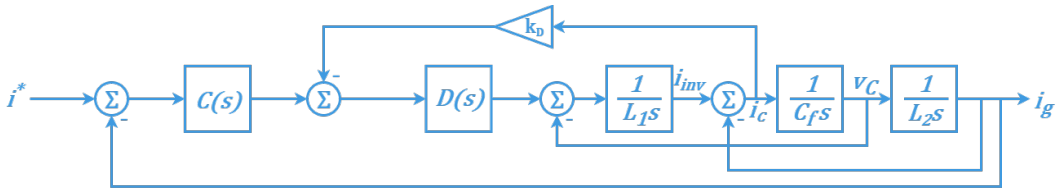


**Figure 3.8:** System diagram including CCAD configuration

Figure 3.8 shows that $i_C = i_{inv} - i_g$, which gives the capacitor current, and the gain $k_D$ acts as a virtual resistor. In this way by the ohms law, $k_D \times i_C = v_C$ is added to the voltage feed-forward stage of the controller which takes the voltage drop over $L_1$, caused by the capacitor, into account. From the inverter's perspective, the presence of the capacitor will not be sensed, causing the extra pole to be damped, and therefore the system will be stable if $k_D$ is well-tuned. [27, 25]

The close loop system zero pole map can be used to observe the effect of increasing $k_D$ in figure 3.9.

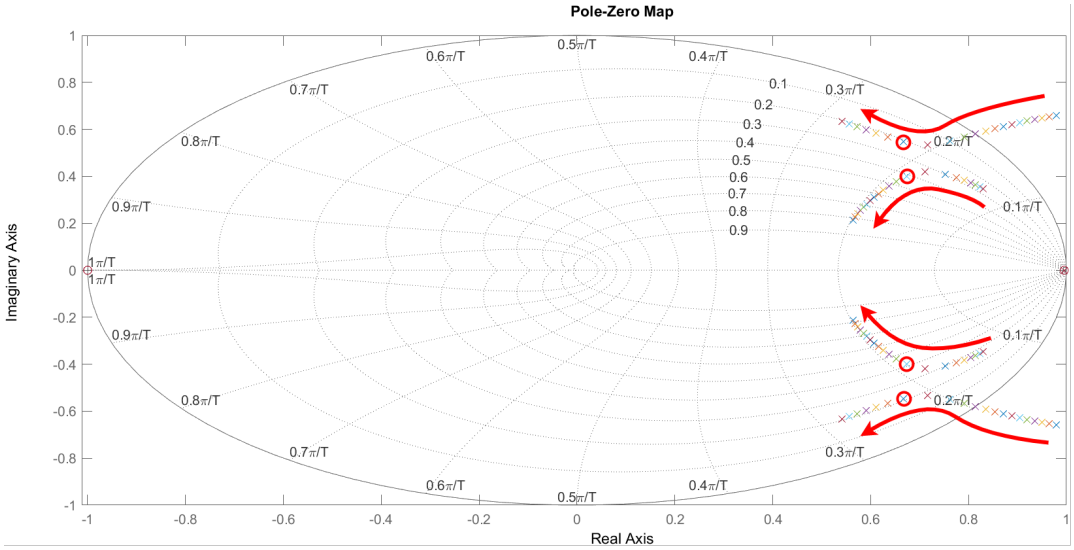


**Figure 3.9:** Close loop system zero pole map for different values of $k_D$

Figure 3.9 demonstrates minimum $k_D = 12$ is required for design configuration in 3.1. The damping can be increased but according to figure 3.9, optimal damping for this configuration can be achieved when $k_D = 15$ [7]. In addition, a trade-off must be made to compensate for the over-current when implementing the system. This is because the protection system of the VSI is set to trip the inverter for currents over $21A$ and if the dynamics of the current controller are not fast enough, it will cause the system to trip. Considering this, the design configuration can be summarized in table 3.1.

**Table 3.1:** Current controller design parameters

| Parameter | Value |
|---|---|
| Settling time | 4 ms |
| Overshoot | 41 % |
| Phase Margin | 35° |
| Bandwidth | 600 Hz |
| Sampling time | 0.1 ms |
| CCAD constant ($k_D$) | 15 |
| Discretized controller | $G_{PI} = 25 + \frac{0.09}{z-1}$ |

Table 3.1 shows the final configuration of the current controller where optimal CCAD is utilized and the trade-off between overshoot, phase margin, and bandwidth is made to compensate for the fast action of the current controller and overcurrent. It can be seen that the phase margin is reduced to 25 deg while the bandwidth is increased to $600Hz$, as is shown in figure 3.10, but the 41% overshoot

is more aggressive.

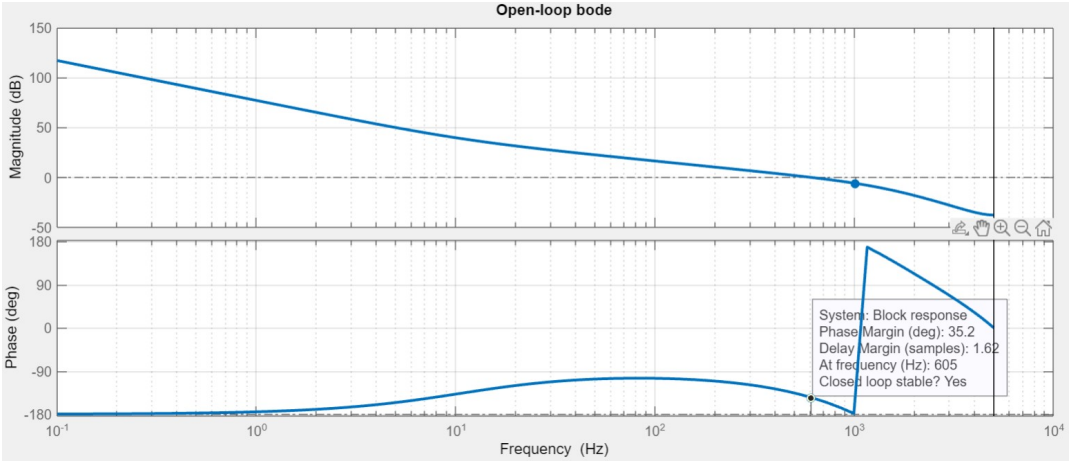


**Figure 3.10:** Open loop bode of the current controller configuration

In figure 3.10 the damped resonance peak can be seen, allowing choosing a higher bandwidth for the system. The magnitude zero crossing indicates the bandwidth of $600Hz$ and phase margin of 25 deg as a tradeoff. The stability of the system can be insured by observing the zero pole plot of the system in Figure 3.11.

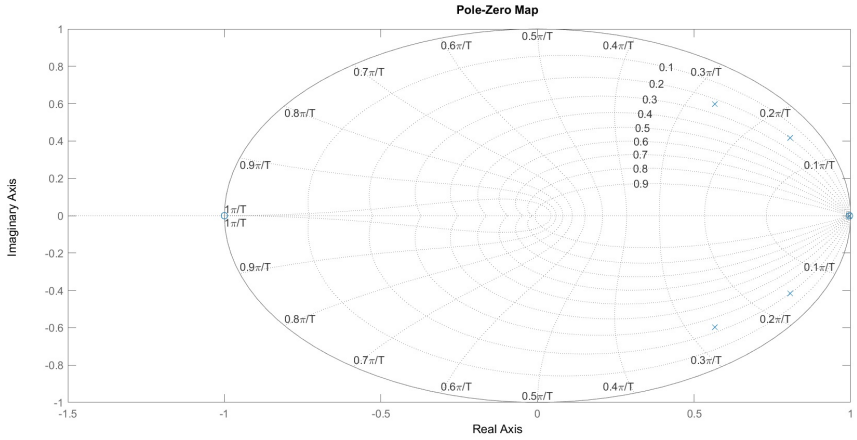


**Figure 3.11:** close loop current controller zero pole map

Figure 3.11 shows that the poles of the close loop are damped inside the stable region and moved a bit toward their loci, shown in figure 3.9 as the gain of the system is increased.

## 3.2 PLL configuration

The additional loop of PLL includes a PI controller which also requires tuning. There are two PLL structures selected, SRF-PLL and MSRF-PLL and in order to tune them, their block diagrams have to be linearized as a small signal diagram.

### 3.2.1 SRF-PLL configuration

The linearized small signal feedback control diagram of SRF-PLL in figure 2.3 is made based on the linear feedback control diagram similar to figure 3.1. The difference is the input and output are set as the phase angle error because the phase angle output of the system is a ramp function. Considering this, the linearized small signal diagram can be made as figure 3.12. [7]

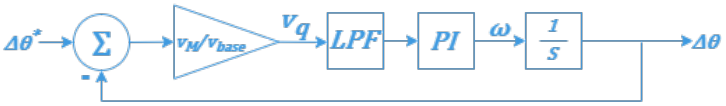


**Figure 3.12:** Linearized system diagram of SRF-PLL

The linearized system diagram includes the exact model of the loop filter and VCO, and the linearized model of the phase detector. When there is no phase angle error and the system is in a steady state, the $v_q$ component can be approximated as $v_M \cdot sin(\Delta\Phi) = \frac{v_M}{v_base} \cdot \Delta\Phi$ where $\frac{v_M}{v_base}$ is the unified magnitude of the voltage vector and $\Delta\theta^* - \Delta\theta = \Delta\Phi$ is the phase angle reference tracking error. [7]

The transfer function for $v_q$ can be written as $v_q = v_M \cdot sin(\Delta\Phi) \cdot G_{LPF}$ where $G_{LPF} = \frac{\omega_f}{s+\omega_f}$ is the transfer function of the filter. $\omega_f$ is the cutoff frequency of the filter which considering the topics covered in 2.5.2 is set as $\omega_f = \frac{\omega}{\sqrt{2}}$ where $\omega$ is the angular speed of the voltage vector. [28]

Similar to the current controller, the PLLs PI controller is tuned so the system achieves $\zeta = \frac{1}{\sqrt{2}}$ and $overshoot = 5\%$. The tuned system parameters are shown in table 3.2.

**Table 3.2:** SRF-PLL tuned system parameters

| Parameter | Value |
|---|---|
| Overshoot | 5 % |
| Bandwidth | 1766 Hz |
| Sampling time | 0.1 ms |
| Discretized controller | $G_{PI} = 110 + \frac{0.2}{z-1}$ |

### 3.2.2 MSRF-PLL configuration

For tuning the PI controller for MSRF-PLL, a similar system diagram in figure 3.12 can be used. When setting the loop filter input to the positive sequence extracted, the phase angle extraction is done with the SRF-PLL concept. However, in section 2.5.2 additional considerations were discussed that highlighted the importance of additional filtering in the phase detector. For MSRF, in order to take the filtering delay of additional loops into account, $\omega_f = \frac{\omega_{1+}}{\sqrt{2}}$ where $\omega_{1+}$ is the angular speed of the voltage vector's fundamental positive sequence. [7, 28, 30]

Similar to SRF-PLL system, in steady state and when $\Delta\Phi$ is small, $v_q = v_M \cdot sin(\Delta\Phi) \cdot G_{LPF} = v_M \cdot \Delta\Phi \cdot G_{LPF}$. Considering this, same as SRF-PLL tuning, the PI is tuned so the loop transfer function achieves $\zeta = \frac{1}{\sqrt{2}}$ and $overshoot = 5\%$. The tuned system parameters are summarized in table 3.3. [28]

**Table 3.3:** MSRF-PLL tuned system parameters

| Parameter | Value |
|---|---|
| Overshoot | 20 % |
| Bandwidth | 141.3 Hz |
| Sampling time | 0.1 ms |
| Discretized controller | $G_{PI} = 100 + \frac{0.2}{z-1}$ |

As can be noticed, although the system type remains the same and the controller can achieve zero steady state, a delay is introduced to the loop due to filtering. The new controller for MSRF-PLL requires adjustments to trade between overshoot and delay in tracking.

## 3.3 PLL Validation tests

Before observing the PLLs' performance in the controller, the configuration will be validated on a test bench. The evaluation confirms if PLL configurations can track a step change in amplitude, phase, and frequency. The test summary is shown in table 3.4.

**Table 3.4:** Evaluation test summary for PLLs

| Event | Expected output | | |
|---|---|---|---|
| **Magnitude step:** | $v_d[pu]$ | $v_d[pu]$ | $v_{1+}(MSRF)[pu]$ |
| *1 pu @ t = 0.2 s* | *1* | *0* | *1* |
| *0.5 pu @ t= 0.4 s* | *0.5* | *0* | *0.5* |
| *1 pu @ t = 0.6 s* | *1* | *0* | *1* |
| **Phase step:** | **Phase angle lead** ($\varphi$) | | |
| $\varphi$=+15° @ *t= 0.8 s* | *In phase with* $v_a = sin(\theta + \varphi)$ | | |
| **Frequency step** | **Phase angle period** ($\theta = 2\pi\frac{1}{T}$) | | |
| *f=50+2 Hz @ t=1.2* | *In phase with* $v_a = sin(2 \cdot \pi \cdot 52 \cdot t)$ | | |

Evaluation results for SRF-PLL are shown in figure 3.13.

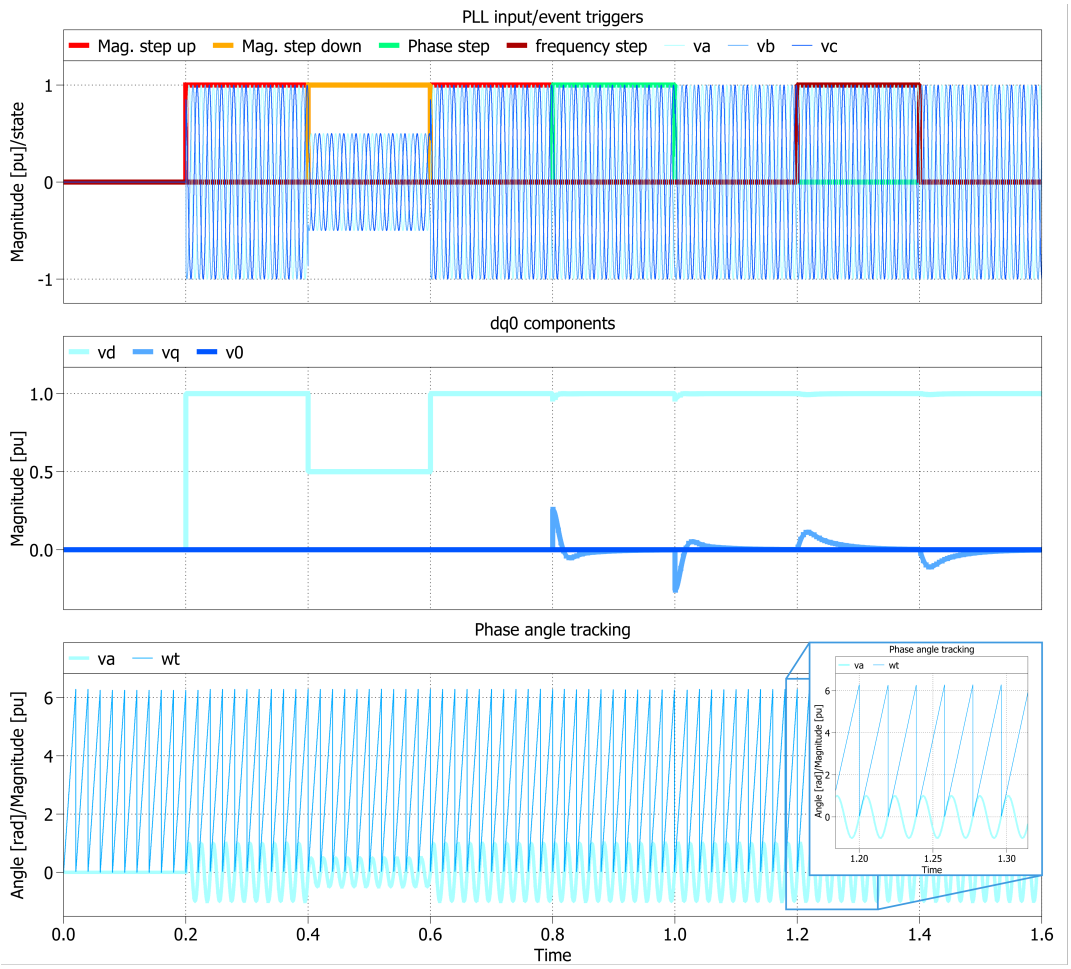


**Figure 3.13:** SRF-PLL evaluation results

Results in figure 3.13 show that SRF response to amplitude steps is with minimum error. However, during phase and frequency steps, a transient error can be seen in $v_q$. It is shown that the angle is always in phase with $v_a$ during all events which means the results for phase and frequency results comply with the criteria in table 3.4. Following, the results for MSRF-PLL evaluation are shown in figure 3.14.

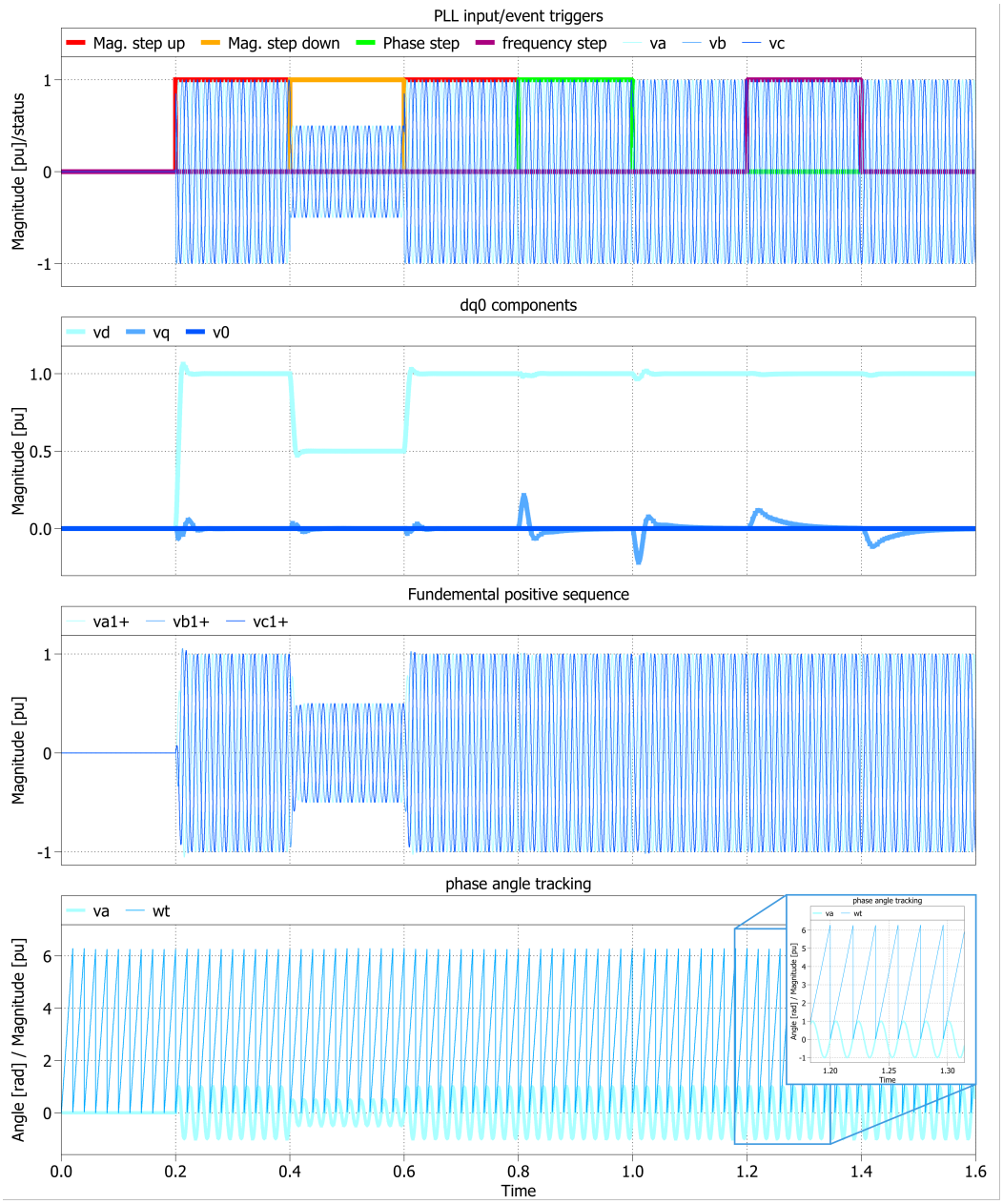


**Figure 3.14:** MSRF-PLL evaluation results

In figure 3.14 the MSRF-PLL response to all events includes a transient error. During amplitude steps, the expected overshoot in the design procedure can be seen, and during phase and frequency steps there is an error in tracking $v_q = 0$. The fundamental positive sequence is in with reference and follows the magnitude and the angle is always in phase and sequence with it during all events. Compared to results from SRF-PLL evaluation in figure 3.13, the trade-off for compensating the MSRF-PLL tracking due to additional filtering causes the difference in tracking amplitude.

## 3.4 VSI controller validation

So far the layout of the controller is introduced in 2.5 and the configuration for individual parts is done in 3.1, 3.2, and 3.2.2. In order to validate the layouts and configuration to be used later, their performance is simulated in software and will be observed. If the theory can be evaluated by simulation, the configured layout is valid to perform further analysis. The validation process is done with a standard scenario, summarized in table 3.5, and monitoring the performance of different parts of the controller including the power controller, current controller, and PLLs.

**Table 3.5:** VSI controller evaluation tests

| Input | Expected output |
|---|---|
| Startup @ t = 0.3 s | $v_d = 1$, $v_q = 0$ |
| $P_{ref}$ = 0.5 pu @ t = 0.5 s | $i_{dref} = i_d = 0.5pu$, $i_a$ in phase with $v_a$ |
| $Q_{ref}$ = 0.5 pu @ t = 0.9 s | $i_{qref} = i_q = -0.5pu$, $i_a$ lagging $v_a$ |
| $Q_{ref}$ = -0.5 pu @ t = 1.1 s | $i_{qref} = i_q = 0.5pu$, $i_a$ leading $v_a$ |

The summarized operation in table 3.5 is a simulation for one second of VSI operating and it is asked to inject or absorb some amount of active and reactive power to or from the grid. The expected values are based on calculations in 2.5 and 3.1. The process of the simulation is similar to the laboratory experiment procedure later, the grid connection is established at $t = 0.1s$ then the inverter starts operating (Gate enable command is sent) at $t = 0.3$(Startup phase). The simulations start at $t = 0.5s$ but before that, in the startup phase, the effect of CCAD can be seen by monitoring the converter side current in figure 3.15 and 3.16.

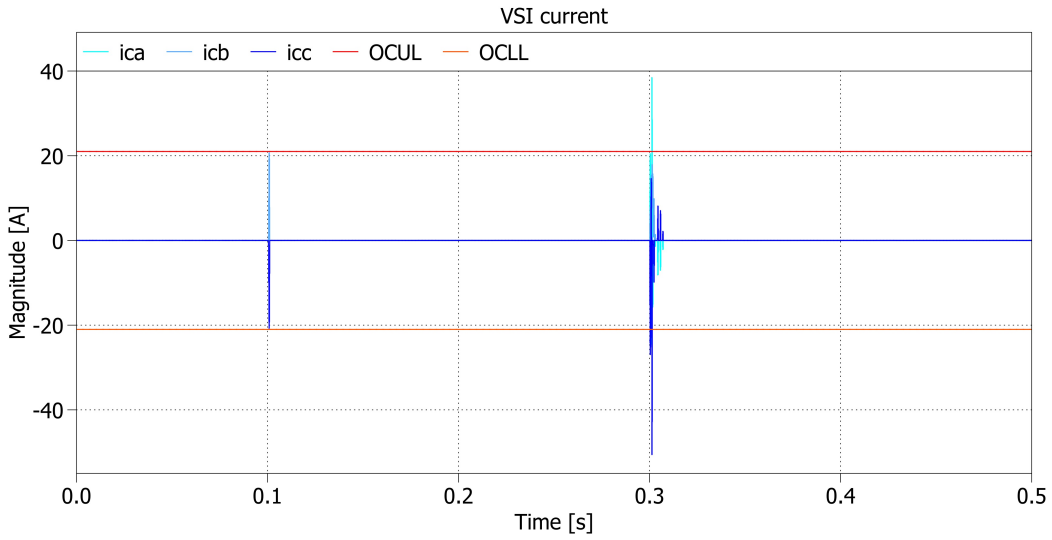


**Figure 3.15:** Converter side current when CCAD is not utilized

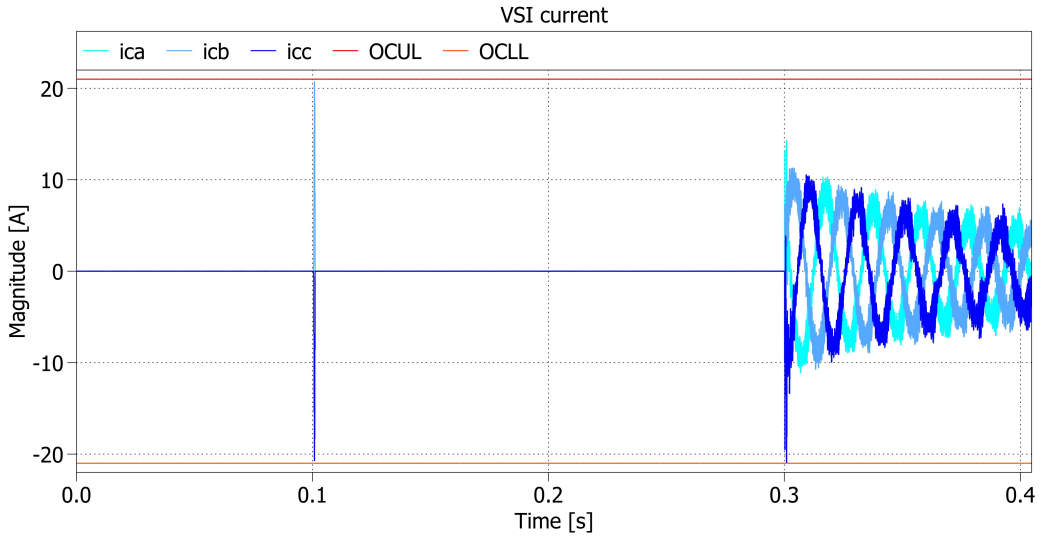


**Figure 3.16:** Converter side current when CCAD is utilized

In both figure 3.15 and 3.16, a simplified command is used to mimic the protection system behavior based on data in [32]. The limit for over-current protection is set to $21A$ and it can be seen without CCAD, the converter protection will trip in the startup phase because of over-current as in figure 3.15. Utilizing the CCAD, the inverter will make it through the startup transient, and the rest of the simulations can be done after time $0.5s$. This is important to be considered because during the experiment it will prevent the system from shutdown. The controller evaluation results are shown in figure 3.17.

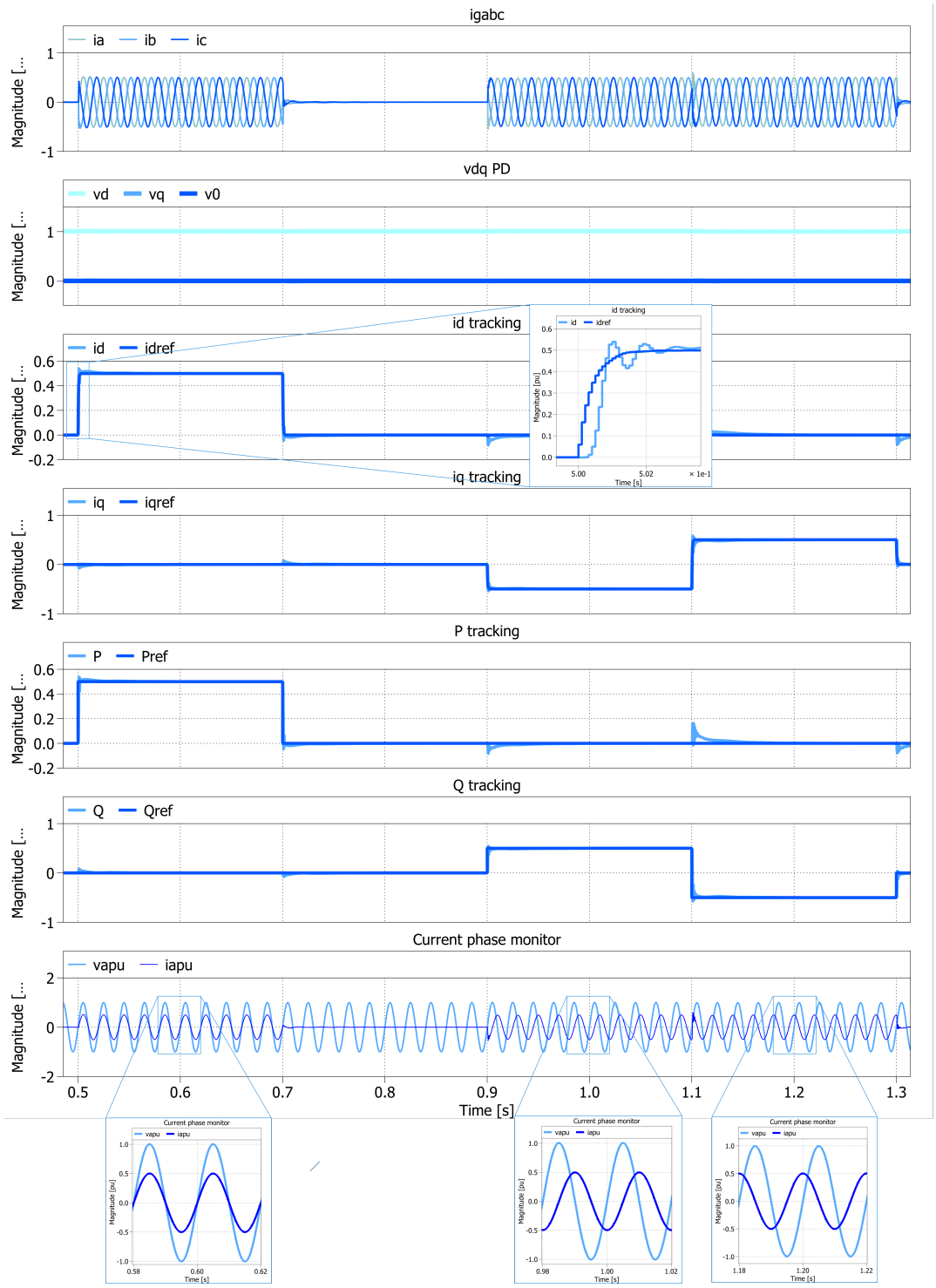


**Figure 3.17:** VSI controller evaluation results

Figure 3.17 shows how the power controller is successfully tracing the reference in "P tracking" and "Q tracking" graphs, providing the equivalent current reference. The plots "id tracking" and "IQ tracking", show the capability of the controller in tracking current reference and matches the calculation in table 3.5. The magnified result of tracking in the "id tracking" plot shows the expected tracking behavior as table 3.1, giving rise time of $t_{90\%} - t_{10\%} = 0.5006 - 0.5002 \simeq 0.0003s$ giving an approximate bandwidth of $600Hz$. Finally, the sign of $i_q$ with respect to $Q$, generates the three-phase current in the correct phase with respect to the voltage shown in the last plot.

## 3.5 Conclution

This chapter spends four sections modeling the VSI controller, 3.1 and 3.2, based on the theory introduced in chapter 2. The simulated models, 3.3 and 3.4, are validated based on the evaluation criteria in chapter 2. Now that the model is confirmed operating as expected, it can be used for further analysis in chapter 4.

# Chapter 4

# Controller simulation under distortion

*In this chapter the verified controller will be examined in different presences of distortion with SRF-PLL and MSRF-PLL utilized. Three scenarios will be covered from the previous chapter, and in each section one of them will be analyzed when SRF-PLL or MSRF-PLL is utilized.*

## 4.1 Case studies summery

To begin with simulations, a summary of the simulation cases is shown in table 4.1 including the distortion condition and utilized PLL.

**Table 4.1:** Summerized grid distortion conditions for SRF-PLL and MSRF-PLL

| Scenario | Parameters |
|---|---|
| **1. Magnitude Unbalance** | VUF=2% @ t=[0.7, 0.9] |
| **2. Harmonics** | vh5=6%<br>vh7=6%<br>THD > 8%<br>@ t=[1, 1.2] |
| **3. Unbalance and harmonics (Magnitude and phase)** | $v_{5\omega} = 6\%$ , $\varphi_{5\omega} = \frac{\pi}{6}$<br>$v_{7\omega} = 6\%$ , $\varphi_{7\omega} = -\frac{\pi}{4}$<br>$VUF = 2\%$ , $\varphi_{-\omega} = -\frac{\pi}{6}$<br>THD > 8%<br>@ t=[1.3, 1.5] |

The simulation of scenarios is done similarly to the validation where the grid connection is established at $t = 0.1s$, the inverter starts at $t = 0.3s$ and then the

scenarios are simulated and shown after $t = 0.5s$. At $t = 0.5s$ inverter starts operating and injecting $0.5pu$ power and during operation, scenarios are performed for both SRF and MSRF.

## 4.2 SRF-PLL based controller performance

The system performance when SRF-PLL is utilized is shown in figure 4.1.

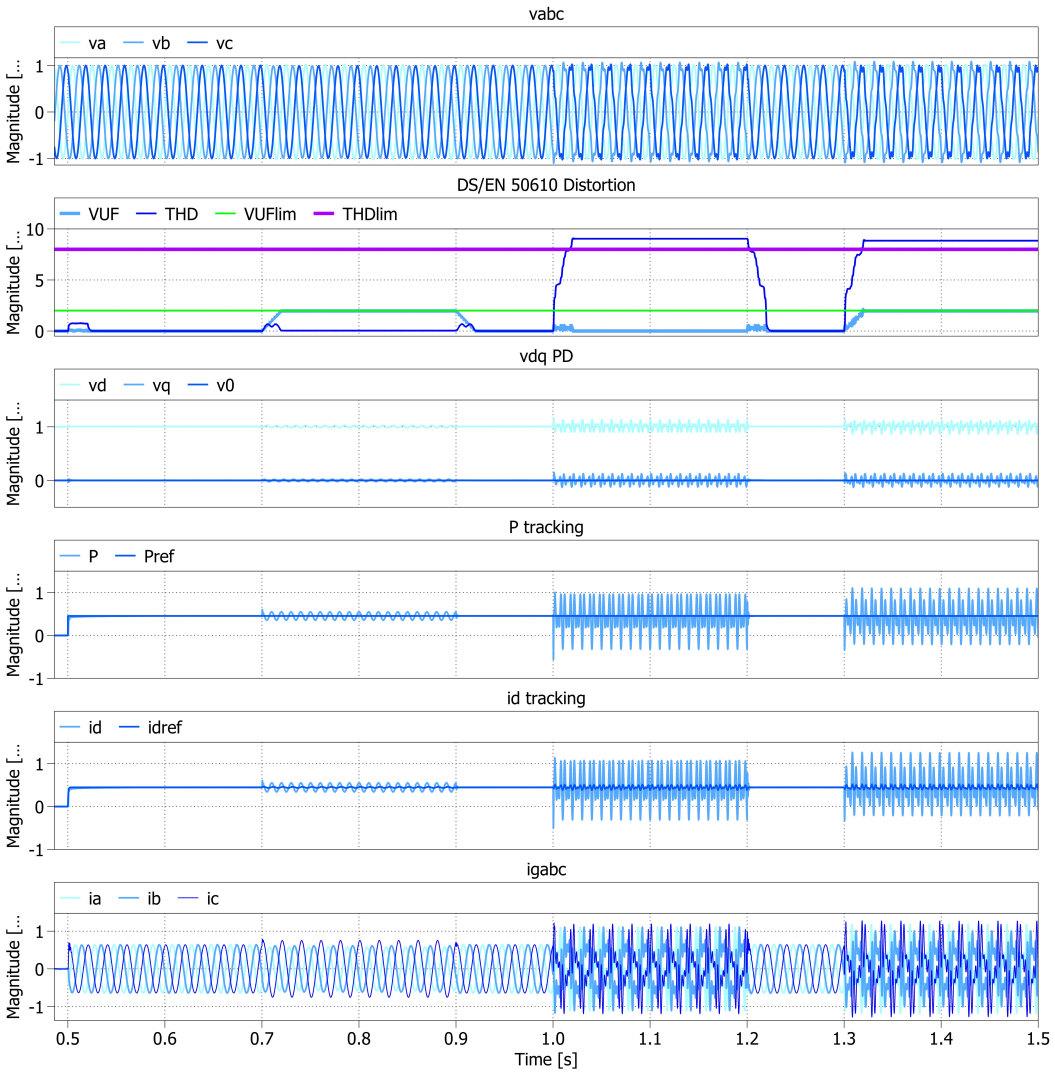


**Figure 4.1:** VSI performance during different scenarios using SRF-PLL-based controller

Simulation results in figure 4.1, showing the grid voltage condition in the first plot where the distortions are applied in time intervals. The second graph shows

the amount of distortion based on standards and the third graph is the PLL phase detector. The "P tracking", "id tracking", "igabc" show the active power tracking, current controller tracking, and output grid current.

### 4.2.1 Scenario 1

When the unbalance condition is applied in time division of [0.7, 0.9]s, the oscillations can be seen in the PLL phase detector. The power and current tracking are also affected by the distortion and three phase output current is also unbalanced because the positive sequence power is injected in unbalanced voltage, resulting in different corresponding currents flowing in each phase.

### 4.2.2 Scenario 2

In time intervals of [1, 1.2]s when grid voltage experiencing harmonics, it can be seen that the SRF-PLL is experiencing more oscillations. The power and current tracking is highly distorted and the output current is not sinusoidal anymore therefore in this case the VSI capability for power delivery is fully compromised.

### 4.2.3 Scenario 3

The grid voltage is affected by both harmonics and unbalances during [1.3, 1.5]s, and similar to 4.2.2 the phase detector of the PLL is experiencing severe oscillations. Power delivery is also compromised, as shown in the last three plots.

### 4.2.4 SRF-PLL-based controller analysis

By performing Fourier analysis of the signals in figure 4.1, using equation 2.3, the components in each frequency of the scenarios are shown in figure 4.2.

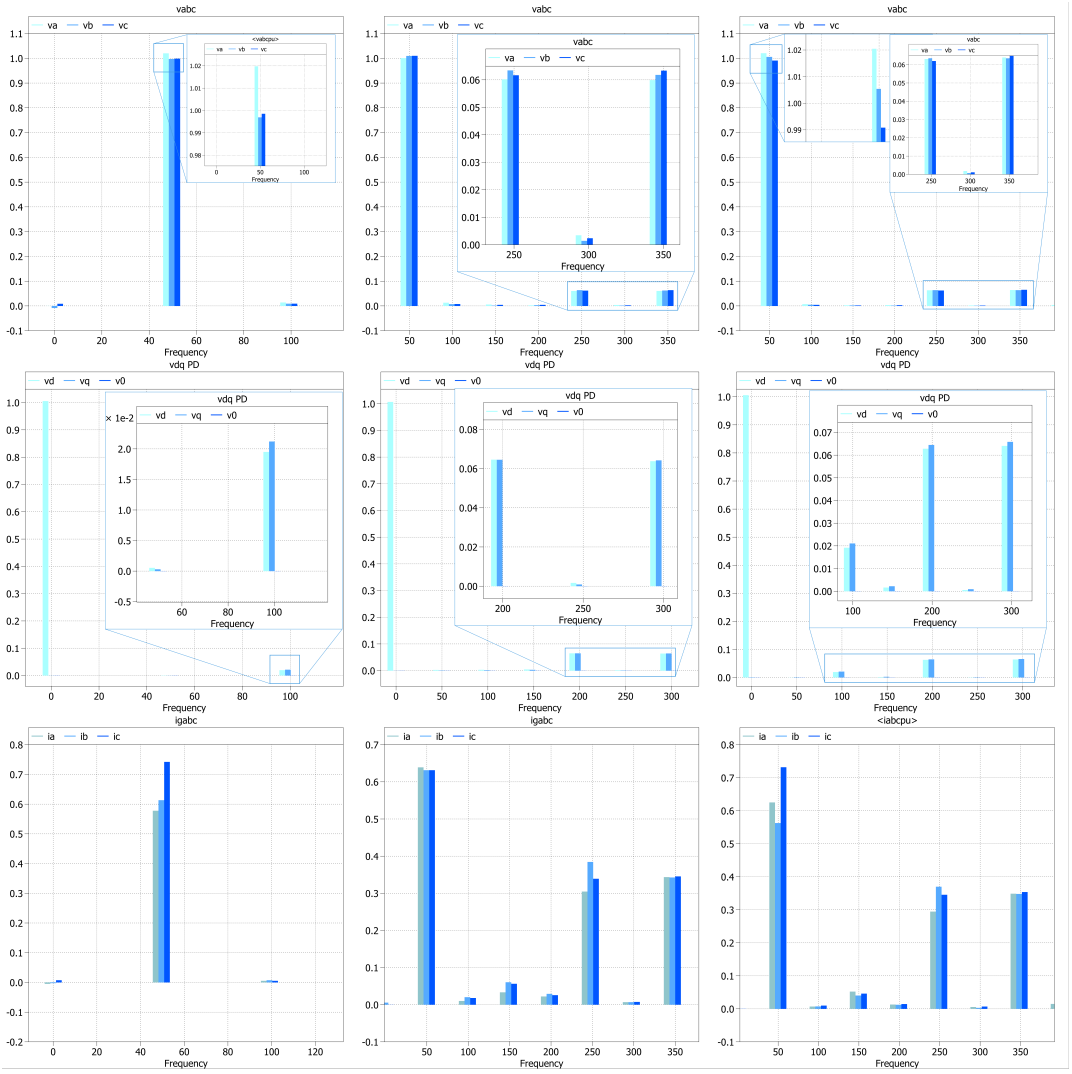


**Figure 4.2:** SRF-PLL-based controller Fourier spectrum

Plots in the first row of figure 4.2 show the distortion content appearing in the simulated frequencies according to table 4.1. The corresponding oscillations in the PLL phase detector are shown in second-row plots according to calculations in equation 2.8 and 2.11. It can be concluded that the SRF-PLL's phase detector is not immune to distortion. This can be noticed in figure 4.3 where the converter side current is monitored during startup and grid voltage is under distortion from scenario 3.

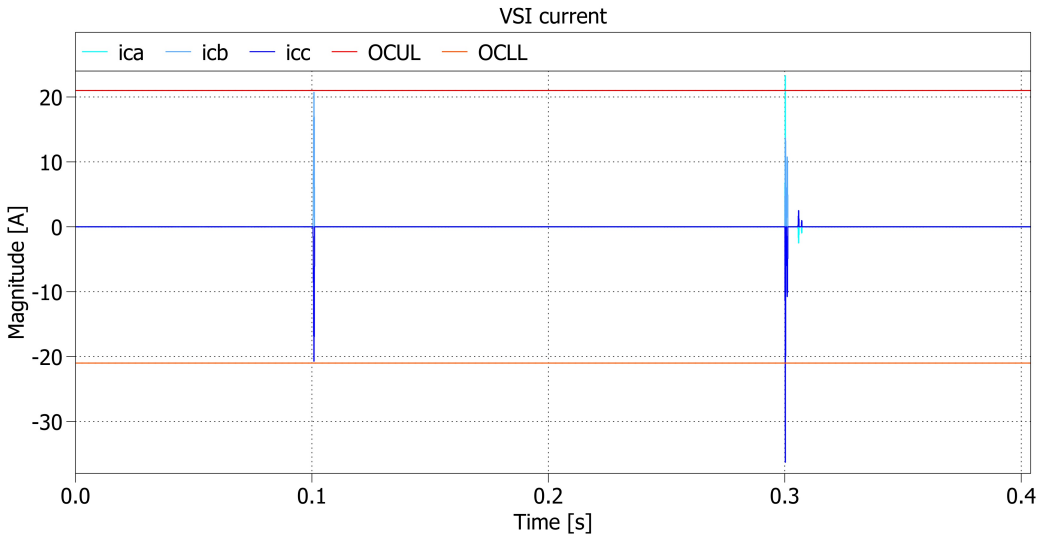


**Figure 4.3:** SRF-PLL-based system converter side current during startup

In figure 4.3 the grid connection is established at $t = 0.1s$ and the inverter is started at $t = 0.3s$. In the presence of distortion, at $t = 0.3s$ the converter protection trips because of overcurrent, and the inverter cannot start.

## 4.3 MSRF-PLL based controller performance

The performance of the system with MSRF-PLL utilized in the controller is shown in figure 4.4.

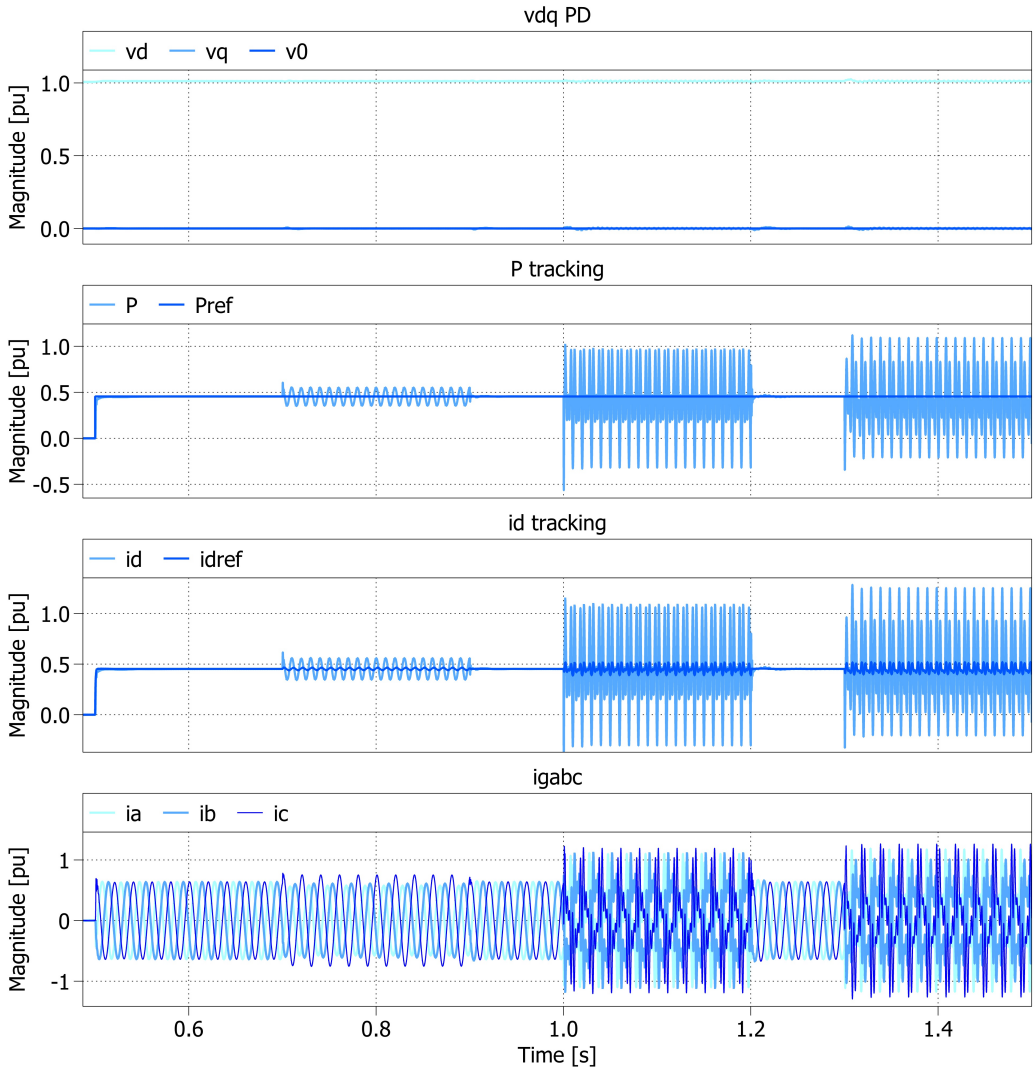


**Figure 4.4:** VSI performance during different scenarios using MSRF-PLL-based controller

In figure 4.4 the first plot shows the PLL phase detector, "P tracking" and "id tracking" showing the controller tracking the power and current and the last plot shows the grid three-phase current output.

### 4.3.1 scenario 1

During the unbalance grid condition at $t = [0.7, 0.9]s$ the PLL phase detector is immune to the distortion and there are no oscillations. The current and power tracking still seems to be disturbed because of the presence of unbalance in the grid voltage when the system is injecting positive sequence power.

### 4.3.2 scenario 2

When the voltage is affected by harmonics, the first plot shows that there are no oscillations in the phase detector. The power and current tracking have oscillations and the three-phase output current is distorted too, both due to power injection in the presence of harmonics.

### 4.3.3 scenario 3

Similar to 4.3.2 the oscillations do not appear in the PLL phase detector. Meanwhile, the power and current track are still affected because of the presence of distortion.

### 4.3.4 MSRF-PLL-based controller analysis

The analysis of scenarios can be backed up by the Fourier analysis of each plot during different scenarios, shown in figure 4.5.

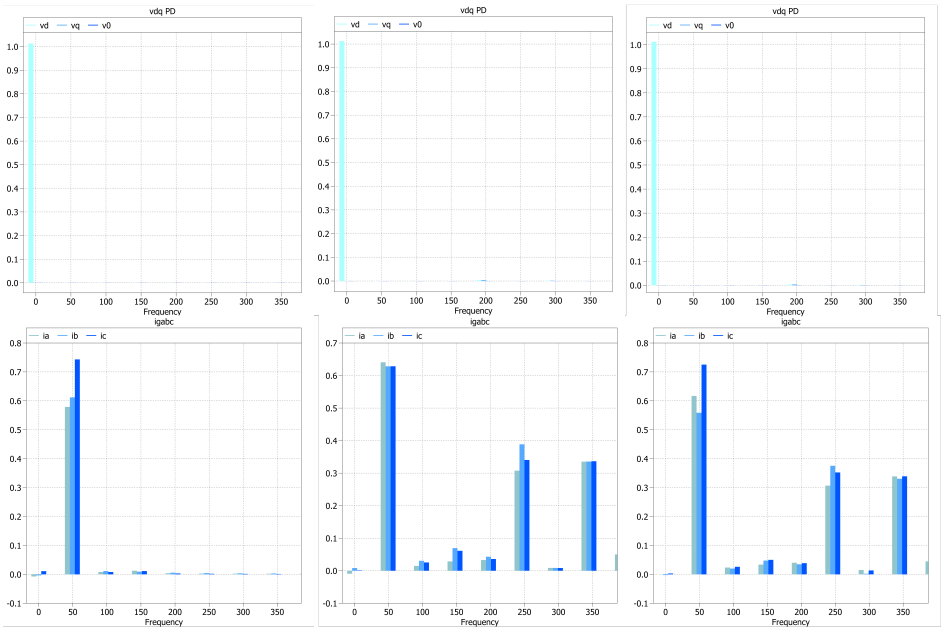


**Figure 4.5:** MSRF-PLL-based controller Fourier spectrum

The plots in the first row of figure 4.5, show that there are no additional terms except fundamental in the spectrum therefore there are no voltage distortions going through the controller. The distortion terms visible in the output current are appearing in the amplitude of three phases for the unbalance scenario. In the case of harmonics, they appear in the same frequencies as voltage harmonics. The fact that the output current of the controller is distorted, although the voltage distortion is filtered, highlights the need for compensation. The capability of the MSRF-PLL-based controller in preventing the voltage distortions from affecting the controller can be seen in figure 4.6 during the startup, where grid voltage is in the condition of scenario 3.

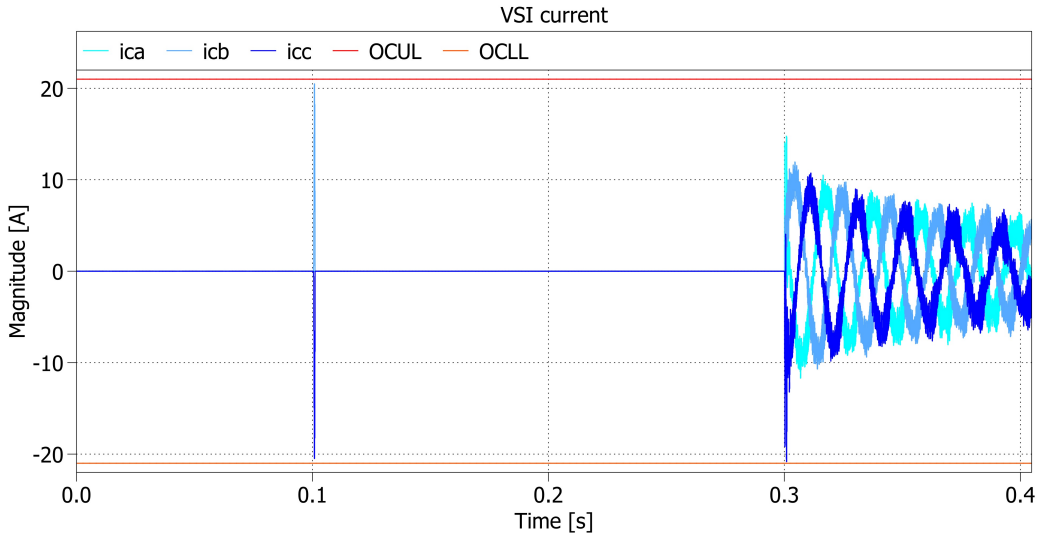


**Figure 4.6:** MSRF-PLL-based system converter side current during startup

Compared to 4.3, figure 4.6 shows highlights the capability of the MSRF-PLL-based controller in filtering out the voltage distortions and therefore, the controller dynamics are not disturbed and can keep the controller synchronized during startup, in addition, prevents the overcurrent tripping.

## 4.4 conclution

In this chapter, the effect of the grid voltage distortion on two PLL configurations and the effect of distortion is observed on the startup and connection phase plus power delivery. Based on the simulation results in 4.1 and 4.4, it is concluded the oscillations in the PLL's phase detector are because of voltage distortion. The oscillations disturb the dynamics of the SRF-PLL-based controller during startup while the MSRF-PLL-based controller is able to maintain system dynamics during

startup. However, both configurations have poor power delivery capability which highlights the need for compensation.

# Chapter 5

# Laboratory implementation

*In this chapter the VSI and PLL validations in chapter 3, plus the test scenarios in chapter 4 will be implemented on the lab setup. The first section is going to introduce the setup layout. Later on, the validation and scenarios are investigated as experiments.*

## 5.1 Setup introduction

As explained in section 1.3.2, the scaled-down system to be analyzed in simulation is identical to the lab setup which the grid-connected system properties are mentioned in table 2.5. The laboratory setup additionally includes measurement, DSP, and interface cards to the data into these subsystems. The controller layout compiled into DSP uses input-output communication blocks in the dSPACE Simulink library to utilize the captured data. These input-output communication blocks are for analog digital inputs from measurements, and the PWM3 block is the interface with the modulator and protection or the VSIs start/stop commands. A schematic of the physical system similar to 1.4 available in the lab is shown in figure 5.1.

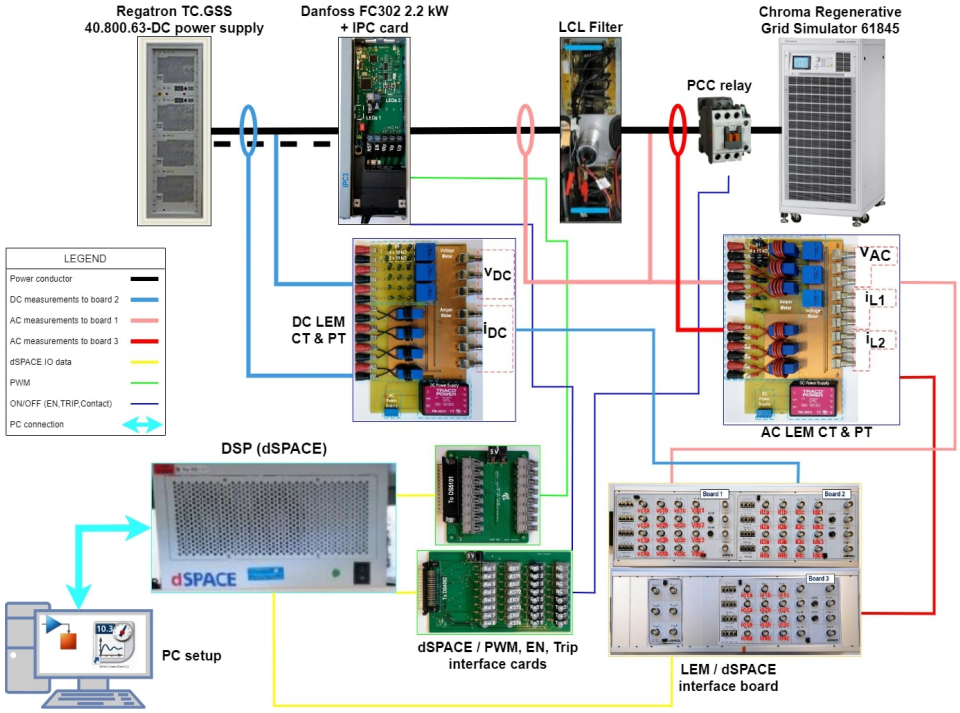


**Figure 5.1:** Graphical schematics of laboratory setup

The additional parts of the system to be introduced include real-time interfacing, control, and monitoring. The data captured from the sensors, as demonstrated in figure 2.2, are sampled for use in the module-based control layout built in Simulink. The duty cycles are also needed to go to the embedded modulator plus additional access points for protection or hardware commands. Therefore, the dSPACE interface card is equipped to process the input-output signals of the controller from the board to dSPACE digital signal processors or to the inverter interface and protection card (IPC).

### 5.1.1 Control desk GUI

After setting up the layout and interface blocks, the layout needs to be compiled via DSP. This is done by converting the modular design to C code inside the DSP, where the user can interact with the layout via a graphical user interface (GUI) in real-time. The GUI for real-time control and monitoring is the dSPACE control desk which is shown in figure 5.2.

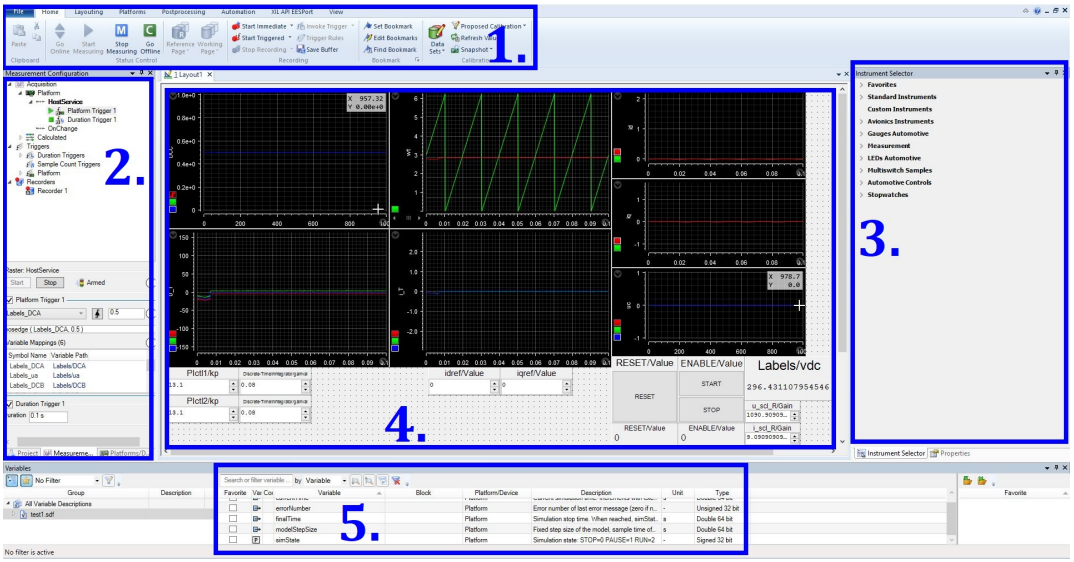


**Figure 5.2:** dSPACE control desk software and GUI

The dSPACE control desk GUI shown in figure 5.2, includes five menus allowing the user to communicate with the interface. Menu 1 is the software control panel for options for special features such as accessing libraries and other menus. Menu 2 includes sub-sections for file settings, triggers, and data recordings. Menu 3 is the instruments libraries for graphical modules for monitoring and control settings. Menu 4 is the desktop where monitoring and control blocks are made and Menu 5 is the variables and signals from the Simulink control layout to be accessed.

## 5.2 Experimental cases

The complete guidelines for using the setup are available in [32], and information for setting up experiments is available. The experiments are basically performing the validation and case studies using the physical system. Due to the limited capability of the grid simulator, the case studies will be less complicated, and the evaluation tests are done step by step. A summary of the experiments is shown in table 5.1.

**Table 5.1:** Summerized experimental case studies

| *Experiment vs Configurations* | *SRF-based vs MSRF-based PLL* | |
|---|---|---|
| *Condition vs stage* | **Startup** | **Operation** |
| *No distortion (Evaluation)* | Synchronization<br>Distortion limits | Power tracking<br>Current tracking<br>3 phase output current |
| *Voltage magnitude unbalance* | VUF=2% | P=0.43pu<br>Q=0.34pu |
| *Harmonic distortion* | $v_{5\omega}$=6.5%<br>$v_{7\omega}$=4.7%<br>THD=8% | P=0.34PU<br>Q=0.34PU |
| *Unbalance and harmonics (Magnitude and phase)* | VUF=2%, $\varphi_{-\omega} = -\frac{\pi}{6}$<br>$v_{5\omega}$=6.5%<br>$v_{5\omega}$=4.7%<br>THD=8% | P=0.34PU<br>Q=0.34PU |

The experiments are conducted once with the SRF-PLL-based and once with the MSRF-PLL-based controller. Each experiment is conducted in different grid conditions similar to the simulation tests in table 3.5 and 4.1 with similar goals and monitoring methods. After compiling the controller configuration in Simulink to C code into dSPACE, the DSP will go online and the setup is powered up. Connection is established via the control desk interface and the inverter starts operating. The experiments are done in the following steps.

- The connection to the grid is established via the control desk by the PCC relay connection command. This is the startup phase when the PLL is synchronized with the grid voltage and the results will show if the grid condition is affecting the PLL.
- The inverter starts operating by enabling VSI pulses. This will be the operation phase when the VSI starts operating and must be stable, following the initial references. The results of this experiment show if the controller is sensitive to distortion.
- The controller is asked to follow a power reference. The reference must be followed and the results will indicate how distortion will affect the output.

It must be noticed that due to hardware limitations, experiments are simplified. In the second case, harmonic generation by grid simulator cannot be done with more than one harmonic at a time, thus, scenario two is done for individual harmonics. Moreover, there is no option for programming phase shift for harmonics plus the magnitude of the harmonics is limited according to the setup manual,

therefore the magnitude of $5th$ harmonics is set to $v_{5\omega} = 6.5\%$ and $7th$ harmonic to $v_{5\omega} = 6.5\%$. Finally, the grid simulator cannot generate the harmonics constantly and harmonic generations are done by activating the output for the period of the experiment. Therefore, in the startup stage, the grid condition is already applied unlike the simulation the controller started in no distorted condition.

### 5.2.1 SRF-PLL-based controller experiment

In this experiment, SRF-PLL is utilized in the control layout so the experiments show the performance of this controller for each scenario. For the operation phase and final step of experiments, the results are only shown for the stable controller active power tracking and full monitoring outputs can be seen in the appendix A.

#### Experiment 1: No distortion (evaluation)

In figure 5.3 and 5.4 the phase angle tracking and the phase detector performance for the SRF-PLL-based controller are shown in the startup phase.

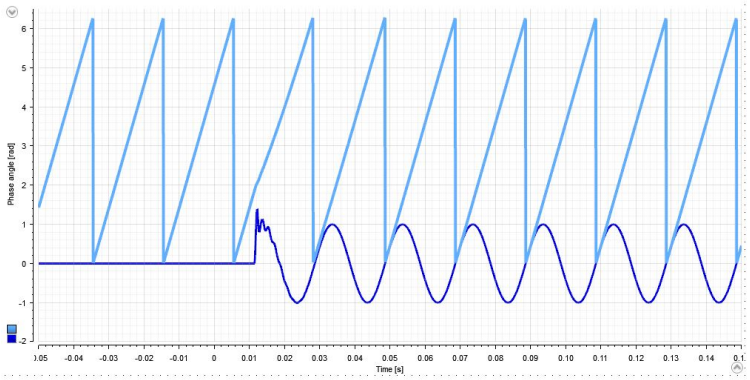


**Figure 5.3:** Experiment 1: SRF-PLL phase angle tracking (phase angle: - , $v_a$: -)

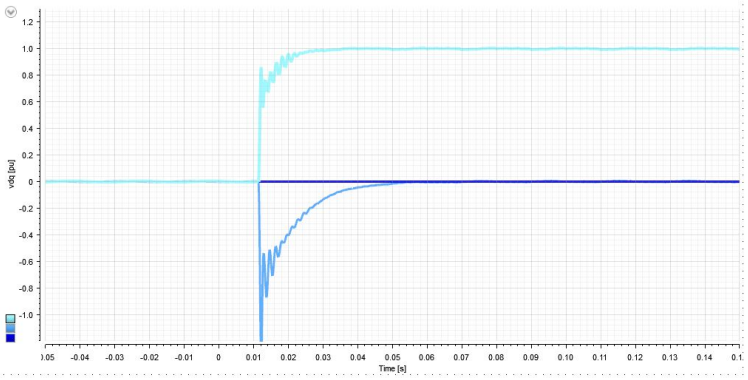


**Figure 5.4:** Experiment 1: SRF-PLL phase detector performance ($v_d$: - , $v_q$: - , $v_0$: -)

Figure 5.3 shows that the SRF-PLL is fully capable of tracking the phase angle of the grid voltage vector. Moreover, it can be seen in figure 5.4 that the phase detector is capturing the $dq$ components. Both results are identical to the simulation output in figure 3.13 and 3.17. The following figures 5.5, 5.6, and 5.7 are the results for controller active power tracking and three-phase current output.

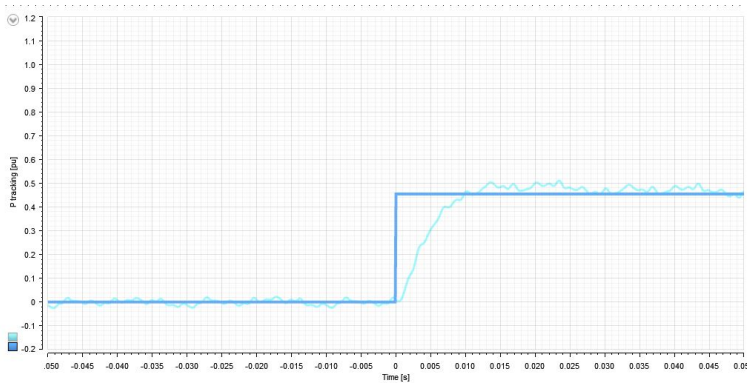


**Figure 5.5:** Experiment 1: controller $P$ tracking ($P$: - , $P_{ref}$: -)

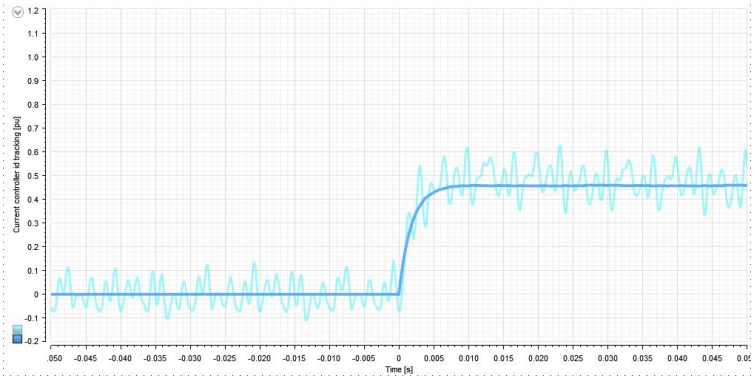


**Figure 5.6:** Experiment 1: controller $i_d$ tracking ($i_d$: - , $i_{d.ref}$: -)

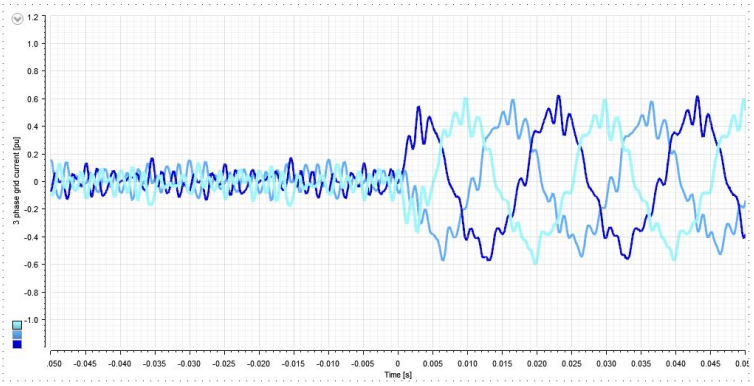


**Figure 5.7:** Experiment 1: Output $i_{abc}$ ($i_a$: - , $i_b$: - , $i_c$: -)

In figure 5.5 it is shown that the controller is able to track the given power reference. Figure 5.6 demonstrates that the controller also tracks the correct corresponding current reference. In figure 5.7 it is shown the three-phase current output of the system is correct according to tracking. All the results are identical to the simulation output for validation in figure 3.17.

It can be concluded that the subsystems of the controller such as the power controller, current controller, and voltage feedforward stage are also performing properly. The difference is in the setup, unlike the simulation, there are small oscillations in tracking and output which is because of the properties of the physical system including switches with realistic switching behavior and additional parasitic passive elements in connections, etc. This means the controller is valid to be used further in the experiments therefore, later on in 5.2.2 only the startup phase for the MSRF-PLL-based controller is shown.

**Experiment 2: Voltage magnitude unbalance**

In this experiment, the connection to the grid is established when $VUF = 2\%$. Figure 5.8 shows the SRF-PLL-based controller's phase detector performance.

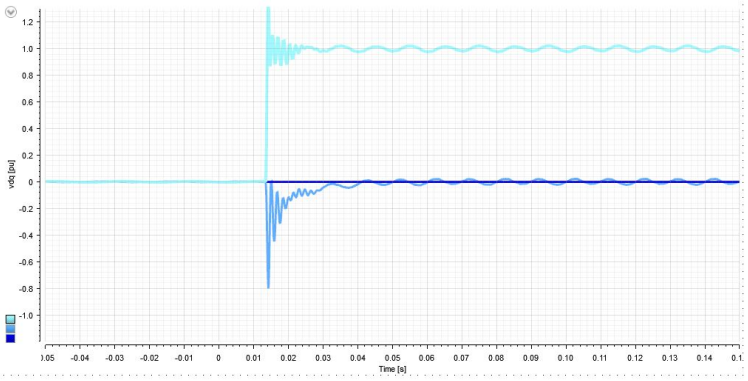


**Figure 5.8:** Experiment 2: SRF-PLL phase detector performance ($v_d$: - , $v_q$: - , $v_0$: -)

In figure 5.8, similar to simulation results in 4.1, it can be seen that the phase detector of the controller is affected by the unbalance. Figure 5.9, 5.10, and 5.11 demonstrate the controller's performance during the operation phase.

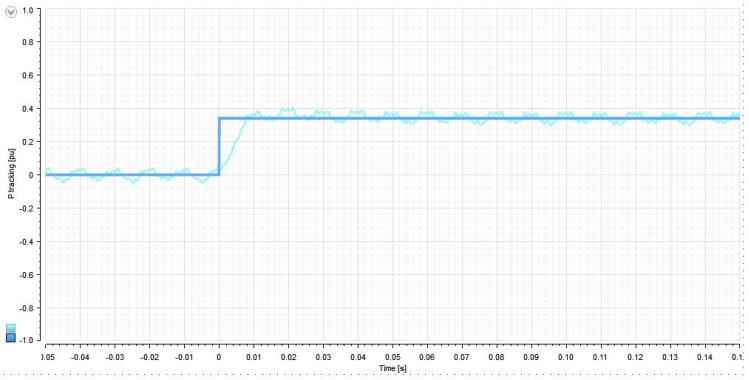


**Figure 5.9:** Experiment 2: SRF-PLL-based $P$ tracking ($P$: - , $P_{ref}$: -)

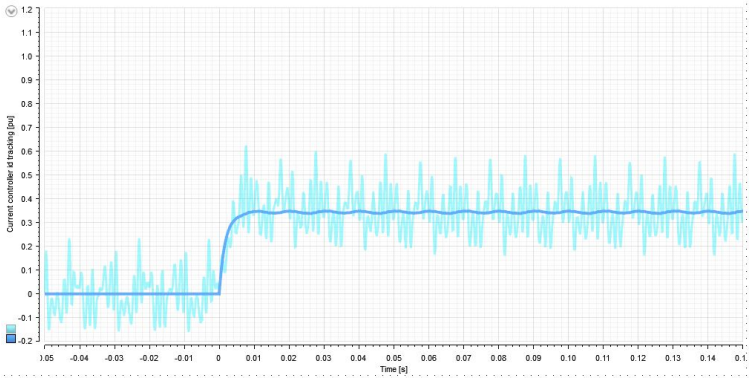


**Figure 5.10:** Experiment 2: SRF-PLL-based $i_d$ tracking ($i_d$: - , $i_{d.ref}$: -)

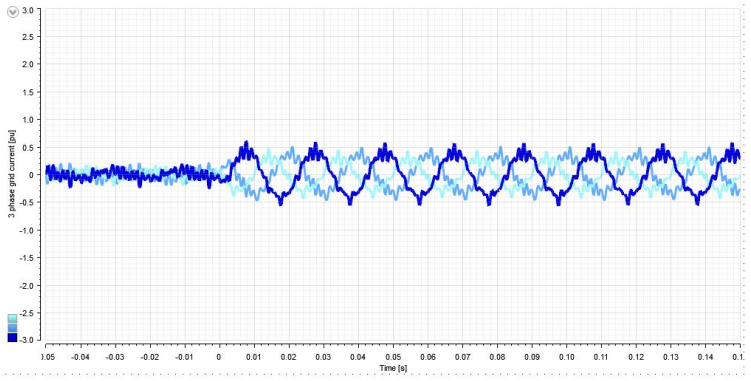


**Figure 5.11:** Experiment 2: SRF-PLL-based $i_{abc}$ output ($i_a$: - , $i_b$: - , $i_c$: -)

Similar to the results from the simulation in figure 4.1, the controller operation is affected by the distortion in which the oscillations in tracking dynamics, figure 5.9 and 5.10, also in the output, figure 5.11, can be observed but the stability and of the system is not compromised.

### Experiment 3: Harmonic distortion

This experiment is done when the grid voltage is affected by harmonics. As it was explained in section 5.2, only one harmonic can be applied and therefore, the results are only shown for $5th$ harmonics and more results are available in the appendix. In figure 5.12 the phase detector performance during startup, in the presence of $5th$ harmonic is shown.

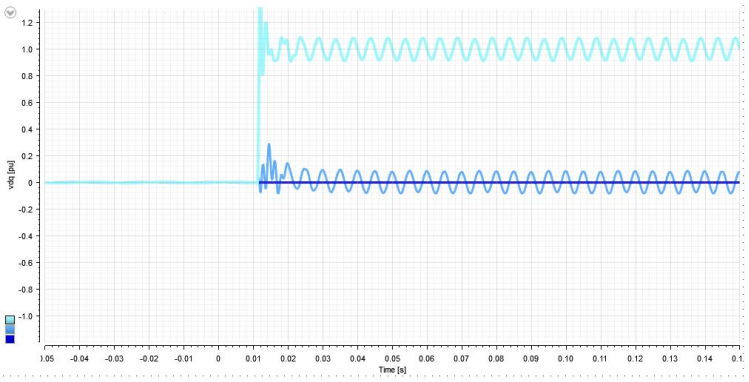


**Figure 5.12:** Experiment 3: SRF-PLL phase detector performance ($v_d$: - , $v_q$: - , $v_0$: -)

The monitoring in figure 5.12 shows similar to the simulation, figure 4.1, the oscillations appearing in the phase detector. The following figures demonstrate the monitoring of system operation.

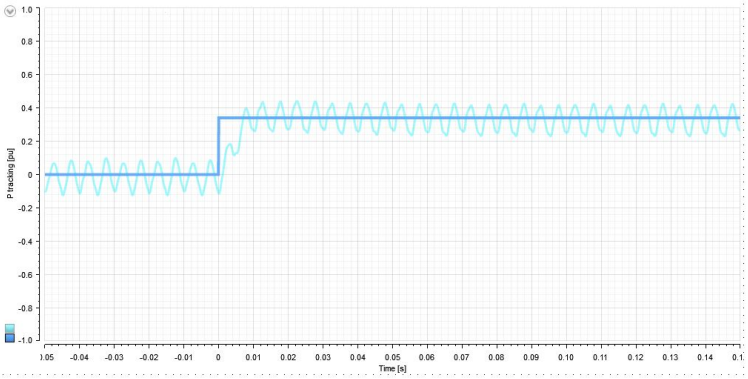


**Figure 5.13:** Experiment 3: SRF-PLL-based $P$ tracking ($P$: - , $P_{ref}$: -)

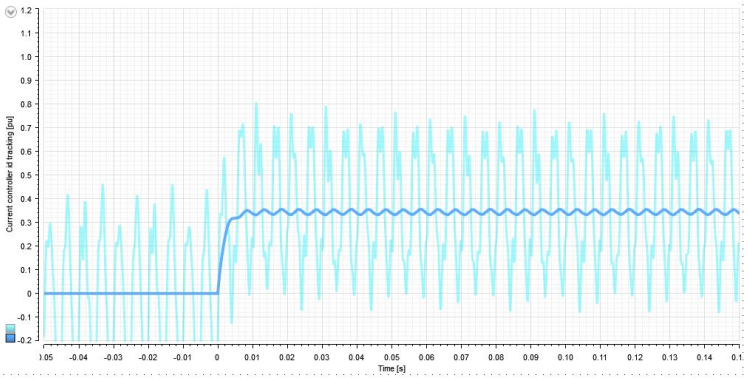


**Figure 5.14:** Experiment 3: SRF-PLL-based $i_d$ tracking ($i_d$: - , $i_{d.ref}$: -)

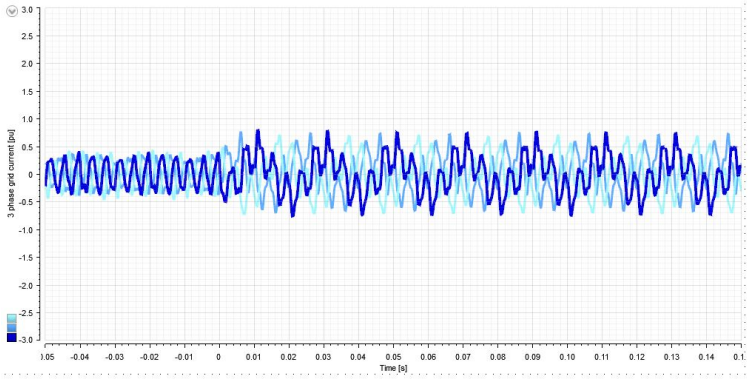


**Figure 5.15:** Experiment 3: SRF-PLL-based $i_{abc}$ output ($i_a$: - , $i_b$: - , $i_c$: -)

As is shown in the simulation monitoring in figure 4.1, the tracking dynamics are also experiencing oscillations as is shown in figure 5.13 and 5.14. The three-phase output current in figure 5.15 is highly disturbed, showing that the SRF-PLL is not capable of either delivering power or filtering out the voltage distortions.

### Experiment 4: Unbalance and harmonics

In this experiment, both distortions, $VUF = 2\%$ and $6\%$ of $5th$ harmonic are applied to the grid voltage. Figure 5.16 shows the phase detectors' performance in this scenario.

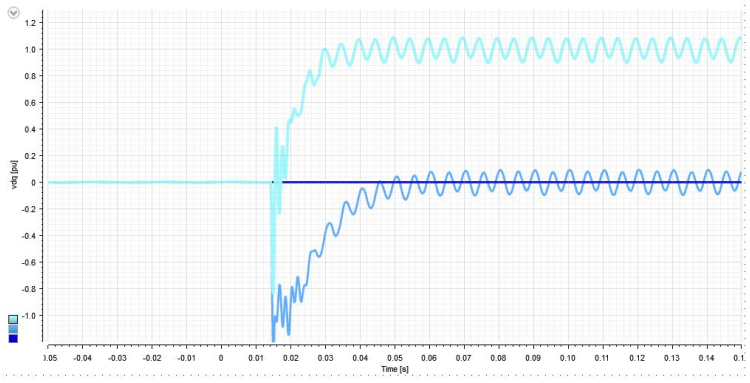


**Figure 5.16:** Experiment 4: SRF-PLL phase detector performance ($v_d$: - , $v_q$: - , $v_0$: -)

It can be seen in figure 5.16, similar to simulation output 4.1, more oscillations are introduced to the phase detector. Further on, as expected in simulation in figure 4.3, this oscillation affects the dynamics of reference tracking, causing the VSI to trip because of overcurrent, as it is shown in figure 5.17

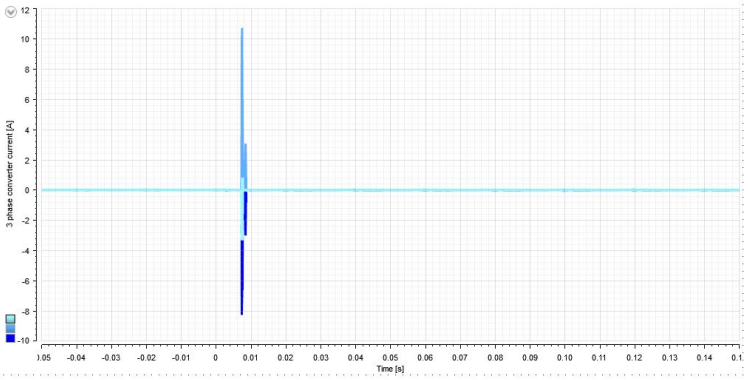


**Figure 5.17:** Experiment 4: Inverter side three-phase current$i_{abc}$ operation when SRF-PLL is utilized ($i_a$: - , $i_b$: - , $i_c$: -)

Figure 5.17 shows the overcurrent happening on the converter side three-phase current. The monitoring results are not showing the spike to 21 A because of additional filterings and limits of interface boards in capturing the sharp dynamics.

### 5.2.2 MSRF-PLL-based controller experiment

This subsection goes through all the steps of the experiment and scenarios when MSRF-PLL is used in the controller. The goal is to observe the PLL noise canceling in comparison with SRF. The complete monitoring results are available in the appendix A, while for tracking capability only the active power tracking is mentioned. In the first experiment, 5.2.2 only the PLL phase detector performance is observed because the goal for observing the controller subsystems is achieved in subsection 5.2.1.

#### Experiment 1: No distortion (evaluation)

Figure 5.18 representing the MSRF-PLLs phase detector capability in tracking the

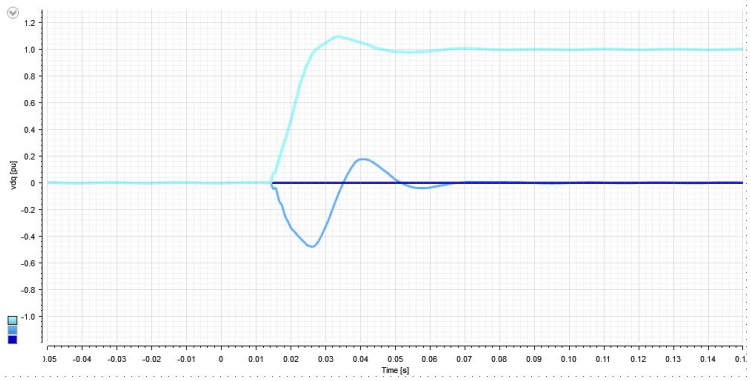


**Figure 5.18:** Experiment 1: MSRF-PLL phase detector performance ($v_d$: - , $v_q$: - , $v_0$: -)

Phase detector monitoring in figure 5.18 shows that similar to simulation observation in figure 4.4, the MSRF-PLL configuration is valid for further experiments.

### Experiment 2: voltage magnitude unbalance

In this experiment, the grid voltage's unbalance factor is $VUF = 2\%$. The PLLs phase detector performance is shown in figure 5.19.

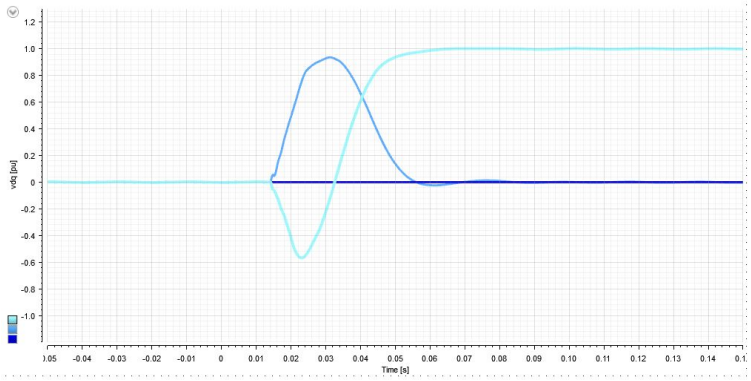


**Figure 5.19:** Experiment 1: MSRF-PLL phase detector performance ($v_d$: - , $v_q$: - , $v_0$: -)

Figure 5.19 shows the same behavior to the simulation output in figure 4.4 where the MSRF-PLL phase detector is immune to distortions during the startup. The following figures demonstrate the tracking and output of the system during power delivery.

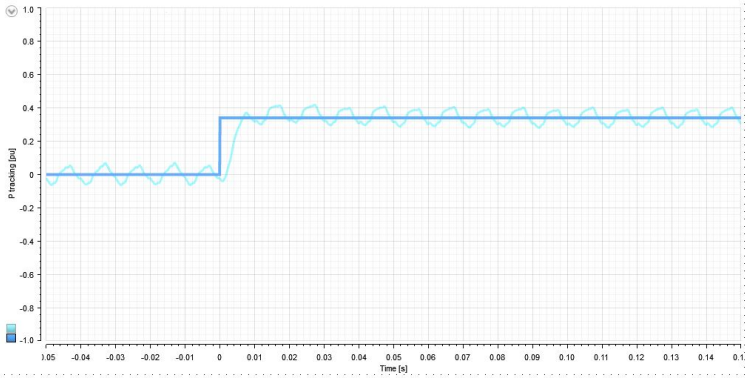


**Figure 5.20:** Experiment 2: MSRF-PLL-based $P$ tracking ($P$: - , $P_{ref}$: -)

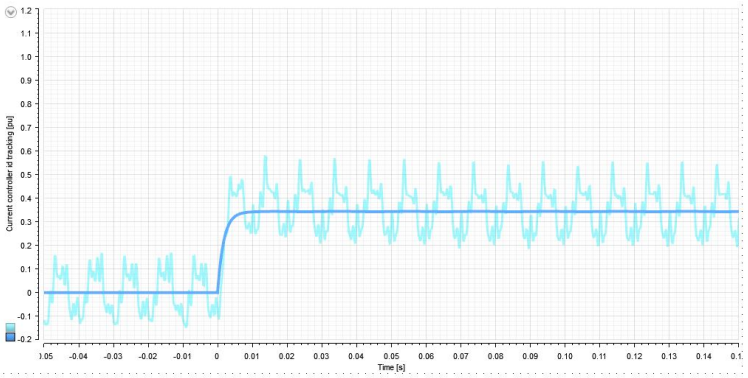


**Figure 5.21:** Experiment 2: MSRF-PLL-based $i_d$ tracking ($i_d$: - , $i_{d.ref}$: -)

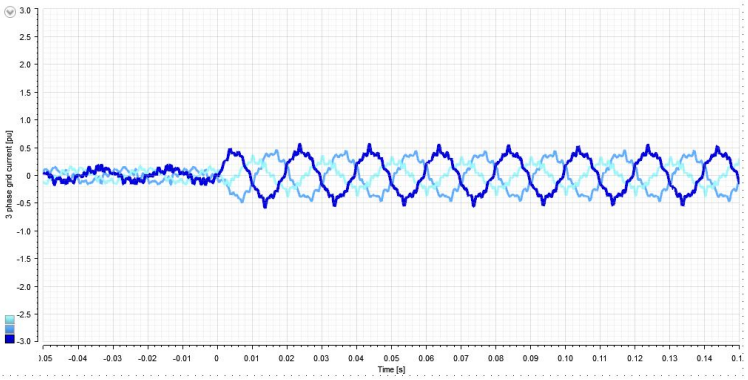


**Figure 5.22:** Experiment 2: MSRF-PLL-based $i_{abc}$ output ($i_a$: - , $i_b$: - , $i_c$: -)

Figures 5.20 and 5.21 show that although the MSRF-PLL successfully filters out the unbalance, the oscillations appear in power and current tracking therefore the output in figure 5.22 is also distorted but the controller's stability and dynamics of

tracking is not compromised. The results are similar to the simulation in 4.4 and highlight the need for compensation in addition to filtering.

### Experiment 3: Harmonic distortions

In this experiment, the 5% harmonic with an amount of 6% is programmed using the grid simulator's output voltage. The full version of the results is shown in the appendix A and due to hardware limitations, the result is shown for $5th$ harmonic only. The MSRF-PLL's phase detector performance is monitored in figure 5.23.

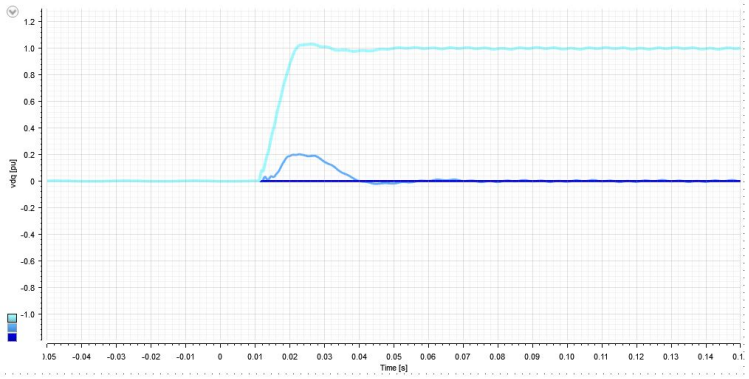


**Figure 5.23:** Experiment 3: MSRF-PLL phase detector performance ($v_d$: - , $v_q$: - , $v_0$: -)

Figure 5.23 indicates similar results to 4.4 where the phase detector of MSRF-PLL is capable of extracting the fundamental positive sequence during the startup in the presence of harmonic. During the operation phase where VSI is activated to inject power into the grid, the tracking and output are shown in figure 5.24, 5.25, and 5.26.

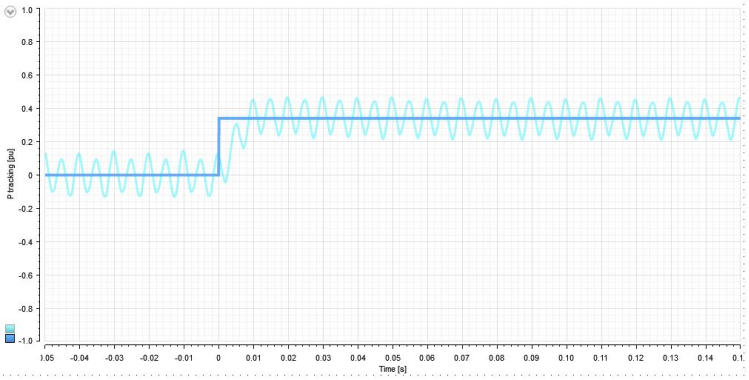


**Figure 5.24:** Experiment 3: MSRF-PLL-based $P$ tracking ($P$: - , $P_{ref}$: -)

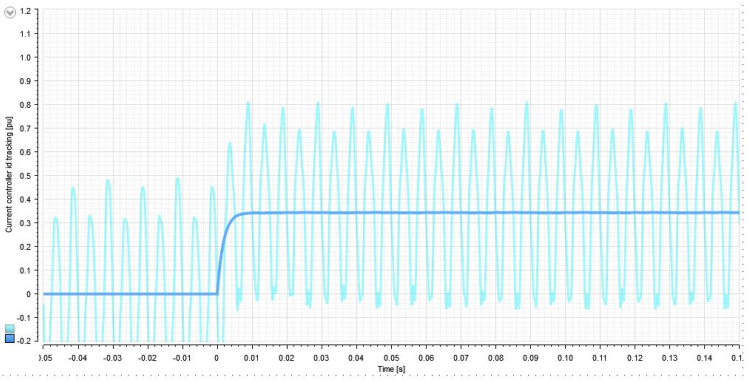


**Figure 5.25:** Experiment 3: MSRF-PLL-based $i_d$ tracking ($i_d$: - , $i_{d.ref}$: -)

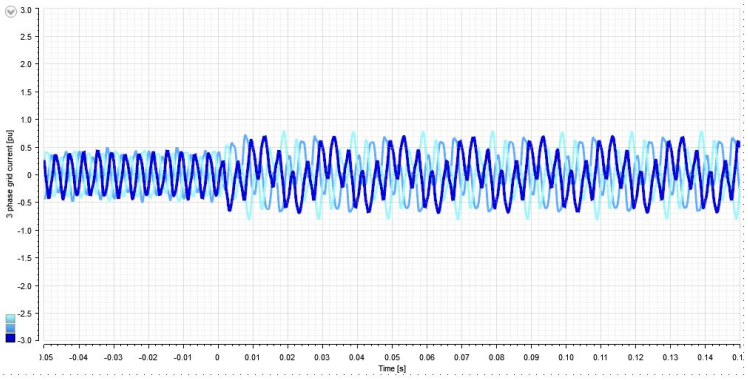


**Figure 5.26:** Experiment 3: MSRF-PLL-based $i_{abc}$ output ($i_a$: - , $i_b$: - , $i_c$: -)

Similar to the simulation output in figure 4.4, it can be seen that power and current tracking are oscillating in figure 5.24 and 5.25, affecting the three-phase output, figure 5.26. In this case, the power quality is fully compromised and compensation is needed but the controller is stable.

### Experiment 4: Unbalance and harmonics

The last experiment for the MSRF-PLL-based controller is programming the grid simulator for $VUF = 2\%$ and $6\%$ $5th$ harmonic distortion. Similar to experiment 5.2.1, the results are only monitored for this condition and other cases are available in the appendixA. First, the phase detector performance during startup is shown in figure 5.27

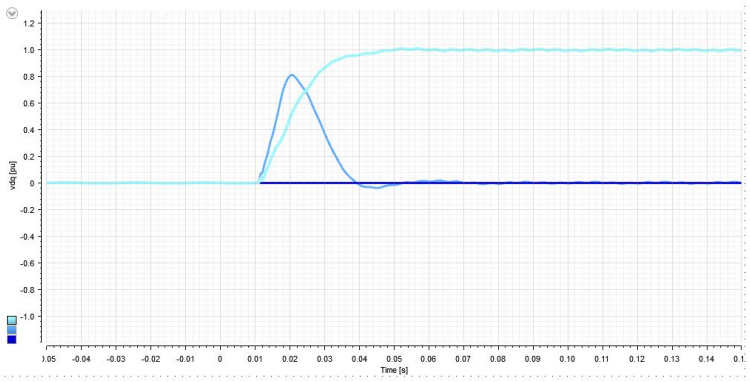


**Figure 5.27:** Experiment 4: MSRF-PLL phase detector performance ($v_d$: - , $v_q$: - , $v_0$: -)

Figure 5.27 shows the MSRF-PLL phase detector is immune to the distortion, as expected in simulation monitoring in figure 4.4. Further on, the operation monitoring is shown in figure 5.28, 5.29, and 5.28.

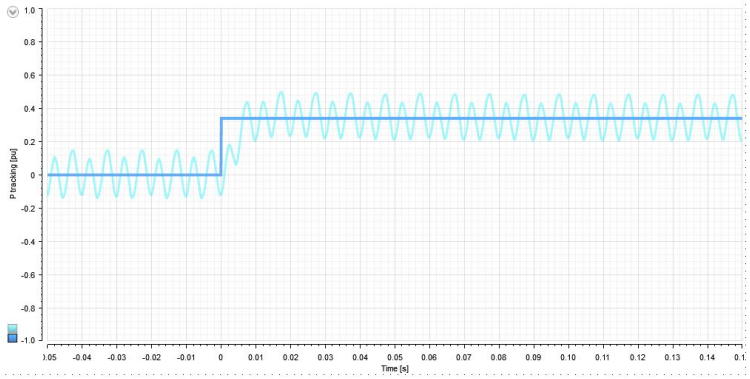


**Figure 5.28:** Experiment 4: MSRF-PLL-based controller $P$ tracking ($P$: - , $P_{ref}$: -)

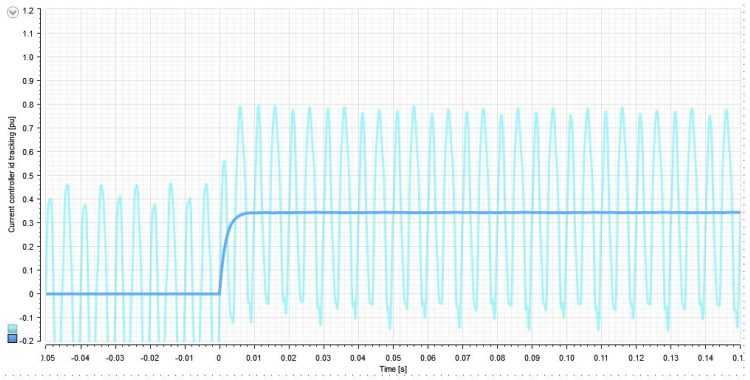


**Figure 5.29:** Experiment 4: MSRF-PLL-based controller $i_d$ tracking ($i_d$: - , $i_{d.ref}$: -)

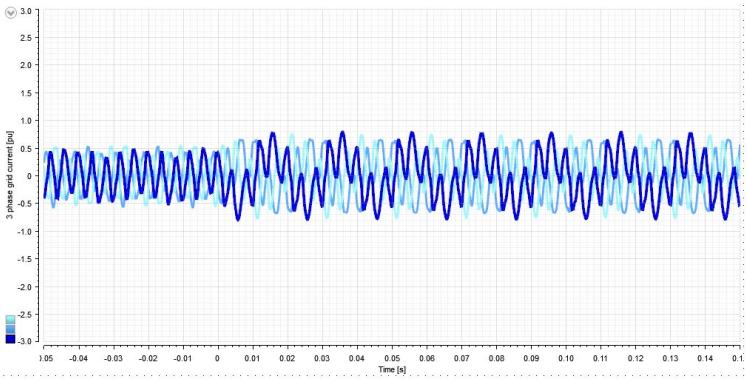


**Figure 5.30:** Experiment 4: MSRF-PLL-based controller $i_{abc}$ output ($i_a$: - , $i_b$: - , $i_c$: -)

Same as the results in 5.2.2, the power and corresponding current tracking in figure 5.28 and 5.29, are still affected by oscillations, causing a distorted output in figure 5.30, as expected based on simulations in figure 4.4. Although the power quality is compromised and there is still the need for compensation, compared to the results in 5.2.1, the stability and dynamics of reference tracking are not disturbed and the overcurrent doesn't disturb the inverter activation.

## 5.3 Conclution

In this chapter, the simulation for controller validation, 3.4, and case studies, 4 are experiments on the laboratory setup. The simulation results are confirmed on the physical system, proving the analysis and effect of grid voltage distortion on the controller. The MSRF-PLL-based controller is capable of filtering out the distortion and maintaining system connection during VSI startup. However, the oscillations in power and current tracking, causing output current distortions, proves that there is still the need for additional assessment and compensation.

# Chapter 6

# Conclusion and Further work

*In this section all the previous reasonings and analyses will be gathered and related to the objective of the project. In the first section, 6.1, all the dots from the introduction chapter, 1 until experimentation 5 will be connected, and the next section, 6.2, will discuss the possible related topics to be continued in the future.*

## 6.1 Conclusion

This project explains in section 1.1 the importance and potential of wind turbine systems in the electricity infrastructures along with the means and technologies for their integration in section 1.2. The third section of chapter one, 1.3, addressed the aspects of voltage distortion where the challenge of maintaining connection and startup in the distorted condition is addressed.

Chapter 2 expanded the theory and criteria of section 1.2 and using the tools in section 1.3.3 and additional considerations in 1.3.2, a simulation is modeled to perform the analysis. The models of distortion and system are validated using criteria in 3 then case studies are performed to observe the different aspects of the challenge. Finally, the validation and case studies are confirmed on a small physical laboratory setup.

The three steps of theoretical modeling, simulation, and experiments confirm the improvement of PLL's phase detector to obtain the fundamental positive sequence voltage that helps the controller maintain its stability, dynamics, and connection during startup transient. In theory, this topic is concluded in 2.8 and 2.11 describing the distortions and in 2.5 the way that it affects the controller is identified.

The scenarios analyzed in chapter 4, confirm the theory by demonstrating how classic SRF-PLL is being affected by the distortion and how MSRF-PLL is capable of filtering out the voltage distortions and satisfying the objective. As a disadvantage, it is mentioned that the system cannot fully comply with power quality criteria

therefore there is still the need for compensation. Similar results are confirmed using experiments on the Lab setup where the startup failure of the SRF-PLL-based controller indicates the importance of filtering out the distortion using a coupled network phase detector to maintain the system dynamics and stability, where utilizing the MSRF-PLL is a considerable solution.

## 6.2 Future work

At the start of the project, the topic of the robustness of the controller is introduced and in the end, the need for compensation is highlighted. Therefore, the potential for further work will be regarding the topics such as:

- Investigating the techniques for the robustness of the controller to fully comply with power quality, even for current. This requires analysis of criteria for current distortions and adding additional loops and decoupling network to the primary control level.
- Looking into the solutions for compensating for the distorted voltage condition on the grid. This requires analyzing the unbalance power theory plus harmonic compensation loops. This way the VSI outer loops are improved to have active filtering capability.
- Analyzing the further integration capability during disturbance conditions. The disturbance mitigations need to be analyzed using grid codes for fault-ride-through.
- Similar analysis can be performed using a more detailed model of a wind turbine system, taking into account the presence of a DC link, machine side converter, and mechanical and aero-dynamic system. Additional chapters can be included, each describing the performance of subsystems in additional scenarios.
- The analysis in this can be performed using modern control methods such as model-predictive control, robust control, or intelligence control. This requires updating the theory of controller design for such cases

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# Appendix A

# Experimental results

*In this appendix the results of experimental monitoring referenced in chapter 5 are mentioned. There are two sections including the output for experiments described in 5.1 SRF-PLL-based controller and the second section is for MSRF-PLL-based controller.*

## A.1 SRF-PLL-based controller

### A.1.1 Scenario 1

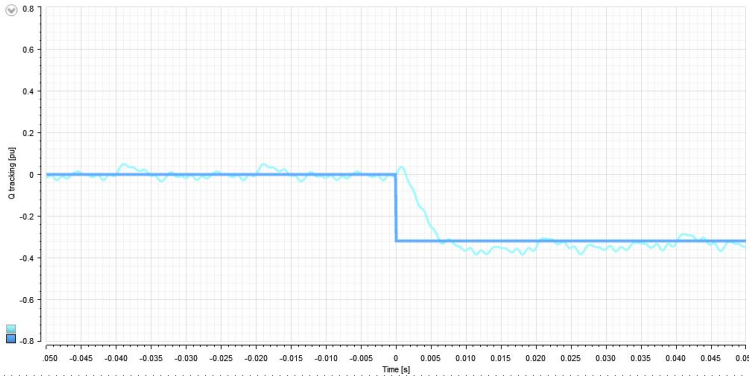


**Figure A.1:** Experiment 1: SRF-PLL-based $Q$ tracking

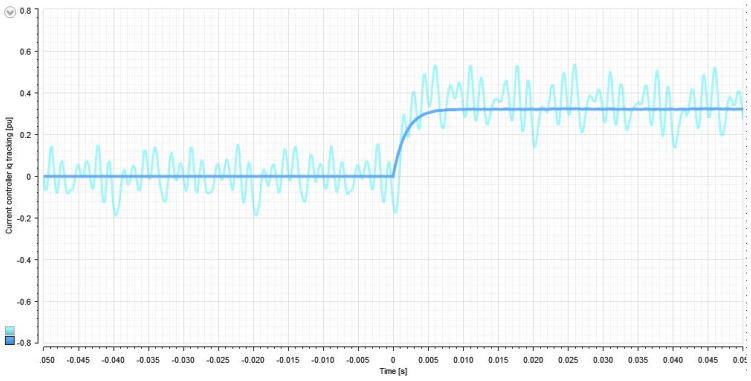


**Figure A.2:** Experiment 1: SRF-PLL-based $i_q$ tracking

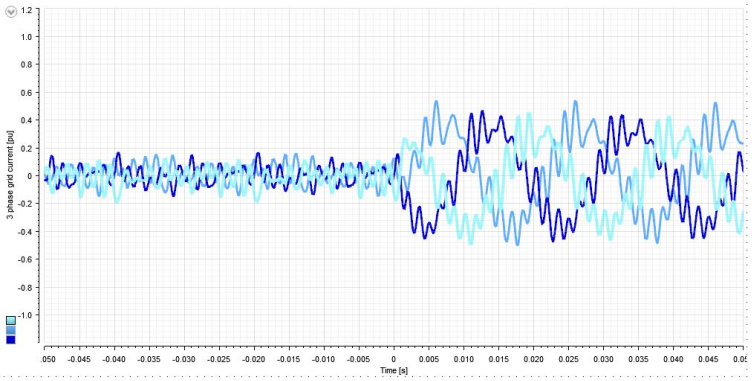


**Figure A.3:** Experiment 1: SRF-PLL-based $i_{abc}$ output

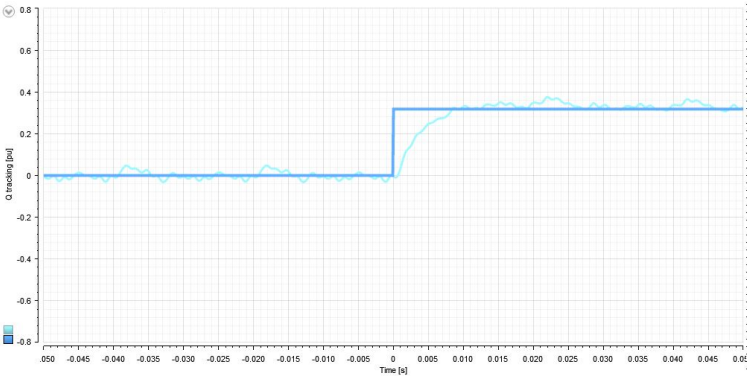


**Figure A.4:** Experiment 1: SRF-PLL-based $Q$ tracking

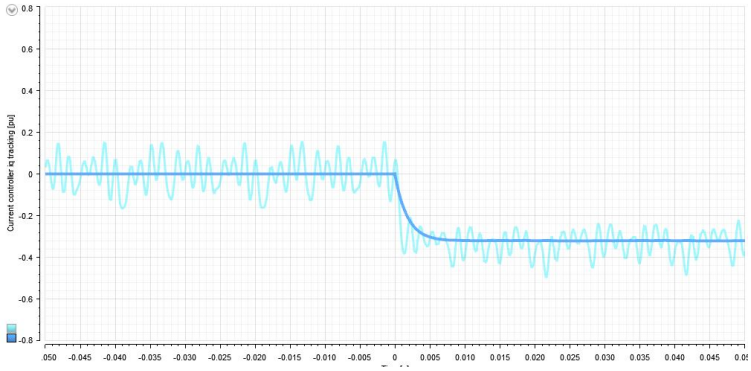


**Figure A.5:** Experiment 1: SRF-PLL-based $i_q$ tracking

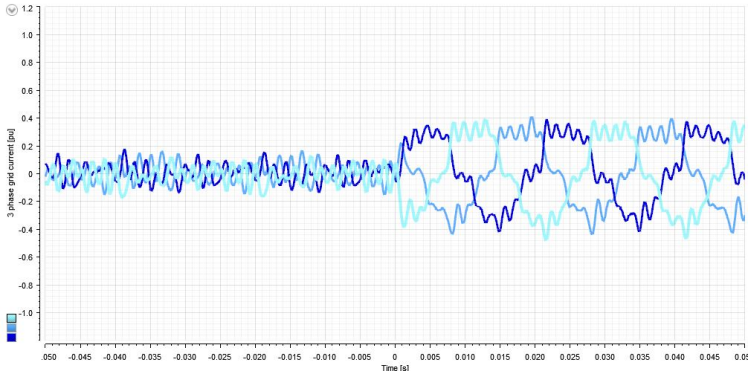


**Figure A.6:** Experiment 1: SRF-PLL-based $i_{abc}$ output

### A.1.2 Scenario 2

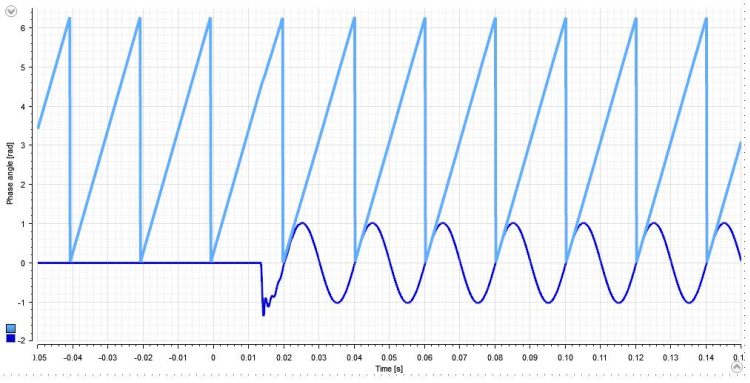


**Figure A.7:** Experiment 2: SRF-PLL-based phase angle tracking

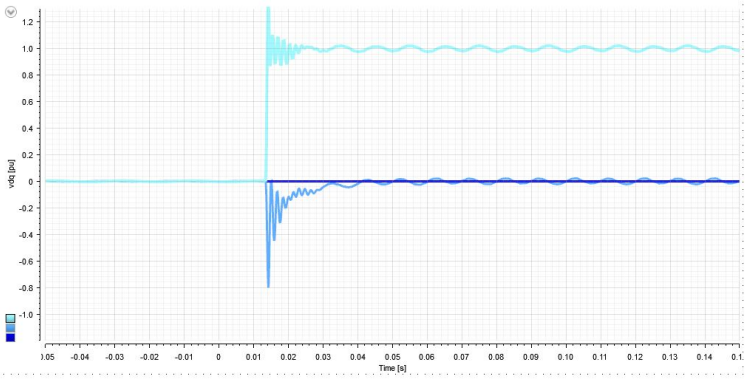


**Figure A.8:** Experiment 2: SRF-PLL-based phase detector output

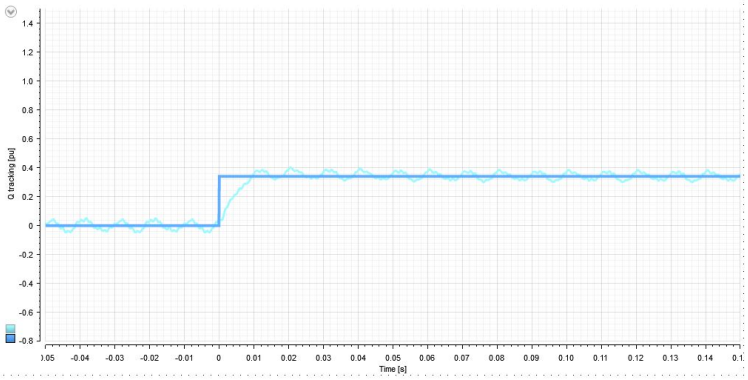


**Figure A.9:** Experiment 2: SRF-PLL-based $Q$ tracking

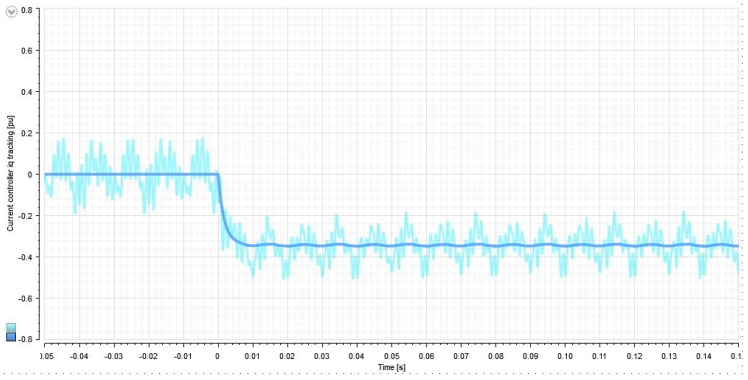


**Figure A.10:** Experiment 2: SRF-PLL-based $i_q$ tracking

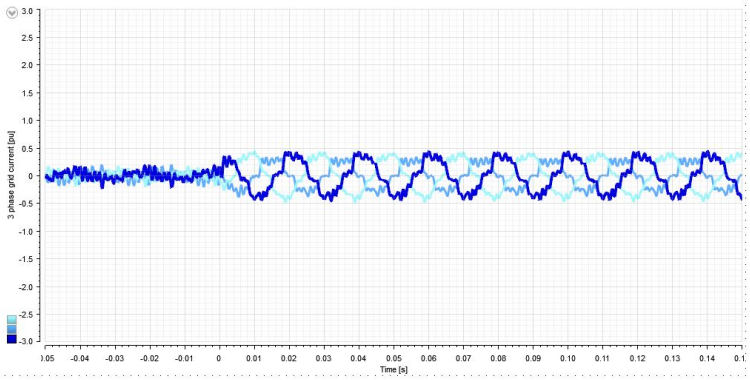


**Figure A.11:** Experiment 2: SRF-PLL-based $i_{abc}$ output

### A.1.3 Scenario 3

#### 5th harmonics

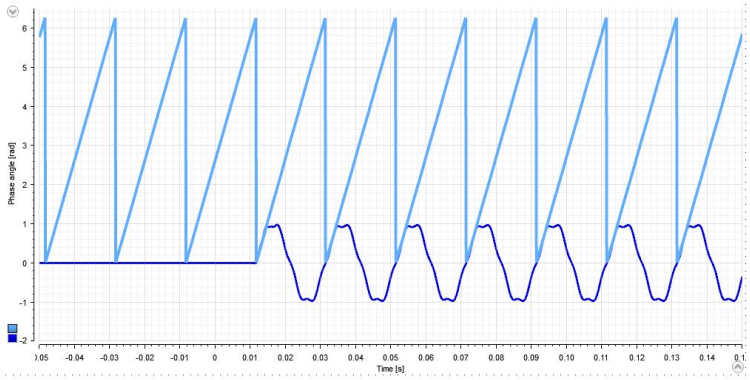


**Figure A.12:** Experiment 3: SRF-PLL-based phase angle tracking

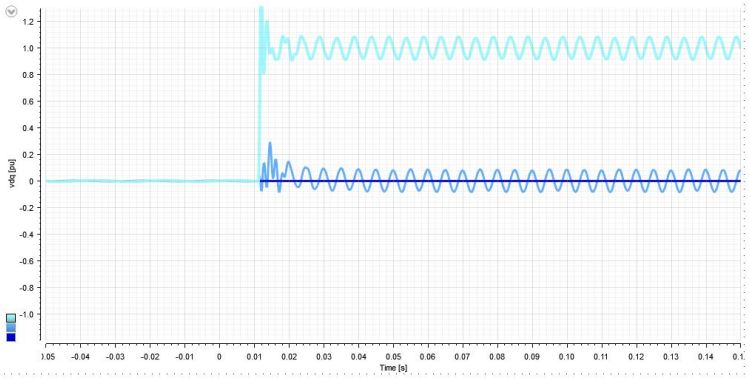


**Figure A.13:** Experiment 3: SRF-PLL-based phase detector output

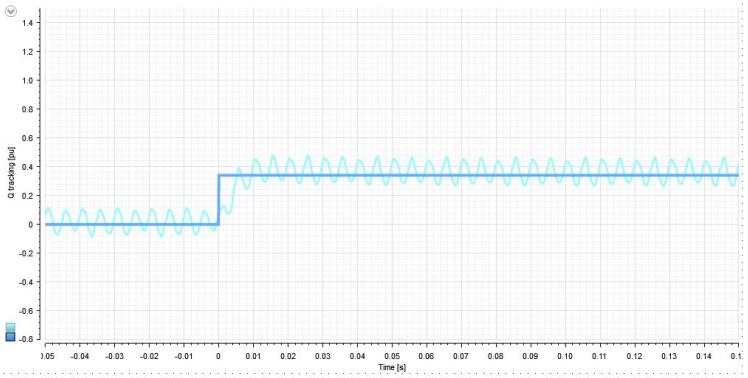


**Figure A.14:** Experiment 3: SRF-PLL-based $Q$ tracking

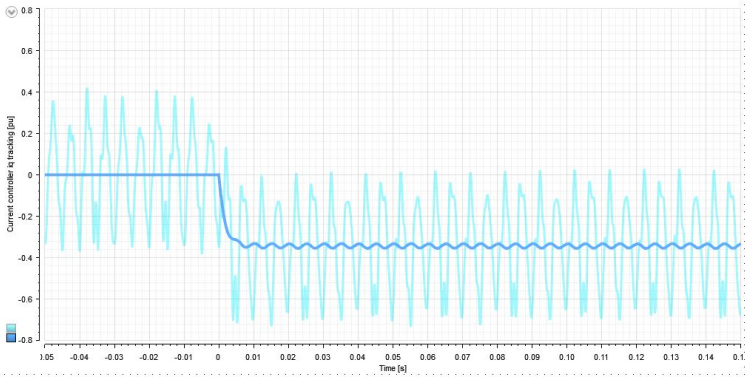


**Figure A.15:** Experiment 3: SRF-PLL-based $i_q$ tracking

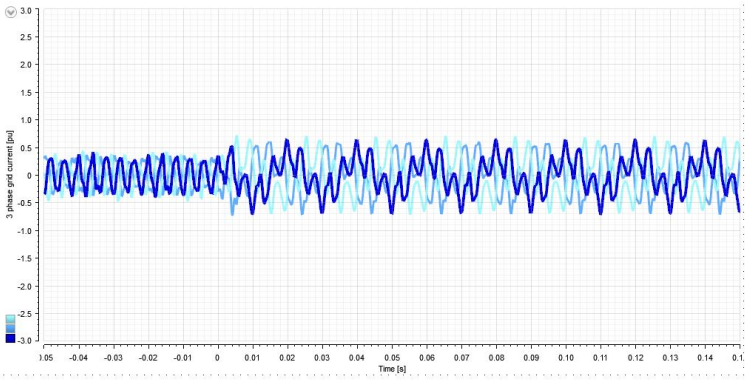


**Figure A.16:** Experiment 3: SRF-PLL-based $i_{abc}$ output

### 7th harmonics

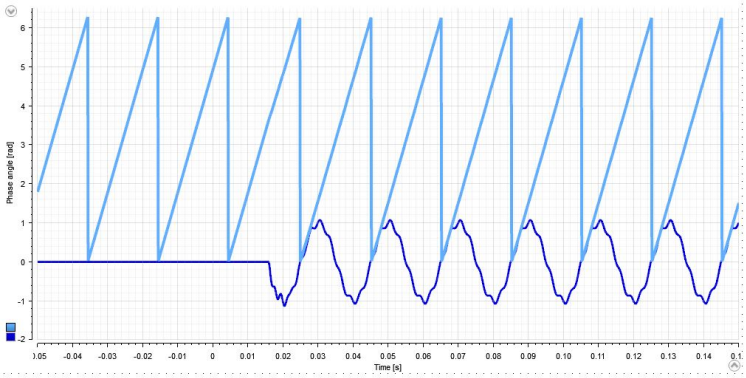


**Figure A.17:** Experiment 3: SRF-PLL-based phase angle tracking

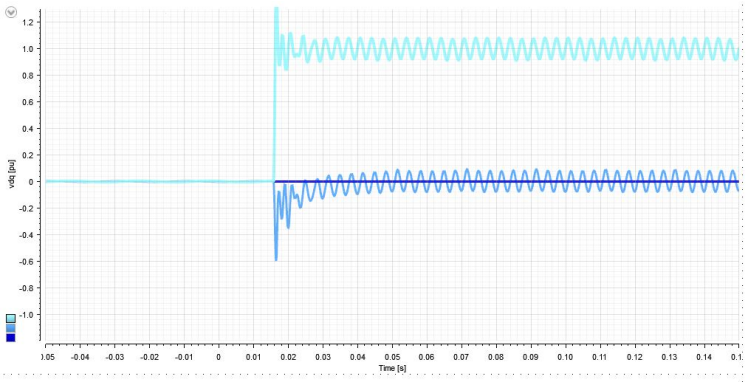


**Figure A.18:** Experiment 3: SRF-PLL-based phase detector output

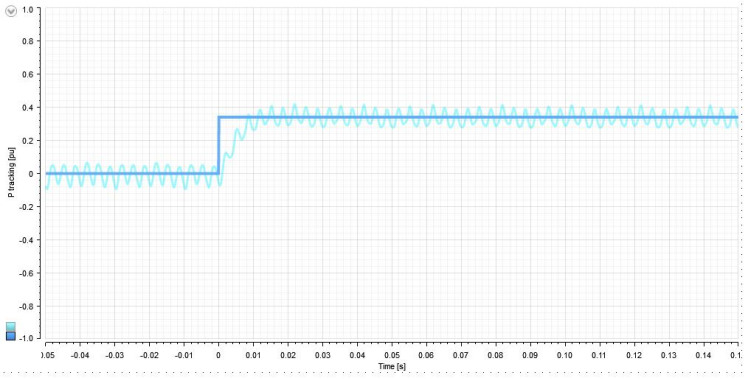


**Figure A.19:** Experiment 3: SRF-PLL-based $P$ tracking

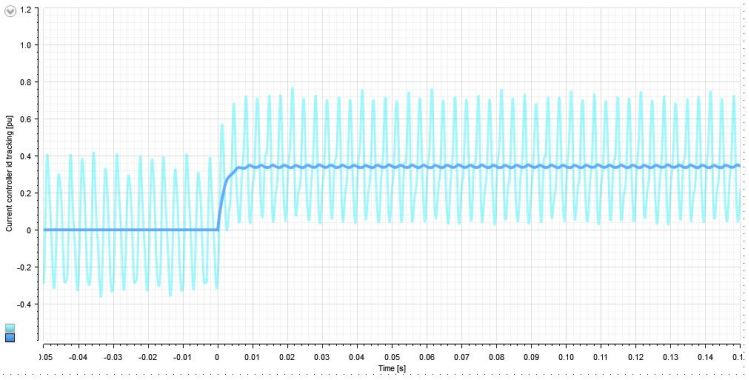


**Figure A.20:** Experiment 3: SRF-PLL-based $i_d$ tracking

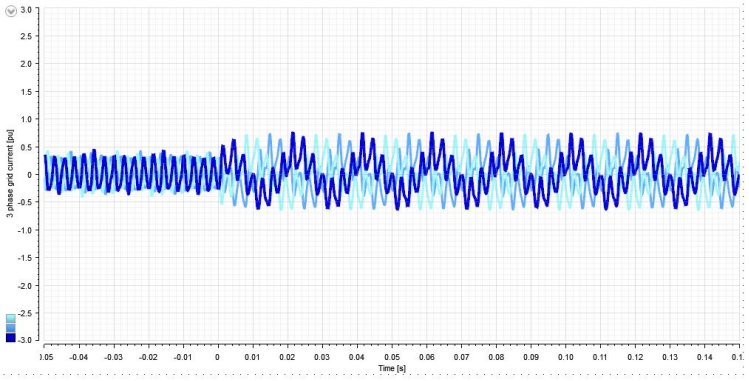


**Figure A.21:** Experiment 3: SRF-PLL-based $i_{abc}$ output

### A.1.4 Scenario 4

#### Unbalance and 5th harmonic

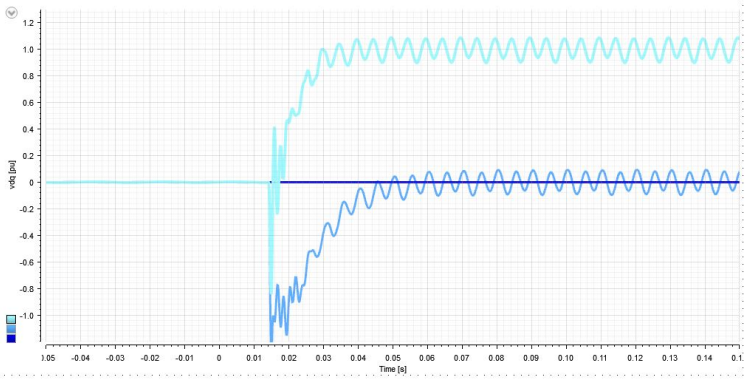


**Figure A.22:** Experiment 4: SRF-PLL-based phase angle tracking

## A.2 MSRF-PLL-based controller

## A.3 Scenario 2

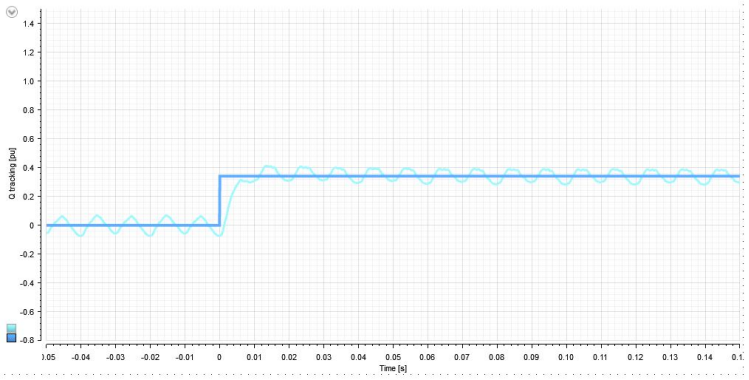


**Figure A.23:** Experiment 2: MSRF-PLL-based $Q$ tracking

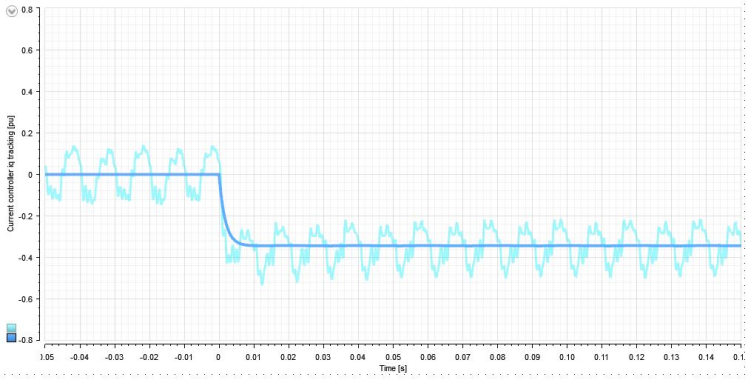


**Figure A.24:** Experiment 2: MSRF-PLL-based $i_q$ tracking

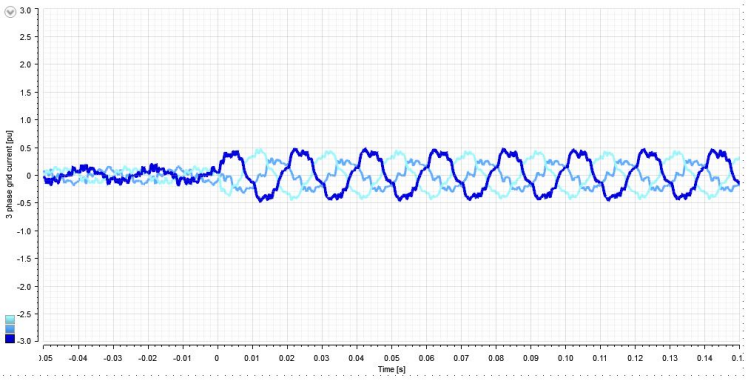


**Figure A.25:** Experiment 2: MSRF-PLL-based $i_{abc}$ output

## A.4 Scenario 3

### 5th harmonic

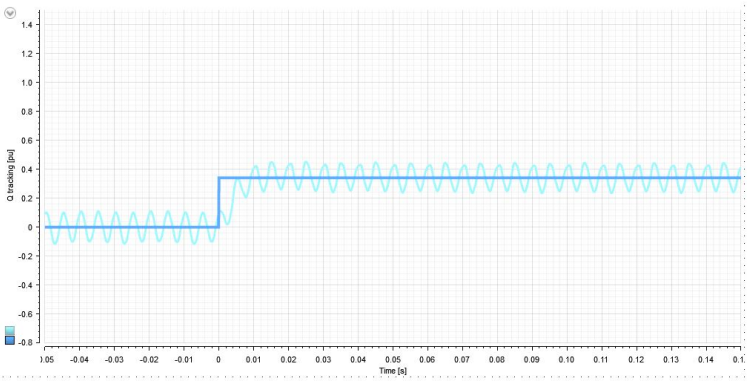


**Figure A.26:** Experiment 3: MSRF-PLL-based $Q$ tracking

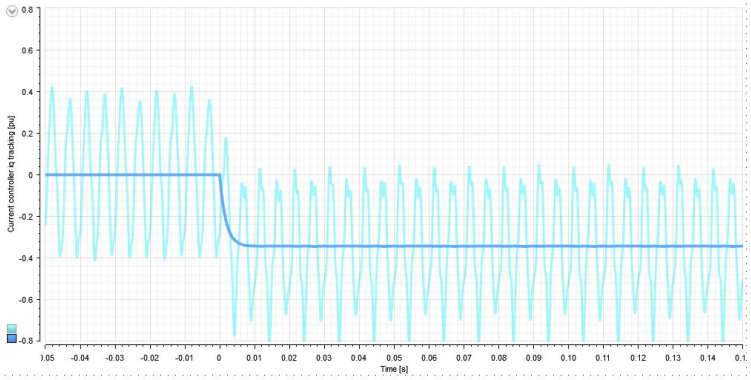


**Figure A.27:** Experiment 3: MSRF-PLL-based $i_q$ tracking

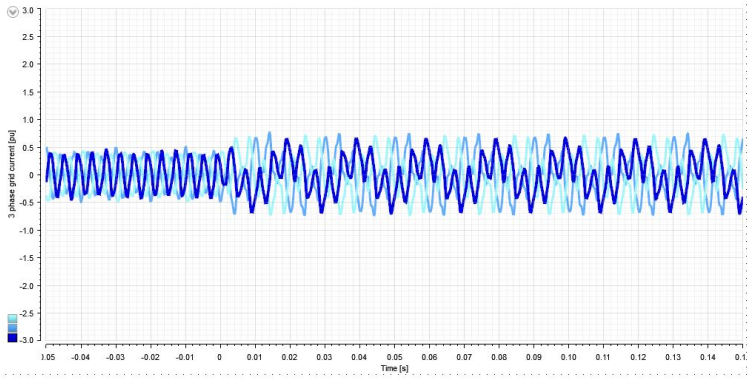


**Figure A.28:** Experiment 3: MSRF-PLL-based $i_{abc}$ output

### 7th harmonic

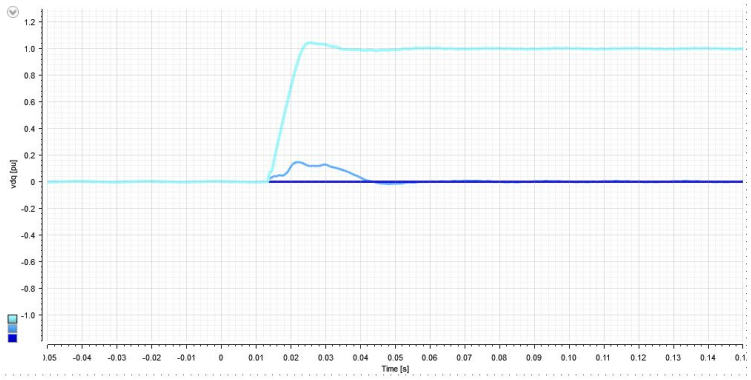


**Figure A.29:** Experiment 3: MSRF-PLL-based phase detector tracking

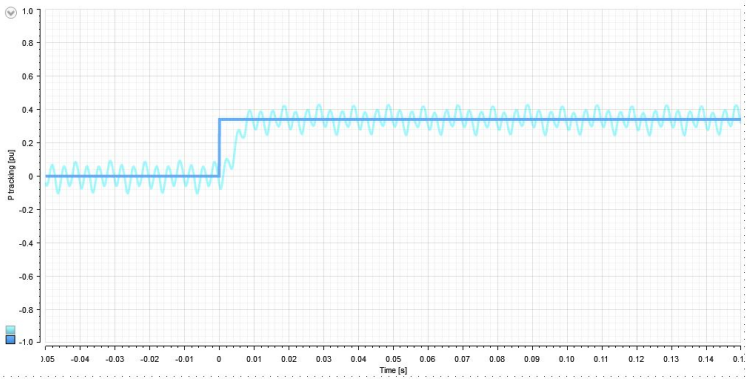


**Figure A.30:** Experiment 3: MSRF-PLL-based $P$ tracking

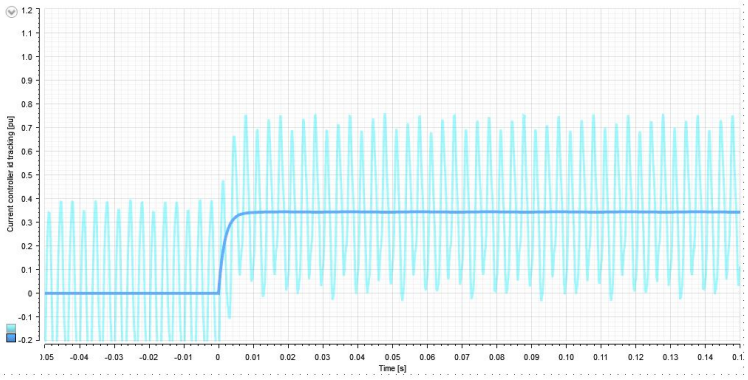


**Figure A.31:** Experiment 3: MSRF-PLL-based $i_d$ tracking

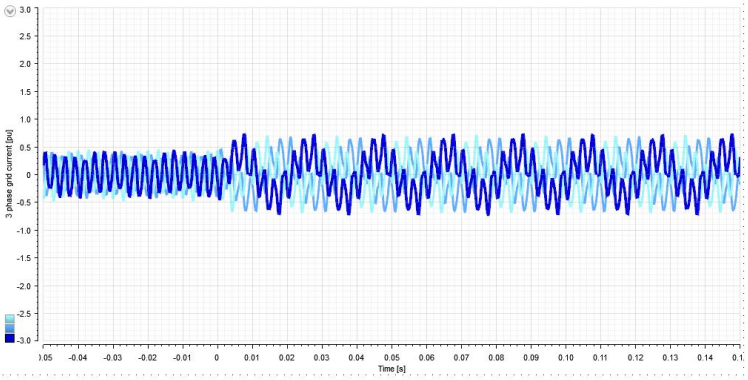


**Figure A.32:** Experiment 3: MSRF-PLL-based $i_{abc}$ output

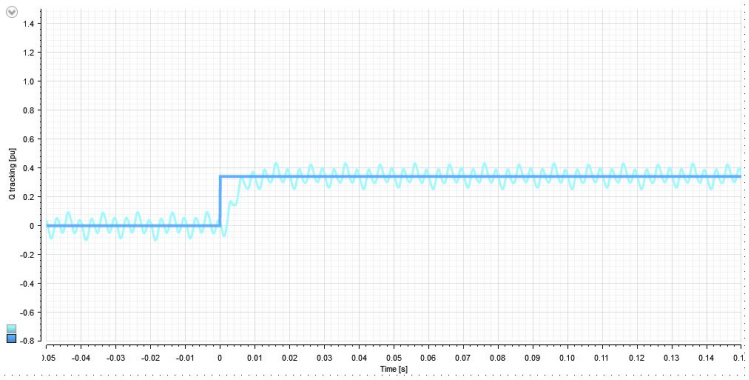


**Figure A.33:** Experiment 3: MSRF-PLL-based $Q$ tracking

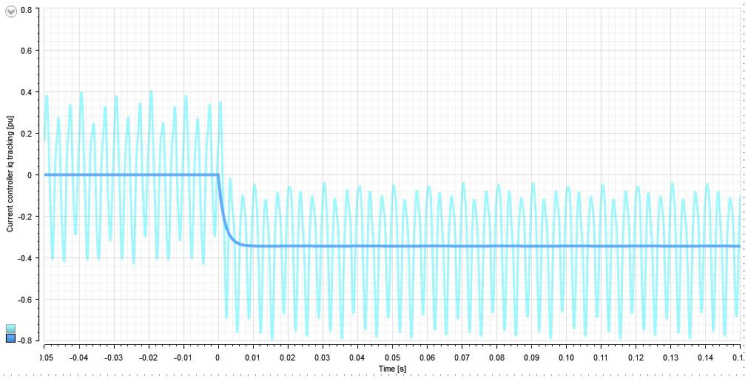


**Figure A.34:** Experiment 3: MSRF-PLL-based $i_q$ tracking

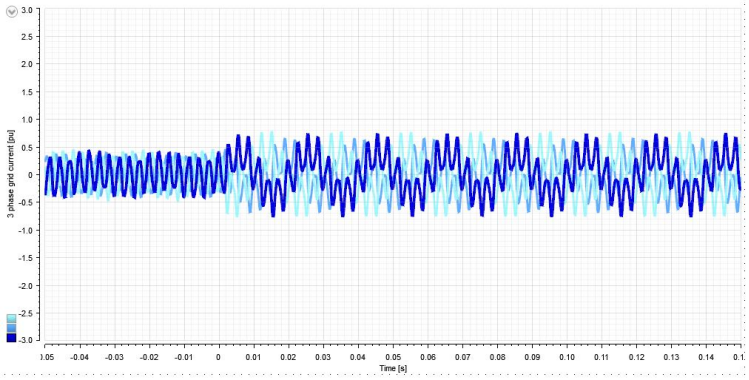


**Figure A.35:** Experiment 3: MSRF-PLL-based $i_{abc}$ output

## A.5 Scenario 4

### Unbalance and 5th harmonic

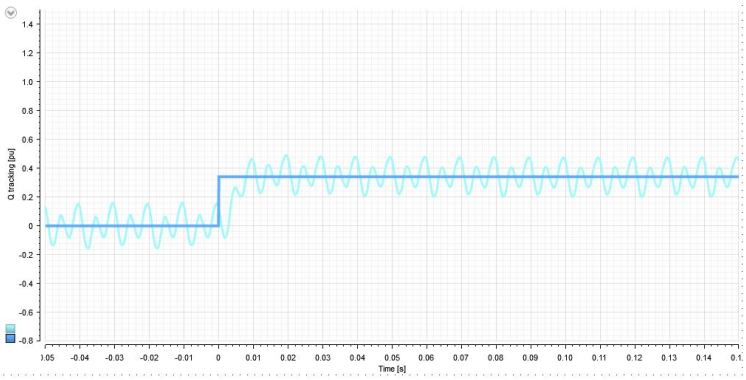


**Figure A.36:** Experiment 4: MSRF-PLL-based $Q$ tracking

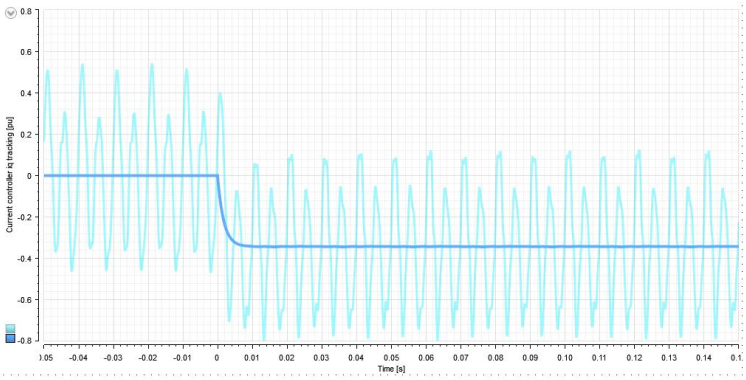


**Figure A.37:** Experiment 4: MSRF-PLL-based $i_q$ tracking

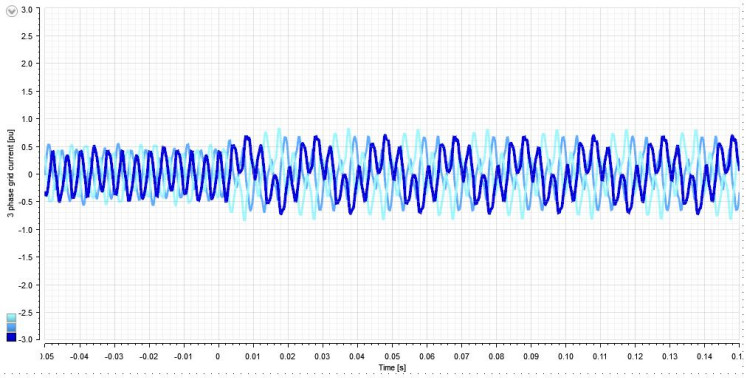


**Figure A.38:** Experiment 4: MSRF-PLL-based $i_{abc}$ output

### Unbalance and 7th harmonic

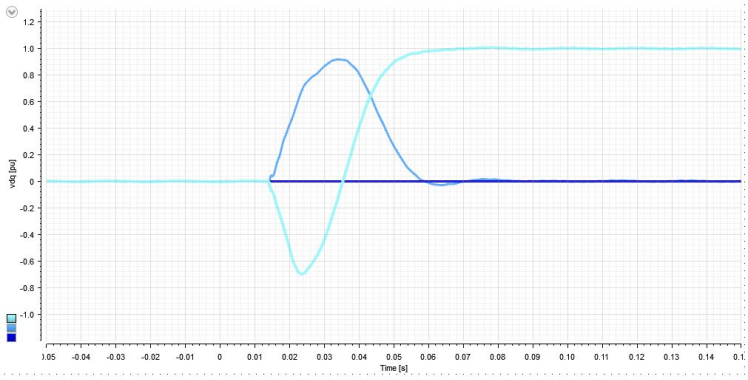


**Figure A.39:** Experiment 4: MSRF-PLL-based phase detector tracking

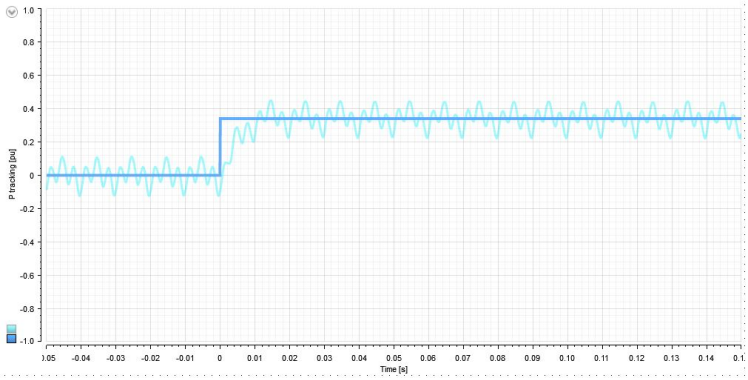


**Figure A.40:** Experiment 4: MSRF-PLL-based $P$ tracking

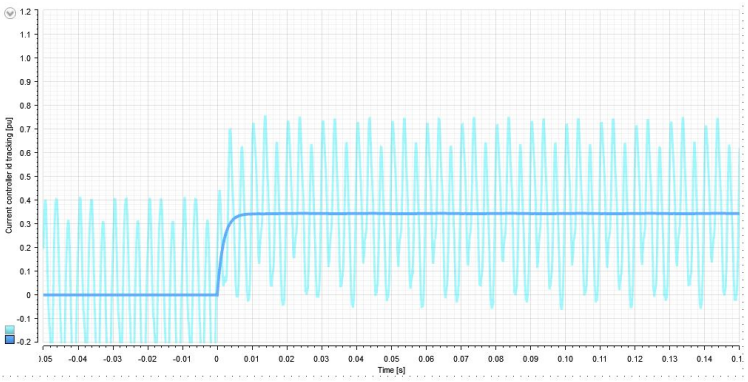


**Figure A.41:** Experiment 4: MSRF-PLL-based $i_d$ tracking

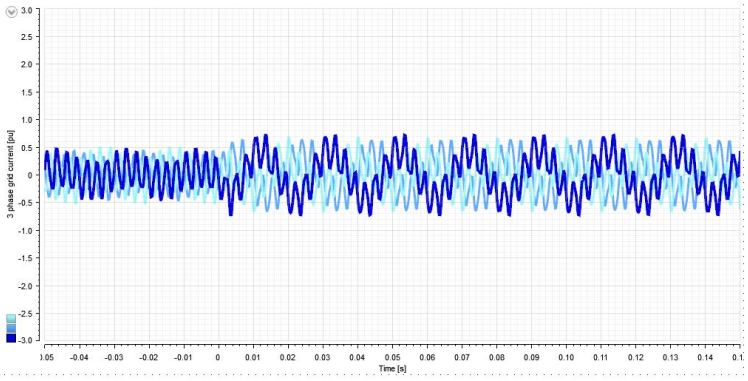


**Figure A.42:** Experiment 4: MSRF-PLL-based $i_{abc}$ output