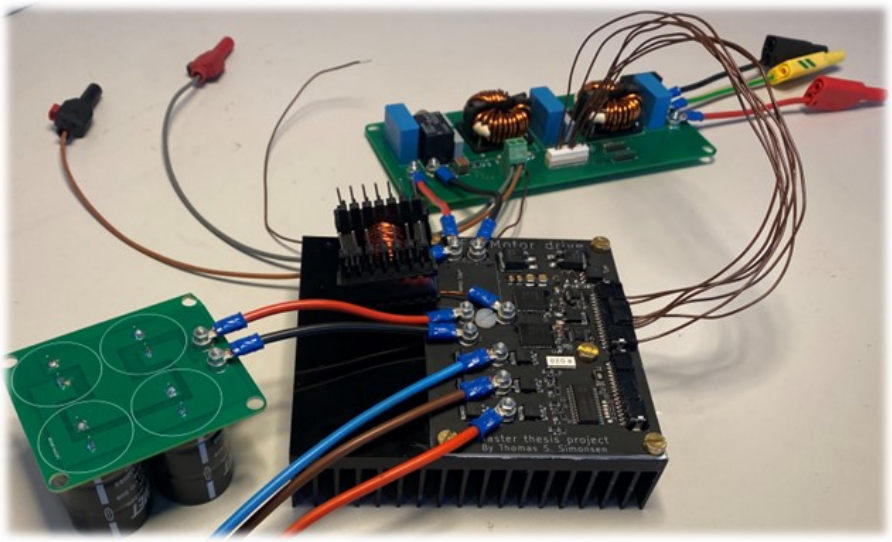
Master Thesis Project Report

Power Electronics and Drives

Design of Metal substrate PFC motor drive

-An investigation of thermal performance of IMS with WBG devices



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Abstract:

Power Electronic technology and optimization of its operation is becoming significantly more important as the electronic industry is growing. The industry moves towards higher power levels which demands greater efficiency in the power electronics converters and better thermal management. Compact and low-cost designs are always sought from the market, therefore the technology of Wide Band Gab (WBG) devices must be utilized alongside Insulated Metal Substrate (IMS) circuit boards. This combined area has not been thoroughly investigated and has not been put into use in the market. Due to that, a very interesting, highly relevant topic for improving Power Electronic technology. Research around different semiconductor devices, IMS materials and layouts, Power Factor Correction (PFC) topologies and operating conditions have been investigated, where the optimal design has been thoroughly considered. This report highlights the difficulties and experiences that were faced during the goal of developing a high performance single phase PFC motor drive.

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Acronyms

BTPPFC Bridgeless Totem-Pole Power Factor correction

CAD Computer-aided Design

CCM Continuous Conduction Mode

CTI Comparative Tracking Index

EEr EE-core round shaped

FEM Finite Element Method

FET Field Effect Transistor

GaN Galium Nitride

IGBT Insulated Gate Bipolar Transistor

IMS Insulated Metal Substrate

IPC Institute of Printed Circuits

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

PCB Printed Circuit Board

PFC Power Factor Correction

RCF Resin Coated Film

SiC Silicon Carbide

SMD Surface-Mount Device

TSP Target Support Package

WBG Wide Band Gab

Preface

This document constitues a project report assigned to 10th semester Power Electronics and Drives students as a part of the final Master Thesis project. It is prepared to give insight into investigating new technology or newsworthy topics and give an overview of experiences and processes that have been applied during the final semester. The main objectives of the project are to investigate how PFC converters can be optimized by changing the conventional Printed Circuit Board (PCB) material with an IMS utilizing the thermal capabilities of this type of PCB.

The inspiration for the topic was Danfoss Drives interest in optimizing and implementing new technology of existing PFC converters, making them more compact, and reducing cost and size of passive components, together with investigating and gaining experience on the switching characteristics of Galium Nitride (GaN) transistors on IMS circuit boards. Thanks to the guidance of Nicklas Christensen of Danfoss Drives and Szymon Beczkowski from Aalborg University, a greater knowledge of PCB design of power electronic converters has been obtained, including the process of developing a PFC motor drive setup

During the Master Thesis Project, many good insights and feedback were provided by the employees of Danfoss Drives and Aalborg University. Guidance and help from the supervisors have paved the way for the project. This project is a continuation of gaining experience in power electronics systems and drives, with much more to come in the future.

Danfoss Drives, Gråsten - Denmark, June 1, 2023

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Chapter 1

Introduction

Danfoss Drives is an engineering company and market leader in Power Solutions and Drives. The company is always striving to be in front of the technology race ensuring that they keep their market leading position. Drives is a subsidiary company of Danfoss A/S and are mainly focused on Power Electronics systems for driving motors. Their purpose is to contribute to the electrification of the world and create a sustainable future powered by electricity[1]. Developing more sustainable products demands high efficiency and less usage of materials therefore new technologies are needed to move towards even greener power electronic solutions.

These technologies would be WBG devices such as Silicon Carbide (SiC) and GaN semiconductors for obtaining low loss switching resulting in the possibility of increasing the switching frequency of the drives and thereby reducing the size of the passive components, making it more compact and cost-effective. Combining these low-loss semiconductors with a metal-core PCB also known as IMS will generate high-performance thermal management resulting in high-efficiency operation of the drive.

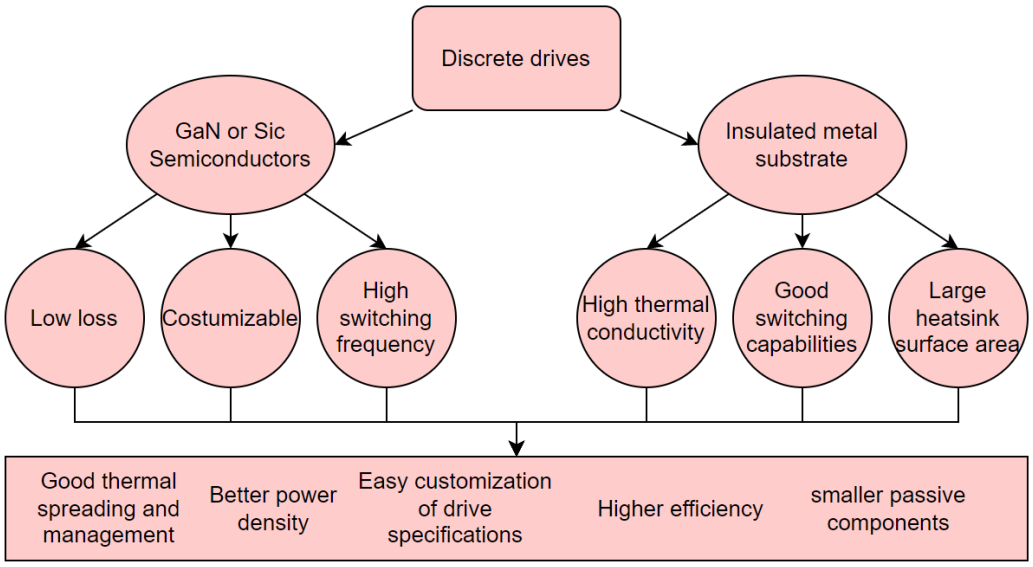


Figure 1.0.1: Benfitis from using WBG semiconductors and IMS circuit board

In Figure 1.0.1 it is visualized how the utilization of both WBG devices and IMS circuit board can enhance the overall performance of any given drive configuration. Here it should be highlighted that this is for discrete components only, since high-power devices would have power module packaging with die bonds and isolating silicon gel. This type of packaging reduces flexibility and removes the modulization possibilities of reusing different semiconductor types on the same circuit board. It is therefore interesting to investigate what power levels can be reached using the described IMS solution.

Chapter 2

Project Scope

2.1 Problem Definition

The use of power electronic devices in motor drive applications requires efficient thermal management, stable switching performance, and fast prototyping capabilities. The current state-of-the-art solutions for PFC converters in these applications rely on traditional PCBs which have limitations in terms of thermal management and the conventional power module packaging lacks flexibility and low production cost. As an attempt to overcome these constraints, the aim of this research is to investigate the feasibility of using IMS circuit boards to develop a PFC converter supplying a three-phase converter running a motor drive application. The research will focus on evaluating the thermal behavior, switching performance, and fast prototyping capabilities of the IMS-based PFC motor drive with high power density and low cost. The desired goal and optimization of PFC motor drives has given the following research statement to investigate and solve:

"Can insulated metal substrates satisfy the thermal requirements of a power factor correction motor drive utilizing high-efficiency wide bandgap devices reaching high power density and providing improved switching performance?"

2.2 Objectives

For overview purposes, the objectives of the project are stated to give an idea of the area of investigation, well as describing the potentials of the project, and what should be accomplished during the project. The objectives of the project can be divided into the following:

Main objectives

1. Develop a PFC converter on Insulated Metal Substrate.
2. Investigate the possibilities of increasing power density of PFC converters.
3. Test the thermal capabilities of IMS and dielectric materials.
4. Test the switching performance of WBG devices on IMS.
5. Analyze the advantages of using IMS compared to conventional PCBs.

Sub-objectives

1. Develop complete PFC motor drive on IMS, with supply PCB and Control circuit.
2. Test PFC motor drive only utilizing passive heat sink.
3. Test PFC motor drive with passive heat sink and motor fan air flow.
4. Test continuous operation of PFC and Three-phase motor drive.

Chapter 3

Processes and Methods

In this chapter, the experiences gained during the master thesis project are explained. The processes and methods used in the project to reach the objectives mentioned in the previous Section 2.2.

3.1 Project processes, experiences and methods

Throughout this master thesis project, the project processes and experience from previous projects have been used to create a good structure and workflow in the project. Therefore Jira software has been used to create a timeline with epics and tasks to complete. Since this is an individual project the timeline has been reviewed with Nicklas Christensen from Danfoss, to ensure a realistic timeline. The following timeline of the project looks as shown in Figure 3.1.1:

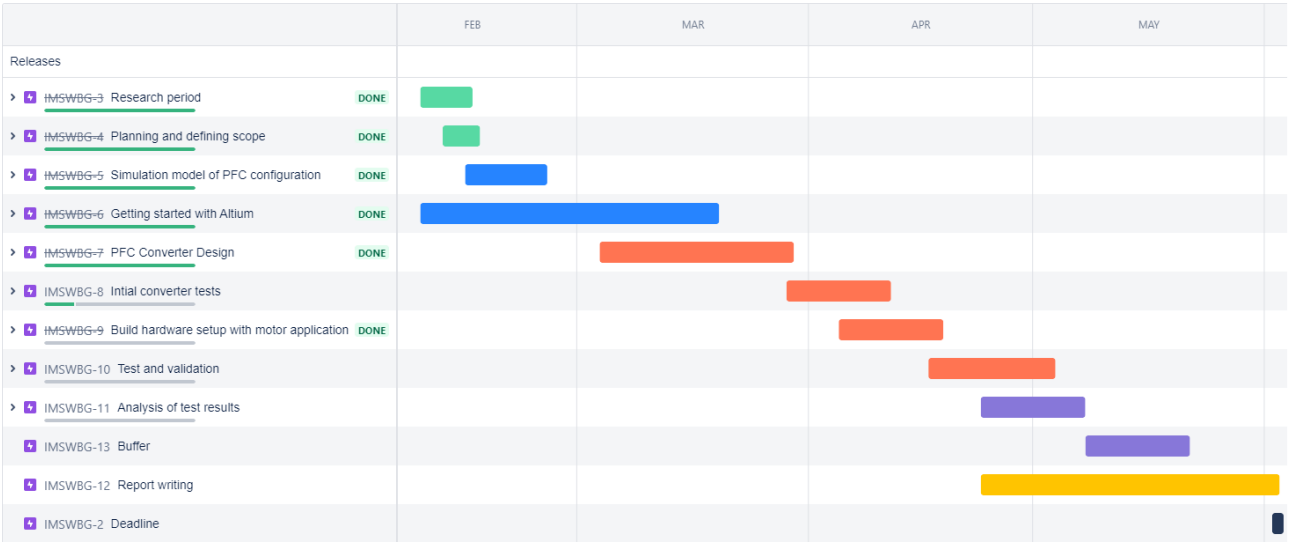


Figure 3.1.1: Project overview and timeline

The timeline is a guide to reach the different objectives in time, as this type of project can be difficult to structure properly due to unknown factors such as delivery times of ordering PCBs, and components and ensuring correct compatibility. Therefore this project has also been delayed significantly more than first planned as production of IMS PCB took 18 days from order to delivery. The soldering and assembly process was extended due to wrongly ordered IC footprints, connection terminals, and other placement issues. Developing hardware with a relatively high complexity on a 4-month project reduces the room for error and the time to rework all the difficulties and changes that have to be overcome to make the system work. The complexity of the system is big, which inevitably will increase the chances of delays.

As the first PCB design project, all these experiences from CAD models to physical assembly

have given a huge increase in hands-on experience in hardware design and the importance of creating a first prototype quickly to see the product as early in the design process as possible and from there optimize on the design, choosing a standard or commonly used component sizes such as connection terminals, newest footprints of ICs and SMD packages.

All of these design and assembly experiences have made it even more clear how iterative methods are important in hardware design. One more iteration of the design process would have improved the product significantly and made it easier to assemble and connect. Through the design process, the iterative method also has been used to develop the control as this had to be developed, run on the microcontroller, checked the pin outputs, and redo the control to adjust to the desired configuration. This was highlighted by the adjustment of the feedback loop scaling and offset since the signal outputs have to be tested before correct control can be implemented.

Lastly, the v-model Figure 3.1.2 has been used, when testing and doing rework, and running the supply PCB as well as the PFC motor drive IMS, this also has an iterative approach verifying and validating the expected working processes, making changes, and redoing the verification and validation process.

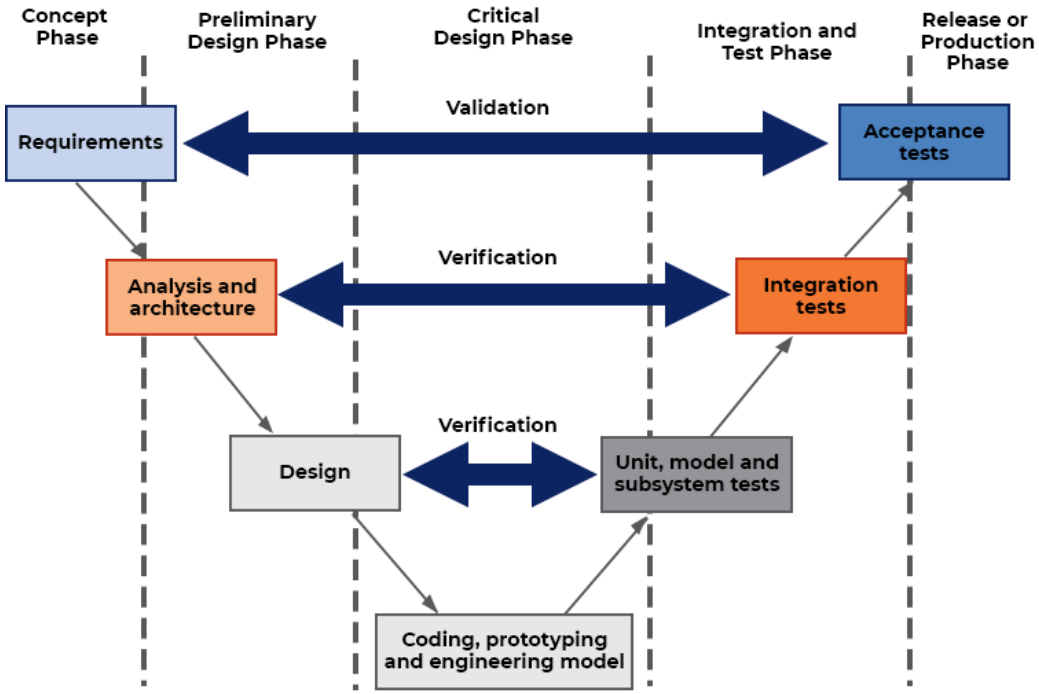


Figure 3.1.2: V-model for development and testing[2]

These development methods and processes have provided huge experience in hardware design, the iterative phases that are needed, and the importance of modularisation to ensure a sufficient connection between PCBs and sizes of footprints and package types. It has also increased the hands-on experience with the design phases of hardware, especially with the time distribution of assembly tests and rework on prototypes before the actual test can be carried out. It has also given a knowledge about why teamwork is important and that parallel processes increase the speed of the development processes significantly, which especially could have been used in a project like this. Hard work has made it possible to reach the following conclusions that can be drawn from this technology investigation project which are documented in the chapters to come.

Chapter 4

Optimal Design Research - Power Factor Correction Motor Drive

This chapter will describe the investigations and considerations of designing a power factor correction converter. Argumentation for making different design choices and parameter identification for optimal design. The chapter will give an overview of the different topics needed to develop a PFC converter on IMS substrate.

4.1 PFC converter topologies

A power factor correction converter is the first power-conversion stage between the grid and the system. It carries the entire load during operation and is required for every line-powered electrical product consuming more than 75W[3]. PFC converters have many different topologies and ways of operation but common for all PFC converters, they are designed for a universal AC input between 85VAC to 264VAC for single-phase applications.

The PFC converter can be divided into two categories, diode bridge topology and bridgeless topologies. The conventional and simple PFC converter topology is with a diode bridge for converting grid-connected AC to DC, often the conventional PFC also has a boost stage for creating a higher DC-Link voltage.

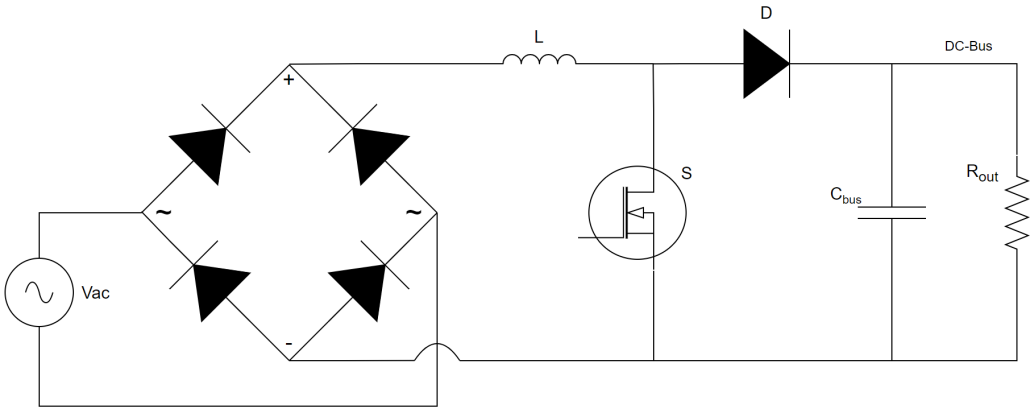


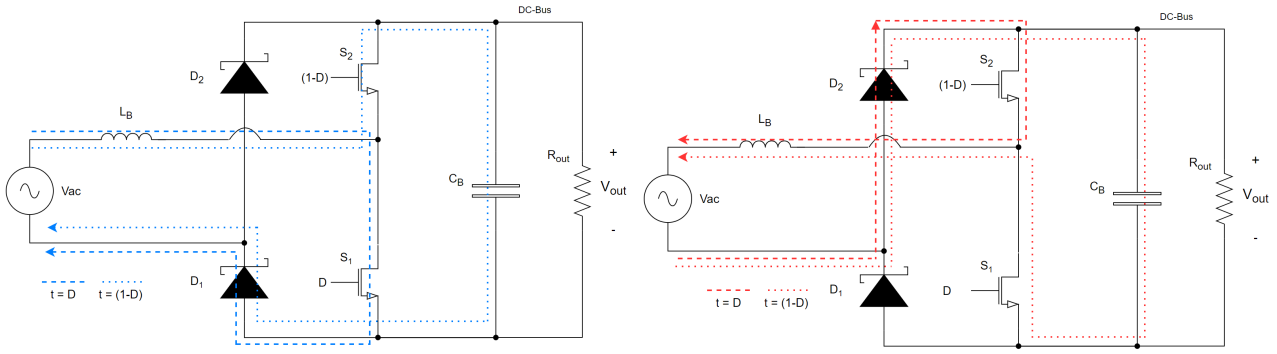
Figure 4.1.1: Convential PFC with diode bridge

In Figure 4.1.1 it can be seen that there is a diode bridge connected to the AC input, this ensures a DC-output after the diode bridge without any control scheme and the only losses added is the voltage drop across the diodes. The inductor and switch after the diode bridge is the boost stage where the inductor stores current and have a positive output RMS current with a ripple across, for the DC output boosting the voltage of the DC bus.[4]
For higher efficiency compared to the conventional PFC boost rectifier, a bridgeless topology can be used, this topology comes in different variations, depending on the desired perfor-

mance, complexity, and application needs. The different topologies of the different bridgeless power factor correction converters are:

- Basic Bridgeless PFC boost rectifier
- Basic Bridgeless PFC boost recitifer with bidirectional switch
- Bridgeless dual boost PFC rectifier
- Pseudo totem-pole bridgeless PFC boost rectifier
- Totem-pole bridgeless PFC boost rectifier

The main goal of bridgeless PFC topologies is to reduce the conduction loss by reducing the number of semiconductor components in the line current path. Since there are many different topologies as mentioned above, there are different things to consider. In this report, the main focus is to have a high-efficiency PFC for a motor drive application. From research the Bridgeless Totem-Pole Power Factor correction (BTPPFC) boost rectifier is the most efficient topology[5] due to the least use of components, the smallest conduction losses, a combination of active and passive components, produces a high voltage output with low output ripple, provides fast switching and good thermal performance, and thereby a high efficiency, high power density, and low EMI, together with the lowest complexity in terms of control strategies. The drawback of the BTPPFC boost rectifier is the non-bidirectional operation. The topology of BTPPFC boost rectifier is as shown in Figure 4.1.2a and Figure 4.1.2b:



(a) Positive AC half cycle

(b) Negative AC half cycle

Figure 4.1.2: BTPPFC boost rectifier

In Figure 4.1.2 it is shown how the single-phase cycles charge and discharge the PFC inductor and DC-link capacitor. In the positive half cycle Figure 4.1.2a the duty cycle value corresponds to the discharge time of the DC-link and the rest of the period is charging the DC-link. The PFC inductor is charged throughout the whole half-cycle period. In the negative half cycle Figure 4.1.2b the duty cycle time corresponds to the discharge of the DC-link and the rest of the period corresponds to charging the DC-link. The PFC inductor is charged throughout the whole half-cycle period. It can be seen that the diodes do not need to fulfill fast operating conditions as these will follow the input frequency which in this project will be a single phase AC grid input, and therefore have a frequency of 50Hz.

From all topologies researched it can be concluded that the totem-pole PFC has the best specifications for the desired PFC requirements. The totem-pole PFC topology has the following operating specifications[6]:

- High power density

- High efficiency
- Distributed heat
- Moderate cost
- Low EMI performance

The most important factors in this project are power density, efficiency, and heat distribution which are all great for this topology. Where cost and EMI performance are off lower prioritization.

4.2 Choice of semiconductor

The most important and critical component of any power electronic system is the semiconductor which is the switching device of any converter. As shown in the topology Section 4.1, the PFC converter needs two active switches and two passive diodes. Both of these devices are contributing with power loss when switching between on and off state. Therefore it is desired to choose the switches with the lowest loss contribution possible. In the power electronics industry, the most efficient semiconductors existing on the market are SiC and GaN and thereby also able to operate at higher switching frequencies, which is desired due to the reduction of passive components size. In this power electronics area, conventional Insulated Gate Bipolar Transistor (IGBT) and Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) are the workhorses of the industry and are the main devices used in power electronics today, but WBG devices are the scope of the investigation. The difference between the semiconductor types are shown in Figure 4.2.1:

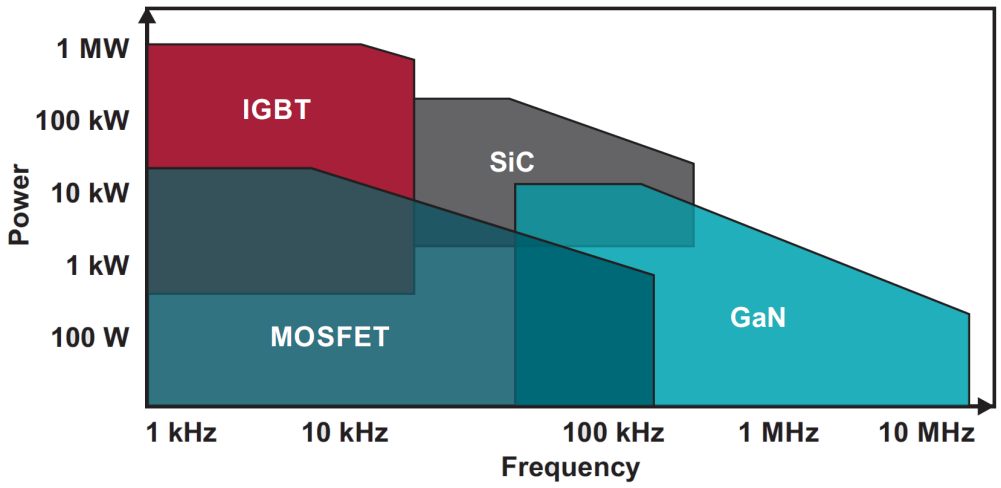


Figure 4.2.1: Power device mapping[3]

These fast-switching semiconductors are in the category of WBG devices, which are for semiconductor materials that have a larger band gap than conventional semiconductors. Between GaN and SiC it should be highlighted that SiC has higher voltage capabilities whereas GaN has lower gate drive losses. The comparison is shown in the following Table 4.1[3][7]:

Performance and benefits of GaN vs SiC			
Power needs:	GaN	SiC	SiC
Voltage levels	600V	650V	1200V
Power levels	$< 10kW$	$\leq 10kW$	$> 10kW$
Gate drive losses:			
Gate charge	1nC-Ω	2.66nC-Ω	4nC-Ω
Output charge	5nC-Ω	9.32nC-Ω	25nC-Ω
Typical operating conditions:			
Frequency	140kHz	100kHz	100kHz
Power density	$211 \frac{W}{in^3}$	$92 \frac{W}{in^3}$	$170 \frac{W}{in^3}$
Efficiency in BTPPFC	99.2%	99%	98.9%

Table 4.1: Performance and benefits of GaN vs SiC

From this Table 4.1 it is clearly highlighted that GaN semiconductors have a better performance in terms of gate drive losses, switching frequency, and power density for systems in the 600V area and less than 10kW power operation. All these performance areas apply to the desired PFC converter capabilities needed for the design. It should also be noted that GaN Field Effect Transistor (FET) has no body diode and therefore no reverse recovery, whereas SiC has a reverse recovery loss of more than 85nC. The drawback of using GaN semiconductors is low turn-on voltage, which makes them more sensitive to voltage changes, but integrated gate drives can reduce this exposure to interference.

This research can therefore conclude that for the desired operating conditions of the PFC converter GaN semiconductors would be the optimal fit due to low loss, high switching frequency, voltage, and power capabilities.

4.3 PCB layout - Thermal vs Electrical performance

In the power electronics industry, the thermal performance of any converter is critical for acquiring sufficient operating conditions. High thermal power dissipation is the most damaging factor of failure for a semiconductor device if not managed by spreading and allocating the dissipated heat into a passive or active heatsink. The tradeoff with good thermal capabilities is electrical performance. The best dielectric layers have inferior thermal conductivity, making heat transfer in the PCB very difficult. Increasing the number of layers in a PCB will improve the electrical performance of a PCB, because of optimal electrical circuitry and fewer loops for EMI/EMC interference. More layers however will result in more dielectric layers and increased thickness increasing the overall thermal resistance of the PCB. It is therefore crucial to find an optimal point between thermal performance and electrical performance.

4.3.1 PCB technologies

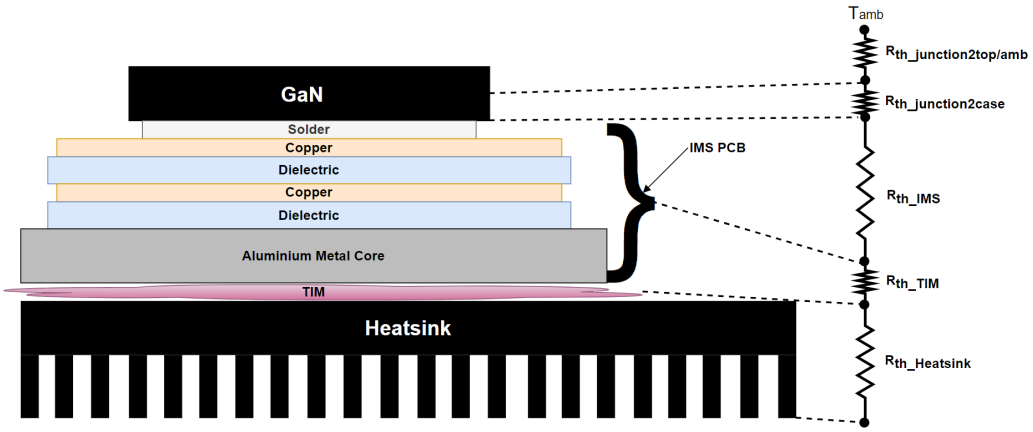
There are many different technologies in the production of printed circuit boards. The conventional PCB type is FR4 with through-hole capabilities and flexibility in terms of multilayer builds. Other PCB types are[8]:

- Aluminium PCBs
- Rigid-Flex PCBs

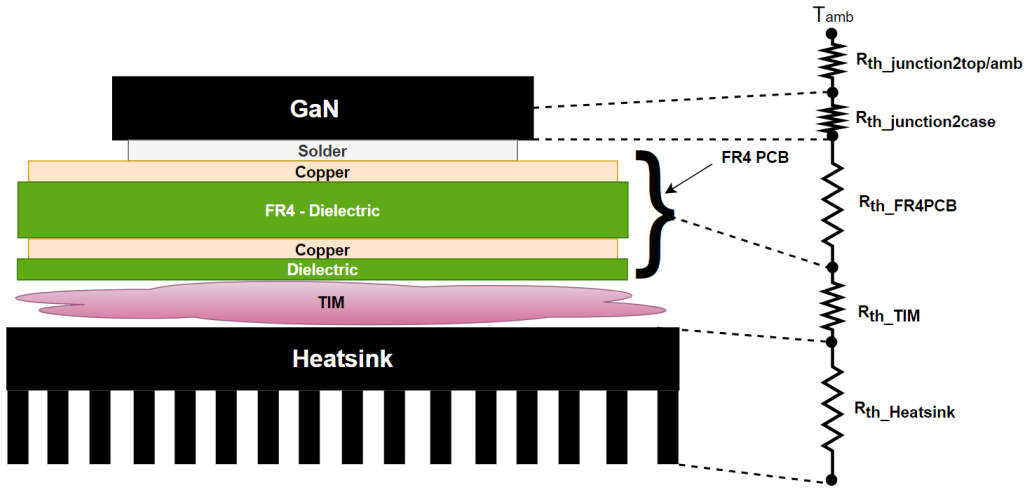
- Metal core PCBs
- Flexible PCBs
- High-Frequency PCBs
- High-TG PCBs
- Thick-Copper PCBs
- HDI PCBs
- LED PCBs

All these different PCB types have special capabilities for any desired specification. In this project, the desired specification is increased thermal conductivity, which therefore would be the Aluminium or Metal core PCBs due to the availability of different metal materials such as copper or other metals. More rare metals will increase the price significantly and therefore the most cost-beneficial metal core PCB is of aluminium.

It is important to have a good path and return path for the PFC converter a 2-layer PCB would be the best option, while still keeping a low thickness and a simple circuit design. For conventional FR-4 PCBs, it can be a double-sided build, because of the through-hole capability, making it possible to have only one dielectric layer. Whereas IMS PCBs generally are single-sided, ensuring an efficient baseplate area for heatsinks, low thermal resistance and strong mechanical strength. The IMS does not have through-hole capabilities and must therefore use Surface-Mount Device (SMD) components. The single-side necessity makes it unavoidable to have less than two dielectric layers, therefore the thermal conductivity of the dielectric layer will be crucial for the overall thermal resistance. A visualization of the two PCB types is shown in the following Figure 4.3.1[9]:



(a) IMS PCB



(b) FR4 PCB

Figure 4.3.1: Layer Stack-up Cross section of FR4 and IMS PCBs

As already mentioned the aluminium of the IMS has good thermal conductivity as a material. The PCB manufacturers have the possibility to produce PCBs with dielectric layers with a thermal conductivity of up to $3W/m \cdot K$ as default. From research, it has been found the dielectric layers can go up to $10W/m \cdot K$ using Aluminium Base Laminate from Ventec[10]. This Resin Coated Film (RCF) has the following capabilities shown in Figure 4.3.2:

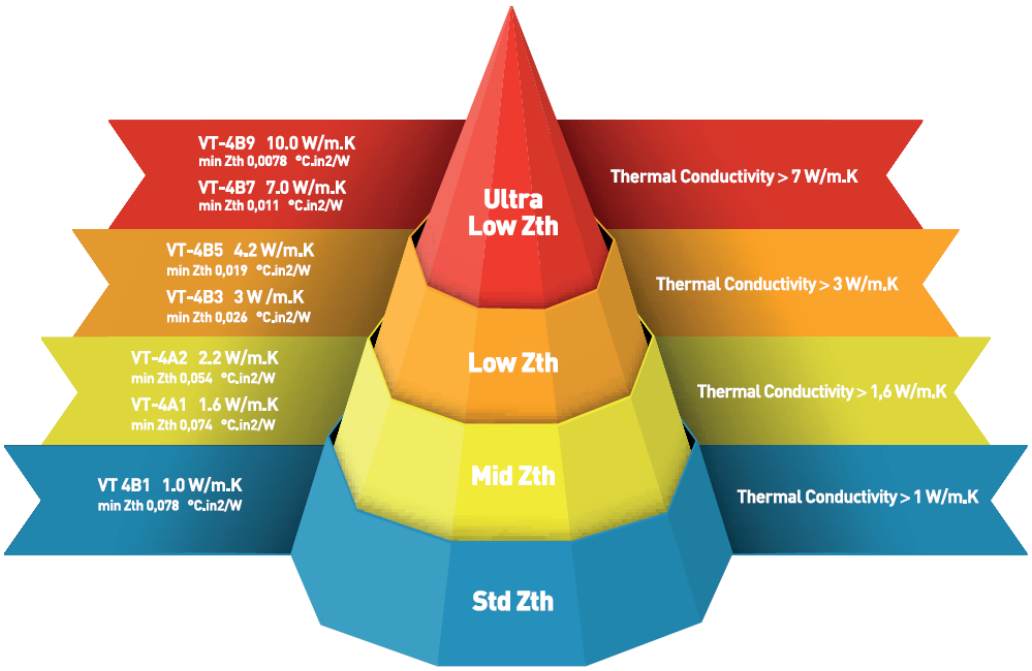


Figure 4.3.2: Ventec Aluminium Base Laminate / RCF (Resin Coated Film)[10]

When finding dielectric layers, the main purpose is to create isolation between the copper layers and the baseplate of the IMS. In the datasheet, these capabilities will be specified through breakdown voltage values and Comparative Tracking Index (CTI). The breakdown voltage levels are significantly dependent on the distance between two conducting materials or the thickness of the dielectric layer. For this material from Ventec, the breakdown voltage varies between 4kV and 12kV with a thickness of 50μm to 200μm, respectively. CTI is an index for specifying the electrical breakdown tracking properties of an insulating material, where tracking is defined as the formation of conductive paths due to electrical stress, humidity, and contamination. The better the insulation, the higher the CTI, which means a lower creepage distance is required, and the closer the two conductive parts can be[11]. The laminate from Ventec has a CTI of 600, which is the highest property of any dielectric laminate. This concludes that for an IMS, using the Aluminium Base Laminate from Ventec will ensure the best thermal and electrical performance in a two-layer single-sided metal core PCB.

4.3.2 Thermal resistance estimations of IMS and FR4 PCB

To prove that there is a thermal advantage in IMS compared to the conventional FR4 PCBs an estimation of the thermal resistances has been carried out. The thermal resistance of the heatsink is found in the datasheet of the heatsink. This thermal resistance varies depending on the convection and airflow through the fins of the heatsink. With natural convection, the heatsink thermal resistance lies between 8K/W and 2.9K/W[12], dependent on the power dissipated from the PFC motor drive. This thermal resistance can be reduced to between 1.5K/W and 0.4K/W with forced air[12], supplied by a fan. These calculations is with the assumption of a straight cut through the layers at the size of one semiconductor device of A = 12mm*12mm, so the thermal resistance is calculated for one GaN switch only. The thermal conductivity of the materials and the thickness are used for this calculation:

Thermal conductivity of materials

$$\sigma_{Al} = 210\frac{W}{m*K} \quad \sigma_{FR4} = 0.25\frac{W}{m*K} \quad \sigma_{TIM} = 0.69\frac{W}{m*K}$$

$$\sigma_{Cu} = 385\frac{W}{m*K} \quad \sigma_{dielectric} = 4.2\frac{W}{m*K} \quad \sigma_{solder} = 50\frac{W}{m*K}$$

Layer thickness

$$l_{Al} = 1500\mu m \quad l_{FR4} = 700\mu m \quad l_{TIM_{IMS}} = 100\mu m \quad l_{TIM_{FR4}} = 250\mu m$$

$$l_{Cu} = 70\mu m \quad l_{dielectric} = 152\mu m \quad l_{solder} = 25\mu m$$

Thermal resistances

$$R_{th_{alu}} = \frac{l_{Al}}{A*\sigma_{Al}} = 0.050\frac{^\circ C}{W} \quad R_{th_{FR4}} = \frac{l_{FR4}}{A*\sigma_{FR4}} = 19.44\frac{^\circ C}{W} \quad R_{th_{TIM_{IMS}}} = \frac{l_{TIM_{IMS}}}{A*\sigma_{TIM}} = 1.006\frac{^\circ C}{W}$$

$$R_{th_{TIM_{FR4}}} = \frac{l_{TIM_{FR4}}}{A*\sigma_{TIM}} = 2.516\frac{^\circ C}{W} \quad R_{th_{copper}} = \frac{l_{Cu}}{A*\sigma_{Cu}} = 0.001\frac{^\circ C}{W} \quad R_{th_{dielectric}} = \frac{l_{dielectric}}{A*\sigma_{dielectric}} = 0.251\frac{^\circ C}{W}$$

$$R_{th_{solder}} = \frac{l_{solder}}{A*\sigma_{solder}} = 0.003\frac{^\circ C}{W} \quad R_{th_{heatsink}} = 2.9\frac{^\circ C}{W}$$

From these thermal resistances an estimation of the differences between 1 layer and 2 layer IMS and conventional FR4 PCBs can be made, which is an extra copper layer and for IMS also an extra dielectric layer. The following thermal resistances of the different types are calculated:

IMS PCB single layer

$$R_{th_{IMS}} = R_{th_{solder}} + R_{th_{copper}} + R_{th_{dielectric}} + R_{th_{alu}} + R_{th_{TIM_{IMS}}} + R_{th_{heatsink}} = 4.212\frac{^\circ C}{W} \tag{4.1}$$

Conventional PCB single layer

$$R_{th_{PCB}} = R_{th_{solder}} + R_{th_{copper}} + R_{th_{FR4}} + R_{th_{TIM_{FR4}}} + R_{th_{heatsink}} = 24.87\frac{^\circ C}{W} \tag{4.2}$$

IMS PCB two layer

$$R_{th_{IMS}} = R_{th_{solder}} + 2*R_{th_{copper}} + 2*R_{th_{dielectric}} + R_{th_{alu}} + R_{th_{TIM_{IMS}}} + R_{th_{heatsink}} = 4.465\frac{^\circ C}{W} \tag{4.3}$$

Conventional PCB two layer

$$R_{th_{PCB}} = R_{th_{solder}} + 2*R_{th_{copper}} + R_{th_{FR4}} + R_{th_{TIM_{FR4}}} + R_{th_{heatsink}} = 24.87\frac{^\circ C}{W} \tag{4.4}$$

From these calculations, the IMS shows a significant improvement in the thermal performance of the PCB since the thermal resistance is almost 6 times lower for a single layer type Equation (4.1) compared to a conventional PCB Equation (4.2) and IMS has a 5.5 times lower thermal resistance for two-layer PCBs Equation (4.3) and Equation (4.4). This shows that there is a huge potential for utilizing the IMS PCB with the high thermal performance dielectric layer compared to conventional PCBs. It also shows that the IMS has a considerable advantage when it comes to thermal management. The FR4 will also be more inclined to create hotspots due to its poor spreading capabilities, a field where the IMS also is superior[9].

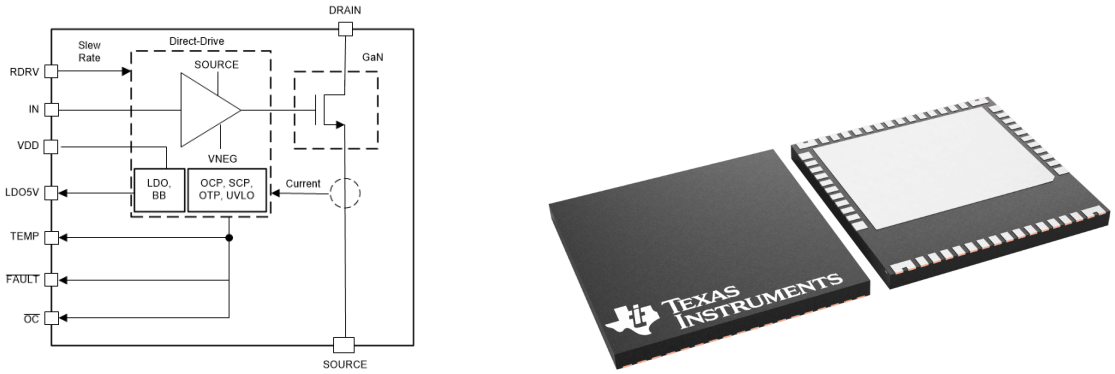
Chapter 5

PFC parameter identification

In this chapter, the design of the PFC motor drive will be described. This includes the sizing of passive components and component selection of ICs and switches. The initial requirements to specify for designing a PFC converter are the input and output. Here it was decided to use a single-phase grid-connected input of 230VAC, and the output should be around 2.2kW at approximately 400VDC. This would make it possible to create heat dissipation on the IMS testing the capabilities without being too ambitious with the power ratings. The topology is a BTPPFC consisting of two GaN switches, two passive diodes, PFC choke inductor, and DC-Link capacitors. The different component sizes are checked in PLECS simulation to verify sufficient operation.

5.1 GaN FET with integrated driver - LMG3422R030

For the switching half-bridge, the Texas Instruments GaN FET with integrated driver[13] has been chosen. The GaN switches are mainly used for high-power density industrial power supplies, solar inverters, and industrial motor drives or uninterruptable power supplies. These applications correspond closely to the PFC motor drive that is being developed. The main reason for choosing these switches is the low on-resistance of 30mΩ, high switching frequency, 600V operating voltage, integrated gate driver, and Surface mounted VQFN package. This fulfills all the requirements needed to create a high-power-density converter. The integrated driver can be seen in the block diagram Figure 5.1.1a and package in Figure 5.1.1b:



(a) Block diagram (b) VQFN Package

Figure 5.1.1: LMG3422R030 with integrated driver and bot side thermal pad

5.2 Diode half-bridge

The diodes are conducting with the grid frequency and therefore do not have to be fast since this is 50Hz and therefore the diodes are only commutating twice per 50Hz. The requirements from the diodes are mainly a sufficient forward current and high efficiency

in terms of low conduction and switching losses. The diodes do not need to be controlled. In the design guide examples, the evaluation boards use a MOSFET for this totem-pole leg. This is done to increase efficiency by removing the reverse recovery losses of the diodes, this would also add extra complexity to the control system which is not the objective of the project. Since the diodes are only commutating twice per 50Hz the reverse recovery losses will not be that significant. The diodes used in the PFC converter are VS-E5TX3006S2L-M3[14].

5.3 PFC Choke inductor

The purpose of the PFC Choke is to store current for conversion into DC controlled by the GaN switches in the totem pole configuration. To reduce the size of the inductor a high switching frequency is used, which is possible when using GaN switches and C2000 microcontroller. The size of the PFC choke is determined by the output power (P_o), input AC voltage(V_{AC}), output DC voltage(V_{DC}), maximum ripple and switching frequency($T = 1/fsw$) as shown in the following equation[15]:

$$L = \frac{1}{ripple} * \frac{V_{AC}}{P_o} * (1 - \frac{\sqrt{2} * V_{AC}}{V_{DC}} * T \tag{5.1}$$

$$L = \frac{1}{0.1} * \frac{230V}{2.2kW} * (1 - \frac{\sqrt{2} * 230V}{390}) * \frac{1}{300kHz} \tag{5.2}$$

$$L = 133.033\mu H \tag{5.3}$$

This gives a value of the inductor value needed to fulfill the requirements which also is shown in the simulation Chapter 6 to be within the ripple value. The maximum inductor current can also be calculated through the known variables as in the previous Equation (5.1). This is mainly dependent on the output power as shown in the following equation[15]:

$$I_L = \sqrt{2} * \frac{P_o}{V_{AC}} * (1 + \frac{Ripple}{2}) \tag{5.4}$$

$$I_L = \sqrt{2} * \frac{2.2kW}{230V} * (1 + \frac{0.1}{2}) \tag{5.5}$$

$$I_L = 14.204A \tag{5.6}$$

These values calculated in Equation (5.1) and Equation (5.4) will be the requirements of the PFC choke for obtaining the power levels desired. Where the minimum value of the PFC choke inductance is 133uH and the maximum current will be 14.204A.

A PFC choke varies in size and cost depending on the necessary requirements, in this project, the high switching frequency would decrease the size of the inductor because of the smaller current ripple, but would then need high switching frequency capability. There are numerous core materials and shapes for an inductor, but the best for high switching frequency is a ferrite core[16] due to the low core losses. The ferrite cores also comes with, good DC bias and low cost, which makes it ideal for optimizing a PFC converter. The shape of the core also provides some specific capabilities, for this project the EE-core round shaped (EEr) shape of the core is most suitable, because of the wide opening to accommodate space for large wires and several winding turns. The EEr shape has a round leg in the middle which makes a shorter path around, meaning lower wire length per winding. This reduces the conduction losses of the windings while still sustaining a high inductor value. The space between the legs also increases the flow of air which will keep the assembly cooler[17].

The core for the PFC choke used in this project is, therefore, a ETD 34/17/11 from TDK, where the numbers of the cores are the dimensions, which is critical for obtaining higher inductor value and saturation current.

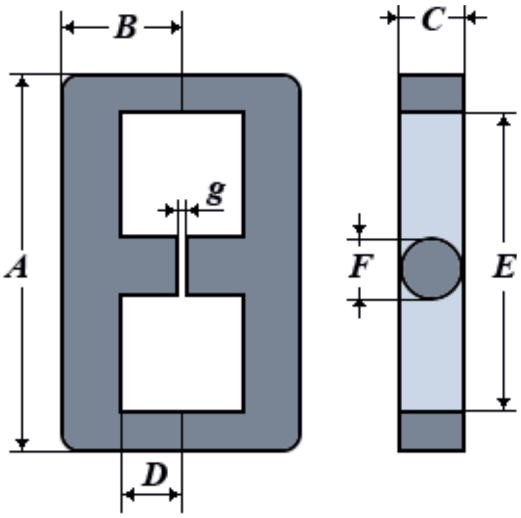


Figure 5.3.1: Dimensions of Ferrite EEr-Core[18]

In terms of saturation current the airgap between the middle leg of the two cores is significant. To calculate the turns and airgap needed to develop a sufficient PFC choke the online inductor calculator has been used from coil32[18]. After the wrapping of the inductor with the e-core the inductor value was as estimated from the online tool, which therefore validates its accuracy, the site also refers to the calculations made for estimating the number of windings. The dimension variables of the EEr core are described in Figure 5.3.1:

E-core calculation Inputs		
Parameter	Value	Variable
L	160μH	Required inductance
A	34mm	Dimension A
B	17mm	Dimension B
C	11mm	Dimension C
D	11.8mm	Dimension D
E	25.6mm	Dimension E
F	11.1mm	Dimension F
g	2mm	Center post gap
μ_r	1650	Relative magnetic permeability
EEr-core calculation Outputs		
Parameter	Value	Variable
N	52	Number of turns
le	77.917mm	Effective magnetic path length
Ae	99.217mm^2	Effective cross-sectional area
Ve	7730.664mm^3	Effective core volume
Ip	9.6736A	Peak current limited by the core saturation

Table 5.1: Inductor design

The values needed for the inductor design are only the number of turns since the air gap and dimensions are already chosen. This number of turns will be needed to obtain the 160μH.

The larger the air gap the higher the peak of the saturation current, but also more turns of the windings to obtain the same inductor value. The higher the inductor value needed the more turns needed with the same airgap. These are the critical variables when designing the inductor. It should also be noted that the flexibility in the inductor design process makes it possible to evaluate which type of loss would be less significant depending on the system requirements, core losses, or conduction losses. Here, core losses for an E-core might be easier to cool, compared to winding losses.

5.4 DC-Link capacitor bank

The purpose of the DC-Link is to reduce the ripple of the DC voltage across the output terminal, this ensures a smooth output voltage without a large drop or rise due to the charge and discharge. The capacitors' size depends significantly on the maximum voltage deviation from the desired output voltage to reduce the low-frequency voltage ripples which is a consequence of a single phase topology. Where a three phase system would have constant power since they are balanced, and not contribute with a voltage ripple, which is the case for single phase systems. The following Equation (5.7) was used to calculate the capacitor value of the bank[15]:

$$C = \frac{P_o}{2 * \pi * f_{line} * V_{ripple} * V_o} \tag{5.7}$$

$$C = \frac{2.2kW}{2 * \pi * 50Hz * 20V * 390V} \tag{5.8}$$

$$C = 897.8\mu F \tag{5.9}$$

The lower the allowed voltage variations the higher the capacitor value, since this project is trying to develop a compact PFC converter the allowed voltage variation was set to 20V, since half of the voltage variation would double the capacitance needed. For the PFC converter 4 electrolytic capacitors of 270μF are used giving a total capacitor bank of 1080μF

5.5 Identified parameters

From the previous calculations, it is now possible to test if the identified parameters of the components live up to the specifications used. This can be done through simulation in PLECS which has been made in Chapter 6 below. The significant things to focus on are the input current ripple and the output voltage deviation from the reference voltage.

Chapter 6

Simulation of PFC motor drive

This chapter will perform preliminary tests of the PFC motor drive. The simulation will confirm the design choices taken in the previous and show the power losses created by the operation of the converter and the three-phase inverter. The simulations of the PFC motor drive are performed separately as a PFC converter and a three-phase inverter. The main focus of the simulation model is to test the inductor design ensuring acceptable input current and ripple, the DC-link capacitor design ensuring an acceptable output voltage and voltage ripple, and lastly validate the thermal resistances and thermal performance differences between IMS and FR4 PCBs, and their performance limits.

6.1 Simulation of Power Factor Correction Converter

As mentioned in the previous Chapter 4 the PFC converter topology is chosen as a BTPPFC converter, using GaN switches as the first leg of the converter and diodes as the second leg. The following simulation Figure 6.1.1 was done in PLECS, utilizing their electrical and thermal domain, and inserting manufacturer models created for PLECS to include real power loss and temperature values represented by turn-on and conduction losses of the GaN switches as a function of the device voltage and current, this also applies to the diodes.

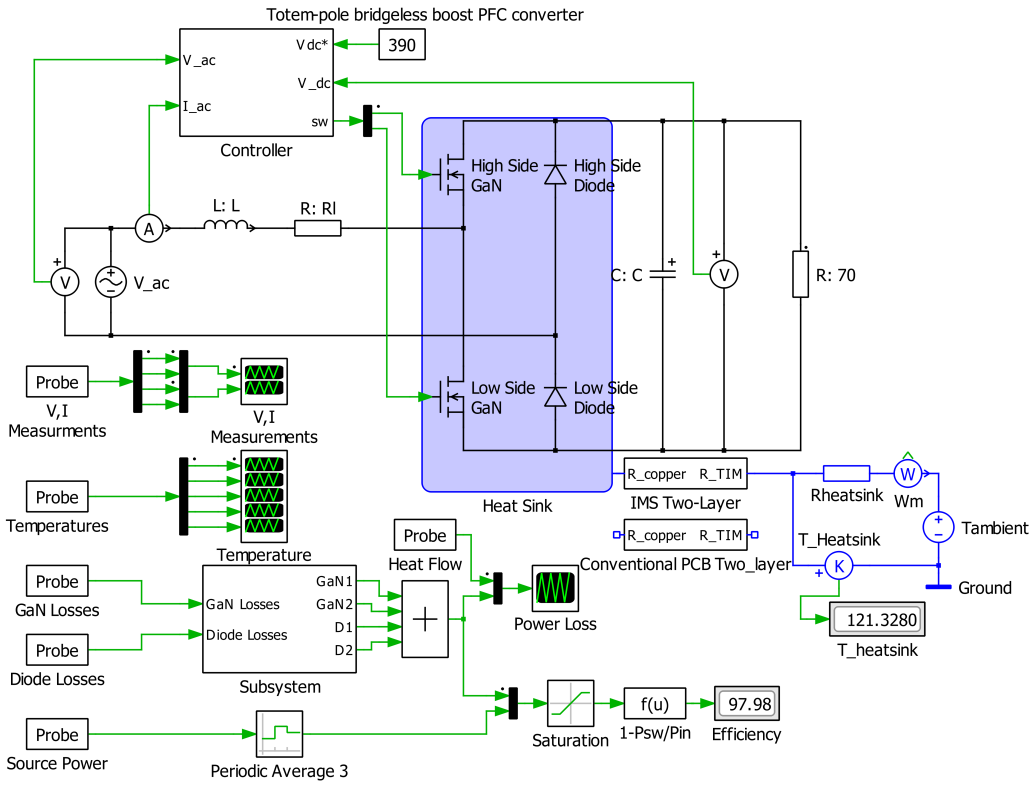


Figure 6.1.1: Simulation model of PFC converter with thermal loss calculation

In the simulation model Figure 6.1.1 it should be mentioned that the symbol of the GaN switches is represented as a MOSFET, but should be seen as a GaN switch. Texas Instruments has made a PLECS model of the GaN switch, which is inserted through the thermal domain of PLECS. This also applies to the diodes, even though the diodes are not represented with the exact diodes as described in the parameter identification Chapter 6. Even though the diodes do not have the exact power loss values they are close to and would therefore still give an indication of the temperature and power loss. This simulation model is inspired by the demo models of PLECS, where they have a representative model of the totem-pole bridgeless Boost PFC converter[19]. The control structure of their model is adapted to fit my application, and adjustments were made to switching frequency and resonance controller to enable stable operation.

Through this simulation model, the conversion from single-phase AC to boosted DC can be investigated. The important factors to explore are the DC voltage following the reference voltage with acceptable voltage ripple, input current and current ripple. When running the simulation the following DC-voltage and AC-current are obtained Figure 6.1.2:

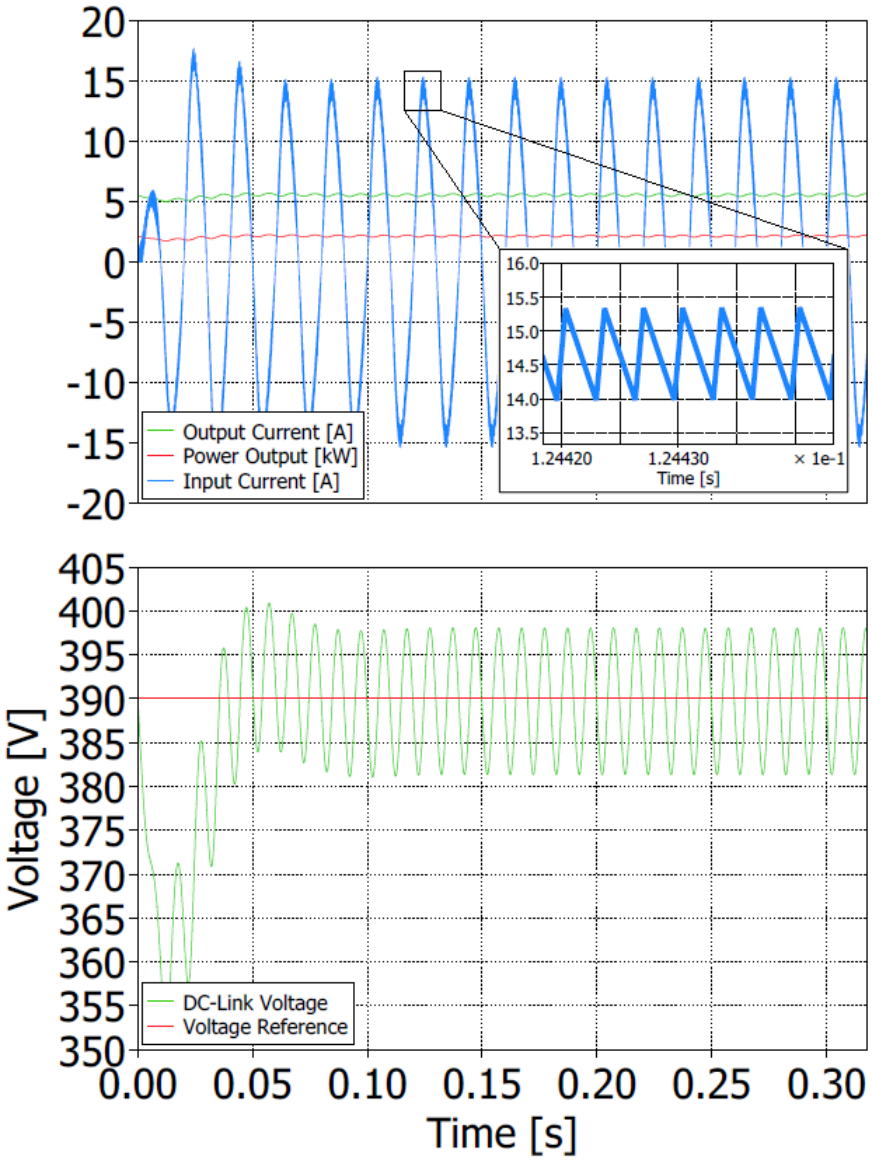


Figure 6.1.2: AC and DC Currents, Power Output, and Output voltage

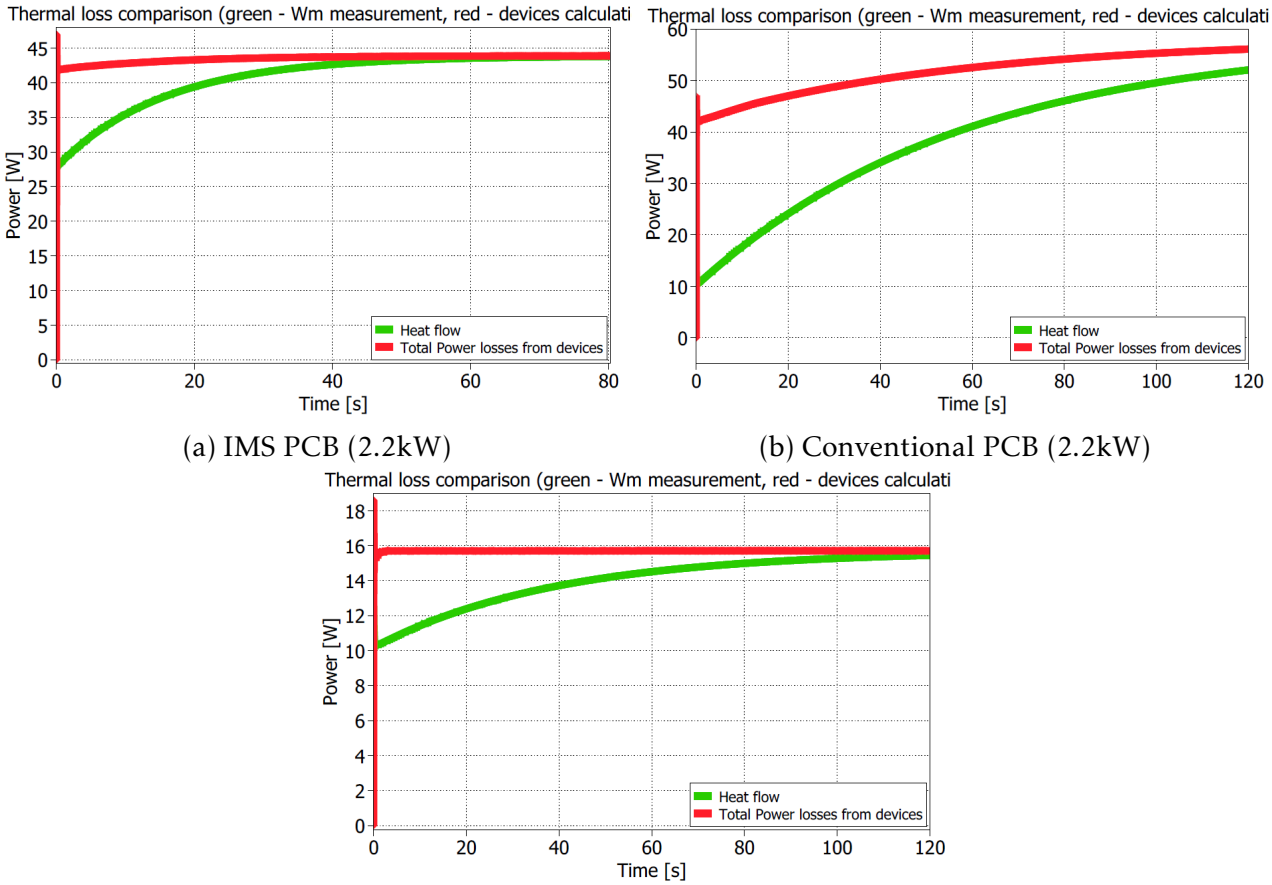
It can be seen in Figure 6.1.2 that the output voltage follows the reference voltage with a ripple value due to the charging and discharge of the capacitor and the voltage ripple is within the expected deviation of 20V as it is fluctuating between 382V to 398V. A 100Hz ripple is observed in the DC voltage which is due to the discharge and charge of the capacitor in each half cycle, and therefore see two times the line frequency, this comes from active rectification of the PFC from a single phase input. The current ripple of the input current was depending on the inductor design as described earlier. In Figure 6.1.2 a current ripple of 1.3A is observed, and at a peak current value of 15.3A, the current ripple was expected to be a maximum of 1.53A which means that the inductor design is sufficiently keeping the current ripple at maximum 10%. The AC current has a peak of ± 15.3A and the DC current is approximately 5.6A, which corresponds to an output power of 2.2kW.

From Figure 6.1.1 there is a blue area covering the switching devices, which corresponds to the case of the devices as a group. As an extension, the different layers of the PCB can be inserted via different thermal resistance values corresponding to the layers. The temperature of each layer can therefore be modeled, and the power dissipation is affecting the junction temperature of the devices. The first conclusions of the PFC converter on IMS with passive heatsink, can therefore be taken, showing it is possible to have a 2.2kW output within temperature limits of $150C°$ and $175C°$, respectively, using GaN switches and diodes in a totem pole configuration, for AC to DC conversion, with choke inductor and capacitor bank. It should be noted that for running at 2.2kW a low flow of air is needed to reduce the thermal resistance of the heatsink from 2.9°C/W to 2.2°C/W. The different temperatures are simulated at full load (2.2kW) for IMS PCB and conventional PCB, and also at 300W for the conventional PCB Table 6.1:

Simulation steady state temperature comparison			
Component	IMS PCB (2.2kW)	FR4 PCB (2.2kW)	FR4 PCB (300W)
High side GaN	145°C	450°C	148°C
Low side GaN	145°C	450°C	148°C
High side Diode	145°C	450°C	145°C
Low side Diode	145°C	450°C	145°C
Heatsink 2.2°C/W	120°C	150°C	58°C

Table 6.1: Component temperature for IMS PCB and FR4 PCB

In Table 6.1 it is clear that the temperatures are really close to each other for each PFC devices, and that the heatsink for IMS is close to the device temperatures as well, showing great thermal management. For the conventional PCB it is shown that at the same load, this PCB will burn the devices instantly because of the bad thermal resistance. Comparable to the IMS with the same heatsink and convection, the convetional PCB will only be able to run at a rated power of 300W, which is significantly lower than the IMS. Again, proving that the IMS has an outstanding thermal performance compared to conventional PCB. To highlight the thermal power dissipation of the different simulations, the heatflow has been measured at is compared to the total power losses of the PFC with different PCB type Figure 6.1.3:



(a) IMS PCB (2.2kW)

(b) Conventional PCB (2.2kW)

(c) Conventional PCB (300W)

Figure 6.1.3: Heat Flow and Device Power loss

In Figure 6.1.3a the heatflow measurement shows that that it is able to reach a sufficient heat dissipation level before the devices hit maximum temperature. For the temperature to be steady the total power losses and the heat flow thorugh the heatsink should be identical. In Figure 6.1.3b the heatflow is significantly slower to reach the total power loss, and this results in crossing the temperature limits of the devices really quickly. In Figure 6.1.3c the total power loss is significantly lower because of the low load operation. Here the conventional PCB is able to transfer the heat sufficiently before the devices reach maximum temperature rating. Overall it can be seen that the conventional PCB needs a 3 times lower total power loss from the switches to be able to operate within the limits compared to the IMS.

6.2 Simulation of Three Phase Inverter

As a load for the PFC converter a three-phase inverter was implemented to the IMS. The desired application is a single-phase grid-connected motor drive. Since the inverter is only for load purposes, simple configuration, devices, and control have been chosen. This includes open loop v/f control, for switching 6 IGBTs to drive the motor at a desired speed. The simulation model of the three-phase inverter can be seen in Figure 6.2.1:

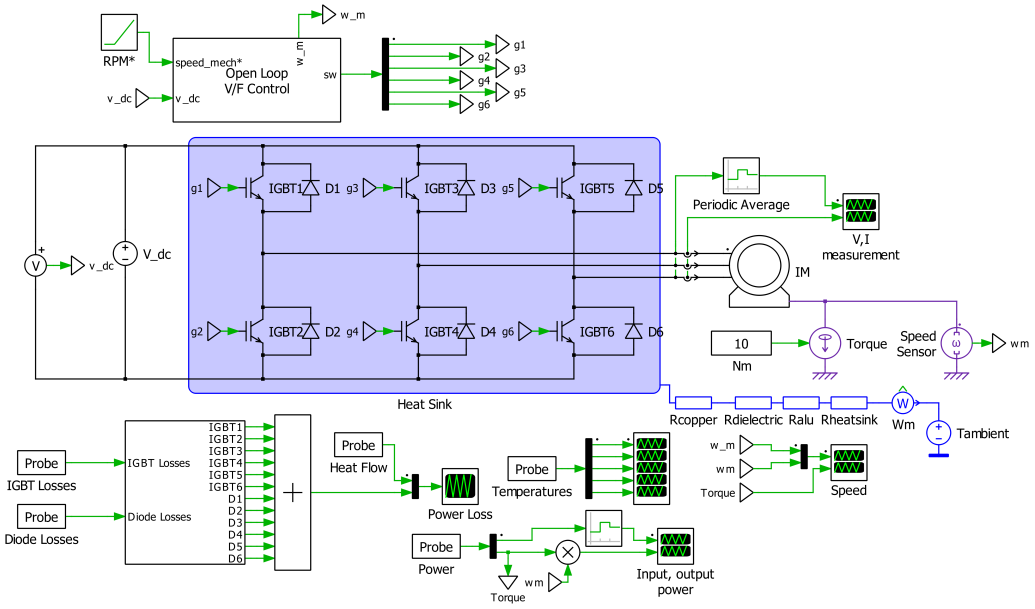


Figure 6.2.1: Simulation model of 3-phase inverter

In this simulation model, the DC source would correspond to the output of the PFC converter which is approximately in the 380V-400V range. Thermal description models of the IGBTs and their diodes have been implemented from a PLECS model which has been offered on the Infineon website. This model gives a good description of the loss and temperature values under operation at different loads. Together with that, an ABB induction motor[20] from the Danfoss test bench has been implemented as the motor load. During operation, the speed is ramped up slowly and the load therefore also increases linearly. During startup there is some instability which makes it even more important to do a slow startup, this can be seen in the following Figure 6.2.2:

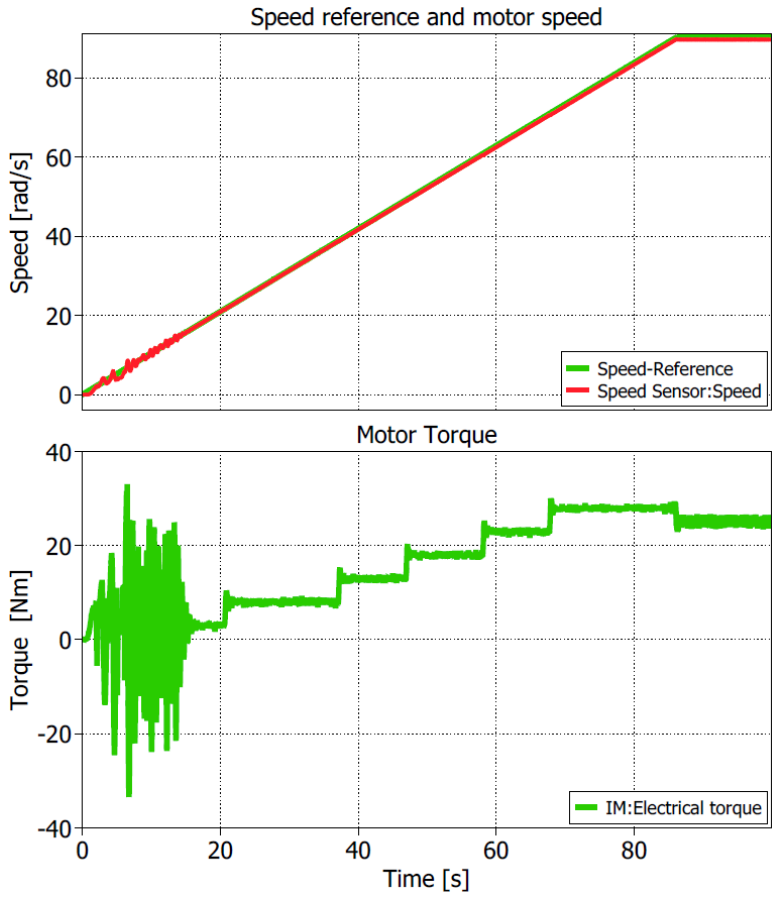


Figure 6.2.2: Induction motor speed ramp and electrical torque

In the first 15 seconds of the startup period, the speed of the induction motor is fluctuating around the reference. This also affects the motor torque during startup, which after 15 seconds reaches steady state at no load condition. After steady state has been reached load torque is applied gradually to increase the load of the motor and thereby apply extra stress to the inverter for testing the power losses of the IGBTs at maximum power. The continuous power is shown in the following Figure 6.2.3:

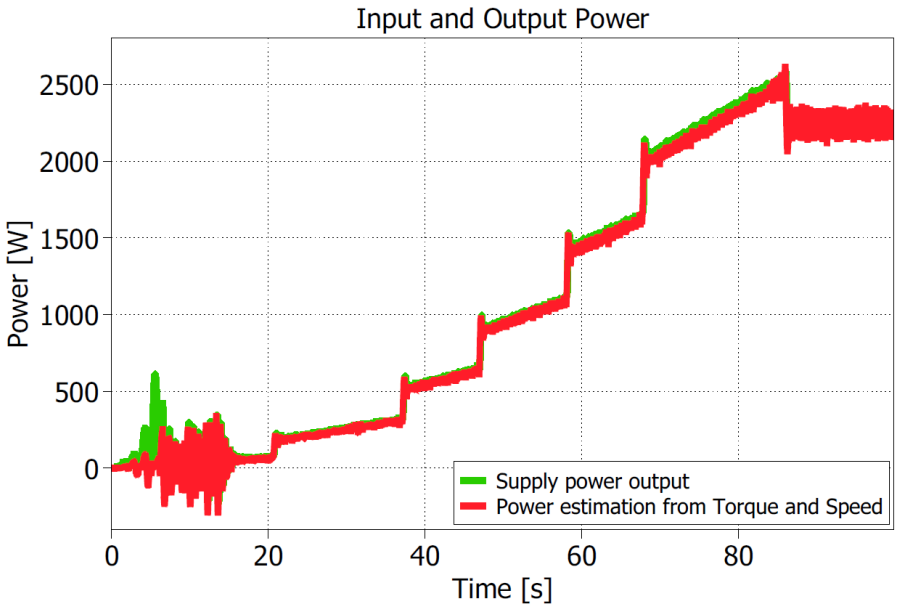


Figure 6.2.3: Source power and motor load

The power input and output of the inverter can be seen with a probe on the DC voltage source for the input and by multiplying the electrical torque with the speed for the output power. The torque is increased to 25Nm to reach between 2kW and 2.5kW. From the power curve, the disturbance is highlighted during the startup of the motor. The torque load increase is also clearly showing an increase in power together with the speed. The torque drops to a steady state condition when the desired speed is reached.

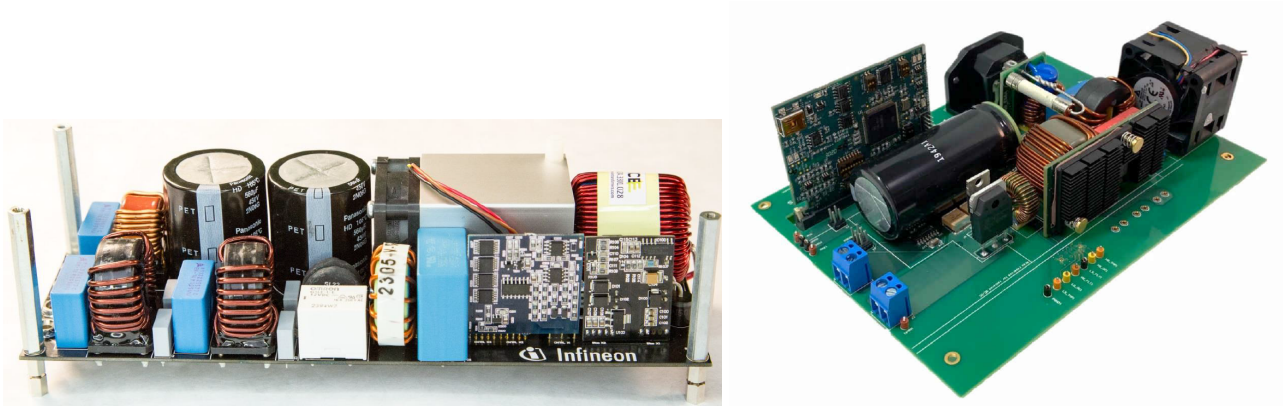
Chapter 7

PCB Design

In this chapter, the PCB Design processes will be described. It will include the different strategies and considerations taken to create the optimal PCB Design for this project. The software program for creating schematics and PCB is KiCad, an open-source Computer-aided Design (CAD) software for developing a PCB design with all features needed. In this project, the PFC motor drive is a prototype, and it is therefore not required to follow the Institute of Printed Circuits (IPC) standards, but the standards will be taken into thought throughout the design process.

7.1 Design guides and Schematic editor

In Chapter 4 the topology, semiconductor, and PCB layout has been investigated and chosen for the optimal design. The starting point of designing the PFC converter was investigating existing PFC converter boards from known manufacturers. Several manufacturers have developed evaluation boards of PFC converters with different specifications, this was used as a reference for the development of the PFC converter in this project. This was mainly used for the schematics and placement of the components of the PCB and to identify the manufacturers' experiences in developing a BTPPFC converters. The reference papers are for PFC converters in Continuous Conduction Mode (CCM) running up to 2.5kW[21] and 3kW[22] maximum power.



(a) 2.5kW PFC Evaluation Board (b) 3kW PFC Evaluation Board

Figure 7.1.1: Design guide evaluation boards

From the design guides of the PFC converters Figure 7.1.1a and Figure 7.1.1b the schematics could be drawn. KiCad has two different editors when developing a PCB, this consists of a Schematic editor and a PCB editor [23]. Where the schematic editor is creating the electrical diagram with component symbols as shown in the example of the power IMS PCB Figure 7.1.2:

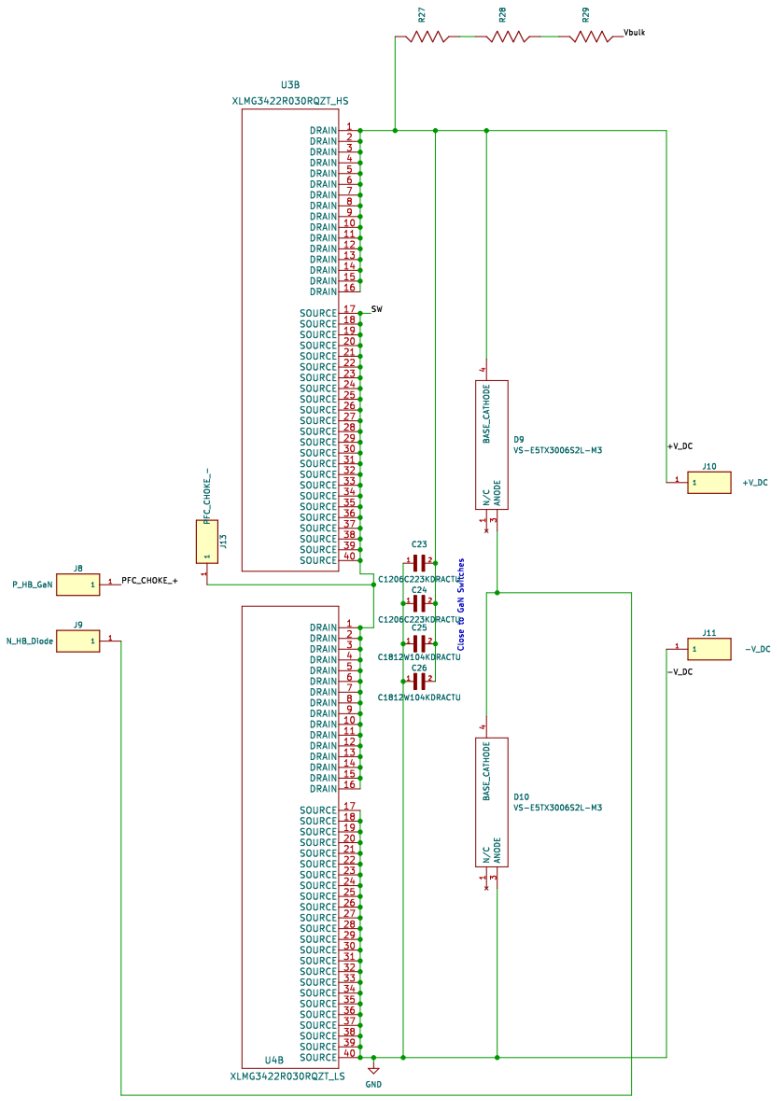


Figure 7.1.2: GaN switch cut of Power IMS schematic

In this editor, all the electrical connections are made identical to the connections eventually printed on the PCB. The schematics can create all the footprints in the PCB editor which ensure that all inserted components in the schematics also exist in the PCB editor. This gives an idea of the dimensions of the PCB layout.

In this project, the important part of the PCB is the Power circuit consisting of the PFC choke, GaN switches, diodes for the PFC converter, and IGBT switches for the three-phase inverter as mentioned in Chapter 4. Since these are the devices dissipating power from the losses they will heat up and need good thermal management, which potentially can be done through the IMS. The other parts of the converter, which is as essential, but have neglectable losses and heat dissipation, can be built on conventional PCBs. Therefore the whole setup has been split into 3 different editors.

- Power IMS - PFC stage and 3-phase inverter
- Supply PCB - Single phase AC input, EMI filtering and control connections
- DC-Link PCB - DC-Link capacitors

Since the Supply and DC-Link PCBs are conventional and simple PCBs with through-hole technology and FR4-material, these are produced with the default build by the manufac-

turer and do not include a lot of design considerations. Therefore the main focus of the PCB design will be on the Power IMS.

7.2 Design Rules and standards

When developing a PCB there are some specific rules and standards to follow to ensure high performance and reliability. In the PCB standards, this comes as a classification of three different levels, Class 1, Class 2, and Class 3. Where class 1 is for General electronic products which have simple functions and a limited lifetime, and are therefore not used since the performance and reliability are reduced[24]. Class 2 is for dedicated service electronic products which support continuous operation, but it is not critical, it has higher reliability and extended life, follows more stringent standards, but still allows some cosmetic imperfections[24]. Class 3 is for high-performance electronic products which can provide uninterrupted service in harsh environments, it consists of high levels of inspection and testing following stringent standards, which makes them highly reliable[24]. From these classifications, the power IMS is produced with class 2, as class 1 often is upgraded by the manufacturer even though the PCB only needs classification 1. Class 3 is always optimal, but comes with additional complexity and cost. Since this project is developing a prototype, the standards and design rules are not crucial. But the quality classification has to be set when ordering and is, therefore, necessary to acknowledge. The KiCad software has a board setup to ensure the most important requirements to follow:

- Board Stackup
  - Board Editor Layers
  - Physical Stackup
  - Board Finish
  - Solder Mask/Paste
- Design Rules
  - Constraints
  - Pre-defined Sizes
  - Net classes
  - Violation Severity

The board editor layers are mainly layer types for overview purposes in the software. It allows the user to see footprint sizes, paste areas, text and numbering, copper layers etc. It is a tool to name the different layers and operate at different layers without seeing them all at the same time. The physical stackup is where the number of layers is identified, this applies to both copper and dielectric layers. Here it is possible to set the minimum thickness of the copper which in the IPC-6012 Class 2 standards is 20μm, during the PCB order the copper thickness is set, and the thicker the layer the better-conducting capability, and since it is copper the thermal resistance will remain low when increasing the thickness as seen in the equations Section 4.3.2. In the Power IMS the copper thickness corresponds to 1 oz/m^2 which is 35μm

The dielectric layer is also set during production order, but during the PCB design the dielectric layer should be carefully chosen since dielectric as prepreq and FR4 as shown in

Chapter 4 has a poor thermal conductivity. A goal is therefore to minimize the thickness while ensuring a sufficient breakdown voltage and insulation. In the standards the minimum thickness of the dielectric layer should be 90μm.

The board finish is for castellated pads or plated board edges, mainly if the board should be able to fit in an edge card connecter.

The Solder Mask/Paste is to ensure a minimum clearance between the solder mask and the PCB surface. The purpose of this clearance is to provide adequate spacing known as solder dams between surface features that receive solder. Typically the with should be half the width of the conductor spacing, usually the minimum clearance is 50μm but can go below[25].

In the design rules of KiCad, it is possible to set constraints, this ensures that all the prespecified requirements have been complied with. When finishing the PCB design a design rules checker will give errors and warnings in places where the constraints are exceeded. The design rule constraints in KiCad are:

- Minimum track clearance
- Minimum track width
- Minimum annular width
- Minimum via diameter
- Copper to hole clearance
- Hole to Hole clearance
- Copper to edge clearance

The minimum clearance ensures a sufficient distance between two traces, to avoid arcing between them. The clearance changes with the voltage levels and specifications of the circuit, and the standards for clearance of uncoated external conductors state 1.25mm for 300V, 2.5mm for 500V, and 5mm for 1000V[26]. On the Power IMS, the 400V tracks are therefore with a clearance of 2.5mm to ensure a margin for taking overvoltages into account. In the PCB design the clearance of the input line and the output phases was given a high clearance, since this is the point of highest voltage difference.

The minimum track width ensures sufficient current conducting capabilities, the wider the track the higher the current rating. This is especially important in the power circuit where the tracks have been made as wide as possible through smoothed polygons. From the IPC standards for 1 oz copper is 2.79mm to 7.62mm from 5A to 10A, respectively[27]. This means that the minimum width of the input line is 7.62mm and at output line minimum width of 2.79mm.

The annular ring is surrounding the hole/via which has been drilled to connect different layers. The ring will ensure a good conductive surface and therefore has to have a minimum size to be sufficient. The tradeoffs in a good conducting annular ring is that it takes up space, where the design normal is trying to be compact. Since this is a prototype compactness is not essential and the annular rings, therefore, has a size of 0.3mm, where the design standards state a minimum width of 0.1mm for inner layers land 0.05mm for outer layers[28].

The vias used on the Power IMS must be blind/buried because of the metal core baseplate. The blind vias is a drilled hole that connects an outer layer with an inner layer and does not go all the way through. Buried vias is connecting one or more inner layers. Standard via sizes are the commonly used sizes which are 0.6mm, but can be 0.2mm and 0.3mm, the restrictions on these sizes mainly come from the manufacturers' capabilities and cost, but most fabricators can create vias down to 0.15mm[29]. On the Power IMS PCB thermal vias, which is filled vias, has been placed underneath the GaN devices to increase the thermal conductivity of the stack. This means that it is possible to use the vias both electrically and thermally. The thermal vias are removing the dielectric layer between the semiconductors and the aluminium plate, which has been proved to be the critical layer for improving the thermal resistance.

The copper to hole and hole to hole clearance is similar to the minimum clearance to avoid arcs between traces, but also from a construction perspective, the holes should have a specific distance between them. In the Power IMS PCB design the minimum clearance between the holes and copper traces is 0.25mm.

The copper to edge clearance is also a structural constraint that avoids holes or traces being on the edges of the PCB. For IMS PCBs it is not possible to plate copper on the edge, as a certain clearance between the aluminium base plate and the copper would be needed. This is highlighting a difference between FR4 PCBs and IMS PCBs.

The pre-defined sizes are for customizing specific track widths, Via size, and holes or other constraints that deviates from the standard constraints set by the user. The Net Classes is a function for customizing different Nets which are the different power, ground, or control connections that can have defined constraints. The violation severity is to control the severity of exceeded limits when using the Design Rules Checker, it ensures that the PCB design is held within the users own specified constraints and requirements. All these standards and design rules are to ensure high performance and reliability of the desired PCB, this is especially important to comply with in high quality production companies and less in the prototyping stages.

Chapter 8

PFC motor drive design

In this chapter, the design of the PFC motor drive will be described. This includes physical construction and placement considerations, and connection terminals. The following sections will be taking all previously mentioned research Chapter 4, parameter identificationChapter 6, design guides Section 7.1, and design rules and standards Section 7.2 into account, and use that information to create the optimal prototype for testing IMS and WBG devices in the PFC motor drive.

8.1 Designing PFC converter

For switching and monitoring the datasheet comes with a recommended circuit for choosing the slew rate, isolating the PWM input, and monitoring overcurrent, temperature, and faults. The design guide references have been used to create the setup with a constant slew rate of 150V/ns by shorting RDRV pin to ground, since this rate is not prioritized to optimize in this project the slew rate will remain constant and not be varied. The two isolators is ensuring an isolated connection between GaN and control signals. These connections can be seen in Figure 8.1.1:

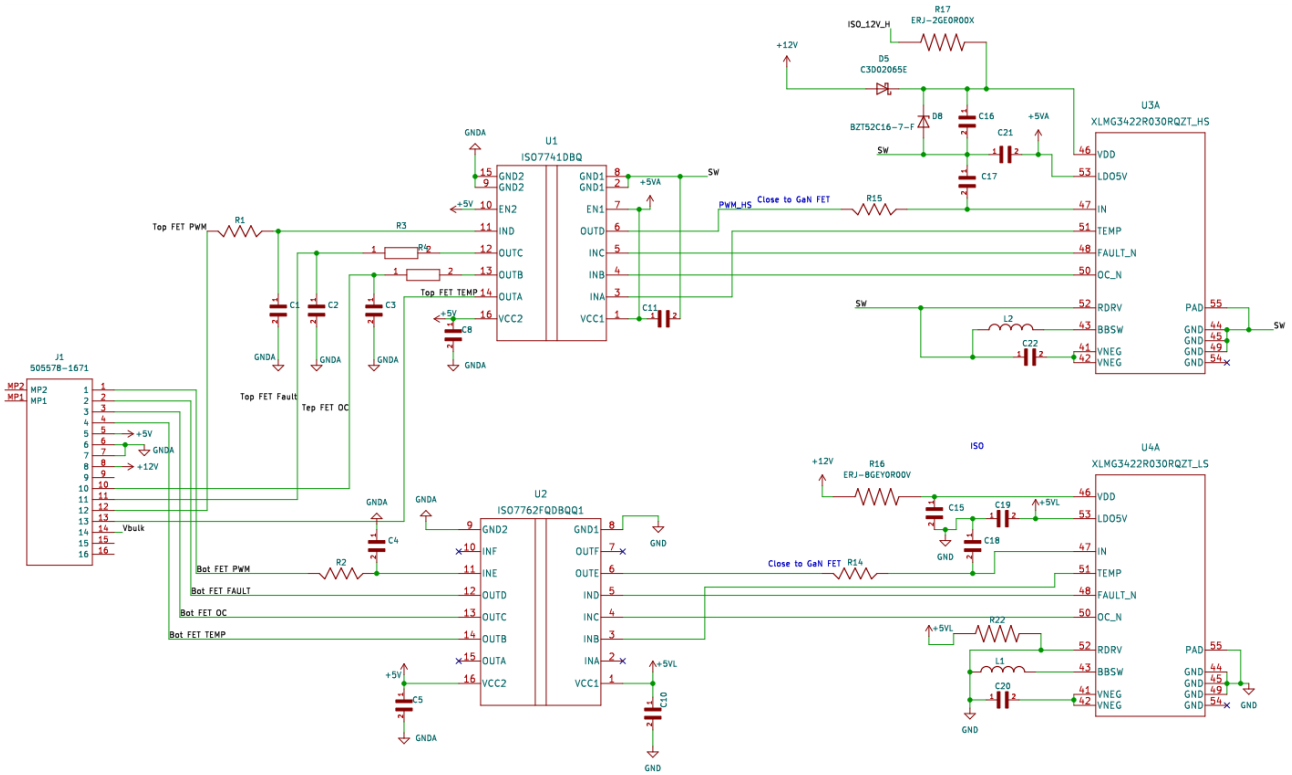


Figure 8.1.1: Communication schematic of GaN

All the information from the GaN switches and the DC Voltage is connected to a pin terminal for communication with the microcontroller. This ensures the safe operation of the PFC

together with low-interference PWM inputs. The GaN switches are supplied by 12V and isolated 12V for lower and upper switches, respectively. This input is connected to the VDD pin. The GaN switches are also ensuring a 5V supply to the digital isolators with a linear regulator at the LDO5V pin. The GaN sensors and protections are on the TEMP, FAULT_N and OC_N pins. There is a buck-boost converter internally in the GaN switches that are ensuring negative voltage to turn off the switch. This requires a power inductor connected to the BBSW pin and output capacitor connected to the VNEG pin. All of this circuitry is designed using the datasheet of the GaN switches[13] to configure it as recommended.

8.2 Designing Three Phase Inverter

For loading the PFC converter under test a Three Phase inverter is built. The goal is to make a simple design that can carry the DC voltage of the PFC converter output and drive an induction motor. The power electronics manufacturer Infineon Technologies AG has made an evaluation board for a 3-phase motor drive with gate drive IC for switching 6 IGBTs[30]. Therefore only one gate driver IC circuit had to be implemented and the IGBT specifications should just contain the needed requirements to ensure sufficient loading when testing the thermal capabilities of the IMS. Therefore 600V, 8A, IGBTs have a rated current able to load the IMS for thermal heat management tests. The schematic of the inverter design is in the following Figure 8.2.1:

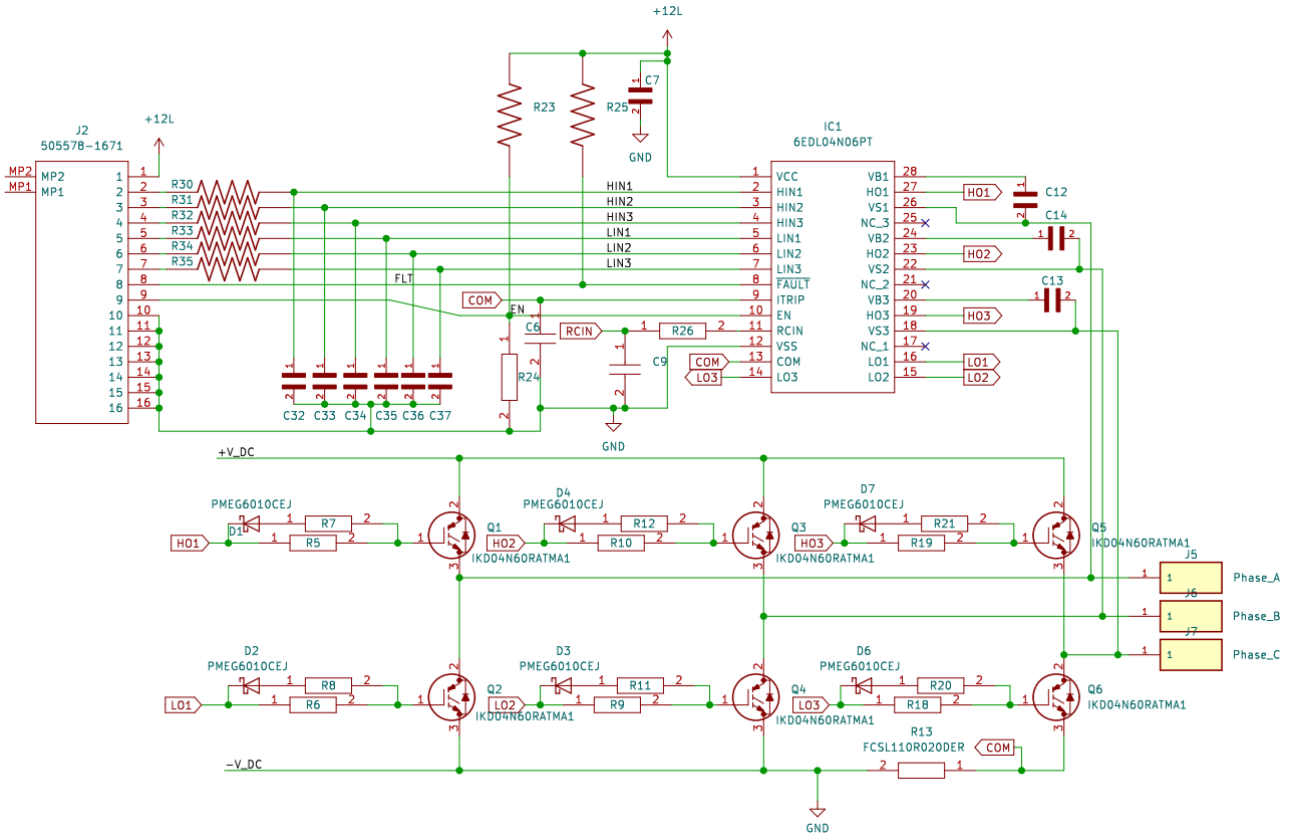


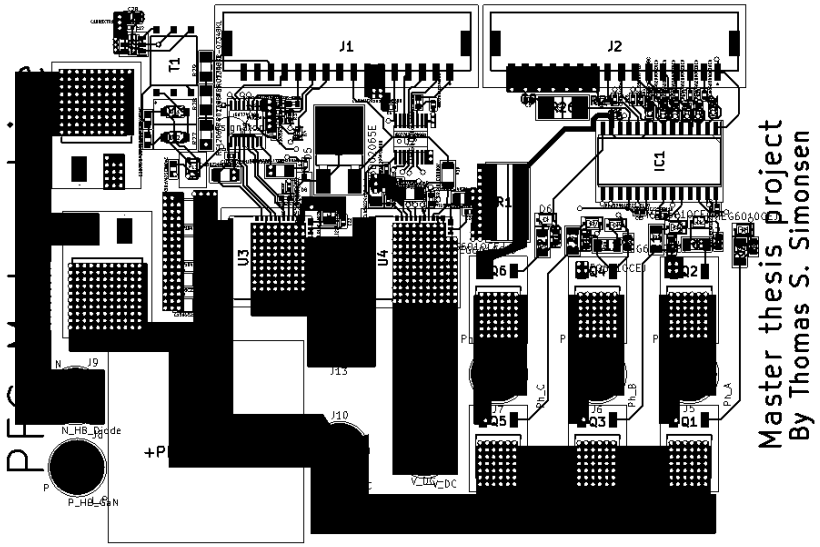
Figure 8.2.1: Schematic of inverter

The main function of the gate driver[31] is to switch the IGBTs, which is done from the PWM inputs (HIN1,2,3 and LIN1,2,3) created by the microcontroller and PWM outputs of the gate driver ensuring a sufficient voltage to switch the IGBTs. In addition, the gate driver IC also has some protection systems to avoid over-current, and under-voltage shown by a

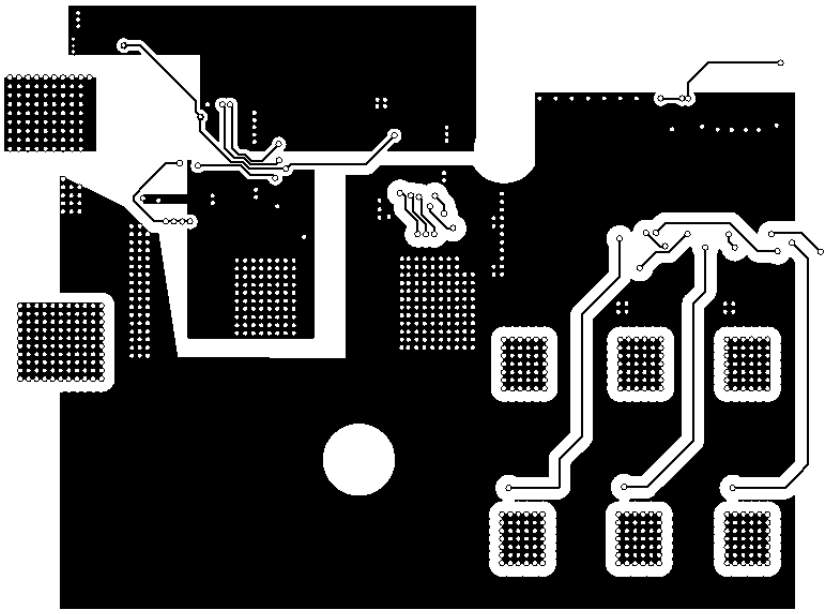
fault output. The ITRIP input is connected to the load feedback current, which is coming from the shunt resistor R13 in the bottom of the schematic. If the ITRIP comparator is triggered by the exceedance of a threshold voltage of typically 0.44V, there will be a hard shutdown of all gate driver outputs. The RCIN input then goes low as the RC network capacitor is discharged and will after a recharge of 5.2V resets the over-current detection. The under-voltage lockout status is visible from the fault pin which shuts down the PWM outputs if the supply voltage drops under 9.8V, this prevents external power switches from low gate voltage levels during on state and therefore also excessive power dissipation from the switches. Lastly, the COM coneection is the low side gate driver reference.

8.3 Compact design of PFC motor drive

As mentioned in Chapter 7 the design was developed in KiCad. The goal was to create a compact design while still meeting the requirements of the basic standards of PCB design. The inductor and capacitors are size-wise the largest components of the PFC converter, but the placement and structure of the components and wiring will be crucial for the size of the PFC motor drive. The challenge is to create sufficient wiring as short as possible to reduce the inductive effect, avoid power loops, and couple traces with a turn and return path to avoid the capacitive effect. The PCB layout in KiCad of the PFC motor drive can be seen in the following Figure 8.3.1:



(a) Front layer drill file



(b) Bottom layer drill file

Figure 8.3.1: PCB layout of PFC motor drive

Figure 8.3.1a is the front layer of the PCB, and the bottom layer is shown in Figure 8.3.1b as the ground layer and signal routing. The thermal vias are inserted to improve the thermal dissipation to the aluminium base layer since this removes one of the dielectric layers. The vias are placed on the thermal pad of the switching devices as these are the loss contributors.

The design was supposed to fit the PFC choke on the PCB as well using a contact pad or thermal adhesive to create a good thermal connection to the IMS. But the available cores for the inductor were bigger than expected, and are therefore not placed on the PCB but on the heatsink of the motor drive. Using a smaller ETD core would make it possible to fit the inductor on the PCB. An overview of the PFC Motor drive can be seen in the following Figure 8.3.2:

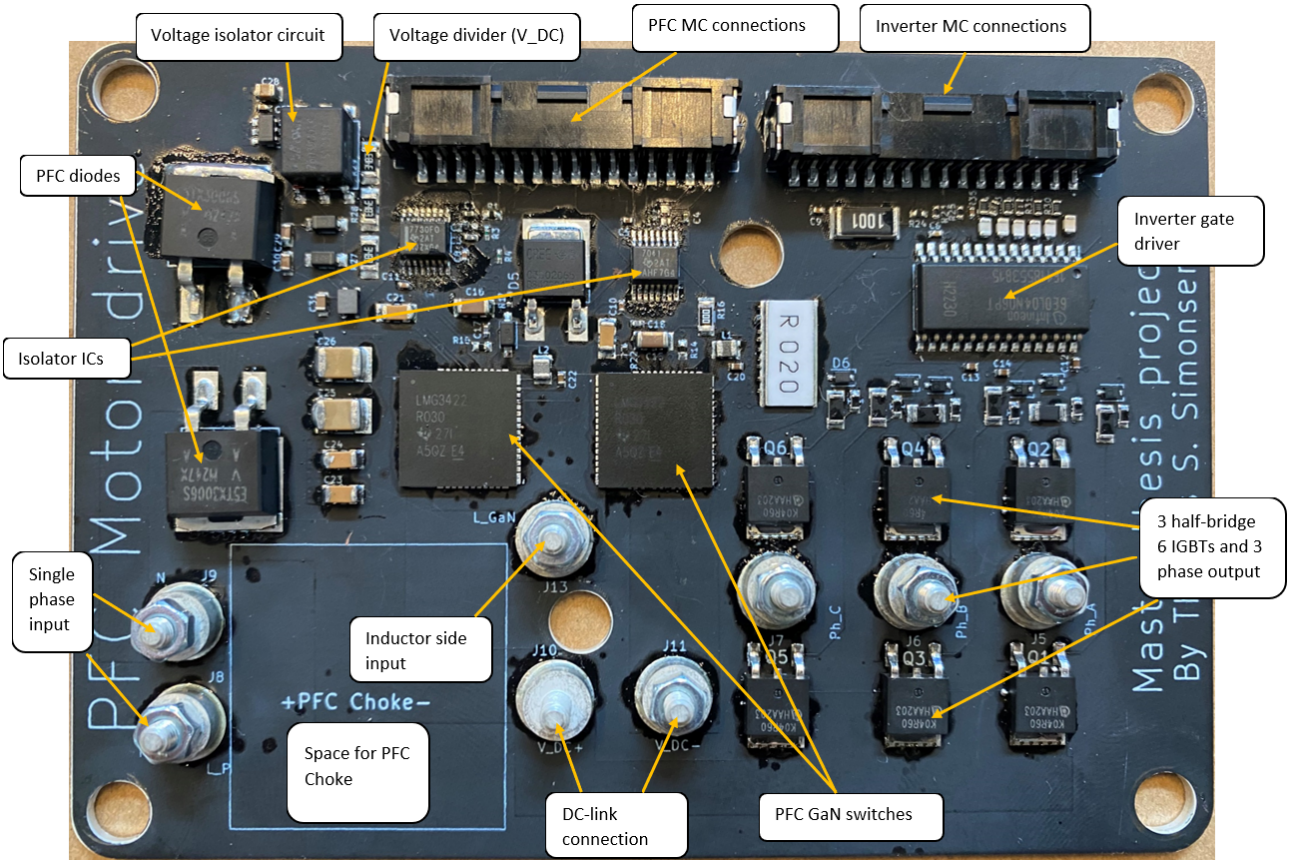


Figure 8.3.2: PFC motor drive overview

8.4 Designing Supply board with microcontroller connections

The PFC motor drive PCB is supplied by a single-phase input from the grid, an EMI filter is, therefore, necessary to ensure a clean input of the PFC converter. With the EMI filter, the supply PCB is also the connecting part between the motor drive and the microcontroller ensuring that the correct measurements are made regarding AC voltage, AC input current, and DC voltage. A hall sensor is placed on the supply board for AC input current measurement, with a voltage divider for the positive and negative sides of the AC input and a voltage divider for the DC voltage. A fuse was also placed to ensure shutdown at overcurrent levels. The following supply board schematic is shown in Figure 8.4.1:

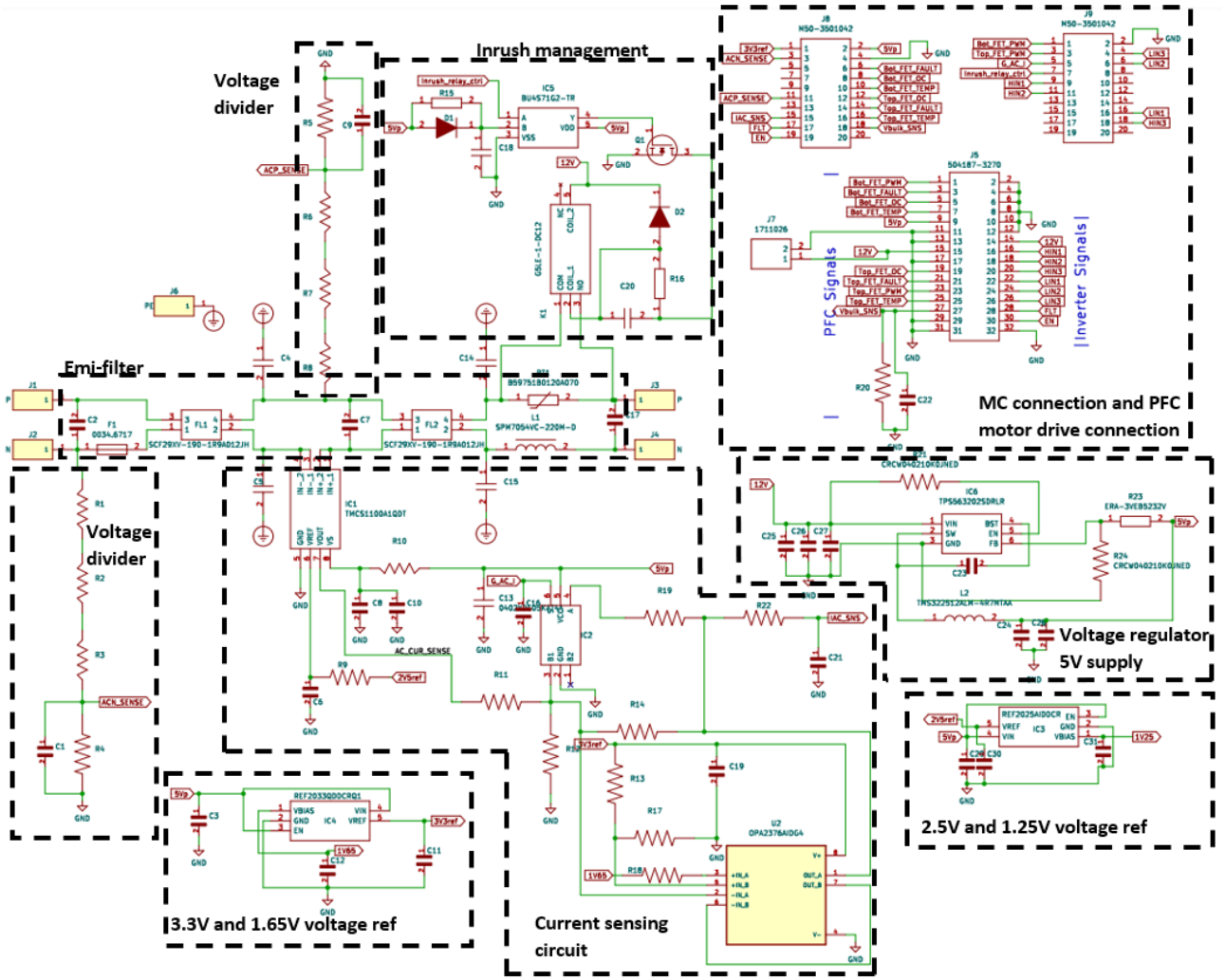


Figure 8.4.1: Supply board schematic

The supply PCB could have been implemented on the IMS as well, but since there isn't any large power dissipation from any of the filter components, voltage regulators, or sensing systems, it was prioritized to have only the switching circuit on IMS and therefore designing the supply PCB on a conventional PCB type, this also reduced the cost of the overall system together with reducing the complexity of creating the PCB motor drive. The three PCBs are connected with surface-mounted terminals compliant with cable shoes. An overview of the physical supply board is shown in Figure 8.4.2:

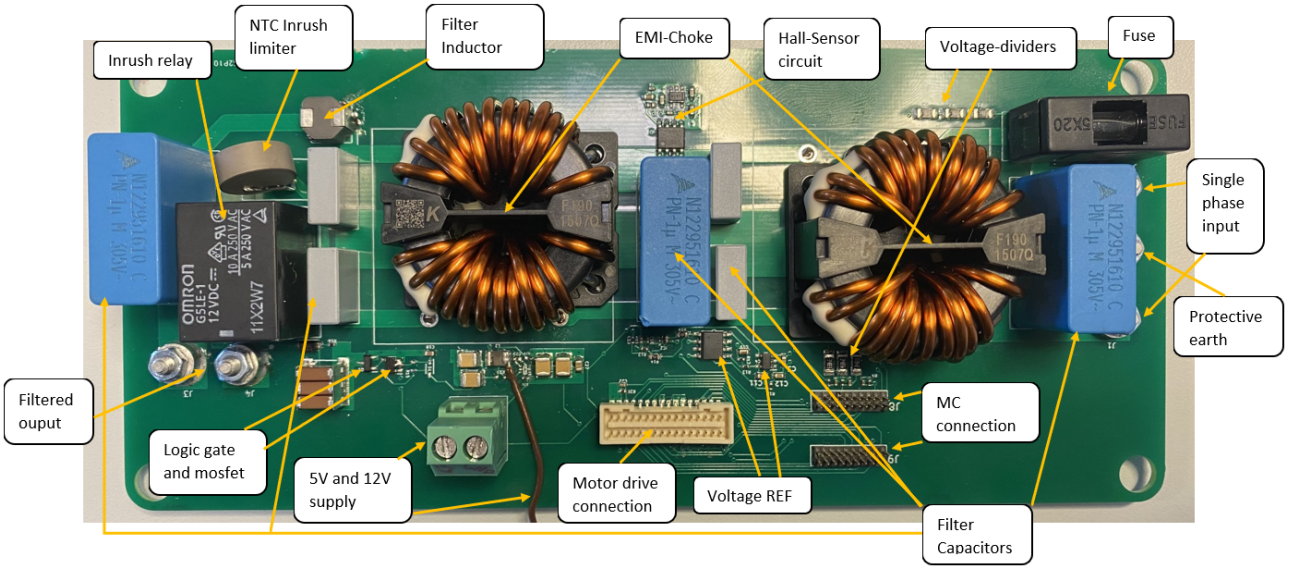


Figure 8.4.2: Supply board overview

From this board the PFC motor drive could be supplied with the required input, attach the desired microcontroller connections, and gather the needed feedback for the control system.

8.5 PFC and Inverter control with autogenerated code

For testing the PFC motor drive, a control code had to be developed. Since this is only for testing the PFC converter and the motor drive inverter, the control is implemented from the TSP in PLECS as an auto-generated code. The TSP is an extension to the PLECS library where digital blocks from a Texas Instrument C2000 microcontroller can be inserted to generate PWM signals, attribute correct PIN numbers and configure the GPIOs and ADCs needed for the control feedback.

8.5.1 PFC control

As the control is not the key focus of this project, inspiration of the control structure is taken from the totem-pole PFC demo model in the PLECS model library, as mentioned in Chapter 6. Using the PLECS model was acceptable since stable operation was obtained in the simulation model. The control block with the TSP is shown in Figure 8.5.1:

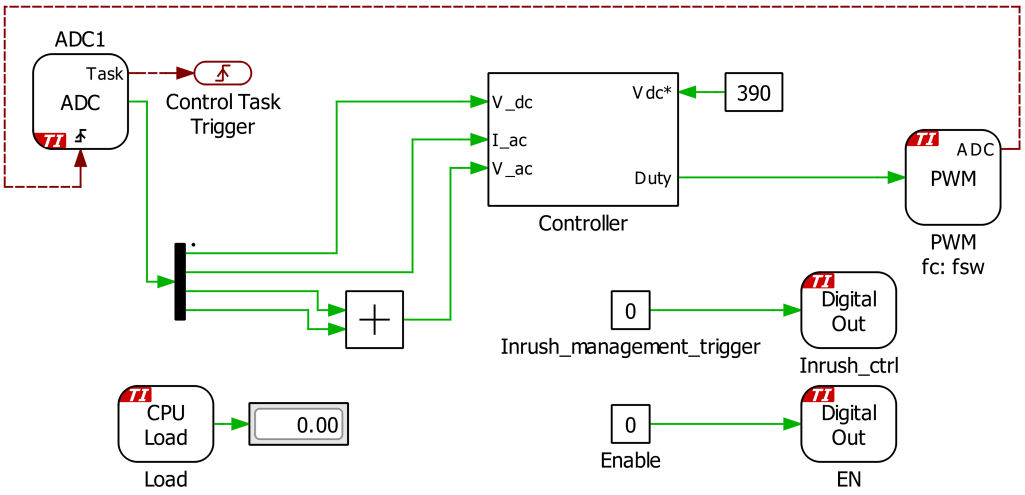


Figure 8.5.1: PFC converter control block using TSP

The ADC block is ensuring to configure the correct ADC channels, scaling the input, and creating an offset. In PLECS all the feedback represented is scaled to ensure correct measurements on the physical setup, the voltage divider is therefore scaled as follows, where a capacitor is inserted to create a low pass filter effect:

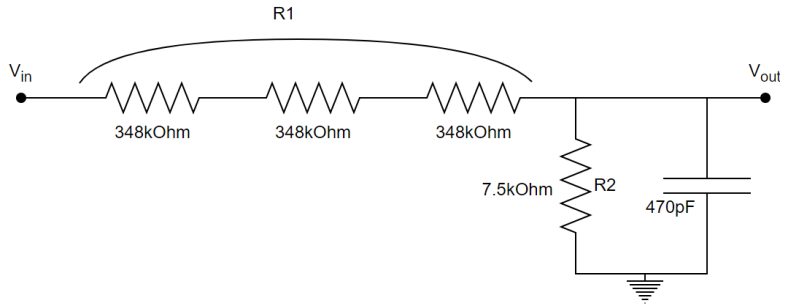


Figure 8.5.2: Voltage didiver circuit

This circuit is used for all three voltage measurements, V_{ACP}, V_{ACN}, and V_{DC}. The divider output is calculated as Equation (8.1):

$$V_{out} = V_{in} * \frac{R_2}{R_1 + R_2} \tag{8.1}$$

Where in this example the input voltage is the peak voltages of the measurements.

$$V_{DC_{meas}} = 390V * \frac{7.5k\Omega}{1044k\Omega + 7.5k\Omega} => 2.781V \tag{8.2}$$

$$V_{ACP_{meas}} = 230V * \frac{7.5k\Omega}{1044k\Omega + 7.5k\Omega} => 1.640V \tag{8.3}$$

$$V_{ACN_{meas}} = 230V * \frac{7.5k\Omega}{1044k\Omega + 7.5k\Omega} => 1.640V \tag{8.4}$$

$$\tag{8.5}$$

Here it should be noted that the DC voltage measurement only needs a reference between 0 and 2.781V to measure the whole range of the DC-voltage, whereas both phase and neutral on the AC input should be able to reach a negative value as well, therefore an offset of 3.3/2 will be scaled to these two values, so the full range will be in between 0V-3.3V which is the maximum input range of the microcontroller.

For the current measurement, a hall sensor has been used. This current is also fluctuating between 0 and should therefore also have en offset of 3.3/2. As a part of the hall sensor circuit a reference is supplying the voltage reference of the hall sensor with 1.645V for offset as the zero current output voltage. The following Equation (8.6) is therefore used to calculate the current measured by the hall sensor in this example 10A:

$$V_{out} = S * I_{in} + V_{REF} \tag{8.6}$$

Where S is the sensitivity of the hall sensor and can vary depending on the choice of IC. For this converter a sensitivity of 40mV/A is used.

$$V_{I_{AC_{meas}}} = 0.4mV/A * 10A + 1.645V => 2.045V \tag{8.7}$$

The maximum measured current is therefore ±41A as this will be the maximum range of the microcontroller 3.3V as mentioned for the voltage divider. Now all feedback is configured to implement in the TSP blocks of PLECS.

The control block used for the PFC converter is a simple closed-loop controller with a voltage and current loop. Where the voltage loop uses a PI controller and the current loop uses a proportional resonant controller for following the grid frequency on the input. The PLECS control block is as shown in Figure 8.5.3:

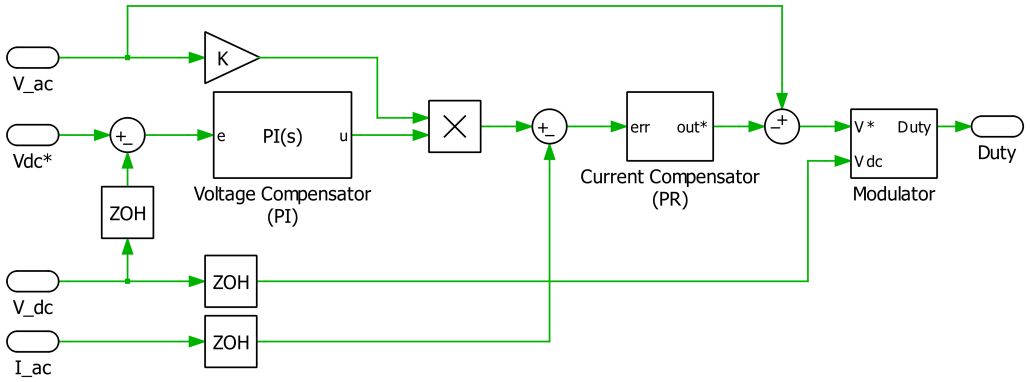


Figure 8.5.3: BTPPFC control block from PLECS[19]

8.5.2 Inverter control

For the 3-phase inverter control open loop was used to give a reference speed of the motor, which also can be seen as a specific peak value of the voltage of the three-phase output. The same blocks from the TSP are used, but only one feedback is needed, which is the DC-link voltage measurement. The DC-link voltage feedback is needed due to the voltage ripple of 20V, if this is not compensated for, this will be carried out on the motor terminals, causing a low frequency power ripple and thereby a 100Hz torque ripple, which is not desireable. The control block is a shown in Figure 8.5.4:

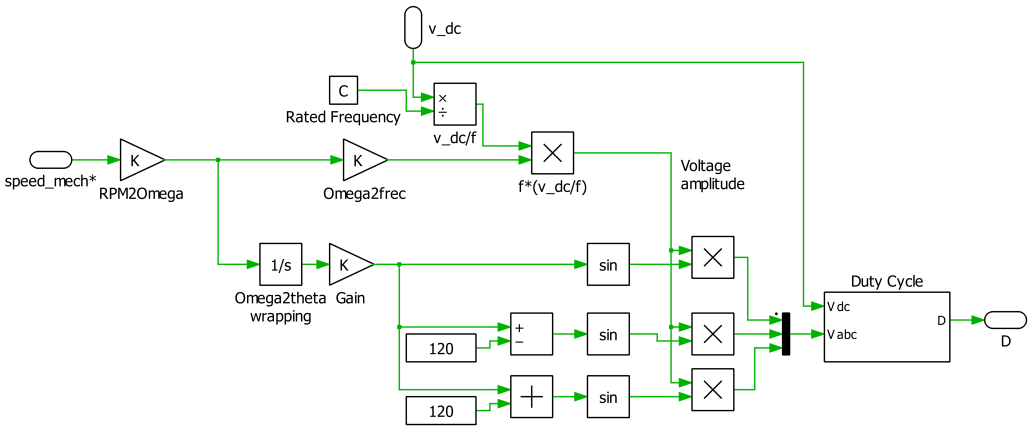


Figure 8.5.4: Open loop inverter control

This control block is sending out a duty cycle corresponding to the desired speed of the motor, and as shown in the simulation Chapter 6, this is sufficient enough to load the inverter and therefore contribute to heat dissipation from the IGBT power loss.

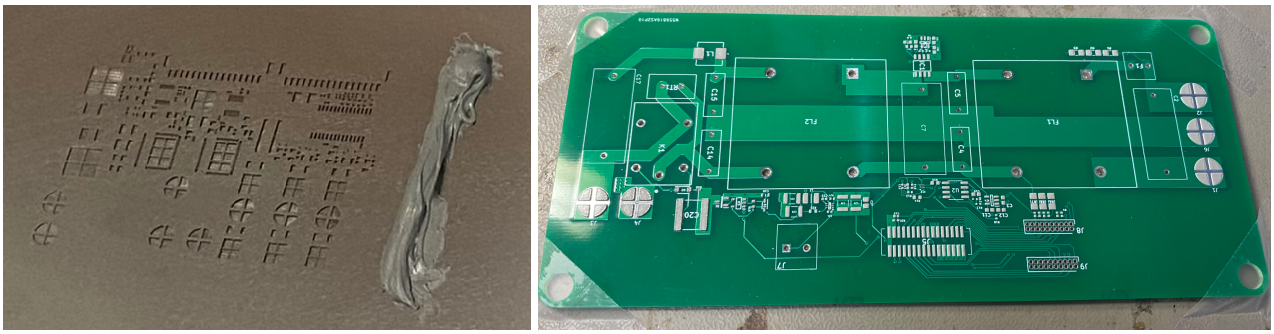
Chapter 9

Implementation of Supply board, PFC motor drive and feedback calibration

In this chapter, the processes of building the motor drive are described. This contains the considerations made in transitioning from CAD schematics and PCB design drawings to the physical connection and soldering of the complete PFC motor drive. The test stages needed to ensure sufficient operation, and the issues faced which needed correction.

9.1 Supply board implementation

The supply board is to ensure smooth input to the PFC converter but also to have inrush management and input measurements such as AC voltage and current. There are different ICs implemented to make everything run smoothly, such as voltage references, voltage regulators, logic gates, and a hall sensor which can be seen in Figure 8.4.1 the previous Chapter 8. For keeping a compact design SMD components were used for most of the circuitry around the ICs and therefore needed to be soldered with a soldering machine using solder paste. The process of applying the solder paste is shown in Figure 9.1.1a and Figure 9.1.1b:



(a) Stencil with solder paste (b) Paste applied on supply board

Figure 9.1.1: Applying solder paste

When the paste has been properly placed using the stencil and a spatula to spread it on the board, and the solder paste has been checked after the removal of the stencil, the components can be placed. Good practice using solder paste is to place the components within 30 minutes so the paste does not evaporate too much. The components were placed and soldered in the oven as seen in Figure 9.1.2:

Figure 9.1.2: Soldering machine used for the soldering process

When the soldering process was done, the last through-hole components could be soldered and the supply board was ready to run initial tests. Here it was important to check if the correct voltages were seen from the voltage regulator when applying 12V, and if the 5V and reference voltages were within the correct values, to operate the different systems.

Hall sensor test

The Hall sensor initial test was to check the current measurement circuit as mentioned in Section 8.5.1 the hall sensor had a sensitivity level and an offset, to create a range between 0 and 3.3V. To wires across the IC were connected as a short circuit and current was injected to take the measurements, the corresponding voltage generated by the halls sensor is then calibrated in the control code as previously mentioned Section 8.5.1. The current test and measurements is shown in the following Figure 9.1.3 and Table 9.1:

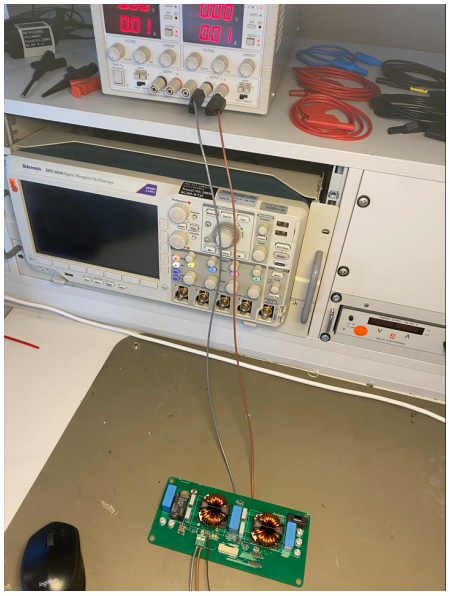


Figure 9.1.3: Current test

Hall sensor - Test measurements	
Current [A]	Voltage reference [V]
0	1.645
1	1.605
2	1.565
3	1.525
4	1.485
5	1.445
6	1.405
7	1.365
8	1.325
9	1.285
10	1.245

Table 9.1: Voltage feedback to MCU

The zero current voltage is at the 3.3/2 offset to ensure current measurements in the negative and positive cycle. The whole cycle will therefore be between 0-3.3V which corresponds to -40A to 40A and since the PFC converter has a maximum current limit at 10 Ampere due to the inductor this current range is more than sufficient.

Inrush Management test

The Inrush Management initial test was the operation of the inrush management. This is inserted to ensure proper charge of the DC-Link before operating the PFC converter. The test of the inrush management was done be measuring the resistance between the input and output of the EMI filter. The NTC thermistors inserted on the board was providing a limited current inrush with the 52Ω resistance, and therefore the measurements showed 52Ω when turned on, and around 1Ω when it was turned off. This was done manually from the control external mode in PLECS.

AC voltage test

The AC voltage initial test was to ensure correct voltage feedback of the AC input. These measurements are done for the negative AC side and the positive AC side if zero crossing detection should have been taken into use. Therefore, two voltage dividers were implemented to ensure desired AC voltage feedback. The test setup and measurements is shown in the following Figure 9.1.4 and Table 9.2:

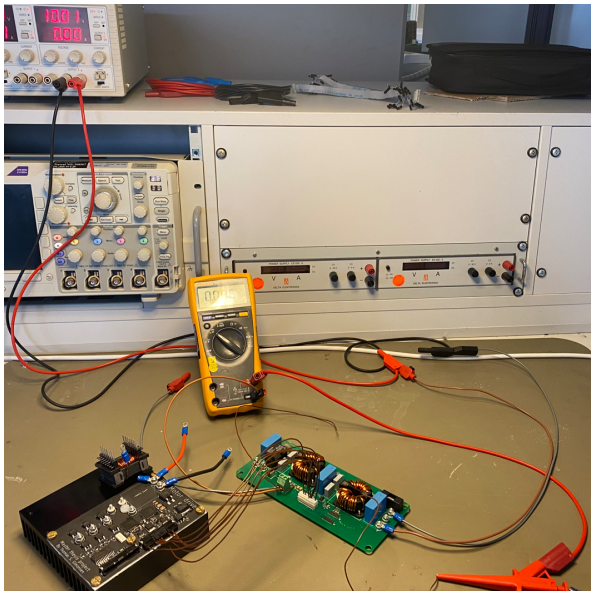


Figure 9.1.4: AC-voltage test

V_{AC} voltage divider - Test measurements		
DC-Voltage [V]		Voltage reference [V]
V_{AC_P}	V_{AC_N}	
5	-5	0.018
10	-10	0.036
15	-15	0.053
20	-20	0.072
25	-25	0.089
30	-30	0.107
35	-35	0.124
40	-40	0.143
45	-45	0.160
50	-50	0.178
55	-55	0.196
60	-60	0.214

Table 9.2: Voltage feedback to MCU

From this test, it is shown that the negative and positive voltage feedback are identical even though the voltage levels are of different polarity, therefore the calibration of the voltage feedback is to invert the negative voltage measurement without an offset, and the positive voltage feedback is offset by 3.3/2. It is also clear that the sensitivity of the voltage measurements is 3.6mV/V, making the measurement range between -450V to 450V.

9.2 PFC motor drive implementation

The PFC motor drive is the system implemented on the aluminum substrate PCB. As previously mentioned it consists of a PFC converter part and a 3 three-phase inverter motor drive. Similar to the supply board, the solder paste was applied with a stencil ensuring proper soldering of all SMD, and the components were placed by hand, an illustration of the process is shown in Figure 9.2.1.

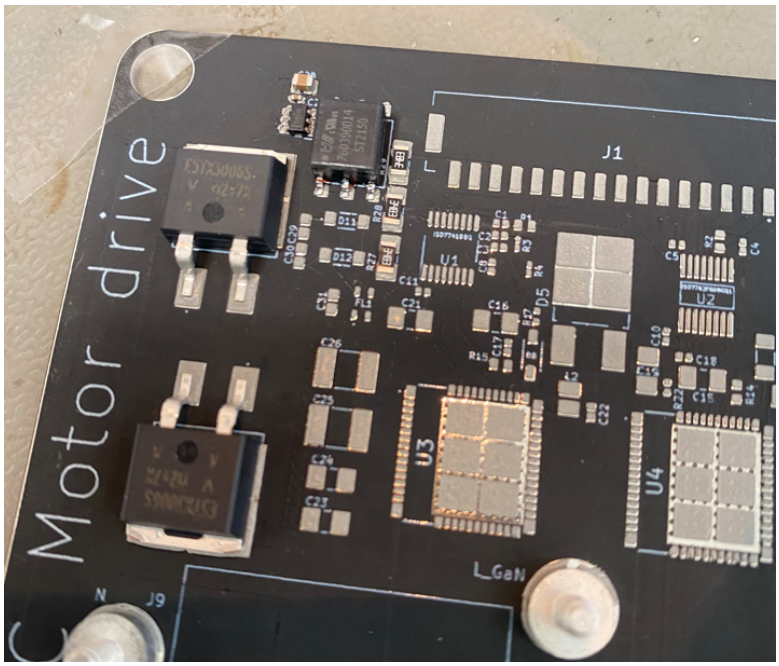


Figure 9.2.1: Soldering machine used for the soldering process

When all the components were properly soldered the wires and connection terminals could be connected. From the PCB design editor the terminals of the different connections were not sized properly and therefore had different pitch sizes and terminal houses, therefore custom-made connection wires were created and thereafter good connection between the PFC motor drive IMS, the supply board, and the microcontroller. Now, the initial tests of the PFC motor drive could begin.

DC-Link voltage reference test

The voltage divider of the voltage measurement is implemented on the PFC motor drive IMS. This test was to ensure proper feedback of the DC-voltage provided by the voltage divider. From the test voltages from 0-60V was applied to the V_{DC} terminals, and the measured voltage was observed Figure 9.2.2 and Table 9.3:

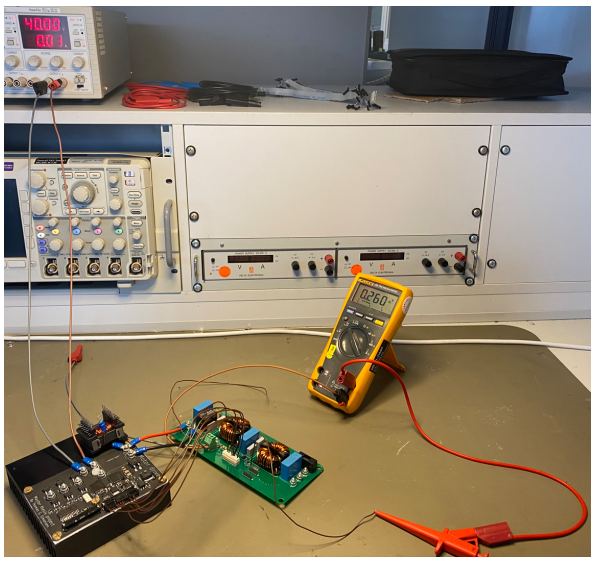


Figure 9.2.2: DC-Voltage test

V_{DC} voltage divider - Test measurements	
DC-Voltage [V]	Voltage reference [V]
5	0.022
10	0.051
15	0.090
20	0.120
25	0.155
30	0.190
35	0.225
40	0.260
45	0.295
50	0.331
55	0.366
60	0.401

Table 9.3: Voltage feedback to MCU

In this test, it is clearly highlighted that the sensitivity of the DC voltage measurements is 7mV/V, which then corresponds to 2.73V at 390VDC, which therefore also leaves a margin for overvoltage measurements. This sensitivity is then calibrated with the microcontroller and here no offset is needed since the DC voltage does not have a negative value, the maximum measurements ranging between 0V-470V.

PFC motor drive rework processes

The initial tests of the IMS did not prove to work right away, there were some complications and errors which had to be fixed before the PCB had proper operation. These complications and errors will always exist in a prototyping phase, and therefore also constitute that several iterations of development are necessary when developing new technology. On the developed circuit the ground properties of the isolated side of the digital isolator IC were grounded to the supply side and the totem pole configuration was grounded to the neutral of the single phase input this changed the communication properties of the system and the supply voltage to the GaN switches. Therefore common ground was implemented with live wires on top of the PFC board.

The operating voltage enabling the digital isolators was also initially set to 5V, which was discovered to have a threshold voltage that was too high for the PWM signal to be sent out on the output side, as the high-level input voltage had a maximum of $0.7 * V_{CC} = 3.5V$ and the PWM reference from the microcontroller only supplied with 3.3V. Therefore the 5V external supply was set to 3.3V instead to ensure sufficient PWM reference to the GaN switches.

This also affected the 5V supply for the isolated 12V supply needed to drive the top-side GaN switch. Therefore, this change in low voltage supply meant that an extra external supply had to be implemented, to establish the desired isolated 12V supply. The connection from the previous 5V supply had to be cut which was done with a drill at a specific place on the PCB since this was a buried connection. After all the rework had been done, and the corrections ensured the correct operation of the PFC motor drive, all initial tests could be validated again and calibrated with the microcontroller, both for the supply board and the PFC motor drive IMS, and the full setup could be assembled as shown in Figure 9.2.3.

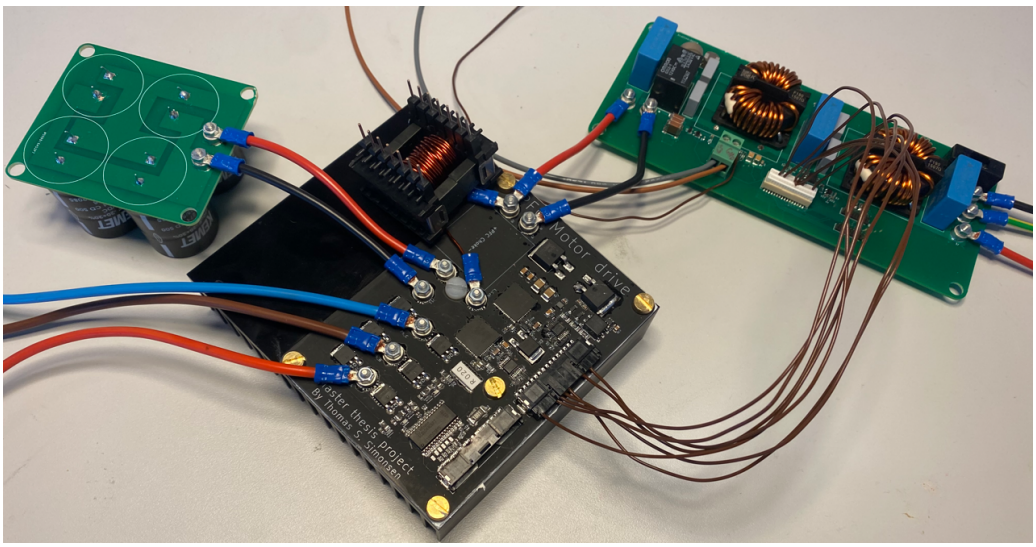


Figure 9.2.3: Complete setup of PFC motor drive

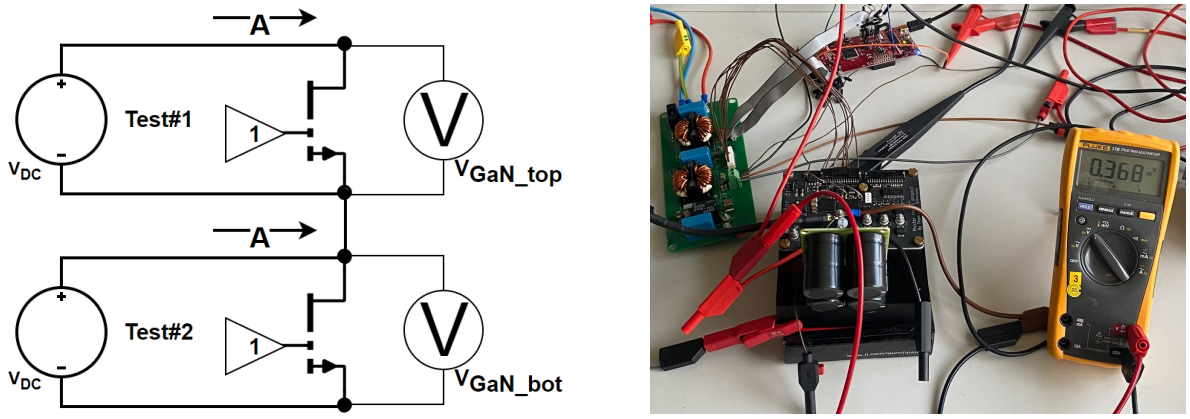
Chapter 10

GaN on IMS tests

In this chapter the tests of the GaN switches on IMS will be performed, starting with a thermal resistance test to compare and validate the thermal resistance values estimated and used in the simulation models. Secondly, a switching test has been performed to investigate the switching performance of GaN switches on IMS. Thirdly, a load test has been performed to investigate if it was possible to reach the desired power ratings, as well as observing the sinusoidal operation of the RL load.

10.1 Thermal resistance validation

The thermal test was carried out by closing each of the switches separately, drawing current through the switches and observing the power dissipation, drain-source resistance, and temperatures to calculate the thermal resistance of the setup. The test setup is shown in the following Figure 10.1.1



(a) Rth test configuration

(b) Physical Rth test setup

Figure 10.1.1: Thermal resistance test configuration and setup

Initially, test number 1 will be performed by drawing 10A and 14A through the top GaN switch, and afterward test number 2 with the bottom GaN switch. The test will reveal the drain-source resistance of the switch by measuring the voltage drop across the switch making it possible to calculate the specific R_{DS_on} for each of the switches at a given temperature. The tests were run with and without the fan to measure the difference in thermal resistance with and without forced air through the heatsink. The typical R_{DS} value is around 25mΩ and maximum 35mΩ at 25°C and typical 45mΩ at 125°C. The following results were obtained Table 10.1:

Thermal resistance test without forced air						
Test #1	Current	Voltage	R_{DS_on}	Temp	R_{th}	P_{loss}
Upper GaN	10A	0.376V	37.5mΩ	37.9°C	3.43 °C/W	3.76W
	14A	0.568V	40.5mΩ	55.7°C	3.866 °C/W	7.94W
Test #2						
Lower GaN	10A	0.464V	46.4mΩ	49°C	5.172 °C/W	4.64W
	14A	0.711V	50.7mΩ	73°C	4.82°C/W	9.954W
Thermal resistance test with forced air						
Test #1	Current	Voltage	R_{DS_on}	Temp	R_{th}	P_{loss}
Upper GaN	10A	0.374V	37.4mΩ	33°C	2.14°C/W	3.74W
	14A	0.547V	39.1mΩ	44°C	2.481°C/W	7.658W
Test #2						
Lower GaN	10A	0.444V	44.4mΩ	40°C	3.378°C/W	4.44W
	14A	0.663V	47.4mΩ	57.8°C	3.534°C/W	9.28W

Table 10.1: Thermal resistance test results

In the test results Table 10.1 it is clearly observed that the thermal resistance of the IMS is lowered with the forced air through the heatsink. It is also observed that the lower GaN switch has a higher drain-source resistance than the upper GaN switch which could be some of the explanation for the higher power losses. The thermal resistance is higher for the lower GaN switch as well, which means there could be a bad thermal path because of a poorly placed TIM layer, where an air bubble could be located close to the lower switch. The same applies to the test results with forced air but at a much lower thermal resistance. If these results are compared to the estimated thermal resistances of the GaN switches Section 4.3.2 these values can be validated Table 10.2:

Thermal resistance comparison without forced air					
Test #1	Current	Temp	R_{th}	Estimated R_{th}	ΔR_{th}
Upper GaN	10A	37.9°C	3.43 °C/W	4.465°C/W	1.022°C/W
	14A	55.7°C	3.866 °C/W	4.465°C/W	0.599°C/W
Test #2					
Lower GaN	10A	49°C	5.172 °C/W	4.465°C/W	0.707°C/W
	14A	73°C	4.82°C/W	4.465°C/W	0.355°C/W
Thermal resistance comparison with forced air					
Test #1	Current	Temp	R_{th}	Estimated R_{th}	ΔR_{th}
Upper GaN	10A	33°C	2.14°C/W	2.265°C/W	0.125°C/W
	14A	44°C	2.481°C/W	2.265°C/W	0.224°C/W
Test #2					
Lower GaN	10A	40°C	3.378°C/W	2.265°C/W	1.113°C/W
	14A	57.8°C	3.534°C/W	2.265°C/W	1.259°C/W

Table 10.2: Thermal resistance comparison between forced air and unforced airflow

From this comparison Table 10.2 it is clearly observed that the measured thermal resistances correspond closely to the estimated Rth values used in the simulation model. For the comparison without forced air, the thermal resistance value is lower for the upper GaN than the estimated resistance and higher for the lower GaN, where this deviation could be caused by other factors than the Rth of the layers, as explained earlier, such as TIM layer, spreading, etc. The average measured thermal resistance is 4.332°C/W which is almost identical to the

estimated Rth with a 4% deviation. For the comparison with forced air, the estimated Rth value is really close to the upper GaN Rth with very little deviation, whereas the lower GaN has a larger deviation. The average measured thermal resistance is 2.883°C/W which is a 27% deviation. All thermal resistance is relatively close to the estimated Rth values, and it can be concluded that the Rth values used in the simulation are valid for modeling the IMS temperatures.

10.2 Switching test

In the switching test, the setup is an inverter configuration where the no-load switching performance is measured between the output of the half-bridge and the reference point between two DC supplies Figure 10.2.1:

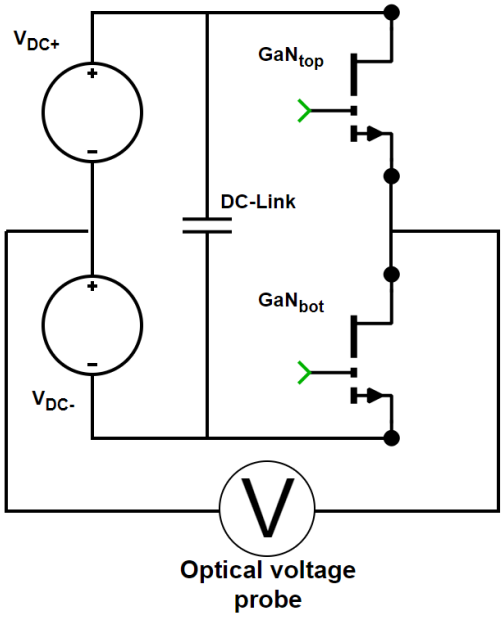
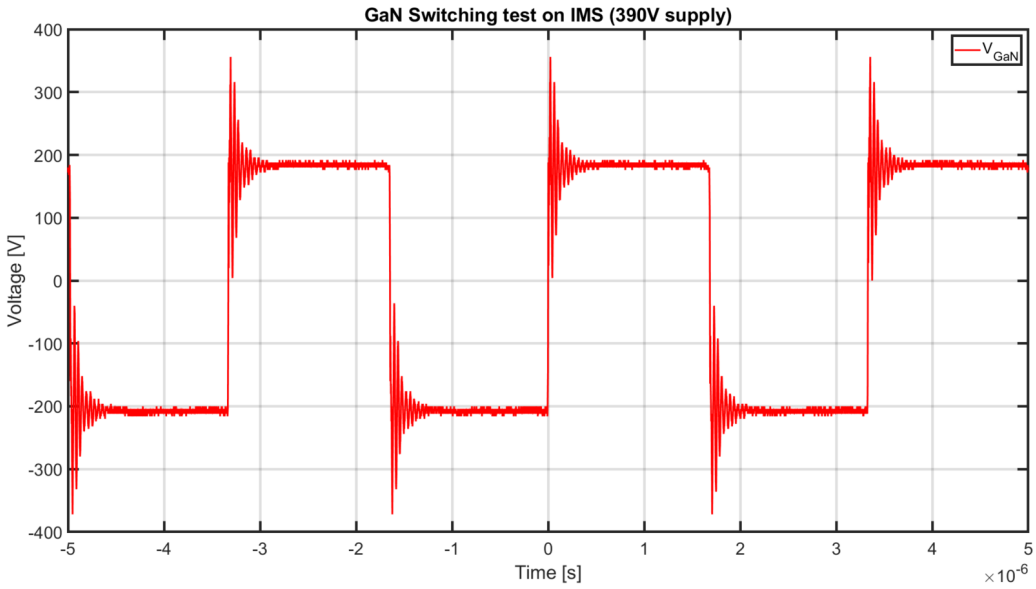
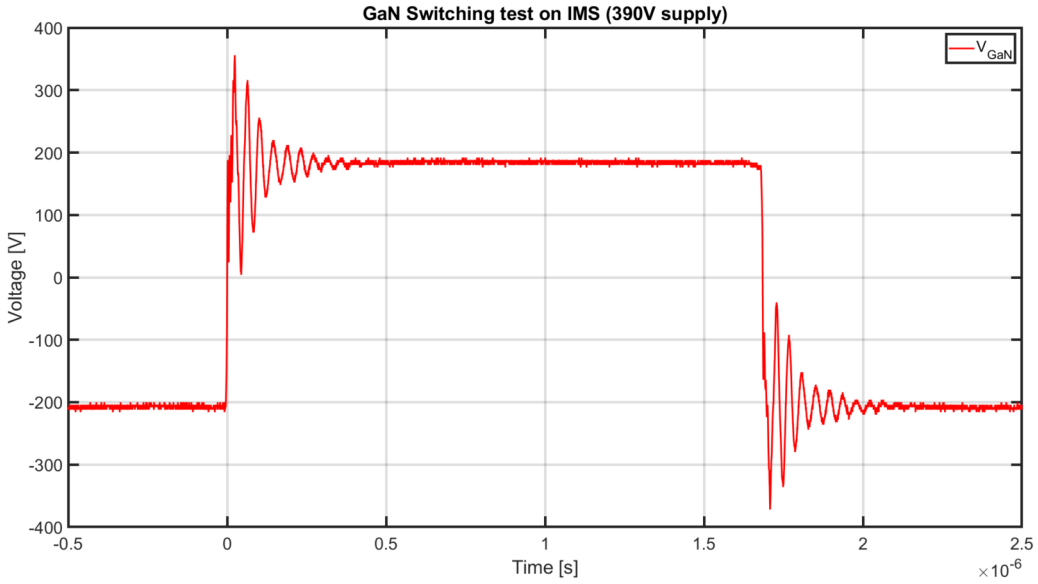


Figure 10.2.1: Test setup of GaN in inverter configuration

In this test, a constant duty cycle will be applied and the switching characteristics will be observed. The critical thing to focus on during this test is the overshoot and oscillations of the switch turn on and turn off. The test was initiated with low voltages and was slowly increased during several tests up to a maximum of 390V, which implied 195V on each DC source, and in the measurements seen as -195V to 195V. The following switching characteristics of the test can be observed in Figure 10.2.5:



(a) Continuous operation at 300kHz



(b) Zoomed to one period

Figure 10.2.2: Switching test

From Figure 10.2.2a it is clearly shown that there is sufficient turn-on and turn-off at 300kHz, the time on the graph shows one period to be around 3.3μs which corresponds to a frequency of 1/T = 303kHz. In Figure 10.2.2b there is a closer view of the turn-on and turn-off characteristics, again, the switching is showing good results on the IMS with the overshoot and oscillations running out to a steady state in 0.4μs. The rise time characteristics of the turn-on are shown in Figure 10.2.3:

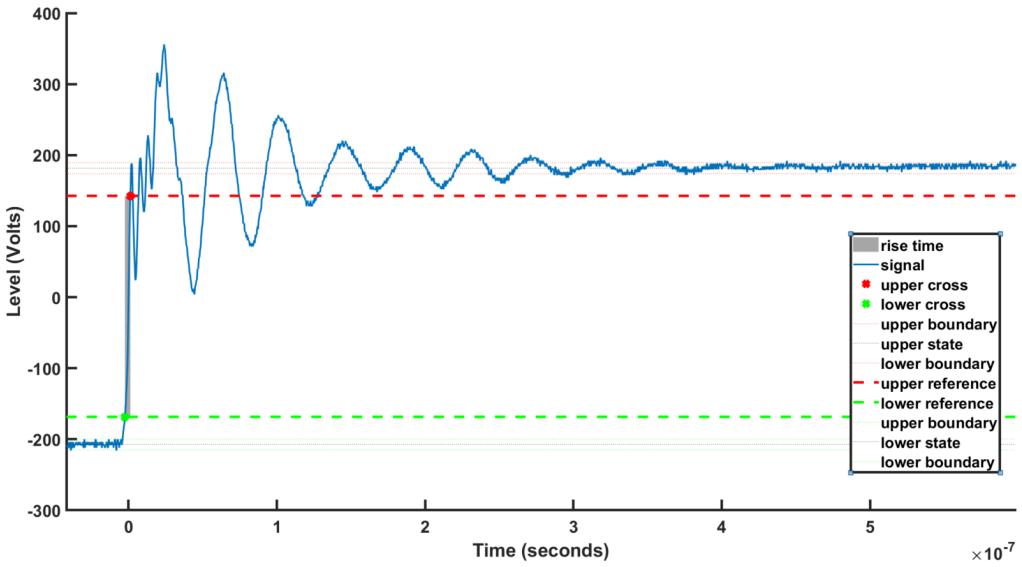


Figure 10.2.3: Risetime analysis of GaN turn-on on IMS

Here, the rise time is calculated to be 3.625ns which corresponds to a slew rate of 107V/ns. The slew rate was configured to be between 100V/ns to 150V/ns, so an acceptable slew rate is measured. When running at lower voltages the slew rate was significantly lower. This is due to the output capacitance since its value will be higher at lower voltage levels. The output capacitance has a significantly higher value until 175V seen in Figure 10.2.4 where it has a slight linear decrease until the rated voltage[13].

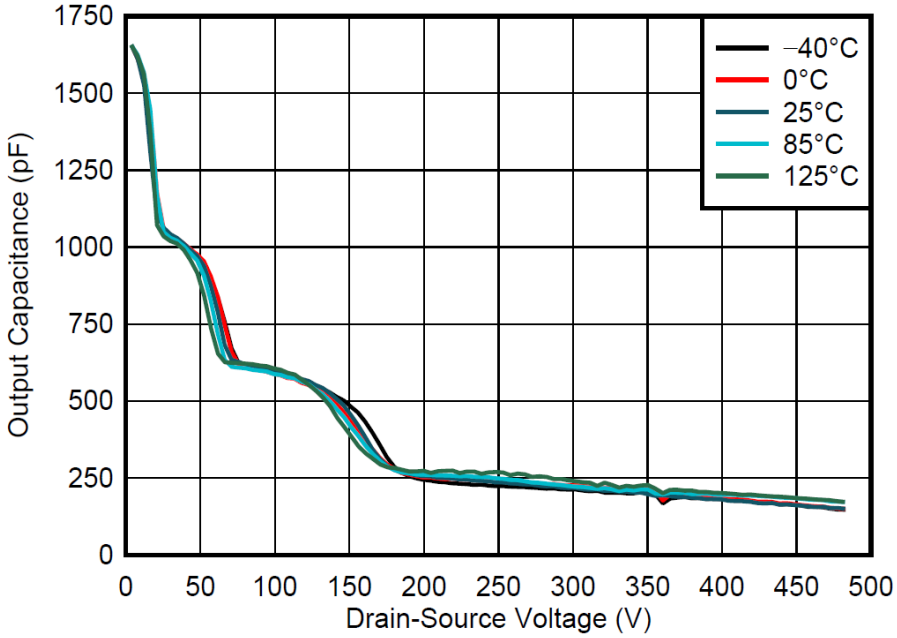
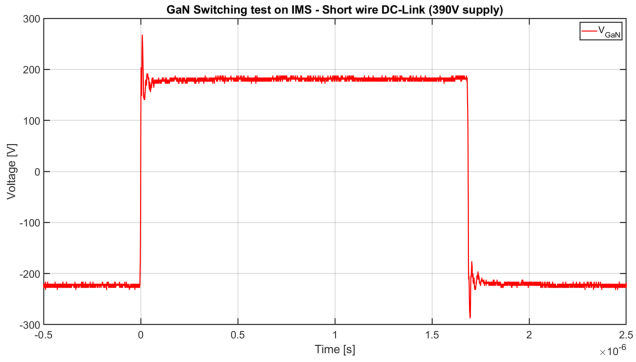


Figure 10.2.4: Output Capacitance vs Drain-Source Voltage

From these observations of the switching tests, improvements to reduce the oscillations were considered, since there are oscillations, and basic switching dynamics can be considered. A possible contributor to the oscillations could be the long wires from the DC terminals and the DC-link capacitors. To test this assumption the wires were removed at attached closely to the DC terminals. The following measurements with the closer DC-link were obtained Figure 10.2.5a:



(a) Short wire DC-Link switching test at 390V (b) From GaN Datasheet on FR4 PCB

Figure 10.2.5: Switching test

In Figure 10.2.5a at is clearly shown that the shorter DC-Link wires has a huge impact to the oscillations after turn on. It has a much smaller overshoot and almost no oscillation afterwards, concluding that the IMS design is really good, and the oscillations left are due to the small distances there still are between the capacitors. The rise time is 3.4ns and the slew rate is around 114V/ns. In Figure 10.2.5b a comparison of the switching performance on an FR4 PCB is shown. Comparing that to the IMS switching performance of GaN on IMS, it is observed that there is almost no difference between the two, and the slight difference could be caused by the distances between the capacitors still existing on the IMS. Concluding that IMS has a great switching performance utilizing GaN switches at high switching frequencies. To see the clear difference between the long and short wires of the DC-link Figure 10.2.6 has been made:

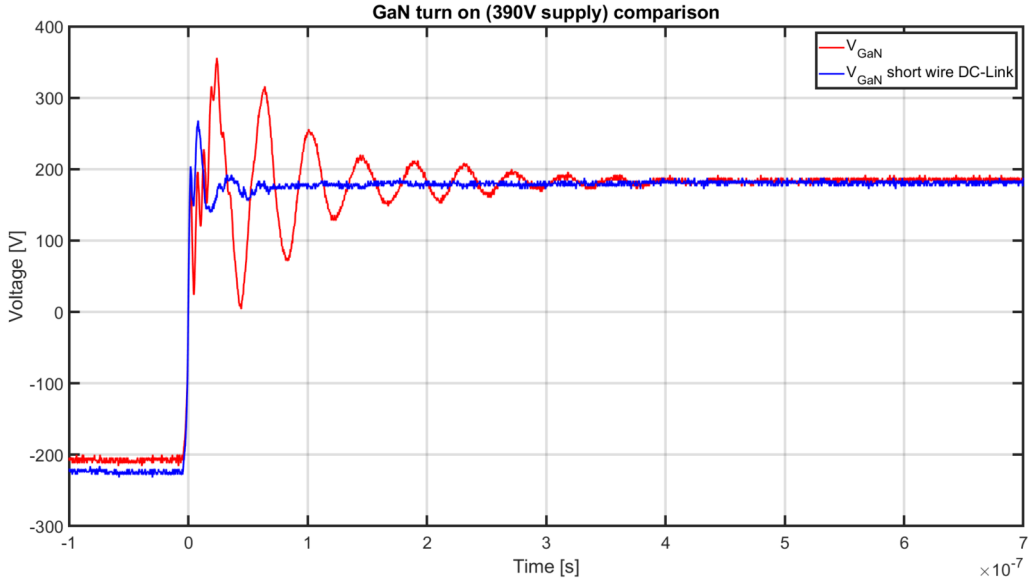


Figure 10.2.6: Comparison between lond and short DC-Link wires

A significant decrease in the overshoot of almost 100V from 350V to 250V and the oscillations have decreased to one oscillation for the short DC-link. This concludes that the design of the IMS can be optimized to perform similarly to conventional FR4 PCBs with a great switching performance at high frequencies.

10.2.1 Results of GaN switching test

From the switching test, it is clear that the switching performance of the GaN switches on IMS lives up to the expectations. It has an acceptable rise time with a slew rate measured up to 114V/ns. The fast reduction of overshoot oscillations shows that the IMS is not making any unwanted disturbances such as EMI noise and that the design of the power loop is sufficiently optimized. If the performance needs to be optimized further, Finite Element Method (FEM) analysis of the circuit should be used, for understanding the inductive and capacitive effects of the circuit design.

The test also shows that the GaN switches are capable of achieving 300kHz switching frequency with great operating performance. Therefore it can be concluded that GaN on IMS does have a good switching performance on IMS under unloaded operation, and the circuit design of the PFC converter power loop is optimal within the expectations of basic EMI knowledge of switching circuits and that the switching performance is not reduced due to the IMS PCB compared to conventional PCBs.

10.3 GaN load test (DC- reference)

The GaN load test was carried out to produce power loss from the GaN switches to see their behavior when having current flow. Initially, the test was executed in the same inverter configuration with two DC sources in series and the output of the GaN half-bridge was connected to the reference point. The duty cycle of the half-bridge was set to 50% for a balanced power loss distribution, but in this configuration at 50% duty-cycle, the RMS current will be close to zero, since the ripple is switching around 0. Because of that, there will not be any current flow when the reference point is between the DC sources, and the change in resistive load has almost no effect on the current, therefore the reference point was changed to DC- as shown in Figure 10.3.1:

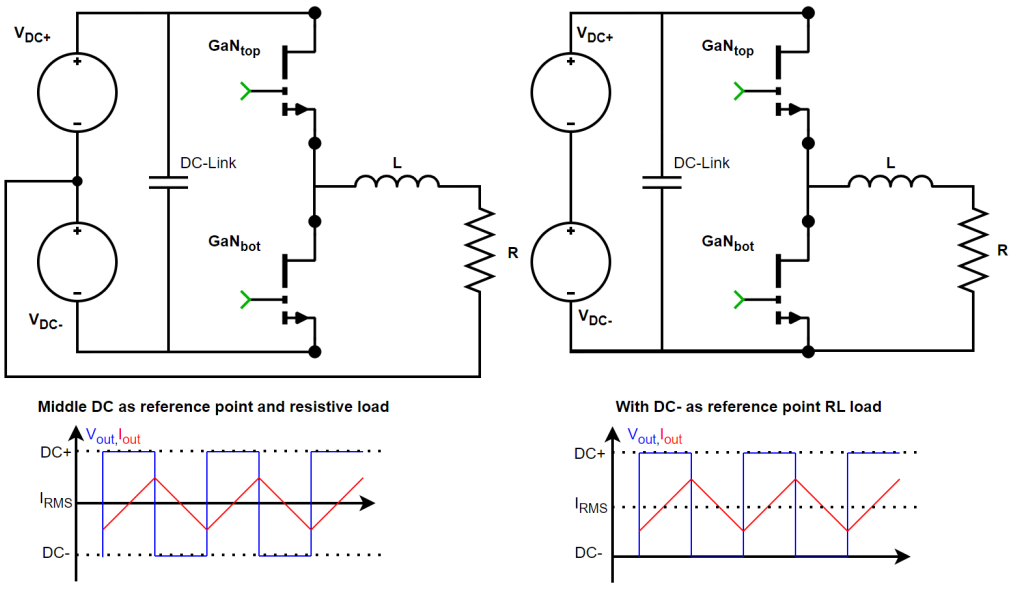


Figure 10.3.1: Change of test configuration

The reason behind the change can be seen in the following equations first for the reference point in the middle of the two DC sources Equation (10.1), and secondly with the reference point at DC- Equation (10.2). The current is directly proportional to the voltage applied

across the resistor, whereas when an inductor is included the current will be stored in the inductor:

$$I_{Mid\_DC} = \frac{D * V_{Mid\_DC}}{R} = \frac{0.5 * 0V}{22\Omega} = 0A \tag{10.1}$$

$$I_{DC-} = \frac{D * V_{DC-}}{R} = \frac{0.5 * 120V}{22\Omega} = 2.72A \tag{10.2}$$

In the configuration with DC- as a reference current is now flowing and the load test can begin. As a starting point, the load was applied at 20VDC and 22Ω, and run for at least 10 minutes to ensure that the system was corresponding as desired, and that the thermal distribution of the switches was withing the limits. This process was initially done stepwise at low voltage levels from 20V to 120V and decreasing the resistance value for obtaining close to the rated current of the designed PFC. Afterwards, new voltage supplies were used to obtain a full voltage level of 390V. The following measurements of maximum load in this specific configuration can be seen in the following Figure 10.3.2:

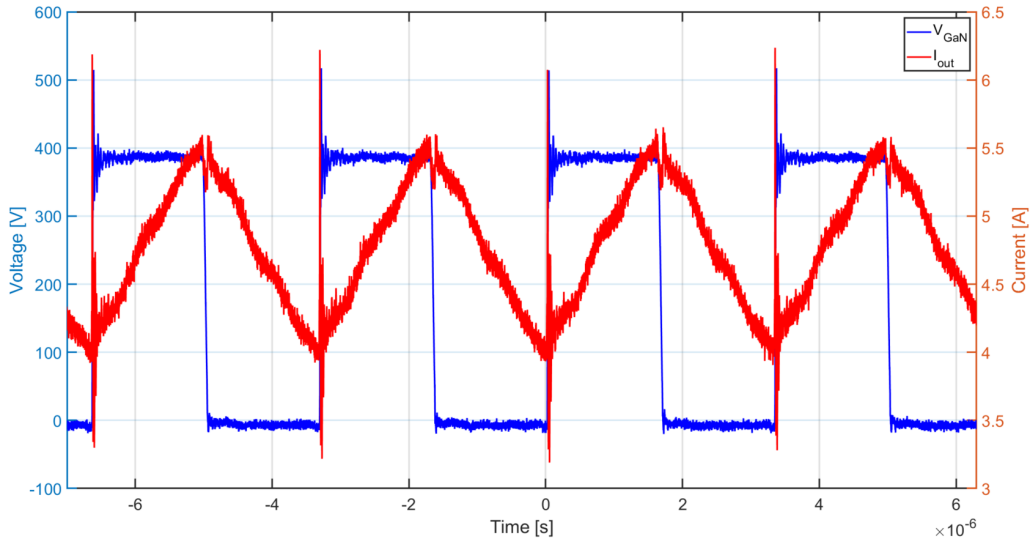


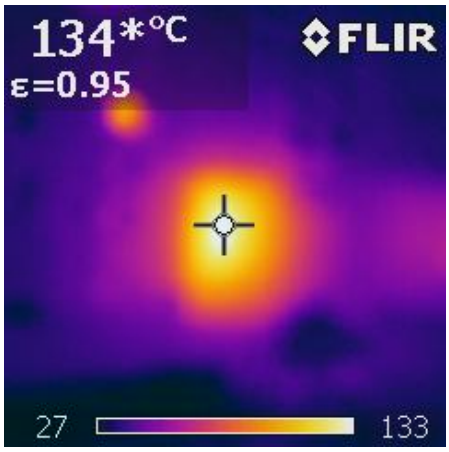
Figure 10.3.2: GaN load test measurements

The interesting observations during this test are that the switching characteristics of the GaN switches still perform as expected and the overshoot oscillations reduce with a settling time of 0.5μs. It is also clear that at 1.8kW load the GaN switches operate unaffected. The goal of this test was to create heat dissipation from the switches to the heatsink and test that the temperature values were kept within the operating limits of the GaN switches. In the initial tests an unbalance in the temperature between the two switches was observed, this temperature unbalance between the two switches, can be explained by the current flow and operation of the GaN switches. The GaN switches have an Ideal-Diode mode operation, where they will be conducting in the opposite direction during off-state. When the upper switch is turned on there will be a current flowing and therefore under hard switching operation. When the bottom switch is turned on, the voltage potential will be zero because of the reference point and therefore operate in soft switching. Therefore the upper switch will dissipate losses from both conduction and switching, whereas the bottom switch only has conduction losses and no switching losses. Despite the unbalance, this test was performed due to the possibility of creating high power losses. During the test, the GaN switches were supplied with different voltage levels between 50V-390V, and the RMS current was measured together with a thermal camera observing the temperature of the GaN switches as shown in Table 10.3:

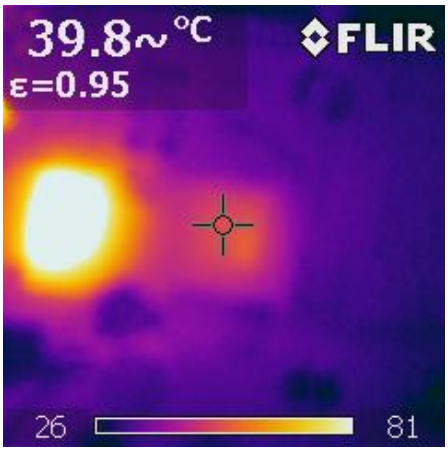
Load test with DC- reference			
Voltage	RMS Current	Temperature	Power level
50V	612mA	30°C	30.6W
100V	1.217A	38°C	121.7W
150V	1.813A	47.7°C	272W
200V	2.420A	60.4°C	484W
250V	2.995A	75.8°C	748.8W
300V	3.588A	90.6°C	1076.4W
350V	4.312A	116°C	1509.2W
390V	4.805A	134°C	1838W

Table 10.3: Load test of GaN switches on IMS in V_{DC-} configuration

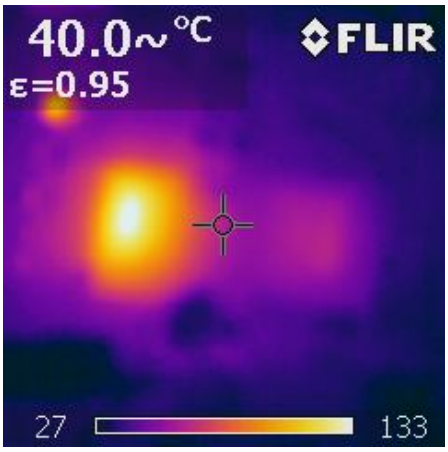
The test was carried out with full voltage levels, this was still in mind with the unbalance due to the soft switching operation of the bottom switch. The heatsink also had a fan ensuring forced airflow through the heatsink to avoid overheating of the switches. In the test Table 10.3 a 38Ω resistor was used and the fan was operating at 7.68W. The results show that it is possible to operate close to the desired 2.2kW power output and as mentioned in Section 10.1, the derating could be due to bad TIM layer, spreading or other circumstances than the circuitry. The temperatures correspond approximately to the maximum junction temperature of the GaN switches and reach 134°C at maximum voltage with the 38Ω resistance as shown in Figure 10.3.3:



(a) Upper GaN switch



(b) Lower GaN switch



(c) Heatsink

Figure 10.3.3: Thermal Temperature measurements GaN load test

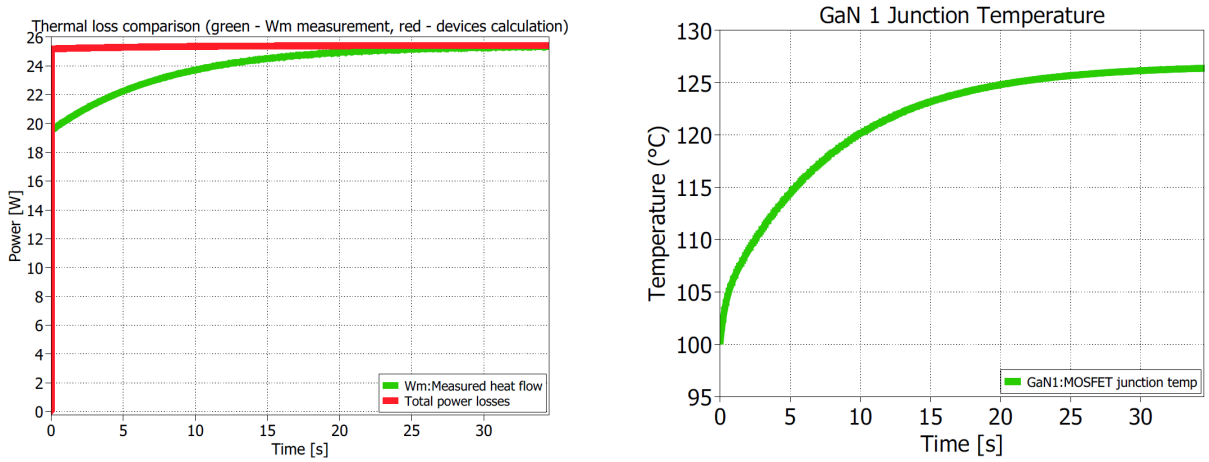
The thermal images highlight the temperature unbalance, in Figure 10.3.3a the full power loss is observed with the high temperature in the upper GaN switch. Calculating the power losses in the switch from the thermal resistance we get a power loss of:

$$P_{loss_{upper\_GaN}} = \frac{T_{meas} - T_{amb}}{R_{th_{upper\_GaN}}} = \frac{136°C - 25°C}{2.481°C/W} = 43.9W \tag{10.3}$$

From simulations Chapter 6 the nominal operation of the PFC shows around 43W total power loss at 2.2kW operation. In Figure 10.3.3b the temperature is similar to the heatsink Figure 10.3.3c around 40°C showing that the conduction losses in the switches are minimal and that the lower GaN switch temperature could be following the heatsink temperature because the high power loss from the upper switch is dissipated to the heatsink. Since there are no switching losses in the lower switch due to soft switching, the conduction losses of the lower switch correspond to the following:

$$P_{loss_{lower\_GaN}} = \frac{T_{meas} - T_{amb}}{R_{th_{lower\_GaN}}} = \frac{40°C - 25°C}{3.534°C/W} = 4.24W \tag{10.4}$$

This calculation highlights that the power loss contribution is almost only coming from switching losses. Since the conduction loss only corresponds to 10% of the total power loss. This showcases that at balanced operation the switching losses would be evenly distributed and that operation at 2.2kW would easily be achieved since the obtained measurements show the capability of operating at 1.8kW with all losses in one switch and therefore assume to be working at 3.6kW with even distribution. To compare the temperature measurements, a simulation has been made with the same operating values of 390V 4.8A Figure 10.3.4.



(a) Heat flow

(b) Upper GaN temperature

Figure 10.3.4: Simulation results of GaN load test

In simulation, the thermal capacitance has been neglected, so the heatsink temperature has an initial temperature value, and assumingly has a faster temperature rise time than in the physical setup. In simulation, the heatsink temperature in steady state is around 98°C with a heat sink thermal resistance of 2.9°C/W. This simulates the junction temperature of the upper GaN switch at 126°C where the measured junction temperature is 136°C thereby having a 10°C deviation.

10.3.0.1 Results of full voltage GaN load test with DC- reference

In the full voltage GaN load test at DC- reference, the maximum power rating is almost reached at 1.838kW and shows that the IMS is capable of cooling the switches at these

power levels. With even loss distribution, it can also be assumed that the test shows the possibility of operating at minimum rated power of 2.2kW, and possibly up to 3.6kW. From the simulation model in Figure 10.3.4 the test shows that the thermal resistance levels are corresponding with the physical behavior with a 7.9% deviation. The cause of not reaching the full power rating is due to the unbalanced operation of the switches, where all the power losses are contributed from the upper switch, and therefore heats up more intensely. Another reason for the derated power could be because of the TIM layer applied by hand, making it non-uniform and could create air bubbles. In the resistance test, this was shown to be significant for the lower switch, where the upper switch showed great thermal resistance behavior, making the effect a small contributor. The load test also showed that the design of the PFC converter is sufficient and that the control circuitry with digital isolators and supplies can operate efficiently at full voltage levels and high power operation. Lastly, the test highlights that the power losses are significantly contributed by switching losses and have a very low conduction loss, where the distribution of the two losses is 90% for the switching losses and 10% for the conduction losses.

10.4 GaN inverter load test with sinusoidal output

In the previous test, an unbalance between the two switches were observed when using V_{DC-} as a reference. Therefore a new configuration was established to create a test with balanced losses. This was also an inverter configuration but now with a sinusoidal output because of a sine wave modulation at 50Hz oscillating the duty cycle between 0 and 1. The reference is now set between the two voltage sources as shown in the following Figure 10.4.1:

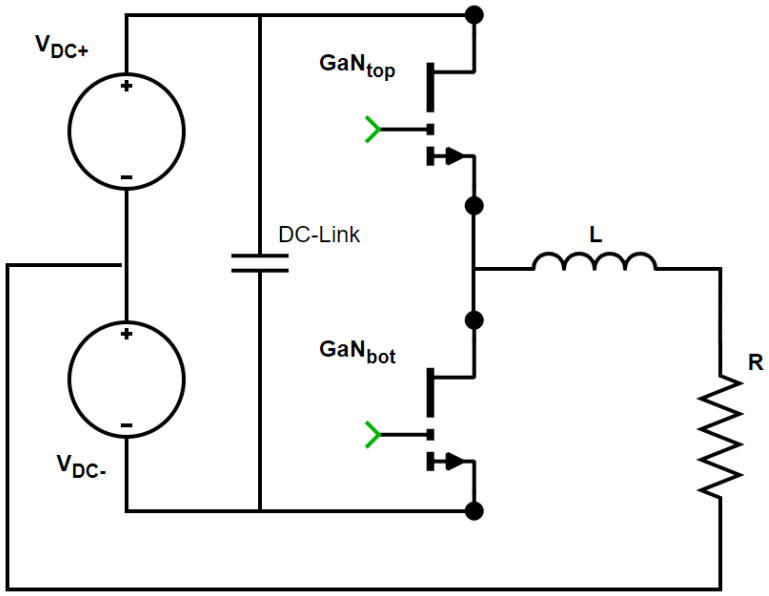


Figure 10.4.1: Inverter configuration test setup

In this configuration, the hard switching operation is obtained for both switches, which also will be the case when running the GaN switches as a PFC converter. The temperature is now balanced and the switching losses are evenly distributed. This type of operation is close to the PFC configuration but inverted where the input is the DC voltage generating a sinusoidal output. Therefore it is also possible to look at the sinusoidal current of the inductor as this ripple will correspond to the current ripple in a PFC configuration. The following test results were obtained Table 10.4:

Load test - Inverter configuration			
Voltage	RMS Current	Temperature	Power level
50V	219mA	30°C	10.95W
100V	436mA	36.8°C	43.6W
150V	646mA	42.9°C	96.9W
200V	852mA	51.8°C	170.4W
250V	1.068A	61.6°C	267W
300V	1.276A	73.3°C	382.8W
350V	1.480A	84.9°C	518W
390V	1.650A	99.4°C	643.5W

Table 10.4: Load test of GaN switches on IMS sine output configuration

The main goal of this test was to observe the switching and sinusoidal behavior of the current. High output power was not reached because of current limitations by the DC sources due to a very high current spike from the sources. It was therefore the main goal to include a resistance value where the full voltage level could be obtained. In this case, the resistance value in the LR-load was 76Ω, and from this, the following switching and sinusoidal behavior was obtained Figure 10.4.2:

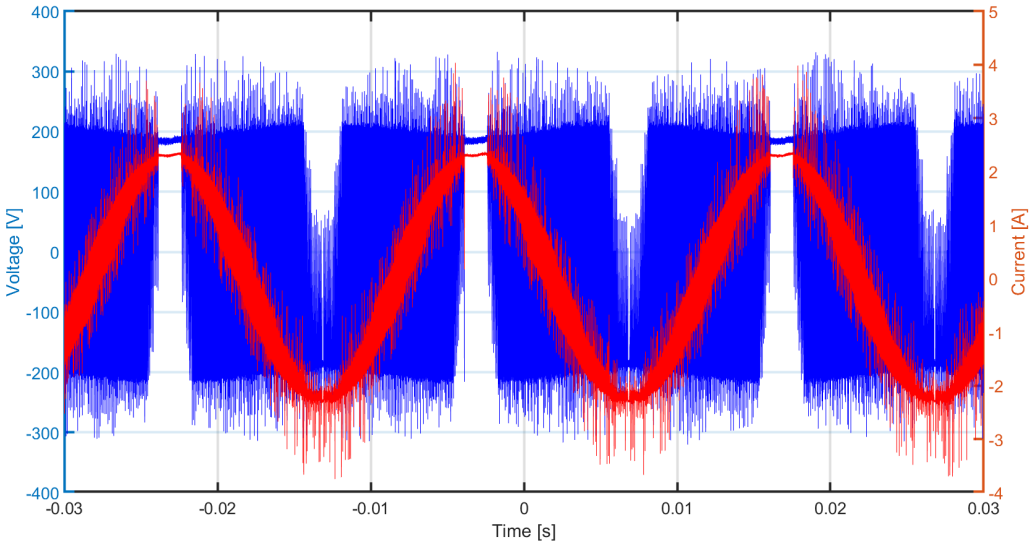


Figure 10.4.2: Swithced voltage and current output

This figure shows an oscillating behavior of the switched voltage, which on average gives a sinusoidal voltage. The current also has a variating ripple, with the ripple having the biggest deviation around the zero crossing and the most minor ripples on the peak. This is due to the voltage deviation of the input voltage, where at 0V the deviation will be highest at 195V thereby contributing to a large ripple, whereas at voltage peak, the deviation is 0V, and therefore no ripple is observed. In the following Figure 10.4.3 the mean voltage is shown and a cut of the ripple is extracted to show the size of the current ripple:

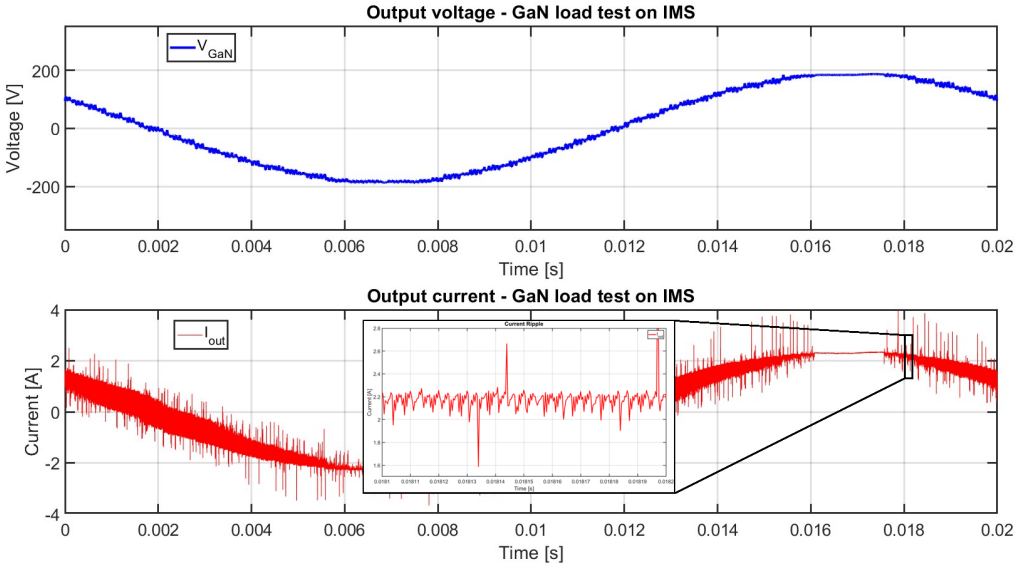
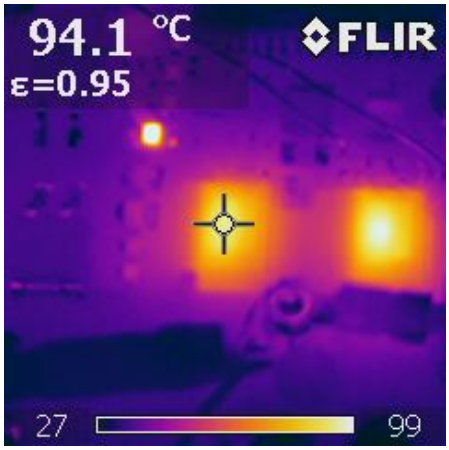


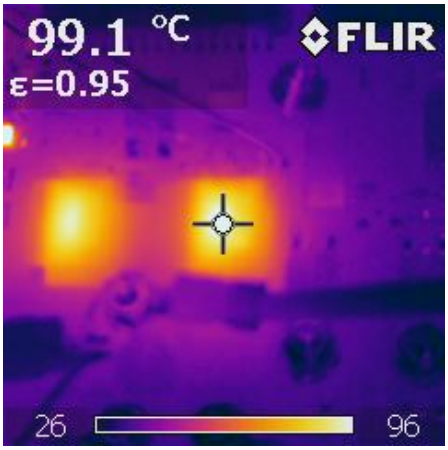
Figure 10.4.3: Voltage and current output with ripple

The current ripple just after the peak is around 10% of its value which is around 2A is 0.2A ripple. This corresponds to the maximum ripple in the calculations of the inductor size.

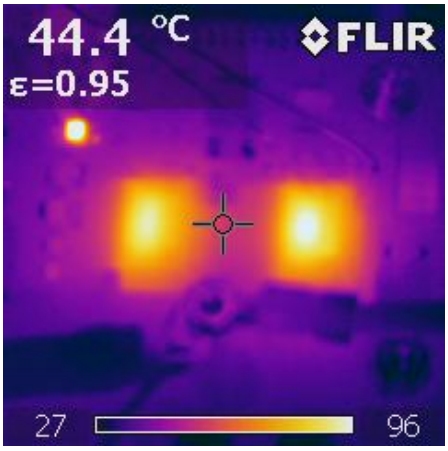
At a maximum voltage of 390V and current of 1.650A the power output is 643.5W and the temperature of this test can be seen in the following Figure 10.4.4:



(a) Upper GaN switch



(b) Lower GaN switch



(c) Heatsink

Figure 10.4.4: Thermal Temp measurements GaN sine output test

From these temperature measurements an even temperature distribution is observed, this shows that the switches are sharing the switching losses. The temperature values of around 100°C gives a 50°C margin to the maximum junction temperature. The total power losses of each switch can be calculated from the measured temperatures:

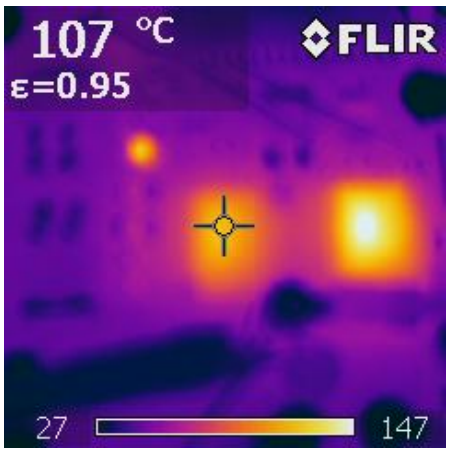
$$P_{loss_{upper\_GaN}} = \frac{T_{meas} - T_{amb}}{R_{th_{upper\_GaN}}} = \frac{94.1°C - 25°C}{2.481°C/W} = 27.85W \tag{10.5}$$

$$P_{loss_{lower\_GaN}} = \frac{T_{meas} - T_{amb}}{R_{th_{lower\_GaN}}} = \frac{99.1°C - 25°C}{3.534°C/W} = 20.97W \tag{10.6}$$

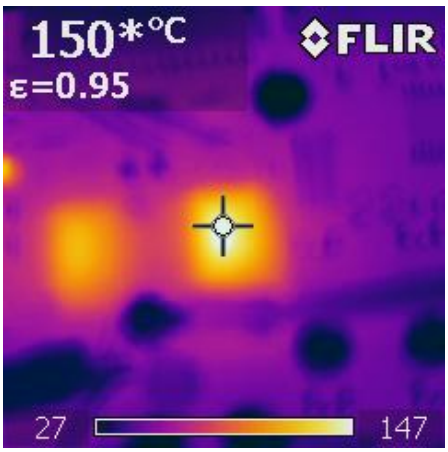
$$P_{Total} = P_{loss_{upper\_GaN}} + P_{loss_{lower\_GaN}} = 48.82W \tag{10.7}$$

Since the power losses consist of almost only switching losses, the increase in voltage will have a high contribution to the amount of switching losses, whereas the increase in current, will have a higher contribution to conduction losses. Therefore, it can be assumed that an increase in the load and therefore the current would have a very small temperature increase effect on the switches, and it would therefore have been possible to reach the rated power if the DC sources did not go into current limitations due to an unexplained current peak from the sources. The calculations of the total power losses also shows that the switches are able to operate at a total power loss of 48.82W which in previous simulations is significantly higher than the total losses calculated from the PFC converter simulations.

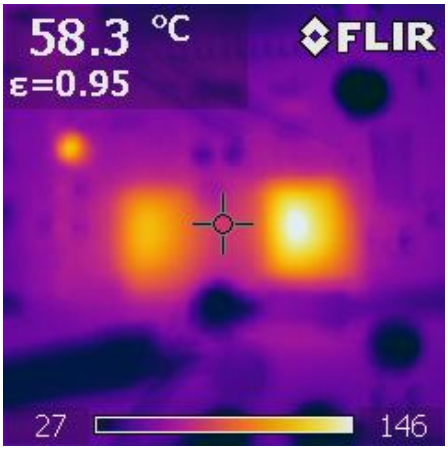
To compare the temperature values from the inverter test with sinusoidal output, a secondary test was performed to show the operation without forced air through the heatsink. The following temperature values were obtained at a similar maximum load as showed in the forced air measurements Figure 10.4.5:



(a) Upper GaN switch



(b) Lower GaN switch



(c) Heatsink

Figure 10.4.5: Thermal Temp measurements GaN sine output test without forced air

In this test, we can see the significance of the larger thermal resistance value in the lower switch, where it under peak operation reaches the maximum junction temperature limit of the GaN switches. The thermal measurements also show, that if the GaN switches had similar, thermal resistance, the IMS would be able to cool the switches without forced air at a power rating of 643.5W with a margin of 43°C. The total power loss of the GaN switches without forced air is calculated:

$$P_{loss_{upper\_GaN}} = \frac{T_{meas} - T_{amb}}{R_{th_{upper\_GaN}}} = \frac{107°C - 25°C}{3.866°C/W} = 21.21W \tag{10.8}$$

$$P_{loss_{lower\_GaN}} = \frac{T_{meas} - T_{amb}}{R_{th_{lower\_GaN}}} = \frac{150°C - 25°C}{4.82°C/W} = 25.93W \tag{10.9}$$

$$P_{Total} = P_{loss_{upper\_GaN}} + P_{loss_{lower\_GaN}} = 47.14W \tag{10.10}$$

Using similar assumptions to the increase of switching losses when increasing the load, there would be a possibility of reaching close to the desired power rating without forced air through the heatsink, and through the total power loss calculations it also shows the IMS is able to cool the switches with a total power loss of 47.14W, thereby showing the great thermal management of the IMS.

10.4.1 Results of GaN inverter load test with sinusoidal output

From the inverter load test with sine output operating GaN switches on IMS it can be concluded that it is possible to operate the switches with a balanced power loss distribution

when running with a sinusoidal output. The measurements obtained from the test shows a significant effect of the difference of thermal resistances between the two switches as calculated in Section 10.1. If this difference were optimized and the DC sources under test did not limit the current it would be possible to operate at the desired power rating both with and without forced airflow through the heatsink.

Chapter 11

Conclusion

Throughout this report, the possibilities of identifying the performance specifications of insulated metal substrate operating with wide band gap devices have been investigated by designing a PFC converter using Galium Nitride semiconductors and testing the thermal resistances, the switching performance, and power ratings. Different Power Factor Correction design guides have been used to create an efficient converter design, for testing and operating GaN switches with a C2000 microcontroller. The development processes from research, design, and implementation to testing phases have increased the knowledge around IMS PCBs for PFC converter and three-phase inverter, and given the possibility to investigate the advantages of using IMS PCBs compared to conventional FR4 PCBs.

The thermal performance of IMS PCBs depends on the choice of dielectric material as well as the choice of the number of layers which affects the thickness, but also the electrical performance. In Section 4.3 of the research chapter, this tradeoff has been considered and a high thermal conductivity layer and two-layer design have been considered the optimal design of a PFC on IMS PCB. The total thermal resistance of the different PCBs was calculated and showed a significant thermal performance of IMS compared to conventional PCBs with a margin of up to 6 times better performance. In simulations Chapter 6 it was highlighted that the IMS was capable of reaching the desired power rating of 2.2kW whereas conventional PCBs only went to 300W at the same maximum junction temperature limitations. Through a thermal resistance test Section 10.1 the Rth values of the two GaN switches were obtained showcasing the validity of the thermal resistances estimated from the calculation using the thermal conductivity, thickness, and surface area. The average measured thermal resistance without forced air through the heatsink was 4.332°C/W obtaining a 4% deviation to the estimated Rth without forced airflow. Similarly, the average measured thermal resistance with forced air was 2.883°C/W obtaining a 27% deviation compared to the estimation. This was a significantly higher deviation but still within an acceptable range and could be due to measurement errors of Rth, as well as a badly placed TIM layer creating air bubbles underneath the GaN, switches. All these observations, tests, and analysis of the thermal performances highlight the conclusion of IMS has a great thermal performance being able to cool GaN switches at 2.2kW and outperforming the conventional PCBs by a great margin.

The switching performance of GaN switches on IMS depends mainly on the circuitry reducing the inductive and capacitive effects through wires and loops. Two-layer design was chosen to create a good turn and return path, together with a very compact design with close connections and small power loops. In Section 10.2 the switching performance of the GaN switches has been tested for observing the switching capabilities on IMS PCB compared to conventional PCBs. Here it was observed that the switching performance in general was sufficient reaching a slew rate of 114V/ns, with acceptable overshoot and ripple oscillations. The design was optimized by reducing the inductive path to the DC-link and significant improvement was shown reducing the overshoot 50% and almost removing the oscillations completely. This switching performance was compared to conventional PCB switching performance and concludes that the IMS switching performance is benchmarking the conven-

tional PCB being able to operate at similar rise times, overshoot, and settling time. The switching test also concludes that great switching performance can be obtained at high frequencies of 300kHz.

The load operation of the GaN switches was carried out in an inverter configuration with constant and oscillating duty-cycle for creating DC and sinusoidal output, respectively. The load test Section 10.3 running at a full voltage level of 390V and a 38Ω resistor, showed the IMS's capabilities of cooling the GaN switches up to a 1.8kW power output. In this test, the power loss distribution was only on one of the switches, and therefore a 43W power loss was seen on the upper switch. This was due to the hard and soft switching operation of the GaN switches, and the switching losses were only placed in the upper switch making it possible to create an assumption of the switches being able to run up to 3.6kW at even switching distribution. The uneven distribution also highlighted that 90% of the losses in the switches were due to switching losses and 10% to conduction losses, concluding that the GaN switches would easily be able to uphold a sufficient temperature at the desired power rating of 2.2kW with and without cooling if the loss distribution were evenly distributed.

The balanced inverter test with sinusoidal output Section 10.4 was performed with the full voltage level of 390V and a 76Ω resistor obtaining only 1.6A and a power output of 640W due to issues with the DC-sources current limitations. Nevertheless, the GaN switches now showed balanced operation and even loss distribution of around 24W per switch totaling 48W power loss. Since the losses mainly consist of switching losses the increase in current will have a less significant effect than the increase in voltage level, making it possible to conclude that the PFC converter would have been able to run at the maximum power rating of 2.2kW. The temperature measurements at 640W only showed around 98°C, therefore, highlighting a margin of 50°C to maximum junction temperature. A second test was made without forced airflow through the heatsink and these measurements showed the significance of thermal resistance differences as there was a 50°C difference between the upper and lower switch temperature. This thermal resistance difference could be caused by a nonuniform thermal interface material layer creating air bubbles which increases the thermal resistance significantly.

Overall this investigation can conclude that there are several advantages to using IMS PCB in a PFC converter configuration with Galium Nitride semiconductors due to the reduction of passive components provided by the high switching frequency improving the power density by making a compact design. The aluminium metal core also shows great thermal management performance and can cool the switches sufficiently from 2.2kW up to 3.6kW and outperforms the conventional PCBs significantly being able to operate at almost 10 times higher power rating. The IMS PCB does not compromise with the switching performance ensuring similar switching characteristics as conventional PCBs ensuring a high slew rate of 114V/ns and low to almost no overshoot oscillations. The investigation can conclude that insulated metal substrate PCBs have a huge potential on low power applications by improving thermal performance and ensuring great switching capabilities.

Chapter 12

Future Scope

In this chapter, the future scope of the investigation will be discussed. This describes the tasks available for improving the results, conclusions, and reflections obtained throughout the project which were not possible to implement due to the time constraints of the project. It highlights other areas to investigate for improving the general picture of IMS PFC motor drives as well as giving inspiration to other considerations.

As a starting point the goal of running the system completely as a PFC converter with feedback is prioritized. This will show the correct converter design as well as give the complete results of the PFC operation on IMS with GaN semiconductors. Similarly, it would be interesting to produce an identical circuit board as a conventional FR4 PCB type to offer a direct comparison between IMS and conventional PCBs operating GaN switches.

Additionally, to the PFC converter operation, an experiment running the full PFC motor drive with motor load would also be interesting to see if the control code developed works as desired, and if the single phase PFC converter can operate a 2.2kW induction motor.

In the existing design of the PFC motor drive, 3 PCBs have been developed to create the drive, making it difficult to calculate the exact power density of the motor drive. Therefore it would be interesting to develop a fully EMI-filter integrated IMS with both supply, control, and microcontroller circuits on the same IMS PCB. This will give a direct indication of the possible power density of the motor drive, making it possible to compare with existing technologies.

The assumptions made with the thermal resistances as a straight cut through the layers give a deviation in terms of the actual thermal resistance, and is somehow a worst-case calculation. The thermal spreading on the IMS will definitely improve the thermal management and therefore an analysis and calculation of the thermal spreading in the IMS and conventional FR4 PCB could be interesting. Also to highlight the advantages IMS has in terms of avoiding hotspots being generated compared to conventional PCBs.

Lastly, the observations of low conduction losses and high switching losses have initiated reflection around investigating different semiconductor R_{DS_on} values. For example, testing a 70mΩ resistance GaN semiconductor instead will reduce the cost, but could also have reduced switching losses and since the conduction losses are significantly low, this increase in R_{DS_on} will not affect the overall power rating. This could also show the differences in efficiency between switching losses and conduction losses, as low-power applications will be more affected by the switching losses than higher-power applications.

To summarise the investigations have created a large ground for reflection around IMS technology as well as WBG technology. New design iterations to optimize the converter design would be applicable to increase the advantages of IMS and GaN technology, through reducing inductive and capacitive effects with FEM analysis.

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