MW-Level Power Converter Solutions for Power-to-X Application

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Abstract:

In an effort to increase sustainable energy, there is a rising trend in the implementation of renewable energy applications. However, without storage, large amounts of energy are lost during the 'off-peak' demand periods. Therefore, a highly promising solution to this issue is the use of Power-to-X systems, whereby excess energy during off-peak periods is stored in the form of gases, which can be used to provide energy in accordance with power demand levels. High current power electronic rectifiers play a major role in this process, as they convert the AC power from the grid to DC Power, which is necessary to operate Power-to-X systems. In this thesis, the analysis of high current rectifier topologies will be carried out to derive the most promising topologies that are suitable for industrial use. Power quality, cost, efficiency, and reliability are key performance indicators that will be considered. Four state-of-the-art topologies will be analysed, as well as a novel topology in order to determine the most optimal candidates for the industry.

Preface

This report has been developed as a completion of the Master's Thesis of project group APEL-4 during the 4th semester of MSc in Advanced Power Electronics at Aalborg University. This project was carried out in collaboration with Haldor Topsøe.

The design, analysis, and comparison of several state of art and a novel Power-to-X converter topologies is carried out and elucidated in this project. Thorough and extensive investigation was carried out during this work which, allowed us to reach a successful conclusion.

We would like to thank our supervisors Pooya Davari, Amin Hajizadeh, Mengxing Chen and Shan He for their great support and invaluable inputs throughout the entirety of the project. Fortunately, both Menxing Chen & Shan He were always available to offer their guidance & counsel for which we are extremely grateful.

Finally, we would like to thank our families and friends for their everlasting love & support, especially during our studies at Aalborg University.

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Table of acronyms

AC	Alternating Current
AFE	Active Front End
APF	Active Power Filter
DAB	Dual Active Bridge
DC	Direct Current
DR	Diode Rectifier
FFT	Fast Fourier Transform
HFT	High Frequency Transformer
IGBT	Insulated Gate Bipolar Transistor
LFT	Line Frequency Transformer
MFT	Medium Frequency Transformer
MMR	Modular Multicell Rectifier
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PI	Proportional and Integral
PF	Power Factor
PLL	Phase Locked Loop
P2X	Power to X
RMS	Root Mean Square
SCR	Silicon Controlled Rectifier
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
12-TR	12 Pulse Thyristor Rectifier
12-DRMC	12 Pulse Diode Rectifier with Multi-phase Chopper
12-TRASPF	12 Pulse Thyristor Rectifier with Active Shunt Power Filter

CONTENTS

1 INTRODUCTION

1.1 Background and Motivation

Today's renewable energy technology is striving to improve in order to meet the ever growing energy demands and simultaneously reach the European ambitions of having zero carbon emission by 2050 [1]. Due to these ambitions, new technologies are emerging in an effort to reduce the effects of fossil fuel use on the environment and meet the global energy crisis. In Denmark, nearly all hydrogen production is based on fossil fuels like coal and natural gas. In an effort to eliminate the use of fossil fuels, the government of Denmark is encouraging and promoting Power-to-X (P2X). Denmark views the P2X as a possible new green utility sector, with the objectives of tackling climate change and reducing emissions from transport and the industrial sector and fulfilling the energy requirements as there is a need of generating new capacity [2], [3], [4]. One way to eliminate the fossil fuel is the use of renewable energy sources such as solar, wind, bio, and hydro energy. Renewable energy sources are an alternative to the fossil fuels as they produce clean electricity. However, these energy sources can have an unpredictable nature, causing intermittent production of electricity. Without storage, large amounts of energy are lost during 'off-peak' periods, due to low demand as seen in **Figure 1**. Therefore, it is necessary to find an approach to make use of the excess energy during these 'off-peak' periods [5].

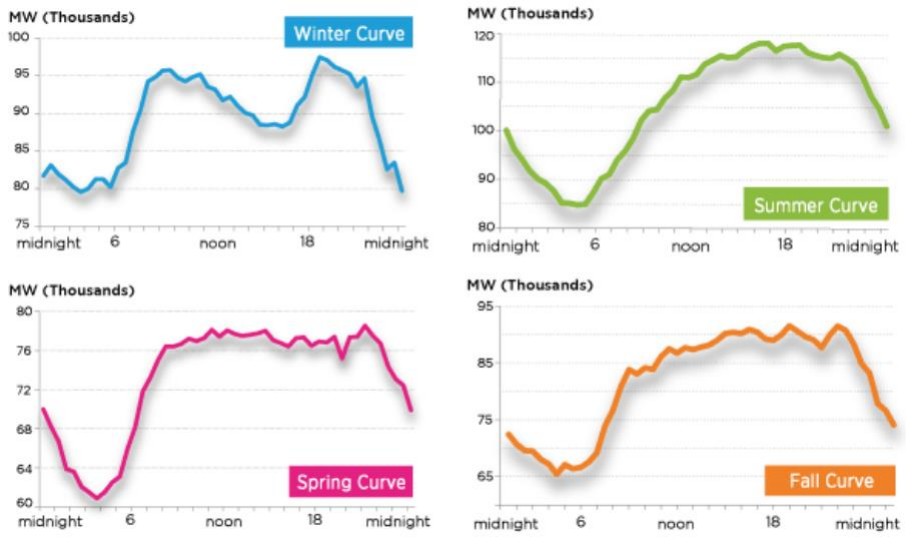

Figure 1: "Off-peak" period power consumption during different seasons [6].

A new strategy is to use the excess energy from renewable energy sources to convert water into hydrogen or hydrogen-based gases; this process is known as Power-2-X (P2X). The core technology behind P2X is called electrolysis, which uses electricity to split water into oxygen and hydrogen. This process typically involves a number of electricity conversions, energy storage, and reconversion pathways that use surplus power produced by renewable energy sources to produce Hydrogen and its by-products.

In order to store energy produced by electricity, usually batteries are utilized. However, the electricity can also be stored by converting it into Hydrogen by the help of P2X. The value of storage is also given by its potential to decouple generation from demand, thus facilitating the integration of high shares of variable renewable energy (VRE) and avoiding curtailment of the generation surplus. A study has shown that between 2017-2025, by using P2X it would be possible to provide sufficient electricity for up to 187.000 homes [2].

Hydrogen, which is considered 'green' when produced with renewable energy, can subsequently be used for industrial purposes or as a fuel directly. It can also be used as a building block for producing a wide range of other fuels, chemicals, and materials. **Figure 2** illustrates the cycle of P2X.

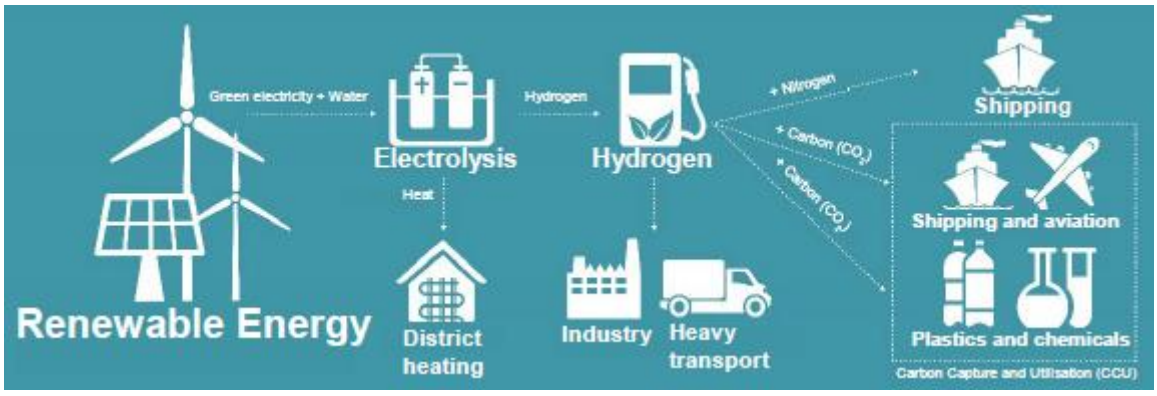

Figure 2: P2X process from renewable to heat and hydrogen [3].

P2X technologies make it plausible to use renewable energy to produce fuels instead of producing them from fossil sources. Hydrogen can be combined with nitrogen to form ammonia. The resulting ammonia could be used as fuel in diesel-like engines in the future or for producing fertilizers and other chemicals. It can also be used to produce methane, methanol, gasoline, diesel, aviation fuel and plastics with the same properties as the fossil-based products. Hence, P2X has a huge potential

to reduce the CO_2 emissions and aid in tackling the challenge of 'Climate Change' and consequently fulfilling the growing energy demands.

The converted electrical energy from the renewable energy sources to hydrogen enables a more controlled output of energy. Hence the P2X plant increases the stability of the grid. Another advantage is that some of these hydrogen-based products consist of carbon, which is extracted from bioenergy plants and is therefore considered as 'green carbon'. The way of extracting the green carbon is called 'Carbon Capture', thereby reducing the carbon emission in this process [5].

However, as new emerging technologies arise, so do the challenges that accompany them. For P2X the challenges are usually related to the power electronic converters (PECs) and corresponding topologies. The PECs will convert the AC power produced by the grid or other renewable energy sources into DC power on the output. Given the challenges involving the PECs, this project will focus on power electronic converter topologies and evaluate the performance of these topologies based on criteria such as power quality, robustness, and efficiency among other aspects investigated. A comparison of the different converter topologies will determine the most promising topologies and hence examine the potential solutions available in today's market.

The aforementioned criteria is important when evaluating the performance of power electronic converter topologies. From an industrial point of view, aspects like cost, reliability and footprint are the decisive factors for implementing a topology. However, the topologies must also be able to meet certain grid codes and standards in order for its implementation to be realized. Hence the most optimal system will often be a compromise between technical and cost criteria.

Reliability, which is a very broad and emerging field, will be briefly discussed due to its importance but will not be investigated in detail. The degree of reliability of each topology will be based on the arrangement and setup of the topology while taking the amount of semiconductor devices into consideration.

Similarly, the footprint of each topology will be briefly touched. The sizes of components could change for each topology, due to the ratings or arrangement in the system. Apart from the semiconductor devices, the sizes of large-scale components, such as transformers may vary depending on the manufacturer.

Cost is usually the most important aspect for any system from an industrial application point of view. Therefore, an assessment of the cost is essential when designing a system. However, this project will focus mostly on the technical aspect, while the cost will be briefly mentioned.

However, as already discussed, from an industrial & business point of view, cost, reliability, and footprint are extremely important factors, which need to be considered for the realization of the system.

1.2 Power to X applications

There are four state-of the art power converter topologies, which will be analysed throughout this thesis, in order to provide the required power output of 1 MW for a P2X application. These topologies are briefly outlined below, including their key features, as well as their advantages and disadvantages. In addition, a novel topology known as Modular Multicell Rectifier (MMR) will be investigated.

12-Pulse Thyristor Rectifier (12-TR)

The 12-TR is one of the most widely known converters used in P2X applications. It consists of a dual thyristor bridge, where the firing angle of the thyristors controls the output power. A larger output firing angle corresponds to a smaller output power with increased harmonic levels and vice versa. The 12-TR has the advantages of smaller footprint, high reliability & efficiency due to its simplistic design [7].

12-Pulse Diode Rectifier with Multi-Phase Chopper (12-DRMC)

The 12-DRMC comprises of a dual diode bridge with a multi-phase chopper, consisting of IGBTs with free-wheeling diodes. By varying the duty cycle of the chopper, the DC output power can be varied accordingly. Its main advantage is that it is fairly simple and can maintain a low current distortion at variable loads [7].

12-Pulse Thyristor Rectifier with Active Shunt Power Filter (12-TRASPF)

This is a topology based on the 12-TR model with the addition of an active power filter (APF) consisting of a 6-pulse IGBT bridge. The APF is in shunt with the 12-TR and can inject reactive power

into the system thus increasing the power factor on the grid side significantly. However, this topology has a large footprint, due to the use of an additional transformer on the active filter side.

Active Front End Rectifier (AFE)

The AFE generally comprises of only dual IGBT bridges or dual IGBT bridges with an additional chopper. For this project the latter option is implemented, in order to obtain the best results of the topology. The main advantage of this topology is that it can deliver high power quality without the use of active or passive filters, which reduces its footprint while remaining robust to the external changes [7].

Modular Multicell Rectifier (MMR)

The modular multicell rectifier is a novel approach. Its main advantage is the modular design which increases its reliability compared to the previously mentioned topologies and its use of high frequency transformer (HFT) significantly reduces its footprint in contrast to the Low Frequency Transformer (LFT) used in the previous topologies. However, the modular design increases its complexity [7].

1.3 Power quality

The aim with regards to the designing of all the topologies is to ensure that they follow the relevant grid codes and standards, thereby maintaining acceptable power quality, while not injecting significant harmonics into the grid. All the PECs are non-linear in nature and therefore inject harmonics into the system and lower the power factor, hence reducing the power quality of the grid [8]. As a consequence, a major aspect of this project involves the methods used in order to mitigate these undesired effects of power converters. To tackle this, the active and passive filters are employed to supress the harmonics so that the limits set by the grid codes and standards are met. Furthermore, in attempts to improve the power quality, challenges arise in terms of footprint and cost.

1.3.1 Power Quality Standards

Consumption plants such as a P2X application, must be designed for the normal operation requirements while also able to withstand external disturbances. The Distributed System Operator (DSO) sets the requirements for normal operation, to ensure stability of the grid. A consumption

plant must abide by these regulations in order to ensure its safe operation. Normal operation is defined when the grid follows the nominal voltage (U_C) with the allowed deviations of ±10% and the frequency in the range of 49-51 Hz. Both nominal voltage and frequency are measured at PoC. The limits for voltage and frequency are set based on the predicted normal variation in the transmission and distribution grid [9].

Another limit for the consumption plant is regarding the power factor, which must be within the range of 0.95-1. However, this limit is a measurement which must be conducted over a period of 15 minutes; hence it will not be feasible to follow this particular regulation very strictly [9]. In order to obtain the power factor for consumption plant, the following equations can be applied:

$$PF = \cos(\theta) = \frac{P}{S} \quad (1)$$

$$PF = \sin(\theta) = \frac{Q}{S} \quad (2)$$

Where $'P'$ denotes active power, $'Q'$ denotes reactive power, $'S'$ denotes apparent power & $'\theta'$ is the power factor angle.

Another aspect to the power factor, is the distortion power factor for non-linear loads, which is calculated as:

$$PF = \frac{Cos(\theta)}{\sqrt{1 + THD_I^2}} \quad (3)$$

Where THD_Idenotes the current THD & θ is the power factor angle. The distortion power factor utilizes the THD, as a tool to determine the power factor. This method is usually used in non-linear load systems [10].

1.3.2 Grid Voltage Variations

A system must be designed to be robust during voltage variations. These variations account for both the normal and abnormal operation, which can occur in the Danish distribution grid. The standard states that under normal operation the system must be able to handle a voltage variation of ±10%. If a severe voltage dip occurs, the system is allowed to decouple from the grid for a short period of time. The period of decoupling must be arranged between the plant operator and related grid operator [9].

Further detailed requirements are covered in DS/EN 61000-6, which are not available through the Aalborg university channels.

Furthermore, it is recommended that the plant can uphold normal operation during voltage dips. This is however a matter of the plant's robustness and may vary between different plants.

1.3.3 Harmonic Distortion

One of the key issues of power quality is harmonic distortion. Harmonic distortion refers to the presence of harmonic orders, which are integer multiples of the fundamental frequency. Harmonics cause signal distortion and reduce the PF of the system; hence they are undesired in a system. 'Dansk energi' accounts for the harmonic orders ranging from the 2nd to the 40th, as these are most dominant and hence create larger signal distortion. However, in theory a signal would include an infinite number of harmonics.

If a signal is symmetrical, implying that the signal's positive and negative half-cycles are symmetrical about the x-axis, only odd harmonics will appear in the signal (3rd, 5th, 7th..37th of the fundamental frequency) [9], [11].

The harmonic distortion needs to be analysed in certain ways in order to ensure safe operation of the system. Many other requirements must be met to ensure safe operation for any system, one of the most important requirements being the total harmonic distortion (THD). The THD is a measurement of the total amount of harmonic distortion present in a system. **Eq. 4** describes the THD calculation of the current:

$$THD_I = \sqrt{\sum_{n=2}^{N} \left(\frac{I_n}{I_1}\right)} \tag{4}$$

Where 'I_n' is the nth order current, with 'I_1' being the first order, commonly referred to as the fundamental. As is the case with THD, the Total Demand Distortion (TDD) is also a measurement of the total distortion in the system. However, the TDD is calculated based on a percentage of the maximum demand current in the system instead of a percentage of the fundamental. When the system is operating at full load, the TDD and THD are equal. Hence when in partial load, the TDD and THD are not equal; TDD being the larger of the two [12].

The IEEE 519 standards can be used to determine the set limit of harmonic distortion for current. However, the IEEE 519 standards do not indicate the distortion as THD but as TDD, with the limit set to 5% [13]. However, the TDD limit depends on the short circuit current at point of common coupling (PCC), hence the ratings of a system. A calculation of the TDD is seen in **Eq. 5** which is difficult to measure due to the measurement range of 15 minutes [14].

$$TDD_i = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + \cdots}}{I_L} \tag{5}$$

Where I_L is the maximum demanded load current.

It is possible to verify the distortion limits of each topology stated by IEEE 519, without measuring the TDD. In order to verify that the TDD demands are met, the THD measurement can be used. From **Eq. 5** it can be deduced that THD measurement will be sufficient, since $I_L > I_1$. Hence with THD measurements within the limits of Error! Reference source not found. then by definition the r equirement for TDD will be met [14].

Besides having an overall requirement of TDD, which as explained measures the overall disturbance of the system, there also exist requirements for each individual order of harmonics. The requirements depend on the system's voltage level at Point of Common Coupling (PCC). For a system with a voltage level of 1-69 kV, the following demands must be met [13]:

Table 1: Current Harmonic Limits for consumption plants (≤69)

$\frac{I_{SC}}{I_L}$	**< 11**	**11 ≤ h ≤ 17**	**17 ≤ h ≤ 23**	**23 ≤ h ≤ 35**	**35 ≤ h**	**TDD**
SCR < 20	4.0	2.0	1.5	0.6	0.3	5.0%
Adjusted for multiplying factor	5.66	2.82	2.12	0.85	0.42	-

However, when lower order harmonics are reduced, it is recommended to increase the values in **Table 1**. The increase depends upon the number of pulses used in the system, determined by the multiplier calculated by using multiplying factor (*p*), which is seen in **Eq. 6**:

$$multiplier = \sqrt{\frac{p}{6}} \tag{6}$$

Hence for a 12-pulse system ($p = 12$), it will be possible to increase the values by a factor of 1.414, thereby adjusting the table limits to what is seen in the final row of **Table 1**.

Figure 3(a) shows the grid voltage and current waveforms for a 12-pulse passive rectifier. The grid voltage as expected is purely sinusoidal; however, the current is distorted due to the presence of the harmonics. Furthermore, the voltage and the current waveforms are slightly out of phase. **Figure 3**(b) shows the same waveforms after a passive filter has been implemented, the current waveform quality improves significantly both in terms of THD and power factor. Now the current waveform is much more sinusoidal with less distortions while being in phase with the voltage.

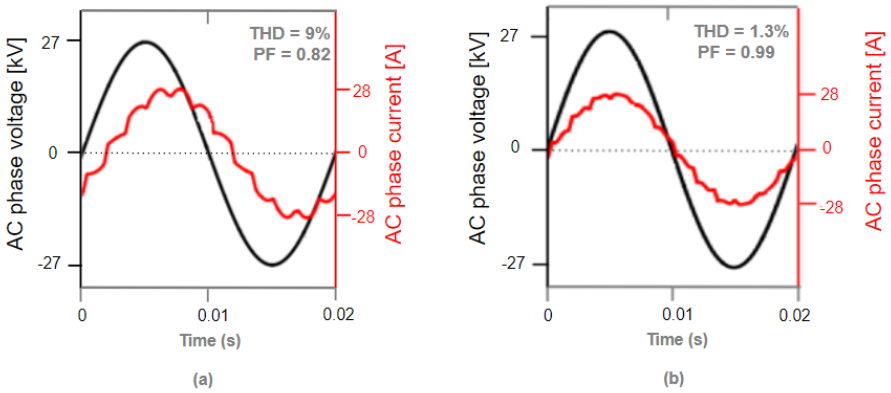

Figure 3: Grid Voltage and Current waveforms when a passive 12-pulse rectifier is connected to the grid (a) without passive harmonic filter (b) with passive harmonic filter

1.4 System Specifications

Table 2 shows the power system specifications for the P2X system. All the topologies follow these specifications to be compared on the same grade.

Table 2: System Specifications for the P2X system

Variables	Values
Grid Voltage	33 kV (Line-to-line, RMS)
Grid frequency	50 Hz
DC Output voltage	1 kV
DC Output current	1 kA
DC Output power	1 MW
Load Resistor	1 Ohm

1.5 Scope of the Project

The aim of the project is to investigate the various aspects of the four state-of-the-art topologies and the novel MMR topology to outline their overall performance. The analysis is performed through extensive simulations, investigating their performance under variable loads, unbalanced loads, and their efficiencies. Further aspects of industrial & business interest will be briefly looked into. Emphasis is given to the technical aspect, as concrete results are obtained from the simulation tests carried out in PLECS platform for the electrical simulations.

1.5.1 Problem Statement

The problem statement involves presenting the most superior power converter architecture and making a preliminary design for the MW-level power converter for Power-to-X application.

1.5.2 Objectives

Simulate four state-of-the-art converter topologies to obtain 1MW DC output and the control configuration related to each one.

a) Design and reproduce four state-of-the-art topologies in simulation tool PLECS.
b) Evaluate performance based on simulation tests for harmonic analysis, unbalanced grid conditions, variable loads, and efficiency.
c) Simulate a novel topology and carry out an identical investigation as conducted with the state-of-the-art topologies in order to evaluate its performance.
d) Analyse results based on the simulations and draw conclusions on overall topology performances.
e) Estimate physical footprint aspect of the topologies for the purpose of comparison.

1.6 Limitations

The limitations & constraints regarding this thesis are as follows:

- The DC output load in all the five simulated topologies has been modelled as a resistor, as per the specification of the P2X application by the company in collaboration with this project, Haldor Topsøe.
- The winding resistance and leakage inductance of the transformer are implemented with ideal values, during the Harmonic Analysis, Unbalanced Grid, and Load Variation tests.

- The cost aspect is mentioned only comparatively between the topologies. Due to lack of information from transformer manufacturer and time constraints on the project, a detailed cost analysis was omitted.
- Due to the time constraints, a reliability analysis of the semi-conductors has not been conducted. However, the fundamental principles of semi-conductor reliability will be briefly discussed, due to its importance.
- For the novel topology Modular Multicell Rectifier, the current sharing between cells was omitted due to lack of literature available on how to implement the specific control method for this topology.

1.7 Thesis Outline

The thesis is outlined as follows:

Chapter 2 presents the background required for the four state-of-the-art topologies. The design and control of the topologies will be illustrated and all the necessary electrical conditions that each of the topologies must follow, will be explained. Requirements for footprint, reliability and cost are also briefly investigated to stress the importance of these criteria as well. The simulation testing methods are also described in this chapter.

Chapter 3 investigates four state-of-the-art topologies and evaluates their performances based on extensive simulations & tests. Tests such as harmonic analysis, unbalanced grid, load variation, and efficiency test will all highlight different performance aspects of the topologies.

Chapter 4 introduces a novel topology, the Modular Multicell Rectifier and investigates this topology based on the tests performed in Chapter 3. The design of this topology will be presented followed by the results obtained during the simulations.

Chapter 5 documents the results from all the simulations and compares them in order to indicate the advantages and disadvantages of each topology. It further discusses the most optimal topology based on the comparison data.

Chapter 6 will present the conclusions obtained from this project. Future work will also be discussed in this chapter.

2 HIGH CURRENT RECTIFIERS - OPERATION AND CONTROL

In this section, the various converter topologies that are investigated in the thesis will be described in detail, including the utilized control scheme for each topology. Furthermore, the methods of harmonic compensation for the topologies will be illustrated. Next, the topics of reliability will be discussed, as well as physical footprint, with regards to the topologies. Finally, the background of the methods used in order to test and obtain conclusions from the topologies will be discussed in detail.

2.1 Converter topologies

In this section of the architectures of the four state-of-the-art topologies will be illustrated. The topologies evaluated are 12-Pulse Thyristor Rectifier (12-TR), 12-Pulse Diode Rectifier with Multi-Phase Chopper (12-DRMC), the 12-Pulse Thyristor Rectifier with Active Shunt Power Filter (12-TRASPF), and Active Front End (AFE). Since the aforementioned topologies are already in use in the industry, implemented in the existing plants, they will be used as benchmarking for the newly emerging Modular Multicell Rectifier (MMR) which is a novelty [15].

2.1.1 12-pulse – Thyristor Rectifier (12-TR)

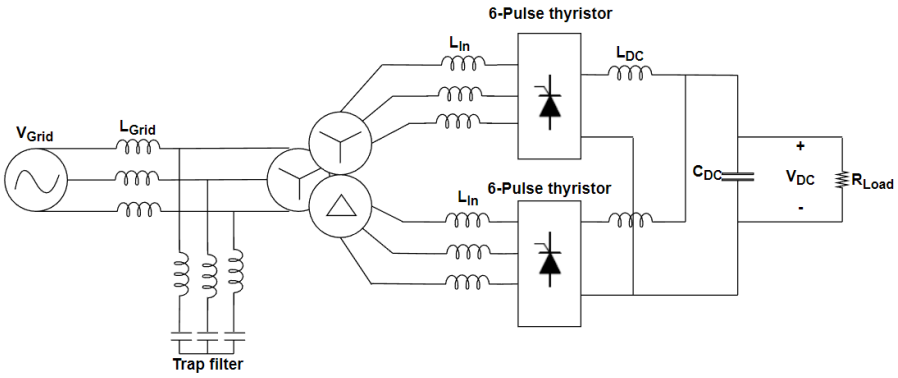

Figure 4: 12-TR model as a single line diagram.

A 12-pulse Thyristor Rectifier is illustrated in **Figure 4**. The 12-TR is a rectifier, hence converting the AC input from the grid to DC output, which is used to deliver DC power to a P2X application. For the topology to meet the standards described in **Section 1.3**, it needs to be regulated by a controller. Since two 6-pulse thyristor rectifiers are used in shunt, it is necessary to ensure the rectifiers are synchronized; this is handled by the PLL. The output signal from the PLL is fed into a 6-pulse

generator, which enables control signals to be sent to the two 6-pulse thyristor rectifiers (TR). A star-delta-star connected LFT, is placed between the grid and the two 6-pulse TR. The transformer receives a 33 kV (line-to-line, RMS) voltage from the grid on its primary windings. The transformer then steps down this voltage to 900 V (line-to-line, RMS) on each of the two secondary windings. **Figure 5** visually describes the control system for this topology.

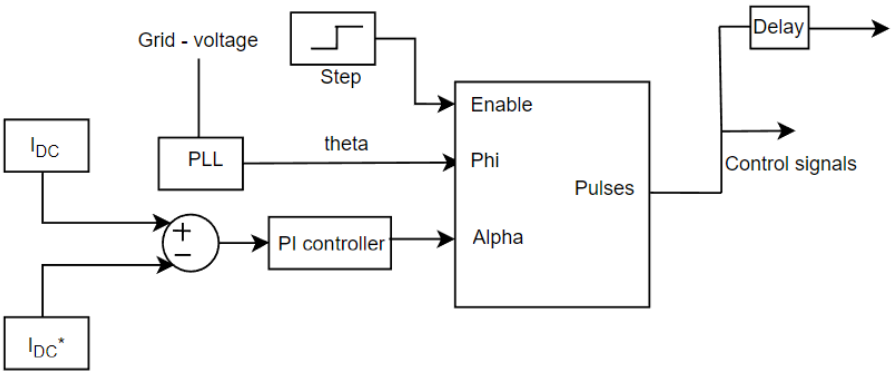

Figure 5: Control diagram of the 12-TR

The secondary side of the LFT is connected to the dual 6-pulse thyristor rectifier bridge. Due to the delta-star coupling of the transformer's secondary side, the phase lag in the delta coupling of the transformer needs to be adjusted. The adjustment is achieved by connecting a pulse delay to 6-pulse generator, controlling the delta coupling. The pulse delay needs a certain delay time, which must correspond to the phase shift of 30 degrees. A simple calculation can be used in order to find the necessary time delay, as explained by **eq. 7** [16]**:**

$$T_{delay} = \frac{\varphi}{360 * f} \tag{7}$$

Where 'T_{delay}' is the time delay, 'φ' is the phase delay angle and 'f' is the operating frequency.

To reduce harmonics in the system, it is possible to increase the number of thyristor rectifiers to 18 and 24. The increase will however lead to higher cost, footprint, and lower reliability, due to the increase of components. The transformer in conjunction with the 12-pulse thyristor setup will eliminate the lower order harmonics, specifically the 5^{th} and 7^{th} order harmonics [17].

The value of DC current consumed by the load of the P2X application can be adjusted by the firing angle (α) of the thyristors. A large firing angle leads to more distortion and decreases the power

factor, which are undesirable traits for the system. However, if lower power is required in the system, it is possible to increase the firing angle at the expense of the power factor, thus decreasing the power quality.

To improve the power quality, a filter can be added thus meeting the grid standards. From **Figure 4** it can be seen that the topology includes a passive 'trap filter' on the grid side, which improves the power quality hence meeting the previously mentioned grid requirements [7]. The passive filter improves the power quality by decreasing the THD by filtering the undesired harmonic to which it is tuned [18].

2.1.2 12-pulse Diode Rectifier with Multi-Phase Chopper (12-DRMC)

Another well-known topology is 12- Pulse Diode Rectifier with a Multi-Phase Chopper, also referred to as 12-DRMC. The topology is illustrated in **Figure 6**.

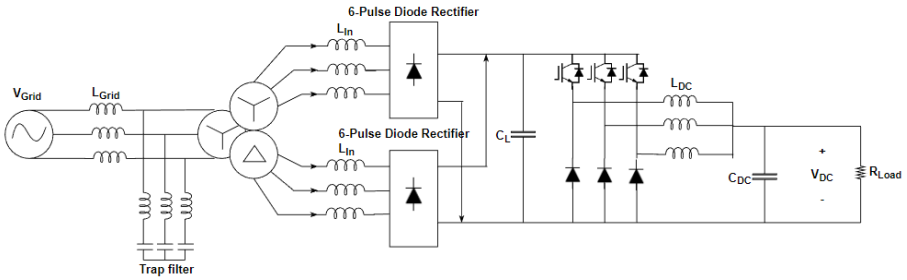

Figure 6: 12-Pulse Diode Rectifier with Multi-phase Chopper

This topology essentially operates in two stages, one being the rectifier stage where the AC input is being converted to DC. In this stage a 12-Pulse diode rectifier has been implemented which converts the AC to DC, as seen in **Figure 7**. The diode-rectifier receives the AC supply from the 12-pulse transformer and converts it to DC to be used in the next stage.

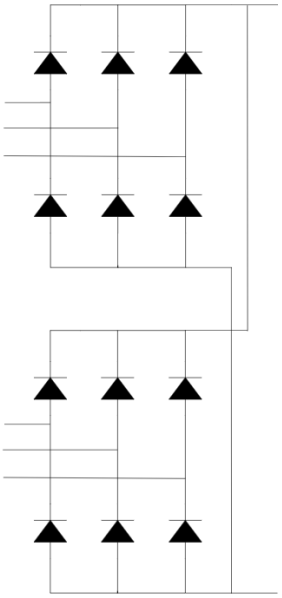

Figure 7: Rectifier stage, AC is converted to DC

For the next stage a DC/DC converter is employed. A chopper will be used for this conversion. The chopper receives the DC output voltage from the rectifier (AC/DC Stage) and steps down the voltage to obtain the desired value as output for the load. A buck converter has been used as a chopper, which is implemented by the Silicon (Si) IGBTs with freewheeling diodes. The buck converters are arranged in an interleaved manner as illustrated in **Figure 9** to attenuate the current ripple on the DC output, where the P2X load is located. These buck converters are controlled by PI controllers to obtain the desired output as shown in **Figure 8.**

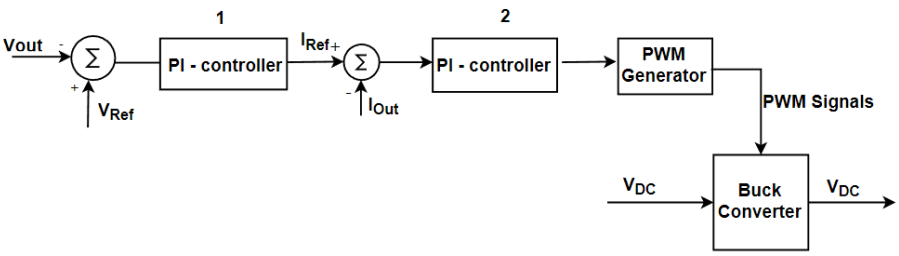

Figure 8: Control Diagram for Buck Converter

The control algorithm consists of a voltage compensator (PI Control) and the current compensator (PI Control) to ensure that the required levels of voltages and currents are transferred across the load and hence the correct power level is supplied across the P2X plant.

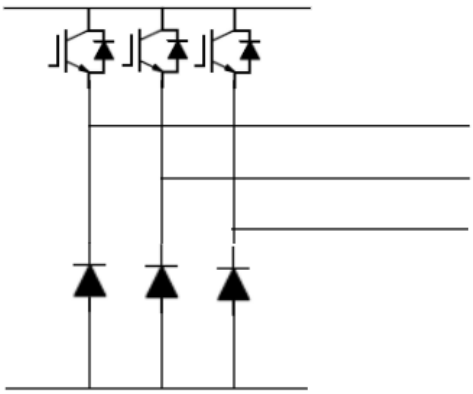

Figure 9: Interleaved Buck Converter Stage

2.1.3 12-pulse Thyristor Rectifier With Active Shunt Power Filter (12-TRASPF)

The 12-Pulse Thyristor Rectifier with Active Shunt Power Filter (12-TRASPF) uses an active filter combination, consisting of a 6-pulse IGBT bridge, each IGBT connected in antiparallel with a free-wheeling diode as seen in **Figure 10**. A shunt connected active power filter (APF) is used on the grid side, increasing the overall power quality. A major advantage of this topology includes reactive power compensation through the use of the active filter, which increases the power factor value, while THD is reduced due to the resonant controlled filter [18], [19]. Similar to the 12-TR topology, the 12-TRASPF utilizes Silicon Controlled Rectifiers (SCRs), so that the firing angle of the thyristors can be adjusted, according to the power application required. A 'star-to-star' transformer is used in shunt, in order to step down the grid voltage to a lower value, in this case 400V, as to not exceed the voltage ratings of the IGBTs used in the APF. [19].

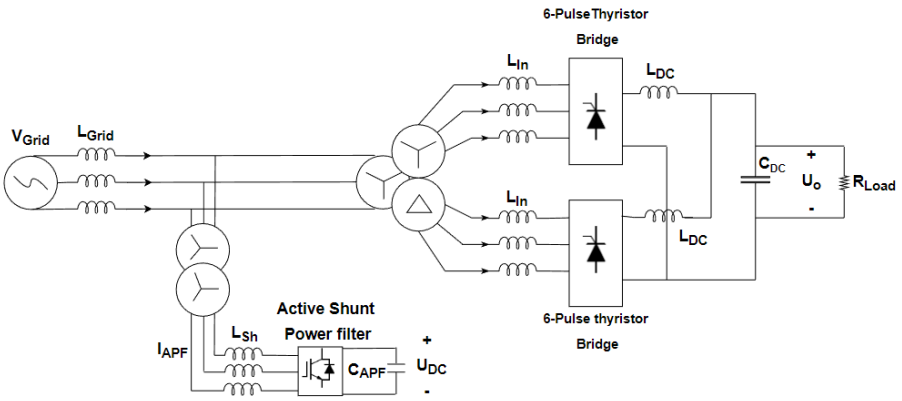

Figure 10: 12-TRASPF Hybrid Filter Topology

The active shunt power filter is shown in detail in **Figure 11**. The direction of the arrows indicates the direction of the flow of the reactive power, during the reactive power compensation that is required for the non-linear load, which for the case of APF is the 12-TR.

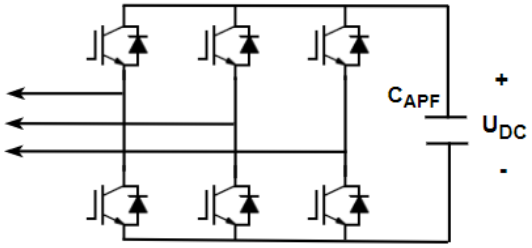

Figure 11: Active Power Filter

2.1.3.1 Hybrid Filter

An active filter can be further enhanced by adding a passive filter to it, typically in either shunt or in series connection. Filters consisting of both an active and passive filter are called as hybrid filters. The advantage of the hybrid filter is that it lowers the overall cost by adding the passive filter to adjust for the higher ratings. As a higher rating for active power filters is required for operation at higher firing angles, the cost of the APFs increases. Therefore, passive filters are introduced to increase harmonic compensation, while APFs compensate for reactive power [18].

2.1.3.2 Harmonic Compensation via Resonant Controllers

However, another method of harmonic compensation is via the use of a resonant (R) controller. The resonant controller tuned to the frequencies of the $12n \pm 1^{th}$ order harmonics, where n is a positive integer attenuates these harmonics, which originate from the 12-TR [20], [21]. The resonant controllers used to eliminate these harmonics are essentially second order filters and their advantage over the trap filter is the physical footprint, as no physical components such as capacitors, resistors and inductors are required. Therefore, resonant controllers can decrease the THD of the grid, without additional physical footprint for every harmonic that requires compensation.

2.1.3.3 Control of 12-TRASPF

To control the APF, an inner current controller loop is required in order to provide the reference voltage that will be fed into the gate of the IGBTs of the APF. The control scheme can be seen in **Figure 12**. Park's transformations are performed on the three-phase grid current so that the synchronous 'dq' reference frame can be achieved. The grid voltage signal is fed into the PLL, in

order to obtain the angle 'θ' and in this way achieve synchronization with the grid. The active 'd' and reactive 'q' components are then passed into the resonant (R) controllers respectively in order for the aforementioned harmonics to be attenuated.

The reactive power compensation is achieved by controlling the 'd' and 'q' components of the current from the APF (I_{APF}). An outer voltage loop is used to provide a reference of 'zero' for the 'd' component of the APF current (I_d*), as only reactive power should be provided by the APF. This is achieved by varying the reactive component of the APF current (I_q*). Once, the inverse Park transformation block is complete, the output of the transformation then determines the voltage reference of the active power filter. After PWM is applied to the output, the reference signal is fed into the control gates of the APF's IGBTs, thus enabling both harmonic and reactive power compensation.

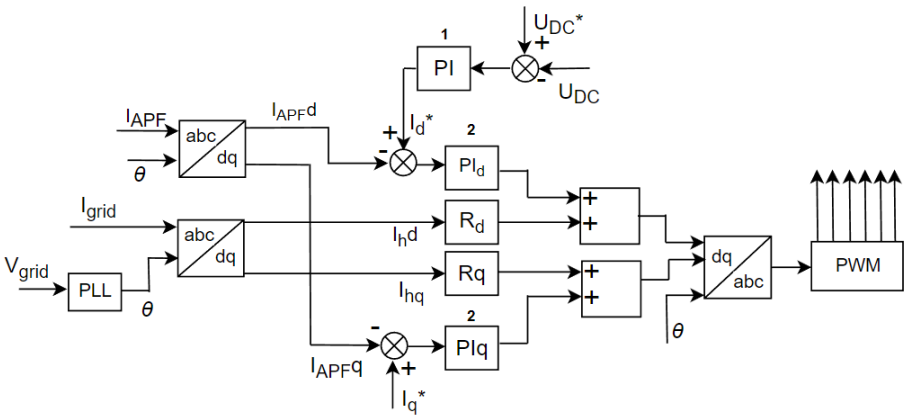

Figure 12: Control Scheme of 12-TRASPF topology

2.1.4 Active Front End – B6 + Chopper

There are several advantages of the conventional diode and thyristor rectifiers, such as low cost, high reliability, and efficiency due to their simplistic design. However, these advantages usually come with the drawbacks of lower power quality, hence necessity of passive and active filters. The high harmonic currents decrease the performance of the converters, while the filters increase the complexity, cost & footprint. The Active Front End (AFE) rectifier as illustrated in **Figure 13**, utilizes a similar overall setup, as presented in the previous topologies. However, due to the active rectifiers, the need for filters becomes redundant [22].

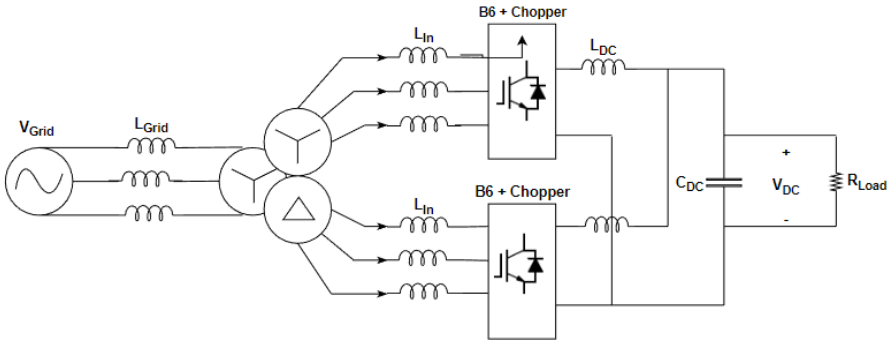

Figure 13: Active Front End Rectifier, with B6+Chopper.

The AFE topology can be classified as a controlled AC/DC converter, since the SCR and DRs are replaced with insulated gate bipolar transistors (IGBTs). These IGBTs are used in three half bridge rectifiers, each of which consists of 2 IGBTs with a free-wheeling diode (IGBT-D). Since the topology uses IGBTs instead of SCRs, a synchronous reference frame control strategy is used in order to control the output DC current of the B6. Furthermore, for a DC/DC converter, a 'chopper' is implemented in this topology. The chopper consists of 3 IGBT-Ds and 3 diodes. The combination of B6 and Chopper is shown in **Figure 14** [23].

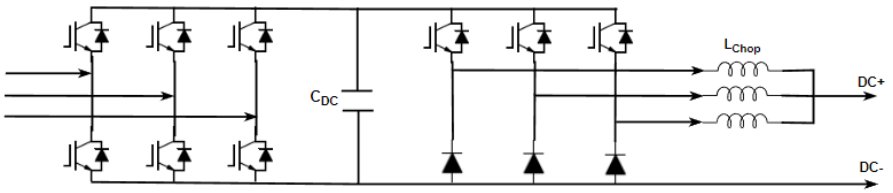

Figure 14: B6+Chopper.

The addition of the chopper circuit to the topology improves the controllability of the DC voltage. The addition of the chopper allows static power electronic devices to convert variable input DC voltage to a fixed output DC voltage. The chopper circuit operates in a similar manner to a high-speed switch, thereby chopping the voltage and allowing for increase or decrease of the output DC voltage as required [24].

2.1.4.1 Control of AFE with B6+Chopper

The control of AFE needs two control loops, one for 'B6' and another for the 'Chopper'. For the B6 control loop, the synchronous reference frame is applied. This method is also referred to as Park's transformation. Here, the grid current and voltage waveform are referred to a rotating reference

frame ‘abc’, which rotates synchronously with the grid voltage. Subsequently, the AC variables are transformed to DC variables, thus allowing for control in the ‘dq’ reference frame and ensuring the DC-link voltage is controlled according to the desired output power [15]. A control diagram depicting the described control method is seen in **Figure 15**.

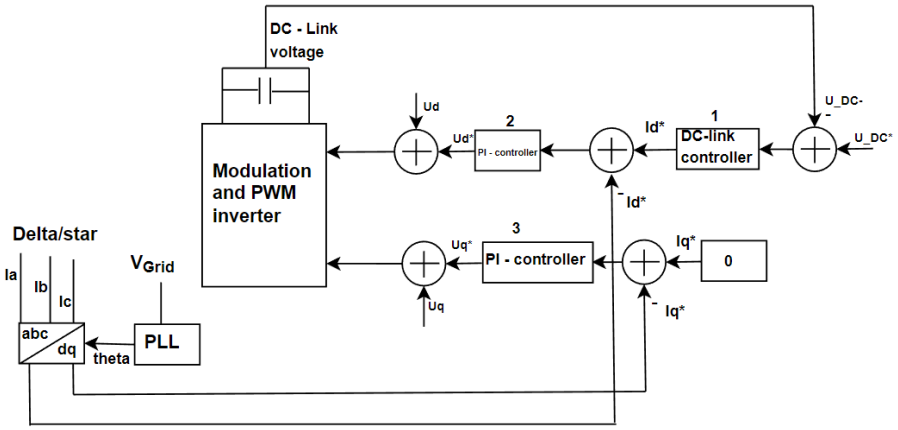

Figure 15: Control diagram for the AFE topology

Since the two secondary windings of the transformer are coupled in a star-delta connection, the phase-lag between the secondary windings must be considered when the control loops are designed for the delta connection. To ensure that no phase difference is present in the system, two separate phase-locked-loops (PLL) are applied to the system, hence decoupling the PLL of the star and the delta windings. In order to account for the 30^{o} phase difference between the star and delta connections, a transport delay with similar delay to the 12-TR model is added. Hence, ensuring that there will be no phase-shift between the star and delta windings on the secondary side of the transformer.

Since two PLLs were implemented, two separate current control loops were necessary. The PLLs are used to ensure that the ‘dq’ reference frame, is synchronized with the grid side. The currents in the ‘dq’ reference frame are represented as ‘I_d’ and ‘I_q’, where ‘I_q’ is set to zero since the reactive power control is not required for this model. However, the active current reference ‘I_d*’ requires a reference input which is provided by the DC link controller, which compares the DC-link voltage to a reference and outputs the ‘I_d*’ as shown in **Figure 16**.

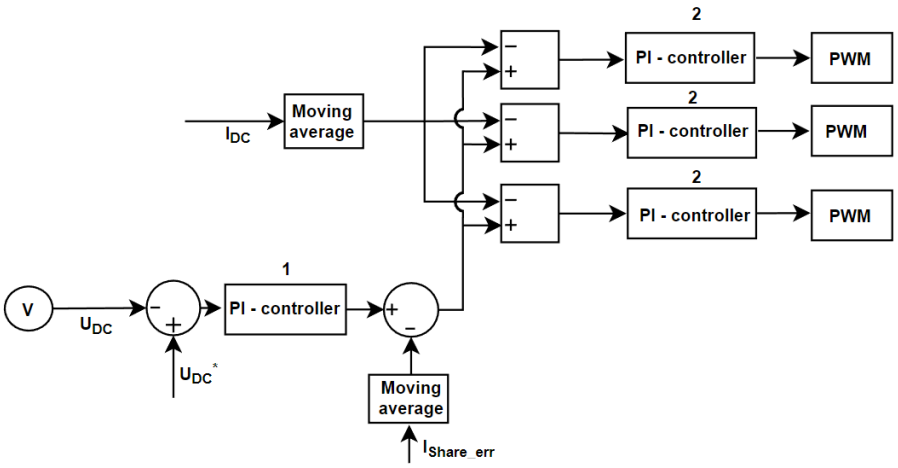

Figure 16: Control diagram for the DC/DC chopper circuit

Figure 16 illustrates the DC/DC chopper circuit. To control the chopper, feedback from the output DC voltage is fed to the chopper, hence regulating the system output. The 'step-down' chopper is implemented in this case which is controlled by pulse width modulation (PWM). The chopper is designed to buck down the 1200 V it receives as input to 1000 V output Hence the chopper is able to control the DC voltage obtained from the B6 rectifier [24].

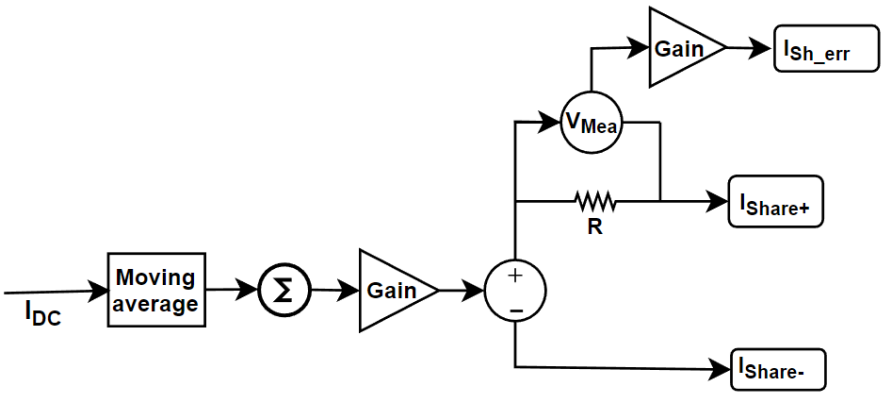

Figure 17: Control diagram for the current sharing.

Figure 17 illustrates the current sharing algorithm, which is implemented in the AFE model. The current sharing helps maintain high efficiency and reliability, when two or more modules are used in the system. The AFE has two modules and possibility of further addition if the system needs to be scaled up. The current sharing helps relieve some of the current stress produced by the switching devices and ensures equal amount of power is shared between each module [25].

2.2 Harmonic Compensation

2.2.1 Trap filter design

The trap filter falls in the category of the passive filter, which is a combination of resistors, capacitors, and inductors. These components are tuned to resonate at a specific frequency in order to suppress the presence of the corresponding harmonic, in this case the 11^{th} and 13^{th} harmonics. Two trap filters are used for each of the following topologies: 12-Pulse Thyristor Rectifier and 12-Pulse Diode Rectifier multi-phase chopper, as they use the 12-pulse converters producing the 11^{th} and the 13^{th} order harmonics among other 12n ± 1 harmonic orders[26].

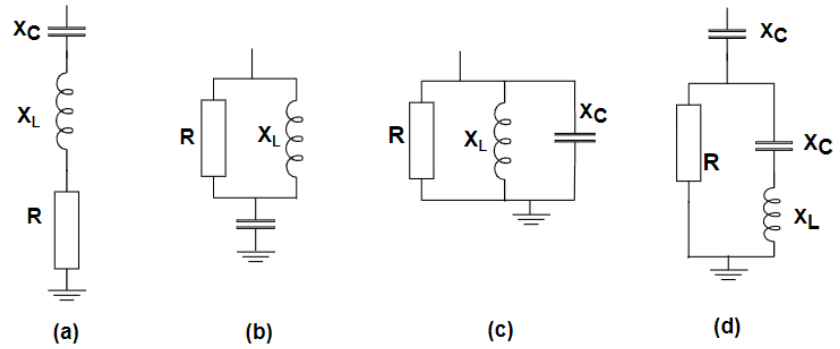

Figure 18: Series, high-pass, band-pass, C-type respectively

The passive filters have different types as shown in **Figure 18**. The trap filter required is a series filter, which is implemented in the project as shown in **Figure 18**(a). Designing the filter requires extensive information about the power system's characteristics, such as line-to-line voltage, fundamental frequency, system configuration, and impedance of the system. Furthermore, if the filter is intended to be realized, certain external factors need to be obtained, such as topology instalment location (indoor, outdoor, offshore etc.) and ambient temperature to ensure the filter is isolated correctly and follows the necessary regulations. However, since this project is only based on the simulations, the environmental factors will be disregarded [26].

When tuning the passive filter, it is recommended to tune the filter between 3-15% below the desired level. This ensures the harmonic content is sufficiently filtered, while allowing for possibly natural detuning. Natural detuning occurs due to the unavoidable changes the system will be

subject to, such as losses in the transformer, maintenance, equipment replacement, and temperature change in the system which will affect the capacitance in the filter.

The filters which will be used in the simulation models i.e., the trap filter will be tuned in order to suppress a single frequency. Therefore, the design is based on five parameters: the desired current harmonic order to be blocked (H), the capacitive reactive power provided (Q_C), the quality factor which defines the bandwidth of the filter (Q), the fundamental frequency of the system (f), and the voltage level of the system (V). **eq. 8-12** are derived on the basis on these variables [26].

$$C = \frac{Q_C}{2 * \pi * f * V^2} \tag{8}$$

$$X = \frac{1}{2 * \pi * f * H * C} = \sqrt{\frac{L}{C}} \tag{9}$$

$$L = \frac{X}{2 * H * f} \tag{10}$$

$$Q = \frac{2 * \pi * f * L}{R} \tag{11}$$

$$R = \frac{1}{2 * \pi * f * C} \tag{12}$$

These equations can be used in order to design the values for the series filters, consequently implemented in the simulations of the designed topologies. These values are determined by mathematical calculations in MATLAB and the bode diagrams are plotted to ensure that the value for the filters is designed to the correct frequencies.

Figure 19 depicts the bode plot of the designed filter for the 11th harmonic which operates at the frequency of 550 Hz. This filter supresses this unwanted component of the waveform. The transfer function of this filter is:

$$G_{11}(s) = \frac{(8.3*10^{-8})*s^2 + (4.4*10^{-7})*s + 1}{(8.8*10^{-7})*s} \quad (13)$$

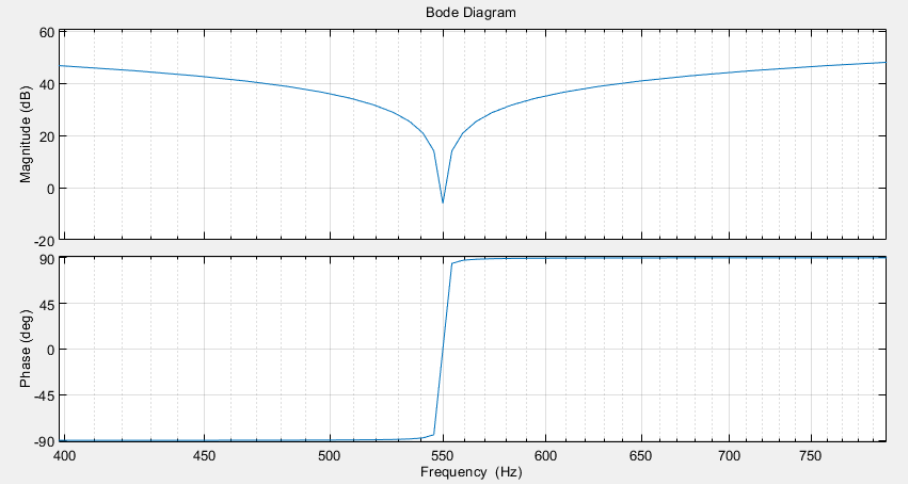

Figure 19: Bode Diagram of the trap filter for the 11th Harmonic (550 Hz)

Similarly, a filter to supress the 13th harmonic has been designed whose bode plot can be seen in the **Figure 20**. The transfer function of this filter is:

$$G_{13}(s) = \frac{(5.9*10^{-8})*s^2 + (43.1*10^{-7})*s + 1}{(8.8*10^{-7})*s} \quad (14)$$

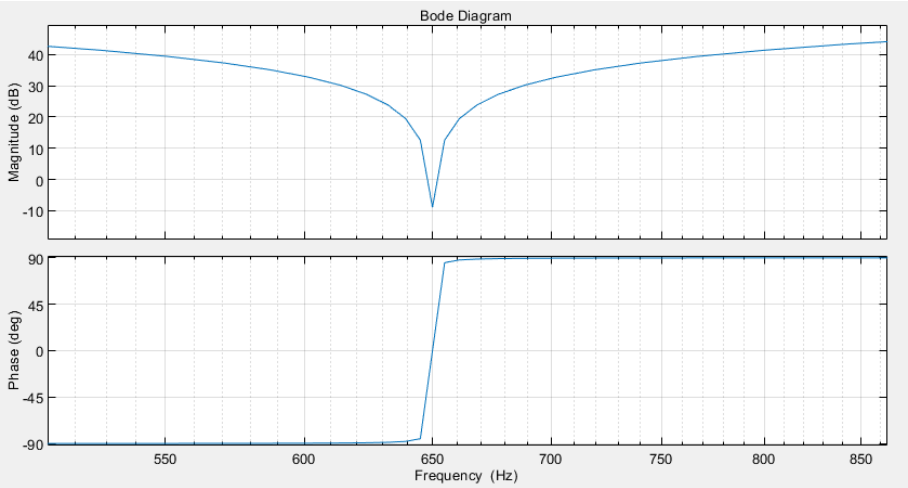

Figure 20: Bode Diagram of the trap filter for the 13th Harmonic (650 Hz)

Bode plots from the **Figure 19** & **Figure 20** show that the trap filters are designed to suppress the intended harmonics. The designed trap filters have been implemented in the simulations and their importance is depicted in the upcoming sections of this report.

2.2.2 Resonant Controllers

As previously mentioned, harmonic compensation can be carried out via the use of resonant controllers, as shown in **Figure 12**, in order to significantly attenuate the $12n \pm 1^{st}$ harmonic orders, where n is a positive integer originating from the implemented 12 pulse converters. The transfer function for the implemented resonant controller is shown in **eq. 15**:

$$R(s) = \frac{s}{s^2 + (2*\pi*f_r)^2} \tag{15}$$

Where 'f_r' is the resonant frequency. In this case the resonant frequencies are 600 Hz, 1200 Hz and 1800 Hz, corresponding to the 12^{th}, 24^{th} and 36^{th} order harmonics attenuating 11^{th} & 13^{th}, 23^{rd} & 25^{th}, & 35^{th} & 37^{th} harmonics respectively. Therefore, three resonant controllers are used in parallel, each tuned to their corresponding frequencies, thus attenuating the harmonics originating from the 12-TR topology. The harmonics of interest are within a bandwidth of 2 kHz in the harmonic spectrum. Below in **Figure 21**, the three resonant frequencies can be seen, as well as the corresponding attenuation of the frequencies on either side of the resonant frequencies.

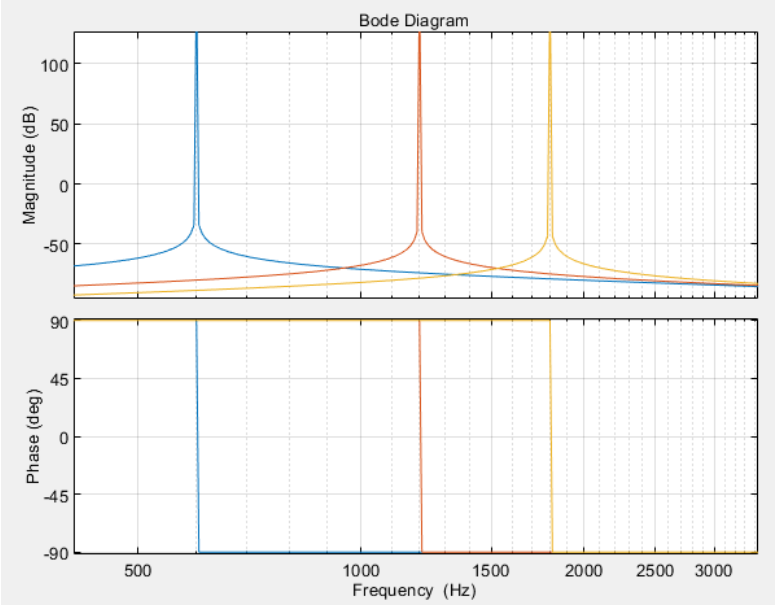

Figure 21: Bode Diagrams of Resonant controllers tuned to 12^{th}, 24^{th} & 36^{th} order harmonic frequencies

2.3 Reliability

Reliability is a performance metric, which needs to be considered during design, manufacturing, and implementation of power electronic devices. Redundancy and optimal design down to component level must be applied to the system to provide the most reliable and failure free system. The reliability of a system consists of several aspects, such as performance, probability, conditions, and time. Performance will indicate how well the system will operate over a period of time.

The reliability is important for the consumption plant since the power semi-conductor devices and capacitors are prone-to-failure. Furthermore, the high number independent components in power electronic equipment, such power electronic converters and consumptions plants, make it susceptible to a wide range of failure modes, thus decreasing the reliability of the overall topology [27].

Failure rate of the power electronic components varies depending on the operating conditions and testing methods. It must also be noted that the control algorithms are equally considered during reliability design of the power electronic systems. Furthermore, temperature cycling, material, and environment all affect the failure rates of the power electronic components [28].

2.4 Physical footprint

The footprint of each topology refers to the area that it utilizes upon installation. This is an important parameter, as a larger footprint leads to increase in real-estate cost, as well as the cost of installation, transportation, maintenance, while minimizing area for any additional installations within the vicinity of the particular topology. The major contributors to a larger footprint with regards to Thyristor Rectifier topologies are components such as transformers, capacitors and the heatsinks, which are attached to the semiconductor modules. Also, as capacitors are found in passive filters, the use of these trap filters increases the footprint of a topology. Ways to decrease the footprint would be to decrease the ratings of components or increase the switching frequency, such as in the case of transformers [29].

When comparing the areas of the different topologies, it is necessary to consider scalability, meaning that if much larger output power than 1 MW is required, the sizes of the components will increase accordingly. As the components that occupy the largest footprints are the magnetic

components, scaling up any of the topologies will require a Low Frequency Transformer with higher ratings and hence a larger footprint.

Regarding the four topologies, the least space consuming topology would be the 12-TR rectifier, as it is the simplest topology and consists of the fewest semiconductor components. The 12-DRMC and the AFE topologies are very similar in their physical footprints, as they both possess similar rectifier capacitor values and DC capacitor values and load inductances, as well as chopper inductances. Regarding their semiconductor volume, the AFE and DRMC consist of similar number of semiconductor devices. The advantage of the AFE is that it requires no passive filter, hence reducing the footprint. However, the sizes of semiconductor devices have a significantly lower footprint when compared to the LFT size and the capacitor and inductor sizes in these topologies.

The largest footprint is that of the 12-TRASPF, as its shunt active power filter requires an extra 'star-to-star' transformer to step down the voltage to a value where IGBTs can operate. This in effect increases the footprint of this topology. As there is a strong linear correlation between the power rating of a transformer and its area, **Figure 22** estimates this relation between the footprint and ratings occupied by 3-phase transformers. As the information for transformers rated higher than 2.5 MVA was not available, an extrapolation of the line of best fit was used, based on values obtained from a manufacturer for transformer ratings of 100 kVA up to 2.5 MVA in order to estimate the area occupied by a transformers rated up to 10 MVA [30]. The primary and secondary winding voltages of the transformers in **Figure 22** are 33kV and 400V respectively, so as to resemble the transformer used in this work for the APF of the 12-TRASPF.

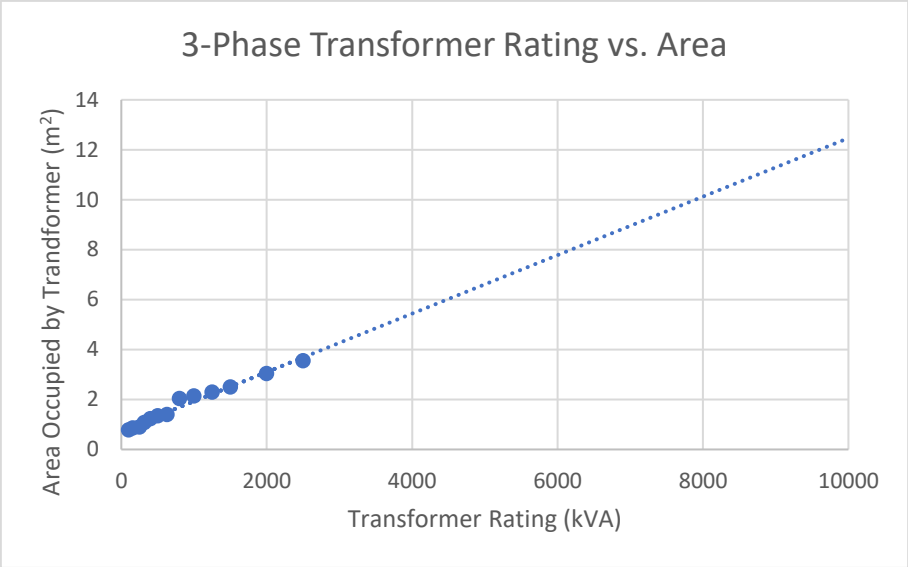

Figure 22: 3-phase Transformer Rating vs. Area Occupied

A further vital consideration regarding the footprint involves the cabinet size in which each topology will be placed, as the final area occupied by any of the four state-of-the-art rectifiers is dictated by the area of the cabinet size in which it is placed. Therefore, **Table 3** shown below gives an indication of the area occupied by the cabinets, as per company 'KraftPowercon Sweden AB', excluding LFTs as they are located externally, due to their size. The height parameter is 0.6 m^2 and remains unaltered for all power ratings [31].

Table 3: Area Occupied by a single Rectifier Topology in terms of Power Rating based on 'KraftPowerCon Sweden AB'

Rectifier Power Rating (MVA)	Area Occupied by Rectifier (m^2)
1	2.235
2.5	2.335
5	4.47
10	8.94

2.5 Operating conditions

This section will focus on the methods used for each topology for conducting the simulation tests with regards to the power quality, robustness and efficiency of each topology. The results obtained from the simulation tests will be used for comparison to determine the strengths and weaknesses

of each topology. The importance of each simulation test will be highlighted and the reason for performing the test will be elaborated.

2.5.1 Harmonic analysis

One measure of power quality involves harmonic analysis of the various topologies. According to the grid codes as per 'IEEE Std 519' the TDD must not exceed 5% and each harmonic up to the 2 kHz range in the harmonic spectrum has its own percentage limitation, according to its order [13]. The 2 kHz range implies that all the harmonic components up to and including the 40^{th} order harmonic are included in the calculation. In the case of 12-pulse thyristor converters, the harmonics of interest that require mitigation are primarily the 11^{th} order and 13^{th} order harmonics, as these are the lower order harmonics that appear, which are most significant in magnitude. Harmonic analysis is therefore vital when evaluating electrical power converters, as the grid code stated in **Section 1.3** must be met for the topologies to be implemented.

As previously mentioned, TDD is not a feasible method to determine if each topology is able to connect to the grid, due to the time range required to obtain the results. Therefore, THD will be used as an indicator in order to compare and rank the topologies when considering the harmonic analysis aspect of power quality. Harmonic analysis is carried out via the Fast Fourier Transform (FFT). The percentage of each harmonic order is calculated and normalized with respect to the fundamental.

In order to compare the harmonics of the various rectifier topologies, THD analysis is carried out. To compute the THD, a sampling period of 10 fundamental periods is used after steady state operation of the converter is reached. This implies a resolution of 5Hz, as the supply frequency is at 50 Hz. The signal of interest is the grid current, as this contains harmonics from the non-linear 12-pulse Thyristor Rectifier. The grid voltage harmonics are negligible, as voltage harmonics arise mainly from high line impedances, which are not the case in the simulations carried out for the purpose of this report.

2.5.2 Power Factor Analysis

Power factor analysis is another key indicator of power quality, as it quantifies how much active and reactive power is injected into the grid. A power factor close to unity is always desirable so as to

have maximum active power delivered across the load. However, inductive, and capacitive loads on lines and in power systems from the grid among various factors cause the power factor to decrease.

Power factor (PF) is measured in all the topologies by calculating the apparent power ('S') and either the active ('P') or reactive ('Q') power and obtaining the value from their relationship, as per **eq.1** and **eq. 2** shown in **section 1.3.1**.

APF is one of the prominent methods used to increase the power factor. It compensates for reactive power, by injecting the reactive power necessary for consumption by the non-linear load, thereby consuming less reactive power from the grid and maintaining a higher power factor. Also, passive filters can increase the system's power factor by tuning them to the resonant frequencies of the present harmonic orders.

2.5.3 Unbalanced Grid

In a three-phase system, voltage unbalances occur when the voltage between phases differs from each other. When the system is balanced, the magnitude of each phase must be identical, while a phase angle of 120 degrees exists between the three phases. Voltage imbalance is defined as: The ratio of negative sequence components to the positive sequence components, a simple formulation can be seen in **eq. 16** [32]**.**

$$V_{Unbalance} = \frac{Negative\ sequance\ voltage}{Positive\ sequance\ voltage} \tag{16}$$

If $V_{Unbalance} = 0$ the system is considered to be balanced. For consumption plants, it is not allowed to cause any unacceptable increase of unbalance to the grid. Due to technical requirements, 'unacceptable increase' must be evaluated for every single consumption plant individually to determine if the imbalance is acceptable. Depending on the rotational direction of the unbalanced voltage, the allowed unbalance level might increase compared to others [9] [33].

An unbalanced system will be undesired regarding power quality since severe imbalance can lead to change of magnitude and phase angle, in worst case leading to system instability. Difference between the phase voltages can occur due to several reasons, such as unbalanced source voltage from utility, unbalanced impedances on the lines, or unequal distribution of single-phase loads. In addition to the power quality issues the reliability of the system is also of concern since the

imbalance will change the system conditions from normal operation to abnormal operation, thereby subjecting the components to these undesired conditions [33].

Therefore, it is increasingly important to investigate how the system reacts to these unbalances. A simple way to emulate a degree of unbalance in each of the topologies is to inject an unbalance in one of the phases of the three-phase grid, hence creating an unbalance by feeding an uneven magnitude or phase angle of voltage to each specific line.

The reason why this test will be of interest is to analyse the effect of the unbalanced on the system and evaluate the robustness of the topologies to the unbalances in the grid. Due to the unbalance, harmonic and power factor changes will be investigated and further analysed. There are no specific requirements for voltage imbalance in the grid codes.

2.5.4 Load variation

In order to observe the stability and robustness of the system, a variable load test is necessary. The output from this test is analysed regards to the effect on THD and the power factor due to the changes incurred by the load variation. This test is conducted by decreasing the output power to the P2X load from 1 MW in decrements of 20% capacity until a partial load of 0.2 MW. To obtain this partial load, 12-TR and 12-TRASPF topologies decrease their reference DC current values, while in the 12-DMRC & AFE topologies the decrement is inputted in the reference DC voltage accordingly.

The voltages for these stages have been calculated by the formula such that the corresponding load variations are achieved:

$$Power = \frac{Voltage^2}{Load\ Resistance} \tag{17}$$

2.6 Efficiency

The section describes the method to estimate the efficiency of the discussed topologies. Usually, efficiency is measured as a ratio between the input power and output power of the system. The efficiency is mathematically calculated by the formula in **eq 17**:

$$\eta = \frac{Power\ recieved\ by\ the\ load}{Power\ delivered\ from\ the\ grid\ side} \tag{18}$$

Where $'\eta'$ represents the efficiency of the system. However, since the models are created in ideal conditions, it would be expected to have an overall efficiency of 100%. Therefore, the models must be altered, such that the components implemented in the models mimic the practical components in terms of variables and attributes, which in an ideal system would not be accounted for.

To emulate the system entirely, components must be selected based on knowledge obtained during the initial implementation of the ideal system, hence finding the semiconductor devices like thyristors, diodes, IGBTs, MOSFETs and transformers which are capable of withstanding attained operational criteria. The criteria for each component may differ depending on the rating and how they are applied in the topology. Furthermore, it is common practice to add a safety margin of 25% to protect against malfunctions if abnormal operation occurs in the system.

2.6.1 Thyristor

As previously mentioned, certain criteria must be met, when choosing thyristors for the topologies such as TR and TRASPF. Parameters are investigated based on available data from the simulations. When selecting an appropriate thyristor, criteria such as the repetitive off-state voltage (V_{DRM}), on-state RMS current ($I_{T(rms)}$), average on-state current ($I_{T(AV)}$) and critical repetitive rate of rise of on-state current ($\frac{dI}{dt}$) are all important parameters to investigate [17].

The specified current limit is shown below in **eq. 19**:

$$I_{T(rms)} = \frac{\pi}{2 * I_{T(AV)}} \tag{19}$$

Hence the average on-state current can be solved from the above equation:

$$I_{T(AV)} = \frac{2}{\pi} * \ I_{T(rms)} \tag{20}$$

Therefore, each of these parameters must be considered when choosing the thyristor. Most of the ratings depends on temperatures. If the temperature is operating at ideal conditions, the SCR can be selected based on the currents $I_{T(rms)}$ and $I_{T(AV)}$ and voltage V_{DRM}. Since the 12-TR and 12-TRASPF operate as full-wave rectification models, SCRs are capable of controlling load currents similar to $I_{T(rms)}$. From the simulation it is possible to measure most of the necessary parameters, to compare different thyristors data with the simulation model.

Table 4: Commercial Thyristor Parameters for 12-TR Simulation

Parameters	Simulated Thyristor values	25% Safety Margin Ratings	Ratings of Commercial Thyristor
V_{DRM}	1440 V	1800 V	1800 V
$I_{T(rms)}$	295 A	370 A	393 A
$I_{T(AV)}$	167 A	270 A	250 A

Table 4 shows the parameters of the thyristor used in the 12-TR simulation specifications are used to obtain commercial thyristors that match the parameters of the simulation model. The best fit needs to have higher rated values for current and voltage, compared to the simulation model, in order to prevent failure.

The commercial thyristor chosen is ND421825 [34]. The voltage of the ND421825 have 20% safety margin, however the Current Rms and average have almost exactly 25% margin. It would be possible to obtain another commercial thyristor model, which would fit the specifications stated in **Table 4** even better. However, for simulation purposes this commercial thyristor should work appropriately. Other important factors when choosing the commercial products are cost and size. However, these factors can only be reduced if the technical specifications allow it.

The above section clarifies how the thyristors are chosen based on specific measurements which can be obtained before choosing the commercial thyristor. Each commercial thyristor will have certain characteristics that will affect the efficiency of the specific thyristor. On-state voltage (V_T) is the voltage which is induced at the input terminals to the thyristors, are based on the forward on-

state current (I_T). The threshold voltage ($V_{T(T0)}$) are defined by a straight line to the voltage axis plotted through $'1 * I_{T(Av)}'$ and $'3 * I_{T(Av)}'$. Examples of the line and values of $I_{T(Av)}$ (blue points) are seen in **Figure 23**.

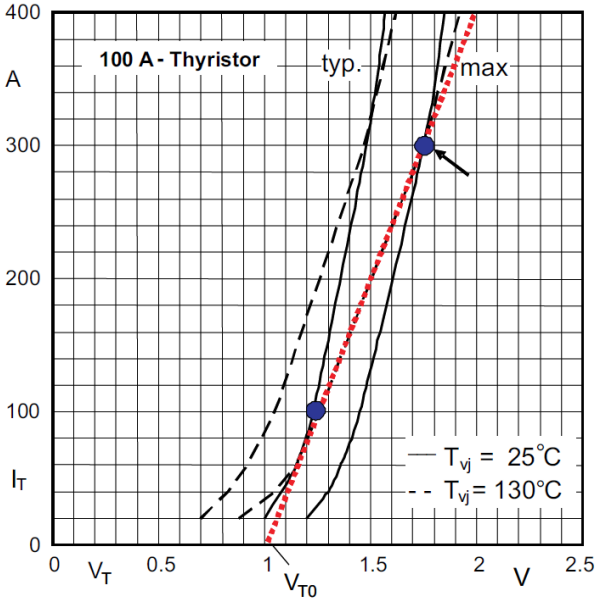

Figure 23: Example of $V_{T(T0)}$ and straight line between $1 * I_{T(Av)}$ and $3 * I_{T(Av)}$ [35].

The line is determined by the **eq. 21**

$$V_T = V_{T(T0)} + r_T * I_T \tag{21}$$

Here (r_T) is defined as the slope resistance of the thyristor and are used in order to calculate on-state power dissipation (P_T).

$$P_T = V_{T(T0)} * I_T + r_T * {I_T}^2 \tag{22}$$

The on-state power dissipations are usually given as an average value ($P_{T(Av)}$), obtained as a function of the average on-state current, voltage threshold and slope resistance. The average power dissipation is calculated in a similar manner.

$$P_{TAV} = V_{T(T0)} * I_{TAV} + r_T * {I_{TRMS}}^2 \tag{23}$$

The Power dissipation can be used in order to calculate the thyristors loss of power. As an example, the loss of ND421825 can be calculated based of its datasheet. The power loss of the thyristor can be calculated to approximately 265 W [35].

2.6.2 Diode

For a semiconductor such as a diode, current is only allowed to flow in one direction. Diodes are commonly referred to as a PN junction, since is consists of P and N-type materials. A diode will conduct only if the voltage applied across it $'V_D'$, is larger than its threshold voltage $'V_{T0}'$. Therefore, if $'V_D < V_{T0}'$, the diode will not conduct, as the current through the diode is very limited, hence resembling an open switch, or very high resistance. When $'V_D > V_{T0}'$, the current in the diode will increase significantly, hence resembling a closed switch or very low resistance path.

Similar to the thyristor, it is necessary to investigate the voltage and current ratings of the diodes in the 12-DRMC topology. The parameters such as voltage across the diode $\mathrm{V_D}$, maximum current peak of diode (I_{FSM}), RMS current of the diode (I_{FRMSM}) and the average current across the diode (I_{FAVM}) are all required parameters for the correct choice of diodes in the topology.

Table 5: Commercial Diode Parameters for 12-DRMC Simulation

Parameters	Simulated diode values	25% Safety Margin Ratings	Rating of Commercial diode
$\boldsymbol{V_D}$	1760 V	2200 V	3600 V
$\boldsymbol{I_{FSM}}$	370 A	465 A	5500 A
$\boldsymbol{I_{F(RMS)M}}$	166 A	210 A	370 A
$\boldsymbol{I_{F(AV)M}}$	95 A	120 A	235 A

Table 5 shows the simulated diode values compared to a commercial diode chosen with ratings of a 25% safety margin. The commercial diode with device name 'SD233N36S50PC' has an appropriate safety margin in all parameters, even when considering the peak conditions of the system. Therefore, this diode was chosen for the model [36], [37].

The above section explains the selection process for diodes and in a similar manner to the thyristors the diode also has some commercial characteristics. The voltage induced at the diode terminals are referred to as forward voltage (V_F), which in a similar manner is based in the induced forward current (I_F). The diodes also include the threshold voltage (V_{T0}) which are defined similarly to that

of thyristors. Similar to the thyristor, the slope resistance is defined as (r_f) and the power dissipation (P_F) is obtained in a similar manner, as shown below in **eq. 24**:

$$P_F = V_{T0} * I_f + r_f * {I_f}^2 \tag{24}$$

The above equation can then be applied in order to determine the power dissipation from the selected commercial diode with device name 'SD233N36S50PSC', thus giving the following loss of 453 W.

2.6.3 IGBT

As with thyristors and diodes, IGBTs must also follow certain criteria. These criteria are essential to ensure safe operation, since transients could lead to deterioration or even complete malfunction of the device. Even continuous use within maximum rated conditions regarding current, voltage and temperature could possibly lead to a significant decrease in reliability.

The parameters of the IGBT need to be investigated in order to choose the correct commercial option. The collector-emitter voltage (V_{CES}) is the maximum voltage between the collector and emitter, that under any condition should be applied to the IGBT. The DC collector current (I_C), is the maximum DC-current the IGBT can conduct. Peak collector current (I_{CM}) is the maximum peak current allowed for the IGBT to switch at. Gate-emitter voltage (V_{GES}) is maximum voltage between gate and emitter of the IGBT [38].

Table 6: Commercial IGBT Parameters for AFE Simulation.

Parameters	Simulated IGBT values	25% Safety Margin Ratings	Ratings of Commercial IGBT
V_{CES}	1200 V	1500 V	1700 V
I_C	600 A	750 A	800 A

Table 6 shows the parameters and respective ratings for the IGBTs used in the AFE model. A similar method is applied in order to determine the ratings of the IGBTS for the 12-DRMC & 12-TRASPF. To ensure the highest reliability of the components, all have been selected with a safety margin of 25% above the measured ratings in the simulation, thus also ensuring the commercial IGBT ratings are

not exceeded. The IGBT chosen for the AFE is manufactured by Infineon and has the following device name: 'FF800R17KP4' [39].

After the selection process is completed, it is necessary to understand how the standard of the chosen IGBT is constructed. The IGBT has a collector-emitter voltage, which is the IGBT 'on-state' voltage drop and is based on the collector current. At rated current, the collector-emitter voltage increases in proportion to temperature. This temperature dependency will impact the losses in the IGBT. The losses from the IGBT are mostly dependant on the 'turn-on' and 'turn-off' energy dissipation ($E_{on/off}$). The on/off energy dissipation is dependent on the collector current and the switching frequency (f_s). The energy dissipation can be calculated in a similar manner for both the 'on' and 'off' losses, per **eq. 25** and **eq. 26**:

$$P_{on} = f_s * E_{on} \tag{25}$$

$$P_{off} = f_s * E_{off} \tag{26}$$

The equation depends on the system's switching frequency in order to determine the power losses. The power losses for 'FF800R17KP4' commercial IGBT device, can be calculated from **eq. 25** and **eq.26**. Hence a total loss from the IGBT will be approximately 12.2 kW. However, it is important to clarify that the losses will vary, depending on the operational temperature of the IGBT and the calculated losses are for operating temperatures of 150 C° [35].

2.6.4 MOSFET

The Modular Multicell Rectifier (MMR) topology, which will be discussed in **Chapter 4**, is composed of MOSFETs. MOSFETs like all other semiconductors needs to be selected in terms of parameter ratings and characteristics. These parameters will be dependent on the application and installation environment.

In that regard, the parameters necessary to consider are the drain-source voltage (V_{DS}), drain current (I_D), and the on-state resistance ($R_{DS(on)}$) of the MOSFET. The drain-source voltage is especially important since it affects the 'on-state' resistance, since there often is a linear dependency between high drain voltage and 'on-state' resistance [40]. Similar to previous components the parameters need to have a safety margin of 25%.

Another important parameter to consider is the gate voltage (V_{GS}). To trigger the MOSFET, 'V_{GS}' must exceed the threshold voltage (V_{T0}) [40].

Table 7: Commercial MOSFET Parameters for MMR Simulation [41]

Parameters	AC/DC MOSFET simulated value	25% Safety Margin Ratings	Rating of commercial MOSFET
V_{DS}	685 V	860 V	1200 V
I_D	26 A	33 A	40 A

Table 7 shows the ratings of a commercial MOSFET with device name 'SK45MH120TSCp', used in the novel topology MMR, which will be analyzed in Chapter 4. The MOSFETS losses are unlike the previous discussed semiconductors. The switching characteristics of the MOSFETs given by the datasheets are determined in a less realistic manner and are usually based on measuring the MOSFETs in an ohmic circuit in order to determine its properties.

The switching losses are determined by the internal and external capacitances, inductances, and resistances of the circuits. Therefore, the datasheets for MOSFETs are used as a rough guide for installation. Hence measurements during the implementation phase in the circuits are necessary [35].

2.6.5 Transformers

Transformers are one of the major contributors to the losses in the system. The losses in the transformers are usually represented by the resistances and inductances in the simplistic equivalent circuit as shown in **Figure 24**.

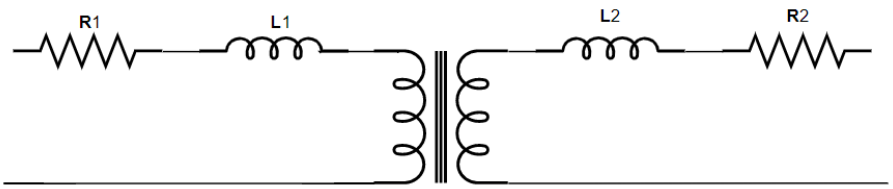

Figure 24: Simplistic Equivalent Circuit of a Transformer

To make the efficiency calculation practical, the values of the resistances (R1 & R2) known as winding resistances & inductances (L1 & L2) known as leakage inductances should be included. The

default values in the PLECS platform for the leakage inductances have been used. The values of the winding resistances have been taken from [42] and are listed in **Table 8**.

Table 8: Winding Resistances of the Transformer

Phases	Value	Unit
Phase A	**13.84**	**mΩ**
Phase B	**13.87**	**mΩ**
Phase C	**13.94**	**mΩ**

3 SIMULATION RESULTS

In this section, the focus will be on the simulation and results of the power converter topologies used in the P2X consumption plant. The following simulations were all conducted in the simulation tool PLECS, hence obtaining the most uniform results for each topology. All topologies will be subject to the same tests, in order to compare the obtained results. The test includes harmonic analysis, unbalanced grid study, load variation and efficiency calculation. These tests provide the performance indication of the mentioned aspects of these topologies. Hence an assessment of the different topologies can be deduced.

3.1 12-pulse Thyristor Rectifier (12-TR) simulation and results

In this section all the tests will be conducted for the 12-TR topology. The tests will be conducted with and without the passive trap filter, which will highlight the importance of the filter.

Table 9 and **Table 10** tabulate the component parameters and control parameters used in all simulation tests of the 12-TR.

Table 9: parameters used in components of 12-TR.

Parameters of control scheme	Values
V_{Grid}	33 kV
L_{Grid}	1^{-6} H
L_{In}	350^{-6} H
L_{DC}	300^{-6} H
V_{DC}	1 kV
C_{DC}	5000^{-6} F
R_{Load}	1 Ω

Table 10: Parameters used in control system for 12-TR.

Parameters of control scheme	Values
I_{DC}*	1 kA
Grid voltage	27 kV
K_P	0.0001
K_I	0.02
Delay	1/600

These parameters referred to **Figure 4** and **Figure 5** respectively.

3.1.1 Output under ideal full load conditions

In this section the general parameters of the topologies are examined in order to verify that every simulation is operational and to set a baseline for the upcoming results. The results presented in this section will revolve around full load ideal simulations on the output DC side of the P2X plant.

For the simulation to operate in ideal conditions, the passive trap filter is necessary. The passive trap filters are placed on the grid side of the topology to mitigate the harmonic distortion in the system.

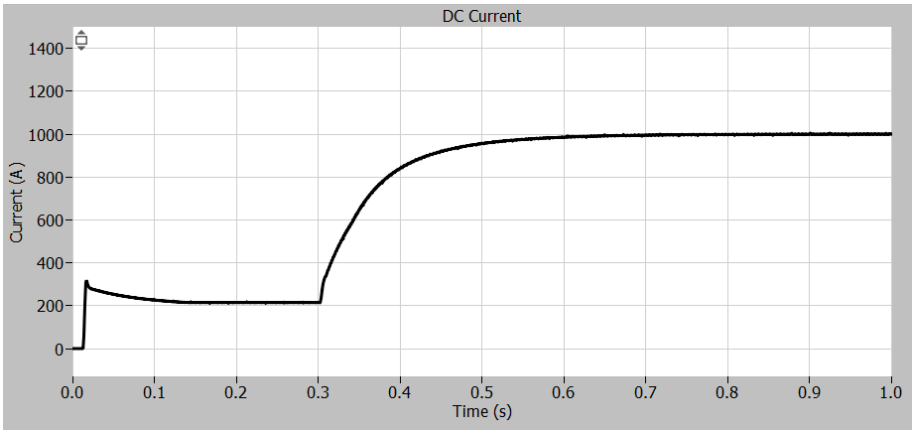

Figure 25: DC current from the 12-TR with passive trap filter

Figure 25 show the DC current output of the 12-TR during ideal conditions described earlier. The current follows the reference at 200 A until 0.3 seconds, before the reference is increased, reaching a steady state at 1000 A.

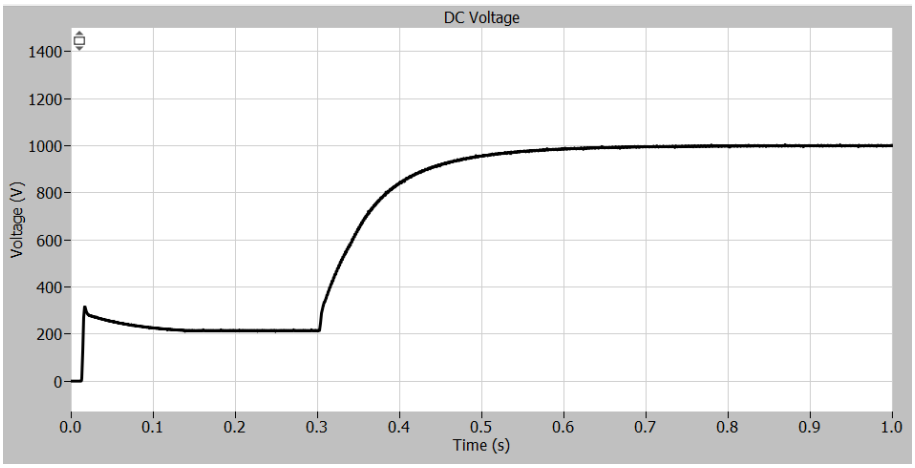

Figure 26: DC voltage from the 12-TR with passive trap filter

Figure 26 depicts the DC voltage of the 12-TR during the ideal conditions. Similar operation as the current can be observed until it reaches a steady state of 1000 V.

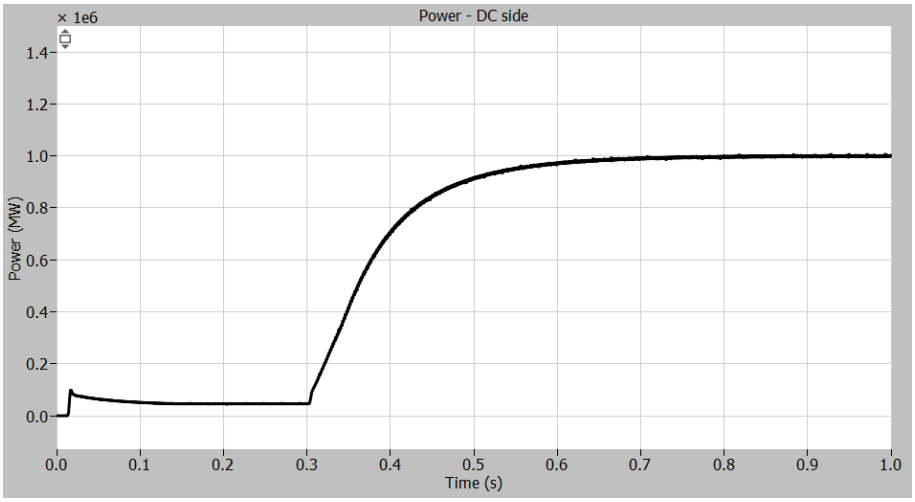

Figure 27: Power at the DC side from the 12-TR with passive trap filter

Figure 27 depicts the DC power output. Similar to the voltage and current, the power will reach a steady stage of approximately 50 kW before the reference is increased. The reference increase results in a steady state value of 1 MW as expected.

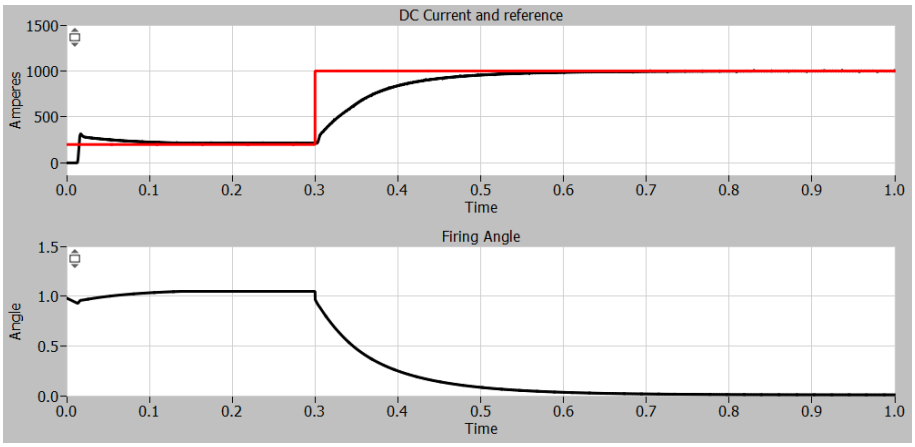

Figure 28: The reference current (Red) and DC current (Black) and the firing angle of the 12-TR with passive trap filter

Figure 28 depicts the reference current and DC-output current in the first graph, while the second graph describes the firing angle. After an increase of the reference (depicted in red) the output changes imminently and corrects itself according to the reference while the firing angle adjusts itself simultaneously.

Table 11 depicts the ideal values of the system in the ideal conditions. The obtained values are all close to the desired values for the topology.

Table 11: 12-TR with passive trap filter parameters

Parameters	Value	Unit
RMS current grid-side	17.6	A
RMS voltage grid-side	33	kV
Power factor grid-side	0.99	-
Current DC-side	1	kA
Voltage DC-side	1	kV
Active power DC-side	1	MW

3.1.2 Harmonic Analysis

Harmonic analysis is conducted for each topology, to ensure that the power quality is within the requirements stated by the IEEE 519 mentioned in **section 1.3**. Each topology is constructed in ideal conditions; hence the obtained results will show the most optimal harmonic levels. Furthermore, this simulation is conducted in order to give an indication of how each individual topology operates under optimum conditions.

12-Pulse Thyristor Rectifier Without Trap Filter

The harmonic analysis for 12-TR will be conducted on the grid side of the model; hence a measurement of current is inserted before the transformer. The simulation tool PLECS includes a simulation block which directly computes the THD of the current. This block is applied to the current measurement in order to measure its THD. **Figure 29** shows the current waveform on the grid side.

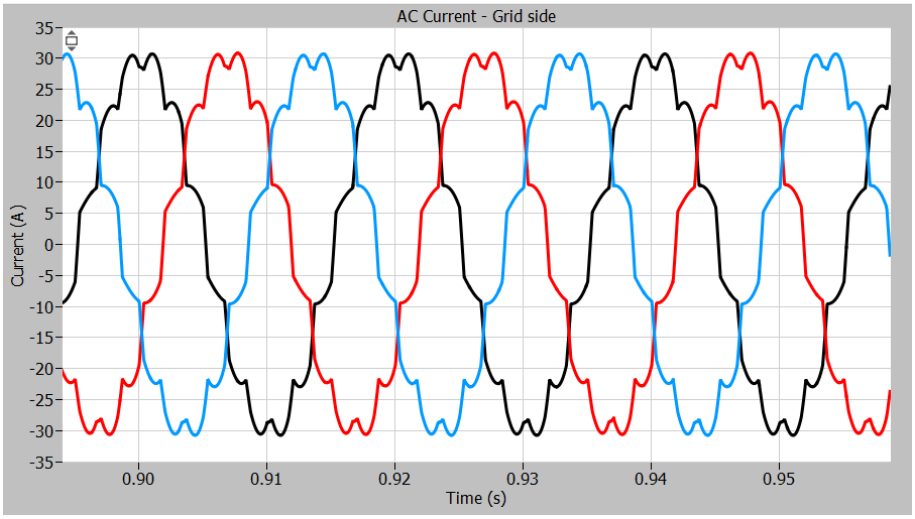

Figure 29: Measurement of current on the grid side

The current graph depicts a highly distorted three-phase current waveform. The calculated THD_I is 8.92% for the grid side current, while the allowed distortion level stated in the standard 'IEEE 519' is 5% TDD. For a fully loaded system THD≈TDD [12]; hence the amount of THD is too high. Therefore, the grid requirements are not met, and the topology will not be allowed to connect to the grid. The measured THD of the model is in excess by an amount of 3.92% above the allowed limits. Hence a passive filter is necessary for the 12-TR to meet the grid requirements.

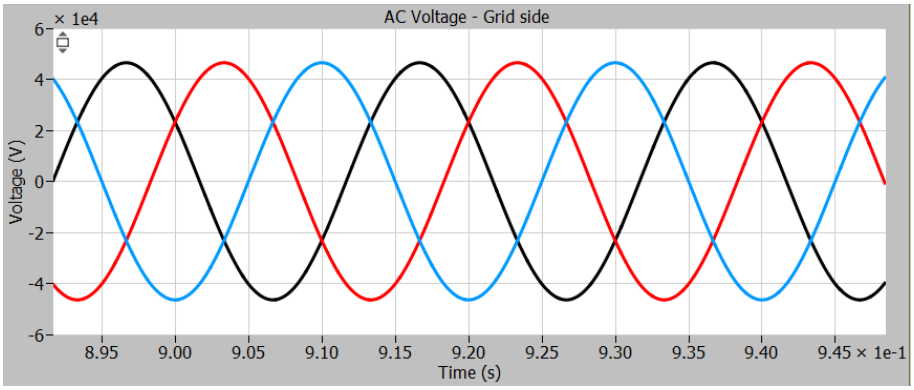

Figure 30: Measurement of voltage on the grid side

The voltage graph in **Figure 30** depicts no visible indication of distortion, which is also confirmed by the THD measurement $THD_V \approx 0.26^{-7}$. The low distortion of voltage is due to the almost ideal impedance on the grid lines; hence no distortion will be seen on the voltage in any of the following topologies.

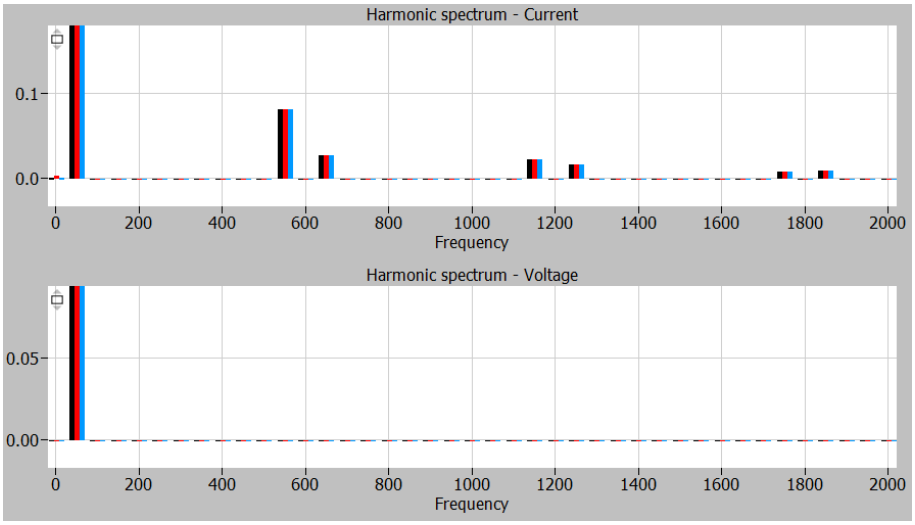

Figure 31: Harmonic spectrum of the current & voltage harmonics on the grid side. Normalized at fundamental frequency of 50 Hz

Figure 31 shows each individual order of current harmonic from $I_1 - I_{40}$. The only harmonics present in the 12-TR are of the orders of 12±1 and multiples of 12±1 visible in the harmonic spectrum above.

Table 12: Harmonic order 1±12 for 12-TR without trap filter

Harmonic Order	Value
11th Harmonic	8.02%
13th Harmonic	2.57%
23rd Harmonic	2.16%
25th harmonic	1.57%
35th harmonic	0.71%
37th harmonic	0.83%
THD	8.94%

Similar to the THD measurement conducted previously shown in **Figure 31**, all of the 12n±1 harmonic order values are documented in **Table 12**. A comparison with **Table 1** indicates that none of the observed harmonic orders are within the specified limits. As already discussed, there is no distortion on the voltage. This is further verified from this harmonic analysis, as only the fundamental voltage harmonic is present in the harmonic spectrum as seen in **Figure 29**. Hence the harmonic analysis of the remaining topologies will only be concerned with the current harmonic spectrum.

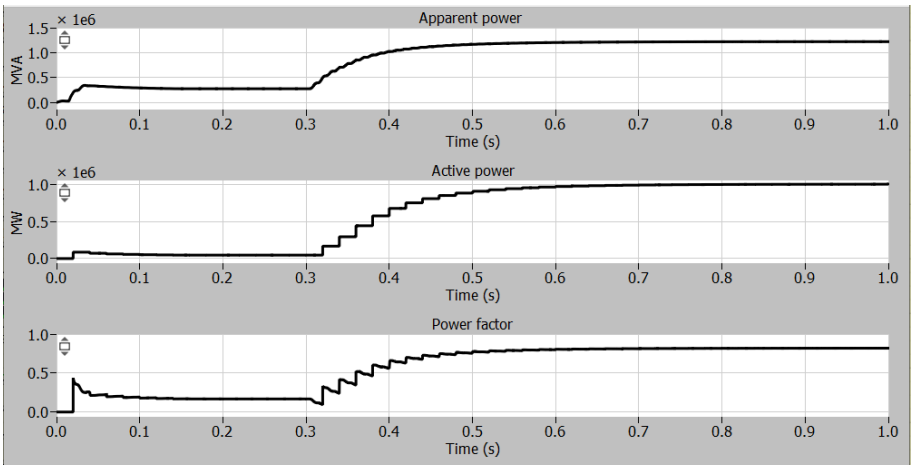

Figure 32: Graphs of Apparent power (S), Active power (P) and Power factor (PF).

Figure 32 shows the apparent power, active power, and power factor respectively. The power factor is measured as 0.82. The power factor also indicates a poor power quality, similar to the THD. Low power factor is an indication of phase shift between the voltage and current signal and an indication

of poor overall power quality since there is an inverse relationship between PF and THD which is shown in **eq. 3** of **Chapter 1**.

12-Pulse Thyristor Rectifier With Trap Filter

The harmonic analysis will now be presented with the inclusion of the passive trap filter. The trap filter is inserted on the grid side of the simulation model, in order to mitigate the harmonic disturbance in the 12-TR topology.

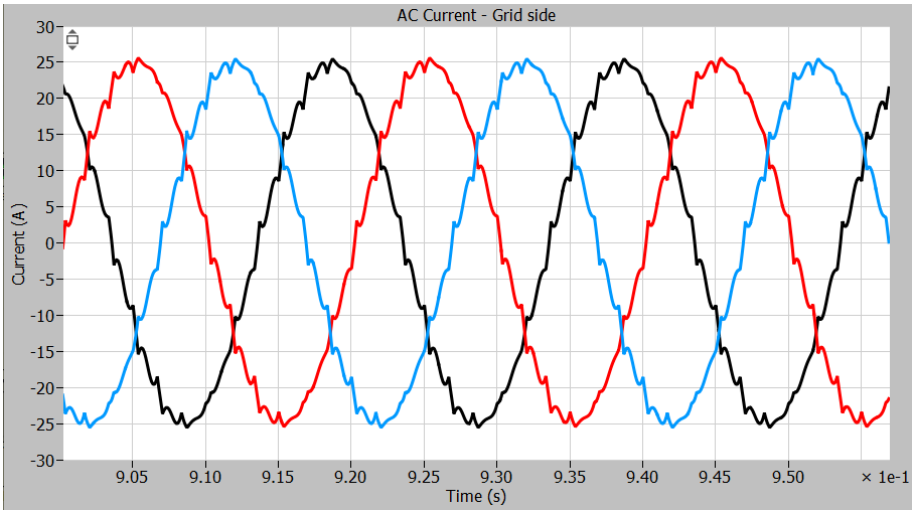

Figure 33: Measurement current on the grid side with passive trap filter

Figure 33 shows the current on the grid side while the trap filter is added to the topology. The graph indicates clear improvements in terms of distortion, which is noticeable by a smoother sinusoidal curving of the current signal.

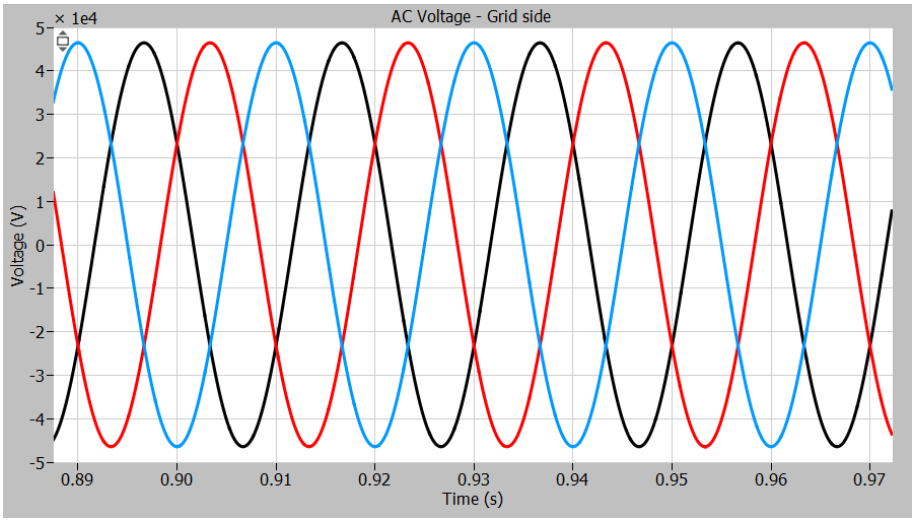

Figure 34: Measurement of voltage on the grid side with passive trap filter

Figure 34 depicts the THDv and grid voltage. The voltage is similar to that of the 12-TR without the passive filter. Hence the trap filter is not inducing any harmonic to the system voltage and the voltage analysis will be omitted for the rest of the topologies.

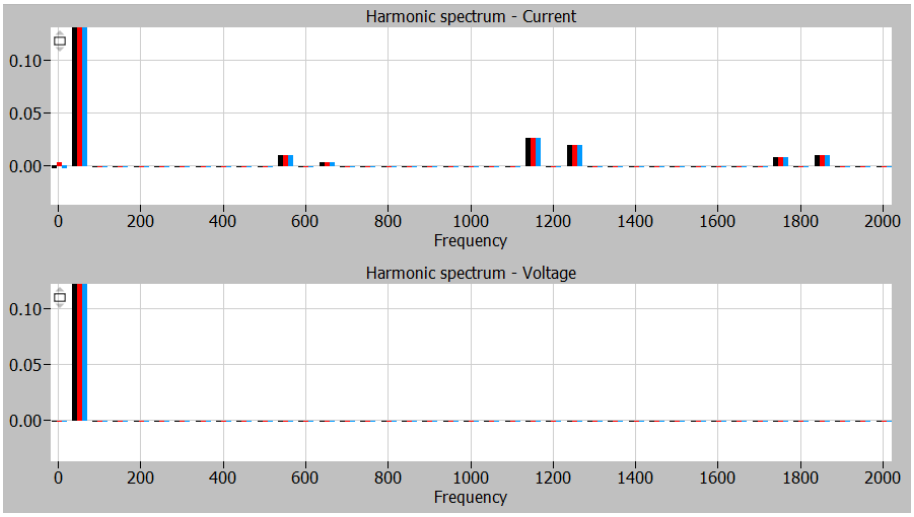

Figure 35: Harmonic spectrum of the current & voltage harmonics on the grid side with passive trap filter. Normalized to fundamental frequency of 50 Hz

Figure 35 shows the harmonic spectrum of the current and voltage respectively. Clear improvements can be seen in the current harmonic spectrum, specifically for the 11^{th} and 13^{th} harmonic orders which are significantly suppressed. The THDi is equal to 3.64% after the trap filters are implemented, showing a remarkable improvement. Further analysis of the individual harmonics is seen in **Table 13**

Table 13: Harmonic order 1±12 for 12-TR with trap filter

Harmonic Order	Value
11^{th} Harmonic	0.9%
13^{th} Harmonic	0.2%
23^{rd} Harmonic	2.5%
25^{th} harmonic	1.9%
35^{th} harmonic	0.8%
37^{th} harmonic	0.9%
THD	3.64%

From **Table 13** mitigation of distortion is observed for the 11^{th} and 13^{th} harmonic and consequently improving the THD within the standards. Thus, proving that the trap filter is operating as intended by mitigating the disturbance in these harmonic frequencies. However, the remaining harmonic orders are still not meeting requirements stated by IEEE 519 shown in **Table 1.** It would be possible

to add additional trap filters to the topology in order to meet the requirements, if deemed necessary but it comes at the expense of additional cost, footprint & complexity.

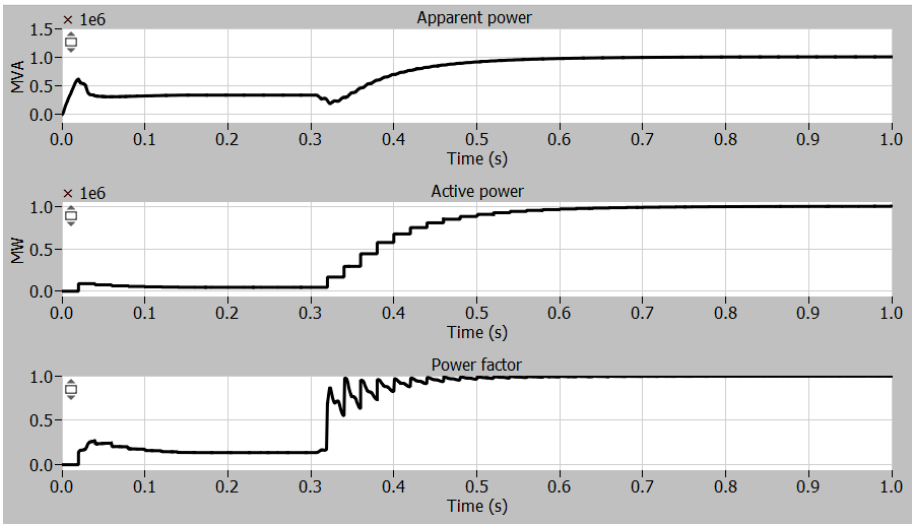

Figure 36: Graphs of Apparent power (S), Active power (P) and Power factor (PF) with passive trap filter.

The apparent power, active power, and power factor can be seen in **Figure 36**. The apparent power shows significant improvements in terms of reactive power being decreased from 1.2 MVA to 1 MVA. The decrease in reactive power can be explained by the trap filter drawing reactive power from the grid, hence improving the power factor of the topology in the process.

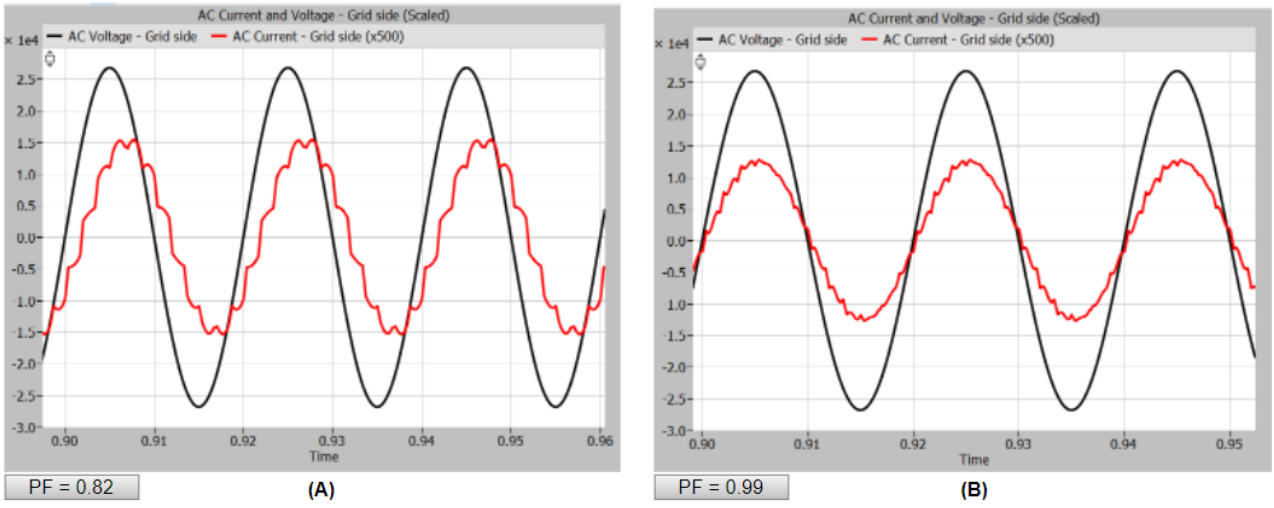

Figure 37: Current and voltage – grid side – (A) depict the waveform with PF of 0.82 while (B) shows with 0.99

Figure 37(A) shows the voltage and current waveform without the trap filters. It can be seen that the current and voltage are slightly out of phase resulting in a poor power factor of 0.82. however, **Figure 37**(B) shows the waveforms with the inclusion of the trap filters. The power factor is 0.99

hence a large improvement is observed, further the current and voltage waveform are seen to be in phase, thus indicating that the power factor will dictate the waveform's phase difference.

3.1.3 Unbalanced Grid

For the unbalance grid simulation, the three-phase voltage source is replaced by three single-phase voltage sources. Replacing the source will enable changes to each individual phase in either magnitude or phase angle, hence inducing imbalance into the system. The changes will be observed and evaluated in order to check the robustness of the topology. Furthermore, the power quality will also be of interest, as it will be used as a tool to get the measure of the robustness during the unbalances.

12-pulse Thyristor Rectifier Without Trap Filter

In order to investigate the impact of unbalanced load on the 12-TR simulation model, a change in either magnitude or phase angle is necessary. The changes will only be induced in one of the single-phased voltage sources, with a dip of 10% in the magnitude.

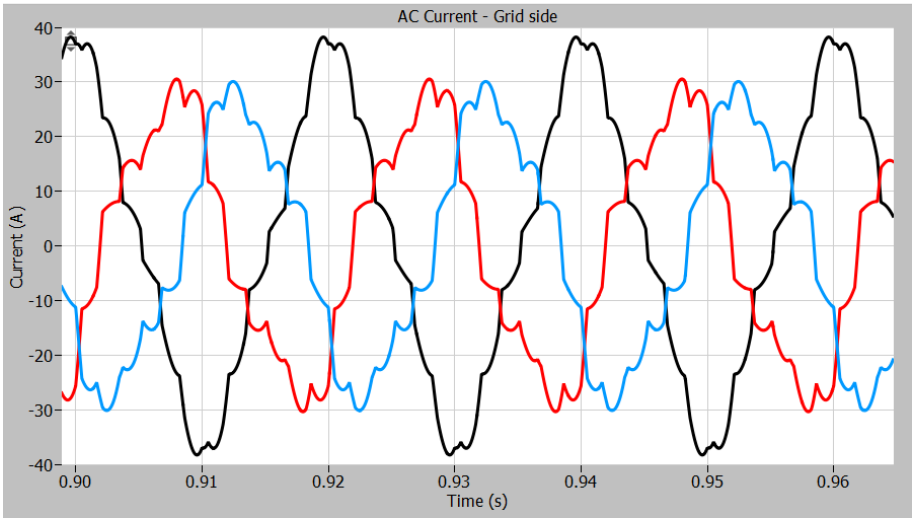

Figure 38: Current measurement with 10% decrease of voltage phase B without trap filter.

Figure 38 shows the grid current during an unbalance with a 10% decrease of magnitude in one of the three star-connected single-phased voltage sources. Imbalance is clearly achieved by decreasing the magnitude by 10%, indicated by the unequal magnitude of phase currents. The imbalance is also shown by an increase in THDi = 13.19% which is present in the system compared to the ideal case shown in **Figure 29**.

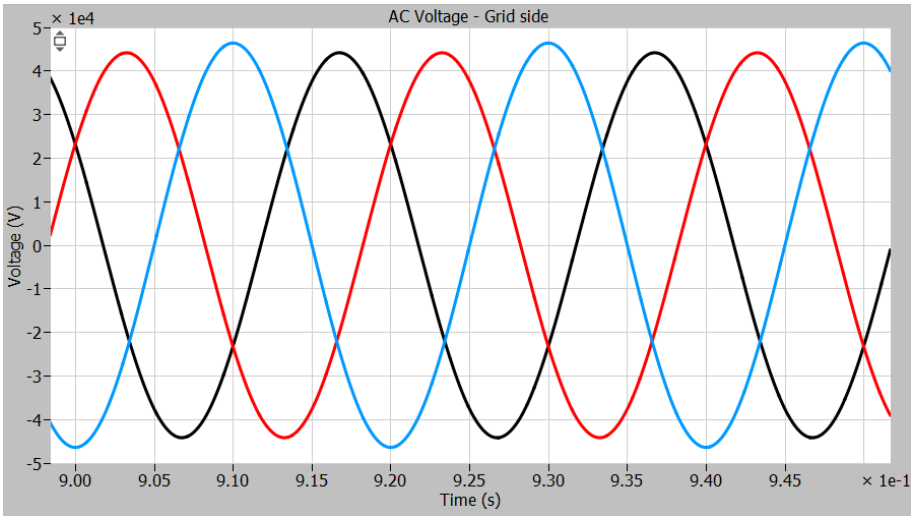

Figure 39: Voltage measurement with 10% decrease of voltage phase B without trap filter.

The grid voltage is also affected slightly by the unbalance in the system, which can be seen in **Figure 39**. The imbalance is shown by the unequal magnitudes of the voltage phases with an induced 10% dip. Since this change will be similar for all the topologies during unbalance studies, the following topologies will omit the voltage study.

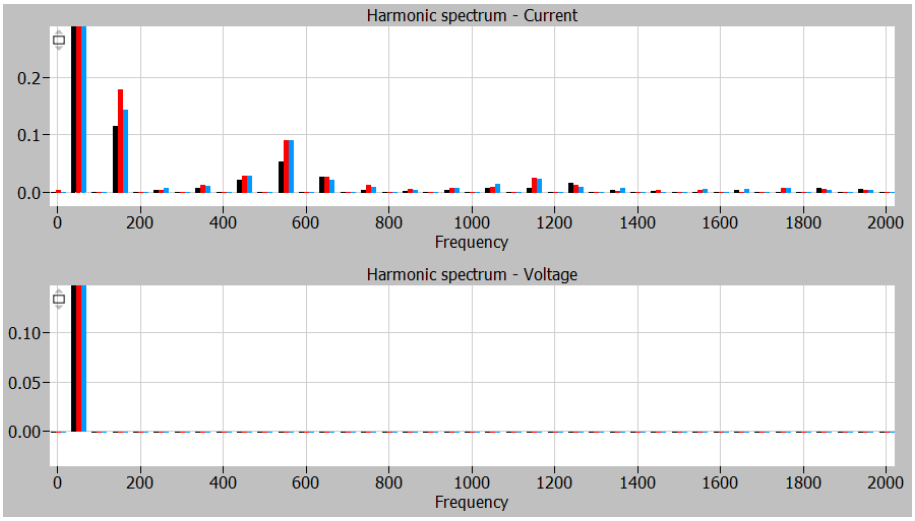

Figure 40: Harmonic spectrum of 10% decrease of voltage magnitude. Normalized to fundamental frequency of 50 Hz

The harmonic spectrum can be seen in **Figure 40.** Compared to the previously discussed ideal case shown in **Figure** 31, significant changes can be observed. When unbalance occurs, a third order harmonic current is induced into the system. Third harmonics originate from the oscillating current in the neutral since this topology does not contain any active unbalance mitigation control. The magnitude difference will create an uneven product of current, which will flow in the neutral wire.

Another interesting part of the harmonic spectrum is the uneven distribution of harmonics in the different phases, which seem to emulate the uneven magnitude of the phases. From the current waveform in **Figure 40** the 'red' and 'blue' magnitude seems to be lower than the black magnitude. When analyzing the harmonic spectrum, an opposite trend occurs. The trend indicates that equal distribution of distortion is in each phase. However, with lower current magnitude the concentration of distortion is amplified and hence the high 'blue' and 'red' orders in the harmonic spectrum.

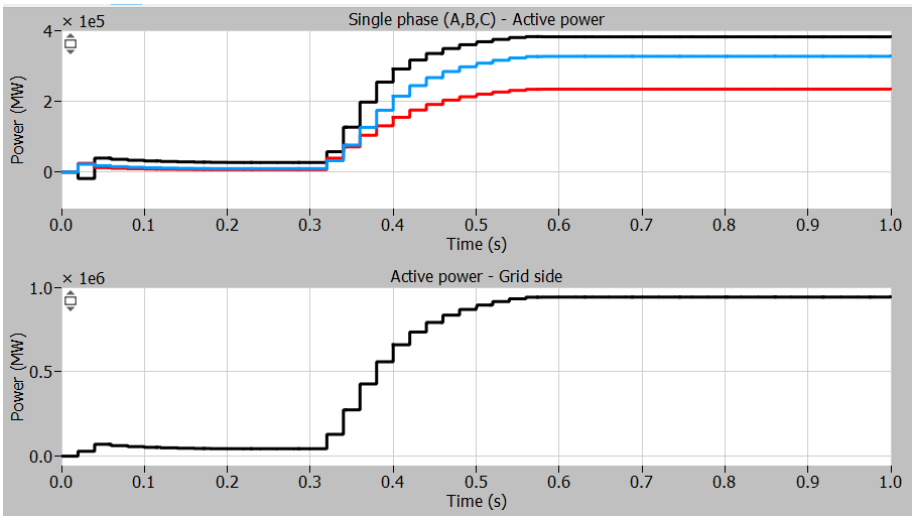

Figure 41: Active Power of Single Phases A, B & C & Total Grid Side Active Power

Figure 41 depicts the active power for each phase and the total amount of active power. A difference in magnitude is observed in the single-phased active power. The grid unbalance causes unequal sharing of power by the different phases as seen in 1st plot in **Figure 41**. However, the total active power is still 1 MW, thus indicating the phases compensate for each other to deliver required power across the load as supported by the graphs shown.

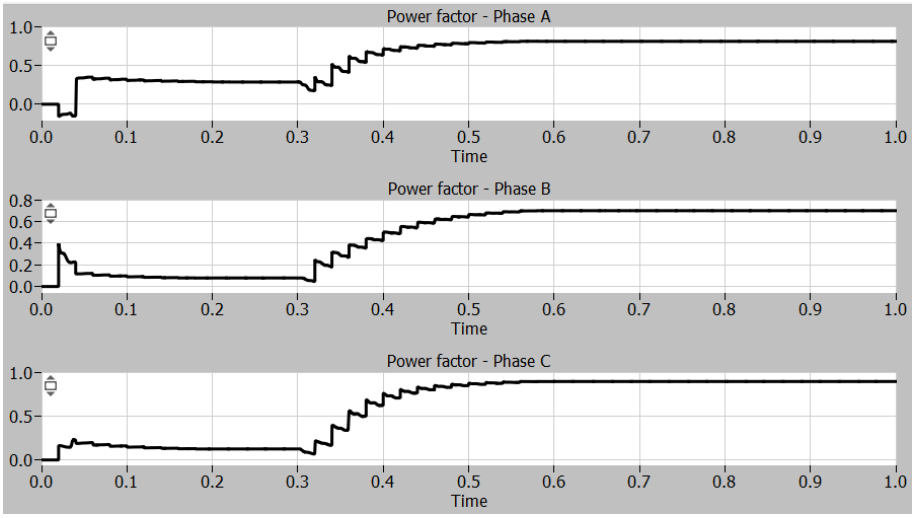

Figure 42: Power Factor of Phases A, B, and C with a decrease of 10% voltage magnitude of phase B

Figure 42 depicts the power factor for each phase. The accurate values of the power factor for each phase are documented in **Table 14**.

Table 14: Overview of power factor and current THD with unbalance change without trap filter

Case	Balanced	Magnitude change		Phase angle change	
Unbalance (%)	**0%**	**5%**	**10%**	**5%**	**10%**
Power factor – Phase A	0.81	0.82	0.82	0.88	0.90
Power factor – Phase B	0.81	0.77	0.70	0.81	0.79
Power factor – Phase C	0.81	0.86	0.90	0.71	0.53
THD_I	8.92%	9.75%	13.19%	18.60%	32.69%
ΔTHD_I	-	0.83%	4.27%	9.68%	23.77%

Table 14 shows an overview of the obtained results from the unbalance test. The magnitude and phase angle change clearly affect the distortion in the system negatively and an increase in THD is observed. Furthermore, a decrease in power factor is observed in phases B and C when imbalance is induced as phase angle change.

Analyzing the harmonic spectrum seen in **Figure 42** and the corresponding THD can be seen in **Table 14**, giving an indication of severe imbalance. The third harmonic current distortion is large, thereby indicating high imbalance.

12-pulse Thyristor Rectifier With Trap Filter

This section will perform a similar analysis with the trap filter connected. Imbalance will be induced to the topology, as either magnitude or phase angle. The test will highlight the effects of the trap filter and show the possible improvements that might appear when adding the trap filter.

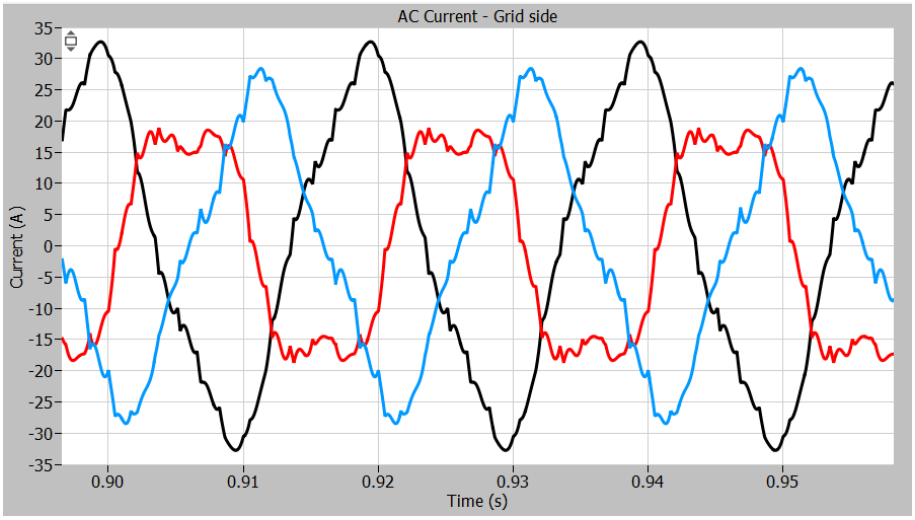

Figure 43: Current measurement with 10% decrease of voltage phase B with trap filter.

Figure 43 shows the current waveform under the condition of an unbalanced grid with a 10% dip in the magnitude of one of the phases. A high degree of unbalance and distortion is seen in the current waveform, which is also indicated by the high level of THD in all the three phases.

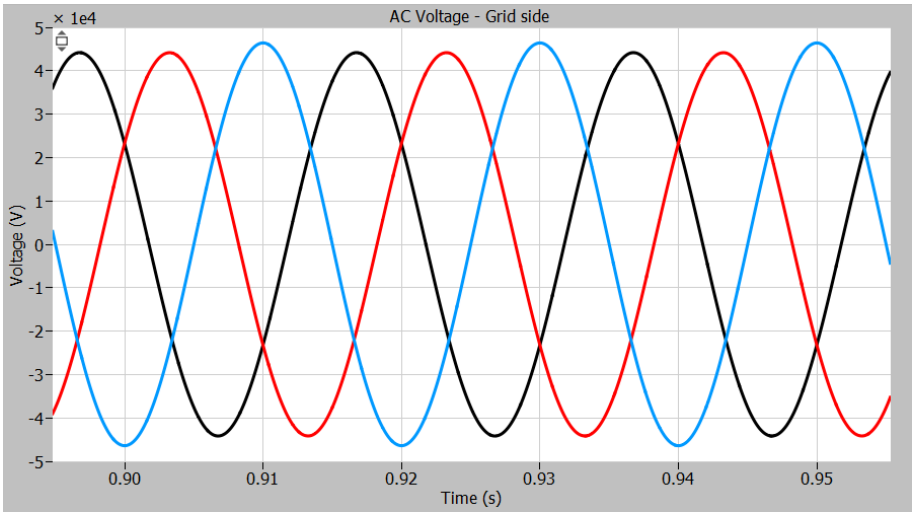

Figure 44: Voltage measurement with 10% decrease of voltage phase B with trap filter.

Figure 44 shows the voltage waveform under the condition of an unbalanced grid with a 10% dip in the magnitude of phase B. There is no change observed on the voltage or related THD compared to simulation without the passive trap filter.

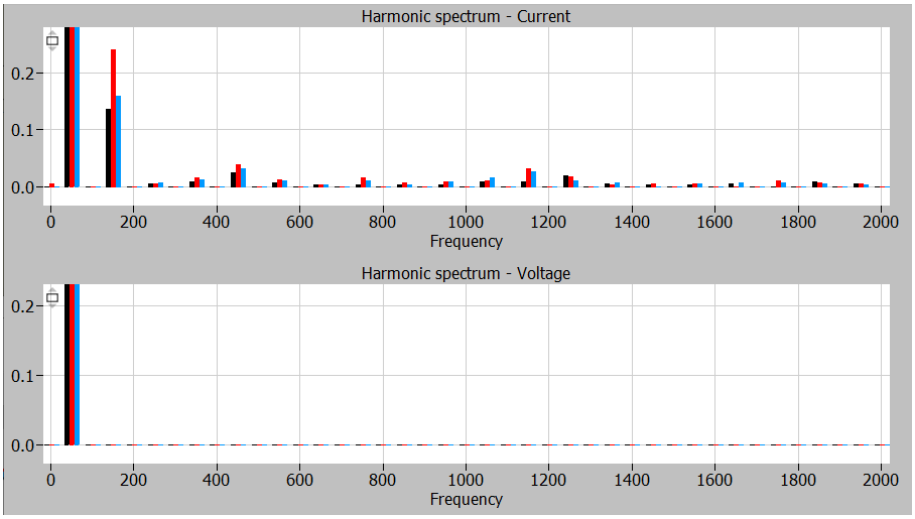

Figure 45: Harmonic spectrum of current and voltage with 10% decrease of voltage magnitude and trap filter. Normalized at fundamental frequency of 50 Hz

Figure 45 shows the harmonic spectrum of the current and voltage respectively. The imbalance has induced harmonic distortions to the system especially the harmonics of 3rd order. The third order harmonics are explained by the unbalance inducing a nonzero current in the neutral. This will cause an oscillating current to form and create a harmonic of third order. The odd harmonics are a sign of a symmetrical system.

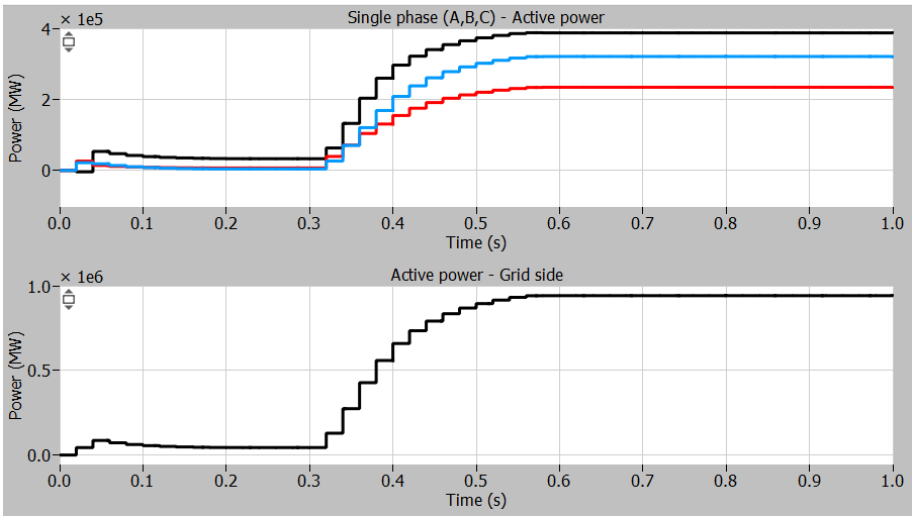

Figure 46: Active Power of Single Phases A, B & C & Total Grid Side Active Power with passive trap filter.

Figure 46 depicts the active power for each phase and total active power in the system. Compared to the topology without trap filter an increase in active power was noticed when imbalances were induced into the system. However, with the trap filters connected, the active power reduces to approximately 0.95 MW during unbalance. This active power reduction occurs due to components of the trap filter which draw some active power.

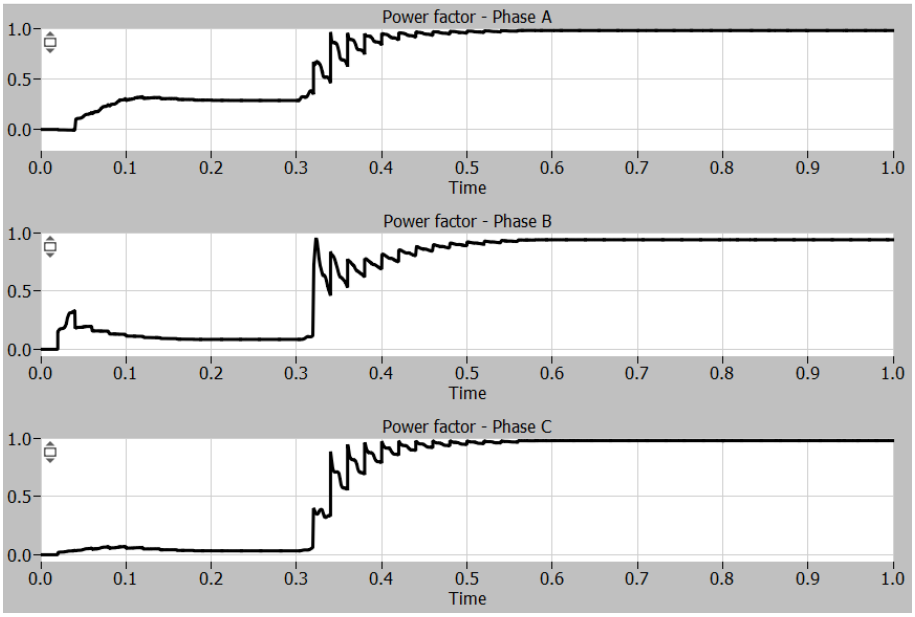

Figure 47: Power Factor of Phases A, B, and C with a decrease of 10% voltage magnitude of phase B with trap filter

Figure 47 depicts the power factors of each phase. All the power factors are close to unity. The actual values are displayed in **Table 15**.

Table 15: Comparison between unbalances in phase and magnitude with trap filter

Cases	Balanced	Magnitude change		Phase angle change	
Change	**0%**	**5%**	**10%**	**5%**	**10%**
Power factor – Phase A	0.99	0.99	0.98	0.98	0.94
Power factor – Phase B	0.99	0.98	0.94	0.97	0.93
Power factor – Phase C	0.99	0.99	0.98	0.95	0.77
$\boldsymbol{THD_I}$	3.64%	8.00%	13.96%	18.63%	32.78%
$\boldsymbol{\Delta\, THD_I}$	-	4,36%	10,32%	14,99%	29,14%

Table 15 depicts the power factor for each phase and the THD measurements from the different types of unbalances in the grid. The overall results with the trap filter seem to have improved the

entire topology. Hence it is able to remain stable even during the phase angle change of 10%. Furthermore, it can be observed that the topology is able to remain within the harmonic limits during a 5% decrease of magnitude which depicts its robustness.

3.1.4 Load Variation

This section will focus on the robustness of the each of the topologies. In order for a topology to be considered robust, the topology must be consistent, in the condition of partial loads. For the simulation with and without the trap filter, the input reference will be changed from 100% to 20% in decrements of 20% at a time.

12-Pulse Thyristor Rectifier Without Trap Filter

This section illustrates the test of load variation conducted on the 12-TR. Since the model uses current control loops, it is the reference current which needs to be altered in order to change power delivered across the P2X load. Since it is assumed that the load used in Haldor Topsøe setup will be fixed, the resistive load will not be altered during the simulation.

Table 16: Load Variation Analysis for the 12-TR

Load Variation	**100%**	**80%**	**60%**	**40%**	**20%**
Active power	1 MW	0.8 MW	0.6 MW	0.4 MW	0.2 MW
Power factor	0.82	0.73	0.62	0.51	0.35
$\boldsymbol{THD_I}$	8.92%	9.26%	9.50%	10.56%	10.78%
$\boldsymbol{\Delta\, THD_I}$	-	0.34%	0.58%	1.64%	1.86%

Table 16 documents the results from the various 12-TR load variation tests. It indicates a lower increase in current THD as the load decreases. Hence the topology operates with higher distortion at lower power levels. The power factor has a decreasing trend with decreasing output power.

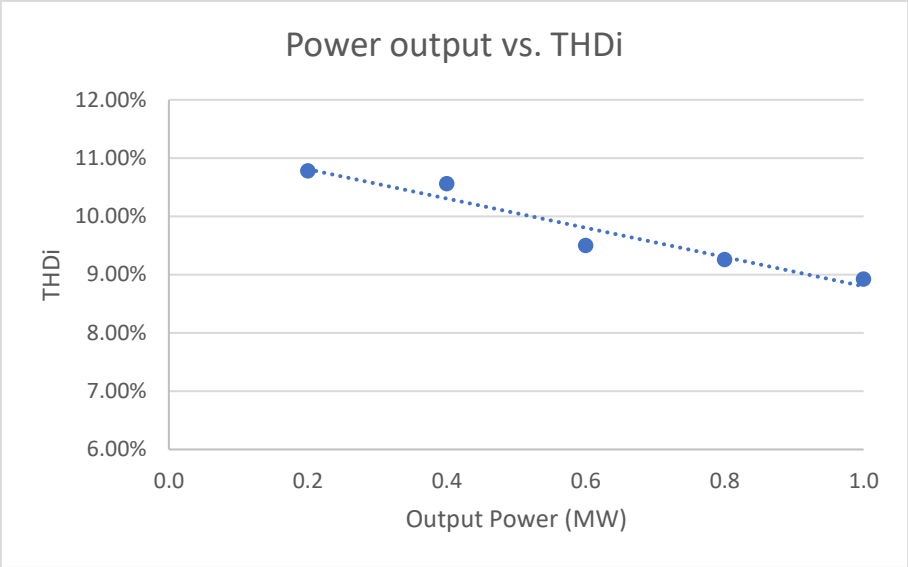

Figure 48: Power output vs THDi for the topology 12-TR without trap filter

Figure 48 depicts the trend of decreasing current distortion as the output power increases. The results are as expected since the 12-TR is known to operate suboptimal under partial load conditions.

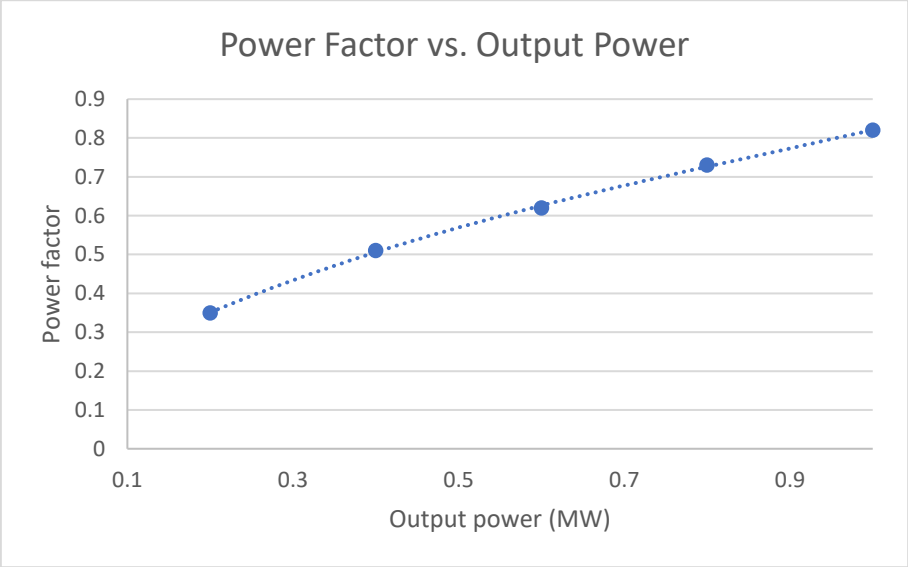

Figure 49: Output power vs power factor for 12-TR without trap filter

Figure 49 depicts the power factor for the 12-TR without trap filter under partial loading conditions. An increasing trend can be observed, as the power increases. Since there is no trap filter, the power factor remains unsatisfactory even at full loading conditions.

12-Pulse Thyristor Rectifier With Trap Filter

The load variation test is conducted in a similar manner as in the previous section, now with the trap filter connected, in order to test the effect of trap filter on the overall robustness of this topology.

Table 17: Load Variation Analysis for the 12-TR with passive trap filter

Load variation	100%	80%	60%	40%	20%
Active power	1 MW	0.8 MW	0.6 MW	0.4 MW	0.2 MW
Power factor	0.99	0.98	0.97	0.98	0.92
THD_I	3.64%	4.64%	4.96%	5.45%	6.06%
ΔTHD_I	-	1%	1.32%	1.81%	2,42%

Table 17 depicts the load variation analysis for the 12-TR with passive trap filter. The topology has improved both in terms of the power factor and the THDi, hence proving to be more stable and robust to external variations.

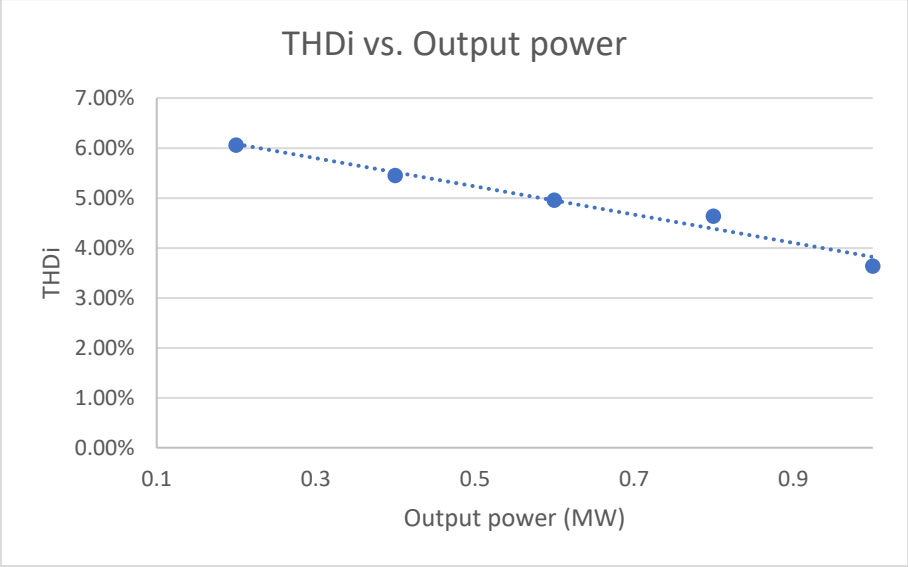

Figure 50: Load variation vs THD for the topology 12-TR, with passive trap filter

Figure 50 shows the linear decrease of current THD as the output power is increased. The current THD, THD_i is observed to be within the limits stated by IEE519 for the loads down to 0.6 MW. Thus, proving the remarkable effect of trap filters with regards to stability and robustness during load variations.

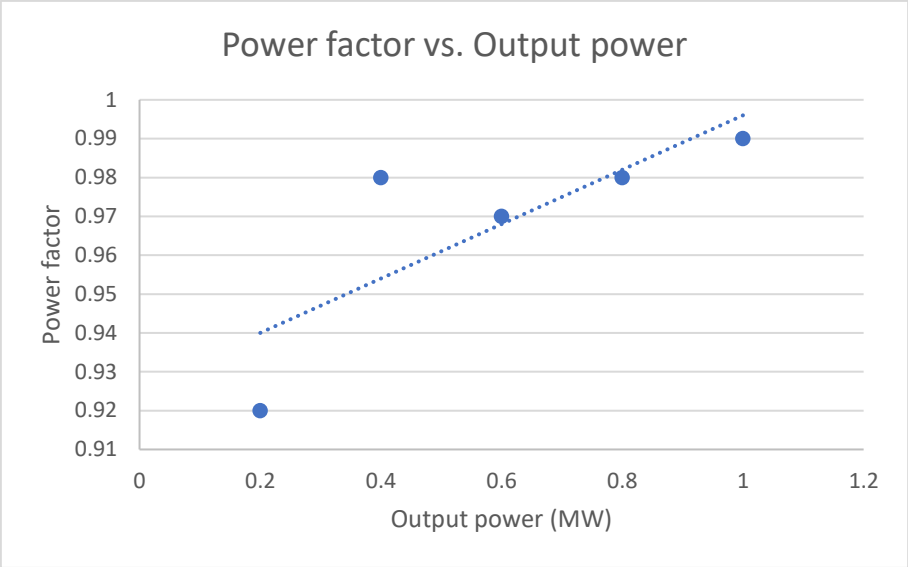

Figure 51: Load Variation vs Power Factor for 12-TR, with passive trap filter

The power factor vs output power graph is shown in **Figure 51**. The results indicate the stability and robustness of the model throughout the entire test after the addition of the trap filter. The power factor remains high, which is due to the trap filter absorbing the otherwise induced reactive power, which could be observed in the simulation model without the trap filter.

3.1.5 Efficiency Calculation

The Efficiency estimation requires information about commercial semi-conductors; therefore, it is necessary to obtain the ratings for each of the semi-conductors used in the topology, which were explained in **section 2.6**. The semi-conductors in the topology, will be altered from completely ideal to non-ideal commercialized semi-conductors. Furthermore, the winding resistance parameter of the transformer will be changed to more practical values. The values obtained for the winding resistance will be used in all the topologies for the efficiency calculation.

12-Pulse Thyristor Rectifier Without Trap Filter

This section conducts the efficiency test without the trap filter. The simulation model is altered by creating a 'thermal description' of the thyristors based on commercial datasheets. The thermal description is made by using 'PLECS simulation tools', by importing the 'conduction loss' curve from the datasheet of the commercial thyristor with device name 'ND421825'. The change will affect the thyristors; hence the efficiency will be altered, resembling the efficiency of a non-ideal system.

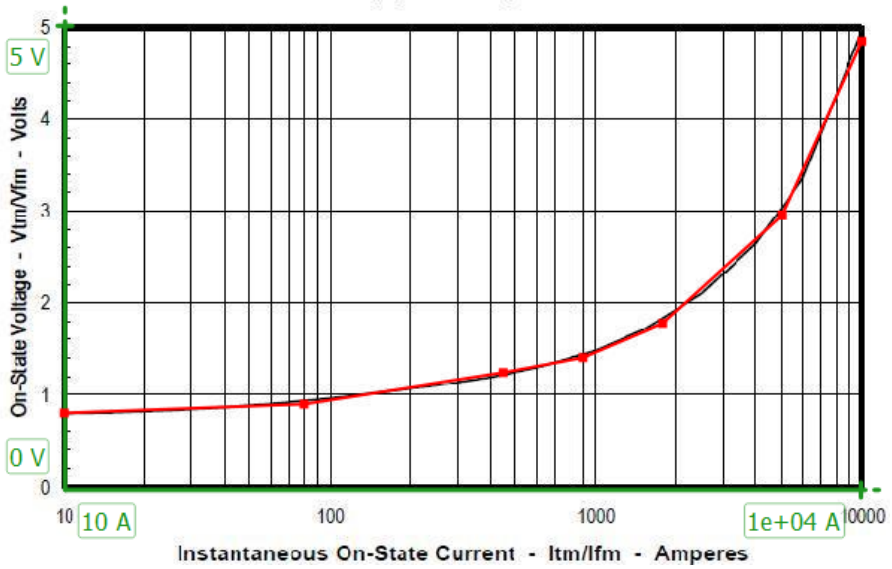

Figure 52: Thermal model of the conduction loss in the thyristor [34].

Figure 52 depicts the changes made in the 'thermal description' of the thyristors. By adding the image of 'Maximum on-state forward voltage drop' from the datasheet of the ND421825, it is possible to model the thyristors according to the actual datasheet and hence obtain an almost identical maximum 'on-state' forward voltage drop of the commercial thyristors. However, it must be noted that there a many possible alterations which can be implemented by this simulation tool. As previously explained in **section 2.6.1**, the thyristor's power loss is dependent on the forward voltage. Therefore, this particular description of the thyristor is necessary.

Table 18: Efficiency estimation of the 12-pulse thyristor rectifier without trap filter

Load Variation	100%	80%	60%	40%	20%
Input active power	1.00 MW	0.81 MW	0.61 MW	0.41 MW	0.20 MW
Output active power	0.99 MW	0.80 MW	0.60 MW	0.40 MW	0.20 MW
Efficiency	98.95%	98.82%	98.81%	98.68%	98.38%

Table 18 shows the efficiency estimation of the 12-TR. From the table a decreasing trend of efficiency is seen when operating in partial load. This is an indication that the topology is most efficient when operating at full load conditions, which would be expected of the 12-TR. However, the topology shows an overall good efficiency at any given load.

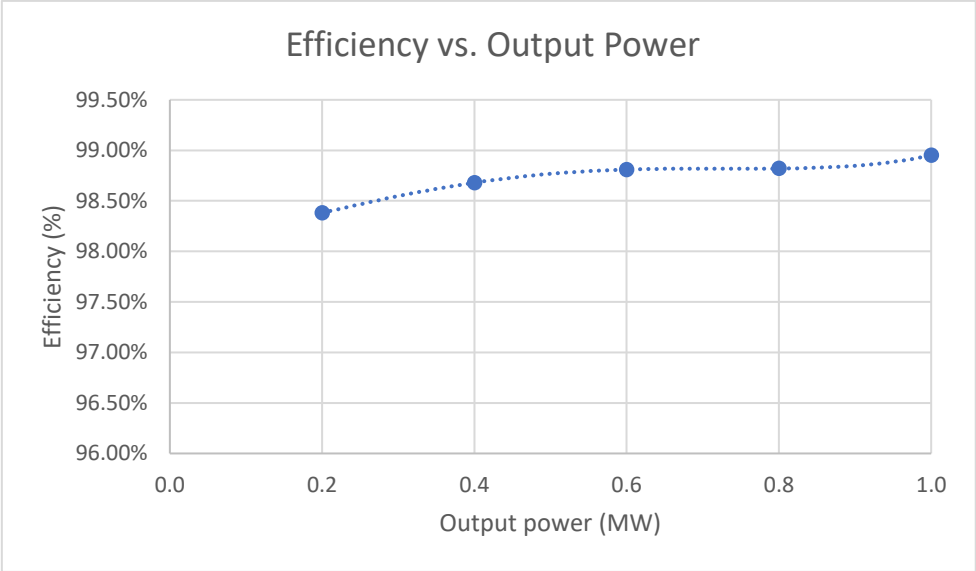

Figure 53: Efficiency vs power graph for 12-TR

Figure 53 illustrates the efficiency vs. output DC-power, which was also shown in the previous table. As mentioned, an increase of efficiency is seen when increasing the DC-power.

12-Pulse Thyristor Rectifier With Trap Filter

This section conducts the test with the trap filter connected. The same commercial thyristor model as seen in Figure 52**Figure 52** will be implemented to the system and the efficiency will be measured again in order to investigate the effect of trap filter on the efficiency.

Table 19: Efficiency estimation of the 12-pulse thyristor rectifier with trap filter

Load variation	100%	80%	60%	40%	20%
Input Active power	1.01 MW	0.81 MW	0.61 MW	0.41 MW	0.20 MW
Output Active power	0.99 MW	0.80 MW	0.60 MW	0.40 MW	0.20 MW
Efficiency	98.94%	98.89%	98.81%	98.66%	98.35%

Table 19 shows almost identical results to the 12-TR in contrast to the case without a filter. Hence the graph shown in **Figure 54** shows an almost identical trend compared to that seen in the previous section. Thus, the need to analyze efficiency with and without the filter in the following topologies will be omitted.

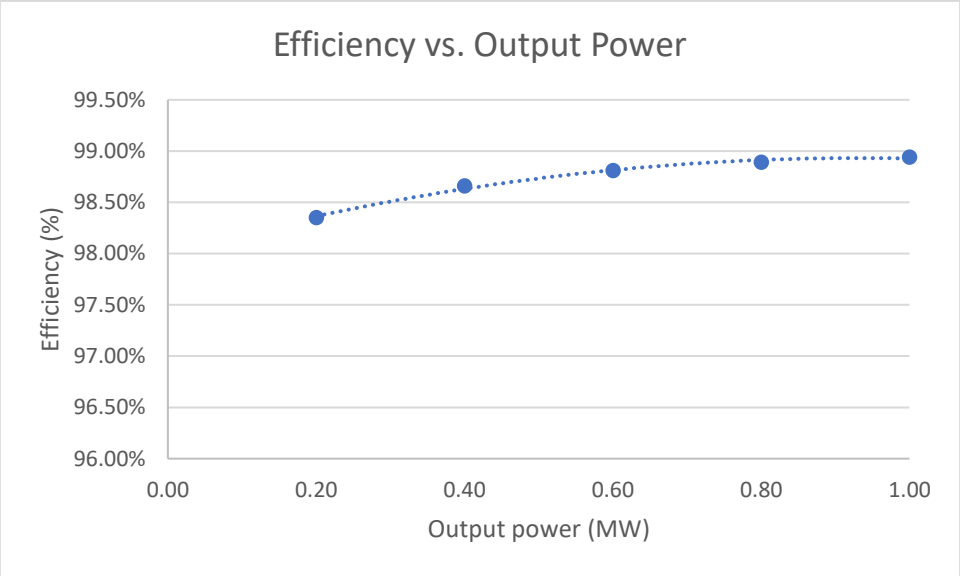

Figure 54: Efficiency vs power

3.2 12-pulse Diode Rectifier with Multi-Phase Chopper (12-DRMC)

12-Pulse Diode Rectifier with Multiphase Chopper (12-DRMC) in one of the common topologies used for the P2X systems. In this section the results from the simulated 12-DRMC topology have been presented with their analysis. The simulations include various tests which investigate the overall performance of the topology. The simulations have been carried out with and without the filter, which indicate the importance of using the filters.

Table 20 & **Table 21** document the component parameters and control parameters used in all simulation tests of the 12-DRMC, respectively.

Table 20: parameters used in components of 12-DRMC.

Parameters of control scheme	Values
V_{Grid}	33 kV
L_{Grid}	1^{-9} H
L_{In}	525^{-6} H
L_{DC}	1000^{-6} H
V_{DC}	1 kV
C_L	100^{-3} F
C_{DC}	50^{-6} F
R_{Load}	1 Ω

Table 21: Parameters used in control system for 12-DRMC.

Parameters of control scheme	Values
K_{P1}	0.005
K_{I1}	20
K_{P2}	10
K_{I2}	2000

The parameters of the **Table 20** & **Table 21** refer to **Figure 6** and **Figure 8** respectively.

3.2.1 Output under ideal full load conditions

This section discusses the output from the 12-DRMC topology under the ideal full load conditions, where the general output will be presented. The parameters are inspected by means of the simulations to set a reference for the further tests to be performed. The results presented in this section will revolve around full load ideal simulations, on the output DC side of the P2X plant.

For the case of 12-DRMC, the output power of 1MW with a voltage of 1 kV was successfully achieved consequently followed by the current of 1 kA. **Figure 55, Figure 56** & Figure 57**Figure 57** show the plots of the output current, voltage & power respectively.

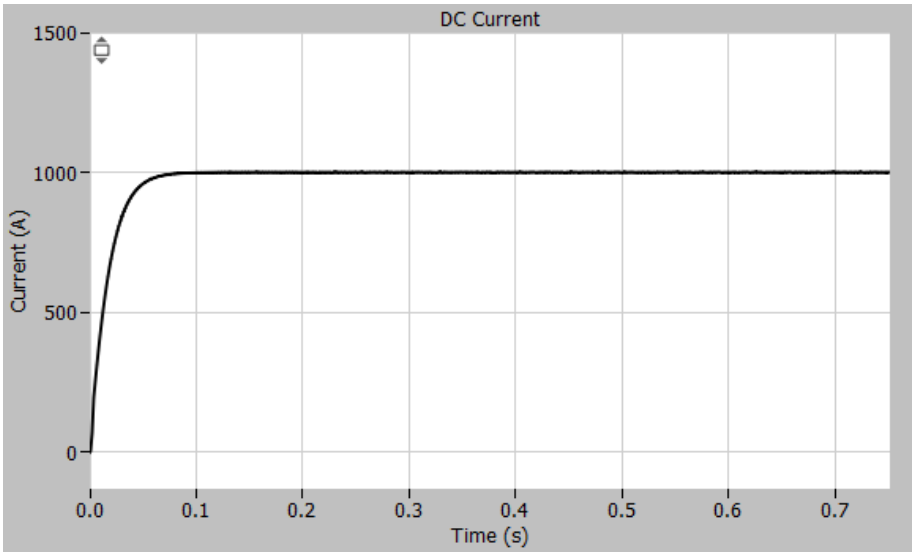

Figure 55: DC Current from 12-DRMC

Figure 55 displays the output DC current to the P2X system from the 12-DRMC topology. The current adjusts itself according to the power transferred which amounts to 1 MW.

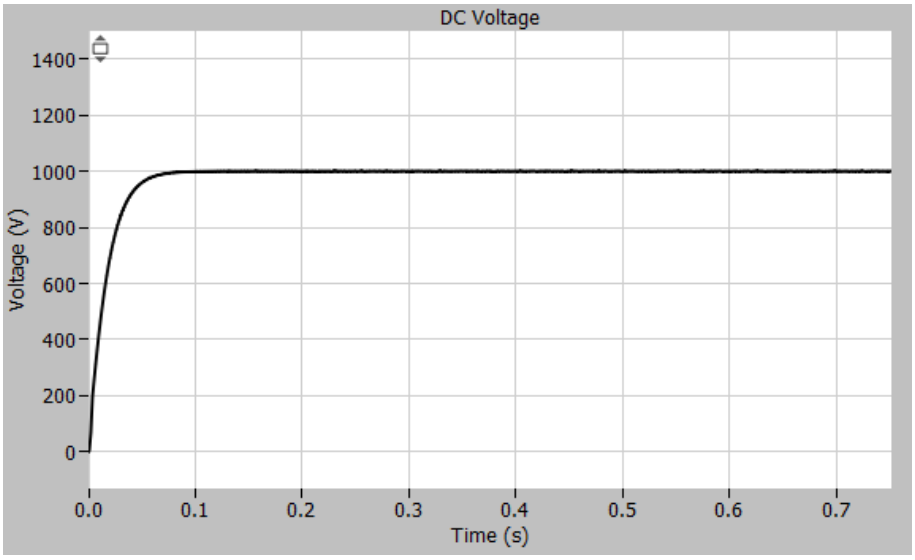

Figure 56: DC Voltage from 12-DRMC

Figure 56 depicts the output DC voltage, which is controlled by the controller to maintain a value of 1 kV.

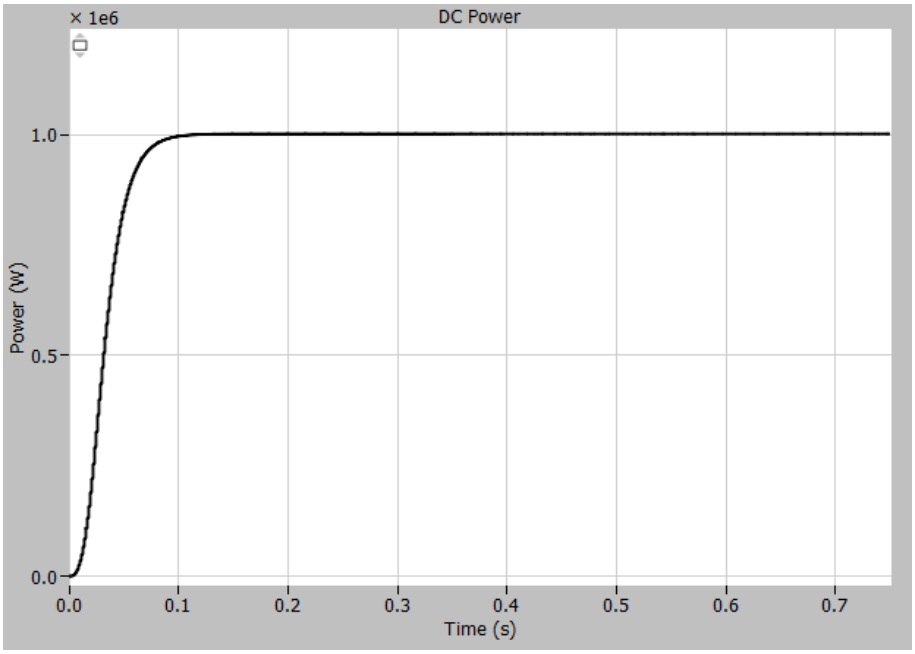

Figure 57: Power at the DC side from 12-DRMC

Figure 57 shows the output power curve, which transfers 1MW of power across the P2X plant.

Table 22 documents the general parameters of the 12-DRMC topology with their values and units under the ideal full load conditions.

Table 22: Relevant parameters of the 12-DRMC topology

Parameters	Value	Unit
RMS current grid-side	18.59	A
RMS voltage grid-side	33	kV
Active power grid-side	1.00	MW
Apparent power grid-side	1.05	MVAr
Power factor grid-side	0.97	-
Current DC-side	1.00	kA
Voltage DC-side	1.00	kV
Active power DC-side	1.00	MW

3.2.2 Harmonic Analysis

A harmonic analysis is to be conducted for 12-DRMC topology, in order to check if it can operate within the given requirements stated in **section 1.3.** The harmonic analysis test was conducted with and without the filters and the analysis is provided in the next subsections.

12-Pulse Diode Rectifier With Multi-Phase Chopper Without trap filter

The THD analysis for the 12-DRMC has been conducted from the measurements taken before the 12-Pulse transformer on the grid side. The THD has been directly calculated by the 'THD' block in the PLECS platform. **Figure 58**Figure 58 shows the measurements of the current on the grid side of the topology.

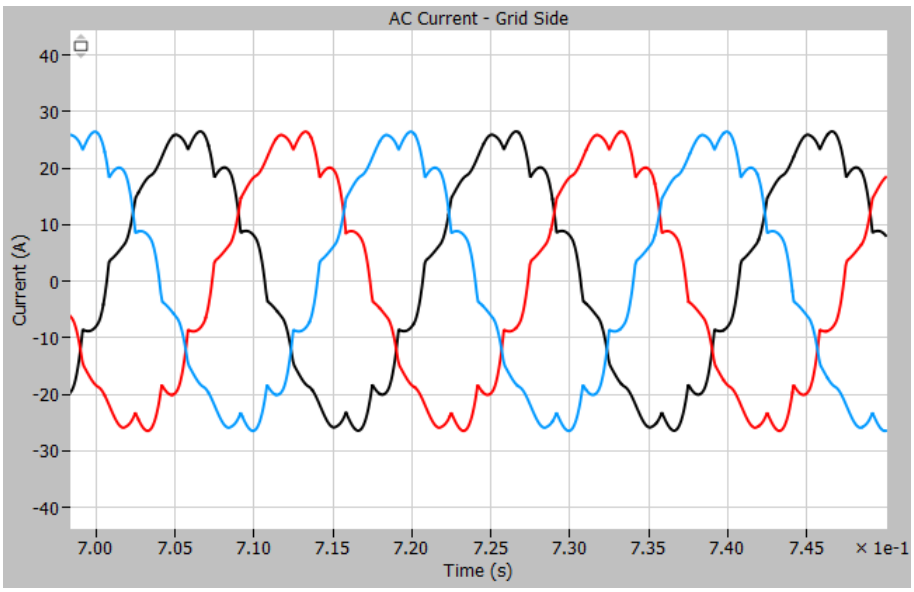

Figure 58: Current measurement on the grid side for 12-DRMC

The AC current waveform above, shows a distorted current which is due to the presence of the harmonics in it. The THD is calculated to approximately 8% which is above the limits of 'IEEE 519'

(5%). This harmonic level indicates that a passive filter is necessary in order for the topology to connect to the grid.

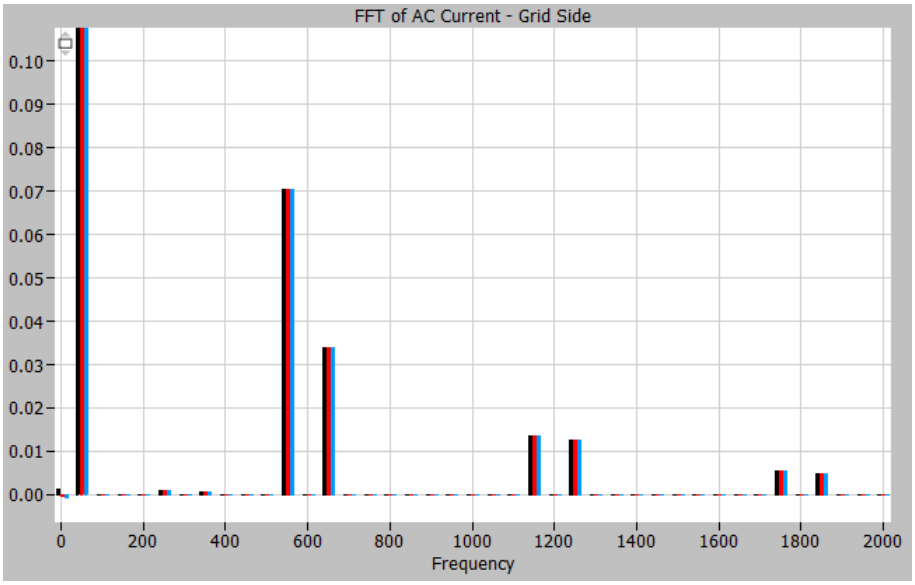

Figure 59: Harmonic spectrum of grid side current, without trap filter. Normalized at fundamental frequency of 50 Hz

Table 23: 12 ± 1 Harmonic Values & THD Value

Harmonic(s)	Value
11th Harmonic	7.02 %
13th Harmonic	3.39 %
23rd Harmonic	1.34 %
25th harmonic	1.24 %
35th harmonic	0.53 %
37th harmonic	0.47 %
THD	8.07 %

Figure 59 shows harmonic spectrum of the grid side current. By the aid of PLECS it is possible to conduct a FFT analysis. The analysis was conducted on the grid current waveform, from the fundamental till the 40th harmonic order.

In current harmonic spectrum presented in **Figure 59**, there is a significant presence of the 11th & 13th (12 ± 1) harmonics which have values of approximately 7% and 3.4% of the fundamental current respectively, which is expected due to the existence of 12 pulse converter used in this topology. These values indicate a requirement for trap filters to suppress the harmonics of the 11th & 13th order, which can reduce the THD levels to the required limits. **Table 23** illustrates the value of

harmonics of 12n ± 1 order and the THD of the 12-DRMC topology, where the values of n are 1, 2 & 3.

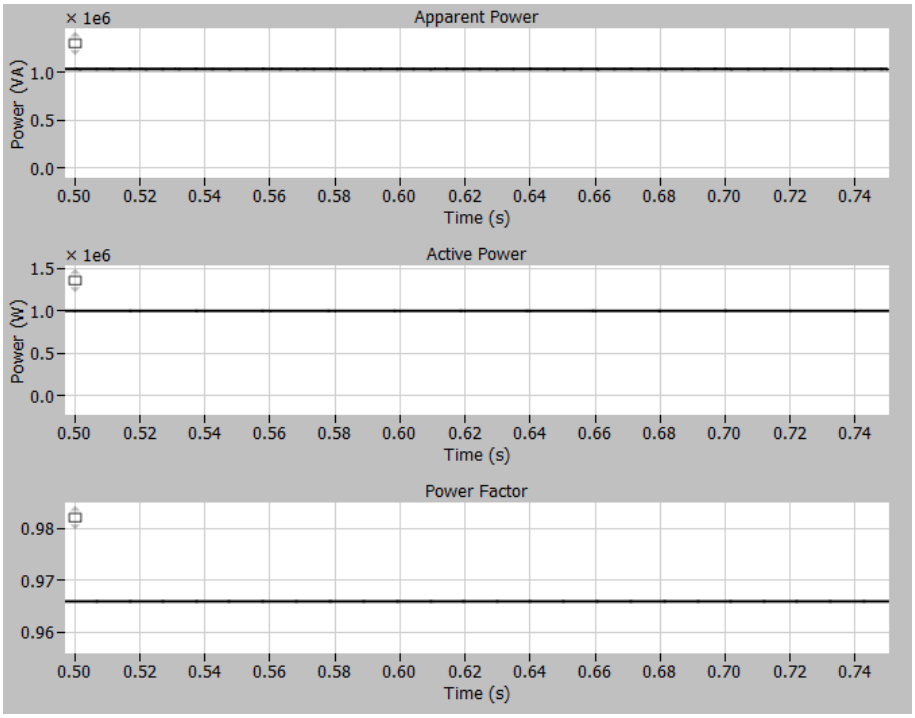

Figure 60: Plots of Apparent power (S), Active power (P) and Power factor (PF).

Figure 60 show the plots of Apparent Power, Active Power & Power Factor in plots 1,2 & 3 respectively. The values of Apparent Power & Active Power in the plots follow the values of the **Table 22**. The power factor maintains the value of around 0.97 at the steady state which is a huge improvement over the 12-TR topology. The Power Factor could be possibly improved further by using the filters.

12-Pulse Diode Rectifier With Multi-Phase Chopper With trap filter

In this section, the harmonic analysis will be implemented using the trap filters designed to suppress the 11^{th} & 13^{th} harmonics. **Figure 61** displays the current waveform while using the filters.

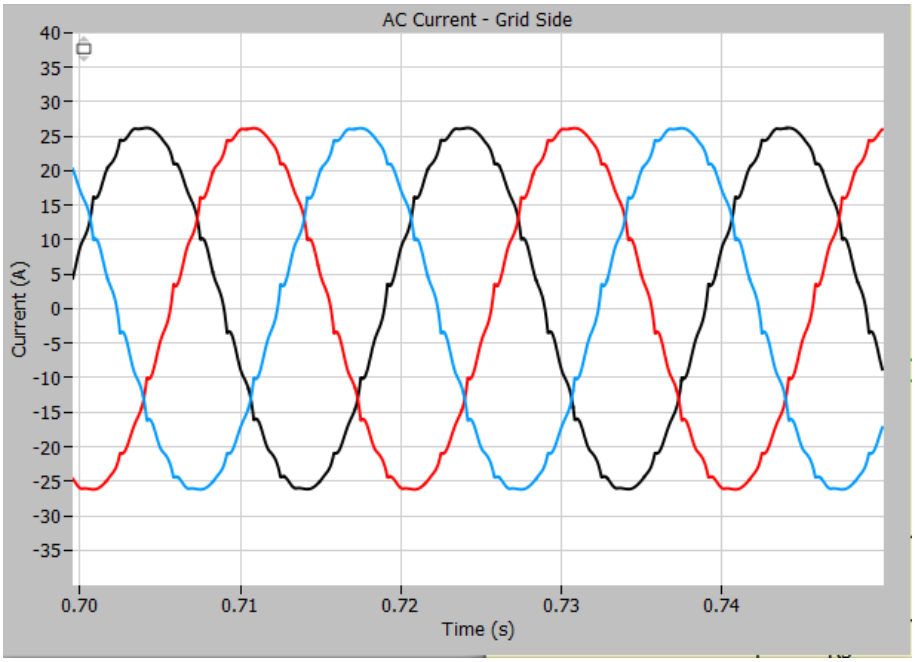

Figure 61: Current measurement on the grid side for 12-DRMC with Filter

The AC current waveform in **Figure 61** is almost purely sinusoidal which indicates the successful effect of the filters. The THD is measured to be just approximately 2% which is within the limits of IEEE standards (5%).

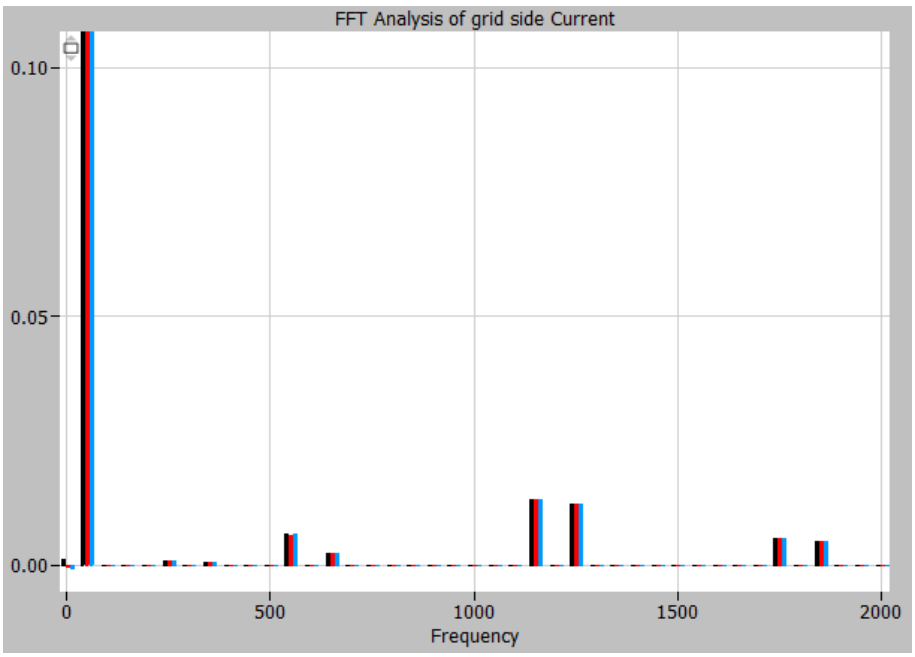

Figure 62: Harmonic spectrum of grid side current with Trap Filters. Normalized at fundamental frequency of 50 Hz

Figure 62 shows the harmonic spectrum of the 12-DRMC topology the 11^{th} & the 13^{th} harmonics have been successfully suppressed, which is observed from both the figure above and **Table 24**. The

value of harmonics of 12n ± 1 order and the THD of the 12-DRMC topology, where the value of n is 1,2 & 3 are shown in the table below.

Table 24: 12 ± 1 Harmonic Values & THD Value

Harmonic(s)	Value
11th Harmonic	0.63 %
13th Harmonic	0.23 %
23rd Harmonic	1.31 %
25th harmonic	1.21 %
35th harmonic	0.52 %
37th harmonic	0.46 %
THD	2.12 %

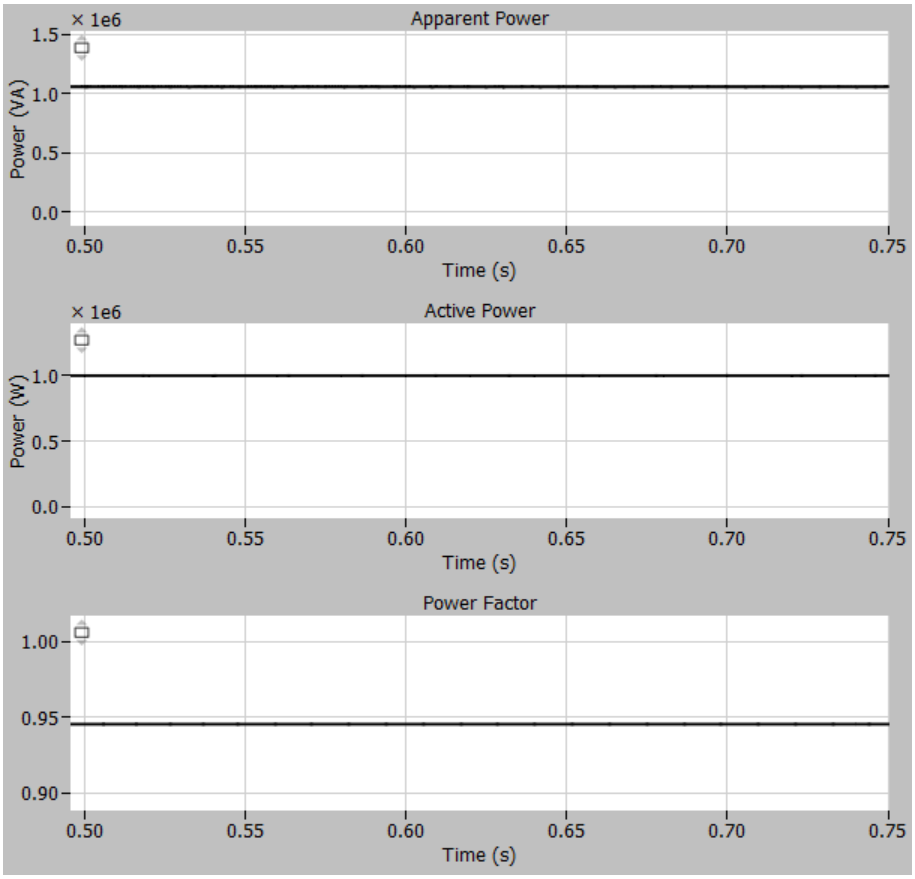

Figure 63: Plots of Apparent power (S), Active power (P) and Power factor (PF).

Figure 63 shows the plots of Apparent Power, Active Power & Power Factor in plots 1,2 & 3 respectively. The values of Apparent Power & Active Power in the plots follow the values of **Table 22**Table 22. The power factor with trap filter is 0.95 at the steady state.

3.2.3 Unbalanced Grid

To study the unbalanced conditions of the 12-DRMC topology, the magnitude, and the phase angle of phase B have been decreased by 5% and 10%; then the simulation has been conducted. Thus, the response of the grid will be examined for the overall power quality under the terms of power factor and THD.

12-Pulse Diode Rectifier With Multi-Phase Chopper Without Trap Filter

To simulate the unbalanced load conditions for the topology of 12-DRMC, phase B of the 3-Phase grid has been changed by 5% & 10% for both the phase angle and the phase magnitude. The results of the changes introduced in the phase angle and the phase magnitude has been investigated in this section.

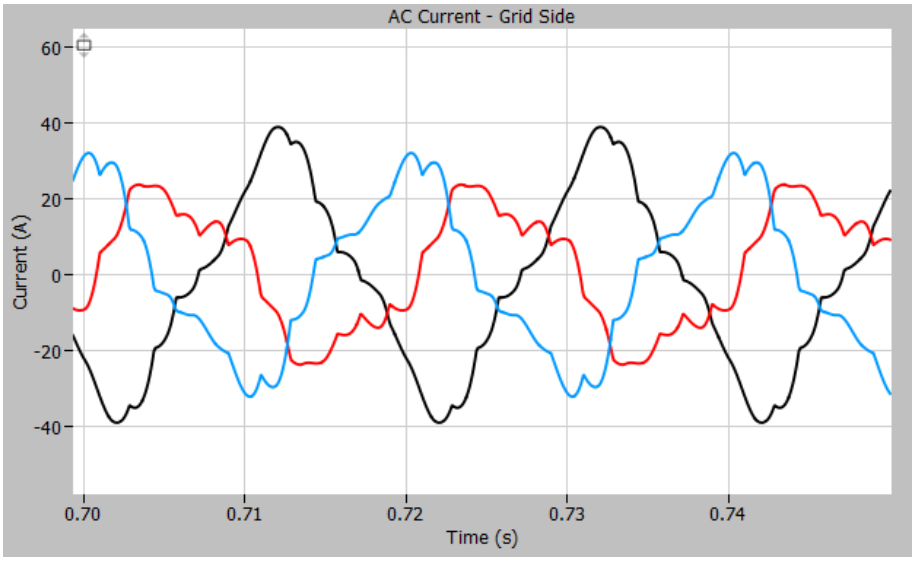

Figure 64: Current measurement with 10% decrease of voltage magnitude phase B without trap filter.

Figure 64 shows the AC grid side current for the case with a 10% decrease in the voltage magnitude for phase B. Furthermore, **Figure 65** shows the grid side voltage with one of the phases having a 10% magnitude dip.

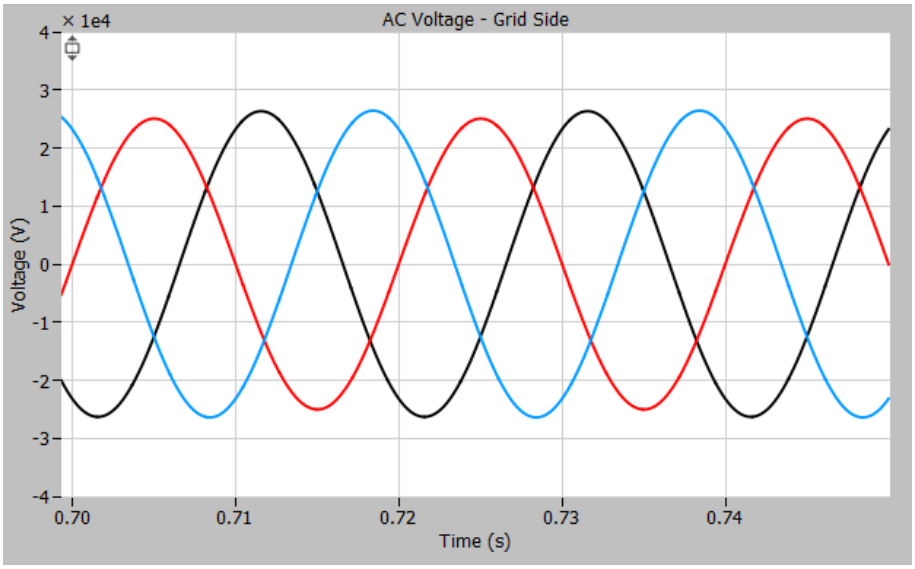

Figure 65: Voltage measurement with 10% decrease of voltage magnitude phase B without trap filter.

When analysing **Figure 64**, the grid currents show clear indications of unbalance. The current waveforms are highly distorted with different amplitudes. The voltage waveforms have difference in the magnitudes due to the injected unbalance as seen in **Figure 65**.

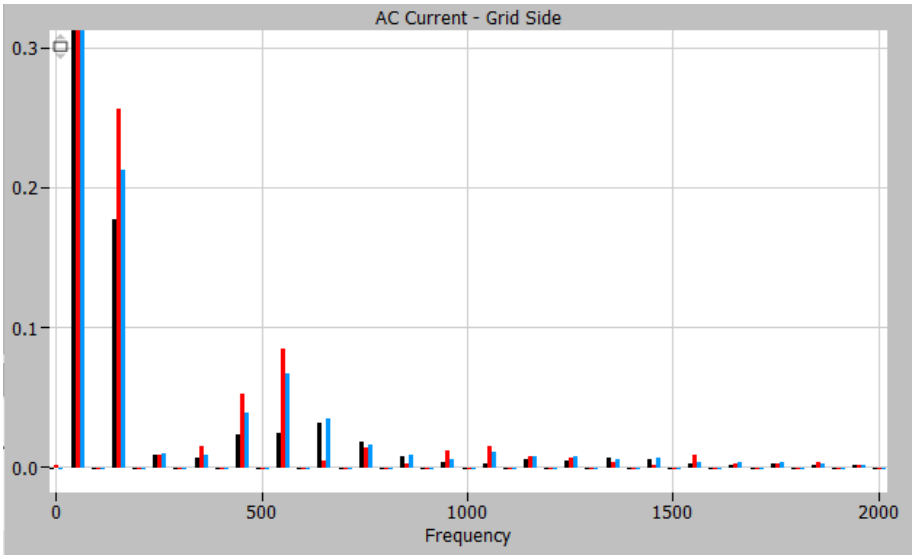

Figure 66: Grid Side Current Harmonic spectrum with 10% magnitude decrease in phase B. Normalized to fundamental frequency of 50 Hz

Figure 66 displays the harmonic spectrum of the 12-DRMC topology under the unbalanced condition. The FFT tool in PLECS has been used for the harmonic analysis; it displays a significant rise of the harmonics and especially the 3rd harmonic, with a small increase in the 9th harmonic, indicating a presence of 3n harmonics where n is a positive odd integer. Also, the effect of the

unbalance results in different magnitudes of harmonics in each of the three phases as noticed earlier in the 12-TR topology as well.

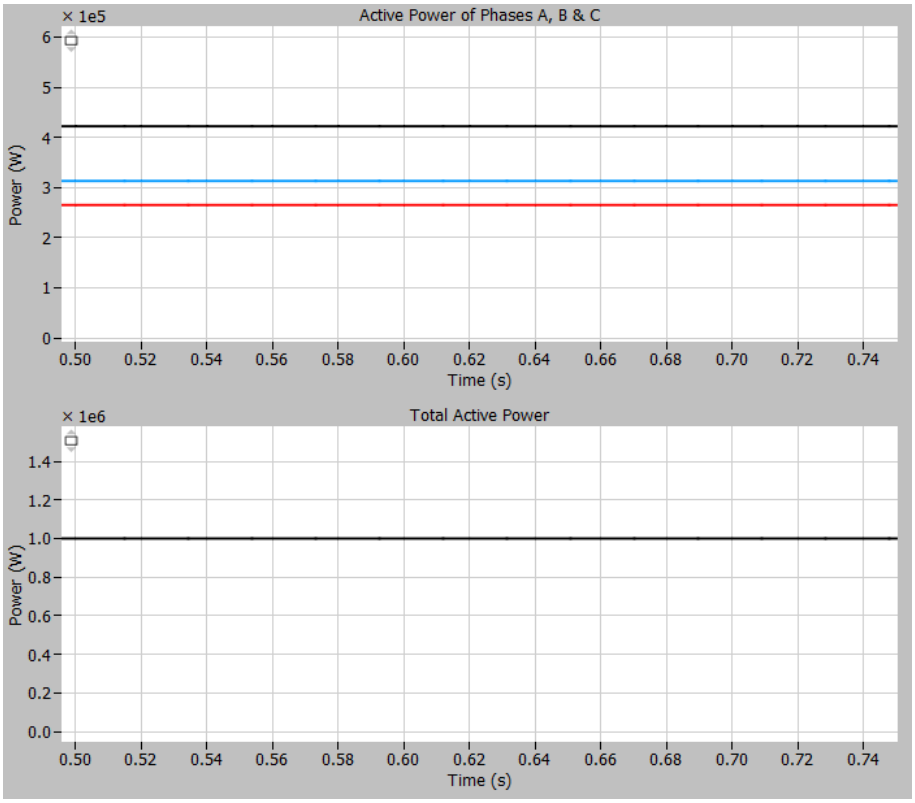

Figure 67: Active Power of Single Phases A, B & C & Total Grid Side Active Power

Plot 1 in the **Figure 67** shows active power of single phases A, B & C under the unbalanced condition. The power carried by each phase is unbalanced, as some of the phases are increased compared to the case of the balanced condition, which should be around 333.33 kW (1MW/3) for each phase. From Plot 2, the total active power transferred from the grid side can be seen which fulfils the requirements of the load. Even though there is a severe unbalance on the grid side, the 12-DRMC topology can successfully deliver the power of 1MW to the load by adjusting the power among the different phases.

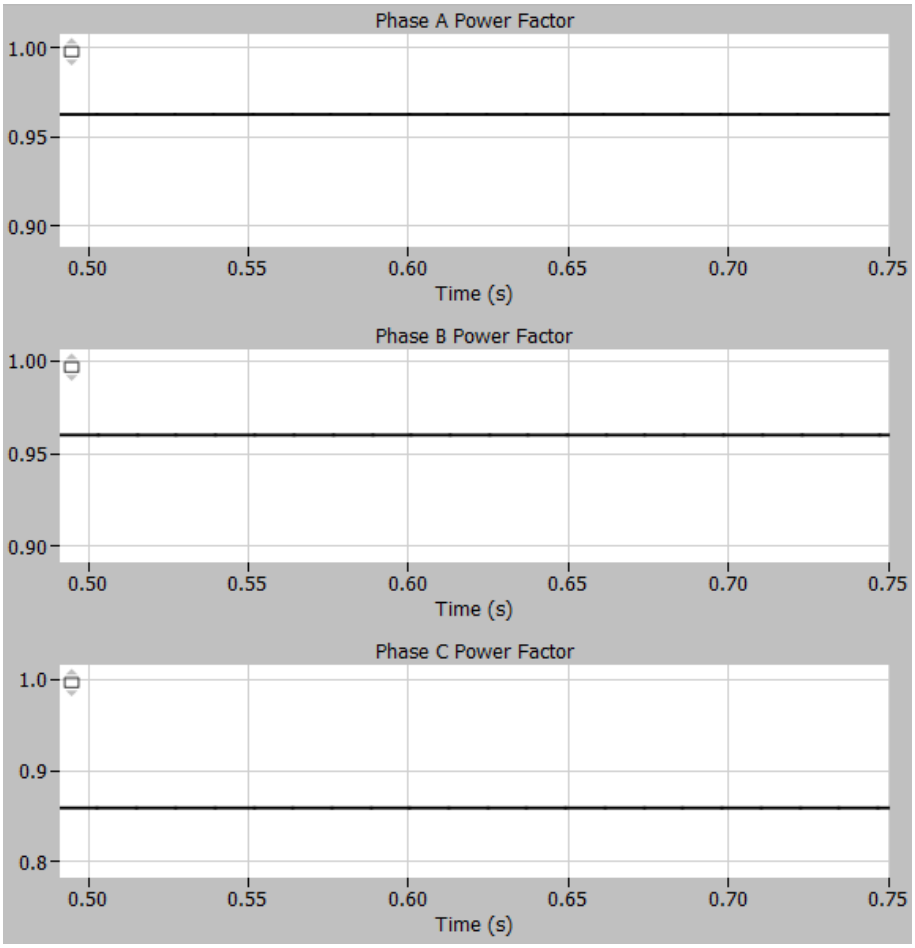

Figure 68: Power Factor of Phases A, B & C

Figure 68 shows the Power Factors of Phases A, B & C on the grid side during the unbalanced condition. From the balanced condition, the power factor doesn't change significantly in the phase A & Phase B, but it drops significantly for phase C due to the unbalanced grid.

Table 25: Overview of power factor and current THD with unbalance change

Operation conditions	Balanced	Magnitude change		Phase angle change	
Unbalance (%)	**0%**	**5%**	**10%**	**5%**	**10%**
Power factor – Phase A	0.97	0.97	0.96	0.97	0.87
Power factor – Phase B	0.97	0.97	0.96	0.85	0.63
Power factor – Phase C	0.97	0.9	0.86	0.94	0.90
$\boldsymbol{THD_I}$	8.07 %	11.74 %	18.44 %	19.58 %	31.31 %
$\boldsymbol{\Delta\, THD_I}$	-	3.31 %	9.54 %	10.74 %	22.09 %

Table 25 documents the power factors of phases A, B & C, as well as THDi under different unbalanced conditions. As expected, the changes are less severe under 5% unbalance of either

phase angle or magnitude, but the phase changes seem more severe compared to the magnitude change. For the change of 10%, the changes are more severe as contemplated, but despite the unbalances the 12-DRMC provides 1MW power to the load.

12-Pulse Diode Rectifier With Multi-Phase Chopper With trap filter

In the last section the unbalanced condition was analyzed for the 12-DRMC without the trap filters. Similar analysis will be performed in this section but including the trap filters suppressing the harmonics present in the system.

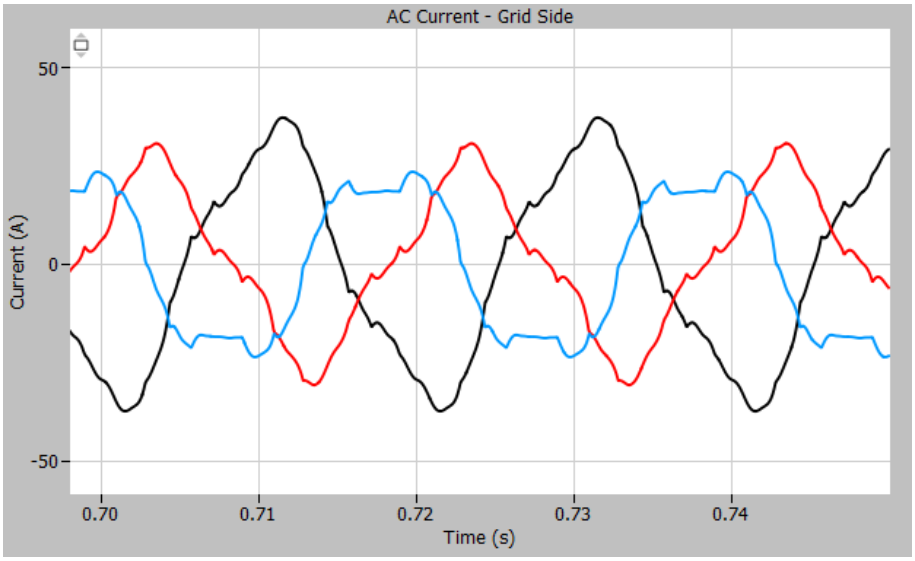

Figure 69: Current measurement with 10% decrease of voltage phase B with trap filter

Figure 69 displays the AC grid side current for the case with a 10% decrease in the voltage magnitude for one of the phases. The waveforms in the case seem less distorted that the previous case (without filters), but the unbalance between the phases is lucid. **Figure 70** further shows the grid side voltage with one of the phases having a 10% magnitude dip.

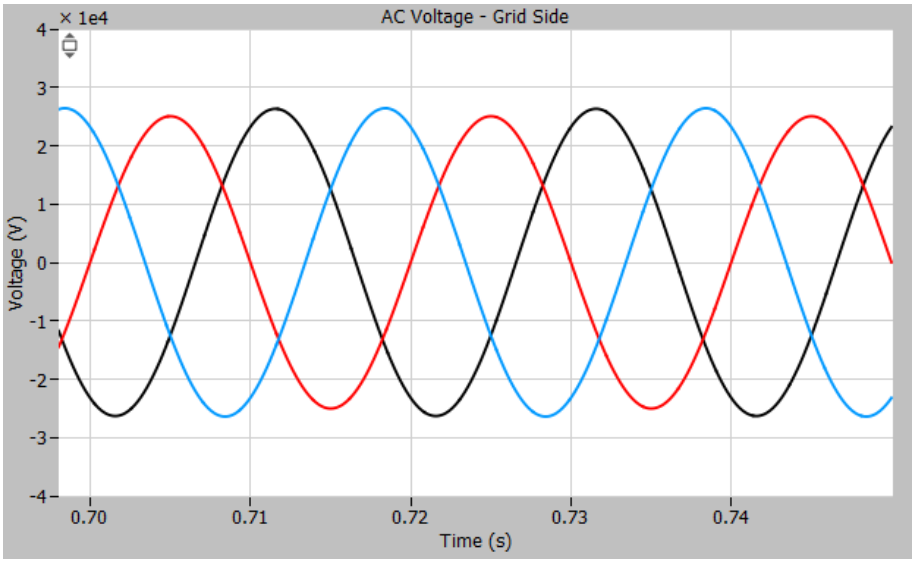

Figure 70: Voltage measurement with 10% decrease of voltage phase B without trap filter

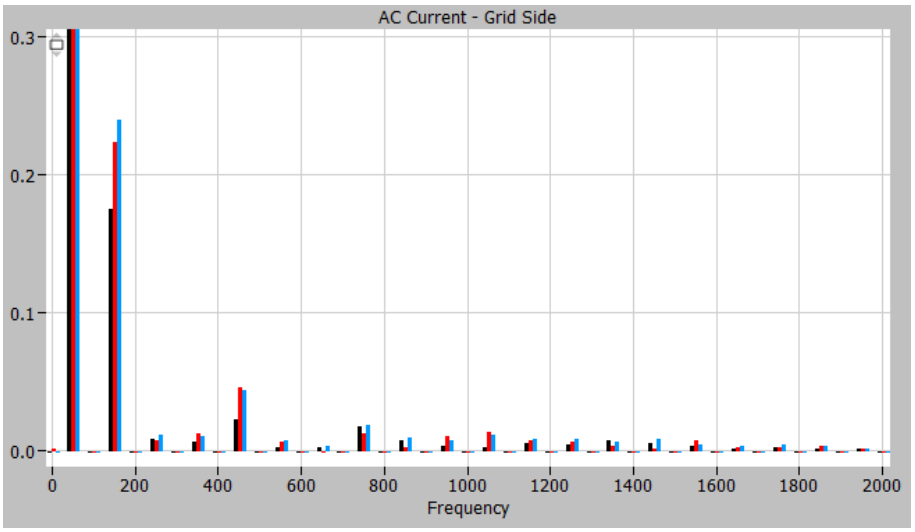

Figure 71: Grid Side Current Harmonic spectrum with 10% magnitude decrease in phase B with trap filters. Normalized to fundamental frequency of 50 Hz

Figure 71 shows the harmonic spectrum of the 12-DRMC with the filters during unbalanced grid and there is no presence of 11^{th} & 13^{th} harmonics as was in **Figure 66**Figure 66. The 11^{th} and 13^{th} harmonics are filtered out but there is still significant presence of the 3^{rd} harmonics and multiples of 3^{rd} harmonics present. Due to unbalance, the harmonic values for each phase are different represented by black, red, and blue colors.

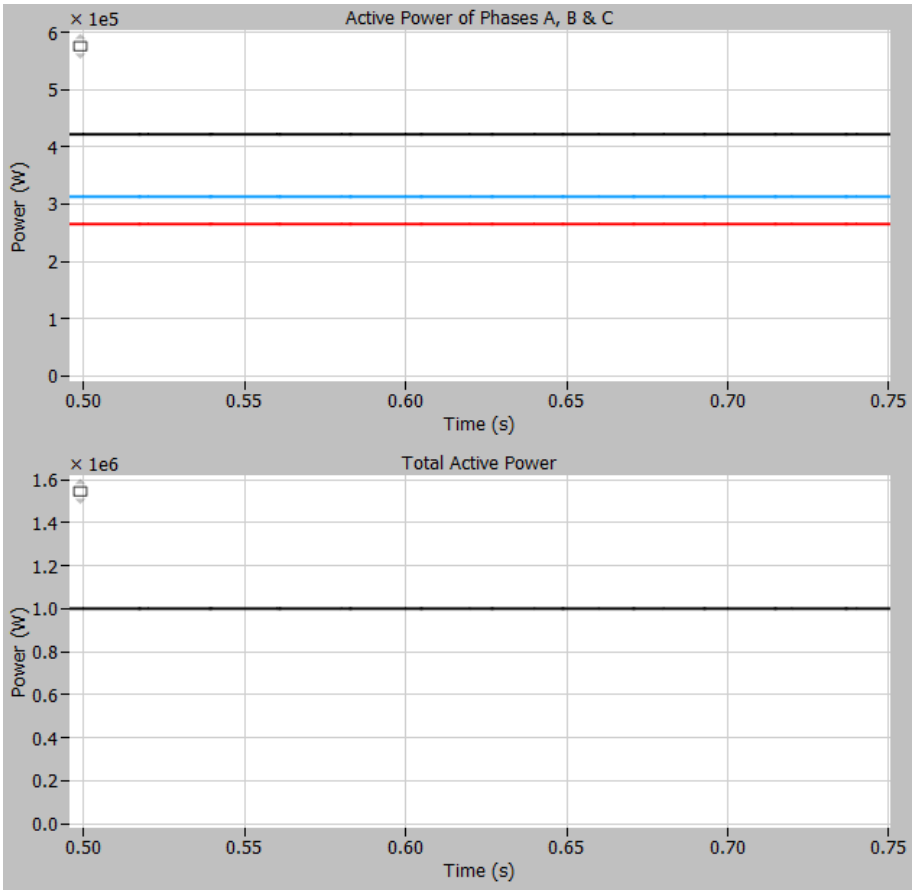

Figure 72: Active Power of Single Phases A, B & C & Total Grid Side Active Power

Like the previous case, 12-DRMC transfers 1MW active power across the P2X plant, but due to unbalance in the grid the power transfer is unequal in each phase as shown in **Figure 72**.

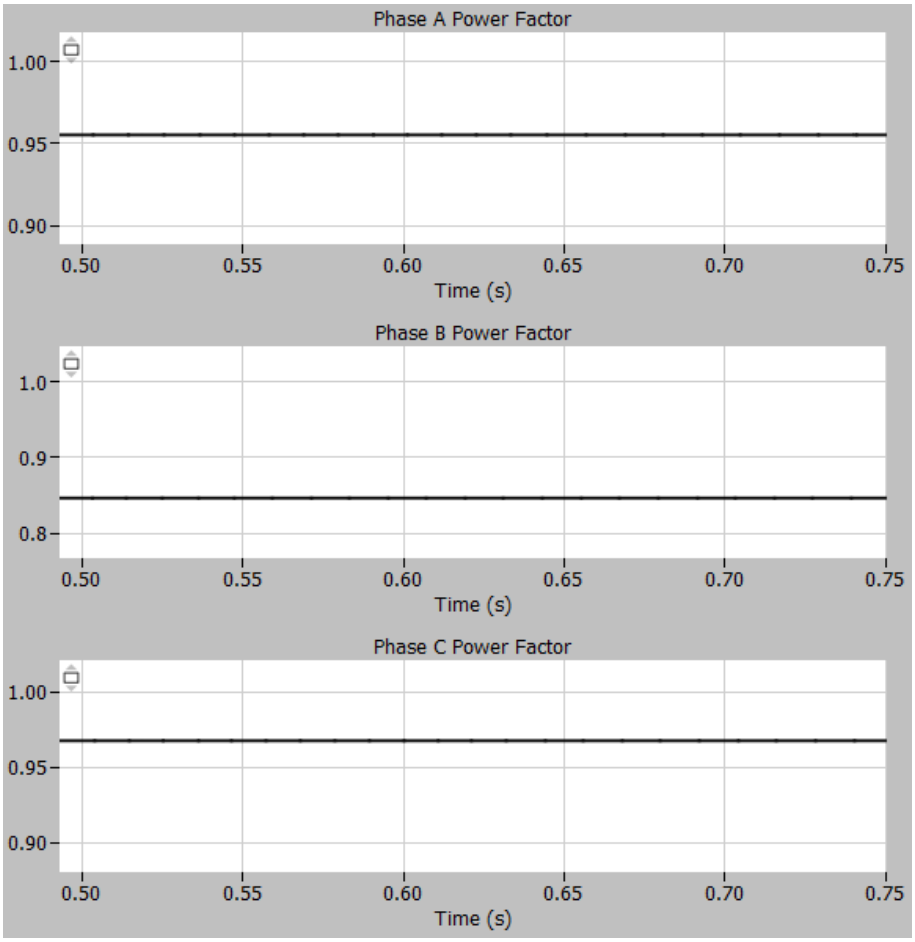

Figure 73: Power Factor of Phases A, B & C

The power factors of each phase are shown in **Figure 73**, Phases A & C has just above 0.95 while phase B has around 0.85. There is a difference in the power factors due to the unbalances as expected but the power factor seems to be the worst in the case of phase B.

Table 26: Overview of power factor and current THD with unbalance change

	Balanced	Magnitude change		Phase angle change	
	0%	**5%**	**10%**	**5%**	**10%**
Power factor – Phase A	0.95	0.95	0.96	0.84	0.71
Power factor – Phase B	0.95	0.91	0.85	0.93	0.81
Power factor – Phase C	0.95	0.97	0.97	0.97	0.95
$\boldsymbol{THD_I}$	2.12 %	9.99 %	17.86 %	19.69 %	33.03 %
$\boldsymbol{\Delta\, THD_I}$	-	7.07 %	14.50 %	16.32 %	29.40 %

Table 26 documents the power factors of phases A, B & C and it further shows the current THD under unbalanced conditions. As in the previous case, the changes are more severe in the case with

10% change, but the change in the current THDs are slightly bigger compared to the case without the filters. Despite the unbalances, it provides the power of 1MW across the P2X plant.

3.2.4 Load Variation

This section will focus on the robustness of the 12-DRMC topologies with reference to the load variation. For a topology to be considered robust, the results should be consistent even in the case of the load variation. For each simulation the input reference will be changed from 100% to 20% in decrements of 20% at a time. The simulations will be performed with and without trap filter separately.

12-Pulse Diode Rectifier With Multi-Phase Chopper Without Trap Filter

For the load variations, the reference voltage has been changed in the simulations such that less power is transferred across the load as the load is constant and cannot be changed. The simulations are run at decrements of 20% from full loads.

Table 27: Load Variation Analysis for DRMC

Load Variation	**100%**	**80%**	**60%**	**40%**	**20%**
Active power	1 MW	0.8 MW	0.6 MW	0.4 MW	0.2 MW
Power factor	0.97	0.97	0.97	0.97	0.96
$\boldsymbol{THD_I}$	8.07 %	8.14 %	9.42 %	10.78 %	14.74 %
$\boldsymbol{\Delta\ THD_I}$	-	0.07 %	1.35 %	2.71 %	6.67 %

Table 27 describes the analysis of the load variation of the system using the 12-DRMC topology. It documents the power factor & THD changes corresponding to the load variations. Figure 74**Figure 74** illustrates the changes in the THD on the grid side while the load is being varied from 100% to 20%. The trendline shows the decreasing trend of the THD as the load variation increases.

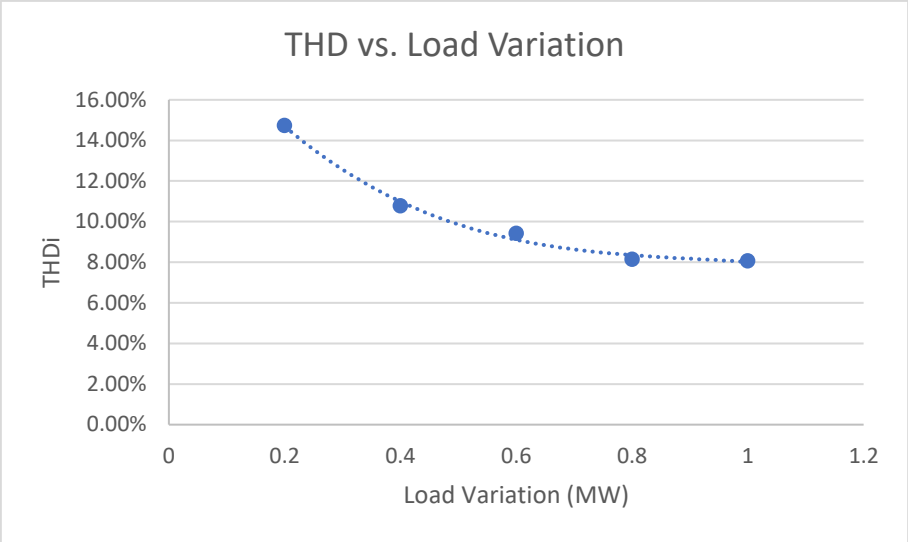

Figure 74: Load Variation vs THD for 12-DRMC

Figure 75 shows the plot of power factor vs load variation which indicates a constant power factor, even during the case of worst load variation (20%). The power factor maintains an approximate value of 0.96-0.97 during the entire load variation as illustrated by the trend line.

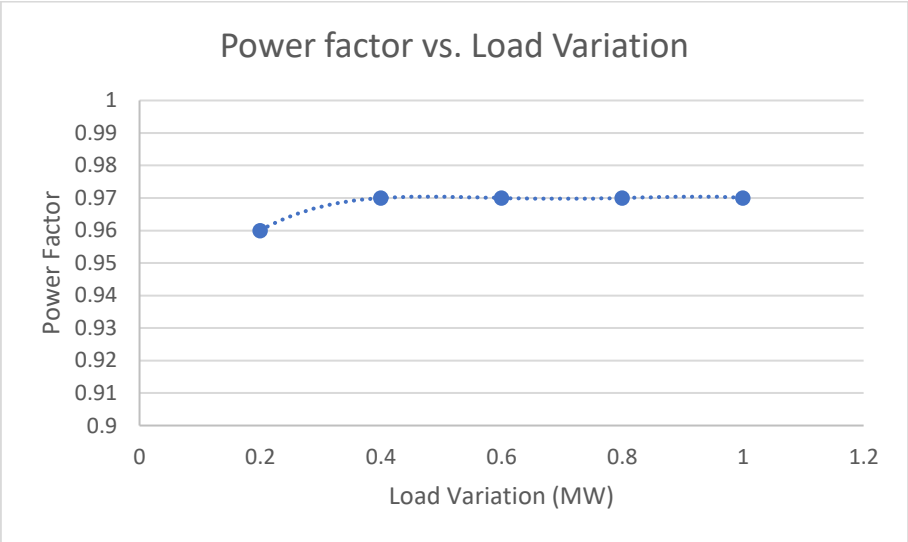

Figure 75: Load Variation vs Power Factor for 12-DRMC

12-Pulse Diode Rectifier With Multi-Phase Chopper With trap filter

The analysis for the 12-DRMC with the trap filter is performed the similar manner, as in the previous section with the variation from 100% down to 20% in decrements of 20%.

Table 28: Load Variation Analysis for DRMC with Filter

Load Variation	100%	80%	60%	40%	20%
Active power	1 MW	0.8 MW	0.6 MW	0.4 MW	0.2 MW
Power factor	0.95	0.90	0.79	0.62	0.34
THD_I	2.12 %	2.29 %	2.33 %	2.07 %	1.66 %
$\Delta\ THD_I$	-	0.17 %	0.21 %	-0.05 %	-0.46 %

Table 28 describes the THDi and Power Factors of the 12-DRMC topology under the different load variations.

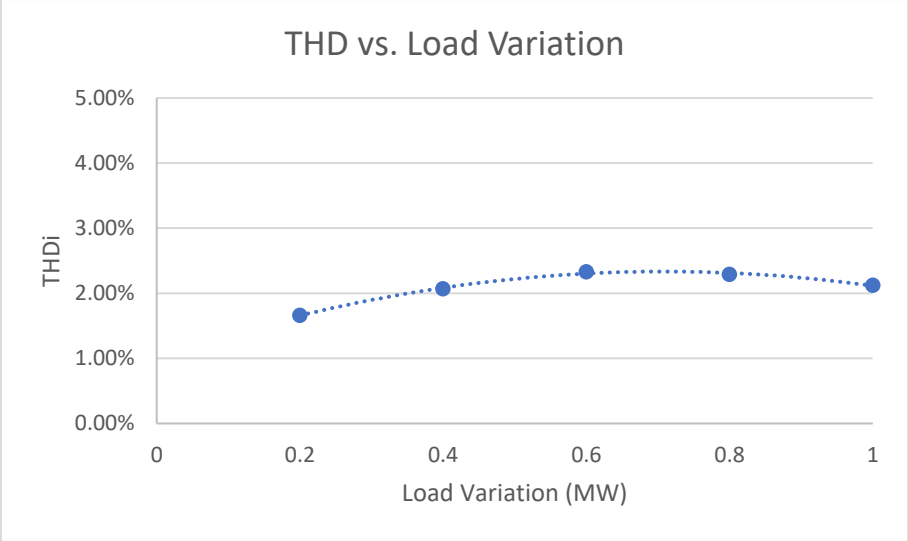

Figure 76: Load Variation vs THD for 12-DRMC with Filter

Figure 76 plots the current THD vs. Load Variation values graphically and it shows that the THD remains constant during the load variation around the value of 2%. It is different from the case without the filter, where the current THD had an increasing trend when the load was decreased from 1 MW to 0.2 MW.

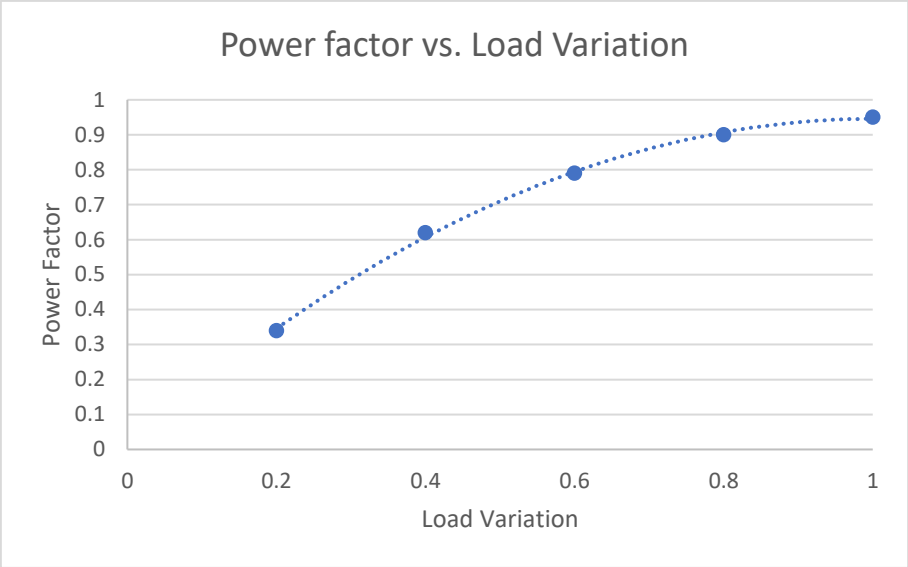

Figure 77: Load Variation vs Power Factor for 12-DRMC

Figure 78 graphically depicts the change in power factor vs. the load variation. There is a decreasing trend of the power factor as the power is decreased from 1 MW as opposed to the constant power factor discussed in the last section.

3.2.5 Efficiency Calculation

This section estimates the efficiency of the 12-DRMC model by comparing the results from the input active power to the output active power. The commercial semi-conductor devices will be used. In this particular case of 12-DRMC topology, the data for the IGBTs & diodes is employed as listed in **Table 29** and **Table** 5 respectivelyTable 5. Hence the efficiencies will be computed in the upcoming sections.

Table 29: Commercial IGBT Parameters for 12-DRMC Simulation.

Parameters	12-DRMC	25% Safety Margin Ratings	Infineion-FD400R33KF2C-K
V_{CES}	1760 V	2200 V	3300 V
I_C	355 A	445 A	600 A

The commercial devices (IGBTs & Diodes) have been added to the model via the 'thermal description' tool in the PLECS platform. **Figure 78 (A)** & **Figure 78 (B)** show the graphs for the commercial IGBT 'FD400R33KF2C-K' from Infineon. Similarly, **Figure 78 (C)** & **Figure 78 (D)** show the same graphs for the diode 'SD200R' from Vishay [36], [43].**Error! Reference source not found.**

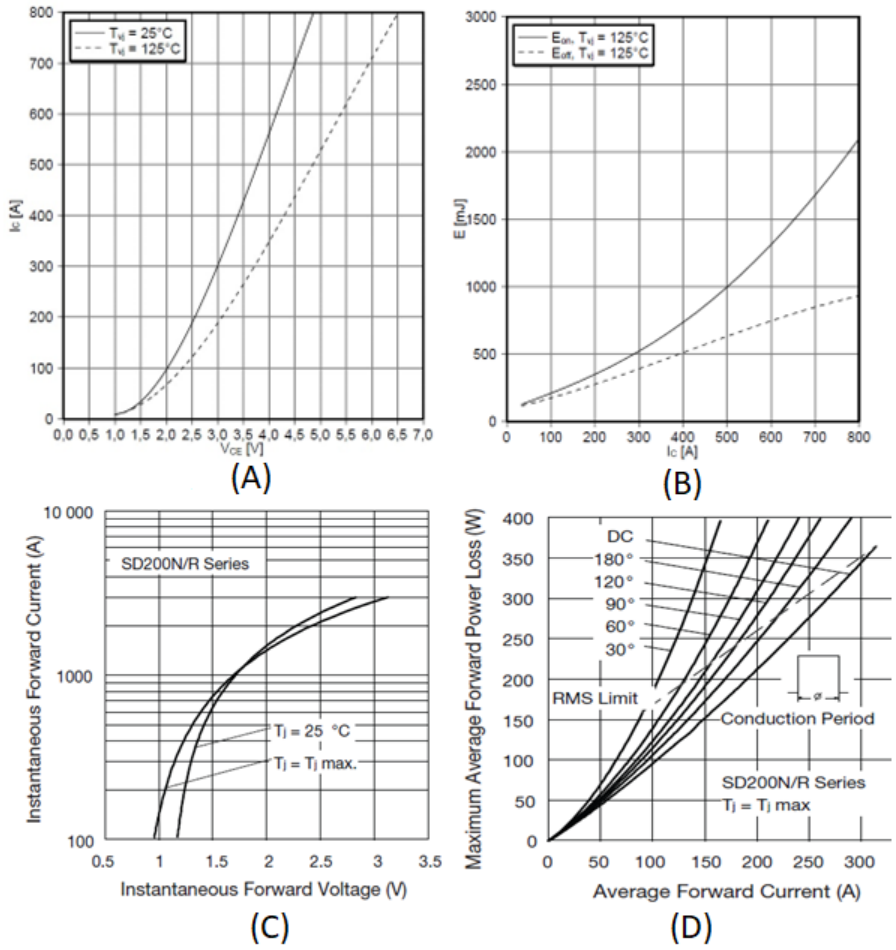

Figure 78: The conduction and switching loss for the IGBT in figure A and figure B, similarly for the diode in figure C and figure D

The graphs in **Figure 78** show the thermal descriptions of these commercial semi-conductor devices, which are added to the PLECS and applied to the 12-DRMC topology to alter its properties, so they resemble those of the commercial devices, hence applying the commercial attributes to the efficiency calculation.

Table 30: Efficiency estimation of the 12-DRMC

Load variation	100%	80%	60%	40%	20%
Input active power	1 MW	0.80 MW	0.60 MW	0.40 MW	0.20 MW
Output active power	1 MW	0.80 MW	0.60 MW	0.40 MW	0.20 MW
Efficiency	95.83%	95.52%	94.96%	93.93%	91.18%

Table 30 documents the estimated efficiency of the 12-DRMC topology at different load variations transferring different power levels across the output of the P2X plant. **Figure 79** plots the efficiency with respect to the output power across the P2X plant which indicates that the efficiency decreases

with decreasing load as indicated by the trendline. As the load is decreased the components operate at lower loads and hence at less temperature, hence increasing the resistance of the components, thereby decreasing the efficiency.

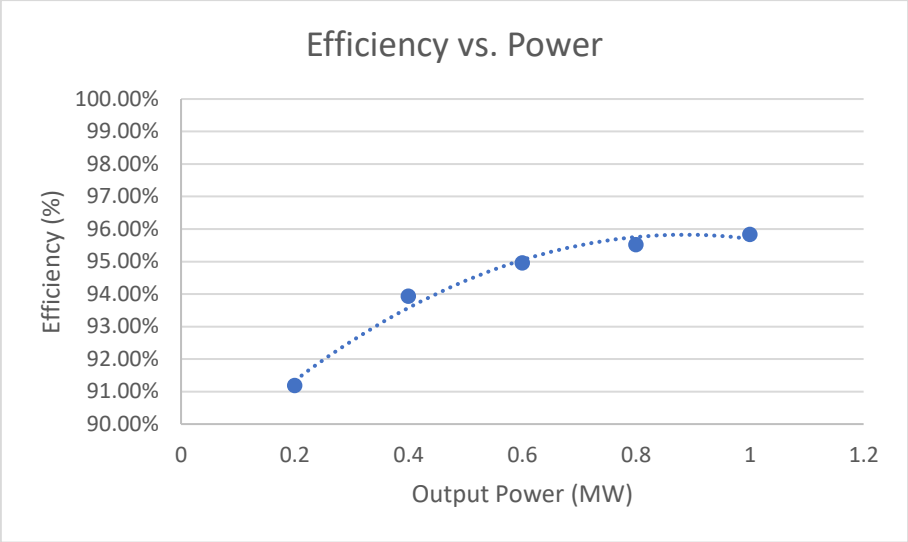

Figure 79: Efficiency vs Power graph for 12-DRMC

3.3 12- pulse Thyristor Rectifier Active Shunt Power Filter (12-TRASPF)

This section will cover the results obtained from the simulations of the 12-TRASPF topology. The format of the section is identical to the one used for all other topologies. The objective is to draw results initially when the 12-TRASPF is under full load conditions, as these results will be used as the reference for comparison. This will be covered in **section 3.3.1**. Next, **section 3.3.2** will cover the harmonic analysis test of this converter topology. Furthermore, in **section 3.3.3** unbalanced grid will be used to test the robustness of the 12-TRASPF, while in section **3.3.4** it will be tested under variable loads. Finally, in **section 3.3.5**, an efficiency test will be carried out, as a means of comparison with the remaining topologies.

Table 31 & **Table 32** documents the component parameters and control parameters used in all simulation tests of the 12-TRASPF respectively

Table 31: parameters used in components of 12-TRASPF.

12-TRASPF Topology Parameters	Values
V_{Grid}	33 kV
L_{Grid}	1 µH
L_{In}	350 µH
L_{DC}	300 µH
V_{DC}	1 kV
C_{DC}	5000 µF
R_{Load}	1 Ω
C_{APF}	1000 µF
I_{Sh}	80 µH

Table 32: Parameters used in control system for 12-TRASPF.

Parameters of control scheme	Values
KP1	0.7
KI1	22.2
U_{DC}	1.1 kV
I_{Out}	320 A
KP2	0.5/550*2
KI2	631/550

The parameters described in **Table 31** & **Table 32** can be referred to **Figure 10** and **Figure 12** respectively.

3.3.1 Output under ideal full load conditions

In this section the outputs and results obtained on the DC side of the 12-TRASPF converter topology under full load operation will be displayed via plots and tables in order to set the reference values for the important parameters such as output power, power factor and THD. The results shown take into consideration the ideal realistic case of an active filter, implying cost restrictions and maximum current ratings of IGBTs in an APF. This implies that the collector current in each IGBT of the APF will be <1kA, in order for IGBTs with a rating of 1200 A to be used, implying a safety margin of at least 25%. Therefore, the power factor can only increase above the value 0.94, by increasing the IGBT current ratings and hence the cost, as the amount of reactive power compensation is related to the IGBT current ratings. For this reason, the reference current 'Iq*', whose value determines the reactive power generation of the APF will be set to the value '-700 A'. The negative sign indicates the direction of the current. This implies that the APF is delivering reactive power and not consuming. This achieves a power factor value of '0.94' without the use of an additional passive

filter. The optimal method to increase the power factor further would be to use an active and passive filter combined (i.e., hybrid filter). However, in this work the hybrid filter has not been analysed.

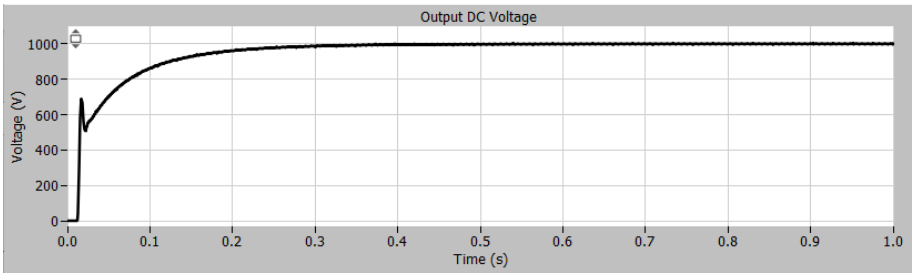

Figure 80: Output DC Voltage of 12-TRASPF converter

In Figure 80**Figure 80** the output DC voltage of the 12-TRASPF converter can be seen to be at 1kV, which is the required DC voltage in order to achieve the desired output of 1 MW.

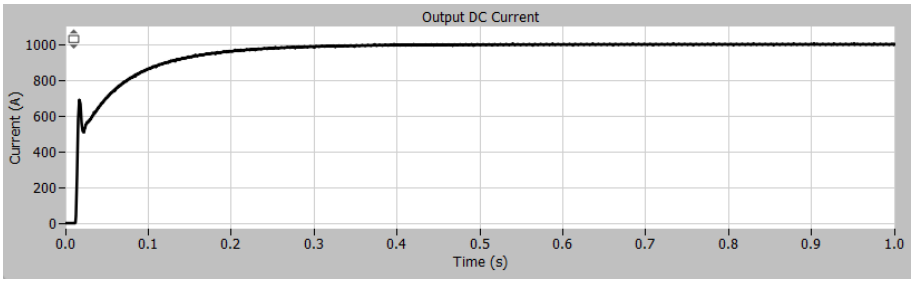

Figure 81: Output DC Current of 12-TRASPF converter

Similarly, in **Figure 81** the output DC current is shown to be 1 kA. A PI controller is used to maintain this value by setting the desired reference and comparing it to the measured value in order to maintain an error close to zero and a steady DC output current of 1 kA. As seen in both **Figure 80** and **Figure 81**, the PI controller requires less than 0.05 seconds to adjust and then gradually reaches steady-state at 0.3 seconds.

Table 33 below shows the parameters of the system under full load conditions. The power factor is 0.94, as 360.5 kVAr of reactive power is delivered from the APF. This has been chosen to be an appropriate value, as larger values of reactive power from the APF would increase the rating of the IGBTs significantly and hence the cost, as also mentioned previously.

Table 33: Parameters of 12-TRASPF under full load conditions

Parameters	Value	Unit
RMS current grid-side	18.84	A
RMS voltage grid-side	33	kV
Active power grid-side	1	MW
Apparent power grid-side	1.06	MVAr
Power factor grid-side	0.94	-
Current DC-side	1	kA
Voltage DC-side	1	kV
Active power DC-side	1	MW

3.3.2 Harmonic Analysis

In this section the simulation results for the 12-TRASPF topology will be presented and analysed, regarding the harmonic analysis aspect. The section is separated into two sub-sections, the first showing the results obtained when harmonic compensation is provided, but no reactive power compensation by the APF is provided. The second section displays the results shown when harmonic and reactive compensation are both utilized to increase the converter's performance.

3.3.2.1 Harmonic analysis without reactive power compensation

The harmonic analysis and power factor of the 12-TRASPF topology depend on several factors, in contrast to the simpler 12-TR topology. As will be depicted by the plots below, the THD_I will be very low due to the harmonic compensation from the resonant controller. Additionally, very small differences will be seen in THD_I when changes are made to the value of the 'q' component of the reference current, 'I_q*', which determines the amount of reactive power compensation provided by the APF to the dual thyristor bridges. The power factor, however, will vary significantly depending on the value set for 'I_q*', as larger negative values of 'I_q*' will correspond to higher power factor values.

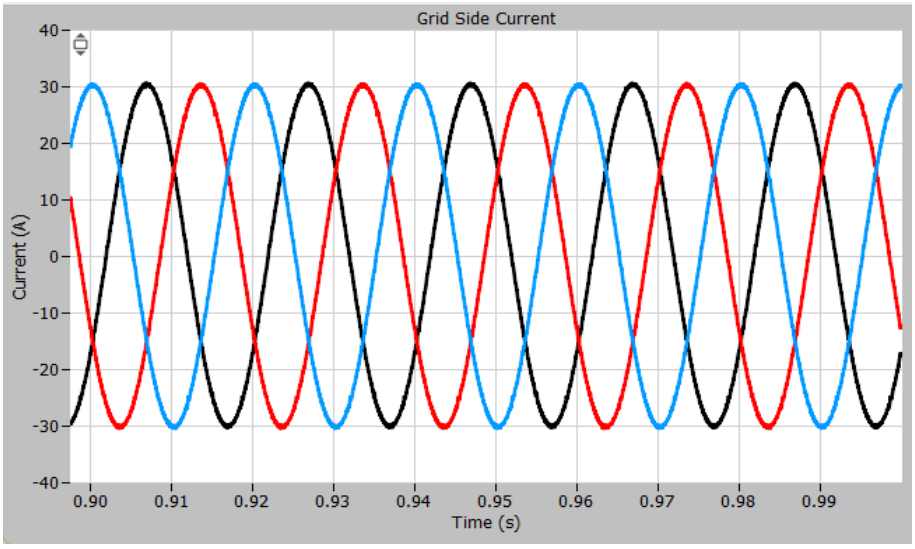

Figure 82: Grid Side Current and Grid side Current of 12-TRASPF with harmonic compensation and 'Iq=0'*

Above, in **Figure 82**, it can be seen that that the grid side current is sinusoidal. This figure depicts the grid side current when harmonic compensation is used for the 12-TRASPF topology and when 'I_q* = 0'. In effect, the APF is not transferring any reactive power to the 12-TR non-linear load. On the other hand, the resonant controller is used to attenuate the 12k ± 1^{th} harmonics, where k is a positive integer, present due to the 12-pulse thyristor bridges. The three resonant controllers are tuned to the harmonic frequencies of the 12^{th}, 24^{th} and 36^{th} harmonic order respectively. As the resonant controller is a second order filter, the 'n+1' and 'n-1' harmonic orders are attenuated, where 'n' is the harmonic order whose frequency, the resonant controller is tuned to.

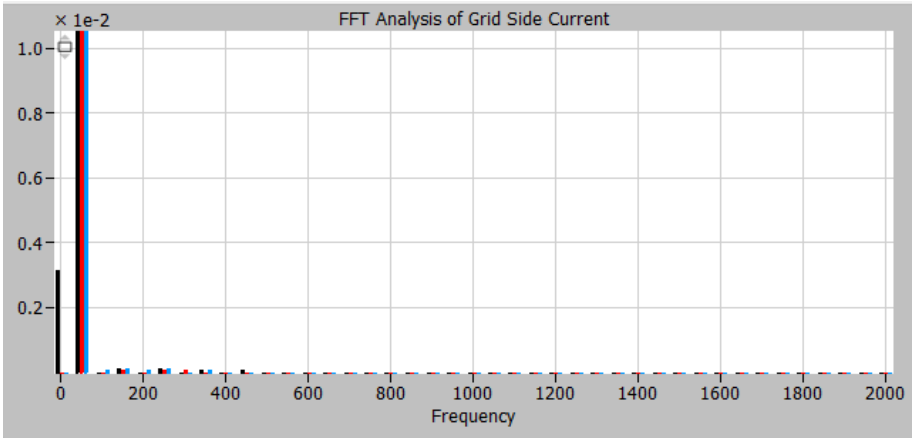

Figure 83: FFT Analysis of Grid side Current of 12-TRASPF with harmonic compensation and Iq = 0*

(Normalized with respect to the fundamental (50 Hz) with magnitude value of 1)

In **Figure 83** above, it can be seen that the harmonics have been attenuated to negligible values. These values are normalized with respect to the fundamental, which has the value of '1'. The current THD is calculated to be 0.7%.

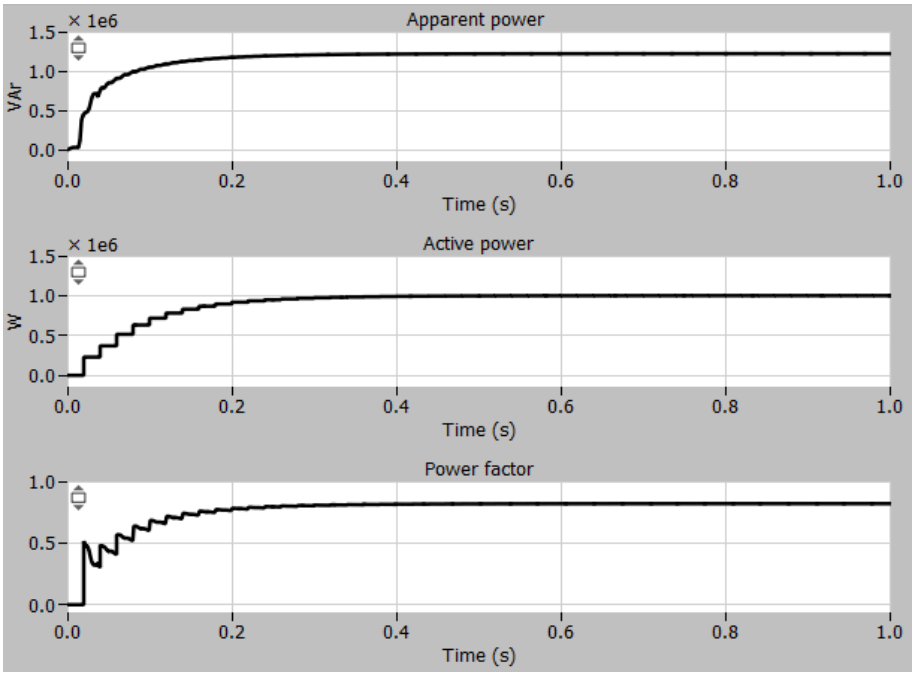

Figure 84: Grid Side Apparent power, Active Power, and Power Factor of 12-TRASPF

Figure 84 shows the 3-phase grid side apparent power to be 1.22 MVA, while the Active power is at full load power of 1 MW, indicating the presence of 0.7 MVAr reactive power in the grid. This low power factor of approximately 0.82 is mainly due to the 12-TR. As it is a non-linear load, it requires reactive power and if an active power filter does not provide reactive power, it will consume reactive power from the grid, causing its power factor to decrease.

The second factor that must be accounted for is the power factor. The harmonic compensation's influence on power factor is negligible; therefore, reactive power must be delivered from the APF to the 12-TR, so that less reactive power is consumed from the grid, thus increasing the grid side power factor. This is done by setting the reactive current reference 'I_q*' to a negative value. The negative sign, as mentioned, indicates the power flow direction; specifically, that reactive power will be delivered from the APF to the 12-TR. Three different cases will be investigated where three different values are set for the reactive current reference and conclusions will be drawn regarding the trend observed in the grid side power factor.

Table 34: Power factor and THD variations for varying reactive current reference

Reactive Current Reference	Iq* = 0	Iq* = -500	Iq* = -700
DC Power Output	1 MW	1 MW	1 MW
Grid Power Factor	0.82	0.91	0.94
Reactive Power Delivered by APF	109 kVAr	226.9 kVAr	359.5 kVAr
THD	0.7%	0.8%	0.82%

As can be seen from **Table 34** above, when reactive power compensation is applied to the system, the power factor increases closer and closer to unity. Finally, the THD is observed to increase by the incremental steps of approximately 0.1% for every increment of '-500 A' of 'Iq*', as the delivery of additional reactive power to the system via the APF will increase harmonic levels. However, the increase in power factor of 7%-9% in the same interval, is significant. An important consideration when referring to the APF, is that higher values of reactive power compensation will increase the collector current in the IGBTs. In effect, if close to unity power factor is required, this implies a higher current rating of IGBTs and hence a larger cost of the APF.

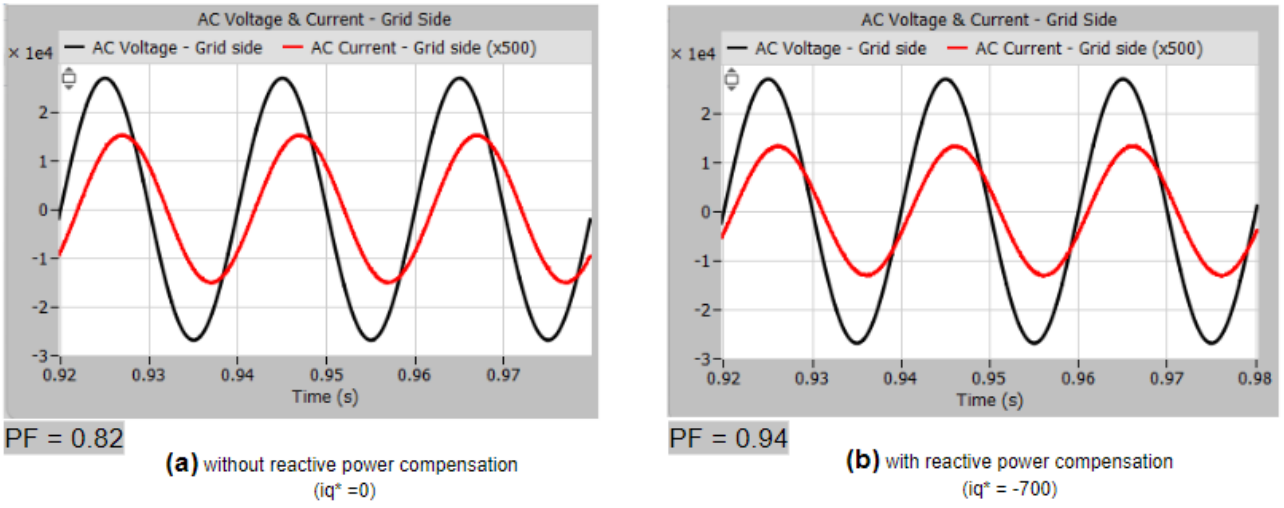

Figure 85: Grid Side Phase Voltage & Grid Side Phase Current (x500) when (a) 'iq = 0' and (b) 'iq* = -700'*

Figure 85 (a) shows the grid side phase voltage (black) and grid side phase current (red) without reactive power compensation (iq* = 0) and with reactive power compensation in **Figure 85** (b), where 'iq* = -700'. The grid phase voltage is to scale, with a value of 27 kV, while the grid phase current has been given a gain of '500' for comparison purposes. The first observation is associated with the power factor, as it can be seen that in **Figure 85** (a) the current phase lag is greater than in

Figure 85 (b) and hence (b) has a higher power factor. The current phase lag also indicates an inductive non-linear load. Furthermore, the peak phase current decreases from 30.4 A in (a) to 26.4 A in (b), indicating that less power is drawn from the grid by the 12-TR non-linear load, as it consumes reactive power from the APF instead.

3.3.3 Unbalanced Grid

In this section the 12-TRASPF topology will be tested with unbalances in the grid voltage's magnitude and phase angle in one phase in order to observe the power factor and THD changes and to what degree this topology can maintain a high-power factor and low THD. In the first sub-section the case with only harmonic compensation will be observed. In the second sub-section, reactive power compensation will be introduced in combination with harmonic compensation and the results will be presented.

3.3.3.1 Unbalance Grid with harmonic compensation and no reactive compensation

The grid voltage is subjected to 10% voltage magnitude decrease in Phase B and the simulation results are analysed.

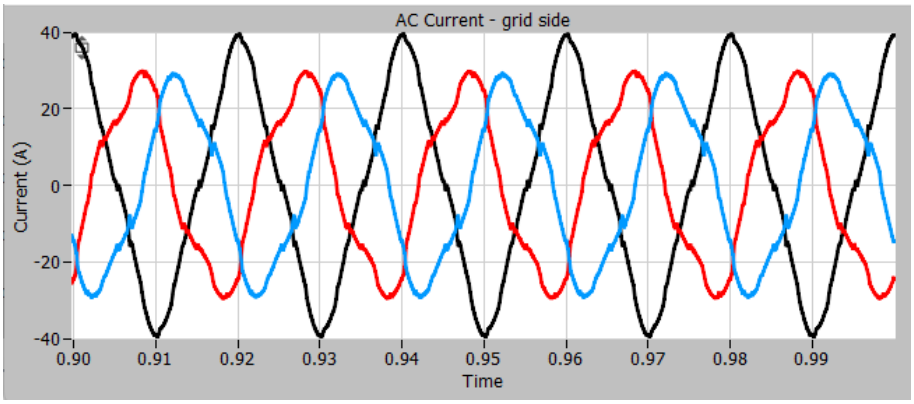

Figure 86: Grid Side Current of 12-TRASPF with 10% grid voltage magnitude decrease in phase B

As can be seen from **Figure 86**, the grid side current becomes unbalanced, as the magnitude of each phase changes. The THD also increases in each. It is observed that in one phase the THD increases from 3.1% to 12.4% and the other phases have higher values.

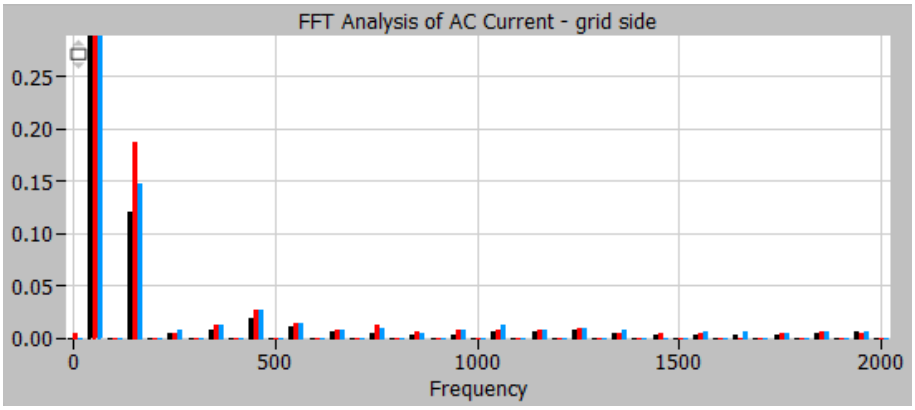

Figure 87: FFT Analysis of Grid side Current of 12-TRASPF with 10% voltage magnitude decrease in phase B.

Normalized to the fundamental frequency of 50 Hz and magnitude value of 1.

When observing the FTT analysis of the harmonics in **Figure 87**, as observed in the 12-TR topology, the presence of the 3rd harmonic is evident that typically arise from imbalances in the grid. The THD of each harmonic is, as always, calculated with respect to the fundamental, whose value is 1.

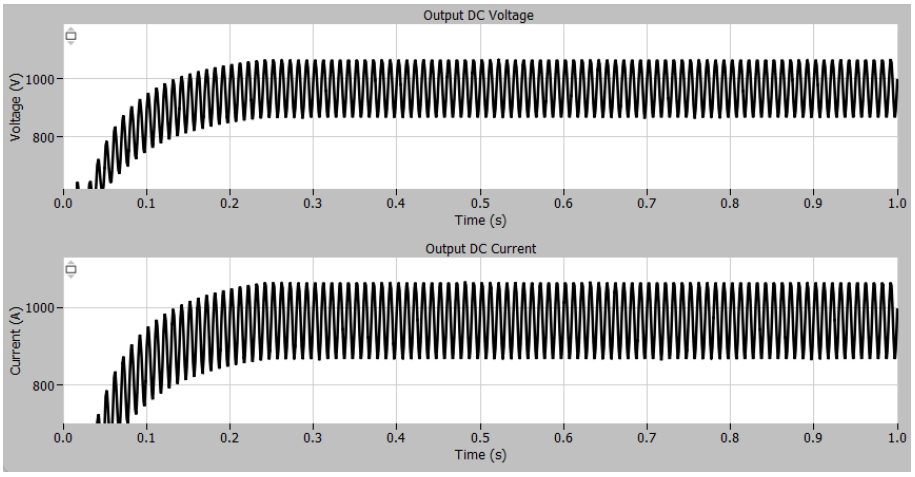

Figure 88: Output DC Voltage (upper plot) and Output DC Current (lower plot) with 10% Grid Volt. magnitude unbalance

Also, when the DC output voltage and current characteristics are observed in **Figure 88**, major fluctuations of the magnitude of '±50 V' and '±50 A' can be seen in both DC voltage and current curves respectively. The active power delivered to the resistive load on the DC side shows to be around 0.9 MW which is approximately 100kW less than the desired 1MW value, as the voltage and current fluctuations are not centered around '1000 V' and '1000 A' respectively.

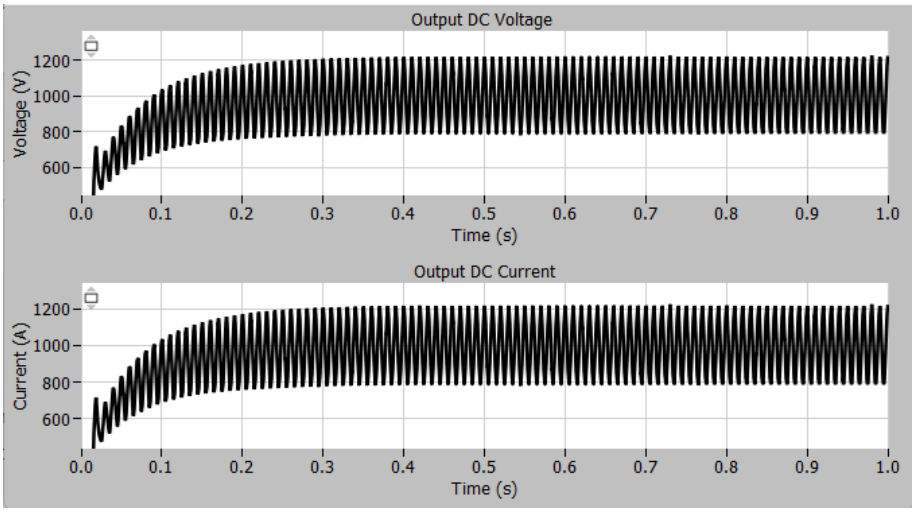

Figure 89: Output DC Voltage (upper plot) and Output DC Current (lower plot) with 10% Grid Phase Volt. unbalance

On the other hand, **Figure 89** shows larger fluctuations in the output DC Voltage and Current. While the average output power can be seen to be 1 MW, as the fluctuating Voltage and Current curves are both centered around the value of '1000 V' and '1000 A' respectively; however, due to the 10% unbalance in the phases of the grid voltage, the fluctuations in the DC output side are '±200 V' and '±200 A'. This is due to the fact that a voltage phase unbalance produces more THD than a voltage magnitude unbalance and therefore this has a larger effect on the DC output side.

Table 35 below shows the power factor values calculated in each phase on the grid side and the THD value of the grid side current when the voltage is subjected to a 5% and 10% change in magnitude and a 5% and 10% change in the voltage phase angle, when only harmonic compensation is applied to the 12-TRASPF, as a measure of comparison with the various topologies, which are analysed. The current THD described in the table refers to the THD calculated in one phase, precisely the one with the lowest THD value for the reason of accurate comparison between the different topologies.

Table 35: Comparison between imbalances in phase and voltage magnitude of 12-TRASPF with only harmonic compensation

Operating Conditions	**Balanced**	**Magnitude change**		**Phase angle change**	
Unbalance (%)	0%	5%	10%	5%	10%
Power factor – Phase A	0.82	0.83	0.82	0.89	0.91
Power factor – Phase B	0.82	0.77	0.69	0.81	0.79
Power factor – Phase C	0.82	0.86	0.89	0.7	0.5
$\boldsymbol{THD_I}$	0.7%	7%	12.4%	11.9%	21.5%
$\boldsymbol{\Delta\, THD_I}$	-	6.3%	11.7%	11.2%	20.8%

3.3.3.2 Unbalance Grid with both reactive compensation and harmonic compensation

The 12-TRASPF was tested under unbalanced conditions when both harmonic and reactive compensation were applied. The results are shown below in both **Table 36** &**Table 37**. The results regarding the power factors of the three phases are more promising than those obtained in **Table 35**. However, due to the reactive compensation, the THD is increased by approximately 1% in the case of voltage magnitude unbalance. Therefore, it can be concluded that there exists a trade-off between harmonic and reactive power compensation, as increased values of reactive power compensation led to slightly higher values of THD. Alternatively, lower reactive power compensation decreases the power factor dramatically and also decreases THD by a smaller degree.

Table 36: Comparison between imbalances in phase and voltage magnitude of 12-TRASPF reactive compensation ***(iq* = -500)***

Operating Conditions	**Balanced**	**Magnitude change**		**Phase angle change**	
Unbalance (%)	0%	5%	10%	5%	10%
Power factor – Phase A	0.94	0.91	0.95	0.95	0.94
Power factor – Phase B	0.94	0.87	0.9	0.88	0.85
Power factor – Phase C	0.94	0.95	0.97	0.83	0.63
$\boldsymbol{THD_I}$	0.7%	11%	13.9%	13.3%	25%
$\boldsymbol{\Delta\, THD_I}$	-	10.3%	13.2%	12.6%	24.3%

Table 37: Comparison between imbalances in phase and voltage magnitude of 12-TRASPF reactive compensation ***(iq* = -700)***

Operating Conditions	**Balanced**	**Magnitude change**		**Phase angle change**	
Unbalance (%)	0%	5%	10%	5%	10%
Power factor – Phase A	0.94	0.94	0.92	0.97	0.94
Power factor – Phase B	0.94	0.91	0.85	0.91	0.87
Power factor – Phase C	0.94	0.97	0.98	087	0.68
$\boldsymbol{THD_I}$	0.7%	8%	13.9%	13.9%	25%
$\boldsymbol{\Delta\, THD_I}$	-	7.3%	13.2%	13.2%	24.3%

3.3.4 Load Variation

The load variation testing of the 12-TRASPF will be displayed in this section via the use of tables and plots. As with the other topologies examined, the 12-TRASPF is tested under different loads from full load to the case of 20% load. In this way, its robustness to load variations is examined. **Table 38**

displays the results obtained under zero reactive power compensation from the APF. The trend is a decrease in power factor and an increase in THD, with decreasing load.

Table 38: Load Variation Testing of 12-TRASPF without reactive power compensation

Load variation	**100%**	**80%**	**60%**	**40%**	**20%**
Active power	1 MW	0.8 MW	0.6 MW	0.4 MW	0.2 MW
Iq* (A)	0	0	0	0	0
Power factor	0.82	0.73	0.63	0.51	0.36
$\boldsymbol{THD_I}$	0.7%	1.2%	1.5%	1%	1.5%
$\boldsymbol{\Delta\, THD_I}$	-	0.5%	0.8%	0.3%	0.8%

The same test was carried out with reactive power compensation involved and as expected the same trend was observed as in **Table 39**. However, the power factors observed are much higher as expected due to the reactive power compensation.

Table 39: Load Variation Testing of 12-TRASPF with reactive power compensation

Load variation (%)	**100%**		**80%**		**60%**		**40%**		**20%**	
Active power	1 MW		0.8 MW		0.6 MW		0.4 MW		0.2 MW	
Iq* (A)	-500	-700	-500	-700	-500	-700	-500	-700	-500	-700
Power factor	0.91	0.94	0.85	0.89	0.77	0.83	0.68	0.77	0.58	0.74
$\boldsymbol{THD_I}$	0.7%	0.8%	1.4%	1.5%	1.7%	1.9%	1.4%	1.5%	2.2%	2.8%

The power factor is also plotted against the load variations in **Figure 90**. It is clear from the figure that there is a steeper gradient when no reactive power compensation is applied, meaning that reactive power compensation is key to maintaining a higher power factor during load variations. The reactive power compensation must increase gradually when the load variation increases in order to maintain a constant power factor.

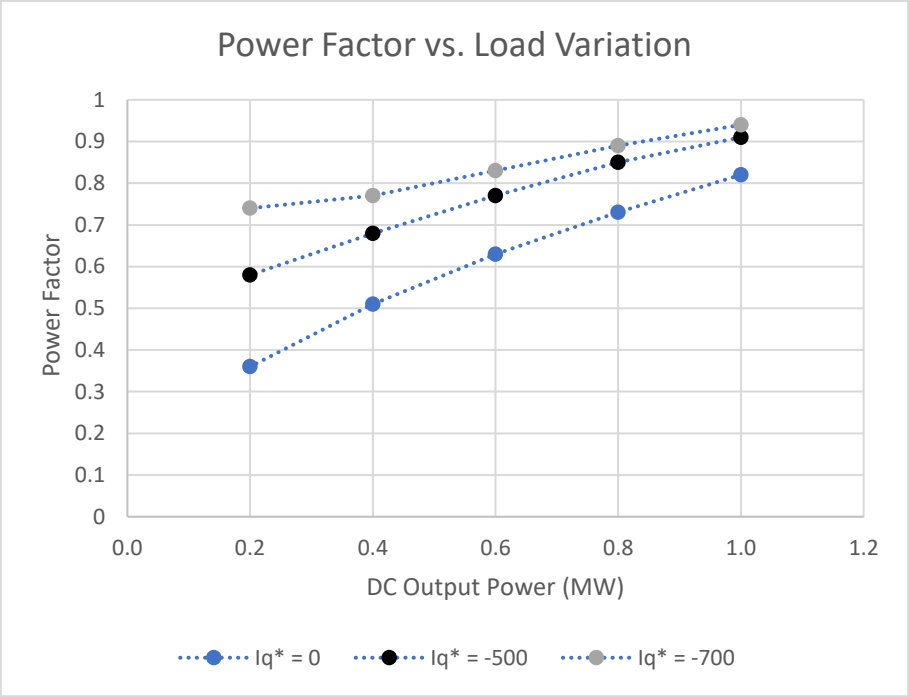

Figure 90: Trend in PF for increasing load variation percentage for 3 different values of 'Iq'*

A similar trend can be seen in **Figure 91** where THD percentage is plotted against DC output active power from the results also shown in **Table 39** above. There is a decrease in THD at 60% load variation, indicating an anomaly in the trend. However, the general trend shows a decrease in THD with decrease in output power.

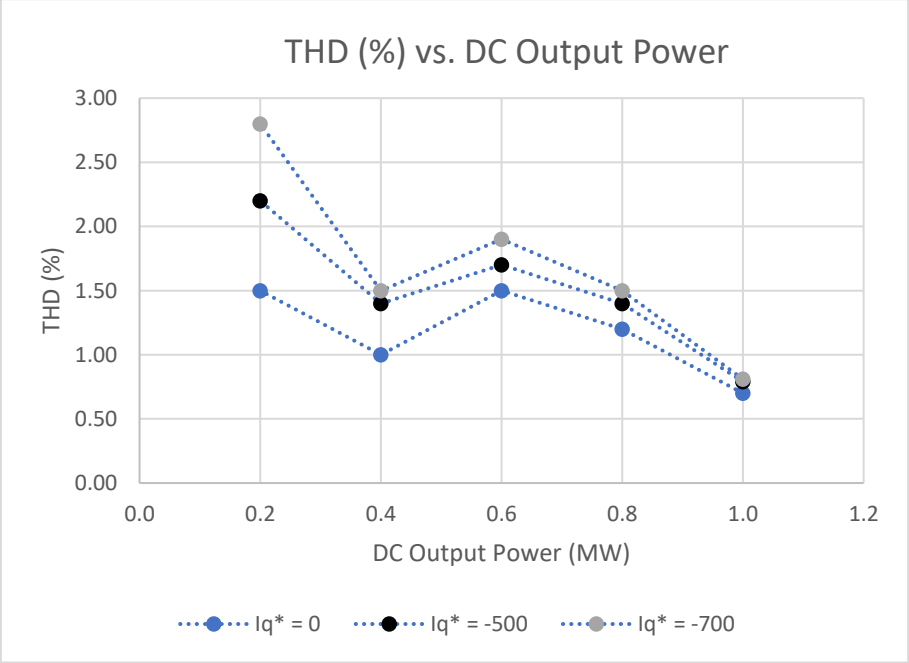

Figure 91: THD (%) vs. Active Power (MW) for 3 different values of 'Iq'*

3.3.5 Efficiency Calculation

The efficiency test for the 12-TRASPF is conducted with non-ideal semi-conductors and similar changes are made to the transformers winding resistance, in order to emulate the losses of an actual system.

Table 40: Commercial Thyristor parameters for 12-TRASPF Simulation.

Parameters	12-TRASPF thyristor simulation value	25% Safety Margin Ratings	Commercial Thyristor Ratings
V_{DRM}	1400 V	1900 V	2000 V
$I_{T(rms)}$	300 A	400 A	400 A
$I_{T(AV)}$	170 A	230 A	250 A

In order to determine the correct commercial thyristor for the 12-TRASPF, similar measurements as for 12-TR have been conducted. The 'IXYS-MCC224-20io1' commercial thyristor has the correct specifications when considering the safety margin of 25%. Thus, this commercial thyristor has been chosen for 12-TRASPF and its ratings can be seen above in **Table 40** [44].

Table 41: Commercial IGBT parameters for 12-TRASPF Simulation.

Parameters	12-TRASPF IGBT simulation value	25% Safety Margin Rating	Commercial IGBT Rating
V_{DRM}	1180 V	1600 V	1700 V
I_C	950 A	1300 A	1400 A

Unlike the 12-TR topology, this topology also includes IGBTs for the active power filter. In order to determine the IGBT parameters a measurement of voltage and current across the IGBT's was conducted. The measurement with and without safety margin and corresponding commercial IGBT [45] can be seen in **Table 41**. The 'FF1400R17IP4' commercial IGBT has been chosen.

Table 42: Efficiency estimation of 12-TRASPF without reactive power compensation

Load percentage	100%	80%	60%	40%	20%
Input active power	1.00 MW	0.81 MW	0.61 MW	0.41 MW	0.20 MW
Output Active power	0.97 MW	0.78 MW	0.58 MW	0.406 MW	0.18 MW
Efficiency	96.91%	96.42%	95,57%	93,79%	88.91%

Table 42 shows the results of the efficiency test with the active power filter connected. The efficiency is measured at various loads to determine if the topology is able to deliver power to a P2X plant without any significant losses. The results obtained in the table are plotted in **Figure 92** The efficiency of the topology is seen to decrease with decreasing load. The magnitude of this decrease is also greater than that of the 12-TR topology, due to the losses from the IGBTs in the APF of the 12-TRASPF.

Table 43: Efficiency estimation of 12-TRASPF with reactive power compensation (iq = -500)*

Load percentage	100%	80%	60%	40%	20%
Input active power	1.00 MW	0.81 MW	0.61 MW	0.41 MW	0.20 MW
Output Active power	0.97 MW	0.78 MW	0.58 MW	0.38 MW	0.18 MW
Efficiency	96.42%	95.79%	94.73%	92.64%	86.58%

Table 44: Efficiency estimation of 12-TRASPF with reactive power compensation (iq = -700)*

Load percentage	100%	80%	60%	40%	20%
Input active power	1 MW	0.81 MW	0.61 MW	0.41	0.2 MW
Output Active power	0.96	0.77 MW	0.57 MW	0.37	0.17 MW
Efficiency	96%	95.24%	94%	91.56%	84.3 %

As can be seen above in **Table 43** & **Table 44**, the efficiencies when reactive power compensation is applied to the system are all lower to those compared in **Table 42**, where no reactive power is delivered by the APF. This is expected, as both the conduction losses and switching losses across the IGBTs increase with increasing reactive power compensation from the APF. This is also shown clearly in **Figure 92** below, where with increasing reactive power compensation, efficiency decreases when

varying the load. At full load (1MW) however, the values of the efficiencies are ≥96% regardless of the amount of reactive power compensation, indicating that the system is most efficient at the operating power it is designed for.

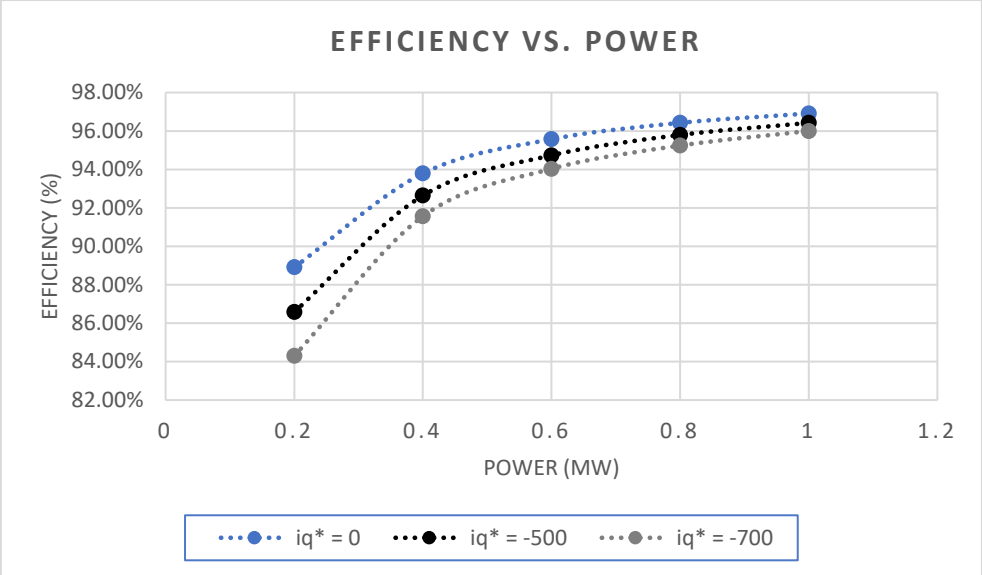

Figure 92: Efficiency vs Power for 12-TRASPF with various reactive compensation

3.4 Active front end – B6+Chopper

In this section all the tests will be conducted for the AFE. The test results will be analysed and to assess the performance of the AFE, the tests will be carried out once, since this topology does not include any filters.

Table 45, **Table 46**, and **Table 47** documents the components parameters, current control parameters, and chopper control parameters used in all simulation tests of the AFE topology.

Table 45: parameters used in components of AFE.

Parameters of control scheme	Values
V_{Grid}	33 kV
L_{Grid}	5^{-6} H
L_{In}	300^{-6} H
L_{DC}	300^{-6} H
C_{DC}	5000^{-6} F
R_{Load}	1 Ω

Table 46: Parameters used in Current control system for AFE.

Parameters of control scheme	Values
V_{Out}	1.2 kV
K_{P1}	1
K_{I1}	200
K_{P2}	0.002
K_{I2}	2
K_{P3}	0.002

Table 47: Parameters used in Chopper control system for AFE.

Parameters of control scheme	Values
K_{P1}	0.03*1.2
K_{I1}	6*1.2
V_{DC}	1 kV
K_{P2}	0.005
K_{I2}	10

Table 45, **Table 46**, and **Table 47** parameters can be referred to **Figure 13**, **Figure 15**, and **Figure 16** respectively.

3.4.1 Output under ideal full load conditions

The results presented in this section will revolve around full load ideal simulations, on the output DC side of the P2X plant. The tests will give an indication of how the model operates under ideal conditions and illustrate its ability to deliver the desired output of 1 MW. The output current, voltage, and power are all simulated in this section, similar to the previous topologies.

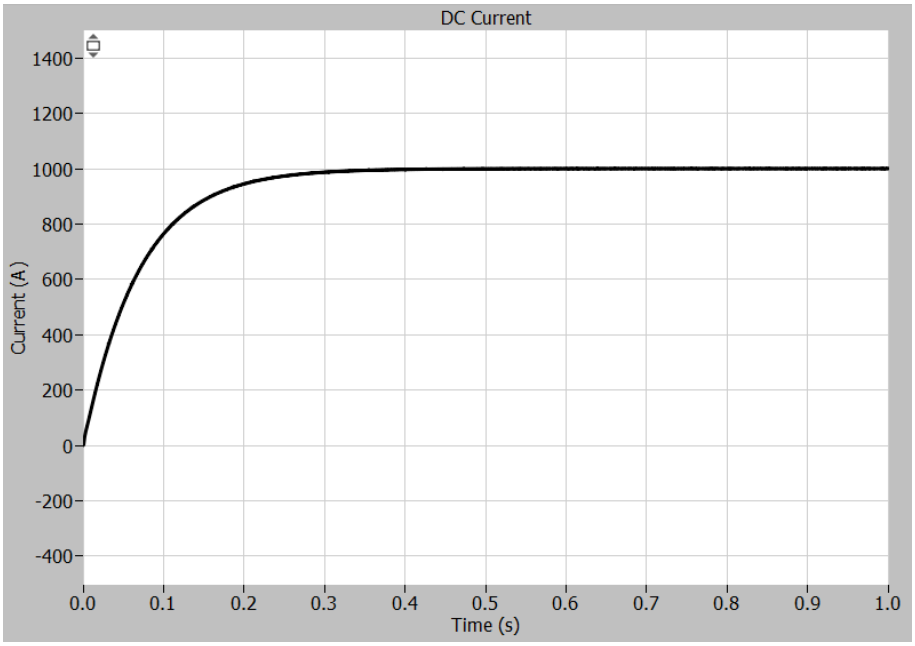

Figure 93: DC current from the AFE

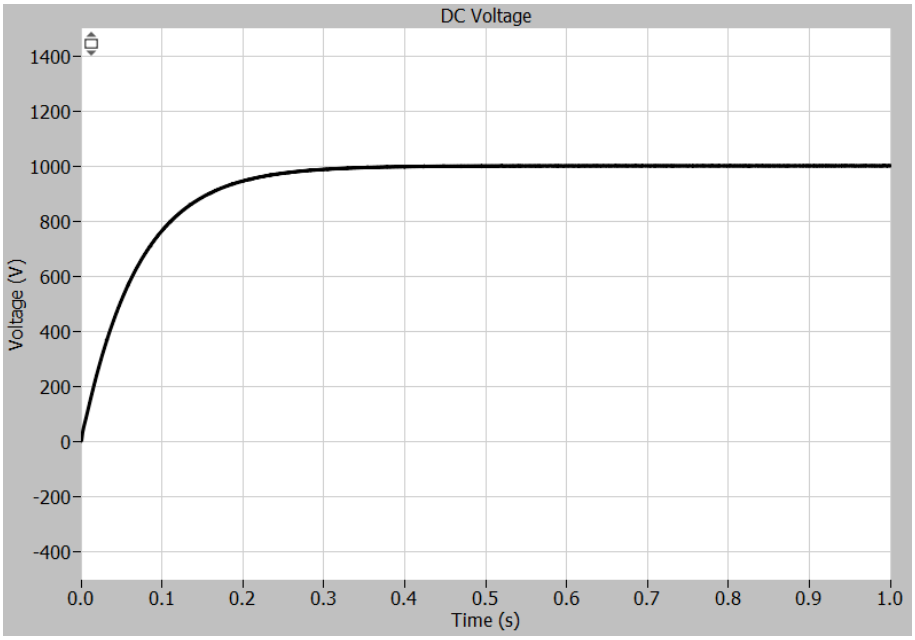

Figure 94: DC voltage from the AFE

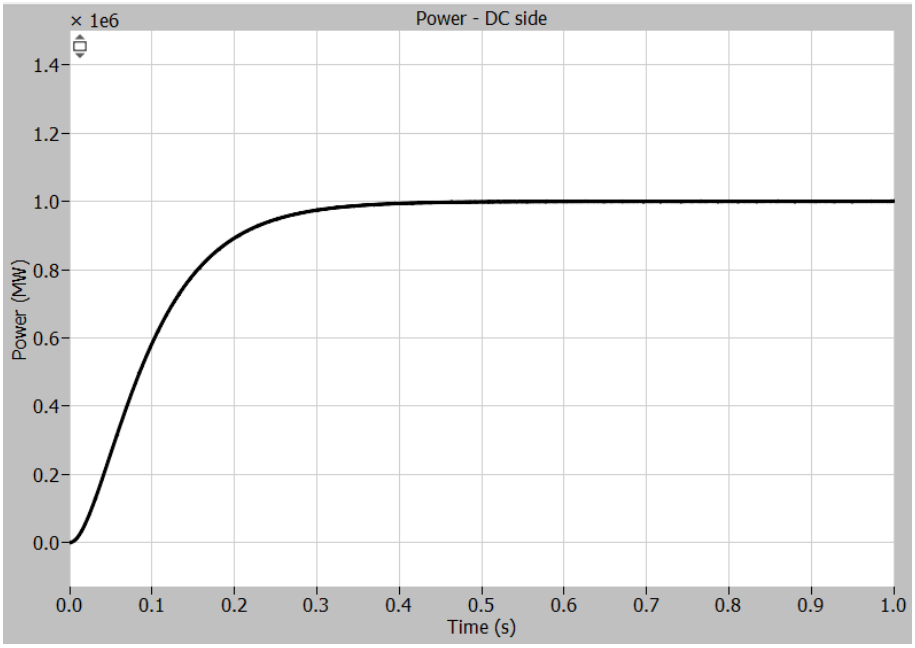

Figure 95: Power at the DC side from AFE

Figure 93, **Figure 94**, and **Figure 95** show the current, voltage and power respectively on the DC side of the AFE topology. The DC current and voltage are both exactly 1 kA and 1 kV which give an equivalent power of 1 MW. The exact values of all the graphs are shown in **Table 48** among other relevant parameters.

Table 48: Relevant parameters of the Active Front End

Parameters	Value	Unit
RMS current - grid side	17.5	A
RMS voltage – Grid side	33	kV
Active power - Grid side	1	MW
Apparent power - Grid side	1	MVAr
Power factor grid-side	99.98	-
Current DC-side	1.00	kA
Voltage DC-side	1.00	kV
Active power DC-side	1.00	MW

3.4.2 Harmonic Analysis

The harmonic analysis of the AFE simulation model is similar to the other topologies and is conducted on the grid side of the topology. **Figure 96** shows the AC Current on the grid side which looks purely sinusoidal, hence showing no presence of harmonics. The distortion is mitigated due to the active rectifiers in the AFE topology. Depending on the number of rectifiers, the distortion is further reduced; hence 18 rectifiers should have even lower distortion. However, as previously

stated this will also increase the cost and footprint of the topology; hence 12 pulse rectifiers are typically used. This topology monitors the input current and rectifies it to a sinusoidal waveform, thereby reducing the harmonics.

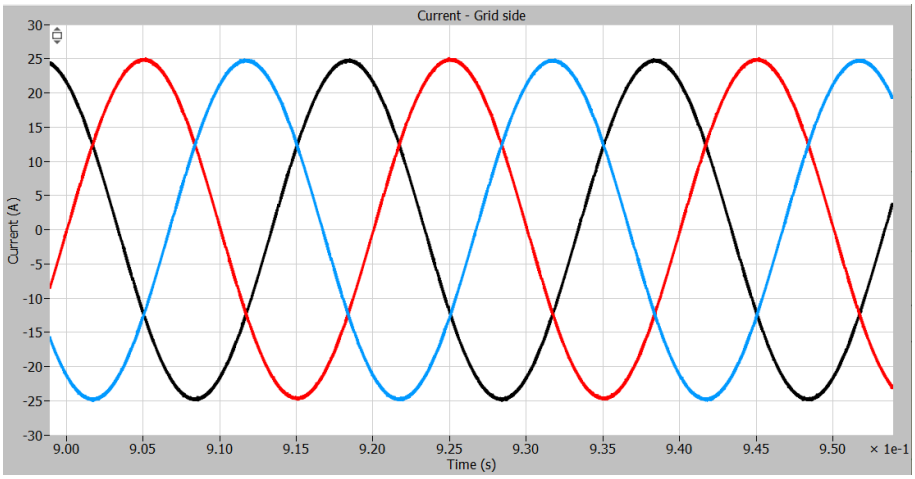

Figure 96: Current measurements on the grid side.

Figure 97 shows current measurement on the grid side. The current distortion is measured to be $THD_I = 0.81\%$, hence the amount of distortion of the current is negligible. Furthermore, an almost perfect sinusoid for the current waveform is seen, which also indicates a negligible amount of harmonic.

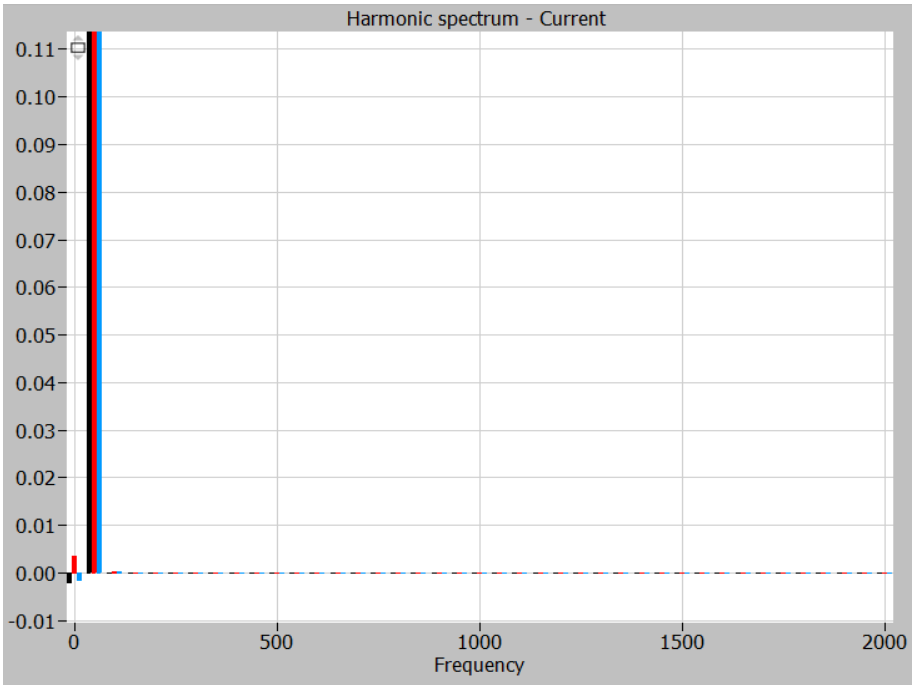

Figure 97: Harmonic spectrum of the current harmonics on the grid side. (Normalized with respect to the fundamental frequency of 50 Hz with magnitude value of 1)

Figure 97 portrays the harmonic spectrum of the AFE topology's current, where the magnitudes of all harmonics are as always normalized to the fundamental of 50 Hz and magnitude of '1'. The measurements of all relevant harmonic orders can be seen in **Table 49**.

Table 49: 12 ± 1 Harmonic orders & THDi Value

Harmonic(s)	THDi
11th Harmonic	3.8e-5%
13th Harmonic	3.7e-5%
23rd Harmonic	1.9e-5%
25th harmonic	1.7e-5%
35th harmonic	1.2e-5%
37th harmonic	1.2e-5%
THD	0.8%

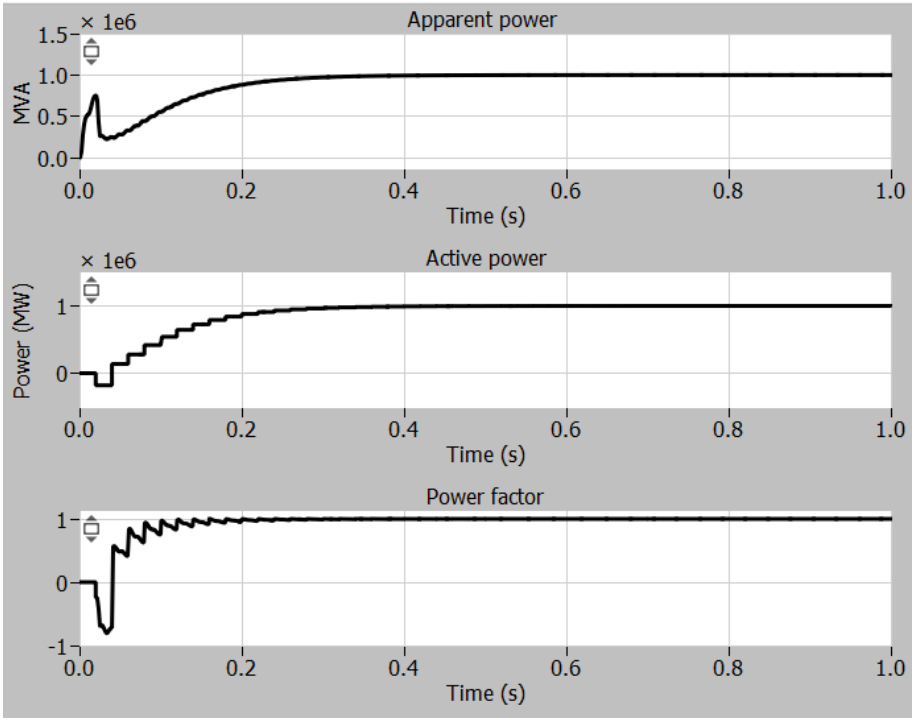

Figure 98: Graphs of Apparent power (S), Active power (P) and Power factor (PF).

Figure 98 shows the Apparent power, Active power, and Power factor of the AFE. Active power is approximately measured to be 1 MW, which is the goal for all the topologies. Furthermore, it is seen that the apparent power is also measured to 1 MVA, this is important in terms of the power factor but also proves the control of the AFE is operating as desired, since 'Iq' is set to zero. The power factor is measured to 0.99 which is expected from a superior topology such as AFE.

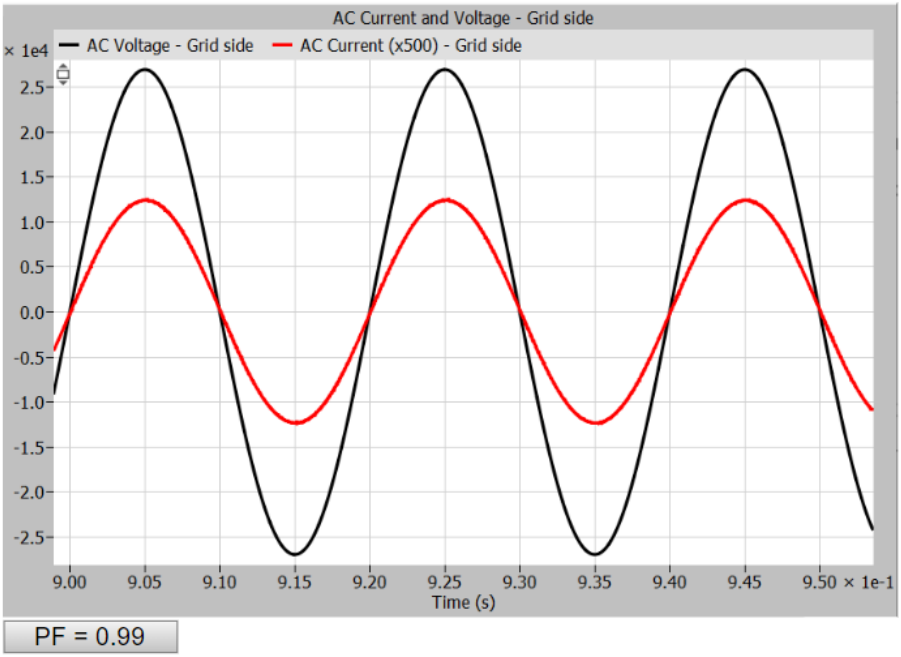

Figure 99: Current (x500) and voltage – grid side – With power factor of 0.99

Figure 99 depict the AC Current and Voltage. The grid current has been enlarged by a factor of 500 in order to show the phase alignment of the current and the voltage. It indicates that AFE produces a very high-power factor, close to unity, hence there in no displacement of phase between the current and voltage.

3.4.3 Unbalanced Grid

Similar to the previous topologies, a decrease of 5% & 10% magnitudes of phase B were implemented to simulate the grid unbalances in order to test the robustness of the topology. Furthermore, the phase angle in phase B were also changed by 5% & 10%, in order to test the topology under unbalanced grid.

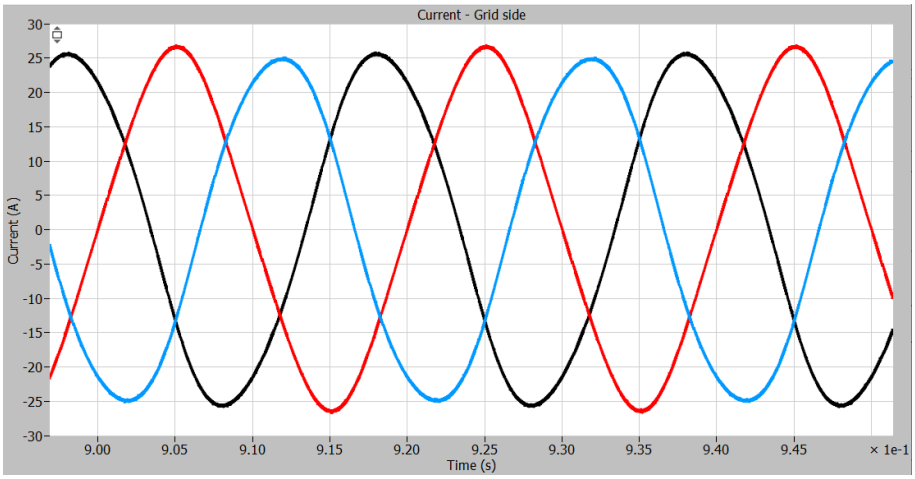

Figure 100: Current measurement with 10% decrease of voltage magnitude of a single-phase.

The unbalanced current measurement is shown in **Figure 100**. The 10% decrease in magnitude of phase B is observed to impact the current waveform slightly. The low impact indicates a very robust operation during the imbalanced phase magnitude. However, when analysing the THD an increase from 0.8% to 3.26% THD_I is noticed.

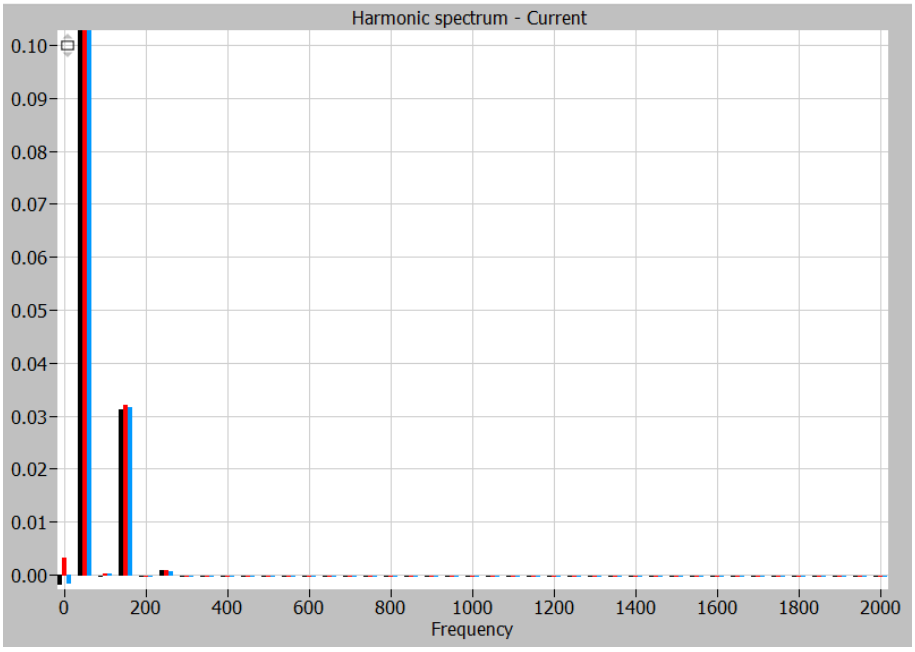

Figure 101: Harmonic spectrum of 10% decrease of voltage magnitude. Normalized to the fundamental frequency of 50 Hz, with magnitude '1'

Figure 101 depicts the harmonic spectrum of the AFE topology with imbalance of 10% in one of the phases. Similar to the 12-TR, DRMC and TRASPF a third harmonic distortion is observed, which indicates a trend. When 12-pulse converters are subject to imbalance, they will produce third

harmonic distortion. The reason for this third harmonic distortion occurrence is the imbalance between all the three phases. The unbalance causes current oscillations in the neutral wire, giving rise to third harmonic currents.

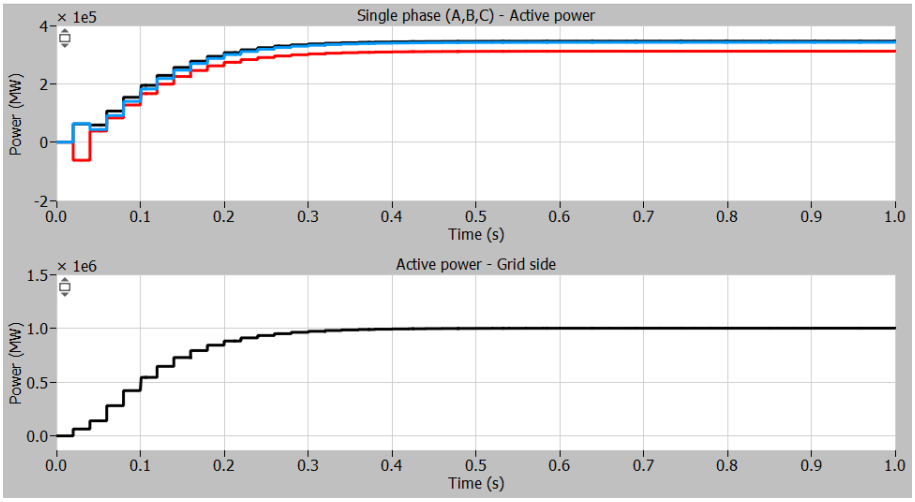

Figure 102: Single phase (A, B, C) and combined active power measurement, with a 10% decrease of phase B voltage magnitude

Figure 102 shows the active power for each phase and the summation of the individual phases. From Phase B (red line), a clear decrease in magnitude is seen due to the imbalance in the system. However, the combined active power still indicates full load of 1 MW, hence phase A and C compensate in order to adjust for the decrease in phase B. The achievement of 1 MW active power on the grid side indicates that the AFE can handle severe unbalanced conditions, by self-adjustments.

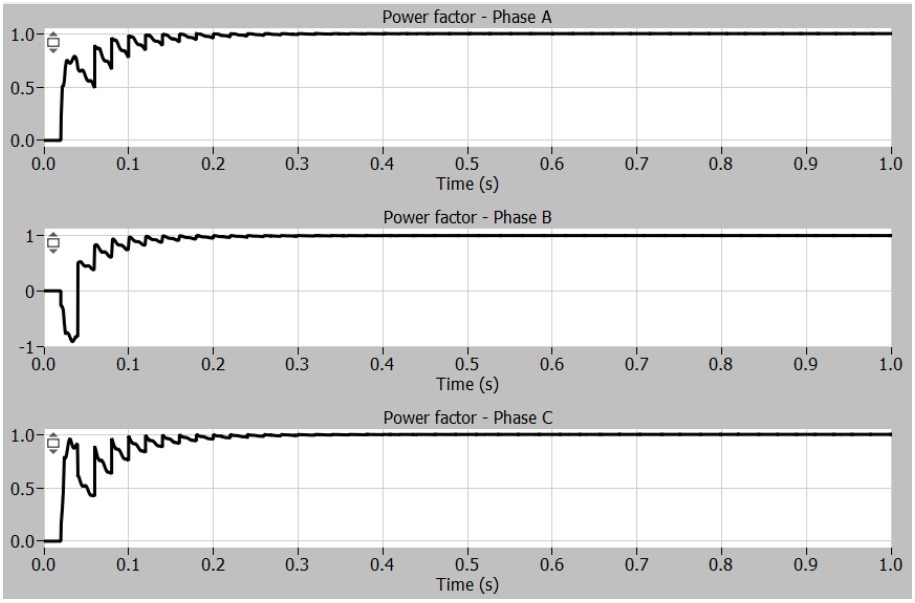

Figure 103: Single phase (A, B, C) power factor with 10% decrease of voltage magnitude.

The power factor of each phase is depicted in **Figure 103**. Each power factor has a unique transition before reaching steady state at approximately 0.2 milliseconds. An overview of measured distortions and power factors is illustrated in **Table 50**.

Table 50: Comparison between unbalance in magnitude and phase angle

Operating Conditions	**Balanced**	**Magnitude change**		**Phase angle change**	
Unbalance (%)	**0%**	**5%**	**10%**	**5%**	**10%**
Power factor – Phase A	0.99	0.99	0.99	0.99	0.99
Power factor – Phase B	0.99	0.99	0.99	0.99	0.99
Power factor – Phase C	0.99	0.99	0.99	0.99	0.99
$\boldsymbol{THD_I}$	0.80 %	1.77%	3.26%	3.4%	6.5%
$\boldsymbol{\Delta\, THD_I}$	-	0.96%	2.45%	2.59%	5.69%

Table 50 indicates the changes in power factor and THD_I with respect to the different types of unbalances. Grid voltage phase angle variation causes the biggest changes in the power factor and THD_I. This can be explained by a change in phase angle that may impact the alignment of the PLL. Hence the entire control loop will be altered. The high amount of distortion seen can be explained by the distortion power factor seen in **eq. 3** seen in **Section 1.3.**

3.4.4 Load Variation

Similar to the previous topologies, the load variation test has been conducted for the AFE, to evaluate the robustness of the topology. In order to conduct the test, the power delivered across the load is decreased in steps of 0.2 MW.

Table 51: Load variation results for the AFE topology.

Load Variation	100%	80%	60%	40%	20%
Active power	1 MW	0.8 MW	0.6 MW	0.4 MW	0.2 MW
Power factor	0.99	0.99	0.99	0.95	0.75
$\boldsymbol{THD_I}$	0.80 %	1.01%	1.34%	1.92%	3.06%
$\boldsymbol{\Delta THD_I}$	-	0.20%	0.53%	1.11%	2.25%

Table 51 shows the obtained results from the load variation test conducted on the AFE. The table documents the power factor and the THD of the AC current on the grid side. The results indicate high robustness of the topology as it maintains a high power factor and a very low THD over a large range of the partial load conditions.

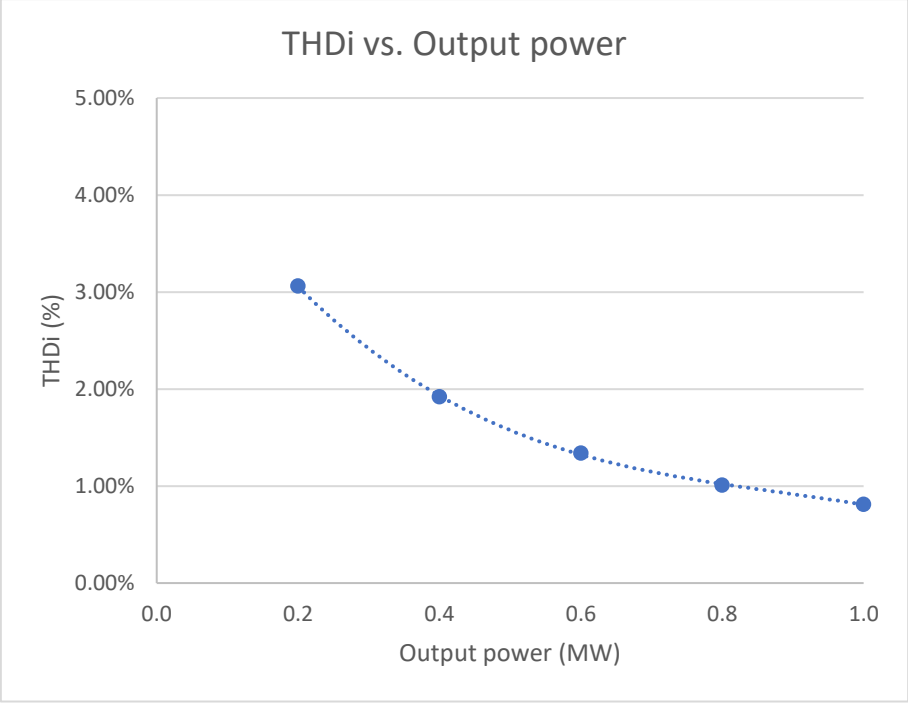

Figure 104: Load variation vs THD for the topology AFE

Figure 104 depicts an expected trend of decreasing current THD as the load increases. For the AFE the increase in THD is minimal compared to the previous topologies, showing a decrease from 3.1% to 0.8% current THD, as the load increases to 100%.

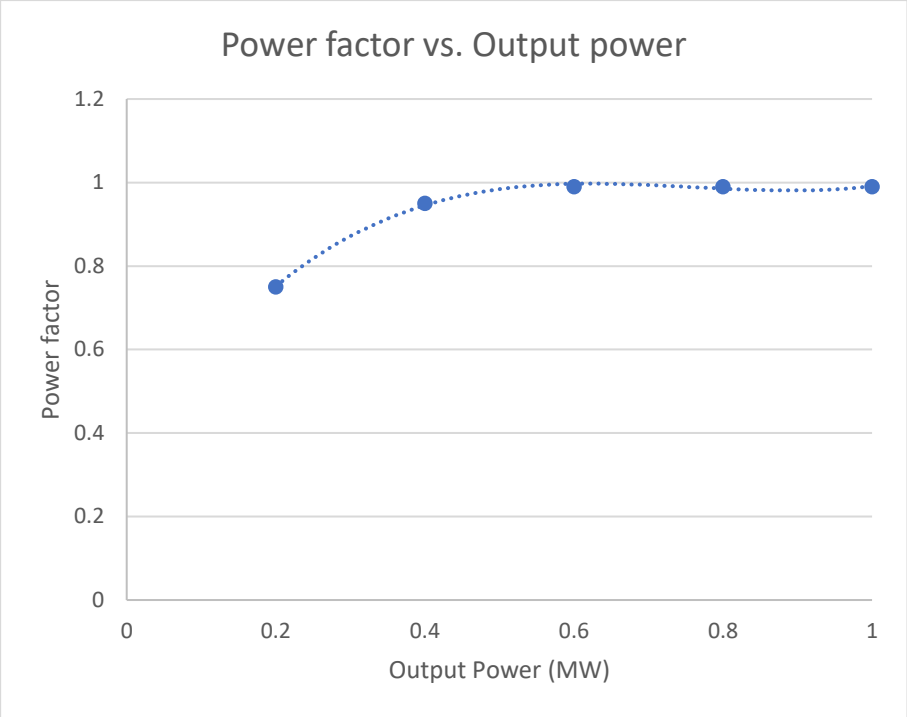

Figure 105: Load Variation vs Power Factor for AFE

Figure 105 depicts the power factor over the load variation range; the power factor is high or close to unity for all the variations except for load of 0.2 MW, where a decrease to 0.75 is observed.

The identical power factor and a small increase in harmonic distortion indicates the system is robust throughout the load variation test. Furthermore, the small increase in harmonic distortion is a positive indication for the topology to be able to operate in partial load conditions. However, when operating in partial load conditions, the reliability can be affected since the equipment operating might vary from the recommended values provided by the manufacturer.

3.4.5 Efficiency Calculation

The IGBTs of the topologies were analyzed for their ratings in order to determine the correct IGBT. The chosen commercial IGBT was the one with device name 'FF800R17KP4' and its ratings are shown in **Table 6** in **section 2.6.3**.

The efficiency test for the AFE is conducted similarly to the other topologies. Hence the thermal description is used in order to obtain the switching and conduction losses. A virtual heat sink is placed under an IGBT, in both the B6 circuit and the chopper circuit. The heat sinks will have a constant temperature which is set to 80° C. A probe is then attached to the IGBTs and switching losses and conduction losses can be calculated and subtracted from the DC Power output. There are additional losses from the transformers winding resistance, which were set to 13.94^{-3} Ω from the available datasheets.

Table 52: Efficiency estimation of the AFE

Load Variation	100%	80%	60%	40%	20%
Input active power	1.01 MW	0.81 MW	0.60 MW	0.40 MW	0.20 MW
Output active power	0.97 MW	0.77 MW	0.57 MW	0.38 MW	0.18 MW
Efficiency	95.70%	95.67%	95.43%	94.66%	91.5%

Table 52 depict the efficiency estimation of the AFE. The efficiency increases, as load increase thus a higher efficiency is achieved when the system is operating in full load conditions.

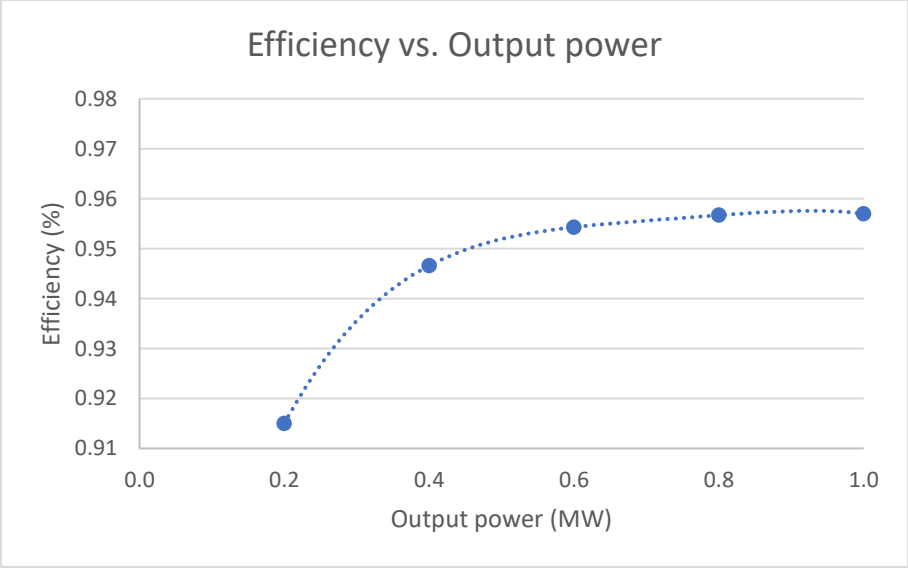

Figure 106: Efficiency vs power for AFE

Figure 106 portrays the efficiency measured at different loading conditions. The plot is made with the results obtained from **Table 52**, hence the previously explained trend is clearly noticed.

4 MODULAR MULTICELL RECTIFIER – A NOVEL APPROACH

All the priorly discussed P2X converter topologies (12-TR, 12-DRMC, 12-TRASPF & AFE) include an unavoidable 12 pulse three winding Low Frequency Transformer (LFT) in the system. It happens to be the one of the largest components in the system, which is accompanied by various complications such as transportation, installation, and footprint occupation. To avoid these intricacies, the emerging research focuses on the idea of eliminating the voluminous LFT from such a P2X converter system by a novel topology called Modular Multicell Rectifier (MMR).

Below in **Table 53**, **Table 54**, and **Table 55**, the component parameters, AC/DC control parameters, and DC/DC control parameters used in all simulation tests of the MMR are shown respectively:

Table 53: parameters used in components of MMR.

Parameters of control scheme	Values
V_{Grid}	0.69 kV
L_{Cell}	1^{-3} H
R_{Cell}	0.001 Ω
C	2000^{-6} H
DC	1 kV
C_{DC}	100^{-6} F
R_{Load}	1 Ω

Table 54: Parameters used in AC/DC control system for MMR.

Parameters of control scheme	Values
K_{P1}	0.1
K_{I1}	5
K_{P2}	75
K_{I2}	50

Table 55: Parameters used in DC/DC control system for MMR.

Parameters of control scheme	Values
K_{P1}	0.001
K_{I1}	2
K_{I2}	10

The above table parameters in **Table 53**, **Table 54** and **Table 55** refer to **Figure 107**, **Figure 110**, and **Figure 112** respectively.

4.1 MMR Topology & its Control

One of the promising novel converter topologies named as Multi Modular Rectifier (MMR) topology manages to eliminate the LFT as shown in **Figure 107**. It has a modular design which allows it to equally distribute the higher grid voltage to smaller voltages between the basic converter cells in this topology. The basic unit (converter cell, **Figure 108**) consists of 2 stages; the first stage converts the AC power from the grid side to DC power using an AC/DC converter. The next stage in the topology uses a DC/DC converter which is connected to the AC/DC converter via a DC link capacitor. It receives the DC output from the AC/DC converter and converts it to the required DC output value via a high frequency transformer (HFT).

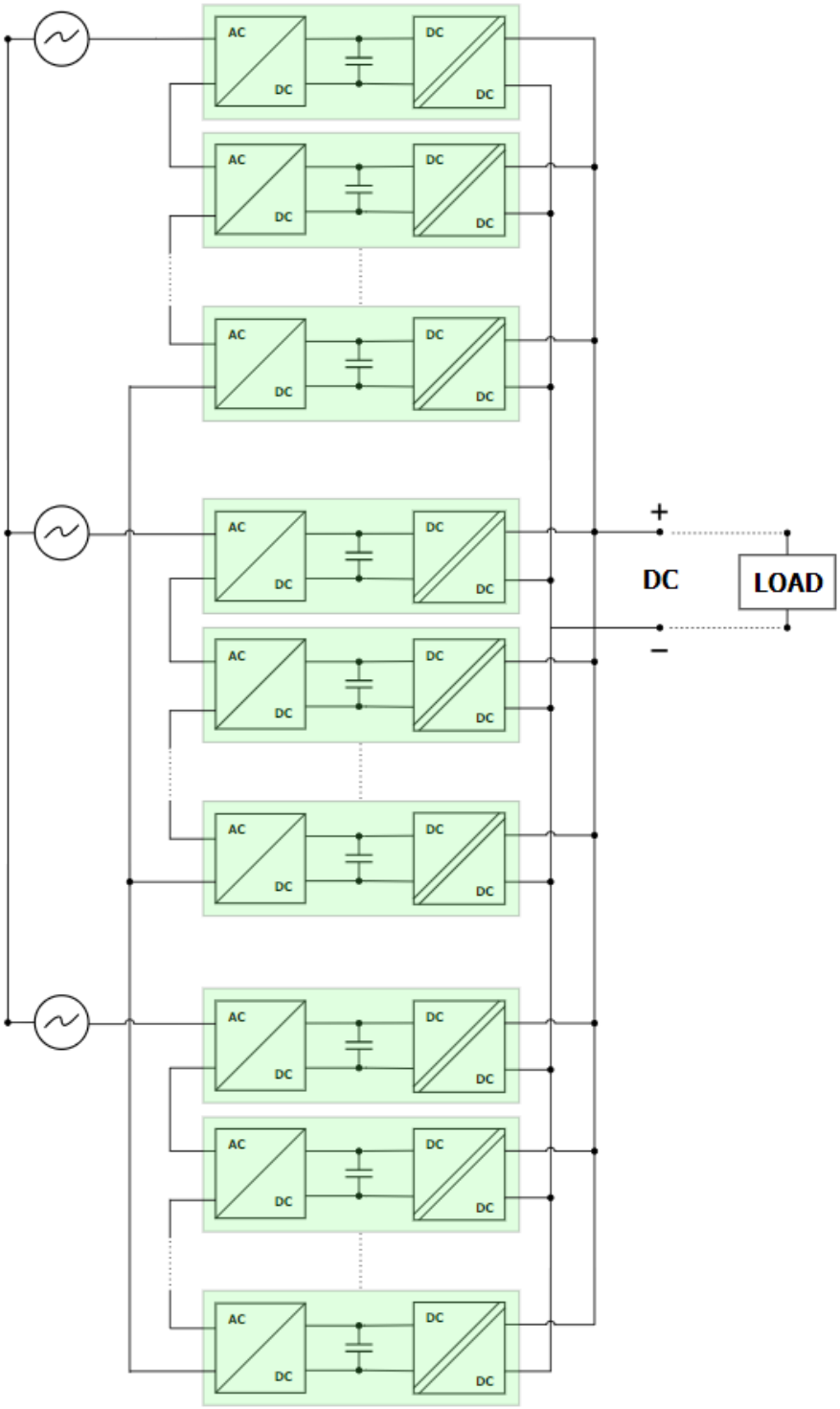

Figure 107: Circuit Diagram of Modular Multicell Rectifier (MMR)

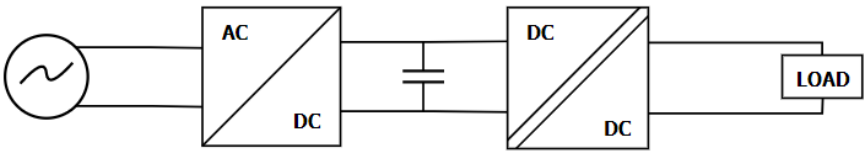

Figure 108: Single Cell construction in the MMR Topology

The modular design of this topology enables to scale the system to higher ratings while also providing the flexibility. Due to the cascaded configuration of the converter cells, Si IGBTs and Si MOSFETs can be used ahead of the DC/DC galvanic isolation in each converter cell.

The realization of the single-phase AC/DC converter can be attained by various well established topologies such as B6 and Flyback Converter to name a few, but in this case the 'totem pole bridgeless boost Converter' [46] has been implemented as shown in **Figure 109.** The 'totem pole bridgeless boost converter' converts the AC input to DC as the output.

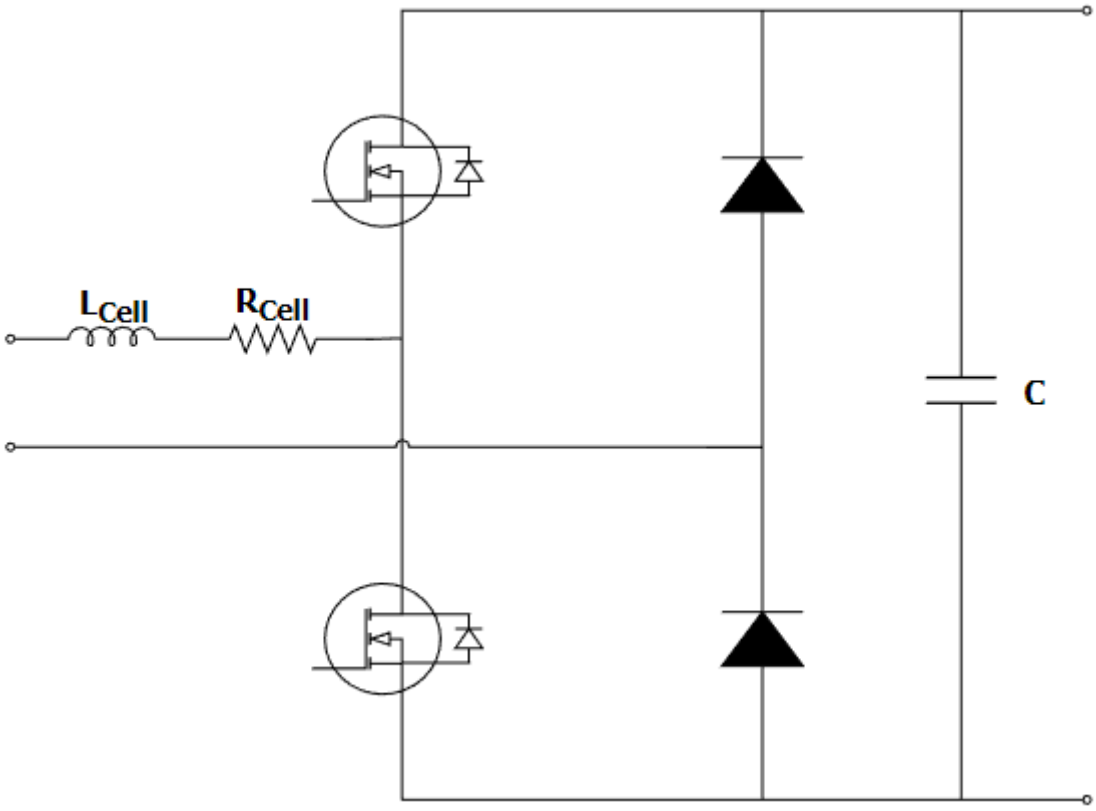

Figure 109: Totem pole bridgeless boost converter configuration (AC/DC Stage)

A closed loop control algorithm has been implemented to control the 'totem pole bridgeless boost Converter', as shown in **Figure 110**Error! Reference source not found.. The Controller receives t he DC output feedback and sends control signals to the AC/DC converter, which provides the desired output on the DC side.

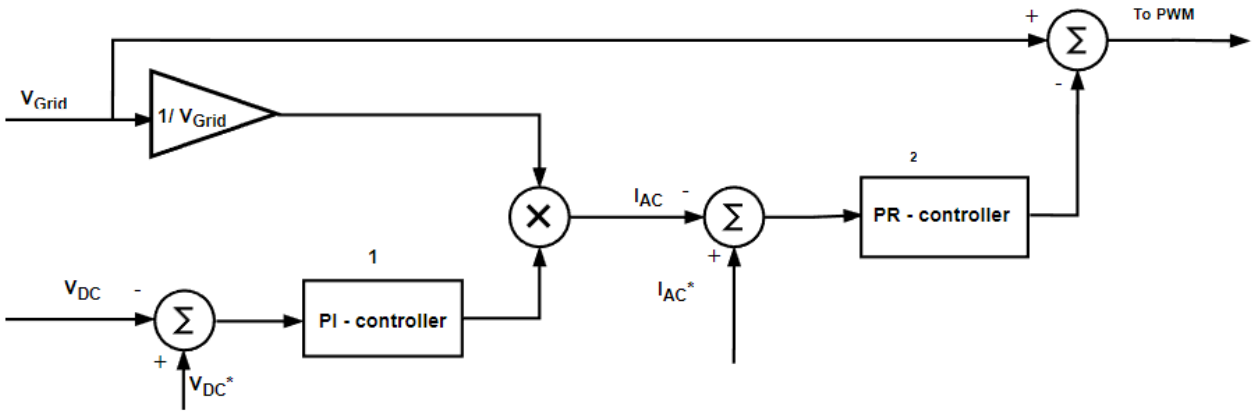

Figure 110: Control technique for AC/DC Converter

The implementation of the DC/DC converter topology can be realized by various well-established topologies such as Dual Active Bridge (DAB) or LLC converter to name a few. In this case, the DAB topology as shown in **Figure 111,** has been implemented. The DAB has essentially two stages. In the 1st stage it converts the DC voltage to AC and steps it up or down via the HFT. In the 2nd stage this AC voltage from HFT gets converted back to the DC voltage as the output.

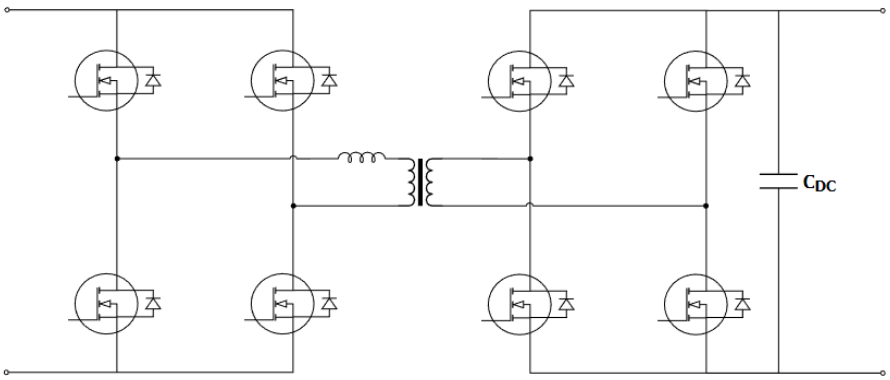

Figure 111: Dual Active Bridge configuration (DC/DC Stage)

To control the converter, a PI controller has been used, which receives the feedback from the system output and generates control signals for the Dual Active Bridge as shown in **Figure 111** to achieve the desired voltage level.

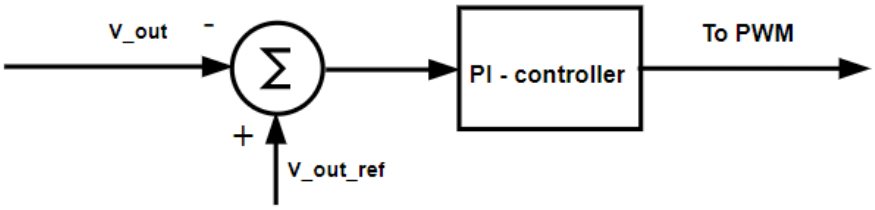

Figure 112: Control technique for DC/DC Converter

Since high frequency transformers (HFTs) or medium frequency transformers (MFTs) are used in this topology; it significantly reduces the size of the system due to the small volume and light weight of the MFTs & HFTs. As the HFTs and MFTs are implemented in the DC/DC converters, MOSFETs are chosen as the switches as they are designed to operate in higher frequency ranges [47], [48]. The highly modularized design brings in complexity in terms of components and control to the system.

4.2 Footprint & Reliability of Modular Multicell Rectifier

Due to the highly modular design of this topology, the input grid voltage is split up into smaller voltages among the modules eliminating the need of a bulky LFT. This is one of the main advantages of this topology as the LFTs occupy a larger footprint and add significantly to cost of the whole setup. Additionally due to the bulky nature of these LFTs, complications arise in other aspects such as transportation, designing & installation. Due to the elimination of the LFTs, the MMR topology occupies a significantly lower footprint.

Another big advantage of this topology due to its highly modular design is the higher reliability of MMR. As the separate modules deliver smaller levels of power to the P2X system, in case one or more of the modules fail, the rest of the modules will still be able to deliver the power to the load at a slightly lower level. Hence, even in case of the failure of some components, this topology still manages to work giving it a high reliability score.

4.3 MMR simulation and results

This section describes the performance of the MMR simulations and documents the corresponding results. The aim of this section is to evaluate the performance of this novel topology and

consequently compare to the other state of art topologies discussed in earlier sections. The simulations are run for various tests under different conditions.

4.3.1 Cell Design

A fundamental cell needs to be designed as shown in **Figure 108** for the P2X system to be simulated. For the total power transfer of '1 MW' across the system, every phase will carry a total active power of '333.33 kW', as the power is split into three sperate phases. The input phase voltage, '33 kV' needs to be distributed into various smaller values for the fundamental cell. The value of '690 V', being one of the values of various commercial devices has been chosen. Hence splitting the value of '33 kV' into cells of '690 V', input voltage will determine the number of cell modules to be used, which are 48 cell modules.

Hence every phase will have 48 cell modules which will transfer '333.33 kW' of power to the system. Therefore, every cell delivers the power of '6.94 kW' of power as the power will be spilt into 48 modules.

The above calculations show that a converter cell can be designed for any value of power and voltage level, which shows the flexibility of this topology. It is theoretically possible to design for any number of cells to transfer the desired power across the system, which makes this topology highly modular. Additionally, if one of the cells stops functioning, the power rating will be reduced slightly without stopping the overall operation, which accounts for its high reliability. **Table 56** documents the specifications of the basic MMR cell for this particular case.

Table 56: Specifications of MMR Cell Module

Input Voltage	690 V
Output Voltage	1000 V
Rated Power	6.94 kW

Due to the limitations of the computation power of the available equipment, all the analysis of the MMR topology has been performed on a smaller scale for the proof of concept. The model used for analysis has 1 cell for every phase; hence the overall power rating will be approximately 21 kW as the power will only be delivered by the 3 modules in the three phases. The implemented topology can be seen in **Figure 113**.

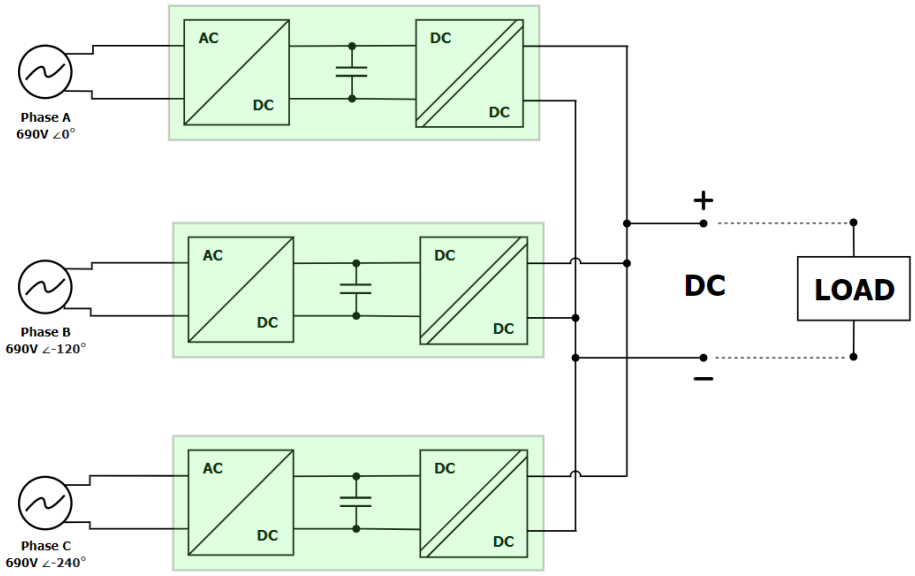

Figure 113: MMR Topology used in the Simulations

4.3.2 Output under ideal full load conditions

The ideal full load conditions are when the full '21 kW' power is transferred across the P2X plant as shown in **Figure 114**, unlike the previous cases where the topologies delivered '1 MW' power across the P2X plant.

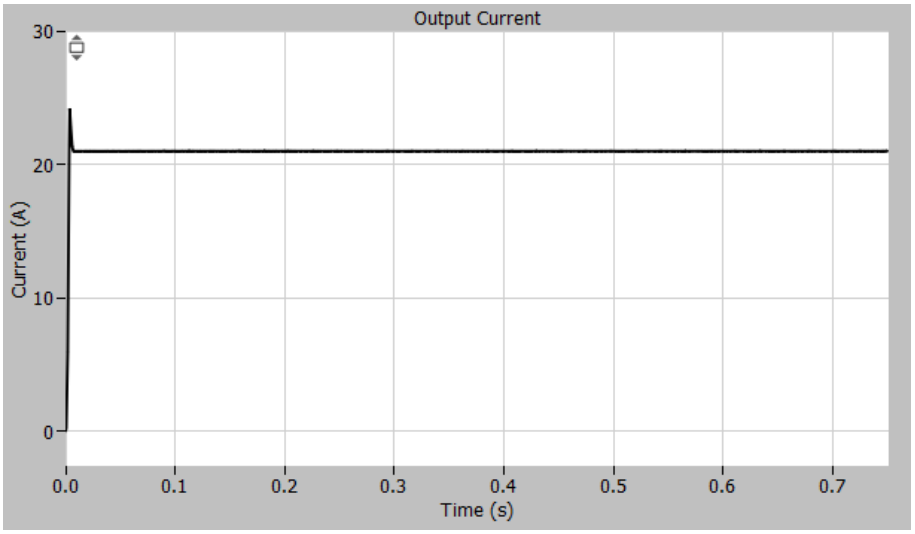

Figure 114: Output DC Current from MMR

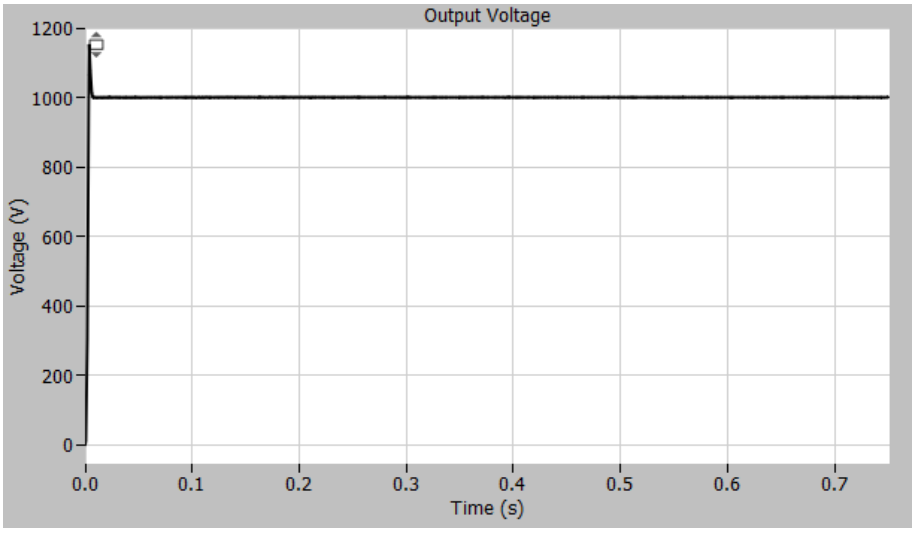

Figure 115: Output DC Voltage from MMR

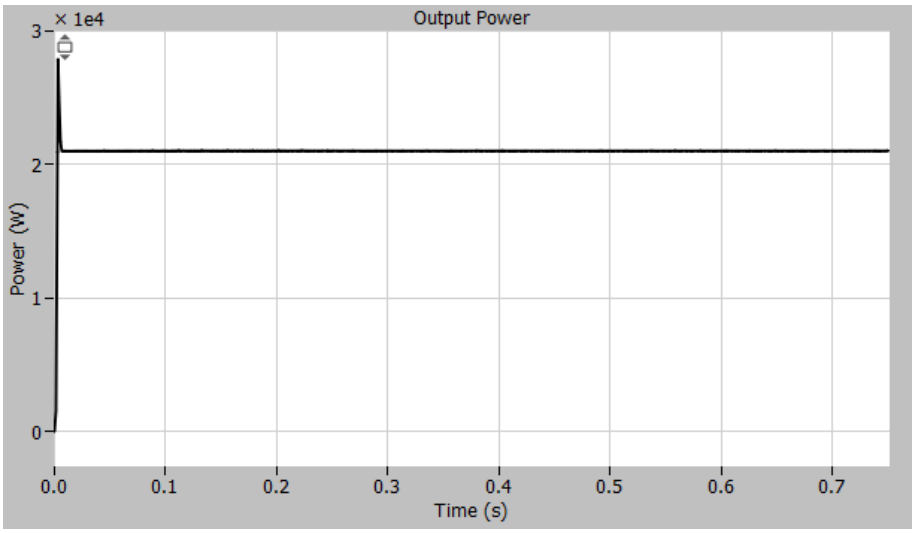

Figure 116: Output Power from MMR

Figure 114, **Figure 115** & **Figure 116** show the output current, voltage, and power across the load in the P2X system. The output voltage is '1 kV' as set by the controller. The current in this case is lower than the previous topologies, due to the previously discussed small-scale version of the simulated model. **Table 57** documents the general parameters of the implemented model.

Table 57: Relevant Parameters of Modular Multicell Rectifier

Parameters	Value	Unit
RMS current grid-side	17.55	A
RMS voltage grid-side	398.37	V
Active power grid-side	20.97	kW
Apparent power grid-side	20.98	kVA
Power factor grid-side	0.99	-
Current DC-side	20.98	A
Voltage DC-side	1	kV
Active power DC-side	20.98	kW

4.3.3 Harmonic Analysis

To assess the power quality of a system, harmonic analysis is performed. The harmonic analysis evaluates the harmonics of the grid side current as shown in **Figure 117**. The current signal being purely sinusoidal with some insignificant distortions results in a very low THD value of approximately 2.5 %.

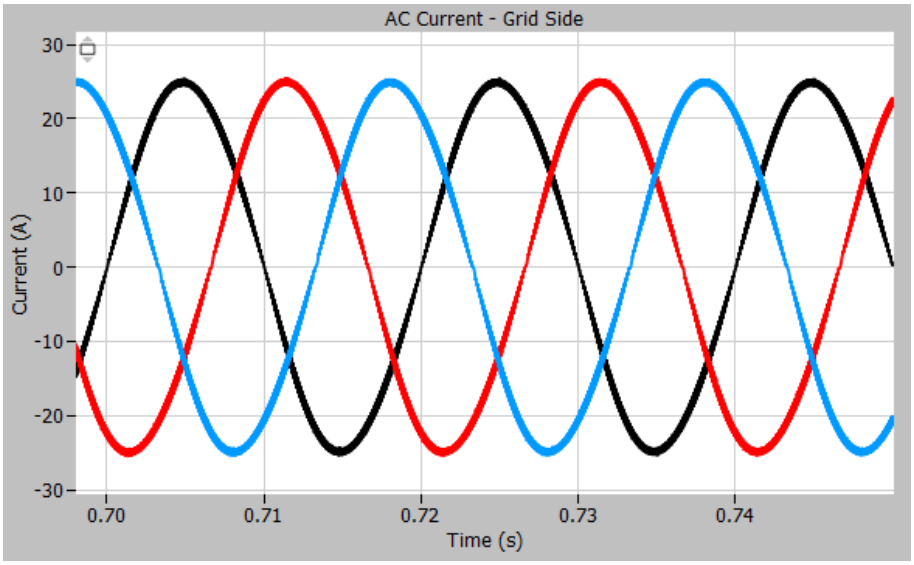

Figure 117: Grid Side AC Current

The FFT tool PLECS tool has been used to show the distribution of the harmonics. **Figure 118** shows the harmonic distribution of the grid side current, only a small presence of the 3rd harmonic in the system. All other harmonic orders are approximately zero which brings the THD to a very low value of approximately 2.5% for each phase. The accurate values of the harmonics and THD are provided in **Table 58**:

Table 58: Overview of the most significant harmonic orders

Harmonic orders	THDi
3rd harmonic	1.66 %
5th harmonic	0.02 %
THD	2.55 %

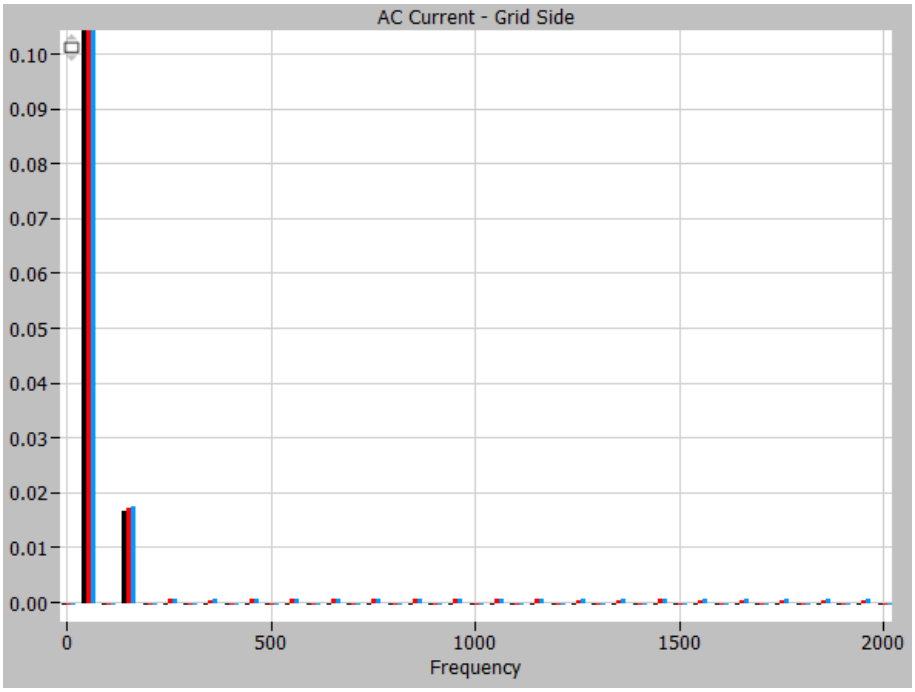

Figure 118: Harmonic Analysis of the Grid Side Current

Figure 119 show Apparent Power, Active Power & Power Factor in plots 1,2 & 3 respectively. The values of Apparent Power & Active Power in the plots follow the values in **Table 57**. The power factor maintains the value of around 1 at the steady state, which is better than most of the other topologies discussed earlier in the report.

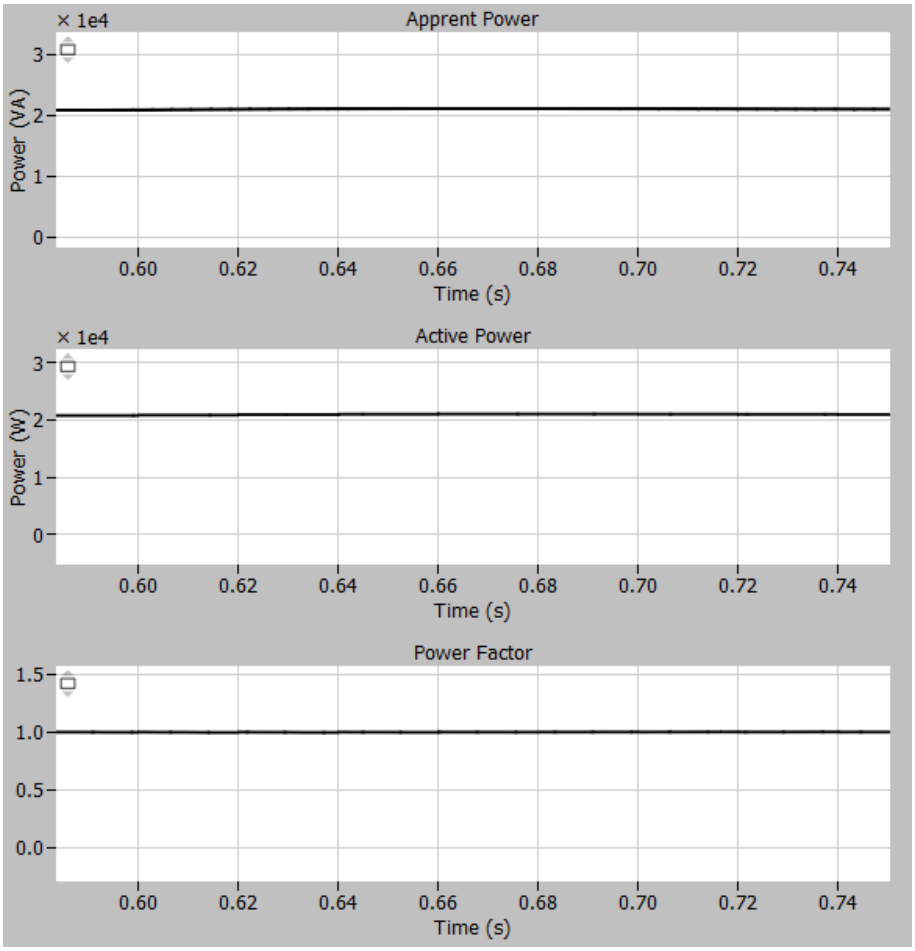

Figure 119: Apparent Power, Active Power & Power Factor from Grid Side for MMR

4.3.4 Unbalance Grid

To investigate the impact of the unbalanced grid on the load, a change in either of magnitude or phase angle is induced in phase B. The unbalance study will be performed for phase B with a 10% drop in magnitude and further unbalances will be documented later in this section.

Figure 120 shows the grid voltages under the unbalanced grid with a drop of 10% in the voltage magnitude of phase B. The current magnitude of one of the phases increases but the grid currents maintain its sinusoidal shape in each of the phases as depicted in **Figure 121**.

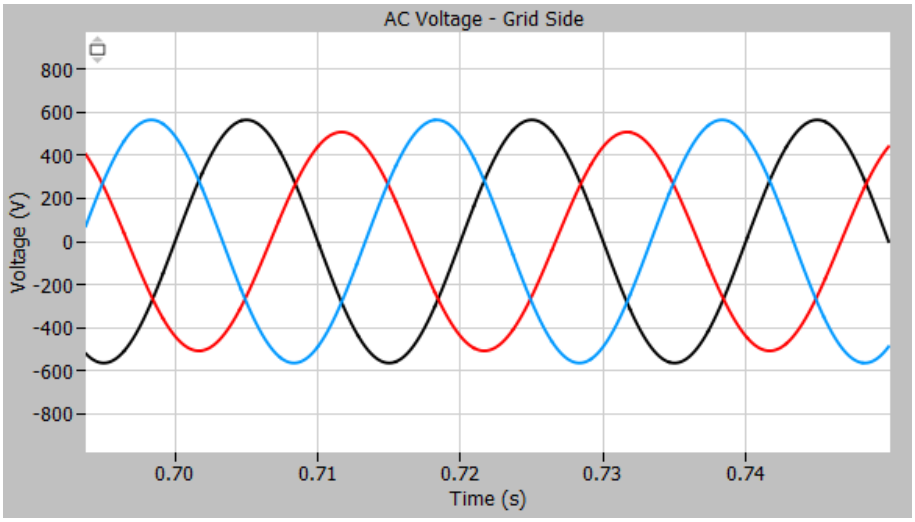

Figure 120: Grid Side Voltages under unbalanced condition

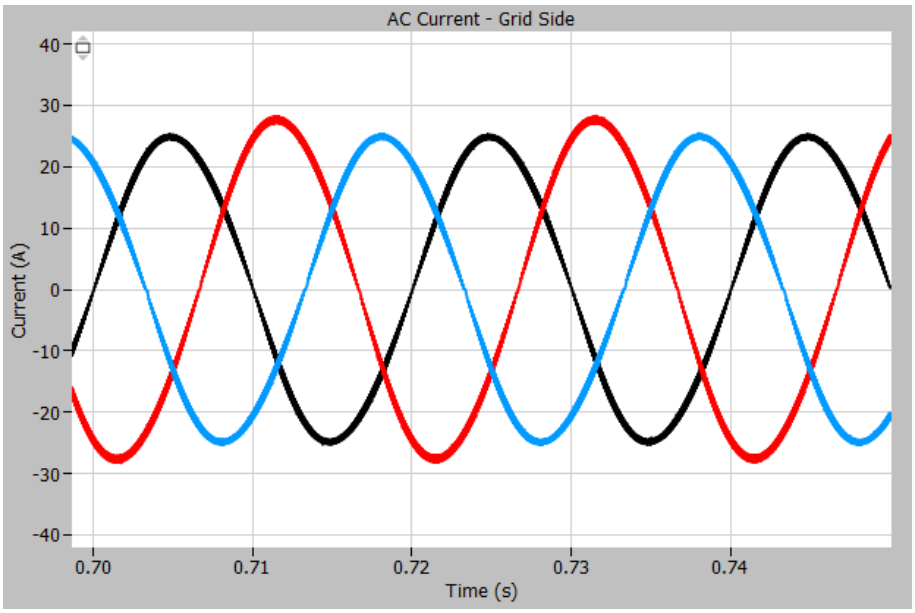

Figure 121: Grid side currents under unbalanced condition

The FFT tool in the PLECS scope evaluates the harmonic spectrum of the grid side current, which is shown in **Figure 122**. There is a small presence of 3rd harmonic which is approximately 2%. This is the similar harmonic order as seen in the balanced ideal conditions in the last section which again indicates the robustness of the system to the unbalanced grid. Additionally, the harmonics seem unevenly distributed for different phases, which depicts unbalance, but the change is small and can be neglected.

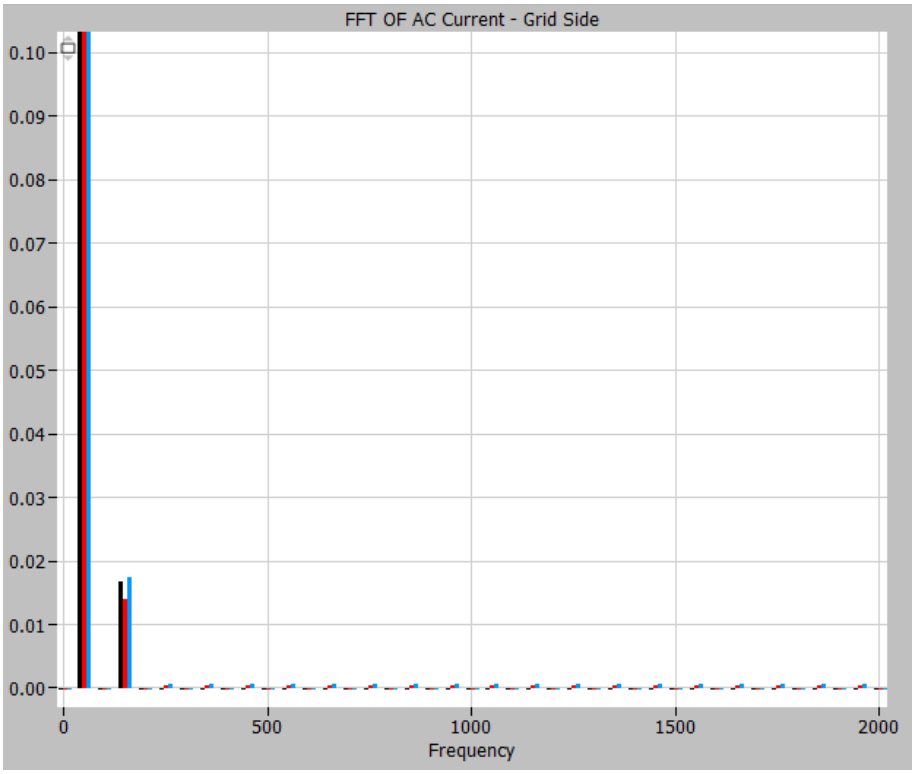

Figure 122: Harmonic spectrum during the unbalance for MMR topology. Normalized at the fundamental frequency of 50 Hz

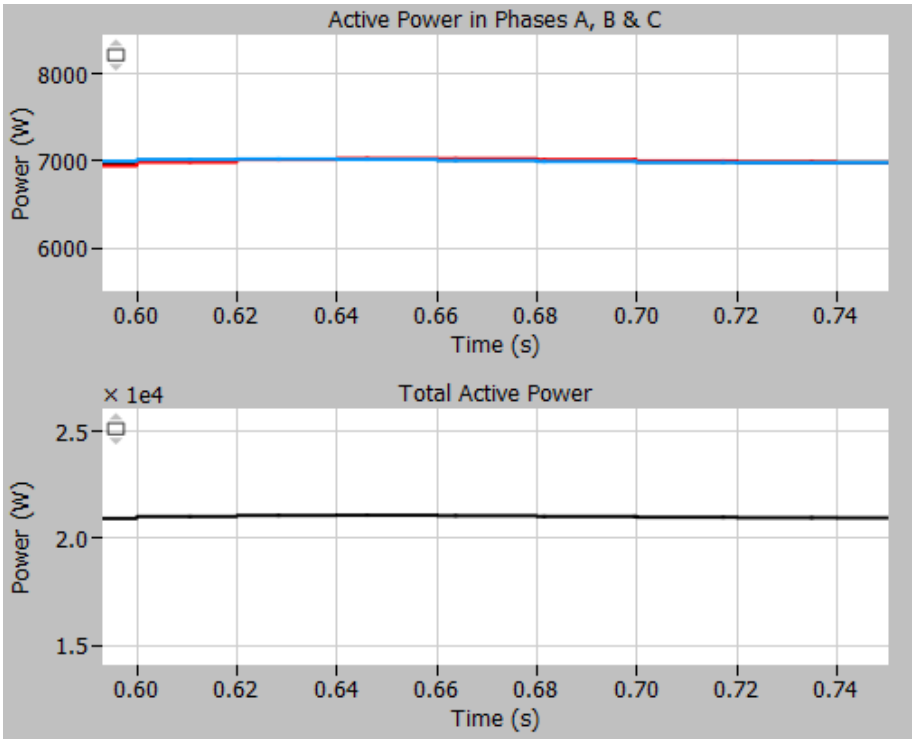

Figure 123: Active Power of Single Phases A, B & C & Total Grid Side Active Power

Figure 123 shows the active power for each phase in the 1st plot and the total active power from the grid side in the 2nd plot respectively. Due to the unbalance in the system, initially there seems to be unequal power sharing between the phases but as the system moves towards the steady state, the power is shared equally among the phases, which again illustrates the robustness of the topology. It further portrays that the topology can handle severe unbalances in the grid without any significant changes in the system parameters. It manages to transfer the 21 kW of power across the P2X plant successfully.

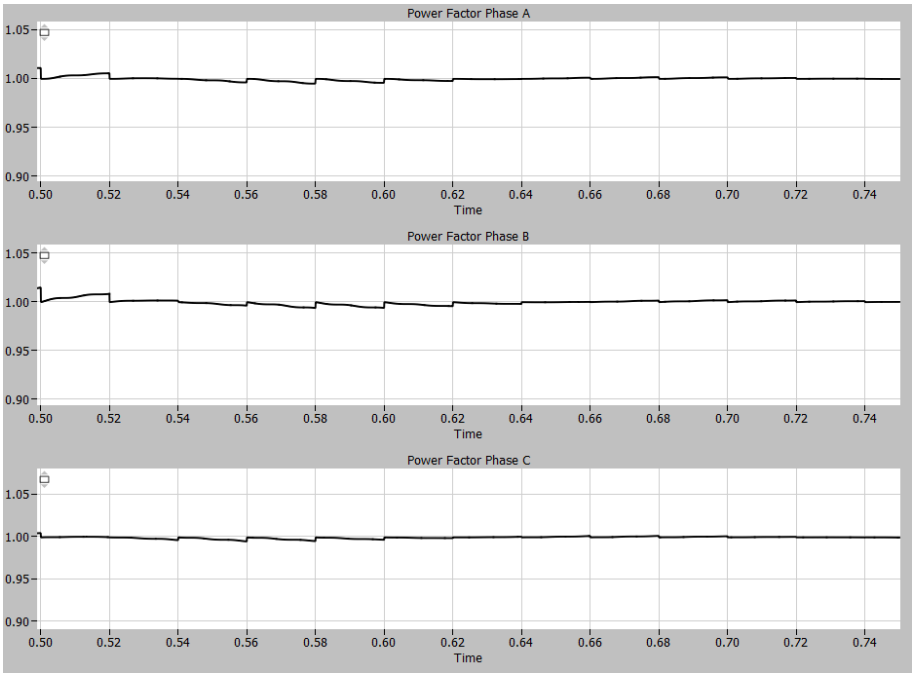

Figure 124: Single phase (A, B, C) power factor during the unbalanced grid.

The power factor of each phase is outlined in the **Figure 124** after the system has reached steady state. The power factor of all the phases is almost unity even after the imbalances in the grid; the accurate values are presented in **Table 59,** which presents the overview of unbalances under different conditions.

Table 59: Overview of power factor and current THD with unbalanced grid

Operating conditions	Balanced	Magnitude change		Phase angle change	
Unbalance (%)	0%	5%	10%	5%	10%
Power factor – Phase A	0.99	0.99	0.99	0.99	0.99
Power factor – Phase B	0.99	0.99	0.99	0.99	0.99
Power factor – Phase C	0.99	0.99	0.99	0.99	0.99
THDi	2.49 %	2.48%	2.48%	2.50%	2.49%

From **Table 59** it can be concluded that the imbalance has essentially no effect on the power factor on the system while using MMR topology. Further the imbalance has no effect on the THD, which remains practically consistent during the imbalances.

4.3.5 Load Variation

The load variation test evaluates the performance of the topology under different load conditions. The test is performed similarly to the tests performed in the previous topologies with the load being varied at the steps of 20% of the full load from 100% to 20%. **Table 60** documents the load variation and its corresponding effects at different steps.

Table 60: Load Variation Analysis for MMR

Load	100%	80%	60%	40%	20%
Active power	20.98 kW	16.79 kW	12.59 kW	8.39 kW	4.19 kW
Power factor	0.99	0.99	0.99	0.99	0.99
THDi	2.55 %	2.90 %	3.58 %	5.01 %	9.48 %

Table 60 shows that there in an increasing trend in THD with the decrease in load as illustrated in **Figure 125,** which shows an inverse effect of the output power (load) with respect to the current THD.

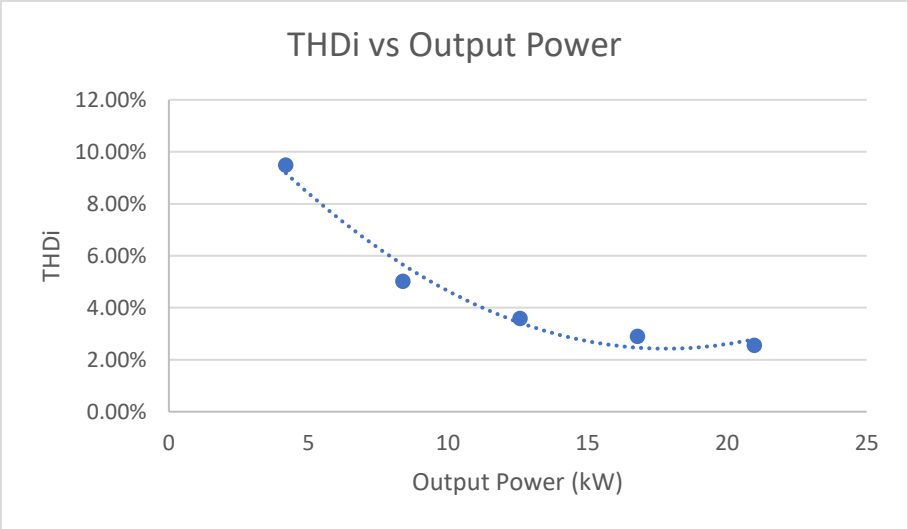

Figure 125: THD vs. Output Power for the MMR Topology

Figure 126 shows the graph of Power Factor vs Load variation which remains constant throughout the process of load variation. The topology maintains a very high constant power factor without the requirement of a filter.

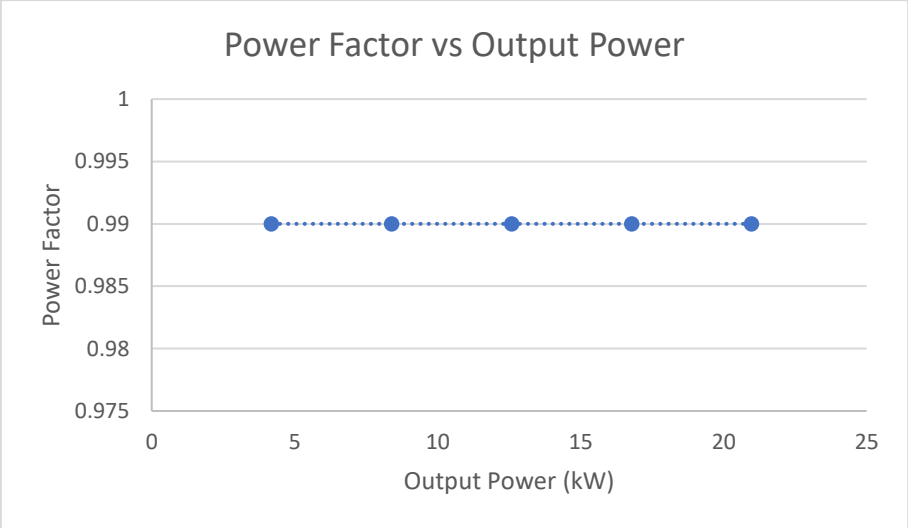

Figure 126: Power Factor (Phase A) vs. Load variation for the MMR Topology

4.3.6 Efficiency Calculation

This section estimates the efficiency of the MMR topology by comparing the power from grid side to the power delivered to the load for the P2X system **Table 7**, **Table 61**, **Table 62** & **Table 63** represent the commercial semiconductor devices used in the PLECS simulation for the MMR topology in the P2X system. These devices have been added to the PLECS platform via 'thermal

description' tool available in the software. The guide in [49] has been used to choose the correct set of the MOSFETs.

Table 61: Commercial Diode Parameters for MMR Simulation[36]

Parameters	MMR Diode ratings	25% Safety Margin Ratings	Vishay 12F
V_D	685 V	860 V	1200 V
I_{FSM}	26 A	33 A	265 A
$I_{F(RMS)M}$	13 A	17 A	19 A
$I_{F(AV)M}$	8 A	10 A	12 A

Table 62: Commercial MOSFET Parameters for MMR Simulation [50]

Parameters	DC/DC MOSFET Grid Side	25% Safety Margin Ratings	Semikron SK80MB120CR03TE1
V_{Dss}	685 V	860 V	1200 V
I_D	60 A	75 A	98 A

Table 63: Commercial MOSFET Parameters for MMR Simulation [51]

Parameters	DC/DC MOSFET Load Side	25% Safety Margin Ratings	Semikron SKM260MB170SCH17
V_{Dss}	1000 V	1250 V	1700 V
I_D	40 A	50 A	378 A

Table 64: Efficiency estimation of MMR

Load variation	100%	80%	60%	40%	20%
Input active power	20.98 kW	16.78 kW	12.59 kW	8.39 kW	4.20 kW
Output active power	20.98 kW	16.78 kW	12.59 kW	8.39 kW	4.20 kW
Efficiency	99.27 %	99.35 %	99.43 %	99.51 %	99.62 %

Table 63 estimates the efficiency of the MMR topology at different partial loads. **Figure 127** plots the efficiency with respect the output load across the P2X plant which indicates the efficiency

slightly decreases while increasing the load as demonstrated by the trendline. Generally, the efficiency of MMR topology remains high in all partial loading conditions.

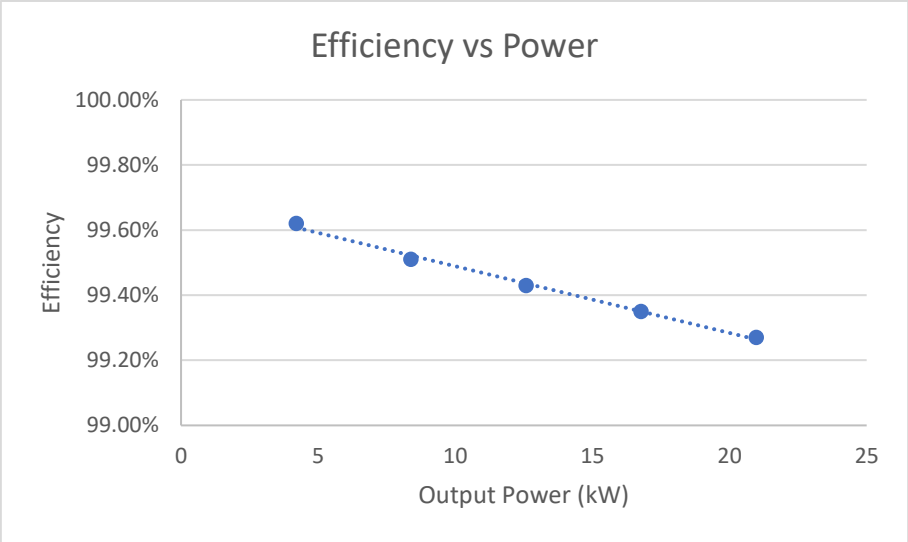

Figure 127: Efficiency vs Power graph for MMR

5 COMPARISON

In this report various power electronic converter topologies have been discussed for power conversion from the power grid to the load side of a P2X plant. This section aims for the detailed comparison of the discussed power electronic topologies according to various aspects such as power quality, load variations, unbalanced grids, and efficiency. All the results shown in this section will include the 12-TR, 12-DRMC, and 12-TRASPF topologies with their respective filters. Furthermore, the control complexity, footprint, reliability, and cost will be briefly discussed.

5.1 Power quality

Power quality is the measure, study and enhancement of sinusoidal waveform at the rated voltage and frequency and is one of the most important features of any system [52]. In order to ensure safe operation, the topologies must follow requirements stated in various grid codes and standards related to the location of installation. The commercial equipment must be selected based on extensive research of the topology and the power quality requirements stated by the grid codes and standards. For verification and comparison purposes, the harmonic spectrum and the power factor are evaluated in order to analyze the power quality of the different power electronic converters in each topology.

5.1.1 Harmonic analysis

In case of the harmonic spectrum, the topologies using 12 Pulse converters i.e., 12-TR, 12-DRMC, and 12-TRASPF with their respective filters have a presence of 12*n ± 1 harmonic, where n is a positive integer but due to the filters used, the most dominant 12 ± 1 harmonics are suppressed bringing the THD level very well under the grid requirements.

In the advanced AFE topology, there is no significant presence of harmonics and the overall THD remains to be below 1%, while the novel MMR topology shows a small presence of 3rd harmonic and the THD is measured to around 2.5%. **Table 65** shows the THD comparison of all the investigated topologies, which is graphically described in **Figure 128**.

Table 65: THD Comparison of every topology.

Topology	12-TR	12-DRMC	12-TRASPF	AFE	MMR
THDi	1.34 %	1.63 %	0.82 %	0.8 %	2.53 %

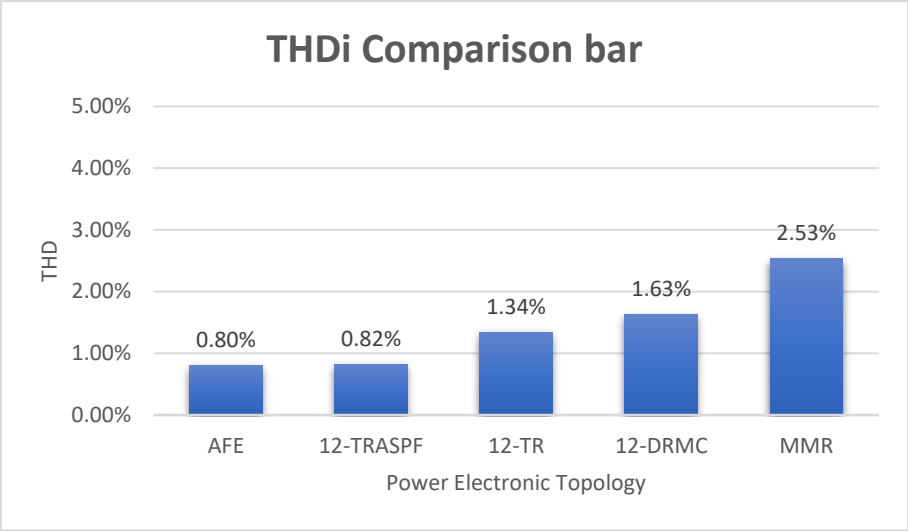

Figure 128: Overview of each topology THDi from best to worst.

Figure 128 portrays the THDi measurements for every topology in ideal conditions; hence the passive and active filters are connected in their respective topologies. Furthermore, it must be noticed that the MMR topology is simulated at much lower power levels of 21 kW. Hence the THD is expected to be lower in case of the actual scale of 1 MW.

5.1.2 Power Factor

Power factor (PF) is one of the most important characteristics of an electrical system, regarding the power quality. The power factor indicates how efficiently the topology converts the apparent power from the grid to the active power into the system. Various techniques can be employed to improve the PF of the system. Passive filters, active filters and Power Factor Correction Boost converter are some of the methods which have been implemented in this work in order to improve the PF of the discussed topologies.

Table 66: Power factor of different Topologies

Topology	12-TR	12-DRMC	12-TRASPF	AFE	MMR
PF	0.99	0.95	0.94	0.99	0.99

Table 66 documents the PFs of different topologies, which are also illustrated in **Figure 129,** showing a comparison of PF in different topologies. The trap filter improves the power factor of the 12-TR to a higher extent in contrast to the active filter used in the 12-TRASPF. The PF of the TRASPF could be further improved, as discussed in **Section 3.3** at the expense of higher cost and footprint.

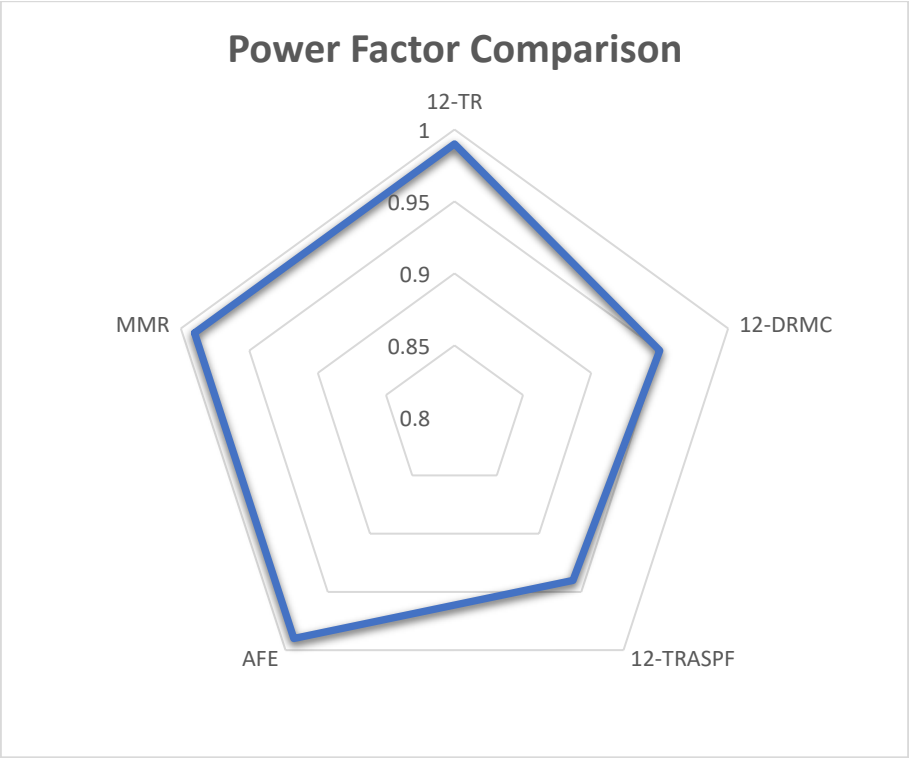

Figure 129: Radar Graph showing Power Factor of different topologies

5.2 Unbalanced Grid

The unbalance study is examined to determine how the topologies react to the unbalances in the grid. The changes will be evaluated in order to investigate the robustness of the topology. The evaluation will be based on the resulting THD and PF during the unbalanced conditions.

Table 67: Power Factor at different unbalance operation conditions

Operating condition	Balanced	Grid Voltage Magnitude change		Grid Voltage Phase angle change	
Unbalance (%)	0%	5%	10%	5%	10%
Power factor 12-TR	0.99	0.98	0.94	0.97	0.93
Power factor 12-DRMC	0.95	0.91	0.85	0.93	0.81
Power factor 12-TRASPF	0.94	0.91	0.85	0.91	0.87
Power factor AFE	0.99	0.99	0.99	0.99	0.99
Power factor MMR	0.99	0.99	0.99	0.99	0.99

Table 67 shows the power factor for each simulation during unbalance operation. The phase angle change has the biggest effect on each of the topologies. However, with the more complex topologies as the AFE and MRR there seem to be no effect from the unbalance on the power factor, which indicates their robustness.

Table 68: THDi at different unbalance operation conditions

Operating condition	Balanced	Grid Voltage Magnitude change		Grid Voltage Phase angle change	
Unbalance (%)	0%	5%	10%	5%	10%
THDi 12-TR	3.64%	8.00%	13.96%	18.63%	32.78%
THDi 12-DRMC	2.12 %	9.99 %	17.86 %	19.69 %	33.03 %
THDi 12-TRASPF	0.90%	8.00%	13.90%	13.90%	25.00%
THDi AFE	0.81 %	1.77%	3.26%	3.40%	6.50%
THDi MMR	2.49 %	2.48%	2.48%	2.50%	2.49%

Table 68 depicts the THDi for every topology, similarly to the analysis from **Table 67** the phase angle has a severe effect on the simpler topologies. However, the complex topologies, such as AFE and MRR depict their robustness and result in smaller deviations.

With 10% phase angle change the simpler topologies such as 12-TR, 12-DRMC & 12-TRASPF, show huge increase of THDi. The distortion originates from the system being unstable due to the mentioned change. The instability comes from the phase change which will consequently enforce this change in the topologies which are not able to handle these severe changes, altering the settings

of the PLL in the relevant topologies. Since the AFE and MMR are both active rectifiers, they are able to adapt to the phase change even in the severe cases.

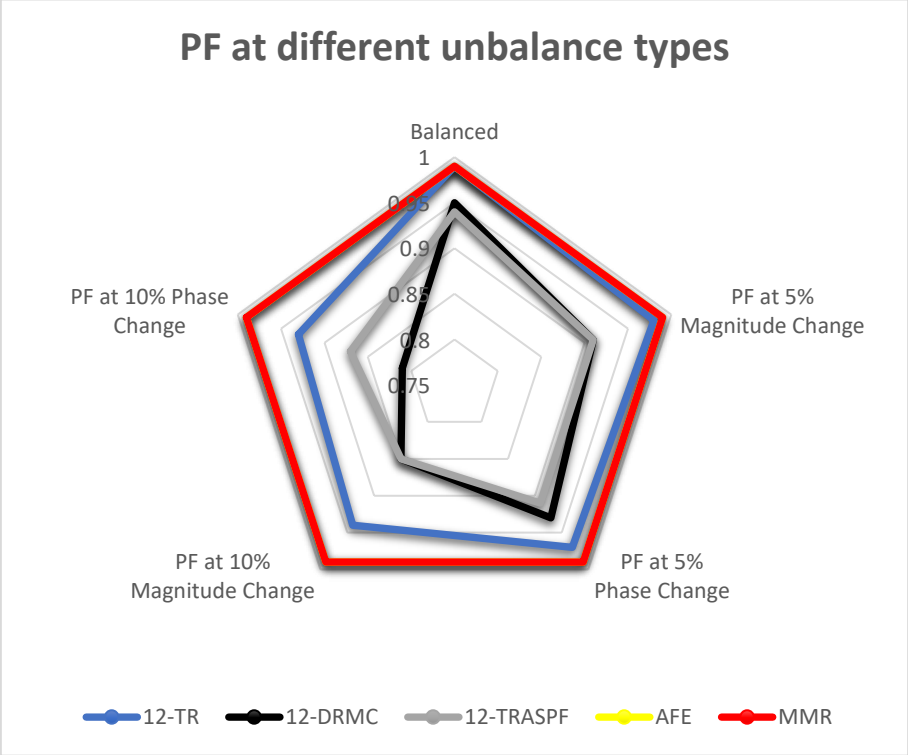

Figure 130: Radar Graph showing Power Factor of all the discussed topologies at different unbalance types

Figure 130 depicts a radar diagram of the power factor for each topology under the different unbalanced and balanced condition. As previously discussed, the AFE and MMR show the highest PF for all the unbalanced grid voltage conditions.

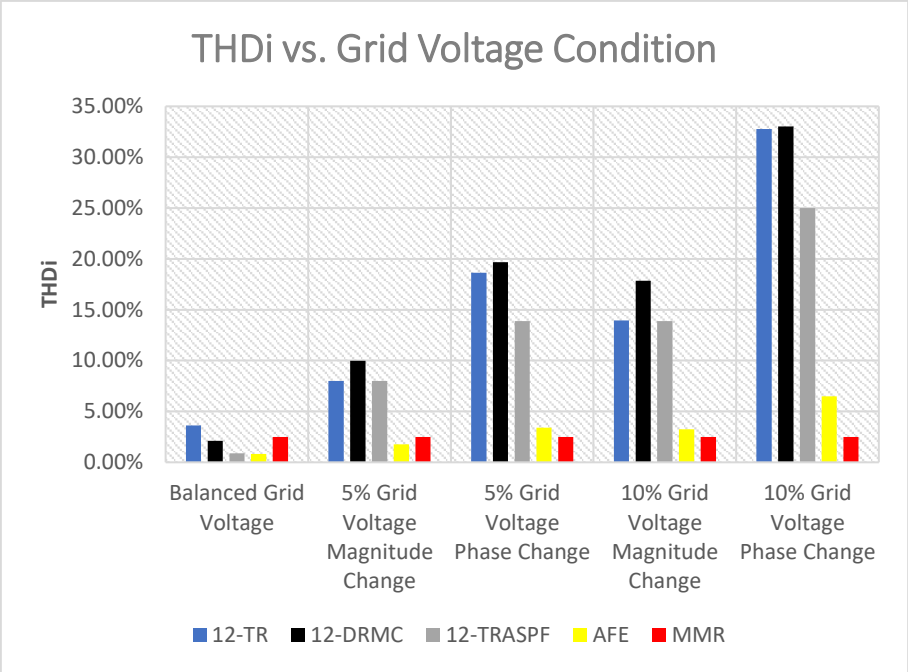

Figure 131: THD at different unbalance types

Figure 131 depicts the current THD values for each topology during the balanced and various other unbalance operating conditions. The 12-pulse converter topologies show significant increase of THDi during these unbalances, while the more robust topologies, which are AFE & MMR can remain consistent with the grid standards, due to their superior control techniques.

5.3 Load Variation

This section compares the response of all the discussed power electronic topologies to the changes in the load. The feedback of the topology to the changes in the load indicates the robustness of that particular topology.

Table 69: Power Factor at different load variations

Topology	12-TR	12-DRMC	12-TRASPF	AFE	MMR
PF at 100% load	0.99	0.95	0.94	0.99	0.99
PF at 80% load	0.98	0.90	0.89	0.99	0.99
PF at 60% load	0.97	0.79	0.83	0.99	0.99
PF at 40% Load	0.98	0.62	0.77	0.95	0.99
PF at 20% load	0.92	0.34	0.74	0.75	0.99

Table 69 shows the power factor for every topology by the load variation. This table indicates that most of the topologies are very robust to the load variations, while the DRMC shows significant decrease of power factor at partial loads.

Table 70: THD at different load variations

Topology	12-TR	12-DRMC	12-TRASPF	AFE	MMR
PF at 100% load	3.64 %	2.12 %	0.8 %	0.81 %	2.55 %
PF at 80% load	4.64 %	2.29 %	1.5 %	1.01 %	2.90 %
PF at 60% load	4.96 %	2.33 %	1.9 %	1.34 %	3.58 %
PF at 40% Load	5.45 %	2.07 %	1.5 %	1.92 %	5.01 %
PF at 20% load	6.06 %	1.66 %	2.8 %	3.06 %	9.48 %

Table 70 depicts the THDi of each topology, most of the topologies are able to meet the grid requirements even in the partial load of 20%. However, some of the topologies are not able to meet these grid requirements under partial load conditions, thus requiring them to disconnect from the grid during those circumstances.

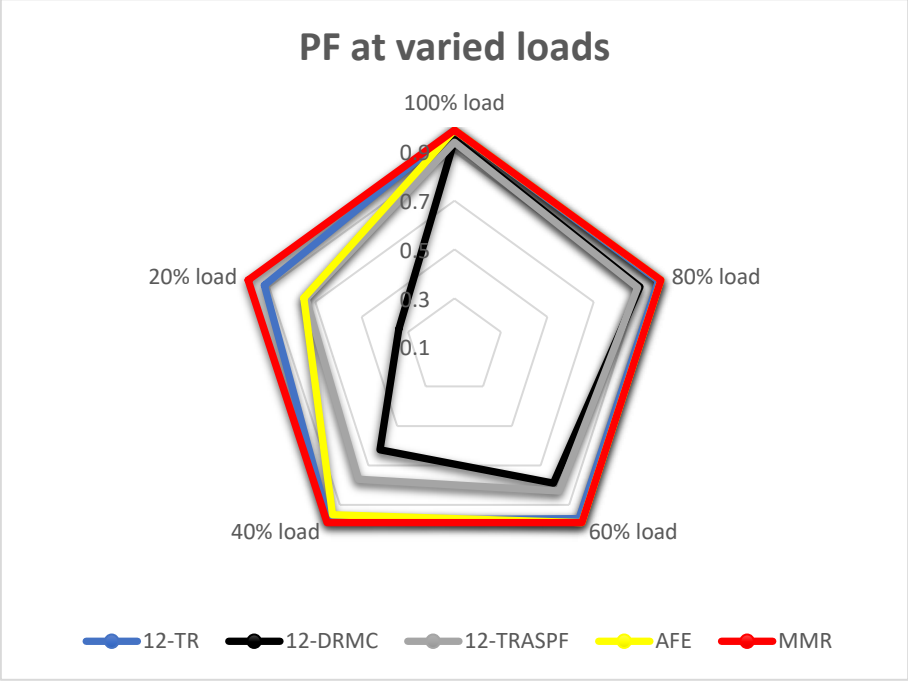

Figure 132: Power Factor at different load variations

Figure 132 depict the power factor for each topology during load variation. The illustration show a high degree of robustness if the radar diagram is filled out to the edges. Hence the only topology which is able to maintain a high-power factor during all the partial load conditions is the MMR. The

12-TR is also able to follow up very closely. AFE proves to be robust until the partial load of 40% and afterwards has a dip in the performance.

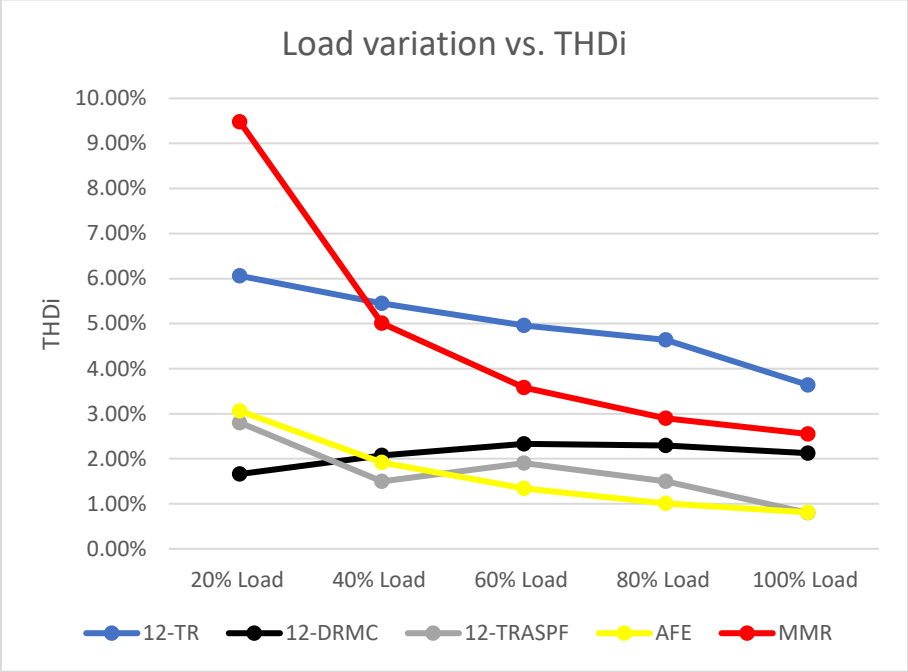

Figure 133: THD at different loads

Figure 133 illustrates the THDi during load variation. AFE, 12-DRMC & 12-TRASPF exhibit robustness to the changing load. MMR shows a significant increase in THDi when running at 20% load compared to the other topologies. The increase to current distortion is contradictive to the otherwise high-power factor. As the MMR simulations are run at an output power of 21 kW. The results can be expected to be much better in terms of THD for the actual 1 MW scale of the system.

5.4 Efficiency

This section estimates the efficiency for each of the topologies. The expected dips in the efficiency are majorly from the transformers and the semiconductor devices among other components. The switching frequency plays a significant role in the efficiency. For the case of the transformers, LFTs produce higher losses leading to decrease in the efficiency while as MFTs & HFTs produce lower losses leading to higher efficiencies. MMR topology uses HFT and hence producing less losses while as the rest of the topologies use LFTs leading to higher losses, which gives the MMR an edge in the efficiency estimation.

In case of the semiconductor devices, the frequency is proportional to the losses produced in the system. Hence the higher frequencies lead to higher losses, consequently leading to lower efficiency systems. In the investigated work, the topologies operate at higher frequencies leading to higher losses, hence lowering the efficiency values.

It is important to clarify that with the correct cooling of the semi-conductors, the switching frequency will not be a problem. However, it is very likely that natural cooling will not be sufficient to cope with the heat produced due to the high switching frequency. Therefore, cryogenic cooling would be optimal and possibly increase the efficiency further [53].

The efficiency of the power electronic topologies is investigated in terms of active power inputted from the grid to the active power delivered across the load. The efficiency will be estimated at different partial loads to assess the performance of the individual topologies.

Table 71: Efficiency at different load variations

Load variation	100%	80%	60%	40%	20%
Efficiency of 12-TR	98.94%	98.89%	98.81%	98.66%	98.35%
Efficiency of 12-DRMC	95.83%	95.52%	94.96%	93.93%	91.18%
Efficiency of 12-TRASPF	96.00%	95.24%	94.00%	91.56%	84.30%
Efficiency of AFE	95.70%	95.67%	95.43%	94.66%	91.50%
Efficiency of MMR	99.27%	99.35%	99.43%	99.50%	99.62%

Table 71 documents the efficiency for every topology at varied loads. As expected, the 12-TR has the highest efficiency, due to the simplicity of the topology. 12-DRMC, 12-TRASPF, and AFE all have high losses due to the use of various semiconductor devices which have a significant loss due to their operation at higher switching frequency. Further losses are injected by the LFTs among other devices. MMR shows high efficiency due to the absence of the LFT, which injects significant losses as expected.

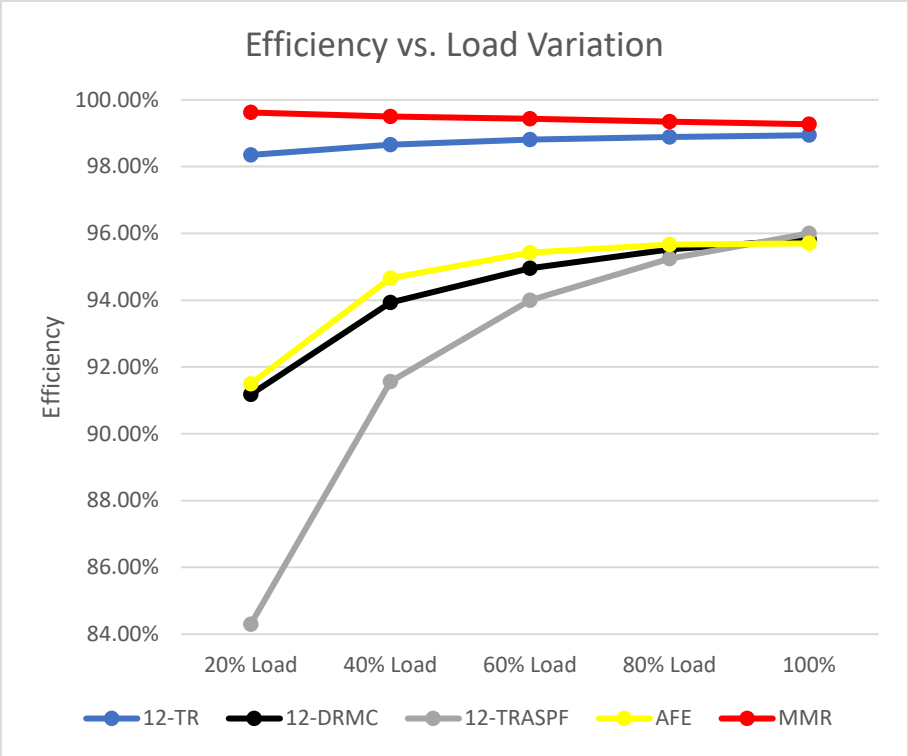

Figure 134: Efficiency at different loading conditions for all the discussed topologies

Figure 134 illustrates the efficiency of the topologies investigated at partial loading conditions. As expected, 12-TR and MMR show very high efficiencies and stay constant over different load variations. 12-DRMC & AFE start from lower values, while 12-TRASPF starts with the lowest efficiency at 20% partial load, further leading to higher efficiency as the system converges to full loading conditions. The lower efficiency of the 12-TRASPF in lighter loading conditions is due to the losses in the IGBTs in the active filter, which account for a higher percentage in this scenario. As the higher reactive power compensation leads to higher currents in the active filter, this leads to higher losses as mentioned in **section 3.3**.

5.5 Complexity, Cost, Reliability, & Footprint

While the main focus of the project has mostly been concerned with the technical aspect of the topologies, as a method of comparison between the topologies, there are other aspects which are also essential, such as cost, reliability, footprint, and control complexity. While a quantitative analysis of cost, reliability and physical footprint have not been carried out in order to provide estimated values for each topology. It is still possible to compare the topologies based upon fundamental principles of these parameters.

Based on the control schematics of the four state-of-the-art topologies shown in **Chapter 2**, it was possible to compare control complexity. The AFE, followed by the 12-TRASPF have control loops of higher complexity, while the DRMC's complexity depends on the number of interleaving stages implemented. The 12-TR has the least complex control, as it is also the simplest topology with the least number of components. The MMR being a highly modular topology brings high control complexity to the system.

Footprint is concerned with the area occupied by each topology. One of the largest contributors to the footprint is the transformer used in the implemented state-of-the-art power electronic rectifiers. An estimation of the size of LFT transformers has been conducted in **Section 2.4**. **Figure 22** shows the footprint estimation with respect to the transformer ratings. However, the sizes of semi-conductor and corresponding heatsinks were not evaluated. Therefore, an estimated footprint can only be conducted based on the transformers in each topology. Since the MMR uses a high frequency transformer the footprint will be lower than the four state-of-the-art topologies. Furthermore, the 12-TRASPF topology requires an additional transformer for the active power filter, which significantly increases the footprint**.** The 12-TR and the 12-DRMC include passive filters, which increases the footprint of these topologies as well. These observations in effect conclude that the AFE has similar or less footprint to the 12-TR and 12-DRMC, as no passive trap filter or active filters are used in the AFE topology.

A quantitative investigation for the reliability has not been carried out, thus the comparison of the topologies will be evaluated in terms of number of components. Starting with the MMR topology, the number of components will be irrelevant since the topology includes redundancy for each cell. If one of the cells in the MMR fails, it still continues to operate which indicates a very high reliability. 12-TR being the simplest topology with least complexity is also expected to perform with high reliability. In comparison, DRMC, AFE & 12-TRASPF are contemplated to be less reliable.

The cost is related to all the aforementioned parameters. However, for a system to operate optimally, there will often be trade-offs between the cost factor and the overall quality of the topology in terms of reliability, power quality or efficiency. Due to these trade-offs between cost and quality, the optimal solution depends ultimately on customer demands. Generally, the simplest topologies are the most cost effective. Hence 12-TR will have the least cost demand, as it includes

the least number of components. In comparison the other topologies will have higher cost demands as they are more sophisticated.

5.6 Comparison Overview

This section gives an overview of the different topologies while comparing them with each other, regarding the discussed aspects in previous sections. To compare the topologies, a table of merits has been devised, allowing to decide for the most optimal topology, which can be seen in **Table 72**. The table will consist of each topology and corresponding measurement indicators obtained from the investigation conducted in this work. The indicators used for the table of merits can be seen below.

Table 72: Comparison of topologies regarding relevant criterions

Topology	12-TR	12-DRMC	12-TRASPF	AFE	MMR
Power Quality	+	O	O	++	++
Robustness	O	-	O	++	+
Efficiency	+	O	-	O	++
Complexity	++	+	-	-	--
Cost	+	O	-	-	+
Footprint	O	O	-	O	++
Reliability	++	+	O	O	++

++	+	O	-	--
Superior	Satisfactory	Neutral	Unsatisfactory	Inferior

In **Table 72**, the power quality computation combines the aspects of harmonic analysis, power factor, grid unbalance & load variation based on the results obtained in this work. In parallel, robustness is computed from the outcome of the load variation & grid unbalance results. **Table 72** is graphically illustrated in **Figure 135**.

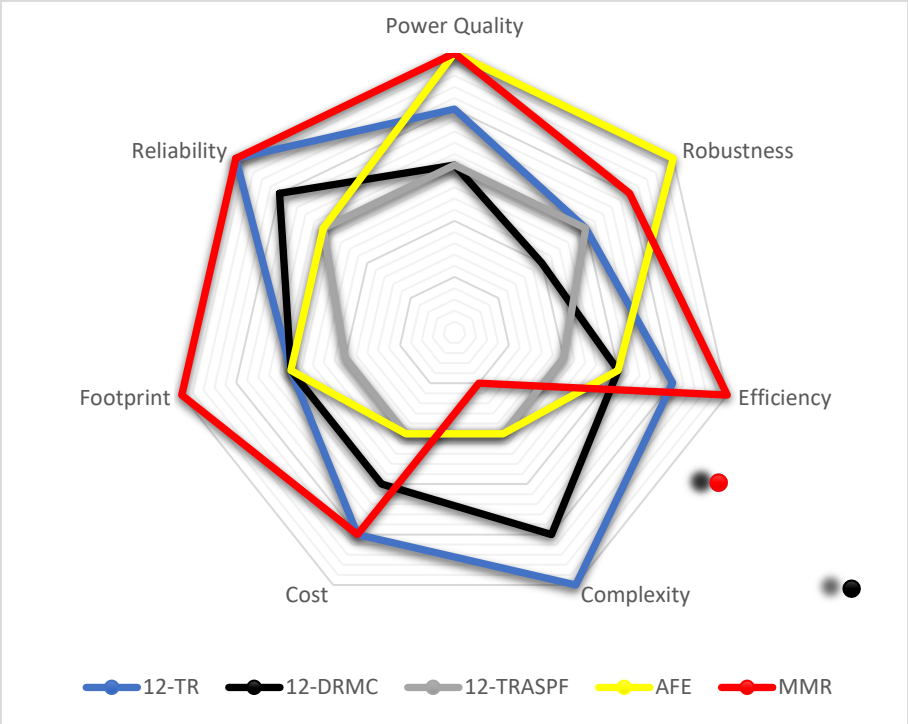

Figure 135: Graphical Comparison of different topologies among various aspects

6 CONCLUSION & FUTURE WORK

6.1 Conclusion

The objective of this work was to design and simulate the state of art MW level power electronic converter solutions for P2X applications. Further, the simulated topologies were run through various tests (power quality, robustness & efficiency) to determine their overall performance in order to compare them with each other. The designing and the simulations were successfully implemented in the PLECS, and their properties were analysed via extensive simulation testing in order to draw conclusions based on fundamental power quality aspects. The additional objectives were to estimate the footprint, reliability, cost, and complexity of the topologies for the purpose of comparison.

The conventional 12-TR is characterized as superior in terms of efficiency, complexity, reliability, footprint & cost, while it also provides adequate power quality. The 12-DRMC takes up the least space and hence performs outstanding in the footprint aspect, while it performs in an acceptable range for all the other investigated aspects; however, it achieved poor results in the aspect of robustness. The 12-TRASPF, whose topology consists of a 12-pulse Thyristor rectifier and a B6 converter-based shunt active power filter, provides a very low THD while compromising on the other aspects such as footprint, reliability, and efficiency. The AFE performs superior in terms of the power quality, robustness, and footprint. It delivers the least THD and an almost unity power factor without the need of any additional filter or compensation measures, while being robust to all the external changes. This superior performance comes at the expense of complexity & reliability, which also translates to its higher costs.

Another important goal of this work was to introduce a novel topology and evaluate its performance. Hence a promising topology, Modular Multicell Rectifier (MMR) was explored in detail which eliminates the bulky LFT used in all of the earlier mentioned topologies.

MMR demonstrates superior power quality and efficiency in contrast to the investigated state of art topologies. It imparts a low THD and an almost unity power factor without the need of any additional filter or compensation measures while providing adequate robustness. The MMR topology operates in the higher frequency range and hence uses much smaller medium/high frequency transformers

(MFTs/HFTs), which have a significantly smaller weight and occupy smaller footprint than the Low Frequency Transformers (LFTs) used in the four state-of-the-art topologies. Since the MMR has a highly modular design, it contributes to a higher reliability, at the expense of higher complexity of the topology.

6.2 Future Work

In this section, related future work for the project is suggested. The suggestions are seen as further improvements to the already obtained results or as additional objectives, which would further verify the already existing results. The future work will also highlight extra work, which was not within the scope of this thesis or was neglected due to the time constraints on the project.

- The switching frequency for each of the topologies, should be decreased to avoid high switching losses during efficiency tests. However, as there is a trade-off between the accuracy and the power losses, an overall uniform switching frequency, which would match all four state-of-the-art topologies needs to be further investigated.
- Further analysis of the Cost, Reliability, and Footprint are required. These aspects will highlight important factors, which need to be considered in commercial setups. Cost is an essential factor, which can govern how the design of an actual consumption plant is implemented.
- The grid impedances and transformer setting for all four state-of-the-art topologies could be investigated further. Additional losses over the grid lines and transformer would have a significant impact on the efficiency of the topology and hence provide the most accurate results for each topology.
- As the 12-TRASPF topology investigated in this thesis only included an active power filter, the topology could be expanded further to include a passive filter additionally, making it a hybrid model. In this way it could be possible to further increase the power factor of the TRASP, without increasing the IGBT current ratings to above 1200A, when using power applications ($\geq$ 1MW).
- The MMR simulations could be made more accurate if the topology is designed for the output power of 1MW instead of the 21kW model used for the proof of concept in this work. The performance is presumed to be much better in the case of the higher ratings. The THD

values and the robustness tests are expected to improve even further to already obtained superior results.

- As the MMR is an emerging topology and is seen to have enormous potential, more research can be conducted in terms of current sharing implementation and other aspects in order to improve its performance even further. Also, control complexity being one of the only drawbacks of this topology could be further researched into.

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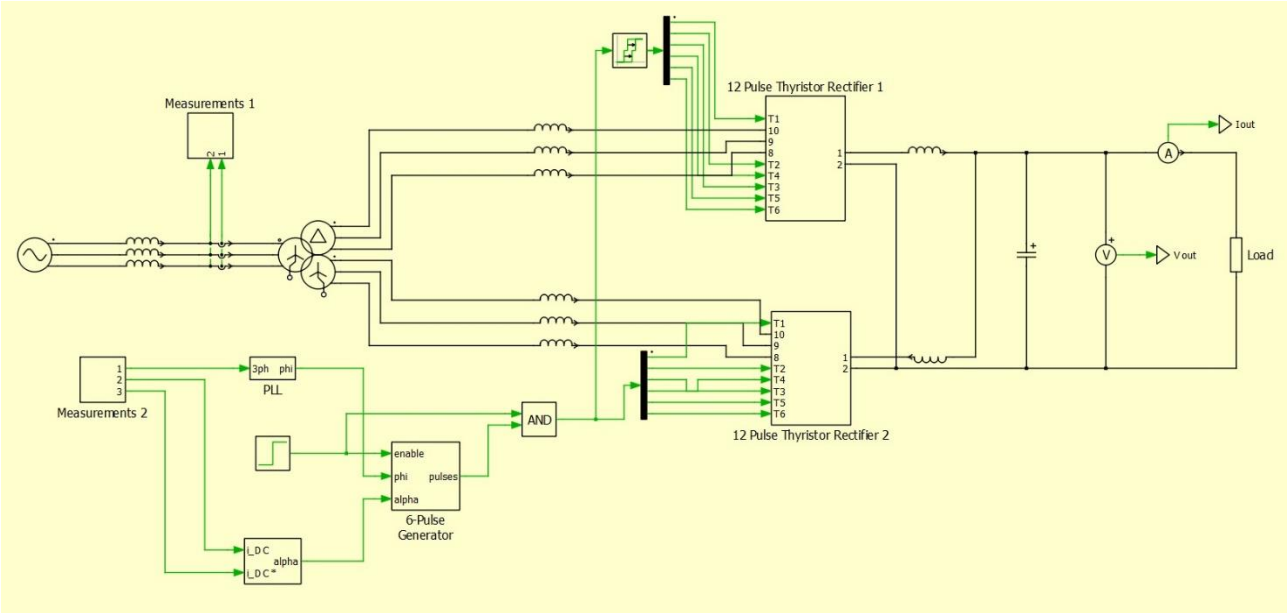
APPENDIX

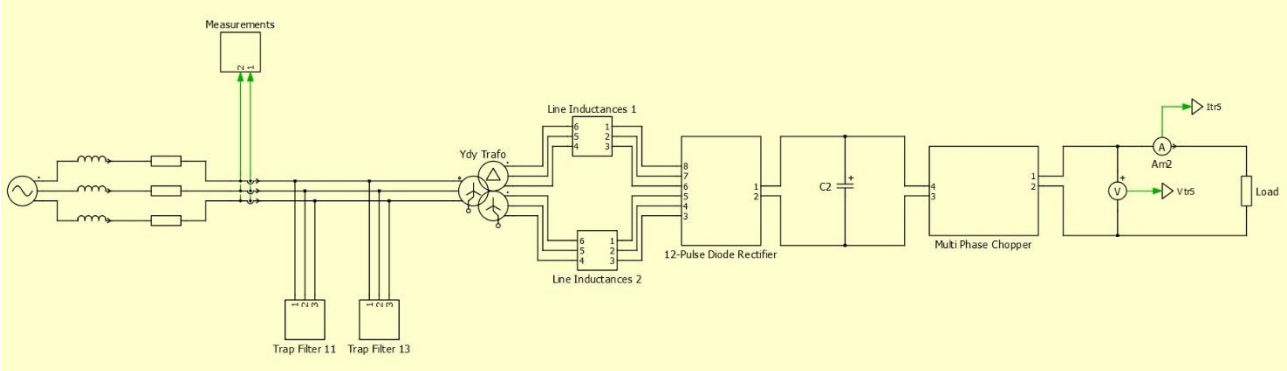
12-Pulse Thyristor Rectifier

Overview of the 12-Pulse Thyristor Rectifier model in PLECS

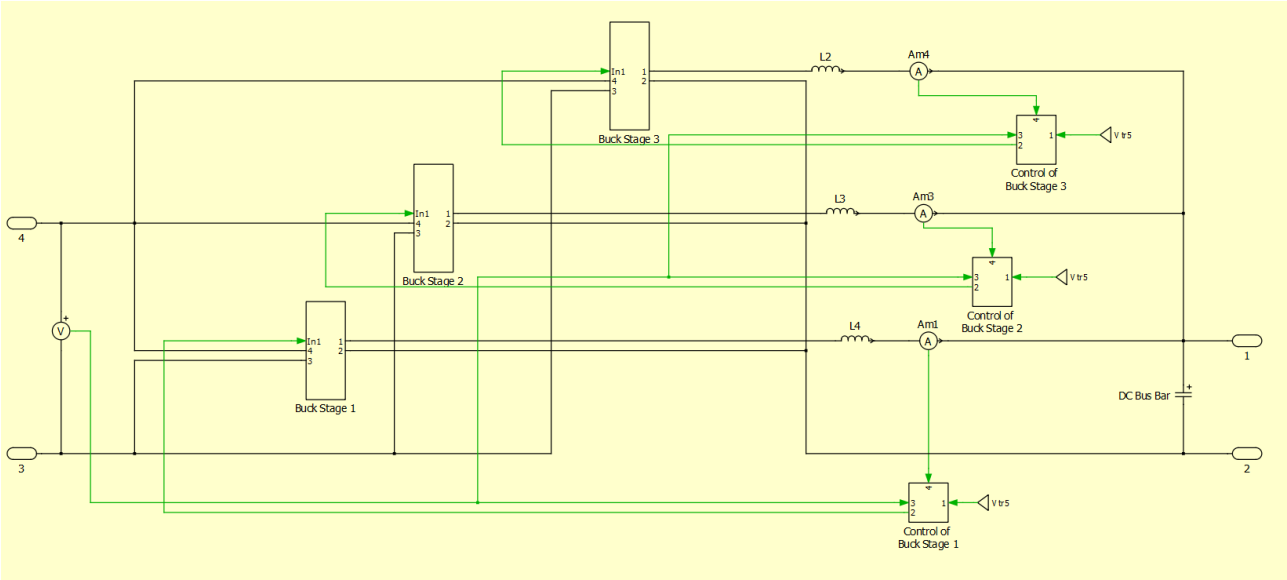


12-Pulse Diode Rectifier Multi-Phase Chopper

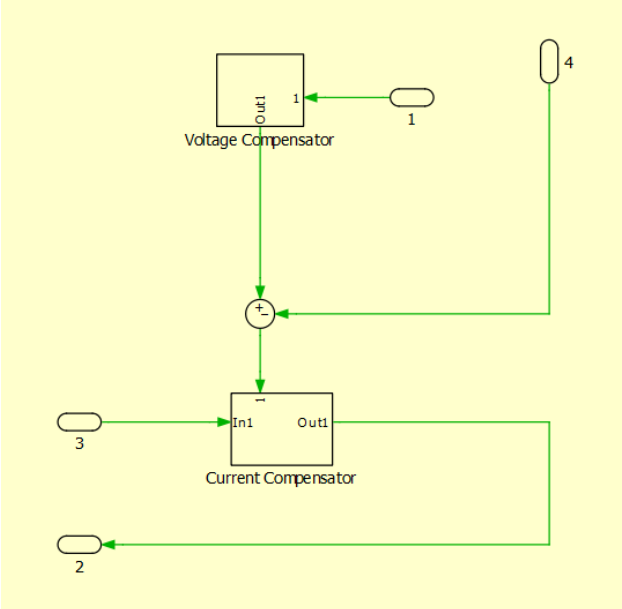
Overview of the 12-Pulse Diode Rectifier Multi-Phase Chopper model in PLECS



Multi-Phase Choppers in 12-Pulse Diode Rectifier Multi-Phase Chopper

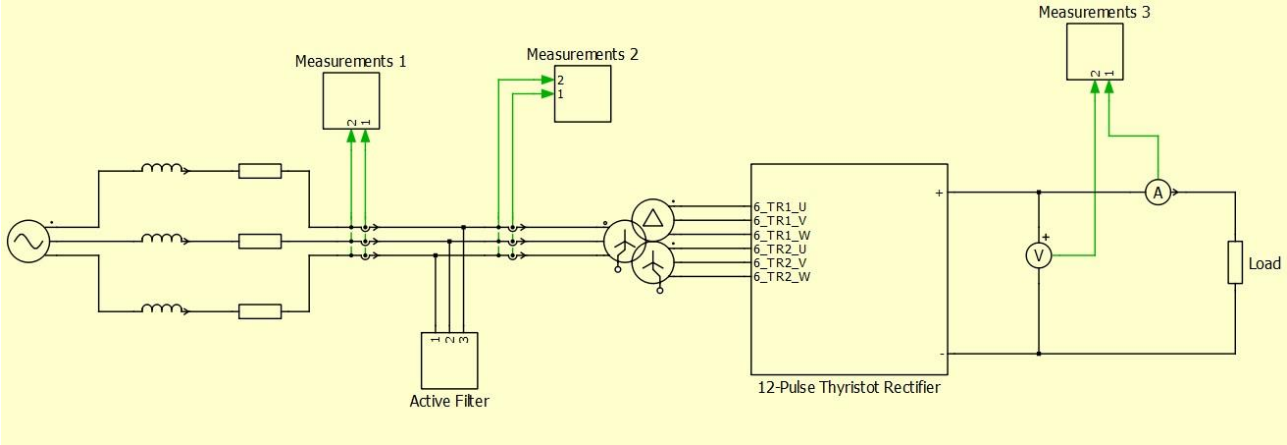


Multi-Phase Chopper Control in 12-Pulse Diode Rectifier Multi-Phase Chopper

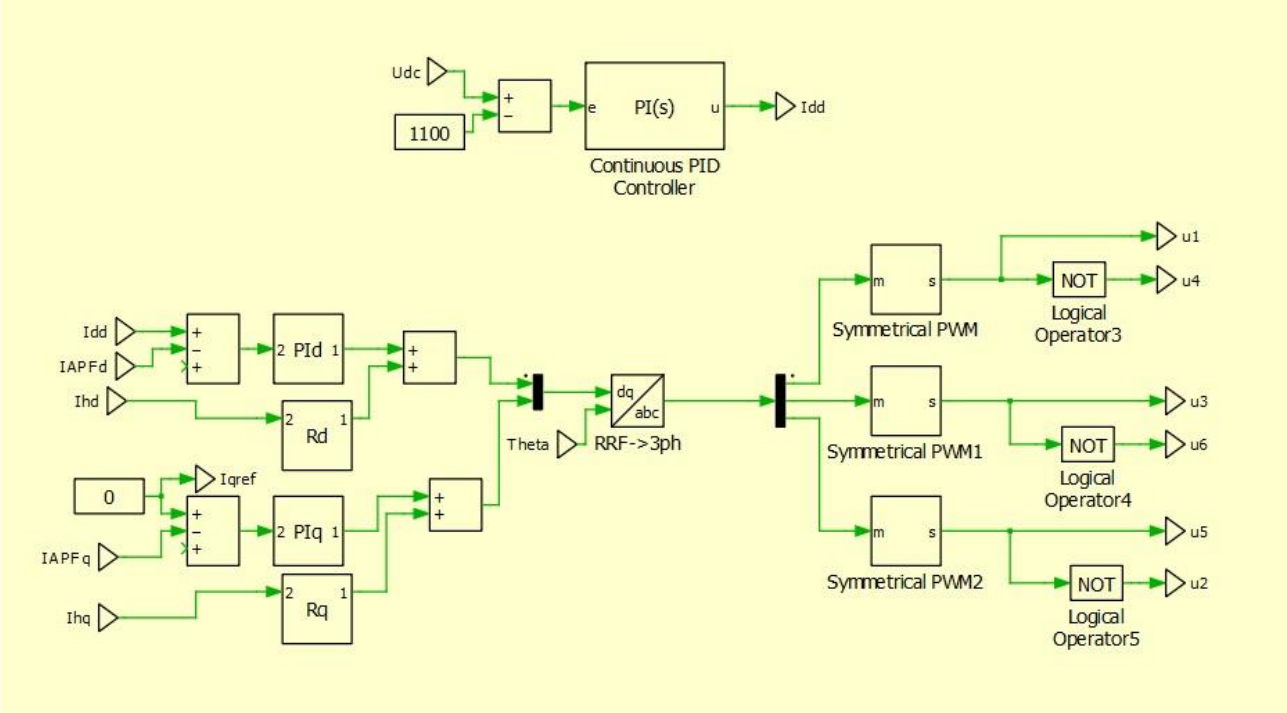


12-Pulse Thyristor Rectifier with Active Shunt Power Filter

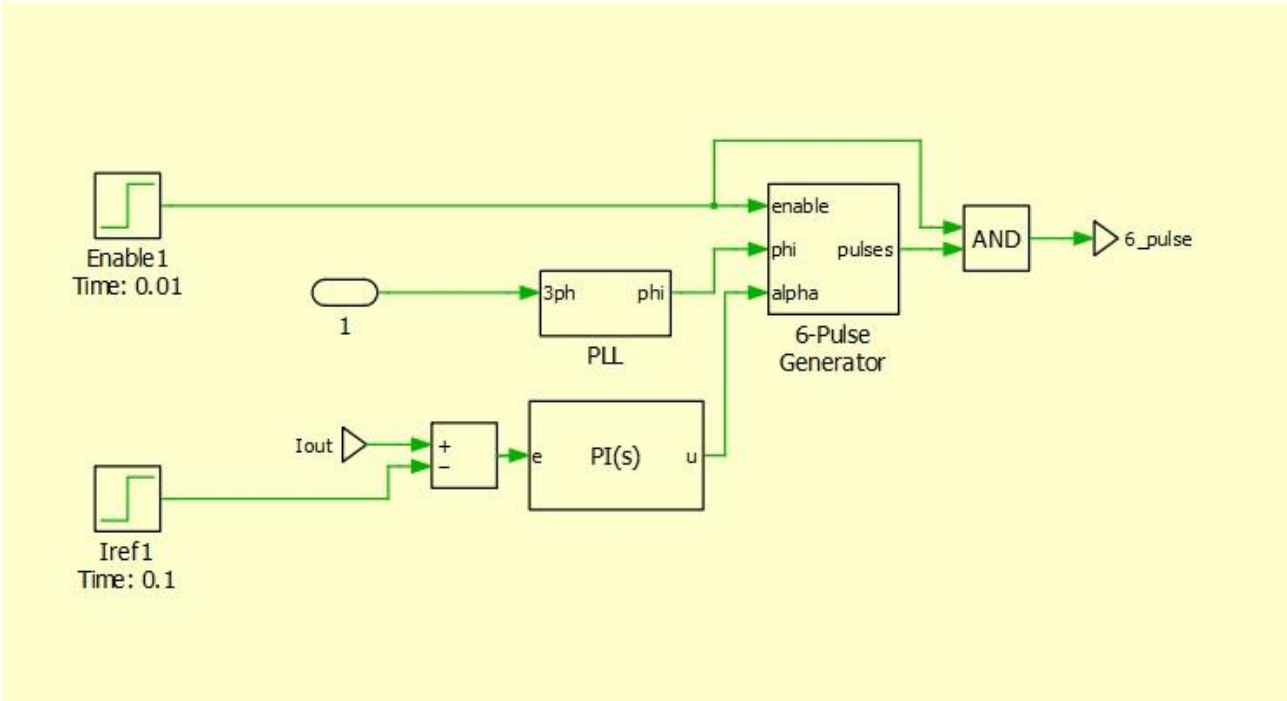
Overview of the 12-Pulse Thyristor Rectifier with Active Shunt Power Filter model in PLECS



Harmonic compensation control for 12-Pulse Thyristor Rectifier with Active Shunt Power Filter

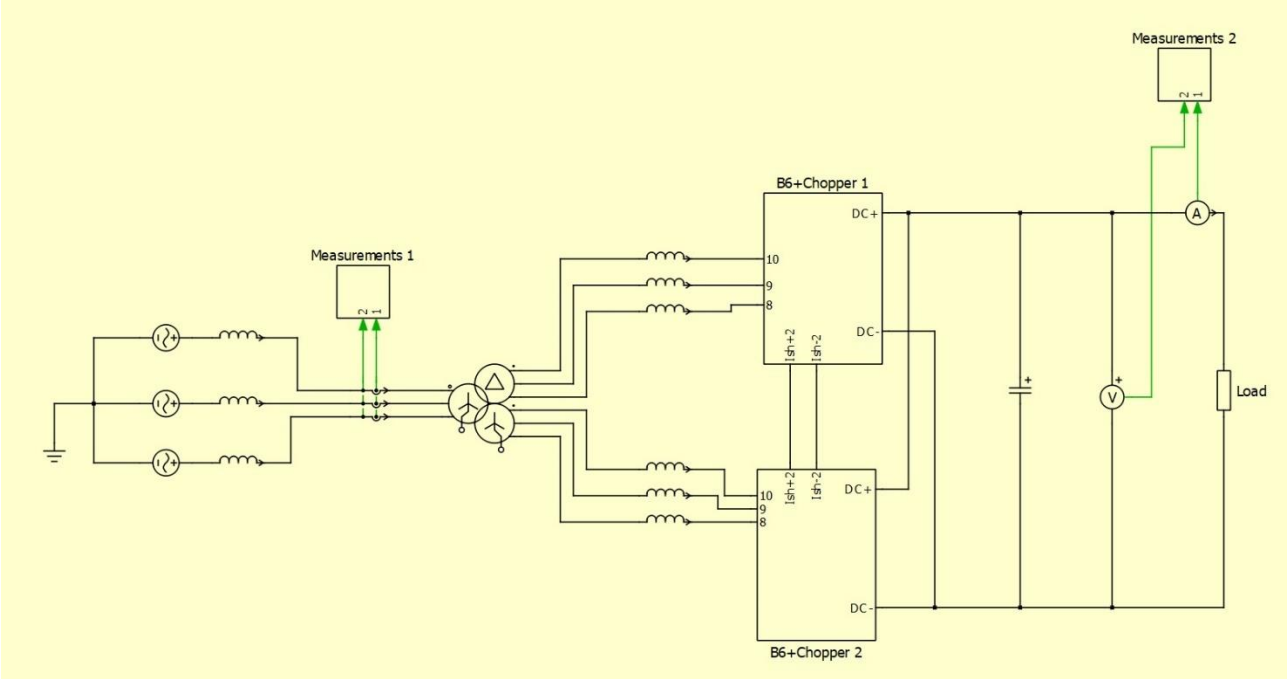


Thyristor Rectifier control for 12-Pulse Thyristor Rectifier with Active Shunt Power Filter

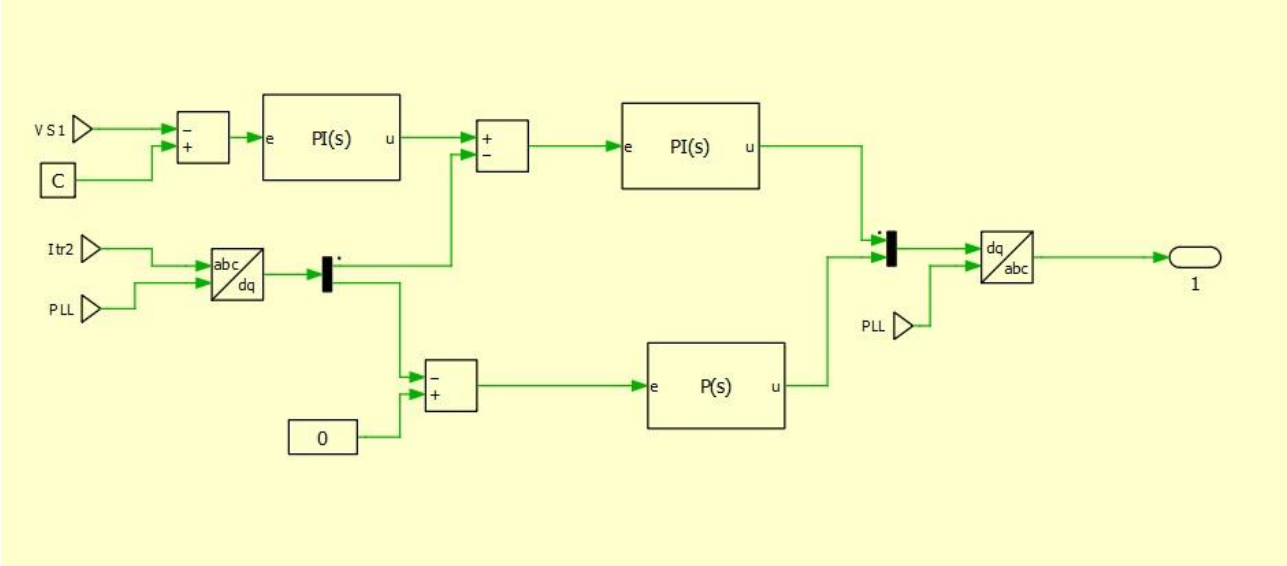


Active Front End – B6 + Chopper

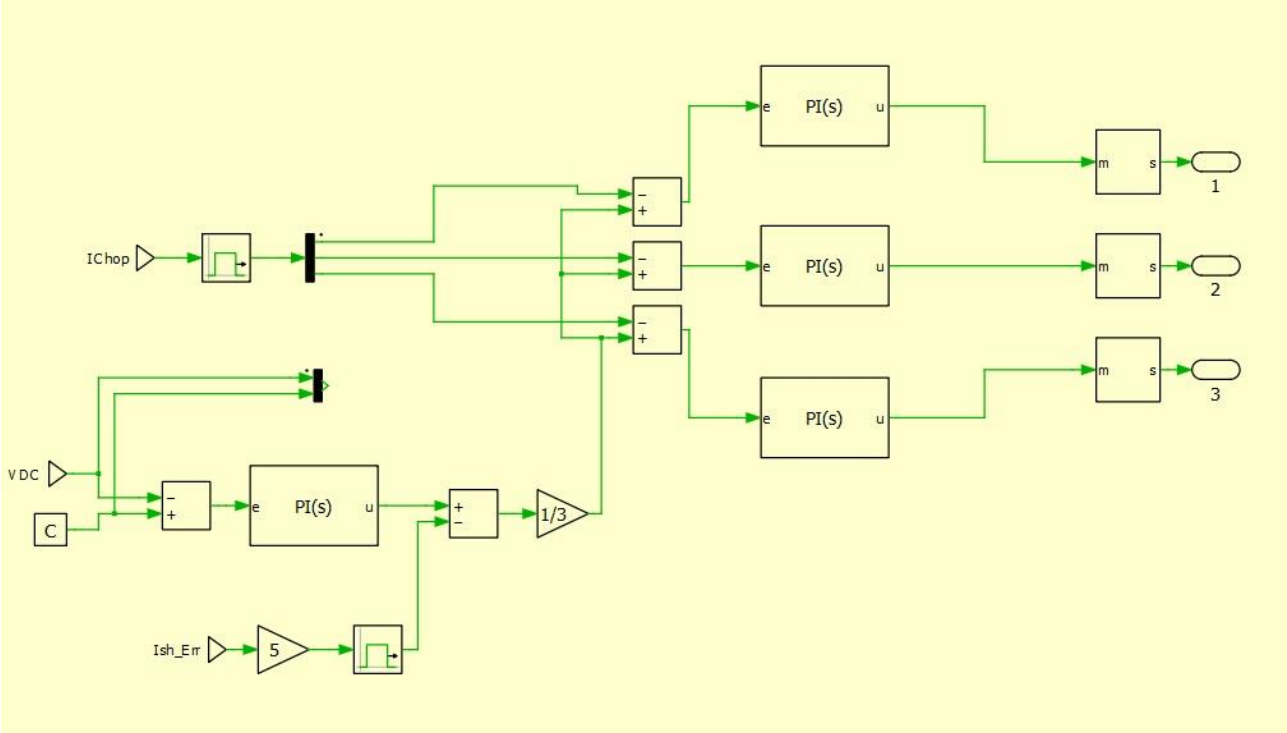
Overview of the Active front end – B6 + Chopper model in PLECS



Current controller of Active Front End – B6 + Chopper

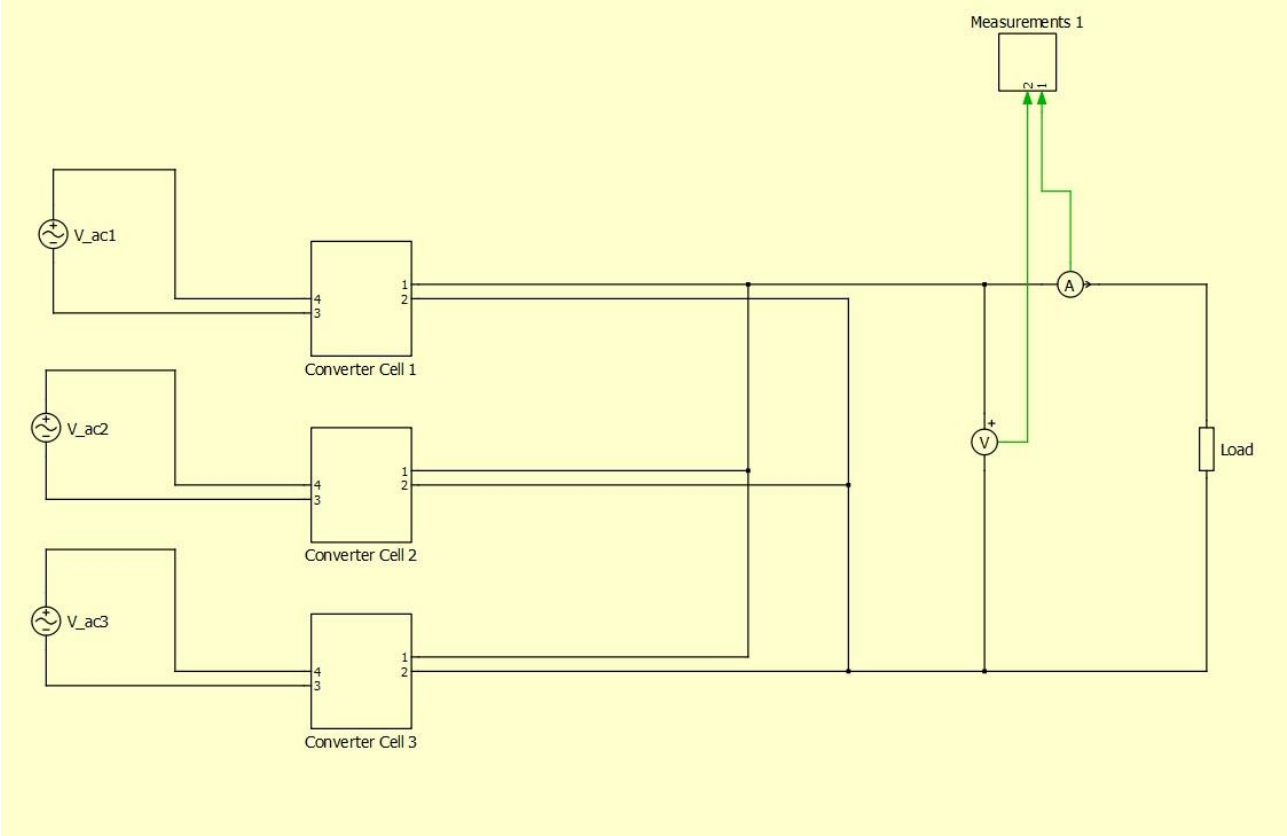


Chopper controller of Active Front End – B6 + Chopper

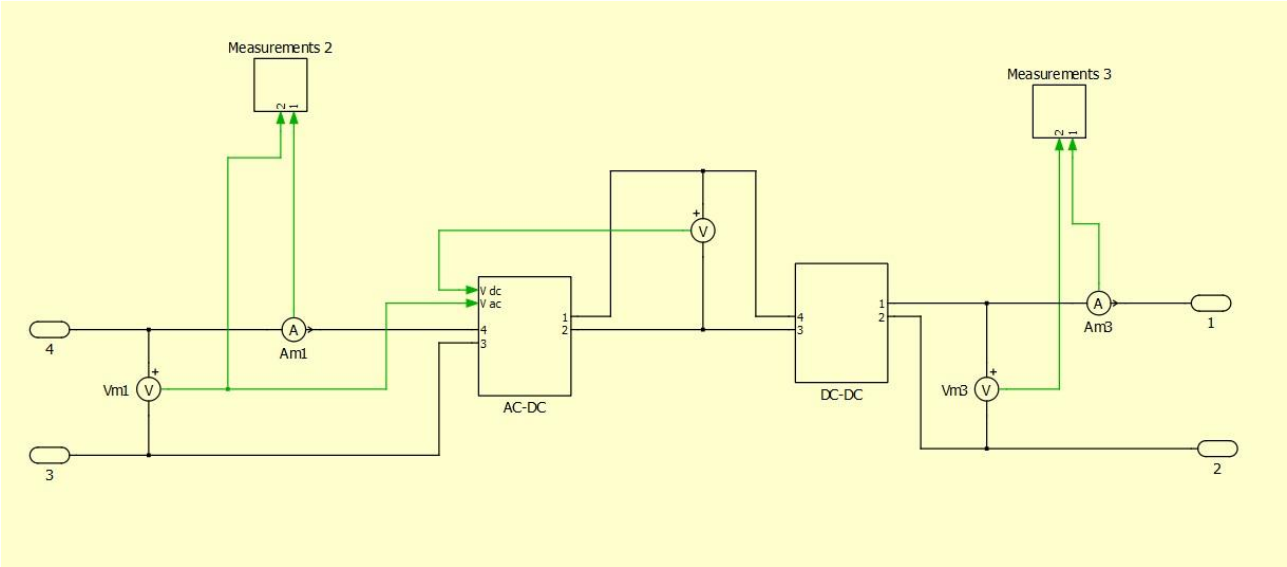


Modular Multicell Rectifier

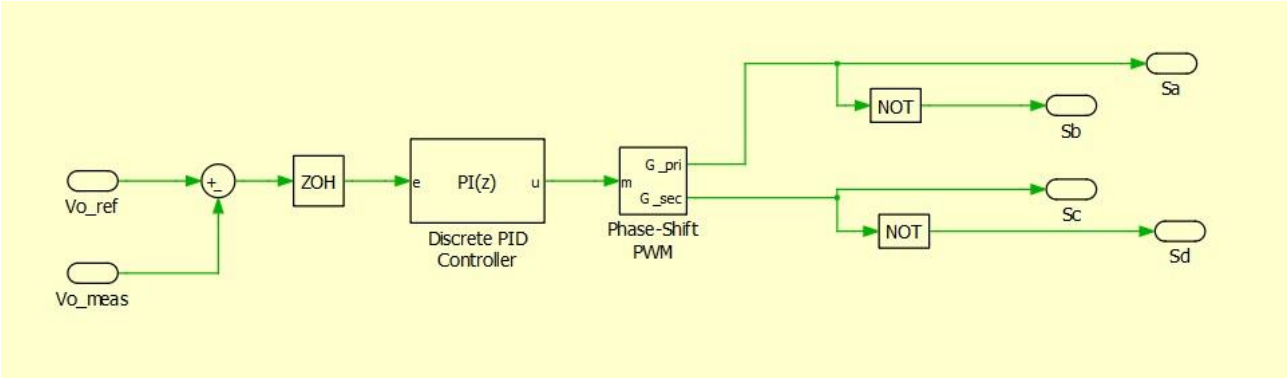
Overview of the Modular Multicell Rectifier Topology



Converter Cell of Modular Multicell Rectifier Topology



AC/DC Control for Modular Multicell Rectifier Topology



DC/DC Control for Modular Multicell Rectifier Topology