Distributed Power Electronics for Second-Life Batteries

MSc in Energy Engineering - Power Electronics and Drives

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Master's Thesis

STUDENT REPORT

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Abstract:
The use of battery storage systems (BESS) is widely considered for supporting the power grid. As the market for electric vehicles is growing rapidly, second-life batteries (SLBs) are becoming an attractive alternative for BESS. However, the use of SLBs has drawbacks due to the different state of health (SOH) and state of charge (SOC) of the batteries. In this work, different control methods for a cascaded H-bridge (CHB) topology for grid connection of second-life batteries are analyzed. By using a CHB topology, the possibilities of controlling the BESS are extended. Alternative switching techniques based on pulse width modulation (PWM) are shown and compared for multilevel inverters (MLI). Various battery energy management (BEMS) system strategies are proposed. Further, an active balancing technique is proposed to balance the state of energy (SOE) among the cells. The results show that the proposed strategies can be applied, extending and widening the battery control capabilities.

Acknowledgments

The work presented is a result of one year of work. The knowledge gained in the bachelor's and two years of learning in the Master of Science with specialization in Power Electronics and Drives at Aalborg University has been used in this project. The primary purpose of my whole studies is not anything other than helping the world become greener in terms of energy source, distribution and consumption. Therefore, I cannot be happier to have carried out this work in distributed power electronics for second-life batteries.

First, I would like to thank my supervisors, Ariya Sangwongwanich and Daniel-Ioan Stroe. Their many input has been crucial for finding good solutions in this year through all the problems we have been dealing with. Moreover, their advice and kind words have encouraged me to continue perfecting this work until the end.

Making this project has first taught me that each lecture I have been introduced to during my studies is worth it. Both the excitement and the boring ones have brought me here. But secondly, has taught me how little I know and that not knowing something cannot make me feel less valuable but encourage me to keep learning

Of course, lots of the lessons I have learned are not an only university related but life related. Moving to a new country for two years is not easy, but great colleagues have made it easy.

I would like to extend my gratitude to all the people who have helped me out, there are not enough pages to thank you all, to sum up: thank you all, friends and family.

Summary

Battery storage systems (BESS) are widely considered for supporting the power grid. However, different technologies exist to store energy, whereas this report is mainly focused on electrochemical batteries. In particular, as the market for electric vehicles (EVs) is growing, second-life batteries (SLBs) are becoming an attractive alternative for BESS.

Second-life battery is a term used to describe the batteries utilized in an EV. Still, due to degradation, it can no longer be used in the high-performance environment required by the EV. Nevertheless, these batteries still have around 70% of their original expected lifetime. However, the use of SLBs has drawbacks due to the batteries' different state of health (SOH) and state of charge (SOC).

This work analyses different control methods for a cascaded H-bridge (CHB) topology for grid connection of second-life batteries. Using a CHB topology, the possibilities of controlling the BESS are extended. Furthermore, alternative switching techniques based on pulse width modulation (PWM) are shown and compared for multilevel inverters (MLI).

Different battery energy management system (BEMS) strategies are proposed. Further, an active balancing technique is proposed to balance the state of energy (SOE) among the cells. The results show that the proposed strategies can be applied, extending and widening the battery control capabilities.

List of Abbreviations

Abbreviation:	Description:
AAU	Aalborg University
BESS	Battery Energy Storage System
BEMS	Battery Energy Management System
BOL	Beginning of Life
CHB	Cascaded H-Bridge
DG	Distributed Generation
EV	Electrical Vehicle
EEC	Equivalent Electrical Circuit
FFSOGI	Frequency-Fixed Second-Order Generalized Integrator
EIS	Electrochemical Impedance Spectroscopy
HPVBS	Hybrid PV Battery Systems
IR	Internal Resistance
OCV	Open-Circuit Voltage
PEC	Power Electronic Converters
PV	Photo-Voltaic
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
RES	Renewable Energy Sources
SLB	Second-Life Batteries
SOC	State of Charge
SOGI	Second-Order Generalized Integrator

Abbreviation:	Description:
SOH	State of Health
SRF	Synchronous Reference Frame
QSG	Quadrature Signal Generator
THD	Total Harmonic Distorsion
WTHD	Weighted Total Harmonic Distorsion

Nomenclature

Generic Variable Usage Conventions

Variable	**Aspect**	**Meaning**
F	CAPITALS	peak values
f	LOWER CASE	variable f instantaneous value
$\bar{f}$	OVERBAR	variable f mean value
$\hat{f}$	DAGGER	variable f estimated value
$\mathbf{f}$	BOLD LOWER CASE	vector
$\mathbf{F}$	BOLD UPPER CASE	matrix

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Chapter 1

Introduction

The world's energy demand is increasing year after year. The utilization of non-renewable sources of energy to accomplish this demand is under discussion. However, the reserves of these sources are decreasing continuously and contribute significantly to the global warming issue. Therefore, renewable energy sources (RES) are becoming more crucial to counteract the problem of future energy supply. Renewable energies market has been one of the most promising in the last years [1], [2]. As a result, the global market was valued at $ 881.7 Billion in 2020, and is expected to reach $ 1977 Billion in 2030 [3]. Wind power and photovoltaic (PV) systems are the most widespread RES. The implementation of these energy sources into the power grid is made through Distributed Generation (DG) plants. By 2050, it is expected that 47% of all renewable energy sources will be generated from solar energy, 34% from wind energy, 13 % from hydroelectric energy and 6% from the other sources [4]. Further, the Global Market Outlook for Solar Power anticipates that the expected amount of installed PV capacities to at least 123.5 MW in 2021 and 174.7 MW in 2025 [5]. Even though these sources of energy have many advantages in terms of environmental impact, they also present some challenges in term of system integration, e.g. variable energy supply due to the volatility of the environmental conditions [6].

Energy storage systems (ESS) aid the grid power distribution when renewable energy generation can not fulfil the required power load, but also maximizing profit when the production is greater than the load and energy can be saved in the ESS. Further, ESS can be utilized in the primary and secondary grid frequency regulation, active power flow and many other applications [7]. Some of the leading technologies used in electrical storage systems are divided into mechanical, e.g. pumped hydro; chemical, e.g. biofuel; electrochemical, e.g. batteries; and cryogenic, e.g. liquid air [8]. Battery energy storage system (BESS) is widely utilized as RES in DG systems [9]. Batteries can be made from a wide range of different technology, e.g. Lead Acid, Lithium-Ion and Nickel-Cadmium. One of the main applications of ESS is the EV market.

It is expected that the amount of EVs (excluding two and three wheels vehicles) will rise from 8 million in 2019 up to 50 million and 140 million in 2025 and 2050, respectively [10]. This rapid growth in EVs will require a large number of batteries. When a battery installed in an EV has reached specific degradation, it needs to be replaced, i.e. the end of its first-life. What to do with the replaced battery is still under discussion, as it can be recycled or, preferably, given a second use in the applications where the requirements are less demanding.

This second-life utilization could be, e.g. for residential applications or grid support [11]. Second-life batteries present some challenges, as the state-of-charge (SOC) and the state-of-health (SOH) varies from battery to battery. Therefore, diagnosing and sorting the batteries into similar ratings needs to be done at a first stage. In later stages, the control power electronic converters play a key role in the system's operation.

Power electronic converters (PEC) are widely used when integrating RES and BESS into the grid [12]. PEC allow flexibility and controllability in the interconnection of generation units and loads. Due to the increase in energy demand, higher power ratings have been developed and multilevel topologies have arisen. Different configurations can be utilized to connect such sources to the grid, e.g. centralized, string, multi-string, ac-module topologies [13], [14]. When utilizing a centralized topology, the overall performance is limited by the operation of the weakest link, i.e. the most degraded battery or PV panel; by utilizing a cascaded H-bridge (CHB) topology, i.e. a distributed topology, the system can be controlled at a more optimal operating point [15]–[17]. In this way, the control method can manage the power delivered from each battery and diagnose the SOC and SOH individually. The CHB topology requires the study and implementation of suitable control strategies and different modulation techniques.

1.1 Problem Statement

The problem statement summarising the essence of this work is formulated as:

Can second-life battery systems be used for residential applications using distributed power electronic system?

This statement includes the following:

- How to develop a method to diagnose the SOH of batteries using power converters.
- How can the balancing of battery systems be achieved using distributed power electronics.
- Benchmark the proposed control strategies to be implemented for second-life batteries with distributed power electronics.

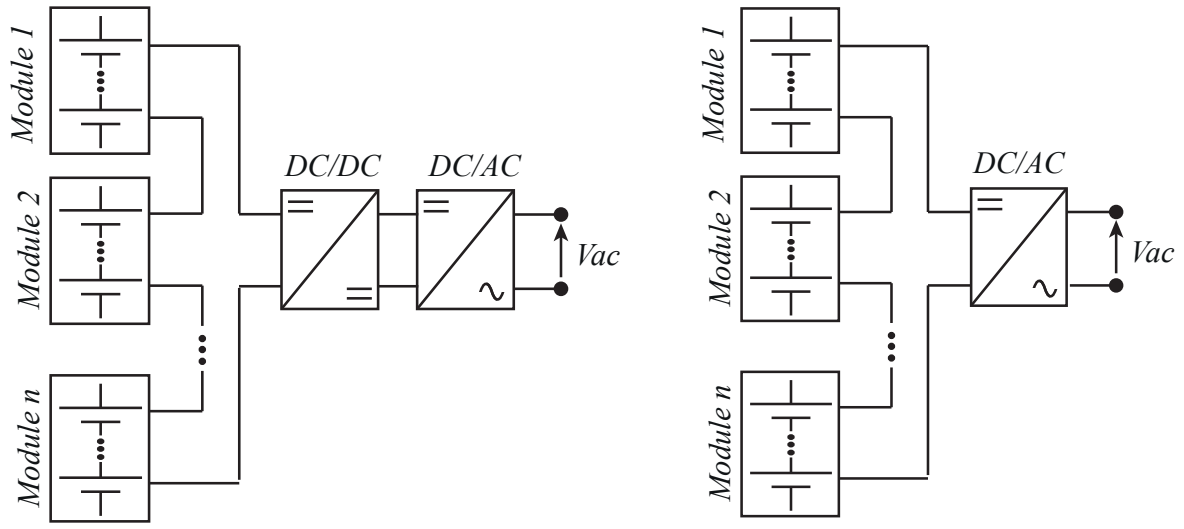
Chapter 2

State of Art

This chapter introduces the basic concepts leading to a better understanding of how a connection of a BESS to the grid utilizing a cascaded H-Bridge topology is made. To control the system, it is of great importance to understand the general working operation and different modulation techniques when utilizing the H-Bridge topology in multilevel inverters. At first, the need for utilizing the cascaded H-Bridge solution when connecting renewable energy sources to the grid is presented. Later, the working principle for the H-Bridge is explained, as well as its implementation in the cascaded H-Bridge topology utilizing different modulation techniques. Further, a comparison between the level-shifted and the phase-shifted pulse width modulation techniques is made. Finally, a description of the batteries' fundamentals and characteristics are presented.

2.1 Grid Connection of Battery Energy Storage Systems

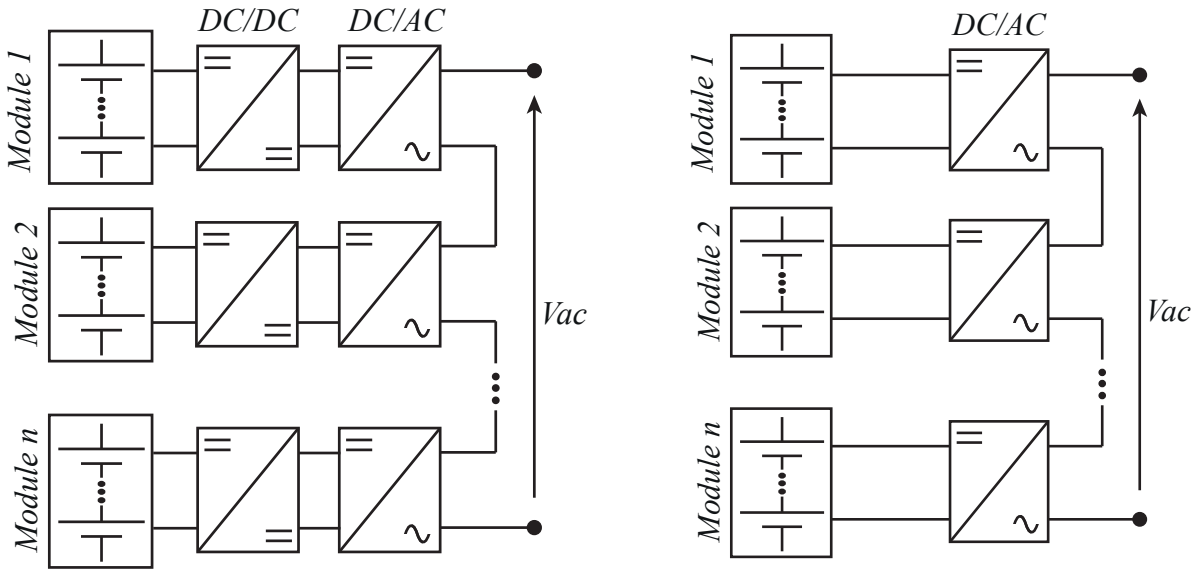
Grid connection of PV-Battery-Hybrid (PVBH) systems has been normally performed using different configurations [1], [14]–[16], [18], as shown in Fig. 2.1 and 2.2 for BESS sources in a centralized and decentralized configuration, respectively.



(a) Double stage.

(b) Single stage.

Figure 2.1: Centralized battery connection. Batteries are connected in series achieving high DC-link voltage.



(a) Double stage.

(b) Single stage.

Figure 2.2: Distributed battery connection. Batteries are connected in parallel to individual converters.

As can be observed in Fig. 2.1 and 2.2, there are two main topologies for power converter systems, a single-stage, i.e. no DC/DC converter is utilized; and a double-stage, i.e. a DC/DC converter is utilized. The use of a double-stage converter is utilized when the battery voltage needs to be stepped up, e.g. to minimize the DC-link voltage level requirement in the PV or battery side, to be able to inject current into the grid [19]. The use of a DC/DC converter ensures constant DC voltage. The main drawbacks of utilizing this DC/DC converter are the increase of complexity in the system and the decreased efficiency and costs[20]. Due to these reasons, the implementation of a DC/DC converter can be suppressed when the total DC-link nominal voltage is high enough. Further, the distributed topology shown in Fig. 2.2b has been proven to achieve higher efficiency than a centralized topology, as in Fig. 2.1b, which makes it attractive for the industry in second-life battery systems applications [21]. In the centralized inverter topology, batteries are connected in series, and the weakest battery module limits the overall system's performance [22], a drawback that is not present in decentralized topologies.

2.2 H-Bridge Topology

The full bridge or H-Bridge topology is widely used in electronic power systems. It was first presented by Mcmurray in 1965 [23]. The H-Bridge topology consists of four semiconductor devices with their respective antiparallel diodes, as it is shown in Fig. 2.3. The semiconductor devices illustrated in the figures are IGBTs.

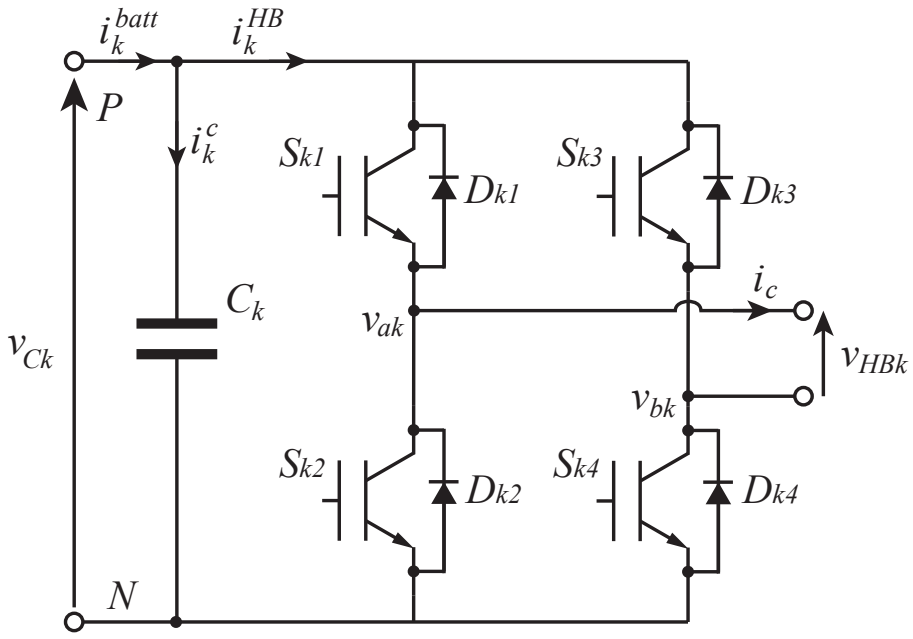


Figure 2.3: H-Bridge Inverter topology. IGBTs states are controlled to transform DC-link voltage into AC voltage at output terminals.

The DC input voltage is applied between P and N terminals. A capacitor on the DC side is used to filter the ripples and ensure constant DC voltage. By switching ON and OFF the semiconductors, it is possible to produce an AC voltage at the output terminals v_a and v_b. When this AC voltage is applied to a reactance, an AC current can be achieved. Then, the DC voltage and current are translated to an AC voltage and current. The power quality of the output signals may vary depending on the modulation technique used to switch ON and OFF the semiconductors.

2.3 Pulse Width Modulation Techniques

Carrier-based pulse width modulation (PWM) techniques are widely used in inverter control [24]–[26]. The principle of operation relies on the comparison of a sinusoidal waveform (modulation signal) with a triangular waveform (carrier signal). The modulation signal will have an amplitude, also known as modulation index, m_a, with a value of $m_a \in [-1, 1]$ in the linear range, and $m_a > 1$ in overmulation. This signal will have a frequency of f_1, i.e. the output voltage fundamental frequency. The carrier signal will have a frequency f_{cr}, and the relation between them is known as frequency modulation index m_f:

$$m_f = \frac{f_{cr}}{f_1} \tag{2.1}$$

The number of modulation and carrier signals will depend on the PWM technique used and the system topology. The output voltage can be obtained by utilizing bipolar or unipolar schemes for the H-Bridge topology.

When utilizing **bipolar** modulation, a single carrier is compared with a single modulation signal, as can be observed in Fig. 2.4

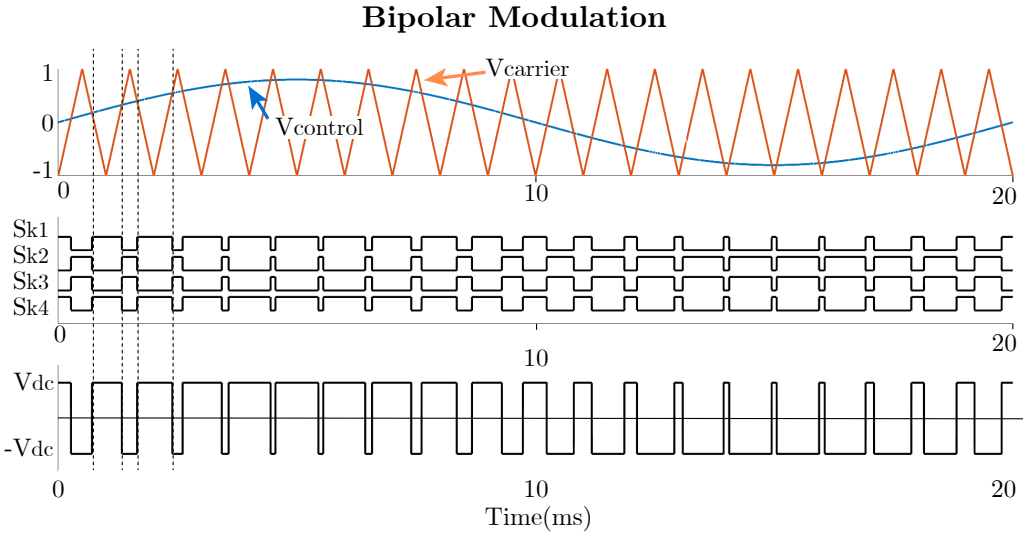


Figure 2.4: Bipolar Modulation Scheme PWM for a H-Bridge inverter. AC output voltage is varied between $\pm V_{dc}$. $m_a = 0.8$, $f_1 = 50$ Hz, $m_f = 10$.

As can be observed, only two output voltage levels can be obtained, $V_{HBk} = \pm V_{dc}$, supposing the DC voltage supply to be constant. The peak output voltage value is, in the linear range [24], assuming the capacitor voltage $V_{Ck} = V_{dc}$

$$\hat{V}_{HBk} = m_a \cdot V_{Ck} \tag{2.2}$$

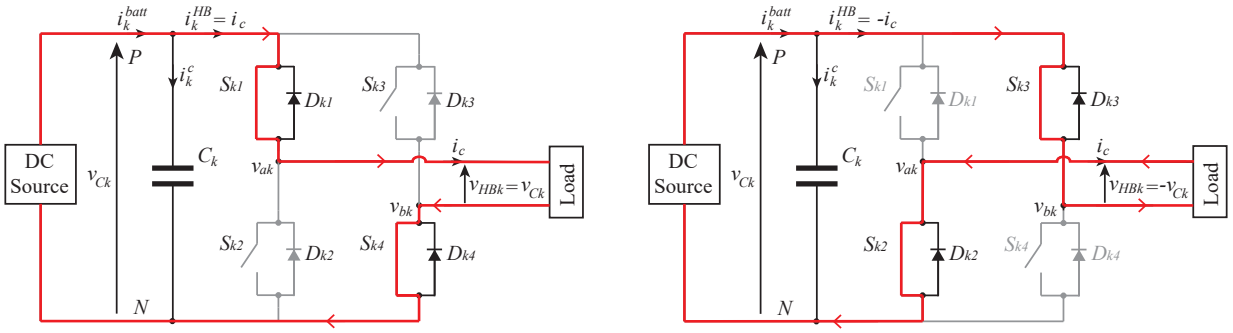
and in overmodulation,

$$V_{Ck} < \hat{V}_{HBk} < \frac{4}{\pi} V_{Ck} \tag{2.3}$$

Because $4V_{Ck}/\pi$ would be the output voltage in square wave modulation. When utilizing bipolar PWM, switches are turned ON and OFF diagonally in a way such as

$$\text{if } V_{control} > V_{carrier} \longrightarrow S_{k1}, S_{k4} \text{ ON and } S_{k2}, S_{k3} \text{ OFF}$$
$$\text{if } V_{control} < V_{carrier} \longrightarrow S_{k1}, S_{k4} \text{ OFF and } S_{k2}, S_{k3} \text{ ON}$$

The switching between ON and OFF is produced at the carrier frequency. Due to this switching pattern, the current paths in a H-Bridge converter may behave as shown in Fig. 2.5a for positive output currents and Fig. 2.5b for negative output currents.



(a) Positive current (b) Negative current

Figure 2.5: Switching states and current path depending on current direction. Considering unity power factor current is always flowing by S_{k1}-S_{k4} or S_{k2}-S_{k3}. Batteries are always either charging or discharging.

The voltage harmonics at V_{HBj} appear at

$$f_h^{bi} = h \cdot f_1 = j(m_f \pm b) f_1 \tag{2.4}$$

That is, the harmonic h will appear as the sideband b^{th} of j times the output fundamental frequency.

When utilizing **unipolar** modulation, more than one modulation signal or carrier signal is needed. Here, a single modulation signal and the two of carrier signals are used. Figure 2.6 shows a three-level unipolar modulation scheme.

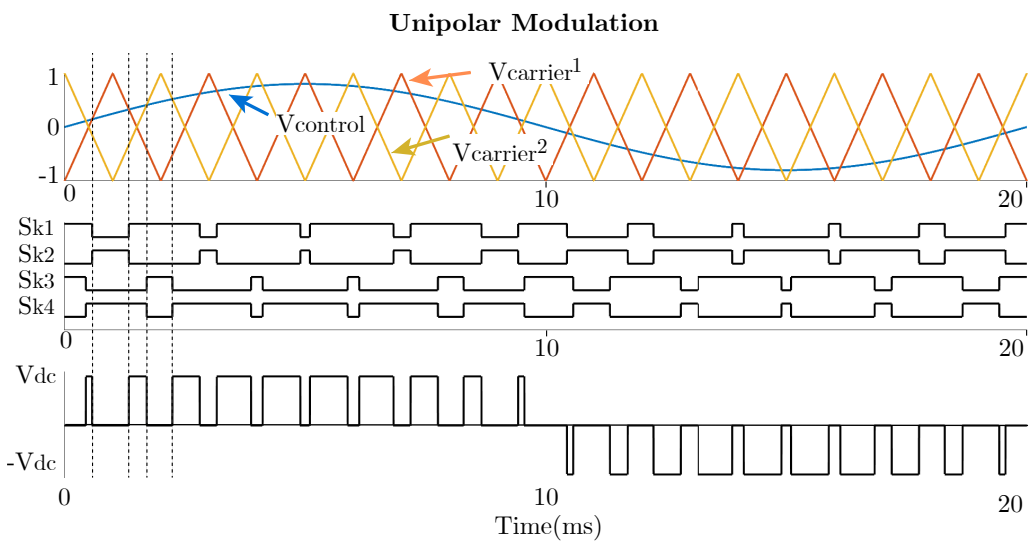


Figure 2.6: Unipolar Modulation Scheme PWM for an H-Bridge Inverter. AC output voltage can have three different states, i.e. $\pm V_{dc}$ or 0. $m_a = 0.8$, $f_1 = 50$ Hz, $m_f = 10$.

The switching pattern extracted from Fig. 2.6 is described as

$$\begin{aligned}
&\text{if } V_{control} > V^1_{carrier} \longrightarrow S_{k1} \text{ ON and } S_{k2} \text{ OFF} \\
&\text{if } V_{control} < V^1_{carrier} \longrightarrow S_{k1} \text{ OFF and } S_{k2} \text{ ON} \\
&\text{if } V_{control} > V^2_{carrier} \longrightarrow S_{k3} \text{ ON and } S_{k4} \text{ OFF} \\
&\text{if } V_{control} < V^2_{carrier} \longrightarrow S_{k4} \text{ OFF and } S_{k4} \text{ ON}
\end{aligned}$$

The H-Bridge inverter shown in Fig. 2.3 can output a maximum of three voltage levels in unipolar modulation, depending on the commutation of the power devices, as shown in Table 2.1.

Table 2.1: Commutation states, voltage levels and conducting devices in unipolar modulation

State	S_{k1}	S_{k2}	S_{k3}	S_{k4}	v_{ck}	**Conducting device**
I	1	0	0	1	V_k^{dc}	S_{k1} and S_{k4} if $i_c > 0$ D_{k1} and D_{k4} if $i_c < 0$
II	1	0	1	0	0	S_{k1} and D_{k3} if $i_c > 0$ D_{k1} and D_{k3} if $i_c < 0$
III	0	1	1	0	$-V_k^{dc}$	D_{k2} and D_{k3} if $i_c > 0$ S_{k2} and S_{k3} if $i_c < 0$
IV	0	1	0	1	0	D_{k2} and S_{k4} if $i_c > 0$ S_{k2} and D_{k4} if $i_c < 0$
V	0	0	0	0	$-V_k^{dc}$ V_k^{dc}	D_{k2} and D_{k3} if $i_c > 0$ D_{k1} and D_{k4} if $i_c < 0$

These states and commutation states yield to the current paths shown in Fig. 2.7a and 2.7b for positive and negative output AC current cycle with unity factor.

Assuming a pure sinewave in the output voltage V_{HBk} as:

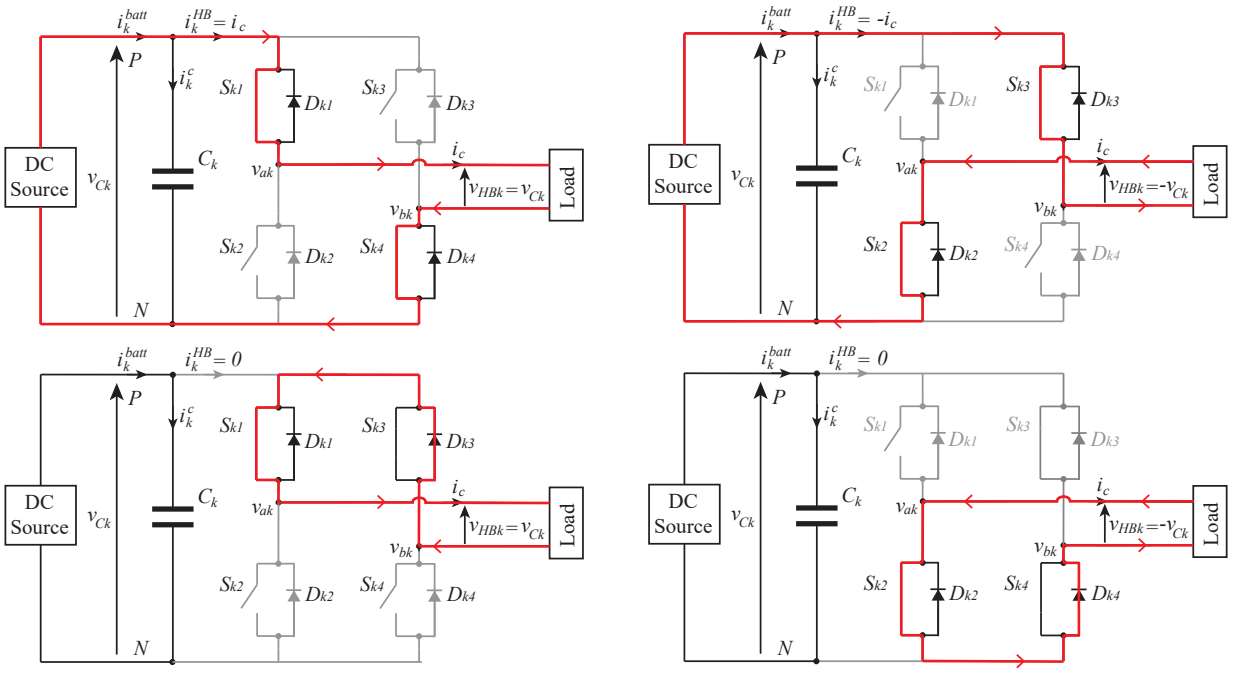
$$v^{h=1}_{HBk} = \sqrt{2} V_{HBk} \sin(\omega_1 t) \tag{2.5}$$

Then, assuming that a well designed filter is applied at the output, the current in the AC side will be have an RMS value of I_s and lagging the voltage with ϕ degrees:

$$i_s = \sqrt{2} I_s \sin(\omega_1 t - \phi) \tag{2.6}$$

Further assuming that the LC filters do not store or dissipate energy, the instantaneous input and output power is equal, with constant DC-source input voltage hence [24]:

$$V_{Ck} \cdot I_k^{HB}(t) = v_{HBk} \cdot i_s = \sqrt{2} V_{HBk} \sin(\omega_1 t) \sqrt{2} I_s \sin(\omega_1 t - \phi) \tag{2.7}$$



(a) Positive current.

(b) Negative current.

Figure 2.7: Switching states and current path depending on current direction. Current can go through free-wheeling diodes when output voltage is 0 and DC Source is remained in idle state not delivering or receiving current.

And therefore:

$$I_1^{HB} = \frac{V_{HBk} I_s}{V_{ck}} \cos(\phi) - \frac{V_{HBk} I_s}{V_{ck}} \cos(2\omega_1 t - \phi) = I_d - I_{ac} \cos(2\omega_1 t - \phi) \tag{2.8}$$

where:

$$I_d = \frac{V_{HBk} I_c}{V_{ck}} \cos(\phi) \tag{2.9}$$

and

$$I_{ac} = \frac{V_{HBk} I_c}{\sqrt{2} V_{ck}} \tag{2.10}$$

It can be seen in (2.8) that the current in the DC-side is a compound of two terms. One is responsible for transferring the power from the DC- to the AC-side, which is I_d DC-link current magnitude. The other one is a sinusoidal current ripple of double the fundamental frequency.

Further, the peak output voltage value is the same as for bipolar modulation, described in (2.2). On the other hand, the harmonics appear at

$$f_h^{uni} = h \cdot f_1 = (j2m_f \pm b) f_1 \tag{2.11}$$

Therefore, as can be observed in (2.4) and (2.11), the harmonics when using unipolar modulation are moved to higher frequencies. In such a way, the output voltage quality is increased significantly, yielding to smaller filters at the output.

Due to the increase in power ratings and growth in energy demand, different solutions arise to accomplish the requirements. The solution chosen to be used in this project is the well known multilevel inverter, the cascaded H-Bridge.

2.4 Cascaded H-Bridge Converters

When multiple H-Bridge inverters are connected in series, a Cascaded H-Bridge (CHB) inverter is formed. The individual H-Bridge along the CHB are also called *power cells*, *bridge cells* or simply *cells*. Figure 2.8 shows a k-order CHB converter, which was first presented in 1975 by Baker and Bannister [27]. This type of converter is part of a wide range of multilevel inverters (MLI). The CHB topology is mainly used in high-power and medium-voltage applications [26]. The input constant voltage source represents any source, i.e. PV or batteries.

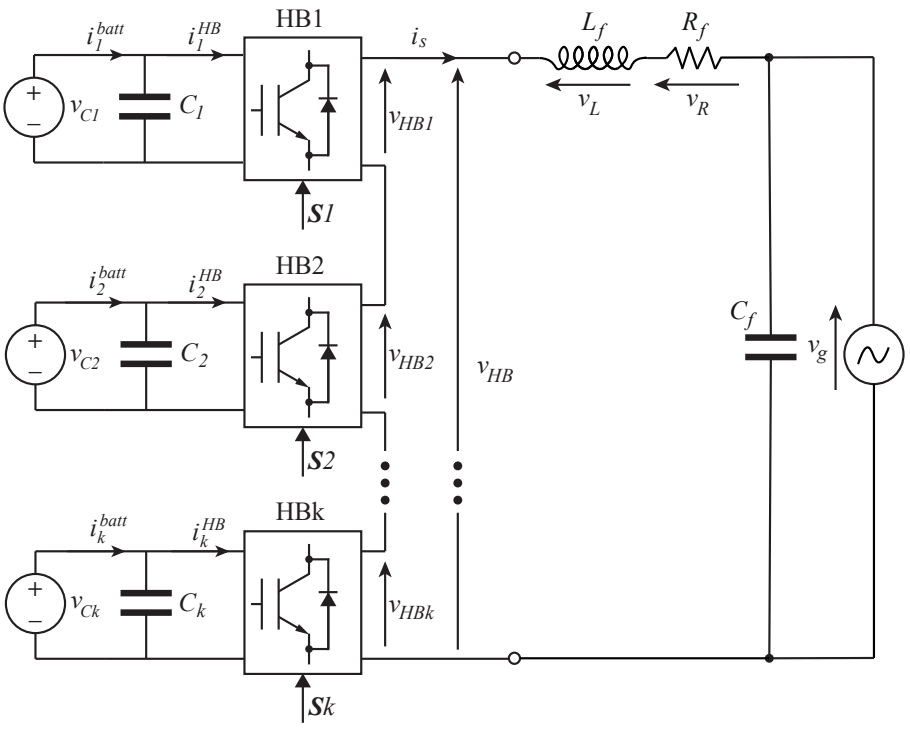


Figure 2.8: Cascaded H-Bridge inverter topology. Multiple H-Bridge inverters output terminals are connected in series, producing a multilevel AC output voltage.

Given that each bridge cell can output three different voltage levels, then $v_{HBk} \in [-V_{Ck}, V_{Ck}]$, which can be controlled within that range by introducing a continuous variable $M_k \in [-1, 1]$ therefore, the dynamical model of the system can be expressed as [16], [28], [29] in (2.12) and (2.13)

$$\dot{i}_s = \frac{1}{L_f}\left(\sum_{k=1}^{k}(M_k v_{Ck}) - R_f \cdot i_s - v_g\right) \tag{2.12}$$

$$\dot{v}_{Ck} = \frac{1}{C_k}(i_k^{HB} - M_k \cdot i_s) \text{ with } k = 1, ..., n \tag{2.13}$$

As can be observed in (2.12), to control the current injected into the grid, which voltage is v_g, the output voltage v_{HB} needs to be controlled, as the total output voltage [30] is

$$v_{HB} = \sum_{j=1}^{k} v_{HBj} = \sum_{j=1}^{k}(M_j v_{Cj}) \tag{2.14}$$

Further, the total amount of voltage levels, m, at v_{HB} are

$$m = 2H + 1 \tag{2.15}$$

being H the number of bridge cells.

For instance, a seven-level CHB comprising three cells, will output the voltage shown in Fig. 2.9. This is because each cell output terminals supplies each voltage level.

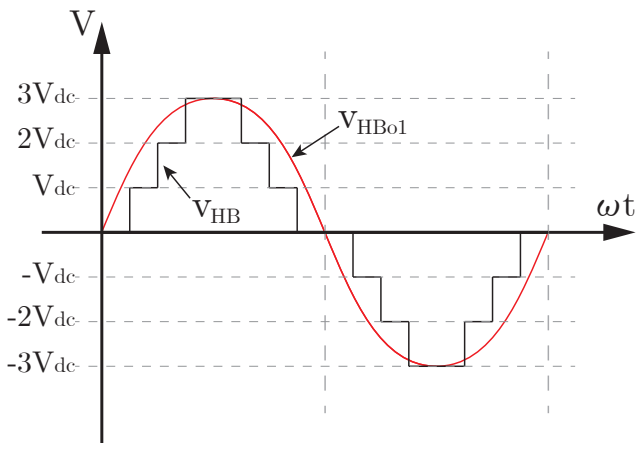


Figure 2.9: Output voltage waveform of a seven-level CHB inverter schematic omitting semiconductor switching. Multiple levels can be achieved by adding the input DC-link voltage of the H-Bridges.

The CHB's output current, i_s, is the same for all HB cells. Because these current must be controlled, the CHB's output voltage must also be controlled. As previously stated, the CHB output voltage is the sum of each cell's output voltage. The output voltage v_{HBj} of each bridge cell must be adjusted to control the power delivered by each cell [31]. In such a way, the CHB topology can be utilized as a distributed power electronic converter.

2.5 PWM for Multilevel Inverters

The basic concepts explained in Section 2.3 can also be applied to multilevel inverters by applying appropriate modifications. Due to the better performance of the unipolar against the bipolar modulation, only unipolar will be considered.

2.5.1 Phase-Shifted PWM

In a phase-shift PWM (PS-PWM) technique, there exist H modulation signals and $m-1$ carrier signals, being H the number of cells and m the number of levels. Here, the modulation signals are in phase and have the same modulation index, i.e. only one modulation signal, called "control" signal is shown. These carrier signals are displaced to each other with an angle of [26]:

$$\phi = \frac{360°}{m-1} \tag{2.16}$$

For example, in a three-cell bridge CHB, i.e. a seven-level CHB inverter ($m = 2 \cdot 3 + 1 = 7$), the number of carriers is $m - 1 = 6$, and are displaced to each other by $360°/6 = 60°$, as in Fig. 2.10.

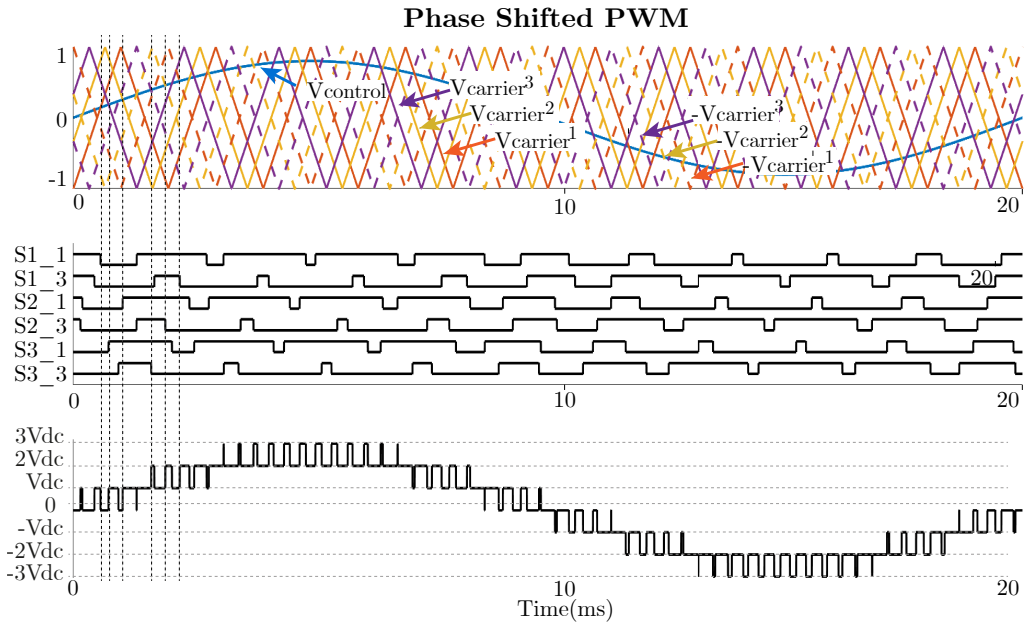


Figure 2.10: Phase Shifted PWM in a seven-level CHB inverter. Modulation signals are in phase. Carriers are shifted in angle. Duty cycles are equal among cells through a fundamental period. $m_a = 0.8$, $m_f = 10$.

As the output voltage of a CHB is the sum of the individual power cells' output voltage, the effective switching frequency utilizing PS-PWM is:

$$f_{sw}^{PS-PWM} = 2H \cdot f_{cr} \tag{2.17}$$

which is the frequency seen from the output CHB terminals.

2.5.2 Level-Shifted PWM

Similarly to the PS-PWM, H modulation signals and $m-1$ carrier signals are utilized. In this case, normalizing the modulation and carrier signals, each carrier is level shifted with an offset, as can be seen in Fig. 2.11.

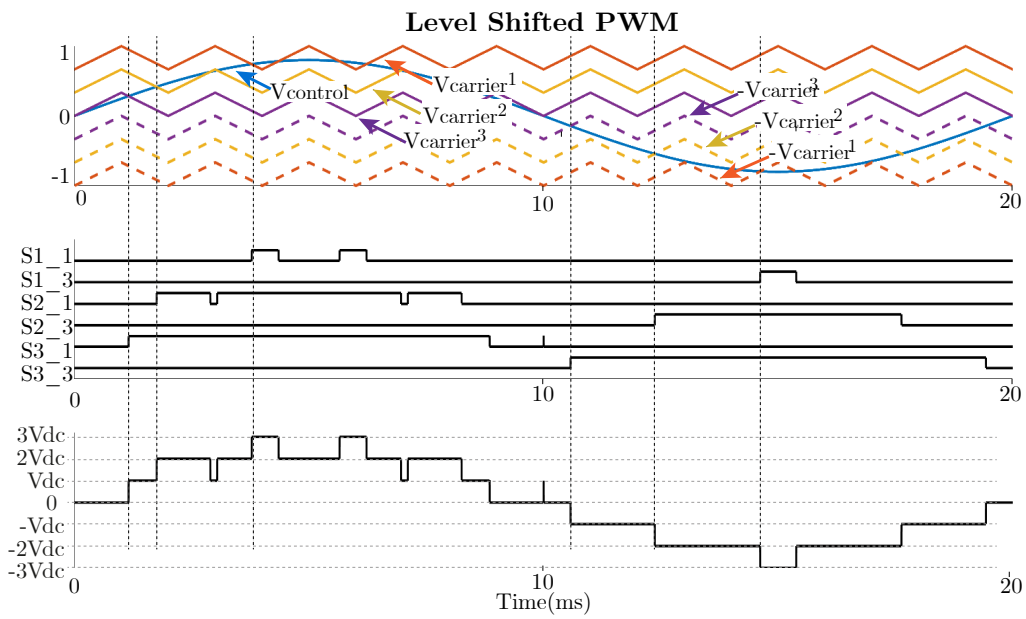


Figure 2.11: Level Shifted PWM in a seven-level CHB inverter. Modulation signals are in phase. Carriers are shifted in amplitude and constant in all operation time. Duty cycles are very different among cells through a fundamental period. $m_a = 0.8$, $m_f = 10$.

The effective switching frequency utilizing PS-PWM is described as

$$f_{sw}^{LS-PWM} = f_{cr} \tag{2.18}$$

There exist three schemes for LS-PWM [32], the in-phase disposition (IPD), the alternated phase opposite disposition (APOD) and the phase opposite disposition (POD), all illustrated in Fig. 2.12. It is proven in [33] that the three LS-PWM schemes perform very similar to each other, therefore only the IPD is considered in this work.

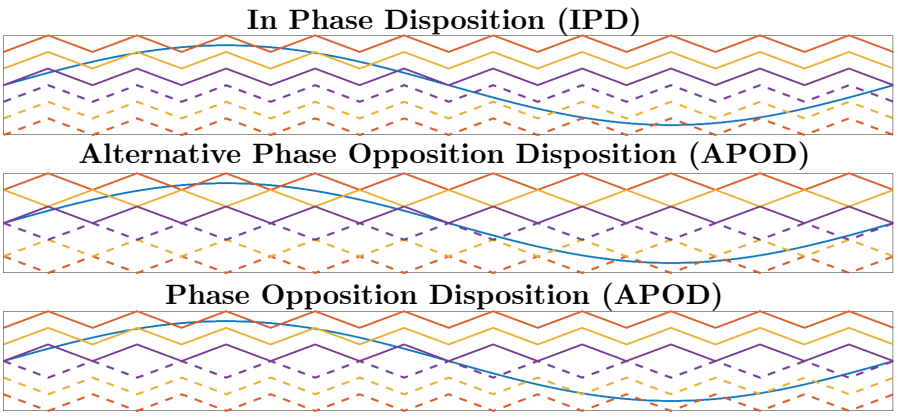


Figure 2.12: Level Shifted PWM in a seven-level CHB inverter. Carriers are shifted in amplitude in different ways.

As can be observed in Fig. 2.11, the amount of time each H-Bridge is conducting is unequally distributed when utilizing LS-PWM. In such figure, it can be seen that $S3\_1$ is conducting the most while $S1\_1$ is conducting the least. One solution to equalize losses among the cells is presented by Angulo et al. [30] propose a rotative LS-PWM in which the levels of the carriers change their offset periodically, as illustrated in Fig. 2.13. In this figure, the permutation is performed every switching period, whereas it can be applied at other integer multiples of the switching period [31] This technique is presented under the name LS-PWM with permutation or LSP-PWM. The LS-PWM with no permutation will be named LSNP-PWM from now on.

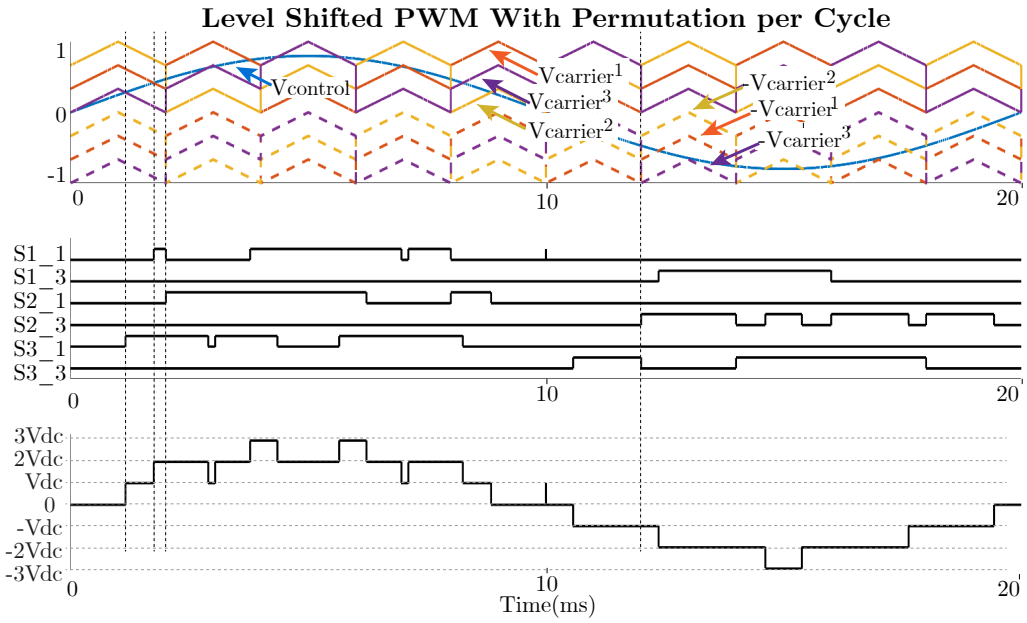


Figure 2.13: Level Shifted PWM with permutation per cycle in a seven-level CHB inverter. Modulation signals are in phase. Carriers are shifted in amplitude and permuted every determined cycles, in this example, every cycle. Duty cycles are equal among cells through a fundamental period. $m_a = 0.8$, $m_f = 10$.

2.5.3 Harmonic Distortion

To quantify the quality of the currents and voltages, the Total Harmonic Distortion (THD) calculation is used. Considering the voltage THD, it can be defined as

$$THD = \sqrt{\left(\frac{V_{rms}}{V_{1,rms}}\right)^2 - 1} \tag{2.19}$$

In which an $V_{1,rms}$ is the fundamental harmonic voltage in rms value, being the Root Mean Square (RMS) quantity calculated as

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T v(t)^2 dt} \tag{2.20}$$

and T the period of the waveform. Expression (2.19) can also be expressed as peak values in the form

$$THD = \frac{\sqrt{\sum_{n\geq 2}^{\infty} V_n^2}}{V_1} \tag{2.21}$$

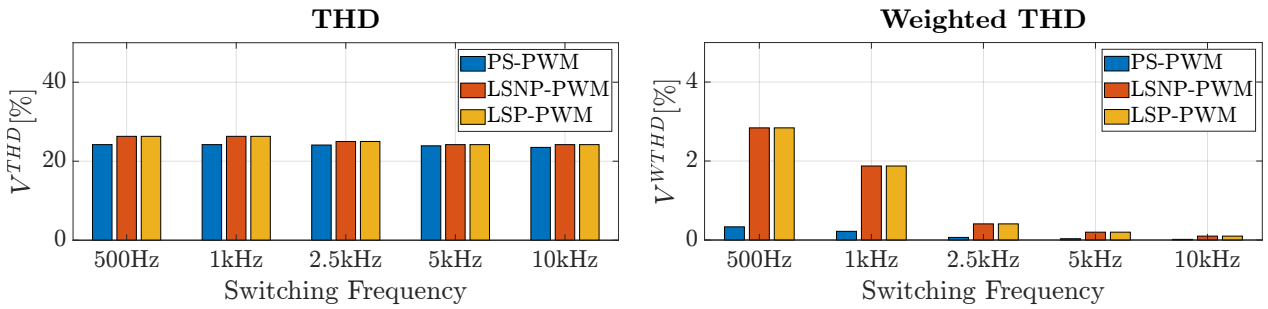
It must be noticed that the THD characterization does not take the place of the harmonics into account, as it calculates the sum of all the harmonics, regardless of the frequency. To take into account how far the harmonics are from the fundamental frequency, the Weighted Total Harmonic Distortion (WTHD) is used.

$$WTHD = \frac{\sqrt{\sum_{n=2}^{\infty}\left(\frac{V_n}{n}\right)^2}}{V_1} \tag{2.22}$$

By inspecting (2.22), it can be observed that the total WTHD value is smaller when the harmonics are moved towards higher frequencies.

The following comparison is given below between PS-PWM, LSNP-PWM (level-shift with no permutation PWM), and LSP-PWM (level-shift with permutation) for different switching frequencies and voltage levels, using the concepts presented in the harmonic distortion.

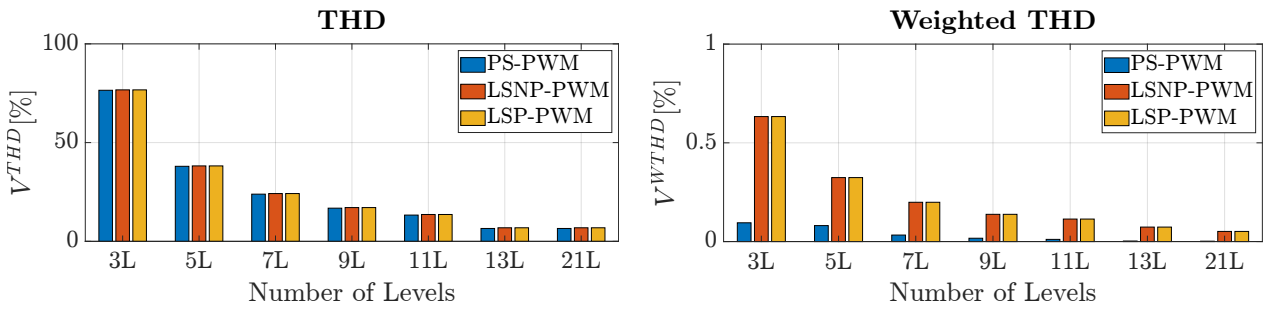
Figure 2.14 shows the simulation results for a 7L CHB with different switching frequencies and a constant modulation index of $m_a = 0.8$. Both THD and WTHD have been calculated utilizing (2.21) and (2.22). It can be observed in Fig. 2.14a that the THD is very similar for all the switching frequencies, as the place of the harmonics is not taken into account. The THD is slightly smaller for the PS-PWM modulation due to the higher effective switching frequency, i.e. six times effective switching frequency, as described in (2.17), because a limited amount of harmonics can be computed. This fact on the effective switching frequency is greatly observed by inspecting Fig. 2.14b, in which the WTHD is performed. As expected, the WTHD for the PS-PWM is much smaller, around one-sixth of the WTHD for the LSNP-PWM and LSP-PWM. Further, it can be observed that the WTHD reduces significantly by increasing the switching frequency for all the PWM techniques.



(a) THD (b) WTHD

Figure 2.14: Simulation - Weighted THD and THD Comparison for different PWM techniques (phase-shift (PS), level-shift with no permutation (LSNP) and level-shift with permutation (LSP)) in a 7L MLI depending on switching frequency with constant modulation index $m_a = 0.8$. THD is remained constant as harmonics component is the same. WTHD is reduced with high frequencies as harmonics are moved towards higher frequencies. WTHD utilizing PS-PWM is lowest because of highest effective switching frequency.

Figure 2.15 shows the simulation results for different levels of a CHB with constant switching frequency of $f_{sw} = 5$ kHz and constant modulation index of $m_a = 0.8$. It can be observed in Fig. 2.15a that the THD is greatly reduced when increasing the number of levels. This is because the more number of levels, the closer the output voltage will look like the fundamental sinusoidal waveform and less THD will be contained. As explained for Fig. 2.14b, the WTHD is greater reduced in PS-PWM compared to that of the LSP-PWM and LSNP-PWM due to the higher effective switching frequency. Further, it can be observed that the WTHD reduces significantly by increasing the number of levels for all the PWM techniques.

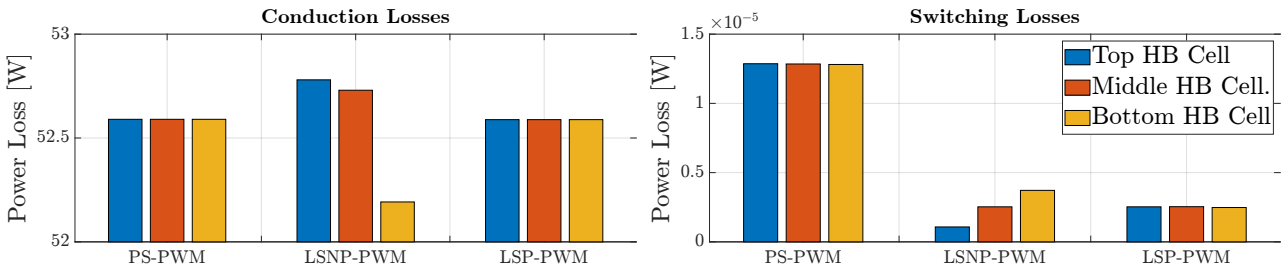


(a) THD (b) WTHD

Figure 2.15: Simulation - Weighted THD and THD Comparison for different PWM techniques in MLI depending on the number of levels with constant modulation index $m_a = 0.8$ and switching frequency $f_{sw} = 5$ kHz. THD is reduced with the number of levels as RMS AC output voltage is closer to sinusoidal fundamental waveform. WTHD utilizing PS-PWM is lowest because of highest effective switching frequency.

It can be observed in Fig. 2.14 and 2.15, that even though the THD is equal for all the PWM techniques, the WTHD for the PS-PWM is less than six times the WTHD of the LSP-PWM and LSNP-PWM. Therefore, utilizing PS-PWM would yield better power quality than the same system utilizing LSP-PWM and LSNP-PWM.

Regarding the losses distribution depending on the PWM technique, it is shown in Fig. 2.16 the losses for the conduction and switching losses in the three cells utilized in the 7L-CHB system at a constant switching frequency of $f_{sw} = 20$ kHz and modulation index of $m_a = 0.8$.



(a) Conduction Losses (b) Switching Losses

Figure 2.16: Simulation - Switching and conduction losses comparison between PWM techniques at 20kHz switching frequency in a 7L CHB.

Firstly, it can be observed in Fig. 2.16a, that, on average, all PWM techniques produce the same conduction losses, as the duty cycle per period remains the same, i.e., they conduct the same amount of current in a fundamental period. As expected, when applying PS-PWM or LSP-PWM, conduction losses are equally distributed among the cells, which is the main advantage of applying LSP-PWM. On the other one hand, when applying LS-PWM without permutation, i.e. LSNP-PWM, conduction losses are distributed unevenly among the cells. More precisely, the cell which is derived through the bottom triangular in the PWM scheme in Fig. 2.11 is the one with the highest conduction losses. Conversely, the cell switched with the top triangular in Fig. 2.11 is the one with lowest conduction losses. The same principle describes the switching losses in Fig. 2.16b for the LSNP-PWM technique, as the bottom cell is switched fewer times compared to the top cell, producing uneven switching power losses. It can be observed in the same figure that the switching losses in the PS-PWM are higher compared to that of the LS-PWM, as the effective switching frequency is of six times that of the LS-PWM.

Finally, it can be seen in Fig. 2.14, 2.15 and 2.16 that to choose the most convenient PWM technique, a balancing between power quality and losses distribution needs to be assessed.

2.6 Energy Storage Systems

The need to satisfy the increasing energy demand has pushed the growth for distributed generation (DG) to arise. DG reduces the power losses in the transmission system, improves power quality and increases the controllability of the system, among other advantages [34]. However, the high penetration of RES in the power grid, e.g. PV systems and wind farms, as examples of DG, implies the challenge of the output power control. To satisfy this issue, energy storage systems appear as a promising solution [35]–[40]. There exist different ways and technologies for storing energy, e.g. flywheels, hydrogen, compressed-air energy storage (CAES), superconducting magnetic energy storage (SMES), supercapacitors, battery energy storage systems (BESS) and pumped hydroelectric storage (PHS). Detailed information on the different ESS can be found in [34], [39]. As this project consists of BESS implementation, only electrochemical batteries are further explained.

2.6.1 Electrochemical Batteries

The utilization of batteries worldwide has spread in the last century, yielding to increasing research and development of materials and manufacturing technologies [41]. From now on, electrochemical batteries will be called *batteries* for the sake of simplification. Batteries convert chemical energy into electric energy by appropriate internal reactions in the cells. The manufactured structure of a battery is shown in a simplified diagram in Fig. 2.17.

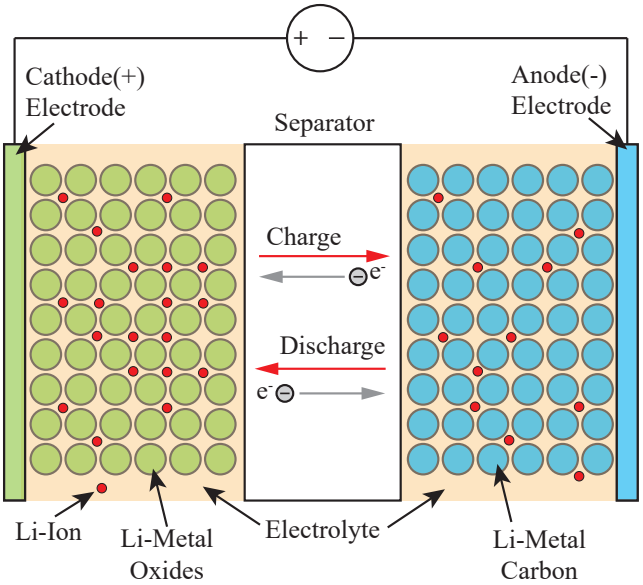


Figure 2.17: Simplified battery diagram. Battery degradation is important in second-life batteries, e.g. caused by electrodes fractures.

As can be observed in Fig. 2.17, the system consists of two electrodes, the cathode and the anode. A current is created when these electrons flow from one electrode to the other. The space between electrodes is called the electrolyte. The exchange of electrons is called the reduction-oxidation process, or *redox*[42]. When connecting a load to the battery, the negative ions leave the anode through the wire, creating a current into the load, and reaching the cathode. When the negative ions reach the cathode, they neutralize the positive ions. If this process continues, all the positive ions will be neutralized, producing an increase in the battery's internal resistance until the potential between electrodes is not enough to create electron flow in the electrolyte, achieving a fully discharged battery state [34]. A battery pack is formed by individual battery cells. Batteries can be recharged once they have been discharged or not, i.e. secondary and primary battery cells, respectively. They can also be distinguished depending on the materials used in the electrodes and electrolyte, the power ratings, power density and more.

The most established secondary batteries are made of, e.g. Lead-acid (Pb-Acid), Nickel Cadmium (Ni-Cd), Nickel-metal hydride (NiMH), Lithium-ion (Li-Ion) and Lithium-ion polymer. An overview of them can be seen in Table 2.2. Table data has been taken from [43], [44]. Economic aspects can be found in [40].

Table 2.2: Battery energy storage technologies - an overview

Type	**Energy Efficiency (%)**	**Energy Density (Wh/Kg)**	**Power Density (W/Kg)**	**Cycle Life (cycles)**	**Self Discharge**
Pb-Acid	70-80	20-50	250-500	200-2000	Low
Ni-Cd	60-90	40-60	140-180	500-2000	Low
Ni-MH	50-80	60-80	220	≤ 3000	High
Li-polymer	70	200	250-500	≥ 1200	Medium
Li-Ion	70-85	100-200	360	500-2000	Medium

Due to the Lithium-Ion battery's high energy and power density, they are increasingly being used in portable and stationary energy applications [45]. This is why Lithium-Ion batteries are widespread in electric vehicles (EVs) and hybrid -EVs (HEVs). It can be found in [46] a database with detailed information on the EV's batteries capacity. Further, in this project, second-life Lithium-Ion (Li-Ion) batteries are utilized for passive load and grid connection. In this matter, more than half of the grid connected BESS are based on Li-Ion technologies [40].

Definitions

The following terms are used to describe the physical and electrical properties of the battery [47]–[49]:

Capacity (C $[Ah]$): the amount of dischargeable charge available in the battery after a full charging.
Nominal Capacity (C_{nom} $[Ah]$): is the discharging capacity at nominal condition (current and temperature) after full charging.
Nominal Voltage (VN $[V]$): is the battery voltage at nominal condition (nominal current and temperature), at 50% SOC.
State of Charge (SOC [%]): is the amount of charge in the battery after a certain time and load conditions [50]:

$$SOC(t) = SOC(t_0) - \frac{1}{C}\int_{t_0}^{t} i(\tau)d\tau \tag{2.23}$$

Where SOC_0 is the starting point. As this method for SOC estimation includes the integral of the current, an increasing error can be computed if the measurement of the current is not precise.
Depth-of-Discharge (DOD [%]): is the inverse of SOC.
Capacity Rate (C_r $[hour^{-1}]$): Is the normalized current per unit of C.

$$C_r = \frac{I}{C} \tag{2.24}$$

State of Health (SOH): The SOH is the relation between the current battery state and the state when it was new. No unique mathematical definition exist [51]. This quantity can be related to different parameters, e.g. battery capacity, resistance, power, etc.

In this work, the SOH is defined as the ratio between the maximum actual C_{act} and the C_{nom}

$$SOH = \frac{C_{act}}{C_{nom}} \tag{2.25}$$

Volumetric energy density (VED $[Wh/l]$): is the energy that can be obtained per battery unit of volume.
Gravimetric energy density (GED $[Wh/kg]$): is the energy that can be obtained per battery unit of weight.
Power density (PD $[W/kg]$): is the power that can be obtained per unit of volume.
Calendar Life (CaL $[Years]$): the amount of time a battery can be stored (idling) before the C reached the end-of-life criterion, e.g., 20% of its initial capacity.
Cycle life (CyL $[Cycles]$): is the number of charging and discharging cycles a secondary type battery can accept before the C reached the end-of-life criterion, e.g., 20% of its initial capacity.
Internal Resistance (Ro $[\Omega]$)is the opposition to flow of current between electrodes.
Open-Circuit Voltage (OCV $[V]$): is the voltage at output battery terminals without any load connected.

2.6.1.1 Battery Model

There exist different ways for modelling a battery, i.e. lifetime and performance models. A lifetime model is used to assess the degradation of the battery and to estimate the expected lifetime for which the battery can meet the requirements. A performance model is used to asses the physical and electrical behaviour of the battery at different operating conditions [52]. The performance model can limit the laboratory testing, avoid hazardous situations with real batteries, and size properly the BESS for a given application. To make a battery equivalent model, different considerations and dependence need to be considered.

The performance battery modelling is derived in three different ways:

- Electrochemical: utilizing this modelling technique, it is possible to describe the behaviour of the microscopic and the macroscopic dynamics individually.
- Mathematical: in most cases, this modelling is obtained with empirical equations, allowing the knowledge of macroscopic quantities, e.g. voltage, efficiency and SOC.
- Electrical: in this technique, the battery is described by general equations illustrating the equivalent electrical circuit (EEC). The EEC is built utilizing voltage sources, capacitors, inductances and resistances.

Electrical Performance Model

The electrical model approach emulates the battery dynamics by utilizing electrical components, such as voltage sources, resistors and capacitors [52]–[55], as shown in Fig. 2.18. Therefore, the greater the number of RC stages, the more accurate the model will be under dynamic changes in the current.

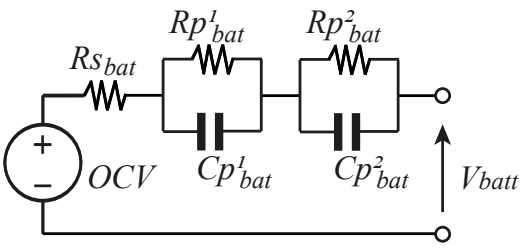


Figure 2.18: Second order electrical equivalent battery model. The higher the number of RC-branches, the better the model accuracy..

It is possible to represent the battery output voltage in state space form, to analyze the physical relation between components, if it was an $\mathrm{n^{th}} - \mathrm{RC}$ stage:

$$\begin{cases} \dot{V}_{cp,i} = \dfrac{i_L}{C_{p,i}} - \dfrac{V_{cp,i}}{R_{p,i}C_{p,i}} \\ V_{batt} = OCV - \displaystyle\sum_{i=1}^{n} V_{cp,i} - i_L R_o \end{cases} \tag{2.26}$$

It should be mentioned that the electrical equivalent battery model is dependent on different parameters, e.g. SOC (OCV), ambient temperature T and storage time [56]–[59]. In the range between 15% to 90%, OCV highly depends on the SOC rather than on the temperature. On the other hand, Z_{eq} highly depends on the temperature rather than on the SOC.

$$\begin{cases} OCV = f(SOC, T) \approx f(SOC) \\ \qquad Z_{eq} = f(SOC, T) \approx f(T) \end{cases} \tag{2.27}$$

The parameters seen in Fig. 2.18 can be obtained by curve fitting of data after a current discharge pulse method is carried on the battery of interest [60]–[63]. The discharge pulse method is shown in Fig. 2.19.

If the model to fit the data in Fig. 2.19 is a 1st order system, the parameters can be obtained as:

$$\begin{cases} R_s = \dfrac{\Delta V_0}{\Delta_I} = \dfrac{OCV - V_1}{\Delta I} \\ R_1 = \dfrac{\Delta V_1}{\Delta_I} = \dfrac{V_1 - V_2}{\Delta I} \end{cases} \tag{2.28}$$

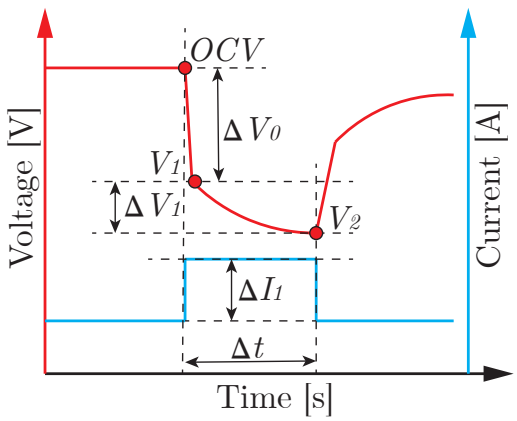


Figure 2.19: Li-Ion battery voltage response because of a discharging current pulse. Series resistance and RC-branch behaviour are related to ΔV_0 and ΔV_1, respectively.

Solving the differential equation for the capacitor voltage:

$$V_2 = V_1 e^{-\frac{\Delta t}{\tau}} \longrightarrow \tau = -\frac{\Delta t}{\ln\left(\frac{V_2}{V_1}\right)} \tag{2.29}$$

Then C_1 can be obtained as $\tau = R_1 C_1$.

2.6.1.2 State of Charge Estimation

The State of Charge (SoC) has a non-linear relationship with the open-circuit voltage (OCV) of the battery cell [64], in which $it \propto SOC$. Different methods to estimate the SOC have been proposed in the literature and the most important ones are shown in Table 2.3 and more can be found in [64], [65].

Table 2.3: SoC estimation methods

Method	Principle of Operation	References	Complexity	Reliable
Open Circuit Voltage	Non-linear relation between SOC-OCV with lookup table which needs to be very accurate	[66]–[69]	Low	High
Impedance Spectroscopy	Measure battery impedance and correlate to SOC with lookup table. The table is computed by measuring the battery impedance at different frequencies	[65], [70], [71]	Medium	Medium
Ampere-Hour Counting	From known initial conditions, which are difficult to determine, measure how much current is delivered and supplied	[72], [73]	Low	Medium
State Estimation	Based on Kalman Filters implement state observers. Not very affected by initial conditions.	[74]–[82]	High	High

The widely used method chosen in this work to estimate the SOC of the batteries is the Ampere-Hour counting method, which is based on (2.23), repeated here for the sake of completeness:

$$SOC(t) = SOC(t_0) - \frac{1}{C}\int_{t_0}^{t} i(\tau)d\tau \tag{2.30}$$

The actual SOC is settled on a previous state of the battery SOC. Therefore, if there exists an error in the initial condition for, i.e. $SOC(t_0)$ is incorrect, then the actual SOC will be affected by an accumulated error. Furthermore, as can be seen in (2.30), the actual SOC is calculated by taking into account the integral of the current in the battery. This current measurement is affected by measurement noise in practical applications, causing the actual SOC to drift from its real value. To overcome this issues, it is proposed in the literature to estimate the SOC by combining two or more methods [83], [84], e.g. Ampere-Hour counting and Open Circuit Voltage look-up table.

Battery parameters are strongly dependent on the SOC. One of the most important parameters to the SOC is the battery open-circuit voltage (OCV). Although there is no unique solution for the relationship between the OCV and the SOC, non-linear solutions have been presented in the literature [79]. The relation between OCV and SOC can be expressed in a polynomial-, logarithmic-, exponential equation, or a combination of them. The combined equation can be expressed as in (2.31) [85] .

$$OCV(SOC) = \alpha_0 + \alpha_1 SOC + \alpha_2 \ln SOC^{-\beta_1} + \alpha_3 e^{-\gamma(SOC-1)} + ... \tag{2.31}$$

In this project, the following (2.32) equation is utilized to describe the relation between SOC and OCV [52]:

$$OCV(SOC) = \alpha_0 + \alpha_1 SOC + \alpha_2 SOC^2 + \alpha_3 SOC^3 + \alpha_4 e^{\beta_1 SOC} \tag{2.32}$$

In which $\alpha_0 = 3.685$, $\alpha_1 = 0.2156$, $\alpha_2 = -0.1178$, $\alpha_3 = 0.3201$, $\alpha_4 = -1.031$ and $\beta_1 = -35$ when the battery is discharging. These parameters are calculated for a single battery cell. The relation between OCV and SOC with (2.32) is shown in Fig. 2.20. In such a figure, a battery pack curve has been plotted. The battery pack OCV-SOC curve is obtained by multiplying the OCV-SOC for a single battery cell with a number of series connected cells. In Fig. 2.20, 70 cells are connected in series to achieve a higher battery voltage level [86]. The curve has been kept equal in the charge and discharge process [59], as the difference caused by not doing so are not of great importance in this project.

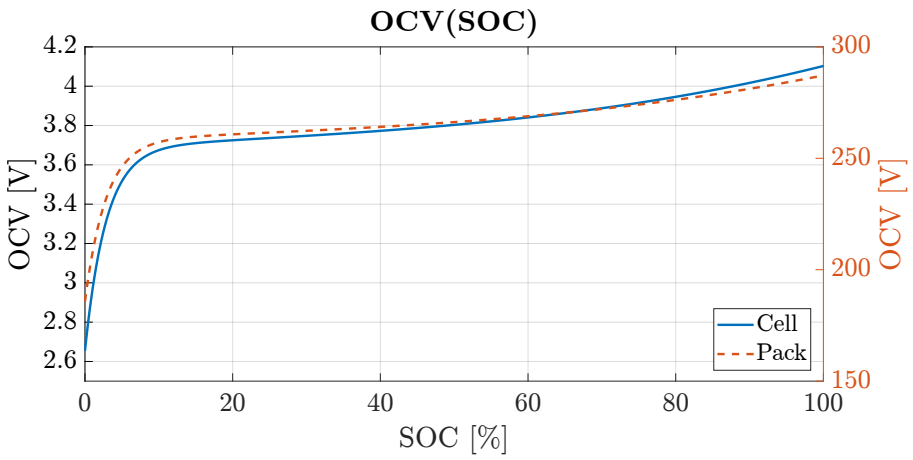


Figure 2.20: OCV as a function of SOC. Battery pack voltage approximated to serial connection of 70 cells.

2.6.1.3 Second-Life Batteries

A battery's lifetime can be defined in different stages. The beginning-of-life (BOL) starts when the battery finishes the manufacturing process. The first-life utilization (concept mainly referred to in the EVs market) ends when the battery fade is below a specific limit, after when the second-life begins. The battery's end of first-life fade limit is different depending on the requirements.

When a battery is at the end of its first-life, i.e. when it has a capacity of roughly 80%[87], [88] of its initial capacity in EVs applications, it can still be employed in applications with less strict requirements, such as residential or grid support [89]. It can be seen in Fig. 2.21 the concept behind battery degradation and second-life batteries (SLB) from beginning-of-life (BOL). The uncertainties related to the remaining capacity of a SLB can be expressed as a normal distribution of an average 75% [90].

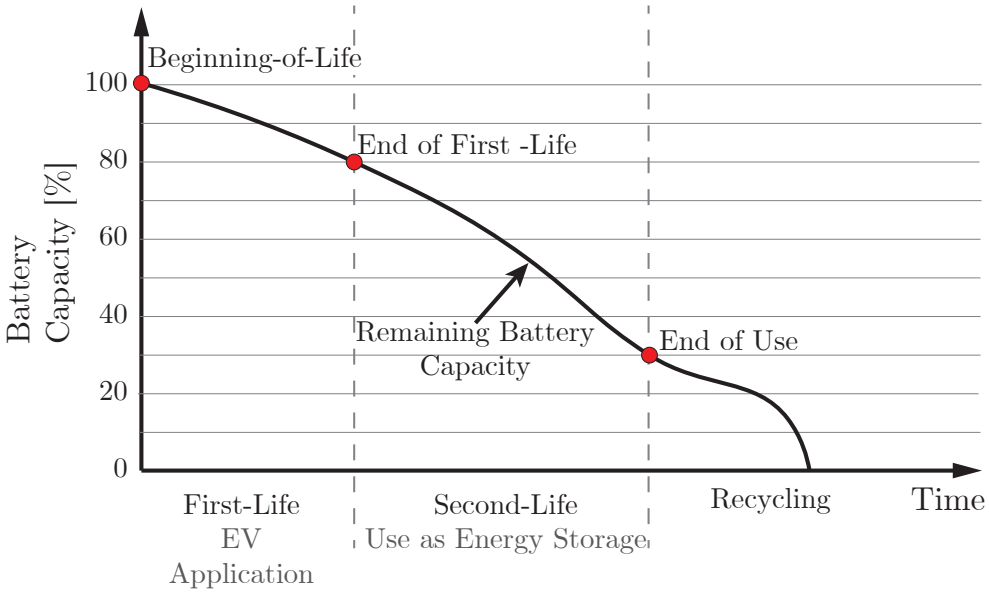


Figure 2.21: Residual battery capacity over lifetime

The actual state of degradation or ageing of a battery can be quantified with the State-of-Health (SOH) [91]. The SOH can be related either to the battery resistance or capacity [92] and depending on the application, one or the other can be used.

Battery degradation or capacity fading is produced both by time (calendar ageing), and the number of cycles (cycling calendar) [93], [94]. Capacity fading can be divided into true capacity fading and rate capability loss [55]. True capacity fading is described by the relation between Li-Ion and active material loss, being independent on the current. In contrast, rate capability loss is related to its electrical variations in the internal resistance, dependent on the current [95]. A degraded battery increments the battery resistance [96] and an impedance growth [87]. Further, the battery impedance provides information on the SOC and SOH [97]. Battery storage at high temperatures can also produce more rapid degradation or capacity fade [87], [98].

The more degraded a battery is, the OCV-SOC curve is shifted more vertically in the discharging process and down in the charging process, producing a wider hysteresis area between them due to an increment in internal resistance [99]. The increasing resistance can be modelled with a polynomial-exponential equation as in [89]. The greater the number of terms, the more accurate the model will be compared to reality. In this project, the rate of change in the internal resistance is modelled as a constant value, as the rate of degradation is relatively low compared to the control time constants.

2.6.1.4 Second-Life Battery Model and Impedance Determination

Measurements and estimations on the battery impedance parameter can provide reliable information on the battery SOC and SOH [45], [97], [100]. Different methods can be used to determine the impedance. One of the most widely used is the Electrochemical-impedance-spectroscopy (EIS), which is an accurate method but challenging to implement due to its high complexity and long experimental times [101]. Other methods are proposed in the literature to overcome these drawbacks, i.e. broadband signal injection, e.g. pseudo-random-sequence (PRS) [102]. EIS method is mainly based on the injection of a sinusoidal current and measurement of the voltage amplitude and phase-shift to determine the impedance, as described by (2.33) [100], [103], [104], in which $Z_{bat}(j\omega)$ is the battery impedance, $V_{bat}(j\omega)$ and $I_{bat}(j\omega)$ are the battery terminal measured voltage and injected current, respectively.

$$Z_{bat}(j\omega) = \frac{V_{bat}(j\omega)}{I_{bat}(j\omega)} \tag{2.33}$$

The sinusoidal current is provided with different frequencies, obtaining the battery impedance spectrum in the real-complex plane, as can be seen in Fig. 2.22.

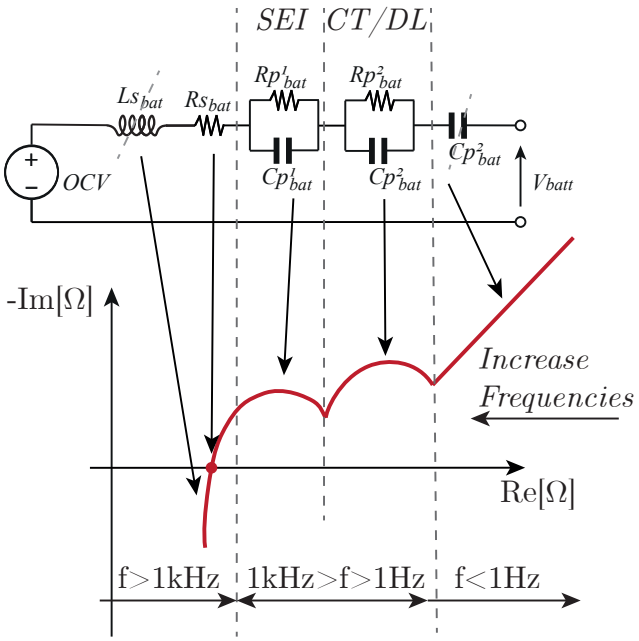


Figure 2.22: Battery Impedance plot in the Nyquist plane.

As seen in Fig. 2.22, the EIS curve consists of two semiellipses. The first semiellipse is related to the growth of the Solid-Electrolyte Interface (SEI), which appears at the battery electrode's material decomposition due to ageing [105]. The second ellipse is related to two processes, i.e. the charge transfer (CT) in the interface between electrodes and electrolyte, as well as the impedance in the battery chemical reaction, i.e. double layer capacity (DL) [106], [107]. Due to these processes related to battery ageing, second-life batteries will show different EIS curves according to their ageing. The greater the ageing, the lower the performance [108]. At very low frequencies, the diffusion effect reflects the mass transportation damping in the electrolytes [105], which can be neglected when considering higher frequencies [109].

In this work, the impedance spectroscopy (IS), is carried out with a CHB system consisting of three cells, i.e. a 7L multilevel inverter. As the system in this work provides power in a single-phase system, the current in the battery has a ripple of 100Hz with a DC offset, described in Section 2 equation (2.8). By measuring this current and the voltage ripple in the battery caused by the battery parameters equivalent circuit, it is possible to obtain an estimation of the battery parameters as described in [110]. In such work, only the internal resistance (IR) of the battery is estimated, which is typically estimated by a current pulse to the battery, measuring the output voltage, i.e. the DC-pulse technique [58]. By considering the DC-pulse technique for parameters extraction (explained in Section 2.6.1.1, this linear equivalent model would reflect only the behaviour of the voltage drop across the internal resistance (ΔV_0), omitting dynamical components added by the RC branches, as shown in Fig. 2.23, in which the IR is equivalent to the series resistance Rs.

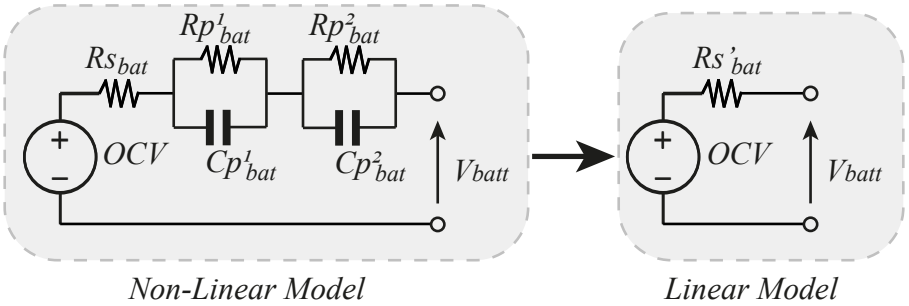


Figure 2.23: Impedance Estimation - Linear model approximation. RC branches dynamical behaviour is neglected.

The internal resistance can be estimated by utilizing (2.34).

$$\hat{Z}(\Omega) = \frac{V_{batt}^{max} - V_{batt}^{min}}{I_{batt}^{max} - I_{batt}^{min}} \tag{2.34}$$

As explained in Section 2.6.1.1, the internal resistance is strongly dependent on the battery operating conditions. Therefore, the internal resistance estimation needs to be computed at similar conditions, i.e. at similar SOC, temperature, etc. The internal resistance can be utilized to estimate the SOH of a battery, as they are related by complex interactions [111]. After obtaining the IR estimation, the OCV can be estimated by utilizing (2.35) [110]. The drawback of this method, is that it would not reflect the degradation of a second-life battery, as the non-linear RC-branches in the performance model may become bigger and are not included in this technique.

$$O\hat{C}V = \bar{V}_{batt} - \bar{I}_{batt} \cdot \hat{Z} \tag{2.35}$$

This estimation of the OCV combined with the SOC estimation can be utilized to estimate the actual battery capacity.

The knowledge of the SOH and battery capacity estimation can be utilized in more complex control techniques in which the batteries with the lowest SOH are being used less in the long-term time scale. In such a way, the SOE can be balanced in the short-term with the proposed strategies shown before and a SOH balancing in the long-term operation. The implementation of the SOH into the control strategies was not included as it is out of the scope of this work.

Chapter 3

System Description

This chapter presents a general description of the system. First, the individual inverter is briefly presented. Then, the DC-link capacitor is explained. Third, as the output LC filter is given, the frequency response is analyzed. Finally, a grid side inductance is designed and explained. The final topology utilized is shown in Fig. 3.1.

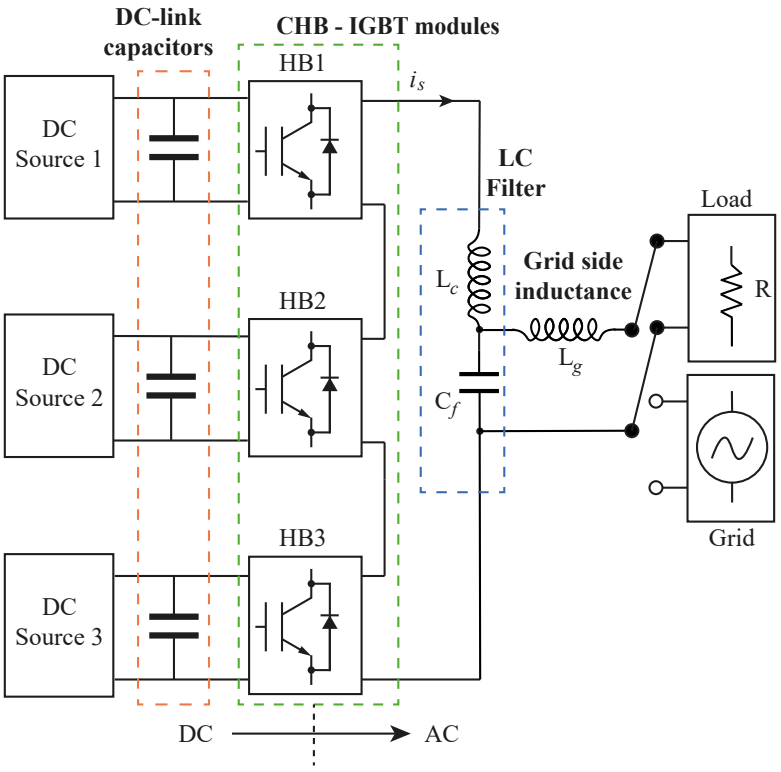


Figure 3.1: Final Topology Utilized. Decentralized topology in a single-stage DC/AC.

The system consists of a three-cell CHB. Each H-Bridge is a three-phase IGBT module and has a DC-link capacitor as explained below. The DC-link voltages in the simulations can go up to 270 V, whereas in the laboratory can only go up to 120 V. The output of the CHB is connected to an LC filter, which was added a grid side inductance to avoid resonances. The system description and analysis is exposed below.

3.1 IGBT Module

The IGBT module utilized is the FS50R12KT4_B15 from Infineon [112]. The IGBT module utilized is a three-phase half-bridge power module, which can be utilized as a single-phase H-bridge by using two of the half-bridges and leaving the third one unconnected. The inverter is mounted on a printed circuit board (PCB), which is described in detail in Appendix A.

3.2 DC-Link Capacitor

Each individual H-Bridge in the CHB has a capacitor at its DC-link voltage input terminals. This capacitor smooths the current ripple, providing a DC current source, with an AC current on top, with double the fundamental frequency, as explained in Section 2.3. The voltage ripple can be set to a allowed maximum of 5% of the capacitor voltage. Then, utilizing (3.1) [113], [114]:

$$\Delta V_{cap} = \frac{Po}{\omega \cdot C \cdot V_c} \tag{3.1}$$

Where ΔV_{cap} is the capacitor voltage ripple, P_o is the average power injected to the load, ω is the fundamental frequency, i.e. 50Hz, V_c the capacitor peak to peak voltage ripple and C is the capacitor capacitance.

$$C_{dc} = \frac{P_o}{\omega \Delta V_c \cdot V_c} = \frac{P_o \text{ W}}{\omega 5\% V_c^2} \longrightarrow C_{dc} = \frac{600 \text{ [W]}}{2\pi 50 \text{ [rad/s]} \cdot 0.05 \cdot 150^2 \text{ [V}^2\text{]}} = 1.7mF \tag{3.2}$$

The PCB in which the DC side filter is mounted on has an equivalent capacitance of 680 μF. An additional PCB has been designed and build to accomplish with the DC side filter requirements, as explained in Appendix A.

3.3 Output Filter Analysis

The output filter used at the AC side of the CHB is an LC filter, as shown in Fig. 3.2. The filter used is the FN5040-24-84 [115], which inductance value is $L_c = 4.8$ mH and capacitance value is $C_f = 5$ μF. The cables for the connection have an omhic resistance of 1 mΩ and are shown in Fig. 3.2.

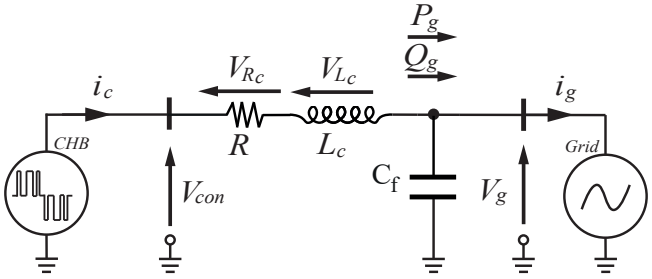


Figure 3.2: Single-phase LCL output filter diagram. Converter side inductance and capacitor are fixed. Grid side inductance can be determined.

The transfer function of the LC filter is expressed as in (3.3) [116].

$$H_{LC}(s) = \frac{sL_c + R}{s^2 C_f L_c + sC_f R + 1} \tag{3.3}$$

Substituting the values given for the LC filter, the bode plot of the frequency response is shown in Fig. 3.3. As can be seen, the resonance frequency is placed at $f_{res}^{LC} = 1$ kHz.

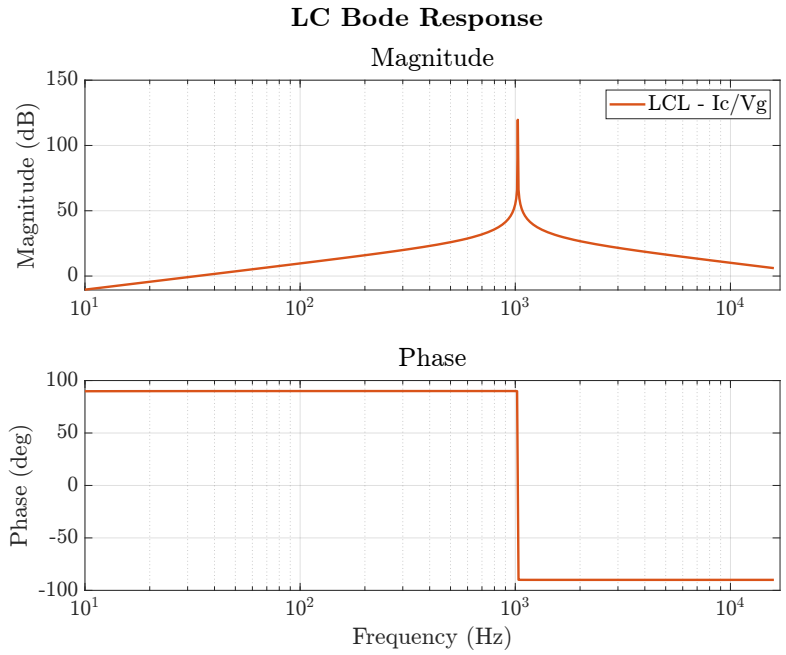


Figure 3.3: Bode diagram of the LC filter utilized in the laboratory. Resonance frequency at 1KHz.

3.3.1 Converter Side Inductance and Capacitor

The converter side inductance is connected between the output of the CHB and the terminals of the filter capacitor. This inductance is designed to limit the current ripple caused by the switching of the converter. To calculate minimum switching frequency that is needed, with the given converter side inductance (L_c) it is used (3.4) from [117], [118]. The maximum voltage which can be achieved in the DC side in the laboratory is 120 V, and the number of levels at CHB output terminals is $m = 7$, then:

$$\Delta i_{max} = \frac{V_{dc}^{cell}}{4(m-1) f_{sw} L_c} \longrightarrow f_{sw} = \frac{V_{dc}^{cell}}{4(m-1) L_c \Delta i_{max}} \tag{3.4}$$

In that way, substituting the values taken to be implemented in the laboratory, allowing a current ripple in the converter side output to be 10% of the rated current, it can be obtained the minimum switching frequency.

$$f_{sw} = \frac{120 \text{ V}}{4(7-1) \cdot 4.8 \cdot 10^{-3} \text{ mH} \cdot 10 \text{ \%} \cdot 10 \text{ A}} \approx 1 \text{ kHz} \tag{3.5}$$

The minimum switching frequency which needs to be applied to the PWM modulation technique is of 1kHz. It is finally utilized a switching frequency of 2.8kHz, which results in a effective switching frequency of $2H \cdot 2.8$ kHz = 16.8 kHz, as explained by (2.17) in Section 2.

After the converter side inductance, the grid side capacitor is placed. The value for this capacitance limits the reactive power production [114]. From the datasheet for the FN-5040 LC filter, the nominal capacitance is of 5 μF. Due to hardware limitations, the output of the LCL filter is connected to a grid simulator with an amplitude of half the grid voltage, i.e. $115V$. Utilizing (3.6), it can be seen that the power factor variation seen from the grid is less than 0.05%.

$$C_f = \Delta C_{g,nom} \frac{Po}{\omega V_{c,g}} \longrightarrow \Delta C_{g,nom} = C_g \frac{\omega V_{cg}}{P_o} \longrightarrow \Delta C_{g,nom} = 5\ [\mu\text{F}] \cdot \frac{2\pi 50\ [\text{rad/s}] \cdot 115\ [\text{V}]}{3 \cdot 180\ [\text{W}]} = 0.033\% \tag{3.6}$$

3.3.2 Grid Side Inductance

When utilizing the above described filter in the laboratory, connected to a grid simulator, which is a conmutated DC supply, it was found that the device created resonances with the system, therefore, a grid side inductance was designed to move the resonance frequencies towards greater frequencies. Then, the original LC filter becomes now an LCL filter, which is shown in Fig. 3.4

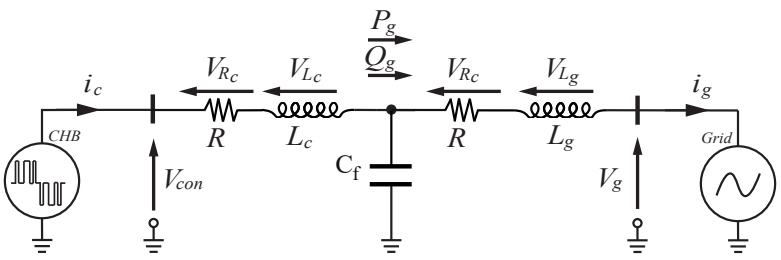


Figure 3.4: Single-phase LCL output filter diagram. Converter side inductance and capacitor are fixed. Grid side inductance is designed.

From Fig. 3.4, the transfer function of the filter can be studied. The total impedance of the filter in the Laplace domain can be expressed as in (3.7) [117], [119], when the grid current and voltage are measured.

$$H(s) = \frac{i_g}{v_s} = \frac{1}{L_c C_f L_g s^3 + s^2(L_c R C_f + R C_f L_g) + (R^2 C_f + L_c + L_g)s + 2R} \tag{3.7}$$

and for $H(s) = i_s/v_s$ as in (3.8), when the converter current and grid voltage are measured:

$$H(s) = \frac{i_s}{v_s} = \frac{L_g C_f s^2 + s C_f R + 1}{L_c C_f L_g s^3 + s^2(L_c R C_f + R C_f L_g) + (R^2 C_f + L_c + L_g)s + 2R} \tag{3.8}$$

The grid side inductance needs to be determined to accomplish with grid quality requirements and avoid undesired resonances in the system.

To avoid resonance, the resonance frequency of the LCL filter needs to be within the range [117], [119]:

$$10 \cdot f_{grid} \leq f_{res} \leq 0.5 f_{sw} \longrightarrow 500Hz \leq f_{res} \leq 8.4kHz \tag{3.9}$$

and given (3.10) [1]:

$$f_{res}^2 = \frac{1}{4\pi^2} \frac{1}{L_g C_f} \cdot \frac{L_g + L_c}{L_c} \tag{3.10}$$

Then, extracting L_g from (3.10) yields to:

$$L_g = \frac{L_c}{4\pi^2 f_{res}^2 C_f L_c - 1} \tag{3.11}$$

Then the grid inductance can be chosen between the limits expressed in (3.9) by placing $L_c = 4.8$ mH and $C_f = 5$ μF.

$$L_g \geq 0.08 \text{ mH} \tag{3.12}$$

The filtering behavior is shown in the bode diagram in Fig. 3.5. The grid side inductance placed in the laboratory has a value of 1 mH.

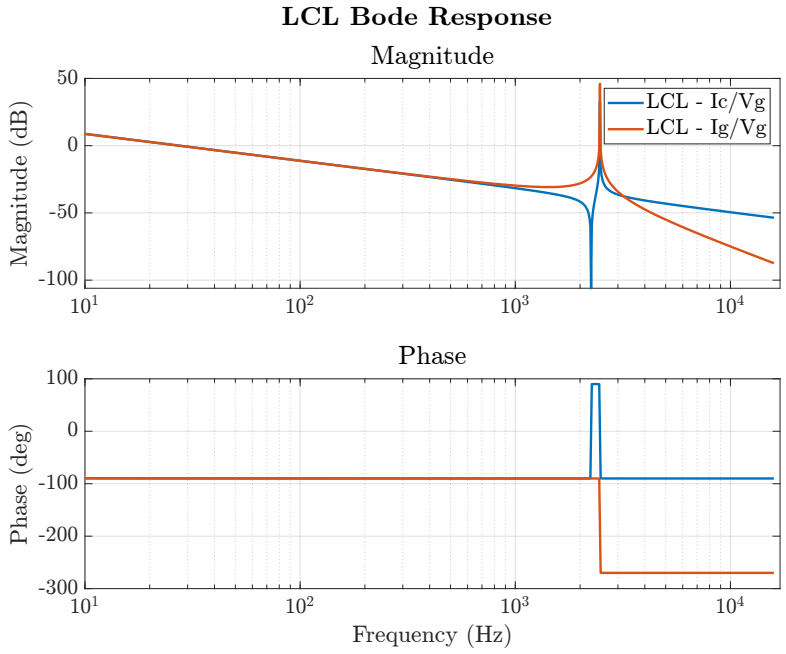


Figure 3.5: LCL Bode diagram. The resonance frequency is at 2.4kHz and the effective switching frequency is at 16.8kHz.

As seen, the resonance frequency has moved from 1 kHz to 2.4 kHz and the resonances where avoided when connecting to the grid simulator. Further, the switching frequency is far from the effective switching frequency, i.e. 16.8 kHz.

Chapter 4

Control of the Cascaded H-Bridge

This chapter will focus on the control techniques and methods used to control the system. First, the topology is shown and the chosen control scheme is described. Then, the current control loop is explained and analyzed compared to standards and literature. The phase-locked-loop is justified with several tests. Once these stages are completed, the battery energy management system is explained by showing a proposed active balancing technique and three strategies to operate the system, followed by simulation results to verify the performance. Lastly, an impedance spectroscopy estimation technique is proposed, however as it is out of the scope of this project, no final conclusions could be assessed.

4.1 Control Scheme Description

As described in Section 2, there exist many ways for interfacing the batteries with the power grid or load. The one used in this project is shown in Fig. 4.1. Different control methods have been proposed to operate the system [1], [13], [15], [16], [18], [120]–[123]. The control method selected to operate such systems is based on the instantaneous power theory (IPT) [1], [29]. The proposed control method can be seen in Fig. 4.2, which shows the final topology utilized in the project. This control method allows to independently control the active and reactive power injection or absorption from the grid. Typically, it provides a unity power factor in the injected power. The grid demands a specific power. This power is translated to a current reference in the output LCL filter, so the converter supplies such current. The voltage across the inductance is controlled to supply such current through the converter side inductance. This voltage across the inductance is produced by the difference between the output CHB voltage and the capacitor voltage of the LCL filter, which is approximately the same as the grid voltage. If the current to be controlled is the load current, then the active and reactive power is handled directly with the IPT. Suppose the converter side inductance current is the one to be controlled. In that case, it is needed to compensate for the active and reactive power consumed and produced by the LCL filter to inject the reference current into the load with the commanded power factor [124]. In this work, it has been assumed that the LCL filter behaves approximately equal to an L filter which is value is the sum of the converter side inductance and the grid side inductance, as explained in the introduction of Chapter 12 in [1]. The output CHB voltage is built up of the sum of the output of each independent H-Bridge converter. Therefore, the voltage reference across the inductance will be split across the H-Bridges converters, depending on different characteristics, summed up in the BEMS unit.

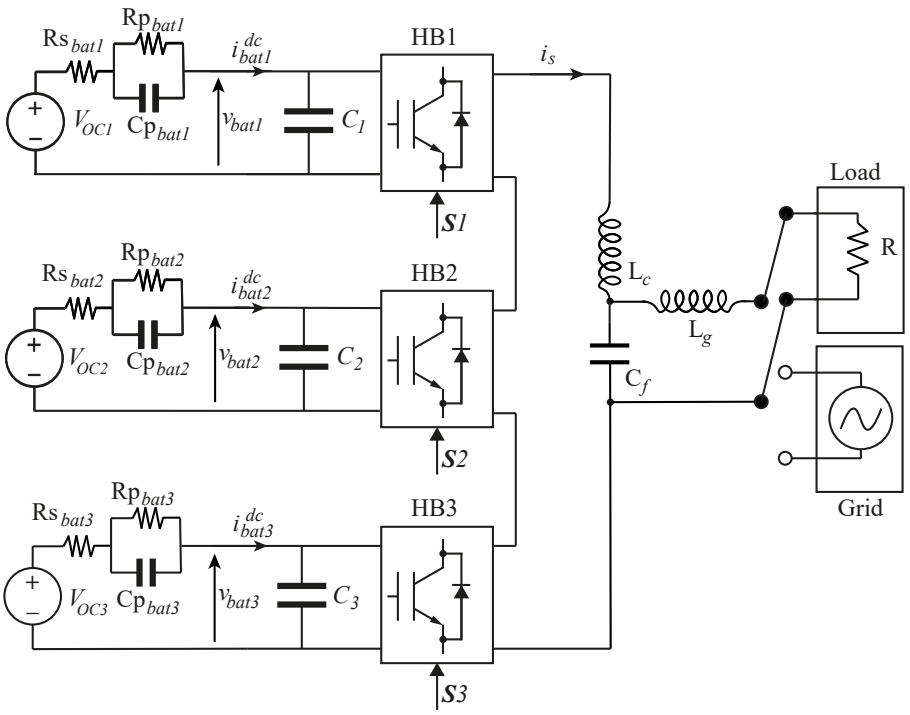


Figure 4.1: Decentralized battery connection in a single stage. Batteries are modelled with a single RC stage and a series resistance. An LCL filter is utilized to interface the CHB with the load and grid.

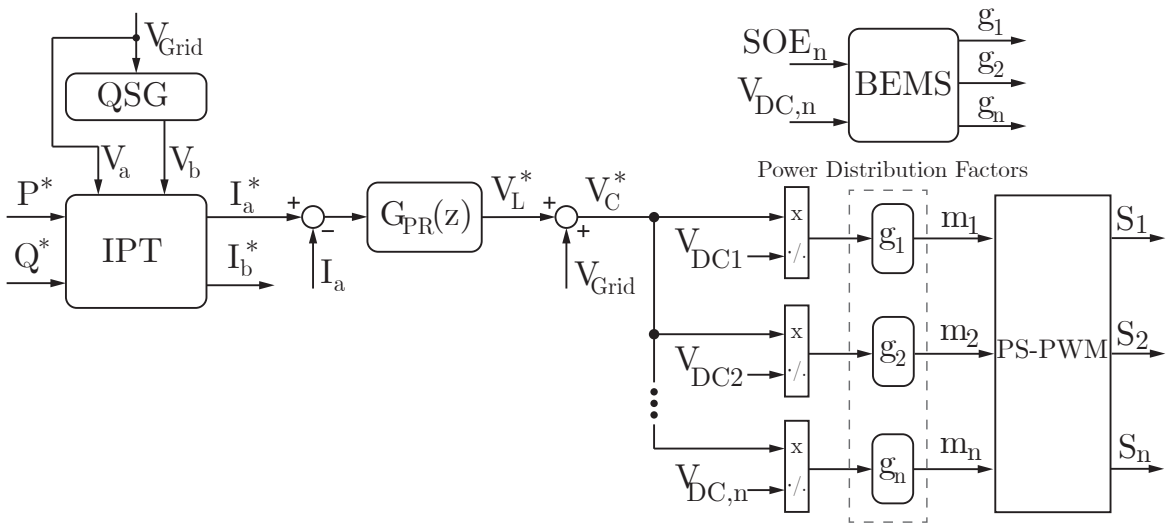


Figure 4.2: Control method based on the instantaneous power theory. One PR Controller is utilized to control the output AC current.

The control scheme shown in Fig. 4.2 is described now. The active and reactive power inputs are provided to the system. The grid voltage is forwarded to the quadrature signal generator to obtain the $\alpha\beta$ voltage components. This fours signals, i.e. P^*, Q^*, V_α and V_β, are computed in the IPT block to obtain the current references. This work is based on a single-phase system, i.e. only the α component is utilized. The current reference is subtracted from the real measured current and fed to the resonant controller block.

The output is the reference voltage that must be applied to the filter to obtain the reference current. The commanded converter side voltage is obtained by adding the grid side voltage. The commanded converter voltage is then divided by the individual DC-link voltages of the CHB to obtain the modulation signals. These modulation signals are modified by the power distribution factors g_n to distribute the power among the cells according to the strategies that will be later explained. Finally, the modified modulation signals m_n are forwarded to the PS-PWM technique utilized in this project to switch the H-Bridges of the CHB. The detailed steps in the control system are elaborated below. The inputs to the system are the power references. which are transformed to currents references by utilizing the IPT matrices [125]:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{4.1}$$

Which then, isolating i_α and i_β yields to:

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{v_\alpha^2 + v_\beta^2} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \cdot \begin{bmatrix} P \\ Q \end{bmatrix} \tag{4.2}$$

4.1.1 Current Control Loop and PLL

Regarding the **PR current controller**, the ideal PR controller block diagram is shown in Fig. 4.3. Therefore, the transfer function can be obtained as in (4.3) [126]–[128].

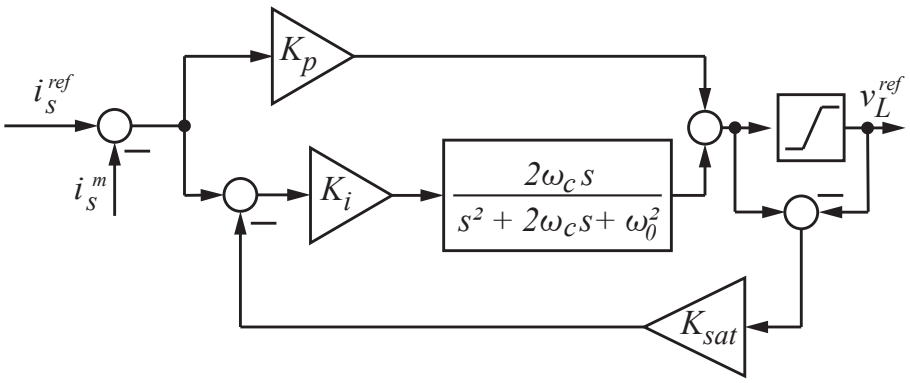


Figure 4.3: Block diagram of a non-ideal PR controller. The cut-off frequency ω_c avoids infinite gain at fundamental frequency ω_0.

$$C_{PR}(s) = K_p + \frac{2K_i s}{s^2 + \omega_0^2} \tag{4.3}$$

As can be seen in Fig. 4.4, at the fundamental frequency, a very high gain is produced. Therefore, a non-ideal PR controller can be applied, which transfer function is (4.4):

$$G_{PR}(s) = K_p + \frac{2K_i \omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{4.4}$$

In which ω_c and ω_0 are the cut-off frequency and fundamental frequency of the controller. The bode diagram of the system for both controllers can be observed in Fig. 4.4. Two different cut-off frequencies have been investigated. The cut-off frequency is a trade-off between steady-state tracking error and the sensitivity of the system against frequency deviations [129]. In this work, the cut-off frequency has been selected to be 2 Hz, which is in the typical range between 5-15 rad/s [130].

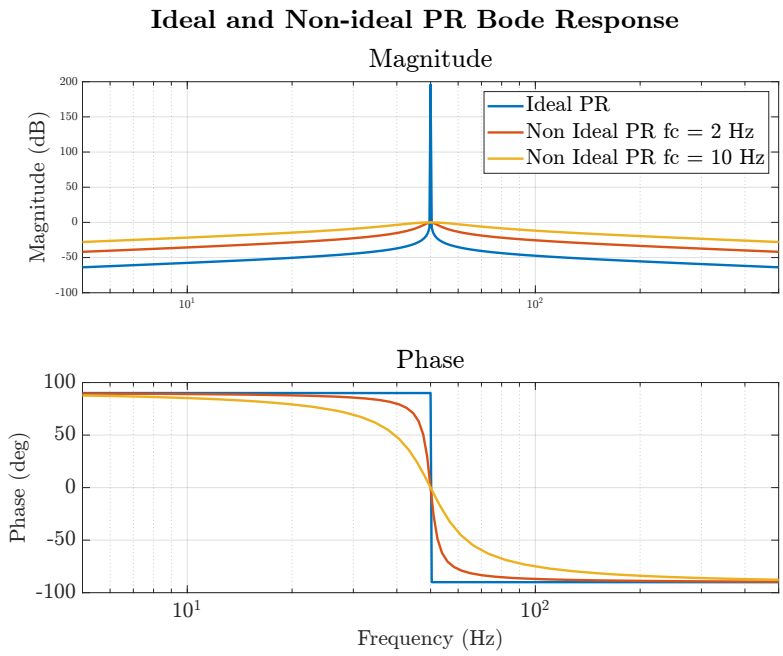


Figure 4.4: PR controller - Bode Diagram

The controller is then discretized using the Tustin method, which is proven in the literature to have better performance [131] with a sampling time of $Ts = 40$ μs or 25 kHz yielding to the transfer function $G_{PR}(z)$ (4.5).

$$G_{PR}(z) = 10^{-4} \cdot \frac{5.02 \cdot z - 5.02}{z^2 - 1.999 \cdot z + 0.999 \cdot z}. \tag{4.5}$$

The system PR parameters have been tune by fitting the parameters in the block diagram shown in Fig. 4.5. A delay block has been implemented to emulate the computation time (or PWM delay [132]) with the sampling time explained before, i.e. $Ts = 40$ μs, represented by $G_d(s)$ in Fig. 4.5 as:

$$G_d(s) = \frac{1}{1 + 1.5T_d s} \tag{4.6}$$

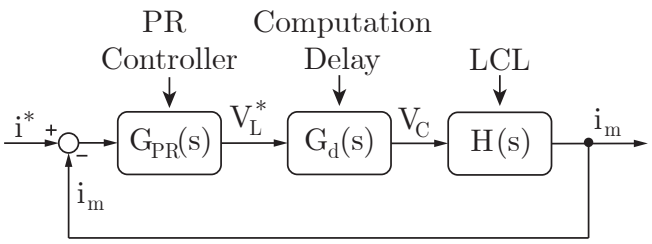


Figure 4.5: PR controller - Controller Block Diagram. The PR controller, computation delay and the LCL filter plant connected in series. The measured current is then fed-back and subtracted to the reference current.

The parameters are tuned to obtain an overshoot of less than 5% against step changes in the measured current, with the optimal damping factor of $\zeta = 1/\sqrt{2}$ [130]. The settling time is less than 5 ms, i.e. the error is less than 5% in less than one-fourth of a fundamental cycle. As explained at the beginning of the chapter, it can be assumed that the capacitance in the LCL filter has a neglectable effect on the frequency response of the filter. Therefore, the PR parameter tuning can be made considering the converter- and grid-side inductances and the cables resistances added together. Therefore, the open-loop transfer function obtained from Fig. 4.5 is shown in (4.7).

$$G_{OL}(s) = \left(K_p + \frac{2K_i\omega_c s}{s^2 + 2\omega_c s + \omega_0^2}\right) \cdot \frac{1}{1 + 1.5T_d s} \cdot \frac{1}{R_c + R_g + (L_c + L_g)s} \tag{4.7}$$

Then, it has been obtained that for a $K_p = 48$ and a $K_i = 2000$, the phase margin is around 42°, being the range typically $30° \leq PM \leq 60°$ [133]. With this parameters which ensure stable operation, the overshoot in a step response is approximately 5% with a 5% settling time of less than 2 ms. The theoretical step response in continuous time domain of the resonant controller is shown in Fig. 4.6

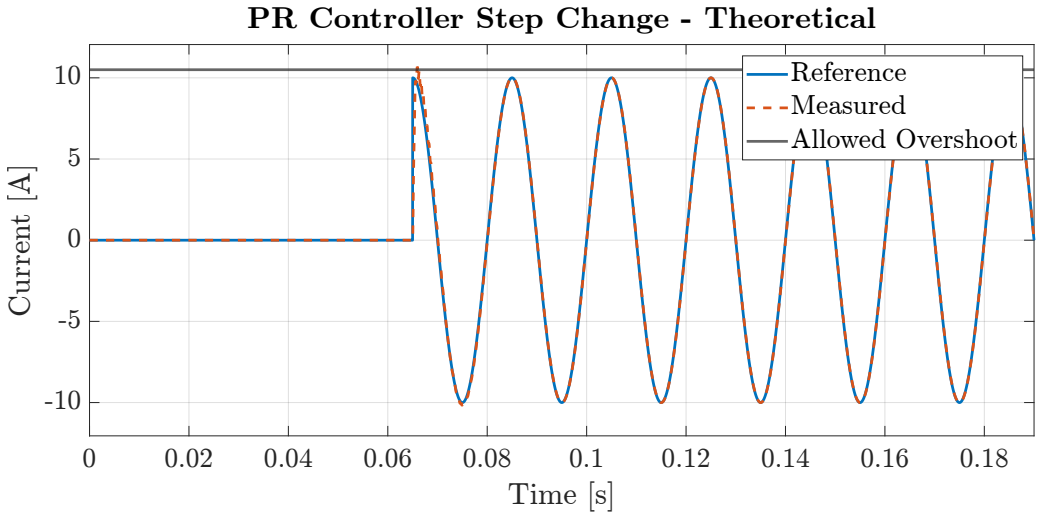


Figure 4.6: PR controller - Step Response Diagram Theoretically

The response of the resonant controller in the simulations is shown in Fig. 4.7. It should be noted that in the simulations, the LCL filter is placed with the capacitor and is implemented in discrete time domain, which makes a slightly difference with the theoretical waveform obtained in Fig. 4.6. As can be seen in Fig. 4.7, the overshoot is less than 5% against a step change. The THD is measured to be 2.68% in simulations, below the limit of 4.5% for the first 40 harmonics, as specified in the danish grid code for battery plants connection [134].

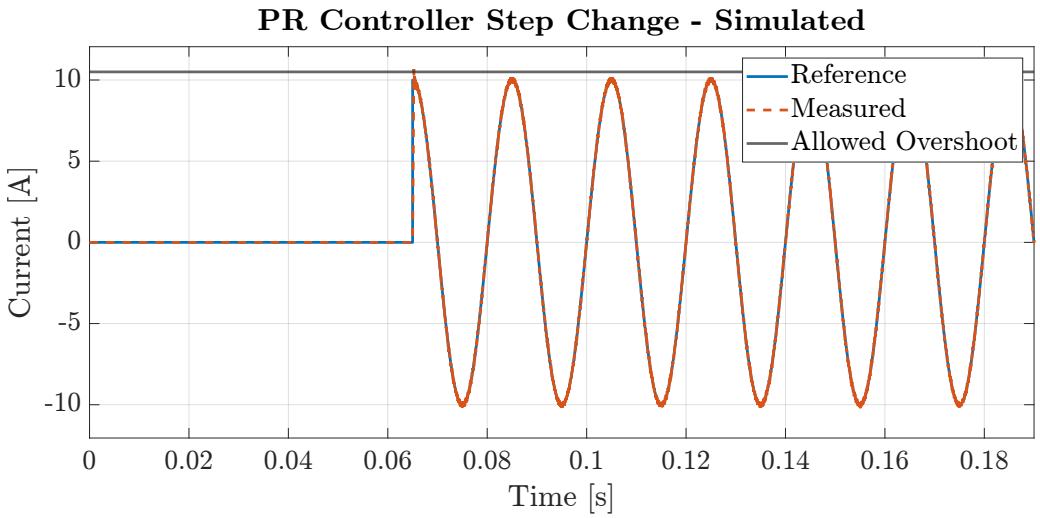


Figure 4.7: PR Controller - Simulated currents waveform response

Further, a THD analysis has being carried out, and is shown in Fig. 4.8. This harmonic indices accomplish with the Danish regulation for grid connection of battery plants [134].

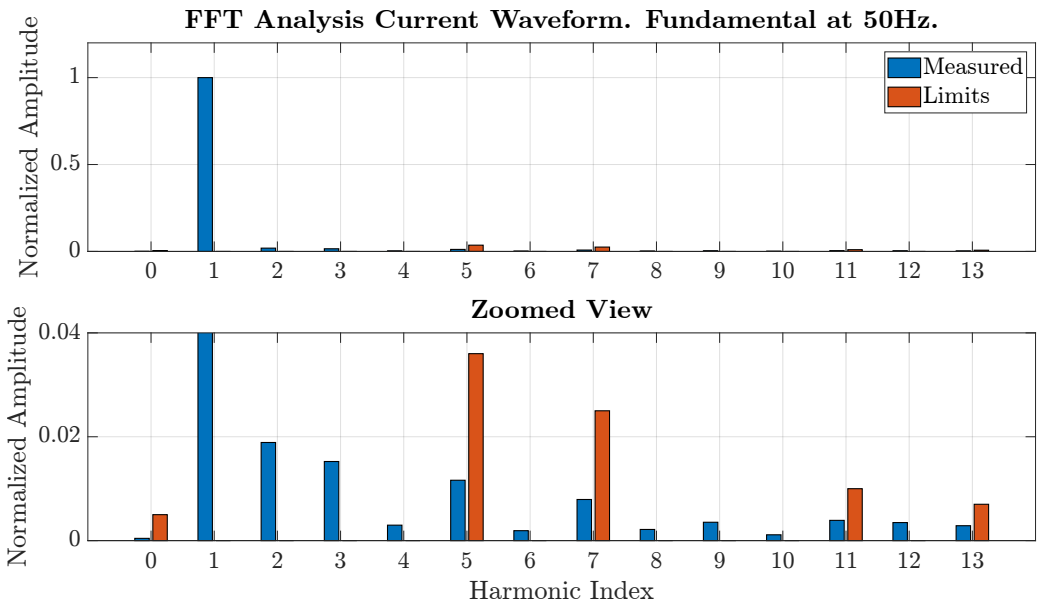


Figure 4.8: PR Controller - Currents waveform response THD analysis

After the PR controller tuning is performed, the voltage reference across the inductance is obtained. The grid voltage is then summed to compute the converter output voltage reference. The connection to the grid needs to implement a phase-locked-loop (PLL). The PLL implemented is designed based on the second-order generalized integrator (SOGI) technique [135]. A simpler implementation of the SOGI-PLL, called the Frequency-Fixed SOGI-PLL (FFSOGI-PLL) is carried out [136]. The block diagram of a FFSOGI System is shown in Fig. 4.9. The parameters for the FFSOGI are calculated in Appendix C. The damping factor $K = 2$, and for the PI block $K_P = 0.5$ and $K_I = 20$.

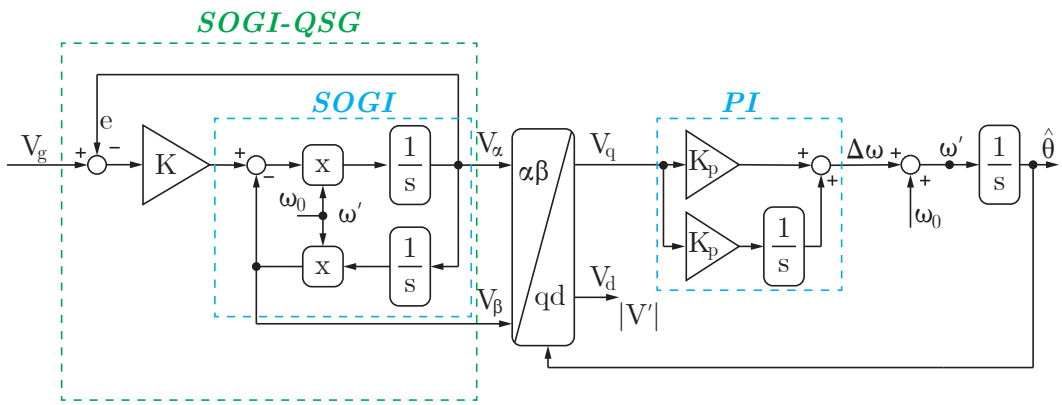


Figure 4.9: Block Diagram of a conventional FFSOGI-PLL

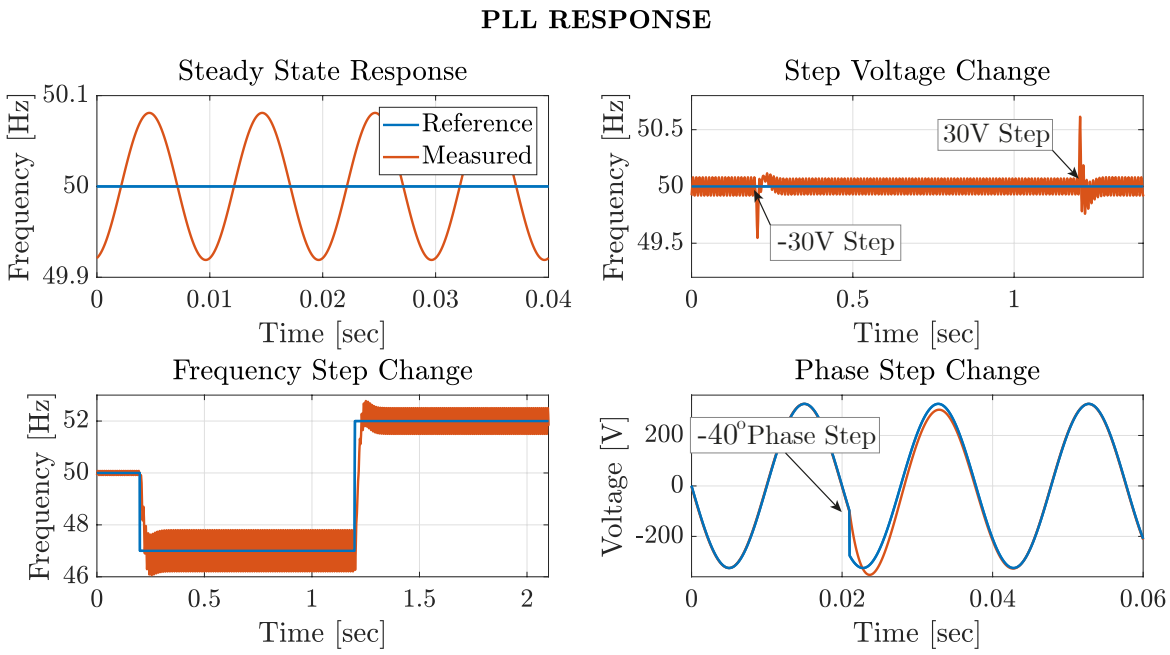


Figure 4.10: PLL controller response against fast changes in amplitude, frequency and phase angle. The designed PLL rejects disturbances

The PLL response is shown in Fig. 4.10. The PLL performance has been tested with voltage, frequency and phase shift step changes. First, the grid voltage is 230 V and 50 Hz. Then, a step change of -30 V, -3 Hz,+2 Hz and -40° in the amplitude, frequency and phase angle are applied. The response is shown in Fig. 4.10. The same experiments were carried out as in [135]. The steady-state following reference frequency is achieved in each case in less than 2.5 fundamental cycles, proving disturbances rejection and robust performance of the PLL response.

4.2 Battery Energy Management System

This section introduces the different battery management techniques proposed. At first, assumptions and previous information are detailed to set the basis of the later proposed strategies. Then, the active balancing technique proposed is described. Finally, three control strategies are exposed.

One main utilization for second-life battery systems could be either for residential applications or to support the grid. In both cases, BESS can be utilized to supply the power required when other energy sources are limited, e.g. PV systems.

The utilization of second-life batteries has the drawback of different initial conditions, i.e. rated voltage, capacity, SOH, etc [137]. In the literature, it is mainly proposed to apply SOC balancing algorithms [138], [139]. Also, specifically for second-life battery systems applications as in [110]. In this work, it is of most interest the State of Energy (SOE) of each battery. Therefore, strategies based on the energy remaining are mainly proposed.

The principle of operation is now presented.

1. Principles of Operation
   - The CHB needs to deliver the power requested by the grid, if possible.
   - The power can be distributed among the cells.
2. Constraints
   - The DC input voltage to the CHB needs to be higher than a certain value to inject power to the grid.
   - The SOC of each battery needs to be within a lower and upper limits, i.e., SOC_l, SOC_u

The power is requested from the grid. The BEMS needs to distribute the commanded power for each cell, taking into account different parameters. The RMS output voltage of the CHB needs to be higher than a specific limit when connecting to the grid to inject power. As the SOC is directly related to the OCV of the batteries. The SOC can be adjusted by adequately charging and discharging the batteries and, therefore, the input DC-link voltage to the CHB. An active balancing technique has been proposed to recirculate current among the cells so that (4.8) is fulfilled.

$$\sum_{k=1}^{h} V_{batt}^{k} \geq V_{lim} \tag{4.8}$$

Being $h \leq n$ the number of batteries that can be connected to deliver power out of the total n batteries.

In this work, some assumptions are made to narrow the project's scope. It is assumed that the power losses across the filters and converters are neglected compared to the power level of the demand, therefore:

$$P_{out} = P_{in} \tag{4.9}$$

The input power to the system is calculated as the sum of power provided by the n individual battery modules:

$$P_{in} = \sum_{k=1}^{n} P_k \tag{4.10}$$

The power delivered by each individual cell is calculated as:

$$P_k = i_k \cdot V_{batt,k} \tag{4.11}$$

Furthermore, as explained in Section 2.6.1.1, the OCV is strongly dependent on the SOC, i.e. $OCV_k = f(SOC_k)$, and

$$SOC_k(t) = SOC_{0,k}(t) \pm \frac{1}{C_k} \int_{t_0}^{t} i_k(\tau) d\tau \tag{4.12}$$

and solving the integral,

$$SOC_k(t) = SOC_{0,k}(t) \pm \frac{\Delta t \cdot i_k(t) \cdot \eta_k}{C_k} \tag{4.13}$$

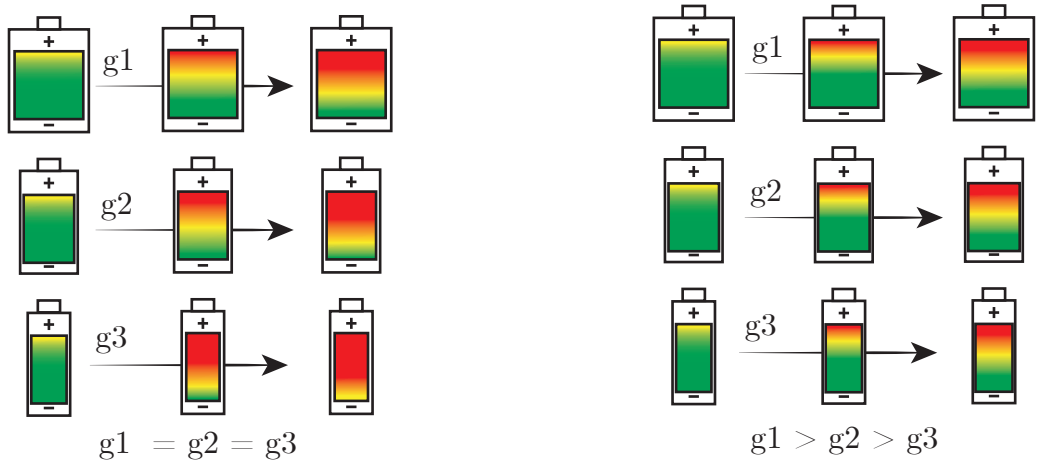
Being η the Ampere-Hour counting efficiency and C_k the battery capacity. It is assumed that $\eta = 1$ and that the battery capacity is different to each other with a difference of 20% to emulate second-life batteries with different SOH or battery suppliers [137], [140].

From a practical point of view, capacity and current delivered by the batteries may become less important to the amount of power remaining in the battery and the power delivered. Therefore, the State of Energy (SOE) is defined as:

$$SOE(t) = SOE(t_0) \pm \frac{1}{E_N} \int_{t_0}^{t} P(\tau) d\tau \tag{4.14}$$

In which $SOE(t)$ is the SOE at a specific moment in time and $SOE(t_0)$ is the initial SOE; E_N is the nominal energy capacity ([Wh]), and P is the power delivered by the battery. It should be noticed that the value of P may change over time. If the battery current is kept to be positive constant, the power delivered will decrease over time as the battery voltage will decrease with the SOC of the battery. Otherwise, the current needs to be increased to keep the battery delivery power constant. In this project, as the working points in the SOC curve are between 80% to 20-30%, it is assumed that the battery terminal voltage does not change significantly. Therefore the power does not decrease significantly over time and no further actions need to be taken. If all batteries in the system deliver the same amount of power, not taking into account the actual SOE, the batteries with less energy will discharge faster than the ones with greater energy remaining, as can be seen in Fig. 4.11a. In this way, the DC-link voltage supplying the CHB can become less than the limit.

The batteries with a larger amount of energy remaining are utilized more than the ones with less energy remaining, as illustrated in Fig. 4.11b. It is proposed in [141], [142] that one method to operate the system could be utilizing LS-PWM, by shifting the carriers of the PWM modulator appropriately to discharge the more charged batteries, taking advantage of the uneven power distribution inherent in the LS-PWM, as explained in Section 2.5.



(a) Equal gains.
Batteries discharge at different rates.

(b) Adjusted gains.
Batteries discharge at same rate.

Figure 4.11: Battery discharging dependent on SOE and capacity visual representation

The variable which is utilized to drive the cells in the CHB is the modulation signal. The BEMS unit is responsible for adjusting the modulation signals with a power distribution factor (also called "gains" for simplicity) to distribute the power among the cells efficiently. Therefore, the modulation index for each H-Bridge converter in the CHB can be defined as:

$$m_k = \frac{V_L^{ref} \cdot g_k}{V_{c,k}} \tag{4.15}$$

In which m_k is the final modulation index driving the PWM for the converter k, g_k is the gain related to BEMS Strategy utilized, and $V_{c,k}$ is the input DC voltage to the H-Bridge k. It is proposed in the literature to obtain such gain by considering the SOC and the power delivered by each battery module [120]–[122].

4.2.1 Active Balancing Technique

An active balancing technique has also been implemented. In commercial applications, it is recommended to utilize the battery in the mid-SOC range, from 20% to 80% of the SOC [143]. Further, as described before, in applications where the DC-link voltage is critical, being able to modify the SOC of a battery widens the control possibilities. Then, if the batteries can still reach the condition (4.8), it is still possible to provide power to the grid. If the DC-link voltage built up with only some batteries is higher than a specific limit, it is possible to utilize those batteries to charge those not used.

The battery charged, i.e. the battery that has reached the end of the mid-SOC range, increases the OCV, and, therefore, returns to the mid-SOC range, as illustrated in Fig. 4.12. The process active balancing process is carried out by modifying the modulation signals driving each cell of the CHB. Fig. 4.13 shows a diagram of the active balancing technique process.

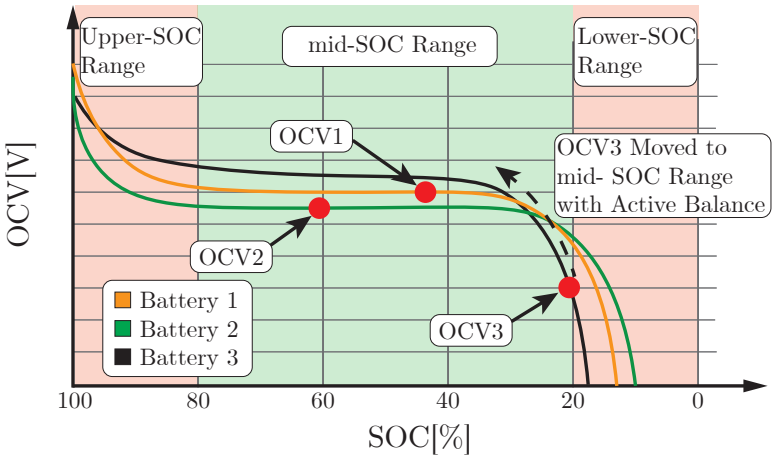
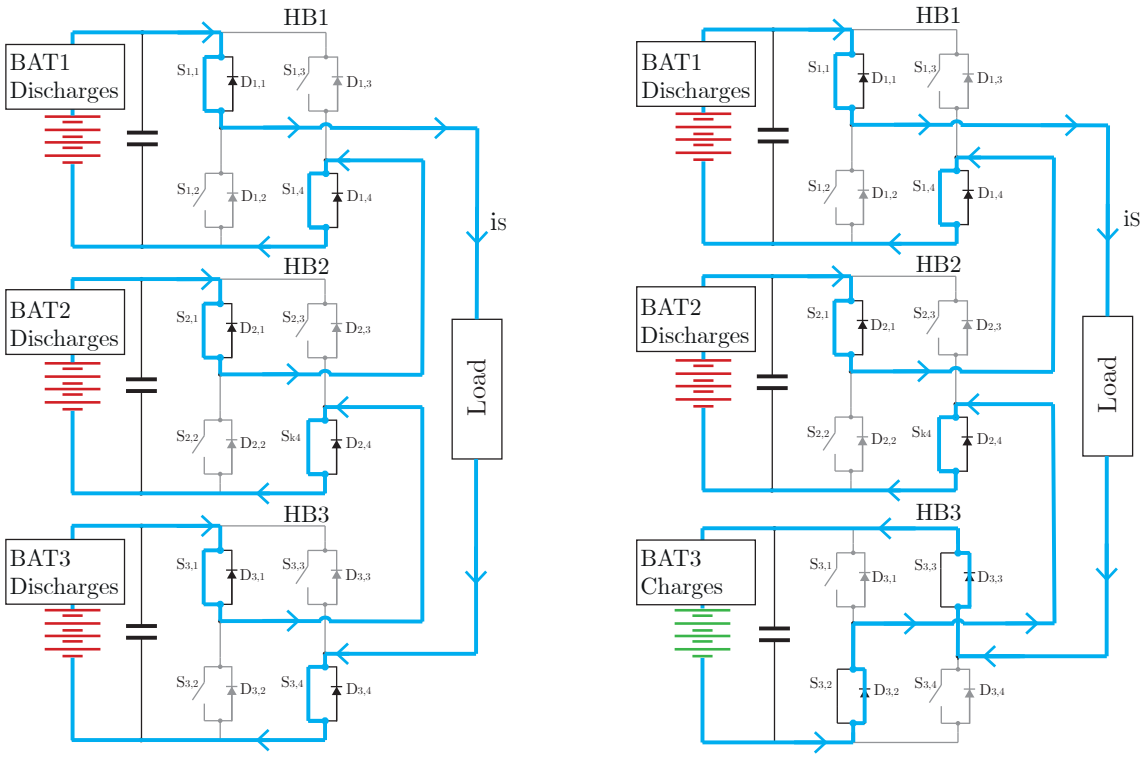


Figure 4.12: Exemplification of active balancing technique in a three-battery system. Battery 3 returns to the mid-SOC range after being charged from batteries one and two.



(a) Discharging (b) Charging

Figure 4.13: Schematic Active Balancing Technique. In the discharge process modulation signals are in phase. In the charge process the modulation signal of the battery to be charged is reversed. Only P states for positive current are shown.

The current controller output a voltage reference needed to obtain the reference current in the inductance. This voltage reference is then shared across the cells producing the modulation signals. These modulation signals can have different amplitudes depending on the DC-link voltages of each cell, but all are in phase. Therefore, by reversing the modulation signals of the HB connected to the battery to be charged, it is possible to charge and discharge the batteries independently.

Then, two new variables are presented for the rate of charge-discharge of the batteries, R_{ch} and R_{dch}, respectively, depending on the excess of voltage available in the most charged batteries.

$$\begin{cases} R_{ch} = & -\dfrac{\sum_{k=1}^{h} V_{c,k} - V_{lim}}{V_{lim}} \\ R_{dch} = & \dfrac{1 + R_{ch}}{h} \end{cases} \tag{4.16}$$

By utilizing (4.16), the remaining voltage available in the h batteries, which can still inject power to the load, is used to charge the remaining batteries, i.e. $k - h$ batteries. The gain driving each cell in the CHB is multiplied by the rate of charge and discharge in (4.16). Figure 4.14 shows the output modulation signals when all cells have the same input DC-link voltage of 120V and a DC voltage limit of 200V, which utilizing (4.16) yields to a charge rate factor of $R_{ch} = -0.2$ for one battery and a discharge rate factor of $R_{dch} = 0.6$. This is later proven in the laboratory, as shown in Section 5.4.

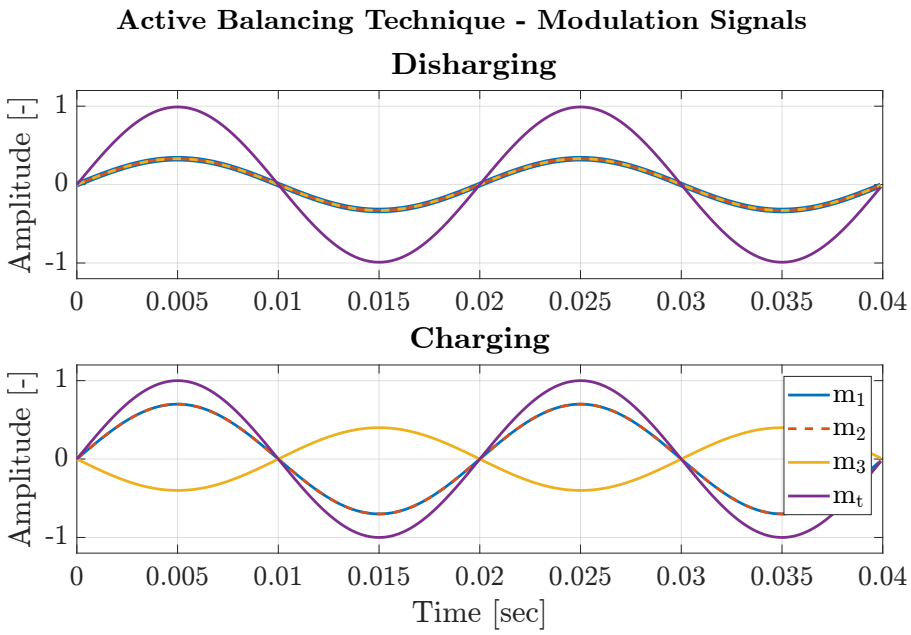


Figure 4.14: Active Balancing Technique - Modulation signals in the balancing process. When all cells discharge, the modulation index is equally among the cells. When one of the cells is charging, the modulation index is inverse and decreased in amplitude and the rest increase the amplitude so the sum is equal to one.

The amplitude of the modulation signals when recirculating current needs to be adjusted in order not to distort the output current quality greater than certain limits. The quality of the output voltage is reduced because of the reduced levels when reversing the modulation signal of the charged battery.

For the modulation signals described by Fig. 4.14, the voltage THD at the output of the converter has increased from 50% to 85%. In Fig. 4.13, the number of levels is reduced from seven level in Fig. 4.13a to five level in Fig. 4.13b. Taking into consideration Fig. 2.15 in Section 2.5.3, in which it was shown that the THD is greatly reduced with the increased number of levels, this technique could be more beneficial in high multilevel systems, where reducing the number of levels does not affect as much as in lower levels systems. A balance between charging-discharging rate and output quality has not being carried out in this work. Further, this technique reflects the advantages of utilizing distributed power electronics for battery energy storage systems, as each battery can be utilized independently.

4.2.2 System Downscale

The active balancing technique is implemented in the simulations in the following proposed strategies. Active balancing has not been proven for all cells in laboratory work due to hardware limitations. When simulating the system of three batteries, the initial conditions are shown in Table 4.1.

Battery	**Capacity [Ah]**	**Initial SOC [%]**	**Initial SOE [%]**
1 (Top Battery)	1.2	80	80
2 (Middle Battery)	1.0	75	75
3 (Bottom Battery)	0.8	70	70

Table 4.1: Batteries simulation conditions

As explained before, EV second-life batteries can have very different rated voltage, capacity and SOH. These batteries can have a capacity of around 120Ah (taking as an example the BMW i3 Rex model [144]). As can be seen in Table 4.1, batteries are tested for capacities around 1Ah, as the main purpose of this work is to test and evaluate the performance of the proposed strategies. Further, the simulations presented for the strategies proposed are described in Fig. 4.15. The input OCV is the one as shown Fig. 2.20 for the battery pack voltage.

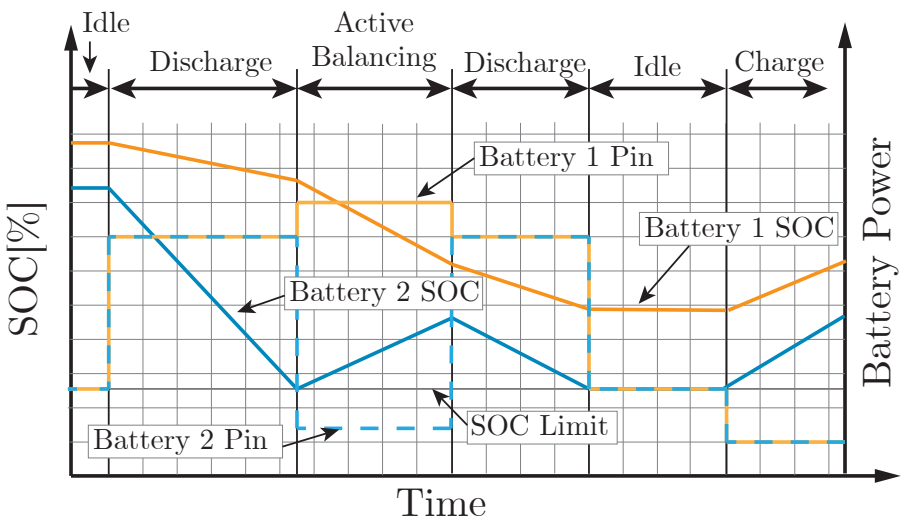


Figure 4.15: Simulation generic description for the simulations carried out in the following proposed strategies

Figure 4.15 describes a generic experiment in which first the system begins with null power delivery. Then, the discharge process starts. When one battery reaches the SOC limit, it is charged utilizing the active balancing technique described in Section 4.2.1. Then, when the batteries are discharged again, and it is no longer possible to deliver power, the system is set to an idle state in which no power is delivered nor requested. Finally batteries are charged from the grid. In the charge process, in the simulations, all batteries are charged with the same amount of power.

4.2.3 BEMS Strategies Proposed

The required power to inject into the load or grid is delivered by the input batteries connected to the CHB. Utilizing this topology makes it possible to distribute the power evenly or unevenly across the cells. Therefore, the possibilities for charging and discharging the batteries are widened. In this work, three strategies are proposed to operate the system. The first one is Equal Distribution (ED). This technique distributes the power equally among the cells. Secondly, the SOE Balancing (SOEB) technique is proposed to discharge the batteries unevenly, depending on their SOE levels. Finally, a SOE Sorting (SOES) algorithm is proposed based on an optimization problem and on the batteries SOE levels.

4.2.3.1 Strategy ED: Equal Distribution

The first strategy is based on the equal power distribution among the cells. A low computational burden is achieved by equalizing the power delivered by the batteries. Moreover, no need to estimate the SOE is required. On the other hand, it can lead to not optimal operation. The voltage reference to produce the output reference current is divided by the battery's cell voltage and then is split equally among the cells, as shown in Fig. 4.16. The gains, i.e. the power distribution factors, are equal to $1/k$ for a CHB with k cells; in this case, $k = 3$.

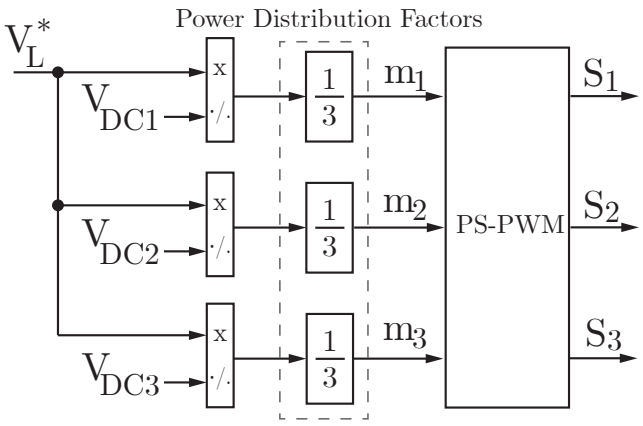


Figure 4.16: Strategy ED - Equal distribution power distribution factor schematic implementation.

First, it is shown in Fig. 4.17 and 4.18a the SOE and SOC of the three batteries. The total power reference is of 1800W, and as this strategy distributes equally the power among the cells, battery three is discharged the fastest, whereas battery one is discharged the slowest.

Further, it can also be seen that at time $t \approx 12$ min, battery three reaches the SOC lowest limit, i.e. 30% for these simulations,as shown in Fig. 4.18a. At that moment, the active balancing technique starts to act, charging battery three. Because they must supply the requested power to the grid as well as the power delivered to battery three, batteries one and two begin to deliver additional power. A steeper curve can see this in the SOE and the SOC curves of batteries one and two. Finally, when battery three SOC reaches one of the other batteries SOC, the charging process finishes, and the three batteries are then utilized to supply power to the grid. The power is delivered until $t \approx 17$ min. After that time, batteries can no longer deliver power to the grid, and the system waits until it is possible to charge the batteries from the grid. At $t = 20$ min, the system starts requesting power from the grid. Figure 4.17 and 4.18a show how the SOE and SOC start to increase from $t = 20$ min. Further, in the charging process happens the same as in the discharging process; battery three is charged the fastest, whereas battery one is charged the slowest, as the input power is distributed equally among the cells. Finally, Fig. 4.17 and 4.18a show one drawback of this technique: the smallest battery suffers more charged and discharged cycles between the upper and lower limit as it is discharged and charged faster. This repeated behaviour may decrease the SOH of battery three faster than for batteries one and two in prolonged operation over time.

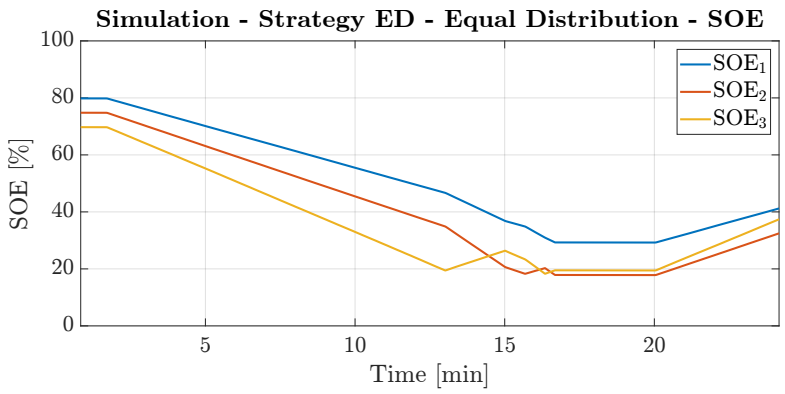
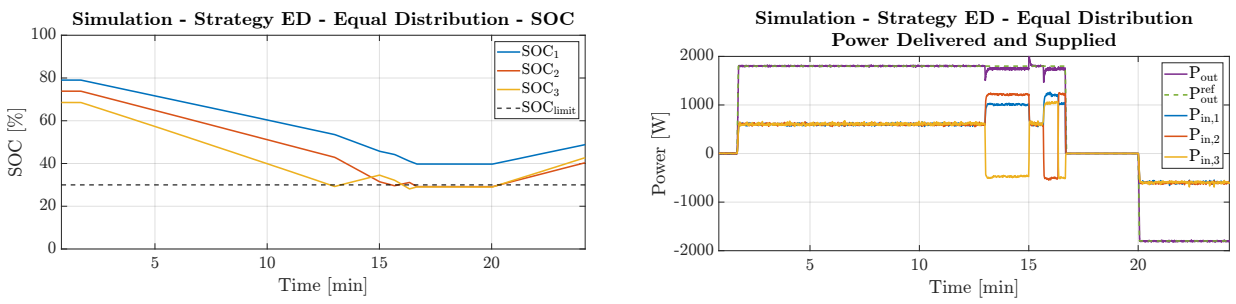


Figure 4.17: Simulation - Strategy ED - Equal distribution - SOE

In Fig. 4.18b, it can be seen the power commanded to the system, first to deliver power from $t \approx 2min$ until batteries are completely discharged at $t \approx 17$ min. Then, at $t = 20$ min, the power reference is negative to charge the batteries.



(a) SOC

(b) Power delivered by CHB and supplied by batteries

Figure 4.18: Simulation - Strategy ED - Equal distribution - SOC and power distribution

4.2.3.2 Strategy SOEB: SOE Balancing

The second BEMS strategy is based on utilizing different state estimation parameters to operate the system. Two main sub-strategies arise, (1) SOE balancing and (2) SOC balancing. In this work, it is most important the SOE balancing. The power is distributed so that the batteries with the highest SOE are utilized more than the ones with least SOE. The power distribution is implemented as in Fig. 4.19.

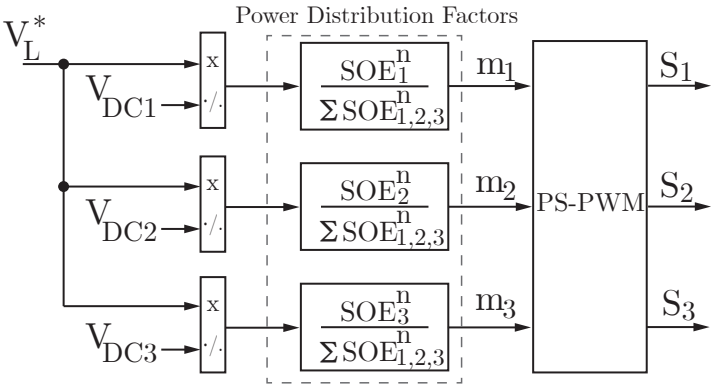


Figure 4.19: Strategy SOEB - SOE Balancing power distribution factors schematic implementation

For a system with k cells, the gains or power distribution factors are calculated as in (4.17) in the discharging process.

$$g_k^{discharge}(SOE) = \frac{SOE_k^n(t)}{\sum_{k=1}^{n} SOE_k^n(t)} \tag{4.17}$$

For the charging process, it can be similarly expressed as in (4.18), which variation can also be found in [110], but which has not been included in the simulations.

$$g_k^{charge}(SOE) = \frac{(1 - SOE_k^n(t))}{\sum_{k=1}^{n}(1 - SOE_k^n(t))} \tag{4.18}$$

It should also be noted that the super-index n is utilized to accelerate the balancing process, as proposed in [145] for a SOC balancing algorithm. For the same difference in SOE among the cells, the greater the value of n, the greater the difference is magnified.

From (4.17), it can be deducted that in order not to have overmodulation, the sum of all gains needs to be equal to one. It can be seen in Fig. 4.20 that with an exponent of $n = 1$, the system is not able to balance the SOE among the cells. Compared to strategy ED before, it can be seen that, even though the same SOE is not achieved, batteries are discharged at a similar rate. Battery three reaches its lowest SOC limit at $t \approx 15$ min, i.e. 3 min after it did in the strategy ED. As in strategy ED explained before, battery three is charged with batteries one and two, due to the active balancing technique. Finally, the SOE is balanced at the very end of the discharge process, as all batteries reach the lowest limit at the same time. At $t = 20$ min, batteries are charged from the grid.

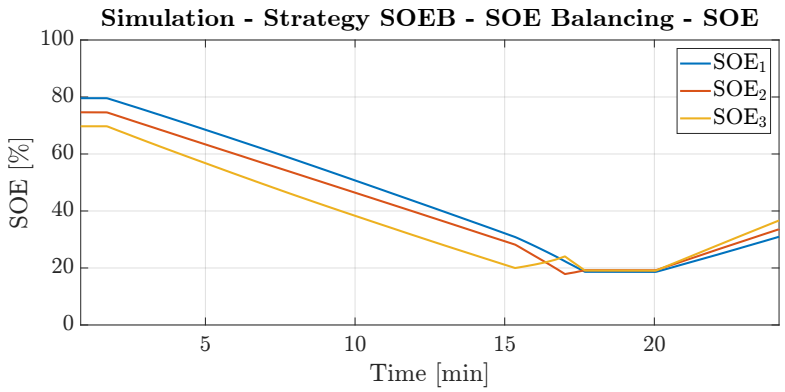
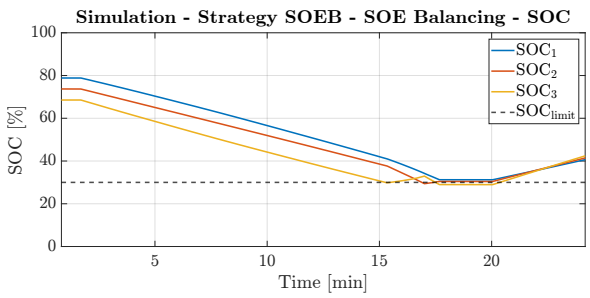
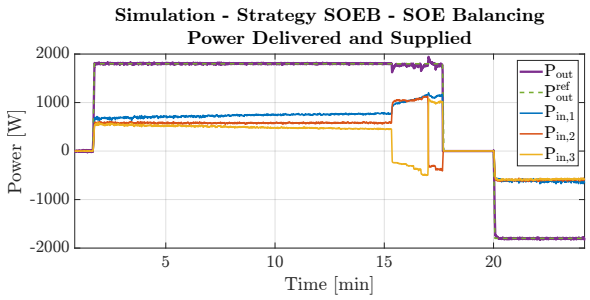


Figure 4.20: Simulation - Strategy SOEB - SOE Balancing $n = 1$ - SOE

Gains are computed continuously over time, causing the batteries to distribute the power continuously; as seen in Fig. 4.21b, battery one delivers most of the power and keeps increasing as the SOE is not balanced.



(a) SOC



(b) Power delivered by CHB and supplied by batteries

Figure 4.21: Simulation - Strategy SOEB - SOE Balancing $n = 1$ - SOC and power distribution

Furthermore, the differences in SOE have been computed to verify the balancing. It can be seen in Fig. 4.22 that the greater the value of n, the faster the balanced process is completed. It can be seen that the active balancing technique start at $t \approx 16$ min. Then, the difference in SOE is reduced, as one battery is charged will the others are discharged, approaching equal SOE. It should also be noted that, the final value at which the differences in SOE are constant, depends on how was the SOE levels when the system can no longer inject power to the grid, either because the SOC reached the limits or because the voltage in the DC side is no longer higher than the limit value.

Note that the sum of the differences in SOE is defined as:

$$\sum \Delta SOE = |SOE_1 - SOE_2| + |SOE_1 - SOE_3| + |SOE_2 - SOE_3| \tag{4.19}$$

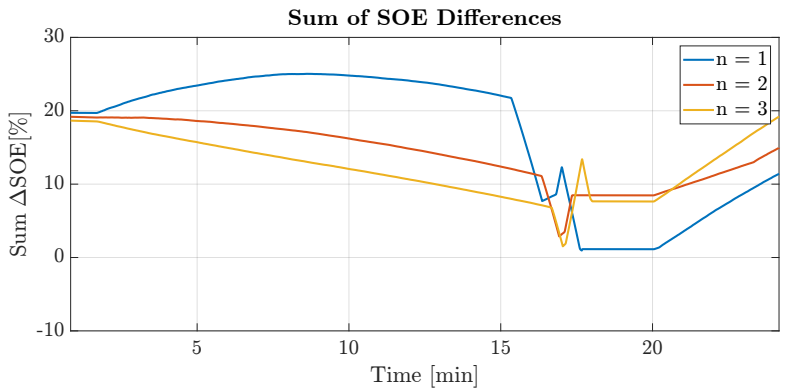


Figure 4.22: Strategy SOES: Sum of Differences in State of Energy dependent on n.

4.2.3.3 Strategy SOES: SOE Sorting

The last control strategy for the BEMS is based on the principle that the grid request a certain amount of power for the longest time possible. This is of particular interest in residential applications to supply power to the house loads when, for example, the grid price is especially high at a certain moment in time. This strategy name has also been proposed by [146] simultaneously to this work, based on SOC balancing algorithms. In [141], [142], a sorting algorithm is presented, based on level-shifted PWM for SOC balancing taking advantage of the uneven power distribution inherent in the LS-PWM technique. In this work, a sorting algorithm is based on the battery's SOE with PS-PWM technique.

The following optimization problem can be formulated:

$$
\begin{aligned}
&\textbf{if} && \sum_{k=1}^{n} Vcaps,k && \leq V_{lim} \Longrightarrow g_k = 0\ , k = 1, \ldots, n. \\
&\textbf{else}\{ \\
&\quad \underset{g_k}{\text{maximize}} && t_s(g_k) && = \sum_{k=1}^{n} g_k \cdot SOE_k \\
&\quad \text{subject to} \\
&\qquad && \sum_{k=1}^{n} g_k && = 1 \qquad . \\
&\qquad && g_k && \leq 1,\ k = 1, \ldots, n. \\
&\qquad && \Delta g_{j,k} && \leq \delta_g,\ j, k = 1, \ldots, n, j \neq k. \qquad \}
\end{aligned}
\tag{4.20}
$$

The gains will change by computing the above optimization problem because it will always utilize the battery with more remaining energy. It is shown in Fig. 4.23 how the implementation is carried out.

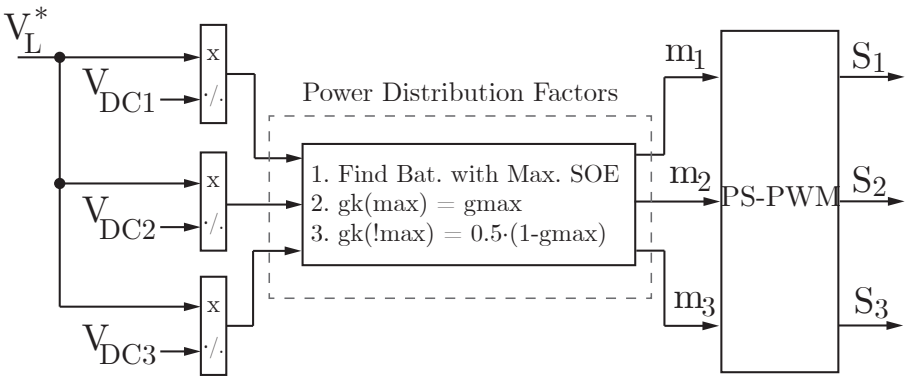


Figure 4.23: Strategy SOES - SOE Sorting power distribution factors schematic implementation for the discharging process. In the charging process, the same can be applief by subtituting 'max' by 'min'.

To reduce the computational burden, only once in a while the optimization problem is computed, i.e. the rate of updates in the power distribution factors can be limited. As the fundamental grid frequency is 50 Hz or 20 ms, the action period for the gain to be updated is 100 times bigger, that is, 2 s. This periodical action also reduces the number of step changes in the load. As none of the constraints is quadratic or cubic, the optimal solution will always be on the vertex of a parallelogram, as illustrated in Fig. 4.24.

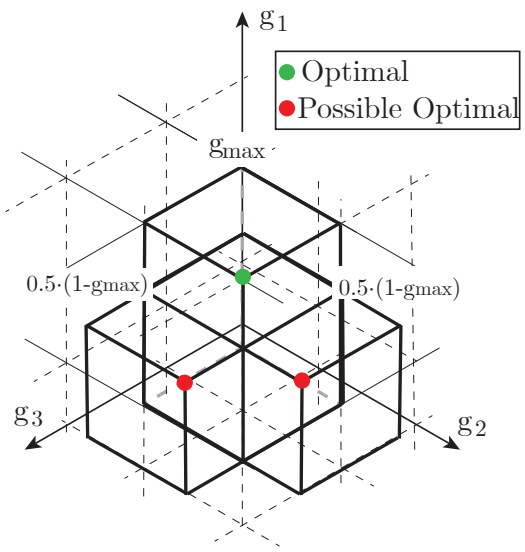


Figure 4.24: Strategy SOES- SOE Sorting. Optimal Solutions to problem formulation in (4.20) jump between vertex of the given parallelogram.

The optimal point will jump between adjacent vertex if the sign of the difference between the remaining energy in the batteries changes. From a practical point of view, this strategy is equivalent to using the battery pack with the highest SOE and least the one with the lowest SOE; for example, having $g_1 = 0.6$, $g_2 = 0.2$ and $g_3 = 0.2$, accomplishing with the constraint expressed in the optimization problem. In fact, the sorting algorithm could be further explored to compute intermediate gains, e.g. $g_1 = 0.6$, $g_2 = 0.3$ and $g_3 = 0.1$, but has not being tested in this work.

It is shown in Fig. 4.25 that this strategy effectively balances the SOE among the batteries. The simulation presented here is modelled by applying a gain of $g = 0.6$ to the module with the highest SOE and $g = 0.2$ to the others, accomplishing the constraint in the problem formulation.

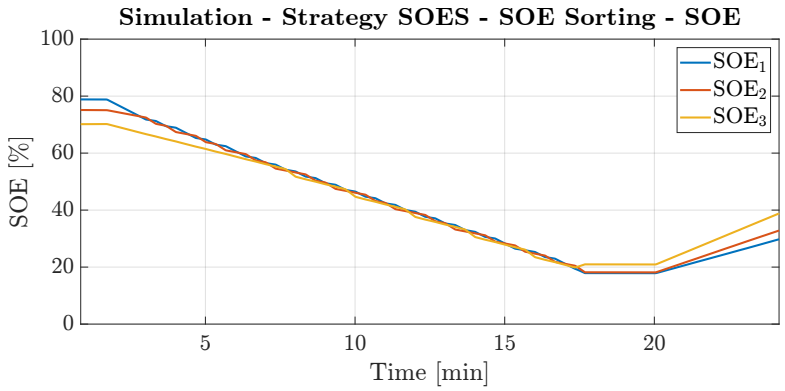
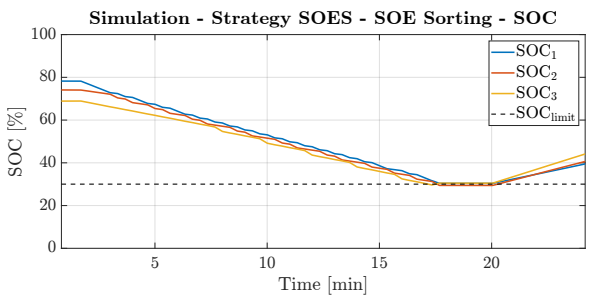
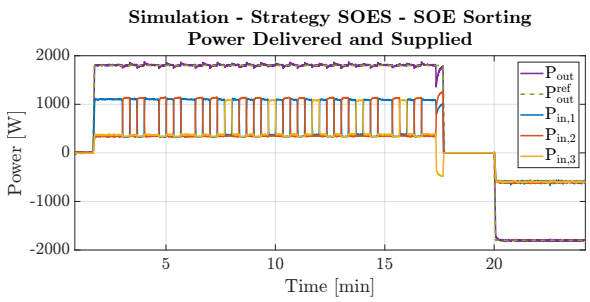


Figure 4.25: Simulation - Strategy SOEB - SOE Sorting $g_{max} = 0.6$ - SOE

It can be seen in Fig. 4.26b that the power delivered by each battery changes when the gain changes. Therefore, this strategy has the drawback of stepping the power delivered and, consequently, the current in the batteries. Furthermore, it can be seen that the output power presents some distortion due to the step changes in the input power.



(a) SOC



(b) Power delivered by CHB and supplied by batteries

Figure 4.26: Laboratory - Strategy SOES - SOE Sorting $g_{max} = 0.6$ - SOC and power distribution

The different strategies proposed are summed up in Table 4.2 with their respective advantages and disadvantages.

Table 4.2: Overview - Strategies proposed

Strategy	**Description**	**Advantages**	**Disadvantages**
[ED] Equal Distribution	Distribute power to deliver equally among the cells, independent of any parameter	Simple to implement. Low computational burden.	Does not efficiently distribute power. Reduce the time batteries can deliver power.
[$SOEB$] SOE Balancing	Continuously computing gains to achieve SOE balanced among the cells	Continuous update of power distribution factors. Depending on factor n, balancing can be achieved faster or slower. Increase time supplying power.	More complex to implement. High computational burden.
[$SOES$] SOE Sorting	Utilize greater the most charged battery	Effectively balance SOE among the cells. Increase time supplying power.	Step changes on current delivered by cells. Medium computational burden. Not efficient with high numbers of voltage levels. Output power can get distorted.

4.2.4 Impedance Determination

As explained in Section 2.6.1.4, the estimation of the battery parameters is very valuable for SOC and SOH estimation. The impedance determination is based on the measured battery voltage and current. It is shown in Section 2.6.1.4 that a proposed battery impedance estimation is based on a simplified linear model, but as discussed, it is not of great interest in second-life battery system, as it may not reflect the SOH degradation of the battery.

To solve this issue, it is more reliable to obtain a wide range of frequencies in the current and voltage measurements, to obtain a full view of the battery impedance estimation. A novel approach is proposed in this work. The idea relies on the distortion of the currents in the batteries by injecting a variable frequency signal into the modulation signals.The control technique implemented is shown in 4.27 based on the control scheme shown in Fig. 4.2. In principle, the modulation signals fundamental frequency is 50 Hz, which produces an AC current ripple of 100 Hz in the DC-link currents. By injecting a signal of frequency f_{EIS} to the modulation signals, the DC-link currents will be composed of a signal with frequencies of 50 Hz $\pm$ 2f_{EIS}. By computing a Fast Fourier Transformation (FFT) of the measured DC-link current and voltage, the impedance (4.21) can be estimated.

$$Z_{bat}(j\omega) = \frac{V_{bat}(j\omega)}{I_{bat}(j\omega)} \tag{4.21}$$

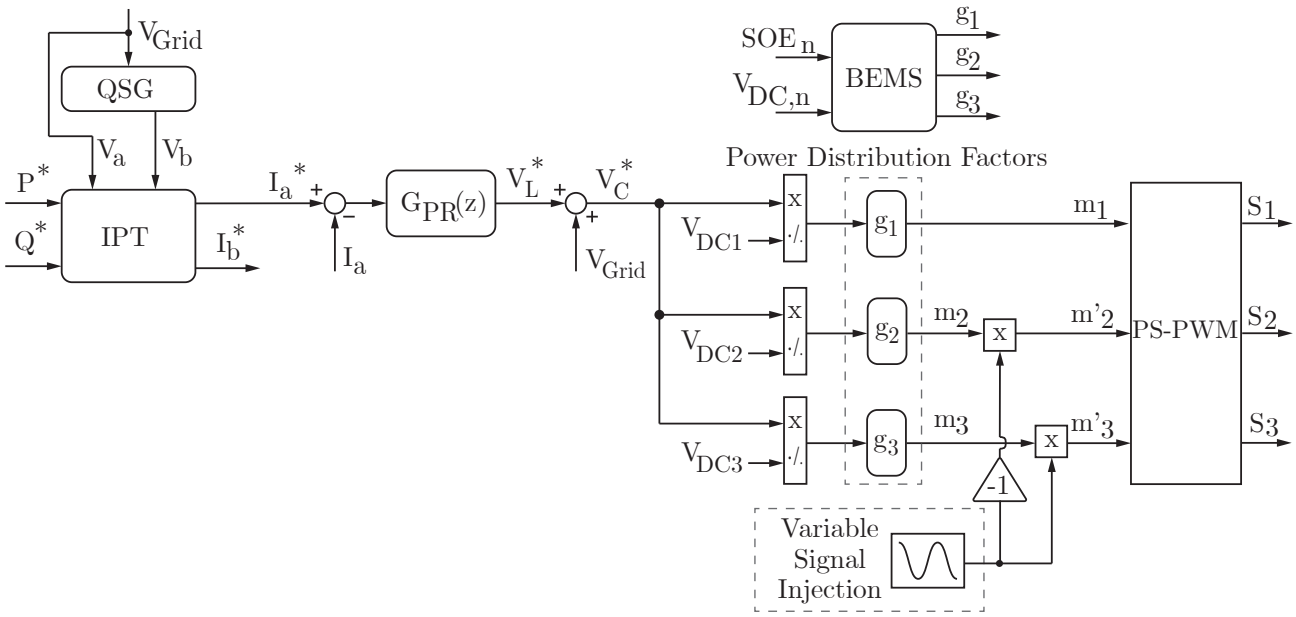


Figure 4.27: Control method based on the instantaneous power theory. A variable frequency signal is injected to the modulation signals.

The injected signal to the modulation signals is shown in Fig. 4.28. The amplitude of the modulation signals needs to be low enough compared to the modulation index in order not to distort the output current waveform significantly.

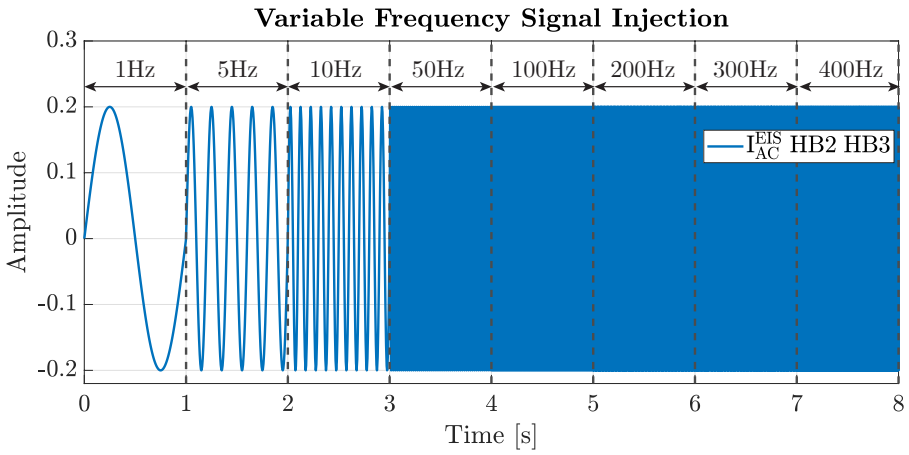


Figure 4.28: Injected current reference frequencies on top of fundamental frequency.

It is shown in Fig. 4.29 the zoom view of the modulation signals at $f_{EIS} = 400$ Hz, i.e. in the time range between 7 and 8 seconds.

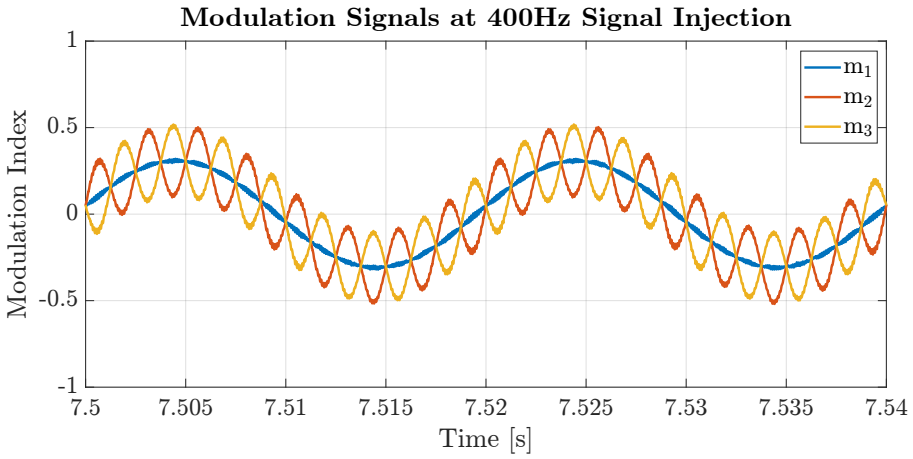
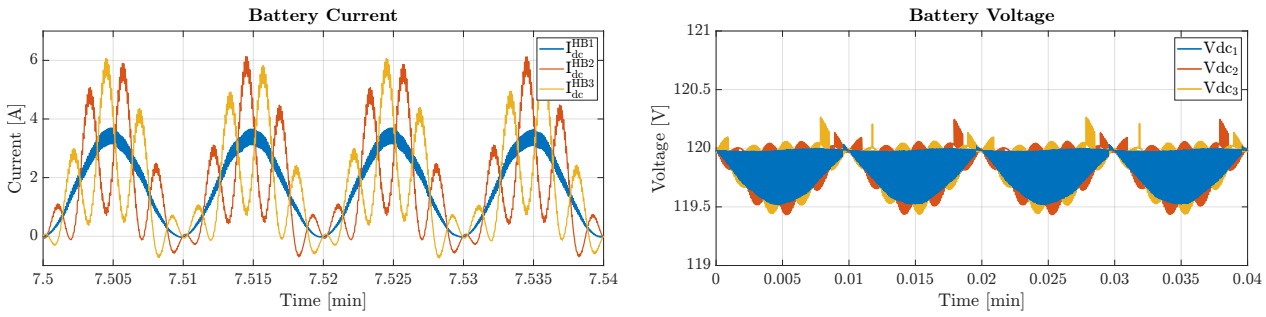


Figure 4.29: Simulation - Modulation signals after variable frequency signal injection - Zoom view at 400Hz.



(a) Battery Currents (b) Battery Voltage

Figure 4.30: Simulation - Battery currents and voltage with 400 Hz frequency injection. The amplitude and phase of the frequency of interest, the impedance spectroscopy can be estimated.

As can be seen, modulation signal m_1 has a fundamental frequency of 50 Hz, whereas m_2 and m_3 have frequencies of 50 Hz $\pm$ 400 Hz on top, producing the currents and voltages in the DC-link shown in Fig. 4.30 which contains signals with frequencies of 100 Hz $\pm$ 800 Hz.

The impedance can be estimated for the whole injected spectrum by applying an FFT analysis in each frequency range. The battery model utilized in this simulations is shown in Fig. 4.31, which parameters are taken from [52], omitting the effect of the SOC on the equivalent impedance parameters, as it is almost constant in the range 20%-80% of SOC, which is of main interest in this project. At very low frequencies, the injected signal can yield to inaccurate measurements, as the battery SOC will change over time, more significantly the smaller the injected signal frequency.

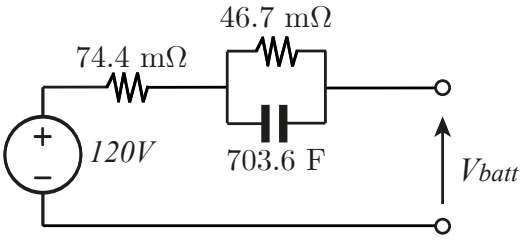


Figure 4.31: Injected current reference frequencies on top of fundamental frequency.

The impedance spectroscopy Nyquist plot shown in Fig. 4.32 shows the theoretical impedance values for frequencies between 1 mHz and 5 kHz. The values obtained from the simulations are not shown and left as future work. As can be seen, the Nyquist plot only shows one semielipse, as only a single RC branch in the battery model was implemented as explained in Section 2.6.1.4.

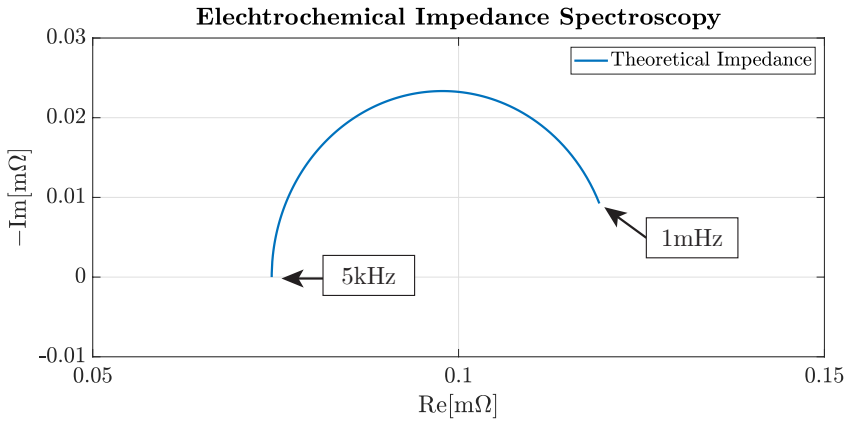


Figure 4.32: Impedance spectroscopy Nyquist plot. Frequencies vary from 5 kHz to 1 mHz. Only the semielipse corresponding to one RC-branch is obtained.

Chapter 5

Experimental Results

This chapter presents the resulting waveforms and data measured in the laboratory. First, the experimental setup is described. Secondly, fundamental experiments are shown to prove the seven-level output voltage, current control loop and PLL response. Then, different experiments are shown to prove the viability of the proposed control strategies with a passive load and a grid simulator at the CHB output. Later, the proposed active balancing technique is tested.

The laboratory setup is shown in Fig. 5.1. The setup was made at Aalborg university, department of AAU Energy, room PON105-3.119; a picture of the setup and a descriptive diagram can be seen in Fig. 5.1 and 5.2, respectively.

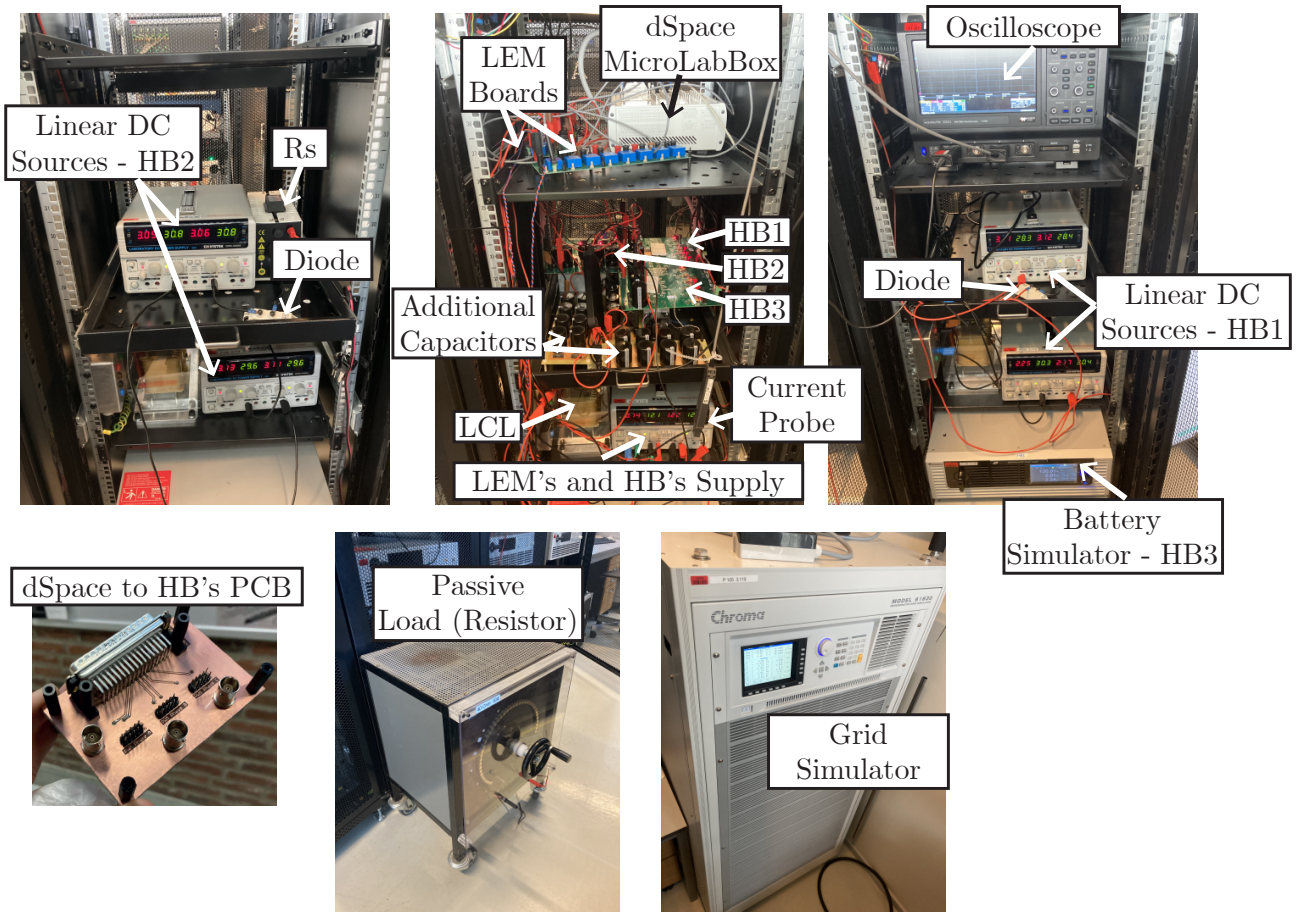


Figure 5.1: Laboratory - Picture of the setup. Three different cabinets where used to store the setup. Values for components and electrical diagram can be found in Fig. 5.2 and Table 5.1.

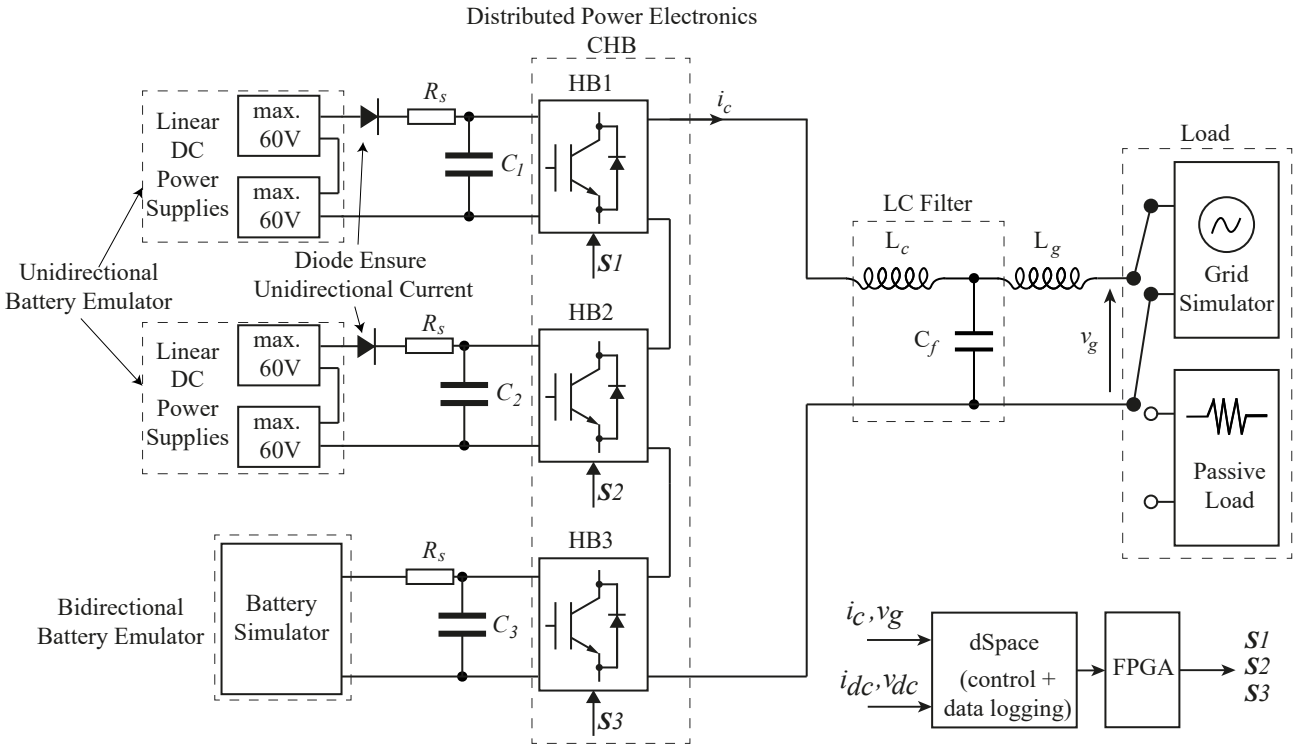


Figure 5.2: Laboratory - Schematic Setup. Four linear DC supplies for batteries one and two emulation. One battery simulator for battery three. Grid simulator or a passive resistor at the output can be placed.

The experimental setup data used in the laboratory is shown in Table 5.1.

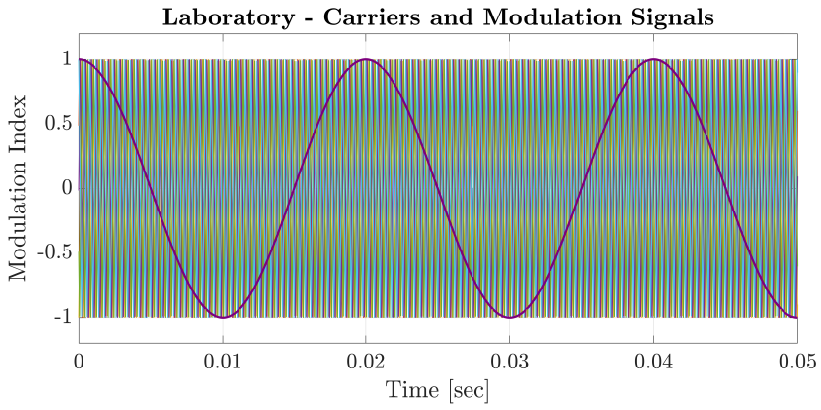
Table 5.1: Hardware parameters

Parameter	**Value**	**Description**
$V_{dc,max}^{HB1,2}$	60 V	Linear DC source Max. Voltage
$I_{dcmax}^{HB1,2}$	3 A	Linear DC source Max. Current
$V_{dc,max}^{HB3}$	600 V	Battery Simulator Max. DC Voltage
I_{dcmax}^{HB3}	±120 A	Battery Simulator Max. DC Current
C_{dc}	1.4 mF	Capacitor in the DC-link
L_c	4.8 mF	LCL Converter Side Inductance
C_f	5 μF	LCL Capacitor
L_g	1 mF	LCL Grid Side Inductance
R_{load}	40 Ω	Passive Load Max. Resistance
f_{sw}	2.8 kHz	Switching Frequency
f_s	25 kHz	Sampling Frequency

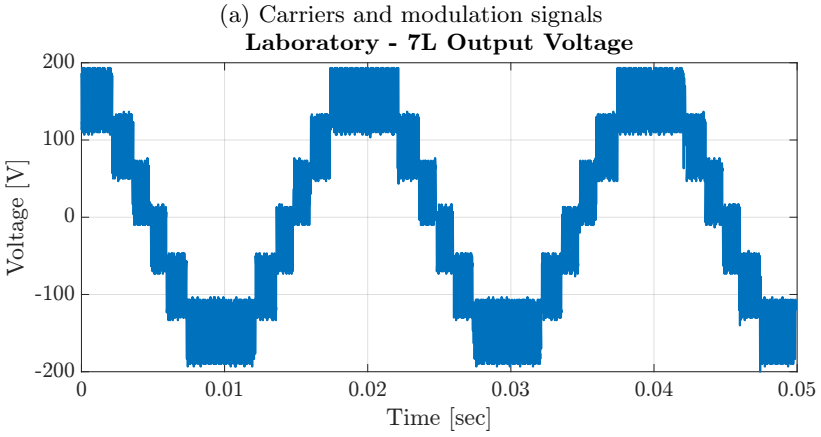
The CHB is controlled from a dSpace. The model is built and compiled utilizing Simulink®. The

individual converter's gate drivers are directed with a phase-shifted carrier PWM, and the comparison between modulation and carrier signals is made in the FPGA, described in Appendix B. It is shown in Fig. 5.3a the triangular waveforms and the modulation signals utilized to control the CHB. Two additional hardware components have been placed, shown in Fig. 5.2, i.e. two diodes in series with the linear DC voltage supplies, ensure that current cannot be injected into the DC supplies, which may damage the device. A resistor has been placed in series with the DC power supply. The resistor is used to reduce the current ripple and emulate the series resistance of the batteries.

The carrier frequency, i.e. the switching frequency is 2.8 kHz, and as PS-PWM is utilized, the effective switching frequency is 16.8 kHz, i.e. $2 \cdot H \cdot f_{sw}^{HB}$, being H the number of CHB modules, as described by (2.17). The sampling frequency is 25 kHz. The reference signal frequency, i.e. the fundamental frequency, is 50 Hz. The seven-level output voltage is shown in Fig. 5.3b, taken from the oscilloscope.



(a) Carriers and modulation signals



(b) CHB output voltage

Figure 5.3: Laboratory - Carrier and modulation signals from dSpace and Seven Level Output Voltage measured in the oscilloscope

5.1 Current Control Loop and PLL

To asses and tune the PLL controller parameters, an input from a signal generator was connected to the dSpace. Then, this signal was scaled to simulate the grid voltage. The response of the PLL against step changes in amplitude, frequency and phase angle, is shown in Fig. 5.4.

The obtained waveforms in the laboratory are similar to the designed and simulated response of the FFSOGI-PLL. The settling time against step changes is under 2.5 fundamental cycles.

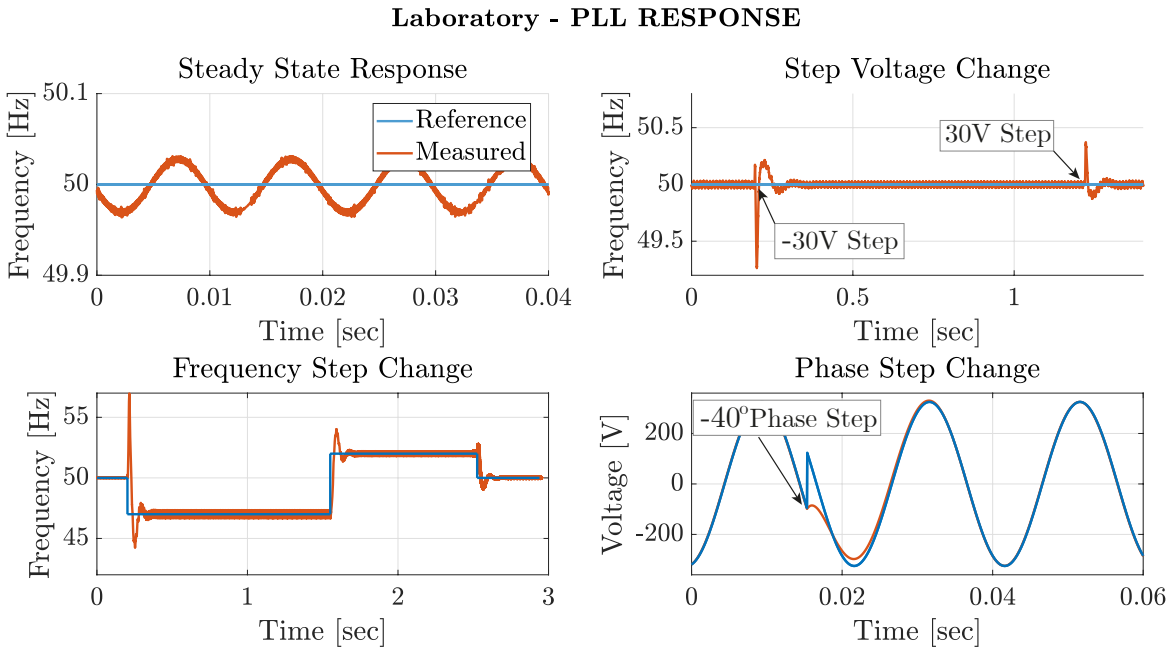


Figure 5.4: Laboratory - PLL response. Step changes in voltage amplitude, frequency and phase shift has been applied to test the robust design.

Then, after testing the PLL response, the current controller is tested. The current waveforms are shown in Fig. 5.5. A rate limiter is implemented in the laboratory to achieve full current in less than 2 ms. As can be seen,the overshoot is less than 5% fitting the theoretical and simulating results shown in Section 4.1.1.

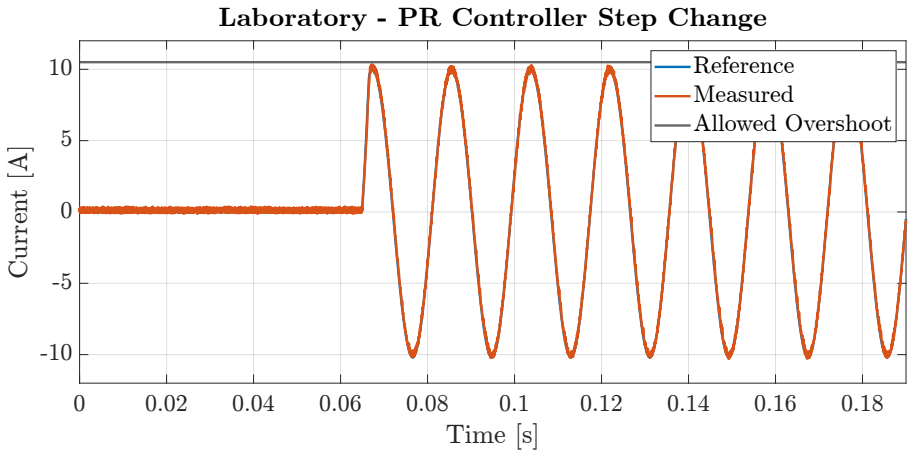


Figure 5.5: Laboratory - Current controller response

By importing the current signal to Simulink and performing THD analysis, the THD of the current is measured to be in the laboratory at around 2.7%, below the limit of 4.5% current THD for battery plants [134]. The FFT analysis of the current waveform is shown in Fig. 5.6. The harmonic content of the waveform accomplishes with the danish grid connection of battery plants [134].

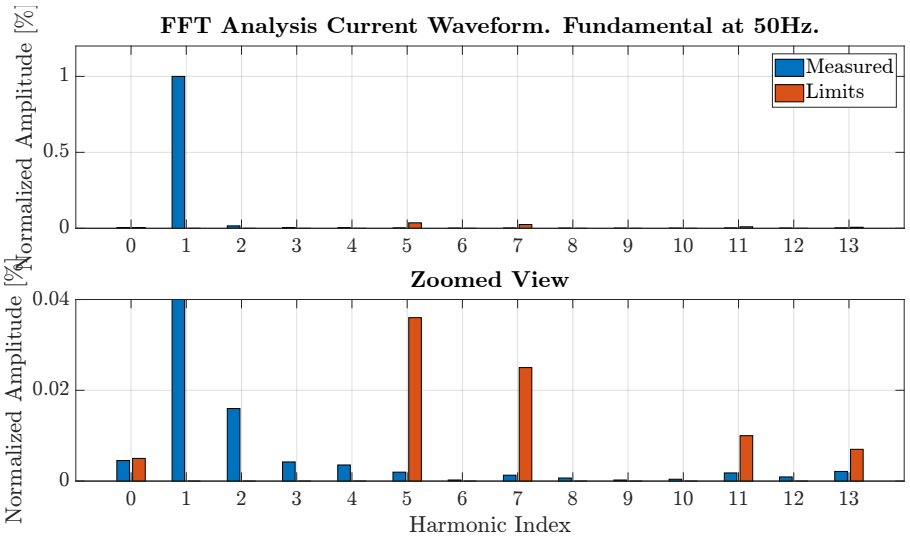


Figure 5.6: Laboratory - FFT analysis of the current controller response. Obtained values are below the standard limits for battery plants connection [134].

Once the previous stages were completed, the strategies were tested. At first, strategies are tested without an active balancing technique. Further, the power is dissipated in a passive load. Finally, the power dissipated is 180 W to analyze the performance for a longer time.

5.2 Strategies Proposed - Passive Load

At first, strategies are tested connected to a passive load. Then, the resistance value can be changed to modify the amount of power delivered. The resistance has been set to around 3 Ω; therefore, to have a peak current as in the simulations of around 11 A, the power reference is 180 W. The DC side voltage for all the cells is set to 120 V. In the worst-case scenario, if one battery needs to deliver all the power, the DC-link current would be 1.5 A on average, and it has been proven to stay within the DC source hardware limitations.

5.2.1 Strategy ED

The first strategy is based on equally distributing the power among the cells, regardless of the SOE level. It can be seen in Fig. 5.7 that the SOE and the SOC diverge in time due to the inherent unbalance in the battery parameters. The battery's initial SOE differs to emulate the practical behaviour of second-life batteries, as explained in Section 2.6.1.3. At first, the active balancing technique was not enabled. Therefore, as can be seen in Fig. 5.8b, power is distributed equally among the three cells. At $t \approx 63$ min, the power is distributed only between batteries one and two until $t \approx 83$ min when one battery is not able to deliver the power to the load. The output current THD is measured to be 2.7%.

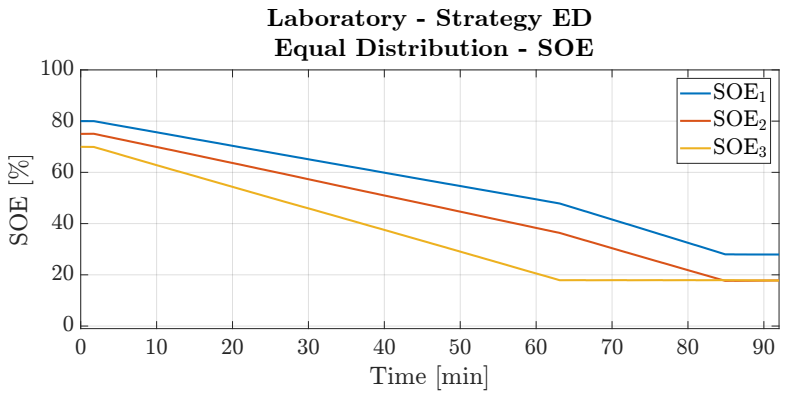
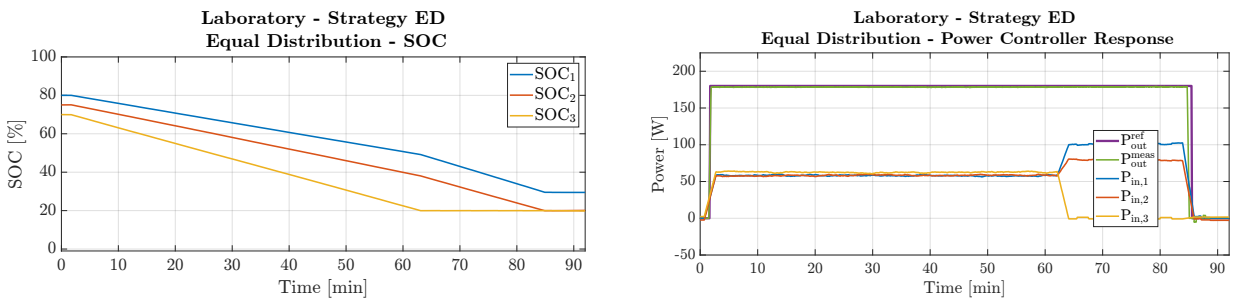


Figure 5.7: Laboratory - Strategy ED - Equal distribution - SOE and SOC

It can be observed in Fig. 5.8b that the power is distributed equally among the cells. The sum of the input power from the cells is around 190 W, whereas the active output power is approximately 175 W. The efficiency of the system is approximately 92.1%. When only batteries one and two are delivering power, it can be seen that battery one delivers more power than battery two. This is due to slightly different input DC voltages set in the laboratory.



(a) SOC

(b) Power delivered by CHB and supplied by batteries

Figure 5.8: Laboratory - Strategy ED - Equal distribution - SOC and power distribution

5.2.2 Strategy SOEB

The second strategy is based on the SOE balancing among the cells. In such a way, the batteries will try to balance in time to achieve the same relative remaining energy capacity. The gains applied are obtained by utilizing (5.1).

$$g_k(SOE) = \frac{SOE_k^n(t)}{\sum_{k=1}^{n} SOE_k^n(t)} \tag{5.1}$$

First, it can be seen in Fig. 5.9 that the SOE is balanced during the operation when applying a factor $n = 5$. It can be seen that the three batteries are discharged at the same rate, achieving the SOC lowest limit at the approximately same time, as the SOE is balanced across the cells.

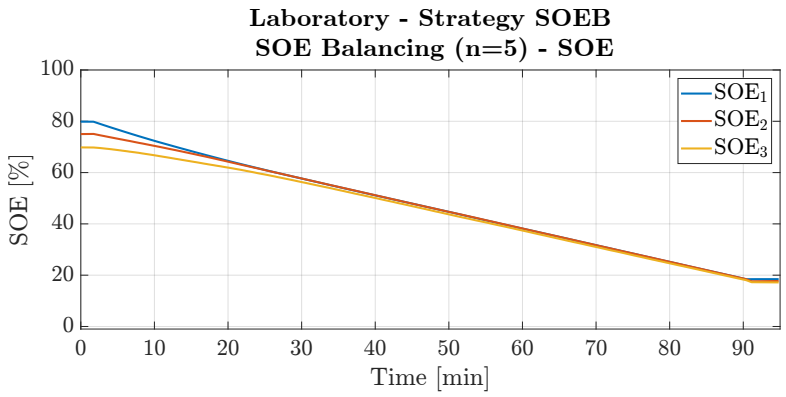
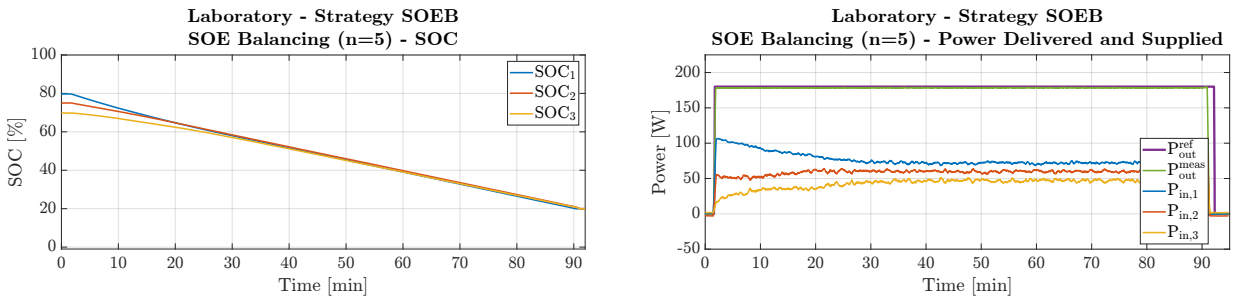


Figure 5.9: Laboratory - Strategy SOEB - SOE Balancing $n = 5$ - SOE

It can be observed in Fig. 5.10b that the power delivered by each of the batteries does not experience steps or fast changes, but smooth increases or decreases in the power delivered. The power delivered by the biggest battery, i.e. battery one, is higher than the smallest battery, i.e. battery three, to have the same discharge rate, as seen in the figure. Further, Fig. 5.10b shows that at the beginning, when the batteries are very different in SOE, power distribution diverges more but converges to almost the same value when the SOE is balanced. The current THD is measured to be 3.1% at 11 A peak current. Further, it should be noted that with strategy SOEB, the CHB can output up to seven-level for longer time, compared to the strategy ED, when only batteries one and two deliver power, producing only a five-level output voltage.



(a) SOC

(b) Power delivered by CHB and supplied by batteries

Figure 5.10: Laboratory - Strategy SOEB - SOE Balancing $n = 5$- SOC and power distributions

Furthermore, several experiments were carried out in the laboratory to verify the effectiveness of the factor n on the SOE balancing strategy. It has been proven with $n = 1, 2, 3, 5, 10$ and 50. It can be observed in Fig. 5.11 how the SOE balancing converges faster when n increases.

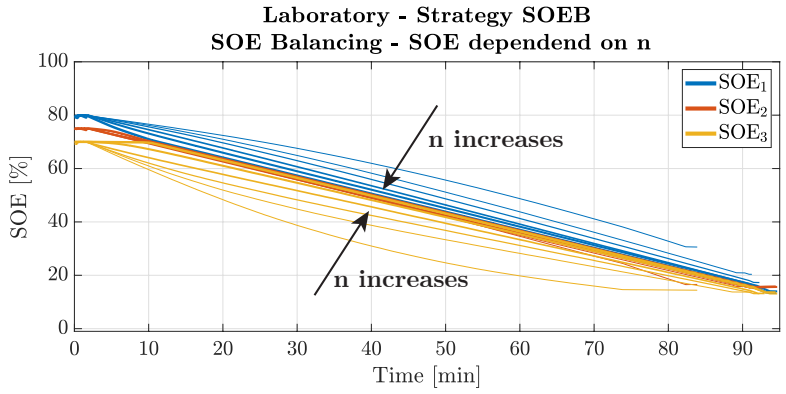


Figure 5.11: Laboratory - Strategy SOEB - SOE Balancing - SOE with increasing values for factor n

Moreover, as seen in the simulations, when the factor n is too small, the balancing strategy cannot balance the system.

5.2.3 Strategy SOES

The third strategy is based on the SOE sorting among the cells. The higher the SOE a battery has, the more it is utilized. The optimization problem is made according to the following steps:

1. Sort the batteries as a function of the SOE
2. Apply a gain g_{max} to the highest SOE battery
3. Apply $(1 - g_{max})/(h - 1)$ to the other batteries, being h the number of batteries that can deliver power.

Furthermore, in order not to step change the power delivered by the cells every switching cycle, the sorting algorithm is performed and updated every 2 minutes. It can be observed in Fig. 5.12 that this strategy effectively balances the SOE among the cells, as in strategy SOEB, but has the drawback of step changing the power delivered by the cells. In short, strategy SOES (SOE Sorting) balances the SOE discretely, whereas strategy SOEB (SOE Balancing) balances the SOE continuously. The following experiments were carried out with $g_{max} = 0.6$. The current THD was 2.9% at a peak current of 11 A.

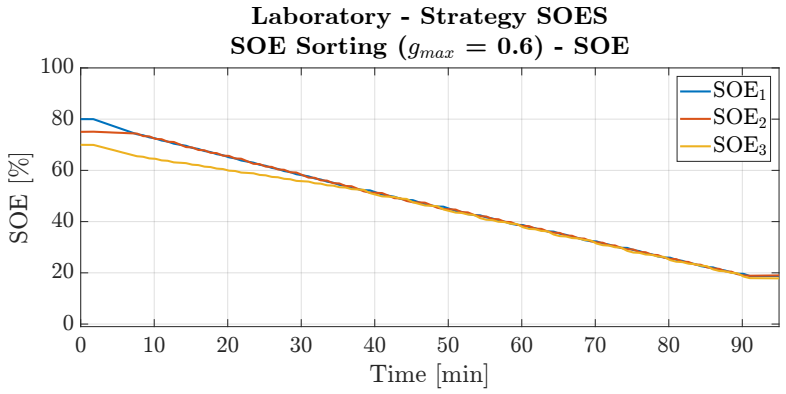
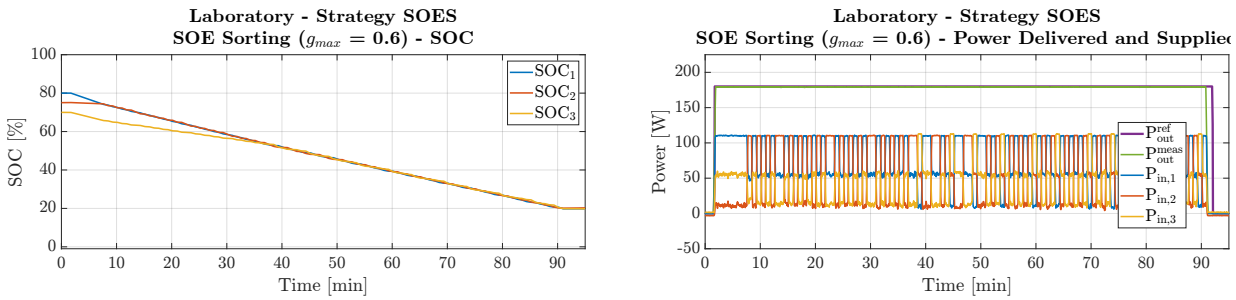


Figure 5.12: Laboratory - Strategy SOES - SOE Sorting $g_{max} = 0.6$ - SOE



(a) SOC (b) Power delivered by CHB and supplied by batteries

Figure 5.13: Laboratory - Strategy SOES - SOE Sorting $g_{max} = 0.6$ - SOC and power distributions

Furthermore, several experiments were carried out in the laboratory to verify the effectiveness of the gain g_{max} on the SOE sorting, where the gain of $g_{max} = 0.4, 0.5$, and 0.6 were applied. It can be observed in Fig. 5.14 how the SOE balancing converges faster when g_{max} increases. The greater g_{max}, the more distorted the output voltage will be. When $g_{max} = 1$, it can only output a 3L voltage, as only a single H-Bridge module will be used at a time.

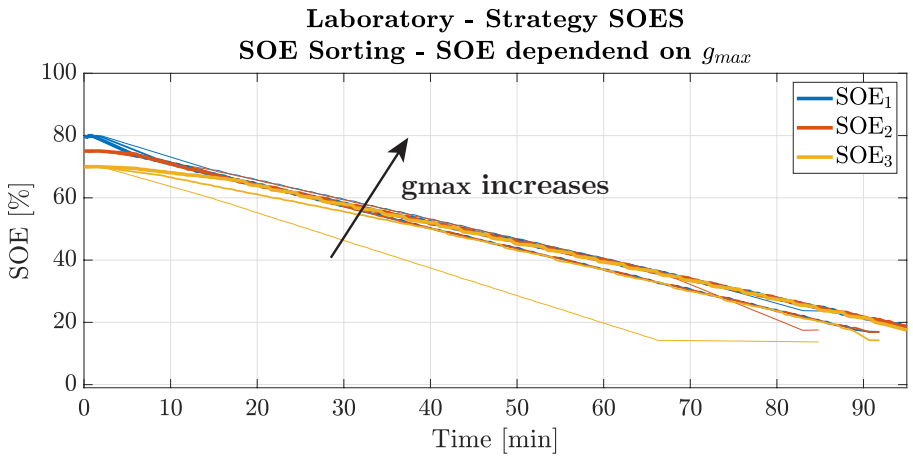


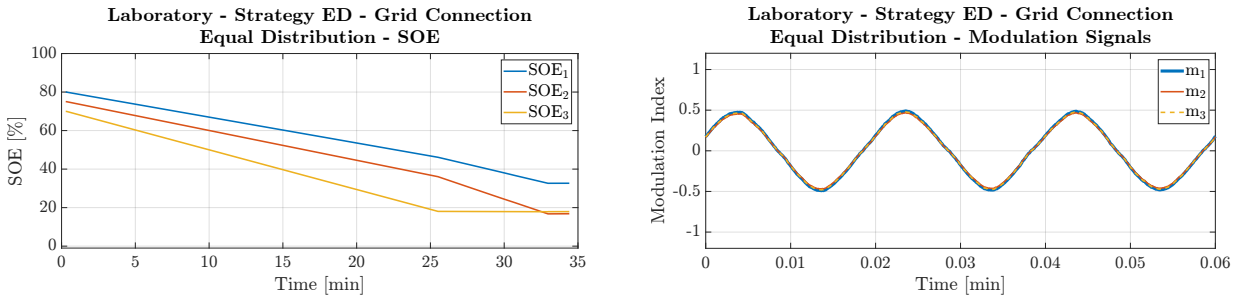
Figure 5.14: Laboratory - Strategy SOEB - SOE Balancing - SOE with increasing values for factor g_{max}

5.3 Strategies Proposed - Grid connection

Different experiments were carried out connected to a grid simulator to demonstrate the viability of supplying power to the grid. The grid simulator output voltage is set to a single-phase voltage of 115 V at 50 Hz. The grid simulator output voltage is lowered to half of the common single-phase grid voltage, i.e. 230 V due to the DC-link voltage limitation supplied to the CHB. The DC-link voltage maximum value is 360 V, i.e. 120 V per cell. In the figures below, only the SOE is shown, as seen before for the passive load experiments; the SOC and the SOE curves are very similar due to the equations utilized to obtain them. The experiments are carried out at a greater power reference to increase the output current amplitude without exceeding the hardware limitations.

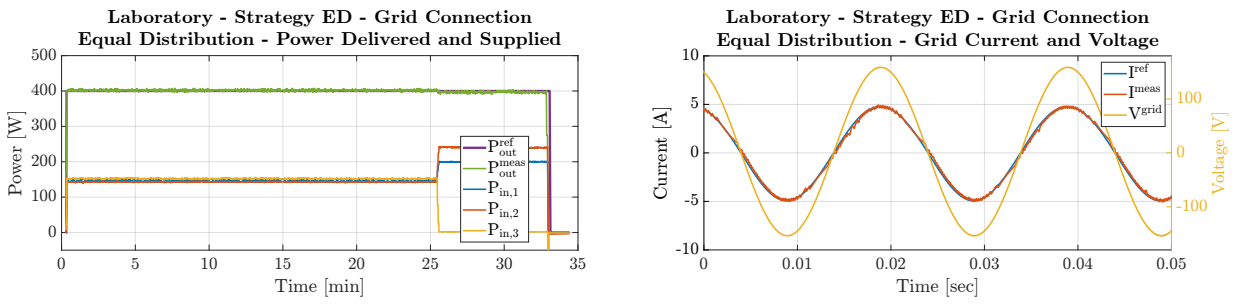
5.3.1 Strategy ED

First, the CHB is connected to the grid simulator with zero power reference. Then, a step change of 400 W is applied. It can be seen in Fig. 5.15a, as for the passive load, that the battery with the greatest capacity, i.e. battery one, is discharged with a lower rate than the smallest battery, i.e. battery three. The same can be seen when only batteries one and two deliver power. In that case, battery two discharges faster than battery one. It is shown in Fig. 5.15b that the modulation signals driving the CHB cells are equal for the three cells. Further, it can be seen how grid voltage and current are in phase, providing almost unity power factor. The power factor is calculated to be $cos(\phi) = 0.9963$, being ϕ the angle shift between grid current and voltage. The current THD is 3.5%.



(a) SOE (b) Modulation Signals

Figure 5.15: Laboratory - Strategy ED - Grid Connection - Equal Distribution - SOE and Modulation Signals

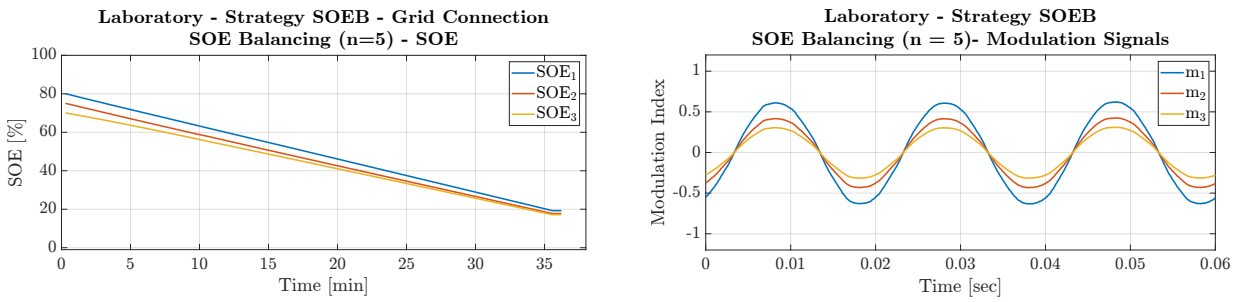


(a) Power Delivered by CHB and supplied by batteries (b) Grid Current and Voltage

Figure 5.16: Laboratory - Strategy ED - Grid Connection - Equal Distribution - Power, current and voltage

5.3.2 Strategy SOEB

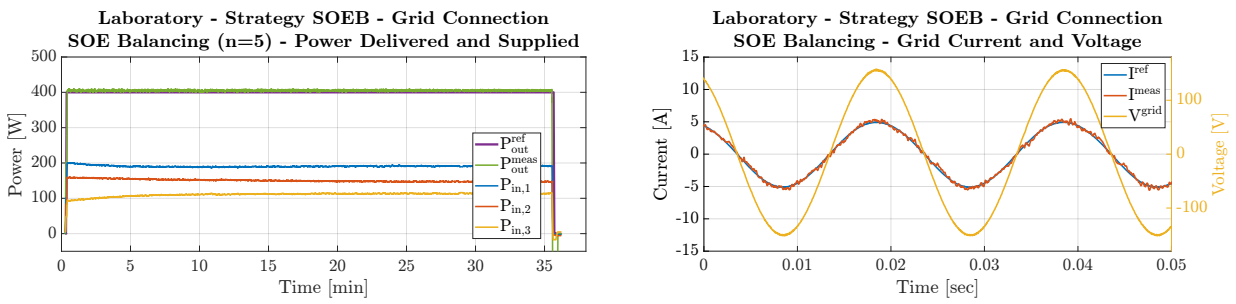
Secondly, strategy SOEB - SOE Balancing was also tested. It can be seen in Fig. 5.17a that as the power delivered has increased; the system balances the SOE slower than when injecting less power to the passive load. Further, Fig. 5.17b shows how the modulation signals are varied with the gain obtained with the differences on the SOE, as shown in (5.1). The modulation signal m_1 has the greater amplitude, whereas m_3 has the smallest, proportional to the SOE of the batteries connected to their respective cells.



(a) SOE (b) Modulation Signals

Figure 5.17: Laboratory - Strategy SOEB - Grid Connection - SOE Balancing $n = 5$ - SOE and Modulation Signals

These modulation signals dictates the uneven power distribution delivered, as in Fig. 5.18a. Battery one delivers most of the energy, whereas battery three delivers the least. The current THD has increased to 4.3%, which is beyond the limits [134].

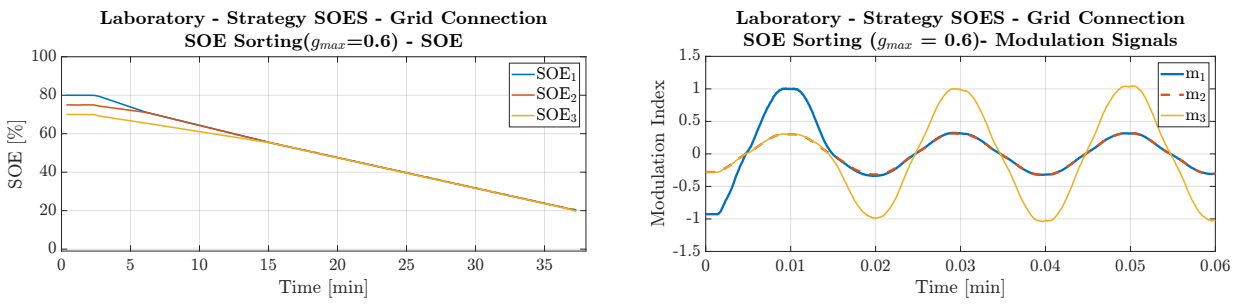


(a) Power Delivered by CHB and supplied by batteries (b) Grid Current and Voltage

Figure 5.18: Laboratory - Strategy SOEB - Grid Connection - SOE Balancing $n = 5$ Power, current and voltage

5.3.3 Strategy SOES

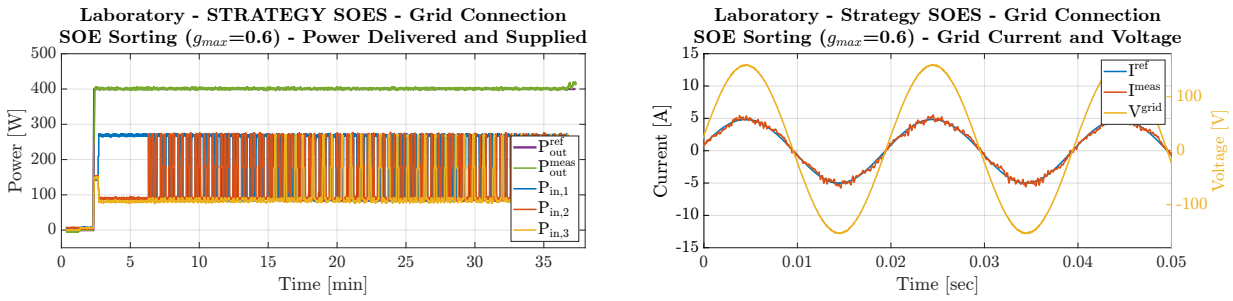
Finally, strategy SOES - SOE Sorting was tested in the laboratory. It can be observed in Fig. 5.19a that the SOE among the cells is balanced efficiently. Further, Fig. 5.19b shows how the modulation signals changes when at instant $t \approx 0.015s$, battery three has a greater SOE level than battery one ($t \approx 15$ min in Fig 5.19a). Then, the modulation signal of battery three, i.e. m_3, becomes the largest, whereas m_1 and m_2 have the same peak amplitude.



(a) SOE (b) SOC

Figure 5.19: Laboratory - Strategy SOES - Grid Connection - SOE Sorting $g_{max} = 0.6$ - SOE and Modulation Signals

As in the implementation when connecting to the passive load, Fig. 5.20a shows the main drawback of strategy SOES. When the SOE is balanced, and the batteries discharge at the same rate, the power delivered by the batteries step changes continuously. The number of times the step changes occur can be decreased by acting fewer times per unit of time, but with the drawback of causing divergence in the SOE among the cells. The THD of the current has been measured to 4.9% at a peak current of around 5 A.



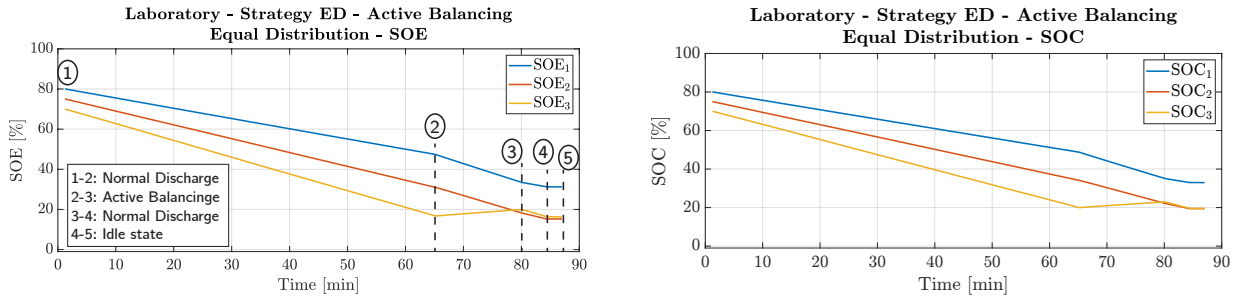
(a) Power Delivered by CHB and supplied by batteries

(b) Grid Current and Voltage

Figure 5.20: Laboratory - Strategy SOES - Grid Connection - SOE Sorting $g_{max} = 0.6$ Power, current and voltage

5.4 Active Balancing Technique

The active balancing technique has been tested with the different strategies proposed in the laboratory. When tested on strategy ED - Equal Distribution, the active balancing technique could charge the third battery, i.e. the battery simulator, by supplying more power from the DC linear power supplies. However, when tested on Strategies SOEB - SOE Balancing and SOES - SOE Sorting, the SOC was balanced when all batteries reached the lowest limit, so the active balancing technique did not act. The SOE and SOC for strategy ED - Equal distribution is shown in Fig. 5.21.



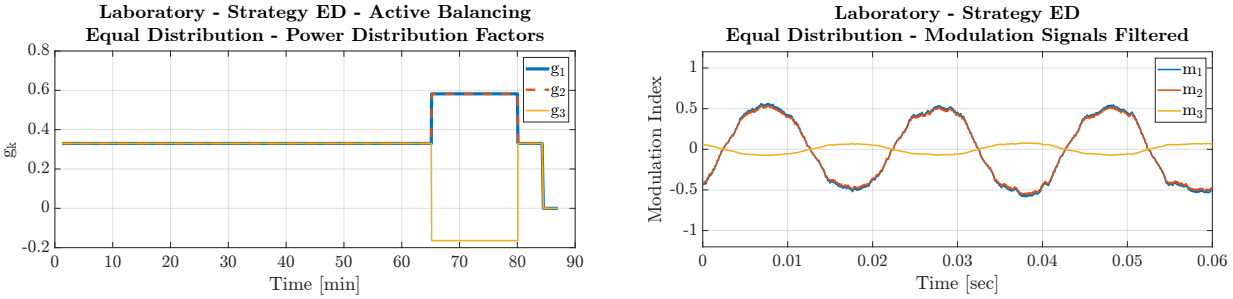
(a) SOE

(b) SOC

Figure 5.21: Laboratory - Strategy SOES - Active Balancing Technique - SOE Sorting $g_{max} = 0.6$ - SOE and SOC

It can be seen in Fig. 5.21 that at a time around 63 min (point (2)) after starting delivering the power, battery three reaches the lowest limit of 20%. At that moment, batteries one and two start delivering more power to supply power to the load and charge battery three; that is why the SOC and the SOE increase in battery three and decrease with a stepper rate at the same time in the other batteries.

The charging process finishes when battery's three SOC is equal to one of the other batteries' SOC (point (3)). It is further shown in Fig. 5.22a that the power distribution factor for battery three is negative in the period when it's charging, whereas gains for batteries one and two need to increase to compensate for the charging of battery three. Finally, the modulation signals obtained by the active balancing technique are shown in Fig. 5.22b, in which it can be observed the 180° phase shift between batteries one and two with battery three.



(a) gains (b) Modulation Signals

Figure 5.22: Laboratory - Strategy ED - Active Balancing Technique - Power Distribution factors and Modulation Signals

As can be observed compared to Fig. 5.7, the active balancing technique does not increase significantly the amount of time the system can deliver power to the load. Still, this technique could be of greater interest in a system with a larger amount of cells. Further, when the DC-link voltage requirement is more strict, the DC-link voltage can be greatly controlled by utilising this active balancing technique.

Chapter 6

Summary and Conclusion

Different stages of the work's development have been evaluated, and the conclusion of each is summarized in this chapter.

The cascaded H-Bridge has been proven to be a suitable topology for distributed power electronics control. Furthermore, the preliminary study of the individual full-bridge topology has led the path to a novel control method for battery impedance spectroscopy. It has been shown that there exists a trade-off between power quality when choosing between phase-shift (PS-PWM), level-shift (LS-PWM) and level-shift with permutation (LSP-PWM) PWM techniques. The PS-PWM offers higher effective switching frequency, moving harmonics to higher frequencies. The concept of Weighted THD is introduced to analyze this effect. On the other hand, switching losses are higher for the PS-PWM than for level-shifted strategies. The LS-PWM method without permutation has uneven losses distribution among the cells, which can be solved by applying a LSP-PWM. In such a way, conduction losses are equalized among the cells. The LSP-PWM method performs better than the LS-PWM without permutation with the drawback of a higher computational burden. Then, battery energy storage systems were presented. Several State-of-Charge (SOC) and State-of-Health (SOH) estimation methods were reviewed. Further, the State-of-Energy (SOE) modelling method is presented and later on being utilized in the control strategies for the Battery Energy Management System (BEMS). Battery electromechanical impedance spectroscopy (EIS) method were also introduced.

To control output current, a proportional-resonant (PR) controller and a phase-locked-loop (PLL) have been designed and tested under disturbances, both in simulations and in the laboratory. It was demonstrated that the current control loop and the PLL fulfil the designed requirements and respond according to theory and simulations.

An active balancing technique is proposed in this work, where the modulation signal of the H-Bridge is regulated according to the battery that is required to be charged. As a result, it has been proven that it is possible to charge and discharge batteries independently, with the trade-off of reducing the output power quality. Three strategies were proposed to distribute the power among the cells when a commanded output power is given to the CHB. The first strategy is the Equal Distribution (ED); where all the batteries deliver the same amount of power regardless of the SOE of the batteries. This approach reduces the computational burden but also the performance of the system.

The second strategy is the SOE Balancing where the controller distributes the power among the cells to balance the SOE among the cells. The time it takes to balance the cells can be controlled with the power distribution factor exponent n. This strategy has a significant computational burden and balances the SOE continuously. The last strategy is the SOE Sorting method. This strategy is based on an optimization problem which maximizes the availability of the system power delivery, by priority the utilization of the battery with the highest SOE. Effectively, this strategy balances the SOE of the batteries but produces step changes in the power input, which may affect the battery performance but has a lower computational burden that the SOE Balancing strategy. The strategies have been tested in simulations and laboratory to prove their viability connected to a passive load and a grid simulator.

An EIS technique is proposed for online battery impedance estimation. This technique allows the battery impedance estimation while supplying power to the grid. The impedance can be determined by distorting the DC-link currents and measuring the current and voltage. The distortion in the DC-link currents is produced by injecting a sinusoidal waveform with various frequencies in the modulation signal used in the PWM technique. Simulation results show that it is possible to distort the DC side currents and voltage, whereas the analysis and impedance spectroscopy has not been assessed in this work.

To conclude, the three problem statements are answered and covered:

- *How to develop a method to diagnose the SOH of batteries using power converters*

The EIS technique proposed can be utilized to estimate the battery impedance parameters but with limited accuracy and frequency range. The accuracy can be improved by injecting a wider range of frequencies, but with the limitation of the controller bandwidth and variation of SOC at low frequencies injection.

- How can the balancing of battery systems be achieved using distributed power electronics.
- Benchmark the proposed control strategies to be implemented for second-life batteries with distributed power electronics.

The active balancing technique is proven to work and charge the batteries when needed in the CHB. Among the three proposed strategies, the one that performed better was the SOE Balancing method as the time delivering power and producing a seven-level output voltage is increased, with the trade-off of highest computational burden. The second strategy which performed better is the SOE Sorting method, as the time delivering power and producing seven-level output voltage is increased but with the trade-off of step changes in the power delivered by the batteries. Finally, the strategy Equal Distribution delivers power and seven-level output voltage for the least time, but with the smallest computational burden. These exposed arguments can answer positively the problem statement questions stated at the beginning of the project.

Chapter 7

Future Work

This chapter suggests future research lines related to the study of distributed power electronics for second-life battery systems. The suggestions need to be seen as a continuation of this project report.

- In this work, a technique for impedance spectroscopy has been proposed. In contrast, it has not been possible to analyze and compute the battery impedance and make the appropriate Nyquist plot. A mathematical analysis of the current and voltage to obtain the battery impedance with different battery parameters and frequencies could prove the proposed technique.
- In this work, the distributed power control among the cells is carried out in the simulations with the same OCV-SOC curve and the same battery equivalent model. The system's dynamic performance can be assessed by testing different battery characteristics, e.g. different series resistance and number of series-connected cells.
- The active balancing technique could be further explored. A mathematical relationship between phase shift and amplitude of the modulation signals, charging and discharging rate and output quality could be assessed. Additionally, the active balancing technique is suggested to perform better in systems with more levels. By testing this technique further in MLIs, it could be proven.
- In this work, only active power has been considered. Further investigations could be assessed to check the system performance when reactive power is considered.
- This work utilizes a decentralized topology in a single-stage, i.e. omitting the DC/DC converter. Further investigations can be carried out to analyze the efficiency and performance of the system when utilizing a decentralized topology in a two-stage, i.e. DC/DC and DC/AC converter.

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Appendix A

DC Side Filter Increasing

The inverter utilized in the present project is incorporated on a printed circuit board (PCB). The purpose of the PCB is to test the connection of PV systems to a three phase grid. Therefore, the input DC side filter was designed for an specific DC voltage and rated power. As the system in this projects works with lower DC voltage and power, the size of the capacitors needed to be increased. As explained in 3, the DC side capacitor values is calculated as follows, repeated here for the sake of completeness:

$$\Delta V_c = \frac{P_{out}}{C_{dc} \cdot \omega \cdot V_c} \tag{A.1}$$

The PCB has a DC capacitor tank of 680 μF, i.e. 2.5 times less than needed. Therefore, it was chosen to replicate three times the capacitor tank, as illustrated in Fig. A.1.

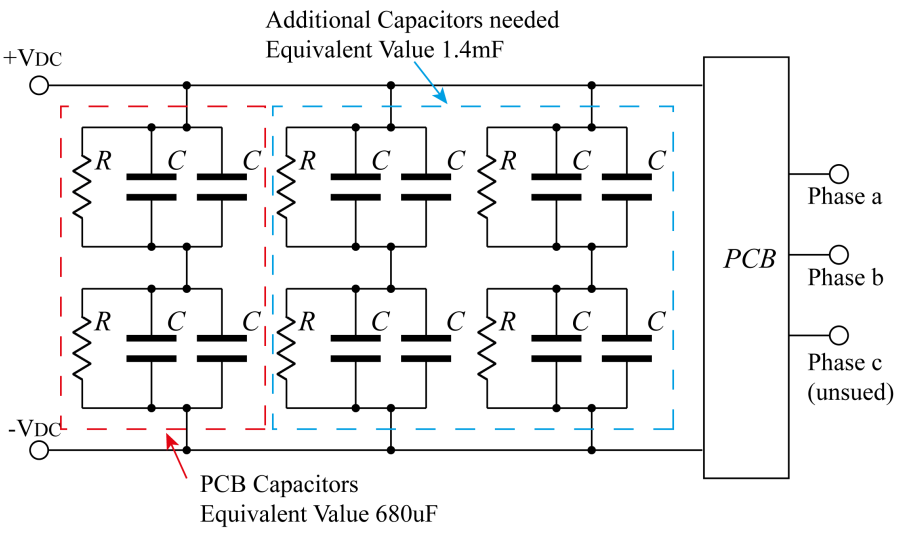

Figure A.1: Laboratory - Capacitor tank implemented

The description of the real topology is shown in Fig. A.2.

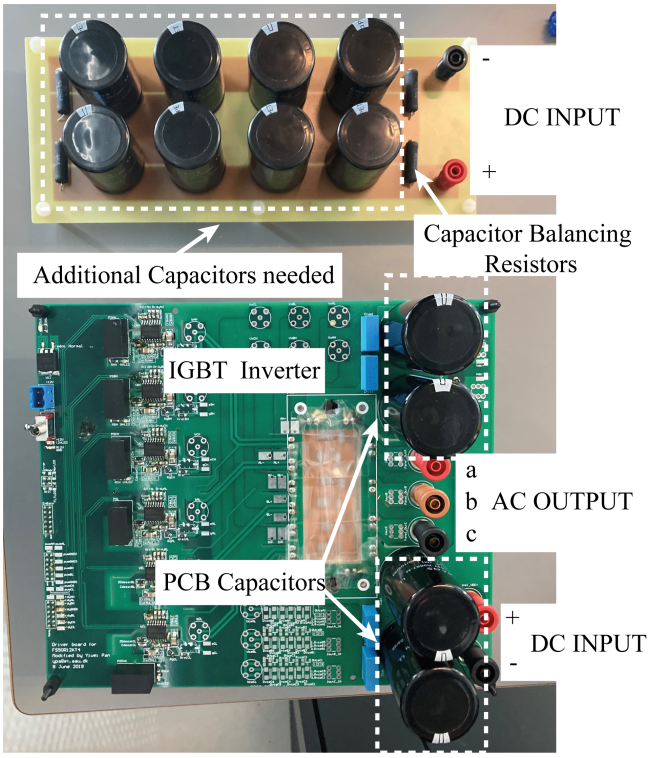

Figure A.2: Laboratory - PCB and Capacitor tank implemented

An experiment is carried out in the laboratory to verify the performance of the capacitor tank calculated and implemented. In the experiments, the voltage in the capacitor is 50 V, the power delivered 90 W and the frequency of the output power 50 Hz. Substituting these values in (A.1), yields to a voltage ripple in the capacitors of 8.4 V for the original system and of 2.8V for the modified system, as can be seen in Fig. A.3.

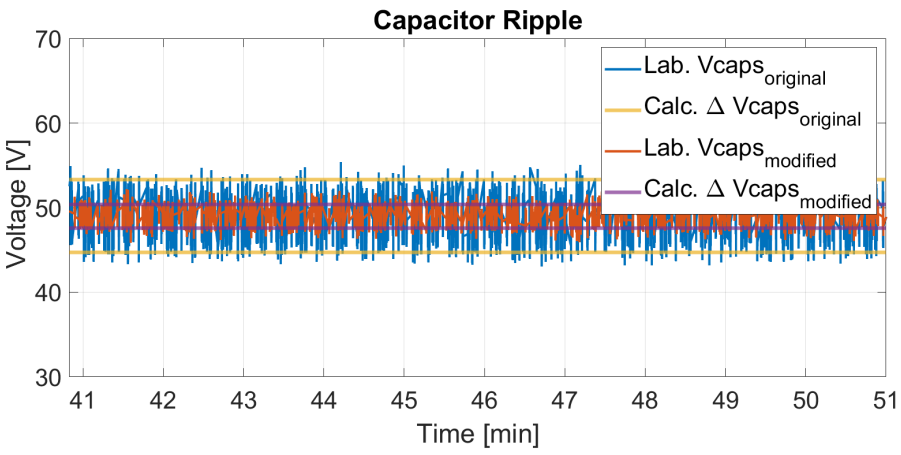

Figure A.3: Laboratory - Capacitor ripple measured in the original and the modified system

Appendix B

FPGA Programming

This appendix explains why and how the FPGA program is made in dSpace. The triangular waveforms are made in dSpace and then fed into the FPGA built. The signal flow is shown in Fig. B.1.

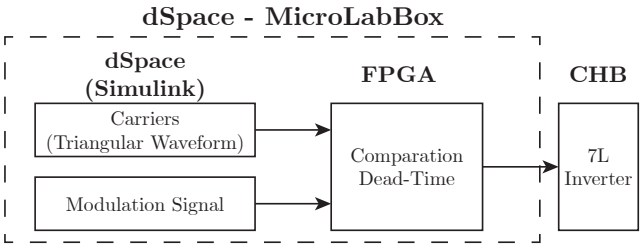

Figure B.1: Modulation signals and carriers are made in Simulink. Comparison and dead-time are made in the FPGA. Signals are provided to the H-Bridge

At first, it was considered to use a default block existing in the dSpace library called " MCU Motor Blockset". This block takes as input three modulation signals (duty cycles), and output the signals to the CHB. As there is not a comparison between carriers and modulation signal, the modulation signals need to be phase-shift with each other. The main problem is that, in case of an event or an immediate action on the system, the phase-shifted signals will not take simultaneously, but with a time lag, as illustrated in Fig. B.2.

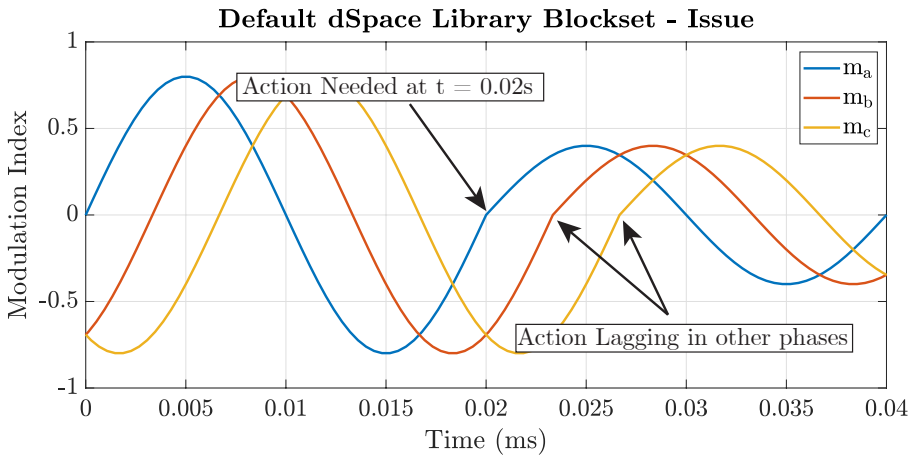

Figure B.2: Modulation signals provided to the default dSpace Blockset are not optimum. The phase-shift between can cause unstable operation

The FPGA is programmed with the software Xilinx Vivado ® [147]. One of the advantages of utilizing a real comparison between carriers and modulation signals is that it can have instantaneously effect in all the H-Bridges in the system almost simultaneously. The second advantage is that the step size in the FPGA is of 10 ns, compared to the maximum 40 μs that is, 4000 times smaller, achieving higher performance.

The triangular waveforms and the modulation signals are generated in the dSpace and the signals are then compared in the FPGA. The inverter utilized in this project has a minimum turn-on delay time of 0.13 μs and a maximum turn-off delay time of 0.4 μs. Moreover, the gate driver in the PCB should be taken into account, which is the $1ED020I12 - F2$ from infineon [148]. The minimum rise time is 0.01 μs and the maximum rise time in the gate driver is delay is of 0.80 μs. Therefore, the total The dead-time should be high enough in order not to short-circuit the DC-link capacitor. It is recommended in [149] that the dead-time should be calculated with (B.1):

$$t_{dead} = n_s \cdot [(t_{d_o ff_m ax} - t_{d_o n_m in}) + (t_{pdd_m ax} - t_{pdd_m in})] \tag{B.1}$$

In which n_s is a safety margin. They suggest that $n_s = 1.2$, whereas in this work $n_s = 1.4$ to increase the safety margin. Then, substituting the values in (B.1):

$$t_{dead} = 1.4 \cdot [(0.4 - 0.13) - (0.80 - 0.01)] \approx 1.3\ \mu\text{s} \tag{B.2}$$

Therefore, it is equal to counting 130 steps of 10 ns. The dead-time is implemented in the FPGA by utilizing logical blocks,i.e. and, not, or, etc. The The block diagram for the comparison with the triangular and the generation of the complementary signal for each H-Bridge including the dead-time is shown in Fig. B.3.

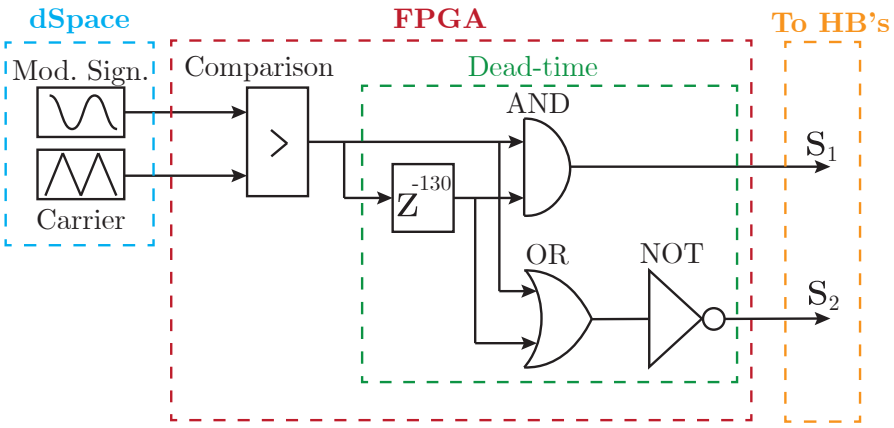

Figure B.3: Block diagram of the implemented FPGA comparison and dead-time.

The logical waveforms of the dead-time block are shown in Fig. B.4.

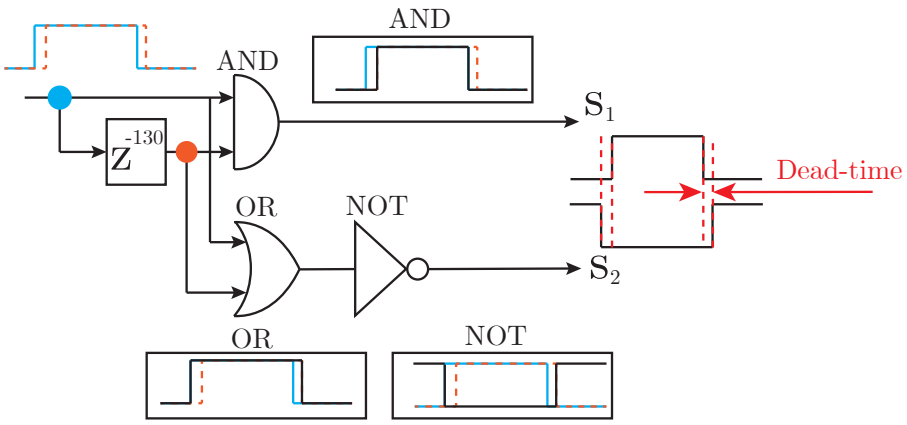

Figure B.4: Block diagram with logical waveforms producing the dead-time in the gate signals.

After installing the software and licenses for Xilinx Vivado, the FPGA programming is made in the following steps:

1. Open a new '.slx' Simulink model. First, the step size for the system needs to be set. In this work, the step is 10 ns. Then, the library Xilinx Blockset needs to be used to drag the blocks into the model. It should be noted that each block will provide a unitary delay to the input signal,i.e. a discrete delay z^{-1}.

2. It is possible to debug the system as a normal Simulink model, y running the system and checking the signals with normal 'Scopes'. The FPGA will have inputs from the dSpace and Outputs to the H-Bridges, as illustrated in Fig. B.1.

3. Once the model is built and debugged, the system needs to be built. The system creates a folder in the working space with a '.ini' file, which contains the FPGA programmed. It is no longer possible to edit this file.

4. The '.ini' file is imported to dSpace into the main control Simulink model, in the highest layer of the model. Typically, the control system is placed inside a triggered subsystem. The FPGA imported file needs to be placed outside of this loop.

5. The Simulink model with the control system is built as normal with the Simulink C-Code plugin.

Appendix C

SOGI PLL Analysis

The phase-locked-loop (PLL) utilized in this project is shown in Fig. C.1, which is a fixed frequency second-order generalized integrator (FFSOGI).

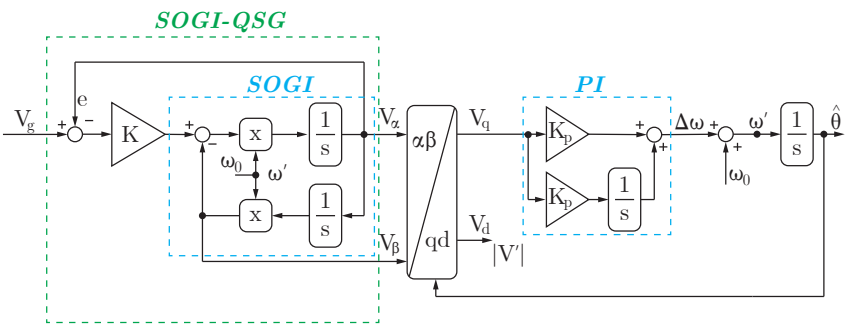

Figure C.1: Block diagram of a conventional FFSOGI-PLL

As the PLL described is two be used in a single-phase system, a quadrature signal generator (QSG) creates a voltage signal which is $\pi/2$ rad lagging the input signal. The transfer function from V_α/V_g, i.e. the ratio between the generated signal and the to be tracked (V_g); and the transfer function between V_β/V_g, i.e. the quadrature signal and the signal to be tracked, are shown in (C.1) and (C.2), respectively:

$$G_\alpha(s) = \frac{V_\alpha(s)}{V_g(s)} = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \tag{C.1}$$

$$G_\beta(s) = \frac{V_\beta(s)}{V_g(s)} = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \tag{C.2}$$

Being k the damping factor for the error in the estimated signal (V_α) and the real signal (V_g), and ω the fundamental frequency of the real signal. The bode plot for both transfer functions are shown in Fig C.2.

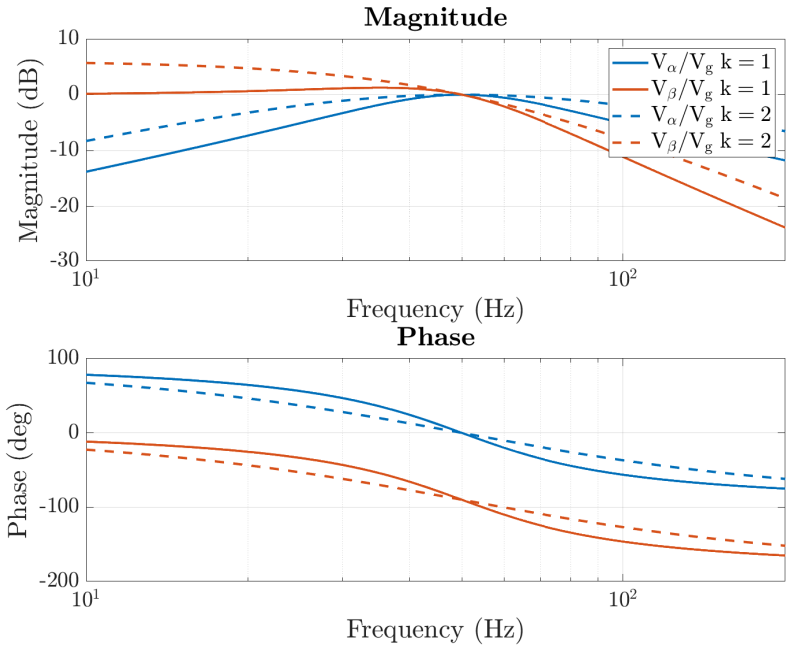

Figure C.2: Bode plot of the QSG transfer functions.

As can be seen, the resonant frequency appears at 50 Hz. The damping factor k is related to the bandwidth and the filtering effect; lower values of k results in higher filtering but higher response times [150]. In Fig. C.2 it can be seen that the gain is reduced in the case of $k = 1$ compared to the one with $k = 2$ and the bandwidth is reduced from 63.6 Hz to 32.11 Hz. On the other hand, the time response against an impulse to G_α is smaller with higher values of k as shown in Fig. C.3.

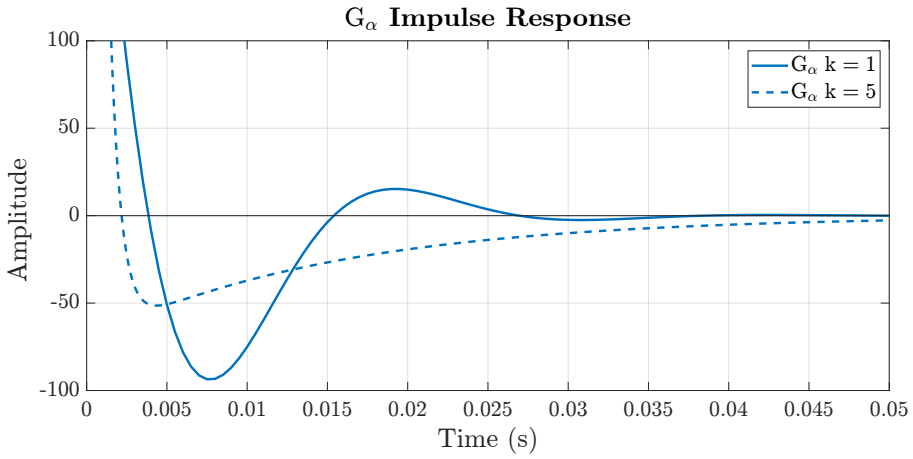

Figure C.3: Impulse response in the quadrature signal generation G_α transfer function

The open- and closed-loop transfer function are shown in (C.3) and (C.5), respectively.

$$G_{OL}(s) = \frac{\theta(s)}{\theta^*(s)} = \frac{K_p s + K_i}{s^2} \frac{1}{\tau_p s + 1} \tag{C.3}$$

Being $tau_p = 2/k\omega$[135]. Typically, the phase margin (PM) of the open-loop transfer function is recommended to be $30° < \text{PM} < 60°$, which yields a value for the damping factor k as in (C.4) [133]:

$$1.732 < k < 3.732 \tag{C.4}$$

In this work, $k = 2$ resulted in a stable operation. Once the stability of the system is established, the transient response performance needs to be designed, i.e. the PI parameter tuning.

$$G_{CL}(s) = \frac{1}{1 + G_{OL}(s)} \tag{C.5}$$

Therefore, by utilizing the second-order system classic parameters

$$\zeta = \frac{K_p}{2\sqrt{K_i}} \tag{C.6}$$

$$\omega_n = \sqrt{K_i} \tag{C.7}$$

In which the damping ratio ζ is selected to be $\zeta = 1/\sqrt{2}$ as the most optimum value for voltage frequency and phase jump [133]; The natural frequency should be chosen to have good filtering and disturbance rejection, while having and acceptable transient performance, in this work $w_n = 5$ Hz. Then the PI parameters are tuned to be $K_i = 20$. The parameter $K_p = 6$ was adapted to be $K_p = 0.5$ in the discrete implementation. The results for voltage jump, frequency jump and phase jump are shown in Section 4.1.1.