# Synchronization Stability of Inverter Based Resources during Faults on Low Voltage Grids

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Energy Technology, PED4-1042, 2022-01

Master's Project Semester

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**Abstract:**

The transition from conventional power system to power electronics dominated power system. Concern regarding the availability and stability of the future power system is emerged. The system will be more prone to short-circuit faults as it will highly dominated by inverter based resources. To address this issue, fault ride through capability is required to avoid voltage and frequency instability. However, loss of synchronization is observed during severe symmetrical faults and second harmonic oscillations for asymmetrical faults. In order to avert the loss of synchronization current injection angle with respect to line impedance characteristics is carried out in this project. To that end, modified positive and negative sequence injection method is proposed to attenuate second harmonic oscillations and avoid over voltage in non faulty phase during asymmetrical faults.

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# Summary

The increasing energy consumption globally an increased electrical production to meet these requirements. In past decades, due to foreseen exhaustion of fossil based energies has brought worldwide attention towards sustainable energy production. The desire to reduce the carbon footprint has made us more inclined towards penetration of renewable energy resources like wind turbine, photovoltaic and energy storage systems into the power-system. The transition from the conventional power-system to power electronics dominated power-system has imposed many challenging issues to the distribution power grid and utility. The generation from renewable energy resources is always time-varying and fluctuating, especially with a high penetration of renewables under the mixed energy infrastructure. This will affect the network stability and more prone to disturbances. The transmission system operators have issued stringent interconnection codes for the grid integration of renewable energy resources. Therefore, concerns regarding the resiliency and stability of the system have been raised especially being vulnerable to extreme weather conditions. In the world around 50% of the network is composed of low-voltage system. Thus making low-voltage network more prone to short circuit faults due severe weather/climate conditions. The stability of the system due to such conditions has raised questions in the past. However, the stability of the system due to severe short-circuit faults is a growing concern with increasing integration of renewable energy resources. The grid-requirement needs to be fulfilled to avoid voltage instability of the system. On the other hand, due to severe faults both voltage and frequency instability occurs leading to unintended disconnection of system from the network. The unintended disconnection of system from the network due to short-circuit faults has lead to concern over synchronization stability under such conditions. The objective is to provide voltage support without losing synchronizm from the network.

During short-circuit faults as per grid-code requirements reactive current injection is required to provide voltage support. However, due to severe symmetrical faults the loss of synchronizm is most likely to occur as it is highly dependent on line impedance characteristics. Accurate current-transfer limits needs to be derived depending upon line impedance characteristics and current injection angle.

On the other hand, the asymmetrical faults leads to the generation of second harmonic oscillations. The conventional method cannot avoid loss of synchronizm or attenuate second harmonic oscillations. However, conventional method during asymmetrical faults also introduces over voltage to non-faulty phase. In order to solve this problem modified flexible positive and negative sequence injection is proposed by considering dc link dynamics to provide flexible current sequence injection. This method attenuates second harmonic oscillations and avoids over voltage to non-faulty phase. The proposed method consider DC link dynamics, avoid use of complex phase locked loops for sequence extraction and less computational burden making it suitable for low-voltage grid integrated system. Time domain analysis is carried out considering different scenarios. The derived controllers are implemented in hardware-in-the-loop to provide a real-time implementation of the considered scenarios. This project considers the worst case scenario possible, where the conventional method fails and aims to provide a feasible solution.

# Preface

The following project is the work carried in $4^{th}$ semester on the masters program of Power Electronics and Drives at the Department of Energy, Aalborg Universitet. This project aims to study the synchronisation stability of inverter based resources in low voltage grids during faults. The theme of the project is to avoid using complex controllers or methodologies. Complex controllers introduce additional delay into the system and not feasible for low-voltage grid integrated system. The solution required for such systems should be less complex, cheap and low computational burden. However mathematical algorithms can be utilised as they won't introduce additional delay and easy to implement. The control strategies implemented in this project will be only dedicated for low-voltage grid integrated system.

The prerequisites for reading this project is basic understanding of classical control theory and integration of grid side converter to the grid. Apart from that, efforts have been made to familiarize the reader with the structure. To further clarify conclusion are provided at the end of every chapter.

This project is highly dependent on different software package applications. MATLAB has been used extensively for numerical calculations, coding and plotting figures. PLECS was used for discrete implementation of controllers and for off-line studies. MATLAB SISO tool was utilised for tuning of all the controller parameters with classical tuning methods during this project.The appendices are attache at the end of report describing basic theory.

Aalborg University, May 30, 2022

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# Contents

# Chapter 1

# Introduction

## 1.1 Background and Motivation

The increasing electrical energy consumption globally imposes an increased electrical production to meet the requirements. However, foreseen exhaustion of conventional fossil-fuel based energies (e.g-coal, oil and natural gas), has brought considerable worldwide attention towards sustainable energy production [1]. Additionally, fossil-fuel based generation causes emission of pollutant gases, which pollute the natural environment and causes global warming. Thus, fossil-fuel based energy generation is considered an unsustainable in long-term strategic plans. To that end, the desire to reduce the $CO_2$ emissions has made us more inclined towards penetration of renewable energy sources (RES), such as Wind Turbine Systems (WTs), Photovoltaic Systems (PVs) and Energy Storage Systems (ESSs) into the power system [2]. Especially, the worldwide installed capacity of PVs and WTs are increased upto a great extent in past decade as depicted in Fig.1.1.

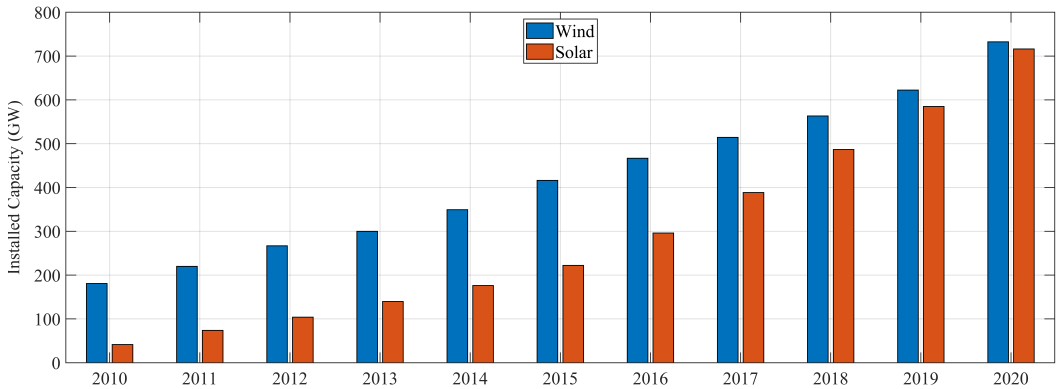


**Figure 1.1:** Global accumulative capacity of Wind and Solar in Giga Watt (GW) from 2010-2020 based on the data available from International Renewable Energy Agency (IRENA) [3]

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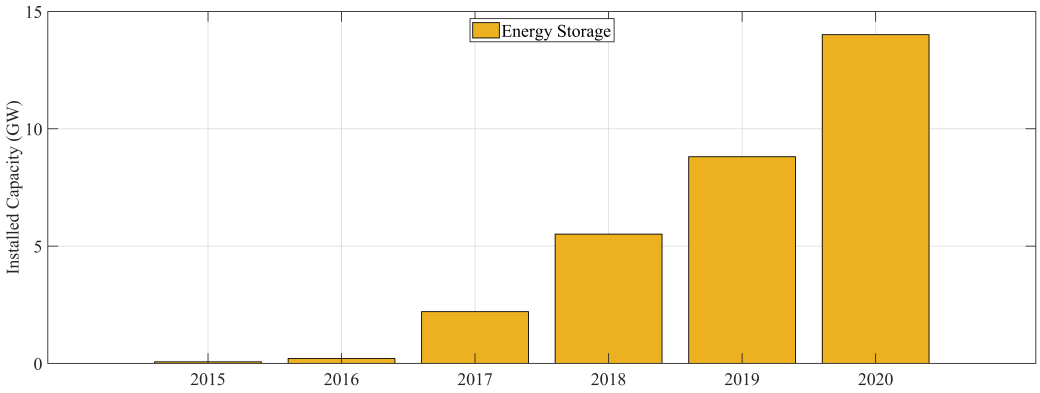


**Figure 1.2:** Global accumulative capacity of Energy Storage in GW from 2015-2020 based on the data available from International Energy Agency (IEA). [4]

On the other hand, ESSs like batteries have starting emerging in past few years and will be scaled upto 148 GW as per IEA as depicted in Fig.1.2 and they can provide more flexibility to the power system and market demands [4]. The global installed capacity of PVs is 720 GW, WTs is 740 GW and ESSs is 14 GW till the year 2020.

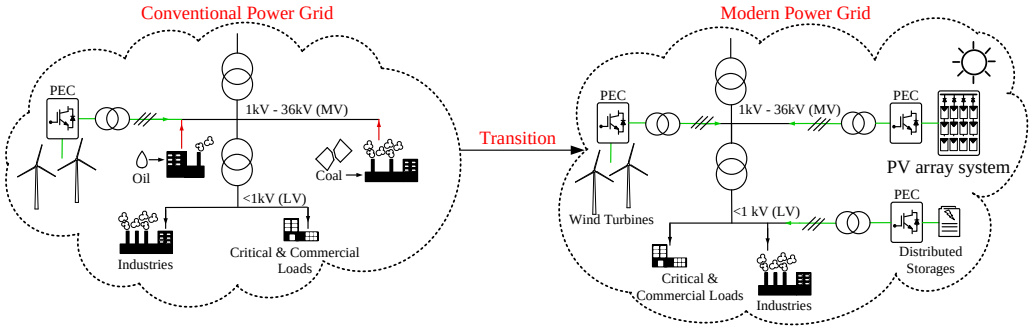


**Figure 1.3:** Renewable Energy Source (RES) interfaced in conventional and modern power grid

However, the conventional power grid is mostly dominated by fossil-fuel based generation and less RES at Low-Voltage (LV) and Medium-Voltage (MV) level [5]. The goal of achieving 100% renewable grid with variable renewable energy (VRE) systems are interfaced to the grid as in Fig.1.3. In order to comply these VRE systems to the grid. The transmission system operator (TSO) provide technical regulations to comply with the grid like National Grid ESO for Great Britain [6], TenneT for Germany [7] etc. Similarly, in Denmark Energinet the Danish national TSO has technical regulations for interconnection of RES to the grid defining minimum technical and functional requirements for different RES. The technical regulations are divided into different categories based on the rated power at the Point of Connection (POC). The category for PVs and WTs are similar but Technical regulations

(TRs) vary as in [8].

**Table 1.1:** Category of plants based on the rated power at the point of connection

| Category | PVs and WTs / ESSs |
|---|---|
| A2/A | above 11 kW including 50 kW / up to 125 kW |
| B | above 50 kW including 1.5 MW /including 125 kW up to 3 MW |
| C | above 1.5 MW including 25 MW / 3 MW up to 25 MW |
| D | above 25 MW or connected to over 100 kV / including 25 MW or above 100 kV |

While for ESSs both TRs and category of plants vary as in [8].In this project, only TRs for RES will be followed. Further, there can be multiple small WTs depending upon their configuration like Type-1 and Type-2 which consists of gear box with induction generator [9] , Type-3 with Double fed Induction Generator (DFIG) having partial scale of PEC [9] and Type-4 with synchronous generator having full scale PEC [10] will be considered. While, for PVs and ESSs there is as such no type.

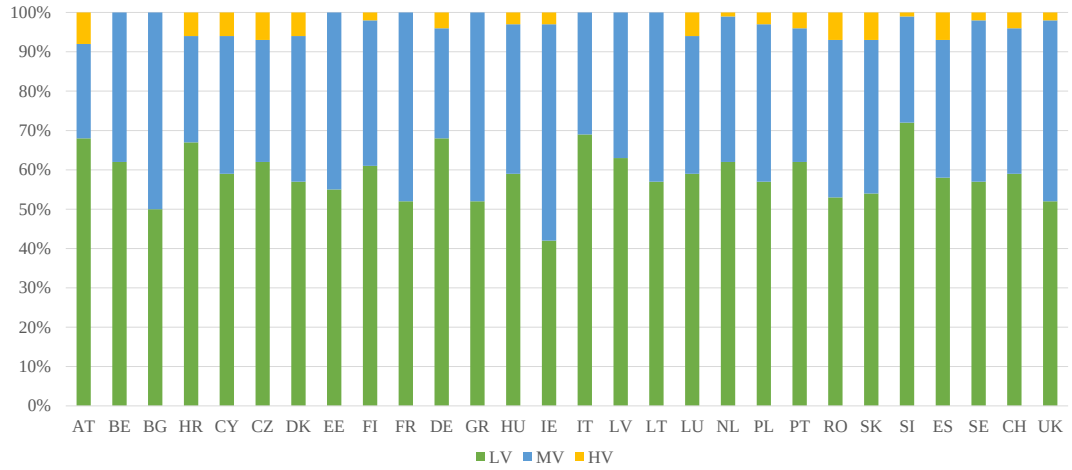


**Figure 1.4:** Share of distribution lines in Europe based on the data available from Euelectric ( AT (Austria), BE (Belgium), BG (Bulgaria), HR (Croatia), CY (Cyprus), CZ (Czech Republic), DK (Denmark), EE (Estonia), FI (Finland), FR (France), DE (Germany), GR (Greece), HU (Hungary), IE (Ireland), IT (Italy), LV (Latvia), LT (Lithuania), LU (Luxembourg), MT (Malta), NL (Netherlands), NO (Norway), PL (Poland), PT (Portugal), RO (Romania), SK (Slovakia), SI (Slovenia), ES (Spain), SE (Sweden), CH (Switzerland) and UK (United Kingdom) [11]

In Europe, 60% power network is composed of LV lines (< 1kv), while rest 37% of MV lines (between 1kv and 36kv) and 3% of High voltage (HV) lines (> 36kv) as in Fig.1.4. In conclusion, the low-voltage lines are more widely distributed as compared to others and more prone to grid faults. However TSO's around the world does not show the requirement of Low-Voltage Ride Through (LVRT), in

order to support the power-system during grid faults. This can be a concern as recent instances have been recorded at DSO (Distribution System-Operator) level. Which represents the need of LVRT to avoid system instability. Power outages is also one of the main concern at DSO level to large number of customers as end users. The **energy tangle in China** is one of the example, where two dozen's of China's 31 administrative units had rolling blackouts in the year 2004[12]. One of the main reason concluded for such frequent and unintended power outages was due to increase in **demand and shortage of generation** as they were highly dependent of fossil-fuel generation especially coal. A similar scenario was observed at the end of year 2000, where a massive blackout in the north-east of the US and Canada happened due to similar reason as in China [13]. As we are moving towards power-electronics dominated grid (PEDG) both supply and demand stability with respect to power-converter control stability needs to be considered to avoid such situations [14].

Fault in power-system also leads to **major blackout** in Italy. The **Italian blackout** in the year 2003 on September $28^{th}$ at 3:01 a.m., a fault on Swiss power-system due to overloading of two Swiss internal lines (interconnection lines heavily loaded by large power import) close to the border of Italy [15]. The coordination between the operators of Swiss and Italy were not sufficient enough to mitigate the overload. As a consequence, cascading outages on the interconnection lines to Italy. This further resulted in **loss of synchronism** and **loss of large import of power**. Eventually, a large frequency decline in Italy, automatic load shedding procedure was not able to shed enough load to maintain the generation and load demand leading to blackout. A similar scenario occurred on $14^{th}$ of August in the year 2003 in **North America** [16]. This blackout was the biggest that North America has ever faced nearly affecting around 50 million people and 61,800 Megawatts (MWs) of load in states of Ohio, Michigan, Pennsylvania, New York and provinces of Canada (Ontario) [17]. Major blackouts reported up till now initiated by a single event or multiple faults gradually leading to **cascading outages** and eventually collapse of power system. Above instances discussed mainly occur due to faults on MV and HV lines. Further, the impact of faults on LV lines causing system instability will be discussed.

In Europe, there are small islands which form their own regional power-system through variable RES penetration as they are far from synchronous generation units. There are various projects being carried out like for energy storage solutions in Canary Islands, Ventotene, Faroe Islands, La Reunion, Tilos and Kythnos [18]. ESSs offer more flexibility and stability to the grid togther with other PVs and WTs like Cyprus, Malta and Kythnos on LV network reducing the disturbances from the WTs and PVs ,especially the disturbances in PVs [18]. These solutions on LV network like roof-top PVs, small WTs are paid for operating during ancillary services [19]. In conclusion, the LV network needs to support the grid during faults

especially in standalone system as in Europe Islands. The next section will discus about power system faults and how instability phenomena occurs due to faults.

## 1.2 Power System Faults and Instability Phenomena

Faults in power system are mainly weather-related [20]. The weather factors that causes Short-Circuit (SC) faults are lightning strikes, heavy rain, strong winds or gales, accumulation of snow, fire and floods adjacent to electrical equipment (underneath overhead lines). Vandalism and human error are also the causes of SC faults, in certain cases there could be breach of minimum clearances between the trees and overhead lines. These are few of the factors that contribute to faults in power system. However, equipment failure like transformers, machines, reactors, cables etc. may also cause faults.

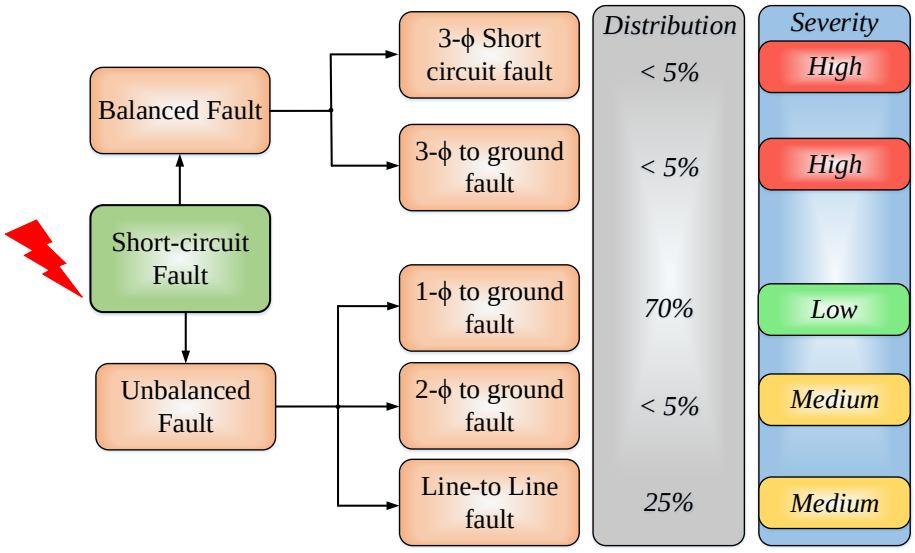


**Figure 1.5:** Types of line faults with their distribution percentage and severity level[21]

The SC fault can be divided into balanced faults (symmetrical faults) and unbalanced faults (unsymmetrical faults) as in Fig.1.5. In symmetrical faults, three-phase (3-$\phi$) fault or 3-$\phi$ to ground fault. The severity of these faults is high but the chances for occurrence of these faults is less then 5%. These faults occur mostly due to human error [20]. On the other hand, unsymmetrical faults can be single-phase (1-$\phi$) fault, double-phase (2-$\phi$) fault and phase-phase fault also called as Line-Ground (LG) fault due to physical contact like lightning [22], Double Line-Ground (DLG) fault due to storm [22] and Line-Line (LL) fault due to close contact of lines [22]. The severity of LG fault is lowest but the occurrence of this fault is the highest.

While, for LL and DLG fault the severity is medium. The LL fault is quite often to occur but less then LG fault. Further, the voltage sag/dip can be divided into seven distinct types depending on the type of fault and the connection (star or delta). At LV/MV/HV it depends on voltage at Point of Connection (POC) and the winding connection of transformers.

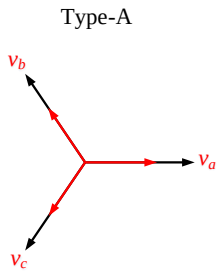


**Figure 1.6:** Type-A (Sag-A) during symmetrical-faults.

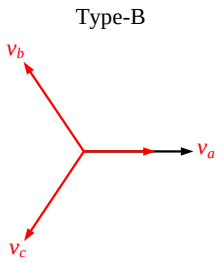


**Figure 1.7:** Type-B (Sag-B) during unsymmetrical-faults.

Type-A sag occurs due to three-phase (3-$\phi$) fault or 3-$\phi$ to ground fault. Where all the three phase ($v_a, v_b$ and $v_c$) dips as in Fig.1.6. Type-B sag occurs due to LG fault for star connected load as in 1.7.

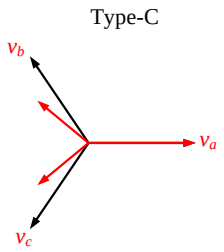


**Figure 1.8:** Type-C (Sag-C) during unsymmetrical-faults with phase jump.

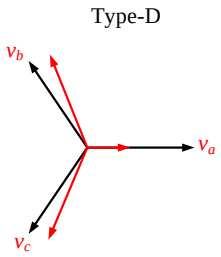


**Figure 1.9:** Type-D (Sag-D) during unsymmetrical-faults with phase jump.

Type-C sag occurs, due to LG fault for delta connected load and LL fault for star connected load with phase jump as in Fig.1.8. Type-D sag occurs, due to LL fault for delta connected load.

Type-E and F sag occurs due to LLG fault for star and delta connected load. While type-G sag also occurs for LLG fault but depends on the winding configuration of transformer.1.2 summarises the disused sags for different star and delta connected load.

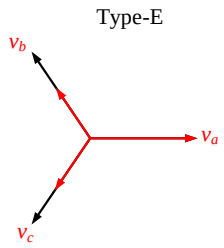


**Figure 1.10:** Type-E (Sag-E) during unsymmetrical-faults.

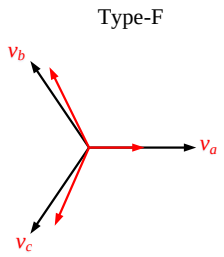


**Figure 1.11:** Type-F (Sag-F) during unsymmetrical-faults with phase jump.

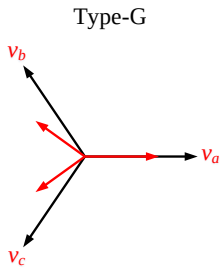


**Figure 1.12:** Type-G (Sag-G) during unsymmetrical-faults with phase jump.

Transformer winding configuration will cause a change in the type of sag from one voltage level to another. Balanced sags always remains the same neglecting the winding configuration. It only varies for unbalanced sags but can be summarised depending on type of transformer configuration. When both star points are grounded the sag on the secondary side is equivalent to primary side. Transformers remove the zero sequence voltage that means voltage of the secondary side is equivalent to voltage on primary side minus the zero sequence component. Usually for zero sequence component elimination, the transformer winding are usually star-star connected with one or both star points not grounded and the delta-delta transformer. While for the rest depending upon winding configurations the line and phase voltages vary. Table1.3 represents the the type of voltage dip on primary side w.r.t to secondary side for type 1, 2 and 3 transformers.

A grid-fault either on the HV or MV further propagates the fault to the LV. In order to describe this instability phenomena a simple distribution network is taken into account as in Fig.1.13 with loads A, B, C and D. The idea is to represent the instability phenomena irrespective of the transformer winding configuration. Where, the $\Delta_1$ gives -30° phase-jump and $\Delta_{11}$ gives +30° phase-jump to all the three phases. To that end, faults at HV, MV and LV will be discussed and how the

**Table 1.2:** Three-Phase balanced and unbalanced sags

| Fault Type | Star-connected Load | Delta-connected Load |
|---|---|---|
| LLL | Type A | Type A |
| LLLG | Type A | Type A |
| LLG | Type E | Type F |
| LL | Type C | Type D |
| LG | Type B | Type C |

**Table 1.3:** Co relation between the secondary-side voltage dip w.r.t to primary-side

| Transformer Type | Type A | Type B | Type C | Type D | Type E | Type F | Type G |
|---|---|---|---|---|---|---|---|
| Type 1 (YGyg) | A | B | C | D | E | F | G |
| Type 2 (Yy,Dd) | A | D | C | D | G | F | G |
| Type 3 (Yd,Dy) | A | C | D | C | F | G | F |

customers at A, B, C and D will experience the sag/dip. As represented in Fig.1.13 if we have a fault at position 1 (HV) will cause a deep sag for the substations connected to the faulted lines. Further, then this sag will propagate to the customers at A, B, C and D. The customers C and D will be out of power as there will be nothing to keep up the voltage. Next the fault at position 2 (MV) the customer B will experience a deep sag. It will not cause a much voltage drop for customer A as the impedance between the HV and MV is large enough to limit the voltage drop for the customer A. While, customer C and D will also experience voltage dip. Finally, fault at position 3 (LV) will cause a power outage for customers C and D, while customer B will experience a small voltage dip but customer A won't be affected at all. In conclusion, customers C and D will be the most affected as there will be nothing to keep up the voltage. This represents the need of certain functionalities from IBR at LV to support the grid during faults and also help during the grid voltage recovery. To counter this problem and to avoid system instability. Therefore a need to comply with certain grid requirements is required to avoid such scenarios.

## 1.3 Grid Requirements

In order, to comply with the grid requirements during faults. There are certain requirements or minimum functionalities that a RES should provide during such conditions. For LV the Energinet does not provide any requirements to support during grid faults. As discussed above section the LV side requires the need to support the grid during faults. The worst scenario was taken into account by

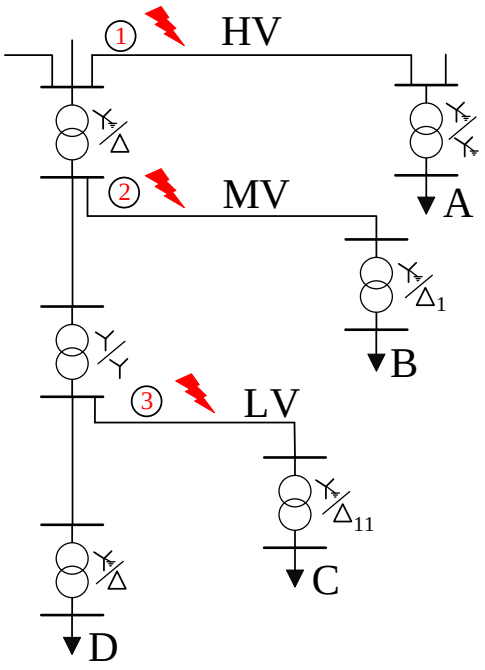


**Figure 1.13:** Distribution network with fault positions and load positions

taking different FRT requirements as represented in Fig.1.15 for MV. Where, $U_c$ is normal operating voltage (line-line voltage) and $U_{POC}$ is normal operating voltage at the POC.

Where, Fig.1.15 represents the worst case scenario with the voltage dip upto 10%, considering the worst case scenario would be $x$% that is severe faults. Zone A means the RES should remain connected to the grid and maintain normal production. Zone B is where the RES should remain connected to the grid and provide maximum voltage support with an injection of controlled reactive current. Finally, in Zone C disconnection of unit is allowed. It should be noted that the requirement implies to all the three-phases during fault. Individual unit is responsible for reactive current injection even at farm level. The reactive current ($I_Q$) injection with tolerance of +10% and -10% as in Fig.1.16. Full reactive current injection should be done below 0.5 $pu$ voltage drop. This condition is also applicable during normal operating conditions or even after disconnection of fault. It should be done in a controlled manner to avoid over-voltage and be within inverter limitation. It is worth mentioning that full priority will be given to reactive power injection during faults especially below 0.5$pu$ voltage drop.

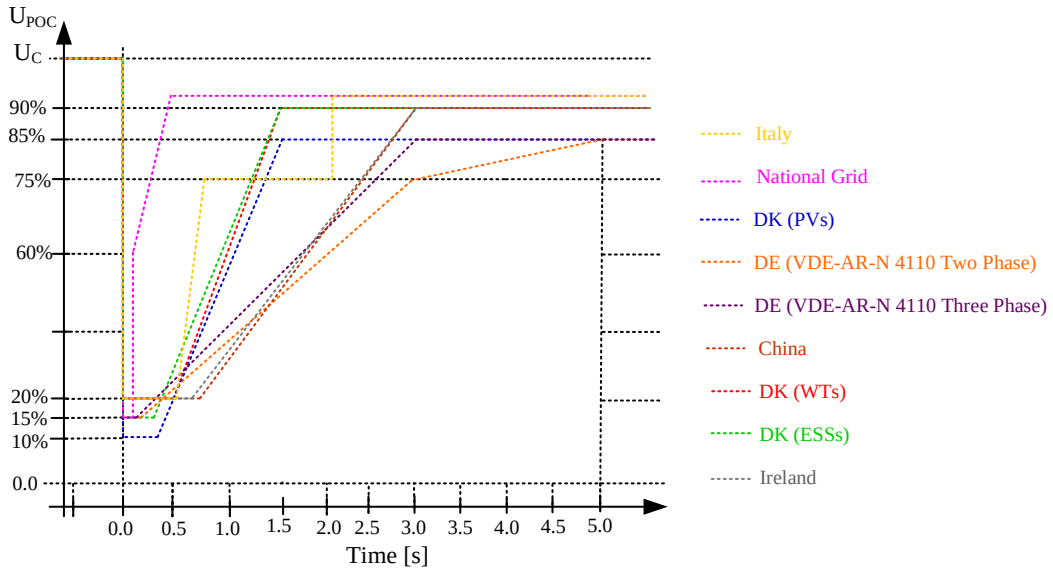


**Figure 1.14:** Fault Ride Through (FRT) requirements for China [23], DK PVs [**5**], DK WTs [**5**], DK ESSs [**5**], DE [24], National Grid (UK) [25] , Ireland [26] and Italy [27]

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## 1.4 State of the Art

Voltage dips experienced due to short-circuit grid faults have a impact over the industries especially adjustable speed drives, which trips off to avoid damage to power electronics components [28]. Classical methods like dynamic voltage restorer, static synchronous compensator were introduced to retain the grid voltage. Analysis of time domain and phasor sequence networks were introduced during voltage dips [29]. The grid current shoots up during such scenarios causing instability. Earlier, to encounter this series LC circuits were introduced to limit the fault current [30]. Further, analysis of Voltage source converter (VSC) is carried out to analyse the impact of faults in conventional *dq*-reference frame [31]. The proposed methodology in [31] represents the elimination of $2\omega$ **oscillation** from the power controller but as such LVRT studies were not carried out. DC-link voltage stability during faults was one of the main encountered issues in inverter drives [32]. To eliminate the influence of $2\omega$ oscillation and avoid overshoot of DC-link during LVRT conditions from the reference power ($P^*$) [33].

Analysis for injection of power during grid-faults utilising second-order generalised integrator (SOGI) as a band-pass filter (BPF) to extract the negative and positive sequence voltage. This is done to eliminate the power oscillations but introduces **highly distorted grid current** [34] and **poor power-quality** [35] . Studies for Type-3 WTs and wind farms were carried by following grid-compliance for LVRT condition [36–38],[39] and controlled reactive current injection [40] dur-

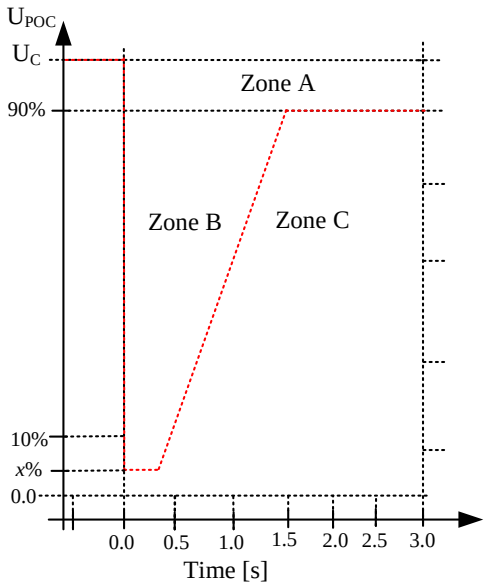


**Figure 1.15:** Low Voltage Ride Through (LVRT) requirements for the RES at LV grid.

ing faults. The injection of active current during faults needs to be limited to avoid loss of synchronism (LOS) of generation units [41]. Further, current injection method were proposed for avoiding the risk of over current during faults by providing correct reference currents from outer loops [42],[43]. The instability of PLL with the reference current generation in addressed through large signal model for PLL. However, this method considers the interaction of converter to the utility grid under weak grid conditions [44]. However, the above methods **neglected the DC-link dynamics**. In order to reduce the $2\omega$ oscillations during asymmetrical faults sequence extractor was utilised to generate the current references [45, 46] and a sample-hold method with sequence extractor for generating voltage reference values for each phase [47]. Low-pass filter (LPF) and Band pass filter (BPF) were also utilised, while sequence extraction but the phase-delay introduced by filters were neglected [48]. The aforementioned methods did not discus the phenomena of LOS as the they only consider reactive power injection during voltage dips.

To mitigate the LOS by avoiding power balance at the POC frequency based active current injection method is introduced depending upon the voltage dip [49]. PLL freezing during such events was on of the possibility to avoid LOS of generating unit [50–52]. **Equal Area Theorem (EAC)** is utilised for PLL in later phase to provide additional damping by taking the conditions before and after fault [53]. This would reduce the $2\omega$ oscillations from PLL during asymmetrical faults. Additional filtering units like Low-pass notch filter can be utilised to mitigate $2\omega$ oscillations but increases the complexity of PLL and introduces phase delay [54]. The major disadvantage of EAC is that it neglects the damping of PLL, which can

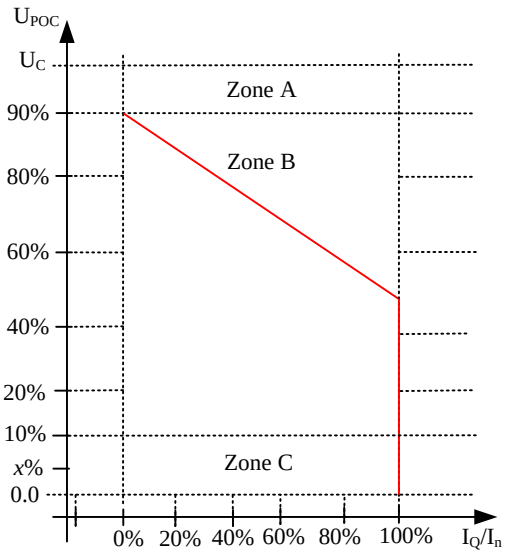


**Figure 1.16:** Reactive current ($I_Q$) and nominal current ($I_N$) injection during voltage dips.

be achieved by carrying small-signal stability of PLL to achieve stability [55]. A lot of attention is brought towards PLL to avoid LOS during short-term voltage stability. However, few methods were proposed by considering different variations in PLL for transient stability like adaptive damping [56], interaction with outer-loop [57] and phase portrait analysis [58]. It should be noted that the focus of this project on short-term voltage stability not long-term voltage stability [59]. Methods carried out for transient stability can be utilised for the synchronisation stability as well. Active power reference generation based on PLL frequency error [60] and actual output power [61] to avoid LOS and improve stability after fault is clear. Advance PLL and FLL (frequency-locked loop) like DSOGI (Double Second Order Generalised Integrator) [62] and DROGI-FLL (Dual Reduced-Order Generalised Integator-Frequency Locked Loop) [63, 64] were introduced for sequence extraction and frequency stability. Further, to extract positive and negative sequence of feedback-current DDSRF (Decoupled Double Synchronous Reference Frame) controller were used extensively to inject positive sequence current [62]. Stability of PLL to avoid LOS and provide voltage stability by maximum reactive power injection is one of the concern. This also introduces $2\omega$ oscillations in the injected active and reactive power during faults. The outer-loop controllers dynamics have been neglected, which have a high impact of the power injected. The term synchronisation and transient stability were mixed up quite often for short-term voltage stability events. The next section discusses the formulation of the problem.

**Table 1.4:** Modelling and control methods to achieve stability during grid faults

| Ref. | Year | Proposal / Drawbacks |
|---|---|---|
| [31] | 2005 | Mitigation of negative sequence current / FRT requirements not followed |
| [34] | 2007 | Instantaneous active reactive control / Distorted grid current. |
| [41] | 2009 | Active current injection limitation during voltage drop / DC-link neglected. |
| [42] | 2011 | Reference current generation to avoid over current / DC-link neglected. |
| [44] | 2012 | PLL based frequency stability / FRT requirements not followed. |
| [47] | 2013 | Generation of voltage references by sample-hold method / DC-link neglected. |
| [49] | 2014 | Frequency based active current injection / Converter current-limitations neglected. |
| [50] | 2014 | K-factor impact on system / line-impedance characteristics neglected. |
| [53] | 2014 | Large-signal stability analysing of PLL (EAC) / FRT requirements not followed. |
| [65] | 2015 | PLL stability considering impedance interaction / ([44]). |
| [54] | 2015 | Low-pass notch PLL for mitigation of $2\omega$ oscillations / Complex PLL. |
| [55] | 2016 | PLL bandwidth variation to achieve stability / FRT requirements not followed. |
| [56] | 2018 | Adaptive PLL damping method / DC-link neglected. |
| [57, 66] | 2018 | Interaction of active power loop with ROCOF / DC-link neglected. |
| [58] | 2018 | Phase portraits for PLL analysis / line-impedance characteristics neglected. |
| [67] | 2018 | Current vector alignment with line impedance to avoid LOS / DC-link neglected. |
| [60] | 2018 | Active power references based on PLL frequency error / STATCOM is included. |
| [51, 52] | 2018 | PLL freezing with phase compensation / Complex PLL system. |
| [68] | 2019 | Power-synchronization control for stability / DC-link neglected. |
| [61] | 2019 | Active power reference based on output power / DC-link neglected. |
| [62] | 2020 | Current reference generation based on DSOGI-PLL / Complex-PLL. |
| [63] | 2020 | DROGI-FLL for sequence extraction / Complex PLL methodology followed. |
| [64] | 2020 | Amalgamation of DROGI-FLL with PLL-freezing for frequency stability / [63]. |
| [69] | 2022 | Dual-sequence model to avoid LOS / Complex PLL methodology followed. |
| [70] | 2022 | Automatic voltage regulation with PLL / DC-link dynamics neglected. |
| [71] | 2022 | Large-signal stability analysis by Lyapunov method / Only PLL is considered. |

## 1.5 Problem Formulation

As discussed in last section, different methods were introduced to **avert the LOS** and **mitigate the** $2\omega$ **oscillations** during fault events. Most of the research ideas have been introduced on PLL to remain synchronised and provide voltage and frequency stability by injecting high reactive current for a single unit. Moving towards advance PLLs or FLLs always provide more stability but are **complex, high computational burden** such systems are not suitable for LV systems, which requires cheap and less complex solution. Moreover, **outer-loop controller dynamics** are neglected especially DC-link controller dynamics. It has a huge impact over

the active-current injection to maintain power-balance between the sending and receiving end. This brings us to one of the main issue that is misconception between the terms synchronization and transient stability. There is as if no definition neither for synchronization stability or transient stability. As per power-engineering task force, the classification of power-system stability can divided into five categories as represented in Fig.1.17 highlighted in blue oval. While, the red oval represents the terms considered for **synchronisation stability of a single-unit**. The focus of the project is only on **voltage-stability** and **frequency-stability**, where grid-faults are considered as short events (150 ms) this brings us to short-term voltage and frequency stability. Further, considered as synchronisation stability.

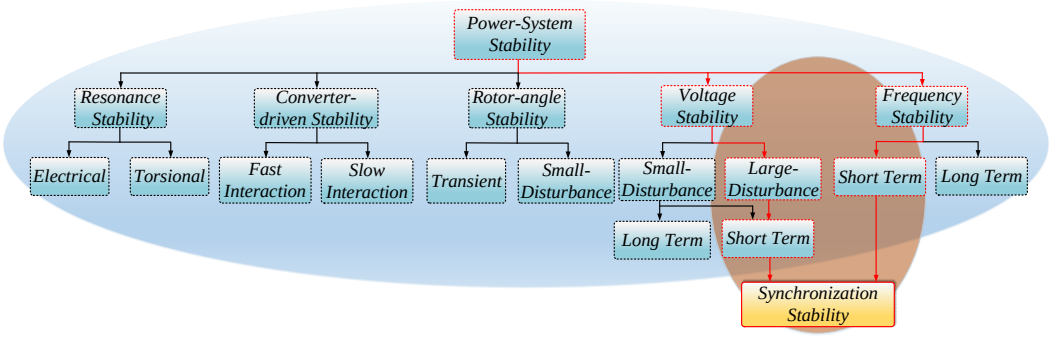


**Figure 1.17:** Classification of power-system stability [59] (blue oval) and synchronization stability (red oval).

However, when the voltage drop is very low at point of connection (POC) drop or rise in frequency can be observed depending upon active and reactive current injection during faults. While, for asymmetrical-faults the situation is quite worst as it leads to generation of $2\omega$ oscillations. An overview of the considered system is represented as in Fig.1.18. This bring us to the objectives of this project discussed in next section.

## 1.6 Project Objectives

The grid-following converters are at the risk of frequency instability under severe faults. Eventually, leading to loss of synchronisation of the unit from the grid. Losing a generating unit under such scenarios will also impact the frequency and voltage stability of the low-voltage grid. From recent studies synchronisation unit (PLL) has been identified as one of the aspects for loss of synchronization. To avert the loss of synchronization few methods like PLL freezing, advance frequency-locked loops have been implemented but have high computational burden and complex. While, PLL freezing method is tend to have a frequency drop during re-synchronization. This projects aims to study the impact of asymmetrical faults

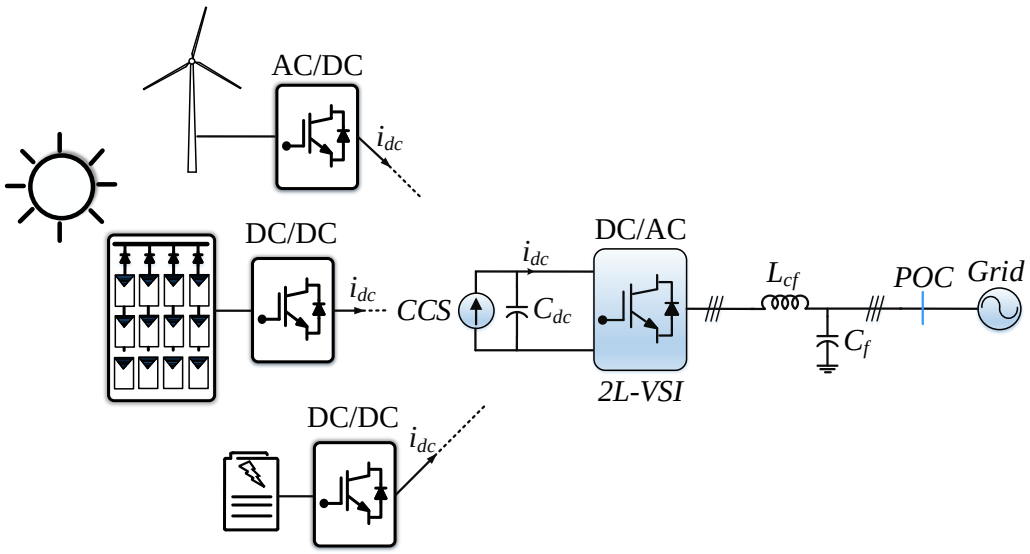


**Figure 1.18:** Generic overview of Grid-following (GFL) inverter with current controlled source (CCS).

initially by taking in account the impact of line impedance for a low-voltage network. Generation of second-harmonic oscillations during such events is also one issues having impact over the power quality. Eventually, those second harmonic oscillations will also disturb other generating units. However, there are as such no appropriate methods defined to mitigate or damp these oscillations. An attempt will be made to damp these oscillations under such events. This project will focus on two main questions:

- How to avert the LOS during severe grid-faults ?
- How to damp the generation of $2\omega$ oscillations during asymmetrical faults ?

The considered objectives will initially be analysed considering basic-control loops and modifications will be made by introducing **additional control strategies without neglecting basic control loops** as per requirement.

## 1.7 Methodology

The following methodology will be followed to reach the project objectives:

- Initially, as depicted in 1.18 considering only the grid-side converter (DC/AC) will be considered.

- The grid-side converter will be modeled in PLECS (Piecewise Linear Electrical Circuit Simulation).
- The control strategy will be implemented initially in s-domain (continuous domain) and then moved to z-domain (discrete domain).
- Once it is implemented fully in z-domain, results will be verified on the lab setup.

## 1.8 Scope and Limitations

The scope and limitations of this project are as follows:

- All dynamics corresponding to energy conversion are neglected in this project. This includes maximum power-point tracking for PVs and WTs and state of charge for ESSs. Only AC-side dynamics are considered to the grid. This can be assumed only grid-side converter control dynamics will be considered.
- The external network for a grid-connected converter is assumed to be Thevenin equivalent.
- Influence of power-system protection schemes associated with circuit breakers or any protection schemes is neglected.
- Grid impedance variation is neglected during this work.
- There is as such no requirement of transformers on LV network.

## 1.9 Content of Report

The report is divided into six chapters mainly. *Chapter-1* mainly discuses the motivation to carry out the project by considering real-life examples following with occurrence of power-system faults and propagation of faults. Grid-code requirements are addressed for LV networks. Finally, an overview of recent methodologies followed is discussed in state of the art. *Chapter-2* discuses the system characterization and the problem identification during faults from conventional method point of view. The current transfer limits for symmetrical faults are discussed considering different scenarios. *Chapter3* introduces solution for asymmetrical faults to provide flexible control during unbalanced grid conditions. *Chapter-4* and *Chapter-5* discus the solution for the studies carried out for off-line studies and experimental work. Finally, *Chapter-6* discusses the conclusion from the studies carried out reflecting the advantages of the solution proposed for asymmetrical faults and research perspectives.

# Chapter 2

# System Characterization

This chapter gives a brief overview of the control structure for the grid-following converter. The system description provides the small-signal analysis for the inner and outer loops. Then the description of low-voltage grid considered during studies is discussed. This brings us to the FRT implementation by conventional method for symmetrical and unsymmetrical faults. Finally, an in depth problem identification for symmetrical and unsymmetrical faults is carried out.

## 2.1 System Description

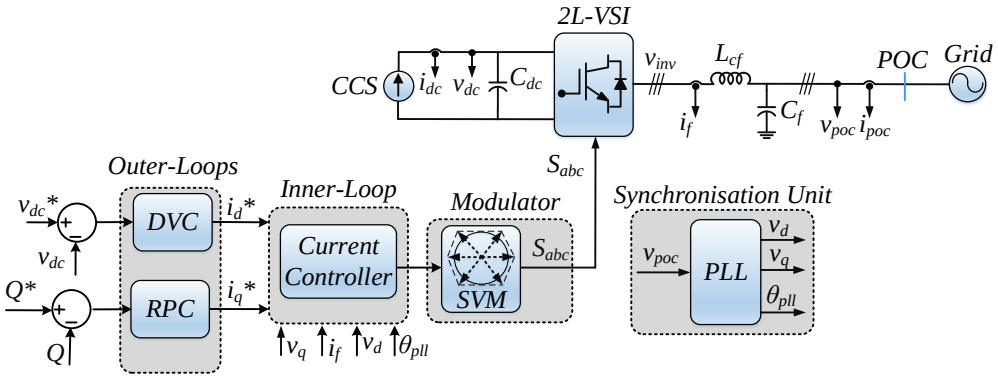


**Figure 2.1:** Schematic of grid-following converter with current controlled source (CCS) [72]

The general structure of grid-following converter is represented as in Fig.2.1 with synchronous reference frame control, also know as *dq* control. It consists of a synchronisation unit also called as phase-locked loop (PLL), which extracts the phase angle of grid voltages. The outer loop controllers mainly consists of Direct voltage controller (DVC) also called as dc-link voltage controller, which controls

the voltage across the dc-link capacitor ($C_{dc}$). While, the Reactive power controller (RPC) controls the injection of reactive power into the grid. Usually, the reactive power reference is set to zero, if the manual control is not allowed. Finally, the inner-loop consists of current controller, which can control both the converter current ($i_f$) or the grid current ($i_{poc}$) depending upon the type of control. However, converter current control is utilised due to protection requirements for converter side and compensating the reactive power generated by filter. Here, space vector modulation (SVM) is utilised as the modulation technique, which provides the switching pulses to the inverter together forming a closed-loop control. As we know, the $dq$ frame control is normally associated with the proportional-integral (PI) controllers as they satisfy the behaviour of regulating dc variables. Next, subsection discusses the small-signal stability analysis for the desired controllers.

### 2.1.1 Phase Locked Loop

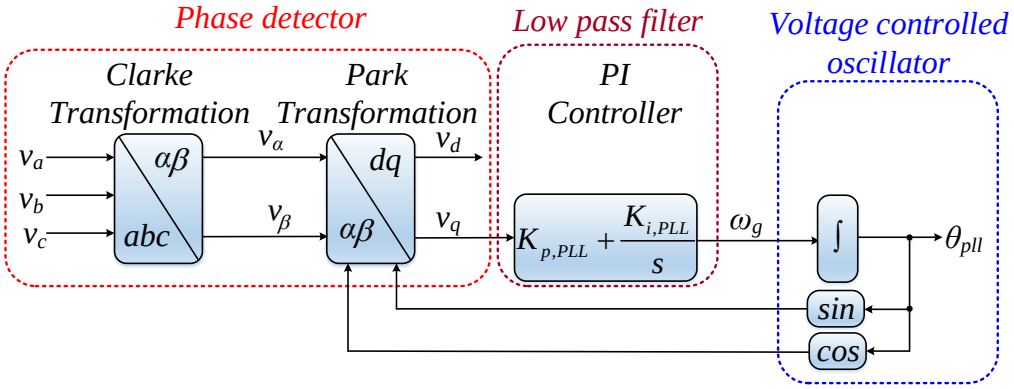


**Figure 2.2:** Structure of SRF-PLL used to estimate the phase angle of the POC (Point of Connection)

The basic structure of PLL consists of three main parts, i.e., a phase detector (PD), low-pass filter (LPF) and voltage controlled oscillator (VCO) as represented in Fig.2.2. In order to inject the desired active and reactive power into the grid. The three phase grid voltage ($v_a, v_b, v_c$) from the voltage at point of connection ($v_{poc}$) are transferred into two phase voltage ($v_\alpha, v_\beta$) by Clarke transformation. The Park transformation is applied to obtain the two phase voltage ($v_d, v_q$) in synchronous reference frame. The PI controller is adopted as a low-pass filter, where the $v_q$ is selected as the input. Then the $q-axis$ component is regulated to zero, so the grid voltage can be aligned to $d-axis$. Finally, the $dq-axis$ coupling can also be achieved. Once the grid frequency ($\omega_g$) is obtained the integrator is implemented to get the phase angle ($\theta_{pll}$) and reverted back to the Park transformation. The closed-loop transfer function can be written as is equ.2.1:

$$G_{2nd}(s) = \frac{2\zeta\omega_N s + \omega_N^2}{s^2 + 2\zeta\omega_N s + \omega_N^2} \tag{2.1}$$

where, $\zeta$ is the damping factor and $\omega_N$ is the natural oscillation frequency.The gains of PI controller can be calculate as in [73]:

$$K_p = \frac{9.2}{T_{set}} \tag{2.2}$$

$$T_i = \frac{T_{set}\zeta^2}{4.3} \tag{2.3}$$

The damping factor is chosen as 0.707, since it provides overshoot less then 5% in step response. The settling time ($T_{set}$) is chosen as $100ms$ [73]. Finally, the $K_P$ and $T_i$ can be calculated as in equ.2.2 and equ.2.3.

### 2.1.2 Current Controller (CC)

In order to control the current injected into the grid. The converter current or grid current can be controlled with a negative feedback loop. Here, the converter current is controlled in synchronous reference frame as PI controller [74]. As we know the response time of inner-current loop is much faster then the outer-loops. The disturbance due to grid-voltage (feed-forward) are neglected. The relation between the converter current and voltage can be defined as in equ.2.4.

$$G_{i_f(s)} = \frac{i_f(s)}{v_{inv}(s)} = \frac{s^2 + w_{LC}^2}{L_{cf}s(s^2 + w_r^2)} \tag{2.4}$$

where,

$$w_r = \sqrt{\frac{L_{cf} + L_{gf}}{L_{gf}L_{cf}C_f}} \tag{2.5}$$

and

$$w_{LC} = \frac{1}{\sqrt{L_{gf}C_f}} \tag{2.6}$$

Since, the grid side filter ($L_{gf}$) is not present. So, the $\omega_r$ (resonance angular frequency) and $\omega_{LC}$ (resonant angular frequency) of the filter can't be calculated. This would avoid the complexity of the third order plant as in equ.2.4. The plant function will be considered equivalent to an inductor. For the worst case scenario resistance of the filter cab be neglected, but a proper step-response can't be achieved. To fulfil this requirement resistance is taken as $0.1pu$ of the $L_{cf}$. A transport delay is induced by the PWM technique, by making a sample delay caused

due to digital implementation. Symmetrical PWM is utilised here that means single sample within a switching period. In total we have a delay of $1.5T_s$ with a delay of one switching period in symmetrical PWM. The open-loop transfer function can be represented as in equ.2.7.

$$G_{OL}(s) = \frac{K_{p,CC}s + K_{i,CC}}{s} \frac{1}{1 + 1.5T_s s} \frac{1}{R_f + L_{cf}s} \tag{2.7}$$

It is worth mentioning that the $d$ axis and $q$ axis have the same dynamics. The tuning of $d$ axis is only considered here. The small-signal control block is represented as in Fig.2.3.

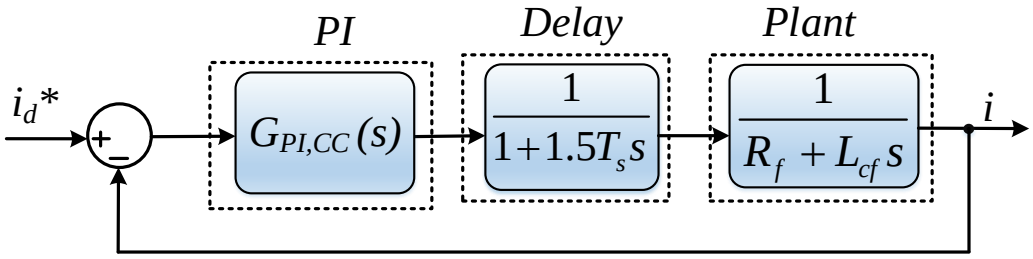


**Figure 2.3:** Small-signal control block diagram for the current-controller [75]

Finally, in order to calculate the $K_{p,CC}$ (proportional gain of CC) and $K_{i,CC}$ (integral gain of CC). Either modulus optimum can be utilised by zero-pole cancellation or Matlab toolbox, Sisotool. The relative stability is considered with gain margin larger than $6dB$ and phase margin greater than 45 degree in open-loop [76]. Finally, the bandwidth of the CC should be between 500 to 1000 Hz for the considered switching frequency in closed-loop. The bode-plot for open-loop appendix update needed .

### 2.1.3 Direct-Voltage Controller

The outer voltage loop also called as DC link voltage controller or Direct voltage controller. The DC link is not constant and needs to be regulated properly to achieve a proper power balance between both the converters. The minimum dc link voltage should be greater then the three-phase line to line peak voltage on AC side. The dc link is not constant and time varying. In order to regulate a constant dc voltage across the DC link capacitor ($C_{dc}$), voltage controller needs to be employed. The rule of thumb is that the bandwidth of dc link voltage controller should be 10 times slower then the current controller to achieve a decoupled control [77].

In order to establish the relationship between the dc and ac side instantaneous power is considered. Usually, converter losses are neglected during the design

of controller. The overall block diagram is represented as in Fig.2.4. The voltage controller consists of the PI controller with $K_{p,dc}$ (proportional controller) and $K_{i,dc}$ (integral controller). Then the closed-loop transfer function of current controller is considered, it can also be taken as equivalent to 1 as the inner-current loop are faster then outer loops. Finally, the DC capacitor plant transfer function is considered as $1/(Cs)$. The open-loop transfer function is represented as in equ.2.8.

$$G_{OL_{dc}}(s) = \frac{K_{p,dc}s + K_{i,dc}}{s} \frac{G_{ol(s)}}{1 + G_{ol}(s)} \frac{1}{Cs} \tag{2.8}$$

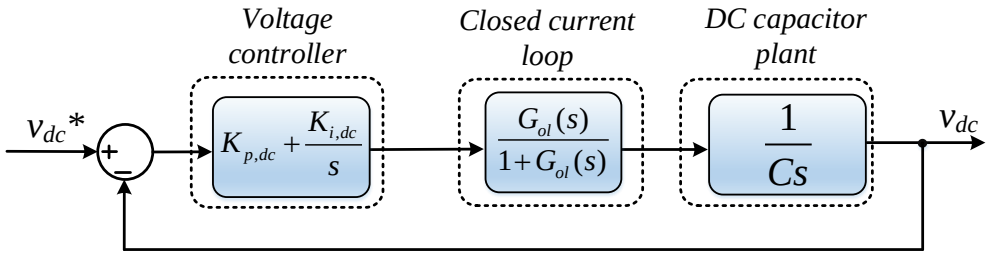


**Figure 2.4:** Small-signal control block diagram for the DC-link voltage controller [78]

The tuning of PI controller is implemented using symmetrical optimum [79]. This method can give a initial point following the relative stability giving the required gain margin and phase margin. The open-loop and closed-loop bode plot with step response is discussed in Append.A.

### 2.1.4 Reactive-Power Controller

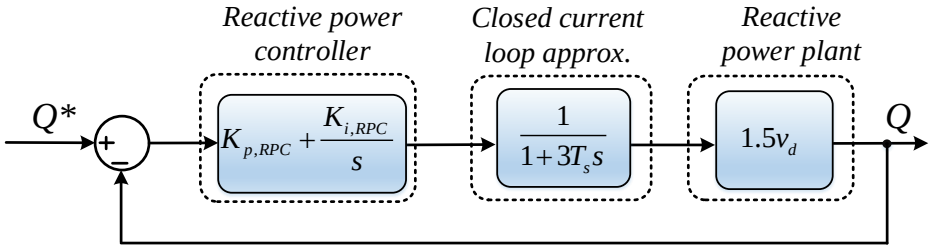


**Figure 2.5:** Small-signal control block diagram for the Reactive power controller [80]

The reactive-power controller (RPC) is for providing the manual reactive power as per requirement. However, it can also be utilised as a part of Q-V droop control. In this project it is neglected. The block diagram for RPC is represented as in

Fig.2.5. The closed-loop transfer function of current controller is approximated or it can also be taken as equivalent to 1 as the outer-loops are slower than the inner current loop. On the other hand, the plant transfer function can be derived as in equ.2.9.

$$Q = \frac{3}{2}(v_q i_d - v_d i_q) = -1.5 v_d i_q \tag{2.9}$$

The plant transfer function can be roughly estimated as $1.5v_d$. It should be noted that the bandwidth of RPC should be lower then DC-link voltage controller to achieve a decoupled control between the DVC and the RPC. The open and closed loop response with bode-plot is discussed in Append.A.

## 2.2 LV Grid for Case Study

This section discuses the details of LV distribution grid used for further studies. As schematic diagram of one of the feeder connected to MV network is considered as represented in Fig.2.6.

The schematic consists of HV grid (G1) with nominal voltage of 60 kV. The short circuit ratio (SCR) is set to 30 with X/R of 10. The source impedance parameters were neglected and considered as default. A step-down transformer (T1) is connected with delta-Y configuration. The nominal power of T1 is 25 MVA with resistance and leakage inductance equivalent to 0.0041104 $pu$ and 0.102918 $pu$. The magnetisation resistance and inductance were taken as default. L1 is a 12 kV MV cable of 10 km length with zero ($Ro$) and positive ($R1$) sequence resistance of 0.508 $\Omega/km$ and 0.0841 $\Omega/km$. The zero ($Xo$) and positive ($X1$) sequence reactance is taken as 0.31 $\Omega/km$ and 0.068 $\Omega/km$. A step-down transformer (T2) is connected having delta11-Y configuration with nominal power of 630 kVA. The winding resistance and leakage inductance were taken as 0.009 $pu$ and 0.0471487 $pu$. Two loads of 500 kW (Load 1) and 10 kW (Load 2) were connected at 0.4 kV bus and POC as represented in Fig.2.6. Line (L2) is a LV between the T2 and POC of 3 km with positive sequence resistance (0.3208 $\Omega/km$), reactance (0.075398 $\Omega/km$) and capacitance (0.56 $microF/km$). It should be noted that the LV line is an underground cable, which are highly resistive with pi-section line. Finally, an IBR is connected at the POC. This concludes the overall parameters of the considered system.

The fault is considered a **km** away from the POC at $S_1$ on LV cable as represented in Fig.2.7. The simplified schematic is represented as in Fig.2.8. The external grid is considered as Thevenin equivalent grid ($v_g$). The line impedance is taken as ($Z_s$), while source impedance ($Z_G$) is taken as default. The next section discuses the fault ride through implementation. It should be noted that to vary the voltage dip fault-impedance will be varied.

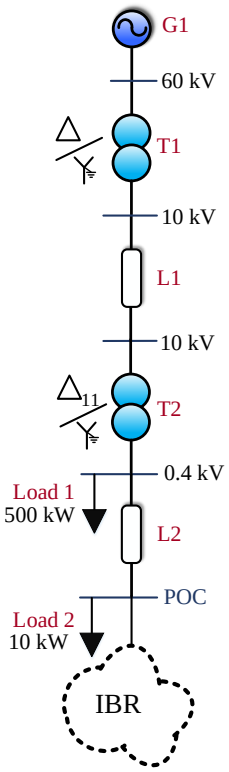


**Figure 2.6:** System considered for fault scenario considering line ($L1$, $L2$) and grid ($G1$) impedance in Thisted, Denmark [81, 82]

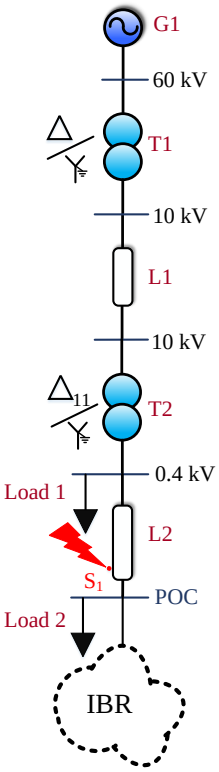


**Figure 2.7:** Point of fault ($S_1$) for the considered system from the POC.

## 2.3 Fault Ride through Implementation

In order to comply with the grid requirements as discussed in Ch.1. To remain connected and support the grid during faults. The conventional method is represented as in Fig.2.9. Where $I_{gm}$ is the maximum is the maximum reactive current as per grid code requirements. As per the requirement 1 $pu$ reactive current needs to be injected during 0.5 $pu$ voltage drop. During such scenarios reactive current is given priority over active current to support the voltage. The conventional method to generate active and reactive current references are represented as in Fig.2.9. The reactive current references is dependent on voltage drop. The active current drops down to zero or low depending upon capability of converter limits. The excessive power flowing to the DC side is usually dissipated by the chopper resistance. As in Fig.2.9, the reactive current reference ($i_q^*$) is dependent upon voltage drop as per grid profile. If the converter current is controlled that adds an additional reactive

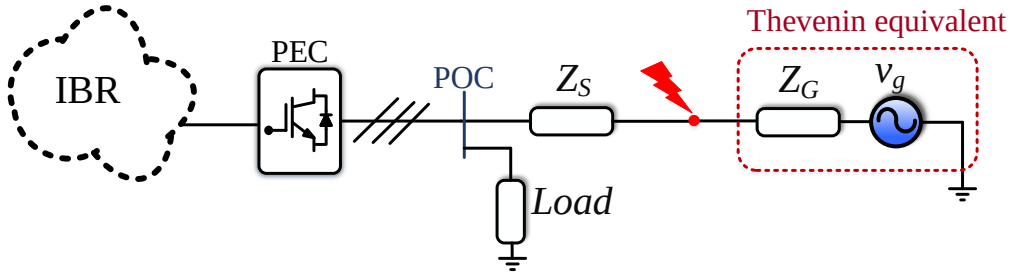


**Figure 2.8:** Simplified system considering the line impedance ($Z_S$) from the point of fault ($S_1$).

power or pre-fault current. Consideration of additional pre-fault current is omitted from the method. The DC link voltage regulation is neglected in recent work during symmetrical faults. This will be taken under consideration during problem identification in next section. The remaining active current capacity ($I_{active-limit}$) is generally calculated based on the maximum current capacity ($I_{max}$) of the converter under normal conditions.

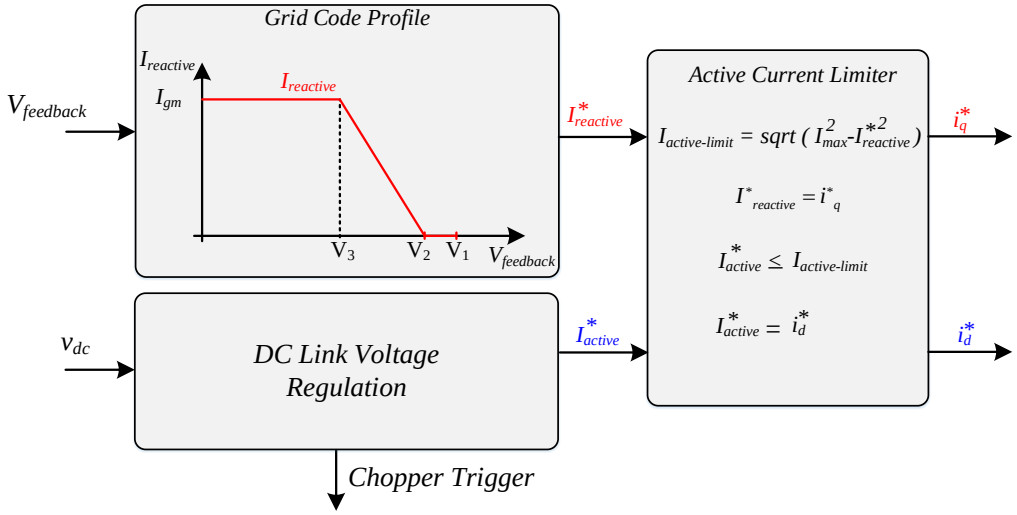


**Figure 2.9:** Conventional method for current reference generation during fault

The current reference generation as per the grid code are represented as in Fig.2.10. The maximum reactive current ($I_{gm}$) is equivalent to $I_{max}$ at $V_3$ that means maximum reactive current injection by the converter. However, a grid-side converter can go up to 1.2 $pu$, an additional 0.2 $pu$ can be considered for safety margin. The remaining 0.2 $pu$ can be utilised as the remaining active current injection during faults. The shaded areas in Fig.2.10 represents that active current injection can vary depending upon the grid code requirements.

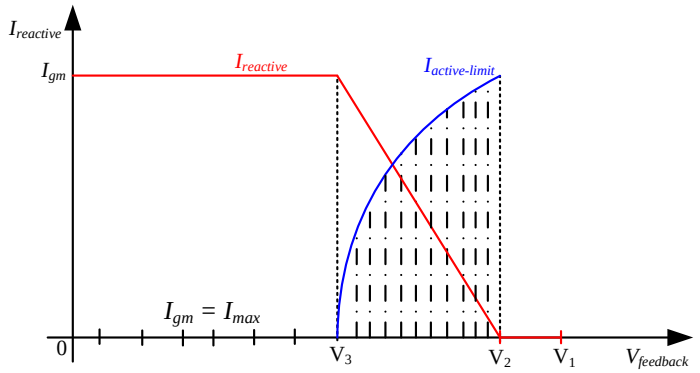


**Figure 2.10:** Current references with conventional method ($I_{gm}$=$I_{max}$)

During a positive sequence voltage drop or voltage drop at $v_{poc}$, the RES are required to stay connected to the grid. To fulfill this requirement positive-sequence reactive current needs to be injected to provide voltage stability. This implies during both symmetrical and asymmetrical faults. As per Energinet, the reactive current ($\Delta I_{reactive}$) injection depending upon voltage drop ($\Delta v$) can be represented as in Fig.2.11. Where, k is the factor dependent upon grid code requirements. Here, $k$ equivalent to 2 is considered with the objective of full reactive current injection during 0.5 $pu$ voltage drop. However, $k$ can be varied but should be less then equal to 2. The grid codes are only prepared for positive sequence voltage drop for symmetrical faults but during asymmetrical faults negative sequence voltage also arises. There as such no separate requirements for negative sequence reactive current injection for asymmetrical faults because it has adverse effects like power oscillations, non-faulty phase rises over nominal value leading to Over-Voltage Ride Through (OVRT) [83].

To fulfill the strict grid code requirements as in 2.11. The Conventional Method (CM) as represented in Fig.2.12 following the reactive current injection. Where, dead zone is applied to avoid any voltage support for 0.1 $pu$ voltage drop or rise [8]. While, the saturation block is applied to avoid entering into overexcited operation. In conclusion, the $I^*_{reactive}$ can be depicted as in equ.2.10. This is also called as Fault-Ride Through (FRT) block as it provides voltage stability. Next section discuses about the problem identification during asymmetrical and symmetrical grid faults as per CM.

$$\Delta I^*_{reactive} = k.(\Delta v - 0.1) \tag{2.10}$$

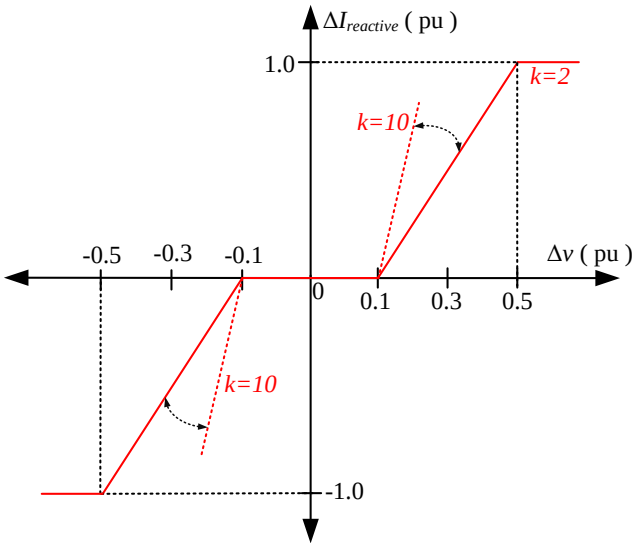


**Figure 2.11:** Reactive current injection during faults as per [8]

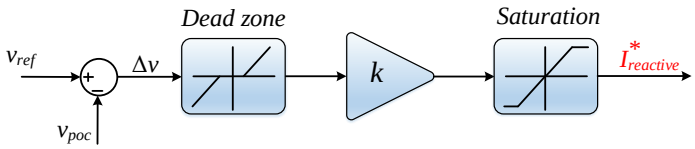


**Figure 2.12:** Reactive current injection as per Fig.2.11

## 2.4 Problem Identification during FRT

This section discusses about the identification of problem by CM during asymmetrical and symmetrical grid faults. It also gives a short overview of how CM is implemented following grid code requirements.

### 2.4.1 Asymmetrical Faults

The CM employing complying with grid-code requirements is represented as in Fig.2.13. The converter-current reference generator (CCG) block is responsible for varying $i_{dc}$ during faults.

The CM method injects only positive sequence current during asymmetrical faults thus boosting the voltage for all the phases including non-faulty phase. This would create a voltage boost for the non-faulty phases at the point of fault [83]. However, zero sequence current and voltage will be attenuated due to dYN transformers present in the system as they provide grounding for the grid side [84].

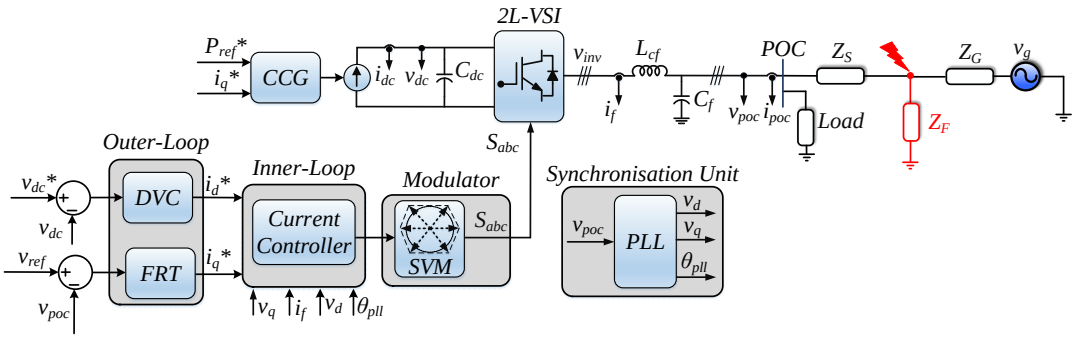


**Figure 2.13:** Aggregated model for asymmetrical faults

Detailed analysis of asymmetrical fault by CM method is discussed in Chapter4 as Case-02. The next sub-section discusses the loss of synchronisation during symmetrical faults.

### 2.4.2 Symmetrical Faults

During symmetrical faults the voltage dip across all the phases is same. This eliminates the necessity of sequence extraction methodology. Loss of Synchronizm (LOS) has been reported in recent studies [84]. This may vary from the type of system and the line impedance parameters taken into consideration. LOS is highly dependent on the type of current injection during faults. It is worth mentioning that reactive current injection will be given priority during faults. This will be discussed in detail by considering different scenarios during severe faults. It should be noted that the point of fault ($v_f$) remains the same.

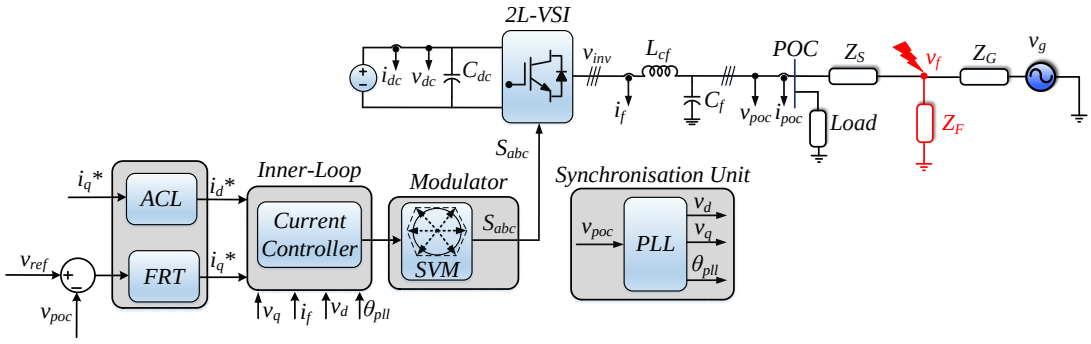


**Figure 2.14:** Aggregated model for symmetrical faults

## 2.5 Loss of Synchronization during Symmetrical Faults

This section discuses the LOS during severe symmetrical faults. Two different cases will be considered with different current injection angle to analyse the limits to avert LOS. The fault-impedance ($Z_f$) is kept low to create a severe fault.

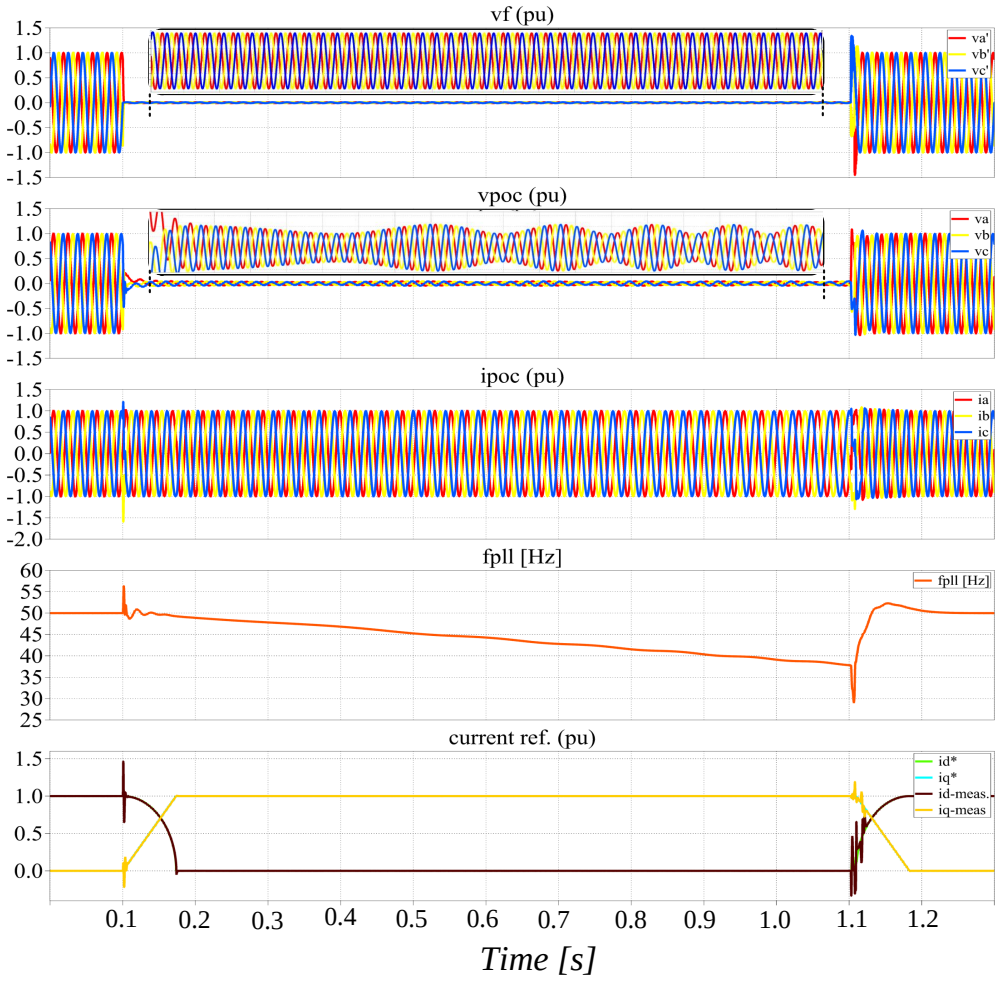


**Figure 2.15:** LOS-Frequency Fall

Initially, full reactive-current ($i_q$) is injected with $v_f$ equivalent to 0.035 $pu$ as represented in Fig.2.15. It can be noticed that the frequency of PLL ($f_{pll}$) starts falling depicting the loss of synchronisation from the network. During the frequency fall the voltage instability occurs at $v_{poc}$. However, the voltage at $v_{poc}$ is greater than that of $v_f$ due to the presence of line-impedance. An envelope like pattern formed at $v_{poc}$ is due to PLL instability [85] with respect to frequency fall.

The $v_f$ is still synchronised with 50 Hz, while $v_{poc}$ is not this represents the impact of line-impedance during severe faults. It is worth mentioning that the active current is brought down to zero as per FRT strategy. This is the point where CM method fails to provide voltage stability leading to LOS. Only pure reactive current is injected the current angle ($\theta_1$) is equivalent to 90°.

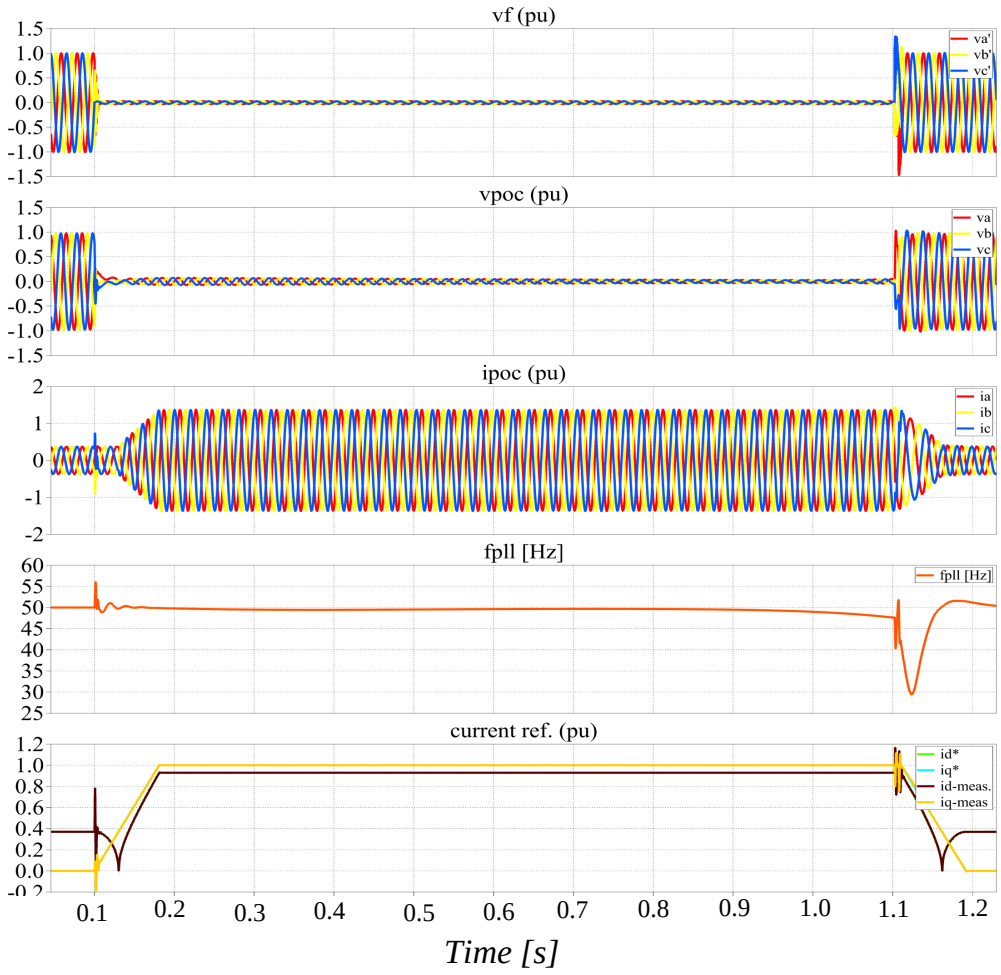


**Figure 2.16:** Synchronised to 50 Hz (No LOS)

Recent studies have shown that injection of adequate active current can avert LOS. A similar case study is created, where the $v_f$ is still equivalent to 0.035 $pu$ during fault. The active current injection ($i_d$) is increased to avoid voltage and frequency instability as represented in Fig.2.17. The grid-current ($i_{poc}$) is increased up to 1.35 $pu$ for a short period of time. This case represents that injection of active current can avert LOS during severe faults. The current angle ($\theta_1$) was found

out to be 46.86° as high active current is injected. It is worth mentioning that for the presented case as in Fig.2.17 the system is synchronised to 50 Hz and no voltage instability would occur. This section can be concluded with the help of Fig.2.17 representing the physical understanding of LOS. It can be noticed that the LOS occurs only for the unit, while the main/rest grid continues to remain synchronised at 50 Hz. Next section provides a clear overview of the active and reactive current transfer limits with respect to line impedance characteristics.

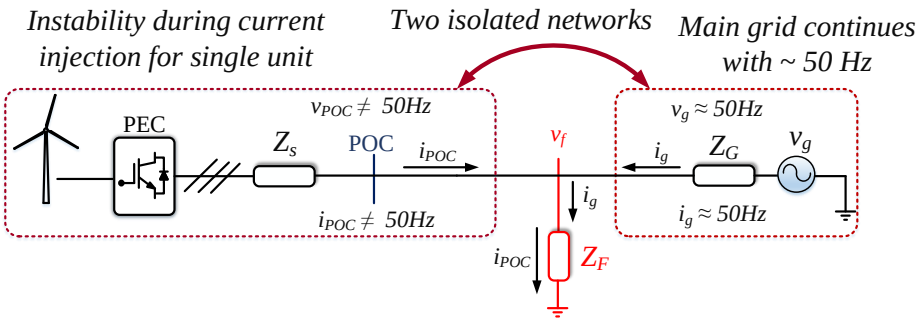


**Figure 2.17:** Physical understanding of LOS for single-unit

## 2.6 Active and Reactive Current Transfer-limits during Symmetrical Faults

This section deals with the active and reactive transfer limits during severe symmetrical faults. The correlation between the sending end bus (*POC*) and receiving end bus ($v_f$) with respect to line impedance ($Z_s$) as a function of voltage magnitude will be discussed. The derived limits will provide a better understanding at which point does the LOS occurs. It should be noted that the impact of $Z_s$ will be studied carefully as discussed in previous section. To avoid complexity *POC* will be considered as $v_s$ and $v_f$ as $v_r$. Emphasize will not be given to the capacitance ($C_s$) considered for line impedance because it provides a couple of voltage boost. However, the variation of the derived limits due to capacitance can be considered as a part of future work.

### 2.6.1 Power Flow on a line considering resistance

In this section power-flow for a line considering the line resistance and inductance will be discussed. Active ($P_s$) and reactive ($Q_s$) power flow equation can be derived as practised in [84]. This will be considered as the base case in this project.

$$P_s = \frac{v_s v_r X_s}{Z_s^2} sin\theta_s + \frac{v_s^2 R_s}{Z_s^2} - \frac{v_s v_r R_s cos\theta_v}{Z_s^2} \tag{2.11}$$

$$Q_s = \frac{v_s X_s}{Z_s^2} - \frac{v_s v_r X_s cos\theta_v}{Z_s^2} - \frac{v_s v_r R_s sin\theta_v}{Z_s^2} \tag{2.12}$$

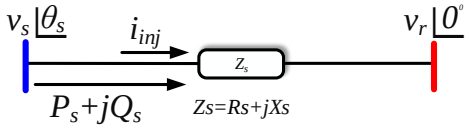


**Figure 2.18:** Single line diagram for the resistive/inductive line

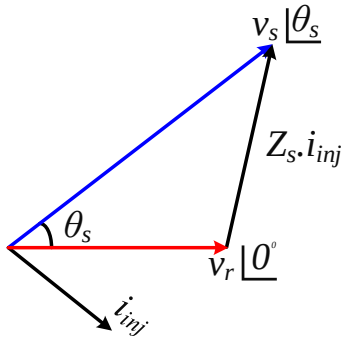


**Figure 2.19:** Phasor diagram for the resistive/inductive line

The derived equ.2.11 and 2.12 can be considered to understand the non-transferable active and reactive power during symmetrical faults. Considering a scenario where the $v_r$ is equivalent to zero. So, the derived $P_s$ and $Q_s$ are represented as in equ.2.13.

$$v_r = 0 \Rightarrow P_s = \frac{v_s^2 R_s}{Z_s^2}; Q_s = \frac{v_s^2 X_s}{Z_s^2} \Rightarrow \frac{P_s}{Q_s} = \frac{R_s}{X_s} \tag{2.13}$$

It can noticed that when the $v_r$ is zero the power from sending end will be dissipated in the form of active ($i_{inj}^2 R_s$) and reactive ($i_{inj}^2 X_s$) power losses of the line. However, when $v_s > v_r$ a minimal amount of active power flow can be done to compensate for the losses arising due to reactive power flow. This statement is only valid for severe faults. In conclusion, the line impedance dictates the relationship between the $v_s$ and $v_r$. This will help us understanding the active and reactive current transfer limits.

### 2.6.2 Current-Angle Characteristics

The current injection defines the process to avert the LOS during severe faults. Active and reactive current transfer limits will be derived from equ.2.11 and equ.2.12. The derived equ.2.14 and equ.2.15 will form a base case scenario for deriving the current transfer limits. Considering the current flow from $v_s$ to $v_r$ with the considered line impedance the single-line diagram can be represented as

$$i_{active} = \frac{P_s}{v_s} = \frac{v_r X_s sin\theta_s}{Z_s^2} + \frac{v_s R_s}{Z_s^2} - \frac{v_r R_s cos\theta_v}{Z_s^2} \tag{2.14}$$

$$i_{reactive} = \frac{Q_s}{v_s} = \frac{v_s X_s}{Z_s^2} - \frac{v_s X_s cos\theta_s}{Z_s^2} - \frac{v_r R_s sin\theta_v}{Z_s^2} \tag{2.15}$$

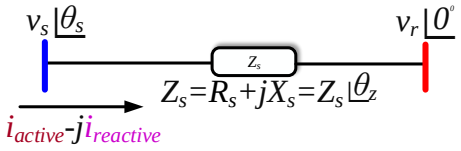


**Figure 2.20:** Single line diagram for the resistive/inductive line with current flow

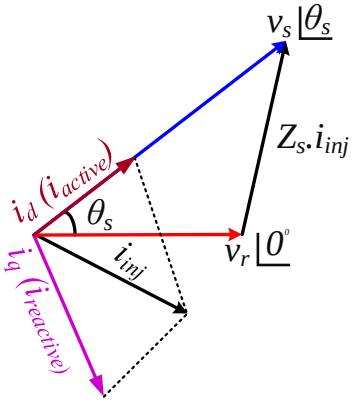


**Figure 2.21:** Phasor diagram for the resistive/inductive line with current flow

Considering a scenario for severe fault, where $v_s > 0$ and $v_r$ is equivalent to zero. The $i_{active}$ and $i_{reactive}$ current can be obtained as in equ.2.16. It is worth mentioning that active and reactive current flowing creates losses on the resistance and reactance of the line. Under severe symmetrical faults when $v_r$ is very low that means not equivalent to zero. This states that a fixed amount of active and reactive current injection is required depending upon $\frac{X_s}{R_s}$ characteristics to avert the LOS.

$$v_r = 0 \Rightarrow i_{active} = \frac{v_s R_s}{Z_s^2}; i_{reactive} = \frac{v_s X_s}{Z_s^2} \Rightarrow \frac{i_{active}}{i_{reactive}} = \frac{R_s}{X_s} \tag{2.16}$$

The dependency of current transfer limits with $\frac{X_s}{R_s}$ characteristics will be discussed further.

### 2.6.3 Derivation of Current Transfer Limits

Power-flow (power-angle) and current-angle characteristics were discussed in the above section. These sections were only limited to $v_s$ and $v_r$ with $\frac{X_s}{R_s}$ characteristics. It cannot provide the operating points for active and reactive current injection for low voltage magnitude. The single line diagram is represented as in Fig.2.22. The current phasor for the single line diagram is represented in Fig.2.22.

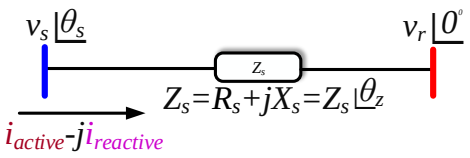


**Figure 2.22:** Single line diagram for derivation of current transfer limits

It is worth mentioning that when $v_r$ drops to very low voltage the voltage and frequency instability occurs at the $v_s$. It is more important to analyse the converter active and reactive current injection limits at $v_s$ because $v_r$ remains stable. The current phasor methodology is represented in Fig.2.23 with $i_d$ aligned to $v_s$ on horizontal axis. The current angle $\theta_1$ is the angle between the $i_d$ and resultant vector $i_{inj}$. To analyse the current injection limits with respect to current-angle ($\theta_1$). We consider that the $v_r$ magnitude remains constant. The $v_r$ can be found out by locating the tip of $Zi_{inj}$ on the circle with $v_s$ as reference axis. On the other hand the angle of $v_s$ with respect to $Zi_{inj}$ will be kept constant as $\theta_1 - \theta_z$ knowing the fact magnitude of $v_s$ is varied. It should be noted that impedance angle $\theta_z$ is less than 90 degrees as it consists of resistive component. Further, to analyse the limits $\theta_1$ will be varied from 0° to 360°.

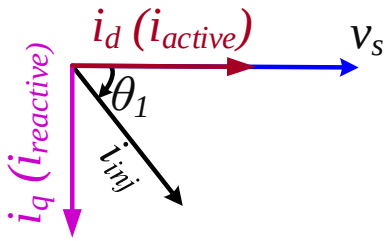


**Figure 2.23:** Methodology to derive current phasor transfer limits

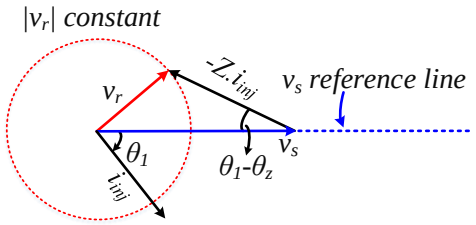


**Figure 2.24:** Current phasor to derive the limits

### Pure Reactive Current ($\theta_1 = 90°$)

The methodology discussed in Fig.2.24 will be considered as base case scenario for all the derived limits. Initially, the reactive current injection starts considering the ramp rates with a low current magnitude as represented in Fig.2.25. The maximum reactive current injection is achieved that is $i_{inj} = i_{limit}$ the angle between the $v_s$ and

$v_r$ becomes 90° as represented in Fig.2.26. The vector $Z_s i_{limit}$ is largest during this point considering the fact $v_r$ is constant. It can be better explained with the help of Fig.2.27, if the magnitude of $Z_s i_{inj}$ becomes greater than the limit the vector cannot be located between $v_s$ and $v_r$. In order to achieve this situation a larger voltage magnitude $v_r$ is required which is not possible. This states that if $i_{inj}$ is greater then the $i_{limit}$ operating point cannot be located then it is just out of transfer limits.

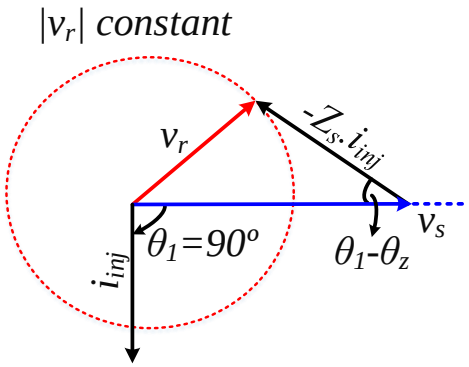


**Figure 2.25:** Current transfer during pure reactive current injection ($\theta_1 = 90°$)

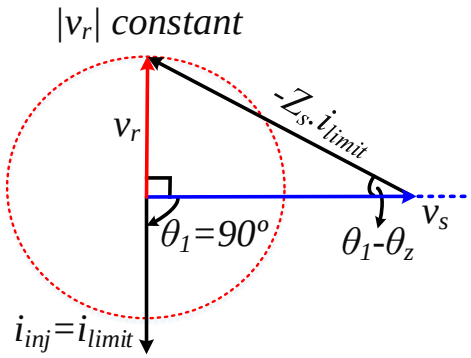


**Figure 2.26:** Current transfer limit at $\theta_1 = 90°$

The current transfer limit can be derived as in equ.2.17. The derived limit can be represented in Fig.2.28

$$\theta_1 = 90° \Rightarrow v_r = Z_s i_{limit} sin(\theta_1 - \theta_z) \Rightarrow i_{limit} = \frac{v_r}{R_s} \tag{2.17}$$

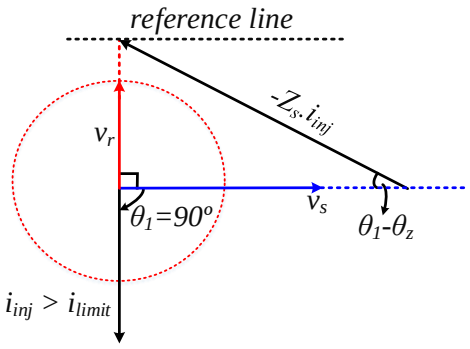


**Figure 2.27:** Out of transfer limits $i_{inj} > i_{limit}$

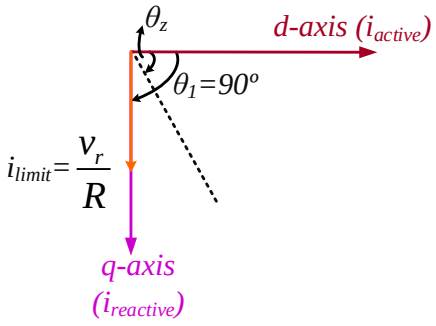


**Figure 2.28:** Current phasor for the derived limit

The derived condition violated under severe symmetrical faults, when the receiving end voltage is very low. Only pure reactive current injection would lead to LOS.

**Current magnitude limit $90° > \theta_1 > \theta_z$**

This type of scenario is considered when active current is injected up to a certain limit to avoid LOS. The current magnitude is increased keeping $\theta_1$ constant as represented in Fig.2.29. The point when $i_{inj}$ is equivalent to $i_{limit}$ that means largest current magnitude as represented in Fig.2.30 $v_s$ will be orthogonal to $v_r$. It is worth mentioning that the $i_{limit}$ cannot be greater than the $i_{inj}$ the operating point cannot be located.

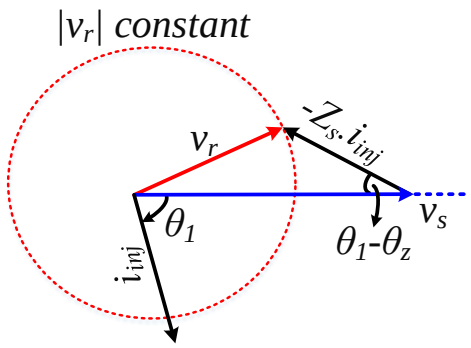


**Figure 2.29:** Current transfer $90° > \theta_1 > \theta_z$

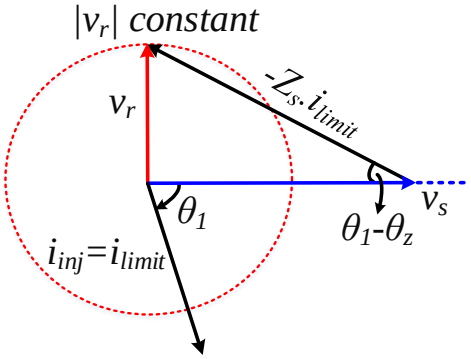


**Figure 2.30:** Current transfer limit $90° > \theta_1 > \theta_z$

The current transfer limit for this case can be derived as in equ.2.18.

$$90° > \theta_1 > \theta_z \Rightarrow v_r = Z_s i_{limit} sin(\theta_1 - \theta_z) \Rightarrow i_{limit} = \frac{v_r}{Z_s sin(\theta_1 - \theta_z)} \tag{2.18}$$

The derived limit can be represented as in Fig.2.31. The blue shaded area represents the operating point. The orange line denotes the $i_{limit}$ from the derived expression.

**Current magnitude limit $\theta_1 = \theta_z$**

This scenario is less likely to occur when the current angle ($\theta_1$) is equivalent to line impedance angle ($\theta_z$) as represented in Fig.2.32. This scenario does not have a current transfer limit but an operating point. If the current magnitude ($i_{inj}$) is increased then the magnitude of $v_s$ is also increased but cannot be increased due

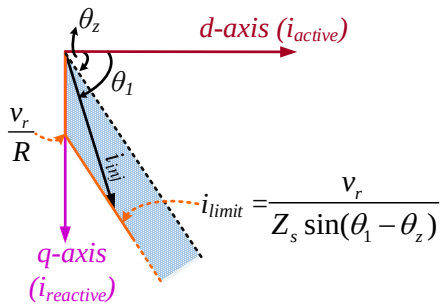


**Figure 2.31:** Current phasor for the derived limit ($90° > \theta_1 > \theta_z$)

to voltage limitations on $v_s$. It also depends upon converter current limitation to avoid undesirable trip. The derived limit is represented as in Fig2.33.

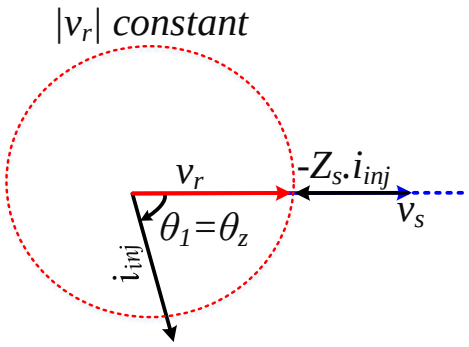


**Figure 2.32:** Current transfer $\theta_1 = \theta_z$

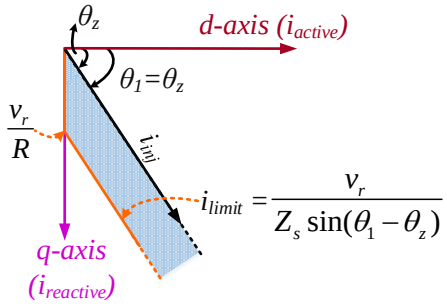


**Figure 2.33:** Derived limit for $\theta_1 = \theta_z$

**Current magnitude limit $\theta_z > \theta_1 > 0°$**

This scenario can occur if the impedance angle ($\theta_z$) is greater than current angle ($\theta_1$) as represented in Fig.2.34. The current magnitude is maximum ($i_{inj} = i_{limit}$) the phase difference between $v_s$ and $v_r$ is 90° as represented in Fig.2.35. This case scenario is different as little high active current is being injected that means magnitude of $v_s$ will be decreased as the active current contribution goes higher. In simple words just opposite case scenario when pure reactive current is injected because there the magnitude of $v_s$ will be increased.

Following similar methodology as in previous cases the current limit can be derived as in equ.2.19.

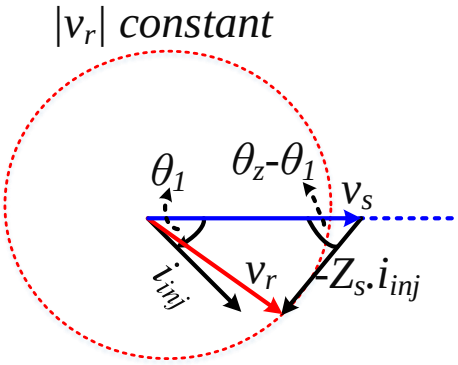


**Figure 2.34:** Current transfer $\theta_z > \theta_1 > 0°$

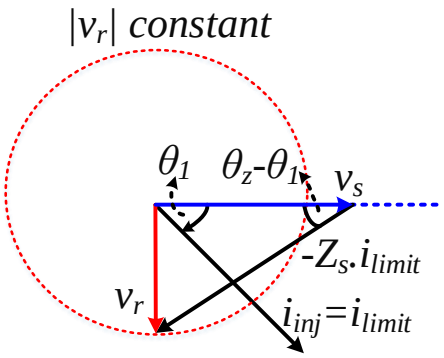


**Figure 2.35:** Current transfer limit $\theta_z > \theta_1 > 0°$

$$90° > \theta_1 > \theta_z \Rightarrow v_r = Z_s i_{limit} sin(\theta_z - \theta_1) \Rightarrow i_{limit} = \frac{v_r}{Z_s sin(\theta_z - \theta_1)} \tag{2.19}$$

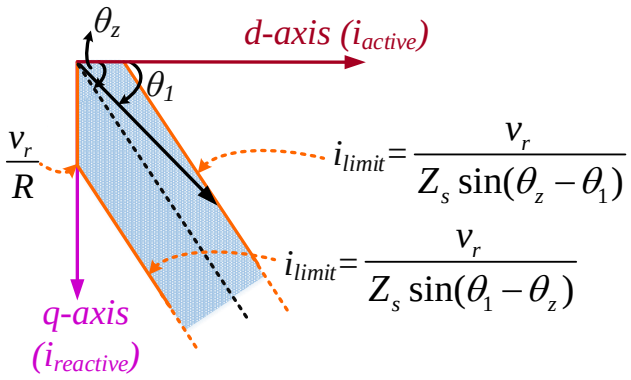


**Figure 2.36:** Current phasor for the derived limit ($90° > \theta_1 > \theta_z$)

805 **Pure active current $\theta_1$ = 0°**

The current angle ($\theta_1$) is set to zero that means pure active current injection. Initially, the current magnitude will be increased keeping the $\theta_1$ constant as represented in Fig.2.37. The current magnitude reaches largest within the operating point as $i_{inj}$ is equivalent to $i_{limit}$. The $v_s$ and $v_r$ will have a 90° phase difference

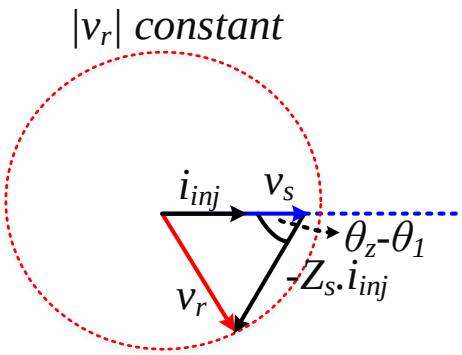


**Figure 2.37:** Current transfer $\theta_1 = 0°$

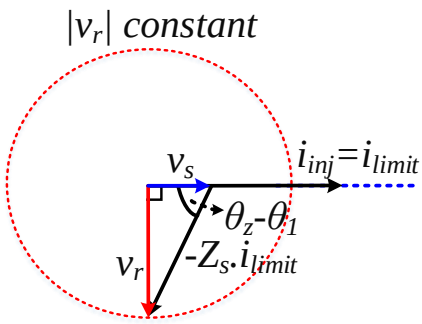


**Figure 2.38:** Current transfer limit $\theta_1 = 0°$

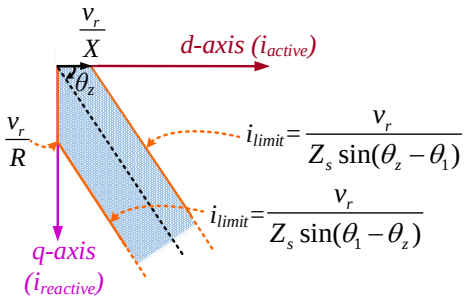


**Figure 2.39:** Current phasor for the derived limit ( $\theta_1 = 0°$)

between them as in Fig.2.38. As already discussed voltage magnitude of $v_s$ will drop down to zero due to pure active current injection.

The similar methodology can be followed to derive the limits for this case as in equ.2.20.

$$\theta_1 = 0° \Rightarrow v_r = Z_s i_{limit} sin(\theta_z - \theta_1) \Rightarrow i_{limit} = \frac{v_r}{X_s} \tag{2.20}$$

The operating point cannot be found if the $I_{active}$ is greater than the derived limit. Injecting highly active current also arises high reactive ($i^2 X_s$) loss in the line, decreasing the reactive power at $v_r$. An attempt will be made to propose novel control methods to avoid LOS during severe faults.

## 2.7 Summary

A brief overview of inner and outer loop controls were discussed with small-signal stability of each controller. Major contribution is the problem identification during asymmetrical faults and severe symmetrical faults by conventional method. Case studies were considered taking into account different current angle to avert LOS. Finally, active and reactive current transfer limits were derived for the symmetrical faults considering line impedance characteristics. Next chapter disuses the modified method proposed for asymmetrical faults to attenuate second-harmonic oscillations.

# Chapter 3

# Flexible Positive and Negative Sequence Control for Asymmetrical Faults

This chapter aims to provide a solution for asymmetrical faults. The problem identification for asymmetrical faults is discussed in the previous chapter. Major drawback of the conventional method is the injection of grid current of same magnitude and no attenuation of second harmonic oscillations due to unbalanced grid voltages during asymmetrical faults. This can create an over voltage on the non-faulty phase also. Recent proposed methodologies as discussed briefly in the state of the art tend to neglect **DC-link voltage control**, use **complex filters**, neglect **converter current reference generation** and use of **complex PLL strategy** for sequence extraction. The modified method proposed in this chapter focuses on **avoiding** complex sequence extraction methods and consider DC-link voltage control. It should be noted that the modified methodology will **consider DC-link dynamics** with converter current reference generation and **low computational burden**. Thus making it suitable for LV grid integrated systems.

### 3.0.1 Instantaneous Power Theory

The basic $p-q$ theory will be utilised for three phase voltages and current $abc$ to $\alpha\beta 0$. Then instantaneous power theory will be come in to derive the sequence component of voltage and current. Initially, clarke transformation will be followed for the transformation of voltage and current in $abc$ to $\alpha\beta 0$. $v_{poc}$ will consists of each phase voltage $v_a, v_b, v_c$ by applying Clarke transformation we get $v_\alpha, v_\beta, v_0$ as in equ.A.1. Similarly, $i_\alpha, i_\beta, i_0$ can also be obtained as in equ.A.2 by Clarke transformation.

It should be noted that no zero sequence current exists in a three-phase three wire systems. The zero sequence voltage can also be neglected. The simplified equation are represented as in equ.3.1 and equ.3.2.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3.1}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.2}$$

The instantaneous voltage and current vector can be defined from the $\alpha$ and $\beta$ components from Clarke transformation. The voltage vector ($e$) and current vector ($i$) can be represented as in equ.3.3 and equ.3.4. Similarly, active power can also be calculated in $\alpha\beta$ components

$$e = v_\alpha + jv_\beta \tag{3.3}$$

$$i = i_\alpha + ji_\beta \tag{3.4}$$

The three-phase instantaneous active power ($p_{3\phi}$) during steady state or transients can be depicted as in equ.3.5 and is equivalent to $\alpha\beta$ components neglecting the zero sequence component.

$$p = v_a i_a + v_b i_b + v_c i_c = v_\alpha i_\alpha + v_\beta i_\beta \tag{3.5}$$

The instantaneous complex power can be derived from equ.3.3 and equ.3.4. It is jus the product of $e$ and conjugate of the current vector ($i^*$) as in equ.3.6. The real power is $p$, imaginary power $q$ and "." represents the dot product.

$$s = e.i^* = (v_\alpha + jv_\beta)(i_\alpha - ji_\beta) = (v_\alpha i_\alpha + v_\beta i_\beta) + j(v_\beta i_\alpha - v_\alpha i_\beta) \tag{3.6}$$

Further, $q$ can be written as in equ.3.7 and "$\perp$" represents the perpendicular. It corresponds to the product of positive-sequence voltage and a positive sequence current lagging (inductive).

$$q = v_\perp.i = \frac{1}{\sqrt{(3)}}[(v_a - v_b)i_c + (v_b - v_c)i_a + (v_c - v_a)i_b] \tag{3.7}$$

with

$$v \perp = \frac{1}{\sqrt{3}} \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} v \tag{3.8}$$

### 3.0.2 Symmetric-Sequence based Instantaneous Power

Sequence extraction for unbalanced phases is proven to be one of the way for right sequence injection during faults. The positive and negative sequence component of voltage and current can be defined as in equ.3.9 and equ.3.10.

$$v = v^{+} + v^{-} \tag{3.9}$$

$$i = i^{+} + i^{-} \tag{3.10}$$

where $v^{+,-} = [v_a^{+,-}, v_b^{+,-}, v_c^{+,-}]^T$ and subscripts "+", "-" denotes the positive and negative sequences. Similarly, for current sequence $i^{+,-} = [i_a^{+,-}, i_b^{+,-}, i_c^{+,-}]^T$. Finally, the instantaneous power based on equ.3.7 and equ.3.5 with sequence components can be written as in equ.3.11 and equ.3.12.

$$p = v.i = (v^{+} + v^{-}).(i^{+} + i^{-}) = v^{+}i^{+} + v^{-}i^{-} + v^{+}i^{-} + v^{-}i^{+} \tag{3.11}$$

$$q = v_{\perp}.i = (v_{\perp}^{+} + v_{\perp}^{-}).(i^{+} + i^{-}) = v_{\perp}^{+}i^{+} + v_{\perp}^{-}i^{-} + v_{\perp}^{+}i^{-} + v_{\perp}^{-}i^{+} \tag{3.12}$$

The active and reactive power derived consists of constant term with the same sequence. The second harmonic terms are derived from the dot product of voltage and current with different sequences. Next section discusses the Flexible Positive and Negative Sequence Control (FPNSC) to regulate the positive and negative sequence voltage and current during asymmetrical fault.

### 3.0.3 FPNSC

The FPNSC method is derived from the PNSC (Positive Negative Sequence Control) [73]. The advantage of this method is to provide current references by including flexible coefficients $(k_1, k_2)$ [73]. Expanding the method from PNSC strategy the current vector $i_P^*$ (active reference current) and $i_Q^*$ (reactive reference current) can be derived as in equ.3.13 and equ.3.14.

$$i_P^* = P^* \left( \frac{k_1 v^{+}}{|v^{+}|^2} + \frac{(1-k_1)v^{-}}{|v^{-}|^2} \right) \tag{3.13}$$

$$i_Q^* = Q^* \left( \frac{k_2 v_{\perp}^{+}}{|v^{+}|^2} + \frac{(1-k_2)v_{\perp}^{-}}{|v^{-}|^2} \right) \tag{3.14}$$

Further, expanding the FPNSC method can be written in $\alpha\beta$ frame in order to provide right current references to the current controller

$$i_{\alpha}^{*} = P^{*}\frac{2}{3}\left(\frac{k_1 v_{\alpha}^{+}}{(v_{\alpha}^{+})^2+(v_{\beta}^{+})^2}+\frac{(1-k_1)v_{\alpha}^{-}}{(v_{\alpha}^{-})^2+(v_{\beta}^{-})^2}\right)+Q^{*}\frac{2}{3}\left(\frac{k_1 v_{\beta}^{+}}{(v_{\alpha}^{+})^2+(v_{\beta}^{+})^2}+\frac{(1-k_1)v_{\beta}^{-}}{(v_{\alpha}^{-})^2+(v_{\beta}^{-})^2}\right) \tag{3.15}$$

$$i_{\beta}^{*} = P^{*}\frac{2}{3}\left(\frac{k_1 v_{\beta}^{+}}{(v_{\alpha}^{+})^2+(v_{\beta}^{+})^2}+\frac{(1-k_1)v_{\beta}^{-}}{(v_{\alpha}^{-})^2+(v_{\beta}^{-})^2}\right)+Q^{*}\frac{2}{3}\left(\frac{k_1 v_{\alpha}^{+}}{(v_{\alpha}^{+})^2+(v_{\beta}^{+})^2}+\frac{(1-k_1)v_{\alpha}^{-}}{(v_{\alpha}^{-})^2+(v_{\beta}^{-})^2}\right) \tag{3.16}$$

### 3.0.4 Sequence Extraction

The sequence extraction for unbalanced phases can be achieved by conventional method without using any second-order generalised integrator (SOGI) [86]. The instantaneous positive ($v_{abc}^{+}$) and negative ($v_{abc}^{-}$) sequence voltage can be denoted as in equ.3.17 and equ.3.18.

$$v_{abc}^{+} = \begin{bmatrix} v_a^{+} \\ v_b^{+} \\ v_c^{+} \end{bmatrix} = \left[T_{+}\right] v_{abc} \tag{3.17}$$

$$v_{abc}^{-} = \begin{bmatrix} v_a^{-} \\ v_b^{-} \\ v_c^{-} \end{bmatrix} = \left[T_{-}\right] v_{abc} \tag{3.18}$$

where $[T_{+}]$ and $[T_{-}]$ can be defined as equ.3.19 and equ.3.20. $a$ equivalent to $e^{j\frac{2\pi}{3}}$.

$$[T_{+}] = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix} \tag{3.19}$$

$$[T_{-}] = \frac{1}{3}\begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix} \tag{3.20}$$

Further, by using Clarke transformation $[v_{\alpha\beta}]$ for both positive $[v_{\alpha\beta}^{+}]$ and negative $[v_{\alpha\beta}^{-}]$ sequence voltage can be obtained.

where $v_{\alpha\beta} = [T_{\alpha\beta}]\, v_{abc}$ with $[T_{\alpha\beta}]$ can be denoted as in equ.3.21.

$$[T_{\alpha\beta}] = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{3.21}$$

Finally, $v_{\alpha\beta}^{+}$ and $v_{\alpha\beta}^{-}$ can be obtained as in equ.3.22 and equ.3.23.

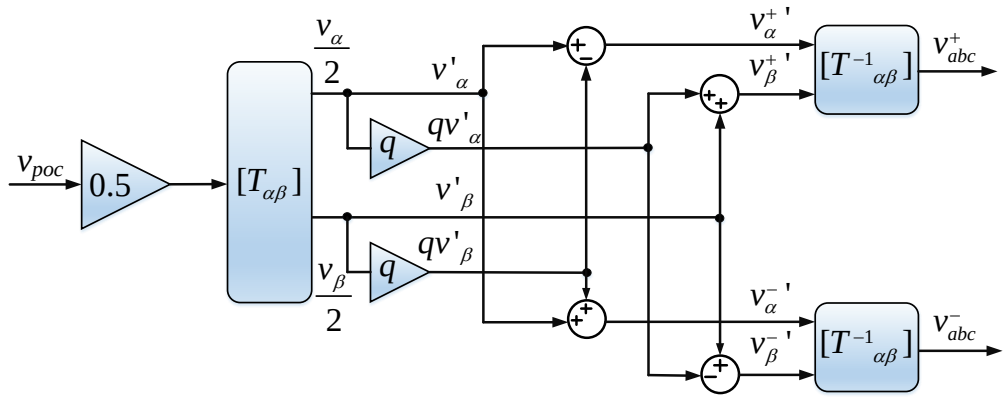


**Figure 3.1:** Positive and negative sequence extractor by conventional method [86]

$$v^+_{\alpha\beta} = [T_{\alpha\beta}][T_+]v_{abc} = \frac{1}{2}\begin{bmatrix}1 & -q\\ q & 1\end{bmatrix} v_{\alpha\beta} \tag{3.22}$$

$$v^-_{\alpha\beta} = [T_{\alpha\beta}][T_-]v_{abc} = \frac{1}{2}\begin{bmatrix}1 & q\\ -q & 1\end{bmatrix} v_{\alpha\beta} \tag{3.23}$$

Where, $q = e^{-j\frac{\pi}{2}}$ will act as a phase-shift time-domain operator. The positive and negative sequence of voltage can be obtained in both $\alpha\beta$ or $abc$ reference frame as in Fig.3.1.

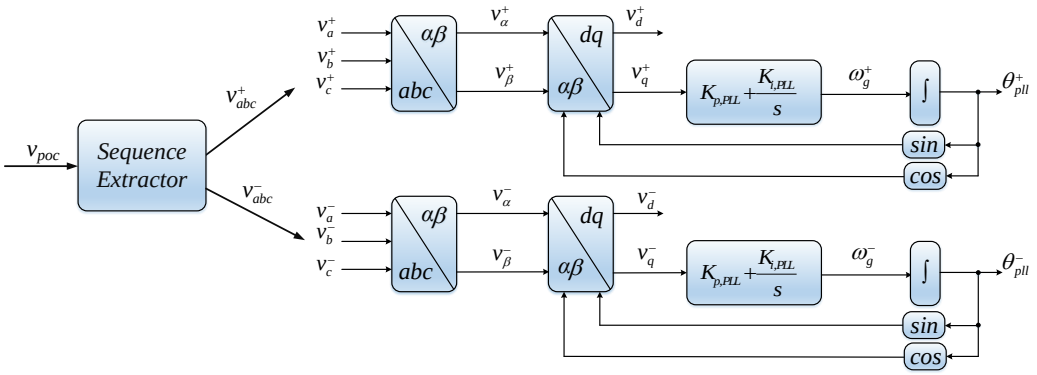


**Figure 3.2:** Dual SRF PLL for positive $v^+_d, v^+_q$ and negative $v^-_d, v^-_q$ sequence extraction

Finally, in order to achieve positive sequence angular position ($\theta^+_{pll}$) and negative sequence angular position ($\theta^-_{pll}$) dual SRF PLL will be utilised to generate the desired responses for desired positive and negative sequence generation from unbalanced voltage.

### 3.0.5 Converter Current Limitation

The FPNSC strategy focuses on the injection of unbalanced current injection. The currents may be different from phase to phase. Acquiring such strategies can result in an undesired trip due to over current protection for each phase. Eventually resulting in unintended disconnection from the network. Therefore accurate control of power converter is necessary during such strategy. It should be noted that the phase current does not exceed the permitted limit, $P$ and $Q$ should be maximised to converter limits and mitigation of unbalanced voltage should be achieved. In order to achieve locus of the current vector analysis will be carried out as practised in [73]. We know that $i^*$ can be divided into active ($i_P^*$) and and reactive ($i_Q^*$) current as in equ.3.24.

$$i^* = i_P^* + i_Q^* = P^* \left( \frac{k_1 v^+}{|v^+|^2} + \frac{(1-k_1)v^-}{|v^-|^2} \right) + Q^* \left( \frac{k_2 v_\perp^+}{|v^+|^2} + \frac{(1-k_2)v_\perp^-}{|v^-|^2} \right) \tag{3.24}$$

To avoid complexity equ.3.24 can be rewritten as in equ.3.25.

$$i^* = i_P^* + i_Q^* = C_1.v^+ + C_2.v^- + C_3.v_\perp^+ + C_4.v_\perp^- \tag{3.25}$$

Where,

$$C_1 = \frac{P^* k_1}{|v^+|^2}; C_2 = \frac{P^*(1-k_1)}{|v^-|^2}; C_3 = \frac{Q^* k_2}{|v^+|^2}; C_4 = \frac{Q^*(1-k_2)}{|v^-|^2} \tag{3.26}$$

It should be noted that the voltage vector $v^+$ and $v^-$ and current vector $i_P^*$ and $i_Q^*$ are developed in stationary reference frame [73]. $v^+$ gives rise to the positive sequence voltage vector and $v^-$ to the negative sequence voltage vector resulting in an ellipse in $\alpha\beta$ domain. Further, addition of $C_1.v^+$ and $C_2.v^-$ will form an ellipse for $i_P^*$ as in Fig.3.3. Similarly, $C_3.v_\perp^+$ and $C_4.v_\perp^-$ will form an ellipse for $i_Q^*$ as in Fig.3.4.

The $i_P^*$ and $i_Q^*$ ellipse will be aligned with locus of $v$ and $v_\perp$ as the constant terms $C_1$, $C_2$, $C_3$ and $C_4$ will scale it as represented in Fig.3.5. The resultant vector $i^*$ will be formed, if the voltage phase are neglected. The voltage phase are shifted by an angle $\delta$ will result in an ellipse as represented in Fig.3.6.

These derived locus provides us the limitation over each phase current. In order to limit the reference current a relationship between the active and reactive power references to the converter current taking into the account the flexible coefficients. The maximum converter limitations can be derived as practised in [87]. Initially, the $\alpha\beta$-axis voltage can be depicted as in equ.3.27.

$$(V^+)^2 = (v_\alpha^+)^2 + (v_\beta^+)^2; (V^-)^2 = (v_\alpha^-)^2 + (v_\beta^-)^2; \tag{3.27}$$

The phase shifted angle $\delta$ can be found as in equ.3.28.

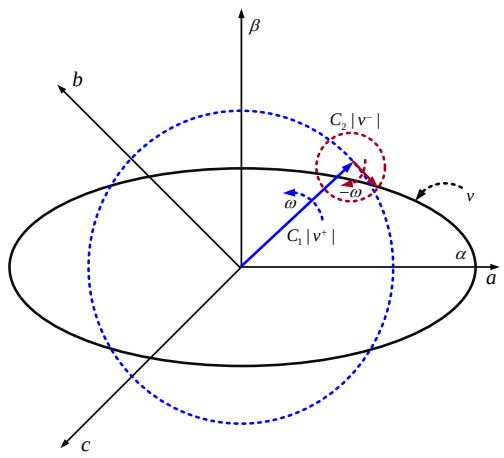


**Figure 3.3:** Loci for active current $i_P^*$

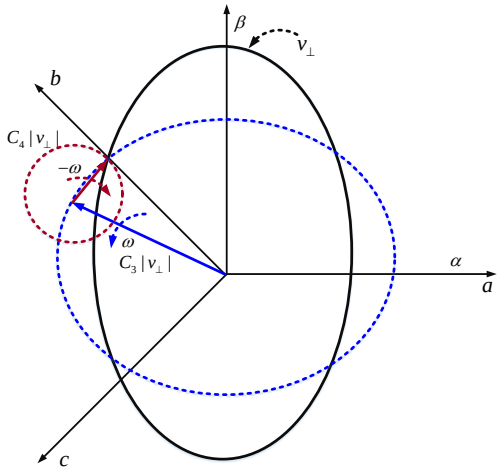


**Figure 3.4:** Loci for reactive current $i_Q^*$

$$cos(\delta) = \frac{v_\alpha^+ v_\alpha^- - v_\beta^- v_\beta^+}{V^+ V^-}; \tag{3.28}$$

The next step is to calculate the sequence current amplitude as in equ.3.29 and equ.3.30 as adopted in [87]

$$I_p^+ = \frac{2k_1 P^*}{3V^+}; I_p^- = \frac{2(1-k_1)P^*}{3V^-} \tag{3.29}$$

$$I_q^- = \frac{2k_2 Q^*}{3V^+}; I_q^- = \frac{2(1-k_2)Q^*}{3V^-} \tag{3.30}$$

Finally, the derived equation by applying inverse Clarke transformation for each phase can be obtained as in equ.3.31-equ.3.33.

$$I_a^2 = I_+^2 + I_-^2 + 2I^+ I^- cos\theta \tag{3.31}$$

$$I_b^2 = I_+^2 + I_-^2 + 2I^+ I^- cos(\theta - \frac{2\pi}{3}) \tag{3.32}$$

$$I_c^2 = I_+^2 + I_-^2 + 2I^+ I^- cos(\theta + \frac{2\pi}{3}) \tag{3.33}$$

where,

$$\theta = tan^-1\left(\frac{Q^+}{P^+}\right) + tan^-1\left(\frac{Q^-}{P^-}\right) - \delta \tag{3.34}$$

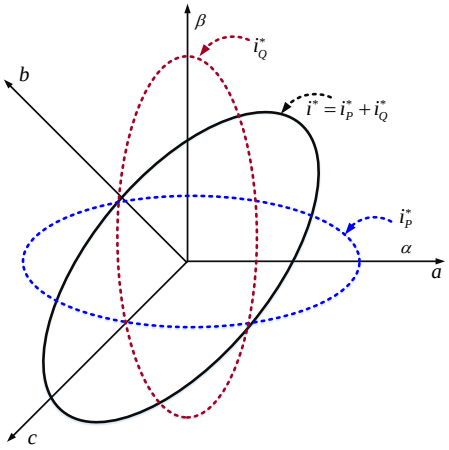


**Figure 3.5:** Locus for resulting current $i^*$

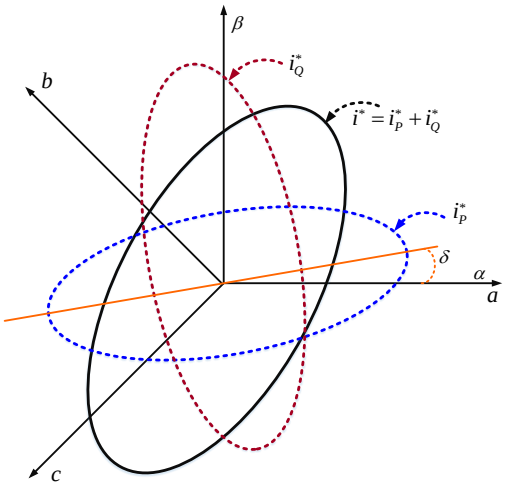


**Figure 3.6:** Locus for resulting current $i^*$ with a certain angle $\delta$

It can be noticed in equ.3.34 the $Q^+$ and $Q^-$ references are not derived. The flexible coefficient ($k_2$ ) is dependent on reactive power reference. The sequence component of $Q^*$ can be done as in equ.3.35.

$$Q^* = Q^+ + Q^- \tag{3.35}$$

Where,

$$Q^+ = Q^* k_2; Q^- = Q^*(1 - k_2) \tag{3.36}$$

The $k_2$ is dependent on voltage unbalance factor as in equ.3.37.

$$k_2 = \frac{Q^+}{Q^*} = \frac{k^+(1 - V^+)}{k^+(1 - V^+) + k^- V^-} \tag{3.37}$$

Further, solving equ.3.36 and equ.3.37 the $Q^*$ can be obtained as in equ.

$$Q^* = Q^+ + Q^- = Q_{max}(k^+(1 - V^+)) + k^- V^- \tag{3.38}$$

Where, $k^+$ and $k^-$ are set equivalent to 2 as per grid code requirement. This sums up the calculation for injection of positive and negative sequence injection method by utilising flexible coefficients. Next section discuses the methodology to attenuate second harmonic oscillations. The FNPSC method will provide flexibility over positive and negative sequence injection within converter current limitation as per grid regulations.

## 3.1 DDSRF Current Controller

The *dq* synchronous reference frame controller is one of the conventional solutions for the control of grid current. However, recent efforts have been devoted by applying additional filter to attenuate the second-harmonic oscillations [88].These additional filters introduce additional delay and complexity in the current controller. In order to mitigate second harmonic oscillations without using complex filters. Decoupled Double Synchronous Reference Frame Controller (DDSRF) will be used in this project as practised in [89]. This current controller is devoted to attenuate the second-harmonic oscillations by injection of positive and negative sequence current. DDSRF utilises low-pass filter (LPF) but does not introduces a phase delay. The positive and negative reference frames are decoupled to eliminate errors in PI controller from oscillations. The DDSRF controller can be presented as in Fig.3.7. Further, the implementation of DDSRF controller will be discussed.

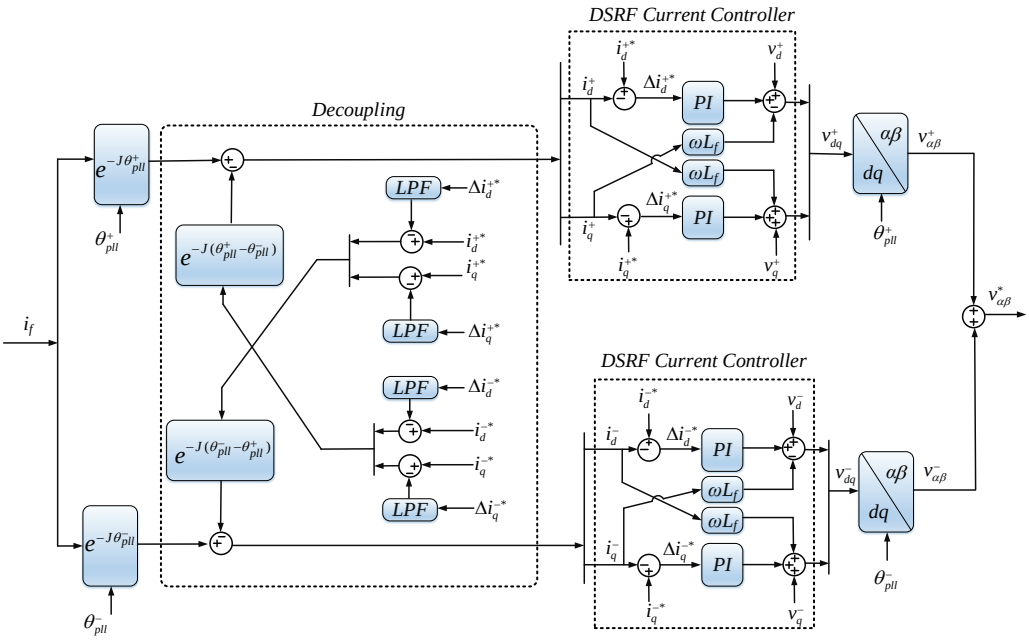


**Figure 3.7:** Enhanced decoupled double Synchronous reference frame controller (DDSRF) [89]

The DDSRF controller consists of $e^{-j\theta}$ also called as Park transformation. This method will be used quiet often to provide decoupling between the positive and negative sequence and eliminate the second-harmonic oscillations. The variables for DSRF current controller can be derived from the above discussion. It should be noted that the $i_d^- *$ is equivalent to zero. The $i_d^+ *$ is calculated based on $v_{dc}$ and FPNSC method. The cut-off frequency of LPF is set to be 25 Hz as such no high selectivity is required for tuning it. The main objective of LPF is to obtain the

current error mean.

## 3.2 Summary

An attempt is made to provide a modified FPNSC method. The flexible coefficients ($k_1$ and $k_2$) plays an important role for the active ($P^*$) and reactive ($Q^*$) power reference generation. Dual-SRF PLL is utilised to extract the $\theta_{pll}^{+-}$ instead of relying on advance PLL structure for sequence extraction. This method aims to provide flexible current sequence injection the maximum converter current limitations are derived to avoid any undesirable trip. Once the voltage and current sequence parameters are calculated DDSRF current controller is used to attenuate the second harmonic oscillations. The main objective of the modified FPNSC method is to avoid using complex filters, PLL and low computational burden making it suitable for LV grid integrated system.

# Chapter 4

# System Implementation

## 4.1 Overview of Simulation Model

The offline studies were carried out using PLECS (Piecewise Linear Electrical Circuit Simulation) blockset. The simulation platform is divided into two parts the continuous electrical part, which consists of all physical components as represented in Fig.4.1. The controllers were implemented in discrete domain with each measurement sampled at $T_s$. Each controller has the sampling period. The implemented model had a single-update PWM. A sample delay is associated with the PWM, the digital electrical part has a sample delay of $1.5T_s$. It is taken as $z^{-1}$ in discrete domain as depicted in Fig.4.1. Finally, the parameters considered for the offline studies are shown in Table4.1.

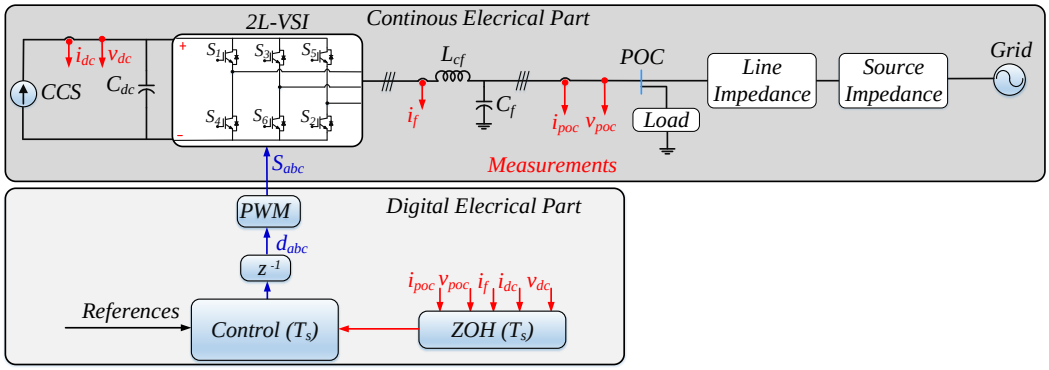


**Figure 4.1:** Simulation model structure implementation with discrete controller part in digital electrical part sampled at $T_s$ and continuous electrical part to emulate the system

.

## 4.2 Model Verification

Further, model verification of the considered system under different scenarios is discussed. This also includes the impact of asymmetrical and symmetrical faults on the system. It should be noted that the grid impedance and line impedance will not be varied only fault impedance ($Z_F$) will be varied to vary the voltage sag.

**Table 4.1:** Main Parameters of the System in Fig.4.1

| Symbol | Description | Physical Value | Bandwidth ($Hz$) |
|---|---|---|---|
| $S_n$ | Rated power | 22.36 kVA | - |
| $v_{poc}$ | Nominal grid voltage | 400 V | - |
| $f_n$ | Rated frequency | 50 Hz | - |
| $v_{dc}$ | DC-link Voltage | 590 V | - |
| $C_{dc}$ | DC-link Capacitance | 2400 $\mu$F | - |
| $f_{sw}$ | Switching frequency | 10 kHz | - |
| $f_s$ | Sampling frequency | 10 kHz | - |
| $L_{cf}$ | Converter-side inductor | 0.0483 pu | - |
| $C_f$ | Filter capacitor | 0.033 pu | - |
| $R_f$ | Filter resistance | 0.0065 pu | - |
| $R_L$ | Resistive load | 64.34 pu | - |
| $L_L$ | Inductive load | 0.2022 pu | - |
| $C_L$ | Capacitive load | 1.75 pu | - |
| $R_S$ | Line impedance (resistance) | 0.0413 pu | - |
| $L_S$ | Line impedance (inductance) | 0.010 pu | - |
| $C_S$ | Line impedance (capacitance) | 0.00068 pu | - |
| $R_G$ | Source impedance (resistance) | 0.0448 pu | - |
| $L_G$ | Source impedance (inductance) | 0.000097 pu | - |
| $K_{p,PLL}$ | Proportional gain of PLL | 92 | 27.67 |
| $K_{i,PLL}$ | Integral gain of PLL | 7931 | - |
| $K_{p,CC}$ | Proportional gain of CC | 4.177 | 725 |
| $K_{i,CC}$ | Integral gain of CC | 36148 | - |
| $K_{p,DC}$ | Proportional gain of DVC | 0.5 | 10.5 |
| $K_{i,DC}$ | Integral gain of DVC | 200 | - |
| $K_{p,RPC}$ | Proportional gain of RPC | 0.000023649 | 6 |
| $K_{i,RPC}$ | Integral gain of RPC | 0.0712 | - |

### 4.2.1 Base Case

The base case is considered as it represents the working of inner and outer loops. The parameters considered for the system are depicted in Table.4.1. The impact of

line impedance is neglected during the base case. Considering a real-time scenario ramp rates were introduced to avoid overshoot in dc-link voltage controller. If ramp rates are not introduced this would lead to increase in grid current ($i_{poc}$) for a very short period of time leading to unwanted trip of VSI. Finally, in order to provide a real-time interface environment switching pulses ($S_{abc}$) were enabled after the PLL was synchronised fully.

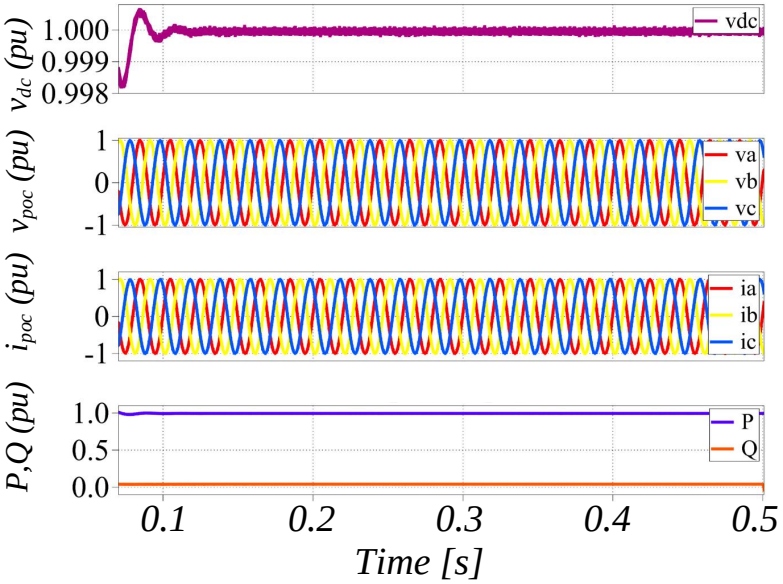


**Figure 4.2:** Simulated response of inner and outer loop with $P^*_{ref}$ = 20 kW and $i_{poc}$ = 28.6 A (RMS)

The $v^*_{dc}$ was set 590 V as represented in Fig.4.2. On the other hand reference power is ramped up slowly to avoid any undesirable trip. It should be noted that the RPC was not considered for the simulated response represented in Fig.4.2. The $i^*_q$ is set to zero, the reactive power by $C_f$ is not compensated. It should be noted that forward euler method is utilised for disretisation of PI controllers from s to z domain.

The RPC is implemented to represent the compensation of reactive power by $C_f$ as in Fig.4.3. The RPC was switched at 0.12 s instantly the reactive power by $C_f$ was compensated by generating the $i^*_q$. This sums up the working of inner and outer loop controllers with the considered parameters. Next case disuses about the implementation of CM for asymmetrical faults.

### 4.2.2 Case-01

This section aims to provide an overview of the problem as discussed in Ch.2 by implementing CM for asymmetrical faults. The simulated response of CM during

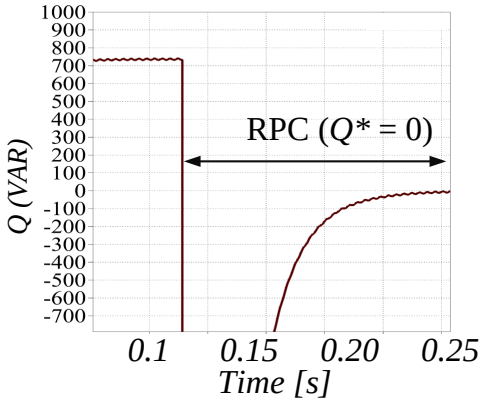


**Figure 4.3:** Simulated response of RPC with $Q^*$ = 0 VAr.

asymmetrical faults is represented as in Fig.4.4. The LG fault is initiated at 0.1 s up till 0.25 s, only 0.15 s of time interval will be taken into account as per Energinet [8].

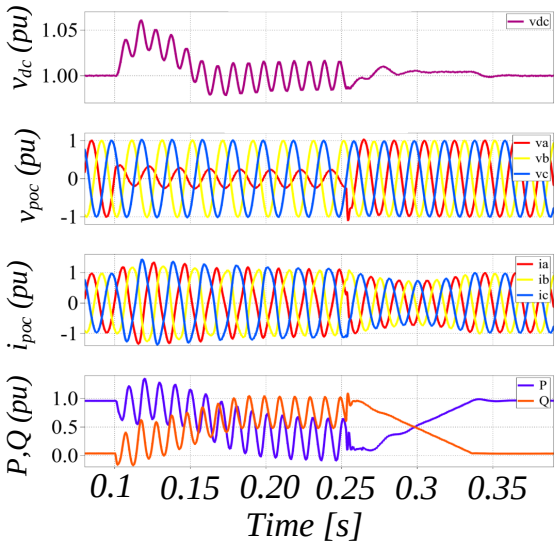


**Figure 4.4:** Simulated response of asymmetrical fault (LG) on Phase-a with $v_a$ equivalent to 0.23 $pu$ during fault

It is worth mentioning that due to unbalanced grid voltages the second harmonic oscillations appear in the $v_{dc}$, $P$ and $Q$ as represented in Fig.4.4. The impact of second harmonic oscillations is the injection of distorted grid current making the power quality poor. It can also be noticed that the $i_{poc}$ rises due to oscillations. These oscillations across $C_{dc}$ make it more prone to failure over period of time.

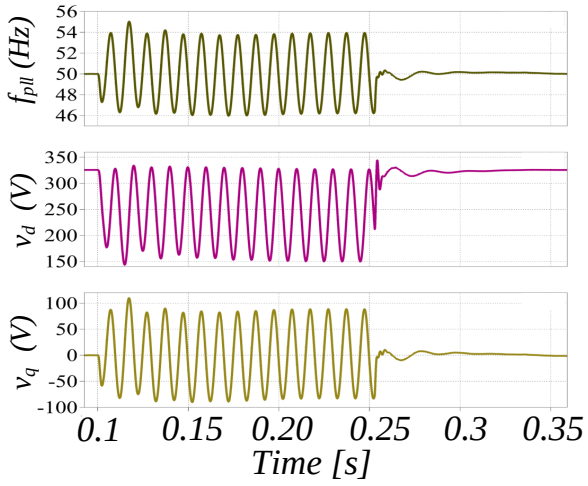


**Figure 4.5:** Simulated response of asymmetrical fault (LG) on Phase-a with $v_a$ equivalent to 0.23 $pu$ during fault on PLL

To be more precise the magnitude of these oscillations increases due to PLL as represented in Fig.4.5. These oscillations further goes into each transformation block and current controller. However, reactive current injection during the fault is accomplished by the CM method but the attenuation of second harmonic oscillations and controlled positive-negative sequence injection cannot be achieved. This brings us to the next section discussing about the flexible positive and negative sequence injection method to attenuate second harmonic oscillations.

### 4.2.3 Case-02

This case discuses the implementation of FPNSC method for voltage sequence extraction. The extracted voltages are represented as in Fig.4.6. The $v^+_{abc}$ (positive voltage sequence) is being used by PLL to obtain $\theta^+_{pll}$. The main advantage of the voltage sequence extractor is to avoid second harmonic oscillations being feed into the transformation blocks and current controller. The $v^+_{abc}$ is equivalent to 0.8 $pu$ during the fault and $v^-_{abc}$ is equivalent to 0.2 $pu$. The negative sequence will be utilised in the DDSRF controller and for the calculation of flexible coefficients ($k_1$ and $k_2$). The $V^+$ and $V^-$ represent the positive and negative sequence voltage magnitude in peak. The $v^-_{abc}$ extracted will feed into SRF-PLL to obtain $v^-_d$, $v^-_q$ and $\theta^-_{pll}$. This will be utilised in DDSRF controller to attenuate second harmonic oscillations.

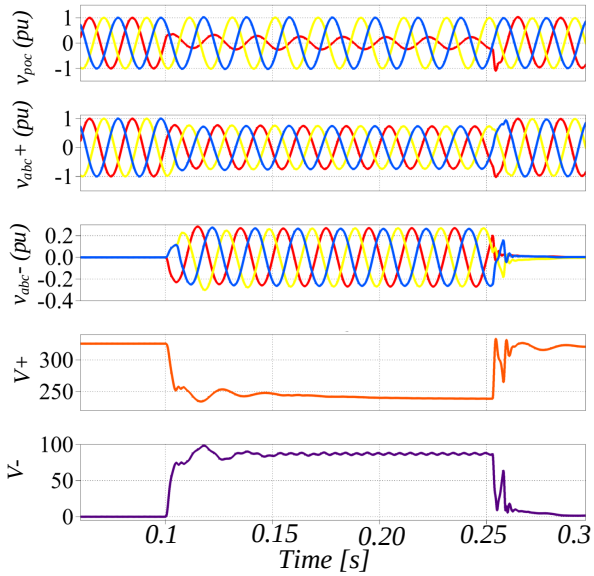


**Figure 4.6:** Simulated response of asymmetrical fault (LG) on Phase-a with $v_a$ equivalent to 0.23 $pu$ during fault with sequence extraction

## 4.3 Summary

This chapter discuses the implementation of different case scenarios. Base case represents working of inner and outer loop controllers. Then problem identification for asymmetrical faults is carried out in case-1 with conventional method. The aim of case-01 is to represent the generation of second harmonic oscillations and it's impact over grid current. Case-02 depicts the extraction of voltage sequences as discussed in previous chapter, which will be utilised in DDSRF controller and other transformation blocks to escape the second harmonic oscillations.

# Chapter 5

# Experimental Work

## 5.1 Experimental Setup

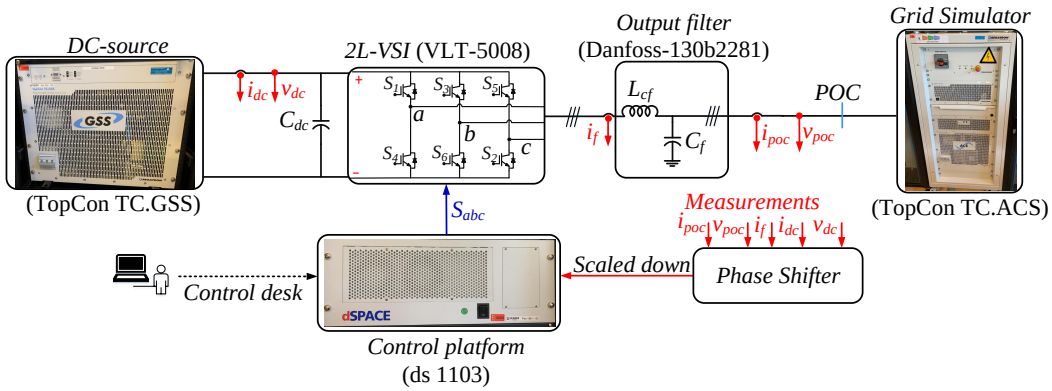


**Figure 5.1:** Laboratory setup used for the experimental verification.The grid-tie inverter is controlled using dSPACE and connected to the output filter and finally, to the Grid Simulator.

The validation of designed controllers as discussed in *Chapter-4* are validated on the experimental setup as in Fig.5.1. The presented HIL (Hardware-in-Loop) consists of a programmable DC-source (TopCon TC.GSS) grid tie source sink. The DC-link capacitor ($C_{dc}$) is in built inside the Danfoss VLT-5008 (grid tie inverter) of 25 kVA.. To attenuate the switching harmonics a *LC* filter is provided. Further, in order to simulate the faults grid simulator will be utilised. The **line-impedance** and **source-impedance** cannot be estimated present in the lab. A real-scenario will be undertaken to cross-verify the proposed methods. The analysis carried out in *Chapter-2* was only limited to show the impact of line-impedance characteristics for LOS during severe symmetrical faults. The phase-shifter is used to scale-down the measurements to a certain level and feed in to the 16-bit ADC (Analog to

Digital Converter) of dSPACE. The dSPACE acts as a control-platform interfaced with Matlab-Simulink to generate the c-code for implementation of controllers. The control desk acts as a platform for varying the reference active power ($P_{ref}$) and reactive power ($Q_{ref}$). The DVC parameters ($K_{pdc} = 0.2$ and $K_{idc} = 5$) are varied for the robust validation of controllers in base case. The model number represents of each component is mentioned in non-italics as in Fig.5.1. The grid-simulator is utilised to act as a voltage source no-filters were presents in the PLL loop to minimise frequency deviations. Harmonic compensators can be added to CC to attenuate the $5^{th}$ and $7^{th}$ harmonics. The base case scenario will be discussed representing the working of inner and outer loop controllers. It should noted that due to limitations on hardware setup small adjustments have been made to avoid instability.

### 5.1.1 Base Case-1

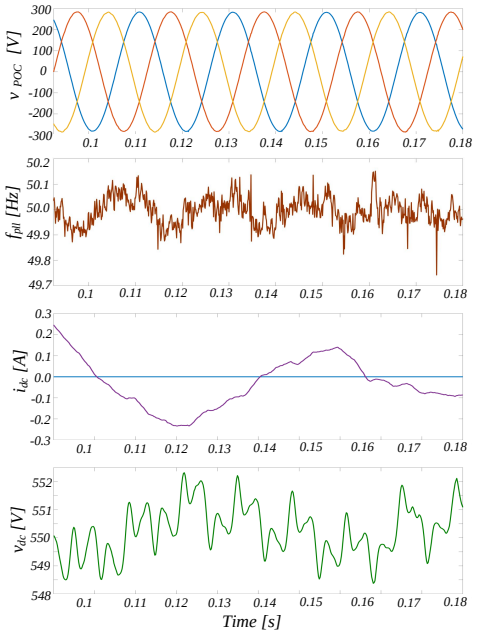


**Figure 5.2:** Base case-01 without enabling switching pulses ($S_{abc}$).

The base case-1 aims to provide the understanding of setup before enabling switching pulses ($S_{abc}$). The adjustments made in the setup are due to DC source limitations. In general for a three phase converter with nominal voltage of 400V (RMS) the minimum DC-link voltage required is around 650 V. However the DC source present has the maximum limitation of 600V only. In order to avoid the saturation limits of the DC source $v_{POC}$ has been set to 200V (RMS) value instead of

230V (RMS). The peak value of $v_{POC}$ is 282.84 V as represented in Fig.5.2. The PLL frequency ($f_{pll}$) is not constant 50 Hz knowing the fact a grid simulator is used. The average frequency deviation observed was around + 0.1 Hz and -0.1 Hz as represented in Fig.5.2. The possible solution to minimise the frequency deviations is to add a low-pass filter in the loop. It should also be taken into account that the setup consists of noise. This also adds on to the deviations observed in the measured quantities. In this case scenario the dc current reference ($i^*_{dc}$) has been set to zero but the actual dc current ($i_{dc}$) was always varying as depicted in Fig.5.2. On the other hand $v^*_{dc}$ was set to be 550V and the measured $v_{dc}$ is close to the reference value as in Fig.5.2. It should be noted that no pulses were enabled that means no power was injected. This case provides a scenario of frequency deviations, noise from measurements and the working of dc-link voltage controller. The next base case discuses the scenario when pulses are enabled.

### 5.1.2 Base Case-2

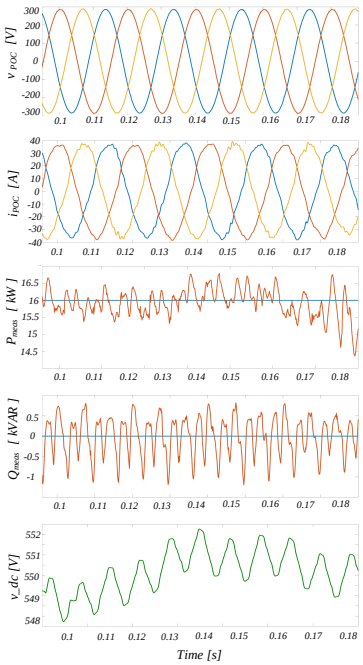


**Figure 5.3:** Base case-02 enabling switching pulses ($S_{abc}$).

The base case-2 discuses the scenario when $S_{abc}$ is enabled. The $P_{ref}$ was set to be 16 kW the measured $P_{meas}$ was around the reference power. The deviations observed in the $P_{meas}$ is due to the varying $i_{dc}$, which can be further observed in the $P_{meas}$ and $Q_{meas}$. The $Q_{ref}$ was set to be 0 kVAR but was an open-loop controller

was so the reactive power from the $C_f$ can be observed in the $Q_{meas}$ as in Fig.5.3. The peak current $i_{POC}$ was 37.47 A and the current THD was found out to be 4% to 5%. However, the setup can go maximum up to 22.36 kVA but due to limitations over $i_{dc}$ from DC source the active power injected can be maximum up to 16 kW. These limitations are to avoid dc-link voltage stability. This sums up the base case scenarios representing the working of outer and inner loops.

## 5.2 Summary

This chapter provides an overview of the experimental setup for this project. Initially, the hardware implementation of base case scenarios is discussed with and without enabling pulses. This provides an overview of the deviation observed in the measured quantities. The limitations on the setup to avoid DC link voltage instability is also discussed. The adjustments are made in the dc link reference and $v_{poc}$ to stay within the limitations. The response of controllers discussed in previous chapter for symmetrical and unsymmetrical faults will be considered as a part of future work.

# Chapter 6

# Conclusion and Future Work

## 6.1 Conclusion

The increasing electrical energy consumption globally imposes an increased production of electricity to meet these requirements. The desire to reduce the carbon foot-print has inclined us more towards penetration of renewable energy systems. In *Chapter-1* a brief overview of category of plants based on the rated power at POC with share of distribution lines is discussed. The state-of-the-art is discussed in detail representing the proposal and drawbacks of selected reference. Finally to sum up problem formulation, project-objectives and limitations of this project are depicted.

In *Chapter-2*, initially small-signal stability analysis is carried out for the inner and outer loops. To benchmark the performed simulation studies LV grid case scenario is considered. The FRT implementation as per grid-code requirements to inject required reactive current as per voltage drop is discussed in detail. The problem identification during FRT by conventional method for symmetrical and unsymmetrical faults is described with different scenarios. Efforts have been devoted to explain the loss of synchronizm during severe symmetrical faults by deriving the active and reactive current transfer limits.

In *Chapter-3* modified FPNSC algorithm is proposed the main objective of this method is to inject flexible positive and negative sequence current injection. This will avoid over voltage on non-faulty phase as compared to conventional method. Complex PLL structure are neglected to avoid complexity. This also avoids the additional phase delay introduced by those complex filters. The modified method has low computational burden because few limitations can already be fulfilled by conventional method. The derivation of FPNSC method and generation of second harmonic oscillations are explained with the help of instantaneous power theory. The converter current limitations were adopted to avoid undesirable trip events.

Finally, *Chapter-4* and *Chapter-5* concludes the different case scenarios consid-

ered during the studies. Initially, base case is considered representing the working of inner and outer loops in both simulation and experimental studies. Then the discussion of problem during asymmetrical faults is carried out. To that end the contribution of this thesis can be summed up as:

- Modified flexible positive and negative sequence control method is proposed as compared to others it has low computational burden, no complex PLL for sequence extraction and DC-link dynamics are not neglected.
- Problem identification for severe symmetrical faults is carried out to represent the phenomena of loss of synchronization. Further, supported by the discussion of active and reactive current transfer limits with respect to line impedance characteristics and current-injection angle.
- Considering the objectives of the project. Modified FPNSC method is proposed to attenuate second harmonic oscillations and avoid over-voltage on non-faulty phase as compared to conventional method. The synchronisation stability due to severe symmetrical faults is represented with different current injection angle. The solution to avert LOS will be considered as a part of future work.

## 6.2 Future Work and Research Prospective

### 6.2.1 DC-link dynamics during symmetrical faults

DC-link voltage controller is being neglected and considered as a constant DC source due to DC-link voltage overshoot during symmetrical faults. A constant DC source is being considered in the recent studies carried out. However, a DC chopper is provided to avoid DC link voltage overshoot. The transition from DC link voltage controller to initiating of DC chopper and acting as an DC source is not studied carefully in the recent studies. It would be interesting to study this phenomena and its impact over current injection during symmetrical faults.

### 6.2.2 Wide comparison of modified FPNSC

A wide comparison of proposed modified FPNSC method needs to be done with conventional method representing it's impact under different unsymmetrical solid and bolted faults.

### 6.2.3 Experimental analysis for FRT strategy

The experimental analysis carried out in the project was only limited to base case scenario. The implementation of FRT strategy still needs to be analysed.

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# Appendix A

# Appendix

## Current controller

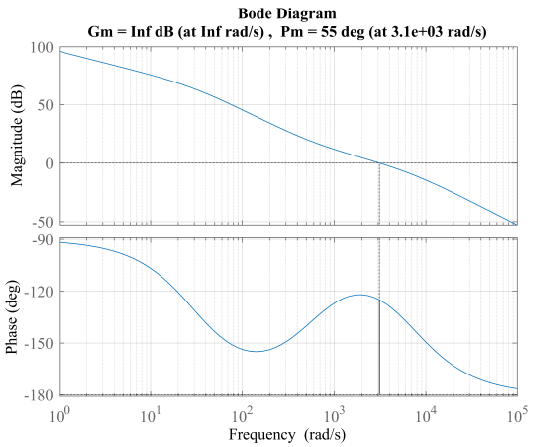


**Figure A.1:** Bode-plot of $G_{ol}(s)$ current-controller

## DC link voltage controller

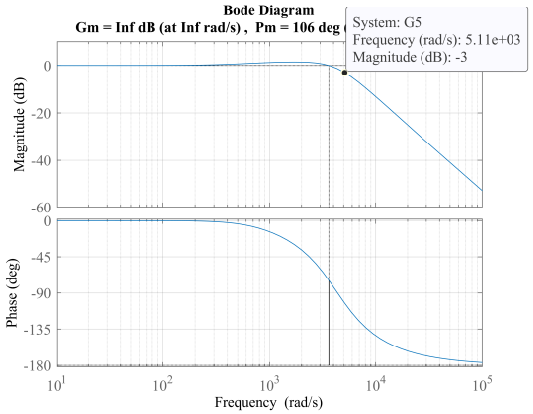


**Figure A.2:** closed-loop (bode-plot) response of current-controller

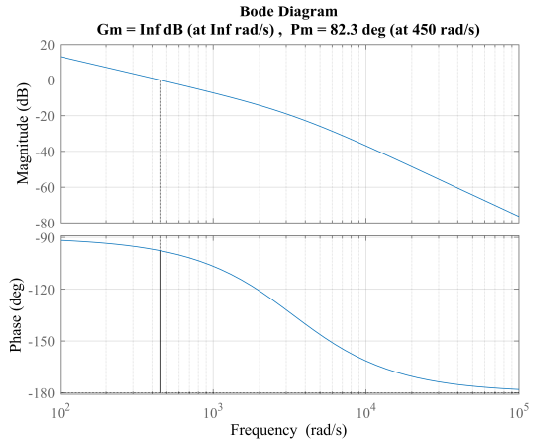


**Figure A.3:** open-loop (bode-plot) response of DC-link voltage controller

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{A.1}$$

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{A.2}$$