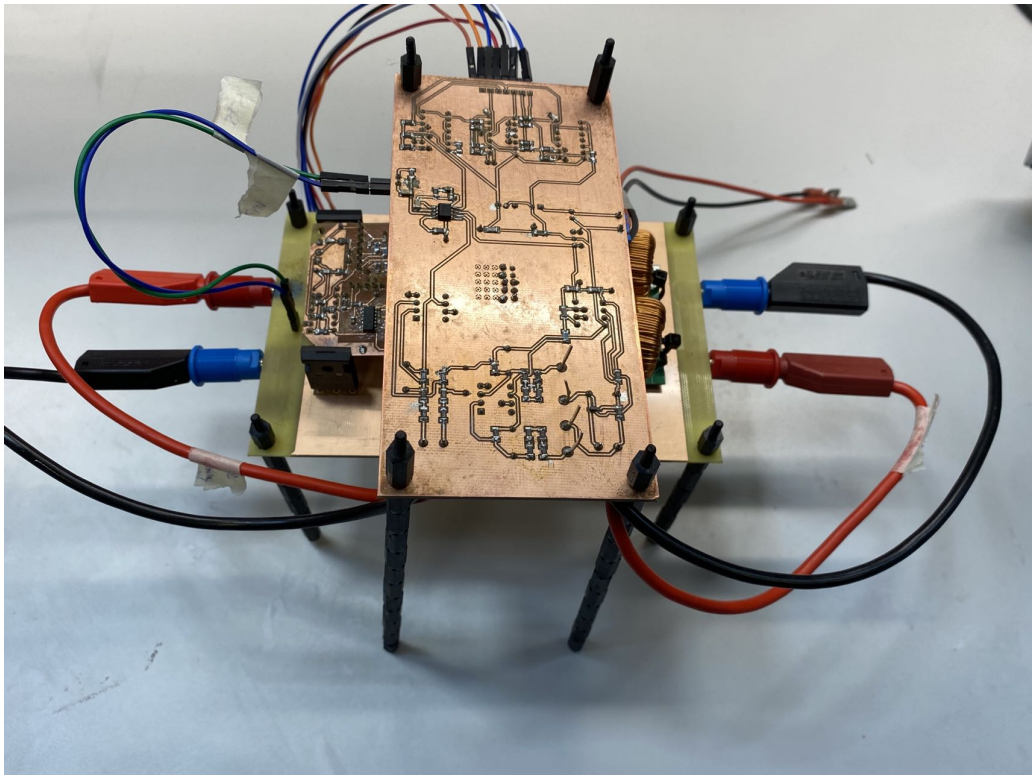
Design and experimental implementation of 3.6 kW bridgeless Totem-pole PFC converter for welding machines

Master Thesis Summary Report

Advanced Project in Power Electronics and Drives



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AALBORG UNIVERSITY
STUDENT REPORT

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Title:
Design and experimental implementation of 3.6 kW bridgeless Totem-pole PFC converter for welding machines

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Advanced Project in Power Electronics and Drives

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Project group:
PED4 - 1040

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Abstract:

Power Factor Correction (PFC) technique is widely applied in the power supply system to solve the current distortion and delay issue caused by the non-linear characteristic of power converters. In the 9th semester, bridgeless Totem-pole PFC was studied due to its high efficiency. A brief simulation model of 3.6 kW bridgeless Totem-pole PFC controlled by analog controller ICE1PCS01 was designed in PLECS. With the designed PLECS model, the output voltage and output power was confirmed to be able to meet the specifications, while there are three main tasks remain to be solved. The first task is implementing an efficiency calculation model to verify whether the efficiency specification can be satisfied. The second task is coming up with a zero-crossing current spike mitigation method. And the third task is experimental verification of the designed simulation model. This project will be based on the three objectives listed above. The efficiency analysis model will be utilized in PLECS, and LTspice will be used to simulate the expected outcome for the experimental circuits based on the selected components. Experimental verification will be conducted on the designed PCB boards, including the power board, the gate drive, and the control board.

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By signing this document, each member of the group confirms participation on equal terms in the process of writing the project. Thus, each member of the group is responsible for the content in the project.

Summary

Input current distortion and phase delay issues in the power supply system can lead to a lot of problems such as low power factor and high distribution loss. In order to tackle these problems, Power Factor Correction (PFC) circuits need to be implemented between the AC power supply and DC link capacitor. In the 9th Semester, 3.6 kW bridgeless Totem-pole PFC was studied and implemented in PLECS. But the efficiency of the proposed model was not investigated. Besides, the proposed design remains to be experimentally verified. Furthermore, the duty ratio variation issue at the zero-crossing point discovered in the 9th semester may need further investigation. So in this project, the main objectives will be firstly building an efficiency calculation model in PLECS based on the study of the 9th semester. Then the zero-crossing current spike issue will be further investigated and a mitigation solution will be provided. Furthermore, the experimental verification of the designed PLECS simulation model will be conducted.

At the beginning of the report, a brief review of the 9th semester project work as well as the background information of bridgeless Totem-pole PFC will be introduced.

After that, for the efficiency analysis, illustrative example of establishing the switching loss and conduction loss lookup table in PLECS based on the datasheets of MOSFETs will be given. And the implementation of PLECS switching loss and conduction loss of MOSFETs will be presented and explained. And the final efficiency result will be derived.

Regarding the zero-crossing current spike issue, apart from the factor that discovered in the 9th semester about the duty ratio variance, another possible factor will be explained. With the investigation of the two possible reasons, one zero-current spike mitigation circuit will be proposed and explained with the help of LTpsice simulation.

The experimental verification will be conducted separately as the whole design was divided into three components, which are the power board, the gate driver board and the control board. For the experimental verification of each board, the hardware design considerations will be explained. Besides, parameter retuning will be expected due to the shortage of desired components. LTspice, PLECS and MATLAB will be of assistance for parameters' tuning. Besides, LTspice simulation will also provide the expected experiment results for the reference of the experimental result. Finally, all three designed boards will be implemented on PCB boards and be tested experimentally. The experimental result will be compared to the LTspice simulation result to verify the correction of the design.

Preface

This thesis report is written by group *PED4 - 1040* at the Department of Energy Technology at Aalborg University. The theme of this project is *"Control of Power Electronic Systems"*. The following software has been used to:

- **Overleaf** - Write the report.
- **PLECS** - Model and simulate the system, and testify the design.
- **Matlab**-Calculate the parameters and bode-plot of the control loop transfer function.
- **LTspice**-Simulate the designed circuits based on selected components.
- **Altium Designer** - Draw schematic and PCB of the hardware setup.
- **Inkscape** - Edit figures.
- **Mathcha** - Graphic design.

Reader's Guide:
Page viii - page x displays all the figures and tables presented in this report.

Page xi displays a nomenclature listing the abbreviations, as well as the variables and their respective units used in this report. The indices will also be presented here.

The bibliography on page 38 presents the literature used in this report. The references are given in the following format:

[Author][Title](Institution)(ISBN)[Year](URL)(Date Accessed)

Where fields in square brackets are mandatory, while regular brackets are only relevant for certain formats, i.e books or web pages. The bibliography entries are sorted after their appearance in the text. Sources will be cited with the Vancouver method [number] where the number represents the number in the bibliography.

Equations will be referenced according to their appearance in the report. As such, equation number 4 in chapter 2 will be referred to as Equation (2.4).

The reference used for figures and tables follow the same logic as for the equations, however without the parentheses.

Table of Contents

List of Figures

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Nomenclature

Abbreviations

2EDL	2EDL23N06PJ
BOM	Bill of material
EMI	Electromagnetic Interference (EMI)
ICE1	ICE1PCS01
IPW	IPW60R024CFD7
NTC	Negative temperature coefficienT
PF	Power Factor
PFC	Power Factor Correction
PLL	Phase-locked loop
PWM	Pulse-width modulation
ST	SCTWA35N65G2V

Variables

Symbol	Description	Unit
η	Efficiency	(%)
ζ	Damping Coefficient	(-)
C	Capacitor	(F)
f	Frequency	(Hz)
i	Current	(A)
L	Inductance	(H)
P	Power	(watt)
R	Ohmic Resistance	(Ω)
s	Laplace Operator	(-)
t	Time	(s)
v	Voltage	(V)
E	Energy	$(W \cdot s)$

Indices

AC	Alternating current
cond	Conduction
d	Drain
DC	Direct current
ds	Drain-source
es	Estimated
g	Gate
gd	Gate-drain
gs	Gate-source
in	Input
out	Output
p	Parasitic
ref	Reference
S	Switch
s	Source
sw	Switching
th	Threshold

Chapter 1

Introduction

Nowadays, power electronic converters are widely applied in industrial and domestic applications to attain certain specified electrical characteristic such as converting AC power supply to certain voltage level DC supply. However, the power converters' non-linear characteristic will bring a current distortion issue to the power system, making the input current out of sinusoidal shape. And may also introduce phase shift between the input current and input voltage. The phase shift issue traditionally can be tackled by introducing reactive load. But the distortion issue, or the harmonics issue, cannot be eliminated by that way. If the harmonics flow in the power system without being contained, it may increase the distribution loss, cause overheat to transformers and shorten the life span of it. Besides. it may mis-trigger relays or breakdown components with low level insulation. Therefore, it is necessary to take actions to minimize the impact of current distortion.

As power factor (PF) reflects the impact of both current distortion and current phase shift, so the method to tackle the current distortion and current phase shift issue in the power supply system is therefore called Power Factor Correction (PFC) technique. Conventionally, PFC is connected between the AC power supply and DC link capacitor. The general function of PFC is by introducing switching devices (known as active PFC) or passive components (e.g. inductors or capacitors, known as passive PFC) to shape the input current in phase with input voltage and remains sinusoidal in shape. A brief function illustration of PFC is shown as Figure 1.1 .

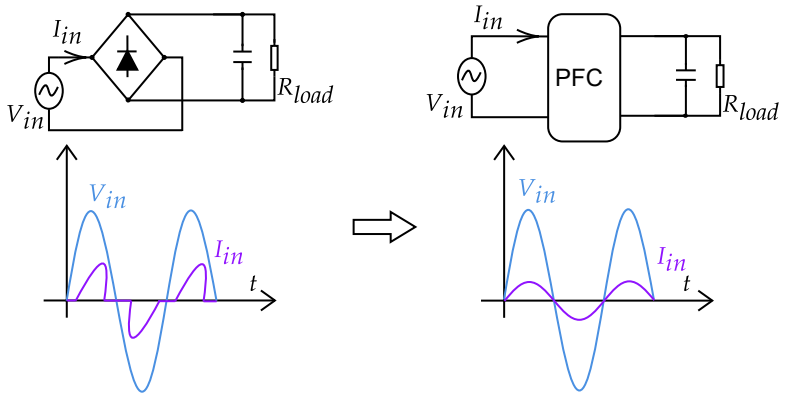


Figure 1.1. Simplified illustration of PFC function

As active PFC has smaller size, lighter weight and lower power loss compared to passive PFC, four different active bridgeless PFC topologies were compared in 9th semester regarding their advantages and disadvantages such as switching devices numbers, control complexity, common-mode noise severity and efficiency. After the comparison, it concluded in Report [1] that although bridgeless Totem-pole PFC topology has more complex control, it is able to achieve higher efficiency than other topologies. As efficiency is the major specification of the project, therefore Totem-pole bridgeless PFC became the research target.

Since it was suggested by Migatronic to utilize analog control to shorten the developing time, analog controller ICE1PCS01 (ICE1) was selected to control Totem-pole topology due to its availability both in market and in PLECS. As ICE1 was originally designed for basic boost PFC, some supplementary circuits need to be designed in order to adapt ICE1 to control Totem-pole PFC. So in the 9th semester, the main work was designing the supplementary circuits to adapt ICE1 to control 3.6 kW bridgeless

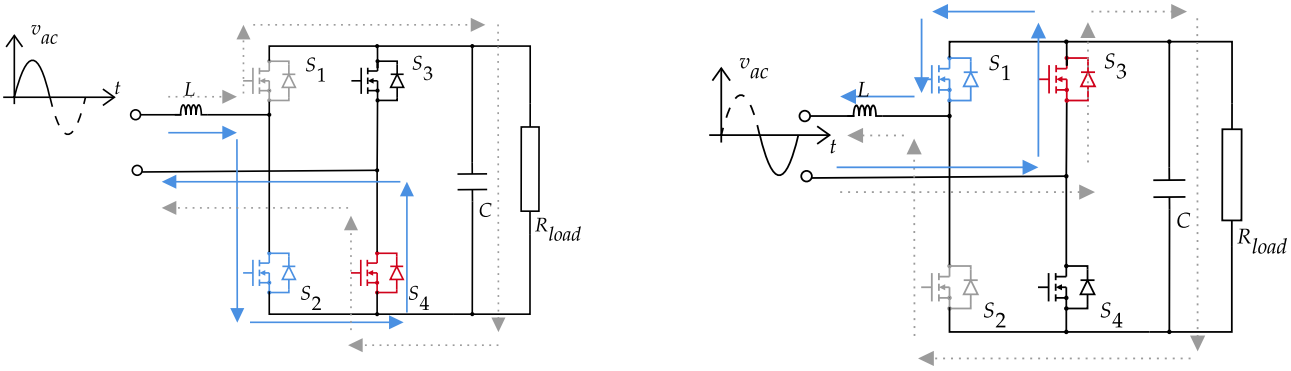
Totem-pole PFC. After implementing the designed 3.6 kW bridgeless Totem-pole PFC with ICE1 and its supplementary circuits, it confirmed the validity of the design as the simulation result can meet the output voltage and power requirement. [1]

However, there are several issues remain to be solved. Firstly, it is about the efficiency analysis, which was not conducted in 9th semester due to time limitation. Secondly, high amplitude starting-up inrush current remains to be mitigated. Thirdly, fast switching MOSFETs duty ratio variation issue at V_{AC} zero-crossing point needs further investigation as it may lead to current spike, which will be explained in Section 1.2. Last but not least, the experimental implementation and verification of the 3.6 kW bridgeless Totem-pole PFC simulation model implemented in PLECS remains to be done.

The following sections will review some basic facts about bridgeless Totem-pole PFC topology and give a brief introduction about the intrinsic problem of the Totem-pole PFC topology, which is the zero-crossing current spike issue.

1.1 Background of bridgeless Totem-pole PFC

Bridgeless Totem-pole PFC is constructed by four switching devices and the switching pattern of it is shown as Figure 1.2.



(a) Positive half cycle switching pattern

(b) Negative half cycle switching pattern

Figure 1.2. Brideless Totem-pole PFC switching pattern

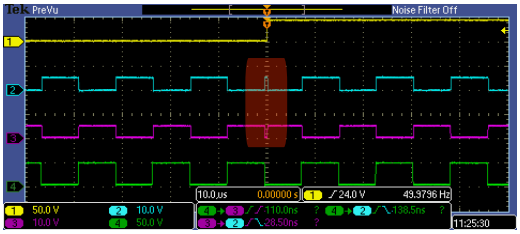
As shown in Figure 1.2, S_1 and S_2 form the left leg (fast leg) and they switch at switching frequency (S_1,S_2 will be referred as fast switches below), S_3 and S_4 from the right leg (slow leg) and they switch at grid frequency (S_3,S_4 will be referred as slow switches below).

During the positive half cycle,S_4 remains ON and S_3 remains OFF while S_1 and S_2 switches complementary. When S_1 is ON and S_2 is OFF, the DC link capacitor will be charged and current flows through as the grey dash line indicated in Figure 1.2a. When S_1 is OFF and S_2 is ON, the DC link capacitor will be discharged and current flows through as the blue solid line indicated in Figure 1.2a.

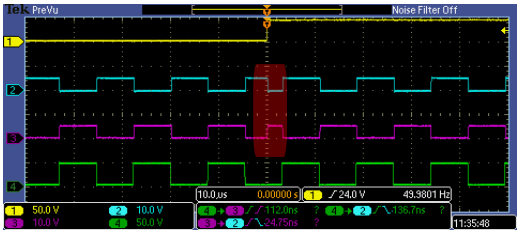
During the negative half cycle,S_3 remains ON and S_4 remains OFF while S_1 and S_2 switches complementary. When S_1 is ON and S_2 is OFF, the DC link capacitor will be discharged and current flows through as the blue solid line indicated in Figure 1.2b. When S_1 is OFF and S_2 is ON, the DC link capacitor will be charged and current flows through as the grey dash line indicated in Figure 1.2b.

1.2 Zero-crossing current spike issue of Totem-pole PFC

During the test of gate logic circuit in the previous project, it was found the duty ratio of S_1 or S_2 varies a lot at every zero crossing point as shown in Figure 1.3.



(a) Gate signal at Zero-crossing time point from negative half cycle to positive half cycle

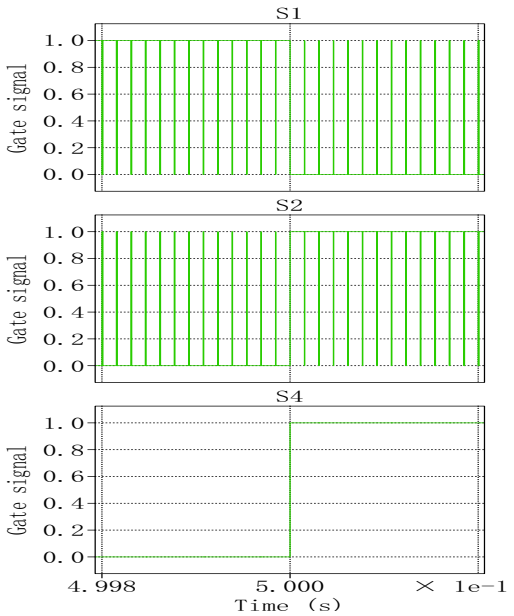


(b) Gate signal at Zero-crossing time point from positive half cycle to negative half cycle

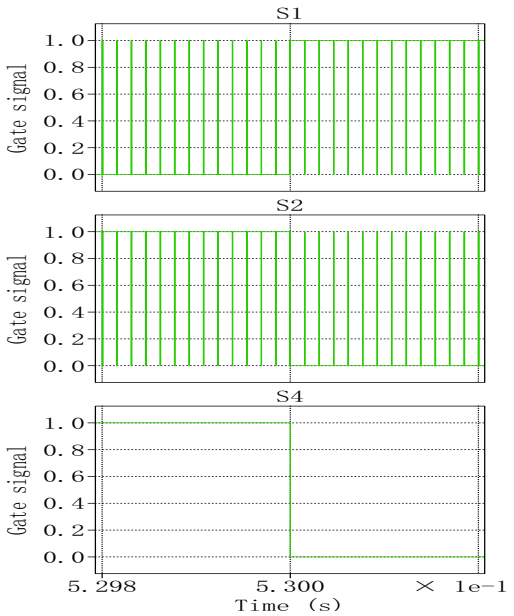
Figure 1.3. Fast switching MOSFETs duty ratio variation issue at zero-crossing point of V_{AC}. Channel 1 represents the gate signal of S_4, channel 2 represents the gate signal of S_1, channel 3 represents the gate signal of S_2 and channel 4 represents a 65 Khz simulated signal from the output of controller ICE1.[1]

By comparing Figure 1.3a and Figure 1.3b, it shows that the duty ratio of fast switching devices S_1 and S_2 varies a lot at two different zero-crossing time points.This is assumed due to the switching frequency is not a integer multiple relationship of the grid frequency in the test, which can be confirmed by checking the waveform of channel 1 and channel 4. As channel 4 deviate relatively from channel 1 at the zero-crossing point V_{AC}, it leads the the duty ratio variation of the fast switching MOSFETs S_1 and S_2.

However, the voltage level of V_{AC} is low at the zero-crossing point. In order to build up enough current to support the load, the fast switch which is in charge of boosting (e.g S_1 for the positive half cycle or S_2 for the negative half cycle) should have almost 100% duty ratio. And an ideal duty ratio pattern is depicted as Figure 1.4.



(a) Gate signal waveform at Zero-crossing time when V_{AC} changes from negative half cycle to positive half cycle



(b) Gate signal waveform at Zero-crossing time point when V_{AC} changes from positive half cycle to negative half cycle

Figure 1.4. Simulated ideal boost switch duty ratio pattern at zero-crossing points of V_{AC}

As shown in Figure 1.4a, when V_{AC} changes from negative half cycle to positive half cycle, S_4 changes from OFF to ON. As the power supply has a low voltage level at zero-crossing point, the boosting switch of positive half cycle S_2 almost has 100% duty cycle. And as complementary to S_2, the duty cycle of S_1 approaches 0%. When V_{AC} changes from positive half cycle to negative half cycle, the duty ratio pattern is shown as Figure 1.4b. During the negative half cycle, S_1 is in charge of boosting and accordingly has a duty ratio of almost 100% and S_2 as complementary, has a duty ratio of almost 0%.

While due to the duty ratio variation issue in reality as shown in Figure 1.3, the boosting switch may have low duty ratio and therefore ,there will be a current spike stimulated to build the desired current. And this is assumed to be one of the reasons that lead to the current spike.

Apart from that, there are also some other scenarios may lead to the current spike issue at zero-crossing point. One of them is due to the slow reverse recovery performance of the slow switches S_3 and S_4 summarized by Reference [7]. An illustration of that problem is shown as Figure 1.5.

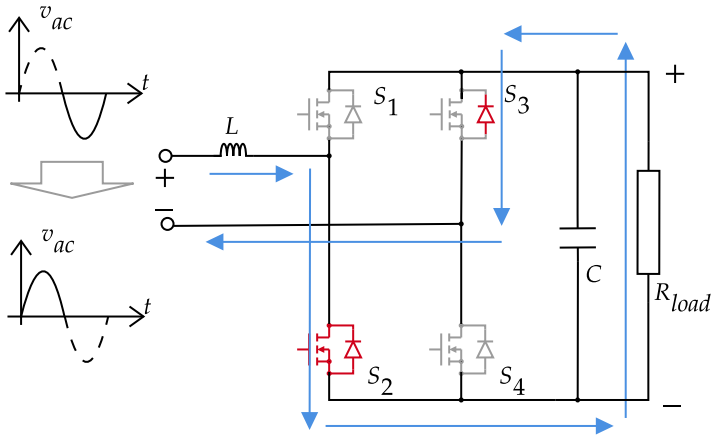


Figure 1.5. Current spike cause at zero-crossing point due the slow reverse recovery performance of slow switch S_3

When V_{AC} changes from negative half cycle to positive half cycle as indicated by Figure 1.5, S_4 should be ON and S_3 should be OFF. Meanwhile S_2 should has a duty cycle of almost 100% and S_1 has a duty ratio of approximately 0%. Due to the slow reverse recovery characteristic of the body diode of S_3, the current will flow as indicated in Figure 1.5 and drain-source voltage will clamped to the output voltage V_{DC}. Consequently, there will be a positive current spike and the spike amplitude is determined by the inductance of L, the voltage value of V_{DC} and the lasting period d_t of the reverse recovery of S_3. As the current spike at zero-crossing point will distorted the current shape and cause severe EMI issue, actions need to be taken to mitigate the current spike.

Overall, this project will focus on the efficiency analysis of the 3.6 kW bridgeless Totem-pole PFC, developing a method to mitigate the current spike at zero crossing point, building hardware according to the simulation model and test designed hardware.

Chapter 2

Problem Statement

The problem statement for this project is the following

" Implementing the efficiency analysis model on the existing PLECS simulation of the single-phase 3.6 kW bridgeless Totem-pole PFC, developing a method to mitigate the zero-crossing current spike and experimentally verify the simulation results of the design."

2.1 Specifications

The requirements from Migatronic for the PFC converter are listed below.

- Input power supply: Single phase 230 V AC, 50 Hz
- Output voltage: 400 V DC ±20 V 100 Hz ripple
- Output power: 3.6 kW
- Efficiency :$\geq$ 97%

2.2 Objectives

In order to solve the problem stated before, the objective scope of this project will include:

- Building efficiency simulation model and conduct loss calculation and analysis
- Design a circuit for mitigating zero-crossing point current spike
- Implementing hardware boards like power board, control board and gate driver boards as illustrated in Figure 2.1
- Conducting hardware experiments and make comparison with simulation results regarding the specifications indicated in Section 2.1

2.3 Schematic of bridgeless Totem-pole PFC with analog controller ICE1PCS01

Based on the previous study of the control strategy of the controller ICE1, there are some sensing circuits need to be designed and implemented to adjust the controller ICE1 for the bridgeless Totem-pole PFC. The sensing circuits include current sensing circuits, voltage sensing circuits, polarity detection circuits and gate logic circuits. And based on the discussion about the zero-crossing current spike issue in Chapter 1.2, a zero-crossing sensing circuit need to be implemented as well. Accordingly, a brief illustration of the hardware setup of the to-be-designed 3.6 kW bridgeless Totem-pole PFC is displayed as Figure 2.1.

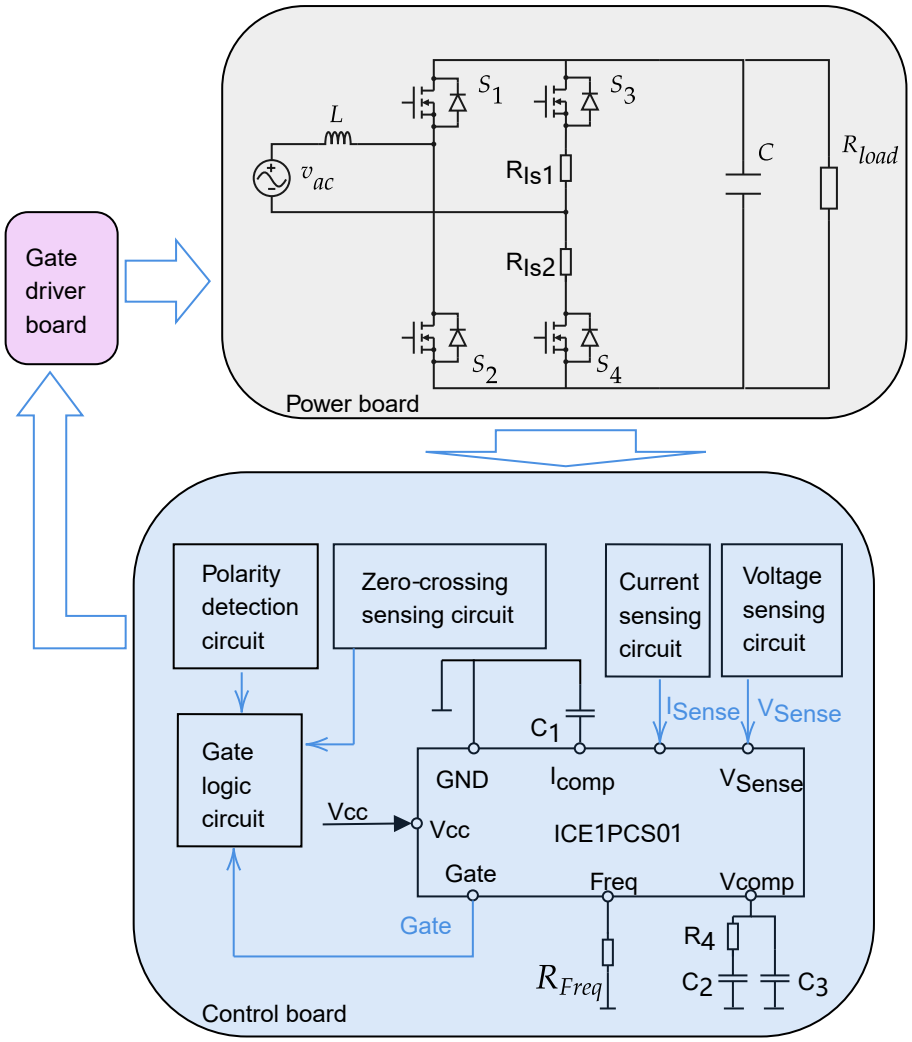


Figure 2.1. Schematic illustration of to-be-designed bridgeless Totem-pole PFC with analog controller ICE1

2.4 Delimitation

- For the efficiency analysis, only the conduction and switching loss will considered for the overall loss of the system, other formats of loss such as loss caused by input inductor, output capacitor, dead time or power supply ICs energy consumption will not be considered.
- For the switching loss simulation, only consider the effect of drain current. Other factors such as gate resistance or the Junction temperature effect will not be considered.
- The influence of the switching frequency on the converter has not been considered in this project because of time constraints. The switching frequency has been chosen to be 65 kHz since this is a common value used.
- EMI filter design and heat sink design will not be involved due to time limitation.

Chapter 3

Efficiency Simulation

Efficiency, as one of the major specifications of this project, needs to be simulated and checked whether it can meet the requirement of being higher than 97% . And in order to simulate the efficiency, the loss calculation of the switching MOSFETs needs to be well estimated. This chapter will introduce about the thermal model of MOSFETs and how to build the thermal description file of it in PLECS according to the datasheets of MOSFETs. The loss and efficiency calculation methodology will be explained and the PLECS model efficiency simulation result will be presented and analyzed.

3.1 Switching and conduction loss of MOSFETs

During circuit analysis, MOSFETS are often expected to switch ideally, which means no turn-on transient time($t_r + t_{d(on)}$) or turn-off time($t_f + t_{d(off)}$) and no on-state resistance($R_{ds(on)}$). However, all those non-ideal characteristics are unavoidable in real application. Due to the non-ideal switching performance, there will be switching loss dissipated during the switching transient period of MOSFETs and conduction loss dissipated during the ON state and OFF state of the MOSFETs. Due to the blocking resistance is big enough, the leakage current of the OFF state can be neglected and accordingly the OFF state power loss will not be considered. A brief illustration of the switching waveform of MOSFETs as well as the loss accumulation is shown as Figure 3.1.

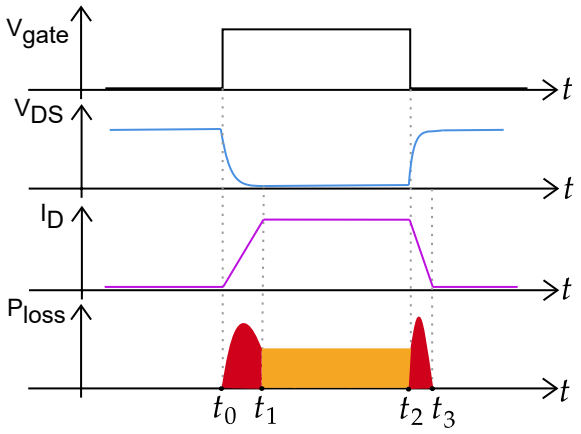


Figure 3.1. MOSFETs turn-on and turn-off transient current and voltage waveforms as well as switching & conduction loss illustration

As indicated in Figure 3.1, from t_0 to t_1, both the current I_D and the voltage V_{DS} across the device are larger than zero, and the time integration of $V_{DS} \cdot I_D$ leads to the large instantaneous turn-on switching losses represented by the left red plane in Figure 3.1. From t_1 to t_2, due to the existence of $R_{ds(on)}$, there will be a conduction loss as indicated by the yellow plane in Figure 3.1 and it equals to the time integration of $I_D^2 \cdot R_{ds(on)}$. From t_2 to t_3, the transient of V_{DS} and I_D will lead to the turn-off switching loss and it equals to the time integration of $V_{DS} \cdot I_D$ as well.

In order to simulate the thermal behavior of switching devices in PLECS, three components are necessary and they are thermal description file of semiconductors, heat sink and ambient temperature.[2] Similar to the electrical circuit, heat dissipation of a circuit can also form an enclosed loop. The loss (or heat dissipation) of the power module can be regarded as current source and the

thermal resistance of the heat sink or the case of the power module can be regarded as the impedance between the power module and the air. And the air (or ambient temperature block in PLECS) therefore resembles a voltage source.[2] A simple illustration of the equivalent thermal circuit is shown as Figure 3.2 :

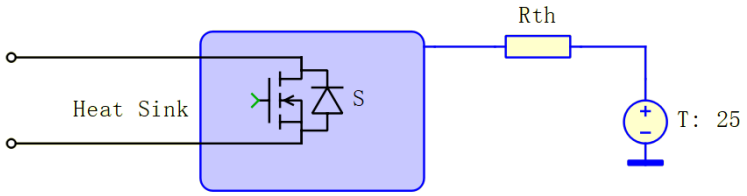
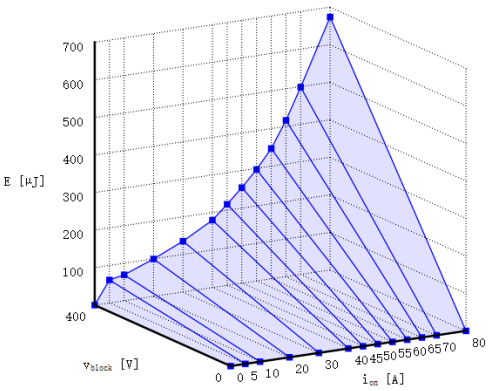
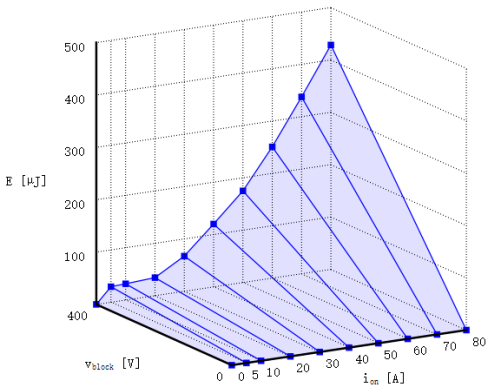


Figure 3.2. Brief diagram of thermal circuit

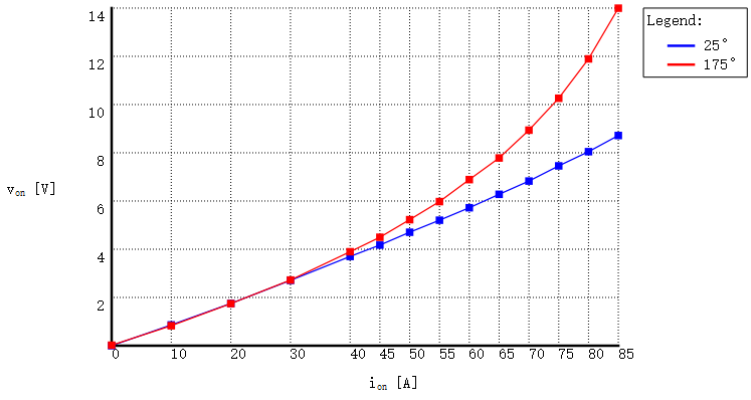
As mentioned in Section 2.4, the heat sink design will not be discussed within the project. For the normal operation of the PLECS simulation thermal model, the thermal impedance of the heat sink is chosen as 0.5 W/K and the thermal capacitance is chosen as 0.01 J/K by referring to the Reference [2]. Then the next step is to add thermal description for the switching devices. By checking the datasheets of the MOSFETs, there will be some experimental results about the switching energy curve or conduction energy curve. By capturing the curves and inserting them into the PLECS thermal model editor, the turn-on/off transient switching loss and conduction loss lookup tables can be generated. The example of the fast switching MOSFETs ST utilized in this project is shown as Figure 3.3.



(a) Turn-on loss



(b) Turn-off loss



(c) Conduction loss

Figure 3.3. Generated thermal description lookup table of fast switch SCTWA35N65G2V

3.2 Loss and efficiency calculation in PLECS

For the switching loss, as discussed in Section 3.1, it is determined by the transient value of V_{DS}, I_D and the transient lasting period turn-on transient time$(t_r + t_{d(on)})$ or turn-off time$(t_f + t_{d(off)})$. So it is really challenging to calculate the switching loss. But PLECS offers a relative simple method to do the switching loss calculation. The general idea is by simplifying the switching transient process to a switching energy pulse(E_{SW}), which can be iterated by the turn-on/off loss lookup table like displayed in Figure 3.3a and Figure 3.3b. And then the switching loss calculation process can be simplified by Equation (3.2) as below :

$$\overline{P_{sw(t_s)}} = \frac{E_{\text{on}} + E_{\text{off}}}{t_{\text{s}}} \tag{3.1}$$

For the conduction loss, dividing the integration of the instantaneous power losses over the switching period will derive the average conduction loss and it can be represented by Equation (3.3c).

$$\overline{P_{cond(t_s)}} = \frac{\int_0^{t_s} R_{ds(on)} \cdot i_D^2(t)}{t_{\text{s}}} \tag{3.2}$$

An overall illustration of the switching loss and conduction loss calculation methodology in PLECS is then displayed as Figure 3.4.

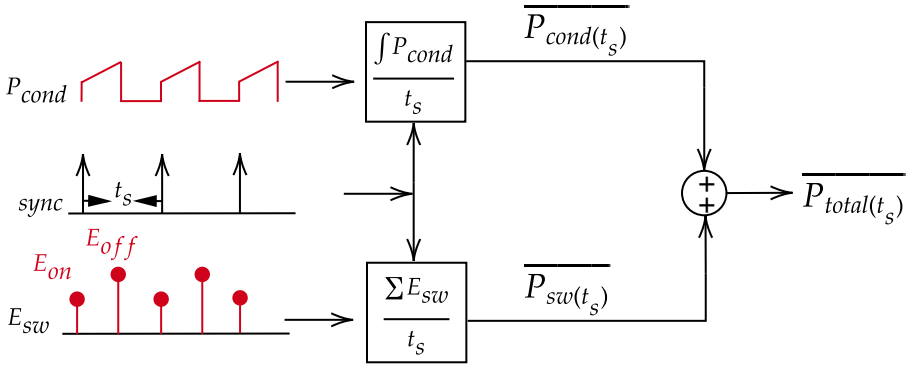


Figure 3.4. Loss measurement illustration[2]

Figure3.4 shows that the total averaged power loss is then expressed by Equation

$$\overline{P_{total(t_s)}} = \overline{P_{cond(t_s)}} + \overline{P_{sw(t_s)}} = \frac{\int_0^{t_s} R_{ds(on)} \cdot i_D^2(t)}{t_{\text{s}}} + \frac{E_{\text{on}} + E_{\text{off}}}{t_{\text{s}}} \tag{3.3}$$

In PLECS, the periodic average function block can realize the conduction loss calculation and the periodic impulse average function block can realize the switching loss calculation as discussed above. Probing the MOSEFTs that need to calculate the loss and connecting them to the periodic average block. By setting the corresponding switching cycle(in this project, t_s of S_1 and S_2 is $\frac{1}{65000}$ s, t_s of S_3 and S_4 is $\frac{1}{50}$ s), the averaged switching loss and conduction loss will be derived. And then by summing the averaged switching loss and averaged conduction, it can get the total averaged power loss of the MOSFETs.

The PLECS loss calculation simulation diagram built according to the above discussion is shown as Figure A.1 in Appendix A. One of things in Figure A.1 deserves notice, that is for the slow switching MOSFETs S_3 and S_4, the switching loss calculation was not implemented and only the conduction of them was considered. One of the reason is due to lack of the relative switching energy information from corresponding datasheet [4]. Another reason is that deducting the switching loss of S_3 and S_4 will theoretically not affect the total loss significantly. As based on Equation (3.2), t_s of S_3 and S_4 is $\frac{1}{50}s$, and the ratio of E_{on} and E_{off} of S_3 and S_4 is supposed to be μJ, therefore the $\overline{P_{sw(t_s)}}$ of S_3 and S_4 is negligible compared to the total average loss. In order to confirm that, a comparison model was built. In the comparison model, the slow switching MOSFETs IPW S_3 and S_4 were replaced with fast switching MOSFETs ST to confirm the validity of neglecting the switching loss of S_3 and S_4.

The loss simulation result is shown as Table 3.1.

Simulation model	**Real model**				**Comparison model**			
Switches	S1	S2	S3	S4	S1	S2	S3	S4
MOSFETs	ST	ST	IPW	IPW	ST	ST	ST	ST
$\overline{P_{sw}}/W$	3.44	3.44	0	0	3.44	3.44	0	0
$\overline{P_{cond}}/W$	10.63	10.71	2.82	2.81	10.67	10.73	10.65	10.59
$\overline{P_{sw,total}}/W$	6.89				6.89			
$\overline{P_{cond,total}}/W$	26.96				42.66			
$\overline{P_{total}}/W$	33.85				49.55			

Table 3.1. Simulation result of the MOSFETs loss, the real model represents the 3.6KW bridgeless Totem-pole PFC topology and the comparison model is conducted to confirm the validity of the omitting switching loss of slow switches S_3 and S_4.

From the result of simulation shown in Table 3.1, it confirms that it is reasonable to neglect the switching loss of the slow switches in this case as it remains zero in the comparison model. Besides, the conduction loss of the comparison model increases significantly compared to the model, and it is assumed due to the $R_{ds(on)}$ of MOSFET ST is 75 $m\Omega$ and is almost two times larger than the $R_{ds(on)}$ of MOSFET IPW, which is 24 $m\Omega$. This also indicates that for the further improvement of efficiency, selecting slow MOSFETs with lower $R_{ds(on)}$ is an potential method.

With the simulated loss data of the switching devices, the efficiency calculation can be done. However, it is noticeable that the efficiency should not be expressed as $\frac{\overline{P_{OUT}}}{\overline{P_{In}}}$. It is because PLECS treats the switching transient as ideal, so the loss calculated based on the thermal file does not correspond to the electrical power consumed by the circuit. Therefore, the efficiency should be expressed as Equation (3.2) .[2]

$$\eta = \frac{\overline{P_{in}} - \overline{P_{loss}}}{\overline{P_{in}}} \tag{3.4}$$

Based on the above discussion, the final PLECS thermal model of the proposed 3.6KW bridgeless Totem-pole PFC is shown in Figure A.2 in Appendix A. And the final efficiency is simulated to be 99.07%, which is bigger than 97% and can meet the efficiency specification. And if assume the input inductor and DC link capacitor will consume roughly 2% of the total power, which is 72 W, it can still meet the efficiency specification.

In this chapter, a briefly illustrative explanation of MOSFETs' switching loss and conduction loss was provided. Then the general process of building thermal model in PLECS was introduced and an

example of building thermal description file for MOSFETs was given. After that, the general idea of how PLECS calculating the switching loss and conduction loss was explained. And finally, the simulation result of the thermal was displayed and analyzed. The conclusion regarding the PLECS efficiency simulation is that , with 99.07% efficiency (only considering the power dissipation of the four switches), the proposed 3.6KW bridgeless Totem-pole PFC can not only meet the efficiency specification as higher than 97% but also leave approximately 2% margin for the power dissipation of input inductor and DC link capacitor. And for further boost the efficiency of the model, selecting MOSFETs with lower $R_{ds(on)}$ to replace the slow switching MOSFETs can be a possible solution.

Chapter 4

Power board design

In Section 2.3, the schematic illustration of the whole hardware setup was displayed as Figure 2.1. This chapter will introduce the design considerations for the power board, which mainly contains the AC inductor, DC capacitor, switching devices, fuse, etc. Apart from those, a starting-up inrush current mitigation method will also be presented.

4.1 Overview of the power board circuit

Core parameters involved in the power board design are shown in Table 4.1 and they are derived by the simulation result from previous project report [1].

Parameter	Value	Parameter	Value
$V_{AC_{rms}}$	230 V	$f_{V_{AC}}$	50 Hz
L_{AC}	211 μH	C_{DC}	1100 μF
$I_{L,P_{inrush}}$	180.5 A	$I_{L,rms_{steady}}$	15.6 A

Table 4.1. Parameters need to be considered for the power board design based on the PLECS simulation result

However, a power inductor that has $211\mu H$ inductance and has the capability of delivering 23.4 A (1.5 ·15.6, 1.5 is the safe margin indicated by Reference [8], 15.6 is the steady state input inductor current RMs value indicated in Table 4.1) coil current is unavailable on the market. And if choose to self-making the power inductor, some key considerations such as saturation current, working temperature range , core loss, magnetic shielding are challenging for testing with the time limitation of the project. Therefore, it is decided to utilize the inductor available in the lab and with all the key characteristics indicated in its datasheet. The inductor kit is 7447075 series from WE electronic and it has characteristics as low core losses, low magnetically leakage field, operating temperature range from –25 $°C$ to +125 $°C$ and 3 A saturation current.

Besides, considering the maximum rating current of load resistor available in the laboratory is 1 A, it is consequently decided to lower the power rate to 400 W. Therefore, the new power inductance value is re-calculated as Equation (4.1)[9].

$$C^{\star}_{DC} = \frac{P_{\text{out}}}{2 \cdot \pi \cdot f_{V_{AC}} \cdot \Delta V \cdot V_{\text{out}}} = \frac{400\text{W}}{2 \cdot \pi \cdot 50\text{Hz} \cdot 40\text{V} \cdot 400\text{V}} \approx 80\mu F \tag{4.1}$$

And the power inductor is re-calculated as Equation (4.2)[9].

$$L^{\star}_{AC} = \frac{V^2_{\text{AC,rms}}}{I_{\text{L,ripple\%}}} \cdot \frac{V_{\text{out}} - \sqrt{2} \cdot V_{\text{in,rms}}}{P_{\text{out}} \cdot V_{\text{out}}} \cdot \frac{1}{f_{\text{sw}}} = \frac{(230\text{ V})^2}{0.2} \cdot \frac{400\text{ V } - \sqrt{2} \cdot 230\text{ V}}{400\text{ W} \cdot 400\text{ V}} \cdot \frac{1}{65\text{ kHz}} \approx 1900\mu H \tag{4.2}$$

Based on the new value of $C^{\star}_{DC}$ and $L^{\star}_{AC}$ and re-run the PLECS simulation (controller parameter tuning will be discussed in Chapter 6), the updated designing parameters for the power board is shown as Table 4.2.

Parameter	Value	Parameter	Value
$V_{AC_{rms}}$	230 V	$f_{V_{AC}}$	50 Hz
$L^{\star}_{AC}$	1900μH	$C^{\star}_{DC}$	80 μF
$I^{\star}_{L,P_{inrush}}$	15.9 A	$I^{\star}_{L,rms_{steady}}$	2.1 A

Table 4.2. Revised parameters for the power board designing based on the PLECS simulation result

4.2 Inrush current mitigation

The inductor current simulation result is shown as Figure 4.1 .

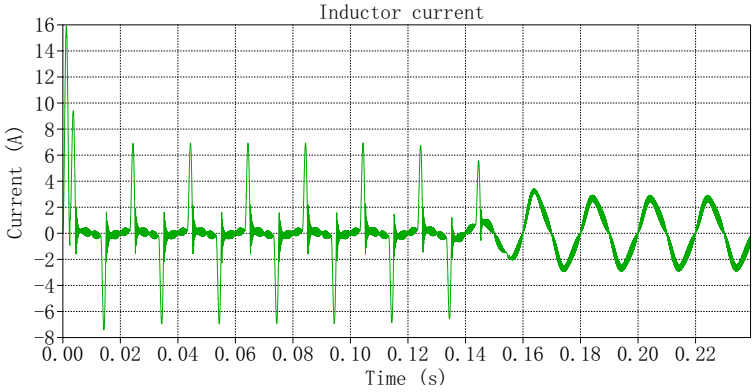


Figure 4.1. Inrush current issue at the starting up transient period

As shown in Figure 4.1, there is an inrush current with peak amplitude around 16A, which will be stressful for the components that current flow through such as fuse, MOSFETs, inductor,etc. One efficient way suggested by Reference[10] to mitigate this current spike is by introducing an negative temperature coefficient thermistor(NTC). A simple illustration of the NTC inrush current mitigation method is shown as Figure 4.2.

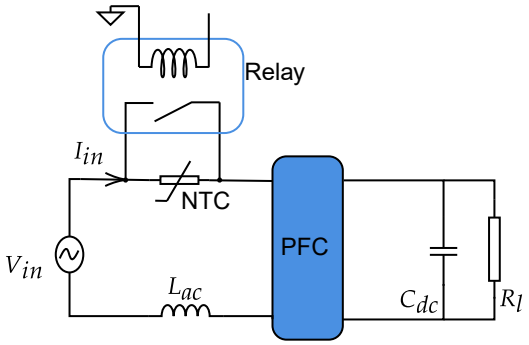


Figure 4.2. Diagram illustration of NTC resistor inrush current mitigation method

As the NTC thermistor has a negative coefficient between the resistance and the temperature, when the the system is powered ON, the NTC thermistor can damp the current spike. And then the thermistor heats up and becomes low resistance , which will allow the system to deliver its full power. As indicated in Figure 4.2, there is also a relay parallelly connected to the NTC thermistor. The function of the relay is to save power loss caused by the NTC thermistor. Besides, if the power system is turned OFF and ON in a short period, the NTC thermsitor may have not cooled down yet and the resistance may be low, which may affect the effect of inrush current depression. With the help of relay, the

NTC thermistor can be bypassed shortly after the system is powered ON and accordingly ensure the NTC thermistor has enough time to cool down[11]. The value of $R_{es,25°C}$ and maximum steady state current need to be considered when selecting the NTC thermistor. For this project, $I^{\star}_{L,rms_{steady}}$ is 2.1 A, and the fuse is accordingly selecting as 3 A as it can keep the inductor from saturation. Therefore, the maximum steady state current should be smaller than 3 A. In this project, CL-90 was selected as the NTC thermistor.The $R_{es,25°C}$ value is 120 Ω and the maximum steady state current is 2 A. A simplified PLECS simulation result comparison is shown as Figure 4.3.

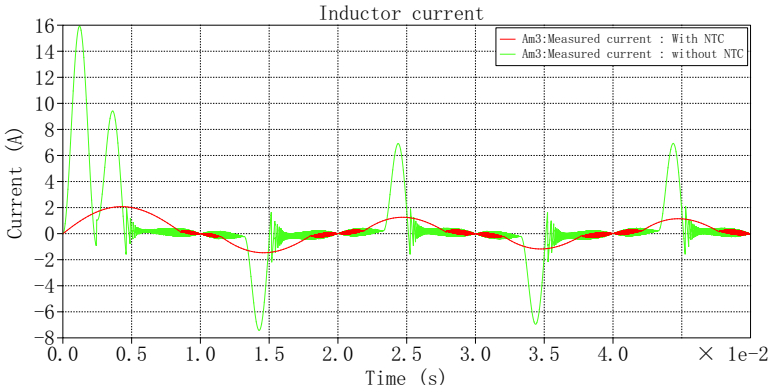
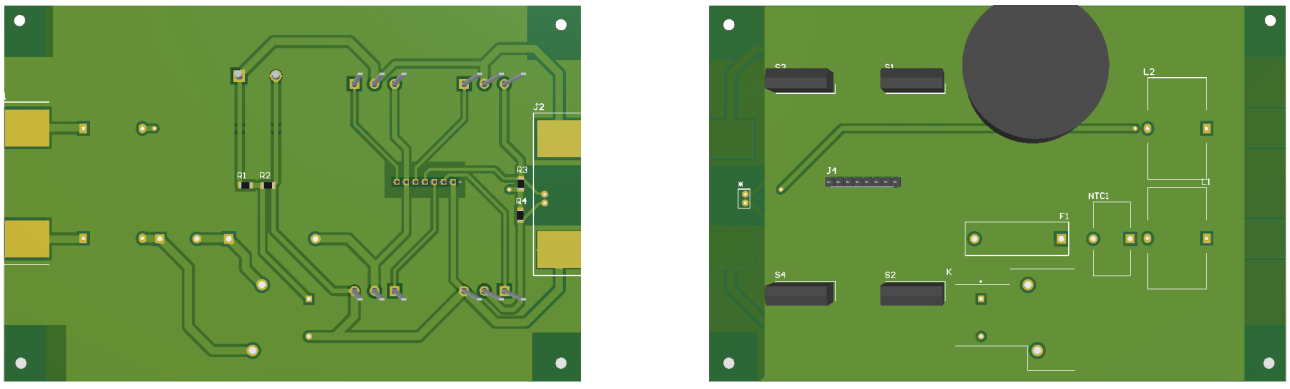


Figure 4.3. Comparison of the PLECS inrush current spike simulation results of with- and without- NTC thermistor CL-90

Figure 4.3 indicates that with 120Ω NTC thermistor at the starting up point, the inrush current peak can be damped to 2A and it is within the designed current range.

4.3 Power board PCB design

With the components' parameters and the inrush current spike mitigation method, the PCB schematic was drawn in Altium Designer and is displayed as Figure 4.4. And the schematic, bill of material list (BOM) as well as the final power board PCB work can be found in Appendix E.



(a) Top layer overview ***(b)*** Bottom layer overview

Figure 4.4. 3D PCB layout of the designed power board

For the design considerations of the power board PCB, the following three aspects were involved :

- Trace width and clearance width. The general idea for them are wider trace width for power line(80mil utilized) and thinner trace width(30mil utilized)for signal line. And the

clearance(30mil utilized) need to be wide enough to ensure the isolation or avoiding signal transmission interference, which is the reason why the surrounding area of gate signal connector J4 was fully cleared shown in Figure4.4a;

- Components layout. As the current keeps conducting and non-conducting in the trace between the MOSFETs bridge quickly, the trace length should be as short as possible. Otherwise the parasitic inductance may cause voltage spike and may lead to EMI issue. The DC capacitor needs to be placed close to the fast switching S_1 and S_2 for the same reason.
- Ground plane. A big ground plane can allow the current flows to the nearest ground and minimized the resistance.Besides, it can act as a heat sink for better heat dissipation.

In this chapter, the power board core parameters were re-designed due to the unavailability of suitable AC inductor and the power rate was updated from 3.6 kW to 400 W. The revised power board parameters can be found in Table 4.2. Afterwards, the starting period inrush current issue was discussed and a method of NTC thermistor combined with relay was introduced to help with damping the inrush current. The PLECS simulation result indicates the validity of that method. Finally, the power board PCB was displayed alongside with its designing considerations concerning the width of trace and clearance, components layout and ground plane.

Chapter 5

Gate Driver Design

This chapter will introduce about the gate driver design, which will include the content of gate driver chip selection, gate driver circuit analysis, breadboard test for the gate driver circuit, dead time circuit design and gate driver PCB test.

Due to the physical structure of MOSFETs, there are three parasitic capacitors existed between the Gate(G), Drain(D) and Source(S) terminals of the MOSFET. The structure illustration is shown as Figure 5.1. C_{gs} represents the parasitic capacitance between the pole G and pole S. C_{gd} represents the parasitic capacitance between the pole G and pole D. C_{ds} represents the parasitic capacitance between the pole D and pole S.

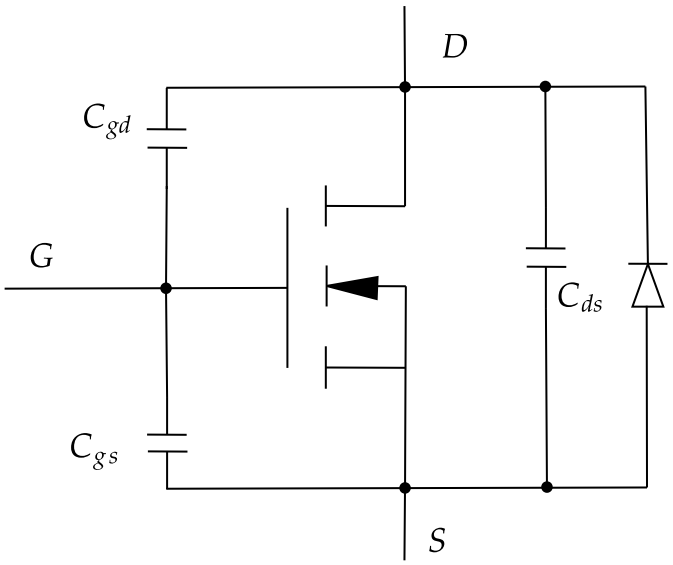


Figure 5.1. N-channel enhancement-type MOSFET parasitic capacitance illustration

Due to the existence of C_{gs}, V_{gs} requires not only enough voltage to be lifted up to the threshold turn-on voltage($V_{GS(th)}$), but also enough current to charge C_{gs} as fast as possible. Therefore, gate drivers are necessary to convert the logic signal from the PWM logic circuit to gate-source voltage signal to turn ON/OFF MOSFETs quickly and reliably.

This chapter will mainly introduce the design considerations for gate driver of this project as well as the simulation and experiment results of the designed gate driver.

5.1 Gate driver chip selection

In this project, SCTWA35N65G2V and IPW60R024CFD7 are selected as the fast switching device(65KHz) and slow switching device(50Hz) respectively.

Firstly, the output voltage of the gate driver needs to be sufficiently bigger than the gate threshold voltage $V_{GS(th)}$. Referring to the datasheets [4][5] [4] of the two switches, the $V_{GS(th)}$ are 3.2 V and 4

V. Besides, it is necessary for V_{GS} to be big enough for the MOSFETs to work in the linear operation region. Furthermore, as the $R_{ds(on)}$ is inversely proportional to V_{GS}, a high V_{GS} need to be selected to achieve less conduction loss. Therefore,by checking the datasheets [4][5] , the the output voltage the gate driver chip needs to be higher than 8 V.

Secondly, the output source current need to be calculated, and it can be determined by Equation (5.1):

$$I_g = \frac{Q_g}{t} \tag{5.1}$$

Q_g represents the total gate charge, t represents the expected the switching on transient time (t$\geq$ $t_r + t_{d(on)}$, the minimum switching on transient time). Based on datasheets [4][5], values of Q_g and $t_r + t_{d(on)}$ and the correspondingly calculated I_g are listed as below:

Switch	Q_g **/nC**	$t_r + t_{d(on)}$ **/ns**	I_g **/A**
SCTWA35N65G2V	73	44	1.66
IPW60R024CFD7	183	91	2.01

Table 5.1. Gate charge(Q_g), minimum switching on transient time $t_r + t_{d(on)}$ and calculated I_g based on switches' datasheets [4][5]

So the minimum output current of the gate driver chip should be 2.01 A.

Furthermore, since the gate driver will be applied on a H-bridge topology, the voltage potential of the pole S of the upper leg is not referenced to the ground. Therefore, the output voltage of the gate driver chip needs to be level shifted based on the voltage potential of the pole S accordingly.

With all the considerations, 2EDL23N06PJ(2EDL) is selected as the gate driver chip. It is a half-bridge gate driver with integrated bootstrap diode. It has a output voltage of 10 V - 17.5 V and the output current is 2.3 A.

5.2 Driving circuit design

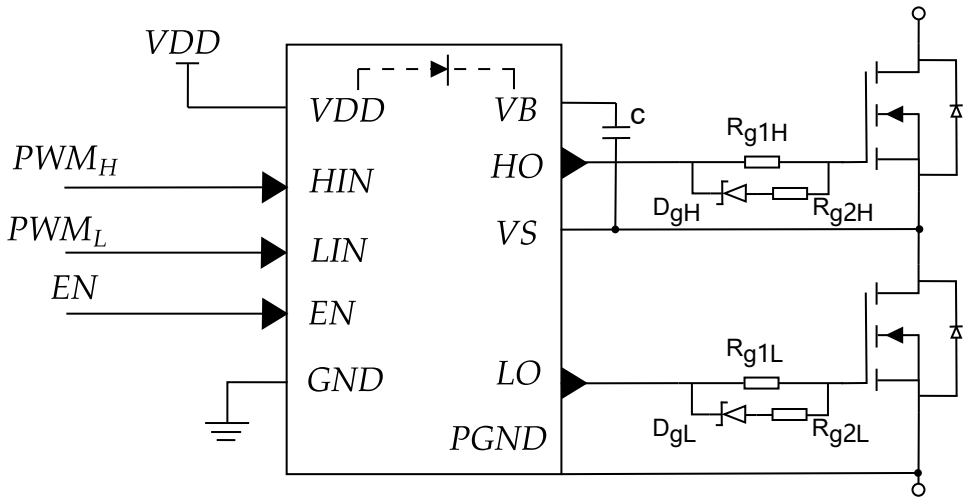
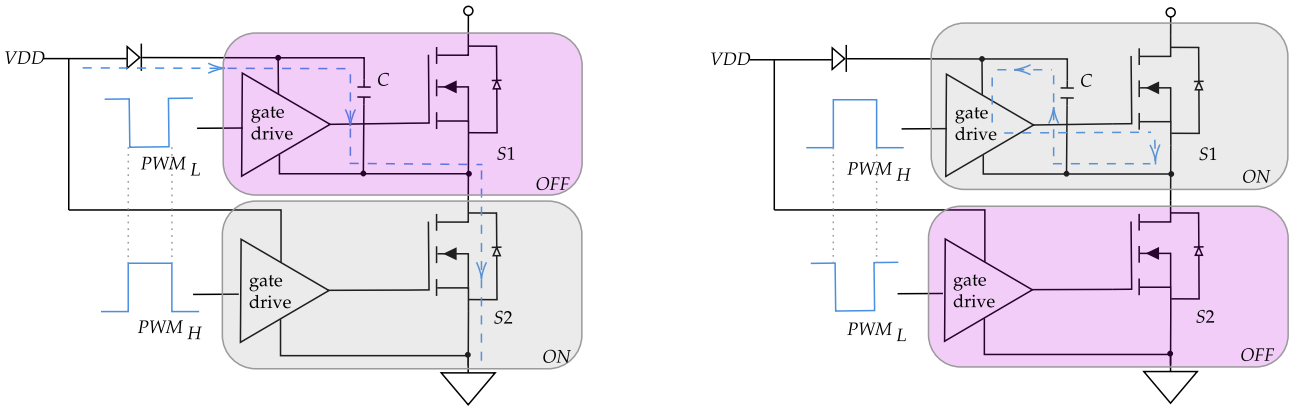


Figure 5.2. Typical application diagram of half-bridge gate driver 2EDL23N06PJ [3]

Based on the datasheet of the gate driver chip 2EDL, the typical gate driving circuit diagram is shown as Figure 5.2. Regarding the driving circuit design, there are two main parts need to be discussed. The first part is about the bootstrap circuit mechanism and the second part is about the gate resistor determination. And they will be discussed in the following sections.

5.2.1 Bootstrap circuit

As mentioned before, 2EDL gate driver chip has an integrated bootstrap diode, together with the bootstrap capacitor C indicated in Figure 5.2, they form a bootstrap circuit and enable to drive the upper leg MOSFET without floating ground issue. A functional mechanism diagram of half-bridge gate driver with bootstrap circuit is shown as below.



(a) Bootstrap capacitor charging path

(b) Bootstrap capacitor discharging path

Figure 5.3. Bootstrap circuit diagram

Figure 5.3a illustrates the scenario when the half-bridge gate driver turns on the down leg MOSFET and meanwhile charges the bootstrap capacitor. When the PWM signal for the down leg is High and for the up leg is Low. The down leg MOSFET will be turned on by the output of the gate driver and the bootstrap capacitor charging path will be conducting. The current flow of this scenario is shown as the blue dashed line in Figure 5.3a. The voltage of the bootstrap capacitor will equals to VDD approximately (not considering the forward voltage drop of the bootstrap diode), which is also the designed V_{gs}.

While for the opposite condition, When the PWM signal for the lower leg is Low and for the higher leg is High. The lower leg MOSFET will be turned off and the up leg MOSFET will be turned on by discharging the bootstrap capacitor. The discharging current path is the blue dashed line as indicated in Figure 5.3b. As the characteristic of the capacitor is maintaining the voltage, so the V_{gs} of the up leg MOSFET will not be affected by the voltage potential variation of its S pole.

5.2.2 Gate resistors' value determination

As indicated in Figure 5.2, there are gate resistors R_{g1H} and R_{g1L} connected between the pole G of MOSFET and the output driving signal of the gate driver. The function of the gate resistors is to damp the amplitude of the driving voltage oscillation and make sure the MOSFETs will not be turned on mistakenly. A simplified gate driving diagram is shown as Figure 5.4.

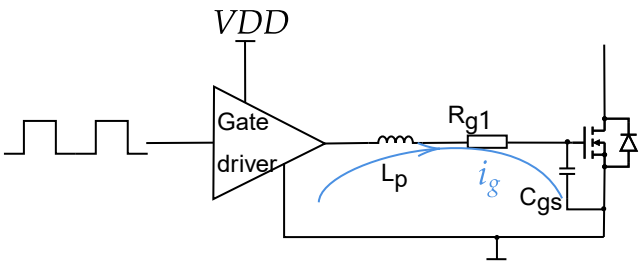


Figure 5.4. Simplified diagram of MOSFET turn ON circuit illustration

L_p refers to the parasitic inductance existed in the gate driving loop. When the MOSFET is ON, VDD will go through L_p, R_g and C_{gs}. The circuit can be expressed in frequency domain as:

$$s \cdot L_{\mathrm{p}} \cdot i_{\mathrm{g}} + R_{\mathrm{g1}} \cdot i_{\mathrm{g}} + \frac{i_{\mathrm{g}}}{s \cdot C_{\mathrm{gs}}} = \frac{VDD}{s} \tag{5.2}$$

Based on Equation(5.2), i_g can be derived as:

$$i_{\mathrm{g}} = \frac{\frac{VDD}{L_{\mathrm{p}}}}{s^2 + \frac{R_{\mathrm{g1}}}{L_{\mathrm{p}}} \cdot s + \frac{1}{C_{\mathrm{gs}} \cdot L_{\mathrm{p}}}} \tag{5.3}$$

Equation (5.3) is a standard second-order transfer function. And the damping ratio of it can be derived as:

$$\xi = \frac{\frac{R_{\mathrm{g1}}}{L_{\mathrm{p}}}}{2 \cdot \sqrt{\frac{1}{C_{\mathrm{gs}} \cdot L_{\mathrm{p}}}}} = \frac{1}{2} \cdot R_{\mathrm{g1}} \cdot \sqrt{\frac{C_{\mathrm{gs}}}{L_{\mathrm{p}}}} \tag{5.4}$$

In order to minimize the current oscillation, ξ needs to be bigger than 1. And based on Equation (5.4), it is derived as :

$$R_{\mathrm{g1}} \geq 2\sqrt{\frac{L_{\mathrm{p}}}{C_{\mathrm{gs}}}} \tag{5.5}$$

The relative information from datasheets [5] [4] that can be used to calculate the value of gate-source parasitic capacitor C_{gs} is shown in Table 5.2:

Switch	C_{iss} **/pF**	C_{oss} **/pF**	C_{rss} **/pF**
SCTWA35N65G2V	1370	125	30
IPW60R024CFD7	7268	143	30

Table 5.2. Parasitic capacitance value of C_{iss}, C_{oss}, C_{rss} of the two applied MOSFETs

Meanwhile, the relationship between C_{iss}, C_{oss}, C_{rss} and C_{gs}, C_{gd}, C_{ds} is shown as Equation(5.6).

$$\begin{aligned} C_{\mathrm{gd}} &= C_{\mathrm{rss}} \\ C_{\mathrm{gs}} &= C_{\mathrm{iss}} - C_{\mathrm{rss}} \\ C_{\mathrm{ds}} &= C_{\mathrm{oss}} - C_{\mathrm{rss}} \end{aligned} \tag{5.6}$$

Based on Table 5.2 and Equation (5.6), the parasitic capacitance value can be calculated and shown as below Table:

Switch	C_{gs} **/pF**	C_{gd} **/pF**	C_{dss} **/pF**
SCTWA35N65G2V	1340	30	95
IPW60R024CFD7	7238	30	113

Table 5.3. Parasitic capacitance value of C_{gs}, C_{gd}, C_{ds} of the two applied MOSFETs

Referring to Equation (5.5) and Table 5.3, it indicates that the value of R_{g1} should be tuned based on the value of parasitic inductance of the gate driving circuit. As L_p is unknown before the PCB is produced, so this part need to be tuned after that.

Apart from avoiding driving voltage oscillation, R_{g2} also needs to be small enough to make sure that the MOSFET can be reliably turned OFF. A simplified MOSFET turn OFF transition circuit illustration is shown as Figure 5.5.

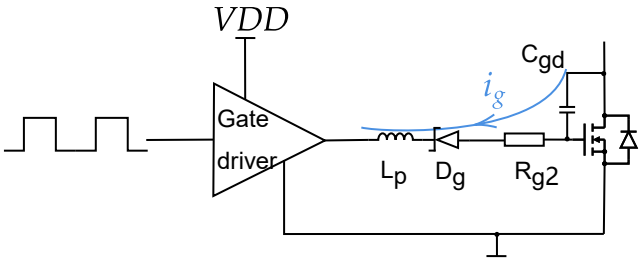


Figure 5.5. Simplified diagram of MOSFET turn OFF circuit illustration

As illustrated in Figure 5.5, when MOSFET is to be turned OFF, there will be a discharging current go through R_{g2}. And the current is :

$$i = c_{\mathrm{gd}} \cdot \frac{dv}{dt} = c_{\mathrm{gd}} \cdot \frac{0 - V_{dc}}{t_{off}} \tag{5.7}$$

In order to make sure that V_{gs} will not reach $V_{GS(th)}$ and mistakenly turn ON MOSFETS, the value of R_{g2} needs to meet the requirement as :

$$c_{\mathrm{gd}} \cdot \frac{dv}{dt} \cdot R_{\mathrm{g2}} < V_{\mathrm{GS(th)}} \tag{5.8}$$

As it is known that V_{dc} is 400 V, C_{gd} values of the two MOSFETS are indicated in Table 5.3, t_{off} values are 44 ns and 180.2 ns attained from datasheets [5] [4], so the maximum value of R_{g2} for the two MOSFETs are :

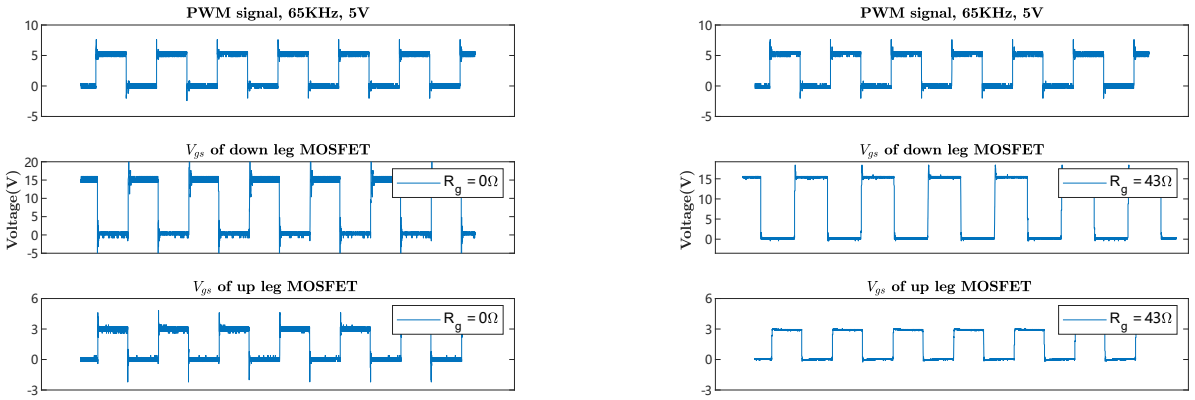
$$\begin{aligned} R_{\mathrm{g2,ST}} &< \frac{V_{GS(th),SCT}}{c_{gd,ST} \cdot \frac{V_{dc}}{t_{off,ST}}} = 8\Omega \\ R_{\mathrm{g2,IPW}} &< \frac{V_{GS(th),IPW}}{c_{gd,IPW} \cdot \frac{V_{dc}}{t_{off,IPW}}} = 60.1\Omega \end{aligned} \tag{5.9}$$

5.3 Breadboard experiment

With all the analysis above, the LTspice simulation was implemented firstly to testify the validity of the analysis. The LTspice simulation model can be found in Appendix C and the simulation result can be found in Section D.1. As the simulation model is ideal and not involving the parasitic interference. So the simulation result will not be analyzed and the breadboard test need to conducted to tune the gate charging resistors. The breadboard test circuit is the same as the simulation schematic as shown in Figure C.1 but without the dead time circuit implemented, which will be discussed in the next section.

The test will be both tested on slow switching leg composed of two IPW and on fast switching leg composed of two ST. In the gate driver breadboard test, the R_{g2} was set to 5 Ω and the R_{g1} value will be the variable. For each set of the gate driver test, four different R_{g1} values were tested, which are 0Ω,21Ω,33Ω and 43Ω. Due to space limitation, only the test result of $R_{g1} = 0\Omega$ and the test result of $R_{g1} = 43\Omega$(because it has better gate voltage response) will be displayed. Other test results can be found in Appendix D.

The test results for the slow switching leg is shown as Figure 5.6.

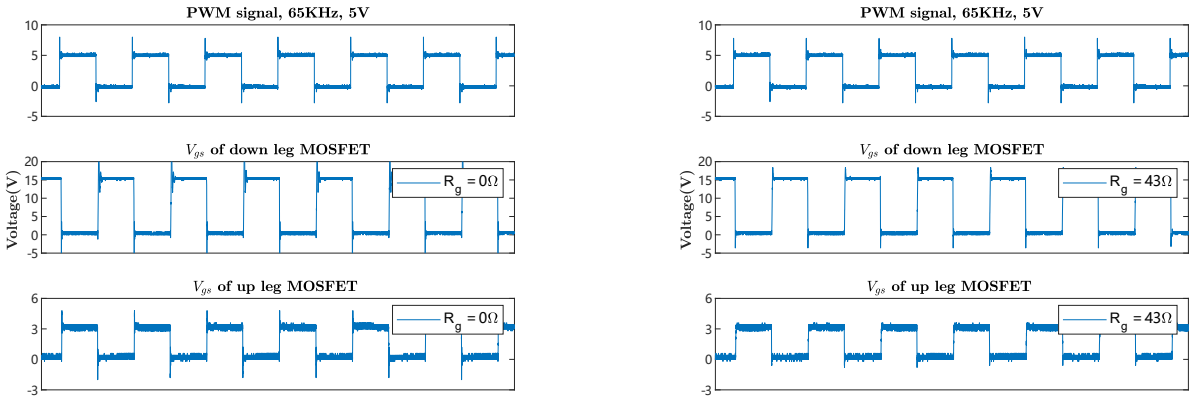


(a) Slow switching leg V_{gs} waveform when $R_{g1} = 0\Omega$ ***(b)*** Slow switching leg V_{gs} waveform when $R_{g1} = 43\Omega$

Figure 5.6. Gate driver breadboard test result comparison of $R_{g1} = 0\Omega$ and $R_{g1} = 43\Omega$ for slow switching leg(R_{g2} remains being 5 Ω).channel 1 represents the PWM signal for the up MOSFET. channel 2 represents the output V_{gs} signal for down MOSFET. channel 3 represents the output V_{gs} signal for up MOSFET(with $\frac{1}{5}$ scaling ratio caused by isolation probe)

The breadboard test result shown in Figure 5.6 indicates that when $R_{g1} = 43\Omega$ and $R_{g2} = 5\Omega$, the designed the gate driver circuit can have an ideal output gate driving voltage V_{gs} for the slow switching leg composed of two IPW MOSFETs.

The test results for the fast switching leg is shown as Figure 5.7.



(a) Fast switching leg V_{gs} waveform when$R_{g1} = 0\Omega$ ***(b)*** Fast switching leg V_{gs} waveform when $R_{g1} = 43\Omega$

Figure 5.7. Gate driver breadboard test result comparison of $R_{g1} = 0\Omega$ and $R_{g1} = 43\Omega$ for fast switching leg(R_{g2} remains being 5 Ω). channel 1 represents the PWM signal for the up MOSFET. channel 2 represents the output V_{gs} signal for down MOSFET. channel 3 represents the output V_{gs} signal for up MOSFET(with $\frac{1}{5}$ scaling ratio caused by isolation probe)

The breadboard test result shown in Figure 5.7 indicates that when $R_{g1} = 43\Omega$ and $R_{g2} = 5\Omega$, the designed the gate driver circuit can have an ideal output gate driving voltage V_{gs} for the fast switching leg composed of two ST MOSFETs.

Therefore, for both the slow switching leg and the fast switching leg, the gate charging resistor R_{g1} is determined to be 43Ω and the gate discharging resistor R_{g2} is determined to be 5Ω.

5.4 Dead time circuit

In order to prevent the shoot-through during the switching transient of fast switching leg, a dead time circuit needs to be implemented. The general idea is by introduce an RC delay circuit to change the rising or falling edge(determined by the direction of the the diode in parallel with the resistor) of square wave signal to a slope. And then it can be flipped by inverter and generate the delay.[12] The dead time circuit implemented in this project is shown a Figure 5.8.

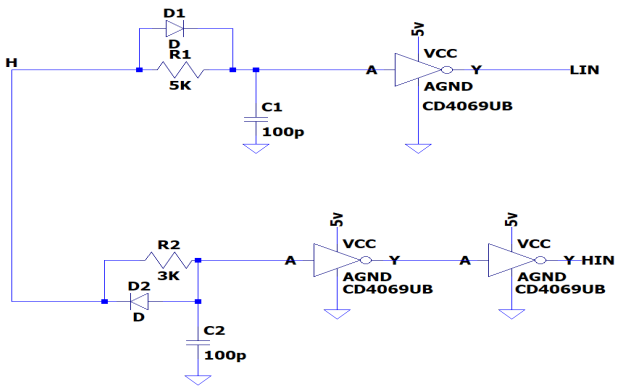


Figure 5.8. LTspice simulation model of the analog dead time circuit implemented in this project

By tuning the values of R_1, C_1, R_2 and C_2 in LTpice, it was find that when $R_1 = 5k\Omega$, $R_2 = 3k\Omega$ and

$C_1 = C_2 = 100pF$, the gate signals for the two switches on the same leg will have enough dead time around 400ns. And the corresponding simulation result is shown as Figure 5.9.

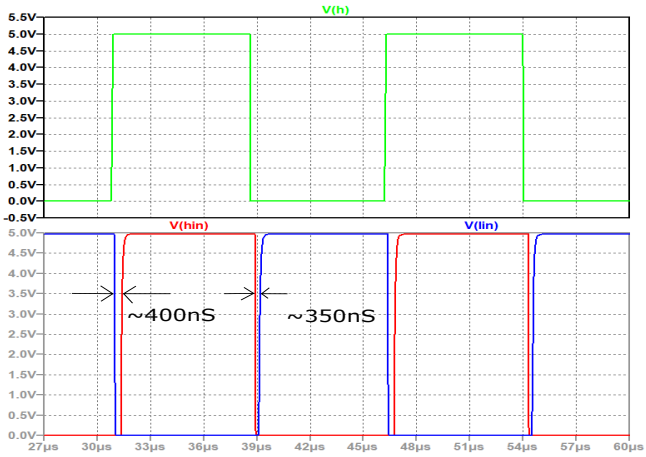
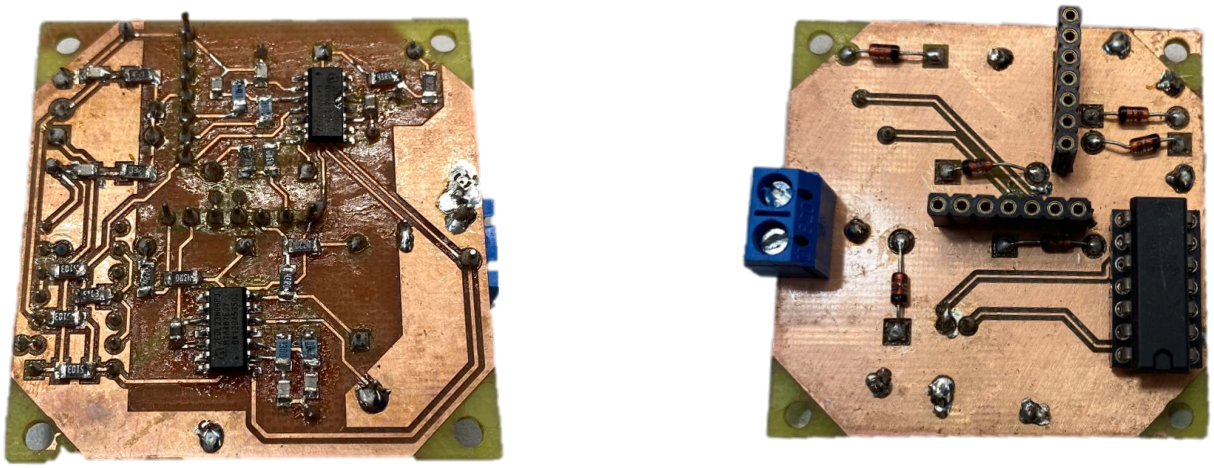


Figure 5.9. Dead time circuit simulation result, the upper plane represents S_2 gate signal from the output of the gate logic circuit, the lower plane represents the gate signal of S_1(blue curve) and S_2 (red curve)

Figure 5.9 shows that, with the tuned parameters, the rising edge of V(hin) is delayed around 400 ns compared to the rising edge of the input $V(h)$ and the rising edge of V(lin) is delayed around 350 ns compared to the falling edge of the input $V(h)$. And therefore it can prevent the overshoot happening on the fast switching leg.

5.5 PCB design and test of gate driver

With the design consideration and simulation results of the gate driver circuit and dead time circuit, the gate driver PCB is then drawn in Altium designer. The schematic overview, PCB overview and the BOM list can be found in Appendix G. The soldered gate driver PCB is shown as Figure 5.10.



(a) Top layer overview

(b) Bottom layer overview

Figure 5.10. Gate driver board

In order to test the function of the designed gate driver, two set of test were conducted.The first test was tested on the slow switching leg and the second test was tested on the fast switching leg. The test result for the slow switching leg is shown as Figure 5.11

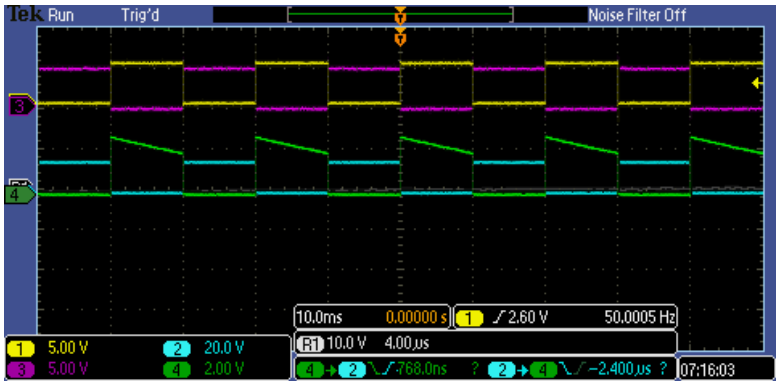
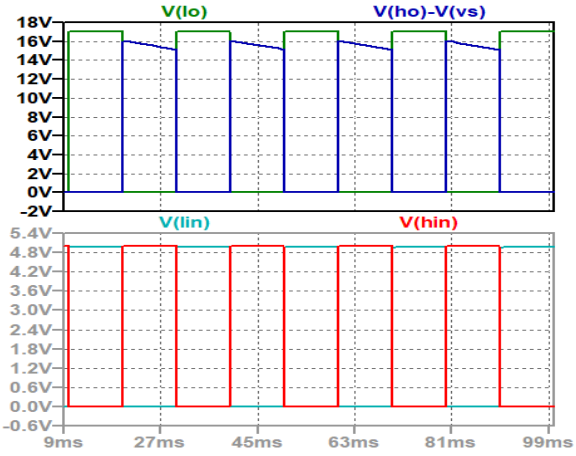
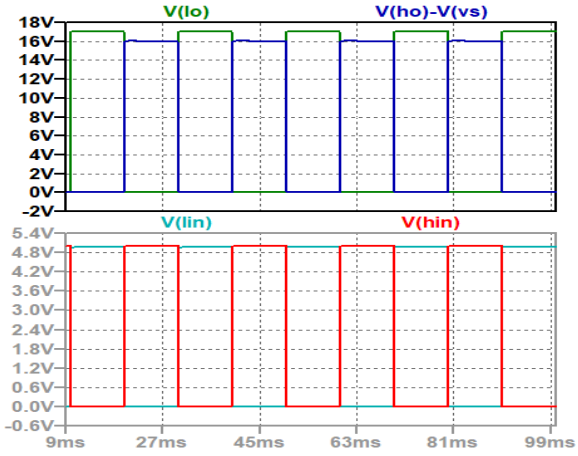


Figure 5.11. Gate driver test result on slow switching leg. channel 1 represents the input PWM signal for the up leg MOSFET. channel 2 represents the input PWM signal for the down leg MOSFET. channel 3 represents the output gate driving signal for the up leg MOSFET.channel 4 represents the output gate driving signal for the down leg MOSFET(with $\frac{1}{5}$) scaling ratio caused by the isolation probe.

From the slow switching leg test result shown in Figure 5.11, it is found that channel 4 signal keeps dropping, which means the output gate driving voltage for the up leg MOSFET of the slow switching leg cannot remain still during switch-on period. By comparing the test result with the breadboard test result shown in Figure 5.6 , it is assumed that the gate driving voltage decreasing problem is due to the small capacity of the bootstrap capacitor. Because in the breadboard test, the input PWM signal is 65KHz, while in this PCB test, it is 50Hz. So the same capacitor may not be able to maintain the V_{gs} in the 50Hz situation. In order to testify the assumption, a pair of simulation was done and the results are shown as Figure 5.12.



(a) $2\mu F$ bootstrap capacitor



(b) $20\mu F$ bootstrap capacitor

Figure 5.12. Comparative simulation results with two different bootstrap capacitor($2\mu F$ and $20\mu F$)for confirming the assumption of low capacitance will lead to V_{gs} decreasing for the up leg MOSFET in the slow switching leg. The up plane represents the output V_{gs} signal.The down plane represents the input PWM signal(50Hz).

As indicated by Figure 5.12a, the upper leg V_{gs} will decrease when the input PWM signal is 50Hz with $2\mu F$ bootstrap capacitor. While for $20\mu F$, the V_{gs} will remain square wave as indicated in Figure 5.12b. The simulation results validate the assumption.Therefore, the bootstrap capacitor for the slow switching driving circuit need to be larger and the desired value remains to be tested. Meanwhile, it is noticed from Figure 5.12 that there is $2.4\mu S$ shoot-through period. But no dead time circuit is

implemented for the slow switching leg. It is because this shoot-through issue will be prevented by the zero-crossing current spike mitigation method to be discussed in the next chapter. Besides, even there is no dead time circuit implemented for the slow switching leg gate driving circuit, there is still delay existed between the V_{gs} of the two switches, one of the reasons is due to the default dead time(75 ns) implemented in the gate driver 2EDL. The parasitic capacitance may also lead to the delay issue. Due to time limitation, this will be investigated in the future work.

For the test result for the fast switching leg, the result waveform is shown as Figure 5.13

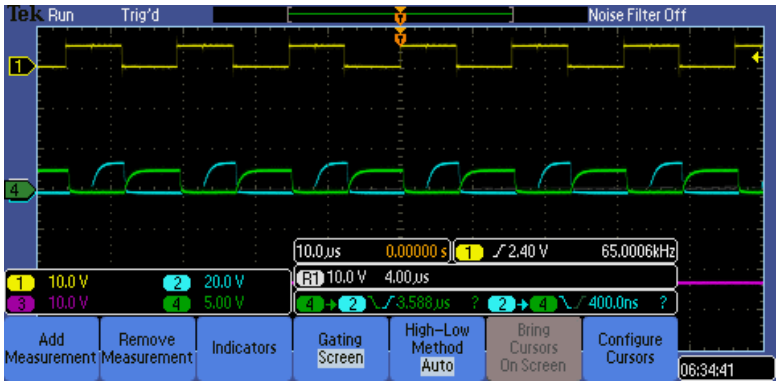


Figure 5.13. Gate driver test result on fast switching leg. channel 1 represents the input PWM signal for the up leg MOSFET. channel 2 represents the input PWM signal for the down leg MOSFET. channel 3 represents the output gate driving signal for the up leg MOSFET.channel 4 represents the output gate driving signal for the down leg MOSFET(with $\frac{1}{5}$) scaling ratio caused by the isolation probe.

Figure5.13 shows that the dead time period between the falling edge of channel 2 (down leg MOSFET) and the rising edge of channel 1 (up leg MOSFET) approximately fits with the simulation result shown in Figure 5.9. But the dead time period between the falling edge of channel 4 (up leg MOSFET) and the rising edge of channel 2 (down leg MOSFET) is approximately $3.588\mu S$ and it is much bigger than the 350 ns from the simulation result shown in Figure 5.9. This is assumed due to the non-ideal trace path for dead time circuit. The trace path can be found in Figure G.3. The confirmation of this assumption is not finished due to time limitation.

In this chapter, gate driver chip selection considerations were presented firstly. In order to meet the requirement of gate driving voltage $\geq$8V, output current $\geq$ 2.1 A and can support floating gate condition, half bridge gate driver chip 2EDL was selected. Then the driving circuit design regarding the effect of gate charging resistor R_{g1} and gate discharging resistor R_{g2} was analyzed. After that, the designed gate driving circuit was tested on breadboard for the tuning of R_{g1} and the results show that when $R_{g1} = 43\Omega$ and $R_{g2} = 5\Omega$, both fast switching leg and slow switching leg can function satisfactory. Further more, dead time explained for the fast switching leg was explained and the simulation result shows there will be around 350 ns and 400 ns dead time period at the status crossing point of the two switches. Finally, the PCB of the gate driver was implemented. Test result for the slow switching leg driving circuit has up leg V_{gs} decreasing issue and it was assumed due to the low capacity of the bootstrap capacitor and the optical capacitance remains to be investigated. The assumption was validated by the simulation. However, the down leg MOSFET V_{gs} delay issue was assumed due to bad trace planning and has not been testified yet due to time limitation.

Chapter 6

Control board design

In order to have an isolated ground plane and save the PCB testing period, the control board was designed separately. All the functional circuits included in the control board are illustrated in Figure 2.1. This chapter will discuss about the parameters retuning due to the power rate change. The proposed method for the zero-crossing current spike issue as discussed in Section 1.2 will be displayed. Afterwards, the simulation of the control board implemented in LTspice will be presented and discussed. In the end, the designed control board PCB along with the tests on the PCB will be introduced and analyzed.

6.1 Controller ICE1 related parameters retuning for the control loop

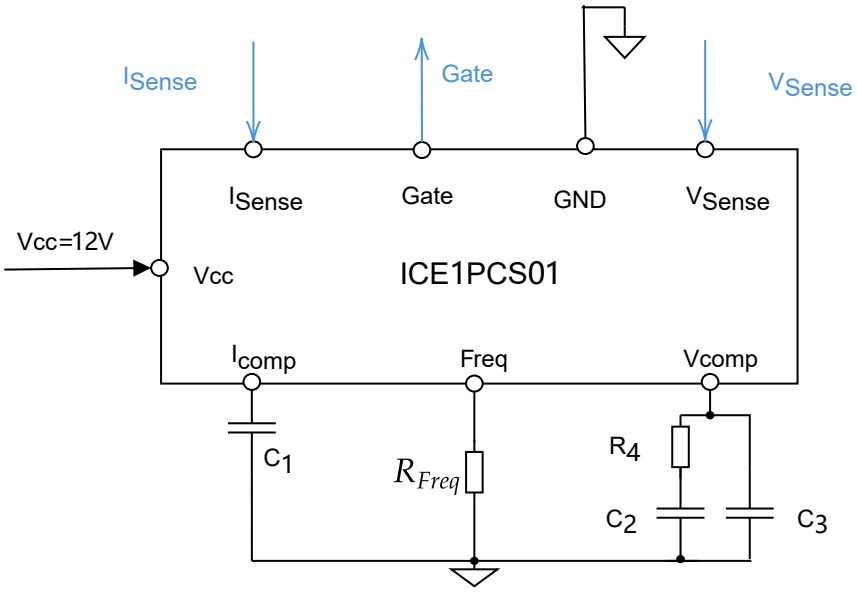


Figure 6.1. Analog controller ICE1PCS01 application circuit

The application circuit of the controller ICE1 adopted in the project is shown as Figure 6.1. It is also indicated that it needs other functional circuits to be able to applied for bridgeless Totem-pole PFC topology. All the functional blocks needed to be implemented in the control board are shown in Figure 2.1.Since the control scheme of the analog controller was introduced in Report [1] before and therefore it will not be presented in this report. However, as discussed in Section 4.1, the power rate was reduced to 400W and the power inductor and DC capacitor were re-calculated to be 1900 μH and 80 μF. And accordingly, the current loop transfer function and voltage loop transfer function need to be retuned. The parameters need to be retuned are shown as Figure 6.1, which includes the current compensation related capacitor C_1 and the voltage compensation related resistor R_4 and capacitors C_2 and C_3. The retuning process and corresponding frequency response will be shown in the following subsections.

The current loop transfer function is shown as Equation (6.1):

$$G_c(s) = \frac{\frac{K_1 \cdot R_{sense} \cdot V_{out}}{K_{FQ} \cdot M_1 \cdot M_2 \cdot L}}{s \cdot (1 + s \cdot \frac{K_1 \cdot C_{icomp}}{M_1 \cdot g_{OTA2})}} [6] \tag{6.1}$$

And based on AppendixB, C_{icomp} is retuned to be 14.5 nF. With the retuned C_{icomp} value, the current loop frequency response bode plot is shown as Figure 6.2.

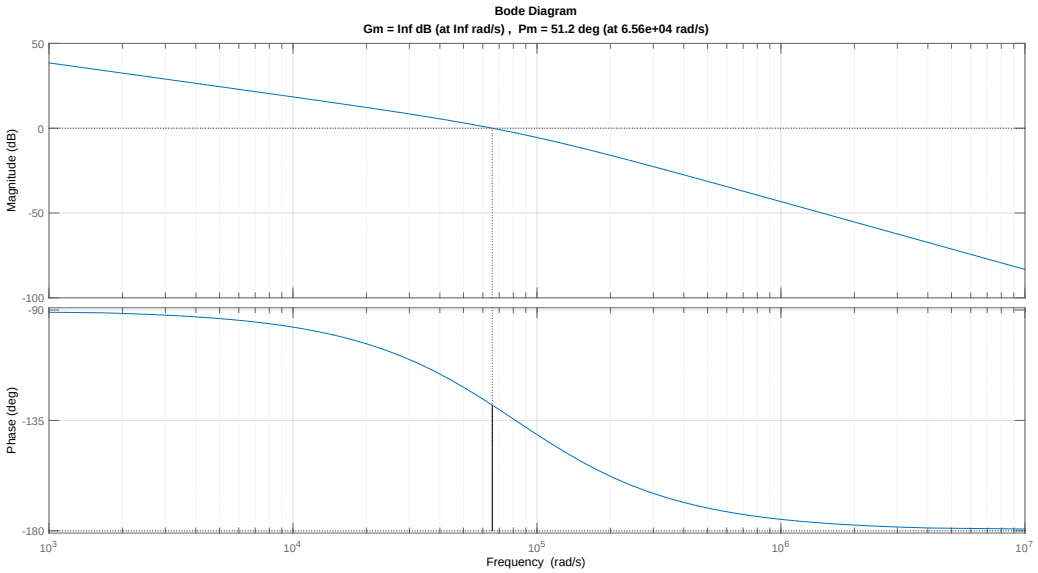


Figure 6.2. Bode plot of current loop with retuned C_{icomp}

Figure 6.2 indicates that the current loop cut-off frequency is approximately $6.56 \cdot 10^4 rad/s$, which equals to 10KHz roughly. And the phase margin is 51.2° . So the retuned the current loop can not only filter out the switching current ripple but also have good stability.

The voltage loop retuning MATLAB script is shown in AppendixF. R_4 is retuned to be 1 $K\Omega$, C_2 is retuned to be $8\mu F$ and C_3 is retuned to be $1\mu F$. The corresponding voltage loop bode plot is shown as Figure 6.3. Figure 6.3 shows that that the voltage loop cut-off frequency is approximately $53.5 \cdot rad/s$,

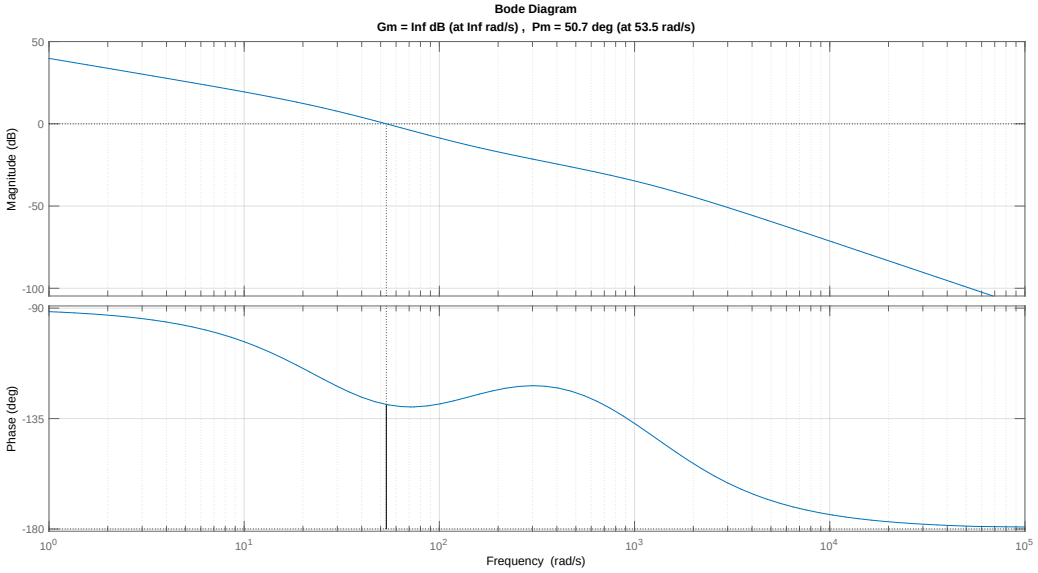


Figure 6.3. Bode plot of voltage loop with retuned C_2, C_3 and R_4

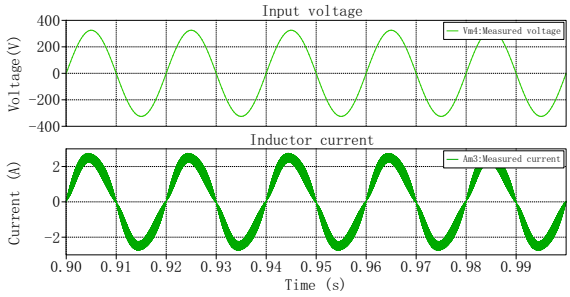
which equals to 8.5Hz roughly. And the phase margin is 50.7° . So the retuned the voltage loop can not only filter out the 100Hz output V_{DC} ripple but also have good stability.

Based on the frequency response, the retuned the parameters can meet the current loop and voltage requirement for noise filtering and having enough phase margin. Next section will confirm whether the

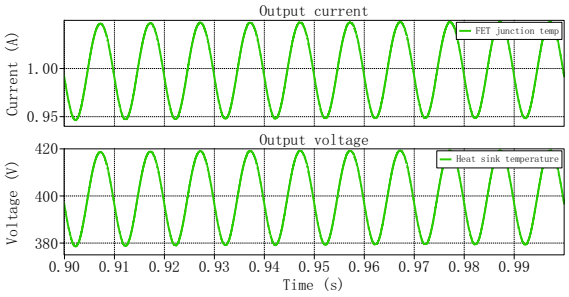
simulation model can work as expected with the retuned parameters.

6.1.1 PLECS simulation results based on the retuned parameters

With the re-calculated AC inductor, DC capacitor value in Section 4.1 and the retuned parameters discussed in the previous section, the new PLECS simulation results are shown as Figure 6.4.



(a) Current and voltage waveform of input side



(b) Current and voltage waveform of output side

Figure 6.4. PLECS steady state simulation results with retuned parameters

Figure 6.4a shows that with retuned parameters, the input current can remain sinusoidal and it can keep in phase with input voltage during steady state. Figure 6.4b shows that with retuned parameters, the steady state output voltage is 400V and its ripple is within $\pm 20V$. The current waveform shares the same pattern as the voltage waveform and its average value is 1A. So the output power is 400W as expected.

6.2 Zero-crossing point detection circuit

Two possible reasons can lead to the V_{AC} zero-crossing point input current spike issue were discussed in Section 1.2 before. One is because of the fast switching switches S_1 and S_2 duty ratio variation at the zero-crossing point. Another reason is due to the slow reverse recovery characteristic of the slow switching switch S_3. In order to tackle this issue, one potential analog solution implemented in LTspice is shown as Figure 6.5 :

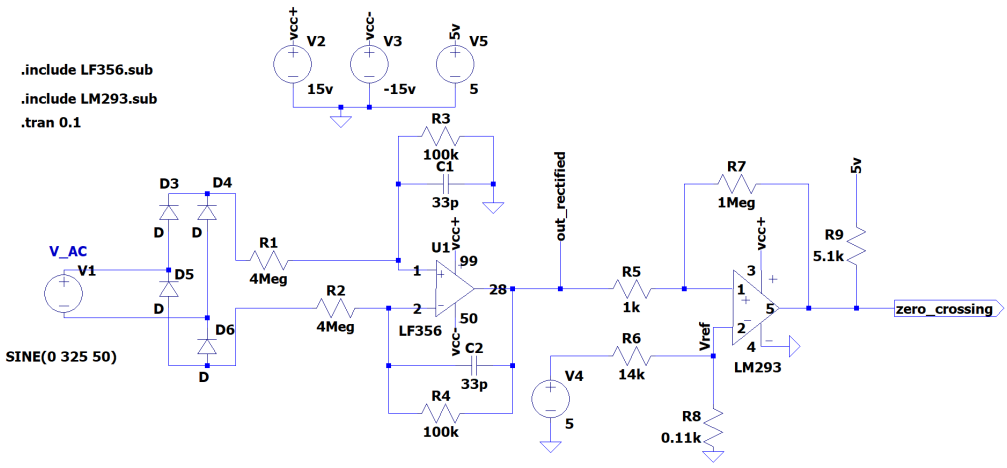


Figure 6.5. LTspice model of the proposed analog solution for zero-crossing current spike mitigation

The general idea of the solution is by turning S_2,S_3 and S_4 OFF for multiple switching cycle to give enough time for S_3 to be fully reverse recovered, and meanwhile can skip the duty ratio variance period. As shown in Figure 6.5,the input voltage is rectified by a diode bridge firstly. Then the rectified positive half-sinusoidal signal is scaled down by an op-amp LM356. After that, by comparing the rectified signal with a DC reference voltage V_{ref}, the final zero-crossing signal is derived. The LTspice simulation result is shown as Figure 6.6.

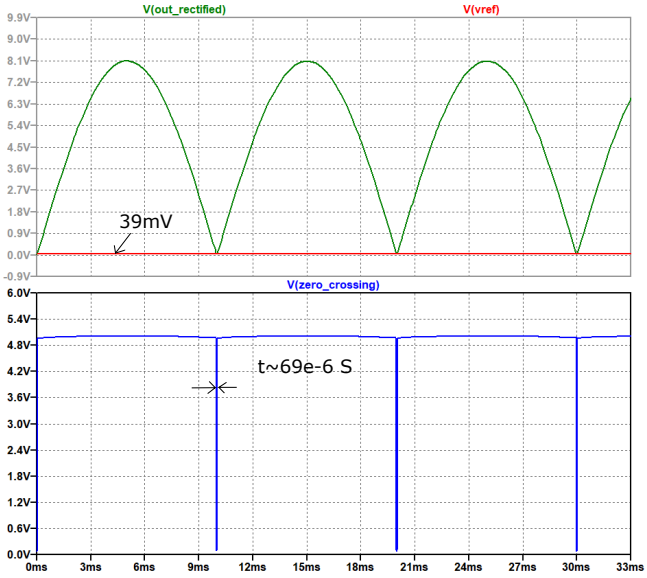


Figure 6.6. LTspice simulation result of the proposed analog solution for zero-crossing current spike mitigation

Based on Figure 6.6, S_2,S_3 and S_4 will remain being OFF for around $69\mu S$ with all the parameters indicated in Figure 6.5. And this time equals to roughly 4 switching period. According to the real zero-crossing spike condition, the length of this time can be tuned by either enlarging the amplitude of the rectified voltage or lowering the amplitude of the reference voltage.

6.3 Gate logic circuit

With the proposed zero-crossing current spike mitigation method, the gate logic is then implemented as Figure 6.7.

The general interpretation of the gate logic shown in Figure 6.7 is as below: During the positive half cycle, the output of the polarity detection should be high (5 V), combined with the output of the

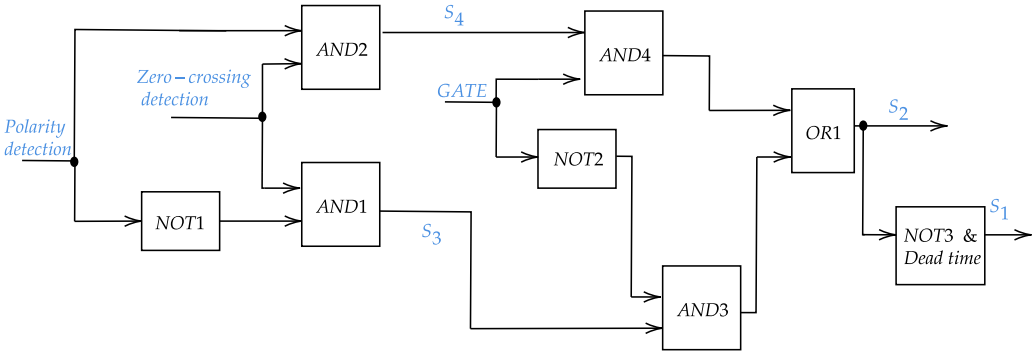


Figure 6.7. Block diagram of the gate logic circuit

zero-crossing point detection circuit, it can get the gate signal for S_4. While for S_3, it remains OFF. During the negative half cycle, the output of the polarity detection should be low (0 V), and then reversed to high by NOT1. Combined with the output of the zero-crossing point detection circuit, it can get the gate signal for S_3. While for S_4, it remains OFF. S_2 will be ON when there is output signal GATE from controller ICE1 and S_3 or S_4 is ON. And S_2 signal goes through the dead time circuit discussed in Section 5.4 and inverse block will get S_1.

The final control board LTspice simulation model can be found in Appendix C. The zero-crossing point of the simulation result is shown as Figure 6.8.

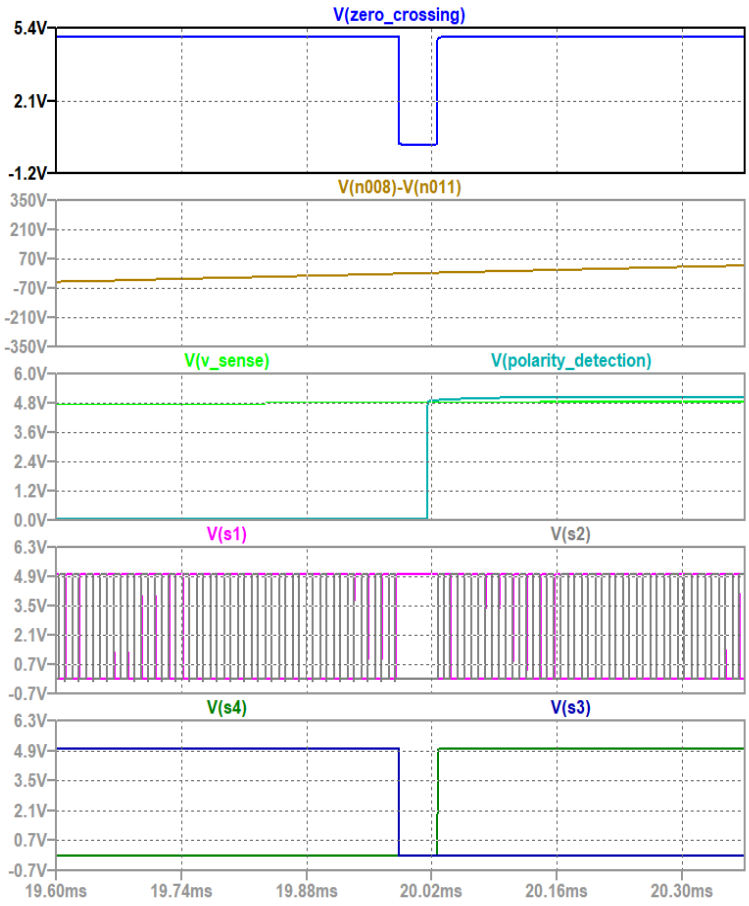
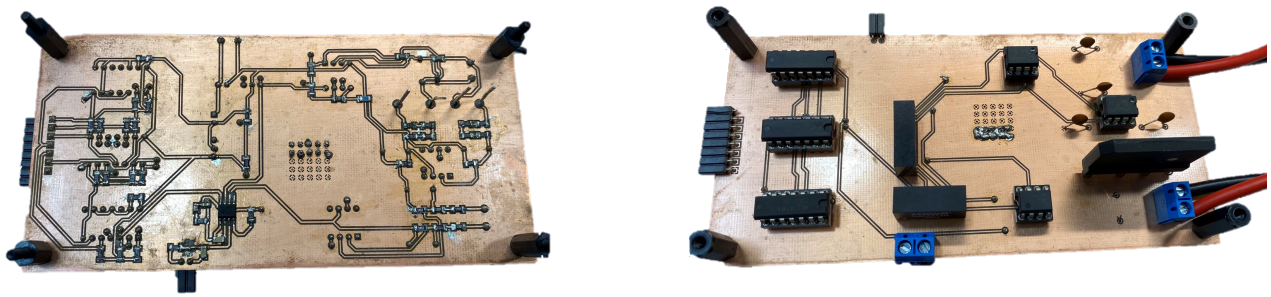


Figure 6.8. LTspice simulation result of the control board at one of the zero-crossing points of V_{AC}

Figure 6.8 shows that at the zero-crossing point when V_{AC} changes from negative half cycle to positive half cycle, the polarity detection circuit output will change from low to high. The output of the zero-crossing detection circuit will be low for around 60 μS, and S_2,S_3 and S_4 will be OFF during the period. The simulation results go as expected. But the validity of the proposed the control board circuit need to be tested. The next section will introduce about the PCB design of the control board as well as the experimental test on the printed PCB.

6.4 PCB design and test of control board

The PCB design of the control board is based on the LTspice simulation model discussed above. The schematic, BOM and PCB overview of the control board implemented in Altium designer can be found in Appendix F. The final soldered control board is shown as Figure 6.9.



(a) Top layer overview

(b) Bottom layer overview

Figure 6.9. Gate driver board

As introduced before, the control board includes voltage sensing circuit, polarity detection circuit, zero-crossing detection circuit, PWM logic circuit and controller ICE1 and its complementary components for current and voltage loop compensation. So the following sections will introduce the control board PCB tests for each of the function circuits. All the tests will be conducted with a signal generator as input signal for safety concern. Therefore, some of the parameters need to be adjusted to be able sensing the small voltage range input signal. The detailed testing information will be introduced in the following sections.

6.4.1 Voltage sensing circuit test

The voltage sensing circuit is designed to sense the 400V output DC voltage. In order to test it, the scaling ratio of the sensing circuit was decreased to $\frac{1}{10}$ instead of the original $\frac{1}{81.63}$as indicated in Figure C.2. In order to simulate the real output voltage, 1 V DC offset and a 0.1 V 100 Hz sinusoidal ripple was configured as the input signal. The updated test circuit schematic shown as Figure 6.10.

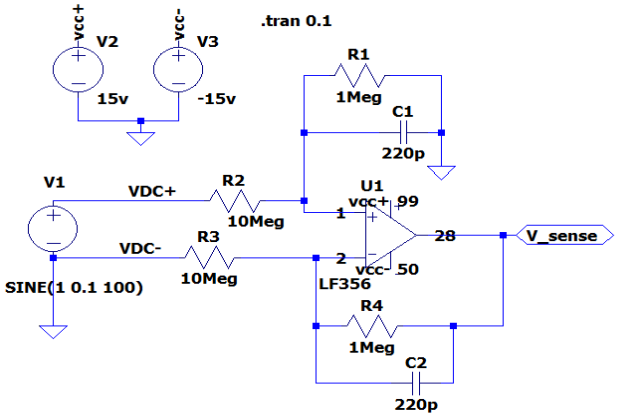
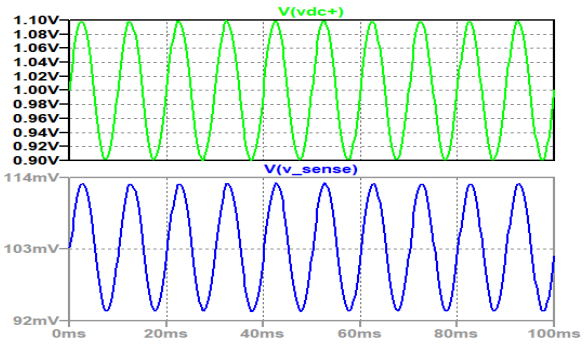
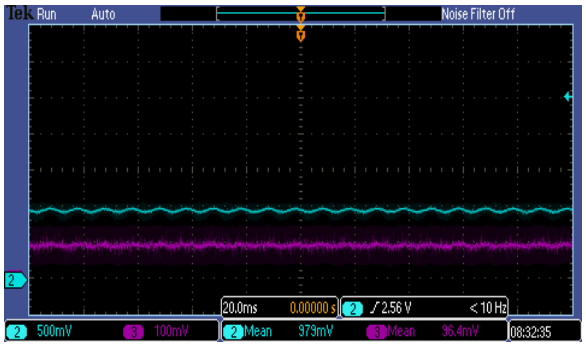


Figure 6.10. Voltage sensing circuit testing schematic with modified $\frac{1}{10}$ scaling ratio

The expected output signal from simulation and the real test result of the control board voltage sensing circuit are shown as Figure 6.11.



(a) Expected test result of the control board voltage sensing circuit



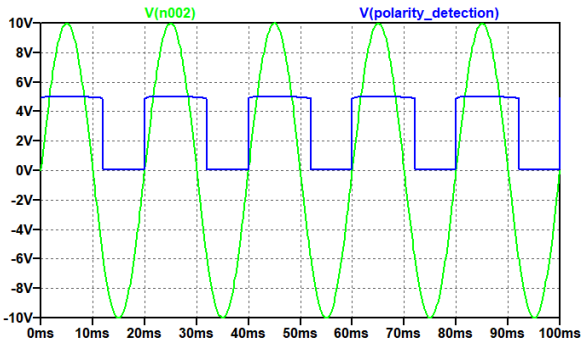
(b) Real test result of the control board voltage sensing circuit

Figure 6.11. Expected and real test results of the control board PCB voltage sensing circuit with modified $\frac{1}{10}$ scaling ratio

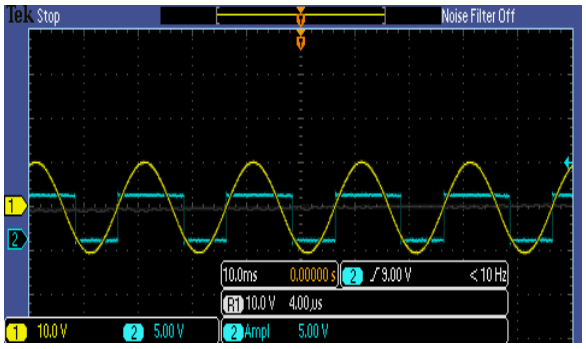
Figure 6.11a shows that the output should be follow the same pattern ad the input voltage but with a scaling ratio of $\frac{1}{10}$ based on the simulation result. Figure 6.11b shows that the real test result fits with the expected result with a a scaling ratio of $\frac{1}{10}$. But the output waveform is noisy and not as clearly sinusoidal as the input voltage.

6.4.2 Polarity detection circuit test

For the polarity detection circuit of the control board PCB, the test schematic remains the same as the original design shown in Figure C.2. But he input signal changes from 325 V to 10 V. The expected output signal from simulation and the real test result of the control board polarity detection circuit are shown as Figure 6.12.



(a) Expected test result of the control board polarity detection circuit



(b) Real test result of the control board polarity detection circuit

Figure 6.12. Expected and real test results of the control board PCB polarity detection circuit with 10 V 50 Hz sinusoidal input

By comparing Figure 6.12a and Figure 6.12b, it can conclude that the polarity detection circuit of the control board PCB can work as expected.

6.4.3 Zero-crossing point detection circuit test

The tested schematic of the zero-crossing detection circuit in the control board PCB is shown as Figure 6.5. But as the input changes to 10 V 50 Hz sinusoidal input, the $R_1, R_2, R_3 and R_4$ value was changed

to 100 $k\Omega$. The final test result is shown as Figure 6.13.

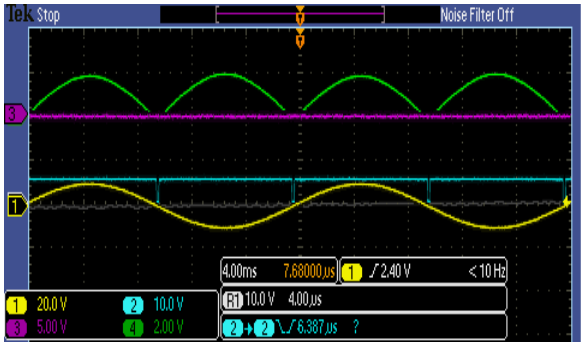


Figure 6.13. Test result of the control board PCB zero-crossing detection circuit. Channel 1 represents the input signal. Channel 2 represents the output signal. Channel 3 represents the reference voltage and Channel 4 represents the rectified voltage.

Figure 6.13 indicates that by rectifying the input sinusoidal signal and comparing the rectified signal to a reference DC voltage scaled from a 5V DC voltage by a resistor voltage divider, a zero-crossing period was detected and the output changed from high level to low level. All the signals tested from the control board PCB follows the pattern as the simulation result shown in Figure 6.6. Therefore the the zero-crossing detection circuit of the control board PCB can work as expected.

6.5 Controller ICE1 circuit with its supplementary components

As indicated in Figure 6.1, with the output of the voltage sensing circuit (adjusted to 5V), current sensing output(-0.1V, 100Hz) and its supplementary components, the output GATE signal is expected to have the pattern as the S_2 signal shown in Figure 1.4. However, there is no output GATE signal from the test. By checking the connections with multimeter, it was found that the current sensing input trace was short circuit due the clearance is not well cleared. But the trace was damaged after trying to solve the short circuit issue. The problem can be found in Figure D.4 .An attempt was made to bridge the broken trace but still failed. Due to time limitation, the control board cannot be re-produced and tested. Since the GATE signal of the controller is the input of the PWM logic circuit, the PWM logic circuit test was not finished either.

In this chapter, the control loop of controller ICE1 was retuned in Matlab to fit with the new power rate 400W. With the retuned parameters($R_4 = 1k\Omega$, $C_2 = 8\mu F$ and $C_3 = 1\mu F$), the PLECS simulation was conducted to test the validity of retunig result. Then a solution for mitigating zero-crossing current spike was proposed and simulation result shows the method can generate a $69\mu s$ period to keep S_2, S_3 and S_4 OFF. After that, the PWM logic was explained. Furthermore, the simulation result of the control board was presented. Due to lack of the simulation model of the controller ICE1, a ideal GATE signal with 50% duty ratio was implemented in the control board simulation model. By the end, the soldered control board PCB was presented and the tests for the functional circuits in the control board were tested. For the voltage sensing circuit, polarity detection circuit and zero-crossing point detection circuit, the test results indicate that the control board PCB can realise those functions as expected. But there is harmonic issue for the voltage sensing circuit. And for the controller and PWN logic circuit, the test was not finished due to the damage of the current sensing trace. And the modification of the control board PCB cannot be done due to time limitation.

Chapter 7

Discussion

In this chapter, the proposed zero-crossing current spike mitigation method will be further discussed. Then the overall analog control designing process will be reviewed. And in the end, factors that may lead to a difference in the simulation results and experimental implementation results will be summarized.

7.1 Zero-crossing current spike mitigation method

As mentioned in Section6.2, the period of S_2, S_3 and S_4 being turn off during zero-crossing point can be tuned by changing the amplitude of the rectified voltage or the amplitude of the reference voltage. However, the longer that period is, the less efficiency and worse power factor it will get. So the optimization of the zero-crossing period needs to be further tuned during the experimental stage. Besides, as the zero-crossing detection result depends on the crossing points of the rectified signal and the reference DC voltage signal and they both have low amplitude (39 mv indicated in Figure 6.5), it is sensitive to the noise and can generate a wrong zero-crossing signal if it is interfered by the noise. If so, then the input current will be distorted and the efficiency and power factor will be low. So in order to have a fast and high interference immunity input voltage phase detection method, phase-locked loop (PLL) can be implemented as suggested by Reference[13]. How to implement and tune PLL remains to be investigated. Apart from that, the solution offered in Reference[13] is realized by STM32F334 microcontroller, which leads to the next topic about analog control and digital control comparison.

7.2 Analog control and digital control

This project has been all implemented with analog control. With analog control, all the sensed signal is transmitted continuously by electrical components, which will not only consume power during the transmission but also will be exposed to a lot of noise. And if the signal transmitted has a small amplitude, it can be interfered severely by the noise. Compared with analog control, digital control can save part of the power loss because the signal is transmitted discretely. Besides, a lot of signal processing can be executed by the microcontroller, which can improve the interference immunity. Therefore, a potential solution for improving the noise immunity of the experimental setup is through digital design.

7.3 The difference between the experiment results and simulation results

In this project, LTspice simulation was always conducted firstly and the simulation result will be regarded as the reference for the experiment result. However, there are some factors may lead to the difference between the simulation results and experiment results. The first factor is about the parasitic capacitance and inductance. As for the tested PCB, pairs of parallel conducting traces on the PCB that are separated by clearance will form parasitic capacitors. Similarly, when conductors form a loop

over PCB and it will form parasitic inductors. One example is about the gate driver test introduced in Section 5.5. The is almost no delay in the fast switching leg down MOSFET based on the simulation result. However, there was around 3.6 μS delay happened in the experiment result. In order to better simulate the real effect of the tested PCB's parasitic components, Ansys Q3D parasitic extraction & analysis can be further implemented.

Another factor is the EMI. For LTpsice simulation, the small voltage signal can be calculated and simulated free of the noise interference. While for the experiment, the EMI noise will disturb the signal transmission and the result may be quite noisy and do not match the simulation result exactly. One example is the voltage sensing circuit test shown in Section 6.4.1. And the potential solution for this issue is as discussed above, by implementing digital control and manipulating small voltage signal by a microcontroller instead of analog circuits.

Chapter 8

Conclusion

The problem statement of this project is described as:

> *" Implementing the efficiency analysis model on the existing PLECS simulation of the single-phase 3.6 kW bridgeless Totem-pole PFC, developing a method to mitigate the zero-crossing current spike and experimentally verify the simulation results of the design."*

To answer the proposed research question, the whole project was divided into three stages. The first stage is introducing the basic facts about bridgeless Totem-pole PFC and offering two possible reasons for the zero-crossing current spike issue. The second stage is implementing the efficiency analysis model in PLECS. And the third stage is experimental design and verification.

For the first stage, Chapter1 offered a general introduction about the connection between this project and the 9th semester project and introduced some background information about bridgeless Totem-pole PFC. The zero-crossing duty ratio variation issue and the consequential current spike issue were also investigated in that section.

For the efficiency analysis stage, the major loss components of the system, which are the switching loss and conduction loss of MOSFETs, were analyzed and modeled in PLECS as loss look-up tables shown in Section 3.1. And then the methodology of the loss calculation with PLECS' average function block and impulse average function block was introduced. After that, one assumption of omitting the switching loss of slow switching was proposed and one pair of simulation results comparison was conducted. The efficiency simulation result not only confirmed the validity of the assumption about omitting the switching loss of the slow switching leg MOSFETs but also got an efficiency of 99.07% of the designed model with selected components, and it is higher than the specified 97% efficiency. Although only the switching and conduction loss of MOSFETs were considered, there was about 2% of the total power (72 W) remained as the loss capacity for the input inductor and output capacitor, which can be referred during the future inductor design. Furthermore, the simulation result comparison indicated a potential method for improving the efficiency, which is alternating slow MOSFETs IPW to a new MOSFET with lower $R_{ds(on)}$.

For the experimental designing and verification stage, the whole system was divided into three boards, which are the power board, the gate driver board and the control board. Each of the boards was individually designed, simulated and experimentally verified.

Regarding the power board, as the input inductor with expected inductance and saturation current was unavailable and it will challenging to be self-made considering the time limitation, it was therefore altered to an inductor available in the laboratory with lower saturation current. And consequently the output power rate decreased from 3.6 kW to 400 W. After that, a starting period inrush current damping method realized by the combination of NTC thermistor and relay was introduced and the PLECS simulation result validated that method. Afterward, the PCB design considerations regarding the trace width, components layout and ground plan schedule were listed. And the designed power board PCB was displayed alongside.

Regarding the gate driver board, four topics were discussed in detail. The first topic was about the gate driver chip selection criteria. The second topic was about the tuning of the gate charging resistor

R_{g1} and gate discharging resistor R_{g2}. With analytical calculation and breadboard tuning, R_{g1} and R_{g2} were determined. The third topic was about the dead time circuit. Making use of the RC delay circuit and inverter can realize the signal delay function. And by tuning the RC circuit parameters in LTspice, the designed dead time circuit will generate around 400 ns dead time for the MOSFETs in the fast switching leg and prevent the shoot-through. The last topic was about the gate driver PCB test. The test results indicated that the designed gate driver can realize its function but with two issues remaining to be improved. One issue is the low capacity of the slow gate driver bootstrap capacitor. Another issue is the delay of the gate driving voltage for the down MOSFET in the fast switching leg.

Regarding the control board, the controller-related parameters (C_2, C_3 and R_4) were firstly retuned in MATLAB to fit with the new power rate. The validity of the retuning was confirmed by the PLECS simulation result shown in Section 6.1.1. Then the zero-crossing current spike mitigation method was proposed and explained with the LTspice simulation result of the proposed circuit. Furthermore, individual tests on the designed control board PCB regarding the supplementary circuits were conducted and analyzed with reference to the LTspice simulation results. With the help of LTspice, it can not only confirm a possible failure reason without re-making a PCB, but also provide expected test results for reference.

Finally, it can be concluded that with the selected MOSFETs (MOSFET ST as fast switching MOSFETs and IPW as slow switching MOSFETs) and designed supplementary circuits for ICE1 controlled 3.6 kW bridgeless Totem-pole PFC , it can meet all the specifications listed in Section2.1. However, it remains to be confirmed about the validity of the proposed zero-crossing current spike mitigation method for mitigating the zero-crossing current spike caused by the duty ratio variation issue and slow reverse recovery issue of S_3 and S_4. Furthermore, although with the LTspice simulation result, the gate driver board design and part of the control board design can be verified to be correct or failure reason confirmed, the whole designed system needs to be further modified, implemented and experimentally verified due to the time limitation.

Chapter 9

Future work

9.1 Gate driver modification

There are still two aspects of the gate driver PCB need to be modified. One is about the slow switching leg gate driver bootstrap capacitance determination. Another is about the trace optimization of the date driving path for the fast switching leg down MOSFET.

9.2 Control board modification

For the control board, as the current sensing circuit was broken, the whole control board need to be re-produced. Apart from that, the voltage-sensing circuit noise issue may also need to be improved.

9.3 Efficiency analysis based on PLECS model

Efficiency analysis conducted in Chapter 3 is based on a simplified model with consideration only limited to the conduction loss and switching loss of the switching devices. However, the input inductor and output capacitor have equivalent series resistor (ESR) and it will also consume certain amount of power, which means the real efficiency is lower than the calculated efficiency in Chapter 3. One example shown in Reference [9] calculated that the loss consumed by the inductor and capacitor reaches 22% of the total loss. Therefore, in order to more precisely calculate the efficiency, the ESR of the inductor and capacitor need to be measured and the loss consumed by the ESR needs to be calculated and considered. Besides, the dead time, the zero-crossing current spike mitigation method and the all the power ICs will also lower the efficiency. However, as mentioned in Chapter 2.4, this part of the loss is not included in the study range due to time limitation.

9.4 Control loop tuning

The control loop tuning in Chapter 6 is based on the ideal sensing signal transmission. There is no delay considered. While in the PCB test stage, the delay was found unavoidable. Therefore, the control loop parameters may need further tuning during the whole setup testing stage as it is a closed-loop control instead of open-loop control.

9.5 PCB soldering and testing

The PCB designing, soldering and testing occupies the most of the time of this project. For the PCB designing, optical trace planning can be further studied. As learned from the test results of the gate driver PCB and control board PCB, bad trace planing will not only have noise but also may introduce signal delay. For the PCB soldering, it needs more practice. During the period of soldering gate driver

and control board, mistakes keep happening such as not well connected to the pad (leading to the signal floating and discontinuous), short circuit and surface mounted chip pin open circuit, etc. In order to find the soldering issue and correct the issue, it needs to refer to the PCB schematic and using multimeter or oscilloscope to measure the ports accordingly. And for the PCB testing, as the input signal may degrade to small rate, some components values may need to be adjusted. As the copper pads and traces are relatively fragile with the manufacturing technique available in the lab, it needs to be careful. Otherwise it may break the trace or pads and needs to re-make the PCBs.

9.6 Design inductor and recover the design for 3.6KW output power rate

Based on Chapter3, it concluded that there is 2% of the total power, which is 72 W, can be spared on the power dissipation of the input inductor and DC link capacitor. Apart from that, Table 4.1 also offers the calculated value for the input inductor. Therefore, designing the input inductor and building the originally designed 3.6 kW bridgeless Totem-pole PFC reamains to be done.

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Appendix A

Schematics of PLECS thermal model

The switching loss and conduction loss of MOSFETs calculation diagram implemented in PLECS is shown as FigureA.1.

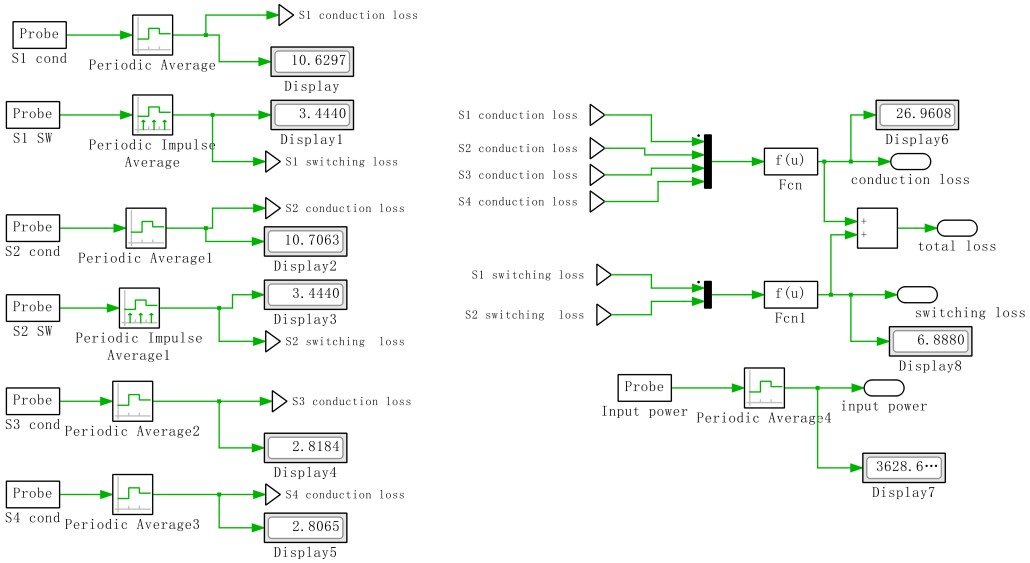


Figure A.1. The switching loss and conduction loss calculation PLECS diagram of the proposed 3.6KW brideless Totem-pole PFC PLECS thermal simulation model

The overall schematic of the proposed thermal model implemented in PLECS is shown as FigureA.2.

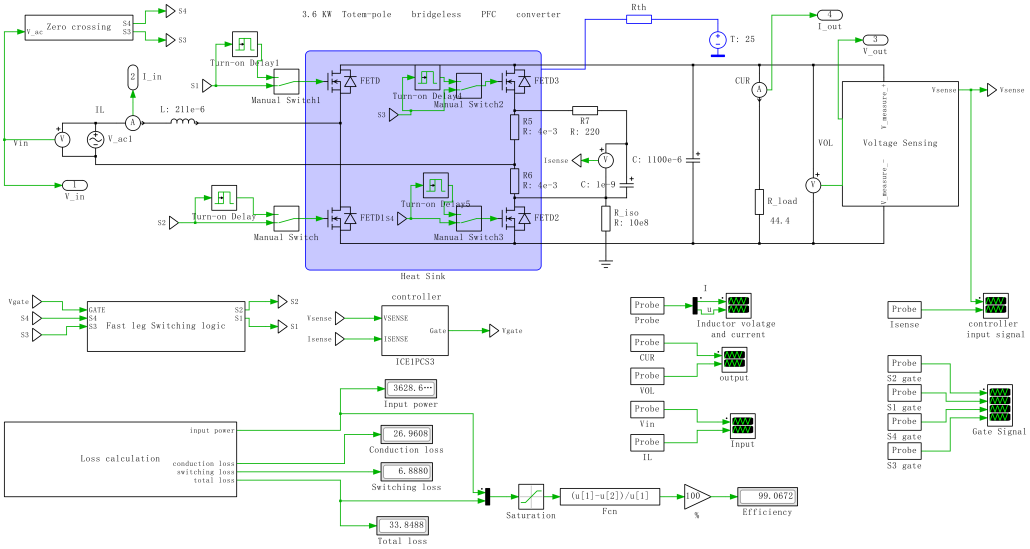


Figure A.2. The schematic of the proposed 3.6KW brideless Totem-pole PFC PLECS thermal simulation model

Appendix B

Transfer function derivation and Matlab script for voltage control loop

According to the controller ICE1 design guide [6], the non-linear gain block lookup table is shown in Table B.1.

Vcomp	M1	M2
0	0.048	1.33e-2
1.5	0.048	1.33e-2
1.85	0.0517	1.92e-2
2	0.0551	3.86e-2
2.5	0.101	1.79e-1
3	0.184	3.35e-1
3.5	0.316	5.08e-1
4	0.477	7.16e-1
4.5	0.629	9.83e-1
5	0.752	1.368
5.5	0.846	1.879
5.6	0.888	1.968
6	0.906	1.982
6.5	0.906	1.987
7	0.906	1.987

Table B.1. Non-linear gains of the non-linear gain block of the controller[6]

Based on the TableB.1 as well as Reference [6], the Matlab code for calculating the transfer functions for the voltage and current loop are shown as below (the transfer function derivation will not be explained as it was included in Report[1] before):

```
clc;
clear all;
close all;

Po = 400;
Vout = 400;
Rsense = 0.004;
Vinrms = 230;
I_Lrms = Po/Vinrms;
KFQ = 9.183;
K1 = 7;
%%%%%%%calculate M1,M2,GNON
% the M1M2_cal used to find the M1 and M2 values in the look-up table
M1M2_cal = ( I_Lrms*K1*Rsense*Vout ) / ( KFQ*Vinrms )

% Since M1M2_cal is calculated to be 0.0092 it can be seen in the non-linear ...
    characteristic table
%that it is between the value given by Vcomp = 2 and Vcomp =2.5
% Linear interpolation is used to determine the M1 and M2 values that
% correspond to the M1M2 = 0.0092
```

```
% The values used for the interpolation is found in the table for the
% non-linear gains
Vcomp1 = 2;
Vcomp2 = 2.5;
M1_1 = 0.0551;
M2_1 = 3.86e-2;
M1_2 = 0.101;
M2_2 = 1.79e-1;
M1M2_1 = 2.127e-3;
M1M2_2 = 1.808e-2;

% Linear interpolation of the Vcomp, M1 and M2 value
Vcomp = Vcomp1 + ( M1M2_cal-M1M2_1 ) / ( M1M2_2 - M1M2_1 ) * (Vcomp2 - Vcomp1)
% Vcomp is found to be 2.2224

M1 = M1_1 + ( M1_2 - M1_1 ) / ( Vcomp2 - Vcomp1 ) * (Vcomp-Vcomp1)
% M1 is found to be 0.0755

M2 = M2_1 + ( M2_2 - M2_1 ) / ( Vcomp2 - Vcomp1 ) * ( Vcomp-Vcomp1 )
% M2 is found to be 0.101

% The value of GNON is determined by the transfer function
% Delta(M1M2)/Delta(Vcomp) found in the design guide
GNON = (M1M2_2 - M1M2_1) / (Vcomp2 - Vcomp1)
% GNON is found to be 0.0319



%%%%%%%%%Gc,Gv and bode plot
% Input and output specifications for the converter
pc_rip = 0.20;          % Percent ripple in the current
% The inductor current rms value in steady state is given by
I_Lrms = Po / Vinrms;             % RMS AC input current under full load

% The Capacitor, inductor and output resistor values are given by
Cout = 80e-6;                  % New output capacitor
L =1900e-6;                      % New input inductor
Io = Po/Vout;                    % Average output current
Rout = Vout/Io;                  % Output resistor value

% Current averaging circuit
GOTA2 = 1.1e-3;                   % The gain from the op-amp in the current ...
    averaging cicuit
% f_ave needs to be 5 times smaller than the switching frequency
fs = 65e3;                       % Switching frequency - can be tuned
fave = fs/5;                     % The f_ave is chosen to be 5 times smaller than ...
    the switching frequency

% Determination of the Cicomp value to satisfy the requirement that the
% break frequency of the current averaging transfer function is 5 times
% smaller than the switching frequency
Cicomp = ( GOTA2*M1) / ( K1 * 2*pi*fave )
% The Cicomp is calculated to be 14.53 nF

% Calculation of the inherent pole of f23 of the transfer function of G23
f23 = 1 / ( 2*pi * ( K1*Rsense*Vout^3*Cout )/ ( KFQ*M1M2_cal*Vinrms^2 )  );

s = tf('s');
```

```
76  G23 = (Vout/(M1*M2)) / ( 1 + s/(2*pi*f23) );
77  G4 = 1/80;                  % Gain of the feedback loop for the sensed current
78  Gnon234 = GNON*G23*G4;
79
80  gOTA1 = 42e-6;              % Internal gain of the controller in the voltage loop
81
82  % The transfer function for the whole current loop is given by
83  Gc = ( ( K1*Rsense*Vout )/( KFQ*M1*M2*L ) ) / ( s * ( 1 + s*K1*Cicomp / ( M1 ...
        *GOTA2 )  ) );
84
85  % Bode plot for the current loop transfer function showing the gain and
86  % phase margin of the current loop controller. The 0 dB cross-over must be
87  % much lower than the switching frequency of 65 kHz
88
89  fig1 = figure('WindowState','maximized')
90  margin(Gc)
91  grid
92  f_cur_cross = 6.56e4 / (2*pi); % Cut off freequncy of current loop is 10 kHz
93
94
95
96  % The values for the external circuit of the voltage error controller is
97  % found by tuning the value until the break frequency for the whole voltage
98  % loop has a value around 10 Hz and the phase margin is above 45 degree
99  R4 = 1e3;       % Tuned value
100 C2 = 8e-6      % Tuned value
101 C3 = 1e-6;     % Tuned value
102 %genenral rule of thumb, C2 and C3 increase and R4 decrease
103
104 G1 = gOTA1 * ( 1+s*R4*C2 ) / ( (C2+C3) * s * (1 + s * (R4*C2*C3)/(C2+C3) ) )
105
106 fig2 = figure('WindowState','maximized')
107 margin(G1*Gnon234)
108 grid
109
110 f_vol_cross = 53.5 / (2*pi); % Cut off freequncy of voltage loop is  8.51 Hz
```

Appendix C

LTspice model of the designed gate driver and control board

The LTspice simulation model of the gate driver circuit is shown as below:

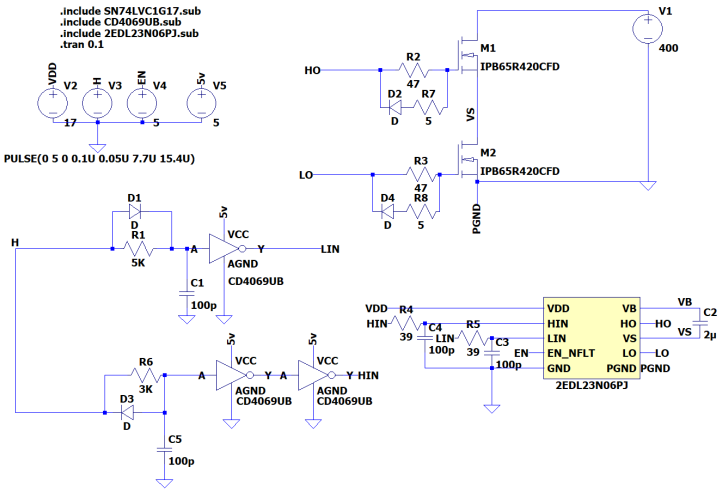


Figure C.1. LTspice simulation model of the gate driver board

The LTspice simulation model of the control circuit is shown as below:

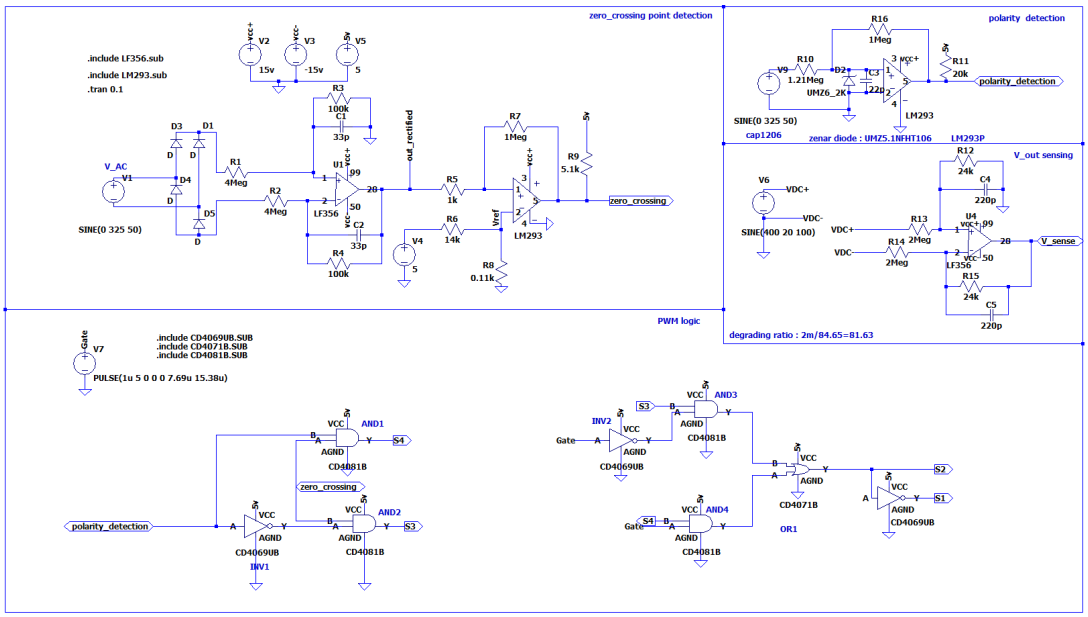


Figure C.2. LTspice simulation model of the control board

NOTE: as the LTspice file of the controller is not available, so the controller and its surrounding components can not be implemented. A simplified 50% duty ratio pulse is implemented to act as the GATE output signal of the controller ICE1.

Appendix D

Supplementary testing waveforms and figures

D.1 Gate driver simulation test waveform

Simulation result of gate driver circuit. The simulation parameters are as indicated in FigureC.1. As the LTspice file for the selected MOSFETs IPW and ST are not available. So in the simulation model, IPB65R42OCFD(share similar parasitic capacitance characteristic with IPW) from the LTspice library was used. And the simulation result is shown as Figure D.1.

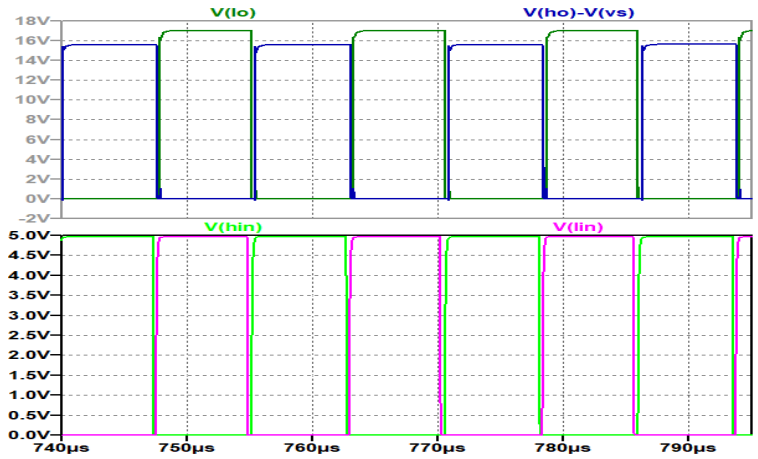
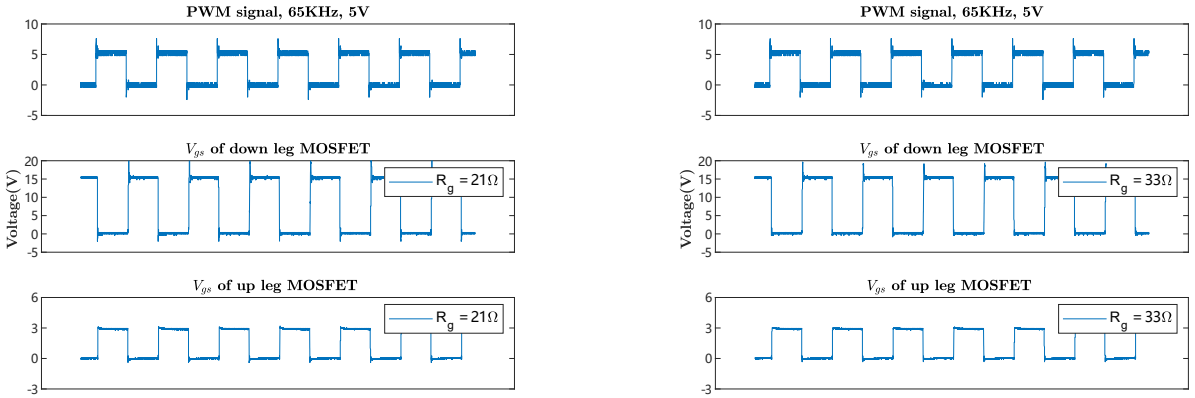


Figure D.1. Simulation result of the gate driver model shown in FigureC.1.

D.2 Gate driver breadboard test waveform

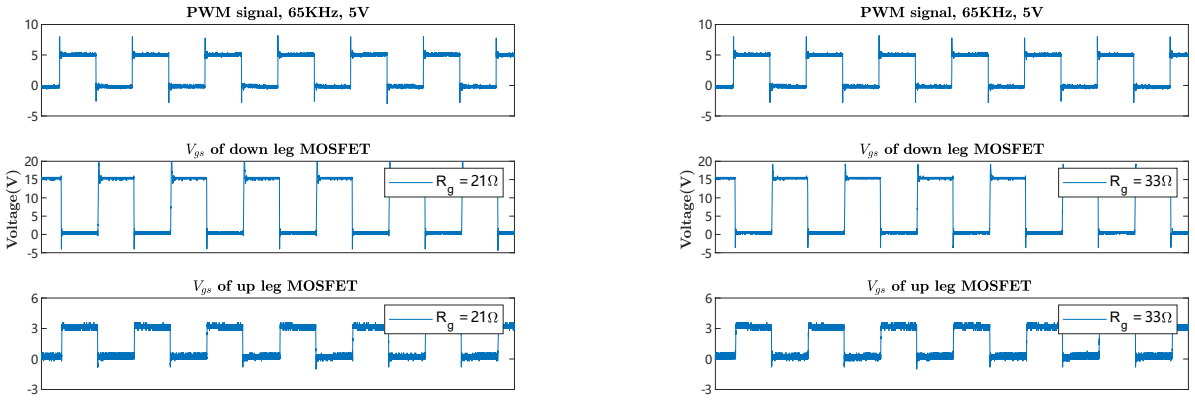
The other two tested R_{g1} value are tested for the slow switching leg and the waveforms are shown as



(a) $R_{g1} = 21\Omega$ ***(b)*** $R_{g1} = 33\Omega$

Figure D.2. Comparison of Rg1 21 and 33 ,rg2 =5 , for slow switching leg

The other two tested R_{g1} value are tested for the fast switching leg and the waveforms are shown as



(a) $R_{g1} = 21\Omega$ ***(b)*** $R_{g1} = 33\Omega$

Figure D.3. Comparison of Rg1 21 and 33 ,rg2 =5 , for slow switching leg

D.3 Current sensing circuit trace broken issue

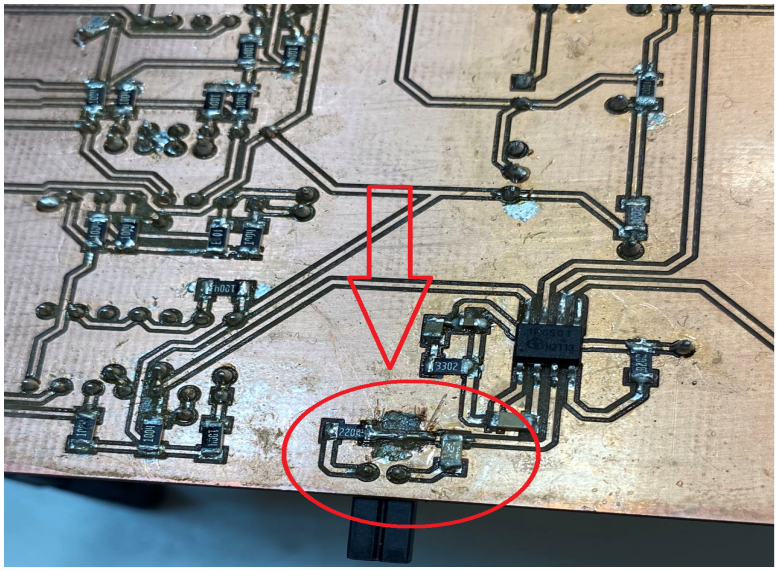


Figure D.4. Current sensing circuit trace damage condition

Appendix E

Main power board PCB files

E.1 Main power board schematic

The schematic of Main power b board implemented in Altium Designer is shown as Figure E.1.

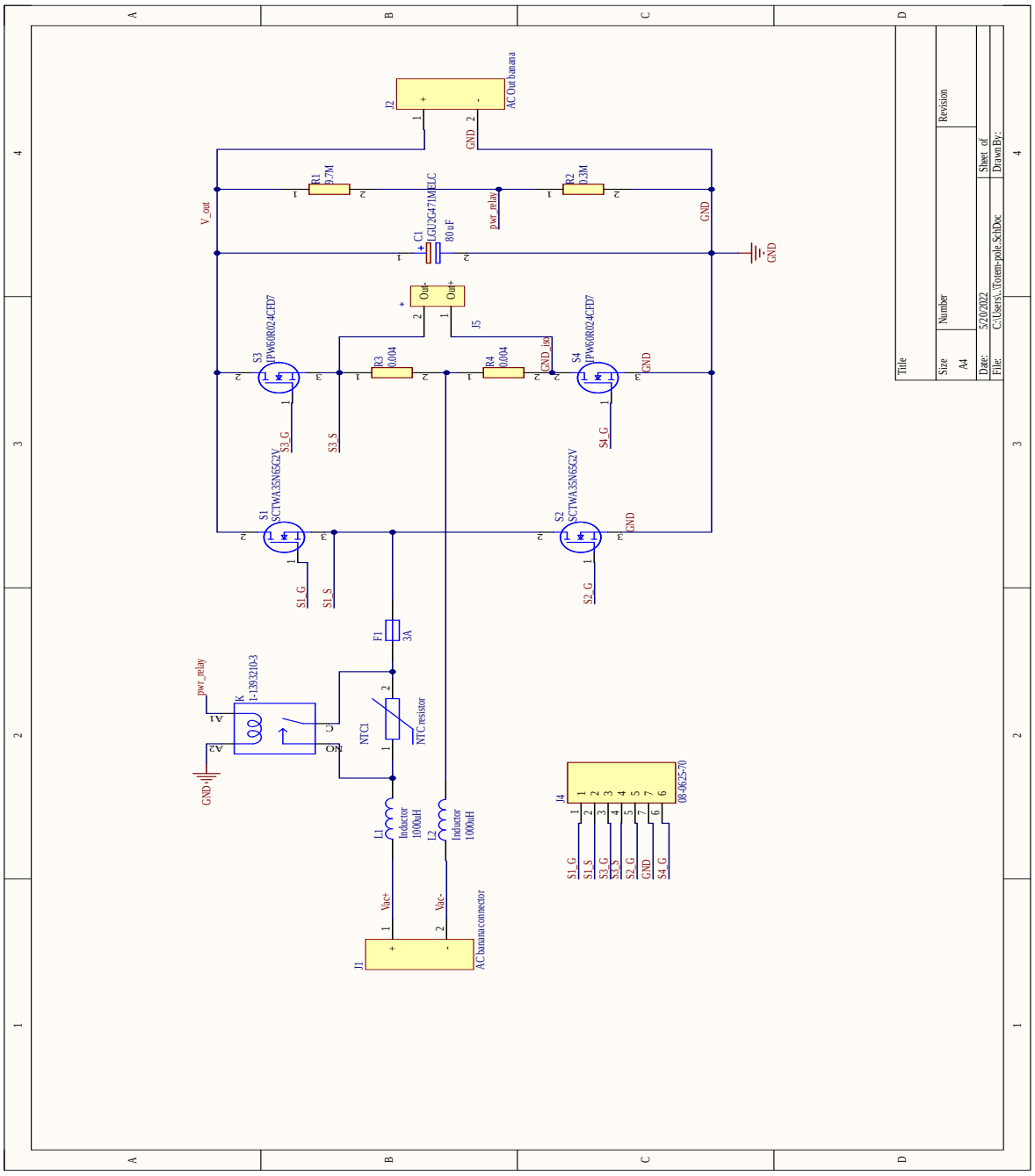


Figure E.1. Main power board schematic

E.2 Main power b board pcb layout

The PCB layout of Main power board implemented in Altium Designer is shown as Figure E.2.

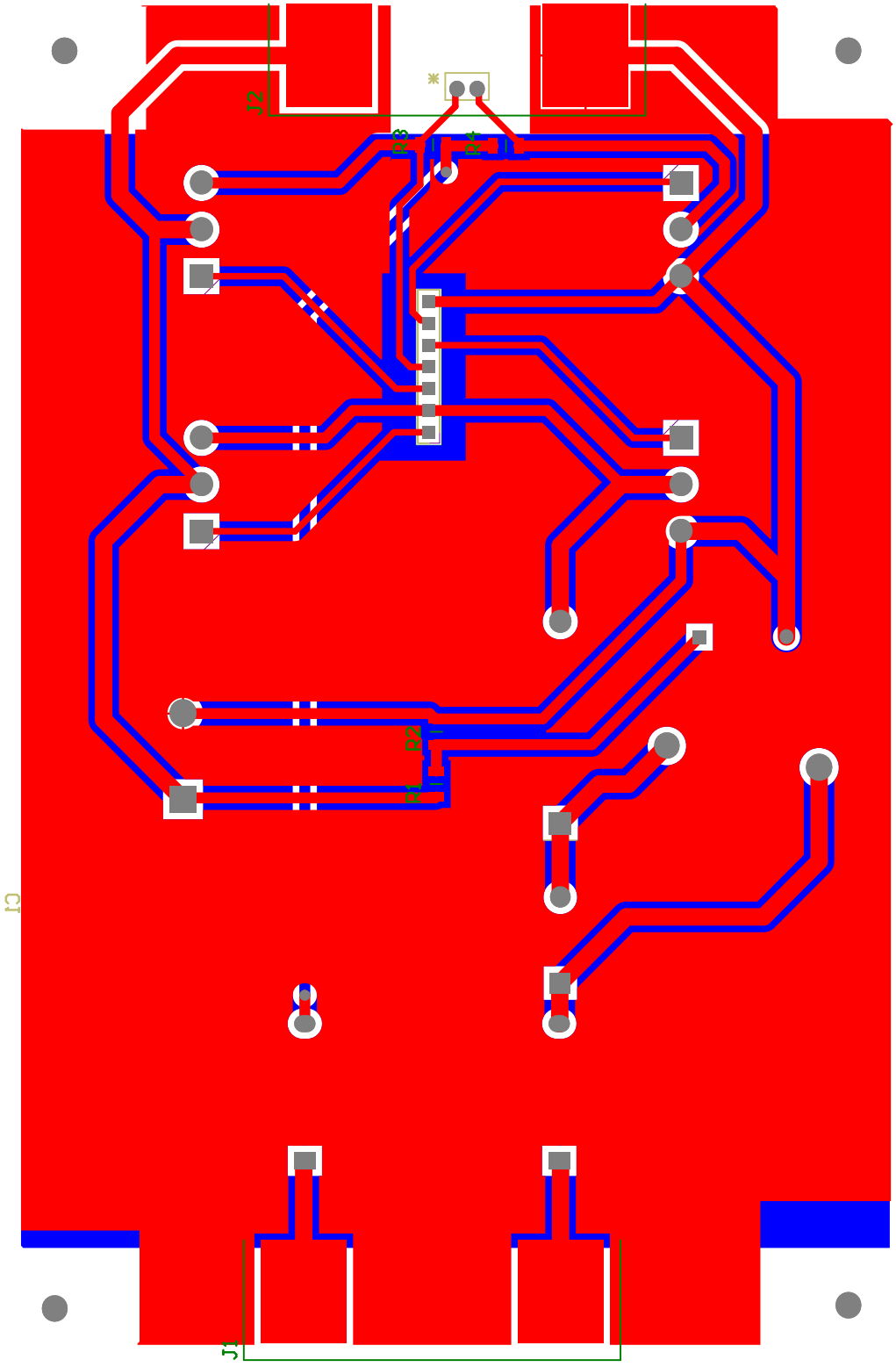


Figure E.2. Main power board pcb layout

E.3 Main power board bill of material(BOM)

The BOM of Main power b board implemented in Altium Designer is shown as Figure E.3.

Comment	Description	Designator	Footprint	LibRef	Quantity
J5			needle connector	needle connector	1
LGU2G471MELC	Capacitor Polarised	C1	CAPPRD1000W190D3575H4200	LGU2G471MELC	1
3A		F1	Fuse	Fuse 1	1
AC banana connector		J1	AC Banana connector	AC Banana connector	1
AC Out banana		J2	AC Out banana	AC Out banana	1
08-0625-70	Connector	J4	HDRV8W51P0X254_1X8_2032X254X816P	08-0625-70	1
1-1393210-3	Electromechanical Relay 12VDC 144Ohm 30A SPST-NO __ 32.51mm 27.43mm 20.4mm__ THT Industrial Relay	K	TE_1-1393210-3	1-1393210-3	1
Inductor		L1, L2	Inductor	Inductor	2
NTC resistor		NTC1	S20 NTC resistor	S20 NTC Resistor	1
9.7M	Resistor	R1	RESC3216X60N	CRCW12061M00FKEAC	1
0.3M	Resistor	R2	RESC3216X60N	CRCW12061M00FKEAC	1
0.004	Resistor	R3, R4	RESC3216X60N	CRCW12061M00FKEAC	2
SCTWA35N65G2V	MOSFET (N-Channel)	S1, S2	TO544P521X1594X2550-3P	C2M0025120D	2
IPW60R024CFD7	MOSFET (N-Channel)	S3, S4	TO544P521X1594X2550-3P	C2M0025120D	2

Figure E.3. Main power board bill of material(BOM)

E.4 Main power board PCB

The printed main power board PCB is shown as Figure E.4.

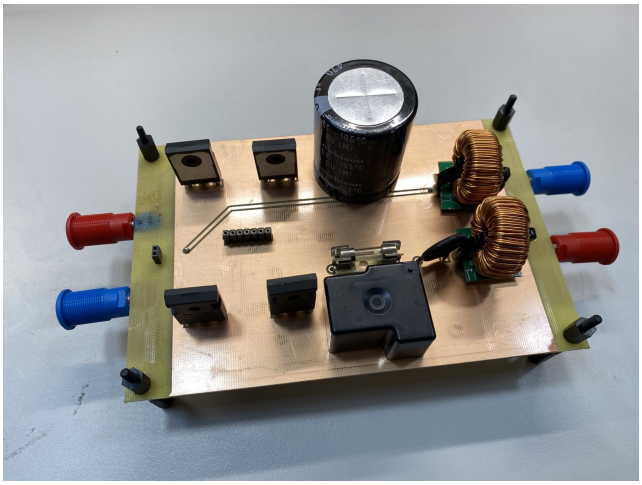


Figure E.4. Main power board PCB

Appendix F

Control board PCB files

F.1 Control board schematic

The schematic of control board implemented in Altium Designer is shown as Figure F.1.

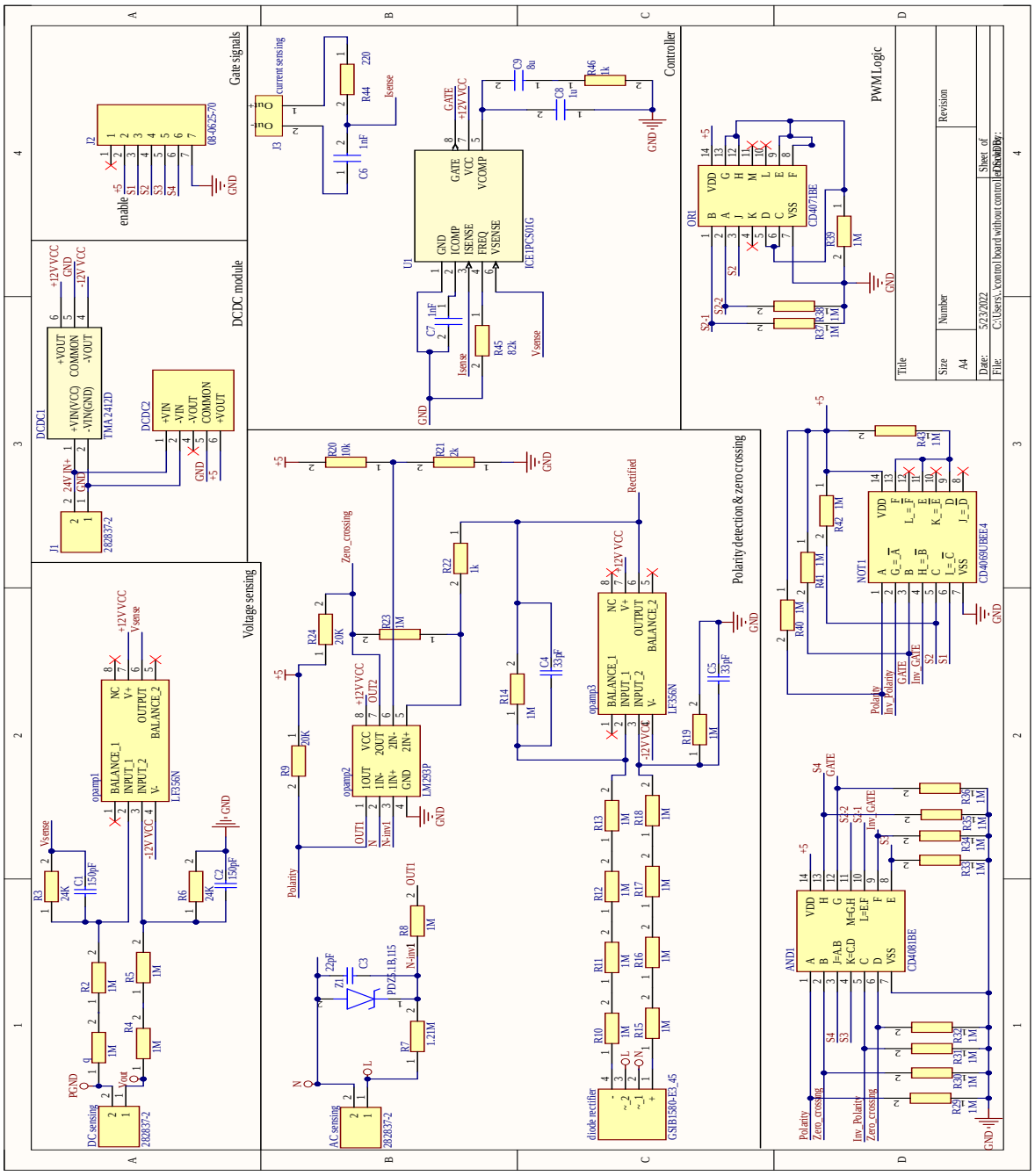


Figure F.1. Control board schematic

F.2 Control board pcb layout

The PCB layout of control board implemented in Altium Designer is shown as Figure F.2.

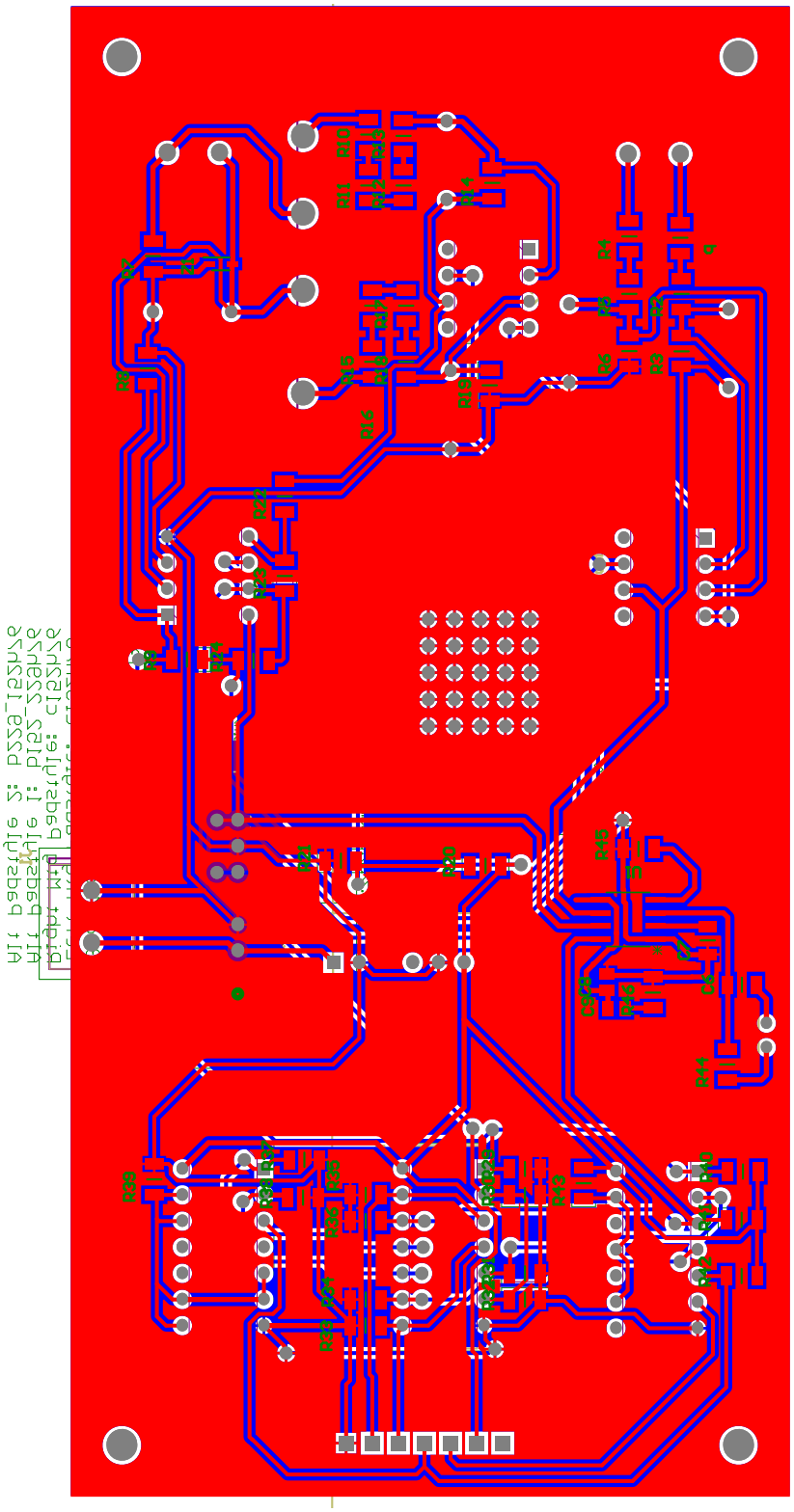


Figure F.2. Control board pcb layout

F.3 Control board pcb board overview

The overview of control board PCB implemented in Altium Designer is shown as Figure F.3 and FigureF.4.

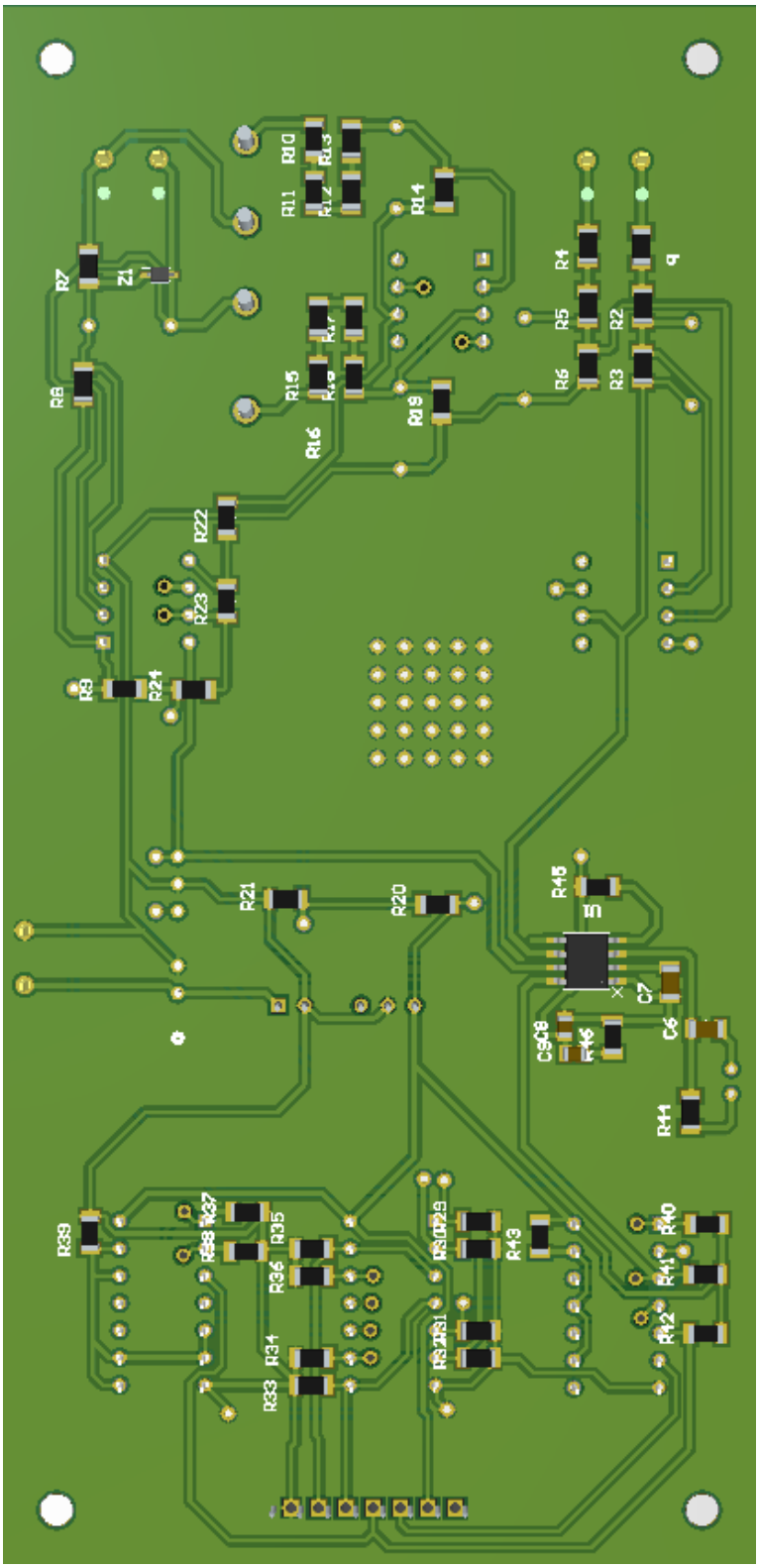


Figure F.3. Control board PCB top layer overview

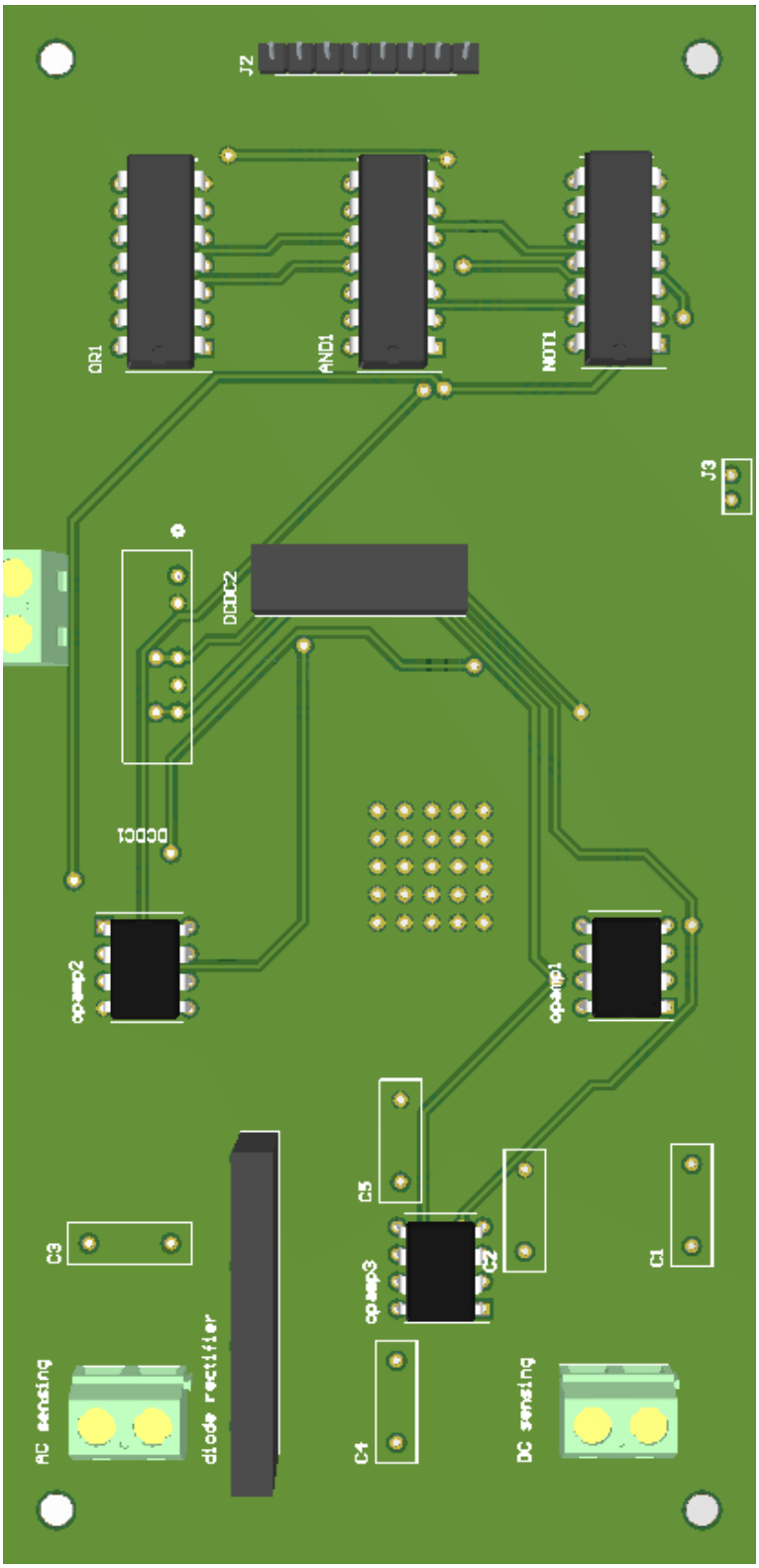


Figure F.4. Control board PCB bottom layer overview

F.4 Control board bill of material(BOM)

The BOM of control board implemented in Altium Designer is shown as Figure F.5.

Comment	Description	Designator	Footprint	LibRef	Quantity
282837-2	Connector	AC sensing, DC sensing, J1	2828372	282837-2	3
CD4081BE	Integrated Circuit	AND1	DIP794W53P254L1930H508Q14N	CD4081BE	1
150pF	Capacitor	C1, C2	RAD-0.3	Cap	2
22pF	Capacitor	C3	RAD-0.3	Cap	1
33pF	Capacitor	C4, C5	RAD-0.3	Cap	2
1nF	Capacitor	C6, C7	CAPC3216X95N	GRM3195C1H102JA01D	2
0.33u	Capacitor	C8	CAPC2012X130N	0805J0250104KXT	1
1.8u	Capacitor	C9	CAPC2012X130N	0805J0250104KXT	1
TMA 2412D	24 to 12 and -12 DCDC converter	DCDC1	24 to 12 and -12 DCDC - TMA-1W-DUAL	24 to 12 and -12 DCDC - TMA 2412D	1
	Power Supply	DCDC2	IQ2415S	IQ2415S	1
GSIB1580-E3_45	Bridge Rectifier	diode rectifier	GSIB1580E345	GSIB1580-E3_45	1
08-0625-70	Connector	J2	HDRV8W51P0X254_1X8_2032X254X816P	08-0625-70	1
current sensing		J3	needle connector	needle connector	1
CD4069UBEE4	Integrated Circuit	NOT1	DIP794W53P254L1930H508Q14N	CD4069UBEE4	1
LF356N	Integrated Circuit	opamp1, opamp3	DIP794W53P254L959H508Q8N	LF356N	2
LM293P	Integrated Circuit	opamp2	DIP794W53P254L959H508Q8N	LM293P	1
CD4071BE	Integrated Circuit	OR1	DIP794W53P254L1930H508Q14N	CD4071BE	1
1M	Resistor	q, R2, R4, R5, R8, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R23, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43	RESC3216X60N	CRCW12061M00FKEAC	31
24K	Resistor	R3, R6	RESC3216X60N	CRCW12061M00FKEAC	2
1.21M	Resistor	R7	RESC3216X60N	CRCW12061M00FKEAC	1
20K	Resistor	R9, R24	RESC3216X60N	CRCW12061M00FKEAC	2
10k	Resistor	R20	RESC3216X60N	CRCW12061M00FKEAC	1
2k	Resistor	R21	RESC3216X60N	CRCW12061M00FKEAC	1
1k	Resistor	R22	RESC3216X60N	CRCW12061M00FKEAC	1
220	Resistor	R44	RESC3216X60N	CRCW12061M00FKEAC	1
82k	Resistor	R45	RESC3216X60N	CRCW12061M00FKEAC	1
32k	Resistor	R46	RESC3216X60N	CRCW12061M00FKEAC	1
ICE1PCS01G	Controller Chip	U1	ICE1PCS01G - PG-DSO-8-1_INF-M	ICE1PCS01G	1
PDZ5.1B,115	Zener Diode	Z1	SOD2512X110N	PDZ5.1B,115	1

Figure F.5. Control board bill of material(BOM)

Appendix G

Gate driver board PCB files

G.1 Gate driver board schematic

The schematic of fast switching gate driver board implemented in Altium Designer is shown as Figure G.1.

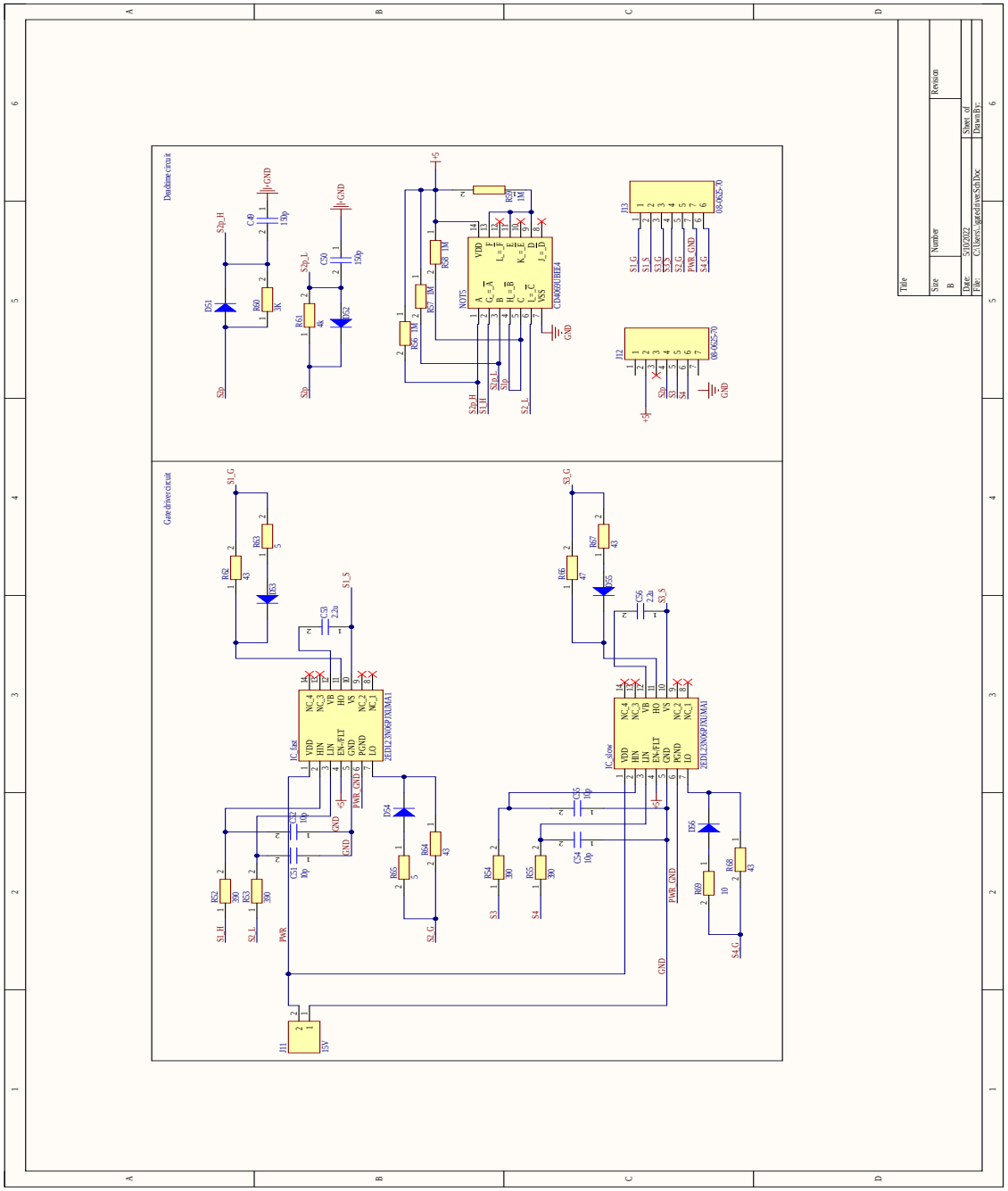


Figure G.1. Gate driver board schematic

G.2 Gate driver board pcb layout

The schematic of fast switching gate driver board implemented in Altium Designer is shown as Figure G.2.

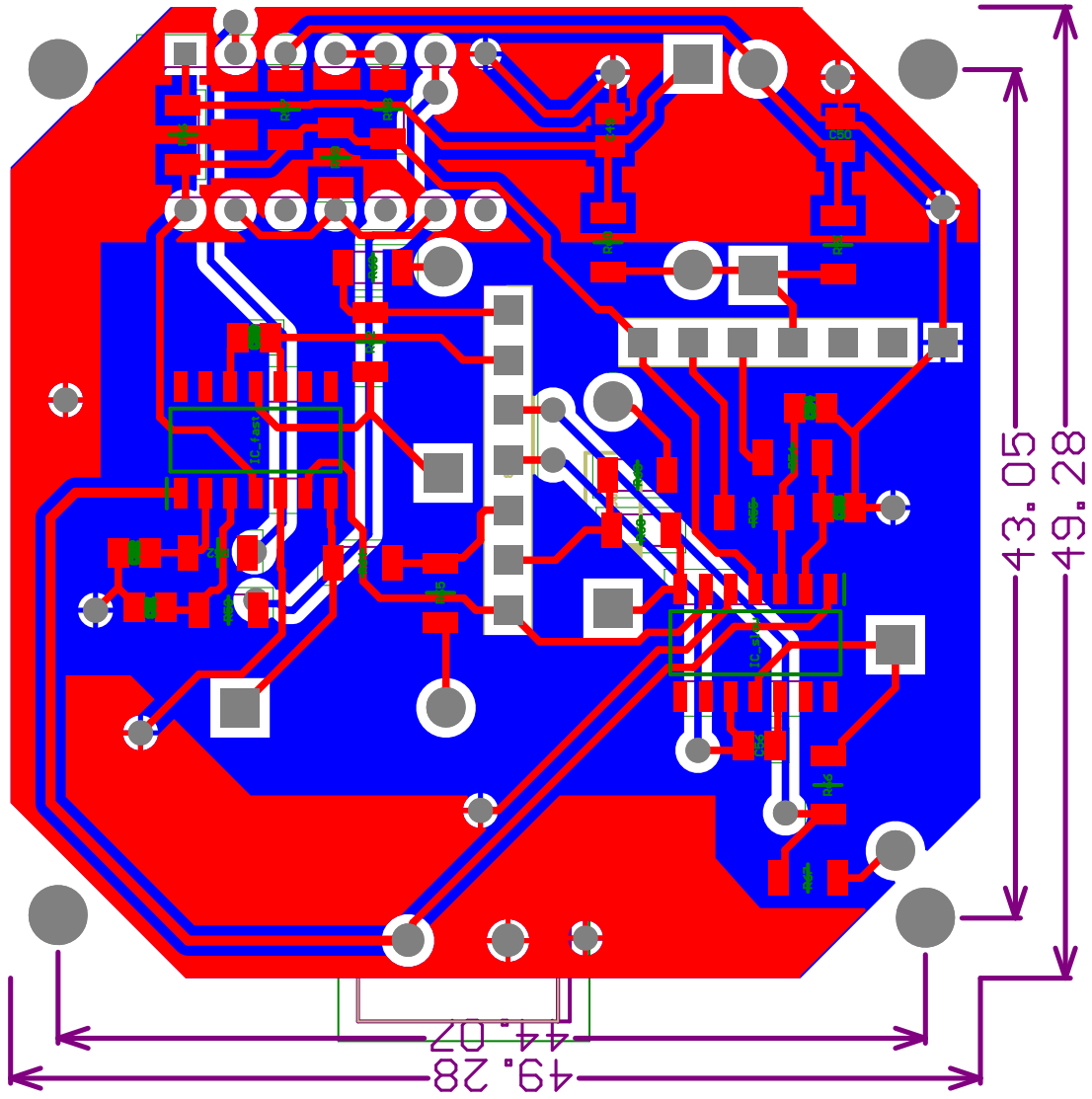


Figure G.2. Gate driver board pcb layout

G.3 Gate driver pcb board overview

The overview of gate driver PCB implemented in Altium Designer is shown as Figure G.3 and FigureG.4.

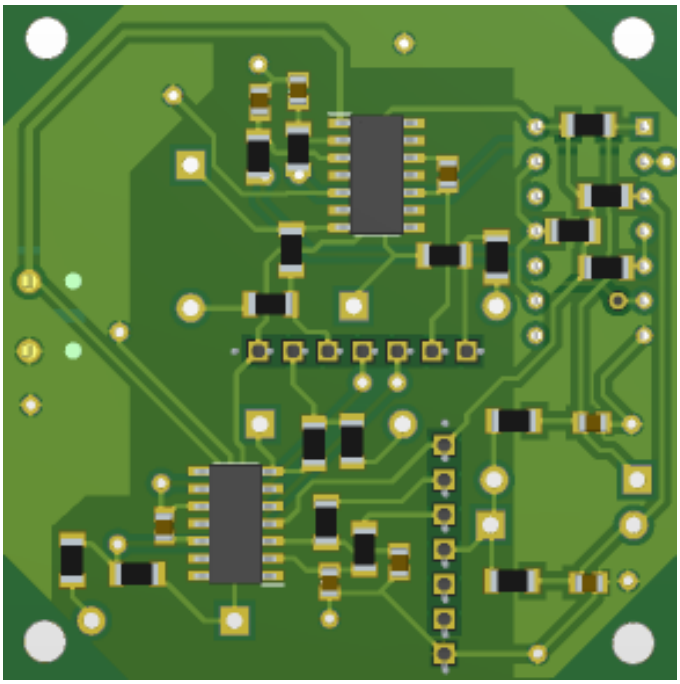


Figure G.3. Gate driver PCB top layer overview

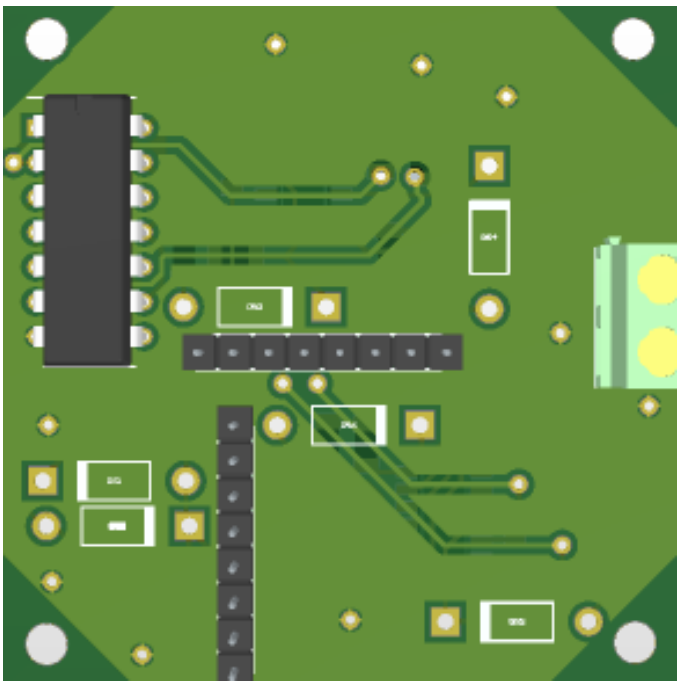


Figure G.4. Gate driver PCB top layer overview

G.4 Gate driver board bill of material(BOM)

The schematic of fast switching gate driver board implemented in Altium Designer is shown as Figure G.5.

Comment	Description	Designator	Footprint	LibRef	Quantity
150p	Capacitor	C49, C50	CAPC2012X130N	GRM2162C1H100JD47D	2
10p	Capacitor	C51, C52, C54, C55	CAPC2012X130N	GRM2162C1H100JD47D	4
2.2u	Capacitor	C53, C56	CAPC2012X130N	GRM2162C1H100JD47D	2
iode 1N4004	1 Amp General Purpose Rectifier	D51, D52, D53, D54, D55, D56	DO-41	Diode 1N4004	6
2EDL23N06PJXUMA1	Integrated Circuit	IC_fast, IC_slow	SOIC127P600X175-14N	2EDL23N06PJXUMA1	2
15V	Connector	J11	2828372	282837-2	1
08-0625-70	Connector	J12, J13	HDRV8W51P0X254_1X8_2032X254X816P	08-0625-70	2
CD4069UBEE4	Integrated Circuit	NOT5	DIP794W53P254L1930H508Q14N	CD4069UBEE4	1
390	Resistor	R52, R53, R54, R55	RESC3216X60N	CRCW12061M00FKEAC	4
1M	Resistor	R56, R57, R58, R59	RESC3216X60N	CRCW12061M00FKEAC	4
3K	Resistor	R60	RESC3216X60N	CRCW12061M00FKEAC	1
4k	Resistor	R61	RESC3216X60N	CRCW12061M00FKEAC	1
43	Resistor	R62, R64, R67, R68	RESC3216X60N	CRCW12061M00FKEAC	4
5	Resistor	R63, R65	RESC3216X60N	CRCW12061M00FKEAC	2
47	Resistor	R66	RESC3216X60N	CRCW12061M00FKEAC	1
10	Resistor	R69	RESC3216X60N	CRCW12061M00FKEAC	1

Figure G.5. Gate driver board bill of material(BOM)