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Current Control and Loss Estimation in a Medium Voltage Silicon-Carbide Power Converter

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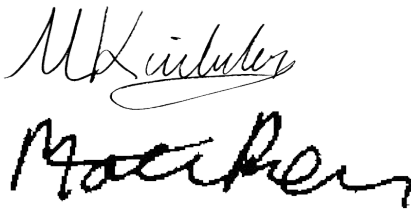

Abstract:
Attention toward wide bandgap materials has increased in the last decades as the inherent advantages of the materials' properties have been proven attractive in semiconductor devices used in power electronic systems. The goal of this thesis is to demonstrate closed loop current control in a 10 kV Silicon-Carbide MOSFET based half-bridge power converter. To mitigate the impact of switching noise on the current feedback signal, the sampling scheme proposed in [1], [2] has been implemented and tested with success. A single phase Proportional-Resonant current controller has been designed and implemented in a DSP control board, which is embedded into a single phase back-to-back experimental setup. The controller includes a dead time compensation algorithm based on a linear approximation made from measured values of the actual dead time voltage error present during the switching transients for various levels of load current. The successful implementation of the current controller has enabled the use of the experimental setup as a test platform that can be used to evaluate the performance of the power modules with regard to their losses and MOSFET die temperatures during operation. This has been experimentally tested for various loading points in terms of DC-link voltage, load current, and switching frequency. The results from the experimental tests have been compared to expected values, which have been derived from the conduction losses calculated from the on-state resistance, and the switching losses based on a double pulse test performed in [3].

Summary

Attention toward wide bandgap materials has increased in the last decades as the inherent advantages of the materials' properties have been proven attractive in semiconductor devices used in power electronic systems. Semiconductor devices based on the Silicon-Carbide technology present higher breakdown voltage, which allows for power converter topologies to enter the medium voltage power electronics applications without the need for series connecting or cascading the semiconductor devices.

Aalborg University, Department of Energy, is heavily enrolled in research activities targeting this specific area. One of such activities is the MVOLT project that seeks to develop a scalable medium voltage power module based on 10 kV Silicon-Carbide MOSFETs that complies with industry standards.

So far, the conducted activities at the department have been primarily focused on the hardware development of the power modules, the gate drivers, and the filter inductors. However, for the successful integration of these components at a system level, it is necessary to consider the practical challenges associated with converter control as well.

Therefore, the goal of this thesis is to demonstrate the operation of a closed loop current controller applicable to the medium voltage power converters developed in the department.

A particular concern has been that of ensuring the integrity of the feedback signal provided from the current sensor, when subject to the extremely high $\mathrm{d}v/\mathrm{d}t$ caused by the fast switching speeds of the Silicon-Carbide MOSFET devices. The impact of the noise in an off-the-shelf closed loop hall-effect current sensor was identified and analyzed in [1], [2] and a sampling scheme was proposed to circumvent the issue. In this thesis, the sampling scheme has been experimentally validated and has been proven to effectively mitigate the switching noise in the sampled currents.

A single phase Proportional-Resonant current controller has been designed and implemented in a DSP control board, which is embedded into a single phase back-to-back experimental setup comprising two 10 kV Silicon-Carbide MOSFET based half-bridge power modules.
The controller includes a dead time compensation algorithm that takes into account the voltage transient during the turn-on and turn-off switching events of the MOSFETs. The algorithm is based on a linear approximation made from measured values of the actual dead time voltage error present during the switching transients for various levels of load current.

The successful implementation of the current controller has enabled the use of the experimental setup as a test platform that can be used to evaluate the performance of the power modules with regard to their losses and MOSFET die temperatures during operation.
The power module losses have been derived from electrical measurements of input power supplied to the DC-link of the back-to-back test setup as well as from calorimetric measurements of the water cooling system of the power stack in which the modules are embedded.
This has been experimentally tested for various loading points in terms of DC-link voltage, load current, and switching frequency. The results from the experimental tests have been compared to expected values, which have been derived from the conduction losses calculated from the on-state resistance, and the switching losses based on the double pulse test from [3].

Preface

This document contains a Master of Science Thesis within the specialization programme in Power Electronics and Drives written at Aalborg University department of Energy in the spring semester of 2022. The thesis is conducted in the time period from February through May 2022 accounting for a workload of 30 ECTS points for each participating student. The thesis is therefore officially a short thesis and should be considered as such, within the rules and regulations governing submission of written work.

However, it is worth noting that the work done in this thesis is a continuation of the work done in an ordinary 9^{th} semester's project conducted in the autumn semester of 2021 by the same students as undersigned in this thesis. A separate section in the introduction contains a short summary of the work done in the previous semester project and the key findings are highlighted. Previous work will be cited throughout this thesis as references [1] and/or [2].

Acknowledgements

Authors would like to express their gratitude to their supervisors on the final two semesters for their guidance and support.

To Prof. Stig Munk-Nielsen for his continuous encouragement and support, for always believing in us, and for trusting us with responsibility and opportunities before, during, and after the thesis work.

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To Dr. Dipen Narendra Dalal for his unwavering support, his will and ability to pass on his expert knowledge in a down-to-earth manner, and for spending countless hours with us engaged in conversation, discussions, and laboratory work.

List of Abbreviations

Abbreviation:	Description:
AAU	Aalborg University
ADC	Analog-To-Digital Converter
B2B	Back-To-Back
CCS	Code Composer Studio
CPLD	Complex Programmable Logic Device
DAC	Digital-To-Analog Converter
DCL	Digital Control Library
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
ENOB	Effective Number Of Bits
FFT	Fast Fourier Transform
FMEA	Failure Modes and Effects Analysis
GPIO	General Purpose Input/Output
HS	High-Side
IGBT	Insulated-Gate Bipolar Transistor
JBS	Junction Barrier Schottky
LS	Low-Side
LSB	Least-Significant Bit
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor

Abbreviation:	Description:
MV	Medium Voltage
PI	Proportional-Integral
PIF	Peripheral Interface
PR	Proportional-Resonant
PWM	Pulse-Width Modulation
P2X	Power-To-X
RES	Renewable Energy Sources
Si	Silicon
SiC	Silicon Carbide
SM	State Machine
SNR	Signal-To-Noise Ratio
SPI	Serial Peripheral Interface
TR	Transmitter/Receiver
UPS	Uninterruptible Power Supply
WBG	Wide Bandgap

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Chapter 1

Introduction

Attention toward wide bandgap (WBG) materials has increased in the last decades as the inherent advantages of the materials' properties such as larger bandgap, electrical breakdown field, and thermal conductivity have been proven attractive in semiconductor devices used in power electronic systems [4]. Semiconductor devices based on the Silicon-Carbide (SiC) technology present higher breakdown voltage, lower switching- and conduction losses, faster switching speeds, and increased operating temperature compared to the conventional Silicon (Si) technology [5], [6]. These advantages have been known for many more years, however, difficulties related to their fabrication processes have hindered their applicability until recently [4].

The higher blocking voltage of the emerging SiC semiconductor devices allows for power converter topologies to enter the medium voltage (MV) power electronics applications without the need for series connecting or cascading the semiconductor devices. This brings significant reductions in the complexity and component count of medium voltage converters which in turn could reduce cost and control complexity as well as improve the overall system reliability [7], [8].

The prospect of medium voltage converter technology is extensive as many present applications rely on efficient and reliable power converter technology. One of such applications is the large power transmission networks of regenerative power plants, for instance, wind turbines and photovoltaics [9], as the current system architecture and topology can be improved with the introduction of medium voltage technology. However, also new emerging applications such as Power-To-X and charging of electric vehicles are expected to benefit from the advantages of medium voltage technology [10], [11].

The motivation behind this project was inspired by the research activities currently being conducted at the Department of Energy at Aalborg University (AAU) within the field of 10 kV SiC MOSFETs utilized in medium voltage power converters. Therefore, an introduction to the background and scientific setting of this thesis within the context of the ongoing research at the department is presented in the following section.

1.1 Background and Setting Within the Context of Ongoing Research at AAU Energy

At AAU, Department of Energy, it is believed that medium voltage power converters based on emerging WBG semiconductor devices could be an enabling technology, and hence, play a key role in the further development and application of power electronic systems. Therefore, new research activities targeting the specific application of such medium voltage converters are being launched, which will utilize both the experience gained and the hardware developed in the recent extensive research carried out in the department. These activities span a wide range of engineering disciplines and technologies from digital design and multi-physics simulation tools, through manufacturing and testing of hardware prototypes, all the way to demonstrating top-level system integration of the semiconductor devices [12]–[15].

These activities are attracting immense interest and many are being carried out in collaboration with major actors in the Danish power electronics industry such as Vestas, Siemens Gamesa, KK Wind

Solutions, Danfoss, Grundfos, etc. These actors, together with the university, all share a common goal of developing the future power electronics devices and systems to become cheaper, more reliable and to improve their efficiency while reducing size and weight.

One of such activities is the MVOLT [15] project, which intends to prove that medium voltage power converters based on SiC MOSFETs can become feasible in commercialized wind turbine converters. This is to be done by developing a scalable medium voltage power module, which should comply with wind turbine requirements as well as IEC industry standards.

The MVOLT project is a continuation of the MV-BASIC project [14] and the combined experience gained from these two projects so far is placing the department and its partners in a strong position to fulfill the promise of maturing the medium voltage converter technology. Already, significant advancements have been made and many important challenges have been identified and addressed. A key design consideration present in the development of the medium voltage power modules has been to reduce the negative impacts of capacitive couplings which arise due to the fast switching speed of the SiC MOSFET devices and can lead to increased switching losses and electromagnetic interference (EMI) issues. Therefore, extensive work has gone into the reduction of parasitic capacitances in the design of the power modules, the gate driver circuitry, and the filter inductors [16]–[23].

The power modules engineered and built in the MVBASIC project are sought to be integrated into a commercially available 500 kVA, 1.7 kV IGBT based liquid cooled converter frame [24]. The rated power of 500 kVA will be achieved by equipping the converter with paralleled MOSFET multi-chip power modules which are currently being developed in the department. As a stepping stone on the way to achieve this, a series of iterations of single-chip power module prototypes have been developed for design validation, proof of concept, and gaining experience with the operation of the power modules. This has resulted in a demonstrated integration of the latest generation of the single-chip power modules in a three phase 50 kVA power stack, which has been successfully operated in an open loop configuration at 6 kV DC-link voltage and 7 A RMS current [24].

While the next generation of the power modules is being developed to achieve the rated power of 500 kVA, the present power modules constitute a test platform where valuable insights into the practical operation of the converter can be gained. So far, the conducted activities at the department have been primarily focused on the hardware development of the power modules, the gate drivers, and the filter inductors. However, for the successful integration of these components at a system level, it is necessary to consider the practical challenges associated with converter control as well.

This thesis has, therefore, been devoted to the implementation and tests of one such closed loop controller utilizing the 50 kVA test platform to identify and address the potential challenges associated herewith. As the main track of the MVOLT project is moving on with further development of the multi-chip power modules, the experimentation with the 50 kVA test platform in this thesis can be branched out entirely from the main project as no activities are directly dependent on the hardware or the results. However, the experience and results gained throughout this thesis will be directly applicable when similar activities are to be conducted on the final demonstrator setup for the MVOLT project. Therefore, the thesis work sits well within this as well as other targeted research activities at the department as illustrated in Fig. 1.1.

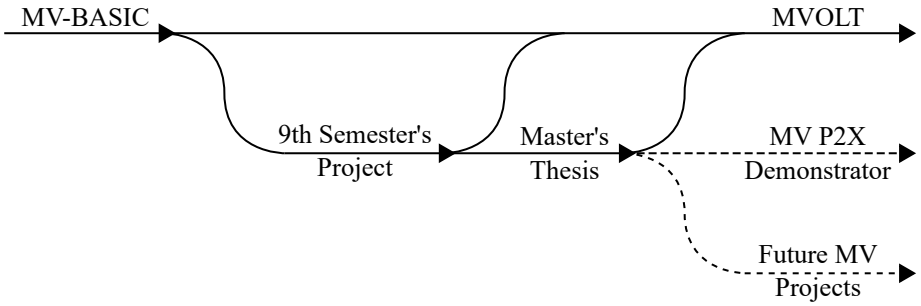


Figure 1.1: Project settings in the context of ongoing research at AAU Energy.

The process of implementing this closed loop current controller was initiated in the autumn semester of 2021 as an ordinary 9$^{\text{th}}$ semester's project. Therefore, some of the foundations for the work presented in this thesis traces back to the 9$^{\text{th}}$ semester's project. However, as stated in the preface, the work presented in this thesis is officially detached from the work done in the 9$^{\text{th}}$ semester's project and should be considered as such. Therefore, to allow the reader to clearly distinguish between the work done in the previous project and the thesis at hand, a brief introduction to the key findings from the previous semester's project will be presented in Section 1.2 and its documentation will be attached as an enclosure to accompany this thesis. These documents include a scientific paper [2] made for the annual internal Conference for Energy Students held at AAU Energy as well as a more comprehensive project report [1].

1.2 Previous Work

To present the reader with an understanding of the background of this thesis, it is necessary to give a short introduction to the key findings from the previous 9$^{\text{th}}$ semester's project [1], [2].

The 9$^{\text{th}}$ semester's project has primarily been focused on the simulation of the laboratory setup and controller design as well as practical current sensing in the medium voltage converter setup.

The first focus area was to implement a simulation model of the three phase back-to-back (B2B) demonstrator setup used in [24] as well as an equivalent single phase model, which constituted the test platforms used throughout the 9$^{\text{th}}$ semester's project. Simulation models of both setups were implemented in PLECS and could then be used to gain familiarity with the systems' behavior.

A proportional-integral (PI) current controller was designed for the three phase setup in the *dq0* reference frame by the use of an analytical pole-zero cancellation approach. The PI controller was designed to achieve a desired rise time of 3 ms. This time constant and parameterization of the PI controller was found from a compromise between controller performance and stability considering that it would have to be applied in a discrete controller with an assumed 1.5 periods sample delay at an update frequency of 5 kHz. The performance of the PI controller was evaluated in the simulation models and deemed sufficient for both the single and three phase setups as robustness was prioritized above performance.

The second focus area has been centered around practical current sensing in the medium voltage converter setup. A special concern in the 9$^{\text{th}}$ semester's project has been that of ensuring the integrity of the measurement signal when applying a current sensor in the high noise environment associated with the medium voltage converter. The extremely fast switching speeds of the SiC MOSFETs result in increased $\mathrm{d}v/\mathrm{d}t$ which raised a specific concern about the capacitive coupling between the current sensor and medium voltage conductor. An assessment of the requirements for a current sensor, when

used in a medium voltage converter, was made and a closed-loop hall effect current sensor, the LEM LA 55-P, was chosen as a candidate solution. This type of current sensor is widely used in low voltage applications, but experience with its use in medium voltage applications is limited.

After choosing this sensor type, it was desired to evaluate the amount of capacitive coupling this particular sensor type was introducing between its primary conductor and secondary measuring circuit of the sensor. The parasitic capacitance of the primary to secondary winding was experimentally determined to be 0.31 pF based on measurements of the frequency response of the secondary circuit when subjected to high frequency sinusoidal voltage inputs at its primary conductor. Based on the measured coupling capacitance, a simple equivalent circuit model was developed to model the expected noise contribution from high $\mathrm{d}v/\mathrm{d}t$ of approximately 30 kV/μs present at the primary conductor during the switching transients.

Experimental measurements of the noise during turn-on switching events of the high-side (HS) and low-side (LS) MOSFETs were made for several DC-link voltages. During these tests, it was found that the measured noise could be decomposed into two distinct components as illustrated in Fig. 1.2.

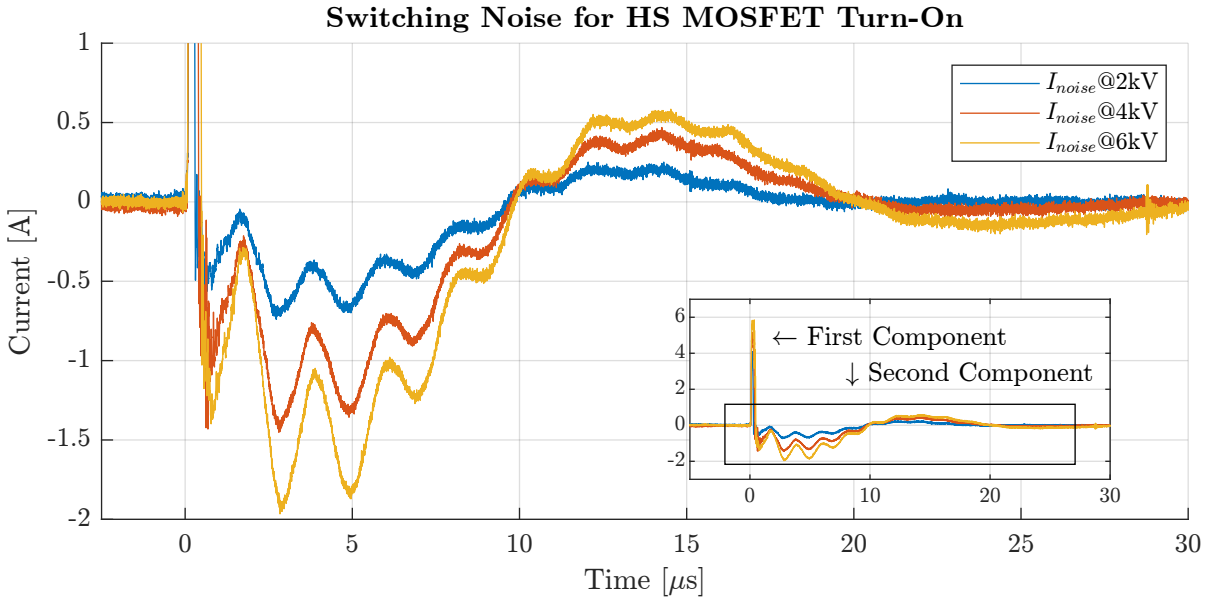


Figure 1.2: Measured switching noise currents for a turn-on switching event of the HS MOSFET [2].

The first component described the noise present during the actual switching transient of the voltage at the primary conductor. The behavior of the switching noise during this period was found to be very well represented by the developed noise model. The noise at the output terminals of the current sensor during this time interval was found to be very high in magnitude, with the noise amplitude approaching the expected output amplitude of the current sensor at the rated primary current. However, as this component of the noise was only present during the actual switching events, it was considered to pose no risk of corrupting the sampled currents in a conventional sampling scheme.

The second component defined a slower acting oscillatory noise, which was smaller in magnitude but present for a time period much longer than the actual switching event lasting for approximately 20 μs. Though smaller in magnitude, this component of the noise was found to be more critical to the integrity of the measurement signal as it would disturb the sampled currents if a conventional sampling scheme was adopted.

Finally, to circumvent this issue, an alternative sampling scheme was proposed to reduce the impact of the switching noise on the measurement integrity. However, within the time frame of the previous semester's project, it was not possible to experimentally verify the sampling scheme to prove its feasibility, and therefore, the experimental evaluation of the sampling scheme was left for future work.

1.3 Limitations

Though initially aimed at implementing the current controller in a three phase B2B experimental setup, the scope has been limited to the implementation of a single phase current controller. This limitation has been imposed due to the limited quantities of power modules available for testing.

1.4 Vision

The main vision of the thesis is to demonstrate the operation of a single phase closed loop current controller in a medium voltage power converter comprising state-of-the-art power modules enabled by 10 kV SiC MOSFETs. The motivation behind arriving at this vision is two-fold.

First and foremost, the process of implementing such a current controller is believed to provide valuable insights into the practical challenges of controlling a medium voltage converter. The experience provided through this thesis could thereby help promote the applicability of medium voltage converters and pave the way for their future integration into more complex systems.

Secondly, upon completion of this main vision, it is envisioned that the experimental setup can be used as a testing platform to evaluate the performance of the power modules at different operating points by mapping their losses and die temperatures. This could be used to validate the design specifications of the power modules and provide experimental data that could be used to (re)evaluate their designed operating point.

The successful completion of the vision relies on reconfiguring the experimental setup presented in [24] to include measurement and protection circuitry by utilizing a dedicated interface board developed in the department. This interface board features complete optical isolation between the controller and the main circuitry of the medium voltage power stack. Further, it relies on evaluating the integrity of the measurement feedback signals and ultimately the control loop stability in the high noise environment associated with the medium voltage converter which is believed to be ensured by adopting the sampling scheme proposed in [1], [2].

The vision can be summarized in the following three hypotheses:

Hypothesis 1:
It is possible to achieve closed loop current control of the medium voltage converter using standard off-the-shelf current sensors by adapting a strategic, yet simple sampling scheme to mitigate measurement noise caused by fast switching events.

Hypothesis 2:
A single phase setup can be utilized to evaluate the current controller performance and estimate the power module losses at different operating points.

Hypothesis 3:
The rated operating point of the power modules can likely be increased if the estimated losses from the measurements align with the results from the analytical loss model, and the measured die temperatures are well below their permissible limits.

Chapter 2

System Description

This chapter includes an overview of the experimental setup used in the thesis. The overview includes a brief description and photographs of the essential components of the setup.

As introduced in the previous chapter, the experimental setup has been initially limited to the single phase setup similar to the one previously used in [1], [2]. However, in this thesis, the setup is reconfigured to include the peripheral interface (PIF) card, which provides significant changes in the interfaces compared to the previous single phase setup.

This setup consists of three main building blocks, namely the medium voltage hardware setup, its control interface, and a PC. The medium voltage hardware setup consists of two DC power supplies feeding the power stack with DC+, COM, and DC-. The power stack consists of two power modules connected B2B and with their front ends connected through a set of filter inductors. The control interface includes the digital signal processor (DSP) and PIF card to control and protect the power modules. The PC is located outside of the high voltage testing cage, being connected to the DSP and DC power supplies through a galvanic isolated USB and optic Ethernet interface. Additional equipment such as measuring equipment and low voltage power supplies are left out for simplicity. A schematic overview of the single phase setup is shown in Fig. 2.1.

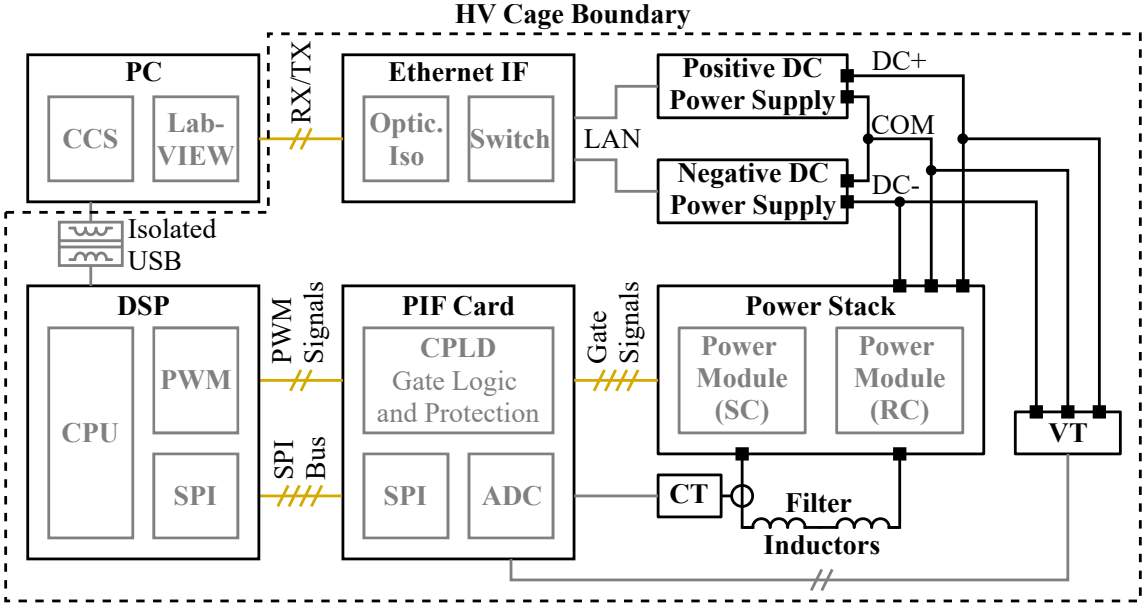


Figure 2.1: Schematic overview of the single phase setup.

Further, a photograph of the single phase setup is shown in Fig. 2.2.

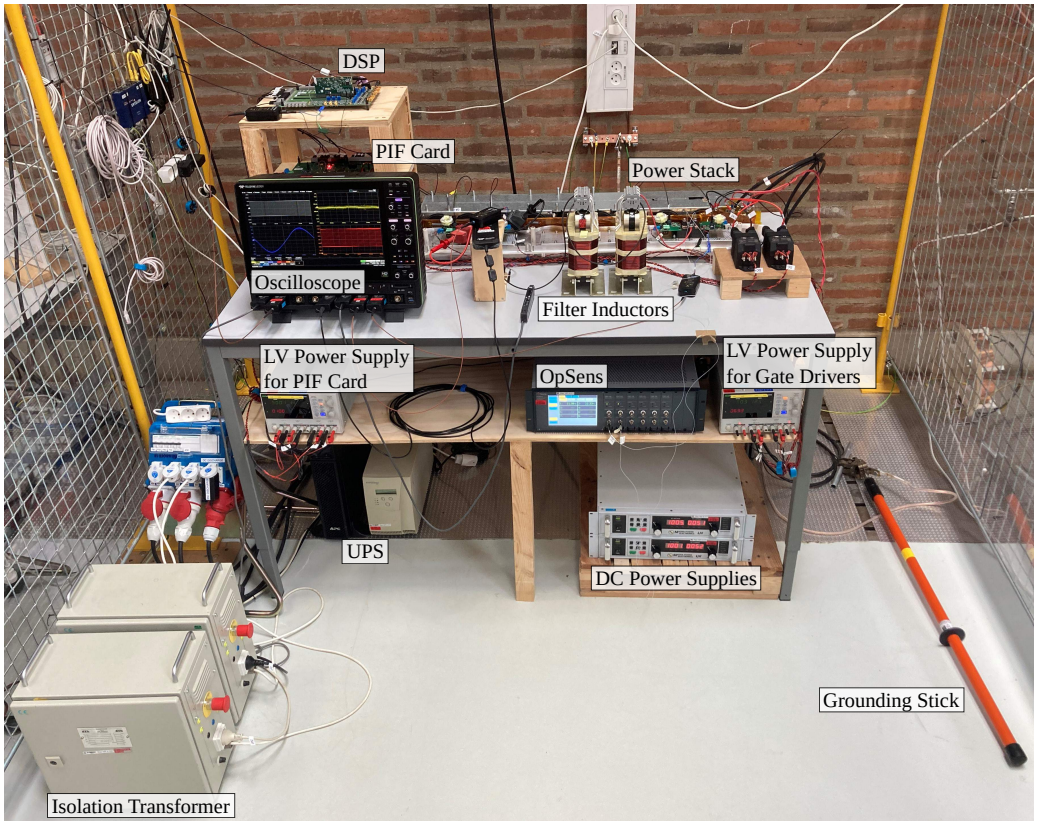


Figure 2.2: Photograph of the single phase setup.

To be able to distinguish between the two power modules in the discussions throughout this thesis they are named the sending and receiving power modules. Depending on the context, the power modules are sometimes also referred to as sending converter (SC) and receiving converter (RC). These two ways of referring to the power modules are used interchangeably. The phase angle of the load current is controlled with reference to the voltage of the power module shown to the right in Fig. 2.3. If the current is controlled to be in phase with this voltage, the right side power module will be consuming active power and is therefore named the receiving power module. In this case, the left side power module will be supplying the active power and is therefore named the sending power module.

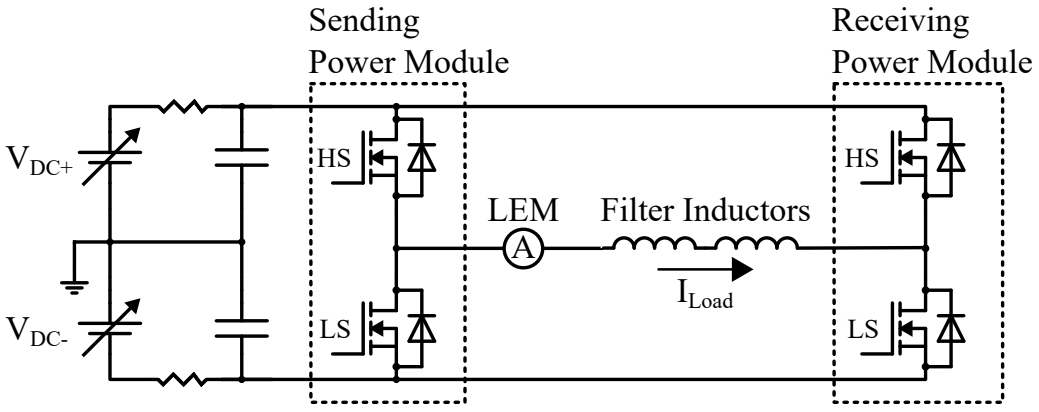


Figure 2.3: Electrical diagram of the single phase setup.

Power stack

The medium voltage power stack is a retrofit of a commercialized 500 kVA, 1.7 kV IGBT based power stack designed for PrimePACK power modules [14], [24]. The power stack consists of mounting pads for power modules, associated gate driver circuits, DC-link capacitors, DC-link busbars, and an integrated liquid cooling system. The power stack is populated with two custom packaged single-chip half-bridge 10 kV 20 A SiC MOSFET power modules manufactured in-house at AAU Energy [25]. The power modules are of the 4^{th} design generation and are populated with 3^{rd} generation 350 mΩ, 10 kV SiC MOSFET dies (CPM3-10000-0350) and JBS diode dies from Wolfspeed [24].

The power modules are rated for continuous operation at a 6 kV DC-link voltage and a load current of 7 A RMS [24] to achieve a total apparent power of approx. 15 kVA as calculated in (2.1) for a sinusoidal PWM without third harmonic injection at a modulation index of unity.

$$S = \frac{V_{DC}}{2 \cdot \sqrt{2}} \cdot m_a \cdot I = \frac{6 \text{ kV}}{2 \cdot \sqrt{2}} \cdot 7 \text{ A}_{\text{RMS}} \approx 15 \text{ kVA} \tag{2.1}$$

where V_{DC} is the full DC-link voltage, m_a is the modulation index, and I is the RMS output current of the power module.

A photograph of a power module and its gate drivers mounted in the power stack is shown in Fig. 2.4.

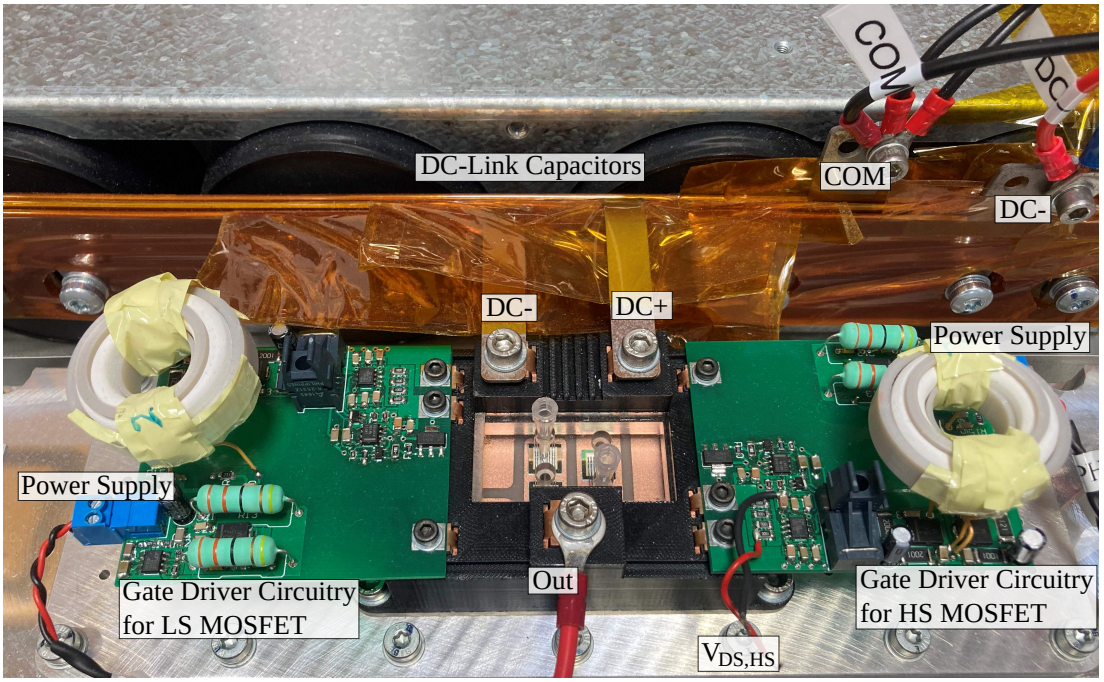


Figure 2.4: Photograph of one of the power modules and its gate drivers.

DC power supplies

The DC power supplies are from the Magna-Power XR series rated at 6 kV and 1 A [26]. A series connection of the DC power supplies is used to achieve a bipolar configuration with a grounded common point. The DC power supplies are controlled remotely through an optic Ethernet connection from the PC in which a LabVIEW interface has been programmed by AAU Energy.

Filter inductors

The filter inductors comprise two series connected single phase medium voltage inductors each having an inductance of 30 mH [27] and a low capacitive coupling of 50 pF terminal to terminal [28]. A photograph of one of the filter inductors is shown in Fig. 2.5.

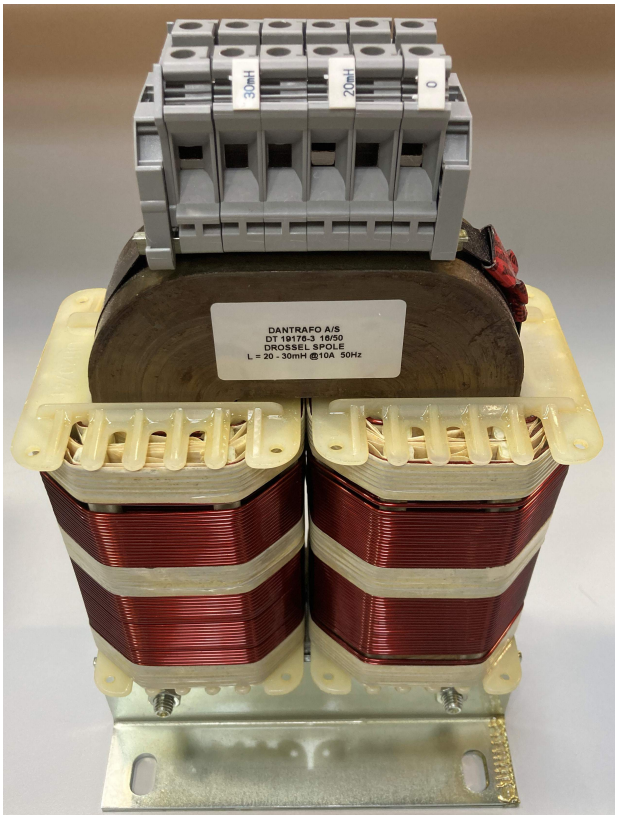


Figure 2.5: Photograph of a filter inductor.

PIF card

The PIF card is designed at AAU Energy by Dipen Narendra Dalal with the purpose of integrating it into the control interface of the new 500 kVA demonstrator setup. The main functionality of the PIF card is to provide hardware protection, electrical isolation, sampling of measurements, and serial communication to the DSP through a serial peripheral interface (SPI) bus. The PIF card is equipped with a complex programmable logic device (CPLD) in which a state machine is implemented to provide the needed functionality. A photograph of the populated PIF card is shown in Fig. 2.6.

DSP

The DSP card used is a TMDSCNCD28379D from Texas Instruments [29] placed in a DSP interface board designed at AAU Energy. The DSP interface board provides optic connectors for PWM signals and SPI communication, GPIO pins for control/triggering of scopes, and SMA connectors for debugging purposes through the DACs. The DSP card is interfaced and programmed remotely through a galvanic isolated USB connection to the PC from which Code Composer Studio (CCS) 11.1.0 is used. A photograph of the DSP interface board is shown in Fig. 2.7.

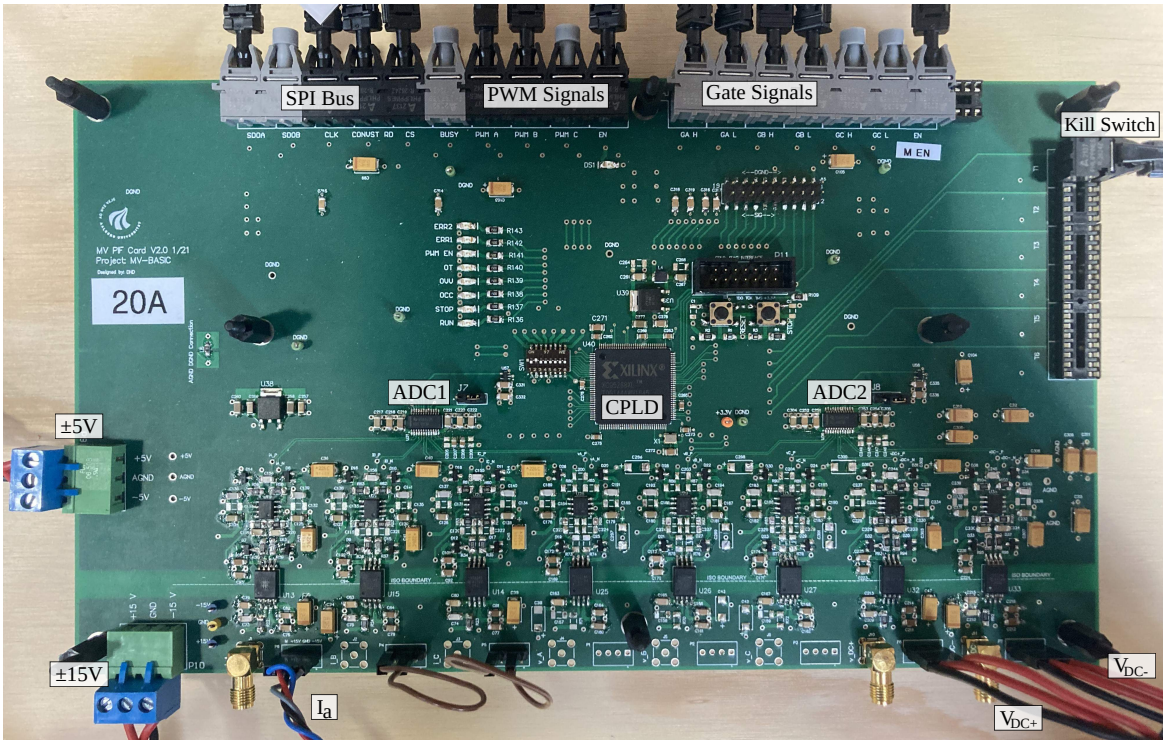


Figure 2.6: Photograph of the PIF card.

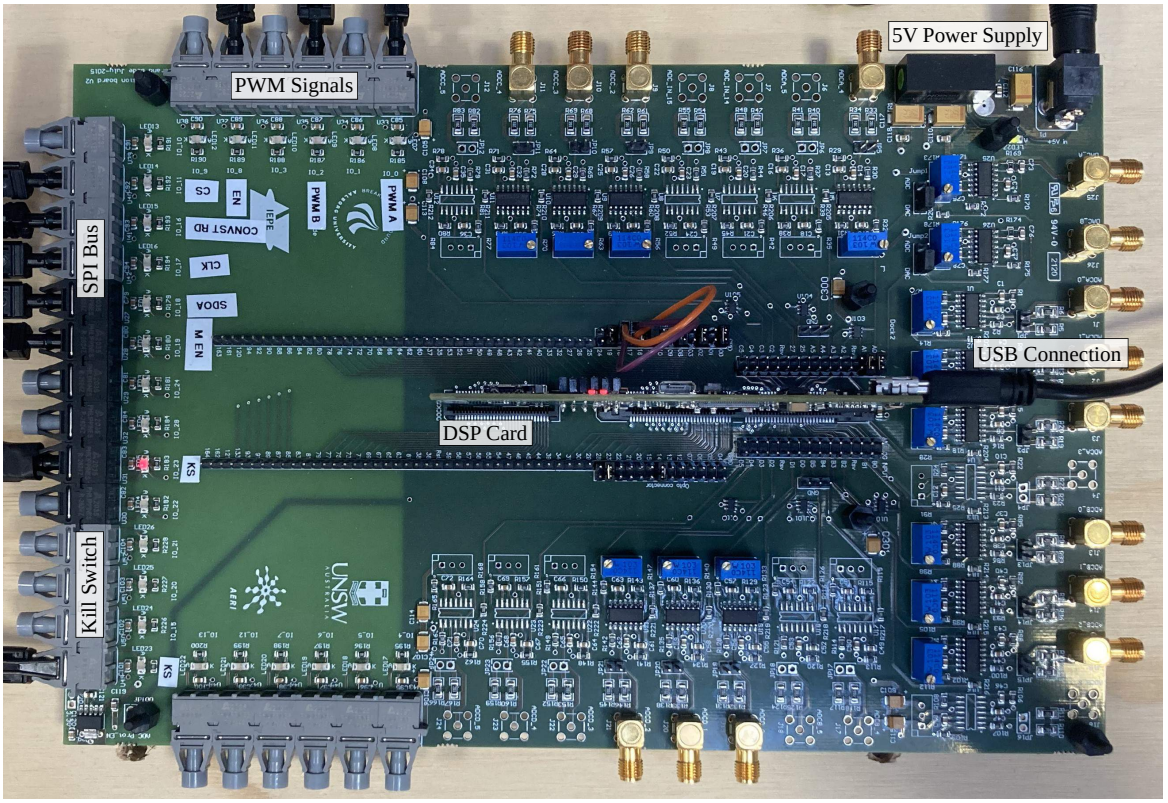


Figure 2.7: Photograph of the DSP interface board and DSP card.

Measuring equipment

The equipment used for reference measurements of voltage, current, and temperature is commercially available equipment from LeCroy and OpSens.

A LeCroy WaveRunner 8058HD Oscilloscope (8 Channel High Definition) [30] is used to measure:

- Gate signals: LeCroy HVFO103-x20 (High Voltage Fiber Optically-Isolated Probe) [31]
- Trigger signal: LeCroy HVFO103-x40 (High Voltage Fiber Optically-Isolated Probe) [31]
- Output voltage: LeCroy HVD3605A (High Voltage Differential Probe) [32]
- Load current: LeCroy CP030 (High Frequency Current Probe) [33]
- Common mode current: LeCroy CP030 (High Frequency Current Probe) [33]

An OpSens ProSens with PSR-100 modules [34] and two OTG-F optical temperature sensors [35] are used to measure the die temperature of the MOSFETs. Further, a measuring unit from Kamstrup with integrated flow rate and temperature sensors [36] is used to measure the flow rate and inlet/outlet temperatures of the water cooling system.

For the feedback signals used in the control loop, the following equipment is used:

- DC-link voltage: LEM DVM 4000 (Galvanic Separated Voltage Sensor) [37]
- Load current: LEM LA 55-P (Closed Loop Hall-Effect Current Sensor) [38]

Chapter 3

Project Planning and Risk Identification

This chapter includes a description of how the project work conducted in this thesis has been planned and executed. The chapter begins by describing how the thesis was initially divided into four distinct phases with specifically assigned milestones. This is followed by a risk identification specifically targeted at reducing the risk of causing damage to the power modules by defining a series of preventive measures. Finally, the chapter presents an overview of the actual resulting timeline for the conducted experiments. This is to present the reader with an understanding of the chronology of the thesis as this is not being followed in the presentation of results in subsequent chapters.

3.1 Project Planning

The thesis is conducted over four months, which leaves little time for derailment from the main objectives and emphasizes the need for a well defined project plan. In this thesis, the project work has been planned based on a milestone approach, where the project work is divided into separate phases each of which is assigned a specific milestone marking the successful finalization of each phase.

The thesis is divided into four phases of approximately one month each.
The **first phase** has the milestone of reconfiguring the experimental setup, introducing the PIF card for protection and signal conditioning, and implementing the open loop control to be able to evaluate the proposed sampling scheme from [1], [2]. The completion of this milestone will form the basis of the following phases.
The **second phase** is assigned with the milestone of implementing a single phase closed loop current controller which should provide accurate and reliable control of the current magnitude and phase.
Upon successfully achieving the second milestone with the implementation of the closed loop current controller, it will be possible to test the performance of the power modules for different operating points which constitutes the main objective of the **third phase**. Getting detailed performance metrics of the power modules will provide a useful benchmark of the power modules against their design specifications which could potentially pave the way for reevaluating and increasing the rating of the power modules.
The final **fourth phase** of the thesis concludes the project work by writing the thesis. An overview of the project phases and corresponding tasks are summarized in tabular form in Table 3.1.

The project phases can further be divided into specific and time limited tasks using time management tools such as Gantt chart, task lists, SCRUM, etc. depending on the desired level of project planning. However, as the group only consists of two group members, and the problem statement has been clear from the beginning of the thesis, it was decided to keep the project planning simple. Therefore, at the beginning of each phase, the main tasks have been identified as presented in Table 3.1.

Table 3.1: Overview and description of project phases.

Phase 1	7th February to 20th March	The first phase contains the initial thesis work. The tasks assigned to this phase are mostly carried over from last semester's project [1], [2], but also include reconfiguring the experimental setup to facilitate its future operation in closed loop control. The phase consists of the following tasks: • Problem identification, formulation, and project planning • Reconfiguring the setup and purchasing equipment • Interfacing of DSP, PIF card, and power modules • Implementation of open loop control • Evaluation of proposed sampling scheme
Phase 2	21st March to 18th April	The second phase contains exclusively laboratory work with the two main tasks being: • Implementation and test of closed loop current control • Development of a suitable dead time compensation algorithm
Phase 3	19th April to 20th May	The third phase contains the concluding laboratory work. This includes: • Testing of power modules at different operating points • Identification of uncertainties in measuring equipment • Estimation of power stack losses derived from electrical and water cooling measurements
Phase 4	21st May to 30th May	The fourth phase contains the final project work which includes the tasks of: • Rounding off any unfinished tasks from the previous phases • Finalizing thesis writing and documentation

3.2 Risk Identification and Planning of Experiments

As the experimental work has been carried out on a custom build prototype comprising state-of-the-art power modules manufactured in-house in very limited quantities, risk reduction has been a key consideration throughout the experimental work. It was of paramount importance that great care was taken not to damage the power modules as only five power modules were available and the manufacturing of replacement modules could not be achieved within the time frame of this thesis. Seen from a project perspective, damaging the power modules would be very critical since it would bring an end to the experimental testing. Therefore, a risk analysis has been made, and the conducted experiments planned accordingly, as will be further elaborated in this section.

The first step in the risk identification was to identify and group the possible risks associated with damaging the power modules to take the preventive measures needed. Therefore, a simple FMEA inspired risk identification, shown in Table 3.2, has been made for the potential failure modes which could cause damage to the power modules.

Table 3.2: Overview of risks associated with power module damage.

Risk	**Effect(s)**	**Preventive measure(s)**
Excessive die temperatures	Failure or malfunctioning of power modules	• Integrated water cooling system • Measurement and continuous monitoring of die temperatures
Faulty measurements caused by switching noise	Malfunctioning of controls and hardware protection potentially causing overcurrents Repetitive false overcurrent trips	• Measurement of noise contribution from switching transient as presented in [1], [2] • Implementation of proposed sampling scheme to reduce noise impact [1], [2]
Loss of measurement signal	Controller instability Malfunction of hardware overcurrent protection	• Software protection in DSP to detect overcurrent • Hardware protection in PIF card to detect overcurrent • Software protection from simulation of plant replica
Loss of DSP communication	Inability to disable the controller	• Careful system layout to reduce common mode noise • Optical isolation in signals from DSP to PIF card • Manual optic kill switch to disable DSP and PIF card
Destructive gate signals	Shoot-through of DC-link causing catastrophic failure	• Hardware protection and integration of dead time in PIF card

The table shows that for most of the identified causes, multiple preventive measures have been considered and implemented. Preferably, the preventive measures should have redundancy and multiple protective layers. As the power modules have previously been tested up to 6 kV [1], [24] insulation breakdown and flashovers are not considered immediate risks as long as auxiliary equipment are carefully placed with sufficient spacing to live parts of the system. Therefore, most of the considered risks are due to or will end up in overcurrent events, which should ideally be cleared by the built-in hardware overcurrent protection on the PIF card. However, in the rare case that the hardware protection should fail, the redundancy in the preventive measures could help save the system from failure.

For example, the risk *loss of measurement signal* where either the signal path for the current or DC-link voltage measurement is lost, will cause the current controller to become unstable as the controller is no longer able to measure and thereby follow its commanded reference. This would most likely cause the controller output voltage to saturate and cause an overcurrent event. In case of a lost current signal path, the situation is worsened as neither the software nor hardware overcurrent protection is capable of detecting the overcurrent. In this case, the redundancy of the protection layers is secured by having a simulated plant replica implemented in the DSP, which would be able to predict and trip on a simulated overcurrent event based on the commanded voltage output from the current controller.

3.3 Chronology and Timeline of Conducted Experiments

The experiments performed in the laboratory have been planned with the aim of reducing the risk of causing damage to the power modules by implementing the preventive measures identified above and by using the concept of module testing before subsystems are integrated into the setup. A description of the chronology of the work done in the laboratory is given in the next paragraphs with references to the chapters in which the work is presented.

The introduction of the PIF card into the experimental setup was seen as a cornerstone in the process of achieving the closed loop control as all of the interfaces between the DSP and medium voltage hardware are allocated on the PIF card. Therefore, this was taken care of first and the initial laboratory work was focused on the successful integration of the PIF card. The work has been grouped into two main activities based on functionality. One of the activities focused on the ADCs, including the selection of proper component values for the scaling and protection circuitry as well as the implementation of the serial interface utilized for data transfer. Whereas the other activity was to ensure the correct output of the gate signals of the power modules, which requires a specific enabling sequence to be sent to the PIF card and its onboard CPLD. These activities are covered in detail in Chapter 4.

Chapter 5 covers the implementation and test of the current controllers. Initially, the system was set to operate in open loop control which was used to qualify the reconfigured system setup and to evaluate the proposed sampling scheme [1], [2]. The open loop control also provides the opportunity to test some of the protective functions before applying the closed loop controller, including the simulated plant replica running on the DSP, the outputs of which can be compared to the actual currents measured during open loop operation.

After successful system operation in open loop control with a positive evaluation of the proposed sampling scheme, the work progressed into implementation and testing of the closed loop controllers. Before applying the closed loop control continuously to the hardware, a very cautious procedure is followed to eliminate some of the risks associated with possible instability when closing the loop. First, an analysis of the controller stability is performed in discrete time using the PLECS simulation model from [1]. Then, the performance of the controllers was tested using the simulated plant model on the DSP, which allowed for initial monitoring of the transient behavior of the discretized controller. Following this, the DSP was reprogrammed to limit the duration in which the closed loop control was applied to a specific number of switching cycles before disabling the outputs. The number of allowed cycles was gradually increased and the resulting current waveforms were carefully inspected before proceeding. Not until this procedure had proven the controller to be stable for numerous periods where the closed loop controllers allowed to run continuously. By following this procedure, it was achieved to run the closed loop controller at 3 kV DC-link voltage. This was defined as the initial testing plateau, as some of the auxiliary equipment, including the medium voltage DC power supplies, started to act irregularly when the voltage was increased further.

It was therefore decided to perform all of the tests at a capped DC-link voltage of 3 kV in the first iteration, which spans the work presented in Chapter 5 as well as Chapter 6. Only after completion of all desired measurements would the objective of increasing the voltage to its rated value of 6 kV be pursued. This also means that the main parts of the results sections in these two chapters are performed at a DC-link voltage of 3 kV. The results achieved at 6 kV DC-link voltage during the second iteration are added in separate sections in both chapters.

Chapter 6 covers the subsequent experiments performed after implementing the closed loop controller to evaluate the performance of the power modules at different operating points. The focus is on determining the losses in the power stack while varying relevant parameters such as voltage, current, and switching frequency. The evaluation also includes measurements of the MOSFET die temperatures during the tests.

A roadmap of the complete experimental workflow is presented in a visual representation in Fig. 3.1.

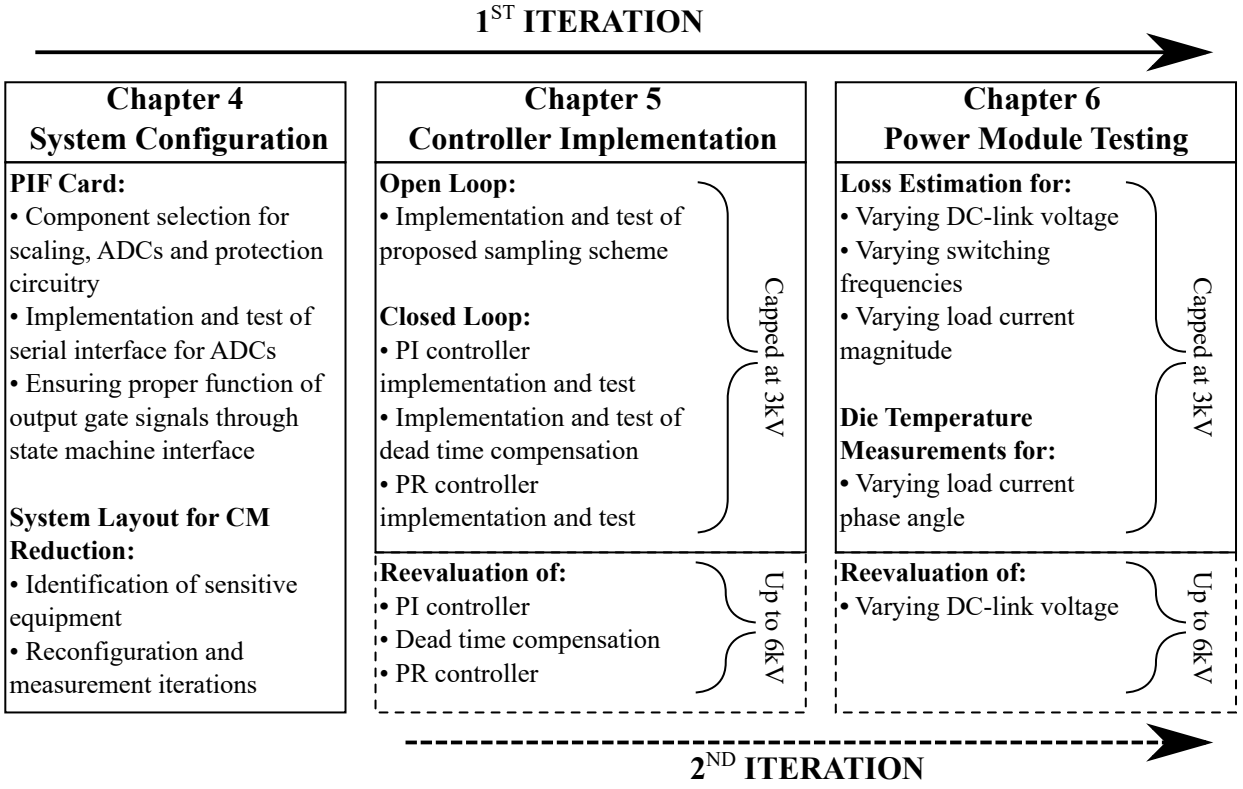


Figure 3.1: Roadmap describing the chronology of the experimental work.

Chapter 4

System Configuration and Interfacing

This chapter includes a detailed description of the system configuration and interfacing. The first two sections focus on the ADCs and the state machine on the PIF card. Simultaneously with the testing of each interface, the DSP code has been built to include the needed functionality. Refer to Appendix A for a detailed description of the digital configuration and implementation of the DSP.

Further, the last section of this chapter identifies and discusses the CM problems experienced while operating the medium voltage converter. The CM problems are caused by the capacitive couplings in the system and due to extremely high $\mathrm{d}v/\mathrm{d}t$ during the switching transients of the SiC MOSFETs. Based on the identified problems and gained experience, a top-level system configuration is proposed to increase the CM rejection of this particular experimental setup.

4.1 Configuration and Interfacing of ADCs

The PIF card contains two identical four (2+2) channel Texas Instruments ADS7863A ADCs [39]. The functional diagram of each of the ADCs is shown in Fig. 4.1. Each of the ADCs contains two separate SAR ADCs each of them having an input MUX allowing for a total of four differential input channels for each ADC.

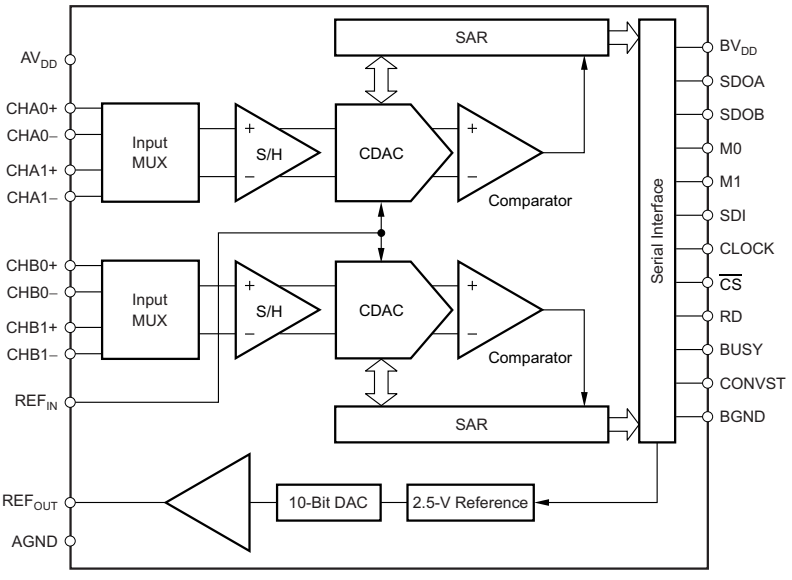


Figure 4.1: Functional diagram of the ADCs used on PIF card [39].

The ADCs used for signal acquisition are located on the PIF card and interfaced through an SPI interface using optic fibers for transmission of the digital signals to the DSP. However, not all of the I/O's from the serial interface seen in Fig. 4.1 are parsed to the DSP, as some of them are configured in the hardware on the PIF card. The six signals transmitted via the optic fibers are SDOA, SDOB, CLOCK, CS, BUSY, CONVST, and RD - the last two of which are physically tied together on the

PIF card and therefore only constitute a single signal CONVST RD. The signals M0 and M1 are configured with a jumper configuration on the PIF card which allows for manually selecting between operating modes *III* and *IV* as will be explained later in Section 4.1.2.

The CPLD multiplexes the serial communication interface from the ADCs onto a single bus between the PIF card and DSP with the use of a CS pin. This all combines to give the configuration shown in Fig. 4.2 with a total of eight ADC channels. Three are used for phase current measurements, three for phase voltage measurements, and two for DC-link voltage measurements. A detailed description of the measurement circuits including scaling, ADC bit resolution, and hardware protection is given in Appendix B.

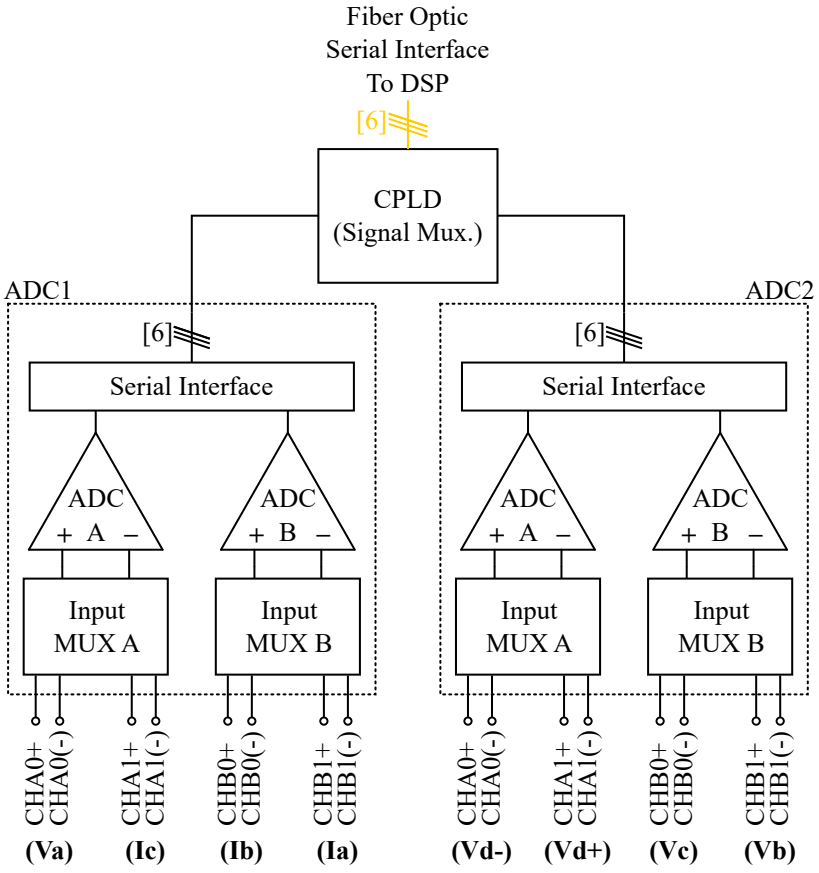


Figure 4.2: ADC configuration and interface on the PIF card.

4.1.1 Timing Requirements of ADCs

For successful interaction with the ADCs, the interface must be carefully designed to fulfill the timing requirements stated in the datasheet of the ADC [39]. The important signals and time intervals worth considering in this specific configuration of the ADCs with the CONVST and RD pins tied together are summarized in Fig. 4.3 and Table 4.1. Refer to the datasheet of the ADC for a complete description of the timings requirements [39].

The timing requirements related to the parameters t_1 through t_6 must be carefully synchronized with the clock to successfully initialize a data conversion of the ADCs. The rising edge to data valid delay, t_7, is particularly important when selecting the clocking scheme and transfer rate for the SPI interface as will be more thoroughly explained in Section 4.1.3.

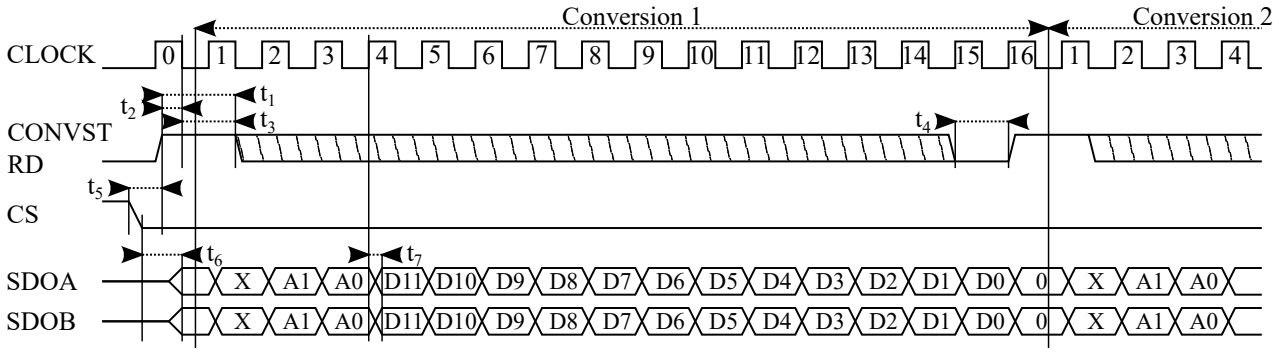


Figure 4.3: Detailed timing diagram of a conversion.

Table 4.1: Timing requirements for the SPI interface.

Parameter	Description	Min	Max	Units
t_1	CONVST RD high time	62.5		ns
t_2	RD high setup time to CLOCK falling edge	10		ns
t_3	RD high hold time to CLOCK falling edge	5		ns
t_4	CONVST low time	1		ns
t_5	CS low RD high delay	10		ns
t_6	CS low to SDOX valid	13		ns
t_7	CLOCK rising edge to data valid delay		9	ns

4.1.2 ADC Operating Modes

As previously mentioned, a jumper on the PIF card allows for manual selection between the two operating modes *III* and *IV* of the ADCs. Both of these operating modes automatically cycle between the input channels of the ADCs in the order from A0, B0, A1 to B1 before it loops back to channel A0 when B1 has been converted. In mode *III*, the data is transferred on both SDOA and SDOB as shown in Fig. 4.4, which means that sampled data from all four channels can be acquired upon sending two read pulses only.

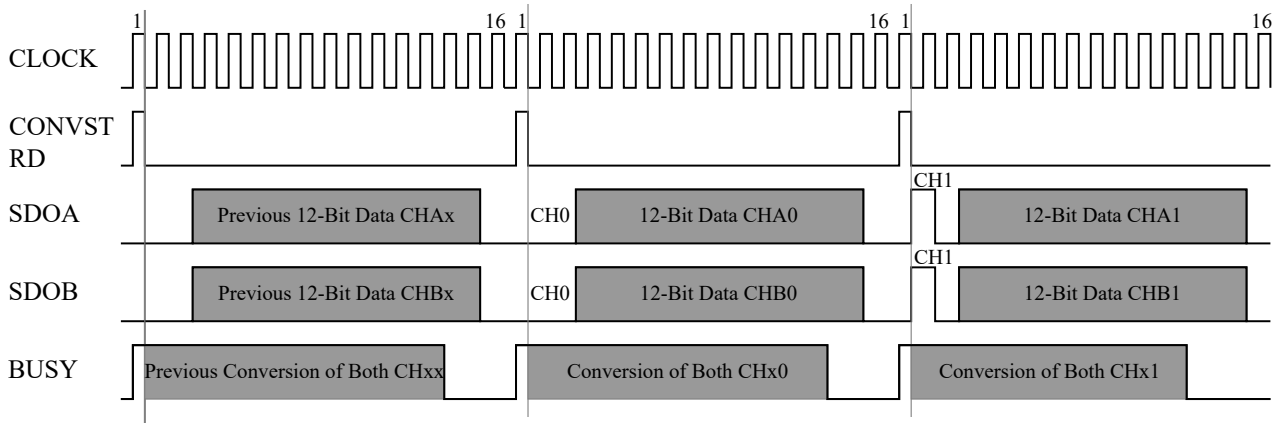


Figure 4.4: Timing diagram for mode *III*.

In mode *IV* all data is being transferred on SDOA only as shown in Fig. 4.5. This provides some simplifications in the practical implementation of the interface, as the SPI modules on the DSP only support one data bus for master in communication. Therefore this is the operating mode which has been chosen for implementation in the DSP. However, the simplification comes with the cost of slowing down the transfer rate by a factor of two.

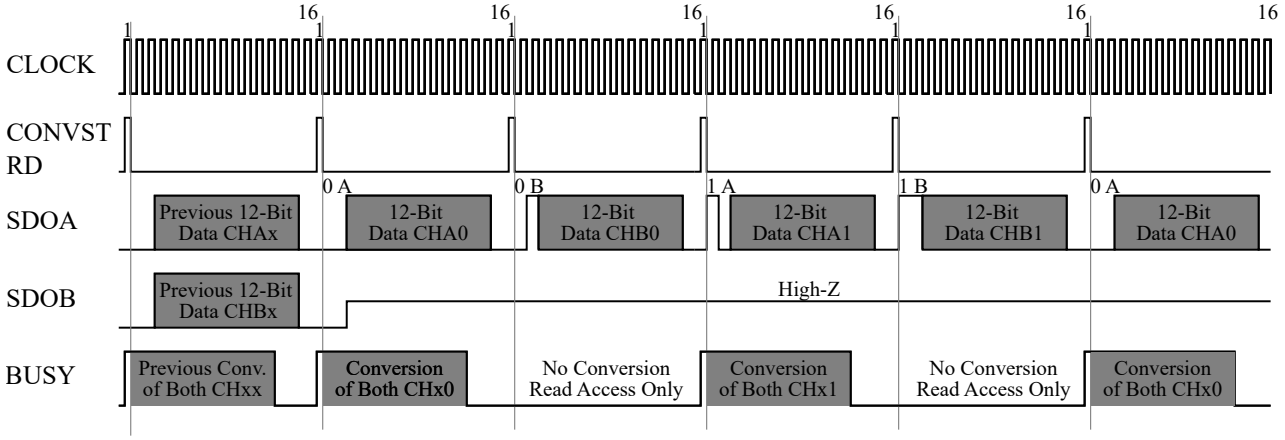


Figure 4.5: Timing diagram for mode *IV*.

Hardware configuration to support operating mode *III* and *IV*

The necessary hardware configuration of the signal interface between the DSP and PIF card to support the two operating modes of the ADCs is illustrated in Fig. 4.6. Here, the signals and components marked in black represent the needed hardware configuration when using mode *IV*, while the signals and components marked in grey represent the additional hardware needed to operate in mode *III*.

The second SPI module in the DSP used in mode *III* is configured as an SPI slave and receives its clock directly from the other SPI module configured as the master, while SDOB from the ADC is fed to its MOSI pin. Using this configuration means that the timing requirements for the clocking scheme will be identical for both SPI modules on the DSP, and therefore, the considerations related to the achievable SPI transfer rate covered in Section 4.1.3 hold for both.

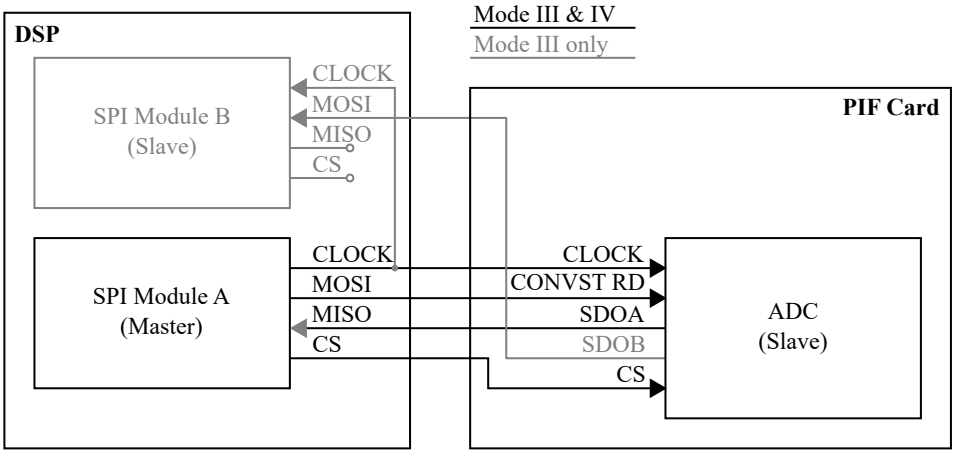


Figure 4.6: Hardware configuration to support SPI communication in mode *III* and *IV*.

4.1.3 Transfer Rate for SPI Interface

It is important to achieve reliable SPI communication between the DSP and PIF card with as high as possible transfer rate to limit the time taken to acquire and transfer the ADC data. It is therefore important in the design phase of the SPI interface to investigate which factors that limit the transfer rate and total transmission time of the ADC data.

One thing that needs to be considered in the design is the mode of operation of the ADCs, which was covered in Section 4.1.2. In the initial design of the SPI interface, the ADCs are configured in operation mode *IV* as this provides a simpler interface that is compatible with the standard SPI modules on the DSP. However, in case the total transfer time becomes too long for mode *IV*, the transfer rate can be increased by changing to mode *III* with the cost of added complexity in the DSP.

The DSP can be configured to have a transfer rate at some specific bit rates defined by the low speed peripheral clock (LSPCLK) of 50 MHz divided by a prescaler [40]. The prescaler register (SPIBRR) can take values between 3 and 127, and the resulting bit transfer rate is calculated as follows:

$$\text{SPI Baud Rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)} \tag{4.1}$$

Hence, the available transfer rates for the DSP are 12.5 MHz, 10 MHz, 8.34 MHz, 7.14 MHz, 6.25 MHz, etc. The ADC can be operated at a transfer rate between 1 and 32 MHz according to its datasheet [39]. At first glance, the limiting factor is therefore the DSP, which defines the maximum achievable transfer rate. With a transfer rate of 12.5 MHz, the theoretical transmission time of all 8 ADC channels using 16 clock cycles each for data transmission is found by:

$$t_{max} = \frac{1}{12.5 \text{ MHz}} \cdot 8 \cdot 16 \approx 10 \ \mu\text{s} \tag{4.2}$$

This data transmission time needs to be short enough to allow for sufficient time to run the control algorithm and update the PWM outputs within the remaining time of the switching period. For a switching frequency of 5 kHz where interrupts happens both on the ZERO and PERIOD counter compare events, the total available time between subsequent interrupts will be 100 μs. Hence the data transmission time for the samples only constitutes a fraction of the available time leaving a good margin to execute the remaining tasks.

Impact of Propagation Delay

Another important consideration in determining the achievable transfer rate is the propagation delay which is introduced by the non-ideal components in the signal path. According to the datasheet of the ADC [39], the ADC introduces a delay of a maximum of 9 ns as a computational delay from when it receives a rising edge before the data is valid as shown in Table 4.1. The optical connections are made of a optic transmitter, fiber, and receiver. From the datasheet of the optic transmitters/receivers [41], it is found that both types have a maximum propagation delay of 30 ns. The propagation delay from the optic fiber is calculated to be 5 ns pr. meter based on the speed of light and the material properties of plexiglas/PMMA [42]. This results in a maximum propagation delay of approx. 65 ns if using optic fibers of 1 meter.

The actual propagation delay has been measured for all of the SPI interface signals from which it is found that they have an equal propagation delay of approx. 30 ns each. A measurement of the propagation delay for the CONVST RD signal measured at the DSP and PIF card is shown in Fig. 4.7.

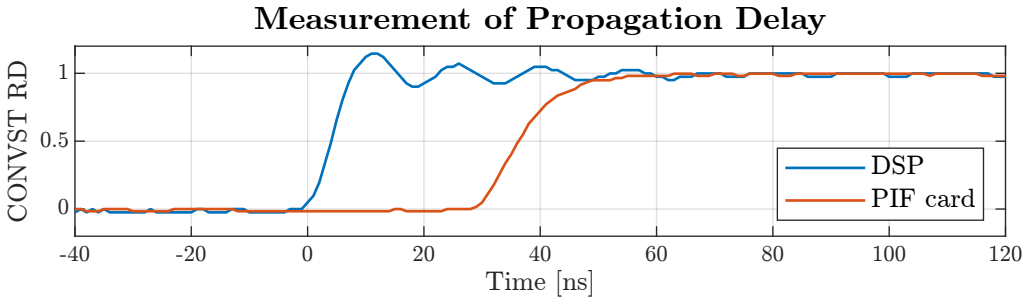


Figure 4.7: Measured propagation delay for CONVST RD from DSP to PIF card.

The total propagation delay from the DSP to the PIF card and then back again to the DSP due to propagation delays in transmitters, receivers, fibers, and ADC is estimated to be approx. 70 ns.

If a data bit returned from an ADC is to be read on the same clock cycle as it was requested, the delay time cannot exceed one half of the SPI clock period. This results in a maximum achievable transfer rate of 7.14 MHz, which means that from the available clock prescaler values, a transfer rate of 6.25 MHz is chosen. Operation of the SPI bus at this bit rate requires the SPI module on the DSP to be set up with a clock polarity of 0 and a clock phase of 1, which results in a clock cycle being initiated on a clock rising edge and data to be sampled on the following falling edge. A timing diagram relating the SPI clocking scheme to the measured propagation delays for the chosen bit rate of 6.25 MHz is shown in Fig. 4.8. Here, it can be seen how the clock generated at the SPI master [CLOCK(M)] will be delayed by the propagation delay of 30 ns when arriving at the SPI slave [CLOCK(S)]. The SPI slave initiates a data bit on its output [SDOx(S)] with a setup time of approx. 10 ns upon receiving the rising edge clock. This data then arrives at the SPI master [SDOx(M)] after an additional 30 ns of propagation delay. Hence, it can be seen that the data bit arrives just in time to be sampled on the falling edge of the same clock cycle at the SPI master.

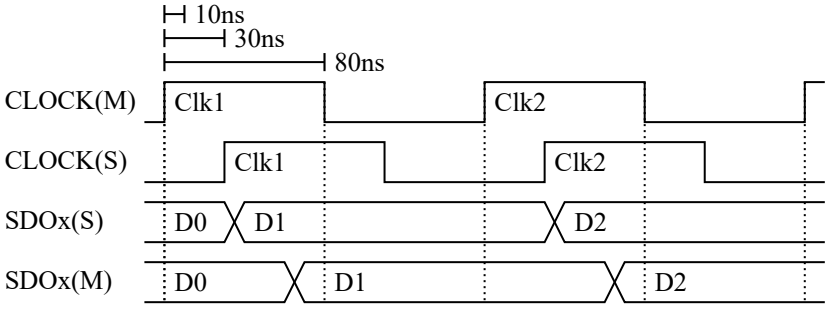


Figure 4.8: Timing diagram for SPI protocol at a bit rate of 6.25 MHz.

The total transmission time has been measured and the results are shown in Fig. 4.9. Here it can be seen that the total transmission time is approx. 32 μs, which leaves 68 μs for executing the control algorithm.

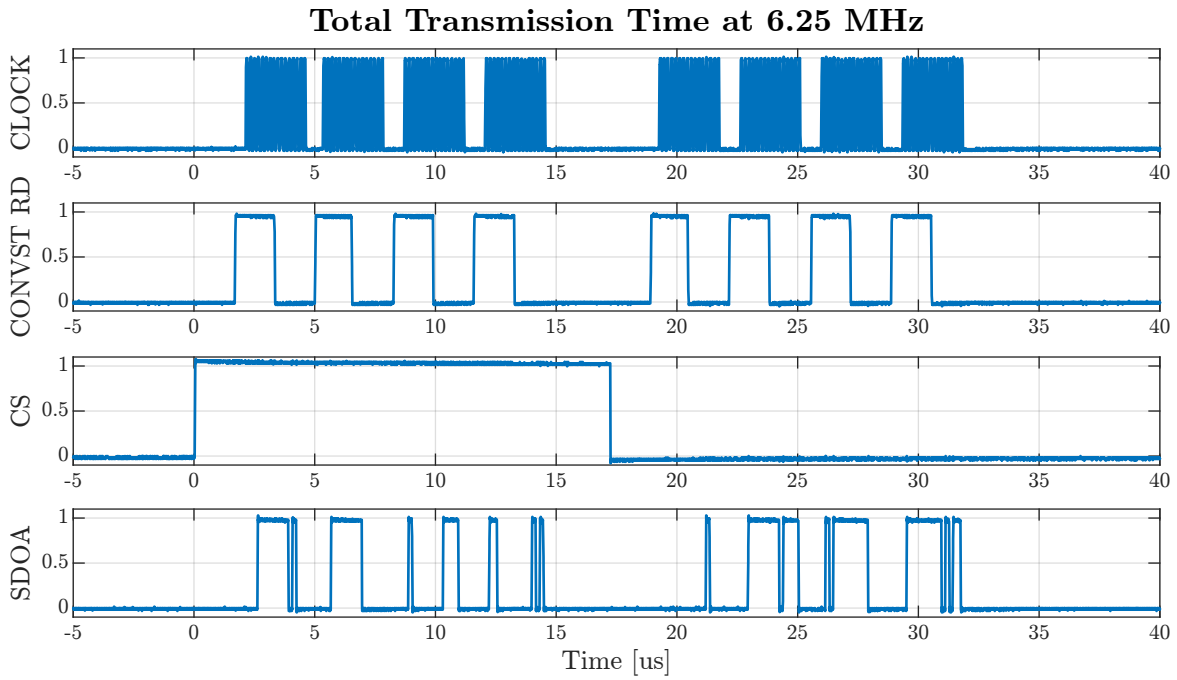


Figure 4.9: Measured total transmission time for all eight ADC channels at 6.25 MHz.

If needed, the transfer rate can be increased by allowing the data bits to arrive at the SPI master with one clock cycle delay from when the read transfer was initiated. This is possible as the ADCs finish each data transfer with a NULL bit as shown in Fig. 4.3. Hence, this bit can be allowed to be shifted out of the signal without any loss of information. The principle of operating the SPI bus in this way is shown by the timing diagram in Fig. 4.10 for the maximum allowable bit rate in the DSP of 12.5 MHz. Here, it can also be seen that the clock polarity can be chosen arbitrarily as both choices will result in data being taken with a safe margin to the setup time but with the before mentioned delay of one clock cycle.

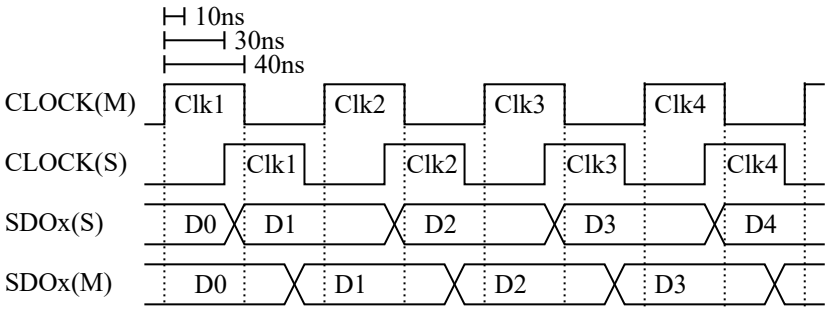


Figure 4.10: Timing diagram for SPI protocol at a bit rate of 12.5 MHz.

The total transmission time when increasing the bit transfer rate to 12.5 MHz has been measured and the results are shown in Fig. 4.11. Here it can be seen that the total transmission time is reduced to approx. 21 μs leaving 79 μs for executing the control algorithm.

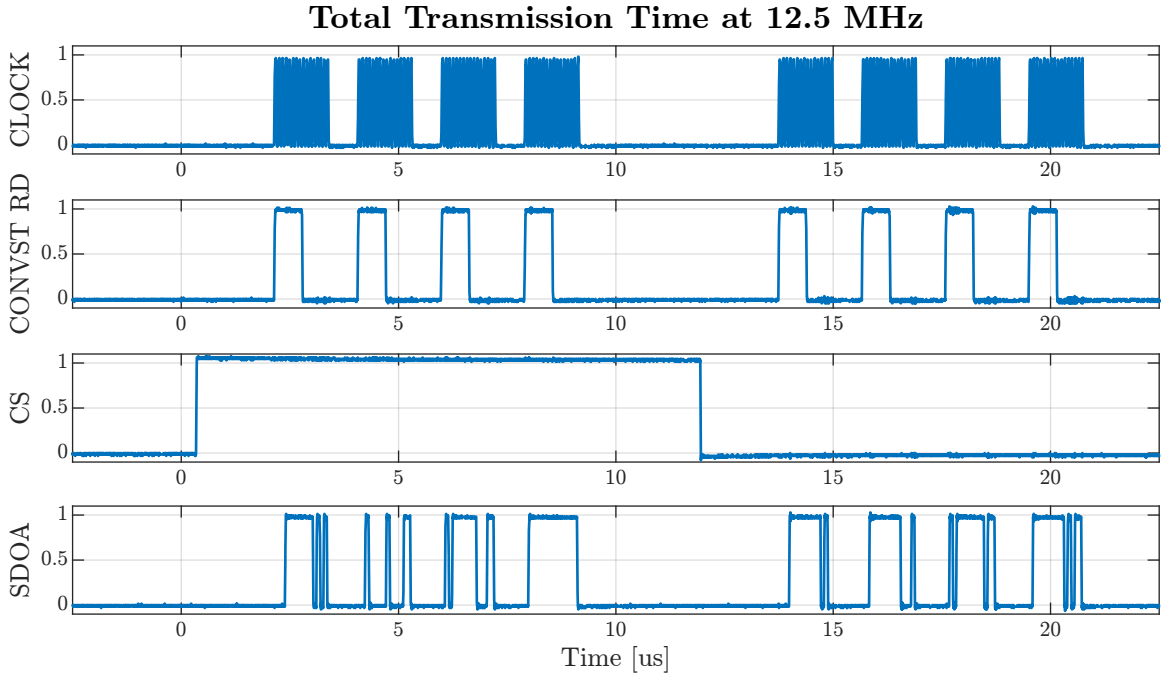


Figure 4.11: Measured total transmission time for all eight ADC channels at 12.5 MHz.

It should be noted that operating the SPI bus in this manner requires detailed knowledge of the propagation delays in the signal path, and therefore, is not recommended as a first measure. However, as the propagation delays have been identified and measured in this configuration, it is chosen to proceed with a transfer rate of 12.5 MHz.

4.1.4 ADC Offset, Signal-to-Noise Ratio, and Effective Number of Bits

To evaluate the effectiveness of the ADC and its measuring circuit, a measuring procedure of the ADC offset, signal-to-noise ratio (SNR), and effective number of bits (ENOB) have been implemented in the DSP to evaluate each of the ADC channels. The procedure takes into account the offset and noise introduced by components from the current/voltage sensors to the ADC inputs of the PIF card.

All of the components in the signal path from the sensor to the ADC will introduce an offset that needs to be measured before it can be corrected. The ADC itself has a typical offset of ± 0.5 LSB according to its datasheet [39]. A measuring procedure for the ADC offset has been implemented, which reads all of the eight ADC channels 1024 times and calculates their offsets based on the readings.

The SNR for each of the ADC channels is calculated from 1024 new readings by subtracting the calculated offsets from each of the new samples. The offset corrected samples are then used to calculate the RMS value which is then converted into a SNR in decibels. According to the datasheet of the ADC [39], it has a SNR of 71.5 dB corresponding to a gain of 0.026% or approx. 1 LSB for a 12 bit ADC. Therefore, an RMS lower than 1 LSB is not possible to achieve in practice with this ADC.

The performance and resolution of an ADC are specified in terms of its available bits, however, due to the above mentioned offset and noise caused by non-ideal components, the effective numbers of bits will be less than its datasheet value. The metric ENOB [43], [44] can be calculated from the SNR with the use of (4.3). The ADC itself has an ENOB of 11.5 bits, which means that it is not possible to achieve a resolution better than that in practice.

$$\text{ENOB} = \frac{\text{SNR} - 1.7609\ \text{dB}}{6.0206\ \text{dB}} \tag{4.3}$$

In the single phase setup, one current and two DC-link voltage channels have been populated on the PIF card. Therefore, those three ADC channels have been evaluated and their results are summarized in Table 4.2.

Table 4.2: Evaluation of ADC offset, SNR, and ENOB.

ADC Ch.	Meas.	Offset [LSB]	RMS [LSB]	SNR [dB]	ENOB [bits]
1	i_A	3	3	62.7	10.1
7	v_{DC+}	-1	4	58.3	9.4
8	v_{DC-}	-1	5	60.2	9.7

From the above table, it can be seen that each of the ADC channels is subject to a slight offset of a few LSB and a noise of less than 5 LSB. This results in a reduced number of effective number bits of around 10 bits, one of which is being used for the sign.

With the current configuration of the ADCs, the ideal 12 bit ADCs ends up having a resolution of approx. 10 mA and 2.5 V for the current and voltage measurements, respectively, according to the calculations from Appendix B. However, as the effective number of bits has been reduced by the noise, the resolution decreases to approx. 36 mA and 15 V, respectively.

4.2 Interfacing the State Machine on PIF Card

The functionality of the state machine (SM) on the CPLD is to provide a secure interface between the DSP and medium voltage power modules. The PIF card is designed to receive three PWM signals at maximum from which the CPLD generates the gate signals with the required dead time between turn-on and turn-off of the MOSFETs. The SM includes hardware protection against overcurrent, overvoltage, and overtemperature, which disables the applied gate signals to the power modules. It should be noted that the PIF card and SM are designed at AAU Energy before the start of this thesis, and therefore, the design choices have been made in advance.

The SM implemented in the CPLD on the PIF card can be described with the state machine diagram shown in Fig. 4.12.

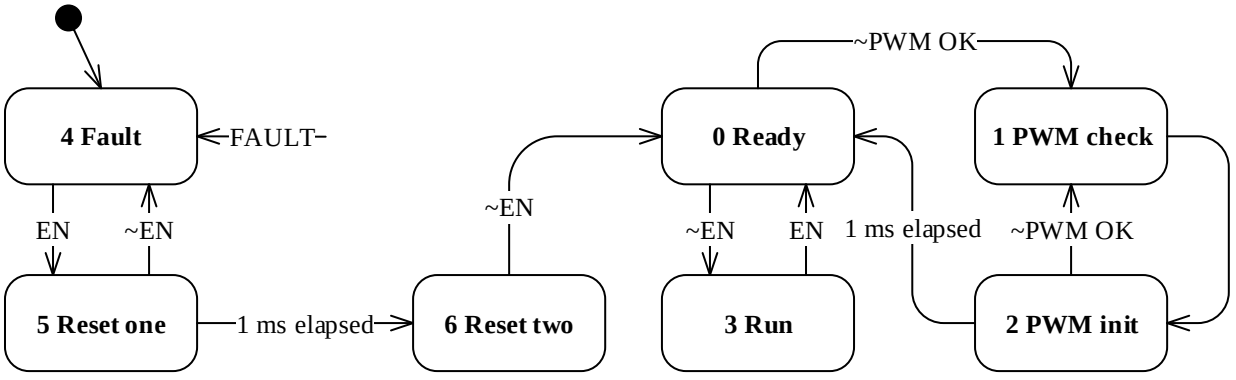


Figure 4.12: Overview of the state machine implemented on the PIF card.

The SM has several states as shown in the figure above, where the first state after powering up the PIF card is the Fault state. The SM will always transition to the Fault state if it receives an overcurrent, overvoltage, or overtemperature trip signal. To put the SM into its Ready state from which the gate signals can be enabled, a timed enabling sequence is required to transition through the Reset one and Reset two states. From the Ready state, the SM will loop into a check and initialization routine of the PWM inputs from the DSP if they are not kept low during the Ready state. If the PWM signals are kept low during the Ready state and the SM receives an enable signal (EN), the SM transitions into its Run state, where it outputs the gate signals with the desired dead time. The CPLD pulls a master enable pin (M EN) high whenever the SM is in its Run state.

With respect to the SM, the interface between the DSP and PIF card is limited to the enable signal (EN) from the DSP and the master enable signal (M EN) from the PIF card. However, the PIF card is designed with three GPIO pins used to indicate the active state of the SM. But, as the GPIO pins are not transmitted optically to the DSP, they cannot be directly connected to the DSP, and therefore, the active state of the SM is unknown for the DSP during the operation of the medium voltage converter.

However, during normal operation conditions, the PIF card will either be in its Fault or Ready state depending on its previous operating conditions. A generic enabling sequence is implemented in the DSP such that the PIF card will always transition into its Run state regardless of its previous state. First, the enabling sequence puts all the PWM signals low, as this is required to pass the PWM check. Simultaneously with pulling the enable signal high, the DSP starts an internal timer of 1.5 ms. Then, the DSP enters a while loop that only breaks if the timer overflows or if the master enable pin is set high by the PIF card. Afterward, the DSP sets the enable pin high to put the PIF card into its Run state where the gate signals are transmitted to the power modules. To disable the gate signal, the DSP needs to pull the enable pin low to put the PIF card back into its Ready state.

The three transitions mentioned above; from Fault to Run state, Ready to Run state, and Run to Ready state have all been tested without connecting the gate signals to the power modules. The enable signal (EN), the master enable signal (M EN), the PWM signal for phase A (PWM A), the gate signal for phase A high-side (GA H), and the active state of the SM have all been captured and are presented below.

Fault to Run State

The transition from the Fault to Run state is shown in Fig. 4.13. The transition shows that the SM transitions through the Reset one and Reset two states before entering the Ready state after 1.5 ms. The transition from the Ready state to the Run state is initialized after an additional 0.5 ms.

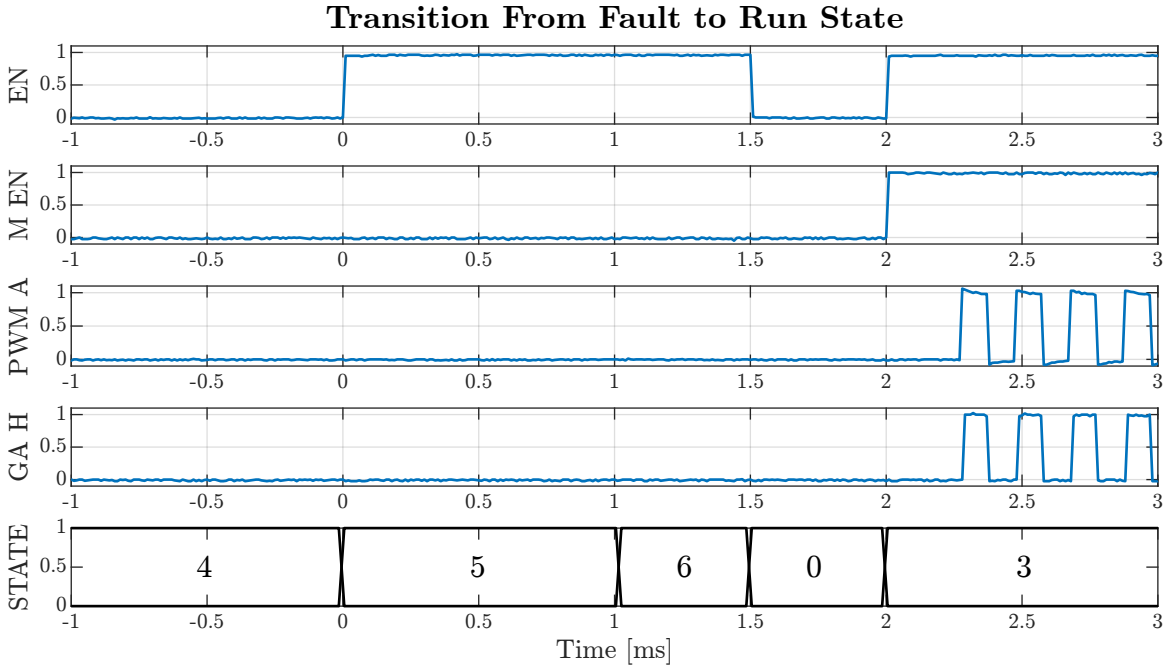


Figure 4.13: Measured transition from Fault to Run state on PIF card.

Ready to Run State

The transition from the Ready to Run state is shown in Fig. 4.14. The transition shows that the SM transitions for a very short period to the Run state before returning to its Ready state. During this short period, no gate signals must be transmitted to the power modules. The transition from the Ready state to the Run state is initialized after 0.5 ms.

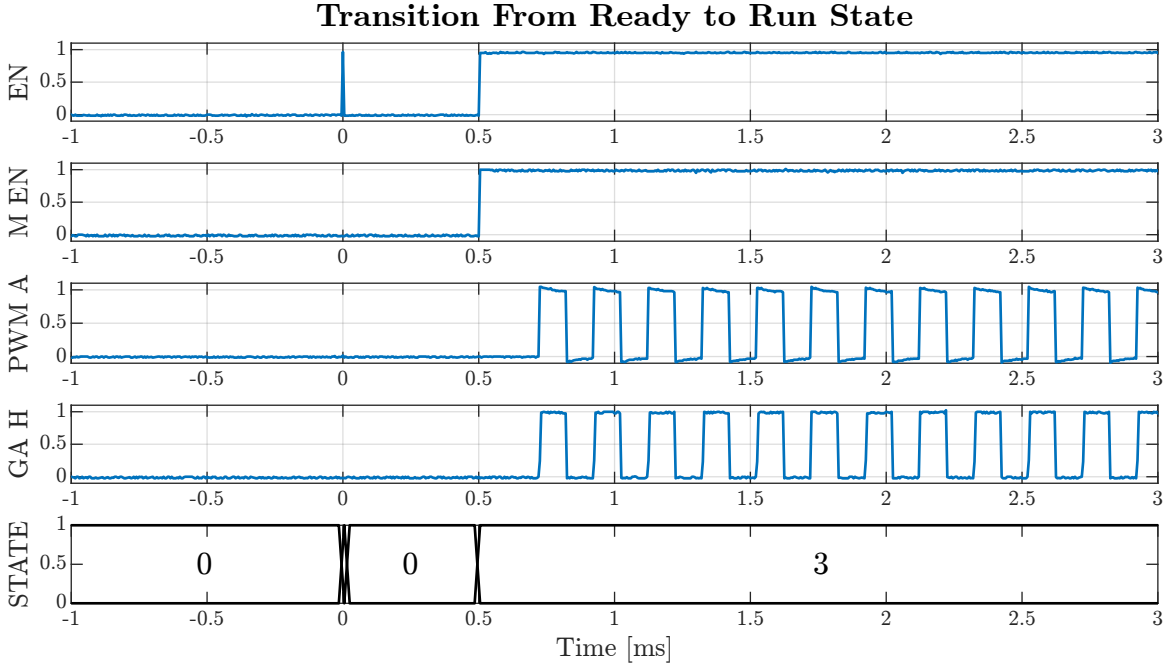


Figure 4.14: Measured transition from Ready to Run state on PIF card.

Run to Ready State

The transition from the Run to Ready state is shown in Fig. 4.15. The transition shows that the SM transitions from the Run state to its Ready state, but the PWM signal are not disabled immediately after pulling the enable pin low. Therefore, the SM transitions once through the PWM check and PWM initialization states before returning to the Ready state after approx. 1 ms. The PWM signals are afterward kept low and the SM stays in its Ready state.

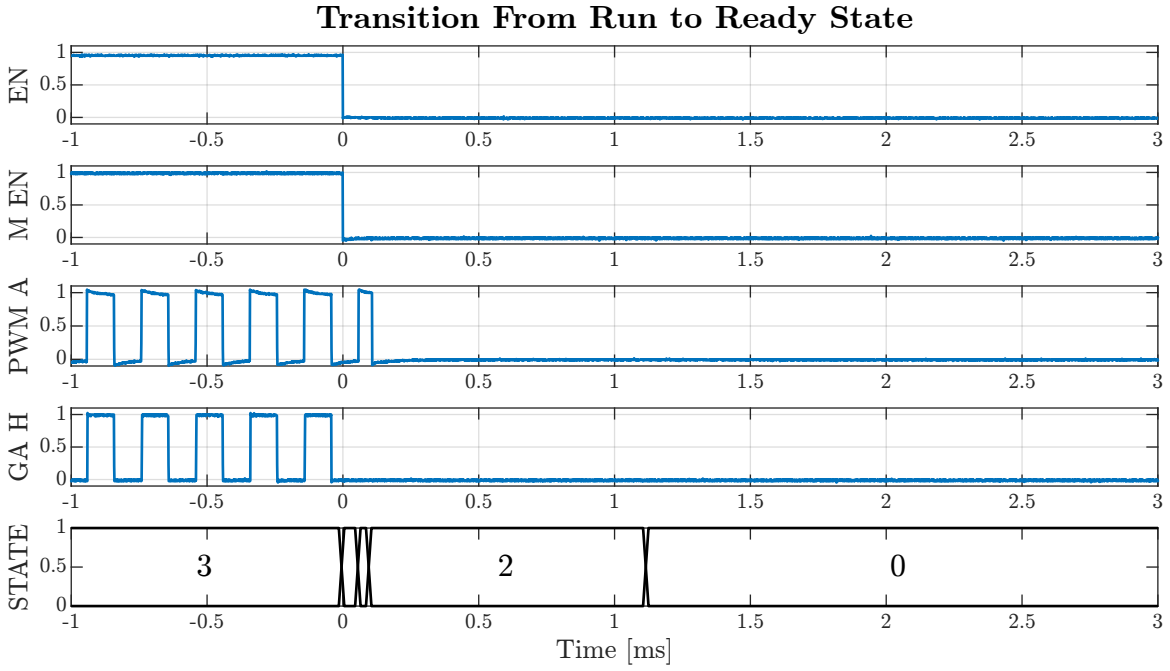


Figure 4.15: Measured transition from Run to Ready state on PIF card.

4.3 Common Mode Rejection on System Level

A special concern when working with medium voltage converters is capacitive couplings as the output terminals experience very high $\mathrm{d}v/\mathrm{d}t$ during the switching transients. In the last semester's project [1], the maximum $\mathrm{d}v/\mathrm{d}t$ of the power modules at hand was measured to be more than 30 kV/μs. At such high $\mathrm{d}v/\mathrm{d}t$ even low capacitive couplings in the picofarad range can result in circulating noise currents, which may cause EMI issues in the auxiliary equipment. Experience from operating the converter in the making of the previous semester's project [1] has shown that auxiliary equipment in the system, e.g. oscilloscope and thermal measurements, can be affected by noise and begin to malfunction when operating the converter at or close to its rated output voltage. The issues seen have not been associated with malfunctioning of the equipment as such, but rather with the remote interfacing of the equipment from outside of the high voltage (HV) cage. When building the setup, it has therefore been necessary to give special thought to the system layout such that the issues associated with the converter switching noise can be reduced to an acceptable level and reliable interfacing of all auxiliary equipment can be secured.

The issue with the converter switching noise is one of conducted EMI which is a very complicated affair to deal with and even more so to analyze and model in any level of detail. Given the many interconnections present in this system, the development of a noise model extends way beyond the scope and resources available for this thesis. Therefore, the noise has had to be dealt with by a

practical approach and has been handled by considering best practices, identifying the critical noise paths, and measuring the actual common mode (CM) currents present in these paths.

The process of reducing the impact of the switching noise has included many iterations made by introducing small changes in the system layout and measuring the CM current in important signal paths to see whether the changes were successful in reducing the measured noise. Attempting to give a detailed description of the procedure of steps would derail the discussion from the important takeaways, therefore, only an overview of the main findings and the changes associated herewith are presented in the following.

Experimental tests of the noise currents were conducted on the single phase setup described in Chapter 2 with both power modules switching synchronized at 50% duty cycle. Switching both power modules simultaneously will have the switching noise from each power module appear at the same time. This has also been shown to produce the largest peak amplitudes for the measured CM currents in the system. Therefore, this case has been defined as the worst-case and will be used for the entirety of the CM noise current tests. Common mode currents in signal wires have been measured with the LeCroy CP030 current probe as shown in Fig. 4.16, which exemplifies a current measurement in the USB cable to the DSP. As many of the measured CM currents are in the low mA range, these measurements are not to be taken for their exact values but have been used as the main debugging tool in determining the extent of CM current in different signal paths and the resulting reduction of them associated with changes to the system layout.

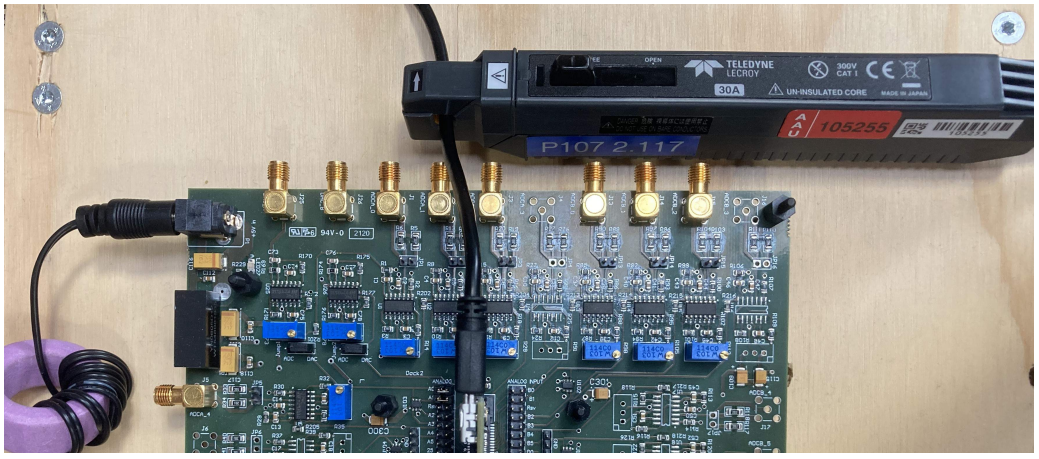


Figure 4.16: Photograph of a common mode current measurement in the USB cable.

After building the setup in its initial configuration, CM currents were measured at different locations in the setup, while the DC-link voltage was gradually increased. During these initial tests, it was experienced that the connections from the PC to the DSP and OpSens were lost and the experienced responsiveness of the connection to the oscilloscope was significantly slowed down when the DC-link voltage approached 2 kV.

4.3.1 Experimental Measurement and Reduction of Common Mode Noise

The loss of connection to the DSP was particularly disconcerting as no further advancements in the pursuit of closed loop control of the system could be made before a reliable connection was secured. Therefore, this has been dealt with first and the CM currents were measured in all wired connections to the DSP indicated in Fig. 2.7, which at that time included its power supply cord, its USB connection to the PC, and a trigger signal connected to the oscilloscope through a coaxial cable. The resulting

CM noise currents represented as their peak-to-peak values can be seen in Table 4.3. It should be noted that a peak-to-peak background noise of approx. 30 mA has been measured at no DC-link voltage for all of the measurement made.

Table 4.3: Measured common mode currents in wired DSP interconnections for the initial system configuration.

DC-link voltage	**1000 V**	**2000 V**	**3000 V**
Power Supply	210 mA_{PP}	350 mA_{PP}	450 mA_{PP}
USB Cable	350 mA_{PP}	600 mA_{PP}	780 mA_{PP}
Trigger to Scope	600 mA_{PP}	1030 mA_{PP}	1380 mA_{PP}

No scope data was saved for these particular measurements, but to illustrate the measured waveform of the CM noise currents, a measurement is taken at the USB cable for the DSP at another time during the attempts to reduce its noise can be seen in Fig. 4.17. It can be seen that the noise is slightly unsymmetrical around zero. This is likely to be explained by the higher $\mathrm{d}v/\mathrm{d}t$ seen during turn-on of the LS MOSFET compared to the turn-on of the HS MOSFET as it was found in [1].

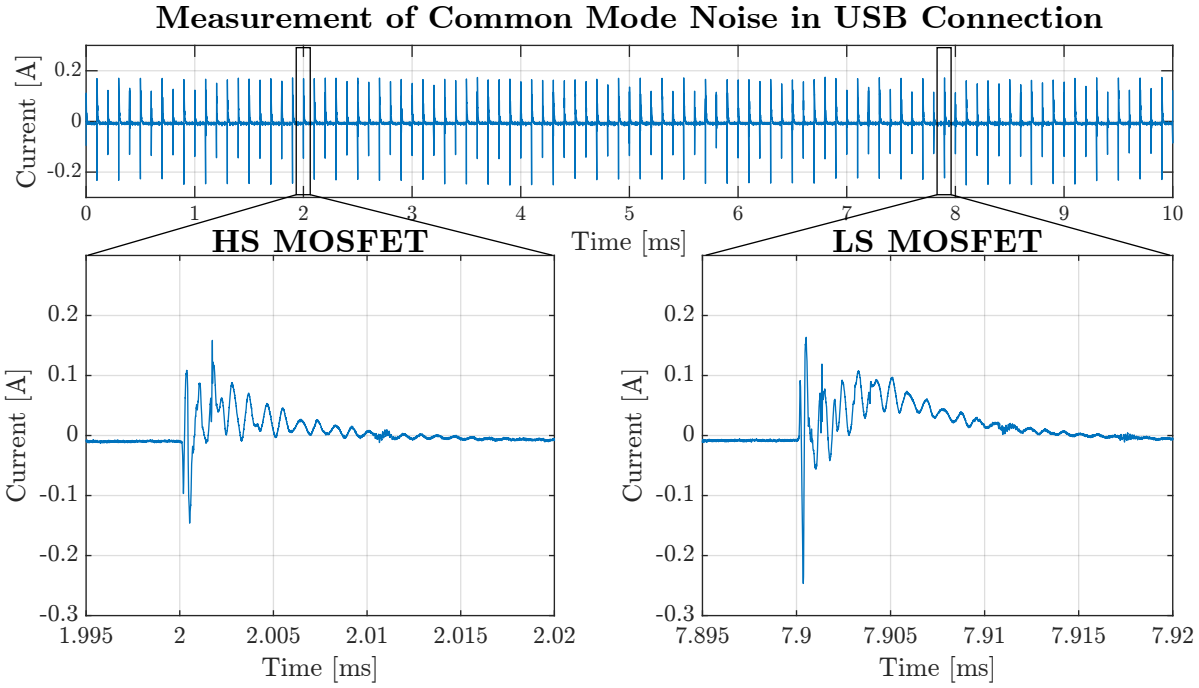


Figure 4.17: Measured common mode current in USB connection between DSP and USB isolator.

While taking the measurements in Table 4.3, it was found that the USB connection to the DSP was repeatedly lost when the CM current in it exceeded 600 mA peak-to-peak. The problem was identified to be in the BB-UHR402 USB isolator [45] which needed to be power cycled before the connection could be reestablished.

The results from Table 4.3 also showed that there was a high CM noise current present in the coaxial cable used to connect the trigger signal from the DSP to the oscilloscope. To prevent this noise current from propagating into the USB cable, the coaxial cable connecting the trigger pin of the DSP to the oscilloscope was removed. Instead, the trigger signal was provided by measuring the voltage at the triggering pin on the DSP with one of the HVFO isolated probes, which provides an optic fiber

interface. The rising edge of the measured voltage from the probe would then be used for generating the trigger event on the oscilloscope.

The high CM noise current measured in the trigger to the oscilloscope suggested that the oscilloscope could be a path of noise propagating from the power modules, through the probes connected to the oscilloscope, and further on to sensitive equipment in the system. It was also found that a significant amount of CM current was present in the power cord for the DSP. Based on these observations two initiatives were made.

First, the CM current in the probes connecting to the oscilloscope was measured to see if any probes in particular, could be associated with high CM noise currents going to the oscilloscope. At that time, the connections to the oscilloscope channels counted:

- 1 LeCroy CP030 current probe (used for measurement of CM noise in the other signals)
- 3 LeCroy HVFO103 isolated probes (not measured due to their optic fiber interface)
  - 2 for measurement of HS gate signals for the power modules
  - 1 for the trigger signal between oscilloscope and DSP
- 2 coaxial cables connected to the input interface of the PIF card
  - 1 for measuring the output of the LEM LA 55-P current sensor used for measuring the load current (voltage across measuring resistor)
  - 1 for measuring the output of the LEM DVM 4000 voltage sensor used for measuring the positive DC-link voltage (voltage across measuring resistor)
- 1 LeCroy PPE4kV high voltage passive probe (used for measuring the output voltage)

The resulting measured peak-to-peak CM currents are shown in Table 4.4. As was the case in Table 4.3, measurements are taken for DC-link voltages of 1, 2, and 3 kV.

Table 4.4: Measured common mode currents in channels to the oscilloscope.

DC-link voltage	**1000 V**	**2000 V**	**3000 V**
LEM LA 55-P	175 mA_{PP}	290 mA_{PP}	375 mA_{PP}
LEM DVM 4000	170 mA_{PP}	275 mA_{PP}	345 mA_{PP}
HV Passive Probe	800 mA_{PP}	1100 mA_{PP}	1370 mA_{PP}

From these results, there was seen to be a substantial amount of CM noise for all three channels, with the HV passive probe being especially troublesome. It was therefore decided to try to replace the HV passive probe with a HV differential probe. The resulting CM currents measured in the HV differential probe can be seen in Table. 4.5

Table 4.5: Measured common mode currents of high voltage differential probe.

DC-link voltage	**1000 V**	**2000 V**	**3000 V**
HV Differential Probe	185 mA_{PP}	290 mA_{PP}	365 mA_{PP}

As the HV differential probe showed to introduce significantly less CM current between the power module and the oscilloscope, it was decided to replace the passive probe with the differential one.

Next, as it had been seen in Table 4.3 that a significant amount of CM currents were also present in the power supply cord for the DSP, it was decided to group the layout of the power supplies into *clean* and *dirty* equipment. The *clean* equipment is categorized as not having any direct electrical connections to the power modules or their DC power supplies. This holds for the DSP and OpSens as all interfaces directly or indirectly connecting these to the power stacks are made using optical fibers. Conversely, *dirty* equipment is defined as everything which is directly or indirectly connected to the power modules or their DC power supplies without the use of optic fibers in the interface. The resulting layout can be seen in Fig. 4.18, where the *clean* equipment is grouped on UPS 1 and the *dirty* equipment is grouped on UPS 2. To further increase the CM impedance, isolation transformers are inserted between the mains supply and the UPS for each of the two groups.

Initially, these two groups of equipment were still connected through an Ethernet cable from the OpSens to the Ethernet switch. This was to be able to remotely access the die temperature measurements from the PC. However, this interface turned out to be very susceptible to noise and the connection to the OpSens was lost for CM currents as low as 50 mA in its Ethernet cable. Therefore, interfacing remotely with the OpSens was given up, and die temperature measurements were read from its display instead.

After implementing these modifications the measured CM currents in the power supply and USB cable for the DSP were significantly reduced compared to the ones presented in Table 4.3 and no more issues were encountered with the DSP interface. The measured values are presented in Table 4.6.

Table 4.6: Measured common mode currents in wired DSP interconnections for the initial system configuration.

DC-link voltage	**1000 V**	**2000 V**	**3000 V**
Power Supply	135 mA_{PP}	215 mA_{PP}	290 mA_{PP}
USB Cable	110 mA_{PP}	150 mA_{PP}	160 mA_{PP}

4.3.2 Drop-out of Ethernet Connection with Increasing DC-Link Voltage

With the connection to the OpSens being removed from the Ethernet switch, the remaining equipment interfaced remotely through a wired Ethernet connection were the two DC power supplies and the oscilloscope. This configuration was working successfully for all the tests taken at 3 kV DC-link voltage. However, as the voltage was further increased to achieve operation of the system at 6 kV, the connection was lost around 5 kV DC-link voltage. This issue was partially solved by interfacing the oscilloscope via a local WiFi network, which was made possible by inserting a USB WiFi dongle into the oscilloscope. This way, the DC power supplies were the only equipment still interfaced with the wired Ethernet connection. Even in this configuration, the interface to the DC power supplies was still not working optimally. At high DC-link voltages, the connection was periodically interrupted but could automatically reestablish itself within a few seconds.

4.3.3 Final Configuration

The final configuration which was successfully used to operate the system at its rated DC-link voltage of 6 kV is shown in Fig. 4.18. Though admittedly not ideal, this was the final configuration used for testing in this thesis, which allowed for operating the system at its rated DC-link voltage of 6 kV. With the difficulties encountered throughout this testing, it is clear that further work needs to be done to secure a more reliable operation of the system. However, this was not achieved within the time frame of this thesis.

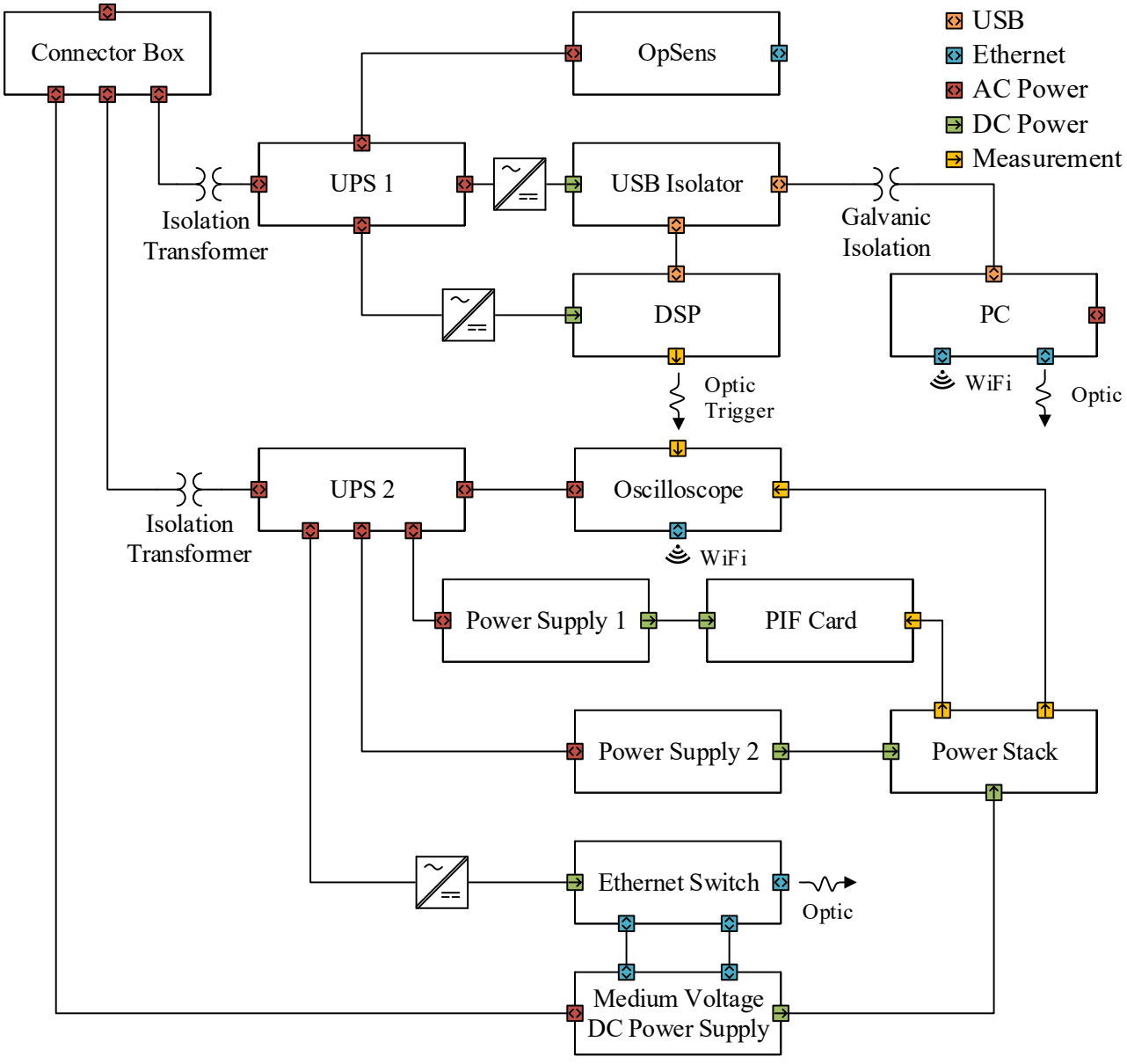


Figure 4.18: System configuration used for successful system operation at 6 kV DC-link voltage.

Chapter 5

Implementation of Current Controllers

This chapter includes a detailed description of the procedure followed to implement, test, and validate the current controllers and the proposed sampling scheme presented in [1], [2].

The first section describes the operation of the system in open loop control and presents the corresponding test results. The main purpose of this section has been to evaluate the performance of the proposed sampling scheme before utilizing the sampled currents to close the control loop. With the proposed sampling scheme successfully evaluated, the current feedback was considered sufficiently good to proceed with closing the control loop and implementing the current controllers as will be described in the subsequent sections.

The second section is concerned with the implementation of a suitable dead time compensation algorithm for the current controllers. As previous simulations made in [1] have shown the voltage error introduced by the converter dead time to have a pronounced effect on the control loop performance, in terms of both magnitude error and current waveshaping properties, the implementation of a suitable dead time compensation algorithm has been a priority form the beginning.

The actual implementation and test of the closed loop current control is presented in the third section. The closed loop control has been implemented and tested first by use of a PI controller and then by a Proportional-Resonant (PR) controller. Results are first presented individually for each controller type before their performances are discussed and compared.

Before proceeding, the reader should be notified that the initial tests are limited to 3 kV DC-link voltage for both open and closed loop control, even though the converter is designed and built for a rated DC-link voltage of 6 kV. This has been done to reduce the risks of causing damage to the power modules as introduced in Chapter 3. Closed loop control has later been achieved at a DC-link voltage of 6 kV and the corresponding results are presented in separate sections of this chapter.

5.1 Open Loop Control

In open loop control, the gate signals are calculated based on the voltage reference defined by a fixed modulation index and phase. Both converters are set to operate at a modulation index of 0.8 and the current is controlled by modifying the phase difference between the voltage references. By considering the plant impedance to be primarily inductive with negligible resistance, the plant can be represented as shown in Fig. 5.1 and controlled by considering the phasor diagram of Fig. 5.2.

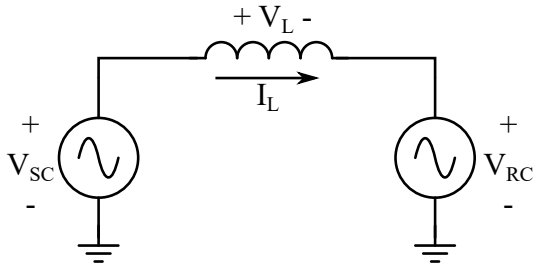


Figure 5.1: Open loop control schematic.

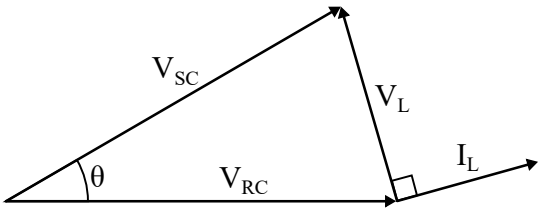


Figure 5.2: Open loop phasor diagram.

A simplified calculation of the phase difference is given in (5.1).

$$\theta = 2 \arcsin\left(\frac{Z_L \cdot I_{L,RMS}}{2V_{RMS}}\right) \tag{5.1}$$

where Z_L is the impedance of the inductor, $I_{L,RMS}$ is the desired RMS load current, V_{RMS} is the RMS voltage for each of the converters, and θ is the phase angle between these voltages.

As the RMS voltages need to be supplied by a PWM converter, it is necessary to express them in terms of their DC-link voltage and modulation index. Therefore, equation (5.1) becomes:

$$\theta = 2 \arcsin\left(\frac{Z_L \cdot I_{L,RMS}}{V_{DC} \cdot m_a/\sqrt{2}}\right) \tag{5.2}$$

where V_{DC} is the DC-link voltage and m_a is the modulation index.

The open loop control has been tested at different DC-link voltages at or below 3 kV and with desired currents between 0 and 7 A RMS with similar results as that presented in [1], [2].

5.1.1 Evaluation of the Proposed Sampling Scheme

With the open loop control successfully implemented, it has been possible to experimentally evaluate the proposed sampling scheme from [1], [2]. The proposed sampling scheme is based on a double sample, single update principle, where the current is sampled both at a ZERO and PERIOD compare event. This means that the voltage reference is only updated once pr. fundamental period based on either the current sample from the ZERO or PERIOD compare event. The sample chosen only depends on the previously calculated duty cycle. For a duty cycle above 50%, the current sample from the ZERO compare event is chosen, whereas, for a duty cycle below 50%, the current sample at the PERIOD compare event is chosen. This ensures that the samples used are never taken in close proximity to the switching events and therefore reduces the risk of sampling the current while being corrupted by noise. The proposed sampling scheme is illustrated in the schematic shown in Fig 5.3.

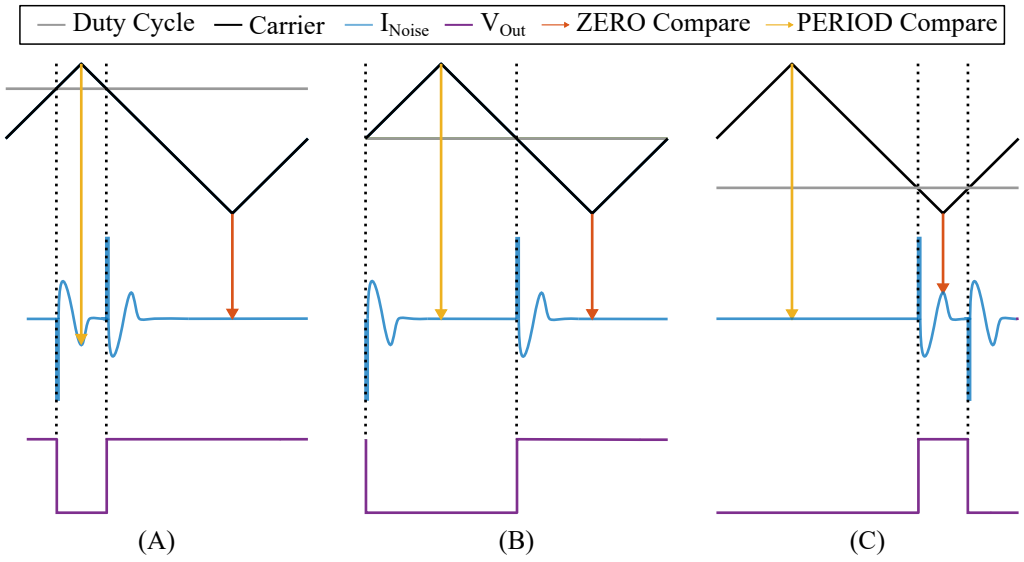


Figure 5.3: Illustration of sampling scheme at duty cycles of (A) 80%, (B) 50%, (C) 20% [1], [2].

The measurements presented onwards in this section are at a DC-link voltage of 3 kV and the desired load current of 7 A RMS. The proposed sampling scheme has been evaluated by sampling the currents on the DSP and comparing them with the measurement output from the current sensor (LEM LA 55-P) taken as the output voltage across the measuring resistor at the input interface on the PIF card. A comparison of these signals shows the effectiveness of the proposed sampling scheme. As will be illustrated in the following, the high noise amplitude present in the input signal is completely eliminated in the sampled signal, partly due to the filtering in the PIF card and partly due to the sampling scheme. The sampled current along with the output from the LEM LA 55-P at the PIF card are shown in Fig. 5.4.

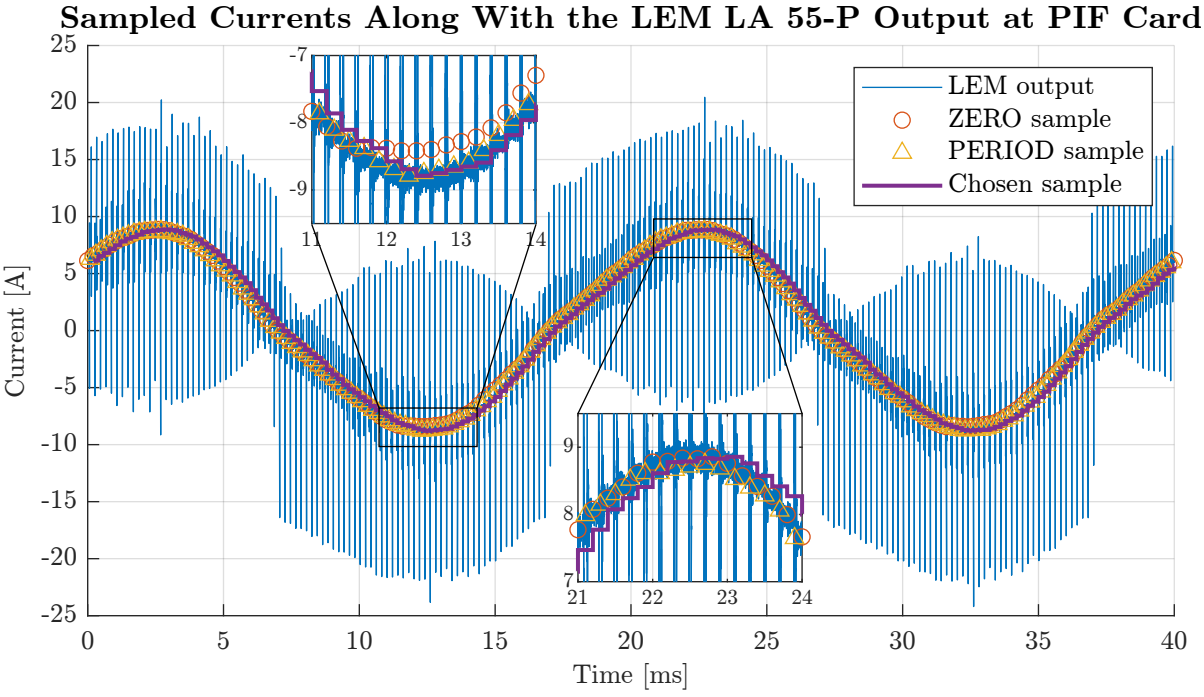


Figure 5.4: Sampled currents compared to the measurement output of LEM LA 55-P.

Furthermore, the sampled currents from the DSP are compared to a reference current measurement made with the current probe (LeCroy CP030). The comparison is shown in Fig. 5.5 and it shows that the sampled currents are well aligned with the reference measurements.

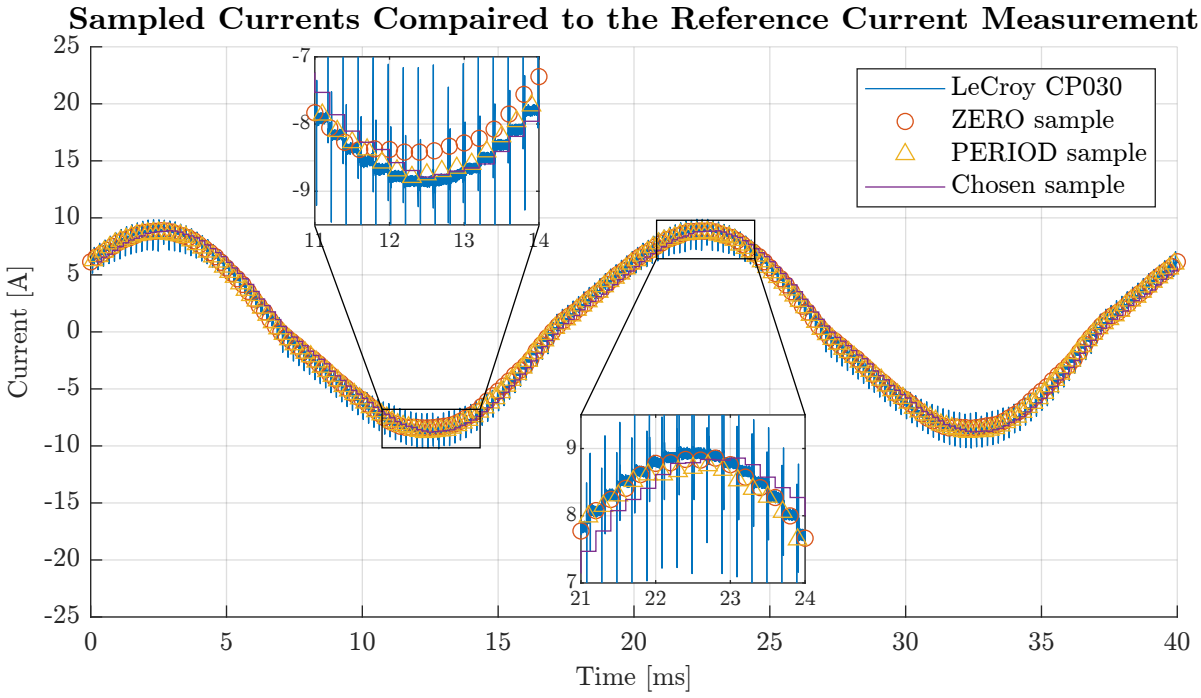


Figure 5.5: Sampled currents compared to the reference measurement made with LeCroy CP030.

From the above figures, it is concluded that the proposed sampling scheme is capable of sampling the current without any significant noise contribution caused by the high $\mathrm{d}v/\mathrm{d}t$ during the switching transients. It can also be noted that the current waveforms are distorted when the converter is operated in open loop control as the peaks are skewed to the right compared to an ideal sinusoid. This phenomenon is affected by multiple non-linear factors, one of which is the dead time voltage error which will be explained in greater detail in the next section.

5.2 Dead Time Compensation

When using a half-bridge converter to generate the desired output voltage, the PWM signals from the modulator need to be converted into complementary gate signals for the HS and LS which can be applied to their respective gate driver circuitry. Due to the finite switching speeds of the power semiconductor devices, it is necessary to implement some form of dead time between the turn-off of one switch and the subsequent turn-on of the complementary. This is to avoid a shoot-through of the DC-link, which can occur if both the HS and LS switches of the same half-bridge are turned on at the same time [46]. However, adding dead time to the gate signals will introduce an error in the resultant output voltage compared to the ideal commanded PWM voltage. The magnitude of this error is derived for ideal switching transients in [46]. Here, the error is shown to be dependent on the load current polarity, the dead time, the switching frequency, and the DC-link voltage, and can described as stated in (5.3).

$$\Delta V = -\frac{t_d}{T_{sw}} \cdot V_{DC} \quad , I_{Load} > 0 \qquad\qquad \Delta V = +\frac{t_d}{T_{sw}} \cdot V_{DC} \quad , I_{Load} < 0 \tag{5.3}$$

where ΔV is the voltage error introduced by dead time, t_d is the dead time, T_{sw} is the switching time period, V_{DC} is the DC-link voltage, and I_{Load} is the load current.

The impact of this dead time error can be seen from the current waveforms presented in Fig. 5.5. Here, it was seen how the waveforms are distorted with their peaks skewed to the right compared to an ideal sinusoidal current. This behavior can be explained by considering the voltage errors presented in (5.3). When the current polarity is positive, the dead time voltage error is negative and the output voltage of the converter is reduced. Therefore, the inductor voltage is less and the rate of change of current is slowed down. Similarly, after the current reaches its peak value, the rate of change of current is decreased by the negative dead time voltage error. This combines to produce the skewed current waveforms and should be compensated for.

5.2.1 Initial Dead Time Compensation Algorithm

Knowing this theoretical voltage error derived assuming ideal switching characteristics, meant that a simple initial compensation algorithm could be implemented merely based on the sign of the measured current. The voltage error from (5.3) is added or subtracted depending on the polarity of the current to compensate for the voltage loss or voltage gain, respectively.

This simple dead time compensation algorithm, even though seemingly effective from the simulations in [1], proved to have some instability issues when implemented in the experimental setup. The issue arises at low current references, where the compensated voltage error is greater than the controller output voltage. The instability issue appears as a step change in the compensation voltage which causes the inductor current to regularly jump as demonstrated by the simulation results shown in Fig. 5.6. Here, the controller is given a 0 A current reference and some noise is introduced in the feedback signal as will be the case in any practical application.

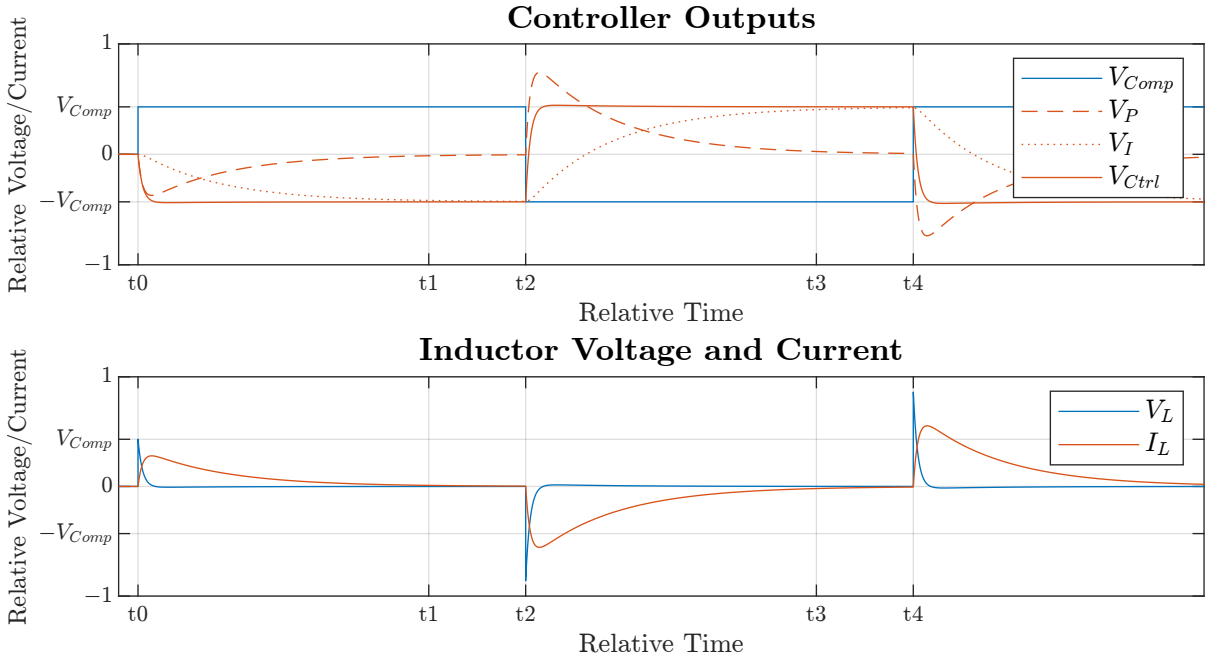


Figure 5.6: Simulation of instability issue caused by the initial dead time compensation algorithm.

At the time t_0, the noise in the feedback signal results in a current measurement with a positive sign, which causes the dead time compensation algorithm to compensate with the voltage V_{Comp}. This

will result in a relatively high voltage being applied to the filter inductors which in turn causes a rapid increase in the inductor current. As the inductor current increases, the proportional term of the PI controller will start to output a negative voltage which reduces the voltage applied to the filter inductor and thereby stabilizes the system shortly thereafter. Then, during the remaining time interval between t_0 and t_1, the controllers integral term will slowly increase its output to take over from the proportional term and to bring back the measured current close to its reference at 0 A. At the time t_2, the measured current has been brought back to its 0 A reference, but now the measurement noise causes the reading of a negative current measurement, which immediately causes the compensation voltage to change sign. This time, the situation is worsened by the integral term which had been built up to compensate for the previous compensation voltage. The current therefore builds up to roughly twice the error as what was seen at t_0 before the proportional term of the controller can counteract the effect and stabilize the current again. From here, the pattern repeats with the integrator building up a voltage to counteract the compensation voltage until the sign of the measured current reverses again at t_4.

A similar pattern occurs at low current references where the necessary output voltage needed to drive the sinusoidal current is low compared to the compensation voltage. This will cause a similar oscillatory behavior as the one demonstrated above but overlaid with the reference sinusoidal current. The simulation results are shown in Fig. 5.7.

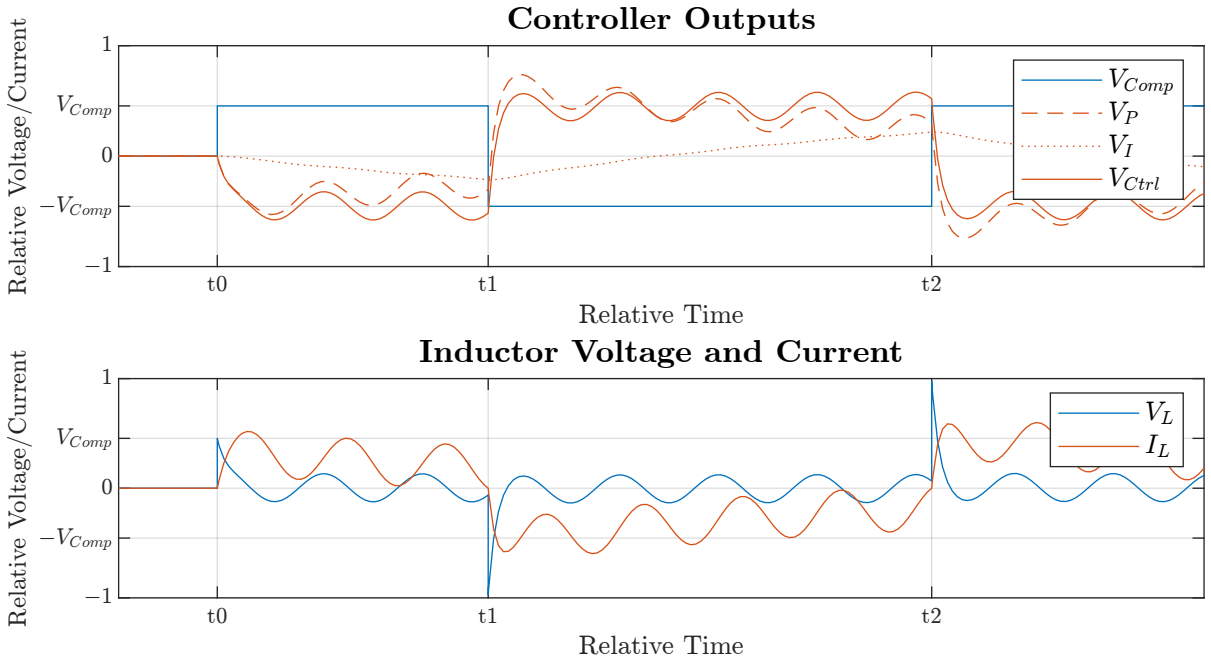


Figure 5.7: Simulation of instability issue caused by the initial dead time compensation algorithm.

Higher current references will tend to stabilize the situation as the controller output voltage will dominate the voltage gain from the dead time compensation algorithm. In this case, the dead time compensation does not upset the system around the current zero crossing but instead helps to compensate for the voltage lost due to the dead time voltage error which helps to bring the load current magnitude closer to its reference.

5.2.2 Fitted Dead Time Compensation Algorithm

Due to the instability issues associated with the initial dead time compensation algorithm, there was a desire to modify it to improve its performance. From the discussion above, it is apparent that something had to be changed in the compensation algorithm at low current references without sacrificing the benefits at higher currents. As the turn-off voltage transients, and thereby the dead time voltage error, is known to be load current dependent [47], it was desired to take the current dependency into account in the new fitted dead time compensation algorithm. This has been done by evaluating the dead time voltage error from measured turn-on and turn-off voltage waveforms for varying levels of load currents.

Load Current Dependency of MOSFET Switching Transient

The switching transients of a power MOSFET depend on a variety of factors including, but not limited to, the I/V characteristics, its gate driver circuitry, the parasitic device capacitances, and the transient behavior of the circuit in which it is applied. This section covers the MOSFET turn-on and turn-off characteristics with the aim of describing the load current dependency of the voltage switching waveforms. The aim is not to provide a detailed and exact analysis of the switching transients but rather to give a qualitative description of the dependency on the load current.

The switching characteristics will be described by considering the generic MOSFET I/V characteristics shown in Fig. 5.8 while taking into account the necessary charging and discharging of the parasitic device capacitances shown in Fig. 5.9.

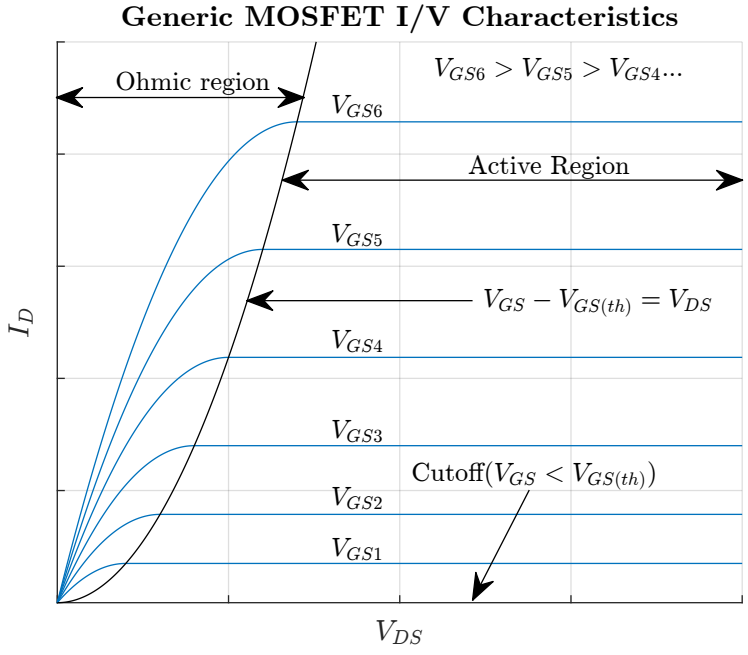


Figure 5.8: Generic MOSFET I/V characteristics.

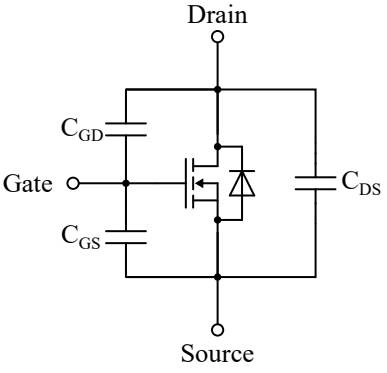
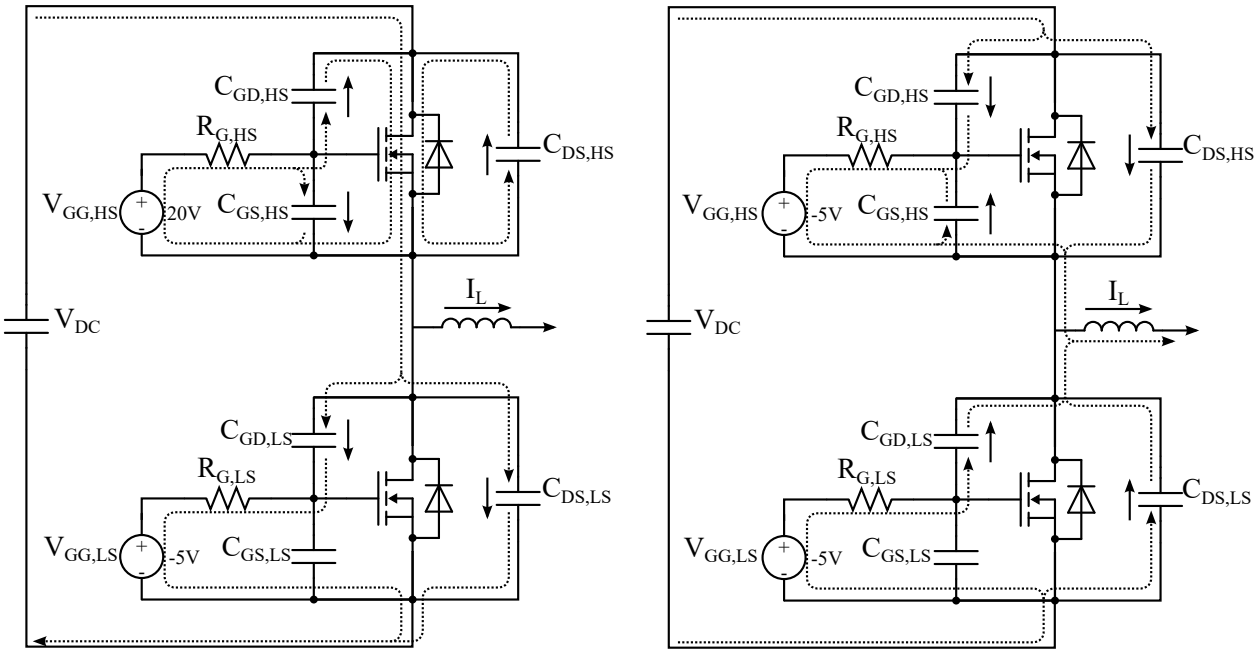


Figure 5.9: MOSFET with parasitics.

First, the **turn-on switching transient** of the HS MOSFET will be considered. The load current is assumed to be positive constant out of the half-bridge. The LS MOSFET is assumed to be turned off, and the LS diode is initially conducting all of the load current with a negligible voltage drop, and hence, the HS MOSFET blocks the full DC-link voltage. During a turn-on of the HS MOSFET, the voltage needs to simultaneously build across the LS MOSFET while decreasing across the HS MOSFET.

This, combined with the charging of the HS gate-source capacitance means that the capacitances $C_{GS,HS}$, $C_{GD,LS}$, and $C_{DS,LS}$ need to be charged while the capacitances $C_{GD,HS}$ and $C_{DS,HS}$ need to be discharged. This charging and discharging of the capacitances gives rise to displacement currents in the capacitances with their directions indicated by the arrowheads in Fig. 5.10a.



(a) HS MOSFET turn-on.

(b) HS MOSFET turn-off.

Figure 5.10: Charging and discharging of parasitic capacitances during switching transients.

When a positive gate signal is applied to the HS MOSFET at time t_0 as shown in Fig. 5.11, the capacitance $C_{GS,HS}$ will begin to charge by the mesh current through $V_{GG,HS}$, $R_{G,HS}$, and $C_{GS,HS}$ as indicated on Fig. 5.10a. With the gate-source voltage initially being below the threshold voltage, the HS MOSFET will be in the cutoff region as illustrated on the I/V characteristics in Fig. 5.8.
Eventually, the gate-source voltage will reach the threshold voltage and the HS MOSFET will start to conduct at time t_1. In the following time until t_2, the gate-source voltage of the HS MOSFET gradually builds up while its drain current increases. The HS MOSFET is vertically ascending the active region of the I/V curves in Fig. 5.8 as it still needs to block the full DC-link voltage due to the forward bias of the LS diode.
At the time t_2, the load current is fully commutated from the LS diode to the HS MOSFET and the LS diode can become reverse biased. The drain-source voltage of the HS MOSFET can now start to decrease while the drain-source voltage of the LS MOSFET increases. During this time interval, the HS MOSFET is traversing the active region of the I/V curves shown in Fig. 5.8 and its gate-source voltage is fixed at the voltage needed to drive the load current. This traversing of the I/V curve is essentially a process of charging and discharging the capacitances through the remaining mesh current loops illustrated in Fig. 5.10a. All of these mesh currents can be sourced through the channel of the HS MOSFET and the charging of the capacitances are therefore independent of the load current. In fact, the process of charging the capacitances will cause both the channel current and the gate-source voltage of the HS MOSFET to be elevated during this time interval as the HS MOSFET channel needs to supply both the load current and the capacitive charging currents [47]. This elevation of voltage and current is shown with dashed lines in Fig. 5.11.

After time t_3, the gate-drain and drain-source capacitances of the HS MOSFET are fully discharged, and the MOSFET enters the Ohmic region shown in the I/V curves of Fig. 5.8. This causes the gate-source voltage of the HS MOSFET to increase to $V_{GG,+}$ and its drain-source voltage to decrease to the voltage drop caused by the on-state resistance.

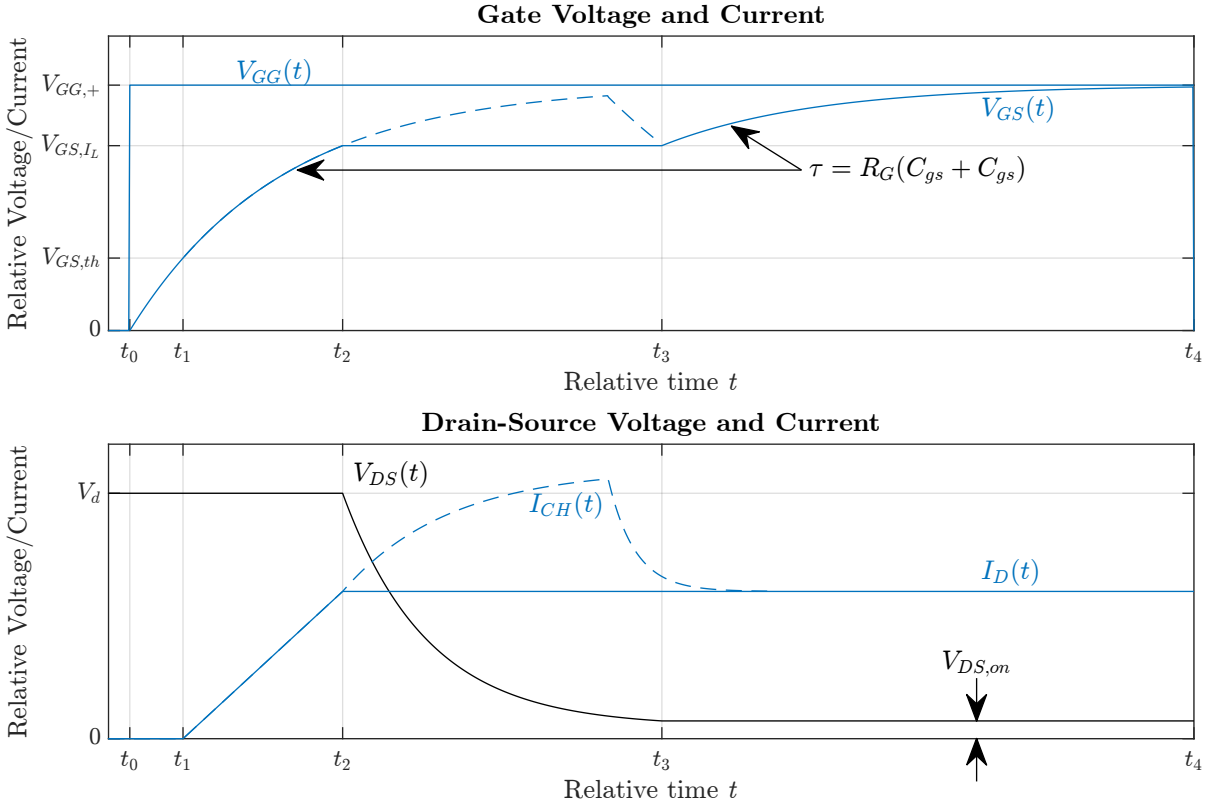


Figure 5.11: Switching transients during turn-on of HS MOSFET.

The **turn-off switching transient** of the HS MOSFET work very differently from the turn-on transients as the currents needed to charge and discharge most of the capacitances are highly dependent on the inductive load current [47]. The only exception is the gate-source capacitance of the HS MOSFET, as this can be discharged directly through the gate driver circuitry. Therefore, the switching speed during a turn-off varies with the load current in contrast to a turn-on, where the switching speed is purely determined by the gate driver circuitry and gate-source capacitance of the MOSFET. The mesh current paths utilized in the capacitive charging process during a turn-off transient are shown in Fig. 5.10b, where the arrowheads indicate the direction of the necessary displacement currents for the charging process. This leads to the different behavior of the turn-off transients for low and high values of load current as illustrated in the switching waveforms presented in Fig. 5.12.

First, the switching transient is considered for a HS turn-off at a high load current illustrated with the solid lines in Fig. 5.12. The turn-off is initiated at time t_0 where the gate driver output is driven low and is characterized by three distinct exponential decays in the gate-source voltage of the HS MOSFET. First, the discharge of V_{GS} initially causes the HS MOSFET to move from the Ohmic region to the boundary of the active region until its gate-source voltage reaches the level needed to drive the load current. In this time interval, the HS MOSFET channel is carrying the full load current. From hereon, the further decrease of the gate-source voltage of the HS MOSFET will start to limit its channel current, I_{CH}.

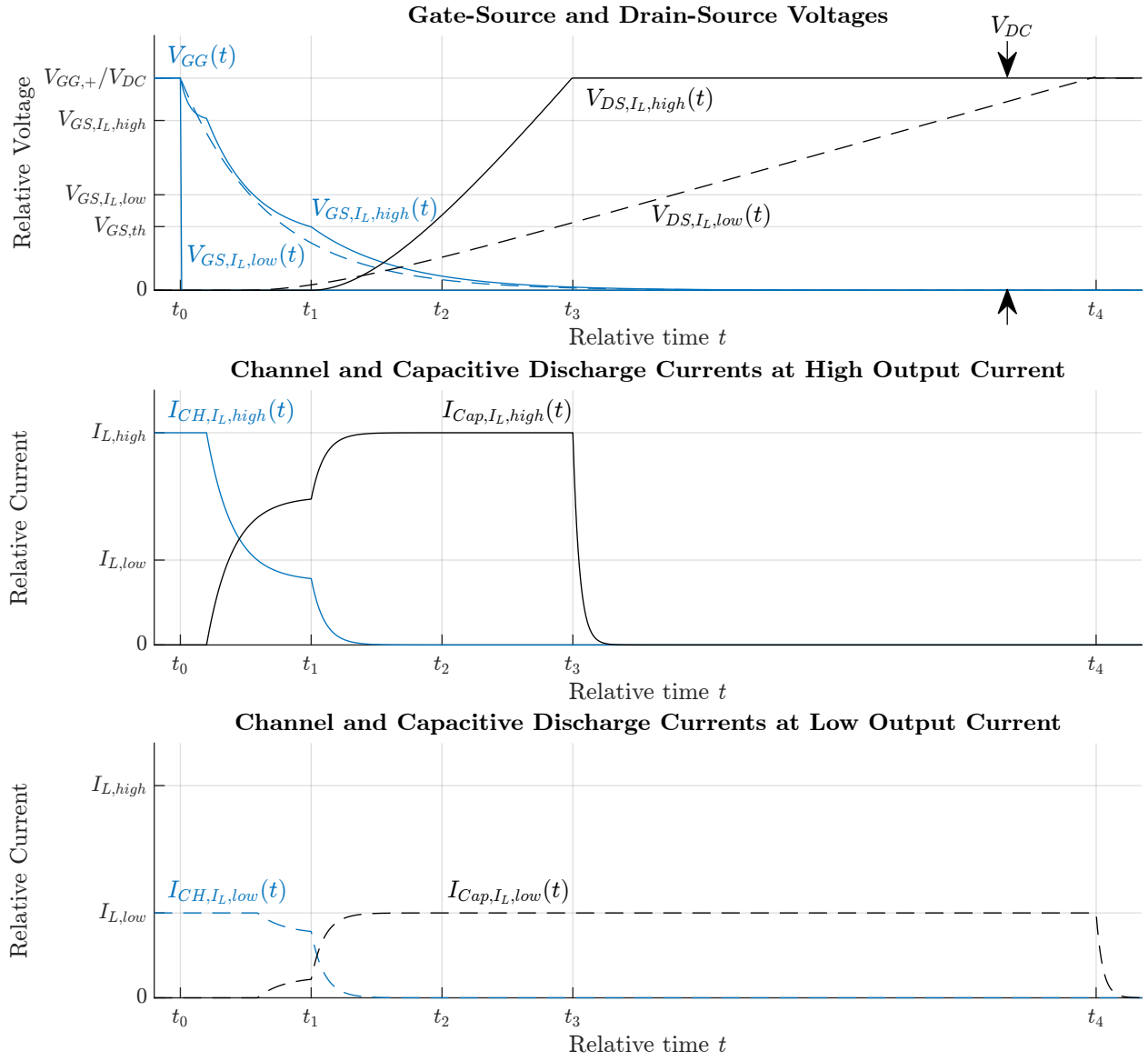


Figure 5.12: Switching transients during turn-off of HS MOSFET.

As the LS diode remains reverse biased and the load current I_L is assumed to be constant, the reduction in the HS MOSFET channel current will need to be taken over by the capacitive charge and discharge currents, I_{Cap}, to maintain the load current such that $I_{CH} + I_{Cap} = I_L$. As the discharging current of $C_{GD,HS}$ is conducting through the gate resistor of the HS MOSFET, the discharging current will cause a voltage drop across the gate resistor. This voltage drop results in the gate-source voltage of the HS MOSFET not decaying to zero but rather to whichever voltage is present across the gate resistor, which results in the second distinct exponential decay until time t_1. At time t_1, the gate-source voltage reaches the threshold voltage and the HS MOSFET channel current cuts off rapidly. All the load current is now supplied from the charging and discharging of the capacitances until time t_3 where the drain-source voltage of the HS MOSFET has to build up to the full DC-link voltage and the LS diode becomes forward biased and takes over the load current, which concludes the switching transient for the HS MOSFET.

At a low load current, the process governing the turn-off is similar to what is described above. However, the low load current means that it takes longer for the charge to build up across the parasitic capacitances of the HS MOSFET. As the discharging current from $C_{GD,HS}$ is now significantly less than in the case above, the resulting voltage drop across the gate resistor will be negligible, and therefore, the discharging of the gate-source voltage will present itself as one single exponential decay towards zero. The HS MOSFET is moving through the Ohmic region of the I/V curves until its gate-source voltage reaches $V_{GS,I_L,low}$ at which its channel current begins to decrease until the threshold voltage is reached at time t_1. Here, the channel current shuts off and the load current is now only supplied by the capacitive discharge currents. As the load current $I_{L,low}$ is only a fraction of $I_{L,high}$, the accumulation of necessary charge for the drain-source voltage of the HS MOSFET to reach the DC-link voltage takes significantly longer and the HS MOSFET turn-off transient does not finalize until time t_4.

In the case of a very low load current, a situation can occur in which the time needed to charge the parasitic capacitances of the HS MOSFET is less than the dead time before the LS MOSFET is commanded to turn-on, i.e $t_4 < t_d$. In this case, when the LS MOSFET turns on, it will supply the charging current for the capacitances of the HS MOSFET, and therefore, the voltage across the HS MOSFET will rapidly increase to the DC-link voltage. As the channel current of the HS MOSFET is already off, this does not cause any shoot-through of the DC-link, however, care should be taken, as the rapid increase in charging current of $C_{GD,HS}$ could cause the voltage drop across the HS MOSFET gate resistor to be high enough that the HS MOSFET experiences a false turn-on.

Measured Dead Time Voltage Error

If the load current dependency of the voltage error was to be determined analytically, this would require a very detailed model of the MOSFETs and their gate driver circuitry, including the non-linear behavior of the parasitic capacitances. Therefore, it was deemed more convenient to measure the converter output voltages and gate signals in order to determine the actual dead time voltage error introduced at different current levels. This will allow for the development of a more suitable compensation algorithm, which takes into account the load current dependency on the dead time voltage error.

The measurement of the dead time voltage error has been done by measuring the applied gate signals and comparing them to the actual output voltage waveforms for different magnitudes of load current. The gate-source voltage is measured at the output of the gate driver circuitry for the HS MOSFET by use of an insulated high voltage probe equipped with a x20 probe tip (LeCroy HVFO130-x20 [31]). The actual turn-on transient of the output voltage of the power module is measured with a high voltage differential probe (LeCroy HVD3605A [32]). Refer to Fig. 2.4 for a photograph of the power module in which the measured voltages are indicated. The measurements are made with a DC-link voltage of 3 kV and the resulting waveforms are plotted for a load current of approx. 10 A in Fig. 5.13 and 0.5 A in Fig. 5.14 for a turn-on and turn-off transient, respectively.

The dead time is implemented as a turn-on delay of $2\mu s$, and therefore, the HS MOSFET gate signal turns on with a delay compared to the ideal voltage reference from the PWM modulator. The ideal voltage output is plotted as a square wave voltage that goes high 2μs before the gate signal is applied. The dead time voltage error for a turn-on transient is calculated as the area between the ideal and actual output voltage shown in the figure. For the turn-off transient, there is no delay for the HS MOSFET gate signal, and therefore, the ideal voltage follows the turn-off of the HS MOSFET gate signal more closely. The total dead time voltage error introduced is found by summing the negative voltage error introduced during the turn-on transient with the positive voltage error introduced during the turn-off transient.

The results in Fig. 5.13 and 5.14 show how the voltage waveforms for the turn-off transient differ significantly for the two current levels. The output voltage decay has been slowed significantly at 0.5 A compared to the case of 10 A and shows a slow gradual decay until chopped by the turn-on of the LS MOSFET at approx. 2μs.

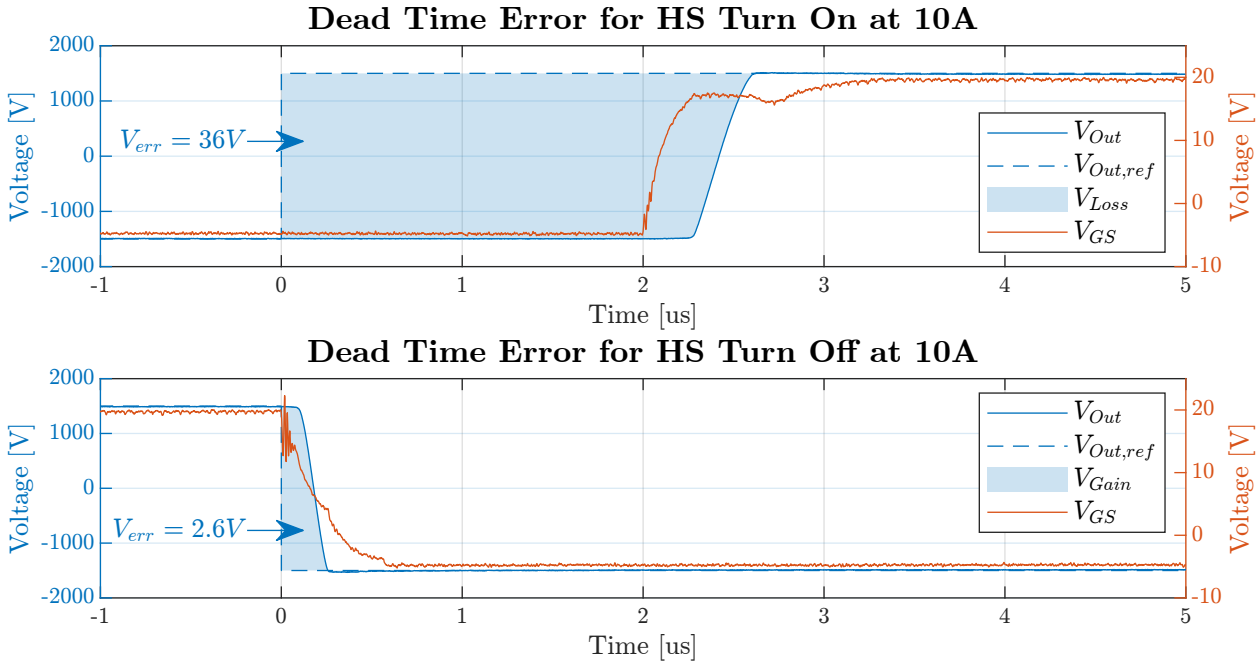


Figure 5.13: Measurement of dead time voltage error at positive 10 A load current.

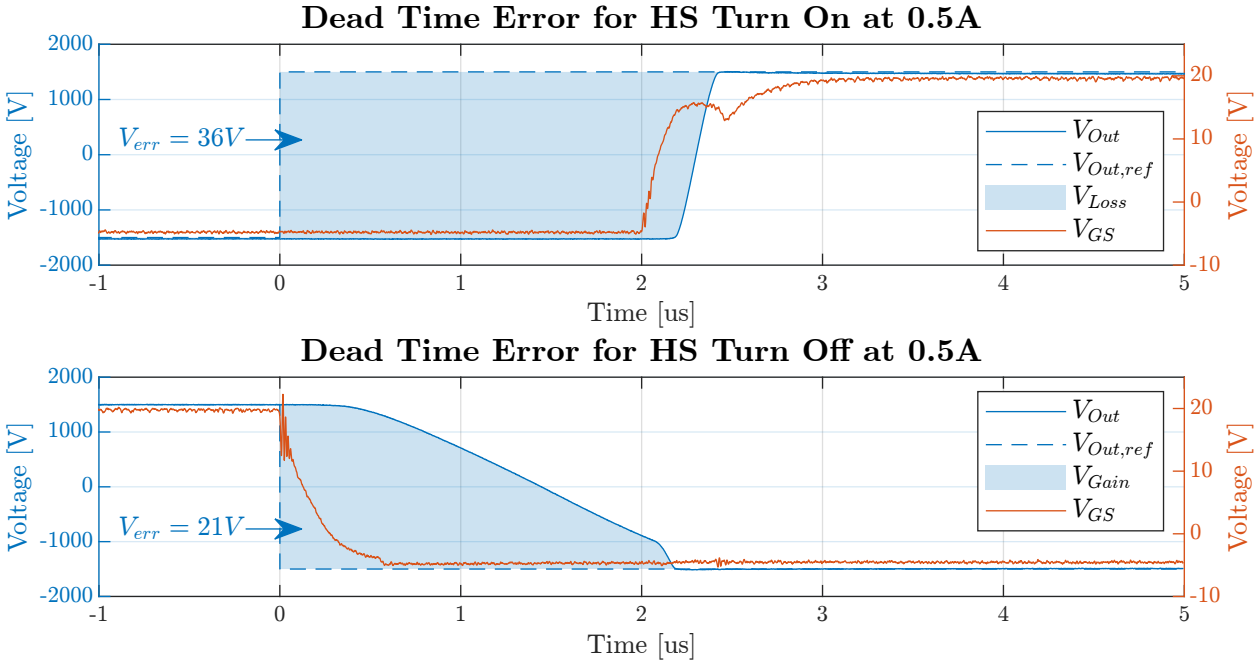


Figure 5.14: Measurement of dead time voltage error at positve 0.5 A load current.

In Fig. 5.15, all of the measured turn-on and turn-off transients for positive load currents are plotted together to illustrate the non-linearity of the relationship between the dead time voltage error and load current magnitude. Here, it can be seen that the turn-on transients only changes slightly with the load current as was presented in the previous analysis. For the turn-off transients, the output voltage is highly dependent on the magnitude of the load current with turn-off times gradually decreasing in the range from 10 A to 2 A and then rapidly decreasing for load currents below 2 A.

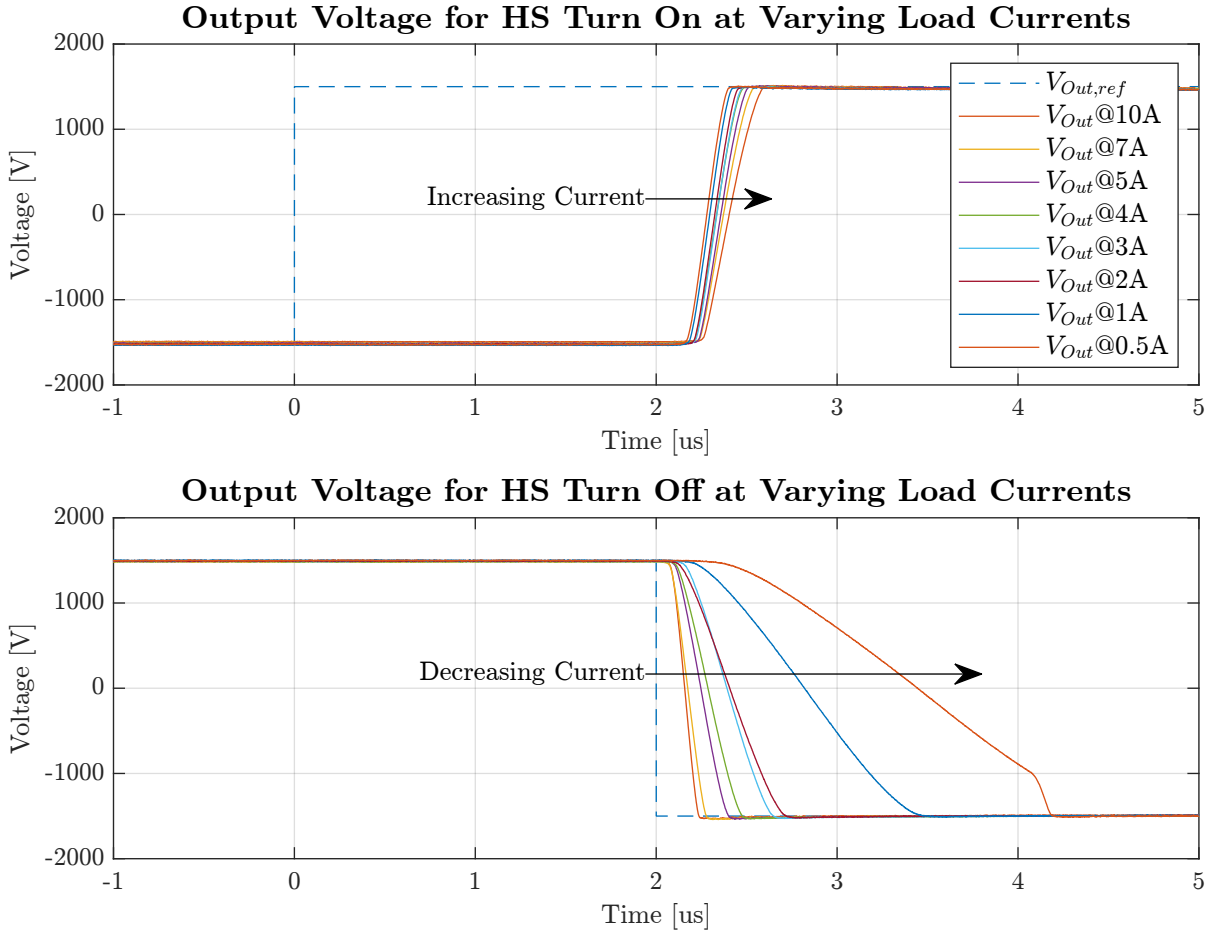


Figure 5.15: Change in output voltage transients for varying magnitudes of load current.

The resulting dead time voltage errors have been plotted as a function of their respective load currents as shown in Fig. 5.16. Also included in the figure is the initial dead time compensation algorithm along with the new fitted dead time compensation algorithm. The fitted dead time compensation algorithm has been made with a simple linear approximation with a slope of 15 V/A that is set to saturate at the expected value of dead time voltage error for ideal switching transients, which in the case of 3 kV DC-link voltage and 2μs dead time is $\pm$30 V using (5.3). This simple linear approximation was chosen for ease of implementation in the DSP to keep down the computational resources. A piece-wise linear approximation or a more sophisticated curve fitting tool could have been used, but the simple approach presented here has shown good performance in the experimental setup.
The introduction of a sloping compensation voltage around zero current has also meant that the issues associated with instability of the initial dead time compensation algorithm at low current references have disappeared. The sloping nature of the fitted dead time compensation algorithm prevents any step changes in the compensation voltage and thereby eliminates the regular current jumps.

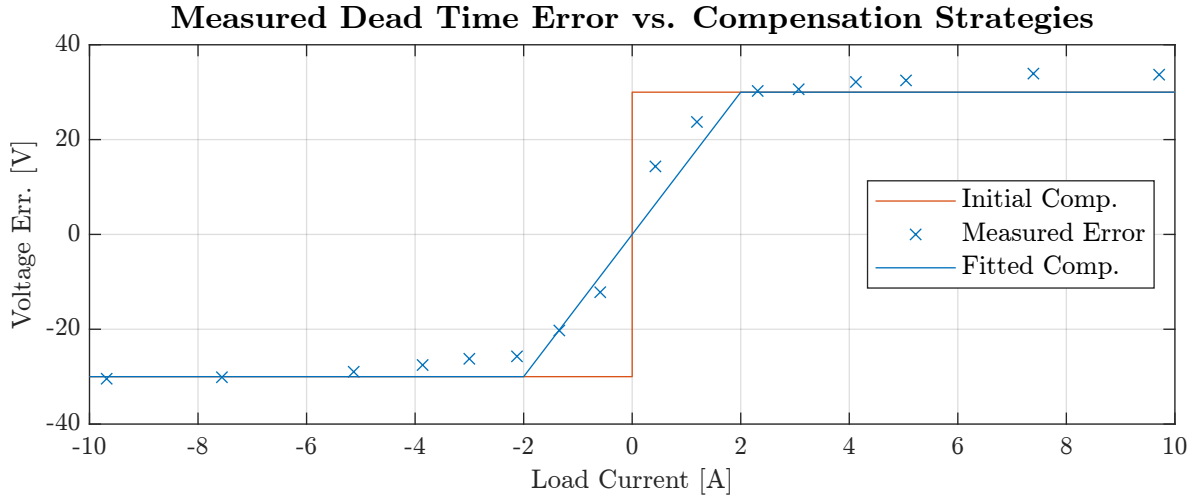


Figure 5.16: Measured dead time voltage error for varying load currents plotted along with the initial and fitted dead time compensation algorithm.

5.2.3 Final Evaluation of Dead Time Compensation Algorithm at 6 kV

As explained in Section 3.3, all results were initially produced with a capped DC-link voltage of 3 kV. In the late stages of the thesis work, it was achieved to raise the voltage to 6 kV, and therefore, a reevaluation of the performance of the current controllers and dead time compensation was made at this voltage level. The results presented here serve as part of that reevaluation.

During the final tests conducted at the rated DC-link voltage of 6 kV, it was desired to measure if the increase in DC-link voltage would impose any significant difference in the voltage error introduced by the dead time. Therefore, a new series of measurements were taken at this voltage and plotted along with the results taken at 3 kV as shown in Fig. 5.17. The results are normalized with respect to the expected dead time voltage error for ideal waveforms at their respective DC-link voltages using (5.3).

Even though it is possible to see a slight change in the normalized dead time voltage errors after increasing the DC-link voltage, the results are still within reasonable proximity of the fitted dead time compensation algorithm made at a DC-link voltage of 3 kV.

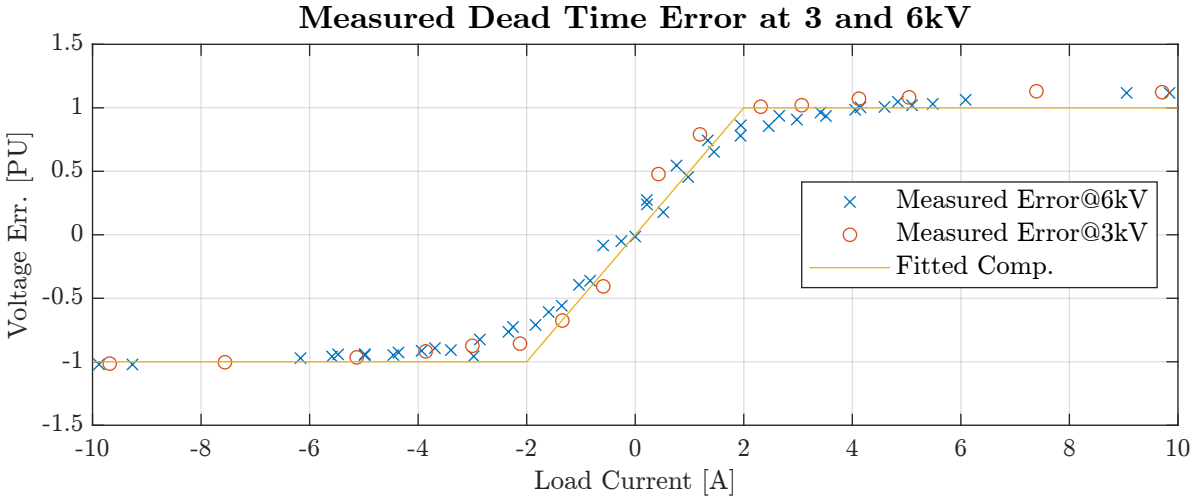


Figure 5.17: Normalized measured dead time voltage errors for 3 kV and 6 kV plotted along with the fitted compensation algorithm made at 3 kV.

5.3 Closed Loop Control

This section describes the implementation and evaluation for the PI controller designed in [1] as well as for a PR controller derived from the initial PI controller design. The PI controller was initially chosen for the design at a stage in the project where robustness was valued over performance. It is known that a pure PI controller cannot be used to control sinusoidal variables without introducing both magnitude and phase error. However, it was believed that the errors introduced could be quite accurately modeled and easily compensated for. However, as initial test results would show, a significant error was introduced by the converter dead time, which meant that the resulting current errors could no longer easily be compensated, resulting in poor tracking of the reference signals. The effect of the dead time voltage error, though predictable in its nature, introduced very significant tracking errors in the controller. Though it was possible to compensate for the dead time voltage by using the compensation algorithms explained presented in Section 5.2, it was desired to investigate the possibilities of implementing another form of current controller which had a better base performance, such that the dependency of a very exact dead time voltage error compensation algorithm could be reduced. It was therefore decided to implement and test a PR controller which is known to be theoretically able to perform sinusoidal current control with neither amplitude nor phase error. As the PR controller is specifically tuned to obtain good tracking at the fundamental frequency, it is expected to be much better at rejecting the disturbance caused by the dead time voltage error. A detailed description of the implementation of these controllers and their results are given in the following sections.

Input current references for the closed loop controllers are given as a peak magnitude and a phase angle with respect to the phase angle of the open loop reference voltage applied to the receiving converter. The reader should be notified that both references in magnitude and phase are imposed with rate limiters which should be considered when inspecting the waveforms shown for the transient responses of the controllers. The rate limit for the reference current magnitude is 2.5 A pr. fundamental 50 Hz period or equivalent to four fundamental periods for the maximum step change in current amplitude of 10 A. The rate limiter used for the phase reference is 36 degrees pr. fundamental period or equivalent to ten fundamental periods for a maximum step change of 360 degrees.

5.3.1 PI Controller

The PI controller is parameterized with a K_P of 40 and K_I of 467 to achieve a desired rise time of 3 ms as analyzed in the previous semester's project [1]. The used structure of the PI controller is the standard form using saturation and anti windup as shown in Fig. 5.18. To discretize the PI controller, the integrator is implemented using the backward Euler method. Refer to Appendix A for a detailed description of the digital implementation.

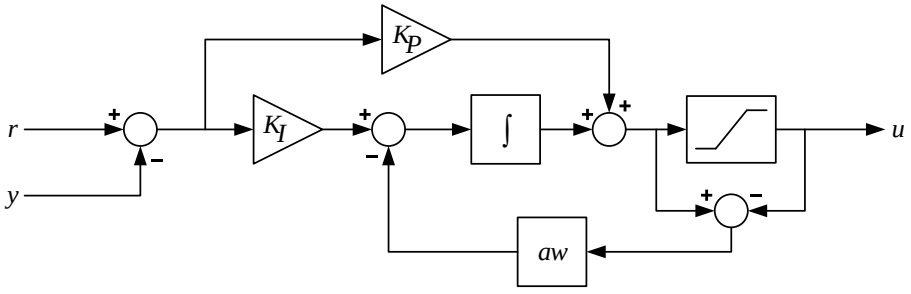


Figure 5.18: Structure of continuous PI current controller.

For the sake of completeness, the bode plot of the PI controller from [1] is presented here again as shown in Fig. 5.19. Included in the figure is the bode plot for the continuous and discrete implementation of the PI controller.

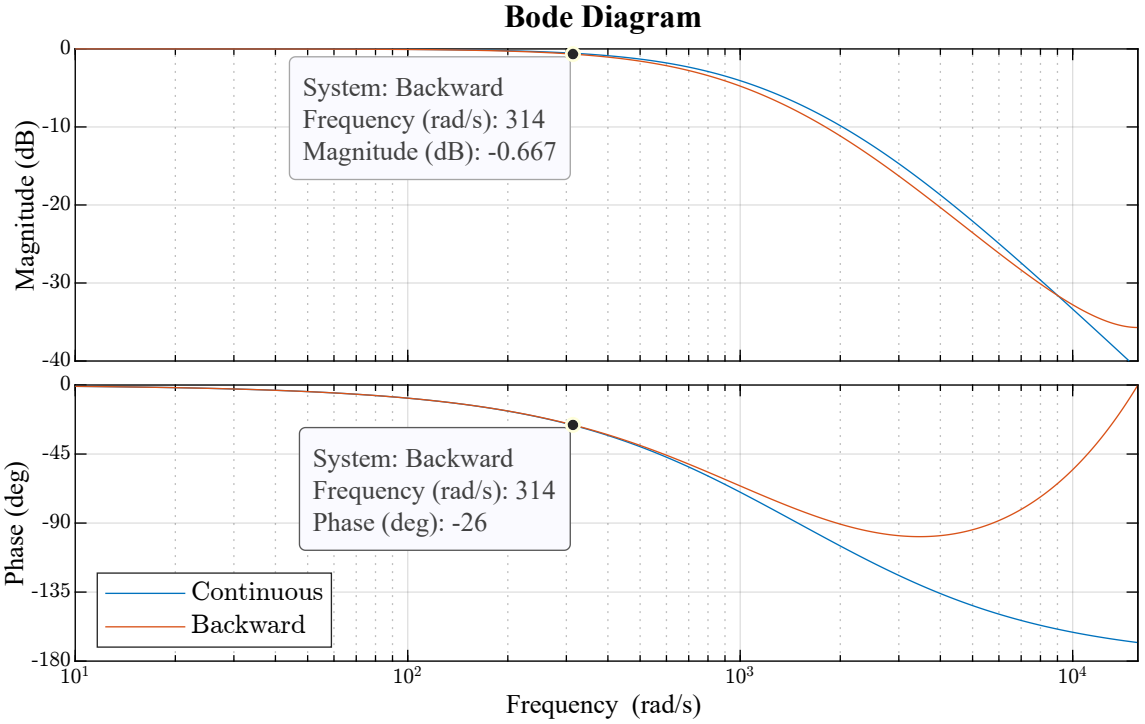


Figure 5.19: Bode plot of PI controller (314 rad/s = 50 Hz) [1].

The success criteria for the measured results with the PI controller is to have the measured waveforms as close as possible to what can be derived from the theoretical gain and phase extracted from the closed loop bode plot of the designed PI controller as shown in Fig. 5.19. That is, measured results should have a gain of -0.667 dB $\approx$ 0.93 and a phase of -26 degrees.

The performance of the PI controller has been evaluated without any dead time compensation at DC-link voltages below 3 kV and with current references from 0 to 10 A. The evaluation includes the rate limited transient response and the steady state performance in two separate figures. The effect of adding dead time compensation to the control loop has been evaluated for the steady state performance of the PI controller at a DC-link voltage of 3 kV and a current reference of 1 and 10 A. Both of the dead time compensation algorithms described in Section 5.2 are implemented and their results are compared.

Without Dead Time Compensation

The performance of the PI controller is first evaluated without adding the dead time compensation to the control loop for both low and high values of reference currents. The transient response of the PI controller with a current reference of 1 A is shown in Fig. 5.20 and the steady state performance is shown in Fig. 5.21. The figure showing the steady state performance also includes the theoretical gain and phase reduction of the PI controller plotted as a dashed line.

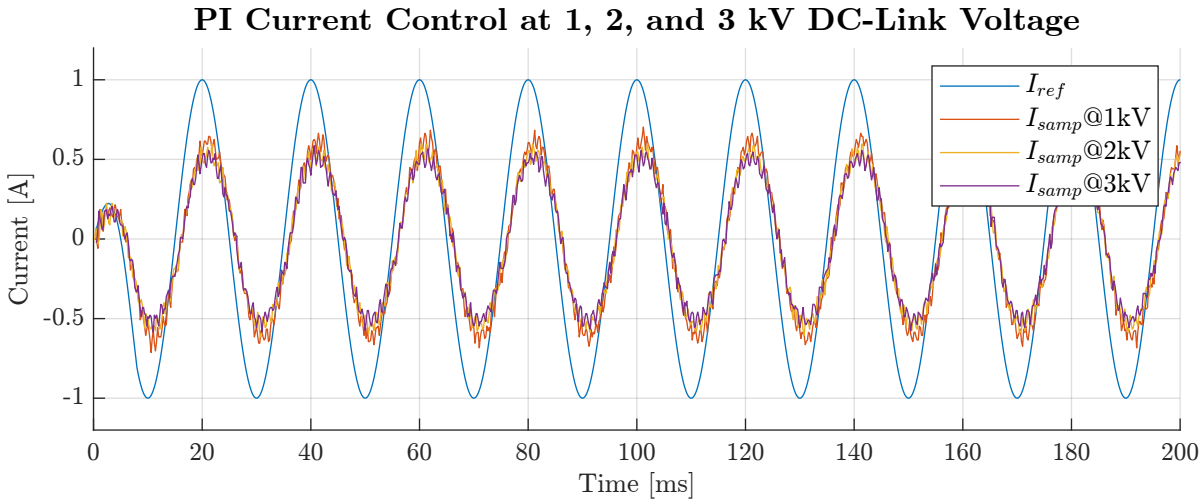


Figure 5.20: PI controller - Transient response of sampled load current at 1 A reference.

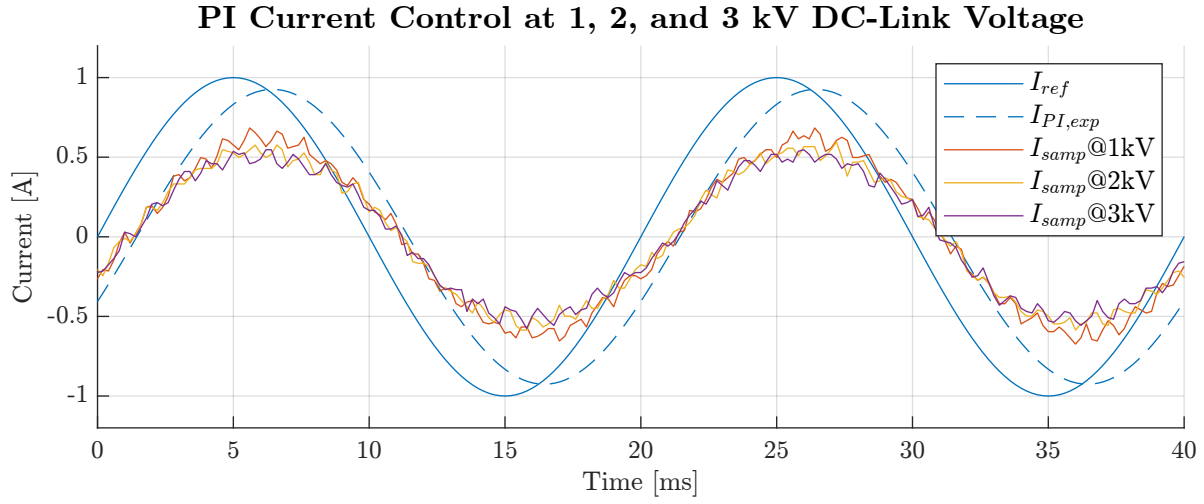


Figure 5.21: PI controller - Steady state response of sampled load current at 1 A reference.

From the above figures, it can be seen that the transient response is well controlled by the PI controller and shows no sign of instability, but the steady state performance is unsatisfactory. Though the phase delay of approximately 26 degrees is as expected, the current amplitudes are very low ranging between 0.5 A and 0.6 A compared to the expected 0.93 A. It can be noted that the magnitude error increases with increasing DC-link voltage, which suggests that this could be highly influenced by the dead time voltage error.

Next, the controller performance is evaluated with a current reference of 10 A. The transient response is shown in Fig. 5.22 and the steady state performance is shown in Fig. 5.23.

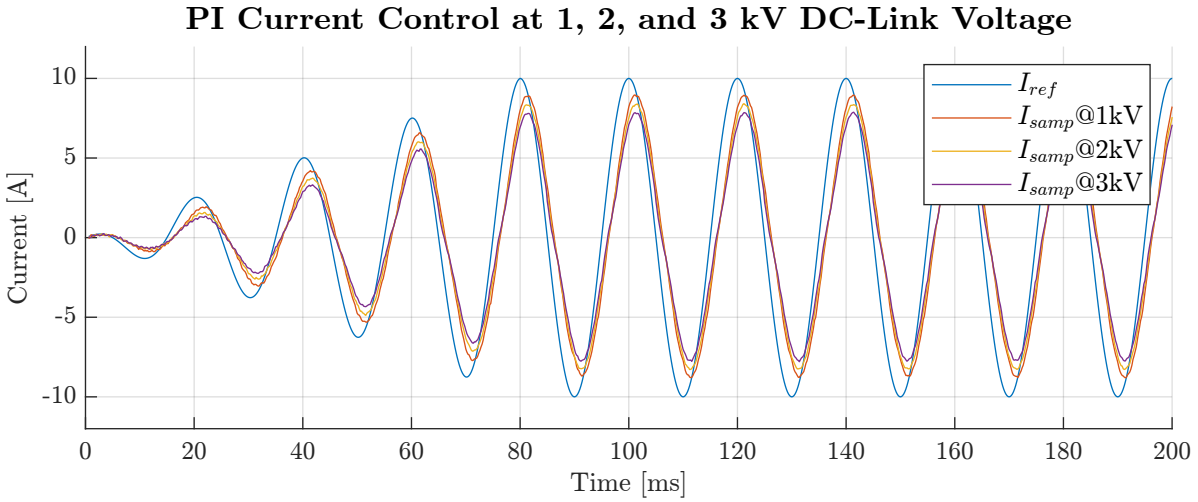


Figure 5.22: PI controller - Transient response of sampled load current at 10 A reference.

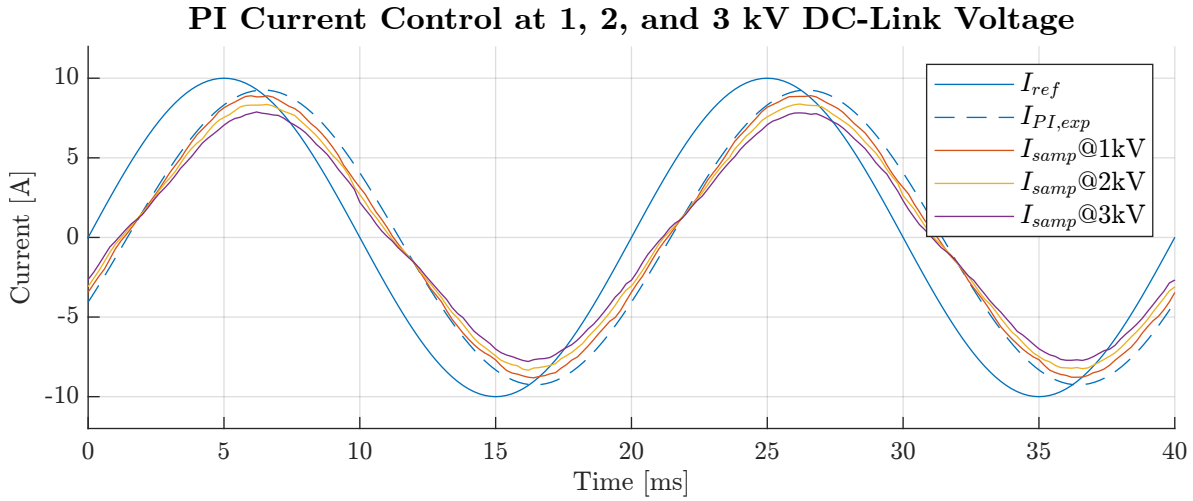


Figure 5.23: PI controller - Steady state response of sampled load current at 10 A reference.

As was the case for the low current reference of 1 A presented above, a stable transient response can be noted along with a significant steady state error. The transient response is prolonged to four fundamental periods due to the rate limiter imposed on the reference signal. As the current reference has increased to 10 A, the SNR has increased significantly, which results in the current waveform looking less noisy. The current amplitudes are noted to have magnitudes ranging between 7.5 A and 9 A compared to an expected 9.3 A, while the phase delay remains unchanged with a value of approx. 26 degrees. Similar to what was seen in the previous case with a current reference of 1 A, it can be seen that the attenuation of the currents increases with DC-link voltage. However, in this case, the relative error is much less than in the case with a 1 A reference. This is to be expected as the dead time voltage error does not increase substantially with the increased current, however, the controller output voltage increases by a factor of ten, and therefore, the relative voltage error is reduced. Still, the additional magnitude error caused at 3 kV is significant and needs to be addressed.

With Dead Time Compensation

The performance of the PI controller with added dead time compensation to the control loop has been evaluated for a current reference of 1 A where the transient response is shown in Fig. 5.24 and the steady state response in Fig. 5.25. The figure showing the steady state performance also includes the theoretical gain and phase reduction of the PI controller plotted as a dashed line.

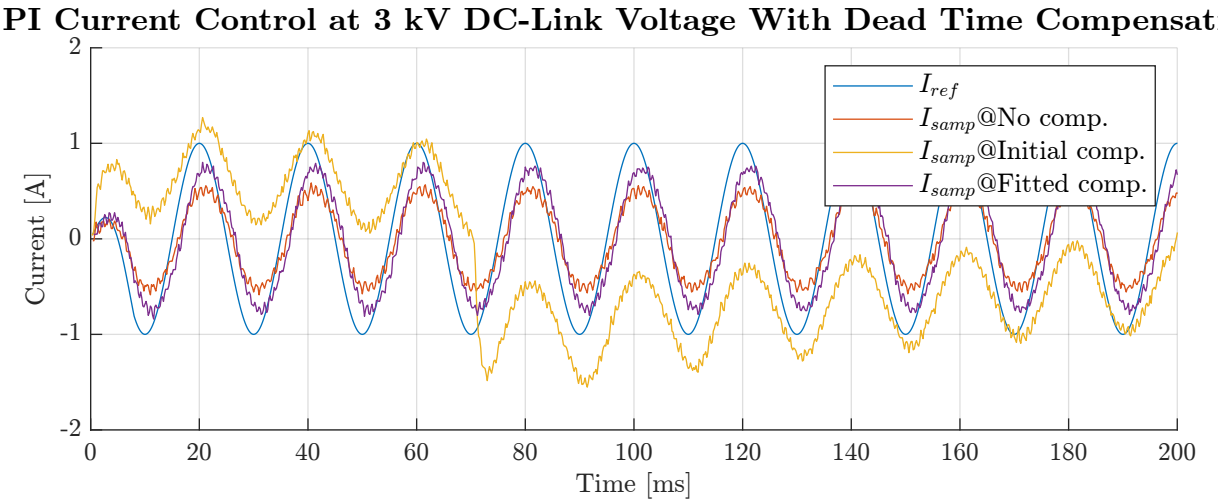


Figure 5.24: PI controller with compensation - Transient response of sampled load current at 1 A reference.

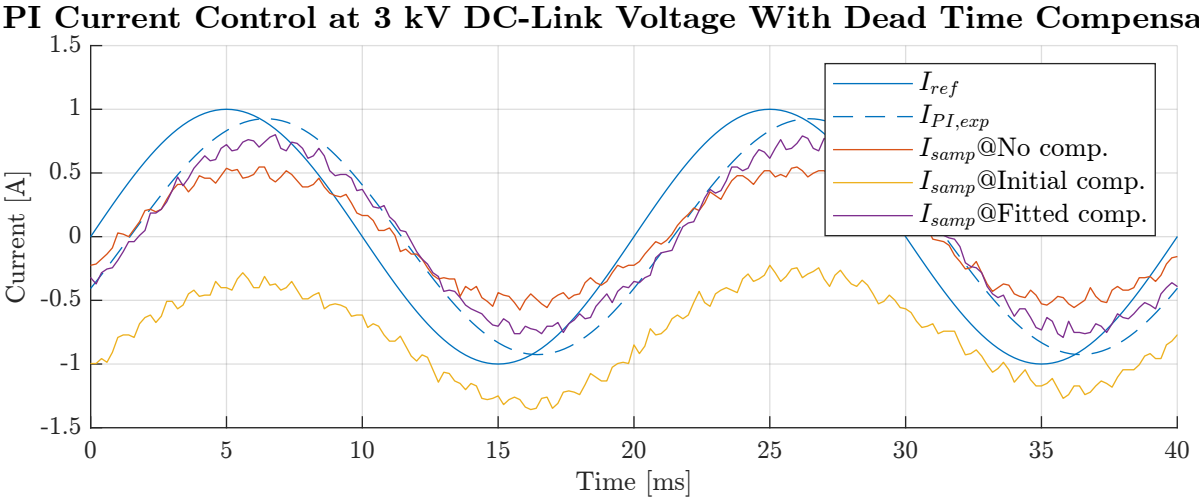


Figure 5.25: PI controller with compensation - Steady state response of sampled load current at 1 A reference.

For the simplified constant term dead time compensation of 2μs, the instability issue introduced in Section 5.2 clearly manifests itself and results in very bad reference current tracking. The fitted dead time compensation algorithm can be seen to eliminate some but not all of the magnitude error and still leaves some 20% unaccounted for. This is likely due to the fact that the fitted dead time compensation is in fact underestimating the dead time voltage error at low current levels as seen if Fig. 5.16. This could likely be improved by making a more advanced and accurate fit.

The effect of adding dead time compensation on the steady state performance of the PI controller at a DC-link voltage of 3 kV and with a current reference of 10 A is shown in Fig. 5.26.

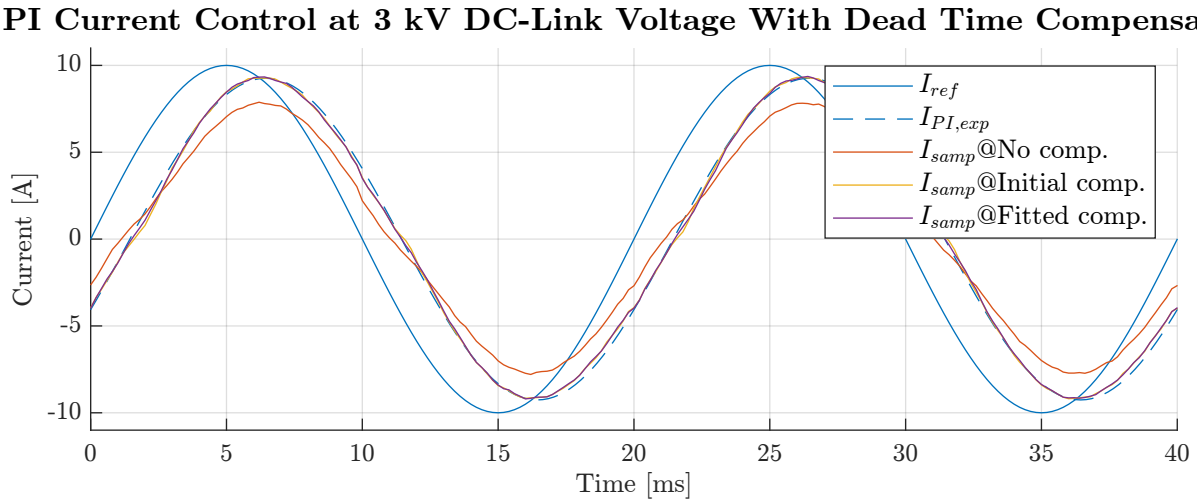


Figure 5.26: PI controller with compensation - Steady state response of sampled load current at 10 A reference.

In this case, the instability issues encountered in the case of a 1 A reference current magnitude are no longer present, and both compensation algorithms show good performance as the measured waveforms are close to the expected one. The dead time compensation can be seen to mainly influence the amplitude and waveshaping properties of the current waveform as the phase angle remains constant with and without compensation.

Another way to look at the controller performance is by inspecting the current error, i.e. the difference between the reference and measured values. This has been done as shown in Fig. 5.27.

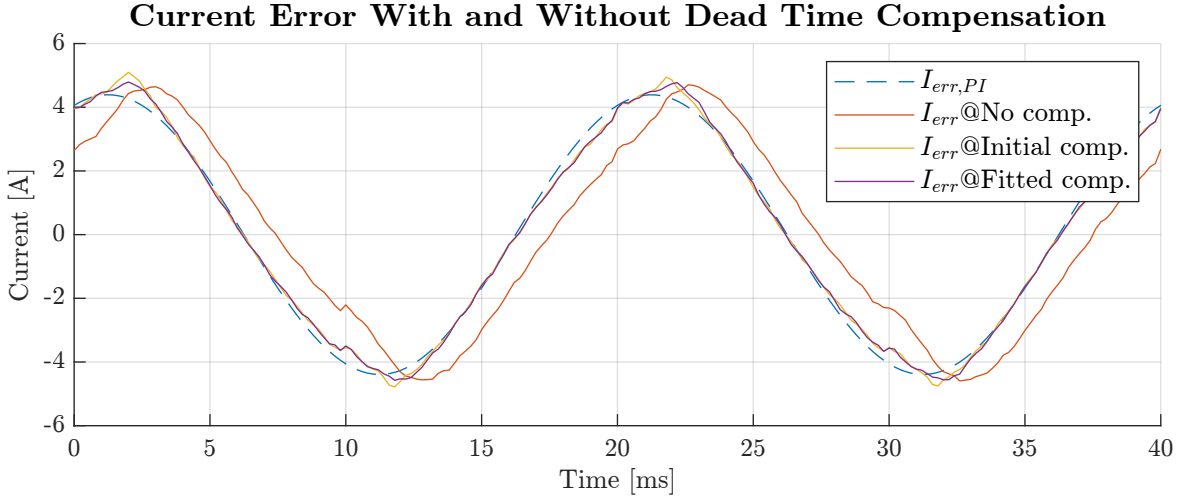


Figure 5.27: PI controller with compensation - Steady state response of sampled load current error at 10 A reference.

From the above figure, it would seem that the current control performance is bad in all cases as the magnitude of the instantaneous current error is rather large. However, it is important to note that when dealing with sinusoidal signals, the *magnitude of the error* does not reflect the *magnitude error*. Rather, the high magnitude of the instantaneous current error arises mostly as a result of the

phase shift between the reference and measured current. In fact, the dashed line shows the expected current error arising from the gain and phase error introduced by the PI controller which is known and can be compensated for. Therefore, it might be more instructive to consider the deviation of the measured current errors from the expected ones. This is done by subtracting the expected error from the measured errors and the results are shown in Fig. 5.28.

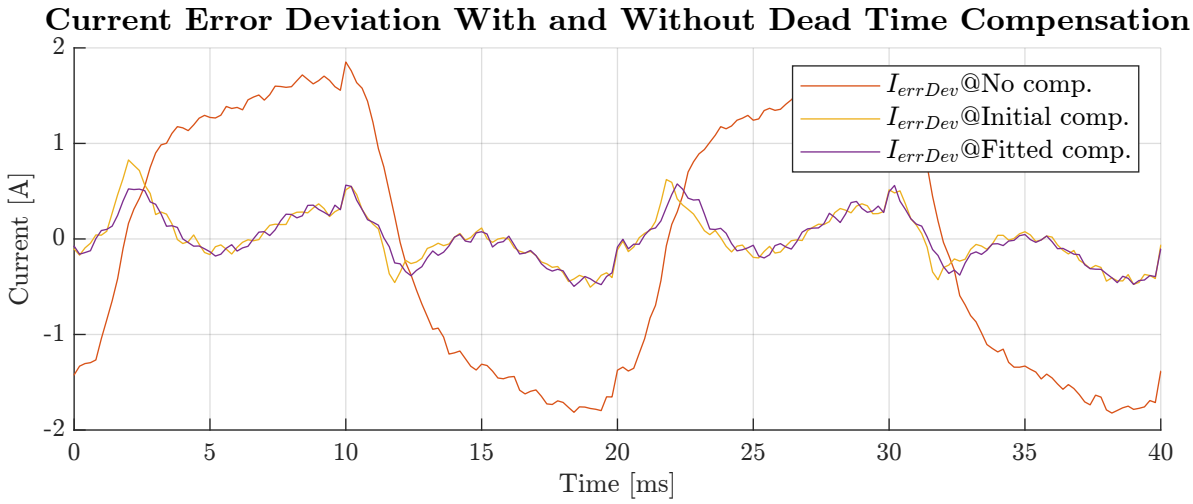


Figure 5.28: PI controller with compensation - Steady state response of sampled load current error deviation at 10 A reference.

Here, it can be seen how the dead time compensation brings a significant reduction to the difference between the measured and expected errors. It would seem from these results that the initial dead time compensation algorithm performs nearly as good as the fitted one, but as it introduces instability issues at low current references as reported in Section 5.2.1, the fitted dead time compensation algorithm will be used onwards.

5.3.2 PR Controller

The PR controller is parameterized with a K_P of 40 and K_I of 2335, being five times larger than the one used for the PI controller to achieve faster dynamic performance. To discretize the PR controller, the resonant term is implemented with its direct integrator discretized using the forward Euler method and its feedback integrator discretized using the backward Euler method. The structure of the PR controller is as shown in Fig. 5.29. A detailed description of the digital implementation can be found in Appendix A.

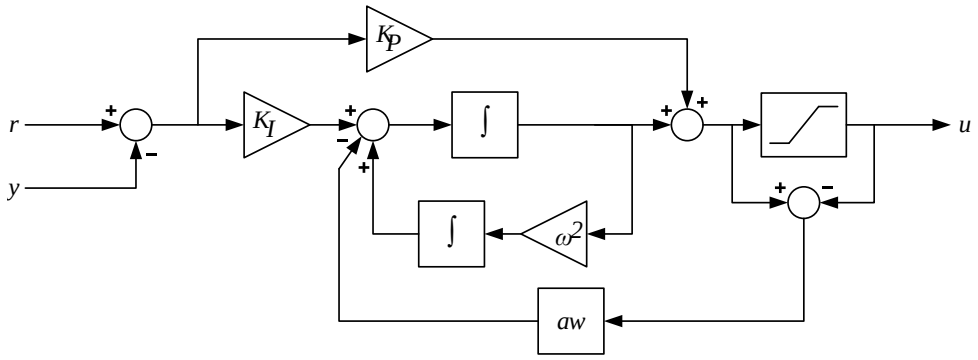


Figure 5.29: Structure of continuous PR current controller.

Further, the bode plot of the PR controller is presented as shown in Fig. 5.30. Included in the figure is the bode plot for the continuous and discrete implementation of the PR controller.

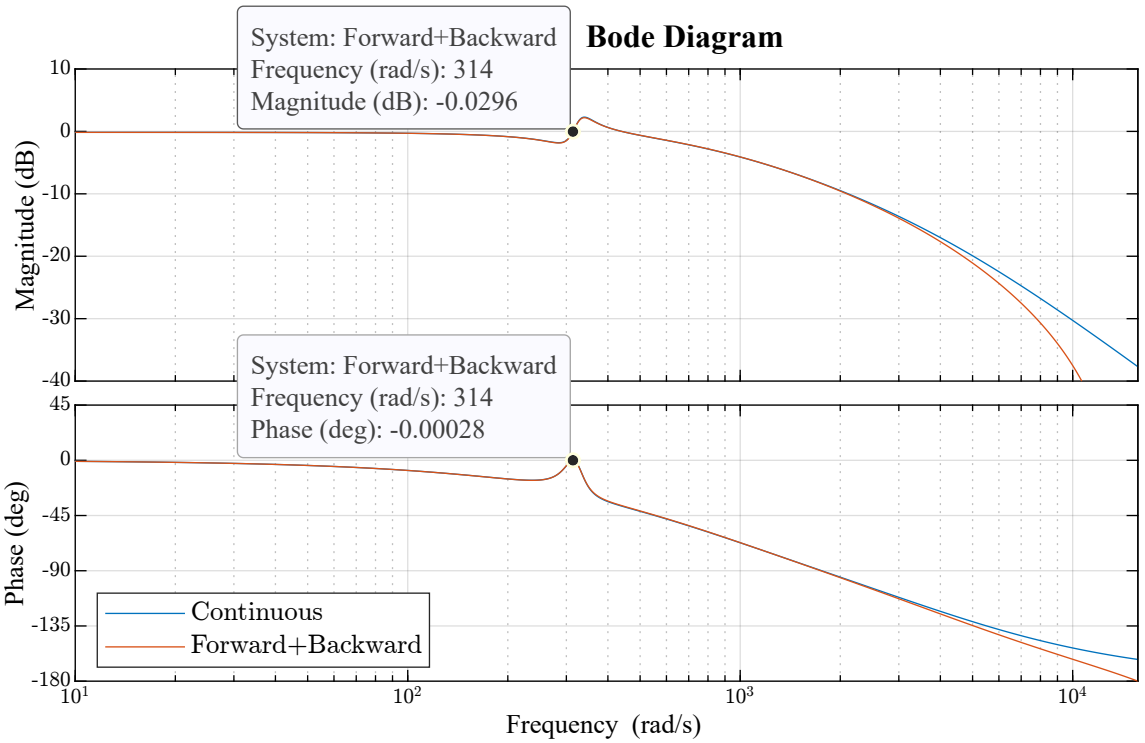


Figure 5.30: Bode plot of PR controller (314 rad/s = 50 Hz).

Similar to the PI controller, the performance of the PR controller has been evaluated with and without dead time compensation at the same test conditions. The performance has been evaluated at different DC-link voltages at and below 3 kV and with current references between 0 and 10 A.

Without Dead Time Compensation

The transient response of the PR controller with a current reference of 1 A is shown in Fig. 5.31, whereas the steady state performance is shown in Fig. 5.32.

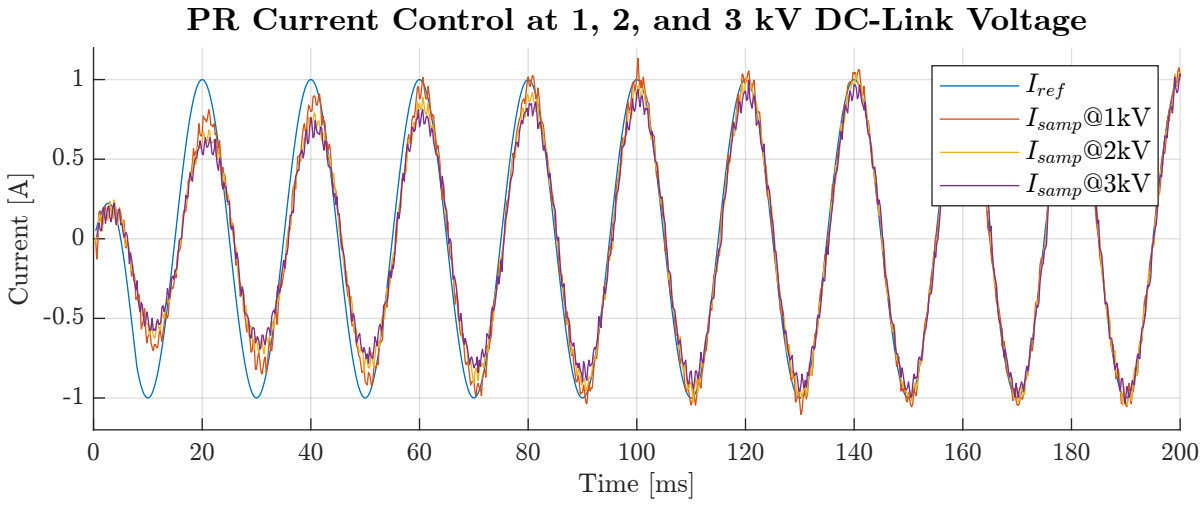


Figure 5.31: PR controller - Transient response of sampled load current at 1 A reference.

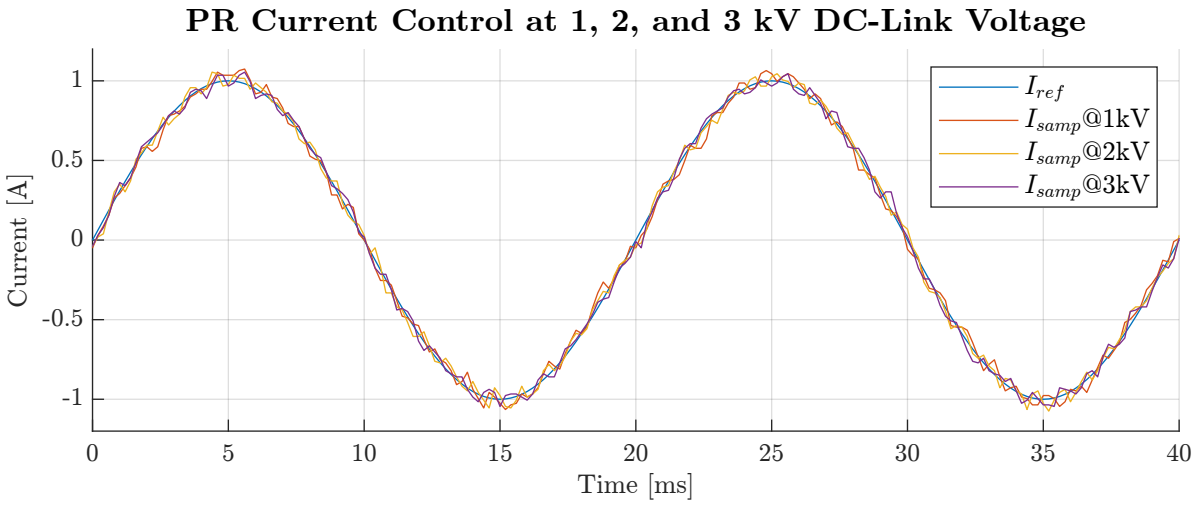


Figure 5.32: PR controller - Steady state response of sampled load current at 1 A reference.

From the above figures, it can be seen that the transient response is well controlled by the PR controller and shows no sign of instability. The steady state performance is found to be significantly improved compared to the PI controller. The current amplitude has no noticeable attenuation or phase delay. Furthermore, the current controller seems to be unaffected by the increasing DC-link voltage and dead time voltage error.

The transient response of the PR controller with a current reference of 10 A is shown in Fig. 5.33, whereas the steady state performance is shown in Fig. 5.34.

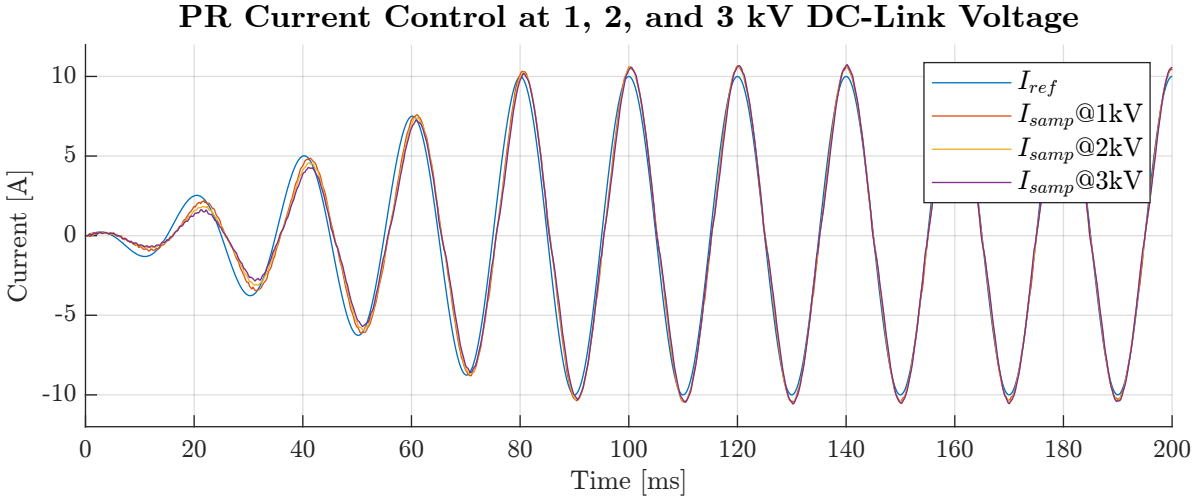


Figure 5.33: PR controller - Transient response of sampled load current at 10 A reference.

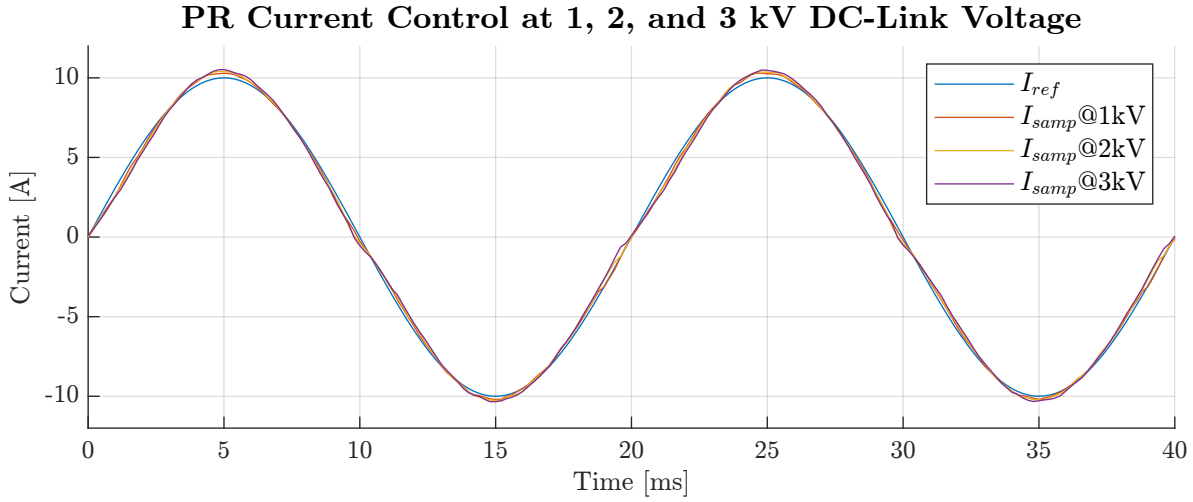


Figure 5.34: PR controller - Steady state response of sampled load current at 10 A reference.

From Fig. 5.33, it could seem that the transient response overshoots slightly after the first four periods, but this is due to a slightly elevated peak current amplitude in steady state as seen in Fig. 5.34. This overshoot can be explained by the inherent working principle of the PR controller. As the PR controller is tuned to control the 50 Hz component of the current to follow its reference, the slight attenuation of measured currents seen around the zero crossings will result in the PR controller increasing the 50 Hz component of its output voltage. This increase does not solve the waveshaping issues associated with the dead time, but merely elevates the magnitude of the entire signal, which results in slightly higher peak amplitude. However, as it will be shown later, the RMS value of the controlled currents has little to no error for the PR controller.

With Dead Time Compensation

The effect of adding dead time compensation to the control loop on the steady state performance of the PR controller at a DC-link voltage of 3 kV and a current reference of 10 A is shown in Fig. 5.35.

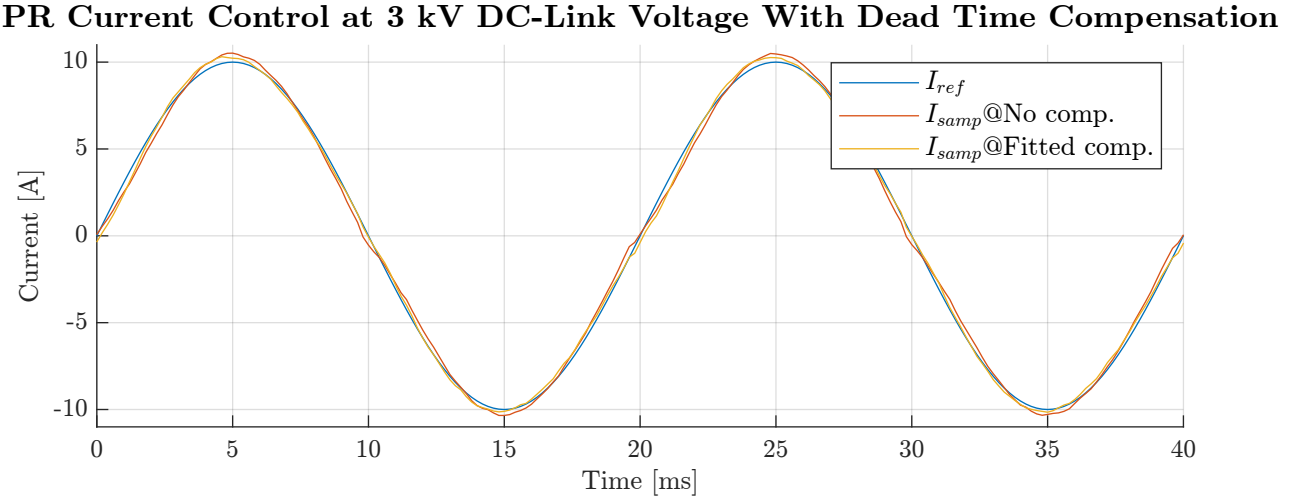


Figure 5.35: PR controller with compensation - Steady state response of sampled load current at 10 A reference.

From the figure, it can be seen how the dead time compensation influences the steady state response of the PR controller. In the case of the PI controller, the dead time compensation influenced the amplitude and waveshaping properties of the current waveform, but in this case, the dead time compensation seems to have a very reduced effect. However, it can be seen that the current amplitude is reduced slightly which suggests that the dead time compensation compensates for some, but not all of the voltage error caused by the dead time.

Again, the current error has been calculated to be able to make the comparison shown in Fig. 5.36.

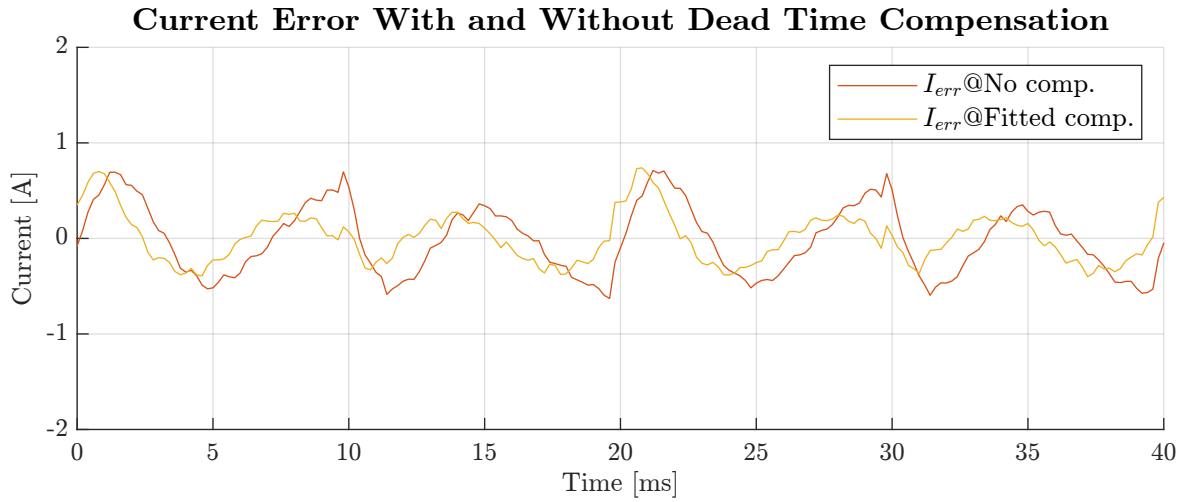


Figure 5.36: PR controller with compensation - Steady response of sampled load current error at 10 A reference.

From the above figure, it can be seen that the instantaneous current error is being phase shifted slightly to the left, but the amplitude is roughly unchanged when comparing with and without compensation.

5.3.3 Comparison of Controller Performance

The comparison of the PI and PR controller performance is based on the results presented in the two previous sections. To make a fair comparison, it is chosen to compare the current error deviation for the PI controller and the instantaneous current error for the PR controller. The comparison is between Fig. 5.28 and 5.36, however, for the sake of completeness, a direct comparison of both controllers with the fitted dead time compensation is shown in Fig. 5.37.

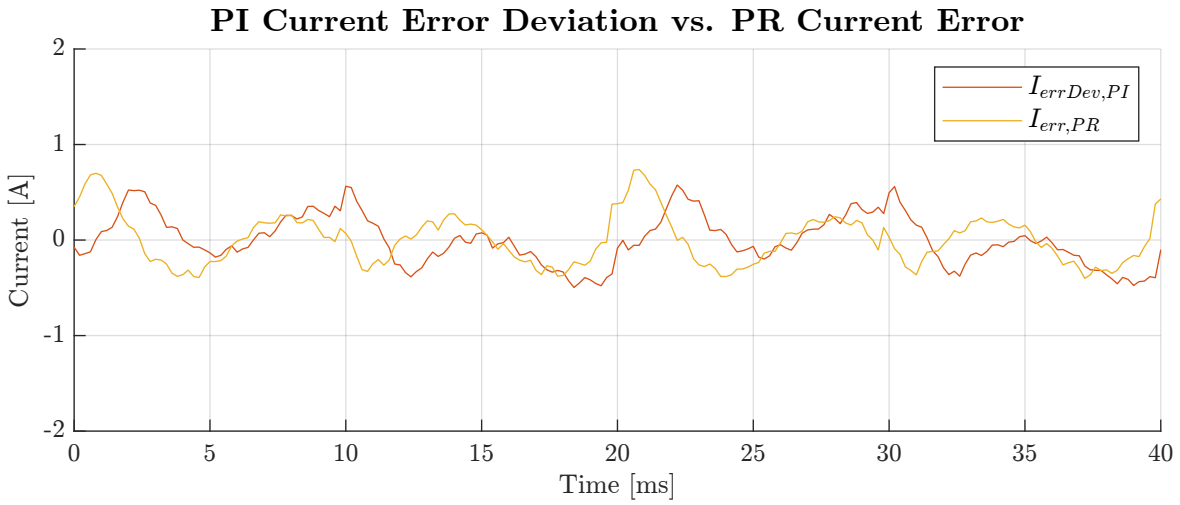


Figure 5.37: Comparison of PI and PR controller performance.

To quantify the time domain comparison, the absolute peak and RMS values of the previously presented currents for both controllers with and without dead time compensation are summarized in Table 5.1. The tabulated values are performed at a DC-link voltage of 3 kV and with a peak current reference of 10 A, and therefore, the presented values are only valid at this operating point. Taking into account the attenuation of 0.93 caused by the PI controller, the expected RMS value is 6.65 A for the PI controller, whereas the expected RMS value for the PR controller is 7.07 A. Further, the table includes measures of the peak and RMS values normalized with respect to the reference.

Table 5.1: Quantification of PI and PR controller performance in time domain. **The dead time compensation introduces instability issues.*

Controller Type	**I_{samp} [A]**	**I_{samp} [A RMS]**	**I_{err} [A RMS]**	**I_{errDev} [A RMS]**	**Norm. Peak**	**Norm. RMS**	**Est. Angle**
PI No comp.	7.84	5.31	2.96	1.34	0.78	0.75	$\angle$ 23°
PI Initial comp.*	9.26	6.44	3.08	0.27	0.93	0.91	$\angle$ 26°
PI Fitted comp.	9.30	6.43	3.07	0.26	0.93	0.91	$\angle$ 26°
PR No comp.	10.5	7.09	0.37	-	1.05	1.00	$\angle$ 0°
PR Fitted comp.	10.2	7.08	0.26	-	1.02	1.00	$\angle$ 0°

From the direct comparison of the controllers' performances in the table, some interesting takeaways can be noticed. First and foremost, the PR controller with the fitted dead time compensation algorithm shows the best performance across the board. The PR controller without dead time compensation follows closely thereafter, being almost similar in its measured RMS value but showing higher deviations in its peak amplitude error. For the PI controller, the results for the uncompensated case are bad. The attenuation of both the peak and RMS current values is much larger than it has been designed for. However, when the fitted dead time compensation is added, both the peak current values and the current phase angle are at the expected values. However, the RMS current is slightly more attenuated. These results suggest that it may be possible to achieve good performance for the PI controller if the known phase and magnitude errors are compensated in the reference signal.

Even though the table above provides valuable insights into the amplitude and phase response of the respective controllers, it is of little use in the quantization of the waveshaping properties of the

controllers. This is better represented in the frequency domain, and therefore, an FFT analysis for the low order harmonic components has been made. The FFT analysis is shown for the first 13 harmonics in Fig. 5.38. Note that the first two plots are absolute values whereas the last plot has been normalized with respect to the amplitude of the first harmonic in the respective cases.

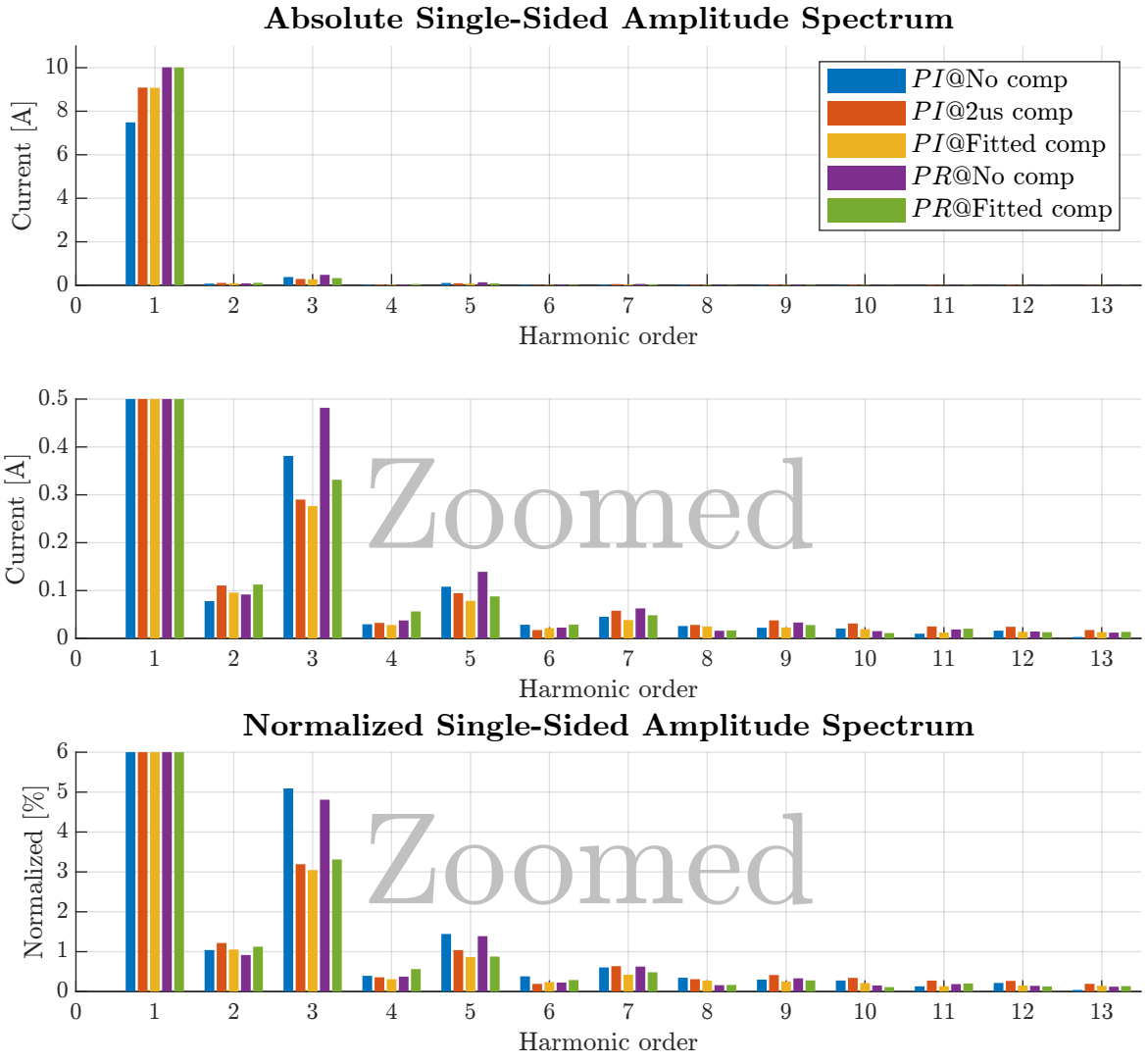


Figure 5.38: Absolute and normalized FFT analysis of PI and PR controller performance.

In Table 5.2, the absolute values for the amplitudes of the selected harmonics are tabulated together. Further, Table 5.3 shows the same harmonic frequencies normalized with respect to their fundamental amplitudes and also shows the THD calculated for the first 50 harmonics.

Table 5.2: Amplitude spectrum of selected harmonic components of the PI and PR controllers' resulting currents.

Controller Type	**1st [A]**	**2nd [A]**	**3rd [A]**	**5th [A]**	**7th [A]**
PI No comp.	7.49	0.08	0.38	0.11	0.05
PI Initial comp.	9.09	0.11	0.29	0.09	0.06
PI Fitted comp.	9.08	0.10	0.28	0.08	0.04
PR No comp.	10.0	0.09	0.48	0.14	0.06
PR Fitted comp.	10.0	0.11	0.33	0.09	0.05

Table 5.3: Normalized amplitude spectrum and total harmonic distortion.

Controller Type	**2nd [%]**	**3rd [%]**	**5th [%]**	**7th [%]**	**THD_{50} [%]**
PI No comp.	1.04	5.09	1.44	0.61	5.51
PI Initial comp.	1.22	3.19	1.04	0.64	3.76
PI Fitted comp.	1.05	3.05	0.87	0.42	3.45
PR No comp.	0.92	4.81	1.39	0.63	5.18
PR Fitted comp.	1.12	3.31	0.88	0.48	3.74

The results from the above comparison in the frequency domain align well with the expectations from the time domain analysis that the PR controller is superior at controlling the fundamental component of the current and tracks it with zero error both with and without dead time compensation. The addition of dead time compensation reduces the harmonic content of the signal, especially for the 3^{rd} and 5^{th} harmonics, and thereby improves the waveshaping properties of the controller.

Interestingly, the amplitude of the first harmonic for the compensated PI controller is only found to be 9.08 and thereby has an attenuation of 0.908 compared to the theoretical attenuation of 0.93 at the fundamental frequency. This suggests that even if the theoretical attenuation was to be compensated in the current reference, the PI controller would still not be able to control the fundamental component without error. Therefore, even though the PI controller with dead time compensation evaluates slightly better in its total harmonic distortion, this is significantly outweighed by the unforeseen reduction of the fundamental component.

Therefore, it is decided to proceed with the PR controller including the fitted dead time compensation for the remaining experiments conducted in this thesis.

5.3.4 Final Evaluation of PR Controller at 6 kV

As explained in Section 3.3, all results were initially produced with a capped DC-link voltage of 3 kV. In the late stages of the thesis work, it was achieved to raise the DC-link voltage to 6 kV, and therefore, a reevaluation of the performance of the PR controller and dead time compensation was made at this voltage level. The results presented here serve as part of that reevaluation.

With all the desired measurements in place at the initial testing plateau of 3 kV DC-link voltage as shown in Section 6.8, efforts were made to try and reach the rated operating point of the power modules being 6 kV DC-link voltage, load current of 7 A RMS, and switching frequency of 5 kHz to evaluate the controller performance at these operating points.

The current controller has been evaluated during operation at 6 kV DC-link voltage and a current reference of 10 A with and without the fitted dead time compensation algorithm. The steady state performance of the PR controller is shown in Fig. 5.39 whereas the instantaneous current error is shown in Fig. 5.40.

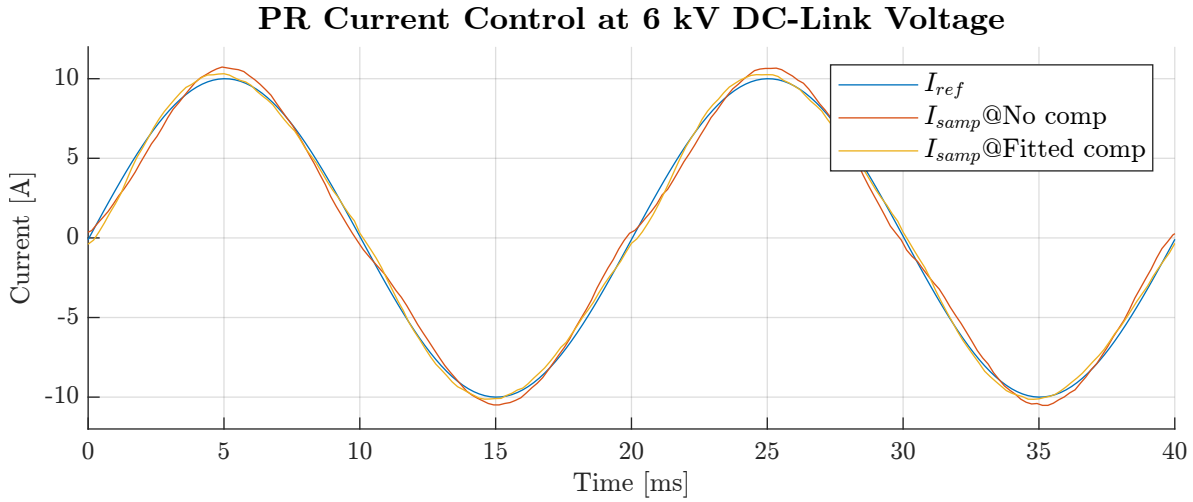


Figure 5.39: Rated operating point - Steady state response of sampled load current.

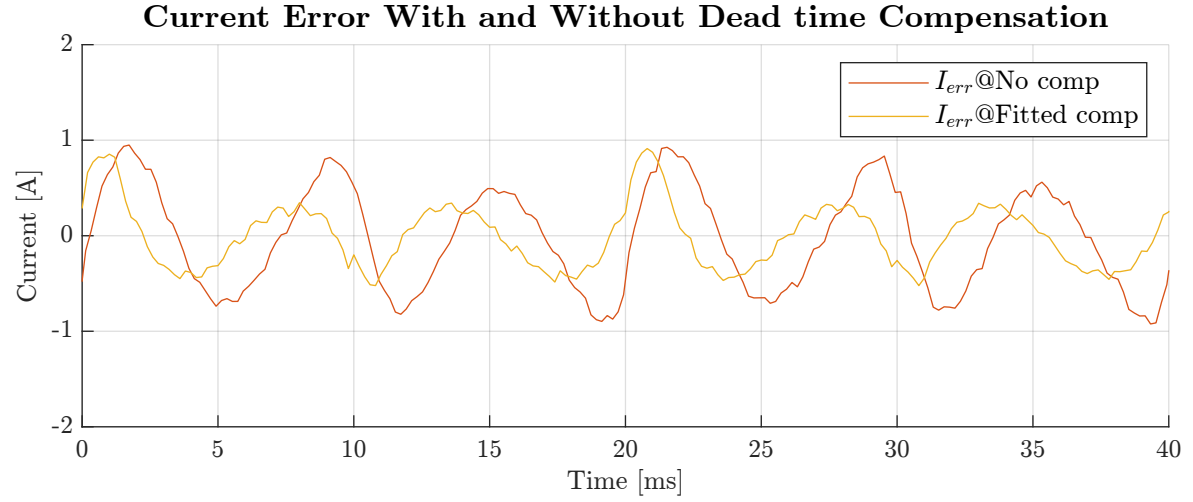


Figure 5.40: Rated operating point - Steady state response of sampled load current error.

From Fig. 5.39 it appears that the waveshaping properties are negatively affected by the increase in DC-link voltage when compared to the results obtained at 3 kV in Fig. 5.34. This goes for the uncompensated as well as the compensated case. This also explains the higher amplitude of the current error seen in Fig. 5.40 when compared to the results obtained for 3 kV in Fig. 5.36.

Further, an FFT analysis of the low order harmonic components in the sampled currents has been performed. The results are presented for the first 13 harmonics in Fig. 5.41. Note that the first two plots are absolute values whereas the last is normalized to its first harmonic.

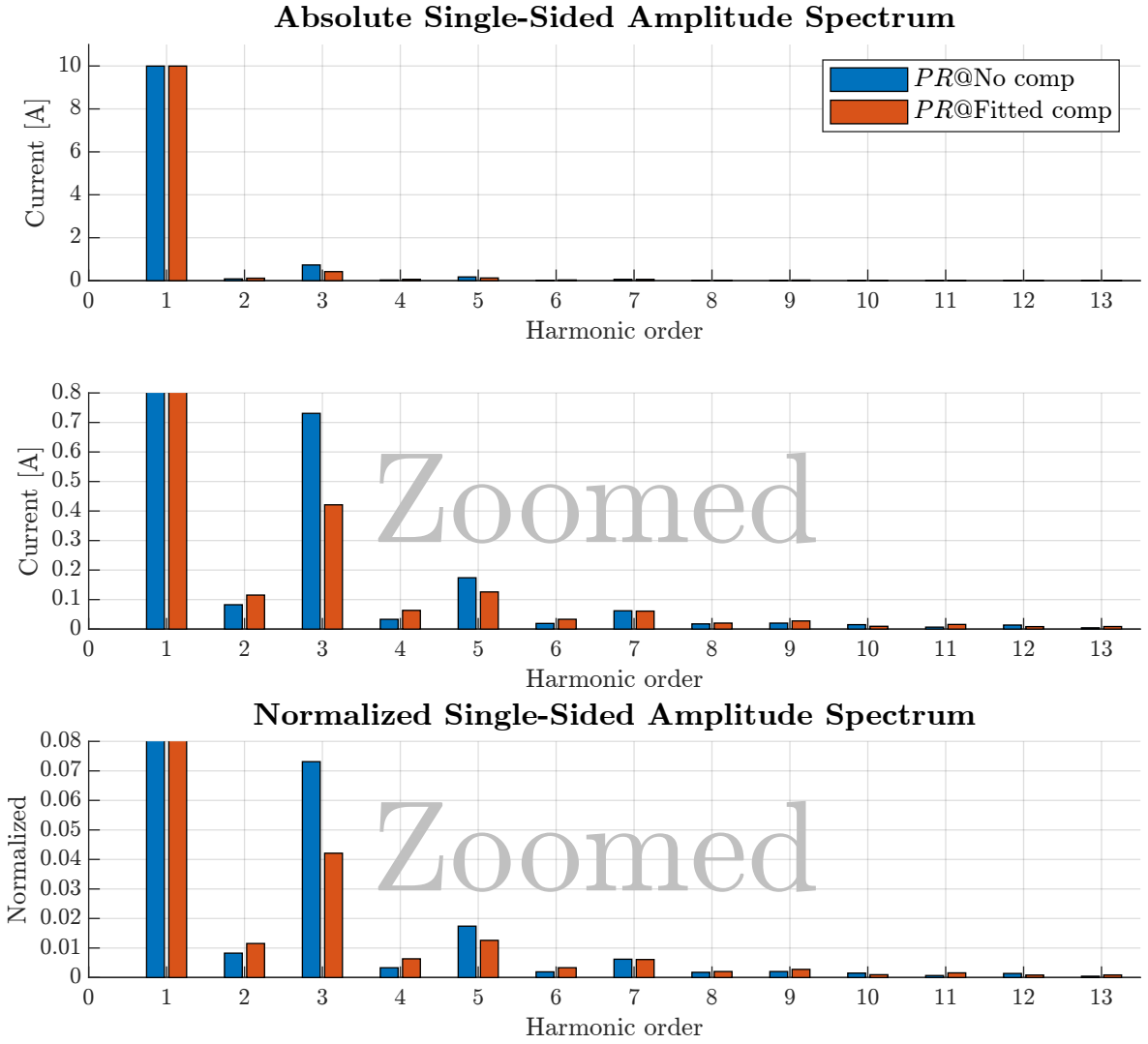


Figure 5.41: Absolute and normalized FFT analysis of PR controller performance at 6 kV.

Selected metrics for both the time domain analysis and the frequency domain analysis for the PR controllers operating at 3 kV and 6 kV DC-link voltages are summarized in Table 5.4.

Table 5.4: Quantification of PI and PR controller performance in time domain. **The dead time compensation introduces instability issues.*

DC-Link Voltage	**Controller Type**	**Rel. Peak**	**Rel. RMS**	**3rd [%]**	**5th [%]**	**THD_{50} [%]**
3 kV	PR No comp.	1.05	1.00	4.81	1.39	5.18
3 kV	PR Fitted comp.	1.02	1.00	3.31	0.88	3.74
6 kV	PR No comp.	1.08	1.00	7.31	1.74	7.61
6 kV	PR Fitted comp.	1.04	1.00	4.21	1.26	4.67

The chosen time domain results are the relative peak and RMS values of the sampled signals normalized with respect to their expected values from an ideal sinusoidal reference with a peak value of 10 A. These results show that the PR controller still effectively controls the RMS value of the current and that its value remains unchanged when the DC-link voltage is increased to 6 kV. However, the relative peak

values increase with the DC-link voltage, due to an increase in the distortion of the signal. This also shows in the frequency domain metrics, where the normalized content of the 3^{rd} and 5^{th} harmonics are shown as well as the total harmonic distortion for the first 50 harmonics. Here it can be seen that the increase in DC-link voltage also increases the harmonic content of the signals. Interestingly though, the relative increase in harmonic distortion is less for the controller with dead time compensation than what is seen for the controller without dead time compensation.

5.4 Chapter Summary and Conclusion

This section presents a summary of the chapter and highlights the main findings presented throughout.

The first objective in the implementation of the controller was to ensure the integrity of the feedback current signal by evaluating the feasibility of the sampling strategy proposed in the 9^{th} semester's project [1], [2]. This was done by implementing the sampling strategy while operating the test setup in open loop control and comparing the results to a reference measurement. The sampling strategy has been proved to be effective in preventing the switching noise from corrupting the sampled currents.

After successful implementation and evaluation of the sampling strategy, it was decided to implement the actual current controller. Two different types of current controllers have been implemented and their performances compared.

First, a PI controller was implemented as robustness was initially valued over performance. However, the results from the PI controller showed that its tracking error was highly influenced by the dead time voltage error. These results deviated strongly from the expected values unless carefully equipped with a proper dead time compensation algorithm.

Two such compensation algorithms have been proposed and tested. The first of which was based on an estimation of the dead time voltage error from the sign of the current, which turned out to be insufficient due to instability issues. Therefore, a new compensation algorithm was implemented based on a fitting to the actual measurements of the dead time voltage error as a function of the measured load current. Though it was possible to make the PI controller approach its expected performance by adapting this dead time compensation algorithm, it was decided to investigate whether some performance gains could be made by deploying a PR controller instead.

For the developed PR controller, it was seen that it was possible to reduce the tracking error of the fundamental component of the 50 Hz reference signal to zero. The PR controller was significantly less affected by the dead time voltage error than what had been seen for the PI controller. While the dead time voltage error had a heavy impact on the amplitude of the fundamental component, this effect was completely eliminated in the PR controller, where the dead time voltage error only affected the harmonic content of the signal. The dead time voltage compensation algorithm is still valuable in the case of the PR controller as it helps in reducing the harmonics content of the signal, but it is not strictly necessary as was the case for the PI controller. Furthermore, no instability issues were encountered with the PR controller, which had been one of the concerns driving the choice for the initial controller implementation towards the PI controller in favor of the PR controller.

In summary, the PR controller has been found to provide superior performance compared to the PI controller without sacrificing the robustness and stability of the control loop. The PR controller effectively rejects the disturbance from the dead time voltage error at the fundamental frequency of the reference signal, but still suffers from the effect of the disturbance in its lower harmonic content, especially at the 3^{rd} harmonic.

Chapter 6

Determination of Power Module Losses

This chapter includes a determination of losses in the power modules at different operating points. In the further development and application of the 10 kV SiC MOSFET power modules, it would be beneficial to get some detailed test results relating their actual operation to the rated values of their design.

With the current controllers successfully implemented as described in Chapter 5, the setup now provides great flexibility for load testing of the power modules, and therefore, it was decided to map the power module losses and MOSFET die temperatures for different operating points, i.e. DC-link voltage, switching frequency, current magnitude, and current phase angle.

As the results presented in Chapter 5 have shown the PR controller with the fitted dead time compensation algorithm to achieve the best performance in terms of tracking the reference regarding current magnitude and phase at the fundamental frequency, this controller will be utilized throughout the tests performed in this chapter.

The chapter begins with a section that provides an overview of the expected loss contributors in the system and describes how they can be measured in practice. The next section introduces some general guidelines to adhere to when dealing with uncertainties in measurements before the chapter proceeds to describe in detail the actual loss measurements and their results.

6.1 Power Loss Contributors in the Experimental Setup

Before measuring the losses in the system, it needs to be considered which parts of the system will contribute to losses and how they can be measured and/or estimated. An overview of the system and the primary loss contributors are shown in Fig. 6.1.

When the converter is operating, losses will be present in the power modules due to switching and conduction. As the two power modules are mounted on the same power stack with a shared cooling system and shared DC supply, their combined losses will be lumped together to form the stack losses denoted as P_{Stack}. Furthermore, the circulation of load current through the filter inductors will result in Ohmic I^2R losses as well as iron losses, which gives rise to the dissipation of heat energy from the inductors to the ambient surrounding air denoted as P_{Ind}. When the system is operating in steady state, the power fed in from the two DC power supplies needs to balance out the combined stack and inductor losses, and therefore:

$$P_{DC+} + P_{DC-} = P_{Ind} + P_{Stack} \tag{6.1}$$

It should be noted that, in this context, the stack losses only account for the losses in the two power modules. Losses in the DC-link capacitors and busbars are neglected, and losses in the gate drivers are omitted from the discussion as they are supplied from a separate low voltage DC power supply.

The DC power supplies include internal measurements of their output voltage and current, and a measure for the power fed into the system from the DC power supplies is therefore readily available. However, before the losses in the power stack can be determined, it is necessary to measure and/or

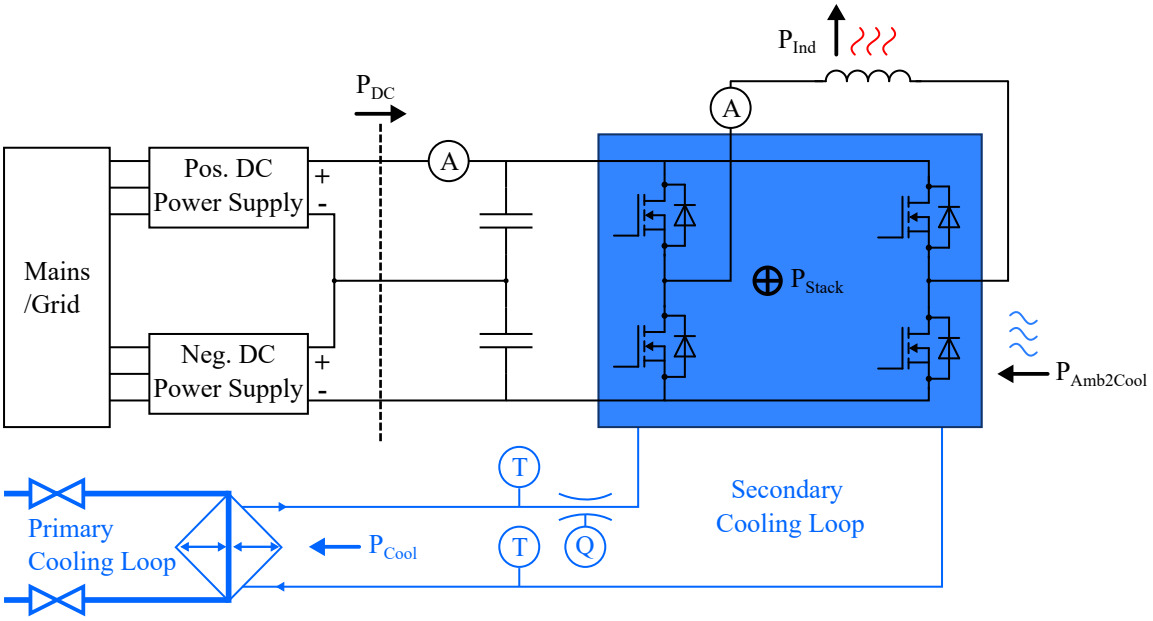


Figure 6.1: System overview and identification of primary loss contributors.

estimate the inductor losses. These losses will be estimated from the measured load current as it will be further explained in Section 6.4. Hence, the losses associated with the power modules in the stack will be determined as:

$$P_{Stack}(V_{DC}, I_{DC}, I_{Load}) = P_{DC}(V_{DC}, I_{DC}) - P_{Ind}(I_{Load}) \tag{6.2}$$

Another possible way to determine the losses in the power stack is to derive it from the flow rate and temperature difference between power stack inlet and outlet temperatures measured in the water cooling system using the integrated measuring unit MULTICAL 603 from Kamstrup [36]. The water cooling system consists of a primary and secondary loop, where the flow rate of the secondary loop is controlled by a pump. The water cooling system used is the *Shower Power* cooling concept from Danfoss, which features direct cooling of the power modules by guiding the cooling liquid along with the module baseplate by use of a turbulator [48]. Water cooling is a very effective way of transporting heat away from the power modules with heat transfer coefficients normally being orders of magnitudes higher than those of air cooling systems. It will therefore be assumed that the heat transfer to the ambient air surrounding the power modules will be negligible and that all the losses in the power modules are taken away through the water cooling system.

The water cooling system operates at coolant inlet temperatures in the range of 10°C to 15°C, and therefore, heat is also being transferred from the ambient air surrounding the setup to the water cooling system. The power associated with this heat transfer will be given the variable name $P_{Amb2Cool}$. Therefore, the total power associated with the water cooling system is determined as:

$$P_{Cool} = P_{Stack} + P_{Amb2Cool} \tag{6.3}$$

The contribution from the cooling of the ambient air, $P_{Amb2Cool}$, can be determined by measuring the power taken away by the water cooling system with the converter turned off (i.e. P_{Stack}=0). The value measured at this condition can then be subtracted from the measured values with the converter in operation to estimate the losses from the power stack as:

$$P_{Stack} = P_{Cool}(Q, \Delta T) - P_{Amb2Cool}(Q, \Delta T_0) \tag{6.4}$$

where Q is the flow rate of the water in the secondary loop, ΔT is the temperature difference between inlet and outlet during operation, and ΔT_0 is the temperature difference between inlet and outlet with the converter turned off.

6.2 Expected Power Module Losses

Before proceeding to describe the procedure for measurement of the losses with the corresponding results, this section presents an analysis of the expected losses in the power modules. The analysis will be based on data from a double pulse test performed on the power modules as presented in [3]. The analysis of the expected losses serves two purposes.

Firstly, it is of interest to see to what extent the power module losses can be predicted based on the previously obtained knowledge about the power modules from the double pulse test. This is particularly interesting, as the results presented in [3] have shown very good agreement between the measured switching losses from the double pulse test and a detailed power module model including its layout parasitics, which have been derived by utilizing digital design tools. If the expected power module losses from these results match with the actual power module losses at actual operating points, as will be measured in the experiments presented in this chapter, this would further underline the quality and usefulness of the digital design tools utilized for the development of the power modules at the department.

Secondly, the expected losses in the power modules need to be considered before calculating the measuring uncertainties to know in which range the uncertainties should be mapped. The losses present in the power modules are the sum of the switching- and conduction losses. The losses can be expressed in terms of the average power dissipated during one full switching period as:

$$P_{Module} = R_{ds(on)} \cdot I_{Load}^2 + (E_{on} + E_{off}) \cdot f_{sw} \tag{6.5}$$

where $R_{ds(on)}$ is the MOSFET on-state resistance, I_{Load} is the RMS output current of the power module during the switching cycle, E_{on} and E_{off} are the turn-on and turn-off switching energy dissipation respectively, and f_{sw} is the switching frequency.

The drain-source on-state resistance of the 10 kV MOSFET dies at 25°C is 350 mΩ as introduced in Chapter 2. The on-state resistance has a positive temperature coefficient meaning that it will increase with increasing temperature as presented in [24]. However, this temperature dependence will be neglected in this analysis and the conduction losses will therefore be determined based on the on-state resistance of 350 mΩ and the RMS output current.

In (6.5), it is worth noting that the switching energy dissipation is only included for a single turn-on and turn-off, even though both the HS and LS MOSFETs are switched on and off during a full switching period. This could lead one to believe that the switching energy dissipation should be multiplied by a factor of two in the equation. However, due to the dead time between the turn-off of one MOSFET and the turn-on of the other which causes freewheeling of the load current through the anti-parallel diode, one of the MOSFETs will effectively be soft-switching with zero voltage across it, and therefore, will have virtually zero switching losses. For positive output current, the freewheeling will take place in the LS diode as indicated in Fig. 6.2, and the LS MOSFET will be soft-switching, while the HS MOSFET is hard-switching the full DC-link voltage. For negative output current, the inverse applies as illustrated in Fig. 6.3.

The above only applies if the combination of the instantaneous output current and the duration of the dead time is such that the charging process of the device's parasitic capacitances, which was explained

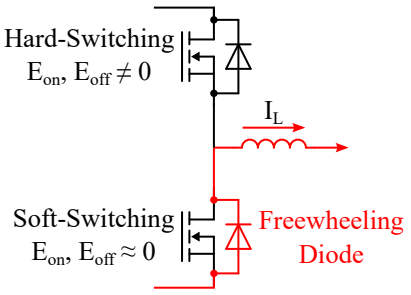


Figure 6.2: Impact of freewheeling on switching losses for positive output current.

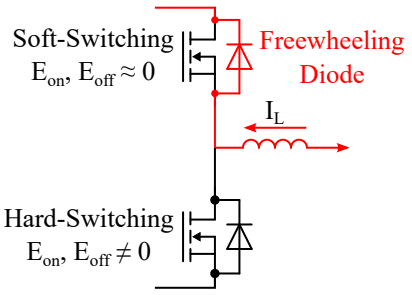


Figure 6.3: Impact of freewheeling on switching losses for negative output current.

in detail in Section 5.2, is complete. If the charging process is not yet complete, the diode is not freewheeling and the MOSFET will turn-on with some voltage across it resulting in switching losses. This will take place when the output current is low, or the dead time is short and will appear as shown in the measured waveform of Fig. 5.14 in Section 5.2, where the output voltage seen for the HS MOSFET turn-off is clamped at 2 μs when the LS MOSFET turns on. Therefore, the correct switching losses when averages across a full fundamental load cycle will be slightly higher than $(E_{on} + E_{off})$.

The switching losses are governed by the actual switching transients which have a complex dependency on both the gate resistance, DC-link voltage, and instantaneous output current. In [3], the total switching energy dissipation in a single MOSFET die embedded in a power module for both a turn-on and turn-off event has been tested with a double pulse test for current levels of 2, 6, and 14 A with DC-link voltages varying from 0.5 to 6 kV in 0.5 kV steps. As it turns out, the switching losses have a non-linear dependency on the output current, and they can therefore not be calculated directly from the RMS load current as was the case with the conduction losses.

To make an estimate of the effective switching losses for one fundamental period of sinusoidal load current, the switching losses will need to be obtained as a function of the instantaneous load current and then averaged across the whole period. To do so, it is needed to have the switching energy dissipation described as a function of the instantaneous load current. This relationship has been obtained by extracting the data from the double pulse test in [3] and making second order polynomial fits as shown in Fig. 6.4.

From the polynomial fits in Fig. 6.4, it is possible to estimate the expected switching losses in the power modules for a variety of operating points in terms of switching frequencies, load currents, and DC-link voltages by using (6.6).

$$P_{sw} = \frac{f_{sw}}{T_0} \int_{t}^{t+T_0} E_{sw}(V_{DC}, i_{Load}(t))\, dt \tag{6.6}$$

where P_{sw} is the expected switching losses, f_{sw} is the switching frequency, T_0 is the fundamental period of the load current, and E_{sw} is the switching energy dissipation for the instantaneous load current $i_{Load}(t)$ at a certain DC-link voltage V_{DC}.

The resulting curves for the combined switching- and conduction losses have been plotted for a switching frequency of 5 kHz in Fig. 6.5. Using these fitted curves, it is possible to predict the expected losses present in the power modules for the tests which have been planned as described in Chapter 3.

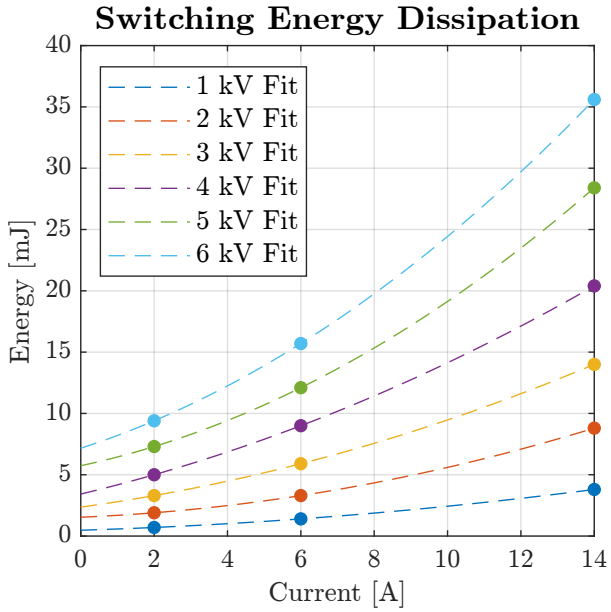


Figure 6.4: Turn-on and turn-off switching energy dissipation for varying load currents and DC-link voltages. *Source of data [3].*

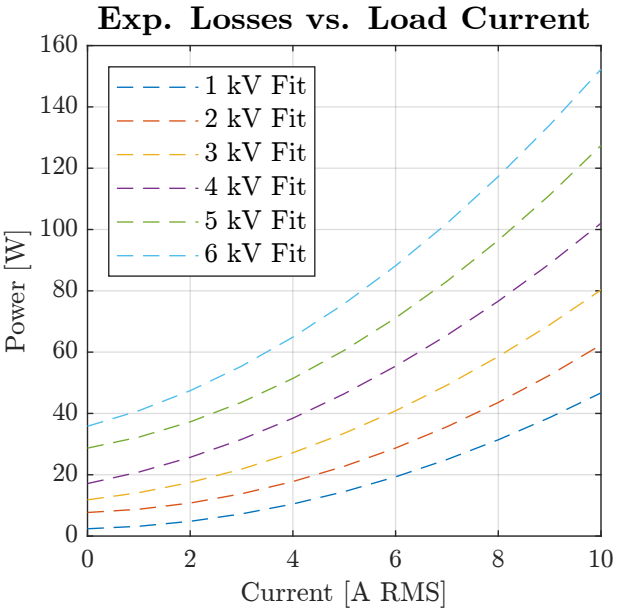


Figure 6.5: Expected power module losses (single module) for varying load currents and DC-link voltages at 5 kHz switching frequency.

6.3 Dealing With Uncertainty in Measurements and Calculations

Measurement of losses in power electronics systems is not a trivial task due to the very high efficiencies of the systems. This causes the losses to be comparatively small and means that measuring losses with high accuracy can be a challenging task. If the efficiency is also to be determined, the task becomes even more challenging. This is partly due to the propagation of uncertainty in calculations, but especially due to the PWM voltages and harmonic distortions in the currents, which are inherently present in power electronics systems and make it challenging to measure the output power with high accuracy. It is therefore very important to consider the accuracy of the measuring system before presenting the losses and efficiencies in power electronic systems. This is especially true for absolute measurements, where the measured results will stand alone in qualifying and specifying the efficiency of a power electronics converter.

In this particular case, however, measurements are to be used for relative comparison between different operating points of the system, and therefore, the requirements can be relaxed to some extent. Furthermore, no statements will be made regarding the overall efficiency and the measurements will focus on determining the losses only. The accuracy still needs to be considered but is not as critical as in the before mentioned case.

Before introducing the uncertainties associated with the measurement of the losses from the electrical and water cooling system, a brief introduction is given concerning how to deal with uncertainty in measurements and calculations. As the determination of losses will include multiplication, division, addition, and subtraction of different measured quantities, it is important to consider how to deal with the concept of propagation of uncertainty in such calculations. This can be dealt with by adhering to the following guidelines, which are derived by considering the uncertainty as the standard error of experiments with non-systematic (random) errors [49] as shown in Table 6.1.

Table 6.1: Guidelines for dealing with uncertainty in calculations.

Operation	**Correlation**	**Procedure**
Addition/ Subtraction	Independent	The **absolute uncertainty** is given as the root sum of squares of the individual **absolute uncertainties**
	Correlated	The **absolute uncertainty** is given as the sum of the **absolute uncertainties**
Multiplication/ Division	Independent	The **relative uncertainty** is given as the root sum of squares of the individual **relative uncertainties**
	Correlated	The **relative uncertainty** is given as the sum of the **relative uncertainties**

Another way to deal with the propagation of uncertainty through calculations is to use the upper-lower bound method. This method, even though not providing theoretically correct uncertainties with respect to the measurement standard error, will give a reasonable estimate of the measurement uncertainty. In fact, the upper-lower bound method will result in a higher value of the calculated uncertainty and is therefore the most conservative way of computing it. The method is based on calculating, the worst-case uncertainty in the measurements from the absolute uncertainties [49]. For example, in the case of calculating DC power from a current measurement of 2.0 A ±0.2 A and a voltage measurement of 5.0 V ±0.2 V, the worst-case variation in the power will be if both values are measured at their upper or lower bounds, that is:

$$\begin{aligned} P_{Upper} &= 2.2\ \text{A} \cdot 5.2\ \text{V} = 11.44\ \text{W} \\ P_{Lower} &= 1.8\ \text{A} \cdot 4.8\ \text{V} = 8.64\ \text{W} \end{aligned} \tag{6.7}$$

and therefore, the true value of the measured power will lie somewhere in that interval.

The uncertainty of a given measurement should also be reflected in the number of significant digits presented in the results. Presenting a result with too many significant digits can mislead the reader to believe that the presented value has a high accuracy even though this might not be the case. For example, consider the above mentioned example, one might be tempted to write the result as 10.0 W. However, as the total uncertainty of those two correlated measurements evaluates as 14% from the guidelines of Table 6.1, the actual result should not be displayed with more than two significant digits that is 10 W ±14%.

In general, it is good practice to adhere to the guidelines presented in Table 6.2 when dealing with significant digits in the representation of measurements.

Table 6.2: Guidelines for dealing with significant digits in representing measured values.

Operation	**Rounding**
Addition/ Subtraction	The result should be rounded off to the **last decimal place** in the **least precise** number
Multiplication/ Division	The result should be rounded to the **smallest number of significant digits** in **any** of the original numbers

Throughout the remainder of this section, accuracy in measurements and calculations will be treated as stated in Tables 6.1 and 6.2 unless otherwise is stated explicitly. As measurements are performed on the same system operating at the same operating points, measurements will be strongly correlated and will be considered as such.

6.4 Estimation of Inductor Losses

Measurement of the inductor losses during the operation of the medium voltage experimental setup is both complicated and impractical. It is therefore desirable to perform a separate experiment to determine the inductor losses as a function of their load current. As the controlled load current is near-sinusoidal with very low ripple content, it is assumed that a corresponding experiment with the inductor losses measured when supplied by sinusoidal output voltage generated from a variable transformer will be representative of the losses in the inductors.

The inductors are therefore taken out of the experimental setup and supplied from a variable transformer as illustrated in Fig. 6.6. A power meter (Voltech PM100 [50]) is inserted in series with the inductors to measure the losses as the active power is supplied to it. Measurements are done with both filter inductors in the loop even though only illustrated as a single inductance below.

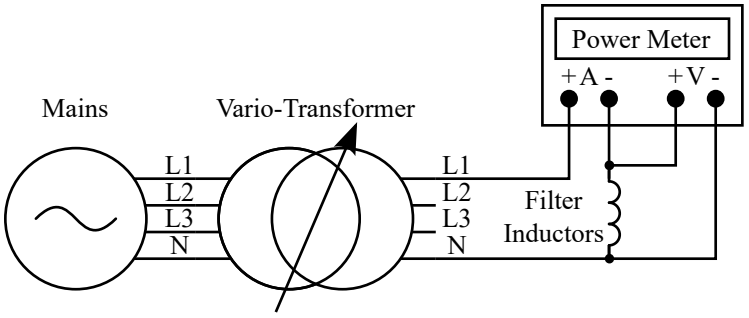


Figure 6.6: Schematic of the inductor loss test.

A photograph of the measurement setup is shown in Fig. 6.7.

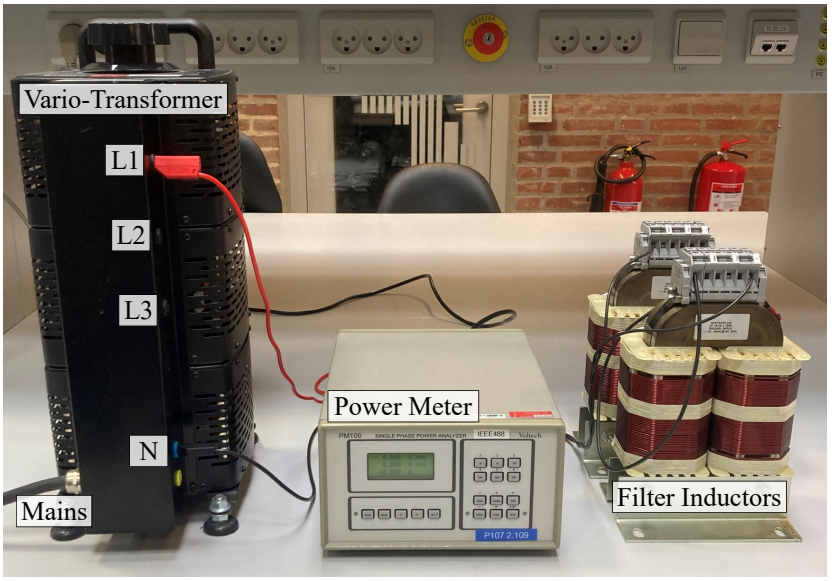


Figure 6.7: Photograph of the inductor loss test.

As the losses are measured using the direct method without any voltage or current probes, the accuracy of the measurement is determined by the accuracy of the power meter only. The datasheet specification of accuracies for the power meter (Voltech PM100 [50]) is as shown in Table 6.3.

Table 6.3: Accuracy of power meter [50].

Reading [%]	**Range** [%]	**Constant** [W]	**Frequency** [% / kHz]
0.2%	0.2%	0.005	0.3%

As the power meter is auto ranging on its current and voltage ranges, the accuracy of the measurements depends on the power range at which the measurement is taken. The accuracy of each measurement has been evaluated in Appendix C, in which it is found that the accuracies highly depend on the power range as they vary within an interval of 8% to 21%.

The measured losses have been fitted to a second order polynomial with a forced interception through zero in Excel. The second order polynomial is chosen as it will account for the quadratic nature of the Ohmic I^2R losses. The curve fitting also includes a first-order term to account for additional non Ohmic losses, e.g. hysteresis and eddy current losses in the core. Even though these additional inductor losses can be very non-linear in their nature, the fitted curve shows good agreement with the measured data. The resulting curve along with the measured values with their absolute uncertainty intervals added is shown in Fig. 6.8.

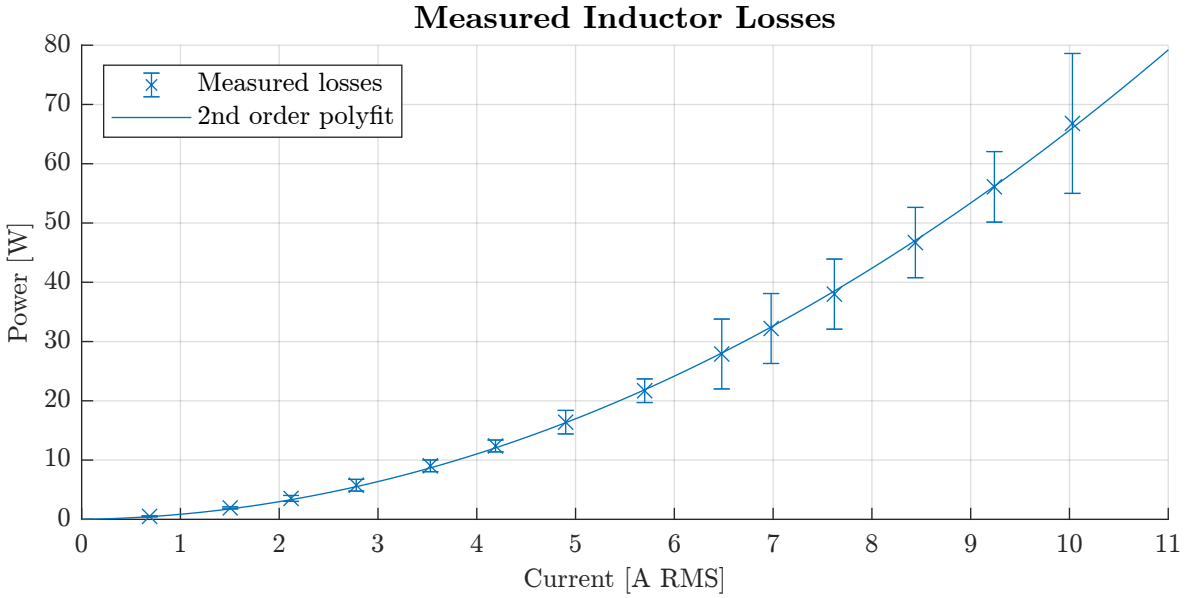


Figure 6.8: Measured power losses from inductor loss test.

The fitted polynomial has an R^2 value of .99 and has the following equation:

$$P_{Ind}(I_{Load}) = 0.6346 \cdot I_{Load}^2 + 0.2195 \cdot I_{Load} \tag{6.8}$$

with P_{Ind} being the power loss in watts and I_{Load} the inductor load current in amperes RMS.

In the following use of the fitted curve for estimating the inductor losses, to simplify the calculations, the resulting inductor losses are assumed to have 20% uncertainty, as this will roughly account for the worst uncertainty seen in the inductor loss measurements.

To qualify the measurement system and to check for any distortion in the waveforms, the applied voltage has been measured with a differential probe (LeCroy HVD3206A [32]) while the load current has been measured with a current probe (LeCroy CP030 [33]). The results are shown in Fig. 6.9.

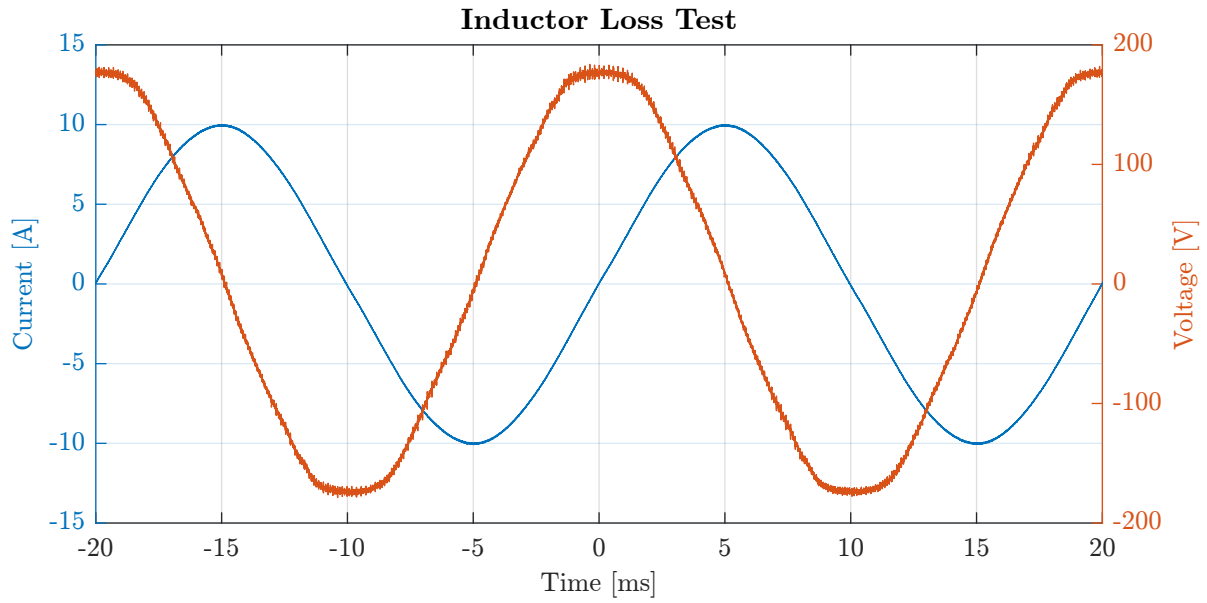


Figure 6.9: Measured current and voltage waveforms during inductor loss test.

It can be seen that the current waveform is close to sinusoidal even though the voltage is somewhat flat-topped. All in all, with the reasonably looking waveforms and the very accurate fit of the polynomial approximation, the determined relationship between the load current and the inductor losses is found to be of good enough quality for further use in the power stack loss estimation.

6.5 Procedure and Uncertainty of Electrical Measurements

Having an estimation of the inductor losses in place, the next step is to measure the power fed into the system from the DC power supplies. This will require measurement of the DC power supplies' voltage and current, which can be multiplied to obtain the supplied DC power.

As stated in the system description in Chapter 2, the DC power supply constitutes two Magna-Power XR6000-1 DC power supplies rated for 6 kW each. The DC power supplies come with built-in voltage and current measurement capabilities, but as the expected losses in the system are very low compared to the combined rated power of 12 kW for the two DC power supplies, it is important to consider whether the accuracy of these built-in measurements will be sufficient for loss estimation.

In the previous chapter, the converter was operated at 3 kV with a rated load current of 7 A RMS and a switching frequency of 5 kHz to evaluate the controller performance. During these tests, the current supplied by the DC power supplies were found to be as low as 40 mA, which is only a fraction of the rated current range of the DC power supplies. It was therefore desired to calculate the uncertainty of the measurements when using the readings of voltage and current from the built-in measurements from the DC power supplies.

6.5.1 Uncertainty of Voltage and Current Measurements

The datasheet specification of accuracies for the internal voltage and current measurements of the Magna-Power XR6000-1 DC power supplies [26] are shown in Table 6.4.

Table 6.4: Accuracy of internal DC power supply measurement [26].

Variable	Range	Range	Accuracy
Voltage	6000 V	±0.2%	12 V
Current	1 A	±0.2%	0.002 A

The relative uncertainty of the total DC power measurement as a function of the measured voltage and current is found in Appendix C to be given as:

$$P_{DC}^{Acc,\%}(U,I) = \left(\frac{12\text{ V}}{U} + \frac{0.002\text{ A}}{I}\right) \tag{6.9}$$

where U is the voltage reading and I is the current reading.

The relative uncertainty can be represented in tabulated form to inspect how the uncertainty changes at different operating points. The resulting uncertainties can be seen in Table 6.5. It should be noted that the table covers the full measuring range of DC power supplies, which spans from a few tenths of watts to six kilowatts at max.

Table 6.5: Uncertainty of voltage and current measurement of DC power supplies.

I [A] \ U [V]	500	1000	1500	2000	2500	3000	3500	4000	4500	5000	5500	6000
0.050	6.4%	5.2%	4.8%	4.6%	4.5%	4.4%	4.3%	4.3%	4.3%	4.2%	4.2%	4.2%
0.100	4.4%	3.2%	2.8%	2.6%	2.5%	2.4%	2.3%	2.3%	2.3%	2.2%	2.2%	2.2%
0.150	3.7%	2.5%	2.1%	1.9%	1.8%	1.7%	1.7%	1.6%	1.6%	1.6%	1.6%	1.5%
0.200	3.4%	2.2%	1.8%	1.6%	1.5%	1.4%	1.3%	1.3%	1.3%	1.2%	1.2%	1.2%
0.250	3.2%	2.0%	1.6%	1.4%	1.3%	1.2%	1.1%	1.1%	1.1%	1.0%	1.0%	1.0%
0.300	3.1%	1.9%	1.5%	1.3%	1.1%	1.1%	1.0%	1.0%	0.9%	0.9%	0.9%	0.9%
0.350	3.0%	1.8%	1.4%	1.2%	1.1%	1.0%	0.9%	0.9%	0.8%	0.8%	0.8%	0.8%
0.400	2.9%	1.7%	1.3%	1.1%	1.0%	0.9%	0.8%	0.8%	0.8%	0.7%	0.7%	0.7%
0.450	2.8%	1.6%	1.2%	1.0%	0.9%	0.8%	0.8%	0.7%	0.7%	0.7%	0.7%	0.6%
0.500	2.8%	1.6%	1.2%	1.0%	0.9%	0.8%	0.7%	0.7%	0.7%	0.6%	0.6%	0.6%
0.550	2.8%	1.6%	1.2%	1.0%	0.8%	0.8%	0.7%	0.7%	0.6%	0.6%	0.6%	0.6%
0.600	2.7%	1.5%	1.1%	0.9%	0.8%	0.7%	0.7%	0.6%	0.6%	0.6%	0.6%	0.5%
0.650	2.7%	1.5%	1.1%	0.9%	0.8%	0.7%	0.7%	0.6%	0.6%	0.5%	0.5%	0.5%
0.700	2.7%	1.5%	1.1%	0.9%	0.8%	0.7%	0.6%	0.6%	0.6%	0.5%	0.5%	0.5%
0.750	2.7%	1.5%	1.1%	0.9%	0.7%	0.7%	0.6%	0.6%	0.5%	0.5%	0.5%	0.5%
0.800	2.7%	1.5%	1.1%	0.9%	0.7%	0.7%	0.6%	0.6%	0.5%	0.5%	0.5%	0.5%
0.850	2.6%	1.4%	1.0%	0.8%	0.7%	0.6%	0.6%	0.5%	0.5%	0.5%	0.5%	0.4%
0.900	2.6%	1.4%	1.0%	0.8%	0.7%	0.6%	0.6%	0.5%	0.5%	0.5%	0.4%	0.4%
0.950	2.6%	1.4%	1.0%	0.8%	0.7%	0.6%	0.6%	0.5%	0.5%	0.5%	0.4%	0.4%
1.000	2.6%	1.4%	1.0%	0.8%	0.7%	0.6%	0.5%	0.5%	0.5%	0.4%	0.4%	0.4%

As can be seen in the above table, the accuracy is highly influenced by the low utilization of the current and voltage range of the internal measurements. With the expected power stack losses being only a few hundred watts, the uncertainty of the DC power supplies should be found within the first two rows, limiting the uncertainty to be 2% or more.

6.5.2 Total Uncertainty of Electrical Measurements

In the final loss estimation for the power stack losses, the inductor losses need to be subtracted from the losses fed by DC power supplies. Therefore, the total absolute uncertainty will be the sum of the absolute uncertainties from both measurements as stated in Table 6.1. The total absolute uncertainty for the power stack losses derived from the electrical measurements is converted into its total relative uncertainty as:

$$P_{Stack}^{Acc}(U,I) = P_{DC}^{Acc}(U,I) + P_{Ind}^{Acc} = P_{DC}^{Acc,\%}(U,I) \cdot P_{DC}(U,I) + P_{Ind}^{Acc,\%} \cdot P_{Ind} \tag{6.10}$$

$$P_{Stack}^{Acc,\%}(U,I) = \frac{P_{Stack}^{Acc}(U,I)}{P_{DC}(U,I) - P_{Ind}} \tag{6.11}$$

The total relative uncertainty for the power stack losses can also be represented in tabulated form to map the uncertainties in the expected operating range as shown in Table 6.6. The table maps the total relative uncertainties for a load current of 7 A RMS resulting in 32.6 W of inductor losses with an assumed uncertainty of 20%. It should be noticed that the current range has been changed to 0.1 A, corresponding to the first two rows of Table 6.5. This is to increase the resolution within the expected range of losses spanning a few hundred watts, being the sum of the expected power module losses from Fig. 6.5 and inductor losses from Fig. 6.8. Further, some cells are grayed out since these are invalid operating points as the inductor losses exceed the power fed by the DC power supplies.

Table 6.6: Uncertainty of power stack losses derived from electrical measurements.

U [V] / I [A]	500	1000	1500	2000	2500	3000	3500	4000	4500	5000	5500	6000
0.010	-	-	-	-	-	-	-	-	-	96%	79%	68%
0.020	-	-	-	-	68%	47%	37%	31%	27%	25%	23%	21%
0.030	-	-	80%	40%	28%	22%	19%	17%	16%	14%	14%	13%
0.040	-	-	37%	23%	18%	15%	13%	12%	11%	10%	9.6%	9.2%
0.050	-	53%	24%	17%	13%	11%	9.9%	9.0%	8.4%	7.9%	7.5%	7.2%
0.060	-	34%	18%	13%	10%	9.0%	8.0%	7.4%	6.8%	6.5%	6.1%	5.9%
0.070	-	25%	14%	11%	8.7%	7.5%	6.8%	6.2%	5.8%	5.5%	5.2%	5.0%
0.080	-	20%	12%	9.0%	7.5%	6.5%	5.9%	5.4%	5.0%	4.8%	4.5%	4.4%
0.090	70%	17%	10%	7.9%	6.6%	5.7%	5.2%	4.8%	4.5%	4.2%	4.0%	3.9%
0.100	50%	14%	9.1%	7.0%	5.9%	5.1%	4.6%	4.3%	4.0%	3.8%	3.6%	3.5%

The table shows how significant the impact is on the total relative uncertainty when the absolute uncertainty of the inductor losses is on the same level as the absolute uncertainty of the DC power supplies. Based on the uncertainties presented in the table, the expected uncertainty for deriving the power stack losses from the electrical measurements will be within the range of 10% to 20%.

6.6 Procedure and Uncertainty of Water Cooling Measurements

To estimate the power stack losses from the water cooling measurements, the uncertainty of the flow rate and temperature measurements needs to be calculated since the power is taken out by the water cooling system is given by:

$$P_{Cool}(Q, \Delta T) = Q \cdot C \cdot \Delta T \tag{6.12}$$

where C is the specific heat capacity of water.

The flow rate and delta temperature of the water cooling system are measured using a MULTICAL 603 measuring unit and sensors from Kamstrup [36]. The MULTICAL 603 is normally used as a measuring unit for district heating of residential or commercial buildings where relatively high delta temperatures are to be expected. The measuring unit and sensors are only type approved for measuring delta temperatures of 3 K to 178 K, and therefore, the datasheet specification of accuracies strictly only applies within this range.

The water cooling system is built for cooling of an IGBT based converter with a rated power of 500 kVA where the losses are much larger than those expected in the current experimental setup. It is therefore important to consider at which flow rate the water cooling system should be operated to avoid having a too low delta temperature. The flow rate of the cooling water can be controlled by setting the supply frequency of the pump to achieve a certain flow rate. The frequency of the pump has been set to its practical minimum being 5 Hz to achieve an average flow rate of around 150 L/h. Operating at this low flow rate has the benefits of achieving higher delta temperatures for the low expected losses but increases the time constant of the system as it takes longer for the coolant to be circulated.

The results used to evaluate the controller performance in the last chapter were performed with an average flow rate of approx. 150 L/h. During these tests, delta temperatures of less than 1 K were measured, being below its type approved range. Therefore, the uncertainty of the measurements is not strictly valid, but the measurements will be taken anyway and compared to the electrical loss estimations.

6.6.1 Uncertainty of Flow Rate and Temperature Measurements

The datasheet specification of accuracies for the flow rate and temperature measurements made with the Kamstrup MULTICAL 603 measuring unit and sensors [36] are shown in Table 6.7.

Table 6.7: Accuracy of Kamstrup MULTICAL 603 measuring unit and sensors [36].

Equipment	**Accuracy**
MULTICAL 603	±(0.15 + 2/ΔT)%
Flow sensor	±(1 + 0.01 q_i/Q)%
Temperature sensor	±(0.4 + 4/ΔT)%

where q_i is the maximum flow rate of 1500 L/h.

The relative uncertainty for the water cooling measurements is the sum of the three accuracies presented in Table 6.7. As shown in the table above, the relative uncertainty is given as a function of the measured flow rate and delta temperature. The relative uncertainty is given by:

$$P_{Cool}^{Acc,\%}(Q, \Delta T) = \left(0.15 + \frac{2}{\Delta T}\right) + \left(1 + \frac{0.01 q_i}{Q}\right) + \left(0.4 + \frac{4}{\Delta T}\right) \tag{6.13}$$

The relative uncertainties can be represented in tabulated form to inspect how the uncertainty changes at different operating points. This has been done for the expected range of measured flow rates and delta temperatures in Table 6.8. The table covers approximately the same power range as presented in Table 6.5, spanning from a few tenths of watts to almost six kilowatts at max.

Table 6.8: Uncertainty of water cooling measurements using Kamstrup measuring unit.

ΔT [K] \ Q [L/h]	50	100	150	200	250	300	350	400	450	500
0.50	14%	14%	14%	14%	14%	14%	14%	14%	14%	14%
1.00	7.9%	7.7%	7.7%	7.6%	7.6%	7.6%	7.6%	7.6%	7.6%	7.6%
1.50	5.9%	5.7%	5.7%	5.6%	5.6%	5.6%	5.6%	5.6%	5.6%	5.6%
2.00	4.9%	4.7%	4.7%	4.6%	4.6%	4.6%	4.6%	4.6%	4.6%	4.6%
2.50	4.3%	4.1%	4.1%	4.0%	4.0%	4.0%	4.0%	4.0%	4.0%	4.0%
3.00	3.9%	3.7%	3.7%	3.6%	3.6%	3.6%	3.6%	3.6%	3.6%	3.6%
3.50	3.6%	3.4%	3.4%	3.3%	3.3%	3.3%	3.3%	3.3%	3.3%	3.3%
4.00	3.4%	3.2%	3.2%	3.1%	3.1%	3.1%	3.1%	3.1%	3.1%	3.1%
4.50	3.2%	3.0%	3.0%	3.0%	2.9%	2.9%	2.9%	2.9%	2.9%	2.9%
5.00	3.1%	2.9%	2.9%	2.8%	2.8%	2.8%	2.8%	2.8%	2.8%	2.8%
5.50	2.9%	2.8%	2.7%	2.7%	2.7%	2.7%	2.7%	2.7%	2.7%	2.7%
6.00	2.9%	2.7%	2.7%	2.6%	2.6%	2.6%	2.6%	2.6%	2.6%	2.6%
6.50	2.8%	2.6%	2.6%	2.5%	2.5%	2.5%	2.5%	2.5%	2.5%	2.5%
7.00	2.7%	2.6%	2.5%	2.5%	2.5%	2.5%	2.5%	2.4%	2.4%	2.4%
7.50	2.7%	2.5%	2.5%	2.4%	2.4%	2.4%	2.4%	2.4%	2.4%	2.4%
8.00	2.6%	2.5%	2.4%	2.4%	2.4%	2.4%	2.3%	2.3%	2.3%	2.3%
8.50	2.6%	2.4%	2.4%	2.3%	2.3%	2.3%	2.3%	2.3%	2.3%	2.3%
9.00	2.5%	2.4%	2.3%	2.3%	2.3%	2.3%	2.3%	2.3%	2.3%	2.2%
9.50	2.5%	2.3%	2.3%	2.3%	2.2%	2.2%	2.2%	2.2%	2.2%	2.2%
10.0	2.5%	2.3%	2.3%	2.2%	2.2%	2.2%	2.2%	2.2%	2.2%	2.2%

As can be seen in the above table, the uncertainty is highly influenced by low delta temperatures, which can cause the uncertainty to be more than 10% in some cases. However, as the water cooling system is operated at a constant flow rate of approx. 150 L/h, delta temperatures of a few degrees are expected at full load, lowering the uncertainty to 5% or below. However, the lowest achievable uncertainty is 1.55% limited by the constant terms for the measuring equipment as presented in Table 6.7.

As introduced in Section 6.1, the water cooling system is operated at coolant inlet temperatures in the range of 10°C to 15°C, and therefore, heat is also being transferred from the ambient air surrounding the setup to the water cooling system. This contribution from the cooling of the ambient air is denoted as $P_{Amb2Cool}$ and has been measured with the converter turned off at an ambient temperature of 21°C. As this will appear as an offset in the loss measurements, it is important to account for it when using the cooling system to deduct the losses. This offset has been measured with an average flow rate of 157 L/h resulting in a delta temperature of 0.22 K, corresponding to a heat transfer offset of approx. 40 W. From (6.13), this measurement has an uncertainty of 29% as the delta temperature is very small. It is assumed that the cooling of ambient air is constant during the converter operation to simplify the computations, and the offset is simply subtracted from the measurements to obtain the stack losses.

6.6.2 Total Uncertainty of Water Cooling System Measurements

To find the final loss estimation for the power stack losses using the water cooling measurements, the losses due to the cooling of the ambient air need to be subtracted from the losses measured during operation. Again, the total absolute uncertainty will be the sum of the absolute uncertainties from both measurements according to the rule of propagation of uncertainties as stated in Table 6.1. The total uncertainty for the power stack losses derived from the water cooling measurements is converted into total relative uncertainty as:

$$\begin{aligned} P_{Stack}^{Acc}(Q,\Delta T) &= P_{Cool}^{Acc}(Q,\Delta T) + P_{Amb2Cool}^{Acc} \\ &= P_{Cool}^{Acc,\%}(Q,\Delta T)\cdot P_{Cool}(Q,\Delta T) + P_{Amb2Cool}^{Acc,\%}\cdot P_{Amb2Cool} \end{aligned} \tag{6.14}$$

$$P_{Stack}^{Acc,\%}(Q,\Delta T) = \frac{P_{Stack}^{Acc}(Q,\Delta T)}{P_{Cool}(Q,\Delta T) - P_{Amb2Cool}} \tag{6.15}$$

The total relative uncertainty for the power stack losses can then be represented in tabulated form to map the uncertainties in the expected operating range as shown in Table 6.9. The total relative uncertainties mapped in the table are subject to an uncertainty of 29% in the measurement of the cooling of the ambient air, resulting in an absolute uncertainty of 12 W in a 40 W measurement. Note that the delta temperature range has been changed to 2 K, corresponding to the first four rows in Table 6.8, to increase the resolution within the expected operating range of a few hundred watts. Further, some cells are marked with gray since these values are invalid as the subtraction of the offset losses results in negative stack losses.

Table 6.9: Uncertainty of power stack losses derived from water cooling measurements.

ΔT [K] \ Q [L/h]	50	100	150	200	250	300	350	400	450	500
0.20	-	-	-	-	-	85%	67%	56%	50%	45%
0.40	-	-	64%	41%	31%	27%	24%	21%	20%	19%
0.60	-	57%	30%	22%	19%	16%	15%	14%	13%	12%
0.80	-	33%	20%	16%	13%	12%	11%	10%	9.8%	9.4%
1.00	82%	23%	15%	12%	11%	9.6%	8.9%	8.4%	8.0%	7.7%
1.20	50%	18%	13%	10%	9.0%	8.2%	7.6%	7.2%	6.9%	6.6%
1.40	37%	15%	11%	8.9%	7.8%	7.1%	6.7%	6.3%	6.1%	5.9%
1.60	29%	13%	9.4%	7.8%	7.0%	6.4%	6.0%	5.7%	5.5%	5.3%
1.80	24%	11%	8.4%	7.1%	6.3%	5.8%	5.5%	5.2%	5.0%	4.9%
2.00	21%	10%	7.7%	6.5%	5.8%	5.4%	5.1%	4.8%	4.7%	4.5%

The table shows how heavily the total relative uncertainty is impacted in the expected operating range. This is due to the high uncertainty present at low delta temperatures, which is worsened by the propagation of uncertainty when subtracting the offset losses from the cooling of the ambient air.

6.7 Uncertainty of MOSFET Die Temperature Measurements

The temperature of the MOSFET dies is measured using the OpSens temperature unit [34] and OTG-F fiber optic temperature sensors from OpSens [35], whereas the inlet coolant temperature is measured using the Kamstrup MULTICAL 603 measuring unit [36] and Pt500 temperature sensors [51]. The datasheet specification of absolute measurement accuracies for the above measuring equipment is summarized in Table 6.10.

Table 6.10: Accuracy of MOSFET die temperature measurements [35], [51].

Equipment	Measurement	Accuracy
OpSens OTG-F	MOSFET die	±0.8 K
Kamstrup Pt500	Inlet coolant	±1.0 K

The delta temperature of the MOSFET die is calculated as the difference between the MOSFET die and inlet coolant temperature as:

$$\Delta T = T_{Die} - T_{Inlet} \tag{6.16}$$

The uncertainty of the delta temperature of the MOSFET die is therefore the sum of the accuracies presented in the above table according to the rule for the propagation of uncertainties for subtraction. Therefore, the used value for the total absolute uncertainty of the delta temperatures of the MOSFET dies is 1.8 K.

6.8 Test of Power Modules At Different Operating Points

With the current controller successfully implemented, the expected power module losses identified, and the uncertainties mapped for both determination methods of the power stack losses, it is now possible to test the power modules at different operating points and make a thorough comparison. The operating points under test are different DC-link voltages, switching frequencies, current magnitudes, and current phase angles. During each of the tests, the estimated power stack losses from both the electrical and water cooling measurements have been measured to map and compare the losses. The estimated power stack losses from both methods are further compared with a dashed line indicating the expected power module losses from Section 6.2 multiplied by two to obtain the total power stack losses. Furthermore, the MOSFET die temperatures of the receiving power module together with the inlet temperature have been measured to calculate the die delta temperature.

It should be noticed that only two pipettes are mounted in the power module defined as the receiving power module. The pipettes are inserted during the manufacturing of the power modules, which leaves room in the silicone gel for the temperature sensors to be placed directly on top of the MOSFET dies. However, with the power modules mounted in the power stack under test, only the two pipettes above the MOSFET dies of the receiving power modules have been inserted, limiting the measurement to only these two MOSFET dies.

In the presented results for the power stack losses, the estimated power stack losses are shown with their absolute uncertainty intervals added as error bars. Both the electrical and water cooling measurements are performed at the same operating point, however, they have been shifted slightly on the x-axis in the presented figures to increase their readability. The actual x-axis operating point for the measurements is given by their nearest x-axis label linked to the grid tick.

Varying DC-Link Voltage

The estimated losses in the power stack while varying the DC-link voltage are shown in Fig. 6.10 and the measured delta temperatures are shown in Fig. 6.11. All of the measurements presented below have been performed with a switching frequency of 5 kHz, a load current of 7.0 A RMS, and a power factor of 1 for the sending power module and a power factor of -1 for the receiving power module. It should be noted that measurements were initially only taken at 3 kV and below, however, a DC-link voltage of 6 kV was achieved later as described in Section 3.3, measurements from 3 to 6 kV have been added afterward.

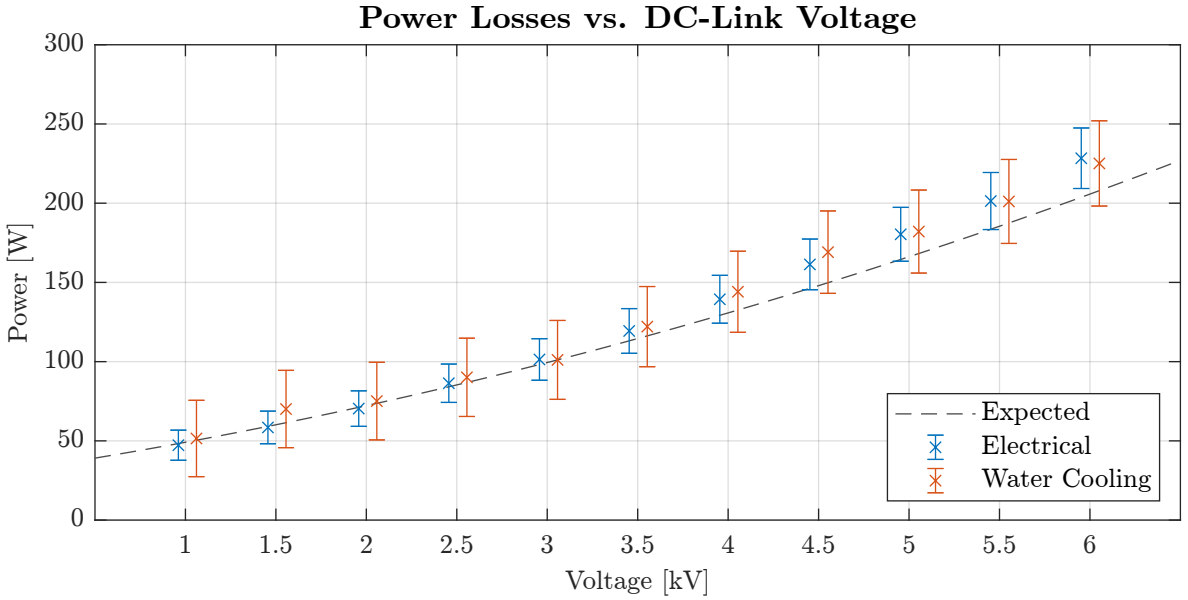


Figure 6.10: Estimated power losses at different DC-link voltages.

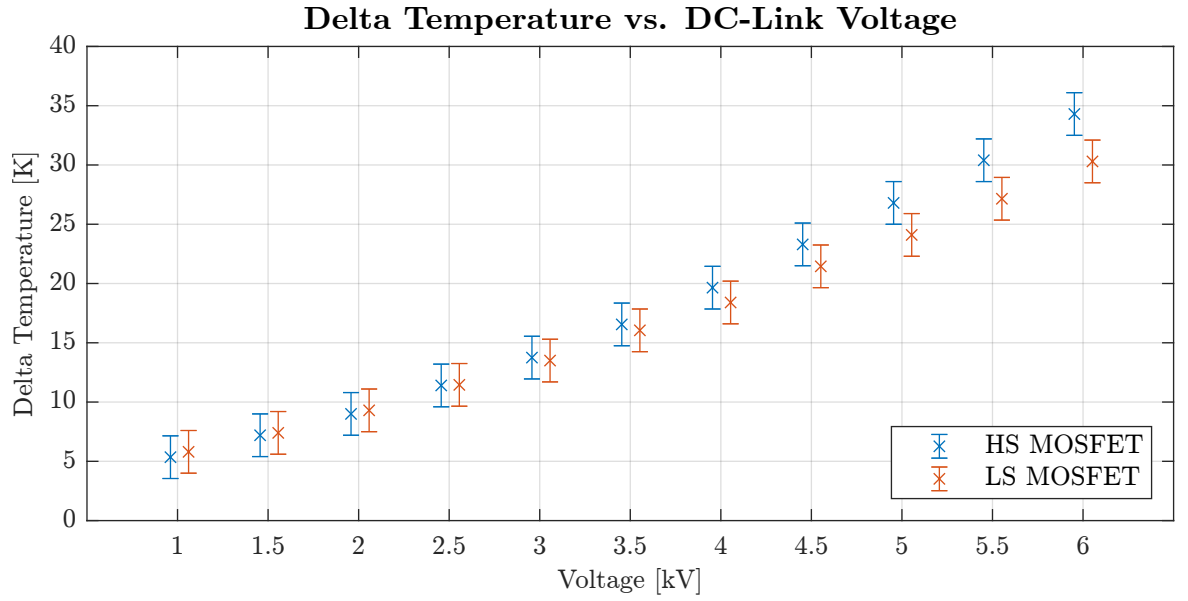


Figure 6.11: Delta die temperature at different DC-link voltages.

In general, it can be seen from the above figures that when comparing the estimated to the expected power stack losses, a very high agreement is seen for DC-link voltages below 3 kV. However, the losses are slightly underestimated for DC-link voltages above 3 kV.

As the last point in this data series contains the data from the rated operating point of the power modules, it is worthy of some extra mentioning. The estimated losses from the electrical measurements are 229 W subject to an uncertainty of 8.3%, whereas the water cooling measurements estimate 225 W with an uncertainty of 12%. The delta die temperatures of the HS and LS MOSFETs are measured to be 34.3 K and 30.3 K, respectively, with an absolute uncertainty of 1.8 K.

Varying Switching Frequency

The estimated power losses for varying switching frequencies are shown in Fig. 6.12 and the measured delta temperatures are shown in Fig. 6.13. All of the measurements presented below have been performed at a DC-link voltage of 3 kV, a load current of 7.0 A RMS, and a power factor of 1 and -1 for the sending and receiving power modules, respectively.

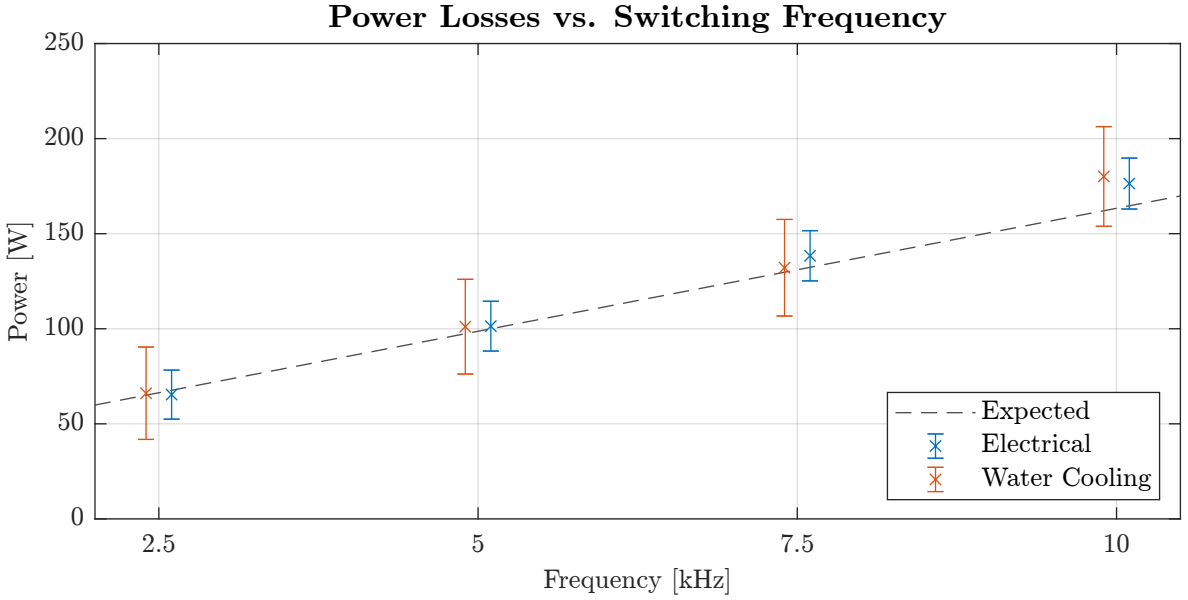


Figure 6.12: Power losses at different switching frequencies.

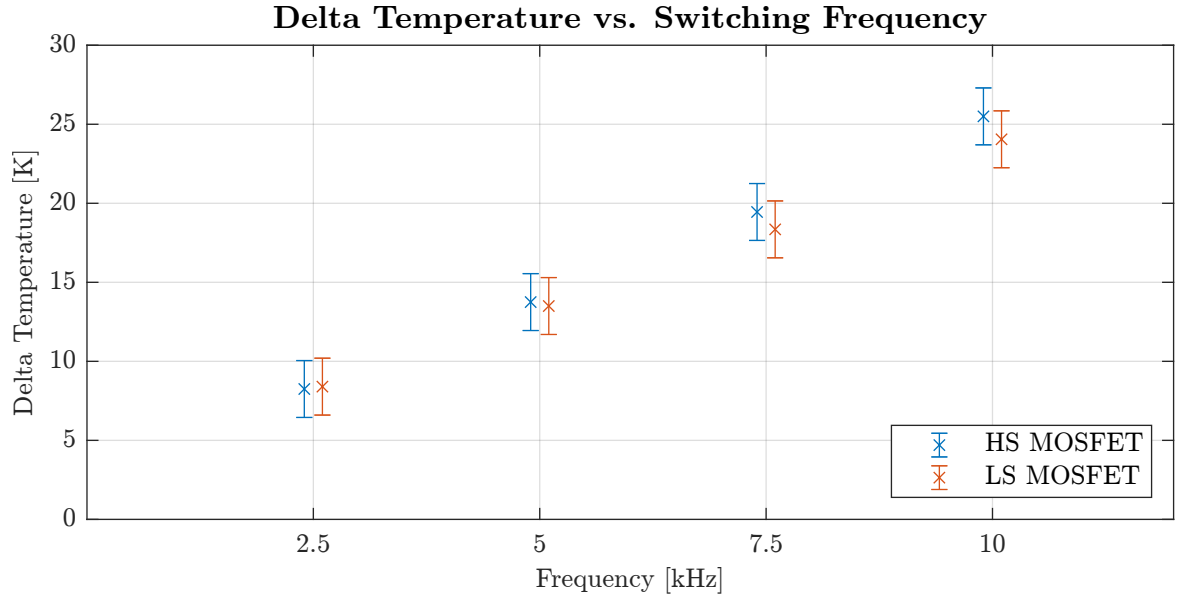


Figure 6.13: Delta die temperature at different switching frequencies.

From the above, it can be seen that the power stack losses and the delta MOSFET die temperatures increases approximately linearly with the switching frequency as expected. However, the trend seems to be slightly higher than expected. This is likely due to a slight underestimation of the switching

energy dissipation, which results in a too low trend when multiplied with the switching frequency to obtain the expected power stack losses.

Varying Current Magnitude

The estimated power losses at different current magnitudes are shown in Fig. 6.14 and the measured delta temperatures are shown in Fig. 6.15. It should be noticed that the x-axes are shown in RMS current. All of the measurements presented below have been performed with a switching frequency of 5 kHz, a DC-link voltage of 3 kV, and a power factor of 1 and -1 for the sending and receiving power modules, respectively.

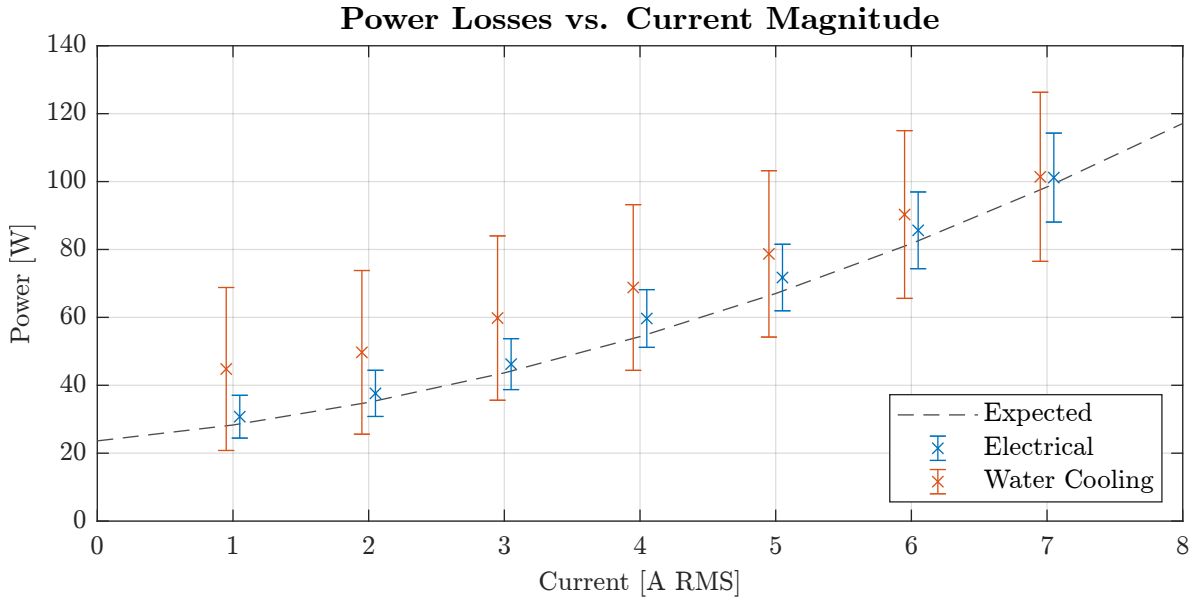


Figure 6.14: Power losses at different current magnitudes.

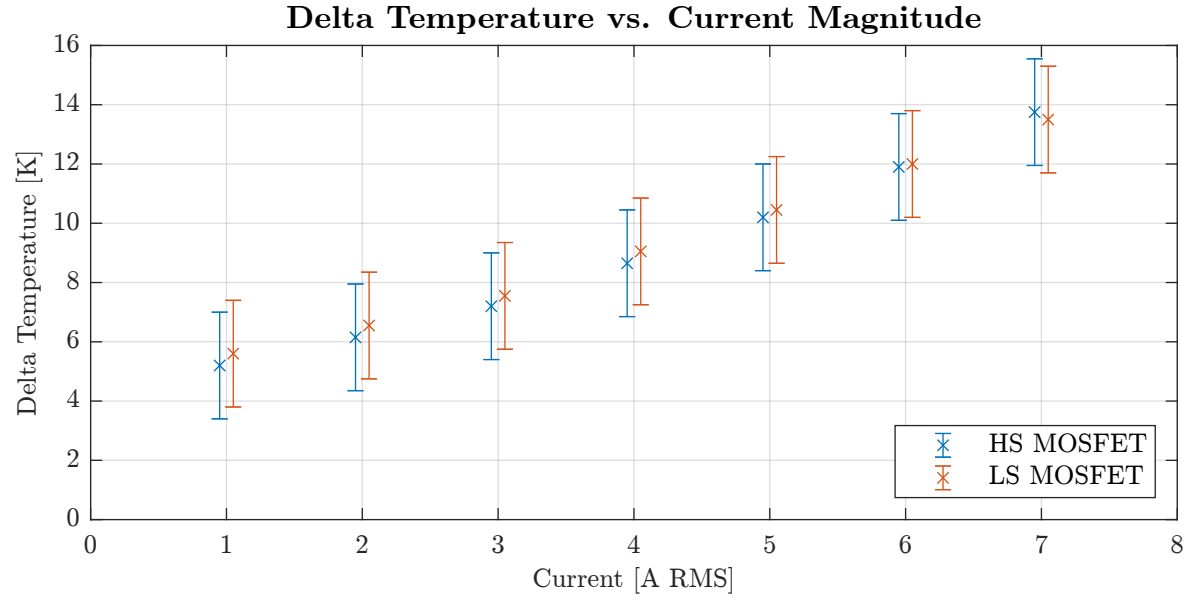


Figure 6.15: Delta die temperature at different current magnitudes.

From the above measurements, it can be noted that the estimated power stack losses from the electrical measurements are very close to their expected values. However, the losses derived from the water cooling measurements seem to be off at the lower end of the range. This is not unexpected as the absolute power loss, in this case, is extremely low compared to the measuring range of the water cooling system. It can be noted though that the uncertainty intervals of both measurements overlap, which should suggest that the true value lies somewhere within that overlap.

Varying Current Phase Angle

As both power modules are mounted on the same power stack utilizing the same integrated water cooling system and fed from the same DC power supplies, it is not possible to distinguish between the losses in each of the power modules when sweeping the current phase angle. However, the variation of losses in the MOSFET dies can be indirectly measured by measuring the MOSFET die temperatures. Even though not possible to estimate the exact power stack losses, it has been possible to measure a variation in the temperature of the MOSFET dies of the receiving power module as shown in Fig. 6.16. All of the measurements presented in the below figure have been performed with a switching frequency of 5 kHz, a DC-link voltage of 3 kV, and a load current of 7.0 A RMS. The phase angle has been varied in steps of 10 degrees, and therefore, the presented results are linked to the closest x-axis tick.

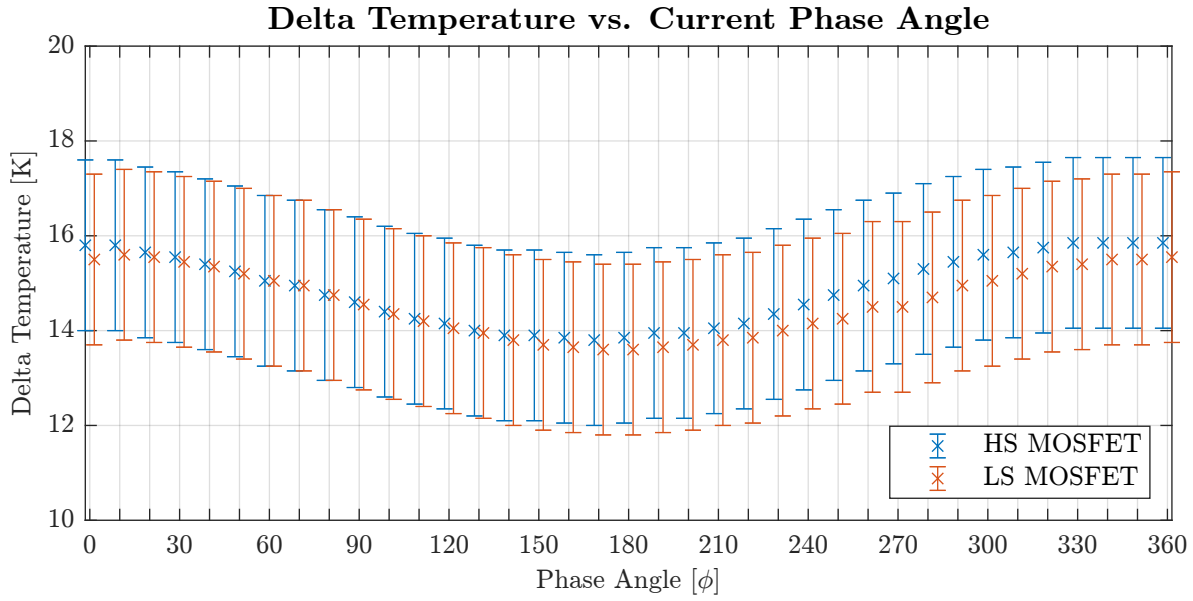


Figure 6.16: Delta die temperature for varying current phase angles.

From the above figure, it can be seen that the delta temperatures of the MOSFET dies are highest at phase angles of 0 and 360 degrees where the power module is operated at a power factor of 1. However, the trend is subject to a relatively high uncertainty as the absolute temperature variation is in the same range as the absolute uncertainty of the measurements.

6.9 Chapter Summary and Conclusion

This section presents a summary of the chapter and highlights the main findings presented throughout.

Prior to the actual experimental measurements of the losses, an overview of the expected losses in the system was presented with a description of how they could be assigned to different system components, and ultimately, how they could be measured in practice.

Following this, an analysis of the expected losses in the power modules was presented based on switching energy dissipation data from a double pulse test as presented in [3].

Hereafter, an analysis of the measurement uncertainty in the available equipment for the tests was made. Generally, the combined uncertainty of the measurements leading to the estimation of the power module losses have been found to be quite large. The actual uncertainties for the measurement points taken during this thesis are ranging from between 7% to 22% for the electrical measurements and 12% to 55% for the water cooling measurements.

The reason why the resulting uncertainties are so large is due to a combination of factors. The base uncertainty of the electrical measurements using the built-in voltage and current measurements of the DC power supplies can be as good as 0.4% at full utilization of the measuring range. For the water cooling system, the best achievable uncertainty at full range utilization is 1.55%.
However, due to the very low power module losses, the actual measurements have very low utilization of the range of the measuring equipment, which in turn causes the base uncertainties to be far from their ideal values at full range utilization.
Furthermore, as the power module losses are not measured directly but derived from the addition and/or subtraction of other measured quantities, the propagation of uncertainties in calculations means that the total uncertainties will be much higher than the base uncertainties of the equipment.

This chapter further includes the resulting estimates of the power module losses, which have been found to be in close agreement with expected losses derived based on the power modules' on-state resistance and results from a double pulse test performed on the modules in [3].
The estimated power stack losses from the measurements have shown close agreement with the expected losses for DC-link voltages below 3 kV. At a DC-link voltage of 3 kV, the resulting losses in the power stack for the electrical and water cooling measurements have been found to be 101 W ±13% and 101 W ±25%, respectively, compared to the expected losses of 100 W.
Above 3 kV the estimated power stack losses from the measurements have been found to be slightly elevated compared to their expected values. At a DC-link voltage of 6 kV, the resulting losses in the power stack for the electrical and water cooling measurements have been found to be 229 W ±8.3% and 225 W ±12%, respectively, compared to the expected losses of 206 W.

Chapter 7

Discussion

This chapter discusses the results obtained in the previous three chapters and highlights key findings and identified challenges.

The main goal of the thesis defined in the initial project stages was to demonstrate a closed loop current controller in the 6 kV medium voltage converter setup based on fast-switching SiC MOSFETs.

It was believed that this could provide valuable insight into the practical challenges associated with the implementation of closed loop control in such a medium voltage converter which could pave the way for integration of the converters into more complicated systems.

It was further envisioned that the resulting experimental setup, with the addition of the current controller, could be utilized for providing valuable test data of the power modules in operation. Specifically, in this thesis, the experimental setup has been used to map the power module losses for different operating conditions while monitoring their MOSFET die temperatures. The data provided from these tests could then be used for assessing whether it would be possible to increase the rated operating point of the power modules.

Challenges Related to Switching Noise

During the work on reconfiguring the experimental setup from its open loop configuration to a configuration which would support the implementation of the current controllers, a number of challenges were encountered.

A central challenge which was already identified in the 9^{th} semester's project leading into this thesis, was how to ensure the integrity of the feedback current signal. In the 9^{th} semester's project, the issue was addressed by analyzing and evaluating the switching noise in an off-the-shelf closed loop hall-effect current sensor and by proposing a sampling strategy to mitigate its effect [1], [2].

In the early stages of this thesis work, the proposed sampling scheme was implemented and tested. The sampling strategy was found to be useful in mitigating the disturbance from the converter switching noise on the feedback current signal, such that reliable measurements could be secured.

Another challenge which has been and still is a major obstacle to overcome is that of the switching noise from the converter interrupting the communication used for remote interfacing of auxiliary equipment in the experimental setup. These issues have been exclusively seen on the interfaces to the PC comprising the remote control of the medium voltage DC power supplies, the oscilloscope, the temperature measurements, and the remote debugger for the DSP as well. Importantly, only the interfaces have been seen to malfunction and no issues whatsoever have been experienced with the secure operation of the equipment themselves. These issues have been partly solved as explained in Section 4.3 by doing a careful layout of the auxiliary system and by decoupling the communication interfaces wherever possible to avoid the propagation of noise in between the signals. With these precautions, it has been possible to operate the converter at its rated conditions, however, the issues persist and need to be further addressed. Particularly as it is only expected to increase if more power modules are added, e.g. in the buildup of a three phase system.

Controller Implementation and Performance

The design of the current controller was initiated in the 9th semester's project considering a simulated three phase back-to-back converter setup. Due to the three phase layout, the converter was initially thought to be controlled in a *dq0* reference frame where the sinusoidal reference signals appear as DC values. Therefore, a PI controller was chosen as the obvious choice for the controller implementation. However, as it was later found in the risk analysis associated with this thesis work as presented in Chapter 3, the limited number of available power modules for the testing meant that it was considered a safer option to do the testing on a single phase setup.

Initially, it was decided to proceed with the PI controller design, even though it was known that it would not be able to control the sinusoidal reference currents without a steady state error. However, when the designed PI controller was used to operate the converter, it was found that it underperformed significantly compared to its design. This was identified to be caused by the dead time voltage error, and therefore, a compensation algorithm had to be implemented. The simple dead time compensation algorithm initially adapted turned out to introduce stability issues at low current references. Therefore, a more thorough investigation of the actual dead time voltage error present during the operation of the converter was initiated, and a more accurate dead time compensation algorithm was implemented based on the findings. This new compensation algorithm completely eliminated the instability issues while still retaining the benefits of having the dead time compensation at higher current references.

As the PI controller, even with the added dead time compensation, was still not able to fulfill its design requirements, it was decided to design and implement a PR controller to test whether better steady state performance could be achieved. A comparison of the performance of the PR controller to that of the PI controller showed that the steady state error for the fundamental harmonic component was completely eliminated, even without the need for compensating the dead time voltage error. The dead time compensation was found though to enhance the waveshaping properties and reduce the low order harmonic content of the current.

Power Module Losses

In Chapter 6, the goal was to perform a mapping of the power module losses for different operating points. However, an initial analysis of the expected losses and the accuracy of the available measuring equipment showed that the uncertainties associated with the experiments would become quite large. These uncertainties were partly affected by the very low power module losses which resulted in measurements being taken very low in the available range of the measuring equipment, which has a negative impact on the uncertainty. Furthermore, during the analysis of the losses on a systems level, it was found that the power modules were not the only loss contributors in the system. For the electrical measurements, the inductor losses would need to be subtracted to obtain the losses in the power modules. Similarly, for the measurement derived from the water cooling measurements, the heat transfer from the ambient surroundings into the cooling also needed to be subtracted to obtain the losses associated with the power modules. These subtractions introduce a propagation of uncertainty in the measurements which further impacts the uncertainty in a negative direction.

Furthermore, the subtracted losses arising from the inductor losses and the heat transfer from the ambient cannot be measured directly during the operation of the converter. These losses are therefore only estimated and the uncertainties associated with these estimations are difficult to quantize. For the water cooling system, the heat transfer from the ambient is dependent on both the inlet temperature, outlet temperature, and ambient temperature, which all change during operation, and the estimation is therefore subject to change. For the estimation of the inductor losses, only the losses at mains

frequency are considered and any losses associated with the current harmonics caused by pulse-width modulation and capacitive currents caused by high frequency switchings will not be included in the estimation.

The estimated power module losses resulting from the measurements have shown to be in good accordance with their expected values derived from the conduction losses calculated from the on-state resistance, and the switching losses based on the double pulse test from [3]. However, for DC-link voltages above 3 kV, the estimated losses from the measurements tend to be slightly elevated compared to the expected values. The explanation for this is likely multifaceted but the following two causes are identified as plausible reasons. Firstly, the on-state resistance has a positive temperature coefficient, meaning that it will increase with increasing temperatures. As the losses in the die increase with the increased DC-link voltage, so does the temperature and hence the on-state resistance. This will result in an underestimation of the conduction losses when the die temperatures begin to rise. Secondly, the switching losses will be impacted by the capacitive loading of the power modules. This includes the parasitic capacitances in all connected equipment and in the filter inductors, which have a terminal to terminal parasitic capacitance of 50 pF each. For the double pulse test, the parasitic capacitance of the filter inductor was only 12 pF [3]. This means that the capacitance is somewhat higher in the experimental setup utilized for this thesis, and therefore, the switching losses are also expected to be elevated compared to the results from the double pulse test.

An important objective of the tests of the power modules was to provide data to assess whether a possible increase in the rated operating point could be proposed. To propose an increase in the rated operating point with some amount of confidence two things needed to be fulfilled. Firstly, the estimated power module losses should be within a reasonable range of their expected values, indicating that the power modules are operating as per their design requirements. Secondly, and perhaps more importantly, the MOSFET die temperatures should not exceed their safe operating area. The exact boundaries of the safe operating area are not known, but die temperatures up until at least 120°C should be permissible. However, the MOSFET die temperature is not the only limiting factor. It is important that the current through the MOSFET does not cause it to enter saturation. Yet, with dies rated for 20 A of continuous drain current, there is still a respectable margin from the present ratings of 7 A RMS for the power modules.

Chapter 8

Conclusion

This chapter concludes the thesis by revisiting the vision presented in the introduction. The thesis was envisioned to demonstrate the operation of a single phase closed loop current controller in a medium voltage power converter comprising state-of-the-art power modules enabled by 10 kV SiC MOSFETs.

This has been achieved partly due to the successful evaluation of the sampling scheme proposed in [1], [2]. Based on the experiments conducted and documented in Section 5.1, the sampling scheme was found to be effective in mitigating the switching noise introduced into the sensing circuit from the high $\mathrm{d}v/\mathrm{d}t$ present in the converters' output voltage.

With the integrity of the current feedback ensured by the adoption of this strategy, a PI current controller has been implemented and tested in the experimental setup. The performance of the PI controller was found inferior to its design criteria which was identified to be partly due to the converter dead time voltage error. Therefore, a dead time compensation algorithm has been developed based on an experimental determination of the actual dead time voltage error as a function of the load current. This dead time compensation algorithm restored the PI controllers' performance to be close to its design requirements.

In an effort to increase the control loop performance further, a PR controller was implemented and tested. The PR controller has been shown to have superior steady state performance with unity gain at the fundamental harmonic component compared to 0.93 for its PI counterpart. Further, the PR controller has low harmonic distortion with an evaluated THD_{50} of 4.67% at its rated operating point of 6 kV DC-link voltage and 7 A RMS load current. The harmonic distortion is mainly present at the 3^{rd} and 5^{th} harmonics, which constitute 4.21% and 1.26%, respectively. The PR controller was therefore chosen as the preferred solution - meeting the main project vision of demonstrated closed loop current control in the medium voltage converter setup.

Upon realization of the main vision, the experimental setup has been utilized to evaluate the performance of the power modules at different operating points. Estimates of their losses have been derived based on both electrical and water cooling measurements. At the same time, the MOSFET die temperatures have been monitored for all the tested conditions.

The resulting estimates of the power module losses have been found to be in close agreement with the expected losses derived based on results from a double pulse test performed on the modules in [3] and the power modules' on-state resistance.
The estimated power stack losses from the measurements have shown the closest agreement with the expected losses for DC-link voltages below 3 kV. At a DC-link voltage of 3 kV, the resulting losses in the power stack for the electrical and water cooling measurements have been found to be 101 W ±13% and 101 W ±25%, respectively, compared to the expected losses of 100 W.
Above 3 kV the estimated power stack losses from the measurements have been found to be slightly elevated compared to their expected values. At a DC-link voltage of 6 kV, the resulting losses in the power stack for the electrical and water cooling measurements have been found to be 229 W ±8.3% and 225 W ±12%, respectively, compared to the expected losses of 206 W.

The measured MOSFET die temperatures have been low for all of the operating points with an absolute high of less than 50°C at rated operating conditions of 6 kV DC-link voltage, 5 kHz switching frequency, and 7 A RMS of load current with coolant inlet temperature in the range of 10°C to 15°C.

It has not yet been possible to conclude upon the hypothesis that the rated operating point of the power modules can be increased. However, the very low die temperatures measured during testing at the present rated operating point is a strong indication of the likelihood of the hypothesis being true. However, further experiments at 6 kV DC-link voltage are needed before the hypothesis can be finally accepted or rejected.

Chapter 9

Future Work

This chapter includes an overview of suggested future work within the context of this thesis.

First and foremost, as the final hypothesis, which states that the rated operating conditions of the power modules could likely be increased, has yet to be accepted or rejected, efforts should be made to reach a final conclusion. To do so, it is recommended to conduct further experiments at a DC-link voltage of 6 kV. More specifically, it is suggested that the measurements performed in this thesis at the capped DC-link voltage of 3 kV with varying load currents and switching frequencies are repeated at the 6 kV DC-link voltage level.

It is also suggested that the method used to estimate the power module losses in this thesis could be revised. It is known that the temperature dependency of the drain-source on-state resistance will give some additional conduction losses which have not been accounted for. It is further suggested that the simulation model presented in [3], which includes the power module parasitics, could be adapted in a modified version for this setup to account for the higher parasitic capacitance of the filter inductors and rerun to obtain a more accurate estimation of the switching energy dissipation.

Another suggestion could be to reduce the harmonic content in the controlled current waveforms. As it has been seen in the frequency domain analysis of the resulting current from the PR controller, the harmonic content was predominantly present in the 3^{rd} and 5^{th} harmonics. Therefore, it could be a valuable option to introduce dedicated compensation at these two frequencies in the control loop.

The issues related to the interruption of the communication signals in the experimental setup due to the EMI caused by the high $\mathrm{d}v/\mathrm{d}t$ of the SiC MOSFETs, though temporarily solved by the initiatives described in Section 4.3, need to be further addressed to achieve higher reliability of the interfaces.

Finally, even though the proposed sampling scheme has shown to be effective in mitigating the effect of the noise present in the current sensor due to the fast switching of the SiC MOSFETs, the underlying principle behind the behavior of the noise is not yet fully understood. As explained in Section 1.2, the noise model developed in the 9^{th} semester's project is able to predict the noise present during the actual switching transients but does not predict the slower acting response which is seen in practice. It is believed that this part of the noise is due to the parasitic coupling to the hall element and its amplification circuit and that further efforts in modeling this part of the sensor could provide a better understanding of its behavior, which in turn could lead to the discovery of some preventive measures. Though not strictly necessary for this project at present, a more detailed understanding of noise in current sensors for medium voltage applications could be a valuable contribution to the power electronics community.

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Appendix A

Design and Implementation of DSP

This appendix includes a description and an overview of the digital implementation of the DSP using Code Composer Studio 11.1.0. The DSP used is a TMDSCNCD28379D from Texas Instruments [29] placed in a DSP interface board. A photograph of the DSP card and DSP interface board can be found in Chapter 2. Throughout this appendix, the technical reference manual [40] is used as a reference.

A.1 Coding Structure

The coding is structured in two layers, where the top layer includes the main functionality, including the *main()* and interrupt service routine (ISR), whereas all the secondary utility functionality is included in the bottom layer. Both layers are described in detail in the following sections.

A.1.1 Top Layer

The top layer describes the overall coding structure. The code is structured in two parts: *main()* and ISR. The *main()* is implemented as a state machine, whereas the ISR is implemented with a sequential flow. A flowchart of the state machine implemented in *main()* is shown in Fig. A.1.

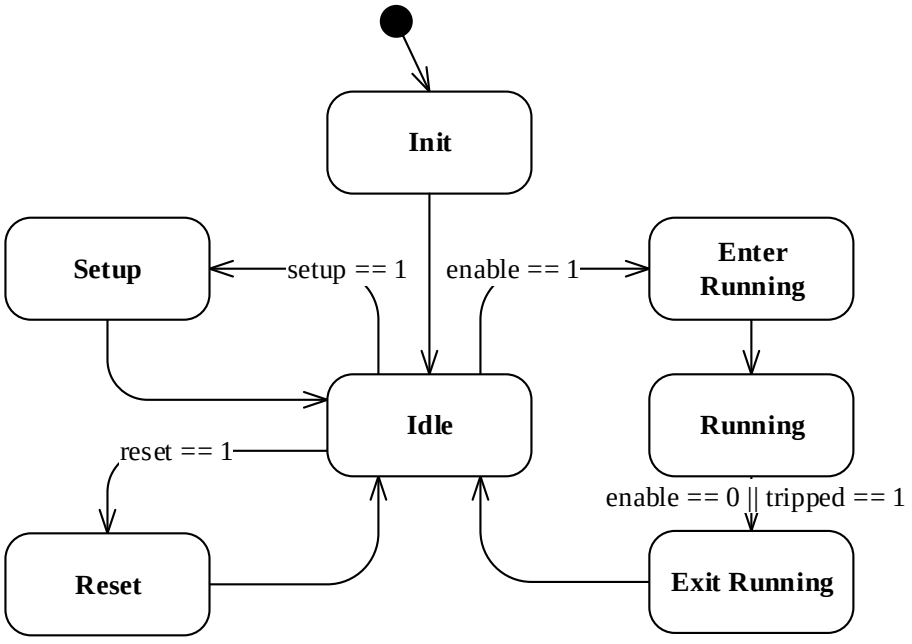

Figure A.1: Flowchart of the state machine running in *main()*.

The state machine contains several states which are briefly described below:

Init: The initialization state sets the overall system variables. This includes the control mode (debug, open loop, or closed loop), current sample (measurement or simulation), discrete controller type (PI

or PR controller), etc. The initialization state sets the setup bit.

Idle: The idle state loops continuously and polls the setup, reset, and enable flags.

Setup: The setup state sets up the DSP based on the system variables set in the initialization state. This includes the SPI, PWM, interrupt, discrete plant and controller, PIF card, and data logger. The setup bit should be set high after a reset.

Reset: The reset state resets the DSP variables to default values. This includes the SPI, discrete plant and controller, PIF card, and data logger.

Enter running: The enter running state puts the DSP into its running state. This state includes setting the PIF card into its Run state and enabling interrupts on the DSP.

Running: The running state checks if any error flag is being raised in the ISR. If an error flag is raised, the state machine transitions into its exit running state. The functionality while running is dedicated to the ISR.

Exit running: The exit running state disables interrupts on the DSP and puts the PIF card into its Ready state.

The main functionality is implemented in the ISR, which is executed with a frequency of 10 kHz. The PWM used to generate the interrupts has a frequency of 5 kHz, however, the interrupt is being generated both on a ZERO and PERIOD compare event. A flowchart of the sequential flow of the ISR is shown inf Fig. A.2.

On a ZERO compare, the ISR requests the ADCs on the PIF card to make a conversion and to transmit the data over the SPI bus. Further, the implemented discrete plant is being simulated with the previously updated duty cycles.

On a PERIOD compare, the ISR likewise requests the ADCs on the PIF card to transmit its data. Afterward, the proposed sampling scheme is used to select the current sample based on the previously updated duty cycle. One of the three control modes (debug, open loop, or closed loop) is then executed to calculate a new set of duty cycles for the converter. Before updating the PWM with the new duty cycles, a safety check is performed to check for conditions that should issue a trip event.

A.1.2 Bottom Layer

The bottom layer contains four objects, where each object is responsible for a specific functionality. An object is defined as a header and source file. The four objects are spiADC, setup, reset, and project.

Object spiADC

The spiADC object is responsible for the SPI functionality used to communicate with the ADCs on the PIF card. This includes the timings requirements of the ADC, a measuring procedure of the ADC offset and SNR, conversion of the data received in 2's complement, and synchronization of the ADCs. A more detailed description of the working principle behind the ADC can be found in Chapter 4 and the datasheet of the ADC [39].

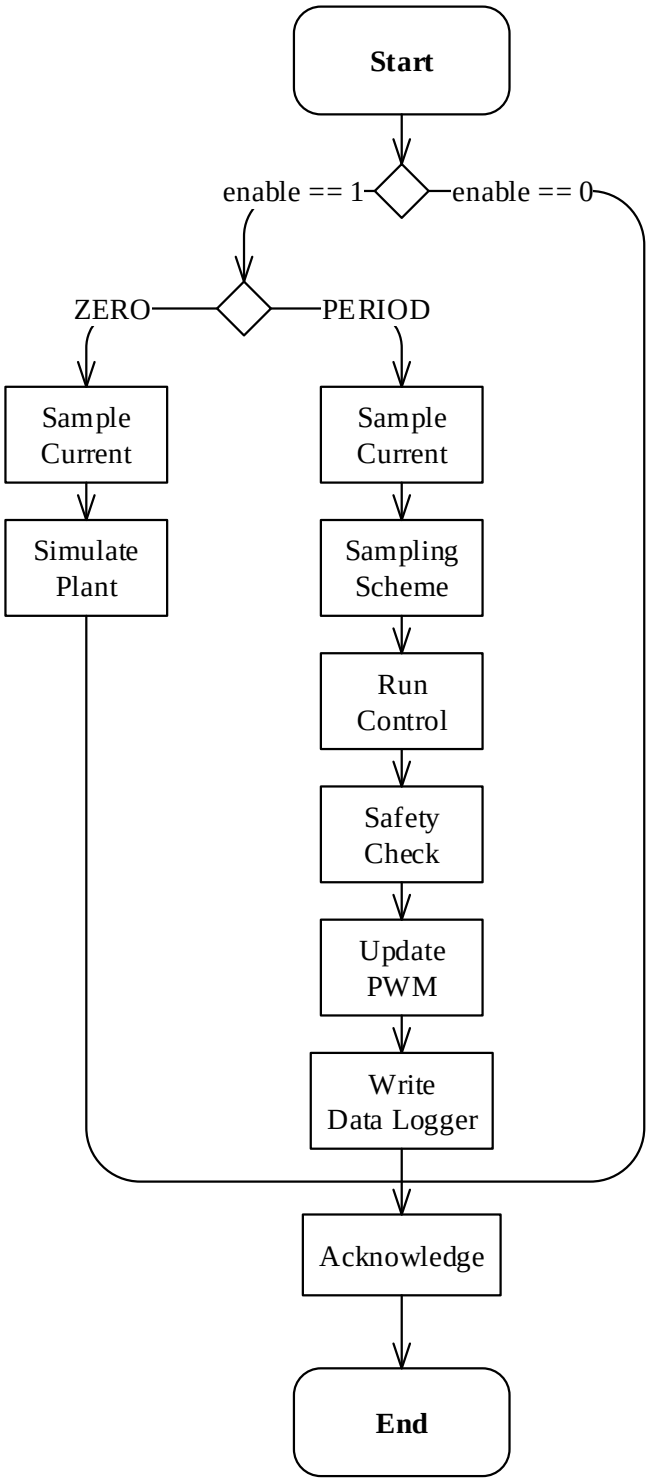

Figure A.2: Flowchart of the interrupt service routine.

Object setup

The setup object contains all of the constant system variables and the functions executed in the setup state. A brief explanation of the setup functions is given below:

setupGPIO(): The GPIO setup function sets up the GPIOs as shown in Table A.1. The GPIO pins are not directly connected to the optical transmitters/receivers (TR) on the DSP interface board. The connection will need to be established in the hardware by use of jumpers or wires, which gives an added degree of layout flexibility. Notice that GPIO17 and GPIO18 and TR17 and TR18 are crossed. Refer to Chapter 8 in the technical reference manual [40] for further explanation.

Table A.1: Setup of the GPIO.

Signal	GPIO	TR	I/O	Description
PWM A	0	0	O	PWM signal to power module 1
PWM B	2	2	O	PWM signal to power module 2
EN	8	8	O	Enable to PIF card
CS	11	11	O	Chip Select to PIF card
MKS	14	14	O	Manual Kill Switch signal to PIF card
CONVST RD	16	16	O	Conversion Start and Read to PIF card
SDOA	17	18	I	Serial Data Out A from PIF card
CLK	18	17	O	Clock to PIF card
MASTER EN	19	19	I	Master Enable from PIF card
MKS	23	23	I	Manual Kill Switch signal from kill switch
CPU BUSY	40	-	O	CPU Busy signal. High during interrupt
DL TRIGGER	41	-	O	Data Logger Trigger. High during data logging

setupPWM(): The PWM setup function sets up the two PWM modules as shown in Table A.2. Refer to Chapter 15 in the technical reference manual [40] for further explanation.

Table A.2: Setup of the PWM modules.

Register	EPWM1	EPWM2
Period load mode	Shadow	Shadow
TB counter mode	UP/DOWN	UP/DOWN
TB period	10.000	10.000
Phase shift load	Disable	Enable
Sync out pulse mode	Counter ZERO	EPWM1 Sync
Count mode after sync	-	Count UP
CC shadow load mode	ZERO	ZERO
AQ action high	DOWN CMP	DOWN CMP
AQ action low	UP CMP	UP CMP

setupInterrupt(): The interrupt setup function sets up the interrupt handled by the ISR. The interrupt source is set as EPWM1 and an interrupt is being generated both on a ZERO and PERIOD compare event. The ISR is executed on each interrupt event. Refer to Chapters 3.4 and 15 in the technical reference manual [40] for further explanation.

setupSPI(): The SPI setup function sets up the SPI module as a master with an internal oscillator clock at 50 MHz, a baud rate of 12.5 Mbit/s, and a data width of 16 bits. The SPI protocol uses a polarity and phase of 0. Refer to Chapter 18 in the technical reference manual [40] for further explanation.

setupSystem(): The system setup function initializes the system variables to known values and sets up the parameters for the discrete plant and controllers. A detailed description of the implementation of the discrete plant and controllers is given in Section A.2.

Object reset

The reset object contains the functions executed in the reset state. The reset object only includes the functionality of resetting the DSP variables to their default values.

Object project

The project object contains the functionality which is not included in the three previously described objects. Therefore, the project object contains many different functionalities, some of which are a simulation of the discrete plant, initialization of the PIF card, proposed sampling scheme, three control modes, safety check, and utility functions needed for the data logger. A brief explanation of the key project functions is given below:

simulatePlant(): The discrete plant is implemented as a difference equation describing the single phase setup as described in Section A.2. The function takes the requested voltage across the plant as an input, updates the variables of the difference equation, and outputs the resulting current.

initPIF(): The PIF card will under normal operation conditions be either in its Fault or Ready state and with the current design of the PIF card, it is not possible for the DSP to know which state the PIF card is in. Therefore, the enabling sequence implemented in the DSP is designed in such a way that it in both cases will put the PIF card into its Run state.

samplingScheme(): The proposed sampling scheme is a double sampling, single update scheme based on the previous duty cycle. For a duty cycle above 50%, the current sample at the ZERO compare event is chosen, and for a duty cycle below 50%, the current sample at the PERIOD compare is chosen.

runControl(): The run control function includes the execution of the three control modes: debug, open loop, and closed loop. In debug mode, the duty cycles are set to 50% to have no current flow. In open loop, the duty cycles are calculated based on voltage references defined by a modulation index and phase angle. In closed loop, the duty cycles are calculated from the closed loop current controller (either PI or PR controller) based on the current reference and chosen current sample.

safetyCheck(): The safety check contains three protective software functionalities to prevent the converter from causing damage. The functionalities are 1) A manual kill switch has been designed to be able to shutdown the DSP in a safe manner if the connection is lost, 2) A overcurrent protection that takes both the measured and simulated currents into account, and 3) A safety measure that checks if the duty cycle difference between the sending and receiving converter exceeds a certain limit.

writeDataLog(): The data logger writes a certain amount of data directly in the global shared ram of the DSP by setting a data logger bit high. When the data logger bit is set, the data logger puts GPIO41 (DL TRIGGER) high at the next coming ZERO compare event such that measurements on an oscilloscope easily can be aligned with the data logged in the DSP ram. Refer to Chapter 3.11 in the technical reference manual [40] for further explanation of the global shared ram.

A.2 Digital Implementation of Plant and Controllers

A description of the implementation procedure for the discrete plant and current controllers is given in this section.

A.2.1 Discrete RL Plant

The implementation of the discrete RL plant takes a starting point in the transfer function of the RL plant in the continuous time domain, known to be given by (A.1).

$$G(s) = \frac{Y(s)}{U(s)} = \frac{1}{R + Ls} \tag{A.1}$$

where $G(s)$ is a transfer function, $Y(s)$ is an output, and $U(s)$ is an input. Transforming the continuous time transfer function into its standard form of a 1st order discrete transfer function using the bilinear z-transformation *(also known as tustin or trapezoidal)* yields (A.2).

$$G(z) = \frac{Y(z)}{U(z)} = G(s)|_{s=\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}} = \frac{1}{R + L\left(\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}\right)} = \frac{\frac{T}{2L}\left(1+\frac{TR}{2L}\right) + \frac{T}{2L}\left(1+\frac{TR}{2L}\right)z^{-1}}{1 + \left(\frac{TR-2L}{TR+2L}\right)z^{-1}} \tag{A.2}$$

The standard form of a 1st order discrete transfer function can be converted into its 2nd order time-invariant difference equation. By cross multiplication and the inverse z-transformation, the difference equation and its inverse z-transform *(shown with T omitted)* yield to (A.3).

$$\begin{aligned} Y(z) =& \frac{1}{a_0}\left[b_0 \cdot U(z) + b_1 \cdot U(z) \cdot z^{-1} - a_1 \cdot Y(z) \cdot z^{-1}\right] \Rightarrow \\ Y(k) =& \frac{1}{a_0}\left[b_0 \cdot U(k) + b_1 \cdot U(k-1) - a_1 \cdot Y(k-1)\right] \end{aligned} \tag{A.3}$$

where the coefficients are given as in (A.4).

$$a_0 = 1 \qquad a_1 = \frac{TR-2L}{TR+2L} \qquad b_0 = \frac{T}{2L}\left(1+\frac{TR}{2L}\right) \qquad b_1 = \frac{T}{2L}\left(1+\frac{TR}{2L}\right) \tag{A.4}$$

The function that sets up the parameters for the discrete plants, *setupSystem()*, uses the coefficients found in (A.4), whereas the functions that simulates the discrete plant, *simulatePlant()*, updates the variables of the difference equation using (A.3).

A.2.2 Discrete PI Controller

The PI controller is implemented using the available Digital Control Library (DCL) from Texas Instruments [52]. The chosen PI parameters are based on the analysis made in the previous semester's project [1], where K_P was found to be 40 and K_I to be 467 to achieve a desired rise time of 3 ms. However, due to the structure of the integrator term of the PI controller from the DCL library, the K_I needs to be multiplied with the switching time period to achieve a correct performance. As shown in the figure, the integrator term is implemented using the backward Euler method. The full structure of the implemented PI controller is shown in Fig. A.3.

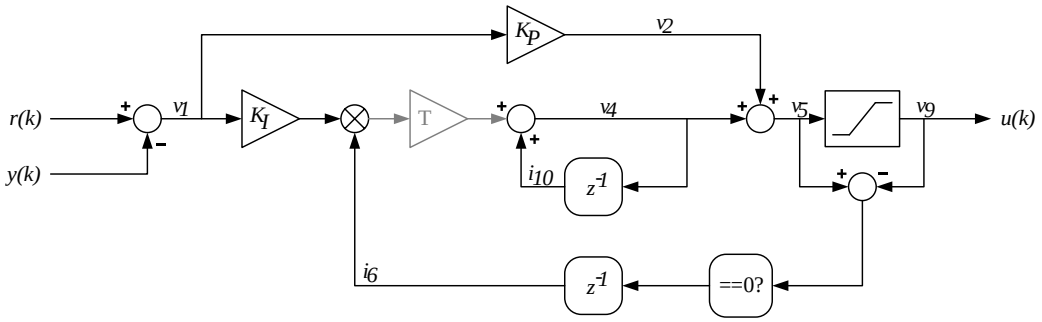

Figure A.3: Structure of the PI controller [52]. *Black: Structure from DCL, Grey: Correction.*

As shown in the figure, some intermediate calculations are marked with v_x, which are being used to convert the figure into c-code. The function from the DCL library which executes the PI controller can be described by the intermediate calculations. First, the error v_1 is found by:

$$v_1 = r(k) - y(k) \tag{A.5}$$

The proportional output of the PI controller can then be found by:

$$v_2 = v_1 \cdot K_P \tag{A.6}$$

And the integral output of the PI controller can then be found by:

$$v_4 = v_1 \cdot K_I \cdot i_6 \cdot T + i_{10} \tag{A.7}$$

where i_6 is a boolean value used for anti windup, i_{10} is the previous integral output, and T is the switching time period. After calculating the current integral output, v_4, the value is then stored in i_{10} for the next calculation. The total output of the PI controller can then be found by:

$$v_5 = v_2 + v_4 \tag{A.8}$$

The last part of the figure includes the saturation of the PI controller output. If the upper and lower saturation limits are not exceeded, the anti windup boolean i_6 is set to 1, however, if one of the limits is exceeded, i_6 is set to 0.

The used c-code for the PI controller is shown in Listing A.1.

```
//#############################################################################
// FILE:            project.c
//#############################################################################
float DCL_runPI(DCL_PI *p, float rk, float yk)
{
    float v1, v2, v4, v5, v9;

    v1 = rk - yk;
    v2 = v1 * p->Kp;
    v4 = (v1 * p->Ki * p->i6 * T) + p->i10;
    p->i10 = v4;
    v5 = v2 + v4;
    v9 = (v5 > p->Umax) ? p->Umax : v5;
    v9 = (v9 < p->Umin) ? p->Umin : v9;
    p->i6 = (v5 == v9) ? 1.0f : 0.0f;

    return(v9);
}
```

Listing A.1: Implementation of PI controller.

A.2.3 Discrete PR Controller

The previously used DCL library for the PI controller does not include a PR controller, which meant that one needed to be implemented. The PR controller is implemented using the same procedure as the one described for the PI controller, however, it has been chosen to implement the direct integrator using the forward Euler method and the feedback integrator using the backward Euler method [53]. Similar parameters are chosen for the PR controller with the only difference that K_I has been increased with a factor of five to achieve faster dynamic performance. The full structure of the implemented PR controller is shown in Fig. A.4.

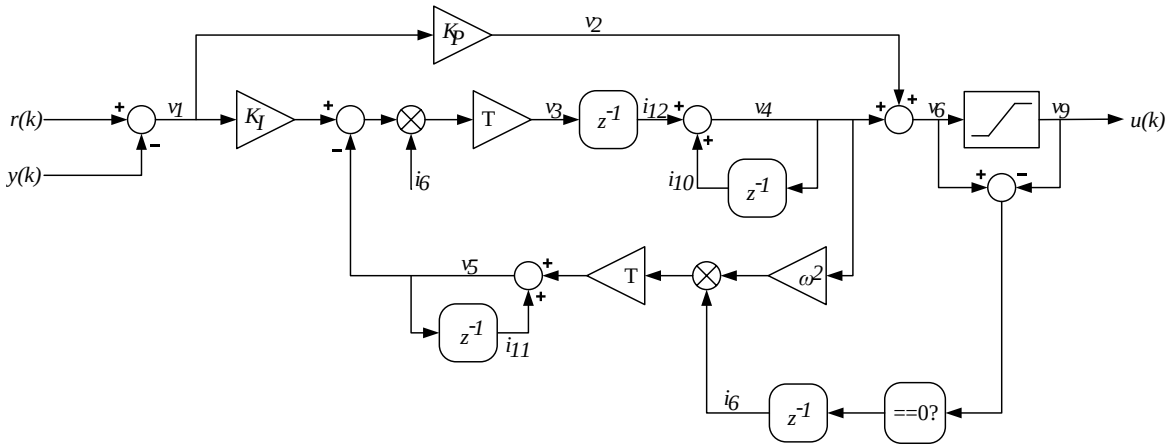

Figure A.4: Structure of the PR controller.

The implemented function which executes the PR controller can likewise be described by the intermediate calculations. Again, the error v_1 is found by:

$$v_1 = r(k) - y(k) \tag{A.9}$$

The proportional output of the PR controller can then be found by:

$$v_2 = v_1 \cdot K_P \tag{A.10}$$

However, the resonant output of the PR controller is not as easily found as was the case for the PI controller as it depends on the implementation of the direct and feedback integrators. In this case, it is found that the direct integrator output can be found by:

$$v_4 = i_{10} + i_{12}; \tag{A.11}$$

And the feedback integrator output can be found by:

$$v_5 = i_{11} + v_4 \cdot \omega^2 \cdot i_6 \cdot T \tag{A.12}$$

where i_6 is still the boolean value used for anti windup, i_{10} is the previous direct integral output, i_{11} is the previous feedback integral output, i_{12} is a previous intermediate calculation, and T is the switching time period. The intermediate calculation of v_3 is found as:

$$v_3 = (v_1 \cdot K_I - v_5) \cdot i_6 \cdot T \tag{A.13}$$

The total output of the PR controller can then be found by:

$$v_6 = v_2 + v_4 \tag{A.14}$$

The last part of the figure includes the saturation of the PR controller output. If the upper and lower saturation limits are not exceeded, the anti windup boolean i_6 is set to 1, however, if one of the limits is exceeded, i_6 is set to 0.

The implemented c-code for the PR controller is shown in Listing A.2.

```
//#########################################################################################
// FILE:                project.c
//#########################################################################################
float DCL_runPR(DCL_PI *p, float rk, float yk)
{
    float v1, v2, v3, v4, v5, v6, v9;

    v1 = rk - yk;
    v2 = p->Kp * v1;
    v4 = p->i12 + p->i10;
    v5 = (v4 * W_SQUARED * p->i6 * T) + p->i11;
    v3 = ((v1 * p->Ki) - v5) * p->i6 * T);
    p->i10 = v4;
    p->i11 = v5;
    p->i12 = v3;
    v6 = v2 + v4;
    v9 = (v6 > p->Umax) ? p->Umax : v6;
    v9 = (v9 < p->Umin) ? p->Umin : v9;
    p->i6 = (v6 == v9) ? 1.0f : 0.0f;

    return(v9);
}
```

Listing A.2: Implementation of PR controller.

At last, the bode plot for the continuous and discrete implementations of the PR controllers is shown in Fig. A.5. The figure compares the different discrete implementations considered during the implementation process.

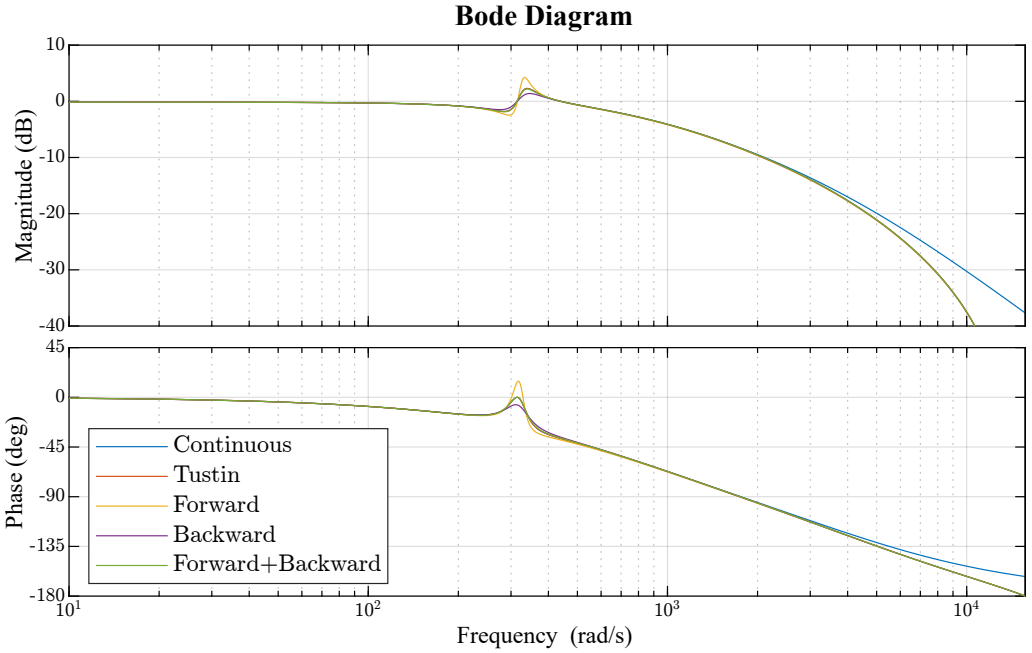

Figure A.5: Bode plot of PR controller. Comparison of discrete implementations.

Appendix B

PIF card

This appendix explains the design choices made related to scaling, ADC resolution, and hardware protection of measurement signals on the PIF card utilized in the experimental setup.

The PIF card is designed to include both a differential isolation amplifier for isolation purposes, a subsequent differential amplifier for scaling the input signals for better utilization of the resolution of the ADC, and an additional comparator used for protective functions.

B.1 General Structure of Scaling and ADC

The PIF card is laid out to provide a total of eight measurement channels to allow for taking three phase current, three phase voltage, and two DC-link voltage measurements. To achieve this, onboard hardware uses a total of eight isolation amplifiers, eight differential amplifiers, and two four-channel (2+2) ADCs. The digital outputs of the ADCs are multiplexed out on an SPI bus for optically isolated serial communication with the DSP. The overall architecture of the PIF card related to scaling and ADCs is shown in Fig. B.1

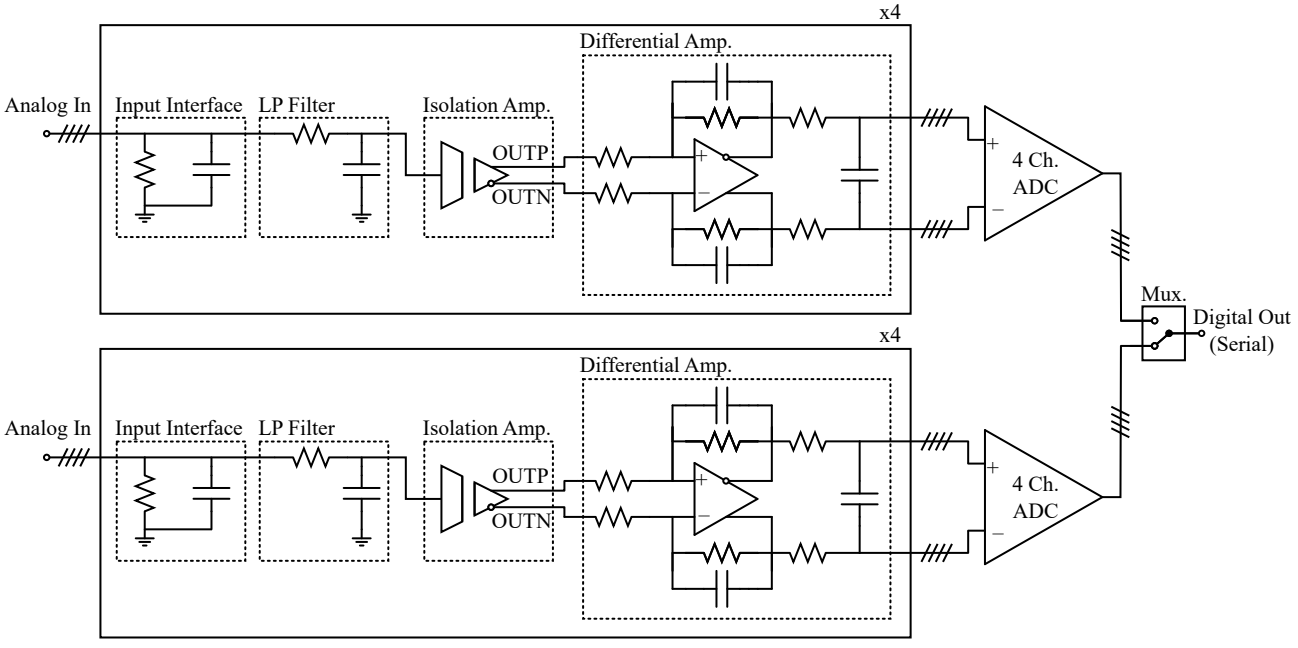

Figure B.1: Overall architecture of PIF card related to scaling and ADCs.

Starting from the top left, the two x4 duplicate blocks each consist of an input interface with the possibility of adding a measuring resistor for conversion from current to voltage signals as well as a smoothing capacitor. Then follows an optional block with an RC low pass filter before the signal reaches the input of the isolation amplifier (ISO224BDWV [54]) with differential output. The differential output is fed to a differential amplifier (LMP8350 [55]) where the gain can be configured by the design

of the input and feedback resistors. The 2x4 differential output signals from the differential amplifiers are then fed to the two separate four channel 12 bit ADCs (ADS7863A [39]) which output their sampled signals via an SPI bus. The output from the ADCs is multiplexed onto one SPI bus with the aid of a chip select pin.

B.2 Phase Current Measurements

This subsection will provide in detail the choice of scaling resistors and filtering capacitors for the blocks in the analog interface described in Section B.1 and depicted in Fig. B.1.

Input Interface

The current measurements are to be taken with a LEM LA 55-P [38] current sensor, which outputs a current signal proportional to the measured current and has a turn ratio N_p/N_s of 1:1000. This output current signal can be converted into a voltage signal by the use of the measuring resistor.

The current sensor has a nominal primary RMS current of 50 A. As the rated RMS current of the power modules used in this thesis is 7 A, corresponding to a roughly 10 A peak - only a fraction of the nominal input range of the current sensors will be utilized, which needs to be taken into account in choosing an appropriate value for this measuring resistor. To allow for the measuring range to be wide enough to provide a good margin to the rated current and to allow for measuring overcurrent events without clipping the measurements, the scaling circuitry will be designed to allow for the measurement of peak currents of 20 A.

For an ambient temperature not exceeding 70°C with ±15 V supply for the LEM LA 55-P, the maximum allowable value for the measuring resistor is 160 Ω. As the desired 20 A measuring range is in the low end of the range for the LEM LA 55-P, a relatively high measuring resistor of 150 Ω will be chosen for the design of the input interface of the current measurement channels. The reason for choosing a 150 Ω over 160 Ω will become apparent when taking into account the gains of subsequent blocks in the PIF card. In the initial design, no filtering capacitor will be inserted in the input interface.

Choosing this value for the measuring resistor will give a resultant output voltage of 150 mV/A in the primary circuit. This will give a total output of 3 V for a 20 A measurement.

LP Filter

The LEM LA 55-P current sensor has a listed -1 dB bandwidth up to 200 kHz. The RC low pass filter should be designed to filter out any high frequency noise from the signal without adversely affecting the bandwidth of the measurement system. It will therefore be designed with a bandwidth of around 250 kHz. This should be achieved by considering a practical value for the capacitor and a reasonable high resistance such that the filter does not load the input interface.

Choosing a capacitor of 220 pF and a resistor of 2.7 kΩ results in a cutoff frequency of approximately 268 kHz as shown in (B.1).

$$f_{c,I} = \frac{1}{2\pi RC} = \frac{1}{2\pi \cdot 2.7\ \text{k}\Omega \cdot 220\ \text{pF}} \approx 268\ \text{kHz} \tag{B.1}$$

Isolation Amplifier

The isolation amplifier has a gain of 1/3. This will result in an attenuation of the 150 mV/A from the LEM LA 55-P and the input interface to 50 mV/A (differential) after the isolation amplifier, which

results in 1 V/20 A. The output is a differential voltage signal and is the difference between V_{OUTP} and V_{OUTN} with the common mode output voltage V_{CMout} at VDD/2 as shown in Fig. B.2.

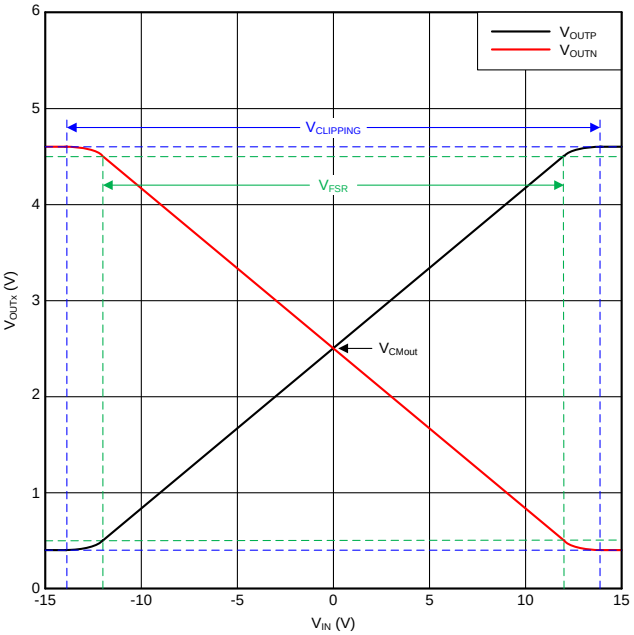

Figure B.2: Relation between input and output voltages for the ISO224 [54].

Differential Amplifier

The differential amplifier should scale the output signal from the isolation amplifier such that the bit resolution from the ADC can be optimally utilized. The ADC can handle differential inputs of ±2.5 V with its reference voltage set to the internal reference voltage of VDD/2 for a 5 V supply voltage. This means that to utilize the full range, the 1 V/20 A from the output of the isolation amplifier needs to be scaled to 2.5 V/20 A i.e. with a gain of 2.5. This can be achieved by using the differential amplifier in its typical fully-differential mode as shown in Fig. B.3.

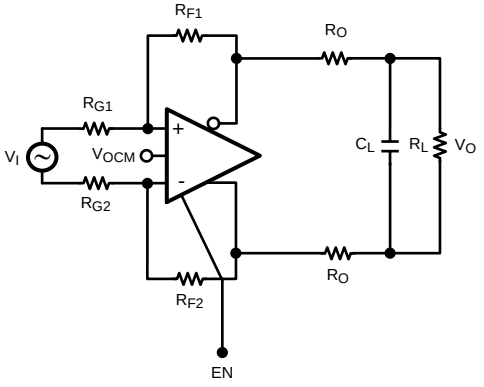

Figure B.3: Typical fully-differential coupling of the LMP8350 [55].

In this configuration, the differential amplifier provides a gain of:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{R_F}{R_G} \tag{B.2}$$

where

$$R_F = R_{F1} = R_{F2} \qquad \text{and} \qquad R_G = R_{G1} = R_{G2} \tag{B.3}$$

With this, the desired gain of 2.5 can be achieved by choosing R_F to 3 kΩ and R_G to 1.2 kΩ.

ADC Bit Resolution

The previous design choices combine to give an input voltage to the ADC of 2.5 V/20 A which gives a total measurement range of ±20 A for the ADC. With the available 12 bits from the ADC, one of which is used for the sign bit, this gives a final resolution of:

$$I_{res} = \frac{\pm 20 \text{ A}}{2^{12} \text{ bit}} = \frac{40 \text{ A}}{4096 \text{ bit}} \approx 9.766 \frac{\text{mA}}{\text{bit}} \tag{B.4}$$

Overcurrent Protection

Also included on the PIF card is a hardware comparator for over- and undercurrent protection as shown in Fig. B.4. The threshold values and hysteresis levels can be set by appropriate choices of resistors in the circuit.

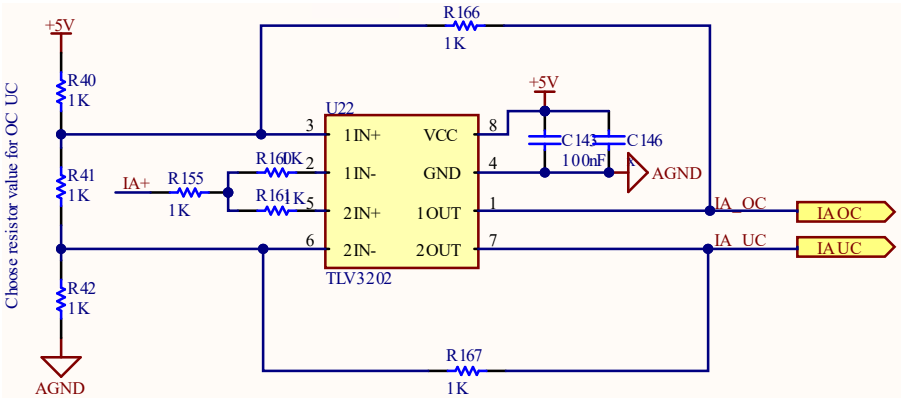

Figure B.4: Comparator circuitry for over- and undercurrent protection.

However, as the overcurrent alarms are latched in the CPLD by default, the system will need to be powered down and reset before an overcurrent alarm can be cleared. Therefore, there will be no need for including the hysteresis, unless specific requirements arise later. The feedback resistors, R_{166} and R_{167}, will therefore be omitted, and the overcurrent protection will be employing a simple comparison of the positive end of the differential amplifier output with a voltage divider that provides the desired threshold levels.

The overcurrent protection is made to clear any event where the current suddenly rises to undesired values and is not meant for detection of continuous operation above rated current, as this will be taken care of in the controls software. Therefore, the overcurrent protection thresholds should be set with a reasonably large margin to allow for momentary operation slightly above rated current. The thresholds will be set at 150% of rated current, i.e. ±15 A.

As the over- and undercurrent protection uses the positive output of the isolation amplifier as its input signal, the voltage at the pin can be described as a function of the primary current as follows:

$$V_{IC+}(I_P) = \frac{VDD}{2} + \frac{1}{2} \cdot 50 \frac{\text{mV}}{\text{A}} \cdot I_P \tag{B.5}$$

Therefore, to have overcurrent protection at 15 A, the upper threshold V_{A+} should be chosen to be:

$$V_{A+} = 2.5\ \text{V} + 25\ \frac{\text{mV}}{\text{A}} \cdot 15\ \text{A} = 2.875\ \text{V} \tag{B.6}$$

Similarly, for the undercurrent protection at -15 A, the threshold voltage V_{A-} should be:

$$V_{A-} = 2.5\ \text{V} - 25\ \frac{\text{mV}}{\text{A}} \cdot 15\ \text{A} = 2.125\ \text{V} \tag{B.7}$$

This can be achieved by choosing R_{41} to 2.4 kΩ, and R_{40} and R_{42} to 6.8 kΩ.

B.3 Phase Voltage Measurements

The phase voltage measurements are not used on the PIF card.

B.4 DC-Link Voltage Measurements

The DC-link voltage measurements will be made using LEM DVM 4000 [37] voltage probes. As the DC-link voltage is applied in a differential with two supplies connected in series with a common midpoint, two voltage probes will be applied, one for DC+ and one for DC-. The maximum rail-to-rail DC-link voltage which will be used during testing is 7.2 kV i.e. ±3.6 kV. To allow for some margin and to be able to measure overvoltage events, the scaling and conversion system will be designed to be able to handle ±5 kV before maxing out on the ADC.

Input Interface

The LEM DVM 4000 provides an output current of 50 mA/4 kV. This needs to be converted into a voltage signal at the input stage on the PIF card by means of an appropriately chosen measuring resistor. The maximum allowable measuring resistor can be calculated from (B.8) [37].

$$R_{M,max} = \min\left(\frac{0.02\ V^{-1} \cdot U_{PN} \cdot (U_C - 1.4\ V)}{U_P \cdot 10^{-3}};\ \frac{0.24 \cdot U_{PN}}{U_P \cdot 10^{-3}}\right)\Omega - 25\ \Omega = 167\ \Omega \tag{B.8}$$

where U_{PN} is the rated primary voltage of 4 kV, U_C is the supply voltage for the voltage sensor, which is 15 V and U_P is the measuring range which will be 5 kV.

Choosing a measuring resistor of 120 Ω will provide an output voltage of 1.5 mV/V which will result in 7.5 V for a 5 kV DC-link voltage.

LP Filter

The LEM DVM 4000 has a frequency bandwidth of 12.8 kHz. The cutoff frequency of the low pass filter should be chosen well above the filter bandwidth. A first order filter with a cutoff frequency of 25 kHz can be made by choosing a resistor of 6.2 kΩ and a capacitor of 1 nF as shown in (B.9).

$$f_{c,V} = \frac{1}{2\pi RC} = \frac{1}{2\pi \cdot 6.2\ \text{k}\Omega \cdot 1\ \text{nF}} \approx 25.7\ \text{kHz} \tag{B.9}$$

Isolation Amplifier

The isolation amplifier ISO224 provides a gain of 1/3 which means that the output voltage after the isolation amplifier will be 0.5 mV/V which results in ±2.5 V for a ±5 kV DC-link voltage.

Differential Amplifier

With the resulting 2.5 V differential output for a full scale measurement of 5 kV as described above for the isolation amplifier, the full range of the input voltage to the ADC is already utilized. Therefore, the differential amplifier will need a gain of 1 only, which can be realized by choosing 1 kΩ resistors for input resistors as well as for feedback resistors.

ADC Bit Resolution

The previous design choices combine to give an input voltage to the ADC of 2.5 V/5 kV which gives a total measurement range of ±5 kV for the ADC. With the available 12 bits from the ADC, one of which is used for the sign bit, this gives a final resolution of:

$$I_{res} = \frac{\pm 5 \text{ kV}}{2^{12} \text{ bit}} = \frac{10 \text{ kV}}{4096 \text{ bit}} \approx 2.44 \frac{\text{V}}{\text{bit}} \tag{B.10}$$

Overvoltage Protection

Similar to what has already been described for overcurrent protection, the PIF card includes an overvoltage protection circuitry made using the same TLV3202 comparators as shown in Fig. B.5.

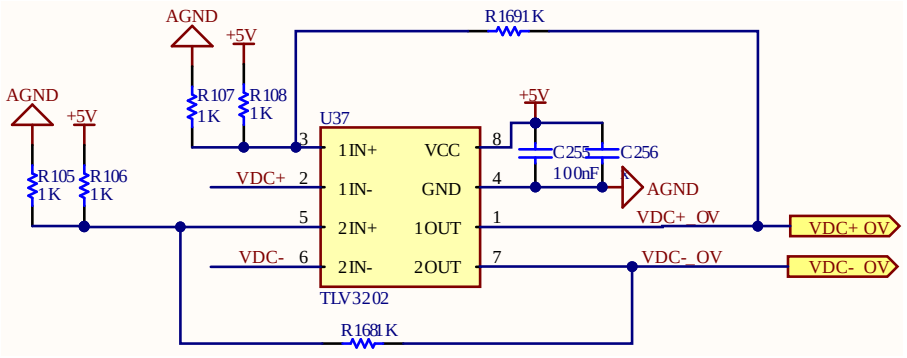

Figure B.5: Comparator circuitry for overvoltage protection.

As with the overcurrent protection, the feedback resistors will be left out initially, such that no hysteresis is achieved. With a rated voltage of 7.2 kV for the total DC-link voltage, the rated voltage for each voltage sensor DC+ or DC- will be 3.6 kV. Therefore, overvoltage protection limits will be chosen to 4 kV. As the overprotection for $VDC+$ uses the positive output of the isolation amplifier as its input signal, the voltage can be described as a function of the primary voltage as follows:

$$V_{IC+}(I_P) = \frac{VDD}{2} + \frac{1}{2} \cdot 0.5 \frac{\text{mV}}{\text{V}} \cdot V_P \tag{B.11}$$

Therefore, to have overvoltage protection at 4 kV, the upper threshold V_{1IN+} should be set to:

$$V_{1IN+} = 2.5 \text{ V} + 0.25 \frac{\text{mV}}{\text{V}} \cdot 4 \text{ kV} = 3.5 \text{ V} \tag{B.12}$$

This can be achieved with the voltage dividers by using 5.6 kΩ resistors for R_{105} and R_{107} and 2.4 kΩ resistors for R_{106} and R_{108}.

Appendix C

Determination of Uncertainty

This appendix supplements the uncertainty determination of the measuring equipment used to estimate the power stack losses. The inductor losses are measured with a power meter whereas the DC power fed by the DC power supplies is measured internally in the DC power supplies. The flow rate and temperature measurements are performed with the integrated measuring unit and sensors.

C.1 Uncertainty of Power Meter

The datasheet specification of accuracies for voltage and current measurements for the power meter (Voltech PM100 [50]) is shown in Table C.1.

Table C.1: Accuracy of power meter (Voltech PM100 [50]).

Reading [%]	**Range** [%]	**Constant** [W]	**Frequency** [% / kHz]
0.2%	0.2%	0.005	0.3%

The uncertainty introduced by the percent of reading, constant error term, and frequency dependent term can be straightforwardly dealt with. However, the power meter is auto ranging on the current and voltage and as a result thereof also auto ranging on the power. The available voltage and current ranges for the power meter are summarized in Table C.2.

Table C.2: Power meter (Voltech PM100 [50]): Voltage and current ranges.

Current Ranges		**Voltage Ranges**	
[A]	**[A RMS]**	**[V]**	**[V RMS]**
0.10	0.07	7.50	5.30
0.30	0.21	15.0	10.6
0.90	0.64	30.0	21.2
2.70	1.91	60.0	42.4
8.10	5.73	120	84.9
24.3	17.2	240	170
72.9	51.5	480	339
200	141	1000	707

The accuracy of the measurements will, therefore, be very dependent on what range the measurements are taken at and is, therefore, most easily dealt with on a pr. measurement basis. The voltage and current ranges are found by rounding up the measured values to the nearest possible range, while the range for the power is found by multiplying the voltage and current ranges. The power meter accuracy, and therefore, the accuracy of inductor losses is calculated with the frequency dependent

term neglected. The absolute and relative accuracies for the inductor losses are calculated as shown in (C.1) and (C.2), respectively.

$$P_{Ind}^{Acc} = P_{Reading}^{Acc,\%} \cdot P_{Ind} + P_{Range}^{Acc,\%} \cdot P_{Range} + 0.005 \text{ W} \tag{C.1}$$

$$P_{Ind}^{Acc,\%} = \frac{P_{Ind}^{Acc}}{P_{Ind}} \tag{C.2}$$

The measurement results are shown in Table C.3. The table further includes the two last columns showing the absolute and relative accuracies, taking into account the auto ranging of the power meter.

Table C.3: Results and accuracies from inductor loss test.

Measured Values			**Ranges**			**Total Accuracy**	
Voltage [V RMS]	**Current [A RMS]**	**Power [W]**	**Voltage [V]**	**Current [A]**	**Power [W]**	**Accuracy [W]**	**Accuracy [%]**
14.05	0.69	0.50	21.2	1.91	40.5	0.09	17
30.20	1.50	1.93	42.4	1.91	81.0	0.17	8.9
42.20	2.12	3.53	42.4	5.73	243	0.50	14
54.75	2.78	5.76	84.9	5.73	486	0.99	17
68.90	3.53	9.03	84.9	5.73	486	1.00	11
80.96	4.19	12.4	84.9	5.73	486	1.00	8.1
93.60	4.90	16.4	170	5.73	972	1.98	12
107.8	5.70	21.7	170	5.73	972	1.99	9.2
121.2	6.48	27.9	170	17.2	2916	5.89	21
129.5	6.98	32.2	170	17.2	2916	5.90	18
139.8	7.62	38.0	170	17.2	2916	5.91	16
152.4	8.44	46.7	170	17.2	2916	5.93	13
163.9	9.24	56.1	170	17.2	2916	5.95	11
174.1	10.0	66.8	339	17.2	5832	11.8	18

As shown in the above table, the accuracies of the individual measurements are found to vary within the interval of 8% to 21%.

C.2 Uncertainty of DC Power Supplies

The datasheet specification of accuracies for the internal voltage and current measurements of the Magna-Power Electronics XR-6000-1 DC power supplies [26] are shown in Table C.4.

Table C.4: Accuracy of internal DC power supply measurement.

Variable	**Range**	**Range**	**Accuracy**
Voltage	6000 V	±0.2%	12 V
Current	1 A	±0.2%	0.002 A

As the power will be the sum of the product of voltage and current for each DC power supply, it is necessary to describe the relative uncertainty of the voltage and current measurements as a function of the actual measured current compared to the measuring range. This can be easily done by relating the measured voltage and current to the absolute uncertainties of the DC power supply as:

$$U_{DC}^{Acc,\%}(U) = \frac{12 \text{ V}}{U} \tag{C.3}$$

$$I_{DC}^{Acc,\%}(I) = \frac{0.002\ \text{A}}{I} \tag{C.4}$$

Then, the uncertainty for the power supplied by a single DC power supply can be calculated by summing the relative uncertainties according to the rule for correlated multiplication as stated in Table 6.1. Thus:

$$P_{DC}^{Acc,\%}(U,I) = U_{DC}^{Acc,\%}(U) + I_{DC}^{Acc,\%}(I) = \left(\frac{12\ \text{V}}{U} + \frac{0.002\ \text{A}}{I}\right) \tag{C.5}$$

The absolute uncertainty of summing the power from the two DC power supplies can be calculated as the sum of the absolute uncertainty of each DC power supply, which can be found as:

$$P_{DC+}^{Acc}\left(U^+,I^+\right) = \left(\frac{12\ \text{V}}{U^+} + \frac{0.002\ \text{A}}{I^+}\right)\cdot\left(U^+\cdot I^+\right) \tag{C.6}$$

$$P_{DC-}^{Acc}\left(U^-,I^-\right) = \left(\frac{12\ \text{V}}{U^-} + \frac{0.002\ \text{A}}{I^-}\right)\cdot\left(U^-\cdot I^-\right) \tag{C.7}$$

$$P_{DC}^{Acc}\left(U^+,I^+,U^-,I^-\right) = P_{DC+}^{Acc}\left(U^+,I^+\right) + P_{DC-}^{Acc}\left(U^-,I^-\right) \tag{C.8}$$

and the relative uncertainty of the total DC power measurement can be found as:

$$P_{DC}^{Acc,\%}\left(U^+,I^+,U^-,I^-\right) = \frac{P_{DC}^{Acc}\left(U^+,I^+,U^-,I^-\right)}{\left(U^+\cdot I^+\right)+\left(U^-\cdot I^-\right)} \tag{C.9}$$

$$= \frac{\left(\frac{12\ \text{V}}{U^+} + \frac{0.002\ \text{A}}{I^+}\right)\cdot\left(U^+\cdot I^+\right) + \left(\frac{12\ \text{V}}{U^-} + \frac{0.002\ \text{A}}{I^-}\right)\cdot\left(U^-\cdot I^-\right)}{\left(U^+\cdot I^+\right)+\left(U^-\cdot I^-\right)} \tag{C.10}$$

If the measured values of voltage and current are assumed to be the same for the positive and negative DC power supply that is $U^+ = U^- = U$ and $I^+ = I^- = I$, the expression reduces to:

$$P_{DC}^{Acc,\%}(U,I) = \frac{2\cdot\left(\frac{12\ \text{V}}{U} + \frac{0.002\ \text{A}}{I}\right)\cdot(U\cdot I)}{2\cdot(U\cdot I)} = \left(\frac{12\ \text{V}}{U} + \frac{0.002\ \text{A}}{I}\right) \tag{C.11}$$

The relative uncertainty of the total DC power measurement using the internal voltage and current measurements can be found using (C.11).

C.3 Uncertainty of Water Cooling System

The total accuracy of the flow rate and temperature measurements made with the Kamstrup MULTICAL 603 measuring unit [36] and sensors depend on the individual accuracies. According to the datasheet, the accuracies are as shown in (C.12).

$$E_c = \pm\left(0.15 + \frac{2}{\Delta T}\right)\% \qquad E_f = \pm\left(1 + \frac{0.01 q_i}{Q}\right)\% \qquad E_t = \pm\left(0.4 + \frac{4}{\Delta T}\right)\% \tag{C.12}$$

where q_i is the maximum flow rate of 1500 L/h.

The total relative uncertainty of the water cooling measurement is the sum of the accuracies presented above. From the above equations, it can be seen that the relative uncertainty depends on the actual flow rate Q and delta temperature ΔT. The total relative uncertainty is given by:

$$P_{Cool}^{Acc,\%}(Q,\Delta T) = \left(0.15 + \frac{2}{\Delta T}\right) + \left(1 + \frac{0.01 q_i}{Q}\right) + \left(0.4 + \frac{4}{\Delta T}\right) \tag{C.13}$$