# *A Power Semiconductor-based Planar Capacitor for the Embedded Solar Microinverter*

*Master's thesis*

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Written By:
Dan-Andrei Gumeni

M4
Group PED4 - 1050
Department of Energy Technology
Aalborg University

AALBORG UNIVERSITY
STUDENT REPORT

**School of Engineering and Science (SES)**
Energy Engineering
Pontoppidanstræde 111
9220 Aalborg Ø, Denmark
http://www.ses.aau.dk/

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**Participants:**

Dan-Andrei Gumeni

**Supervisors:**
Huai Wang
Haoran Wang

**Abstract:**

Current technological trends have lead to a significant reduction in the width of PV panels. Although this offers compelling benefits regarding the transportation and ease of installation of these new generation panels, it does come with concerns regarding the continuous use of PV embedded micro-inverters, as these converters are currently limited by their passive capacitor DC-link when it comes to any height reductions in line with those of the panels. The objective of this project is to develop an active capacitor design as a viable substitute for the conventional passive DC-link solution, while respecting the new height limits imposed by the thinner panels. This has covered the design process, the software validation and the hardware implementation and testing, while also including comparisons with the initial passive capacitor. Finally, the main objective of the project was accomplished, as the active capacitor system manages to directly oppose the presence of the ripple component in the input signal, resembling the voltage stabilising capabilities of the passive capacitor.

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*By signing this document, each member of the group confirms participation on equal terms in the process of writing the project. Thus, each member of the group is responsible for the all contents in the project.*

# Summary

This report concerns the design, simulation and implementation of an active capacitor for use in the DC-link of a solar PV embedded micro-inverter. The objective is to implement a prototype that is limited to a height of 20 mm and to prove that it can be used to mimic the voltage ripple attenuation capabilities of a much larger passive capacitor. The prototype does so by use of a control scheme and an auxiliary circuit, which work to counteract the ripple resulted across a smaller passive capacitor. In doing so, the active capacitor is no longer subjected to the same limitations as the conventional passive capacitor, regarding the balance between its height and its capacitance.

In Chapter 1 the context is presented in which the height of the embedded solar micro-inverter, more specifically that of its DC-link, is becoming a problem. The active capacitor is advanced as a possible solution to this issue that warrants further research. Therefore, the research question is defined, together with the main project objectives and limitations.

In Chapter 2 the overall structure of the standard micro-inverter is presented and the limitations of the currently implemented passive capacitor DC-link are further explained, as well as the importance of maintaining the panel embedded structure of the PV micro-inverter. Building on this, the main operation and structure of the active capacitor are presented, which are then used to justify how this concept can be applied to solve the problem the next generation of thinner PV panels will bring regarding the currently available micro-inverters.

Chapter 3 theoretically described the design process of the active capacitor control scheme and components selection. The latter concerns both the passive and the active elements. Each stage is presented in general terms, since the design process is based on the ratings of the application for which the active capacitor is constructed. In this way, once these ratings are known, they can simply be substituted in the equations presented in this part of the report, which is the case in Chapter 4 for a 350 W rating micro-inverter. This is an iterative process, in which multiple design iterations were deemed unsatisfactory at various points. Therefore, only the final solutions, which satisfied all the presented requirements, the most important being the 20 mm height limit, are presented in the report.

The resulting design is simulated in various testing scenarios in Chapter 5, including direct comparisons with the initial passive capacitor used as the DC-link of the 350 W micro-inverter on which the design was based. As the results were satisfactory, this served to confirm the design for further hardware implementation, in the form of a PCB, and for further laboratory testing, both of which are described in the rest of the chapter. Nevertheless, the active capacitor prototype is successfully controlled to generate an output voltage that opposed the ripple voltage component of the feedback signal, this being the mechanism by which the active capacitor emulates the ripple mitigation capabilities of the larger passive solution.

Finally, this leads to the conclusion presented in Chapter 6, which is that the research question initially advanced in Chapter 1 is successfully answered by the capability of the active capacitor to output this voltage opposing the ripple, while also maintaining a maximum height of 20 mm. Other relevant continuations of the work accomplished in this report are presented in Chapter 7.

# Preface

This report was written by Dan-Andrei Gumeni, group number *PED4 - 1050*, at the Department of Energy Technology at Aalborg University. This project is a 4th-semester master's thesis. The purpose is to ascertain the feasibility of an active capacitor design, limited to a height of 20 mm, as an alternative to the conventional passive capacitor, when used in the DC-link of a solar micro-inverter.

The software that has been used over the course of the project is:

- **Overleaf** - Write the report.
- **Mendeley** - Sort bibliography and provide citations.
- **MATLAB** - Design calculations.
- **Inkscape** - Edit figures.
- **PLECS** - Simulate the electrical circuits.
- **Altium Designer** - Design the schematic and the PCB layout.
- **C2000 Embedded Coder & Code Composer Studio** - Program the Texas Instruments DSP.

**Reader's Guide:**

At page v, a table of contents is provided. The hyperlink found there can be used for fast navigation to specific sections of the report.
On page vi a nomenclature can be found, that lists the abbreviations and the variables used throughout this report.

The bibliography found at page 63 presents the relevant literature for this report. The citations are provided in the following format:

[Author][Title](Institution)(ISBN)[Year](URL)(Date Accessed)

The fields in square brackets are obligatory, while the ones in regular brackets are relevant for only certain publications, i.e web pages or books. These citations are sorted by order of their appearance in the report.

# Table of Contents

# Nomenclature

## Acronyms

| | |
|---|---|
| AC | Alternating Current |
| ADC | Analog-to-Digital Converter |
| DC | Direct Current |
| DSP | Digital Signal Processor |
| EU | European Union |
| GM | Gain Margin |
| LF | Loop Filter |
| LV | Low Voltage |
| MPP | Maximum Power Point |
| PD | Phase Detector |
| PI | Proportional-Integral |
| PLL | Phase Locked Loop |
| PM | Phase Margin |
| PWM | Pulse Width Modulation |
| RES | Renewable Energy Sources |
| RMS | Root Mean Square |
| THD | Total Harmonic Distortion |
| VRE | Variable Renewable Energy |
| VSI | Voltage Source Inverter |

## Variables

| **Symbol** | **Description** | **Unit** |
|---|---|---|
| $C$ | Capacitance | [F] |
| $C_{dc}$ | DC-link Capacitance | [F] |
| $d$ | Diameter | [m] |
| $d$ | Duty Cycle | [-] |
| $e$ | Error | [-] |
| $f$ | Frequency | [Hz] |
| $G_{HPF}$ | High-pass filter Transfer Function | [-] |
| $G_{LPF}$ | Low-pass filter Transfer Function | [-] |
| $G_{PI}$ | Controller Transfer Function | [-] |
| $H$ | Height | [m] |
| $I$ | Current | [A] |
| $I_{dc}$ | DC Current | [A] |
| $i_g$ | Grid-side Current | [A] |
| $i_i$ | Inverter-side Current | [A] |
| $I_{pk}$ | Peak Current | [A] |
| $K_i$ | Integral Gain | [-] |
| $K_p$ | Proportional Gain | [-] |
| $L$ | Inductance | [H] |
| $l$ | Length | [m] |
| $L_f$ | Filter Inductance | [H] |
| $m$ | Modulation Index | [-] |
| $Q$ | Electric Charge | [C] |
| $R$ | Ohmic Resistance | [Ω] |

| | | |
|---|---|---|
| $R_{th}$ | Thermal Resistance | [°C/$W$] |
| $T$ | Temperature | [°C] |
| $t$ | Time | [s] |
| $T_s$ | Sampling Time | [s] |
| $V$ | Voltage | [V] |
| $V_{dc}$ | DC-link Voltage | [V] |
| $V_g$ | Grid Voltage | [V] |
| $v_i$ | Inverter-side Voltage | [V] |
| $v_o$ | Output Voltage | [V] |

## Indices

| | |
|---|---|
| meas | Measured |
| norm | Normalised |
| oc | Open Ciruit |
| out | Output |
| ref | Reference |
| rms | Root Mean Square |
| sc | Short Ciruit |
| sw | Switching |
| th | Thermal |

Chapter 1

# Introduction

## 1.1 Background

The ways in which electrical energy is generated have significantly changed in the past few decades in the context of the ongoing climate crisis. Different approaches have been tried in order to limit the amount of greenhouse gases being released into the Earth's atmosphere. These ranged from improving the efficiency of the conventional fossil-fuel based energy generation methods to substituting them altogether with environmentally friendly renewable sources.

The latter approach is increasingly embraced throughout the world, thanks to significant technological advances, which also led to decreased costs [1]. For instance, by April 2017, 5% of the total annual energy produced in the United States and 13% in Europe came from renewable sources [2]. Even more so, some European countries like Denmark, Ireland and Germany have produced even more than 20% of their electrical energy from such alternative sources [2]. In 2020, for the first time in history, Germany produced more energy from renewable sources than from fossil fuels [3].

Out of the all the available renewable energy sources, one of the most promising and broadly implemented ones are photovoltaics (PV). By using the photovoltaic effect, PV panels can directly convert the solar radiation to electricity, in a clean and efficient manner [4]. Thanks to this, solar energy has become one of the fastest growing energy sectors in the world. For example, in 2020 solar energy generation was the fastest growing energy sector in the United States, increasing by 20.7% in the first four months when compared to the same period in the previous year, with wind energy in second place at only 12% [5].

Similar positive trends can be seen throughout the world (Figure 1.1), with only China installing over 30 GWp of power in 2019 alone, more than the amount installed in 2010 in the entire world. It is also especially important to point out the significant share associated with the rest of world category, which would include emerging economies such as Africa or South America, continents with very high potential when it comes to solar energy, due to their geographical location. The amount of PV power installed in these regions is expected to further grow along with their economical development [6].

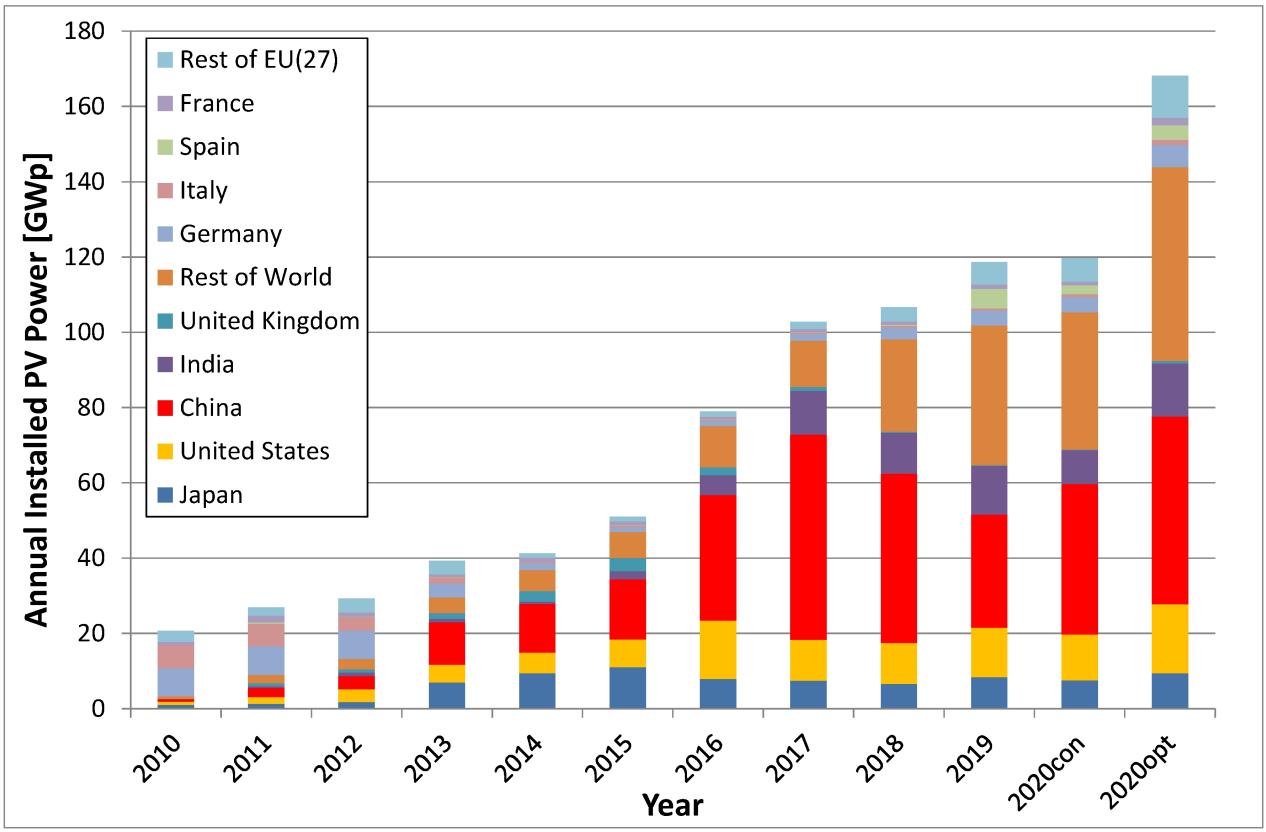


**Figure 1.1:** Amount of PV power installed each year around the world, measured in GW, under peak conditions of solar radiation and temperature [6]

The growth of the PV sector can be even more clearly seen when considering the total installed peak PV power (Figure 1.2). In the span of a decade the entire installed PV power of the world increased 16 times, going from 40 GWp in 2010 to 640 GWp in 2019. Since this growth only accelerated in the second half of the decade, with countries such as China, India and the United States visibility increasing their share of PV power, the solar energy sector is expected to continue growing rapidly in the coming decade. Even the most conservative estimate for 2020 signaled an increase of 120 GWp.

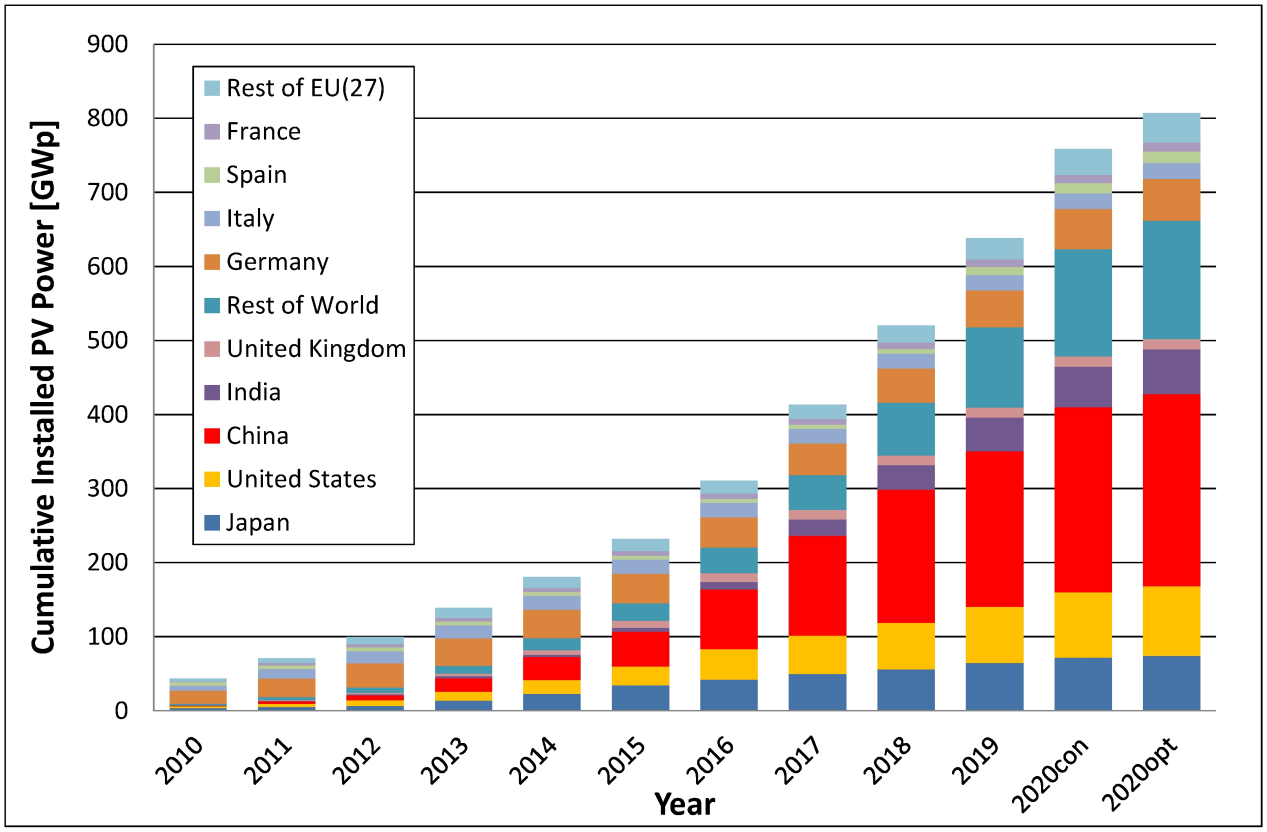


**Figure 1.2:** Total amount of PV power installed around the world, measured in GW, under peak conditions of solar radiation and temperature [6]

As previously stated, the growth of the PV sector was also accelerated by the technological advances made. Initially, most of the cost of the PV system was comprised of the cost of the PV panel itself, as the inverter, installation and maintenance were significantly cheaper [7]. However, in the recent years, the progress made in panels manufacturing has lead to a sharp decrease in their prices, resulting in the DC/AC converter becoming a larger part to the overall cost of the PV system. In this context, efforts have been made to increase the cost efficiency of the inverter in PV applications, one such option being the use of panel-embedded micro-inverters [7].

These are a type of lower power rating inverters which are mounted underneath or inside each PV panel and convert the output power to the appropriate voltage and frequency depending on the application. This is different from conventional PV inverters, where one main converter is used for converting the power output of the entire array of PV panels. The problem in that case is that individual control of panels, through maximum power point tracking (MPPT), is not possible, as the PV arrays are seen as a single total voltage source by the inverter. Yet, factors such as the levels of solar radiance, shading and temperature differ from panel to panel, resulting in different optimum operating points for each module. Therefore, in the case of a central inverter, there is a risk that some individual PV panels are not efficiently used [7] [8].

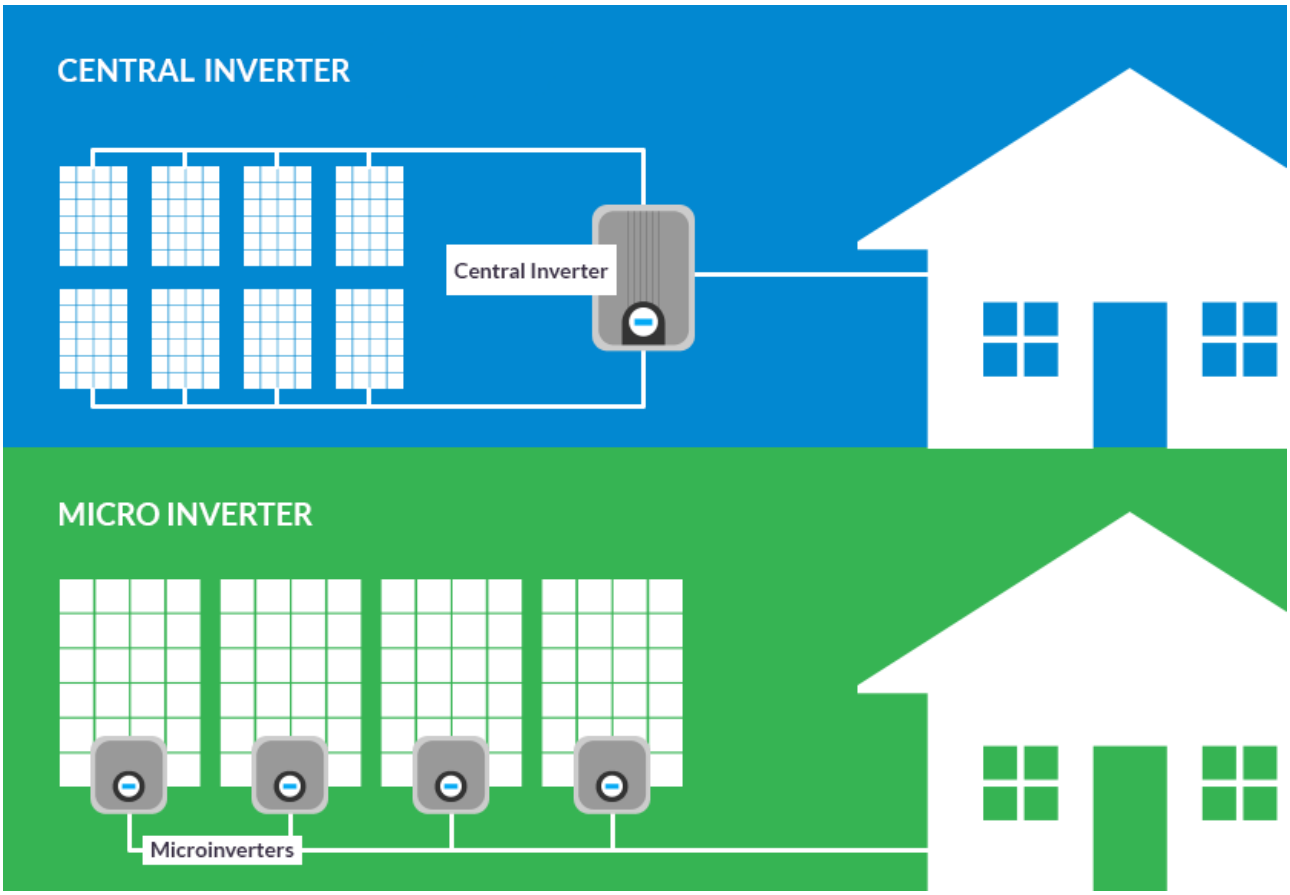


**Figure 1.3:** Diagram representations of central and micro inverter-based residential PV systems [9]

This disadvantage is negated when using embedded micro-inverters, which can optimize each individual PV module. Other advantages come from their convenience, ease and cost of installation, as additional PV modules equipped with embedded micro-inverters can later simply be added next to the existing modules, allowing for the possibility of easily scaling the power output capabilities of the entire PV system. That would not be the case in conventional solar energy systems, where the addition of extra PV panels would be conditioned by the maximum power rating of the central inverter [7] [8].

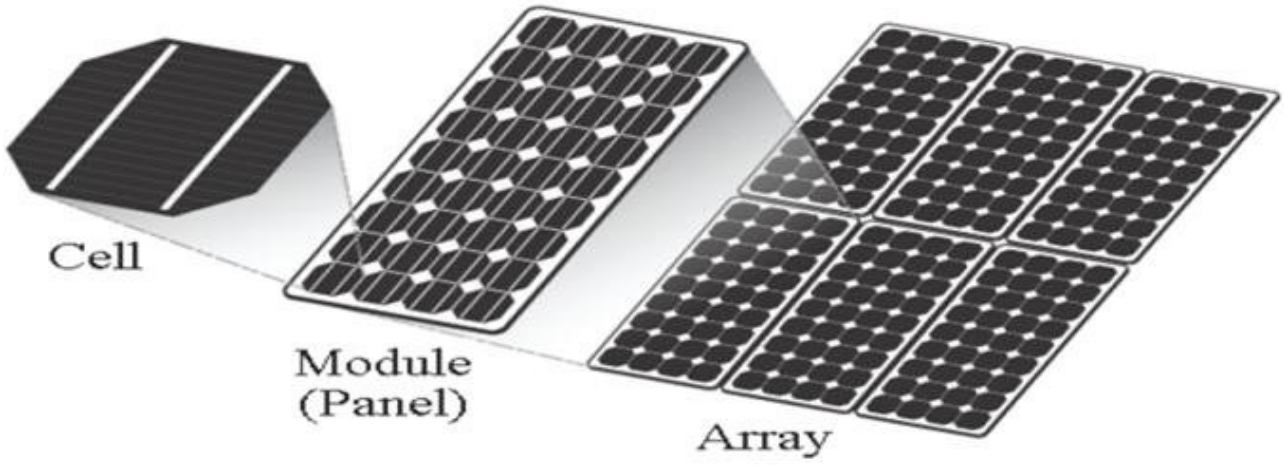


**Figure 1.4:** Representation of the difference between a PV cell, a PV module and a PV array [10]

One last major advantage is the increase in reliability, as the failure of one micro-inverter would only shutdown the power generation capabilities of one PV module, while the failure of a central inverter would hamper the necessary energy conversion of the entire PV system. Yet, embedded micro-inverters still have a higher cost-per-watt than conventional central inverters, which makes them less cost efficient in large PV farms, but better suited for small commercial or residential applications [7] [8].

Nevertheless, this still represents a significant percentage of the solar PV sector. According to [11], 44% and 41% of the total solar PV power installed globally in 2018 and in 2019, respectively, was installed in the residential and commercial sectors, with the rest being in the utility sector. Similar percentages are projected until at least 2025. In this scenario the use of embedded micro-inverters becomes even more desirable, as it represents the superior choice for residential and commercial PV applications and would lead to the most efficient use of such solar panels. Accordingly, research and development of new embedded micro-inverter designs is a topic worth exploring, if they are to match the technological and economical developments of the PV panels themselves.

A current design limitation for PV micro-inverters comes in the form of the DC-link. Used for voltage ripple attenuation and power balancing, the capacitive DC-link is a major part of most voltage source converters (VSC) [12]. However, the conventional passive capacitor solutions tend to generally have an increased physical size in order to properly minimize the voltage ripple variations [13]. Therefore, this is leading to more and more restrictive design limitations for embedded micro-inverters which, as stated above, are usually fixed inside or underneath the PV panels, and therefore have to conform to certain height limitations. Because the width of these panels has been constantly reducing in the past years, the problem is being raised regarding the height of the conventional micro-inverter, particularly the height of its DC-link capacitor, as the next generation of PV panels will continue the trend of reducing their width until current passive capacitors will become unusable [14] [15].

The following paper proposes a solution to this height problem by utilizing a planar two-terminal active capacitor DC-link topology in place of the conventional passive capacitor [13]. This concept employs an active auxiliary power electronics circuit connected in series with a smaller passive capacitor. The circuit is controlled so that it directly counteracts the ripple variations, exceeding the usual limitations of the conventional capacitors, which normally have to balance their ripple attenuation capabilities with an increased size. Thus, the use of this additional circuit allows for a reduction in the capacitance and, therefore, the height of the primary capacitor [16]. This would directly solve the issue of the micro-inverters not fitting inside the new generation of PV panels. Further benefits could stem from an increase in the expected lifetime of the capacitor and ease of installation due to its modular design [13][17].

## 1.2 Research Question

Considering the theoretical analysis, the following research question is advanced:

*"Is the two terminal planar active capacitor a suitable solution for the DC-link of a 350 W embedded solar PV micro-inverter, provided that its maximum height is limited to 20 mm?"*

## 1.3 Project Objectives

- Establish the importance of researching alternative solutions for the DC-link of an embedded solar micro-inverter under the current technological trends
- Present the system characterization of the two-terminal active capacitor, based on the existing literature on the subject
- Design a new active capacitor adapted for use in a 350 W solar micro-inverter, while explaining the design process, and provide the resulting bill of materials
- Simulate the design in stand-alone operation and when inserted in a solar micro-inverter as the DC-link
- Once verified in simulations, design and build PCB containing the active capacitor prototype, as well as any possible necessary secondary additions, and program controller based on previously simulated control scheme
- Test the resulting experimental setup in a laboratory environment

## 1.4 Project Limitations

- The requirements regarding the harmonic content of the output current when connecting photovoltaic inverters to the power grid are not considered. Therefore, the ways in which the active capacitor would impact this harmonic content are also not investigated.
- Expected lifetime of components of active capacitor are considered only in relation to the rated lifetime of the initial passive capacitor. Thus, no thermal simulations are implemented in order to determine the actual operating temperature and expected lifetime, instead relying on the datasheet values.
- An external controller is used for the laboratory experiments, instead of an internal one inside of the active capacitor.
- The experimental validation presented in the report verifies the performance of the auxiliary circuit and of the control scheme, therefore functioning as an open loop test of the active capacitor.
- The ongoing COVID-19 pandemic has stopped or severely restricted the laboratory access at various stages throughout the semester, as well as caused delays in the shipping of necessary components, which has limited the amount of time available for experimental work.

Chapter 2

# State of the art

## 2.1 The grid-connected PV micro-inverter

The last decades have seen substantial technological advances in small scale inverters, leading to their implementation as solar PV micro-inverters, a viable alternative to the more established central (or string) inverter. Some crucial developments came in the form of an increased expected lifetime, a higher DC/AC conversion efficiency and an advantageous modular design which allows for easy installation and later expansion by simply adding additional units to the existing ones [18]. As described in Chapter 1, the global solar power market has expanded extensively and is expected to continue doing so. In this context, newer technologies such as the embedded micro-inverter present a valuable opportunity for further developing an already rapidly growing sector.

As mentioned above, a regular micro-inverter can be compared with as a small inverter, converting the output power from a single PV panel to the necessary voltage level and providing grid synchronisation. Therefore, when supplying power, the micro-inverter has to adhere to all the usual regulations of its application, related to frequency, voltage level, total harmonic distortion (THD) and power factor [7]. Because of this, it needs to utilise all the conventional necessary controls, such as the current controller, phase-locked-loop (PLL) and maximum power point tracking (MPPT).

A PLL is a closed-loop system that outputs a signal whose phase is matched to that of an input signal. It employs a phase detector which determines the difference between the input and the feedback signals. This phase difference is then fed into a loop filter and a voltage controlled oscillator. Ultimately, the PLL is used to synchronize the two signals, as well as to track any changes in the input frequency [19].

Most grid-tied converters employ a regulator for two primary reasons: controlling the output AC current and the DC-link voltage. The first one is regulated with the purpose of supplying the main grid or a micro-grid with power, while the latter is done in order to stabilize and maintain the voltage at a certain value [19].

The MPPT is an algorithm used in PV applications to determine the voltage value at which the solar panel or array can produce the maximum amount of power. This maximum point varies with the ambient temperature, the PV cell temperature and the available solar radiance. For any such conditions, PV cells have a certain operating point at which the values of their voltage V and current I result in the maximum output power P. The relationship between voltage and current is exemplified in a non-linear I-V curve for any PV cell, module or array, based on which a similar P-V curve is obtained. An exemplification is shown in Figure 2.1. Once this P-V characteristic is known, the voltage corresponding to the maximum power output can be easily determined and used as a reference for the rest of the control scheme [20].

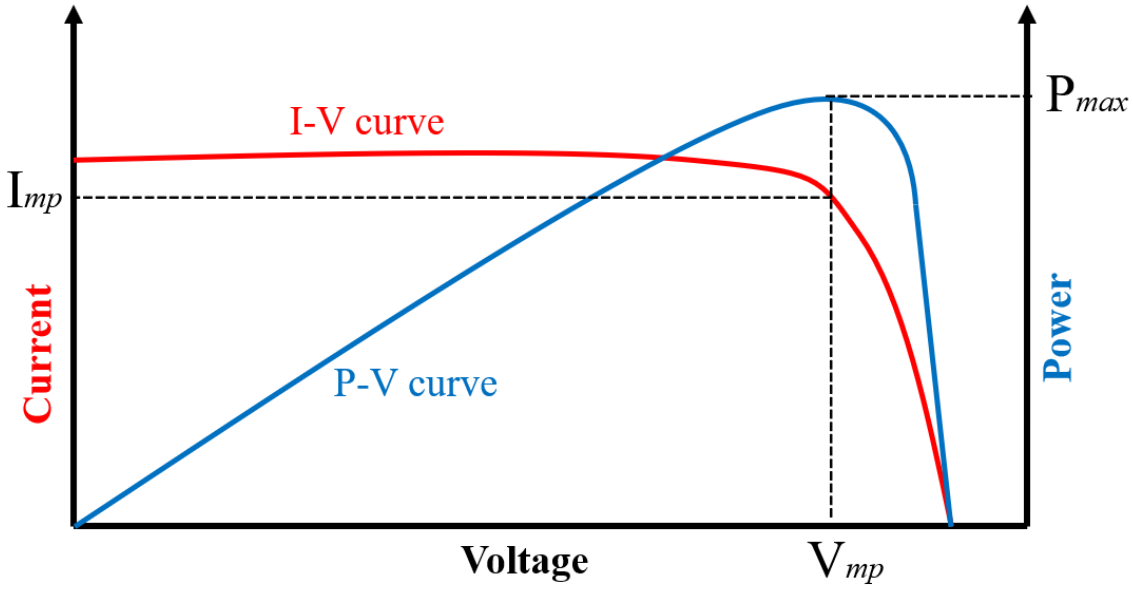


**Figure 2.1:** I-V and P-V curves, at a certain temperature level, used in maximum power point tracking

The dependency of these curves on external factors such as the solar radiance leads to one of the most important distinctions between the micro-inverter and the conventional central inverter. The former allows for individual use of MPPT for each PV module, thanks to each associated micro-inverter, thereby guaranteeing that all panels will output the maximum available power.

On the other hand, in the case of the latter, MPPT can only be applied to the entire PV array, not to individual modules. This does not represent a problem in ideal scenarios of solar radiance for each panel, but it creates a major issue when any form of shading is present. Because of the use of a central MPPT, the maximum point calculated will not represent the optimum voltage value of individual panels and the power output of the unshaded panels will be limited by the presence of shaded ones. In this case, the efficiency of the entire PV array is reduced as a consequence, while in the case of micro-inverters each individual panel is producing the maximum power in the current conditions [7].

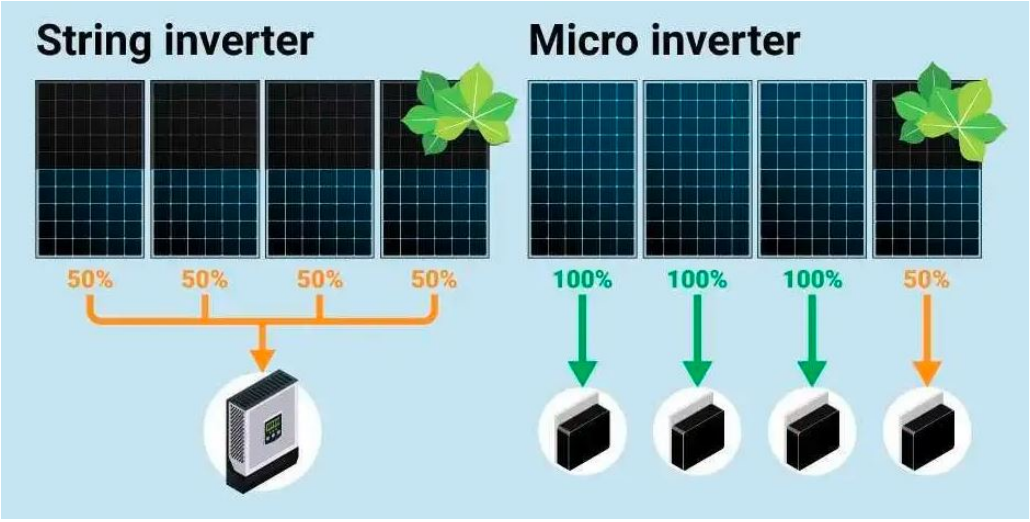


**Figure 2.2:** Effect of MPPT-based control of PV panel arrays in which one panel is partially shaded in string inverters and in micro inverters [21]

This property of the individual use of MPPT in micro-inverters has varying benefits depending on the solar PV application. It is less useful in the case of large scale PV farms, as they are usually designed to maximize the generated power. With virtually no tall structures neighbouring the panels, the only possible shading produced would come from the clouds. Moreover, such panels are constantly monitored and maintained free of dust or any other particles gathered on their surface that could reduce the levels of radiance they receive [20].

Therefore, panel-specific MPPT is better suited for smaller scale PV inverter applications. In urban and residential applications, the careful design concerning possible shading that was present in PV farms can no longer be relied upon. Nearby trees or buildings and the shape of the roof the PV was installed on can all lead to additional shading [20]. On top of that, constant maintenance can no longer be guaranteed, as it was in solar power plants. Accordingly, the extra efficiency of the per-panel micro-inverter is required [7].

As stated above, the necessary voltage value of the PV system is calculated using the MPPT algorithm and is used as a reference value for the different types of control schemes implemented in order to regulate the output of the PV system. One of the most common solutions for that purpose is the use of a DC-DC boost converter, connected to the primary DC-AC converter, forming a two-stage PV inverter. This DC-DC converter is modulated according to the MPPT, obtaining the desired voltage value across the capacitor $C_{boost}$, supplying the DC-link of the inverter with power from the PV module [22].

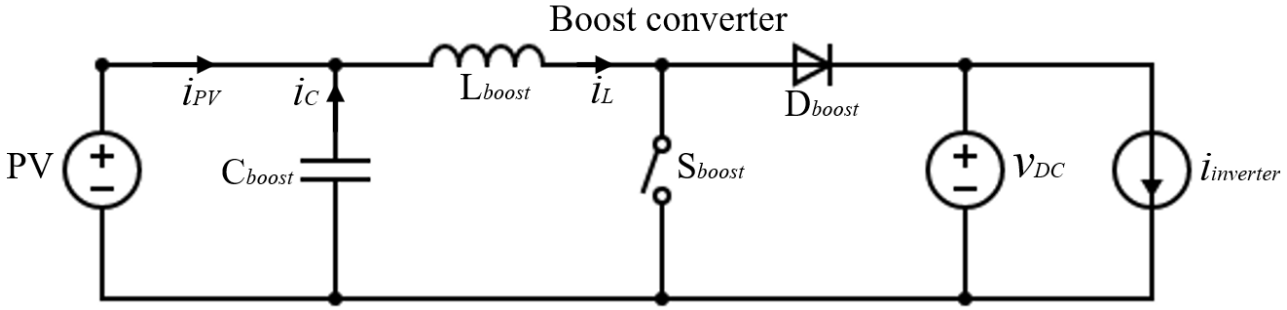


**Figure 2.3:** Diagram of DC-DC boost converter used in two-stage PV inverters

The DC-link capacitor is an important element conventionally used in voltage sourced power inverters which are interfacing with non-ideal DC voltage sources, ranging from PV panels, fuel cells, batteries to other converters like rectifiers or DC-DC converters. A varying supply voltage will result in ripples in the output current of the power converter, raising energy quality concerns [23]. Therefore, the capacitor is used to mitigate the fluctuations of the associated supply, for example solar radiation variations in the case of PV panels. By getting charged from the DC-source and operating as a short-term energy storage device, the capacitor mitigates these supply deviations and function as a continuous linear DC-source for the input side of the inverter.

In order to maintain the DC-link voltage ripple within a chosen limit of $V_{pp}$, a minimum capacitance has to satisfy the following formula [17]:

$$C_{DC} = \frac{\sqrt{2}I_{AB}}{2\omega_{grid}\frac{V_{pp}}{2}} = \frac{V_m I_m}{\omega_{grid} V_{DC-link} V_{pp}} \tag{2.1}$$

in which $I_{AB}$ is the root-mean-square (rms) value of the current flowing through the DC-link, $\omega_{grid}$ is the grid-side frequency, $I_m$ and $V_m$ are the magnitudes of the AC current and voltage and $V_{DC-link}$ is the average value of the DC-link voltage. Based on this constraint a balance has to be reached between the allowable voltage ripple and the capacitance value.

According to [23] and [17], the most commonly used type of DC-link capacitor is the electrolytic one, with the film and ceramic capacitors also being possible solutions. The electrolytic capacitor generally offers a higher capacitance for the same price and size, while having the disadvantages of its polarized structure and of its relatively increased equivalent series resistance (ESR). On the other hand, both film and ceramic capacitors are non-polarized, have lower ESR (therefore, better ripple current handling capabilities), are more robust when it comes to over-voltages and temperatures and have increased lifetimes. Between the two of these, the ceramic capacitor is very limited when it comes to its capacitance values, usually having relatively low ones, making it a niche choice for DC-link applications. Overall, electrolytic capacitors are preferred because of their size and cost efficiency, but film capacitors may be required if the expected temperature and ripple current are concerning [24].

The two-stage design of the PV converter means that two back-to-back converters are linked together, with the DC-AC converter generating the output current. In order to shape this output to be closer to a sinusoidal signal an LCL harmonics filter, formed out of the inductances $L_1$ and $L_2$, the capacitor $C_f$ and the damping resistor $R_d$, is connected between the DC-AC converter and the load of the inverter [25].

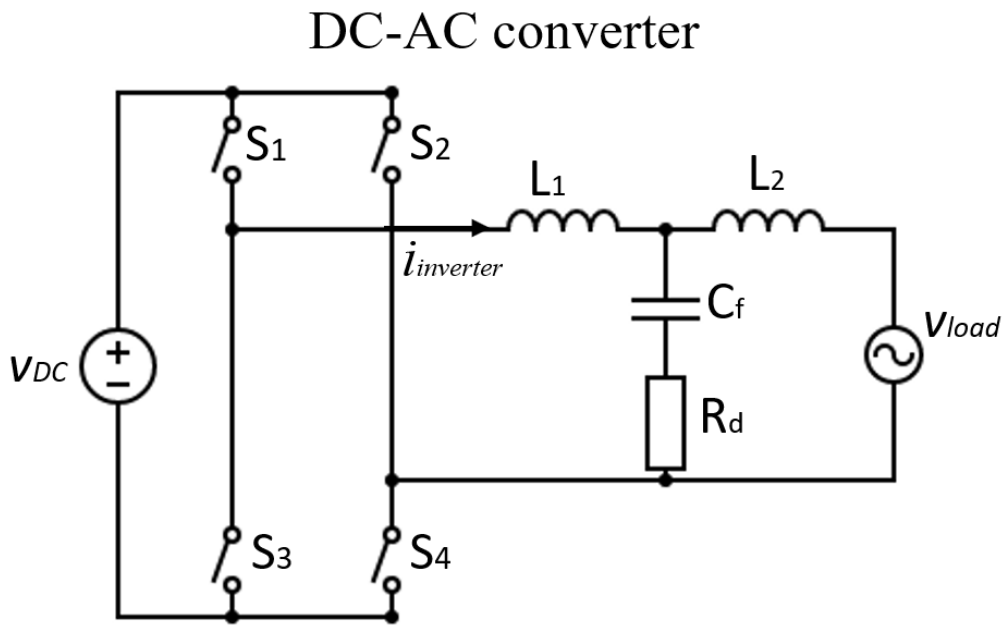


**Figure 2.4:** Diagram of DC-AC converter used in two-stage PV inverters, including the LCL harmonics filter

As stated at the beginning of the section, a PV module-embedded micro-inverter can be generally treated as a small scale inverter, possessing the same hardware structure (in this case, the back-to-back DC-DC and DC-AC converters). Figure 2.5 represents an exemplification of the structure of a grid-connected two-stage PV micro-inverter.

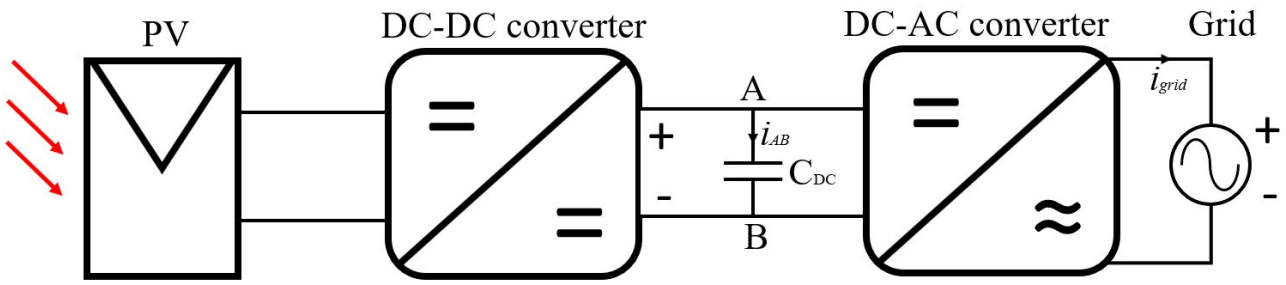


**Figure 2.5:** Diagram of a two-stage solar PV grid-connected inverter

## 2.2 Panel embedded design

The embedded characteristic of the solar PV micro-inverter is one of its most representative features. By mounting the inverter on the back or inside of each individual PV module, the micro-inverter is protected from direct solar radiation and is therefore safe from the associated temperature increase [7]. This is coupled with the reduced voltage level it has to withstand by being connected to only a single PV module, which leads to decreased thermal stress due to the lower power output. The result is that no additional cooling system is required and an increased expected lifetime is achieved when compared to the traditional central inverter [26].

More so, as the inverter is integrated with the panel it can be treated as a complete package. It can be pre-assembled by the manufacturer, allowing for easier and cheaper transportation, especially in larger quantities. Accordingly, it also reduces the time, manpower and expertise required during the actual installation, as well as allowing for easy further expansion at a later time. Another added benefit of the modular design is that DC/AC conversion takes place entirely inside the panel-inverter layout, therefore minimal DC equipment, such as wiring and cabling, is necessary on top of the already existing AC-specific equipment [27].

Because of its convenient installation possibilities and the resulting per-unit MPPT control, the use of integrated micro-inverters is specifically suited for solar energy applications in residential or urban areas, where they are usually mounted on rooftops, and factors such as the available space, the shade caused by nearby buildings or the geometry of the roof become a problem [7].

However, this type of structure also results in an important limitation of the micro-inverter design, as its size becomes strictly restricted by the necessity of fitting within the dimensions of the associated solar panel. According to [28], the depth of most residential PV panels varies from 33 mm to 45 mm, primarily depending on the thickness of the frame and of the area of the panel itself. So far, embedded micro-inverter designs have been able to accommodate this restriction. However, as manufacturers continue to search for methods to further reduce the costs of producing solar panels, the depths of the PV panels are being lowered bellow the current standards.

Innovations have been focused on reducing both the thickness of the silicon cells as well as of the metal frame. Due to advances in the manufacturing process, thinner silicon layers, which were considered too fragile and brittle in the past and where leading to significant losses on the production line due to breakage, can now be safely utilised in solar cells [29]. Additionally, because the aluminium frame was one of the most expensive elements after the silicon layers, panel designs were also adjusted in order to minimize the frame's thickness [15]. The reduction in used material also resulted in a lowered weight, which, coupled with the decreased thickness, would allow for easier and cheaper transportation. Based

on these innovations, an industry trend towards reducing the depth of the PV panels has emerged.

In this context, in order to maintain its embedded design, the solar micro-inverter has to be down-sized to comply with the reduced depth of the PV panels. Currently, the DC-link passive capacitor is the highest element, limiting the development of thinner inverters. The 280 W two-stage solar micro-inverter described in [30], with the bill of materials given in [31], is used as an example proof of this statement, as its power rating is close to that of most conventional solar micro-inverters (between 250 W and 350 W [22]). Out of the main hardware components, the power switches have a height of 20.8 mm; the diodes, used for both the DC-DC and DC-AC converters, of 10.3 mm; the DC-DC converter filter film capacitor of 31.1 mm; the DC-DC converter filter inductor of 32.51 mm and, finally, the DC-link electrolytic capacitor of 40 mm. As expected, the DC-link capacitor was the tallest element, acting as the main barrier for any possible height reduction of the inverter.

As was described by Equation 2.1, in order to maintain the DC-link voltage ripple within a certain limit a minimum capacitance value has to be ensured. However, a balance also has to be provided between this resulting capacitance and the physical area of the capacitor, as is demonstrated by Equation 2.2. This describes the dependency of the capacitance $C_{DC}$ on the area $A$ of the metallic plate, with $\varepsilon$ and $d$ being the permittivity of the dielectric and the distance between the two plates, respectively.

$$C_{DC} = \frac{\varepsilon A}{d} \tag{2.2}$$

These two relationships are what leads to increased sizes and, consequently, heights, for passive capacitors if certain capacitance values are to be met. As its technology has reached a mature state, being a staple of electrical circuits since the 1800s, further reductions in the height of the capacitor are difficult to implement [13]. Because of that, substitutes such as the active capacitor are worth considering.

## 2.3 Two-terminal active capacitor

The active capacitor [13] utilizes a combination of passive circuit elements, in the form of smaller capacitors and inductors, and active power semiconductors. By employing an auxiliary circuit it can surpass the limitations of the passive capacitor regarding the dependency of the capacitance value on the plate area and on the properties of the dielectric, previously exemplified in Equation 2.2. Thanks to this structure, a performance that is equivalent to that of a much larger capacitor can be achieved by one with a significantly reduced height. The active capacitor represents a viable alternative to the conventional passive capacitor.

Its two-terminal (A and B) architecture greatly simplifies its installation and use in existing circuits, basically taking the same form as the traditional passive capacitor. The lack of additional terminals is possible thanks to two features of its design [13]: instead of an outside source for powering the controller and the gate drivers a self-power structure is implemented [32], and the control scheme is directly devised so that no external signals are used as feedback.

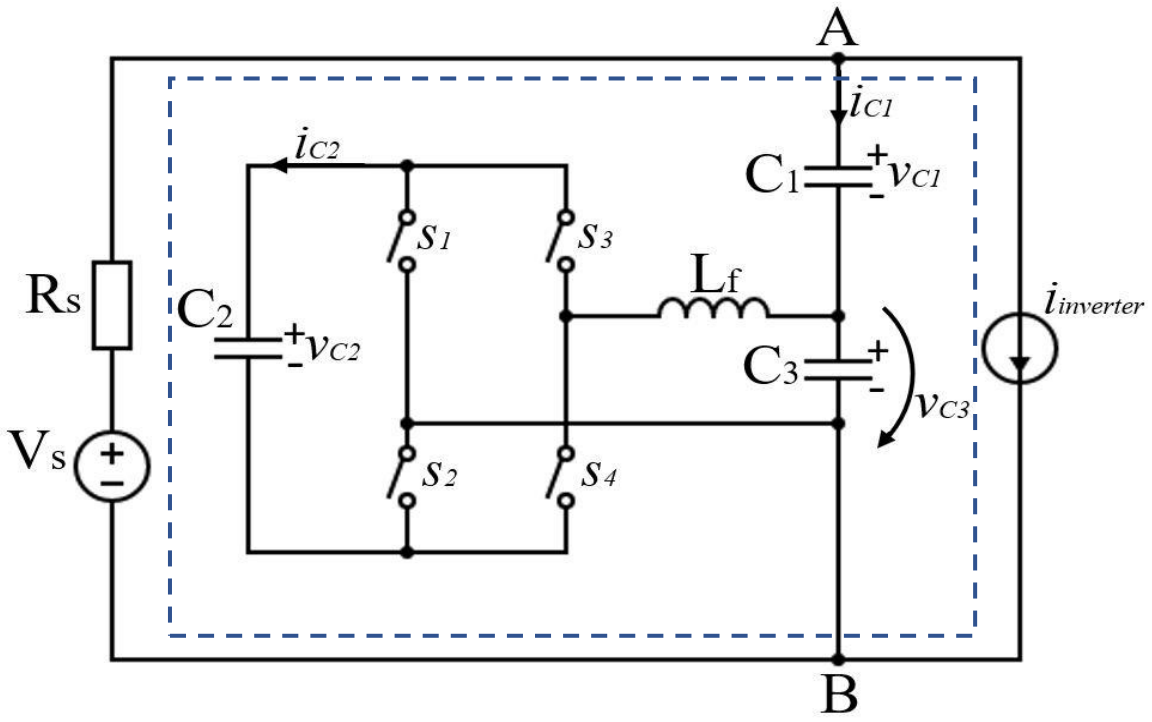


**Figure 2.6:** Structure of the active capacitor used in an inverter DC-link application

The structure of the active capacitor is shown in Figure 2.6 and is comprised out of a capacitor $C_1$ in series with an auxiliary circuit in the form of a full-bridge converter. $C_1$ serves the purpose of a conventional DC-link passive capacitor, mounted in parallel to the voltage supply $V_S$ with the internal resistance $R_S$, but with the benefit of a smaller required capacitance (and size) thanks to the presence of the auxiliary circuit. Another capacitor $C_2$ acts as the DC-link of this low-voltage auxiliary circuit, while at its output an LC harmonics filter is implemented, formed from an inductor $L_f$ and a capacitor $C_3$. By using the necessary control scheme, the switches $(S_i, i = \overline{1,4})$ are modulated so that the resulting output AC voltage across $C_3$ is equal in magnitude but of opposite sign to the ripple component $\Delta v_{C1}$ of the voltage across $C_1$, therefore canceling each other out. Ideally, only the DC $V_{AB}$ component will be seen as the bus voltage of the DC-link by the rest of the circuit, simplified in this diagram as an ideal current source $i_{inverter}$. This concept is exemplified in Figure 2.7. The control strategy used to obtain this behaviour is described in depth in Chapter 3.

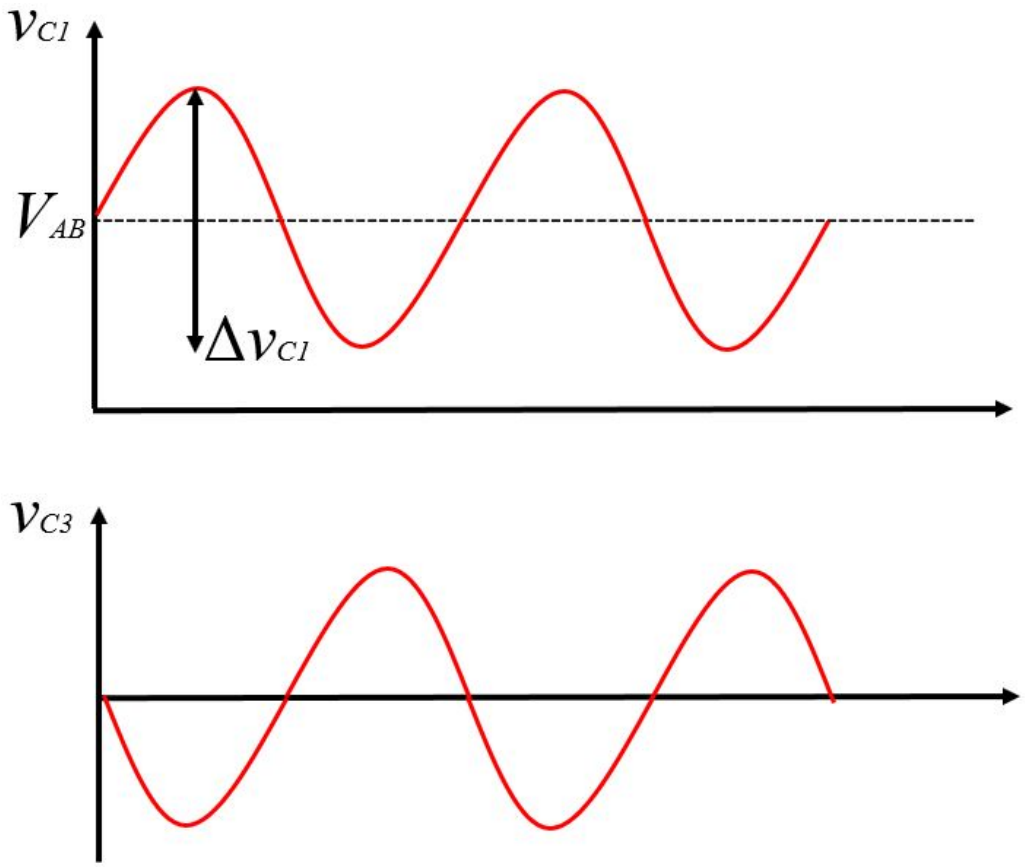


**Figure 2.7:** Waveforms of the ripple voltages across the capacitors C1 and C3

As already stated, the omission of an external power supply for the controller and for the drivers is possible thanks to the use of a self-power structure. One such structure is described in [32], which uses a combination of capacitors, inductors and diodes to power up each gate driver and the controller. A different method is attempted during the course of this project, which uses two voltage regulators supplied by being connected to $C_2$. The first regulator down-scales $v_{C2}$ down to a voltage level appropriate for powering up the gate drivers, while the second one is used to generate an even lower voltage, necessary for the controller. As they are supplied by $C_2$, which in turn is charged from the larger circuit, this creates another self-supply mechanism and allows the active capacitor to maintain its two-terminal characteristic.

This two-terminal structure and the possibility of emulating the characteristics of a conventional passive capacitor make the active capacitor a solution worth considering for use in several power electronics applications, one of which being as the DC-link of an embedded PV micro-inverter. The rest of this report will focus on ascertaining the feasibility of this concept for use in such an application.

Chapter 3

# System Characterisation

The first two chapters have described the context in which new solutions for the DC-link of solar micro-inverters are a topic worth researching. The following chapter will focus on further detailing the proposed active capacitor as an answer to the raised problem. This will cover both the control scheme of the circuit, as well as hardware considerations necessary for the given application.

As a general interpretation, the active capacitor, illustrated in Figure 2.6, would simply replace the conventional passive capacitor in the DC-link of the inverter. As mentioned in Section 2.3, this can easily be achieved thanks to its two-terminal characteristic, resulting in the overall circuit scheme for the two-stage inverter depicted in Figure 3.1.

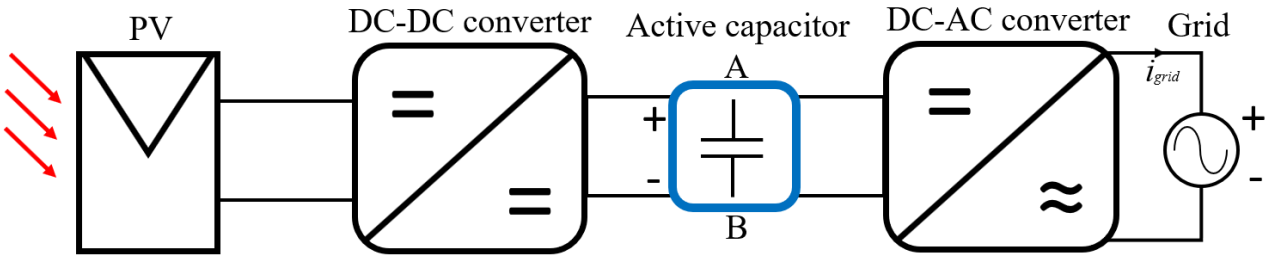


**Figure 3.1:** Diagram of a two-stage solar PV grid-connected inverter with active capacitor DC-link

## 3.1 Active capacitor control scheme

As exemplified by Figure 2.7, the main objective of the auxiliary circuit employed by the active capacitor is to generate an output voltage $v_{C3}$ which will mitigate the ripple resulted from the down-scaled $C_1$ passive capacitor, while maintaining the DC component $V_{AB}$. By doing so, the behaviour of the active capacitor, as seen from the AB terminals, will be the same as that of the conventional passive capacitor. For this purpose, the full-bridge converter previously depicted in Figure 2.6 is modulated according to the controller scheme proposed in [13] and presented in Figure 3.2.

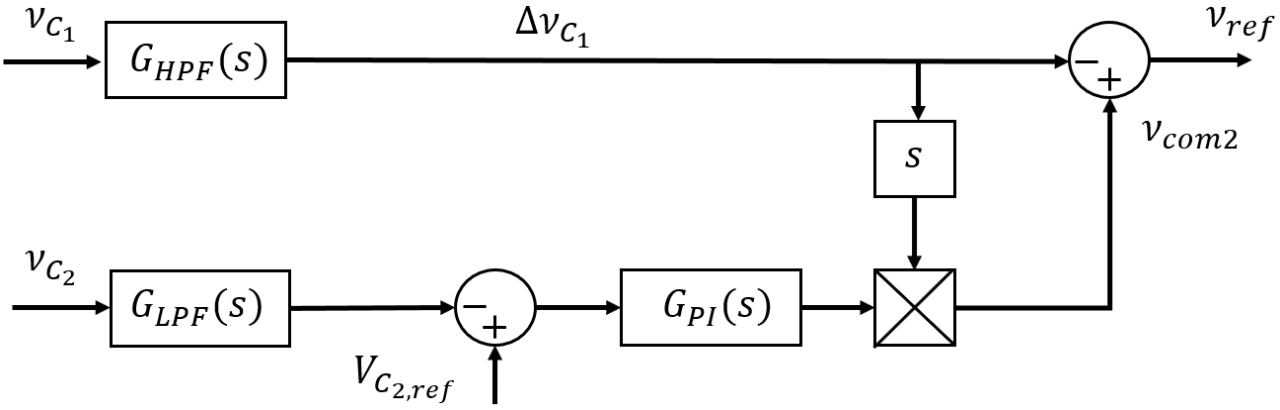


**Figure 3.2:** Control scheme for active capacitor [13]

This control algorithm is based on only two input signals, the voltages across the $C_1$ and $C_2$ capacitors.

Since both signals are measured inside the active capacitor this makes its control independent of the rest of the circuit in which it is employed. As mentioned in Section 2.3, the lack of any feedback signals external to the active capacitor is very advantageous, as it is one of the factors which allows for its two-terminal structure.

The control scheme is formed out of two separate control loops. The primary one is the upper loop, used to regulate the converter's output voltage, which has $v_{C1}$ as an input. This signal is then fed into a high-pass filter $G_{HPF}(s)$, that is used to extract the AC ripple component $\Delta v_{C1}$ of the input and to eliminate the DC component $V_{AB}$. The transfer function of the high-pass filter is:

$$G_{HPF}(s) = \frac{f_c s}{f_c\, s + 1} \tag{3.1}$$

where $f_c$ represents the cut-off frequency. The $\Delta v_{C1}$ signal is the first component of the reference voltage $v_{ref}$ and is used to control the auxiliary converter in order to obtain the necessary $v_{C3}$, according to Equation 3.2.

$$v_{C3} = -\Delta v_{C1} \tag{3.2}$$

The second control loop is used to regulate the voltage across $C_2$ to the desired value and to compensate for any power losses of the capacitor or of the auxiliary circuit. It generates $v_{com2}$, the second component of $v_{ref}$, used to control $v_{C2}$. $C_2$ is charged initially by extracting power from the larger circuit. It acts as the voltage source of the full-bridge converter and it is desired to be maintained at a constant voltage value $V_{C2,ref}$ which is chosen in the design stage. The input of this loop is $v_{C2}$, which is fed into a low-pass filter $G_{LPF}(s)$, with the transfer function given in Equation 3.3, in order to eliminate any high frequency components and to obtain its DC component.

$$G_{LPF}(s) = \frac{1}{f_c\, s + 1} \tag{3.3}$$

The difference between the resulting signal and $V_{C2,ref}$ is the error fed into a PI controller $G_{PI}(s)$, which works to eliminate it via the output $v_{PI}$. The transfer function of the PI controller is given in Equation 3.4, where $K_P$ and $K_I$ are the proportional and the integral gains, respectively.

$$G_{PI}(s) = K_P + \frac{1}{K_I} s \tag{3.4}$$

Considering that the purpose of this PI controller is to regulate the voltage across $C_2$, which already acts as the DC-link of this full-bridge inverter, then the use of this PI controller can be considered equivalent to the conventional DC-link voltage controller present in inverter applications, such as those described in Subsection 2.1. Because of that its design is greatly simplified, as it can be tuned based on the block-diagram provided in Figure 3.3 [33].

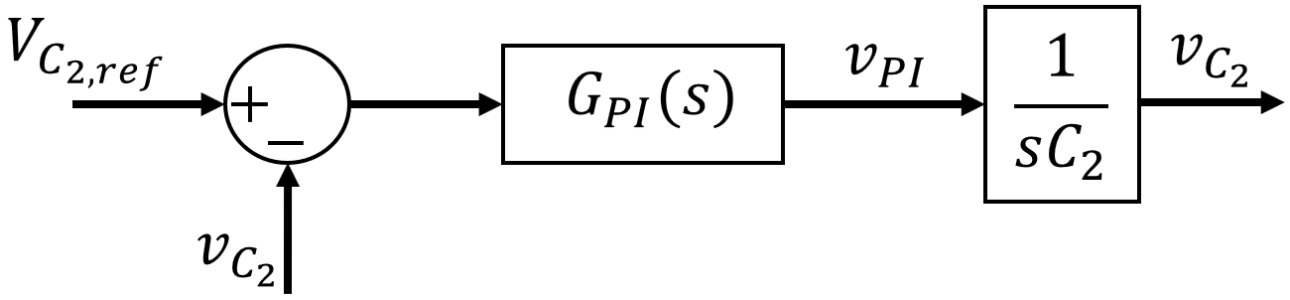


**Figure 3.3:** Block diagram of DC-link voltage controller used for $G_{PI}$ tuning [33]

The system has to absorb active power through the AB terminals from the external circuit in order to compensate for the losses of the full-bridge converter and to maintain $v_{C2}$ constant. This is a consequence of the two-terminal structure, which acts in this way in order to charge $C_2$, instead of using an external constant voltage source. This capacitor charge compensation scheme leads to additional switching instances for the power semiconductors of the auxiliary circuit, added to the ones resulting from the first control loop which are necessary to regulate $v_{C3}$. Nevertheless, the alternative would be using an external voltage source for the auxiliary full-bridge converter, which would eliminate the convenience of the two-terminal structure presented in Section 2.3, or using an additional battery connected to $C_2$, which would maintain the two-terminal characteristic, but would lead to extra high costs associated with the price of the battery. Therefore, this out-weights the disadvantage of the extra semiconductors switching, leading to the use of the control scheme in Figure 3.2 and of the self-charge mechanism.

In order to absorb the necessary active power, $v_{com2}$ and $i_{C1}$ have to be synchronized, which is equivalent to a 90° phase shift between $v_{com2}$ and $\Delta v_{C1}$, introduced in the control scheme by use of a product between $v_{PI}$ and the derivative of $\Delta v_{C1}$, resulting in $v_{com2}$ [13].

The outputs of the two control loops form the reference signal $v_{ref}$, based on the formula given by Equation 3.5.

$$v_{ref} = (V_{C_{2,ref}} - v_{C2}\, G_{LPF}(s))\, G_{PI}(s)\, s\, v_{C1}\, G_{HPF}(s) - v_{C1}\, G_{HPF}(s) \tag{3.5}$$

This is then fed into a sinusoidal pulse-width modulation (PWM) algorithm, resulting in the modulation signal $m$ in Equation 3.6, where $V_{tri}$ is the amplitude of the carrier triangular wave of the PWM. These pulses are used for the control of the full-bridge converter.

$$m = \frac{v_{ref}}{V_{tri}} \tag{3.6}$$

Therefore, by modulating the four power switches accordingly, both the $\Delta v_{C1}$ ripple mitigation function, as well the $v_{C2}$ voltage stabilisation, can be achieved.

## 3.2 Active capacitor circuit elements

The most important step in the design of the active capacitor is represented by the choice of the necessary components. These were previously depicted in Figure 2.6, ranging from passive components

to power semiconductors.

The following section focuses on describing the theoretical considerations by which the sizing of the components is realised. General sizing equations are derived which are applicable to different cases depending on the specifications of the applications in question. Additionally, the requirements of these applications also lead to direct restrictions regarding these components, such as the minimum lifetime and the maximum height. These are combined with an overall objective of minimizing the cost.

### 3.2.1 Capacitor $C_1$

The smaller $C_1$ capacitor represents the main passive element of the active capacitor design, as it acts as the direct replacement of the conventional bulkier DC-link capacitor. Thus, the DC-bus voltage $V_{AB}$ appears entirely on $C_1$. While the smaller capacitor brings the benefit of the desired height reduction, it also leads to the consequence of a reduced capacitance, leading to significant values of the voltage ripple $\Delta v_{C1}$ [13]. Therefore, the components of the $v_{C1}$ voltage, previously depicted in Figure 2.7, can be described by Equation 3.7.

$$v_{C1} = V_{AB} + \Delta v_{C1} \tag{3.7}$$

These resulting ripple values would not be sustainable in any DC-link application, as they would lead to, in the best case, an extreme reduction of the expected lifetime of components due to the added stress and, in the worst case, even to an unstable DC-link. Therefore, the downsized $C_1$ capacitor is coupled with the auxiliary circuit, which is utilized to mitigate the resulting additional ripple voltage by generating the opposing $v_{C3}$. With assistance from the auxiliary full-bridge converter the active capacitor can maintain the benefits of the smaller $C_1$, while eliminating its disadvantages.

The interaction between $C_1$ and the auxiliary circuit results in an important sizing criteria for the former of the two. Essentially, the capacitance of $C_1$ is what determines the amount of apparent power $S_{aux}$ directed towards the auxiliary circuit and the efficiency of the active capacitor [13]. The lower the $C_1$ capacitance is, the higher the $\Delta v_{C1}$ ripple becomes, following the same principle described by Equation 2.1. Accordingly, the first loop of the control scheme described in the previous section will counteract $\Delta v_{C1}$, generating an increased $v_{C3}$, based on Equation 3.2. As a consequence, as the modulation index of the full-bridge converter is increased, this will also result in a faster discharging of $C_2$ and in increased losses, which will have to be compensated by the second control loop. Overall, the entire apparent power amount handled by the auxiliary converter is increased to mitigate the effects of the reduced $C_1$. Accordingly, the opposite is valid if a $C_1$ with a higher capacitance is chosen, with $S_{aux}$ decreasing. Therefore, a balance has to be determined between the value of the $C_1$ capacitance, which might be limited by height limitations of the capacitor and by cost, and the acceptable value of $S_{aux}$, as well as of the resulting system efficiency.

The current $i_{C1}$ running through the active capacitor circuit is determined by the equation:

$$i_{C1} = I_{C1} \cos(\omega t + \delta) \tag{3.8}$$

in which $I_{C1}$ is the amplitude, $\omega$ is the ripple frequency and $\delta$ is the phase shift of the current [13]. As a simplification, Equation 3.8 only considers the fundamental component of $i_{C1}$.

An important point has to be made about the ripple frequency $\omega$ before the theoretical design of the active capacitor can be continued, that point being that $\omega$ is equal to twice the grid angular frequency $\omega_{grid}$ in the case of a grid connected single phase inverter [16]. This can be proved by using Equation 3.9 for determining the instantaneous output inverter power $p_{grid}$, in which $i_{grid}$ and $v_{grid}$ are the current being fed into the grid and the grid voltage, respectively, with $I_{grid}$ and $V_{grid}$ being their amplitudes [34].

$$p_{grid}(t) = v_{grid}(t)\, i_{grid}(t) = \sqrt{2}\, V_{grid}\, \cos\omega_{grid}t\, \sqrt{2}\, I_{grid}\, \cos\omega_{grid}t = V_{grid}\, I_{grid}\, (1 + \cos 2\omega_{grid}t) \quad (3.9)$$

As previously described in Chapter 2, the DC-link acts to compensate the power imbalance between the DC and the AC sides of the inverter. This means that the power variation at $2\omega_{grid}$ will be reflected in the DC-link in the form of a voltage variation applied on top of the constant $V_{AB}$ voltage, leading to the behaviour described by Equation 3.7, causing the ripple component $\Delta v_{C1}$ to vary at a frequency $\omega$ twice that of $\omega_{grid}$ [34].

The ripple voltage $\Delta v_{C1}$ is described by:

$$\Delta v_{C1} = \frac{1}{2}\Delta V_{C1} \sin(\omega t + \delta) \quad (3.10)$$

in which $\Delta V_{C1}$ represents the peak to peak ripple voltage across $C_1$. Accordingly, by substituting Equation 3.10 into Equation 3.7, the equation for $v_{C1}$ is obtained:

$$v_{C1} = V_{AB} + \frac{1}{2}\Delta V_{C1} \sin(\omega t + \delta) \quad (3.11)$$

On the other hand, based on Equation 3.2, the equation for $v_{C3}$ becomes:

$$v_{C3} = -\frac{1}{2}\Delta V_{C1} \sin(\omega t + \delta) \quad (3.12)$$

The apparent power $S_{aux}$ can be determined as the product of the rms values of the output voltage $v_{C3}$ of the auxiliary circuit and of the current $i_{C1}$ through the active capacitor [13]. Based on Equations 3.12 and 3.8, this results in Equation 3.13.

$$S_{aux} = \frac{\Delta V_{C1}}{2\sqrt{2}} \frac{I_{C1}}{\sqrt{2}} \quad (3.13)$$

The total power $S_{main}$ is considered as the product of the average terminal voltage $V_{AB}$ and of $I_{C1}$ [13], resulting in:

$$S_{main} = V_{AB} I_{C1} \quad (3.14)$$

Accordingly, by considering $\varepsilon_S$ as the ratio between the apparent power $S_{aux}$ transferred to the auxiliary circuit from the total apparent power $S_{main}$ the result becomes:

$$\varepsilon_S = \frac{S_{aux}}{S_{main}} = \frac{\Delta V_{C1}}{4 V_{AB}} \quad (3.15)$$

By rearranging the terms of Equation 2.1 and adapting them for the case of $C_1$ the relationship between its capacitance and the ripple voltage can be obtained:

$$\Delta V_{C1} = \frac{2I_{C1}}{\omega C_1} \tag{3.16}$$

and substituted into Equation 3.15 to obtain the relationship between the relative power consumption of the auxiliary system and the capacitance of $C_1$.

$$\varepsilon_S = \frac{S_{aux}}{S_{main}} = \frac{I_{C1}}{2\omega C_1 V_{AB}} \tag{3.17}$$

Finally, Equation 3.18 can be formed to represent the minimum $C_1$ as a function of $\varepsilon_S$.

$$C_1 \geq \frac{I_{C1}}{2\omega\varepsilon_S V_{AB}} \tag{3.18}$$

This equation is the analytical proof that the $C_1$ capacitance and the power ratio $\varepsilon_S$ are inverse proportional, with a decreased capacitance resulting in a higher apparent power used by the auxiliary circuit. Thus, these two parameters have to be balanced accordingly in the design phase of the system, based on how much power out of the total is acceptable to be used by the auxiliary circuit in order to minimize the ripple voltage across $C_1$.

### 3.2.2 Capacitor $C_2$

The next step in the design of the active capacitor is represented by the determination and the choice of $C_2$. The values of $v_{C2}$ and $C_2$ are directly influenced by the previous choice of $C_1$, seeing as $C_2$ acts as the DC-link of the full-bridge converter auxiliary circuit, as can be observed from the structure of the circuit in Figure 2.6. Since $v_{C3}$ is the output voltage of the full-bridge, the relationship between it and the input $v_{C2}$ is described by Equation 3.19.

$$v_{C3} = m\, v_{C2} \tag{3.19}$$

Seeing as the modulation index has to be a maximum of 1 in order for $C_2$ to be able to correctly supply the necessary input voltage, without going into overmodulation range, to obtain the desired $v_{C3}$, the relationship between the two voltages becomes [16]:

$$v_{C2} \geq v_{C3} \tag{3.20}$$

If Equations 3.2 and 3.10 are also considered, then the relationship can be written as:

$$v_{C2} \geq \frac{\Delta V_{C1}}{2} \tag{3.21}$$

which proves the relationship between the required DC-link voltage of the full-bridge converter and the amplitude of the ripple component of $v_{C1}$. Considering that $\Delta v_{C1}$ is also dependent on the choice of

$C_1$, as was characterized by Equation 3.16, then the dependency between the two capacitors is already proved indirectly.

Therefore, the first restriction regarding $C_2$ is that it must withstand a voltage level at least equal to the amplitude of the ripple component determined by $C_1$, with an added safety margin. Finally, once the desired value for $v_{C2}$ was chosen based on Equation 3.21, the controller scheme described in the previous section is adapted by using this value as $V_{C2,ref}$, which will stabilise and maintain the voltage across $C_2$ at the expected value.

The second restriction, meaning the minimum $C_2$ capacitance, is obtained by initially rewriting Equation 3.19, while considering the fact that $m$ has to be at most 1, into the following:

$$m = \frac{v_{C3}}{v_{C2}} \leq 1 \tag{3.22}$$

Both terms have to be substituted in order to reach the final equation. $v_{C3}$ is replaced using Equation 3.12, in which $\Delta V_{C1}$ has been substituted using Equation 3.16. $v_{C2}$ has to be substituted accordingly, starting from Equation 3.23, which equates the instantaneous power in $C_2$ with the power at the terminals of $C_3$, under the assumption that there are no power losses in the auxiliary circuit.

$$v_{C2} i_{C2} = v_{C3} i_{C1} \tag{3.23}$$

In this equation $i_{C2}$ can simply be replaced using the general equation for current flowing through a capacitor:

$$i_{C2} = C_2 \frac{dv_{C2}}{dt} \tag{3.24}$$

Additionally, by substituting the $i_{C1}$ current with Equation 3.8 and the $v_{C3}$ voltage with Equation 3.12, Equation 3.23 can be written in the form:

$$C_2\, v_{C2} \frac{dv_{C2}}{dt} = \frac{I_{C1}^2}{\omega C_1} \cos(\omega t + \delta) \sin(\omega t + \delta) \tag{3.25}$$

This is a first-order differential equation. According to [16], the general solution for this equation is:

$$v_{C2} = \sqrt{V_{C2,dc}^2 - \frac{I_{C1}^2}{2\omega^2 C_1 C_2} \cos 2\omega t} \tag{3.26}$$

where $V_{C2,dc}$ represents the average value $v_{C2}$ and is equal to the desired value $V_{C_{2,ref}}$, previously chosen based on the first restriction for $C_2$. Using Equation 3.26, $v_{C2}$ can also be substituted in Equation 3.22, resulting in:

$$\frac{v_{C3}}{v_{C2}} = \frac{\frac{I_{C1}}{\omega C_1} \cos \omega t}{\sqrt{V_{C2,dc}^2 - \frac{I_{C1}^2}{2\omega^2 C_1 C_2} \cos 2\omega t}} \leq 1 \tag{3.27}$$

Considering that the maximum value for this equation can be obtained when $\omega t$ is 0, $\pi$, $2\pi$..., then it is sufficient that the maximum value still satisfies the condition of being less than or equal to 1. Therefore the expression will result in:

$$\frac{v_{C3}}{v_{C2}} = \frac{\frac{I_{C1}}{\omega C_1}}{\sqrt{V_{C2,dc}^2 - \frac{I_{C1}^2}{2\omega^2 C_1 C_2}}} \leq 1 \tag{3.28}$$

After further rearranging the terms and simplifying, this equation becomes:

$$\frac{I_{C1}}{\omega} \leq C_1 V_{C2,dc} \sqrt{\frac{2C_2}{2C_2 + C_1}} \tag{3.29}$$

The final form of this equation is written to express the dependency of $C_2$ on $C_1$ and $V_{C2,dc}$:

$$C_2 \geq \frac{I_{C1}^2 \frac{C_1}{2}}{(\omega C_1 V_{C2,dc})^2 - I_{C1}^2} \tag{3.30}$$

This relationship results in the second restriction regarding $C_2$, dealing with the minimum capacitance required for specific values of $C_1$ and $V_{C2,dc}$. Knowing that the desired DC-value of $v_{C2}$ was also a consequence of the choice of $C_1$, then the entire equation can be treated as another proof of the dependency of $C_2$ on $C_1$. As it was made evident in this subsection, the choices of $C_1$ and $C_2$ capacitors are closely linked together and cannot be designed separately.

### 3.2.3 Capacitor $C_3$ and inductor $L_f$ of the LC filter

The last of the major passive components of the active capacitor topology are represented by the inductor $L_f$ and by the capacitor $C_3$. Their role in the circuit and their general theoretical sizing criteria are covered in the following subsection.

As previously described, the voltage generated across $C_3$ is the primary mechanism by which the auxiliary circuit can counteract the voltage ripple $\Delta v_{C1}$. This voltage $v_{C3}$ is achieved and controlled by employing the power switches of the full-bridge converter according to the control scheme described in Section 3.1, therefore acting as the output of the converter. Thus, as it was also expressed by Equations 3.2 and 3.20, an essential constraint of $C_3$ is that it must withstand a voltage high enough to accomplish its ripple mitigation role, with an added safety margin.

Additionally $C_3$, paired with the inductor $L_f$, form the LC filter connected at the output of the full-bridge. Coupled together with the converter this results in the assembled auxiliary circuit depicted in Figure 2.6. Therefore $C_3$ has a double role. The first one is as the circuit element across which the voltage opposing the ripple component of $v_{C1}$ is generated, while the second one as part of the LC harmonics filter.

An LC filter is used for the full-bridge converter due to the presence of harmonics caused by the switching of semiconductors. Using only one series inductor for the filter is another common option, but it would result in a large value for the inductance in order to properly reduce the current harmonics created around the switching frequency. This would lead to issues regarding the inductor's size, cost

and high power losses. Because of that an LC filter is preferred, as it can achieve the same harmonic attenuation with a lower size, cost and total inductance [35].

The switching harmonics are not desirable in the output $v_{C3}$ as they would negatively impact the overall voltage at the terminals of the DC-link. Therefore, $C_3$ and $L_f$, acting as a low-pass filter, are introduced at the output of the full-bridge, with the objective of attenuating these high-frequency harmonics and creating an output voltage with a sinusoidal waveform, similar to the waveform of the ripple component $\Delta v_{C1}$.

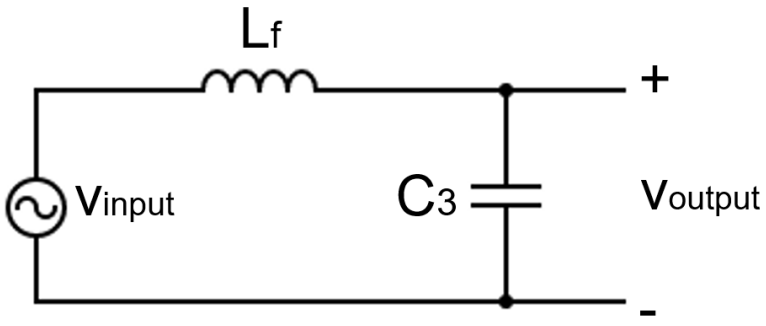


**Figure 3.4:** Diagram of standard LC filter

The inductor $L_f$ dictates the ripple component of the inductor current and mitigates the low frequency harmonics [25]. The value of the inductance is a function of the ripple current. This relationship can be expressed as [17]:

$$\Delta I_{L,max} = \frac{v_{C2}}{2L_f f_{sw}} \tag{3.31}$$

in which $\Delta I_{L,max}$ is the maximum current ripple and $f_{sw}$ represents the switching frequency of the full-bridge of the auxiliary circuit. The maximum current ripple occurs when the input voltage $v_{C2}$ is at the peak and when the output voltage $v_{C3}$ of the full-bridge is at 0 V. Considering that, Equation 3.31 can be rewritten as:

$$\Delta I_{L,max} = \frac{\sqrt{V_{C2,dc}^2 + \frac{I_{C_1}^2}{2\omega^2 C_1 C_2}}}{2L_f f_{sw}} \tag{3.32}$$

According to [25], the ratio between $\Delta I_{L,max}$ and the load current is usually chosen between 5% to 25%. By reducing the ripple current as much as possible the conduction and switching losses of the semiconductors are significantly lowered, but it will also results in a larger filter inductor, generating higher core and coil losses.

Finally, after considering a desired value for for $\Delta I_{L,max}$, Equation 3.32 can be rearranged in order to obtain the sizing criteria for $L_f$ in Equation 3.33.

$$L_f = \frac{\sqrt{V_{C2,dc}^2 + \frac{I_{C_1}^2}{2\omega^2 C_1 C_2}}}{2\Delta I_{L,max} f_{sw}} \tag{3.33}$$

The value of $C_3$ capacitance depends on the characteristics of the system in question, such as its requirements regarding the total harmonic distortion THD. This would primarily affect the value of the chosen cutoff frequency $f_{LC}$, as the level of attenuation at specific frequencies would be influenced by it [17]. The choice of $f_{LC}$ has to result in an LC filter which attenuates the high frequency noise as much as possible, while ensuring that none of the desired low frequency component is affected. Nevertheless, this project does not have a strong requirement regarding the THD value of $v_{C3}$, so the choice of $f_{LC}$ is not heavily restricted.

The relationship between the frequency $f_{LC}$ and the passive elements of the LC filter is described by Equation 3.34.

$$f_{LC} = \frac{1}{2\pi L_f C_3} \tag{3.34}$$

Having already determined the value of the inductance $L_f$ and having chosen a desired cutoff frequency $f_{LC}$, the minimum value for the capacitance $C_3$ can be determined by rearranging the terms of Equation 3.34 into Equation 3.35.

$$C_3 \geq \frac{1}{4\pi^2 f_{LC}^2 L_f} \tag{3.35}$$

In conclusion, Equations 3.33 and 3.35 are the main sizing criteria of the LC harmonics filter incorporated in the auxiliary circuit, with the final values of $L_f$ and $C_3$ being influenced by design choices such as the ripple current $\Delta I_{L,max}$ and the cutoff frequency $f_{LC}$.

## 3.3 Auxiliary circuit components

### 3.3.1 Power switches

With the choice of passive elements explained, the following subsection is dedicated to the power semiconductors forming the full-bridge converter of the auxiliary circuit. This topology was also described by Figure 2.6.

The first restriction, which can be immediately determined, is that the voltage rating of the power semiconductors has to withstand the necessary operational voltage. Considering Equation 3.19, the maximum output voltage $v_{C3}$ would occur at a modulation index of 1 and it would be equal to $v_{C2}$. However, the final withstand voltage of the semiconductors has to allow for a substantial safety margin. According to [36], a desired withstand voltage can be chosen based on the characteristics of the application in question, such as the reliability of the supply and the presence of over-voltage protections. Additionally, it is also stated that a withstand voltage of twice the value of the nominal rms voltage is sufficient for most industrial applications.

Overall, a balance has to be maintained for the final rating. If its value is too close to the nominal operating point, then a large risk of failure is present. On the other hand, if the voltage rating is exaggerated compared to the nominal value, then the system's performance and efficiency will be negatively affected. This is caused by the fact that higher rated semiconductor devices demand thicker silicon layers, leading to higher losses [36].

Apart from the operational safety requirement, the expected voltage rating of the application will also usually influence the choice of the type of semiconductor picked, as each type of power switch is better suited for a different voltage level. For example, according to [37], the power metal–oxide–semiconductor field-effect transistor MOSFET is the preferred device for voltage levels of up to around 1 kV. On the other hand, the insulated-gate bipolar transistor IGBT is better suited for voltage ratings higher than 1 kV. Other options, such as the bipolar junction transistor (BJT) or the gate turn-off thyristor (GTO), are heavily restricted when it comes to their operating frequencies.

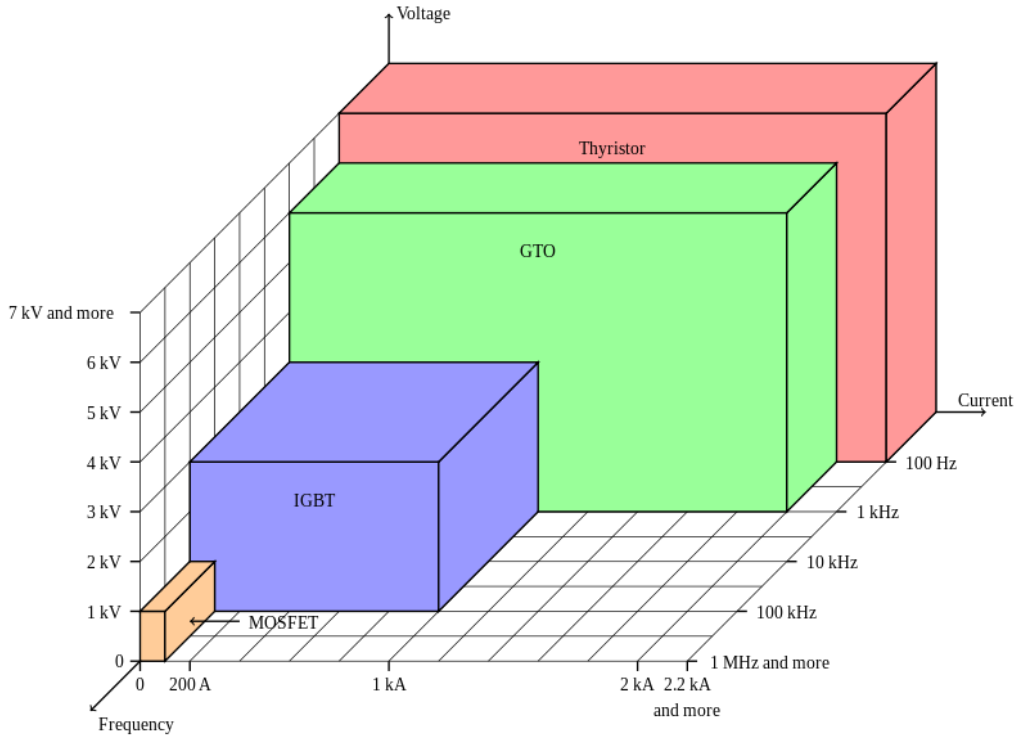


**Figure 3.5:** Representation of the voltage, current and frequency ranges of different power switches [38]

As previously mentioned in Section 2.2 micro-inverters operate at low-voltage levels, since they are connected to a single PV panel. Because of that, MOSFETs are the preferred semiconductor solution for them [7].

As an added benefit, while MOSFETs are incapable of sustaining high voltage levels, they are significantly better suited for increased switching frequencies, being able to operate at as high as 1 MHz [37]. This adds an important benefit to any converter application, as the possibility of using an increased switching frequency would benefit the performance of the system by reducing the harmonic content of the output signal. These two factors are also applicable for the full-bridge converter of the auxiliary circuit. Therefore, MOSFETs were chosen as the type of semiconductors used during this project.

Another important factor to consider in the selection of power semiconductors is the maximum allowable junction temperature. This has to be sufficient to withstand the expected operating temperature determined during the design process of the application.

Before the operating junction temperature can be approximated the expected power losses of the semiconductors have to be determined. There are two types of possible losses for MOSFET devices: conduction losses and switching losses [39]. The instantaneous MOSFET conduction losses are

described by:

$$p_{CD}(t) = u_{DS}(t)\, i_D(t) = r_{DS}\, i_D^2(t) \tag{3.36}$$

in which $u_{DS}(t)$ represents the instantaneous drain-source voltage, $i_D(t)$ the instantaneous drain current and $r_{DS}$ is the internal drain-source resistance. By integrating Equation 3.36 over one MOSFET switching period ($T_{sw}$) the relationship used to determinee the average conduction losses is obtained in Equation 3.37. $I_{Drms}$ represents the rms value of the drain current.

$$P_{CD} = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_{CD}(t)\, dt = r_{DS}\, I_{D,rms}^2 \tag{3.37}$$

$r_{DS}$ is determined based on information from the product's datasheet, while $I_{Drms}$ depend on the nominal operating point of the application in question.

The second possible source of MOSFET power losses, the switching losses, are determined by using Equation 3.38 [39]. These losses are influenced by the switching frequency utilised and by the load characteristics.

$$P_{SW} = V_{DS,rms}\, I_{D,rms}\, f_{sw}\, \frac{Q_{GS} + Q_{GD}}{I_G} \tag{3.38}$$

In the above equation, $Q_{GS}$ and $Q_{GD}$ are the electrical gate-source charge and gate-drain charge. They are needed for the gate driver to charge the MOSFET and they can be determined based on the product's datasheet, while $I_G$ is the gate current, the value of which is a design choice. Overall, Equation 3.38 describes the total switching losses required to drive the gate, for both the turn-ON and turn-OFF actions.

Once the conduction and switching losses are known, then the total expected power loss can be calculated as the sum of the two.

$$P_{loss} = P_{CD} + P_{SW} \tag{3.39}$$

If these power losses are high enough, when compared to the total operating power, then the question of efficiency becomes a problem. However, their biggest consequence is that they lead to an increase in the operational temperature of the power switches. If this increase is significant it might lead to a junction temperature $T_j$ above the rated maximum value from the datasheet, potentially leading to the failure of the MOSFET.

Considering this risk, each application has to be carefully designed so that it can be guaranteed that the maximum temperature is not exceeded. The relationship between the expected power losses and the resulting junction temperature rise is described by Equation 3.40 [40].

$$\Delta T_j = T_j - T_a = P_{loss}\, (R_{thJC} + R_{thCA}) \tag{3.40}$$

In this equation $R_{thJC}$ and $R_{thCA}$ represent the thermal resistance from the junction to the case and from the case to the ambient, respectively. Both of these depend on the characteristics of the device. If

the ambient temperature $T_a$ is approximated based on standards, then the equation can be rewritten to obtain the expected operating junction temperature.

$$T_j = T_a + P_{loss} \left( R_{thJC} + R_{thCA} \right) \tag{3.41}$$

If this resulting temperature is lower by a significant margin when compared to the maximum allowable junction temperature, then MOSFET can be operated in the specified application without the use of an additional heatsink [40]. This is desirable in order to simplify the design process and to reduce the use of extra component. Therefore, the final choice of MOSFETs should provide a satisfying safety margin regarding the maximum junction temperature, based on the design of the application, leading to another requirement concerning the choice of power switches.

### 3.3.2 Gate drivers

Another very important component necessary for the operation of the full-bridge auxiliary converter, next to the power switches themselves, is the gate driver. It represents the intermediary between the power module and the outputs of the controller. Because of this role, the selection of the gate driver and the calculation of its associated parameters are an important step in any converter application. If the driver fails to correctly power the gate of the power switch then this might result in the malfunctioning of both the power module and of the driver.

The switching characteristics of the turn-ON and turn-OFF sequences of a MOSFET module are affected by its semiconductor structure, by the presence of internal capacitances and by the values of the external and internal gate resistors [41].

#### Gate charge $Q_{gate}$

In the design process of a MOSFET gate driver, when determining the output power necessary to drive the MOSFET gate, the deciding specification comes in the form of the gate charge. This parameter is determined by the corresponding internal capacitances: gate-drain $C_{GD}$, gate-source $C_{GS}$ and drain-source $C_{DS}$ [41].

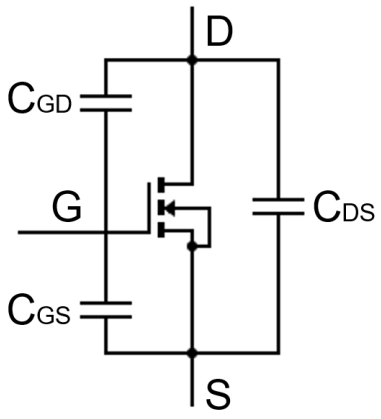


**Figure 3.6:** MOSFET input capacitances

These three internal capacitances have a significant effect on the turn-ON process. In fact, the result is that the entire process of turning-ON the MOSFET becomes divided into three subsequent parts. The resulting stages of the switching process are: charging the gate-source capacitor $C_{GS}$, charging the gate-drain capacitor $C_{GD}$ and, finally, charging the gate-source capacitor again until the MOSFET is fully saturated and the gate has been fully energized.

In order to determine the value of these gate charges, corresponding to the internal capacitances, the gate charge characteristic of the device has to be used. This characteristic describes the variation of the gate-source $V_{GS}$ with respect to the gate charge $Q_{gate}$ value and is provided in the data sheet of the MOSFET. A general representation of this characteristic is presented in Figure 3.7.

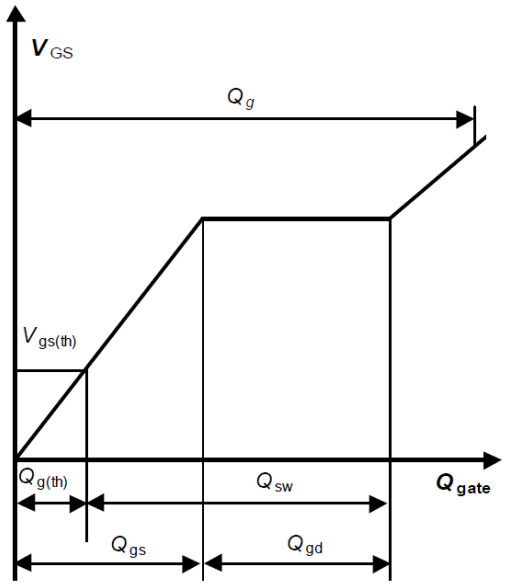


**Figure 3.7:** General representation of the gate charge characteristic of a MOSFET [42]

In Figure 3.7 $V_{gs(th)}$ and $Q_{gs(th)}$ represent the threshold voltage and the threshold gate charge, respectively, while $Q_{sw}$ is the switching charge. $Q_{gs}$ and $Q_{gd}$ are the gate to source and the gate to drain charges. The gate charge $Q_{gate}$ is theoretically described by Equation 3.42 as the variation of current $i$ in time.

$$Q_{gate} = \int i\,dt \tag{3.42}$$

However, using the gate charge characteristic provided in the data sheet greatly simplifies its calculation, assuming the desired gate voltage $V_{GS}$ is already known.

### Gate voltage $V_{GS}$

Therefore, the value of the gate charge is linked to another important parameter in the design of the gate driver, which is the desired output gate-source voltage $V_{GS}$. Its value is a design choice that must fulfill a series of aspects in order to guarantee the proper switching of the MOSFET.

Firstly, this applied voltage has to surpass the threshold gate-source voltage by at least a small margin so that the gate can be reliably energized. Otherwise the device will not conduct. Therefore a minimum

value is set by the threshold constraint and is supplied in the data sheet of the device.

Secondly, the structure of the MOSFET limits the range of the possible $V_{GS}$ values, therefore also resulting in a maximum admissible value. However, in order to avoid any possible damage occurring on the gate of the MOSFET, the choice of $V_{GS}$ should include a safety margin, so that the maximum value is guaranteed to not be exceeded. Nevertheless, the range of admissible $V_{GS}$ is once again supplied by the manufacturer in the data sheet of the device.

$$V_{GS} = R_G \, I_G \tag{3.43}$$

Overall, a balance has to be achieved between a gate-source voltage high enough to exceed the threshold value, which would energize the gate of the MOSFET in a fast and reliable manner, and a value low enough that would guarantee the safety of the device.

#### Gate resistor $R_G$

The gate resistors $R_G$ is another component with a large influence on the switching behaviour of the MOSFET. A gate resistor that it not properly optimized could raise significant problems leading to large spikes of the gate voltage or overly extended switching periods, while it also affects the drain-source voltage rise time. Because of its significance, an external gate resistor is usually added to any gate driver application, next to the already existing resistor $R_{G,in}$ internal to the power switch [43].

As stated above, the switching behaviour of MOSFETs is heavily influenced by the gate resistor. The input capacitances mentioned before, gate-source $C_{GS}$ and gate-drain $C_{GD}$, have to be charged and then discharged at every ON/OFF switching interval. With the applied pulse voltage $V_{GS}$ the resistor $R_G$ is limiting the gate current $I_G$ and is, therefore, controlling the time needed for the input capacitances to charge. This can be proved by starting from Equation 3.43 and rearranging the terms accordingly, resulting in Equation 3.44. This is the relationship based on which the peak gate current is determined [44].

$$I_G = \frac{V_{GS}}{R_G} = \frac{V_{GS(on)} - V_{GS(off)}}{R_G + R_{G,in}} \tag{3.44}$$

In this equation $V_{GS(on)}$ represents the value of the gate voltage applied during the ON state of the switch, usually a positive value above the threshold voltage, and $V_{GS(off)}$ is the value applied during the OFF state, usually a negative value or 0.

The positive aspect of an increased peak gate current, obtained by using a reduced $R_G$, is that the input capacitances will charge significantly faster. This will lead to reduced turn-ON and turn-OFF instances, therefore also reducing the switching losses [43]. On the other hand, $R_G$ can also not be reduced bellow a certain value. This is because of the large current rise di/dt that occurs when large current are switched in fast intervals. Coupled with the stray inductances that exist in the larger circuit, this results in large voltage spikes on the MOSFET. This behaviour is described by Equation 3.45 [44].

$$V_{stray} = L_\sigma \, \frac{di}{dt} \tag{3.45}$$

The reason why the gate resistor is important for this relationship and why its value cannot pass bellow a certain point is that $R_G$ acts to lower and limit the current rise di/dt. Therefore, the $V_{stray}$ is reduced by increasing $R_G$, eliminating the risk of the MOSFET being damaged by the resulting large voltage spike [44].

In order to simplify the gate circuit, the same resistor can be used for both ON/OFF switching, as opposed to using separate ones for each instance [44]. Therefore, the control of the gate is symmetrical. However, if this configuration is used then the gate driver or the controller must include a dead time to avoid any potential short circuits in the MOSFET.

Overall, when deciding on a value for the gate resistor $R_G$, a number of criteria have to be considered. The value of the resistor has to be larger enough that it guarantees that the MOSFET is safe from any damage caused by the large voltage spike in Equation 3.45. At the same time, it should be minimized as much as possible in order to reduced the switching times and the resulting losses. According to [44], the value of a gate resistor should usually be chosen from a range between the value given by the data sheet of the MOSFET, obtained under the specified test conditions, and double that amount. In this case, the resistance provided in the data sheet is the minimum value, which might not actually be appropriate depending on the application. Twice the value can be used as a rough approximation for a maximum limit.

### Gate driver specifications

Once the desired gate voltage $V_{GS}$ and external gate resistor $R_G$ have been calculated the specifications based on which the gate driver is chosen can be determined. As previously mentioned, the gate charge $Q_{gate}$ is determined from the gate charge characteristic once $V_{GS}$ is known. Following that, the average current output of the driver can be calculated using Equation 3.46, with the switching frequency already chosen during the MOSFETs selection process, while the peak current output has previously been described by Equation 3.44.

$$I_{G,av} = Q_{gate}\, f_{sw} \tag{3.46}$$

Finally, the necessary power that the gate driver has to generate in order to drive the gate of the MOSFET is determined by Equation 3.47.

$$P_G = I_{G,av}\,(V_{GS(on)} - V_{GS(off)}) \tag{3.47}$$

For the purpose of expressing this relationship as a function of the primary design parameters $Q_{gate}$, $f_{sw}$ and $V_{GS}$, Equation 3.46 is substituted into Equation 3.47, leading to the final relationship in Equation 3.48, which the choice of gate driver has to satisfy.

$$P_G = Q_{gate}\, f_{sw}\,(V_{GS(on)} - V_{GS(off)}) \tag{3.48}$$

### 3.3.3 Final design

This section has focused on presenting the theoretical specifications by which the passive and active elements of the active capacitor circuit have to be selected, ranging from the electrical ratings to the properties of the component. The mentioned selection criteria are determined based on each individual application. Particularly, in the case of the solar micro-inverter application investigated in this report, factors such as the power rating and the voltage of the inverter DC-link have a significant impact on the design of the active capacitor. Based on these parameters the specifications of each component have to be determined by using the equations presented during the course of this chapter.

Another parameter which is dictated by the requirements of the final application is the expected lifetime. As mentioned in Chapter 1 and Subsection 2.3, this is a topic where the active capacitor could outperform the passive capacitor. This is due to the fact that the bulky electrolytic capacitors used in the conventional DC-link are generally slightly more prone to failure than other capacitor types [16].

Nevertheless, the expected lifetime is closely linked to the operating temperature as well. Therefore, this raises the question of maintaining a safe temperature for the components of the active capacitor circuit so that the operational lifetime is not massively reduced. This topic can be further investigated using thermal models and simulations. However, this does not directly link to the main topic of this report. Thus, when it comes to the thermal characteristics and to the expected lifetime, the choice of components will have to simply satisfy at least a minimum expected lifetime equal to that of the original passive capacitor. This is considered satisfactory to initially ascertain the viability of the active capacitor solution.

Moreover, the most important restriction is, of course, represented by the component height constrain, since it was the entire basis of the research conducted during this project, as was mentioned in Chapters 1 and 2. Because of that, every component of the active capacitor topology, from the passive components to the power switches and gate drivers, has to satisfy the maximum height criterion, otherwise the initial reason for utilizing the active capacitor instead of a simple passive capacitor is invalidated.

Although the height of the components is the primary concern regarding the physical size, the overall volume and weight are also design parameters. The area of components impacts the cost of the necessary PCB on which they are mounted, while their weight affects the transportation costs. Generally, these parameters should be as low as possible, without sacrificing the performance of the active capacitor.

On top of that, some components are also restricted by the role in which they are used inside of the circuit, therefore leading to a specific type of component being suitable for that particular role. This is the case with the $C_3$ capacitor. It can be observed from Figure 2.7 that the voltage $v_{C3}$ across the capacitor is a sinusoidal AC voltage. This restricts the choices of $C_3$ into only non-polarised capacitors, eliminating the possibility of using an electrolytic capacitor [16]. Therefore only film and ceramic capacitors were considered for $C_3$.

Additional requirements are related to the rest of the components, ancillary to the active capacitor circuit. One such components is the microcontroller unit MCU, which has to provide the necessary computational power to reliably control the auxiliary full-bridge converter, via the gate drivers, and enough memory to initially upload the required code. However, considering the relative simplicity

of the control scheme described in Section 3.1, the performance of the microcontroller is not heavily scrutinized during the selection process.

In the end, the final selection of components is also restricted by the available solutions, determined while consulting the necessary databases. After all of the remaining components satisfy the major restrictions mentioned above, the final solution in each case is determined based on all of the secondary criteria, including minimizing the overall cost of the topology.

Overall, the design process of the active capacitor is an iterative process, as the choice of some components depends on another selected component. An example of this is the capacitor $C_2$ in Equation 3.30, whose selection depends on the choice of $C_1$ and $V_{C2,dc}$. The design starts from a number of input parameters, mostly application dependent, as well as the overall objective of height minimization, and continues with the component choice for each step. If at any point the options available in the database cannot satisfy the requirements of the present component then the process is restarted.

## 3.4 Summary

This chapter has focused on presenting only the theoretical aspects of the design process. All of the equations were presented as general formulas, in which numerical values can be substituted and calculated.

Section 3.1 described the controller scheme used for modulating the power switches of the auxiliary circuit. The two control loops used in this scheme included a high-pass filter $G_{HPF}(s)$, a low pass filter $G_{LPF}(s)$ and a PI controller $G_{PI}(s)$.

Section 3.2 covered the entire components sizing necessary for the active capacitor. The role of each circuit element was described and general equations were determined which are applicable on any type of application, provided its specifications and ratings are known.

Once again, this chapter presented only the theoretical considerations of the components of the active capacitor, as well as a general design process to be followed. The rest of the design procedure, meaning the numerical design, is continued in Chapter 4.

# Chapter 4

# System Design

The following chapter focuses on the numerical design of the system, using the general theoretical considerations formulated in Chapter 3. Based on the resulting calculations, the choices of parameters and of components are presented.

## 4.1 System Parameters

The general restrictions obtained previously are independent on the type of power converter application the active capacitor is used in. However, they are instead functions of the ratings of the application in question. The ratings for the case of the solar PV embedded micro-inverter described in Chapters 1 and 2 are presented in Tables 4.1 and 4.2.

**PV Micro-Inverter:**
The single phase grid-connected PV embedded micro-inverter on which the design of this project is based has its parameters presented in Table 4.1.

**Table 4.1:** Parameters of the micro-inverter

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Power Rating | $S_{main}$ | 350 | W |
| Nominal DC-link voltage | $V_{AB}$ | 400 | V |
| Grid Voltage Magnitude | $\|v_g\|$ | 325 | V |
| Nominal Grid Frequency | $f_g$ | 50 | Hz |

**Initial passive solution:**
The characteristics of the initial passive DC-link capacitor are listen in Table 4.2.

**Table 4.2:** Parameters of the initial passive capacitor

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Capacitance | $C_{DC}$ | 150 | $\mu F$ |
| Voltage Rating | $V_{C_{DC}}$ | 450 | V |
| Ripple Current Rating | $I_{C_{DC}}$ | 1.1 | A @85° |
| Type | - | electrolytic | - |
| Rated Lifetime | - | 10000 | hours |
| Diameter | $d$ | 30 | mm |
| Height | $H$ | 30 | mm |

As stated in Section 2.2, most PV micro-inverters have a power rating between 250 W and 350 W [22]. Therefore, basing the design of the active capacitor on the 350 W micro-inverter in Table 4.1 should guarantee its applicability with lower rated micro-inverters too.

When it comes to the conventional passive capacitor solution, the primary parameter from Table 4.2 that is desired to be improved on by the active capacitor design is the 30 mm height. On top of the height reduction, an increase of the expected lifetime for all components would be an added bonus.

The power ratings of the embedded micro-inverter serve as the input parameters of the design process. According to the findings presented in [28], [29] and [15], an approximately 10 mm reduction in the width of newer generation of PV panels can be taken as a reference. Assuming that the same gap between the panel and the micro-inverter is kept (necessary in order to allow for enough air circulation and proper cooling), obtaining a maximum active capacitor height of 20 mm is formulated as the primary design objective, deemed as a satisfactory reduction from 30 mm. Therefore, every component of the active capacitor has to satisfy this maximum height criterion of 20 mm. Finally, another generally applicable objective for each component is to minimise the price.

## 4.2 Passive components sizing

This section presents the final solutions regarding the sizing and the choices of passive components for the active capacitor hardware design. As mentioned in Chapter 3, this process has an iterative nature, meaning that parts of the design or the entire design had to be redone when a point was reached in which at least one element could not satisfy the requirements of the design, either because a constraint was violated or because of the lack of availability of the necessary component in the database. In order to simplify the presentation of the process, these failed design iterations are not presented in this section, instead only presenting the final choices of components which satisfied all the criteria.

### 4.2.1 Capacitor $C_1$ sizing

The sizing of the $C_1$ capacitor is done based on Equation 3.18. More specifically, the primary design concern for $C_1$ is adjusting the balance between the relative power usage $\varepsilon_S$ and the capacitance $C_1$. The former deals with how much apparent power is acceptable for the auxiliary circuit to extract from the total apparent power, while the latter is closely linked to the size (more importantly, the height) of the capacitor used.

First, the $I_{C1}$ current has to be determined by rearranging Equation 3.14 into:

$$I_{C1} = \frac{S_{main}}{V_{AB}} \tag{4.1}$$

Both $S_{main}$ as 350 W and $V_{AB}$ as 400 V are known as input parameters from Table 4.1. The results is that $I_{C1}$ is equal to 0.875 A.

Second, since the grid frequency is now known as 50 Hz, the frequency of the ripple component across $C_1$ is known to be twice that at 100 Hz, based on the theoretical considerations covered in Section 3.2.1 regarding the relationship between these two frequencies.

As these parameters are thus known and are constants of the application, the ratio $\varepsilon_S$ between the apparent power in the auxiliary circuit and the total apparent power is used as the only input for Equation 3.18, which can be varied in a range of 4% to 20% in order to obtain and compare different values of the minimum $C_1$. Some examples of the results are presented in Figure 4.1.

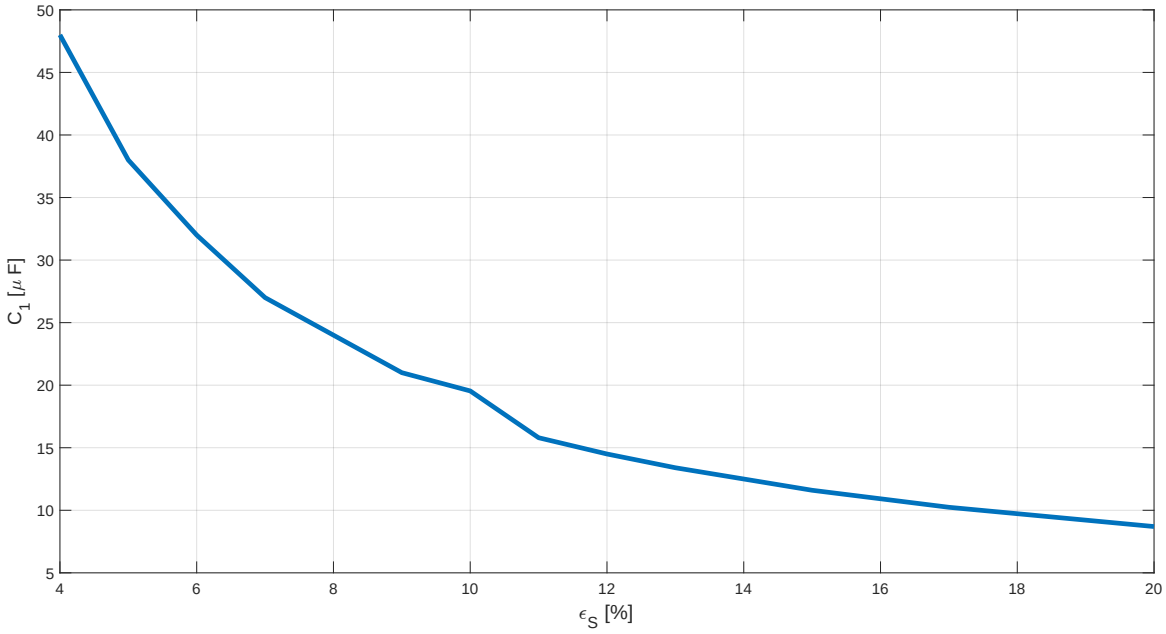


**Figure 4.1:** Example of values of $C_1$ obtained based on different input values of $\varepsilon_S$ using Equation 3.18

Based on the same design procedure, the final value for $C_1$ is selected as 16 $\mu$F, leading to a ratio $\varepsilon_S$ of 10.88%, as it was considered to be a sufficient reduction of $C_1$ while still maintaining a relatively low $S_{aux}$ consumption. Another indirect limiting factor of $S_{aux}$ and, consequently, of $\varepsilon_S$, besides balancing the overall efficiency of the system, was the power rating of the MOSFETs available in the database. Although it allows for the usage of lower values of $C_1$, increasing $S_{aux}$ and $\varepsilon_S$ to higher values also lead to a higher necessary output voltage $v_{C3}$ (and, therefore, to a higher DC-link input voltage $v_{C2}$), used to compensate for the decreased $C_1$. This acted as a limiting maximum point for $\varepsilon_S$ of approximately 20%, corresponding to an amplitude ripple $\Delta v_{C1}$ value of 160 V which had to be compensated, values at which the remaining MOSFETs which could fulfill these increased withstand voltage requirements were not considered viable solutions because of their increased price and size.

Knowing the desired value of $C_1$, the choice of capacitor has to satisfy the remaining requirements. Another important one is the voltage rating, resulting from Equation 3.7. Since $V_{AB}$ is known, the ripple voltage $\Delta v_{C1}$ has to be determined by rearranging Equation 3.15 into:

$$\Delta V_{C1} = 4\,\varepsilon_S\,V_{AB} \tag{4.2}$$

$V_{AB}$ is known as 400 V, while $\varepsilon_S$ was chosen as 10.88%, therefore resulting in the peak-to-peak ripple voltage across $C_1$ being equal to 152 V. Therefore, the voltage rating has to allow for the capacitor to withstand the sum of $V_{AB}$ with half of $\Delta V_{C1}$, meaning a rating of at least 476 V.

Other than these primary requirements, the withstand frequency range of $C_1$ has to cover the 100 Hz frequency of the ripple voltage. Since this is a relatively low frequency this should not prove to be a major problem. Other criteria are the operating temperature range and the expected lifetime, which were chosen to be at least equal to the initial passive capacitor from Table 4.2.

Based on these parameters, a choice of $C_1$ is made between various capacitors of the three types presented in Section 2.1. All the ceramic capacitor choices were eliminated immediately however, as capacitance values higher than 1 $\mu$F lead to large price increases for this type of capacitor [23]. A

comparison was made between the remaining film and electrolytic capacitor options regarding price and total volume, with the final choice being the film capacitor presented in Tables 4.3 and 4.4.

### 4.2.2 Capacitor $C_2$ sizing

In each design iteration the sizing of the $C_2$ capacitor can take place only after a $C_1$ choice has been determined. As described in Subsection 3.2.2, this is because Equation 3.30, which is the governing equation for sizing $C_2$, depends on the previous choice of $C_1$.

Another parameter from this equation than needs to be determined before a choice of $C_2$ can be made is $V_{C2,dc}$, the DC-component value of $v_{C2}$. As described by Equation 3.21, the $v_{C2}$ voltage, acting as in the input of the auxiliary circuit full-bridge converter, has to guarantee an output value high enough to counteract the ripple variation $\Delta v_{C1}$. Since the amplitude of $\Delta v_{C1}$ is equal to half of the peak-to-peak $\Delta V_{C1}$, meaning 76 V, $V_{C2,dc}$ was selected as 100 V in order to satisfy this requirement and guarantee a substantial additional margin.

Having selected $V_{C2,dc}$ and knowing the values for the other parameters from the previous design stage, with $I_{C1}$ as 0.875 A, $C_1$ as 16 $\mu$F and $\omega$ as $200\pi$, the minimum value for $C_2$ is calculated as 25 $\mu$F using Equation 3.30.

Regarding the type of capacitor, electrolytic and film capacitors are both suitable, while the relatively large capacitance value eliminates the possibility of using ceramic capacitors once again. The same considerations as those presented for $C_1$ regarding expected lifetime and temperature range were considered.

Finally, as the design calculations impose only a minimum $C_2$ value and not a also a maximum, simulations were undertaken to ascertain what $C_2$ value, out of the remaining database options once all the other constraints were applied, leads to the best performance, ultimately settling on 220 $\mu$F. It is also worth mentioning that the the final choice was an electrolytic capacitor, therefore the extra requirement to have a ripple current rating high enough to sustain $I_{C1}$ had to also be verified before confirming the final component choice, presented in Tables 4.3 and 4.4. The withstand rating of $C_2$ is 1.105 A, compared to $I_{C1}$ at 0.875 A, and was considered sufficient.

### 4.2.3 Filter LC sizing

The presence of the inductor $L_f$ and the capacitor $C_3$, connected to the output of the full-bridge inverter, serves two purposes: they form an LC harmonics filter, which makes the output voltage of the inverter more stable, and it allows for $v_{C3}$ to be applied across $C_3$, which is then used to counteract the ripple voltage $\Delta v_{C1}$.

The design of the LC filter starts from Equation 3.33. As previously described, a balanced value for $\Delta I_{L,max}$ has to be selected between 5% and 25% [25]. The choice was made for 11% as a middle value in that interval, which would offer a degree of switch losses mitigation, while also avoiding a substantial increase in the size of the inductor.

The switching frequency also had to be selected at this stage. Considering the initial general choice of using MOSFETs for the semiconductors, described in Subsection 3.3.1, relatively high values of $f_{sw}$ can be selected, provided they do not later lead to switching losses above the acceptable limit. In order to

guarantee a lowered harmonics presence in the output voltage, $f_{sw}$ was chosen as 100 kHz. This choice will later be validated based on the switching power losses and the expected junction temperature calculated in Section 4.3.

After selecting these two parameters and knowing the other values from the previous two design stages, substituting into Equation 3.33 leads to a choice of a 47 $\mu$H inductor. In order to also determine $C_3$ based on Equation 3.35 the desired cut-off frequency $f_{LC}$ has to be selected. A broad value for this parameter can be determined, based on [25], as the geometrical mean between the load frequency, in this case $f$ at 100 Hz, and the switching frequency of 100 kHz.

$$f_{LC} = \sqrt{f\, f_{sw}} \tag{4.3}$$

Based on Equation 4.3, $f_{LC}$ is selected as 3.2 kHz. Although this is a relatively simple selection method, it is considered sufficient for the objectives of this project. Substituting this frequency and the previously obtained $L_f$ into Equation 3.35 leads to a $C_3$ value of 15 $\mu$F.

Considering Equations 3.2 and 3.19, $C_3$ has to withstand the amplitude of the ripple voltage $\Delta v_{C1}$. For safety reasons, the withstand voltage was chosen as 100 V, which would be the applied voltage in case of unity modulation index.

When it comes to the type of capacitor in this case, as opposed to the previous two stages, the only suitable option considered is the film capacitor. This is because the expected $v_{C3}$ voltage applied across it will be an AC voltage, which would make the polarised electrolytic capacitor incompatible. As the capacitance values for ceramic capacitors are once again very limited, the only remaining non-polarised option is the film capacitor.

Other than that, all the same criteria regarding height, volume, price, expected lifetime, temperature range and frequency range as the ones used for $C_1$ and $C_2$ are applied for $C_3$, with the final choice being presented in Tables 4.3 and 4.4.

### 4.2.4 Summary

As stated at the beginning of this section, the values presented so far are the values of the final components selection. Multiple design iterations were implemented, out of which some were abandonment because all the remaining database choices for a component failed to satisfy the criteria, while others were successfully completed, leading to full design, but were deemed inferior to the solution presented here when it comes to price or total volume.

Therefore, as an overview, the parameters of the chosen design are presented in Table 4.3, while the components manufacturer's numbers are given in Table 4.4, as well as in the bill of materials in Annex B.

**Table 4.3:** Parameters of passive components selected for active capacitor design

| Component | Value | Rating | Height | Size | Max. temp. | Lifetime |
|---|---|---|---|---|---|---|
| $C_1$ | 16 $\mu$F | 500 V | 19.2 mm | 41.5 x 24 mm | 105° | 100000 h |
| $C_2$ | 220 $\mu$F | 160 V | 20 mm | 18 mm diameter | 105° | 10000 h |
| $L_f$ | 47 $\mu$H | 2.7 A | 7 mm | 13 mm diameter | 125° | 10000 h |
| $C_3$ | 15 $\mu$F | 100 V | 11 mm | 6.3 diameter | 105° | 144500 h |

**Table 4.4:** Manufacturer's numbers of passive components selected for active capacitor design

| Component | Manufacturer's number |
|---|---|
| $C_1$ | C4AQLLU4800A12K |
| $C_2$ | UCY2C221MHD6TN |
| $L_f$ | SRR1205-250ML |
| $C_3$ | 685MMR100K |

## 4.3 Active components selection

### 4.3.1 Power MOSFETs selection

Based on the reasons described in Subsection 3.3.1, MOSFETs were selected as the type of power semiconductors used for the active capacitor applications, before the proper design phase started. The following subsection focuses on the selection process of the actual MOSFET product used.

The first restriction considered is the withstand voltage rating. If the sizing procedure described previously is to be followed, then the MOSFETs should be able to withstand at least a voltage of twice the rms value of $v_{C3}$. If its amplitude is assumed to be equal to $v_{C2}$ at 100 V, then that would result in a minimum withstand voltage for the MOSFETs of 142 V.

Based on the voltage rating and the rest of the usual criteria regarding the height, price, volume and frequency range, an initial choice is selected, which then has to be validated based on the expected operating temperature and power losses.

The conduction and switching losses are determined using Equations 3.37 and 3.38, respectively. Starting with the conduction losses $P_{CD}$, the resistance $r_{DS}$ has to be determined based on the output characteristics provided in the product datasheet [42]. It has to be mentioned that this characteristic was determined at the test junction temperature of 25°C and is dependent of the applied gate voltage $V_{GS}$, which was selected as 12 V and is described more in detail in the next subsection.

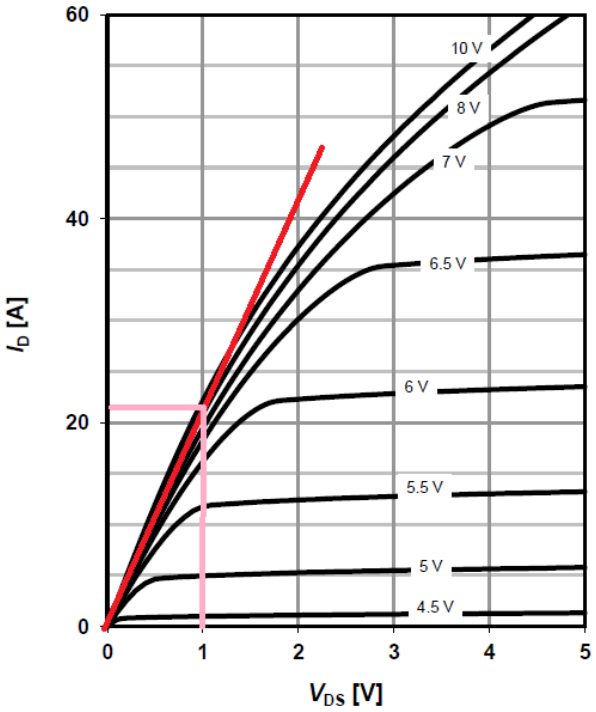


**Figure 4.2:** Output characteristic used for determining calculating $r_{DS}$ [42]

Based on Figure 4.2, calculating the slope between a 1 V drain-source voltage and 22 A drain current results in an $r_{DS}$ of 0.045 Ω. Next, the value of $I_{D,rms}$ was determined from simulations at 4.96 A, resulting in an expected conduction losses of 1.1 W, based on Equation 3.37.

Next, before determining the switching losses, the value of the $Q_{GS}$ and $Q_{GD}$ charges are, again, found in the datasheet [42] as 3.8 nC and 1.5 nC, respectively. The gate current $I_G$ is a parameter covered by the gate driver design and is described in the next subsection. Nevertheless, its value was determined as 1.2 A. Knowing that $V_{DS,rms}$ is equal to the rms value of the applied $v_{C2}$ of 100 V, the result of Equation 3.38 becomes 15.45 mW switching losses. Therefore, the total switch losses $P_{loss}$ stand at approximately 1.10015 W.

Finally, in order to validate the choice of MOSFETs, the expected junction temperature is calculated based on Equation 3.41. Once again, the sum of the junction-case and case-ambient thermal resistances, the junction-ambient thermal resistance, was taken from the datasheet [42] as 62 K/W. Even considering a relatively high ambient temperature $T_a$ of 40°C, this results in a $T_j$ of 108.21°C, which is substantially bellow the datasheet withstand temperature of 175°C by a safety margin of approximately 37%. This result thus validates the choice of MOSFETs, confirms that $f_{sw}$ does not lead to exceedingly high switching losses and can be kept as 100 kHz, all without the use of an additional heat-sink.

### 4.3.2 Gate driver selection

The last major component selected is the gate driver. In order to choose a suitable gate driver the necessary characteristics have to be calculated.

The desired gate voltage $V_{GS}$ that drives the MOSFET is chosen between from a range of 4 V, the

threshold voltage, to 20 V, the maximum value. The performance of the MOSFET under different values in this range is assessed based on the output and transfer characteristics provided in the datasheet [42], resulting in the value of 12 V. Overall, this value guarantees a high enough gate voltage, which lowers the duration of the switching instances and results in decreased switching losses, while also providing a safety margin compared to the 20 V, therefore avoiding the risk of voltage surges damaging the device.

As described in Subsection 3.3.2, the gate resistor can be approximated based on the datasheet test value, which acts as the minimum recommended choice, while double the value acts as the maximum. This results in a range of 6.4 Ω to 12.8 Ω. The final value was selected as 7.9 Ω, small enough to minimize the switching times, but high enough to limit any potential voltage spikes, especially when considering the added 2.1 Ω internal gate resistance of the MOSFET. Finally, knowing both $V_{GS}$ and $R_G$, the gate current $I_G$ was calculated as 1.2 A using Equation 3.44.

The gate charge $Q_{gate}$ is determined based on the gate charge characteristic of the chosen MOSFET, presented in Figure 4.3 [42]. The resulting $Q_{gate}$ at 12 V $V_{GS}$ is 10 nC.

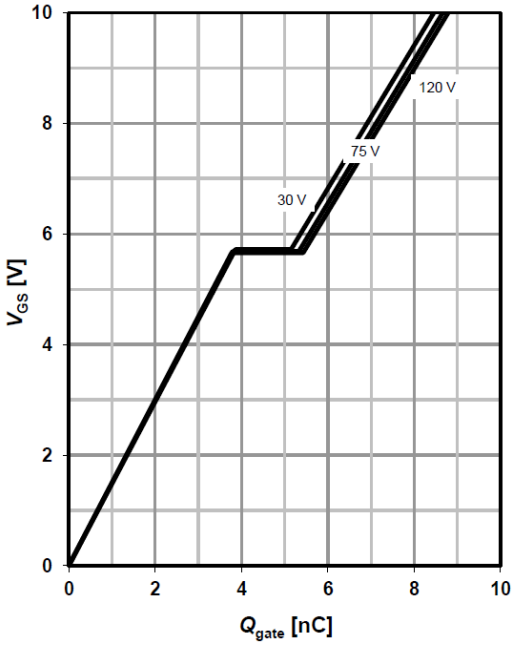


**Figure 4.3:** Charge characteristic used for determining calculating $Q_{gate}$ [42]

Finally, the necessary power output of the driver is determined based on Equation 3.48, where $V_{GS(on)}$ is the entire $V_{GS}$ of 12 V, while $V_{GS(off)}$ is simply kept as 0 V. The resulting $P_G$ is 12 mW. The final choice of gate driver is presented in Annex B.

## 4.4 Controller scheme tuning

The controller loops presented in the larger control scheme in Figure 3.2 have to be tuned to accommodate for the design of the active capacitor. This control scheme consists of the high-pass filter, the low-pass filter and a PI controller.

### 4.4.1 High-pass filter HPF

Considering the transfer function given in Equation 3.1, the only choice of parameter that has to be made is the cut-off frequency $f_c$. Based on this value the HPF either blocks signals with frequencies lower than $f_c$ or allows them to pass if they are higher than $f_c$.

The signal that is desired to be allowed to pass is the $\Delta v_{C1}$ ripple of 100 Hz, while blocking the DC-signal $V_{AB}$. Theoretically, a value of $f_c$ slightly lower than 100 Hz should be ideal. However, in practice, low frequency disturbances bellow 100 Hz can occur and will negatively affect the performance of the active capacitor [17]. If the cut-off frequency is too high, then these low frequency signals will just be blocked by the HPF and they will continue to negatively impact the operation of the active capacitor. If $f_c$ is decreased however, then these low frequency disturbances will be allowed to pass and will be fed into the $v_{C1}$ controller loop and will, therefore, be canceled out by the output voltage $v_{C3}$. In order to prove this point, a simulation of the active capacitor, using the component values determined in Section 4.3, is configured using an $f_c$ value of 60 Hz and of 20 Hz, respectively. The Fourier spectrum for each of the two cases of the output voltage $v_{C3}$ are presented in Figures 4.4 and 4.5.

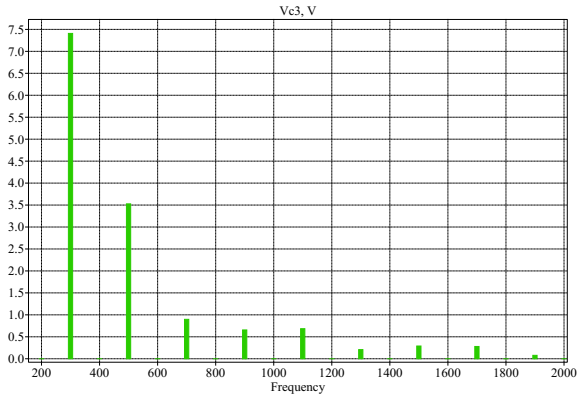


**Figure 4.4:** Fourier spectrum of $v_{C3}$ when using a 60 Hz $f_c$ for the HPF

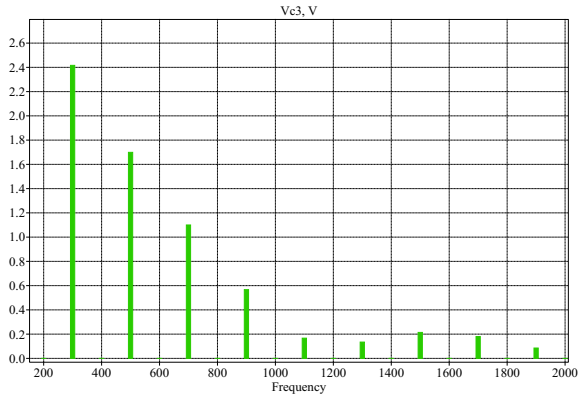


**Figure 4.5:** Fourier spectrum of $v_{C3}$ when using a 20 Hz $f_c$ for the HPF

The 60 Hz cut-off frequency leads to a third harmonic at 300 Hz of almost 7.5 V, while the 20 Hz $f_c$ results in one of only 2.4 V. This behaviour can also be observed when considered the higher order harmonics, as the 5th, 7th, 9th, 11th, 13th, 15th and 17th reach values as high as 3.5 V in the 60 Hz $f_c$ case, while all of them are below 1.8 V in the 20 Hz case. These high frequency harmonics are even more damaging that the third order harmonics, as they could exceed the operating frequency ranges of the selected components, resulting in the decrease of their operating lifetimes. Because of that, the 20 Hz cut-off frequency is considered to lead to a better performance of the active capacitor and is the value of choice for the rest of the project.

### 4.4.2 Low-pass filter LPF

The opposite case can be made for the low-pass filter used in second loop of the control scheme. Its cut-off frequency should, ideally, be as low as possible, since the input $v_{C2}$ is approximated as a DC-signal, while the extra higher frequency oscillations it contains need to be filtered out of the controller

input. However, the same low frequency disturbances present in $v_{C1}$ also appear in $v_{C2}$, which makes slightly increasing the cut-off frequency of the LPF necessary so that the PI controller can mitigate them. In order to simplify the design of the control scheme, the same $f_c$ is used as the cut-off frequency of both the HPF and the LPF, since the same low frequency disturbances are affecting both $v_{C1}$ and $v_{C2}$.

### 4.4.3 PI controller

As described in Section 3.1, the PI controller can be tuned similarly to the conventional DC-link voltage controller presented in Figure 3.3. Since $C_2$ is known as 220 $\mu$F after the components sizing stage, then the plant based on which the PI controller is designed is now also known [33].

The choice of the proportional $K_P$ and integral $K_I$ gains was done by using a simple root locus method (Figure 4.6). The value of $K_P$ was varied until the system became stable, after which $K_I$ was used to eliminate the remaining steady state error. By comparing the closed-loop step response (Figure 4.7) and the bode diagrams (Figure 4.8) the final values of $K_P$ and $K_I$ were determined as 0.004 and 0.02, respectively, since these resulted in a settling time of only 2.5 ms, no overshoot and a phase margin of 90°, which were considered satisfactory.

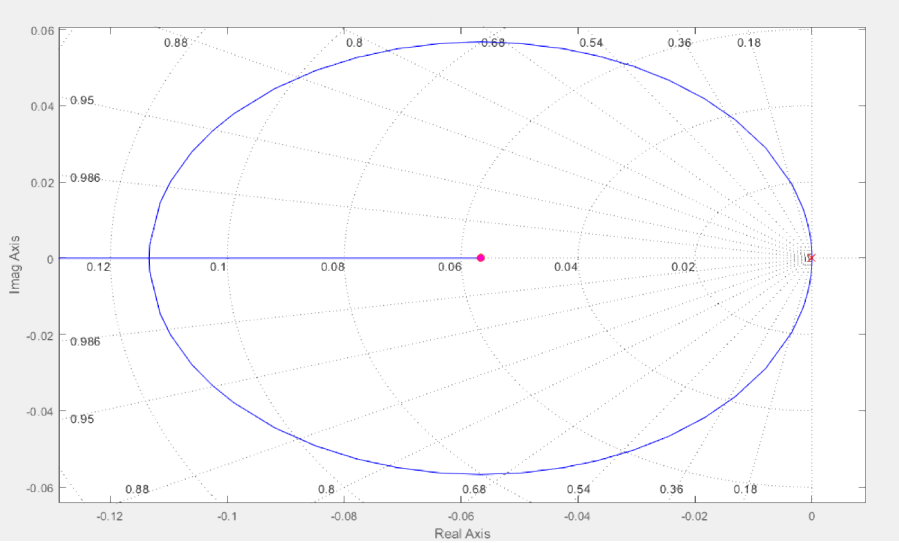


**Figure 4.6:** DC-link $v_{C2}$ voltage controller root locus

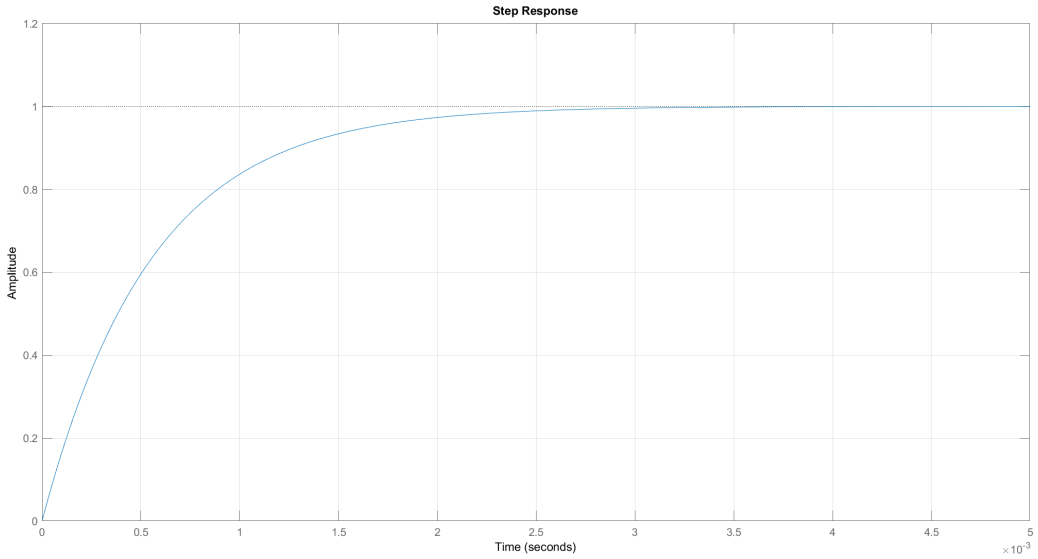


**Figure 4.7:** DC-link $v_{C2}$ voltage controller closed-loop step response

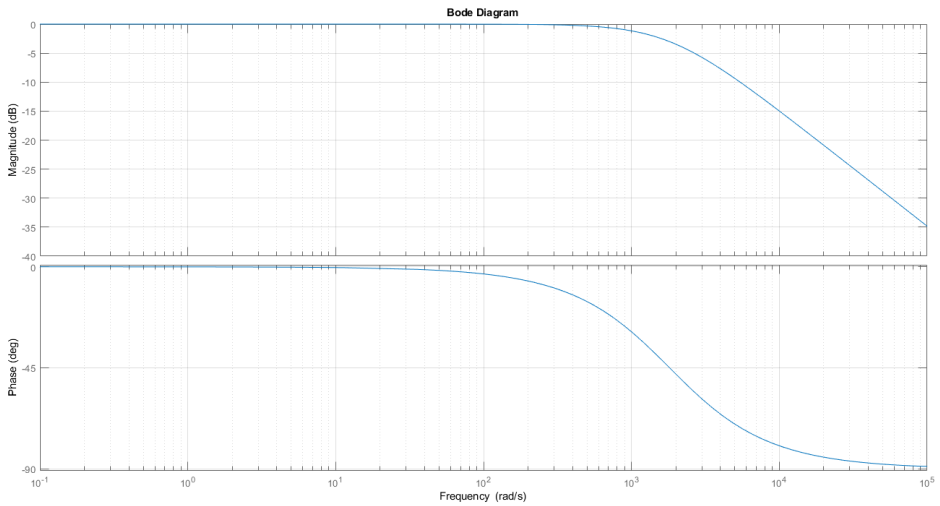


**Figure 4.8:** DC-link $v_{C2}$ voltage controller bode diagrams

### 4.4.4 Summary

Finally, all the gains of the controller scheme are presented in Table 4.5.

**Table 4.5:** Parameters of controller scheme selected for active capacitor design

| Parameter | Value |
|---|---|
| $f_c$ | 20 Hz |
| $K_P$ | 0.004 |
| $K_I$ | 0.02 |

With the controller tuned and with the components selected the testing and implementation of the active capacitor prototype can be realised and is described in the next chapter.

Chapter 5

# Implementation and results

The following chapter focuses on presenting the simulation and experimental results obtained with the micro-inverter active capacitor prototype described so far.

## 5.1 Software simulations

This section describes the implementation of the concept in a number of simulations realised in the PLECS platform. These will range from stand-alone tests of the active capacitor, as well as tests involving replacing the passive DC-link of a pre-existing micro-inverter model with the active capacitor circuit and its control scheme.

### 5.1.1 Standalone active capacitor simulation

In order to prove the functionality of the design described in Chapter 4, a stand-alone circuit simulation is performed based on the architecture in Figure 2.6. The active capacitor is then supplied with a constant DC voltage at its two terminals, used to represent the voltage normally supplied from the DC side of the two-stage micro-inverter, while a current source is used to apply the 100 Hz ripple coming from the AC side. The voltage $V_{AB}$ measured at the two terminals of the active capacitor, meaning the voltage which would be seen by the inverter, is presented in Figure 5.1, along with $v_{C1}$, $v_{C2}$ and $v_{C3}$.

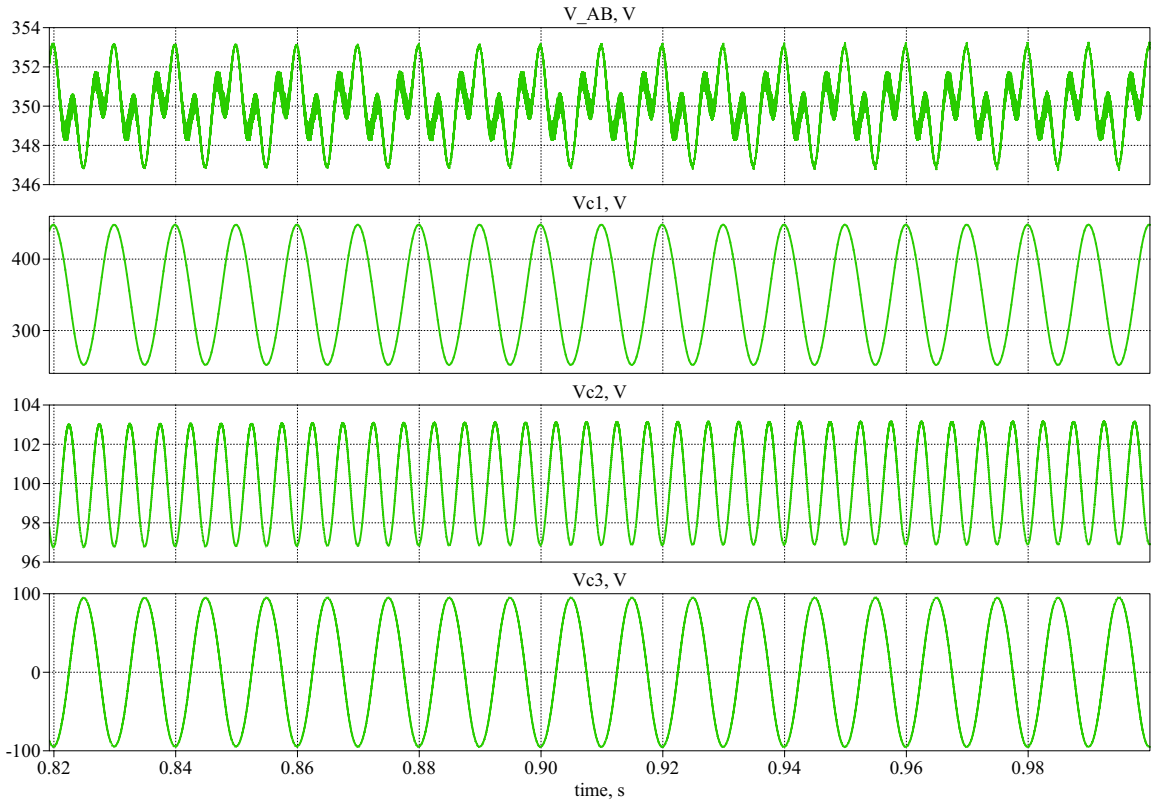


**Figure 5.1:** The $V_{AB}$, $v_{C1}$, $v_{C2}$ and $v_{C3}$ voltages resulted from the stand-alone simulation

As expected, a significant ripple component $\Delta v_{C1}$ of around 100 V can be observed in $v_{C1}$, on top of a constant 350 V average. If the undersized $C_1$ capacitor would have been used directly, without implementing the corresponding auxiliary circuit, then the terminal voltage $V_{AB}$ would have been equal to this highly oscillatory $v_{C1}$. Instead, the auxiliary circuit full-bridge inverter is successfully controlled to generate a complementary $v_{C3}$ that, almost entirely, negates $\Delta v_{C1}$. The result can be observed in $V_{AB}$, where the ripple component is mostly eliminated and the voltage oscillates by only 3 V, close to being an entirely constant value. It is worth mentioning, however, that the initial applied DC voltage is 400 V, but because no external DC voltage control is implemented, like it would normally be in a full PV inverter control scheme, the resulting voltage is only approximately 350 V, due to the voltage drops across the extra impedances present in the circuit.

Additionally, the control loop tasked with maintaining $v_{C2}$ at 100 V and compensating for its discharge is also running successfully, although a small 2 V variation around the 100 V average can still be observed. This is attributed to the presence in the circuit of the remaining ripple, which was not eliminated and was also seen in the waveform of $V_{AB}$.

These simulation results were captured once the output had become fully stable. Instead of that, Figure 5.2 presents the full behaviour of the active capacitor since the start of the simulation until its stabilisation.

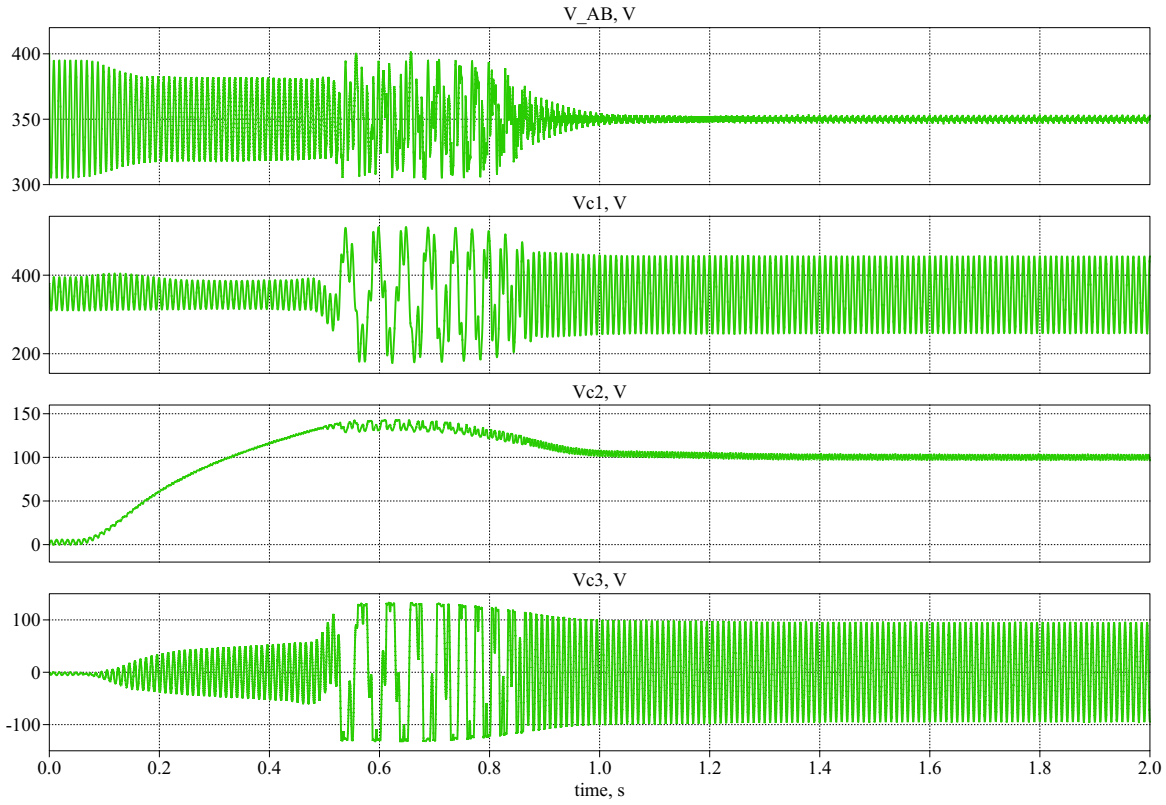


**Figure 5.2:** The $V_{AB}$, $v_{C1}$, $v_{C2}$ and $v_{C3}$ voltages resulted from the stand-alone simulation, including the transitory period at the beginning of operation

It can be observed that a transitory period is necessary until the operation of the active capacitor can become fully stable at around 1 s. This is attributed to the behaviour of $C_2$, which requires the 1 s period to become totally charged and stable at a 100 V average. Until then the ripple component of $V_{AB}$ is considerably larger than during stable operation, because the auxiliary circuit simply does not have a supply high enough to generate an appropriately big $v_{C3}$. This small transitory period that occurs when the active capacitor is turned-ON is worth considering and planning for accordingly in practical implementations of the concept, possibly by connecting the AC side of the two-stage converter only after $C_2$ is fully charged.

Finally, the stand-alone performance of the active capacitor is compared in Figures 5.3 and 5.4 with the behaviour of the initial passive solution presented in Table 4.2, under the same test conditions.

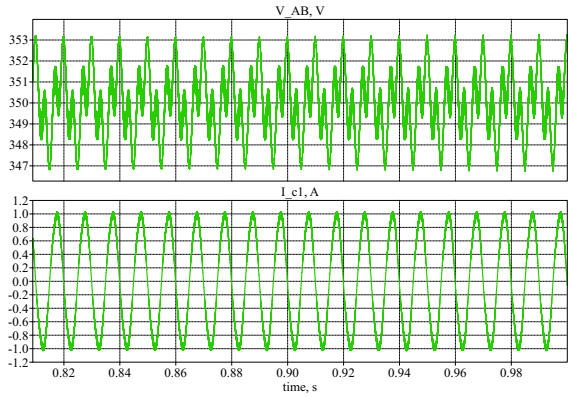


**Figure 5.3:** Voltage across AB terminals of DC-link and current waveforms when using the designed active capacitor

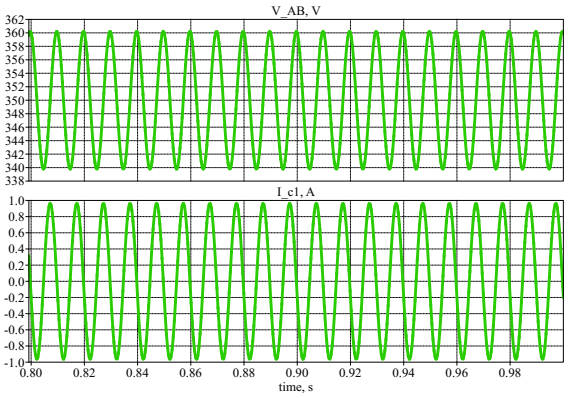


**Figure 5.4:** Voltage across AB terminals of DC-link and current waveforms when using the initial passive capacitor

It can be observed that the active capacitor manages to provide a ripple attenuation that is even better than the initial solution, as the resulting ripple is reduced from the initial 10 V amplitude to only 3 V when using the active capacitor. The explanation that is attributed to this superior performance is that the control scheme is outperforming the innate ripple attenuation capabilities of the initial passive capacitor, especially considering the high switching frequency used, of 100 kHz, which allows for an increased level of control of $v_{C3}$, with a lower THD, by the MOSFETs.

### 5.1.2 PV micro-inverter simulation using active capacitor

Once the active capacitor was tested in the standalone simulation it can be used in a PV inverter application like the one in Figure 3.1. This is done by using an example demo model provided by PLECS at [45] of the two-stage PV inverter and replacing the default passive DC-link with the previously designed and tested active capacitor and its associated control scheme. The parameters of this initial model are modified to reflect the ratings of the PV micro-inverter for which the active capacitor was designed in Table 4.1.

The concept of the two-terminal active capacitor is that of a plug-and-play device, which can be connected to an already existing micro-inverter as its DC-link. Therefore, this approach of using an existing inverter model was considered highly suitable. The stable operation of this newly created circuit is tested and presented in Figure 5.5.

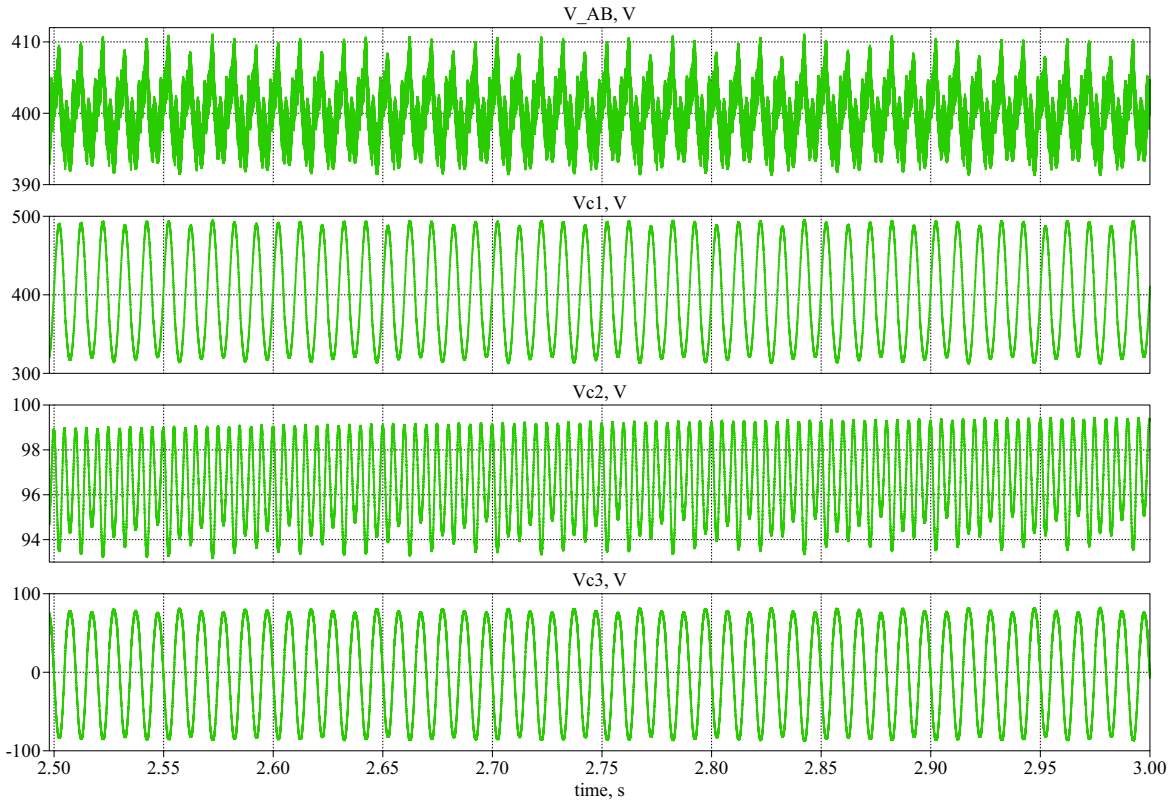


**Figure 5.5:** The $V_{AB}$, $v_{C1}$, $v_{C2}$ and $v_{C3}$ voltages resulted from the full micro-inverter simulation

Although the ripple component of $V_{AB}$ does increase to an amplitude of 10 V, the active capacitor still manages to limit these oscillations and to create a stable DC-link voltage. The difference between this test and the standalone simulation is that this model better reflects a practical application, as it includes the effects the rest of the two-stage converter has on the operation of the active capacitor. For example, the operation of the added switches in the boost converter and in the inverter was expected to have an impact, as they would add extra switching harmonics which could have destabilized the operation of the active capacitor. Fortunately, it can be seen that the design of the active DC-link is robust enough to sustain these added harmonics, with a slight increase in the overall ripple of $V_{AB}$.

Another interaction with the larger converter comes in the form of the DC-link voltage control, part of the DC-AC converter control scheme. By comparison with Figure 5.1 it can be seen that this external control loop manages to compensate for the voltage drops inside of the active capacitor circuit and maintains an average value of 400 V across its terminals. Once again, this is another aspect in which the active capacitor manages to successfully integrate in the existing hardware and control scheme.

Additionally, this represents a testing environment that is closer to the specifications in Table 4.1, ratings based on which the active capacitor was designed, since the DC-link voltage is now maintained at the nominal average of 400 V, as opposed to the 350 V in the stand-alone simulation. Accordingly, the resulting ripple component of $v_{C1}$ is closer to the expected 76 V from the design calculations.

Figure 5.5 was taken during the steady state operation of this converter. Next, in order to further prove the stability of the active capacitor, the load of the two-stage converter is varied. This is done

by modifying the solar radiance level of the input PV cells, lowering the total power generated by the system. The results are compared with the behaviour of the initial passive capacitor presented in Table 4.2, under the same test conditions.

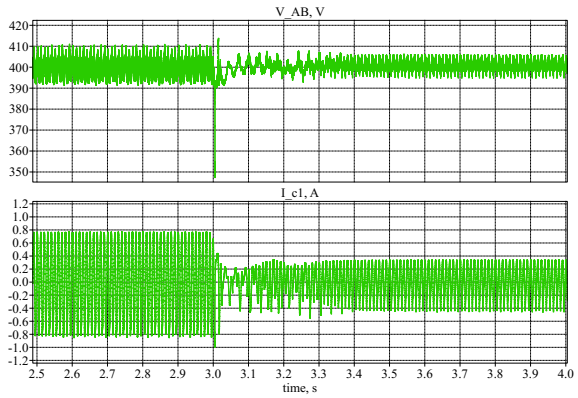


**Figure 5.6:** Voltage across AB terminals of DC-link and current waveforms of active capacitor when PV power output is lowered from 350 W to 150 W

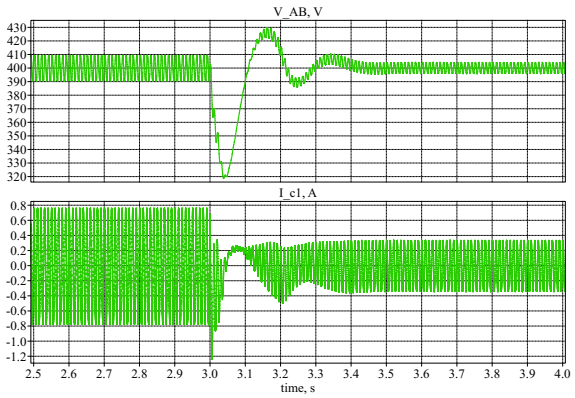


**Figure 5.7:** Voltage across AB terminals of DC-link and current waveforms of passive capacitor when PV power output is lowered from 350 W to 150 W

Even though the design of the active capacitor in Chapter 4 was created for the 350 W nominal operating power, the system still manages to recover after the shift in the available power which occurs at 3 s in Figure 5.6. Following a transitory period the system becomes stable once again at 3.4 s, this time with a reduced ripple of 5 V peak. Although this period is quite large, the drop in available power was also significant, causing an initial instability which had to be compensated in time. This would not be the case in a real application, where the available power would decrease more gradually.

When comparing with Figure 5.7 it can be observed that the two capacitor solutions behave almost identical in the period before the load change, with the only difference being the presence of small voltage overshoots in the $V_{AB}$ of the active capacitors. These are attributed to high frequency oscillations which are caused by the presence of additional MOSFETs in the auxiliary circuit of the active capacitor.

After the load change occurs are 3 s, the active capacitor manages to reach a stable $V_{AB}$ faster by approximately 0.1 s than the passive capacitor. This is credited to the presence of the active capacitor control scheme, which modulates the auxiliary circuit MOSFETs at 100 kHz, therefore managing to eliminate the disturbance caused by the load change quicker than the passive capacitor does, which has to rely on the external DC-voltage controller operating at only 20 kHz. On the other hand, once both cases of $V_{AB}$ have stabilised, the resulting ripple voltage is sligtly higher for the active capacitor at 5 V peak than it is for the passive capacitor at 3 V, which is attributed to the design described in Chapter 4 being based on the 350 W operating power, not on 150 W. Nevertheless, this is a very small difference which does not present a significant issue for the performance of the active capacitor. Lastly, the resulting $i_{C1}$ currents for both cases are within the expected values based on the operating power levels of 350 W and 150 W, respectively.

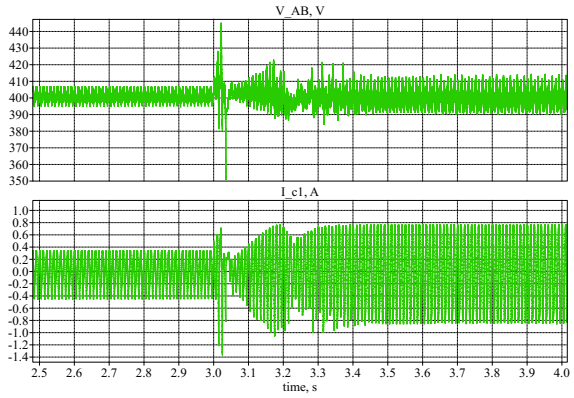


**Figure 5.8:** Voltage across AB terminals of DC-link and current waveforms of active capacitor when PV power output is increased from 150 W to 350 W

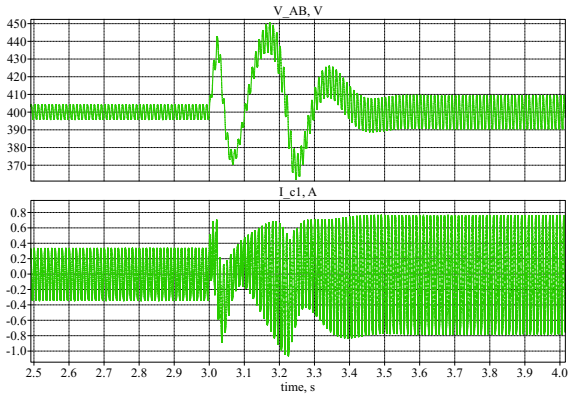


**Figure 5.9:** Voltage across AB terminals of DC-link and current waveforms of passive capacitor when PV power output is increased from 150 W to 350 W

Secondly, the opposite case is tested, in which a power of 150 W is increased back to 350 W, and the results are presented in Figure 5.8. Similarly to the previous case, the shift in available power occurs at 3 s, after which the system manages to balance the deviation and recover to a stable $V_{AB}$ with the initial ripple component of 10 V peak.

Most of the observations made previously in relation to the passive capacitor can be observed again in Figure 5.9, only this time reversed. Once again, the system recovers faster when using the active capacitor, but presents some small added ripple overshoots both before and after the load change, due to the design process or to the presence of additional MOSFETs. Overall, the active capacitor successfully emulates the behaviour of the passive capacitor under the same test conditions when faced with both a load decrease and a load increase.

With the suitability of the chosen active capacitor design now proven in a PV micro-inverter application, the following section will focus on the hardware implementation of the prototype. This will include both the necessary setup for implementation to be possible, as well as the final results.

## 5.2 Experimental validation

This section describes the preliminary work needed in order to build the experimental setup and presents the results obtained after implementing the hardware design.

### 5.2.1 Experimental setup

The primary element needed for building the hardware setup on which the design will be tested is the printed circuit board (PCB), which will contain all the active capacitor components, as well as any additional elements that might be necessary. The PCB was designed using the Altium Designer software.

The final PCB layout and 3D-model are provided in Figures 5.10 and 5.11, respectively. These contain the primary components of the active capacitor, from the passive elements to the power switches circuit to the self-supply structure, as well as additional space for adding extra capacitors in parallel with

each of $C_1$, $C_2$ and $C_3$, either for filtering unwanted noise or to allow for the possibility of increasing each equivalent capacitance, if this would be necessary during the testing phase.

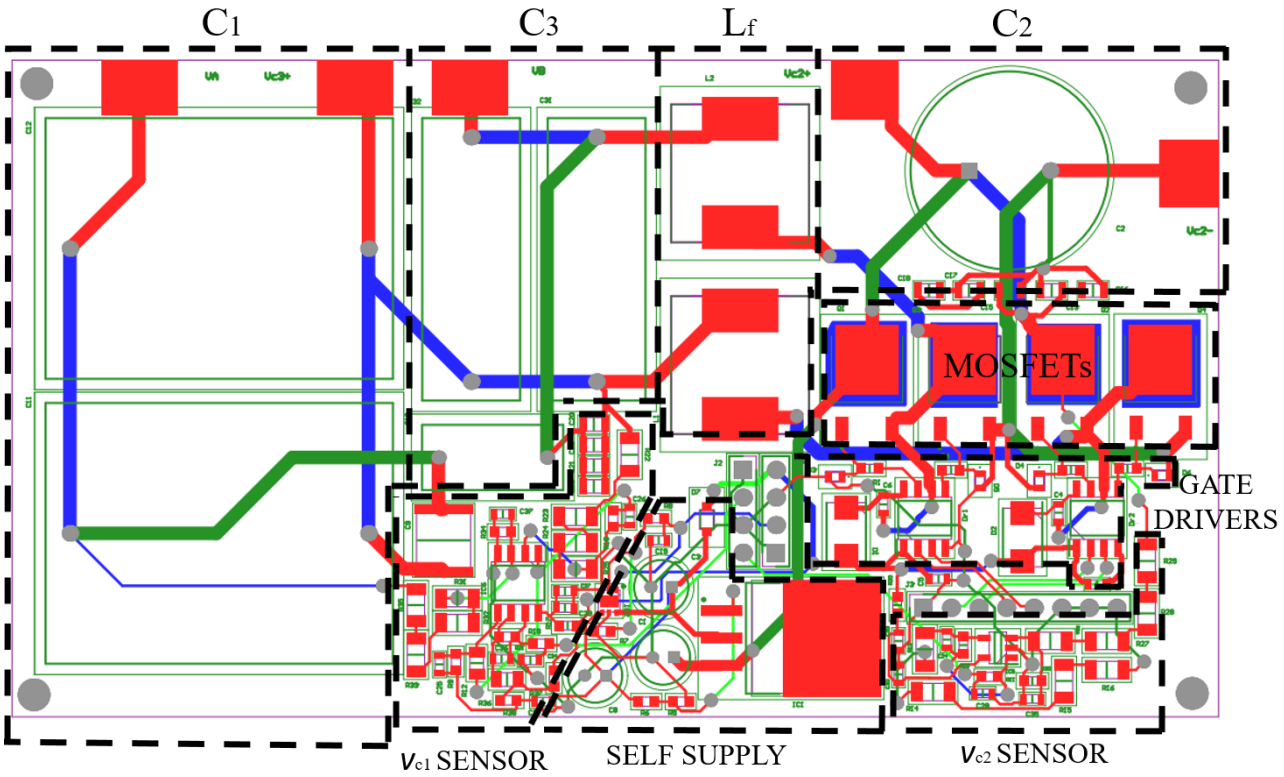


**Figure 5.10:** The layout of the active capacitor PCB

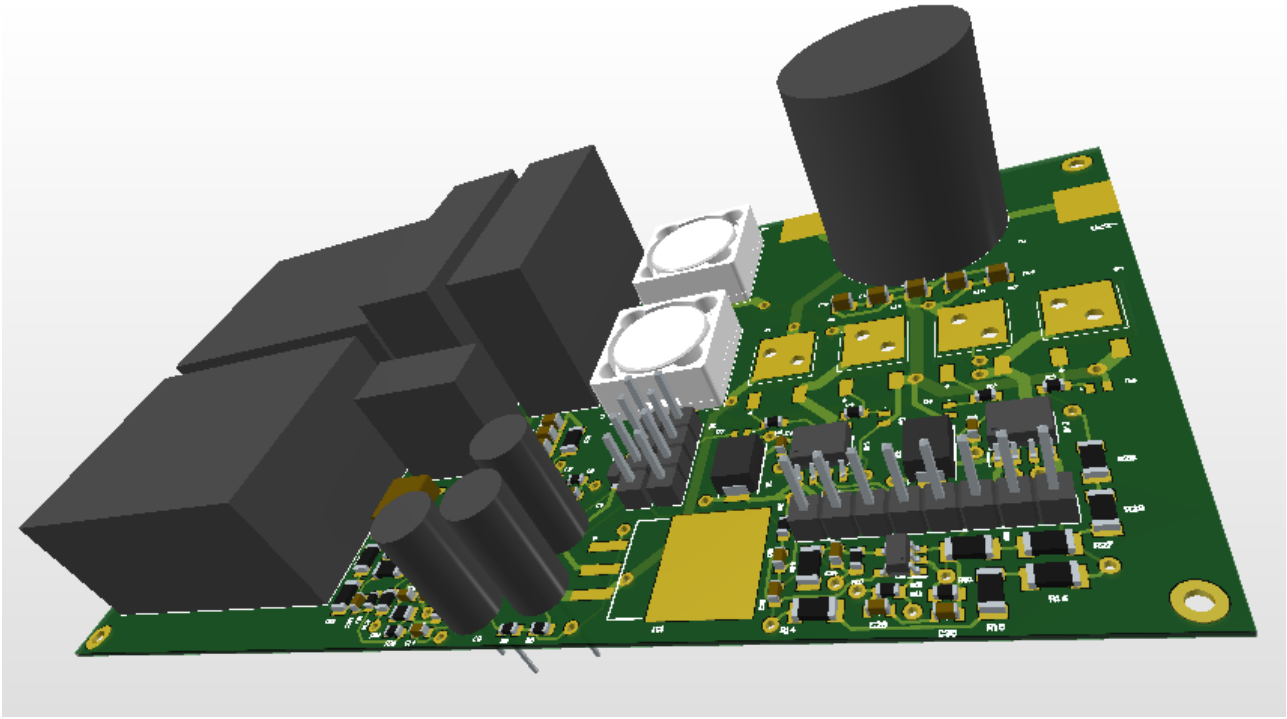

**Figure 5.11:** The 3D-model of the active capacitor PCB

Also included are the differential amplifiers used as sensors, which measure $v_{C1}$ and $v_{C2}$, so that they

can be used as feedback for the controller scheme. The design of these sensors is covered in Annex A. Once again, it can be observed from Figure 5.11 that the highest component of this design is the $C_2$ capacitor, at 20 mm, with everything else being bellow, resulting in a final design that accomplishes the goal of limiting every component to a maximum of 20 mm. Overall, all the components which are part of the final PCB are provided in the bill of materials in Annex B.

The measured signals are sent to an external controller, in the form of a TMS320F28335 DSP, which was programmed using the software Code Composer Studio, in the C programming language. In a final design of this active capacitor prototype the controller chip would have to be included together with the rest of the circuit, so as to maintain the two terminal structure. However, in order to simplify the testing process, this approach with an external controller was taken. Finally, the experimental setup, made out of the PCB, the external DSP, a signal generator, a voltage source and an oscilloscope, is depicted in Figure 5.12.

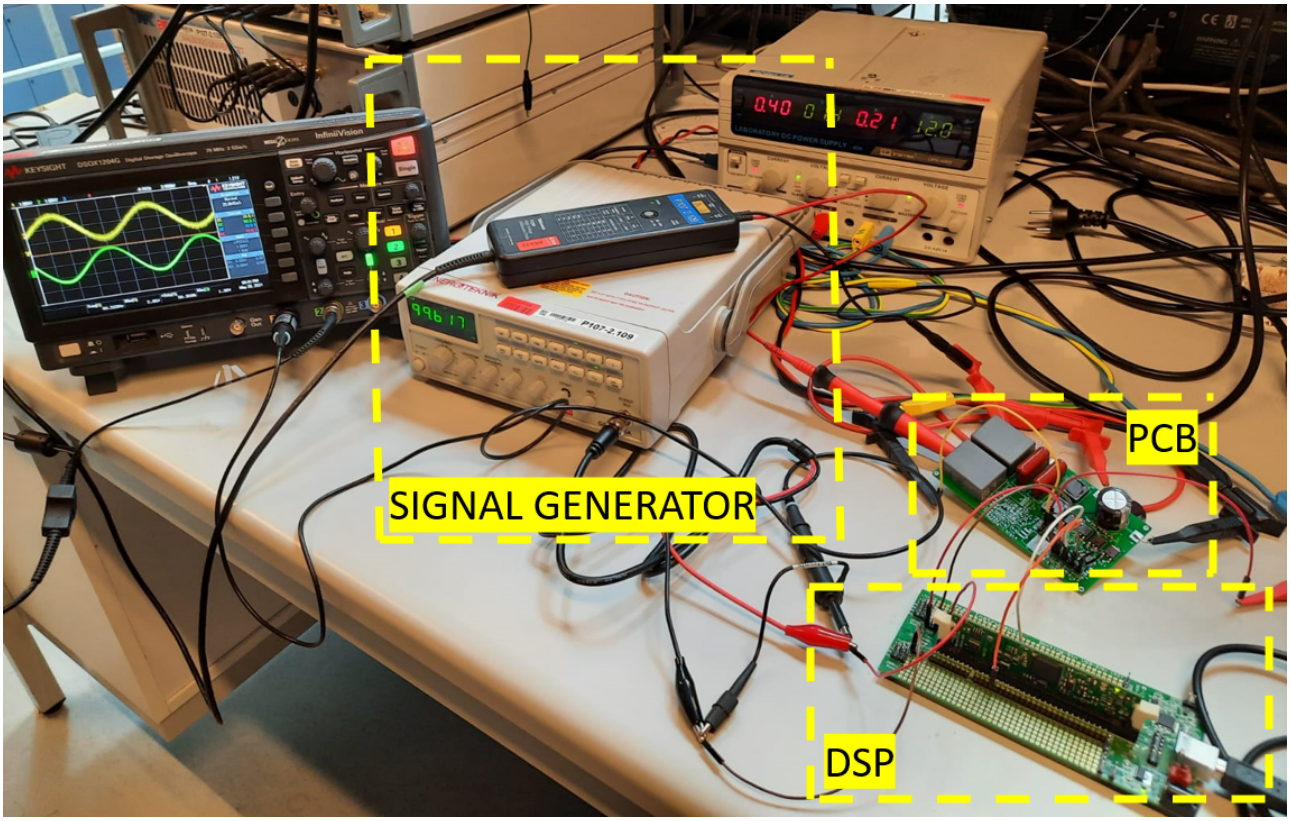


**Figure 5.12:** Experimental laboratory setup used for auxiliary circuit and controller testing

The signal generator is used to output a sinusoidal waveform with a minimum of 0.522 V and a maximum of 2.543 V, with a DC-offset of 1.5325 V. This particular signal would correspond to a scaled down $v_{C1}$ voltage variation of 300 V to 500 V, with an offset of 400 V DC. These values were obtained based on the sensors calculated in Annex A and used in the design of the PCB.

If the PCB layout in Figure 5.10 is considered, this low voltage signal is meant to represent the output of the $v_{C1}$ sensor, if the active capacitor terminals AB would be clamped to an external DC voltage of 400 V, under the nominal load of 350 W. By using this feedback signal generated externally, which corresponds to what the measured $v_{C1}$ would have been in that situation, the performance of the control scheme and of the auxiliary circuit can be tested directly, eliminating any interference that the sensor circuit might have had. Since in this testing scheme the terminals AB are not supplied, the $C_2$

capacitor cannot be charged externally. Therefore, a voltage source has to be connected in parallel to $C_2$, so that it can function as the DC-link of the auxiliary circuit.

Based on the design calculations presented in Chapter 4, the ripple which would result from using a 16 $\mu$F $C_1$ capacitor would be approximately 76 V. For this test, as a worse case scenario, a ripple component of 100 V peak is considered, which would be the maximum value that a $V_{C2,dc}$ supply of 100 V would be able to mitigate.

### 5.2.2 Experimental implementation

With the test setup in Figure 5.12 fully implemented, the test previously described can be conducted. The generated signal is fed into the DSP controller, which utilises the control scheme in Figure 3.2. Therefore, the high-pass filter works to eliminate the DC-component of 1.5325 V, corresponding to the 400 V in a practical scenario. The resulting PWM signals are sent to the gate driver, which generates the gate-source voltages presented in Figure 5.13 for the top switch of the first leg and in Figure 5.14 for the top switch of the second leg. A software low-pass filter is used to represent the 100 Hz component of this resulting voltage, for better visualization.

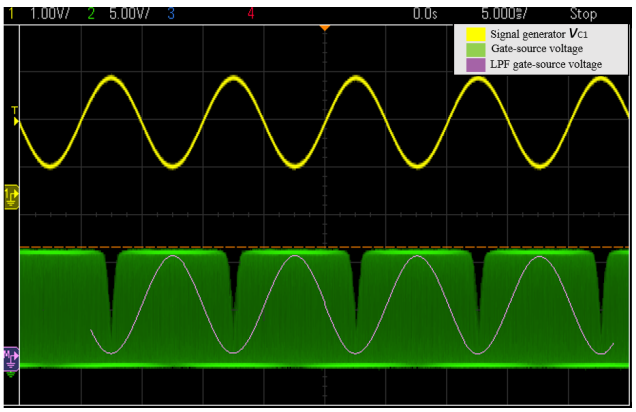


**Figure 5.13:** Gate-source voltage applied to top MOSFET of first leg in order to mitigate ripple component of low-voltage feedback signal $v_{C1}$

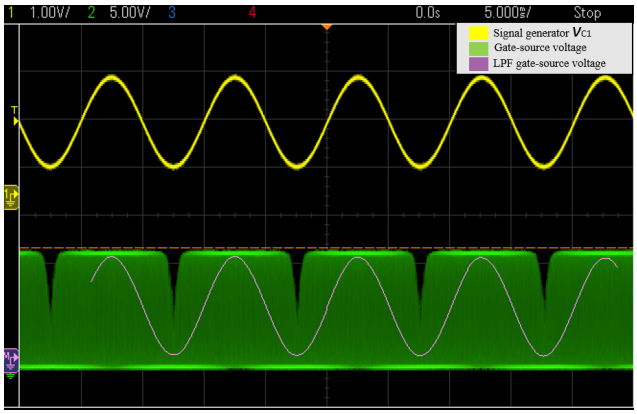


**Figure 5.14:** Gate-source voltage applied to top MOSFET of second leg in order to mitigate ripple component of low-voltage feedback signal $v_{C1}$

As expected, the first switch is modulated with a signal that is 180° opposite that of the ripple component of the feedback signal. This is proof of the proper functionality of the control scheme and code. Based on these gate-source signals, the drain-source voltages for the same two switches are obtained in Figures 5.15 and 5.16. Once again the software low-pass filter is used.

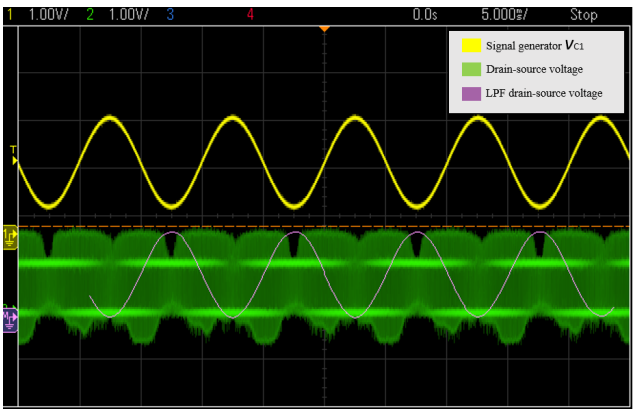


**Figure 5.15:** Drain-source voltage across top MOSFET of first leg generated to mitigate ripple component of low-voltage feedback signal $v_{C1}$

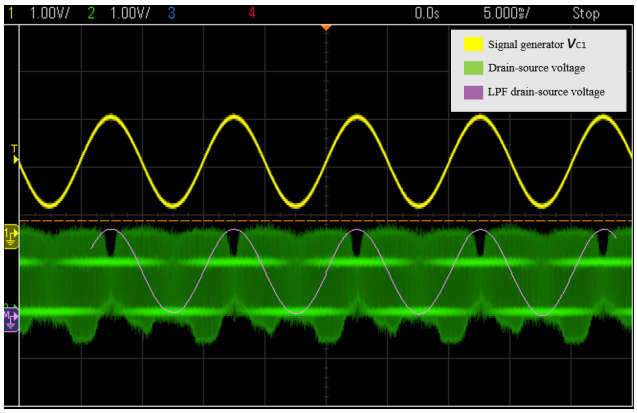


**Figure 5.16:** Drain-source voltage across top MOSFET of second leg generated to mitigate ripple component of low-voltage feedback signal $v_{C1}$

Both of these waveforms manage to correctly follow the inverse of the two halves of the feedback signal. As the proper operation of the controller and of the MOSFETs is observed, the resulting output voltage $v_{C3}$ can be recognized in Figure 5.17.

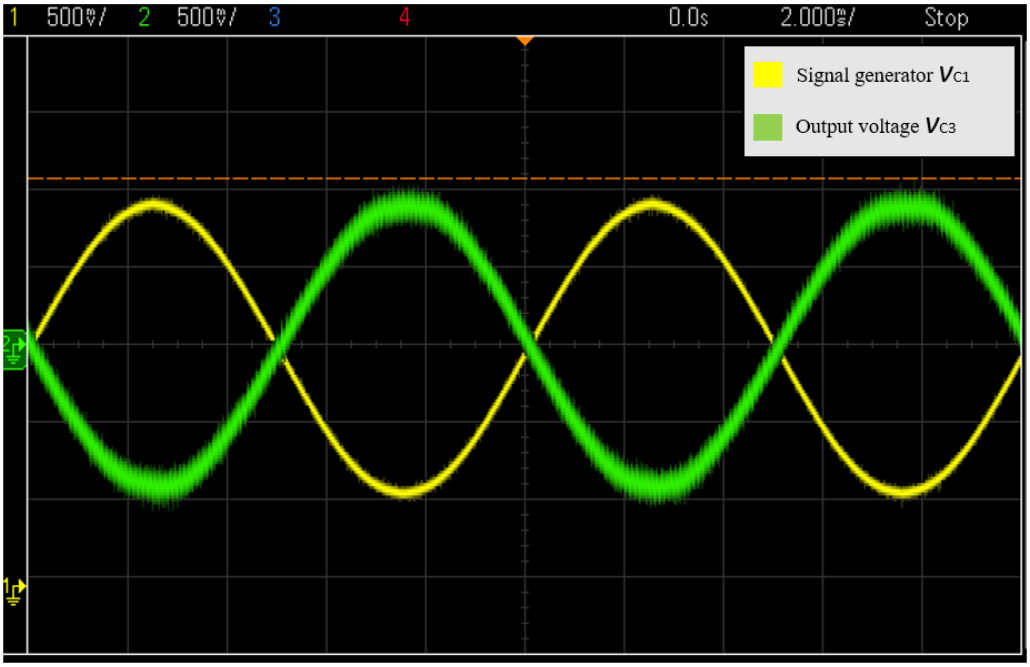


**Figure 5.17:** Resulting output voltage $v_{C3}$ controlled to mitigate the ripple component in the low-voltage feedback signal $v_{C1}$

$v_{C3}$ is successfully controlled to be equal in amplitude and of opposite sign to the ripple component of $v_{C1}$. This proves that the ripple component is properly identified by the controller high-pass filter and that the generated PWM signals manage to modulate the auxiliary circuit accordingly, so that this ripple component can eventually be eliminated from the terminal voltage $V_{AB}$. As the waveform is sinusoidal with a low visible harmonics content, it can also be concluded that the LC filter was designed correctly.


**Figure 5.18:** Resulting output voltage $v_{C3}$ controlled to mitigate low-voltage feedback signal $v_{C1}$, across a larger time interval

$v_{C3}$ can be observed to be stable over a larger period of time in Figure 5.18. Finally, on top of the proper amplitude and waveform, it also manages to hold the same 100 Hz frequency as the ripple component in the feedback $v_{C1}$, accomplishing all the requirements necessary in order for it to successfully negate this ripple and to create a constant DC voltage for $V_{AB}$.

In order to test its performance under different load conditions, the feedback signal representing $v_{C1}$ is lowered to a variation of 1.1285V to 1.937 V, with the same DC offset. This represents a $v_{C1}$ of 420 V amplitude, which is the value obtained under a 150 W load, also used previously in the simulations in Section 5.1. This corresponds to a 20 V peak ripple component and the results are depicted in Figures 5.19 and 5.19.

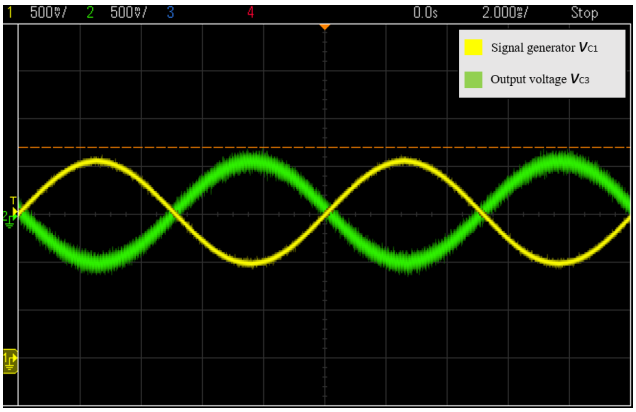


**Figure 5.19:** Resulting output voltage $v_{C3}$ controlled to mitigate a low-voltage feedback signal $v_{C1}$ equivalent to a reduced load of 150 W

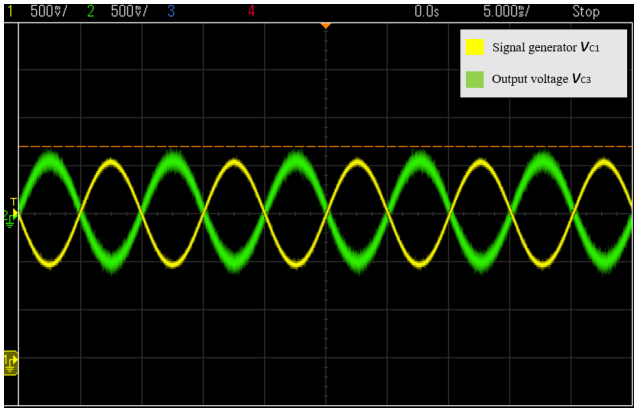


**Figure 5.20:** Resulting output voltage $v_{C3}$ controlled to mitigate a low-voltage feedback signal $v_{C1}$ equivalent to a reduced load of 150 W, across a larger time interval

The algorithm manages to adapt to the new measurement accordingly, generating an appropriate $v_{C3}$. Therefore, it is concluded that the controller and the auxiliary circuit maintain their proper

functionality under different load conditions too.

## 5.3 Summary

This chapter has focused on simulating, testing and validating the active capacitor design previously developed based on the theoretical considerations presented in Chapter 3 and on the numerical calculations presented in Chapter 4.

Section 5.1 presented the simulations undertaken using the PLECS platform. Firstly, the stand-alone active capacitor circuit, controlled by the scheme designed in Subsection 4.4, was simulated successfully, the end result being an almost entirely eliminated $\Delta v_{C1}$ ripple and a $V_{AB}$ terminal voltage that oscillates by only 3 V, even outperforming the initial passive component by a substantial margin.

Secondly, building on these results, the active capacitor design was coupled with a micro-inverter model. Although an increase in the final ripple component in $V_{AB}$ was observed, the overall results were still considered satisfactory, as they were closely in line with the performance of the passive capacitor in the same simulation, even under load change conditions.

With this design and control scheme successfully modeled, the next step was building an appropriate PCB to mount the necessary components, as well as transferring the control into code appropriate for the DSP used, both of which were then validated in a laboratory setup, with the results presented in Section 5.2 in the form of oscilloscope measurements. The conclusion was that this topology can be used to generate a suitable output voltage $v_{C3}$ equal in magnitude to $\Delta v_{C1}$, but of opposite sign, which can be implemented to cancel the ripple component from the overall terminal voltage $V_{AB}$. The success of this layout and control is especially important when considering that it validates the primary target of the design process, as it manages to create a system which can be used to counteract the ripple caused by a reduced DC-link capacitor, while maintaining all of its components under the 20 mm height limit.

# Chapter 6

# Discussion

The objective of this thesis was to investigate the suitability of a two-terminal active capacitor as the DC-link of a 350 W embedded solar PV micro-inverter. The context of this research was formed by recent emerging trends in photovoltaics manufacturing, which were focused on and succeeded in creating new designs which resulted in thinner panels, due to various technical and economical incentives. These technological advancement raised a problem for the current generation of panel-embedded micro-inverters, which are restricted when it comes to any possible height reduction by the characteristics of the conventional passive DC-link capacitor.

Therefore, the active capacitor is presented as a viable alternative that would solve this issue. A standard 350 W PV micro-inverter, presented in Section 4.1, is used as the design basis of this proposal. The design implemented over the course of this project managed to reduce the height of its initial DC-link, in the form of a passive capacitor at 30 mm, by replacing it with an active capacitor at 20 mm. The results obtained proved that this can be a viable substitute that can mimic the performance of the initial capacitor when it comes to ripple attenuation and DC-voltage stabilisation, while also providing the advantage of a reduced height.

Sections 2.1 and 2.2 elaborate on why the current passive solution is limited by the necessity of balancing its increased size and height with its ripple mitigation capabilities. As described by Figure 2.7, the active capacitor architecture circumvents this constraint by combining a small capacitor with the auxiliary circuit in Figure 2.6 and with the control scheme in Figure 3.2. Chapter 4 covers the design of such an active capacitor for the specific ratings of the 350 W micro-inverter, which is then validated in by the simulations in Section 5.1.

In fact, Figure 5.1 can also be used as a showcase of the effect that a reduced capacitor has on the DC-link voltage. When the capacitance value is reduced to 16 $\mu$F, in line with the reduction in height made necessary by the thinner PV panels, the resulting $v_{C1}$ voltage across this capacitor is affected by a large ripple component of almost 100 V. This would be the resulting voltage of the entire DC-link, if not for the implementation of the series-connected auxiliary circuit, which counteracts this oscillations by its output $v_{C3}$, resulting in the ripple component being almost entirely eliminated from the terminal voltage $V_{AB}$. The same behaviour was afterwards replicated in a larger PV micro-inverter model, specifically modified to reflect the one in Section 4.1.

In both test environments, stand-alone and micro-inverter model, the active capacitor manages to duplicate, or sometimes even out-perform, the initial passive capacitor when it comes to its ripple mitigation effectiveness, all while maintaining its 20 mm height limit. This is primarily attributed to the effectiveness of its control algorithm. Some negative characteristics of the active capacitor can however be observed in Figure 5.5, such as the impact of the auxiliary circuit MOSFETs on the stability of $V_{AB}$.

With the design thus validated, the next step was represented by building the corresponding PCB for the hardware implementation, with the final product being presented in Figures 5.10 and 5.11. The objective of the experimental process was to test the capability of the auxiliary circuit and of the control scheme to generate a corresponding $v_{C3}$, equal in magnitude but of opposite sign to the ripple component of a feedback signal $v_{C1}$. Although the PCB was equipped with all the necessary components for a full active capacitor test, meaning the voltage sensors for measuring the externally

applied $v_{C1}$ and the $v_{C2}$, as well as the self supply circuit for powering the gate drivers and the controller, testing the control scheme and the auxiliary circuit in this manner was prioritised in the context of limited laboratory time and access. This was done because, once their proper functionality was proved in Section 5.2, these two systems will serve as the backbone of any further experimental implementations, since they are the mechanism by which the active capacitor can react to stabilise the terminal voltage $V_{AB}$. As these tests were successful, it can be concluded that the main objective of the active capacitor design, which was to prove its ripple mitigation capabilities by a generating an output voltage controlled to counteract this ripple component, is achievable while still limiting all its components to a height of 20 mm.

Based on the bill of materials provided in Annex B, the total price of the components has amounted to approximately 10.67 EUR. Added to this is the price of the PCB at 4.6 EUR, resulting in a total of 15.27 EUR, without including the price of the controller. This is a relatively high cost compared to that of the original passive capacitor at 5.7 EUR. However, it should be mentioned that this prototype serves as a first design of this particular active capacitor and the primary focus was placed on facilitating the hardware testing process, not on mass manufacturing. Because of that, extra components, such as extra parallel capacitors, were included, which would normally not be the case if cost optimisation was the main objective. Likewise, the size of the PCB can also be further reduced once testing the design is no longer necessary, which would also lower the overall cost. Accordingly, these changes would serve to make the active capacitor an even more competitive alternative to the passive capacitor, when used as a solar micro-inverter DC-link.

In conclusion, although further testing and cost optimisations are required, the active capacitor can be designed with a maximum height of 20 mm and still manage to act as a suitable solution for the DC-link of an embedded solar micro-inverter, thanks to its structure being able to counteract the resulting ripple component.

Chapter 7

# Future Work

The objective of this chapter is to specify several methods and topics by which the scope of this report could be further continued and enlarged. These range from further possible experimental work to different designs that can be undertaken.

The results of Section 5.2 serve as the basis of the full operation of the active capacitor and can be completed by a closed-loop hardware test. Before that could be implemented, the $v_{C1}$ and $v_{C2}$ voltage sensors would have to included and tested, with the resulting scaling factor being compared to the one calculated in Annex A. After that the circuit can be supplied with an external voltage source or even connected as the DC-link of an existing micro-inverter system. Knowing that the auxiliary circuit and the control scheme were already successfully tested, it is expected that this would result in a mitigation of the ripple component created across $v_{C1}$, which would be generate an approximately constant $V_{AB}$.

Once the close-loop implementation is successful, the current design of the PCB can be fully validated by implementing the self-supply function as well. This would mean that no external voltage supply would be connected to the circuit, except for the voltage applied to the AB terminals of the DC-link. The objective is that the self-supply structure manages to power the gate drivers and the external controller, continuing the operation of the active capacitor.

Before a new design can be undertaken, the temperature of the present one can be measured while in operation. This would serve to pinpoint any spots on the circuit where the temperature is exceeding the advisable limits. This knowledge can be later used during a new design process, which aims to improve the current prototype. Thermal simulations can be undertaken during this new design phase, based on the measurements obtained on the previous one, to calculate the expected lifetime of the components.

Likewise, this new design process can be used to improve on other aspects of the previous PCB, such as reducing its size or the length of the traces. As stated in the last chapter, extra components were included in the current design in order to ease the experimental process. However, considering the results obtained in Section 5.2, it can be concluded that components such as the LC filter were successfully designed initially, as the resulting $v_{C3}$ has a relatively low harmonic content. This can allow for future prototypes to not include some of the additional components previously used, which can lead to a lower overall cost.

Finally, in order to create the final two-terminal active capacitor, the external DSP has to be replaced with a micro-controller chip mounted together with the active capacitor. The performance of this controller can also be significantly reduced when compared to the DSP used for this report, simplifying the programming stage, since, as previously state, the code necessary for implementing the control scheme is relatively simple.

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# Appendix A

# Voltage sensors

Two voltage sensors are necessary for down-scaling $v_{C1}$ and $v_{C2}$, so that they can be used as input signals for the DSP controller, which only accepts inputs between 0 V and 3 V. Differential amplifiers are used for this purpose, having their circuit diagram and governing equation presented in Figure A.1 and Equation A.1, respectively.

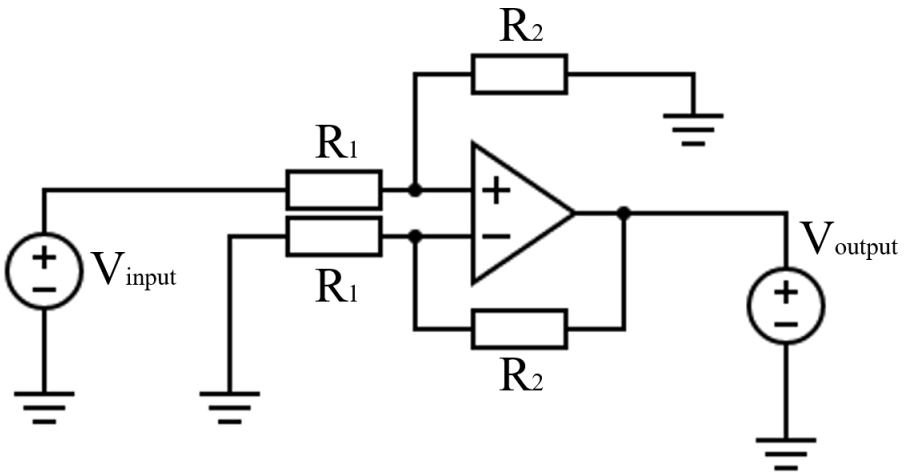


**Figure A.1:** Diagram of differential amplifier used as voltage sensors

$$V_{output} = \frac{R_2}{R_1} V_{input} \tag{A.1}$$

Using one amplifier, $v_{C1}$ is down-scaled from a range of 300-500 V to one of 1.6-2.65 V. This output is then fed into another amplifier, in which the negative input is a voltage of 1.35 V, obtained with a voltage divider from the 12 V used to power the gate driver. This is done in order to subtract from the 1.6 V minimum and extend the resolution of the final signal to a range of 0.522-2.543 V. This entire sensor circuit is simulated and the comparison between $v_{C1}$ before and after scaling is presented in Figure A.2. On the other hand, $v_{C2}$ is approximated as a constant voltage at 100 V, so it is only scaled down to 2.23 V using one amplifier, with the results presented in Figure A.3.

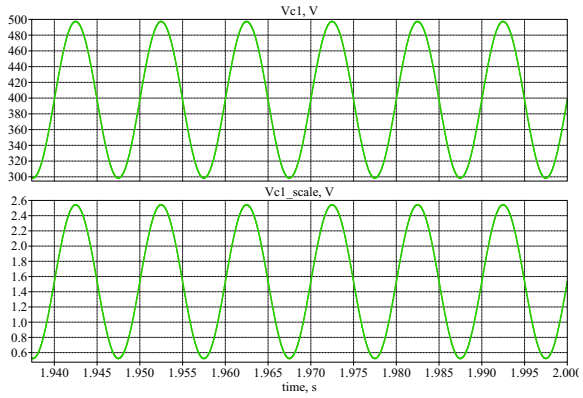


**Figure A.2:** Comparison of $v_{C1}$ voltage before and after down-scaling

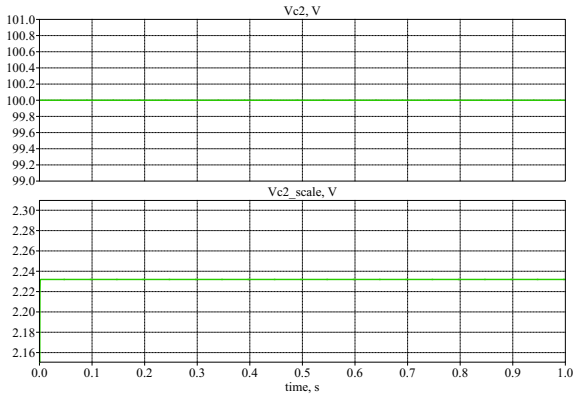


**Figure A.3:** Comparison of $v_{C2}$ voltage before and after down-scaling

The $R_1$ and $R_2$ resistors obtained for each of the two sensors, used to control the scaling factors, are implemented in the PCB design and can be found in the bill of materials in Appendix B.

# Appendix B

# Bill of materials

| Comment | Description | Designator | Footprint | LibRef | Quantity |
|---|---|---|---|---|---|
| ESL105M100AC3AA | Capacitor Polarised | C1, C3, C8 | CAPPRD200W50D500H1250 | ESL105M100AC3AA | 3 |
| UCY2C221MHD6TN | Capacitor Polarised | C2 | CAPPRD750W80D1825H2150 | UCY2C221MHD6TN | 1 |
| 1u | CGA3E1X7R1E105K080AC | C4, C6 | CAPC1608X90N | CGA3E1X7R1E105K080AC | 2 |
| 0.1u | CGJ3E2X7R1E104K080AA | C5, C7 | CAPC1608X90N | CGJ3E2X7R1E104K080AA | 2 |
| 1u | CGA9P4X7T2W105M250KA | C9 | CAPC5750X280N | CGA9P4X7T2W105M250KA | 1 |
| ECW-FE2W224KA | Capacitor | C10 | ECWFE2W224KA | ECW-FE2W224KA | 1 |
| C4AQLLU4800A12K | Capacitor | C11, C12 | C4AQLLU4800A12K | C4AQLLU4800A12K | 2 |
| 1uf | C2012X7S2A105K125AB | C13, C15, C16, C17, C18, C20, C21, C22, C23 | CAPC2012X145N | C2012X7S2A105K125AB | 9 |
| CL10B105MO8NNWC | Capacitor | C14 | CAPC1608X90N | CL10B105MO8NNWC | 1 |
| CL10A225KP8NNNC | Capacitor | C19 | CAPC1608X90N | CL10A225KP8NNNC | 1 |
| 1n | CGA3E2X7R2A102K080AA, Capacitor CGA3E2X7R2A102K080AA | C24, C26, C28, C34, C35, C36, C37 | CAPC1608X90N | CGA3E2X7R2A102K080AA | 7 |
| 1u | C1608X7R1E105K080AB | C25, C27, C30 | CAPC1608X80N | C1608X7R1E105K080AB | 3 |
| CGA3E2X7R1E104K080AA | Capacitor | C29 | CAPC1608X90N | CGA3E2X7R1E104K080AA | 1 |
| 685MMR100K | Capacitor | C31, C32 | 685MMR100K | 685MMR100K | 2 |
| 100n | CGA3E2X7R1E104K080AA | C33 | CAPC1608X90N | CGA3E2X7R1E104K080AA | 1 |
| MURS120-E3_5BT | Diode | D1, D2 | DIOM5436X244N | MURS120-E3_5BT | 2 |
| CDBURT0530LL-HF | Schottky Diode | D3, D4, D5, D6 | CDBURT0530LLHF | CDBURT0530LL-HF | 4 |
| CUS551V30,H3F | Schottky Diode | D7 | 1SS357TPH3F | CUS551V30,H3F | 1 |
| IRS2007SPBF | Integrated Circuit | Driver 1, Driver 2 | SOIC127P600X175-8N | IRS2007SPBF | 2 |
| TL783CKTTR | Integrated Circuit | IC1 | TO254P1524X483-4N | TL783CKTTR | 1 |
| TPS7A2501DRVR | Integrated Circuit | IC2 | SON65P200X200X80-7N | TPS7A2501DRVR | 1 |
| OPA171AIDBVT | Integrated Circuit | IC5 | SOT95P280X145-5N | OPA171AIDBVT | 1 |
| OPA2171AQDRQ1 | Integrated Circuit | IC6 | SOIC127P600X175-8N | OPA2171AQDRQ1 | 1 |
| TSW-104-07-L-S | Connector | J1, J2 | HDRV4W64P0X254_1X4_1016X248X838P | HTSW-104-07-L-S | 2 |
| TSW-108-07-L-S-LL | Connector | J3 | HDRV8W64P0X254_1X8_2032X248X838P | HTSW-108-07-L-S-LL | 1 |
| SRR1205-250ML | Inductor | L1, L2 | SRR1205101KL | SRR1205-250ML | 2 |
| IPD530 | MOSFET (N-Channel) | Q1, Q2, Q3, Q4 | IPD70R900P7SAUMA1 | IPD530N15N3GATMA1 | 4 |
| CRCW060310R0FKEAC | Resistor | R1, R2, R3, R4, R17, R20 | RESC1608X55N | CRCW060310R0FKEAC | 6 |
| CRCW060360R4FKEA | Resistor | R5 | RESC1608X50N | CRCW060360R4FKEA | 1 |
| 6.98R | CRCW06036R98FKEA | R6 | RESC1608X50N | CRCW06036R98FKEA | 1 |
| CRCW06031M18FKEA | Resistor | R7 | RESC1608X50N | CRCW06031M18FKEA | 1 |
| CRCW06033M65FKEA | Resistor | R8 | RESC1608X50N | CRCW06033M65FKEA | 1 |
| 10k | CRCW060310K0JNEA | R9, R21 | RESC1608X50N | CRCW060310K0JNEA | 2 |
| CRCW060315K0JNEBC | Resistor | R10, R30 | RESC1608X55N | CRCW060315K0JNEBC | 2 |
| CRCW0603510RJNEA | Resistor | R11, R19 | RESC1608X50N | CRCW0603510RJNEA | 2 |
| 3.4k | CRCW08053K40FKEA | R12, R36 | RESC2012X50N | CRCW08053K40FKEA | 2 |
| CRCW1206174KFKEA | Resistor | R13, R14, R15, R16, R26, R27, R28, R29 | RESC3216X60N | CRCW1206174KFKEA | 8 |
| 4.75k | CRCW06034K75FKEA | R18 | RESC1608X50N | CRCW06034K75FKEA | 1 |
| 196k | CRCW1206196KFKEA | R22, R23, R24, R25, R32, R33, R35 | RESC3216X60N | CRCW1206196KFKEA | 7 |
| CRCW1206196KFKEA | Resistor | R31 | RESC3216X60N | CRCW1206196KFKEA | 1 |
| CRCW06034K75FKEA | Resistor | R34 | RESC1608X50N | CRCW06034K75FKEA | 1 |
| CRCW0603806RFKEA | Resistor | R37 | RESC1608X50N | CRCW0603806RFKEA | 1 |
| 150R | CRCW0603150RFKEA | R38 | RESC1608X50N | CRCW0603150RFKEA | 1 |

**Figure B.1:** Bill of materials for active capacitor PCB