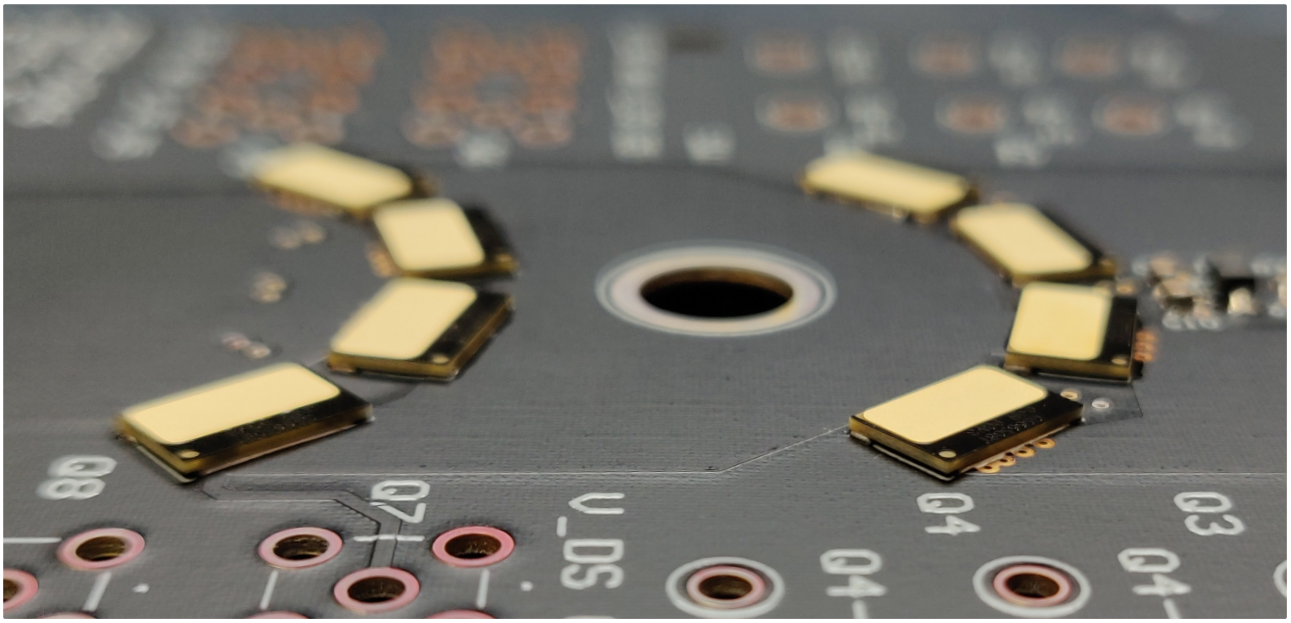
Design and Optimisation of a Half-Bridge Switching Module With Parallel GaN HEMTs for High Power Applications Using Finite-Element Analysis

Master's Thesis

Power Electronics and Drives



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STUDENT REPORT

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Abstract:

The main objective of this project was to design a half-bridge switching module with four GaN HEMTs in parallel. The parallel operation of GaN HEMTs was analysed to understand how the parasitics would affect the operation. Three different designs were created, based on the previous analysis, using a digital design process with the FEA software Ansys Q3D to calculate the parasitic content. These parasitics were then implemented in an LTspice model to account for all the parasitics and non-linearities in the designs. This process was further optimised to minimise the number of simulations needed as the parallel designs required a high number of iterations per design. A method of integrating LTspice with Matlab was developed, where a simulation could be looped, with each iteration containing different component values. Using optimisation theories, the components could be evaluated, and an optimal component could be selected. The switching performances of the three designs were tested in the laboratory with a double pulse test, where one of the designs switched at 400 V and 50 A, but a failure occured at 60 A. Undesired ringings on the gate-source voltage were observed in one of the other designs, which is thought to be caused by too high gate loop inductance.

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By signing this document, each member of the group confirms participation on equal terms in the process of writing the project. Thus, each member of the group is responsible for the all contents in the project.

Dansk Resumé

I denne rapport blev et halvbro-skiftemodul, med fire galliumnitrid-baserede chips i parallel, designet til at kunne skifte ved en spænding på 400 V og en strøm på 80 A. Det var valgt at lave et halvbro-skiftemodul med fire galliumnitrid-baserede chips, for at kunne øge effekten og dermed antallet af applikationer hvor disse chips kan bruges. Dermed kan man udnytte deres fordele, som f.eks. hurtige skiftetider, lave skiftetab og mulighed for høj effekttæthed.
Eftersom at galliumnitrid-baserede chips er følsomme over for støj fra power delen af kredsløbet, så blev der lavet en analyse af hvilke parameter der påvirker deres virke mest, når de er anvendt i parallel. De primære parameter der påvirker det parallelle virke er source induktansen og koblingen mellem effekt og styrekredsene. Disse parametre skal minimeres og holdes så symmetrisk som muligt på tværs af alle fire chips. Derudover, så skal induktanserne i effekt og styrekredsen induktansen minimeres og ligeledes for styrekredsen skal det holdes så symmetrisk som muligt.
Tre forskellige designs blev lavet for at teste effekten af de forskellige parametre, for at kunne validere hvilken design strategi der ville være bedst for et halvbro-skiftemodul. En digital design process blev anvendt, hvor Ansys Q3D blev brugt til at beregne det parasitiske indhold på de tre designs. Dermed var det muligt at analysere på dynamikkerne i kredsløbene både numerisk og ved hjælp af LTspice simuleringer. Denne proces blev samtidig optimeret i forhold til tidligere processer, hvilket reducerede antallet af nødvendige simuleringer til kun en ved at videreudvikle databehandlingen fra den simulering.
Ligeledes, så blev processen med at udvælge komponenter optimeret ved at LTspice og Matlab blev integreret. Dette muliggjorde at Matlab kunne bruges til at køre flere LTspice simuleringerne i træk og samtidig skifte imellem hver simulering. Dette blev anvendt til at optimere på modstande og ferritkerner i styrekredsen til de galliumnitrid-baserede chips.
Alle tre designs blev produceret på printplader og testet eksperimentielt. Dette blev gjort ved at generere to pulser, hvor ved dynamikkerne ved tænd og sluk af en galliumnitrid-baseret chip kunne blive testet ved forskellige strøm amplituder. Dette blev testet på det første design ved 400 V, hvor der blev skiftet ved en strøm på 60 A. Efter det havde skiftet, så blev der opdaget nogle uhensigtsmæssigheder i designet, da en af galliumnitrid chippene eksploderede.
I testene for det næste design blev der foretaget flere målinger for at bedre kunne undersøge hvilke forhold der påvirkede foregående design. Med det andet design blev der lavet gentagende test ved flere strømamplituder, men ved tredje test på 30 A og 400 V skete der en kortslutning imellem to chips. I dette tilfælde mistænkes det, at der på den øverste chip var kommet støj ind på styrekredsen, som tændte chippen mens at den nederste chip var tændt.
Det sidste design blev ligeledes testet, men grundet opdagelsen før, så blev der målt nøje på styrekredsen på de øverste chips. Her det opdaget ved 100 V, at der var støj på øverste styrekreds som fik spændingen til at gå over grænsespændingen for chippene. Dette skyldes formentlig for høj induktans i styrekredense for de øverste chips, som skaber de høje oscillationer.
Ud fra den digitale design process og de eksperimentielle data, så kan det konkluderes, at der i et halvbro-skiftemodul med galliumnitrid chips skal være stor fokus på design af styrekredesen i forhold til at minimere induktanserne. Den digital design og optimeringsproces har potentiale til at hjælpe med at teste mange forkellige komponenter i et ulineært kredsløb, som med høj præcision afspejler det praktiske kredsløb. Dette kan sikre at flere iterationer bliver testet digitalt uden at bygge ressourcekrævende fysiske prototyper.

Preface

This Master's thesis is written by group *PED4 - 1046*, a 4th semester Master's student group with specialisation in Power Electronics and Drives at the Department of Energy Technology at Aalborg University.

The following software has been used to:

- **LaTeX** - Write and format the report.
- **Mendeley** - Sort and share the bibliography.
- **MATLAB** - General calculations, scripting and data processing.
- **Microsoft Excel** - Data processing.
- **Inkscape** - Create figures.
- **Comsol** - Thermal analysis.
- **LTspice** - Simulation of electrical circuits.
- **Altium Designer** - Design of PCB.
- **Ansys SIwave** - Conversion of PCB files.
- **Ansys Q3D** - FEA of PCB layout.
- **Code Composer Studio** - Program DSP.

Reader's Guide:

On page v, a table of contents is given. When viewing this report as a PDF, hyperlinks will allow fast navigation to the desired sections.
Page vii displays a nomenclature listing the abbreviations, as well as the variables and their respective units used in this report.

The bibliography on page 122 presents the literature used in this report. The references are given in the following format:

[Author][Title](Institution)(ISBN)[Year](URL)(Date Accessed)

Where fields in square brackets are mandatory, while regular brackets are only relevant for certain formats, i.e books or web pages. The bibliography entries are sorted after their appearance in the text. The references will be placed according to the text they are related to. This can be seen in the following example:

[1, p. 1].	*Before period*	Will add to the sentence before.
. [1, p. 1]	*After period*	Will add to the section before.

Table of Contents

Nomenclature

Acronyms

2DEG	2D-Electron-Gas
Al	Aluminium
ANPC	Active-Neutral-Point-Clamped
Cu	Copper
DBC	Direct Bonded Copper
DPT	Double Pulse Test
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FB	Ferrite Bead
FEA	Finite Element Analysis
FFT	Fast Fourier Transform
FoM	Figure of Merit
GaN	Gallium Nitride
GD	Gate Driver
HB	Half-Bridge
HEMT	High Electron-Mobility Transistor
IMS	Insulated Metal Substrate
MLCC	Multi-Layer Ceramic Capacitor
NPC	Neutral-Point-Clamped
Qx	GaN HEMT x
Si	Silicon
SiC	Silicon Carbide
SOA	Safe Operating Area
SW	Switch Node
THD	Total Harmonic Distortion
TIM	Thermal Interface Material
WBG	Wide-Band-Gap

Variables

Symbol	**Description**	**Unit**
δ	Skin Depth	[m]
μ	Permeability	[H/m]
ρ	Resistivity	[Ωm]
ζ	Damping Factor	[-]
A	Area	[m^2]
BW	Bandwidth	[Hz]
C	Capacitance	[F]
D	Diameter	[m]
d	Distance	[m]
di/dt	Rate of Change of Current	[A/s]
dv/dt	Rate of Change of Voltage	[V/s]
E	Energy	[J]
f	Frequency	[Hz]

H	Height	[m]
h	Heat Transfer Coefficient	[W/m^{2}K]
I	Current	[A]
K	Coupling Coefficient	[-]
k	Thermal Conductivity	[W/mK]
L	Inductance	[H]
l	Length	[m]
M	Mutual Inductance	[H]
P	Power	[W]
Q	Electric Charge	[C]
q	Heat Flux	[W/m^2]
Q_f	Quality Factor	[-]
R	Resistance	[Ω]
R_Θ	Thermal Resistance	[K/W]
T	Temperature	[°C]
t	Time	[s]
V	Voltage	[V]
w	Width	[m]
Z	Impedance	[Ω]

Indices

A	Ambient
avg	Average
CH	Case to Heat Sink
CLK	Clock
CS	Common-Source
D	Drain
DD	On Gate Supply
Dec	Decoupling
DL	Drain-Lead
DS	Drain-Source
EE	Off Gate Supply
El	Electrolytic
G	Gate
GDr	Gate Driver
GND	Ground
GP	Plateau
GS	Gate-Source
HA	Heat Sink to Ambient
iss	Input (Capacitance)
J	Junction
JC	Junction to Case
JPCB	Junction to PCB
L	Inductor
max	Maximum
N	Pull-down
off	Off
on	On
oss	Output (Capacitance)
P	Power

par	Parallel
PCBA	PCB to Ambient
pk	Peak
Pup	Pull-up
QS	Quasi-Common-Source
r	Resonance
S	Source
SD	Source-Drain
ser	Series
SL	Source-Lead
SW	Switch Node
sw	Switching
th	Threshold
Z	Zener

Chapter 1

Introduction

As there is a global growth in population and wealth the demand for energy is increasing. Alongside the increasing demand for energy there is also a requirement for higher efficiencies in power conversion and generation. As the limits of silicon (Si)-based power transistors are approached, new solutions must be developed [1]. One area which has seen increased interest in recent time is the use of Wide-Band-Gap (WBG) semiconductor materials instead of Si, as these promise to offer increased efficiency and quicker switching times. The most prominent WBG materials for use in power electronics are Silicon-Carbide (SiC) and Gallium-Nitride (GaN). SiC is the more mature material, while GaN is only starting to see increased use in power electronics. As GaN is still in the early stages of development, there are still some significant challenges to be overcome. One of these challenges is the power level which can be achieved by the devices, where GaN based devices fall behind their counterparts. This project will investigate the challenges of increasing power levels of GaN based solutions, and propose a design solution of a GaN-based switching module. [2][3][4]

GaN is used in a High Electron Mobility Transistor (HEMT) structure in order to obtain the high performance switching to compete with MOSFETs and similar power transistors. GaN HEMTs have the advantages of low on-resistance within the 650 V range, which leads to lower conduction losses compared to Si MOSFETs. GaN HEMTs also have very small intrinsic capacitances due to their structure, which has the benefit of decreasing the turn-off and turn-on times of the device yielding lower switching losses and allowing for higher system efficiencies. This also enables very high switching frequencies which can help reduce the size of passive components, which further helps to increase power density of converters using GaN HEMTs. [2][4][5]
Due to their lateral structure, GaN HEMTs are mostly used in applications up to 650 V as reaching higher breakdown voltages would require a vertical structure, which is currently at the experimental stage. [4][6]

The advantages stated above have been realised in different applications, where the low switching losses and high power density of the GaN HEMTs have allowed for converters with high efficiencies and high power densities. An example of an application where GaN HEMTs are used, is in a 10 kW Active-Neutral-Point-Clamped (ANPC) converter [7], where GaN HEMTs were applied as a high-frequency switching leg to replace the diode-leg in an NPC converter. This was done to minimise the passive components and to increase system efficiency [7]. Also, a fully GaN based ANPC was designed with a power rating of 2 kW [8].
GaN HEMTs have been used in different multilevel converters with a power rating of 3.1 kW and considerations have been made for a 70 kW converter. Again, the advantage seen was a reduced inductor. Moreover, due to the operation of the multilevel converters and high switching frequency of the GaN HEMTs the output voltage had a low amplitude high frequency ripple, yielding low Total Harmonic Distortion (THD) on the output current. [9][10]
Moreover, GaN HEMTs have been implemented in AC-DC converters such as the bridgeless totem-pole converter, where the symmetry of the GaN HEMT structure allows for reverse conduction without the use of a diode, enabling efficient hard-switching as there is no reverse recovery effect. By hard-switching, a low THD is achieved as the inductor current could be controlled more precisely [11][12]. This also enabled better power factor correction. Using GaN HEMTs in this topology, it is possible to achieve efficiencies close to 99 % [13]. However, the power ratings for the referenced converters are only ranging from 1 kW to 2.2 kW.

It is evident from the different applications referenced using GaN HEMTs, that they are not commonly used in power ranges above 10 kW. This is corroborated in Figure 1.1, where the power and switching frequency ranges of different semiconductors are compared.

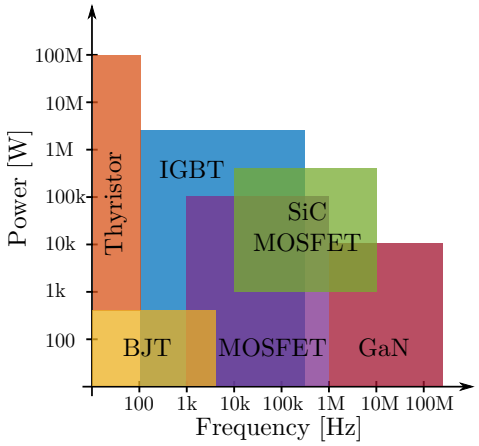


Figure 1.1: Comparison of power rating and frequency range for different semiconductor technologies [14].

Common for all the applications referenced, is that the GaN HEMTs are used in a Half-Bridge (HB) configuration, where the power rating is mainly limited by the current capability of the specific GaN HEMT used. One way to increase the power capability of the HB switching module is to parallel the GaN HEMTs. This could increase the usage of GaN HEMTs in high power applications of up to 100 kW or above [15]. Parallel operation has been used for a 10 kW LLC DC-DC Converter where GaN HB switching modules were designed with two GaN HEMTs in parallel to increase the power capability. However, great care had to be taken in the PCB layout to ensure stable performance, as asymmetry in the parasitic content of the different loops, combined with the fast switching speeds could disturb the gate voltages of the GaN HEMTs, which due to the low threshold voltage of GaN HEMTs could cause unintended turn-on. [16] Other applications have successfully used two GaN HEMTs in parallel operation [17][18], but there is not much literature describing the parallel operation of more than two devices. This indicates that there might be some difficulty in paralleling more than two devices. This is also stated by GaN Systems, a manufacturer of GaN HEMTs [15]. But to increase the power level of GaN HEMTs and the applications range in which GaN HEMTs are used, the operation of more than two devices in parallel need to be studied.

With the small size of the GaN HEMTs, it is crucial to determine an adequate cooling solution that can dissipate the heat from the small packages of the GaN HEMTs as insufficient cooling can degrade the performance. [4][6]

In order to increase the power range of GaN HEMT based converters, this project will attempt to design a high power HB switching module with parallel GaN HEMTs. However, the above mentioned issues with design layout of parallel GaN HEMTs and the cooling of these will need further analysis in order to design a well-performing module. This leads to the initial problem stated below:

"What are the design issues with paralleling GaN HEMTs in a HB switching module, and which cooling solutions could be used, to achieve optimal performance."

This initial problem will be analysed in the following chapter, which will lead to the research question of the report.

Chapter 2

Problem Analysis

In this chapter, the initial problem stated in Chapter 1 will be examined. Firstly, the general function of a GaN HEMT will be explained by a short analysis of its structure and operation. This will be done to obtain a better understanding of its characteristics, which will help in the analysis of paralleling such devices. The different stages of the switching of a single GaN HEMT will be explained, where the issues of paralleling GaN HEMTs will be coupled to the switching dynamics. The analysis of the switching will form the basis for essential design rules for the parallel layout.
Next, different GaN HEMT devices will be compared in order to determine the most suitable devices for parallel operation in terms of high power rating and stable operation. Lastly, an analysis of different cooling solutions for these devices will be performed. Using this analysis, a better understanding of the possible cooling solutions is obtained, which will be used later in the design process, such that an optimal HB switching module can be designed.

2.1 Function of a GaN HEMT

To better understand the advantages, disadvantages, and operation of GaN HEMTs, the structure of the devices is analysed. This will be done by examining a general structure of a GaN HEMT as seen in Figure 2.1.

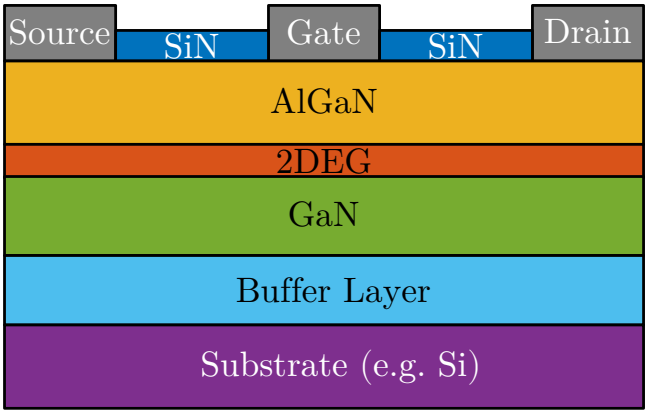


Figure 2.1: Schematic of the general structure and layers of a GaN HEMT.

The 2D-Electron-Gas (2DEG) channel enables the conduction of current between source to drain. The 2DEG is formed at the interface of the aluminium (Al) GaN and GaN layers, as the band-gap of each layer is different, forming a hetero-junction of different semiconductor materials. At this hetero-junction, a sudden jump in conduction band energy is observed, such that a narrow channel of electrons can form. The concentration of electrons is high in this channel, resulting in an extremely high electron mobility. This gives the HEMT its good conduction characteristics. In order to control the conduction of current between source and drain, a voltage is applied to the gate of the GaN HEMT, which will control the density of electrons in the 2DEG channel below the gate and thereby turn the device on or off. [19][20]

From the structure of the GaN HEMT, it can be observed that there is no pn-junction in the conduc-

tion path, yielding no intrinsic body diode. However, due to the structure of the HEMT, it can achieve reverse conduction without the disadvantages of body diodes. This means, that no reverse recovery effects are observed. This is advantageous in applications where hard-switching is preferred, where the losses and Electromagnetic Interference (EMI) can be reduced by use of GaN HEMTs. However, it should be noted that the voltage drop across the source-drain terminals in reverse conduction is usually higher than that of the body diodes of Si MOSFETs [21]. The voltage drop V_{SD} in reverse conduction is dependent on the threshold voltage, gate-source voltage during off-state and conduction losses: [20][21]

$$V_{SD} = (V_{th} - V_{GS}) + I_{SD} \cdot R_{DS,on} \tag{2.1}$$

As the gate-source voltage V_{GS} during the off-state can be negative to increase stability of the Gate Driver (GD), the voltage drop V_{SD} and losses during reverse conduction are large. This makes it crucial to minimise the dead-time to decrease these losses [21]. From the operation of the GaN HEMT it can be observed that the practical operation is similar to a Si MOSFET. This can be seen in Figure 2.2, where the I_{DS} vs. V_{DS} performance at different V_{GS} can be seen. These performance characteristics can be observed to be similar to the behavior of a conventional MOSFET.

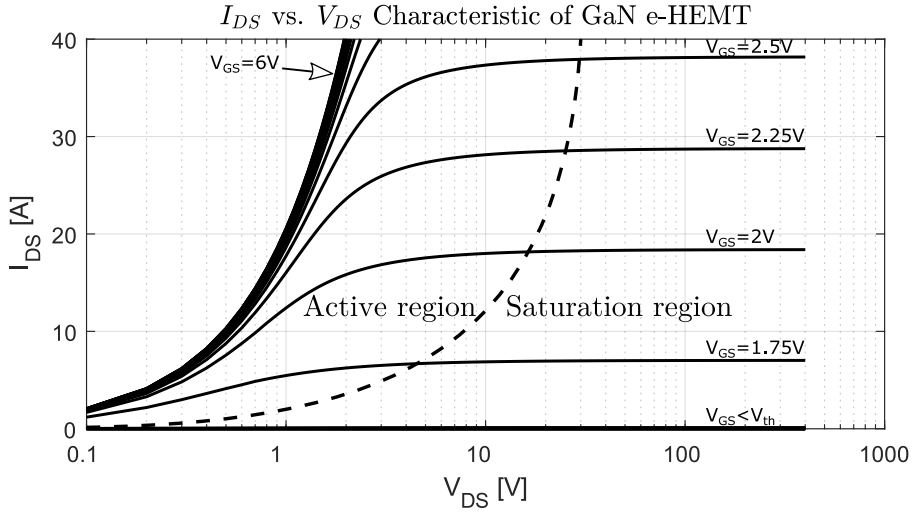


Figure 2.2: I_{DS} vs. V_{DS} characteristic performance of GaN e-HEMT. The figure is generated from a SPICE model of a GS66508T e-HEMT from GaN Systems. The active region is seen left of the dashed line, while the device is in saturation to the right of the dashed line.

As GaN has a high breakdown electric field compared to Si, less material is needed to achieve a given breakdown voltage compared to Si. This enables small packages and consequently fast switching as the intrinsic capacitances can be kept small. However, as the GaN HEMTs have low input capacitances and a low threshold voltage, they is sensitive to disturbances from high di/dt and dv/dt during these fast switching transients [6][22]. As mentioned in Chapter 1, great care has to be taken in the design of the circuitry due to the sensitivity to disturbances. These disturbances could have a greater effect when operating in parallel, as asymmetry in the parasitic content of the gate and power loops can cause different loading of each parallel GaN HEMT [15].

2.2 Analysis of Paralleling GaN HEMTs

In this project a high power GaN HEMT HB switching module is to be designed. In order to increase the current carrying capability of GaN HEMT HB switching modules, devices can be connected in parallel, effectively sharing the current between the different GaN HEMTs. The electrical characteristics of the GaN HEMT are advantageous for this purpose, as they have a temperature independent threshold voltage, as well as a positive $R_{DS,on}$ temperature dependence [23]. This helps to balance the load on the different GaN HEMTs, as any device experiencing higher current flow than others will heat up, increasing the $R_{DS,on}$. This reduces its current, resulting in a self-balancing behavior of the parallel GaN HEMTs [15]. An example of a schematic of a HB switching module utilising GaN HEMTs in parallel is seen in Figure 2.3. Parasitic components which are considered to be influential to the switching performance are included.

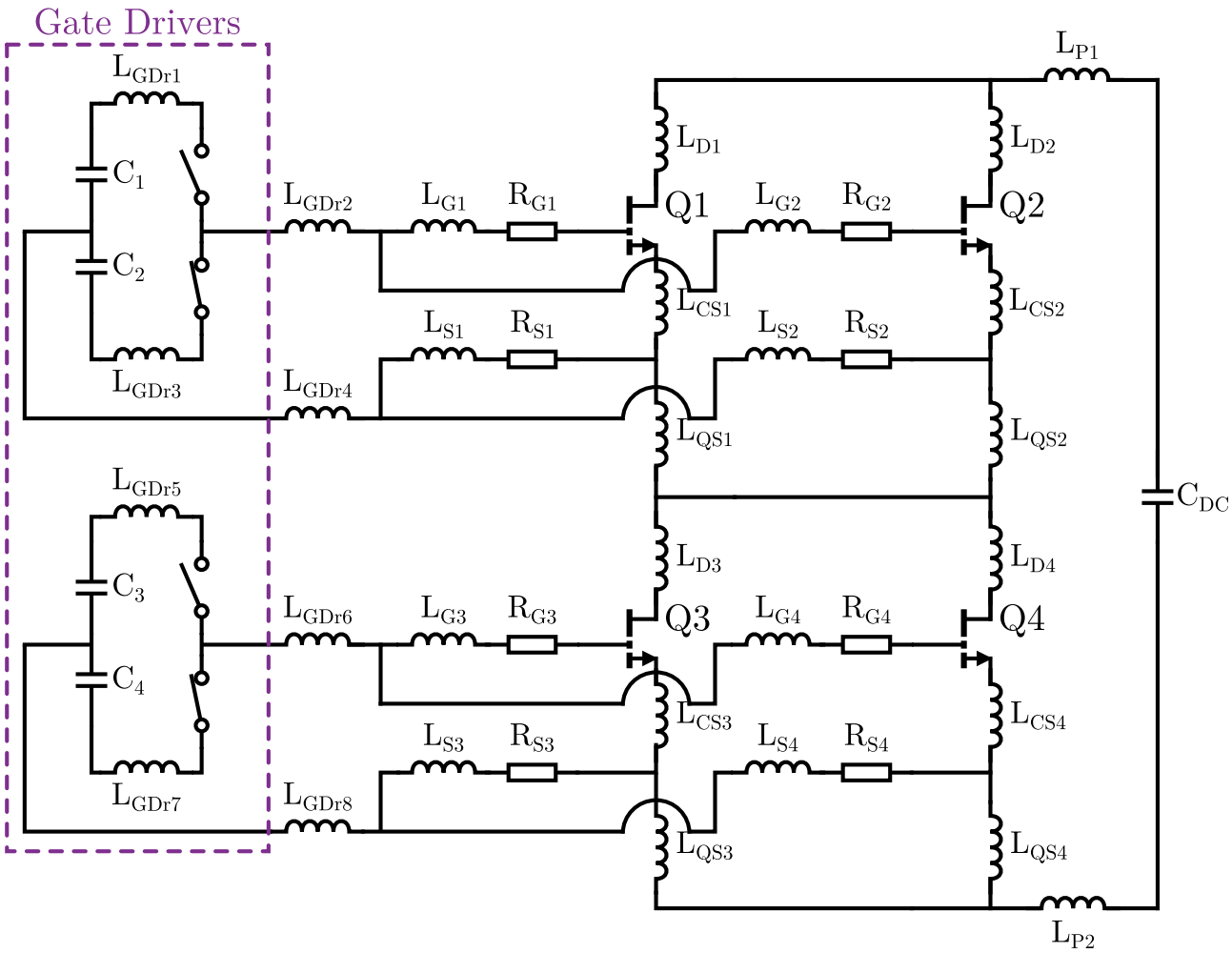


Figure 2.3: Schematic showing circuit of paralleled GaN HEMTs in a HB configuration. Parasitics with influence on performance are included.

This schematic shows the use of single output GDs with the possibility of negative turn-off voltage, i.e. bipolar GDs. Each GD is used to drive both devices in their respective position. This circuit could be extended by adding additional GaN HEMTs in parallel.

2.2.1 Explanation of Turn-On Behaviour

In order to get a better understanding of the issues regarding paralleling GaN HEMTs, the switching process will be explained, such that a clear idea of the influence of parasitics on the switching performance can be achieved. The turn-on process can be explained in four stages [15]. These are shown in Figure 2.4, where both the switching waveforms in the time domain are shown, as well as the I_{DS}/V_{DS} on the chart. These figures are generated using an LTspice circuit without parasitic components, showing the turn-on behaviour at 19 A with an inductive load for the GS66508T GaN e-HEMT from GaN Systems [23]. Important to note is that this simulation shows the switching of a single GaN e-HEMT, and is therefore not subject to the issues of paralleling devices. The simulation is only for demonstrative purposes. The junction temperature is kept at 25 °C to eliminate thermal effects on the performance. The on gate supply voltage is 6 V, and the off gate supply voltage is −3 V. A split output GD is used, with $R_{G,total} = 16.7\ \Omega$ in the turn-on loop, and $R_{G,total} = 2\ \Omega$ in the turn-off loop.

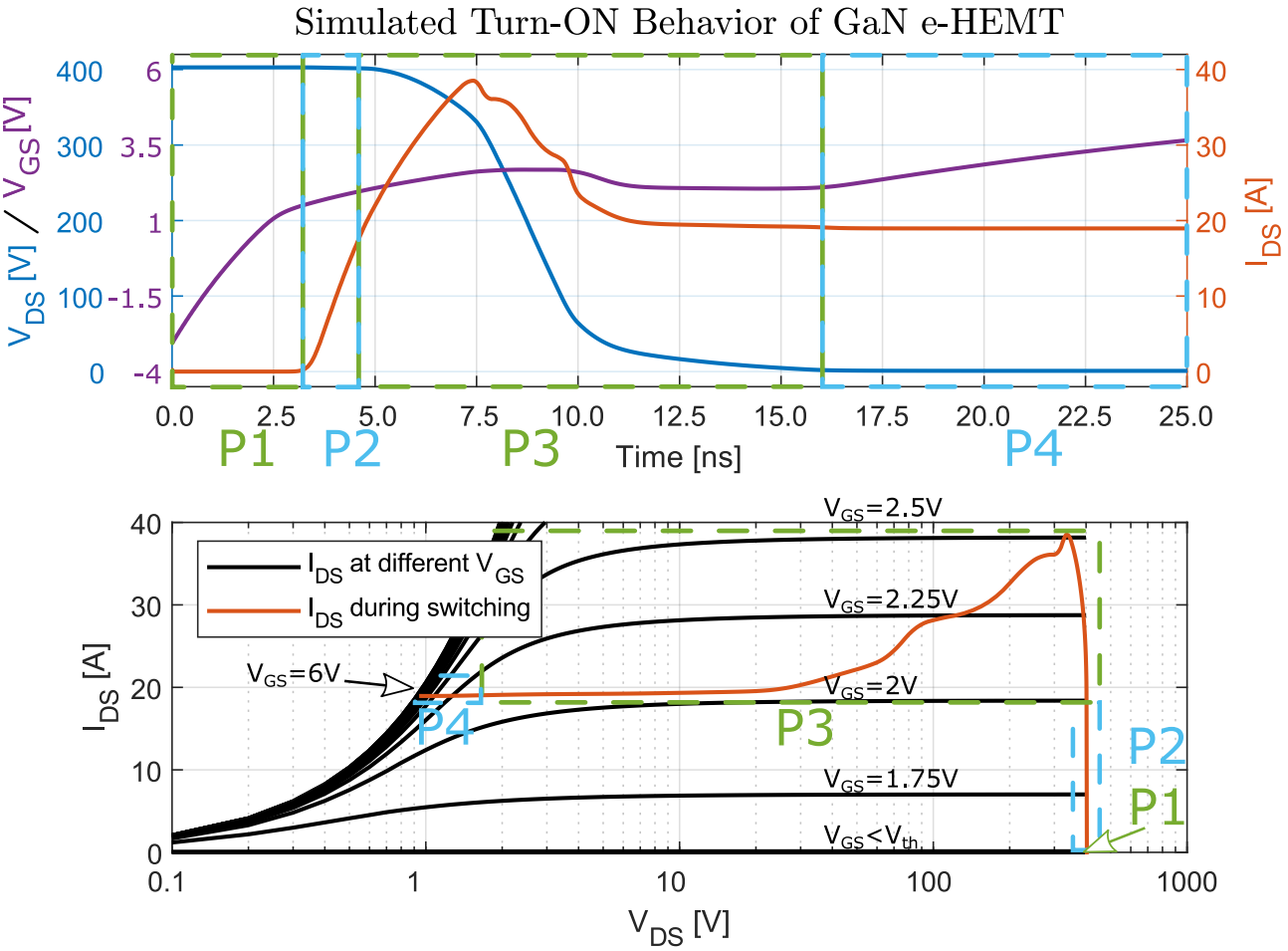


Figure 2.4: Turn-on behaviour of GaN e-HEMT in an LTspice simulation. Switching at $\approx 19A$.

Looking at Figure 2.4, it can be seen, that the turn-on behaviour is split into four stages, P1, P2, P3 and P4. These stages are explained in the following sections:

P1 - Delay Stage: P1 is the delay stage, where a gate-source voltage V_{GS} is applied to the GaN e-HEMT, but no current is flowing through the drain of the device. This period lasts until the gate-source

voltage V_{GS} of the device reaches the threshold voltage V_{th}, at which point the GaN e-HEMT will start to conduct. The GD loop circuit parameters determine the rate at which the input capacitance of the GaN e-HEMT is charged, i.e. the loop inductances and resistances, combined with the capacitance of the device, determine the time to charge up to the threshold voltage V_{th} of the e-HEMT. When turning on multiple paralleled GaN e-HEMTs with a single GD, as seen in Figure 2.5, deviations between the different gate loops will cause the input capacitors of the different devices to charge at different rates.

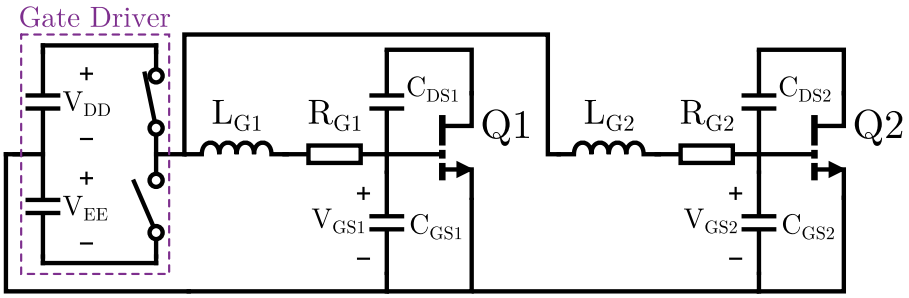


Figure 2.5: Equivalent circuit of GD loops of two GaN HEMTs in parallel. Parameters have been combined to simplify. Power loop is not included.

As the length of the two loops might not be the same, the inductances L_{G1} and L_{G2} can be different. This might cause devices to reach their threshold voltages V_{th} at different times, resulting in an imbalance of drain-source current I_{DS} sharing. For this reason, it is important to have symmetrical GD loops for each device, such that there is a minimal imbalance in the turn-on times of the devices. Another important factor in this stage is the specific threshold voltage V_{th} of each device, as these can vary from device to device [24]. As a result of this variance, it will be difficult to perfectly synchronise the switching of the devices, even with perfect circuit layout. Therefore the circuit design as a whole must be able to sustain some variation.

P2 - di/dt Stage: When the gate-source voltage V_{GS} of the GaN e-HEMT reaches the threshold voltage V_{th}, the device will start conducting. Looking at Figure 2.4, it can be seen that this occurs in the saturation stage, where the drain-source voltage V_{DS} will stay at a constant value, while the drain-source current I_{DS} and gate-source voltage V_{GS} rise. It can be seen that the drain-source voltage does not change until the current in the inductive load is reached by the device.

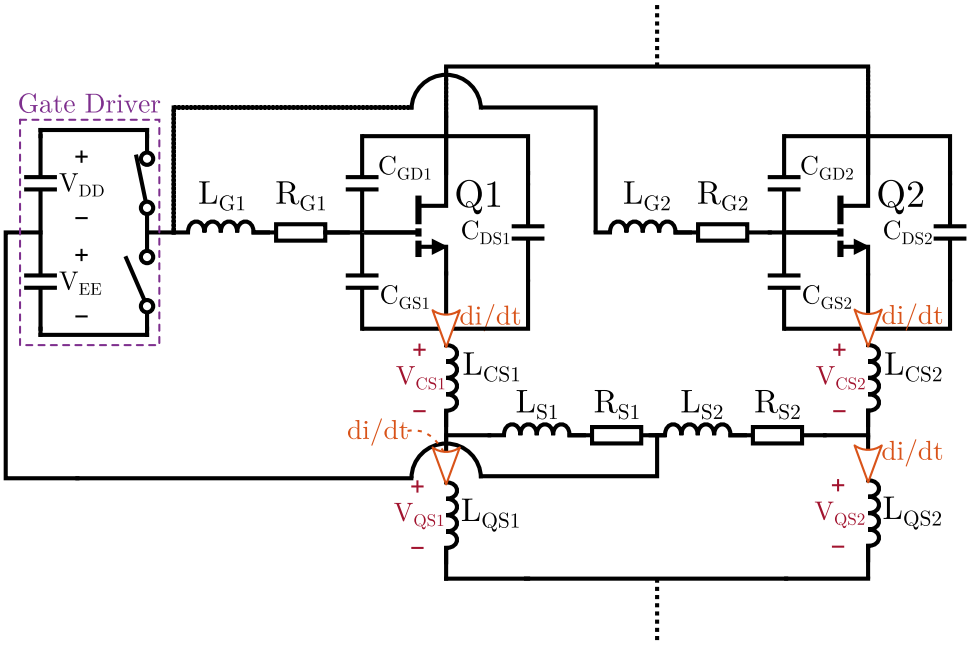


Figure 2.6: Simplified equivalent circuit of paralleled GaN e-HEMTs in the di/dt period.

As the gate loop and power loop share a common inductance in the source inductance of the device L_{CSx}, as seen in Figure 2.6, this inductance will start to have an influence on the gate-source voltage V_{GS}, as there is a high di/dt in this inductance when switching, resulting in a voltage drop V_{CSx}. As the gate is comparatively sensitive to disturbances, with a threshold voltage V_{th} in the low single digits, and a maximum gate-source voltage V_{GS} of 7 V in the case of GaN e-HEMTs from GaN Systems [23], this voltage drop V_{CSx} can have a significant influence on the performance and reliability of the device. This is because it is subtracted from the gate-source voltage V_{GS}, when referred to the GD voltage V_{DD}. In the case of a positive di/dt, as seen in Figure 2.6, this will reduce the effective voltage applied to the gate, slowing down switching times. When the gate-source voltage V_{GS} increases, the current through the device will increase as well, resulting in a di/dt over the inductance L_{CSx}. This causes a voltage drop to occur in the GD loop, causing the rate of change of the gate-source voltage V_{GS} to fall, slowing down the rise time [25]. This can have a considerable effect on parallel devices, resulting in an imbalance of current carrying in the transient [26]. Therefore, it is important to minimise this common inductance as much as possible by the use of a Kelvin connection. By creating a return path for the gate loop as close to the junction of the device as possible, the common inductance L_{CSx} between gate loop and power loop is minimised. Some devices have a dedicated Kelvin connection in the form of an additional lead [27], which is to be used as a gate return, while others include a small lead inductance [23], such that the circuit can be designed with this common inductance in mind, having a source return to the GD with as small a shared area with the power trace as possible. It should be noted, that in Figure 2.6, this common inductance is indicated as the lead inductance of the device. This common inductance will of course include trace inductances as well.

When paralleling these devices, the quasi-common-source inductances L_{QSx} also have a large impact on the switching behaviour and stability of the gate voltage. If the size of these inductances is not the same for the different devices, the source voltage of each device will differ, as there there will be different voltage drop over each of these inductances, if they are subject to the same di/dt. As each device is connected to the same GD, instability can occur, as there is a voltage drop over the source return impedances L_{Sx} & R_{Sx} of the devices. This will cause a current to flow across the source return

impedances of each device, resulting in an imbalanced voltage drop in each GD loop. I.e. one GD loop will have a positive voltage drop over its return impedances L_{Sx} & R_{Sx}, while the other will have a negative voltage drop over its return impedances. This will affect the current sharing capability of the paralleled devices, and may induce some oscillations.

Therefore, to equalise the current sharing of these devices, these quasi-common-source inductances L_{QSx} of the different devices should equal to each other, such that any voltage drop seen on a gate-source voltage, is mirrored by other devices, and the current is shared appropriately. Moreover, these inductances should generally be minimised as much as possible.

One other important circuit element to consider when designing circuits is mutual inductance between the gate drive loop and power loop M_x. The mutual inductance comes as a result of the inductive coupling between the GD loop inductance and power loop inductance. This mutual inductance is important to consider and minimise, as it will cause the high di/dt currents on the power loop to be induced into the GD loop, effectively causing the gate-source voltage V_{GS} to be influenced by the change in drain current through the device. This has the possibility of causing gate instability and oscillations, and affecting the switching times of the devices.

P3 - dv/dt Stage: Once the current through the device reaches the load inductor current level, the dv/dt period starts. At this point, the drain-source voltage V_{DS} can change, as the output capacitance C_{oss} can be discharged. This moves the device towards the active region of its performance. However, the discharging of the output capacitance C_{oss} causes a significant current to flow through the device, which can be seen in Figure 2.4, resulting in an overshoot in the drain-source current I_{DS}. This also causes the gate-source voltage V_{GS} to increase to the required level to accommodate this current overshoot. The Miller plateau can be observed, as the gate-source voltage V_{GS} stays at an almost constant value, whose magnitude depends on the drain-source current I_{DS}. This voltage is known as the plateau voltage V_{GP}. This plateau occurs as a result of the device being in the saturation region. While in this region, the gate-source voltage V_{GS} is determined by the load inductor current, and will therefore stay constant until out of the saturation region. Therefore, all of the current from the GD will flow into the gate-drain capacitance C_{GD}, effectively discharging it. By discharging C_{GD}, the drain-source voltage V_{DS} of the device will fall. It will discharge with a constant current, which is dependent on the plateau voltage V_{GP}, the GD voltage V_{DD} and the gate resistance R_G:

$$I_G = \frac{V_{DD} - V_{GS}}{R_G} \tag{2.2}$$

As mentioned, this V_{GS} will stay at a constant value V_{GP} in the Miller plateau region, resulting in a constant current through the gate. As this plateau voltage depends on the drain-source current I_{DS} through the device, at higher currents, the resulting gate current in the plateau region is lower. Therefore, the gate-drain capacitance C_{GD} will be discharged at a slower rate, resulting in slower switching times. This effect might be influential on paralleling performance, as parallel devices with unbalanced current sharing will have different plateau voltages V_{GP}, resulting in different gate currents in this stage.

As the di/dt of the device is lower in this stage, the effects of the inductances, intrinsic and parasitic are reduced. However, as the voltage over the device will change at a high rate, parasitic capacitances will start to have an influence on the switching performance. This has an influence on the circuit design, as parasitic capacitances between nodes of high dv/dt to each other will cause a current to flow. This is important to consider in various areas of the circuit. If a considerable parasitic

capacitance is present over the drain-source leads of the device, the switching behaviour might be altered. Moreover, this extra energy stored in the parasitic capacitance will be dissipated every switching period, increasing losses. This effect is important to consider as the switching frequency increases, as the rate at which this energy dissipation occurs will also increase, thereby resulting in higher power losses. This is especially important to consider when using devices such as GaN HEMTs, which offer increased switching frequency capabilities. In order to minimise these capacitances, the physical circuit layout must be carefully considered. The capacitance between two conductors is a function of their common area, and inversely proportional to the distance between them. Therefore, it is important to place conductors with high dv/dt to each other in an orientation, which minimises this plate-capacitor effect, if parasitic capacitance is unwanted. Thus, these conductors should not be placed on the immediate opposite side of the PCB, if these parasitic capacitances should be avoided.

P4 - Remaining Period: When the drain-source current I_{DS} and drain-source voltage V_{DS} have reached their final values, the gate-source voltage V_{GS} is again free to increase, as the device is moved out of the saturation region into the active region. C_{GS} will then continue to be charged, increasing the V_{GS} voltage, until it reaches the GD voltage V_{DD}.

2.2.2 Explanation of Turn-Off Behaviour

The turn-off sequence can also be analysed in four stages [15].

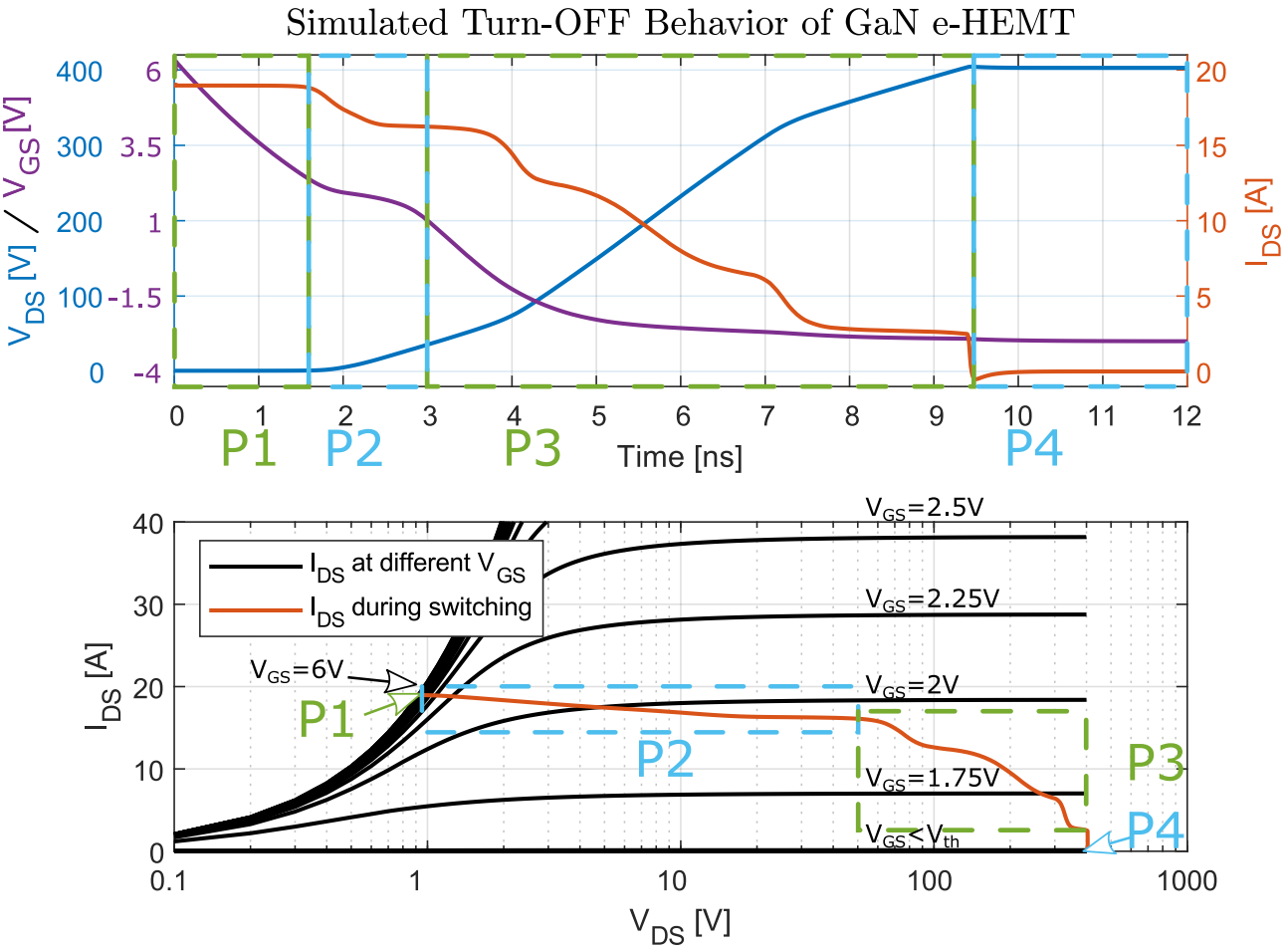


Figure 2.7: Turn-off behaviour of GaN e-HEMT in an LTspice simulation. Switching at $\approx 19A$.

P1 - Delay Period: Before the turn-off sequence begins, the input capacitance of the device C_{iss} would have been charged up to the GD voltage V_{DD}. This would place the device well into the active region of its function. Therefore, before a change in drain-source voltage V_{DS} occurs, the input capacitance C_{iss} has to be discharged until it leaves the saturation region. The time for this delay is dependent on the GD loop parameters. The explanation for this behaviour is similar to what was shown in P1 for the turn-on behaviour. The equivalent circuit with the relevant parameters can be seen in Figure 2.5. Again, an imbalance in the different GD loops will cause the gate-source voltages of the different devices to change at different rates. This could cause one device to exit the active region at an earlier point in time than others, causing an imbalance in current carrying capability. This further reiterates the need for symmetrical GD loop designs.

P2 - Plateau Period: When a sufficiently low gate-source voltage V_{GS} is reached, the GaN HEMT moves out of the active region, into the saturation region. A short plateau period is observed, as the gate-source voltage V_{GS} flattens out for a short time. This plateau voltage V_{GP} is determined by the amplitude of the drain-source current I_{DS}. As was shown in (2.2), the gate current I_G is dependent on the gate-source voltage V_{GS}. As a negative gate current I_G is required to turn off the device, a higher negative drain-source current I_{DS} will cause the device to turn off faster. This comes as a result of the higher saturation gate-source voltage V_{GS}, resulting in a higher gate current, thereby discharging the input capacitance C_{iss} quicker. Therefore, the device switching speed is dependent on the drain-source current I_{DS}. This might again have an influence in parallel circuits, as devices with different V_{GS} slew rates might conduct different amounts of current, causing an imbalance in current sharing.

P3 - di/dt & dv/dt Period: In this period, both the voltage and current have their highest rate of change. This is caused by the increased gate current I_G, as was explained previously. This increased rate of change in both current and voltage will have an increased effect on the parasitic disturbances in the circuit. As mentioned in the turn-on procedure, an imbalance in the parasitic trace inductances, shown in Figure 2.6, will cause some undesirable effects for paralleling applications, such as an imbalanced gate-source voltages as a result of imbalanced quasi-common-source inductances L_{QSx}, and imbalanced common source inductances L_{CSx}. As the turn-off procedure might cause higher di/dts to occur, these effects may be more pronounced compared to the turn-on period. These effects and their influence on the gate-source voltage V_{GS} stability can be partly negated by the use of a very low resistance in the turn-off loop of the GD, i.e. using different gate resistances for the turn-on and off loop. This does, however, limit the flexibility of choosing different slew rates for the turn-off procedure.

P4 - Remaining Period: After the switching is finished, there might be some ringings seen on the device. This is not seen in the simulation shown previously, as no parasitics were included in the simulation parameters.

2.2.3 Device Parameter Variation

Besides the circuit design having an influence on the paralleling performance of a module, parameter variations in the devices themselves also have an influence on the current sharing of the parallel devices. In [26], different SiC MOSFETs of the same model were parameterised, and the effects of combining devices with varying threshold voltages and on-resistances were investigated. This study showed that

these variations might cause the devices to sustain different amounts of current in the switching period, effectively straining one device more than the other. These effects would be expected to occur in GaN HEMTs in the same way, as GaN HEMTs also experience parameter variations [24][28, pp. 11-14]. However, due to the positive $R_{DS,on}$ temperature dependency, and the constant V_{th}, these variations seem to have a minimal effect on paralleling performance in regards to thermal performance [24], as an effective circuit was designed by randomly choosing GaN HEMTs from GaN Systems.

2.3 Design Priorities of Paralleled GaN HEMT Circuits

Based on this analysis, some design rules can be set up, such that a proper design, which exhibits good performance can be developed. These are in broad terms: symmetrical gate drive circuits and uniform loading of the devices [15][29][30]. More specifically, some priorities of the circuit design of paralleled GaN HEMTs can be laid out, where specific parts of the circuit seen in Figure 2.3 are considered. These priorities are as follows:

Primary Priorities		
Description	**Parameters**	**Design Rules**
Quasi-Common Source Inductance	L_{QSx}	Minimise, equalise across devices
Mutual Inductance between Gate and Power loop	M_x	Minimise, equalise across devices
Common Source Inductance	L_{CSx}	Minimise

Table 2.1: Primary priorities for circuit design of paralleled GaN HEMT circuit.

Secondary Priorities		
Description	**Parameters**	**Design Rules**
Power Loop Inductance	L_{Px},L_{Dx},L_{QSx}, L_{DLx}, L_{CSx}	Minimise
GD Loop Inductance	L_{GDrx}, L_{Gx}, L_{Sx}	Minimise, equalise across devices
Drain-Source Capacitance	C_{DS}	Minimise

Table 2.2: Secondary priorities for circuit design of paralleled GaN HEMT circuit.

As can be seen in Tables 2.1 and 2.2, both parasitic inductances and capacitances should be considered when designing an optimal circuit. However, some trade-offs may have to be made in these parameters, as they are somewhat inversely correlated. I.e. a more compressed circuit might allow for lower parasitic inductances, but might increase the parasitic capacitances.

The intrinsic inductances L_{SLx} and L_{DL1} can be reduced in the circuit by simply choosing different packages. Therefore, depending on the design requirements, some packages might be excluded for paralleling purposes. Therefore, a more in-depth comparison of GaN devices follows, to determine the optimal device for use in this configuration.

2.4 Comparison of GaN HEMT Devices

In order to determine the most suitable GaN HEMT, different devices will be compared for their applicability for usage in paralleling. These devices will be chosen based on the following parameters:

- A voltage rating of or above 400 V
- As low lead inductances as possible
- Low on-state resistance
- Good thermal properties
- Small intrinsic capacitances
- Normally-Off devices only

These parameters are based on the need for a high power rating in the HB switching module, low lead inductance, as mentioned in the previous section, to ensure as stable operation as possible in parallel and a device that can be cooled easily.

Based on the criteria of a low lead inductance, devices with large lead inductances such as those with TO-class packages will not be considered due to the large lead inductance in the legs of up to 10 nH. This is high compared to SMD packages with lead inductances below 1 nH [31][32]. Based on the remaining parameters the following devices, listed in Table 2.3, are considered.

Device Comparison								
Device	**V_{DS} [V]**	**I_{DS} [A]**	**$R_{DS,on}$ [mΩ]**	**Q_G [nC]**	**FoM**	**C_{iss} [pF]**	**C_{oss} [pF]**	**Package Cooling**
GaN Systems GS66508	650	30	50	6.1	305	242	65	Top/Bottom-Side
GaN Systems GS66516	650	60	25	14.2	355	518	126	Top/Bottom-Side
Infineon IGO60R070D1	600	31	70	5.8	406	380	72	Top/Bottom-Side
GaNPOWER GPI65060DFN	650	60	25	16	400	420	143	Bottom-Side

Table 2.3: Different GaN e-HEMTs considered for parallel operation. **Note:** Devices which have noted both top and bottom-side cooling have alternative product names for the top-side cooled versions. [23][27][33][34]

In order to compare the different devices, a Figure of Merit (FoM) calculation will be done by looking at the on-resistance and the typical gate charge. This will give a rough comparison of the conduction and switching losses for the devices. This is important in order to achieve a high power HB switching module as the lower the FoM the less heat needs to be dissipated. It is calculated by using:

$$FoM = R_{DS,on} \cdot Q_G \tag{2.3}$$

From this comparison it can be seen that the GaN Systems devices have the lowest FoM, with the GS66508 having the lowest FoM of 305. Based on the FoM, it is decided to narrow the comparison down to the two devices from GaN Systems.
The two devices were compared in another paper, in terms of switching energy at different drain-source currents, where two GS66508 were compared to one GS66516. It was seen that with the two GS66508 less energy was lost during the switching compared to the bigger GS66516 [9]. This could be advantageous, as this would allow the same power rating, but with less cooling. A practical matter is that this could lead to more devices needed with the GS66508 and as discussed previously a symmetrical layout can be difficult to achieve when increasing the number of devices.

2.5 Cooling of GaN HEMTs

Despite the good electrical properties of the GaN HEMT, it has been proven difficult to exploit their full potential [35]. Limitations in junction temperature and cooling bottlenecks are key challenges when operating GaN HEMTs at high powers. This section will investigate where the limitations are, and which cooling solutions exist to maximise the potential of the GaN HEMTs.

2.5.1 Thermal Limitations of GaN HEMTs

The thermal limitations of GaN HEMTs are not subject to lower allowed temperatures of the semiconductor material itself, since GaN has a maximum temperature of 700 °C, which is significantly higher than the maximum allowed temperature of e.g. Si, which is 300 °C [36]. However, the limitations due to the structure and size of the GaN HEMT can pose a challenge to dissipate the generated.

Intrinsic Limitations

There are thermal limitations intrinsic to the GaN HEMT, whose cross-section is presented in Figure 2.1 on page 3.

The 2DEG, which acts as the conducting channel limits the movement of electrons to a lateral direction. Joule-heating of electrons consequentially creates a thermal hot-spot in this layer, reaching a transistor heat flux numbers higher than the Sun's surface [37][38]. The generated heat has to be dissipated through the GaN HEMT, where amorphous inclusions and material disorders within the lattice, as well as the borders of the buffer layer govern the thermal resistance in the GaN material [39]. Additionally, GaN has a lower thermal conductivity (130 W/mK) compared to other WBG materials, such as SiC (490 W/mK), and similar to that of Si (130 W/mK) [37][39].

Size Limitations

Even though the thermal conductivity of GaN is comparable to Si, the small size of the thermal pads of GaN Systems devices, reduce the ability to dissipate heat. Compared to a TO-247 package usually used for discrete power devices, their thermal pad areas might be an order of magnitude smaller. This is seen in Figure 2.8.

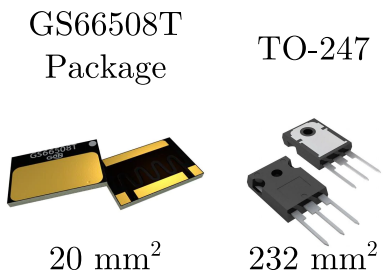


Figure 2.8: Comparison of GaN Systems 30A top cooled GaN e-HEMT and TO-247 package thermal pad areas. [23][40][41]

Small packages are necessary to minimise stray inductance to allow for high frequency switching. With smaller packages, the area through which the heat is dissipated is reduced significantly, which results in a higher thermal resistance [40], as seen in:

$$R_\theta = \frac{l}{k \cdot A} \tag{2.4}$$

Where l is the length of material the heat is dissipated through, k is the thermal conductivity, and A is the surface area. The relationship between temperature, power, and thermal resistance is given by:

$$T = P \cdot R_\theta \tag{2.5}$$

This makes it challenging to stay below the Safe Operating Area (SOA) of the junction temperature when operating at high power [35].

2.5.2 Thermal Pad

Generally, there are two options for the location of the thermal pad of an SMD. It can either be located at the bottom or on top of the SMD component. Top cooled devices allow for a cooling approach, as seen in Figure 2.9, where the TIM and the heat sink are mounted on top of the device and form the thermal conduction path. However, the small size of the thermal pad can lead to high thermal resistances of the TIM. Apart from extracting the heat through the thermal pad on top, heat is also dissipated through the drain and source pads on the bottom of the device. Typical values of thermal resistance from the junction to the board lie between 3-7 K/W for GaN Systems devices [42].

Bottom cooled devices dissipate most of the heat through the PCB as seen in Figure 2.11 on page 18. This requires the PCB to be utilised to spread the heat in the lateral direction. This adds the thermal resistance of the PCB to the thermal equivalent circuit, but also increases the contact area of the TIM, which can reduce the thermal resistance inflicted by it.

However, it needs to be carefully evaluated whether the trace connected to the thermal pad terminal can be exploited efficiently to spread and dissipate the heat without compromising the electrical performance of the circuit. As the thermal pad is often electrically connected to either the source or the drain terminal, its voltage can vary significantly in a HB configuration. If a larger area is connected to this high dv/dt node, capacitive coupling can cause performance issues.

2.5.3 Top Cooled Solutions

Most top cooled solutions include a cooling system with three main components, as seen in Figure 2.9

- A transistor, from where the heat is to be extracted through a thermal pad, which is typically electrically connected to either the drain or the source terminal of the transistor.
- A gap filler or Thermal Interface Material (TIM) which ensures thermal conduction to the heat sink and can provide electrical insulation if needed.
- A heat sink, which increases the surface area through which heat can be dissipated to the ambient air through either natural or forced convection.

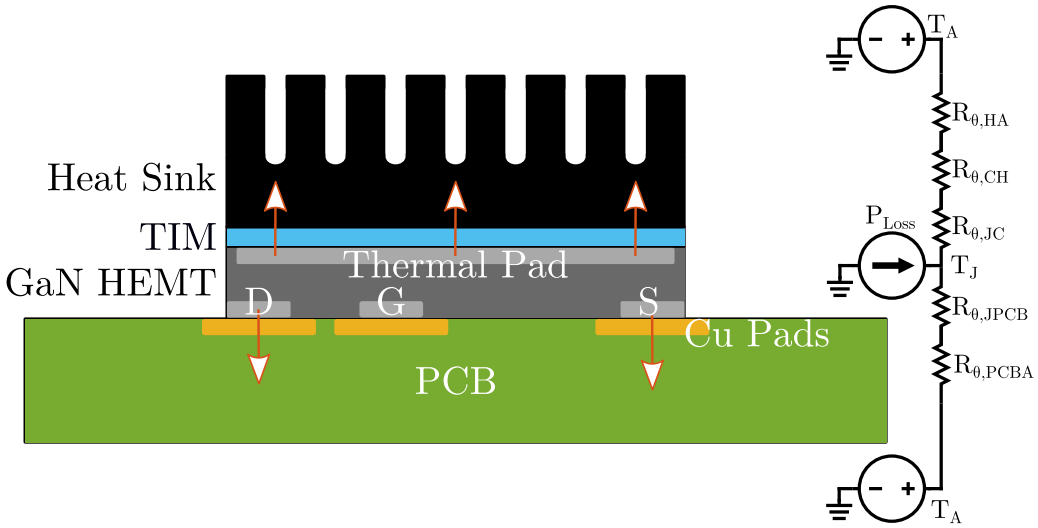


Figure 2.9: Schematic of top cooled solution with equivalent thermal circuit. Objects not to scale.

Figure 2.9 shows a schematic of a top cooled system and its equivalent thermal circuit. Dissipated power is represented with a current source, the ambient temperature with a constant voltage source, and the thermal resistances are represented by resistors. The GaN HEMT is shown in grey, including the thermal pad and the drain, gate, and source terminal. The heat flow is represented with orange arrows and is dissipated upwards from the junction to the thermal pad ($R_{\theta,JC}$) through the TIM in blue ($R_{\theta,CH}$) and the heat sink in black, from where it is dissipated by natural or forced convection ($R_{\theta,HA}$) into the ambient air. Through the drain and source pads, the heat is dissipated towards the bottom to the PCB ($R_{\theta,JPCB}$) from where it is dissipated into the ambient air ($R_{\theta,PCBA}$).

These approaches are widely used solutions for GaN HEMTs, but have a set of limitations [31][35][40]. Namely, the TIM can result in a thermal bottleneck due to the comparably small size of the thermal pad of the GaN HEMT, which results in a limitation of the power that can be dissipated. Moreover, the small package height of the GaN HEMTs may cause clearance issues with components close to the device, as the heatsink will be physically close to the PCB surface. This can be alleviated by the use of a pedestal heatsink, which extends down to the PCB, with a small extrusion [43].

Thermal Interface Material

To counteract the bottleneck posed by the size of the thermal pad, it is important to choose a TIM with a minimal thermal impedance, i.e. a high thermal conductivity.

There are many types of TIMs, both electrically isolating and conductive materials. In this section they will be compared according to their thermal impedance [Kcm^2/W] and the respective breakdown voltage.

Different studies examining cooling solutions for high power GaN HEMT applications were analysed to characterise the performance of different TIMs. The examined materials include various silicone sheets, ceramic base materials, an adhesive TIM, a phase change material and thermal insulating gels [31][40][44]. Figure 2.10 shows the thermal impedance of the different TIMs as well as the breakdown voltage.

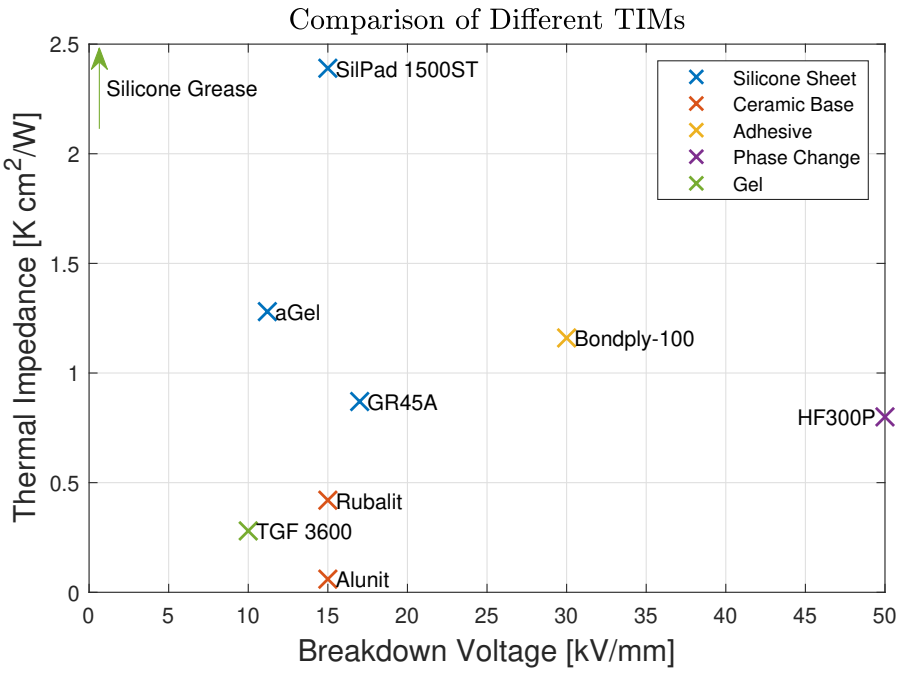


Figure 2.10: Comparison of thermal impedance and breakdown voltage of different TIMs. **Note:** The thermal impedance of silicone grease is 8.65 Kcm^2/W.

It can be seen that the ceramic base TIMs generally exhibit the lowest thermal impedance compared to phase-change materials and silicone sheets. Silicone sheets cover a larger span of thermal impedances, where some high quality silicone sheets can compete with the examined phase-change material.

Compared to other materials, Alunit, which exhibits the lowest thermal impedance, is the most expensive by a large margin, which can make it a less desired choice if the price is a priority [40].

An additional aspect to consider for the TIM is whether it is electrically insulating or not. As either the source or the drain terminal of the GaN HEMT is connected to the thermal pad, electrical insulation is required when GaN HEMTs with different source potentials are connected to the same heat sink to avoid short-circuits. If no electrical insulation is provided by the TIM, the heat sink will have the potential of the source terminal of the GaN HEMT, which in HB configurations can vary significantly within nanoseconds. This can lead to EMI issues and capacitive coupling with the PCB.

In Figure 2.10, the phase change material shows the highest break down voltage at 50 kV/mm. Most TIMs exhibit a breakdown voltage in the range of 10-20 kV/mm.

Heat Sink

Heat sinks are used to dissipate the heat to the ambient air by natural or forced convection as well as by radiation. In [31], a square pin, cylindrical pin, and finned heat sink were compared. The finned heat sink exhibited the lowest thermal resistance of the three. By adding forced convection, the thermal resistance could be cut more than in half.

By using a push-pin heat sink, the heat sink can be attached to the TIM with increased pressure, increasing the thermal conductivity. The pressure can be adjusted, but it can be distributed unevenly, as the applied force is higher in the corners of the heat sink compared to the middle. QSZ clips can be

used as an alternative as they allow the pressure to be distributed evenly. Their disadvantage however is that the PCB can experience warpage due to the applied force [44].

2.5.4 Bottom Cooled Solutions

With bottom cooled packages, the heat can be dissipated and spread through the PCB, as shown in Figure 2.11.

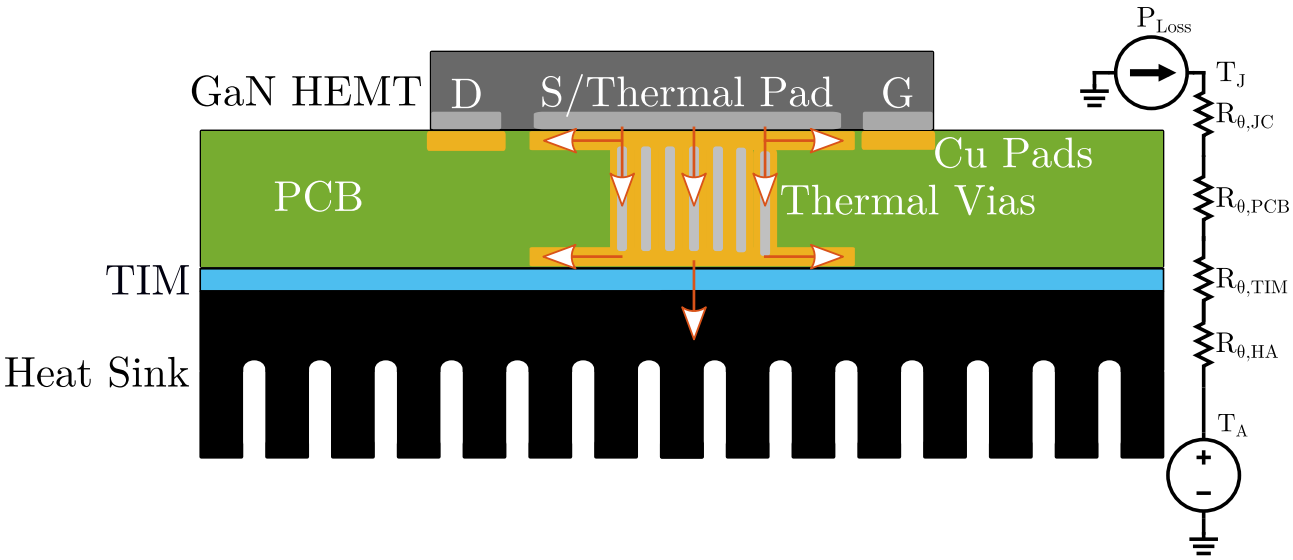


Figure 2.11: Schematic of the heat spreading in a bottom cooled system with equivalent thermal circuit. Objects not to scale.

Figure 2.11 shows an example of a bottom cooled PCB, with the GaN HEMT indicated in grey, the PCB in green, the copper pads and traces in yellow, the TIM in blue, and the heat sink in black. Thermal vias are used to conduct the heat, represented by orange arrows, away from the thermal pad through the PCB.

To decrease the thermal resistance of the PCB, the solder mask of the entire trace connected to the thermal pad can be removed. Furthermore, the area of the bottom copper layer can be increased in order to provide a bigger area of contact with the TIM, which lowers the thermal resistance of the TIM significantly. Additionally, the solder mask can be removed at the bottom layer as well. To further increase the thermal conductivity of the copper, the thickness of the copper layer can be increased. [44]

By increasing the copper area which is electrically connected to either the source or the drain potential, there is an increased risk of unwanted capacitive coupling between different nodes. To counteract this issue, thermal jumpers can be implemented. Thermal jumpers are electrically insulating, thermally conductive, and have a low capacitance. They can be used to allow heat flow to larger planes, e.g. ground planes, in order to keep high dv/dt traces as small as possible. [45]

Thermal Vias

Conventional PCBs use FR4 epoxy, which has a relatively low thermal conductivity of 0.3 W/mK [40]. To increase the thermal conductivity between layers, thermal vias can be used to channel the heat, as shown in Figure 2.11.

The thermal resistance of one thermal via can be calculated as [44]:

$$R_{\theta,via} = \frac{l_{via}}{k_{Cu} \cdot A_{via}} \tag{2.6}$$

Where l_{via} is the length of the via, given by the thickness of the PCB, k_{Cu} is the thermal conductivity of copper, which is 401 W/mK, and A_{via} is the cross-sectional area of the plated copper wall of the via.

The cross-sectional area of the plated copper wall of the via, through which the heat is conducted is given by (2.7).

$$A_{via} = \pi \cdot (d_{via} + w_{wall}) \cdot w_{wall} \tag{2.7}$$

Where d_{via} is the diameter of the whole of the via, and w_{wall} is the width of the copper plated wall, which is typically 25 µm [44].

By adding more thermal vias in parallel, the thermal resistance can be reduced significantly. Additionally, the conductive area can be increased by increasing the thickness of the plated via wall, or filling the via with copper entirely. However, this comes with an increased cost.

Alternative substrates to FR4

As mentioned, the thermal conductivity of the typically used FR4 epoxy in PCBs is very low at 0.3 W/mK. Different substrates such as Direct Bonded Copper (DBC), normally used in power modules, or Insulated Metal Substrate (IMS) can reduce the total thermal resistance significantly [40][46].

DBC consists of a copper top layer, and a ceramic isolator. The high thermal conductivity of 26 W/mK of the ceramic isolator Al oxide results in a superior thermal performance of the DBC substrate. However, the design flexibility is reduced and magnetic flux cancelling is not easily realised in DBC, which can cause issues with parasitic components [46]. Therefore, DBC is not considered further.

IMS consists, similarly to the DBC, of a copper top layer, a dielectric layer and a metal base, usually made of Al. This metal base has an excellent thermal conductivity of 238 W/mK and helps to dissipate the heat. Depending on the dielectric material, the thermal conductivity of IMS ranges from 3-7 W/mK [46]. The design flexibility is higher than DBC and it allows for flux cancellation, making it an attractive solution to dissipate heat efficiently.

In [46], PCB, DBC, and IMS configurations were compared, and it was shown that a DBC could reduce the junction-to-heatsink thermal resistance by 80% in respect to a PCB, while the thermal resistance was reduced by 70% by using IMS compared to PCB, which makes IMS a very promising solution for high power applications.

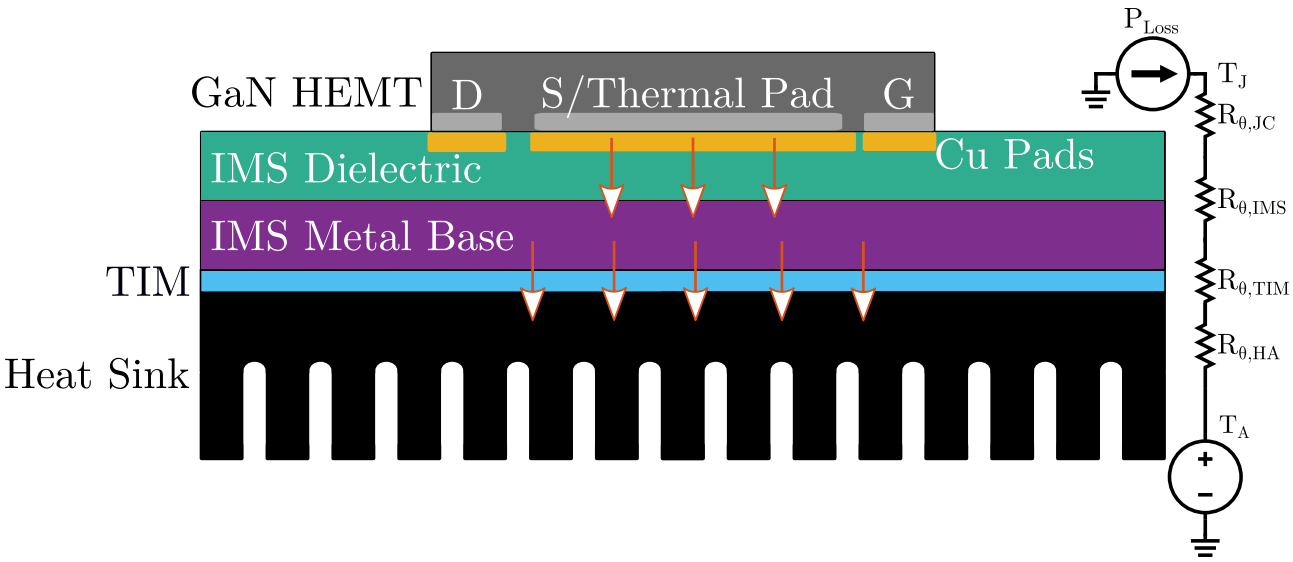


Figure 2.12: Schematic of the heat spreading in a bottom cooled system with IMS instead of conventional PCB, and its equivalent thermal circuit. Objects not to scale.

Figure 2.12 shows a schematic of a bottom cooled system using an IMS. The GaN HEMT is depicted in grey, the conducting copper layers in yellow, the dielectric layer of the IMS in turquoise and the metal base, which allows for an increased thermal performance, in purple.

The metal base of the IMS provides a low thermal resistance path for the heat to be dissipated, resulting in the superior thermal properties of IMS. However, IMS often only uses a single layer of conductors, limiting the design possibilities. Therefore, only the power stage is usually implemented on an IMS board, while the driver circuitry is placed on a separate, conventional PCB [43][47]. This makes the circuit design more complex, results in more parasitic content in the circuit, and reduces the possibility to implement flux cancellation.

2.5.5 Comparison of Cooling Solutions

To examine which cooling solution provides the lowest thermal resistance, cooling solutions in various studies have been analysed regarding the achieved thermal resistance. Top cooled PCB, bottom cooled PCB, and IMS solutions are compared in Figure 2.13. To make a fair comparison, the area of the thermal pad of the GaN HEMT has been considered as well, by multiplying it with the total thermal resistance of the system. This results in the thermal FoM presented in Figure 2.13

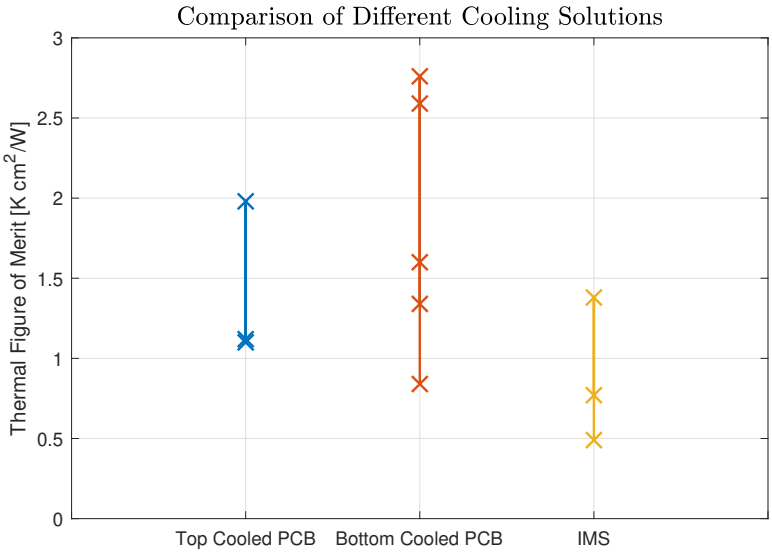


Figure 2.13: Comparison of the thermal FoM of different cooling solutions. [35, 43, 44, 46–48]

It can be seen that similar performance can be achieved for top and bottom cooled PCB solutions. However, bottom cooled solutions show a broader range, both including lower and higher thermal FoM compared to top cooled solutions.

However, since the thermal resistance of the TIM becomes the limiting factor in cooling solutions for both top and bottom cooled devices, increasing the contact area of the TIM is crucial, and this is efficiently achieved with bottom cooled solutions [35].

IMS solutions appear to have the highest potential in dissipating heat efficiently. With the electrical limitations of IMS, top and bottom cooled devices on FR4 can provide an adequate compromise between electrical flexibility and heat dissipation ability.

In this chapter it was seen that great care had to be taken into the design of the circuitry for the parallel GaN HEMTs to ensure a symmetrical design and minimise specific inductances. Through a comparison of different GaN HEMT devices, it was determined that either the GaN systems GS66508 or GS66516 would be the best choice. This was determined by looking at the FoM for on-resistance and typical gate charge, where the two devices yielded the lowest scores.
As both of these devices had a version with either top or bottom cooling, an analysis was performed on cooling solutions for both types. Different TIM materials were compared in regards to their thermal impedance and breakdown voltage, such that an overview of their performances could be clarified. This will be used in the design process in order to optimise thermal performance. Lastly, different cooling solutions with different substrate materials were compared. FR4 was analysed with top and bottom cooled devices, and IMS was analysed with bottom cooled devices. It was found that the IMS could achieve superior cooling performance compared to FR4, but posed additional challenges in the electrical design.

Chapter 3

Research Question

Based on Chapter 1 and 2 the following research question for this project has been formulated:

"How can a GaN HEMT based HB switching module with four GaN HEMTs in parallel be designed and optimised using a digital design process, and how can the digital design process be expanded upon to improve its capabilities?"

3.1 Method

This section will go over the methods used in this project, in order to answer the previously presented research question.

In order to answer the first part of the research question: *"How can a GaN HEMT based HB switching module with four GaN HEMTs in parallel be designed and optimised using a digital design process"*, the operation and design of a parallel GaN HEMT HB must be investigated further. In Chapter 5, the design of different circuit elements will be investigated. Firstly, the GD of the HB will be analysed and designed. This includes choice of components, and component sizing. Moreover, an analysis of different circuit vulnerabilities will be performed, and ways to alleviate these vulnerabilities will be presented. Then, to get a better grasp on the origins of parasitic components, these will be investigated, such that effective circuit designs can be conceived. In Chapter 6, three different HB designs will be presented, and their inductive parasitic content will be compared. These three designs will have different amounts of parasitic content, in different areas of the circuit. By analysing the performance of these different circuits, a correlation between the different parasitics and their influence on the performance can be achieved. Moreover, this will also be used to evaluate the design criteria presented in Section 2.2 on page 5. These three different designs will be evaluated both by simulation and by physical prototypes. By using the Finite Element Analysis (FEA) software Ansys Q3D, LTspice circuits, which accurately portray the circuit behaviour are generated. In the LTspice circuits, non-linearities of the devices, which would not be included in simplified equations, are included. This increases the accuracy of performance predictions, compared to previous methods. The LTspice circuits allow for a digital prototyping process, where several designs can be tested and evaluated, without the need for physical prototypes. By building physical prototypes, and comparing these with their digital counterparts, the accuracy of the digital models can be evaluated.

In order to answer the second part of the research question: *"How can the digital design process be expanded upon to improve its capabilities?"*, a deeper look into the digital design process is needed. The digital design process described by previous papers [49][50][51][52], will be examined briefly. In Chapter 4, an analysis of the digital design process and the different tools used will be given. At first the different phases and tools involved in the digital process will be shown to show the needed steps, to showcase how this process can be an advantage compared to other design processes. A process of extracting the parasitic parameters with Ansys Q3D will be proposed, in which the process of parameter extraction is automatised using a Matlab script, which analyses the raw data from Ansys

Q3D, in order to extract relevant data. This aims to improve the efficiency of parameter extraction compared to previous methods [50], allowing for quicker turn-over time, and better analyses.

In this project, a novel method of component sizing is proposed, utilising the concepts of digital design. By being able to accurately simulate circuit performance, components can be tested digitally at a rapid pace. By running the non-linear LTspice circuit models using a Matlab script, a number of these simulations can be executed, evaluating a large amount of components. Then, by evaluating the performance of the components digitally, optimisation theory can be applied, such that the optimal component choice is achieved. The application of this method is presented in Chapter 8, where the method will be applied in order to find the optimal combination of gate resistors, comparing different evaluation parameters such as power loss and switching speeds. Moreover, the method will be used to compare the performance of different ferrite beads, used to dampen oscillations on the gate.

3.2 Delimitations

- The GS66508T was chosen due to its easy availability from mainstream vendors and low FoM compared to the GS66516.
- It was chosen to use 4-layer PCB for the three designs in this project as this was deemed to be a good compromise between cost and needed degrees of freedom in terms of route the compact design. Moreover, this configuration proved to be more easily available in terms of production and shipping times.
- Frequency dependent parasitics are not considered in the FEA and LTspice models.
- The decoupling capacitors used in this project was chosen based on prior experience [50].
- The main focus of the project will be on the electrical performance of the HB switching module with a Double Pulse Test (DPT), meaning that no practical thermal solutions will be implemented.

Chapter 4

Digital Design

In this chapter the digital design process and the methods used will be explained in order to clarify their functions.
At first the different phases and tools of the digital design process will be explained in order to clarify the process. The electrical FEA software Ansys Q3D is used to estimate the parasitics of a given electrical circuit. To get a better understanding of this, the process of using the software will be explained. In order to improve the capabilities of this process, a new method of data processing the Ansys Q3D results is presented.
The data from Ansys Q3D are then implemented in an LTspice model, which can simulate system performance with high accuracy.
Finally, the optimisation parameters and theory used in the digital design process will be explained to give a clear indication on how the components selected for optimisation are chosen.

4.1 Digital Design Process

With the advent of new semiconductor devices utilising WBG materials such as SiC and GaN, quicker switching times can be achieved. However, this requires increased consideration of parasitic electrical components, as these have an increasing impact on circuit performance, at higher switching speeds. In order to quantify the impact of these parasitics, digital design, in the form of FEA, can be used to predict their size and contribution the the circuit behaviours. This can be done entirely digitally, such that the circuit dynamics can be predicted without the use of physical prototypes. [49][50][51][52] A general overview of the digital design process used in this project is illustrated in Figure 4.1.

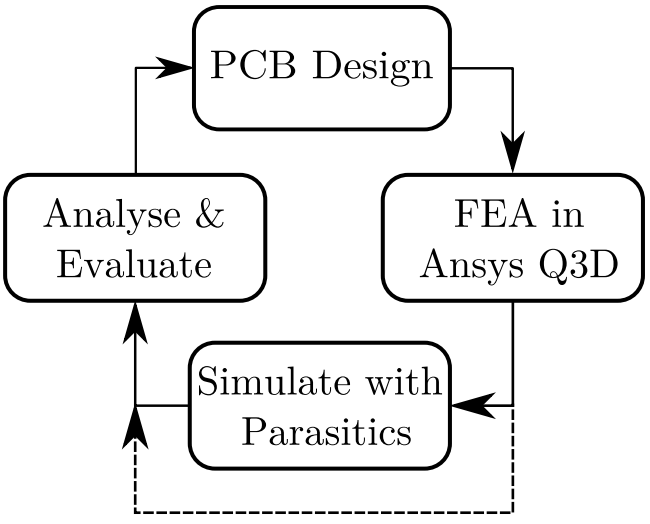


Figure 4.1: Flowchart of the digital design process. [50]

The process is divided into four phases, starting with the design phase of the PCB. The electrical schematic is realised in a PCB layout, and the components and their connections are carefully placed while considering parasitic components. When a design is ready in Altium Designer, it is exported in the format IPC-2581 and imported into Ansys SIwave. As Ansys Q3D cannot use the exported

PCB file from Altium Designer directly, it must be converted in Ansys SIwave into an .aedt file; a proprietary Ansys fileformat, which can be opened by Ansys Q3D. With Ansys Q3D the parasitic parameters can be extracted from the PCB design by applying FEA which is explained in detail in the following sections. The extracted data can be implemented in an LTspice model of the PCB and evaluated based on the desired evaluation parameters. The efficacy of the PCB can also be evaluated numerically, measuring the inductance values, and comparing between different designs. With these results the design can be reevaluated and altered without needing to perform any physical tests which can increase the number of design iterations can be made during a time-limited design process.

4.2 Ansys Q3D Simulation

The FEA software used in this project for extracting parasitic components from PCBs is Ansys Q3D. After importing the 3D model of the PCB and its traces into Ansys Q3D, one has to define the relevant nets and terminals. A net is defined as the sum of conductors, which are physically connected. The terminals are where components are connected to the nets, e.g. the pads of SMD components, plugs and legs of through-hole components. For the simulation, the terminals have to be defined as either a sink or a source. These designations are used to calculate the resistance and inductance values of the given net. On any net, only one sink can be defined, but multiple sources can be defined. All the resistance and inductance values are then found in the trace from the sink to each source. I.e. every source terminal has a self inductance and resistance. All the self-resistances are then mutually coupled by some value to every other self-resistance on the net, and all the self-inductances are mutually coupled to every other self-inductance on the PCB. Moreover, Ansys Q3D calculates a capacitance value between each of the nets.

For the scope of this project, focus has been placed on the parasitic inductance, above the other parasitic components. It was deemed, that the parasitic inductances have a larger influence on system dynamics, than the other parasitics, as mentioned in Section 2.3. Therefore, this section and the following analysis of this report, are primarily based on the parasitic inductances. However, to get a better idea of the actual circuit dynamics, and to be able to get a superior numerical analysis, the capacitances and resistances could also be considered. However, it should be noted that for the LTspice simulations, these parasitics are included, and are therefore influential on the circuit dynamics.

To get a better understanding of how these parameters are defined in Ansys Q3D, a small example has been created: In Figure 4.2 an example PCB is shown, which is composed of a two layer PCB, with one net on each side of the PCB. On each net, one sink is defined, along with two source terminals.

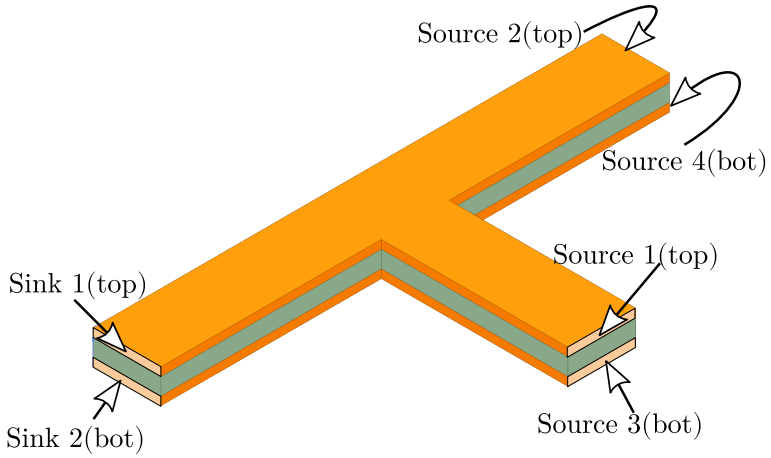


Figure 4.2: Example circuit made in Ansys Q3D, with two nets, each having one sink and two sources. The orange layers represent copper, while the green layer represents FR4.

The inductances in this circuit are defined as seen in Figure 4.3.

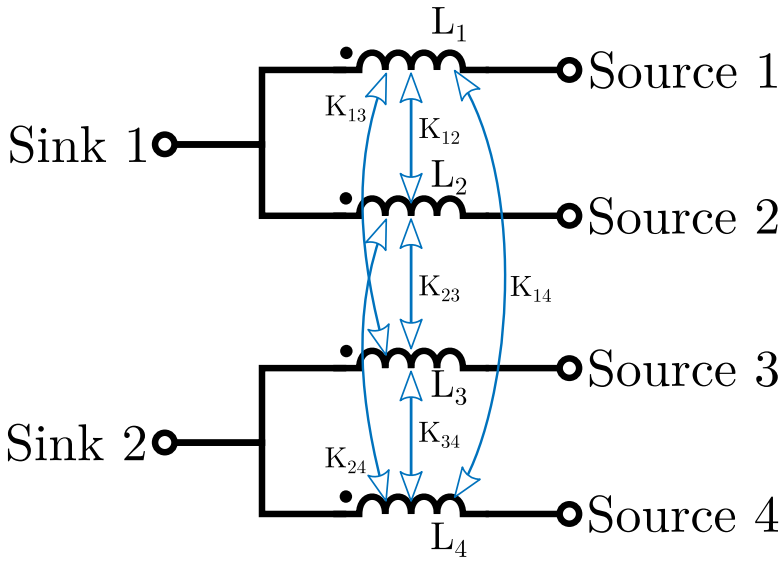


Figure 4.3: Circuit schematic showing the inductance definitions of example circuit.

Where the coupling coefficient K_{12} is related to the mutual inductance M_{12} as follows:

$$M_{12} = K_{12}\sqrt{L_1 \cdot L_2} \tag{4.1}$$

Figure 4.3 shows a simplified circuit model of the example circuit shown in Figure 4.2. It can be seen that the two nets with two sources in each, results in four different self-inductance values, all being coupled to each other. These inductances can be expressed in a matrix form as seen in Table 4.1.

	N1, S1	**N1, S2**	**N2,S3**	**N2,S4**
N1, S1	L_1	M_{12}	M_{13}	M_{14}
N1, S2	M_{12}	L_2	M_{23}	M_{24}
N2, S3	M_{13}	M_{23}	L_3	M_{34}
N2, S4	M_{14}	M_{24}	M_{34}	L_4

Table 4.1: Inductance matrix of Figure 4.3. N refers to Net number, S refers to source number.

Where each source will have its own self-inductance from its corresponding sink terminal. Then, each self-inductance is coupled magnetically, as defined by the the mutual inductance. This will be elaborated upon in Section 4.2.2 .

Moreover, the resistances and capacitive couplings can also be found. In order to simplify the demonstration, some details have been omitted from Figure 4.4.

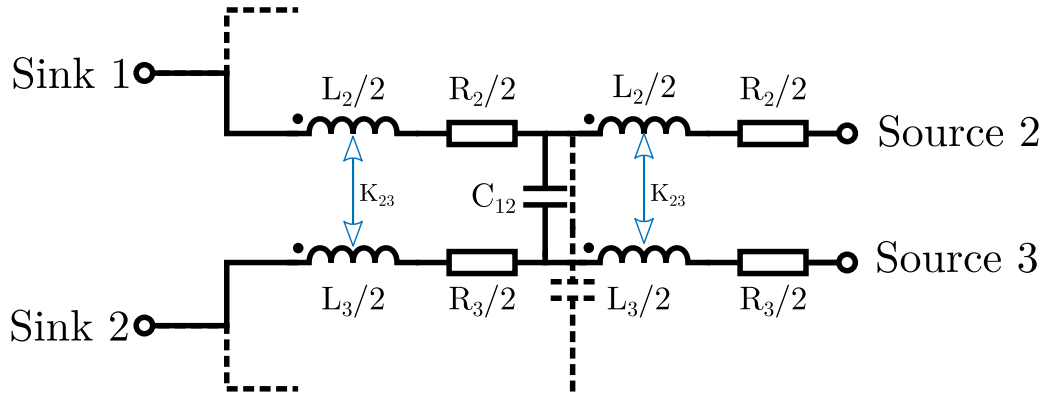


Figure 4.4: Circuit schematic showing how the resistance and capacitances are connected in the Ansys Q3D simulation. Only the capacitive coupling between Source 2 and Source 3 are included. Others have been excluded for simplicity.

As can be seen in Figure 4.4 the inductance has been split into two equal parts. The parasitic resistance is also shown, also divided into two equal parts. In between these parasitics, the parasitic capacitance is connected. The FEA software finds a capacitive coupling between each net, and couples this capacitance, by splitting the inductances and resistances, and connecting to this midpoint. [51]

While the data found from Ansys Q3D can be directly implemented in an LTspice simulation, which will be explained in Section 4.3, the values seen in the matrices are difficult to intuitively understand, as one cannot inherently determine the inductance between two source terminals, only the self-inductances of each source terminals and their mutual coupling to others. For example, looking at Figure 4.3, it is difficult to intuitively determine the inductance between Source 1 and Source 2, given the data which Ansys Q3D extracts from the PCB. Therefore, in order to numerically evaluate the circuit, additional analysis has to be performed.

4.2.1 Manual Extraction of Parasitics

One way to get a better understanding of the individual inductances, is to simulate an isolated portion of the PCB, looking only at a specific trace path, thereby extracting only a certain inductance value. I.e. defining only one sink and one source per net, and looking at the self-inductance of the trace between these two terminals. This gives an intuitive understanding of inductance values of this specific trace. Moreover, this idea can be extended to find loop inductances, where the effects of flux cancellation are also considered. By connecting several sink-source combinations in series, using the "reduce matrix" function in Ansys Q3D, a current path through several of these traces can be found, and a total loop inductance can be determined. This is relevant for calculating the critical loops such as the different GD loops, as well as the power loops between the GaN devices and decoupling capacitors, as these loops take advantage of the loop inductance reducing effects of flux cancellation, as explained in Section 5.3.3.

The disadvantage of this procedure, is that for every measurement which is desired, a new simulation has to be setup, the terminals have to be defined, and an FEA analysis has to be run. While the procedure may be reasonable to perform for simple circuits, the time required quickly adds up when considering more complex circuits with more relevant loops, such as in the parallel GaN circuit in this project. For example, each GaN HEMT has two GD loops, the turn-on and turn-off loops. In order to achieve good switching performance, there must be good symmetry between the loops of different devices. With eight GaN HEMTs in total, this results in 16 different loops to analyse. Moreover, there are four critical power loops between the GaN HEMTs and their respective decoupling capacitors. Also, if specific inductances values are to be analysed, e.g. the source inductances of different devices, a simulation has to be run for each of these.

Therefore, an easier and quicker solution to extract these parasitics for numerical analysis is required.

4.2.2 Automatic Extraction of Parasitics

In order to numerically analyse a given PCB design, some specific parameter values have to be able to be extracted:

- Inductance values between two given terminals on the PCB
- Loop inductance values, with and without cancellation effects

To achieve these results, the raw data from Ansys Q3D must be processed, such that the inductance between two terminals with and without cancellation effects can be easily analysed. The data from Ansys Q3D is exported as a .csv file, which contains the terminal names and their given nets, with a self-inductance and mutual inductances to all other self-inductances. To find the relevant data, a Matlab script is written, which takes in the names of the terminals to be analysed, and uses these to extract the relevant inductances and their couplings from the .csv data file. The code for the Matlab script, which calculates these inductances can be seen in Appendix E on page 140.

As mentioned, the inductances in a given net are defined as the self-inductance between the sink and each source, with a given coupling between each self-inductance. A circuit schematic of a net with two sources and one sink can be seen in Figure 4.5.

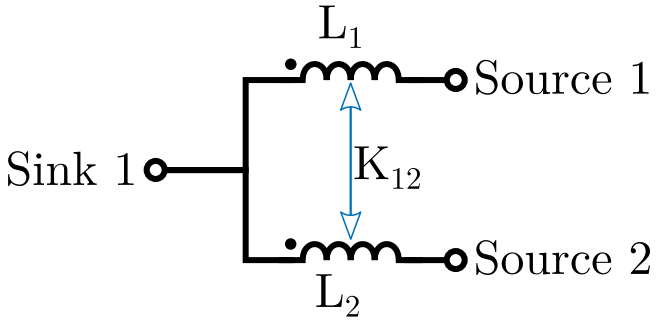


Figure 4.5: Simple net from Ansys Q3D with one sink and two sources.

The circuit can be described in a matrix form as seen in Table 4.2.

	N1, S1	**N1, S2**
N1, S1	L_1	M_{12}
N1, S2	M_{12}	L_2

Table 4.2: Inductance matrix of Figure 4.5. N refers to Net number, S refers to source number.

In order to find the inductance from Source 1 to Source 2, the self inductances can be considered as two inductors connected in series, with opposing mutual inductances. Therefore, the inductance of these in series can be found as:

$$L_{12} = L_1 + L_2 - 2M_{12} \tag{4.2}$$

Using (4.2), it is possible to extract any specific inductance between two terminals in the circuit.

4.2.3 Loop Inductance

In order to find the loop inductance in a circuit, the coupling between inductances in different nets has to be considered. Another example circuit has been created, which can be seen in Figure 4.6.

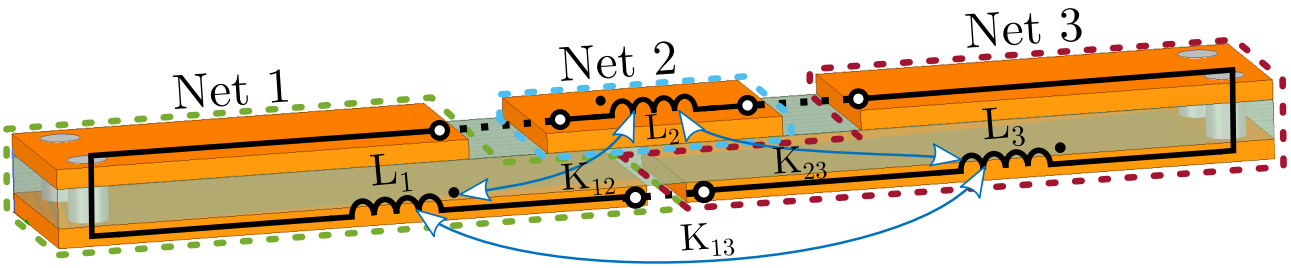


Figure 4.6: Example circuit showcasing a loop.

In Figure 4.6, an example circuit showcasing a loop is seen. It can be seen, that for every net, an inductance is defined. Each of these inductances are magnetically coupled with each other. This concept is explored further in Section 5.3 on page 46. This circuit can also be described as an electrical schematic as seen in Figure 4.7:

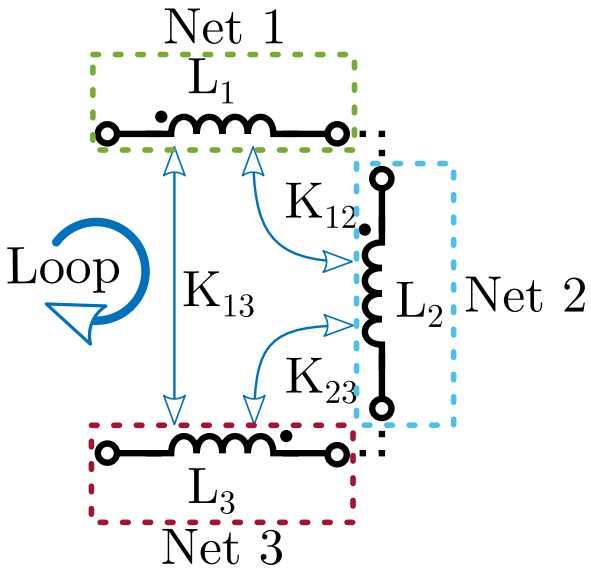


Figure 4.7: Three nets as defined in Ansys Q3D, each with one set of sinks and sources.

This loop can be seen in matrix form in Figure 4.3.

	N1, S1	**N2, S2**	**N3, S3**
N1, S1	L_1	M_{12}	M_{13}
N2, S2	M_{12}	L_2	M_{23}
N3, S3	M_{13}	M_{23}	L_3

Table 4.3: Inductance matrix of Figure 4.7. N refers to Net number, S refers to source number.

As the inductors seen in Figure 4.7 are connected in series, with aiding mutual inductances, as opposed to the opposing mutual inductances seen in Figure 4.5, the total inductance can be calculated as adding series coupled inductances. For example, the inductance of L_1 and L_2 in series can be found as follows:

$$L_{12} = L_1 + L_2 + 2M_{12} \tag{4.3}$$

This means, that in order to get the total loop inductance, with flux cancellation, taking all three nets in consideration, one simply has to add all of the entries of the matrix together. The requirement for this to be possible, is that the nets should be defined in the right order, as the current would flow in the circuit. However, if the inductance of the loop without flux cancellation is desired, the self-inductances in the main diagonal of 4.3 can be summed. The relation between the inductance with and without flux cancellation can be an indication of how much flux cancellation has been achieved.

Using these concepts and equations, the process of finding trace inductances and loop inductance can be automated, only requiring a .csv file with all of the self-inductances. The matlab script then requires the name of the .csv file, and which terminals are to be considered. This lessens the time of finding specific circuit inductances, as all the required inductances can be extracted from a single simulation, improving efficiency and reducing turnover time.

4.3 Integration with LTspice

After simulating a circuit by FEA using Ansys Q3D, a SPICE circuit block can be exported, which includes all of the calculated inductances, capacitances and resistances. By implementing this block into a spice circuit, the electrical characteristics of the parasitics found by FEA can be implemented in a spice simulation which includes the dynamic performances of different components. An example of this, with the final circuit can be seen in Figure B.1 on page 133. The block will have a number of nodes, corresponding to the number of terminals defined in the Ansys Q3D simulation. Inside of the block, these nodes are connected using the inductances, mutual inductances, capacitances and resistances found in Ansys Q3D.

A simpler example of this block can be seen in Figure 4.8, where the circuit shown previously, in Figure 4.2, has been evaluated in FEA, and an LTspice block has been generated.

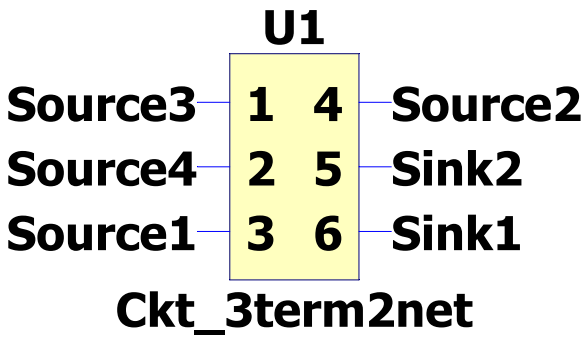


Figure 4.8: LTspice block generated from example circuit.

As mentioned, this circuit had a total of 6 terminals; two sinks, and four sources. The internal code of this block can be seen in Section B.1 on page 131.

When the LTspice block has been generated, it can be connected to various SPICE components, including all of the active switching components, and passive components. The block will then connect all of these components internally, using the parasitic components found in the FEA. The parasitic content of the circuit found in the FEA then shapes the performance of the circuit, aiming to accurately represent the electrical performance of the circuit. By analysing this simulated performance, the designed circuit can be evaluated. This procedure can be thought of as a prototyping procedure, without the use of physical prototypes. Therefore, it can hasten the design and prototyping process of a circuit, as it can be performed digitally, as opposed to needing to build physical prototypes to test a given circuit.

4.4 Optimisation Using Digital Design

When choosing components for use in a complex circuit, it may be difficult to precisely determine the required component parameter, as they are often chosen as a trade-off between different performance characteristics. For example, when choosing gate resistors, a higher resistance may result in more stable performance, but slower switching times. In order to achieve a good performance, one can follow general "rule-of-thumb" design criteria, to scale the specific components. However, this approach will most likely not result in an optimal setup. Another approach would be to manually try different components on a physical setup, iteratively varying component parameters, until a satisfactory result is achieved. However, this is a time-consuming process, as one has to de-solder the old component, and solder on the new component for each iteration. By removing and replacing components multiple times, the PCB can be damaged from excessive, repeated heating.

By calling the LTspice model with the included parasitic block from a Matlab function, the process of finding the optimal component for a given circuit can be greatly improved. Firstly, the circuit to be modelled is exported as a SPICE netlist. This netlist includes all of the component connections, and their given parameters. This netlist can then be used to run an LTspice simulation from the Matlab code. Then, using loop functions in Matlab, a number of simulations can be executed, whilst altering relevant component parameters. This can be repeated, until a sufficient amount of data is achieved. The simulations can then be numerically analysed in terms of different performance characteristics, such as device switching times and efficiency. By utilising optimisation concepts, such as the Pareto optimality, the ideal component parameters can be chosen, with an optimal trade-off between two

evaluation parameters. This concept is utilised in Chapter 8, in order to determine the optimal FB in the gate of the GaN HEMT, as well as to find the optimal gate resistor configuration.

With this approach, the time and resource consuming process of empirically testing the performance of specific components in the circuit in an experimental setup, as proposed by the manufacturer [53], can be moved to a digital platform. This allows to analyse a broader range of components than what otherwise would be suitable.

4.4.1 Optimisation Parameters

To evaluate the efficacy of a component in a given design, the performance of a design has to be parameterised. To exploit the fast switching of the GaN HEMTs, the first parameter of interest is the rate of change of drain current, or di/dt, which defines how fast the current rises or falls during turn-on and turn-off, respectively. First of all, the rise and fall times have to be defined. In this project, the rise time will be defined as the time interval between 10 % and 90 % of the final amplitude. The fall time is likewise defined as the time interval between 90 % and 10 % of the amplitude.

The di/dt for turn-on is then defined as:

$$\frac{\mathrm{d}i}{\mathrm{d}t} \approx \frac{\Delta I}{\Delta t} = \frac{I_{90\%} - I_{10\%}}{t_{rise}} \tag{4.4}$$

Where $I_{90\%}$ and $I_{10\%}$ is the value of the current at 90 % and 10 % of the amplitude. respectively. For turn-off, di/dt is defined as:

$$\frac{\mathrm{d}i}{\mathrm{d}t} \approx \frac{\Delta I}{\Delta t} \frac{I_{90\%} - I_{10\%}}{t_{fall}} \tag{4.5}$$

This parameterises how fast a design switches. The higher the di/dt, the faster the switching, which means that this parameter is to be maximised. On the other hand, fast switching can lead to overshoot and oscillations, which in turn can cause unwanted self turn-on and increased heat dissipation. Therefore, another important parameter which is considered in the optimisation process is the average dissipated power. This value takes switching losses, conduction losses, and eventual unwanted self turn-on into account, and is calculated as follows:

$$P_{avg} = \frac{1}{t_{end}} \int_{t_0}^{t_{end}} |I_D \cdot V_{DS}| \, \mathrm{d}t \tag{4.6}$$

Where t_{end} is the final time of a simulation, t_0 is the start time of the data of interest, I_D is the drain current and V_{DS} the drain-source voltage of the device. To have an efficient HB switching module, the average power dissipation should be as low as possible, and will therefore be minimised in the optimisation process.

4.4.2 Pareto Optimality

To maximise the di/dt, and minimise the average dissipated power, pareto optimality theory will be applied. In the context of this analysis, a point is a pareto optimal point if no other point exists with a higher di/dt and lower average power dissipation. This leads to a set of pareto optimal points, that each include an optimal compromise between a high di/dt and low power dissipation [54]. To choose a solution out of this set, the concept of the utopia point can be introduced. The utopia point is the

point which incorporates the highest di/dt and the lowest average dissipated power out of the entire set [54]. Figure 4.9 shows example data from a simulation run to illustrate the concept.

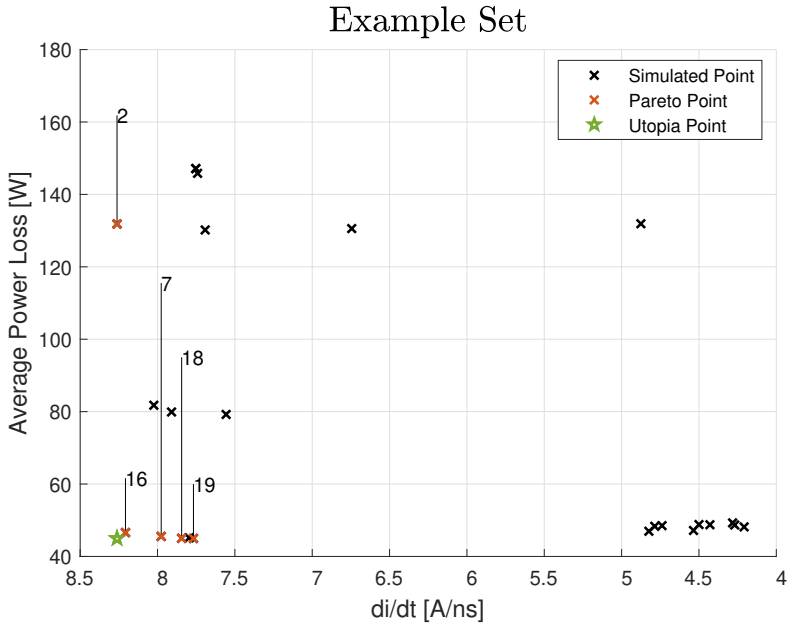


Figure 4.9: Example data to illustrate the concept of pareto optimality and utopia point.

In Figure 4.9, the pareto optimal set consists of points 2, 7, 16, 18, and 19. The utopia point consists of the maximum di/dt of 8.26 A/ns, achieved by point 2, and the minimum average power loss of 44.97 W, achieved by point 19. In this example case, the optimal point is determined to be point 16, at it lies very close to the utopia point, which incorporates the best performance of each parameter [54].

Chapter 5

Circuit Analysis

This chapter will analyse the circuit design of the parallel HB switching module, such that a practical prototype can be created. This will include an analysis of the requirements for the GD design, where features such as a bipolar and split output GD will be discussed. Moreover, issues with high side driving will be explained as this can be difficult due to a floating source reference. These analyses will lead to the selection of the relevant components for the GD circuitry such as the specific GD IC, DC-DC converter, optical receiver and more. Next, the function of the gate resistors will be explained to understand which dynamics are affected by the gate resistance. Also, FBs will be analysed as these can be utilised at the gate of the GaN HEMTs to dampen specific frequencies.
On the power side the decoupling capacitors function will be analysed in order to clarify which parameters affect its operation.
Finally, the basics of parasitic contents of PCBs will be discussed in order to understand how they affect the circuit dynamics, and how the parasitic content can be minimised.

5.1 Gate Driver Design and Analysis

In order to activate the GaN HEMTs, a charge has to be delivered from a GD IC into the gate of the device. In order to get a better understanding of the GD and its purpose, the equivalent circuit of a single GaN HEMT with a simplified GD as seen in Figure 5.1.

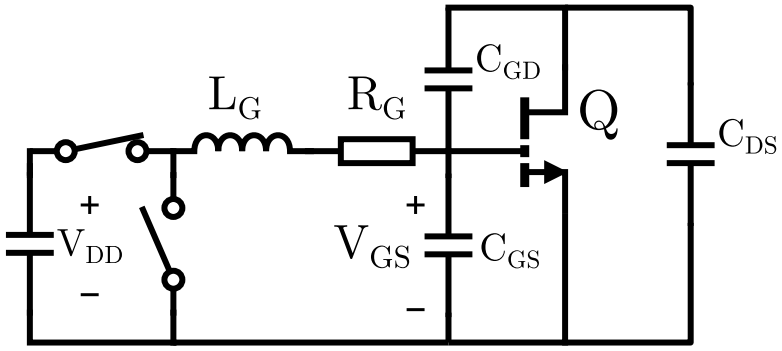


Figure 5.1: Equivalent circuit of GaN HEMT with a simplifed GD.

As can be seen in Figure 5.1, the GD, together with the input capacitance C_{iss} can be thought of as a switched RLC circuit. In order to turn on the GaN HEMT, the gate-source voltage V_{GS} must increase above the threshold voltage V_{th} of the device. To do this, the input capacitance, which is comprised of the gate-source capacitance C_{GS} and the gate-drain capacitance C_{GD}, must be charged. Together with the gate resistance R_G and parasitic GD loop inductance L_G, this forms a series RLC circuit.

In order to design the appropriate GD circuit, the average power and current supplied to the device must be found [55]. Looking at the datasheet of the device, the total gate charge Q_G to turn on the device is found to be 6.1 nC [23]. As the device will be activated at a given switching frequency f_{sw}, and the charge to the device is to be supplied at the rate of the switching frequency, the power and current required to drive a device can be found:

$$I_G = Q_G \cdot f_{sw} \tag{5.1}$$

This is the average current required to drive a device at a given frequency. Moreover, the power required to drive a device is found by considering the drive voltage:

$$P_G = f_{sw} \cdot V_{DD} \cdot Q_G \tag{5.2}$$

As four devices are to be activated at the same time, with one GD, the current and power have to be multiplied by four to find the total current and power requirements.

In order to maximise the performance and stability of the GD circuits, some considerations have to be made, which are presented in the following sections.

5.1.1 Bipolar Gate Driver

To improve the gate stability, and reduce the risk of unwanted turn-on effects, a bipolar supply voltage can be used in the GD circuit. This bipolar voltage supply allows the GD to apply a negative voltage to the gate when turned off. To achieve such a bipolar gate drive voltage, a supply voltage is split in two, resulting in a positive and a negative voltage reference. This can be done by the use of a zener diode, generating a voltage reference. As the zener diode has a stable reverse conducting voltage drop, it can be used to generate a stable negative voltage reference. This circuit can be seen in Figure 5.2.

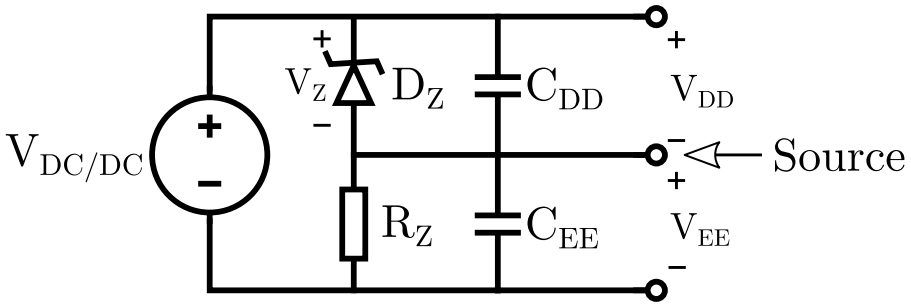


Figure 5.2: Bipolar voltage generating circuit.

Looking at Figure 5.2, it can be seen that the zener circuit effectively divides the input voltage source into two different voltages. The capacitors in the circuit are used to even out these supply voltages, and account for the current draw of the GD circuit. The resistor is connected to the zener diode is present in order to ensure a constant desired current draw through the zener diode, ensuring the required reverse voltage is achieved. As the GaN HEMT device from GaN Systems requires an on gate supply voltage V_{DD} of 6 V [23], the zener diode is chosen accordingly, with a 6 V reverse voltage drop. The MMSZ5233BT1G [56] from ON semiconductors is chosen.

5.1.2 Split Output

A split output GD can be utilised in order to achieve better control of both the turn-on and turn-off sequences. With a split output, the turn-on and turn-off loops can have individual parameters, and the dynamics of each can be adjusted individually. This can be utilised to achieve a miller clamping effect. By choosing a low resistance gate resistor in the off loop, the voltage drop over the gate impedance caused by the miller effect can be reduced, increasing stability of the circuit.

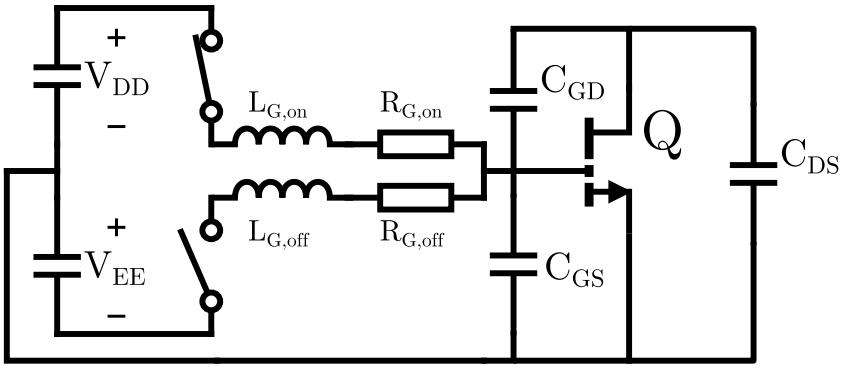


Figure 5.3: GD with split output and bipolar gate voltage.

In Figure 5.3 the GD circuit with both bipolar voltage and split outputs is illustrated. It can be seen, that as these two loops form individual RLC series circuits, whose damping and resonance frequencies might be different. The parasitic inductances in the loops will depend on the trace length and loop area from the GD to the device. As the on and off loops occupy roughly the same area on the PCB, these inductance values will be similar. Moreover, apart from effects of non-linear capacitance values of the device [23], the capacitance in the two RLC circuits will be similar as well. However, the resistance values in these loops can be varied according to need. In order to ensure fast switching speeds, the gate resistances can be kept small. This reduces the damping factor in the RLC circuit and increases slew rates of the device. However, this may risk the loop being underdamped, causing overshoots on the gate voltage, and leaving the circuit susceptible to induced oscillations.

The importance of a low off-resistance can be explained by looking at Figure 5.4.

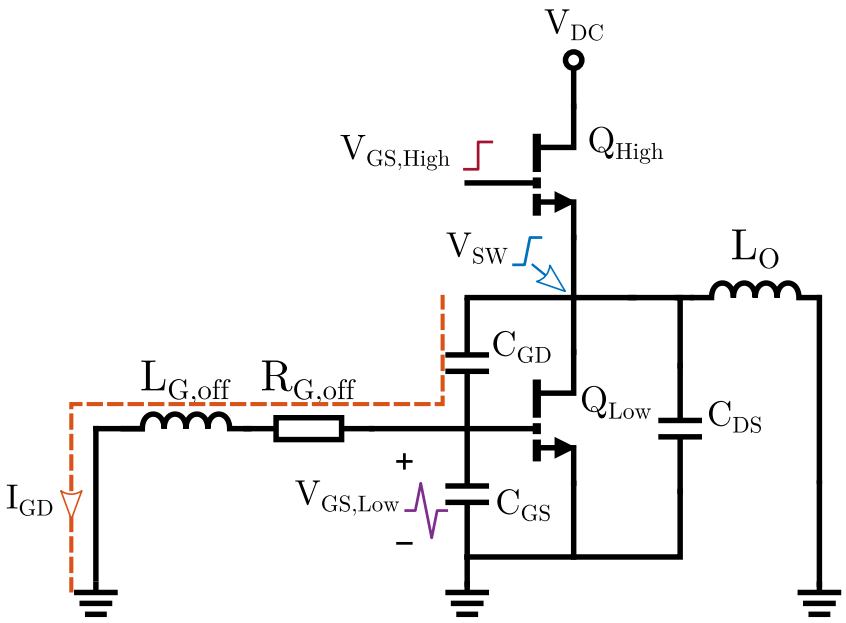


Figure 5.4: Miller induced gate voltage disturbance. [53]

Figure 5.4 shows an example of Miller current induced disturbance on the gate of the low side device in an HB configuration.

As the high side device Q_{High} turns on, the voltage V_{SW} over the low side device will quickly rise from the ground potential, until reaching the DC bus voltage V_{DC}. This will charge the drain-source

capacitance C_{DS} up to this voltage. Moreover, the gate-drain capacitance C_{GD} must also be charged to a value of $V_{SW} - V_{GS}$. This will cause a current I_{GD} to flow through C_{GD}, into the GD. As the slew rate of these devices can reach hundreds of volts per nano-second, this current can have a considerable amplitude. This current will then flow into the GD loop. As a result of this current, a voltage drop will occur over the gate loop impedances. This voltage drop is essentially added on to the GD voltage, and the gate-source voltage is disturbed. This could cause the device to unintentionally turn on, possibly resulting in a shoot-through of the HB. This effect is especially relevant in GaN HEMTs, as a result of their high slew rates and low threshold voltages [53]. To minimise this effect, a low resistance in the off loop should be used, effectively a miller clamp. Due to this effect, it is also important to minimise the loop inductances as much as possible.

5.1.3 High Side Driving

In a HB circuit configuration, one has to take into account the floating source reference of the high side devices. This means that the voltage reference for the GD of the high side devices must be referred to the source pin of the high side devices, not to the ground reference. There are different ways to achieve this floating voltage, such as using bootstrap diodes to charge a capacitor referred to the high side device [55]. This circuit has the advantage of being simple and cheap, but has some drawbacks such as limiting the duty-cycle capabilities of the circuit, requiring a certain time to charge the capacitor every switching cycle. Moreover, as the bootstrap GD in a HB configuration is itself referred to the low side device source, as this low side device enters reverse conduction, the source reference of the high side device will be negative, as there is a voltage drop over the reverse conducting device. This can cause issues in the bootstrap GD [57]. In GaN HEMTs, the reverse conducting voltage drop can be considerable, as it depends on the gate voltage applied during turn-off, as seen in (2.1).

Another way to achieve the high side voltage, referred to the high side device is to use an isolated DC-DC converter. This converter is supplied by a given DC voltage, and converts it to the desired output voltage, while providing galvanic isolation. This galvanic isolation ensures that the voltage for the high side side GD can be referred to the high side device source node.

One important challenge to consider when choosing an isolated DC-DC converter, especially in high dv/dt application such as a GaN HEMT HB, is the parallel capacitance of the DC-DC converter. As the output of the DC-DC converter on the high side driver is connected to the source pin of the high side device, it will endure the high dv/dt of the HB switch node (SW). As there is some parallel capacitance between the input and output of the DC-DC converter, this dv/dt will cause a current to flow through the GD circuit. This is illustrated in Figure 5.5.

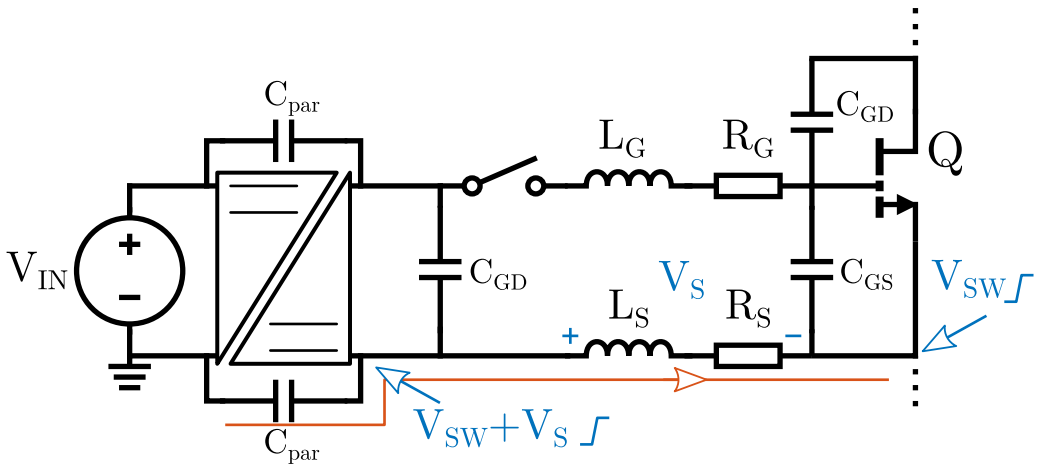


Figure 5.5: Effect of DC-DC converter parallel capacitance. **Note:** The GD circuit is simplified.

As can be seen in Figure 5.5, a dv/dt over the DC-DC converter causes a current to flow through the parallel capacitance of the DC-DC converter C_{par}. This will then cause a voltage drop over the GD loop impedances L_S and R_S for example. This voltage drop may cause disturbances in the GD loop, altering the voltage supplied to the gate of the device. This could cause the circuit to exhibit unstable behaviour during switching. Therefore, a DC-DC converter with a minimal parasitic capacitance should be chosen.

5.1.4 Optical Receiver & Signal Inverter

In order to electrically isolate the HB switching module from the Digital Signal Processor (DSP) it is controlled by, optical isolation is used. This way, there is no electrical connection between the DSP and the HB, reducing the possibility of interference and improving safety. The optical receivers used are SFH551V [58]. The setup of this is shown later in Figure 9.2 on page 92. As the optical receivers output is inverted when related to the optical signal, an issue of safety occurs. This means, that if a gate should be off, its corresponding optical receiver should receive an optical signal. If the fiber optic cable would be accidentally removed, or the light signal is removed by some cause, the gate of the device would turn on. This is a safety hazard, as this could cause both the high side and low side devices to turn on at the same time, causing a shoot-through of the HB. In order to improve safety, a signal inverter, SN74LVC1G04 from TI [59], is placed at the output of the optical receiver. This way, if the optical signal is lost, the corresponding devices will be turned off.

5.1.5 Choice of GD

When driving multiple devices in parallel, it is important to be able to turn these devices on simultaneously. Therefore, it is chosen to only use one GD for all the devices which are paralleled. This decision is made to avoid the possibility of dissimilar propagation delays, if multiple GDs were used. This could cause some devices to turn on before others, causing an imbalance in load sharing. However, the disadvantage of having single GD to drive all devices in parallel, is the GD loop inductances might be larger, as the gates of the devices all have to be connected to a common point, i.e. the output of the GD. Therefore, it might be difficult to get identical loop inductances in the different GD loops going to each device. The effects of this imbalance was discussed in Section 2.2.

Based on the considerations previously mentioned, the GD chosen to drive the HB circuit is the Si8271 single GD [60]. This GD has a split output, allowing for separate on and off loop parameters.

5.1.6 Choice of DC-DC Converter

In order to be able to choose the required components for use in the GD, the power usage of the whole GD circuit should be considered. As the DC-DC converter will supply this power, it should be rated as such.

The power losses in the GD from driving one GaN HEMT can be approximated as [60]:

$$P_{GDr} = f_{sw} \cdot Q_G \cdot V_{DD} \cdot \frac{R_{Pup}}{R_P up + R_{G,on}} + f_{sw} \cdot Q_G \cdot V_{DD} \cdot \frac{R_N}{R_N + R_{G,off}} + 2 \cdot f_{sw} \cdot C_{GDr} \cdot {V_{DD}}^2 \quad (5.3)$$

Where $R_{Pup} = 2.7\Omega$ is the internal pull-up resistance of the GD, $R_N = 1\Omega$ is the internal pull-down resistance of the GD and $C_{GDr} = 370pF$ is the internal parasitic capacitance of the GD. [60] For the scope of this analysis, the gate resistors $R_{G,on}$ and $R_{G,off}$ are assumed to be $= 14\Omega$. For this calculation V_{DD} is assumed to be $= 9V$. The gate charge C_G is 6.1 nC, as defined in the datasheet [23].

The total power usage of the GD with 4 GaN HEMTs can then be summed, using (5.2) and (5.3)

$$P_{G,total} = 4 \cdot (P_G + P_{GDr}) \quad (5.4)$$

The power calculated in this section may not be equal to the power draw of the final circuit, but will be used to determine the required DC-DC converter. This is due to the fact that the gate charge used in (5.3) is defined as the gate charge required to bring the input capacitor of the device from 0 V to 6 V. In reality, this charge would be greater, as charging the input capacitor from a negative voltage would require a greater charge. Moreover, the gate resistance in further designs of the circuit will change according to need.

Using (5.4), and sweeping the frequency, it is found that by using a 1 W DC-DC converter, a maximum switching frequency of approximately 2 MHz can be achieved. This is considered to be sufficient for the scope of this project. Considering this power draw, and the importance of low parasitic capacitance explained in Section 5.1.3, a DC-DC converter can be chosen. In order to increase the stability of the parallel GaN circuit additionally, a 12 V output is chosen. Combined with a 6 V zener diode in the bipolar gate voltage circuit explained in Section 5.1.1, this results in an on gate voltage of 6 V, and an off gate voltage of -6 V. A DC-DC converter which fulfils all of these requirements is the RP0512S from RECOM. It has a low parasitic capacitance of 4-10 pF, an output power of 1W and an output voltage of 12 V. [61]

5.1.7 Gate Resistors

To operate the GaN HEMTs properly it is important to select the right gate resistances, as choosing a too low resistance will result in overshoots and excessive ringing on the gate-source voltage, and an excessively high resistance will slow down the switching times of the GaN HEMTs.

This effect can be explained in terms of the damping factor of different gate resistances [62].

The value of the damping factor ζ can then be determined:

$$\zeta = \frac{R}{2} \cdot \sqrt{\frac{C}{L}} \tag{5.5}$$

This damping then expresses the dynamic behaviour of the RLC circuit, whether it is over-, under- or critically damped. From (5.5) it can be determined that the damping of the series RLC will increase as the gate resistance increased.

When using a single GD in parallel operation, the gates of the different devices will be connected. This makes each devices susceptible to noise from the other devices if not symmetrically arranged. At turn-off a high di/dt will occur through the drain inductance L_D. This will increase the drain-source voltage V_{DS} rapidly which creates a high dv/dt across the gate-drain capacitor. This high dv/dt across the gate-drain capacitor will force a current to flow into the gate loop as seen in Figure 5.6 [63].

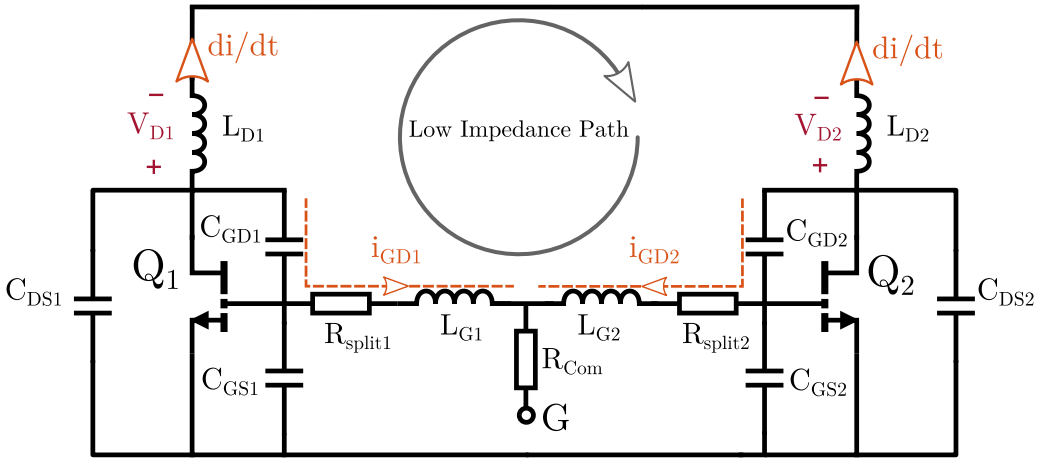


Figure 5.6: Illustration of two devices in parallel with a shared gate connection. A low impedance path is created between these devices, forming a series RLC circuit.

Looking at the gate current coming from each gate-drain capacitor, it can be seen that the current from Q1 flows in the opposite direction from the one of Q2. If these currents are identical, they will cancel each other out. However, if the parasitic inductances in the drains are not identical, this can lead to a current flowing from the faster switching device to the slow switching device through the low impedance loop illustrated in Figure 5.6 [64]. This low impedance loop can be seen as a series RLC loop. The circulating current will trigger the resonance of the series RLC circuit, which in turn will affect the gate-source voltages of the devices. This could lead to unintended turn-on or breakdown of the devices.
To ensure the stability of the series RLC circuit it is important to analyse the quality factor. The

quality factor for a series RLC resonance circuit is given by [63]:

$$Q_f = \frac{1}{R} \cdot \sqrt{\frac{L}{C}} \tag{5.6}$$

The quality factor describes the behaviour of the resonance circuit and how well the resonance is damped for the specific RLC circuit. The impedance of this series RLC circuit can be found as follows:

$$Z(f) = \sqrt{R^2 + \left(2\pi f L - \frac{1}{2\pi f C}\right)^2} \tag{5.7}$$

By increasing the resistance the impedance at the resonance is increased, which will damp the resonance and thereby decrease the amplitude of the resonance. This will in term give a lower quality factor. This is illustrated in Figure 5.7 with different resistances, where the circuit without any added resistance is represented by the blue plot with 2.5 Ω. In the orange plot, resistance has been added to the circuit, such that a total resistance of 25 Ω is achieved. Equation (5.7) is used to find the impedance of the series RLC circuit.

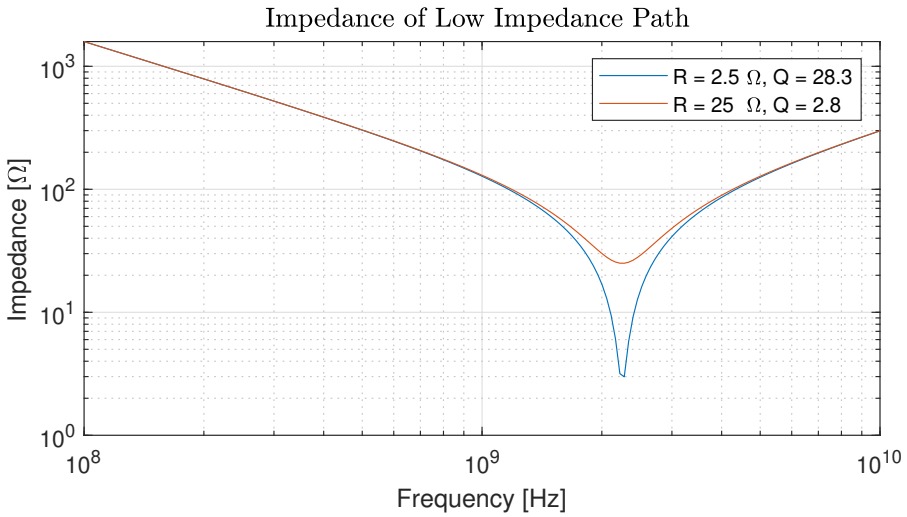


Figure 5.7: Illustration of impedance of the RLC circuit with different resistances. The quality factor along with the different resistances can be seen in the legend. Parameters are chosen as an estimate of a circuit with GaN HEMTs in parallel. $C = 1pF$, $L = 5nH$.

To increase the impedance of the RLC circuit, split resistors can be placed at the gate of both devices. The split resistors will help to lower the quality factor, and reduce any effects of the resonance of the low impedance path. However, having both a common resistance at the GD and a split resistor at the gate of the device it is important to consider the total impedance of the gate loops. This means that selecting the right combination of common resistance and split resistance to ensure proper switching times and damping of unwanted oscillations. This will be determined through a digital optimisation process in Chapter 8.

5.1.8 Ferrite Beads

Another solution that can be implemented to reduce unwanted oscillations on the gates of power transistors are FBs. These have been shown to be able to reduce oscillations in various types of devices and circuit configurations [65][66]. By placing a FB close to the gate pad of the device, the unwanted ringings can be dampened, improving switching performance [67], especially when paralleling high di/dt and dv/dt devices such as GaN HEMTs, where paralleling can cause excessive ringings. In [68] the effects of adding FBs to paralleled MOSFETs was examined, and showed that these could dramatically improve the switching performance of the paralleled devices.

FBs are components which have a frequency dependent impedance. FBs can be thought of as parallel RLC circuits, as they posses specific inductance, capacitance and resistance values, tuned to give a specific response. The equivalent circuit of a FB can be seen in Figure 5.8.

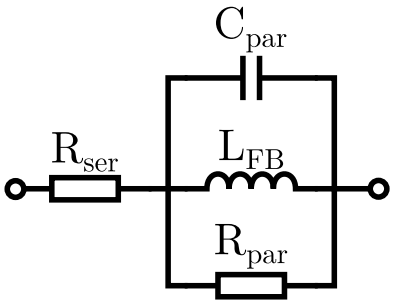


Figure 5.8: Equivalent circuit of a FB.

Looking at Figure 5.8, it can be seen that the FB can be represented as a parallel RLC circuit, with a series resistance. The FB to be used can be chosen by its frequency response, such that a wanted damping at a specific frequency can be acquired, while having a low impedance at lower frequencies.

The impedance at a specific frequency is calculated as follows:

$$Z(f) = R_{ser} + \frac{1}{\sqrt{(\frac{1}{R_{par}})^2 + (2\pi fC - \frac{1}{2\pi fL})^2}} \tag{5.8}$$

Using this, a frequency response can be plotted as seen in Figure 5.9.

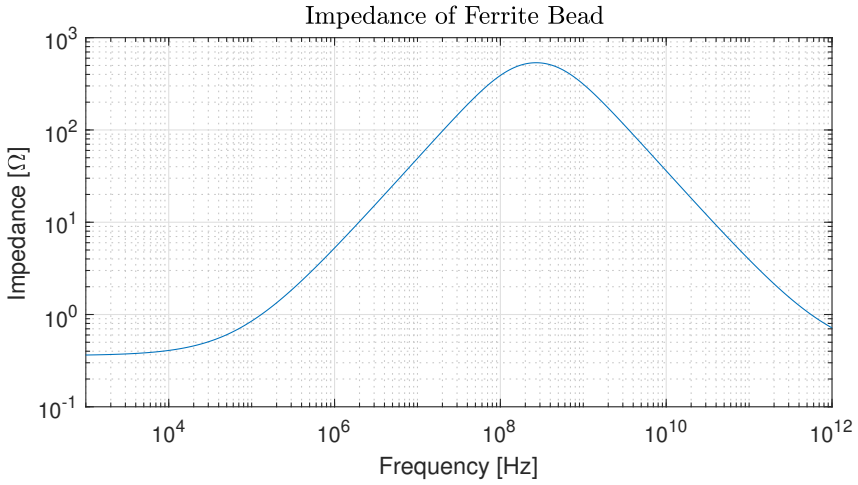


Figure 5.9: Frequency response of Ferrite Number 24 in Table C.1 on page 134.

The impedance graph can be divided up into three regions; the inductive at the lower frequencies, resistive at the resonanse, and capacitive at higher frequencies. In the inductive region, the impedance of the circuit increases as the frequency increases, and the current lags the voltage by 90 degrees. At the resonance frequency of the circuit, the inductive and capacitive reactances cancel each other out, and the resistive impedance remains. Above the resonance frequency, the capacitive region causes the impedance to fall at higher frequencies. Moreover, the voltage will lag the current by 90 degrees in this region.

Comparing the frequency response of the low impedance path shown previously in Figure 5.7 to the frequency response of the FB, seen in Figure 5.9, it can be observed that these have an opposite tendency, the low impedance path being a series RLC circuit, and the FB being a parallel RLC circuit. By adding the FB on the gate of each device, these are effectively added into the low impedance loop. These two RLC circuits in relation can be seen in Figure 5.10.

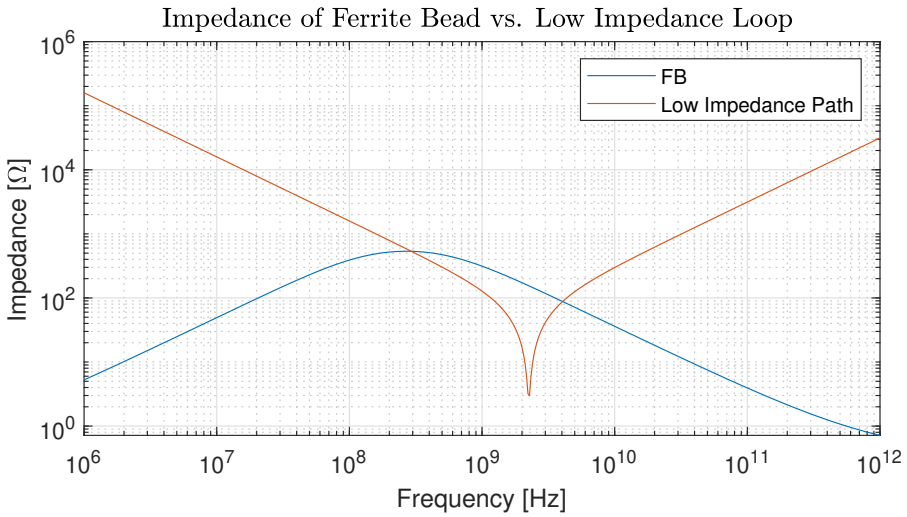


Figure 5.10: Frequency response of a FB vs the low impedance loop of paralleled GaN HEMTs.

As the low impedance path is generated from an estimation of the loop parameters, and the FB is arbitrarily chosen, these do not match up perfectly. But by choosing an ideal FB for a real, given circuit, this could be a way to alleviate the resonance of the low impedance loop without adding too much resistance in the loop.

In Chapter 8, the digital design method will be used to choose the optimal FB for a given circuit.

5.2 Output Capacitors

In order to filter the high frequency switching current from the GaN HEMT HB, decoupling capacitors in the power loop have to be used. These capacitors are used to shunt high frequency current to ground, such that a stable DC voltage can be seen on the output of the circuit.

In order to further understand the need for these, the equivalent circuit of a capacitor can be examined in Figure 5.11.

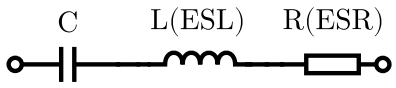


Figure 5.11: Equivalent circuit of a capacitor.

As can be seen in Figure 5.11, the high frequency equivalent circuit of a capacitor includes a capacitance, an inductance and a resistance. In the context of a circuit, these parameters include both intrinsic parasitics in the capacitor package, as well as parasitics from the circuit itself. These three components form a series RLC circuit, whose resonance frequency is given by:

$$f_r = \frac{1}{2\pi\sqrt{L \cdot C}} \tag{5.9}$$

Where f_r is the resonance frequency of the RLC circuit, L is the inductance in the circuit and C is the capacitance of the circuit. Looking at (5.9), it can be seen, that the inductance and capacitance have an inverse relation to the resonance frequency.

5.2.1 Types of Capacitors

Different types of capacitors exists, that have various capabilities and use-cases. For the scope of this project, electrolytic capacitors and Multi-Layer Ceramic Capacitors (MLCCs) will be used and examined. Electrolytic capacitors exhibit large capacitance values, and are therefore used as a DC storage bank in the circuits in this project. A representation of the use of these capacitors can be seen in Figure 5.12, where its placement in relation to the power loop of the HB can be seen. The disadvantage of electrolytic capacitors, is that their electrical characteristics are subpar, when compared to other types. I.e. their Equivalent Series Inductance (ESL) and Equivalent Series Resistance (ESR) values are considerably higher than in other types. The ESL of electrolytic capacitors can range between 5 and 25 nH. [69] As GaN HEMTs can achieve rise and fall times in the order of a few nano-seconds, the frequency content of the resulting current is in the tens to hundreds of MHz. This can be seen in Figure A.1 on page 130. This makes the electrolytic capacitors unsuitable for attenuation of the high frequency currents resulting from switching GaN HEMTs. In order to be able to shunt the high frequency current to ground, MLCCs are utilised. MLCCs offer much better high frequency performance, as their parasitic composure is much smaller. Their ESL is in the range of approximately 1 nH [70]. The MLCC in the circuit can also be seen on Figure 5.12.

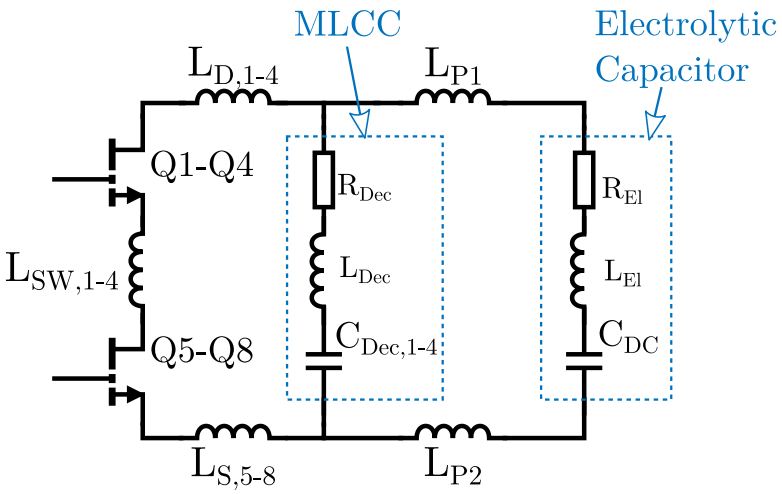


Figure 5.12: Schematic of output capacitors in relation to switching devices. $L_{Px} >> L_{Dx}, L_{Sx}$

It can be observed, that the MLCCs are placed closer to the switching devices on the schematic, than the electrolytic capacitors. This represents the practical setup, as the MLCC decoupling capacitors will be placed as close to the switching devices as possible, while the electrolytic capacitors will be placed further away. Combined with differences in intrinsic parasitic composure of the capacitors themselves, the difference in the inductance, and therefore the high frequency capability of the MLCCs will be considerably better. To visualise the difference in capabilites of these different capacitors, their frequency responses can be examined. In Figure 5.13, using (5.7), the frequency response of three series RLC circuits is plotted. Firstly, the frequency response of a 470 µF, 269 mΩ electrolytic capacitor, with a total inductance of 75 nH, including parasitic and trace inductances, is shown. Then, the frequency response of a 100 nF, 20 mΩ MLCC is shown. This is shown in two scenarios, one with an inductance of 5 nH, representing the RLC circuit of the MLCC with trace and parasitic lead inductance. The other shows the RLC circuit of the MLCC with an inductance of 1 nH, representing the MLCC without trace inductance.

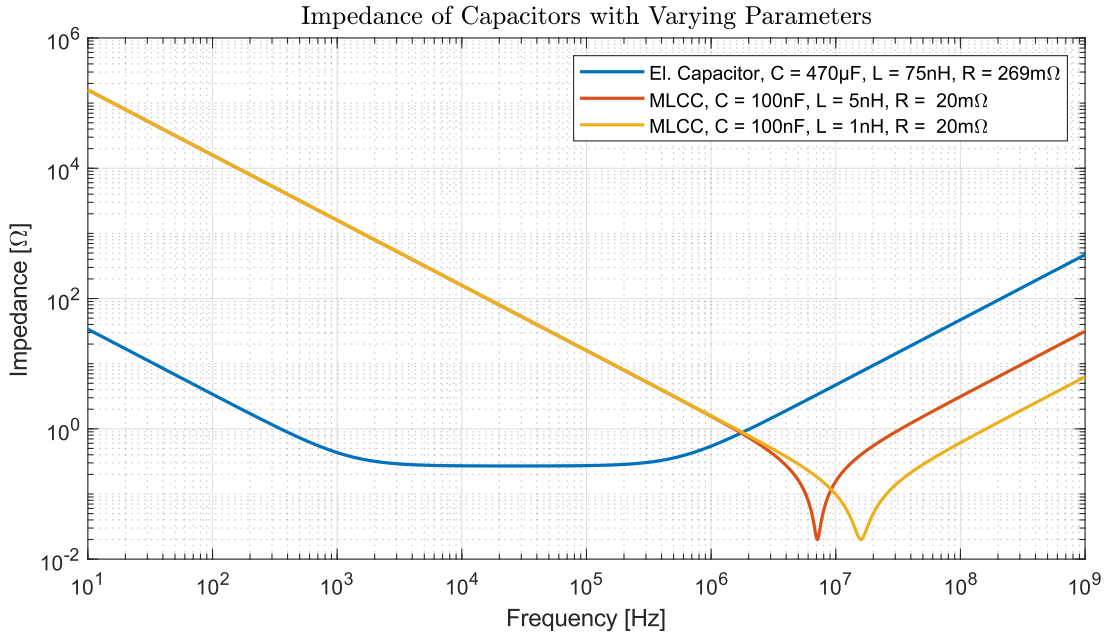


Figure 5.13: Frequency response of series RLC circuits of three different capacitor configurations. Equation (5.7) is used to calculate the impedance.

Looking at the frequency responses of the capacitors, a general trend can be observed. Their impedance is high at low frequencies, falls until a resonance between the capacitive and inductive reactances is reached, and rises at higher frequencies. Comparing the electrolytic capacitor to the MLCC, it can be seen that the resonance frequency of the electrolytic is considerably lower. Approximately 20 kHz for the electrolytic, to several MHz for the MLCC. Comparing the MLCC with and without trace inductance, it can be seen that the resonance frequency considerably different between the MLCC with 5 nH loop inductance, and the one with 1 nH. Moreover, it can be seen that the frequency range at which the electrolytic capacitor is at its lowest impedance spans more decades. This comes as a result of the higher resistance, and therefore lower quality factor. It also means, that the lowest impedance, at the resonance frequency, is higher for the electrolytic capacitor than the MLCC. When comparing the MLCC with 5 nH loop inductance to the one with 1 nH, it can be observed that the higher the inductance value, the worse the high frequency performance of the circuit exhibits. Therefore, it is important to carefully consider the placement of these capacitors in relation to the switching devices, such that an excessive loop inductance is not induced, and the high frequency performance of the capacitor can be retained.

5.2.2 Dielectric Materials of MLCCs

MLCC come in different classes, two of these being class 1 and class 2. These classes indicate the type of dielectric used in the construction of the capacitor, and which applications they are most suited for. Class 1 MLCCs have a more stable capacitance across different temperature and voltage ranges, where class 2 MLCCs might have some variation in capacitance values due to these external factors. However, class 2 MLCCs have higher capacitance densities, and are therefore available in higher capacitance values [71]. The influence of these variations should be considered, as the capacitance of class 2 capacitors could vary considerably under operating conditions.

5.3 Parasitic Content of a PCB

When designing a PCB it is important to consider the parasitic contents, as they will contribute to the system performance with added RLC content. If the content is not considered or reduced to a sufficiently low value, it will have a damaging effect to the system stability. This section will discuss the fundamentals of parasitic RLC content in the PCB design, and determine the important factors to be considered to reduce the effects of them.

5.3.1 Trace Resistance

As there is no ideal PCB trace there will be resistance when routing the PCB. This added resistance will result in losses and increased trace temperature. Moreover, this resistance will influence different RLC resonant circuits, altering the damping of the RLC circuit as discussed in Section 5.1.7. The resistance can be divided into an DC and AC component, where the DC component is given by [72]:

$$R_{DC} = \frac{\rho \cdot l}{w \cdot H} \tag{5.10}$$

Where ρ is the resistivity of the conductor, l is the trace length, w is the width of the trace and H is the trace thickness, as illustrated in Figure 5.14.

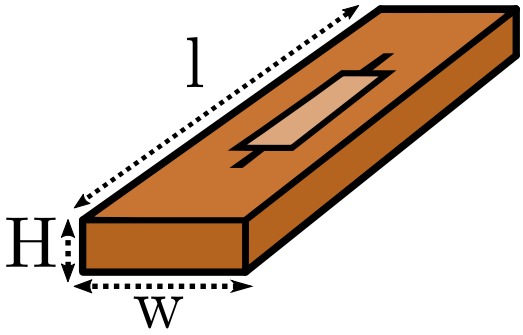


Figure 5.14: Illustration of a PCB trace and the parameters affecting the resistance.

It can be determined from (5.10), that to minimise the DC losses it is critical to keep the traces as wide as possible, and to increase the copper thickness. This is especially critical for high power traces and in areas where high power components dissipate heat. DC currents will be distributed along all of the conductor, but as the frequency increases, the currents start to flow on the surface of the conductor. This is called the skin effect, and as the frequency increases the current will stay closer to the surface area of trace and further away from the center of the trace. This tendency is called the skin depth and is described by [72]:

$$\delta = \sqrt{\frac{\rho}{\pi \cdot f \cdot \mu_0}} \tag{5.11}$$

Where f is the frequency of the current and μ_0 is the vacuum permeability. It can be seen that the skin depth decreases as the frequency of the current increases, as described before. This shows that the AC resistance changes with the frequency, thus the area in which the current flows decreases. As with the DC resistance, when the area decreases the resistance increases, which for the AC resistance can be approximated by [72]:

$$R_{AC} \approx \frac{\rho}{\delta \cdot w} \tag{5.12}$$

It should be noted that this is an approximation and has limitations as it is only viable when the skin depth is less than the conductor thickness [72]. In (5.12) it can be seen that as the skin depth decreases it will increase the AC resistance and this can be countered by making the trace wider.
In general for both the DC and AC resistances, it is important to keep the high power traces as wide as possible to decrease the resistance, and for high frequency operations it is important to consider the AC resistance as it will become increasingly significant.

5.3.2 Trace Inductance

The inductance of a trace is an important factor to consider as stated in Section 2.3 as the high di/dt from the fast switching can give high voltage drops across the parasitic inductances. To reduce the trace inductance it is important to consider the dimensions when routing the PCB as described by: [73]

$$L_{trace} = 0.2 \cdot l \cdot \left[ln\Big(\frac{2 \cdot l}{w + H}\Big) + 0.2235 \cdot \frac{w + H}{l} + 0.5 \right] \tag{5.13}$$

Where L_{trace} is the trace inductance. From (5.13) it can be determined that the length of the traces has a significant impact on the trace inductance compared to the width and thickness [73], which has to be taken into consideration in the design of the PCB.

When connecting traces on both sides of a PCB a via is used. However, a via will introduce added parasitic inductance in the corresponding loop. An approximation of this inductance can be made: [73]

$$L_{via} = 2 \cdot H \left[ln\left(\frac{4 \cdot H}{D}\right) + 1 \right] \tag{5.14}$$

Where D is the diameter of the via and L_{via} is the inductance of the via. From (5.14) it can be seen that by increasing the diameter of the via the inductance can be increased. However, the board thickness is the most significant influence on the via inductance. The via inductance can also be decreased by utilising several vias in parallel.

5.3.3 Magnetic Field Cancellation

As discussed in Section 4.2.2 the mutual coupling of adjacent traces have to be considered in terms of the loop inductance. This coupling happens due to the magnetic field being generated when a current flows through a conductor as illustrated in Figure 5.15 with two adjacent conductors.

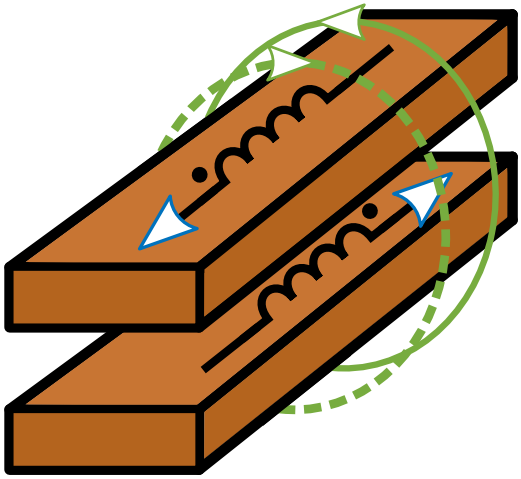


Figure 5.15: Illustration of flux cancellation with two traces and opposite flowing currents.

In Figure 5.15 the blue lines dictate the current direction and the green circular lines are the magnetic field generated by the current. When the magnetic field lines for both conductor are strong enough they will couple and impact the total impedance. When it is as illustrated in Figure 5.15 and the current directions are opposite, the magnetic fields will create a negative coupling meaning that the overall loop inductance will be lowered due to a decrease in the overall magnetic field. However, if the current directions are the same directions, a positive coupling will occur and the loop inductance will be increased.
To ensure a good cancellation it is important to consider the geometry of the adjacent traces as they must have an identical length and dimensions to produce the same, but opposite flux. [74]

5.3.4 Parasitic Capacitance

When designing a multi-layer PCB with semiconductors and high and low voltage sections it is important to consider the capacitive coupling. The capacitance created between two planes is described by: [73]

$$C_{par} = \frac{\kappa \cdot l \cdot w}{11.3 \cdot d} \tag{5.15}$$

Where κ is the relative dielectric constant of the board material, l is the length of the overlapping area and w is the width of the overlapping area and d is the distance between the two planes. This relation is illustrated in Figure 5.16.

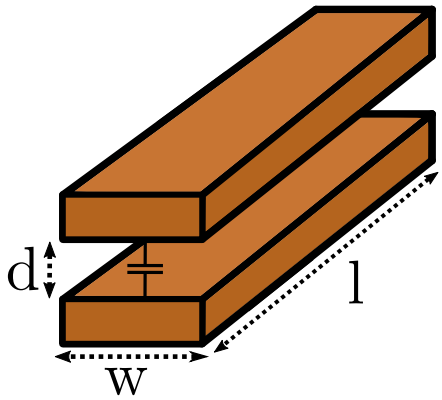


Figure 5.16: Illustration of the capacitive coupling between two planes on a PCB.

It can be seen from (5.15), that to minimise the capacitive coupling, it is important to consider how much of area of the plane or trace that is overlapping another trace. Especially for traces where a high dv/dt occurs, as a current will start to flow across this capacitance, which could affect the system stability. Moreover, it is important to consider the distance d between the planes as increasing the distance will decrease the capacitance created. However, doing this will also minimise the flux cancellation effect, thus it is important to consider which factor will impact the performance the most.

Chapter 6

PCB Design Strategies

In order to determine the impact of the different parasitic inductances and design rules mentioned in Section 2.3, different design strategies will be applied and tested on three different PCBs. This will be done to evaluate the best design compromise for a switching module consisting of four GaN HEMTs in parallel.

All of the designs will have the same GD design and decoupling capacitors as mentioned in the previous sections, and only the layout of the GaN HEMT, traces, and power terminals will vary depending on the specific design strategy of each layout. Both the power loops and GD designs have been evaluated through several design steps before the final designs are presented in this chapter. This has been done with the digital design process by evaluating the inductance improvements on each design numerically.

The source inductance and the power loop inductance are the primary inductances which are varied in size and symmetry across the four GaN HEMTs on the different layouts. The source inductance is defined as the inductance from the source pad of a device to its corresponding power plug. Previously, the quasi-common source inductance was discussed as a high importance design parameter. However, it proved to be difficult to quantify. Therefore, the source inductance was evaluated in its stead, as it was deemed to be somewhat correlated to the quasi-common source inductance.

The primary priority for the GD layout will be to ensure as much flux cancellation as possible by routing the return trace below or as close to the on and off loops of the different devices. In order to achieve this, it is chosen to use a 4-layer PCB board, as this greatly increases the degrees of freedom and is deemed as the minimum number of layers which is needed to route the GD loops from one GD to all four GaN HEMTs appropriately. The secondary priority is to obtain a high symmetry between the GD loops going to each device. As a single GD is used to drive four parallel GaN HEMTs, the distance from the GD to the individual GaN HEMTs will differ. In order to achieve symmetry in the GD loops, care must be taken to place components and traces. Moreover, the capacitive coupling between the power and GD loops should be minimised, as the high dv/dt in the power loop could cause unwanted currents to appear in the GD loop. This is especially important in the high side GD, as the dv/dt from the GD to the DC High plane is considerable.

In the following sections, the design of the different 4-layer PCBs will be presented. For each design, the overall structure of the circuit will be presented, along with the GD structure. To get a clearer view of the layer structure, the four layers are coloured as seen in Figure 6.1.

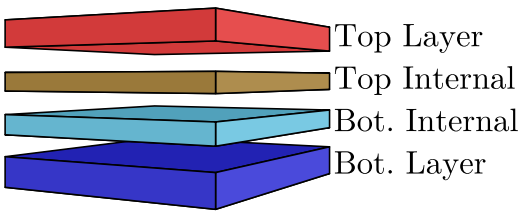
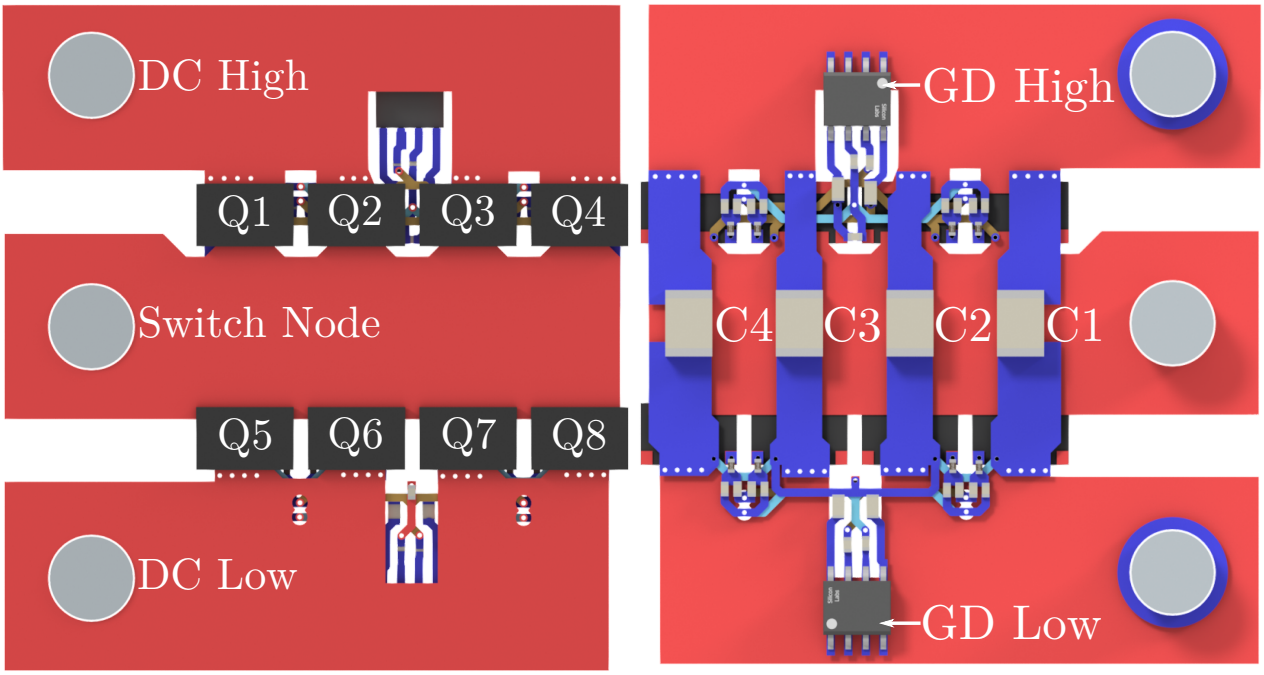


Figure 6.1: Colour distribution of the different layers in the following illustrations of the different designs.

In order to improve electrical and thermal performance of the high power traces, these are routed on the outer 2 oz layers, while lower current signal traces are routed on the internal 1 oz layers.

6.1 Design A

The first design strategy of the HB module is based on an example design layout from GaN Systems, where four GS66516T are paralleled and tested with a DPT at 400 V and 240 A [15]. The design is not described in detail, but general guidelines can be determined. GaN Systems uses a 6-layer PCB, places all the parallel GaN HEMTs in one single line yielding two lines of GaN HEMTs, i.e. high and low side GaN HEMTs. The decoupling capacitors are placed on the bottom layer, along with the GD. These principles were implemented in Design A as illustrated in Figure 6.2a and Figure 6.2b where the design can be seen from the top and bottom side.



(a) The top side of the PCB of Design A. **(b)** The bottom side of the PCB of Design A.

Figure 6.2

In Figure 6.2a it can be seen that all the power traces are placed on the top layer along with the GaN HEMTs. The power traces are placed on an external layer in order to improve the heat dissipation as this layer is the thickest layer. The GaN HEMTs on the top of Figure 6.2a are the high side GaN HEMTs Q1-Q4 having the drain terminal at the top at the DC-high node and the source terminal at the bottom at the SW. GaN HEMTs Q5-Q8 are placed at the bottom from left to right connecting the drain pads to the SW and source pads to the DC-low node. The power terminals connecting to the DC high, SW and DC low nodes are placed on the left side of the PCB. In order to minimise the capacitive coupling between the high side GD and the power trace, a small cutout has been made in the power trace due to the large dv/dt of the GD in relation to DC high.

The decoupling capacitors can be seen on the bottom layer in Figure 6.2b. Each pair of high and low side GaN HEMTs, e.g. Q1 & Q5, have a separate decoupling capacitor to handle the high frequency current from the fast switching. This high frequency current path is routed on the thicker bottom layer and is made as wide as possible to decrease resistance. The decoupling capacitors are connected through vias directly to the pads of the GaN HEMTs in order to decrease the loop inductance. Several vias have been placed, such that the total inductance could be reduced, by effectively putting the vias

in parallel.

The GD layout for the high side GaN HEMTs can be seen in Figure 6.3 and low side in Figure 6.4.

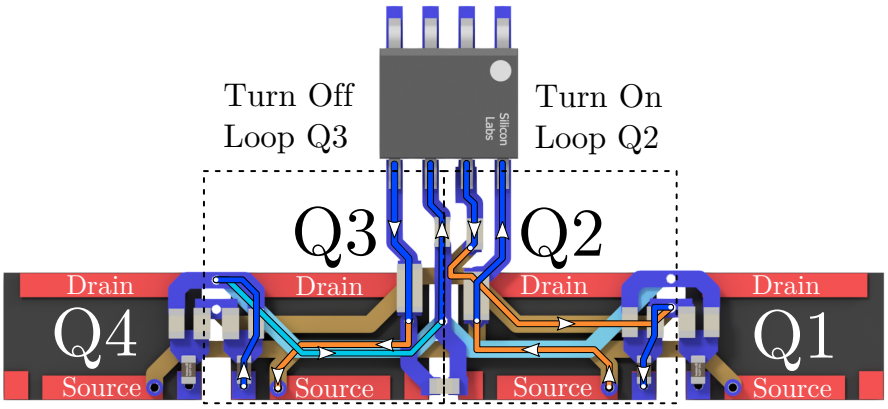


Figure 6.3: The high side GD layout for Design A. The arrows and their corresponding lines indicate the current flow in different gate loops

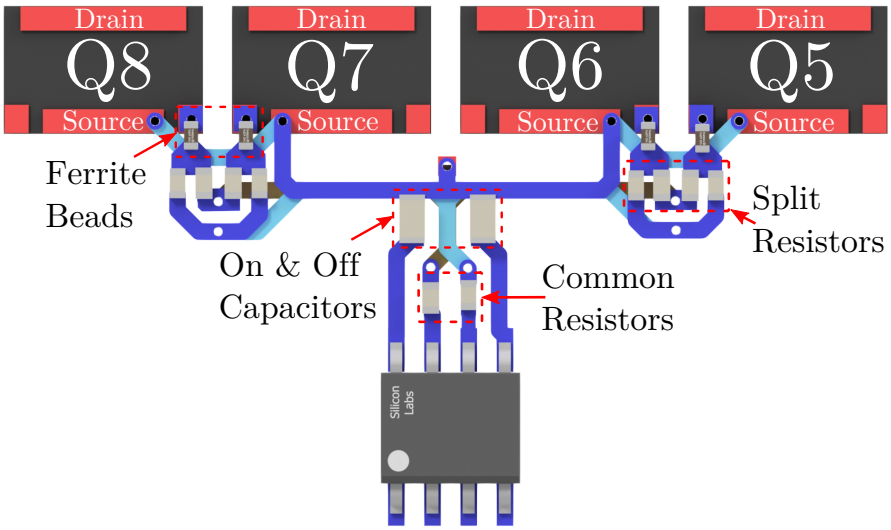


Figure 6.4: The low side GD layout for Design A

In Figure 6.3 the turn-off loop for Q2 and turn-on loop for Q3 are highlighted in order to illustrate the layout of the GD circuitry. In Figure 6.4, the different component groups are designated.

At the gate of each GaN HEMT, a FB and a set of split resistors are placed as close as possible to the gate. The split resistors are then connected to their respective common on and off-resistors, which are placed near the pins of the GD IC. Due to the arrangement of the gate pads being at the same side of the GaN HEMT as the source pad, the gate pads of the high side GaN HEMTs are more difficult to route in terms of cancellation. This is due to the power loop going from the drain of the high side devices to the decoupling capacitors, and down to the source pad of the low side devices. This restricts the number of layers the GD loops can be routed on, thus limiting the cancellation effect on the high side. This can be seen in Figure 6.3, where the return path from the Kelvin connection and the on-loop are both on the top internal layer, and the off-loop is on the bottom internal layer. This means that the off-loop will get more cancellation from the return path, as they can be routed directly above each other. This is desirable, such that the Miller induced gate voltage disturbance is minimised for the off

loop, as explained in Section 5.1.2 on page 35. In the case of the low side GD layout, it is possible to achieve cancellation effects from the return path for both the on and off loop, and utilise this effect to obtain lower loop inductance.

To obtain a maximal symmetry between all the devices connected to one GD IC, the different sets of FB and split resistors connect to a via located an equal distance between the two adjacent devices. From the via at the split resistors, a trace goes to a common point where all devices are connected. This common point is the connected to the GD IC through the common resistor. With these considerations, the total length from the GD to each device should be as equal as possible. The level of symmetry and the total inductance of the on and off loops of the GD circuit can be seen in Figure 6.5.

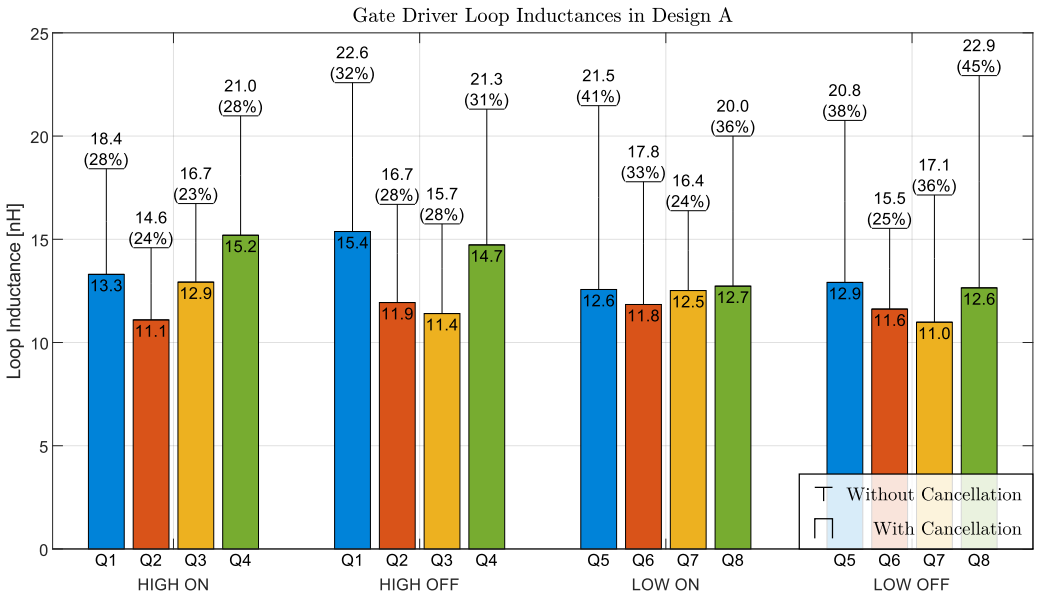
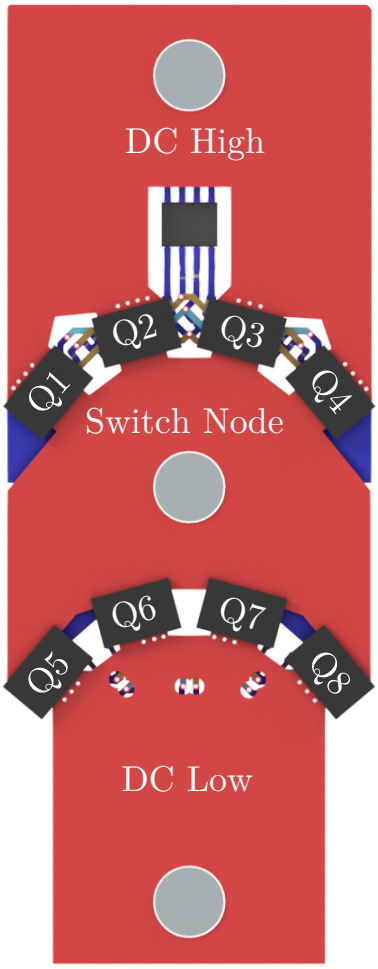


Figure 6.5: GD loop inductances of Design A.

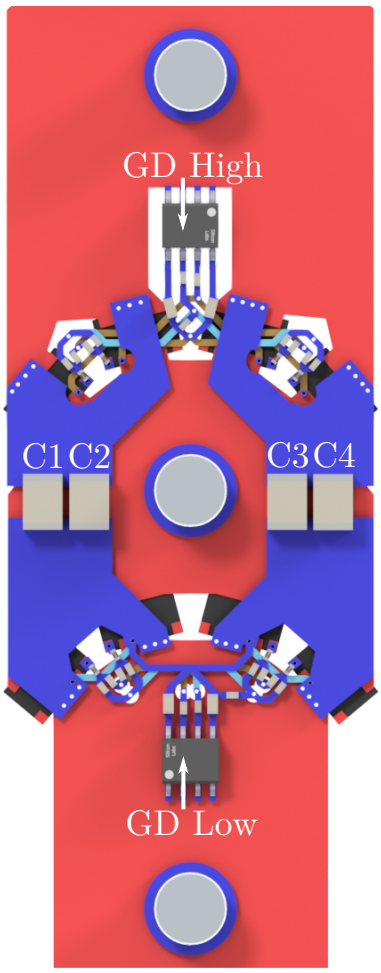
Figure 6.5 shows the GD loop inductances of Design A. These inductances and their flux cancellation effects are found as shown in Section 4.2 on page 25. The high side on and off loops can be seen at the left side of the figure for Q1-Q4. The low side GD loops are shown on the the right side for the on and off loops of Q5-Q8. On top of each bar, a whisker can be seen. The top number above this whisker is the inductance without cancellation. Below this, the amount of flux cancellation in percentage can be seen. Finally, within the bar itself, the loop inductance with cancellation is seen. In Figure 6.5 it can be seen that the greatest symmetry has been achieved in the low side, where the highest amount of flux cancellation occurs. It can be observed, that the high side loops generally have more asymmetry, as well as less flux cancellation. As the power side decoupling trace occupies the bottom trace near the high side driver, the GD loops can not be routed on the bottom trace. This reduces the flexibility of trace routing, and symmetry is more difficult to achieve.

6.2 Design B

In order to test the effect of keeping the source inductances low and symmetric, another design was derived. By centralising the power terminals and equalising the distance from the power terminals to the source pads of both the high and low side devices, it is deemed that the source inductances would be more symmetrical and smaller. To ensure this, the high and low side devices are angled to form a downward semi-circle which can be seen from a top and bottom view in Figure 6.6a and 6.6b,



(a) The top side of the PCB of Design B.



(b) The bottom side of the PCB of Design B.

Figure 6.6

By having the power terminals in the center and achieving greater symmetry in the source inductances, a better current distribution should be achieved, which will help equalise losses in the devices. In Figure 6.6b it can be seen that obtaining source symmetry results in a larger power loop inductance, as the SW is elongated. As the decoupling capacitors are pushed to the side, it was chosen to pair the decoupling capacitors to keep a wide trace and decrease resistance as seen in Figure 6.6b.

From Figure 6.6a and 6.6b it can be seen that the length from the source pads at the low side devices to the DC low power terminals is not as equal as for the high side. This is because of the placement of the GD IC, which makes it difficult to achieve perfect symmetry in the source inductances in the low side devices, as there has to be room for the components connecting to the input of the GD IC.

The GD layout for the high side GaN HEMTs can be seen in Figure 6.7 and low side in Figure 6.8.

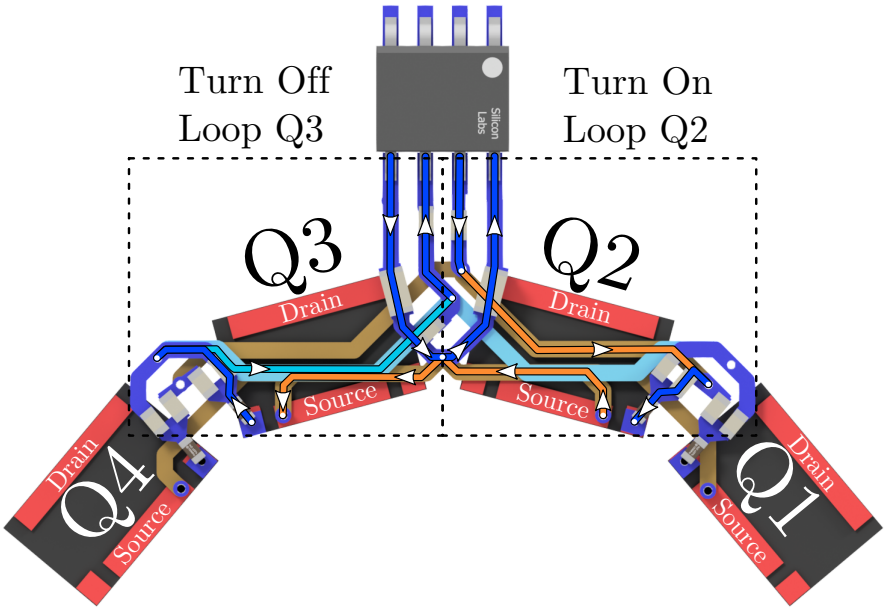


Figure 6.7: The high side GD layout for Design B. The arrows and their corresponding lines indicate the current flow in different gate loops

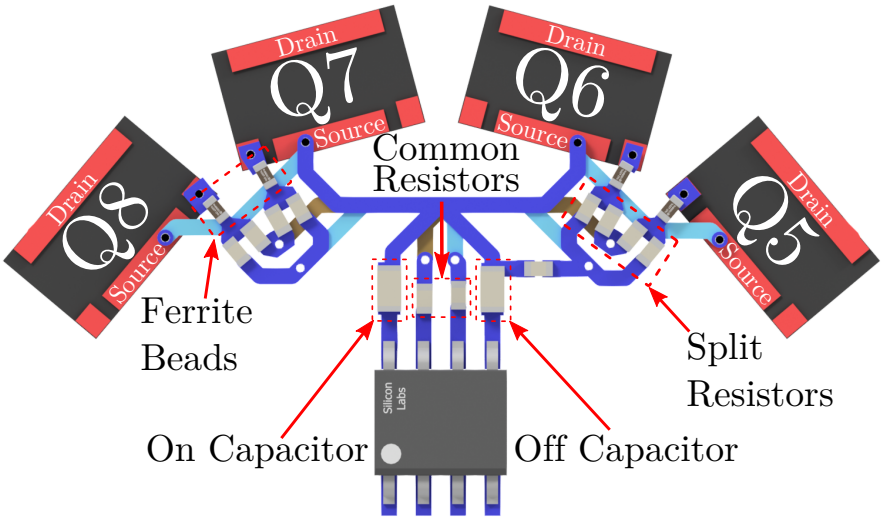


Figure 6.8: The low side GD layout for Design B

The design strategy from Design A is applied to the GD layout of Design B in terms of achieving symmetry and obtaining as much flux cancellation as possible. The same routing method is used in the high side GD as seen in Figure 6.7, where the return path and on loop are routed on the same plane due to the power loop bottom trace seen in Figure 6.6b. For the low side GD it is again possible to obtain cancellation for both the on and off loop due to the advantages of the gate pad placement of the devices.

The difference between Design A and B is that the high and low side loops are much more different in terms of total loop inductance due to the semi-circle layout and the placement of the gate pads to the GD IC. The high side has much longer traces compared to the low side and as there is more

cancellation in the low side as seen in Figure 6.9.

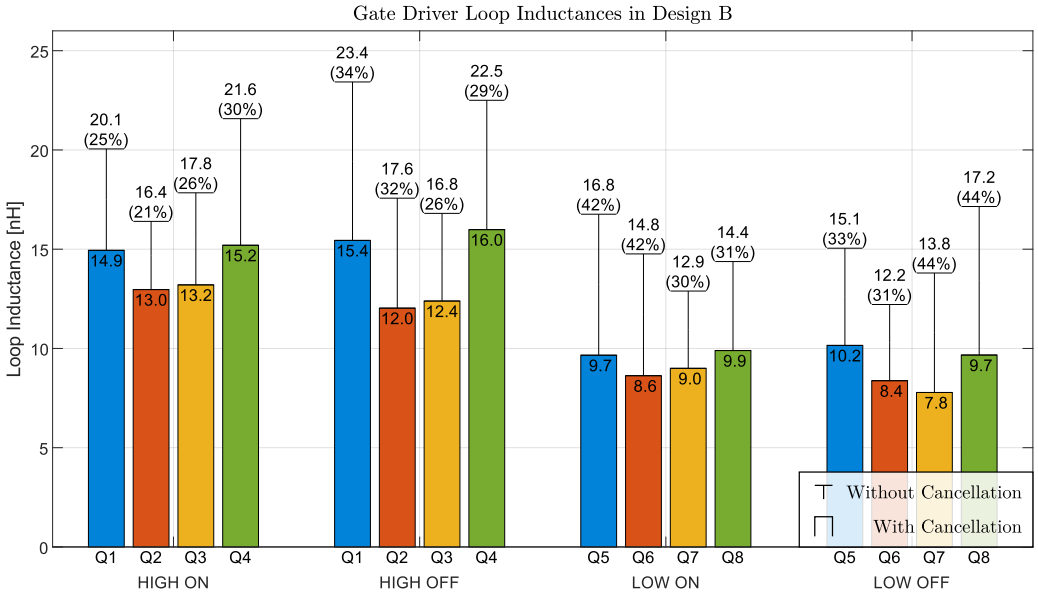
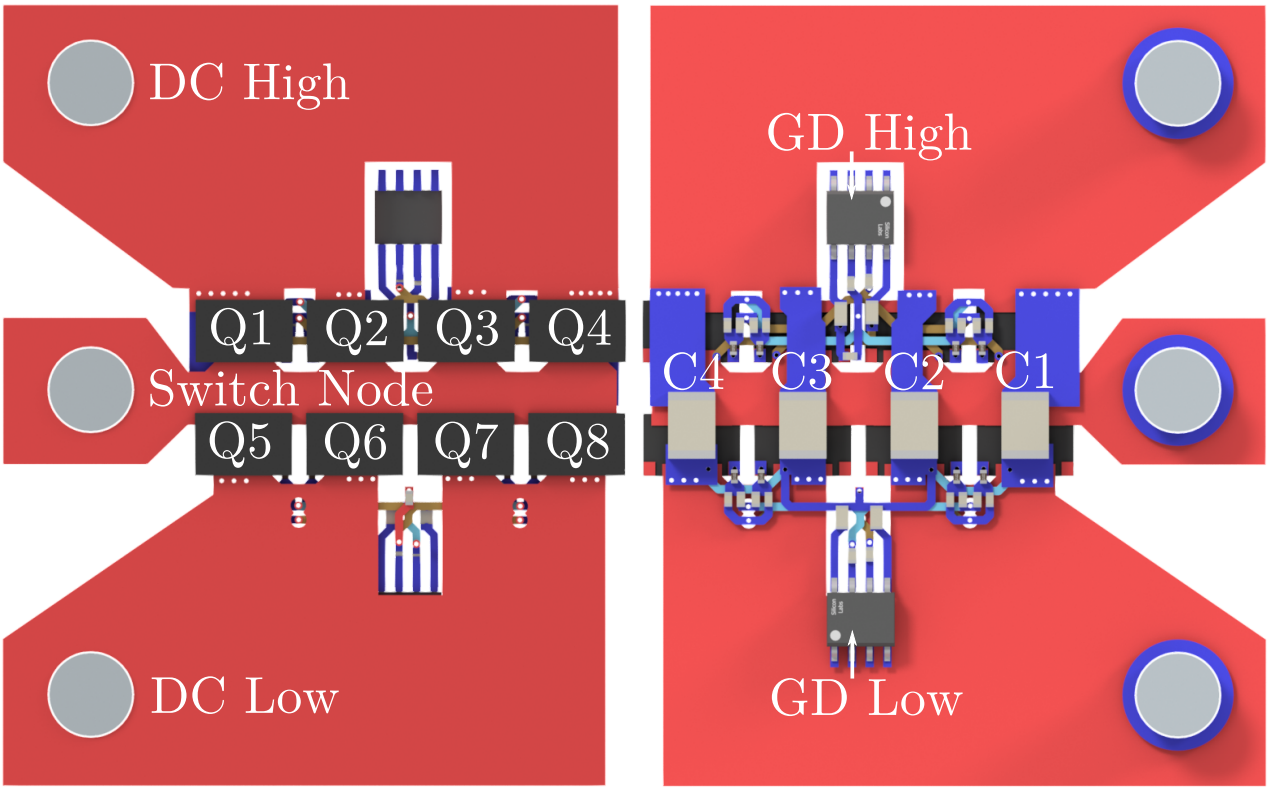


Figure 6.9: GD loop inductances from Design B.

In this design, it can be observed that there is a great difference in the high side and low side loops. The low side loops exhibit much less loop inductance, as well as more symmetry compared to the high side loops. The lower inductance comes as a result of the orientation of the devices, resulting in a shorter distance from the GD to the devices. Conversely, the length from the high side device gate pads to their respective GD is longer, resulting in a higher inductance. It can also be observed that in percentage the flux cancellation is much higher for the low side devices, which again is due to the additional layer possible for routing the GD loops.

6.3 Design C

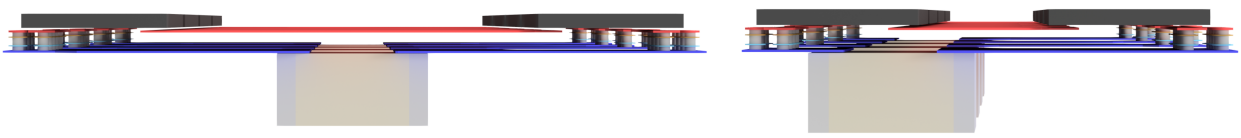
The final design approach is to try to minimise the power loop inductance compared to Design A. The layout strategy will be the same as for Design A, where the devices are placed in a line, but now the distance between high side and low side devices is reduced. This can be seen in Figure 6.10a and 6.10b, where a top and bottom view of Design C is displayed.



(a) The top plane of the PCB of Design C. **(b)** The bottom plane of the PCB of Design C.

Figure 6.10

In Figure 6.10a it can be seen that the SW has been minimised. The high and low side devices are much closer compared to Design A, yielding lower power loop inductances. To do this, the decoupling capacitors had to be placed closer to the low side GaN HEMTs, to make room for the high side GD circuitry, as seen in Figure 6.10b. By comparing the power loops from Design A and Design C, as illustrated in Figure 6.11a and 6.11b, it can be seen that the loop area is reduced when compared to Design A.



(a) The power loop of Design A. **(b)** The power loop of Design C.

Figure 6.11

The GD layout for the high side GaN HEMTs can be seen in Figure 6.12 and low side in Figure 6.13.

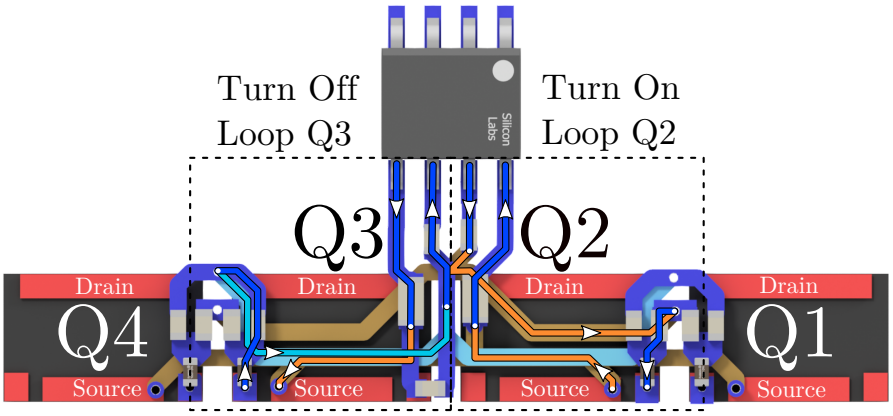


Figure 6.12: The high side GD layout for Design C. The arrows and their corresponding lines indicate the current flow in different gate loops

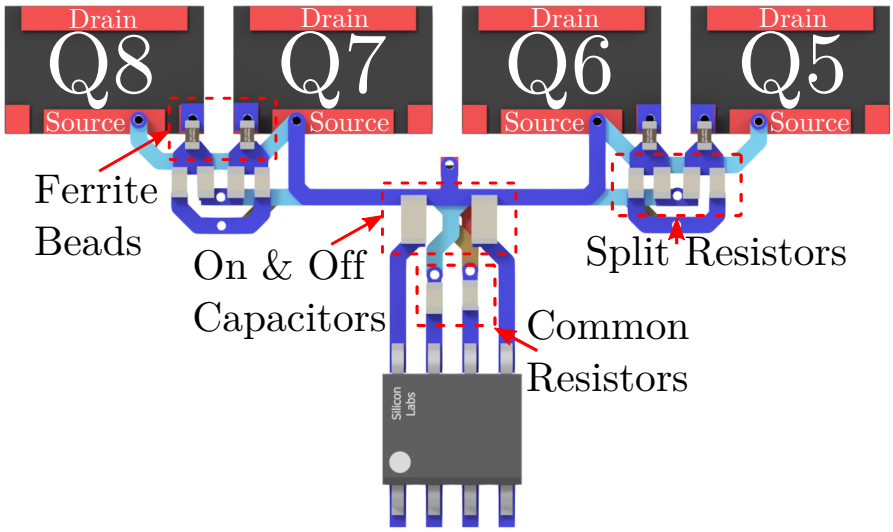


Figure 6.13: The low side GD layout for Design C

The design layout of the GD is almost identical between Design A and C, as primarily the power loop was altered. The extracted loop inductances for the GD can be seen in Figure 6.14.

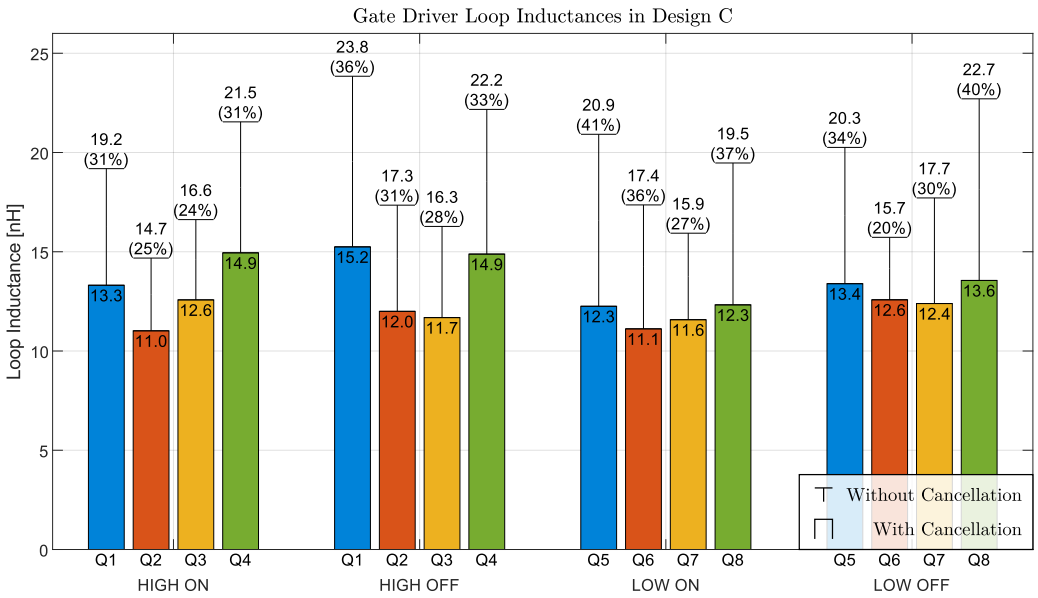


Figure 6.14: GD loop inductances from Design C.

In Figure 6.14 it can be seen that as with Design A, the greatest symmetry is in the low side GD.

One factor that could affect the high side GD layout are the decoupling traces that are routed right below the GD loops. This is not the case for the low side GD, and could be one of the factors that cause the added asymmetry in the high side besides the different routing of the on loop.

6.4 Comparison of Different Designs

In order to compare and evaluate the different design strategies, the power loop inductances will be compared. The power loop is the critical power loop between the high side devices, the low side devices and their respective decoupling capacitors. A schematic of power loop can be seen in Figure 6.15

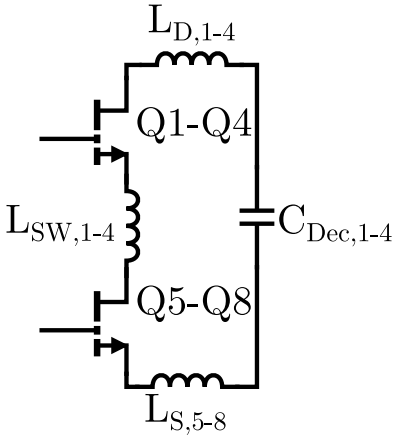


Figure 6.15: Schematic showing the critical power loop of the GaN HEMT HB.

For each of the power loops in Design A, B and C the total loop inductance is comprised of $L_{SW,1-4}$, $L_{D,1-4}$ and $L_{S,5-8}$ and the flux cancellation is also taken into account. This is illustrated for all designs and compared in Figure 6.16

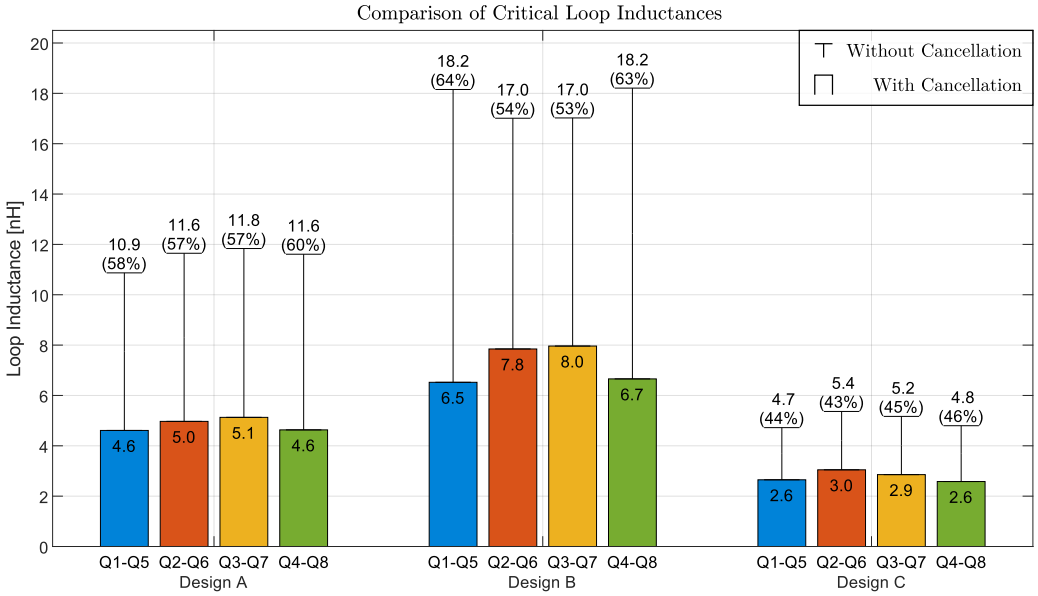


Figure 6.16: Critical loop comparison.

In Figure 6.16 it can be seen that between Design A and C there is a reduction in power loop inductance of approximately 2 nH per loop. It can be seen in Design C that the two inner loops Q2-Q6 and Q3-Q7 exhibit larger loop inductances than the two outer loops, which is thought to be due to the decrease of width in those traces, as seen in Figure 6.10b. It is also evident in Design B that the requirement for minimised and symmetrical source inductances has an impact on the power loop, as it is about 3 nH larger than Design A. However, in terms of utilising the effect of flux cancellation Design A and B is better than Design C. This is due to the increased trace area of Design A and B compared to C, as less trace area leads to lower flux cancellation effects.

To get a better comparison of the different designs and their respective GD loop inductances, these are compared in Figure 6.17. For each area, the average of the four loops is found, and the loops with the highest and lowest inductances are found. This gives an insight into the variance in each area of the different designs.

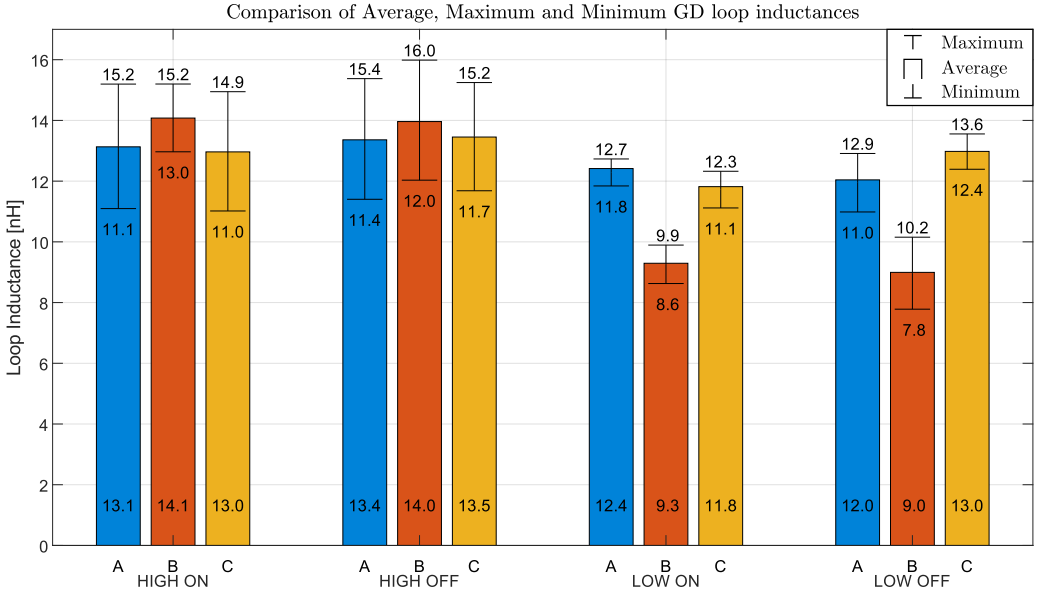


Figure 6.17: Comparison of GD loops in all three designs.

Looking at Figure 6.17, it can be seen that designs A and C have very similar parameters across all four areas of the GD. Especially in the high side loops, with a slightly higher deviance in the low side loops. Moreover, the size of the maximum and minimum loops in each design are comparable for all areas. This similarity is to be expected, as the GD layouts for these designs are similar, whereas the power loops in these layouts differ. Design B can be seen to have higher loop inductances in the high side areas, while having lower inductances in the low side areas, compared to the other two designs. This is to be expected, as the orientation of the GaN HEMT devices is altered. The length from the GD to the devices is longer in the high side areas, and shorter in the low side areas. As the GD loop inductances have an influence on the switching times of the devices, a large variation in these could cause the switching times of the various devices to differ. This could cause some devices to switch earlier than others, sustaining a higher load, resulting in a loading imbalance.

As the primary design approach of Design B was to optimise power side symmetry, the source inductances on the high sides are compared in Figure 6.18. The source inductance is defined as the inductance from the source pad of a device, to its corresponding power plug, e.g. the source pads of the high side devices to the SW plug.

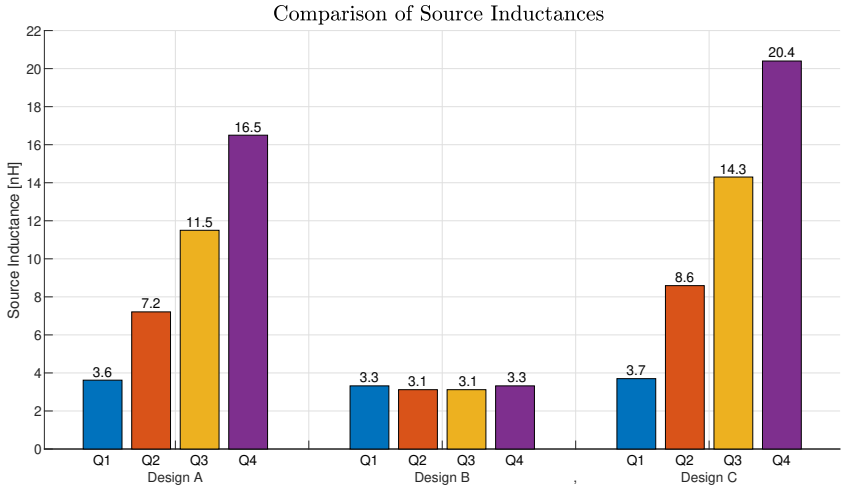


Figure 6.18: Comparison of source inductances.

It can be seen that in Design A and C, there is a large deviation in source inductances, as the device closest to the plug, Q1, has the lowest source inductance. Conversely, Q4 has the highest inductance. However, looking at the source inductances of Design B, it can be seen that they are almost identical, achieving a high level of power side symmetry.

Chapter 7

Thermal Analysis

In this chapter, the thermal characteristics of the three designs will be examined by using the thermal FEA software COMSOL Multiphysics to find the steady state temperature of the PCB and GaN HEMTs. Firstly, the setup of the simulation, the relevant equations and assumptions will be described. Secondly, the results of the thermal FEA will be analysed based on the junction temperature of the individual devices and the heat distribution on the PCB. Furthermore, the average junction temperature of the devices is calculated for different heat transfer coefficients and power loss combinations. This will provide an overview of the required heat transfer coefficient to keep the GaN HEMTs below a given junction temperature at a specific power dissipation.

7.1 Simulation Setup

First, the 3D models of the PCB and the GaN HEMTs, are imported in the software. The PCB layout for each design is imported including the copper and dielectric FR4 layers. The relevant thermal conductivity parameters are then assigned to the specific layers, which is 0.3 W/mK for the FR4 layers and 400 W/mK for copper.

The 3D model of the GaN HEMT is modelled with a high thermal conductivity for the entire package including the die to ensure an equal temperature distribution. The thermal and electrical pads of the top-cooled device are assigned a thermal conductivity equivalent to the thermal resistance provided by the manufacturer, which are 0.5 K/W for the thermal pad and 5 K/W for the electrical pads [42]. The equivalent thermal conductivity is found by rearranging (2.4) on page 15.

$$k = \frac{l}{R_\theta \cdot A} \tag{7.1}$$

Where l represents the thickness of the pads, and A the total area of the pads according to the datasheet [23]. For the thermal pads, the values are directly taken from the datasheet. The thermal resistance of a thin solder layer with a thickness of 60 µm and a thermal conductivity of 60 W/mK is added to the electrical pads. The resulting parameters can be seen in Table 7.1.

	R_Θ [K/W]	l [mm]	A [mm^2]	k [W/m^2K]
Thermal Pad	0.5	0.04	20.15	3.97
Electrical Pads	5.12	0.18	8.61	4.09

Table 7.1: Parameters for calculating the equivalent thermal conductivity of the electrical pads and the thermal pad of the GaN HEMT.

With the geometry and the material properties defined, the thermal properties and boundary conditions can be set. The initial temperature of the system and the ambient temperature is set to 40 °C. It is assumed that each GaN HEMT is dissipating an equal amount of power.

The system is cooled by the heat flux as presented in (7.2).

$$q = h(T_a - T) \tag{7.2}$$

Where h is the heat transfer coefficient in W/m^2K, and T_a is the ambient temperature. Natural convection of $5\,W/m^2K$ [75] is applied to the entire PCB, while a varying h-coefficient is applied to the thermal pad of the GaN HEMTs to represent different cooling solutions. The h-coefficient is typically 100 - $300\,W/m^2K$ for forced air convection, 500 - $2000\,W/m^2K$ for PCBs with a heat sink and $10\,000\,W/m^2K$ or above for water cooled systems [76–81]. The power and the heat transfer coefficient of the thermal pad are then swept to calculate the junction temperature of the different devices.

7.2 Design A

The simulation results for Design A with a power dissipation of 20 W per device and a heat transfer coefficient of $2000\,W/m^2K$ are shown in Figure 7.1.

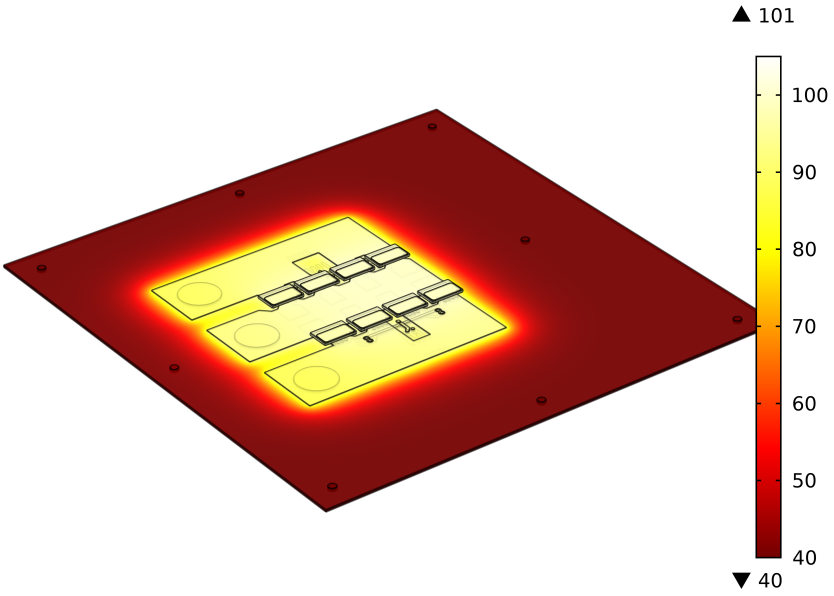


Figure 7.1: Thermal FEA of Design A, with an ambient temperature of 40 °C, a power dissipation of 20 W per device, natural convection of $5\,W/m^2K$ of the PCB, and cooling of the thermal pad with a heat transfer coefficient of $2000\,W/m^2K$. The maximum and minimum temperature values are indicated on top and below the temperature scale. The temperature scale is in °C.

It can be seen that the heat generated by the power dissipation spreads across the copper plane, reaching an average temperature of 97 °C on the SW plane between the two rows of GaN devices. The junction temperature of the individual devices can be seen in Table 7.2.

	Junction Temperature [°C]			
High Side (Q1-Q4)	98.31	99.87	100.47	100.14
Low Side (Q5-Q8)	98.15	99.46	100.13	100.19

Table 7.2: Junction temperature of the GaN HEMTs in Design A, with an ambient temperature of 40 °C, a power dissipation of 20 W per device, natural convection of $5\,W/m^2K$ of the PCB, and cooling of the thermal pad with a heat transfer coefficient of $2000\,W/m^2K$.

It can be seen that the devices further away from the power terminals, i.e. Q3, Q4, Q7, and Q8

experience slightly higher junction temperatures. This can be traced back to the fact that the remaining devices are adjacent to a larger copper area, which dissipates more heat, keeping the area close to the electrical pads of the devices cooler. Furthermore, it can be observed that the coolest devices are Q1 and Q5, indicating that there is a significant effect of mutual heating between the devices, as the remaining GaN HEMTs get warmed by the heat dissipated by the two adjacent devices. However, the junction temperatures do not vary greatly and due to the positive correlation between junction temperature and on-resistance, a warmer device will have a higher on-resistance, resulting in a lower current and thus less power dissipation, which could even out the temperature imbalance. The average junction temperatures of the eight GaN HEMTs are analysed at different power levels and heat transfer coefficients, which can be seen in Figure 7.2

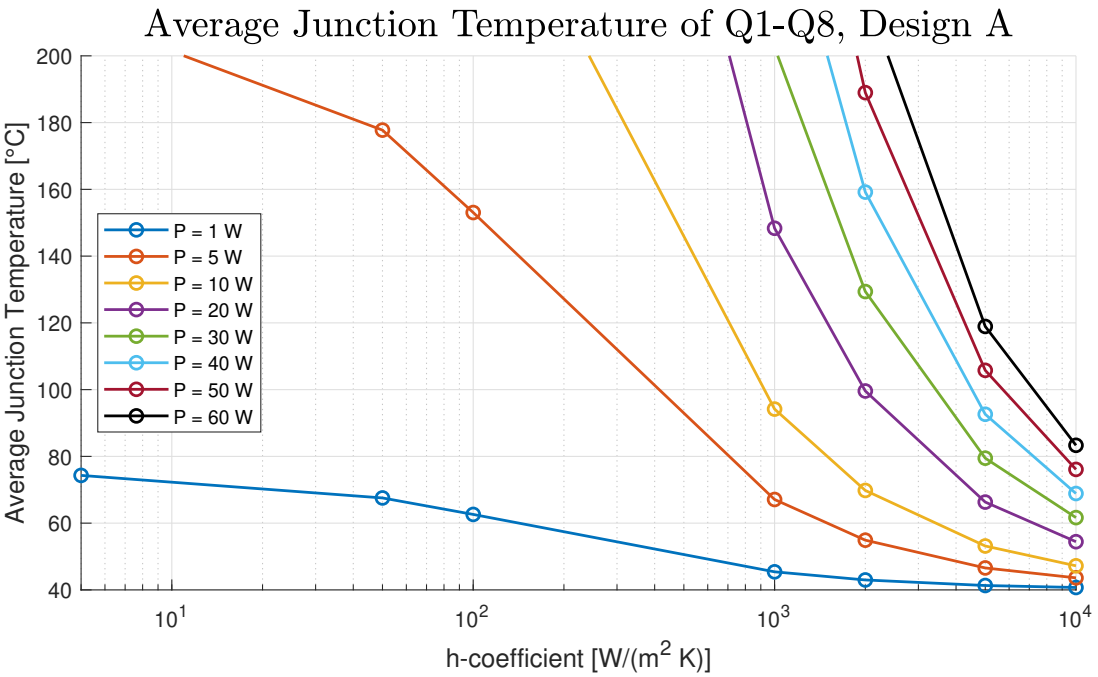


Figure 7.2: Average junction temperature of Q1-Q8 for different power levels and heat transfer coefficients for Design A.

It can be seen in Figure 7.2, that advanced cooling solutions are needed to cool the semiconductors when the dissipated power exceeds 30 W if the junction temperature is not to exceed the absolute maximum rating of 150 °C [23].

7.3 Design B

The simulation results for Design B with a power dissipation of 20 W per device and a heat transfer coefficient of 2000 W/m^2K are shown in Figure 7.3.

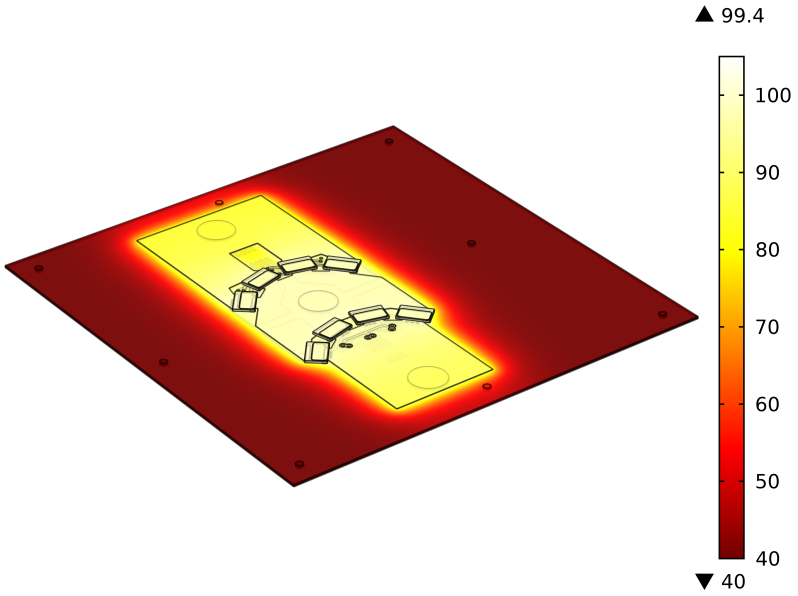


Figure 7.3: Thermal FEA of Design B, with an ambient temperature of 40 °C, a power dissipation of 20 W per device, natural convection of 5 W/m^2K of the PCB, and cooling of the thermal pad with a heat transfer coefficient of 2000 W/m^2K. The maximum and minimum temperature values are indicated on top and below the temperature scale. The temperature scale is in °C.

It can be seen that the heat generated by the power dissipation spreads across the copper planes, reaching an average temperature of 97.85 °C on the SW plane. Generally, Design B reaches lower temperatures due to the increased area of the copper planes and the increased distance between the high side and low side GaN HEMTs, as well as between the devices themselves. The junction temperature of the individual devices can be seen in Table 7.3.

	Junction Temperature [°C]			
High Side (Q1-Q4)	99.41	99.44	99.18	99.40
Low Side (Q5-Q8)	99.18	99.40	99.40	99.18

Table 7.3: Junction temperature of the GaN HEMTs in Design B, with an ambient temperature of 40 °C, a power dissipation of 20 W per device, natural convection of 5 W/m^2K of the PCB, and cooling of the thermal pad with a heat transfer coefficient of 2000 W/m^2K.

It can be seen that the parity of the individual junction temperatures is very high as they only deviate slightly from each other. This is thought to be due to the increased area of the copper plane in the SW and the distance between the devices themselves, which reduces the effect of mutual heating. The average junction temperature of the eight GaN HEMTs is analysed at different power levels and heat transfer coefficients, which can be seen in Figure 7.4.

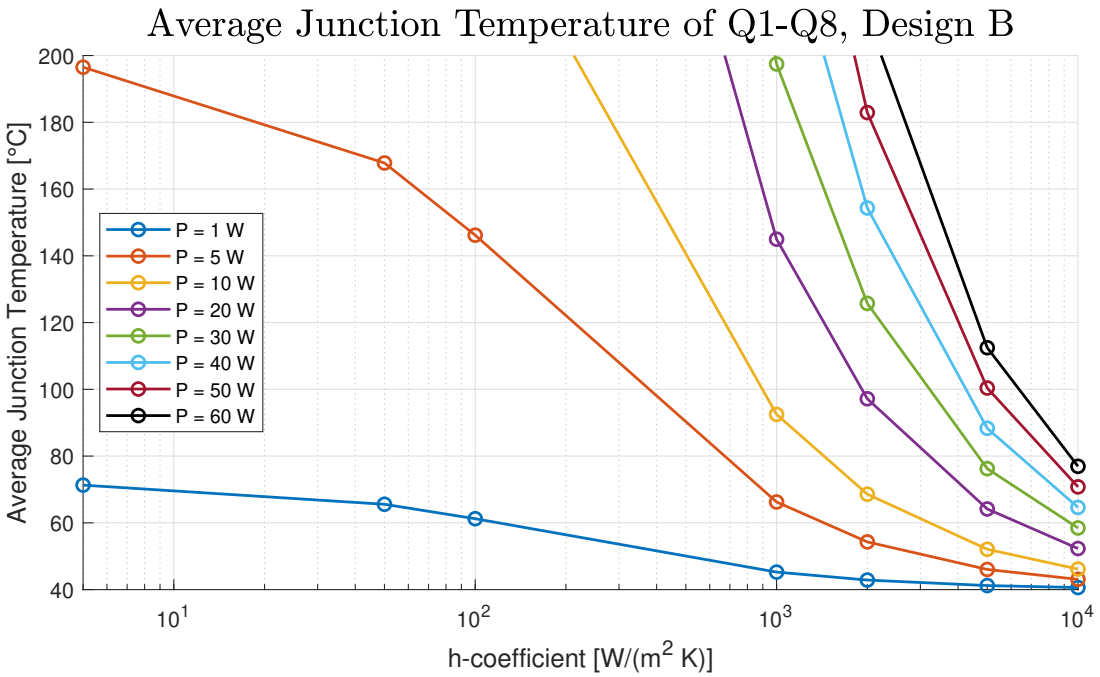


Figure 7.4: Average junction temperature of Q1-Q8 for different power levels and heat transfer coefficients for Design B.

In Figure 7.4, the same tendencies as in Design A can be seen. Albeit the junction temperatures generally are lower in Design B in the same operating points, advanced cooling solutions are needed to cool the devices when the dissipated power exceeds 30 W to keep the junction temperature below absolute maximum rating of 150 °C [23].

7.4 Design C

The simulation results for Design C with a power dissipation of 20 W per device and a heat transfer coefficient of 2000 W/m^2K are shown in Figure 7.5.

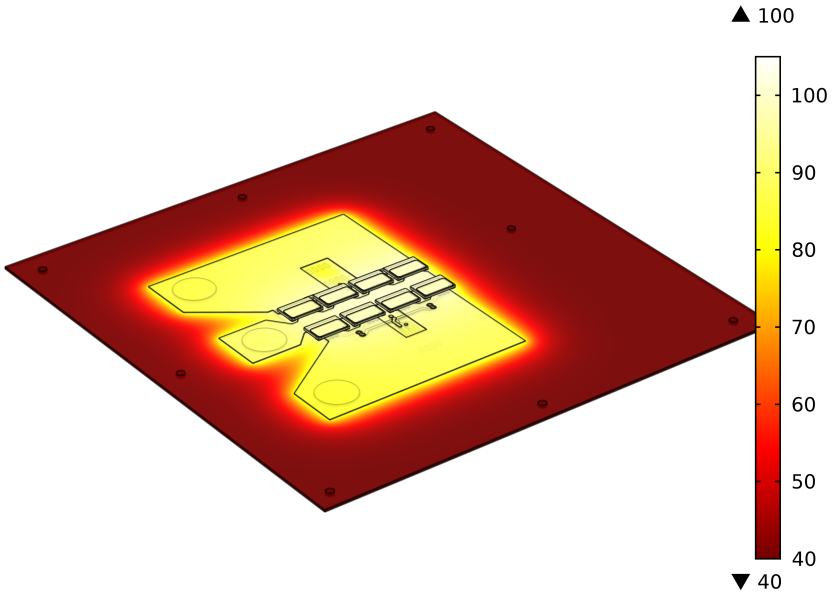


Figure 7.5: Thermal FEA of Design C, with an ambient temperature of 40 °C, a power dissipation of 20 W per device, natural convection of 5 W/m^2K of the PCB, and cooling of the thermal pad with a heat transfer coefficient of 2000 W/m^2K. The maximum and minimum temperature values are indicated on top and below the temperature scale. The temperature scale is in °C.

It can be seen that the heat generated by the power dissipation spreads across the copper planes, reaching an average temperature of 94.88 °C on the SW plane. The junction temperature of the individual devices can be seen in Table 7.4.

	Junction Temperature [°C]			
High Side (Q1-Q4)	97.88	99.81	100.35	99.88
Low Side (Q5-Q8)	97.77	99.41	100.05	99.89

Table 7.4: Junction temperature of the GaN HEMTs in Design C, with an ambient temperature of 40 °C, a power dissipation of 20 W per device, natural convection of 5 W/m^2K of the PCB, and cooling of the thermal pad with a heat transfer coefficient of 2000 W/m^2K.

It can be seen that the parity of the individual junction temperatures are higher in Design C compared to Design A. This is thought to be due to the increased area of the copper planes of the DC High and DC Low nodes, which increases the heat dissipation of those planes. However, the effect of mutual heating can still be observed, as the middle devices experience higher temperatures. The average junction temperature of all GaN HEMTs is analysed at different power levels and heat transfer coefficients, which can be seen in Figure 7.6.

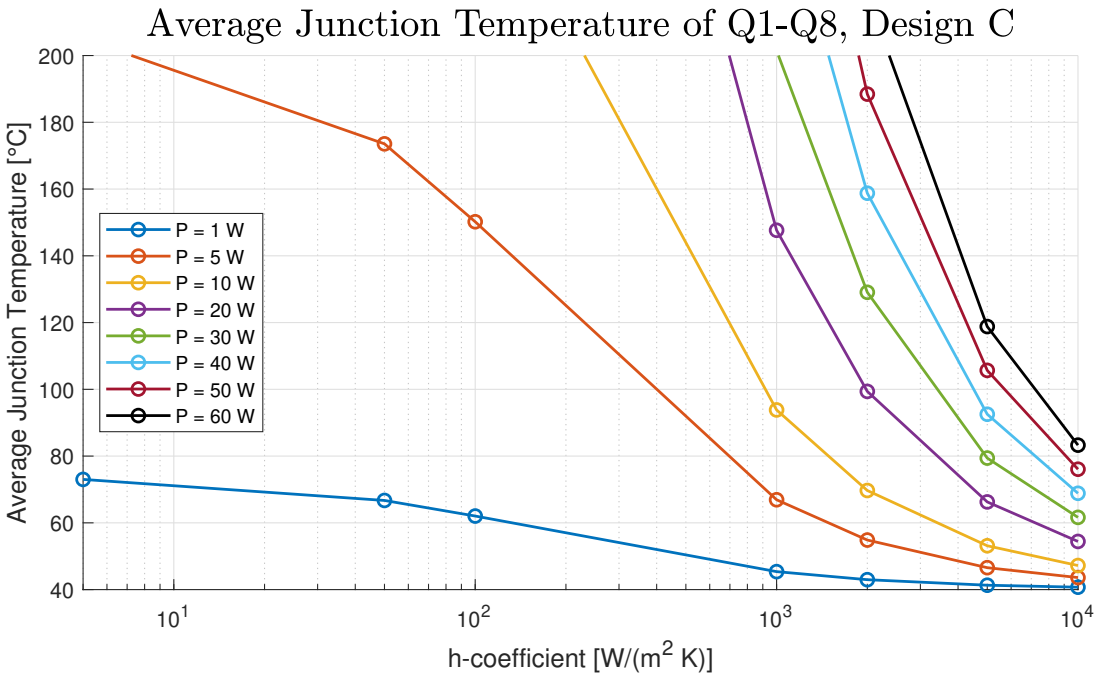


Figure 7.6: Average junction temperature of Q1-Q8 for different power levels and heat transfer coefficients for Design C.

In Figure 7.6, it can be seen that the results do not vary greatly from the results of Design A, leading to the same conclusion. I.e. sophisticated cooling solutions are needed to cool the devices when the dissipated power exceeds 30 W to keep the junction temperature below absolute maximum rating of 150 °C [23].

7.5 Summary

In this chapter, it has been shown how the heat dissipated in the GaN HEMTs distribute on the specific PCB layout and how mutual heating can increase the junction temperature of the middle devices in Design A and Design C. Design B exhibited the best thermal behaviour, as the copper plane of the SW makes out a larger area, resulting in a higher rate of heat flow. This slightly reduces the maximum temperature by 1.6 °C. Furthermore, it can be concluded that cooling the devices becomes a complicated task when the power dissipation of the devices exceeds 30 W.

Chapter 8

Simulation & Optimisation

In this chapter the different designs presented in Chapter 6 will be simulated in LTspice in order to determine how the three designs behave in a simulation. The LTspice circuit and the included component models are elaborated and the simulation results

Based on the initial performance the designs will be optimised through the digital optimisation process explained in Section 4.4, which utilises an integration of LTspice into Matlab. By using Matlab, it is possible to sweep one or several component parameters in the same simulation. This makes it possible to e.g. find a combination of gate resistors which excels in the parameters that are to be optimised, while taking the non-linearities and parasitic components into account. This method will be applied to find the components which have the best compromise of low average power dissipation and high di/dt. It is anticipated that this optimisation approach has the potential to yield very promising results and move the time consuming iterative process proposed by the manufacturer [53] to a digital platform, saving both time and resources.

8.1 LTspice Simulation

The three different PCB designs presented in Chapter 6 are analysed using FEA as explained in Chapter 4, and the results are extracted as a component which can be used in a SPICE simulation in order to simulate the influence of the parasitic components, as described in Section 4.3. The other relevant components and setup of the simulation include:

- Model of the GaN HEMT
- Model of the GD
- Simplified bipolar GD voltage circuit.
- Inductor to test under load
- Dead time generator
- Constant duty cycle

A complete schematic of this LTspice simulation can be seen in Appendix B.2 on page 133 and a simplified schematic can be seen in Figure 8.1.

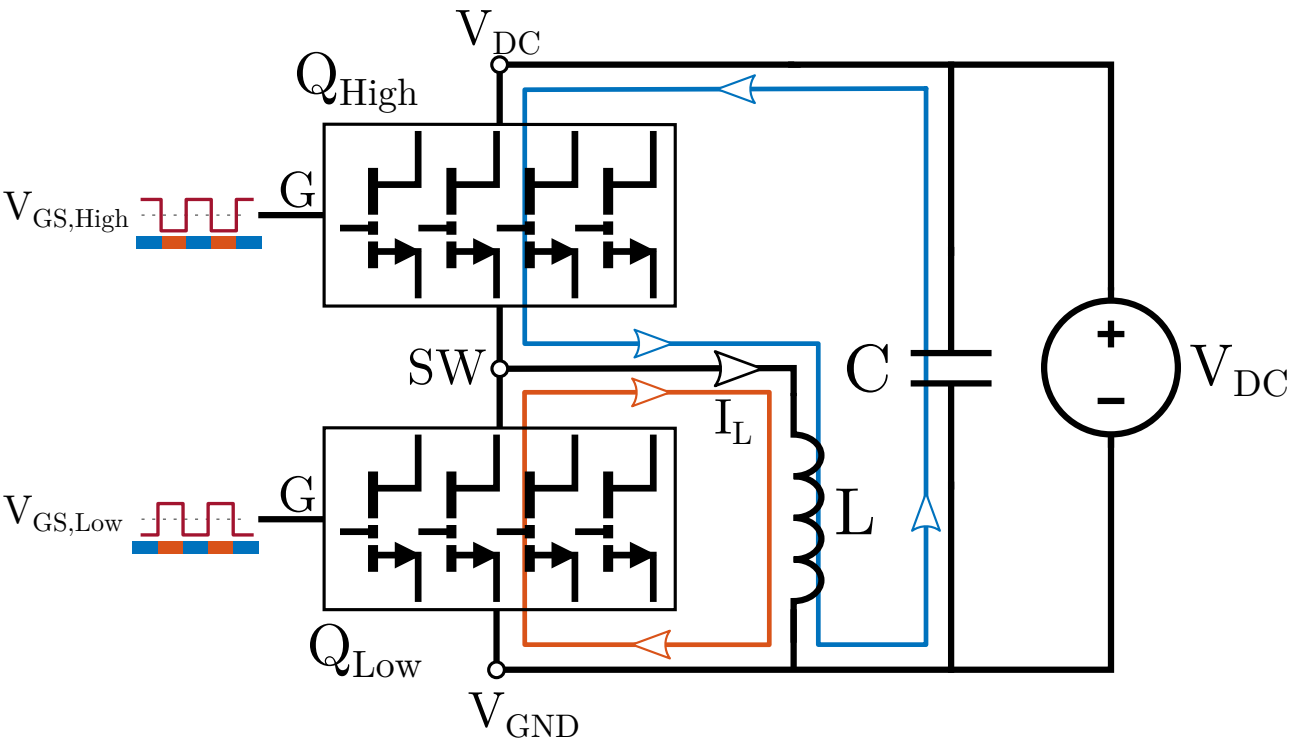


Figure 8.1: Simplified schematic of the circuit used for the optimisation process.

The reason for using the circuit seen in Figure 8.1 is that it allows for switching of both of the devices. This enables an analysis of the switching dynamics, for both high and low side GaN HEMTs, during the optimisation process. This was done to increase the speed of the optimisation process, while still having dynamics similar to that of a DPT.

8.1.1 Model of GaN HEMT

GaN Systems provides a SPICE model for the GaN HEMT GS66508T which is used in this project, including various important properties to represent the transistor, such as the IV performance as a function of temperature, a thermal network, intrinsic voltage dependent capacitances and the intrinsic inductances of the package [82].

8.1.2 Model of the Gate Driver

The bipolar GD described in Section 5.1 is simplified for LTspice simulation and is modelled without propagation delay or rise and fall times as two ideal switches alternating between the on gate supply voltage and the off gate supply voltage. However, it includes the static on-resistances of the high and low output transistors, which are 2.7 and 1 Ω respectively. The bipolar voltage is supplied by two capacitors with the respective initial voltage of 6 V for V_{DD} and −3 V for V_{EE}. To simplify the simulation, the DC/DC converters, and Zener diodes are not included in the simulation.

8.1.3 Inductive Load

At the SW between the high and low side GaN HEMTs, an inductor is connected to the DC low node, as seen in Figure 8.1, in order to build up current and switch under load. The inductor is modelled to reach a very large inductance at around 100 A, while remaining at very low inductance at lower currents. This allows the current to build up quickly to the desired switching value of 25 A per device, and keeping it constant after that value is reached. This is done in order to reduce simulation times. Figure 8.2 shows the current dependency of the inductor used in the simulation.

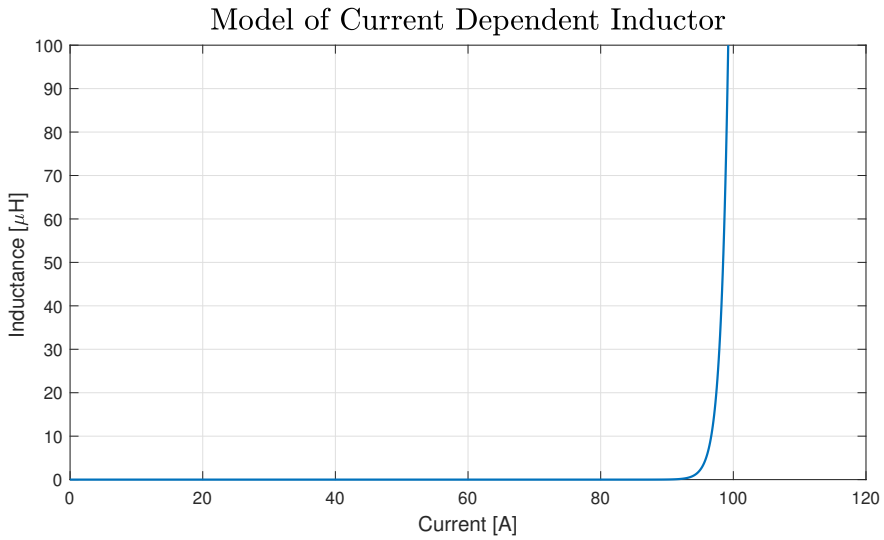


Figure 8.2: Current dependency of inductor used in simulation.

The exponential function used to achieve this behaviour is given by:

$$L(I_L) = 192.46 \cdot 10^{-45} \cdot 2.4557^{I_L} \tag{8.1}$$

With this current dependent inductor, both the high and the low side devices can be investigated during turn-on and turn-off while under load. In order to avoid a short circuit, a dead time of 100 ns is implemented as well. The LTspice simulation schematic can be seen in Appendix B.2 on page 133.

8.2 Simulation Results

Three circuits are simulated with the PCB layout of Design A, B, and C, respectively. They are switched under minimal load below 100 mA and without any FB to examine how the circuit behaves under minimal load before increasing the current to the desired value. The gate resistances used are 10 Ω as the common on-loop resistance, 100 mΩ as the common off-loop resistance, and 11 Ω for the split resistor for both the on and off-loop.

Design A

The simulation results of the circuit including the parasitics of Design A at low load are shown in Figure 8.3.

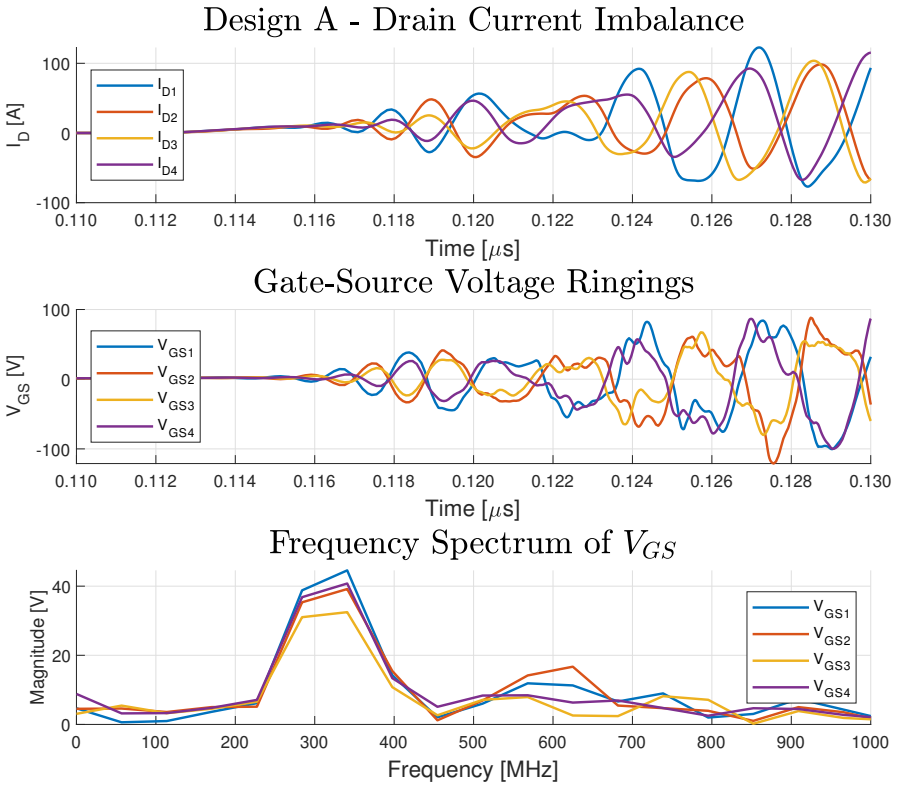


Figure 8.3: Simulation Results of Design A with no FB. Switching under low load.

It can be observed that the drain currents in the high devices start oscillating, and that the oscillations seem to occur in pairs. This is assumed to originate from the symmetry of the GD circuit, where Q1 & Q4, and Q2 & Q3 share approximately the same distance and a similar gate loop inductance, as seen in Figure 6.5 on page 53. The instability can further be observed in the gate-source voltage ringings of the high devices, which oscillate similarly. It has to be noted that the voltages greatly exceed the voltage limits of the devices.

To investigate the frequency content of the oscillations, a Fast Fourier Transform (FFT) of the gate-source voltages is conducted. The results show large frequency contents in the range of 340 MHz, and

at 620 MHz.

Design B

The simulation results including the parasitics of Design B at low load are shown in Figure 8.4.

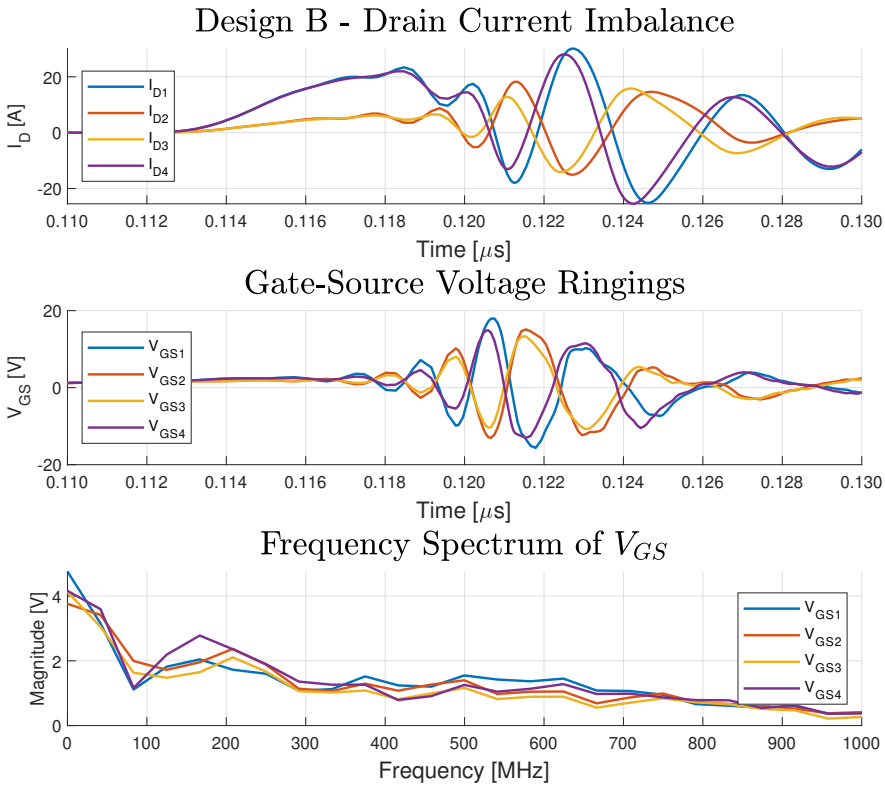


Figure 8.4: Simulation Results of Design B with no FB. Switching under low load.

As in Design A, it can be observed that there are significant imbalances in the drain current distribution caused by asymmetry in the gate loop. However, the magnitudes of these oscillations, both in the drain current and the gate-source voltage are significantly lower than in Design A. However, the oscillations are still great enough to exceed the voltage rating of the devices, which would lead to a defect circuit. The most significant oscillations occur in the range of 160 MHz.

Design C

The simulation results including parasitics of Design C at low load are shown in Figure 8.4.

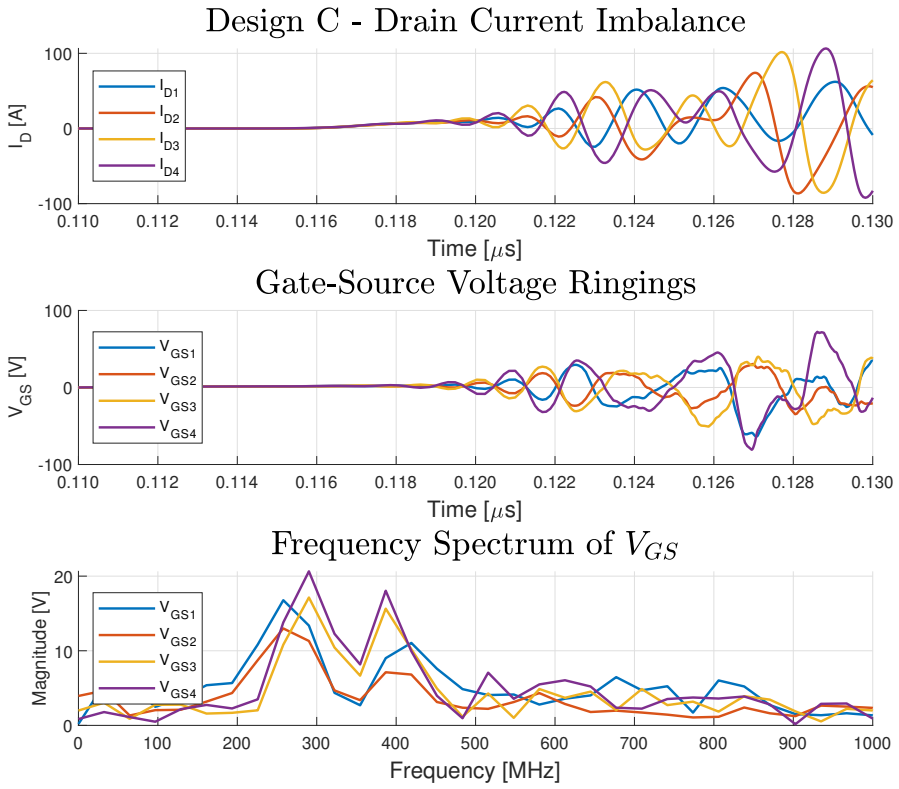


Figure 8.5: Simulation Results of Design C with no FB. Switching under low load.

The same trends as in Design A & B can be observed in Design C. The amplitude of the oscillations is similar to Design A, which can be explained by the similarity in GD circuitry of the two designs. However, it can be noted that the oscillation frequencies are not as similar for all devices as they were for Design A. The most significant oscillations are in the range of 260-290 MHz and 380-420 MHz.

The frequency spectrum of V_{GS1} of all three designs is shown in Figure 8.6.

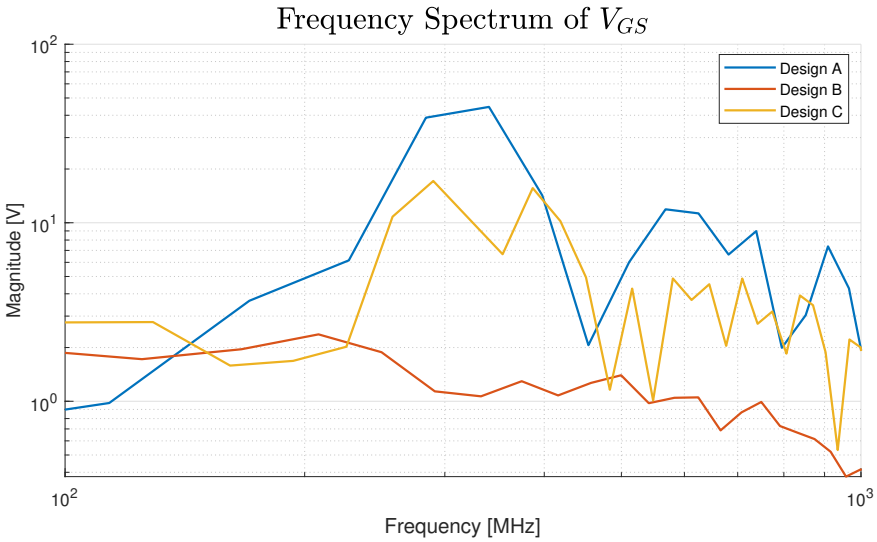


Figure 8.6: Frequency spectrum of the gate-source voltage of Q1, for all three designs.

It can be seen that Design A & C have a similar range of frequencies with significant magnitude, but that the magnitude of the oscillations of Design A are around three times as intensive. The magnitude of the oscillations of Design B are, however, much lower. As mentioned in Section 5.1.8 on page 42 FB can be a solution to dampen these oscillations and this will be investigated using the optimisation process mentioned in Section 4.4 on page 31

8.3 Choice of Ferrite Beads

In order to find the most suitable FB for each design, the circuits are simulated with various FBs in the appropriate package size of 0402. The list of the 26 different FBs and their lumped circuit parameters can be found in Appendix C. The simulation results are first evaluated for their stability. The stable simulations are then evaluated by comparing the average power dissipated, as calculated by (4.6) on page 32, during switching and conduction, and the rate of change of the drain current, i.e. di/dt, for both turn-on and turn-off. Pareto optimisation is applied to find a FB with the lowest dissipated average power and the highest di/dt, as explained in Section 4.4.1 on page 32.

Design A

The results of this process for Design A can be seen in Figure 8.7.

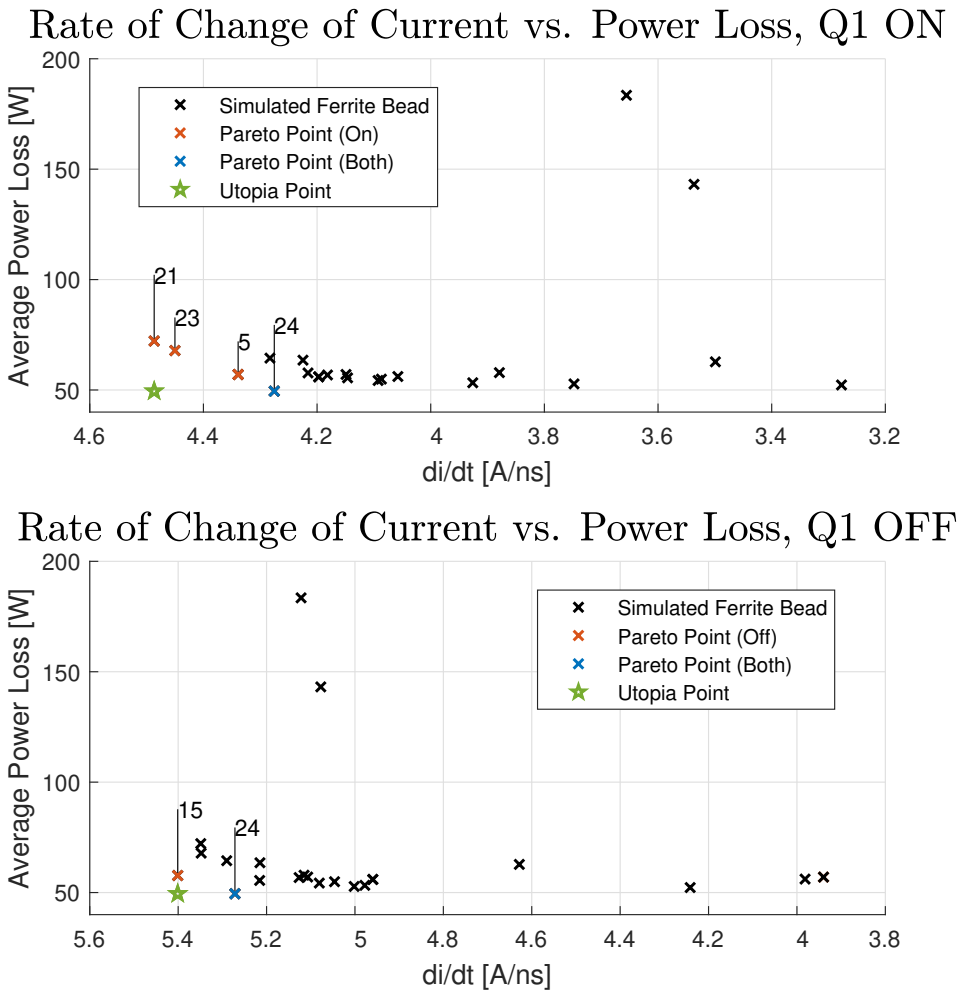


Figure 8.7: Average power loss and di/dt of drain current of the different FBs for turn-on and turn-off for Design A.

Figure 8.7 shows the data points from the simulations of all FBs. For the turn-on sequence, the pareto points include the following FBs from the list presented in Appendix C. 21, 23, 5, and 24. For the turn-off sequence, it includes FB 15 & 24. FB 24, which is Würth Elektronik's 782422331 WE-CBA 0402, is deemed to be the most suitable FB for Design A, as it is a pareto optimal point in both turn-on and turn-off, which results in a balanced compromise of highest di/dt and lowest power dissipation.

Design B

The process is repeated for Design B, which can be seen in Figure 8.8

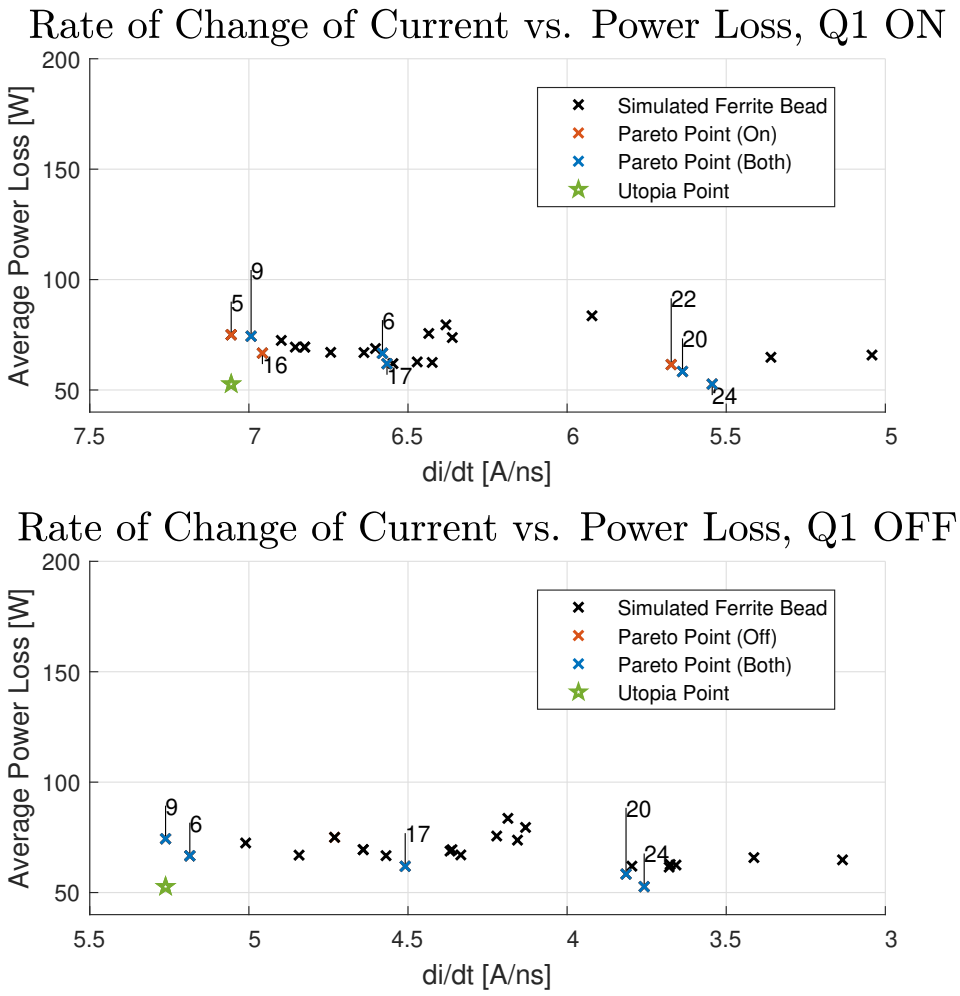


Figure 8.8: Average power loss and di/dt of drain current of the different FBs for turn-on and turn-off for Design B.

It can be seen that FB 9, which is Würth Elektronik's 742792716 WE-CBF 0402, shows excellent performance during both turn-on and turn-off, as it is very close to the utopia point of both sequences. It will therefore be chosen as the most suitable FB for this design.

Design C

The simulation results for Design C can be seen in Figure 8.9.

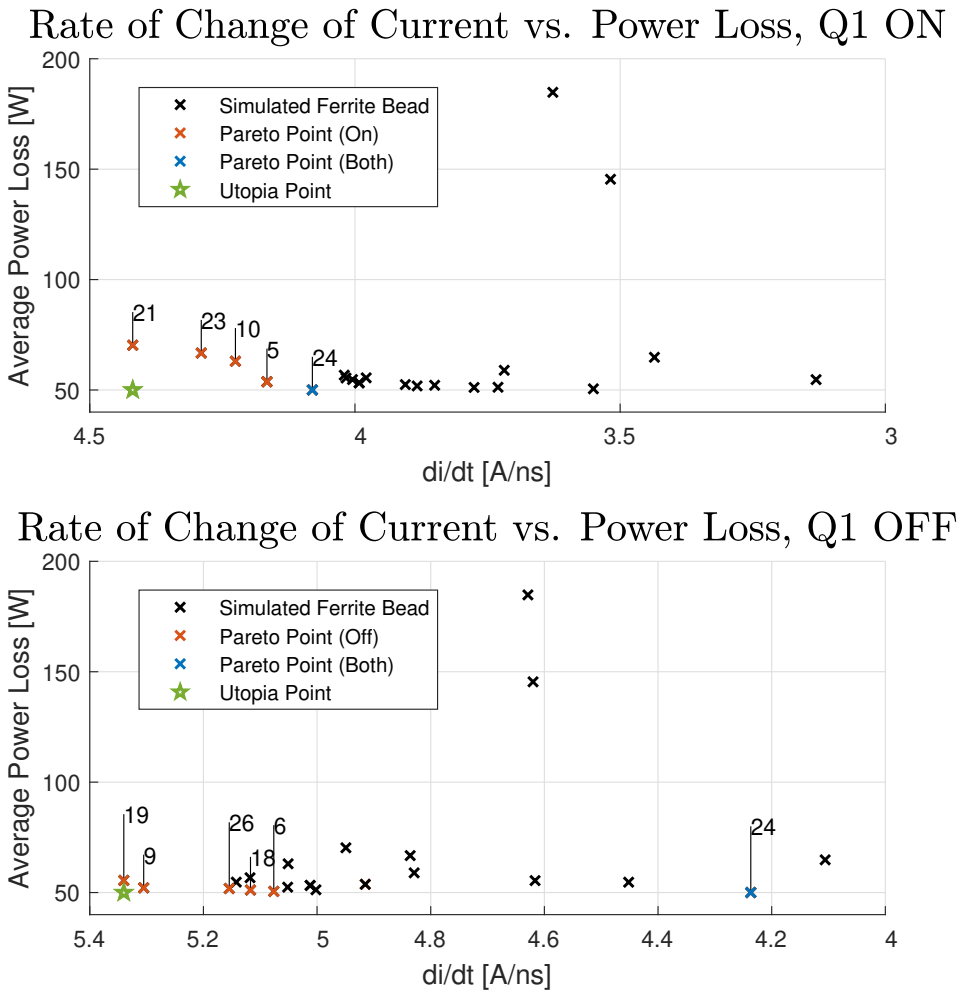


Figure 8.9: Average power loss and di/dt of drain current of the different FBs for turn-on and turn-off for Design C.

As FB 24 is a pareto optimal point in both turn-on and turn-off, it is chosen as the most suitable FB for this design. Even though the di/dt is not at the highest rate for Design C with FB 24, the dissipated power is minimal.

8.4 Gate Resistors

The simulations for choosing the FB have been conducted with a generic set of gate resistors, with 10 Ω as the common on-loop resistance, 1 mΩ as the common off-loop resistance, and 11 Ω for the split resistor for both the on and off-loop. To find a combination of gate resistors which further enhances the performance of the circuit, a similar simulation analysis is conducted for different values of common and split resistors. The optimal FBs for each design are used to find a combination of gate resistors shown in 5.6 on page 40.

8.4.1 Common Gate Resistors

In a first sweep, the influence of the common resistance is examined for Design A. The most efficient combination of common resistors in terms of di/dt and dissipated average power will then be kept for finding the most efficient combination of split gate resistors in the remaining two designs.

In Figure 8.10, different combinations of split and common gate resistances are simulated and analysed, where the common gate on-resistance is varied from 10 Ω and 100 mΩ, while the common gate off-resistance is omitted, as suggested by [83].

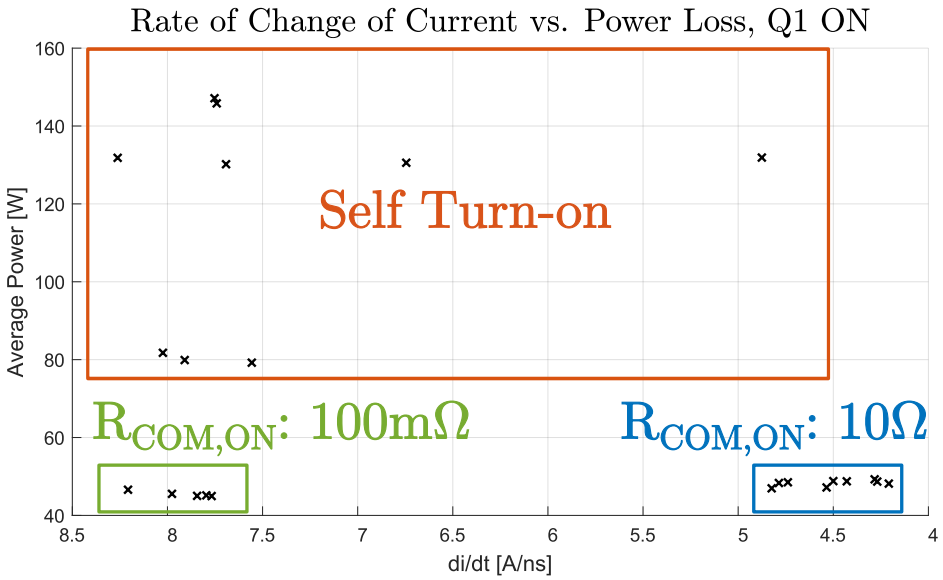


Figure 8.10: Influence of common gate on-resistance in terms of average power dissipated and di/dt.

It can be seen that the simulations with a significantly lower common gate on-resistance, i.e. when it is reduced from 10 Ω to 100 mΩ, have a much higher di/dt, while dissipating less power. Thus, a low common gate on-resistance is preferred. Furthermore, it can be seen that certain combinations of gate resistances lead to self turn-on and therefore significantly increase the dissipated power. This can be traced back to low split gate off-resistances, which lead to gate-source voltage oscillations that exceed the threshold voltage.

8.4.2 Split Gate Resistors

The split gate resistances are varied for the three designs, while the common on-resistors are kept at 100 mΩ and the common off-resistor is omitted, to find the most suitable combination according to the same criteria as presented before.

Design A

The split resistor combinations shown in Table D.1 on page 135 are analysed in terms of average dissipated power and di/dt, as seen in Figure 8.11.

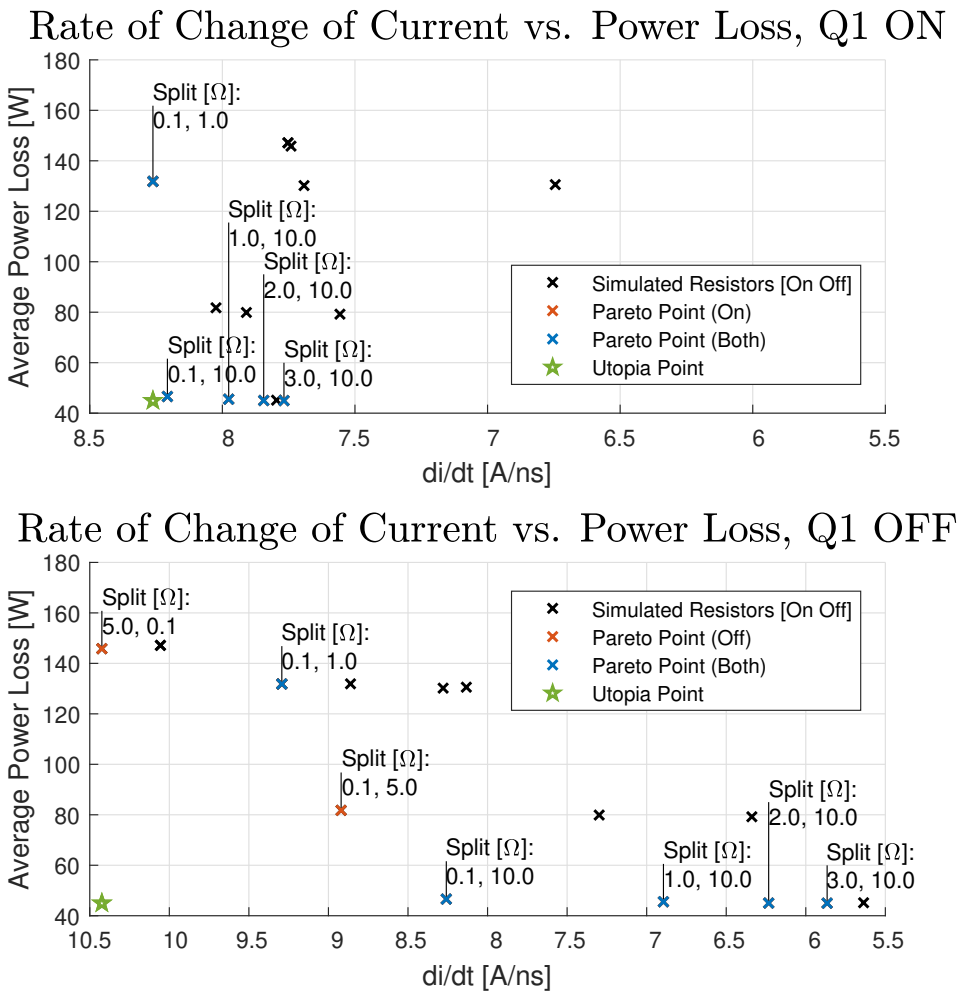


Figure 8.11: Average dissipated power and di/dt of drain current for turn-on and turn-off for Design A with different split gate resistors. **Note:** Resistance values are displayed in the format [On, Off].

It can be seen that there are various pareto optima for both turn-on as well as turn-off. The combination 0.1 & 10 Ω lies very close to the utopia point of turn-on, and has minimal power dissipation. Therefore, 0.1 & 10 Ω is deemed to be the most suitable combination of split gate resistors.

The switching performance for Design A with the optimised FB and gate resistors can be seen in Figure 8.12, where the switching performance is evaluated at 400 V and a drain current of 25 A on

each of the GaN HEMTs.

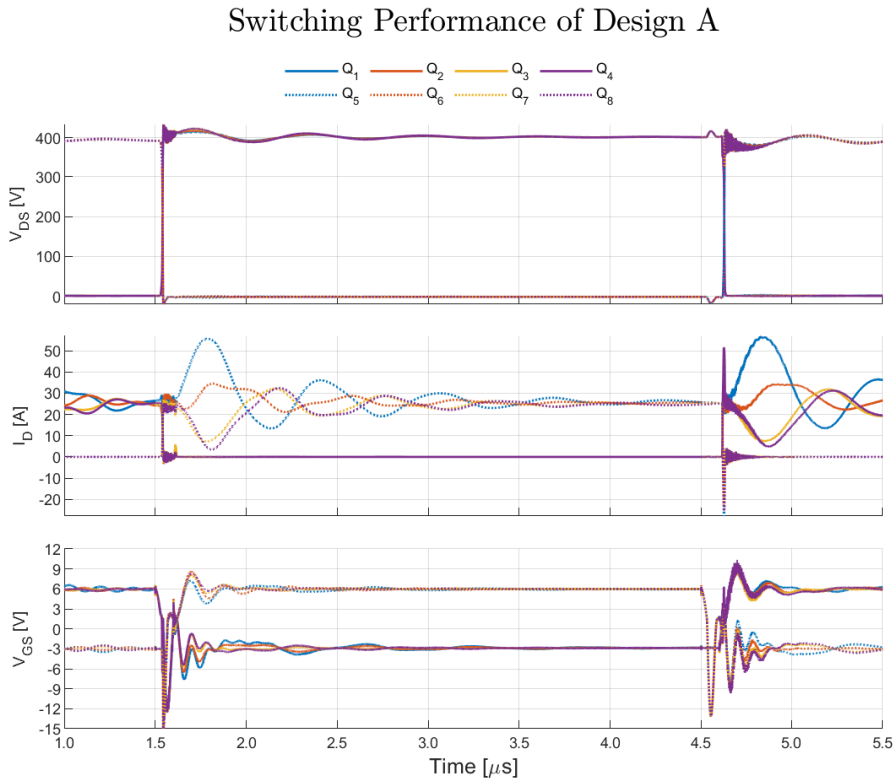


Figure 8.12: Switching performance under load of Design A after power dissipation and di/dt optimisation.

At the first switching instance in Figure 8.12, at 1.5 µs the high side devices turn off and the low side turn on. The drain-source voltages of the high side devices can be seen to have a small overshoot, but settle quickly. The low side drain-source voltages turn off with a very small undershoots and stabilise. This is almost the same case at the second switching, where the low side devices turns off.

The drain current can be seen to oscillate at both switching instances and a current imbalance is evident for both the high and low side during turn-off. Especially for Q1 and Q5, where a large current of approximately 55 A can be seen. This is not desirable, but it is within the limits of the chosen GaN HEMT [23]. This is thought to be due to the asymmetry of the source inductances as discussed in Section 2.2 on page 5. It can be observed that these oscillations eventually settle.

The gate-source voltage can be seen to oscillate significantly for both turn-on and turn-off at both switching instances. This is especially clear in Figure 8.13.

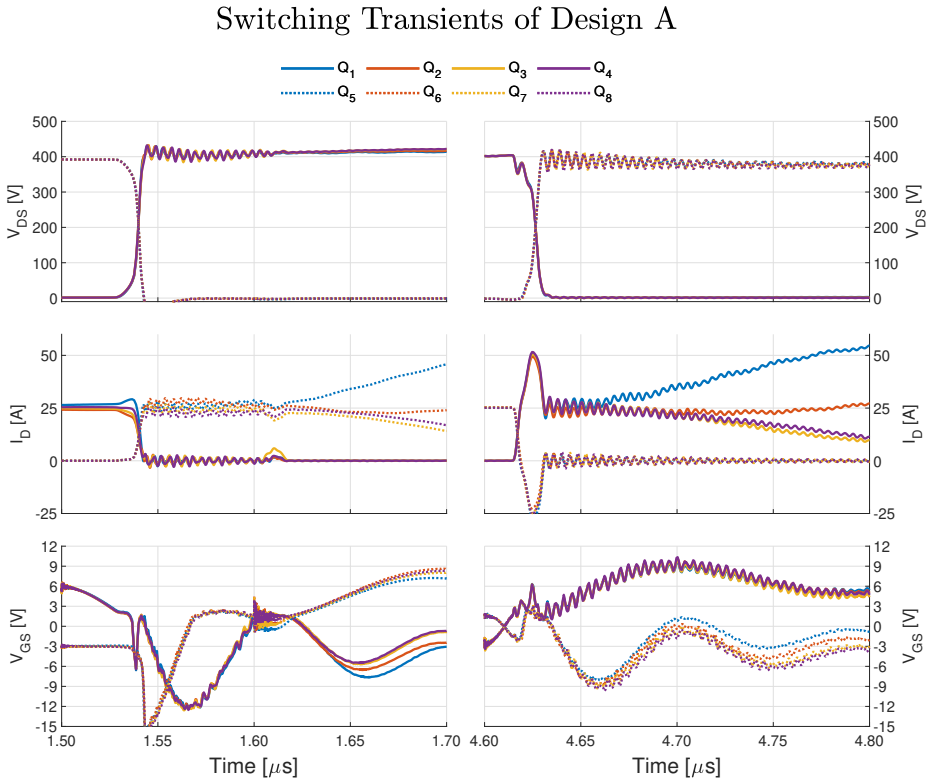


Figure 8.13: Switching transients under load of Design A after power dissipation and di/dt optimisation.

In Figure 8.13, it can be seen that the gate-source voltages have a lot of ringings and the high side gate-source voltage even has self turn-on at 1.6 µs. This is very undesirable as this can potentially create short circuits and cause instant breakdown of the devices. However, as the simulations for the optimisation was done with an off-voltage of −3 V and the experimental setup will be with −6 V, as mentioned in Section 5.1.1 on page 35, it is deemed that this will be sufficient to keep it stable.

The switching performance parameters, such as overshoot, di/dt, dv/dt, switching energy, and average power dissipation for Design A are listed in Table 8.1.

Design A	**Mean**	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**	**Q8**
V_{DS} OS [%]	6.28	7.45	8.23	8.18	8.07	3.19	4.71	5.19	5.23
I_D OS [%]	81.60	127.14	97.53	102.44	106.31	123.13	38.35	28.38	29.53
di/dt (on) [A/ns]	6.40	8.21	8.22	8.48	8.57	5.47	4.90	4.28	3.09
di/dt (off) [A/ns]	6.64	8.26	2.30	3.25	5.41	9.14	7.95	8.16	8.66
E_{sw} (on) [µJ]	70.76	133.32	130.44	132.33	135.08	8.76	8.71	8.72	8.73
E_{sw} (off) [µJ]	23.34	20.60	14.73	15.30	17.20	33.37	26.17	29.52	29.85
P_{avg} [W]	42.55	46.60	41.32	42.95	41.07	44.22	40.85	41.89	41.51
dv/dt (on) [V/ns]	51.71	60.58	56.61	54.57	55.05	46.90	46.51	46.97	46.51
dv/dt (off) [V/ns]	45.50	37.46	37.51	37.09	36.95	56.11	53.87	52.34	52.70

Table 8.1: Switching performance parameters of Design A for all switching devices.

Design B

The split resistor combinations shown in Table D.2 on page 136 are analysed in terms of average dissipated power and di/dt, as seen in Figure 8.14.

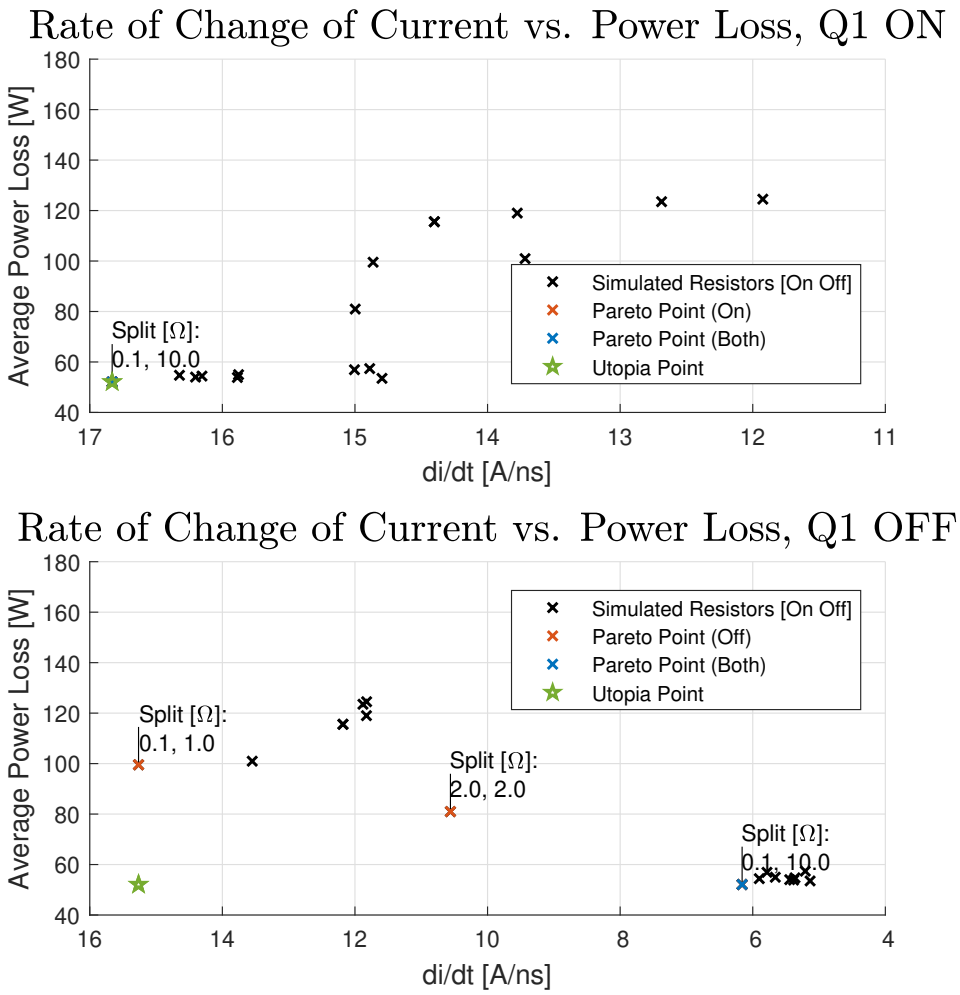


Figure 8.14: Average dissipated power and di/dt of drain current for turn-on and turn-off for Design B with different split gate resistors. **Note:** Resistance values are displayed in the format [On, Off].

As the combination of 0.1 & 10 Ω is a pareto optimum point for both turn-on and turn-off, it is deemed the most suitable combination of split gate resistors to guarantee fast and efficient switching during both turn-on and turn-off. Moreover, this combination lies on the utopia point for turn-on, which makes it the optimal simulated combination for turn-on.

The switching performance for Design B with the optimised FB and gate resistors can be seen in Figure 8.15.

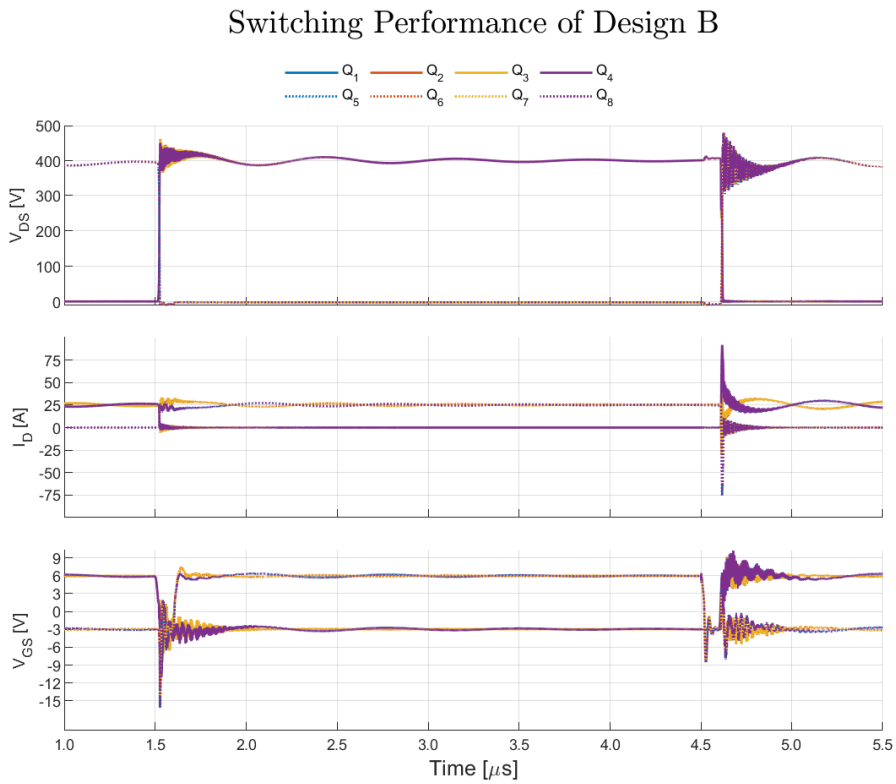


Figure 8.15: Switching performance under load of Design B after power dissipation and di/dt optimisation.

In Figure 8.15, it can be observed that the drain-source voltages have a higher overshoot than Design A, which is due to the increased power loop inductances of Design B. However, it remains within a reasonable limit and is far from the 650 V SOA of the GaN HEMTs [23].

On the drain current, it can be seen that due to the increased source symmetry there is a much better current distribution. From both switching instances, it can be seen that the current of Q1 % Q4 oscillate together, and conversely, Q2 % Q3. Again, this is due the source symmetry between the source pads and the power terminals, as seen in 6.18 on page 61.

The gate-source voltages can again be seen to have the same oscillations in both switching instances. This is illustrated more clearly in Figure 8.16.

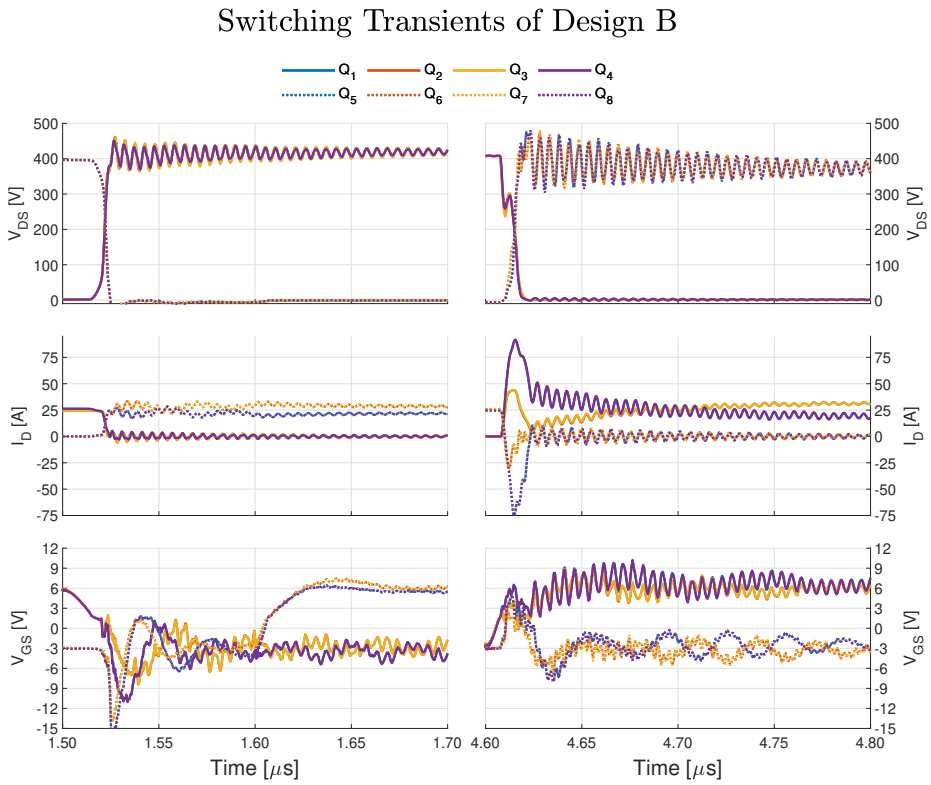


Figure 8.16: Switching transients under load of Design B after power dissipation and di/dt optimisation.

It can be observed that as the low side devices enter reverse conduction after the switching instance, there is a slight self turn-on. This does not have such a significant effect, as it simply turns the reverse conducting GaN HEMTs on, which can be seen by the slight increase in the low side drain-source voltage and decrease in high side drain-source voltage. The gate-source voltage at the second switching instance is more stable and the high increase on both drain-currents is due to the gate-drain and output capacitances which are charging and discharging after switching. It can be noted that the drain currents reach an amplitude of about 85 A for high side and −75 A for low side devices. This increase compared to Design A could be due to the added capacitive coupling between both the high and low side to the switch node. As the switch node and the traces to the decoupling capacitors have a larger overlapping area, a larger parasitic capacitance s created, as explained in Section 5.3.4.

The switching performance parameters, such as overshoot, di/dt, dv/dt, switching energy, and average power dissipation for Design B are listed in Table 8.2.

Design B	Mean	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
V_{DS} OS [%]	16.70	13.03	15.41	14.99	12.81	19.03	18.33	19.99	20.04
I_D OS [%]	144.50	266.70	75.82	75.84	266.64	204.14	33.55	34.24	199.06
di/dt (on) [A/ns]	11.08	16.83	11.82	11.19	18.99	7.99	7.37	6.91	7.58
di/dt (off) [A/ns]	11.34	6.16	10.16	9.52	5.80	13.53	15.45	16.21	13.87
E_{sw} (on) [µJ]	54.41	129.67	72.95	71.76	126.58	8.57	8.58	8.58	8.57
E_{sw} (off) [µJ]	28.26	12.57	12.41	12.31	12.48	72.09	16.52	15.54	72.17
P_{avg} [W]	61.57	52.09	47.26	47.93	52.24	84.41	61.60	61.61	85.45
dv/dt (on) [V/ns]	66.96	74.53	64.89	64.19	72.58	69.94	60.95	61.27	67.34
dv/dt (off) [V/ns]	51.44	35.40	34.12	34.30	35.88	68.05	68.42	67.96	67.39

Table 8.2: Switching performance parameters of Design B for all switching devices.

Design C

The split resistor combinations shown in Table D.3 on page 137 are analysed in terms of average dissipated power and di/dt, as seen in Figure 8.17.

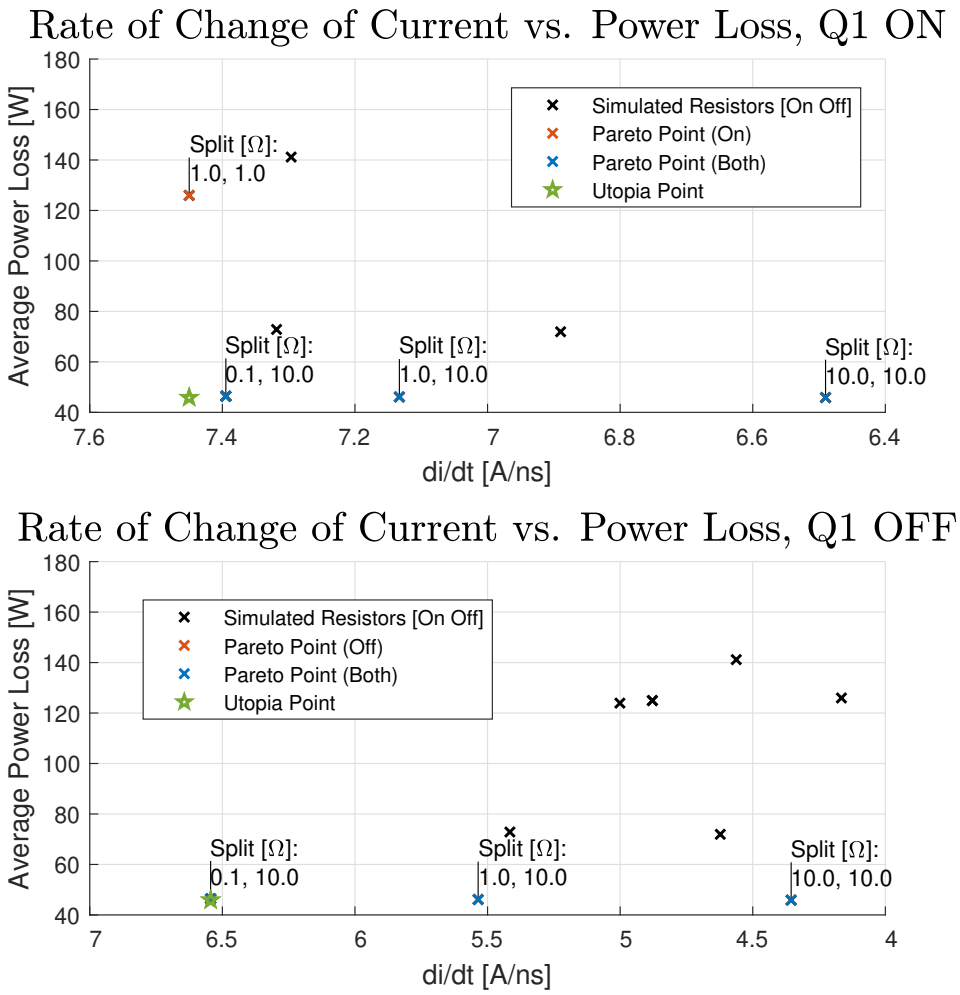


Figure 8.17: Average dissipated power and di/dt of drain current for turn-on and turn-off for Design C with different split gate resistors. **Note:** Resistance values are displayed in the format [On, Off].

As the combination of 0.1 & 10 Ω is a pareto optimum point for both turn-on and turn-off, while also being close to the utopia points, it is deemed the most suitable combination of split gate resistors.

The switching performance for Design C with the optimised FB and gate resistors can be seen in Figure 8.18.

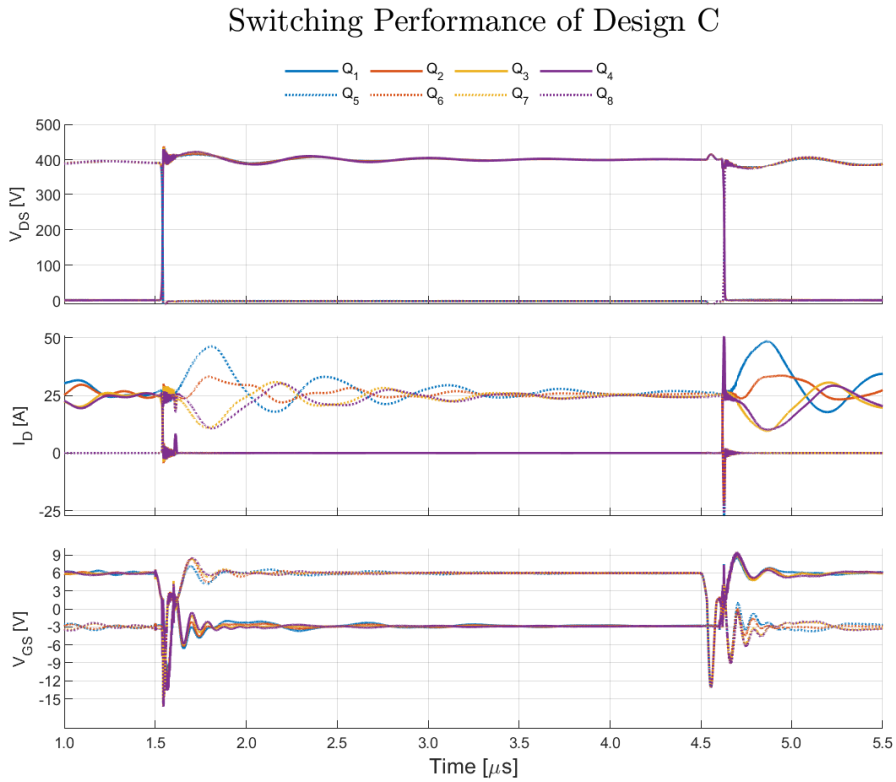


Figure 8.18: Switching performance under load of Design C after power dissipation and di/dt optimisation.

In Figure 8.18 the drain-source voltages can be seen to have a better damping of the ringings. Again, the overshoot is well within the limits of the devices.

As with Design A there is a poor drain current distribution after switching. However, it can be observed that the drain currents do not reach the same amplitudes as with Design A after switching.

The gate-source voltages can be seen to be ringing again as with Design A. This can be clearly seen in Figure 8.19.

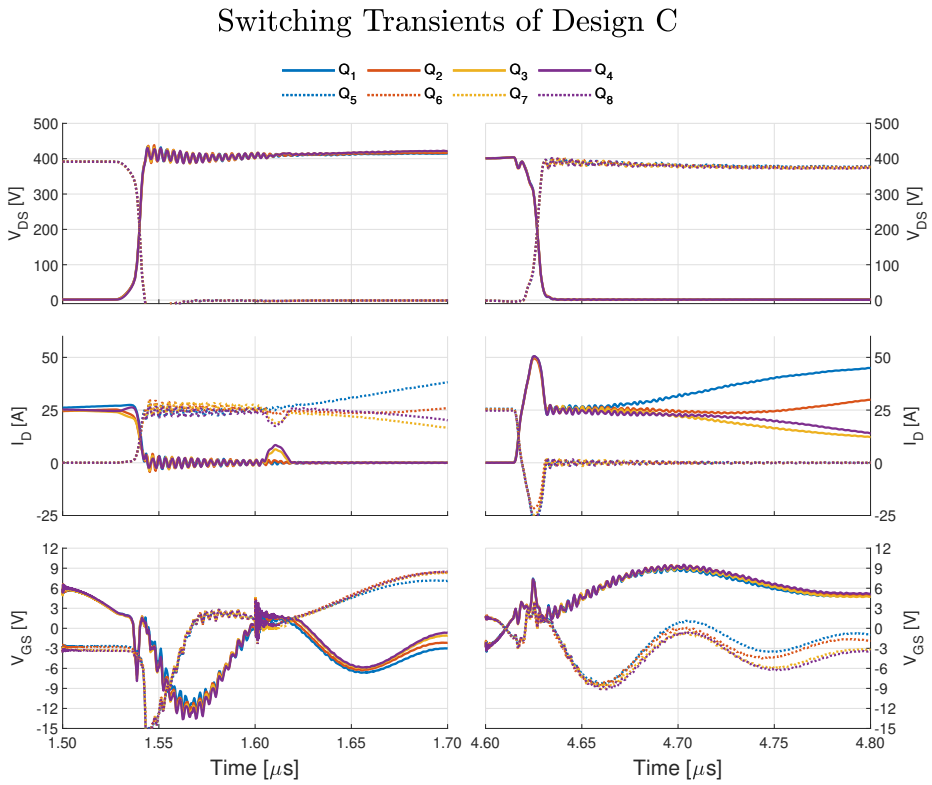


Figure 8.19: Switching transients under load of Design C after power dissipation and di/dt optimisation.

In the low side gate-source voltage a self turn-on can be seen at 1.6 µs as with Design A, which can be noticed briefly on the drain current. As mentioned with Design A, the off-voltage in the experimental setup will be −6 V, which is deemed to ensure stable operation. At the second switching as the low side devices turns off it can be seen that the gate-source voltage goes slightly above the threshold voltage, but is does not seem to impact the drain current or drain-source voltage.

The switching performance parameters, such as overshoot, di/dt, dv/dt, switching energy, and average power dissipation for Design C are listed in Table 8.3.

Design C	**Mean**	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**	**Q8**
V_{DS} OS [%]	5.06	8.38	9.62	8.65	7.66	1.10	1.36	1.79	1.88
I_D OS [%]	70.66	102.07	98.26	101.02	102.51	85.00	32.58	23.17	20.69
di/dt (on) [A/ns]	6.26	7.39	7.67	7.79	7.82	5.12	4.67	4.66	4.97
di/dt (off) [A/ns]	6.16	6.54	3.54	2.03	6.46	7.67	7.45	7.76	7.87
E_{sw} (on) [µJ]	73.65	139.99	137.74	137.96	138.23	8.82	8.80	8.80	8.82
E_{sw} (off) [µJ]	25.17	19.59	15.53	14.78	17.24	37.03	27.57	34.00	35.64
P_{avg} [W]	37.92	46.39	43.93	44.18	45.60	34.31	30.38	29.39	29.18
dv/dt (on) [V/ns]	50.63	55.99	54.17	56.05	57.70	45.91	45.23	45.04	44.93
dv/dt (off) [V/ns]	46.54	39.73	39.49	38.86	38.77	53.42	52.37	54.01	55.67

Table 8.3: Switching performance parameters of Design C for all switching devices.

8.5 Summary

In this chapter a digital optimisation process has been conducted to choose a suitable FB, as well as a suitable combination of common and split gate resistors for each design. The results can be seen in Table 8.4.

Design	**FB Nr.**	**Rcom,on [mΩ]**	**Rcom,off [mΩ]**	**Rsplit,on [mΩ]**	**Rsplit,off [Ω]**
A	24	100	1	100	10
B	9	100	1	100	10
C	24	100	1	100	10

Table 8.4: Chosen FB and gate resistors for each design. The FBs are listed in Appendix C on page 134.

Even though it was mentioned in Section 5.1.2 on page 35 that the off-resistance should be very small, the results from the optimisation process imply that a higher gate off-resistance yields better switching performance. It is decided to continue with the values found during the optimisation process to evaluate the validity of this approach. Each design was simulated with these parameters. The mean value of all switching devices for relevant parameters for the three designs are compared in Table 8.5.

Design	**A**	**B**	**C**
V_{DS} OS [%]	6.28	16.70	5.06
I_D OS [%]	81.60	144.50	70.66
di/dt (on) [A/ns]	6.40	11.08	6.26
di/dt (off) [A/ns]	6.64	11.34	6.16
E_{sw} (on) [µJ]	70.76	54.41	73.65
E_{sw} (off) [µJ]	23.34	28.26	25.17
P_{avg} [W]	42.55	61.57	37.92
dv/dt (on) [V/ns]	51.71	66.96	50.63
dv/dt (off) [V/ns]	45.50	51.44	46.54

Table 8.5: Mean value of switching performance parameters across all switching devices for the three designs.

It can be seen that the average power dissipated in Design B is higher than its counterparts, even though the switching energy during turn on is lower. This is due to the increased amplitude of the drain-source voltage ringings, which is not included in the calculation of the switching energy.

Chapter 9

Experiment

In this chapter, the different designs explained in Chapter 5 will be experimentally validated by conducting a DPT. This will be done to validate the switching performance of the circuit i.e. that the GaN HEMTs can switch under load.

At first, the operation of the DPT will be presented to show the different steps of the test. This includes a presentation of the equipment used, such as the DSP used to generate the necessary gate pulses, the load inductor, DC capacitors, and measurement equipment. Also, practical issues which occurred during the assembly of the PCB will be discussed.

Next, the results of the DPT will be shown and analysed for the three design. Lastly, the experimental data will be compared to the LTspice model in order to evaluate the accuracy of the simulation model in comparison to the experimental data.

9.1 Double Pulse Test

In order to verify the switching performance of the GaN HEMT switching module it is chosen to perform a DPT. A DPT is used to test the switching of a device under load, with minimal heating. The HB circuits designed earlier can be tested using this setup, simply by connecting an inductor from the SW connection to the high side connection. Then, a DC supply and a DC capacitor bank are connected from the high side to the low side of the HB. By turning on the low side devices, the DC bus voltage is applied across the inductor, causing its current to rise. This is illustrated in Figure 9.1 by the orange path. As the low side devices are turned off, the current in the inductor will force the high side devices to reverse conduct. This is also illustrated in the Figure 9.1 by the blue path. Then, the low side devices are turned back on, and a switching transient while turning on under load is recorded. Next, the low side devices are turned back off, and a switching transient while turning off under load is recorded. Finally, the inductor current will discharge through the high side devices, until depleted.

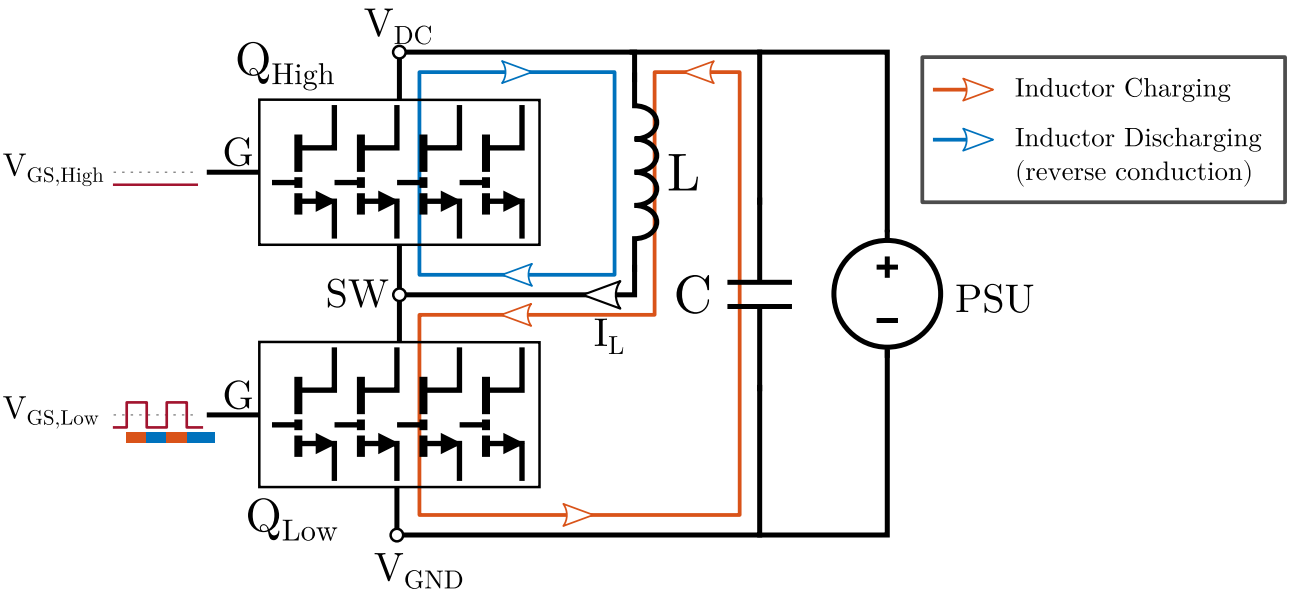


Figure 9.1: Illustration of DPT of the GaN HEMT HB.

By altering the length of the pulses sent to the bottom device gates, different current levels can be achieved, and the devices can be switched under different loads.

In order to generate these pulses, and control their lengths, a TMS320F28335 DSP from Texas Instruments is used [84].

9.1.1 DSP

As explained in Section 5.1.4, optical isolation is used between the DSP and the PCB, requiring optical receivers on the PCB, and optical transmitters on the DSP. By connecting the DSP to optical transmitters with its GPIO pins, the optical signal can be controlled according to C-code running on the DSP to achieve a specific pulse length. The entire code used in this project is shown in Appendix F.3 on page 143. In order to generate a pulse signal, the GPIO pin connected to an optical transmitter can be turned on, a small delay is set, and the GPIO pin is turned back off. By adjusting the length of the delay, the width of the pulse can be adjusted. While the development tools included with the DSP from TI include a delay function, it was found that this could not generate signals with a length lower than around 35 µs. Therefore, an alternate method of delay generation was devised. This was done by taking advantage of the time required to perform a simple task in software, such as running a while loop. This task will take a specific number of clock cycles to perform, which will correspond to a given time.

As the clock frequency of the DSP is 150 MHz, the time for each clock cycle will be 6.67 ns, given by:

$$t_{CLK} = \frac{1}{f_{CLK}} \tag{9.1}$$

By then running the while loop several times, additional clock cycles are required, and the pulse can be made longer. This is shown in F.2 on page 142 and F.3 on page 143, where it is used both used to define the time of the pulse, and the time between pulses. While this relation between clock cycles and time corresponds nicely when measuring directly on the DSP, it was seen that this time does not correspond perfectly, when measuring on the gate voltage of the devices. This is likely due to the various delays in the GD circuit adding up, such that the total length of the pulse is higher than expected. This was taken into account when generating the pulses for the different tests.

In order to improve the controllability of the experiment, a button is used to start the experiment. When the button is pressed, the DPT is performed a single time. The implementation of this can be seen in F.2 on page 142 and F.3 on page 143, where it can be seen that the pulse generation code only happens when the button is pulsed. After the pulse generation is finished, a long delay is introduced, such that only one pulse can be performed at a time. This is to avoid button bounce.

An illustration of the DSP in relation to the laboratory setup for the DPT can be seen in Figure 9.2.

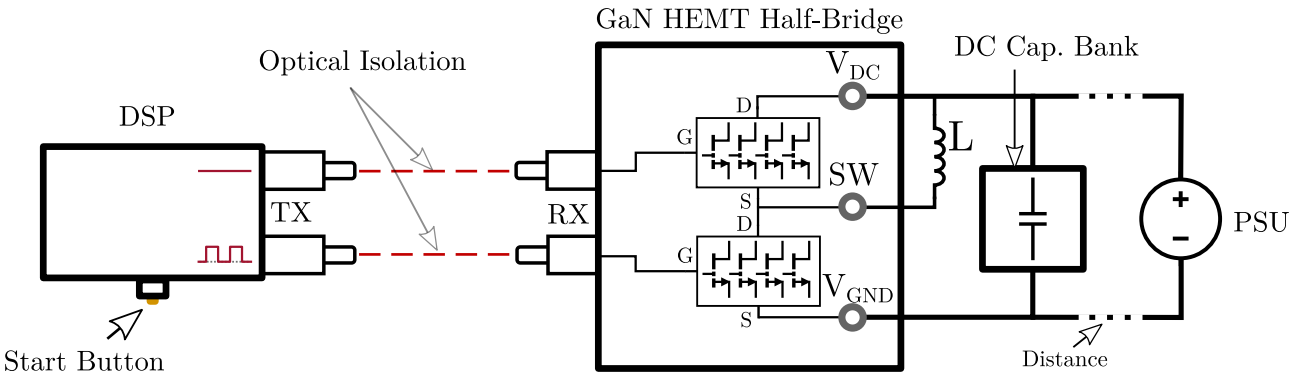


Figure 9.2: Illustration showing the laboratory setup for the DPT.

The physical laboratory setup can be seen Figure 9.3.

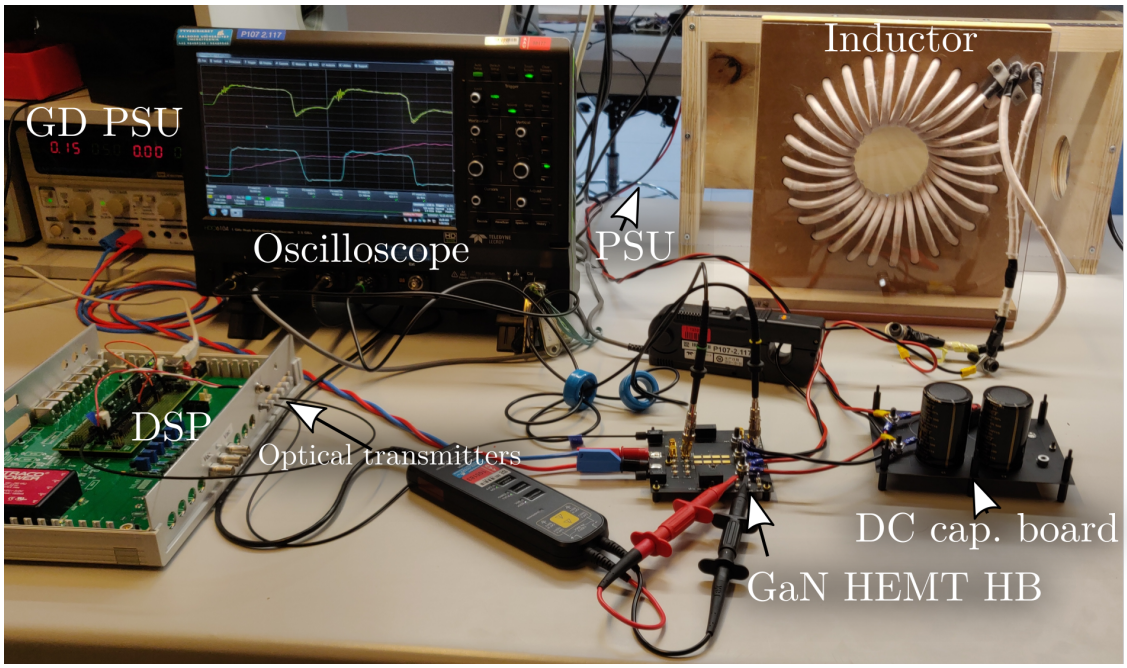


Figure 9.3: Picture of the laboratory setup used in the DPT.

9.1.2 Load Inductor

In order to perform a DPT, a load inductor is needed. By applying a voltage across the inductor, a current can be built up, such that it can be used to perform a DPT, by switching under load. The load inductor is connected between the V_{DC} and SW terminals. When the low side devices are turned on, a current will start to rise in the inductor, until the low side devices are turned back off. At this point, the current in the inductor will force the high side devices to reverse conduct, causing the current to circulate in the loop between the high side devices and the load inductor. Then, the low side devices are turned back on, the high side devices will stop reverse conducting, and the current through the inductor will go through the low side devices again.

In order to optimise the performance of the DPT, an air-core inductor is chosen. The air-core inductor has the advantage of not having a saturable core, thereby keeping the inductance constant at different

currents. Moreover, the air cored inductor should have a minimal amount of parasitic capacitance, thereby increasing its resonance frequency, and inductive frequency range.

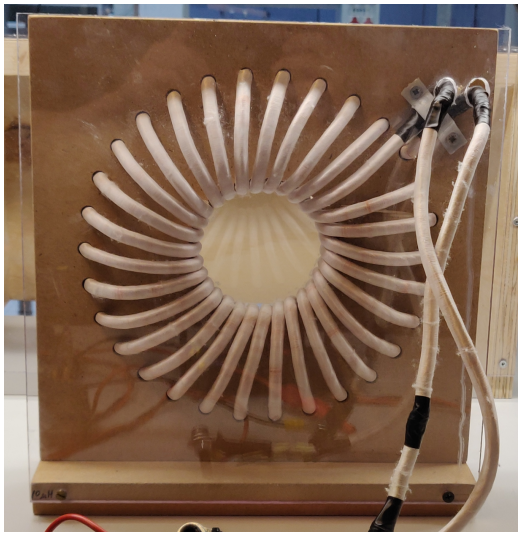


Figure 9.4: Air core inductor used in the DPT.

The air core inductor used for the experiment, seen in Figure 9.4 has an inductance of 9.8 µH, and a resistance of 4.66 mΩ, as measured with an RLC meter. The RLC meter was not able to measure the parasitic capacitance. If a more accurate estimation of the parallel capacitance was needed, an impedance analyser could be used.

9.1.3 DC Capacitor Bank

In Figure 9.2, a capacitor bank is connected in parallel with the PSU. As the PSU will be placed a distance away from the physical test setup, a capacitor bank is required to decouple the PSU from the HB. This capacitor bank will supply the current for the short pulses required to perform the tests. To charge this capacitor bank, the PSU voltage is slowly turned up, until the wanted voltage is achieved. This way, the PSU will endure a minimal loading, and will only have to deliver low amounts of current. A PCB was designed and built, which has room for four 470 µF ALC10(1)471EH500 electrolytic capacitors from KEMET [85]. This PCB is then connected by wires to the PCB and the PSU. While a short distance can be achieved between the capacitor bank PCB and HB PCB, a longer wire is required to connect the capacitor bank to the PSU.

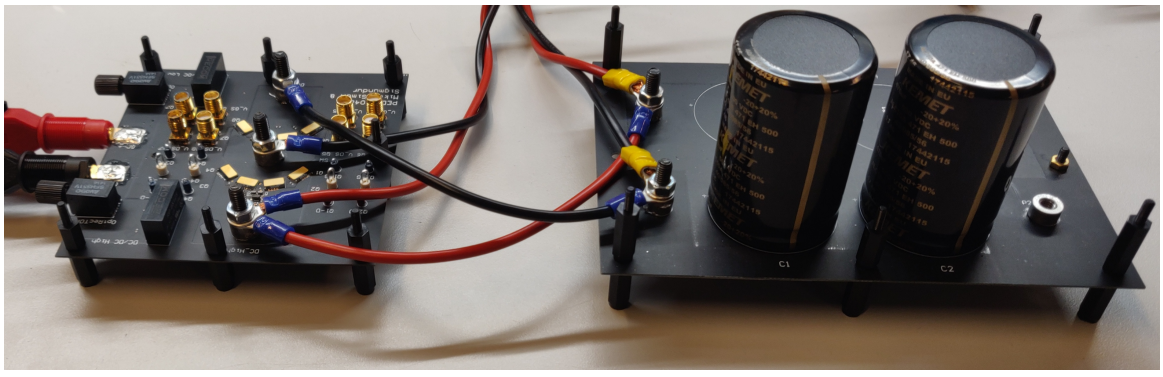


Figure 9.5: DC capacitor bank PCB with two capacitors, connected to a GaN HEMT HB board.

The DC capacitor PCB, with two capacitors, connected to a GaN HEMT HB, can be seen in Figure 9.5.

9.1.4 Measurements

SMA connectors

In order to optimise the voltage measurements on the circuit, coaxial SMA connectors were used. Using these with SMA to BNC adapters, passive voltage probes could be connected to the measurement points without creating a large ground return loop, resulting in a minimal loop inductance. This should increase the frequency range of the measurement, resulting in more accurate data.

Probes

PP026 passive voltage probes from Teledyn LeCroy, with a bandwidth of 500 MHz, were used [86]. The bandwidth of the probe can be related to the rise time it can accurately measure by [87]:

$$t_{rise,min} \approx \frac{0.35}{BW} \tag{9.2}$$

Where $t_{rise,min}$ is the fastest rise time a probe can accurately measure, given its bandwidth (BW). Calculating this minimum rise time for the probes used, yields a time of approximately 0.7 ns. Comparing this to the expected transient times of the devices [23], it can be concluded that these probes are sufficient. These probes were then calibrated according the the user manual [86], such that an accurate measurement could be achieved.

To measure the high side voltages, P5200A, 50 MHz differential probes from Tektronix were used [88].

To measure the current through the inductor, a CP150, 150 A, 10 MHz, current probe from Teledyne LeCroy is used [89].

Oscilloscope

The quick transient times of the GaN HEMT devices also require an oscilloscope with a sufficiently high BW and sample-rate. For this, an HD6104 oscilloscope from Teledyne LeCroy is used [90]. This oscilloscope has a BW of 1 GHz, and a sample rate of 2.5 GS/s. This is sufficient for the measurements to be made.

9.1.5 Physical Assembly of PCBs

The PCBs for the three different designs are ordered from an international PCB manufacturer. Moreover, a PCB with room for four electrolytic capacitors is designed and ordered. All the PCBs are ordered with a thickness of 0.8 mm to improve flux cancellation, reducing loop inductances. With the PCBs, solder paste stencils are ordered, such that the SMD components can be soldered efficiently and accurately.

SMD soldering

Using the solder paste stencil, solder paste is applied to the pads. Then, using a manual pick and place machine, the SMD components are placed in their respective positions. The PCBs are then soldered in a vapor phase reflow oven. The reflow soldering process follows a specific heating profile. This SMD soldering process is necessary for the GaN HEMTs, as their electrical pads are located under the package itself, which would make it infeasible to solder by hand. After all of the SMD components have been soldered, the through-hole components are soldered by hand.

Issues with PCB assembly

It was observed, that some of the SMD components ended up being lifted from one of the pads, only being connected to one of the pads after being soldered. This issue is commonly known as tombstoning. This requires manual retouching of the PCB, in order to properly place the components. The cause of this effect could be a difference in thermal mass of the traces connected to each pad. This causes the pads to heat up at different rates, such that the solder liquefies on one pad earlier than the other. Combined with the low mass of the 0402 components, the surface tension of the liquid solder then causes the component to be lifted. However, given the use of a vapor phase reflow oven with a specifically tuned heating profile, this issue should be minimised. One other cause could be the use of vias under the pads. In order to compress the design, it was chosen to place vias under some of the SMD pads. As the solder was reflown, it could have been suctioned into the hole of the via. This could then have caused a small force to be applied to the SMD component, resulting in it being lifted off of its opposite pad.

9.2 Results

Firstly, all of the designs were tested to ensure that the GD was functioning as intended. This was done without the power side connected, only supplying a signal to the low side GD and measuring the gate-source voltage V_{GS}. With the gate properly functioning, the power terminals were connected and a minimum pulse of about 290 ns was given to the low side devices to ensure a minimal current during the switching. The DC voltage was then increased to 20 V and a DPT was executed and the performance was evaluated. The DC voltage was then increased small steps until the desired voltage of 400 V was tested. Then, the current level was ramped up slowly, and data was captured at different operation points.

The rise times and fall times of the circuits under different loads will be presented. The rise time is defined as the time it takes the drain-source voltage of a device to rise from 40 V to 360 V, i.e. it is calculated from the point at which the drain-source voltage increases to 10 % of its steady state value to 90 %. The fall time is defines as the time it takes the drain-source voltage to fall from 360 V to 40 V, i.e. 90 % to 10 %.

The results presented in this section are presented in the order as they were found in the laboratory. This was done due to the events that occurred during the initial testing of the designs, which changed the purpose of the experimental work and initiated a different learning process.

9.2.1 Design A

The PCB layout presented for Design A in Section 6.1 was produced and the PCB used for the experimental work can be seen in Figure 9.6.

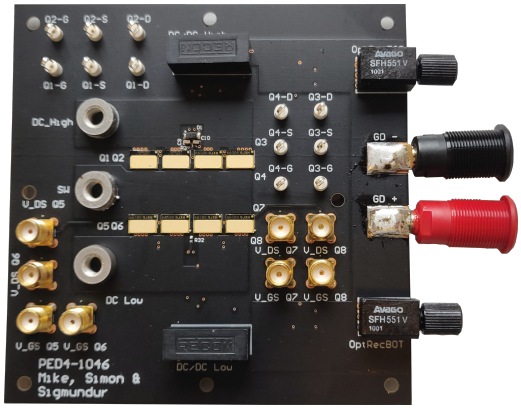


Figure 9.6: PCB of Design A.

When the functionality of Design A had been verified at lower voltages, the DC bus was increased to 400 V, and DPTs were performed. Starting at the lowest possible current with the specific setup of DSP and inductor, a current of approximately 11.3 A was built up in the inductor, and the circuit switched as intended. This test was repeated, increasing the pulse lengths, and thereby the current by approximately 10 A every time. During the DPT, the gate-source voltage of Q5 was measured and recorded with a passive probe, along with the drain-source voltage of Q5. Moreover, the inductor current was measured with a current probe. Lastly, the drain-source voltage of Q1 was measured with a differential probe.

The complete DPT sequence at 50 A is shown in Figure 9.7.

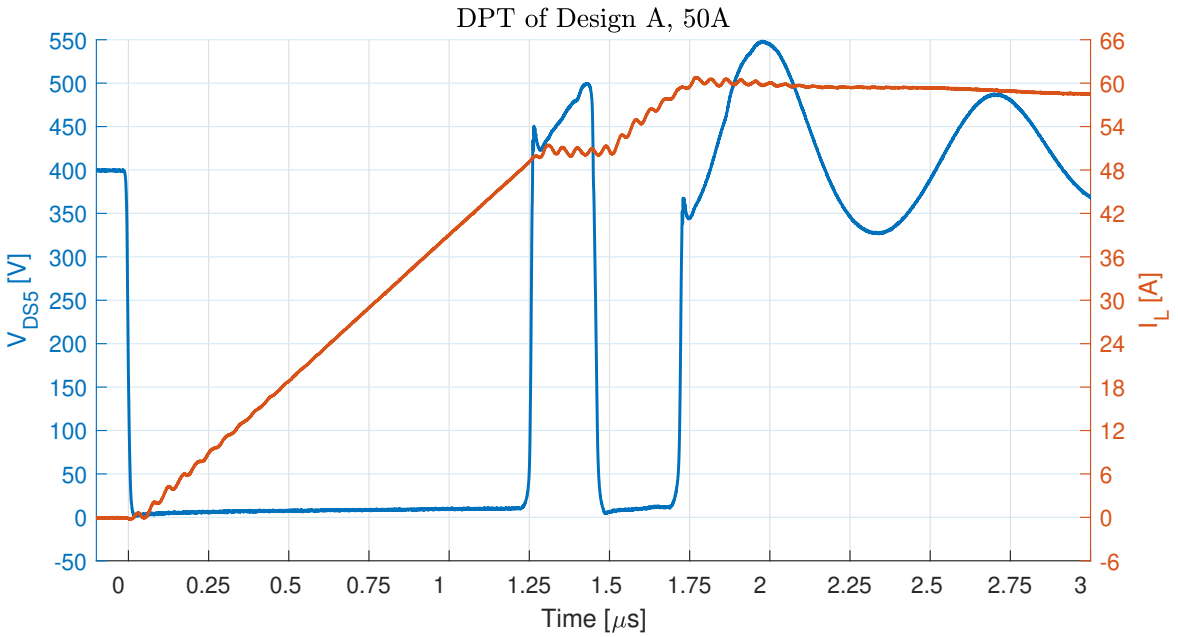


Figure 9.7: DPT of Design A at 50 A.

Looking at Figure 9.7, it can be seen that the low-side voltage of Q5 falls to approximately zero, and the current starts to rise. This continues until the low side devices are turned back off, and the current stagnates. Then, the low side devices are turned back on, and the inductor current starts to rise again, until the low side devices are turned back on. Looking at the inductor current, it can be seen to follow a mostly linear trajectory, as a result of the use of an air-core. Some small ripples can be seen on the inductor current, however these are not considered to be an issue. However, when looking at the drain-source voltage across Q5, a large, low frequency oscillation can be seen. This causes the voltage to rise up to almost 550 V. The oscillation has a resonance frequency of approximately 1.3 MHz. The origin of this resonance is thought to come as a result of the interaction between the decoupling capacitors and electrolytic DC bank capacitors. As the GaN HEMTs under test are turning off, a high frequency current is required to charge the output and gate-drain capacitances. This decreases the voltage across the decoupling capacitors, which in turn causes a current to flow from the DC capacitors to charge the decoupling capacitors. As this is a low resistance path with a large inductance, due to the cables used, it has a high quality factor, which means that the resonance will take longer to die out, as seen in Figure 9.7. The cause of this was understood too late in the experimental work to be accounted for, but this effect could have been reduced by either reducing the length of the cables, increasing the resistance to dissipate the energy of the resonance or adding a FB for that specific resonance.

To get a better impression of the switching performance of Design A, the switching transients under load are examined. At first the turn-off transients are shown in Figure 9.8.

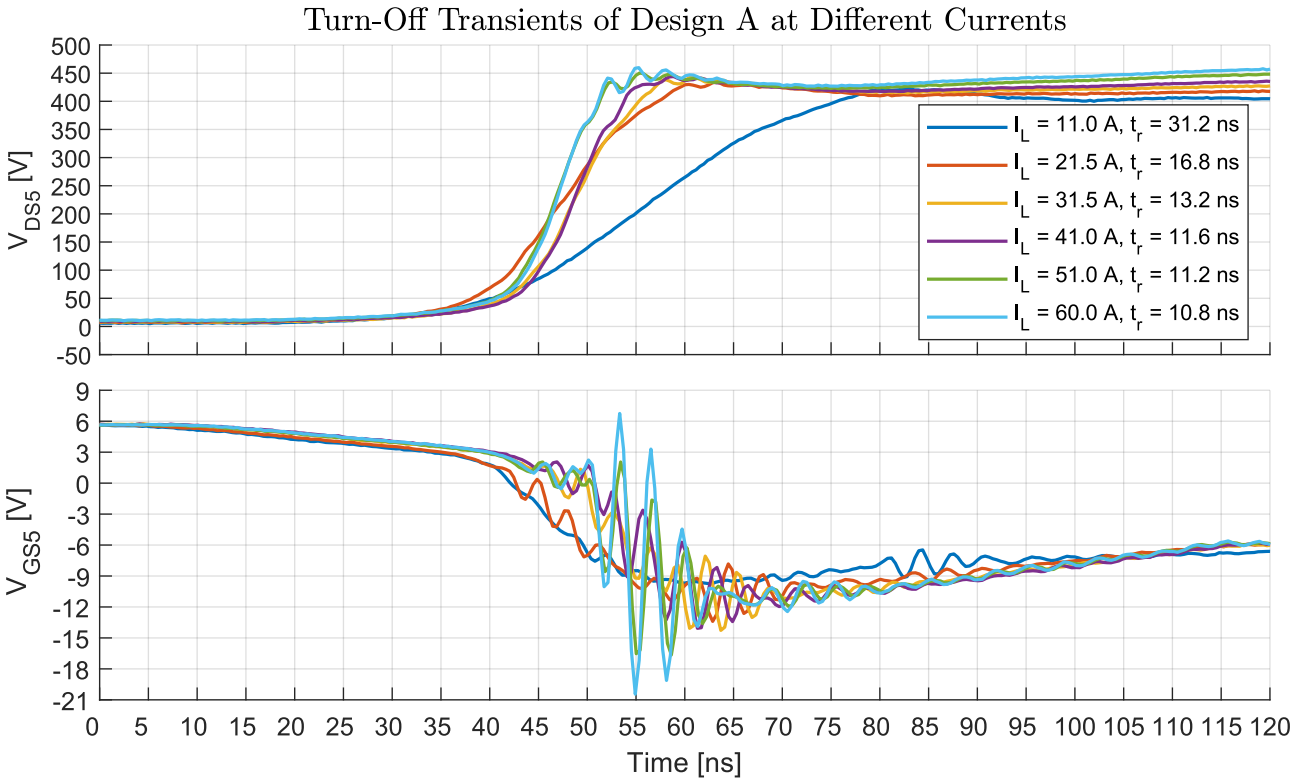


Figure 9.8: Turn-off switching transients of Design A at different currents.

In Figure 9.8, the turn-off transients of Design A at different currents are seen. In the top plot, the drain-source voltage of Q5 is shown, while the gate-source voltage of Q5 is shown on the bottom plot. It can be seen, that at higher currents, the rise time tends to decrease. The most dramatic difference is seen when the load current goes from 11.3 A to 21.5 A, where the rise time is almost

halved. When looking at the drain-source voltages, they generally seem to be stable at the switching instance. However, when looking at the gate-source voltage of Q5, the increase in current can be seen to cause increasingly larger oscillations on the voltage. As discussed in Section 5.1.2 on page 35 the gates of the devices are susceptible to a current injected from the gate-drain capacitance. As the gate-drain capacitance sees the high dv/dt on the SW and will start to charge. The current from the gate-drain capacitance triggers a resonance in the low impedance path, as illustrated in Figure 5.6, which is thought to induce the ringings on the gate-source voltage, seen in Figure 9.8.

Another possible cause of these disturbances could be the mutual inductance between the GD and power loops. As the operating point of the DPT is increased, the higher drain current will induce an increasing current into the gate loops. The turn-on switching performance of Q5 can be seen in Figure 9.9

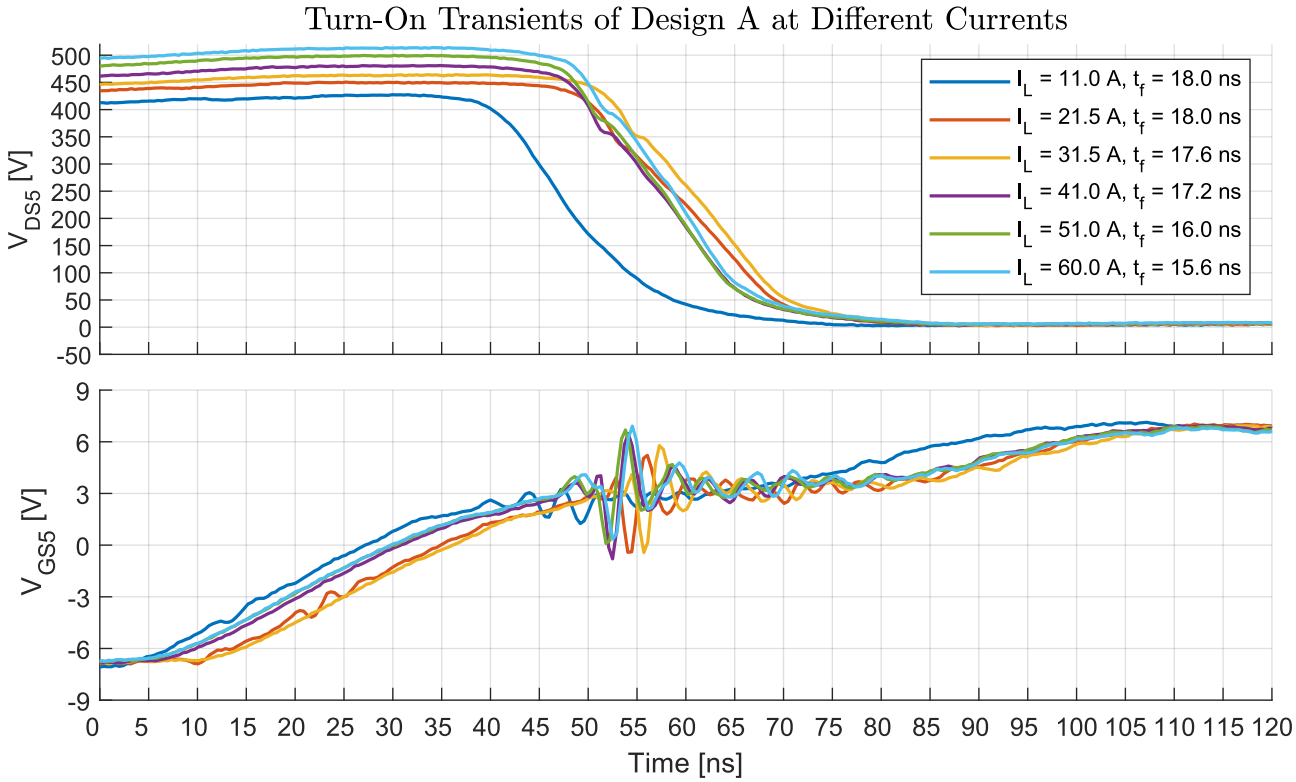


Figure 9.9: Turn-on transients of Design A.

In Figure 9.9 the turn-on transients of Design A at different currents are seen. It can be noticed that the drain-source voltage before switching is different at the different currents. This comes as a result of the oscillation shown in Figure 9.7. This voltage is seen to increase in amplitude as the current increases. When looking at the transients, they can be observed to have the same general slope, with the fall time only being reduced from 18 ns at a current of 11 A to 15.6 ns at 60 A. It can be noticed that the drain-source voltage at 11 A starts decreasing earlier compared to at the other current levels.

Looking at the gate-source voltage, it can be observed to have some oscillation at the switching point at the higher currents. These oscillations are thought to be caused by the drain current overshoot which happens as the device starts to conduct and the drain-source voltage decreases. This dv/dt across the output and gate-drain capacitance forces a discharge, which coincides with the flow of the drain current. This could cause undesirable voltage drops across the parasitic inductances on the power side, which could affect the gate-source voltage. This is also illustrated in Figure 2.4 on page 6. It can also

be seen for the higher currents, that the gate-source voltage oscillates around the threshold voltage, which could affect the rise of the drain current and thereby the di/dt of the parasitic inductances.

The different rise and fall times during turn-on can be seen in Figure 9.10 for the different current levels.

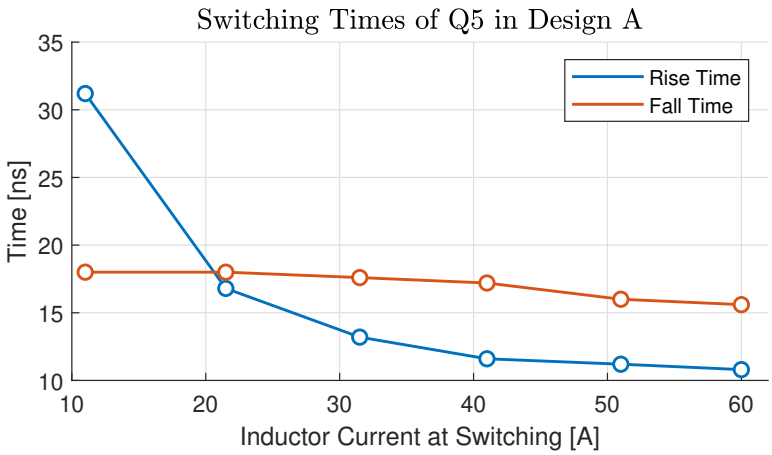


Figure 9.10: Switching times of V_{DS5} in Design A at different load currents.

In Figure 9.10 the rise times (turn off) and fall times (turn on) of the drain-source voltage of Q5 in Design A at different currents has been plotted. A tendency can be observed in that the rise time decreases at higher currents. This effect does have diminishing returns, as the greatest change in rise time is seen when going from 11.3 A to 21.5 A.

The tendency of the reducing rise time can be explained by the plateau voltage, which is dependent on the drain current. The gate current when turning off is dependent on the voltage drop over the gate impedance, as shown in (9.3).

$$I_G = \frac{V_{EE} - V_{GS}}{R_G} \tag{9.3}$$

Where I_G is the gate current, V_{EE} is the off gate supply voltage, V_{GS} is the gate-source voltage, and R_G is the total gate resistance.

When a higher drain current is flowing through the device, a higher plateau voltage on the gate-source voltage is achieved. This results in a higher voltage drop over the gate loop impedance, resulting in a higher gate current. This gate current defines the speed at which the gate-drain capacitance charges, thereby determining the switching time of the device.

While the transients measured when switching at 60.3 A look similar to what was observed at lower currents, a failure occurred. Looking at Figure 9.11, it can be observed that Q7 encountered a failure, causing it to explode due to a short in the circuit.

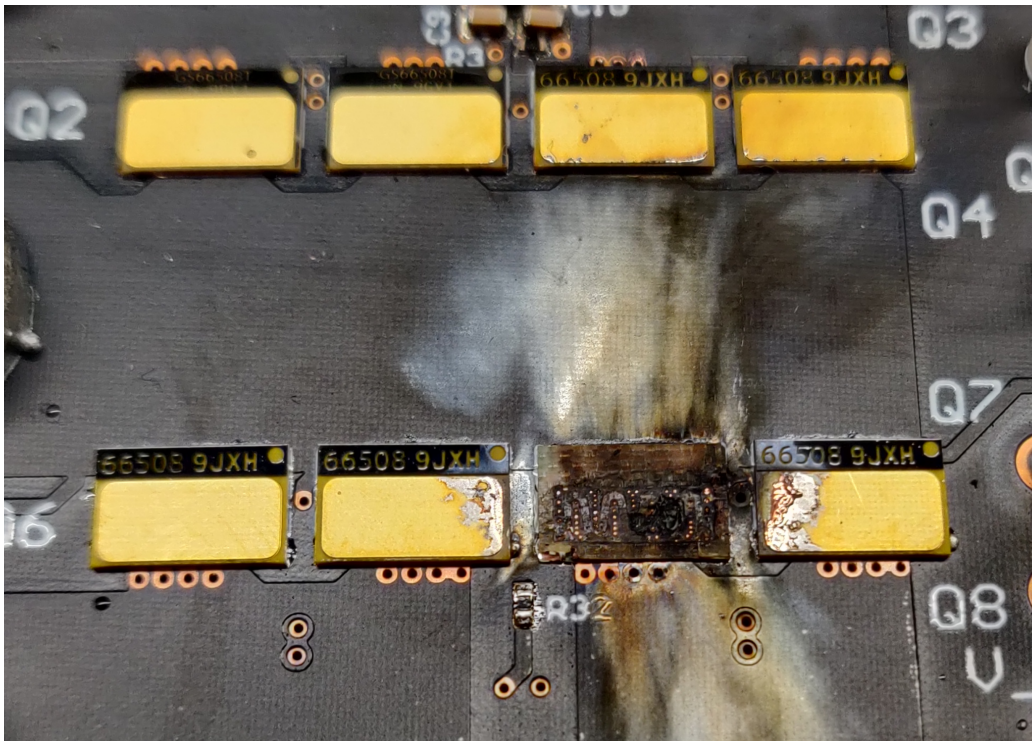


Figure 9.11: Image of Design A after failure during the DPT.

Switching at 60.3 A, an equal sharing of current would only result in approximately 15 A per device, much less than the rated currents of the devices [23], allowing for 30 A continuous, and 60 A pulsed current. Therefore, it can be postulated, that an uneven current sharing was experienced, causing a single device to carry a larger load, causing its destruction.

9.2.2 Interpretation of Results from Design A

As the destruction of Q7 came as a surprise, the waveforms should have been examined further before the current was increased. This way, the unintended behaviour of the circuit could have been noticed earlier, and the test could have been stopped until a better understanding could have been achieved. Due to this unexpected failure, insufficient measurements were made, as only the drain-source voltage and gate-source voltage of Q5 was measured on the low side devices. Therefore, no measurements of Q7 were made.

While a failure was experienced when switching at 60 A, these tests showed a successful switching, turn-on and turn-off, at up to 50.5 A, and successful turn-off of approximately 60 A, as seen in Figure 9.7.

9.2.3 Design C

Next, the circuit for Design C was tested, which can be seen in Figure 9.12.

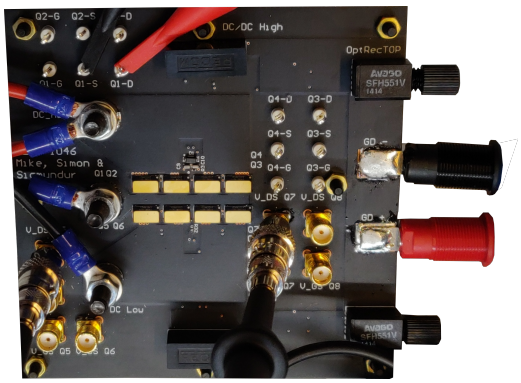


Figure 9.12: PCB of Design C.

As with Design A, the function of the GD circuit of Design C was verified without a DC bus voltage. Then, the circuit was tested at low voltages, until finally stepping up to 400 V. Given the mistakes made when testing Design A, more care was given for the measurements of Design C. For every current level tested, all of the low side drain-source voltages, the low side gate-source voltages and the high side drain-source voltages were measured. Moreover, the load current was also measured in every test. As the oscilloscope used for measuring the test had 4 inputs, probes had to be moved around on different measuring points, and each test had to be repeated with the different probe placements.

As more measurements were made, the behaviours of different devices in the circuit during switching can be compared. This is shown in Figure 9.13, switching at 22 A.

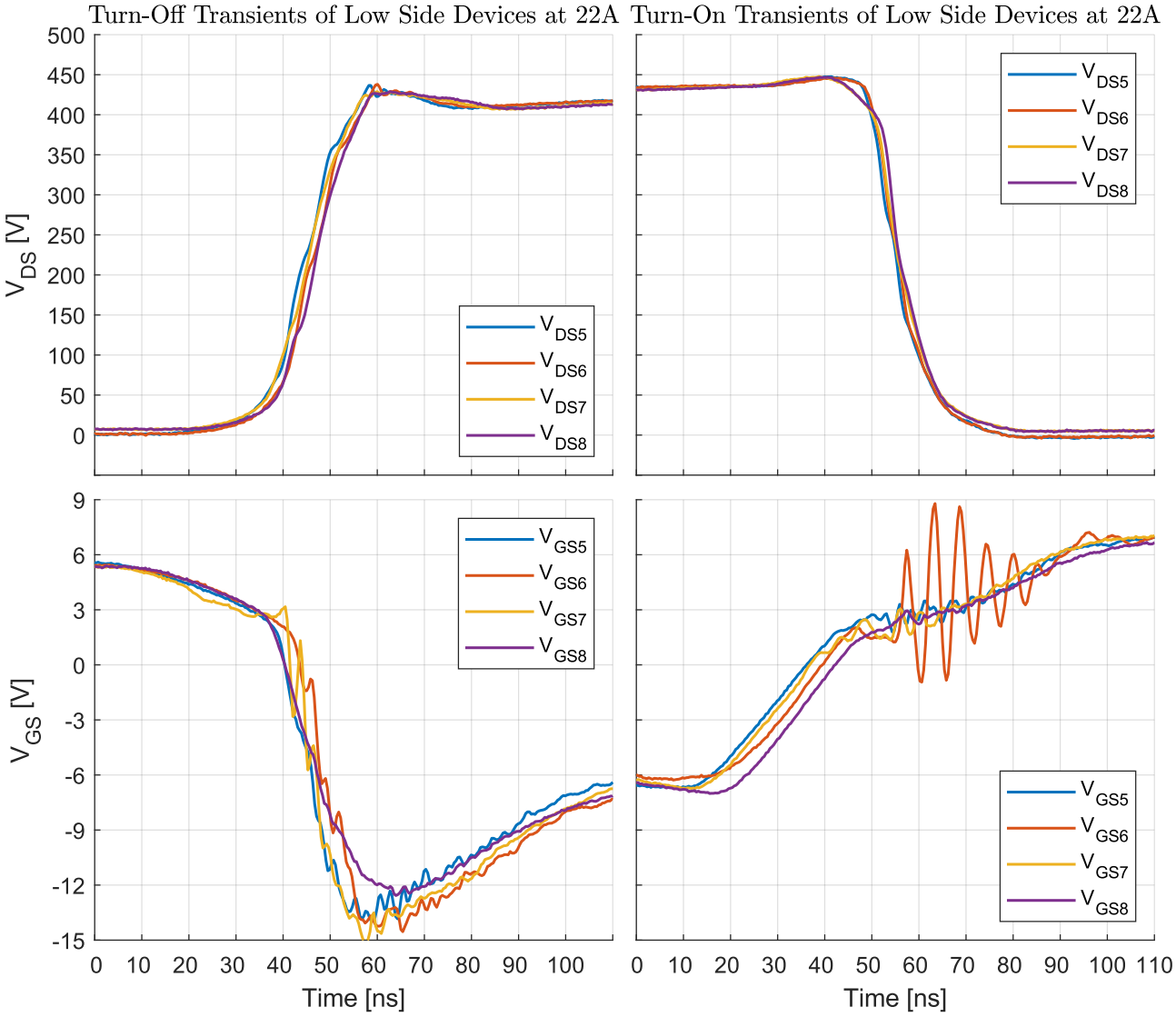


Figure 9.13: Comparison of drain-source and gate-source voltages of devices Q5-Q8.

Looking at the drain-source voltages of the different devices under switching, their behaviour seems to be very similar. However, looking at the gate-source voltages, some difference can be noted. The outer devices, Q5 and Q8 seem to have cleaner wave forms, while the inner devices Q6 and Q7 seem to have some more distortion and oscillation. Especially in the turn-on transient, where the gate-source voltage of Q6 can be seen to oscillate significantly.

This could be caused by the fact that the measuring points were changed between each test and that the gate-source and drain-source voltages for the same device could not be measured at the same time, as the measurement points had been placed too close to each other. This means that the measurements of the gate-source voltages do not correspond directly to the drain-source voltage of same device, as these measurements were made at different times.

Moreover, it should be noted that when measuring, the probe itself will add some parasitic capacitance to the node itself. This will alter the circuit performance slightly.

As the current level was increased to 30 A a failure occurred at this current level as shown in Figure 9.14.

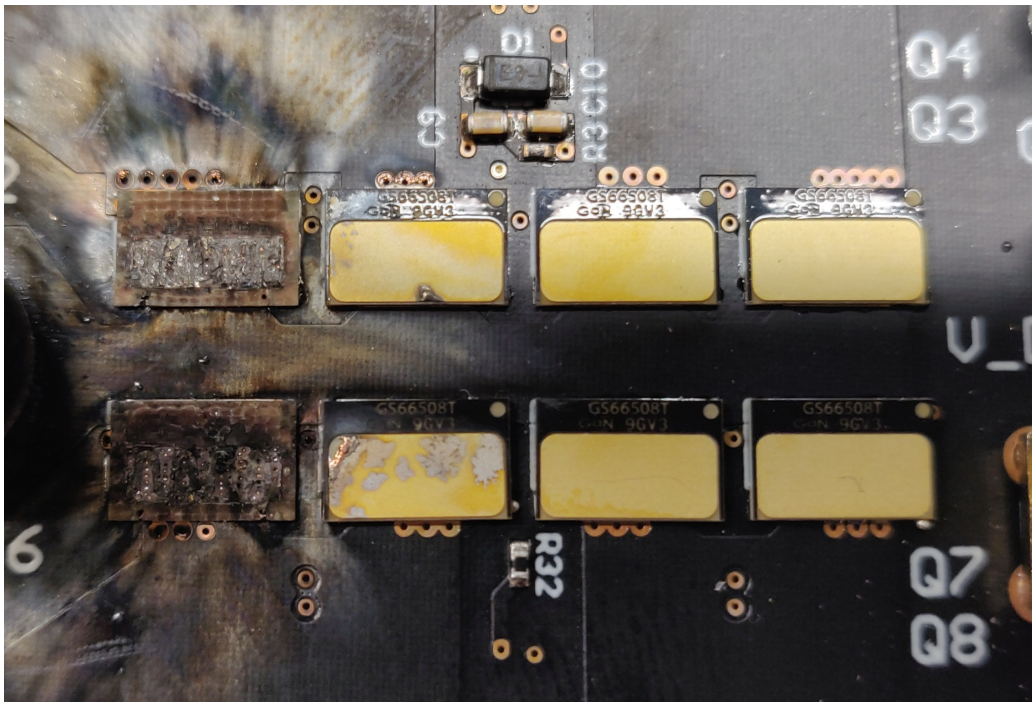


Figure 9.14: Design C after failure.

It can be observed, that a shoot-through occurred, as both Q1 and Q5 were destroyed. This indicates that both devices have been conducting at the same time, shorting the DC capacitor supply. While the circuit was destroyed, measurements were retrieved for the the earlier tests, and some further analysis can be made. In Figure 9.15 the turn-off transients measured on Q5 in Design C are seen.

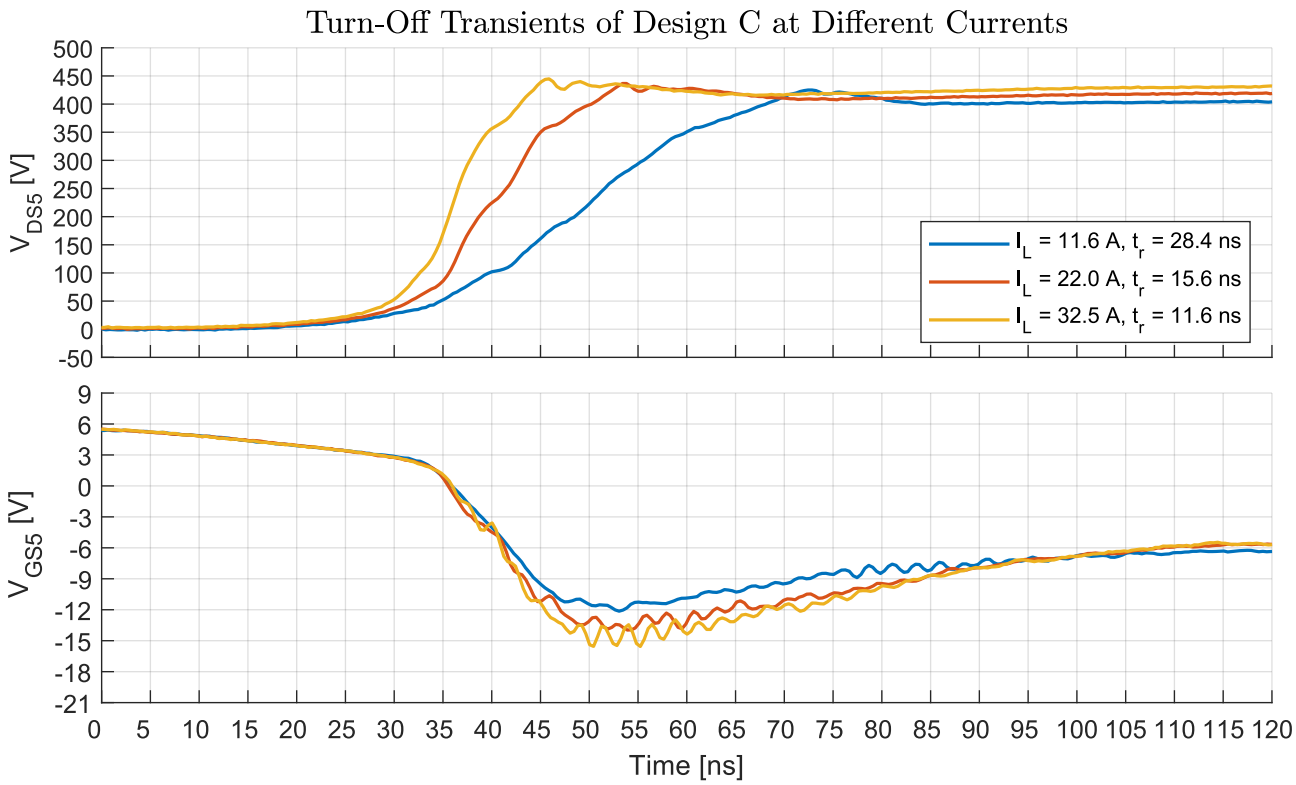


Figure 9.15: Turn-off transients of Design C at different currents.

It can be seen, that the rise time of the drain-source voltage of the low side device is highly dependent on the load current. This was also seen in Design A. Looking at the gate-source voltage, it can be seen that there is a considerable undershoot, as it reaches down to approximately −15 V. While this is within the rated conditions of the device for transients [23], repeating this could potentially cause issues, degrading the device.

In Figure 9.16 the turn-on transients of Design C are seen.

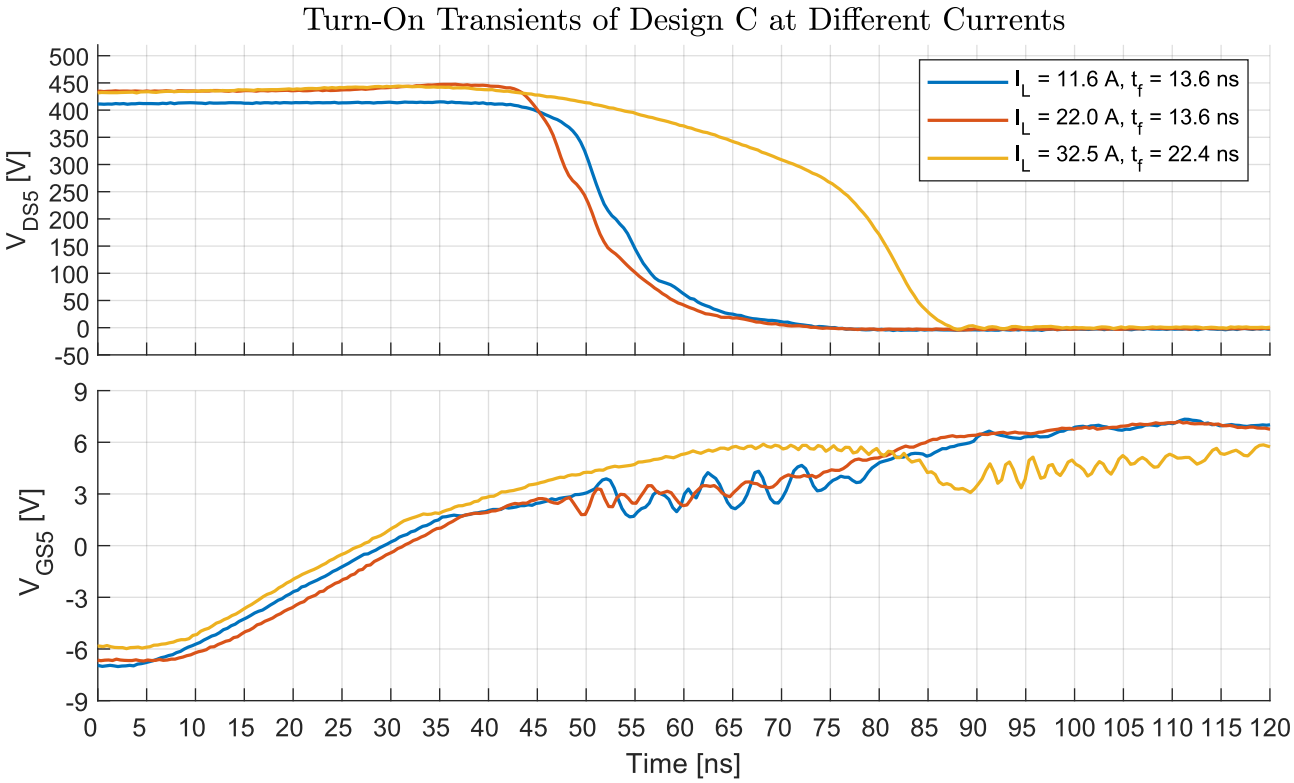


Figure 9.16: Turn-on transients of Design C at different currents.

While switching at 11.6 A and 22 A, the circuit seems to function normally, switching at 32.5 A causes some unwanted behaviours to occur. Looking at the top figure showing the drain-source voltage of Q5, it can be seen that the device voltage seems to fall much more slowly at 32.5 A, than at lower currents. The drain-source voltage seems to fall slowly at the start, with a low dv/dt, until a voltage of approximately 200 V is reached, when the dv/dt is similar to the other wave forms.

This anomaly is also reflected in the waveform showing the gate-source voltage of Q5. It can be seen that the gate-source voltage reaches the 6 V V_{DD} voltage much quicker than at lower currents, seemingly not encountering the miller plateau. Then, as the drain-source voltage approaches 0 V, the gate-source voltage falls.

This whole sequence is unusual, and indicates some sort of anomaly in the circuit. This behaviour was unfortunately not noticed when testing the circuit, and therefore the testing continued. After changing the measurement points on the circuit, in order to get more data, the circuit was again run at a load current of 32.5 A.

In Figure 9.17 the recorded switching times of Q5 for Design C are showcased.

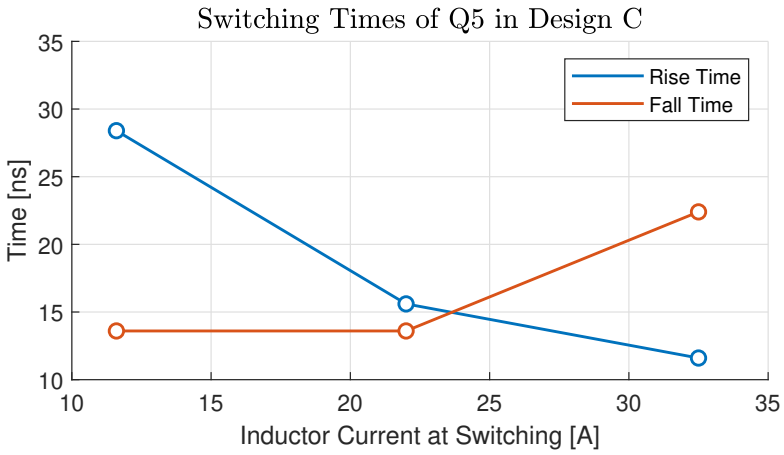


Figure 9.17: Switching times of V_{DS5} in Design C at different load currents.

Comparing this to what was seen for the switching of Design A, in Figure 9.17, the switching times seem to be lower. This showcases the importance of low power loop inductance. The exception is the turn-on at 32.5 A, where Design C is much slower. This further indicates the unusual circuit behaviour.

9.2.4 Design B

Finally, the circuit for Design B was tested and the PCB can be seen in Figure 9.18.

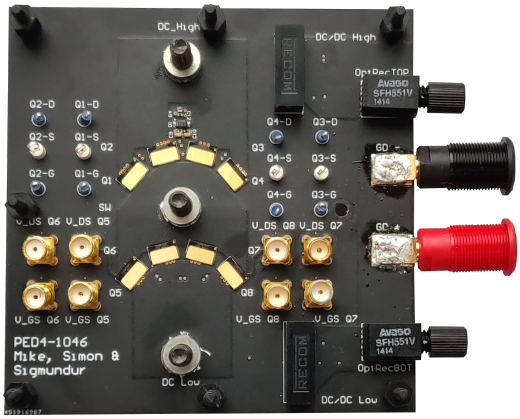


Figure 9.18: PCB of Design B.

In reflection of the results of the tests performed on the other circuits, another approach was taken for testing Design B. As the other circuits had critical failures when testing at 400 V, the circuit of Design B was tested at lower voltages, and minimal currents, in order to attempt to isolate the potential causes of failure with a lower risk of failure. It was also decided to measure the high side gate-source voltage as it was suspected that there was unwanted turn-on.

In the optimisation process shown in Chapter 8, split on and off gate resistances were found. As mentioned in Section 8.5 , the values found for the gate resistors using the optimisation procedure are different to what is generally recommended for gate circuits for GaN HEMTs. Especially the off loop resistance seemed to be too large. Too large off loop impedances could cause devices to experience unwanted turn-on effects [53][91]. To attempt to reduce this effect, the off loop split resistances were changed from 10 Ω to 1 Ω, and the on loop split resistances were changed from 0.1 Ω to 10 Ω for the following tests.

The circuit was initially tested at 50 V, with the shortest pulses which could be generated. This resulted in a load current of 1.65 A when switching.

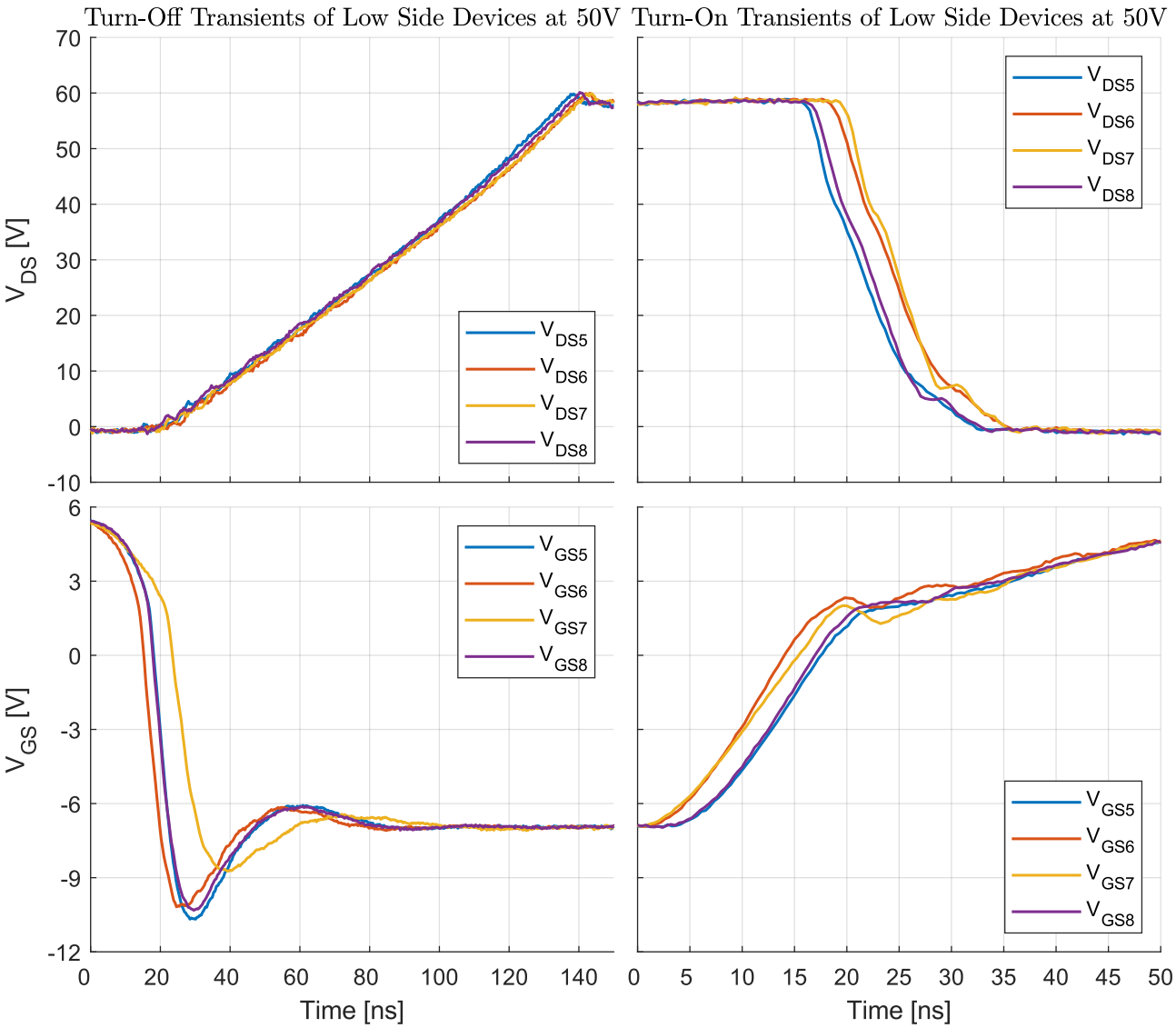


Figure 9.19: Switching transients of Design B at 50V.

In Figure 9.19 the switching performance of the low side devices of Design B, switched at 50 V 1.65 A, is seen. Looking at the drain-source voltages, it can be seen that the turn-off transient is very slow compared to the turn-on transient. This may be due to the non-linear gate-drain capacitance, which is much larger at lower voltages, than at voltages above 100 V.

When comparing the different devices, they seem to have very similar transients in the drain-source voltages. This is to be expected, as no significant load is put on the devices. However, when looking at the gate-source voltages, some difference can be seen, especially in the turn-off transients, where V_{GS7} has a different shape than the other gate-source voltages. This does not seem to have an effect on the performance of the circuit, from the given measurements.

To further investigate the circuit, the voltage was increased to 100 V. The turn-off transient of this compared to the transient at 50 V is seen in Figure 9.20. As the pulses could not be made shorter, and the two experiments were run using the same pulse lengths, the current of the 100 V test was almost twice that of the 50 V test.

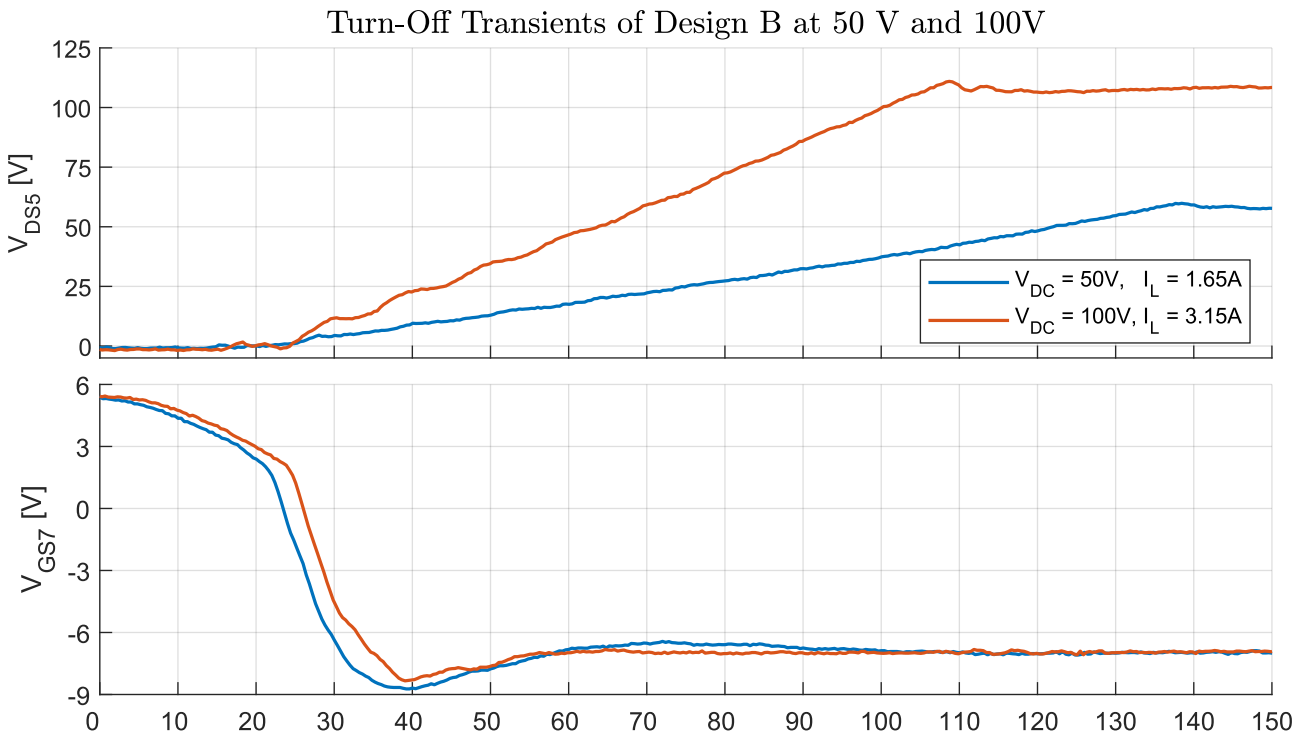


Figure 9.20: Turn-off transients of Design B at 50 V and 100 V

It can be seen, that the 100 V test has a slightly shorter rise time, otherwise no significant difference can be noted.

While running these tests, the high side gate voltages were also measured. In Figure 9.21, the turn-on transients of Design B at 100 V and 50 V.

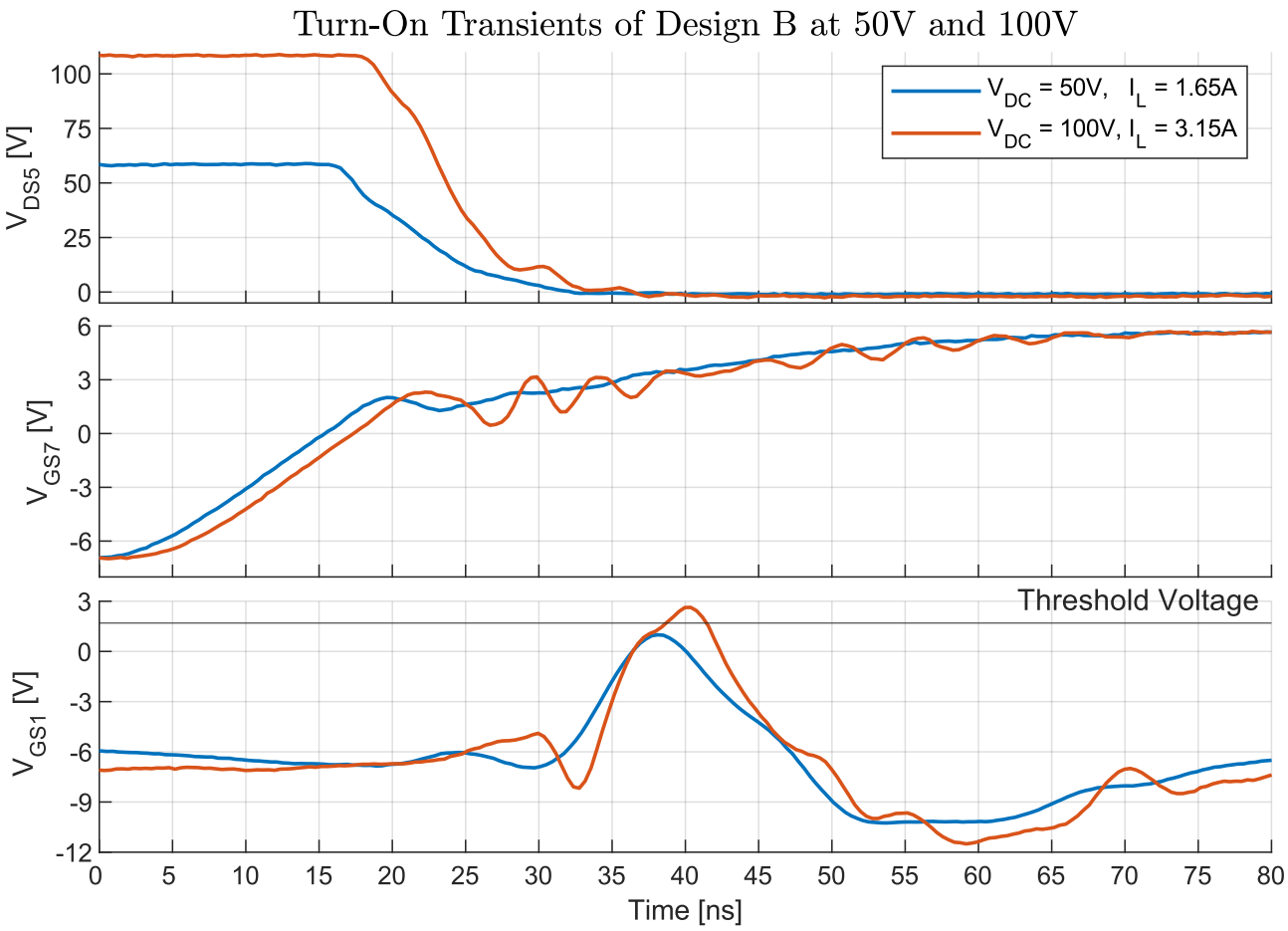


Figure 9.21: Turn-on transients of Design B at 50 V and 100 V.

In the bottom plot of Figure 9.21, the gate-source voltage of the high side device $Q1$ is shown. It can be seen that during the turn-on transient of the low side devices, this voltage rises. This effect seems to get larger at the higher voltages, causing the high side gate-source voltage to exceed the threshold voltage of the device. This could be an explanation of the failures of the previous PCBs, as these were operating at even higher loads. The reason for this voltage spike could be attributed the current from the gate-drain capacitance, inducing a voltage drop over the gate impedance [91]. It was attempted to reduce this effect by reducing the off impedance, but this was not enough to reduce the voltage spikes on the high side. Therefore, it could be assumed that this means that the GD loop inductances are too high. The GD loop inductance for high side of Design B was also the highest of all GD loops as seen in Section 6.3 on page 57. A high GD loop inductance would cause such voltage spikes to occur, when the miller current flows from the gate-drain capacitance into the gate supply. In order to reduce this loop inductance, new circuits would need to be designed, where more focus on reducing the GD loop inductances was exhibited.

9.3 Comparison Between Experimental Data and Simulation

As the digital design process used in this project is based a SPICE simulation, which attempts to accurately replicate the behaviour of the actual circuit, the results found in the laboratory data will be compared to what is seen in the simulation. This will give an insight into the accuracy of the simulation, and evaluate the validity of the digital design process.

To make this comparison, a DPT is performed on the simulated Design A circuit. Firstly, the circuit is run at a low current, 22 A in the load inductor at the switching instance. This can be seen in Figure 9.22.

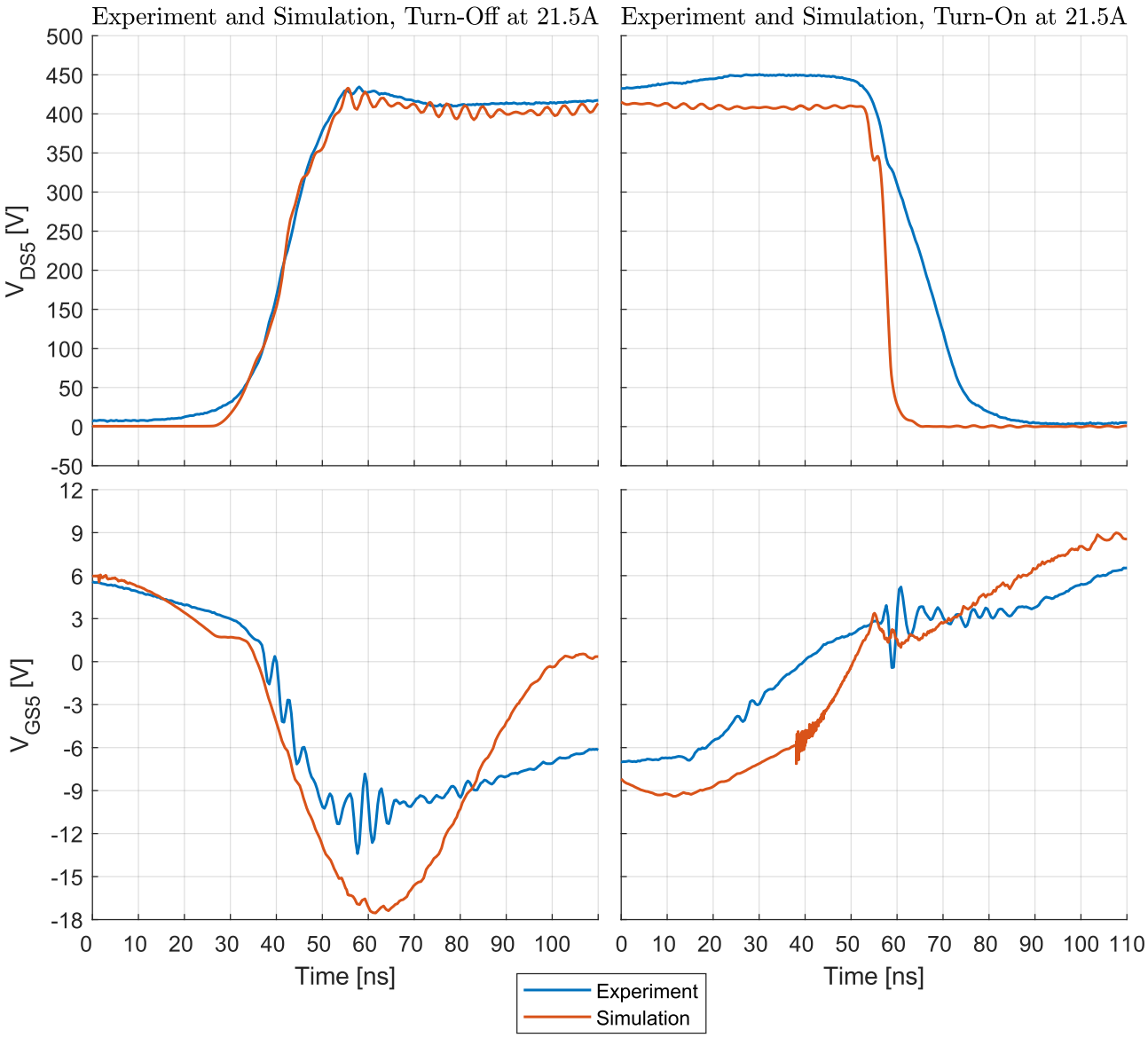


Figure 9.22: Comparison of switching in experiment and simulation, in Design A.

In the top figures, the drain-source voltage of Q5 is shown, with a turn-off transient and a turn-on transient. When looking at the turn-off transient in the top left, it can be seen that there is a good resemblance between the experimental and simulated data. The slew rate and time to switch can be seen to be almost identical. There does seem to be some more damping in the results of the

experiment, as the simulated data has some high frequency ringing on the waveform, which is minimal in experimental data. However, the small ringing that can be seen on the experimental data seems to be in the same order of magnitude as the simulated ringing, indicating some resemblance in the parasitic content. The difference between these two could be attributed to the measurement method, as the simulated data is measured directly on the node, and the experimental data will be filtered by the probe and oscilloscope used, as these have a limited bandwidth. Another difference between these results is that the simulation does not include frequency dependent inductances and resistances. At higher frequencies, the skin-effect starts to have an effect, increasing the trace resistance. This will add additional damping to the circuit. Moreover, the inductance will change at higher frequency, ending up at a lower value [92][93].

However, the turn-on transients seem to be less alike, as the experimental transient is much slower, with a lower slew rate. Moreover, the experimental drain-source voltage starts at a higher voltage, as a result of the lower frequency ringing seen in the experiment. This behaviour is not replicated in the simulation.

Looking at the bottom charts, the gate-source voltages can be seen. In the bottom left figure, the gate-source voltages of Q5 in the turn-off transient are seen. There is some resemblance, with the voltages having similar slew rates, but the experimental data exhibits some high frequency ringing, while the simulation has some lower frequency oscillations. A similar tendency is seen on the turn-on transients.

Next, a similar comparison is made at a higher load current, this time at 51 A. This is seen in Figure 9.23.

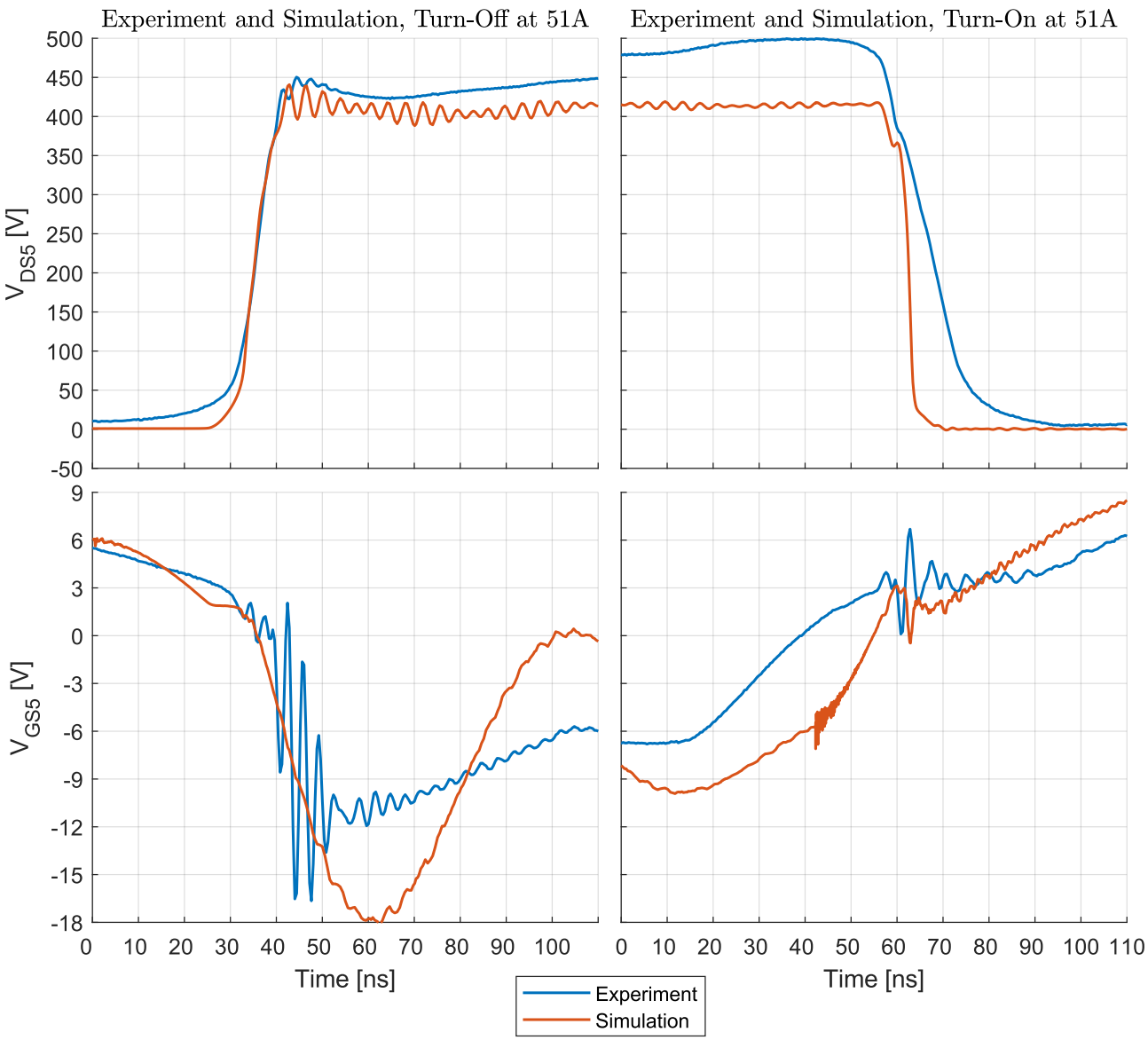


Figure 9.23: Turn-on transients of Design B at 50 V and 100 V.

Again, the turn-off transient of the drain-source voltage seems to have a decent match, exhibiting similar slew rates, with some difference in the ringing after the switching. In the turn-on transient, the same tendency, as was seen in the lower current comparison, is observed. The experimental transient is much slower than the simulated transient, also starting at a higher voltage, as a result of the low frequency oscillation not modelled in the simulation.

Looking at the bottom left chart, some more deviance is seen in the gate-source voltages. The experimental waveform exhibits considerable high frequency ringing, which is not seen in the simulation. The turn-on transient of the gate-source voltages has the same tendency as was seen in the lower current comparison.

9.3.1 Evaluation of SPICE Model Accuracy

The comparison between the experimental data and the LTSPICE simulation showed decent resemblance, especially in the turn-off transient. However, when looking at the turn-on transients, a considerable difference could be noted. This indicates that there are some behaviours of the circuit which are not replicated in the simulation. It can be concluded, that there is room for improvements in the simulation, in order to achieve a greater parity between the simulated data and experimental data. This would improve the digital design efficacy, as the physical properties could be represented more accurately.

Chapter 10

Discussion

This chapter will discuss and analyse this project, evaluating the validity of the tools and methods applied in this project. Moreover, sources of error which are deemed to have an influence on the validity of the objectives will be discussed.

10.1 Digital Design

In this project, a digital design process was used to optimise the design procedure of an electrical circuit. This process aimed to make the design process more effective. Digital design processes presented in previous papers were utilised. However, it was deemed that these lacked some key capabilities needed in order to optimise the digital design process. Therefore, new methods of evaluating digital circuits were conceived.

10.1.1 Data Processing

In a complex circuit with many relevant areas of parasitic composure, it had previously been difficult to easily evaluate a large number of parasitic components and loop inductances. By developing a method of evaluating the inductance matrices Ansys Q3D extracts from a given circuit, the process of numerical parasitic evaluation was optimised. This made it possible to numerically evaluate a greater extent of a given circuit than what would be feasible with previous methods. In this project, this method was used to analyse GD loop inductances, which made it possible to easily compare different design strategies. Moreover, this made the iterative process of circuit design quicker, allowing for a higher number of design iterations of a circuit to be thoroughly evaluated and compared.

10.1.2 Optimisation Process

The integration of LTspice and Matlab to sweep various component parameters in a non-linear system including the parasitic content is deemed to have a very high potential, especially if combined with optimisation methods and algorithms. Due to time and scope constraints of this project, a relatively simple optimisation method was used with unweighted optimisation parameters. If examined further, other parameters could have been evaluated to analyse the switching performance of the HB, and designated optimisation algorithms could have been used to efficiently find the optimum solution.

In the beginning of the optimisation process, a suitable FB was found with an non-optimised set of gate resistors, which was then kept constant to find the gate resistor values. It is possible that if the different FBs were simulated with a range of different gate resistors, another FB would have performed optimally. However, due to the many possible combinations of FBs and gate resistor values, the analysis would not have been able to be conducted within the time constraints of this project.

Furthermore, the parameter sweeps of the gate resistors were conducted rather unmethodologically by trying out few specific values. With an optimisation algorithm, a better combination of gate resistors could have been found. Alternatively, more sweeps could have been conducted for different

combinations. While this optimisation process was able to evaluate component combinations in terms of the defined optimisation parameters, it was found that it was necessary to investigate the simulated wave forms manually, in order to verify the performance. This suggests that more suitable optimisation parameters could be defined.

10.1.3 Accuracy of LTSpice Model

As the digital design process based on SPICE simulation relies on the accuracy of the estimated circuit parameters contained in the SPICE block, it is important that this block is realistic. When comparing the experimental data to the corresponding spice model in Section 9.3, it was found that some areas achieved excellent parity, while other areas saw some difference in transient response. Some possible causes of this difference could be considered:

Definition of Terminals in Ansys Q3D

When defining terminals, i.e. sources and sinks in Ansys Q3D, the surface of an object has to be selected as the terminal. In order to improve simulation result continuity, it was found that using a small object surface provided the best results. However, some electrical components, such as the GaN HEMTs have large pads as electrical connections. When defining the terminals of such components in the Ansys Q3D simulation, the whole pad was not used as the terminal, and a small object was placed in its stead, as this provided the best continuity when comparing results. This choice could have an influence on the validity of the simulation.

Frequency Dependent Parasitics

Given a circuit with large high frequency content such as the GaN HEMT HBs shown in this project, frequency dependent resistances and inductances will start to have an influence on the dynamics. However, to simplify the digital design process, it was chosen not to calculate these AC-parasitics, and only DC-parasitics were included. In order to accurately represent real circuit dynamics, one could dynamically change between these different parasitic representations, using DC-parasitics at lower frequencies, changing to AC-parasitics during transients. This would improve the model accuracy.

Probe Interference

During the testing of the different physical designs, PP026 passive probes from LeCroy were used to measure the drain-source and gate-source voltages of the low side devices. However, this adds additional capacitance across the drain-source and gate-source terminals thereby affecting the switching dynamics. The PP026 adds 10 pF across the measuring points [86], which is significant as the GS66508T only has 65 pF output capacitance [23]. As seen in Figure 8.12, a large overshoot in the drain current was observed when the current direction of the inductor current and current from the discharging output capacitance was the same. With the added capacitance from the PP026, this current overshoot is likely higher than simulated, which could potentially heat up the device more than expected. As a probe was only applied to a maximum of two devices, this could lead to some added difference in current distribution during transient periods. The effects on the measured gate-source voltage would

be increased charging time before the the device would turn-on, which could alter the symmetry during turn-on between the parallel devices in a negative way. As the probe placement can have an influence on the switching dynamics of the circuit, these should be included in the simulation model, to achieve optimal parity.

Inductance of Components

The results obtained from Ansys Q3D for the loop inductances only account for the parasitic inductance in the copper traces. The components were not considered, which left gaps in the copper traces, where the current would have passed through the components. This means that the cancellation effect, discussed in Section 5.3.3, in practice might be greater thereby yielding a lower loop inductance than shown by the data from Ansys Q3D. This could explain some of the differences between the simulation results and the experimental data. However, the ESL of the SMD components was not taken into account, which would have increased the total loop inductance seen in Chapter 6. Besides the common resistors and on and off capacitors, additional split resistors and FBs were added to the GD circuitry, which could perhaps have added as much as 1 nH in the GD loops [70].

Parameter Variation

In this project the LTspice model was designed without considering the parameter variance of the GaN HEMTs. In practice the threshold voltage V_{th} and on-resistance $R_{DS,on}$ will differ between the parallel devices, as mentioned in Section 2.2.3, which will affect the current distribution. The threshold voltage variation will influence the current sharing of devices during transients. The difference in on-resistance will impact the steady-state current distribution [26].

10.1.4 Thermal Analysis

In Chapter 7, models of the PCB designs were evaluated on their thermal performance. A parametric sweep of the heat transfer coefficient and different power dissipation levels allowed for analysing the junction temperature of the GaN HEMTs at a given operation point. This gives an approximation of the range of the heat transfer coefficient required to keep the devices within the SOA at a given power level, so that an appropriate cooling solution can be estimated. The model only incorporates the losses in the GaN HEMTs, which were assumed to be uniform. Further analysis could incorporate the power dissipation per device at a given load power based on simulation results, as well as the power losses in the PCB traces and other components present in the system, such as the Zener diode or the GD IC and power terminals. As the impact of these components was disregarded, the temperatures in the system could have been underestimated, which would mean that the heat transfer coefficient would have to be higher than what the simulation results showed.

Furthermore, the heat transfer coefficient was only swept for the thermal pad area of the GaN HEMTs, while the remaining parts of the PCB were cooled by natural convection. The influence of forced convection along the PCB surface could be examined to see whether the heat transfer coefficient of the thermal pad could be reduced by applying forced convection at a certain air velocity.

10.2 Experimental Results

In Chapter 9 the DPT of the different designs showed that there was room for improvement in all of the design strategies. The main focus throughout the project was on varying the electrical parameters on the power side and a generic, but optimised, GD layout was applied to the designs. However, it was seen that the GD layout was still too high in loop inductance as this is thought to be the main reason behind the failures experienced, which was verified by testing Design B at low voltages. It should still be noted that it was possible to obtain switching at 400 V and 60 A for Design A. This could be increased by improving on the GD layout.

Due to a lack of foresight, insufficient measurements were made on the first laboratory experiments. The experimental setup failed before sufficient measurements were made. The lack of measurements of the high side gate-source voltages and most of the low side devices meant that it was very difficult to analyse what exactly caused the initial failure of Design A. By having these measurements it could perhaps have been possible to improve on the PCB to ensure a higher operating point for all designs in the DPT.

The series of breakdowns with Design A and C impacted that number of probes were added to the system, i.e. two passive probes, two differential probes and two current probes. This raised the question of whether this high number of probes impacted the system dynamics and could add to the oscillations seen in the system.

10.3 Additional Considerations

10.3.1 Quasi-Common Source Inductance

In Section 2.3 on page 12, the importance of the quasi-common source inductances was established. However, it was deemed infeasible to apply this concept when more than two GaN HEMTs are paralleled, as it resulted in an overly complicated circuit with little physical meaning. Therefore, it was assumed that the source inductance had a strong correlation with the quasi-common inductance, i.e. a high symmetry in the source inductances corresponds to a high symmetry in the quasi-common inductances. This assumption has not been verified further and could lead to unidentified circulating currents due to a potential lack of symmetry of the quasi-common inductances. However, a small investigation into the quasi-common source inductance was performed, which can be seen in Appendix H on page 146.

This could be a factor in explaining the difference between the LTspice model and the experimental data. Also, in the experimental work, where Q7 in Design A experienced a breakdown, its performance could have been more affected due to a lower threshold voltage or higher on-resistance compared to its neighbouring devices. By implementing the minimum and maximum variation into the LTspice model the PCB design could have been made to function with these variations.

10.3.2 Low Frequency Ripple

The low frequency ripple seen on the drain-source voltage in Chapter 9 affected the actual switching performance of the devices. This made it difficult to evaluate the actual drain-source voltage overshoot of the devices and it could perhaps have affected the transient performance of the drain-source voltage. This decreases the validity of the drain-source voltage analysis and the impact of it should be taken into account for a future setup.

10.3.3 Placement of SMA Connectors

When placing the SMA connectors used for the measurements on the low side devices it was found that the distance between the connectors had been misjudged. This had the implication that it was not possible to connect the passive probes to two neighbouring measurement points. This meant that it was not possible to measure both the drain-source and gate-source voltages for one specific devices during testing. To be able to get both the drain-source and gate-source voltages two separate tests were required, whereafter the data could be combined later. This was not ideal because by moving the different probes around for each test could impact the measurements obtained, which could make it difficult to directly match the drain-source and gate-source voltage for a given device. This could lead to some inaccuracy in the analysis performed on the switching waveforms obtained from the DPT in Chapter 9.

10.3.4 Manual Soldering of 0402 Components

Some 0402 components had to be manually soldered, both due to tombstoning and errors in the component placement before vapor phase reflow soldering. With manual soldering, there is a larger possibility of a higher variance in the amount of solder, and thus could alter the individual current paths and parasitic content. This can lead to additional imbalances. As these manual corrections were mainly conducted on the sensitive GD circuit, where the 0402 components were used, this could have an impact on the switching performance

Chapter 11

Conclusion

In Chapter 3, the following research question was posed:

"How can a GaN HEMT based HB switching module with four GaN HEMTs in parallel be designed and optimised using a digital design process, and how can the digital design process be expanded upon to improve its capabilities?"

To answer the the research question, the circuit was analysed, and suitable components were chosen for the application. It was found that different areas of the circuit should be analysed and optimised in terms of parasitic composure. Using the digital design process, new iterations could be evaluated digitally, allowing for digital prototyping.

By researching previous works, some design priorities regarding parasitic composure could be set up. These were then evaluated using three physical prototypes, each incorporating different design strategies. The evaluation of these design criteria was unfulfilled, as the prototypes failed to function as intended. However, switching at 400 V and 50 A was achieved during a DPT which is deemed to be a success.

It was found that a proper GD layout with low and symmetrical inductances is vital in order to ensure a functioning module, and that this should be of high priority in the design process, when paralleling more than two GaN HEMTs.

The data processing is a major part of the digital design process and has previously been a time consuming process. This project optimised the data processing of Ansys Q3D results, making it possible to only perform a single FEA for every circuit, while still being able to numerically analyse the relevant loops, as well as self and mutual inductances.

Moreover, using Matlab to sweep component parameters in the LTspice simulation including the parasitic content of the circuit opened up the possibility to find the optimal component while taking the complex non-linearities of a realistic circuit into account. Previously, this was done experimentally, which is both time and resource consuming. Even though weaknesses in the applied optimisation theory were found, refining the applied methods can greatly enhance the digital design process.

Chapter 12

Future Work

In this chapter, considerations for future research and design improvements are listed.

12.1 Simulation Time

As the digital design and optimisation process is heavily dependent on the LTspice model it is crucial to consider ways of optimising the simulation time. With a reduced simulation time is would be possible to achieve more optimisation sweeps. This could be done by simplifying parts of the LTspice model, which were not necessary for the given optimisation sweep. As this is a very time consuming task, it could be crucial for a project with restricted time to minimise this time without compromising the validity of the optimisation results.

12.2 Thermal Design

The main priority of this project was to evaluate and optimise the electrical performance of a HB switching module with four GaN HEMTs in parallel with a DPT. The thermal performance of different design strategies was analysed in Section 2.5 order to determine the best compromise between electrical and thermal performance. However, for the practical evaluation of the module a cooling was not considered as this was not needed for the DPT.

The practical implementation of a thermal solution would have to be considered in the future work of the module in order to ensure that it can perform continuously. As was illustrated in Chapter 7 a lot of heat was dissipated in the module requiring a cooling solution with high performance.

The impact on the electrical performance would also have to be evaluated, as this could be affected, depending on the specific chosen thermal solution. It should be noted that the PCB design for the DPT was made with 2 oz external layer thickness and 1 oz internal. By increasing the thickness of the board the temperature of the traces could be reduced as the heat would be distributed over a larger volume.

12.3 Multiboard Design Strategy

For this project it was chosen to implement the GD circuitry on the same PCB as the power circuitry. However, this reduces the degrees of freedom in terms of altering the GD layout for the different design strategies presented in this project. As the same GD layout strategy was utilised for both Design A,B & C, it was not possible to determine the impact of placing the on and off loops differently. A different GD strategy could perhaps have increased the robustness of the GD to the noise from the power side of the PCB or lead to a overall decrease in inductance in the GD.

By placing the GD circuitry on a separate PCB, it could decrease the inductive coupling between the power and GD, which is an important factor to avoid as mentioned in Section 2.3. However, depending

on the connection between the GD and power boards there could be some added inductance due to long lead connections. This would have to be accounted for in the GD layout to ensure that the loop inductance would not affect the performance negatively.

Using a multiboard design would also allow for more flexibility if failure occurs as it would be possible to reuse the boards, which are unaffected by the failure. This could allow for less time soldering new PCBs and more time for experimental work. This could also make it easier to test different GD layouts, which in this project could have proven beneficial.

12.4 Failure Mode and Effects Analysis of PCBs

As discussed in Chapter 9, there was a lack of proper measurements for the first tests, especially for Design A. In order to fully understand what caused the failures in Design A and C it would be necessary to assemble a new PCB and perform new test. This time additional measurements would be performed, to gather information on both the high and low side drain-source and gate-source voltages. This would be the first step in order to properly determine the cause of the failure and thereby to determine the needed optimisation on the PCBs. Besides observing the drain-source and gate-source voltage it could be possible to add a Rogowski coil in the GD setup as the high and low side GD share the same power input and this could have a common-mode current circulating. This could originate from unequal voltages in the high and low side GD, which could be determined by using the Rogowski coil.

Bibliography

[1] Larry Spaziani and Lucas Lu. Silicon, GaN and SiC: There's room for all: An application space overview of device considerations. Proceedings of the International Symposium on Power Semiconductor Devices and ICs, 2018 May:Pages 8–11, 2018. ISSN 10636854. doi: 10.1109/ISPSD.2018.8393590.

[2] Fabrizio Roccaforte, Patrick Fiorenza, Giuseppe Greco, Raffaella Lo Nigro, Filippo Giannazzo, Ferdinando Iucolano, and Mario Saggio. Emerging Trends in Wide Band Gap Semiconductors (SiC and GaN) Technology for Power Devices. Microelectronic Engineering, 187-188:66–77, 2018. ISSN 01679317. doi: 10.1016/j.mee.2017.11.021. URL `https://doi.org/10.1016/j.mee.2017.11.021`. (Last Accessed: 25.05.2021).

[3] Chao Tsung Ma and Zhen Huang Gu. Review of GaN HEMT Applications in Power Converters Over 500 W. Electronics (Switzerland), 8(12), 2019. ISSN 20799292. doi: 10.3390/electronics8121401.

[4] Yan Berube, Amin Ghazanfari, Handy Fortin Blanchette, Christian Perreault, and Karim Zaghib. Recent Advances in Wide Bandgap Devices for Automotive Industry. IECON Proceedings (Industrial Electronics Conference), 2020 October:2557–2564, 2020. doi: 10.1109/IECON43393.2020.9254478.

[5] Ke Li, Paul Evans, and Mark Johnson. SiC/GaN Power Semiconductor Devices: A Theoretical Comparison and Experimental Evaluation Under Different Switching Conditions. IET Electrical Systems in Transportation, 8(1):3–11, 2018. ISSN 20429746. doi: 10.1049/iet-est.2017.0022.

[6] Niloufar Keshmiri, Deqiang Wang, Bharat Agrawal, Ruoyu Hou, and Ali Emadi. Current Status and Future Trends of GaN HEMTs in Electrified Transportation. IEEE Access, 8:70553–70571, 2020. ISSN 21693536. doi: 10.1109/ACCESS.2020.2986972.

[7] Giorgo Kapino, Alireza Kouchaki, Jesper Nielsen, and Morten Nymand. Simple Digital Model-Based Design and Implementation of Carrier-Based PWM for High Frequency Hybrid 3-L Active NPC Inverter. Proceedings - 2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering, CPE-POWERENG 2018, pages 1–6, 2018. doi: 10.1109/CPE.2018.8372519.

[8] Emre Gurpinar and Alberto Castellazzi. 600 V Normally-Off p-Gate GaN HEMT Based 3-level Inverter. 2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia, IFEEC - ECCE Asia 2017, pages 621–626, 2017. doi: 10.1109/IFEEC.2017.7992110.

[9] Zhongyi Quan and Yun Wei Li. Multilevel Converter Topologies with Internally Paralleled Power Stages. 2018 IEEE Energy Conversion Congress and Exposition, ECCE 2018, pages 5651–5656, 2018. doi: 10.1109/ECCE.2018.8558286.

[10] Christopher B. Barth, Pourya Assem, Thomas Foulkes, Won Ho Chung, Tomas Modeer, Yutian Lei, and Robert C.N. Pilawa-Podgurski. Design and Control of a GaN-Based, 13-Level, Flying Capacitor Multilevel Inverter. IEEE Journal of Emerging and Selected Topics in Power Electronics, 8(3):2179–2191, 2020. ISSN 21686785. doi: 10.1109/JESTPE.2019.2956166.

[11] Binxing Li, Rongchi Zhang, Nannan Zhao, Gaolin Wang, Junya Huo, Lianghong Zhu, and Dianguo Xu. GaN HEMT Driving Scheme of Totem-Pole Bridgeless PFC Converter. Proceedings - 2018 IEEE International Power Electronics and Application Conference and Exposition, PEAC 2018, 2018. doi: 10.1109/PEAC.2018.8590677.

[12] Shaobo Liu, Binxing Li, Rongchi Zhang, Nannan Zhao, Gaolin Wang, Junya Huo, Lianghong Zhu, Dianguo Xu, and Frede Blaabjerg. Impact of Parasitic Parameters on GaN HEMT Driving Module for Totem-pole Bridgeless PFC Converter. 2019 22nd International Conference on Electrical Machines and Systems, ICEMS 2019, 2019. doi: 10.1109/ICEMS.2019.8922463.

[13] Liang Zhou and YiFeng Wu. 99% Efficiency True-Bridgeless Totem-Pole PFC Based on GaN HEMTs. Power Conversion Intelligent Motion (PCIM), 2013. URL https://www.transphormchina.com/sites/default/files/transphorm/news/Totem-pole%20paper_0.pdf. (Last Accessed: 25.05.2021).

[14] Alicia Triviño-Cabrera, José M. González-González, and José A. Aguado. Fundamentals of Wireless Power Transfer. pages 1–18, 2020. ISSN 18604676. doi: 10.1007/978-3-030-26706-3_1.

[15] Juncheng Lucas Lu and Di Chen. Paralleling GaN E-HEMTs in 10kW-100kW Systems. Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, pages 3049–3056, 2017. doi: 10.1109/APEC.2017.7931131.

[16] Bingyao Sun, Rolando Burgos, Dushan Boroyevich, Sandeep Bala, and Jing Xu. 10 kW High Efficiency Compact GaN-Based DC/DC Converter Design. 2018 IEEE Energy Conversion Congress and Exposition, ECCE 2018, pages 6307–6313, 2018. doi: 10.1109/ECCE.2018.8557541.

[17] Juncheng Lu, Hua Bai, Alan Brown, Matt McAmmond, Di Chen, and Julian Styles. Design consideration of gate driver circuits and PCB parasitic parameters of paralleled E-mode GaN HEMTs in zero-voltage-switching applications. Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, 2016-May:529–535, 2016. doi: 10.1109/APEC.2016.7467923.

[18] Juncheng Lu, Hua Kevin Bai, Scott Averitt, Di Chen, and Julian Styles. An E-mode GaN HEMTs Based Three-Level Bidirectional DC/DC Converter Used in Robert Bosch DC-grid System. WiPDA 2015 - 3rd IEEE Workshop on Wide Bandgap Power Devices and Applications, pages 334–340, 2015. doi: 10.1109/WiPDA.2015.7369254.

[19] Timothy Boles. GaN-on-Silicon - Present Capabilities and Future Directions. AIP Conference Proceedings, 1934(February), 2018. ISSN 15517616. doi: 10.1063/1.5024484.

[20] GaN Systems Inc. GN001 Application Note - An Introduction to GaN Enhancement-mode HEMTs. 2020. URL https://gansystems.com/wp-content/uploads/2020/04/GN001_An-Introduction-to-GaN-E-HEMTs_200416.pdf. (Last Accessed: 25.05.2021).

[21] Bingyao Sun. Does GaN Have a Body Diode? - Understanding the Third Quadrant Operation of GaN. (February):1–7, 2019. URL https://www.ti.com/cn/lit/an/snoaa36/snoaa36.pdf?ts=1621921980598&ref_url=https%253A%252F%252Fwww.google.com%252F. (Last Accessed: 25.05.2021).

[22] Alex Lidow and Johan Strydom. Gallium Nitride (GaN) Technology Overview. Efficient Power Conversion Corporation, 2012. URL http://www.digikey.co.uk/Web%20Export/

Supplier%20Content/EfficientPowerConversion_917/PDF/epc-wp-wp001.pdf. (Last Accessed: 25.05.2021).

[23] GaN Systems Inc. GS66508T Top-side cooled 650 V E-mode GaN Transistor Preliminary Datasheet. pages 1–16, 2020. URL https://gansystems.com/wp-content/uploads/2020/04/GS66508T-DS-Rev-200402.pdf. (Last Accessed: 25.05.2021).

[24] Juncheng Lu, Ruoyu Hou, and Di Chen. Loss Distribution Among Paralleled GaN HEMTs. 2018 IEEE Energy Conversion Congress and Exposition, ECCE 2018, pages 1914–1919, 2018. doi: 10.1109/ECCE.2018.8557988.

[25] Alan Elbanhawy. Effect of Source Inductance on MOSFET Rise and Fall Times. Maplesoft - Application demonstration, 2008. URL https://www.maplesoft.com/applications/view.aspx?SID=5730&view=html. (Last Accessed: 25.05.2021).

[26] Helong Li, Stig Munk-Nielsen, Xiongfei Wang, Ramkrishan Maheshwari, Szymon Beczkowski, Christian Uhrenfeldt, and W. Toke Franke. Influences of Device and Circuit Mismatches on Paralleling Silicon Carbide MOSFETs. IEEE Transactions on Power Electronics, 31(1):621–634, 2016. ISSN 08858993. doi: 10.1109/TPEL.2015.2408054.

[27] Infineon. IGOT60R070D1. pages 1–17, 2020. URL https://www.infineon.com/dgdl/Infineon-IGOT60R070D1-DataSheet-v02_12-EN.pdf?fileId=5546d46265f064ff016685fa65066523. (Last Accessed: 25.05.2021).

[28] Yingying Gui. Gate Driver for Phase Leg of Parallel Enhancement-Mode Gallium-Nitride (GaN). 2018. URL https://vtechworks.lib.vt.edu/handle/10919/83516. (Last Accessed: 25.05.2021).

[29] Y. F. Wu. Paralleling High-Speed GaN Power HEMTs for Quadrupled Power Output. Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, pages 211–214, 2013. doi: 10.1109/APEC.2013.6520210.

[30] Nidhi Haryani, Jun Wang, Rolando Burgos, and Rolando Haryani, Nidhi; Wang, Jun; Burgos. Paralleling 650V/60A GaN HEMTs for High Power High Efficiency Applications. IEEE Energy Conversion Congress and Exposition (ECCE), pages 3663–3668, 2017. doi: 10.1109/ECCE.2017.8096649.

[31] X. Jorda, X. Perpina, M. Vellvehi, D. Sanchez, A. Garcia, and A. Avila. Analysis of Natural Convection Cooling Solutions for GaN HEMT Transistors. 2018 20th European Conference on Power Electronics and Applications, EPE 2018 ECCE Europe, pages 1–8, 2018. URL https://ieeexplore.ieee.org/document/8515557. (Last Accessed: 25.05.2021).

[32] GaN Systems Inc. GN003 Application Note - Measurement Techniques for High-Speed GaN E-HEMTs. (August):1–26, 2018. URL https://gansystems.com/wp-content/uploads/2018/08/GN003-Measurement-Techniques-for-High-Speed-GaN-E-HEMTs_20180816.pdf. (Last Accessed: 25.05.2021).

[33] GaNPower. GPI65060DFN - Datasheet. 2021. URL http://iganpower.com/wp-content/uploads/2019/11/GPI65060DFN.pdf. (Last Accessed: 25.05.2021).

[34] GaN Systems. GS66516T Top-side cooled 650 V E-mode GaN transistor Datasheet. pages 1–16, 2018. URL https://gansystems.com/wp-content/uploads/2020/04/GS66516T-DS-Rev-200402.pdf. (Last Accessed: 25.05.2021).

[35] Alejandro Rujas. Thermal Performance Analysis of GaN-Based High-Power Converters Characterization of GaN Devices. 2018 20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), pages 1–10, 2018. URL https://ieeexplore.ieee.org/document/8515551. (Last Accessed: 25.05.2021).

[36] Fujiang Lin, Weiqiang Qian, Lei Li, and Mehdi Khan. GaN device and modeling with emphasis on trapping effect and thermal challenges for PA design (Invited). 2015 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications, IEEE MTT-S IMWS-AMP 2015 - Proceedings, pages 15–17, 2015. doi: 10.1109/IMWS-AMP.2015.7324951. URL https://ieeexplore.ieee.org/document/7324951. (Last Accessed: 25.05.2021).

[37] Raoul Guggenheim and Lior Rodes. Roadmap Review for Cooling High-Power GaN HEMT Devices. 2017 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems, COMCAS 2017, November:1–6, 2017. doi: 10.1109/COMCAS.2017.8244734.

[38] Chieh-an Wang, Hsin-ping Chou, Stone Cheng, and Po-chien Chou. In Depth Thermal Analysis of Packaged GaN on Si Power Devices. 25th International Symposium on Power Semiconductor Devices & ICs (ISPSD), pages 101–104, 2013. ISSN 19460201. doi: 10.1109/ISPSD.2013.6694406.

[39] Yoonjin Won, Jungwan Cho, Damena Agonafer, Mehdi Asheghi, and Kenneth E. Goodson. Cooling Limits for GaN HEMT Technology. Technical Digest - IEEE Compound Semiconductor Integrated Circuit Symposium, CSIC, 2013. ISSN 15508781. doi: 10.1109/CSICS.2013.6659222.

[40] Bainan Sun, Niels Elkjaer Iversen, Zhe Zhang, and Michael A.E. Andersen. Research of Gap Filler Material in the GaN Transistor Thermal Management. ICPE 2019 - ECCE Asia - 10th International Conference on Power Electronics - ECCE Asia, pages 390–395, 2019. doi: 10.23919/ICPE2019-ECCEAsia42246.2019.8796905.

[41] STMicroelectronics. TO-247 image. 2021. URL https://media.digikey.com/Renders/STMicro%20Renders/TO-247-3-HiP.jpg. (Last Accessed: 25.05.2021).

[42] GaN Systems Inc. GN002 Application Note - Thermal Design for GaN Systems Top-side Cooled GaNPX®-T Packaged Devices. 2018. URL https://gansystems.com/wp-content/uploads/2018/10/GN002_Thermal-Design-Guide-for-Top-Side-Cooled-GaNpx-T-Devices_Rev-181030.pdf. (Last Accessed: 25.05.2021).

[43] Gan Systems Inc. GN002 Application Note - Thermal Design for Packaged GaNPX® Devices. 2018. URL https://gansystems.com/wp-content/uploads/2021/03/GN002-Thermal-Design-for-GaNPX-Packaged-Devices-Rev.201127-1.pdf. (Last Accessed: 25.05.2021).

[44] Texas Instruments. Thermal Considerations for Designing a GaN Power Stage. (October):1–12, 2018. URL https://www.ti.com/lit/an/snoaa14b/snoaa14b.pdf?ts=1621948160513. (Last Accessed: 25.05.2021).

[45] Vishay. ThermaWick TM Thermal Jumper Surface Mount Chip. pages 1–3, 2020. URL https://www.vishay.com/docs/60157/thjp.pdf. (Last Accessed: 25.05.2021).

[46] Juncheng Lu, Di Chen, and Lyubov Yushyna. A High Power-Density and High Efficiency Insulated Metal Substrate Based GaN HEMT Power Module. 2017 IEEE Energy Conversion Congress and Exposition, ECCE 2017, 2017-January:3654–3658, 2017. doi: 10.1109/ECCE.2017.8096647.

[47] Pavel Skarolek and Jiri Lettl. GaN Transistors Cooling Options Comparison. International Conference on Electical Drives and Power Electronics, 2019-September:323–326, 2019. ISSN 13393944. doi: 10.1109/EDPE.2019.8883894.

[48] Chenjiang Yu, Cyril Buttay, and Éric Labouré. Thermal Management and Electromagnetic Analysis for GaN Devices Packaging on DBC Substrate. IEEE Transactions on Power Electronics, 32(2):906–910, 2017. ISSN 08858993. doi: 10.1109/TPEL.2016.2585658.

[49] Bainan Sun, Zhe Zhang, and Michael A.E. Andersen. Research of Low Inductance Loop Design in GaN HEMT Application. Proceedings: IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society, pages 1466–1470, 2018. doi: 10.1109/IECON.2018.8591732.

[50] Zäch, Mike Robin , I Gardi, Sigmundur and Olsen, Simon. Digital Design and Optimisation of a Bridgeless Totem-Pole PFC Converter Using Finite-Element Analysis. 2020. URL https://drive.google.com/file/d/1DKCOmuyPMXLER-gxyM0kC46NnTDBNFu0/view?usp=sharing. (Last Accessed: 25.05.2021).

[51] Asger Bjørn Jørgensen. Packaging of Wide Bandgap Power Semiconductors using Simulation-based Design. APETT - Advanced Power Electronic Technology and Tools, 2019.

[52] Asger Bjorn Jorgensen, Stig Munk-Nielsen, and Christian Uhrenfeldt. Overview of Digital Design and Finite-Element Analysis in Modern Power Electronic Packaging. IEEE Transactions on Power Electronics, 35(10):10892–10905, 2020. ISSN 19410107. doi: 10.1109/TPEL.2020.2978584.

[53] GaN Systems Inc. GN001 Application Note - How to Drive GaN Enhancement Mode Power Switching Transistors. pages 1–13, 2014. URL https://www.mouser.com/catalog/additional/GaN%20Systems_GN001%20App%20Note%202014-10-21.pdf?fbclid=IwAR2O2nl3phsn29UKw-T1SQhUNQ9KyhF_q_XTFdOviihbDUtJ37DBnrcFcZQ. (Last Accessed: 25.05.2021).

[54] Jasbir Arora. Introduction to Optimum Design. 2012. doi: 10.1016/C2009-0-61700-1.

[55] Laszlo Balogh. Fundamentals of MOSFET and IGBT Gate Driver Circuits. Application Report, (October):1–48, 2017. ISSN 1083-351X. URL https://www.ti.com/lit/ml/slua618a/slua618a.pdf?ts=1621961211178&ref_url=https%253A%252F%252Fwww.google.com%252F&fbclid=IwAR3qZ00Zju0OLCp3qLRwndCUPeYb-LSwQgq8V7gdfy6whpOvQr6fDpI9yF8l. (Last Accessed: 25.05.2021).

[56] ON semiconductor. MMSZ5221BT1 Datasheet - Series Zener Voltage Regulators. pages 1–6, 2006. URL https://www.onsemi.com/pdf/datasheet/mmsz5221bt1-d.pdf. (Last Accessed: 25.05.2021).

[57] On Semiconductor. AN-6076 Design and Application Guide of Bootstrap Circuit for High Voltage MOSFETs. pages 1–15, 2008. URL https://www.onsemi.com/pub/Collateral/AN-6076.pdf. (Last Accessed: 25.05.2021).

[58] Avago Technologies. Datasheet SFH551. pages 1–5. URL https://manualzz.com/doc/19753864/sfh551-1-1-and-sfh551-1-1v-receiver-with-digital-output-s... (Last Accessed: 25.05.2021).

[59] Texas Instruments. Datasheet - SN74LVC1G04 Single Inverter Gate. (April 1999), 2007. URL https://www.ti.com/lit/ds/symlink/sn74lvc1g04.pdf?ts=1621964438270&ref_url=https%253A%252F%252Fwww.google.com%252F. (Last Accessed: 25.05.2021).

[60] Silicon Labs. Si827x DataSheet. pages 0–42, 2015. URL https://www.silabs.com/documents/public/data-sheets/Si827x.pdf. (Last Accessed: 25.05.2021).

[61] Recom. Datasheet - DC/DC Converter 1 Watt SIP7 Single and Dual Output. pages 1–8, 2019. URL http://www.farnell.com/datasheets/2787753.pdf. (Last Accessed: 15.12.2020).

[62] Jeffrey Agarwal, Anant; Lang. Foundations of Analog and Digital Electronics. Paperback. Morgan Kaufman, 1st edition, 2005. ISBN-13: 9780080506814.

[63] Toshiba Electronic Devices & Storage Corporation. MOSFET Parallening (Parasitic Oscillation between Parallel Power MOSFETs). pages 1–21, 2018.

[64] Alpha & Omega Semiconductor. Paralleling Power MOSFETs in Switching Applications. pages 1–8, 2013. URL http://www.aosmd.com/res/application_notes/mosfets/MOS-010.pdf. (Last Accessed: 25.05.2021).

[65] Zhan Wang, Jim Honea, Yuxiang Shi, and Hui Li. Investigation of driver circuits for GaN HEMTs in leaded packages. 2nd IEEE Workshop on Wide Bandgap Power Devices and Applications, WiPDA 2014, (LV):81–87, 2014. doi: 10.1109/WiPDA.2014.6964629.

[66] Fangwei Zhao, Yan Li, Qing Tang, and Lu Wang. Analysis of Oscillation in Bridge Structure Based on GaN Devices and Ferrite Bead Suppression Method. 2017 IEEE Energy Conversion Congress and Exposition, ECCE 2017, 2017-January:391–398, 2017. doi: 10.1109/ECCE.2017.8095809.

[67] F. Stueckler, J. Hancock, and E. Vecino. CoolMOS ™ C7 : Mastering the Art of Quickness CoolMOS ™ C7 Technology and Design Guide. Infineon, (April):1–30, 2013. URL https://www.infineon.com/dgdl/Infineon-ApplicationNote_650V_CoolMOS_C7_Mastering_the_Art_of_Quickness-AN-v01_00-EN.pdf?fileId=db3a30433e5a5024013e6a966779640b. (Last Accessed: 25.05.2021).

[68] Jonathan Dodge. Eliminating Parasitic Oscillation between Parallel MOSFETs. Advanced Power Technology, 2003. URL https://www.microsemi.com/document-portal/doc_download/14693-eliminating-parasitic-oscillation-between-parallel-mosfets. (Last Accessed: 25.05.2021).

[69] VISHAY. Capacitance and Esr. page 1, 2017. URL https://www.vishay.com/docs/48298/_did-you-know-aluminum-parasitics_vmn-ms7377-1710.pdf. (Last Accessed: 25.05.2021).

[70] Jeffrey Cain. Parasitic Inductance of Multilayer Ceramic Capacitors. URL https://www.avx.com/docs/techinfo/CeramicCapacitors/parasitc.pdf. (Last Accessed: 25.05.2021).

[71] Johanson Dielectrics. Basics of Ceramic Chip Capacitors. pages 1–14, 2007. URL https://www.johansondielectrics.com/downloads/basics-of-ceramic-chip-capacitors.pdf. (Last Accessed: 25.05.2021).

[72] Mohammad S. Sharawi. Practical Issues in High Speed PCB Design. IEEE Potentials, 23(2): 24–27, 2004. ISSN 02786648. doi: 10.1109/MP.2004.1289994.

[73] John Ardizzoni. A Practical Guide to High-Speed PCB Layout. Analog Dialogue, vol. 39, no. 9, pages 1–6, 2005. URL https://www.analog.com/media/en/analog-dialogue/volume-39/number-3/articles/high-speed-printed-circuit-board-layout.pdf. (Last Accessed: 25.05.2021).

[74] Andrew J. McDowell and Todd H. Hubing. Parasitic Inductance Cancellation for Surface Mount Shunt Capacitor Filters. IEEE Transactions on Electromagnetic Compatibility, 56(1):74–82, 2014. ISSN 00189375. doi: 10.1109/TEMC.2013.2271257.

[75] Lyesse Laloui and Alessandro F. Rotta Loria. Analysis and Design of Energy Geostructures. Elsevier, 2019. ISBN 978-0-12-820623-2.

[76] Asger Bjorn Jorgensen, Szymon Beczkowski, Christian Uhrenfeldt, Niels Hogholt Petersen, Soren Jorgensen, and Stig Munk-Nielsen. A Fast-Switching Integrated Full-Bridge Power Module Based on GaN eHEMT Devices. IEEE Transactions on Power Electronics, 34(3):2494–2504, 2019. ISSN 08858993. doi: 10.1109/TPEL.2018.2845538.

[77] Cheng Qian, Amir Mirza Gheitaghy, Jiajie Fan, Hongyu Tang, Bo Sun, Huaiyu Ye, and Guoqi Zhang. Thermal Management on IGBT Power Electronic Devices and Modules. IEEE Access, 6: 12868–12884, 2018. ISSN 21693536. doi: 10.1109/ACCESS.2018.2793300.

[78] Robert Skuriat and C. M. Johnson. Direct Substrate Cooling of Power Electronics. CIPS 2008 - 5th International Conference on Integrated Power Electronics Systems, Proceedings, pages 339–344, 2008.

[79] Issam Mudawar, Desikan Bharathan, Kenneth Kelly, and Sreekant Narumanchi. Two-phase spray cooling of hybrid vehicle electronics. IEEE Transactions on Components and Packaging Technologies, 32(2):501–512, 2009. ISSN 15213331. doi: 10.1109/TCAPT.2008.2006907.

[80] Daniel Kearney, Slavo Kicin, Enea Bianda, Andrej Krivda, and David Bauman. PCB Embedded Power Electronics for Low Voltage Applications. CIPS 2016 - 9th International Conference on Integrated Power Electronics Systems, pages 3–8, 2019. URL https://ieeexplore.ieee.org/document/7736700. (Last Accessed: 25.05.2021).

[81] Gudrun Feix, Eckart Hoene, Oleg Zeiter, and Kristian Pedersen. Embedded Very Fast Switching Module for SiC Power MOSFETs. PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of, (May):19–21, 2015. URL https://ieeexplore.ieee.org/document/7148825. (Last Accessed: 25.05.2021).

[82] GaN Systems Inc. LTspice Model User Guide. pages 1–7, 2017. URL https://gansystems.com/wp-content/uploads/2018/05/LTspice-Model-User-Guide.pdf. (Last Accessed: 25.05.2021).

[83] GaN Systems Inc. GN004 Application Note - Design Considerations of Paralleled GaN HEMTs. 2020. URL https://gansystems.com/wp-content/uploads/2020/09/GN004-Design-Considerations-of-Paralleled-GaN-HEMTs_200910.pdf. (Last Accessed: 25.05.2021).

[84] Texas Instruments. TMS320F2823x Digital Signal Controllers. page 203, 2016. URL http://www.ti.com/lit/ds/symlink/tms320f28335.pdf. (Last Accessed: 15.12.2020).

[85] KEMET. Datasheet DC-Link Capacitor. pages 1–16, 2021. URL https://content.kemet.com/datasheets/KEM_A4020_ALC10.pdf. (Last Accessed: 25.05.2021).

[86] Teledyne Lecroy. PP026 User Manual. 2020. URL http://cdn.teledynelecroy.com/files/manuals/pp026-passive-probe-om.pdf. (Last Accessed: 25.05.2021).

[87] Suvankar Biswas, David Reusch, Michael de Rooij, and Tom Neville. Application Note 23 - Accurately Measuring High Speed GaN Transistors. pages 1–6, 2017. URL https://epc-co.com/epc/Portals/0/epc/documents/application-notes/AN023%20Accurately%20Measuring%20High%20Speed%20GaN%20Transistors.pdf. (Last Accessed: 25.05.2021).

[88] Tektronix. Tekteonix P5200A High Voltage Differential Probes - Datasheet. pages 1–6, 2017. URL https://uk.tek.com/probes-and-accessories/high-voltage-differential-probes. (Last Accessed: 25.05.2021).

[89] Teledyne Lecroy. Teledyne LeCroy CP150 Current Probe - Datasheet. pages 1–4, 2017. URL http://cdn.teledynelecroy.com/files/pdf/current-probes-datasheet.pdf. (Last Accessed: 25.05.2021).

[90] Teledyne Lecroy. HDO6000 Datasheet. pages 1–20. URL http://cdn.teledynelecroy.com/files/pdf/hdo6000_oscilloscope_datasheet.pdf. (Last Accessed: 25.05.2021).

[91] Toshiba. MOSFET Self-Turn-On Phenomenon. pages 1–19, 2018. URL https://toshiba.semicon-storage.com/info/docget.jsp?did=59473. (Last Accessed: 25.05.2021).

[92] M. Ouda and A. Sebak. Efficient Method for Frequency Dependent Inductance and Resistance Calculations. IEEE WESCANEX Communications, Power, and Computing, 2:473–477, 1995. doi: 10.1109/wescan.1995.494076.

[93] Emre Gurpinar, Francesco Iannuzzo, Yongheng Yang, Alberto Castellazzi, and Frede Blaabjerg. Design of Low-Inductance Switching Power Cell for GaN HEMT Based Inverter. IEEE Transactions on Industry Applications, 54(2):1592–1601, 2018. doi: 10.1109/TIA.2017.2777417.

Appendix A

GaN Switching Frequency Content

In order to determine what frequency content the switching of the GaN HEMTs will send into the circuit, an LTspice model of a single GaN HEMT is created, and a single switching of the device is measured. This device is switched at approximately 18 A for this test.

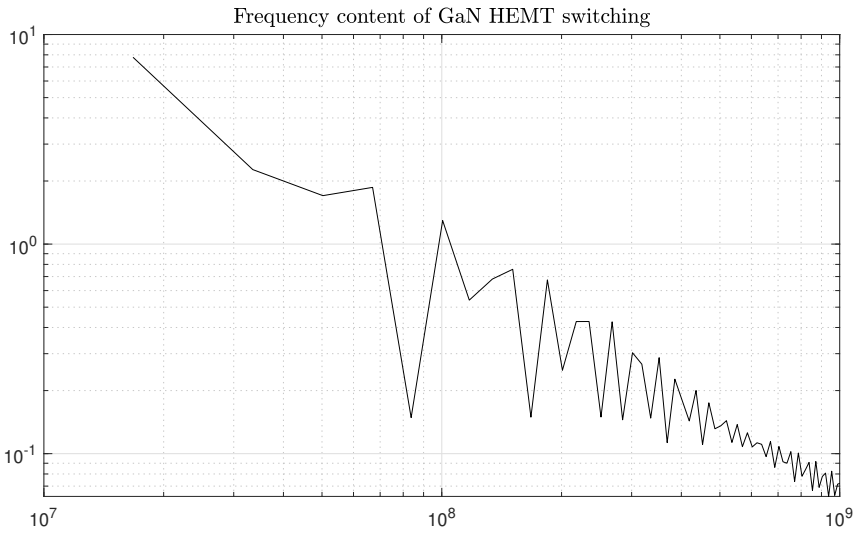


Figure A.1: Frequency response of GaN HEMT switching. The unit of the x axis is [Hz], y axis is [A].

Looking at Figure A.1, it can be seen that the switching results in amplitudes of around 1 A at 100 MHz. In order to effectively shunt this high frequency current, the capacitor and the circuit it is contained within must be carefully considered.

Appendix B

LTspice Model

B.1 LTspice Example Code

```
* BEGIN ANSOFT HEADER
* node 1     Net2:Source3
* node 2     Net2:Source4
* node 3     Net1:Source1
* node 4     Net1:Source2
* node 5     Net2:Sink2
* node 6     Net1:Sink1
* END ANSOFT HEADER

.subckt Ckt_3term2net 1 2 3 4 5 6
XZhalf1 1 2 3 4 9 10 11 12 Ckt_3term2net_half
XY1 9 10 11 12 Ckt_3term2net_parlel
XZhalf2 9 10 11 12 5 5 6 6 Ckt_3term2net_half

.subckt Ckt_3term2net_half 1 2 3 4 5 6 7 8
V1 1 9 dc 0.0
V2 2 10 dc 0.0
V3 3 11 dc 0.0
V4 4 12 dc 0.0
R1 9 13 0.0110539148758
R2 10 14 0.0125674975612
R3 11 15 0.0111239153611
R4 12 16 0.0125842742075
F1_2 13 9 V2 0.566431
F2_1 14 10 V1 0.498212
F3_4 15 11 V4 0.564783
F4_3 16 12 V3 0.499242
L1 13 5 6.60426166846e-11
L2 14 6 9.36774099447e-11
L3 15 7 6.63379963476e-11
L4 16 8 9.37440268717e-11
K1_2 L1 L2 0.595842
K1_3 L1 L3 0.738515
K1_4 L1 L4 0.466227
K2_3 L2 L3 0.468592
K2_4 L2 L4 0.783815
K3_4 L3 L4 0.595586
.ends Ckt_3term2net_half

.subckt Ckt_3term2net_parlel 1 2 3 4
```

```
41 RG1_3 1 3 486164.96217
42 RG1_4 1 4 486164.96217
43 RG2_3 2 3 486164.96217
44 RG2_4 2 4 486164.96217
45 R3_0 3 0 5245432002.43
46 R4_0 4 0 5245432002.43
47 C1_0 1 0 1.67922926178e-15
48 C1_3 1 3 1.75930951081e-14
49 C1_4 1 4 1.75930951081e-14
50 C2_0 2 0 1.67922926178e-15
51 C2_3 2 3 1.75930951081e-14
52 C2_4 2 4 1.75930951081e-14
53 C3_0 3 0 1.67146922436e-15
54 C4_0 4 0 1.67146922436e-15
55 .ends Ckt_3term2net_parlel
56
57 .ends Ckt_3term2net
```

B.2 LTspice Schematic

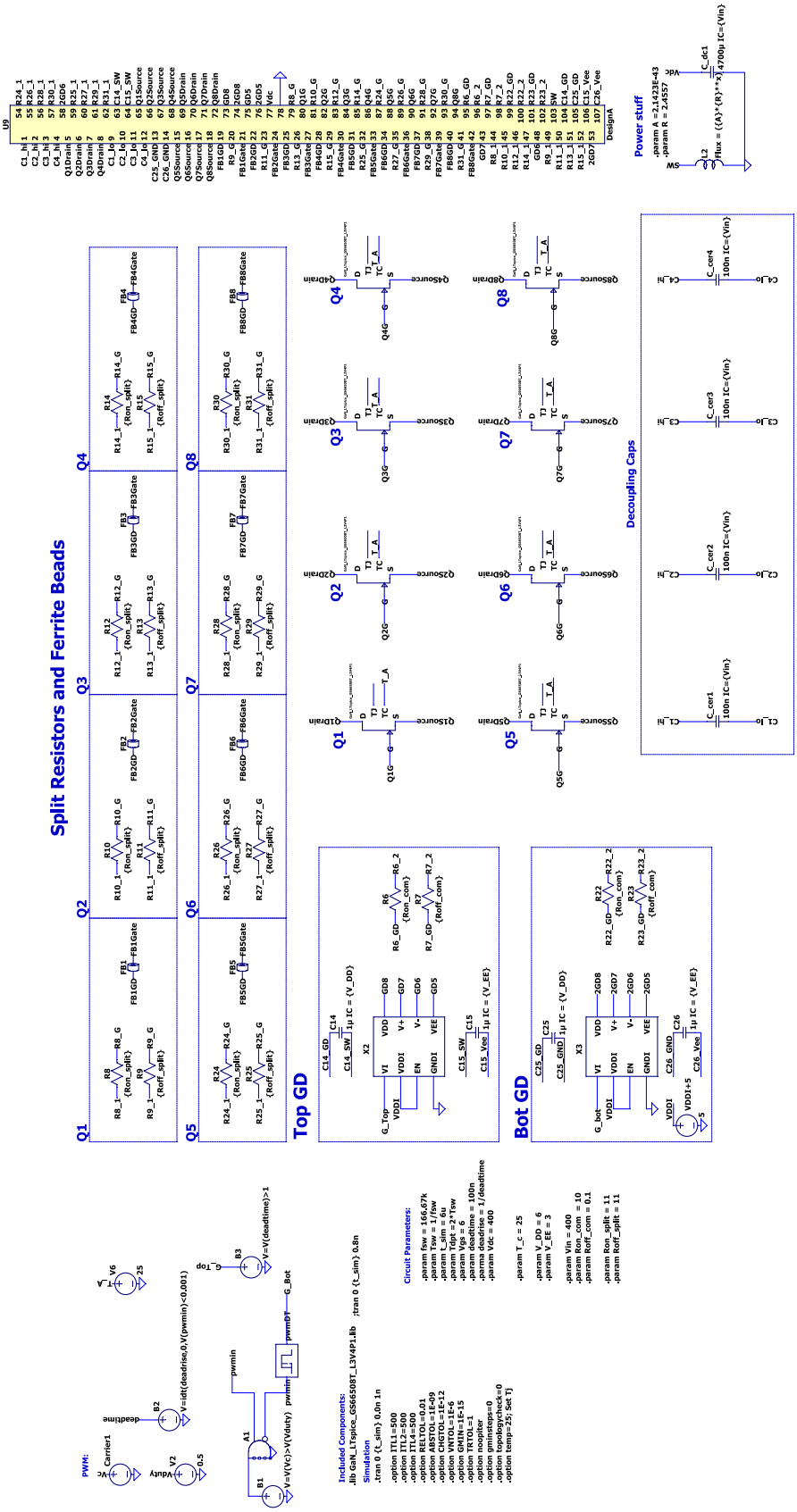


Figure B.1: LTspice circuit with parasitics included.

Appendix C

Ferrite Bead List

The following FBs have been simulated in LTspice:

Ferrite Number	L [µH]	R_{ser} [Ω]	R_{par} [Ω]	C_{par} [pF]	f_r [MHz]	Z_{max} [Ω]	I_{pk} [A]	Manufacturer	Part No.
1	0.194	0.118	122	0.153	923.79	122	0.3	Würth Elektronik	74279270 WE-CBF 0402
2	0.04	0.016	10.9	3.2	444.85	11	0.5	Würth Elektronik	742792701 WE-CBF 0402
3	0.38	0.245	200	0.35	436.41	200	0.5	Würth Elektronik	74279271 WE-CBF 0402
4	0.022	0.044	13	1.6	848.30	13	0.5	Würth Elektronik	7427927110 WE-CBF 0402
5	0.2	0.34	850	0.337	613.04	850	0.35	Würth Elektronik	7427927112 WE-CBF 0402
6	0.053	0.023	108	0.209	1512.20	108	0.3	Würth Elektronik	7427927130 WE-CBF 0402
7	0.985	0.138	145	0.33	279.15	145	0.3	Würth Elektronik	742792716 WE-CBF 0402
8	1.6	0.3	930	0.54	171.22	930	0.4	Würth Elektronik	7427927160 WE-CBF 0402
9	0.12	0.256	655	0.6	593.14	655	0.4	Würth Elektronik	7427927170 WE-CBF 0402
10	0.39	0.167	230	0.288	474.89	230	0.4	Würth Elektronik	7427927218 WE-CBF 0402
11	1.6	0.505	570	0.36	209.71	571	0.3	Würth Elektronik	7427927291 WE-CBF 0402
12	0.622	0.2	24	0.348	342.09	24	0.3	Würth Elektronik	74279273 WE-CBF 0402
13	0.26	0.08	130	0.38	506.34	130	1.2	Würth Elektronik	742792731 WE-CBF 0402
14	0.33	0.012	12	2	195.91	12	2	Würth Elektronik	7427927310 WE-CBF 0402
15	0.3	0.08	135	0.3	530.52	135	1.2	Würth Elektronik	7427927311 WE-CBF 0402
16	0.178	0.1	73	0.38	611.95	73	1.2	Würth Elektronik	7427927370 WE-CBF 0402
17	0.108	0.25	39	0.266	939.00	39	0.3	Würth Elektronik	74279274 WE-CBF 0402
18	0.106	0.152	71	0.063	1947.59	71	0.3	Würth Elektronik	74279276 WE-CBF 0402
19	0.273	0.35	102	0.255	603.21	102	0.3	Würth Elektronik	74279277 WE-CBF 0402
20	0.67	0.115	270	0.42	300.03	270	0.3	Würth Elektronik	742792780 WE-CBF 0402
21	0.46	0.26	540	0.128	655.90	540	0.5	Würth Elektronik	742843122 WE-CBF HF 0402
22	0.6	0.219	120.5	0.279	388.99	121	0.3	Würth Elektronik	782422101 WE-CBA 0402
23	0.43	0.184	330	0.37	399.01	330	0.3	Würth Elektronik	782422221 WE-CBA 0402
24	0.78	0.359	535	0.445	270.14	535	0.3	Würth Elektronik	782422331 WE-CBA 0402
25	0.0232	0.023	14	0.057	4376.62	14	1.5	Würth Elektronik	782423100 WE-CBA 0402
26	0.125	0.0657	154	0.349	762.00	154	1.2	Würth Elektronik	782423700 WE-CBA 0402

Table C.1: List of simulated FBs.

Appendix D

Gate Resistor Sweeps

D.1 Design A

For Design A, the following split resistances were simulated:

Design A			
Sim. Nr.	**$R_{split,on}$ [Ω]**	**$R_{split,off}$ [Ω]**	**Stable?**
1	0.1	0.1	Yes
2	0.1	1	Yes
3	0.1	5	Yes
4	1	0.1	No
5	1	1	No
6	1	5	Yes
7	1	10	Yes
8	5	0.1	Yes
9	5	1	Yes
10	5	5	Yes
11	5	10	No
12	10	0.1	No
13	10	1	Yes
14	10	5	No
15	10	10	No
16	0.1	10	Yes
17	0.5	10	No
18	2	10	Yes
19	3	10	Yes
20	4	10	Yes

Table D.1: Overview of simulated split resistor combinations for Design A.

D.2 Design B

The simulated combinations of the split resistors for Design B can be seen in Table D.2

Design B			
Sim. Nr.	**$R_{split,on}$ [Ω]**	**$R_{split,offF}$ [Ω]**	**Stable?**
1	0.1	0.1	Yes
2	0.1	1	Yes
3	0.1	5	Yes
4	0.1	10	Yes
5	1	0.1	Yes
6	1	1	No
7	1	5	Yes
8	1	10	No
9	5	0.1	Yes
10	5	1	No
11	5	5	Yes
12	5	10	Yes
13	10	10	Yes
14	10	1	No
15	10	5	Yes
16	10	0.1	Yes
17	0.1	8	No
18	12	10	No
19	2	2	Yes
20	3	4	Yes
21	4	2	No
22	3	1	Yes
23	2	4	Yes

Table D.2: Overview of simulated split resistor combinations for Design B.

D.3 Design C

The simulated combinations of split resistors for Design C can be seen in Table D.3

Design C			
Sim. Nr.	**$R_{split,on}$ [Ω]**	**$R_{split,off}$ [Ω]**	**Stable?**
1	0.1	0.1	No
2	0.1	1	No
3	0.1	5	No
4	0.1	10	Yes
5	1	0.1	Yes
6	1	1	Yes
7	1	5	Yes
8	1	10	Yes
9	5	0.1	Yes
10	5	1	Yes
11	5	5	Yes
12	5	10	No
13	10	1	Yes
14	10	5	No
15	10	10	Yes

Table D.3: Overview of simulated split resistor combinations for Design C.

Appendix E

Matlab Code

```
function [Lloop1,LrelevantSimple] = findloopinductance(filename,loopnodes)
%findloopinductance This function returns the calculated loop inductance
%from the Ansys q3d file you specify, and which nodes are in the loop
%   The Ansys q3d data should be saved as a .csv, including only the DC
%   resistance and inductance.
%Input the filename of the .csv file, as well as the nodes to be analysed.
%Output is [1] the loop inductance (single number) [2] The loop inductance
%matrix(includes self-inductances and mutual inductances.
%Example: Q1ONnodes = ["Q1Gate", "R_R8_N",  "R_R8_P",  "R_R6_N", "R_R6_P", "GD7", "GD8", "C_C14_P" "C_C14_N", "Q1Source"];
%[Q1ONloop, Q1ONM] = findloopinductanceV3(fname1,Q1ONnodes)

Loop1 = loopnodes;

% First, we extract the data
name = filename;
Ldataraw = readmatrix(name);                                %Reading data. (MUST BE SAVED AS CSV WITH MATRIX. ONLY INCLUDE DC RES AND INDUCTANCE
Ldataraw(:,1) = [];                                         %Deleting first column (just NaNs)
Ldataraw(:,end) = [];                                       %Deleting last colum   (just NaNs
sz = size(Ldataraw);                                        %Fidning the size of the matrix, which is diagonally symmetrical. I found the number of columns, need to delete excessive rows now
Ldata = Ldataraw;                                           %Taking a copy
Ldata(sz(2)+1:end,:) = [];                                  %Deleting excess rows(below)

% Then we extract the labels
Llabelsraw = readcell(name);

sz2 = size(Llabelsraw);                                     %Size of raw labels matrix
for n = 1:sz2(1)                                            %For loop to isolate DC inductance labels
    if contains(Llabelsraw(n,1),'DC Inductance Matrix')     %Finding where Inductance starts
```

```
29              Lindex = n;
30      end
31      if contains(Llabelsraw(n,1),'DC Resistance Matrix')          %Finding
            where Resistance starts
32              Rindex = n;
33      end
34  end
35
36  Llabels1 = Llabelsraw;                                           %Taking
        copy
37  Llabels1(1:Lindex,:) = [];                                       %Delete
        everything above inductance
38  Llabels1(1:Rindex-Lindex,:) = [];                                %Delete
        all resistance
39  Llabels1(:,3:end) = [];                                          %Delete
        everything but two columns we want
40  Llabels1(1,:) = [];
41  sz3 = size(Llabels1);
42
43  for n1 = 1:sz3(1)                                                %In this
        for loop, we delete everything after comma in the label matrix column
        2
44      Llabels2{n1,1} = eraseBetween(Llabels1{n1,2},',',length(Llabels1{n1
            ,2}),'Boundaries','inclusive');
45  end
46  Llabels1clean = Llabels1;
47  Llabels1clean(:,2) = [];                                         %Isolate
        column 1 in big label matrix
48  LlabelsCleaned = cat(2,Llabels1clean,Llabels2);                  %
        Concatenate, such that we have Net name in column 1, node name in
        column 2
49
50  %NOW WE START CALCULATING
51  %First we want  to find where our relevant data is
52
53  Loop1index = zeros(length(Loop1),1);
                                                                     %DEFINE EMPTY MATRIX FOR
        THE DATA
54  for i = 1:length(Loop1)
                                                                     %This for-loop
        finds all the indeces, where you can find your variables in the large
        matrix
55  for n2 = 1:length(LlabelsCleaned)
56        if contains(LlabelsCleaned(n2,2), Loop1(i))
57          Loop1index(i) = n2;
58        end
59              if Loop1index(i) == 0
```

```
60              Loop1index(i) = length(Ldata)+1;
61          end
62
63  end
64  end
65  Ldata = cat(1,Ldata,zeros(1,length(Ldata)));
                                        %Adding empty row and column to Ldata
    (used when the node called is a sink)
66  Ldata = cat(2,Ldata,zeros(length(Ldata),1));
67
68  %We then extract all of the relevant data using our indeces, into the
69  %"relevant matrix"
70  Lrelevant = zeros(length(Loop1),length(Loop1));
71  lengthLrelevant = length(Lrelevant);
72
73  %We insert all of our relevant data into the matrix
74  for j = 1:length(Loop1)
75  for i1 = 1:length(Loop1)
76      Lrelevant(j,i1) = Ldata(Loop1index(j),Loop1index(i1));
77  end
78  end
79
80  LrelevantSimple = zeros(length(Loop1)/2,length(Loop1)/2);
                        %We want to simplify this relevant matrix, so we
    create a matrix half the size
81  lSimple = length(LrelevantSimple);
82
83  for l = 1:length(LrelevantSimple)
                                                %Inductance matrix is
    calculated
84  for k = 1:length(LrelevantSimple)
85      k1 = k*2-1;
86      l1 = l*2-1;
87      LrelevantSimple(kc,l) = Lrelevant(k1,l1)+Lrelevant(k1+1,l1+1)-
            Lrelevant(k1+1,l1)-Lrelevant(k1,l1+1);
88  end
89  end
90   % THEN WE FIND THE INDUCTANCE BY SUMMING THE MATRIX
91   Lloop1 = sum(LrelevantSimple,'all')
92
93  end
```

Appendix F

DSP C Code

In this appendix, the code used to perform the required tests is shown.

F.1 Initialisation

```
#include "DSP28x_Project.h"
void main(void)
{
    EALLOW;
      GpioCtrlRegs.GPAMUX1.bit.GPIO0 = 0;
      GpioCtrlRegs.GPADIR.bit.GPIO0 = 1;
      GpioCtrlRegs.GPAMUX2.bit.GPIO16 = 0;
      GpioCtrlRegs.GPADIR.bit.GPIO16 = 1;
      GpioCtrlRegs.GPBPUD.bit.GPIO32 = 0; //Disable pull-up resistor
      GpioCtrlRegs.GPBQSEL1.bit.GPIO32 = 0; //Select amount of samples for qualifying, 0
     = 1 sample.
      GpioCtrlRegs.GPBMUX1.bit.GPIO32 = 0;     // Select GPIO from MUX
      GpioCtrlRegs.GPBDIR.bit.GPIO32 = 0;      // Select digital input
      EDIS;

InitSysCtrl();

Uint16 pinValue;
float t1on = 5000;               //write time in nanoseconds for pulse 1
float t3on = t1on;                //write time in nanoseconds for pulse 2
float deadtime = 350;             //write time in nanoseconds for deadtime (If this time
     is to be used, change to while loop
int t1 = t1on/80+34/80;
int dead = deadtime/80+34/80;
int t3 = t3on/80+34/80;
int i;
int j;
int k;
int de;
int ded;
```

F.2 Double Pulse Test Code

```
1
2
3  while(0)                  //DPT test (set to 1 if want to do DPT, otherwise 0
4      {
5          pinValue = GpioDataRegs.GPBDAT.bit.GPIO32;
6          if(!pinValue)
7          {
8
9          //ALL PINS OFF INITIALLY
10         GpioDataRegs.GPADAT.bit.GPIO0 = 0;
11         i = 1;
12         j = 1;
13         k = 1;
14         DELAY_US(100);
15
16         //FIRST PULSE
17         GpioDataRegs.GPADAT.bit.GPIO0 = 1;
18         while(i<t1)          //delay is generated here
19         {
20             i++;
21         }
22          //    j = 1;
23         //HS Pulse OFF
24         GpioDataRegs.GPADAT.bit.GPIO0 = 0;
25
26
27 //         while(j<dead)          //to adjust deadtime, uncomment this, and comment the k
28 //         {
29 //             j++;
30 //         }
31         k = 1;           // delay (lowest clock cycle delay i could find)
32
33         //SECOND PULSE
34         GpioDataRegs.GPADAT.bit.GPIO0 = 1;
35         while(k<t3)
36         {
37             k++;
38         }
39       //  j = 1;
40         //HS Pulse OFF
41         GpioDataRegs.GPADAT.bit.GPIO0 = 0;
42         DELAY_US(1000000);
43         }
44         pinValue = 0;
45     }
```

F.3 Multiple Pulse Test Code

```
//multiple pulse test settings
int n = 15;                 //number of pulses
int d;                     //dummy deadtime variable
float pulselength = 500;
int pulse = pulselength/80+34/80;


while(1)                          //Set to 1 if you want to do a multiple pulse test
    {
    pinValue = GpioDataRegs.GPBDAT.bit.GPIO32;
            if(!pinValue)
            {
            GpioDataRegs.GPADAT.bit.GPIO0 = 0;
            GpioDataRegs.GPADAT.bit.GPIO16 = 0;

                for (i = 1; i <= n; ++i)
                {
                    k = 1;
                    d = 1;
                    de = 1;
                    ded = 1;
                    GpioDataRegs.GPADAT.bit.GPIO16 = 0;
                                while(de<dead)
                                {
                                    de++;
                                }
                    GpioDataRegs.GPADAT.bit.GPIO0 = 1;

                        while(k<pulse)
                            {
                                k++;
                            }


                    GpioDataRegs.GPADAT.bit.GPIO0 = 0;
                                while(ded<dead)
                                {
                                    ded++;
                                }
                    GpioDataRegs.GPADAT.bit.GPIO16 = 1;
                         while(d<pulse)
                             {
                                 d++;
                             }
                }
                GpioDataRegs.GPADAT.bit.GPIO16 = 0;
                GpioDataRegs.GPADAT.bit.GPIO0 = 0;
                DELAY_US(1000000);
            }
    }
}
```

Appendix G

Altium Schematics

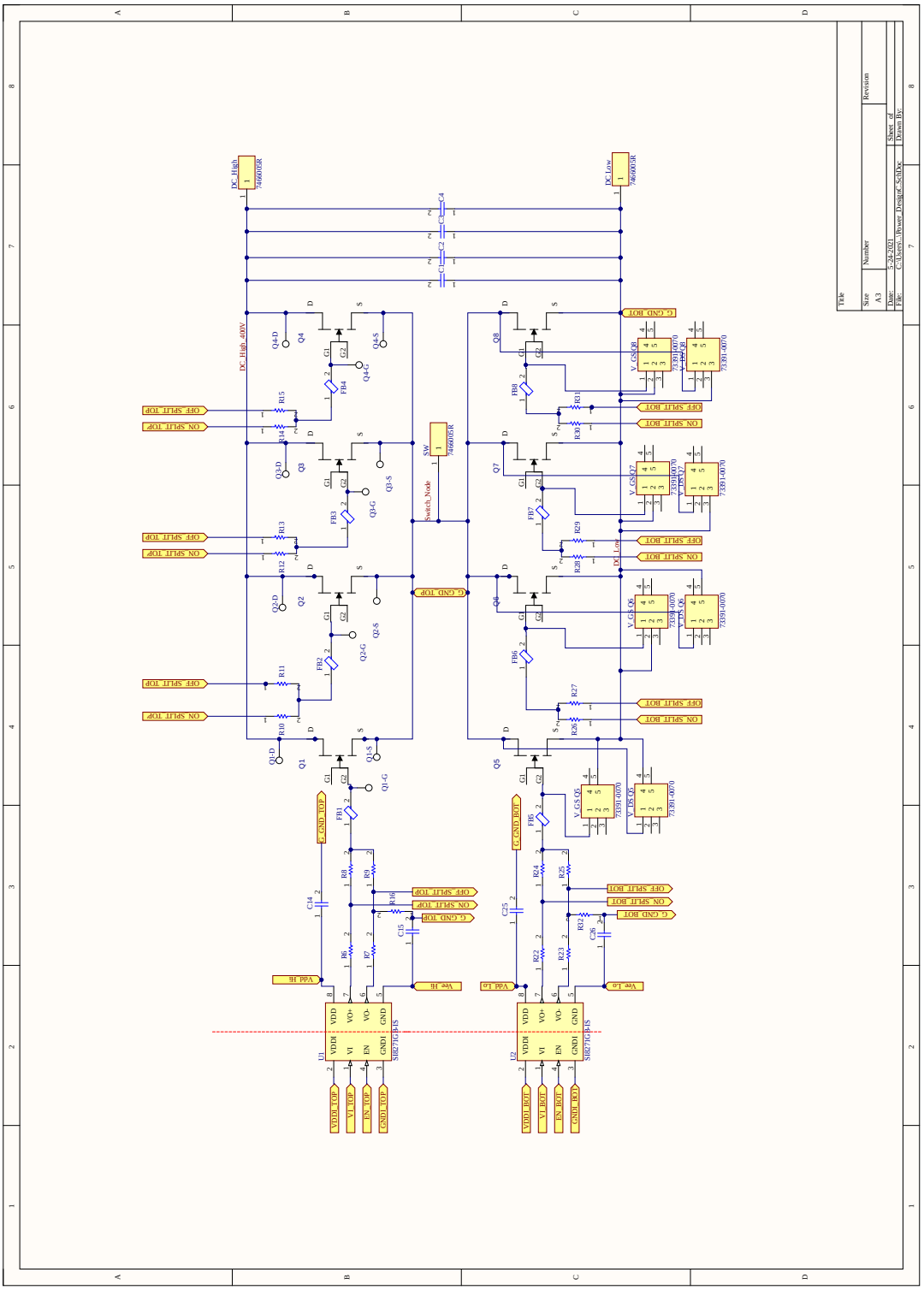


Figure G.1: Altium schematic for the power side.

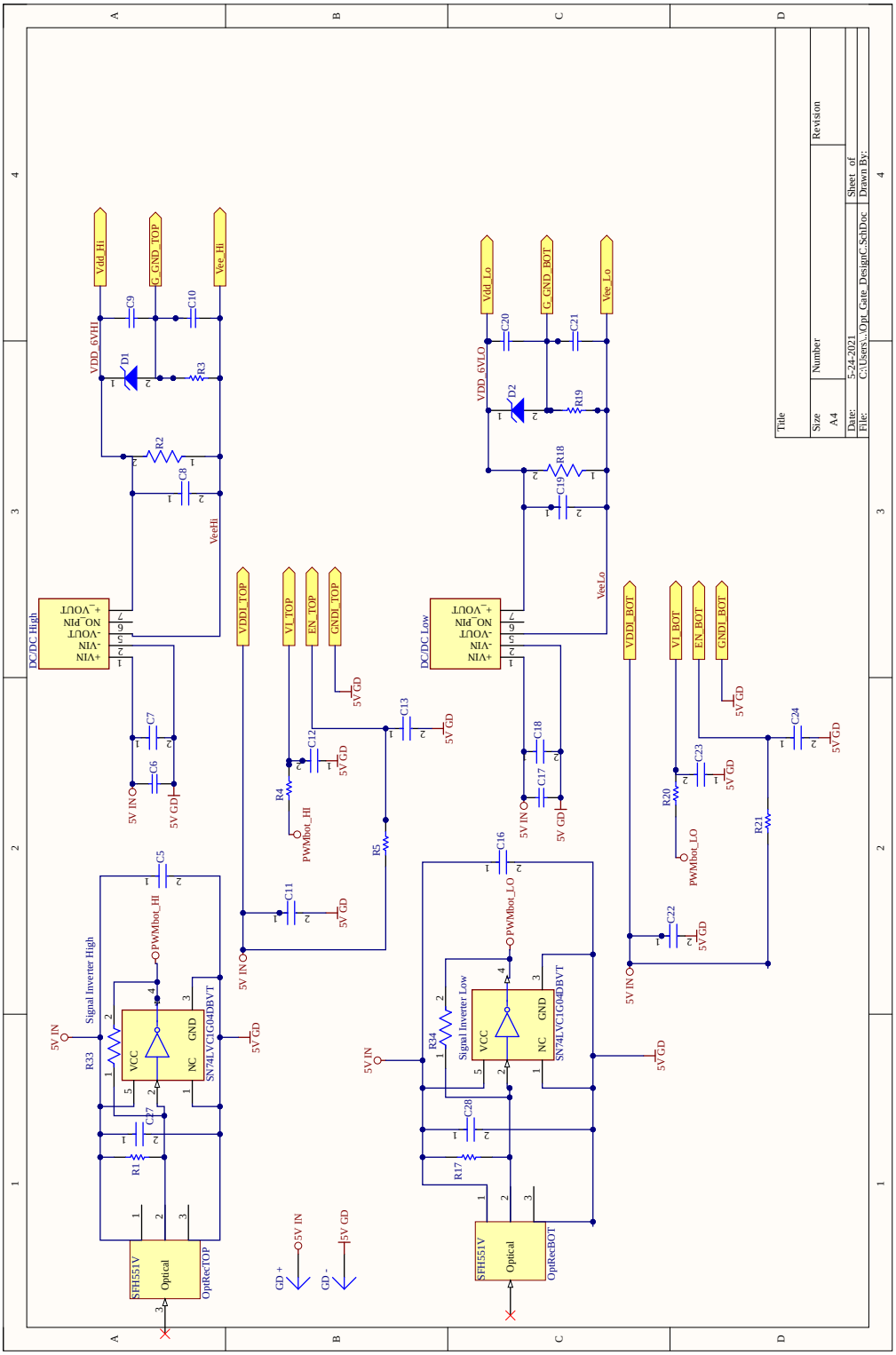


Figure G.2: Altium schematic for the optical to gate driver input side.

Appendix H

Quasi-Common Inductance Source Inductance

Presented in Section 2.2, a model of the parasitics of a HB with four devices in total was shown. The parasitics are defined, such that their influence on system stability can be quantified. Specifically, the quasi-common inductance was presented, and its importance was recognised. A schematic representation of it for two parallel devices can be seen in Figure H.1.

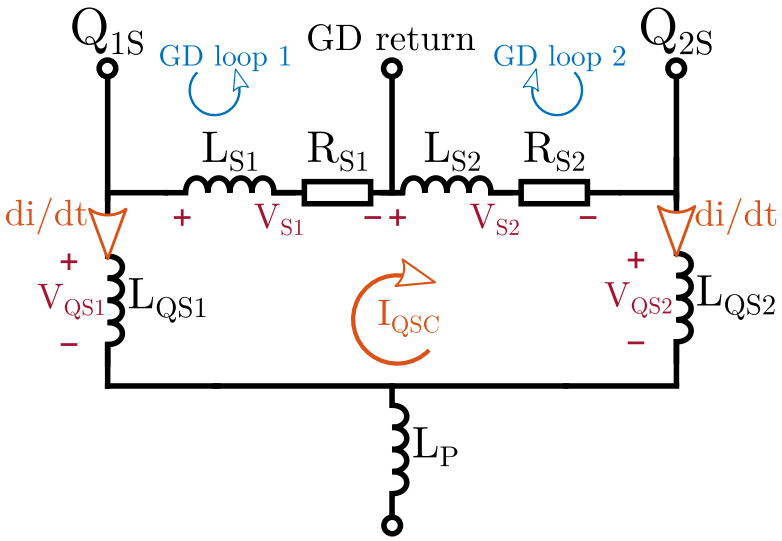


Figure H.1: Simplified circuit schematic of quasi common loop for two devices. The common source inductance between power and GD loops has been removed for simplicity.

In Figure H.1, the effect of the quasi-common inductance is demonstrated. An imbalance in either the quasi-common inductances L_{QSx}, an imbalance in the di/dt seen over these inductances, or a combination of these will cause a current I_{QSC} to circulate over the source return impedance. The voltages over the quasi-common inductances can be found as seen in Figure (H.1).

$$V_{QSx} = \frac{di_x}{dt} L_{QSx} \tag{H.1}$$

The resulting circulating current is seen in (H.2).

$$I_{QSC} = \frac{V_{QS1} - V_{QS2}}{R_{S1} + R_{S2}} + \frac{1}{L_{S1} + L_{S2}} \int V_{QS1} - V_{QS2} dt \tag{H.2}$$

This results in voltage drops in each of the GD loops as seen in (H.1).

$$V_{Sx} = I_{QSC} \cdot R_{Sx} + L_{Sx} \frac{di_{QSC}}{dt} \tag{H.3}$$

Looking at Figure H.1, it can be seen that the voltage drops V_{S1} and V_{S2} affect their respective GD loops in opposite directions, i.e. one GD loop will have its voltage increased, the other will have its voltage reduced. This may cause an imbalance in the current carrying capability of the devices, as their gate voltages will differ. This may in turn cause an imbalance in the di/dt of the devices, causing further imbalance. A feedback loop may occur as a result of this.