Design of MMC Sub-Module for High-Power Testing Applications

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Master's Thesis

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Abstract:

In recent years, the need for high-power testing such as grid emulation systems has become increasingly popular. Following former investigations by the authors in [1], a Modular Multilevel Converter (MMC) based grid emulator is of interest. This thesis considers the development of an MMC Submodule (SM) for high-power test applications. In the pursuit of finding a suitable design, a development methodology is presented considering different development phases, introducing Design Failure Mode and Effect Analysis (DFMEA) as part of the procedure. During the project, various subsystems of the SM are determined, mainly focusing on two streams, namely, power hardware and control hardware. In the design phase, a clear test methodology is developed to test the SM, including both commissioning and design validation tests. The test shows results within the requirements of the considered MMC for high-power testing. Finally, the design is validated based on the experimental results and a Technology Readiness Level (TRL) analysis. It can be concluded that the MMC SM shows promising properties for future engaging in a full MMC, with only a few failure modes which are detected and mitigated.

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Summary

In recent years, the grid code compliance testing of high-power electronic-based sources has been increasingly demanded due to the increased penetration of renewables which are mostly coupled to the grid using power electronic converters.

Following this trend, high-power testing equipment has been developed to ensure that standards and grid codes can be verified for new developments. Today, different types of test equipment exist for testing various functionalities and requirements; however, using converters to test high-power sources is one solution that is getting increasing attention due to its flexibility and controllability. The use of converters as testing equipment is most often referred to as grid emulators. Following this approach, studies to find the most suitable converter topology have been conducted by the authors in [1], [2], finding Modular Multilevel Converter (MMC) a suitable topology due to its scalability and versatility towards voltage level, power and functionality. From these studies, requirements for the Sub-module (SM) level are derived.

In this thesis, the focus is on developing a SM for an MMC used in a high-power testing application such as grid emulators. A design methodology is made to have a clear development strategy throughout the thesis as an initial step. A Design Failure Mode and Effect Analysis (DFMEA)-based approach is chosen to avoid failure modes before the prototype stage by mitigating these in the design phase and planning detection strategies such as commissioning tests. The overall design is made in two parallel design streams: a power hardware design and a control hardware design. The power hardware considers the choice of the power module, capacitors and busbar design, while the control hardware covers the choice of gate driver circuitry and design of control Printed Circuit Board (PCB), including various components for data acquisition, hardware protection and choice of controller. Finally, an assembly plan and test campaign are defined for the SM. The test campaign includes various commissioning test conducted iteratively with assembly to detect failure modes, and prototype test derived to ensure compliance with the design requirements for the full MMC.

The test of the SM shows results verifying operation within the requirements. When considering the commissioning test during the assembly, most results show positive performance; however, a failure mode considering the noise rejection of the data acquisition is detected, which is partly mitigated, allowing tests at a slightly lower operation voltage. Besides the electrical test showing a switching performance within voltage and current requirements, the thermal performance is validated at various operation points, and the worst-case cooling operation is detected.

Based on the test results, it can be concluded that the first iteration of an MMC SM prototype is achieved. Electrically and thermally, the SM operates within the stated requirements for a full MMC. The failure modes detected in the results are mitigated, and future improvements are given. Both qualitative and quantitative optimization levellers are detected for all design phases, which can be used for future optimizations. Finally, the design is validated considering Technology Readiness Level (TRL) which is estimated to a level 3, with the improvements found from the prototype. A new iteration of the design implementing the improvements is therefore concluded to be needed in a future full MMC setup.

Nomenclature

ΔT_{jc}	Junction-to-baseplate temperature	$[^{\circ}C]$
ΔT_{SF}	Temperature safety factor	$[^{\circ}C]$
ΔV_{SM}	Allowed SM voltage ripple	$[-]$
Δ	Difference	$[-]$
ϵ_r	Relative permittivity	$[-]$
$\frac{\Delta_i}{\Delta_t}$	Diode current rate of change	$[\frac{A}{s}]$
ϕ	Reference signal phase shift	$[^{\circ}]$
τ	Time constant	$[s]$
C_{ge}	IGBT gate-to-emitter capacitance	$[F]$
C_{ies}	IGBT input capacitance	$[F]$
C_{res}	IGBT transfer capacitance	$[F]$
C_{RR}	Reverse recovery capacitance	$[C]$
C_{SM}	Sub-module capacitor	$[F]$
e	Electron charge	$[C]$
E_{crit}	Si breakdown electric field	$[\frac{V}{m}]$
$E_{off_{IGBT}}$	IGBT turn-off energy	$[J]$
$E_{on_{IGBT}}$	IGBT turn-on energy	$[J]$
$E_{rec_{Diode}}$	Diode recovery energy	$[J]$
f_c	Carrier frequency	$[Hz]$
F_{flow}	Heat sink water flow	$[l/min]$
f_{LC}	Resonant frequency	$[Hz]$
f_{out}	Reference frequency range	$[Hz]$
f_s	Switching frequency	$[Hz]$
I_{arm}	Arm current	$[A]$
I_c	IGBT collector current	$[A]$
I_F	Diode forward current	$[A]$
I_{rr}	Peak reverse recovery current	$[A]$

L_Σ	Power module stray inductance	$[H]$
m_a	Amplitude index	$[-]$
N	Number of sub-modules	$[-]$
N_b	Base doping	$[cm^{-3}]$
P_{cond}	Conduction losses	$[W]$
p_{in}	Heat sink pressure input	$[PSI]$
p_{out}	Heat sink pressure output	$[PSI]$
P_{sw}	Switching losses	$[W]$
q	Elementary charge	$[C]$
Q_{rr}	Reverse recovery charge	$[C]$
R_{dc}	DC-link discharge resistor	$[-]$
R_m	Power module resistance	$[\Omega]$
$R_{th,ca}$	baseplate-to-ambient thermal resistance	$[\frac{^\circ C}{W}]$
$R_{th,jc}$	Junction-to-baseplate thermal resistance	$[\frac{^\circ C}{W}]$
R_{th}	Thermal resistance	$[\frac{^\circ C}{W}]$
SF	Power module nominal voltage safety factor	$[-]$
t	Thickness	$[m]$
T_{amb}	Ambient temperature	$[^\circ C]$
$T_{baseplate}$	Baseplate temperature	$[^\circ C]$
t_f	Fall time	$[s]$
T_j	IGBT junction temperature	$[^\circ C]$
t_{off}	IGBT OFF time	$[s]$
t_{on}	IGBT ON time	$[s]$
t_r	Rise time	$[s]$
T_s	Switching period	$[s]$
$V_{ce_{SAT}}$	IGBT collector-to-emitter saturation voltage	$[V]$
V_{ce}	IGBT collector-to-emitter voltage	$[V]$
V_{dc}	DC-link voltage	$[V]$
V_F	Diode forward voltage	$[V]$

V_{ge}	IGBT gate-to-emitter voltage	$[V]$
V_g	Gate voltage	$[V]$
V_{out}	Sub-module output voltage	$[V]$
V_{PM}	Power module nominal voltage	$[V]$
V_R	Diode reverse voltage	$[V]$
V_{SM}	Sub-module nominal voltage	$[V]$
V_{th}	IGBT threshold voltage	$[V]$
W_b	Metallurgical base width	$[m]$
$Z_{th,ca}$	baseplate-to-ambient thermal impedance	$[\frac{^\circ C}{W}]$
$Z_{th,jc}$	Junction-to-baseplate thermal impedance	$[\frac{^\circ C}{W}]$

Acronyms

ADC Analog-to-Digital Converter.

B2B Back-to-Back.

DAB Dual Active Bridge.

DFMEA Design Failure Mode and Effect Analysis.

DSP Digital Signal Processor.

DUT Device Under Test.

EMC Electromagnetic Compatibility.

EMI Electromagnetic Interference.

EMT Electromagnetic Transient.

FB Full-Bridge.

FEM Finite Element Method.

FPGA Field-Programmable Gate Array.

FSI Fast Serial Interface.

HB Half-Bridge.

HS Heat Sink.

IGBT Insulated Gate Bipolar Transistor.

LDO Low-DropOut.

MMC Modular Multilevel Converter.

PCB Printed Circuit Board.

PCC Point of Common Coupling.

PWM Pulse Width Modulation.

SELV Safety Extra Low Voltage.

SM Sub-module.

THD Total Harmonic Distortion.

TRL Technology Readiness Level.

TVS Transient Voltage Suppressor.

UML Unified Modeling Language.

Contents

Preface

This project has been made by two tenth semester students on the Power Electronics and Drives specialization enrolled at the Department of Energy Engineering, Aalborg University (AAU). The project has been created in the period from 1^{st} of February to 28^{th} of May 2021, with submission date on 28^{th} of May 2021 and evaluation on 10^{th} of June 2021.

This project was made in collaboration with R&D Test System A/S. We are grateful to R&D for their contributions to the mechanical design and test setup which would not have been possible otherwise.

Aalborg University, May 27, 2021

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Reading guide

The project describes the development and test of an MMC-based power electronic SM for high-power testing applications such as grid emulation systems.

The thesis consists of six chapters. The first chapter gives an introduction to the high-power testing application, converter topologies for high-power testing and why MMC is chosen for this application.

The second chapter describes the design and development methodology of the MMC SM, considering the requirements given in the introduction.

The third chapter focuses on developing a test campaign for the SM, considering the before mentioned requirements.

The fourth chapter presents the results and discussion, including the final validation of the developed design.

Finally, the fifth and sixth chapters present the conclusion and future work of the project, respectively.

The following software has been used in this thesis:

- **LaTeX** - Written work.
- **Mendeley** - Organisation of references.
- **yEd Graph Editor, Draw.io, Microsoft Visio** - Figures and drawings.
- **Matlab, Mathcad** - Calculations and plots.
- **Altium Designer** - PCB and electrical circuit design.
- **PLECS** - Simulations at electrical system level including control.
- **LTspice XVII** - Electromagnetic Transient (EMT) modelling and simulation of power devices and parasitics.
- **Ansys Q3D** - Evaluation and generation of busbar parasitics.
- **SolidWorks** - Mechanical drawings.
- **Code Composer Studio (Texas Instruments)** - DSP programming using C code.

Chapter 1

Introduction

In recent years, testing of high-power renewable energy sources has gained increasing attention by grid operators and manufacturers. Especially, high-power renewable sources such as wind turbines are rigorously tested to secure future power system stability and quality. These sources are often characterised by having at least one power electronic converter that transforms the power generator's output, typically an electrical machine, to the voltage and frequency level required by the grid connection, commonly 11, 33 and 66 kV along with 50 or 60 Hz. The grid connection has defined and regulated properties established in the so-called grid codes by the local grid operators, and these have to be strictly fulfilled. Any system that pursues a connection to the grid needs to demonstrate grid code compliance as these will be part of a network formed by multiple sources and loads. Grid code compliance can be verified by simulation models, but it is very often done by practical tests on site. These tests mainly focus on the power quality of the energy sources, making sure that their output voltage and frequency are within the allowed limits and their voltage harmonic content. Additionally, it is also of interest to evaluate the reaction of the power converter when unexpected variations occur at the Point of Common Coupling (PCC). These variations can be voltage unbalances or dips due to, for example, a nearby line short-circuit in the worst scenario. These can create a sudden increase in the current and the reactive power needed from the device under test. The power converter will, in this case, need to keep supporting the grid for some required time for then to be disconnected safely if the fault continues. Nowadays, there are various ways of performing these tests, such as passive components networks to create voltage dips, which were analysed in [1]. However, most of them only allow performing a single variable test, e.g. voltage variations or low-voltage ride-through. Developing a system that permits testing more than one feature is of interest as it saves costs and time.

1.1 Application

Once the need for a new generation of testing equipment for high-power energy sources is stated, the characteristics and right technology for implementing it are further analysed. The main idea driving this investigation is going from single-variable to multi-variable testing equipment. To achieve this, hardware that can reconfigure its output in real-time and varies more than one test parameter is required. Potential candidates to develop such a system are power electronic converters. Power electronic converters are widely present in modern power systems, both for generation and load, and are characterised by being fully controlled. Besides acting as an interface between the generator/load and the grid, which is their most typical application, power converters have also been proposed and studied in emulation systems. These include machine/generator emulators [3], load emulators as EVs [4], [5] and grid emulators [6], [7]. Their main usage is for testing purposes and, the typical arrangement is shown in Fig. 1.1.

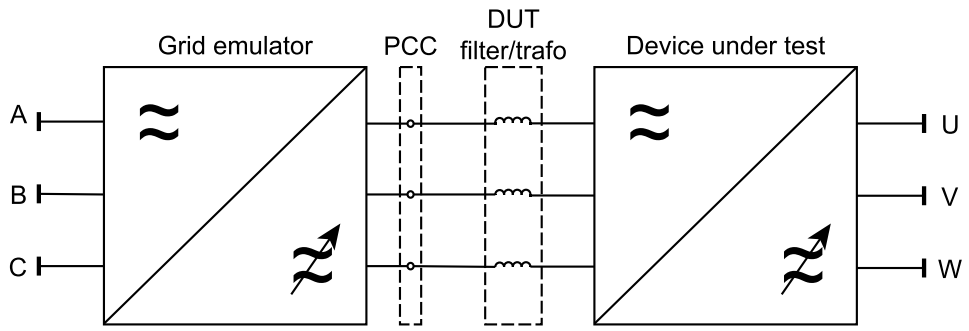


Figure 1.1: Test arrangement.

Based on the idea of using power converters for high-power sources testing, the grid emulator concept is expanded. A grid emulator is a system that can reproduce the grid properties, mainly voltage and frequency, on its output. This solution can mainly create two main advantages: decoupling from the grid and versatility as it allows high controllability.

The decoupling from the main grid, which is achieved by having a back- and front-end converter, creates a safe environment for testing. From the Device Under Test (DUT) side, it should operate as it was connected to the real grid, not affecting its operation. By doing this, the grid does not get influenced by the DUT reaction resulting from various test profiles, which cannot be achieved by traditional equipment based on passive components. At the same time, it enables the possibility of emulating a distorted grid by adding harmonic content on its output, seen only by the specific DUT and not affecting other systems connected to the main grid.

Furthermore, power converters can act as controlled voltage or current sources, allowing the development of a test bench to reproduce different test scenarios. Based on this, the grid voltage seen by the DUT can be easily changed to create different voltage patterns under fully controlled conditions, compared to existing equipment, which requires an exchange of passive components to create a specific voltage event. Additionally, frequency is left uncontrolled in existing solutions, meaning that both test equipment and DUT would need to be placed in an area having the rated frequency of interest, allowing normal grid frequency variations during the test. Here, the grid emulator based on power converters allows changing the output frequency through its control loop and, thereby, keeping stable test conditions. Thereby, an energy source tested in 50 Hz areas can be tested for areas where the rated frequency is 60 Hz, without erecting two prototypes. Therefore, the grid emulator would save the manufacturer a lot of time and cost of transport and mounting the DUT on the test site. However, the additional control that needs to be implemented can be complex. Therefore, this additional complexity will add cost to the solution depending on functionalities that need to be implemented. In general, the solution complexity is a disadvantage of using power electronics compared to today's simpler solutions.

Despite the disadvantages, there are numerous advantages of using power converters for grid compliance testing. One main keyword for this type of testing equipment is, therefore, its **versatility**, as just one controlled and configurable converter-based grid emulator can substitute and overcome the limitations of many different test equipment. As multiple test sites have

different nominal voltages and DUTs have both different nominal voltages and power ratings, it is essential to accommodate both. Therefore, a second keyword for this type of equipment is **scalability** in power and voltage. Finally, to simplify and improve the transport and the arrangement in the testing location, a compact and easily movable system needs to be developed. Therefore, a third keyword is being **transportable**. In the pursue of converter-based test equipment, these key features form qualitative requirements for the initial design.

1.2 Technology

Multiple types of converter topologies exist which could potentially be used as high-power testing equipment. Focusing on the keywords presented in the previous section, former investigations conducted by the authors in [1], [2] have found the Modular Multilevel Converter (MMC) topology to be most suitable for the application. The reason found in this investigations was, among others, that the MMC answers the keywords by being both scalable and versatile. The MMC is scalable in voltage as it is made of Sub-module (SM)s whereby increasing their number can increase the voltage. It also has the opportunity to be coupled in parallel at converter or SM level, as explained in [8], to increase current ratings. This configurability concludes its versatility to accommodate multiple test cases which need to be conducted. Besides the keywords, it also allows reduced, or even removed, filters and potentially transformers, as, e.g. Total Harmonic Distortion (THD) requirements can be accommodated by having more levels and voltage by increasing the number of SMs. For these reasons, the MMC is technically the most suitable for testing applications where different DUTs can have various ratings and requirements for a test at high power.
Some disadvantages of the MMC solution can be an additional cost and that these often become bulky solutions. Further, the MMC has not yet been used in the industry as a grid emulator for high-power testing, but mostly HVDC and STATCOM [9]–[12], hence the maturity of the solution for grid emulation is lower. In [1], [2], various MMC topologies such as indirect Back-to-Back MMC, Hexagon MMC and Matrix MMC have been studied. However, it was found that traditional indirect Back-to-Back (B2B) MMC was the most suitable topology, due to various parameters such as operation frequency range which is limited for direct MMCs. Adding to that, the maturity of this topology compared to the other MMC topologies is also higher with available commercial products on the market for other applications, as mentioned. The traditional indirect MMC, seen in Fig. 1.2, mainly consists of either Half-Bridge (HB) or Full-Bridge (FB) SMs. Here, it was found that FBs could have an advantage considering that over-voltage events can be created by using fewer SM as FBs allows amplitude modulation indexes above one. Therefore, making it a more feasible solution as the number of SMs can be reduced for a particular over-voltage event that needs to be emulated. Considering the disadvantages of the FB, it would need an additional power module in order to create the full bridge, thereby increasing the cost.

In general, for all MMCs, an inevitable component is the SM which needs to have a robust design that enables the top-level converter requirements for the MMC. The SMs are also the components that in the end make it possible to scale the MMC using more or less SMs. The converter, therefore, heavily depends on these basic building blocks to be designed properly. To achieve such a design, the SM needs to accommodate all MMC interfaces for both power and control. Seen from the power side, the SM's interface is its connection to other SMs used

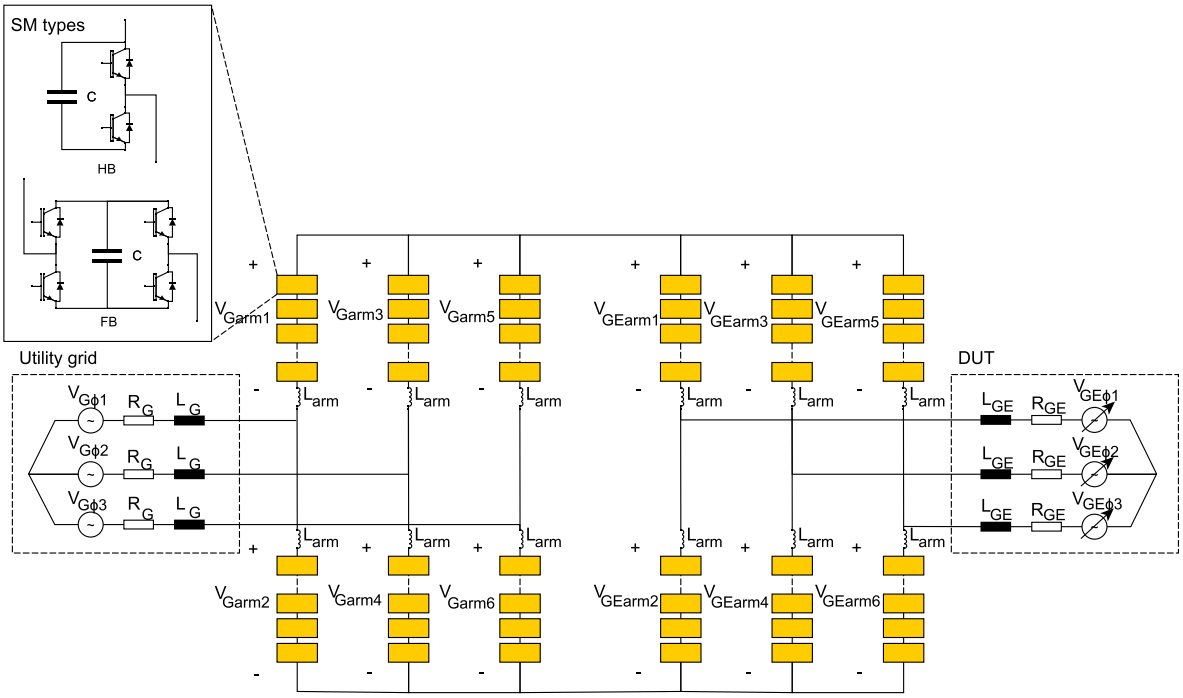


Figure 1.2: Traditional indirect back-to-back MMC.

to form the MMC arms. Here, it needs to enable the full load current ratings while inserting or bypassing its nominal voltage. Further, it is required that the SM is efficient, as large losses are released during switching of the SMs. These can be summarized in the following key topics:

- Enable required voltage, current, power and frequency.
- Allow both series and parallel connection.
- Provide a thermal interface for transfer of losses.
- Operate as an electrically isolated unit.

From the control side, the SMs need to efficiently communicate with each other and the main MMC controller while itself operating independently as a FB. The SM controller needs to allow the control strategy to be implemented. Depending on the control strategy [13], a distributed control could require extensive controller performance compared to central control. These can be summarized in the following key topics:

- Allow integration of different control strategies.
- Enable data transfer for control, protection and monitoring purposes.
- Ensure necessary control bandwidth.

Besides managing the interfaces, the internal architecture and components of the SM need to be identified. This identification includes finding all the necessary components and auxiliary systems within the requirements of the MMC. These parts need to be answered and developed

in order to build the foundation for a robust MMC design. The requirements of the SM are formed from the full MMC based on [1], [2], presenting the sizing equations for the full MMC considering high-power testing applications. In this project, specific grid emulator design requirements are used as the background for the project. These requirements are transformed into MMC SM requirements in Table 1.1 based on [1], [2].

Table 1.1: Transformation of top level converter requirements for high-power test converter to MMC SM requirements, using [1], [2].

Converter requirements	**Value**		**SM requirements**	**Value**
Nominal voltage	11/33/66 kV		SM topology	Full-bridge
Minimum apparent power	11 MVA		SM nominal voltage	1000 V
Voltage range	0.9-1.3 p.u.	Using $\Longrightarrow$ [1], [2]	Maximum SM voltage ripple allowed	$\pm$ 10%
Frequency range	45-65 Hz		MMC arm current	500 A
Maximum arm voltage ripple allowed	$\pm$ 10%		SM capacitance	4 mF
Minimum THD	5%		Reference frequency range	45-65 Hz
			Carrier frequency	500 Hz

These requirements are used as the foundation for the MMC SM design in the following chapter.

1.3 Problem formulation

The goal of the thesis is to design an MMC SM for high-power converter testing applications. The design includes all electrical and thermal component choices and sizing following the requirements presented in the former section for a 7 MVA grid emulator, derived using the method developed by the authors in [1], [2]. The main research question to be solved by this thesis is:

How an MMC SM is designed and validated for a high-power testing application?

1.3.1 Objectives

The following thesis objectives need to be fulfilled to answer the research question:

- To find a suitable development and test methodology for the MMC SM.
- To design and test an MMC SM evaluation prototype.
- To evaluate the developed SM concept considering improvements and Technology Readiness Level (TRL).

1.4 Thesis limitation

To limit the design to the MMC SM itself, some assumptions have been made. These include:

- The design to accommodate assemble of the the full MMC is not considered.
- No closed-loop control for SM tests.
- The SM is supplied from an external source and not through its DC-link capacitor bank.
- Top-level control and MMC operation are not validated in this thesis.
- No bypassing strategy is considered.

Chapter 2

Design

In this chapter, an overall SM design methodology is given. The specific designs are chosen and evaluated based on relevant calculations and simulation.

2.1 Sub-Module (SM) Architecture and Design Methodology

The architecture for the first design iteration includes components that are initially needed to form the FB SM. The interface features listed in Chapter 1 lead to the overall SM architecture presented in Fig. 2.1.

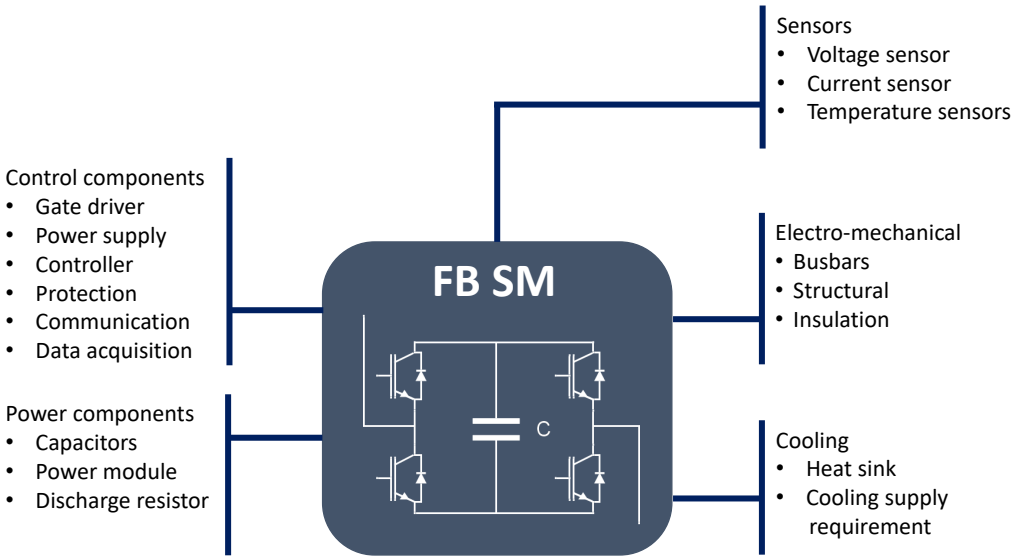


Figure 2.1: SM architecture and components.

The architecture, shown in Fig. 2.1, only includes the important topics to be designed and is extendable as some hardware require additional components, which is investigated during this chapter. These need to be derived and chosen following a structured design process, as some components lead to requirements for others. To achieve such a design process, a methodology needs to be developed. The design methodology followed in this thesis is specified in Fig. 2.2. As mentioned in Chapter 1, the initial input to this thesis is based on an MMC investigation for a specific grid emulator application, done in [1], [2]. The main SM consists of a full-bridge topology with a capacitor which size is based on the full MMC energy storage requirement, DC-link voltage, and its operation following the specific application. Besides the capacitor size, the SM voltage, maximum current, operational frequency, and switching frequency are found in Table 1.1. These input requirements form the basis of the design investigation and choices in this thesis. Therefore, the first step in the methodology is to find suitable power hardware components following the requirements. These are found based on available commercial components suitable for the application, including the switching devices

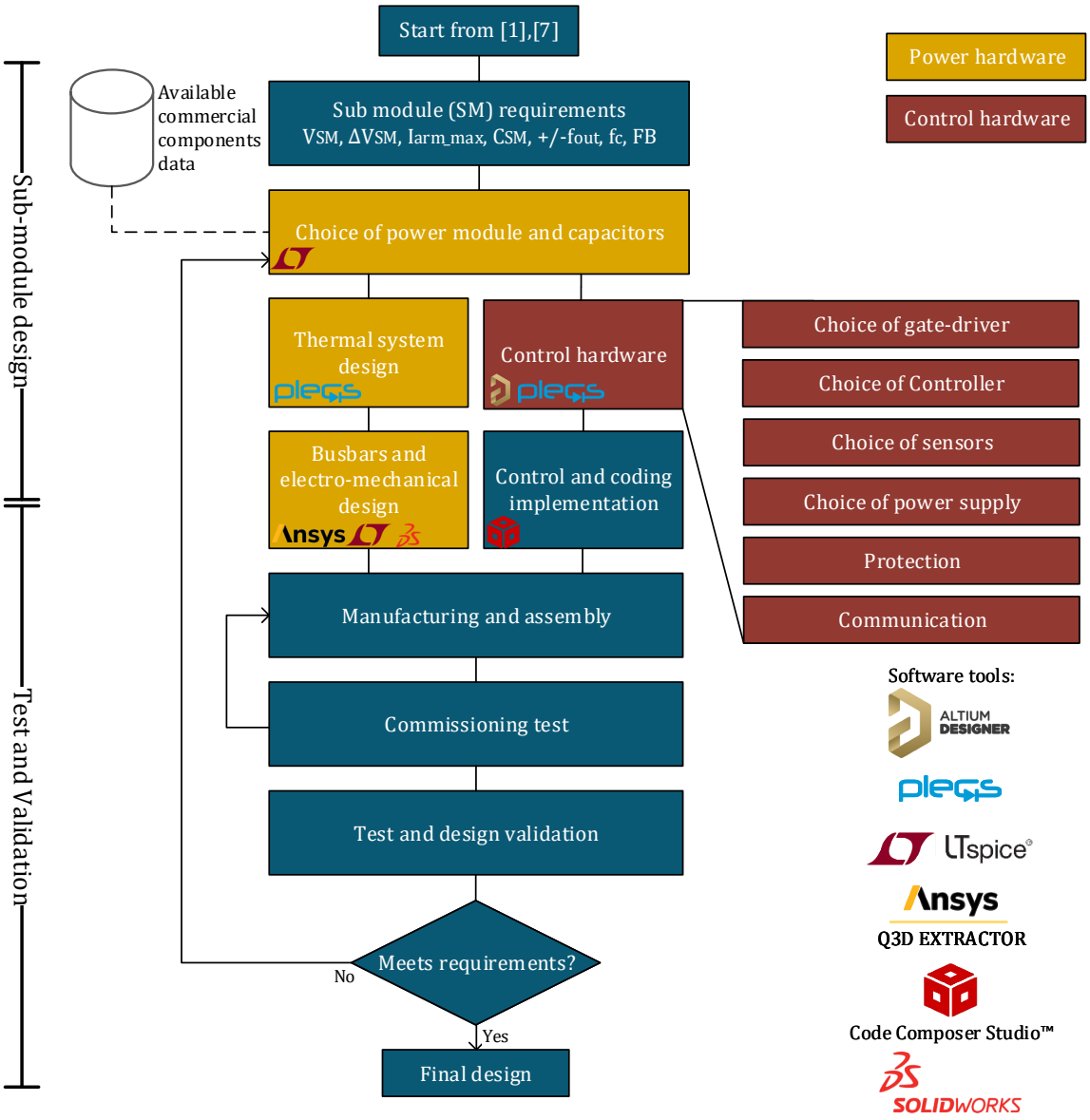


Figure 2.2: Methodology flowchart.

and passive components. After the choice of these components, the methodology splits into two paralleled tracks, mainly; power hardware considering the design and choices of the thermal and electro-mechanical parts, and control hardware considering protection investigation, gate drivers and control PCB. In these paralleled tracks, the hardware is found and verified using simulations whenever possible. The simulations should be used to verify the design before physical hardware manufacturing to minimize risk, cost and the number of design iterations needed. The different design software and simulation tools used in the individual steps are presented in Fig. 2.2. Next, the SM is manufactured and assembled. For the first couple of iterations, the SM design is expected to be a prototype which later should lead to a final commercial design. The SM parts will undergo sub-system tests in a commissioning test phase before the final assembly to ensure that the sub-system interfaces are working properly.

Therefore, the assembly and commissioning tests are done iteratively. Finally, the assembled SM is tested to verify the design against the required ratings and functionality considered as prototype test. If the test results do not show missing functionalities or failure modes, the requirements are met, and a final design is found. The choice of a final design will additionally be made depending on the reached Technology Readiness Level (TRL). This thesis considers the first iteration prototype design following the methodology presented to find the MMC FB SM.

2.2 Requirements

As an input to this thesis, some initial SM requirements are given. These are based on the evaluation of an indirect B2B MMC using FBs in a grid emulator application as described in [1], [2]. The input requirements are given in Table 1.1 and repeated below in Table 2.1.

Table 2.1: SM requirements from Table 1.1.

Requirement	Symbol	Value
SM topology	–	Full-bridge
SM nominal voltage	V_{SM}	1000 V
Maximum SM voltage ripple allowed	ΔV_{SM}	$\pm$ 10%
MMC arm current	I_{arm}	500 A
SM capacitance	C_{SM}	4 mF
Reference frequency range	f_{out}	45-65 Hz
Carrier frequency	f_c	500 Hz

The requirements are based on sizing the MMC for a apparent power of 7 MVA at 11 kV, 33kV or 66kV, considering the grid emulator requirements as presented in Chapter 1. From these requirements, the FB SM should be formed. The next step is to identify the potential risk considering the architecture presented in Fig. 2.1.

2.2.1 Design Failure Mode and Effect Analysis (DFMEA)

Before initializing the design, a Design Failure Mode and Effect Analysis (DFMEA) is conducted to cover the components presented in Fig. 2.1. The reason for including a DFMEA is to avoid issues later in the prototype stage by highlighting important topics that need to be considered, which otherwise could lead to a higher cost. The DFMEA is shown in Table 2.2. From the DFMEA, some clear failure modes need to be mitigated. Generally, some mitigation techniques used are additional commissioning test and using commercially available components to achieve higher design confidence. The highlighted actions and the design controls already considered in the architecture stage are used further in the following design chapter.

Table 2.2: SM DFMEA.

Main item	Sub-item	Function	Potential Effect of Failure	Severity	Potential Cause of Failure	Occurrence	Current Design Controls	Detection	RPN	Recommended action
Power components	Power module	Creating switching events from $\pm$Vdc	System failure	8	Short-circuit	3	Over-current and voltage protection	2	48	Conduct electrical SM tests
	Capacitance	Maintaining constant DC-link voltage of the SM	System failure	8	Short-circuit or aging	3	Over-current and voltage protection	2	48	None
Electro-mechanical design	Busbars	Supplying current from capacitors to power modules	System failure	1	Over-temperature	1	None	10	10	None
	Insulation	Insulating busbars positive and negative polarity	System failure	8	High dv/dt	8	Choose material with high dielectric strength	9	576	Electrical isolation test
Cooling	Heat sink	Heat transfer from power modules to cooling system	SM overheating	7	Over current/cooling water temperature	4	Current and temperature surveillance	2	56	Conduct thermal SM tests
Control board	Gate-driver	Supplying gate voltage and current to PM gate and isolating main controls, upper and lower IGBT from each other	No control of SM	8	Wrong design with too low current capability	7	None	10	560	Use existing commercial available technologies
	Power supply	Supplying rated power to different sensor, controllers, gate drivers, etc.	No/little power	8	Wrong choice of power capability	1	Tested during commissioning	2	16	None
	Controller	Enable controllability and data acquisition of SM components	No controllability	7	Glitch or other noise	5	Tested during commissioning	2	70	None
	Protection	Ensuring self-protection of SM	System failure	9	Over-voltage, current and temperature	7	Implementing protection in controllers	9	567	Implementation of hardware-based protection
	Communication	Enable efficient control between main controller and SMs	Main controls loss	5	Noise or wrong communication strategy for MMC	9	Commissioning testing	5	225	Investigate best strategy for MMC based SM
Sensors	Voltage sensor	Translate DC-link voltage to readable signal in controller	No voltage protection	9	Defect sensor	3	Commissioning testing	5	315	Use commercial available sensor
	Current sensor	Translate SM current to readable signal in controller	No current protection	9	Defect sensor	3	Commissioning testing	5	315	Use commercial available sensor
	Temperature sensor	Read temperature sensor of PM and translate to readable signal in controller	No temperature protection	7	Defect sensor	3	Commissioning testing	5	105	Use commercial available sensor

2.3 Power Hardware

This section includes the investigation of power hardware, including power modules, capacitors, thermal system, and busbar design, following the methodology presented.

2.3.1 Choice and Design of Power Hardware Components

To initiate the SM design, a power module needs to be chosen. Here semiconductor type, device type and package topology are categorical variables that can be chosen. The semiconductor type includes various semiconductor materials such as Si, SiC or GaN. In this thesis, available commercial components for high-power are needed, and at the current time, the Si is still the widest available semiconductor for high power, which is therefore used in this thesis. Considering the device types within Si, the IGBT is the widest used due to its high blocking capabilities [14]. However, special devices such as the IGCT are used in some applications, but these need to be customised and require special driver circuits that are not widely available. From the choice of a Si IGBT, the final decision of package topology needs to be made. Here, a larger variety of solutions are available on the market. These include single-switch, half-bridge and even full-bridges. Before making this choice, the ratings of the power module should be found. From the requirements presented in Table 2.1, the SM current and voltage are given. For the voltage, some margin should be given to avoid over-voltage. The minimum voltage rating of the power module should be found as (2.1).

$$V_{PM} = \frac{V_{SM}(1 + \Delta V_{SM})}{SF} = \frac{V_{SM}(1 + 0.1)}{0.8} = 1375kV(DC) \tag{2.1}$$

where SF is a chosen safety factor of the power module (typically 20%) and ΔV_{SM} the allowed ripple. The traditionally available power module voltage ratings around this range are 1.2, 1.7 and 3.3 kV. As 1.2 and 3.3 kV are too low and high, respectively, 1.7 kV is the closest match. This voltage rating vote out some package types for higher voltage, such as the press-pack IGBTs which, in comparison to other solutions, are known for their better short-circuit failure mode characteristics [15] which could be beneficial for a MMC. However, due to its compact design and ability to reach voltages higher than 2.5 kV, the price is also heavily increased. Some solutions with different package solutions within the lower 1.7 kV voltage range are presented in Table 2.3.

Table 2.3: Power module candidates.

Topology	Product number	Nominal current	Housing type	Cost[1]
Single switch	FF500R17KE4	500 A (100%)	62 mm	216 €
Half-bridge	FF600R17ME4P	600 A (83%)	EconoDUAL™3	280 €
Half-bridge	FF650R17IE4P	650 A (77%)	PrimePACK™2	420 €
Half-bridge	FF1000R17IE4	1000 A (50%)	PrimePACK™3	623 €

[1] Price for one single module not wholesale with lead-time of up to 18 weeks [16]

It can be seen in Table 2.3 that various solutions exist within the 1.7 kV range. In this case, Infineon products have been chosen. However, similar products are available from other suppliers like the PrimePACK, which is standard in size. The loading of the power module depending on the SM nominal ratings can also be seen in the table. The single switch is maximum loaded at rated current, while the others are partially loaded. Further, two modules

need to be used to form one HB therefore doubling the price compared to integrated HB modules. The HB solutions are partially loaded, which can be an advantage in case of over-current; however, an additional cost is added. When comparing the module prices, going from FF600R17ME4P to FF1000R17IE4 results in twice the price; however, the current is not fully doubled. For higher ratings of the MMC module than the 7 MVA, the FF1000R17IE4 could be more feasible as it results in a more compact solution than two FF600R17ME4P. Concerning this, another option to create one more degree of freedom, to find an optimised solution, could be to parallel IGBTs. This solution is an option; however, some problems when considering IGBTs is their collector-emitter voltage in the saturated region and parasitic inductance between them. Considering the collector-emitter voltage in the saturated region, IGBTs have a positive temperature dependence at higher currents which is a positive feature considering paralleling. However, at lower currents, which also can cover the nominal range, the dependence can be negative, meaning that it will be unevenly distributed. The reason for this is that the temperature has a positive effect on high on-state voltage drops at high current densities; however, at low current densities, the temperature has a negative effect on the on-state voltage drop, also known as the knee point [17]. This will create uneven current distributions at the lower currents. For the parasitic inductance, the parallel connections to the IGBT's collector and emitter need to be close to zero, which otherwise can create oscillations, higher voltage overshoots, and importantly imbalanced currents. The paralleling of IGBTs is often done on package level; however, for terminal levels, it should be done with caution. For the first iteration design, an available power module with similar ratings to FF1000R17IE4 is chosen. The reason being that the initial prototype design should be used to verify the design. When a single converter block size is settled in a later design iteration, the power module size can be adjusted depending on the final ratings found from this iterative design. Further, due to the delivery time, shown in Table 2.3, an available power module needs to be used. The power module used is from Danfoss [18] with the ratings seen in Table 2.4.

Table 2.4: Power module choice - first iteration.

Type	Product number	Nominal current	Housing type
Half bridge	DP1000B1700TU103727	1000 A (50%)	PrimePACK™3

To finalise the SM design, the DC-link capacitor bank should be formed from available capacitors. The MMC SM, given in Table 2.1, requires 4 mF with a nominal voltage of 1000 V DC, including 10% ripple. Further, the SM should be able to utilise the full-arm current peak and, therefore, similar for the capacitor bank. Here, the capacitance and current requirements can be reached by paralleling multiple capacitors. Some possibilities are given in Table 2.5 which are available from the manufacturer Electronicon's E50 1.1kV series [19]. From Table 2.5, various capacitance values are presented along with their corresponding current and ESR values. The specific capacitance values are chosen such that their integer multiple is at least 4 mF without too high excessive capacitance. The number of capacitors needed is also shown in the table, followed by the total capacitance. What is important to notice is that a higher capacitance value per capacitor does not lead to a proportional rise in current capability; hence, choosing a large capacitor of 2.1 mF will only lead to a capacitor bank with a current capability of 240 A. Therefore, the capacitor size should be chosen from a bank size that leads to the requirement of 500 A. From Table 2.5, the solution of $580\mu F$ or below. Further, as the ESR is inversely proportional to the number of capacitors, choosing a higher number will

Table 2.5: Capacitor choice - first iteration.

Capacitance [mF]	Maximum current [A]	ESR[mΩ]	Number to form >4 mF	Total capacitance [mF]	Total current [A]	Total ESR[mΩ]	Total cost[1] [€]
250	70	0.73	16	4.00	1120	0.046	1180
375	90	0.67	11	4.13	990	0.061	714
400	59	2.1	10	4.00	590	0.210	946
415	65	0.79	10	4.15	650	0.079	878
450	80	0.86	9	4.05	720	0.096	1046
580	80	0.88	7	4.06	560	0.126	1026
830	90	0.68	5	4.15	450	0.136	-
1000	65	0.89	4	4.00	260	0.223	634
1410	90	0.87	3	4.23	270	0.290	554
2115	120	0.82	2	4.23	240	0.410	531

[1] Total price based on purchase of single units not wholesale considered

lead to a lower ESR as larger capacitors have similar ESR as smaller values. The smaller ESR value leads to increased efficiency of the SM as an additional benefit. Finally, the total cost of the capacitors is lowest from 375 to 415μF which therefore are concluded to be the best solution. From available capacitor sizes, the first iteration prototype is made from 400 μF [20] capacitors, even though these have slightly higher total ESR. The characteristics of the chosen capacitor can be seen in Table 2.6.

Table 2.6: Capacitor parameters [20].

Parameter	Value
Rated DC voltage V_{dc}	1100 V
Maximum ripple voltage V_r	250 V
Non-recurrent surge voltage u_s	1650 V
Capacitor ESR ESR	250 $\mu\Omega$
Self inductance L_e	10nH

From the table, it can be seen that the capacitor has the lowest voltage rating in the system. It is also the maximum allowed DC-link voltage requirement, which is 1350 V considering maximum nominal voltage and allowed ripple. As only a non-recurrent surge voltage is given, it also forms the requirement for the maximum allowed recurrent surge voltage

Electromagnetic Transient (EMT) Model

To verify the electrical SM design, the chosen power components are modelled to form an Electromagnetic Transient (EMT) model of the power module as shown in Fig. 2.4. This model is used to verify the chosen power module and, later, is used in a complete EMT model, including the parasitics from the SM design such as DC-link busbars. The chosen power module does not include a SPICE model from the manufacturer. Therefore, as one of the thesis's aims is to verify the design using a model-based approach before a prototype when possible, the next step is to find a suitable model. The model is made from the power module datasheet [18], and it should, therefore, be noticed that making an exact EMT model can not be possible without a test, as the datasheet is not expected to include important parameters and precise characteristics. However, a model which is precise enough to be used for evaluating the electrical characteristics of the SM is of interest. For the modelling in this

thesis, the used datasheet values and characteristic plots are used. The datasheet values used are given in Table 2.7.

Table 2.7: Power module parameters [18].

Parameter	Conditions	Value
Collector-to-emitter voltage V_{ce}	$V_{ge} \leq 0$	1700 V
Collector current I_c	-	1000 A
Threshold voltage V_{th}	-	5.8 V
Peak Reverse Recovery current I_{rr}	$V_R = 900$ $I_F = 1000A$ $\Delta i/\Delta t = 10500A/\mu s$ $T_j = 150°C$	$1050A$
Module Resistance R_m	-	$250\mu\Omega$
Module stray inductance L_σ	-	$10nH$

The model is developed in LTspice where traditional power devices models are included and can be modified to a specific device. First, the IGBT of the power module is modelled, which is achieved by using its datasheet values and calculating suitable parameters as seen in Table 2.8.

Table 2.8: IGBT model parameters - LTspice NIGBT model.

Parameter	Formula	Value
Device area	$Area = \frac{I_{peak}}{J_{th}}$	5 cm^2
Metallurgical base width	$W_b = \frac{2V_{ce}}{E_{crit}}$	$13 \times 10^{-6} m$
Base doping	$N_b = \frac{E_{crit}^2 e}{2V_{ce_{SAT}} q}$	$1.48 \times 10^{17} cm^{-3}$
Gate-Emitter capacitance per unit area	$\frac{C_{ge}}{Area} = \frac{C_{ies} - C_{res}}{Area}$	$8.7nF/cm^2$
Gate-Collector oxide capacitance per unit area	$\frac{C_{gc}}{Area} = \frac{C_{res}}{Area}$	$0.289nF/cm^2$

The values in the table form the basis of the IGBT implementation. However, to form a more precise model, the parameters are subject to adjustments. Besides the parameters in the table, the trans-conductance is used as a degree of freedom. To find the first model, a DC-sweep test at different gate-emitter voltages is proposed in the datasheet to compare. The comparison is seen in Fig. 2.3a. As it can be seen from the DC-sweep, the models and datasheet have some deviations; however, having a relatively close fit, where the largest deviations are seen in the desaturation region. The trans-conductance is chosen to be 95. Following the DC-sweep of the IGBT, the diode is similarly modelled as seen in Fig. 2.3b. Compared to the IGBT model, the diode only requires forward voltage drop and on-state resistance, which can easily be found from the datasheet plot of forward voltage and current. The model and datasheet have a close fit, and the model is, therefore, concluded suitably. The complete power module model so far is verified using a double pulse test simulation. In this model, both the IGBT and diode model without the before mentioned reverse recovery are included. One half-bridge of the FB SM is used for the simulation. Besides the model created, the power module parasitics are added. Here, two values are given in the datasheet for parasitic inductance and resistance, which are distributed as can be seen in Fig. 2.4 and are explained in [21]. The parasitic input and transfer capacitance, C_{ies} and C_{res}, affecting IGBT turn-on and turn-off are already included intrinsically in the model as these are used to calculate the initial parameters in Table 2.8.

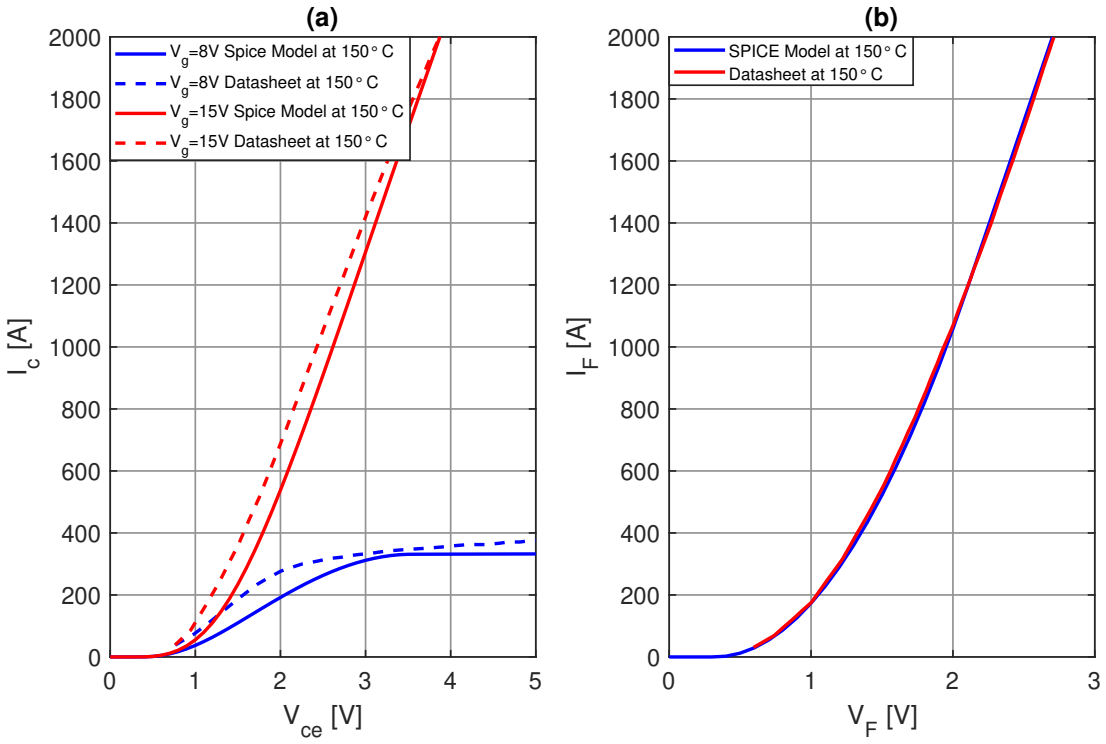


Figure 2.3: (a) DC sweep of IGBT at $V_g = 8V$ and $V_g = 15V$ using a external gate resistor of 1.1Ω, (b) DC sweep of diode.

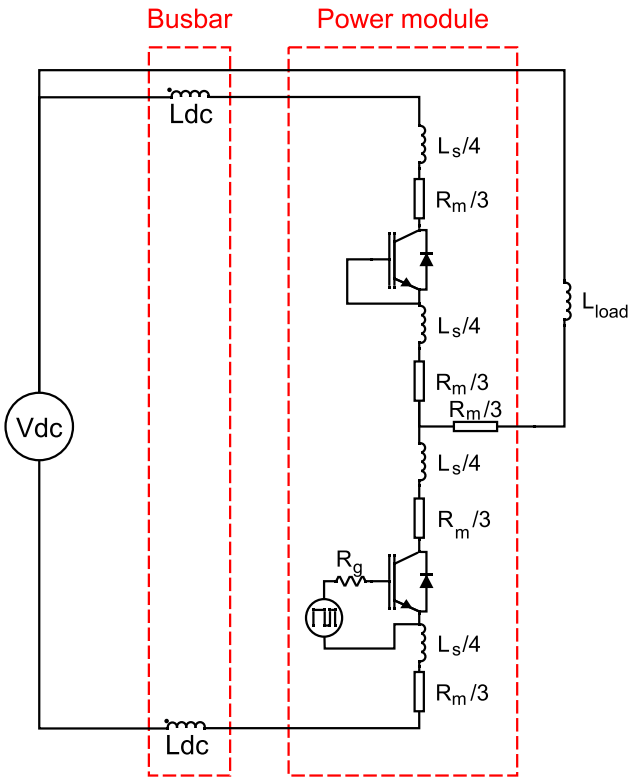


Figure 2.4: Double pulse test diagram including power module EMT model and DC-link parasitic inductance.

The final simulation is seen in Fig. 2.5 using a load inductance of 500 μH.

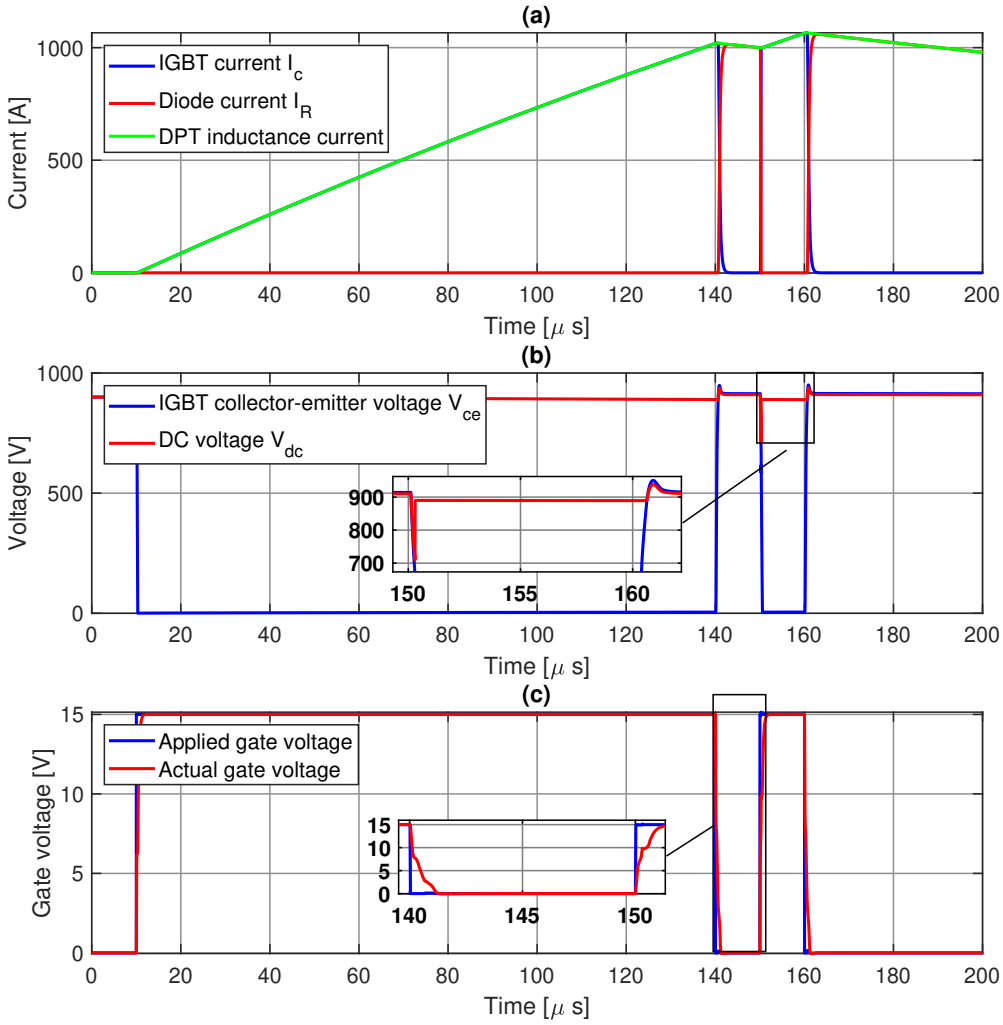


Figure 2.5: Double pulse test for 900 V source and $L_{load} = 500\mu H$.

From the simulation, the current is rising through the load inductance during turn-on of the IGBT. Similarly, it is falling during turn-off where the current is commutated to the diode. Until it reaches the rated current at 1000 A, it is limited by the on-time, load inductance, and applied voltage. The power module's parasitics effect is seen in the collector-emitter voltage, which shows a slight overshoot. The DC-link voltage also has some voltage over- and undershoot due to the DC-link stray inductance, where 10 nH are added as an initial guess, which will be studied in more detail later. From the gate voltage, the characteristic IGBT curves are shown, including the Miller plateau. The reason for this Miller effect is the gate capacitance which, first, charges to the gate voltage corresponding to current in the saturated region, where it stays until the collector-emitter voltage has dropped and it can charge to the full gate voltage. To finalise the model, a diode in high-power applications often includes PIN diode behaviour, resulting in a reverse recovery current during turn-off. This is also the case for the chosen power module diode, which behaviour is not available by default in the

SPICE model provided by LTspice. The reverse recovery can, however, be added following the approach presented in [22] and the additional SPICE model developed by the same author, adding the diode model developed so far to it. Here the dv/dt and the final current peak value in Table 2.7 are used to the correct fit of the reverse recovery together with the double pulse test measurement performed on the same power module in [23]. The final DPT is seen in Fig. 2.6. A reverse recovery of approximately 2000 A is seen at rated current. This value

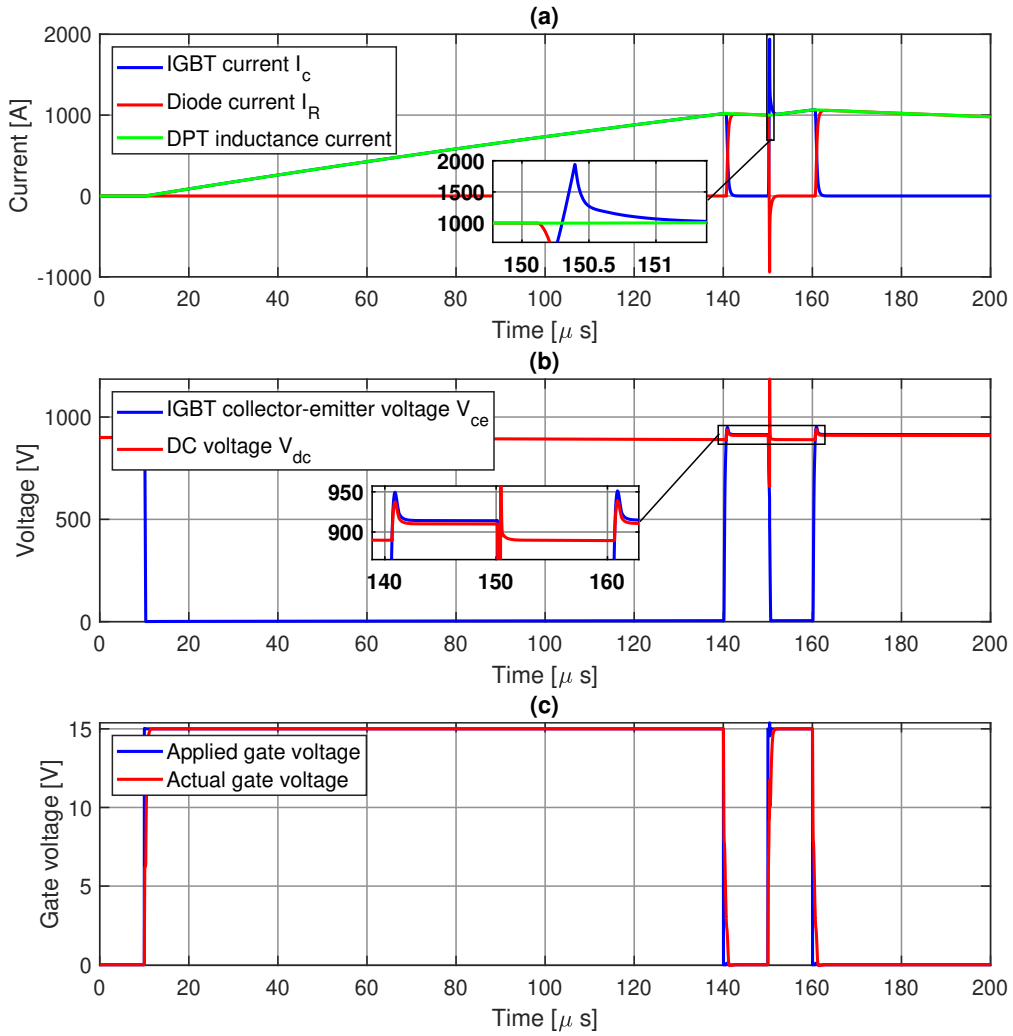


Figure 2.6: Double pulse test for 900V source and $L_{load} = 500\mu H$ - including reverse recover behaviour of the diode

matches well with the one given by the datasheet of a similar magnitude at 900 V applied DC voltage. Further, the $\Delta i/\Delta t$ is found to be $10161 A/\mu$s, which is close to the datasheet [18] value of $10550 A/\mu s$. This concludes the power module EMT model, which will be used as a basis for the final EMT model of the SM.

2.3.2 Thermal System Design

After the choice of power hardware, one of the paralleled workflows in the methodology is to design the power hardware assembly. One important component to be considered in this assembly is the cooling system, which for the SM includes a heat sink. The heat sink needs to be settled at the beginning of the process as it significantly influences the mechanical setup. The following requirements are given for the heat sink in Table 2.9.

Table 2.9: Heat sink requirements.

Requirement	Value
Expected power sink per SM	2 kW
Minimum footprint	89mmx250mm (PrimePACK™3)
Maximum power module temperature (junction)	150°C

The main requirement for the heat sink is to dissipate the expected power losses originated from switching and conduction losses which are transferred through the power module baseplate. In that process, the temperature requirement of the power module IGBT and diode junction can not reach higher temperatures than the maximum requirement. To find a suitable heat sink, an estimated power loss for the worst-case operation of the power module should be found. A good estimation is needed as a wrong estimation could lead to a heat sink that is unsuitable for sinking the power loss and could result in over-temperature, while a too-large heat sink could lead to unnecessary cost. The first estimation is calculated from the datasheet [18] plots of switching energy loss characteristic and output characteristic for conduction losses for both IGBT and diode at 500 A. These are found from (2.2) and (2.3) for switching and conductor losses, respectively.

$$P_{sw} = f_s(E_{on_{IGBT}} + E_{off_{IGBT}} + E_{rec_{Diode}}) = 500Hz(200mJ + 200mJ + 180mJ) = 290W \tag{2.2}$$

$$P_{cond} = \frac{t_{on}}{T_s}(V_{ce}I_c) + \frac{t_{off}}{T_s}(V_F I_F) = 0.5(1.8V \times 500A) + 0.5(1.5V \times 500A) = 825W \tag{2.3}$$

In (2.2) and (2.3), the operating point considered as worst-case is the maximum arm current with corresponding collector-emitter and forward voltage. These are found from the IGBT and diode characteristic curves in the power module datasheet [18] at a 50% duty cycle. Taking the worst-case at 50% duty cycle for the design, corresponding to the worst-case for converters outputting AC, leads to some safety margin for its operation. The total estimated loss is therefore slightly above the estimated input to the design of 1 kW (2 kW per SM) with a total calculated loss of 1115 W. To verify this calculation, a simulation is conducted for the losses. Two possible simulations can be conducted to pursue the estimated losses further. First, the electrical SPICE model of the power module produced in the former chapter can be used to find the losses from the turn-on and turn-off characteristics of voltage across and current through the power module. However, as the model is not verified from the real measured characteristics of the power module, the usage of the model could lead to some deviations. Secondly, the PLECS simulation software can extract the IGBT, and diode thermal and electrical characteristics directly from the datasheet [18] to form a thermal model. This model is therefore used to verify the estimated losses as it is considered more precise. A simulation, conducted at a constant 50% duty cycle, is seen in Fig. 2.7a and c, while a simulation using MMC-related duty cycle is also shown in Fig 2.7b and d using Pulse Width Modulation (PWM) signals from simple MMC open-loop control references [1].

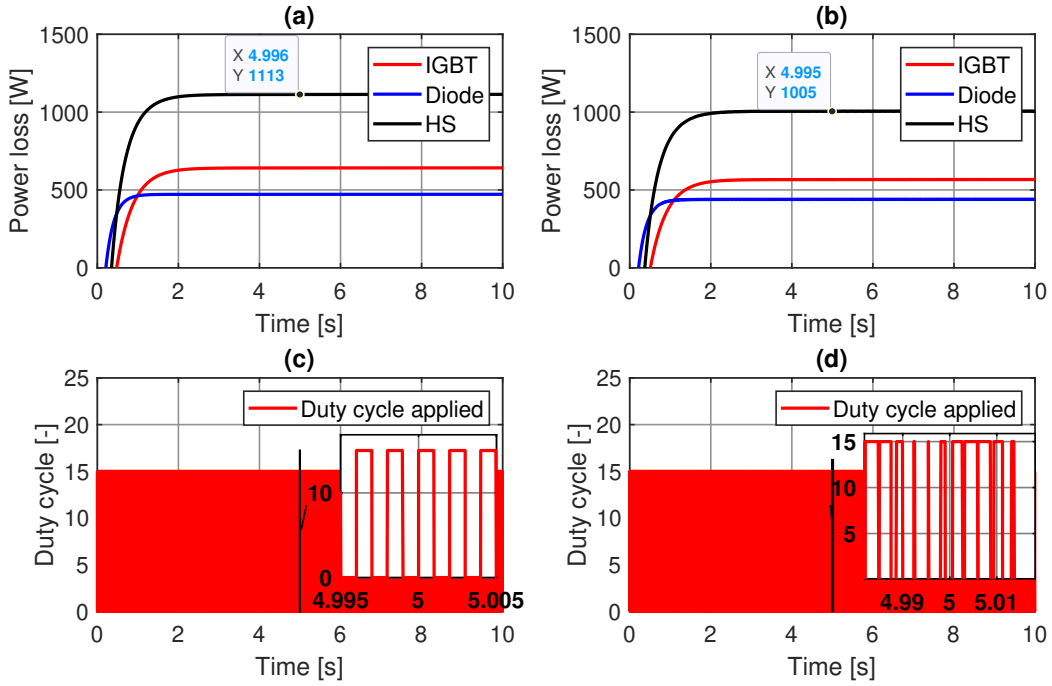


Figure 2.7: Loss simulation of one half-bridge's IGBT, diode and Heat Sink (HS); (left) $f_s = 500Hz$ Duty cycle: 50% $I_{arm} = 500A$ DC, (right) MMC open-loop operation switching $I_{arm} = 500A$ DC.

From Fig. 2.7a, it can be seen that the maximum calculated losses, at worst-case operation, match well with the simulation results. In the right plot in Fig. 2.7, the MMC operation shows lower losses as some duty cycles are lower than 50%. Therefore, lower losses should be expected for the MMC operation. The estimated losses are next used to find a suitable heat sink. However, in order to specify it, a requirement of a maximum allowable heat sink resistance should be found, using the simplified thermal diagram in Fig. 2.8.

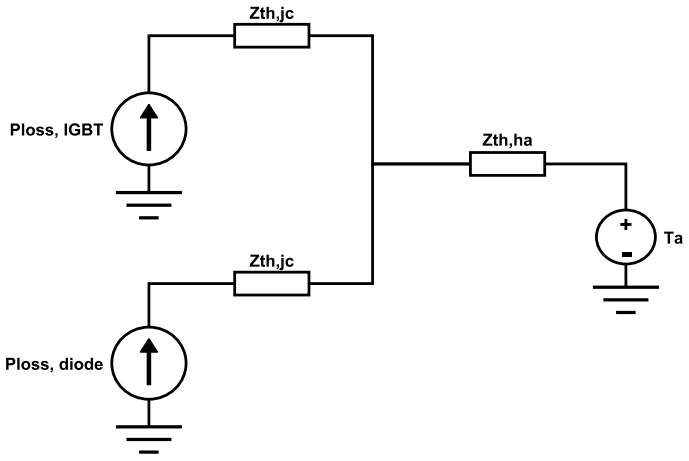


Figure 2.8: Thermal diagram of IGBT and diode heat sources and all thermal resistances.

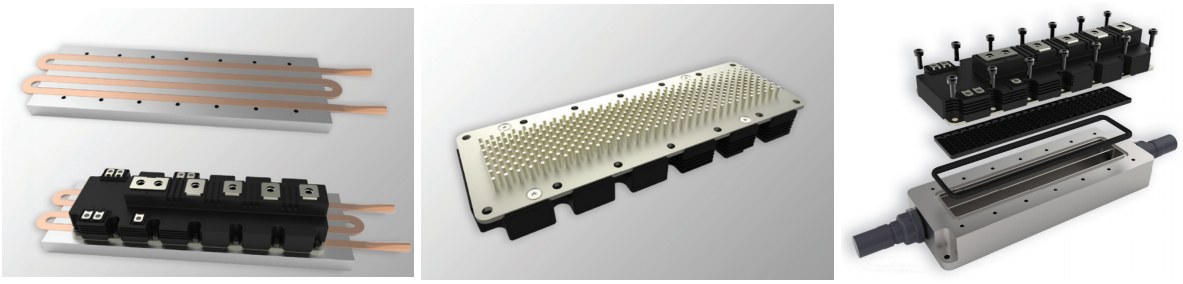
First, the temperature drop from junction-to-baseplate is found for IGBT and diode in (2.4).

$$\begin{cases} \Delta T_{jc_{IGBT}} = R_{th,jc_{IGBT}} P_{loss_{IGBT}} = 24\frac{^\circ C}{kW}(0.5(1.8V \times 500A) + 500Hz(200mJ + 200mJ)) \approx 15.6^\circ C \\ \Delta T_{jc_{diode}} = R_{th,jc_{diode}} P_{loss_{diode}} = 45\frac{^\circ C}{kW}(0.5(1.5V \times 500A) + 500Hz(180mJ)) \approx 21^\circ C \end{cases} \tag{2.4}$$

where $R_{th,jc_{IGBT}}$ and $R_{th,jc_{diode}}$ are found from the IGBT and diode transient thermal resistance in the datasheet [18] using the time corresponding to 500 Hz, using the 50% worst-case duty as earlier assumed. It is seen that the largest ΔT is found across the diode junction-to-baseplate and is therefore used in (2.5) to find the maximum allowable temperature,

$$R_{th,ca} = \frac{T_{j,max} - T_{diode} - T_a - \Delta T_{SF}}{P_{sw} + P_{cond}} = \frac{150 - 21 - 40 - 50}{290W + 825W} \leq 0.035\frac{^\circ C}{W} \tag{2.5}$$

where ΔT_{SF} is a chosen safety margin of 50°C and an ambient temperature of 40°C is considered. Finally, the heat sink should be found among available commercial options. By investigating different manufacturers, it has been found in this thesis that power modules are often bought including a sized heat sink. As the power modules in this thesis do not include a built-in heat sink, other solutions need to be found.



(a) Traditional cold plate. **(b)** Pin-fin heat sink. **(c)** Danfoss ShowerPower® heat sink.

Figure 2.9: Commercial heat sink types available [24].

Multiple solutions exist as seen in Fig 2.9, most common ones being:

- Indirect: Cold plate with internal water flow
- Direct: Pin fins baseplate
- Direct: Shower power (Danfoss)

The direct versions are superior to the traditional indirect cold plate [25] as these bring the cooling water to the baseplate itself, eliminating baseplate-to-heat sink thermal resistance and thereby lowering the overall thermal impedance. Some disadvantages of direct cooling are that the pin fins method requires a special base-plate, while the shower power method requires a special labyrinth design for the water to flow through. However, the main disadvantage of direct cooling is a higher pressure drop across the heat sink which requires more motor power of the cooling system as studied in [25]. For this thesis, the pin fins solution cannot be used in this case as it would require the baseplate of the power module to be changed, hence, a new power module. The shower power could be used with the power module, however it has been found that these are only available as a combined power module and heat sink solution. Therefore, a traditional cold plate is chosen for this design iteration, but could potentially

be changed to other types in future designs. In order to find a suitable cold plate, different solutions are investigated. The widest available solution is the heat sink shown Fig. 2.10.

Figure 2.10: Heat sink with copper tubes cast into aluminium plate [26].

First of all, the mechanical interface needs to fit, here one heat sink shows a promising fit as seen in Fig. 2.11.

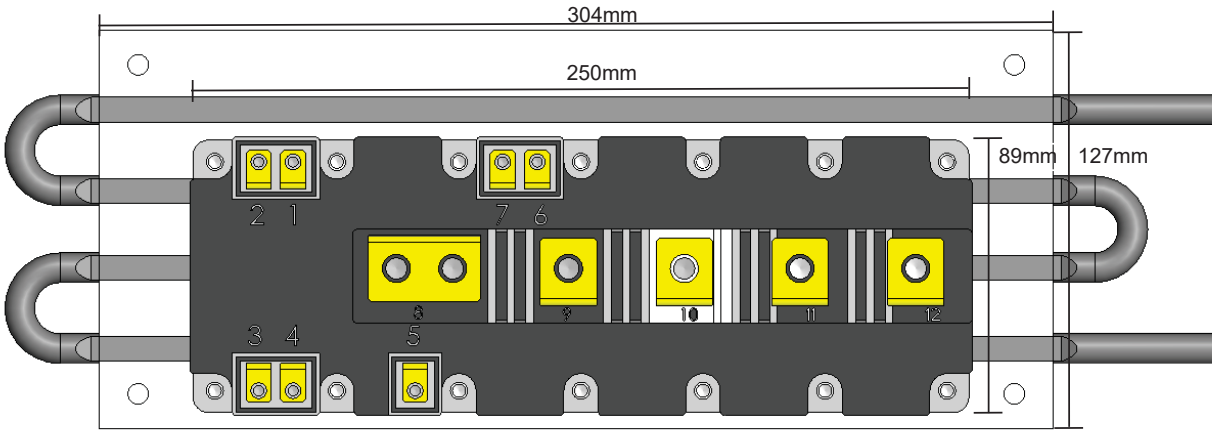


Figure 2.11: Power module on heat sink verifying that hole pattern and pipes are not interacting.

The chosen heat sink is a cold plate consisting of bent copper tubes cast into an aluminium plate. Compared to other cold plates where the water channels are milled into the aluminium, this heat sink brings the copper pipes close to the power module to lower the thermal resistance. Larger heat sinks of the same type, which could carry both power modules of the SM are available. However, as the cooling water circulates below one power module before it reaches the second power module, a ΔT would be excepted and could create unequal operation between power modules, which is highly temperature-dependent. Therefore, single heat sinks are adopted which inputs and outputs are coupled in parallel. The heat sink datasheet [26] gives the thermal resistance as a function of flow in Fig. 2.12.

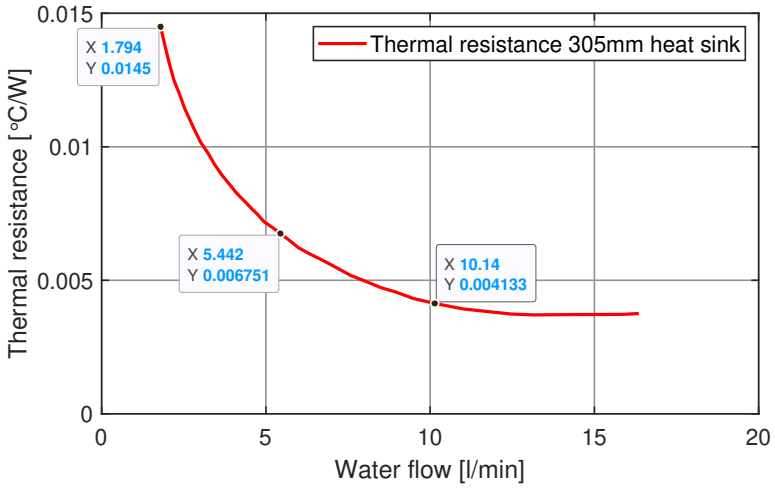


Figure 2.12: Heat sink thermal resistance as function of water flow [26].

As seen in the plot, the thermal resistance is highly water flow-dependent, which means that the water flow could be increased for this operation to allow higher losses. A nominal point is given at 5.5 l/min corresponding to a thermal resistance of approximately 0.0065 K/W, which is well below the requirement of 0.034 K/W. Even at lower flows, down to approximately 1.8 l/min, the thermal resistance is approximately 0.015 K/W and, therefore, still below the requirement. It is therefore concluded that the heat sink should be able to fulfil the requirements. A simulation is conducted in Fig. 2.13.

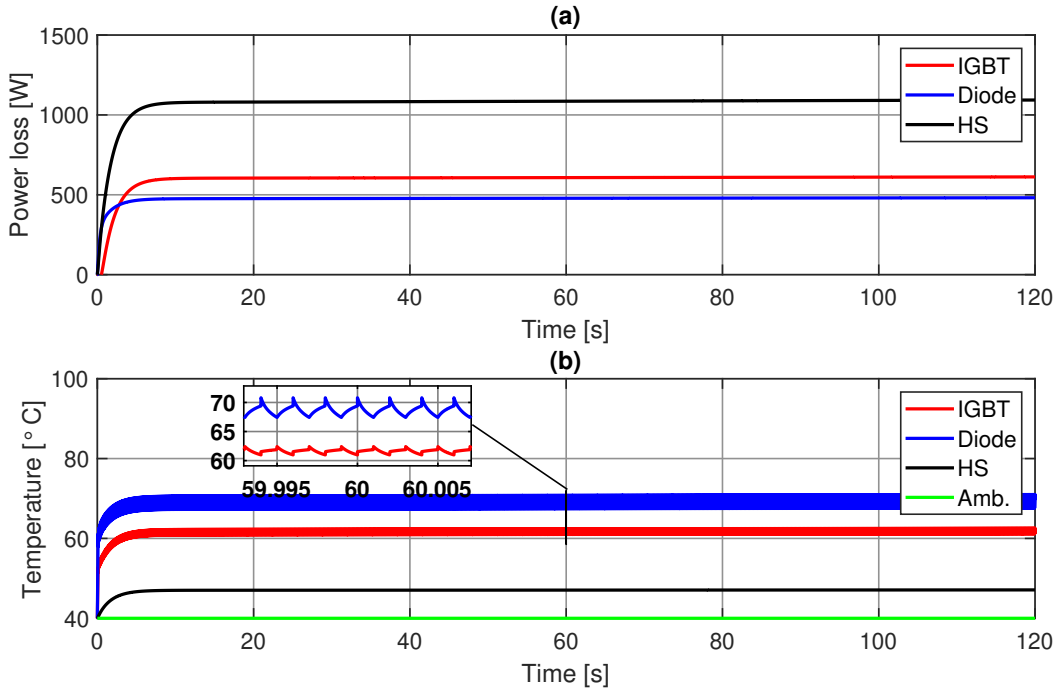


Figure 2.13: Thermal simulation at full load ($f_s = 500Hz$ Duty cycle: 50% $I_arm = 500A$) and nominal flow: 5.5 L/min corresponding to 0.0065 K/W, showing temperature and power losses from IGBT, diode and Heat Sink (HS) along with ambient temperature (Amb).

where a nominal thermal resistance is assumed (corresponding to nominal flow), operation at full-load operation and an ambient water temperature of 40°C is used. 40°C is used as ambient temperature as it is assumed to be a typical water temperature for high-power cooling systems[27]. The reason for this is that if the ambient air temperature rises above the cooling water, condensation emerges which can lead to failure of the electronic components. It is seen that the junction temperatures of both IGBT and diode are below maximum of 100 °C (with 50 °C safety margin). Similarly, a simulation at the lowest given thermal resistance is conducted which is seen in Fig. 2.14.

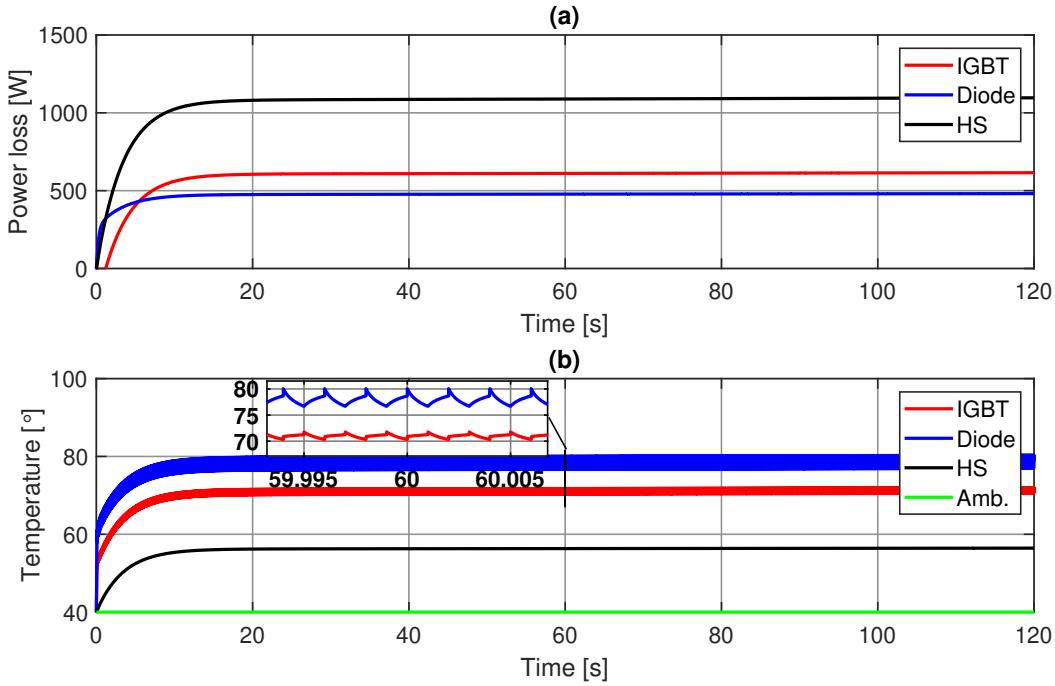


Figure 2.14: Thermal simulation at full load ($f_s = 500Hz$ Duty cycle: 50% $I_arm = 500A$) and nominal flow: 1.8 L/min corresponding to 0.015 K/W.

Similarly, as the lower flow in the heat sink, the maximum junction temperature stays below the maximum temperature allowed as expected. This, therefore, concludes the heat sink choice for the SM. However, in this heat sink design, some simplifications are made, which should be highlighted, as these could lead to deviations at a later test stage. These are listed below:

- Constant ambient temperature across the heat sink plane
- Pure water without the addition of glycol
- Influence of thermal grease and potential air voids in the power module-to-heat sink interface

These simplifications would not hold in practice as the water is heated across the heat sink plate resulting in an uneven heat flow, leading to a higher temperature. However, it is assumed that this effect is minor as a heat sink is used for each power module. The addition of glycol should be made in practice to avoid pipe corrosion. Adding glycol lowers the thermal resistance, as discussed in [27], where the thermal resistance is adjusted based on empirical

formulas for glycol content. It should also be noticed that the chosen heat sink can not be used at infinitely power losses at it also has a maximum temperature. The manufacturer does not give the maximum temperature; however, a maximum power loss of around 3 kW can be dissipated. Finally, thermal grease is applied between the heat sink and power module, which has a thermal resistance of 0.0310 K/W. This is not included as it depends on the layer thickness, which is difficult to ensure in practice and, therefore, hard to model.

2.3.3 Busbar and Electro-Mechanical Design

Besides finding the power hardware components and heat sink, the components need to be coupled into a physical SM design. Concerning this, it is important to pay attention to how the physical surroundings of the converter need to be. In this thesis, a few keywords are given in the introduction which is important for the physical appearance of the final complete converter:

- Scalable, in power and voltage
- Transportable

The first iteration design needs to ensure that these, already at this stage, are considered. Such that later designs can be easier adapted, even though the full MMC design is not a direct target of this thesis. Interpreting the requirements, the final converter needs to be made in modules both at SM and converter-level that allow series or parallel connection at both levels, respectively, to be both scalable in voltage and power. The transportable keyword leads to a converter design that needs to be protected considering its robustness to the environment during transportation and test. Further, it involves being compact to allow transportation that is limited by available transportation forms. In industrial high-power converter applications, converters are often placed in standard electrical cabinets, which are made to make these more robust and protect the equipment. For the design of the SM, it is therefore chosen to pursue a compact SM design such that this later can fit in a limited space. The scalability in voltage will be achieved by serialising the MMC SMs; hence, the SMs need to be coupled in series with each other to form MMC arms. The output of the FB SMs, therefore, needs to be able

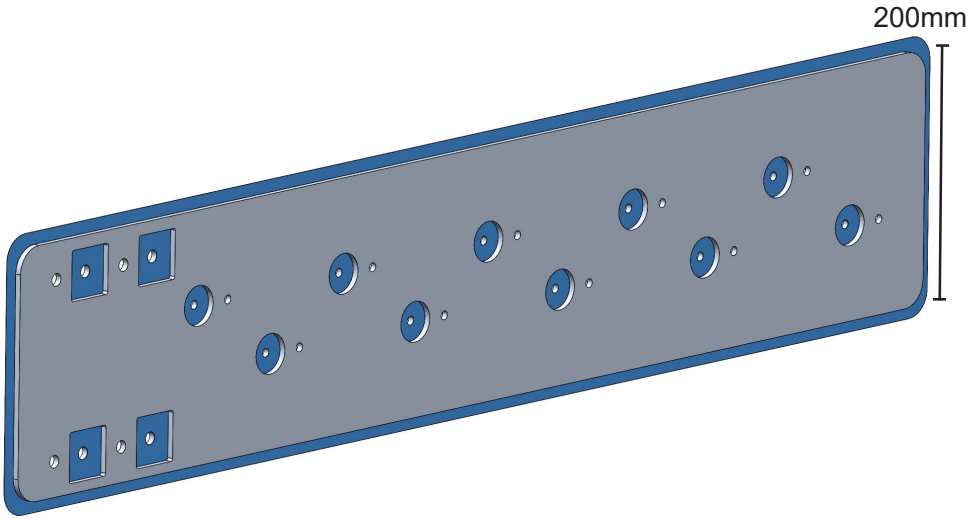


Figure 2.15: Busbar design 1.

to link to each other easily. The following concept design adopts these keywords. An initial sketch of the design is seen in Fig. 2.15. The first initial design consists of a simple two-plate DC-link busbar which is separated by insulation sheets (sandwich structure), similarly to the design studied in [28]. Mechanically, the sandwich busbar structure allows compact and straightforward connection of devices by connecting to either the upper or lower plate by casting larger holes in the opposite plate to allow high enough clearance distances to avoid short-circuits. The specific design in Fig. 2.15 allows simple assembly; however, it has an extensive length which could be problematic for standard electrical cabinets or other solutions. Therefore another design, focusing on making a more compact solution, is shown in Fig. 2.16.

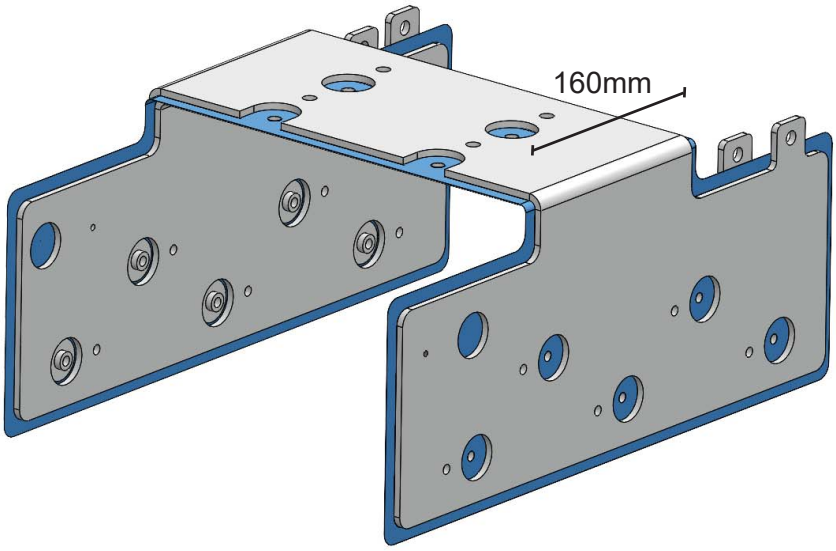


Figure 2.16: Busbar design 2.

This design tries to make the SM as compact as possible to fit it into a compact environment, adopting the same compact DC-link design from the former design using insulation sheets. The assembly compactness could, however, create a more complex assembly process. The mechanical and electrical advantages and disadvantages of the two designs are summarised in Table 2.10.

Table 2.10: Comparison of SM designs.

Design	**1**	**2**
Compactness	-	+
Assembly simplicity	+	-
Robustness	-	+
Symmetry	-	+

In this thesis, the mechanical design is not evaluated further as mechanical analysis is out of scope. However, at later stages, the SM needs to be further developed with the focus on the complete converter design. Therefore, the focus from this point is to compare the designs further, considering their electrical design based on electrical parasitic's influences at SM level, together with the power module EMT model, which was earlier developed.

Besides comparing the two solutions, this analysis also ensures that the influence of the parasitics in each design does not surpass component ratings. By introducing the sandwich busbar concept presented earlier in both designs, the parasitics are reduced due to the large area of the busbars, especially at the terminals, as also studied in [28]. However, the length of the busbars varies between the designs. Further, symmetry is mentioned in the short comparison table above as it is clearly seen that the distances create various current paths from the capacitors to the power modules for both solutions. However, the current travel distance for design 1 is much longer than design 2, which can lead to additional oscillations or ringing due to different delays cost by the parasitics. Both concepts are modelled in 3D and simulated in Ansys Q3D, which is a FEM tool explicitly made to analyse parasitics for power electronic connections considering high-frequency responses. To initialise this analysis, some materials for the insulation and busbars should be chosen. For the busbar, the most used materials are copper and aluminium. With copper, slightly smaller busbar dimensions can be reached; however, the weight is much larger. Therefore, to not add too much weight to the SM design, aluminium is chosen. For the insulation sheet, a mylar sheet is used, similarly to [28]. This insulation is flexible and has a high dielectric strength which makes it suitable for both designs. Some characteristics of the materials are shown in Table 2.11.

Table 2.11: Materials characteristics.

Material	**Aluminium (5754 H111)**	**Mylar**
Resistivity [Ωm]	0.049×10^{-6}	1×10^{17}
Dielectric strength [V/mm]	-	11.7
Permittivity ϵ_r	-	3.2

These material properties are used in the simulations to verify the designs. Before initialising the simulations, the thickness of the materials has to be determined. First, the busbar is sized based on aluminium ampacity, typically given between 0.7 to 1.2 A/mm^2. 0.7 A/mm^2 is used to make a conservative estimation of the busbar thickness. The thinnest dimension for which the full current needs to pass is used to find the minimum thickness from the ampacity. For design 1, this is 200 mm and, for design 2, 160mm. The busbar width can therefore be found to (2.6).

$$\begin{cases} t_{design1} \geq \frac{I_{arm_{max}}}{0.7\frac{A}{mm^2}w} = \frac{500A}{0.7\frac{A}{mm^2}200mm} \approx 3.6mm \\ t_{design2} \geq \frac{I_{arm_{max}}}{0.7\frac{A}{mm^2}w} = \frac{500A}{0.7\frac{A}{mm^2}160mm} \approx 4.5mm \end{cases} \tag{2.6}$$

From the above approximation of the minimum thickness, the final thickness of the two designs is chosen to 5 mm to satisfy both solutions. Next, the thickness of the mylar is chosen. Mylar is available in multiple thicknesses, ranging typically from 0.01 to 0.1 mm, which increases the dielectric strength ranging similarly from 2.5 to 11.7. The mylar available for this project is 0.1 mm and is the one presented in Table 2.11. The mylar has a relatively large dielectric strength compared to the nominal SM voltage of 1000 V. In theory, only one sheet is needed; however, two are used to ensure high-quality insulation after assembly where mechanical stress can reduce the strength of the insulation. Finally, the total thickness is 0.2 mm. Where bolts penetrate the busbars mylar, a minimum clearance distance of 8 mm is needed, considering IEC60664-1 [29] where a rated impulse voltage of 8 kV should be expected, leading to the clearance distance. Next, the analysis of the two busbar solutions is initiated to find their parasitic values. The Ansys Q3D simulation is made using the individual 3D model of

the busbar with the dimensions earlier described for the electrical conditions and a size large enough to fit the ten capacitors and two power modules chosen in the former section. The parasitics are calculated based on finding resistance, self-inductance (same busbar), magnetically coupled inductance (between busbars), and capacitance value between specified nodes, for which the principle is shown for four nodes in Fig. 2.17.

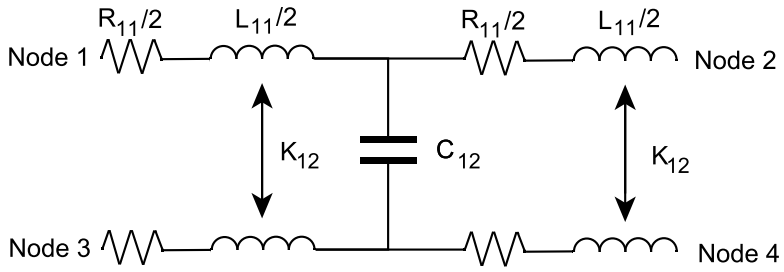


Figure 2.17: Principle of Q3D simulation.

As both busbar designs have several nodes, considering the number of capacitors and power module nodes, the impedance matrices are extremely large. However, as Q3D can export to a SPICE model block, it simplifies the implementation in LTspice. Still, to compare the solutions before the SPICE simulation, the worst-case parasitics are extracted in Table 2.12.

Table 2.12: Worst-case parasitics.

Design	**1**	**2**
DC-link parasitic capacitance [nF]	11.9	11.7
Worst-case DC Resistance [$\mu\Omega$]	34.3	24.1
Worst-case DC Inductance [nH]	521.2	185.1
Worst-case AC Resistance [$m\Omega$]	81.2	21.3
Worst-case AC Inductance [nH]	265.6	98.8

First, the parasitic capacitance is given. As this analysis is made for the DC-link, this capacitance is not of a significant influence as the DC-link is charged to a constant DC voltage. This capacitance will, therefore, just add to the capacitor bank of 4 mF. However, the resistance and, especially, the inductance are of interest as these will influence the voltage during IGBT turn-on and off due to high di/dt. The worst-case conditions given in Table 2.12 are for design 1 from the capacitor in the furthest corner of the busbars to the power module. For design 2, it is from the capacitor in the lower right corner (Fig. 2.16) to the power module. It can be seen that the parasitic inductance is halved from design 1 to design 2 considering the AC inductance, which is analysed at 30 MHz to find the value influencing at high frequency. Due to the skin effect, the AC resistance is also only 1/4 for design 2 compared to design 1. Next, to see the influence of all the parasitics, a simulation is conducted using the EMT model of the power module. The main parasitics effect of interest is the inductance, as it will give rise to oscillations in both voltage and current. A comparison of the DC-link parasitics is seen in Fig. 2.18 for the DC-link voltage and collector-emitter voltage in a no-load saturation.

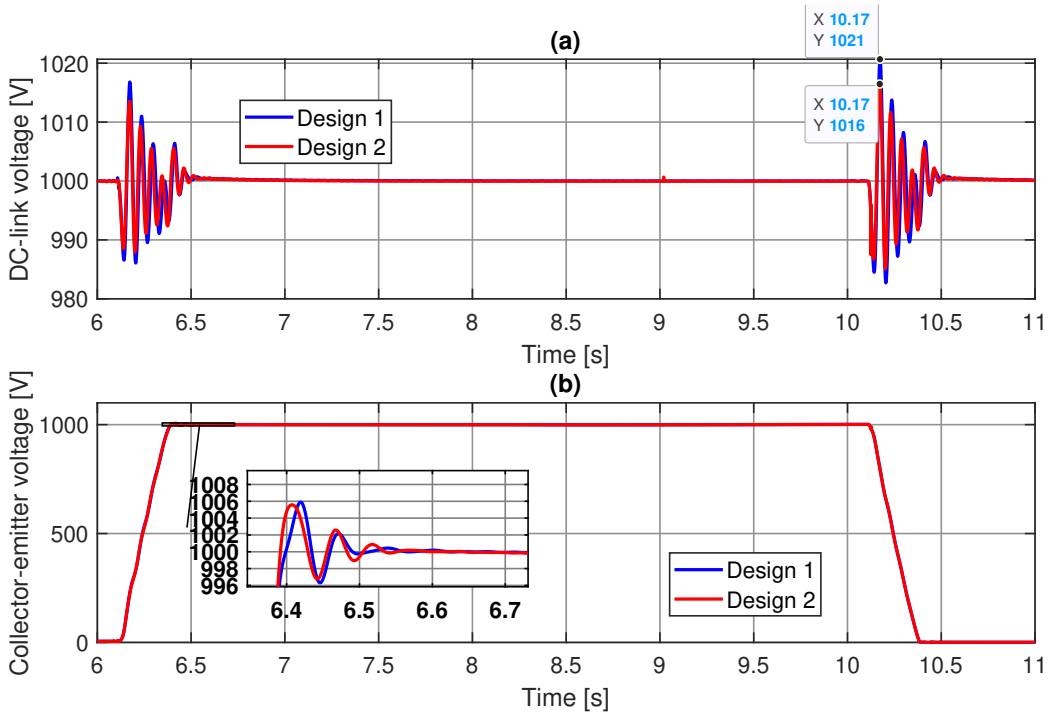


Figure 2.18: Transient comparison of FB SM design 1 and design 2 with DC-link voltage of 1000 V DC at no-load.

As it can be seen, the DC-link in Fig. 2.18a presents oscillations leading to a voltage peak of up to 21 V for design 1 while only 16 V for design 2. These results are expected as the parasitic inductance is higher for that solution. However, both solutions only contribute with a few percentages of voltage above nominal and are therefore far from the maximum requirement of 1350 V, considering the maximum capacitor voltage leading to a maximum overshoot of 35%. Therefore, both solutions could be potentially used based on this simulation. Similarly, considering the collector-emitter in Fig. 2.18b, the overshoot during switching allowed is 70% (considering the nominal of 1000 V and 1700 V maximum rating), both solutions are within this range. To see the effect of load current, a simulation is conducted in Fig. 2.19 for around 500 A. From the load simulation, it can be seen that a slightly higher overshoot is obtained at the load case. The reason is that the reverse recovery of the diode influences the voltage due to the high reverse current. The high current also influences the parasitics, which therefore lead to a lower voltage on the DC-link. Both cases are, however, within the limits of allowed -10% voltage. It should be stated that in the case that the SM has low voltage due to voltage ripple under load, which could create a low voltage event. From the investigation above, design 2 is the most suitable design from an electrical point of view. Any further optimisations should therefore lead to only smaller distances between the individual terminals.

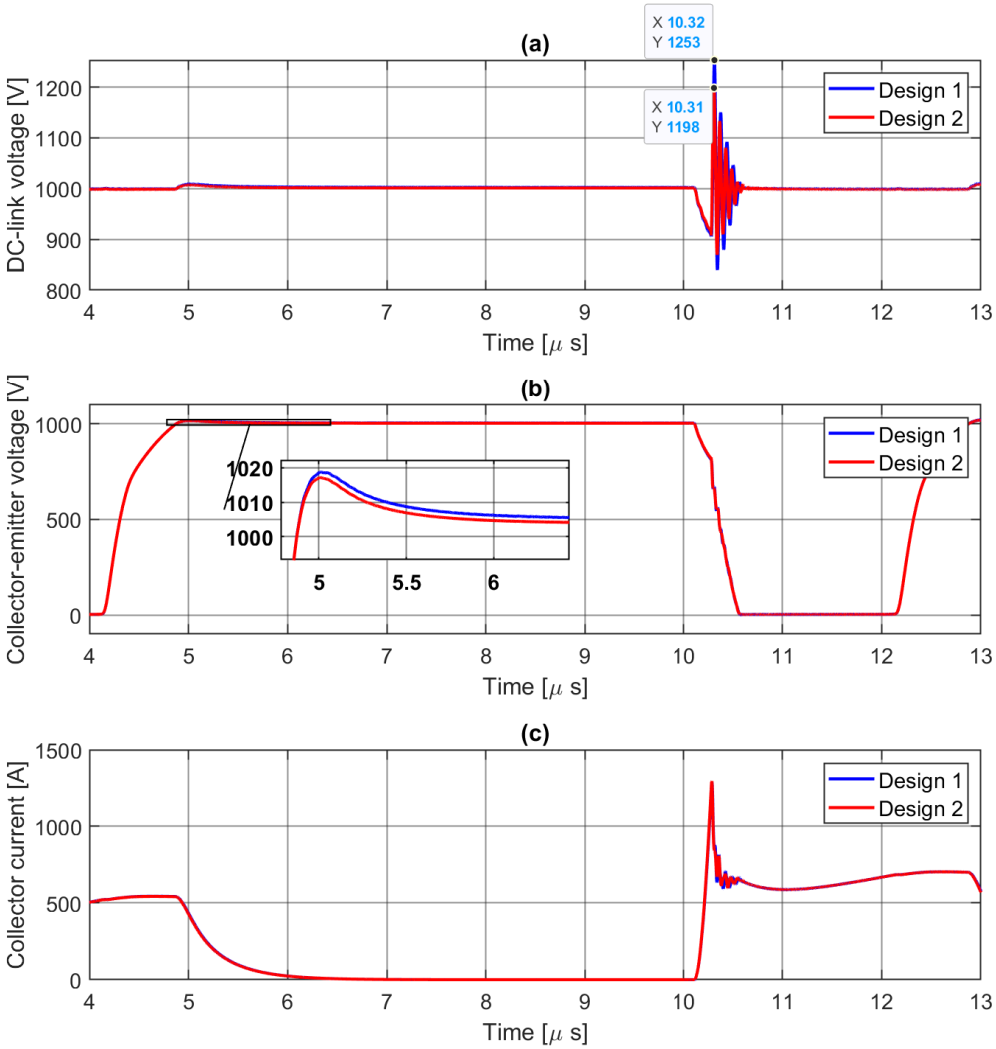


Figure 2.19: Transient comparison of FB SM design 1 and design 2 with DC-link voltage of 1000 V DC at approximately 500 A DC load.

From the above analysis, involving both mechanical and electrical characteristics analysis, the choice of the SM electro-mechanical design is chosen to design 2. It is concluded that the design has the best properties both electrically, considering its influence during operation, and mechanically, considering its compactness. The "cubical" design opens the possibility for various solutions, not limited to specific power hardware. Further, it allows updates in all dimensions for future iterations, considering the full converter setup and alternative power hardware. The final assembly with all power hardware, including also control hardware, which is described in the coming sections, can be viewed in Fig. 2.20.

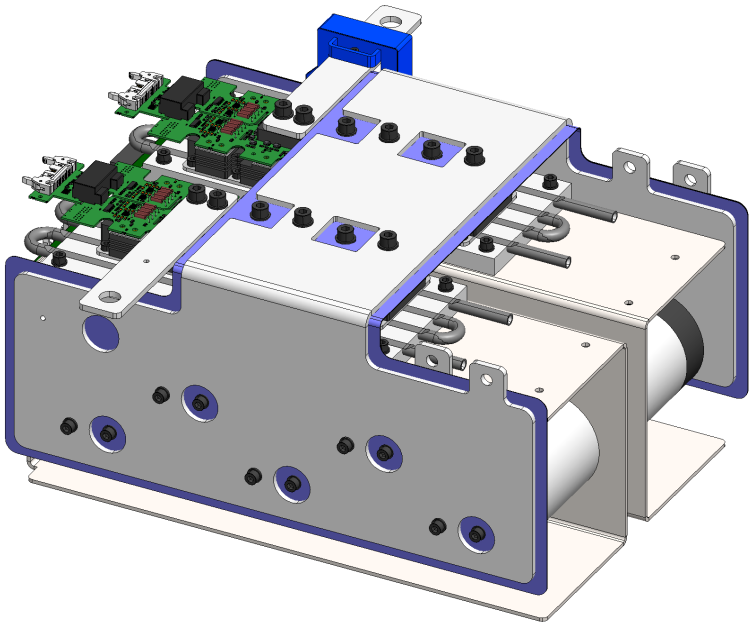


Figure 2.20: Final SM with all power hardware.

Discharging Resistor

To discharge the DC-link, a discharging resistor is added across the DC-link. The resistor should be chosen based on the three criteria in (2.7).

$$\begin{cases} \tau = R_{dc}C_{SM} = R_{dc} \times 4mF \\ I_{R_{dc},max} \geq \frac{V_{dc}}{R_{dc}} = \frac{1000V}{R_{dc}} \\ P_{R_{dc},max} \geq \frac{V_{dc}^2}{R_{dc}} = \frac{(1000V)^2}{R_{dc}} \end{cases} \tag{2.7}$$

In (2.7), it is of interest to decrease the discharging time; however, as the resistor is always coupled to the DC-link, it will decrease the efficiency of the SM. Therefore a resistor in the $k\Omega$ range is of interest which also requires lower space. A resistor with the properties in Table 2.13 is chosen.

Table 2.13: DC-link resistor of $50k\Omega$ ratings.

Property	Value
Resistance [Ω]	50 $k\Omega$
Power dissipation without heat sink [W]	40 W
Voltage maximum (DC)	1400 V

The reason for choosing the resistor is its maximum voltage rating above the rated DC-link voltage of 1000 V $\pm$10%. The chosen resistor does not give a maximum current; however, it gives the maximum voltage rating and power dissipation. In this case, a resistor rating without a heat sink is chosen; even though larger dissipation could be possible with a heat

sink, only 10 W is needed. To be conservative, two resistors of 50 $k\Omega$ are chosen, giving the characteristics in (2.8).

$$\begin{cases} \tau = RC = 100k\Omega \times 4mF = 400s \approx 6.7min \\ I_{R_{dc},max} \geq \frac{V_{dc}}{R_{dc}} = \frac{1000V}{100k\Omega} = 0.01A \\ P_{R_{dc},max} \geq \frac{V_{dc}^2}{R_{dc}} = \frac{(1000V)^2}{100k\Omega} = 10W \end{cases} \tag{2.8}$$

The discharging time is therefore 6.7 min for discharging from the nominal voltage to 0, where 25 V is chosen as the safety voltage as it is below the Safety Extra Low Voltage (SELV) level of 50 V, as described in IEC60364 [30].

2.4 Control Hardware

In this section, the second paralleled track in the methodology giving the description and design of the SM-level control hardware is presented. It mainly consists of two elements: the gate driver, which serves as an interface to the power hardware, and a control Printed Circuit Board (PCB) which is in charge of the local control of the SM, data acquisition and interfacing to other SMs and the top-level controller [13]. These elements are further described in the following sections.

2.4.1 Gate Driver

As presented in Section 2.2, the SM topology chosen is a FB, therefore, four switches need to be controlled. For this purpose, a suitable gate driver needs to be found. Gate drivers play an important role as these interconnect the control side of a power converter with its power stage, providing fast switching times and reducing the related losses. Special attention needs to be put when designing or choosing the gate driver circuitry as typically, the components on the control side are not rated to withstand the higher voltages on the power side. Further, the semiconductor device's gate terminal has specific requirements which can not be fulfilled by control circuitry directly. To have a clearer idea, Fig. 2.21 shows the standard structure of a gate driver.

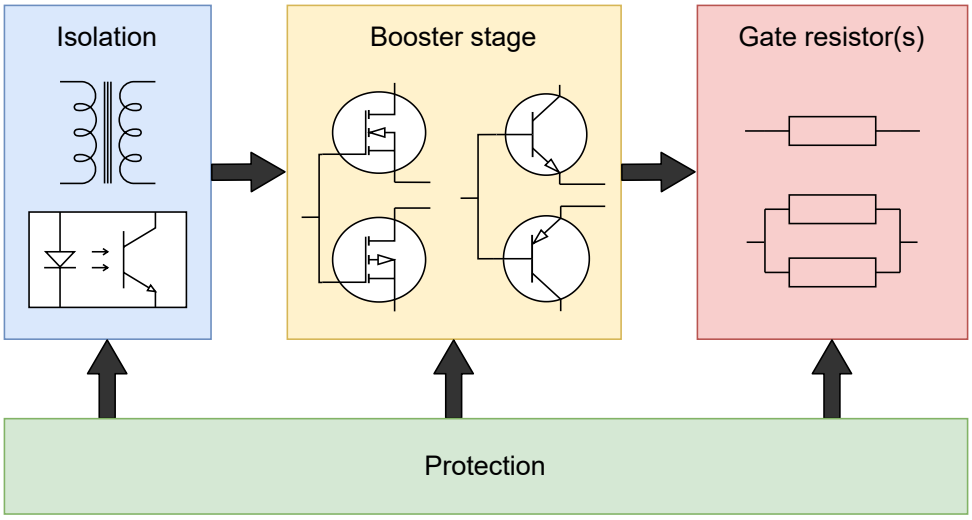


Figure 2.21: Basic structure of a gate driver circuit.

From Fig. 2.21, four main stages can be identified in a gate driver:

- Isolation. It ensures that the control and power sides of the converter are decoupled, avoiding high voltages to be applied across the control circuit components. The galvanic isolation can be magnetic, which is typically included in the gate driver power supply but also for the gate driving signals, or optical, which is mainly used for the PWM and other control signals. It also provides a barrier for undesired distorting signals on the control side generated by the switching.

- Booster stage. It adapts the switching pattern generated by the corresponding control unit to the voltage levels that should be applied in the semiconductor device gate terminal to either turn it on or off while delivering the required gate charge and peak current. This stage consists typically of an arrangement of BJTs, MOSFETs or a combination of both.

- Gate resistor(s). These are in charge of limiting the current through the gate terminal and controlling the turn-on and -off times as these interact with the power module internal capacitances. Different resistor arrangements can be adopted depending on the desired performance of the semiconductor device. In most applications, a single resistor is used for both turn-on and turn-off processes; however, it is highly recommended to have different resistor values for each process as the internal dynamics of the IGBTs are also different in these two cases. Optimisation of the resistors can also be used to optimise the power loss characteristics.

- Protection. This block makes sure that both the gate driver circuitry and its corresponding switch are operated safely. To protect the gate driver outputs, Schottky diodes are placed to provide a path for reverse currents that can damage the booster stage's transistors. Typical protection measures are under-voltage lockout (UVLO), programmable dead-time, over-current, over-temperature, dv/dt protection commonly by active Miller clamping, switch desaturation detection for short-circuit protection, among others.

Another essential feature of gate drivers is their powering. In most HB applications, the low switch is referred to as ground, and it is only the high side that needs delicate attention as it is referred to the middle point of the HB. For applications where the DC-link voltage is higher than the rated voltage of available isolated gate drivers, the gate driver circuit needs to be supplied from a separate voltage source which can provide even higher isolation from the high voltage DC-link [31], [32]. However, in MMC applications, a single SM can be considered floating in the converter arm, which is important as the DC-link voltage across multiple SM will be higher voltage-to-ground than the individual SM local DC-link voltage. If the SM were not floating, it would require much higher isolation. With the assurance of a floating SM, the required isolation can be focused on the SM alone. Therefore, a separation between high- and low-side gate driver circuits must be provided using either isolated drivers or a dedicated power supply.
Special attention is also needed in the gate driver circuitry when operating IGBT switches in parallel, as mentioned in the previous section. The gate driver must ensure equal current sharing among the different paralleled devices as this can have a significant effect on the switch lifetime [33]. First, the gate driver needs to have enough driving strength to guarantee the turn-on of all devices. The propagation delay of the PWM signals through the gate driver also plays an important role in the current distribution. Another critical component of the

gate driver circuit affecting IGBT paralleling is the gate resistor. Having a unique gate resistor for all the switching devices can lead to oscillations of the collector voltage and current and non-simultaneous turn-on if the IGBTs characteristics such as threshold voltage or gate capacitance are different. Therefore, having a gate resistor for each IGBT is highly recommended. It is also essential to minimise the parasitic inductance of the parallel gate connection as it can lead to additional oscillations.

Knowing this structure, different approaches can be followed. The first one is designing the gate driver circuitry for the specific application. This requires more design effort as all the components need to be chosen and integrated based on the application. This solution is typically adopted when using discrete-packaged power devices. The second approach is appropriate when using power modules, for which commercial plug & play drivers are available. These simplify the design process, are easy to mount on the power module, and typically adapted for a specific semiconductor device model, presenting the corresponding layout and gate resistors values. For this thesis, a Danfoss power module in HB configuration is used; therefore, a suitable gate driver is chosen, considering the requirement of using commercial products for the driver from the DFMEA. Among different manufacturers, Concept Technologie (part of Power Integrations) offers a wide range of gate drivers, being the 2SP0320x series the best fit for the considered power module [34], [35]. This gate driver presents two types of interfaces: an electrical and a fiber-optic interface. For a first iteration of the MMC SM design, the electrical interface is chosen in this thesis as it simplifies the control hardware design part, needing fewer additional components than the fiber-optic option. As functionally, both gate driver options behave equally, the electrical-interface variant still allows evaluating the SM performance. The gate driver model considered in this thesis is the 2SP0320T2C0-17, and it is shown in Fig. 2.22.

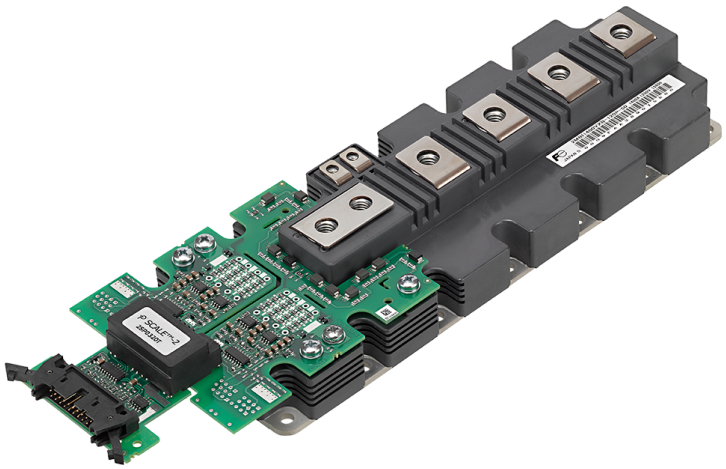


Figure 2.22: 2SP0320T2C0-17 mounted on the IGBT module.

Among the different characteristics of the 2SP0320T2C0-17, the following are highlighted:

- Suitable for half-bridge topologies.
- Blocking voltage up to 1700 V.
- High isolation level (5 kV).

- 15 V logic level for the electric signals.
- +15/-10 V gate driving.
- On-board isolated DC/DC supply.
- Small time delay and low jitter.

Besides the electrical characteristics, the chosen gate driver presents appealing functionalities. To explain them, the gate driver block diagram is introduced, which is shown in Fig. 2.23.

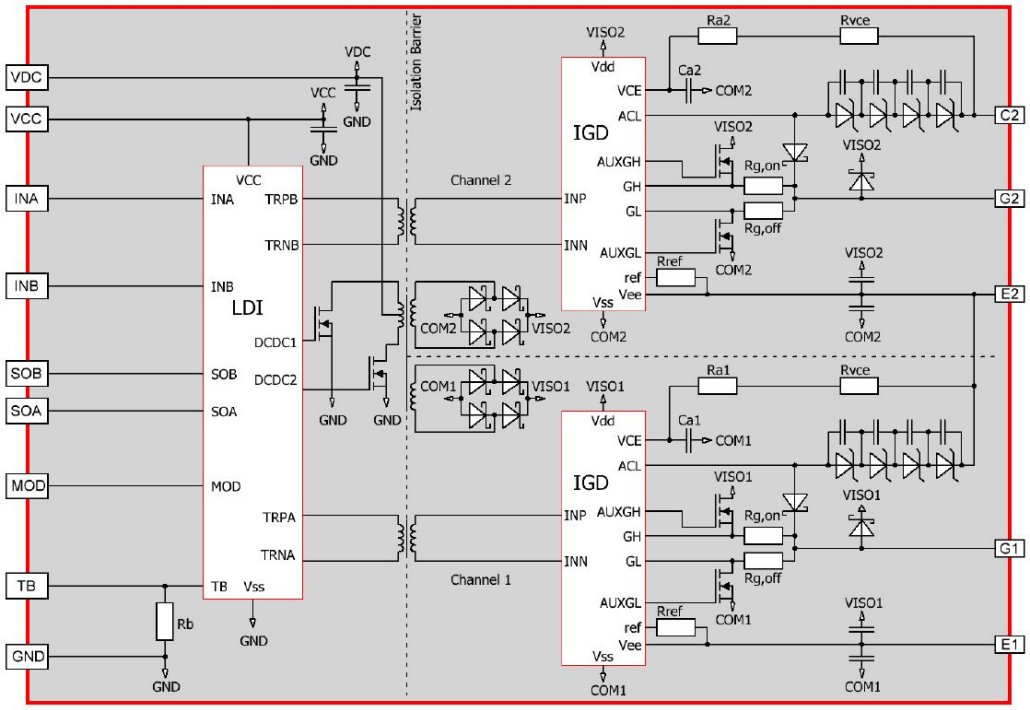


Figure 2.23: 2SP0320T2C0-17 block diagram [35].

The first functionality is the mode selection which can be configured through the input pin MOD. In direct mode, each gate signal follows the corresponding PWM pattern received in pins INA and INB. The signals are independent of each other at the gate driver level, and it is the corresponding controller which has to ensure that the dead-time between both allows a safe operation of the power module. However, in half-bridge mode, only one driving signal is needed (INA), and the gate driver itself is in charge of generating the dead-time. The other input (INB) is used as enabling signal, blocking both channels when having a low level.

From Fig. 2.23, signals SOA and SOB can also be identified in the gate driver interface. These signals are related to the gate driver protection and output a high level (15 V) when no fault is detected. 2SP0320T2C0-17 protects against power supply under-voltage and short-circuit of the power module events. For the first one, the gate driver has an under-voltage monitoring circuit that measures the supply voltage of the primary side and the secondary side for both the upper and lower switch. If any of the voltages go lower than the configured threshold, the gate driver immediately sets a negative gate voltage on both IGBTs, turning them off, and SOA and SOB outputs are set to a low voltage level to indicate the fault event. Regarding the

short-circuit scenario, the gate driver presents a collector-emitter voltage monitoring circuit, based on a resistor network, for both IGBTs. After the corresponding IGBT turn-on, V_{ce} is measured and, if its value is higher than the programmed threshold, a short-circuit has happened, following the gate driver the same procedure explained for the supply under-voltage case. The fault output pins (SOA and SOB) value are reset after a blocking time has elapsed. During this blocking time, the PWM pulses sent by the controller unit are disregarded. This blocking time has a default value of 90 ms, but it can be modified to a value between 20 and 90 ms by placing the correct resistor value between pin TB in Fig 2.23 and GND [35].

The gate driver also presents an advanced active clamping function. This feature allows to partially turn on the IGBT when its collector-emitter voltage exceeds a specific value during the turn-off, keeping the IGBT in the linear operating range. This feature is accomplished by creating a path from the IGBT collector to its gate terminal using Transient Voltage Suppressor (TVS) components. Additional protections not covered by the gate driver circuitry are discussed later in this section.

2.4.2 Control PCB

Once the gate driver is selected based on the power module used, the next step is to design the control PCB that hosts the corresponding controller and the different components needed to ensure the correct operation of a standalone SM. There are two main functionalities for the control PCB; the SM local control and the communication with the top-level control unit.
Regarding the SM control, different approaches have been studied in literature [36]–[39] but, in general, all of them have the same purpose; a balanced SM capacitor voltage to ensure stable operation. This is usually linked to the control of the circulating current through the converter arms. Additionally, different modulation techniques can be applied for the switching of the SM semiconductor devices [36], [40], [41], and the chosen one is also implemented in the local controller. However, before configuring and testing the SM for a MMC application, the SM design needs to be tested both electrically and thermally as described by the DFMEA in Section 2.2.1, which are the focus for the design in this thesis as described in thesis limitation. Therefore, to test the SM design, the control PCB is used to switch the IGBTs through the gate driver circuitry by an open-loop control strategy and monitor the different magnitudes in the SM, following the test modes that are described in Chapter 3.
There are several options for the local controller, where Digital Signal Processor (DSP) and Field-Programmable Gate Array (FPGA) being the most popular [13], [42], [43]. Each of them presents different pros and cons. The DSP has a wide range of peripherals with a fairly high computational speed and a reasonable cost; while, the FPGA allows lower time delays, which is appealing to maximise the control bandwidth as much as possible. However, the FPGA has no embedded peripherals, needing external components or modules to complement its operation, which is translated into a higher cost (added to the base cost of the FPGA which is already higher than most DSPs). Therefore, the controller choice is based on a trade-off between performance and cost.
Complementing the main controller, several sensors and ICs are needed for signal processing and interfacing to other elements within the SM. All these elements, and other auxiliary components like power supplies, connectors and passive components, are integrated into a PCB which block diagram is shown in Fig. 2.24.

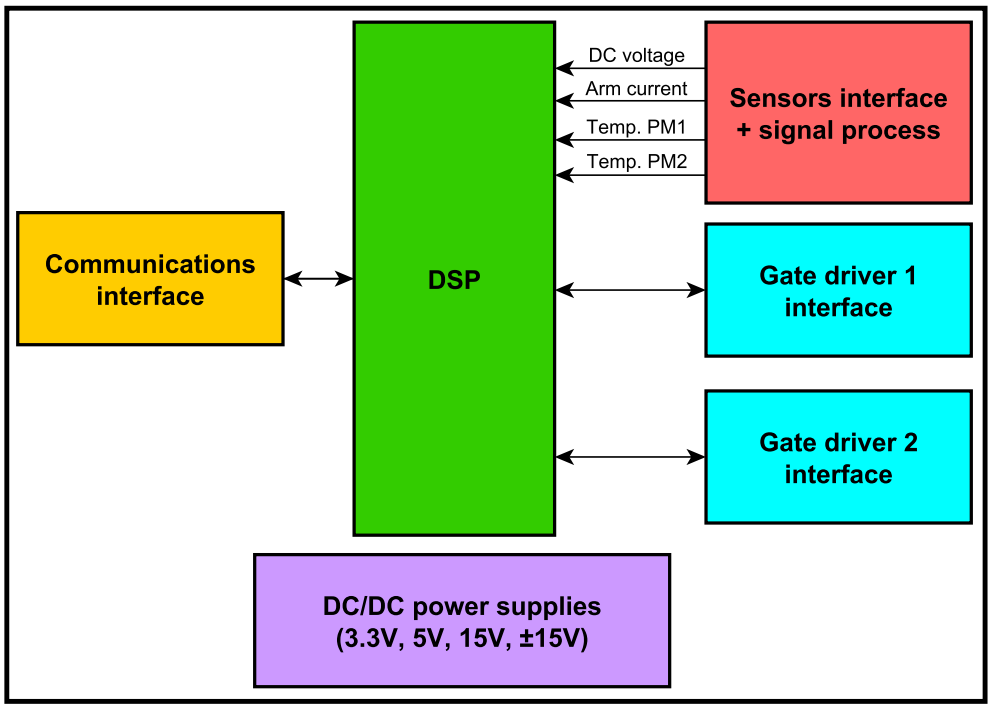


Figure 2.24: Sub-module interface PCB block diagram.

In the following parts, the functionalities of the interface PCB are explained in greater detail, as well as the choice of the different components to accomplish each of them, following the groups presented in Fig. 2.24.

DSP

In this thesis, a DSP is chosen as the core element for the SM control due to its lower cost compared to the FPGA which additional performance is not needed for the SM due to its low switching frequency. Specifically, the selected DSP is the TMS320F280025 from Texas Instruments [44]. This DSP choice is made based on a particular feature available in this specific DSP named Fast Serial Interface (FSI) [45], [46]. This new communication protocol may be interesting for MMC applications where the communication network can be large and complex due to the high number of SMs involved. The transmission rates achieved by FSI are appealing as these permit a big chain of SMs with a relatively small time delay which allows reaching a high control bandwidth. This communication method is further explained later in this section.
Besides this feature, the DSP has other interesting characteristics for the control of power converters. These are listed below:

- 32-bit core at 100 MHz.
- Floating-Point Unit and Trigonometric Math Unit. Suitable for power applications control.
- 128 KB on-chip flash memory.
- 14 PWM channels with integrated dead-band support.

- 12-bit Analog-to-Digital Converter with 16 channels.
- Traditional communication protocols as CAN, I2C, SPI or UART.

Based on these specifications, the chosen DSP can satisfy the demands required for a SM controller such as:

- Reading the analogue signals involved in the power hardware operation.
- Calculating the new references for the control actions and, correspondingly, the switching signals for the IGBTs.
- Communication to other SMs and top-level controller.
- Local faults detection.

For this thesis, a Texas Instruments controlCARD based on the mentioned DSP is chosen (TMDCNCD280025C), which is illustrated in Fig. 2.25. This controlCARD and its corresponding docking station are mounted on the control PCB. This makes the overall design process faster and simpler for prototypes.

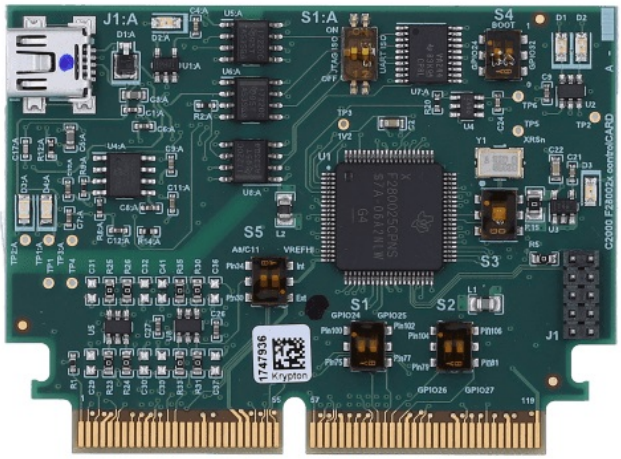


Figure 2.25: TMDCNCD280025C controlCARD.

Gate Drivers Adaptation Interface

As introduced in Section 2.4.1, the chosen gate driver, 2SP0320T2C0-17, can control one HB so there are only two connections from the PCB to the power modules. The interface from the controller to the gate driver is identical for each of the gate drivers. Moreover, for this thesis, the chosen interface is based on electric signals. The selected gate driver operates with a 15 V logic [35]. Therefore, the PWM signals provided by the DSP need to be adapted from 3.3 V to 15V. For this purpose, a voltage-level shifter is used. In this case, the CD4504B IC from Texas Instruments has been selected [47]. Additionally, the gate driver provides two output fault signals, one per IGBT, which are related to both an under-voltage event in the primary- or secondary-side power supply of the driver or a short-circuit of any of the power modules. Similarly, the CD4010B IC is used to translate the voltage level from 15 V down to 3.3 V [48], making the fault signals suitable for being read by the DSP. A schematic of this interface is shown in Fig. 2.26.

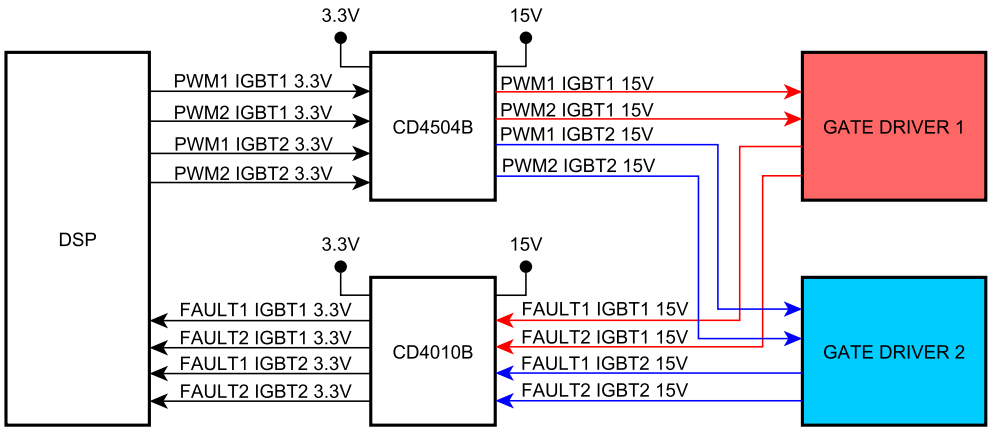


Figure 2.26: Interface between control PCB and gate drivers.

Sensors and Analog Signal Processing

Measuring the analogue signals during operation is an important part of any power converter. The measurements are typically used for control purposes, but these can also be used for monitoring and protection. In MMC applications, signal sensing takes place at two levels: top-level, which deals with the three-phase output, and internal level, related to the SM dynamics. As this thesis covers the SM hardware design, this section describes the data acquisition at this level. The most critical action at the SM level is keeping the capacitor energy balanced to ensure a stable operation of the overall MMC [36]–[39]. To achieve this, the SM capacitor voltage needs to be controlled and measured at any time. Concerning the current measurement, it is typically done per converter arm as the same current magnitude flows through all the SMs. However, as this thesis focuses on a first design concept, the SM output current measurement is included for testing and validation purposes. Finally, the Danfoss IGBT module used has an embedded temperature sensor available that can be used to monitor the device's baseplate temperature for a safe operation objective.
There are multiple approaches and types of sensors that can be chosen. One option can be using commercial sensors that directly translate the high voltages and currents signals to lower voltages/currents. Standard values for industrial sensor outputs are typically 0-5 V, 0-10 V, $\pm$5 V and $\pm$10 V for voltage, and 0-20 mA, 4-20 mA and $\pm$25 mA for current signals [49]. An alternative can be using dedicated ICs like AMC1302, and AMC1311 from Texas Instruments [50], [51], for current and voltage sensing, respectively, which are high-precision reinforced isolated amplifiers. However, this option would require additional components like a resistive voltage divider or a shunt resistor and an isolated power supply for the primary side of the ICs. Furthermore, any of the options require additional signal processing to adapt the output of the corresponding sensor to an acceptable input level for the DSP Analog-to-Digital Converter (ADC), in this case, 0-3.3 V which are further converted into a 12-bit result. The following lines present the sensor choice as well as the adaptation circuits for each of the magnitudes, considering the DFMEA requirement of using commercial sensors.

The DC-link voltage measurement is done with a voltage transducer, specifically DVC 1000P (Fig. 2.27) from LEM [52]. It allows measuring a voltage range of $\pm$1.5 kV, directly inputted on its terminals, being both DC and AC. Its use is fairly simple as it can be directly mounted

on a PCB without requiring extensive space or add-ons. Some of its appealing characteristics are listed below:

- 5 V power supply.
- 0.5-4.5 V voltage output (internal offset of 2.5 V).
- High isolation (4.2 kV).
- 47 kHz bandwidth (-3 dB).
- Low linearity error ($\pm$0.2%) and thermal drift ($\pm$0.4%).
- Low power consumption.

Figure 2.27: Sensor DVC 1000-P.

As mentioned, the sensor output is in the 0-5 V range; for the DSP to read it. The signal, therefore, needs to be translated to the correct voltage level between 0-3.3 V. A common approach for the adaptation of analogue signals is using circuits based on operational amplifiers. In this case, the selected operational amplifier is the OPA2354 from Texas Instruments [53], which is a wide-bandwidth rail-to-rail input/output amplifier. A voltage divider with a 3.3/4.5 gain is connected to the non-inverting input of an Op-amp used in a buffer configuration. A second-order RC low-pass filter with a cut-off frequency of approximately 10 kHz is added in between the DVC 1000-P and the voltage divider to filter possible high-frequency undesired components coupled to the circuit without the addition of high phase lag, leading to the time delay for the signals of interest in the 0 to 65 Hz range. The resulting circuit can be seen in Fig. 2.28.

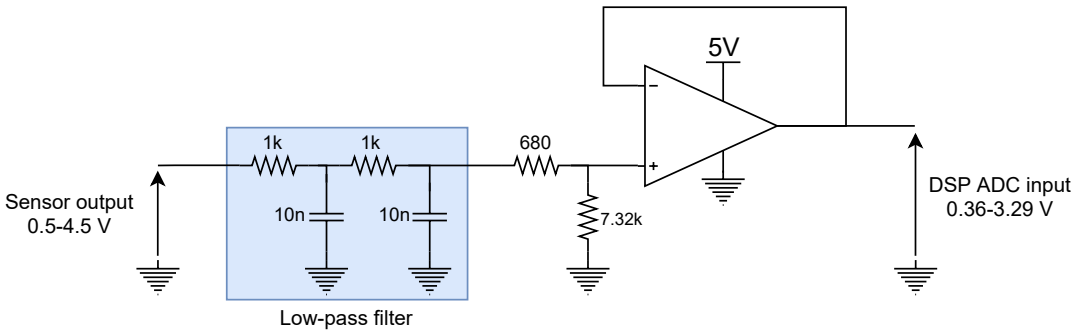


Figure 2.28: DC-link voltage signal processing circuit.

A PLECS simulation emulating the voltage sensor output is carried out to check that the signal obtained after the Op-amp is suitable to be connected to the DSP range. The simulation result can be seen in Fig. 2.29.

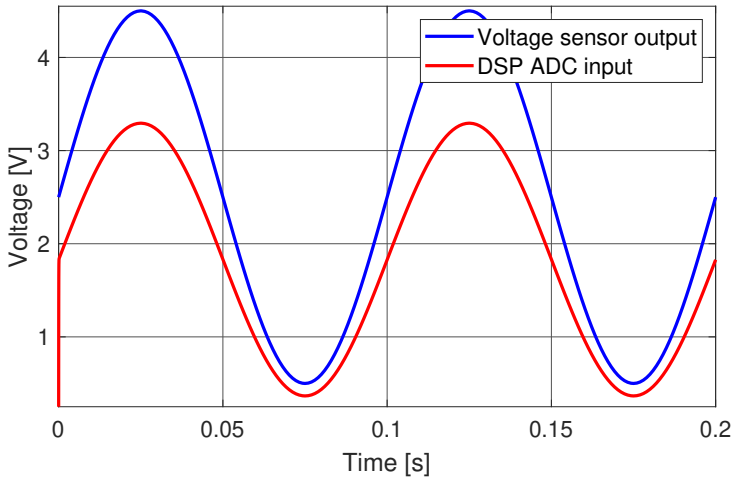


Figure 2.29: DC-link voltage signal processing circuit simulation result.

For the current measurement, the HAT 1000-S hall effect current transducer is considered, also from LEM [54] and shown in Fig. 2.30. Its measuring range covers from -1 kA to 1 kA, both DC and AC. Some of its features are presented below:

- $\pm$15 V power supply.
- $\pm$4 V voltage output (using a load resistor $\geq$10 kΩ).
- High isolation (5 kV).
- Low linearity error ($\leq \pm$1%) and thermal drift ($\pm$0.1%).
- Low power consumption.

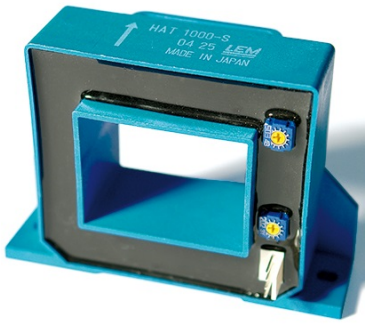


Figure 2.30: Sensor HAT 1000-S.

To adapt the current sensor output to the DSP input range, the circuit shown in Fig. 2.31 is implemented. A second-order passive low-pass filter with the same value as the voltage signal is added to the sensor output to filter possible disturbances. As seen, the current sensor has a

bipolar output (±4 V) which can not be directly inputted to the DSP. An offset of 4 V should be added to place the signal in the right range. This offset is achieved by adding a stable voltage reference obtained from the ZRT040GC1TA from Diodes Inc. [55] which is based on a Zener diode. After adding this offset, the signal is in the range 0-4 V. A double operational amplifier stage is used to first translate the signal to 0-5 V and, finally, from 0 to 3.3 V.

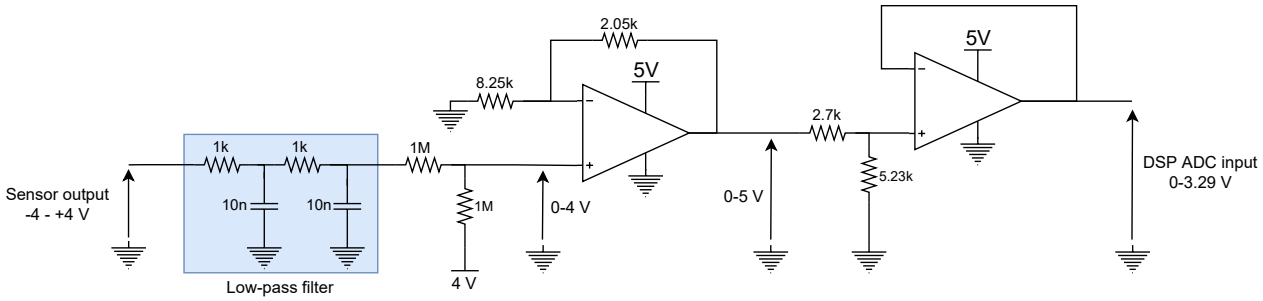


Figure 2.31: SM output current signal processing circuit.

In the same way, as for the voltage measurement circuit, a simulation has been conducted to validate the current signal measuring circuit design. The result is presented in Fig. 2.32.

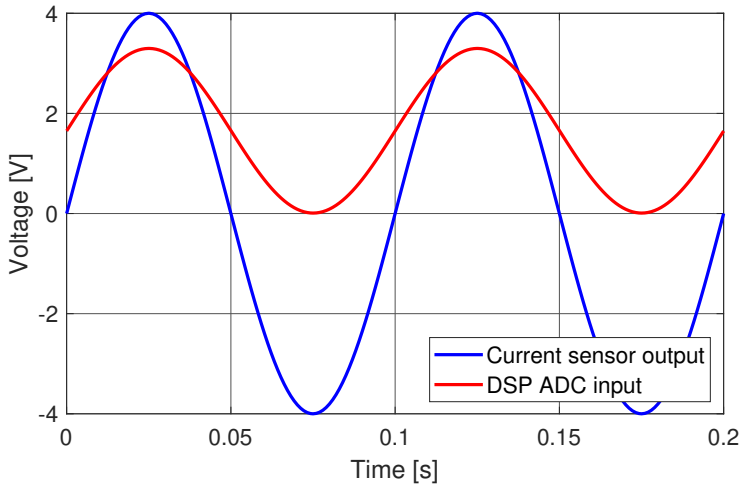


Figure 2.32: SM output current signal processing circuit simulation result.

Regarding the temperature measurement, a specific sensor is not chosen itself. However, there is an available built-in NTC thermistor in the power module, which can be used for temperature monitoring. It has a measuring range from 0 to 160°C, being 5 kΩ its resistance at ambient temperature (25°C). Its characteristic curve, given in the power module datasheet [18], is shown in Fig. 2.33. In this thesis, the maximum temperature to be measured by the electronic instrumentation circuit is fixed to 140°C, as the power module's junction temperature limit is 150°C. A Wheatstone bridge is implemented to convert the resistor value to a voltage representing the temperature. The Wheatstone bridge is a suitable circuit for measuring variable or unknown passive components using a reference voltage. The reference resistor value is chosen based on the curve given in Fig. 2.33, obtaining a bridge output voltage of 0 V for a resistor value of 200 Ω, corresponding to 140°C, and 4.7 V for a 5 kΩ which is translated into a temperature of 25°C. The output of the Wheatstone bridge is fed to a first OPA2354 in

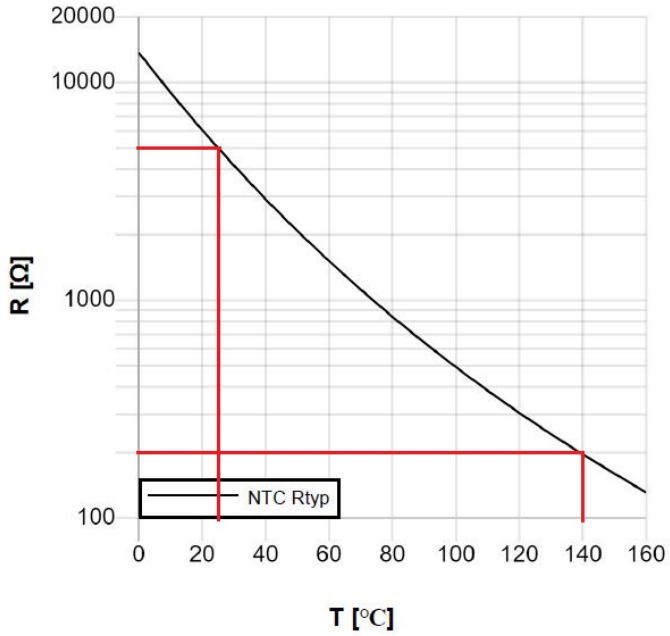


Figure 2.33: NTC characteristic curve [18].

a differential configuration with unity gain. A second operational amplifier stage scales the voltage down from 0-4.7 V to 0-3.3 V. The circuit implementation for temperature measuring is shown in Fig. 2.34. It should be highlighted that the circuit is implemented twice for each of the two IGBT modules forming the FB SM.

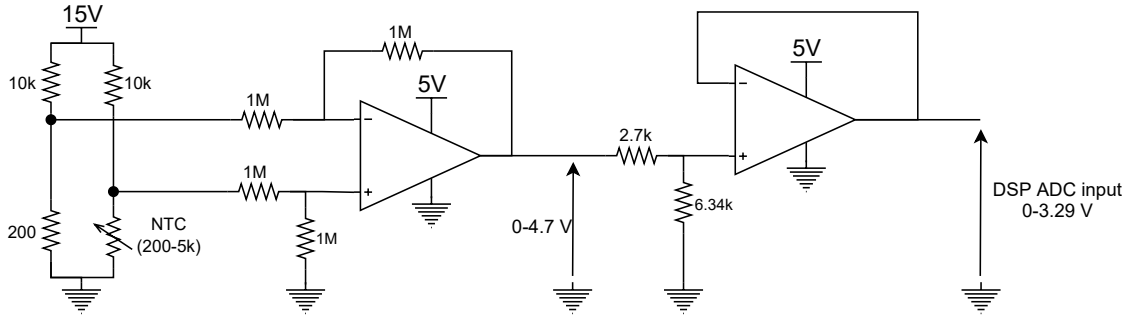


Figure 2.34: NTC thermistor signal processing circuit.

As previously done for the voltage and current signal processing circuits, a simulation is conducted to check the temperature measurement circuit. In this case, a variation from 25 to 140°C is emulated by varying a resistor from 5000 to 200 Ω. The simulation results can be seen in Fig. 2.35.

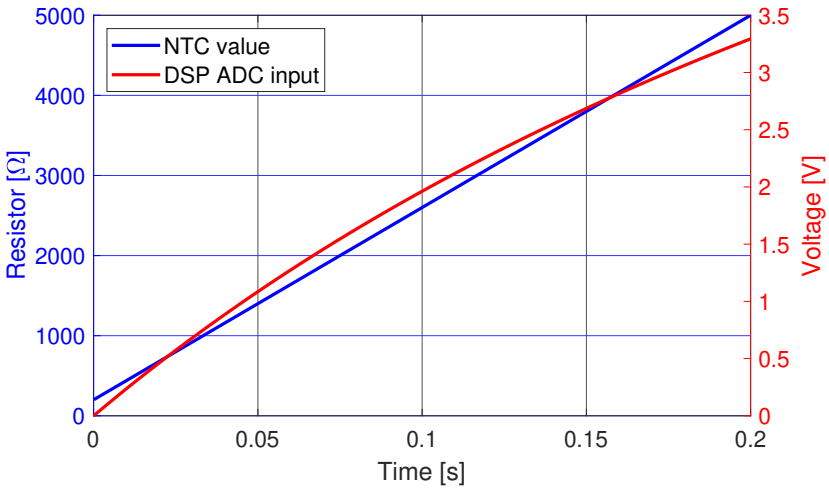


Figure 2.35: NTC thermistor signal processing circuit simulation result.

PCB Power Supply

The local power supply is needed to supply the DSP and all the auxiliary circuits in the control board. In an MMC application, where all the SMs are isolated from each other, the local control board needs to be supplied from the SM capacitor bank as it is the local reference voltage. Once more, as in the case of the gate driver, the voltage level of the SM DC-link capacitor is much higher than the acceptable supply level of the control PCB components. Therefore, firstly the voltage needs to be stepped down to an acceptable level, and secondly, isolation is crucial to protect the components and ensure the correct functioning of the control system. For this purpose, an isolated DC/DC converter needs to be designed. Possible topologies that could be used are the Flyback or Dual Active Bridge (DAB) converters, as both include a transformer that would provide the required galvanic isolation. However, the design effort required is much higher as the converter hardware needs to be sized and integrated, and suitable control is required to ensure that the desired DC voltage that supplies the control board is stable. An alternative to this option is finding a commercially available solution that can be used. Even though there are not many options that allow a high input voltage, some DC/DC converters can still be found. Some possibilities are the PVxx-29Bxx series from Mornsun [56] or JVA15 and JVA40 series from XP Power [57], [58]. Both options allow an input voltage of 200-1500 V, high isolation of 4000 VAC and different output voltages (5 to 24 V) and power (10, 15 and 40 W) versions. An estimation of the approximate power consumption of the different main components in the control PCB is listed in Table 2.14.

Table 2.14: Control PCB power consumption.

Component(s)	Consumption [W]
Gate drivers	15 (max.)
Voltage sensor	0.175
Current sensor	0.225
DSP controlCARD	0.25 (max.)
ICs (level shifters, op. amps. and logic components for protections)	0.5 (max.)
Total	16.2

From Table 2.14, it can be seen how the approximate power consumption of the control PCB slightly exceeds the 15 W. The only available option is, therefore, a 40 W DC/DC supply version. Regarding the required output voltage level, the choice can be done based on the different components' voltage requirements. These are summarised in Table 2.15.

Table 2.15: Control PCB supply voltages.

Component(s)	**Supply voltage [V]**
Level shifter (DSP side) Logic components for protections	3.3
Op. amps. DSP controlCARD Voltage sensor	5
Level shifter (gate driver side) Gate driver	15
Current sensor	$\pm$15

Based on the different voltage levels reflected in Table 2.15, it can be concluded that a voltage of 24 V can be reasonable for the DC/DC converter output. The other needed voltage levels can be obtained from these 24 V by using additional DC/DC converters or Low-DropOut (LDO) regulators. For this thesis, however, a different strategy is used to supply the control PCB. In a first iteration of the SM design, a 24 V external supply is used for simplicity, as described in the thesis limitations. However, to emulate the isolation of the SM as in a real application, individual isolated DC/DC converters are used to generate the different required voltage levels. Specifically, series TMR3, THN15 and THL25 from TRACO Power are used [59]–[61]. These power supplies are provided with both film and tantalum capacitor on their output to provide filtering properties.
Another remark related to the control board supply is the ground distribution. The PCB is designed with separate ground areas to avoid interference between the digital and analogue circuits. These ground areas are connected following the single-point grounding technique to lower the common impedance coupling between them [62]. This connection is accomplished by placing a 0 Ω resistor connecting both ground planes, as illustrated in Fig. 2.36, where the isolation from the DC/DC converters is also highlighted.

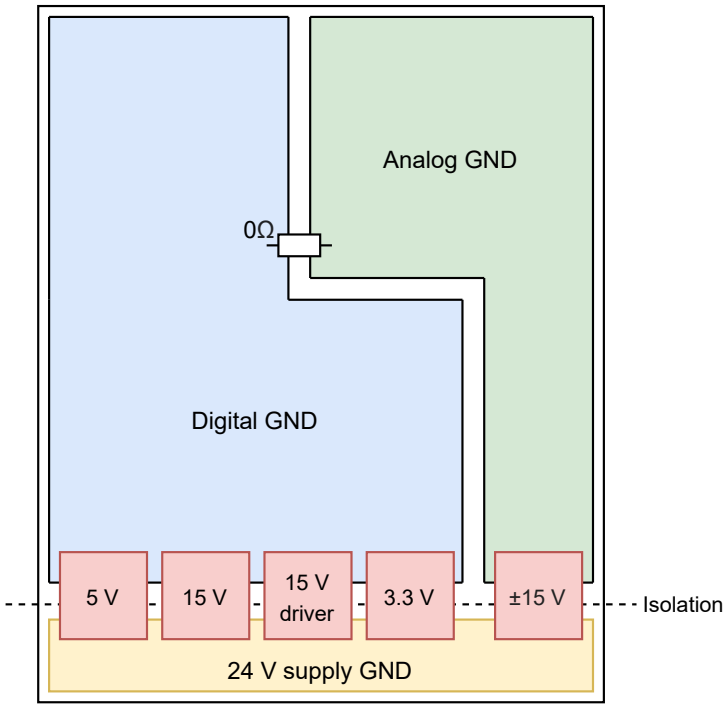


Figure 2.36: Ground distribution in the control PCB.

Protection

The SM protection is implemented to guarantee an operation under safe conditions, protecting the SM power hardware components against fatal consequences, and, if needed, trip the whole converter to protect other SMs as well as different elements connected to the grid emulator system. The most typical faults that can be encountered at the SM level are: short-circuit of the IGBTs, over-voltage of the DC-link, over-current through the SM and excessive temperature that can damage the IGBTs. Additionally, there can be other faults that are not directly related to the power hardware operation like under-voltage of the auxiliary power supplies, failed or lost communication to the top-level control unit or DSP malfunctioning, among others. These faults can be managed in multiple ways but what is crucial is detecting them as fast as possible. To achieve this, the fault detection mechanisms implemented in this thesis are summarised in Fig. 2.37. As it can be seen, both hardware and software protections are combined. This combination allows better performance, as these compensate each other limitations and have redundancy if any of them fails. The figure also specifies the different thresholds allowed for the SM, being 1350 V for the DC-link voltage, 550 A for the circulating current and around 100°C for the IGBT temperature given a margin from baseplate-to-junction of 50 °C where at nominal operation the maximum difference was found to be 21 °C from junction to baseplate in (2.4). In the following lines, the different protection measures are described in further detail.

The hardware protections are implemented as these provide a fast response against fault situations. Robustness is also an appealing feature of hardware protections, as these can operate standalone, ensuring that the SM switching is stopped even if the DSP experiments malfunctioning issues due to noise or other interference. This protection is achieved by employing logic circuits. As mentioned earlier, the gate driver includes its protection against supply under-voltage and short-circuit cases, which do not need to be considered on the control

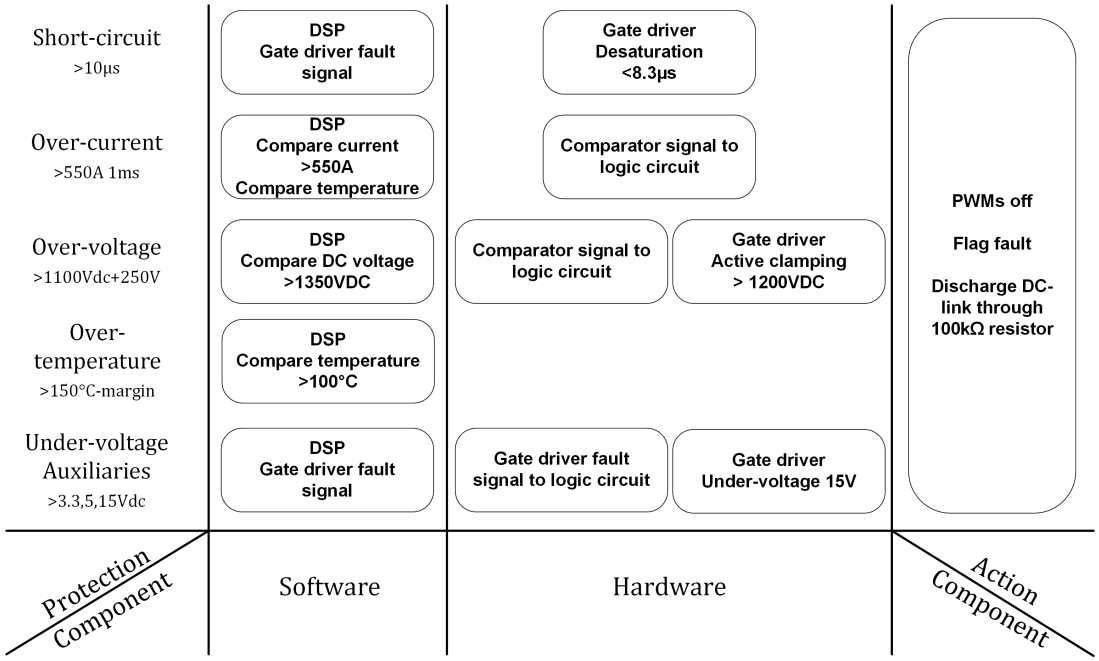


Figure 2.37: SM protections overview.

board; however, these are still routed for fault detection. Besides its fault processing, each gate driver sends two digital fault signals that the hardware protection can use. Additionally, the over-voltage and over-current protections are implemented hardware-wise, considering both positive and negative maximum current cases as the SM current will be AC. A comparator circuit is used to digitalise the analogue signals. The comparator used is the LM339 from Texas Instruments [63] and it compares the analogue signals for the DC-link voltage and the SM current, in the 3.3V-voltage range, with the corresponding reference values that match the allowed limits (1350 V and $\pm$550 A). The comparator output is '1' while there is no fault and '0' when an over-voltage or over-current happens to keep the same logic as the implemented in the gate drivers. Using this logic will also protect the circuit in case of failure on any power supply leaving a '0'. The comparator outputs are fed together with the four-fault signals from the gate driver to a D-type latch, which is used to hold the fault signals' values. The selected D-latch is the CD54HC373 from Texas Instruments [64]. The D latch outputs are connected to a main AND gate that generates a unique fault signal when any input presents a '0' value. Again, the same logic is kept in this case, where a '0' output indicates that a fault has occurred. This fault signal is fed back to the DSP to acknowledge that the hardware protection circuit has detected a fault and stop its operation if necessary. The chosen 8-input AND gate is CD4068B from Texas Instruments [65]. Finally, the output signal from the main AND gate is connected to four separate AND gates together with the individual PWM signals for each of the four IGBTs. As a result, the PWM signals are blocked first by the logic circuit in case the DSP does not react faster enough to the fault. The selected AND gate is SN74AC08 from Texas Instruments [66]. It is a quadruple two-input AND gate which allows handling the four PWM signals with the same IC. The schematic of this implementation is illustrated in Fig. 2.38.

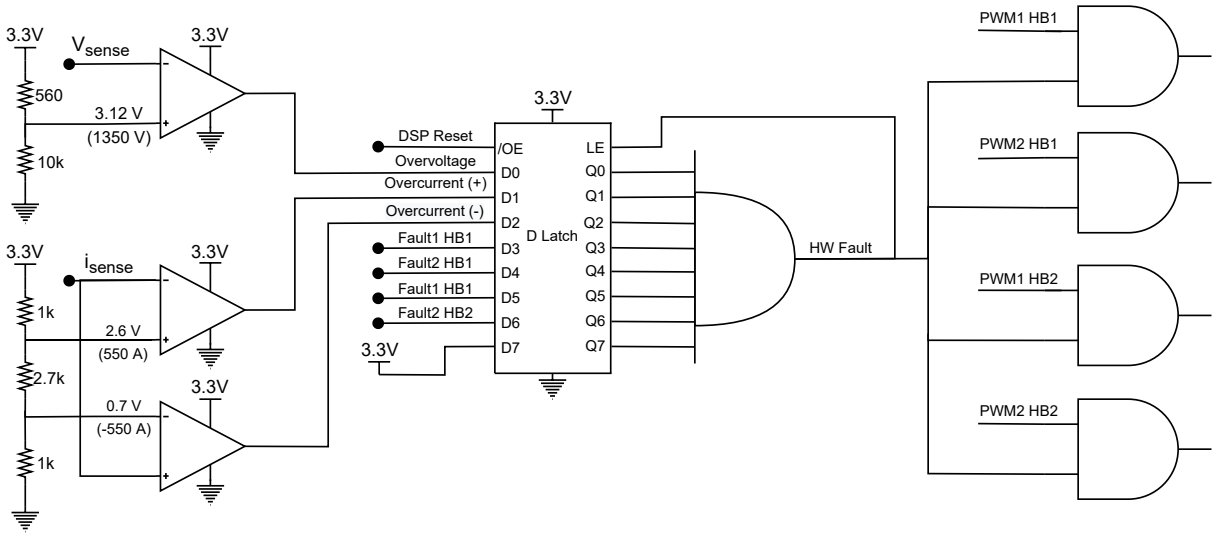


Figure 2.38: Hardware protection circuit.

Complementing the hardware protections, the DSP also monitors the different signals to ensure that these have the correct logic value for the digital signals and are within the allowed boundaries for the analogue ones. Typically, the DSP is slower than the hardware protection; however, it can ensure that the SM operation is safely stopped after detecting the fault. Additionally, it can also inform the top-level controller via communication and notice the converter user through an interface or other indicators.

Communication

The last block from Fig. 2.24 to be discussed is the communication interface. This feature plays an important role in the SM integrability in a MMC application, connecting each SM with the unit in charge of the top-level control. The communication strategy is a delicate aspect for MMC as typically a large number of elements are involved, and the time delays related to the communication, added to the ones corresponding to the control loops, can affect the maximum allowed control bandwidth. Different communication strategies have been studied in literature due to their impact on the converter performance [67]–[69]; however, as it was mentioned in the DSP section, a new communication protocol, Fast Serial Interface (FSI), developed by Texas Instruments for their new DSP generations is proposed, and its feasibility is evaluated.

FSI is a serial communication peripheral block suitable for reliable and isolated high-speed communications, with a transmission rate of up to 200 Mbps. FSI is designed for systems that must exchange information through isolation devices due to the converter nature. These isolation barriers typically introduce an additional time delay, but FSI ensures the communication is performed without adding a significant delay. Further investigation on the delay is studied in Appendix A.

Alternatively to FSI, an interface to an EtherCAT transceiver is also included in the control PCB design. EtherCAT is a well-known and widely-used industrial communication protocol that can reach transmission rates from 0.1 to 10 Gbps. It has been the focus of several research papers when applied to MMC applications [69]–[71]. The considered transceiver is the FB1111-014x from Beckhoff [72]. An electrical interface for both protocols is included on the control PCB to have the ability to verify the protocols considering the aspect of control delay.

After listing all the individual PCB features and choice of different components needed, all of them are integrated as part of the control board, which is designed using the software Altium Designer. A 3D sketch of the first version of the board can be seen in Fig. 2.39 which primary components are listed below.

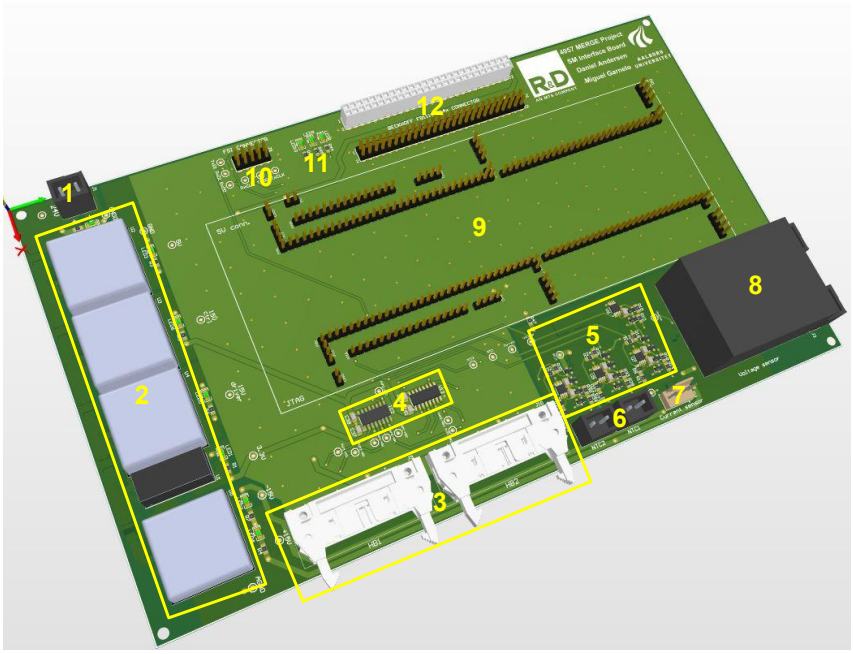


Figure 2.39: 3D model of the first control PCB version.

1. 24 V supply connector.
2. Switch-mode DC-DC power supplies.
3. Gate driver connectors.
4. Level shifters.
5. Signal processing circuit (Op-amps, filter and gain resistors).
6. NTC connectors.
7. Current sensor connector.
8. DVC 1000-P voltage sensor.
9. DSP docking station socket.
10. FSI communication interface.
11. LEDs for debugging purposes.
12. FB1111-014x EtherCAT board interface.

2.5 Control and Coding Implementation

In the final stage of the design, some software structure is implemented to the SM controller. In the final SM controller, a control strategy will be implemented for MMC operation. However, in this initial implementation, the focus is on establishing a fixed framework for initialising the SM, first to conduct the test which is investigated in Chapter 3 but later should create a basic framework for the MMC control implementation and SM start-up. Software implementation is made using a state machine methodology to ensure that specific tasks are executed within a specific state. The state machine is shown in Fig. 2.40.

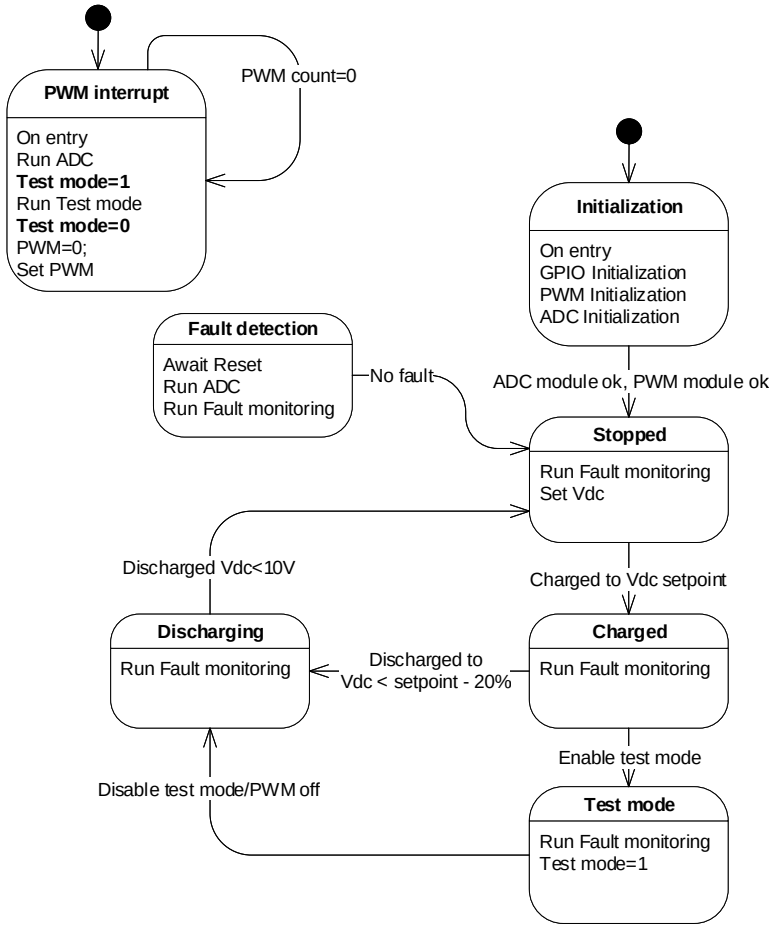


Figure 2.40: State machine.

The state diagram shows two state machines: the main state machine involving all the functional states and an interrupt state. These are shown as two states as these run at different speeds. The main state machine is running at run-time, while the PWM interrupt state is based on the PWM switching frequency of 500 Hz, required for the SM. Firstly, the main state machine is explained.

The main state machine is initialised at controller power-up. In the first initialisation state, the controller is initialised by setting up various functionalities for PWM, ADC, I/O pins

which are set to initial values to ensure safe start-up. After the initialisation, the SM is placed in stop mode from where it reads ADC values (using PWM interrupt) for monitoring and surveillance of faults on both digital (gate drivers, hardware protection) and the analogue inputs (voltage, current and temperature). In stop mode, an initial DC-link voltage can be set. The stopped state awaits charging of the DC-link capacitor-bank as this happens externally both for the initial test but also the final SM which is charged for its DC-link by the main converter supply. When charged to the setup point, it moves to the charged state, where it again waits similarly to the stop state to enable a test mode. If the DC-link is discharged below 20% of its set point before a test is initialised, it goes to discharging state and awaits discharge of the SM. The test mode state is initially thought of as a run state for controlling the SM. However, as the thesis focuses on the first iteration prototype, it is used to execute a specific open-loop test of the SM, hence calculating PWM compare values from manual references. The open-loop test modes are future developed in Chapter 3. The test mode state is the only state that can initialise PWM output. After stopping a test, the discharging state is started where the SM awaits discharge of the DC-link. After which, it circulates back to the stopped state, in which state it is also safe to switch off the SM. Finally, in all states, a fault monitoring is done, which checks all the sensor and digital inputs as explained in Section 2.4 and the fault signalling from the hardware protection. If any fault is detected, the SM is in the fault state. Here, it awaits reset before it again checks for faults before leaving the fault state.

The PWM interrupt state machine is used to read ADC input, calculate new compare values and set the new PWM values to the PWM register at the entry of the state. After that, it

Main
Void InitPWM(void) Void SetPWM(float PWM1a,float PWM1b,float PWM2a,float PWM2b) Void InitFault_monitoring(void) Void Fault_monitoring(void) Void GPIO_config(void) Void ADC_config(void) Void ADC_read(void) Void Test_mode_init(void) Void Test_mode_run(void) interrupt void pwm_isr(void)

Uint16 State;
Uint16 Entry_exit;
Bool Test mode;
PWM_count 50000
bool PWM_set = 0;
float PWM[4]={0};
float PWM_old[4]={0};
bool trip=0;
bool Reset=0;
Uint16 Fault_type=0;
Uint16 adcResult0;
Uint16 adcResult1;
Uint16 adcResult2;
Uint16 adcResult3;
float DC_link_voltage=0;
float arm_current=0;
float NTC_temp1=0;
float NTC_temp2=0;
float t1=0;
float V1=0;
float V2=0;
float angle=2;
float amplitude=0.5;

Figure 2.41: UML diagram.

awaits a new zero PWM count. This interrupt is linked to the PWM channel 1 and ensures that all new PWM values are initialised synchronously. Further, by reading before the switching event of the two channels, it is possible to avoid inaccurate measurements due to noise during the switching event.

All code for the state machines are implemented as functions to call from all states. These corresponding variables can be seen in the Unified Modeling Language (UML) diagram in Fig. 2.41. The state machines are implemented as a switch-case in traditional C code which is allowed by the Texas DSP as described in Section 2.4.2.

Timing diagram

The state machine is, as mentioned, divided into two parts, one running in the run-time of the program while one is synchronised to the PWM switching frequency using the PWM interrupt. Normally, all code could be done in the PWM interrupt; however, due to the low switching frequency of 500 Hz the task of fault detection is still left for run time. However, sampling of new data, calculation of new PWM set points and setting the PWM values are left for the PWM interrupt. When updating the PWM registers, a dead-time of 1.4μs is added to avoid short-circuit of the IGBTs in the same leg, which is derived from the maximum turn-on and turn-off time of the IGBT with a small margin. Due to the low switching frequency, the main protection is laid upon the hardware protection as it checks for faults continuously. However, the controller controls the reset and blocks the faults until a software reset is made.

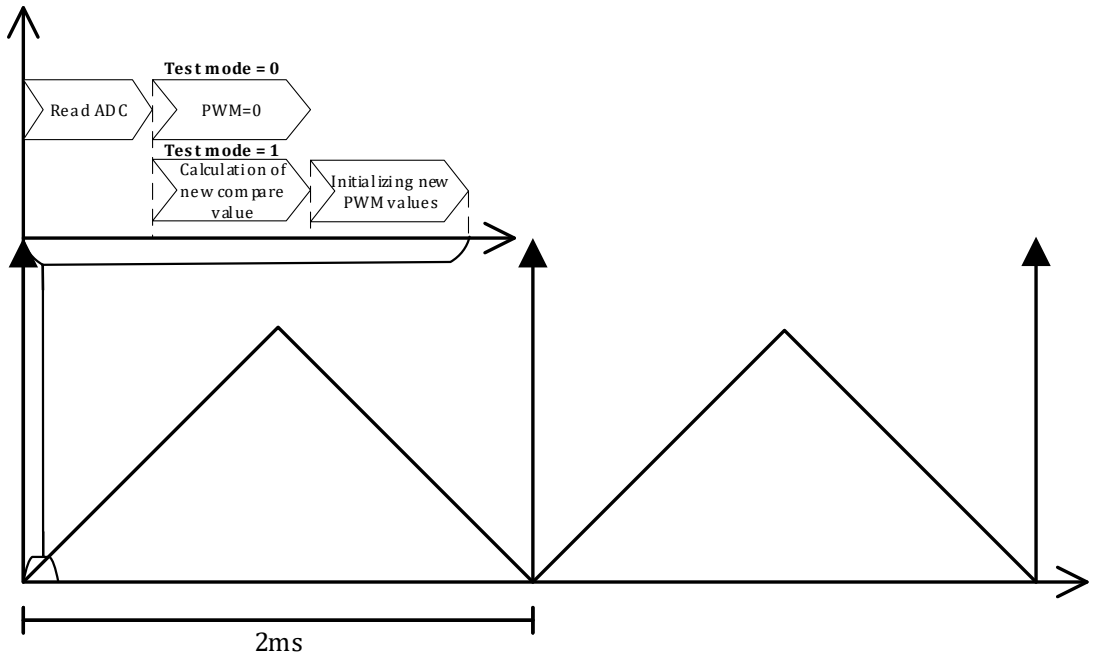


Figure 2.42: Timing diagram of PWM interrupt.

2.6 Manufacturing and Assembly

Once all the individual components that form the SM are sized, chosen and designed, the next step is assembling all of them to obtain a first MMC SM prototype. The objective is obtaining a SM as compact as possible, for which assembly could be problematic, as earlier highlighted. For this purpose, a detailed assembly plan is developed, which is illustrated in the flowchart in Fig. 2.43.

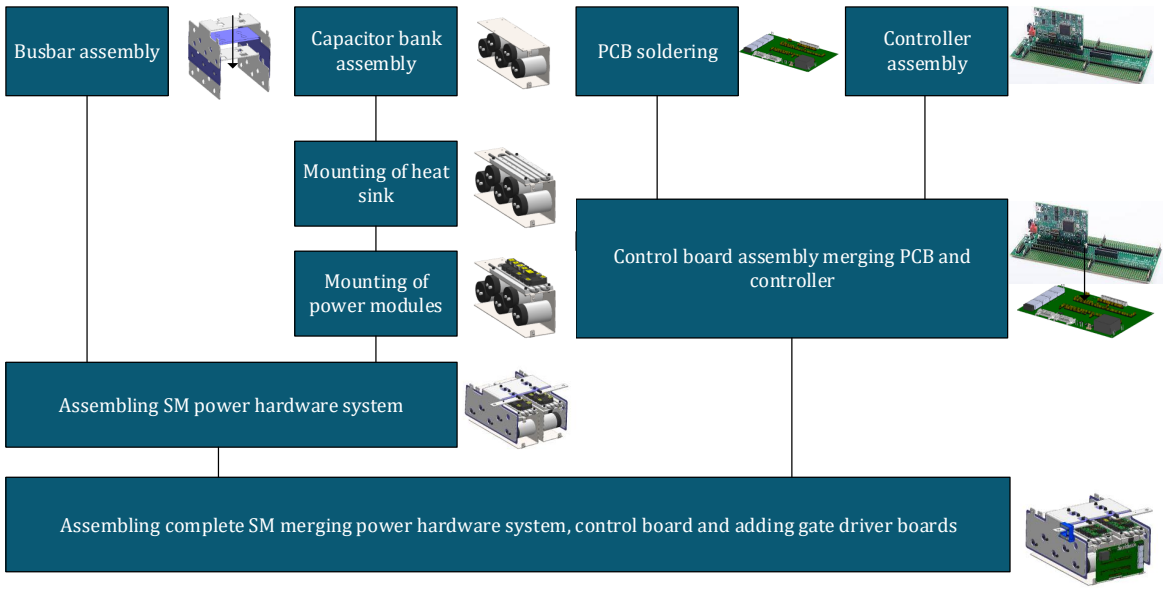


Figure 2.43: Flowchart of assembly process for the first iteration SM.

From Fig. 2.43, it can be seen how the SM assembly process follows two clear streams: one for the power hardware and the other related to the control hardware. Finally, both parts are merged in the final SM.

The first step is assembling the busbar by placing the positive and negative aluminium plates and the mylar sheets together. The pieces are glued together using silicon glue to ensure a solid and robust joint. The chosen glue is the 732 from Dow Corning, which has good dielectric properties. The busbar-glueing and -assembly process is shown in Fig. 2.44.

Figure 2.44: Busbar assembly process.

The next step is arranging the capacitor bank that forms the DC-link capacitor. As mentioned in Section 2.2, the total capacitance of 4 mF is considered, which is achieved by using ten 400 μF capacitors in parallel. The capacitors are divided into two groups of five and mounted in their corresponding stands, as seen in Fig. 2.45. By doing so, the capacitors are distributed and fixed, making it easier to fasten them to the U-shape busbar.

Figure 2.45: Capacitor bank assembly process.

Once the capacitors are mounted, the water-cooled heat sink is placed over the stand and fastened. Previously, the necessary holes are drilled in the cold plate to mount the IGBT power module over it. After this, the power module is affixed on the cold plate by using bolts. Before, a non-silicone thermal grease from Boyd Corporation[73] is applied in the power module base plate to provide good thermal contact and favour the heat dissipation. The bolt's tightening sequence is made following [74] in order to ensure proper distribution of the thermal grease. Finally, all the power hardware elements are merged, which is achieved by fastening the IGBT module collector and emitter terminals to the positive and negative busbar plates, respectively. Each terminal of the capacitor is also fixed to the corresponding plate. Additionally, two small plates are connected to the middle points of each HB, defining the SM output terminals.

Besides the power hardware, the control hardware has its assembly process. From the PCB design made in Altium, the PCB is manufactured. All the components are soldered in their corresponding locations, as can be seen in Fig. 2.46.

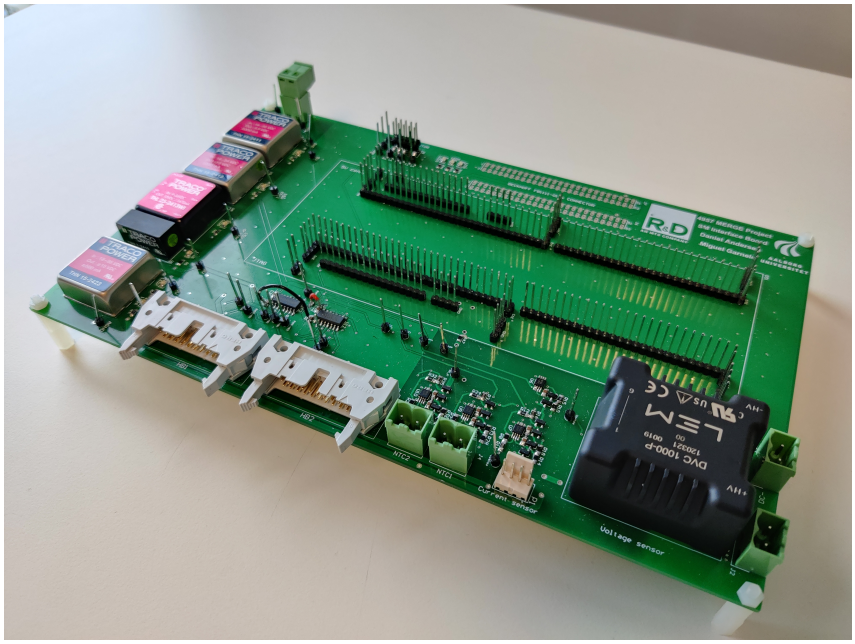


Figure 2.46: PCB with components.

The controlCARD is plugged into the docking station. After that, the assembly is mounted on the control PCB. Jumpers and cables are used to make all the internal connections in the PCB to the DSP pins. The final result is shown in Fig. 2.47.

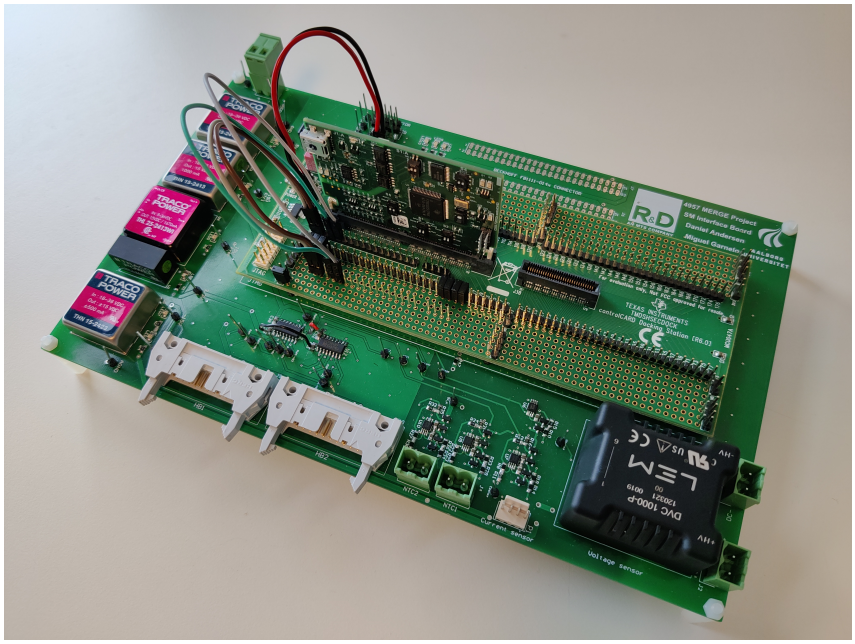


Figure 2.47: PCB with components and DSP.

Finally, the PCB is fastened on one side of the SM structure. At the same time, the 2SP0320T2C0-17 plug & play gate driver is fastened to the gate terminals in the power module. In the end, the gate drivers are connected to the control PCB through cables, as well as the different sensors inputs. The voltage sensor terminals are wired to each of the busbar plates. The current sensor, which is mounted on one of the SM output plates, is also connected through a four-wire cable to the PCB. Similarly, each of the NTC thermistors is routed to the control board. The last part to be connected is the external 24 V power supply that supplies the PCB. The assembled SM is shown in Fig. 2.48.

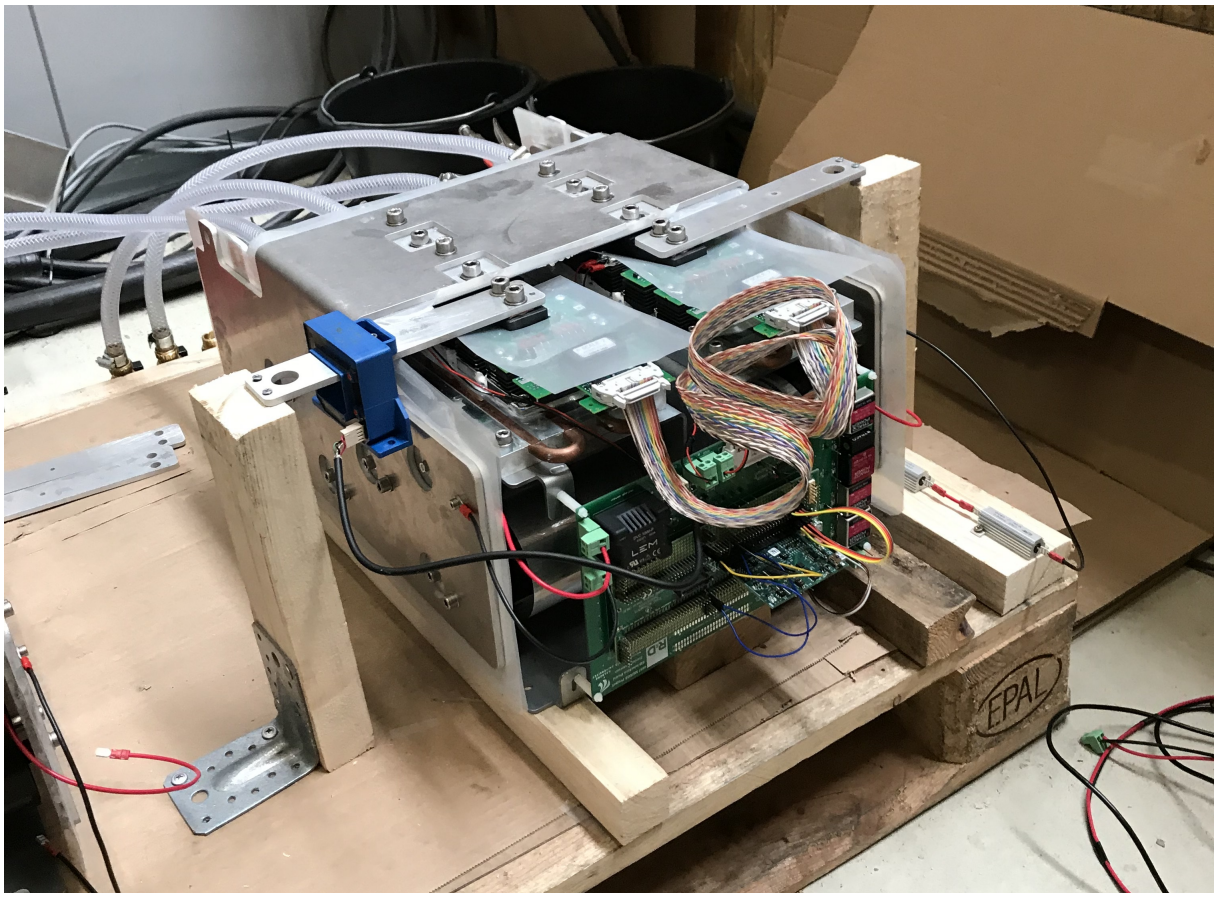


Figure 2.48: Final SM assembly.

2.7 Commissioning

In the commissioning phase, the design of the SM is tested before complete assembly. This is done to ensure that all sub-systems are working correctly before complete assembly and to reduce the risk of failure for some components, as it was originally found in the DFMEA in Section 2.2.1. These test, therefore, cover the component and system integration test needed to verify the SM internal system, while the complete SM is considered in Chapter 3. As it is presented in Fig. 2.2 in the methodology section, this process is iteratively done while assembling the SM. The flowchart from the assembling section is therefore updated with the various test campaigns which should be considered in the individual phases are seen in Fig. 2.49.

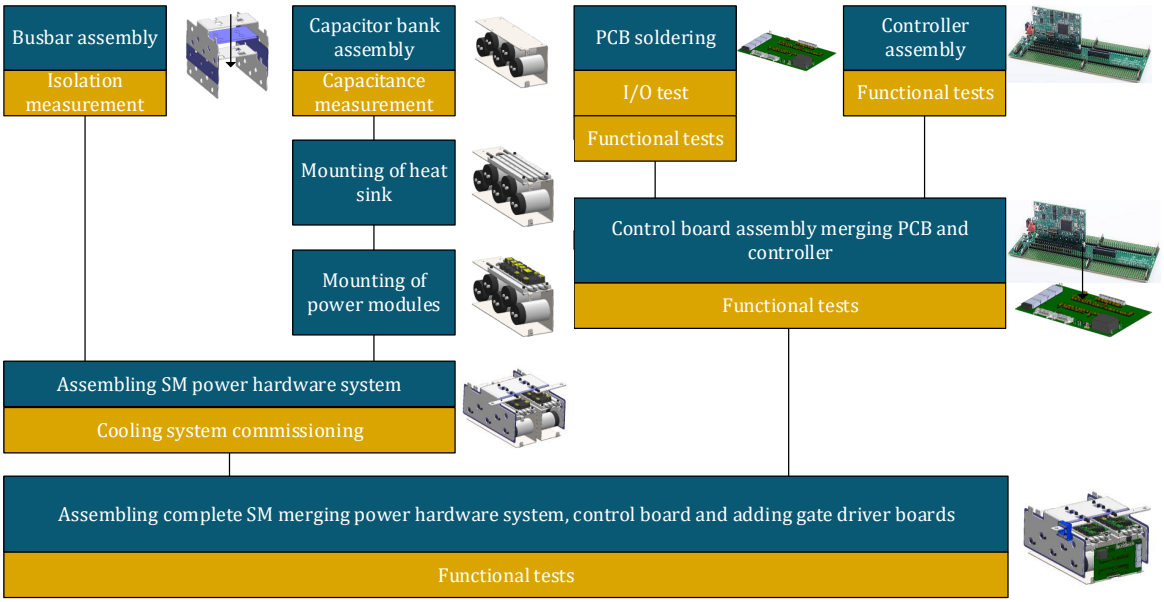


Figure 2.49: Flowchart of assembly process with added commissioning tasks for the first iteration SM.

Starting in the first column of assembly, the busbar assembly is tested using a high voltage isolation tester. The leakage current is observed through its parasitic resistance by applying a high DC voltage to the positive and negative busbar poles. This test is conducted at a DC voltage, and the capacitance value is therefore not evaluated. However, any scratch making penetration of the insulation material during the mechanical assembly would be detected, which justifies this type of test. For the capacitor bank assembly, the capacitance is measured on the individual capacitors. Further, the final capacitance of the SM is then measured at the end of this assembly. This test is done using an LCR meter. After assembling the SM power hardware, the cooling connections are also tested before merging it with the control hardware part. Considering the control hardware, the PCB is I/O tested to ensure that all connections are intact and no short-circuit is made. Then, all the components are functionally tested to ensure these are functioning correctly. The supplies and ICs are tested using external function generators, the offset of current and voltage sensors is measured by connecting their input to 0 A and 0 V, and the controller is also tested for the implemented functionalities using function generators and oscilloscopes before assembly with the control PCB. The controller test includes measuring the computational time required by the DSP to execute the open-loop control. After merging the PCB and controller, these are again tested for their functionalities. The DSP ADC bit loss is quantified both before and after connecting it to the control PCB. Finally, after adding the control board to the SM assembly, functional tests of high voltage and current sensors are verified using high voltage power supply and current. The complete list of commissioning test is summarized in Table 2.16.

Table 2.16: SM commissioning test.

Component/assembly	Test	Acceptance
DC-link busbars assembly	Isolation measurement	>500MΩ
DC capacitors	LCR meter measurement	400uF +/-10%
DC capacitor bank (10 psc)	LCR meter measurement	4mF +/-10%
PCB	I/O test	<1mΩ
PCB	Functional test	
	• Power supplies	Ok
	• Voltage references	Ok
	• Op-amps circuitry	Ok
	• Voltage level shifters	Ok
	• Sensor input (without high voltage and current sensors)	Ok
DSP	Functional test	
	• PWM strategy (frequency, deadtime, etc.)	Ok
	• ADC	Ok
	• Fault conditions	Ok
Control board (PCB+DSP)	Functional test	
	• PWM output	Ok
	• ADC input	Ok
	• Auxiliary LEDs	Ok
	• Fault signals by emulation of gate driver, over-voltage, over-current, temperature	Ok
Submodule complete assembly	Functional test with 0V DC on DC-link	
	• PWM including gate driver boards and PM at 0 V DC	Ok

	• ADC including sensors
	  • Voltage sensor at 0-1000V
	  • Current sensor at 0-10A
		Ok

Chapter 3

Test Description

This chapter describes the tests which are conducted on the SM to test and verify the complete design. The tests are found considering the full SM from the stage where all commissioning tests mentioned in the former chapter are finalised. Therefore, the tests in this chapter are considered to be prototype test to verify the first iteration prototype considered in this thesis. The tests are conducted on a single SM and do not verify MMC operation and control of the SM.

3.1 Test Methodology

This section presents the test methodology used in this thesis to verify the SM design. The test considered in this part covers the acceptance test of the full SM concerning the requirements, in contrast to the commissioning test, which covers the component and system integration test. The tests ensure that interfaces can operate as specified within the worst-case conditions considering the electrical ratings in Table 2.1 and that the full assembled SM can withstand it. These tests are done at SM level and not full MMC level, as a test on full level is not considered to give more information of the withstand levels for the design and is more relevant for control strategy and communication investigations. The derived tests are shown in Fig. 3.1.

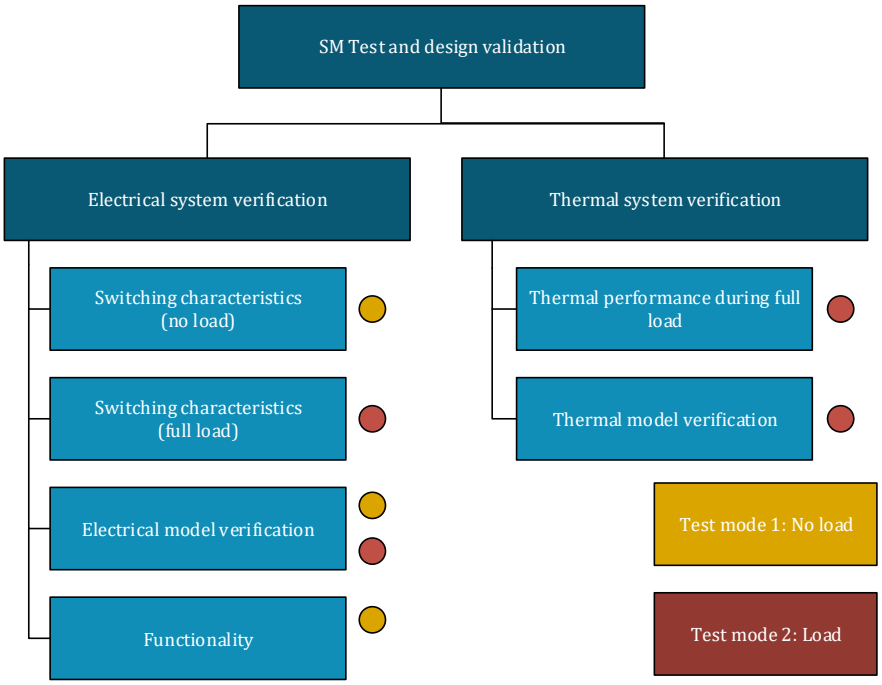


Figure 3.1: Test overview for testing SM operation.

The derived tests are found based on two categories, electrical and thermal verification, described independently.

The electrical verification is added to test and verifies the turn-on and turn-off behaviour of the SM, considering the electrical parasitics of both the parts developed in this thesis and the components such as the power module. The idea is to verify the behaviour and determine if it is acceptable. This verification is conducted both during no-load and load conditions to see the effect of temperature dependencies and load current. Further, the electrical model developed for verifying the behaviour in simulation should be compared to verify the model for its use in future electrical verification for full MMC simulations.
The thermal verification category is added to verify the chosen cooling system to ensure that the maximum temperature of the SM stays within limits. This is done at various operation conditions to create a clear mapping of the safe operating area. Similar to the electrical simulations, the thermal model should be compared to the measurement to verify its accuracy for later full MMC simulations.
In general, the verification of simulation models is important for future work as prototypes of full converter level is expensive.
All tests are divided into two test campaigns: a no-load test (test mode 1) and a load test (test mode 2). In these two, tests are made to obtain the data for the various measurements iteratively, which are marked by the yellow and red colour in Fig. 3.1. As mentioned in the thesis limitations, all tests are conducted as an open-loop test, as the safe operation area of the SM is not yet established. For the two test campaigns, the necessary test setup and investigations are presented in the following sections.

3.2 Test setup

To conduct the test mode 1 and test mode 2, a test setup needs to be developed. As mentioned, a single SM test is used for the verification and the proposed test setup is seen in Fig. 3.2.

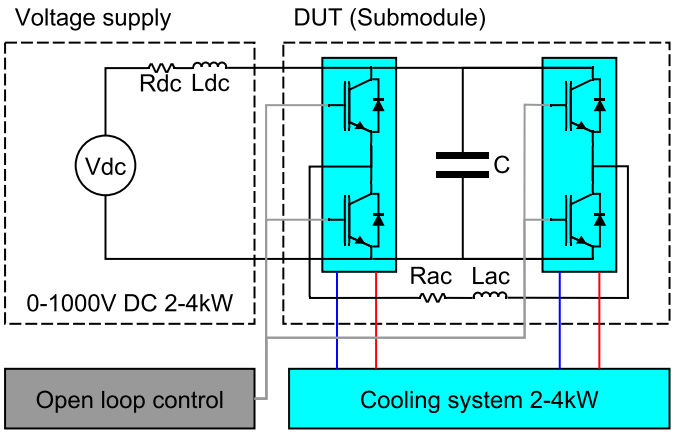


Figure 3.2: Test setup - top level.

First of all, as no active load is available for the load test, reactive power is circulated from one half-bridge to another to emulate the current operation. For this test, a load inductance is

needed which can withstand the full load current. The load inductance value needs to be low enough to allow current flow within the voltage operation range and, similarly, large enough not to surpass the operation range. The choice of load inductance is further investigated in Section 3.2.1. Besides the load inductance, a voltage supply and cooling system are needed as auxiliary systems. The voltage supply should supply the DC-link voltage during the test, within the testing range, while supplying the losses. An auxiliary cooling system needs to be included as well to dissipate the SM losses from the power modules during operation. The auxiliary cooling system needs to supply a water flow at a controllable ambient temperature and have a heat exchanger large enough to dissipate the power. It should preferably have the flexibility to change both flow and ambient temperatures to emulate various working points. These auxiliary systems are further discussed in Section 3.2.2.

3.2.1 Open-loop load mapping

In this thesis, an open-loop control strategy approach is used in the test mode state, described in Section 2.5. The reason for open-loop control at this point is that the hardware is not yet verified and, before full protection is ensured, closed-loop should not be used. The open-loop strategy is presented in Fig. 3.3.

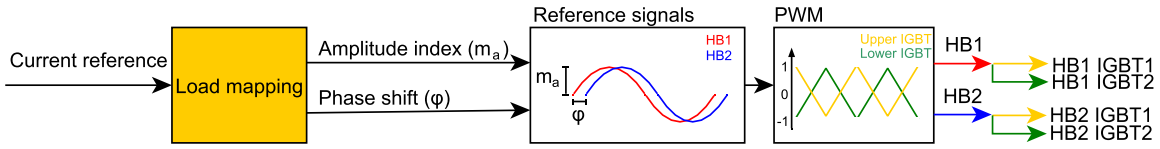


Figure 3.3: Open-loop control strategy.

For the test of the SM, a requirement is to set the current to specific set points. This current reference is fed to a load mapping which gives a specific amplitude index and phase shift. From these parameters, reference signals can be formed for the SM's two HBs, which are compared to two PWM carrier signals. One carrier signal forms the PWM signals for the left IGBTs while the other forms the PWM signals for the right IGBTs in the FB. In order to achieve this kind of control, it is important to know the response from the specific load as the reference is manually set. In this thesis, a load inductance is coupled to the SM output in order to emulate a load. By using an inductor, the current can be circulated using mainly reactive power. Therefore, the next step is to find an inductance that is valid for the needed operation point up to full nominal load current. Next, the load inductance value and its influence on the SM test is analysed. The inductance value plays an important role as it controls the output current rise time during the open-loop tests. As mentioned, the SM is tested by circulating reactive power between the two HBs forming the SM, and this is achieved by introducing a phase shift between the reference signals used for the modulation of each HB, as seen in Fig. 3.3. This technique creates a PWM output voltage that enables the desired load current waveform depending on the duty cycle and inductance value. The minimum duty cycle needs to be known to find the inductance value. The chosen power module determines its limitation for the SM as the minimum duty cycle pulse width is equal to the IGBT turn-on time. The reason for this is that the output voltage pulses are obtained from the difference between the two HB PWM patterns leading to that the smallest pulse width allowed needs to be larger or equal

to the IGBT turn-on time to guarantee that both switches are fully ON. If this requirement is not fulfilled, the IGBT turn-on would not fully happen, and the PWM pulses would not reach the nominal DC-link voltage before it is turned off again by the opposite HB. If a sinusoidal current is of interest, as it is in this case, this would first lead to a more distorted current as the current rise does not reach the slope needed to recreate the desired fundamental frequency waveform. Later if the duty cycle width is further decreased, the current will decrease until it finally disappears. Therefore, it is important that the inductance value is not too low as it would lead to an over-current. It should further be noted that the current is already distorted due to the low switching frequency (500 Hz) of a single SM. However, this would be removed in a real MMC with the right amount of SMs in the arm, creating a smoother output current waveform due to the common switching frequency of all SMs.

The output current is analysed for different load inductance values considering this criterion. The study is done for the minimum output voltage pulse width for each inductance value and obtaining the current response. This analysis, thereby, shows the minimum output current reached with each inductance value within the criterion. As higher pulse widths are always possible, and higher currents can therefore always be reached within the non-saturated area of the inductance. A simulation is done for obtaining a 50 Hz current waveform having a reference waveform amplitude for the modulation of 0.025 and a phase shift between the HBs references of 30°which creates the minimum possible duty cycle. The result of this investigation is shown in Fig. 3.4 with the current response in per unit for various DC-link voltages and their linear increased base values.

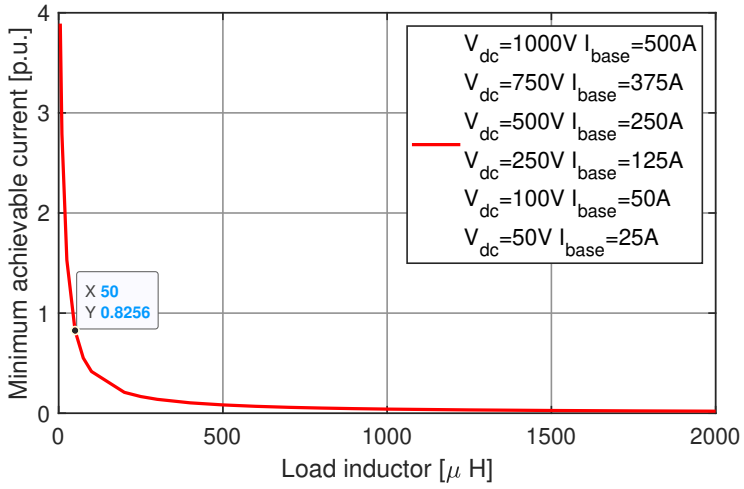


Figure 3.4: Minimum achievable current depending on inductance size considering the SM's power modules turn-on time as minimum duty cycle width.

The figure shows a wide range of possibilities for the load inductance values which could be chosen. It can be seen how the larger the inductance value is, the lower the load current values can be achieved. Therefore, the value should be selected depending on the load conditions that are required for the SM test. However, commercial inductors in the 500 A range are not available for high inductance values due to the high current leading to thick windings. For this thesis, a three-phase reactor is available in the laboratory, which properties are summarised in Table 3.1.

Table 3.1: Load inductor parameters.

Parameter	Value
Inductance (single-phase)	27 μH
Winding resistance	126 $\mu\Omega$
Nominal voltage	690 V
Current	4086 A
Frequency	50/60 Hz
Weight	725 kg

As it can be seen, the inductance value for a single-coil is 27 μH, which lies in the left part of the x-axis in Fig. 3.4. Two of the coils are coupled in series to obtain a higher inductance value to achieve a wider current range, 54 μH in this case. This coupling is done such that the inductors are not magnetically short-circuited, leading only to the leakage inductance, hence not cancelling out mutually coupled magnetic fields. This coupling leads to a higher field density which could lead to saturation. However, as the inductor is rated for 4086 A, its knee point would not be reached, as the maximum rated current is set to 500 A. The three-phase inductor and the series-connection can be seen in Fig. 3.5.

(a) Load inductor series-connection.

(b) LCR meter measurement of the load inductor after series-connection.

Figure 3.5: Load inductor.

This inductance value is used in the experimental part of this thesis which is presented in Section 3.3. The inductance value, highlighted in Fig. 3.4, is corresponding to a current peak of 0.83 p.u., which, for a 1000 V DC-link voltage, is translated into 400 A approximately. A simulation of these test conditions is conducted, and its results are presented in Fig. 3.6. The figure shows the SM output current at 1000 V DC-link voltage. It can be seen how the peak value matches the expected 400 A. The minimum PWM pulse width is also highlighted, which is slightly larger than 650 ns and, therefore, fulfils the imposed criteria. It should be noted at this point that the current shown is, in reality, high for this inductance value. This effect is therefore studied next.

To validate the SM design, various load conditions need to be tested to have a clear picture of

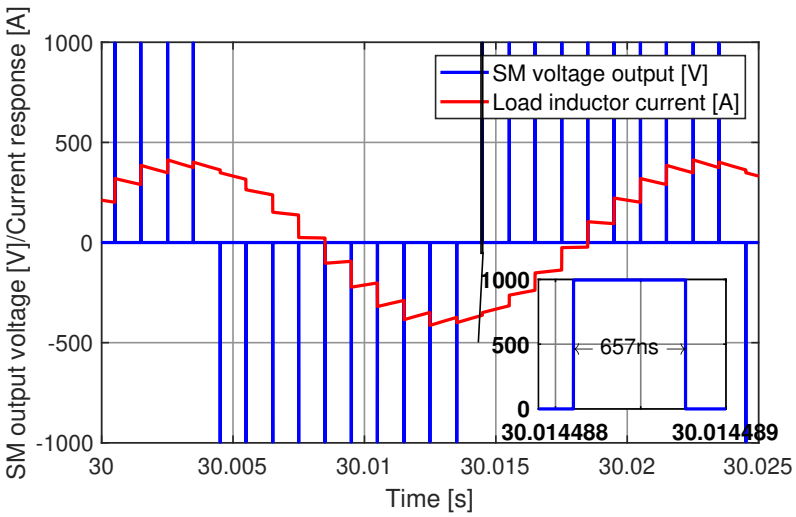


Figure 3.6: SM output voltage and load inductance current response for a $54\mu H$ load inductance at lowest achievable duty cycle, when considering a 50 Hz sinusoidal AC response.

its performance in different cases. For this, tests as the one shown in Fig 3.6 need to be conducted to extract the switching characteristics and thermal load and conclude on the design based on these results. However, as it can be seen in Fig. 3.6, due to the low load inductance value available, the load current achieved for those test conditions (m_a=0.025, phase shift = 30° and DC-link voltage=1000 V) is close to the SM maximum rating (500 A from Table 2.1). It is, however, of interest to test the SM at lower load current values as a starting point and then increase the load current level iteratively to avoid faults at low values. To pursue this idea of the possible working points, an investigation varying the amplitude and phase shift factors of the reference signals for the modulation of each of the HBs is conducted. The investigation aims to find working points at the minimum duty cycle allowed by the power module properties and knowing the output current conditions expected as the tests are run in open-loop control and need to be manually set. The simulation result is shown in Fig. 3.7.

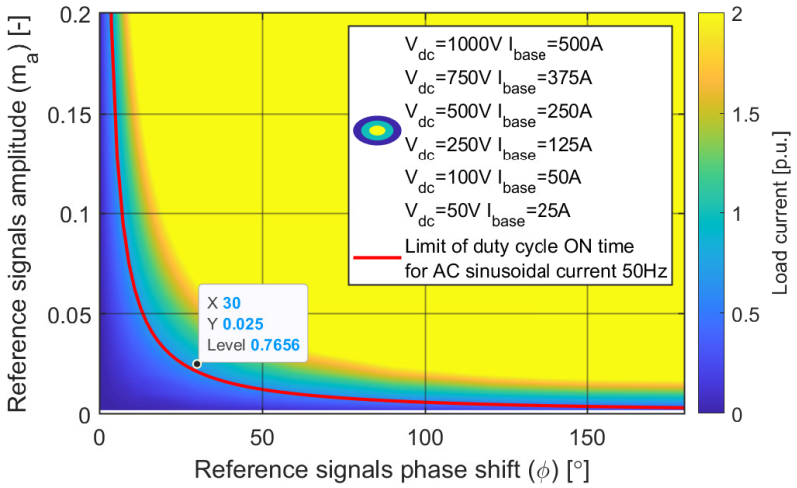


Figure 3.7: Maximum load current peak depending on the two SM HB's reference signals amplitude (m_a) and phase shift (ϕ), with available load inductance of $54\mu H$. Limitation of duty cycle ON time depending on IGBT turn-on time (650 ns) is shown to ensure sinusoidal AC current at 50 Hz.

From Fig. 3.7, different current testing points can be extracted. The red line marks the boundary of the test points that satisfy the requirement of having a minimum duty cycle larger or equal to the criterion of 650 ns. Therefore, only the ones to the right side of the red curve can be used. An example is highlighted in the plot, corresponding to the case of a load current of 0.76 p.u., which for a DC-link voltage of 1000 V leads to a load current peak of 380 A approximately. As can be seen from the figure, most of the points in the allowed area present a similar or higher load current value. To test the SM at lower load current conditions, it is, therefore, expected that lower than nominal DC-link voltages would be needed, e.g. an initial test with 100 V leading to 38 A, using the same point highlighted earlier with a lower base value. As lowering the DC-link voltage reduces the load current proportionally, the plot in Fig. 3.7 can be used for other voltage conditions, interpreting the maximum current base value as shown in the plot legend, correspondingly. This enables different test points to be used in the different test modes for the SM design assessment.

3.2.2 Auxiliary Systems

Different test equipment is needed to achieve the pursued test setup. This chapter considers the equipment which has to be investigated to achieve the proposed test setup in Fig. 3.2.

Power Supply

The power supply needed for supplying the DC-link of the SM is required to charge the DC-link and supply necessary losses during operation. For this purpose, a power electronic converter laboratory supply is used, which can be adjusted from 0 to 1000 V DC and can supply up to 30 kW at a maximum of 30 A. The output can only operate in the first quadrant operation for these types of power electronic converters, hence, sourcing power. Therefore, it has to be ensured that no power sinks to the power supply and is protected. For this purpose,

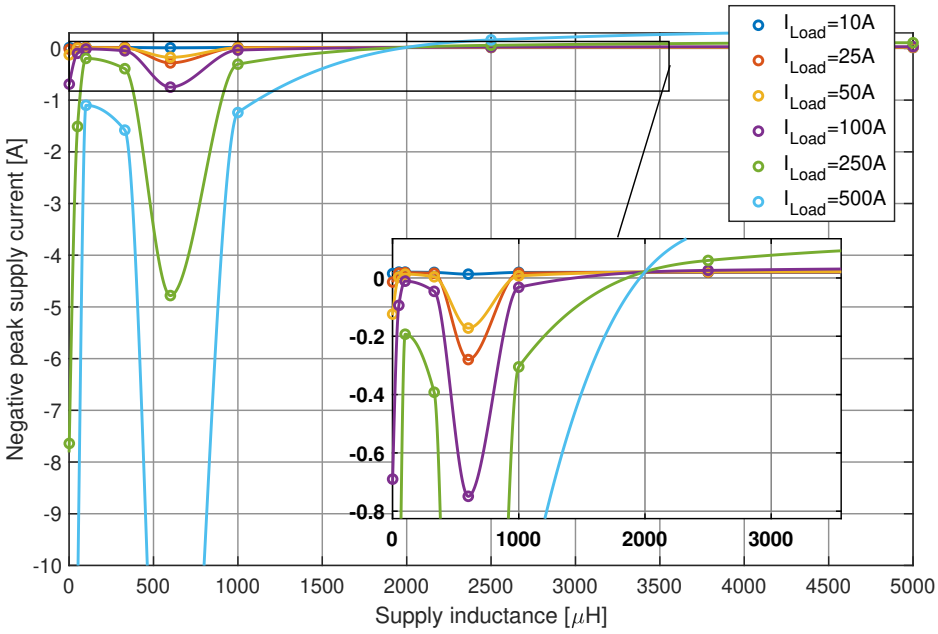


Figure 3.8: Supply inductance for power supply protection at various currents (50 Hz).

an impedance needs to be added to the load terminals. Simulating the setup presented in Fig. 3.2, the simulation result of using an inductance to decouple the power supply at various currents can be seen in Fig. 3.8. Here, it can be seen that a minimum inductance of 1 mH is needed to ensure no current-sinking into the power supply, which is a relatively high value. The reason is that a resonance frequency is formed between the DC-link capacitor bank of 4 mF and the supply inductance, which, in the case of applying a 50 Hz current, results in a relatively high sinking current. The maximum resonance frequency can be found from (3.1),

$$f_{LC} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{633\mu H 4mF}} \approx 100Hz \tag{3.1}$$

which shows that the resonance frequency is placed at 100 Hz. As the operational frequency of the SM is placed at 45-65 Hz, a high inductance value would be necessary. If instead a resistor is used, the simulated result is seen in Fig. 3.9.

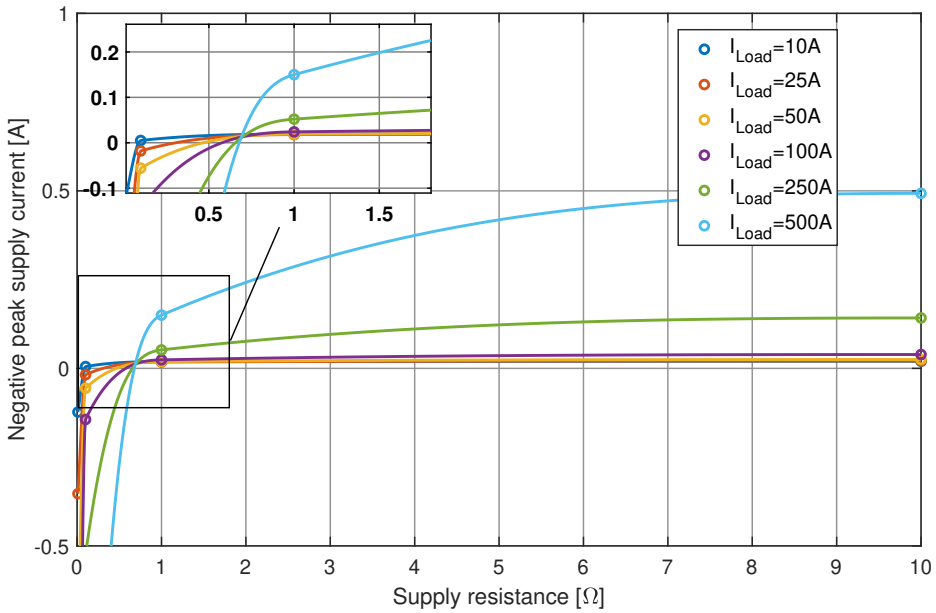


Figure 3.9: Supply pre-charge resistor for power supply protection at various currents (50 Hz).

This type of resistor is typically known as a pre-charge resistor to limit the charging time of the DC-link capacitor to avoid over- and oscillating voltages during pre-charging. From the simulations, it can be seen that from a resistance value of approximately $\geq 1\Omega$ no power (negative current) sinks to the power supply as the resistance value is constant. Therefore, this choice is better for this application, even though a slight voltage drop and loss should be expected. A value of 10Ω is chosen for this purpose.

Cooling System

Considering the cooling system, some requirements are derived from the investigations in Chapter 2. These are summarized in Table 3.2. A power loss per SM is estimated based on the full-load simulations conducted. The flow is derived from the datasheet where the flow-pressure drop is derived, which is seen in Fig. 3.10.

Table 3.2: Cooling system and sensor requirements requirements.

Requirement	Value
Estimated power loss	2 kW (1 kW per power module)
Flow	2-16 l/min (1-8 l/min per heat sink)
Pressure drop	0-20 PSI
Water temperature adjustment	20-60°C

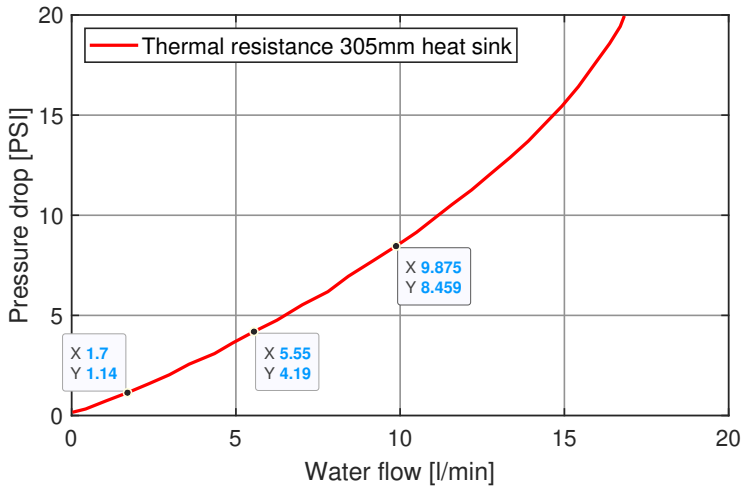


Figure 3.10: Heat sink pressure drop as function of water flow (single heat sink) [26].

Besides flow and pressure drop, a requirement of adjusting the ambient water temperature for 20 to 60°C is set to operate at various temperatures in the heat sinks. The cooling system solution is given in Fig. 3.11. The cooling system proposed consists of an inner and outer circuit. The inner circulates the water from a heat exchanger where the water is cooled by using a pump. The pressure drop and flow requirement are put on the pump, which needs

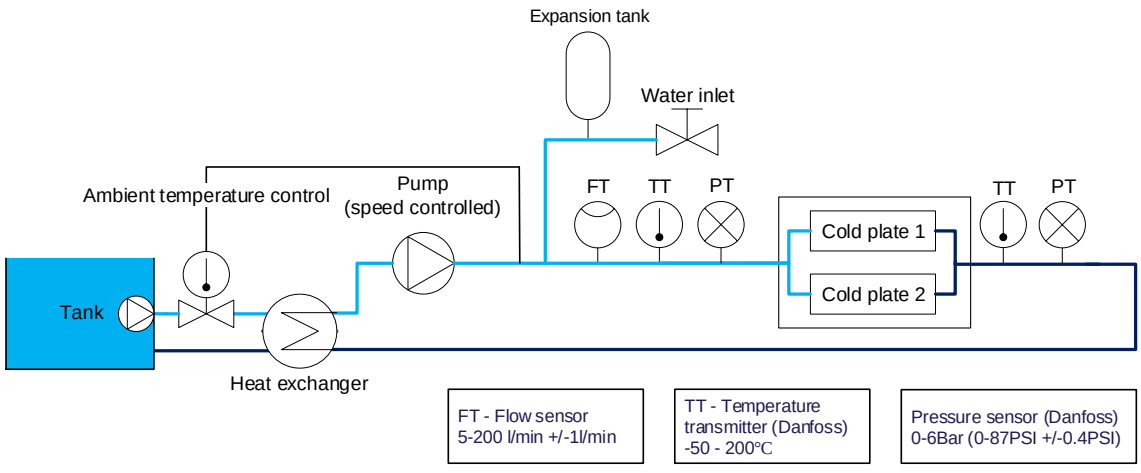


Figure 3.11: Cooling system for test setup.

to supply the required flow depending on the pressure drop of the heat sink. The ambient temperature requirement is solved using a temperature regulator controlling a valve, changing the flow to the heat exchanger and heating the inner circuit. The outer circuit water goes to a tank with enough cooled water to ensure a stable cooling water supply for the testing time. For sensing the flow, a flow sensor is used. This measurement can be cross-collated with a calculated flow from pressure drop measurements from pressure sensors and using Fig 3.10. Finally, a differential temperature measurement is added to measure the ΔT of the water.

3.3 Test specifications

In this section, the tests to be performed on the SM are explained. These include the two test modes mentioned earlier and a safe start-up/shut-down procedure for both cases. In the test cases, the test conditions and measurements are presented.

3.3.1 Start-up and shut-down procedure

A safety procedure is implemented to ensure safe start-up and shut-down of the SM during the test. Two procedures are made, one for starting up the SM and one for turning off the SM. These are correlated with the implemented software procedure in Fig. 2.40 to ensure consensus between these parts. The start-up procedure can be seen in Table 3.3.

Table 3.3: Start-up procedure for SM test.

Start-up procedure	
Scenario:	1) Remove short-circuit clamp 2) Close test area using Lock Out, Tag Out (LOTO) 3) Enable auxiliaries to control hardware and await initialization (state 0 and 1 in Fig. 2.40) 4) Turn on DC-supply 5) Charge to voltage set point (state 2) 6) Test mode (state 3) can be enabled

The first step of the start-up procedure involves removing the safety precautions made to ensure that the SM stays discharged. The test area is cleared, and the control hardware is initiated. After connecting to the SM, it is charged, and the test can begin. The shut-down procedure is similar and is shown in Table 3.4.

Table 3.4: Shut-down procedure for SM test.

Shut-down procedure	
Scenario:	1) Disable Test mode (state 3) 2) Turn off DC-supply 3) Wait for discharge of DC-link capacitors through resistor (state 4) 4) When discharged (state 5), break LOTO 5) Ensure discharge with grounding stick 6) Add short-circuit clamp for permanent discharge of DC-link capacitors

After stopping a test, the DC supply should be turned off, and the SM is discharged through the DC-link resistor. When fully discharged, the LOTO procedure can be removed. After entering the testing area, the SM is ensured to be discharged with a ground stick before the permanent short-circuit clamp is put to ensure constant discharge of the capacitor bank as it can charge slightly by itself, which could create dangerous situations between tests. The start and shut-down procedures are pre- and post-caution measures implemented for all test cases before and after any test.

3.3.2 Test Mode 1: No-load Test

The purpose of test mode 1 is, as illustrated in Fig. 3.1, to perform the measurement needed to verify the design, which does not need the SM to be under load. This test mode includes an electrical test to see the switching characteristics to verify turn-on and turn-off behaviour against the result used for the design. Besides this, the general operation and functionality of the SM should be seen. The minimum duty cycle ON time is also verified in this test mode to compare with the minimum turn-on time of 650 ns from the power module datasheet and verify the open-loop control performance. The test mode is described in Table 3.5.

Table 3.5: Test mode 1: No-load for SM test.

Test mode 1: No load	
Test conditions:	• DC-link voltage: 100 V, 250 V, 500 V, 1000 V • Frequency: 50 Hz • Reference signal amplitude (m_a): 0.02, 0.1, 0.2, 0.5, 1 • Reference signals phase shift (ϕ): 10°20°60°100°180°
Parameters to obtain:	• SM output characteristics to ensure output mapping in Fig. 3.7 • SM turn on and off characteristics
Measurements:	• Electrical: V_{out}, V_{ce}, V_g, V_{dc}
Scenario:	1) Charge DC-link voltage to 100 V 2) Enable test mode (state 3) 3) Adjust reference signals (amplitude/phase shift) to first point 4) Obtain measurements 5) Repeat from 3) with next point 6) Charge DC-link to next reference point 7) Repeat from 3) 8) Disable test mode 9) End of test

The test conditions described in Table 3.5 are the conditions for which the test is conducted. All conditions having multiple parameters are conducted in a combination of each other to obtain the data. In this case, the DC-link voltage is increased gradually to verify it at lower voltages before entering the full-voltage state. In these cases, various reference signals are set to ensure that the open-loop control is working correctly. The parameters to be obtained and their corresponding measurements are the needed data to be measured during the test, which are later used for the final validation. The presented scenario includes all parameters obtained during all combination of test conditions and assumes no error in any test. If an error is found, the test is terminated using the shut-down procedure.

3.3.3 Test Mode 2: Load Test

The second test mode is made to conduct the test where the load current is applied. From the first test mode, the operation in open-loop is validated considering the operation conditions in Fig. 3.7. In this test mode, the current should therefore be fully controllable. The test mode is described in Table 3.6. In test mode 2, the same voltage levels from test mode 1 are

Table 3.6: Test mode 2: Load for SM test.

Test mode 2: Load	
Test conditions:	• DC-link voltage: 100 V, 250 V, 500 V, 1000 V • Arm current (peak): 50 A, 100 A, 250 A, 500 A • Frequency: 50 Hz • Flow: 1.7 l/min (low), 5.55 l/min (nominal), 10 l/min (high) • Ambient water temperature (T_{amb}): $20°C$, $30°C$, $40°C$ • Pure water
Parameters to obtain:	• SM turn-on and off characteristics during load conditions both in the **beginning** of test and **after** thermal stability is reached. • SM thermal characteristics including baseplate temperature, ambient water temperature, heat sink flow, SM pressure drop and power module voltage and current for loss estimation.
Measurements:	• Electrical (start and end of test): V_{out}, I_{arm}, V_{ce}, I_c, $I_{dc,supply}$ • Thermal (start to thermal stability): $T_{baseplate}$, T_{amb}, F_{flow}, p_{in}, p_{out}
Scenario:	1) Charge DC-link voltage to 100 V 2) Adjust cooling system flow to first point 3) Adjust reference signals to accommodate first current point 4) Enable test mode (state 3) 5) Wait until thermal stability is reached 6) At thermal stability, obtain one electrical measurement 7) Disable test mode (state 3) 8) Await thermal stability 9) Repeat from 3) with next current point 10) Repeat from 2) with next flow point 11) Charge DC-link to next reference point 12) Repeat from 3) 13) Disable test mode 14) End of test

considered, starting at lower than rated values. Again this is done to not have full voltage on the SM, as this now influences the current response rate. The current is also increased from low to rated values when possible, using open-loop control and following the load mapping earlier described. Besides the electrical open-loop control, the cooling system is set first to nominal flow and later to higher flow to validate the thermal characteristics. During this test, the electrical characteristics are measured after thermal stability is reached. This is done to see the characteristics for full-load at rated temperature. Besides verifying the electrical characteristics, the measurements are used to estimate the power losses. All thermal measurements are made during the full testing time while electrical measurements are obtained at test start and after thermal stability is reached.
The next chapter describes the experimental results after implementing and conducting these test modes in the actual hardware.

Chapter 4

Results and Discussions

In this chapter, the test results from the commissioning and test modes of the SM are presented. The results are validated based on the design requirements and choices made in Chapter 2. From the results, discovered failure modes and improvements are discussed together with possible mitigation. Finally, conclusions of the first iteration SM design are made, and improvements for a potential next iteration stated.

4.1 Commissioning Results

In this section, the results of the various commissioning tests, presented in Table 2.16, are presented and concluded. The same table extended with results is seen in Table 4.1. In the assembly phase of the power hardware, the isolation test of the busbars is conducted using an isolation tester. This measurement shows that the insulation is in good condition with an insulation resistance found to be higher than 1GΩ, as seen in Fig. 4.1a at 1056 V DC. All capacitors' capacitance is measured independently. These are all found in the lower tolerance band range, close to the -10% as seen in the table. The reason for the lower capacitance is assumed to be the cause of capacitor ageing during storage. Fig. 4.1b shows the measurement of the capacitor bank, which also shows a total capacitance within the -10%, therefore, within the range and exactly ten times the single capacitors, meaning that all capacitors are efficiently coupled in the DC-link.

(a) Isolation measurement between busbars.

(b) LCR meter measurement of the complete capacitor bank.

Figure 4.1: Power hardware commissioning activities measurements.

Considering the control hardware, the PCB shows promising results in the initial commissioning test. The PCB connections are made correctly, and measurements verify all the functionalities on the individual components and ICs. The PWM is tested using both waveform generator and later DSP and shows minimal time delay from DSP out to the gate driver PWM

input of around 120 ns, as seen in Fig. 4.2. The dead-time setting of 1.4 μs is found to be 1.9 μs in Fig. 4.3 which leaves some additional margin. Additionally, the computational time required by the DSP to execute the open-loop control in the PWM interrupt is also measured, both for the cases when the test mode is disabled and enabled. The timings are found to be 55.9 μs and 62.9 μs, respectively, as it can be seen in Fig. 4.4, hence additional 7 μs to calculate and update the reference signals. This result supports the diagram given in Fig. 2.42. The analogue signals processing circuitry and DSP ADC are first tested emulating the inputs, however, without the sensor before having the full assembled SM. During this initial test, the offset of the voltage and current is 5 mV and 14 mV, respectively. These offsets are compensated in the DSP code when calculating the analogue measurements. The final tests involving the full assembled SM consist of the PWM test and testing the actual voltage, current and temperature sensors. The PWM including gate drivers shows a close fit with only additional 100 ns from level-shifter output to the gate driver's actual gate signal reaction, giving a total of 220 ns delay from the controller to gate signal reaction, as seen in Fig. 4.2. The test is carried out for the sensors with zero voltage in the DC-link, coupling the DC supply directly to the voltage sensor and a 1 A supply with 10 windings on the current sensor. During these tests, it is observed that the output values of the sensors fluctuate in their value. This phenomenon is further studied in the following section.

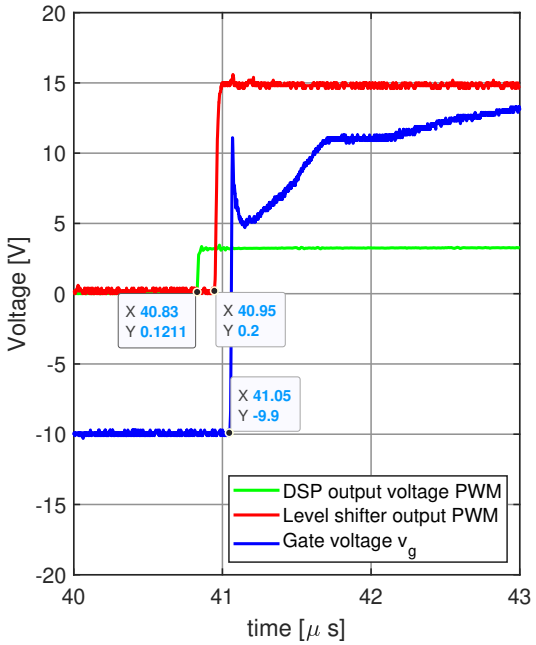


Figure 4.2: PWM delay from DSP output to gate voltage reaction.

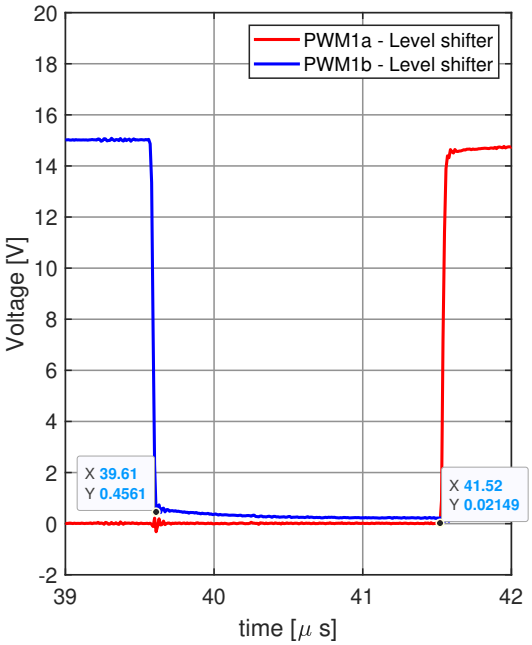


Figure 4.3: PWM dead-time between upper and lower switch of one HB.

Table 4.1: SM commissioning test.

Component/assembly	Test	Acceptance	Results/accept	Notes
DC-link busbars assembly	Isolation measurement	>500MΩ	>1000MΩat 1056V DC	
DC capacitors	LCR meter measurement	400uF +/-10%	367.90uF +/-4.32uF	CI: 95%
DC capacitor bank (10 psc)	LCR meter measurement	4mF +/-10%	3.67uF	
PCB	I/O test	<1mΩ	Ok	
PCB	Functional test			
	• Power supplies	Ok	Ok	
	• Voltage references	Ok	Ok	
	• Op-amps circuitry	Ok	Ok	
	• Voltage level shifters	Ok	Ok	
	• Sensor input (without high voltage and current sensors)	Ok	Ok	
DSP	Functional test			
	• PWM strategy (frequency, dead-time, etc.)	Ok	Ok	
	• ADC	Ok	Ok	
	• Fault conditions	Ok	Ok	
Control board (PCB+DSP)	Functional test			
	• PWM output	Ok	Ok	
	• ADC input	Ok	Ok	
	• Auxiliary LEDs	Ok	Ok	
	• Fault signals by emulation of gate driver, over-voltage, over-current, temperature	Ok	Ok	
Submodule complete assembly	Functional test with 0V DC on DC-link			
	• PWM including gate driver boards and PM at 0 V DC	Ok	Ok	
	• ADC including sensors	Ok		
	• Voltage sensor at 0-1000V		(Ok - reduced operation)	Noise in sensor values observed
	• Current sensor at 0-10A		(Ok - reduced operation)	

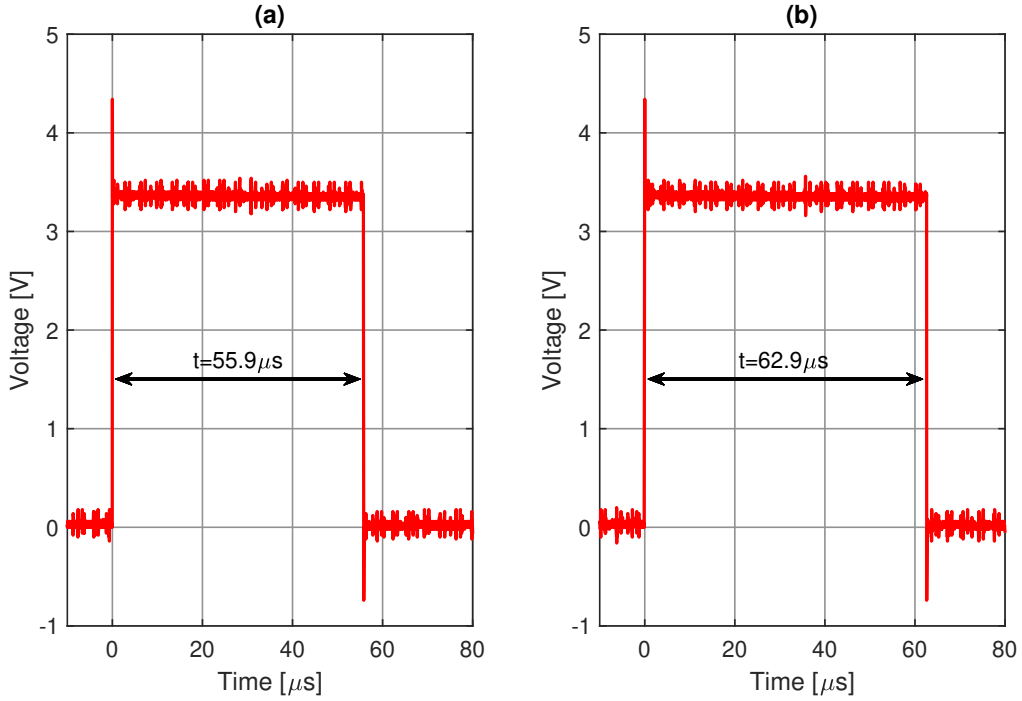


Figure 4.4: DSP PWM interrupt computational time (a) Test mode disabled. (b) Test mode enabled.

4.1.1 EMC analysis of data acquisition

As mentioned in the commissioning activities of the signal processing circuit, the voltage sensor is tested to evaluate its performance before using it in the SM tests. All the test results shown in the following figures correspond to the case of having a stable 0 V input in the DVC 1000-P voltage sensor (Fig. 2.27) and reading the analogue signal fed to the DSP ADC, after the circuit shown in Fig. 2.28, which for a 0 V DC on the DC-link should give a constant output of 1.82 V.

After configuring the test as explained and reading the signal to the DSP, the measurement shows a fluctuating result instead of the expected constant value. This problem is analysed in further detail in the measurement presented in Fig. 4.5. Observing this result, it can be seen that there is a noise issue affecting the analogue signals. In the DC-link voltage case, a high-voltage range of $\pm$1.5 kV is transformed to 0-3.3 V; therefore, a change of a few mV in the low-voltage signal is translated into a severe voltage jump when the DSP calculates the DC-link voltage. This also explains the fluctuations observed in the ADC result. This problem is categorised as an Electromagnetic Compatibility (EMC)/Electromagnetic Interference (EMI) problem, where three possible solutions exist, mainly; remove the noise source creating EMI, remove or improve the noise path, or improve the data acquisition EMC including noise rejection. When observing this problem, an effort is first made to detect the noise source, firstly with the hypothesis that the noise originates from the signal processing circuit in charge of the data acquisition signal conversion. The components involved in this circuit, mainly sensor DVC 1000-P and Op-amps, are checked to verify any malfunctioning. Additionally, the low-pass filter passive component values are verified for giving the desired cut-off frequency. However, no intermediate results show evidence that any of these initially studied components should be faulty or the noise source.

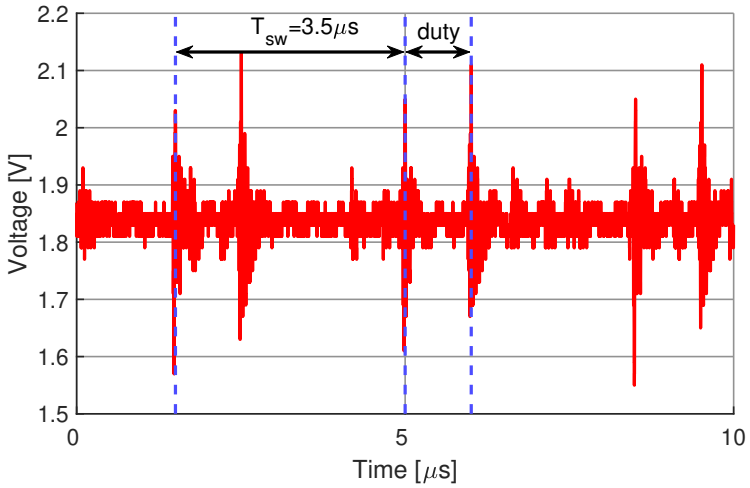


Figure 4.5: DC-link voltage measurement on 3.3 V side when having a 0 V input on the high-voltage side.

However, analysing the measurement in Fig. 4.5 in detail, it is observed that a periodic behaviour is seen in the noise signal. In this case, the period corresponds to 3.5 μs, which is related to a frequency of 285 kHz. Analysing this fact, the only components in the control PCB that have a defined switching frequency are the isolated DC/DC power supplies. When analysing the datasheets of the different models, the THL25 power supply used to feed the gate drivers has a switching frequency that matches the 285 kHz observed. To verify this hypothesis, the mentioned DC/DC power supply is disabled on its input, interrupting the connection to the main 24 V supply. After doing this, the voltage signal is measured, giving the result shown in Fig. 4.6.

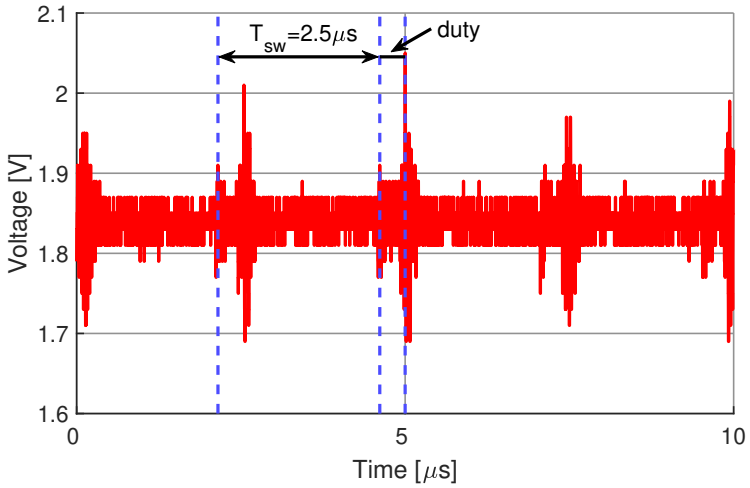


Figure 4.6: DC-link voltage measurement on 3.3 V side when having a 0 V input on the high-voltage side after removing the DC/DC power supply feeding the gate drivers.

As it can be observed from Fig. 4.6, the noise having the 285 kHz is now gone and proves that it originates from the THL25 supply. However, there is still noise affecting the voltage sensor signal, characterised by a lower peak value and a different period. From the figure, it can be measured that the noise now has a period of 2.5 μs, corresponding to a switching frequency of

400 kHz. Keeping the proven hypothesis that the noise source is still the switch-mode power supplies, this frequency is related to the DC/DC supplies of the THN15 series.
From this analysis, it can be concluded that the DC/DC power supplies are the primary source of noise. These fluctuations are not acceptable as these can lead to spurious representations of the voltage and current signals, which, when used in closed-loop control, can lead to instability or even make the SM protection trip. In a first attempt of solving this problem focusing on the EMC side, the MLCC filtering capacitors in the output of each power supply are increased in value. However, this solution does not have a significant effect, and the noise still has an inadmissible magnitude. Next, all the isolated DC/DC converters are disabled to reduce this phenomenon. External laboratory supplies supply the different voltages of the control PCB for the cases of 5 V, 15 V, and $\pm$15 V. While the 3.3 V are obtained from a built-in LDO in the DSP docking station from the 5 V. After implementing this additional solution, the measurement is repeated, showing the plot in Fig. 4.7. From this figure, it can be seen how the noise is dramatically reduced, presenting acceptable levels and ready to be used, again concluding that all the switch-mode power supplies inject unacceptable EMI noise considering the data acquisition EMC capabilities.

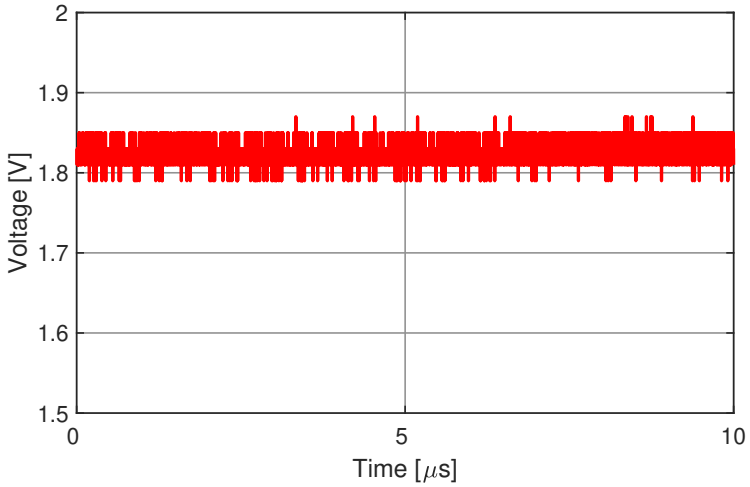


Figure 4.7: DC-link voltage measurement on 3.3 V side when having a 0 V input on the high-voltage side and supplying the PCB by external supplies.

It should be pointed out that the results presented so far are obtained with the control PCB separated from the rest of the SM hardware and just connected to the high-voltage power supply presented in Section 3.2.2. However, after mounting the control PCB on the SM, the voltage measurement fluctuations are observed again, as shown in Fig. 4.8. Besides the analogue measurements, the two gate drivers are the only additional connections made to the control PCB from the SM power hardware compared to the earlier tests. Therefore, these must be the new noise sources. Observing Fig. 4.8a, it can be seen how a periodic noise waveform is present, which has a switching frequency of 285 kHz worth mentioning without enabling PWM switching. The chosen gate driver has a built-in DC/DC converter to supply its electronic components. It can, therefore, only be concluded that this additional supply is injecting noise back to the control PCB through the interface connectors when considering the former investigation. This noise magnitude is intensified when IGBT's PWM is enabled as it can be observed at 15 μs in Fig. 4.8b. This additional noise increase can be avoided by not

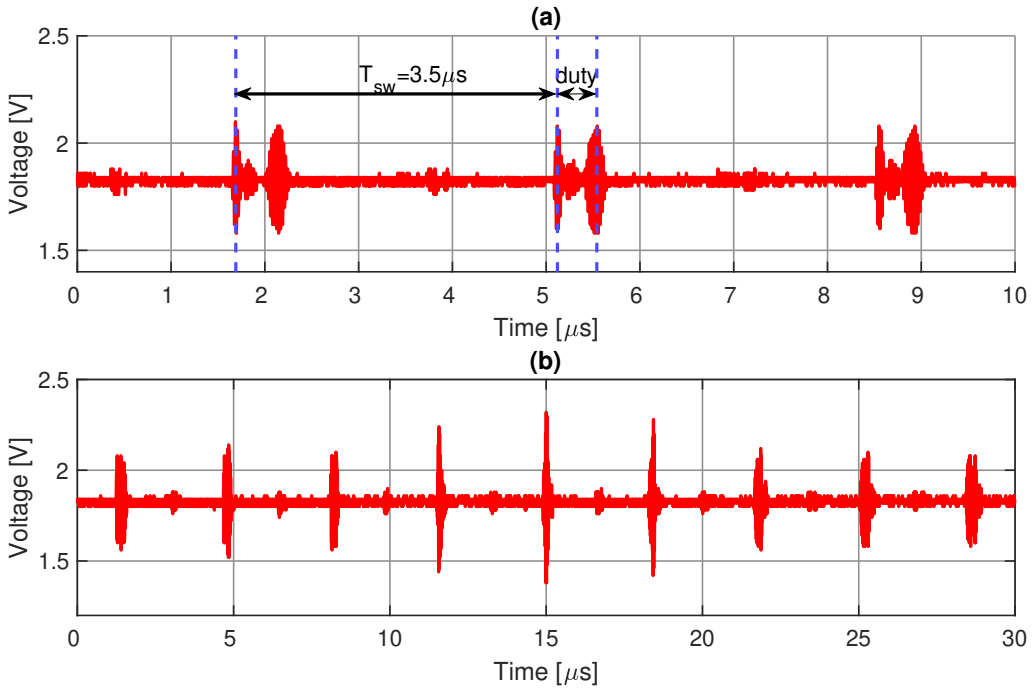


Figure 4.8: DC-link voltage measurement on 3.3 V side when having a 0 V input on the high-voltage side after connecting the gate drivers. (a) No IGBT switching. (b) IGBT switching.

sampling the analogue signals when a switching event is produced. However, as the DC/DC supply on the gate drivers is not synchronised with the PWM and has its switching frequency, it is not possible to avoid its effect in this way. Further, the hardware protection will still be affected by the switching noise for which it should be immune.
In general, it can be concluded for all DC/DC supplies on the control board that the noise is not acceptable for the current EMC properties of the developed data acquisition. Therefore, a solution needs to be found. As the gate driver is a commercial component, it can not be

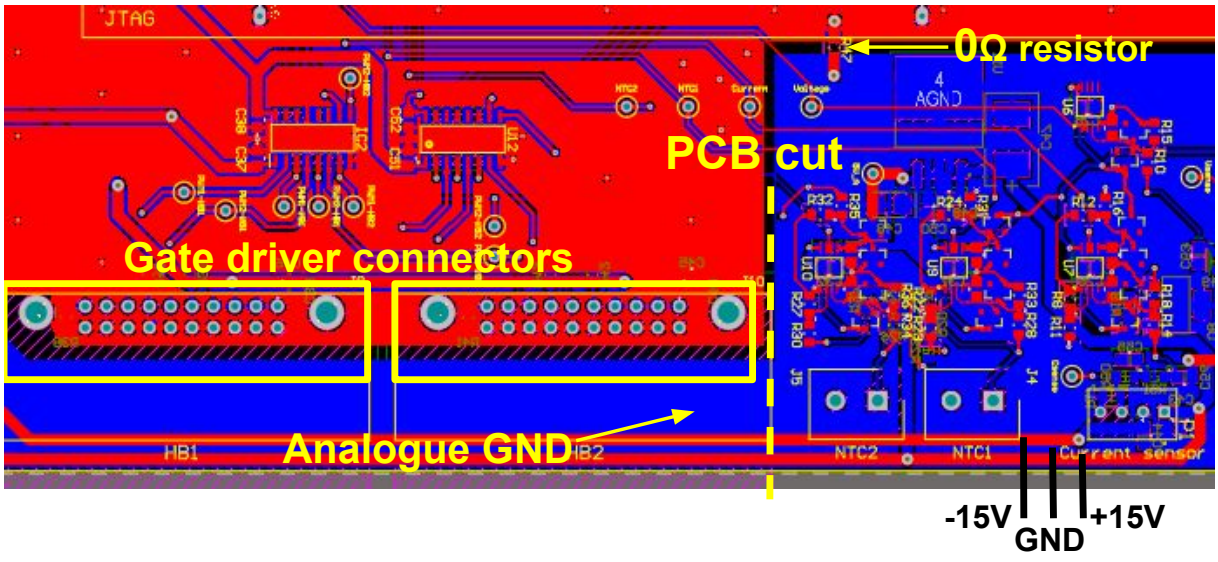


Figure 4.9: PCB arrangement to reduce noise coupled from the gate drivers.

modified, and therefore no further EMI improvements can be made, leaving improvements on the noise route and EMC properties as solutions. When observing the PCB layout, it is seen that the connectors of the gate drivers are placed close to the analogue ground plane, being crossed by the cables routed to the gate driver boards. This arrangement can allow the gate driver noise to be coupled to the analogue part of the PCB, affecting the signals. Based on this observation, the analogue ground plane is interrupted, disabling the part interfering with the gate driver connection and enabling a connection through another part of the control PCB, which is shown in Fig. 4.9. It should be pointed out that after cutting the PCB, the analogue ground and supplies are re-routed from the external supplies, as shown in the figure. The 0 Ω is kept as it acts as a returning path for the analogue signals. After implementing this measure, the voltage sensor signal is re-evaluated, giving the result in Fig. 4.10.

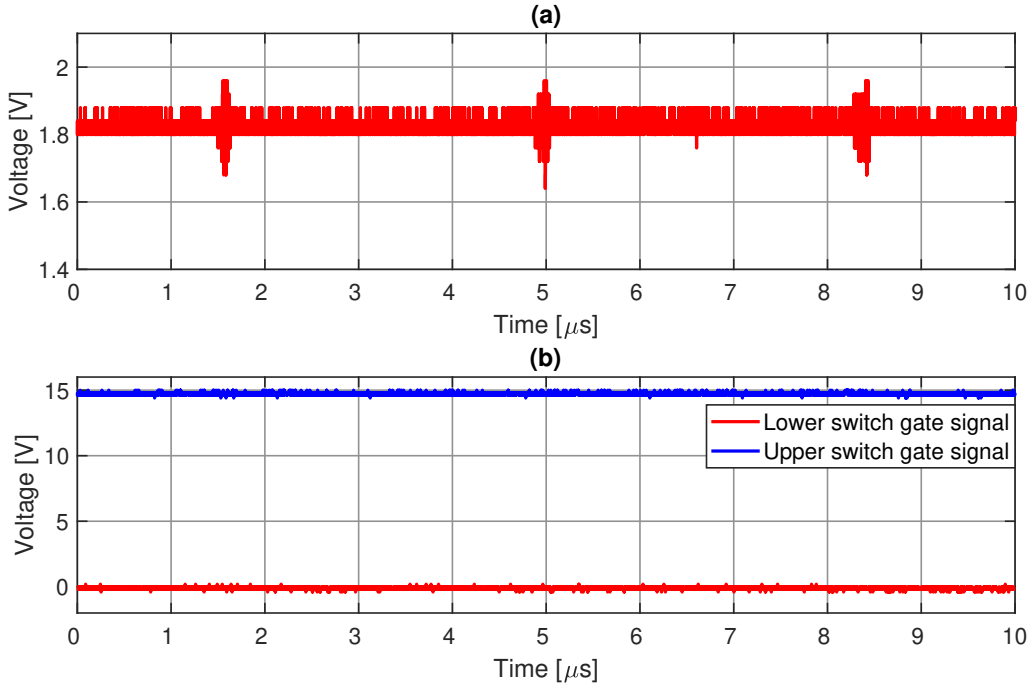


Figure 4.10: (a) DC-link voltage measurement on 3.3 V side when having a 0 V input on the high-voltage side after connecting the gate drivers and rearranging the PCB layout. (b) Gate voltage signals on HB1.

Fig. 4.10a shows the noise effect on the DC-link voltage signal from the data acquisition to the DSP when no switching of the IGBTs is conducted, as indicated by the gate signals plotted in the plot (b). Comparing plot (a) in this figure to Fig. 4.8a, it can be seen how the noise magnitude is reduced, hence validating the improvement in Fig. 4.9. Fig. 4.11 shows the measurement result when a switching event takes place. It can be seen in Fig. 4.11a how the noise magnitude is increased when this occurs. The switching event is also plotted in Fig. 4.12 with a larger time scale. Besides observing the switching effect commented for Fig. 4.11, the effect of the gate driver power supply can also be seen over time.

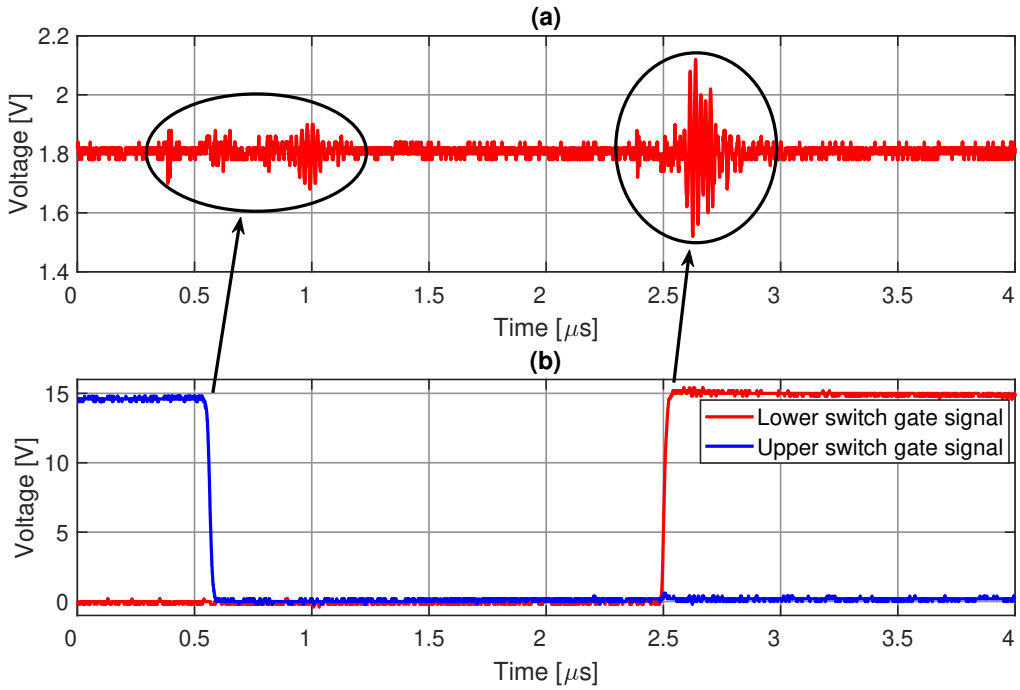


Figure 4.11: (a) DC-link voltage measurement on 3.3 V side when having a 0 V input on the high-voltage side after connecting the gate drivers and rearranging the PCB layout. (b) Gate voltage signals on HB1.

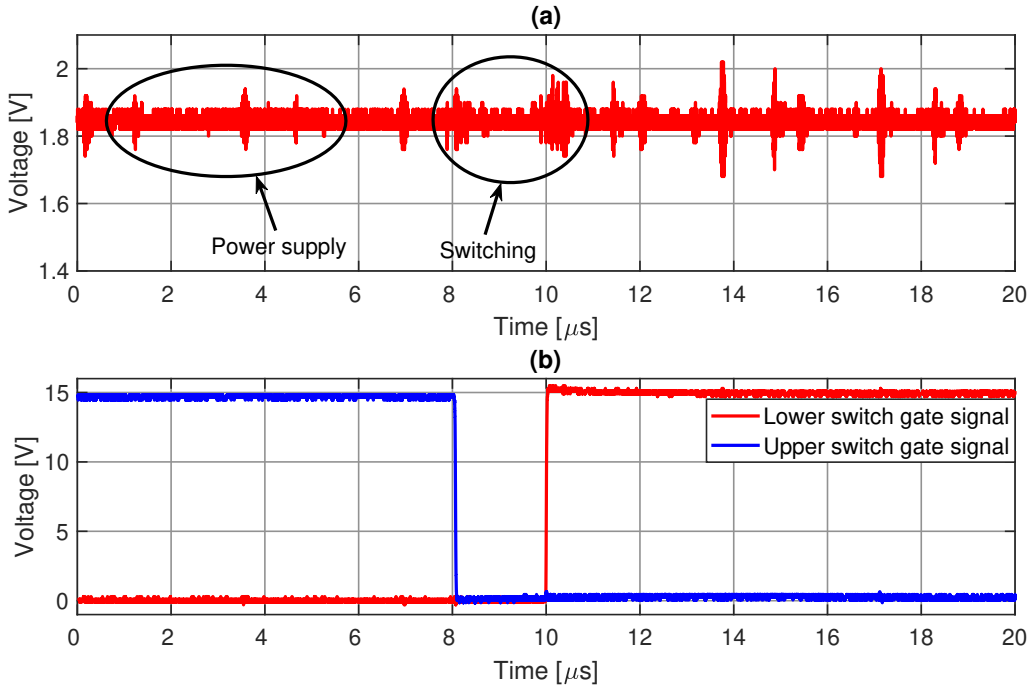


Figure 4.12: (a) DC-link voltage measurement on 3.3 V side when having a 0 V input on the high-voltage side after connecting the gate drivers and rearranging the PCB layout. (b) Gate voltage signals on HB1.

After these investigations, it can be concluded that the analogue part of the control PCB needs to be improved in terms of noise immunity. This noise affects the analogue signals acquisition

as it lowers the DSP ADC resolution by worsening the signal-to-noise ratio. Fig. 4.13 shows how many ADC bits are lost due to the noise. Fig. 4.13a shows a measurement of the DSP ADC when measuring its own ground reference, without being mounted on the control PCB. It can be seen how the maximum lost bits obtained is 8, which, for the 12-bit ADC, corresponds to 3.3*(8/4095)=4.2 mV or 4.3 V on the DC-link. However, Fig. 4.13b, higher bit losses are observed. The largest bit loss corresponds to 54, translated into 46.3 mV or 47.4 V on the DC-link.

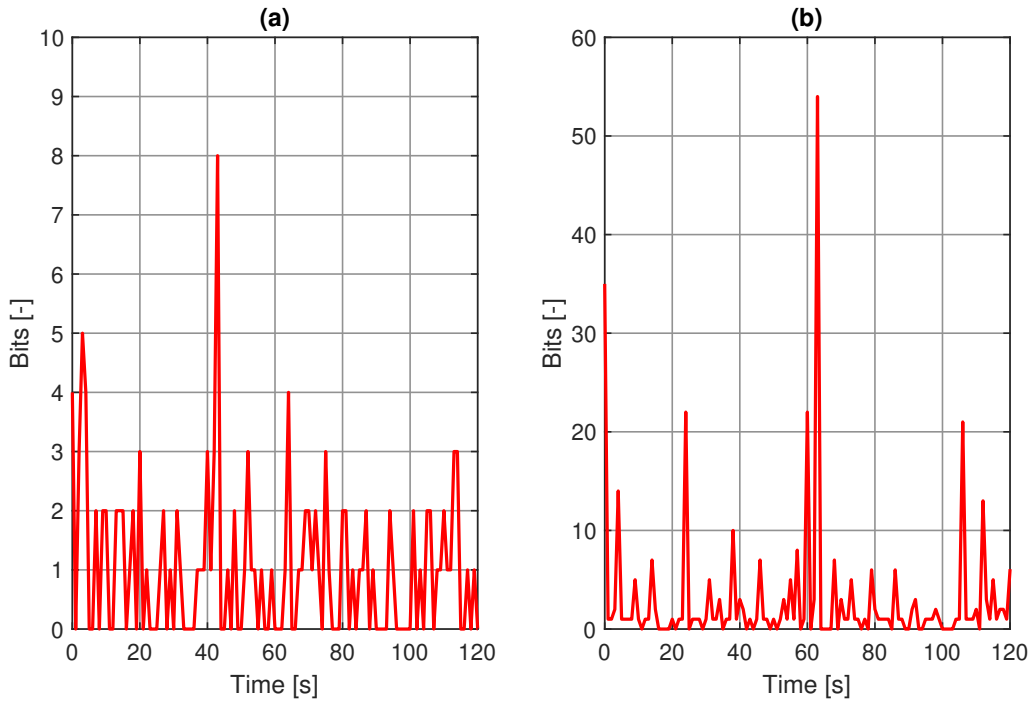


Figure 4.13: DSP ADC measurement of ground voltage. (a) Standalone DSP controlCARD. (b) DSP mounted on control PCB.

Additionally, the SM operation is limited due to the noise present in the DC-link voltage signal. This signal is used in the hardware protection to protect the SM against over-voltage scenarios, where the voltage limit is set at 1350 V, as introduced in Section 2.4. As the DC-link voltage signal processing circuit translates $\pm$1500 V to 0-3.3 V, small variations in this signal mean a high jump in the voltage seen by the protection. These fluctuations due to noise in the signal create a momentary time where the voltage seen by the over-voltage protection surpasses the reference value, even though the DC-link voltage is much lower. This noise makes the protection trip and stops the SM operation. This phenomenon is investigated during the commissioning stage of the project. Here a limit of 480 V is found as the maximum operating voltage of the SM in the actual conditions. The result can be seen in Fig. 4.14. From 4.14b in the figure, it can be seen how the comparator output goes to the low level, which indicates a fault when the DC-link voltage reaches 480 V approximately, seen in plot 4.14a. It should be noted that this test is conducted during charging of the DC-link, without any IGBT switching enabled.

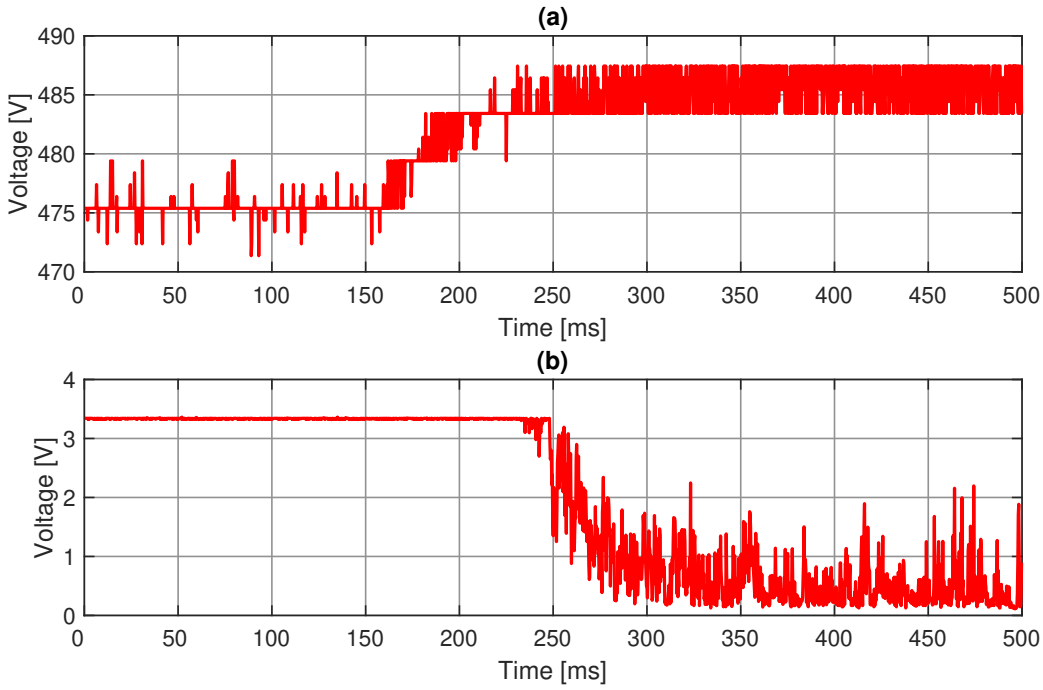


Figure 4.14: SM DC-link voltage limitation due to PCB noise. (a) DC-link voltage. (b) DC-link voltage comparator output value of hardware protection.

4.2 Test Results

This section describes the test results of the no-load and load test conducted on the setup, which is described in Chapter 3.

4.2.1 Test mode 1: No load

This section presents the results of the no-load test conducted on the prototype. As a reminder, the main objectives of the no-load test are to verify the switching operation of the design and the load mapping in Fig. 3.7. The first focus is on the electrical switching characteristics of the first operations measured at open terminals of the SM. Here the focus is on obeying the maximum requirements of the power hardware components while operating as intended.

Transient switching analysis - no-load

The first operations are made at a DC-link voltage of 100 V. One turn-on and turn-off event at this voltage are seen in Fig. 4.15 As it can be seen in Fig. 4.15a and b, the collector-emitter voltage includes some ringing which is concluded to originate from the parasitic resistance and inductance of busbars. Focusing on the turn-off in Fig. 4.15b which leads to the highest voltage overshoots, it can be seen how the collector-emitter voltage ringing reaches 162.5 V, leading to an overshoot of 62.5% over the actual DC-link of 100 V. Assuming that the highest voltage leads to a similar overshoot, this is within the maximum of 70% given in the design chapter. The DC-link voltage in Fig. 4.15b has a voltage overshoot of 9.5 V, leading to a 9.5% overshoot which also complies with the ratings of the maximum capacitor voltage, allowing

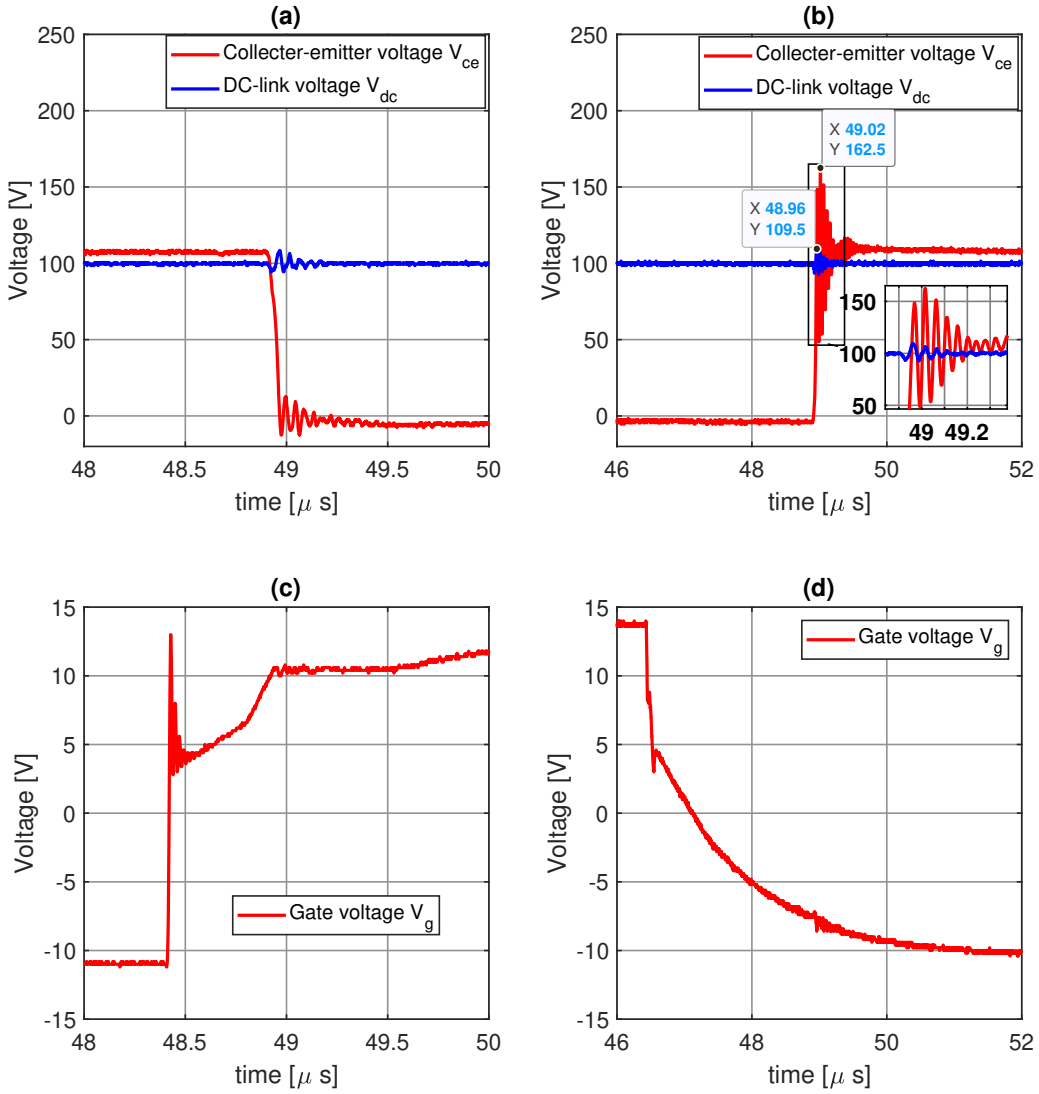


Figure 4.15: SM IGBT switching characteristics at 100 V DC-link.

35% overshoot. It should be mentioned that these tests are conducted with no-load current, and therefore the voltage overshoots are caused by the different current travel distances from the various capacitors and their interactions. Adding the load current will further increase the di/dt and increase the voltage overshoot, which will be studied further in the load tests. The gate voltage shows expected behaviour where the voltage is close to the full gate voltage due to the no-load conditions, where the IGBT is rapidly brought from the saturated to the triode region due to the fast collector-emitter voltage transition to zero. Further, due to the gate's parasitic inductance, a voltage overshoot is seen when the gate turns on. The DC-link voltage is increased to 250 V to test the voltage oscillations at higher voltages, and the results are seen in Fig. 4.16.

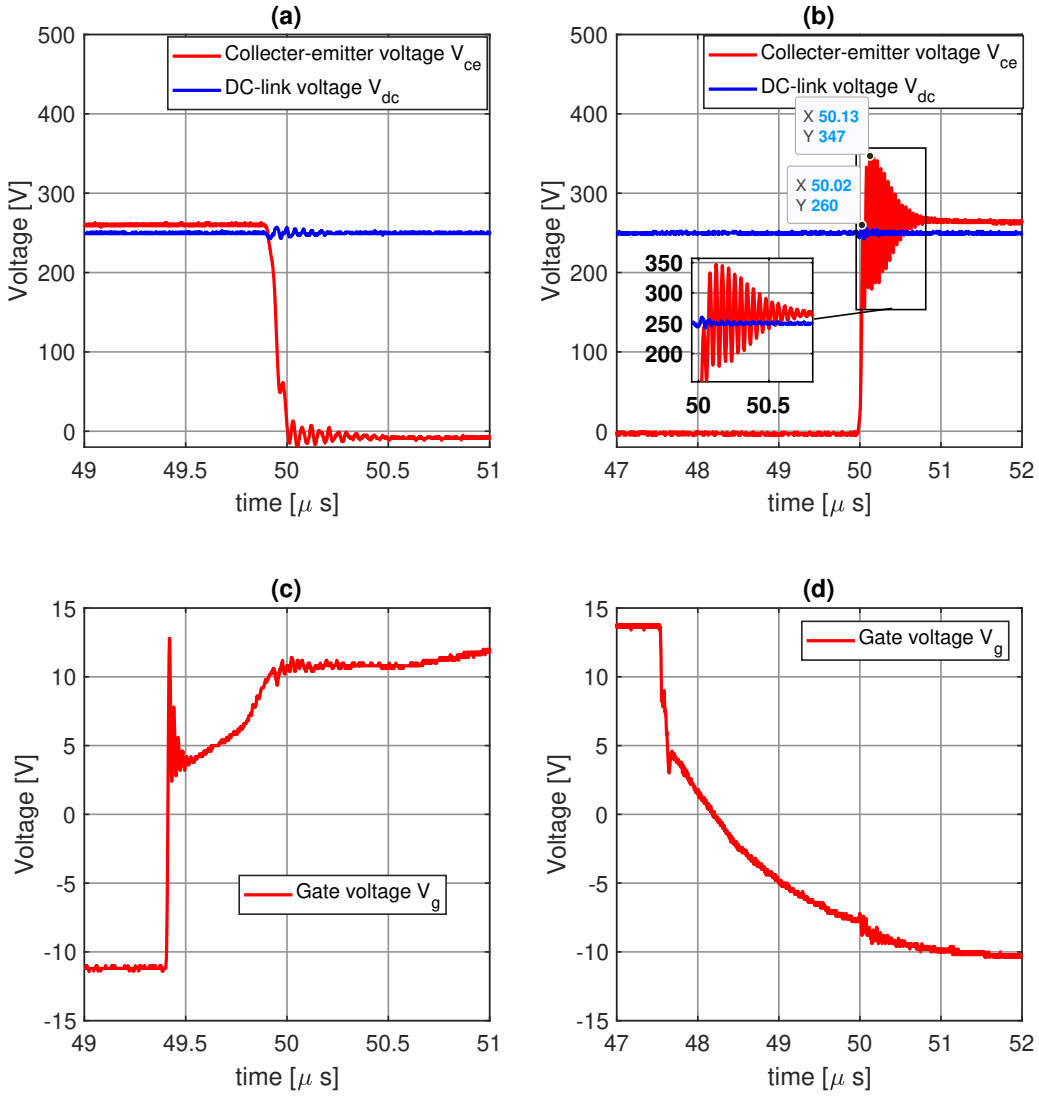


Figure 4.16: SM IGBT switching characteristics at 250 V DC-link.

Fig. 4.16b, again shows the largest oscillations during turn-off. The collector-emitter overshoot increases to 347 V, corresponding to an overshoot of 38%, meaning that compared to the 100 V case, the maximum percentage overshoot decreases, as the voltage overshoot only increases from 62 V to 97 V. One reason for this is that the di/dt is still the same small leakage current as no load is applied. The ringing, therefore, stays at a similar amplitude. Further, the DC-link overshoot is still approximately 10 V leading to an overshoot of around 4%. Increasing the voltage further to 500 V as planned for test mode 1 leads to a problem with the hardware protection, which detects an over-voltage due to the EMC problem in the data acquisition as earlier mentioned. Therefore, the voltage is increased to 400 V, for which the protection does not trip. This can be seen in Fig. 4.17.

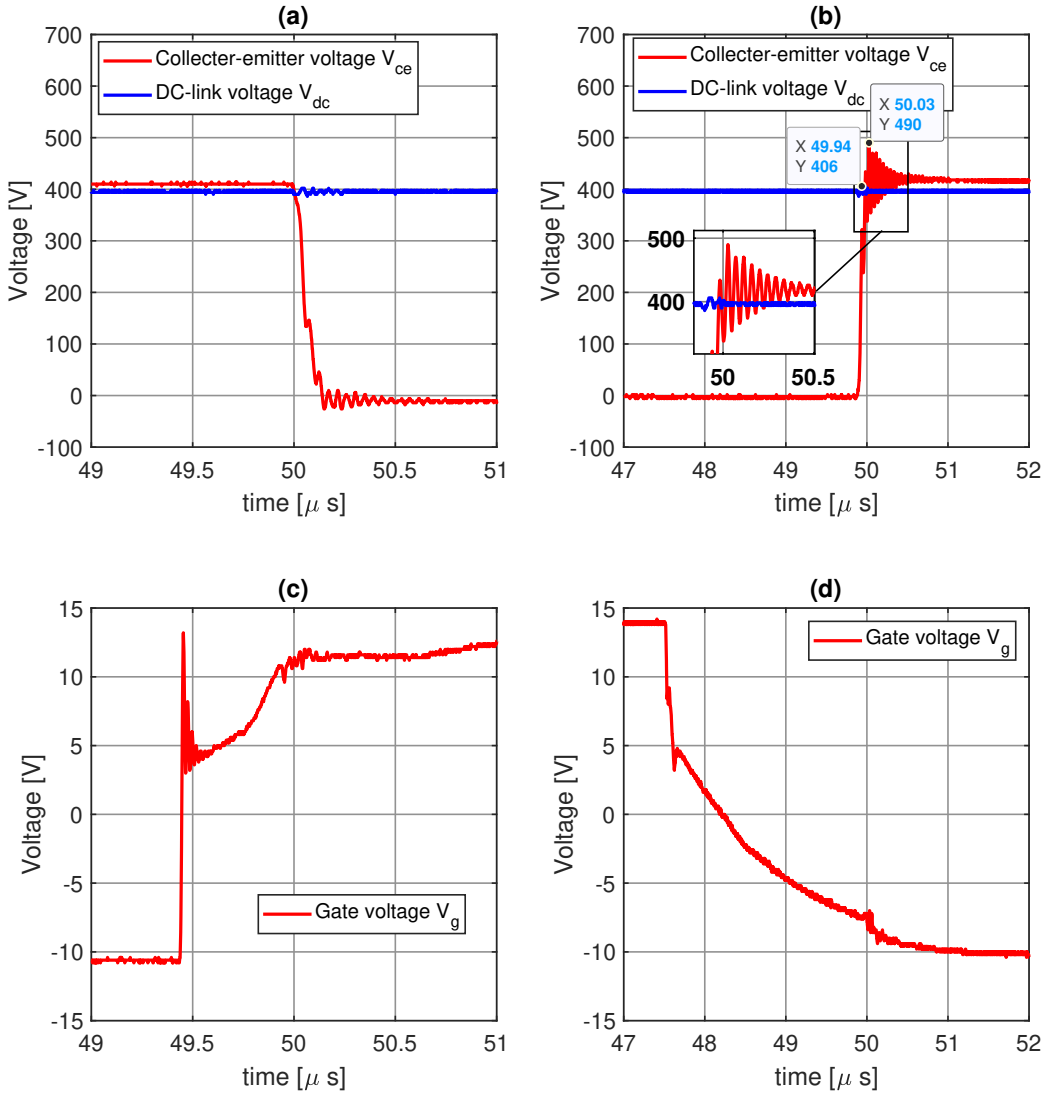


Figure 4.17: SM IGBT switching characteristics at 400 V DC-link.

After further increasing the voltage to 400 V DC, the collector-emitter voltage overshoot does not increase further but decreases slightly from 38% at 250 V DC to 22.5% seen for the turn-off in Fig. 4.17b. Similarly, the DC-link overshoot is at 1.5%. Comparing the turn-on and turn-off time of the collector-emitter voltage presented, increasing the DC-link voltage in general decreases the fall and rise time, respectively. However, the dv/dt is increased when considering the higher voltage going from 4 V/ns at 100 V to 5.3 V/ns at 400 V considering turn-off and 2 V/ns at 100 V to 3.2 V/ns at 400 V considering turn-on. The turn-on is generally slower. However, as this is a no-load case, the load current effect is expected to influence significantly. This influence will, therefore, be studied further during load conditions later in this chapter. Finally, the experimental measurement is compared to the simulation model it order to validate its accuracy. The comparison is shown for the collector-emitter voltage in Fig. 4.18.

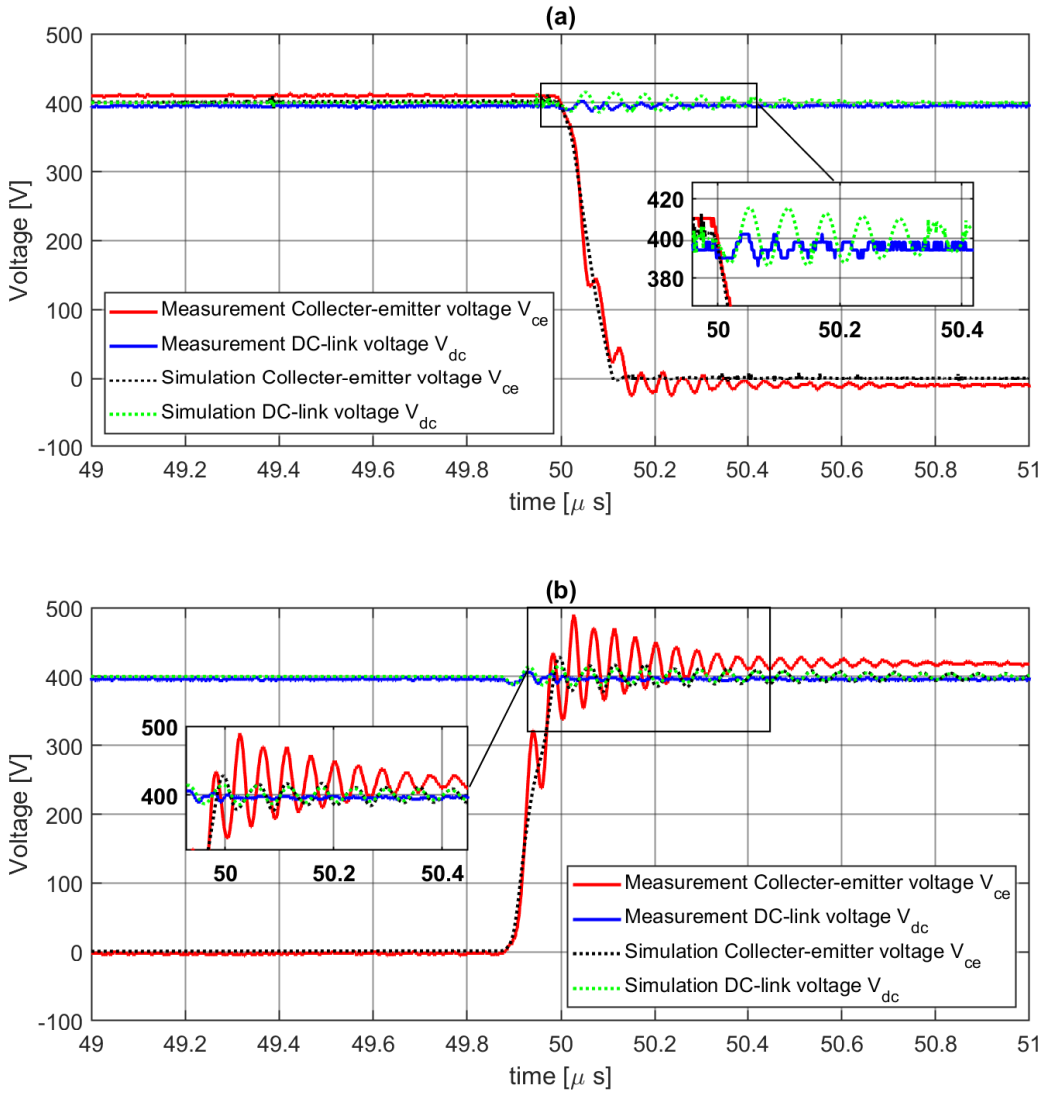


Figure 4.18: SM IGBT collector-emitter voltage at 400 V DC-link simulation compared to real measurements where (a) is turn-on and (b) is turn-off.

As it can be seen in the plot in Fig. 4.18, the simulation and measurements have some differences. Focusing on the DC-link, which was modelled earlier, it can be seen that lower voltage ringing is obtained in the measurement for both turn-on and turn-off compared to the simulation, meaning that the simulation slightly overestimates the voltage ringing. Therefore, dimensioning the SM using the simulation for the maximum overshoot is a conservative model. The oscillations are considerably higher than the simulation considering the collector-emitter voltage. One reason could be that for the output, only the internal parasitics in the power module are induced from the datasheet [18]. The external connection bars seen earlier in Fig. 2.48, include additional inductance along with measurement cables and probes. Similarly to the earlier discussion, no-load current is included; hence the influence of parasitics at high di/dt and reverse recovery is not evaluated in this simulation. A comparison considering the load current effect follows in test mode 2 results to finally evaluate the model.

Open-loop load mapping verification

The second objective of the first test mode of the SM is to verify the load mapping presented in Section 3.2.1. This test is carried out under no-load conditions to verify that the SM can reproduce the required switching pattern to generate a desired current waveform. This test is important to validate the open-loop control performance to know if the reference leads to the same PWM duty cycles and, therefore, later load current. If the operation is different than expected, it can lead to a distorted or even destructive output current. The mapping is verified by comparing the SM prototype voltage output to the simulation results used for obtaining the load mapping result in Fig. 3.7. The results of interest which should be extracted from these measurements are, therefore, the verification of the different working points which can

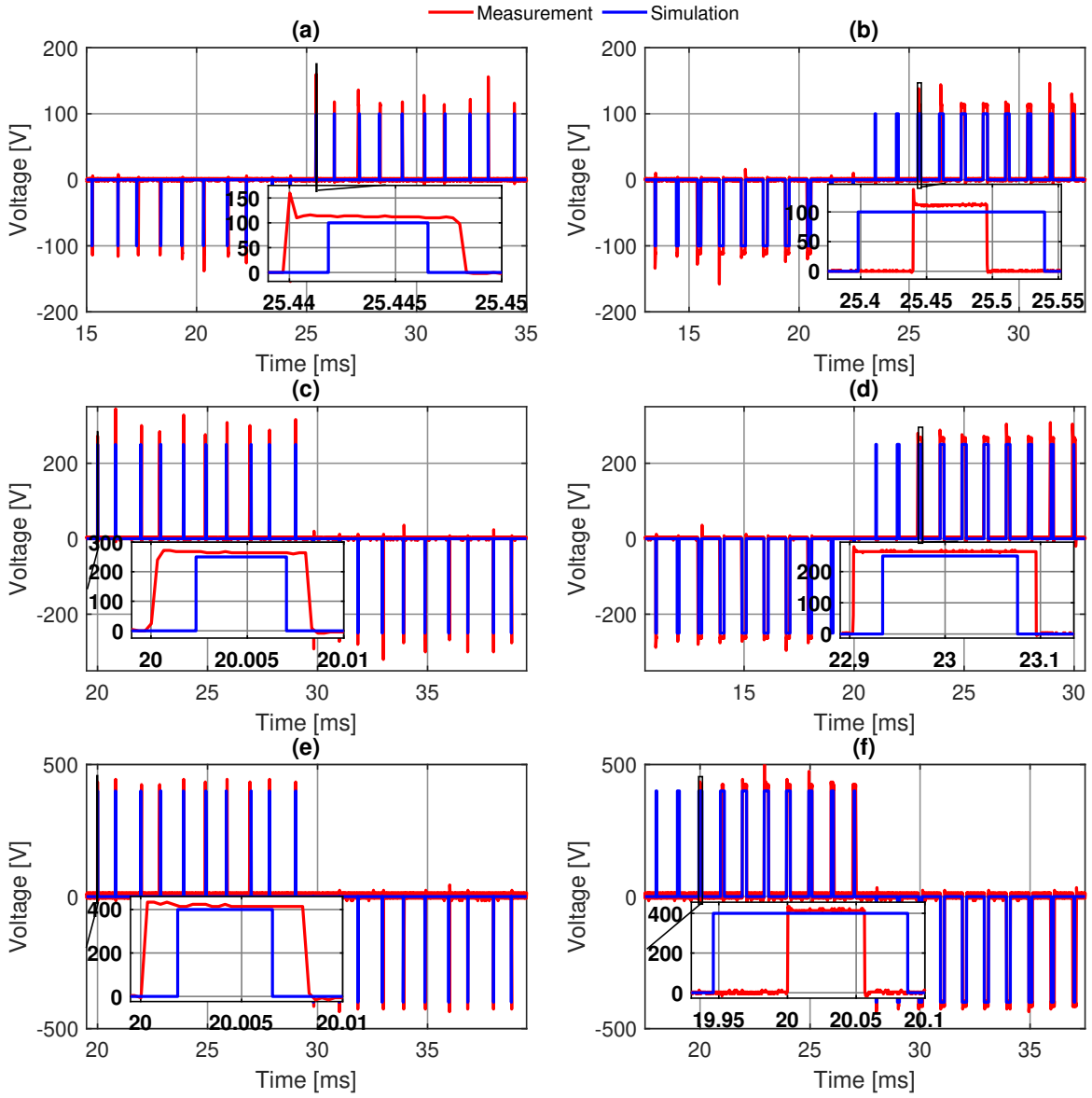


Figure 4.19: Comparison between measurement and simulation results of SM Test mode 1. (a) m_a=0.2, ϕ=10°; (b) m_a=0.2, ϕ=180°at V_{dc}=100 V. (c) m_a=0.2, ϕ=10°; (d) m_a=0.2, ϕ=180°at V_{dc}=250 V. (e) m_a=0.2, ϕ=10°; (f) m_a=0.2, ϕ=180°at V_{dc}=400 V.

fulfil the minimum duty cycle criteria imposed by the real setup, introduced in Section 3.2.1 where 650 ns was assumed the minimum on-time.
As an initial step, the experimental and simulation results are plotted to show the similarities between them. This is done for three different DC-link voltage levels, 100, 250, and 400 V, with an amplitude modulation index of 0.2 and a minimum and maximum reference signal phase shift of 10 and 180°. The corresponding results are presented in Fig. 4.19. From these results, some differences can be observed between the simulation and the SM measurements. First, the voltage pulses do not occur exactly at the same time or have the same width. These can be attributed to the power module material properties, time delays in the PWM transmission from the control board to the gate driver and the absence of dead-time between upper and lower switches in simulation. All these can affect the PWM pulses time duration compared to the simulation case. Secondly, the experimental results show voltage overshoots due to the SM power hardware parasitics, which are not included in the simulation for the load inductor mapping. Therefore, the mapping done by simulation needs to be verified with the real power hardware constraints to find possible limitations of the working points. Therefore, the mapping presented in Fig. 3.7 is re-evaluated based on test measurements. The test is conducted following the different test condition points described in Table 3.5 and checking if the shortest SM output voltage pulse has equal or larger duration than the required minimum duty cycle. To illustrate this, the different tested points are plotted on top of Fig. 3.7, which can be seen in Fig. 4.20.

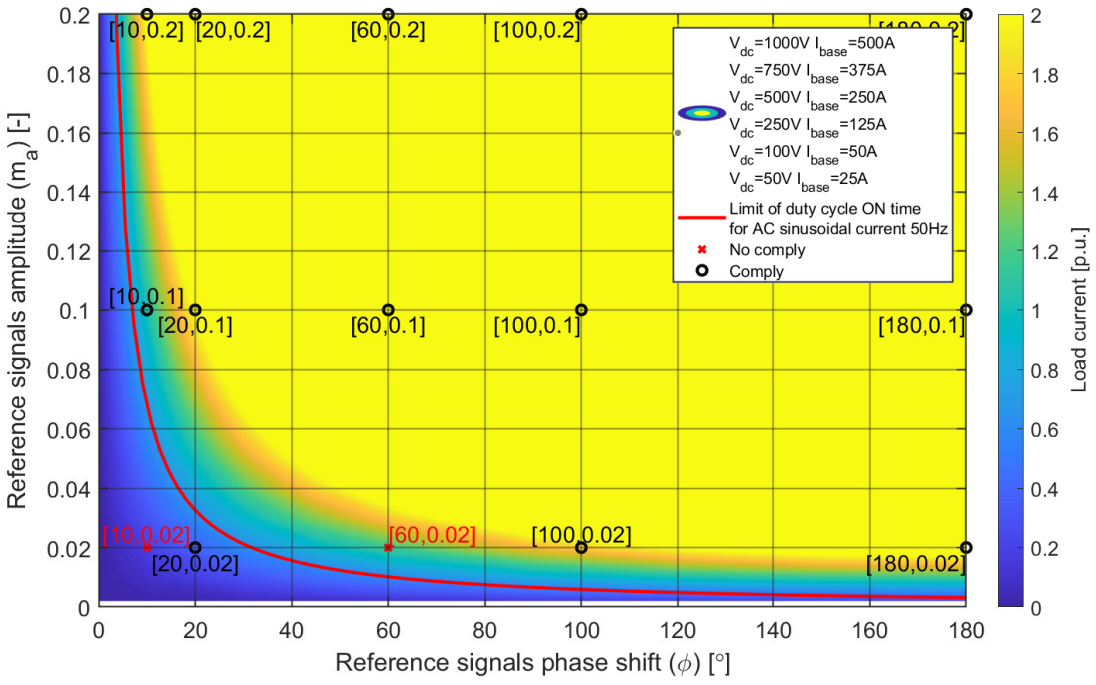


Figure 4.20: Tested points for evaluation of open-loop control for different maximum load current cases based on the result presented in Fig. 3.7.

From Fig. 4.20, it can be seen how most of the points specified in Table 3.5 comply with the minimum duty cycle criteria; however, several points should be analysed in greater detail. First, the point [0.02,60°] that in simulation satisfied the minimum duty cycle requirement is found dissatisfactory experimentally and can, therefore, not be used. Additionally, points on

the left side of the red line, which marks the theoretical limit of the minimum duty cycle for the working points, are of particular interest. It can be observed in the left side of the red line in Fig. 4.20 how there are points such as [0.02,20°] that, when tested on the SM prototype, comply with the imposed minimum duty cycle requirement, which theoretically should not be the case. This difference indicates that the hardware physical properties may differ from those considered in simulation from the power module datasheet. Further, the dead-time is not considered in the simulation case, which can also affect the PWM pulses width. The deviations presented have a clear effect on the allowed working points and justify the difference shown in the figure. Additionally, it can also be seen how there are points that do not comply with the experimental results as was expected from the load mapping, such as [0.02,10°], which was already below the criteria boundary (left of the red line).

Fig. 4.21 shows an example of a voltage pulse that does not comply with the minimum duty cycle criteria. This measurement is obtained with a reference signal amplitude of 0.005 and a phase shift between the two HBs references of 10°. From the figure, it can be seen how the output voltage rises to the V_{dc} value, 400 V in this case, after the turn-on pulse and, immediately, it is turned off. The resulting waveform is a triangular pulse instead of a rectangular one, which would lead to a wrong and limited current rise.

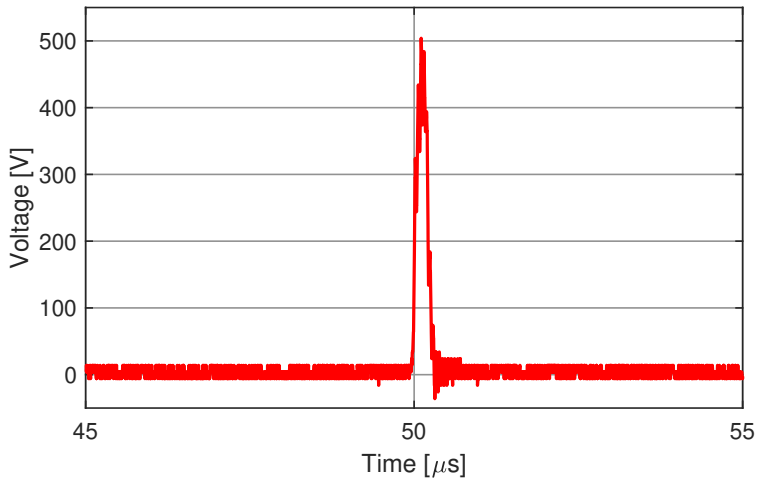


Figure 4.21: Example of an output voltage pulse not complying the minimum duty cycle requirement. m_a=0.005, ϕ=10°.

From this re-evaluation of the load mapping, the open-loop control is checked and validated. Next, the SM need to be tested under load current conditions to justify the load mapping before the load test.

4.2.2 Test mode 2: Load

This section presents the results related to the test under load, hence applying load current while performing relevant tests. As a reminder, the test conducted in this section is made to verify the operation of the SM considering electrical transient switching and thermal heat run. Firstly, a validation of the load mapping for open-loop control is validated to ensure controllability during a test.

Open-loop load mapping validation

In the previous section, several points of the mapping were verified in test mode 1 to fulfil the minimum duty cycle limited by the power module properties, however, with the expected load inductor value assumption. In this section, the points in the mapping are further verified from the current measurements obtained during the test to conclude the load mapping for the open-loop control.
The first test is conducted to verify that the current level on the SM prototype behaves as in simulation. A test is done with a DC-link voltage of 400 V, and the open-loop control parameters are chosen to be m_a=0.4 and ϕ=7°to compare the simulation and experimental results. The corresponding results are presented in Fig. 4.22 where the plot (a) shows the experimental results and (b) the result obtained from simulation.

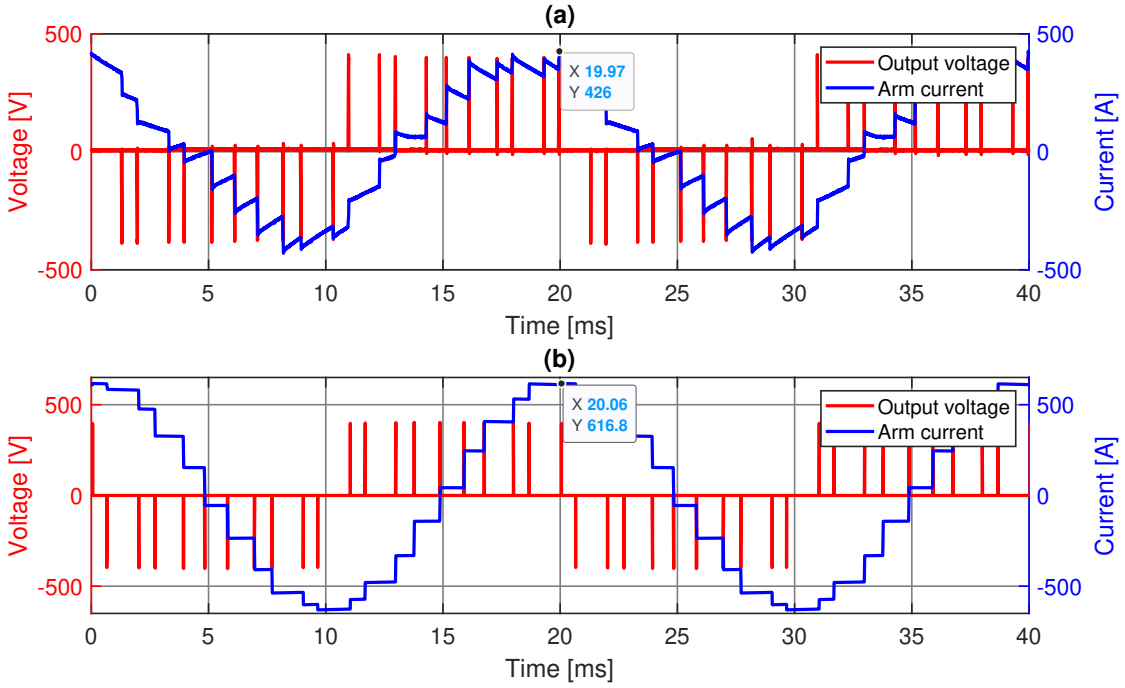


Figure 4.22: Comparison between experimental and simulation results of SM Test mode 2 at V_{dc}=400 V and I_{arm}=440 A. (a) Experimental measurement. (b) Simulation result.

Figs. 4.22a and 4.22b have similar current waveforms, however, these differ when observing their maximum current peak values. The experimental result value is found to be 426 A, while the simulation result is 617 A. This difference is assumed to be due to two main reasons. First, comparing the duty cycle values between experimental and simulation results, the latter shows higher pulse width values, leading to a higher current increase over time. Additionally, the test setup is expected to have a larger total load inductor as the connection cables are left out of the simulation for simplicity, potentially introducing 5 to 10 μH from a rough estimation of similar sized cables. This additional inductance adds to the load inductance value; therefore, a lower output current is expected in the experimental case, as observed. Furthermore, from Fig. 4.22a, it can be seen how the load current has a higher discharging rate than the simulation case. The reason for that is that the simulation has considered ideal switching components as PLECS is originally intended to verify the whole system performance,

especially the open-loop control dynamics, leaving the detailed electrical characteristics for the model developed in LTspice, as introduced in Section 2.3. However, the power module parameters are present in the experimental test and, therefore, should also be considered in PLECS simulation to achieve a more accurate comparison. Including the main parameters of IGBT and diode, mainly forward voltage and on-resistance, the result in Fig. 4.23.

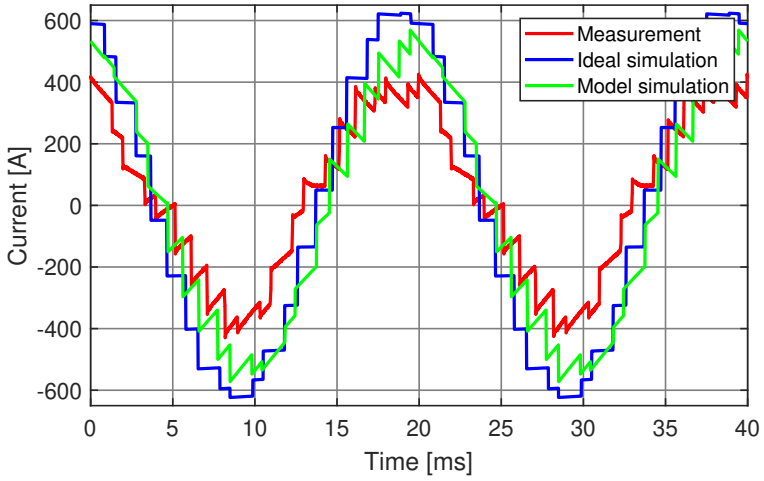


Figure 4.23: Output current waveform comparison between experimental and simulation results of SM Test mode 2 at V_{dc}=400 V and I_{arm}=440 A, considering ideal and modelled switching devices in simulation.

From Fig. 4.23, it can be seen that including the mentioned parameters in the PLECS simulation (green waveform), the simulation result resembles more to the one obtained experimentally (red line). However, the peak value is still higher in simulation due to the mentioned reasons.

Continuing with the mapping investigation, the plot given in Fig. 3.7 shows how different combinations of amplitudes (m_a) and phase shift (ϕ) can lead to different load current cases (in p.u.), which depend on the applied DC-link voltage as it defines the base current value for the available 54 μH inductor. A test case is conducted to verify the load current dependency on the DC voltage, where the open-loop parameters are kept constant, and two different DC-link voltage levels are applied to the SM. The results for 250 and 400 V, respectively are shown in Fig. 4.24. From Fig. 4.24a, considering the stated open-loop control conditions, a peak current of 274 A is obtained for a DC-link voltage of 250 V. For this case, the base current (1 p.u.) corresponds to 125 A (from Fig. 3.7). Therefore, a per unit value of 274/125 = 2.19 is found for these test conditions. Similarly, for the 400 V case in Fig. 4.24b, 426 A is the obtained peak current measurement, which for a base current of 200 A leads to 426/200 = 2.13. This result proves that the load mapping plot can be used for any test, independent of the DC-link voltage, only paying attention to the corresponding base current to know the maximum current that can be obtained for each voltage.

Finally, as indicated in the test mode 2 descriptions given in Table 3.6, different current points are intended to be tested for verifying both the switching characteristics and the thermal model of the SM. These points, which results are presented in the following sections, are illustrated in the current mapping shown in Fig. 4.25 for a case of 400 V DC-link, as it is the highest test condition which is used for the heat run test. Both simulation and experimental measurements are presented in the plot concerning each point. Comparing the current values

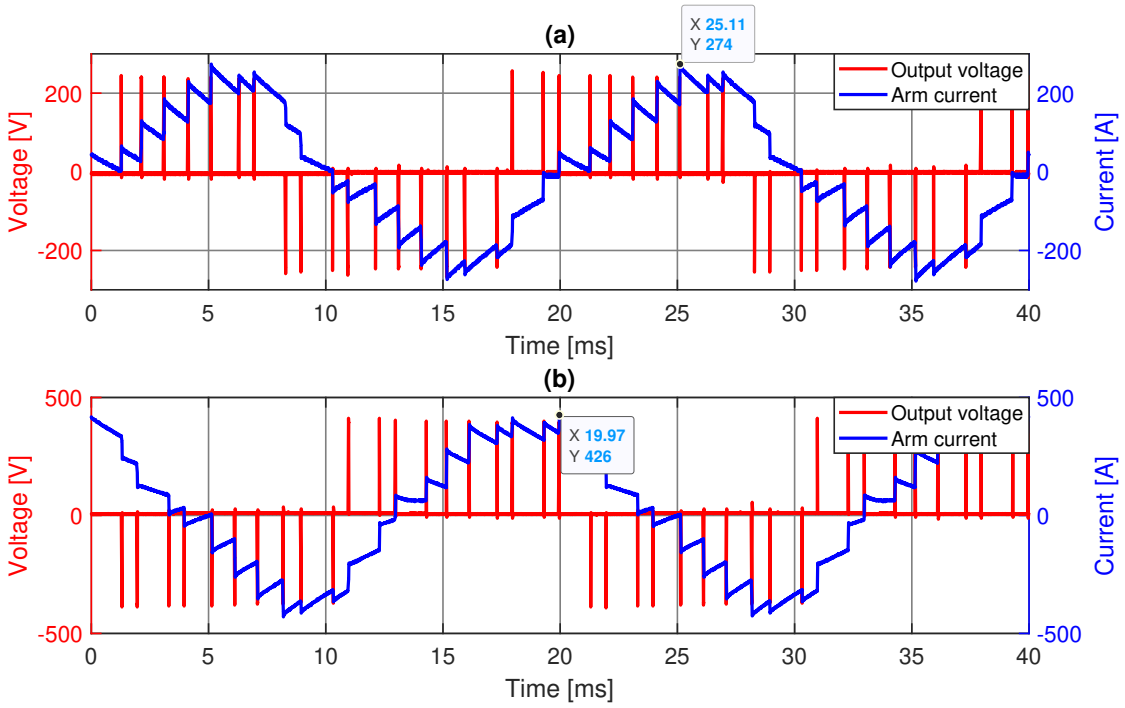


Figure 4.24: Verification of current dependency on the DC-link voltage for the same open-loop conditions (m_a=0.4 and ϕ=7°). (a) Experimental measurement with V_{dc}=250 V. (b) Experimental measurement with V_{dc}=400 V.

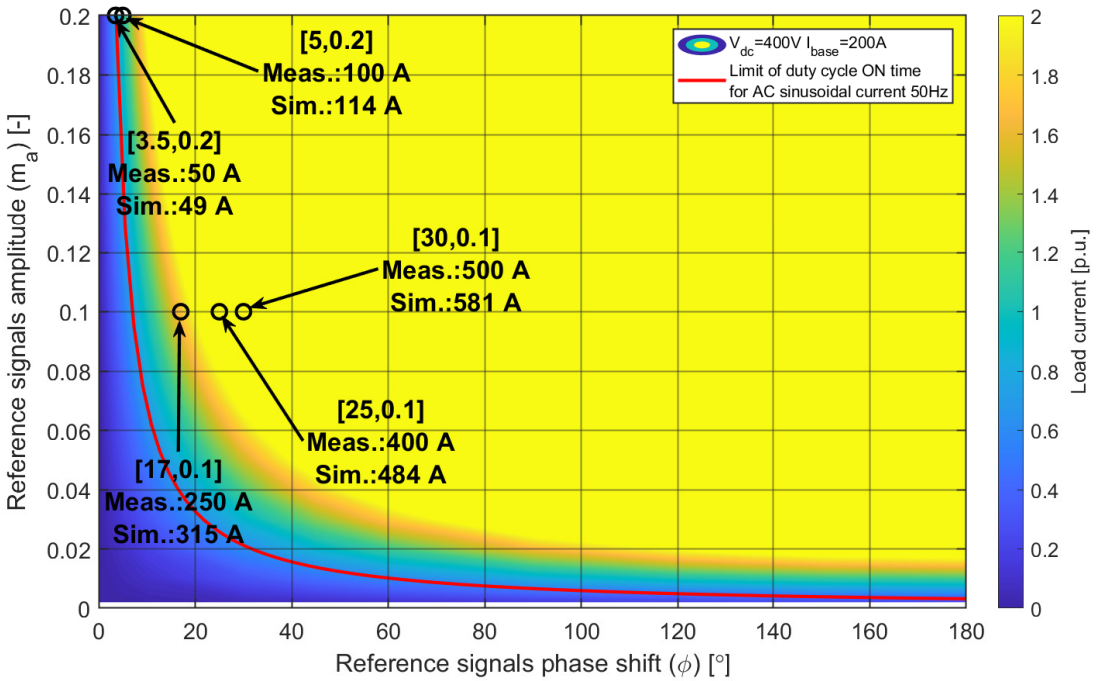


Figure 4.25: Load current mapping for test mode 2 current points, according to the test description in Table 3.6, for a DC-link voltage of 400 V.

given in the figure shows how at lower currents, the measurement and simulation show a closer match. However, as the current increases, the difference between simulated and tested

values is also increasing. The points to obtain the load current of interest are therefore adjusted to fit the real test setup and create the foundation for the load map to be used in the following test cases, which will be more precise than the more conservative simulation. From the establishment of the load mapping, the open-loop references needed are obtained hence, the electrical and thermal tests can be conducted, which are presented below.

Transient switching analysis - load

In continuation of the discussion of the SM design's switching characteristics during no-load, a similar test is conducted at the load points described in 3.6 for DC-link voltages of 100 V, 250 V and 400 V while applying various load currents. Starting at a lower voltage and current, test results are shown in Fig. 4.26 for a DC-link of 100 V, applying a 50 Hz current with an amplitude of 50 A peak. It should be mentioned that it is not possible to measure the collector current due to the compact design of the busbar and the size of current probes. The reverse recovery can, therefore, not be validated. The results used for the model from the test in [23] for the same power module, therefore, need to create evidence for this part

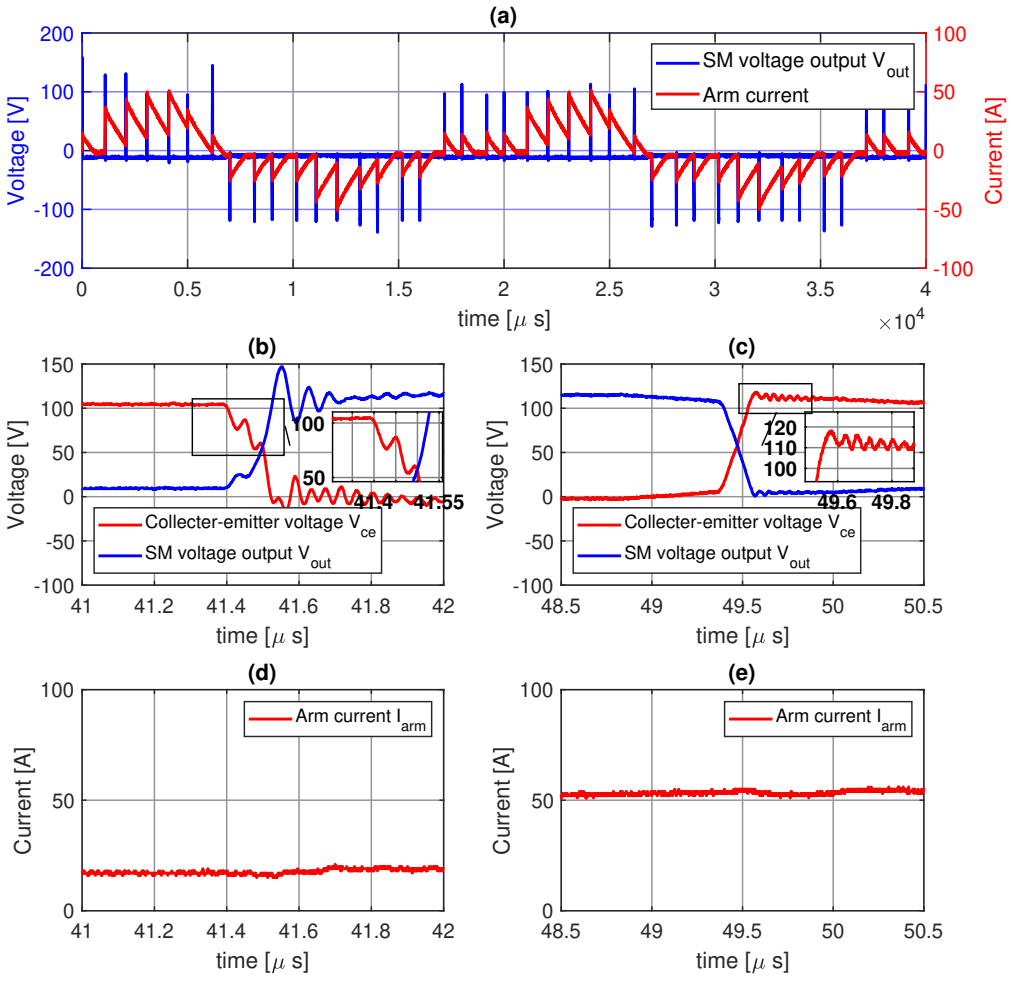


Figure 4.26: SM switching characteristics at 100 V DC and 50 A peak 50 Hz current.

of the model verification. From the result, it can be seen that applying load current leads to different characteristics compared to the no-load case, as expected from the simulation. Fig. 4.26b shows the turn-on where the influence of the parasitic inductance is pronounced by creating a voltage drop due to the di/dt. Similarly, for the turn-off in Fig. 4.26c, an overshoot is obtained. The effect is, however, still small since the current is low at this stage. Next, the voltage is increased to the maximum possible voltage of 400 V DC in Fig. 4.27, considering the protection noise problem.

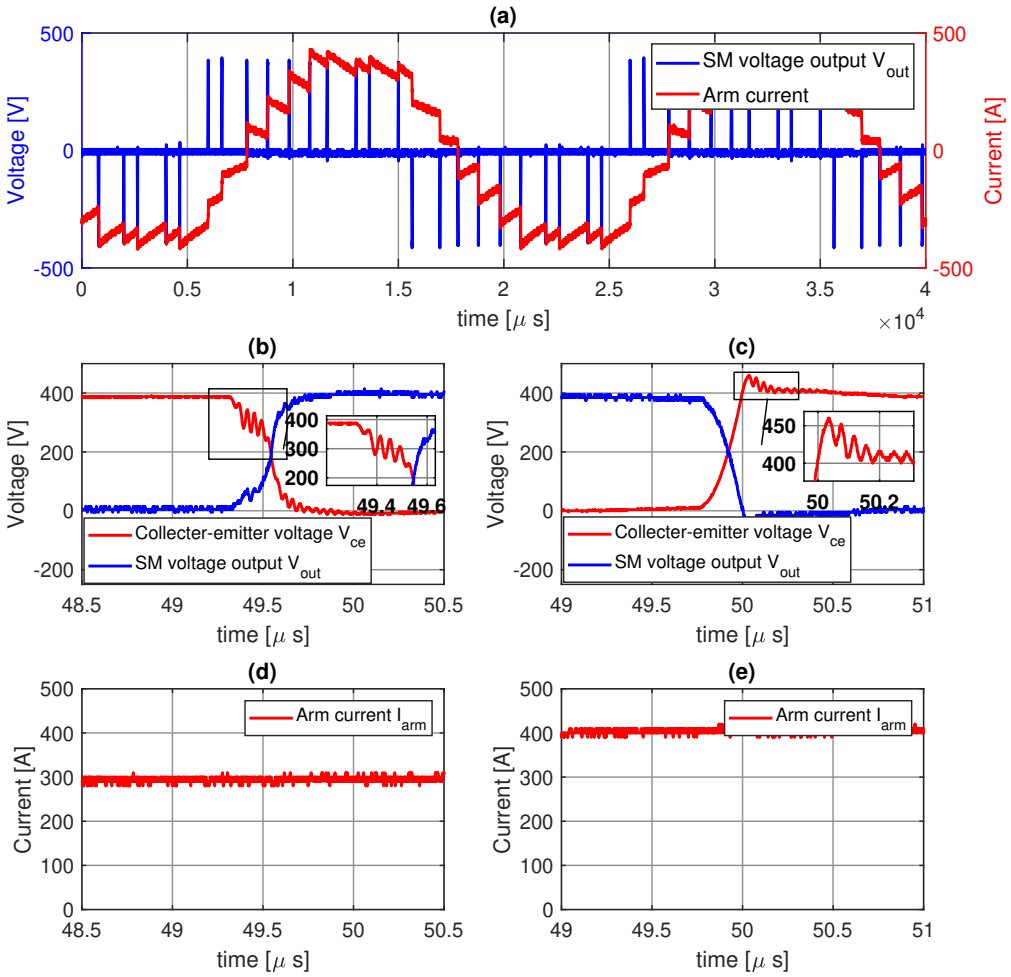


Figure 4.27: SM switching characteristics at 400 V DC and 400 A peak 50 Hz current.

After increasing the voltage, the current is increased to the maximum allowed between 400-500 A peak. In this maximum operation state, the voltage overshoot during turn-off is increased to approximately 60 V, leading to an overshoot of 15%, still within the maximum allowed. Further, the voltage drop is now more pronounced due to the high di/dt. This test, therefore, verifies that the switching characteristics of the design are acceptable. To analyse the different load cases, the collector-emitter voltage is shown in greater detail for turn-on in Fig. 4.28a and turn-off in Fig. 4.28b.

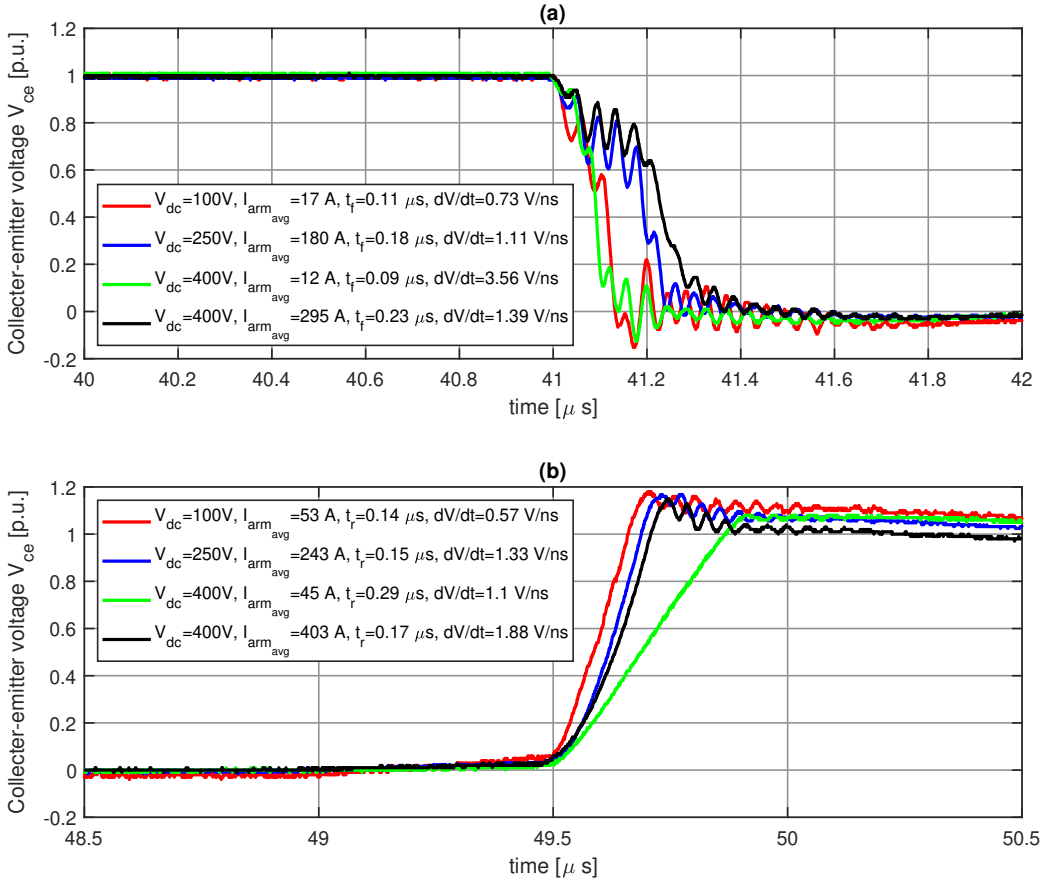


Figure 4.28: Collector-emitter voltage at various DC-link voltages, normalized to per unit using V_{dc} as base value, and current levels ($I_{arm_{avg}}$: current average of the 2 μs plotted).

Focusing on the turn-on in Fig. 4.28a, it can be seen that increasing both the DC-link voltage and current affect the fall time and, thereby, the dv/dt. Increasing DC voltage from 100 V to 400 V, keeping a low load current, increases the fall time from 0.11 μs to 0.09 μs. The fall time is not greatly increased; however, as this fall time is at four times the voltage, the dv/dt is increased from 0.73 V/ns to 3.56 V/ns. However, when increasing the load current from 12 A to 295 A, the fall time increases from 0.09 μs to 0.23 μs, decreasing the dv/dt to 1.39 V/ns. Next, observing the turn-off in Fig. 4.28b, both voltage and current increase the rise time considering the voltage magnitude and dv/dt. Here the dv/dt is increased from 0.57 V/ns to 1.88 V/ns when going from lowest voltage and current to highest. In general, for all results, a faster turn-on and turn-off time is found when the load current is applied. The reason can be the higher di/dt influencing the voltage due to the parasitic inductances.
Next, the simulation model is compared to the real measurement in Fig. 4.29.

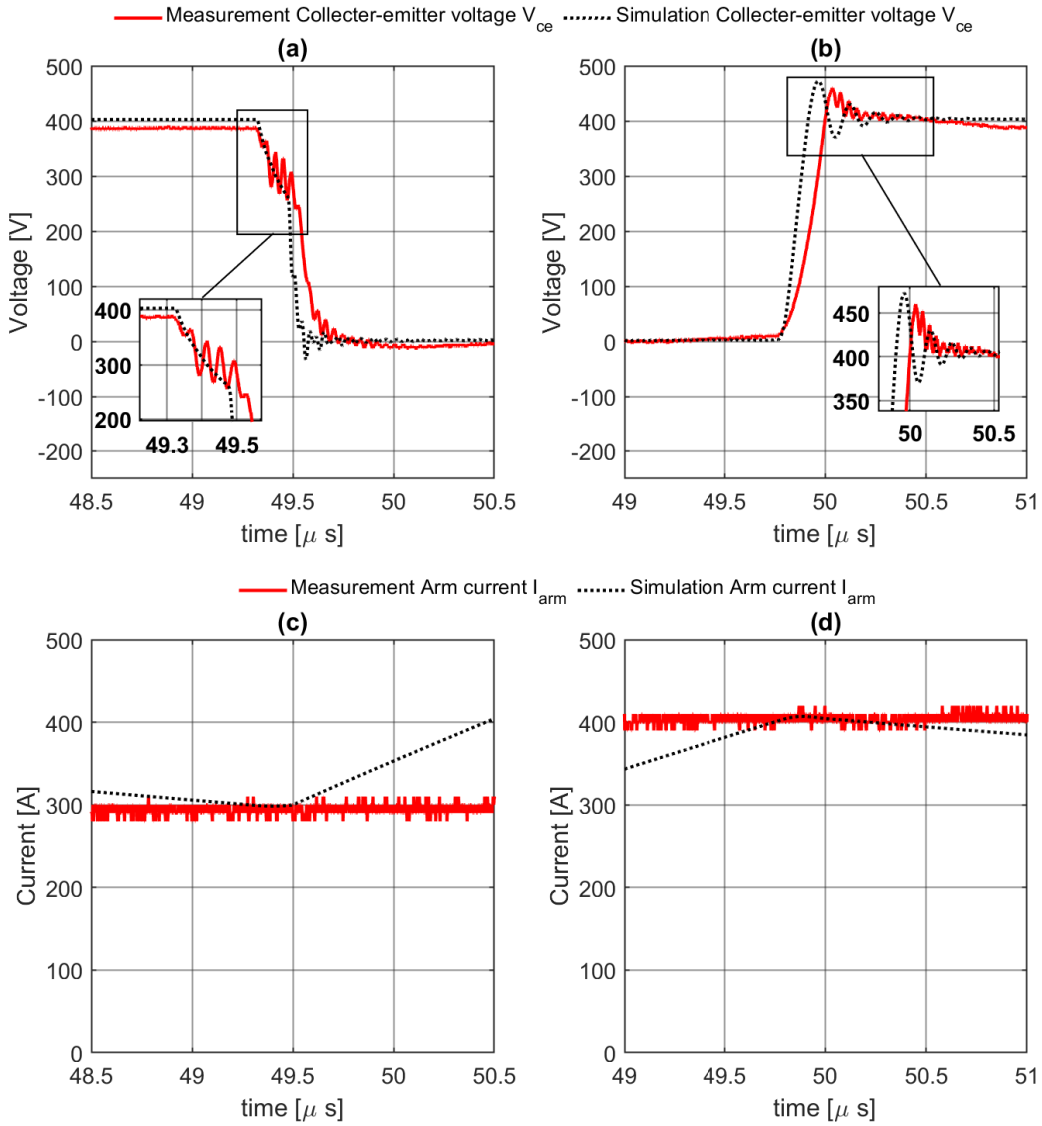


Figure 4.29: SM IGBT collector-emitter voltage at 400 V DC-link simulation compared to real measurements with a load current of 400 A for turn-off and 300 A for turn-on.

From Figs. 4.29a and c, the corresponding turn-on collector-emitter voltage and total current can be seen. The collector current is not shown as it is not possible to be measured as earlier mentioned. However, the output current is similar; however, the current rise after turn-on shows a different rate as lower inductance is considered in simulation due to computational limitations. From the turn-on, it can be seen that a similar characteristic is obtained. The effect of parasitic inductance is similar; however, the ringing is more dominant on the experimental measurement, especially at the beginning of the turn-on process. The reason could be that the output inductance has now further increased as components such as cables are not modelled, similar to the discussion in the no-load test. Further, the turn-on time of the collector-emitter voltage is slightly faster in simulation than the measurement, where the simulation shows a fall time of 170 ns compared to 270 ns in the measurement. This case also corresponds to 1.9 V/ns in simulation while 1.2 V/ns in the measurement. For the turn-off case, Figs. 4.29b and

d, the turn-off time is again faster in the simulation, where the simulation shows a fall time of 100 ns compared to 160 ns in the measurement. This case also corresponds to 3.2 V/ns in simulation while 2 V/ns in the measurement. The peak overshoot voltage has a similar magnitude; however, more dominant ringing is seen in the simulation. These differences can improve the model; however, the result is quite close to the measurement. The simulation has given valuable results before the prototype stage for the preliminary design evaluation for evaluation of the design.

Thermal analysis

After analysing the electrical properties of the SM, the main property pending for test is the thermal circuit which needs to ensure that the SM can operate at rated conditions by removing the heat, hence, keeping the power modules temperature within their safe operating area. Additionally, some natural cooled components such as capacitors and test inductor are measured to avoid overheating. All temperature measurements obtained are presented in Fig.

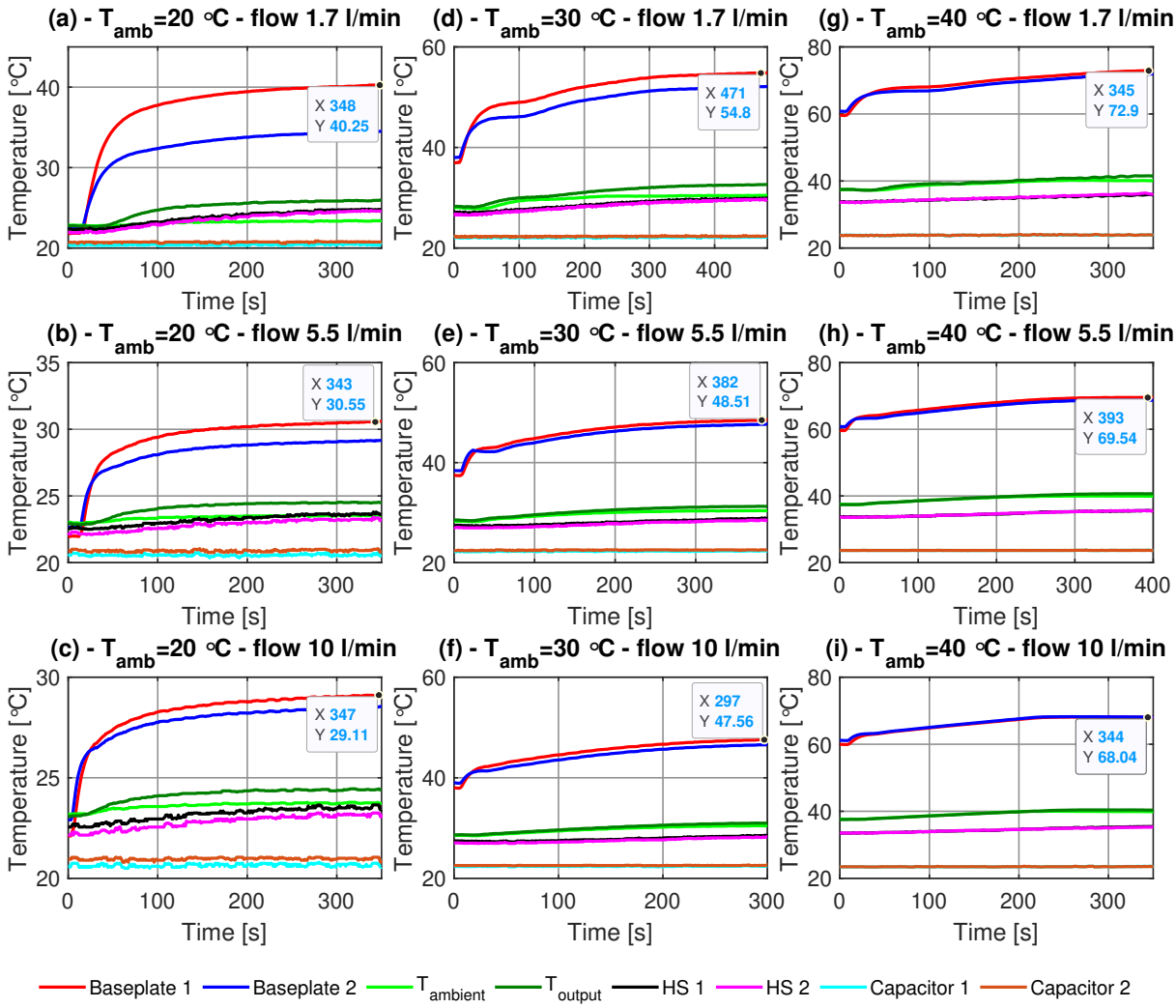


Figure 4.30: SM thermal characteristics - temperatures responses at DC-link voltage of 400 V DC and 50 Hz 500 A peak AC current.

4.30 showing the temperature rise in various operation conditions; three water flows to achieve different thermal resistance, namely 1.7, 5.5 and 10 l/min, and three ambient temperatures, namely 20°C, 30°C and 40°C. The essential values of these temperature measurements are the final steady-state value used further in this study, while the transient characteristics are of less importance. Further, the ambient temperature of 20°C is taken as the lowest water temperature available. However, this could probably not be used in a real application due to condensation, as mentioned in the design chapter. In this study, the electrical operation point is maintained constant using a reference from the open-loop control mapping that leads to a 500 A peak current defined as maximum operation. The power loss which leads to these temperature increases, their corresponding temperature rise of outlet water temperature, and ambient water are presented in Fig. 4.31. It can be seen that the temperature losses are kept more or less constant during the operation. It should be mentioned at this point that the active power losses include all SM losses and not only the switching losses. However, it is assumed that most losses originate from the switching and conduction losses of the power modules and minimal losses from capacitor ESR and busbar ohmic losses. Further, the load

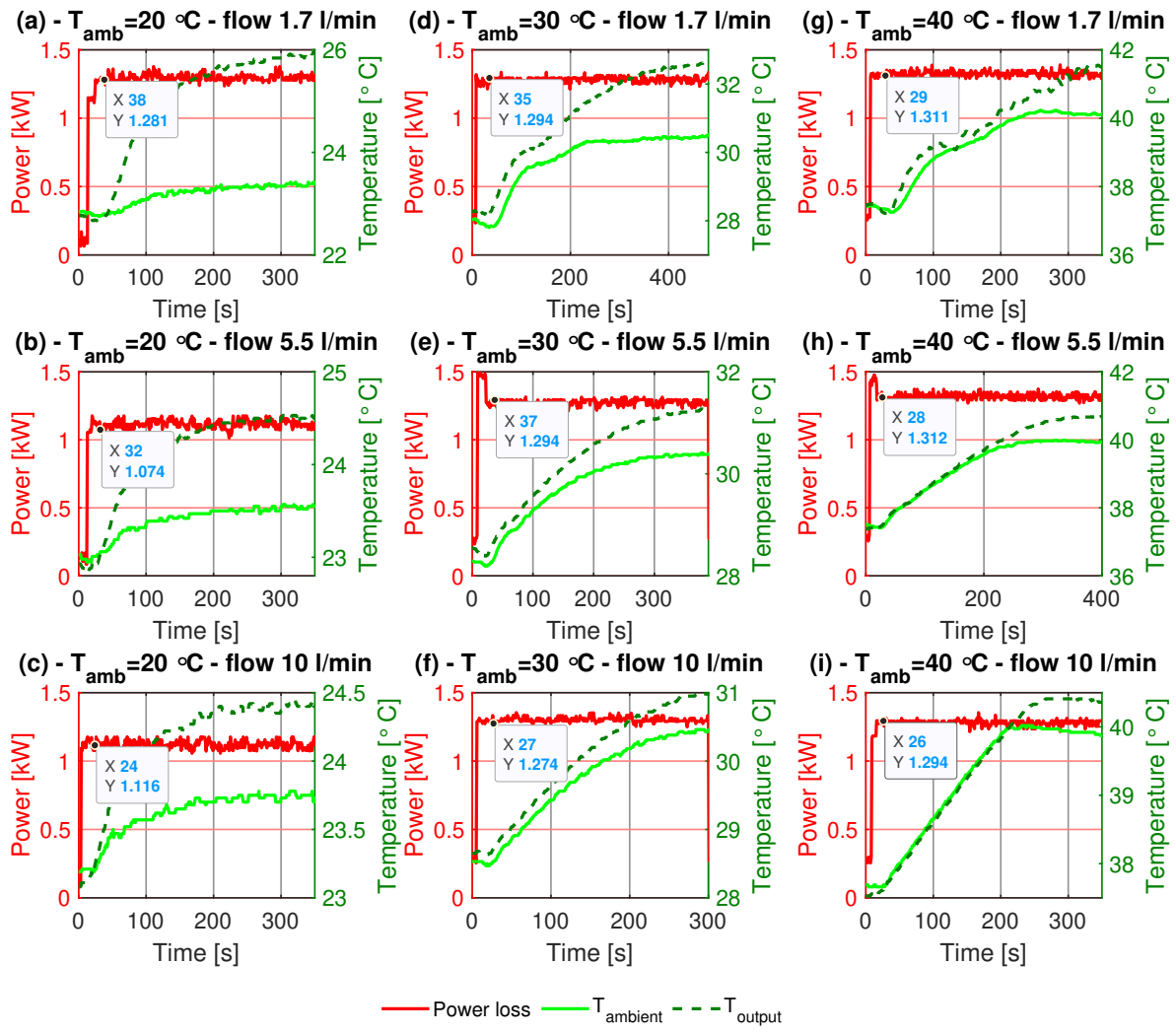


Figure 4.31: SM thermal characteristics - loss responses at DC-link voltage of 400 V DC and 50 Hz 500 A peak AC current.

inductor ohmic losses are included, but due to its low winding resistance in Table 3.1, it should not lead to a large influence. From the results, different operation conditions lead to slightly different power losses. Some reasons for this could be that higher temperatures lead to higher losses due to the temperature dependencies of power modules and resistances. The temperature rises of the heated output water depend on both flow and ambient temperature, where lower flow and higher ambient temperatures lead to higher differential temperature. This dependency is further studied in the following discussion of these results.
First, one random transient baseplate temperature is compared to the simulation model used for the design. In this case, a 20°C baseplate with a flow of 1.7 l/min is used in Fig. 4.32.

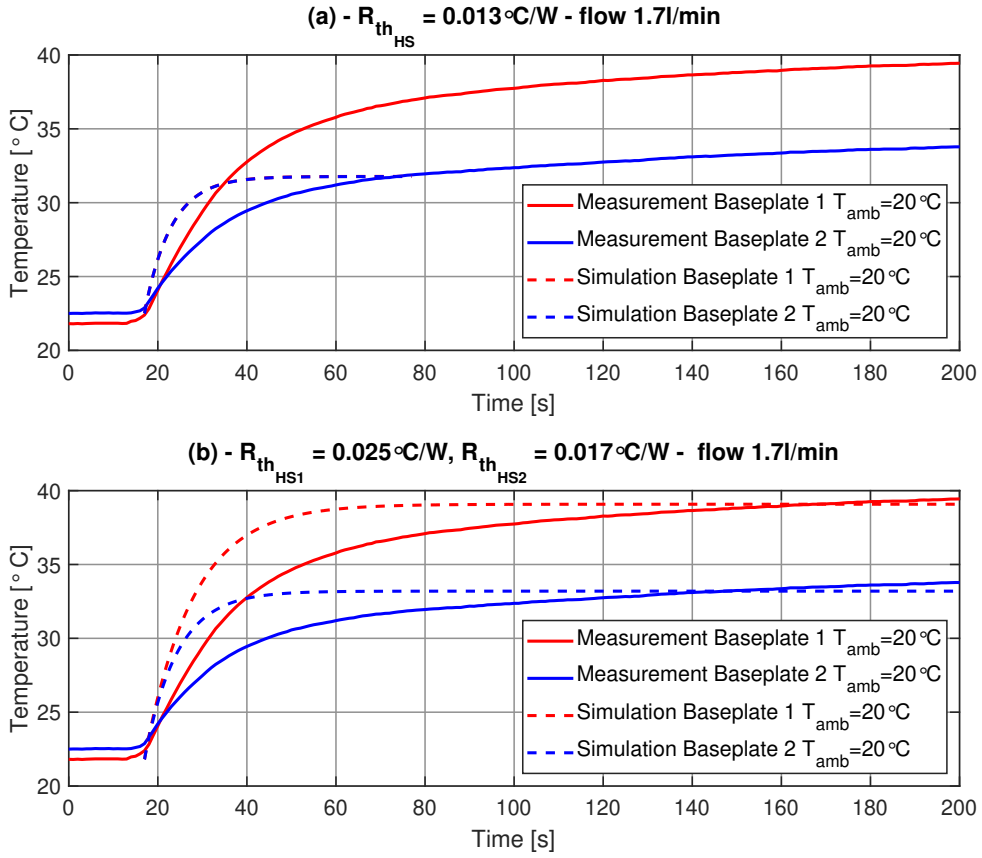


Figure 4.32: Transient temperature response at $T_{amb} = 20°C$ and flow of 1.7 l/min; (a) simulation with datasheet thermal resistance and (b) simulation with derived thermal resistance from measurement.

From Fig. 4.32a, it can be seen that the baseplate temperature measured inside the power modules shows slightly different temperatures with around 4°C difference. Further, compared to the simulation, where the temperatures are the same for both baseplates, the measurements show different steady-state temperatures. To analyse this further, the thermal resistance as a function of flow is derived in Fig. 4.33a from the corresponding power losses in 4.33b and differential temperature from baseplate to ambient temperature in 4.33c, assuming that the power losses are evenly distributed between the power modules. The inlet temperature is used for the ambient temperature, which could be slightly higher across the heat sink as the water is heated, creating some deviations from the simulation where it is considered constant. The flow is in all measurements measured depending on the pressure drop and using the

datasheet relation in Fig. 3.10. It is seen that the thermal resistance derived from the measurement is slightly higher than the one from the datasheet. Some reasons for this behaviour could be that the interface from the baseplate to the heatsink includes the thermal grease, which is not modelled in the simulation and could also include air voids, leading to increased temperatures. Further, the thermal resistance is rising depending on both lower flow and higher ambient water temperature. This result is expected as the thermal resistance depends on ambient water temperature and flow as discussed and modelled in [27]. In the design, a higher thermal resistance should therefore be expected, as seen in this discussion. The difference between baseplate 1 and baseplate 2 could be due to the slightly different pressure drop of the two baseplates, meaning that the flow is unevenly distributed from the manifold dividing the cooling water to the heat sinks. Further, the mounting of the power modules and slightly different power losses could have an impact. After using the obtained thermal resistances in 4.33 a simulation is conducted in 4.32b showing similar steady-state temperatures. The model transient response seems to be higher than expected, which could be due to the missing thermal capacitance of the heat sink only including thermal resistance as a function of flow in the datasheet. However, the thermal impedance and a more precise thermal impedance model, such as a Foster model, could be derived directly from the measurements if a more precise transient response would be of interest, e.g. cooling system response time, which will be discussed later.

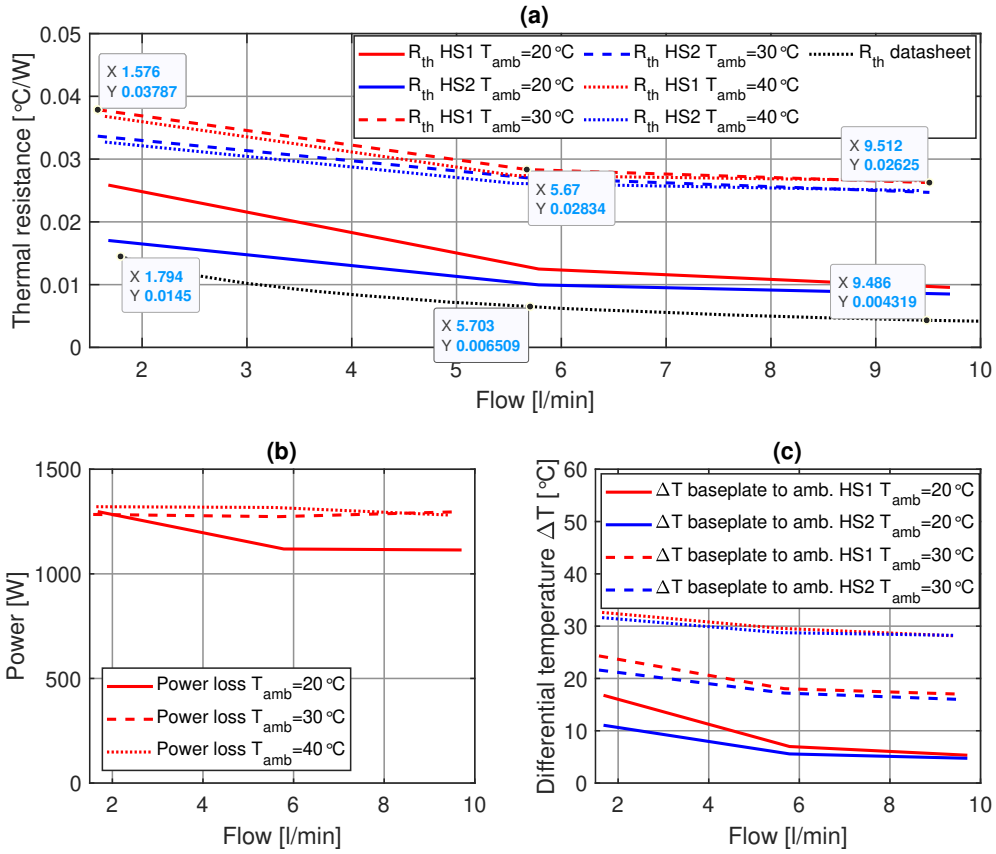


Figure 4.33: (a) Derived thermal resistance depending on flow, (b) corresponding total SM power losses, and (c) baseplate to ambient inlet temperature differential temperature.

Next, in order to further validate the design, the baseplate temperatures are given in 4.34a depending on flow and ambient water temperature.

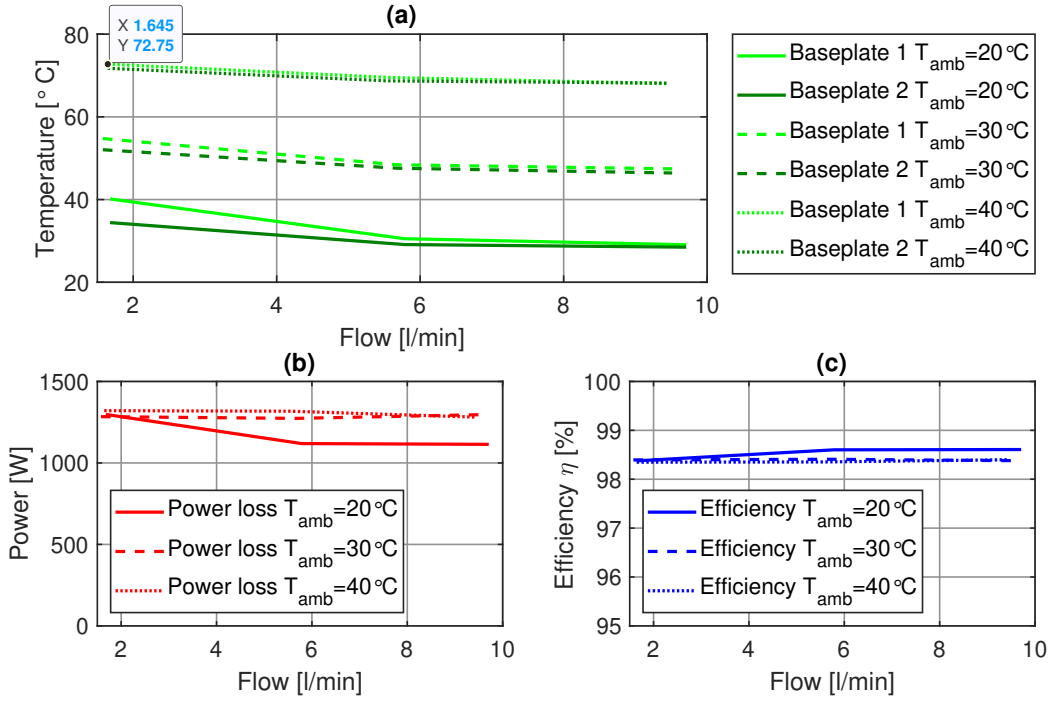


Figure 4.34: (a) Baseplate temperatures, (b) corresponding total SM power loss, and (c) estimated SM efficiency considering a maximum active power output of 100 kW made possible from a fundamental 400 V peak voltage and 400 A current.

As expected from the former discussion of thermal resistance, the temperatures decrease with higher flows and lower ambient temperatures. From the design chapter, it was found that the maximum temperature allowed on the baseplate would be around 77.6°C in (2.5), which includes a margin of 50°C of the IGBT and diode junction. At the maximum ambient water temperature and lowest flow, the maximum temperature reaches 72.7°C meaning that all operating conditions can be used. This result also corresponds to the thermal resistance of $0.038°C/W$, which is slightly above the maximum allowed in (2.5) of $0.035°C/W$. Therefore, higher ambient water temperatures and flows would not be possible considering the margin of 5°C left to the maximum temperature allowed. Further, this test is conducted with a 400 V DC link. If the full DC-link voltage of 1000 V was present, this could lead to slightly higher losses during switching. From the power losses, efficiency is derived in 4.34c. This efficiency is estimated assuming that at an operation of 500 A peak AC and 400 V peak AC, a power of 100 kW could be delivered from the SM having the same losses. This assumption would not be fully accurate as different duty cycles could lead to different conduction losses. The calculated efficiencies are around 98.5% for all cases as the power losses are similar and only small temperature dependence leads to small deviations. The efficiency is, therefore, around 1.5%, which is realistic for Si-based converters, as also studied in [75].
Finally, an analysis of the cooling system requirements is carried out. This analysis gives requirements for a future cooling system that will host multiple SMs in a complete MMC. Therefore, to size the complete cooling systems, the individual SM requirements are a necessity. Some requirements are given in Fig. 4.35.

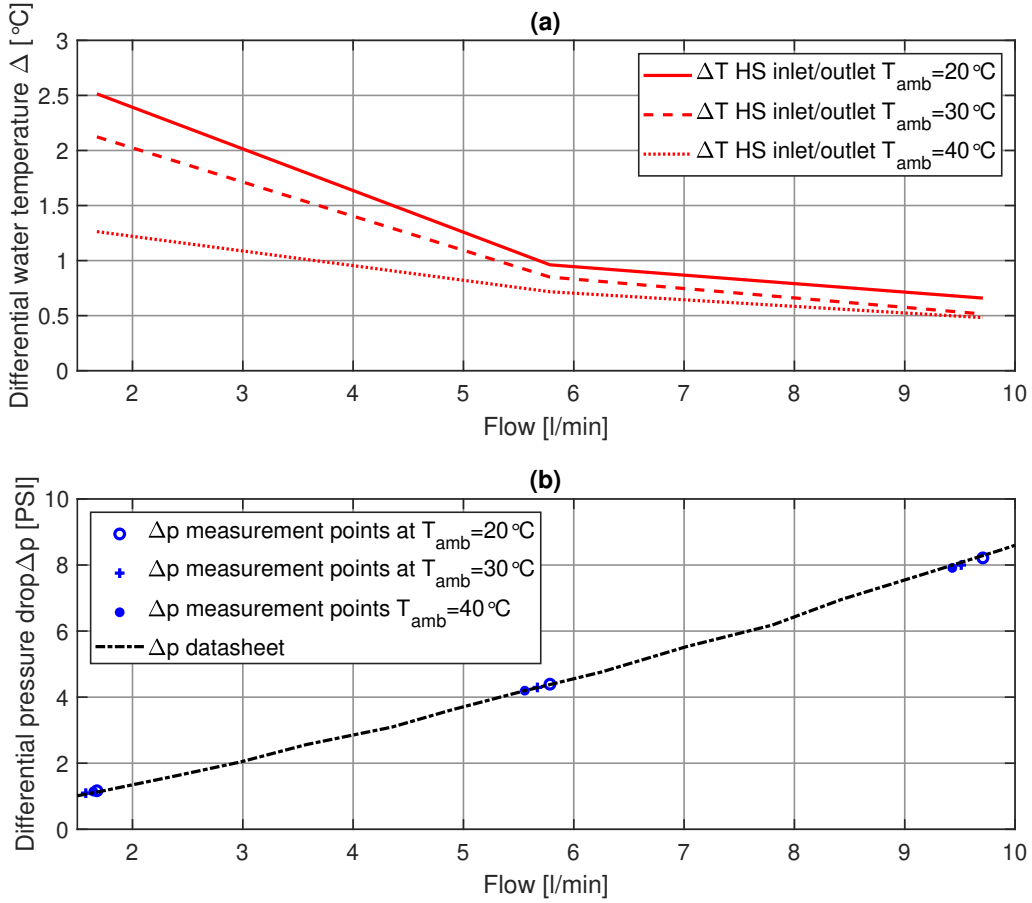
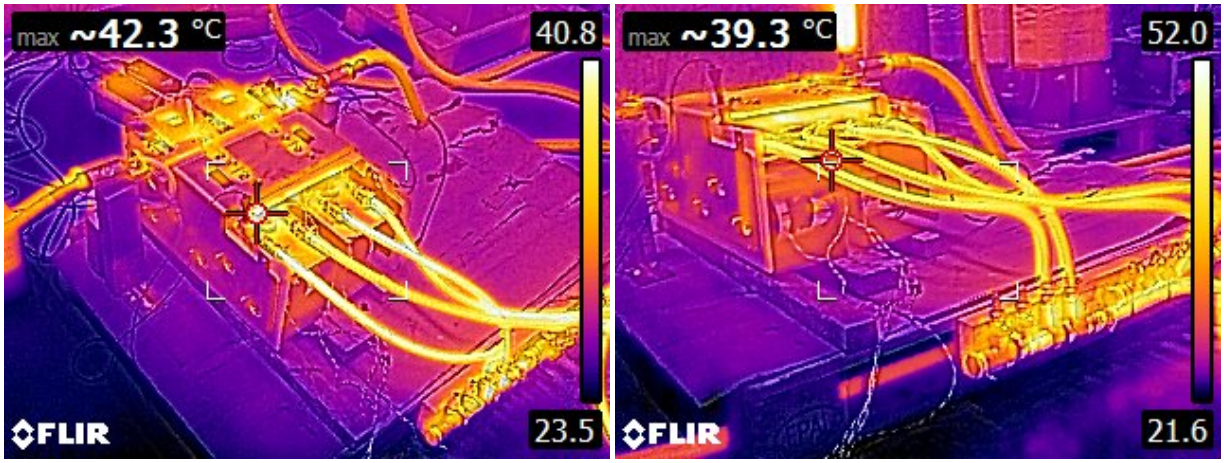


Figure 4.35: Cooling system requirements per SM

In Fig. 4.35a, the differential water temperature from the ambient input to the ambient output is presented as a function of flow. It can be seen that at lowest flow and lowest ambient temperature, the water is heated around 2.5°C. At higher ambient temperatures, the temperature rise is slightly lower as less heat travels to the water in time. As the 20°C case would probably not be used due to the discussed condensation problem. The requirement for a water cooling system ambient temperature would, therefore, be for the 30 °C or 40 °C case which are above the air ambient temperature in most areas. In Fig. 4.35b, the pressure drop as a function of flow is derived from the datasheet pressure-to-flow relation in Fig. 3.10. This requirement is important to size the cooling system pump power. The last requirement could be the transient case in Fig. 4.32, as the time constant of the SM form the model in which the cooling system needs to follow to avoid thermal overshoots.
Finally, to validate the temperature measurements, a thermal camera is used in all cases. One measurement for the highest temperature is shown in Fig. 4.36.



(a) Top picture. **(b)** Side picture.

Figure 4.36: Thermal camera measurement during $T_{amb} = 40°C$ and flow of 1.7 l/min.

It can be seen that the hot spot temperature is around 40°C fitting with the ambient temperature of 40°C. The heat sink surface is measured to be 35°C using a surface temperature sensor. However, with the deviations of this type of sensor, it is assumed to be within the tolerable range. In Fig. 4.36b, it can also be seen that one capacitor seems to have a slightly higher temperature on its terminals. However, this has not been studied in greater detail as the individual currents can not be measured. Still, the thermal camera measurement can give extra assurance of terminal connections as an addition to the total capacitance measurement performed during the commissioning.

4.3 Failure Modes

This section provides an update to the DFMEA table given in Section 2.2.1 based on the knowledge and results obtained during the experimental part of the thesis. From the results presented in the previous section, the main issue affecting the SM performance is the EMC/EMI problem detected during the commissioning phase, which leads to a lower signal-to-noise ratio. As mentioned in Section 4.1.1, the noise present in the analogue signals limits the maximum DC-link voltage allowed, which significantly reduces the SM operation. Therefore, the DFMEA given in Table 2.2 is expanded, including this phenomenon and the consequences related to it. It should be pointed out that none of the failure modes described originally in Section 2.2.1 show a failure, showing the effectiveness of the DFMEA method. Table 4.2 summarises the new failure modes obtained from the first iteration test and analysis. Once these failure modes are found, a deep analysis of these is needed for a future second iteration of the MMC SM design, giving rise to different improvements which are covered in the next section.

Table 4.2: SM DFMEA (updated).

Main item	Sub-item	Function	Potential Effect of Failure	Severity	Potential Cause of Failure	Occurrence	Current Design Controls	Detection	RPN	Recommended action
Control board	Power supply	Supplying rated power to different sensor, controllers, gate drivers, etc.	Switching noise worsening the signal-to-noise ratio	8	Wrong output filter	10	Tested during commissioning	2	160	Tune an appropriate filter Avoid switch-mode supplies
	PCB	Integrate and interconnect different components	Wrong operation of the SM	8	Faulty connection No noise immune layout	8	Tested during commissioning	2	128	Implement stricter EMC practices Perform Q3D and EMT analysis
	Analogue signals processing circuit	Convert sensor measurements to DSP allowed voltage levels	No controllability Undesired protection tripping	10	Low noise immunity	10	Tested during commissioning	2	200	Choose components with higher noise rejection Improving ICs supply filtering

4.4 Improvements

During the commissioning and testing phases of the first iteration of the MMC SM design proposed, different possible design optimisations, referred to as optimisation levellers, and some operational issues are found. This section provides a list of improvements for a second iteration of the SM design for mitigation of issues and optimisation levellers.

Starting with the noise problem presented in Section 4.1.1, an update of the control PCB is required. The PCB needs to be designed to present as low noise on the analogue signals as possible to improve the signal-to-noise ratio. Different measures can be adopted to achieve this. Analysing any EMI/EMC issue, three parts can be identified: an emitter, a receiver or victim, and the path between them. All of these contribute to the noise problem and, therefore, improvements can be made for each of them. Regarding the emitter, the isolated DC/DC power supplies are identified as the main noise source. As the PCB is already manufactured, there is no room for many changes. If the same power supplies are to be used in a future version, adding ferrite beads to the output can improve the filtering of the high-frequency signal. Further, in a future version, as it was mentioned in Section 2.4.2, the control PCB would be supplied from the DC-link. For this purpose, an isolated DC/DC converter is used to obtain the main supply voltage, which needs an appropriate output filter. The supply noise problem effort would, therefore, need to be made in this part. The rest of the voltage levels can then be obtained from LDOs, which have lower noise levels than switched power supplies [76], [77]. These measures would reduce the overall noise coming from the emitter. Op-amps with higher noise rejection should be chosen for the victim part, and the decoupling capacitor value on its supply can be increased. Finally, concerning the noise injection path or route, the overall PCB layout should be studied and improved to achieve a high noise immunity. As mentioned before, ferrite beads can be distributed in the power and ground tracks to filter their high-frequency components. Decoupling capacitors to the ground can also be added to long tracks to filter and stabilise the signal levels. The different grounds distribution shown in Fig. 2.36 needs to be modified, separating the noise-sensitive parts from the ones that can handle a higher EMI level. The analogue ground should be placed far from the power components, in this case, the gate driver interface, which should have its ground area separated from the digital and analogue ones. The distance among these ground planes should be increased. A single-point connection from the power and analogue grounds to the digital ground should be performed to avoid ground current loops. Ideally, a four-layer PCB would be of interest, having a single layer for power supply and ground, respectively. This layout would eliminate long power tracks and reduce the number of filtering elements needed. Additionally, the ground layer would shield external noise interference, which has not yet been considered. Complementing these changes and for further evaluation, a FEM simulation of the PCB layout, using Ansys Q3D, for example, can be done to detect board parasitics and problematic tracks or loops and, based on its results, implement the corresponding design optimisation.

Regarding other control PCB improvements for a future iteration, the following optimisation levellers can be implemented. First, as the DSP code has been verified, the controlCARD and docking station solution, which is adopted in this thesis simplifying the design process and connections to the DSP, can be substituted by the chosen DSP IC only. This choice would considerably reduce the control PCB size as the docking station is the component that requires the most significant space. Second, a fibre-optics interface is required for FSI communication. The

corresponding transceiver and circuitry need to be designed to achieve this. Finally, as a general observation, some of the component choices, such as the sensors, should be re-evaluated. In this thesis, commercial components are used when possible to simplify the design process due to the limited amount of time for developing the SM prototype. However, for the next iteration, some components can be exchanged by others that provide a better and cheaper solution even though the design effort required may be slightly higher.

Concerning the power hardware, no direct error has been detected. However, some improvements and optimisation levellers are observed, which are not covered in this thesis so far. First of all, the power module chosen has a higher nominal current rating than required of the SM. Therefore, the choice of power module could be optimised to a smaller size in a new iteration. Further, a power module solution including a heat sink can limit the volume as the chosen heat sink is relatively large compared to the power module. Following the power module, the capacitors chosen could be optimised to the most optimum solution from Table 2.5. A new solution could lead to fewer capacitors or higher current ratings. Further, the ESR is lower for many other capacitors since the model used is an older version. The busbar design used in this thesis is the most beneficial; however, an improvement to the assembly could be made to ease this process. Further, the busbar thickness is found quite conservative and can be reduced in thickness. The weight of the power module is also still significant and could be reduced by reducing the weight of the capacitors supports that hold them, which could be changed to aluminium instead of steel.

4.5 Technology Readiness Level Analysis

After testing and evaluation of the first iteration of the SM design, a final analysis is conducted to conclude on the maturity of the SM design reached in this thesis. For this purpose, the Technology Readiness Level (TRL) method is used, which assesses the maturity level of technology products [78]. The method was initially developed by the US Department of Defense (DoD) and NASA together in the 2000s and later extrapolated to other scientific and technological fields such as renewables in [79]. To evaluate the product state, TRL is based on a nine-level scale where 9 is the highest level, hence the level where the product is sufficiently

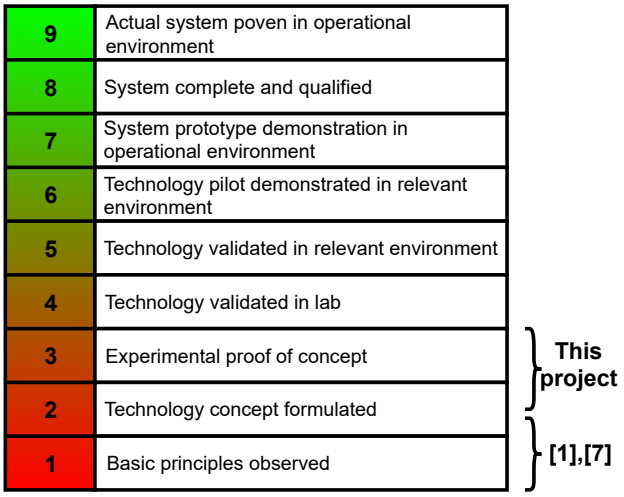


Figure 4.37: Technology Readiness Level description.

matured to be commercialised. The different levels and their description are illustrated in Fig. 4.37. Based on the levels presented in the figure defined in [79], the development of a product can be divided into four main categories. TRL 1 and 2 comprise the initial stage, which covers the research and concept formulation. TRL 3 and 4 include the first prototyping phase and test in a laboratory environment. TRL 5, 6 and 7 deal with the development and testing phase of the product in the application environment. Finally, TRL 8 and 9 cover the deployment part where the system has been fully proven and ready to be manufactured.
This section aims to apply this analysis to the high-power testing application pursued in this thesis. For this purpose, the MMC-based grid emulator system design and implementation progress is evaluated following the TRL description given in Fig. 4.37 and each level definition according to [79]. Starting from the first level, TRL 1 covers the initial thoughts, application definition and technology research concerning the product. For the grid emulator case, this analysis was carried out in a previous study by the authors [1], [2] where the grid emulator application was defined and characterised. Additionally, different power converter topologies were presented and compared regarding their suitability for the targeted application. The advantages of the proposed system over existing products were also listed and evaluated. Therefore, it can be concluded that TRL 1 has been completed for the grid emulator system in former work, as indicated in Fig. 4.37. Considering TRL 2, this level focuses on the concept formulation and initial dimensioning. In [1], [2], the Back-to-back MMC was concluded as the most suitable topology for grid emulator applications. A methodology for sizing the power hardware elements was also developed, finding an initial guess for the full MMC converter electrical and physical magnitudes. However, an MMC is a complex system as it is composed of smaller sub-systems that need a structure and control system to achieve correct functioning. Moreover, the grid emulator features can add additional complexity to the system. Therefore, the development of the grid emulator system needs to be divided into sub-systems to guarantee a successful process. Each of the individual components needs to achieve a certain TRL grade before being able to be integrated into the final product.
In this thesis, the focus is on a SM sub-system for a MMC grid emulator, hence the TRL level of this component is estimated. Both to estimate the maturity of the SM itself but also for the full MMC where the SM plays an important role. As earlier mentioned, the TRL level 1 and partly 2 was achieved in earlier works considering the full MMC for grid emulation. To fulfil TRL 2, the sub-system level needs to be considered and specified due to the complexity of the system. Starting from this point, the expected goal of this thesis is to raise the TRL from this initial point considering the SM as a sub-system. To fully achieve the TRL level 2, the SM concept needs to be settled similarly to the top-level grid emulator concept. Concerning this, materials and components of the SM should be found, which is a main task for the thesis by settling available technologies and materials for the SM. From these choices, the first SM concept is achieved along with important solutions needed to achieve the keywords, especially scalability, presented in the introduction in Chapter 1. Following this, many improvements are found in striving to optimise the chosen SM solution by investigating different choices of the SM's components in a qualitative fashion. Finally, the laboratory test of the SM is settled, which concludes the main requirements to achieve TRL 2. The focus then moves towards the TRL 3, which includes the experimental proof of concept. In this case, considering the SM as a sub-system of the full grid emulator MMC, hence other sub-systems also need to fulfil the TRL 3 to achieve the level for the full technology. When considering the experimental proof, the SM is tested as a full-size prototype compared with relevant modelling. As a sub-system to the full MMC, the relevant interfaces are tested following the specifications settled in TRL

2 as well as the internal components. In this thesis, the proof of the SM concept is therefore achieved, hence the SM as a sub-system is considered to reach TRL 3. To reach TRL 4, the system needs to be fully validated in a laboratory environment, considering a reduced size prototype but considering grid emulator MMC, and not only the SM itself. Further, more improvements need to be made to the SM before it can engage in such a prototype. To reach TRL 4, other sub-systems such as communication and MMC structures and auxiliary components need to reach TRL 3 for together engaging in the pursue of TRL 4. Then, besides MMC operation, TRL 4 needs to consider the grid emulator operation using MMC.

Concluding on this investigation, the contribution from this thesis is a rise from TRL 2 to TRL 3, giving a tested concept and including improvements to enable a second iteration design for a prototype used in TRL 4 investigations. The SM itself can therefore not, as expected, be considered the final SM and another iteration considering the methodology in Fig. 2.1 is needed.

Chapter 5

Conclusion

In this thesis, a SM for a MMC used for high-power testing such as grid emulation is developed. Throughout a research process, a methodology is proposed for the development, including necessary steps. As an outcome, an initial SM design including sub-system and material choices is defined. A first integration prototype is produced, assembled and tested following the test campaign derived. Finally, the SM prototype has shown promising results following the requirements and possible improvements and optimisations are identified.

Considering the developed methodology, a DFMEA based approach reducing risk and raising design confidence is employed. The DFMEA based approach has proven a strong tool to obtain tests, which is important to detect weaknesses in the design phase. From the methodology, a clear test campaign is developed considering test to mitigate possible failure modes and ensure SM's MMC interfaces to be valid. Further, the methodology gives a structured model for the development of a MMC SM and potentially other power electronic-based converters in the megawatt range.

Following the proposed methodology, a SM design is achieved. The various systems are detected and developed, mainly considering power and control hardware. Focusing on the power hardware, a robust design is achieved, including detection of some qualitative and quantitative optimisation levellers such as power modules and capacitors, and busbar design, respectively. In the case of the control hardware, the thesis results in a PCB design, including control hardware and interfaces to a chosen gate driver circuits. During the development phase, some failure modes are detected considering the data acquisition. The control hardware is therefore proven to be the more difficult part that needs to be improved for future versions. The SM is tested to ensure that it can withstand operation within the interface requirements. The SM design shows promising results considering its electrical and thermal operation, lacking only a test at the maximum voltage ratings due to the data acquisition problem stated. The SM is not proven in MMC operation, it is however concluded that this is not a necessity to validate the SM design itself.

The developed design and test results are validated considering the prototype improvement, failure modes and Technology Readiness Level (TRL). From these analyses, some improvements and optimisation levellers are detected. Further, analysing the TRL, it is concluded that the technology reaches level 3 considering the SM as a sub-component of the full MMC for high-power testing.

Based on the previously mentioned points, it can be concluded that a first iteration MMC SM prototype is achieved, which creates the initial step for a MMC-based grid emulator development.

Chapter 6

Future Work

This chapter introduces improvements that are detected during the development of this thesis and are, therefore, left as future work. Further, some features and studies that are not covered in this report due to time limitation are also included.

During the commissioning and experimental phases of the project, some weaknesses are found in the control PCB regarding electromagnetic noise immunity (EMC). Therefore, its design should be reconsidered in a future version to overcome this issue. In general, optimisation of this control PCB is needed as the component choices in this thesis were done taking into account the time limitation. Regarding other SM elements, it is also noticed that some components such as the busbars or the heat sink can be reduced in dimensions. This will lead to an even more compact SM design.

Besides improvements of the existing components, the SM design can be expanded with some features and components that are not studied in this thesis. First, the SM low-voltage components should be supplied from its DC-link voltage, taking into account the capacitor voltage variations and allowed ripple. Additionally, a by-passing protection needs to be defined to disable the whole SM if a local fault happens. Regarding the grid emulator system, the development of the mechanical structure needs to be done. This includes the design of the frame/cabinet that will host the converter, isolators between SMs and the requirements these demand for the MMC topology. Complementing the mechanical setup, a converter-level cooling system needs to be sized, for which some initial requirements are analysed in this thesis at SM level. The converter communication link also needs to be specified where an optical fibre network is the best candidate. Therefore, optical fibre transceivers are needed in both SMs and top-level controller. It should be pointed out that each of the mentioned parts needs to achieve a specific TRL before their integration on the final grid emulator system.

Finally, the SM testing could not reach nominal voltage values due to hardware protection tripping caused by the noise issue. Once this problem is solved, the SM needs to be tested at full load conditions to have a complete assessment of its design. When the SM design is validated, it will be of interest testing the SM in a MMC application environment as this operation will have an influence on the power losses and components lifetime, among others. To accomplish this, a test using two SM can be carried out, as described in [80], [81], where one SM acts as a current source emulating MMC operation and the other as a real SM itself. This will provide a more realistic evaluation of both design and application.

The proposed FSI communication implementation and testing could not be achieved due to time limitation; therefore, it is still pending as future work. This test will provide both control hardware and bandwidth requirements as it will allow analysing the different time delays and constants in the system.

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Appendix A

FSI Communication Influence in Sub-Module Number

Adding to the brief presentation of FSI in Chapter 2, for a fast evaluation and test of the protocol, an electrical FSI interface is chosen instead of an optical link, as it requires fewer components and the time delay due to the electrical-to-light signal transceiver can be neglected. Nevertheless, for a final design, a fiber optical interface is required due to MMC nature. The maximum FSI clock allowed by the TMS32F280025 DSP is 50 MHz and the transmission can be done using one or two FSI data lines [44], [82]. There are different ways of interconnecting these data lines among the converter elements, being the two main ones: a star connection, where all the slaves (SMs in these case) are connected point-to-point to a single master (top-level controller); and, a daisy chain connection, where all the devices involved in the communication process are connected forming a ring. Even though the star topology would allow a lower latency, it is not suitable for MMC applications as it would require complex and expensive infrastructural hardware due to the high number of strings. Therefore, the daisy chain option would be preferred.
Knowing that FSI would be the desired communication protocol, calculating how many SMs, or slaves, can be managed by a master device for a specific data length and maximum control frequency is of interest. For this purpose, transmission times between two nodes are introduced in Table A.1, which are given in [46].

Table A.1: Transmission times for a FSI frame across two nodes.

Data size (words) 1 word = 16 bits	Transmission time [μs] 1 data line	Transmission time [μs] 2 data lines	Transmission time at each slave [μs]
1	0.56	0.4	2
2	0.72	0.48	2
3	0.88	0.56	2
4	1.04	0.64	2
5	1.2	0.72	2
6	1.36	0.8	2
7	1.52	0.88	2
8	1.68	0.96	2

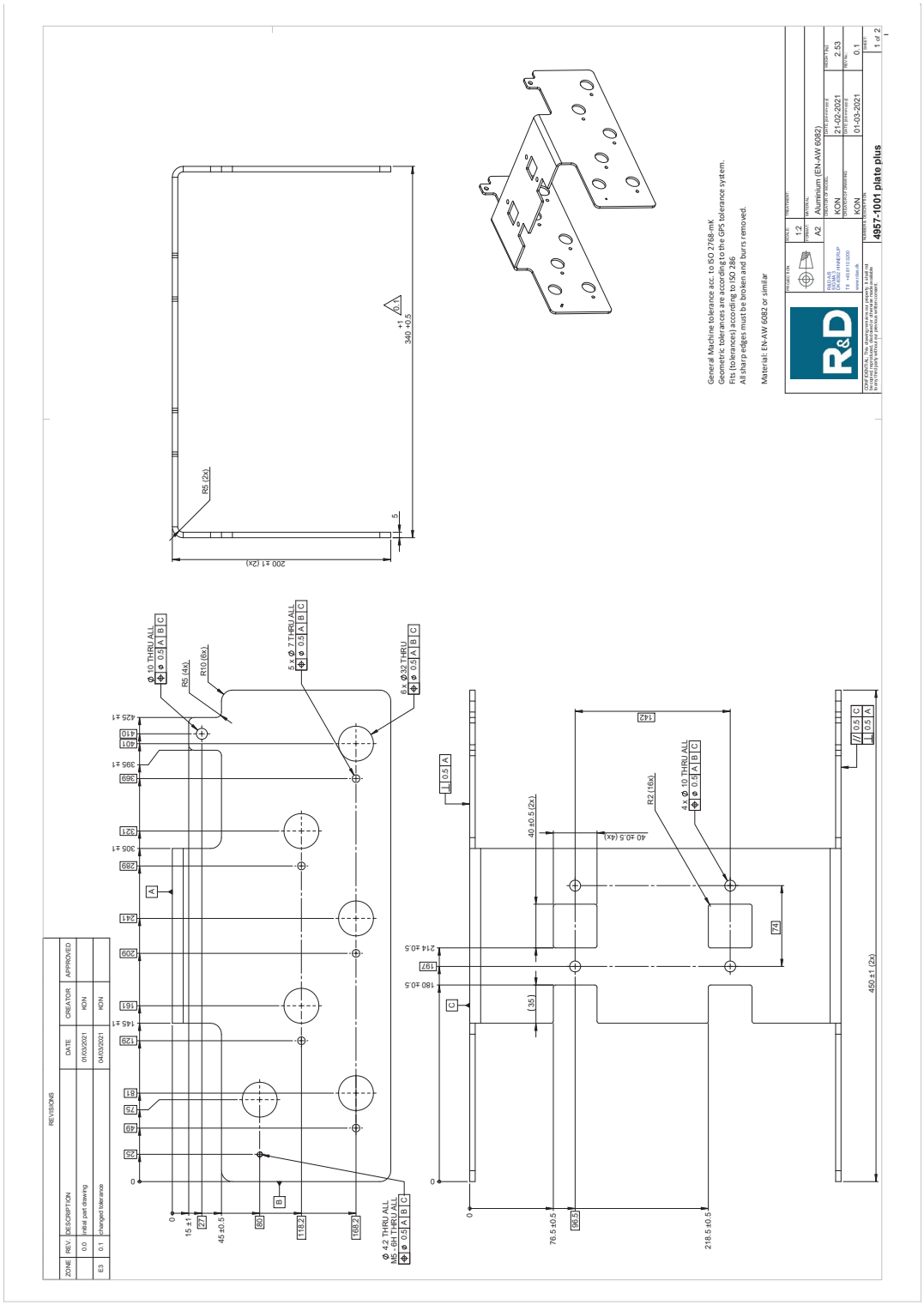
Considering the case of a 64-bit data (4 words) transmission and a control frequency of 10 kHz, the maximum number of SMs allowed is calculated in (A.1), when using only one data line; and, in (A.2), for two data lines.

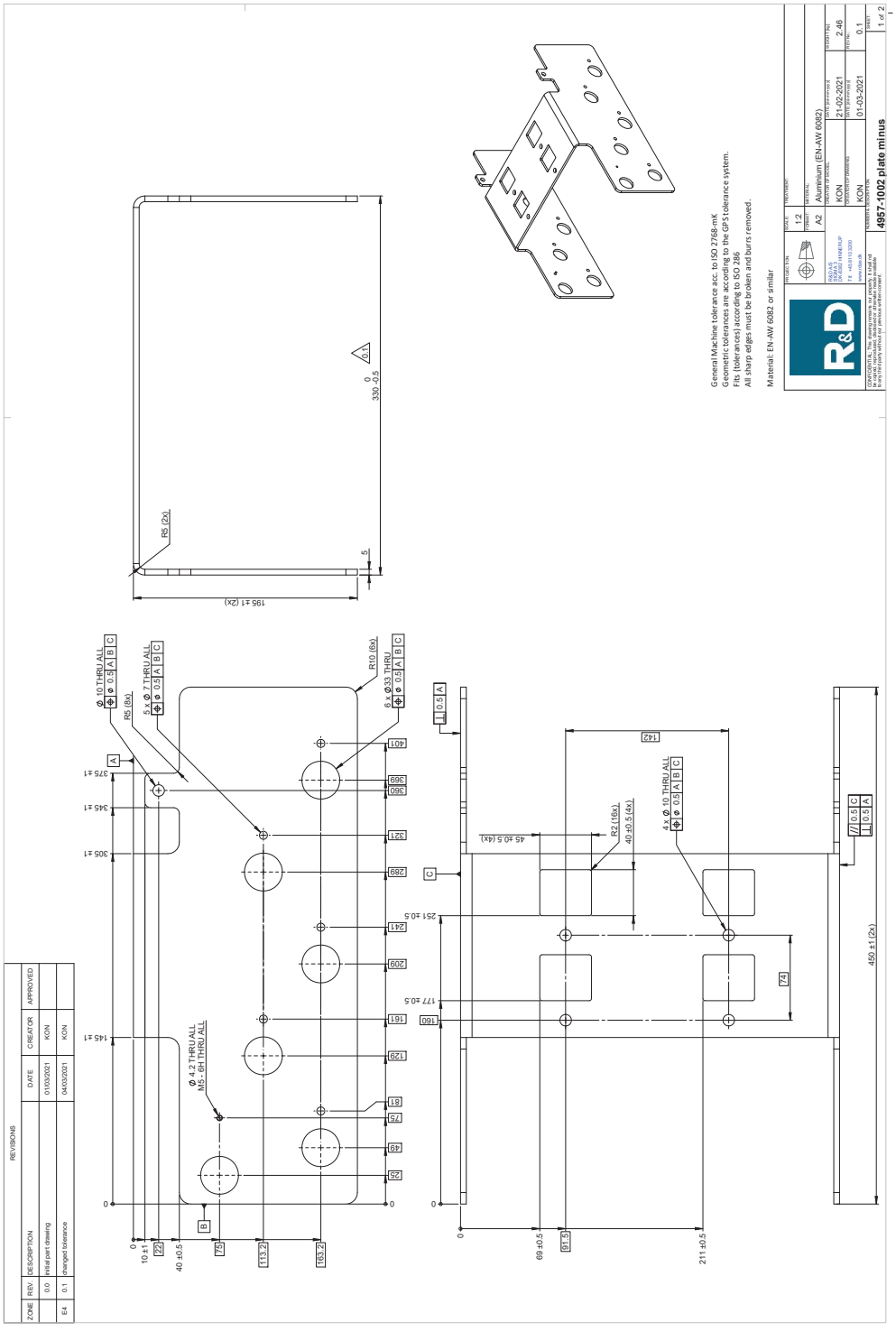
$$\frac{1}{N \cdot 1.04\mu s + (N-1) \cdot 2\mu s} = 10000 \rightarrow N = 33 \tag{A.1}$$

$$\frac{1}{N \cdot 0.64\mu s + (N-1) \cdot 2\mu s} = 10000 \rightarrow N = 38 \tag{A.2}$$

Appendix B

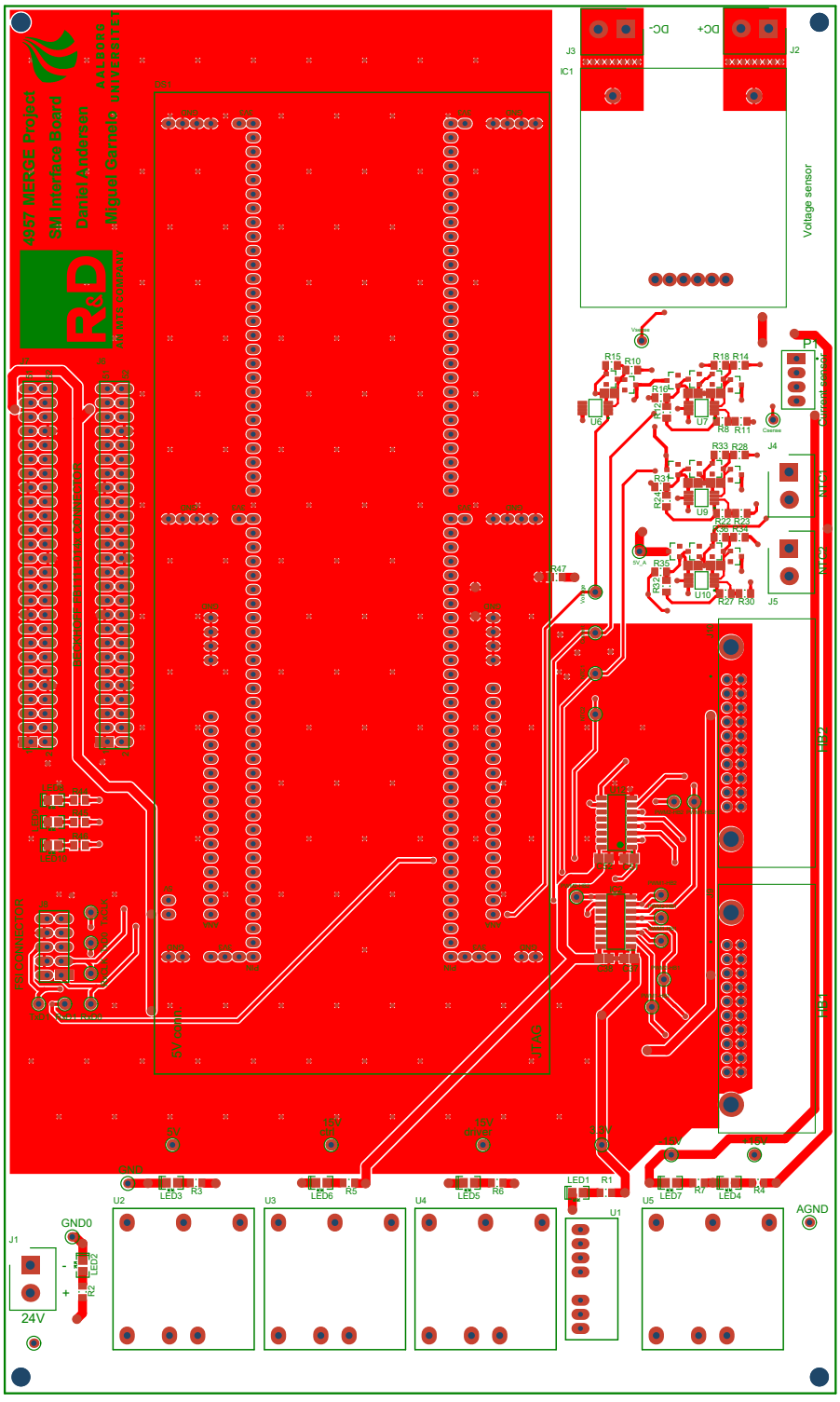
Mechanical busbar drawings

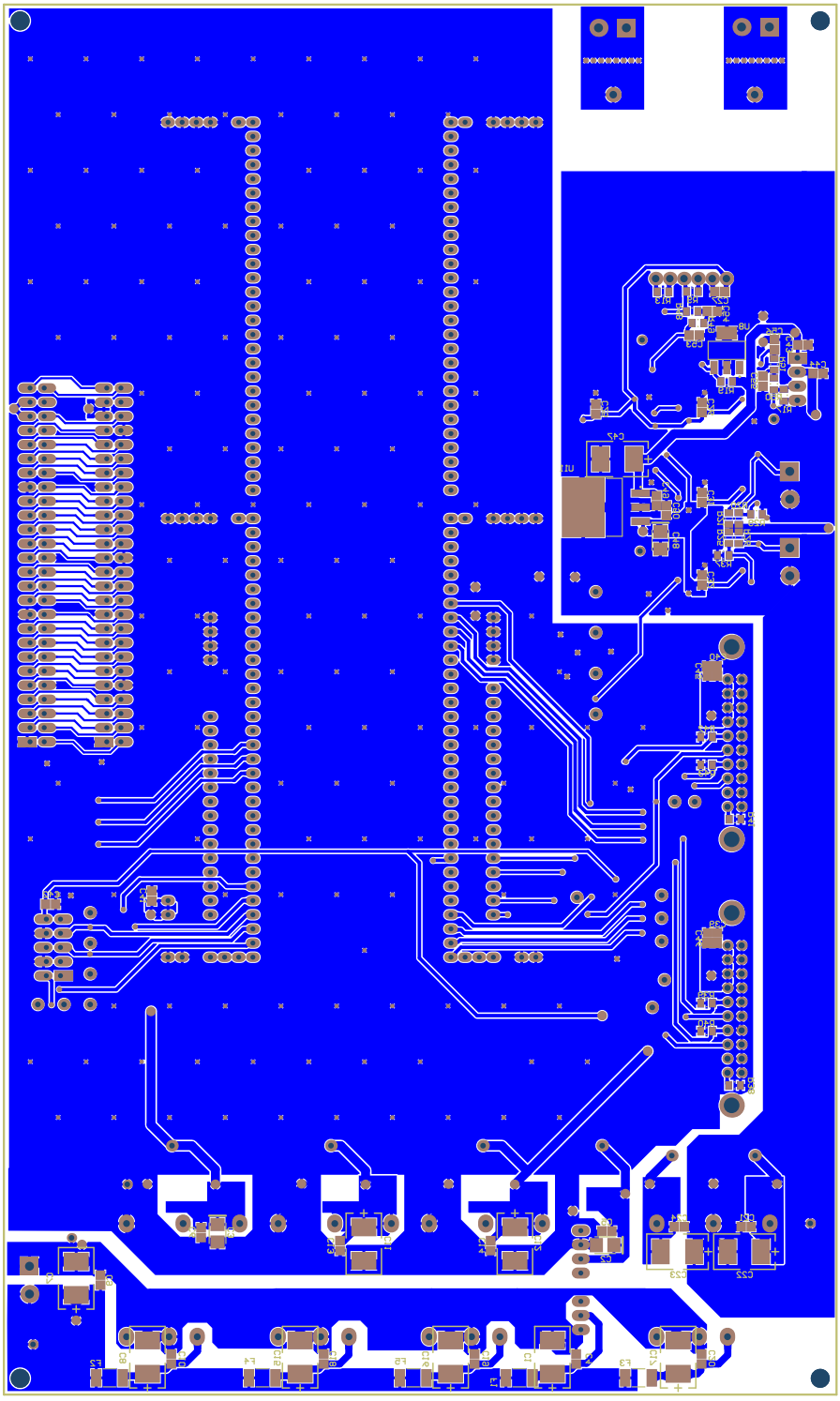



REVISIONS
ZONE
REV
DESCRIPTION
DATE
CREATOR
APPROVED
0.0
Initial part drawing
01/03/2021
KON
0.1
changed tolerance
04/03/2021
KON
E4
General Machine tolerance acc. to ISO 2768-mK
Geometric tolerances are according to the GPS tolerance system.
Fits (tolerances) according to ISO 286
All sharp edges must be broken and burns removed.
Material: EN-AW 6082 or similar
R&D
Aluminium (EN-AW 6082)
21-02-2021
01-03-2021
4957-1002 plate minus
1 of 2
R5 (2x)
195 ±1 (2x)
330 -0.5
5
450 ±1 (2x)
211 ±0.5
69 ±0.5
91.5
40 ±0.5
75
113.2
163.2
10 ±1
25
145 ±1
305 ±1
345 ±1
375 ±1
177 ±0.5
251 ±0.5
74
142
160
45 ±0.5 (4x)
R2 (18x)
40 ±0.5 (4x)
R5 (8x)
R10 (6x)
Ø 4.2 THRU ALL
M5 - 6H THRU ALL

Appendix C

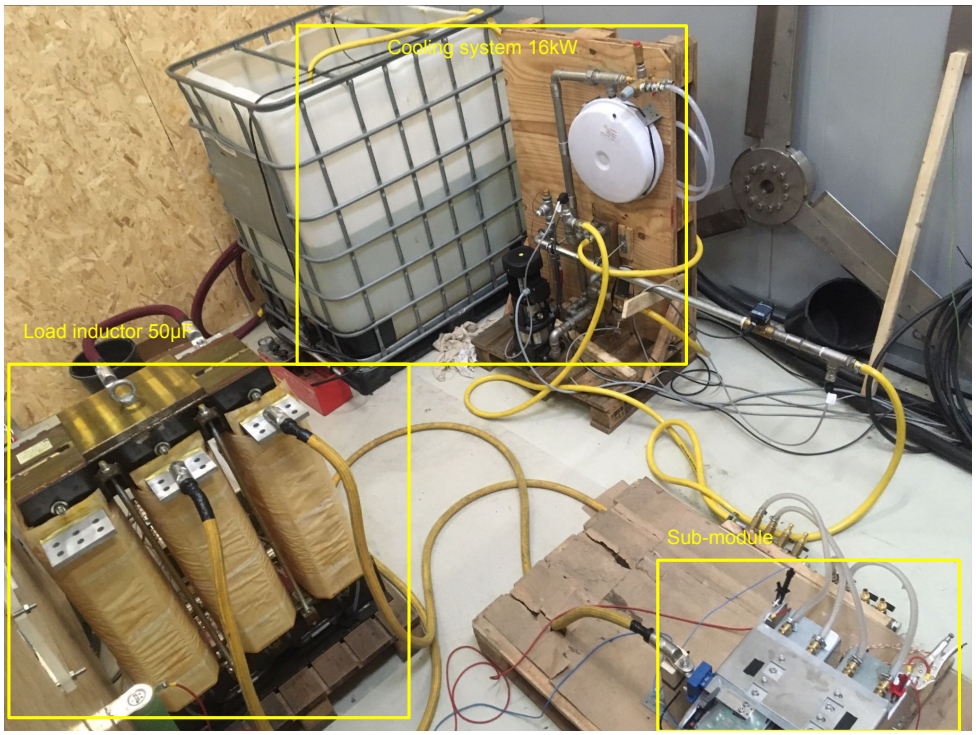
PCB drawings

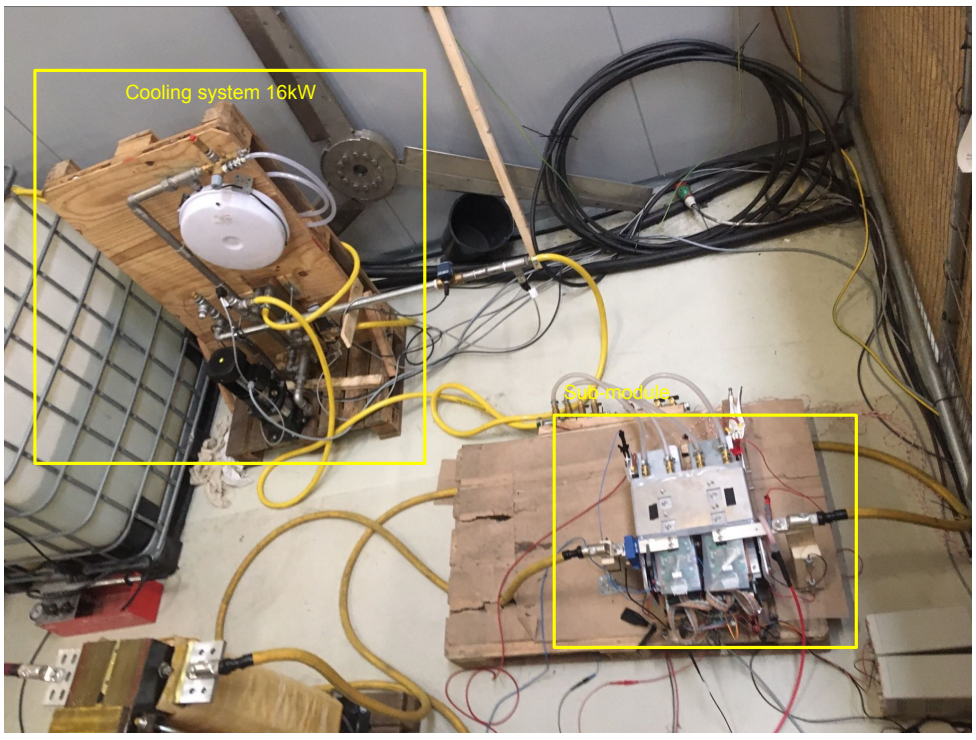


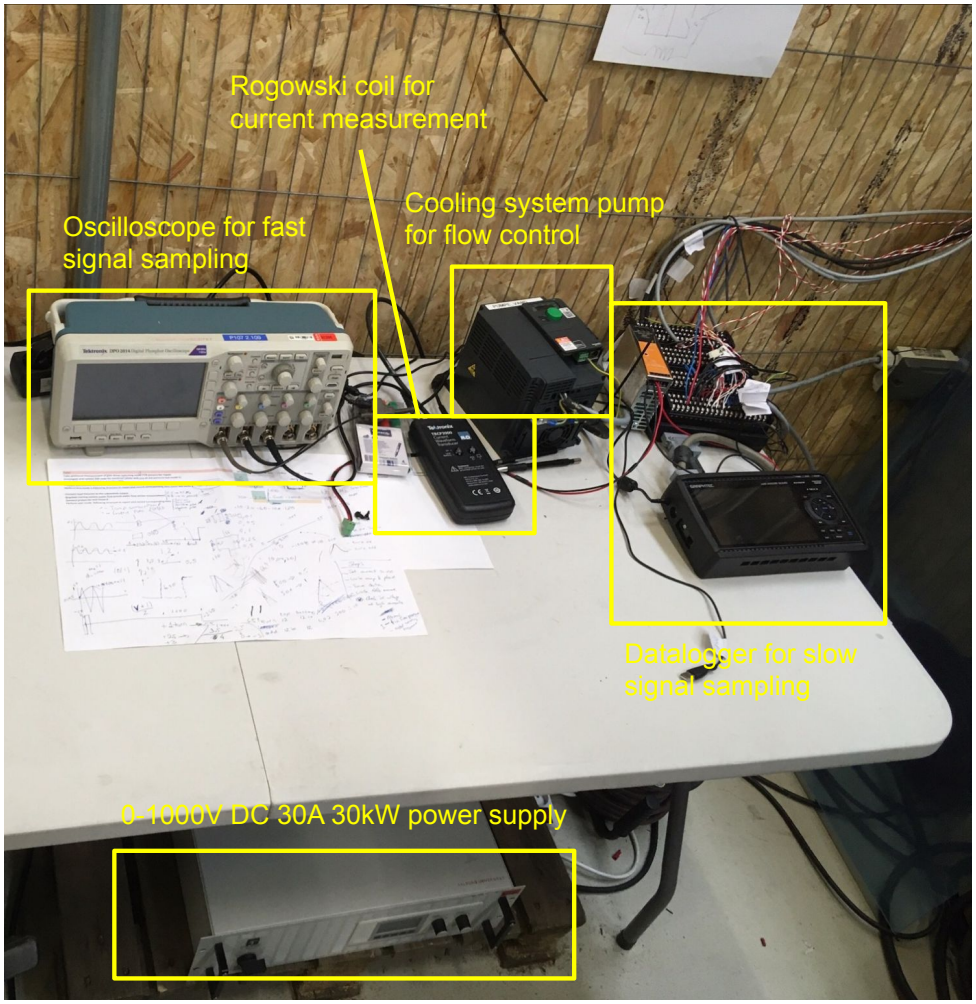


Appendix D

Test setup






Rogowski coil for
current measurement
Cooling system pump
for flow control
Oscilloscope for fast
signal sampling
Datalogger for slow
signal sampling
0-1000V DC 30A 30kW power supply

Appendix E

Sub-module budget

This appendix summarises the total price of the first iteration of the MMC SM proposed on this thesis, only considering component and parts price.

Table E.1: Sub-module budgetary list.

Component	**Quantity**	**Price [DKK]**
Power module	2	9.300,00
DC capacitor	10	7.035,00
Busbars	1	2.950,00
Heat sink	2	2.412,00
Gate driver	2	4.320,00
Control PCB	1	68,00
DSP controlCARD	1	1.010,00
Voltage sensor	1	516,00
Current sensor	1	426,00
Data acquisition	1	110,00
Power supply	1	1.260,00
Hardware protection	1	20,00
Misc. (resistors, capacitors, LEDs, connectors, bolts)	1	1.410,00
Total		**30.837,00**