# *Mission Profile Based Lifetime Evaluation of Grid-Connected PV Inverter*

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**Participants:**

Martin Vang Kjær

**Supervisors:**

Frede Blaabjerg
Huai Wang
Yongheng Yang

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**Synopsis:**

In the last decade renewable generation have become the preferred source of production of electricity and two-thirds of the net installations in 2018 were renewable based, which marked the seventh consecutive year, where renewable installations were above 50%.

Photovoltaics is the globally most preferred technology in terms of most installed renewable power generation and PV inverters are also identified as the assemblies which have the highest failure rate compared to other parts. This project conducts lifetime estimation on a grid-connected PV inverter, with the purpose of identifying the critical components in terms of reliability.

Each component in the system is subjected to state-of-the-art reliability modelling in terms of translating real-field mission profiles and in terms of conducting the wear-out analysis for long-term operation. Large efforts are made to include relevant uncertainties by means of including electrical parameter variation and the highly influential variation of the lifetime model parameters. The project includes design for reliability aspects in terms of analysing different subsystem configurations in order to improve the lifetime.

# Preface

### Reading Guide

Each chapter is introduced and finished with a short paragraph written in *italic* form. These paragraphs are introductions and partial conclusions for the given chapters. There will appear source references throughout the report. These references will be collected in a source list at the end of the report. The reference method used in the report is the Harvard Method, which implies that the reference is placed in the text with following notation [Number which refer to Author etc.]. If the reference contains multiple sources, then each source is separated by comma. The references refer to the list of sources where books is stated with author, title, publisher, edition and year of publication while web pages is stated with author, web address, title and the point of time that indicates the last visit at the web page. Equations, tables and figures are numbered in accordance with the given chapter, i.e. Figure 1.2 is the second figure in chapter one. Explanatory text for figures and tables is located beneath the given tables and figures as captions.

Martin Vang Kjær

# Nomenclature

| | |
|---|---|
| AC | Alternate Current |
| CDF | Cumulative Distribition Function |
| CI | Confidence Interval |
| CTE | Coefficients of Thermal Expansion |
| DC | Direct Current |
| ESR | Equivalent Series Resistance |
| FFT | Fast Fourier Transform |
| IGBT | Isolated Gate Bipolar Transistor |
| LCOE | Levelized-Cost-of-Energy |
| MPP | Maximum Power Point |
| MPPT | Maximum Power Point Tracking |
| NOCT | Nominal Operating Temperature of the PV Module |
| OC | Open Circuit |
| PO | Perturbation and Observe |
| PCC | Point of Common Connection |
| PDF | Probability Density Function |
| PI | Proportional Integral |
| PLL | Phase Lock Loop |
| PM | Phase Margin |
| PoF | Physics of Failure |
| PV | Photo Voltaic |
| RBD | Reliability Block Diagram |
| RMS | Root Mean Square |
| SC | Short Circuit |
| SI | Solar Irradiance |
| STC | Standard Test Conditions |

| | | |
|---|---|---|
| VSC | Voltage Source Converter | |
| $\alpha$ | Multiplicative Coffin-Manson Parameter | [-] |
| $\beta$ | Weibull Shape Parameter | [-] |
| $\eta$ | Weibull Scale Parameter | [-] |
| $\lambda$ | Hazard Rate | [failures/t] |
| $\omega$ | Radial frequency | [rad/s] |
| $\phi$ | Phase | [degrees] |
| $\tau$ | Time Constant | [ |
| $C$ | Capacitance | [F] |
| $D$ | Damage | [−] |
| $D$ | Duty Cycle | [−] |
| $E_a$ | Activation Energy | [J/mol] |
| $E_g$ | Silicon Band Gap Energy | [$J$] |
| $f$ | Frequency | [Hz] |
| $G$ | Solar Irradiance | [ |
| $I$ | Current | [A] |
| $i$ | Iteration Index | [-] |
| $j$ | Complex Operator | [-] |
| $k$ | Boltzmann Constant | [J/Kelvin] |
| $L$ | Inductance | [H] |
| $L_f$ | Time to Failure | [−] |
| $L_o$ | Rated Lifetime | [−] |
| $m$ | Modulation Index | [ ] |
| $n$ | Diode Ideality Factor | [−] |
| $n$ | Exponential Coffin-Manson Parameter | [-] |
| $N_f$ | Number of Cycles to Failure | [−] |
| $P$ | Electrical power | [$W$] |
| $p$ | Exponential Capacitor Lifetime Model Parameter | [−] |
| $Q$ | Reactive Power | [var] |

| | | |
|---|---|---|
| $q$ | Elementary Electron Charge | $[C]$ |
| $R$ | Resistance | $[\Omega]$ |
| $R_{th}$ | Thermal Resistance | $[K/W]$ |
| $S$ | Apparent Power | $[VA]$ |
| $S$ | Laplace Operator | [-] |
| $T$ | Temperature | [ |
| $t$ | Time | $[s]$ |
| $V$ | Voltage | [V] |
| $X$ | Reactance | [ |
| $Z_{th}$ | Thermal Impedance | [W/K] |

# Table of contents

# 1 Introduction

In the past decades, policies has been adopted, which are in favour of reversing the effects of global climate changes, and therefore technologies which do not rely on fossil fuels have seen an increase worldwide. Renewable generation is becoming the preferred source of production of electricity and a capacity of 181 GW renewable power was added in 2018, which was an increase in respect to the added capacity of the previous years. In total the renewable generation accounts for nearly one-third of the global installed power generation capacity and nearly two-thirds of the net installations were renewable based, which marked the seventh consecutive year where renewable installations were above 50 % as shown in Figure 1.1 [50]

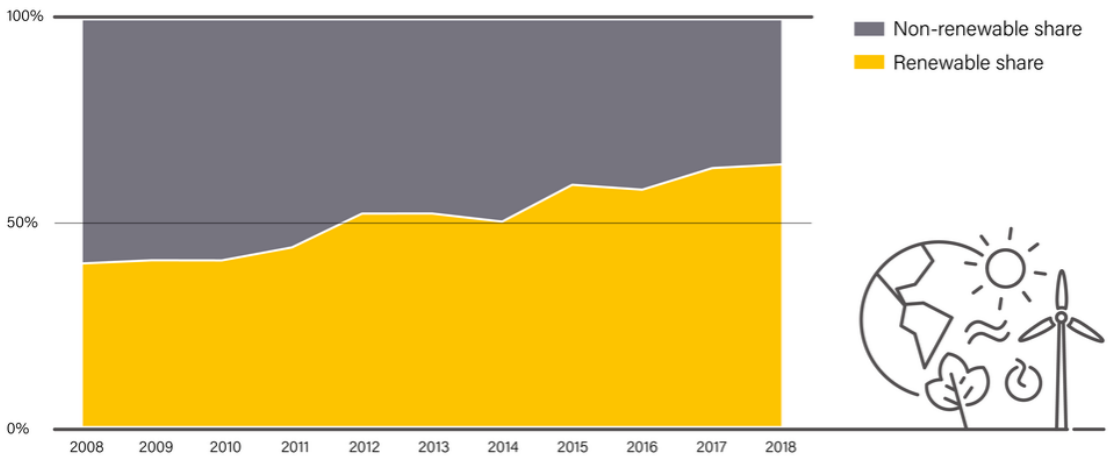


Figure 1.1: Share of renewable power generation capacity,2008-2018 [50]

One of the key technologies, used to obtain a sustainable energy supply, is power electronics, which constitutes a substantial part of power systems and is widely used within renewable power generation. The integration of power electronics into power systems enables efficient and flexible interconnection of renewable generators, loads and electrical grids as depicted in Figure 1.2 [9].

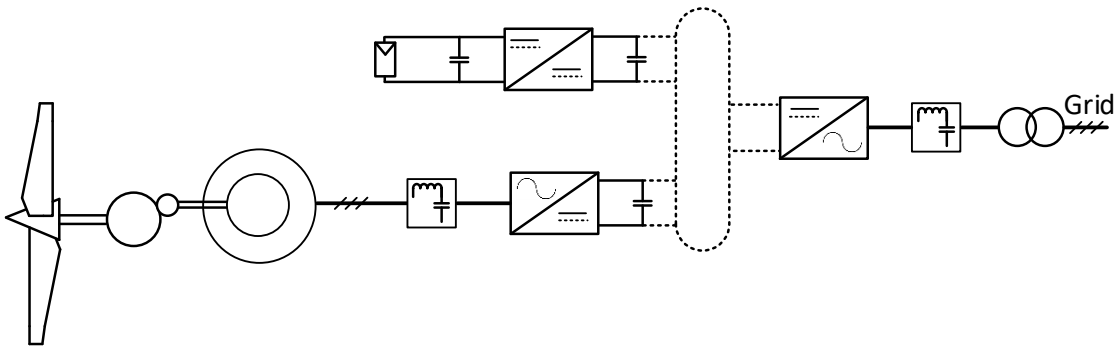


Figure 1.2: Power electronics interfaced renewable generation

Due to the indispensable role of power electronics within power systems, the overall performance, including reliability, of power electronic converters has a significant influence on the efficiency and cost of the system [67].

## 1.1 Power electronics and the importance of their reliability

As the continuing evolution of power devices, passive components, circuit topologies, control strategies, and system integration technologies, many variations of power electronic converter systems are available today. With the present tendency, the technologies will continue to evolve [74]. The performance of the converter systems is dictated by the selected components, the adapted circuit topology, control strategy, and environmental and operational conditions [71]. Among the main factors, cost of failure is of major concern when designing the power electronics power system application. As the downtime of generation units could result in significant negative financial consequences, a comprehensive cost analysis should be carried out with the possibility of using components with ratings well above the expected stress levels or by applying the stress in a conservative manner by usage of certain control strategies. While the targeted efficiency is within reach, power electronic converters are, according to the literature [78], identified as the most fragile sub-systems and could therefore constitute the bottleneck of the entire system, in terms of reliability. The definition of reliability with regards to engineering is the probability that an item is capable of performing its required task without failure under specified conditions and time [53]. A well developed reliability analysis within power electronics should include the failure criteria of the components, the stress conditions, the reliability numbers (%), the confidence level (%) and at which specific time those reliability numbers apply [16]. In respect to field experience, a 3,5 MW PV plant are depicted in Figure 1.3, which reveals that PV inverters are one of the most critical sub-systems in terms of failure rate, lifetime and maintenance cost.

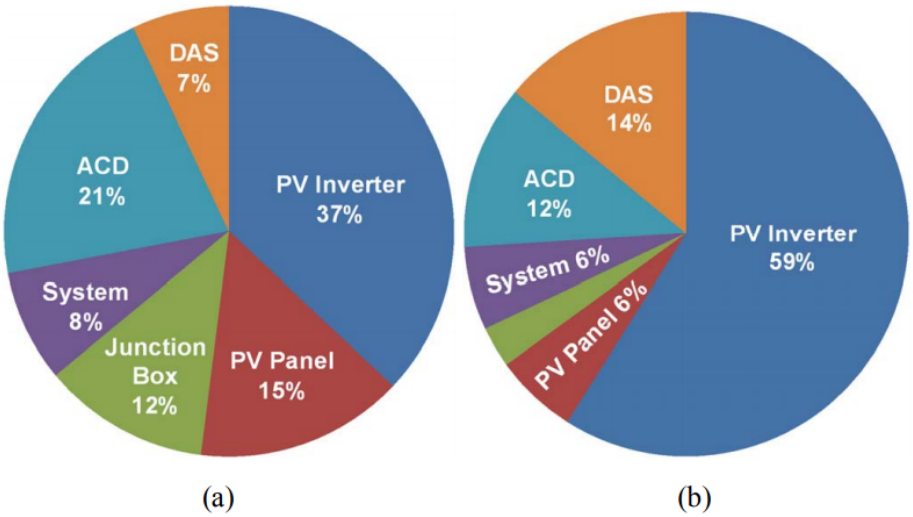


Figure 1.3: Field experience of a 3.5 MW PV plant [49]: (a) failure events, (b) unscheduled maintenance costs. Where DAS denotes data acquisition systems and ACD denotes AC disconnectors.

The field data in [49] are collected in a time span of five years consisting of 11,700 identical PV modules, and 26 identical PV inverters rated at 135kW. As it can be observed in Figure 1.3, PV inverters are resposible for 37% of the failure events and 59% of the unscheduled maintenance costs.

Not only will the fragility of these components alter the cost of energy generation negatively, but also induce the risk of a reduction in delivered energy due to system downtime. Recent research efforts are therefore concerning the subject of estimating the lifetime of the power electronic converters and thereby increase the availability by means of predictive maintenance, which results in lowering the Levelized-Cost-of-Energy (LCOE) [71].

## 1.2 Key concepts of reliability in power electronics

This section will introduce the key reliability concepts, which will be applied throughout the project. The frequency of failure occurrence in power electronic components can therefore be represented by means of a failure distribution, which is modelled as a normally distributed probability density function (PDF), denoted as f(t) [53]. Figure 1.4 shows an example of a failure distribution as a function of years, for a capacitor used in a power electronic application. The cumulative distribition function (CDF), denoted as F(t), describes the accumulation of the failure probability at the time of interest, which is expressed as

$$F(t) = \int_0^t f(t)dt \tag{1.1}$$

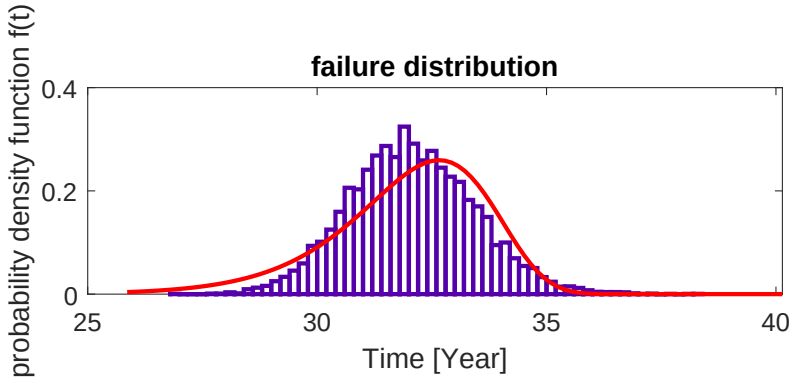


Figure 1.4: An example of the failure distribution for a capacitor used in a power electronic application.

If $F(t)$ is defined as the cumulative distribution function, the reliability can be expressed as

$$R(t) = 1 - F(t) = 1 - \int_0^t f(t)dt \tag{1.2}$$

The hazard rate h(t) is defined as the percentage of a population, which fail in a defined time interval.

$$h(t) = \frac{f(t)}{R(t)} \tag{1.3}$$

There are different statistical distributions but the one used in this project and arguably the most popular in reliability engineering is the Weibull distribution. The Weibull (PDF) is expressed as [16]

$$f(t) = \frac{\beta}{\eta^\beta} t^{\beta-1} \exp\left[-(\frac{t}{\eta})^\beta\right] \tag{1.4}$$

The corresponding reliability function is

$$R(t) = \exp\left[-(\frac{t}{\eta})^\beta\right] \tag{1.5}$$

From (1.4) and (1.5), the hazard rate i.e the instantaneous can be calculated as

$$\lambda = \frac{\beta}{\eta^\beta} t^{\beta-1} \tag{1.6}$$

Where $\beta$ is the shape parameter, $\eta$ is the scale parameter, corresponding to when 63.2% of a population has failed. In this project the lifetime will be presented in the form of percentile life which is used to state at which time a certain percentage of the population has failed. In Figure 1.5 the time of a 10% failure, $B_{10}$ value, is shown. A $B_{10}$ percentile lifetime corresponds to reliability of 0.9. [16].

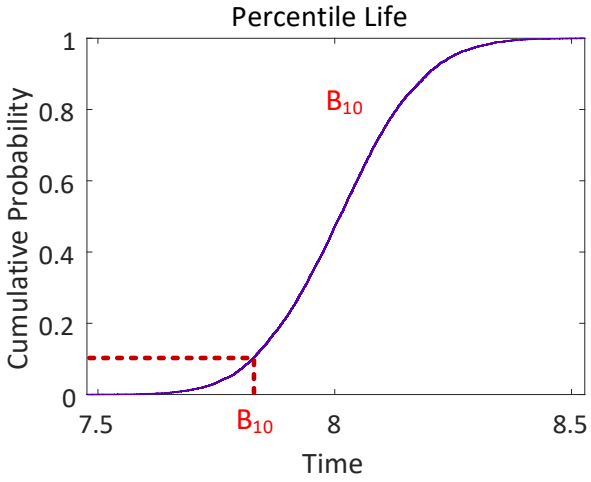


Figure 1.5: Stating the lifetime as a percentile of the population which has failed

A means to show how the failure rate is evolving throughout the entire life of an electronic component is the bathtub curve. It consists of the superposition of 3 failure rates: the failure rate for extrinsic, intrinsic and random failures as shown in Figure 1.6 [4]

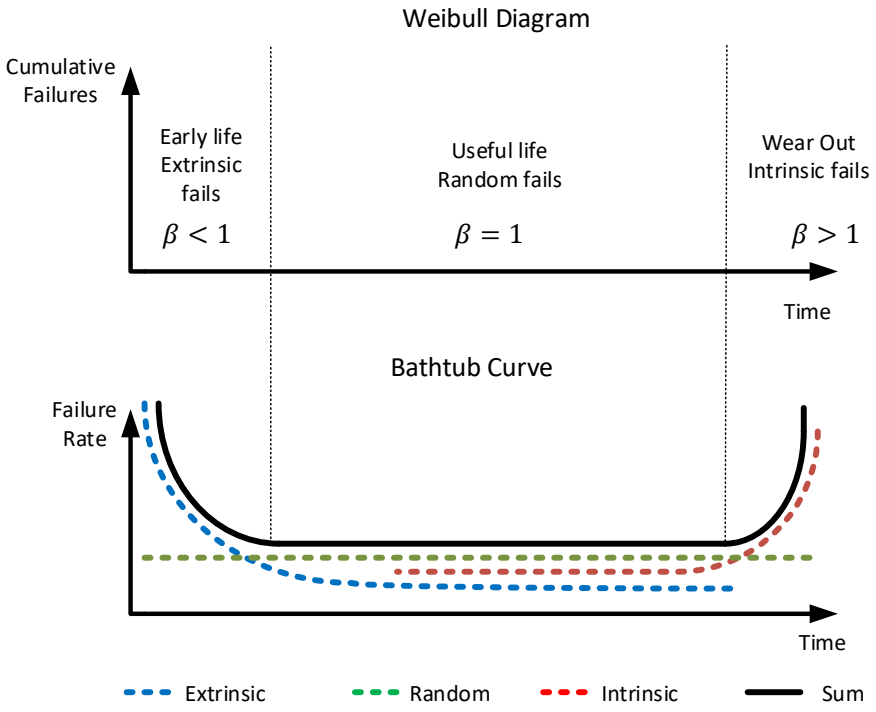


Figure 1.6: Bathtub curve, failure type, and Weibull parameter $\beta$

The extrinsic failure is due to unintended defects and deviations created during the manufacturing process, this failure is characteristic for infant mortality. Intrinsic failure is due to natural deterioration (wear-out) of the processed materials. If the extrinsic and intrinsic failure rates are reasonably separated in distance, then the straight line, which connects them, represents the useful life of the component [10]. The main object of this project is to predict the wear-out phase of the components in which the failure

rates are increasing i.e. $\beta > 1$. The failure rate of power converters, is analysed by means of identifying the key components, which are prone to fail through an in-depth reliability analysis, where the electronic components are subjected to a real-field loading profile. The conventional reliability analysis of power converters are based on failure data and field statistics. However, it may result in unrealistic prediction results as wear-out failure mechanisms are not considered and provides limited insights in how to improve the design. Instead, the physics of failure (PoF) approach is utilised by employing the obtained knowledge of the root causes of failures [70]. The main concept of the PoF is to gather understanding of how the operational requirements of the product are related to the physical characteristics. Moreover, an understanding of how the elements of the converter react to various stresses and how these stresses affect the lifetime degradation is obtained through PoF analysis. In general a failure of a power electronic component occurs when the applied loading exceeds the design strength as shown in Figure 1.7 [74] [16]

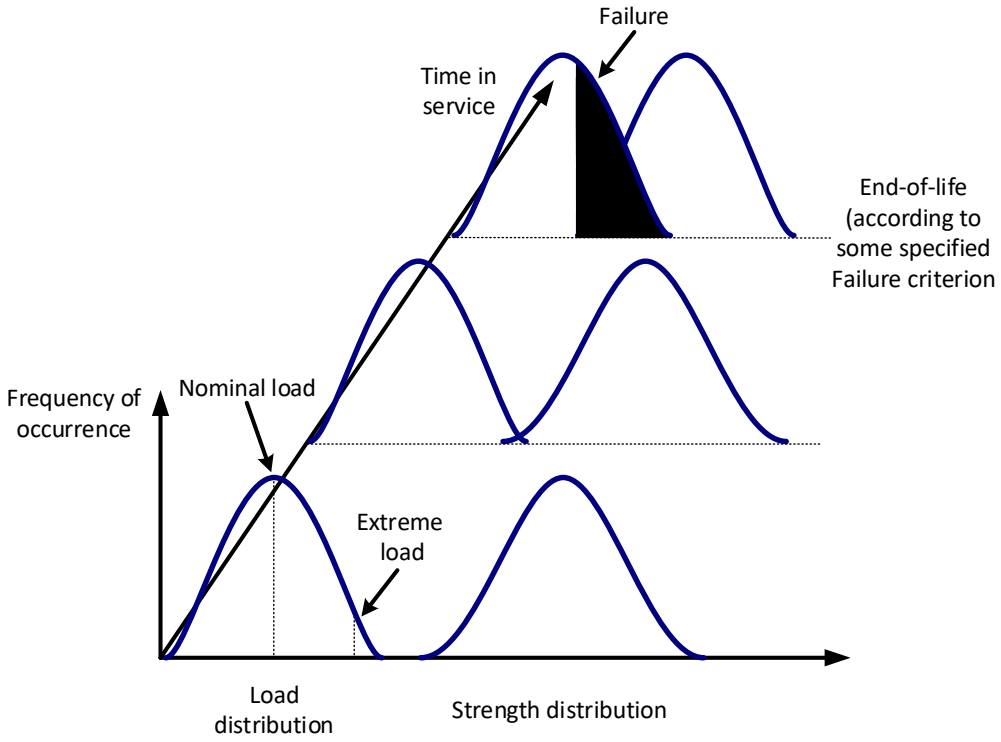


Figure 1.7: Load-strength curves to illustrate overstress and wear-out

The result of the PoF approach is an improvement of the understanding of the different failure mechanisms, which may provide a more realistic lifetime prediction of power electronic products. Therefore, the PoF methods have been investigated intensively in recent years and will be adopted in this project.

The design and operational demands is based on mission profile loading, which is a representation of the relevant operational and environmental conditions during an entire life cycle. The mission profiles is taking into account the long term operational variations e.g. wind speeds, solar irradiance fluctuations, temperature ranges, etc. For power devices in particular the loading caused by these factors will result in temperature cycling and the damage accumulation will cause wear-out. Applying these real field loading conditions

to lifetime models which describes certain physical failure mechanisms is resulting in a improvement in lifetime estimation compared to handbook based methods [55].

As stated earlier, the time-to-failure of a population of components with the same part number could vary due to material tolerance and manufacturing variation. Additionally the coefficients of the lifetime models are based on results obtained at some certain testing conditions. These models are used with components operating under different conditions, the uncertainties in the lifetime models due to different operating condition should also be taken into account. Finally, the loading conditions caused by the mission profiles will vary on a year-to-year basis causing uncertainty in operating conditions [58].

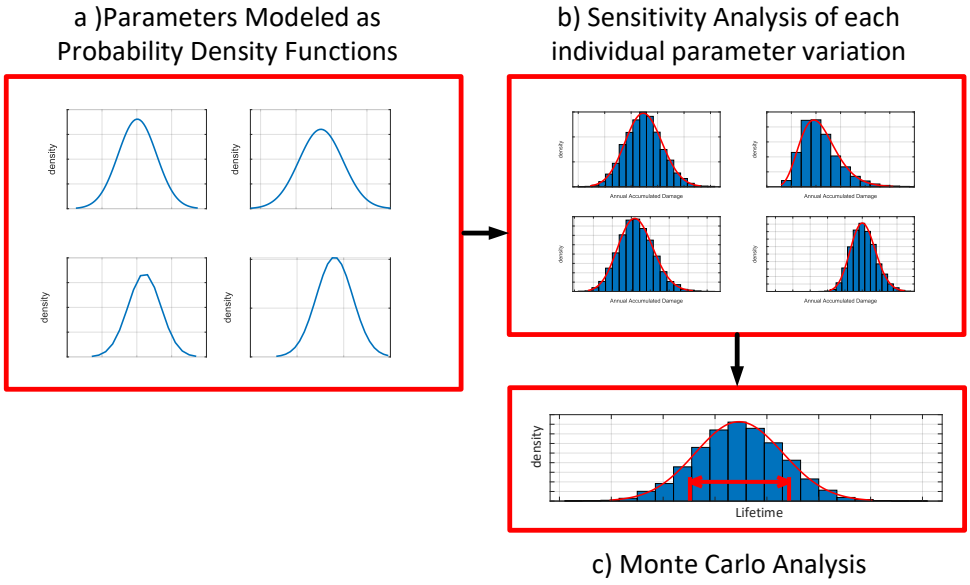


Figure 1.8: Monte Carlo analysis flowchart

The above mentioned uncertainties are taken into account by means of applying a sensitivity analysis, for each of the known parameters. The uncertainty is modeled as a probability density function. Random samples are taken from each of the modeled parameter distribution, so the influence of each uncertainty in the system on the lifetime can be known. In the end a Monte Carlo analysis is performed, where the variations of all the parameters are included and an overall lifetime distribution is obtained. The resulting lifetime is presented with a confidence interval (CI). Finally, the lifetime of the complete system can be obtained by means of reliability block diagram based on the reliability of each component of interest. The flowchart of a Monte Carlo analysis is shown in Figure 1.8.

## 1.3 Case study

In terms of being the technology with most installed renewable power capacity, PV is globally the prefered type. In 2018 alone there was added 100 Gigawatts (GW) of solar PV power capacity which accounted for 55% of new renewable capacity, while wind power accounted for 28% as shown in Figure 1.9 [50].

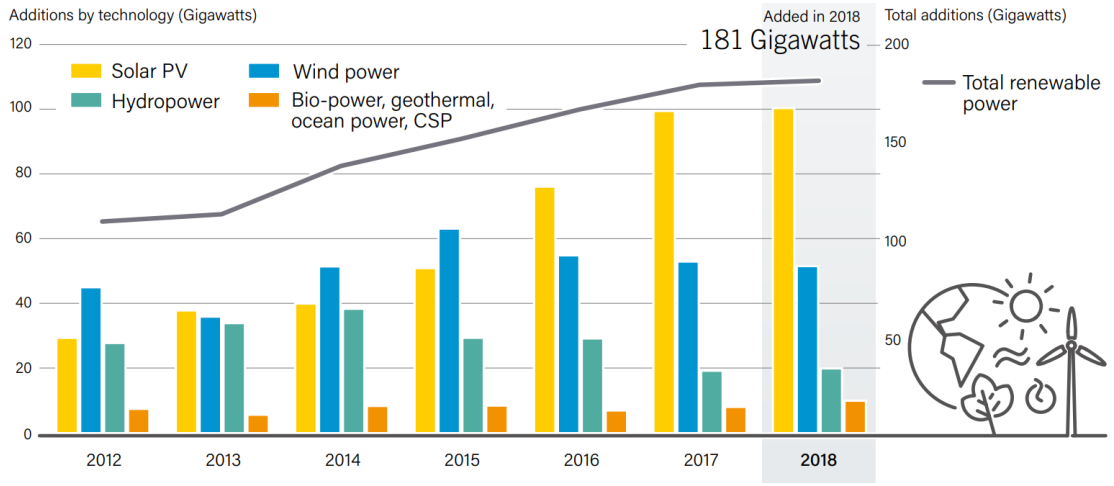


Figure 1.9: Annual Additions of Renewable Power Capacity [50]

The composition of installed renewable power is currently shifting among the different technologies. Hydropower is no longer accounting for half of the cumulative renewable power capacity, falling to 48% as of the end of 2018. Wind power on the other hand rose to compromise to about 25% and PV exceeded 20%. In total renewable energy now accounts for more than 33% of the world's total installed power generation capacity [50].

The combination of PV being the renewable technology with most newly installed capacity and PV inverters also being identified as the assemblies which have the highest failure rate compared to other parts, gives rise to examine the reliability of PV inverters. The case study will therefore comprise a three-phase 2 level voltage source PV-inverter (2L-VSI) in order to illustrate the proposed reliability methods. The inverter stage is compromised of an IGBT module of 1200V/50 A as depicted in Figure 1.10. As previously stated, semiconductor components exposed to cyclic thermal stress are identified as being critical ones, which are prone to fail [78]. The lifetime of the active switches and diodes in the power module and the boost stage will therefore be estimated. According to a survey presented in [73] capacitor is also one of the most reliability critical component in converter systems as presented in Figure 1.11

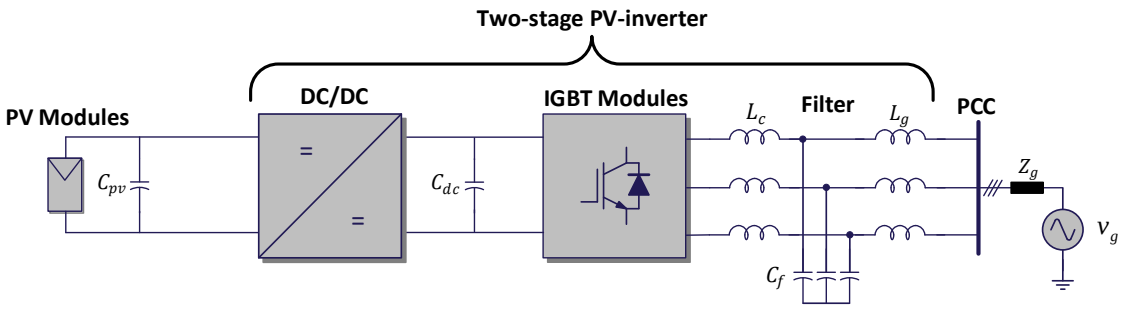


Figure 1.10: Grid connected PV-system: $C_{pv}$ is the PV input capacitor, DC/DC is the boost stage, $C_{dc}$ is the DC-link capacitor, and PCC is the point of common connection.

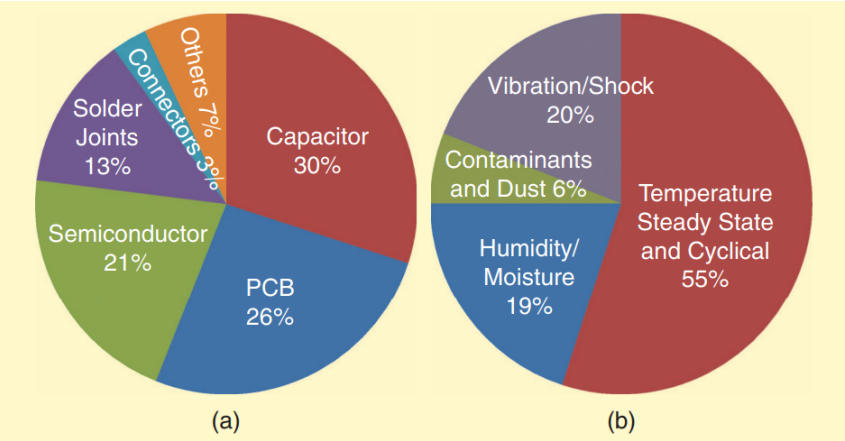


Figure 1.11: Survey on failures in power electronic systems (a) failure distribution among components, (b) source of stress distribution for failures [73]

The DC-link capacitor will therefore also be evaluated in terms of lifetime.

## 1.4 Lifetime evaluation of IGBTs

Among the components in renewable power generation, IGBT modules are known to be one of the most fragile [7]. The failure modes of IGBTs can generally be divided into two main categories: chip related and packaging related. Undesired phenomenons such as electrical overstress can lead to catastrophic failures, but in modern day power systems these failures are covered by the protection system, instead the research is focused on packaging related failures. Figure 1.12 shows the internal structure of an IGBT module with a typical bond-wire [17]

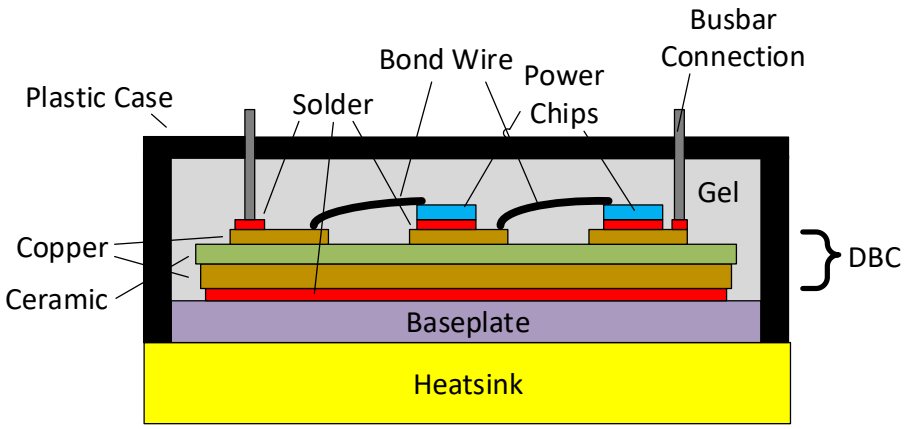


Figure 1.12: Internal structure of IGBT power module

When the converter is subjected to a fluctuating loading it causes long time power cycling. The temperature will fluctuate accordingly to the applied mission profile and to the line frequency cycles. As a result of different mechanical properties of the multilayered module, each layer inhibits different coefficients of thermal expansion (CTE). The heat loss is mostly transferred vertically downwards and the temperature gradient, which is different for each

layer, arises from top to bottom. The alternating electrical stress and the accompanying mechanical stress causes the bond wires to bend, which in worst case can lead to cracking between the aluminium lead of the bond-wire and the silicon of the power chip. The cracking will eventual spread under continuously thermal stress and in the end it will lead to bond-wire lift off [77]. The root cause of failure can therefore be identified as the internal temperature fluctuations and the difference in CTE is leading to mechanical stress on the interconnected materials in the power module. Experience show that power cycles with periods of milliseconds to tens of seconds leads to bond-wire lift off, while the ones with cycling periods of several minutes lead to baseplate solder fatigue also due to CTE mismatch. Mission profile dictated stress will cause cycling periods of several minutes while the line frequency will cause them in the millisecond range, which implies that both failures can occur at long time operation. In this project focus will be on the slow cycling stress caused by the mission profile and not on the stress caused by line frequency loading [69].

Newly adopted constraints of power devices tends to reflect itself in terms of complicating reaching the reliability demands. The increasing demands is due to power devices being introduced in new applications e.g. automotives, which pushes the constraints on weight and space reduction, operating temperatures and increasing voltages. Along with the continuous reliability improvement of devices, the traditional reliability assessment methods that is basing the failure rate solely on experience are being replaced, as these will require different test of millions of accumulated hours in order to achieve some statistical precision. Instead built-in closed-loop reliability assessment tools are introduced. The reliability performance is thereby a part of the design and manufacturing phase.

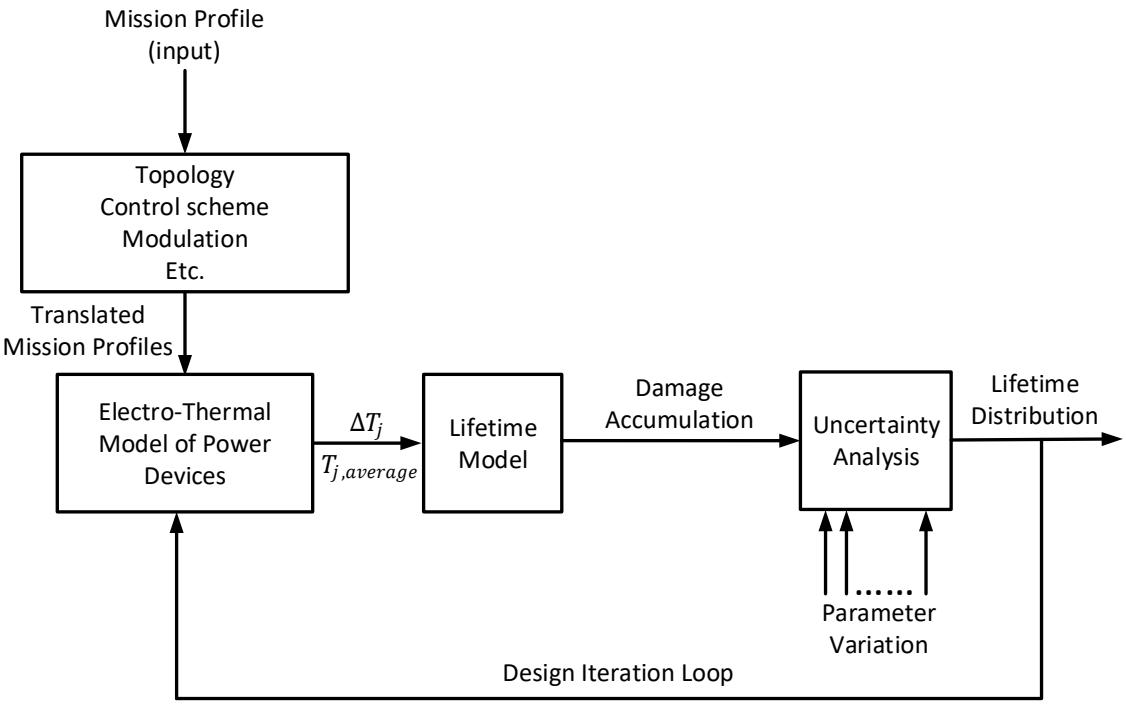


Figure 1.13: Example of Design for Reliability

In case of not meeting the demands, devices are being redesigned to deal with the initial

specifications [71] [58]. The general aspects of the design for reliability method can be illustrated as shown in 1.13. The resulting lifetime distribution is iterated back until a proper selection of the power devices guarantees the lifetime target. Using different design specifications will also lead to a diverted stress and different failure modes can appear. The change in failure modes will be obvious if the slope of the failure distribution on the Weibull chart differs from one another, which is part of the lifetime analysis [10]. The main advantage of this method is that the definitions of the root cause of the failure mechanisms and their relationship with product specifications can be obtained. Additionally, the variations in product design will provide knowledge of the constituting elements relationship with the loading and how the loading affect the product reliability [16].

Junction temperature is the main factor which causes power devices to fail in accordance with the previous mentioned failure mechanisms. In the conditions for the case renewable generation the temperature fluctuations can be divided into short, medium and long time scales. The short time scale is the fluctuations which will resonate around the fundamental frequency caused by output of the power converter. The medium time scale fluctuations is caused by the input and output power fluctuations of the power converter due to changes in the amount of available energy such as solar irradiance. The long time scale fluctuations are those caused by the slowly changing ambient temperature. Each of these different time scale fluctuations will contribute to lifetime consumption of the power module [19].

The most commonly used method to estimate the junction temperature is by means of a thermal network representing all the layers of the module. Initially, the power loss of the device is calculated in accordance with the operating conditions and then the junction temperature is calculated by networks representing the case to ambient temperature difference and the junction to case temperature difference [57]. The thermal network parameters are either given by manufacture of the device or extracted via finite element analyses or experimental characterization. The limiting factor in terms of accuracy is the use of a one dimensional thermal network when in reality the heat distribution is three-dimensional. Also the accuracy of the power loss model will influence the estimation of the junction temperature[6].

Finally, customers are interested in lifetime expectancy under certain operating conditions, since targeted lifetime evaluations can be a tool to decrease maintenance cost but also help to develop new designs, which are optimized to suit the specific operational conditions and therefore provide a longer service life [1]

### Lifetime Model

There are two main types of models, which are the physical models and the empirical based models. The physical based models take into account the strain of the material and combines it with ageing testing data. The main advantage is that is has a good reflection of actual failure mechanisms but it also has the disadvantage of complicated mathematical expression combined with the difficulty of obtaining the actual parameters. In contrast, the use of analytical models is pretty straight forward and they are therefore also the most widely used. Analytical models are based on fitting experimental lifetime data along with relations containing the main factors, which influence the lifetime, and the number of

cycles to failure. An example of testing data provided by a leading manufacture is shown in Figure 1.14 [76].

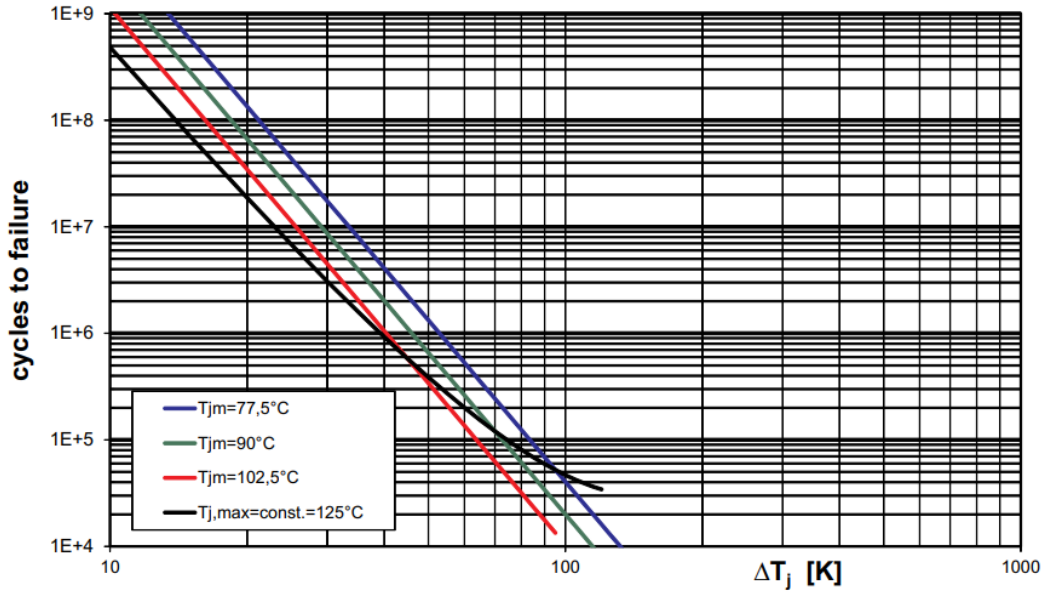


Figure 1.14: Number of cycles to failure dependency on temperature cycling amplitude and mean temperature [76]

As shown in Figure 1.14 the two quantities relating the number of cycles to failure are the temperature cycling amplitude, $\Delta T_j$ and the mean junction temperature, $T_{jm}$. A commonly used empirical model, which accounts for the junction variation temperature only, is the Coffin-Manson model, which can be expressed as [44]

$$N_f = \alpha(\Delta T_j)^{-n} \tag{1.7}$$

The parameters $\alpha$ and $n$ is obtained from fitting the testing data curves shown in Figure 1.14. In order to improve the accuracy, an extension of the Coffin-Manson formula, which includes the Arrhenius equation, which takes into account the mean junction temperature and which can be expressed as [34]

$$N_f = \alpha(\Delta T_j)^{-n} \exp\left(\frac{E_a}{KT_{mean}}\right) \tag{1.8}$$

where K denotes the Boltzmann constant and $E_a$ is the activation energy. As the failure of the power devices is caused by the damage of each cyclic stress applied, the lifetime estimation is to be based on the accumulation of damage caused by each of these cycles. A widely used assumption is the linear damage accumulation, which is known as Miner's rule and which can be expressed as [80]

$$A_D = \sum_{i=1}^{n} \frac{n_i}{N_{f,i}} \tag{1.9}$$

where $n_i$ is the number of cycles of the $i^{th}$ stress level and $N_{f,i}$ is the corresponding number of cycles until the end-of-life. When $A_D = 1$, the end-of-life is reached and the estimated

lifetime can then by obtained as the reciprocal value of the accumulated damage.

$$\text{Lifetime} = \frac{1}{A_D} \tag{1.10}$$

The thermal loading cannot be directly applied to a lifetime model as a result of its dynamical nature and therefore a counting algorithm is necessary [61]. The counting algorithm extracts the discrete values of the variables of interest, i.e., the junction temperature variation amplitude $\Delta T_j$, the mean junction temperature $T_{j,mean}$ and the cycle period $t_{on}$ for the amount of cycles contained in the stress range, $n_i$. The working principle of the algorithm is the counting of the load reversals and each obtained cycle is defined as a hysteresis loop in the stress/strain plane. Each of these hysteresis loops have a strain range and a mean stress associated with it that can be compared with the constant amplitude [51]. The main working principle of the algorithm is depicted in Figure 1.15

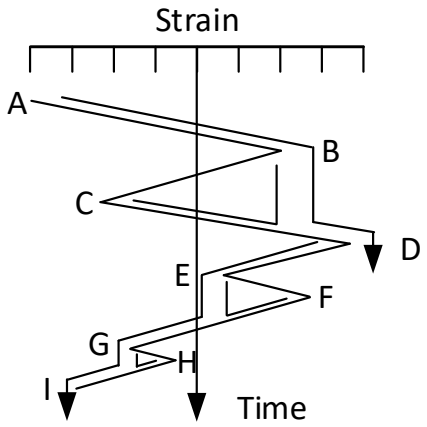


Figure 1.15: Working principle of the rainflow algorithm

it can be observed in Figure 1.15, that the load reverses at point B and the material will therefore unload elastically onto point C. When the load is reapplied from point C to D the material will be assummed to be elastically deformed in a magnitude which corresponds to that of point B, which is remembered from prior time history and the deformation continues along the path from A to D as if step B to C never occurred. A flowchart of the entire workflow, which is needed to obtain a lifetime prediction of power devices, is shown in Figure 1.16. Initially, the environmental factors contained in the mission profile need to be translated into the thermal loading profile of the power devices. Secondly, the irrational loading profile needs to be categorized into quantities, which are applicable for the lifetime model by means of the rainflow algorithm. Thirdly, the number of thermal cycles, which the module is able to withstand, is calculated and then compared to the amount of extracted cycles via the counting algorithm. With the comparison of the number of cycles to failure and the amount of extracted cycles, the accumulated damage caused by applying the mission profile to the PV-system is obtained. In the end, the lifetime expectancy can be obtained from the results of the accumulated damage. The complete methodology is used in the project to obtain a lifetime expectancy of the IGBT power modules operating in the two-stage PV-inverter.

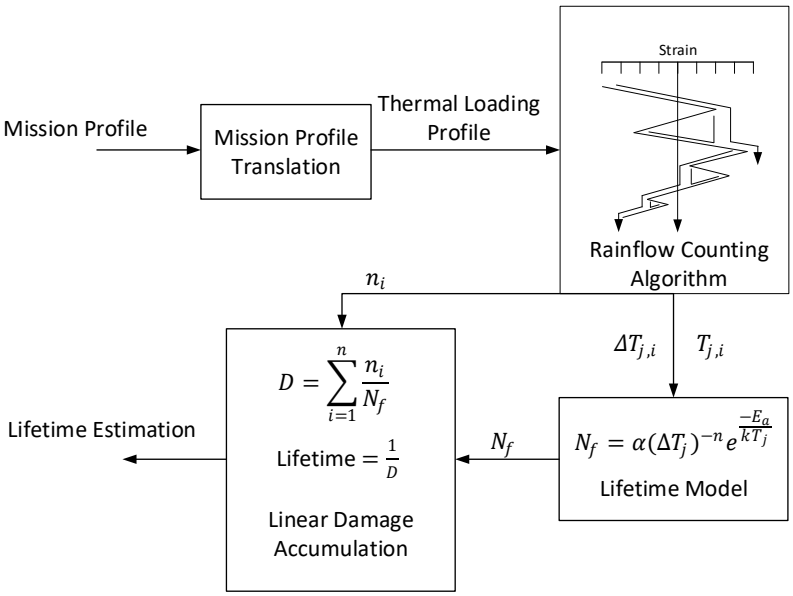


Figure 1.16: Flow chart of the lifetime estimation

## 1.5 Lifetime estimation of DC-Link capacitors

DC-link capacitors serve as an important part of the PV inverter in terms of size, cost and lifetime. Its main functionalities are to reduce the DC-link voltage ripple, absorb the harmonics and provide energy storage when needed. The DC-link capacitors chosen for this particular system is the electrolytic capacitors because of their simplicity and their relatively good cost-effectiveness [70]. The use of this specific type of capacitors introduce some reliability related challenges, such as their tendency to degrade as a result of electrolyte evaporation and electro-chemical reaction, which is highly dependent on the applied electro-thermal stresses [2]. The main source of electro-thermal stresses is the internal self-heating caused by the losses, which are generated by the ripple currents. Not only will the self-heating inflict a rise of the hot-spot temperature, it can also lead to an increase in the equivalent series resistance, which will induce increased losses and thereby accelerate the ageing process [70]. As a consequence, when designing the DC-link capacitors, lifetime is one of the main aspects to consider, which both depends on the inherent capabilities of the capacitor but also on the field operating conditions [56]. The first step to obtain the lifetime of the DC-link capacitor, is to determine the harmonic current spectrum in the DC-link. The harmonic spectrum depends on both the topology on the input side and the topology on the output side, which both contribute to the overall harmonics as shown in Figure 1.17 [79]. In general the spectrum consists of low-order harmonics as a result of unbalance between input and output power and high-order components generated by the switching of power electronic components. The root mean square (RMS) of the current in the entire spectrum influences the thermal loading of the capacitor and therefore also the reliability [46]. At each given frequency in the spectrum, the power loss is the product of the ripple current and the equivalent series resistance (ESR), while the entire power loss is its summation of the whole frequency range as shown in equation (4.3) [72]

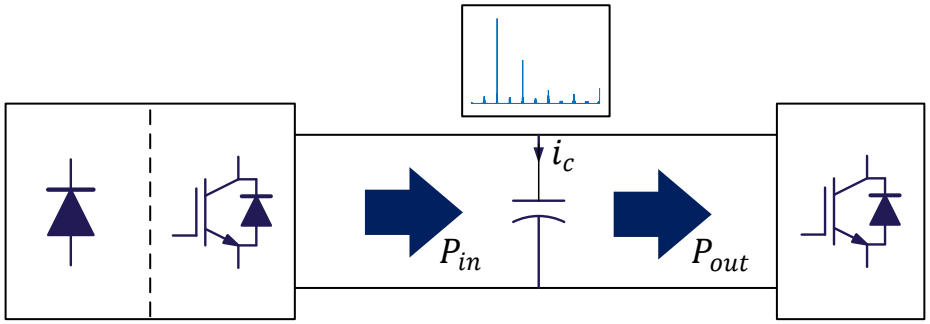


Figure 1.17: Harmonic spectrum consisting of a combination of unbalance in input power and output power and high order switching components

$$P_{loss} = \sum_{i=1}^{n} [ESR(f_i) \cdot I_{rms}^2(f_i)] \tag{1.11}$$

where ESR($f_i$) is the ESR at frequency $f_i$, $I_{rms}$ is the RMS value of the ripple current evaluted at the same frequency, $f_i$. The hotspot temperature is the sum of the internal temperature rise as a consequence of the current stress and the ambient temperature and can be calculated as [75]

$$T_h = T_a + R_{ha} \cdot \sum_{i=1}^{n} [ESR(f_i) \cdot I_{rms}^2(f_i)] \tag{1.12}$$

where $T_h$ is the hotspot temperature and $T_a$ is the ambient temperature. $R_{ha}$ is the total thermal resistance from hotspot to ambient, which consists of two thermal resistances, one from hotspot to case and one from case to ambient. The thermal resistance values are either provided in the manufacture datasheet or determined experimentally

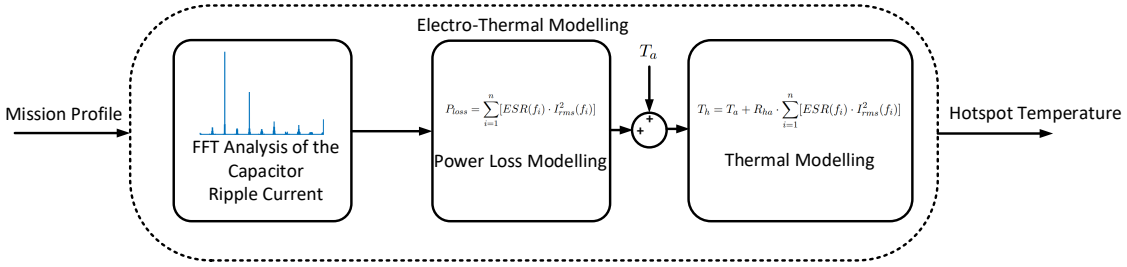


Figure 1.18: Electro-Thermal Modelling of Capacitors

from the obtained thermal loading profile the lifetime can be estimated by widely used lifetime model, which is given as [54]

$$L_f = L_0 \cdot \left(\frac{V}{V_0}\right)^{-p_1} \cdot 2^{\frac{T_0 - T_h}{p_2}} \tag{1.13}$$

where $L_0$, $V_0$, $V$, $T_0$ and $T_h$ is the rated lifetime, rated voltage, applied voltage, rated temperature and hotspot temperature. For the electrolytic capacitors the parameter

denoted $p_1$ is usually in the range of 3-5 whereas the parameter $p_2$ is often at a value of 10 [54]. Some characteristics of the capacitor change during its lifetime such as the ESR, so it can be argued that the damage should be accumulated in a nonlinear fashion but as the rated lifetime, $L_0$ is obtained with a constant stress profile the change of these characteristics is already taken into account when obtaining the rated lifetime. For long term operating conditions, the Miners rule can be applied [28]

$$D = \sum_{i=1}^{n} \frac{l_i}{L_{f,i}} \tag{1.14}$$

in which $l_i$ is the duration of the applied operating profile while $L_{f,i}$ is the time to failure calculated in (1.13), from the specific stress conditions applied from the profile. End-of-life is reached when the damage D = 1. If the predicted lifetime does not fulfill the requirements, different configurations such as number of paralleled capacitors and other types of capacitors will be examined. With the accumulated damage at hand, the static equivalent of the hotspot temperature can be determined, which will provide the foundation of carrying out an uncertainty analysis, as explained in section 1.2. The static equivalent is the most probable value the hotspot temperature will have, i.e. the mean of the probability function, as depicted in the flowchart presenting the damage accumulation shown in Figure 1.19

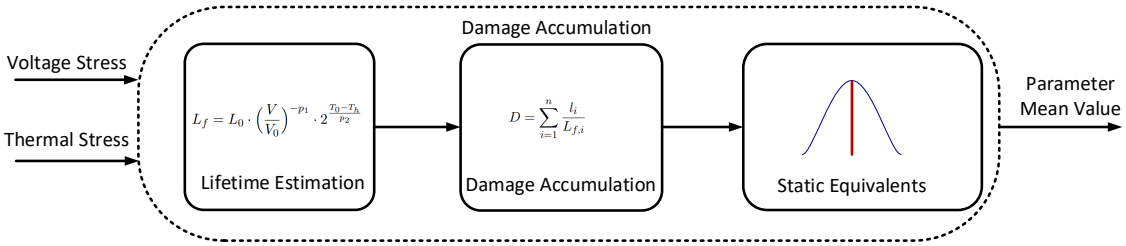


Figure 1.19: Flowchart of how the accumulated damage is obtained

With the main theory in terms of the reliability of the prone-to-fail components at hand, the overall objectives of the project can now be stated.

## 1.6 Project objectives

***The main objective of this project is to apply the general theory presented in this chapter on a specified PV inverter. The lifetime of the entire system, is to be determined by means of in-depth reliability analysis. When the lifetime of each subsystems is determined, the reliability critical components can be identified and the overall system reliability can be obtained. Additionally design for reliability concepts will be incorporated in the analysis throughout the report. The design for reliability aspect will consist of analysing which configurations and choice of components will improve the reliability of the system.***

## 1.7 Methodology

The first step is to get the complete system specified. As the type of renewable source has been decided, next step is to choose at which part of the power system, is this particular subsystem located. The voltage levels and the amount of processed power depends on the system being located on transmission or distribution level. With the overall framework clarified the methodology used to obtain the lifetime of the PV inverter can be summarised as

- Modelling and control of each subsystem is developed
- Electro-thermal modelling of the relevant components
- Mission profile based lifetime estimation
- Uncertainty analysis
- Reliability block diagram
- Simulations and experiments

Each step described will be thoroughly explained later in the report and the workflow of the entire method is depicted in Figure 1.20

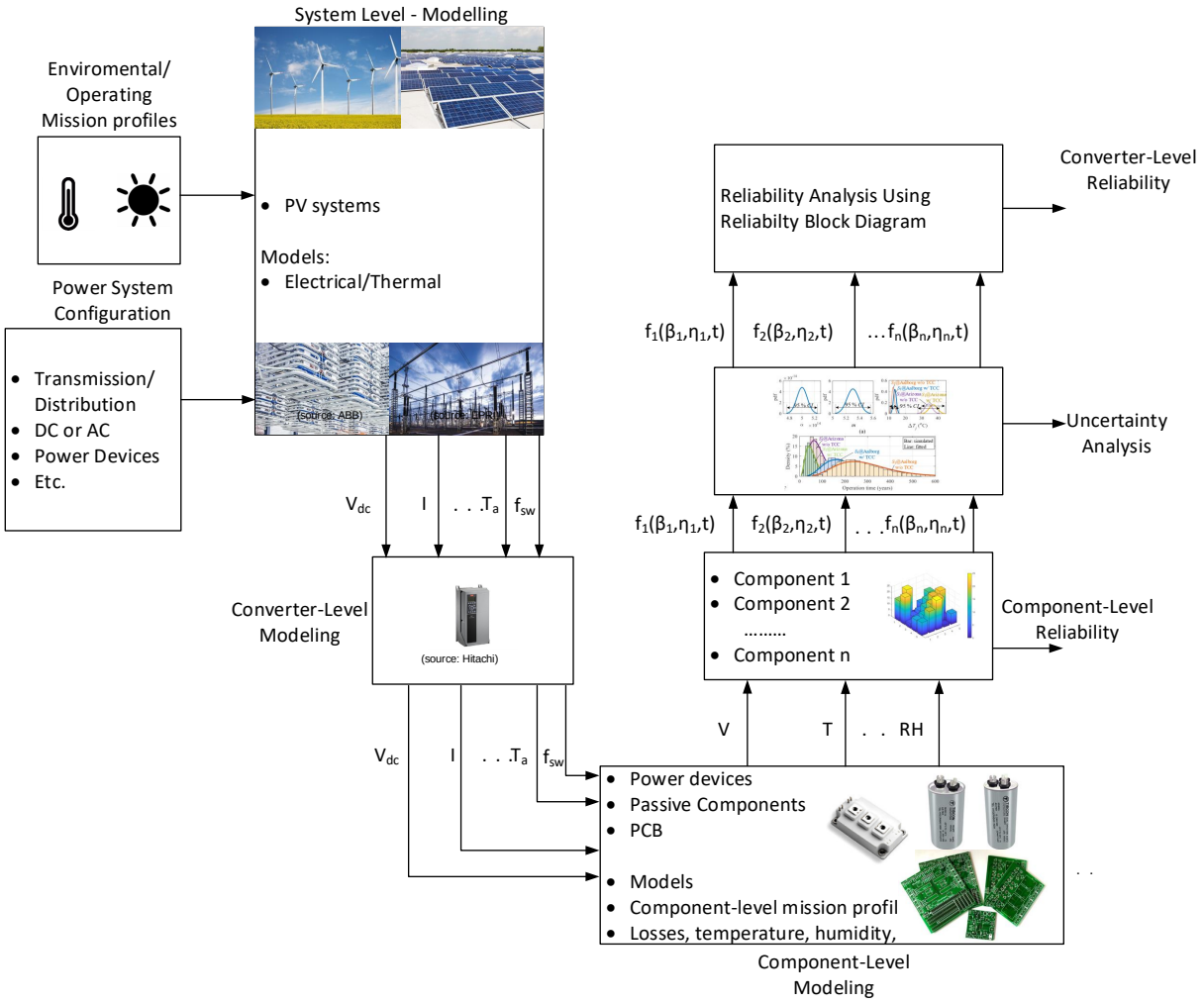


Figure 1.20: Methodology flowchart to obtain lifetime

## 1.8 Problem statement

In the introduction it was concluded that renewable generation is becoming the preferred source of production of electricity. It was also concluded that two-thirds of the net installations in 2018 were renewable based, which marked the seventh consecutive year, where renewable installations were above 50 %. One of the key technologies used to obtain a renewable based energy supply, is power electronics, which constitute a substantial part of the power system and is widely used with renewable power generation. It was shown that power electronic converters are identified as the most fragile sub-systems, and does therefore constitute the bottleneck of the entire system, in terms of reliability. Not only will the fragility of power electronic components alter the cost of energy conversion negatively but also induce the risk of a reduction of delivered energy due to system downtime. It is therefore of utter importance to be able to estimate the lifetime of power electronic systems and thereby increase the availability by means of predictive maintenance, which results in lowering the Levelized-Cost of Energy (LCOE).

Finally, it was also concluded that PV is the globally most preferred technology in terms of most installed renewable power generation and PV inverters are also identified as the assemblies which have the highest failure rate compared to other parts. It is therefore highly relevant to perform in-depth reliability analysis on a PV inverter, which leads to the following problem statement.

***Is it possible to obtain mission profile based lifetime estimation on a grid-connected PV inverter and thereby identify the critical components in terms of reliability***

The following aspects are covered in order to perform an coherent analysis

- Real field environmental data are used as loading profile to obtain results which are in accordance with real operational PV generation systems
- Uncertainty aspects of both electrical parameters and lifetime model parameters are incorperated in the analysis, in order to obtain realistic lifetime predictions
- Design for reliability will be incorporated to optimize the reliability of the system

# System Specification and Modelling and Control

# 2

*In this chapter, the system is specified in terms of used components, its dimensions and its ratings. Additional both stages are modelled and their controlled methods are developed to provide the ability to manipulate the stress on the components according to the applied mission profile*

## 2.1 Initial considerations

As a starting point a 12kVA inverter was chosen, because a physical converter of this rating was available for laboratory testings and validation of the obtained results. From that starting point the dimensions of the renewable energy source, i.e. the PV array could be determined. The sizing of the PV will influence the amount of output power and therefore also the amount of stress applied on the power electronic components.

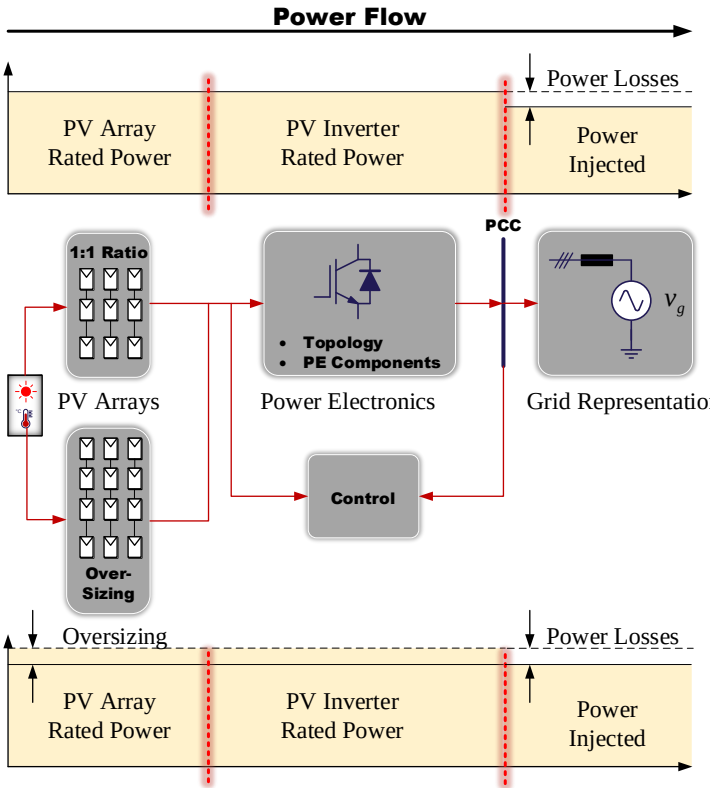


Figure 2.1: The concept of PV Array Sizing Ratio

A common approach is to oversize the PV-array in to respect to the converter rating in order to obtain a wide-scale utilization of such systems, as the PV-array rarely operates at its ratings due to insufficient available solar irradiance. The amount of surplus loading very much depends on the installation site, which also impacts the converter lifetime. In Denmark, the solar irradiance is relatively low during winter time compared to summer time and in countries with this type of changing weather during the seasons, the converter lifetime is highly dependent on the sizing of the PV array [62]. The concept of PV array sizing and the delivered power is depicted in Figure 2.3. In this project it is chosen to size the array conservatively, so its output power matches the rated power of the converter. Now that the rating of the array is fixed the configuration of it is to be determined in terms of number of paralleled strings and how many modules are connected in series in each string. Initially the DC bus voltage is to be determined with the goal of having a suitable output voltage of the PV-array configuration. In order to be able to create the grid voltage, the DC-link voltage has to be off magnitude of at least the peak value of the line-to-line voltage

$$V_{DC,min} = \sqrt{2} \cdot \sqrt{3} \cdot V_{phase} = \sqrt{2} \cdot \sqrt{3} \cdot 230V \approx 563V \tag{2.1}$$

In order to avoid modulation issues, a considerable margin also has to be included and the DC bus voltage is therefore chosen at 750V. The output voltage of the array should be considerable below the DC bus voltage as the DC/DC stage will control and boost the output voltage of the PV array and the output voltage of the array is therefore chosen at 600V.

## 2.2 Sizing and modeling of the PV array

The PV multicrystalline module BP365 is used in this project due to having access to all its data specifications and its availability in the used simulation software, which is used throughout the project. The electrical characteristics of the BP365 module is summarized in Table 2.1

In order to reach an output power which is in accordance with the rated power of the inverter, the following numbers of modules is needed

$$N_{PV} = \frac{P_{inv}}{P_{max}} = \frac{12000W}{65W} \approx 165 \tag{2.2}$$

Photovoltaic (PV) modules are often connected in series strings to increase the input DC voltage, which is applicable for the PV inverter. The number of modules connected in series in each string can be determined by dividing the total desired output voltage of the array with the voltage available at maximum power operation of each individual module

$$N_{series} = \frac{V_{DC}}{V_{mp}} = \frac{600}{17.6} \approx 34 \tag{2.3}$$

and finally the amount of needed strings can be obtained by dividing the total amount of modules with the amount of modules in each string

$$N_{strings} = \frac{N_{PV}}{N_{series}} = \frac{165}{34} \approx 5 \tag{2.4}$$

| Electrical Characteristics of BP365 PV Module | |
|---|---|
| Maximum Power $P_{max}$ | 65W |
| Voltage at Maximum Power $V_{mp}$ | 17.6V |
| Current at Maximum Power $I_{mp}$ | 3.69A |
| Warranted Minumum Power $P_{max}$ | 60W |
| Short Circuit Current $I_{SC}$ | 3.99A |
| Open-Circuit Voltage $V_{OC}$ | 22.1V |
| Temperature Coefficient of $I_{SC}$ | (0.065±0.015)%/°C |
| Temperature Coefficient of $V_{OC}$ | -(80±10)mV/°C |
| Temperature Coefficient of Power | -(0.5±0.05)%/°C |
| NOCT | 47 ± 2 °C |
| Number of Cells In Series | 36 |
| Boltzmann Constant, $k$ | $1.38{\cdot}10^{-23}\ J/m^2K$ |
| Standard Test Condition Temperature, $T_{STC}$ | 298.15K |
| Elementary Electron Charge, $q$ | $1.602{\cdot}10^{-19}C$ |
| Silicon Band Gap Energy, $E_g$ | $1.8{\cdot}10^{-19}J$ |

Table 2.1: Electrical characteristics of the used PV module

With regards to the electrical circuit modelling of the PV-module it should account for the non-linear I-V characteristics, which is an effect of the temperature and the insolation strength. The essential circuit elements is a single diode in parallel with a current source, which output is proportional to the solar irradiance applied to the module. Adding some resistance to the circuit will take into account the power loss as a result of circulating current will complete the model. The precision but also the level of complexity increases as the number of diodes and resistors increase. In this project where the modelling of the PV module is not the main focus, a single diode equivalent circuit seems to provide a reasonable trade-off between precision and simplicity [12]. The single-diode equivalent circuit is governed by a non-linear equation with five unknown parameters, which are the photo-generated current, $I_{ph}$, the diode ideality factor, $n$, the dark saturation current of the diode, $I_o$, the series resistance of the module, $R_s$ and the shunt resistance of the module, $R_p$. The single-diode circuit diagram is shown in Figure 2.2

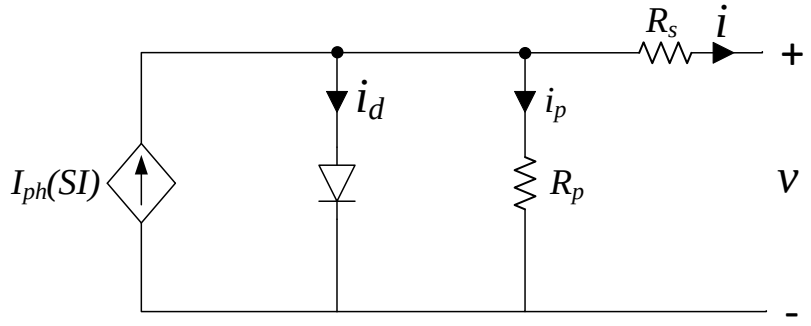


Figure 2.2: Single-Diode Equivalent Circuit for PV Module

Applying Kirchoffs current law (KCL) on upper left node the following expression for the output current, $i$ is obtained

$$i = I_{ph} - i_d - i_p = I_{ph} - I_o\Big(e^{\frac{v+R_s \cdot i}{n \cdot N_s \cdot V_{th}}} - 1\Big) - \frac{v + R_s \cdot i}{R_p} \tag{2.5}$$

where the current through the diode, $i_d$ and the current through the shunt resistor, $i_p$ is stated explicitly. $N_s$ is the number of series connected PV cells in the module and $V_{th}$ is the thermal voltage of a single cell, which can be expressed as

$$V_{th} = \frac{kT}{q} \tag{2.6}$$

where $k$ is the Boltzmann constant, $T$ is the standard temperature in Kelvin and $q$ is the electron charge. There exist research with numerous different ways to determine the unknown parameters, where most of them is in terms of direct analytical expression, which depends only on datasheet values [68]. The method adapted in this project involves direct analytical expressions with the aid of datasheet values to determine $I_{ph}$,$n$ and $I_o$ whereas $R_p$ and $R_s$ are estimated using the Lambert-W function. The adapted method was first proposed in [26]. Initially is should be noted, that the operating module temperature used, $T$, in the following expressions is related to the ambient temperature by

$$T = T_a + \frac{(NOCT - 20)}{0.8} G \tag{2.7}$$

in which $G$ represents the amount of applied solar irradiance, NOCT is the nominal operating temperature of the module, which is provided in the datasheet. Now consider equation (2.5) under short circuit condition where $i = I_{sc}$ and $v = 0$, then the following expression is obtained

$$I_{sc} = I_{ph} - I_o\Big(e^{\frac{R_s \cdot I_{sc}}{n \cdot N_s \cdot V_{th}}} - 1\Big) - \frac{R_s \cdot I_{sc}}{R_p} \tag{2.8}$$

and with the knowledge that $I_o$ being in the proximity of zero and that the last term is negligible, as a result of the ratio of the two resistances is small when compared to the photovoltaic current, makes the following assumptions valid

$$I_{ph} = I_{sc} \tag{2.9}$$

where the value of the short circuit current can be found in the datasheet. Consider now equation (2.5) under open circuit conditions where $i = 0$ and $v = V_{oc}$ the following is obtained

$$0 = I_{ph} - I_o\Big(e^{\frac{V_{oc}}{n \cdot N_s \cdot V_{th}}} - 1\Big) - \frac{V_{oc}}{R_p} \tag{2.10}$$

and by adopting (2.9), noting that $I_{ph} \gg V_{oc}/R_p$ and $e^{\frac{V_{oc}}{n \cdot N_s \cdot V_{th}}} - 1 \gg 1$ following is obtained

$$I_o = I_{sc} e^{\frac{-V_{oc}}{n \cdot N_s \cdot V_{th}}} \tag{2.11}$$

The formula used for obtaining the diode ideality factor consists solely on the temperature coefficients given in the datasheet and can be expressed as [18]

$$n = \frac{\alpha_v - \frac{V_{oc}}{T_{STC}}}{N_s V_{th}\Big(\frac{\alpha_i}{I_{ph}} - \frac{3}{T_{STC}} - \frac{E_g}{kT_{STC}^2}\Big)} \tag{2.12}$$

where $\alpha_v$ is the open-circuit voltage temperature coefficient, $\alpha_i$ is the short-circuit current temperature coefficient, $E_g$ is the silicon energy band-gap, $k$ is the Boltzmann constant and $E_g$ is the silicon band gap energy. All the values for the before mentioned coefficients is avaliable through Table 2.1. Finally the series and shunt resistance of the module is given as [26]

$$R_s = \frac{xnV_{th} - V_{MPP}}{I_{MPP}} \tag{2.13}$$

and

$$R_p = \frac{xnV_{th}}{I_{ph} - I_{MPP} - I_o(e^x - 1)} \tag{2.14}$$

where $V_{MPP}$ and $I_{MPP}$ is the maximum power point voltage and current respectively. The coefficient x is given by

$$x = \frac{2V_{MPP}}{nN_sV_{th}} - \frac{2V_{MPP}^2}{n^2N_s^2V_{th}^2} + W\left\{\frac{V_{MPP}(2I_{MPP} - I_{ph} - I_o)e^{\frac{V_{MPP}(V_{MPP}-2nV_{th})}{n^2n_s^2V_{th}^2}}}{nN_sI_oV_{th}}\right\} \tag{2.15}$$

where $W\{...\}$ denotes the Lambert-W function, which is a means to solve functions of the particular form $y = xe^x$. The Lambert function was evaluated using the software MATLAB®. The PV parameter values obtained using the presented theory is shown in Table 2.2

| Obtained Electrical PV module Parameters | |
|---|---|
| Photo generated Current $I_{ph}$ | 3.99A |
| Diode Ideality Factor $n$ | 1.186 |
| Dark Saturation Current of the Diode $I_o$ | $7.1\cdot 10^{-9}$A |
| Series Resistance $R_s$ | 0.112 Ω |
| Shunt Resistance $R_P$ | 157.68 Ω |

Table 2.2: Electrical Characteristics of the Used PV Module

Obtaining the parameters is not going to fully emulate the behaviour of the PV modules as environmental conditions dictated by the temperature and solar irradiation variations does also need to be accounted for. In order to do so, the photovoltaic current, $I_{ph}$ will be made dependent on solar irradiation and the dark saturation current of the diode will be made temperature dependent. In this project, it is assumed that only the photo-generated current and the dark saturation current are dependent on environmental conditions. First the temperature dependent short circuit current is presented, as it is needed to obtain a temperature dependent saturation current $I_o$(T) [64]

$$I_{sc}(T) = I_{sc}\Big[1 + \frac{\alpha_i}{100}(T - T_{STC})\Big] \tag{2.16}$$

and the temperature dependent open circuit voltage is given as

$$V_{oc}(T) = V_{oc} + \alpha_v(T - T_{STC}) \tag{2.17}$$

and the thermal voltage as

$$V_{th}(T) = V_{th}\frac{T}{T_{STC}} \tag{2.18}$$

which provides the knowledge of the temperature dependent dark saturation current can be expressed as

$$I_o(T) = \Big(I_{sc}(T) - \frac{V_{oc}(T) - R_s I_{sc}(T)}{R_p}\Big) e^{\frac{-V_{oc}(T)}{nN_s V_{th}(T)}} \tag{2.19}$$

the temperature dependent photo-generated current is then described as

$$I_{ph}(T) = I_o(T) e^{\frac{V_{oc}(T)}{nN_s V_{th}(T)}} + \frac{V_{oc}(T)}{R_p} \tag{2.20}$$

the final expression for the photo-generated current with the inclusion of the solar irradiance dependency is simply obtained by the multiplication of the solar irradiance

$$I_{ph}(G,T) = I_{ph}(T)G \tag{2.21}$$

Finally the expression which describes the i-v characteristics of the PV module, (2.5) can be expressed in terms of temperature and solar irradiance

$$i = I_{ph}(G,T) - I_o(T)\Big(e^{\frac{v+R_s i}{nN_s V_{th}(T)}} - 1\Big) - \frac{v + R_s i}{R_p} \tag{2.22}$$

It can observed that the equation describing the i-v characteristics contain an algebraic loop, which complications is dealt with in simulation by inclusion of a loop filter. The PV module is now specified and the electrical characteristics are modelled as shown in Figure 2.3

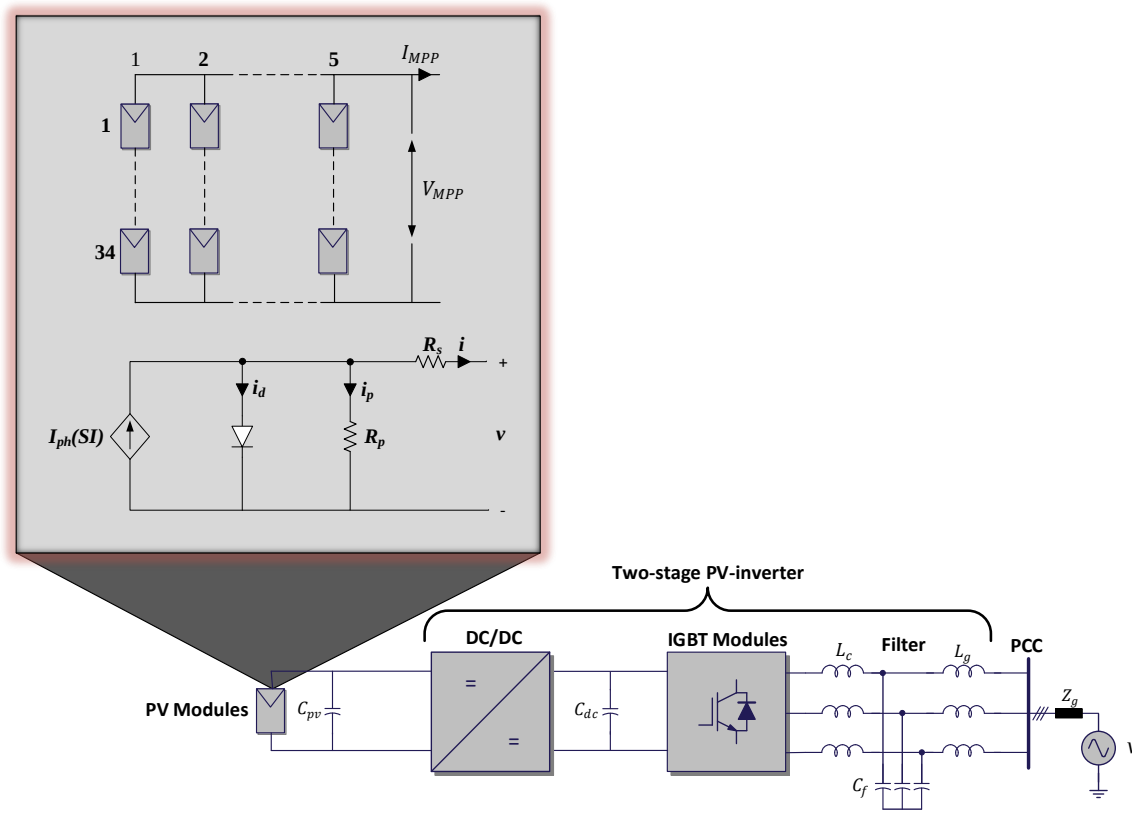


Figure 2.3: PV System With Emphasize on PV Model and Specifications

## 2.3 Modelling of DC/DC stage

The PV array provides a maximum power output for a particular loading condition at a certain reference voltage across its terminals, which is known as the maximum power point (MPP) [25]. The MPP tracker make use of an algorithm which generates the MPP reference voltage. The DC/DC converter is controlled to track the MPP output of the PV array and thereby utilize as much of the generated energy as possible. The equivalent circuit of the well known boost topology is shown in Figure 2.4

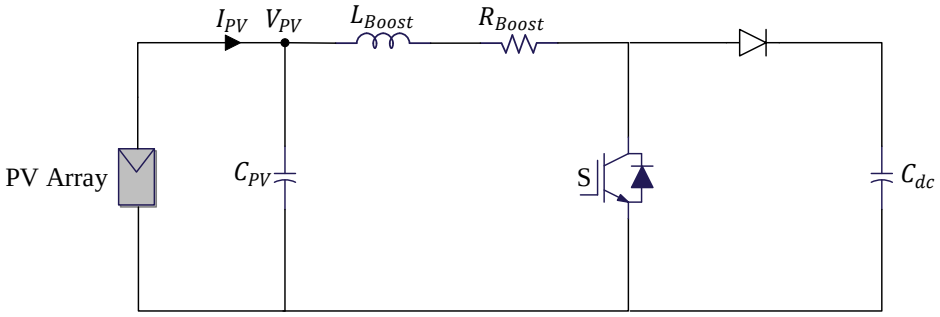


Figure 2.4: Boost Converter Equivalent Circuit

The capacitor $C_{PV}$ is connected across the PV array to reduce the ripple produced by the inductor. The DC link capacitor at the output terminals has the main purpose of making the DC voltage stiff, by making it less vulnerable against load current changes but the capacitors also helps to maintain a proper energy balance between the PV array and the AC grid during transient disturbances. The switching is realized by means of an IGBT based DC chopper module with a high efficient diode from a leading manufacturer [32]. The most relevant preliminary data is summarised in Table 2.3 and the circuit diagram of the module is shown in Figure 2.5.

| IGBT DC chopper power module | |
|---|---|
| Parametrics | DF120R12W2H3_B27 |
| Configuration | Chopper |
| Rated collector-emitter voltage $V_{CE}$ | 1200V |
| Rated continuous collector current $I_{C,nom}$ | 40A |
| Rated repetitive peak collector current $I_{CRM}$ | 80A for $t_p$ = 1ms |
| Rated gate-emitter peak voltage $V_{GE}$ | ±20V |

Table 2.3: Preliminary data of the DC chopper power module [32]

The modelling of the boost converter is based on the state space principle as proposed in [22]. Initially the state equations are obtained for each operational subinterval by means of elementary circuit analysis performed on the circuit shown in Figure 2.4.

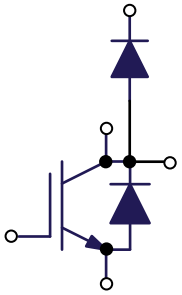

Figure 2.5: DC chopper power mpdule circuit diagram

When switch, $S$ is operating in on-state following expressions can be obtained for the inductor voltage and the input capacitor current

$$C_{PV}\frac{dv_{PV}}{dt} = i_{PV} - i \quad \text{and} \quad L\frac{di}{dt} = v_{PV} - R_{boost}\cdot i - R_{on}\cdot i \tag{2.23}$$

where, $R_{boost}$ is the inductor resistance, $i_{PV}$ is the current delivered by the PV array, $R_{on}$ is the on-state resistance of the IGBT and $i$ is the inductor current. When switch, $S$ is operating in off-state following expression can be obtained for the inductor voltage and the input capacitor current

$$C_{PV}\frac{dv_{PV}}{dt} = i_{PV} - i \quad \text{and} \quad L\frac{di}{dt} = v_{PV} - R_{boost}\cdot i - v_{dc} - V_D \tag{2.24}$$

where $V_D$ is the diode forward voltage. The two set of state equations are now averaged for a entire switching period and small pertubations around the steady-state value are included. The transfer function, which describes the dynamical relation between the small pertubation value of the PV array output voltage, $\tilde{v}_{PV}$ and the converter duty cycle, $d$ is presented in (2.25). For detailed walktrough of the state-space averaging calculations please refer to [22]

$$G_{boost}(s) = \frac{\tilde{v}_{PV}}{d} = \frac{\frac{-K_2}{LC_{PV}}}{s^2 + \frac{K_1}{L}s + \frac{1}{LC_{PV}}} \tag{2.25}$$

where the two constants $K_1$ and $K_2$ are giving by

$$K_1 = R_{boost} + R_{on}D \quad \text{and} \quad K_2 = V_{dc} + V_D - R_{on}I \tag{2.26}$$

Where D is the steady-state duty cycle of the boost converter which is expressed as [22]

$$D = 1 - \frac{V_{PV}}{V_{DC}} = 1 - \frac{600}{750} = 0.2 \tag{2.27}$$

### 2.3.1 Design of Passive Elements

The inductor and the capacitor will be designed based on operational restrictions on the ripple ratio with respect to their steady-state values. Equating the expression for inductor ripple current with a ripple restriction of less or equal to ten percent

$$\frac{\Delta i}{I} = \frac{D(1-D)^2 T_s R}{L} \leq 10\% \quad \Leftrightarrow \quad L \geq 10D(1-D)^2 T_s R \tag{2.28}$$

The active switch is switched at 20000kHz which results in a switching period of $T_s = 50\mu$s and the inverter can be expressed as a load as its role is to control the amount of current injected in the grid

$$R = \frac{V_{DC}^2}{P_{inv}} = \frac{750^2}{12000} \approx 47\Omega \tag{2.29}$$

With these numbers in hand the inductance value obtained is $L \geq 3mH$. As previously stated, the input capacitor, $C_{PV}$ main purpose is to filter out the current ripple introduced by the inductor and the capacitance can therefore be determined on the basis of the ripple current requirements and the maximum allowed voltage ripple, which in this case is chosen to be 3% of the steady-state value, i.e, $\Delta V_{PV} = 18$V

$$C_{PV} = \frac{\Delta i T_s}{8 \cdot \Delta V_{PV}} = 73\mu F \tag{2.30}$$

### 2.3.2 Modified PI method used for control of the boost converter

Regular PI-controllers are often used to control DC/DC converters and they serve the purpose of eliminating the steady-state error by introducing a pole at origin. The pole at origin provides infinite dc gain and as the available gain increase, the error decreases. Regular PI-controllers does also inherent the negative aspect of reducing the phase margin of the system and therefore make it more susceptible to become unstable, when the system is of second order as is the case in (2.25) [27]. Instead of using a regular PI-controller a modified k-factor controller is used in order to obtain higher phase margin. This method is also known as a loop shaping technique in where the transfer function is shaped to obtain some pre-specified dynamical performance requirements.

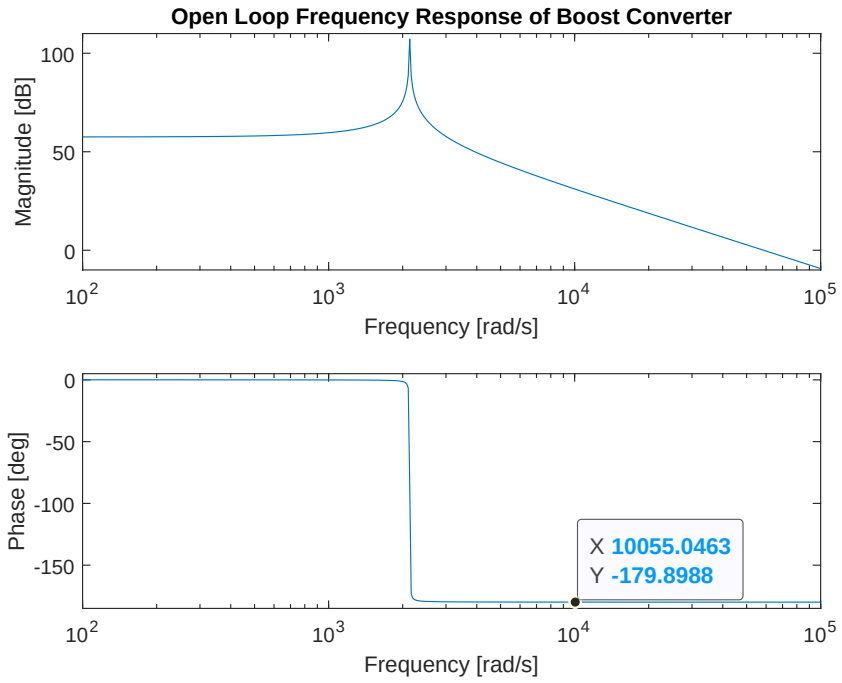


Figure 2.6: Frequency response of the boost converter

The dynamical performance is very much dependent on the bandwidth of the system and therefore a suitable cross over frequency needs be determined. The bandwidth should be chosen to be well above the resonance frequency of the converter to obtain a fast response. At the bandwidth should at the same time be limited to be 1/10th of the switching frequency to avoid amplification of the high order switching noise. Hence, $\omega_{cr} = 10000$ rad/s seems to be a suitable choice, when observing the open loop frequency response shown in Figure 2.6. At the the chosen cross over frequency, $\omega_{cr}$ the phase is at -179.9 degrees and there is no available phase margin in the uncontrolled system. If a regular PI was used an additionally 90 degree phase lag would be introduced and the system would inherent high tendency of becoming unstable. What is needed is a controller which is able to boost the phase and remove the phase lag at the chosen cross over frequency in order to achieve a desired phase margin, which a type III k factor controller is capable of

$$G_c(s) = \frac{K_c}{s} \frac{\left(1 + \frac{s}{\omega_z}\right)^2}{\left(1 + \frac{s}{\omega_p}\right)^2} \tag{2.31}$$

where

$$\omega_z < \omega_p \tag{2.32}$$

This type of controller can be designed accurately for a specified phase margin and cross over frequency instead of using zero-pole cancellation. As the integration part is introducing additional phase lag a type III is chosen which has a double zero pair and a double pole pair, which makes it capable of introducing a phase boost of $\phi_{boost} \geq 90$ degrees. The main idea is to place the zeros at an appropriate location so the phase boost occurs at the chosen cross over frequency, adjust the constant gain to shift the frequency response up in order to achieve the required bandwidth and also to place the pole pair at high frequency in order to attenuate the high frequency switching noise. The gain and phase characteristics of the controller is shown in Figure 2.7

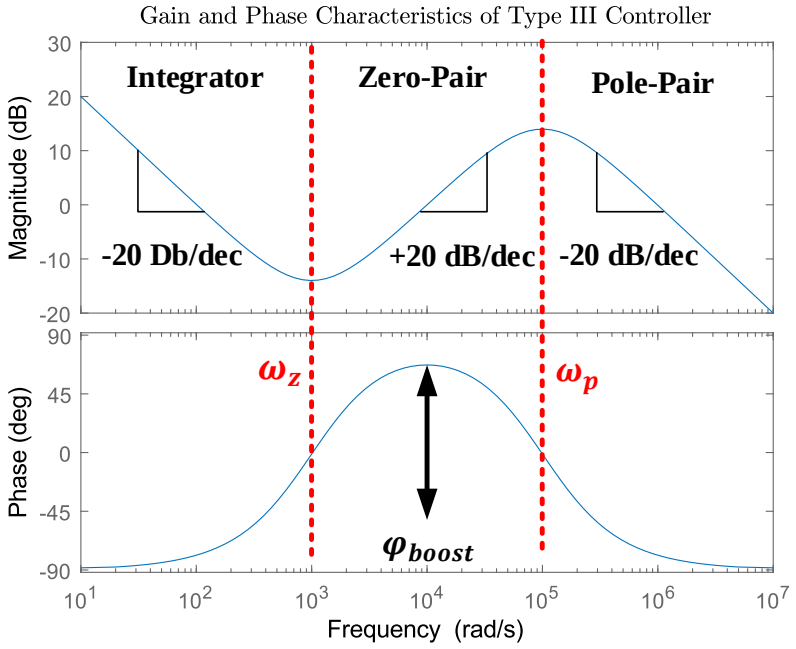


Figure 2.7: Gain and phase characteristics of type III K-factor controller

The desired phase margin is chosen at 60 degrees, which will ensure a highly stable system and which was made achievable as a controller with a double zeros was chosen. The phase margin is defined as the phase of the open loop system evaluated at the cross over frequency plus 180 degrees and is essentially how many degrees the system is above the -180 point. With that in mind an expression for the phase boost needed can be obtained, $\phi_{boost}$

$$P_m = \phi_{sys} + \phi_c + 180 = \phi_{sys} - 90 + \phi_{boost} + 180 \Leftrightarrow \phi_{boost} = P_m - \phi_{sys} - 90 \quad (2.33)$$

where the -90 degrees included, is the phase lag introduced by the integration part of the controller. As there was no phase margin in the uncontrolled plant the obtained value for the needed phase boost was 150 degrees. In order to ensure that the maximum value of the phase boost occur at the cross over frequency, it should be located at the geometric mean of the added zeros and poles [48]

$$\omega_{cr} = \sqrt{\omega_z \cdot \omega_p} \quad (2.34)$$

the locations of the added zeros and poles is then determined as

$$\omega_z = \frac{\omega_{cr}}{k} \quad \text{and} \quad \omega_p = \frac{k}{\omega_{cr}} \quad \text{as} \quad \omega_z \cdot \omega_p = \omega_{cr}^2 \quad (2.35)$$

as k, which is nothing but a measure of seperation, is increased the further the zero and the poles will be apart and the larger a phase boost is obtained. An expression for the constant $k$ can be obtained as [48]

$$\phi_{boost} = \angle \frac{1 + \frac{j\omega_{cr}}{\omega_z}}{1 + \frac{j\omega_{cr}}{\omega_p}} = tan^{-1}\Big(\frac{\omega_{cr}}{\omega_z}\Big) - tan^{-1}\Big(\frac{\omega_{cr}}{\omega_p}\Big) \quad (2.36)$$

substituting the known relations from (2.35) into (2.33) the following is obtained

$$\phi_{boost} = tan^{-1}\Big(k\Big) - tan^{-1}\Big(\frac{1}{k}\Big) \quad (2.37)$$

and by means of the fundamental triogonometric relation [37]

$$tan^{-1}\Big(x\Big) + tan^{-1}\Big(\frac{1}{x}\Big) = 90^\circ \quad (2.38)$$

expression (2.37) can be written as

$$\phi_{boost} = 2 \cdot tan{-}1(k) - 90^\circ \quad (2.39)$$

but as this is derived for a single zero-pole pair and for our case which has a double zero-pole pair the expected phase boost is twice the obtained value

$$\phi_{boost} = 4 \cdot tan{-}1(k) - 180^\circ \quad (2.40)$$

and finally isolating for $k$ results in

$$k = tan\Big(\frac{\phi_{boost}}{4} + 45^\circ\Big) \quad (2.41)$$

as the needed $\phi_{boost}$ was previously determined to 150°, $k$ is $\approx 7.6$, which results in the following zero and pole locations $\omega_z = 1316$ rad/s and $\omega_p = 75958$ rad/s. The controller

gain, which should guarantee the desired cross over frequency, is obtained by observing the magnitude of the open loop gain, $|G_{ol}|$ at the cross over frequency with the designed controller and $k_c$ initially set at 1. The final controller gain value is the multiplicative inverse of the obtained open loop gain

$$k_c = 1/\left|\frac{1}{j\omega_{cr}}\frac{\left(1+\frac{j\omega_{cr}}{\omega_z}\right)^2}{\left(1+\frac{j\omega_{cr}}{\omega_p}\right)^2}\cdot G_{boost}(j\omega_{cr})\right| \tag{2.42}$$

and the value obtained for $k_c$ is 1.81. With all the controller parameters determined the open loop frequency response is computed and shown in Figure 2.8

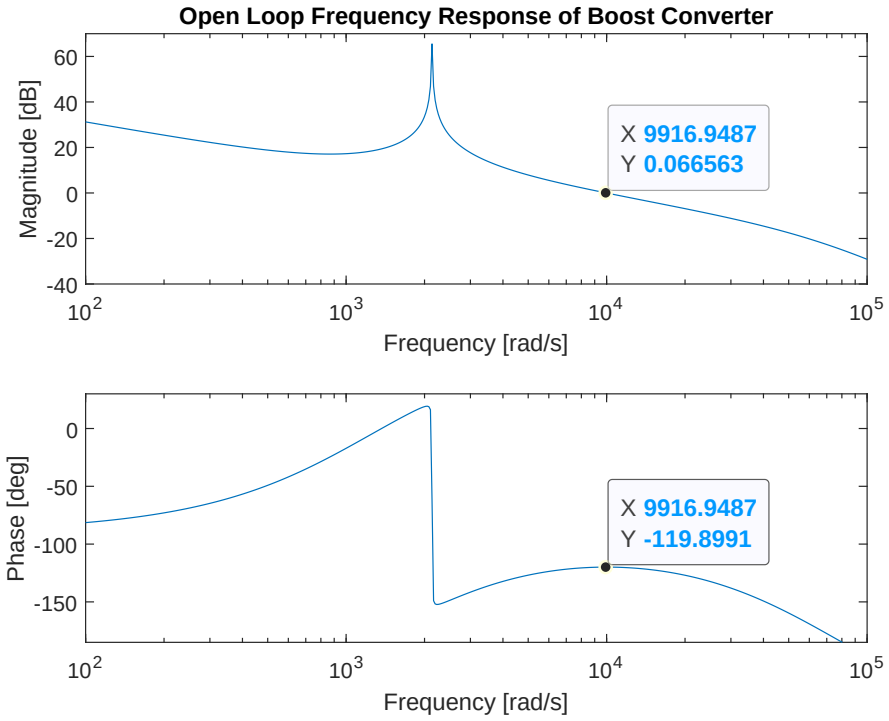


Figure 2.8: Frequency response of the open loop system

As it can be observed in the frequency response, the obtained phase margin is 60° and the obtained bandwidth is 10000 rad/s, which exactly is the previously stated desired characteristics.

### 2.3.3 Pertubation and observation MPPT algorithm

The peturb and observ (P&O) algorithm is used for tracking the maximum power output of the PV array. The main principle is to perturb the voltage and observe how this change influence the power output as shown in Figure 2.9. If an increase in the output power of the PV array occurs when pertubation is done in one direction, then the pertubation is continued in the same direction and if the case is the opposite then the pertubation will be reversed. In other words, this is a continuous process of determining the voltage of the PV array, which will produce the maximum power output [33]

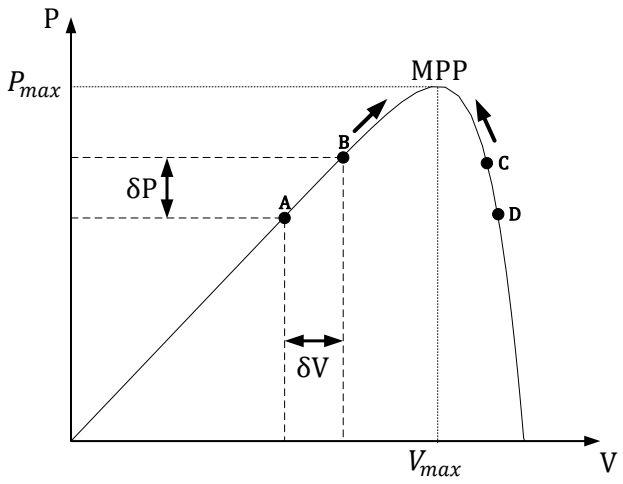


Figure 2.9: Perturbation and Observation MPPT Principle

The operational principle of the P&O algorithm is elaborated through means of the algorithm flowchart, which is shown in Figure 2.10

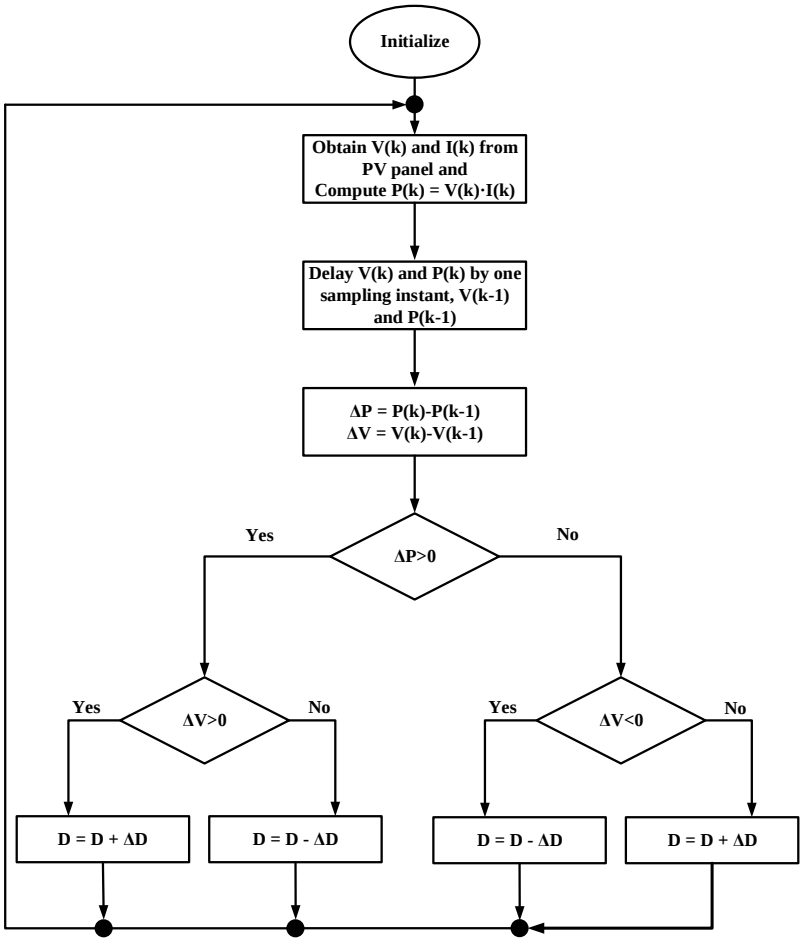


Figure 2.10: The principle of the pertubation and observation algorithm

Finally, the different output characteristics of the designed PV array is presented. The i-v and p-v curves are presented for four different levels of applied solar irradiance and for four different ambient temperatures as shown in Figures 2.11 and 2.12

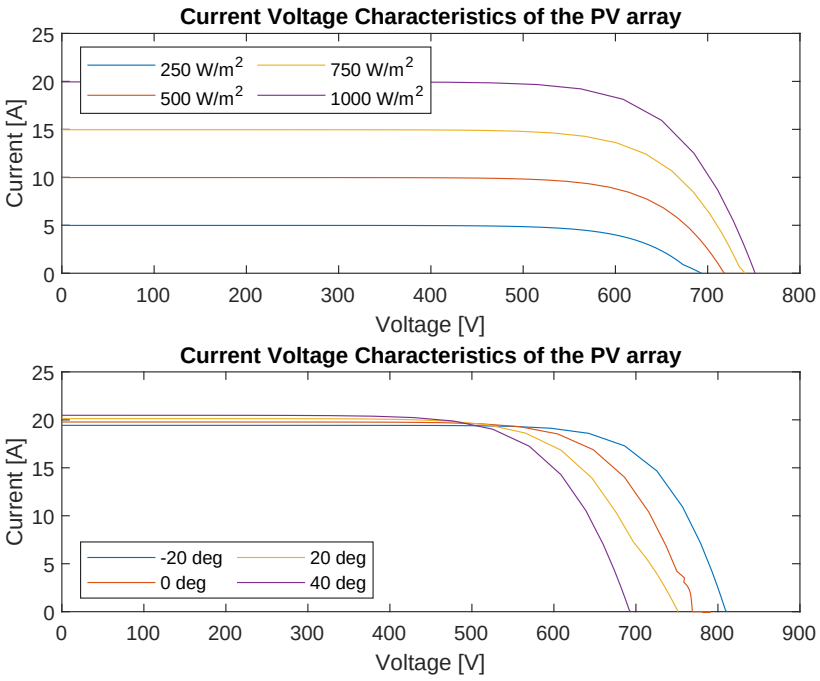


Figure 2.11: Current and Voltage Characteristics of the PV module for different solar irradiance intensity and different temperatures

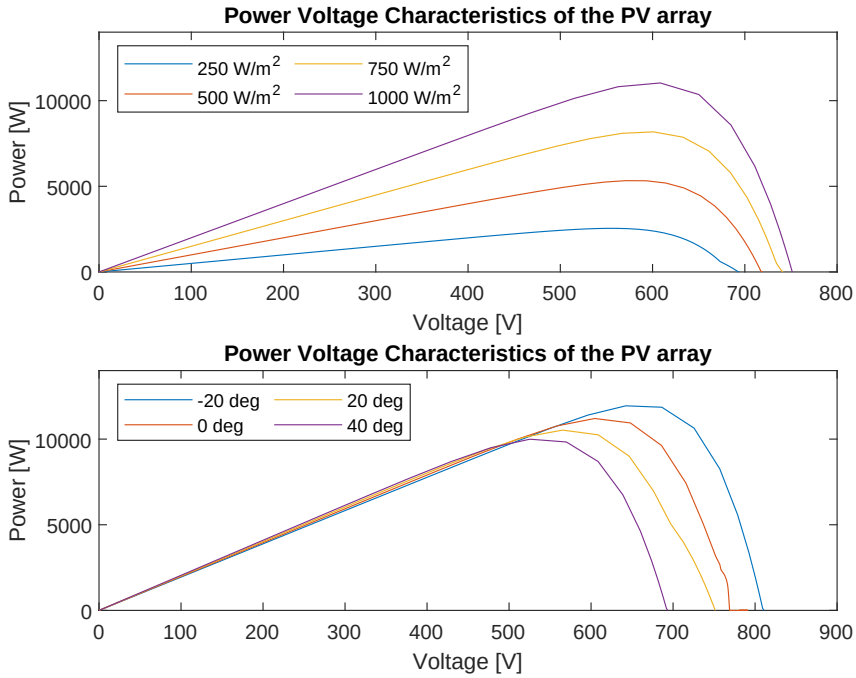


Figure 2.12: Power and Voltage Characteristics of the PV module for different solar irradiance intensity and different temperatures

The modelling and control of the DC/DC stage has not been outlined and the equivalent circuit along with the control scheme is shown in its entirety in Figure 2.13

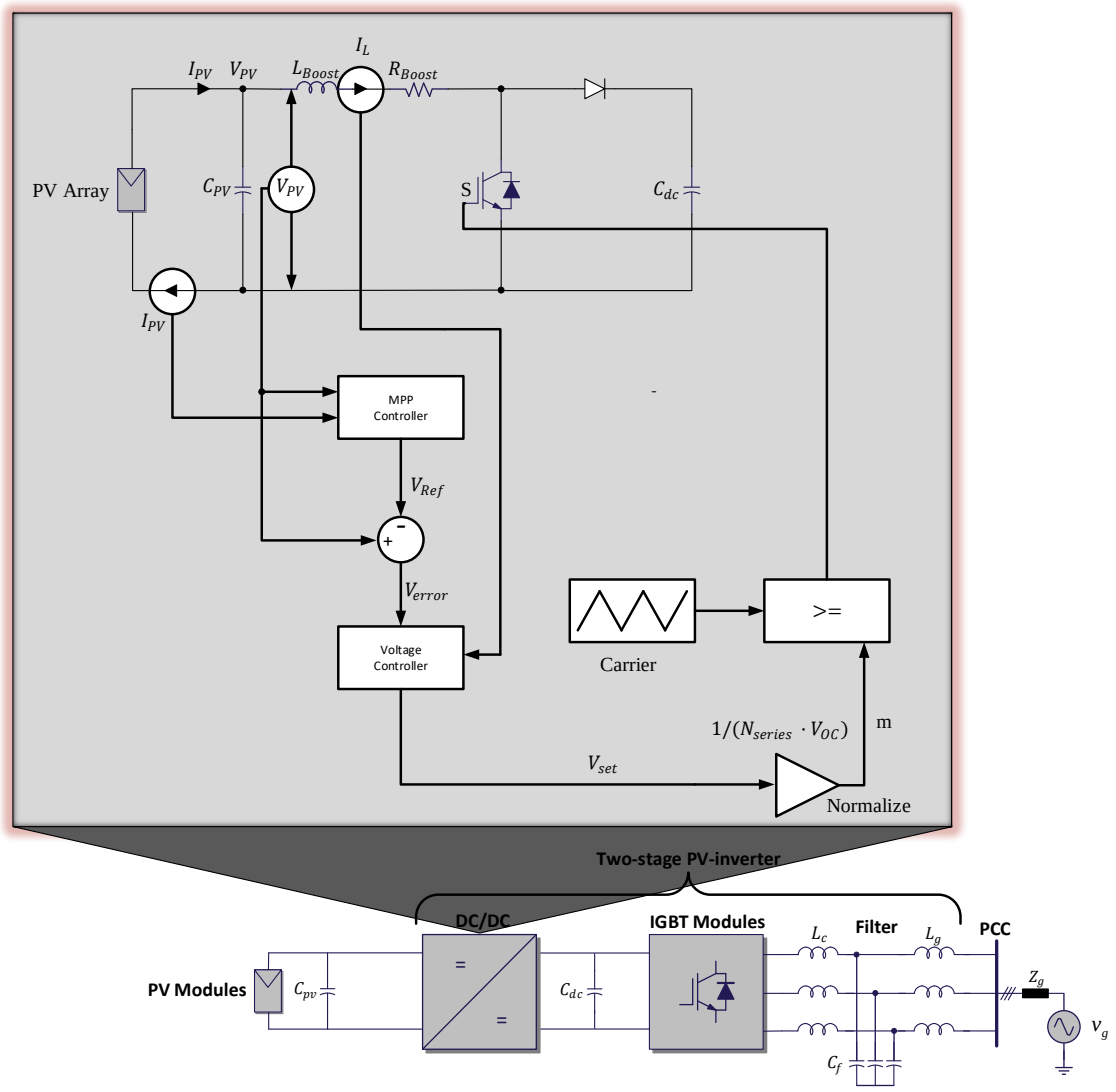


Figure 2.13: Model and Control Scheme Used in the DC/DC Stage

## 2.4 Modelling of DC/AC stage

The power is at this stage transfered to the dc link where DC/AC power conversion is needed in order to feed the power to the grid. In this project, an ordinary 2-level voltage source converter (2L-VSC) is the topology used for realization of the DC/AC power conversion. A cascaded control structure method, based on instantaneous power theory, is adapted, where current is fed into the grid at unity power factor. The 2L-VSC consists of six IGBTs, which each inherent a free-wheeling diode as shown in Figure 2.14.

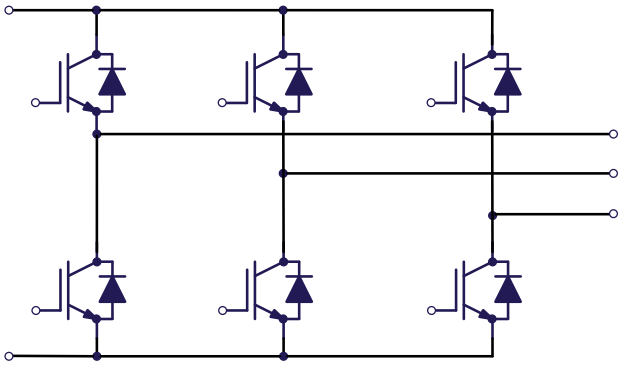

Figure 2.14: Circuit Schematic of the 2-Level Inverter

The inverter is realized by a power module from a leading manufacture [31]. The most relevant preliminary data is summarised in Table 2.4

| IGBT Based Inverter Power Module | |
|---|---|
| Parametrics | FS50R12KT4_B11 |
| Configuration | Sixpack |
| Rated collector-emitter voltage $V_{CE}$ | 1200V |
| Rated continuous collector current $I_{C,nom}$ | 50A |
| Rated repetitive peak collector current $I_{CRM}$ | 100A for $t_p$ = 1ms |
| Rated gate-emitter peak voltage $V_{GE}$ | ±20V |

Table 2.4: Preliminary Data of Sixpack Inverter Power Module [31]

### 2.4.1 Rotating reference frame theory

With the aim of applying linear controllers to sinusiodal quantities, a reference frame transformations is needed. The main concept is to project the three-phase quantities into a space vector, which can be transformed into the rotating reference frame. A conceptual representation of the three-phase projected into a space vector is shown in Figure 2.15

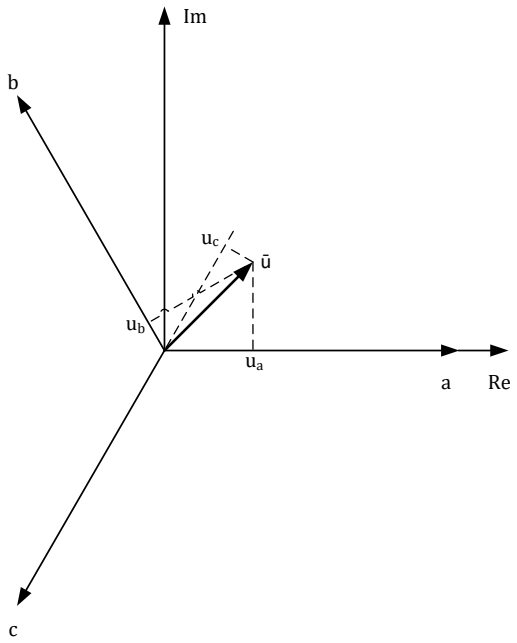


Figure 2.15: Conceptual illustration of the space-vector projection

In order to obtain time-invariant signals, which can be controlled by linear controllers, the reference frame needs to rotate in synch with the fundamental frequency as shown in Figure 2.16

This is realised by transforming the abc components into two components, q and d, which are separated by 90° and which are rotating at angular velocity, $\omega$. The transformation from abc to dq0 can be obtained by applying following state transformation matrix [krause]

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = \frac{3}{2} \begin{bmatrix} cos(\theta) & cos(\theta - \frac{2\pi}{3}) & cos(\theta + \frac{2\pi}{3}) \\ -sin(\theta) & -sin(\theta - \frac{2\pi}{3}) & -sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \tag{2.43}$$

for balanced systems the zero component is non-existing and the transformation simplifies to

$$f_{abc} = (f_d + j f_q) e^{j\theta} \tag{2.44}$$

With the reference frame theory clarified a space vector representing the three phase quantities as shown in Figure 2.15 is defined as

$$f_{abc} = F_m e^{j\theta_{abc}} \tag{2.45}$$

where $F_m$ represents the magnitude of the three phase signals. Transforming the space vector onto the rotating reference frame by means of vector projection the d and q component can be obtained as

$$f_d = Re\Big(\frac{f_{abc}}{e^{j\theta}}\Big) = F_m cos(\theta_{abc} - \theta) \tag{2.46}$$

$$f_q = Re\Big(\frac{f_{abc}}{e^{j\theta+90^\circ}}\Big) = F_m cos(\theta_{abc} - \theta + 90^\circ) \tag{2.47}$$

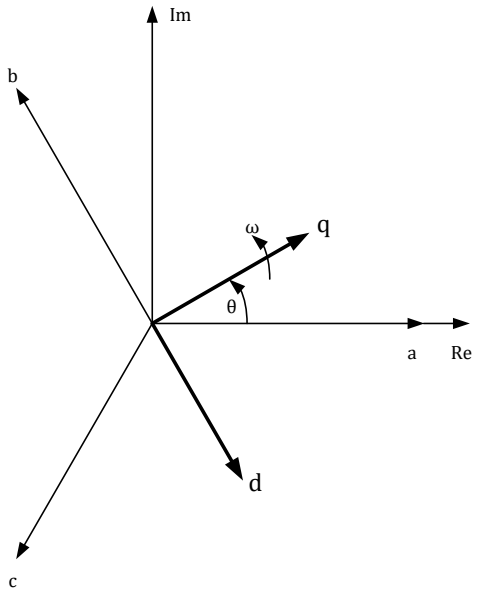


Figure 2.16: Conceptual representation of the rotating reference frame

By observing equations (2.46) and (2.47) it can be observed, that in case of same angular frequencies of the abc quantities and the rotating reference frame, then $f_d$ and $f_q$ will appear as DC values and additionally $f_q$ is zero. This fact will be utilized to align the dq-reference frame with the 3 phase voltages and thereby apply conventional linear controllers to control the currents. Additionally if the grid voltages are aligned with the d-axis, the power can be injected in the grid at unit power factor. In the case of the voltage and current phase difference, the $i_d$ and $i_q$ components are defined as [35]

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} I_m cos(\delta) \\ -I_m sin(\delta) \end{bmatrix} \tag{2.48}$$

where $\delta$ is the power factor angle. The expression for complex power, $s = v \cdot i^*$, can be expressed by means of vector notation in the rotating reference frame as [36]

$$v^s = \frac{2}{3}\Big(v_a + v_b e^{j120^\circ} + v_c e^{j240^\circ}\Big) \tag{2.49}$$

$$i^s = \frac{2}{3}\Big(i_a + i_b e^{j120^\circ} + i_c e^{j240^\circ}\Big) \tag{2.50}$$

Substituting expression (2.49) and expression (2.50) into the expression for complex power [35]

$$s = \Big(\frac{2}{3}\Big)^2\Big[v_a i_a + v_b i_b + v_c i_c + j\frac{1}{\sqrt{3}}(v_{ab} i_a + v_{bc} i_b + v_{ca} i_c)\Big] \tag{2.51}$$

Seperating the active power part and the reactive power part results in

$$P = v_a i_a + v_b i_b + v_c i_c \tag{2.52}$$

$$Q = \frac{1}{\sqrt{3}}(v_{ab}i_a + v_{bc}i_b + v_{ca}i_c) \tag{2.53}$$

Transforming the two expressions for the active and reactive power into the rotating reference frame one obtains

$$P = \frac{3}{2}(v_d i_d + v_q i_q) \tag{2.54}$$

$$Q = \frac{3}{2}(v_q i_d - v_d i_q) \tag{2.55}$$

if the rotating reference frame is rotating at synchronous speed in respect to the 3 phase voltages, the q-component is zero, $v_q = 0$. If a phase difference between the voltage and the current is present, which implies that $i_q \neq 0$, the active power and reactive power in the rotating reference frame simplifies to

$$P = \frac{3}{2}v_d i_d \tag{2.56}$$

$$Q = -\frac{3}{2}v_d i_q \tag{2.57}$$

which illustrates, that the active power can be controlled solely by controlling the d component, $i_d$, and the reactive power can be controlled solely by controlling the q-component, $i_q$. [35] [59]

### 2.4.2 LCL filter design

To ensure power quality, which is consistent with the grid standards, a filter is introduced in the system. A commonly used filter configuration, used for attenuation of the harmonics generated by the converter, is a LCL type filter. As the LCL filter is of third-order it attenuates with $60dB/$decade, at frequencies above the resonance frequency and does therefore have a high ability to cut off the high frequency components. Besides providing a superior attenuation, relatively to a type L filter, the LCL filter can also be designed with small inductance and capacitance values. The single phase representation of the a LCL type filter is shown in Figure 2.17 [38].

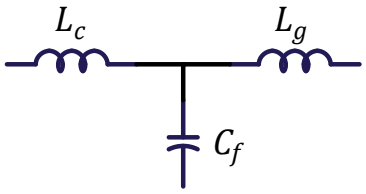


Figure 2.17: Single phase representation of LCL type filter

where $L_c$ denotes the converter side inductor, $L_g$ denotes the grid side inductor and $C_f$ denotes the filter capacitor. Several considerations should be made when designing a filter such as allowed ripple ratio, correct damping of the system to avoid resonance issues and

the consistency with grid standards. In this project the design procedure will be outlined without further considerations, as this is not the major purpose of the project. Initially system base values is used to aid the design of the filter, the obtained base values are presented in Table 2.5.

The filter is designed step wise where first step involves the determination of the converter side inductance, $L_c$, which is determined on the basis of the maximum allowed ripple current on the converter side [11]

| Base Values Used for Filter Design | |
|---|---|
| Base Power, $S_b$ | 12000kVA |
| Base Voltage, $V_b$ | 400V |
| Base Current, $I_b$ $(S_b/V_b)$ | 30A |
| Base Radial Frequency, $\omega_b$ | 314 rad/s |
| Base Impedance, $Z_b$ $(V_b^2/S_b)$ | 13.33 Ω |
| Base Inductance, $L_b$ $(Z_b/\omega_b)$ | 42mH |
| Base Capacitance, $C_b$ $(1/(Z_b \cdot \omega_b))$ | 238$\mu$F |

Table 2.5: Base Values Used for Filter Design

$$\Delta I_{max} = \frac{1}{n} \frac{V_{dc}}{L_c \cdot f_s} \tag{2.58}$$

where $\Delta I_{max}$ is chosen as 10% of the fundamental magnitude, which results in $\Delta I_{max} = 0.1 \cdot I_b = 3$A. n = 12 for a two-level converter modulated by space vector modulation, which is the case in this project. Inserting the values and rearranging the expression results in a value for the converter side inductance of 2 mH. The remaining part of the harmonic attenuation is realized by means of the grid side inductor, $L_g$, and the filter capacitor, $C_f$. The relation between the input current and the output current of the filter can be expressed as [38]

$$\frac{i_g(h_{sw})}{i(h_{sw})} = \frac{z_{LC}^2}{|\omega_{res}^2 - \omega_{sw}^2|} \tag{2.59}$$

where $\omega_{res}$ is the resonance frequency expressed in radians, $\omega_{sw}$ is the switching frequency expressed in radians and $z_{LC}^2 = [C_f \cdot L_g]^{-1}$. The capacitor size is limited by not influencing the power factor, when the converter operates at rated power and in general this amounts to a limitation of less than 5% of the absorbed reactive power at rated conditions. In this project a percentage of 3% is adopted [38]

$$C_f = x \cdot C_b = 0.03 \cdot 238\mu F = 7.16\mu F \tag{2.60}$$

The grid side inductor is designed accordingly to the desired relation between the harmonic attenuation at the converter side and grid side. The grid side inductance can therefore be expressed in terms of the the ratio of the converter side inductance [38]

$$L_g = r \cdot L_c \tag{2.61}$$

The ripple attenuation relation (2.59) can be rewritten, when considering relation (2.60) and (2.61), as

$$\frac{i_g(h_{sw})}{i(h_{sw})} = \frac{1}{|1 + r(1 - a \cdot x)|} \tag{2.62}$$

where $a = L_c C_b \omega_{sw}^2$ and x is the percentage of reactive power absorbed under rated conditions. Adopting a ripple attenuation on the grid side of 20%, in respect to the converter side, amounts to a left-hand side of 0.2. Rearranging the expression, then the inductor factor, $r$, can be determined to have a magnitude of 0.49, which amounts to a grid side inductance 1 $mH$. Before settling on the obtained values for the inductors and capacitors, the resonant frequency, which will be obtained using these values, needs to be verified. In order to avoid any resonant issues, the resonance frequency should be located somewhere in between ten times the line frequency and one-half the switching frequency [38]

$$10 \cdot f_1 < f_{res} < \frac{f_{sw}}{2} \tag{2.63}$$

The resonance frequency can be calculated as

$$f_{res} = \frac{\sqrt{\frac{L_c + L_g}{L_c \cdot L_g \cdot C_f}}}{2\pi} \tag{2.64}$$

which results in a resonance frequency of, $f_{res} = 1764$Hz. The obtained resonance frequency is well above 500Hz and well below 5000Hz, which verifies the chosen filter values. The undamped transfer function describing the relation of the converter output voltage and the grid current can be expressed as

$$\frac{i_g}{v_c} = \frac{1}{C_f \cdot L_c \cdot L_g \cdot s^3 + (L_c + L_g) \cdot s} \tag{2.65}$$

inserting the obtained filter values in (2.65), the frequency characteristics shown in Figure 2.18 is obtained

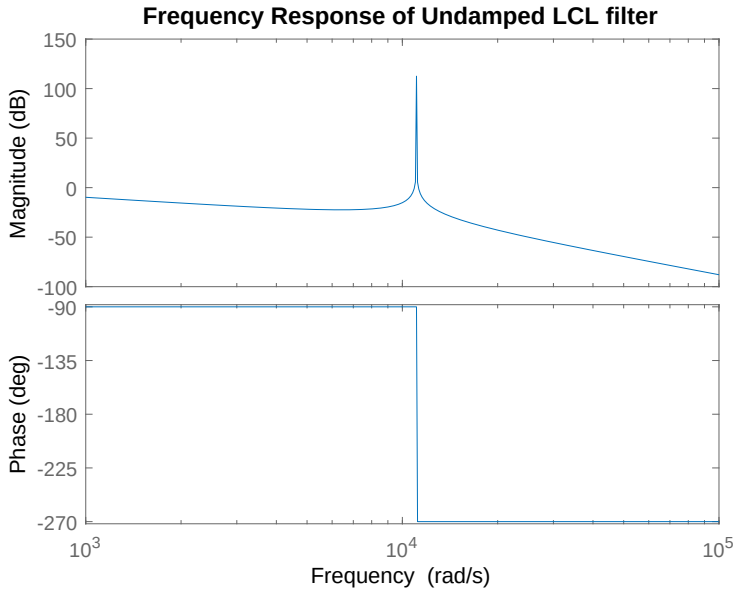


Figure 2.18: Frequency response of undamped LCL filter

it can be observed from the bode plot that a large gain occurs at resonant frequency as a result of the filter impedance being zero at that given frequency. The resonant gain can be decreased to some degree by adding damping resistors in series with the filter capacitors. The choice of damping resistors is a compromise of reducing the resonance gain and not adding to much resistance in the system and thereby lowering the system efficiency. As suggested in [23], the damping resistance should be in the same order of magnitude as the reactance of the filter capacitor when evaluated at the resonance frequency

$$R_{damp} = X_c(\omega_{res}) \tag{2.66}$$

which results in a value of 7.5Ω. Using that high a value will not only induce a significant amount of resistive losses in the system, but also reduce the harmonic attenuation capability of the filter. An initial value of the damping resistance is therefore chosen to be 10% of the capacitor reactance, when evaluated at resonance frequency. The transfer function of the LCL filter with added damping resistance can be expressed as

$$\frac{i_g}{v_c} = \frac{C_f \cdot R_d \cdot s + 1}{L_c \cdot C_f \cdot L_g \cdot s^3 + C_f \cdot R_d \cdot (L_g + L_c) \cdot s^2 + (L_c + L_g) \cdot s} \tag{2.67}$$

and with a damping resistance of 0.75Ω, the frequency characteristics of the filter shown in Figure 2.19 is obtained

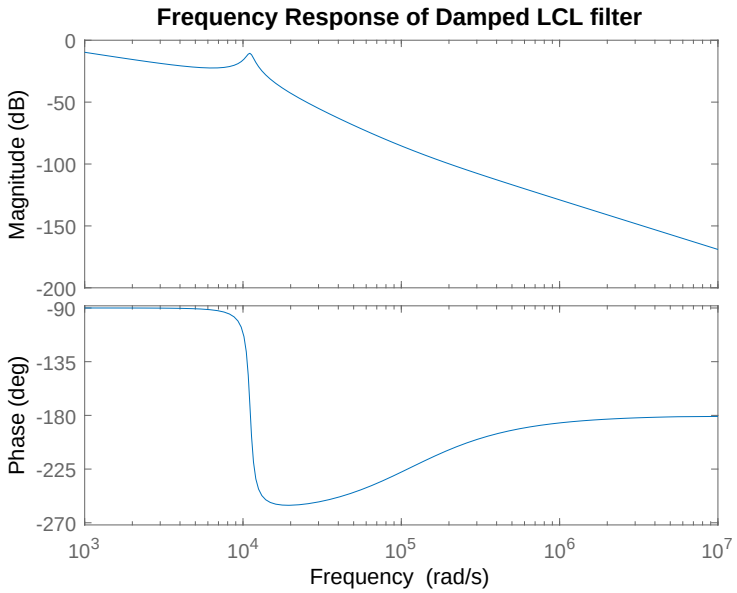


Figure 2.19: Frequency Response of Damped LCL filter

It can be observed from the bode plot that resonant peak is significantly reduced as a result of adding damping to the filter. Unfortunately the harmonic attenuation of the filter is reduced to 43.5 dB/decade compared to the 60 dB/decade of the undamped filter.

### 2.4.3 Synchronous frame voltage orientated control

The control method adopted in this project, to control the three-phase inverter, is known voltage orientated control and is based on a cascaded structure with an inner current

control loop and an outer voltage control loop. The control is realised in the synchronous reference frame, in order to utilize the advantage of using simple linear controllers.

### 2.4.4 Grid synchronization

Phase-locked loop (PLL) is a technique used to synchronize signals. The technique is commonly used to synchronize the converter output current with the power grid voltage. The main functionality of the PLL is use an internal oscillator, which tracks the periodical input signal by means of a feedback loop. The method is superior to the zero crossing methods, as the avoidance of multiple readings in a distorted signal is met, which is often the case in presence of switching harmonics [59]. The overall structure of the PLL is presented in Figure 2.20

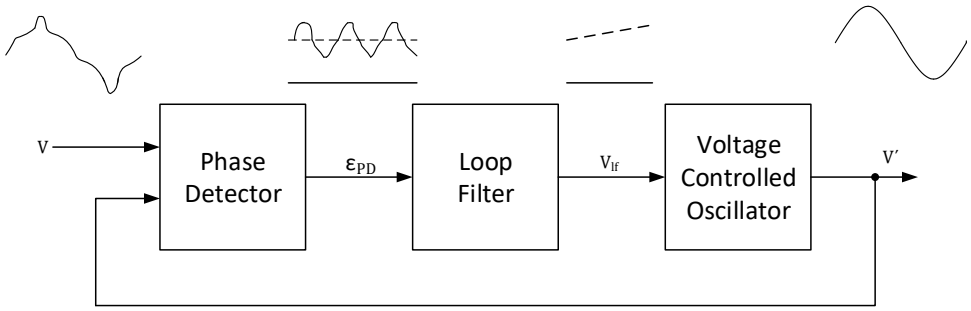


Figure 2.20: General structure of a PLL system

The phase detector generates a signal, which is proportional to the phase difference between the input signal $v$ and the output of the oscillator. The output signal represents the phase difference of the two signals and requires to be zero difference in order to obtain a perfect synchronization. A loop filter, with the same characteristics as a low-pass filter, is used to remove the phase difference and the filter attenuates the high frequency AC components from the phase detector output. The loop filter can be realized by either a first-order low-pass filter or a PI controller. Finally, the phase angle is obtained by integrating the small variation output of the loop filter [59]

For the three-phase system, a PLL system is implemented in the dq-reference frame, where the three-phase voltages are represented by a vector containing each voltage component. For a thee-phase balanced system the rotation of the voltage vector is kept at a fixed speed. The angular position of the reference frame, is then controlled by a PI controller in a feedback loop, which will regulate the q-component to zero. A synchronous reference frame PLL is shown in Figure 2.21.

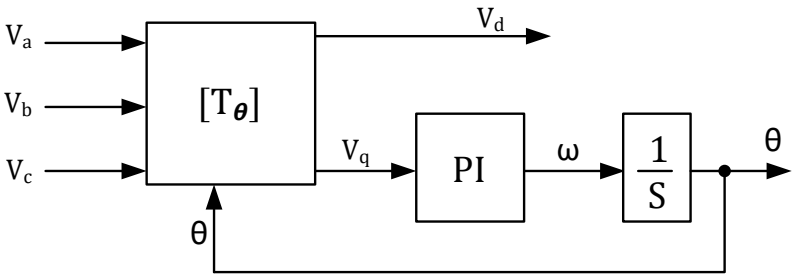


Figure 2.21: Block diagram of a synchronous reference frame phase locked loop

When the q-axis component,$V_q$, is fixed to zero, the rotating reference frame will be aligned and synchronized with the abc reference frame, which enables the extraction of the phase angle. Since grid synchronization is not the scope of the project, it will not be further elaborated. A complete step by step derivation of the PLL transfer function and tuning of the PLL PI can be found in [59].For compensation of not going into detail with the subject, simulations of the three-phase sinusiodal voltages, the tracking of the q and d voltage components and the output phase angle of the PLL is presented in Figure 2.22

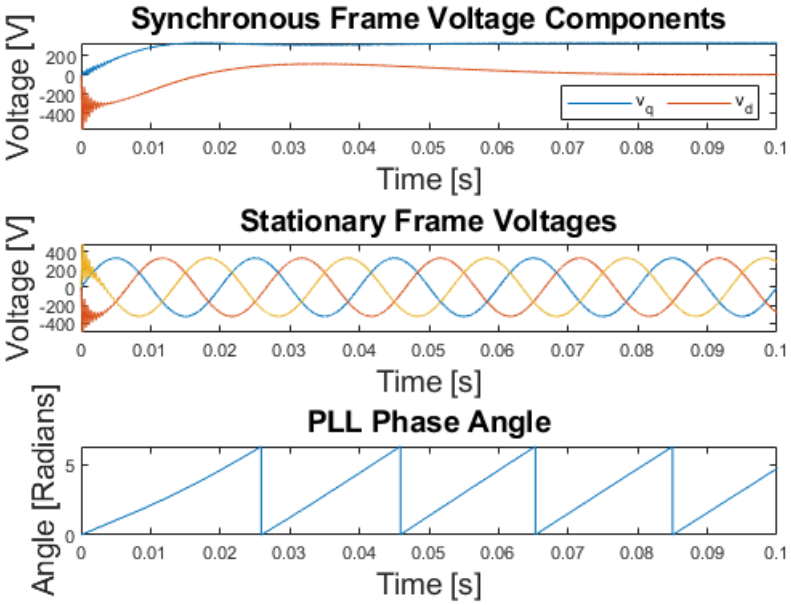


Figure 2.22: Response of voltage components and the phase angle output of the PLL

it can be observed in the Figure that the phase output of the PLL follow the three-phase voltages and resets for every fundamental cycle.

### 2.4.5 Grid Current Control

The current references are generated on the basis of how much active and reactive power is desired to inject in the power grid and the references are therefore calculated by means of the instantaneous power equations derived in Section 2.4.1. The errors of both the

active and reactive power are fed to each of their respective PI controller, which generates the current references. The $i_d$ reference is also a function of the DC voltage controller in the outer loop. The calculation of the reference currents are shown in block diagram form in Figure 2.23 [59]. In this project only the active power reference is manipulated in order to stress the power electronic components accordingly to each defined operational condition, whereas during real-life conditions both active and reactive power is needed to be controlled to maintain the correct grid voltage amplitude at the point of common connection.

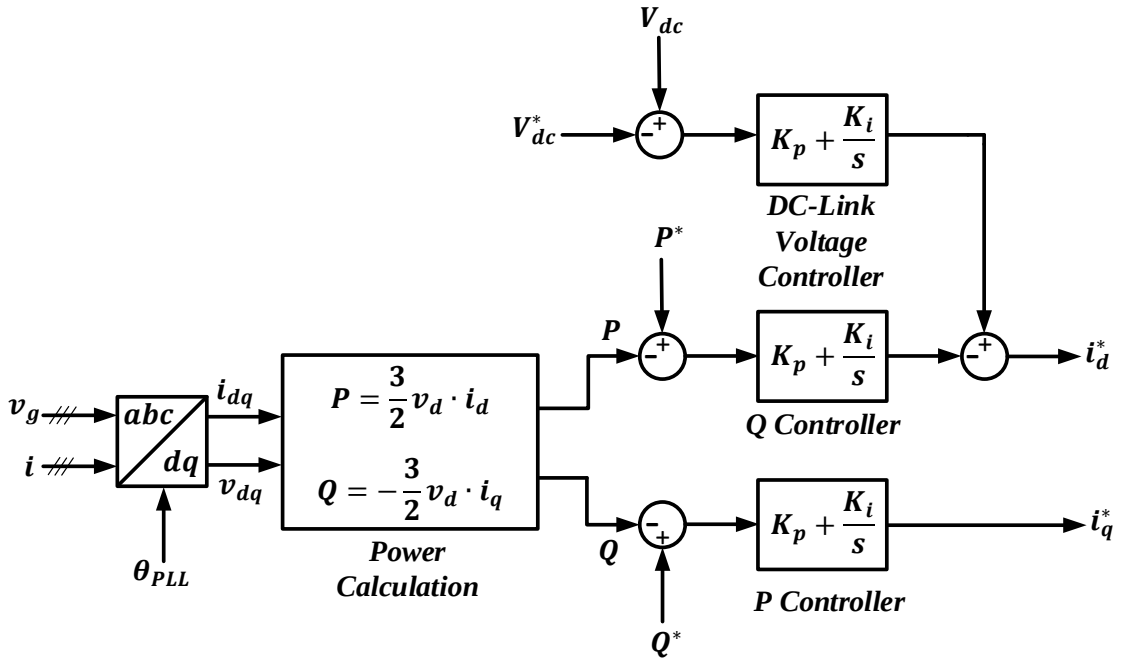


Figure 2.23: Block Diagram Representation of Reference Currents Calculations

It should be noted that the filter capacitor is not taken into account when designing the current controllers, which is due to the dominance of the inductors at low frequency. The dominance of the inductor, at low frequency, is verified in the frequency response, where both filter configurations is compared, shown in Figure 2.24 [40]

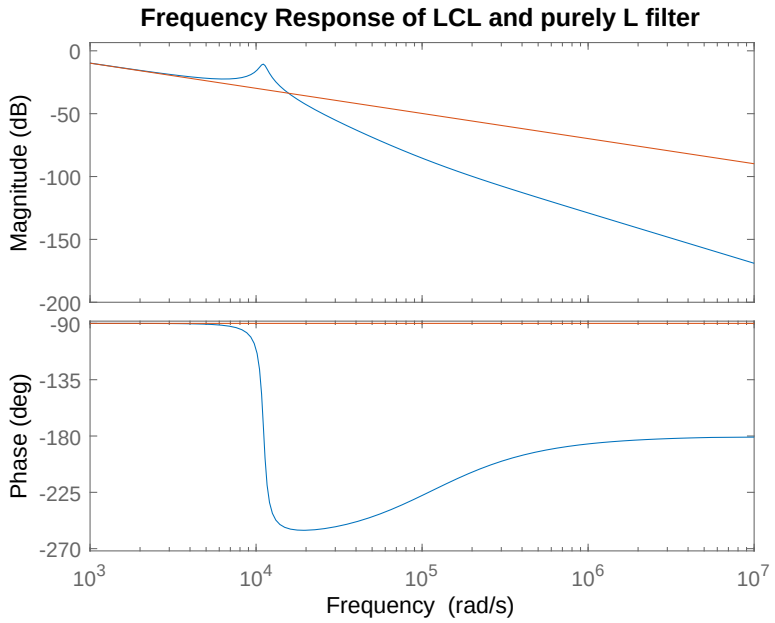


Figure 2.24: Frequency response of the LCL filter and a L filter

as seen in Figure 2.24, the approximation of the filter being purely inductive at low frequencies is valid. The filter is then represented as the total inductance of the converter side inductance and the grid side inductance, when designing the current controllers. The voltage equation for the AC-side can then be expressed as grid voltage

$$v_i(t) = L_t \frac{di(t)}{dt} + i(t) \cdot r_t + v_g(t) \tag{2.68}$$

where $L_t$ is the total inductance, $r_t$ is the total inductor resistances, $v_i$ is the converter output voltage and $v_g$ is the grid voltage. Applying the park transformation to equation (2.68), the rotating reference frame quantities are obtained as

$$v_d = L_t \frac{di_d}{dt} + i_d \cdot r_t + v_{gd} - \omega L_t i_q \tag{2.69}$$

$$v_q = L_t \frac{di_q}{dt} + i_q \cdot r_t + v_{gq} + \omega L_t i_d \tag{2.70}$$

it can observed from the two equations (2.69) and (2.70) that each q and d voltage equation depends on each others current component and to obtain an optimal dynamical performance, the two components is required to be controlled independently of each other [3] [47]. The decoupling of the d and q components is done through mathematical manipulations as shown in block diagram representation in Figure 2.25 [59]

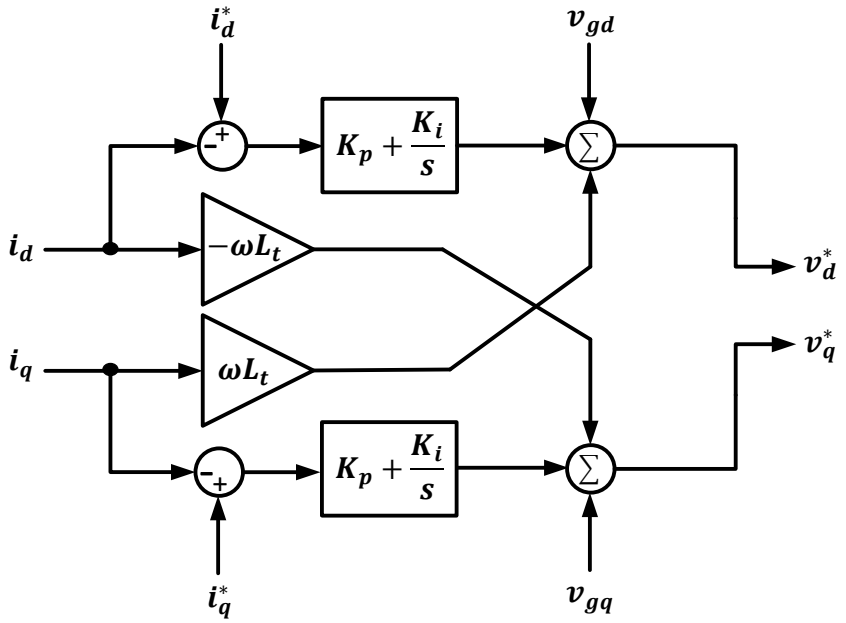


Figure 2.25: Block diagram representation of current decoupling

The controllers are tuned by means of analysing the current control loop, which consists of the PI controller, a delay approximation and the L filter as shown in Figure 2.26

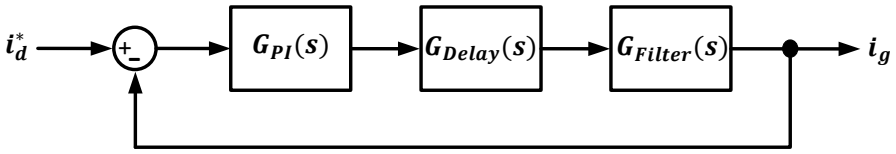


Figure 2.26: Block diagram representation of the current control loop

where the PI controller is expressed as

$$G_{PI}(s) = \frac{K_p s + K_i}{s} = K_p \cdot \frac{T_i s + 1}{T_i s} \tag{2.71}$$

where $T_i = K_p/K_i$. The filter transfer function can be expressed as

$$G_{Filter}(s) = \frac{1}{L_t s + r_t} \tag{2.72}$$

The delay transfer function is taking into account a combination of the computational delay and sampling delay, which in total amounts to three-halfs of one sampling period

$$G_{Delay}(s) = \frac{1}{1.5 T_s s + 1} \tag{2.73}$$

the open loop is the product of those three transfer functions and can be expressed as [59]

$$G_{ol} = \frac{K_p(T_i s + 1)}{T_i s(1.5 T_s s + 1)(L_t s + r_t)} \tag{2.74}$$

The controller is designed accordingly to ensure defined stability margins and bandwidth of the open loop system and damping and overshoot of the closed loop system. The phase margin should be at least 45° and a gain margin of 10dB to ensure a stable response. Overshoot should be limited to the a very small degree, as current overshoots are critical in respect to causing permanent damage components of the system. To ensure a high bandwidth of the current loop, the $T_i$ is chosen to cancel out the dominant pole of the system, which is the one introduced by the filter

$$T_i = \frac{L_t}{r_t} \tag{2.75}$$

additionally $K_p$ is chosen to obtain a damping ratio of $1/\sqrt{2}$, which ensures a good compromise between speed and stability of the system and as suggested in [39], the proportional gain can calculated to obtain that specific damping ratio as

$$K_p = \frac{L_t}{3 \cdot T_s} \tag{2.76}$$

The obtained values are, $T_i = 0.01$ and $K_p = 10$ and the obtained phase margin, gain margin and system response is shown in Figure 2.27.

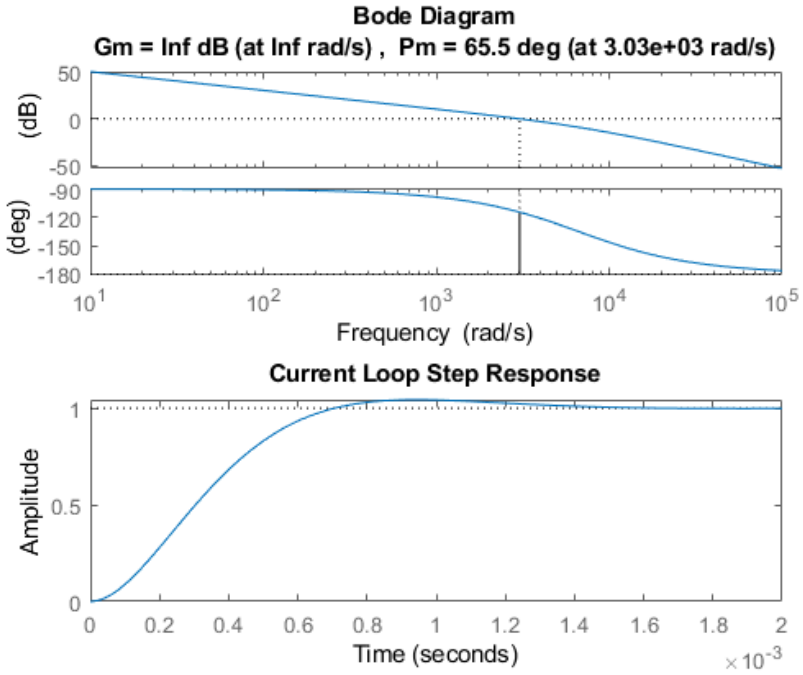


Figure 2.27: Gain and Phase Margin of the Open Loop and Step Response of the Closed Loop

It can be observed that an infinite gain margin and a phase margin of 65.5° was obtained in the open loop. Applying a step function to closed loop system it can observed that a fast inner loop response is obtained, with a settling time of 1.3ms and while not having any considerable overshoot. The current loop inhibits a satisfactory behaviour, as the desired system characteristics is obtained.

### 2.4.6 DC-Link voltage control

Whereas the inner loop was designed to obtain a high bandwidth by cancelling the dominant pole the main goal of the outer loop is to obtain stable response and at least a bandwidth of one decade lower with respect to the inner loop. With a bandwidth of one decade lower the two loops can be considered to be decoupled as the currents will have reached their reference values when designing the voltage controller [59]. A simplified first order approximation is used to approximate the inner loop, when designing the voltage loop

$$G_{inner}(s) = \frac{1}{3T_s s + 1} \tag{2.77}$$

The transfer function describing the DC-link voltage relation with the $i_d$ current can be expressed as

$$\frac{v_{dc}}{i_d} = \frac{\sqrt{3}}{2} \frac{R_o}{(1 - R_o C s)} \tag{2.78}$$

Where $R_o$ is the steady-state resistance at the input side of the DC-link, the $\sqrt{3}$ factor is the amount which the DC link is required to be higher than the peak AC voltage. The value of the equivalent capacitance of the DC-link capacitor branch is $410\mu$F. Adding a PI as described in (2.71) and utilizing that $R_o C >> 3T_s$ the open loop transfer function can be described as [59]

$$G_{vdc}(s) = \frac{\sqrt{3} k_p (T_i s + 1)}{2T_i s (3T_s s + 1)(Cs)} \tag{2.79}$$

The method applied at the DC/DC stage of choosing the crossover frequency at the geometric mean of the poles is also adapted here. The crossover frequency is expressed as

$$\omega_c = \frac{1}{3aT_s} \tag{2.80}$$

where a is a function of the desired phase margin

$$a = \frac{1 + cos(\phi)}{sin(\phi)} \tag{2.81}$$

the time constant of the controller is related to the a parameter as

$$a = \sqrt{\frac{T_i}{3T_s}} \tag{2.82}$$

As the bandwidth is required to be one-tenth of the inner loop it leads to $a = 11$, which results in $T_i = 0.0036$. The proportional gain of the PI can be calculated as [59]

$$K_p = \frac{C}{2\sqrt{3} a T_s} \tag{2.83}$$

inserting the obtained values leads to $K_p = 0.108$ and the outer loop characteristics shown in Figure 2.28 was obtained

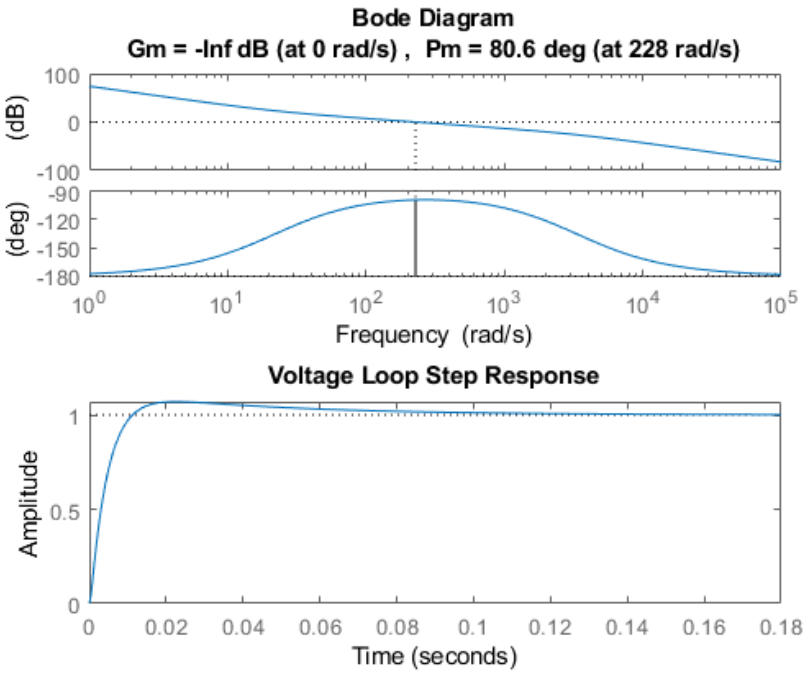


Figure 2.28: Gain and phase margin of the open loop and step response of the closed loop

as observed in the frequency response, the obtained bandwidth is below 300 rad/s and the two loops can therefore be considered decoupled. It can also be observed that the crossover frequency is at the geometric mean and a phase margin of 80.6° is obtained along with a system response overshoot of 7%.

***Now that the entire system is modelled and is controllable, the stress applied on each power electronic component can be manipulated accordingly to the applied mission profile, which is an important tool to carry in respect to perform the wear-out analysis in the following chapters. To finalize the chapter a complete overview of the DC/AC stage control structure is shown in Figure*** 2.29

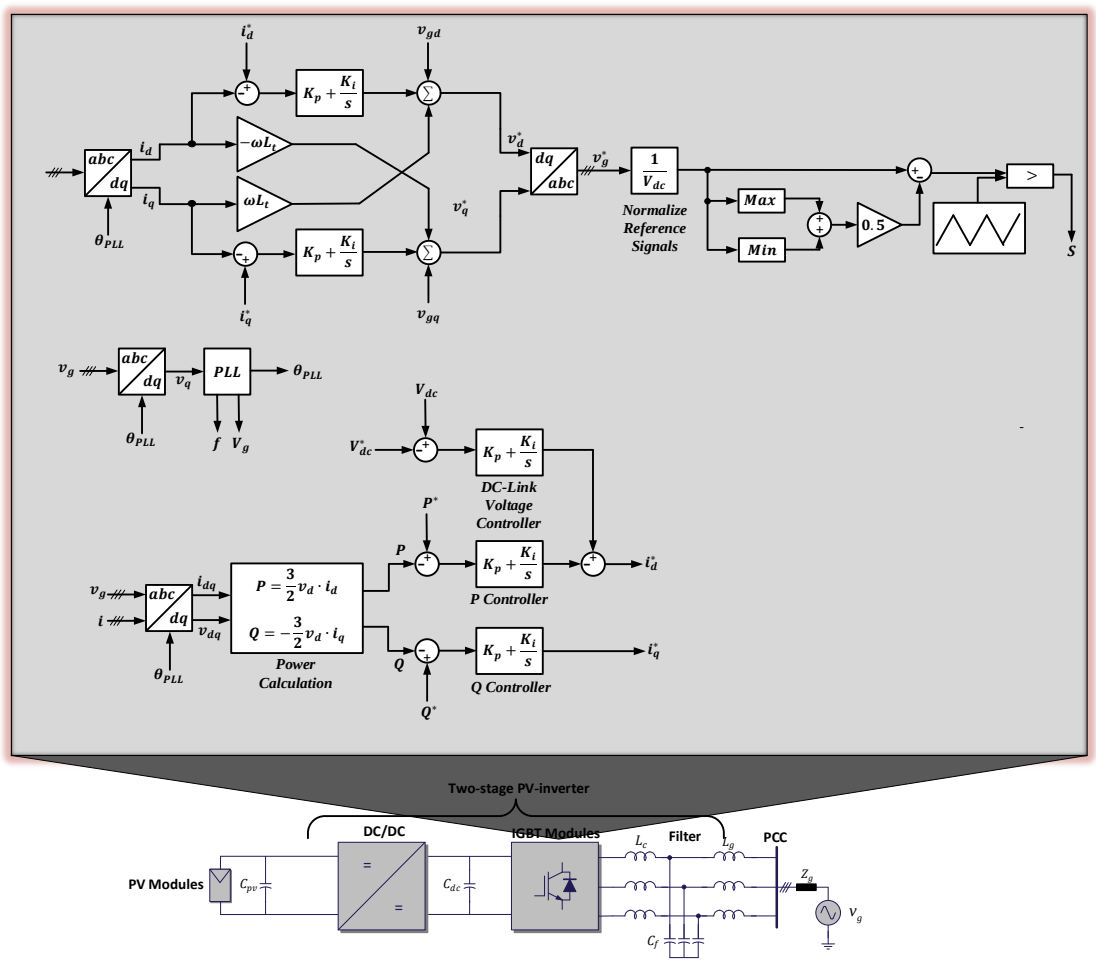


Figure 2.29: Control scheme of the DC/AC stage

# Lifetime Estimation of Active Components 3

***In this chapter the wear-out analysis of the active components will be carried out. The analysis requires several steps to in order to obtain the lifetime estimation of the power devices. First step is to obtain the thermal loading by means of a mission profile translation. When the thermal loading is obtained, it it required to be applied to a counting method, which decomposes the irregular profile into several cycles, which applicable with the used lifetime model. The damage accumulated from the annual profile is then obtained and the lifetime can be estimated. Finally, the uncertainties linked to power electronic components are taken into account and a lifetime distribution is obtained by means of a Monte Carlo analysis***

## 3.1 Inverter IGBT power module

The mission profile containing solar irradiance and ambient temperature is required to be translated into a thermal loading profile, which can be used to evaluate the lifetime of the power devices. The translation consists of two major modelling parts; the loss modelling and the thermal modelling.

### 3.1.1 Mission profile translation

When the loading stress is applied the power devices, power loss will be dissipated. The total power loss is the sum of the switching losses and the conduction losses as shown in Figure 3.1. The switching and the conduction losses, can be obtained by means of a long line of analytical expression. Instead it is chosen to utilize the built-in loss GUI in the used simulation tool, for the sake of simplicity.

Instead of determining the semiconductor switching losses from current and voltage transients, the simulation tool measure the operation condition before and after each switching event. The measured parameters are the forward current, blocking voltage and junction temperature. Using these parameters it calculates the dissipated by means of multi-dimensional look-up tables, which are constructed on the basis of extracted datasheet values from the manufacturer. The look-up table used to obtain the turn-on energies is shown in Figure 3.2

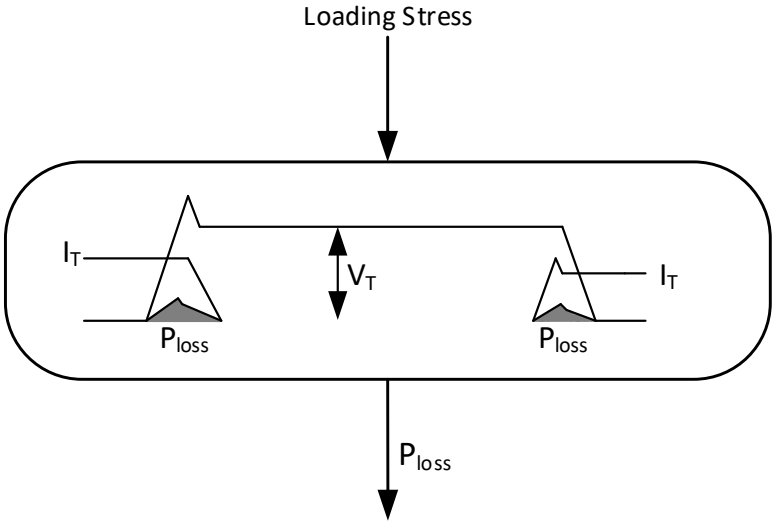


Figure 3.1: Power losses of power devices

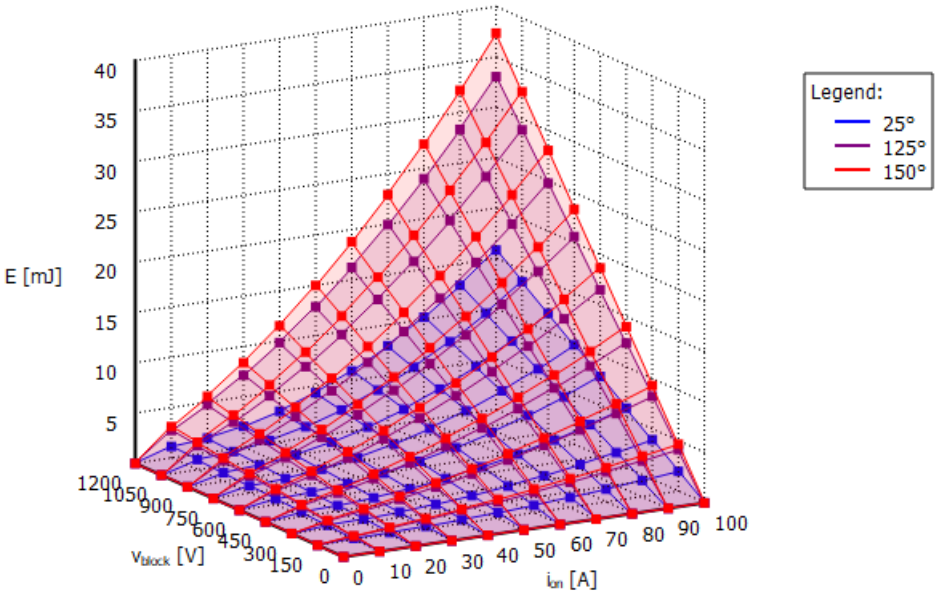


Figure 3.2: Look-up table used to obtain the turn-on energies of the IGBTs

The same modelling procedure is carried out for diodes contained in the system with the exception of a few changes, which is elaborated in the lifetime estimation of the inherent diodes section 4.2. During the on-state condition, the dissipated power is computed with the use of the forward current and junction temperature, which is illustrated by the look-up table shown in 3.3. The look-up tables are constructed from datasheet information of the IGBT power module shown in Table 2.4 [31]

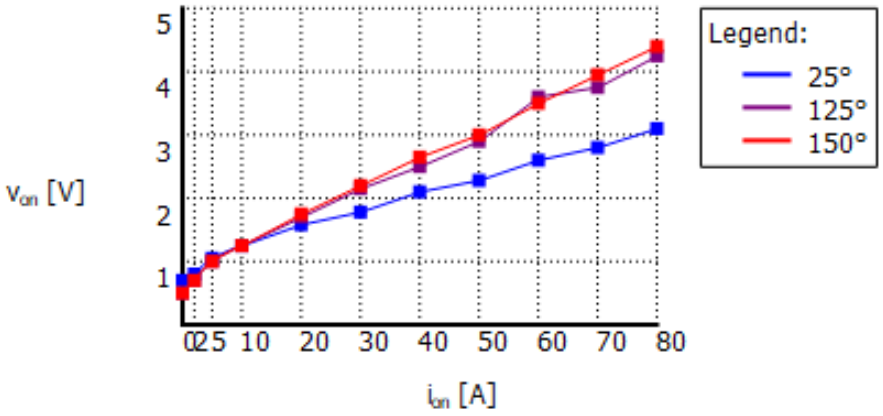


Figure 3.3: Look-up table used to obtain the conduction losses of the IGBTs

As shown in Figure 3.4, the losses will generate heat, which is commonly known to have a lifetime degrading effect on electronic components and therefore it is desired to conduct as much heat as possible from the power devices and through each layer of the module to the heat sink.

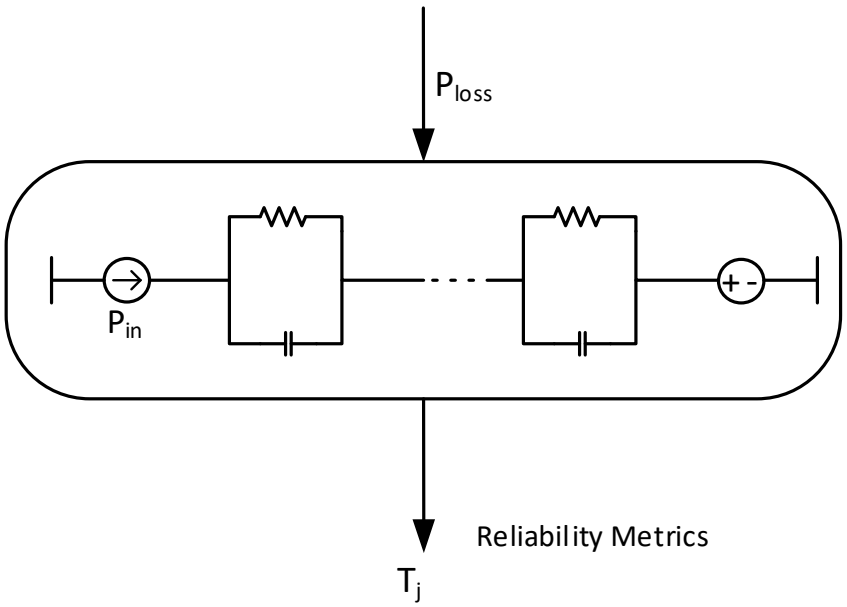


Figure 3.4: Loss leads to termperature rise of the power devices

The complete thermal model consists of a thermal model describing the internal thermal characteristics of the power module and a thermal model describing the external cooling network as shown in Figure 3.5 where $Z_{th(j-c)}$ is thermal impedance from junction to case, $Z_{th(c-h)}$ is the thermal impedance from case to heatsink and $Z_{th(h-a)}$ is thermal impedance from heatsink to ambient. The junction temperature of the IGBT can then be obtained

as

$$T_j = P_{loss(IGBT)} \cdot Z_{th(j-c),IGBT} + (P_{loss(IGBT)} + P_{loss(diode)}) \cdot Z_{th(c-a)} + T_a \tag{3.1}$$

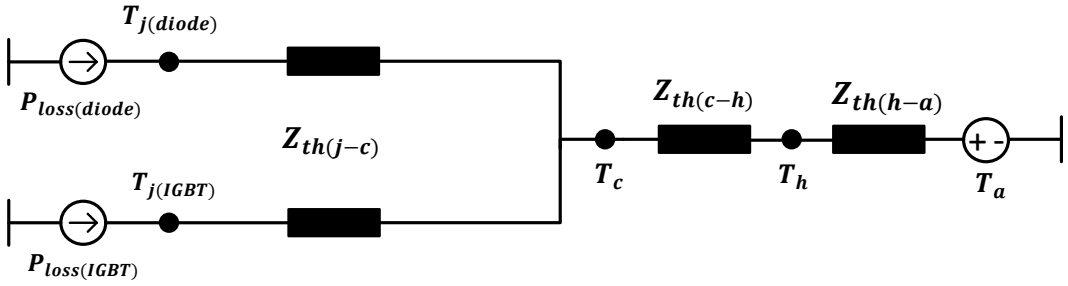


Figure 3.5: Complete thermal model of the power module and the external cooling components

The internal and external parts are modelled by different types of networks, the different layers of the module connecting the power chips to the case is modeled by means of a non-physical model, known as the Foster network. Each layer are represented by a thermal resistance connected in parallel with a thermal capacitance, which describes the transient temperature characteristics. The foster network is shown in Figure 3.6 [45] [8]

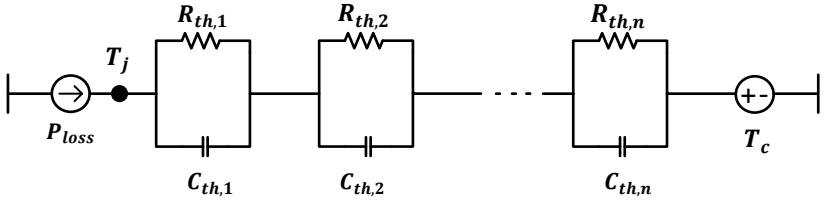


Figure 3.6: Foster network, which is used to model the temperature difference from junction to case

The calculation of the total is analogous to those of a first-order electrical circuit and is expressed as

$$Z_{th(j-c)}(t) = \sum_{i}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}}\right) \tag{3.2}$$

As stated earlier, the network has no physical relation and the foster network parameters are obtain by heating up the module and during cool-down the parameters are fitted from the cooling curve, obtaining the thermal resistance and the time constants, from which the thermal capacitance can be calculated as

$$C_i = \frac{\tau_i}{R_i} \tag{3.3}$$

The thermal impedance representing the four layers for junction to case for the power module in question is provided by the manufacture datasheet [31] and are shown in Figure 3.9

| | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| R | 0.0324 K/W | 0.1782 K/W | 0.1728 K/W | 0.1566 K/W |
| τ | 0.01 s | 0.02 s | 0.05 s | 0.1 s |

Figure 3.7: Thermal impedance from junction to case

The cooling components are modeled by means of the Cauer model, which parameters are based on actual physical properties such as geometric and material composition of each layer. The parameters for each layer are often obtained by means of finite element simulations and the parameters obtained for each layer is used in each of the RC lumps as shown in Figure 3.8 [45]

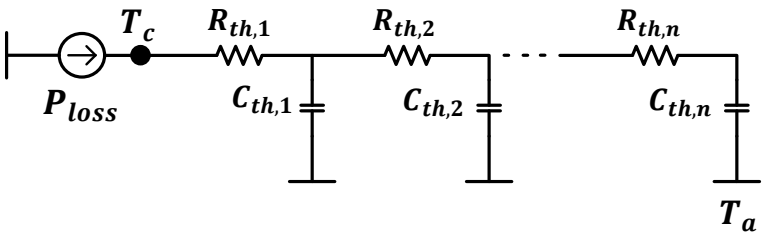


Figure 3.8: Cauer network used to model the external cooling components

The thermal resistance from case to heatsink represents the thermal grease and thermal paste located between the case and the heatsink. The thermal resistance value is provided by the manufacture datasheet [31] as $R_{th(c-h)} = 0.2$ K/W. The thermal impedance of the heatsink is selected on the basis of how much heat is needed to be dissipated from the power module and which type of cooling system is applied in terms of natural convection or external applied cooling. The thermal capacitance of the heat sink is many times larger than the one of the power module and is often in the order of several minutes. Aluminium base sinks cooled by natural convection have thermal time constants in the range of 4-15 minutes, while the ones with forced air-cooling is less than a minute, which is the relevant case here and the thermal time constant is chosen to be $\tau_h = 40$s [52].

The thermal resistance providing the steady-state temperature of the heat sink chosen on the based assumption

- **The heatsink-to-ambient temperature difference is limited to** $\Delta T_{(h-a)} \leq 30°$

Additionally it should be considered that the power electronic components are located inside an enclosure in order to protect it from hostile environmental conditions and inside this enclosure the environment is of different nature as a result of heat dissipated by the power electronic components. As i have not performed any FEM analysis on how much the temperature difference is between inside the closure and the global ambient temperature, inspiration is gathered from [65], where a temperature difference of about 35° from local to global ambient temperature in the case of a PV micro-inverter. As this case differs from the one in cited paper, both in terms of ratings and other factors such as diffent enclosure etc. could differ, a conservative temperature difference of 20° is chosen between the local

and global ambient temperature. Combining the heatsink temperature difference and the inclusion of local ambient temperature, an assumption of a case to ambient temperature difference of 50° at rated power loss

$$R_{th(h-a)} = \frac{\Delta T_{ca}}{P_{rated}} - R_{th(c-h)} = \frac{50°c}{P_{rated}} - 0.2K/W \tag{3.4}$$

The system was simulated at rated power and the average losses of the switching and conduction losses of both the diode and the IGBT as it can be observed in Figure 3.5 both components power loss contributes to the temperature difference from case to ambient. It is assumed that the entire power loss is distributed to the cooling network, when in reality some of it will be absorbed by the junction-to-case impedance of both the diode and the IGBT.

A total power loss of 18 watts was obtained from both components at rated power condition, which leads to a thermal resistance from case to ambient of 2.7 K/W when considering equation (3.4). As the case to heat sink accounted for 0.2K/W it results in a thermal resistance for the heatsink to ambient of 2.5K/W. With the use of the obtained thermal resistance and the time constant of 40 seconds, the thermal capacitance of heatsink can be obtained by use of equation (3.3) as $C_h = 16$J/K

Unfortunately it is not possible to combine the curve fitted parameters with an external Cauer network for modelling of the case to ambient, without altering the thermal tendency of the junction to case temperature cooling curve as shown in Figure 3.9

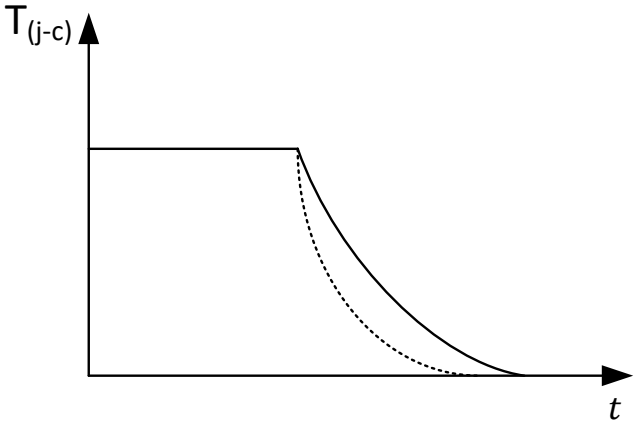


Figure 3.9: Alternating the thermal tendency of the junction to case by combining an external Cauer network with the fitted parameters

A solution is to divide the thermal network into two, one which will provide the right amount of power to the cooling network by means of a low pass filter which parameters are based on Foster to Cauer transformation [42]. The adaptation of this solution will provide the right case temperature to the foster network, which then will provide the correct junction temperature

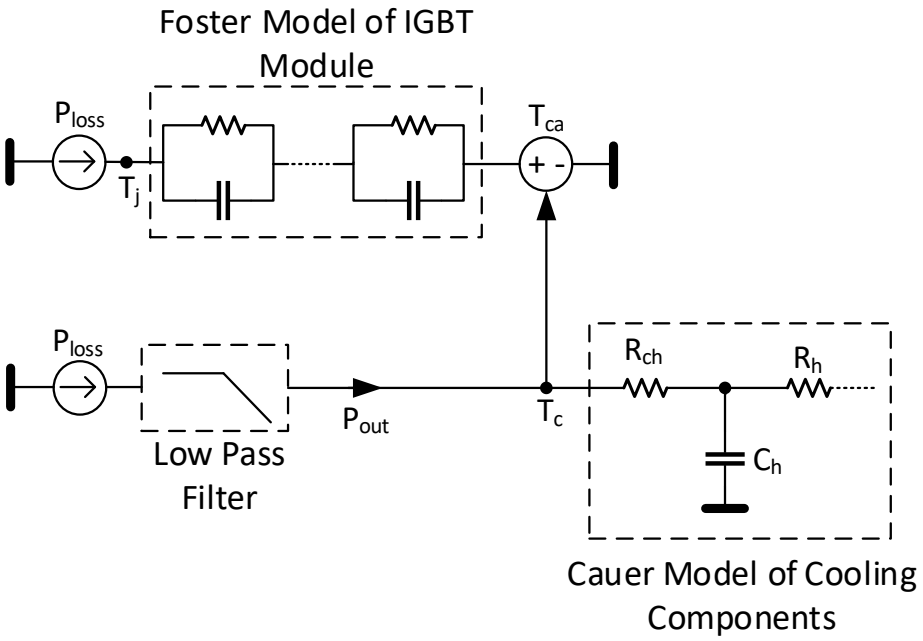


Figure 3.10: Two circuit thermal network to combine the foster network with an external cauer network

The calculation of the Foster to Cauer transformation based low pass filter is rather tedious and can be found in [42], while only the obtained values will be presented here. Transforming the Foster parameters of the IGBT as shown in Figure 3.9, the following low-pass filter is obtained

$$G_{th,filter} = \frac{1}{(C_1 s + R_1)(C_2 s + R_2)} = \frac{1}{(0.007329s + 0.08914)(0.02626s + 0.2191)} \tag{3.5}$$

With the electro-thermal model in place the thermal loading caused by applied mission profile can be obtained, which is realised by obtaining the thermal junction temperature for a set of defined operational conditions by means of simulation. The stress on the inverter components according to the defined operating conditions, is realised by manipulating the $i_d$ reference as shown in Figure 3.11

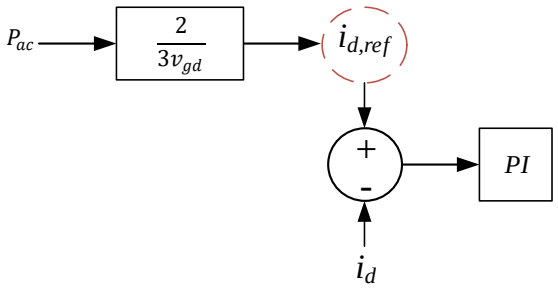


Figure 3.11: Manipulation of the Loading Stress

and in Figure 3.12, the obtained junction temperature response is shown at rated conditions

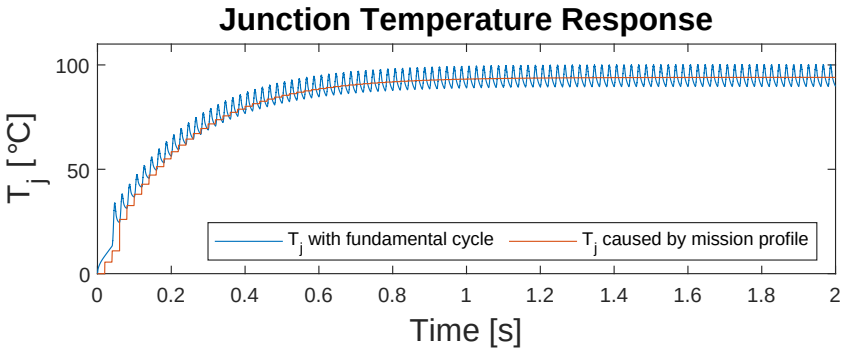


Figure 3.12: Junction temperature response at rated conditions

As stated in Section 1.4, there are power cyclings at different timescales in the thermal loading profile. In the Figure 3.12 both the loading caused by the changes in environmental condition and the loading which reasonate around the fundamental frequency and only the damage caused by the thermal stress caused by environmental conditions is taken into account. The steady-state junction temperature value is monitored and collected for each operating condition in the defined intervals of the solar irradiance and ambient temperature as shown in Figure 3.13

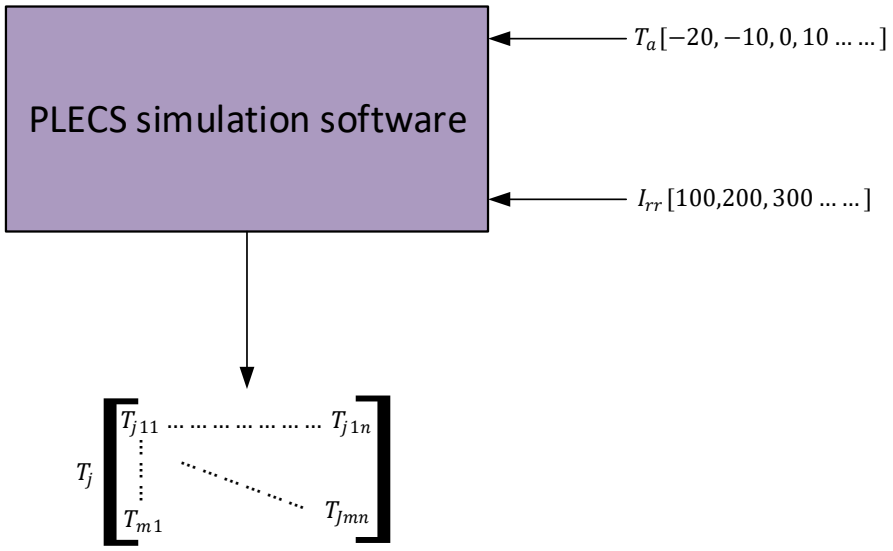


Figure 3.13: Obtain the junction temperature for each defined operational condition of the PV system

The junction temperature points contained in the obtained matrix is then used for interpolation of the applied mission profile, which is shown in Figure 3.14

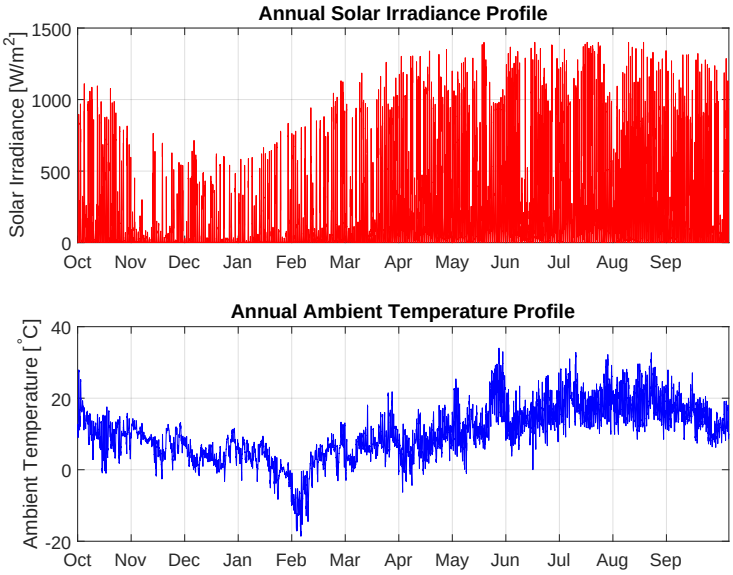


Figure 3.14: Annual Mission Profiles from Aalborg University

The data is collected at the local weather station at AAU the profile is of 1 second resolution. Interpolating the annual mission profile with the use of the operation condition points, the annual DC-link power and thermal loading profile is obtained as shown in Figure 3.15

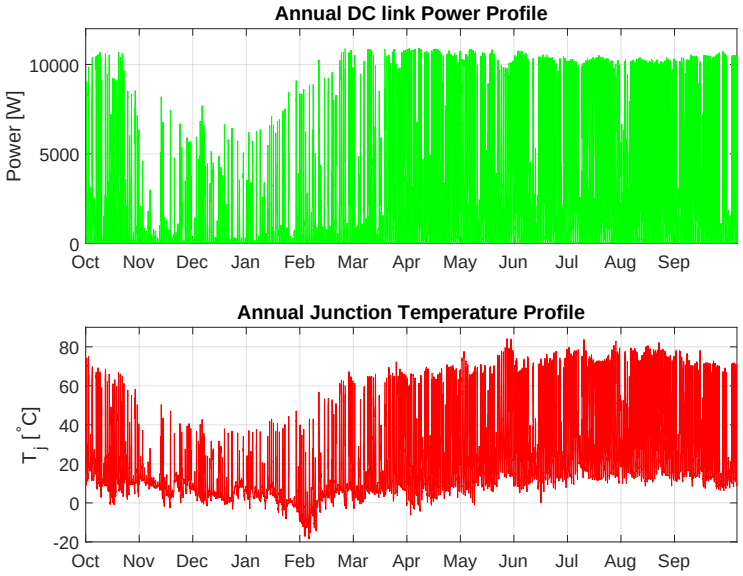


Figure 3.15: Annual DC-link Power and Junction Temperature Profiles

It is worth noticing that the thermal loading profile is far from being anywhere near the maximum allowed junction temperature of the IGBT at any point during the year of operation. The maximum allowed operating temperure of IGBTs is usually 150°c and there is a rule-of-thumb among eletrical engineers to include a design margin, which results in an operating temperature considerably lower than the maximum allowed in order to ensure

a longer lifetime of the device. In this case, where the margin is relatively big, the switch is rated at a continuous collector-emitter current of 50 A, while at rated conditions the current is no more that 23 A. Additionally is should be noted that the converter very rarely operates at rated conditions as a result of the applied mission profile only reaches this condition shortly during summertime. If the system, on the other hand, was designed with oversized PV array with respect to the converter rating, the scenario would have been of different character.

With the annual thermal loading profile at hand the wear-out analysis can be carried out but before initializing it, the entire mission profile translation analysis is summarised in the flowchart shown in Figure 3.16

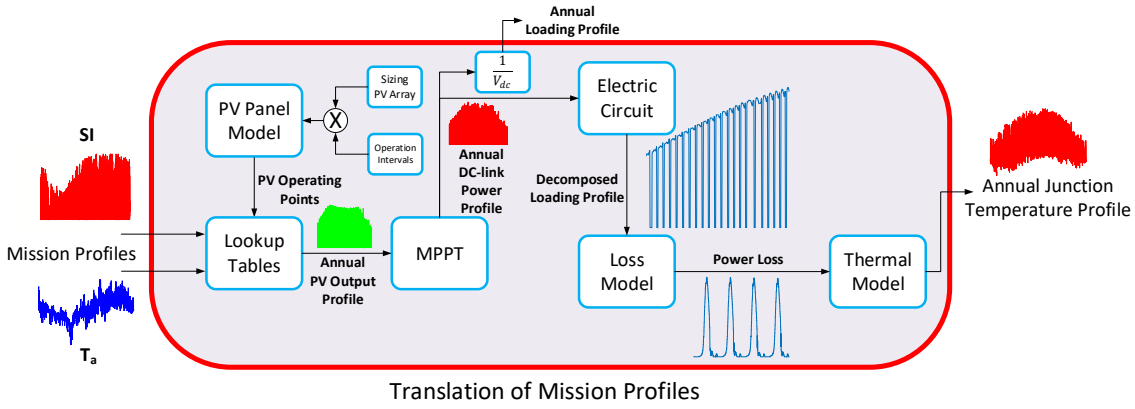


Figure 3.16: The mission profile analysis used to obtain the annual thermal loading profile

### 3.1.2 Wear-out analysis

In this section the damage caused on the IGBTs is obtained and their lifetime is estimation from the basis of the accumulated damage. Initially the thermal loading profile is required to be applied a counting algorithm to make it applicable to the used lifetime model.

As explained in 1.4 the dynamical nature of the obtained annual thermal loading profile is not applicable with the used lifetime model. A counting method is therefore required, in order to decompose the profile into categorized regular cycles and then apply the categorized cycles to a lifetime model [29]. The rainflow algorith is a widely used counting method in stress analysis related to thermal cycling and is applied to the annual thermal loading profile to extract the listed variables at load reversals

- Cycle Amplitude, $\Delta T_j$
- Cycle Mean Value $T_{j,mean}$
- Number of Cycles $n_i$
- Cycle Beginning Time
- Cycle Period, $2 \cdot T_o n$

The rainflow output is visualized through the Rainflow matrix histogram as shown in Figure 3.17

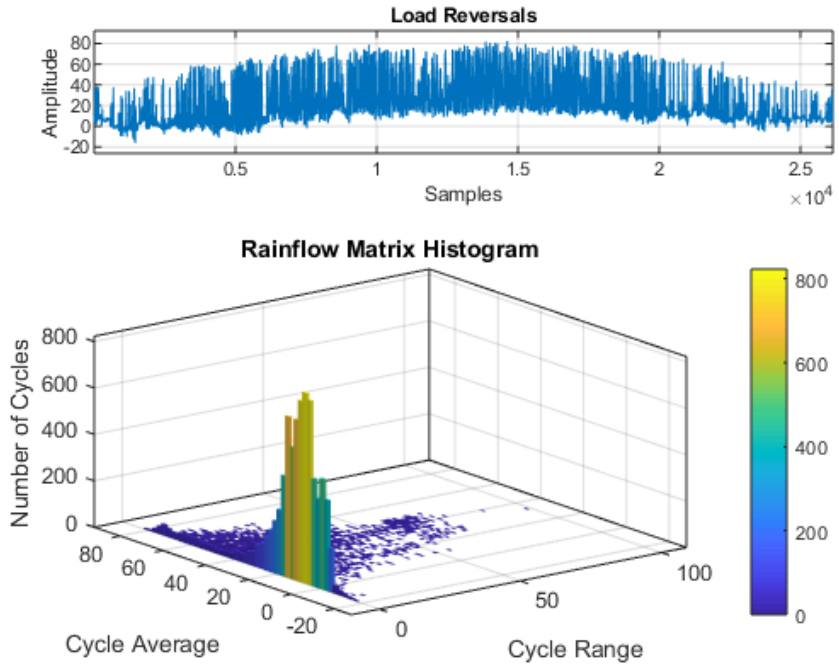


Figure 3.17: Histrogram of the output of the Rainflow Algorithm

It can be observed that the majority of the extracted cycles is of low amplitude, which contribution to the accumulated damage is more or less insignificant. Still all the extracted cycles is applied in the lifetime model used for estimating the lifetime of the IGBTs, which is expressed as [63]

$$N_f = L \cdot (\Delta T_j)^{\beta_1} \cdot e^{\left(\frac{-\beta_2}{T_{j,mean}}\right)} \cdot \left(\frac{t_{on}}{1.5}\right)^{-\beta_3} \tag{3.6}$$

The model in (3.6) is based on the Coffin-Manson law, which relates the temperature variation amplitude, $\Delta T_j$, with the number of cycles to failure. Additionally, the cycle period and the Arrhenius term are added to take into account the lifetime degrading effect of the mean junction temperature and the heating time. The $\beta_2$ parameter in the Arrhinus term, denotes the ratio of the activation energy, $E_a$, and the Boltzmann's constant, $k_b$ [16].

The parameters of the lifetime model is determined with the aid of curve fitting of experimental data, which are supplied by the manufacturer of the power devices as presented in [30]. The obtained model parameters and their corresponding fitted functions are presented in Figure 3.18

The cycle period, $t_{on}$, used during lifetime testing was 1.5 seconds. A typical relation for use of other cycle periods follows a linear trend on a logarithmic scale and can be expressed as

$$\frac{N_{cyc}(t_{on})}{N_{cyc}(1.5s)} = \left(\frac{t_{on}}{1.5s}\right)^{-0.3} \tag{3.7}$$

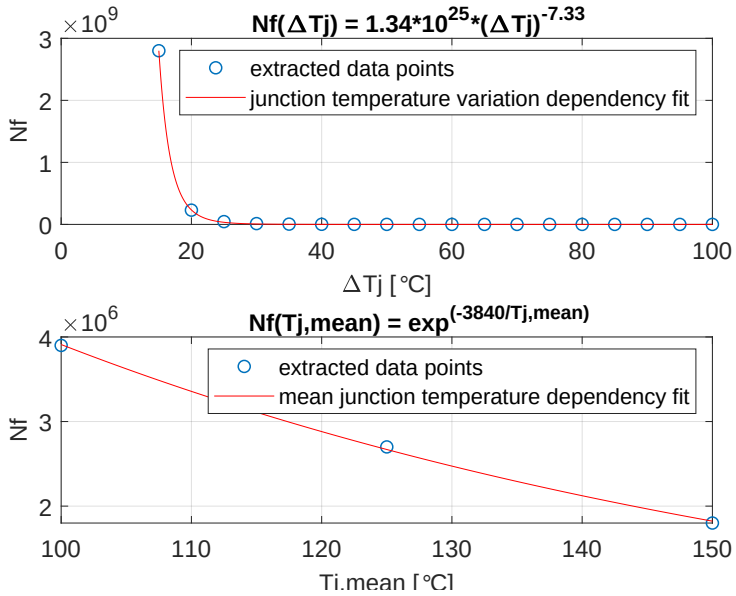


Figure 3.18: Upper: Determination of the Coffin-Manson parameters. Lower: Determination of the Arrhenius parameter

As it can be observed from (3.7), the value of $\beta_3$ is 0.3, which ensures the correct cycle period dependency correlation to other values for $t_{on}$ than 1.5s [30]. This particular on-time relation is only applicable for cycles of $t_{on} \leq 60s$. Applying cycles of longer duration can result in wrong lifetime results and as a result all the extracted cycles above one minute duration, is changed to be of one minute [60]. It should also be noted that the parameter values and the corresponding lifetime estimation is inevitable to lose some precision, when the condition of manufactures testing condition is replaced with those of the converter in field operation. The optimal approach would be to determine the lifetime model parameters on real field data i.e data obtained from converters operating under actual working conditions [58].

The lifetime consumption is calculated by use of the Miner's rule, which make use of the assumption of linear damage accumulation and it can be expressed as [80]

$$A_D = \sum_{i=1}^{n} \frac{n_i}{N_{f,i}} \tag{3.8}$$

where $n_i$ is the amount of cycles extracted from the rainflow counting and $N_{f,i}$ is the number of cycles until the end-of-life obtained in (3.6), which is dependent on the thermal reliability metrics extracted from the rainflow counting. The lifetime consumption is used as an indication of how much of the total lifetime of the power device is consumed, as a result of applying the annual mission profile to the system. The thermal cycling variables is iterated for all the contained values in the thermal loading profile and the annual damage of the switch, due to cyclic stress, can be obtained as

$$A_D = \sum_{i=1}^{n} \frac{n_i}{A \cdot (\Delta T_{j,i})^{\beta_1} \cdot e^{\left(\frac{E_a}{k_b \cdot T_{j,mean,i}}\right)} \cdot \left(\frac{t_{on,i}}{1.5}\right)^{-\beta_2}} = 0.1259 \tag{3.9}$$

the annual accumulated damage caused by the applied mission profile is 12.6% of the total lifetime of the switch, which results in a estimated lifetime of

$$\text{IGBT Lifetime} = \frac{1}{D_A} \approx 8\,\text{Years} \tag{3.10}$$

### 3.1.3 Sensitivity analysis

Uncertainty needs to be taken into account as the parameters of the lifetime model will vary at different testing and operating conditions and the electrical parameters of the components can also differ to variations in the manufacturing process and lastly the applied stress to components can also vary on a year-to-year basis due to climate variations. Instead of using fixed valued parameters, each parameter will be modelled as probability density functions with each having carefully chosen variance. Taken into account the uncertainty of each parameter will result in a more useful lifetime estimation, which can be presented with a certain amount of statistical confidence [66] [58] [81] [43].

#### Determination of static equivalents

Initially static parameter values of the stress variables is to be determined. The static equivalents of the variables used in the lifetime model is determined as to produce the same amount of number of cycles to failure as the entire amount of stress cycles extracted from the rainflow algorithm did

$$N_{f,i} = N_{f,static} = A \cdot (\Delta T_{j,static})^{\beta_1} \cdot e^{\left(\frac{E_a}{k_b \cdot T_{j,mean,static)}}\right.} \cdot \left(\frac{T_{on,static}}{1.5}^{\beta_2}\right) \tag{3.11}$$

The static equivalent values is then used as the mean values when modelling the stress variables as probability density functions. The static equivalents of the cycle on-time and the mean junction temperature is simply determined by use of the mean value during the entire operation, which leads to $T_{on,static} = 9.62$s and $T_{j,mean,static} = 42.54°$ [58]. With the aforementioned static values at hand, results in one degree-of-freedom in (3.11). The known values are inserted and $\Delta T_{j,static}$ is isolated variable, which results in a static value for the temperature variation of $\Delta T_{j,static} = 39.9°$. Besides the stress parameters, the lifetime parameters obtained from curve fitting will also be used as mean values when modelling the probability density functions of the lifetime parameters. The mean values of the lifetime model parameters along with the number of extracted cycles from the rainflow algorithm and relevant lifetime model coefficients are summarised in table 3.1

| Obtained lifetime model parameters and useful lifetime model coefficients | |
|---|---|
| Number of Extracted Cycles $N_{cycle}$ | $3.27{\cdot}10^{6}$ |
| Lifetime Model Multiplicative Temperature Variation Parameter $A$ | $1.34{\cdot}10^{25}$ |
| Lifetime Model Exponential Temperature Variation Parameter $\beta_1$ | -7.33 |
| Lifetime Model Exponential Cycle On-time Parameter $\beta_2$ | -0.3 |
| Activation Energy of the IGBT $E_a$ | $5.75{\cdot}10^{-20}$ J/mol |
| Boltzmann Constant $k_b$ | $1.38{\cdot}10^{-23}$ J/K |

Table 3.1: Obtained lifetime model parameters and fixed coefficients used in the lifetime model

### 3.1.4 Modelling the parameters as distribution functions

The static equivalent values along with previously used lifetime model parameters are used as mean value of the normally distributed probability density function. The tolerances used in the lifetime model parameters is based on [5], which conducted some regresssion models to determine the tolerance. An exception is the multiplicative A parmameter, which is chosen to have a tolerance of 10% of the mean value. All the parameters are modelled as normal distributions based on their respective means and variance. The distribution function models for each of the parameters contained in the lifetime model are shown in Figure 3.19

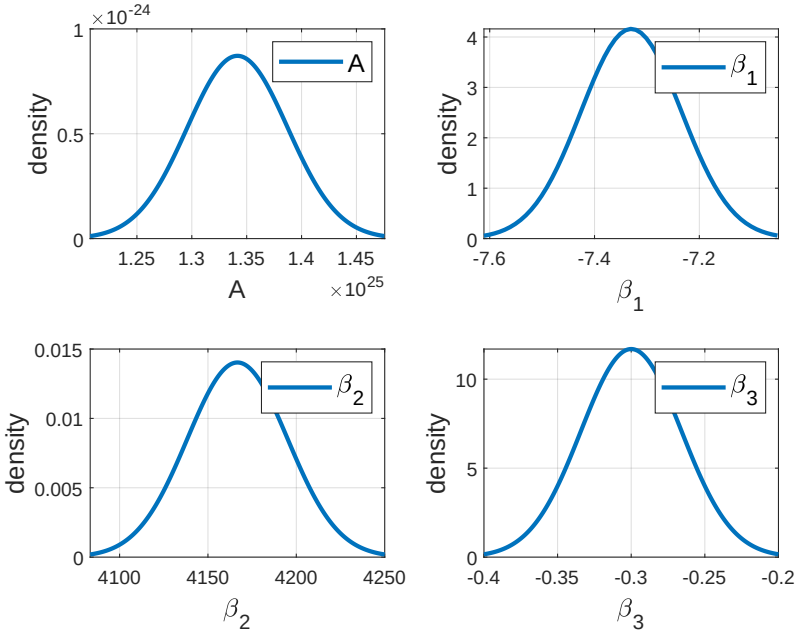


Figure 3.19: Distribution Function Models of the Lifetime Model Parameters

where each of their respective tolerances are summarised in Table 3.2

| Tolerances Used for Distributions Functions | |
|---|---|
| Multiplicative Temperature Variation Parameter $A$ | $1.34{\cdot}10^{24}$ |
| Lifetime Model Exponential Temperature Variation Parameter $\beta_1$ | 0.281 |
| Lifetime Model Exponential Mean Temperature Parameter $\beta_2$ $(E_a/k_b)$ | 83.33 |
| Lifetime Model Exponential Cycle On-time Parameter $\beta_3$ | 0.1 |

Table 3.2: Tolerances used when modeling the lifetime model parameters as distribution functions [5]

As for the electrical parameter variation, the collector emitter voltage is stated in the datasheet to have a tolerance of 0.3V [31]. The variation of the collector-emitter voltage has an influence on the conduction losses and therefore also indirectly on the junction temperature and is therefore needed to be taken into consideration. The system at

rated power without added collector-emitter voltage tolerance is simulated and a value of mean junction temperature of $81°C$ was obtained. Executing the simulation again at same operating condition but added the collector emitter voltage tolerance a variation in temperature of $\Delta T_{j,vce} = 6°C$ was obtained. The tolerance of the collector-emitter voltage does not only influence the mean junction temperature but also the magnitude of the temperature variation, this change in magnitude was determined analytically by use of the following expression [76]

$$\Delta T_j(t_p) = P \cdot \sum_{v=1}^{n} R_{thv} \cdot \left( \frac{1 - \frac{-t_p}{e^{\tau_{thv}}}}{1 - \frac{-t_T}{e^{\tau_{thv}}}} \right) \tag{3.12}$$

where $t_p$ is on-time of the loss cycle, $t_T$ is the period of the entire cycle, $R_{thv}$ is the resistance of each layer in the Foster/Cauer network used to represent the thermal modelling and $e^{\tau_{thv}}$ is the term representing the time constant of each respective layer [76]. Using the additional power loss caused by the collector emitter voltage tolerance in equation (3.12) a temperature variation of 0.87° was obtained. Finally a variation in mean junction temperature due to variation of ambient temperature is included. An optimal approach would be to apply mission profiles at different locations from around the world but as focus was put other wisely, the approach of including variance in the junction temperature was adopted to make amends. A variation interval of 15° was adopted in this project to compensate for not including several mission profiles. The distribution models for each of the aforementioned parameters are shown in Figure 3.20

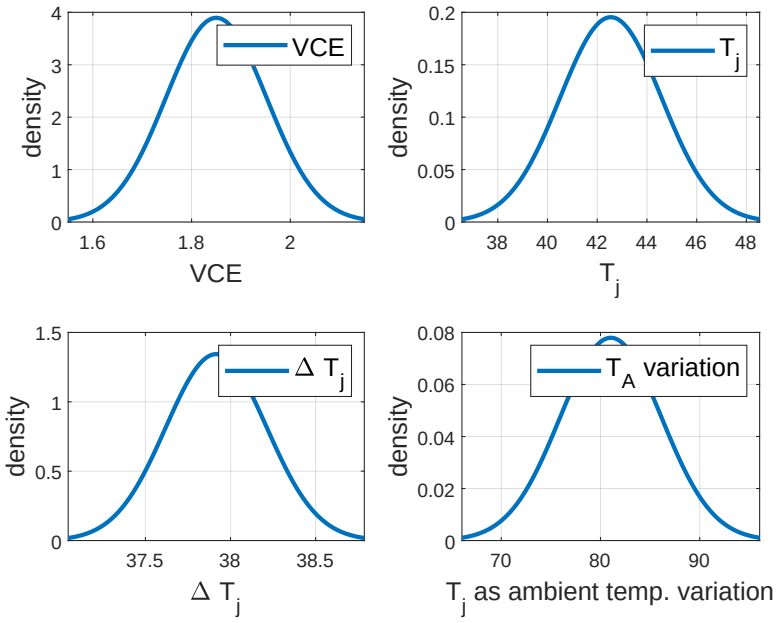


Figure 3.20: Distribution function models of $V_{CE}$, $T_{j,mean}(V_{CE})$, $\Delta T_j(V_{CE})$ and $\Delta T_j(T_a)$

10000 random samples constitute the parameter distributions used for the each of the parameters, which is included in the sensitivity analysis. The sensitivity analysis will provide insight in how much influence each of these tolerances has on the number of cycles to failure. This is by including individual parameter variation while the remaining parameters are kept at their mean values. As it can be observed in Figure 3.21, the

exponential temperature variation of $\beta_1$ parameter, results in a big standard deviation in the number of number of cycles to failure distribution.

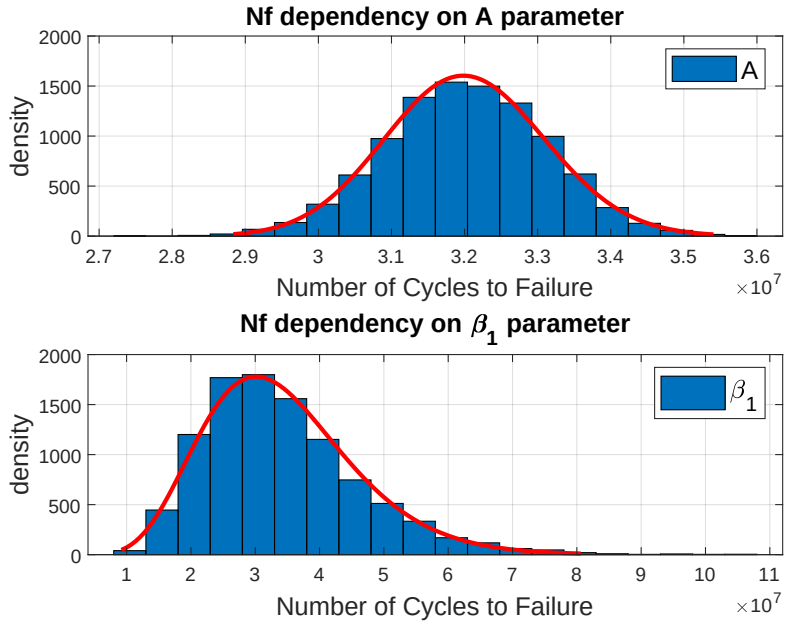


Figure 3.21: Sensitivity analysis of the number of cycles to failure dependency on the multiplicative temperature variation $A$ parameter and the exponential temperature variation $\beta_1$ parameter

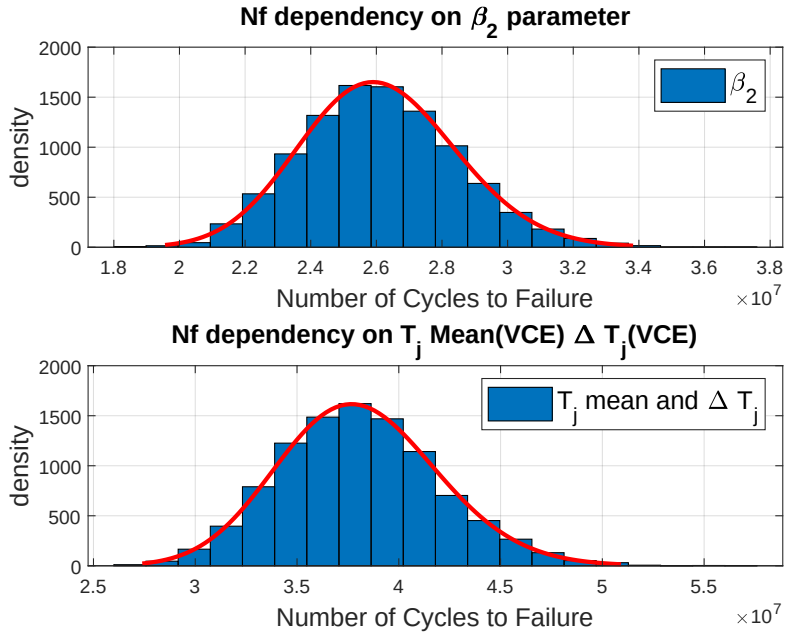


Figure 3.22: Sensitivity analysis of the number of cycles to failure dependency on the Arrhenius term mean junction temperature $\beta_2$ parameter and the combined impact from the mean temperature and the variation temperature amplitude both caused by tolerance of the collector-emitter voltage

The relatively big standard deviation indicates that the $\beta_1$ parameter has a major influence

on the number of cycles to failure, despite having minor tolerance value. The variation of number of cycles to failure caused by the junction temperature variation amplitude $A$ parameter is relatively small even though the tolerance value are of 24th order. In Figure 3.22 the mean junction temperature $\beta_2$ variation can be observed to have a fairly small impact on number of cycles to failure variation. Both variations of the mean junction temperature and the temperature variation amplitude, which are caused by the $V_{ce}$ tolerance, are combined to examine the overall impact of the collector emitter voltage variation and as it can be observed, it does have some impact on the number of cycles to failure. Lastly it can be observed in Figure 3.23 that the exponential on-time $\beta_3$ parameter has a small impact on the number of cycles to failure

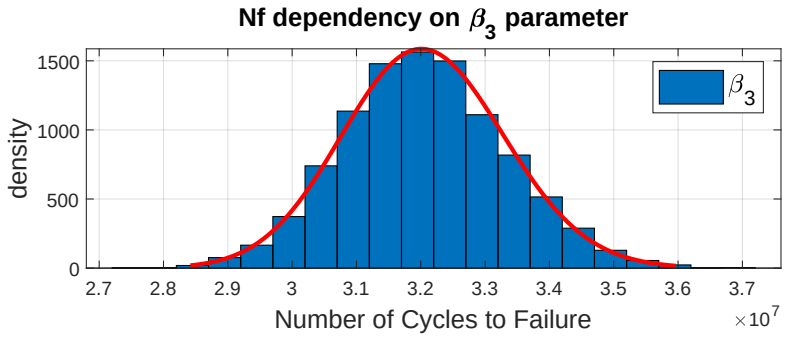


Figure 3.23: Sensitivity analysis of the number of cycles to failure dependency on the exponential en-time $\beta_3$ earameter

In order to provide a more exact view on these parameter variations direct impact on the lifetime, the accumulated damage distributions for each are now presented.

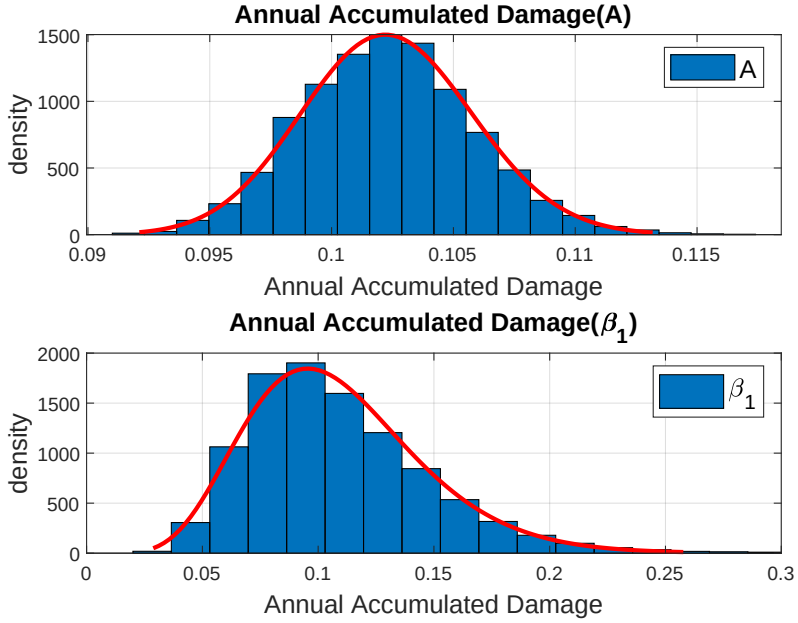


Figure 3.24: Sensitivity analysis of the annual accumulated damage dependency on the multiplicative temperature variation $A$ parameter and the exponential temperature variation $\beta_1$ parameter

As it can be observed in Figure 3.24, the variation of the exponential temperature variation $\beta_1$ parameter can cause a difference from 5 to 20 percent of the total lifetime consumed by applying the year long mission profile. The multiplicative temperature variation $A$ parameter only leads to a variation from 9.5% to 11% accumulated damage caused by the same mission profile. The variation in accumulated damage is limited to maximum 5% for both the cases of the variation of the Arrhenius mean junction temperature $\beta_2$ parameter and the variation of temperature caused by the collector emitter voltage tolerance, as can be observed in Figure 3.25

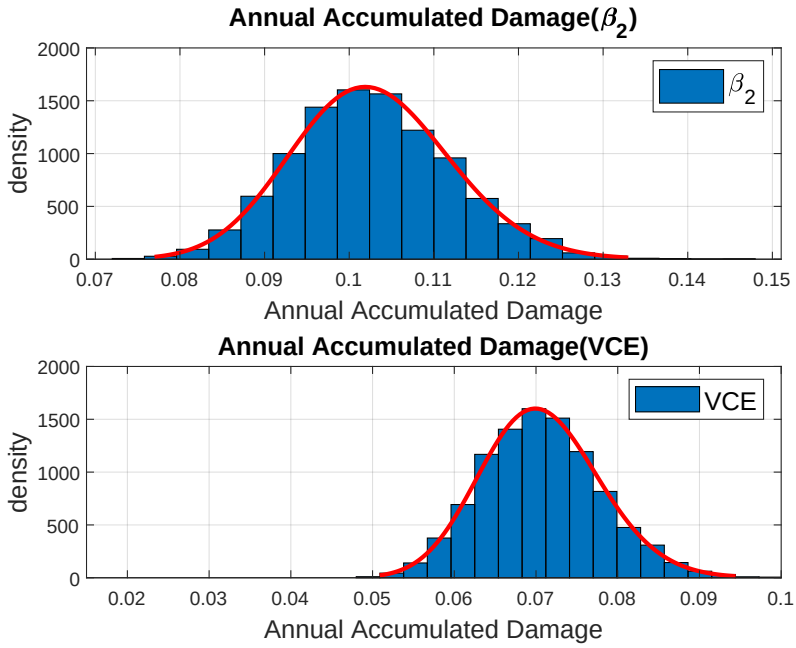


Figure 3.25: Sensitivity analysis of the annual accumulated damage dependency on the Arrhenius mean junction temperature variation $\beta_2$ parameter and the collector-emitter voltage tolerance

The exponential on-time $\beta_3$ parameter has an even smaller impact on the accumulated damage with only a variation of 1.5%, as seen in the distribution shown in Figure 3.26

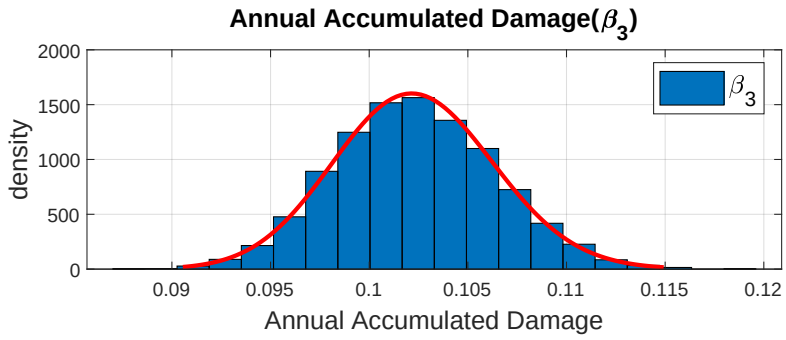


Figure 3.26: Sensitivity analysis of the annual accumulated damage dependency on the exponential on-time $\beta_3$ parameter

As it can be concluded from the sensitivity analysis, the lifetime of the IGBTs depends mostly on the parameters, which are related to the junction temperature variation, $\Delta T_j$.

The variation of all the parameters are executed in order to obtain an overall lifetime distribution of the IGBTs, which is commonly knows as a Monte Carlo analysis. 10000 random samples is taken from each of the distributions of all the parameters which are subjected to variation within their predefined tolerances. The obtained lifetime distribution is within a interval of 5 to 20 years with an undefined confidence level. The number of cycles to failure distribution and the lifetime distribution obtained from carrying out the Monte Carlo analysis are shown in Figure 3.27

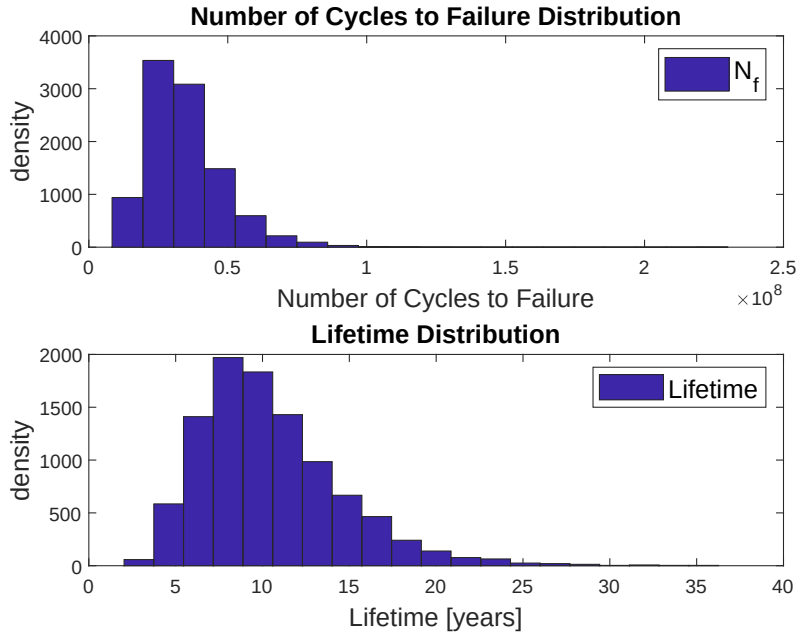


Figure 3.27: Number of cycles to failure distribution and lifetime distribution of the IGBT when applied to an annual mission profile from Aalborg University

It can be observed in the lower histogram in Figure 3.27, that the lifetime distribution ranges from about 4 to 25 years, when the uncertainty of all the relevant parameters are taken into consideration. The obtained lifetime distribution is then fitted to a Weibull chart with the use of the obtained shape, $\beta$, and scale, $\eta$, parameters

$$\beta_{wb} = 11.75 \quad \text{and} \quad \eta_{wb} = 2.65 \tag{3.13}$$

These parameters are used to obtain the cumulative distribution function, which can express the unreliability as a function of time. In other words the unreliability function represents the proportion of failures within the entire population as a function of time.

$$F(t) = 1 - e^{-\left(\frac{t}{\eta}\right)^{\beta}} \tag{3.14}$$

The cumulatively distribution function for the obtained lifetime distribution is shown in Figure 3.28. The y-axis denotes the probability of failure over the timespan of the IGBT lifetime. For a population of IGBTs 10% of the population is said to have failed at the

probability of 0.1, which is known as the $B_{10}$ lifetime. In the case of the IGBTs, the $B_{10}$ lifetime is 6 years as shown in the Figure 3.29

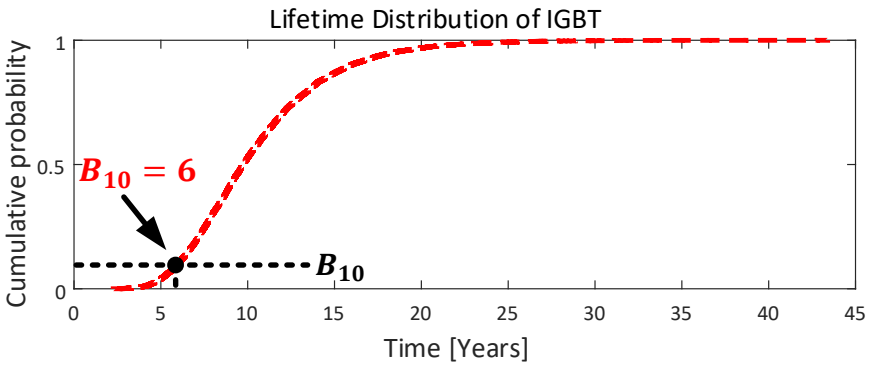


Figure 3.28: Cumulative Distribution Function of the IGBT Lifetime

With the lifetime distribution of the inverter IGBTs at hand, the lifetime of the remaining components is be determined. Before moving on to the single IGBT in the DC/DC stage the complete wear-out analysis is summarised in Figure 3.29

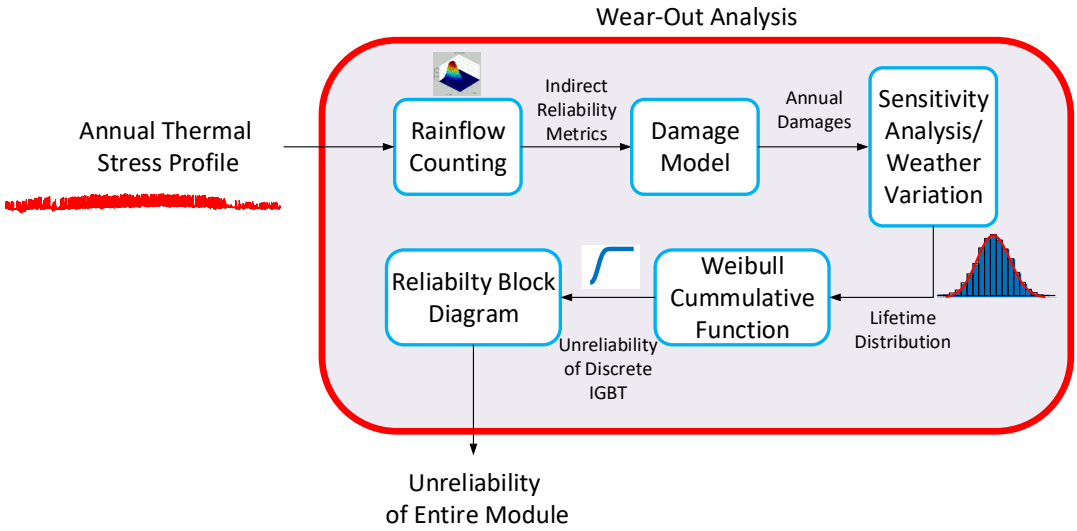


Figure 3.29: Flowchart of the Wearout Analysis Conducted in this Chapter

As it can be observed in Figure 3.29, the last step is to obtain the reliability of the entire module, as the lifetime obtained in this chapter is for a discrete IGBT only. The entire lifetime of the module and the system in general is carried out in Chapter 5.

## 3.2 IGBT in the DC/DC stage

As the lifetime analysis of the IGBT in the DC/DC stage is completely analogous to the one previously carried out for the inverter IGBTs in Section , only the results will presented

in this section. The turn-on and turn-off energies are obtained in the same manner with the extraction of the datasheet information, which is extracted and used for power loss modeling in the simulation software. The turn-on energies for the active switch in the DC/DC stage is shown in Figure 3.30

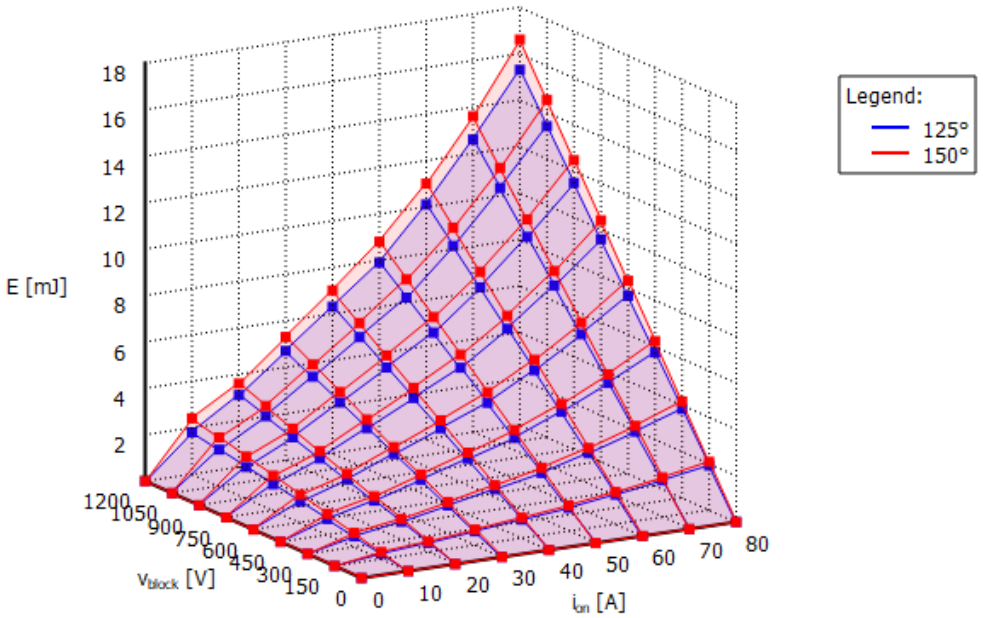


Figure 3.30: Look-up table used to obtain the turn-on energies of the IGBT

As observed in the Figure 3.30, the turn-on energies are somewhat lower than those of the active switch in the DC/AC stage shown in Figure 3.2. As the switch in the DC/DC is at lower ratings, the junction temperature is still expected to be higher than the ones obtained in the DC/AC stage, as the turn-on energies difference in the switches is relatively small. The turn-off energies is not shown, but the trend is the same with lower values compared to those of the DC/AC stage switches. The modeling of on-state losses is also modeled in the same manner as those of the DC/AC stage and presented in Figure 3.31

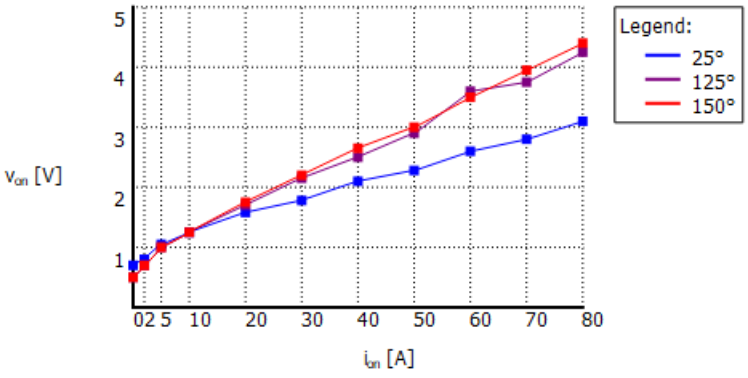


Figure 3.31: Look-up table used to obtain the conduction losses of the IGBT

The forward voltage trend seems at first impression to be the exact same of those of the

DC/AC stage, but as the current rating is lower for this particular switch, the forward is higher at the same load currents compared to DC/AC switch. The thermal impedance of the IGBT in the DC/DC stage differs only from the one in the DC/AC stage in terms of the junction to case part as the external thermal network used, is the exact same at both stages. The foster parameters representing the junction to case thermal impedance of the active switch in the DC/DC stage is shown in Figure 3.32

| | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| R | 0.051 K/W | 0.117 K/W | 0.426 K/W | 0.506 K/W |
| τ | 0.0005 s | 0.005 s | 0.05 s | 0.2 s |

Figure 3.32: Thermal impedance from junction to case

As observed in Figure 3.32 the total thermal resistance is twice the size of those of the DC/AC switch, when summing the thermal resistance of all four layers. The increase in thermal resistance is going to affect the annual loading profile to be more severe in terms of more aggressive loading when compared to the loading of the active switch in the DC/AC stage. Obtaining the junction temperature for all the predefined operating conditions of the DC/DC stage and then by means of interpolation, the annual thermal loading profile of the active switch can be obtained as shown in Figure 3.33

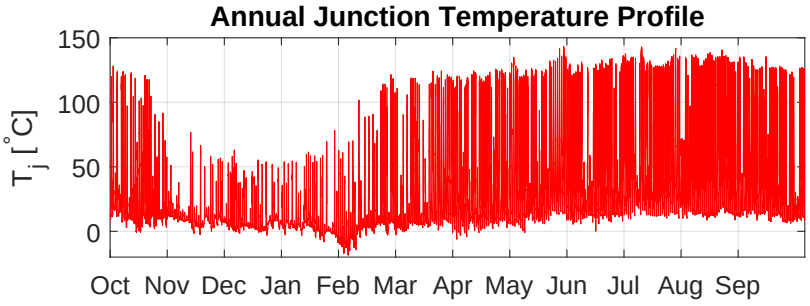


Figure 3.33: Annual thermal loading of the active switch in the DC/DC stage

The resulting profile is a lot more aggressive than expected, with temperatures in the proximity of the maximum allowed of the switch doing a large part of the year. This is probably not only caused by the higher thermal resistance of the junction to case thermal impedance but is most likely also caused by how the loading is applied. The switch at the DC/DC stage handles all the transferred energy, whereas the switches in the DC/AC stage divides the stress among the six switches during one fundamental period. In retrospect, the active switch in this stage, should have been chosen at higher ratings, as the lifetime obtained is about 2 years.

### 3.2.1 Monte Carlo analysis and B10 lifetime

The static equivalents differ a lot from those obtained in the previous section for the DC/AC stage as the number of cycles to failure, as used in expression (3.11), is reduced significantly. The static value, which has the largest influence on the lifetime distribution,

as proven in the previous sensibility analysis, is the static equivalence of the junction temperature variation, $\Delta T_{j,static}$. The obtained value is of $\Delta T_{j,static} = 59.6°c$, which is considerably higher than the one obtained in Section 3.1.3. The obtained lifetime distribution and the cumulative distribution function are shown in Figure 3.34

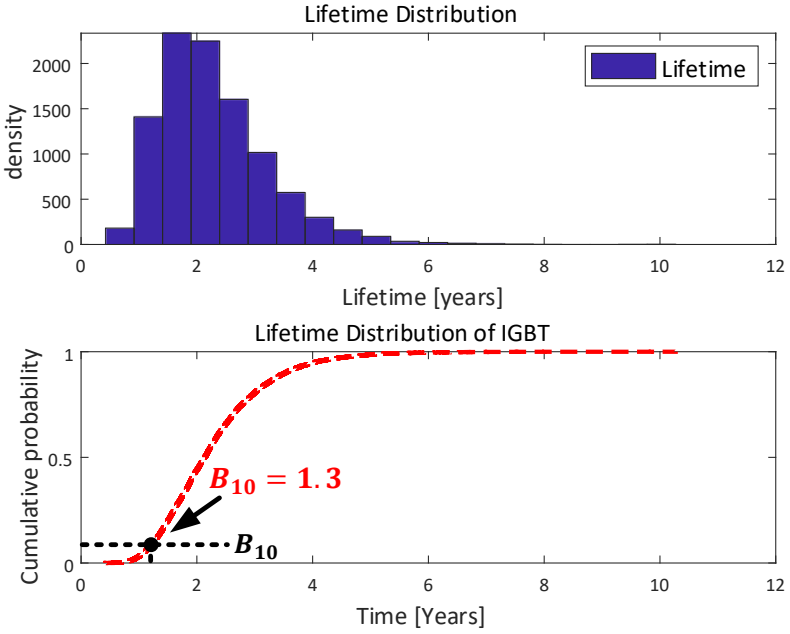


Figure 3.34: Lifetime distribution and cumulative distribution function obtained for the active switch in the DC/DC stage

As it can observed from the unreliability plot in Figure 4.13, a $B_{10}$ lifetime of only 1.3 years was obtained for the active switch, which its highly critical and the analysis should have been repeated with several other switches but due time and page limitations, it will not be included in this project.

# Lifetime Estimation of Passive Components 4

*In this chapter the wear-out analysis of the passive components will be carried out. This mostly concern the DC-capacitor, as lifetime analysis of capacitors differ from the previous analysis carried out in Chapter 3. In case of the diodes only the result will be presented, as their lifetime analysis is analogous to the one used to obtain the lifetime of the active switches. In case of capacitors it also involves obtaining the thermal loading by means of a mission profile translation, which is used for obtaining the annual accumulated damage, from which the lifetime can be estimated. Finally, the uncertainties linked to capacitors are taken into account and a lifetime distribution is obtained by means of a Monte Carlo analysis*

## 4.1 DC Link capacitor

As mentioned in 1.5, DC-link capacitors serve as important part of the PV-system, as they reduce the DC-link voltage ripple, absorb the harmonics and provide energy storage. A visualization of the DC-link as being a part of the overall PV-system is shown in Figure 4.1

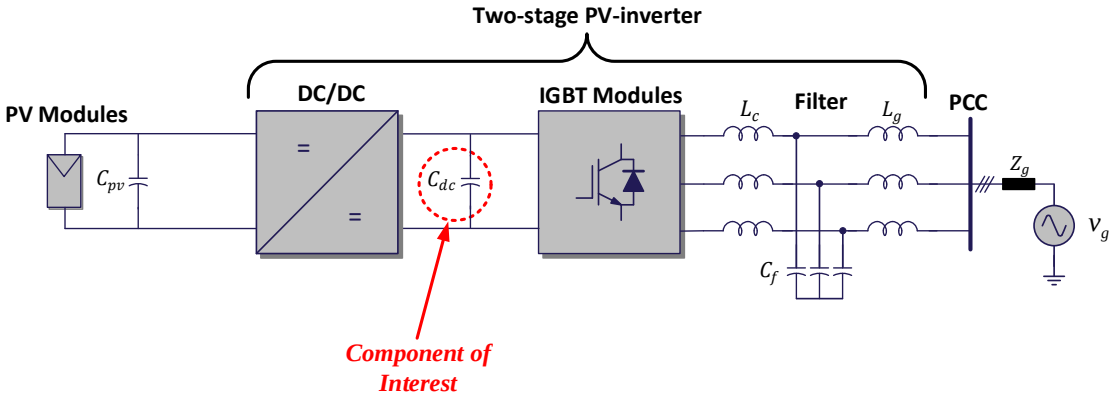


Figure 4.1: Visualization of the DC link capacitor in the overall PV system

A commonly used equivalent circuit representation used for modeling of the DC link capacitor is shown in Figure 4.2 [79]


Figure 4.2: Commonly used equivalent circuit representation of the capacitor

As seen in the equivalent circuit in Figure 4.2, the capacitor also consits of an equivalent series resistance and an equivalent series inductance, which will dominate the impedance at high frequencies. In terms of reliability the equivalent series resistance is important factor, as when capacitors is subjected to loading resistive losses will occur, which will induce a temperature increase. The temperature is a function of the external generated heat generated by the resistive losses but also the surrounding ambient temperature of the operational environment. The size of the resistance can be determined by means of the dissipation factor (DF), which is shown in Figure 4.3. [21]

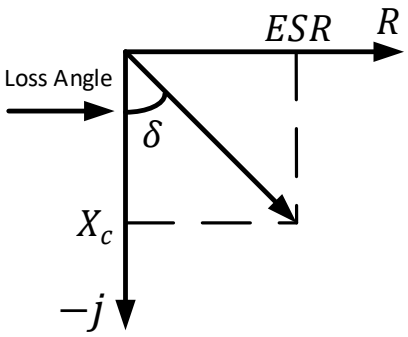


Figure 4.3: Impedance plane with the loss angle shown, which is used to determine the size of the equivalent series resistance

Applying general triogonometric theory, the loss angle can be determined as the tangent to the ratio of the ESR and the amplitude of the capacitive reactance as

$$tan(\delta) = \frac{\text{opposite}}{\text{adjescent}} = \frac{ESR}{|X_c|} \Leftrightarrow ESR = \frac{1}{\omega C} \cdot tan(\delta) = \frac{1}{2\pi f C} \cdot tan(\delta) \tag{4.1}$$

Inserting the values of the capacitance and the loss angle provided by the datasheet of the manufacture, the ESR at 100Hz is determined to be 70mΩ.

### 4.1.1 Modelling of the ESR

Similar to the impedance of inductors and capacitors the resistance is frequency dependent and using a fixed value will provide an incorrect amount of losses generated in the capacitor and therefore also an incorrect amount of thermal stress applied [15]. The ESR usually decreases with temperature, as it is often dictated by the variation in the electrolytic viscosity but in some cases some capacitors are dominated by the positive temperature coefficients of the metallic and dielectric material [20] .

In all cases the ESR decreases monotonically with the increasing of the frequency until the skin effect of the metallic components has its on-set, which is typically at $f \geq 100kHz$

[20]. The ESR of the given capacitor was measured in a large frequency range by means of a conventional LCR meter and the normalized values was used to create a frequency dependent model of the ESR as shown in Figure 4.4.

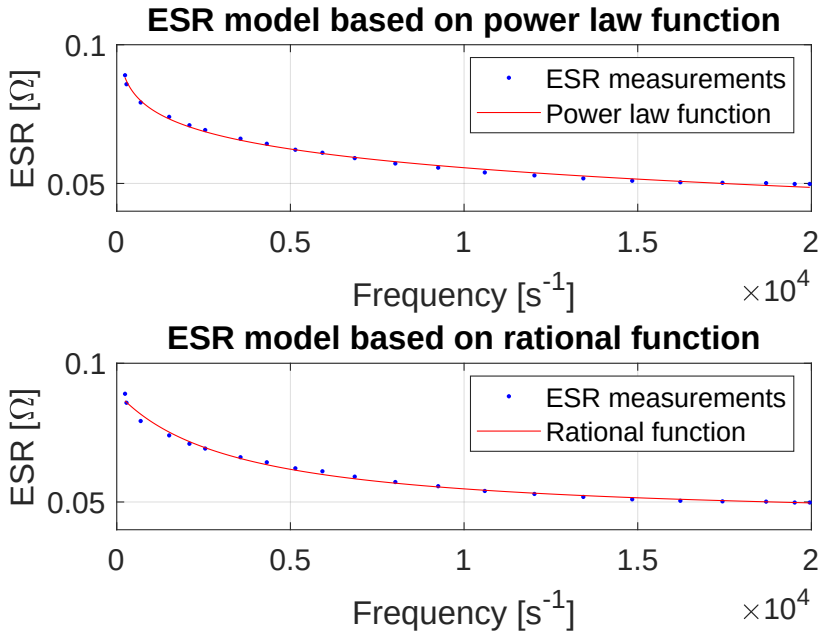


Figure 4.4: Models used to describe the frequency dependency of the equivalent series resistance

Two types of models showed potential by replicating the tendency of the data points at the entirety of the frequency range, the two models are based on the power law and the rational function respectively. As shown in Figure 4.4, the power law function seems to underestimate the ESR value at high frequencies, which is not the case with the rational function, that seems to be in accordance with the measured values in the span of the entire frequency range. The frequency dependent ESR model based on a rational function is described as

$$ESR(f) = \frac{0.04288 \cdot f + 305.2}{f + 3410} \tag{4.2}$$

It should be noted at this stage, where a complete design of the capacitor bank is unknown, that it is only for certain that two capacitors in series is needed, as the capacitors are rated at 450V and the DC link operates at 750. A relatively large voltage margin is needed to be included, as the series connection of the two capacitors is not balanced a 100% and the capacitors does therefore not share the DC link voltage equally. A solution to the non-equal share, is to include balancing resistors in parallel with the capacitors but as this tends to make the configuration more complex and also introduce additional resistive losses, the solution is not chosen to be an integrated part of the DC link in this project. The final capacitor configuration will have a significant influence of how much stress each of the capacitors will be subjected to [24].

### 4.1.2 Ripple content and capacitor power loss

The power loss in the capacitor is obtained by the product of the ripple current components and the corresponding ESR value at a given frequency. The ripple current depends on which topologies is used at both the input and the output side of the DC-link as depicted in Figure 4.5 [46]

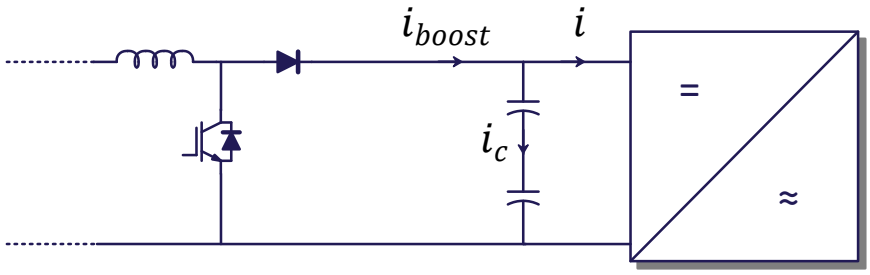


Figure 4.5: Ripple current content in the capacitor depends on the used topologies at the input and the output side of the DC link

In this case, active-based topologies is used on both sides of the DC-link, which results in a harmonic content of the capacitor at the switching frequency, its multiples and the corresponding sidebands of both converters as seen in Figure 4.6 [52]

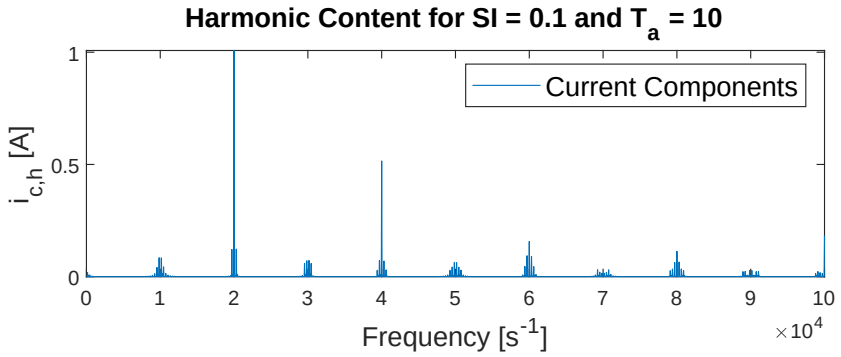


Figure 4.6: Harmonic content in the DC link in the case of active based topologies on each side of the DC link

The harmonic spectrum is obtained for each set of operational conditions by means of the fast Fourier transform (FFT) and the power loss in the capacitor can then be obtained as

$$P_{loss} = \sum_{h=1}^{N} i_{rms}^2(f_h) \cdot ESR(f_h) \tag{4.3}$$

In this case, the RMS value is obtained by utilising that all FFT components ia a weighted sum of sines and cosines [13]

$$i_{rms}(f_h) = \frac{i(f_h)}{\sqrt{2}} \tag{4.4}$$

It is a necessity, to obtain the RMS value is this manner, as each individual component is to be multiplied with the corresponding ESR value at a given frequency.

The exact same one second resolution mission profile, as presented in 3.1.1, is applied when estimating the lifetime of the DC-link capacitor. Applying the mission profile in the case of a single capacitor branch, results in the annual loss profile shown in Figure 4.7

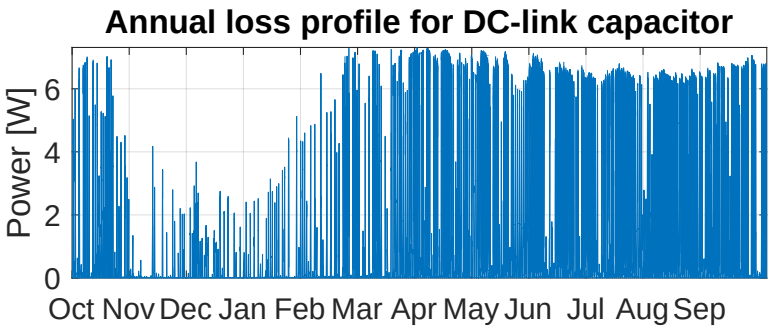


Figure 4.7: Annual generated loss profile in the case of a single capacitor branch

This is a relatively high power loss for this specific capacitor. The relatively high power loss is a result of having one single capacitor branch, which is to handle the entire ripple current. Using this configuration will result in a short capacitor lifetime, as the hotspot temperature would end up being above the rated one during a large part of its operation cycle.

### 4.1.3 Bank configuration

In order to ensure a proper lifetime of the capacitors, a proper bank configuration is required in terms of number of parallel branches, which will share the ripple current as depicted in Figure 4.8

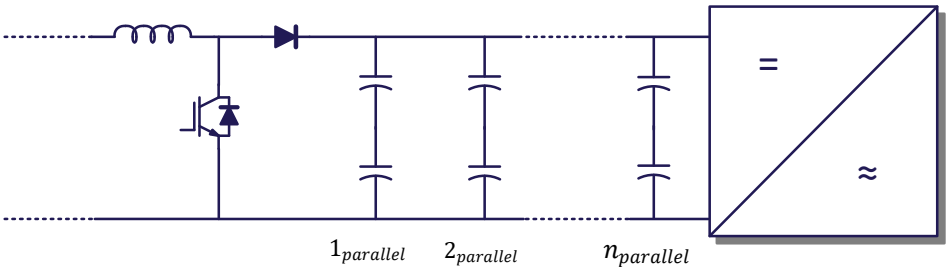


Figure 4.8: Design of the capacitor bank by introducing several parallel branches to improve the ripple current capability

There are some issues which should be considered, when laying out a grid of capacitors such as the mutual heating among capacitors. If for example a grid of 3 x 4 is used the design ends up having two capacitors, which are completely surrounded by other capacitors, the capacitors placed in the center tend to get much warmer, than the surrounding capacitors and the grid does therefore need external cooling. Introducing external cooling will lower

the efficiency of the system, which is why that in a n x m grid either n or m should exceed 2. On the other hand a long and narrow bank configuration tends to complicate the goal of equal sharing of the ripple current [20]. In regards to connecting capacitors in series for voltage sharing purpose it also important that the capacitors in series operate at same core temperature, as this will dictate the leakage current profile of each capacitor, which is the main factor for the obtaining of voltage balance during steady-state conditions [20]. From the datasheet, it is stated that the used capacitor inherent a rated ripple current of, $i_{ac,max} = 2.52A_{rms}$ at 120Hz, a ripple multiplier of 1.41 for frequencies $f > 10kHz$, which are the relevant frequencies in this case [14]. The root mean square value of the current frequency components are calculated by means of the Parseval theorem, which states that the total energy is preserved through FFT and which can be expressed as [41]

$$i_{rms} = \sqrt{\sum_{f=50}^{f=100000} i_f^2} \tag{4.5}$$

The bank configuration design could be obtained by means of design iteration until a favorable lifetime is obtained as explained in 1.4. Instead it is chosen to develop a function which describes the ripple current for each configuration to prevent the tiresome approach of applying design iteration. The RMS current is calculated for each different parallel configuration, for the operation condition which will result in the maximum current injection in the DC-link. In this particular case, the condition is at $SI = 1.0$ and $T_a = -20°$. The resulting ripple current, as a function of n-paralleled converters, along with the maximum rated value at the relevant frequencies are shown in Figure 4.9

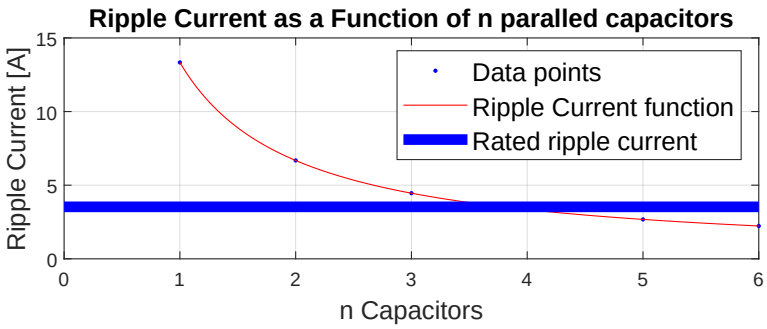


Figure 4.9: DC-link ripple current as a Function of n-paralleled capacitor branches

It can observed from Figure 4.9, that four parallel branches is required, to ensure that the ripple current content will not exceed the ratings at any time during an entire operation cycle. The power loss is once again calculated for each operational condition and the annual power loss for the chosen bank configuration is obtained and compared to the one consisting of one single branch. The annual loss profile for a 4 parallel capacitor branch configuration is shown in Figure 4.10

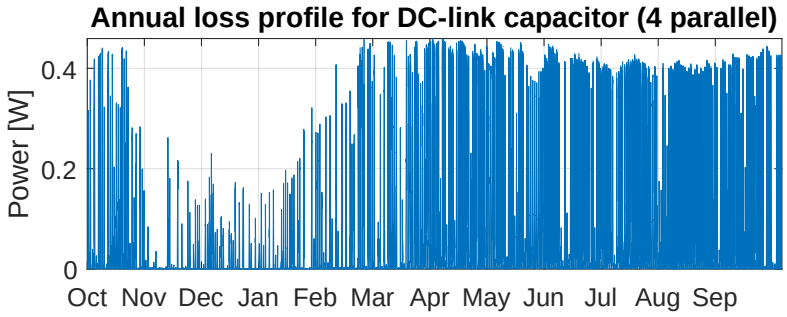


Figure 4.10: Annual loss profile obtained with the selected bank configuration

As seen in Figure 4.10, the loss in each capacitor is decreased significantly, by adding additional parallel branches for sharing of the ripple current.

### 4.1.4 Thermal model and the inclusion of local ambient temperature

A previously explained the main factor, which has a lifetime degrading effect is the operational temperature of the capacitor also known as the hotspot temperature. The annual hotspot profile can be obtained by means of applying the annual loss profiles to the thermal network shown in Figure 4.11

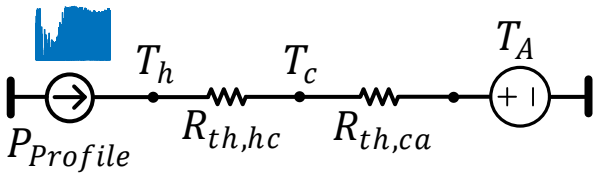


Figure 4.11: Thermal network used to obtain the annual hotspot temperature profile

where $R_{th,hc}$ is the thermal resistance from hotspot to case and $R_{th,ca}$ is the thermal resistance from case to ambient. The values for each is of the thermal resistances are gathered from a thermal resistance chart, which is provided by a leading manufacture of this particular type of capacitors [20]. The values used in this case are specifically for the condition of free convection, which implies that no external cooling are applied the capacitor bank. The used values are $R_{th,hc} = 3.28\,°C/W$ and $R_{th,ca} = 6.38\,°C/W$. The hotspot temperature can be obtained mathematically as

$$T_h = T_{hc} + T_{ca} + T_a = P_{profile} \cdot (R_{th,hc} + R_{th,ca}) + T_a \tag{4.6}$$

Applying the annual power loss profiles to the thermal network results in the annual hotspot temperature profiles for both the 4-branch and the single branch configuration as shown in Figure 4.12

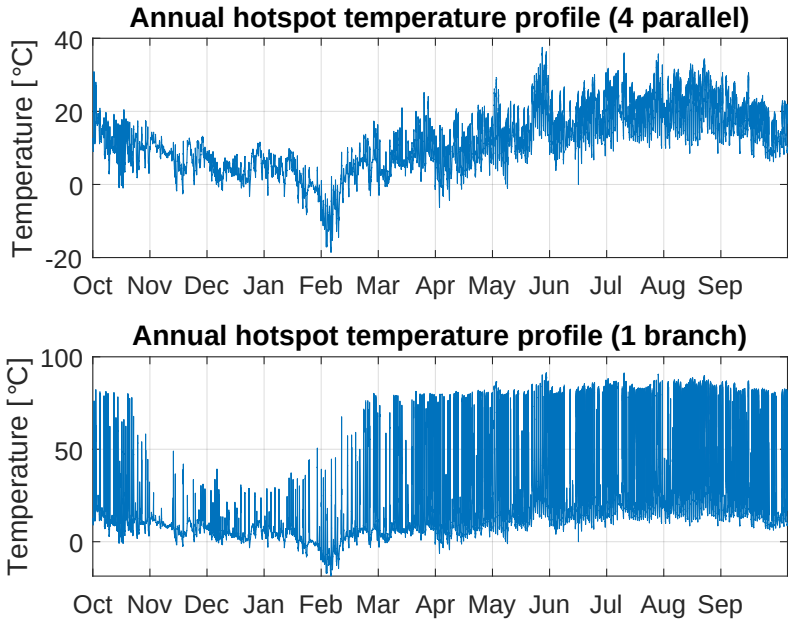


Figure 4.12: Obtained annual hotspot temperature profiles

The difference in stress caused by using different configurations is made very clear from Figure 4.12 . With the annual hotspot temperature available, the lifetime of a single capacitor can be obtained as [54]

$$L_c = L_o \cdot (4.3 - 3.3 \cdot \frac{V_o}{V_R}) \cdot 2^{\frac{T_m - T_h}{10}} \tag{4.7}$$

Where $L_o$ is the lifetime obtained when the capacitor is operated at rated voltage and at maximum hotspot temperature. $V_o$ is the steady-state operating voltage of the DC-link, $V_R$ the rated voltage of the capacitor and $T_m$ is the maximum operational hotspot temperature. The accumulated damage caused by the annual profile can be obtained by the ratio of the resolution of the mission profile and the lifetime model (4.7) evaluated at each hotspot temperature contained in the profile as [80]

$$D_A = \sum_i \frac{\mathrm{MP}_{res}}{L_o \cdot (4.3 - 3.3 \cdot \frac{V_o}{V_R}) \cdot 2^{\frac{T_m - T_{h,i}}{10}}} \tag{4.8}$$

Iterating through the entire hotspot temperature profile, the lifetime of each configuration is obtained as, operational years $= 1/D_A$ and the results are presented in Figure 4.13. As seen in the right column, a lifetime of nearly 50 years is obtained for the chosen 2 x 4 configuration, which seems like a relatively long lifetime. One of the main causes is that the global ambient temperature is used as reference temperature, when the stress related temperature increase is added. During real-life operation the power electronic components are located in an enclosure with a considerable amount of heat dissipation and the environment in which the power electronic components are located in, are in fact not the global ambient temperature but the local one in the enclosure.

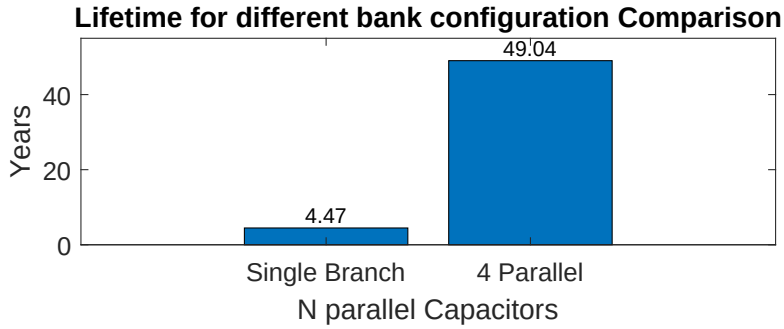


Figure 4.13: Lifetime obtained for a single branch configuration and a 2 x 4 configuration

Similar to the analysis of the IGBTs, an additional local ambient term is added to the existing model, in order to obtain a more realistic hot spot temperature profile. The contribution for the local temperature is once again proportional to the power dissipated in the capacitor, which results in the following expression for the hotspot temperature

$$T_h = T_{hc} + T_{ca} + T_{local} + T_a = P_{loss} \cdot (R_{th,hc} + R_{th,ca} + 35 \cdot \frac{1}{P_{loss,rated}}) + T_a \qquad (4.9)$$

As stated in 3.2, the chosen temperature difference is of approximately 35°, between the global temperature and the local at rated conditions. As the finite element analysis, was not conducted for this particular system, the proportional constant is chosen accordingly to the research in [65]. The thermal network with the adapted local ambient temperature contribution is shown in Figure 4.14

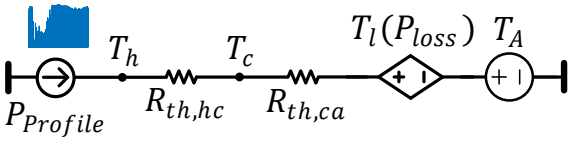


Figure 4.14: Thermal network of the capacitor including the adaptation of the local ambient temperature

Applying the annual loss profile to the thermal network the annual hot spot temperature in shown in Figure 4.15 along side the obtained lifetime when applying the annual hotspot temperature to the lifetime model (4.7).

With a lifetime of a fixed value at hand, parameter variation is taken into account by means of an uncertainty analysis.

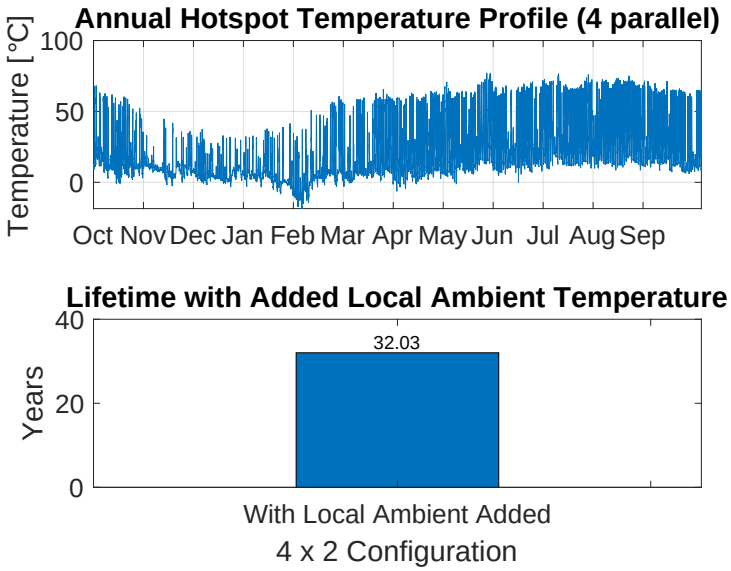


Figure 4.15: The obtained annual hotspot temperature and obtained lifetime when taking local ambient temperature into account

### 4.1.5 Sensitivity analysis and lifetime distribution

Before initializing the sensitivity analysis of the DC-link capacitor, an assumption is made that the capacitor was applied non-constant loading during the testing, which constitute the basis of the developed lifetime model. If the case was, that the lifetime model was developed under the circumstances of constant current applied through the life cycle of the testing, the increase of the ESR, caused by wear-out, would already be taken into account and there would be no reasoning for including it in the sensitivity analysis. According to [20], the ESR can double its value when approaching end-of-life, which will accelerate the wear-out of the capacitor significantly. The influence of including variation of the ESR, in terms of the parameters it will inflict, is shown in Figure 4.16

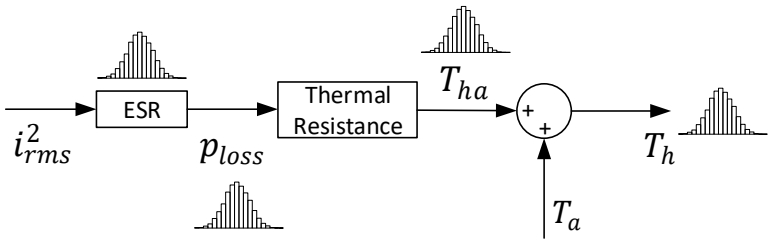


Figure 4.16: Visualisation of which parameters which will be influenced by the variation of the ESR

As shown in Figure 4.16, the variation of ESR will cause variance in the losses, which will cause variance in the hotspot to ambient temperature and in the end cause variance in the hotspot temperature. Initially the static value of the hotspot temperature will be determined from two different hotspot temperature profiles. One obtained with the rated ESR value at the beginning of operational life and one hotspot temperature profile obtained with an ESR value at the wear-out phase of the capacitor. The difference in the

two static hotspot temperature values will constitute the variance, caused by using the two different ESR values. The static equivalent of the hotspot temperature can be obtained by rearranging Equation (4.7) and the following is obtained

$$T_{h,static} = -\frac{10 \cdot ln\left(\frac{\text{length}_{mp}}{3600 L_c L_o}\right)}{ln(2)} + T_m \tag{4.10}$$

where $\text{length}_{mp}$ is the amount of temperature points contained in the annual hotspot temperature profile. The factor of 3600 is needed to convert the resulting operational lifetime in hours, which is obtained from a profile with a resolution of one second. The mean of the hotspot distribution is the static equivalent value obtained with the use of the rated ESR value and the variance is obtained from the difference of the two static values. The obtained hotspot temperature distribution and the according lifetime distribution is Shown in Figure 4.17.

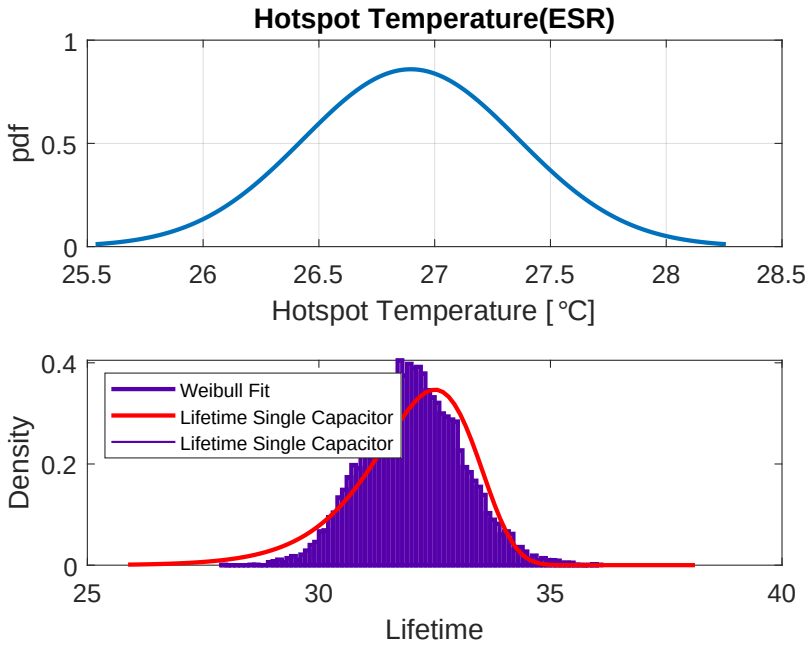


Figure 4.17: Hotspot distribution obtained by introducing variance of the ESR and the according lifetime distribution

As it can be observed from the lifetime distribution shown in 4.17, a four year range is observed within two standard deviations from the mean. Two standard deviations from the mean corresponds to a 95% confidence interval (CI) and therefore it can be stated, that as a result taking the uncertainty of the ESR value into account, the lifetime of one single capacitor is 95% certain to be within a lifetime of about 30 to 34 years. It can be argued whether or not it is valid to include variance in the lifetime model parameters due to different operation conditions, since this is exactly what the lifetime model does, it converts the rated life, $L_o$, at maximum rated conditions, into other conditions. None the less, a small variation of the rated life parameter of 2 % was include to examine the effect on the obtained lifetime. The resulting rated lifetime parameter distribution along with the corresponding lifetime distribution is shown in Figure 4.18

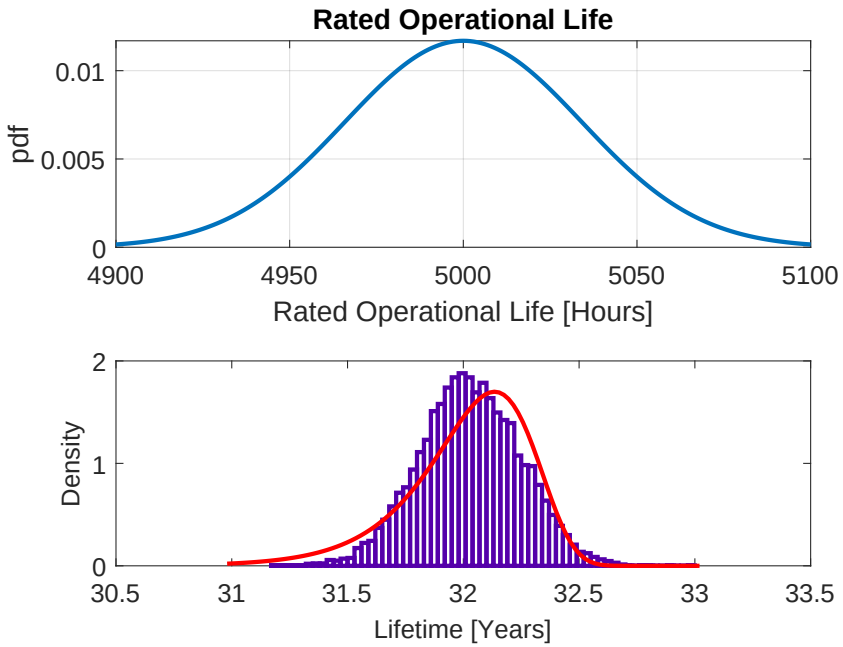


Figure 4.18: Rated life parameter distribution and its corresponding lifetime distribution

as observed in the distribution plot in Figure 4.18, the variance of the rated lifetime parameter resulted in a lifetime range of one year within a 95% (CI), which is a relatively small range and is most likely a result of choosing a conservatively variance percentage. It can be concluded, that it does have some effect on the overall lifetime. The last parameter, which is subjected to variation, is the exponential parameter which divides the difference in hotspot temperature and the maximum rated hotspot temperature.

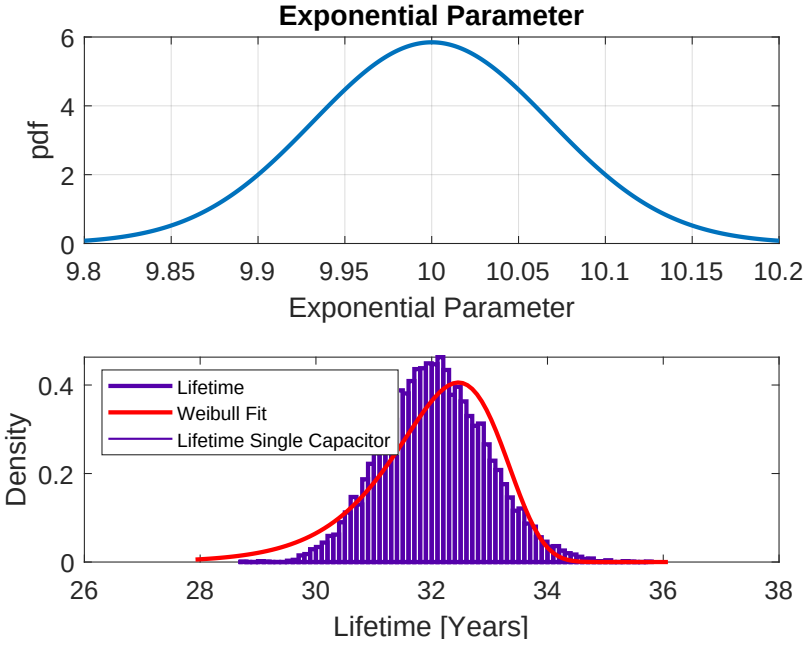


Figure 4.19: Exponential lifetime parameter distribution and its corresponding lifetime distribution

The cause for including variation, is due to different operating conditions compared to those during lifetime testing. The case of including variation to the exponential parameter, can better ba justified, as this is not a parameter, which is directly linked to the rated values used in the lifetime model. The parameter is usually fixed at a value of ten and the variation of the parameter is chosen to be at a value of 2%, which results in the parameter distribution and the corresponding lifetime distribution shown in Figure 4.19. As observed in the lifetime distribution this parameter has a significant influence on the lifetime, which makes sense, as the size of this parameter dictates how much the difference in actual hotspot temperature and the rated hotspot temperature will influence the lifetime. It can be observed that a range of four years within a 95% CI, is caused by variating the exponential parameter by only two percent. Finally, a Monte Carlo analysis is executed, where the variation of all parameters are included to obtain an overall lifetime distribution. In this case, the total variation does only include the variation in hotspot temperature caused by ESR variation and the exponential lifetime model parameter, as the author do not believe, it can be truly justified to include to rated lifetime parameter. The overall lifetime distribution and the corresponding cumulative distribution function for one single capacitor and two series connected capacitors are shown in Figure 4.20.

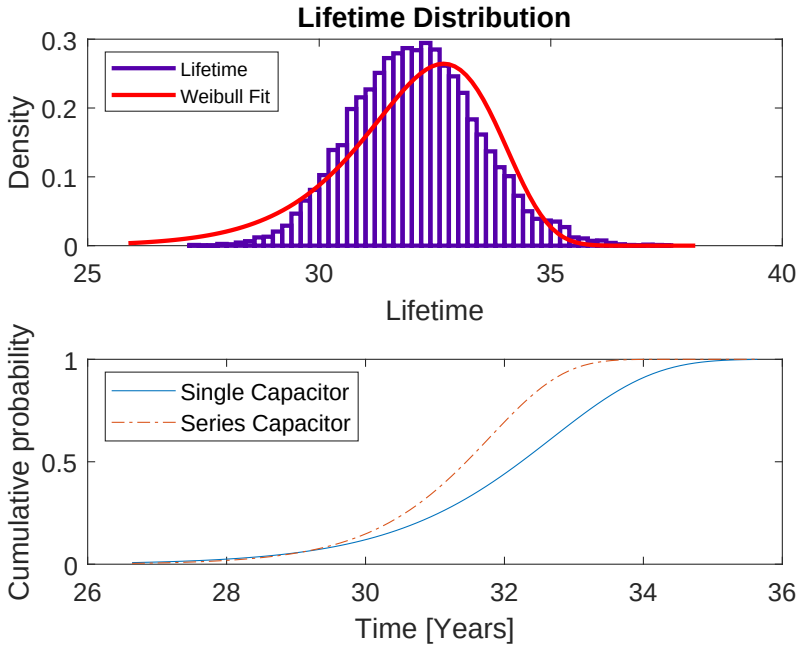


Figure 4.20: Overall lifetime distribution and its corresponding cumulative distribution functions

As it can be observed in Figure 4.20, the total lifetime distribution of a single capacitor is with 95% confidence within a range of 6 years and the $B_1$ value for both a single and two series connected capacitor is approximately 27 years, whereas their $B_{10}$ value is approximately 30 years. The obtained $B_{10}$ values will be used as part of determining the overall lifetime of the entire system in Chapter 5

## 4.2 Inherent diodes in the inverter power module

As the analysis for diodes is more or less analogous to the one carried out in Section 3.2 for IGBTs, this section will mostly consist of presenting the results obtained for the inherent diode in the inverter power module, as to avoid to present the same material twice. The aspects which differ for diodes in respect to active switches, will be pointed out and elaborated.

### 4.2.1 Power loss comparison of IGBTs and diodes

A major aspect, which can lead to lifetimes for diodes, which differs from those obtained for the IGBTs, is the losses generated in the diodes. A major difference is that the turn-on transient of diodes is very fast and efficient and the turn-on losses are therefore neglected when considering the diode losses. During turn-off transient of the diode there is generated losses due to the phenomenon known as reverese recovery, which leads to current flow in the reverse direction until the forward voltage is removed. The energy loss during turn-off can be expressed as [52]

$$E_{D,rr} = Q_{rr} \cdot V_i \tag{4.11}$$

where $Q_{rr}$ is the reverse recovery charge, which is stated in the datasheet provided by the manufacturer, $V_i$ is the diode blocking voltage during turn-off. During on-state the diode will inhibit conduction losses in the same manner as the IGBTs and the model for the diode during on-state is shown in Figure 4.21

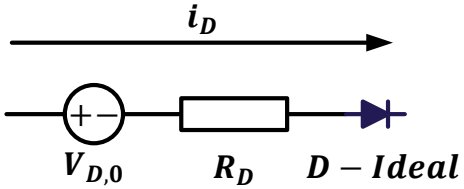


Figure 4.21: On-state diode model

which leads to the following expression for the conduction losses

$$P_{con} = V_{D,0} \cdot i_{D,rms} + R_D(T[^\circ C]) \cdot i_{D,rms}^2 \tag{4.12}$$

where $V_{D,0}$ is the forward voltage of the diode. In the same manner as for the IGBTs the datasheet information regarding the diode losses is extracted and modelled in the simulation software as shown in Figure 4.22 and Figure 4.23 respectively

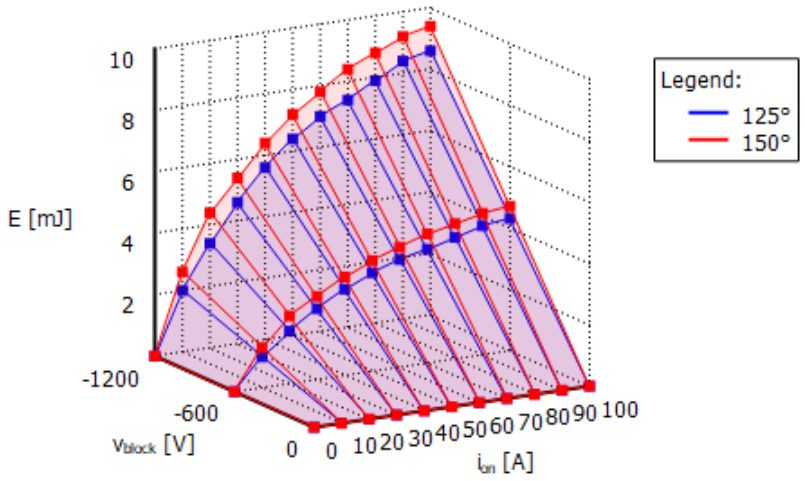


Figure 4.22: Look-up table used to obtain the turn-off energies of the diode

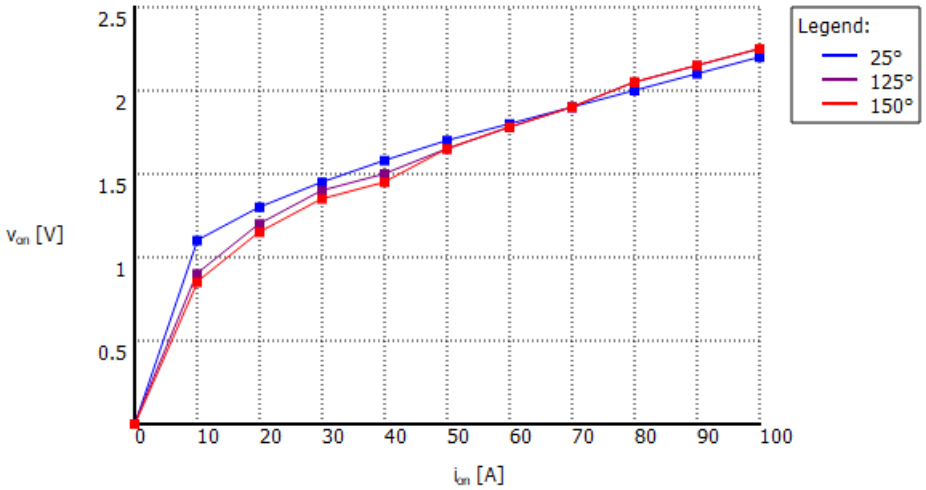


Figure 4.23: Look-up table used to obtain the conduction losses of the diode

As one half of the switching losses events is absent, in respect to the IGBTs the annual stress profile can be expected to be somewhat lower than the one obtained for the IGBTs and as the lifetime is evaluated by means of the exact same model, the lifetime of the diodes can be expected to be higher than those of the IGBTs. The losses of both devices is shown in Figure 4.24 at same operating conditions.

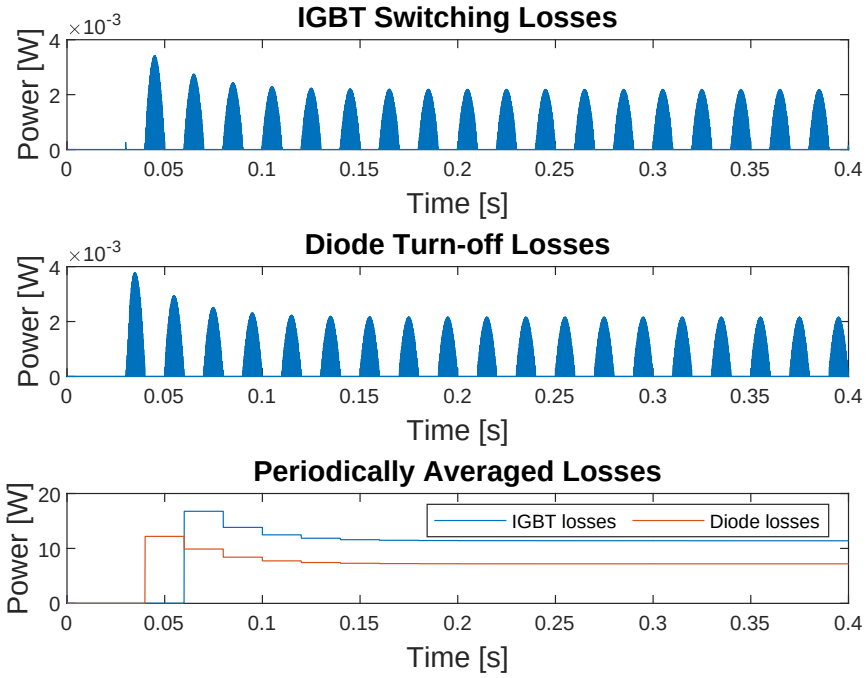


Figure 4.24: IGBT switching losses, diode Turn-off losses and the periodically averaged losses for comparison

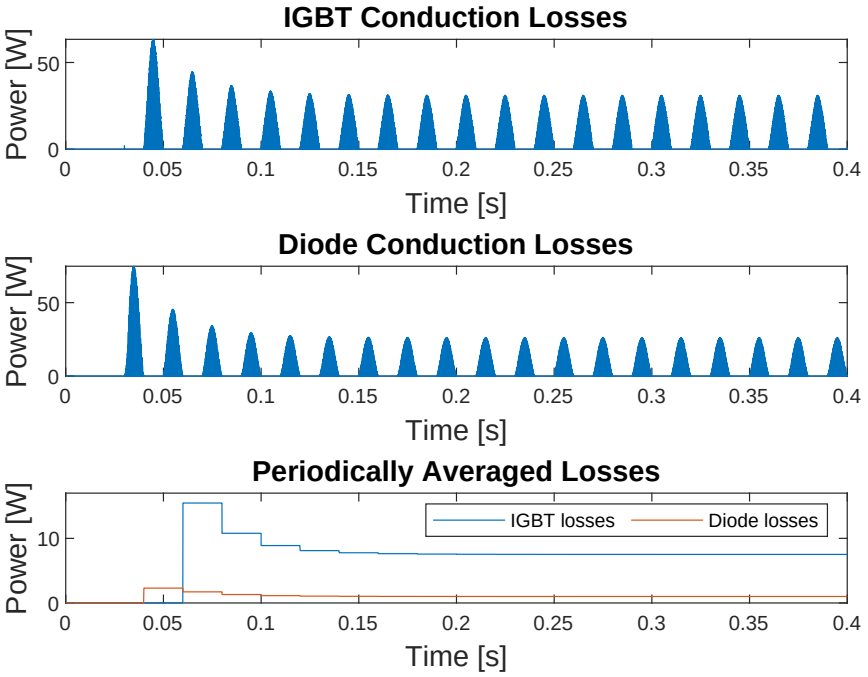


Figure 4.25: IGBT conduction losses, diode conduction losses and the periodically averaged losses for comparison

it can be observed from the bottom most plot in Figure 4.24, where the periodically averaged losses of both the IGBT and diode are shown, that the switching losses of the

IGBT is considerably higher, than those of the diode, at same operating condition. The same comparison is now done for each of the devices conduction losses as shown in Figure 4.25. As it can be observed in Figure 4.25, the conduction losses in the IGBT is multiple of the conduction losses of the diode. The thermal model from case to ambient is shared with those of the IGBT and only the thermal impedance from junction to case differs, which is extracted parameters from the datasheet of the manufacture and which are presented in Figure 4.26

| | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| R | 0.0486 K/W | 0.2673 K/W | 0.2592 K/W | 0.2349 K/W |
| τ | 0.01 s | 0.02 s | 0.05 s | 0.1 s |

Figure 4.26: Foster parameters representing the junction to case thermal impedance of the diode

The complete mission profile translation analysis, as presented in Figure 3.16, is carried out for diodes as well and the annual thermal loading profile is obtained as shown in Figure 4.27.

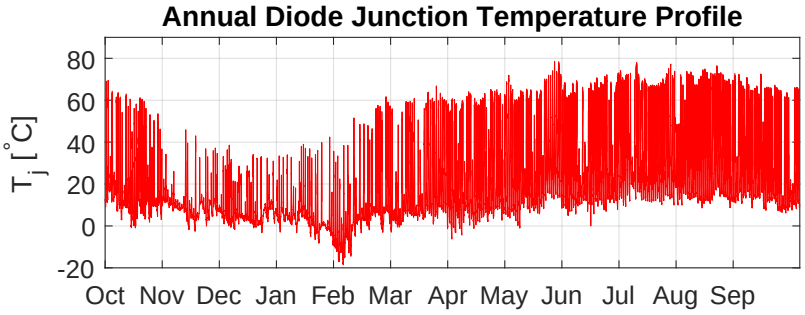


Figure 4.27: Diode annual thermal loading profile

As expected the profile is shifted to somewhat lower degrees, when compared to the annual profile of the IGBTs, which are shown in Figure 3.15. After applying the rainflow algorithm to the obtained annual profile, the stress variables was applied to the same lifetime model (3.6), as used for evaluation of the lifetime of the IGBTs. Accumulating the damage from the applied profile shown in Figure 4.27 and the obtained lifetime for a single diode is approximately 13 years, which is somewhat higher, compared to the IGBTs, as expected.

### 4.2.2 Monte Carlo analysis and B10 lifetime

Initializing the Monte Carlo analysis by once again determining the static equivalents and as the number of cycles to failure is higher than the one obtained for the IGBTs, the static equivalent values are expected to be lower. The static value of the mean junction temperature, $T_{j,mean,static}$ is 38.46°C and the static value of the junction temperature fluctuation, $\Delta T_{j,static}$ is 37.16 °C. The parameters, which are modelled as distribution functions are exactly the same as for the IGBTs and a sensitivity analysis, of how much influence each parameter has on the lifetime, will therefore not be presented again as only

the mean values of the distribution functions will differ. Instead, the analysis will only include the overall lifetime distribution and the according cumulative distribution function, which are both shown in Figure 4.28

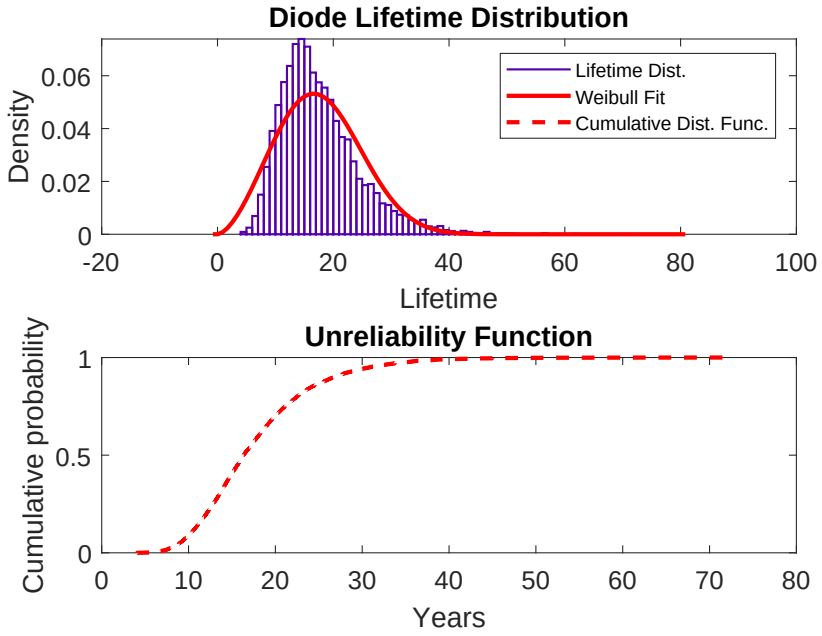


Figure 4.28: Diode Lifetime Distribution and Cumulative Distribution Function

Observing the unreliability plot in Figure 4.28, it can be seen that a $B_{10}$ of 10 years was obtained for the diodes, which as expected, was higher compared with those of the IGBT. The obtained $B_{10}$ value will be used to obtain an overall system lifetime in chapter 5.

## 4.3 Chopper diode in the DC/DC stage

As every aspect concerning the lifetime estimation of diodes has been explained in the previous section only the loading profile and lifetime distribution will be presented for this particular diode. The annaul loading profile, obtained by means of the previously explained mission profile analysis, is shown in Figure 4.29

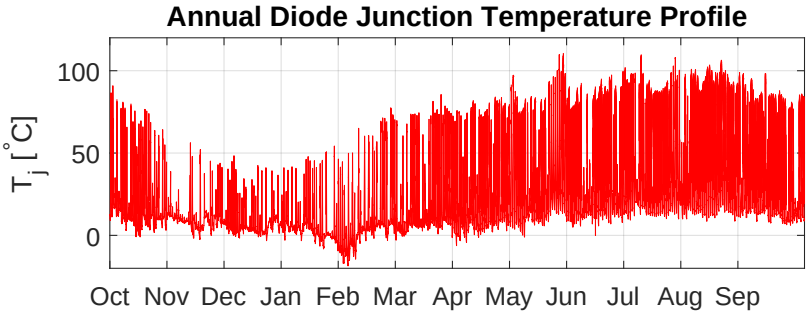


Figure 4.29: Diode annual thermal loading profile

As it can be observed in Figure 4.29, the thermal stress is significantly higher, than the stress which the diodes in the DC/DC stage are subjected to. The thermal loading profile is even more aggressive than the ones for active switches in the DC/AC stage even though the diode was shown to inhibit lower total losses. Executing the exact same Monte Carlo analysis as for previous diode, the lifetime distribution and the according cumulative distribution function shown in Figure 4.30 are obtained

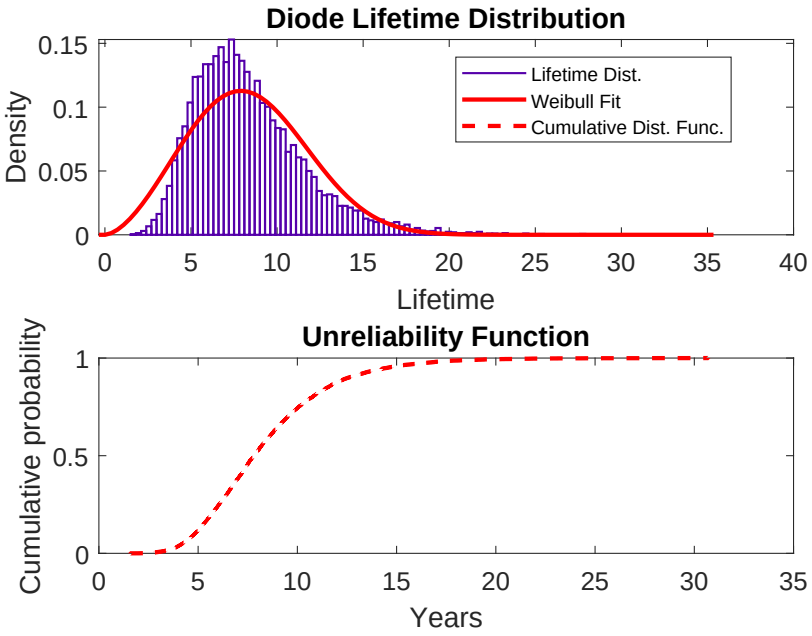


Figure 4.30: Diode Lifetime Distribution and Cumulative Distribution Function

The trend of the components of the DC/DC stage having a shorter lifetime is also reflected through the obtained lifetime of the chopper diode used in the boost converter. The obtained probability of failure function will be used to obtain an overall system lifetime in chapter 5.

# System Lifetime Assessment 5

***In this chapter the the overall lifetime of the entire system will be determined. This is done by means of considering each components individual unreliability functions and combine each of them mathematically with the aid of reliability block diagram analysis until an system unreliability function is obtained.***

The impact of the failure of each of the systems components is now required to be taken into consideration, as the impact of their respect failure will influence how each of these component are connected in the reliability block diagram. If the failure of either component will lead to failure of the system, the individual components will be connected in series as shown in Figure 5.1

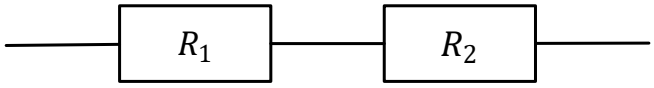


Figure 5.1: Reliability block diagram series connection

The reliability of a series connected system is the combined probability of no failure of either component and which can be described as the product rule

$$R_{system} = \prod_{i=1}^{n} R_i \tag{5.1}$$

As we are dealing with unreliability and not reliability a substitution of the following is needed

$$F = 1 - R \tag{5.2}$$

and the probability of failure for a series connected configuration can be expressed as

$$F_{system} = 1 - \prod_{i=1}^{n} (1 - F_i) \tag{5.3}$$

In case of active redundancy, where the system is able to operate if either or both components function, the reliability blocks are connected in parallel as shown in Figure

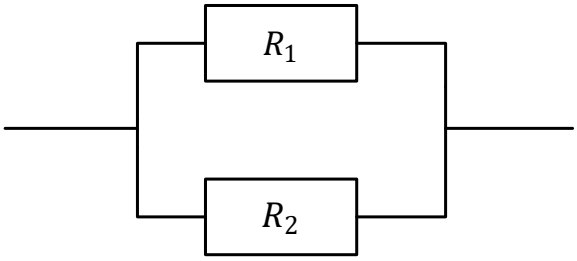


Figure 5.2: Dual redundant reliability block diagram configuration

The general reliability expression for active parallel redundancy is

$$R_{system} = 1 - \prod_{i=1}^{n}(1 - R_i) \tag{5.4}$$

considering the unreliability of a redundant configuration is simply the product of each failure probability

$$F_{system} = \prod_{i=1}^{n} F_i \tag{5.5}$$

Initially the unreliability of each stage will be determined and then the DC/DC stage, the DC-link and the DC/AC stage will be treated as a 3-block series connection, which will provide the unreliability function of the entire system.

## 5.1 Lifetime estimation of the DC/DC stage

The two components, which constitute the reliability analysis of the DC/DC stage, is the IGBT and the chopper diode, which is both integrated in the same power module. As the failure of either the IGBT or the diode will compromise the functionality of the DC/DC stage the overall failure probability is determined by considered the components to be connected in series and determined by the use of Equation (5.3) as

$$F_{dcdc} = 1 - F_{IGBT} \cdot F_{diode} \tag{5.6}$$

The individual unreliability functions are shown along with the unreliability function of the DC/DC stage in Figure 5.3

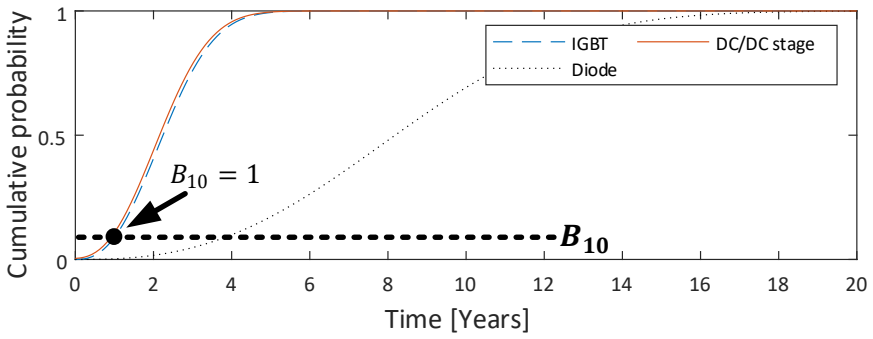


Figure 5.3: The unreliablity functions of the IGBT, diode and the entire DC/DC stage

As shown in Figure 5.3, the $B_{10}$ value for the DC/DC stage is one year, which is a result of having two components with individually relatively low $B_{10}$ values.

## 5.2 Lifetime estimation of DC-link

In section 4.1 the probability of failure for one single branch, consisting of two series connected capacitors, was obtained. The capacitor bank was designed to include 4 parallel branches in order to achieve a proper ripple current capability. If either of these branches will fail the DC-link will still be functional but the wear out of the remaining branches will accelerate due to each of the remaining branches are handle more ripple current. The failure of one branch will therefore also lead to changes in the failure probability of the remaining capacitors. The change of failure probability if failure occurs will not be into consideration and as the DC-link will be able to function with only one branch, m-out-of-n redundancy will also not be necessary to include. Instead general active redundancy will applied for the four capacitor branches in the DC-link and they will therefore be treated as parallel connections as shown in 5.2. The probability of failure for the DC-link be expressed by use of Equation (5.5) as

$$F_{dclink} = \prod_{i=1}^{4} F_{branch,i} \tag{5.7}$$

The obtained unreliability function for DC-link is presented along with the unreliability of one single capacitor branch in Figure

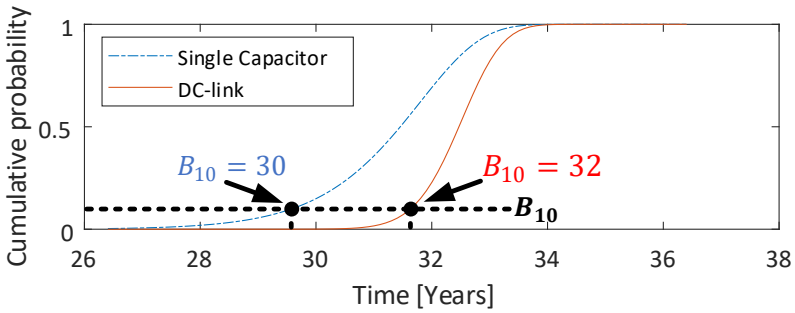


Figure 5.4: The unreliablity functions of one single capacitor branch and the DC link

It can be observed from Figure 5.4 that introducing redundancy in the system improves the reliabity, as the $B_{10}$ value of the entire is higher than the $B_{10}$ one single capacitor branch. A $B_{10}$ value of approximately 32 years was obtained for the DC-link.

## 5.3 Lifetime estimation of DC/AC stage

The DC/AC consists of six active switches with a antiparallel diode connected to each of them. If either one if the switches or diodes fail, the inverter will no longer be able be to generate its desired output. Since the inverter losses its function of one single components fails, all individual components are connected in series when obtaining the failure probability of the DC/AC stage. It is chosen to obtain the failure probability of

the entire module by the product of the failure probability of the six active switches and the failure probability of the six diodes as shown in Equations (5.8),(5.9) and (5.10)

$$F_{IGBTs} = 1 - \prod_{i=1}^{6} F_{IGBT,i} \tag{5.8}$$

$$F_{Diodes} = 1 - \prod_{i=1}^{6} F_{diode,i} \tag{5.9}$$

$$F_{dcac} = 1 - F_{IGBTs} \cdot F_{Diodes} \tag{5.10}$$

Alternatively the failure probability product of one switch and one diode could be determined and thereafter consider six combined switches and diodes to obtain the probability of the module. Using the strategy explained, the failure probability functions of one single IGBT, one single diode, six IGBTs, six diodes and the entire DC/AC stage is shown in Figure 5.5

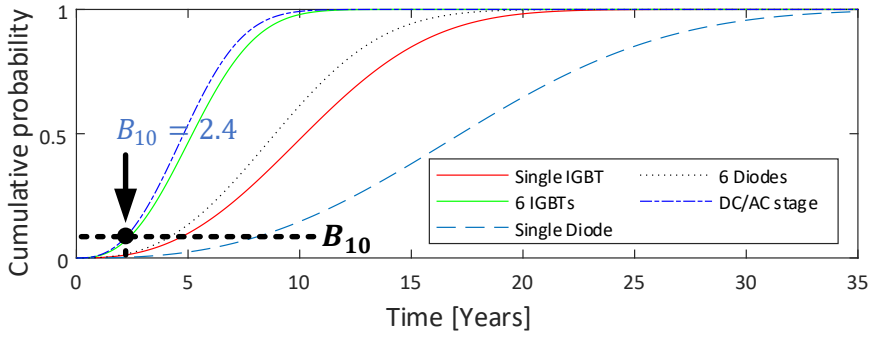


Figure 5.5: The unreliablity functions of one single IGBT, one single diode, six IGBTs, six diodes and the entire DC/AC

The obtained $B_{10}$ value of the power module, including all six active switches and six antiparallel diodes, is approximately 2.4 years.

## 5.4 Lifetime estimation of the system

Finally, the reliability function of the entire system can be determined as the failure product of each and the dc-link, as the failure of either will result in the systems loss of function. Obtaining the failure probability as the product of each stages, the unreliability function of the system is obtained as shown in Figure 5.6

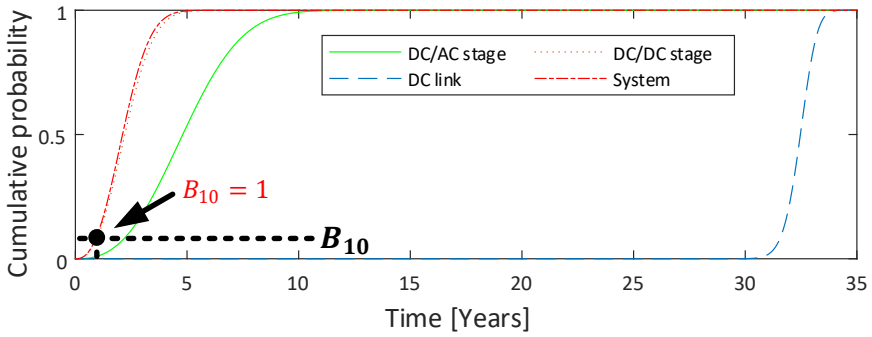


Figure 5.6: The unreliablity functions of the DC/DC stage, the DC-link, the DC/AC stage and the entire system

It is clear from Figure 5.6, that the lifetime of the system is dictated by the reliability of the DC/DC stage, as this is the subsystem which is least reliable. Combining the three subsystems failure probability functions results in a system lifetime of one year, as was the case with the DC/DC stage. The obtained $B_{10}$ values of the system is summarised in Table 5.1

| Obtained $B_{10}$ values | |
|---|---|
| Single IGBT DC/AC stage | $B_{10} = 5.2$ years |
| Single diode DC/AC stage | $B_{10} = 8.7$ years |
| Inverter Power Modules | $B_{10} = 2.4$ years |
| DC link capacitor bank | $B_{10} = 32$ years |
| IGBT DC/DC stage | $B_{10} = 1$ years |
| Diode DC/DC stage | $B_{10} = 4$ years |
| Power module DC/DC stage | $B_{10} = 1$ years |
| PV-inverter | $B_{10} = 1$ years |

Table 5.1: Obtained $B_{10}$ values from the reliability analysis

# Experimental work 6

***This chapter presents the laboratory implementation of the three-phase two-level voltage source inverter. It is worth to mention that the simulation of the inverter presented in previous chapters is not identical to the test bench prototype as well as the controller parameters, which have been considered in the laboratory setup***

A laboratory test-bench was developed, which enables the possibility of measuring the junction temperature of the power device, which are subjected to an one day mission profile. In regards to the system ratings used in the project, the system ratings of the used prototype is different and as listed in Table 6.1

| Parameters of the PV-inverter used in the test bench | |
|---|---|
| Rated power of the PV array $P_{pv}$ | 2500 W |
| Rated output current $I_{mp}$ | 30 A |
| DC link voltage $V_{dc}$ | 600 V |
| DC link capacitance $C_{dc}$ | 340$\mu$F |
| Filter inductance $L_{filter}$ | 2.5mH |
| Resistive load $R_{load}$ | 16.5$\Omega$ |
| Switching frequency $f_s$ | 10kHz |
| Fundamental frequency of the output current $f_g$ | 50Hz |
| Ambient temperature $T_a$ | 25°C |

Table 6.1: Electrical characteristics of the test bench

The power device in the prototype is the same 1200V/50A three-phase IGBT module from [31], as used in the analysis throughout the report and which is shown in Figure 6.1. As observed in the Figure, the print circuit board of the hardware prototype is custom made, which provides direct access of the IGBT chip and the junction temperature can therefore be measured by means of optic fiber, during the real-field mission profile operation.

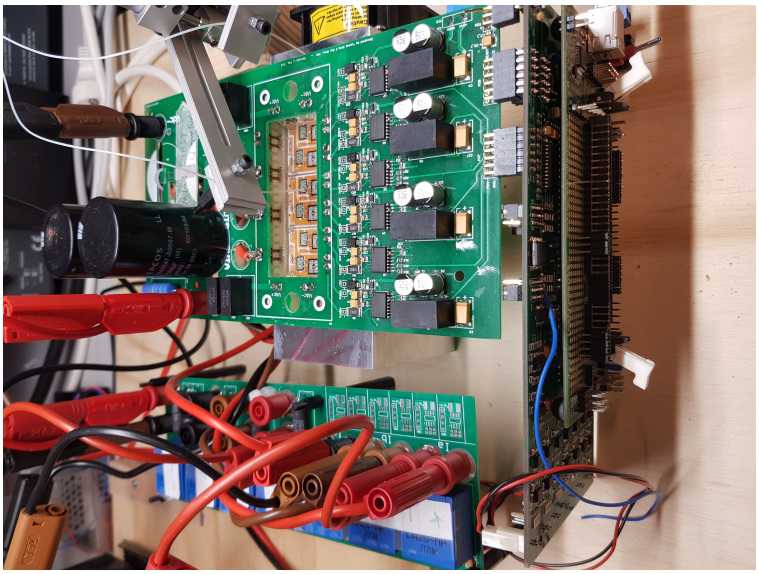

Figure 6.1: Hardware prototype of the PV inverter test-bench

As discussed in Section 3.2, the thermal stress is highly dependent on the loading dynamics and in order to demonstrate the impact of mission profile dynamics on the thermal stress, a real-field mission profile is subjected to the test bench prototype and the thermal stress profile shown in in Figure 6.2 is obtained

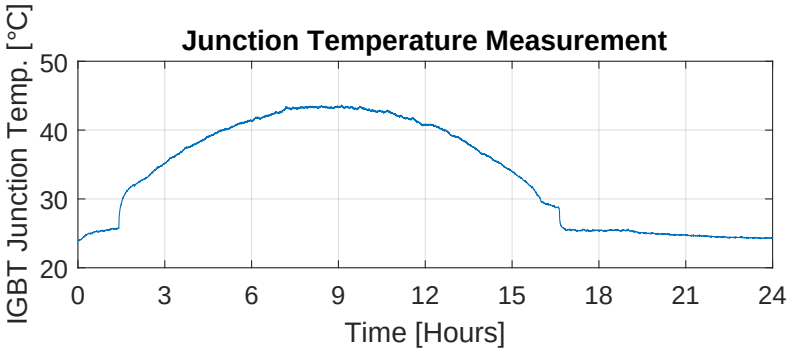


Figure 6.2: Junction temperature measure of IGBT chip, when subjected to a one-day mission profile

From the stress profile shown in Figure 6.2, it can observed that the thermal dynamics replicates the tendency of the loading profile, which is presented in terms of maximum power, maximum voltage and maximum current, shown in Figure 6.3

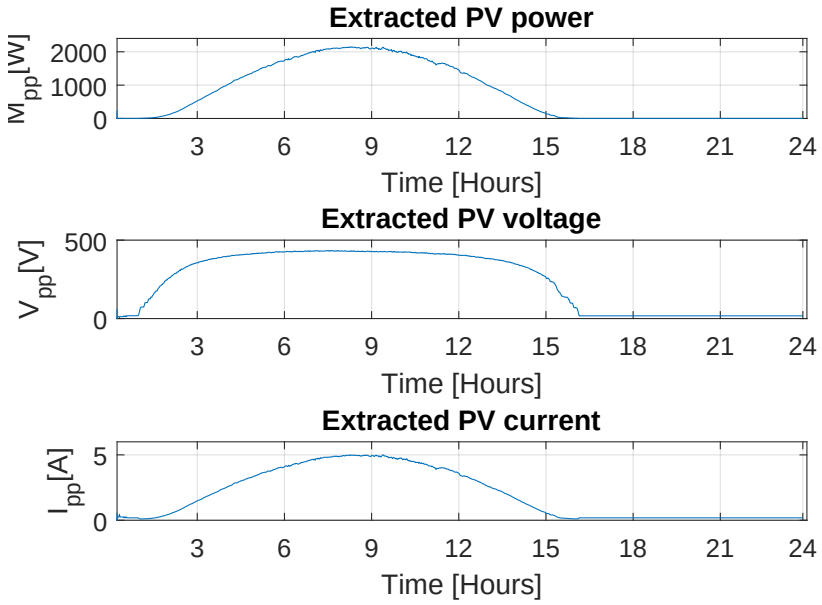


Figure 6.3: Maximum power, voltage and current extracted from the PV-array

For further work it could highly relevant to compare the present experimental results, with the mission profile modelling, as was presented in Section 3.1.1. It would also be relevant to compare multiple configurations of the thermal models, with the experimental results, this would provide the knowledge of how much accuracy is lost when using steady-state models, which is only based on thermal resistances. Steady-state models are often used when dealing with long-term stress profiles for the sake of their convenience. There is no doubt that stedy-state models are capable of capturing the slow dynamics of temperature change whereas solar irradiance can change abruptly due to shifting in cloudy weather. Additional to validating different thermal models with the obtained experimental data, it would also be relevant to examine how each of these models perform under different mission profile resolutions and under different data sampling frequencies.

# Conclusion and Discussion 7

### 7.0.1 Achieving the pre-specified project objectives

The main objective of this project was to estimate the lifetime of a two stage PV-inverter when the system was subjected to a real-field loading mission profile. The desired outcome of conducting such analysis, was to be able to identify the critical components in terms of reliability.

- Initially, each part of the system was modelled with great detail, which enabled the possibility to control the stress applied to each of the systems components and thereby being able to replicate the stress, which was dictated by the real-field mission profiles.
- Each component contained in the system was subjected to state-of-the-art reliability modelling in terms of translating the real-field mission profiles and in terms of the analysis concerning the wear-out, which resulted in the knowledge of the lifetime consumption due to long-term operation. The challenging points, which led to assumptions, was highlighted along the progress of the report, such as stating assumptions regarding the heatsink thermal impedance and the temperature contribution from the power electronic being located in protective enclosure.
- Additionally large efforts was made to include all the relevant uncertainties for each individual component by means of including electrical parameter variation and the highly influential variation of the lifetime model parameters. Including the uncertainties lead to lifetime distributions, which is a large improvement in lifetime estimates when compared to single value estimates which only occurs in ideal cases.
- The design for reliability aspect was included in the analysis it terms analysing different subsystem configurations, which could lead to improved reliability. Different DC-link configurations was examined in order to improve the lifetime, while still considering the issues related to having a bank configuration consisting of a large number of capacitors

The lifetime distributions and unreliability functions of each individual components was used to obtain the distributions and unreliability of the subsystems by use of statistical theory. Finally, each subsystem was used to determine the lifetime distribution of the entire system.

From carrying out the reliability analysis, it can be concluded that the most critical components are the active switches, namely the one being part of DC/DC stage. By reaching this conclusion, there are some issues which could inflict the outcome and which needs to be discussed.

### 7.0.2 Discussion

There are a few factors, which could have a significant influence on the obtained outcome. First is the method of how the lifetime model parameters was obtained, which was conducted by means of fitting the experimental lifetime data provided by the manufacture. Loosing only slightest precision when extracting the data points, which are used to determine the lifetime parameters, will have a significant influence on the outcome of the lifetime model. As shown in sensitivity analysis, performed in Section 3.1.3, the exponential parameter, which is linked to the junction temperature variation has a large influence on the obtained lifetime and even a small change of this parameter results in very different outcomes.

The obtained lifetime model parameters was compared with some from the literature, which are used as reference in this project and the parameters used in this particular case was somewhat aggressive when compared to others, which could be the main cause of the relatively low lifetime estimations obtained in this project. Still the purpose was to identify the critical components and therefore should the lifetimes not be considered for their absolute values but how the lifetime of each component is relatively to each other. The outcome of their relative values is a fully valid result, as these component, with the exception of the DC-link capacitor, is evaluated with the use of the exact same lifetime model. It is therefore valid to compare the lifetime of the active switches and the diodes whereas the comparison of the lifetime of the DC-link capacitor with the remains of the system components.

As previously stated, the analysis revealed that the components in the DC/DC stage was subjected to a higher stress when compared to the ones in the DC/AC stage. One of the possible main causes, is that the active switch and the diode in the DC/DC stage are subjected to all the transferred energy whereas the loading is distributed among all six power devices in the DC/AC, during a full fundamental period. Another possible cause for the shorter obtained lifetime at the DC/DC stage is that, even though the module was chosen with a margin with respect to the maximum loading condition, the margin of the DC/DC module was not nearly as big as the margin, which was available with the chosen module in the DC/AC stage. Also the thermal resistance of the power module, used as realisation of the boost converter, was twice the value of the thermal resistance of the power module of the inverter. As the two stages shared the external thermal network, a higher junction to case thermal impedance of the DC/AC module will lead to higher thermal loading.

In terms of the obtaining the stress, the mission profile translation analysis used in this project was thorough and detailed. Yet one major factor, which could be a source of error, is the assumption of the thermal impedance case to ambient. A finite element analysis, would have provided the actual thermal impedances and would have been a large improvement of the thermal-electro modelling part. With respect to the translation of the operating conditions to annual profiles, the use of linear interpolation is fully justified, as an extensively amount of operation conditions was used in this project, namely 11 different solar irradiance intensity each at 13 different temperatures. The adopted method is precise but also extremely time consuming in terms of simulation hours.

Finally, more work could have been put into comparing different module solutions at each stage, but as this is already a comprehensive project, it was chosen not to be included.

### 7.0.3 Further work

- Extend the analysis to include several generation units, which should consist of both wind generation and solar generation. The extended analysis should merge the power electronic reliability concepts with those of power system reliability and should also include the phenomenons which are related to having parallel converters in one system. The CIGRE LV distribution network, which is shown in Figure 7.1, could be an obvious case for conduction such analysis, as it consists of several different generation and storage units.

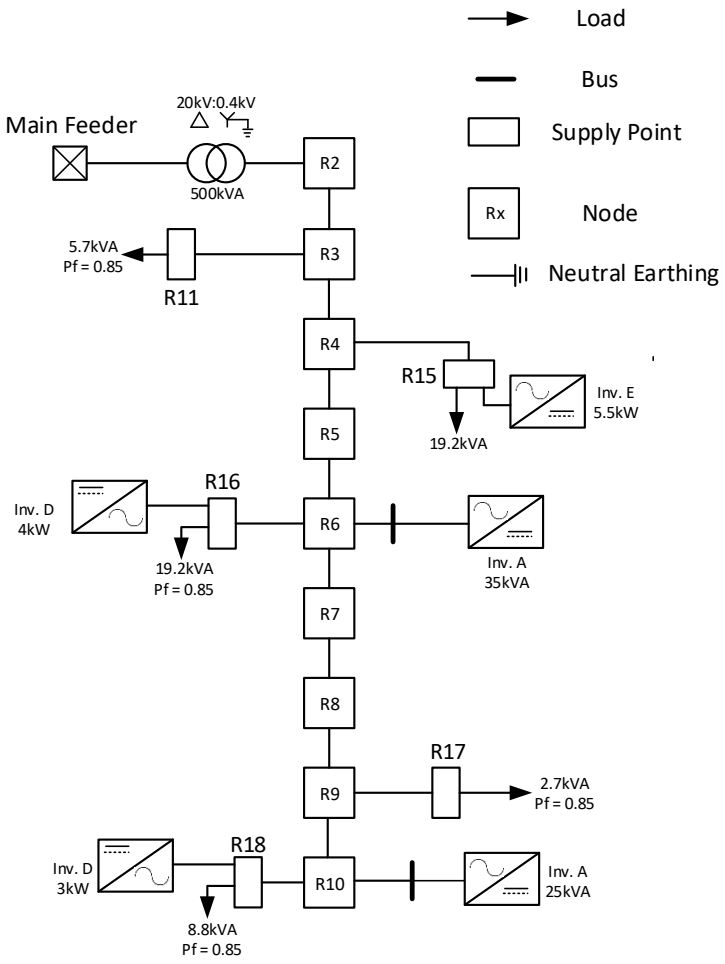


Figure 7.1: CIGRE LV distribution benchmark network 7.1

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