Insulation Evaluation in a SiC Power Module via Electric Field Simulation and Partial Discharge Measurement

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Abstract:

Silicone carbide (SiC) wide bandgap (WBG) materials are one of the most promising solution to reduce the size and weight of the power semiconductor modules. Such modules are able to tolerate high voltages and currents, temperatures and switching frequencies. One of the high voltage applications (10 kV) that they are envisoned to be widely used in the future is railways. However, the high operating voltage can be an obstacle for using WBG-based power modules. The increased blocking voltage enhances the local electric field that may become large enough to induce partial discharges (PDs) within the SiC module. High PD activity accelerates the ageing of the insulating silicone gel, shortening the lifetime of the whole module dramatically. In this study, the electrical insulation of 1.2 kV SiC MOSFET module has been evaluated. In FEM simulation the highest electric field strength was seen at the interface between the silicone gel and the metalized ceramic. PRPD measurements showed that a surface discharge was likely to occur at this point. Lastly, the electric field control methods in the SiC MOSFET module were proposed.

Contents

Nomenclature

Abbreviations

$a-Si$	Amorphous silicon
AC	Alternating current
Al_2O_3	Alumina
AlN	Aluminum nitride
CC	Connecting cable
CD	Coupling device
DC	Direct Current
DIV	Discharge Inception Voltage
$E-field$	Electric field
FDC	Field dependent conductivity
FDP	Field dependent permittivity
FEM	Finite element method
HV	High voltage
IEC	International Electrotechnical Commission
$IGBT$	Insulated Gate Bipolar Transistor
MI	Measuring instrument
$MOSFET$	Metal-Oxide-Semiconductor Field Effect Transistor
OL	Optical links
PD	Partial Discharge
$PDIV$	Partial Discharge Inception Voltage
$PRPD$	Phase-resolved Partial Discharge
PWM	Pulse Width Modulation

Si	Silicon
SiC	Silicon-Carbide
WBG	Wide bandgap

Chapter 1

Introduction

1.1 Problem introduction

The evolution of power electronics technology has always moved toward higher electrical energy efficiency, higher power density and improved reliability. In this undergoing dynamic evolution power semiconductor devices play a crucial role [1],[2]. Almost all power devices are manufactured utilising silicon (Si). However, Si power devices have approached the theoretical limitations of their performance [1],[3]. For example, the maximum blocking voltage of the IGBT is 6.5 kV, whereas the power MOSFET is rated for blocking voltages up to 600 V. Moreover, the switching speeds of IGBTs are relatively slow, limiting them to lower switching frequency applications [1]. Thus, semiconductors having better properties than Si are required. Silicon carbide (SiC) is one of the most promising semiconductor material for the next-generation power devices, that will replace conventional silicon based semiconductors [3]. One of the high voltage applications (10 kV) that SiC modules are expected to be used in is railways. As a wide bandgap (WBG) material, SiC has higher blocking voltage capability, higher temperature tolerance, and higher switching frequency than Si technology [2]. 4H-SiC material has about 3 times wider energy bandgap and around 10 times larger electric breakdown field, comparing with Si. Due to that the drift region distance of 4H-SiC power devices can be made shorter than that of Si ones having the same blocking voltage. Therefore, the resistance of the drift region, which is on-state resistance, gets smaller. The smaller on-state resistance enables the SiC chips to be smaller. Furthermore, the dopant concentration in drift region of SiC devices is much higher compared to Si devices [1],[3]. All these properties indicate that the packaging dimensions of SiC devices can be reduced significantly. Whereas the 15 kV blocking voltage of SiC IGBT is 2.3 times higher than Si IGBT (6.5 kV), its volume is one-third that for the Si IGBT [4].

Nonetheless, this causes local electric field (E-field) concentration inside the SiC module. The high magnitude of E-field may initiate partial discharge (PD) within an insulation system of high voltage WBG modules. There are two common insulating materials used in power modules such as soft dielectric silicone gel and solid ceramic substrate, which is most likely aluminum nitride (AlN) or alumina (Al_2O_3). The silicone gel is used to encapsulate the whole module to prevent electrical discharges in air and to protect substrates, semiconductors, and connections against dirt, humidity, and vibration. The ceramic substrate ensures electrical insulation between the die and the baseplate, which is ususally grounded. The critical region inside the power module is the silicone gel close to the sharp edges of copper metallization as can be seen in Figure 1.1 [2],[4].

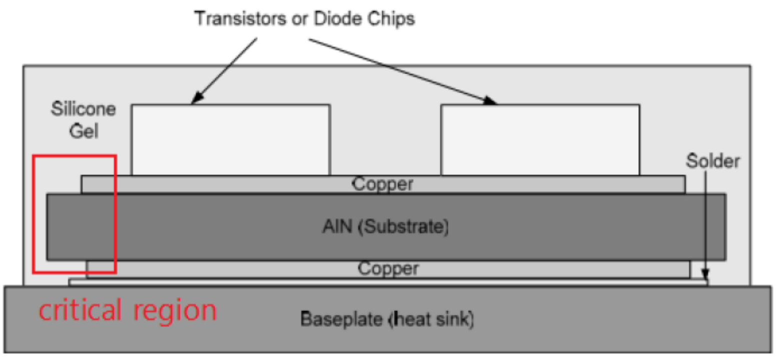


Figure 1.1: Cross-section view of typical power module [5]

Repetitive and intensive PD destroys the silicone gel. This leads to electrical insulation failure and reduces the reliability of the SiC module in the long term. Therefore, the electric field distribution in SiC modules must be evaluated carefully and PD caused by local electric field enhancement must be monitored and controlled. In this project, the SiC MOSFET module which is rated at 1.2 kV and 55 A is taken as a study case.

1.2 State of the art

1.2.1 Partial Discharges

Partial discharge, PD in short, is an insulation concern which should be considered by designers and operators of power modules. Understanding of partial discharge behavior of power modules are important in order to properly evaluate the insulation level of the module. A detailed evaluation of the insulation level in insulated gate bipolar transistor (IGBT) was presented in [6], where PD measurements from three different 3.3 kV IGBTs were conducted using the normalized method from standard IEC 60270 and a proposed improved measurement method. For both evaluation methods, focus is mainly set on measuring the Discharge Inception Voltage (DIV) to evaluate the insulation of the power module, as this phenomenon is the main cause of module/inverter failure [6]. The two possible origins of PDs are: the packaging and the die itself [6]. A volume/void discharge can either appear in the ceramic substrate, or the gel. Volume discharges appear in voids such as gas bubbles. When filling the power module with silicone gel, air bubbles and voids may be formed at the interface between the metallization-substrate and the gel bulk, if the degassing process is not enough. PD might be triggered from these voids and air bubbles in the form of surface discharges, which occur at the edge of the metallization areas at the metallization-substrate interface. Corona discharges can occur at sharp edges, either on the high voltage or earthed potential side.

1.2.2 PD measurement

The normalized test recommends applying AC voltages between the module's base plate and the three electrical connections (emitter, gate and collector, for an IGBT) shorted together. This method doesn't represent the real stresses endured during normal operation [6], as the test setup only considers sinusoidal waves of 50 HZ, whereas the power module withstands several kHz during normal operation. A new test proposition is necessary, because of the limitations of the normalized test. The proposed test PD detection circuit is the same as in the normalized test. The difference is the applied voltage waveform to the test object. In the normalized method, a 50 Hz voltage is applied, but the improved method applies, as stated in [6], a 50 Hz AC voltage combined with a DC voltage, so the resulting Voltage is $V_{AC} + V_{DC}$ [6]. One of the important findings from this paper, are the low DIV observed using the proposed new test, and signals were detected for voltage values which were lower than the rated ones [6]. Paper [7] found a similar conclusion using a proposed test by their own. The standard test setup, from standard IEC 60270, was realized by supplying the test object with a 50 Hz sinusoidal waveform with voltage rms values increased in steps, according to the IEC procedure. The proposed new test setup in [7] was performed with a 50 Hz PWM modulated sinusoidal waveform, with voltage rms values increased in steps, according to the IEC procedure, but was obtained by modulating a PWM signal with 1 kHz carrier frequency.

Because of the higher frequencies applied to the test object, more intensive PD activity was expected. PWM stress emulates the real IGBT operating conditions. The discharge inception voltages for the same test object, using a sinusoidal wave vs. a PWM pattern, were different, partly due to the PWM signals having multiple positive and negative crest values in one period of the sinusoidal wave. For the same DIV for the PWM setup, no PDs were observed in the standard IEC setup [7].

1.2.3 Simulations

Measuring PDs using a lab setup is a commonly used method, for evaluating the insulation level of a power module. Apart from this method, high electric fields can be localized using a FEM simulation software. When simulating the electric field strength in a power module, inherent problems arise, such as:

- The electric field strength calculated at perfectly sharp edges are infinite [8], and good techniques should be implemented to avoid this problem.
- The electric field strength is evaluated based on the mesh size in the simulation. A very fine mesh is more accurate than a big mesh.

Paper [9] focuses on making a mesh-independent electric field strength simulation, while also simulating electric field strengths during electric transients. A common practice, to accurately simulate electric field strengths on the edges of the metallization on the ceramic substrates, is to simplify the model, or "zoom in" to the critical area. This is generally done to minimize simulation time and computing power. The paper also analyzed physical and geometrical variations, which could impact the electric field strength in the simulations, the geometrical variations are shown in Figure 1.2 [9].

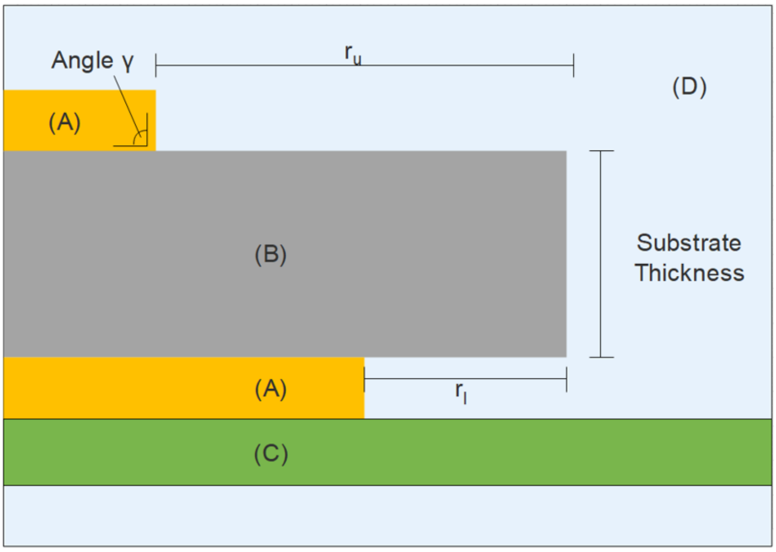


Figure 1.2: Rim section of the critirical area, of a typical power module. (A) is the copper mettalization, (B) is the ceramic substrate, (C) is the baseplate and (D) is the silicone gel [10]

To reduce the maximum electrical field magnitude of the power module, some improvements could be made by varying the following parameters:

- Increasing the thickness of the ceramic substrate layer, from 1 mm to 2 mm, and it led to an electric field reduction of 30 %, according to [10].
- Increasing the angle γ so the compression of potential lines around the edge decreases, and the electric field strength in the substrate-metallization boundaries decreases.
- Normally, the distance from the metallization to the rim is 2 mm on the top of the ceramic and 1 mm on the bottom. Offset is calculated as following:

$r_{off} = r_u - r_l$. By setting the offset to -0.9 mm, the max electric field value is found, and is decreased by 70 %, comparing to standard power modules [9].

- It helps when filling the region around the triple point, with a material with a similar permittivity as the ceramic substrate.

1.2.4 Optical Imaging

The simulated electric field strengths, can be verified by localizing PDs, using optical imaging techniques. Paper [11] focuses on finding the origins of partial discharges in IGBT modules. This was done by observing PDs, using optical imaging, while stressing the test object. This was done in a dark room by using a photocamera with a sensitive film. Optical imaging, simulations and PD spectroscopy of IGBTs rated at 6.5 kV were performed, and this was done according to standard IEC 1287 [11]. It was found that the PDs occurred in the triple point, along the copper rim between the substrate and the silicone gel. The PDs did not occur homogeneously/uniformly, but rather at a few distinct locations. This was due to imperfect etching at the rim of copper metallization. The influence of the shape of the ceramic was very pronounced. Solder residues were found to be a source of PDs at lower voltages, around 5 kV. The type of silicone gel and its curing conditions had a slight influence regarding PDs [11]. The shape of the edge of the ceramic metallization had a much greater influence. A PD spectrograph was measured at different voltages starting at 3 kV to 7 kV. The PDs were strongly dependent on the voltage magnitudes, and the phase of the PDs weren't constant, meaning different types of PDs were happening at different voltage levels [11].

1.2.5 Effective factors on E-fields

Different techniques and insulation materials have been tested to minimize PDs in power modules. There are three main dielectric systems in a power module, and these are: the ceramic substrate, the encapsulant and the boundary between these two components. The most commonly used insulation material in power modules for the encapsulation is silicone gel [5]. When pouring gels, it is necessary to ensure the absence of air bubbles in the power module, as these air bubbles could be sources of PDs [5]. This is typically done by degassing the module, using a vacuum, but this technique is not flawless [5].

The most commonly used insulators for substrates are Aluminum nitride (AIN) or Aluminum oxide ceramic. The substrates Aluminum nitride (AIN) or aluminum oxide ceramic are used for their good dielectric strength and thermal conductivity [5].

As discussed before, the triple point, connecting the metallization, silicone gel and the substrate is the most critical area. Paper [5] has investigated the use of different encapsulation gels to relieve the stress at the triple point. A form of stress relieving composite is discussed in this paper [5]:

- An insulation composite that varies the conductivity of the capsulant with the applied electric field (field dependent conductivity, or FDC).

FDC insulation composites, are polymer/gels filled with zinc oxide or silicon carbide (semi conductive fillers). Paper [5] conducted an experiment comparing two types of insulation materials, pure silicone gel and 15 % filled barium titanite silicone gel. The test setup was executed using 1 mm thickness of insulation between two 20 mm diameter plane electrodes. The setups were tested using different voltage levels. After this a finite element method was used to simulate the PDs of the substrate surface. The simulation concluded that the barium titanite filled silicone gel resulted in around 70 % reduced electric field around the substrate surface. It was found in the lab tests that the barium titanite filled silicone gel had a 60 % increase of the DIV [5]. The barium titanite fillers increased the viscosity, the density and the thermal conductivity of the insulating gel [5]. The increase of gel density and viscosity posed no significant silicone gel manufacturing challenges.

Another method to decrease the electric field at the triple point, is to coat the ceramic substrate with a high resistive coating (high amorphous silicon) [12]. As shown in [12] due to the high amorphous silicon coating, the electric field peaks were reduced and the partial discharges, under a testing voltage of 10 kV did not exceed 10 pC. Thus, paper [12] found a significant reduction of PDs by coating the substrates with amorphous silicon a-SI. The layer thickness was around 300 nm. It was found that the module with the resistive coating, had an increase of over 300% of the DIV, comparing to the standard power modules [12].

1.3 Problem Statement

Based on the introduction the following problem statement has been formulated and will be addressed in this project

How to evaluate the electrical insulation in the SiC MOSFET module by simulating the electric field distribution inside and measuring partial discharge signals?

1.4 Objectives

To answer the problem statement the following objectives are established:

- Investigate the state of the art of the insulation evaluation in SiC power modules.
- Simulate the electric field distribution inside the SiC MOSFET module based on finite element model (FEM) method.
- Validate the electric field computation by partial discharge normalised testing using IEC 60270 and IEC 61287 standards.
- Analyse the test results identifying which type of partial discharges takes place when testing the SiC MOSFET module, possible origins, magnitude, number and intensity of the observed signals.
- Summarize the normalised test and provide limitations that it presents.
- Propose feasible measures to improve the insulation in the SiC MOSFET module.

1.5 Methodology

The methodology is used to elaborate the main objectives of the project

In order to investigate the state of the art of the insulation evaluation in SiC power modules, a literature review is done in Chapter 1. Throughout this section, the existing E-field simulations methods, PD measurements and PD control techniques are elaborated.

For conducting the necessary simulations, Chapter 3 is done. In this chapter, the electric field strength inside the SiC MOSFET module is evaluated, using the FEM simulation software COMSOL Multiphysics®. Eight different cases are examined. The region with the maximum electric field magnitude is figured out.

Chapter 4 is written to describe the conducted PD measurements. The analysis of the measured PRPD patterns is done in order to investigate the SiC MOSFET insulation under PD conditions and validate the electric field simulation results.

1.6 Limitations

For this project the limitations made are elaborated below:

1. Regarding a PD location, this project will focus only on critical region, which is the interface between the silicone gel and the metallized aluminum nitride ceramic substrate. Hence, PDs inside the ceramic substrate will not be studied, assuming that it is PD-free.
2. In the simulations the sharp edges of bond wires will not be considered.
3. The thermal distribution inside the SiC MOSFET module will not be investigated as only E-field distribution is of interest.
4. The accuracy of FEM simulation will be determined by the level of edges sharpness.
5. The study of insulation degradation will not be included.

Chapter 2

Theory

Throughout this chapter, the theoretical background needed to get a better understanding of the project problem will be described. First, the main electric field characteristics will be elaborated. Next, partial discharge phenomena and international standards on PD tests on power modules will be investigated. Afterwards, the description of insulating materials for power electronics devices will be given. Since electrostatic field computation in the SiC MOSFET module will be based on the COMSOL FEM software, the finite element method will be explained.

2.1 Electric field

Electrostatics

Electric charge, is an attribute as fundamental as mass. As objects with mass are accelerated by gravitational forces, electrically charged objects are accelerated by electric forces. Charge is quantized and obeys a conservation principle. When charges are fixed at a stationary position, they exert *electrostatic* forces on each other. Electrostatic forces are governed by a relationship known as *Coulomb's law* and are described by using the concept of *electric field*. This section will describe the fundamentals of electrostatics, Gauss's law and Maxwells equations.

Electric charge and electric field

There are two important principles which are implied in electric charges. First is the *principle of conservation of charge* which states [13]:

The magnitude of charge of the electron or proton is a natural unit of charge.

The second is:

The algebraic sum of all the electric charges in any closed system is constant.

The observed sum of electric charge is always a multiple integer of this basic unit. A charge is *quantized*. The charge on any macroscopic body is either zero or a multiple integer (negative or positive) of the charge on the electron [13].

Coulomb found that the forces exerting on each other two point charges q_1 and q_2 are proportional to each charge, and are therefore proportional to the two charge product $q_1 q_2$. Coulomb thus defined what is now called the *Coulomb's law* [13]:

The magnitude of the electric force between two point charges is directly proportional to the product of the charges and inversely proportional to the square of the distance between them.

In mathematical terms it can be expressed as Equation 2.1 the magnitude F of force that each of the two point charges q_1 and q_2 a distance apart exerts on the other[13].

$$F = k \cdot \frac{|q_1 q_2|}{r^2} \tag{2.1}$$

Where k is a constant of proportionality the numerical value of which depends on the unit system used, usually Coulombs conmstant. r is the distance between the two charges. The bars with absolute value are used in Equation 2.1 since the q_1 and q_2 charges can either be positive or negative, while the force magnitude F is always positive [13].

When a small test charge q_0 is put at field point P, at a distance from the source point, then Coulomb's law gives the magnitude of force, from Equation 2.1 to Equation 2.2 [13]:

$$F_0 = \frac{1}{4\pi\varepsilon_0} \cdot \frac{|qq_0|}{r^2} \tag{2.2}$$

Where ε_0 is the vacuum permittivity. At a point, the electric field $\overrightarrow{E}$ can be defined as the electrical force $\overrightarrow{F_0}$ experienced at the point by a test charge q_0, divided by the charge q_0. That is, at a given point the electrical field is equal to the electrical force per unit charge at that point, as in Equation 2.3:

$$E = \frac{1}{4\pi\varepsilon_0} \cdot \frac{|q|}{r^2} \tag{2.3}$$

A vector equation can be derived by using the unit vector that gives the magnitude and direction of the electrical field $\overrightarrow{E}$ of a point charge q as in following Equation 2.4 [13]:

$$\overrightarrow{E} = \frac{1}{4\pi\varepsilon_0} \cdot \frac{q}{r^2} \cdot \hat{r} \tag{2.4}$$

Gauss's Law

Gauss's law offers a different way of expressing the relation between electric charge and electric field. Gauss's law is technically similar to Coulomb's law but simplifies problems which have a high degree of symmetry. Gauss's law states:

The magnitude of the electric force between two point charges is directly proportional to the product of the charges and inversely proportional to the square of the distance between them.

So according to the Gauss law; the total flux linked with a closed surface is $\frac{1}{\varepsilon_0}$ times the charge enclosed by the closed surface, with the resulting equation, as in Equation 2.5 [13]:

$$\phi_E = \oint \overrightarrow{E} \cdot d\overrightarrow{A} = \frac{Q_{encl}}{\varepsilon_0} \tag{2.5}$$

Maxwell's equation

The simulation software used in this project, COMSOL, to simulate electric fields uses Maxwell's first equation. Maxwell's equations are a set of four differential equations that form the theoretical basis of classical electromagnetism, which are derived from:

- Gauss's law for electricity

$$\oint \overrightarrow{E} \cdot d\overrightarrow{A} = \frac{Q_{encl}}{\varepsilon_0} \tag{2.6}$$

- Gauss's law for magnetism

$$\oint \overrightarrow{B} \cdot d\overrightarrow{A} = 0 \tag{2.7}$$

- Faradays law of induction;

$$\oint \overrightarrow{E} \cdot d\overrightarrow{s} = \frac{d\phi_b}{dt} \tag{2.8}$$

- Ampere's law

$$\oint \overrightarrow{B} \cdot d\overrightarrow{s} = \mu_0 i + \frac{1}{c^2}\frac{\partial}{\partial t}\int \overrightarrow{E} \cdot d\overrightarrow{A} \tag{2.9}$$

As this project focuses on the electrostatic fields, only Maxwell's first equation is relevant. Maxwell's first equation, describing the electrostatic field, is immediately derived from Gauss's theorem, which in turn is a result of Coulomb's inverse square law. In a slightly different notation, Gauss's theorem states that the electrostatic field D's surface integral over a closed surface is equal to the surface's enclosed charge as in Equation 2.10. Which is:

$$\oiint_s D \cdot d\sigma = \oiiint_v \rho dV \tag{2.10}$$

Where ρ is the charge per unit volume. The surface integral area of a vector field over a closed surface is equal to the integral volume of its divergence, and thus giving Equation 2.11:

$$\oiiint_v divDdV = \oiiint_v \rho dV \tag{2.11}$$

And thus giving as in Equation 2.12

$$divD = \rho \tag{2.12}$$

Using the nabla notation gives Equation 2.13:

$$\nabla \cdot D = \rho \tag{2.13}$$

This is Maxwell's first equation of electrostatics.

Dielectric Polarization

Dielectric polarization is the term used to describe the behavior of a dielectric material when applied to it by an external electric field. When measuring current through a good insulator, polarization is the dominant factor for the displacement current measured. Polarization P increases the electric displacement D, and the relation is defined by the equation [14]:

$$D = \varepsilon_0 E + P \tag{2.14}$$

The dielectric response function $f(t)$ characterizes linear polarization and relates the linear and isotropic material to the electric field E, using the equation [14]:

$$P(t) = \varepsilon_0 \int_0^t E(\tau) f(t-\tau) d\tau \tag{2.15}$$

The polarization is not by itself a measurable amount, but it generates the major part of the displacement current of test object. Maxwell postulated in 1891, that an electrical field $E(t)$ applied to a dielectric produces a current density $j(t)$. The current density $J(t)$ is defined using Equation 2.16 as the sum of conduction and total displacement current [14]:

$$J(t) = \sigma_0 E(t) + \frac{dD(t)}{dt} \tag{2.16}$$

Here σ_0 is the effective d.c. conductivity of the material. By replacing the electric displacement and polarization in Equation 2.16, the current density can be expressed as Equation 2.17 [14]:

$$J(t) = \sigma_0 E(t) + \varepsilon_\infty \frac{dE(t)}{dt} + \varepsilon_0 \frac{d}{dt} \int_0^t E(\tau)F(t-\tau)d\tau \tag{2.17}$$

where, ε_∞ is the relative permittivity for 'high' frequencies. When replacing the electric field with the voltage v applied over the insulation (placed between the electrodes) and changing Equation 2.17, the total current in the time domain through the dielectric can be written as Equation 2.18 [14]:

$$i(t) = C_0 \left[\frac{\sigma_{dc}}{\varepsilon_0} v(t) + \varepsilon_{r\infty} \frac{dv(t)}{dt} \frac{d}{dt} \int_0^\infty f(\tau)v(t-\tau)d\tau \right] \tag{2.18}$$

In the absence of dielectric, C_0 is the geometric capacity of the space between the electrodes and $\varepsilon_{r\infty}$ is the relative permittivity at high frequencies. The first term of the equation represents the material's dc conductivity, while the second and third terms describe the pure capacitive behavior and the dielectric polarization, respectively. The current and voltage within the time domain can be transformed into the frequency domain using the Fourier transform, and the dielectric properties can be represented in the frequency domain parameters. Complex capacitance C represents the relation between current and voltage phasors as shown in Equation 2.19 [14]:

$$I(\omega) = j\omega C_0 \left(\frac{\sigma_{dc}}{j\omega\varepsilon_0} + \varepsilon' - js\varepsilon'' \right) V(\omega) - j\omega(C' - C''_{app}) = j\omega \tilde{C} V(\omega) \tag{2.19}$$

ε'' is dielectric loss, ε' is dielectric constant, the imaginary part C''_{app} refers to the loss effect in the dielectric and the real part of complex capacitance C' refers to a capacitive effect. Loss tangent is a parameter that is independent of geometry and defined as Equation 2.20:

$$\tan\delta = \frac{\varepsilon''_{app}}{\varepsilon'} = \frac{d + \frac{\sigma_{dc}}{\omega\varepsilon_0}}{\varepsilon} = \frac{C''app(\omega)}{C''(\omega)} \tag{2.20}$$

Where δ is the dielectric loss angle. A voltage is applied to the system to achieve the dielectric response of the insulation device, and the current that flows through the insulation is measured. Insulation properties such as $\tan\delta$, C', and C'' can be calculated from the measured current and voltage.

Electrical fields and breakdown strength of insulating materials

This section will descripe the electrical breakdowns in different mediums. It will describe the elecrical breakdown in gases, liquids and cavities.

Electrical breakdown in gases

The relationship between the voltage difference V_b between the electrodes at which a breakdown occurs at a given temperature, their inter-distance d, and the gas pressure p, follows the so-called Paschen's law as in Equation 2.21 [14]:

$$V_b = F(pd) \tag{2.21}$$

For each gas, the curve defined by this law at a given temperature has a minimum voltage between the electrodes below which no breakdown can occur between inter-electrode distance and gas pressure. Across the electrodes, one is likely to find combinations of inter-electrode distance and gas pressures at which an electrical breakdown can occur. That is why the use of gas as a dielectric, while usually very effective at high pressures or at very low pressures (high vacuum), can become dangerous if the gas pressure changes over a wide range as it changes temperature. Figure 2.1 shows an extrapolation of the so-called Paschen curve from many studies. At high pressures a further rise in pressure raises the gas density but also reduces the mean free path: while the probability of collisions raises, the lower collision energy is dominant due to the shorter mean free path and provides a rise in V_b [14].

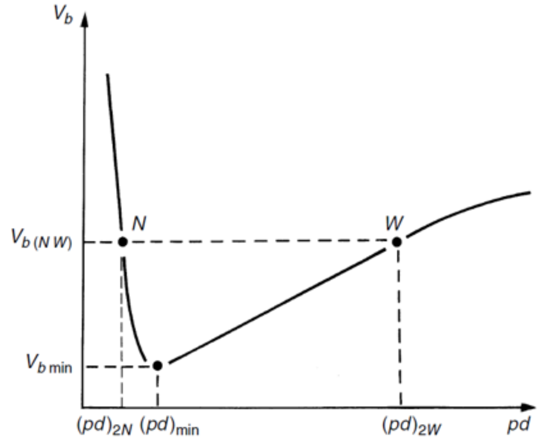


Figure 2.1: Paschen's curve [14]

A further reduction in pressure at low pressures increases the mean free path but also reduces the gas density: while the energy of the collision increases due to the longer mean free path, the lower likelihood of ionizing collisions provides an increase of V_b. To sum up, the mean free path is dominant at high pressures, the likelihood of collision is dominant at low pressures and there is a product pd at which V_b has a minimum [14].

Breakdown in liquids

For high voltage transformers, converters, condensers, switches, and circuit breakers, electrical insulating liquids are used, for general oils. In many cases they serve as both dielectric and coolant medium. A critical parameter when designing liquid insulators, is the liquids pureness. When an electric field is applied to an electric isolating liquid, impurities initially control the current. Electron emissions can start at fields higher than 100 $\frac{kV}{cm}$ at the impurity interfaces, triggering an ionization process which could lead to an electrical breakdown. The mechanisms for breakdown of liquids are still not fully understood. The requirement for the initiation of electron avalanche is obtained by equating an electron's gain in energy over its mean free path to that necessary for molecule ionization as in Equation 2.22 [14]:

$$eE\lambda = chv \tag{2.22}$$

Where E is the field applied, the electron means free path, hv is the sum of energy lost in the ionization of the molecule, and c is an arbitrary constant [14].

Cavity breakdown

As [14] shows, the insulating liquids can contain bubble-shaped gaseous inclusions. Processes by which bubbles form include:

- gas pockets on the electrode surface,
- changes in temperature and pressure,
- dissociation of products by electron collisions giving rise to gaseous products,
- liquid vaporization by corona-type discharges from points and irregularities on the electrodes,

The electrical field in a spherical gas bubble that is submerged in a liquid with permittivity ε_{liq} is governed by Equation 2.23 [14]:

$$E_b = \frac{3E_0}{\varepsilon_{liq} + 2} \tag{2.23}$$

E_0 describes the field in the liquid without any bubble. Once field E_b is equal to the field of gaseous ionization, discharge occurs which will result in liquid decomposition and breakdown can follow [14].

2.2 Partial discharge

The definition given in the International Electrotechnical Commission (IEC) International Standard for partial discharge, is [14]:

> *Partial discharge (PD) is a localized electrical discharge that only partially bridges the insulation between conductors and which may or may not occur adjacent to a conductor.*

PDs do not completely bridge the space between two conductors, thus it's not a full breakdown. PDs are electrical discharges which can occur within electrically insulated devices. The insulations of the devices can consist of any combination of, solid, liquid, or gaseous materials. If PDs occur continouosly, an electrical breakdown can happen. Partial discharges has several different types of discharge phenomenons. These are described in[14] and shown in Figure 2.2 as:

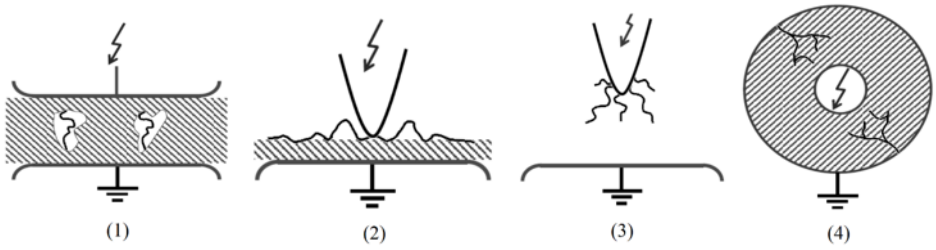


Figure 2.2: Types of Partial Discharges [14]

- (1) shows the internal discharge phenomenin. It can occur in voids or cavities within a solid or a liquid dielectric.
- (2) shows the surface discharge phenomenon. It appears at the boundaries of insulation materials.
- (3) shows the corona discharge phenomenon. It occurs in gaseous dielectrics.
- (4) show the treeing phenomenon. It happens when a solid insulating material experiences a continuous impact of discharges. These impacts form channels that decrease the materials PDIV..

The lifetime of an insulator, is affected by PDs, and the insulator deteriorates by each discharge event. So preventing PDs will increase an insulators lifetime.[14]

Internal Discharges

Internal discharges follows Paschen's law in gas-filled cavities. When a PD is initiated, it can initiate further PDs. Even if the applied voltage to the insulation is below the PDIV. As the PD happens, due to the displacement of the charge the voltage around the cavity decreases to the residual value. The voltage across the cavity will again exceed the minimum PDIV, in order to allow new discharges. The voltage through the cavity builds up in the reverse direction as the impulse decays. If the electrical field around the space is decreased below the minimum PDIV by the impulse and the occurring discharge, there will be no more discharges until the peak cavity stress rises to its minimum PDIV again. In conclusion, if the impulse initiates a cavity PD, the PD is likely to be continuous, as the cavity extinguishing voltage is much lower than the PDIV. [14].

Surface Discharges

Surface discharges are PDs between different insulating materials. The behavior of surface PDs are influenced by the applied electrical fields, the materials permittivity and the materials conductivity. An applied voltage can initiate a so-called "streamer" discharges that can propagate to the ground electrode and their propagation distance will be different depending on the magnitude of the voltage and may result in a complete flashover. Ionization of gas or liquid caused by PDs may assist in the development of PD and the wider spread of surface charges. Boosting the electrical field at the ionized zone leads to more ionization that can assist in the development of PD. The velocity of the streamer and the density of the space charged in dielectric liquid depend on the magnitude of the voltage. A streamer may be stopped by a solid barrier, resulting in accumulation of local charges. The gas or liquid medium itself can have both positive and negative ions; applied electrical field and ion adsorption can lead to accumulation of surface charge on the solid. Another possible mechanism leading to surface charging is the dissociation of charges from the surface.

Corona discharges

Corona is a stream of charged particles such as electrons and ions that is accelerated by an electric field. They occur when an applied E-field exceeds the electrical strength of a gas. A corona may occur when the electric field strength around a conductor is high enough to create a conductive area but not high enough to cause an electric breakdown to nearby objects. The phenomenon is important in high voltage engineering where non-uniform fields are possible, so methods have been carefully implemented to minimize E-fields in high voltage devices. Under positive voltage a corona emerges over the entire surface of an electrode in the form of a uniform bluish-white sheath. But the corona appears as reddish flashing spots on negative electrodes scattered around.

2.2.1 The basic PD test circuit

Electrical PD detection methods are based on the "PD (current or voltage) pulse" arising at the test object terminals. Firstly, in order to evaluate the main quantities of a PD pulse, the test object is considered as a simple capacitor as represented in Figure 5.9. There is a solid or liquid insulating material between the two electrodes A and B with a gas-filled cavity. The cavity capacitance is C_c, while C_b' and C''_b are the "healthy" series capacitances on both sides of the cavity within the dielectric. The parallel capacitance of the dielectric around the "sick" branch is represented by $C_a = C_a' + C''_a$. Furthermore, the inequality of the capacitances magnitudes is considered by condition in Equation 2.24 [14].

$$C_a \gg C_c \gg C_b \tag{2.24}$$

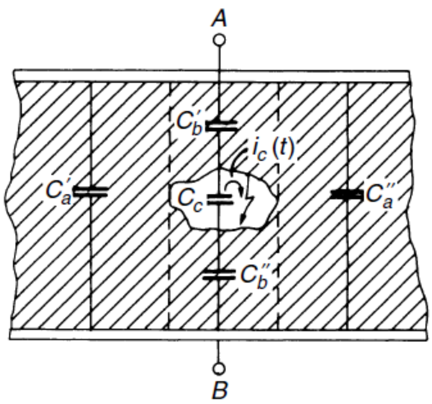


Figure 2.3: PD test object. Structure of an insulation system with a void [14]

If an applied sinusoidal voltage is increased, then after a certain value a PD may occur in the void. Thus, the voltage drop at the cavity leads it's capacitance C_c to discharge significantly. With a further increase or decrease by the negative slope of the applied AC voltage the discharge phenomena happens repeatedly during each cycle [14].

This phenomena can be described by the equivalent circuit which is shown in Figure 2.4. Where the switch S simulates an electrical sparking within the cavity, when it's capacitance C_c gets discharged. It is controlled by the voltage V_c between the cavity capacitance C_c, and it is closed only for a short duration of the current $i_c(t)$ flow. The time interval, during which the PD takes place, is modelled by R_c resistor. Since the discharge current $i_c(t)$ is very small in amplitude (smaller than 10^{-4} A) and is a very short pulse (less than about 1 μs), it cannot be measured [14].

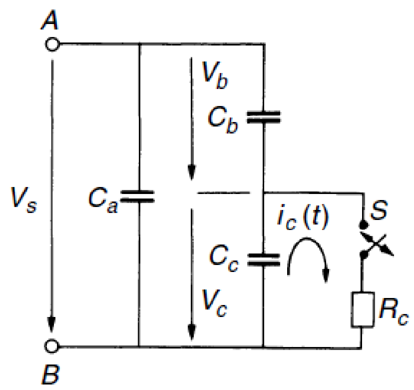


Figure 2.4: Equivalent circuit of PD in a dielectric [14]

However, the voltage drop at the cavity also causes a voltage change at the dielectric C_a as in Equation 2.25 [14].

$$\Delta V_a = \frac{C_b}{C_a + C_b} \cdot \Delta V_c \tag{2.25}$$

Since V_a is the voltage variation at the dielectric, it is a quantity that can be measured. Nonetheless, according to Equation 2.24 during PD the magnitude of this voltage drop at the dielectric is very small. Therefore, the detection circuit based on another quantity, which can immediately be determined, is needed. It can be seen in Figure 2.5 [14].

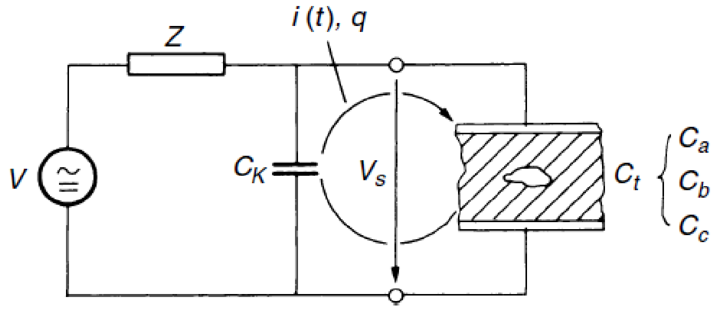


Figure 2.5: The PD test object C_t in a PD test circuit [14]

The sample is connected to an AC voltage source V. An impedance Z, consisting either only of the natural impedance of the lead between the power supply and the parallel configuration of the "coupling capacitor" C_k and the test object C_t, or extended by a PD-free low-pass filter. This filter may disconnect C_k and C_t from the power source during the partial discharge process. The capacitor C_k acts as a stable voltage source during the short duration of the PD phenomena. It releases the PD pulse current $i(t)$ between C_k and C_t and keeps the voltage across the test specimen C_t constant. After that, the pulse current $i(t)$ provides the charge quantity, which is given by Equation 2.26 [14].

$$q = \int i(t) = (C_a + C_b) \cdot \Delta V_a \tag{2.26}$$

By substituting Equation 2.25 into Equation 2.26, this charge can be determined as in Equation 2.27 [14].

$$q = C_b \cdot \Delta V_c \tag{2.27}$$

This charge is called *apparent charge of a PD pulse*. It is a PD quantity, which is much more realistic than ΔV_a, since the sample capacitance C_a, which is the main component of C_t, does not affect it [14].

PD signals analysis

It is very important to analyse PD signals, in order to figure out the PD source, which indicates the weak point in the insulation system. It can be done by Phase-resolved Partial Discharge (PRPD) patterns. The illustration of a typical PRPD pattern can be seen in Figure 2.6.

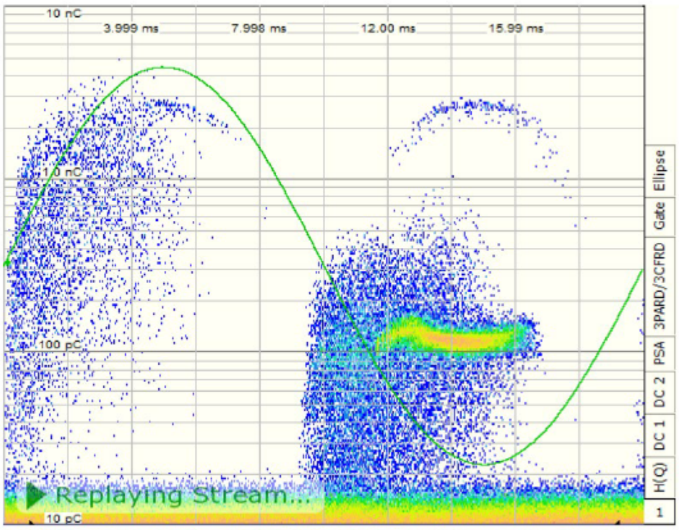


Figure 2.6: An example of PRPD pattern

The phase axis (x-axis) shows one complete cycle of the applied voltage, while the PD charge magnitude axis (y-axis) represents the range of magnitude observed. PD data within certain number of the applied voltage cycle is sketched on the x-axis of one voltage cycle. Hence, a PRPD patterns show PD occurrences at a specific phase of the applied voltage with certain charge magnitude within certain number of the applied voltage cycles. PRPD techniques can be used to recognize the types of PD, based on the patterns detected [15].

Internal PD takes place around the zero crossing with respect to the applied voltage. As stated earlier, internal discharges occur in voids in solid or liquid dielectrics. If the void is placed in the middle of the dielectric, the electric field on the cavity surface is symmetrical. Thus, the PRPD patterns of void discharge at positive and negative cycles of the applied voltage are symmetrical. Unlike internal discharge, surface discharge is assymetrical on two halves of the applied voltage. Corona discharge happens at 90°or 270°of the applied voltage, being assymetrical as well [15].

2.2.2 International standards on PD tests on power electronics devices

Power electronic devices are subjected to partial discharges using IEC 60270 and IEC 61287 normalized tests.

According to IEC 60270, in order to measure the apparent charge magnitude, a measuring system must be integrated into the test circuit described in section 2.2.1. The measuring circuit is represented in Figure 2.7 [14], [16].

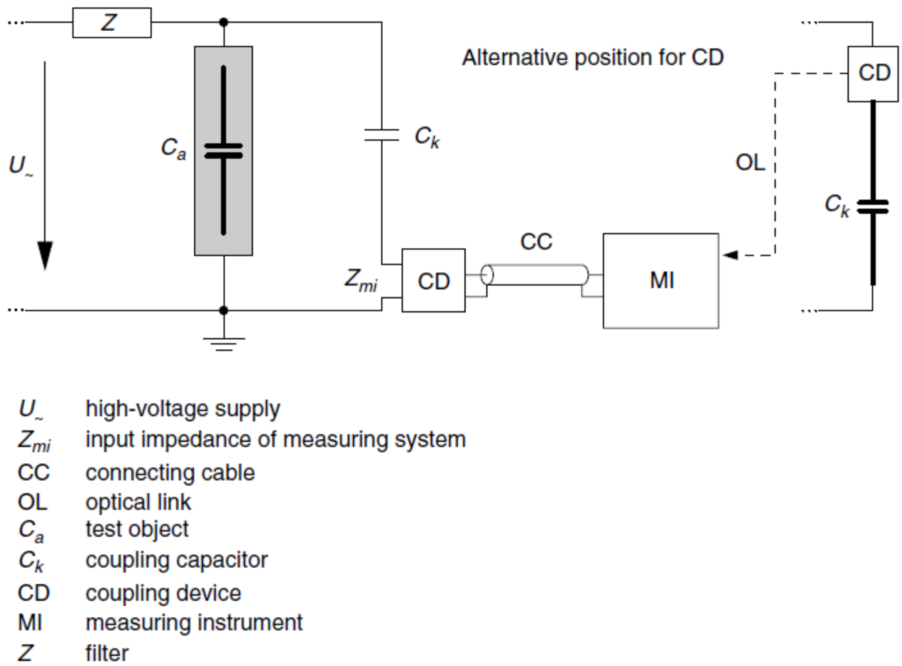


Figure 2.7: Basic PD measuring circuit [14], [16]

The coupling device CD together with its measuring impedance Z_{mi} forms the measuring system input end. Moreover, as it is seen from the Figure 2.7, if the test specimen has one grounded terminal, the CD can be set in high-voltage potential. In that case, for connecting the CD with the measuring instrument MI optical links OL are used instead of a connecting cable CC [14], [16].

As regards the IEC 61287, this International Standard is applicable to power electronic converters mounted on board railway rolling-stock. It recommends to apply an AC rms test voltage equal to $1.5\frac{U_m}{\sqrt{2}}$. U_m is the highest permissible blocking voltage of the power module. In this project, for the 1.2 kV power MOSFET, it is $1.5\frac{1.2}{\sqrt{2}} = 1.27$ kV. The voltage is increased up to $1.5\frac{U_m}{\sqrt{2}}$ in 10 s and is applied for one minute. Some PD's can be detected during the first part of the test cycle. After that, the voltage is decreased $1.1\frac{U_m}{\sqrt{2}}$ in 10 s. For the 1.2 kV power MOSFET, this voltage corresponds to 0.93 kV. This voltage is maintained for 30 seconds. During the last 5 s of the second part of the test cycle the peak magnitude of PD in pC is recorded. In this project, the value for a component to pass PD test is selected as 10 pC [12]. The test cycle is summarized in Figure 2.8 [2], [12], [17].

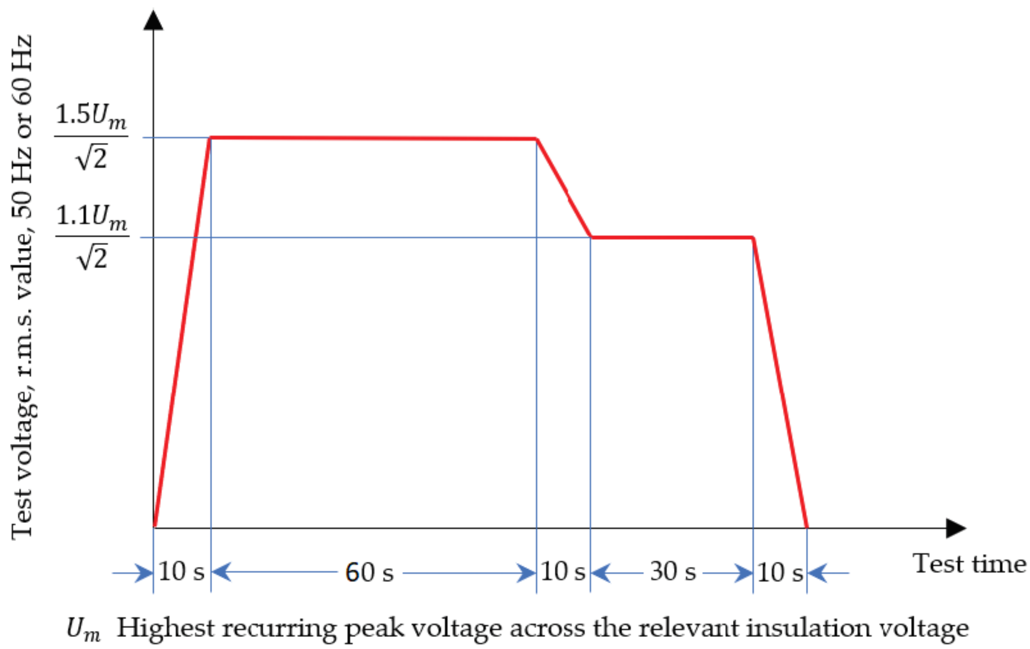


Figure 2.8: Partial discharge test; voltage versus time [2], [12], [17]

The partial discharge measurements must be performed at 50 or 60 Hz. According to IEC 61287, the electrical terminals of power electronics modules should be shorted together, and PD's are measured when AC voltage is applied between the short circuited terminals and the module's base plate.

2.3 Insulating materials for power modules

Different types of insulating materials have different industrial applications. Some are more suitable for use in avionics; some are more suitable for PCBs, while others have proved to be the best for applications where severe vibrations such as motors and generators have to bear on insulation. Wide spread applications of insulation materials have been found everywhere in power modules, transformers, electrical switches and circuit breakers. Researchers are heading toward newer and more reliable insulation materials. More and more insulation materials are being introduced in electronics and integrated circuits to cope with demands of high speed switching. Aluminum nitride (AlN), Alumina (Al_2O_3), and silicone gels are most widely used in power modules as insulating materials.

Even though AlN is more expensive than Al_2O_3, it is frequently used in high-power applications due to its better thermal properties. Many studies have been done on the analysis of PD's in AlN under AC stress to calculate the PD inception voltage, and to assess the system's reliability. Typical electrical strength of AlN is 170 $\frac{kV}{cm}$ [18].

Silicone gels are gaining popularity in electrical applications as insulating materials, owing among others to their good thermal stability, high elasticity, fast processing and good dielectrical properties. The surface discharge in the module is well known to be one of the weakest points in insulation and those discharges cause silicone gel cavity growth. Typical electrical strength of silicone gel is 267 $\frac{kV}{cm}$ [18].

2.3.1 Electrical degradation of the silicone gel

Power electronic modules have a complex inner structure and thus an inhomogeneous field distribution. Simulations of the E-field inside modules show large values of the local electric field at the interface between the rim of the metallization on ceramic substrates and silicone gel. Therefore, partial discharges mainly occur at that area. These PDs interfere with the silicone gel and give rise to it's electrical degradation, which shortens the lifespan of power electronic devices significantly [19], [20].

In some studies [19], [20] the silicone gel was investigated in a strongly inhomogeneous electric field, created by needle-plane geometry. This models the E-field in the critical region of power modules described above. In one of these studies [19] the needle diameter was 0.6 mm, while the needle's tip radius was around 5 μm. The radius r_e of plane electrode was 5 mm. The gap distance s was 3 mm. The electrodes were embedded in silicone gel. The layout of this model is shown in Figure 2.9

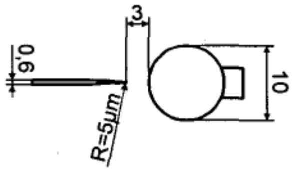


Figure 2.9: Layout of the needle-plane geometry [19]

First, the inception voltage of the sample amounted to 9 kV. Nonetheless, in order to get a sufficient amount of PDs, the applied test voltage was set to 10 kV. This voltage led to the electrical breakdown in less than one hour. In microscopic analysis of the breakdown channel electrical treeing close to the tip was observed. A photomicrograph of this electrical tree can be seen in Figure 2.10 [19].

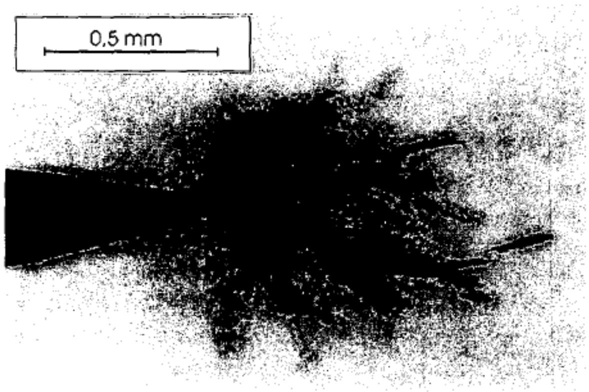


Figure 2.10: Photomicrograph of the electrical treeing near the tip of needle [19]

Moreover, violently moving bubbles close to the needle tip were developed. The next day these bubbles disappeared and the breakdown channel became smaller. A few days later the inception and the breakdown voltages of the same destructed specimen dropped to 2.5 kV and 4 kV respectively. Thus, silicone gel partially restored it's insulating properties. As a consequence, this self healing effect was limited to a certain number of partial discharge impulses. If PDs were repeated at the same location, the gel structure close to the needle would get destroyed and an irreversible degradation would occur [20]. Therefore, it was concluded that, in order to assure the insulation long lifetime, possible PD sources have to be avoided [19].

2.4 Finite element method (FEM)

For insulation of electrical equipment an accurate electric field computation is required. It can be done by numerical techniques enabling to solve problems where use of analytical methods is impossible [21]. One of the most widely used numerical methods is finite element method (FEM). FEM-based E-field computation is based upon the minimizing the energy within the whole field region [14].

The common mathematical problem to be solved is the determination of the electrostatic potential ϕ and the field $E = -\nabla\phi$ within two-dimensional (2D) region, which is satisfied by Laplace's or Poisson's equation as in Equation 2.28 [21].

$$\nabla^2\phi = -\frac{\rho}{\varepsilon_r\varepsilon_0} \tag{2.28}$$

Where ρ is the space charge density, ε_r and ε_0 are relative and absolute permittivity of the free space respectively [21].

Now the volume of the region is reduced to the area limited by boundaries. Thus, in order to solve partial differential Equation 2.28, the following boundary condition is considered [14], [21]:

- The electric potentials of all points on the boundary are known (Dirichlet condition).

The energy within an area-limited electric field is as in Equation 2.29 [14].

$$W = z\iint_A \left[\frac{1}{2}\left\{\varepsilon_x\left(\frac{\partial\phi}{\partial x}\right)^2 + \varepsilon_y(\left(\frac{\partial\phi}{\partial y}\right)^2\right\}\right] dxdy \tag{2.29}$$

Where z is a constant and therefore $\frac{W}{z}$ is an energy density per elementary area dA. The finite element analysis method requires the following four major steps [14]:

1. Discretization of the solution region into a finite number of sub regions (elements).
2. Development of the governing equations for the sub region (element).
3. Assembly all the elements in the solution region.
4. Solution of equations.

Finite elements discretization

A section of a 2D solution region A is divided into triangular elements (sub regions) as it is shown in Figure 2.11. The sides of this triangular elements form a grid with nodes. For instance, i, j and m for element e [14].

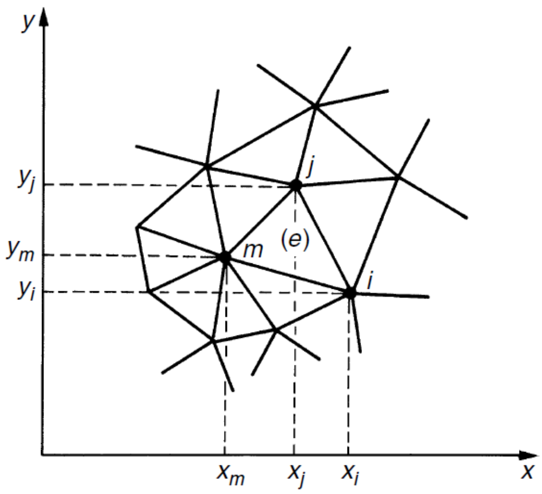


Figure 2.11: A part of solution region A divided into triangular elements. Nodes i, j and m for element e

The potential distribution $\phi(x, y)$ of the element is formulated by polynomial approximation as in Equation 6.1 [14].

$$\phi(x, y) = \phi = \alpha_1 + \alpha_2 x + \alpha_3 y \tag{2.30}$$

Governing equations of each finite element

The potentials at nodes i, j and m are obtained by Equation 2.31 [14].

$$\left.\begin{aligned} \phi_i &= \alpha_1 + \alpha_2 x_i + \alpha_3 y_i \\ \phi_j &= \alpha_1 + \alpha_2 x_j + \alpha_3 y_j \\ \phi_m &= \alpha_1 + \alpha_2 x_m + \alpha_3 y_m \end{aligned}\right\} \tag{2.31}$$

The coefficients α_1, α_2 and α_3 for element e in Equation 6.1 are determined as in Equation 2.32 [14].

$$\alpha_1 = \frac{1}{2\Delta_e}(a_i\phi_i + a_j\phi_j + a_m\phi_m); \tag{2.32a}$$

$$\alpha_2 = \frac{1}{2\Delta_e}(b_i\phi_i + b_j\phi_j + b_m\phi_m); \tag{2.32b}$$

$$\alpha_3 = \frac{1}{2\Delta_e}(c_i\phi_i + c_j\phi_j + c_m\phi_m); \tag{2.32c}$$

where

$$\left.\begin{aligned} a_i &= x_j y_m - x_m y_j \\ a_j &= x_m y_i - x_i y_m \\ a_m &= x_i y_j - x_j y_i \end{aligned}\right\} \tag{2.32d}$$

$$\left.\begin{aligned} b_i &= y_j - y_m \\ b_j &= y_m - y_i \\ b_m &= y_i - y_j \end{aligned}\right\} \tag{2.32e}$$

$$\left.\begin{aligned} c_i &= x_m - x_j \\ c_j &= x_i - x_m \\ c_m &= x_j - x_i \end{aligned}\right\} \tag{2.32f}$$

Δ_e is the area of the element e, which is as in Equation 2.33 [14].

$$\left.\begin{aligned} 2\Delta_e &= a_i + a_j + a_m \\ &= b_i c_j - b_j c_i \end{aligned}\right\} \tag{2.33}$$

With Equations 6.1, 2.31 and 2.32 the potential distribution within the element may therefore be related to the adjoining nodes potentials. Now it can be expressed as in Equation 2.34 [14].

$$\begin{aligned} \phi_e(x,y) = \frac{1}{2\Delta_e}[(a_i + b_i + c_i)\phi_i + ... \\ + (a_j + b_j + c_j)\phi_j + (a_m + b_m + c_m)\phi_m] \end{aligned} \tag{2.34}$$

or as in Equation 2.35 [14].

$$\phi_e = [N_i, N_j, N_m] \begin{Bmatrix} \phi_i \\ \phi_j \\ \phi_m \end{Bmatrix} \tag{2.35}$$

Where the functions N are the "shape functions", which depend on the elements shape (rectangular, square and etc.). With Equation 2.34 or Equation 6.1 the element energy X is determined by Equation 2.36 [14].

$$X^e = \frac{W_e}{z} = \frac{1}{2}\Delta_e \left\{ \varepsilon_x \left(\frac{\partial \phi}{\partial x}\right)^2 + \varepsilon_y (\left(\frac{\partial \phi}{\partial y}\right)^2 \right\}_e \tag{2.36}$$

with

$$\begin{aligned} \frac{\partial \phi}{\partial x} &= \alpha_2 = f(\phi_i, \phi_j, \phi_m) \\ \frac{\partial \phi}{\partial y} &= \alpha_3 = f(\phi_i, \phi_j, \phi_m) \end{aligned} \tag{2.37}$$

Assembling all the elements

However, as FEM concerns itself with minimization of the energy within the whole system, instead of absolute values of these energies only their derivatives in regard to the potential distribution are taken into account. Consequently, the energy minimization of the entire system can be written as in Equation 2.38 [14].

$$\frac{\partial X}{\partial \{\phi\}} = 0 \tag{2.38}$$

It is also may be written as a matrix as in Equation 2.39 [14].

$$\frac{\partial X^e}{\partial \{\phi\}^e} = \frac{\varepsilon_e}{4\Delta_e} \begin{bmatrix} (b_i^2 + c_i^2) & (b_i b_j + c_i c_j) & (b_i b_m + c_i c_m) \\ & (b_j^2 + c_j^2) & (b_j b_m + c_j c_m) \\ sym & & (b_m^2 + c_m^2) \end{bmatrix} \begin{Bmatrix} \phi_i \\ \phi_j \\ \phi_m \end{Bmatrix} = [h]^e \{\phi\}^e \quad (2.39)$$

Where $[h]^e$ is the "stiffness matrix" for each element, which involves the geometric quantities and the material's permettivity ε_e. From Equation 2.39 it is obvious that any node potential of this system will be dependent on the surrounded nodes potentials [14].

Solving the resulting equations

In the last step the example with four triangular elements is considered. In Figure 2.12 the elements and nodes are numbered [14].

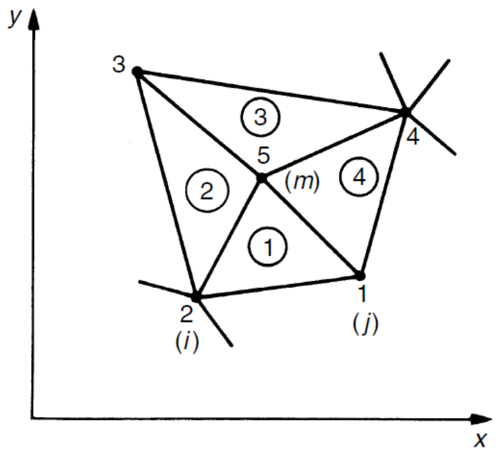


Figure 2.12: Four triangular elements with connected node 5

According to Equation 2.38, the minimization of the energy of this system is as in Equation 2.40 [14].

$$\frac{\partial X}{\partial \phi_5} = 0 \quad (2.40)$$

The stiffness matrix is as in Equation 2.41 [14].

$$[h]^e = \begin{bmatrix} (h_{ii})_e & (h_{ij})_e & (h_{im})_e \\ & (h_{ij})_e & h_{jm})_e \\ sym & & (h_{mm})_e \end{bmatrix} \tag{2.41}$$

where

$$\begin{aligned} (h_{ii})_e &= \frac{\varepsilon_e}{4\Delta_e}(b_i^2 + c_i^2) \\ h_{ij})_e &= \frac{\varepsilon_e}{4\Delta_e}(b_i b_j + c_i c_j) \\ &. \\ &. \\ &. \\ &\text{etc.} \end{aligned} \tag{2.42}$$

Substituting the e with the numbers of the each element in Figure 2.12 gives Equation 2.43 [14].

$$\begin{aligned} \frac{\partial X}{\partial \phi_5} &= 0 = \\ \text{(from element 1)} &= [(h_{im})_1\phi_2 + (h_{jm})_1\phi_1 + (h_{mm})_1\phi_5 + ... \\ \text{(from element 2)} &= [(h_{im})_2\phi_3 + (h_{jm})_2\phi_2 + (h_{mm})_2\phi_5 + ... \\ \text{(from element 3)} &= [(h_{im})_3\phi_4 + (h_{jm})_3\phi_3 + (h_{mm})_3\phi_5 + ... \\ \text{(from element 4)} &= [(h_{im})_4\phi_1 + (h_{jm})_4\phi_4 + (h_{mm})_4\phi_5]. \end{aligned} \tag{2.43}$$

The last equation can be expressed as in Equation 2.44 [14].

$$H_{15}\phi_1 + H_{25}\phi_2 + H_{35}\phi_3 + H_{45}\phi_4 + H_{55}\phi_5 = 0 \tag{2.44}$$

where

$$\begin{aligned}
H_{15} &= [(h_{im})_4 + (h_{jm})_1] \\
H_{25} &= [(h_{im})_1 + (h_{jm})_2] \\
&\;\;. \\
&\;\;. \\
&\;\;. \\
H_{55} &= [(h_{mm})_1 + (h_{mm})_2 + (h_{mm})_3 + (h_{mm})_4] = \sum_{r=1}^{4}(h_{mm})_r
\end{aligned} \tag{2.45}$$

From this equation ϕ_5 could be obtained directly in case the potentials ϕ_1 to ϕ_4 were noted. The nodes potentials 1 to 4 might still be located in a larger triangular mesh [14].

Chapter 3

Modeling and simulation of the E-field distribution inside the SiC MOSFET module

This chapter will explain the setup and methods used for simulating electric fields in the MOSFET power module. Previous chapters have explained the fundamental theories used in this section, which include; Maxwells equations, Finite element method and dielectric polarization.

With 1200 V_{DSS} (drain source PDIV (peak)), 55A SiC MOSFETs designed and developed by Microsemi ®, the dc bus voltage of a 1200V 2-level voltage source converter allows these SiC devices to be used extensively in applications such as wind, solar and motor drives. In this paper, the 1200 V, 55 A SiC MOSFET is characterized for its insulation properties. A top view of the MOSFET power module is illustrated in figure 3.1:

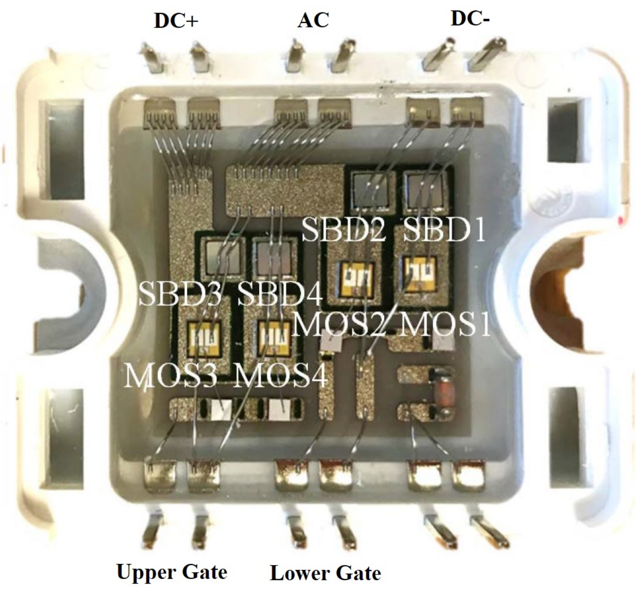


Figure 3.1: Top view of the Microsemi SiC power module

This module consists four SiC MOSFET dies (MOS1-MOS2 and MOS3-MOS4) and their series connected SiC Schottky barrier diodes (SBD) dies (SBD1-SBD2 and SBD3-SBD4). The stacked structure, can be seen as a cross section view in figure 3.2:

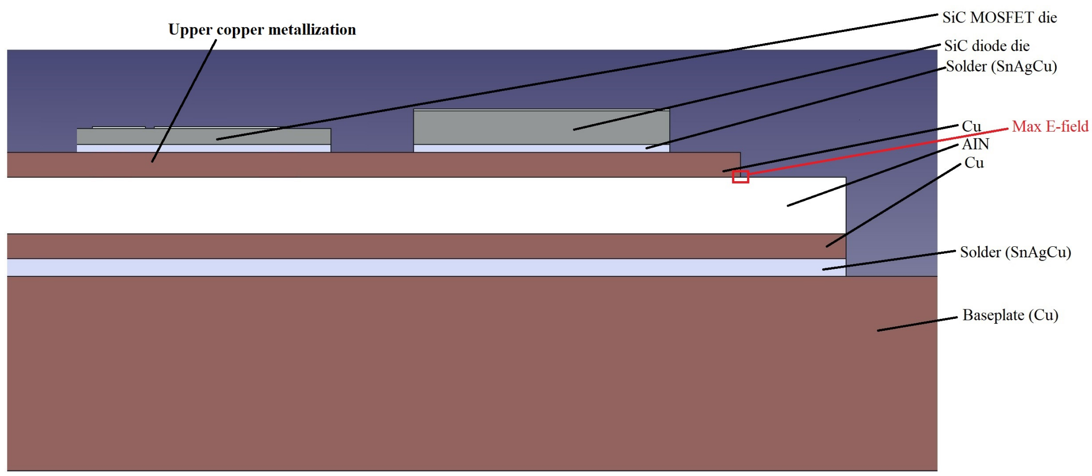


Figure 3.2: Cross section view of the stacked struccture of the Microsemi SiC power module

The MOSFET and diode dies, are soldered on the upper copper metallization using solder (SnAgCu). The upper and lower copper metallizations are bonded to the ceramic substrate AIN, using direct copper bonding (DCB). The Copper-AIN-Copper structure is soldered on a Copper baseplate using solder (SnAgCu). The relevant layer thicknesses, in the structure, can be seen in table 3.1:

Table 3.1: Material thickness

Material	Thickness [mm]
Mosfet die	0,18
SBD die	0,377
Mosfet Solder	0,09
SBD solder	0,09
Copper (upper)	0,28
Copper (Lower)	0,28
AIN	0,63
Solder	0,2
Baseplate	0,22

The simulation software chosen for this project is COMSOL Multiphysics®, which is a cross-platform software used for multiphysics simulation and uses the finite-elements method. It makes user interfaces and coupled systems of partial differential equations (PDEs), based on traditional physics. COMSOL offers electrical, mechanical, gas, acoustics, and chemical systems with an IDE and streamlined workflow. Besides the classical problems that can be solved with framework modules, it is possible to use the core Multiphysics kit to solve PDEs in weak form. For external control of the program an API for Java and LiveLink for MATLAB can be used. An Application Builder can be used to create independent simulation applications that are tailored to the domain. Users can use Drag-and -Drop or programming tools. Many modules are available for COMSOL, these modules focus on the physics within: Electrical, Mechanical, Fluid, Acoustic, Chemical, Multipurpose, and Interfacing application fields. This project uses the AC/DC module, specifically steady state electrostatics in COMSOL. The AC/DC module provides a wide range of modelling features and numerical methods for investigating electromagnetic fields and EMI/EMC by solving Maxwells equation. Maxwells equations are described in chapter 2. The fundamental electric constants, used for the electrostatic simulations can be found in Appendix A. To make a simulation in COMSOL, it is necessary to define the following parameters:

- Geometry
- Materials
- Physics and boundary conditions
- Mesh

3.1 Simulation setup

The 3D model of the MOSFET power module, has been created in SolidWorks, which then could be imported to COMSOL. The 3D model can be seen in figure 3.3:

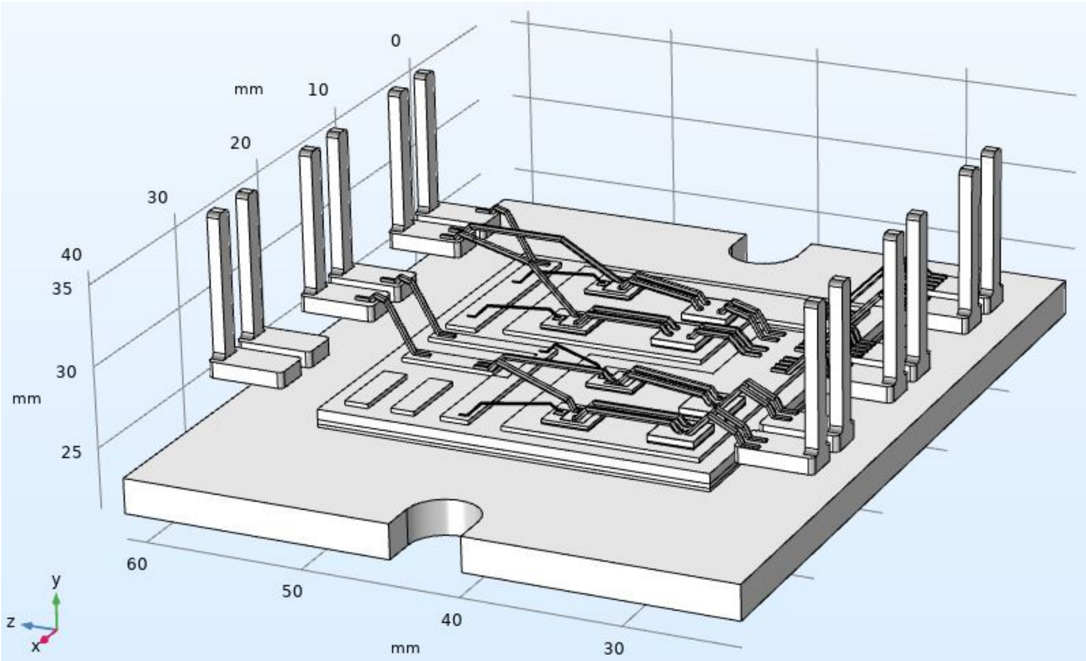


Figure 3.3: 3D model of MOSFET module APTMC120AM44CT1AG from COMSOL.

The 3D model, illustrated in figure 3.3, includes almost all of the the module components. The critical area, the triple point as shown in figure 3.2, is of interest in this project, thus many parts can be deleted. Parts are deleted to minimize the computational power needed to simulate the electrostatic problem. First, the main electrical circuit is identified in the MOSFET Power module. A top view of the module is illustrated in Figure 3.4:

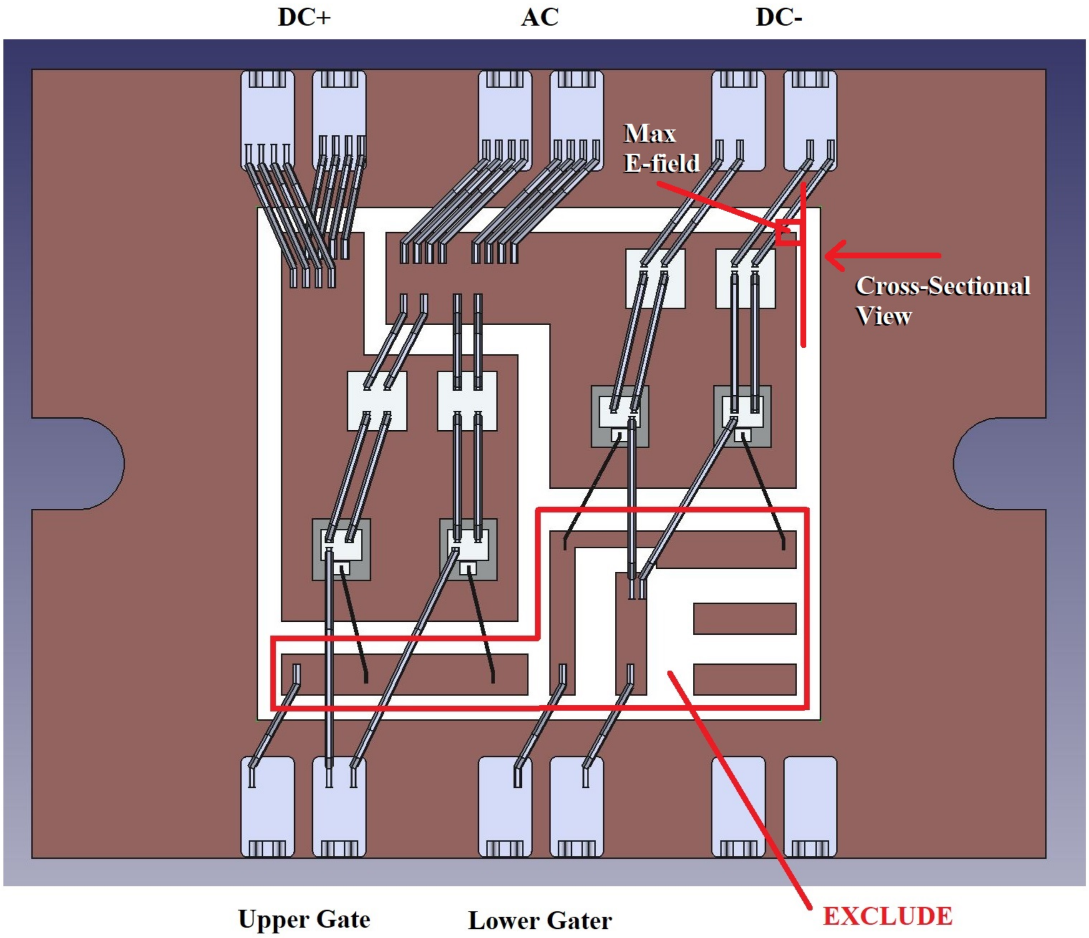


Figure 3.4: Upper copper metallization to exclude.

The upper copper metallizations used for upper/lower gates are excluded, because of the low voltage applied to this section. The applied voltage to the gates are much lower than the applied voltage to the main circuit, and can thus be ignored. This results in two upper copper metallizations, that can be simulated in COMSOL. To further decrease the computing power needed for simulating the electrostatic problem, one of the two upper copper metallizations can be excluded, by making a low-accuracy simulation. The bond wires, dies, solder to dies and pins are also deleted from the 3D model.

The modules solid arrangement, as shown in fig. 3.2, is covered with silicone gel as an insulation. The area where the peak intensity of the electric field o ccurs is identified with a rectangle 'Max E-field', in fig. 3.2. In this project, this area was investigated. The upper layer of metal is applied with a voltage of 1.2 kV DC while the lower layer of metal attached to the conductive baseplate is at ground potential. COMSOL has a materials library, which can be imported to the project. And, to make a simulation of the electrostatics in the model, COMSOL uses the relative permittivity of each material. The relative permittivity and PDIV for each material, used in this project is illustrated in Table 3.2:

Table 3.2: Material properties used in this project

Material	Relative Permittivity	PDIV [kV/cm]
Copper	100000	-
AIN	9,21	550
Solder	10000	-
Baseplate	100000	-
Silicone gel	2,2	267
DuPont Performance Polymers Zytel®	2,4	330
Silicon coating	11,7	200
Silicon carbide coating	9,7	3000

The base 3D model, had metallization edges that were infinitely sharp. Infinetely sharp edges can create infinetely high E-fields, according to the proportionality rule, shown in. eq.3.1 [9]:

$$E_{MAX} \propto \frac{1}{r^{\frac{1}{3}}} \tag{3.1}$$

Where E_{MAX} is the maximum E-field, and r is the radius of a 90 degree edge. These edges were thus filletet, to approximate a realistic model. The fillet radius used, were both 10 and 30 micrometers. The zoom-in of the metallization shown in figure 3.5, has a fillet radius of 10 micrometers. For calculating the FEM, a fine mesh is generated. Mesh generation is a computer aided practice, of creating a mesh, which generates a subdivison of a continuos geometric space into discrete geometrical and topological cells. These meshes can be created by human guidance, as it's done in COMSOL. The finer the mesh, the more computing power is require for the FEM, but the results will be more accurate. For all simulations the upper mesh limit was set to 1 millimeter, while the lower mesh limit was set to 5 micrometers, a sketch of this can be seen in figure 3.5:

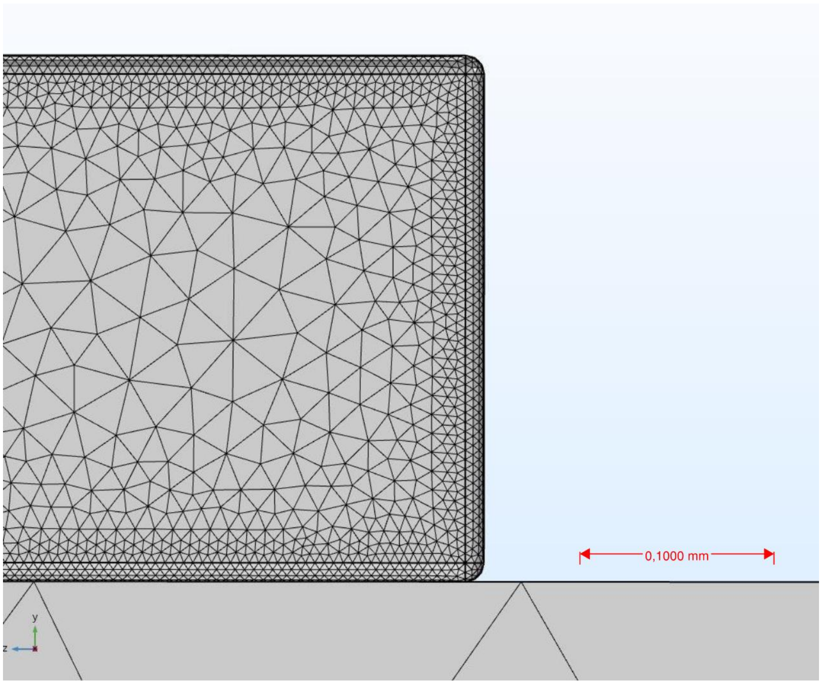


Figure 3.5: rounding all the edges and fitting them to a refined mesh size of 5 micrometers.

Accoring to [9], to get a realistic E-field value from the simulations, the E-field is evaluated at a point, 50 micrometers from the metallization edge, this is illustrated in the simulation reults. Right next to the edge, the generated E-fields of the idealized simulation will surpass the electrical strengths of the normally used covering materials (for silicone gel, these values are [9], typically 26.7 kV / mm). Experiments have shown that partial discharge does not occur all along this critical edge [9]. Not included in the simulations, are defects. Defects in the metallizations are usually the main reason for PDs along the metallization.

Figure 3.6 demonstrates a simulation, where COMSOL identifies the highest producest E-Field in the model. This is done to identify which one of the two metallizations can be deleted.

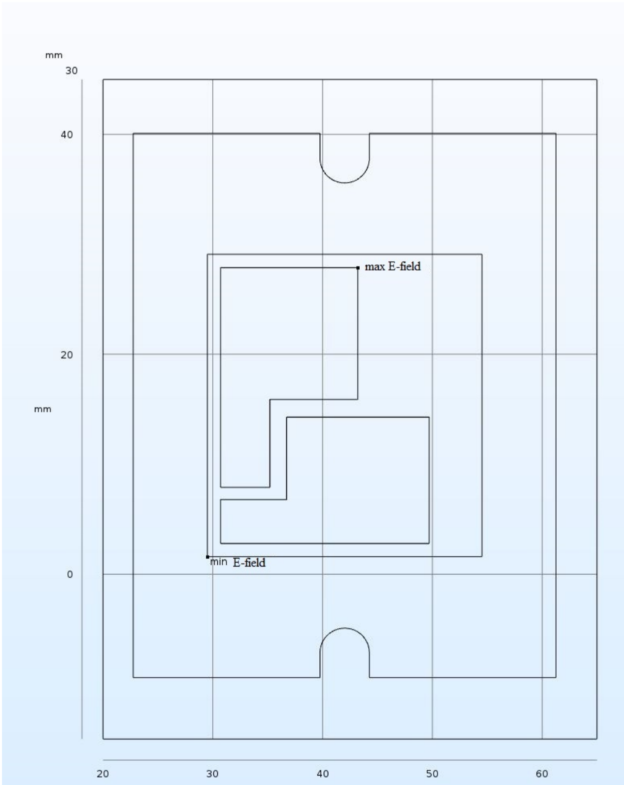


Figure 3.6: 3D model of MOSFET module APTMC120AM44CT1AG from COMSOL. Simulating minimum and maximum E-Fields, without any Electrodes, dies or bondwires, to locallize the critical areas.

The upper copper metallization is illustrated in figure 3.2. The upper copper metallization which produces the highest E-field, i s k ept, w hile t he o ther o ne is deleted, to minimize simulation computing power. The final s etup c an b e s een in figure 3.7:

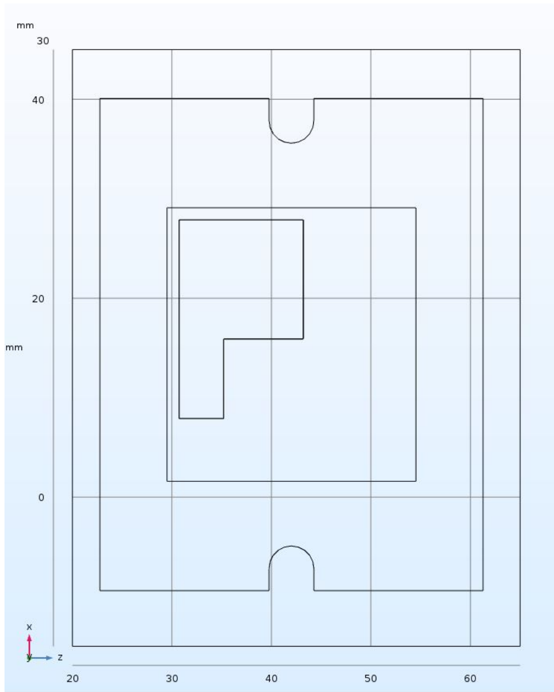


Figure 3.7: The setup used for all of the simulations.

Figure 3.7shows the setup that is used for all of the simulations.

3.2 Cases and results

This section will investigate and simulate two different cases (Case 1 and 2). The cases simulate the actual setup of the MOSFET power module. The procedure for evaluating the electric field strength has been discussed in the previous chapter. To make a reliable measurement of the E-field [9] recommends measuring the E-field at a distance of 50 micrometers from the metallization edge E-Field. All the cross-sectional views are indicated in figure 3 .4. The critical zone (the triple-point), is indicated in figure 3.2. All the simulation figures can be found in Appendix B.

3.2.1 Case 1 - 10 micrometer fillet on upper metallization edges

Case 1 investigates the actual setup of the MOSFET power module. For the electrostatic simulations outlined in case 1, the upper metal layer was applied with a voltage of 1.2 kV peak. A PDIV was then simulated, using a trial-and-error method. The lower metal layer was connected to the conductive base plate, which was connected to ground potential. For high volt-age applications, electrode shapes are often optimized to minimize peaks in E-field strengths, particularly near the edges of the electrodes. Such peaks can be avoided when rounding sharp edges[22]. Figure 3.2 illustrates, the edges of the upper copper metallization, which are filletet with a radius of 10 micrometers.

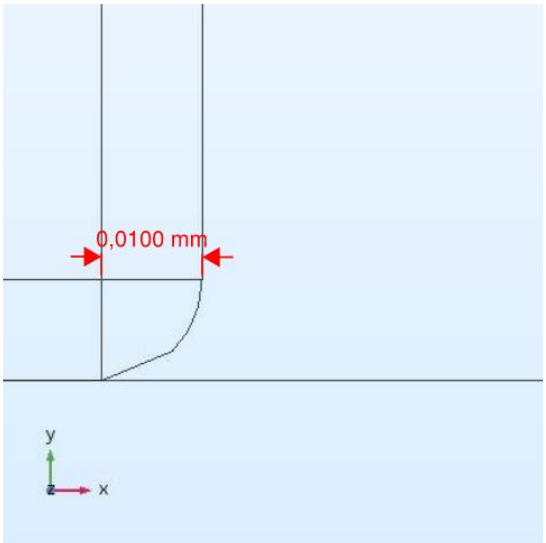
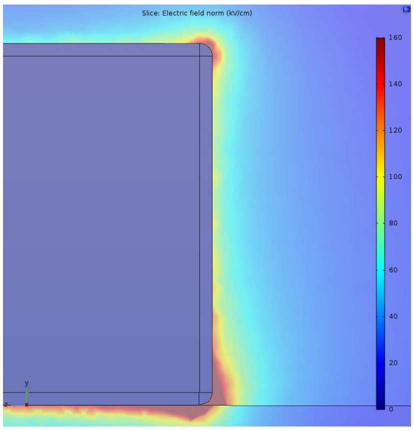


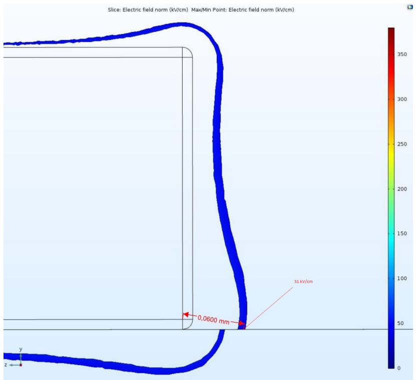
Figure 3.8: Cross-section of the critical area (Triple point), using COMSOL E-field simulation, showing an edge of 10 micrometer radius. [14]

The fillet radius of 10 micrometers, is based on the simulations done in paper [9], where the metallization edge can have a fillet radius anywhere between 5 to 100 microm-eters. The setup illustrated in figure 3.2 applies for Case 1. This solid arrange-ment is covered with silicone gel as insulation. The thickness of the materials, for case 1, can be seen in table 3.1. The material thicknesses are based on the 3D model "MicrosemiAPTMC120AM55CT1.STEP". To make an accurate simulation of the MOSFET power module, the material thicknesses must be accurately assessed, as a deviation of this can have consequences for the results, this will be shown in the "PD control" chapter, where the substrate thickness is modified. The material properties used for the simulation in case 1, are shown in table 3.2, where DuPont Performance Polymers Zytel® , Silicon coating and Silicon carbide coating are excluded.

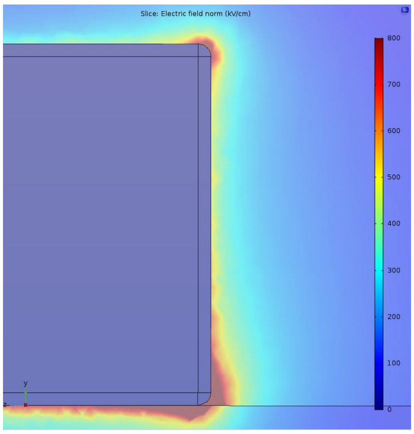
The relative permittivity, for the electrostatic simulation, is the determining factor for calculating the electric field strength. The interesting relative permittivities, for this case, are the relative permittivities for the Aluminium Nitride and silicone gel. The breakdown strengths of the materials are used for calculating the PDIV. It can be seen in table 3.2, that the breakdown strength of AIN is around twice as high, than the breakdown strength of silicone gel. The relative permittivity of AIN is around four times higher than the relative permittivity for silicone gel. The results of simulating case 1, can be seen in figure 3.9 (a-d):



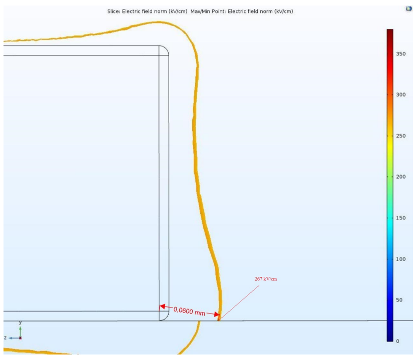
(a) E-field at operating condition, 1.2 kV



(b) E-Field at operating condition, 1.2 kV, measured 50 micrometers from edge.



(c) E-field at PDIV, 6300 V



(d) E-field at PDIV, 6300 V, measured 50 micrometers from edge.

Figure 3.9: Simulation of the E-fields in the power module, at the critical zone during normal operation and at PDIV, of case 1.

Figure 3.9(a-d), illustrates the cross section of the simulated E-field, near the triple-point for case 1. The resulting module is simulated, where the metalization edges are filletet with a radius of 10 micrometers. The upper copper metallization is applied a voltage of 1,2 kV. Fig 3.9(a), illustrates the simulation result as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 160 kV/cm. The blue line shown in figure 3.9(b), is an E-field isoline, containing data between 50 to 52 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge. The E-field measured at this distance resulted in 51 kV/cm. Fig 3.9c illustrates the simulation as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 800 kV/cm. The yellow line shown in figure 3.9d, is an E-field isoline, containing data between 265 to 270 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge. The E-field measured at this distance resulted in 267 kV/cm (the PDIV). The PDIV has been reached when an the applied voltage produces an E-field, which is higher than the electrical strength of the surrounding insulating material, for silicone gel it is 267 kV/cm. The simulated PDIV for case 1 is 6300 V, as shown in table 3.3:

Table 3.3: Case 1 - results

E- field at 1.2 kV [kV/cm]	PDIV [V]
51	6300

Table 3.3 shows the measured E-field and PDIV for case 1 . As shown, the E-field at 1200 V is 51 kV/cm, and the PDIV is 6300 V.

3.2.2 Case 2 - 30 micrometer fillet on upper metallization edges

Case 2 investigates the actual setup of the MOSFET power module. Figure 3.10 illustrates, the edges of the upper copper metallization, which are filletet with a radius of 30 micrometers.

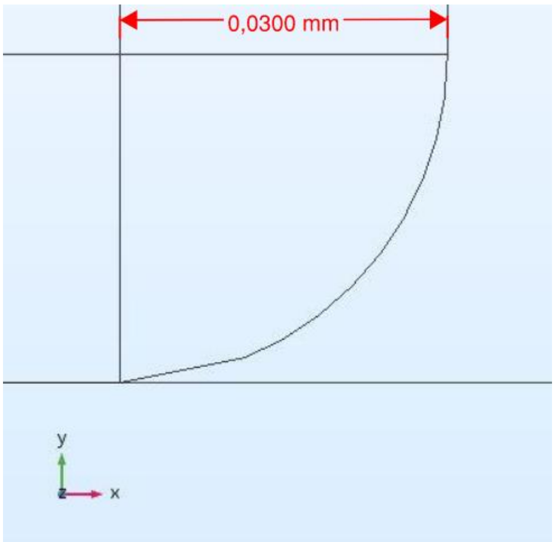
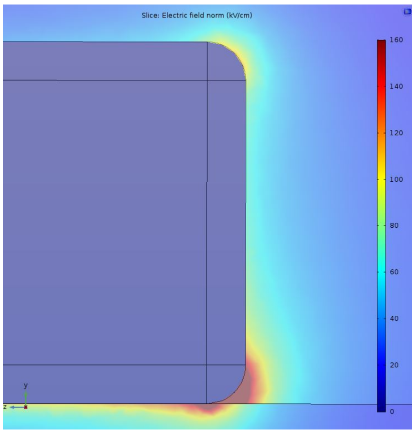


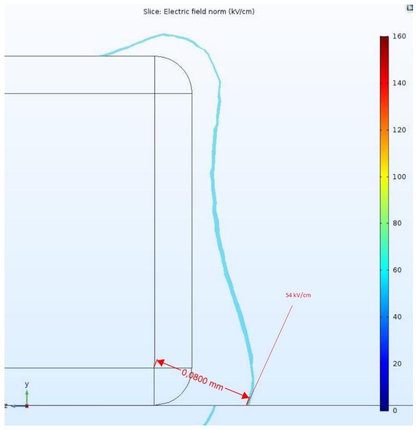
Figure 3.10: Cross section of the power module - Case 2 . [14]

The setup illustrated in figure 3.2 apply for Case 2. This solid arrangement is covered with silicone gel as an insulation. The thickness of the materials, for case 2, can be seen in table 3.1.The material properties used for the simulation in case 2, are shown in table 3.2, where DuPont Performance Polymers Zytel® , Silicon coat-ing and Silicon carbide coating are excluded.

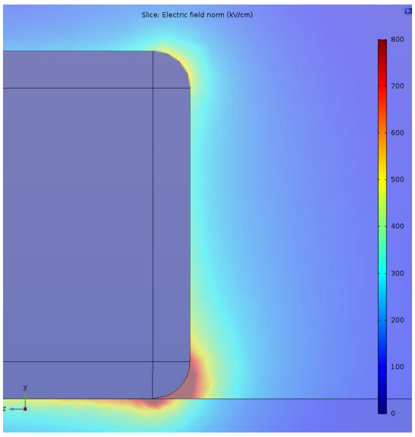
The material properties illustrated in figure 3 .2 a pply f or c ase 2 . T he interesting relative permittivities, for this case, are the relative permittivities for the Aluminium Nitride and Silicone gel. The results of simulating case 2, can be seen in figure 3.11 (a-d):



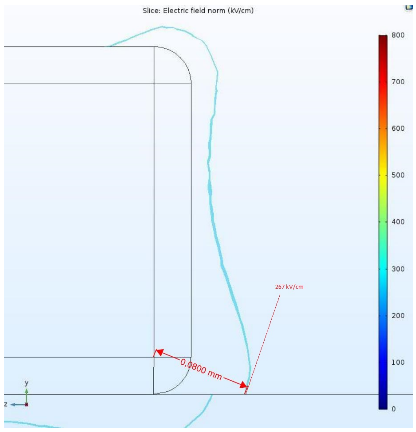
(a) E-field at operating condition, 1.2 kV



(b) E-Field at operating condition, 1.2 kV, measured 50 micrometers from edge.



(c) E-field at PDIV, 5900 V



(d) E-field at PDIV, 5900 V, measured 50 micrometers from edge.

Figure 3.11: Simulation of the E-fields in the power module, at the critical zone during normal operation and at PDIV, of case 2

Figure 3.11 (a-d), illustrates the cross section of the simulated E-field, near the triple-point for case 2. The resulting module is simulated, where the metalization edges are filletet with a radius of 30 micrometers. The upper copper metallization is applied a voltage of 1,2 kV. Fig 3.11(a), illustrates the simulation result as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 160 kV/cm. The light blue line shown in figure 3.11(b), is an E-field isoline, containing data between 52 to 54 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge. The E-field measured at this distance resulted in 54 kV/cm. Fig 3.11(c) illustrates the simulation as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 800 kV/cm. The light blue line shown in figure 3.11(d), is an E-field isoline, containing data between 265 to 270 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge. The E-field measured at this distance resulted in 267 kV/cm (the PDIV). The PDIV has been reached when a voltage produces an E-field, that is higher than the electrical strength of the surrounding insulating material, 267 kV/cm for silicone gel. The simulated PDIV for case 2 is 5900 V, as shown in table 3.4:

Table 3.4: Case 2 - results

E- field at 1.2 kV [kV/cm]	PDIV [V]
54	5900

Table 3.4 shows the measures E-field and PDIV for case 2. As shown, the E-field at 1200 V is 54 kV/cm, and the PDIV is 5900 V.

3.3 Summary

Table 3.5: Simulation results

Case	E-Field at 1.2 kV [kV/cm]	PDIV [V]
Case 1	51	6300
Case 2	54	5900

The first two cases, include a simulation of the actual setup of the MOSFET power module. The PDIV for case 1 (using 10 micrometer fillet) was simulated to be 6300 V, while the PDIV for case 2 (using 30 micrometer fillet) was simulated to be 5900 V. The simulations show that the PDIV increased, after increasing the fillet radius. This does not follow the proportionality rule, stated in eq. 3.1. This problem can loosely be compared to the rod to plane configuration, where the mean E-field produced is proportional to the applied voltage divided to the rod diameter, at a given distance between them. As the rod diameter increases, the mean E-field decreases, but over a larger area. When using the measurement method 50-micrometers-from-edge, there is a chance that the measurement point is still within the area between the copper electrode and the AIN subtrate plane, giving a higher E-field measurement. The simulations in chapter 5, will thus be done according to case 1, using a 10 micrometer fillet. The parameters which can be modified for improvements are:

- Copper thickness
- Substrate thickness
- Insulating gel permittivity
- Grounding the triple-point with a semiconductor

Chapter 4

Laboratory PD test

In this chapter, the PD test on the SiC MOSFET module will be represented and analysed using measured PRPD patterns. The main scope of this chapter is to study PD behavior of SiC MOSFET insulation and verify the COMSOL electric field computation in the module presented in the previous chapter.

4.1 Test setup

In order to perform the partial discharge test on the SiC MOSFET module, the PD test circuit with integrated measuring system was used. The description of the PD test circuit with measuring system is given in chapter 2. There are some specific requirements indicated by IEC 60270 standard that must be fulfilled by measuring system [14], [16]:

- In order to measure the specified PD magnitude at the specified test voltage, the coupling capacitor C_k should be PD-free and designed with low inductance.
- In order to measure the specified PD magnitude at the specified test voltage, the HV source should exhibit a quite low level of *background noise*;
- In order to measure the specified PD magnitude at the specified test voltage, HV connections should exhibit a quite low level of *background noise*;

The schematic of the PD measurement circuit used in the laboratory is shown in Figure 4.1.

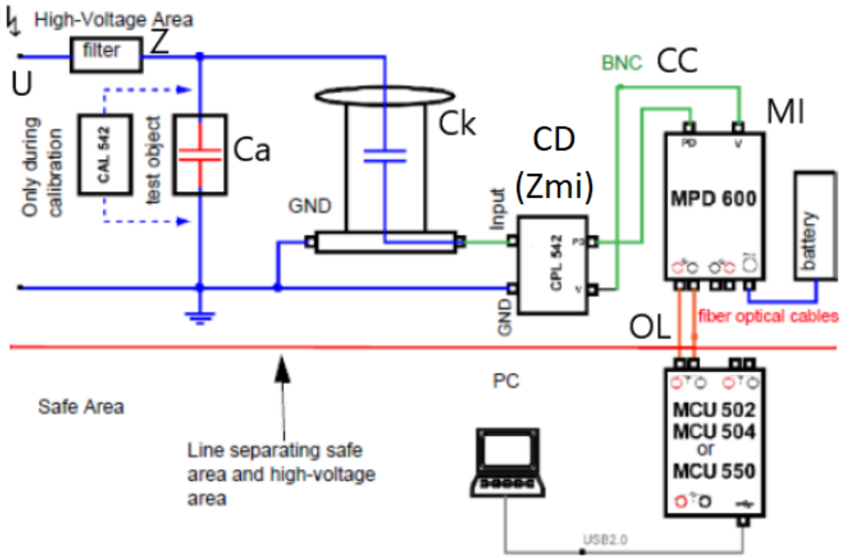


Figure 4.1: Measurement system within the PD test circuit

The high-voltage source U, is an AC power source that applied between 0 and 5 kV to the test object. The low-pass filter Z between the power source and the rest of the circuit reduces the high-frequency noise and disconnects the test object and coupling capacitor during the partial discharges. The test object C_a is in parallel with the coupling capacitor C_k. The coupling capacitor cancels the voltage drop across the test object during the quick discharges. The input impedance Z_{mi} of the coupling device CD to the measuring device MI transfers the impulse current into voltage and supresses the interferences of power frequency and harmonics from the source. The measuring instrument MI calculates the PD charges and transmits the information through an optical cable. An optical cable OL is used so the test circuit is electrically isolated, which improves the accuracy.

Before performing the test, a calibration of the measuring system for the *apparent charge* q measurement was made, in order to reduce the measuring errors during the PD test. It was done by injecting a calibrating charge $q_0 = 50$ pC across the terminals of the test object using a PD calibrator.

The test object was a half-bridge SiC MOSFET module (Microsemi APTMC55CT1AG), rated at 1.2 kV and 55 A. Its top view can be seen in Figure 4.2.

Figure 4.2: Top view of the SiC module (Microsemi APTMC55CT1-AG) and its connecting method to the measurement circuit

Partial discharge measurement was performed according to IEC 61287 standard, which procedure is fully described in chapter 2. Based on that the electrical terminals (gate, drain and source) were short circuited and PD signals were measured after the test voltage was applied between the connected together terminals and the module's base plate. This can also be seen in Figure 4.2.

In order to apply the required voltage to the module, voltage calibration was done as well. Multimeter with HV probe was used to downscale the voltage.

4.2 Results

All below quoted voltage values correspond to the root mean square (RMS) value. Firstly, as stated in the IEC 1287 standard, an applied AC 50 Hz test voltage was increased to 1.27 kV. The measured PRPD is shown in Figure 4.3.

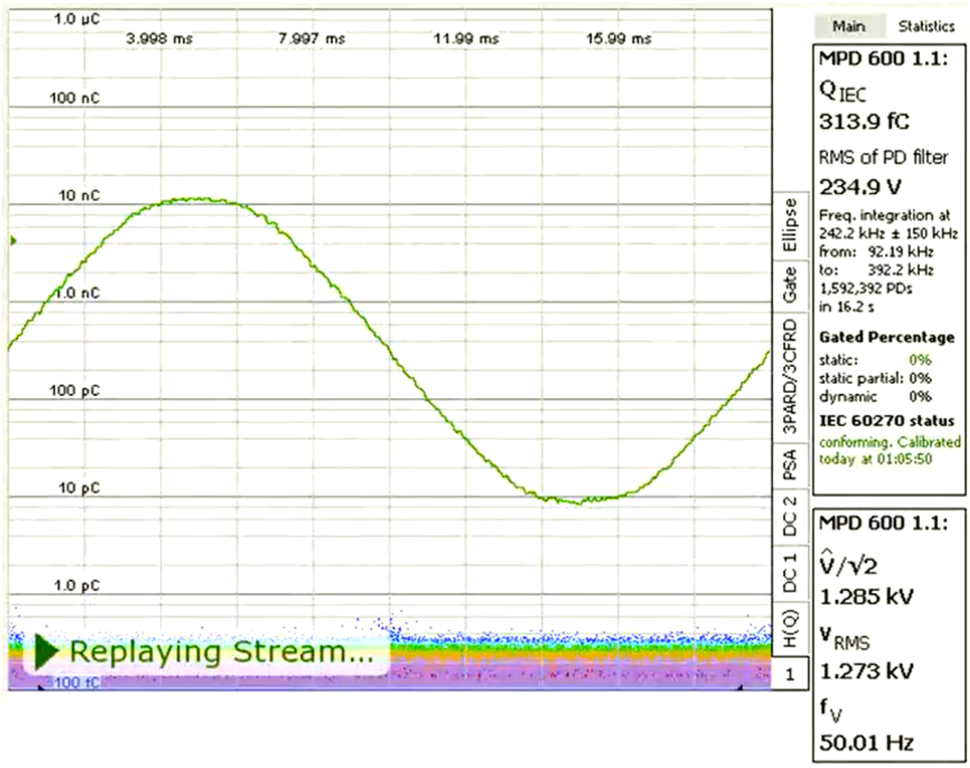


Figure 4.3: PRPD pattern of the SiC module at a voltage of 1.27 kV_{rms} (IEC 1287)

It can be seen that the average amount of discharge is 313.9 fC, which is much lower than the detection threshold of the system (10 pC). This value is close to the charge of PD detection noise. Thus, no PD is triggered.

Afterwards, according to the next step of the IEC 1287 PD test procedure, the applied voltage was decreased to 0.93 kV. The recorded PD pattern is represented in Figure 4.4.

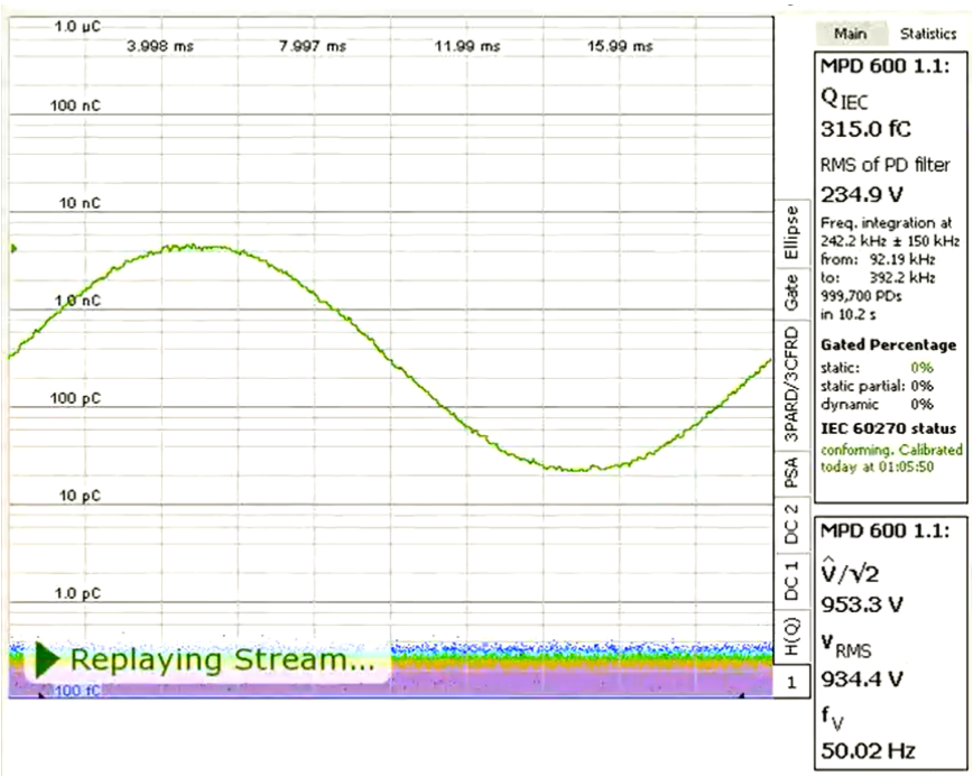


Figure 4.4: PRPD pattern of the SiC module at a voltage of 0.93 kV_{rms} (IEC 1287)

At the voltage of 0.93 kV the average number of PD charges is 315 fC. Again there is no PD activity, therefore, the SiC MOSFET module passed the partial discharge test to IEC 1287.

Nonetheless, in order to define the discharge inception voltage (PDIV), the applied test voltage have been increased further (up to about 5 kV in steps of 0.5 kV). It can be seen in Figure 4.5.

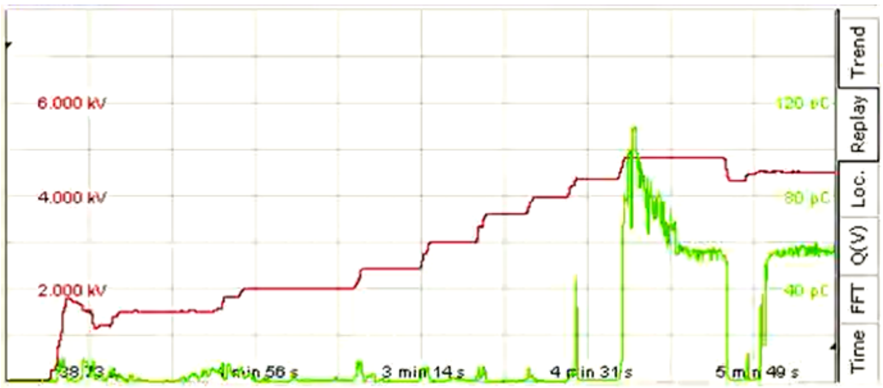


Figure 4.5: The applied test voltage in steps of 0.5 kV for PDIV defining (red) with the corresponding average number of PD charges (green)

No PD activity was witnessed at higher voltages (up to about 4.6 kV). The PDIV was close to around 4.7 kV. The obtained PD pattern is shown in Figure 4.6, where the average magnitude of PDs exceeds 10 pC (36.10 pC).

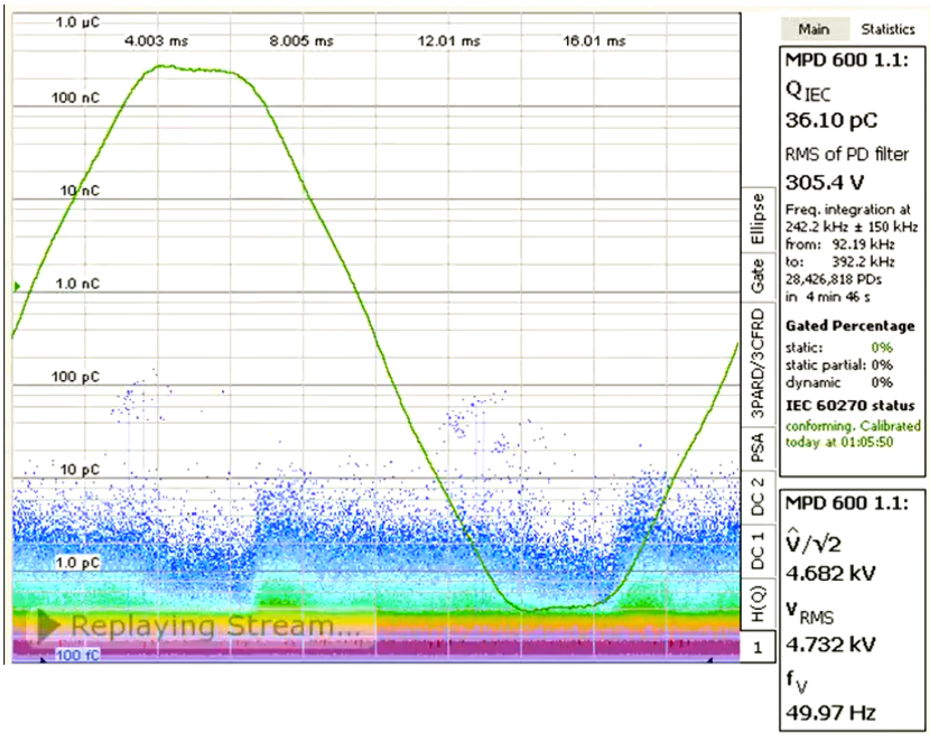


Figure 4.6: PRPD pattern of the SiC module with PDIV at a voltage of 4.7 kV_{rms}

After that the intensity and number of discharges increased drastically with rising voltage, as it is seen in Figure 4.7 at about 4.8 kV.

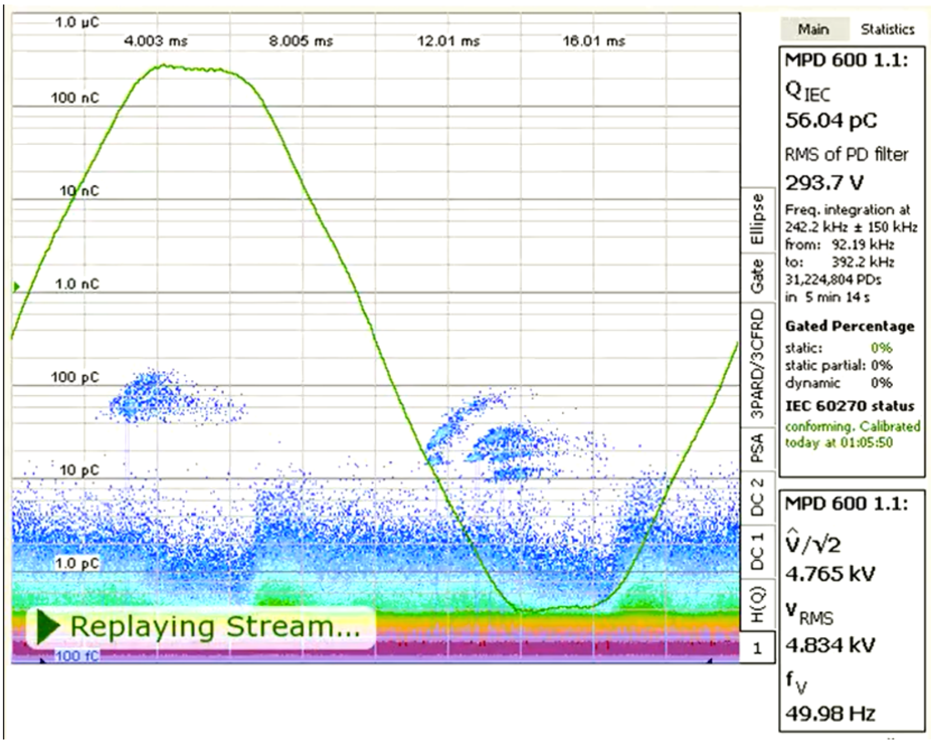


Figure 4.7: PRPD pattern of the SiC module at a voltage of 4.8 kV_{rms}

The average number of discharges increased by about 55 % (56.04 pC). Furthermore, PD took place at a phase between zero and a voltage peak (between 0-90°and 180-270°). The shape of the PD charges can be explained by the surface discharge at the interface between the silicone gel and the substrate. This type of PD is explained in chapter 2. According to the PD patterns, they are most likely occur at the interface between the metalized ceramic and the silicone gel. Furthermore, the COMSOL electric field distribution simulations showed the highest electric field strength at this triple point.

4.3 Summary

In this chapter, the PD measurement in the SiC MOSFET module was introduced. This was done in order to analyse the PD behavior of module's insulation and validate the electric stress inside the module simulated in COMSOL FEM software. Initially, the MOSFET module was tested according to IEC 1287 standard. As a result, no PD signals were triggered at rated voltage. Thus, the voltage was further increased to ignite PDs. The PDIV was observed at about 4.7 kV rms. Then, at higher voltage (around 4.8 kV rms) the strong rise of number and strength of discharges was seen. Finally, by analysing the PRPD pattern of the observed partial discharge phenomena, it was suggested that the surface discharge took place at the the interface between the metalized ceramic and the silicone gel, where the highest magnitude of electric field was obtained via COMSOL simulations.

Chapter 5

PD control

This chapter will investigate improvement techniques, used to decrease the E-fields in a power module. The implemented techniques also increase the PDIV, either to lower or eliminate PDs in a MOSFET popwer module. This chapter will investigate and simulate seven different cases (case 3-9). The seven cases are simulated and the improvements will be investigated. To make a reliable measurement of the E-field [9] recommends measuring the E-field at a distance of 50 micrometers from the metallization edges. All the simulation figures can be found in Appendix B.

5.1 Cases and results

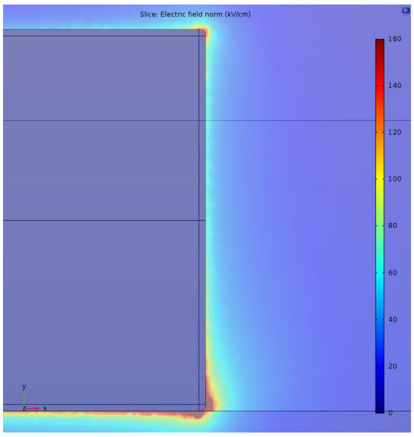
5.1.1 Case 3 - Doubling the upper copper metallization thickness

Case 3 investigates doubling the thickness of the upper copper metallization in the setup of the MOSFET power module. The setup in figure 3.1 applies to case 3. This solid arrangement was covered with silicone gel as an insulation. The thickness of these materials, for case 3, can be seen in table 5.1:

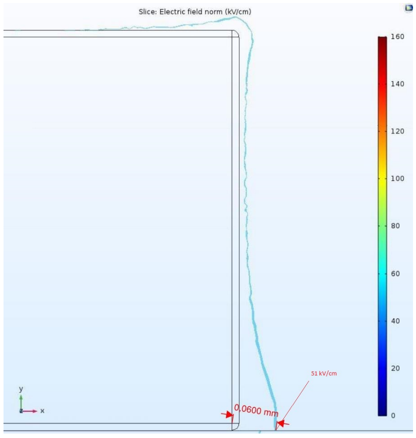
Table 5.1: Case 3 - Material thickness

Material	Thickness [mm]
Copper (upper)	0,56
Copper (Lower)	0,28
AIN	0,63
Solder	0,2
Baseplate	0,22

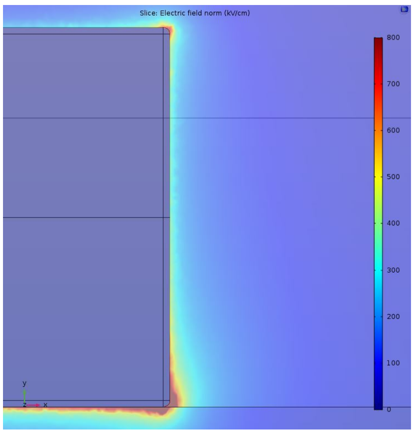
The material properties illustrated in figure 3.2 apply for case 3. The relative permittivity, for the electrostatic simulation, is the determining factor for calculating the electric field strength. The interesting relative permittivities, for this case, are the relative permittivities for the Aluminium Nitride and Silicone gel. The results of simulating case 3, can be seen in figure 5.1 (a-d):



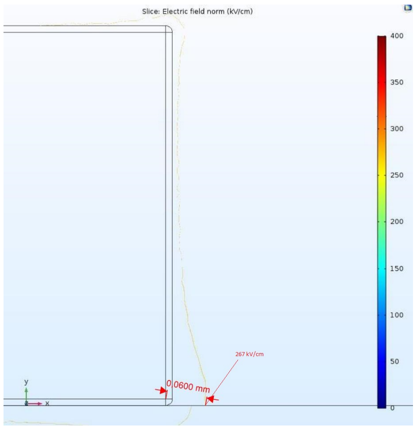
(a) E-field at operating condition, 1.2 kV



(b) E-Field at operating condition, 1.2 kV, measured 50 micrometers from edge.



(c) E-field at PDIV, 6300 V



(d) E-field at PDIV, 6300 V, measured 50 micrometers from edge.

Figure 5.1: Simulation of the E-fields in the power module, at the critical zone during normal operation and at PDIV, of case 3

Figure 5.1 (a-d), illustrates the cross section of the simulated E-field, near the triple-point for case 3. The resulting module is simulated, where the metalization edges are filletet with a radius of 10 micrometers. The upper copper metallization is applied a voltage of 1,2 kV. Fig 5.1(a), illustrates the simulation result as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 160 kV/cm. The blue line shown in figure 5.1(b), is an E-field isoline, containing data between 50 to 52 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge. The E-field measured at this distance resulted in 51 kV/cm. Fig 5.1(c) illustrates the simulation as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 800 kV/cm. The yellow line shown in figure 5.1(d), is an E-field isoline, containing data between 265 to 270 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge. The E-field measured at this distance resulted in 267 kV/cm (the PDIV). The PDIV has been reached when an the applied voltage produces an E-field, which is higher than the electrical strength of the surrounding insulating material, for silicone gel it is 267 kV/cm. The simulated PDIV for case 3 is 6300 V, as shown in table 5.2:

Table 5.2: Case 3 - results

E- field at 1.2 kV [kV/cm]	PDIV [V]
51	6300

Table 5.2 shows the measured E-field and PDIV for case 3. The E-field at 1200 V is 51 kV/cm, and the PDIV is 6300 V.

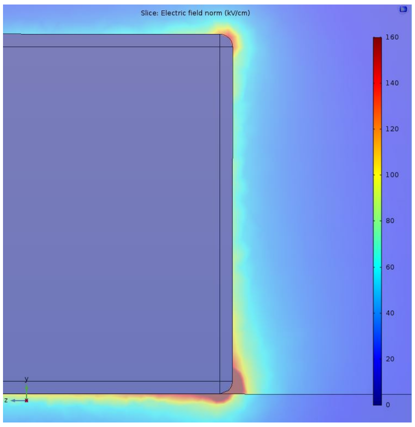
5.1.2 Case 4 - Doubling AIN substrate thickness

Case 4 investigates the setup of the MOSFET power module, where the AIN substrate is doubled in thickness. The setup illustrated in figure 3.2, applies for case 4. This solid arrangement is covered with silicone gel as an insulation. The thickness of these materials, for case 4, can be seen in table 5.4:

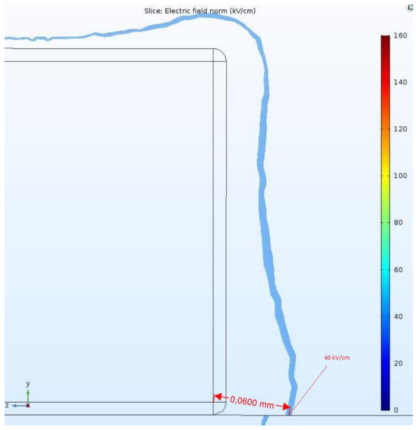
Table 5.3: Case 4 - Material thickness

Material	Thickness [mm]
Copper (upper)	0,28
Copper (Lower)	0,28
AIN	1,26
Solder	0,2
Baseplate	0,22

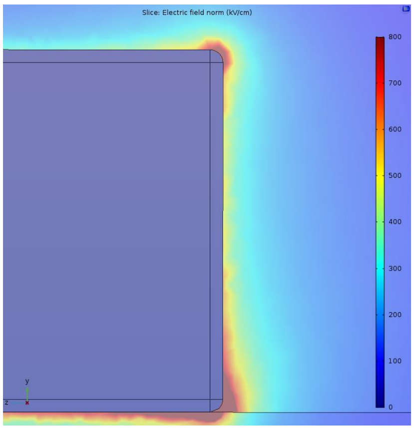
The material properties illustrated in table 3.2 apply for case 4, where DuPont Performance Polymers Zytel®, Silicon coating and Silicon carbide coating are excluded. The interesting relative permittivities, for this case, are the relative permittivities for the Aluminium Nitride and silicone gel. The results of simulating case 4, can be seen in figure 5.2 (a-d):



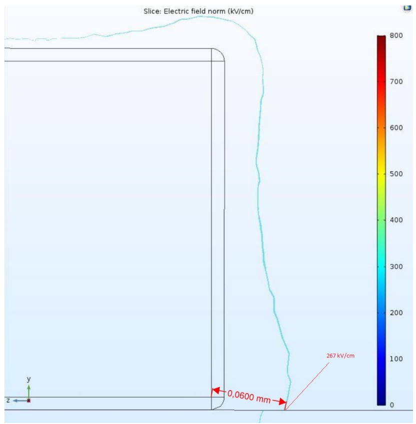
(a) E-field at operating condition, 1.2 kV



(b) E-Field at operating condition, 1.2 kV, measured 50 micrometers from edge.



(c) E-field at PDIV, 8000 V



(d) E-field at PDIV, 8000 V, measured 50 micrometers from edge.

Figure 5.2: Simulation of the E-fields in the power module, at the critical zone during normal operation and at PDIV, of case 4

Figure 5.2 (a-d), illustrates the cross section of the simulated E-field, near the triple-point for case 4. The resulting module is simulated, where the metalization edges are filletet with a radius of 10 micrometers. The upper copper metallization is applied a voltage of 1,2 kV. Fig 5.2(a), illustrates the simulation result as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 160 kV/cm. The blue line shown in figure 5.2(b), is an E-field isoline, containing data between 39 to 40 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge.

The E-field measured at this distance resulted in 40 kV/cm. Fig 5.2(c) illustrates the simulation as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 800 kV/cm. The yellow line shown in figure 5.2(d), is an E-field isoline, containing data between 265 to 270 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge. The E-field measured at this distance resulted in 267 kV/cm (the PDIV). The PDIV has been reached when an the applied voltage produces an E-field, which is higher than the electrical strength of the surrounding insulating material, for silicone gel it is 267 kV/cm. The simulated PDIV for case 4 is 8000 V, as shown in table 5.4:

Table 5.4: Case 4 - results

E- field at 1.2 kV [kV/cm]	PDIV [V]
40	8000

Table 5.4 shows the measured E-field and PDIV for case 4.The E-field at 1200 V is 40 kV/cm, and the PDIV is 8000 V.

5.1.3 Case 5 - Using a silicon coating

Case 5 investigates the setup of the MOSFET power module, where a silicon coating is used. The setup of the MOSFET power module can be seen in figure 5.5.

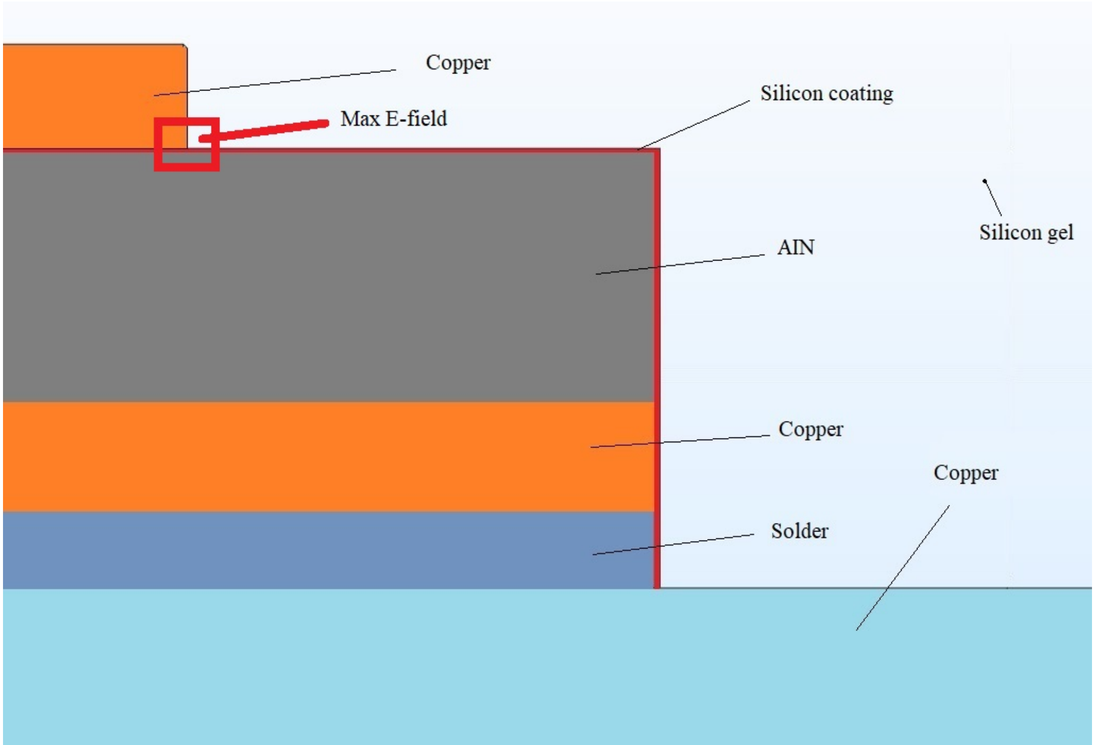


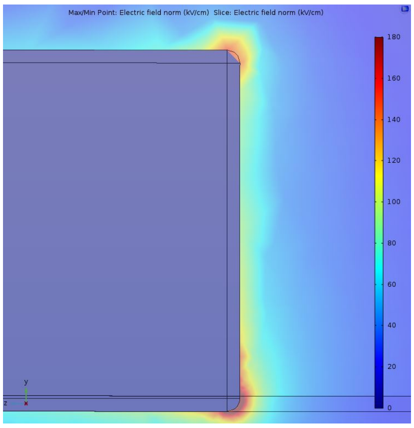
Figure 5.3: Cross section of the power module - Case 5. [14]

The setup in figure 5.5 has a metallization (Copper) located on top of an insulating ceramic substrate. There is a further copper metallization at the bottom of this substrate that is soldered to a base layer. The technique used in this case, is to add a silicon coating along the surface, which connects the high potential to the ground. This solid arrangement is covered with silicone gel as an insulation. The thickness of these materials, for case 4, can be seen in table 5.7:

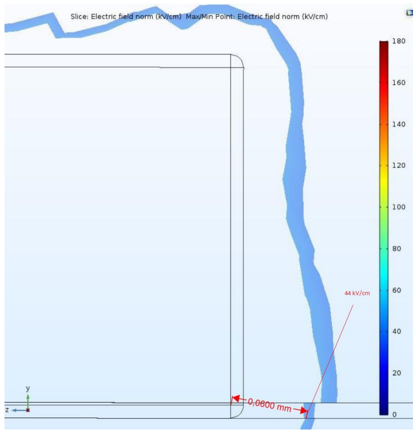
Table 5.5: Case 5 - Material thickness

Material	Thickness [mm]
Copper (upper)	0,28
Copper (Lower)	0,28
AIN	0,63
Silicon coating	0,012
Solder	0,2
Baseplate	0,22

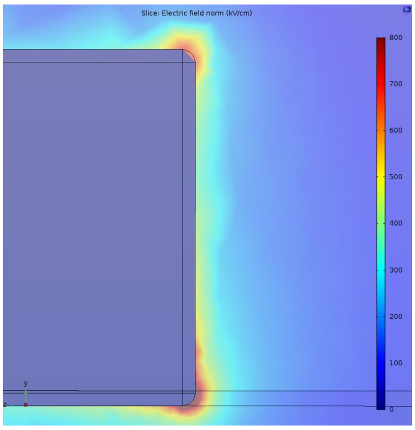
The material thicknesses are based on the 3D model "MicrosemiAPTMC120AM55CT1.STEP", where a silicon coating is added along the surface of the AIN and the upper copper metallization, and the high potential is connected to the ground. The material properties used for the simulation in case 5, are shown in table 3.2. The relative permittivities of interest, for this case, are the relative permittivities of the silicon coating, Aluminium Nitride and silicone gel. The breakdown strength of silicon coating is lower than the breakdown strength of silicone gel. The relative permittivity of AIN is around four times higher than the relative permittivity for silicone gel. The relative permittivity of silicon coating is around five times higher than the relative permittivity of silicone gel. The results of simulating case 5, is illustrated in figure 5.6 (a-e):



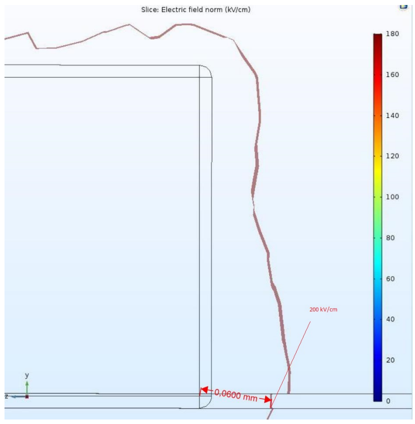
(a) E-field at operating condition, 1.2 kV



(b) E-Field at operating condition, 1.2 kV, measured 50 micrometers from edge.



(c) E-field at PDIV, 5400 V



(d) E-field at PDIV, 5400 V, measured 50 micrometers from edge.

Figure 5.4: Simulation of the E-fields in the power module, at the critical zone during normal operation and at PDIV, of case 5

Figure 5.4 (a-d), illustrates the cross section of the simulated E-field, near the triple-point for case 5. The resulting module is simulated, where the metalization edges are filletet with a radius of 10 micrometers. The upper copper metallization is applied a voltage of 1,2 kV DC. Fig 5.4(a), illustrates the simulation result as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 160 kV/cm. The blue line shown in figure 5.4(b), is an E-field isoline, containing data between 40 to 45 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge. The E-field measured at this distance resulted in 44 kV/cm. Fig 5.4(c) illustrates the simulation as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 800 kV/cm. The red line shown in figure 5.4(d), is an E-field isoline, containing data between 195 to 200 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge. The E-field measured at this distance resulted in 200 kV/cm (the PDIV). The PDIV has been reached when an the applied voltage produces an E-field, which is higher than the electrical strength of the surrounding insulating material, for silicon coating it is 200 kV/cm. The simulated PDIV for case 5 is 5400 V, as shown in table 5.6:

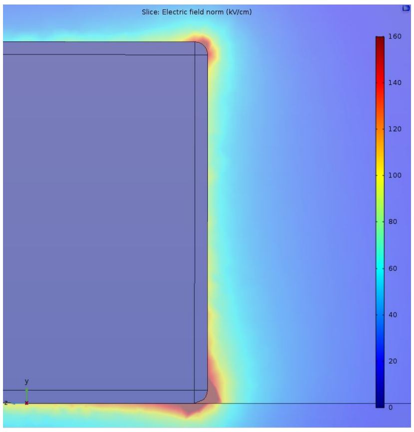
Table 5.6: Case 5 - results

E- field at 1.2 kV [kV/cm]	PDIV [V]
44	5400

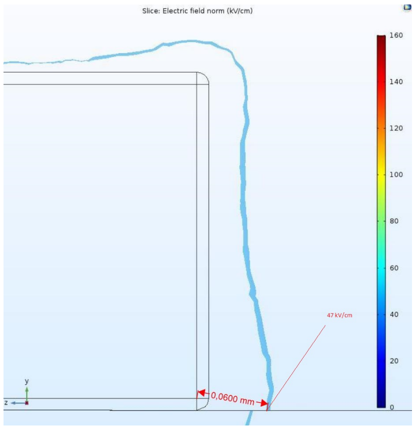
Table 5.6 shows the measured E-field and PDIV for case 5. The E-field at 1200 V is 44 kV/cm, and the PDIV is 5400 V.

5.1.4 Case 6 - Using a performance resin to replace the silicon gel

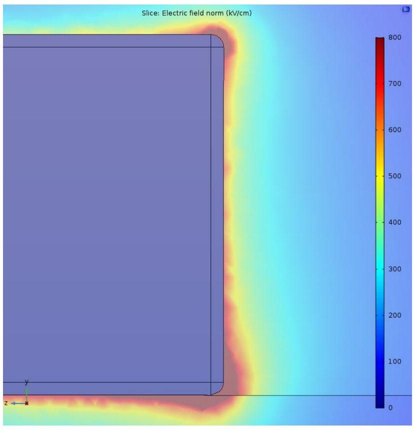
Case 6 investigates replacing the silicon gel with a high performance resin, in the MOSFET power module. The setup of the stacked structure is illustrated in figure 3.2, and it applies for case 6. This solid arrangement is covered with a high performance resin as insulation. The thickness of the layers in the stacked structure, for case 6, are stated in table 3.2. The material properties are stated in table 3.2 apply for case 6. For this case, the interesting relative permittivities are the high performance resin and Aluminium Nitride. It it is stated in table 3.2, that the breakdown strength of AIN is around twice as high, than the breakdown strength of the high performance resin. The relative permittivity of AIN is around twice as high as the high reltavie permittivity for the high performance resin. The results of simulating case 6, can be seen in figure 5.5 (a-d):



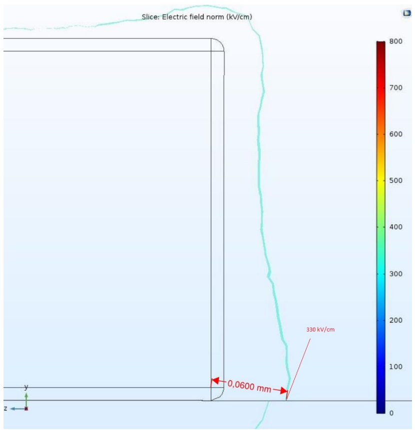
(a) E-field at operating condition, 1.2 kV



(b) E-Field at operating condition, 1.2 kV, measured 50 micrometers from edge.



(c) E-field at PDIV, 8400 V



(d) E-field at PDIV, 8400 V, measured 50 micrometers from edge.

Figure 5.5: Simulation of the E-fields in the power module, at the critical zone during normal operation and at PDIV, of cacse 6

Figure 5.5 (a-d), illustrates the cross section of the simulated E-field, near the triple-point for case 6. The resulting module is simulated, where the metalization edges are filletet with a radius of 10 micrometers. The upper copper metallization is applied a voltage of 1,2 kV. Fig 5.5(a), illustrates the simulation result as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 160 kV/cm. The light blue line shown in figure 5.5(b), is an E-field isoline, containing data between 45 to 47 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge. The E-field measured at this distance resulted in 47 kV/cm. Fig 5.5(c) illustrates the simulation as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 800 kV/cm. The light blue line shown in figure 5.5(d), is an E-field isoline, containing data between 325 to 330 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge. The E-field measured at this distance resulted in 330 kV/cm (the PDIV). The PDIV has been reached when an the applied voltage produces an E-field, which is higher than the electrical strength of the surrounding insulating material, for silicone gel it is 330 kV/cm. The simulated PDIV for case 6 is 8400 V, as shown in table 5.8:

Table 5.7: Case 6 - results

E- field at 1.2 kV [kV/cm]	PDIV [V]
47	8400

Table 5.8 shows the measured E-field and PDIV for case 6. The E-field at 1200 V is 47 kV/cm, and the PDIV is 8400V.

5.1.5 Case 7 - Doubling AIN substrate thickness and using silicon coating

Case 7 investigates the setup of the MOSFET power module, where a silicon coating is used and the AIN substrate thickness is doubled. The setup of the stacked structure of the MOSFET power module is illustrated figure 5.6.

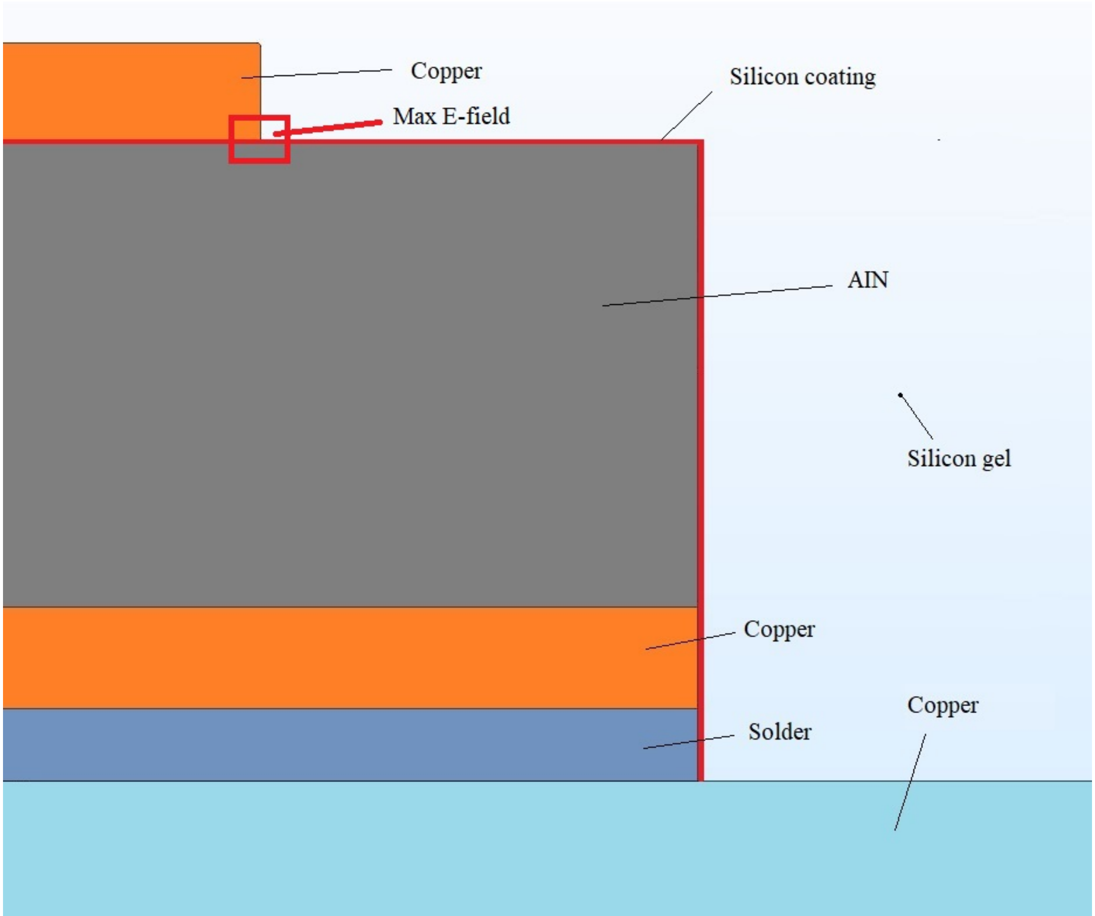


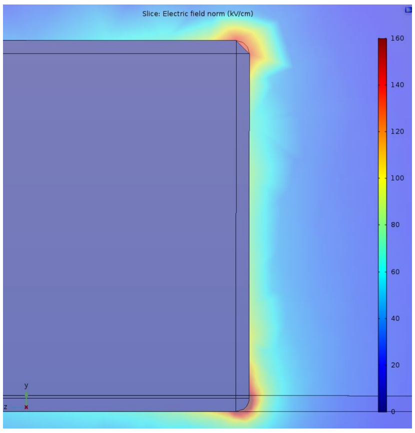
Figure 5.6: Cross section of the power module - Case 7 . [14]

The setup in figure 5.6 has a metallization (Copper) located on top of an insulating ceramic substrate. There is a further copper metallization at the bottom of this substrate that is soldered to a base layer. The technique used in this case, is to add a silicon coating along the surface, which connects the high potential to the ground. The thickness of the AIN substrate is doubled. This solid arrangement is covered with silicone gel as insulation. The thickness of the materials, for case 7, can be seen in table 5.8:

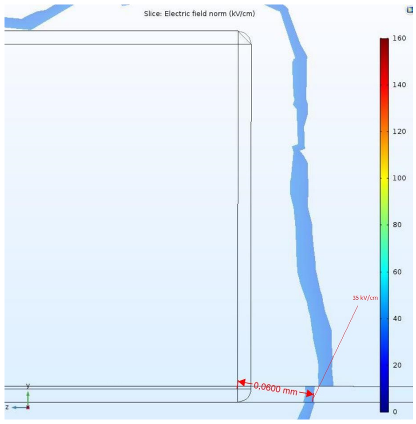
Table 5.8: Case 7 - Material thickness

Material	Thickness [mm]
Copper (upper)	0,28
Copper (Lower)	0,28
AIN	1,26
Silicon	0,12
Solder	0,2
Baseplate	0,22

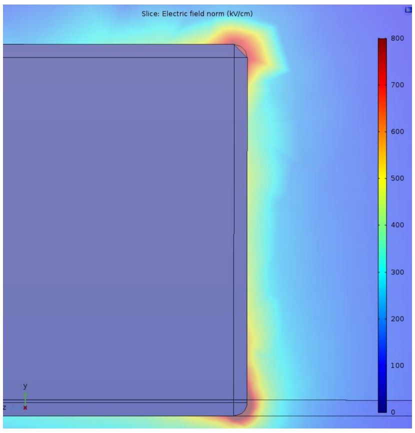
The material properties shown in table 3.2, apply for this case. The interesting relative permittivities, for this case, are the relative permittivities of the silicon coating, Aluminium Nitride and silicone gel. The results of simulating case 7, are illustrated in figure 5.7 (a-d):



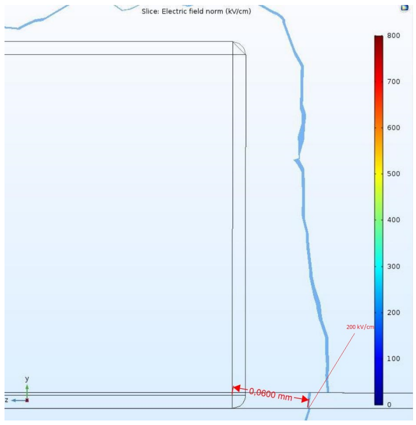
(a) E-field at operating condition, 1.2 kV



(b) E-Field at operating condition, 1.2 kV, measured 50 micrometers from edge.



(c) E-field at PDIV, 6800 V



(d) E-field at PDIV, 6800 V, measured 50 micrometers from edge.

Figure 5.7: Simulation of the E-fields in the power module, at the critical zone during normal operation and at PDIV, of case 7

Figure 5.7 (a-d), illustrates the cross section of the simulated E-field, near the triple-point for case 7. The resulting module is simulated, where the metalization edges are filletet with a radius of 10 micrometers. The upper copper metallization is applied a voltage of 1,2 kV peak. Fig 5.7(a), illustrates the simulation result as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 160 kV/cm. The light blue line shown in figure 5.7(b), is an E-field isoline, containing data between 35 to 40 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge.

The E-field measured at this distance resulted in 35 kV/cm. Fig 5.7(c) illustrates the simulation as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 800 kV/cm. The light blue line shown in figure 5.7(d), is an E-field isoline, containing data between 195 to 200 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge. The E-field measured at this distance resulted in 200 kV/cm (the PDIV). The PDIV has been reached when an the applied voltage produces an E-field, which is higher than the electrical strength of the surrounding insulating material, for silicone gel it is 200 kV/cm. The simulated PDIV for case 7 is 6800 V, as shown in table 5.10:

Table 5.9: Case 7 - results

E- field at 1.2 kV [kV/cm]	PDIV [V]
35	6800

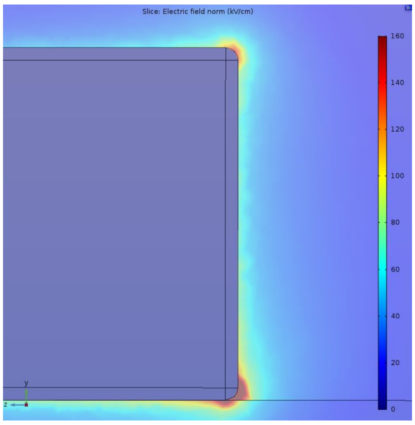
Table 5.10 shows the measured E-field and PDIV for case 7. The E-field at 1200 V is 35 kV/cm, and the PDIV is 6800 V.

5.1.6 Case 8 - Using a performance resin to replace the silicon gel and doubling the AIN substrate thickness

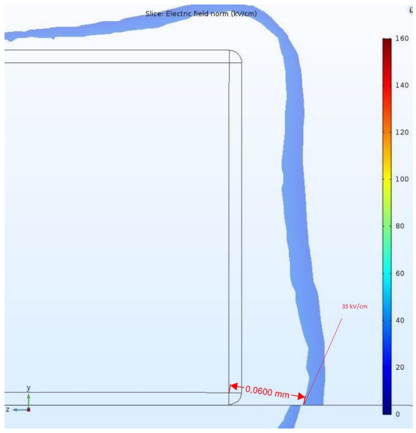
Case 8 investigates replacing the silicon gel with a high performance resin and doubling the AIN substrate thickness, in the MOSFET power module. The setup illustrated in figure 3.2 applies for case 8. This solid arrangement is covered with a high performance resin as insulation. the material thicknesses stated in table 3.1 apply for case 8. The material properties stated in table 3.2 apply for case 8, where the silicone gel is replaced with a high performance resin Dupont Performance Polymers Zytel®.

The relative permittivity, for the electrostatic simulation, is the determining factor for calculating the electric field strength. The interesting relative permittivities, for this case 8, are the relative permittivities for the high performance resin and Aluminium

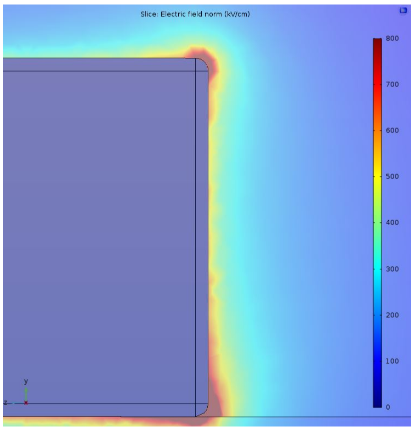
Nitride. The breakdown strengths of the materials are used for calculating the partial discharge inception voltage (PDIV). The interesting material properties for this case, are the material properties of the performance resin and the AIN. The simulation results for this case, are illustrated in figure 5.9(a-d):



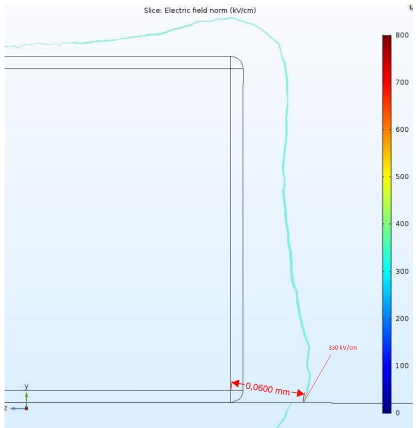
(a) E-field at operating condition, 1.2 kV



(b) E-Field at operating condition, 1.2 kV, measured 50 micrometers from edge.



(c) E-field at PDIV, 11300 V



(d) E-field at PDIV, 11300 V, measured 50 micrometers from edge.

Figure 5.8: Simulation of the E-fields in the power module, at the critical zone during normal operation and at PDIV, of case 8 - 1 MHz

Figure 5.8 (a-d), illustrates the cross section of the simulated E-field, near the triple-point for case 8. The resulting module is simulated, where the metalization edges are filletet with a radius of 10 micrometers. The upper copper metallization is applied a voltage of 1,2 kV peak. Fig 5.8(a), illustrates the simulation result as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 160 kV/cm. The blue line shown in figure 5.8(b), is an E-field isoline, containing data between 30 to 35 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge. The E-field measured at this distance resulted in 35 kV/cm. Fig 5.8(c) illustrates the simulation as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 800 kV/cm. The light blue line shown in figure 5.8(d), is an E-field isoline, containing data between 325 to 330 kV/cm. The measurement is taken 60 micrometers from the center of radius of the fillet, resulting in 50 micrometers from the edge. The E-field measured at this distance resulted in 330 kV/cm (the PDIV). The PDIV has been reached when an the applied voltage produces an E-field, which is higher than the electrical strength of the surrounding insulating material, for silicone gel it is 330 kV/cm. The simulated PDIV for case 8 is 11300 V, as shown in table 5.10:

Table 5.10: Case 8 - results

	E- field at 1.2 kV [kV/cm]	PDIV [V]
35	11300	

Table 5.10 shows the measured E-field and PDIV for case 8. The E-field at 1200 V is 35 kV/cm, and the PDIV is 11300V.

5.1.7 Case 9 - Replacing the silicone gel with a high performance resin and using silicon carbide coating

Case 9 investigates an improvement of the MOSFET power module, where a SiC coating is used and the silicone gel is replaced with a high performance resin. The setup of the MOSFET power module is illustrated in figure 5.9.

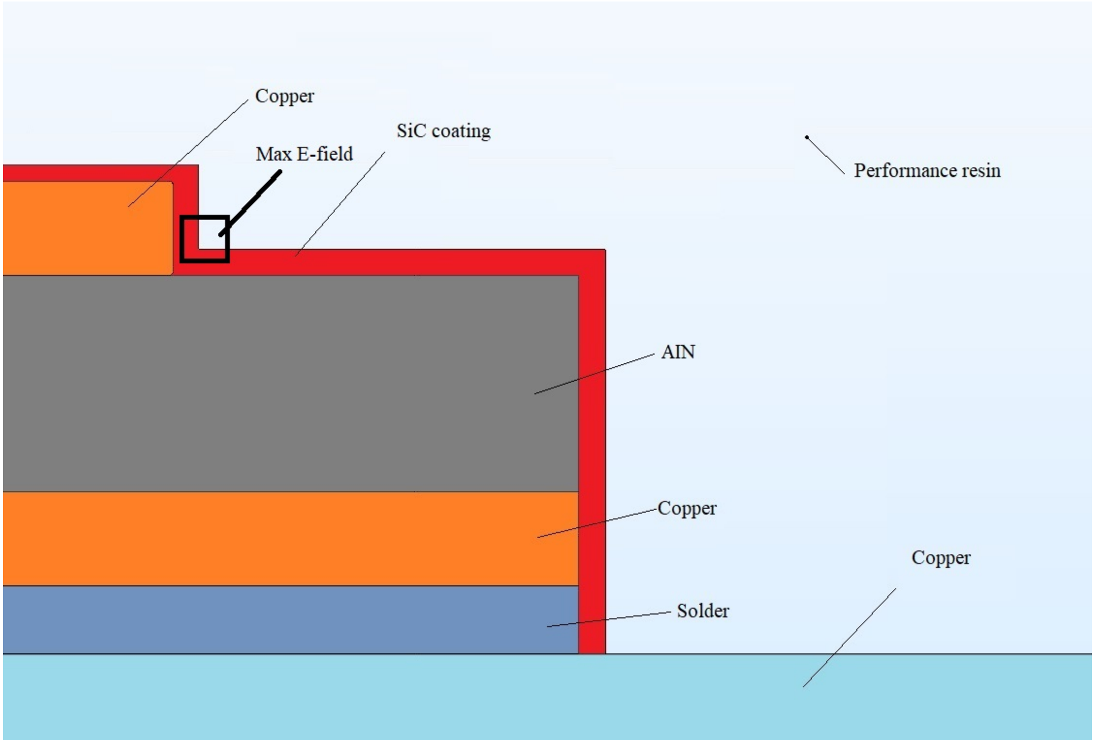


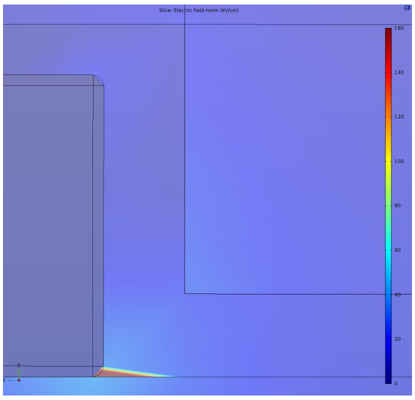
Figure 5.9: Cross section of the power module - Case 9 . [14]

The setup in figure 5.9 has a metallization (Copper) located on top of an insulating ceramic substrate. There is a further copper metallization at the bottom of this substrate that is soldered to a base layer. This solid arrangement is covered with silicone carbide, with a thickness of 77 micrometers. A performance resin then covers the rest. The thickness of these materials, for case 9, can be seen in table 5.9:

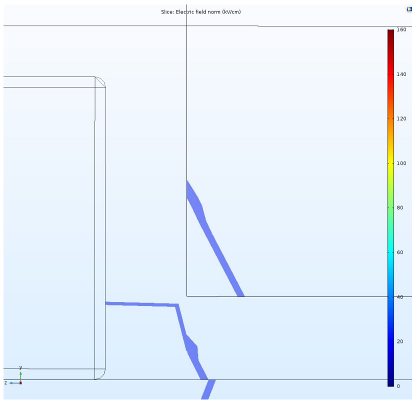
Table 5.11: Case 9 - Material thickness

Material	Thickness [mm]
Copper (upper)	0,28
Copper (Lower)	0,28
AlN	1,26
Silicon Carbide coating	0,077
Solder	0,2
Baseplate	0,22

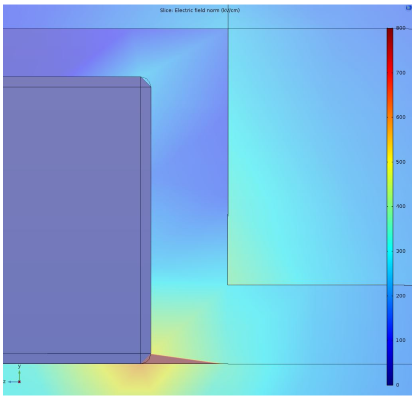
The material properties stated in table 3.2 apply for case 9. The interesting relative permittivities, for this case, are the relative permittivities of the silicon carbide coating, Aluminium Nitride and performance gel. The breakdown strengths of the materials are used for calculating the partial discharge inception voltage (PDIV). The results of simulating case 9, is illustrated in figure 5.10 (a-d):



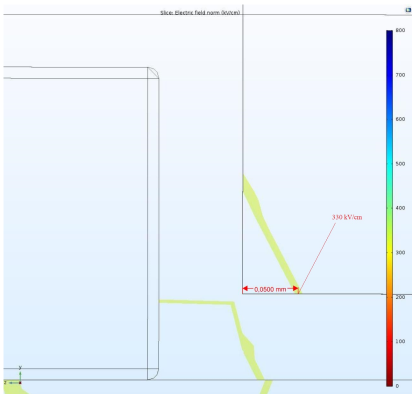
(a) E-field at operating condition, 1.2 kV



(b) E-Field at operating condition, 1.2 kV, measured 50 micrometers from edge.



(c) E-field at PDIV, 16300 V



(d) E-field at PDIV, 16300 V, measured 50 micrometers from critical edge.

Figure 5.10: Simulation of the E-fields in the power module, at the critical zone during normal operation and at PDIV, of case 9.

Figure 5.10 (a-d), illustrates the cross section of the simulated E-field, near the triple-point for case 9. The resulting module is simulated, where the metalization edges are filletet with a radius of 10 micrometers. The upper copper metallization is applied a voltage of 1,2 kV peak. Fig 5.10(a), illustrates the simulation result as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 160 kV/cm. The blue line shown in figure 5.10(b), is an E-field isoline, containing data between 24 to 24.5 kV/cm. The measurement is taken 50 micrometers from the SiC edge. The E-field measured at this distance resulted in 24 kV/cm. Fig 5.10(c) illustrates the simulation as a rainbow color table, where the E-field is shown as a spectrum with the E-fields ranging from 0 kV/cm to 800 kV/cm. The yellow line shown in figure 5.8(d), is an E-field isoline, containing data between 325 to 330 kV/cm. The measurement is taken 50 micrometers from the SiC edge. The E-field measured at this distance resulted in 330 kV/cm (the PDIV). The PDIV has been reached when an the applied voltage produces an E-field, which is higher than the electrical strength of the surrounding insulating material, for silicone gel it is 330 kV/cm. The simulated PDIV for case 9 is 16300 V, as shown in table 5.13:

Table 5.12: Case 9 - results

	E- field at 1.2 kV [kV/cm]	PDIV [V]
at 100Hz	24	16300

Table 5.12 shows the measured E-field and PDIV for case 9.The E-field at 1200 V is 24 kV/cm, and the PDIV is 16300 V.

5.2 Summary

To increase the PDIV, cases 3, 4, 5, 6, 7, 8 and 9 were investigated. Case 3 investigated how increasing the upper copper metallization thickness would impact the PDIV. The PDIV, for case 3 was simulated to be 6300 V. Case 4 investigated how increasing the AIN thickness would impact the PDIV. The PDIV for case 4 was simulated to be 8000 V. Case 5 investigated how using a silicon coating would impact the PDIV. The PDIV for case 5 was simulated to be 5400 V. Case 6 investigated how using a performance resin to replace the silicone gel would impact the PDIV. The PDIV for case 8 was simulated to be 8400 V. Case 7 investigated how using a silicon coating and increasing the AIN thickness would impact the PDIV. The PDIV for case 7 was simulated to be 6800 V. Case 8 investigated how using a performance resin to replace the silicon gel and increasing the AIN substrate thickness would impact the PDIV. The PDIV for case 8 was simulated to be 11300 V. Case 9 investigated how using a silicon carbide coating and replacing the silicone gel with a high performance resin would impact the PDIV. The PDIV for the SiC was not investigated, as the breakdown strength for SiC is much higher than the breakdown strength of the other materials. The PDIV for case 9 was simulated to be 16300 V. The results can be seen in table 5.13:

Table 5.13: Simulation results

Simulation results

Case	E-Field at 1.2 kV [kV/cm]	PDIV [V]
Case 3	51	6300
Case 4	40	8000
Case 5	44	5400
Case 6	47	8400
Case 7	35	6800
Case 8	35	11300
Case 9	24	16300

Chapter 6

Discussion

In this chapter, the results obtained in this project are discussed. First, the results of the electric field distribution inside the SiC MOSFET module came from simulations in chapter 3 are discussed. Next, the laboratory PD test results described in chapter 4 are elaborated. Lastly, the electric field reduction methods written in chapter 5 are discussed.

SiC MOSFET E-field strength simulations

This section will discuss the simulation results obtained in case 1 and 2. Case 1 and 2 were made in COMSOL to approximate realistic values. Considering case 1 and 2, case 1 had a higher breakdown voltage than case 2. As seen in table 6.1, the breakdown voltage in case 2 decreased compared to case 1, from 6300V to 5900V, a decrease of 6,7%. Case 1 had a fillet radius of 10 micrometers while case 2 had a fillet radius of 30 micrometers. This is opposite to the proportionality, stated in eq. 6.1 [9]:

$$E_{MAX} \propto \frac{1}{r^{\frac{1}{3}}} \tag{6.1}$$

Where E_{MAX} is the maximum E-field, and r is the radius of a 90 degree edge. The lab test resulted in a PDIV of 6500V peak. When comparing the PDIV from case 1 to the PDIV from the lab test, it had a deating factor of 3.2%. The derating factor for case 2 was 9.2%. As the results from case 1 were more reliable, all the following simulations in chapter 5, were done with a fillet radius of 10 micrometers.

Laboratory PD mesurement

This section will discuss the results obtained from PD test. The PD behavior of the SiC MOSFET insulation was studied, subjecting the module to normalised PD test (IEC 1287). It resulted in no PD activity at rated voltage. Nevertheless, since this standard test is based on sinusoidal excitation, it does not represent the real electric stresses during normal operation (like PWM excitation). Hence, testing the module under PWM stress would result in different PRPD patterns.

As regards PD origins, since they could not be seen, it was speculated based on the PRPD patterns that PD happened at the interface between the silicone gel and the substrate and the rim of metalization. This assumption was based on electric field simulations, where the peak electric strength was figured out at that triple junction.

E-field reduction methods

This section will discuss the improvements made to the SiC MOSFET module. The improvements were simulated in COMSOL, and six improvement cases were made (case 3-8).

In case 3, the upper copper metallization thickness was doubled. When comparing the results from case 3 to case 1, they resulted in the same E-field at 1.2 kV and the same breakdown voltage, 6.3 kV. This means that the technique used in case 3 made no improvements to the MOSFET power module.

In case 4, the AIN substrate thickness was doubled. As illustrated in table 6.1, comparing case 4 to case 1, the E-field at 1.2 kV was lowered from 51 kV/cm to 40 kV/cm. The breakdown voltage increased from 6.3 kV to 8 kV, which is an improvement of 27%.

In case 5, a silicon coating was added along the surface of the AIN substrate and the upper copper metallization, where the high potential was connected to the ground. As illustrated in table 6.1, when comparing case 5 to case 1, the E-field at 1,2 kV was lowered from 51 kV/cm to 44 kV/cm. The breakdown voltage decreased from 6.3 kV to 5.4 kV. This concludes that the technique used in case 5 decreased the breakdown voltage by 16.6%. Although the silicon coating has a permittivity similar to the AIN substrate, it has a lower breakdown strength than the silicone gel.

In case 6, the silicone gel was replaced with a high-performance resin. The permittivity of the resin is frequency-dependent, so a simulation was made of the resin at 100 HZ and 1 MHz. As illustrated in table 6.1, when comparing case 6 at 100Hz to case 1, the E-field at 1,2 kV was lowered from 51 kV/cm to 36.5 kV/cm. The breakdown voltage increased from 6.3 kV to 10.7 kV. When comparing case 6 at 1MHz to case 1, the E-field at 1,2 kV was lowered from 51 kV/cm to 47 kV/cm. The breakdown voltage increased from 6.3 kV to 8.4 kV. This concludes that the technique used in case 6 at 100HZ improved the modules PDIV with 69% and at 1MHz, 33%.

In case 7, the techniques in case 4 and 5 were combined. A silicon coating was added along the surface of the AIN and the upper copper metallization, so the high potential was connected to the ground. In addition to this the AIN substrate thickness was doubled. As illustrated in table 6.1, when comparing case 7 to case 1, the E-field at 1,2 kV was lowered from 51 kV/cm to 35 kV/cm. The breakdown voltage decreased from 6.3 kV to 6.8 kV. This concludes that the technique used in case 5 increased the breakdown voltage by 8%.

In case 8, the techniques in case 4 and 6 were combined. The silicone gel was replaced with a high-performance resin, and the AIN substrate thickness was doubled. The permittivity of the resin is frequency-dependent, so a simulation was made of the resin at 100 HZ and 1 MHz. As illustrated in table 6.1, when comparing case 8 at 100Hz to case 1, the E-field at 1,2 kV was lowered from 51 kV/cm to 29 kV/cm. The breakdown voltage increased from 6.3 kV to 13.6 kV. When comparing case 8 at 1MHz to case 1, the E-field at 1,2 kV was lowered from 51 kV/cm to 35 kV/cm. The breakdown voltage increased from 6.3 kV to 11.3 kV. This concludes that the technique used in case 8 at 100HZ improved in 116% and at 1MHz, 79%.

In case 9, the techniques in case 6 were combined with coating the module with SiC. The silicone gel was replaced with a high-performance resin, and the setup was coated with SiC. The permittivity of the resin is frequency-dependent, a simulation was made of the resin at 1 MHz, as the relative permittivity is lower at this frequency thus creating a higher E-field. As illustrated in table 6.1, when comparing case 9 at 1MHz to case 1, the E-field at 1,2 kV was lowered from 51 kV/cm to 24 kV/cm.

The breakdown voltage increased from 6.3 kV to 16.3 kV. This concludes that the technique used in case 9 at 1MHZ improved in 158%.

Table 6.1: Simulation results

Case	Technique	E-Field @ 1,2 kV [kV/cm]	PDIV [V]	Improvement [%]
Cae 1	10 micrometer fillet	51	6300	0%
Case 2	30 micrometer fillet	54	5900	-6,70%
Case 3	increasing copper thickness	51	6300	0%
Case 4	increasing substrate thickness	40	8000	27%
Case 5	using silicon coating	44	5400	-17%
Case 6	replacing gel with resin	47	8400	33%
Case 7	combining case 4 and 5	35	6800	8%
Case 8	combining case 4 and 6	35	11300	79%
Case 9	Combining case 6 with SiC coating	24	16300	158%

Chapter 7

Conclusion

This chapter will draw the main conclusions from this project. The scope of this report was to evaluate the electrical insulation in the SiC MOSFET module via electric field simulation and partial discharge measurement.

The electric field distribution of a SiC MOSFET module has been analyzed, using the software COMSOL. Methods to reduce the E-field compressions have been provided and their effectiveness has been verified via COMSOL FEM simulations. A measurement method using COMSOL, was implemented with an error of 3.2%, when comparing simulation results to the lab-test results. The E-field reduction methods are useful in reducing the electric stress inside the insulation and to increase its reliability by the reducing PDs. Doubling the thickness of the AIN substrate increased the PDIV by 27%. Using silicon coating decreased the PDIV by 17%. and using a high performance resin increased the PDIV by 33-69%. By combining the E-field reduction methods, the E-fields could be reduced even further. Doubling the thickness of the AIN substrate combined with using silicon coating, decreased the PDIV by 8%. The simulation results of this project, show that the most feasible method, to increase the PDIV and decrease the E-field, is to increase the AIN substrate thickness combined with replacing the silicone gel with a high performance resin. Doubling the thickness of the AIN substrate combined with using a high performance resin increased the PDIV by 79-116%. The best method, but least feasible, was to replace the silicone gel with a high performance resin and coating the solid structure of the MOSFET setup with silicon carbide. This methhod increased the PDIV by 158% (from 6.3kV to 16.3 kV).

The PD test on the SiC MOSFET module was performed and the obtained PRPD patterns were examined. Firstly, the module was stressed according to IEC 1287. No presence of partial discharges has been revealed during the test, meaning that the module could be used in its nominal application range (1.2 kV). Therefore, it was necessary to increase the applied voltage up to 5 kV to induce PD. The first measured PD higher than 10 pC marked the PDIV. It was at around 4.7 kV rms with the average magnitude of PDs at 36.1 pC. At higher voltage (4.8 kV rms) the PD number and intensity sharply increased. Lastly, analysing the PD pattern, it was concluded that the surface discharge initiated at the triple point, where the maximum E-field was obtained in FEM simulations.

Chapter 8

Future Work

Throughout this chapter, suggestions on future work, which could be made based on the analysis made in this project, will be presented.

One obstacle of this project, was to reliably predict the E-field from the simulations. The chosen method, was the one used in [9]. It turned out, this method wasn't reliable after using it on two simulations (case 1 and 2), thus a more reliable measurement method can be investigated by combining simulation results and real-life measurement results.

The simulation results from case 1, predicted a PDIV of 6300V. Measurements from the lab-test resulted in a PDIV of 6500V. The resulting error, comparing the simulation result to the lab-test is 3.2%. The simulation results from case 8, resulted in a PDIV of 11300V and 13600V. If the simulation results have an derating factor of 3.2%, compared to real-life results, then real-life PDIV could increase between 10940V to 13160V. Which is an improvement of 68-102%. The simulation results from case 9, resulted in an improvement of 158%, with a PIDV of 16300V. To test this, the improvements from case 4 to 9 could be implemented to the MOSFET power module. It is unknown if the derating factor remains constant for all cases, this should also be investigated.

Regarding laboratory PD test, power MOSFETs are known for their high frequency operation (up to about 100 kHz) and moving to SiC MOSFETS implies higher switching frequencies. Therefore, instead of at power frequency, PD measurements should be performed at higher one. Furthermore, as it is stated earlier, PWM stress-type is closer to the actual working conditions of power modules. Hence, the PD test could be carried out subjecting the SiC MOSFET module to this type of stress. Apart from electrical PD measurements with PRPD patterns, optical ones could be conducted in order to visualise the PD locations inside the module.

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Appendix A

Appendix A

Fundamental Electric Constants

Under Coulomb's law the value of the proportionality constant k depends on the unit system used. Most of the common units like volt, ampere, ohm, and watt are included in the SI electric units. The electric charging unit SI is numbered one coulomb (1 C). In SI units the constant in Equation 2.1 is as in Equation A.1:

$$k = 8.9875517 \cdot 10^9 \cong 8.988 \cdot 10^9 \qquad [N \cdot \tfrac{m^2}{C}] \quad \text{(A.1)}$$

k is known to such significant figures as this value is closely related to the speed of light in vacuum, which is precisely defined as $c = 2.99792458 \cdot 10^9$ $[N \cdot \frac{m^2}{C^2}]$. The value of k is specified in terms of light speed c to be precisely in Equation A.2 [13]:

$$k = 10^{-7} \cdot c^2 \qquad [N \cdot \tfrac{s^2}{C^2}] \quad \text{(A.2)}$$

By theory the electric force F can be measured at a given distance r between two equivalent charges q and use Coulomb's law to calculate the charge. Thus k's value can be called a coulomb operational description. It is easier to describe the coulomb in terms of a unit of electrical current (charge per unit time), the ampere, equal to 1 coulomb per second, for purposes of experimental precision. The constant k in SI units is usually written in Equation 2.1 as if (another constant is "epsilon-nought" or "epsilon-zero." The Law of Coulomb can be written as in Equation A.3 [13]:

$$F = \frac{1}{4\pi\varepsilon_0} \cdot \frac{|q_1 q_2|}{r^2} \quad \text{(A.3)}$$

Coulomb's law: force between two point charges [13].

In Equation A.3, the constants are defined approximately as in Equation A.4 and in Equation A.5:

$$\varepsilon_0 = 8.854 \cdot 10^{-12} \qquad [\tfrac{C^2}{N \cdot m^2}] \quad (A.4)$$

$$k = \frac{1}{4\pi\varepsilon_0} = 8.988 \cdot 10^9 \qquad [N \cdot \tfrac{m^2}{C}] \quad (A.5)$$

Where ε_0 is the constant of permittivity in vacuum and k is the Coloumb constant. In examples and problems the approximate value will be often used as in Equation A.6:

$$k = \frac{1}{4\pi\varepsilon_0} = 9.0 \cdot 10^9 \qquad [N \cdot \tfrac{m^2}{C}] \quad (A.6)$$

That's inside the right value of around 0.1 per cent.

The charge of an electron or a proton is denoted by e which has the value as in Equation A.7:

$$e = 1.602176487 \cdot 10^{-19} \qquad [C] \quad (A.7)$$

One coulomb represents about $6 \cdot 10^{18}$ electrons [13].

Appendix B

Appendix B

Simulation Results

This Appendix includes all the simulation figures appearing in the project, as the figures in the project can be small.

Case 1

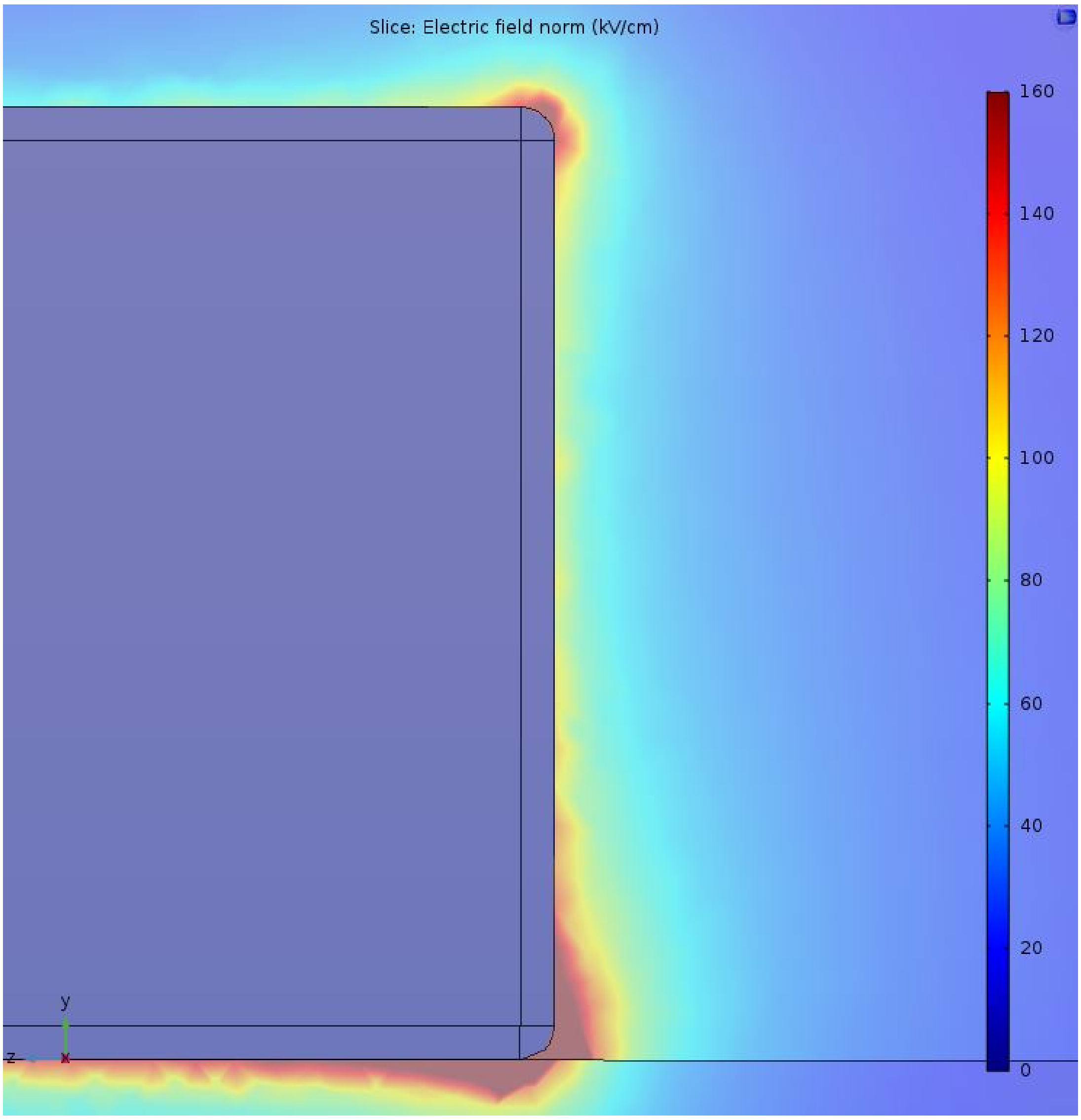

Figure B.1: Case 1, E-field at operating condition, 1.2 kV

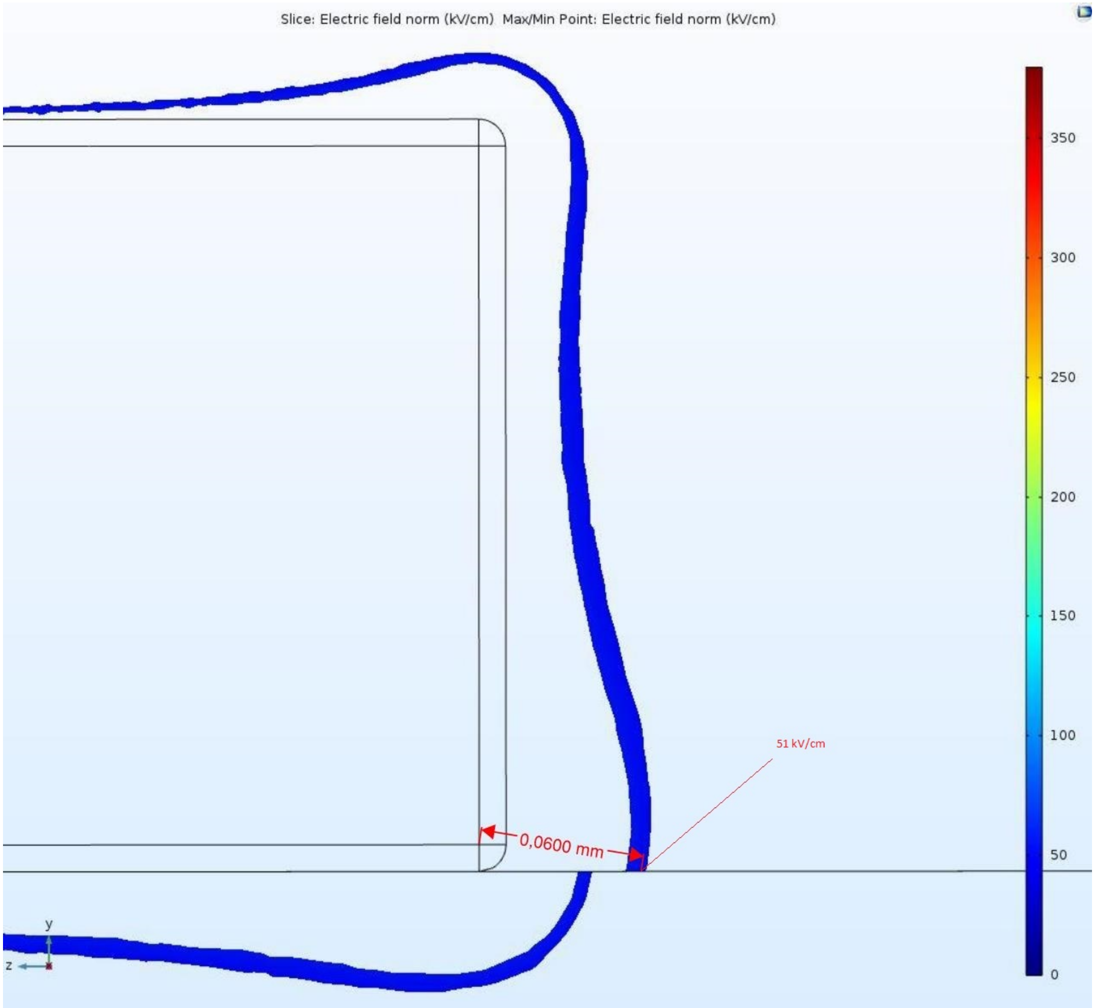

Figure B.2: Case 1, E-field at operating condition, 1.2 kV, measured at 50 micrometers from the edge, 51 kV/cm

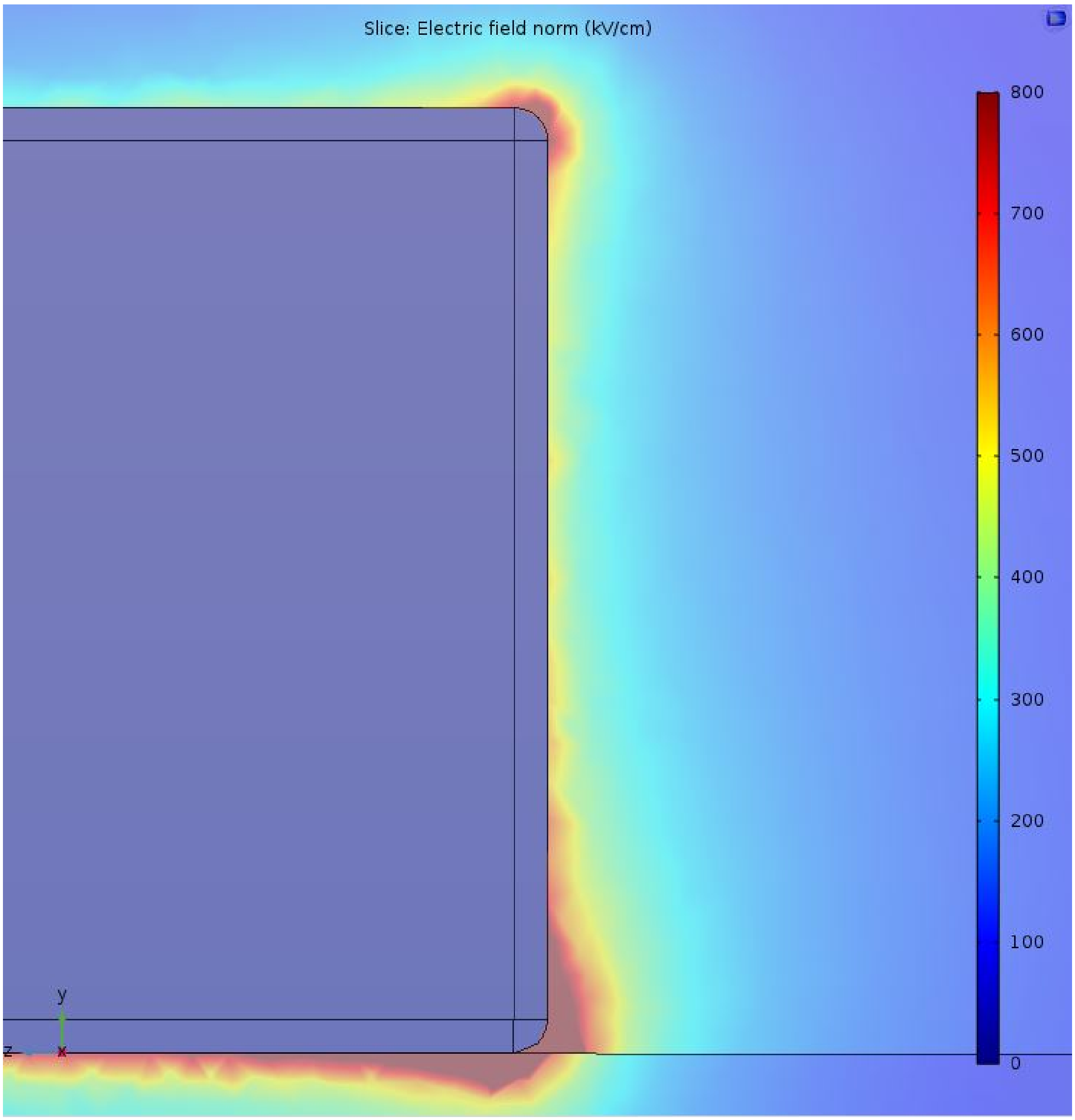

Figure B.3: Case 1, E-field at PDIV, 6.3 kV

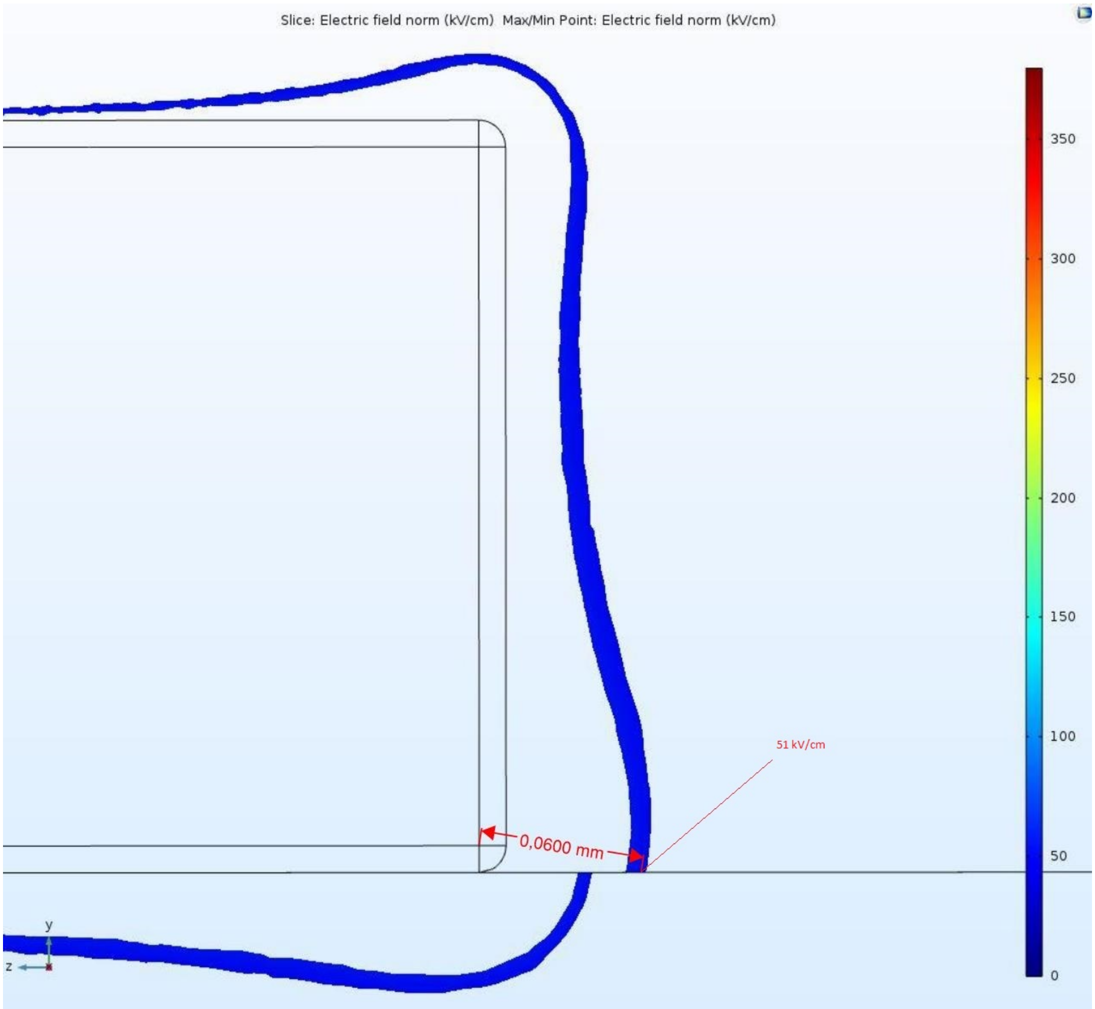

Figure B.4: Case 1, E-field at PDIV, 6.3 kV - measured 50 micrometers from edge

Case 2

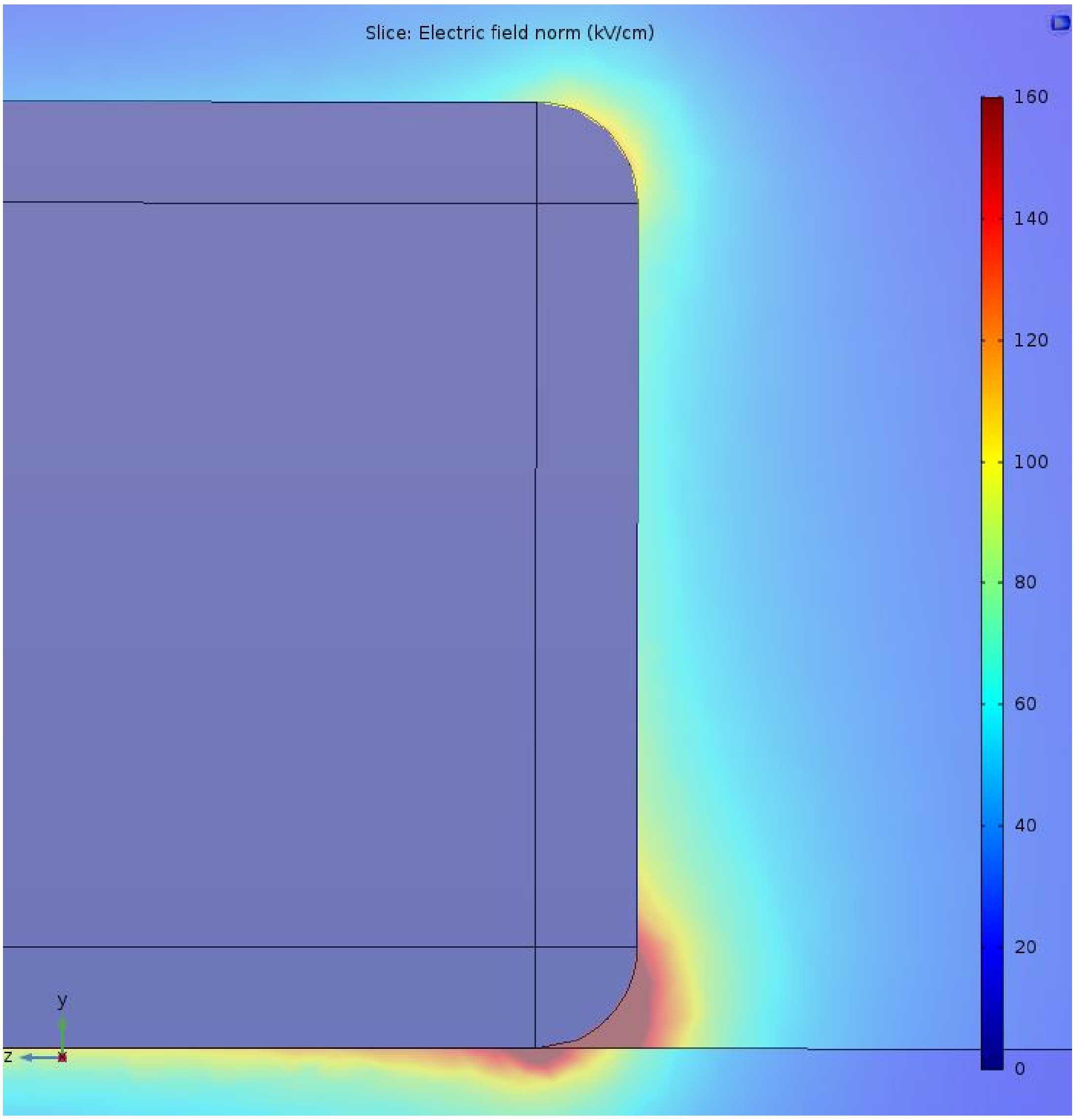

Figure B.5: Case 2, E-field at operating condition, 1.2 kV

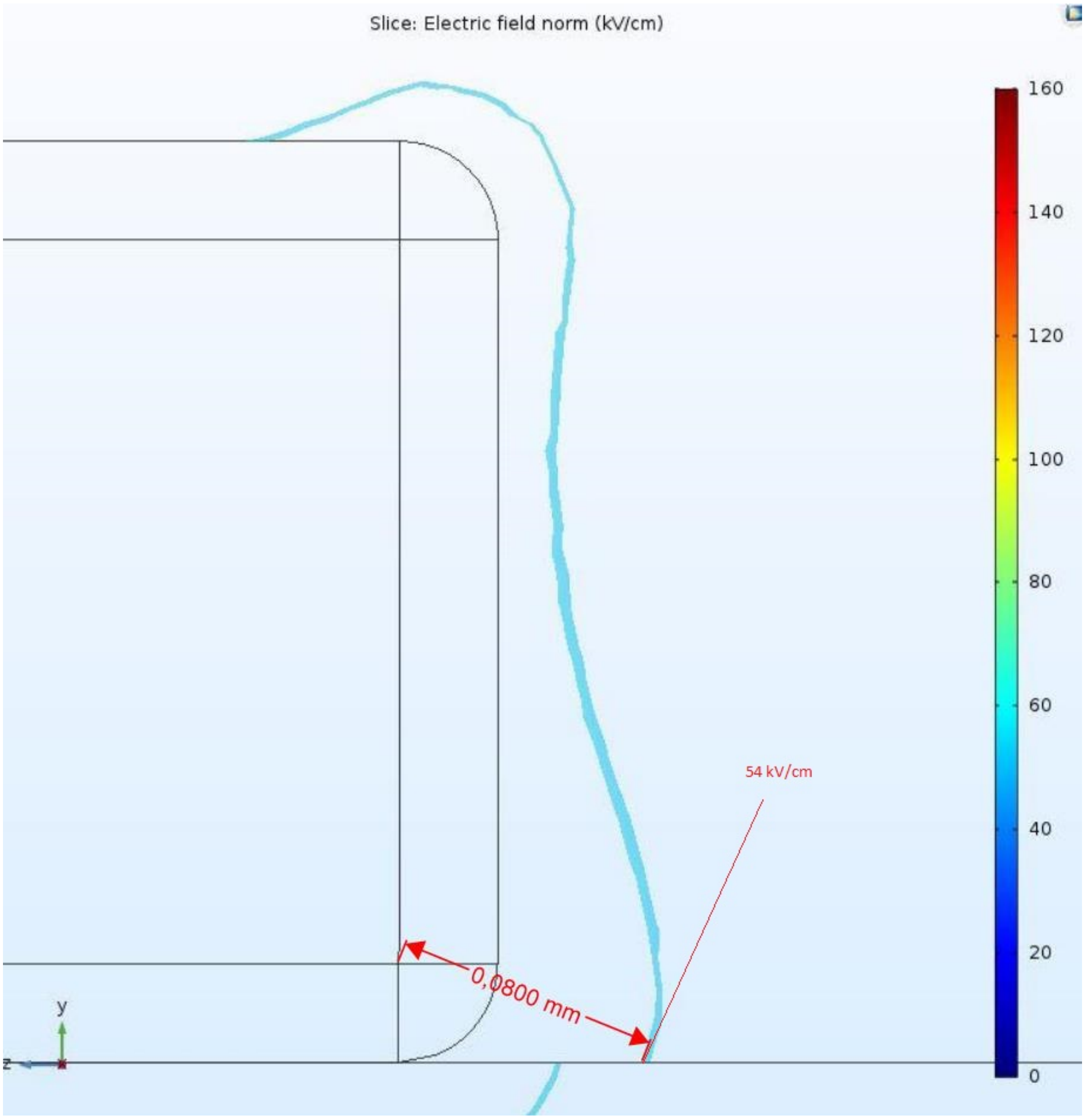

Figure B.6: Case 2, E-field at operating condition, 1.2 kV, measured at 50 micrometers from the edge, 51 kV/cm

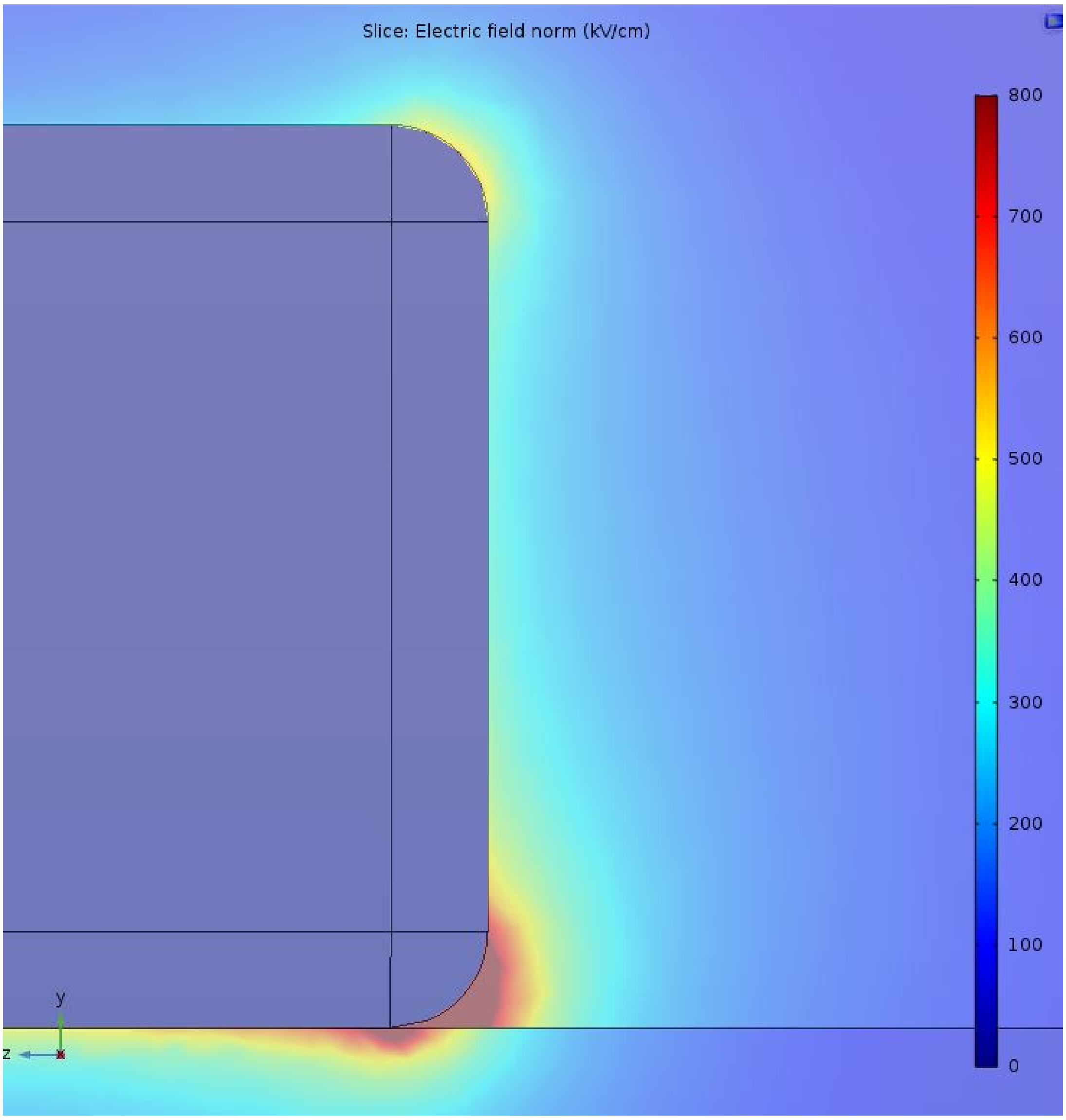

Figure B.7: Case 2, E-field at PDIV, 5.9 kV

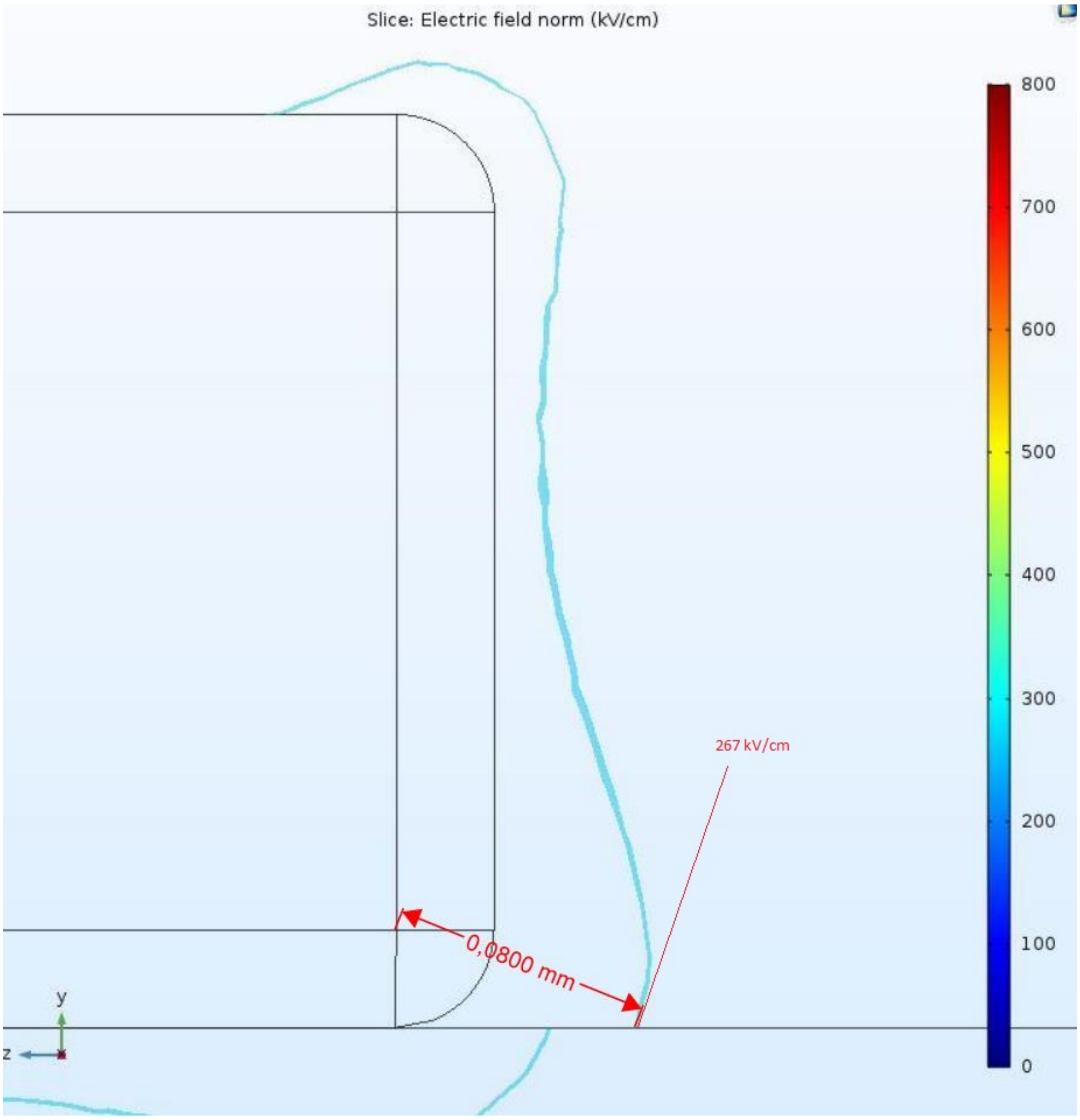

Figure B.8: Case 2, E-field at PDIV, 5.9 kV - measured 50 micrometers from edge

Case 3

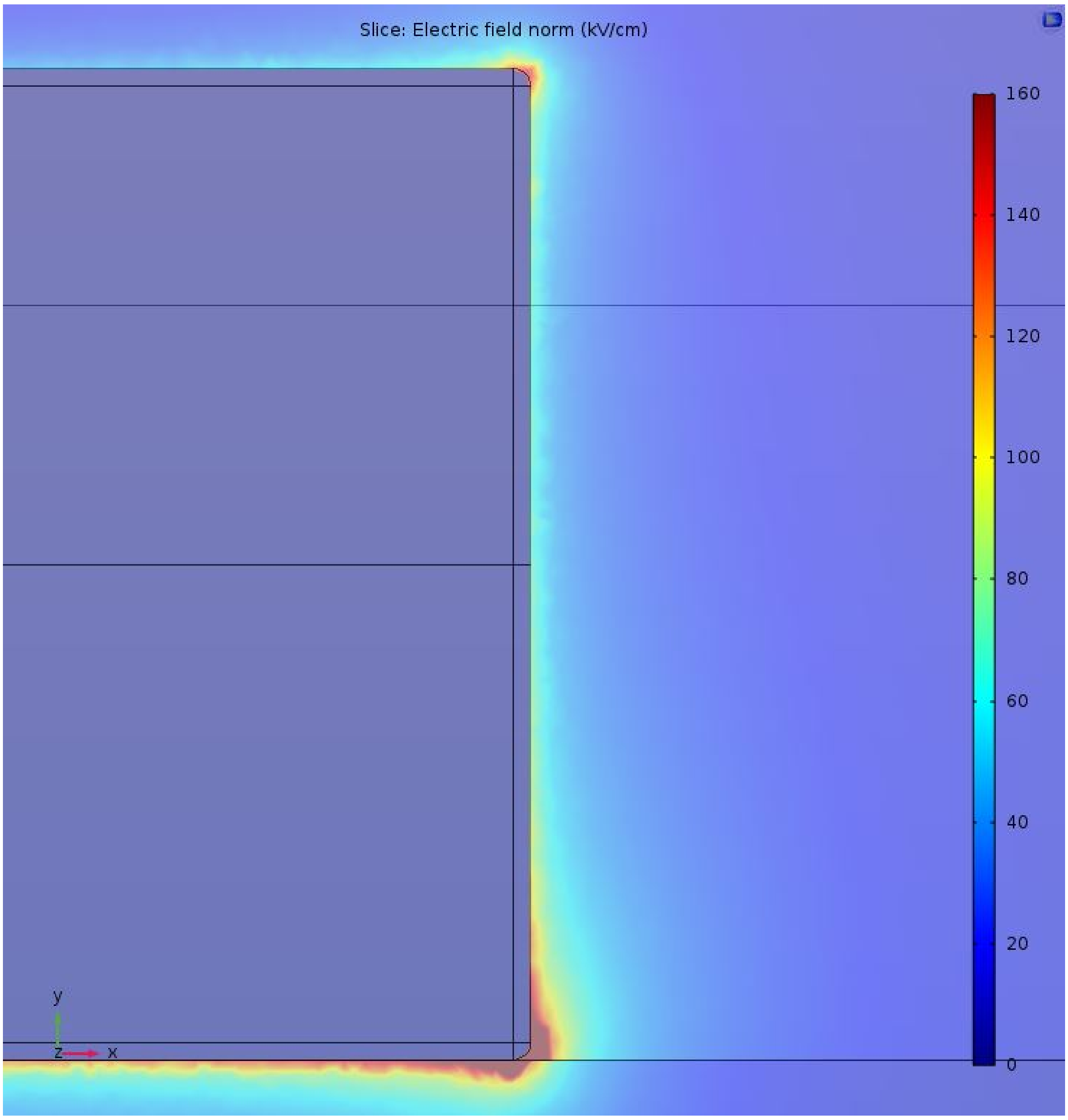

Figure B.9: Case 3, E-field at operating condition, 1.2 kV

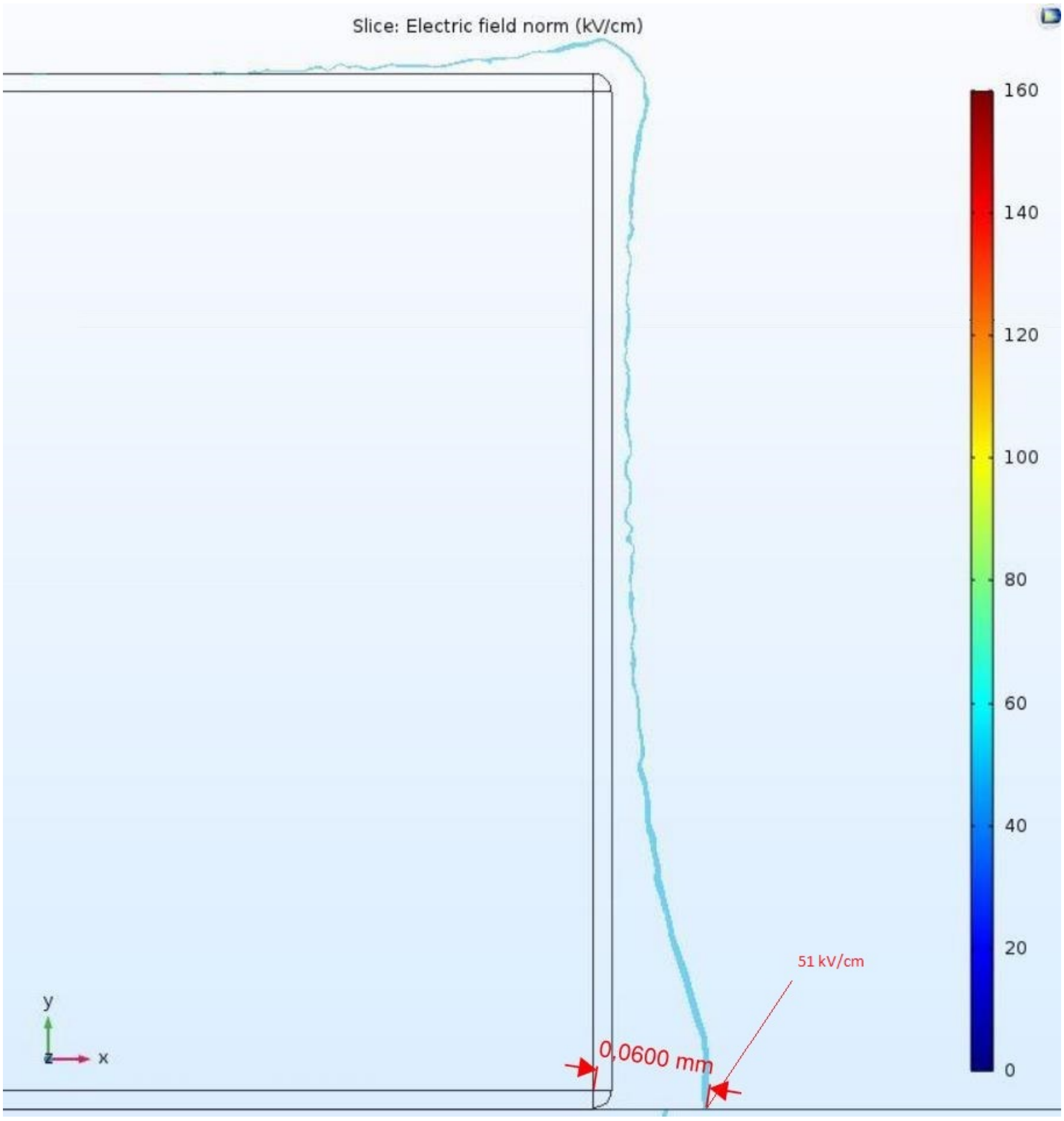

Figure B.10: Case 3, E-field at operating condition, 1.2 kV, measured at 50 micrometers from the edge, 51 kV/cm

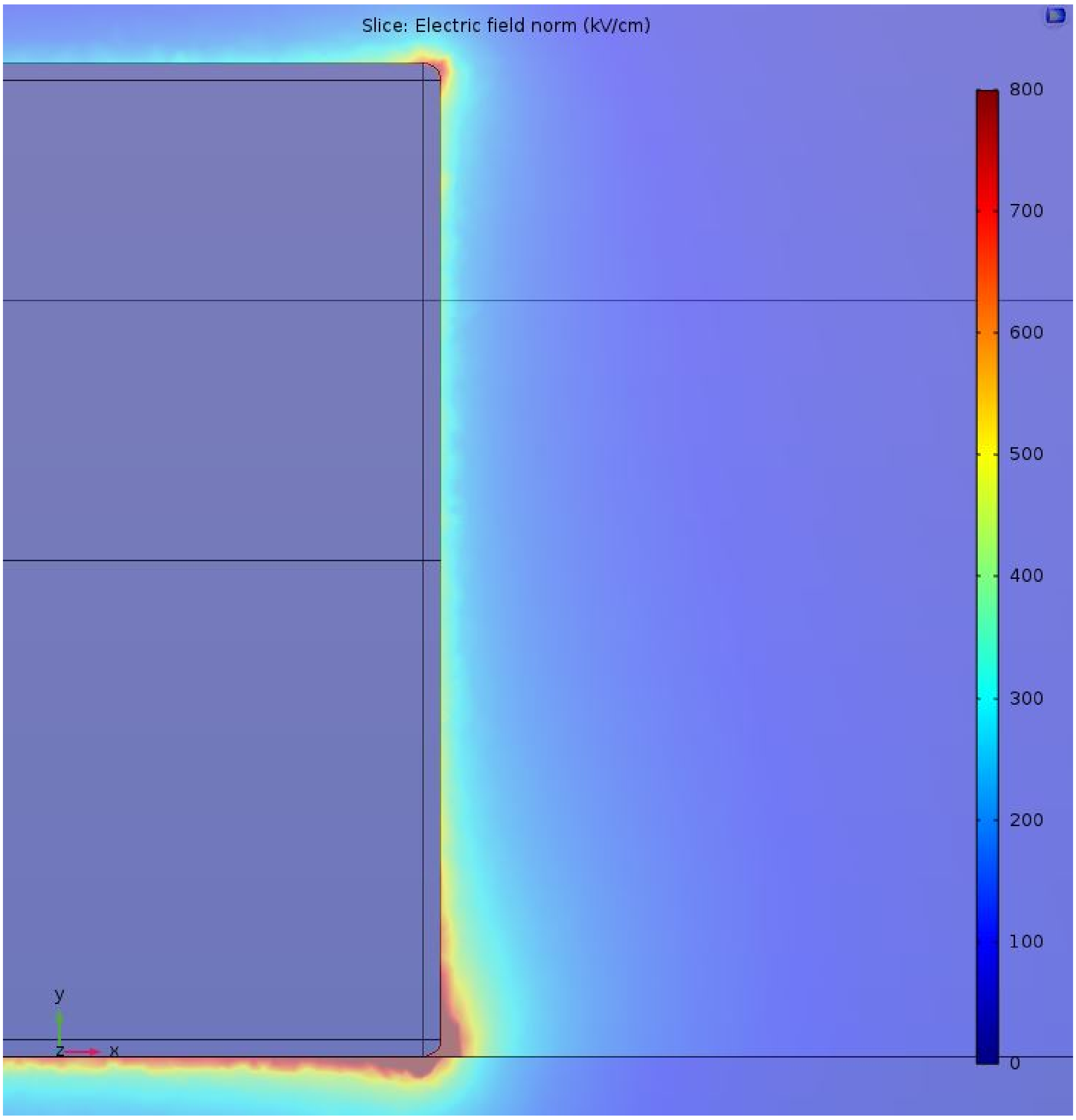

Figure B.11: Case 3, E-field at PDIV, 6.3 kV

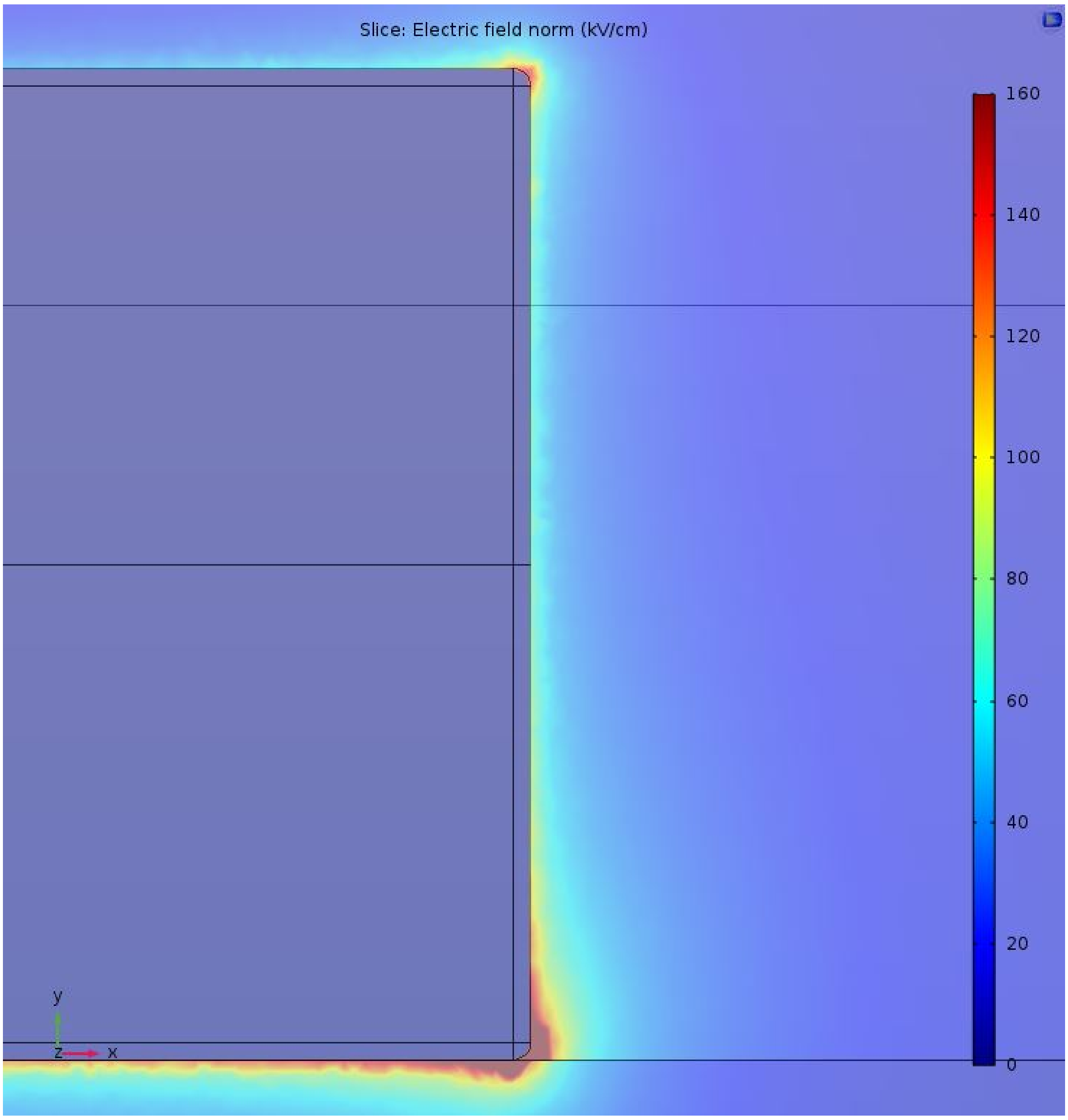

Figure B.12: Case 3, E-field at PDIV, 6.3 kV - measured 50 micrometers from edge

Case 4

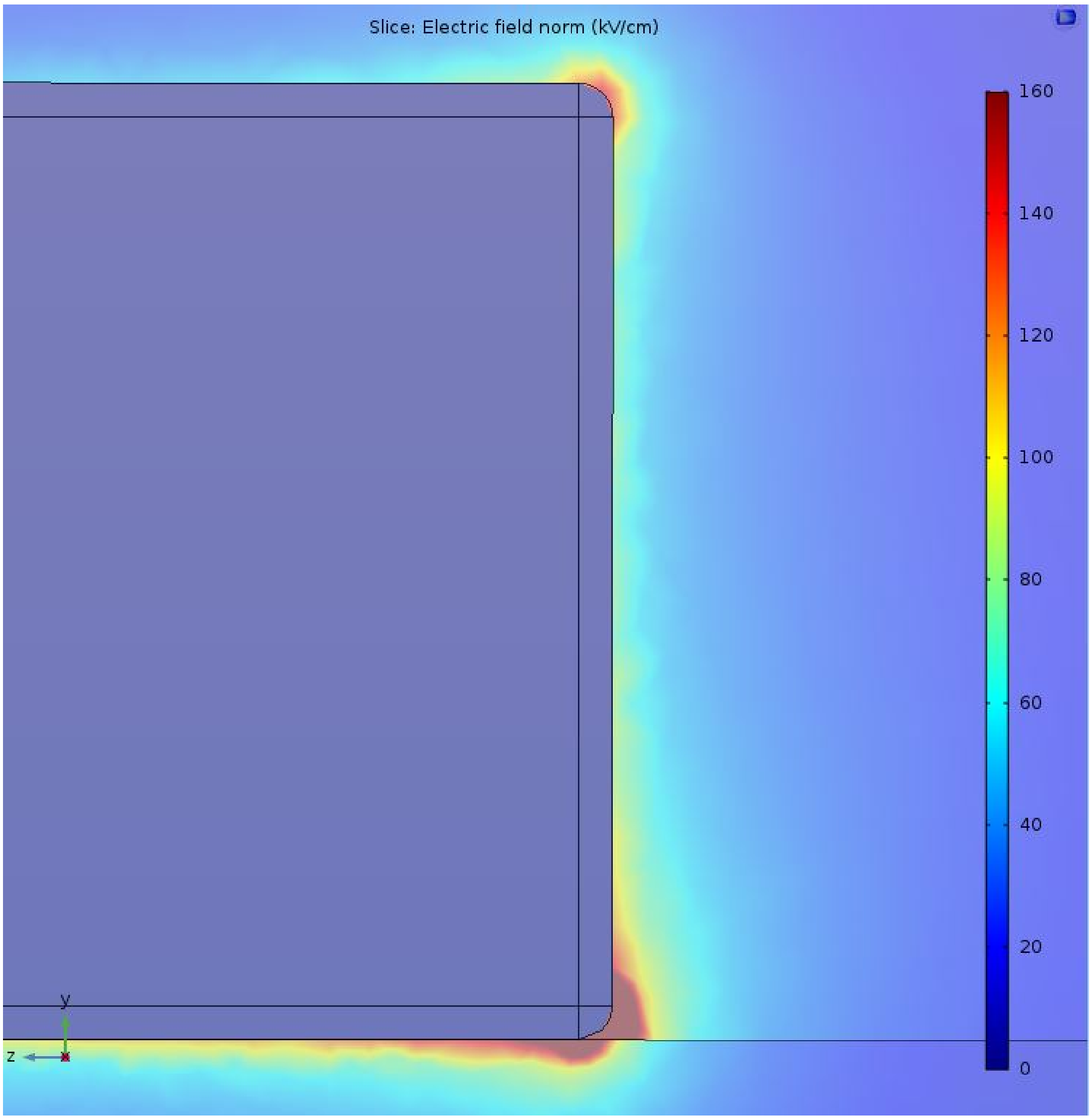

Figure B.13: Case 4, E-field at operating condition, 1.2 kV

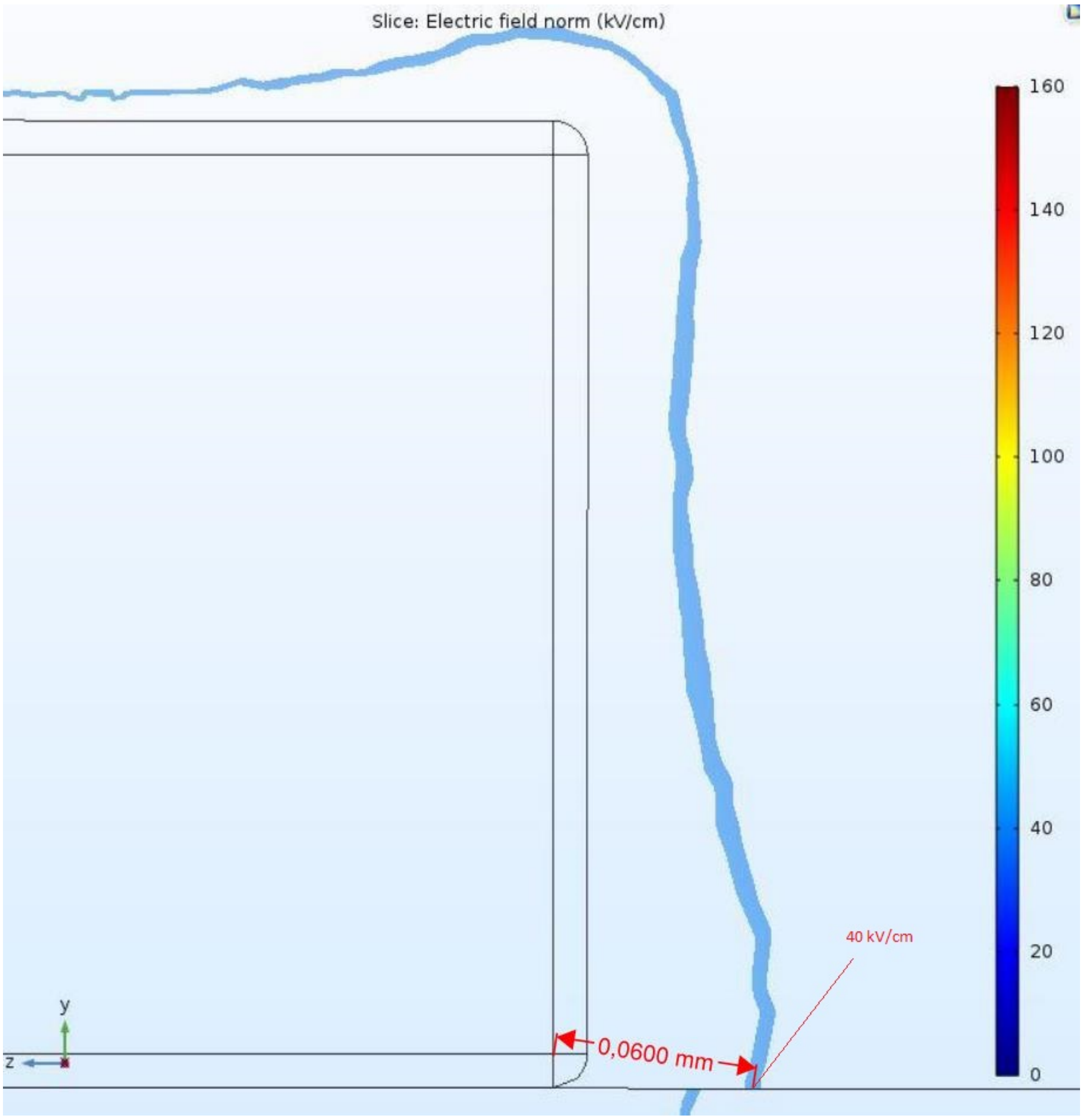

Figure B.14: Case 4, E-field at operating condition, 1.2 kV, measured at 50 micrometers from the edge, 51 kV/cm

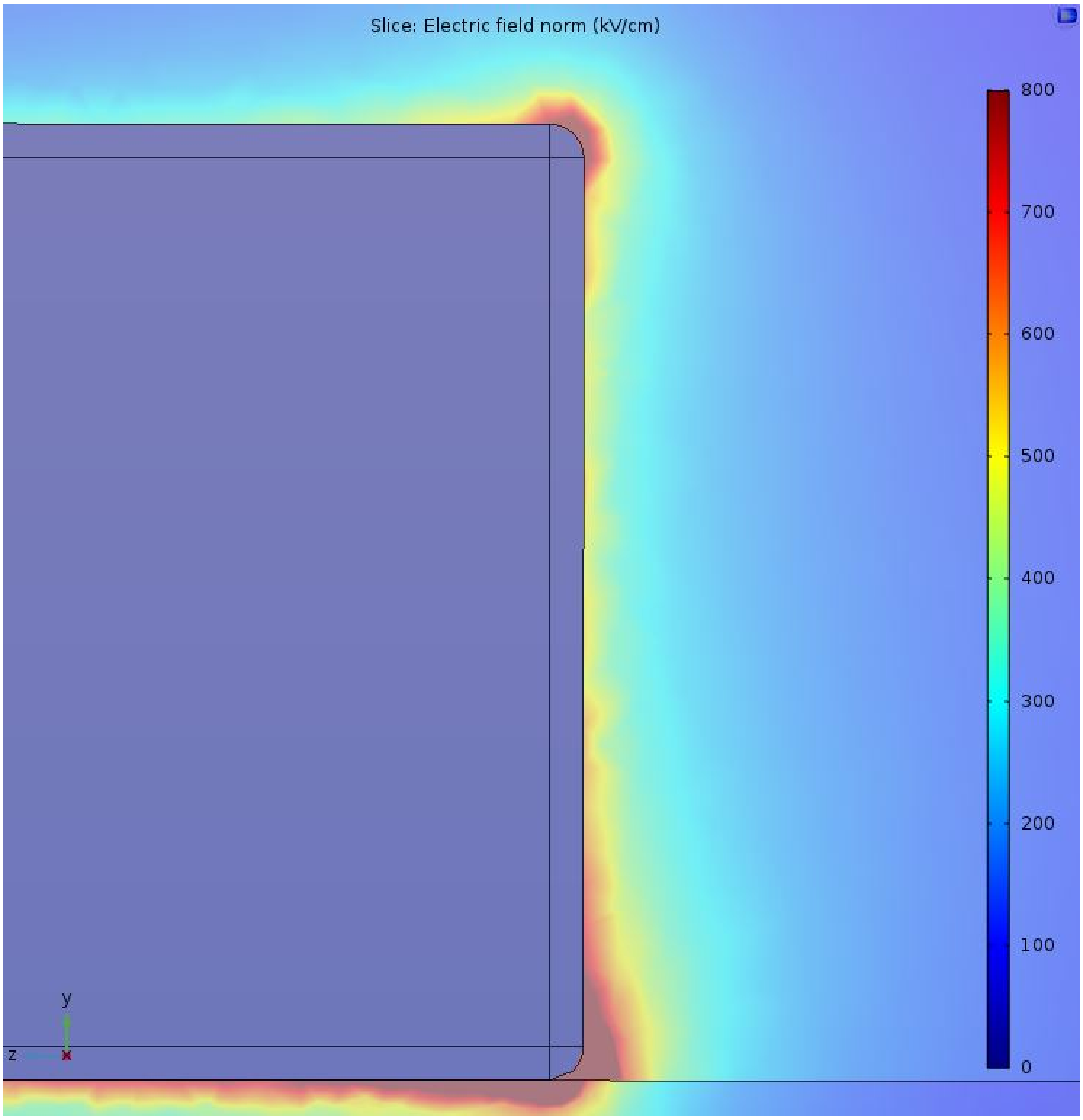

Figure B.15: Case 4, E-field at PDIV, 8 kV

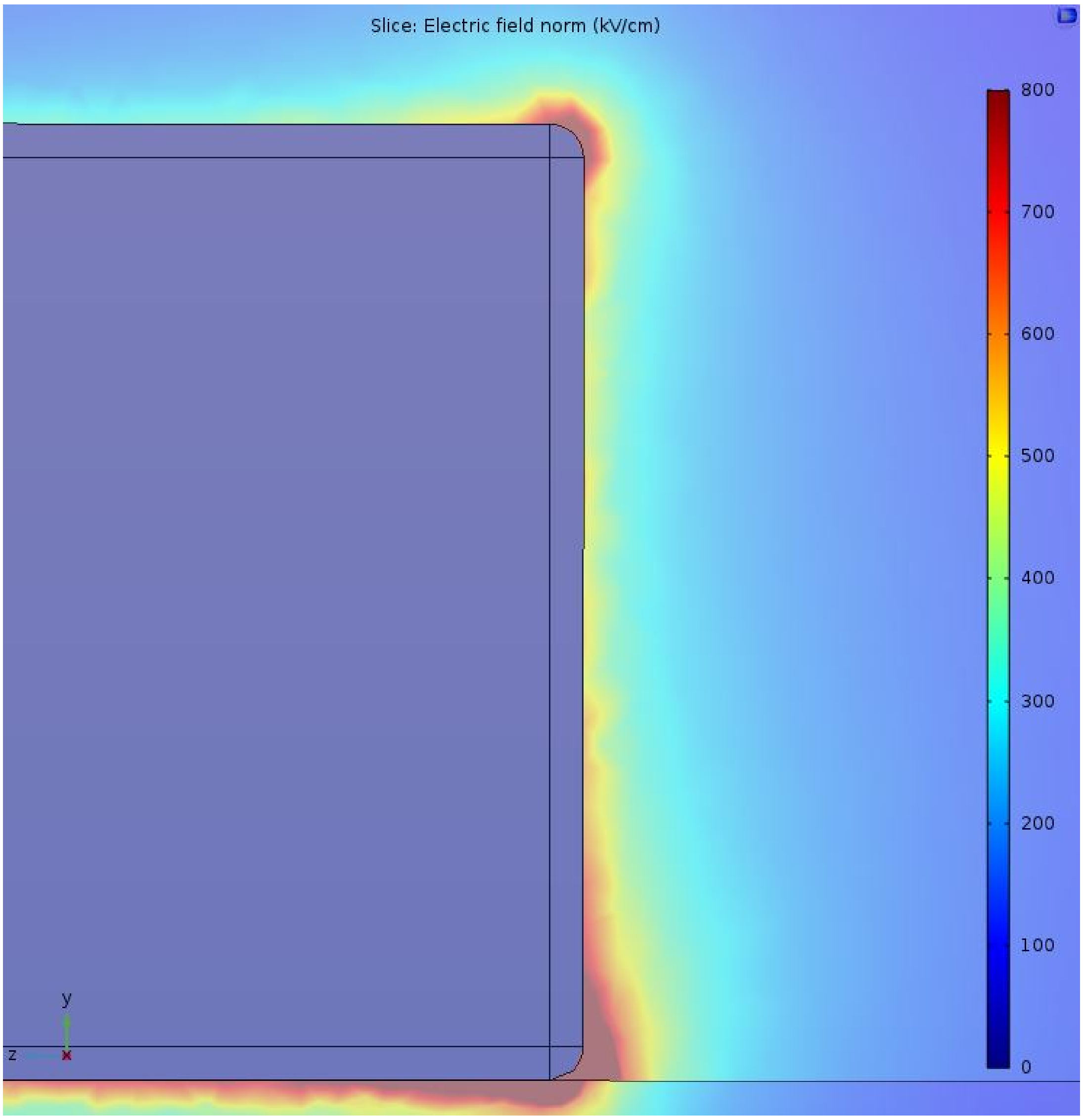

Figure B.16: Case 4, E-field at PDIV, 8 kV - measured 50 micrometers from edge

Case 5

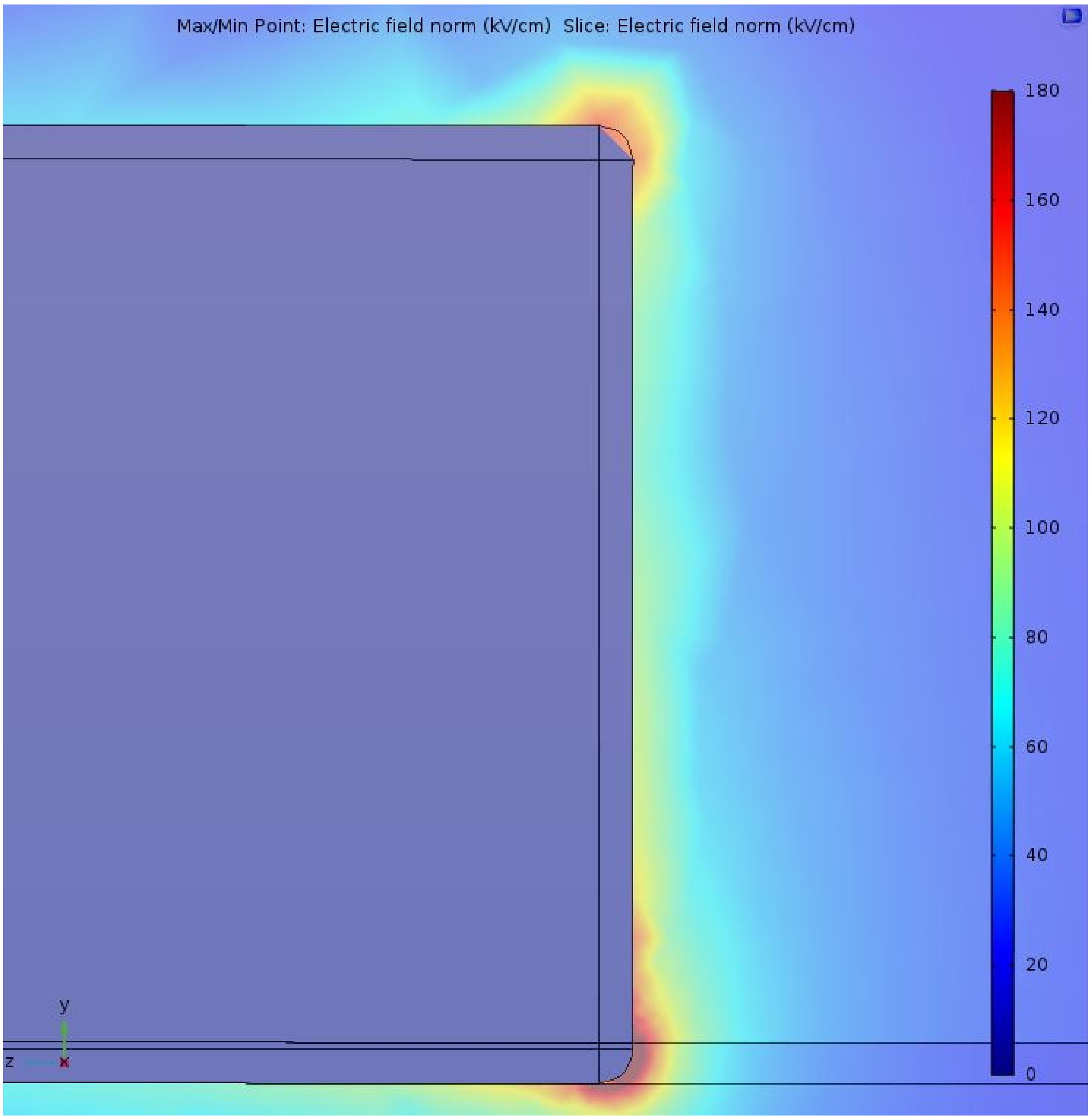

Figure B.17: Case 5, E-field at operating condition, 1.2 kV

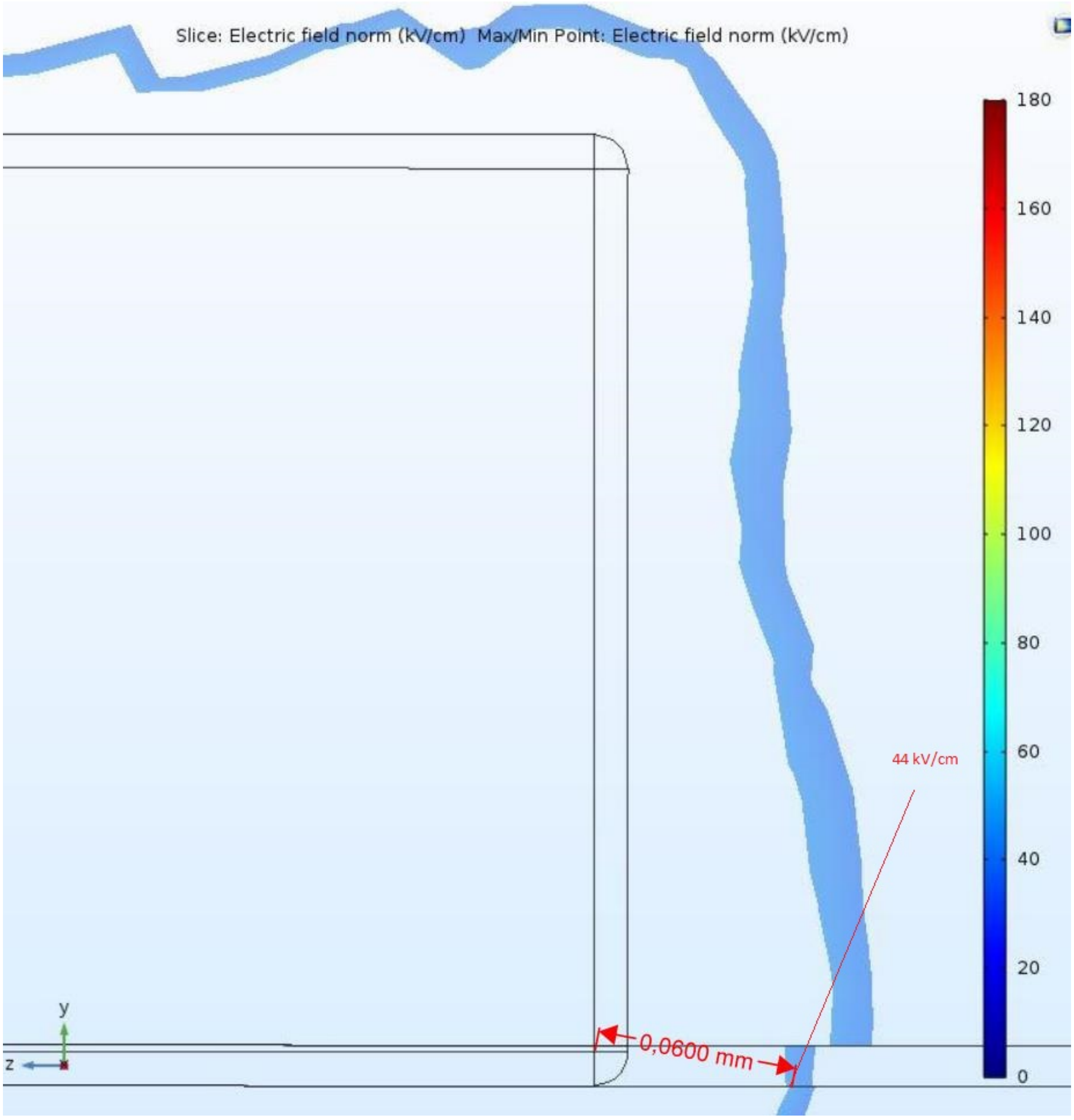

Figure B.18: Case 5, E-field at operating condition, 1.2 kV, measured at 50 micrometers from the edge, 51 kV/cm

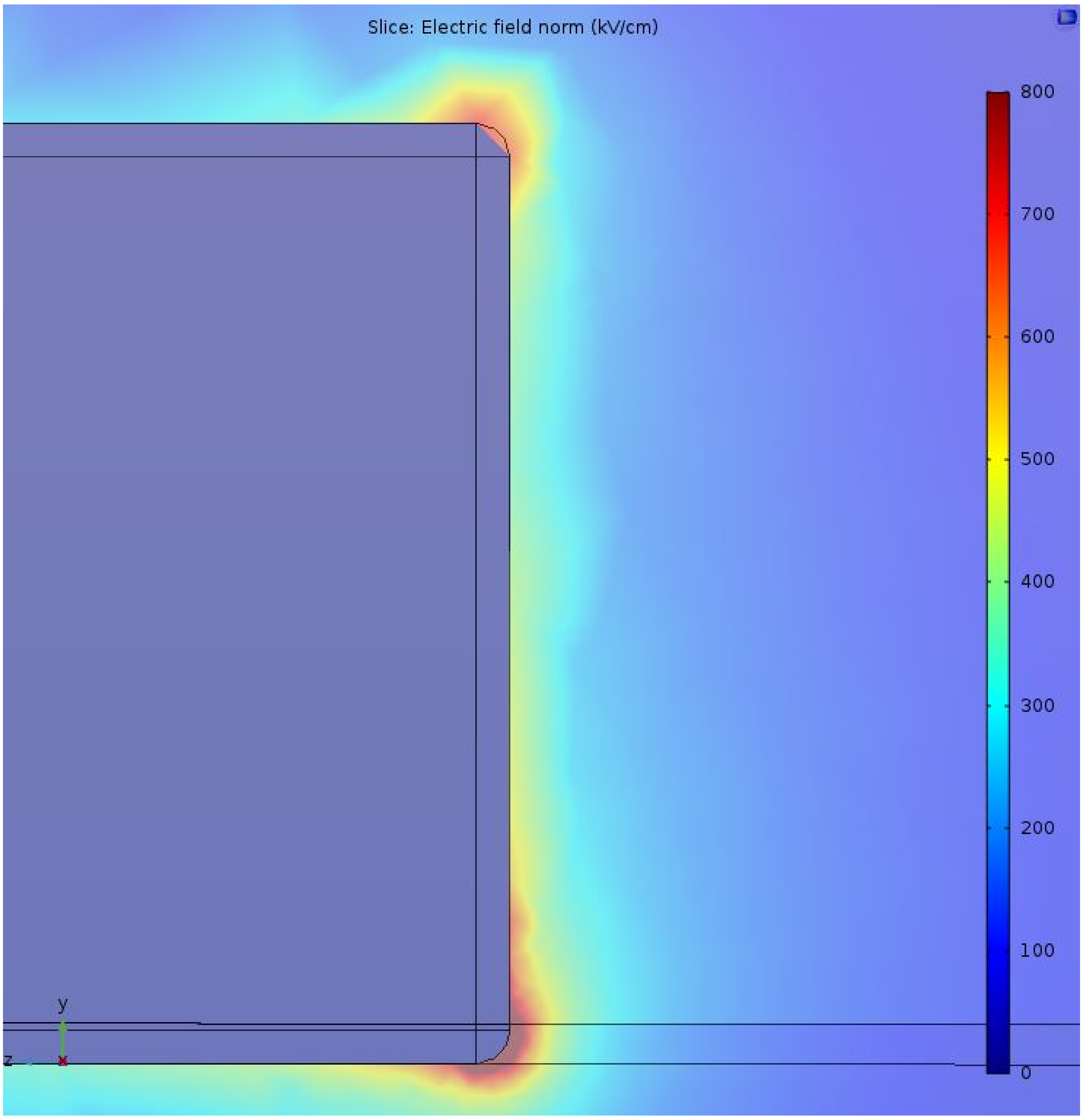

Figure B.19: Case 5, E-field at PDIV, 6.3 kV

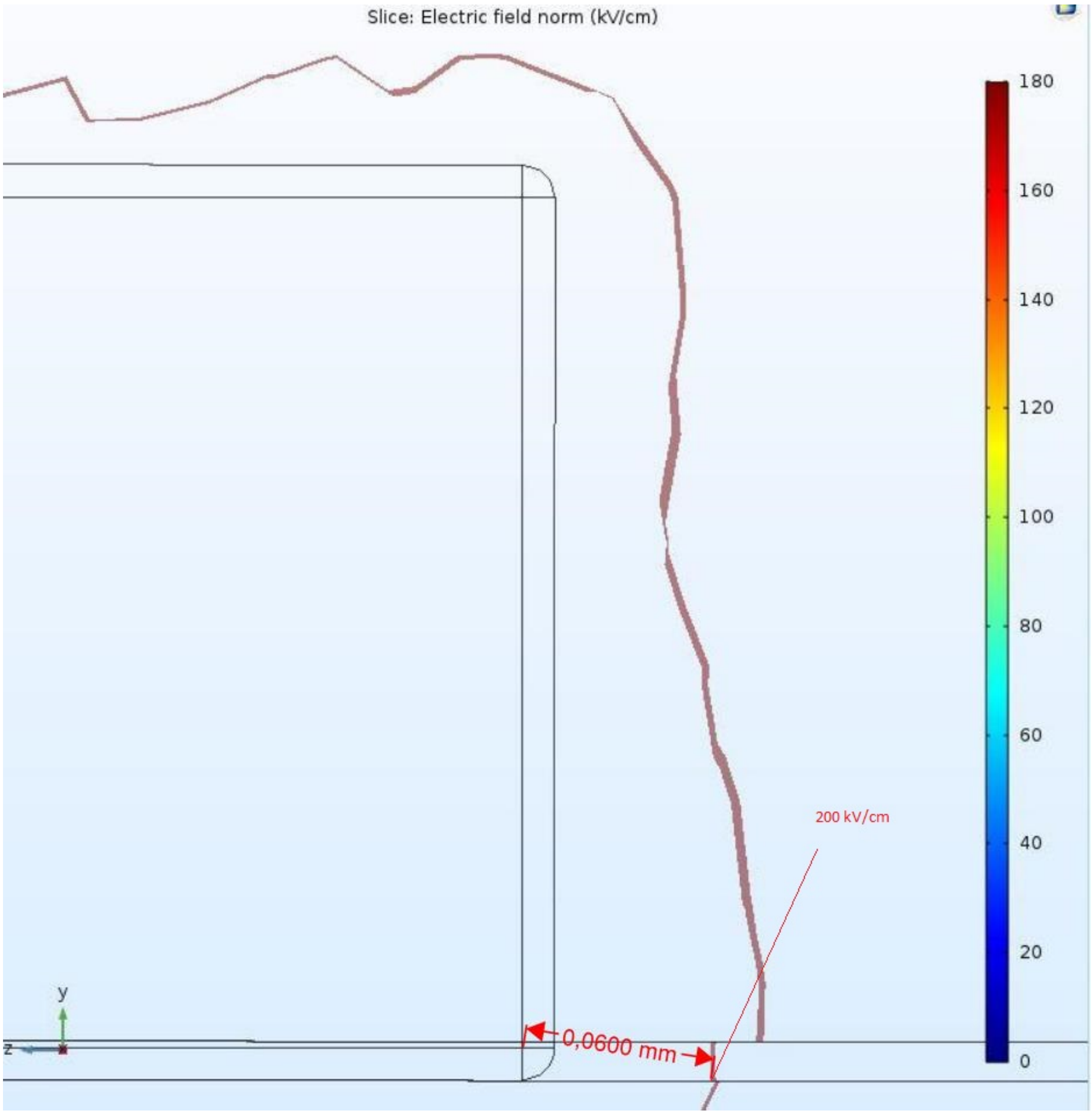

Figure B.20: Case 5, E-field at silicon breakdown strength, 6.3 kV - measured 50 micrometers from edge

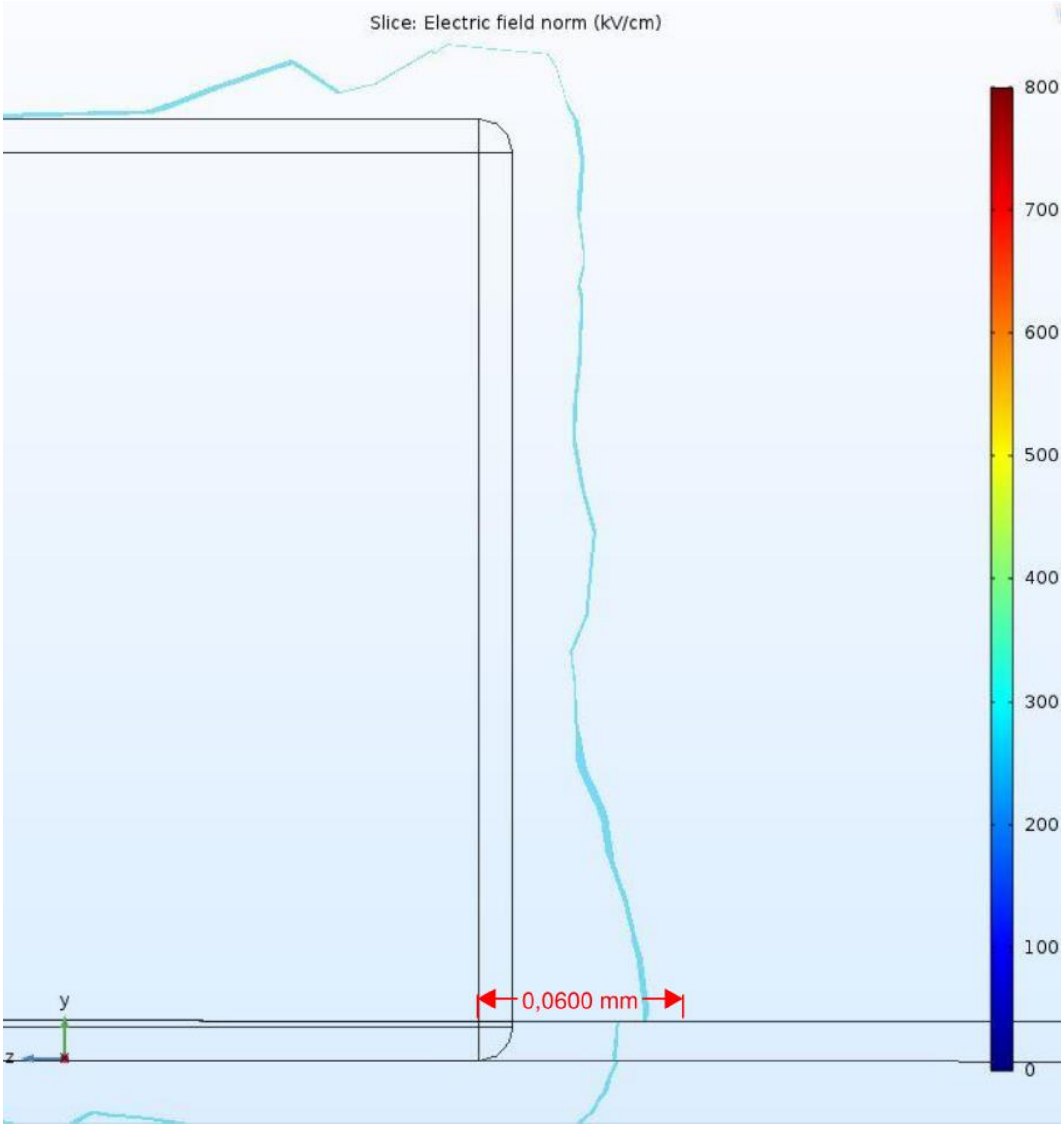

Figure B.21: Case 5, checking E-field at near silicone gel, 6.3 kV - measured 50 micrometers from edge

Case 6

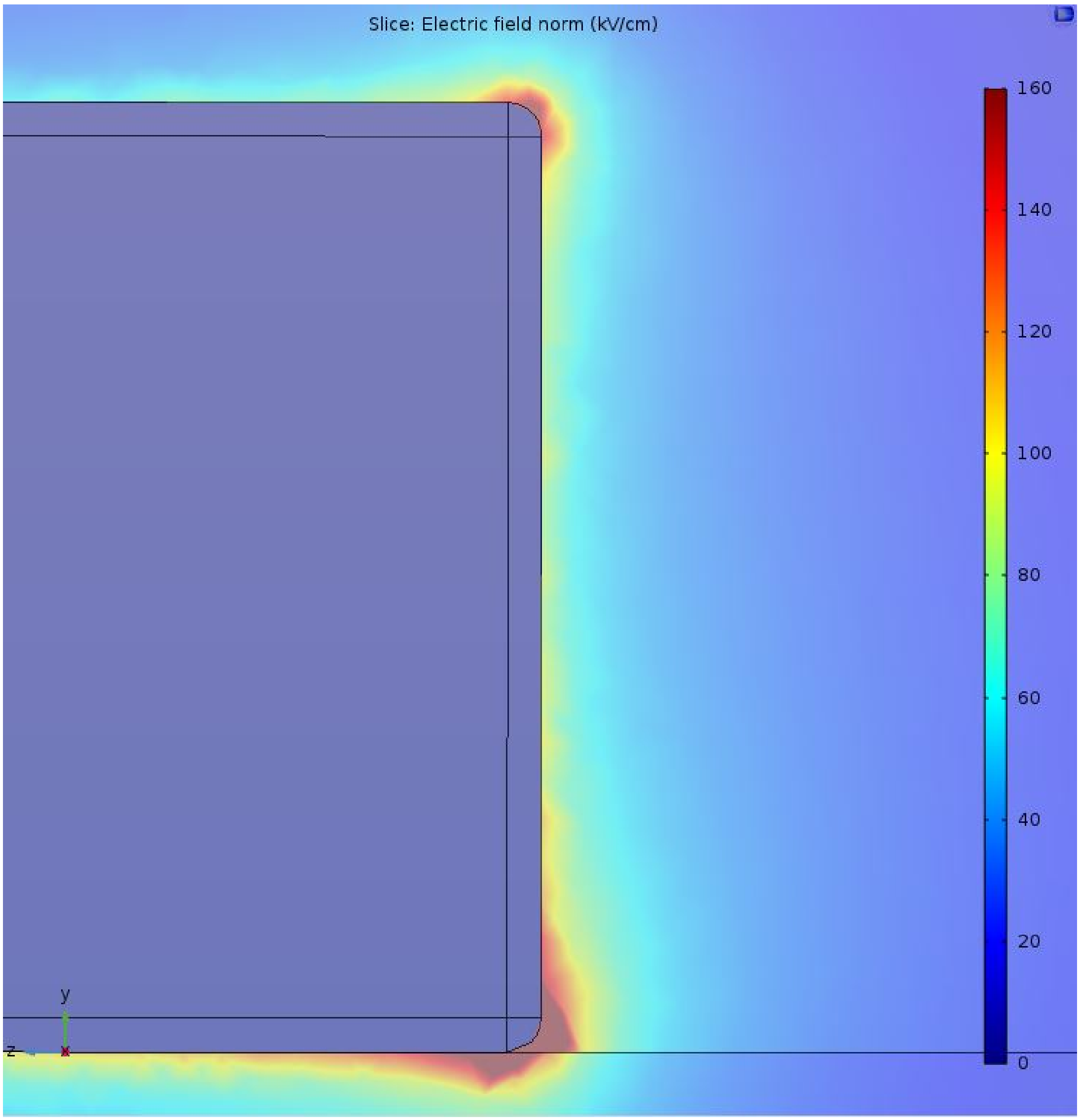

Figure B.22: Case 6, dupont resin at, E-field at operating condition, 1.2 kV

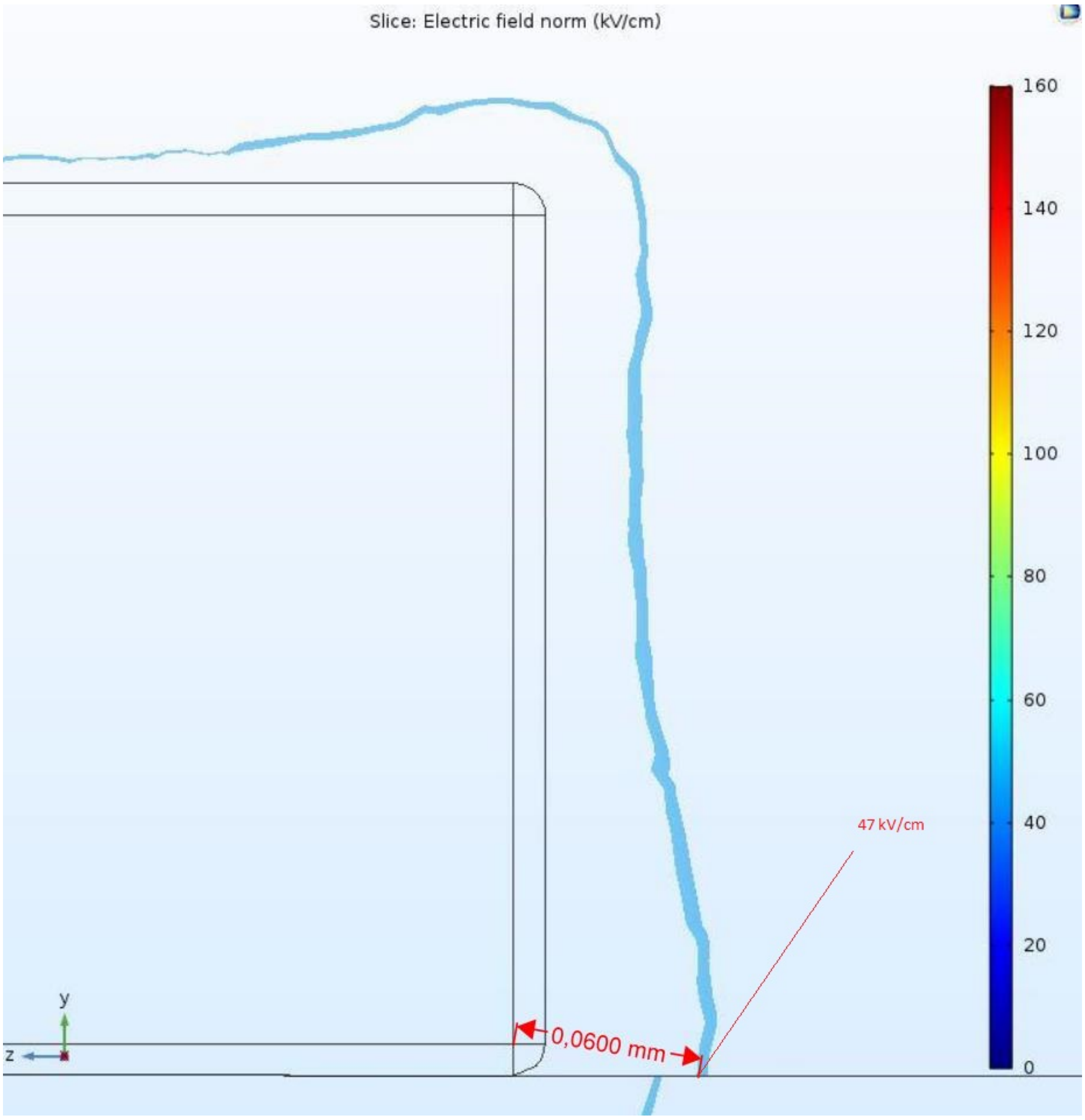

Figure B.23: Case 6, dupont resin, E-field at operating condition, 1.2 kV, measured at 50 micrometers from the edge, 51 kV/cm

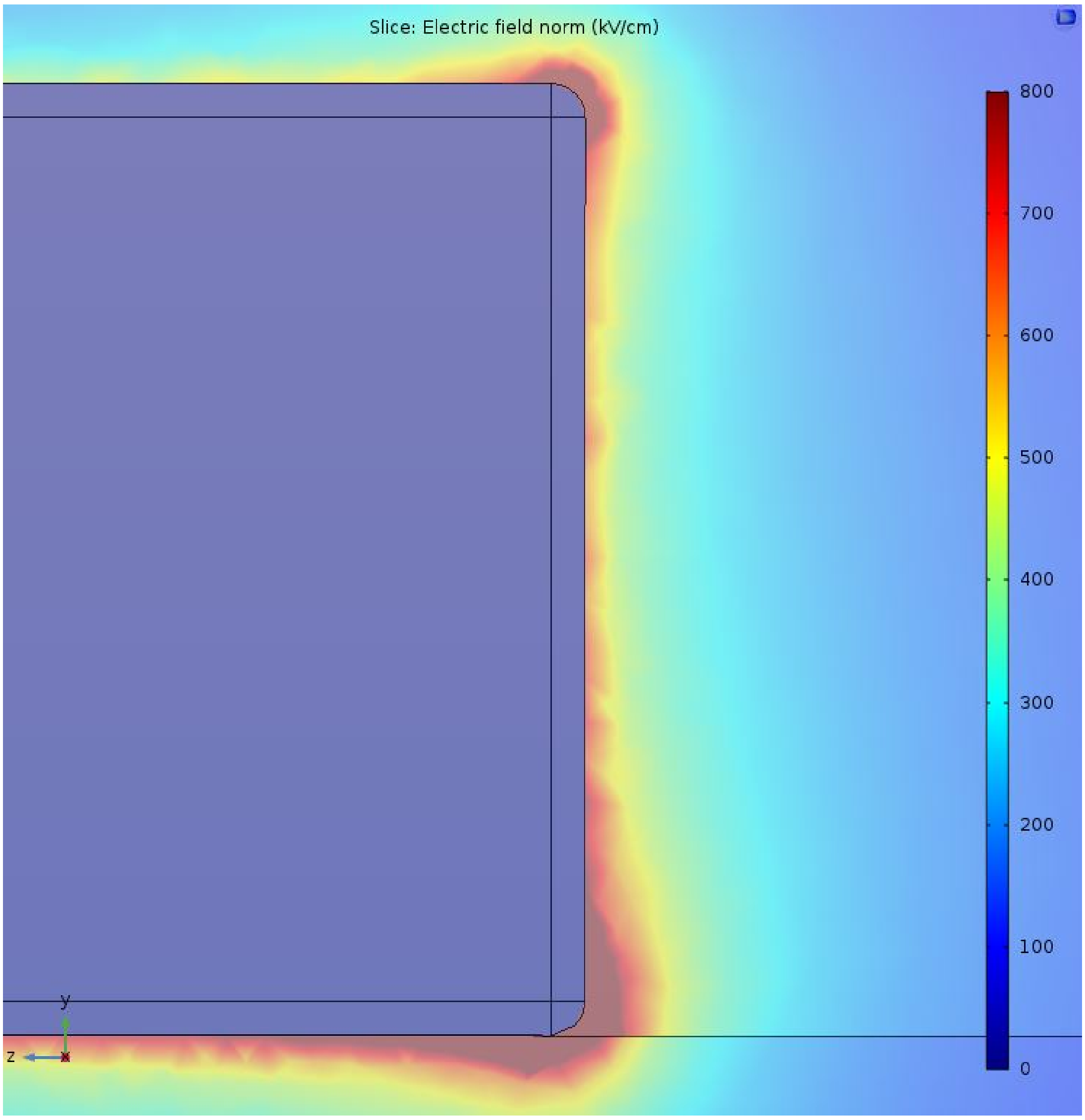

Figure B.24: Case 6, dupont resin , E-field at PDIV, 8.4 kV

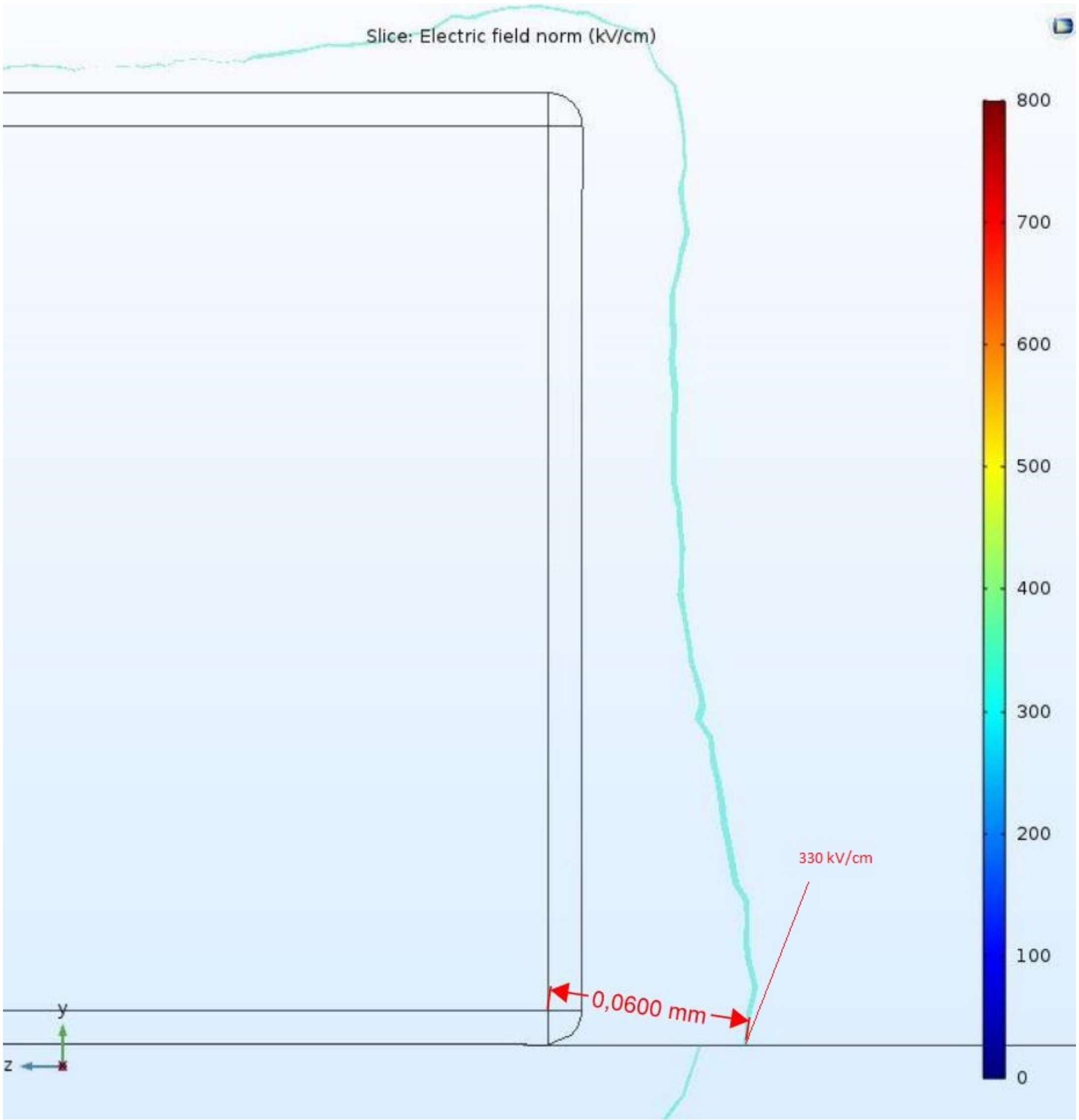

Figure B.25: Case 6, dupont resin , E-field at PDIV, 8.4 kV - measured 50 micrometers from edge

Case 7

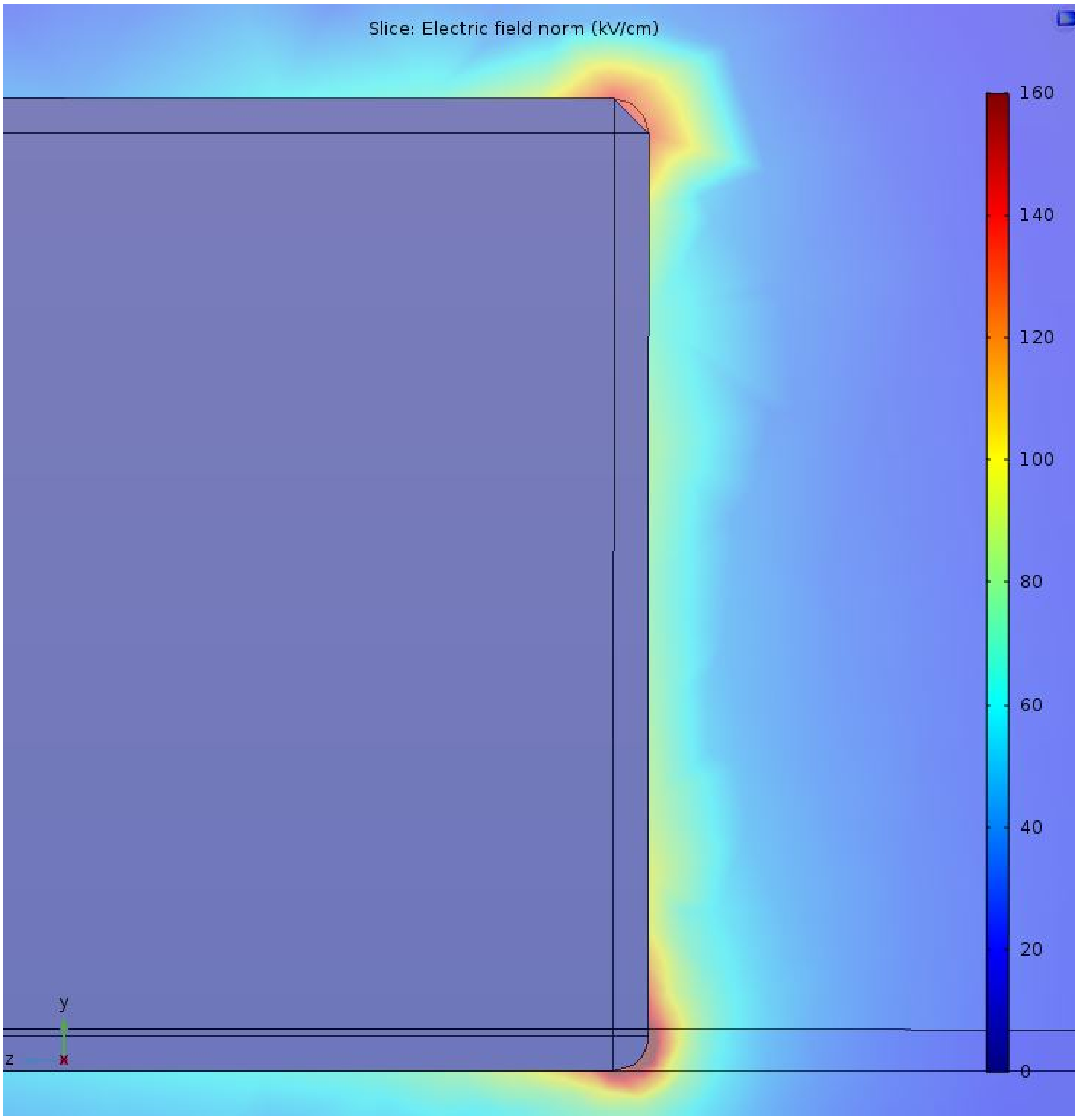

Figure B.26: Case 7, E-field at operating condition, 1.2 kV

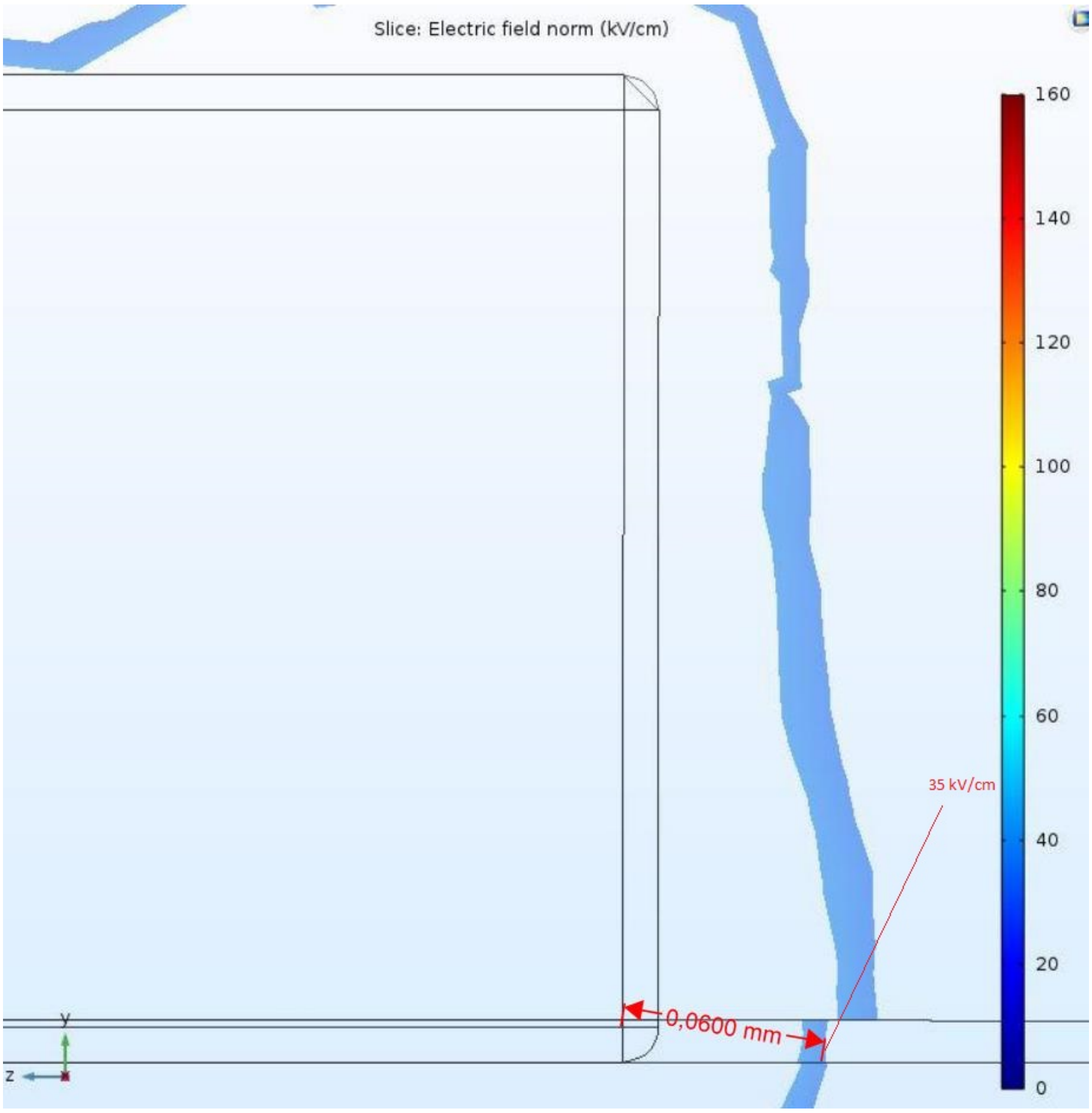

Figure B.27: Case 7, E-field at operating condition, 1.2 kV, measured at 50 micrometers from the edge

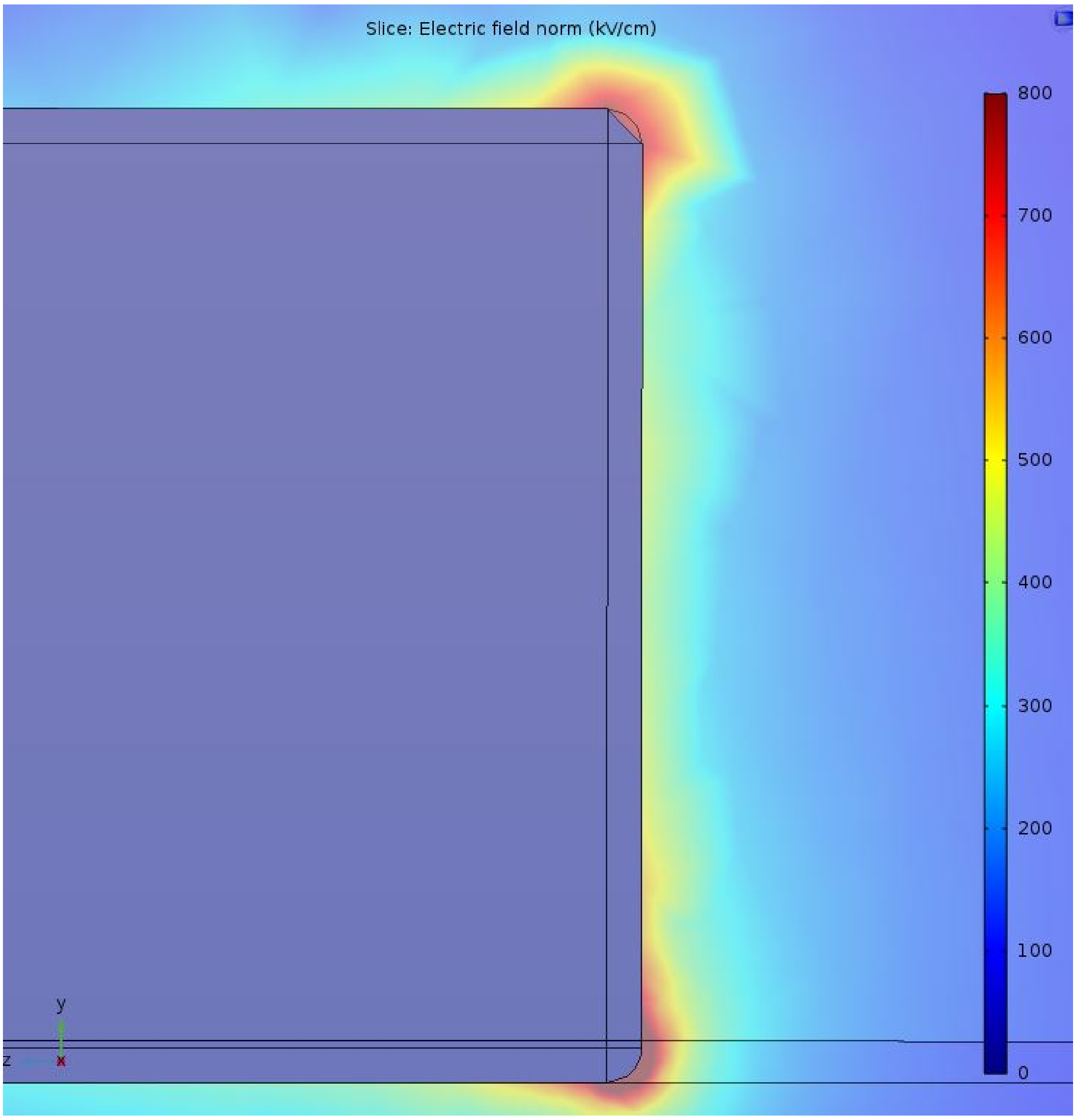

Figure B.28: Case 7,E-field at 6.3 kV

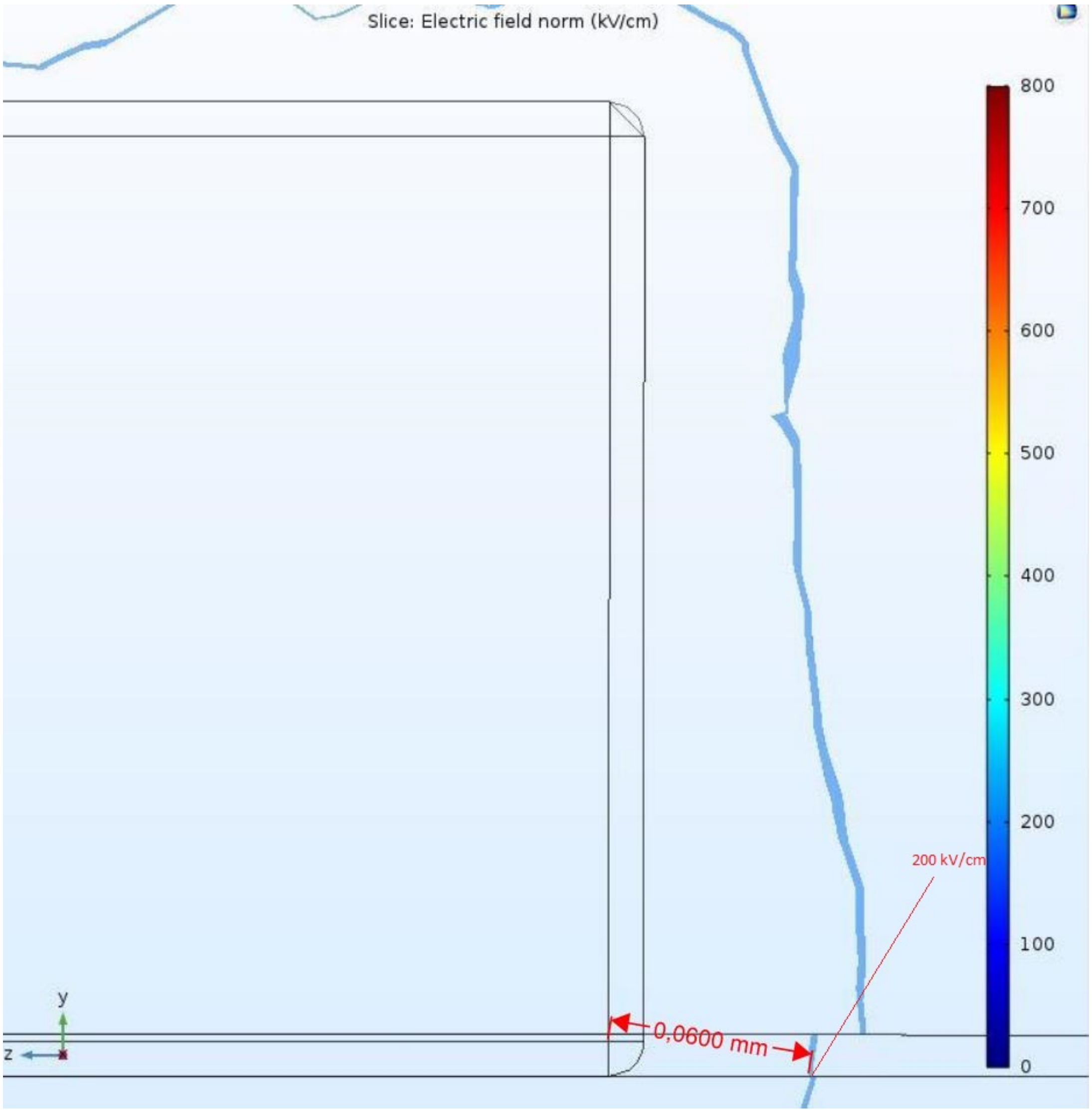

Figure B.29: Case 7, E-field at silicon PDIV, 6.8 kV

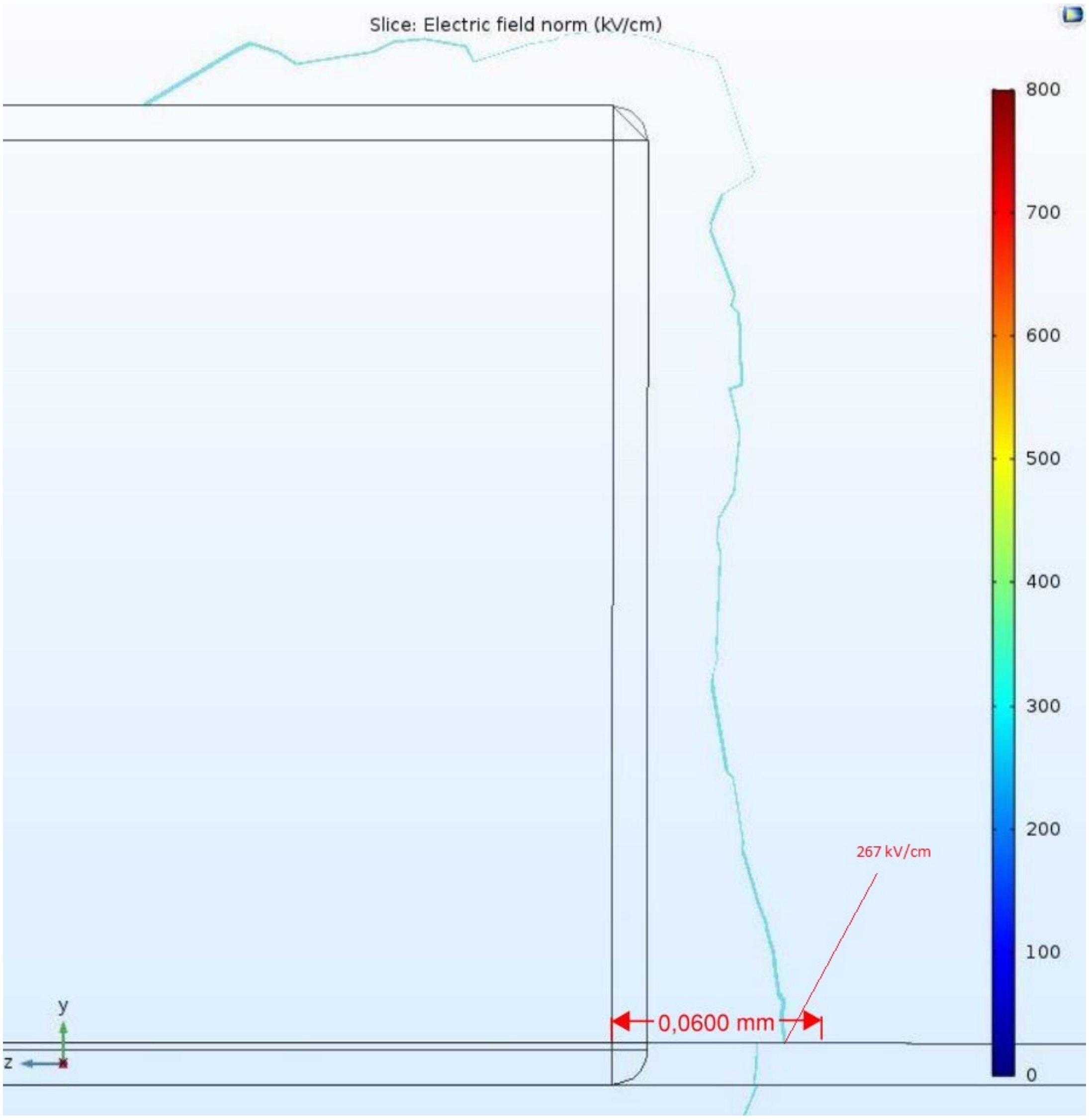

Figure B.30: Case 7, E-field near silicone gel, 6.3 kV - measured 50 micrometers from edge

Case 8

at 1 MHz

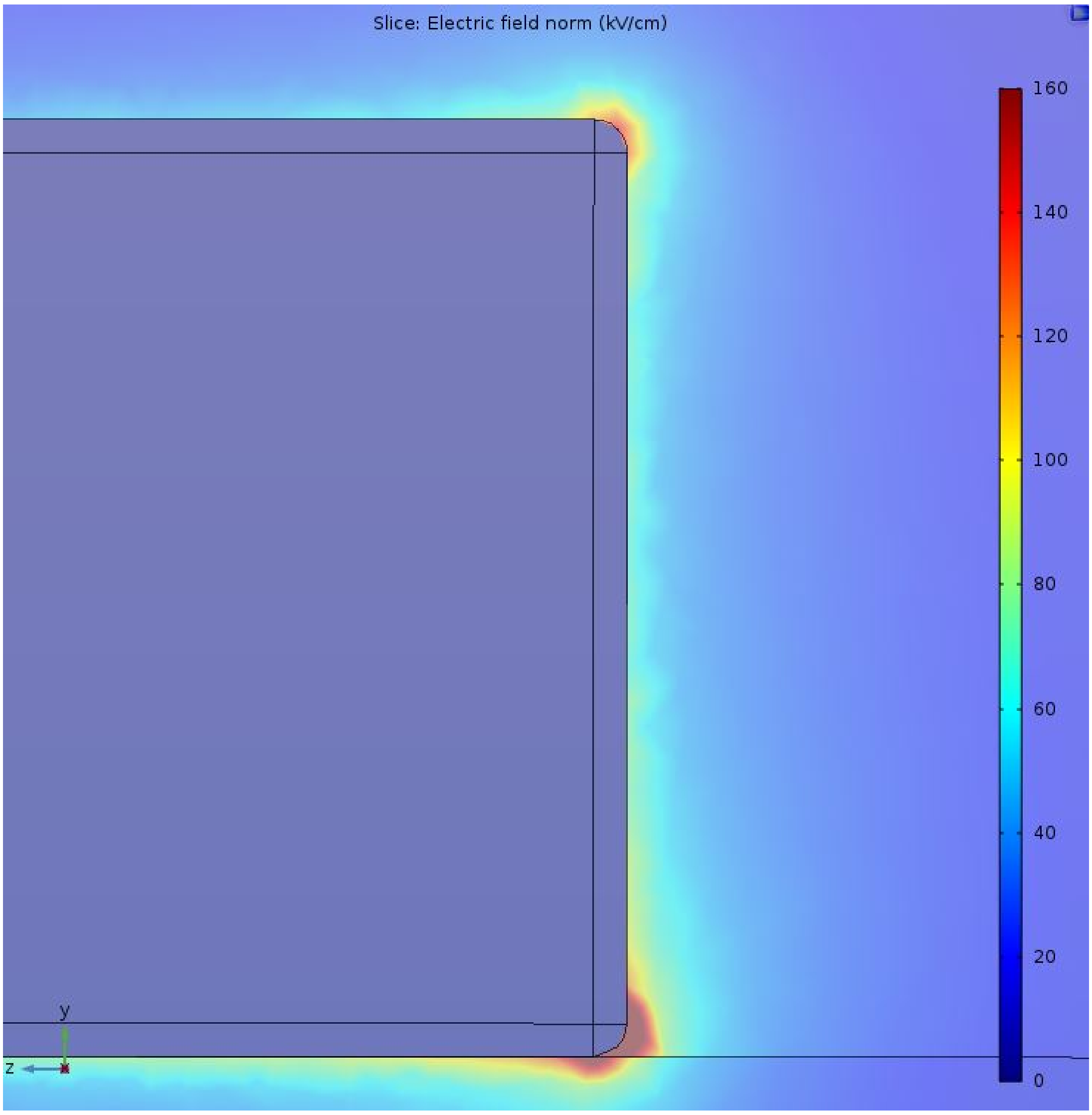

Figure B.31: Case 8, dupont resin, E-field at operating condition, 1.2 kV

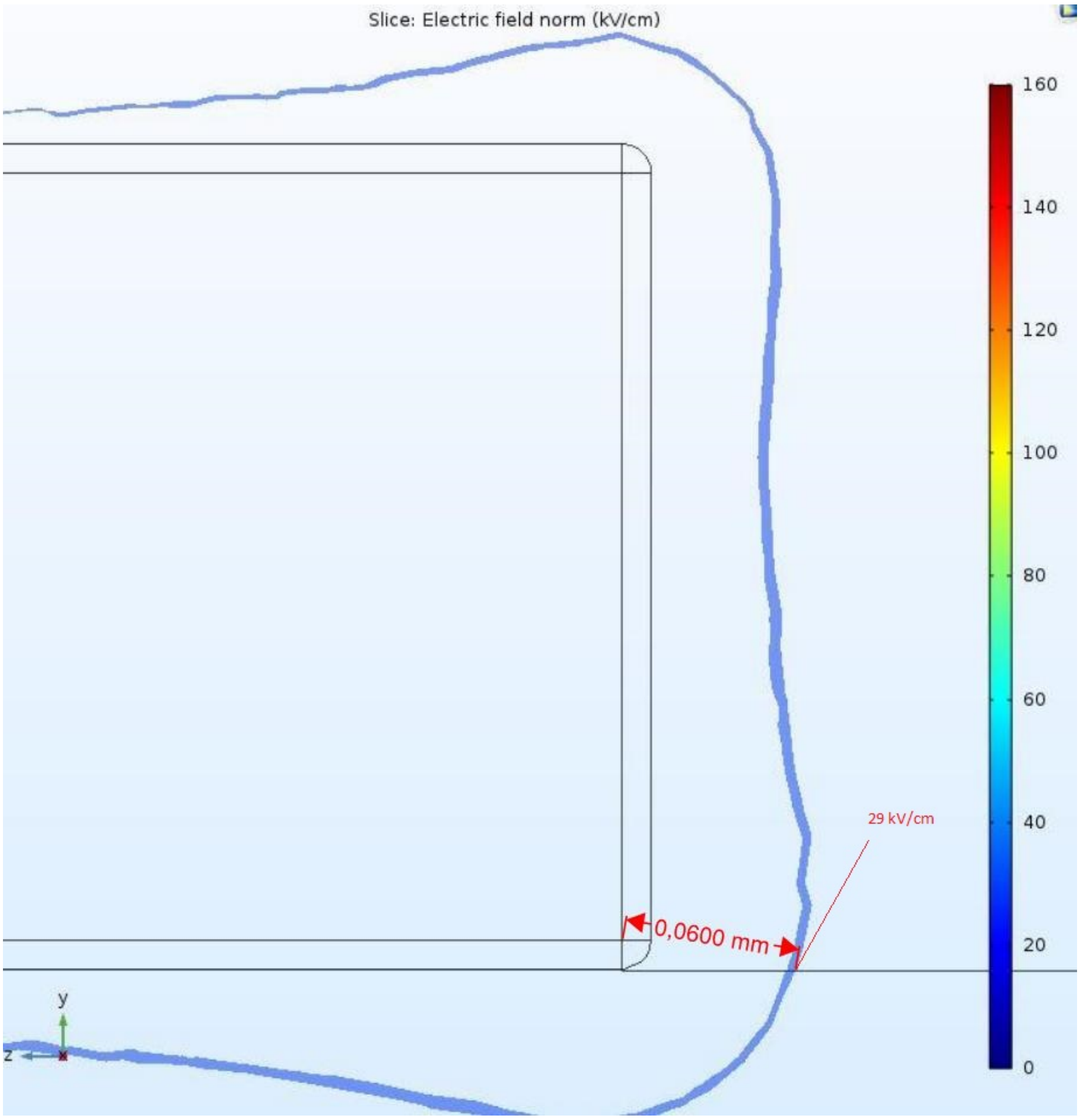

Figure B.32: Case 8, dupont resin, E-field at operating condition, 1.2 kV, measured at 50 micrometers from the edge

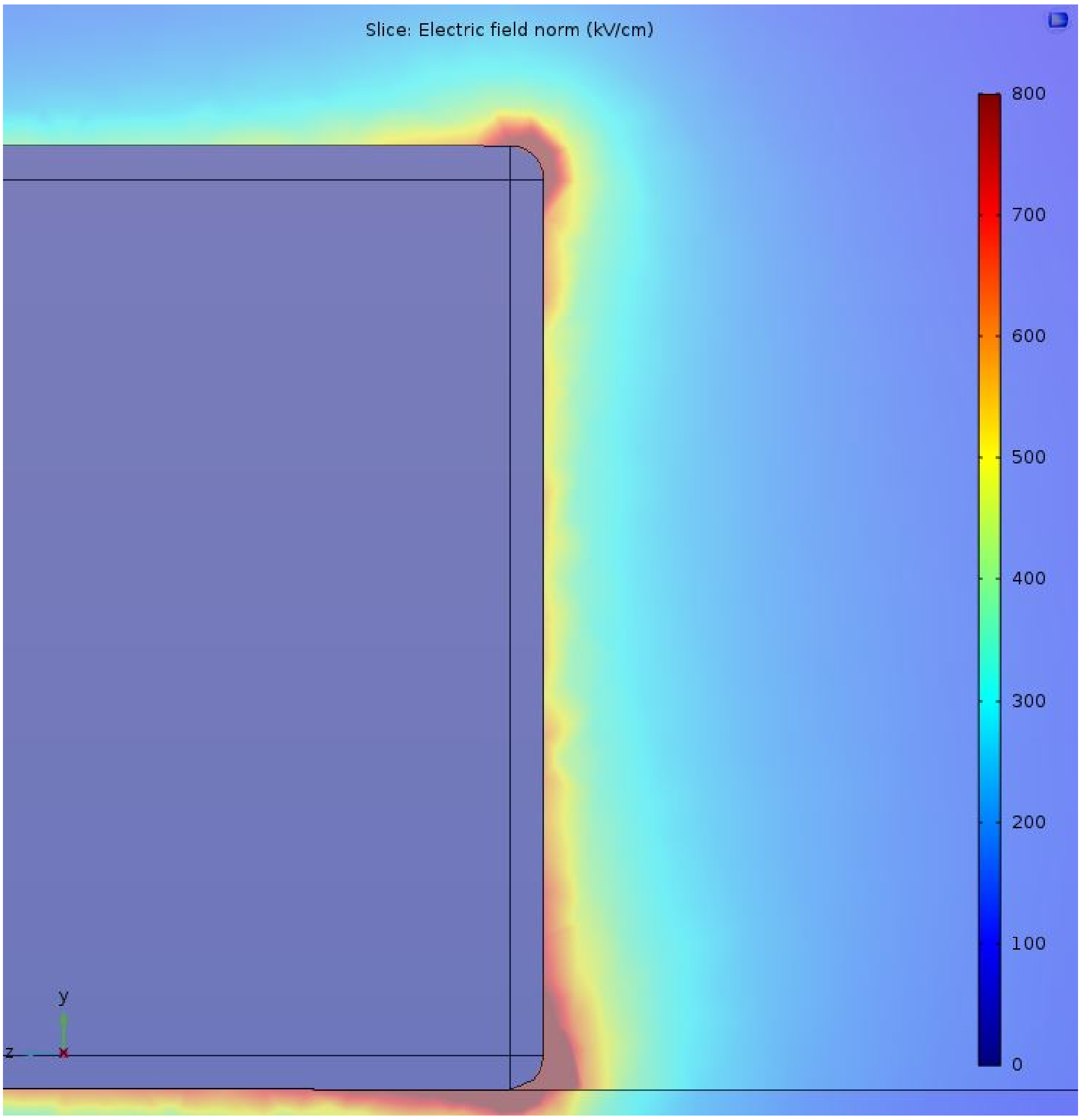

Figure B.33: Case 8, dupont resin, E-field at PDIV, 11.3 kV

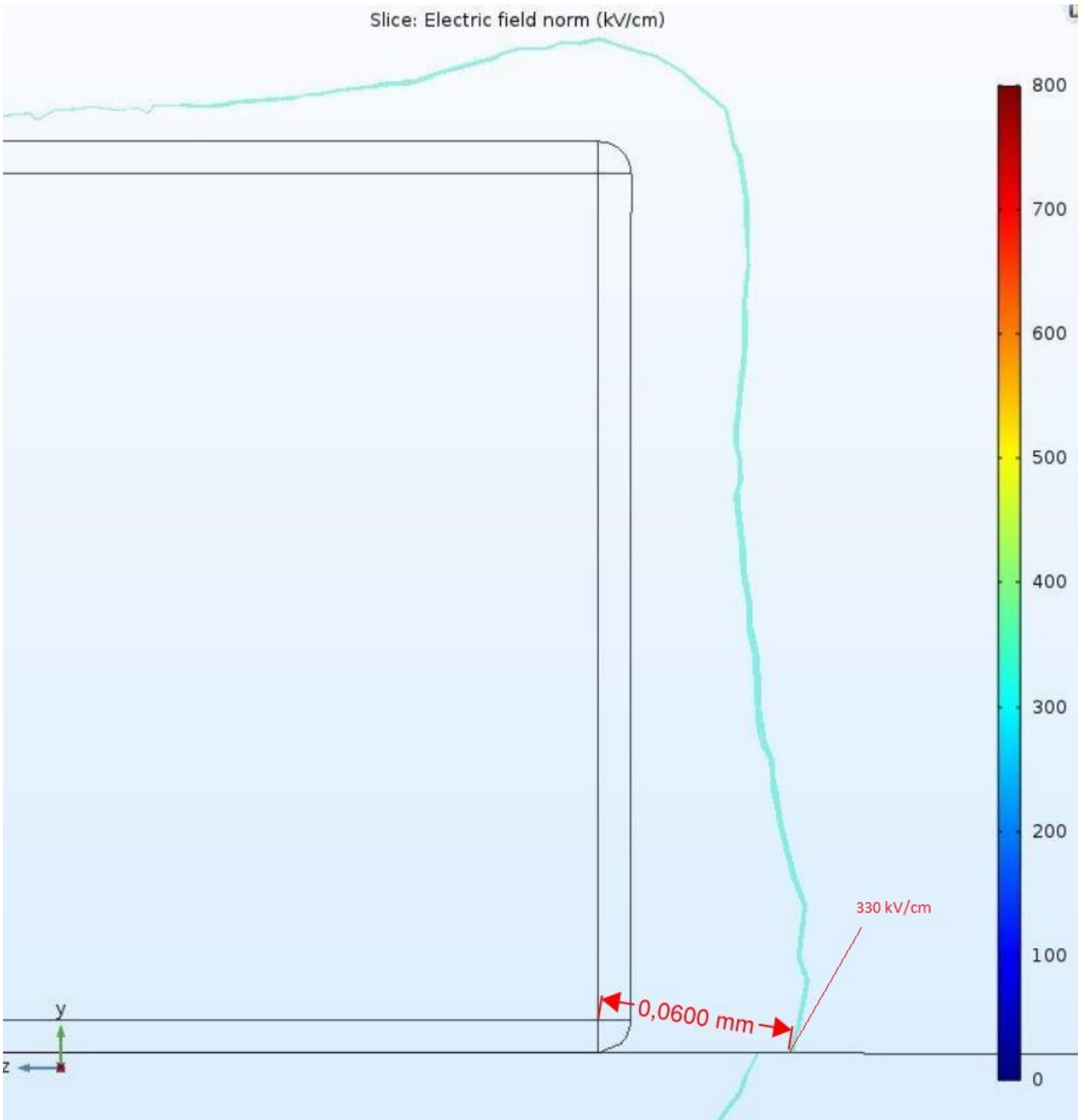

Figure B.34: Case 8, dupont resin , E-field at PDIV, 11.3 kV - measured 50 micrometers from edge

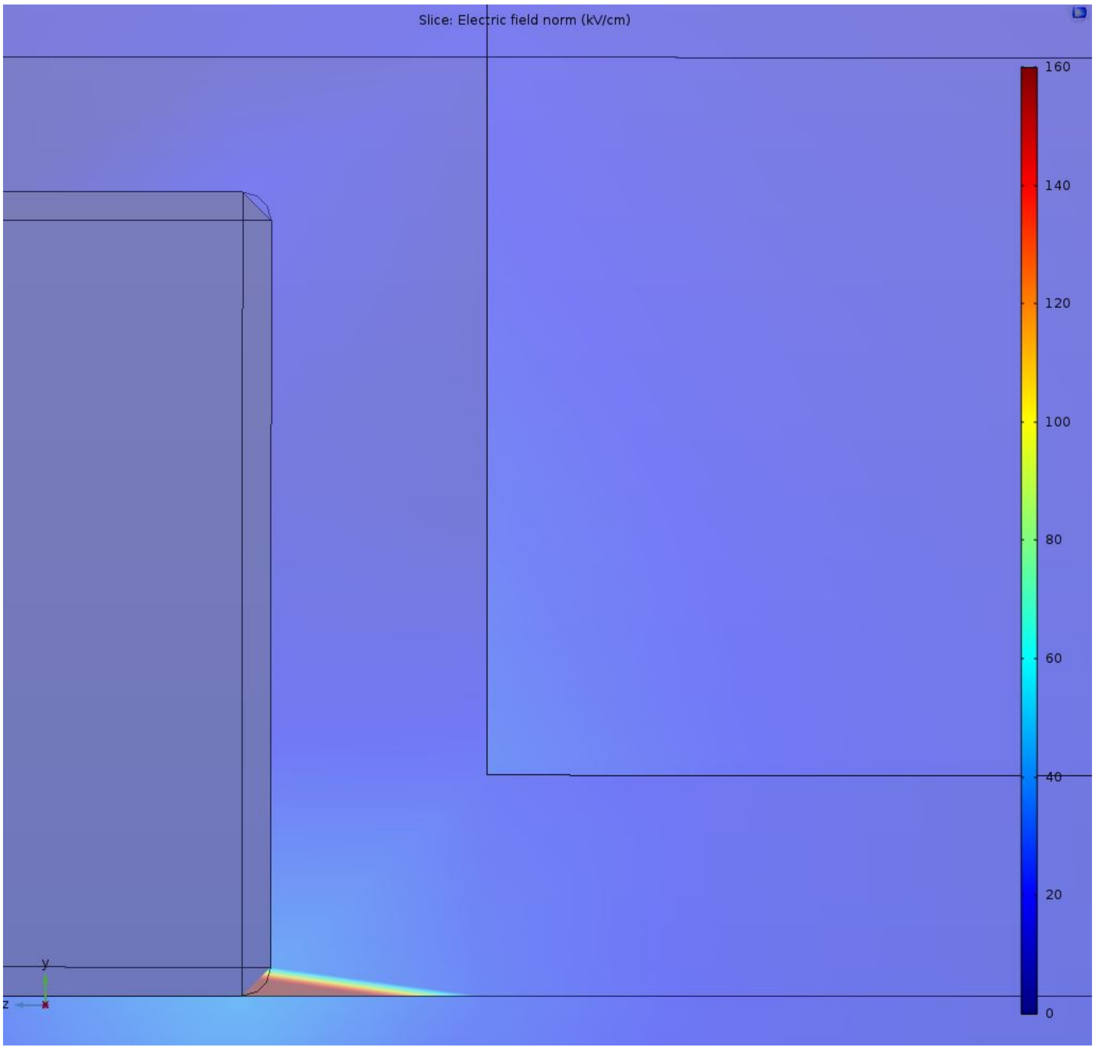

Figure B.35: Case 9, dupont resin at 1MHz and SiC coating, E-field at operating condition, 1.2 kV

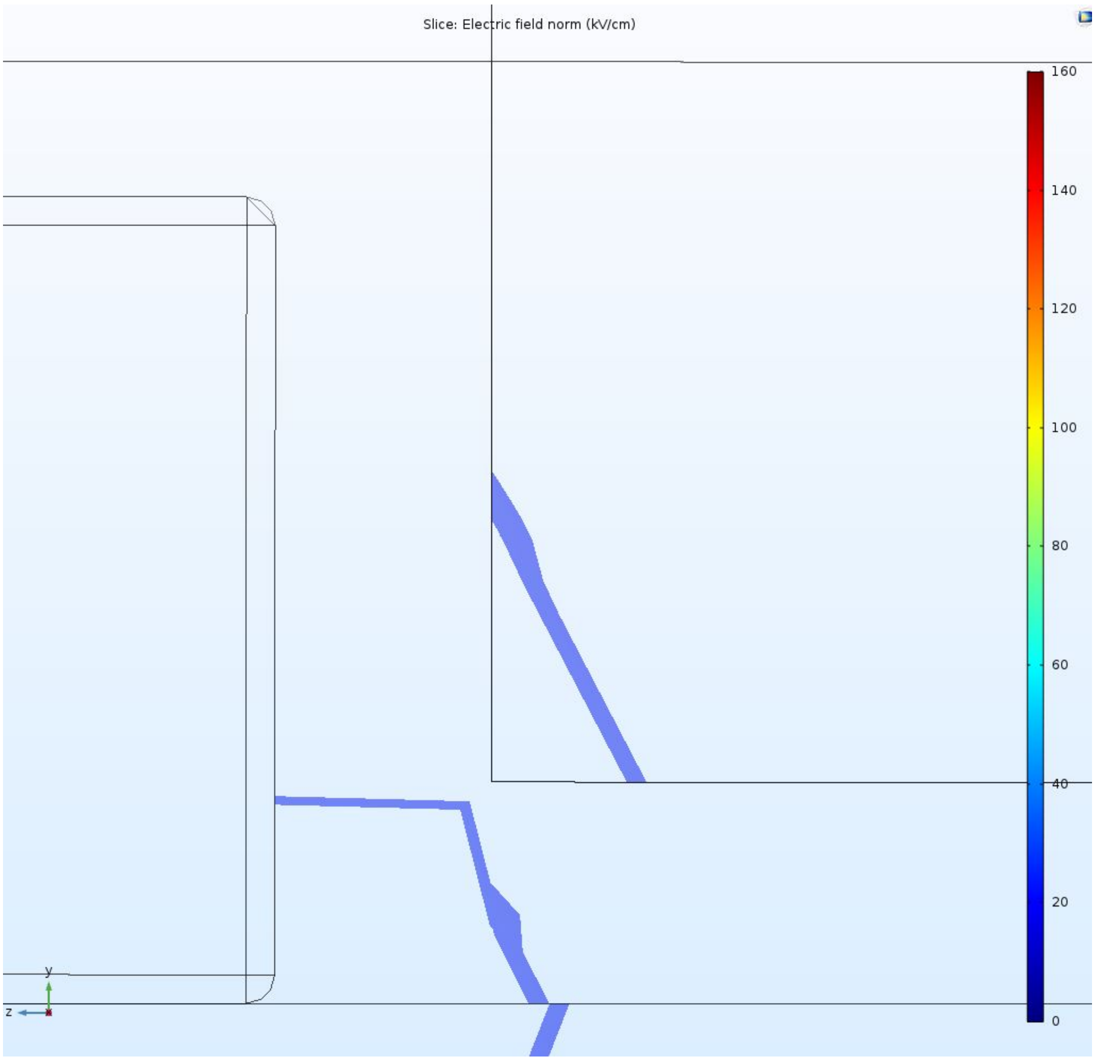

Figure B.36: Case 9, dupont resin at 1MHz and SiC coating, E-field at operating condition, 1.2 kV - measured 50 micrometers from edge

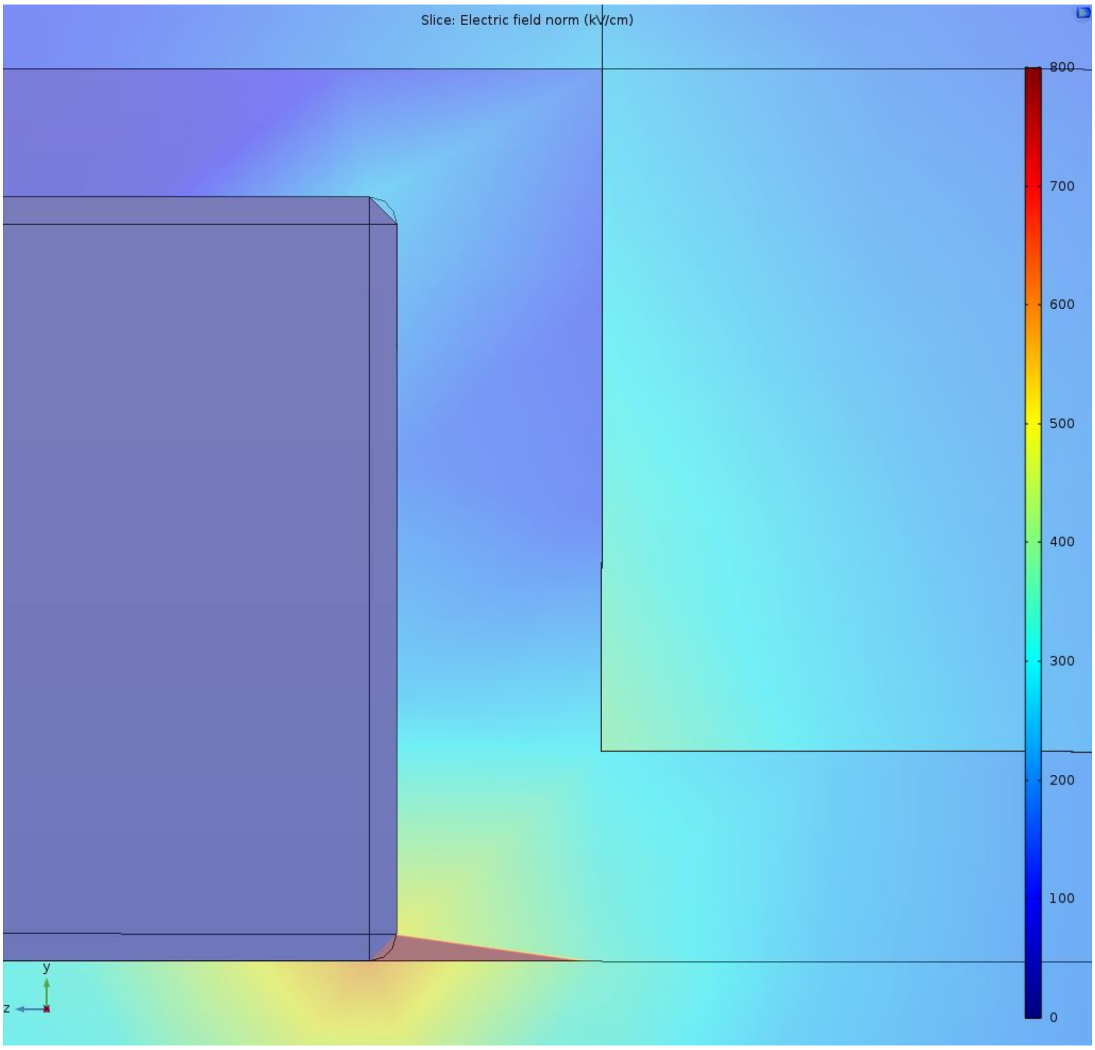

Figure B.37: Case 9, dupont resin and SiC, E-field at PDIV, 16.3 kV

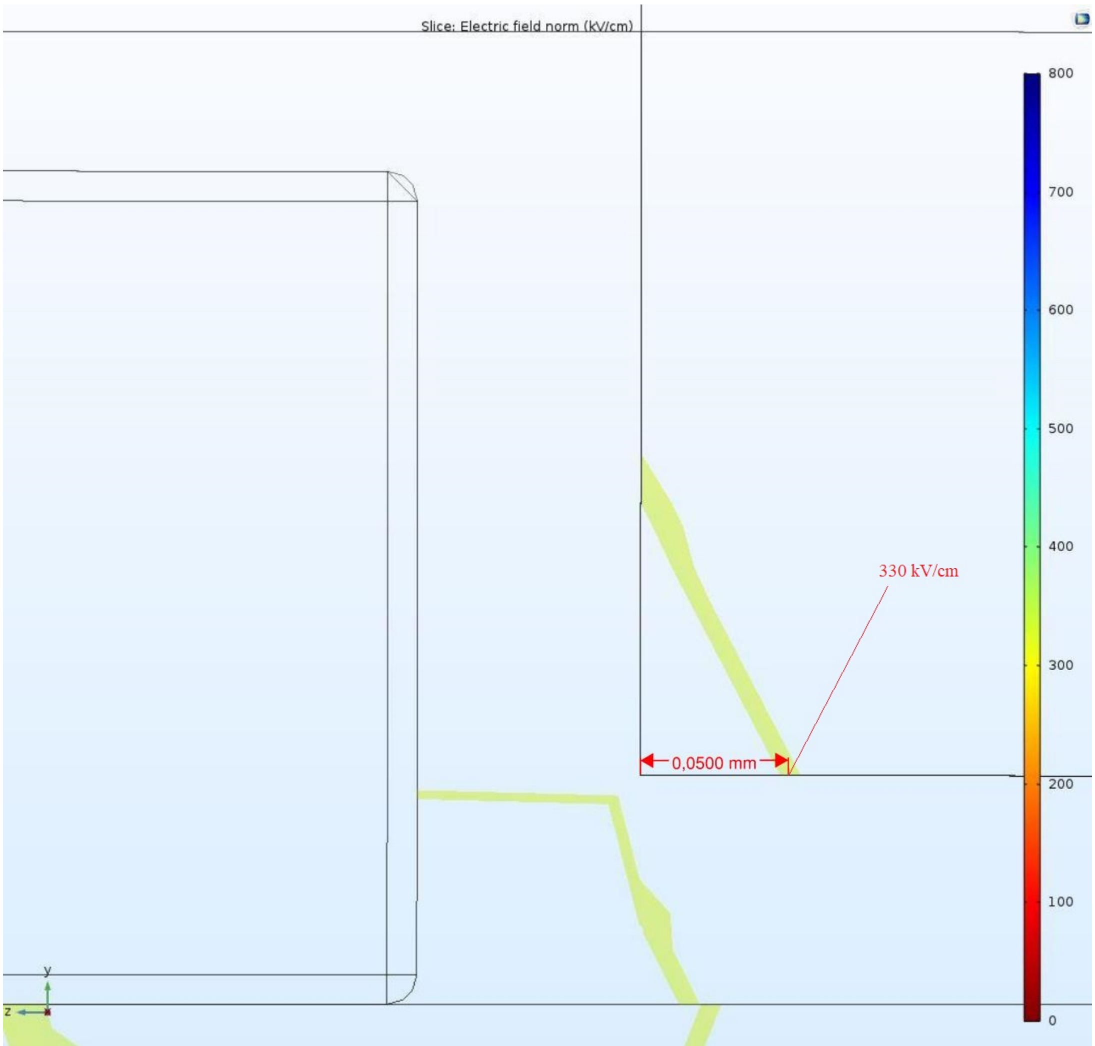

Figure B.38: Case 9, dupont resin and SiC, E-field at PDIV, 16.3 kV - measured 50 micrometers from edge