Power Control in Fuel Cell Electric Vehicle

Design of fuel cell mean output power controller, utilizing parallel super capacitor converter and bank

Jonas Jacobsen

Energy Technology, MCE10, 2020-5

STUDENT REPORT

AALBORG UNIVERSITY

Written in Latex. Pictures created in Inkscape. Simulations done in Simulink and Matlab. SolidWorks used for CAD.

Energy technology
Aalborg University
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AALBORG UNIVERSITY
STUDENT REPORT

Title:
Power control in Fuel cell electric vehicle

Theme:
Mechatronics

Project Period:
Spring Semester 2020

Project Group:
MCE4-1028

Participant(s):
Jonas Jacobsen

Supervisor(s):
Erik Schaltz

Copies: 1

Page Numbers: 98

Date of Completion:
May 28, 2020

Abstract:

The topic of this study is the implementation of super capacitors in a fuel cell electric vehicle. The problem statement is to design a power controller for controlling the mean fuel cell power output. The designed controller is able to accomplish this task under any operation condition imposed by the electric motor, which is regarded as a disturbance to the system. It does so by controlling the DC-bus voltage, which is tied to the fuel cell voltage in the parallel DC-bus. Thus by controlling the DC-bus, the fuel cell voltage and power in extension, is controlled. Feedforward disturbance rejection is used to enhance the disturbance rejection capabilities of the DC-bus voltage controller. The result is that giving a 0-270 W motor power step the DC-bus voltage is only perturbed with a 0.1 to 0.5 V voltage ripple. The mean output power is within 10% of the wanted power value.

Nomenclature

Abbreviations

A/D	Analog to digital conversion
CPU	Central processing unit
D/A	Digital to analog conversion
DMAC	Direct memory access channel
FOC	Field oriented control
KCL	Kirchoff's current law
KVL	Kirchoff's voltage law
MCU	Microprocessor controller unit
PEM	Polymer Electrolyte Membrane
PMSM	Permanent magnet synchronous machine
PWM	Pulse width modulation
SCB	Super capacitor bank
SCC	Super capacitor converter
SISO	Single input single output
TCC	Timer compare channel

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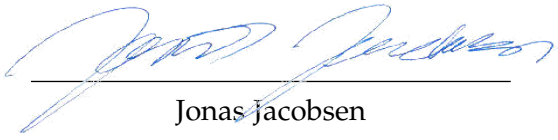
Preface

This masters study is made with Shell Eco-marathon in mind. Shell Eco-marathon is a competition that gives birth to cutting edge technology. The aim of my study is to analyse the power system of the newest car Cimbrer III, in-depth and come up with a power management scheme, which is useable in a race and understandable for future members of the team. Covid-19 unfortunately meant only a single experiment was performed before the lockdown. I would like to thank my team who have worked tirelessly on the Ecoracer project for years and I hope this study will serve as a theoretical basis for the time to come. I would also like to thank my supervisor Erik Schaltz for his project guidance in these trying times.

Aalborg University, May 28, 2020



Jonas Jacobsen
<jjacob15@student.aau.dk>

Chapter 1

Introduction

Contents

This study is about the implementation of super capacitors in the Ecoracer, this entail a Super Capacitor Converter (SCC) and a Super Capacitor Bank (SCB). The Ecoracer is a fuel cell prototype vehicle, in the urban concept category. This means is has similar proportions and requirements as a normal car. The vehicle competes in a yearly competition called Shell Eco-marathon hosted by Shell. Universities from around the world compete against each other, aiming to achieve the highest efficiency within the set of rules possible. The vehicle runs on pure hydrogen with an equivalent mileage of over 600 km per litre gasoline. Even a few percent increase in efficiency, can mean tens of kilometres of extra mileage. This means that to win, the teams have to utilize state of the art technologies and do it better than the other teams. The biggest change during the last years have been the implementation of super capacitors. With super capacitors it is possible to direct the power flow within the vehicle to a much higher degree. This means that tactical or efficiency based control systems can be designed to improve the vehicles performance in the race. In other words, super capacitors are a necessity for Team Aalborg Energy to keep competing on an international higher education level. The main issue of not having super capacitors is that the power drawn from the fuel cell is directly dictated by the motor. This can be disadvantageous because for fuel cells, fuel efficiency diminishes the more power is drawn. It should be noted that batteries or flywheels are not allowed in this competition class, so super capacitors are the only solution to control the power flow. Super capacitors, with a proper implementation, will open up the vehicle for many potential efficiency improvements.

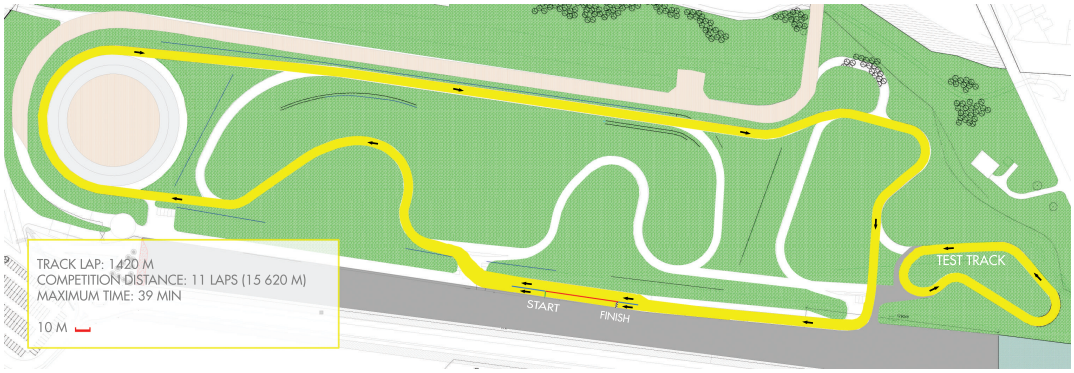


Figure 1.1: Map of track Shell Eco-marathon 2019

1.1 Project overview

In 2019 the competition, Shell Eco-marathon, took place on the track shown in Fig. 1.1. The competition entailed driving 11 laps, a total distance of 15620 m, in less than 39 minutes. Additionally the vehicle had to start and stop at the finish line after each lap, to emulate urban driving. This driving pattern resulted in operation points for the motor and fuel cell that are all over the possible operation space. In other words, neither the motor or fuel cell have been efficiency optimized. This problem leads to this enhancement project for the vehicle. The project is separated into two sub-projects. The first sub-project is to integrate the SCC and SCB into the existing system and design a power control solution. The second sub-project is to optimize the efficiency with the increased power control available from sub-project one. This study is solely about sub-project one and it is paramount that this is finished before moving onto sub-project two.
To give a simple overview of the system refer to Fig. 1.2. The power train is divided into three separated modules; The fuel cell, the motor and the SCB. The fuel cell is unidirectional while the motor and SCB are bidirectional in power flow. This, for example, means that when the motor is returning power to the DC-bus, then the SCB must accept this power because the fuel cell can not. If the SCB does not absorb this power then the DC-bus capacitor will blow up. The motor power is controlled by a driver, who will attempt to follow an operation strategy, possibly mathematically optimised. However, because this is a human interface with uncertain factors like other vehicles, the motor load be erratic. Thus the SCB has to designed in a robust manner so that no matter what the driver sets the motor to, the power flow will be balanced and the DC-bus voltage under control. This leads to the four bulletins written in Fig. 1.2. The SCC/SCB must provide power control, DC-bus voltage control, State of charge (SOC) control of the SCB and alleviate peak power demands.
It is also the teams ambition that the power train is modular. In other words, that

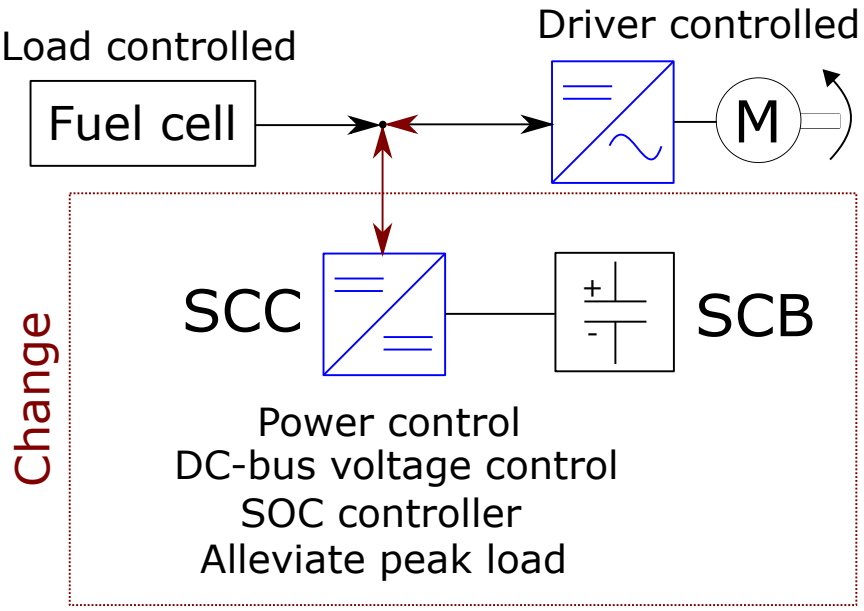


Figure 1.2: Power train simplified schematic. Arrows indicate power flow directions. The node at which all flows converge is a DC-bus.

it is possible to swap out modules like the fuel cell and fan controller or the SCC and SCB quickly. The reason for this is part because of the racing conditions, if a module fails, then a fully tested replacement can be swapped in. Another reason is that by making the system modular, separate in-depth studies of the modules can be conducted without taking the entire system into account. In other words, the SCC and SCB designed in this study are entirely self-contained, if they fail the vehicle can revert to the old power train without them.

1.2 Problem statement

Originally the study was focused on PCB design and practical implementation of a super capacitor module. However, this changed after Covid-19 to system modelling, control design and simulation. Because the problem statement was forcefully changed halfway through the project there are elements of practical implementation in the study from before the change.
The primary goal or project statement is to derive a power control solution that can control the power of the fuel cell using the super capacitor module. The super capacitor module should be able to do this no matter how the driver uses the motor. It could be that the motor is regenerating power or using power in pulses. No matter what it is, the super capacitor module should be robust enough to handle it and control the control the fuel cell power. The structure of the problem

solution is to analyse and derive a model for each of the system modules. The super capacitor module is subject to a large degree of design freedom because it is a new module. Whereas the fuel cell and motor are not. Yet these two still need a model in order to simulate the entire system. The procedure to answer the problem statement is written in the sub tasks below. Sub task #2 is a necessity to acquire a complete image of the vehicle operation. Sub task #5 is one of the largest tasks, because controlling the current on both sides of a DC/DC converter means to control the power. If the current control is not good enough then this will affect the overall performance of the power control solution. Sub task #6 is about putting the results of sub tasks #1 through #5 together and designing the solution to the problem statement.

Problem statement:

Design flexible power management control for low-power fuel cell and super capacitor electric vehicle (The Eco-racer)

Sub tasks:

#1 Derive fuel cell model. (Chapter 2).

#2 Derive mechanical model. (Chapter 3).

#3 Derive motor model and design current controller. (Chapter 4).

#4 Derive super capacitor bank model. (Chapter 5).

#5 Derive super capacitor converter model and design current controller. (Chapter 6).

#6 Design power control and simulate the entire system. (Chapter 7).

It is an option to skip from here to Chapter 7 where the problem solution is presented. In Chapters 2 through 6 models and controller designs are presented. The results in these Chapters play a large role in the problem solution so it is encouraged to read them as well.

Chapter 2

Fuel cell analysis

Contents

The fuel cell is the component of this system that has the least amount of configuration freedom. Therefore it makes sense that it is the first component that is analysed. This way the fuelcell analysis can be used to make design decisions regarding the other system components. In Fig. 2.1 the fuel cell module is shown. In the picture a Troowin PEM fuel cell rated around 1000W can be seen, along with the fuel cell circuit board visible at the front. The fuel cell circuit boards primary function is to cut off hydrogen supply in case of a safety switch being triggered. On the underbelly of the fuel cell there is a fan controller board, this board controls the temperature by controlling the airflow through the stack.
This fuel cell analysis is based on the premise that no/little electrochemical knowledge is required. In other words there are three variables; stack voltage, stack current and stack temperature. The temperature affects the electrochemical reaction and thus influences the current-voltage relation or commonly called the polarisation curve. This curve is an essential performance graph for a fuel cell. Other factors like water accumulation, which decreases the reaction area and thus the voltage over time, is disregarded since it requires electrochemical knowledge to analyse properly. In other words, the polarisation curve is assumed to be constant in time.

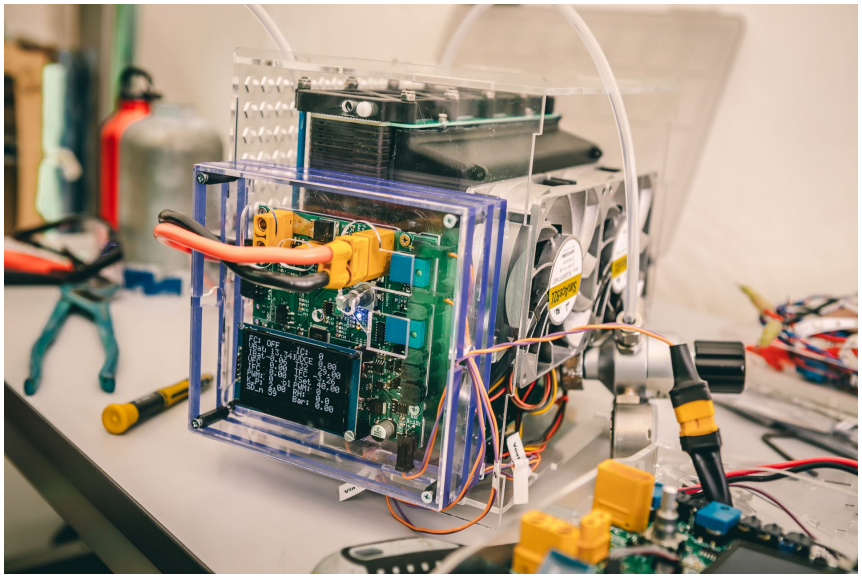


Figure 2.1: Troowin PEM fuel cell module as used at Eco-marathon 2019.

2.1 Fuel cell model

The goal of this section is to obtain a simple approximate electric model from the limited data available. The data available for fuel cell analysis is shown in Fig. 2.2. It can be seen on Fig. 2.2(b) the temperature is not constant. This has an effect on the fuel cell voltage and thus the polarisation curve. However, since this effect is electrochemical and outside the scope of this study, it is assumed that in the final system the fuel cell has temperature control.
A simple polarisation curve fitting can be acquired by assuming that the fuel cell will never exceed a current of 15 A, corresponding to around 400W. Then the only electrochemical effects to be considered are the activation losses and the ohmic losses. The activation losses can be seen as a sharp drop in stack voltage, when drawing a small amount of current. The ohmic losses can be seen as a linear decrease in voltage, as the current is increased further. [1] Kim et al. defines a simple empirical model seen in Eq. (2.1) which disregards concentration losses. [2]

$$u_{fc} = E0 - i_{fc}R - Aln(\frac{i_{fc}}{I_{ex}}) \tag{2.1}$$

$$E0 = 47\left(1.482 - 0.000845T_K + 0.0000431T_K ln(p_{H_2}p_{O_2}^{0.5})\right) \tag{2.2}$$

Where E0 is the Nernst voltage calculated on the basis of absolute temperature T_K and partial pressure of the reactants p_{H_2} and p_{O_2}. It is assumed that the reactants have a constant temperature of $30°C$ and that the pressure of the hydrogen is 1.5 bar and the pressure of the oxygen is 1 bar. This results in a Nernst voltage of

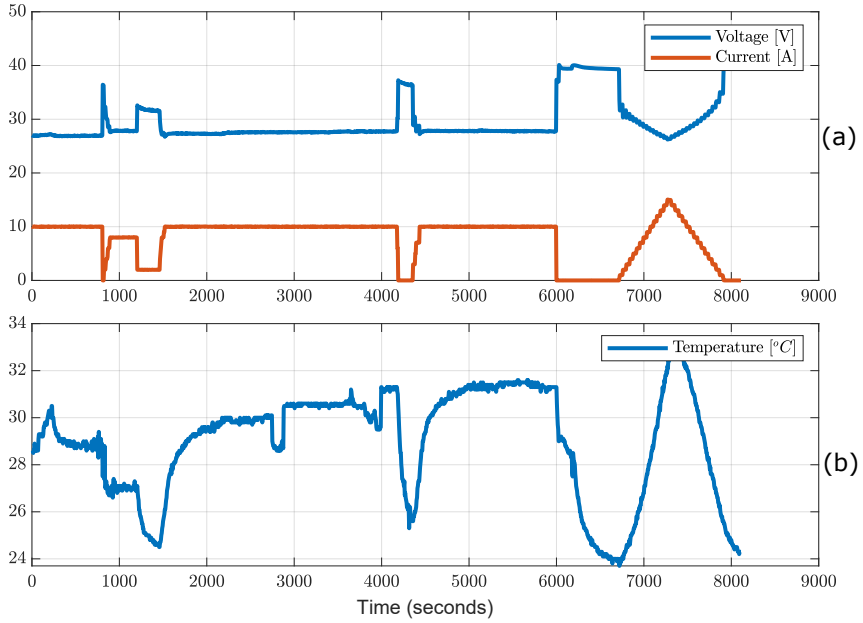


Figure 2.2: Fuelcell data, courtesy of AAU Associate professor Simon Lennart Sahlin

51.707 V, which is the maximum theoretical voltage of the fuel cell at no load. This corresponds to 83% of the burning value of hydrogen. [1]
The power of the fuel cell can be expressed by multiplying to stack voltage with the stack current, this is shown in Eq. (2.3). Because the voltage is a function of the current, power control essentially has one degree of freedom. Controlling either voltage or current will result in power control. In this study the stack terminals are connected in parallel to the DC-bus, why controlling the DC-bus voltage, also means to controlling the fuel cell voltage. By controlling the fuel cell voltage the fuel cell current and therefore power is also controlled. To avoid reverse currents, into the fuel cell, a diode can be used. It should be noted, that a diode will introduce a voltage drop from the stack terminals to the DC-bus, making the previous statement less accurate.

$$P_{fc} = n_{cells} i_{fc} u_{fc} \tag{2.3}$$

where $n_{cells} = 42$ and P_{fc} is the electrical power at the stack terminals.

2.2 Fuel efficiency of fuel cell

The fuel efficiency of the fuel cell can be expressed by dividing the cell voltage by 1.481 V. This is the equivalent voltage per cell that corresponds to 100% of the burning value of hydrogen. So the fuel cell stack efficiency can be calculated as shown in Eq. (2.4). [1]

$$\eta_{fc} = \frac{u_{fc}/n_{cells}}{1.481} \tag{2.4}$$

Where, u_{fc} is the stack voltage and η_{fc} is the theoretical efficiency of the fuel cell. The factor 1.481 V could also be found by computing the Nernst voltage from Eq. (2.2) per cell. This is around 1.23 V, which corresponds to 83% of the burning value of hydrogen and then multiplying it by 1.0/0.83 to get 1.481 V. [1]
In Fig. 2.3(a) on the left axis the model shown in Eq. (2.1) is fitted to the data shown in Fig. 2.2(a). In Fig. 2.3(b) on the right axis the power is calculated by multiplying the fitted voltage model to the current as shown in Eq. (2.3). In Fig. 2.3(b) the fuel efficiency is calculated based on the fitted voltage model and Eq. (2.4). It can be seen in Fig. 2.3(b) that the fuel efficiency decreases when the power increases. So in conclusion, to get the most energy out of the hydrogen fuel, the fuel cell power has to be kept as low as possible. In the next chapter the vehicle and mechanical load will be analysed, to give an idea of the operation region, where the fuel cell will be operated.

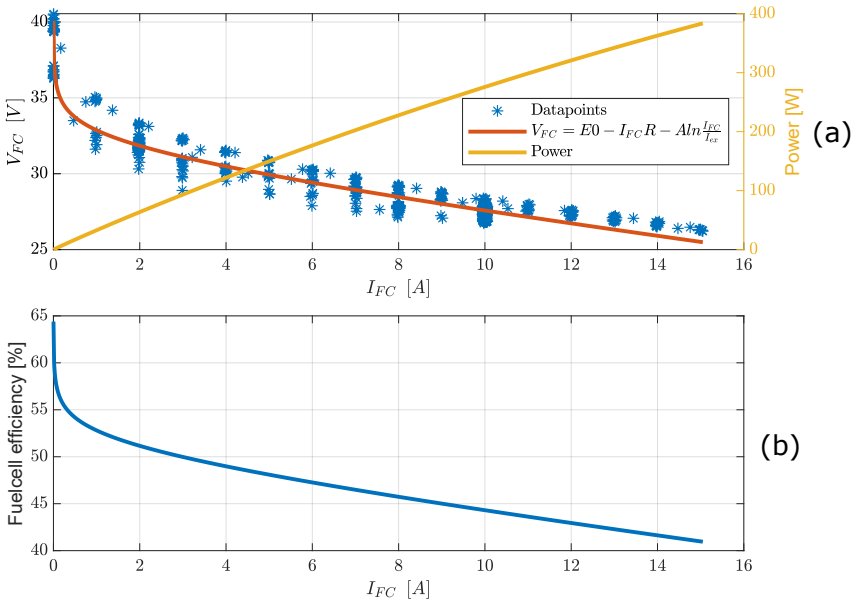


Figure 2.3: (a) left y-axis: Measured and fitted stack voltage. Fit equation is shown in Eq. (2.1). Right y-axis: Power at given current. (b) Fuel cell efficiency calculated using Eq. (2.4).

Chapter 3

Vehicle model and mechanical load analysis

Contents

The vehicle that is Cimbrer II has been mechanically optimised over the years. This involves aerodynamic drag reduction and attention to detail when it comes to bearings, tires, weight and so on. This means that there is accumulated enough data to model the vehicle in this Chapter. The majority of this Chapter is about constructing a mechanical model of the vehicle. At the end of the Chapter, the mechanical model is used to simulate how much torque is required to drive a lap, exactly as fast as a data logged attempt from Eco-marathon 2019.

3.1 Vehicle model

The forces acting on the vehicle are illustrated in Fig. 3.1. The resulting acceleration is a sum of all the forces acting on the vehicle in the vehicles direction. The force balance is shown in Eq. (3.1), where parameters can be viewed in Tab. 3.1. Aerodynamic drag and rolling resistance will always work against the motion. The elevation force depends on the incline of the road and the driving force is the force acting from the back wheel onto the road, assuming no slip between the two surfaces. The driving force F_x is what the drive train supplies to the force balance. If F_x is positive then the car is accelerating and if it is negative then the car is decelerating. In Eq. (3.2) the driving force is isolated from Eq. (3.1).

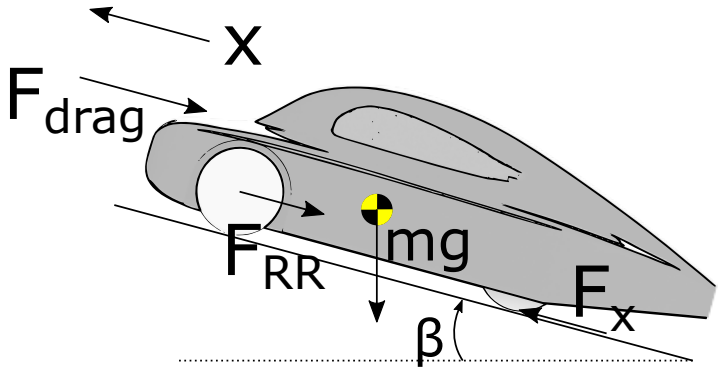


Figure 3.1: Forces acting of vehicle. Inspiration from [3].

$$m_{car}\dot{v} = -F_{drag} - F_{RR} + F_x - F_{elev}(\beta) \tag{3.1}$$

$$F_{drag} = \frac{1}{2}\rho C_D A_v v^2, \quad F_{RR} = m_{car} g C_{RR}, \quad F_{elev} = m_{car} g sin(\beta)$$

$$F_x = m_{car}\dot{v} + \frac{1}{2}\rho C_D A_v v^2 + m_{car} g C_{RR} + m_{car} g sin(\beta) \tag{3.2}$$

Parameter	Value[unit]	Note
m_{car}	∼170[kg]	Point mass of vehicle
v	$(-)[m/s]$	Linear speed of vehicle
F_{drag}	$(-)[N]$	Aerodynamic drag force
F_{RR}	$(-)[N]$	Rolling resistance force
F_x	$(-)[N]$	Drivetrain propulsion force
g	$9.82[\frac{m}{s^2}]$	Gravitational acceleration constant
β	$(-)[^\circ]$	Tilt angle of the road
ρ	$1.2041[\frac{kg}{m^3}]$	Density of air at 20°C
A	$0.8440[m^2]$	Frontal area of car
C_{RR}	$\frac{1.5}{1000}$[-]	Rolling resistance constant

Table 3.1: m: official weight of car + driver 2019. C_{RR}: Official rolling resistance of Michelin UC95/80R16 tyre. C_D, A: Calculated constants from CFD analysis of car shape in [4].

Because the transmission gearing is constant the load can be viewed from the motors point of view. The gearing is defined as the number of teeth on the wheel gear (n_w) divided by the number of teeth on the motor gear (n_m). The range of G is between 5 and 10 on the vehicle.

$$G = n_w / n_m$$

With prior knowledge of the motors efficiency as a function of rotational speed

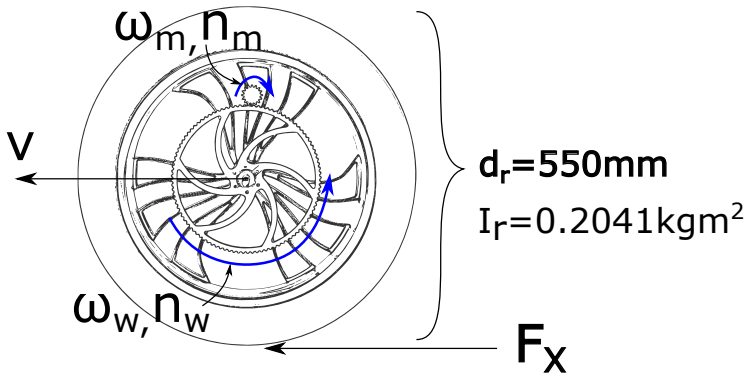


Figure 3.2: motor to road transmission

and torque the gearing can be chosen accordingly. However, this optimization is reserved for another study.
An image of the motor to road transmission is showed in Fig. 3.2. Where v is the linear speed and ω_m, ω_w are the motors and wheels rotational speed, respectively. The mechanical load as seen by the motor is defined in Eq. (3.3).

$$\tau_{load} = \frac{F_x \cdot r_{wheel}}{G} \tag{3.3}$$

Where r_{wheel} is the radius of the wheel, half of the diameter d_r defined in Fig. 3.2. The torque equilibrium seen at the motors point of view is defined as shown in Eq. (3.4).

$$I_r \dot{\omega_m} = \tau_m - \tau_{load} - B\omega_m \tag{3.4}$$

Where I_r is the inertia of the motor and wheels, where the wheels inertia is transformed to the motors point of view. τ_m is the torque generated by the motor while τ_{load} is F_x transformed to the viewpoint of the motor. B is the viscous friction of ball bearings in the motor. This entails two 6001-2Z ball bearings in the motor and further 8 in the wheels running at G^{-1} of the motors rotational speed.
The custom motor is only rewound so the inertia of the motor is unchanged around 0.0027 kgm^2 as found in the motors data sheet [5]. The new wheel assembly for Cimbrer III are designed by me in Solidworks. Thus by specifying material properties similar to Hokotol aluminium alloy, which we are machining them out of, the principle moment of inertia can be read using the weight tool. I have also modelled the tires in Solidworks with a single point mass and distribution of mass close to the real tires. Like with the wheel assembly the principal moment of inertia of the tires was read using the weight tool. The total principle moment of inertia per wheel is around 0.2041 kgm^2, when summing the two principal moment of inertias. This means the motor sees $0.2041 \cdot 4 \cdot (G^2)^{-1}\ kgm^2 + 0.0027\ kgm^2 =$ from all four wheels and the motor itself. The inertia seen by the motor caused by the mass of the car is $m(r_{wheel}/G)^2$, where the mass of the car was found during an official

weigh-in of the car at Eco-marathon 2019. The gearing is a system variable that can be chosen on an optimization basis. At the time of writing the gearing is 7, so this is used for the rest of the study.
Inserting (3.2) into (3.4) and substituting the linear velocities with the equivalent motor rotational speeds as shown in Eq. (3.5) the load seen from the motors point of view is expressed as shown in Eq. (3.6). The advantage of Eq. (3.6) is the simplicity. If the speed is known, then the motor torque can be found or the other way around. Additionally the Equation can be decomposed into the different torques; acceleration, rolling resistance, aerodynamic drag and elevation. By multiplying each of the decomposed torques with the rotational speed, the powers can be found. By looking at the individual power flows, the reversible and irreversible powers can be identified. This results in an estimation of possible regenerative braking power and irreversible losses. The losses combined over a lap are what the fuel cell must deliver to the system, otherwise power balance is negative and the super capacitor will discharge.

$$v = \frac{\omega_m r_w}{G} \quad , \dot{v} = \frac{\dot{\omega_m} r_w}{G} \tag{3.5}$$

$$\left(I_r + m\frac{r_w^2}{G^2}\right)\dot{\omega_m} = \tau_m - \left(\frac{1}{2}C_D A_v \rho \left(\frac{\omega_m r_w}{G}\right)^2 + mgC_{RR} + mgsin(\beta)\right)\frac{r_w}{G} - B\omega_m \tag{3.6}$$

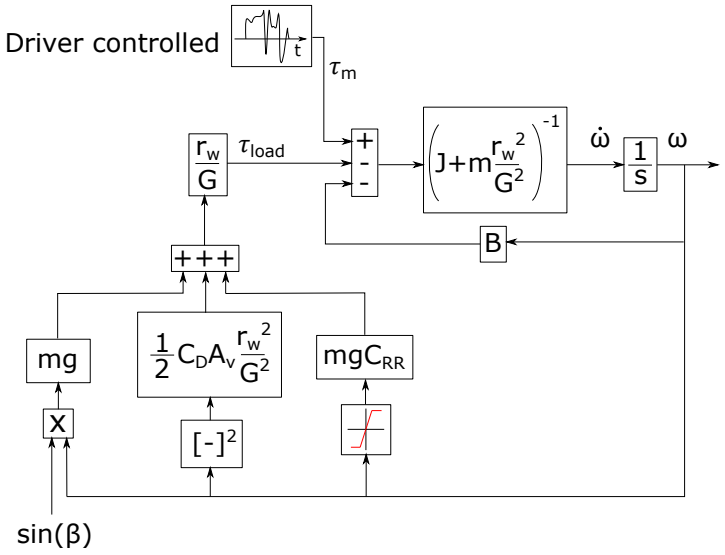


Figure 3.3: Load diagram with current guidance for driver.

3.2 Motor torque simulation

In Fig. 3.3 Eq. (3.6) is put on a diagram form. The driver is controlling the torque of the motor directly using FOC (Field oriented control).
Fig. 3.3 is used to simulate the different torques by specifying the acceleration. Acceleration data is found by differentiating the speed data obtained from the best attempt of Eco-marathon 2019, shown in Fig. 3.4(a). The velocity is GPS data acquired from Shell, which is noisy so a smoothing spline is applied. Differentiating the smoothed velocity then yields the acceleration data shown in Fig. 3.4(b). The repeating pattern of the data is caused by the start and stop rules at the competition.
The acceleration from Fig. 3.4(b) is transformed to the motors point of view and inserting it into the simulation diagram shown in Fig. 3.3. In Eq. (3.7) the motor torque is isolated as a function of acceleration and simulated torques. Fig. 3.5 shows the torque the motor must deliver to achieve the same lap times as the best attempt at a gearing of G=7. 2-3 Nm of positive torque is very doable for the motor used, but 6 Nm of negative torque is over the maximum torque of the motor. This large negative torque is naturally physical brakes, but with super capacitor implementation that will be regenerative braking instead. In the next chapter the motor will be modelled and control for it designed. The simulation done here will be continued, including a decomposition of losses and reversible power.

$$I_r \dot{\omega_m} + \tau_{load} = \tau_m \tag{3.7}$$

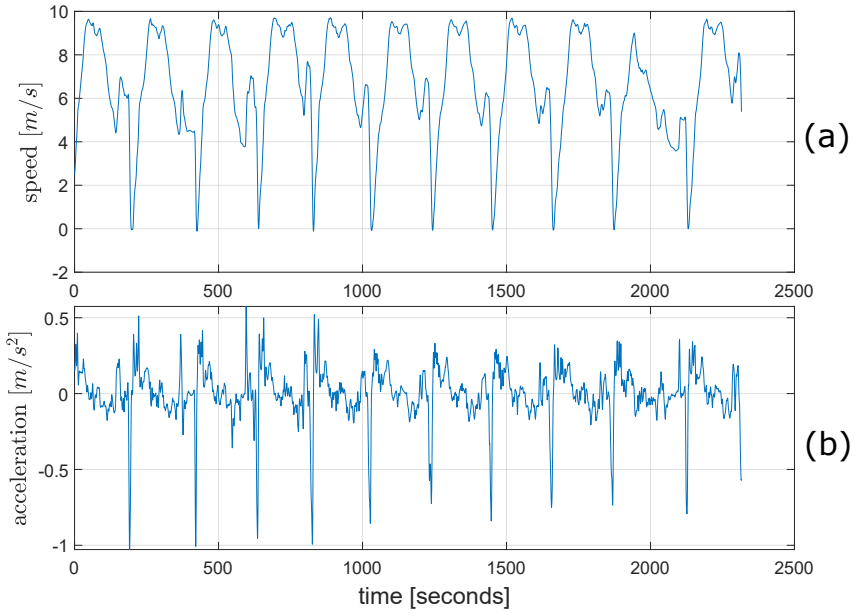


Figure 3.4: (a) Spline smoothed GPS speed data. (b) Acceleration differentiated from speed data. Attempt 2 Eco-marathon 2019 (Best attempt).

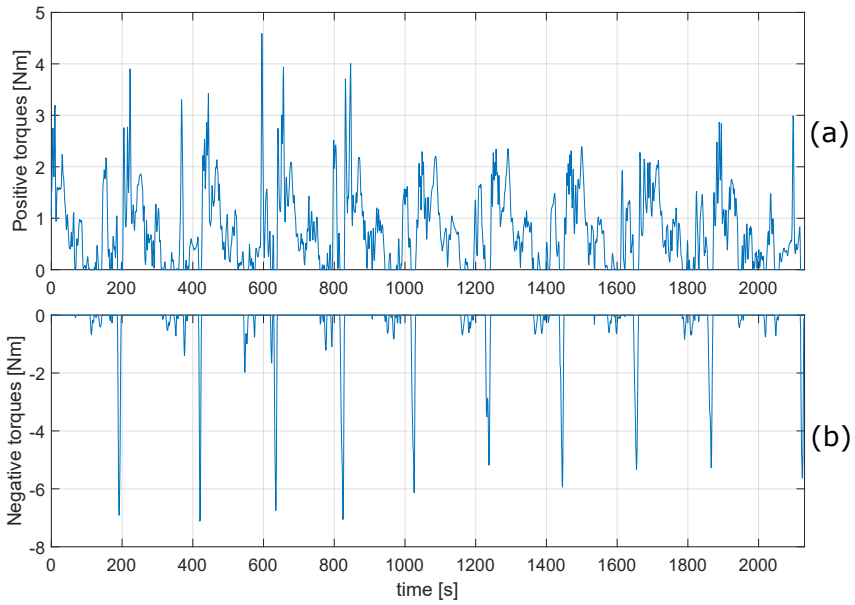


Figure 3.5: Torque simulation based on acceleration data showed in Fig. 3.4(b)

Chapter 4

Motor & inverter analysis

Contents

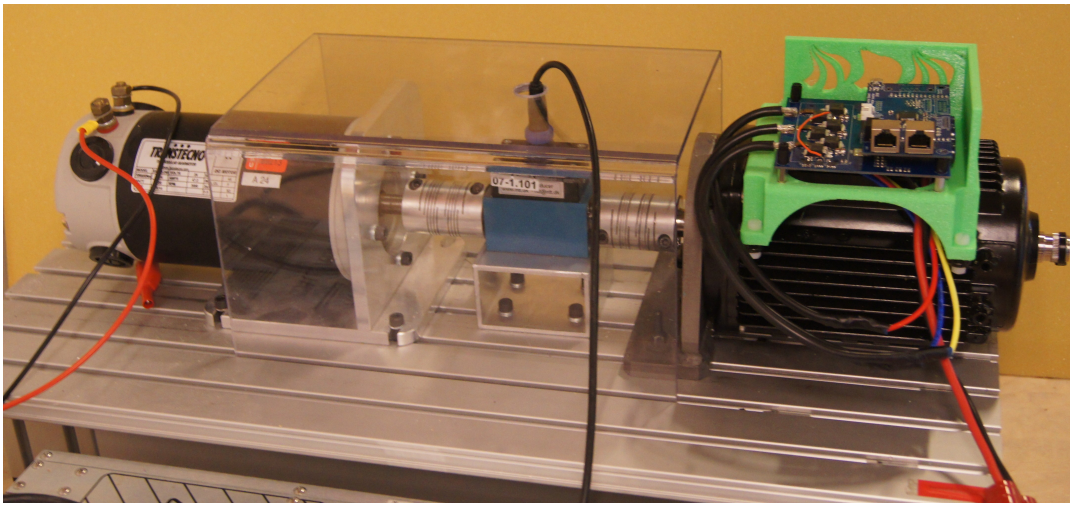


Figure 4.1: Right; Custom Grundfos PMSM MGE motor with VESC inverter. Middle: DR3000 Torque transducer. Left: Brushed DC motor with electronic power load.

Having established a mechanical model in the previous Chapter a model for the motor will be established in this Chapter. The Chapter is separated into a classic FOC model and control design. This is followed by a motor and mechanical simulation, where reversible and irreversible power flows are investigated. Then a fuel

efficiency simulation is run. This is to get an idea of the potential energy savings of having the motor draw peak power from the super capacitor module, rather than directly from the fuel cell. Finally an estimation for the DC-bus current draw is made, with the intention of using it for feedforward disturbance rejection when designing power control in chapter 7.

4.1 Motor model

The motor used in the vehicle is a customised MGE71A PMSM rated at 550W. Originally the motor was rated for 3 x 400V supply. The customization aim was to change the motor voltage rating to be close to 3 x 30V, making the motor high-current, low voltage. To do this the wiring is made thicker from 73x0.5mm to 52x1.18mm stranded wires and the phases are wired in parallel. Rewiring the phases to parallel decreases the voltage rating by 1/3 bringing it down to 3 x 133V. The much thicker wires means less turns and thus further decreases the voltage rating. For the inverter a so-called VESC inverter is used. The VESC is open-sourced, meaning anyone can download the board schematics and software, then order the PCB and components, solder them and install the software. [6] The advantage of choosing an inverter like the VESC is that it has a large online community, and it is tested and verified. For the Ecoracer using the VESC means an in-depth and debugged software platform for motors where the hardware can be changed to a certain degree in order to optimise performance. For example, the MOSFETs on the inverter is changed to IRFS7530 from IPB044N15N5. The main difference being the on-resistance decreasing from 4.4 mΩ to 1.4mΩ. The decrease in on-resistance comes at the cost of voltage rating from 150 V to 60 V, but the rating of the motors are supposed to be 30 V so there is some safety margin. To model the motor, a synchronous dq0-reference frame is used. A drawing of the electrical stator and rotor reference frames can be seen in Fig. 4.2. The three stator phases $a+, a-$, $b+b-$ and $c+c-$ generate a magnetic flux along a_s, b_s and c_s that will link with the magnetic flux of the rotor. The rotor magnetic flux is aligned with the d-axis and is rotating synchronously with the flux vector generated by the stator currents. The q-axis is leading the d-axis by $90°C$. As a result of this dq0 definition the inductances seen on the d and q axes are constant instead of position dependant, which greatly simplifies the control scheme of the motor.
In the dq0-reference frame the essential voltage equations can be set up as shown in Eq. (4.1) and (4.2). [7] In appendix A blocked rotor and open-circuit terminal tests are conducted to determine $L_d, L_q, \lambda_{mpm}, R_s$.

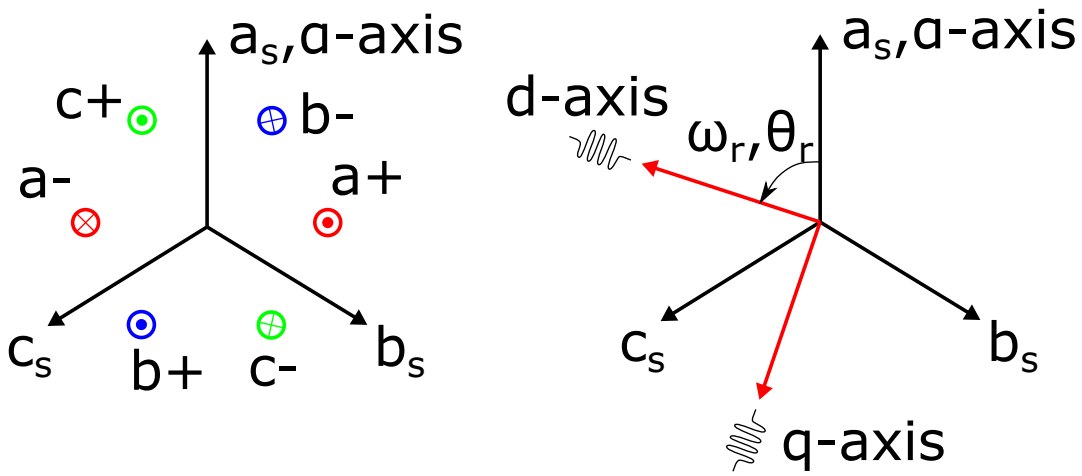


Figure 4.2: Left: Wired stator phases representation in relation to stationary flux axes. Right: dq-reference frame in relation to stationary flux axes.

$$u_q = R_s i_q + \frac{d}{dt}\lambda_q - \omega_r \lambda_d \tag{4.1}$$

$$u_d = R_s i_d + \frac{d}{dt}\lambda_d + \omega_r \lambda_q \tag{4.2}$$

$$\lambda_q = L_q i_q \tag{4.3}$$

$$\lambda_d = L_d i_d + \lambda_{mpm} \tag{4.4}$$

The torque generated by the motor can be described by Eq. (4.5). Substituting in λ_d and λ_q the torque equation changes to (4.6). In order for Eq. (4.7) to be valid either the motor has to be non-salient ($L_q = L_q$) or $i_d = 0$, the latter condition is used in this study since the motor is salient ($L_q \neq L_d$). The condition requires that the current controller for i_d has no steady state error. This is something that will be looked at next. [8]

$$T_e = \frac{3}{2} N_{pp} \left(\lambda_d i_q - \lambda_q i_d\right) \tag{4.5}$$

$$T_e = \frac{3}{2} N_{pp} \left(\lambda_{mpm} i_q + (L_d - L_q) i_d i_q\right) \tag{4.6}$$

$$T_e = \frac{3}{2} N_{pp} \left(\lambda_{mpm} i_q\right) \tag{4.7}$$

4.2 Field oriented current/torque controller

In order to design control for i_q and i_d by classical control methods, it is necessary to decouple the voltage equations (4.1) through (4.4). This is accomplished as

shown in figures 4.3 and 4.4. [7]

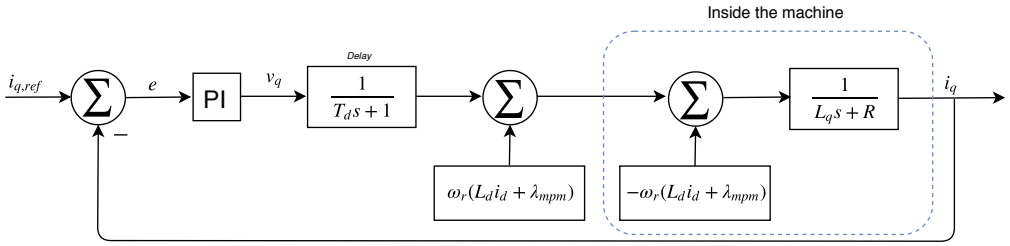


Figure 4.3: Decoupled d-current control of PMSM. Taken from [7]

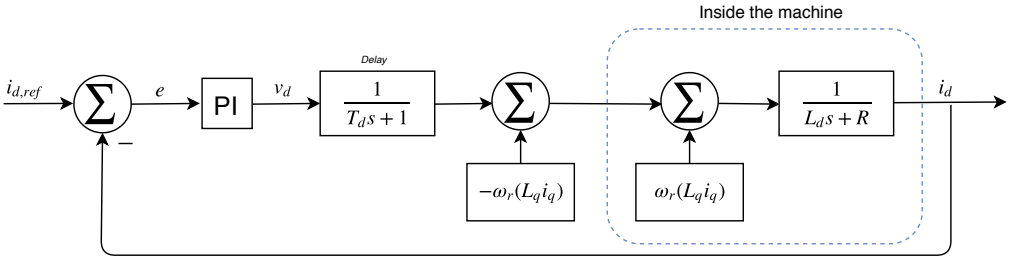


Figure 4.4: Decoupled q-current control of PMSM. Taken from [7]

The delay block containing T_d describes the time for the inverter to apply a field voltage from receiving a voltage command. T_d is approximately 1.5 times of the switching time of the inverter. [9] In this study the motor current control bandwidth goal is approximately 1000 rad/s. A delay of 1.5 times the switching frequency of 20 kHz provides insignificant phase delay to this controller bandwidth, thus the delay is disregarded. With the cancellation of the coupling between d -and q current axes and disregarding the delay term the transfer function for each axes become as shown in equations (4.8) and (4.9).

$$G_{i_d}(s) = \frac{i_d(s)}{u_d(s)} = \frac{1}{L_d s + R} \tag{4.8}$$

$$G_{i_q}(s) = \frac{i_q(s)}{u_q(s)} = \frac{1}{L_q s + R} \tag{4.9}$$

Unfortunately the VESC software only supports a single configurable PI-controller for both current axes. This limitation extends to the VESC assuming a single system inductance. This is a problem because perfect control can not be achieved on both axes with a single PI-controller with a salient machine. It is also a problem in terms of the decoupling not being ideal and thus there being coupling effects.

Nevertheless it will be investigated if the inductance used for decoupling is the mean of L_d and L_q. The effect will be investigated by designing a controller for the average inductance or system inductance L_s and then simulating and checking the response.
A PI-controller is shown in Eq. (4.10). This controller is chosen to cancel out the slow pole of i_q and increase the system type.

$$C_{pi,iq}(s) = K_p \frac{s + K_i/K_p}{s} \tag{4.10}$$

The open-loop transfer function is defined in (4.11) and the closed-loop transfer function, assuming perfect pole cancellation, is defined in Eq. (4.12).

$$L_{i_q}(s) = G_{i_q}(s)C_{pi,iq}(s) = 1/R \frac{R/L_q}{s + R/L_q} \cdot K_p \frac{s + K_i/K_p}{s} \tag{4.11}$$

$$T_{i_q}(s) = \frac{K_p/L_q}{s + K_p/L_q} \tag{4.12}$$

From Eq. (4.12) the bandwidth of the resultant first-order system is observed to be K_p/L_q, so with a desired bandwidth ω_{i_q} a gain K_p can be found with Eq. (4.13). Subsequently the integral gain can be found with Eq. (4.14).

$$K_p = \omega_{i_q} L_q \tag{4.13}$$

$$K_i = K_p \frac{R}{L_q} \tag{4.14}$$

A pole cancellation is only as good as the model and even if the model is perfect the constants will typically drift as the temperature increases in operation. Assuming the q-axis pole cancellation is perfect and there is no parameter drift there is still the matter of the d-axis. The fact that there is only one PI-controller and it is used to cancel the i_q pole means the i_d pole is not cancelled, instead the open-loop transfer function for i_d becomes what is shown in Eq. (4.15).

$$L_{i_d}(s) = \frac{K_p}{L_d s} \frac{(s + R/L_q)}{(s + R/L_d)} \tag{4.15}$$

$$T_{i_d}(s) = \frac{\frac{K_p}{L_d s}(s + R/L_q)}{(s + R/L_d) + \frac{K_p}{L_d s}(s + R/L_q)} \tag{4.16}$$

Not only is the d-axis system pole not cancelled, but a slow closed loop pole is instead a result of the mismatched pole cancellation. A simulation of implementing the same PI-controller on both i_d and i_q tuned for the q-axis with imperfect

decoupling is shown in Fig. 4.5. The q-axis current bandwidth is set to 1000 rad/s and $i_{q,cmd}$ is stepped by 5 A at a time, this is shown in Fig. 4.5(b). The d-axis $i_{d,cmd}$ is set to zero at all times. i_d can be seen in Fig. 4.5(a). To start, in Fig. 4.5(a). The response to the disturbances is indeed very slow as a result of the mismatched pole cancellation tuned for the q-axis. But even if the response is slow, the value is very low and it does decrease in steady state, so this is evaluated to be good enough. The q-axis response is too fast to see in Fig. 4.5(b) therefore in Fig. 4.6 there is a zoomed view of the step from 0 to 5 A. In Fig. 4.6 a first order response can be seen with a response time of 1 ms, which is equivalent to a bandwidth of 1000 rad/s. From this it can be concluded that the motor current control design is adequate to proceed in the study.

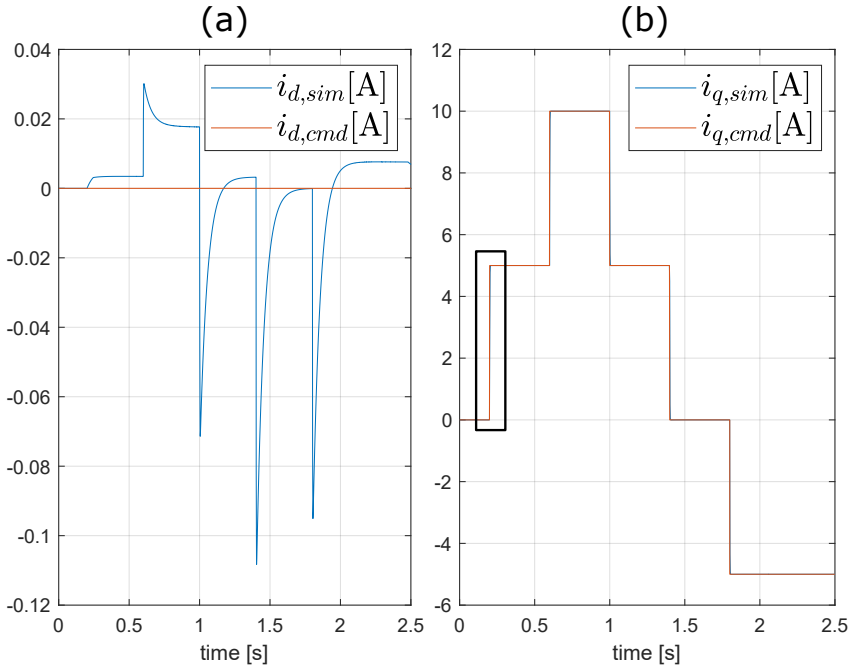


Figure 4.5: Current response simulation, with PI-controller tuned for i_d. $i_{d,cmn} = 0$ and $i_{q,cmd}$ is stepped.

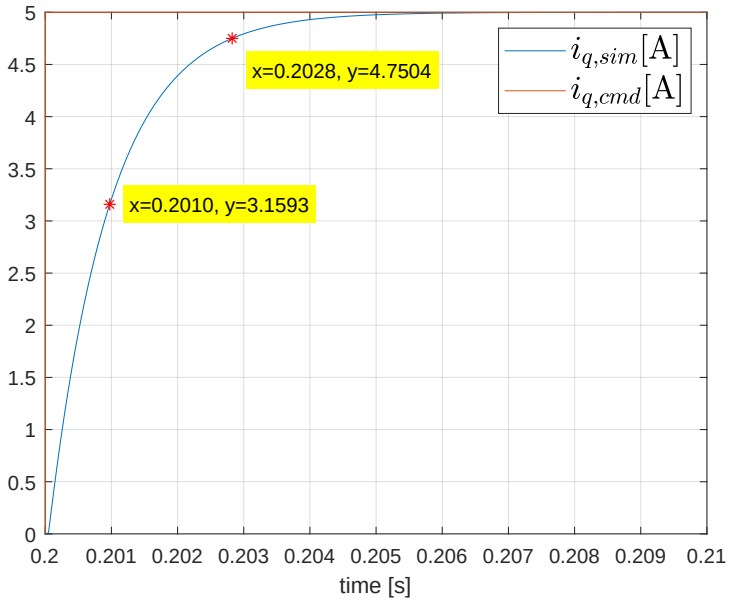


Figure 4.6: Command current to output q-axis current. Points at response time (63% of step) and settling time (95% of step)

4.3 Motor and mechanical simulation

With motor torque controllers designed it is possible to simulate a probable lap of the track. The aim of this simulation is to emulate one of the best attempts from Eco-marathon 2019. Instead of injecting data into the mechanical model, a speed controller is designed to emulate the drivers current commands. In other words, this simulation is about how well the FOC would perform under a realistic load. Also by doing it this way it is possible to saturate the control input to the motor and see the effect of that.
The transfer function from q-axis current to rotational speed of the motor is given in Eq. (4.17).

$$\frac{\omega_m(s)}{i_q(s)} = G_{iq,\omega}(s) = \frac{3/2 N_{pp}\lambda_{mpm}}{I_r s + B_m} \tag{4.17}$$

Because the speed reference is known beforehand it is possible to feed forward this information to obtain better tracking. The feed forward gain is the inverse of the DC-gain of the plant, calculated as shown in Eq. (4.18).

$$G_{iq,\omega}(0)^{-1} = \frac{B_m}{3/2 N_{pp}\lambda_{mpm}} \tag{4.18}$$

The Matlab SISO control design tool Sisotool is used to find the a suitable response. The criteria is a response within 0.2 seconds, similar to the reaction time of a human

and no steady state error. This controller is simply an emulation of a driver since in the final application the driver will be controlling the current by intuition, like with the throttle of a combustion car, so the accuracy or performance is not important. The result of simulating with the speed controller, tracking the telemetry data can be seen in Fig. 4.7. It can be seen towards the end of the data that there is a tracking error. This is because there is a current limit of 50 A in this simulation, which translates to around 4 Nm of braking torque. To get proper tracking around 7 Nm is necessary, translating to around 90 A motor current, which is not viable.

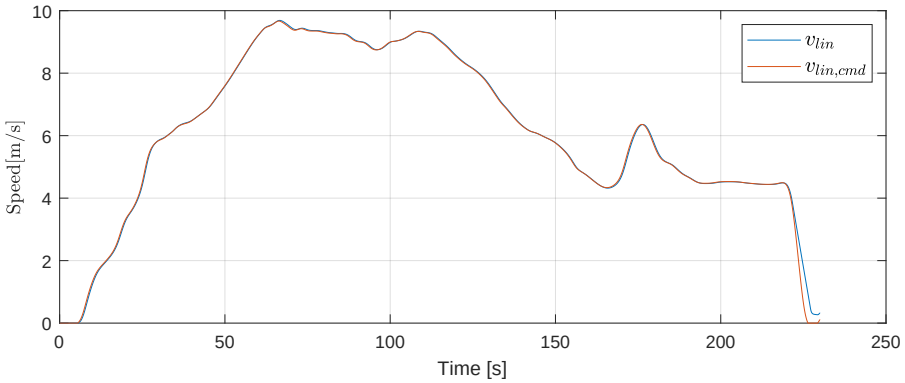


Figure 4.7: Vehicle load and motor simulation. Reference is data from a lap at Eco-marathon 2019. Impromptu designed speed controller to emulate a driver is shown in Eq. (4.17) with reference feed forward shown in Eq. (4.18).

By decomposition of the mechanical model it is possible to identify the reversible and irreversible powers of the system. Torques and powers are shown decomposed in Fig. 4.8. In Fig. 4.8(a) the motor power (P_m) and accelerating power (P_{acc}) are shown. P_m is the acceleration power added to the accumulated losses shown in Fig. 4.8(b). The only reversible power is that contained in P_{acc}, or rather stored in the inertia of the vehicle. Taking a look at Fig. 4.8(b) again it can be seen that at speeds below 40 km/t the power loss P_{RR} from rolling resistance is dominant. The power loss from aerodynamics P_{aero} on the other hand increases with the cubic root of speed and would dominate if the speed was faster. As a side note, the aerodynamic loss is under the assumption of no wind. Say for example that the vehicle is travelling with a speed of 10 m/s and there is a 10 m/s headwind. Then the relative speed between vehicle and wind is doubled. The aerodynamic torque resistance rises with the square power of relative speed, so it the power loss would quadruple. The viscous friction is less than 10W as expected with quality bearings. The torques shown in the Fig. 4.8(c) and Fig. 4.8(d) tell much of the same story as the first two graphs. For example that the motor has to supply a minimum of 0.4 Nm at standstill to overcome the rolling resistance. Likely there is also a significant static friction the vehicle has to overcome at standstill, yet this is not

modelled. All of the powers and torques will change if the gearing is changed and so these graphs are not a final indicator of the mechanical powers. An optimization will be necessary to determine which gearing is optimal.

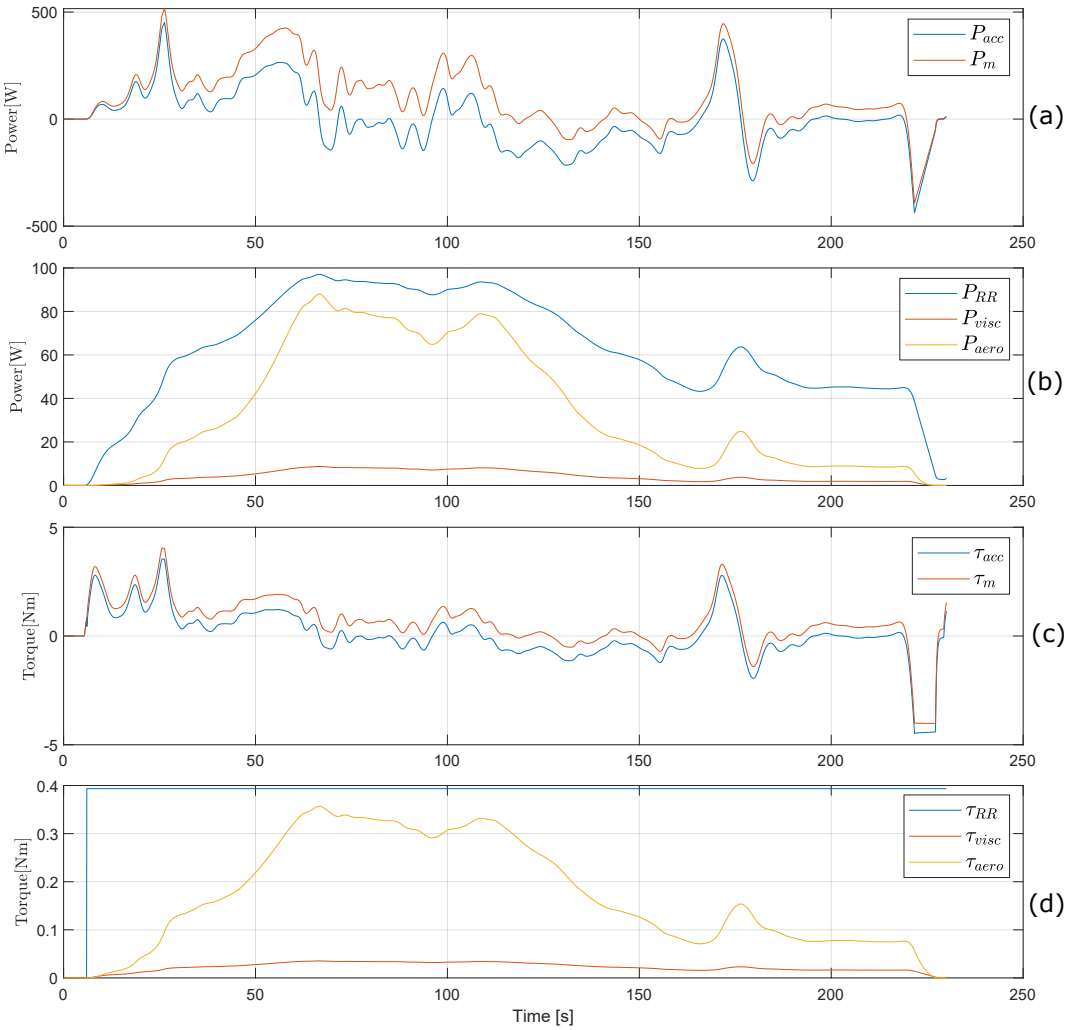


Figure 4.8: (a) Acceleration and motor power. (b) Power losses. (c) Acceleration and motor torques. (d) Torque losses.

Assuming that there are no converter losses in the system. Then taking the integral of P_m in Fig. 4.8(a) or the accumulated losses in Fig. 4.8(b) would be the average power the fuel cell has to deliver to balance the system. This means that the super capacitor is delivering power to the motor along with the fuel cell, when above the mean power and receiving power from the fuel cell when below. When using regenerative braking the motor will also supply power to the super capacitor. This simple concept is shown in Fig. 4.9, where the fuelcell is supplying a constant

power of around 100 W and the super capacitor is either receiving or supplying power to the DC-bus, depending on what the motor is doing.

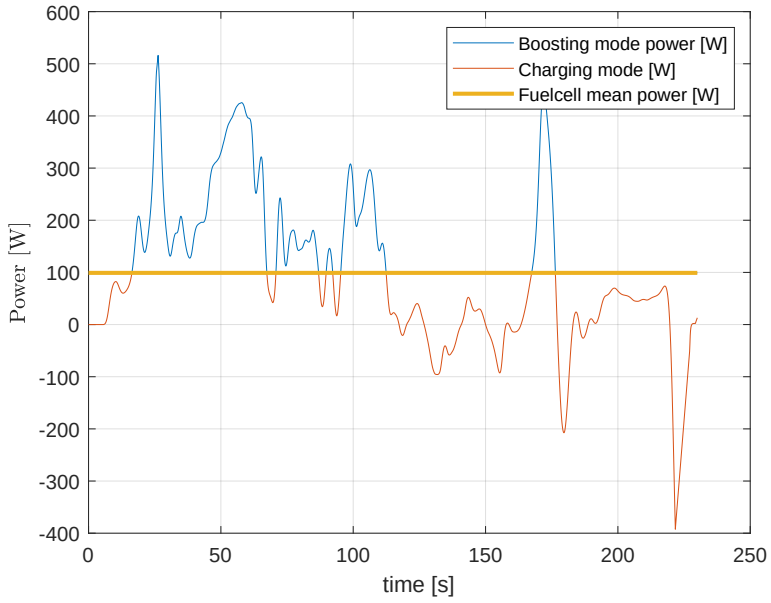


Figure 4.9: Motor power draw; super capacitor bank in boosting or charging mode dependant on fuelcell set mean power.

4.4 Fuel efficiency

In Fig. 4.9 it was shown that if the fuel cell supplies a mean power of 100 W to the system and regenerative braking was enabled then the power balance after an entire lap should break even. If the power drawn from the fuel cell is a constant 100 W, then the voltage will be a constant 31 V which gives the fuel cell an efficiency of $(31/42)/1.481 = 0.4984$.This means that the energy consumed over a lap of 230 seconds can be calculated as shown in Eq. (4.19).

$$E_{lap,sc} = \int_0^{T_{lap}} 100\,\mathrm{W}/0.4984 dt = 200.64\,\mathrm{W} \cdot 230\,\mathrm{s} = 46147\,\mathrm{J} \tag{4.19}$$

The alternative scenario is that the motor power P_m is drawn directly from the fuel cell. These two scenarios are shown in Fig. 4.10(a). However, because the fuel cell has uni-direction power flow only the positive P_m are used. When the motor power is negative, it is assumed that mechanical brakes are engaged instead of regenerative braking. The efficiency is found by simulating the motor and fuel cell together, with the fuel cell model being described in chapter 2. By dividing the instantaneous power with the instantaneous efficiency the equivalent fuel power consumption can be found. The energy consumed without a super capacitor is found by integrating the equivalent fuel power consumption from 0 to 230 s. This calculation is shown in Eq. (4.20).

$$E_{lap,nosc} = \int_0^{T_{lap}} P_{FC}(t)/\eta_{FC}(t) dt = 60232\,\mathrm{J} \tag{4.20}$$

This means that 15000 J or 30% of the total energy consumption is saved by implementing power control, just looking at the fuel cell efficiency. Naturally the converters are not ideal and moving power back and forth the system will induce considerable losses. But with converter efficiencies being in the high nineties percent, it is likely that power control is still worth it. This section has shown the potential gains of power control.

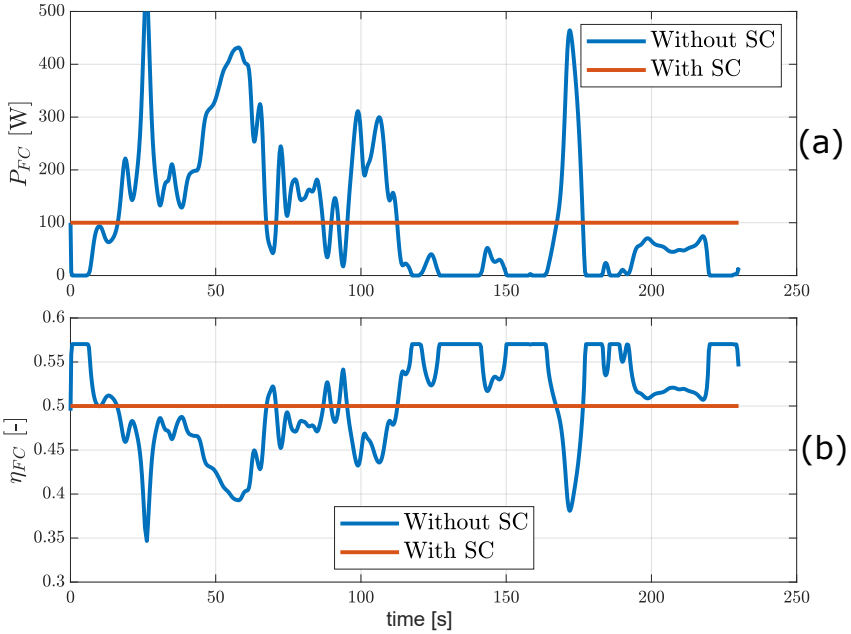


Figure 4.10: Conceptual fuel cell efficiency simulation. (a) Power draw from fuel cell with and without super capacitor module. (b) Instantaneous fuel cell efficiency as a function of fuel cell power draw, with and without super capacitor module.

4.5 Motor DC-bus current draw

Since the motor is considered a disturbance to the DC-bus, it is useful to derive an estimation for this disturbance. The estimation will be used for feedforward disturbance rejection in the power control solution to achieve better DC-bus voltage control performance.
Assuming that the inverter is ideal, the power 'in' is equal to the power 'out'. On the DC-bus side, the current is DC so the power is simply the voltage multiplied by the current. The power on the motor side will consist of a reactive and active power summed up and then multiplied by 3/2 to make it power invariant. The power balance is shown in Eq. (4.21) where i_m is the instantaneous current drawn by the inverter. By dividing with the DC-bus voltage (u_{dc}) on both sides an expression for the instantaneous current is found in Eq. (4.22). [8]

$$P_{dc}(t) = P_{ac}(t) \Rightarrow u_{dc}(t)i_m(t) = \frac{3}{2}(i_q(t)u_q(t) + i_d(t)u_d(t)) \tag{4.21}$$

$$i_m(t) = \frac{3}{2}\frac{i_q(t)u_q(t) + i_d(t)u_d(t)}{u_{dc}(t)} \tag{4.22}$$

Eq. (4.22) will be used in the simulation to simulate the motors current draw from the DC-bus. In the power control solution it will be more advantageous to estimate

the motor current drawn by the inverter with as few variables as possible. The reason being it is not easy to measure u_d, u_q, i_q or i_d. To get a simple estimation first the dq-reference voltage equations are substituted into Eq. (4.22), this is shown in Eq. (4.23). Then it is assumed that i_d is controlled to be zero or at least insignificant compared to i_q, this reduces the expression to what is shown in Eq. (4.24). Finally a Laplace transform is performed under the assumption that all initial states are zero, this is shown in Eq. (4.25).

$$\begin{aligned} i_m(t) = \frac{3}{2u_{dc}}[&i_q(i_q R_s + \frac{d}{dt}L_q i_q - \omega_r L_d i_d - \omega_r \lambda_{mpm}) \\ &+ i_d(i_d R_s + \frac{d}{dt}i_d L_d + \frac{d}{dt}\lambda_{mpm} + \omega_r L_q i_q)] \end{aligned} \tag{4.23}$$

$$\xrightarrow{i_d=0} i_m(t) = \frac{3}{2u_{dc}}(i_q^2 R_s + \frac{d}{dt}i_q^2 L_q - i_q \omega_r \lambda_{mpm}) \tag{4.24}$$

$$\xrightarrow{\frac{d}{dt}=s} i_m(s) = \frac{3}{2u_{dc}}(i_q^2 R_s + s i_q^2 L_q - i_q \omega_r \lambda_{mpm}) \tag{4.25}$$

It is possible to write i_q as a function of the reference $i_{q,ref}$, by using the closed loop transfer function found in Eq. (4.12). This closed loop first order response can also be written as shown in Eq. (4.26). The reason why this is advantageous is because then the disturbance estimation does not depend on fast measurements. The driver will send a command to the motor, this command will pass through the super capacitor module where it will be used to estimate the coming disturbance.

$$i_q(s) = \frac{1}{\tau_{i_q} s + 1} i_{q,ref}(s) \tag{4.26}$$

Substituting Eq. (4.26) into Eq. (4.25) yields Eq. (4.27), which is an estimation of the disturbance based on the speed, the current command and DC-bus voltage, all of which are measured.

$$i_m(s) = \frac{3}{2u_{dc}}\left((\frac{1}{\tau_{i_q} s + 1} i_{q,ref}(s))^2 (R_s + sL_q) - \frac{1}{\tau_{i_q} s + 1} i_{q,ref}(s) \omega_r \lambda_{mpm}\right) \tag{4.27}$$

$$i_m(s) = \frac{3}{2u_{dc}}\left(\frac{R_s + sL_q}{(\tau_{i_q} s + 1)^2} i_{q,ref}^2(s) - \frac{\omega_r \lambda_{mpm}}{\tau_{i_q} s + 1} i_{q,ref}(s)\right) \tag{4.28}$$

The estimator is implemented in the simulation as shown in Fig. 4.11. In Fig. 4.12 the performance of the estimator is compared with a direct calculation using Eq. (4.22). The transient performance of the estimator is good, but there is a gain difference between the two values. This discrepancy is acceptable, because in real-life the estimation would not be perfect either. This just means that the DC-bus voltage controller must be robust enough to compensate for imperfect feedforward disturbance rejection.

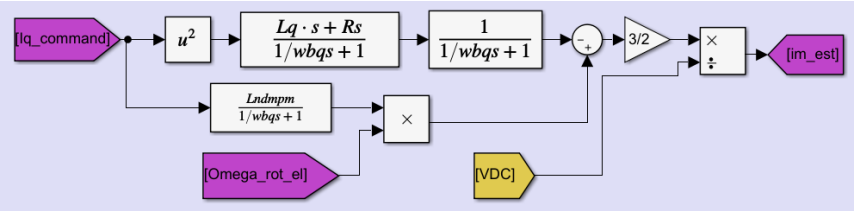


Figure 4.11: Eq. (4.28) implemented in simulation.

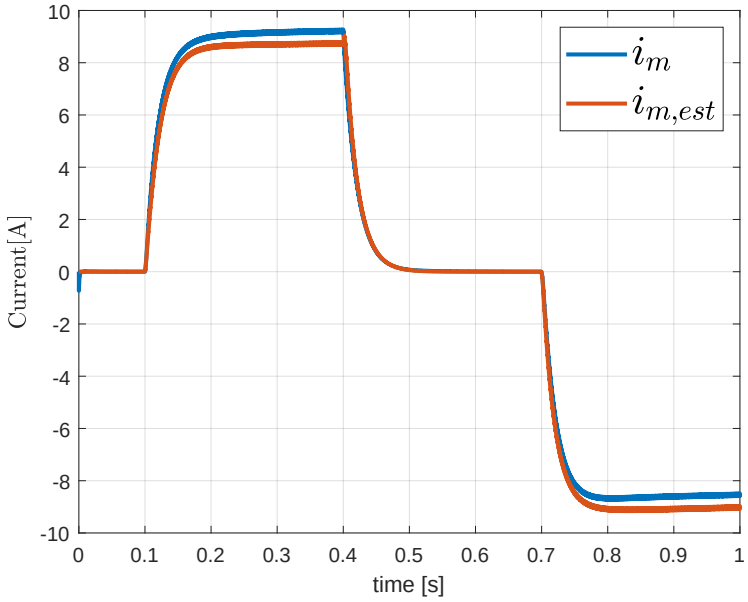


Figure 4.12: Simulation stepping i_q and estimating motor current draw from DC-bus. i_m is calculated using Eq. (4.22), $i_{m,ref}$ is calculated using Eq. (4.28) shown implemented in Fig. 4.11.

Chapter 5

Super capacitor bank

Contents

In this chapter the primary energy buffer, the super capacitor bank is analysed. The goal is to make a simple super capacitor bank model and dimension it in relation to the rest of the system. At the end of the chapter the state-of-charge (SOC) variation is simulated for the designed super capacitor bank during a lap.

5.1 Super capacitors bank design

An accurate model for a super capacitor bank is a lumped parameter model, which includes many parasitic effects. However a much simpler RC circuit is deemed to be an adequate model for this study, where inactive periods or very fast transients are not of interest. [10] The super capacitor cells used are supplied by Aowei. They are called UCR27V1500 which means it is rated at 2.7 V with a rated capacitance of 1500 F. The surge voltage rating is 2.9 V and the parameter tolerance is $\pm 10\%$. The equivalent series resistance (ESR) is 0.6 mΩ. The data sheet for the super capacitor cells is attached in appendix E.
In Fig. 5.1 a simplified model of a super capacitor cell put in series to form a super capacitor bank is shown. The capacitance is a function of the cell voltage and can be approximately described with Eq. (5.1). The capacitance dependency on the cell voltage is also illustrated in Fig. 5.2. [10]

$$C_{sc}(u_{sc,cell}) = C_0 + k_v u_{sc,cell} \tag{5.1}$$

If the voltage variation is assumed to be small then the capacitance voltage dependency becomes small. This is an assumption I make because the data sheet

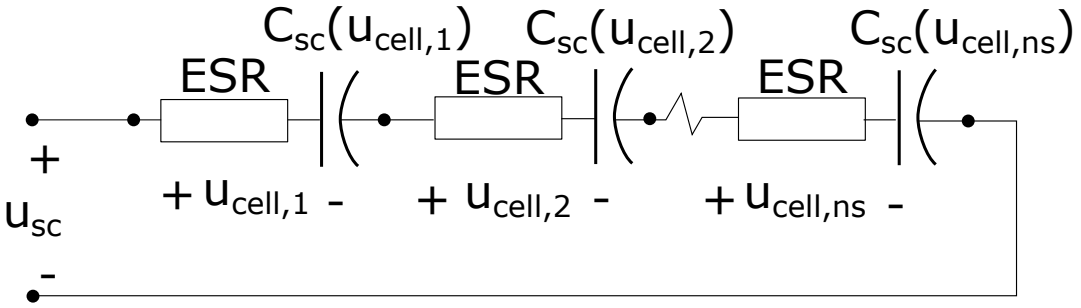


Figure 5.1: Simplified super capacitor model, from [10]. Put in series to form the super capacitor stack.

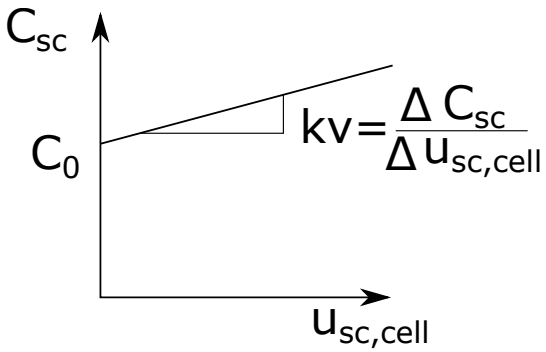


Figure 5.2: Capacitance dependency on cell voltage, from [10].

does not specify anything other than what was previously stated. By doing a few experiments it would be possible to model the capacitance more accurately.
Cells are put in series until the rated voltage is 27 V. So the number of cells in series is n_s=10. This amount is chosen for two reasons. First reason: The converter is of the buck type, which will be explained in the next chapter, which means the voltage of the super capacitor bank has to be below the fuel cell voltage. This means that the fuel cell can supply approximately 200 W before the voltage of the fuel cell drops below the voltage of a fully charged super capacitor bank. As a side note, the super capacitor bank should never be allowed to exceed 27 V. Second reason: Aowei supplied the team with exactly 20 super capacitor cells, why it makes sense to build two stacks, granting some redundancy. The capacitance could also be increased by placing 10 cells in parallel with the other 10 cells, but this results in a physically large and heavy super capacitor bank, which is unfavourable. The total bank resistance and capacitance can be calculated as shown in Eq. (5.2) and Eq. (5.3).

$$R_{sc} = \frac{n_s}{n_p} ESR \tag{5.2}$$

$$C_{sc} = \frac{n_p}{n_s} C_{rated} \tag{5.3}$$

$$\tag{5.4}$$

where n_s and n_p are super capacitors in series and parallel, respectively. With $n_s = 10$ the stack resistance is R_{sc}=6 mΩ and the capacitance is C_{sc} =150 F.

5.2 State-of-charge simulation

To get an idea of the sizing of the super capacitor energy-of-charge can be used. It can be approximated by Eq. (5.5). Say for example the initial voltage is $u_{sc}(t_1) = 25$ V and final voltage is $u_{sc}(t_2) = 20$ V then from these two voltages the bank holds 16875 J, equivalent of 281.2500 W for 60 seconds.

$$E_{max} = \frac{1}{2} C_{sc} (u_{sc}(t_1)^2 - u_{sc}(t_2)^2) \tag{5.5}$$

Another common measure of charge is State-Of-Charge (SOC) definition. The simplest is the absolute charge definition, written in Eq. (5.6). [11]

$$SOC_{qa} = \frac{u_{sc}(t)}{U_{sc,mx}} \tag{5.6}$$

Where $U_{sc,mx} = 27$ V is the maximum rating of the super capacitor. This means that $SOC_{qa} = 0$ is 0 V and $SOC_{qa} = 1$ is 27 V. The voltage should never drop even

close to zero during the race and instead the goal is to keep the SOC between 20 V and 27 V, corresponding to $SOC_{qa,min} = 0.74$, $SOC_{qa,max} = 1$. The super capacitor voltage can be estimated by integrating the capacitor current, shown in Eq. (5.7).

$$u_{sc}(t) = \frac{1}{C_{sc}} \int_0^t i_{sc}(t)dt \tag{5.7}$$

And the capacitor current can be expressed in terms of the fuel cell and motor current multiplied by a conversion factor corresponding to the voltage between the voltage of the DC-bus and super capacitor bank. (More on this in Chapter 7.)

$$u_{sc}(t) = \frac{1}{C_{sc}} \int_0^t \frac{u_{sc}(t)}{U_{dc}} (I_{fc} - i_m(t))dt \tag{5.8}$$

Assuming the fuel cell delivers a constant mean power, then the fuel cell current and DC-bus voltage will be constant. $I_{fc} = 3.24$ A and $U_{dc} = 31$ V. This leaves an analytical function for the super capacitor voltage as a function of the motor current. Taking the speed data for a lap at Eco-marathon 2019 and using the FOC motor model to simulate the motor current and injecting this data into Eq. (5.8) yields the SOC result shown in Fig. 5.3. The primary result of this analysis is that SOC_{qa} starts around 92.5% or 25 V and only drops to 86% or 23.2 V at the lowest point during the lap, when the fuel cell is supplying a constant power of 100 W. Because the SOC variation is not larger it is argued that SOC control is not needed other than basic safety features. Basic safety features being that if the SOC exceeds the minimum or maximum voltage levels, then the SCB can not charge or discharge according to the situation.

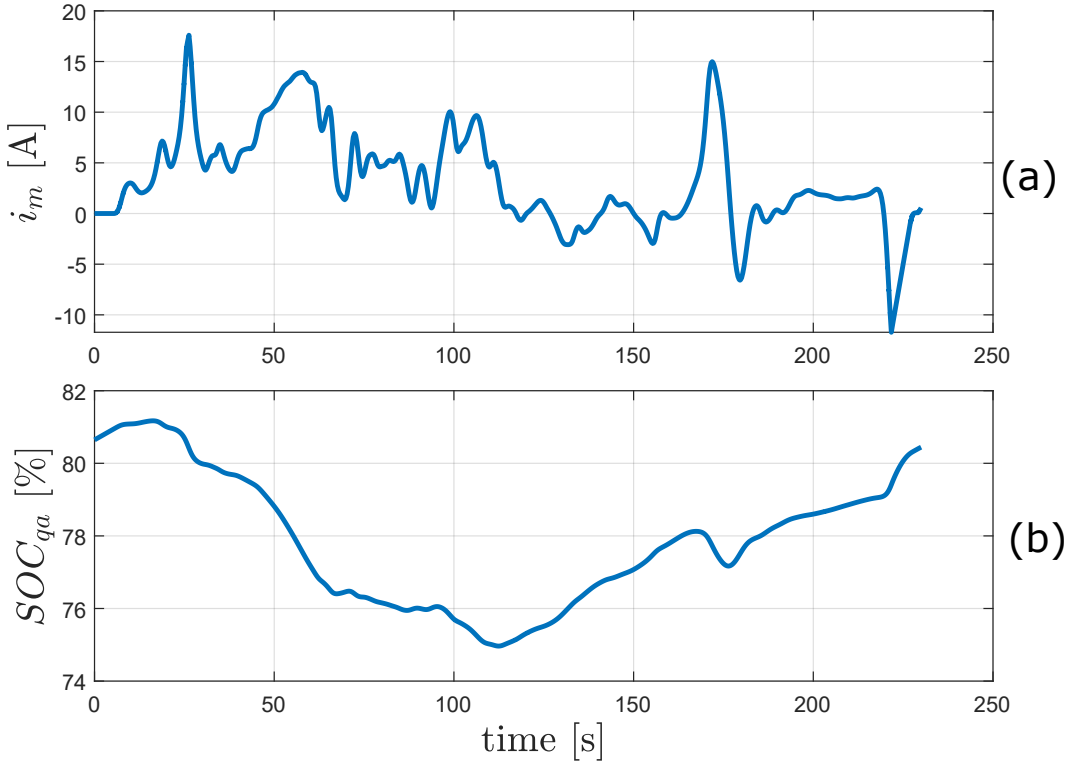


Figure 5.3: (a) Simulated motor current following speed data from Eco-marathon 2019. (b) Calculated SOC over a lap using Eq. (5.8)

Chapter 6

Bidirectional DC/DC converter analysis/design

Contents

The goal of this chapter is to model a suitable converter and design a current controller that can be used to control the power flow of the DC-bus. The first part of the chapter is about choosing a converter topology. This choice is based on a literature study and requirement for a converter in this project. The second part of this chapter is about constructing a non-linear simulation that can be used throughout the rest of the chapter to simulate the converters operation. After having established the topology and simulation, a state space model is derived from which a describing transfer function is extracted. The transfer function is then used to design a LTI SISO controller for current. After validating the LTI controller it is discretized to emulate the effect of a sampled data-hold system, which the real system will be. Finally effects like the quantization and current ripples are investigated.

6.1 Design of DC/DC converter

The choice of converter initially fell on the bidirectional DC/DC topology as shown in Fig. 6.1. This converter is a four quadrant converter, meaning it is current bidirectional both in voltage buck and boost mode. [12] The choice fell on this topology because many sources have reported large efficiency benefits with Zero voltage switching (ZVS). This is accomplished by shaping the inductor current which can be done by phase-shifting the buck and boost-leg switches. Methods for obtaining ZVS with this converter topology has been amply described in [13], [14], [15] and [16]. In these articles the efficiency when using phase-shift control is as high as 93-97% for 300W rated converter in [13] and 96-98% for 10kW in [14]. As of yet it has not been possible to configure phase-shift of the PWM in the software. The board layout is preserved with a buck and boost-leg, but the boost-leg is shorted effectively resulting in a bidirectional buck converter. In future iterations of this board it is the plan that the four quadrant topology is chosen and the prospects of ZVS is explored for higher efficiency and versatility.
Many choices were made in the design process of the converter like the board layout and choice of components. Some of the most important design choices are the choice of switches, gate drivers, microprocessor and inductor. With a collaborative project like this, a few people have been involved in the design iteration, so I do not take credit.
For the gate driver a synchronous gate driver called LM5104 was chosen because it is able to drive the chosen MOSFETs while not being over-dimensioned. The chosen MOSFETs are IPB010N06N which were chosen because they have low on-resistance and a voltage rating of 60 V. More about the switches and gate drivers are described in appendix C. Essentially the primary goal of proper gate drive design is to open and close the MOSFETs as fast as possible while avoiding shorting them.
The microprocessor chosen is of the SAMC21 32-bit architecture with a CPU clock speed of 24 MHz. This is a microprocessor the team is familiar with, additionally it has integrated CANbus and is in the low power range of the ARM series. All code is done in Atmel studio with a middleware add-on called FreeRTOS. FreeRTOS is a software add-on that enables a timer interrupt based code execution structure. In simple terms, it makes it easy to write a time-critical deterministic control loop which is a prerequisition for a digital controller.
The inductor built for the project is a toroid iron core, wound with as much Litz wire we could find. Originally the wire used was a heavy gage copper wire, but the AC-resistance at 20 kHz was measured to be high. According to a model made in [17] the AC-resistance of Litz wire is lower than solid wire in the range 20 kHz to around 600 kHz, thus we changed to Litz wire. The plan was to iteratively optimize the inductor by maximising the inductance while minimising the resistance. This would decrease the inductor current ripples while also reducing the

resistive power loss. However, the lockdown stopped this optimization process and the inductor wound with Litz wire was the best of the two, so it is used in the coming analysis. The parameters were measured to be L=307 uH and R_L=79 mΩ. The output capacitor chosen has capacitance of 1000 μF with an equivalent series resistance of $R_c = 270\ m\Omega$. All relevant system parameters are listed in Tab. 6.1.

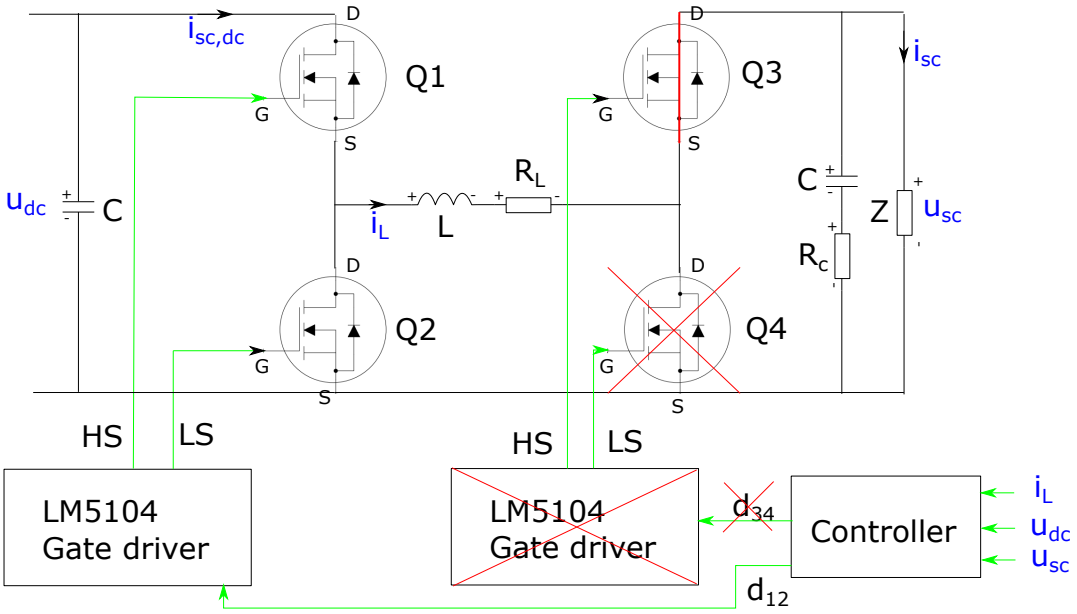


Figure 6.1: Four quadrant bidirectional DC/DC converter. The PCB shown in Fig. 6.2 is built using this topology. Crossed out components are de-soldered or shorted, effectively making the converter a bidirectional buck converter. Spots are still left of the PCB to solder components back on for future iterations. Inspiration from [13].

Parameter	Value[unit]	Note
T_{DT}	100 $[ns]$	Half-bridge dead-time
f_{sw}	20 $[kHz]$	Switching frequency
R_{sc}	6 $[m\Omega]$	Super capacitor bank total equivalent series resistance
C_{sc}	150 $[F]$	Super capacitor bank capacitance
R_c	270 $[m\Omega]$	≈ESR of 1000μF 100 V Alu-capacitor
C	1000 $[\mu F]$	Converter output capacitor
R_L	79 $[m\Omega]$	Measured inductor resistance @20 kHz
L	307$[\mu H]$	Measured inductor inductance @20 kHz

Table 6.1: Key parameters for super capacitor converter

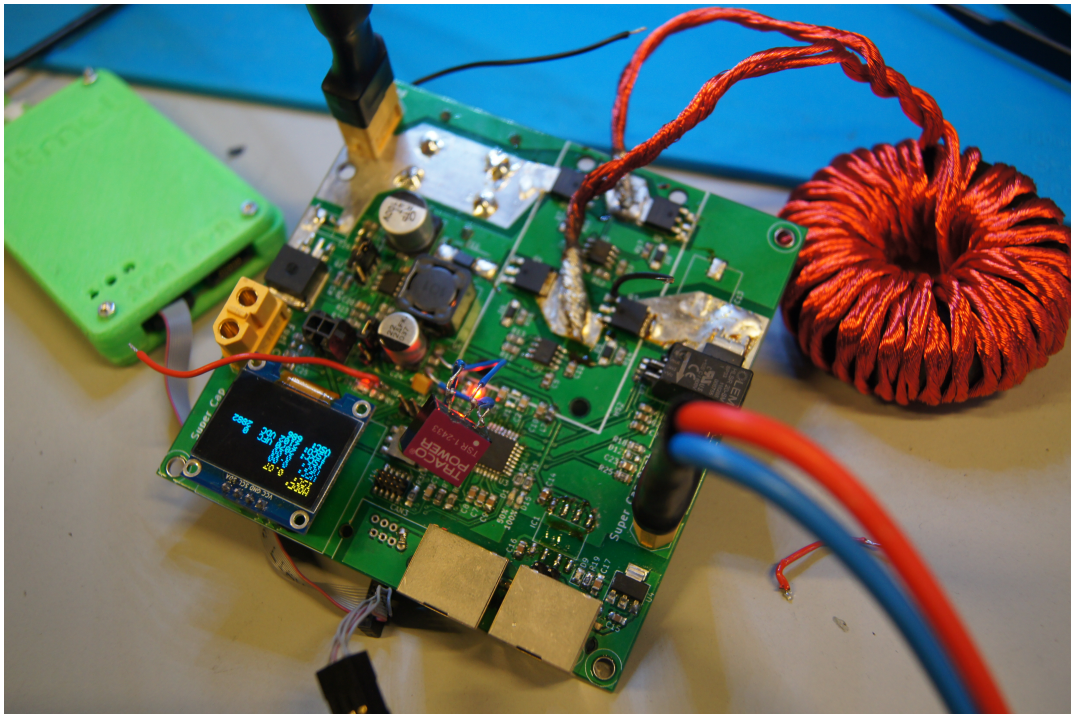


Figure 6.2: Ecoracer picture: Bidirectional DC/DC converter.

6.2 Non-linear buck converter simulation setup

A Plecs simulation is set up based on the schematic shown in Fig. 6.1, the Plecs schematic is shown in Fig. 6.3. In Tab. 6.1 the key parameters used for the converter simulation are listed.

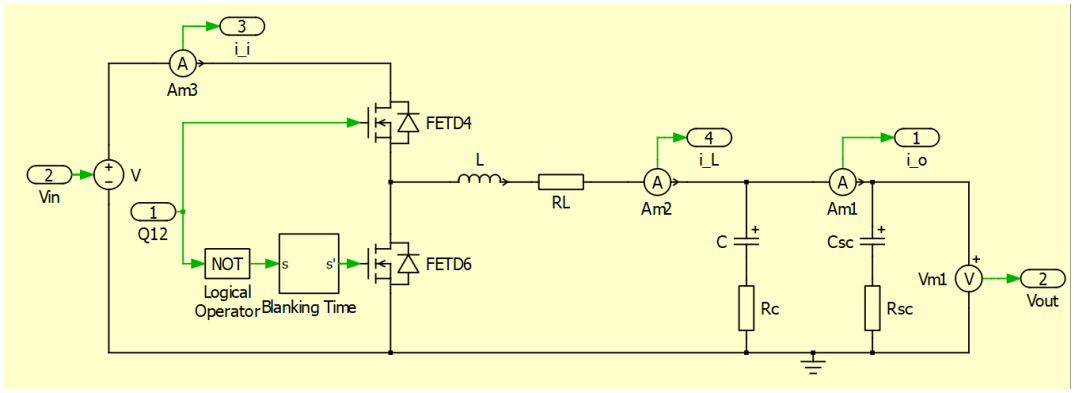


Figure 6.3: Plecs buck converter. Switches are ideal with on the input dead time. i_L, the inductor current is the primary variable of interest. Output capacitor C and super capacitor C_{sc} have initial conditions.

In Fig. 6.4 the signals of the model can be seen. The point of showing this figure is to emphasize the ADC sampling block. The sampling occurs when the center-aligned dual-slope PWM hits a top. This is ideally exactly in the middle of the current waveform of interest, giving an average current. This is all further explained in appendix D. For control the sampled signal $i_{L,samp}$ will always be used because it makes filters redundant. Feedback delay can be activated on the feedback as shown in Fig. 6.5 by setting "delay1=1". A choice can also be made between a constant duty cycle "`sw_duty=0`", continuous control "`sw_duty=1`" or digital control "`sw_duty=2`". For example in the next section a continuous controller is simulated, for that `sw_duty=1`.

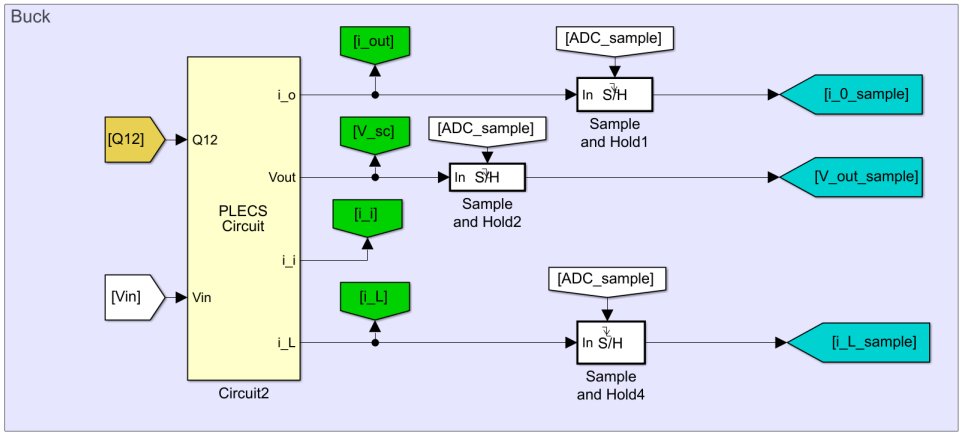


Figure 6.4: Simulink sampling. The sample-and-hold is triggered by the center-aligned PWM at a rate of 20 kHz.

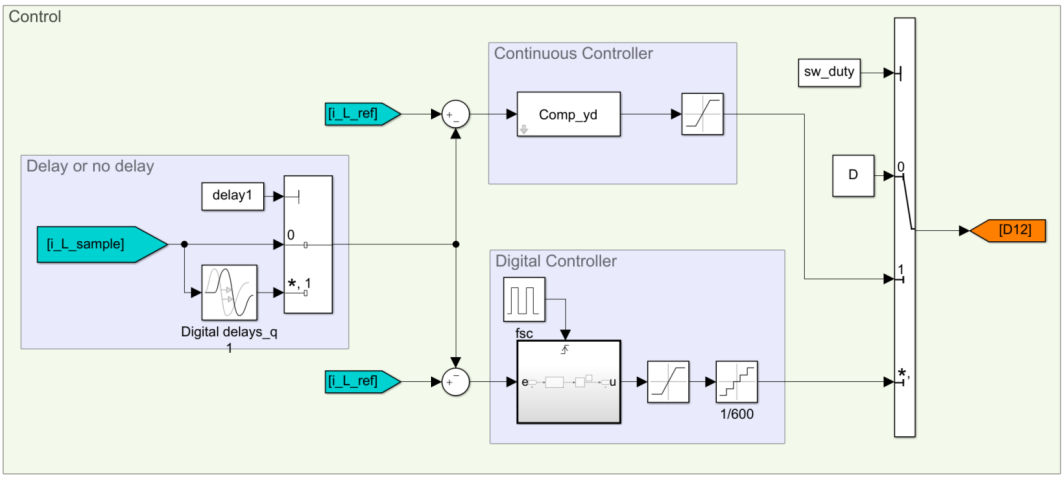


Figure 6.5: Simulink control, script controlled. The digital controller subsystem is triggered at a frequency of 2 kHz. Both control loops saturate at d_1=[0 1]. Quantization error is implemented equal to the real controller on digital branch.

6.3 Converter model for control design

As mentioned previously when the boost-leg in Fig. 6.1 is shorted (Q3='ON', Q4='OFF') the resulting circuit is a buck-synchronous converter. By assuming ideal switches the diodes will never conduct and thus the buck-synchronous converter can be viewed as having two modes of conduction. These two modes of conduction can be reviewed in Fig. 6.6. The aim of this section is to obtain as simple a model as possible and then look retrospectively on the accuracy of the derived model by comparing with the previous defined Plecs model in Simulink. In the future the results obtained here should be compared with experimental data to know for sure if the model or even the simulation is accurate.

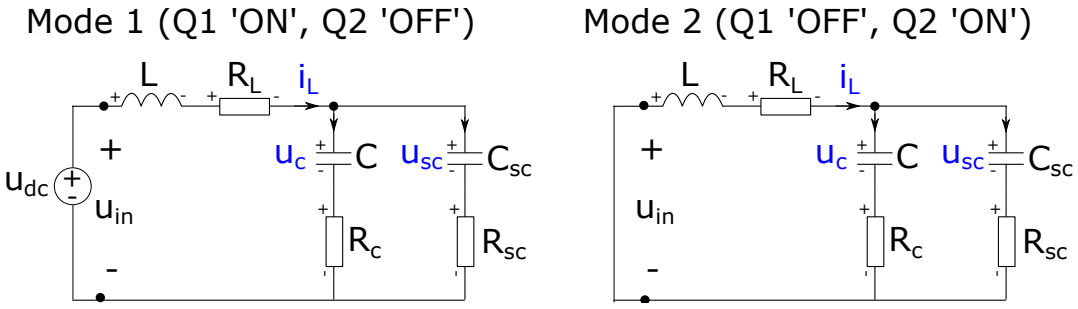


Figure 6.6: Buck-synchronous converter, idealised switches with parasitic series resistances for inductor, output side capacitor and super capacitor.

State-space averaging technique is used to acquire a linear model of the system. The technique involves finding a number of dynamic equations equal to the num-

ber of active components in the circuit for each mode. These dynamic equations are then written on a state-space form. The averaging arithmetic is as shown in Eq. (6.1) through Eq. (6.3). In the two modes shown in (6.6) everything to the right of the input voltage is unchanged through the two modes. This means that the average state matrix A is just state matrix A. [18]

$$\bar{A} = A_1 d_1 + A_2(1 - d_1) \tag{6.1}$$
$$\bar{B} = B_1 d_1 + B_2(1 - d_1) \tag{6.2}$$
$$\bar{C} = C_1 d_1 + C_2(1 - d_1) \tag{6.3}$$

Acquiring the dynamic equations is straightforward power circuit analysis. KVL is used on the voltage loop containing L and C_{sc} and then the voltage loop containing C_c and C_{sc}. The resulting dynamic Equations are Eq. 6.4 and Eq. 6.5 respectively. The third dynamic Equation is obtained by using KCL at the output current node, Eq. (6.6) is the result of that.

$$-u_{dc}(t) + R_L i_L(t) + L\frac{di_L(t)}{dt} + u_{sc}(t) + R_{sc}C_{sc}\frac{du_{sc}(t)}{dt} = 0 \tag{6.4}$$
$$-R_c C_c \frac{du_c(t)}{dt} - u_c(t) + u_{sc}(t) + R_{sc}C_{sc}\frac{du_{sc}(t)}{dt} = 0 \tag{6.5}$$
$$i_L(t) - C_c\frac{du_c(t)}{dt} - C_{sc}\frac{du_{sc}(t)}{dt} = 0 \tag{6.6}$$

There are three dynamic equations and three system states with their respective derivative, so it is a simple exercise of algebra to derive the governing derivative equations. First $\frac{du_c(t)}{dt}$ is isolated in (6.6) and substituted into Eq. (6.5) this gives an expression for $\frac{du_{sc}(t)}{dt}$ that can be rearranged to acquire Eq. (6.9). This process is repeated to acquire the expression for $\frac{du_c}{dt}$ shown in Eq. (6.8). Finally (6.9) is substituted into Eq. (6.4) and rearranged to give Eq. (6.7).

$$\frac{di_L(t)}{dt} = \frac{1}{L}\left[u_{in}(t) + i_L(t)\cdot(K_1 R_L - R_L) + u_{sc}(t)(K_1 - 1) + u_c(t)\cdot(-K_1)\right] \tag{6.7}$$
$$\frac{du_c(t)}{dt} = K_2\left(-u_c(t) + u_{sc}(t) + R_L i_L(t)\right) \tag{6.8}$$
$$\frac{du_{sc}(t)}{dt} = K_3\left(u_c(t) - u_{sc}(t) + R_L i_L(t)\right) \tag{6.9}$$

Where

$$K_1 = \frac{R_{sc}C_{sc}}{R_{sc}C_{sc} + R_c C_{sc}}, \quad K_2 = \frac{1}{R_c C_c + R_{sc}C_c}, \quad K_3 = \frac{1}{R_c C_{sc} + R_{sc}C_{sc}} \tag{6.10}$$

Already now it can be seen that the input u_{dc} only occurs in the first dynamic equation, so it is only the input-to-state matrix B that needs to be averaged, this is done in Eq. (6.11).

$$B_1 = \begin{bmatrix} \frac{u_{dc}(t)}{L} \\ 0 \\ 0 \end{bmatrix} \quad B_2 = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \Rightarrow \bar{B} = B_1 d_1 + B_2(1 - d_1) = \begin{bmatrix} \frac{u_{dc}(t)}{L} \\ 0 \\ 0 \end{bmatrix} d_1(t) \tag{6.11}$$

From Equations (6.7), (6.8) and (6.9) the state matrix is acquired and from Eq. (6.11) the input-to-state matrix. In Eq. (6.12) the state matrix, input-to-state matrix and state-to-output matrix, which is just the identity matrix to pass through the states, are shown. The states are, in order i_L, u_c and u_{sc}. The control input is the duty cycle d_1.

$$\begin{gathered} \dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}u, \quad \mathbf{y} = \mathbf{C}\mathbf{x} \\ \begin{bmatrix} \dot{i_L}(t) \\ \dot{u_c}(t) \\ \dot{u_{sc}}(t) \end{bmatrix} = \begin{bmatrix} \frac{K_1 R_L - R_L}{L} & \frac{-K_1}{L} & \frac{K_1 - 1}{L} \\ R_{sc} K_2 & -K_2 & K_2 \\ R_c K_3 & K_3 & -K_3 \end{bmatrix} \begin{bmatrix} i_L(t) \\ u_c(t) \\ u_{sc}(t) \end{bmatrix} + \begin{bmatrix} \frac{u_{dc}(t)}{L} \\ 0 \\ 0 \end{bmatrix} d_1(t) \\ \begin{bmatrix} i_L(t) \\ u_c(t) \\ u_{sc}(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_L(t) \\ u_c(t) \\ u_{sc}(t) \end{bmatrix} \end{gathered} \tag{6.12}$$

In appendix B the derivation of a average state space system with a resistive load instead of a capacitative load is done. In appendix B.1 the linearisation of a state space system is described. The linearisation results in the small signal state space system shown in Eq. (6.13) and Eq. (6.14). [18].

$$\dot{\tilde{\mathbf{x}}} = A_1 \tilde{\mathbf{x}} + B_1 \Delta_1 \tilde{u_{dc}} + B_1 U_{dc} \tilde{d_1} \tag{6.13}$$

$$\tilde{\mathbf{y}} = C_1 \tilde{\mathbf{x}} \tag{6.14}$$

Where U_{dc}, Δ_1 are the linearisation points of the DC-bus voltage and duty cycle respectively. $\tilde{u_{dc}}, \tilde{d_1}, \tilde{\mathbf{x}}$ are the small-signals or perturbations of the dc-bus voltage, duty cycle and states respectively. Because $\tilde{d_1}$ is the control input, $\tilde{u_{dc}}$ is set to zero and the linear state space system of interest can be written as shown in Eq. (6.15) and Eq. (6.16).

$$\dot{\tilde{\mathbf{x}}} = A_1 \tilde{\mathbf{x}} + B_1 U_{dc} \tilde{d_1} \tag{6.15}$$

$$\tilde{\mathbf{y}} = C_1 \tilde{\mathbf{x}} \tag{6.16}$$

The eigenvalues of the modes calculated using the parameters from Tab. 6.1 are shown in Eq. (6.17).

$$eig(A_1) = \begin{bmatrix} -252.1 & \text{rad/s} \\ -3623 & \text{rad/s} \\ -0.08615 & \text{rad/s} \end{bmatrix} \tag{6.17}$$

At this state it is a good idea to check the controllability. This can be checked by finding the rank of the controllability matrix defined in Eq. (6.18). There are three states and the rank is three, thus it has full rank, which means all states are controllable with the single input.

$$Co \triangleq [B \quad AB \quad A^2B] \tag{6.18}$$

We do not measure the states u_c and u_{sc} directly, but the super capacitor resistance is $R_{sc} = 6m\Omega$, which is low. This means that for practical implementation where it is desired to control u_{sc} it will be assumed that u_{sc} is identical to the super capacitor bank voltage, which is measured directly. The inductor current is directly measured. It will not be a goal to observe u_c so the system can be said to be observable.
Laplace transformation can be performed on the linearised state space system by assuming that the initial states are zero ($\mathbf{x}(t = 0) = 0$). This transform results in the transfer functions shown in Eq. (6.19). [19]

$$G(s) = C_1(sI - A_1)^{-1}B_1U_{dc} = \begin{bmatrix} g_{11}(s) \\ g_{21}(s) \\ g_{31}(s) \end{bmatrix} \tag{6.19}$$

These three transfer functions describes what happens to either of the three states given a change in duty cycle.
The transfer function of interest is from control input to inductor current, so g_{11} from Eq. (6.19). This transfer function is shown symbolically in Eq. (6.20). The root locus of the same transfer function is shown in Fig. (6.7).

$$g_{11}(s) = \frac{\tilde{i_L}(s)}{\tilde{d}_1(s)} = \frac{a_1s^2 + a_2s + a_3}{s^3 + b_1s^2 + b_2s + b_3} \tag{6.20}$$

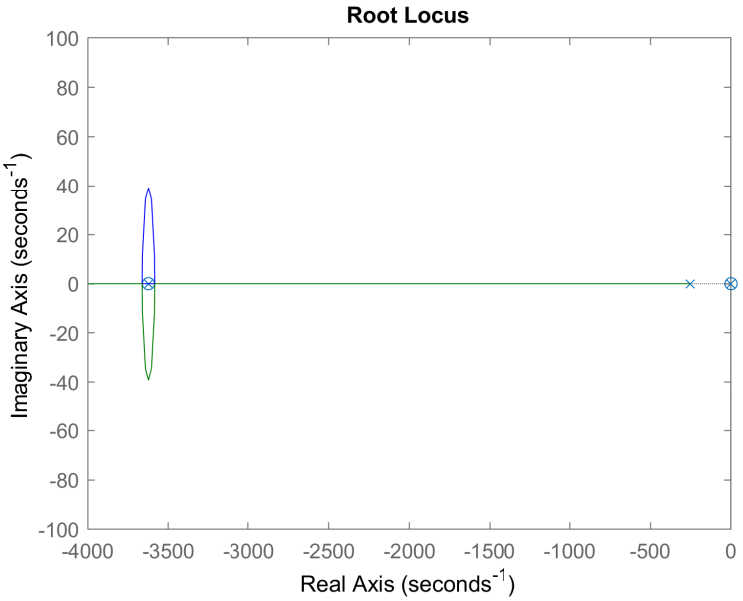


Figure 6.7: Root locus of (6.20). Pole and zero located at -0.08615 rad/s and -3623 rad/s.

There are three system poles in the root locus in Fig. 6.7, these correspond to the eigenvalues found in (6.17). Stepping the linearised state space system with d_1 at the operation point $U_{dc} = 30$ V results in the response shown in Fig. 6.8. The important thing to notice here is that the inductor current step response is a first order response that has a bandwidth of 252.1 rad/s. Now there is also the output capacitor and super capacitor whose response can be seen when zoomed out in Fig. 6.9. It can be seen in this step that even though the output capacitor has a fast response, presumably the fastest pole at 3623 rad/s, it follows the super capacitor voltage which has the slowest pole at 0.08615 rad/s. With this knowledge of the system a controller for the inductor current will be designed while disregarding the slow super capacitor pole and very fast output capacitor pole.

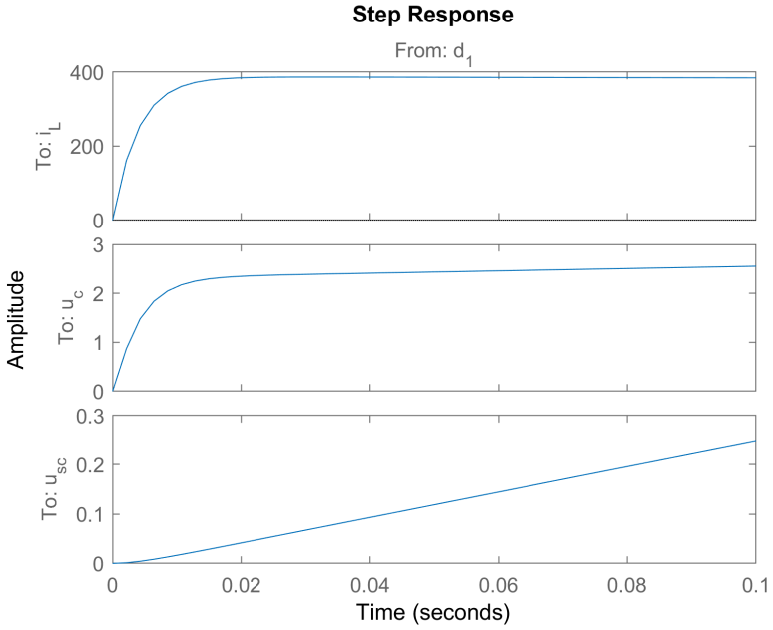


Figure 6.8: Step response of linearised state space system (6.15). $U_{dc} = 30$ V. Zoomed to 0.1s.

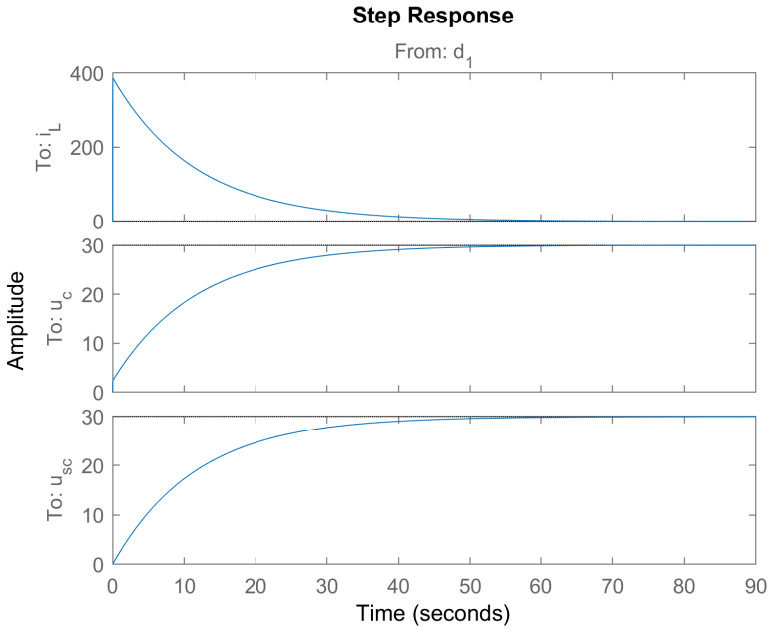


Figure 6.9: Step response of linearised state space system (6.15). $U_{dc} = 30$ V.

6.4 LTI current controller design

Through deductions from typical RL circuits it was found that R_L/L=-257.3290 rad/s which is close to the system pole at -252.1 rad/s. Thus this pole estimation will be used to design a controller because it is generally much more convenient to analyse and design symbolically. Besides, the measured parameters and parameters acquired from data sheets also have an uncertainty or tolerance. In conclusion the controller just has to be designed robust enough to handle parameter uncertainties. After removing the pole and zero pairs in Eq. (6.20) that cancel out, the resulting first order transfer function can be written as shown in Eq. (6.21).

$$minreal(g_{11}(s)) = \frac{U_{dc}}{R_L}\frac{\frac{R_L}{L}}{s+\frac{R_L}{L}} = K_{sc}\frac{a_{sc}}{s+a_{sc}} \tag{6.21}$$
$$K_{sc} = \frac{U_{dc}}{R_L}, \quad a_{sc} = \frac{R_L}{L}$$

A PI-controller is chosen because it contains a zero which can cancel out the pole of the system and a free integrator which increases the systems type. The PI-controller transfer function is shown in Eq. (6.22). To cancel out the pole of the system the PI-controller zero K_i/K_p has to equal the dominant pole of the system located at R_L/L. It also means that only the proportional gain has to be found and that it can be found with $K_i = K_p \cdot R_L/L$.

$$C_{pi,sc}(s) = K_p\frac{s+K_i/K_p}{s} \tag{6.22}$$

In Eq. (6.23) the open-loop transfer function of the super capacitor current loop is defined. In Eq. (6.24) the sensitivity function is defined and finally in Eq. (6.25) the closed-loop response transfer function is defined. [19]

$$\begin{aligned} L_{sc}(s) &= G_{sc,s}(s)\cdot C_{pi,sc}(s) \\ &= K_{sc}\frac{a_{sc}}{s+a_{sc}}K_p\frac{s+K_I/K_p}{s} \\ &= K_{sc}K_p\frac{a_{sc}}{s} \end{aligned} \tag{6.23}$$

$$\begin{aligned} S_{sc}(s) &= (1+L_{sc}(s))^{-1} \\ &= (1+K_{sc}K_p\frac{a_{sc}}{s})^{-1} \end{aligned} \tag{6.24}$$

$$\begin{aligned} T_{sc}(s) &= \frac{L_{sc}(s)}{1+L_{sc}(s)} \\ &= \frac{K_{sc}K_pa_{sc}}{s+K_{sc}K_pa_{sc}} \end{aligned} \tag{6.25}$$

The bandwidth is defined as being the frequency where the absolute value of the sensitivity function ($S_{sc}(s)$) crosses -3dB or $1/\sqrt{2}$ in magnitude from the bottom up. As such setting Eq. (6.24) equal to $1/\sqrt{2}$ and solving for K_p yields the expression shown in Eq. (6.26). [19]

$$K_p = \frac{\omega_{sc}}{K_{sc} a_{sc}} \tag{6.26}$$

Where ω_{sc} is the chosen bandwidth of the current controller in rad/s. In Fig. 6.10 and Fig. 6.11 step response simulation are done to see the performance of the designed continuous controller. The rise time is defined as being 63% of the relevant step size, so for a step of 0 to 5 A shown in Fig. 6.10(a) the time response is the time it takes to reach 3.15 A. For Fig. 6.10(a), Fig. 6.11(a) and 6.11(b) the time response is consistently at 1.01 ms, very close to 1000 rad/s. In Fig. 6.10(b) the Plecs model is slightly slower than the state space model. In essence the only difference between the state space and the Plecs model is the switching operation, in particular the dead time between the switches are suspected to be the cause of this occurrence. Another observation is that it only happens when crossing zero, which is an additional argument that it is dead time related.

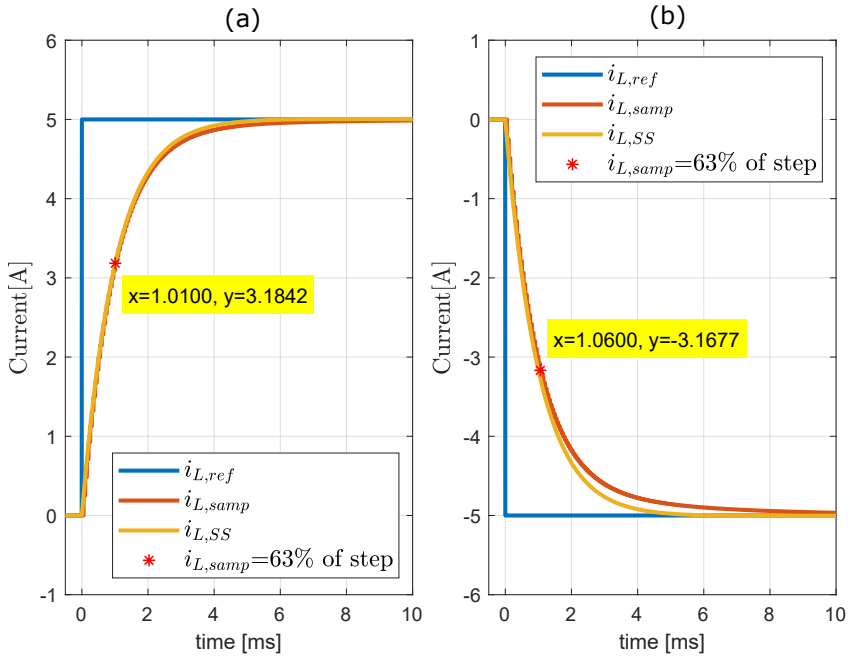


Figure 6.10: (a) 0 to 5 A step response. (b)0 to -5 A step response. Simulated sing simulation setup from Section 6.2. Continuous PI-controller shown in Eq. (6.22) tuned to a bandwidth of 1000 rad/s. $u_{sc}(t = 0) = 25$ V, $u_{in} = 30$ V.

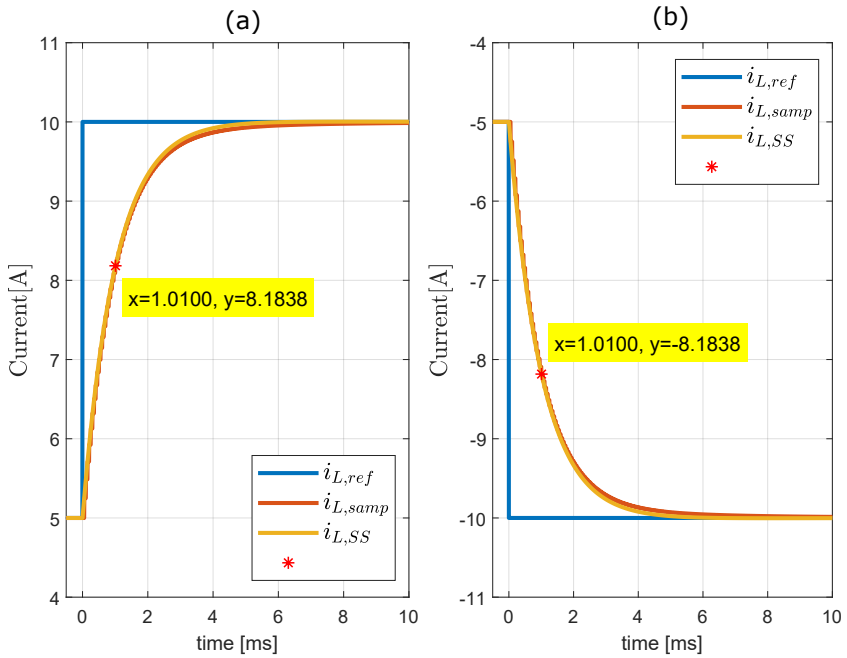


Figure 6.11: (a) 5 to 10 A step response. (b) -5 to -10 A step response. Simulated sing simulation setup from Section 6.2. Continuous PI-controller shown in Eq. (6.22) tuned to a bandwidth of 1000 rad/s. $u_{sc}(t=0) = 25$ V, $u_{in} = 30$ V.

6.4.1 Parameter uncertainty

The controller design is based on perfect pole cancellation with the PI-controller. So what happens if the parameters used for the control are larger or smaller than the actual values? In Fig. 6.12 a root locus plot of imperfect pole cancellation is shown. In Fig. 6.12(a) the parameters used for control design are too small while in Fig. 6.12(b) they are too large. In Fig. 6.12(a) root locus it can be seen that the closed loop poles break out and loop around, meaning they can be fast, but will also be under-dampened for certain gains. The root locus in Fig. 6.12(b) on the other hand has the closed loop poles moving towards the left plane and zero. This means that if the parameters are too large then the closed loop pole moving towards zero will make the system slow. I would choose to place the zero cancellation a little to the left of the pole because then fast dynamics can still be obtained.

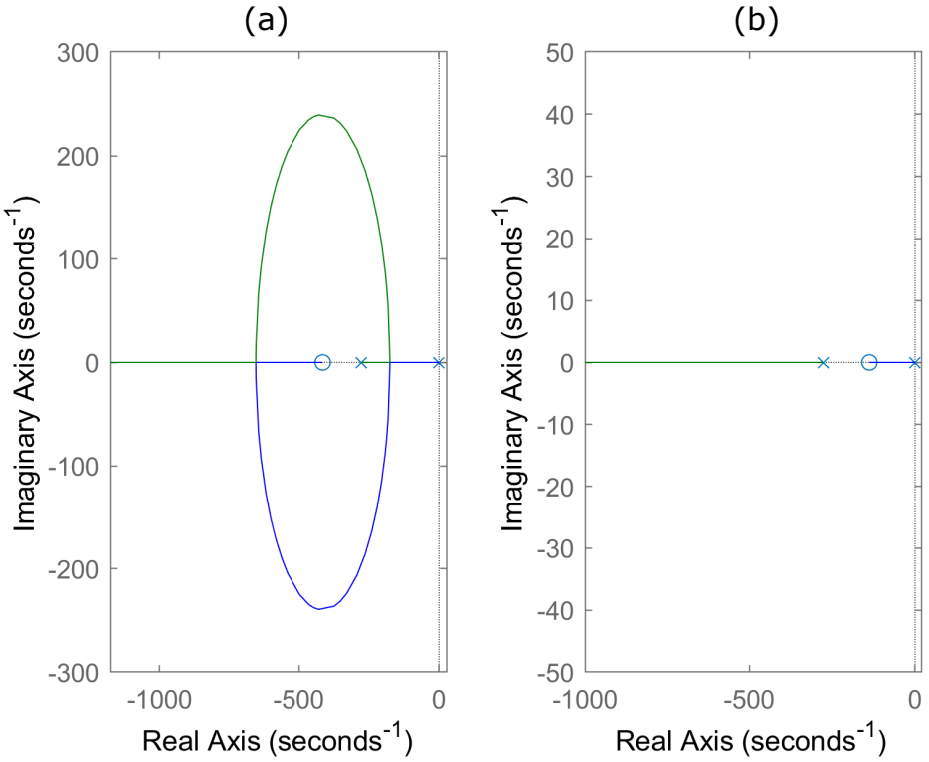


Figure 6.12: Root locus of open-loop continuous transfer function with mismatched pole cancellation.

6.5 Sampled data-hold Current Controller

In Fig. 6.13 a general sampled control system with a data-hold and a feedback filter is shown. The plant is $g_{11}(s)$ from Eq. (6.21) and the controller is $C_{pi,sc}(s)$ from Eq. (6.22).

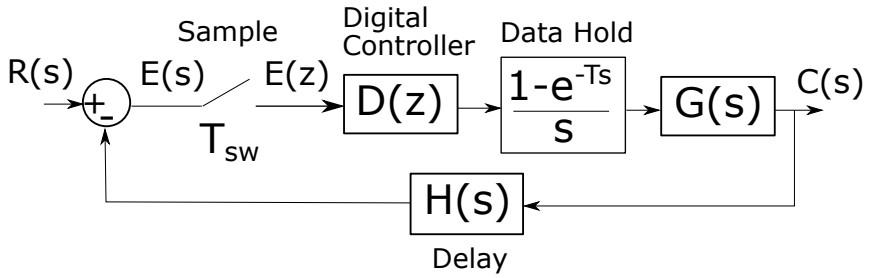


Figure 6.13: Digital control system diagram, from [20].

The closed loop transfer function of the control diagram in Fig. 6.13 is shown in Eq. (6.27) and the open-loop transfer function is shown in Eq. (6.28). [20]

$$T_{sc}(z) = \frac{C(z)}{R(z)} = \frac{D(z)G^*(s)}{1 + D(z)GH^*(s)} \tag{6.27}$$

$$L_{sc}(z) = D(z)GH^*(s) \tag{6.28}$$

The star signifies the starred transformation from a continuous to a sampled-data transfer function. [20] Previously the s-plane was used for analysing the LTI system, however to use bode plots and root locus techniques on a discrete time system we need to analyse it in the w-plane. The w-plane means to use the bilinear or 'Tustin' mapping from the s-plane to z-plane. w-plane signifies the starring transformation has been done with the bilinear method defined in Eq. (6.29). [20]

$$w \triangleq \frac{2}{T_{sw}}\left[\frac{z-1}{z+1}\right]_{z=e^{s}T_{sw}} \tag{6.29}$$

In Fig. 6.14 the Root locus of the open-loop transfer function from Eq. (6.28) is plotted with a gain from 0.01 to 10. The feedback is set to H=1 to emulate a unity feedback. The red cross marked with an accompanying data tip is the minimum real closed loop pole of the system at a gain of 1. This closed loop pole is obtained from the characteristic equation which is the denominator of the closed loop transfer function in Eq. (6.27). In the figure it can be seen that the minimum real closed loop pole is located close to 1000 rad/s which it was designed for.

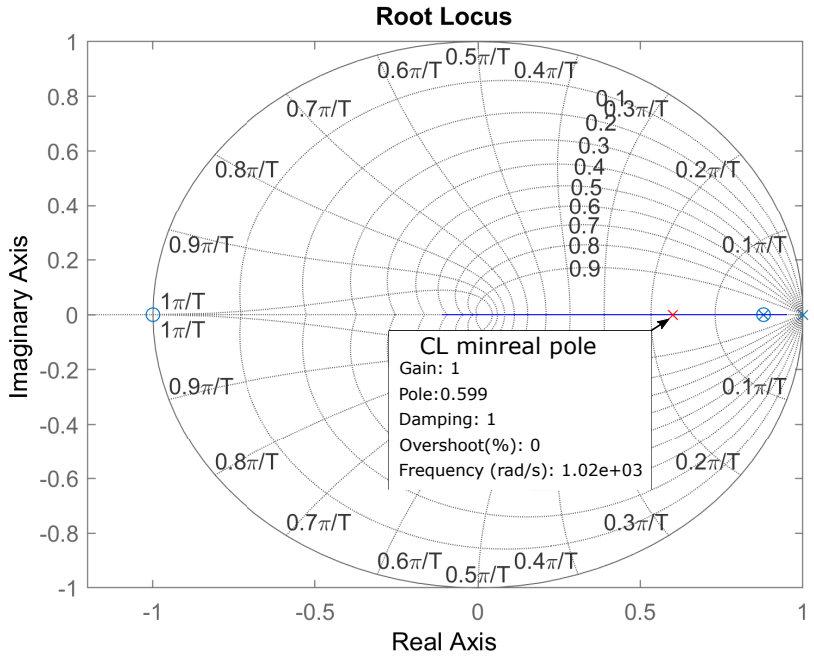


Figure 6.14: Root locus analysis of Eq. (6.27) in the w-plane. With unity feedback.

In appendix D it was investigated how the A/D and D/A peripherals of the hardware would affect the timing in the control. It was found that the worst case of feedback delay was one period (PER) of the PWM frequency corresponding to 1/20 kHz or $PER = 0.5\mu s$. The first order response signifies the shunt resistor op-amps effective bandwidth. The effective bandwidth of said op-amp is specified to be 10 kHz in its datasheet [21]. This means that the first order lowpass filter on the feedback has a bandwidth of 10 kHz. The sampling rate of the system is only 2 kHz, so it is impossible to capture the transient of the op-amp. Yet the transient will still add additional delay on the sampled signal corresponding to the rise time of the op-amp. In Eq. (6.30) the expected feedback transfer function is shown.

$$H(s) = \frac{e^{-s \cdot PER}}{\frac{1}{2\pi 10000}s + 1} \tag{6.30}$$

A third order Páde estimation is used to approximate the delay for root locus and bode plot analysis purposes. The reason why a Páde estimation is used is because then pole-zero tools can still be used to analyse the system and design control.
In Fig. 6.15 the same procedure as Fig. 6.14 is used to plot the root locus, with the minimum real closed loop pole marked with a red cross. Instead of having unity feedback the delay function (6.30) is now used to investigate the effect of a delay in the sampling. As can be seen on the data tip in Fig. 6.15 the minimum real closed-loop pole is now located at 1080 rad/s. Thus having a delay on the feedback causes the response to quicken. It should be noted that with a delay of one PER, the real pole is critically damped until the gain is above 3. This is the gain where the root locus passes origin in Fig. 6.15. With a gain higher than 3 the system is still stable, but it is under-dampened.

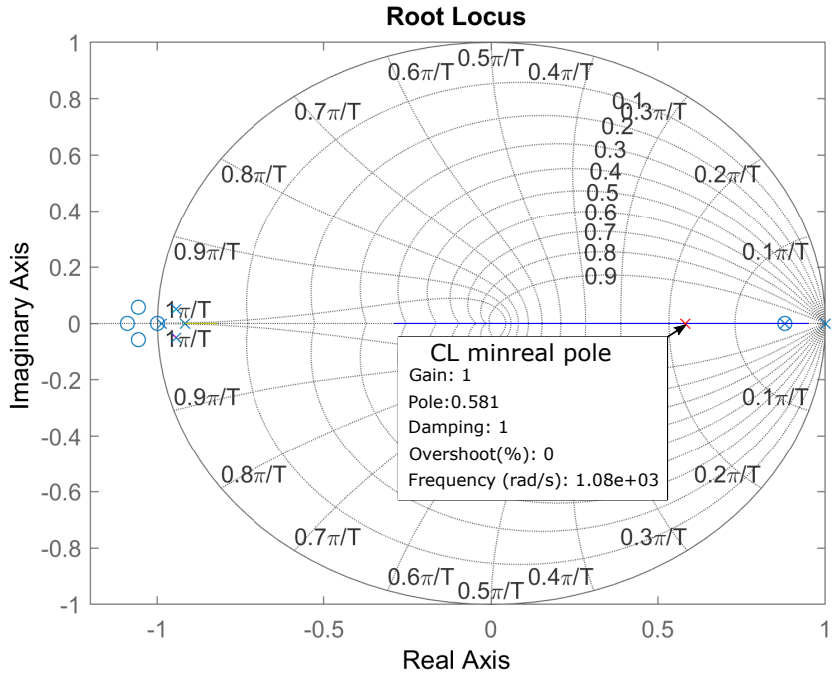


Figure 6.15: Root locus analysis of Eq. (6.27) in the w-plane. With delay feedback seen in Eq. (6.30). The Páde delay estimation is what causes poles and zeros on around the point -1.

Another way to look at the robustness of this control is to look at the open-loop bode plot as is shown in Fig. 6.16. Here it can be seen that the phase margin is 87 degrees, which means the controller can be pushed a lot more before it becomes unstable, in other words it is robust. The next step is to simulate some steps with the discrete controller in the non-linear simulation to see how accurate the w-plane analysis is.
In Fig. 6.17(a) the system is stepped from 0 to 5 A and in Fig. 6.17(b) the from 0 to -5 A. First it can be seen that the Plecs model and the state space model are still following each other, except in 6.17(b) where the Plecs model is slower like with the continuous controller. An important thing to to see from the current steps is that the response time is 0.81 ms corresponding to 1235 rad/s. This is faster than the expected closed loop pole with delay, which was 1080 rad/s from Fig. 6.15. Nevertheless, the response is consistent and stable, so the current controller can be considered to be finished. The last question to answer is about the steady state ripples occurring on both the State Space average model and the Plecs model. The fact that they occur on the State Space average model means it has nothing to do with the switching and rather it is found that it is because of the quantization error. The effect is not profound, but it will be investigated along with the inductor current ripples in the next section.

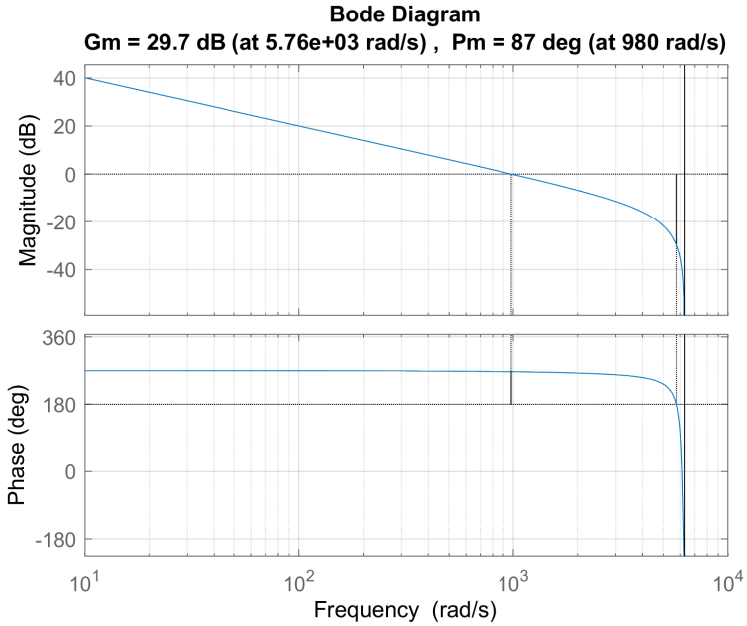


Figure 6.16: Bode plot of open loop transfer function Eq. (6.28) with phase and gain margins marked at the top. With delay.

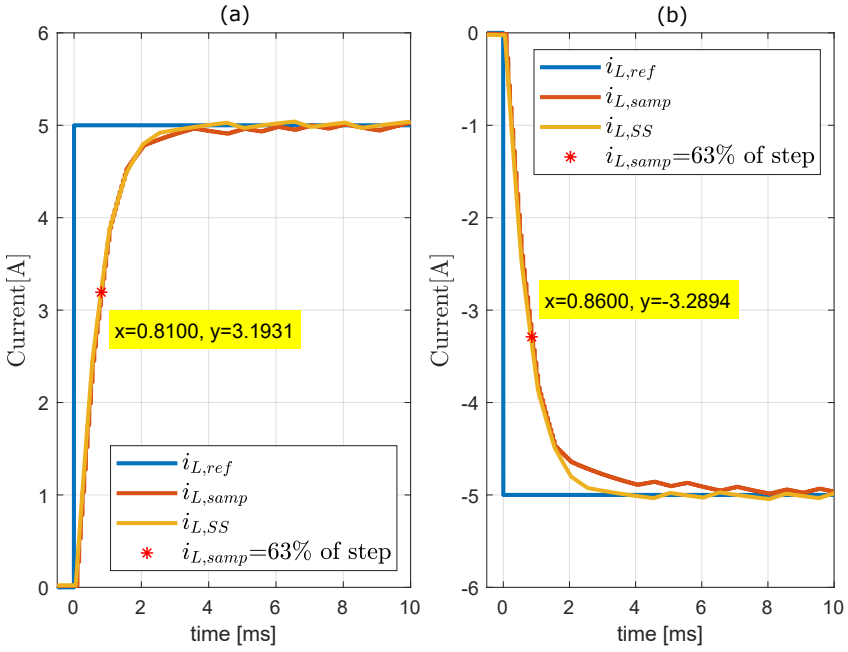


Figure 6.17: Current stepping 0 to 5 A and 0 to -5 A. $u_{sc}(t=0) = 25$ V, $u_{in} = 30$ V. Simulated sing simulation setup from Section 6.2.

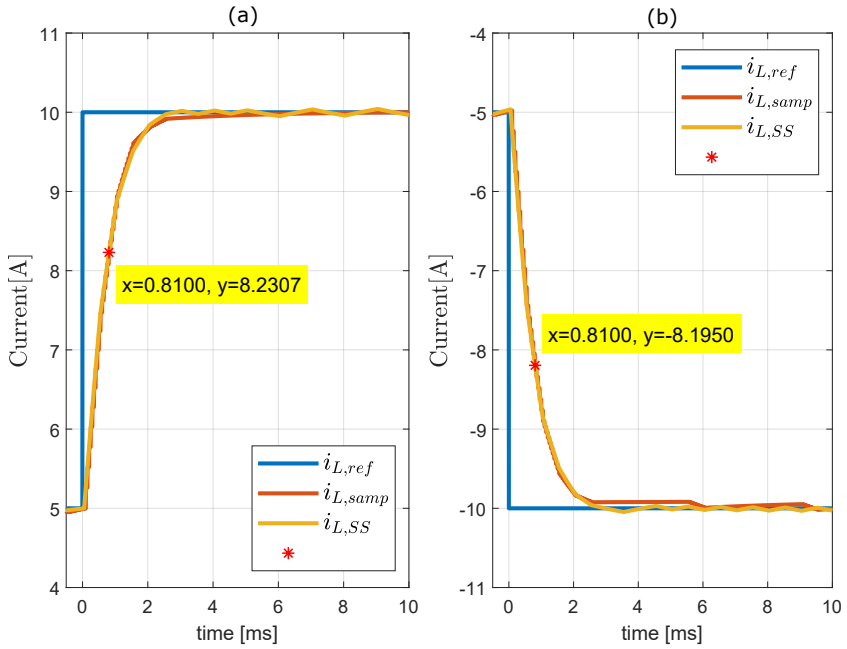


Figure 6.18: Current stepping 5 to 10 A and -5 to -10 A. $u_{sc}(t = 0) = 25$ V, $u_{in} = 30$ V. Simulated sing simulation setup from Section 6.2.

6.5.1 Quantization error and current ripples

In the current steps in Fig. 6.17 and Fig. 6.18 it can be seen that there are ripples in the average current when it is in steady state. This is a clear indicator that the steady state control input is bouncing between two available duty cycle set points. Quantization error or control input resolution is determined to be $1/600$ for 0 to 1 in duty cycle. The calculation for this resolution is described in appendix D. To investigate this effect the simulation was run until inductor current reached steady state with an array of different duty cycles and input voltages. The super capacitor is replaced with a voltage source at 25 V, because otherwise the voltage would blow up or discharge completely in a steady state simulation. The result of this steady state simulation is shown in Fig. 6.19. Fig. 6.20 shows the small red box in Fig. 6.19 zoomed in.

Fig. 6.20 is read like each grid line is a settable duty cycle. This means that between 10 A and 20 A there are 16 settings of duty cycle and as a consequence the DC-current resolution is $10A/16ticks = 0.625A/tick$. This means that certain current references can cause the duty cycle to bounce between two values. The resolution can be increased by choosing single-slope PWM rather than dual-sloped PWM. This will double the resolution. Alternatively the PWM frequency can be decreased, however, this will result in larger current ripples unless the inductors inductance is increased at the same time. The explanations for why this will reduce

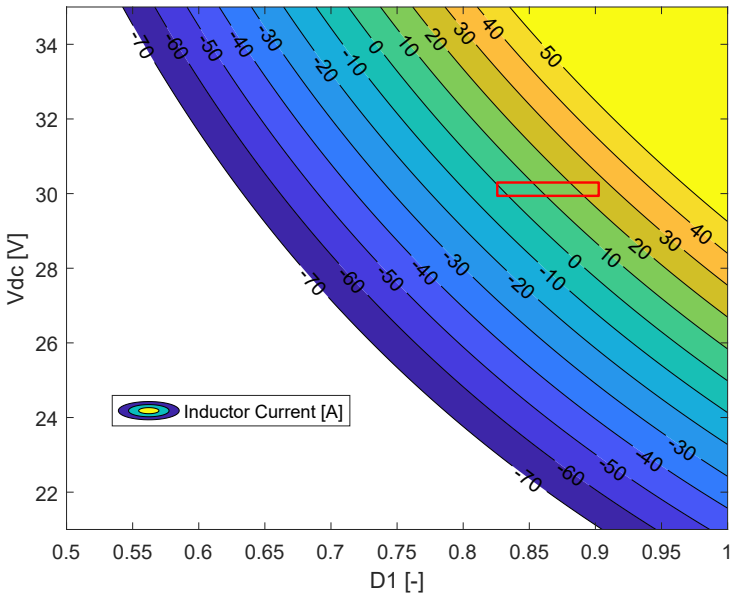


Figure 6.19: Steady state inductor current isoclines. Alternating input/DC-bus voltage and open-loop duty cycle. Super capacitor considered to be a constant voltage source of 25 V.

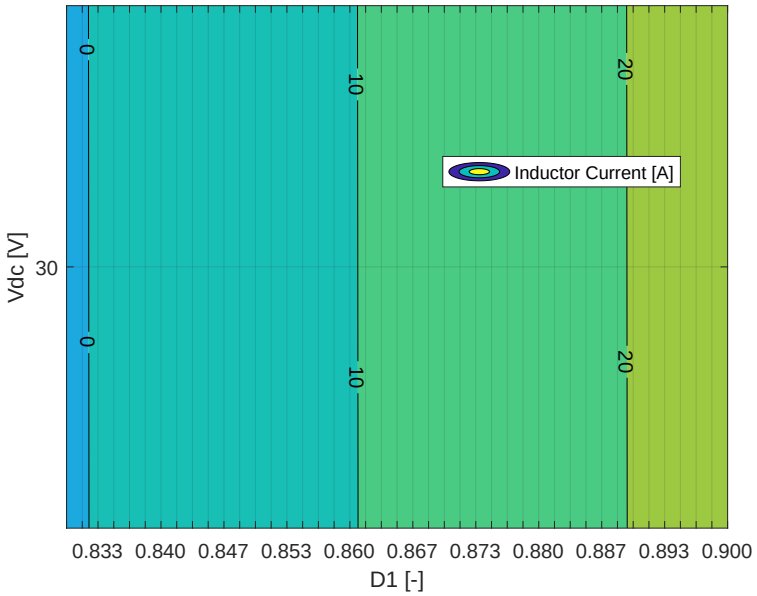


Figure 6.20: Inductor Current Isocline, zoomed in on 30 V input voltage between D1=[0.83, 0.9] of Fig. 6.19. x grid corresponds to 1/600 resolution of duty cycle for PWM.

the quantization error can be found in Appendix D.
In Fig. 6.21 a zoomed in view of the steady state current from Fig. 6.18(b) is presented. Fig. 6.21 shows the quantization ripples and inductor ripples at steady state. It can be seen that the current ripples from the switching are around ± 0.4 A and the slower ripples caused by the quantization error has a amplitude of ± 0.1 A. In conclusion the quantization error is noticeable but not critical. The switching ripples amplitude of 4% of the average current is acceptable.

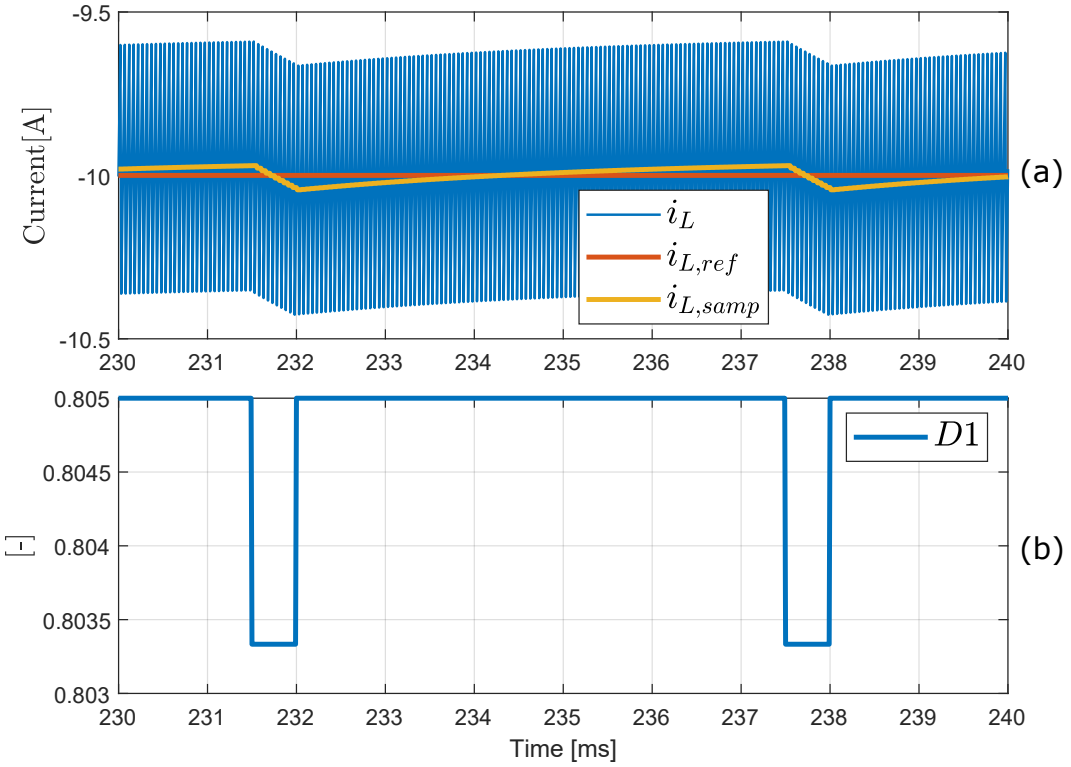


Figure 6.21: Zoomed view of steady state current ripples. (a) Inductor current, continuous, reference and sampled. (b) Control input bounce due to quantization error. 1 PER delay, quantization (1/600) error, $\omega_{sc} = 1000 rad/s$, $u_{dc} = 30V$, $U_{sc} = 25V$.

Now that a current controller has been designed and analysed for the Super Capacitor, the next step is use this controller to design a DC-bus voltage controller.

Chapter 7

Power control Solution

Contents

This chapter combines the knowledge obtained from all the previous chapters to design a power control solution that can answer the problem statement. Specifically the aim is to be able to control the fuel cell output power while maintaining a stable DC-bus voltage. The chapter is divided into three sections. The first section is about a general power control strategy. The second section is about designing a controller for the DC-bus voltage. The last section is a simulation of the full dynamic system using the power control solution designed in the first and second section.

7.1 Power control strategy

The ultimate goal of implementing the super capacitor bank in the system is to control the output power of the fuel cell. In chapter 4 it was proposed that the fuel cell could supply a constant 100 W to the system. The DC-bus is in parallel to the fuel cell stack output, why controlling one means controlling the other. In Chapter 2 the fuel cell was analysed and a polarisation curve for the fuel cell voltage as a function of fuel cell current was found. The polarisation curve has one degree of freedom, so controlling one means controlling the other. Since the power is given by multiplying the voltage and current, then that means controlling the voltage or current is enough to control the output power of the fuel cell.
The DC-bus voltage set point can be chosen by considering the fuelcell voltage and power correlation shown in Fig. 7.1. If the wanted mean fuel cell power is

calculated to be 100 W, then the fuel cell current should be 3.24 which corresponds to a fuel cell voltage of 31 V. Then the DC-bus voltage controllers set point should be set to 31 V. Or if the wanted power was 200 W, then the set point should be close to 29 V. The point is that if the DC-bus voltage is controlled then there is a large degree of freedom in choosing the mean fuel cell power.

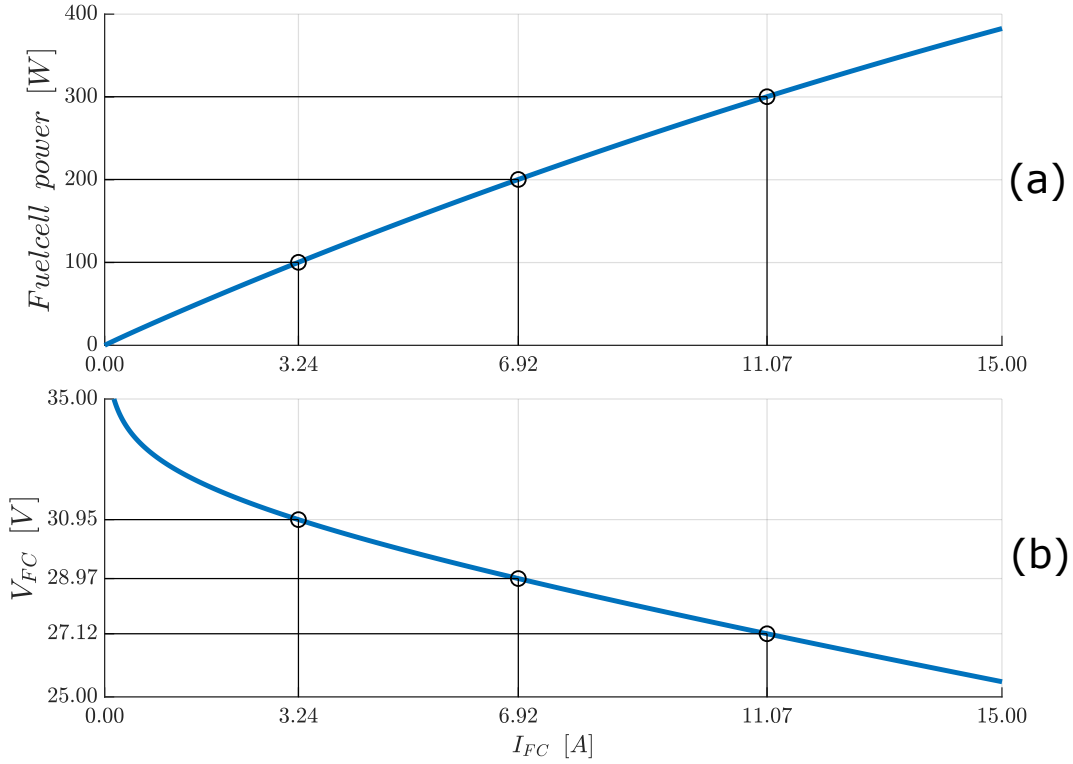


Figure 7.1: (a) Fuel cell power curve. (b) fuel cell polarisation curve. Correlation between fuelcell power and DC-bus/Fuelcell voltage. Example: Choose mean fuelcell power of 100 W. This requires 3.24 A to be drawn which corresponds to a fuelcell voltage of approximately 31V. By controlling DC-bus voltage to be 31 V the power draw from the fuelcell will be 100 W.

7.2 DC-bus voltage control design

In chapters 2,6 and 4 models are derived for the fuelcell, super capacitor converter and motor, respectively. The purpose of the models derived, is to describe the power flow of the system components through the DC-bus node where they connect. In Fig. 7.2 the DC-bus node and its connection to the three system components is shown. There are four currents at the DC-bus node, defined as shown in the diagram.

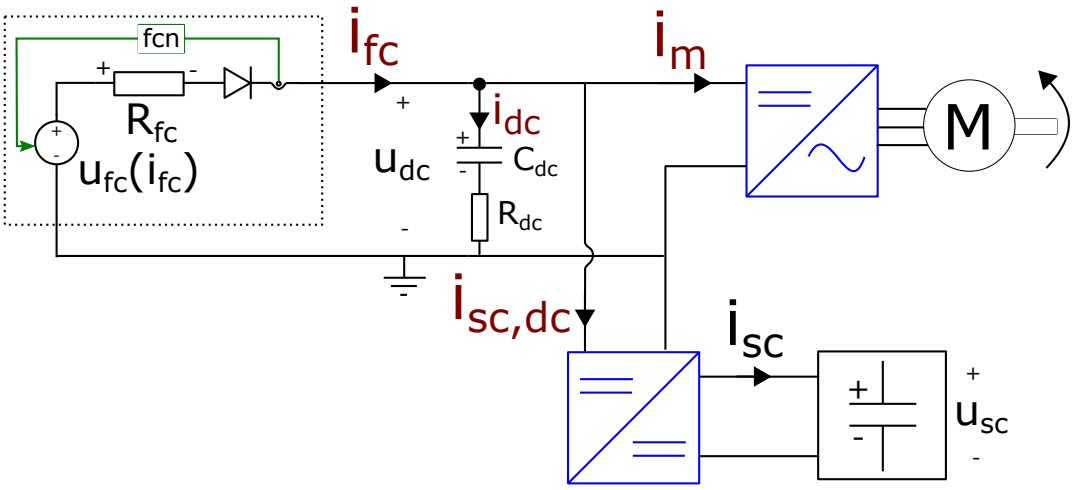


Figure 7.2: Electric diagram of DC-bus. Converter, inverter and fuel cell are analysed in their separate chapters.

The voltage drop over the DC-bus capacitor and equivalent series resistance can be described as shown in Eq. (7.1). Assuming that the initial states are zero a Laplace transform is performed resulting in Eq. (7.2). In Eq. (7.3) a transfer function for the DC-voltage with the DC-current as an input is derived from Eq. (7.2). With a transfer function for the DC-bus voltage voltage, the next step is make a transfer function for the DC-bus current.

$$u_{dc}(t) = \frac{1}{C_{dc}} \int i_{dc}(t)dt + R_{dc} i_{dc}(t) \tag{7.1}$$

$$u_{dc}(s) = \frac{1}{sC_{dc}} i_{dc}(s) + R_{dc} i_{dc}(s) \tag{7.2}$$

$$\frac{u_{dc}(s)}{i_{dc}(s)} = \frac{1}{sC_{dc}} + R_{dc} = \frac{1 + R_{dc}C_{dc}s}{C_{dc}s} \tag{7.3}$$

The instantaneous currents can be described with KCL on the DC-bus current node, this balance is shown in Eq. (7.4). Again assuming initial states are zero, the Laplace transform can be performed, the result of which is shown in Eq. (7.5) with $i_{dc}(s)$ isolated.

$$i_{fc}(t) - i_{dc}(t) - i_m(t) - i_{sc,dc}(t) = 0 \tag{7.4}$$

$$i_{dc}(s) = i_{fc}(s) - i_m(s) - i_{sc,dc}(s) \tag{7.5}$$

Eq. (7.3) and Eq. (7.5) are used to describe the DC-bus voltage response, but each current in Eq. (7.5) also has to be described. The motor current i_m is treated as a disturbance in this study, so when designing control it suffices to have an

idea of its frequency. The frequency of the disturbance is by filtering the motor reference with a pre-filter, or more specific a lowpass filter. The fuel cell current is inversely proportional to the DC-bus voltage with the equivalent fuel cell Ohmic resistance. This is under the assumption that the fuel cell is only operated in the Ohmic operation region above approximately 50 W. The Super capacitor current seen from the DC side is $i_{sc,dc}$. This current can be calculated by assuming a lossless converter for the super capacitor. Under this assumption the power balance can be written as shown in Eq. (7.6). In the transfer functions the conversion factor u_{dc}/u_{sc} is linearised to a DC-gain, otherwise the non-linearity will make control design unnecessary complex. Assuming the DC-bus voltage is controlled close to 31 V and the super capacitor voltage is close to 25 V then the conversion DC-gain is 25/31.

$$u_{dc}(t)i_{sc,dc} = u_{sc}(t)i_{sc}(t) \Leftrightarrow i_{sc,dc}(t) = \frac{u_{sc}(t)}{u_{dc}(t)}i_{sc}(t) \Leftrightarrow i_{sc}(t) = \frac{u_{dc}(t)}{u_{sc}(t)}i_{sc,dc}(t) \quad (7.6)$$

The instantaneous motor current drawn from the DC-bus i_m is derived from Eq. (7.7). The estimate of the current, based on the FOC current reference and designed response is shown in Eq. (7.8). Eq. (7.7) is used in the simulation, while Eq. (7.8) is used for feedforward disturbance rejection of the motor current.

$$i_m(t) = \frac{3}{2}\frac{i_q(t)u_q(t) + i_d(t)u_d(t)}{u_{dc}(t)} \quad (7.7)$$

$$i_{m,est}(s) = \frac{R_s + sL_q}{(\tau_{i_q}s+1)^2}i^2_{q,ref}(s) - \frac{\omega_r\lambda_{mpm}}{\tau_{i_q}s+1}i_{q,ref}(s) \quad (7.8)$$

In Fig. 7.3 the final system diagram is shown. A negative feedback loop is added for controlling the DC-bus voltage with the super capacitor converter. The next step is to close the inner loops to acquire an open-loop transfer function to which control can be designed.
There are two inner loops, the first is the fuel cell current feedback. Closing this loop yields a new plant transfer function which is shown in Eq. (7.9).

$$G_{dc,fc}(s) = \frac{u_{dc}(s)}{i_{sc,dc}(s)}\frac{-G_{dc}(s)}{1 - \frac{1}{Rfc}G_{dc}(s)} \quad (7.9)$$

The super capacitor converter inner loop from $i_{sc,ref}$ to i_{sc} is estimated by a first order response in the w-plane, shown in Eq. (7.10).

$$T_{sc,est}(w) = \frac{i_{sc}(w)}{i_{sc,ref}(w)} = \frac{1}{\tau_{sc}w + 1} \quad (7.10)$$

Where w denotes the Tustin transformation. In Fig. 7.4 the resulting diagram from closing the inner loops is shown. In theory if $i_{m,est} = i_m$ then perfect feedforward

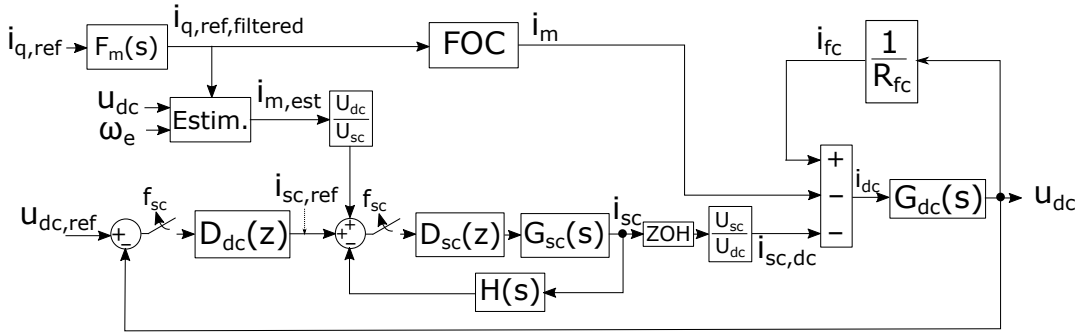


Figure 7.3: DC-bus voltage control structure. Estim. is an estimator for the motor current based on the reference i_q current. FOC is the model that contains the motor and mechanical dynamics. $F_m(s)$ is a pre-filter (Lowpass) to the motor current reference.

disturbance rejection can be achieved. [20] Yet, the world is not ideal, so a robust controller is designed next. The criteria is that it has zero steady state error and acceptable disturbance rejection, even without feedforward disturbance rejection.

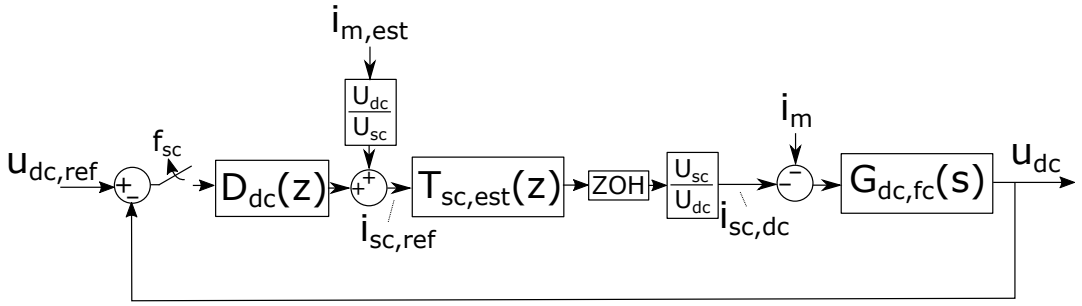


Figure 7.4: System diagram from Fig. 7.3 with closed inner loops. Recognizable as a standard sampled data-hold control diagram. [20]

An open loop transfer function can be acquired from Fig. 7.4 from $u_{dc,ref}$ to u_{dc} by setting i_m and $i_{m,est}$ to zero.
The open-loop transfer function is shown in Eq. (7.11). Where the star denotes the Tustin discretization of the plant. $T_{sc,est}$ is already in the discrete plane and D_{dc} will be designed directly in it.

$$L_{dc}(w) = D_{dc}(w)T_{sc,est}(w)\frac{U_{sc}}{U_{dc}}G^*_{dc,fc}(s) \tag{7.11}$$

In Fig. 7.5 the root locus of the open-loop transfer function from Eq. (7.11) is shown. An important thing to notice in the root locus for the open-loop transfer function is that there is no free integrator. The zero and pole at z=1 cancels each other out, so the system type is zero. It is important that the system type is at least one, otherwise there will be a steady state reference tracking error. The simplest way to increase the system order is to insert a free integrator with a gain. Doing

so will result in the root locus shown in Fig. 7.6. The gain is then increased until the closed loop poles are located where the red crosses are drawn in Fig. 7.6. The controller is as shown in Eq. (7.12). The closed loop poles have characteristics of a dampening of 0.707, around 4.5% overshoot and 180 rad/s in bandwidth. There is no reason to choose a more advanced controller since the controller criteria are met.

$$D_{dc}(w) = 360/w \tag{7.12}$$

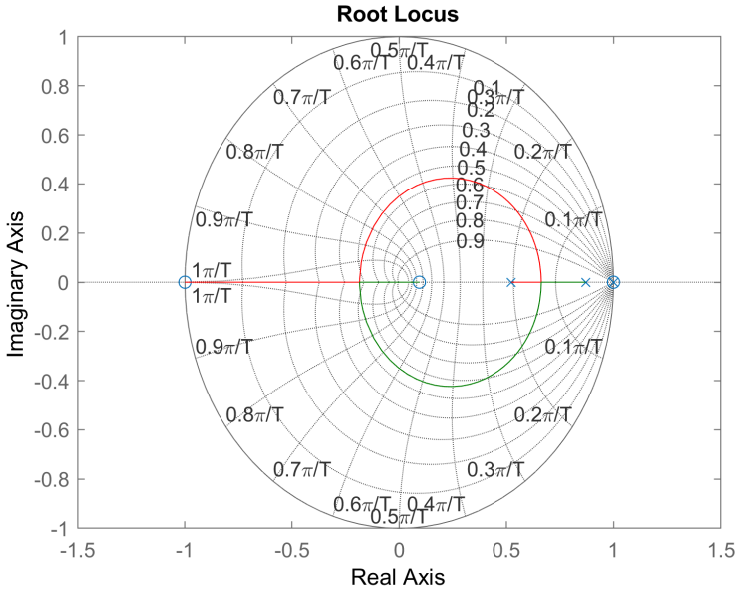


Figure 7.5: Root locus of Eq. (7.11).

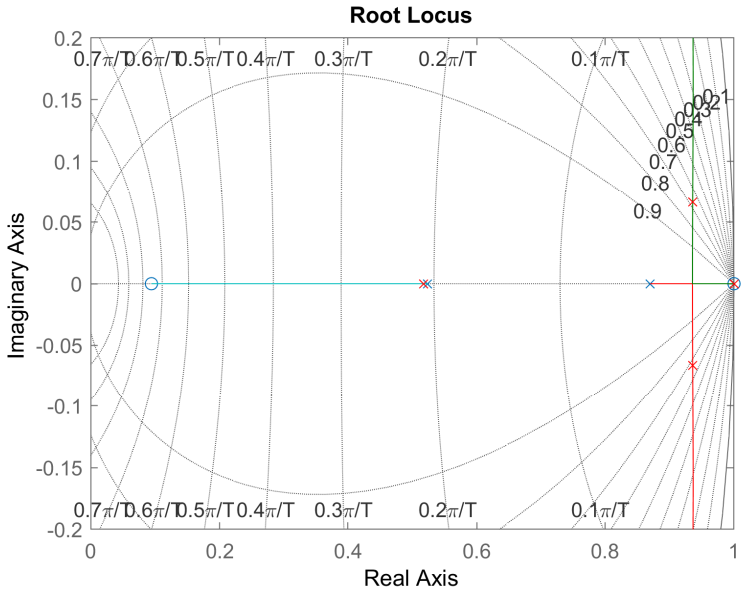


Figure 7.6: Root locus of Eq. (7.11) with a free integrator to increase system type

To check the disturbance rejection a closed loop transfer function from i_m to u_{dc} has to be derived. This is done by setting both $u_{dc,ref}$ and $i_{m,est}$ to zero and closing the loop. The disturbance transfer function or sensitivity transfer function is shown in Eq. (7.13). In Fig. 7.7 the disturbance transfer function is stepped with a pre-filtered step with a of 10 A. The pre-filter is a measure that is implemented because there is simply no reason for instantaneous stepping of the motor torque reference in the real system. In this analysis the pre-filter is a lowpass filter with a bandwidth of 50 rad/s. In the real implementation the pre-filter may be set to something like 10 rad/s, then with a bandwidth of 180 rad/s on the DC-bus voltage control loop the disturbance rejection will be much better. Yet, for the sake of the argument of using feedforward disturbance and pushing the system, the pre-filter bandwidth is left at 50 rad/s.

$$\frac{u_{dc}(w)}{i_m(w)} = \frac{G_{dc,fc}(w)}{1 + L_{dc}(w) D_d c(w)} \tag{7.13}$$

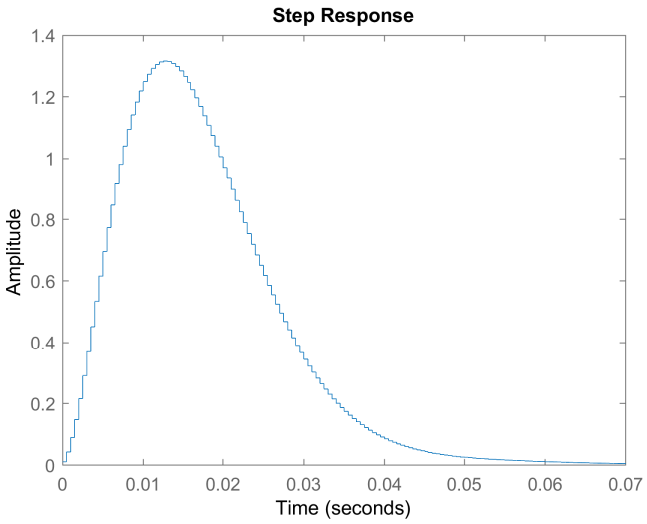


Figure 7.7: Pre-filtered step of Eq. (7.13) with amplitude of 10 to test disturbance rejection of the system. Equivalent to i_m being stepped from 0 to 10 A filtered with a lowpass filter that has a bandwidth of 50 rad/s.

7.3 Full dynamic simulation

Having designed control for the DC-bus and investigated the expected disturbance rejection capabilities of the system it is time to simulate it.
The full Plecs schematic is shown in Fig. 7.8. The super capacitor current control is implemented with the digital controller as it was simulated in Chapter 6. In fact, most of the simulation is explained in Chapter 6. Additionally the simulation is attached to the project and can be run from the Matlab file `'Full_dynamic_sim.m'`. The changes of the Plecs schematic from in Chapter 6 is the addition of the fuel cell simplified model and parallel motor current source in parallel with the DC-bus. The change in the control structure is that an outer loop feedback loop is added to control the DC-bus voltage.

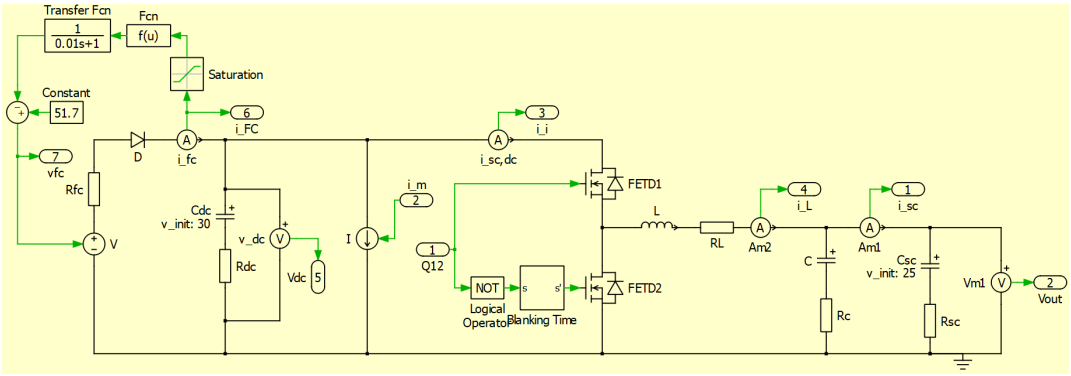


Figure 7.8: Dynamic plecs model

The reference $u_{dc,ref}$ is set to 31 V, which should mean approximately 100 W is drawn from the fuel cell. The motor i_q is stepped from 0 to 10 A, from 10 A to 0 A and finally from 0 A to -10 A. i_q and i_m are not to be confused, i_q controls the torque, but if the vehicle is at standstill this still translates to $i_m = 0$. Thus the rotational speed of the motor has an initial condition which translates to approximately 19 km/h in linear vehicle speed. The super capacitor initial charge is at 25 V.
In Fig. 7.9 data from the full dynamic model is shown. In Fig. 7.9(a) the currents of the system are shown. i_{sc} is the super capacitor current, seen at the super capacitor side. i_m is the motor current disturbance and i_{fc} is the current drawn from the fuel cell at the DC-bus. In Fig. 7.9(b) the DC-bus voltage is shown, both sampled and continuous. In Fig. 7.9(c) the motor and super capacitor power are shown. Finally in Fig. 7.9(d) the fuel cell power is shown, continuous and with a moving average filter. First thing to notice in Fig. 7.9(b) is that $u_{dc} = 31$ V in steady state, thus no steady state error. The second thing to notice in the same graph is that the disturbances at 0.2, 0.5 and 0.8 seconds are close in shape to the disturbance step in Fig. 7.7 with an almost identical amplitude of 1.3 V, meaning the sensitivity transfer function is correct or close to. In Fig. 7.9(d) the fuel cell power can be seen to be very close to 100 W when the motor is drawing power. When the motor is supplying power the fuel cell power drops to around 90 W in steady state, which is still okay because the motor is drawing power most of the time in the race. The DC-bus voltage disturbance ripple with an amplitude of 1.3 V can be reduced by using the feedforward disturbance rejection shown in Eq. (7.8). The results of repeating the same simulation, but now with feedforward disturbance rejection is shown in Fig. 7.10. In Fig. 7.10(b) is can be seen that the disturbances at 0.2 and 0.8 s are reduced to 0.1 V in amplitude while the one at 0.5 is reduced to 0.5 V in amplitude. This is a large improvement over the simulation shown in Fig. 7.9. It can also be seen on the power drawn from the fuel cell in Fig. 7.10(d) is more consistent because the disturbance has less influence on the DC-voltage. From these simulations it is postulated that this control system will also work for any

other operation. If it can handle relatively fast disturbance steps it can also handle 'softer' disturbances which are more likely to occur during actual operation. The first result of this solution is that any reasonable motor operation profile can be used and the super capacitor will be able to keep the DC-bus stable. The second result is that the fuel cell mean power can be adjusted at any time because the DC-bus voltage can be controlled.

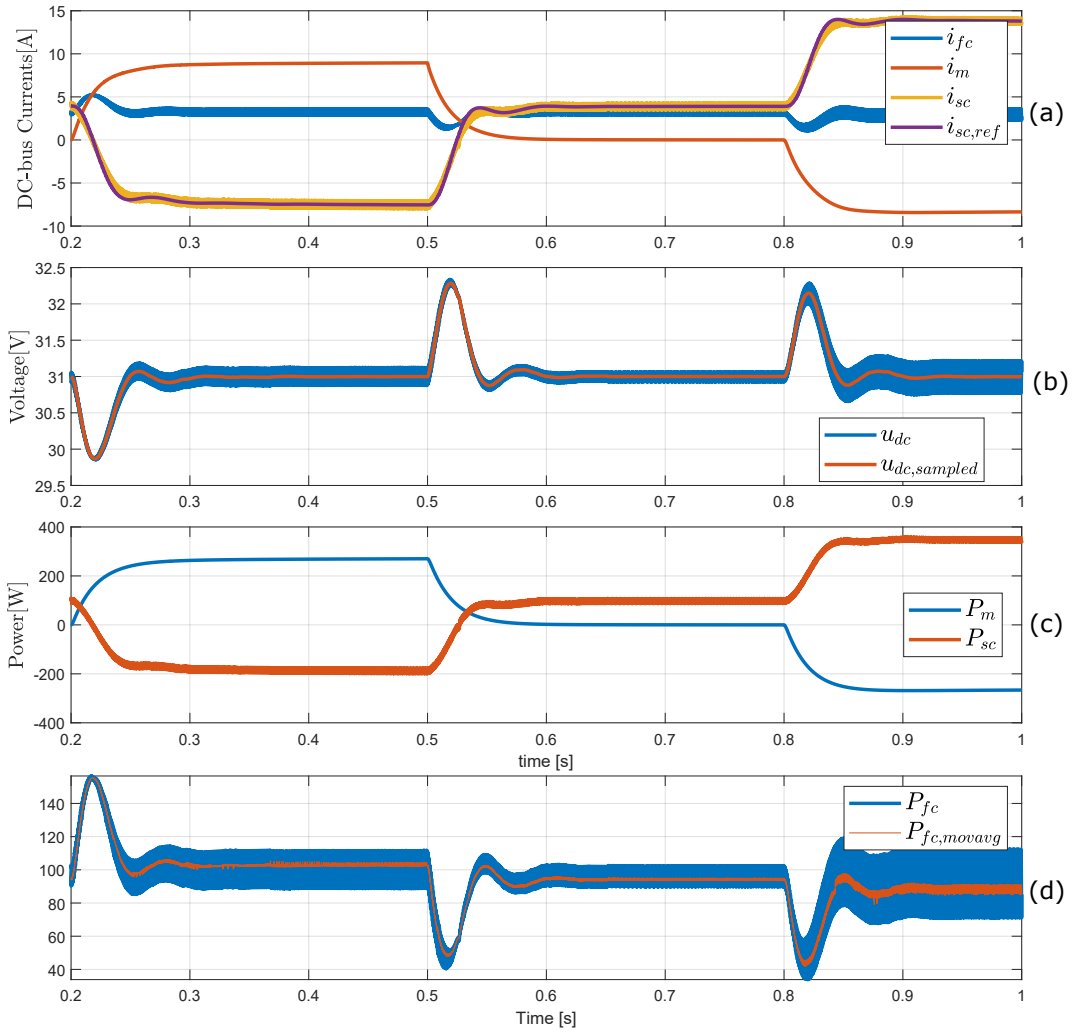


Figure 7.9: DC-bus simulation **without** disturbance feedforward, refer to Fig. 7.8 for Plecs and Fig. 7.3 for control schematic. (a) DC-bus node currents. (b) DC-bus voltage. (c) Motor and SCC power. (d) Fuel cell power, continuous and filtered.

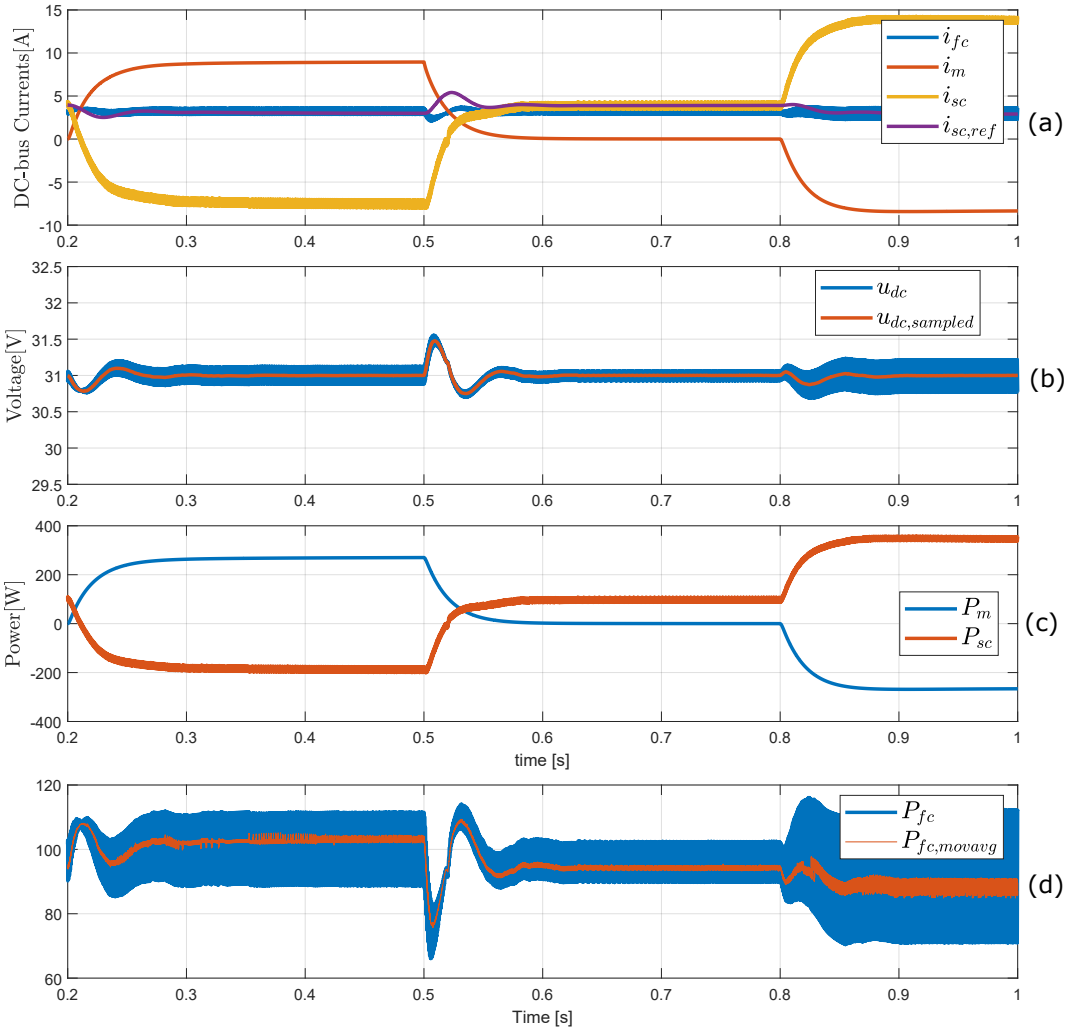


Figure 7.10: DC-bus simulation **with** disturbance feedforward, refer to Fig. 7.8 for Plecs and Fig. 7.3 for control schematic. (a) DC-bus node currents. (b) DC-bus voltage. (c) Motor and SCC power. (d) Fuel cell power, continuous and filtered.

Chapter 8

Conclusion

In this study a comprehensible power control solution for a fuel cell electric vehicle, with super capacitor parallel storage unit, is designed. The power control algorithm controls the mean power output of the fuel cell, by controlling the DC-bus voltage which is linked to the voltage of the fuel cell stack. Controlling the voltage of the fuel cell means to control the power output by extension. The DC-bus voltage is perturbed by a PMSM motor, which can either be drawing or supplying power to the DC-bus. A Super Capacitor Converter is used to control the DC-bus voltage, while rejecting disturbances caused by the motor. A motor DC-bus current draw estimation is used for disturbance feedforward rejection, improving the disturbance rejection capabilities of the system. Without feedforward disturbance rejection a motor current step of 9 A equivalent to 270 W of motor power, causes a voltage ripple of 1.3 V on the DC-bus. With feedforward disturbance rejection the same motor current step causes a ripple of 0.5 V and 0.1 V, greatly improving the disturbance rejection capability of the system. It is concluded that using this control structure it is possible to inject any pre-filtered motor reference and the DC-bus voltage controller will be able to handle it. By extension the mean output power of the fuel cell can be controlled under any operation conditions imposed by the motor, as long as the super capacitor bank SOC is within operational values. There remain two major tasks before the implementation of super capacitors in the Ecoracer is finished. The first is to experimentally validate all the models and test the designed controllers. The second is to run an efficiency optimization algorithm for the motor operation and test this in a live experiment.

Chapter 9

Further work

9.1 Planned experiments

The focus of this study was initially heavily test based, as such experiments were scheduled to be performed. The scheduled experiments are listed below and they need to be conducted before final implementation is possible. Some of the experiments are for verifying data and estimations while others are to verify the designed controllers in this study.

Test current steps for the super capacitor converter on a resistive load check if the discrete controller works as intended and the sample timing is correct. After the controller is tested for resistive load a capacitive load can be swapped in, with updated controller values. The voltage source in the lab is bi-directional so positive and negative current steps can be checked when the super capacitor voltage is within operating range.

Run FOC on motor and step $i_{q,ref}$ while measuring i_q, i_d, u_q, u_d and $i_{m,dc}$. i_d should converge to zero, and i_q should inhabit a first order response to the reference value. i_m calculated from i_q, i_d, u_q, u_d in the simulation and the measured value should be close after taking the efficiency of the inverter into account.

Measurement of motor efficiency as a function of torque and rotational speed. Testing the motor efficiency is done by using a second BDC motor as a torque load by drawing power from it with an electronic load. Speed control is implemented on the VESC controller. The procedure is; set the speed, step the torque load a multitude of times, take a note of i_m, u_{dc} and motor torque (read from torque transducer) for input and output power, change the speed, repeat. Do this for as many operation points as possible and an efficiency surface can be fitted to the operation points. This was done in this study, however the result was unsatisfactory so it was scheduled to be repeated but never was before the lockdown.

Measure the polarisation curve of the Fuel cell. The data for the fuel cell was acquired second hand and it was not very accurate. If the temperature of the fuel

cell was controlled then a more distinct polarisation curve may be obtained.
Test the DC-bus voltage control. If everything else is verified then the entire system can be tested. A programmable voltage source can be used to emulate the fuel cell by controlling the voltage with the measured current. The motor will be acting as the disturbance to the DC-bus supplying or drawing power and the super capacitor converters role is to control the DC-bus voltage and in extension the emulated fuel cell. If the results from this experiment is satisfactory the next thing would be to work on the motor operation profile. It is proposed that optimal scheduling is used for this purpose.

9.2 Optimal scheduling

The result of the power control solution, in this study, is that any motor operation profile could essentially be used and the fuel cell would still be delivering close to the set mean power. Assuming the super capacitor converter is ideal or close to, the remaining task is to optimise how the motor is driven. In Fig. 9.1 the motor efficiency isocline from [5] is shown. The isocline is from the old motor, but the new motor is similar in the shape. The first optimization variable is to choose the motor to wheel gearing, this will determine how much the car accelerates with a given torque. The next optimization variable is to define a stochastic set of motor current commands ($i_{q,ref}$), that will directly influence the acceleration of the car and thereby the speed. In Fig. (9.2)(a) such a set of motor current commands are shown with the expected resulting speeds in (9.2)(b). The optimization problem can be written as shown in Eq. (9.1) through Eq. (9.6). The optimization goal in (9.1) is to minimise how much energy is used in total during an entire lap. The optimization variables are the set of motor current setpoints and gearing. The first and second constraint, Eq. (9.2) and Eq. (9.3) are constraints that the instantaneous power must not be higher or lower than some value. Eq. (9.4) is a constraint from the race rule set that states that the vehicle must not exceed 40 km/h. Eq. (9.5) is a constraint for the SOC of the super capacitors, they must not overcharge or undercharge. The constraint in Eq. (9.6) is that the vehicle must complete a full lap in a certain amount of time and the last in Eq. (9.7) is that the car must be stopped at the end. This is a sort of brute force method which would likely take a lot of computing power. Yet, a set of motor current set points that satisfy all the constraints while minimising the cost function would be an optimal operation profile. To get a global optimal operation profile requires more work.

$$\min_{i_{q,ref},G} \quad f_{cost} = \int_0^{T_{lap}} P_{losses}(t)dt \tag{9.1}$$

ST.
$$g_1(\tau_m(t), v(t)) = P_m(\tau_m, v(t)) < 400 \quad [\text{W}] \tag{9.2}$$
$$g_2(\tau_m(t), v(t)) = P_m(\tau_m, v(t)) > -200 \quad [\text{W}] \tag{9.3}$$
$$g_3(v(t)) = 0 < v(t) < 40 \quad [\text{km/h}] \tag{9.4}$$
$$g_4(u_{sc}(t)) = 20 < u_{sc}(t) < 27 \quad [\text{V}] \tag{9.5}$$
$$g_5(v(t)) = \int_0^{T_{lap}} v(t)dt > 1420 \quad [\text{m}] \tag{9.6}$$
$$g_6(v(t)) = v(t = T_{lap}) = 0 \tag{9.7}$$

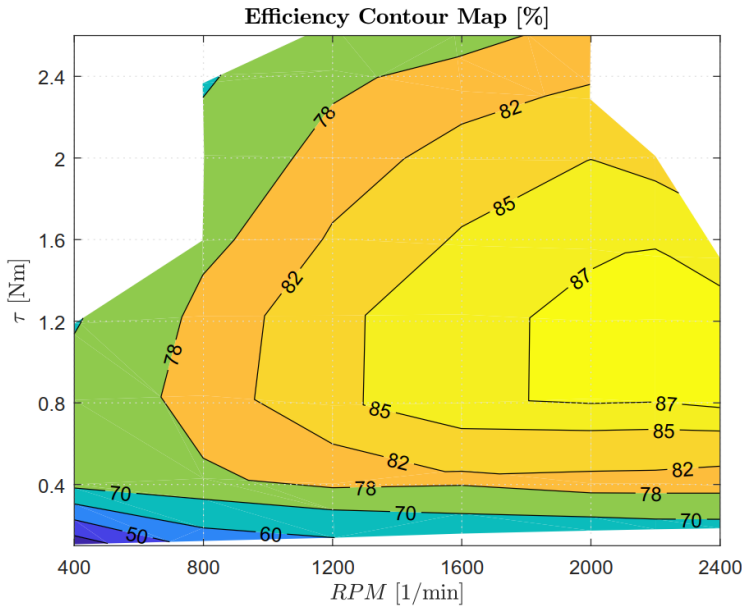


Figure 9.1: Motor efficiency isocline from old motor, taken from [5]

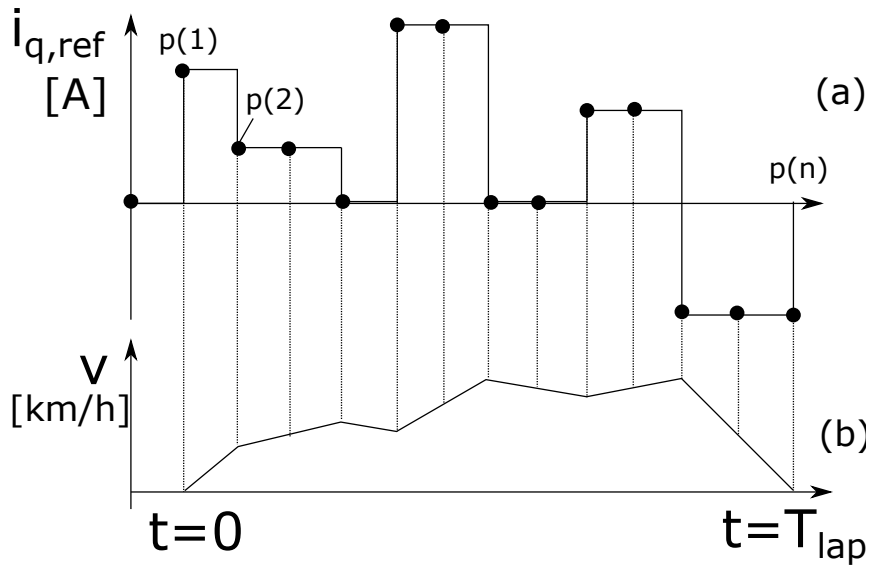


Figure 9.2: Illustration how a set of motor current set points (p(1)..p(n)) can affect the car velocity.

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Appendix A

Motor Parametrisation

In this appendix the unknown motor parameters L_d, L_q, λ_{mpm} and R_s are found. In the dq-reference frame the voltage Equations; Eq. (A.1) and Eq. (A.2) are all that is needed to find the parameters.

$$u_q = R_s i_q + p\lambda_q - \omega_r \lambda_d \tag{A.1}$$
$$u_d = R_s i_d + p\lambda_d + \omega_r \lambda_q \tag{A.2}$$
$$\lambda_q = L_q i_q \tag{A.3}$$
$$\lambda_d = L_d i_d + \lambda_{mpm} \tag{A.4}$$

Three tests are performed to determine these parameters; the first is a simple DC measurement of the resistance, the second is an open-circuit test and the thirds a blocked-rotor test. Similar tests are done in [5].

A.1 Blocked Rotor test

A blocked rotor test is done by injecting a current on the α-axis, which align the d-axis of the rotor with the α-axis of the stator. Then the rotor is locked mechanically so that $\omega_e = 0$ and $\theta_e = 0$. Blocking the rotor results in a cancellation of terms from Eq. (A.1) through Eq. (A.4), the resulting voltage equations can be reviewed in Eq. (A.5) and Eq. (A.6).

$$u_q = R_q i_q + pL_q i_q + \cancelto{0}{\omega_r \lambda_d} \tag{A.5}$$
$$u_d = R_d i_q + pL_d i_d + \cancelto{0}{p\lambda_{mpm}} + \cancelto{0}{\omega_r \lambda_q} \tag{A.6}$$

Where λ_{mpm} is a constant peak value, why it is cancelled out together with the speed terms.

Rearranging Eq. (A.5) and (A.6) and integrating it is possible to find an expression for the flux linkage as shown in Eq. (A.7) and (A.8).

$$\lambda_q = \int u_q - R_q i_q dt \tag{A.7}$$

$$\lambda_d = \int u_d - R_d i_d dt \tag{A.8}$$

Then from Eq. (A.3) and (A.4) it is noticed that the flux linkage is proportional to the d or q current and the corresponding inductance. Plotting the flux against the current shows a linear relationship shown in Fig. A.1. The values of the fitted linear regressions can be seen in table A.1. The average $L_d = 977.1$ uH and $L_q = 2545uH$.

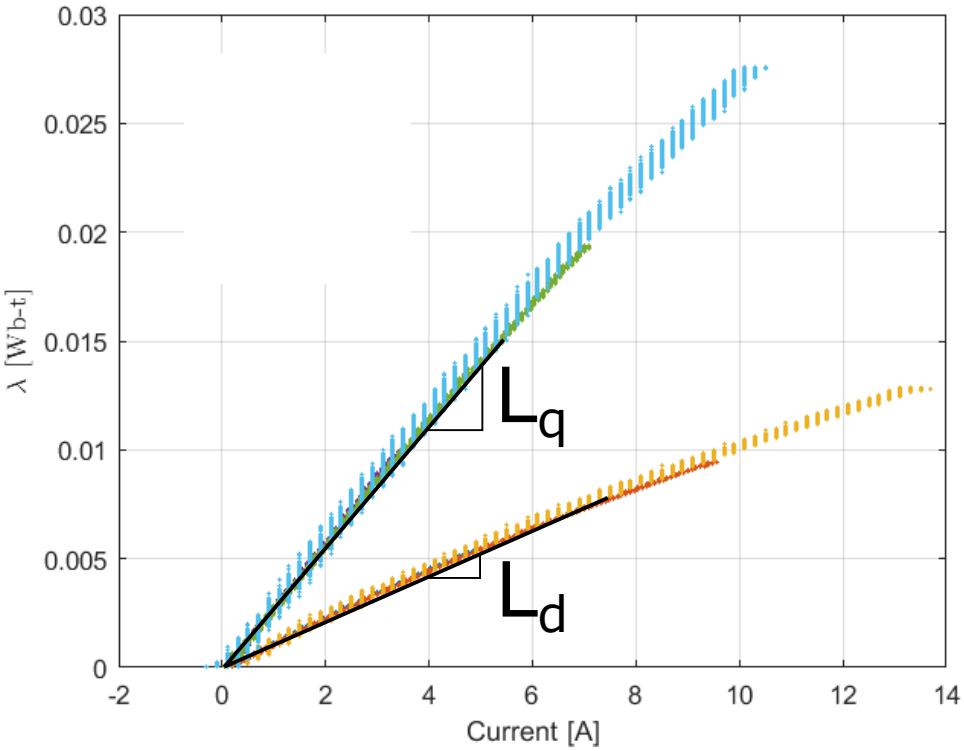


Figure A.1: Blocked rotor test. Calculated flux linkage against current, slope describes inductances

Table A.1: Blocked rotor motor test.

Axis [mH]	Inductance [uH]
α/d-axis (#1)	996.2
α/d-axis (#2)	990.0
α/d-axis (#3)	945.1
β/q-axis (#1)	2363
β/q-axis (#2)	2612
β/q-axis (#3)	2662

A.2 DC-resistance test setup

The DC-resistance of the wires can be measured using a multimeter. Or it can be calculated by using the DC values of the voltage and current through a phase when blocking the rotor. The phase resistance can be derived using test configuration 1 as shown in Eq. (A.9).

$$U_{bc} = 2R_s I_{an} \Leftrightarrow R_s = \frac{U_{bc}}{2I_{an}} = 48.6m\Omega \tag{A.9}$$

Where U_{bc} is the voltage from line-to-line voltage when conducting blocked rotor test on beta axis, ie. stepping the voltage on b to c phase. I_{bn} is the steady state phase current and R_s is the stator resistance.

A.3 Open-circuit test

For the open-circuit test the motor terminals are open-circuited, this means that the phase current is zero and this cancels out terms of the voltage equations. The terms left of the voltage Eq. is shown in Eq. (A.10) and (A.11).

$$u_q = \cancelto{0}{R_q i_q} + \cancelto{0}{pL_q i_q} - \cancelto{0}{\omega_r L_d i_d} \omega_r \lambda_{mpm} \tag{A.10}$$

$$u_d = \cancelto{0}{R_d i_q} + \cancelto{0}{pL_d i_d} + \cancelto{0}{p\lambda_{mpm}} \cancelto{0}{\omega_r L_q i_q} \tag{A.11}$$

What remains is shown in Eq. (A.12). Since λ_{mpm} is a peak value it is only necessary to find the peak value of u_q and the electrical speed to calculate.

$$u_q = -\omega_r \lambda_{mpm} \tag{A.12}$$

The open-circuit test is performed by driving the motor with a brushed DC-motor of which the voltage is adjusted to change the speed. The amplitude of the first fundamental is then found by performing a FFT on the line to line voltage measurement. The first line-to-line voltage measurement is shown on the left of Fig.

A.2 and the single siden amplitude spectrum of this signal following a FFT transform that is shown in the right of Fig. A.2. The fundamental line-to-line voltage from the amplitude spectrum is then converted to a RMS phase voltage and then the permanent magnet flux can be calculated as shown in Eq. (A.13).

$$\lambda_{mpm} = \frac{\sqrt{2}}{\sqrt{3}} V_{ab,1} \omega_r \tag{A.13}$$

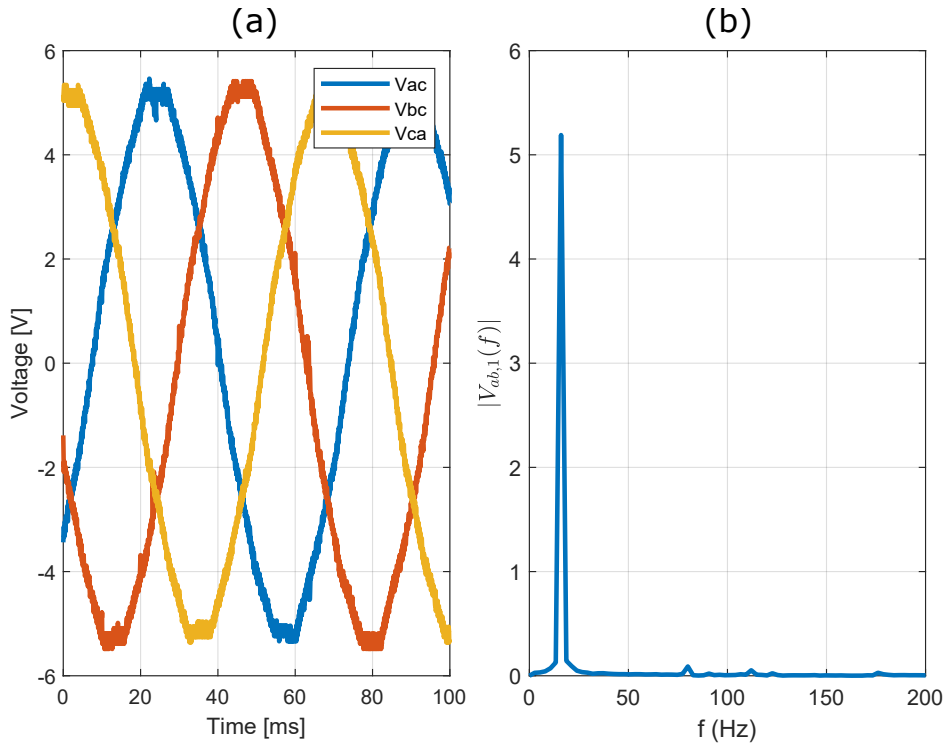


Figure A.2: Open-circuit motor test at 94.25 rad/s. (a) measured line-to-line voltages. (b) Calculated single sided amplitude spectrum of line-to-line voltage V_{ac}.

Repeating this process a few times while varrying the speed with the external motor yields the results shown in Tab. A.2. The mean of the calculated flux linkages is $\lambda_{mpm} = 44.7mWb$.

Table A.2: Open-circuit motor test.

ω_e [rad/s]	$U_{ab,1}$ [V]	λ_{mpm} [mWb]
94.25	5.189	0.0450
188.5	10.27	0.0445
377.0	20.77	0.0450
565.5	30.97	0.0447
754.0	41.21	0.0446

Appendix B

State-averaging, resistive load

The planned testing procedure was to test the converter with a resistive load to make sure it technicalities like the sampling works before connecting the super capacitors. To this end an average model is derived for a resistive load in this chapter. In Fig. B.1 the two modes of the buck converter with a resistive load can be seen. Starting with mode 1, KVL is used to find the inductor dynamics and KCL is used to find the capacitor dynamics, the governing dynamic equations are given in Eq. (B.1) and (B.2)

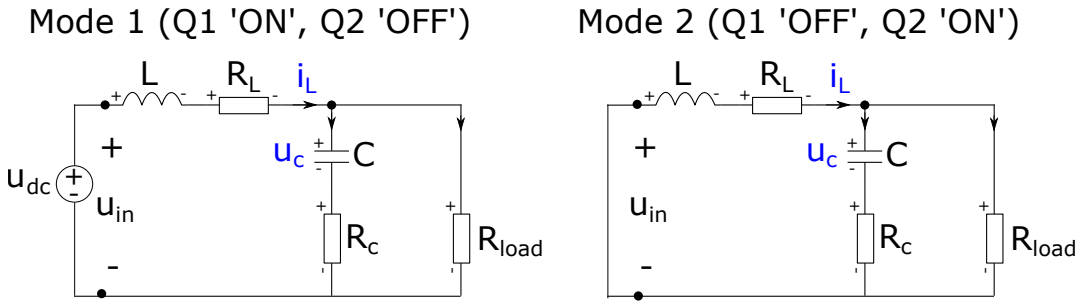


Figure B.1: Buck-synchronous converter, idealised switches with parasitic series resistances for inductor, output side capacitor and resistive load.

$$\frac{di_L}{dt} = \frac{u_{dc}}{L} - \left(\frac{R_{load}R_c}{(R_{load}+R_c)L} + \frac{R_L}{L}\right) i_L + \left(\frac{R_c}{R_{load}+R_c} - \frac{1}{L}\right) u_c \tag{B.1}$$

$$\frac{du_c}{dt} = \frac{R_{load}}{C(R_{load}+R_c)} i_L - \frac{1}{C(R_{load}+R_c)} u_c \tag{B.2}$$

The state space system in Eq. (B.3) are extracted from the dynamic equations in Eq. (B.1) and (B.2).

$$
\begin{aligned}
\dot{\mathbf{x}} &= A_1\mathbf{x} + B_1 u, \quad \mathbf{y} = C_1\mathbf{x} \\
\begin{bmatrix} \dot{i_L} \\ \dot{u_c} \end{bmatrix} &= \begin{bmatrix} -\left(\frac{R_{load}R_c}{(R_{load}+R_c)L} + \frac{R_L}{L}\right) & \frac{R_c}{R_{load}+R_c} - \frac{1}{L} \\ \frac{R_{load}}{C(R_{load}+R_c)} & -\frac{1}{C(R_{load}+R_c)} \end{bmatrix} \begin{bmatrix} i_L \\ u_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} u_{dc} \\
\begin{bmatrix} i_L \\ u_c \end{bmatrix} &= \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_L \\ u_c \end{bmatrix}
\end{aligned} \tag{B.3}
$$

The state matrices are the same for mode 2, with the exception of the input matrix B_2 which is null. So $A_1 = A_2$, $B_2 = [0, \ \ 0]^T$, $C_1 = C_2$.
Summing these two states over their active time will subsequently result in an average state-space model. Over a single switching period the state space averaged equation shown in Eq. (B.4) is true.

$$
\begin{aligned}
\dot{\bar{\mathbf{x}}} &= A_{av}\mathbf{x} + B_{av}\bar{u} \\
\bar{\mathbf{y}} &= C_{av}\bar{\mathbf{x}} \\
A_{av} &= A_1 d_1 + A_2(1-d_1) = A_1 \\
B_{av} &= B_1 d_1 + B_2(1-d_1) = B_1 u_{dc} d_1 \\
C_{av} &= C_1 d_1 + C_2(1-d_1) = C_1 \\
\begin{bmatrix} \dot{\bar{i_L}} \\ \dot{\bar{u_c}} \end{bmatrix} &= \begin{bmatrix} -\left(\frac{R_{load}R_c}{(R_{load}+R_c)L} + \frac{R_L}{L}\right) & \frac{R_c}{R_{load}+R_c} - \frac{1}{L} \\ \frac{R_{load}}{C(R_{load}+R_c)} & -\frac{1}{C(R_{load}+R_c)} \end{bmatrix} \begin{bmatrix} \bar{i_L} \\ \bar{u_c} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} u_{dc} d_1 \\
\begin{bmatrix} \bar{i_L} \\ \bar{u_c} \end{bmatrix} &= \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \bar{i_L} \\ \bar{u_c} \end{bmatrix}
\end{aligned} \tag{B.4}
$$

What is shown in Eq. (B.4) is the average state space system of the synchronous buck, for this to be transformed to a transfer function it needs to be linearised.

B.1 Linearising state-space average model

Linearisation of a state space system is performed by separating each system variable into a steady state value and a small signal perturbation. The linearisation process used here is well documented in [18, p. 1041].

$$\bar{\mathbf{x}} = \mathbf{X} + \tilde{\mathbf{x}} \tag{B.5}$$

$$\bar{u_{dc}} = U_{dc} + \tilde{u_{dc}} \tag{B.6}$$

$$\bar{d_1} = \Delta_1 + \tilde{d_1} \tag{B.7}$$

$$\bar{\mathbf{y}} = \mathbf{Y} + \tilde{\mathbf{y}} \tag{B.8}$$

Substituting Eq. (B.5) through (B.8) into Eq. (B.9) yields a state space Equation shown in (B.10) consisting of steady state and transient terms.

$$\begin{aligned} \dot{\tilde{\mathbf{x}}} &= A_1\mathbf{x} + B_1\tilde{d_1}\tilde{u_{dc}} \\ \bar{\mathbf{y}} &= C_1\bar{\mathbf{x}} \end{aligned} \tag{B.9}$$

$$\begin{aligned} \dot{\tilde{x}} + \cancelto{0}{\dot{\mathbf{X}}} &= A_1(\tilde{\mathbf{x}} + \mathbf{X}) + B_1(U_{dc} + \tilde{u_{dc}})(\Delta_1 + \tilde{d_1}) \\ \mathbf{Y} + \tilde{\mathbf{y}} &= C_1(\tilde{\mathbf{x}} + \mathbf{X}) \end{aligned} \tag{B.10}$$

Factoring steady state and transient terms in Eq. (B.10) and neglecting higher order terms result in Eq. (B.11) for steady state and Eq. (B.12) for small signals.

$$\begin{aligned} 0 &= A_1\mathbf{X} + B_1\Delta_1 U_{dc} \\ \mathbf{Y} &= C_1\mathbf{X} \end{aligned} \tag{B.11}$$

$$\begin{aligned} \dot{\tilde{\mathbf{x}}} &= A_1\tilde{\mathbf{x}} + B_1\Delta_1\tilde{u_{dc}} + B_1 u_{dc}\tilde{d_1} \\ \tilde{\mathbf{y}} &= C_1\tilde{\mathbf{x}} \end{aligned} \tag{B.12}$$

The result is the steady state response shown in Eq. (B.11). The steady state response can be used for feed-forward control, which is often very useful. Eq. (B.12) describe the system response under the influence of small changes. This small signal model is like a super positioning of all system inputs.
By setting one or the other system input to zero in Eq. (B.12) transfer functions can be derived. This is equivalent to regarding the other system input as a disturbance. The resultant transfer functions are shown in Eq. (B.13) for small duty cycle changes and (B.14) for small input voltage changes.

$$\frac{\tilde{\mathbf{y}}(s)}{\tilde{d_1}(s)} = C_1(sI - A_1)^{-1}B_1U_{dc} = [\frac{\tilde{i_L}(s)}{\tilde{d_1}(s)}, \quad \frac{\tilde{u_c}(s)}{\tilde{d_1}(s)}]^T \tag{B.13}$$

$$\frac{\tilde{\mathbf{y}}(s)}{\tilde{u_{dc}}(s)} = C_1(sI - A_1)^{-1}B_1\Delta_1 = [\frac{\tilde{i_L}(s)}{\tilde{u_{dc}}(s)}, \quad \frac{\tilde{u_c}(s)}{\tilde{u_{dc}}(s)}]^T \tag{B.14}$$

Appendix C

Gate drive design considerations

This appendix chapter is about some of the design consideration that were made when designing the super capacitor converter. Due to the circumstances it was not possible to actually test the finished PCB, but these design considerations are still valid, they just need testing.
The gate driver chosen is the LM5104, because it fulfils the voltage requirements, is fast and is designed for synchronous switching operation. In Fig. C.1 the typical application schematic is shown, acquired from its data sheet [22]. The PCB is designed just like shown in the application schematic. VDD, the voltage supply for the gate drive is 12V (recommended 9-14V).

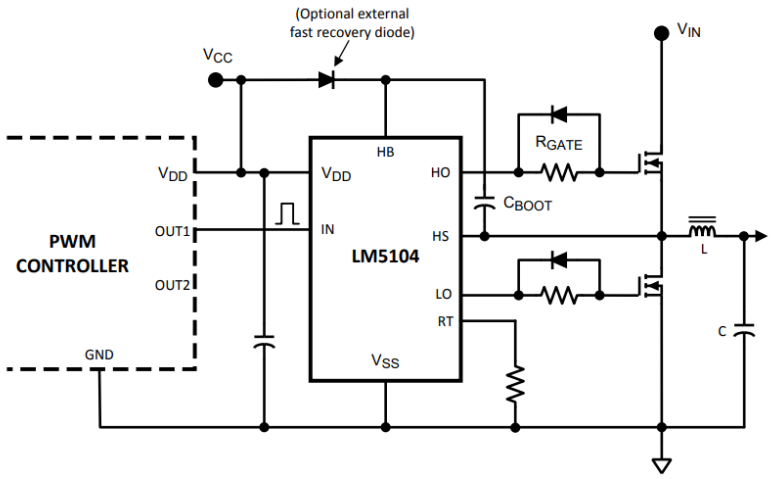


Figure C.1: Typical application diagram of LM5104 synchronous gate driver, from [22].

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	1.0	mΩ
I_D	180	A
Q_{oss}	228	nC
Q_G(0V..10V)	208	nC

Figure C.2: Power transistor IPB010N06N key parameters, from [23].

Dead time

The dead time must be chosen such that it is greater than the turn-off delay of the used MOSFET. [12] In [23], the datasheet for the IPB010N06N Mosfet, the turn-off delay is specified to be 74 ns under similar operating conditions to the ones in this study. The dead time is set to 100 ns, this leaves a small safety margin. If the dead time is too low then there is a risk of short-circuiting the half-bridge. If the resistor Rt=20 kΩ then the dead time will be approximately 100 ns. In Fig. C.3 the principle of the programmable dead time from the LM5104 gate driver is illustrated. [22] In Fig. C.3(c) the gate to source voltages are shown, if a given signal is high then that gate is 'ON' otherwise it is 'OFF'. When a 'HIGH' gate signal is received by the LM5104 gate driver it will wait until the gate voltage falls to $V_{DD}/2$, a propagation delay, after which it will wait T_{DT}=100 ns as specified, before actually turning 'ON' the 'HIGH' gate. So there is a delay on the control input corresponding to $t_p + T_{DT}$, which is in the range of 130 ns. In the simulation only the dead time will be simulated since having gate transients would make the simulation much slower because of the condition number. However this is an interesting point to check in the real implementation.

Bootstrap capacitor

The bootstrap capacitor is needed to drive the MOSFET gates. The capacitance is determined based on the rule of thumb that it must be able to drive the gate of the high-side MOSFET without discharging more than 10%. This means the bootstrap capacitor capacitance must be ten times greater than the gate capacitance. The MOSFET choice is based on a compromise where low parasitic resistance while having a high voltage rating is prioritised, even though this means the gate capacitance increases. More on what gate capacitance and gate resistance does to losses briefly. The key parameters for the chosen MOSFET are shown in table C.2. The gate capacitance can be calculated using the gate reactance (Q_G). [24]

$$C_G = \frac{Q_G}{VDD} = 17.33[nF] \Rightarrow C_{BOOT} > 10 \cdot 17.33[nF] \tag{C.1}$$

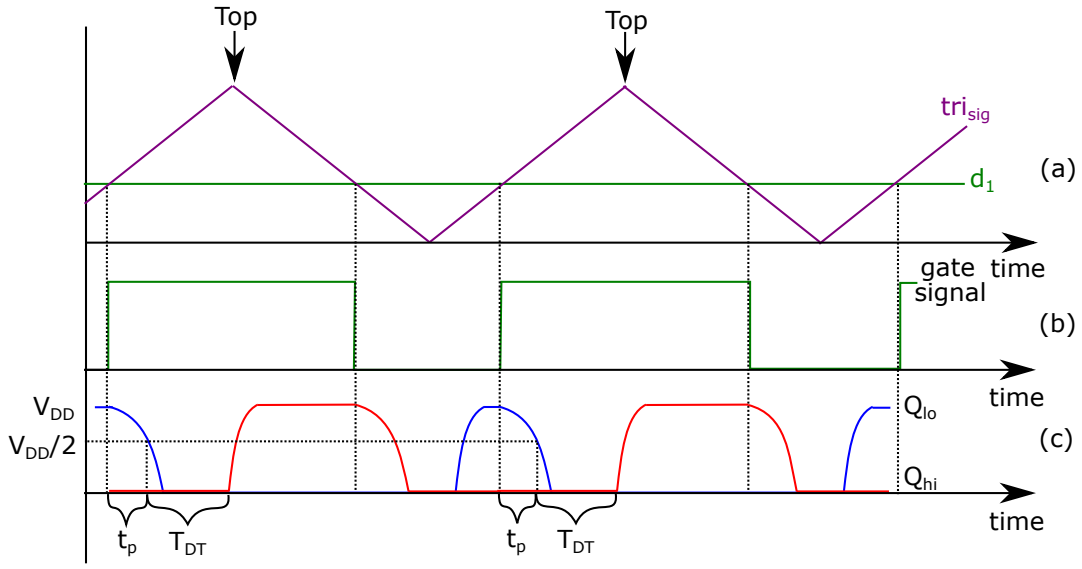


Figure C.3: (a) Dual slope carrier signal and duty cycle. (b) Gate signal sent to LM5104. (c) High (Q_{hi}) and low (Q_{lo}) side gate to source voltages. $V_{DD} = 12$ V. t_p is propagation time from gate signal to gate voltage falls to $V_{DD}/2$. T_{DT} is chosen dead time.

This in turn means the bootstrap capacitor, between VDD and GND in Fig. C.1 must be at least ten times larger than C_{BOOT}. [24]

Bootstrap resistor

A bootstrap resistor R_{BOOT} cab be added in series with the bootstrap capacitor C_{BOOT} in order to reduce the dv/dt charging of the bootstrap capacitor. This may help during start-up, to reduce the stress on components like the external bootstrap diode. An external bootstrap diode is also added in series with the bootstrap resistor and capacitor. This diode will reduce the ringing effects by blocking currents trying to return to VDD after switching the gate.
The diode and resistor must be chosen so that they can handle the initial charging. In Eq. (C.2) a expression for the initial peak current is shown. [24]

$$i_{BOOT,max} = \frac{VDD - V_{fw,diode}}{R_{BOOT}} \tag{C.2}$$

A Schottky diode on-stock with low forward voltage but high voltage rating is the B350A-13-F. It has current rating of 3A, a forward voltage of 0.55V and a voltage rating of 50V. With this current rating $R_{BOOT} > 4$ because this gives a maximum charging current under 3A.

MOSFET losses

In [25] the conduction and switching losses of a buck converter is analysed. In Eq. (C.3) an expression for conduction losses is shown.

$$P_{con} = R_{DS(on)} \frac{V_{OUT}}{V_{IN}} (I_{OUT}^2 + \frac{I_{ripple}^2}{12}) \tag{C.3}$$

Where $R_{DS(on)}$ is the conduction resistance and $\frac{V_{OUT}}{V_{IN}}$ is the DC-bus voltage to the super capacitor bank voltage. I_{OUT} is the steady state output current and I_{ripple} is the ripple content of the current output. [25]
The conduction losses depend of the operation conditions. Assuming a maximum charging power of 250 W at $V_{IN} = 30$ V with $V_{OUT} = 25$ V, then $I_{OUT} = 10$ A and simulations show that the ripple content of the inductor current is $I_{ripple} = 0.3$ A at 20 kHz. $R_{DS(on)} = 1\ m\Omega$. Under these conditions the conduction losses are 0.0833 W.
The gate drive losses on the other hand is a function of gate reactance and switching frequency as shown in Eq. (C.4). [25]

$$P_{GATE} = Q_G VDD f_{sw} \tag{C.4}$$

Where $Q_G = 208nC$, VDD=12 V and $f_{sw} = 20kHz$, which gives 0.0499 W. Adding the conduction and gate drive losses the total MOSFET losses equate to 0.1332 W. Based on these theoretical losses it is apparent that the major losses lie in the inductor and super capacitor, having equivalent series resistances of 79 $m\Omega$ and 6 $m\Omega$ respectively.
Based on the same operating conditions sketched for conduction losses the losses in parasitic resistance of the inductor and super capacitor bank would be around 85 $m\Omega 10^2 A = 8.5$ W. This gives a converter efficiency of $(250 - 8.5)/250 = 96.6\%$. Considering the MOSFET losses as well the efficiency decreases by a further 0.1%. During initial testing it was found that one of the MOSFETs got hot. It is my hypothesis that this was because the bootstrap capacitor capacitance was too low. The bootstrap capacitors capacitance was 22 nF while the gate capacitance was 17nF, this means that the bootstrap capacitor is almost entirely discharged each time it switches. Therefore the gate may not actually be turned fully on which would increase the resistance significantly.

Appendix D

A/D and D/A timing analysis

A very common method of sampling current in inductive circuits with adequately high switching frequency is to sample exactly in the middle of the duty cycle. In Fig. D.1(a) the duty value d1 is compared with a dual-slope carrier wave to create the gate signal shown in Fig. D.1(b). With ideal switches the inductor waveform will be as shown in Fig. D.1(c). The hardware peripheral that generated the gate signal is called the TCC (Timer Compare Channel). The TCC is a peripheral of the C21 chip that counts for every tick of a pre-scaled clock. When the count reaches a set value called PER it resets or in this case with a dual-slope PWM it starts counting down. The TCC peripheral can be configured in such a way that when the counter reaches an overflow of a TOP or BOTTOM value it can generate an interrupt, shown with arrows in Fig. D.1(a). This interrupt is used to trigger an asynchronous A/D conversion which will then sample the signal of interest. If the switches are ideal and the switching frequency is fast enough in relation to the inductance, then the A/D will be triggered exactly in the middle of the current slope, which is also the average current. By triggering the A/D at the correct timing the average of the signal of interest can thus be directly obtained without filtering. If asynchronous A/D is not used, but rather something like synchronous free-running sampling, then the sample-rate has to be approximately 10 times faster than the switching frequency to avoid aliasing. Additionally a filter has to be used to find the average, which will introduce phase lag.
After the A/D triggers and it has finished the conversion from analog to digital it will generate a new interupt. The DMAC peripheral (Direct Memory Access Controller) is then triggered by the finished conversion interrupt and moves the digital signal directly into the memory, this means skipping the CPU, which makes it a very fast operation.
The propagation delay for a sample is the time it takes from the start of sampling to a finished conversion shown in Fig. D.2. If the resolution is 12-bit and the ADC clock is 32 MHz with a pre-scaler of 2 the propagation delay is 0.8 μs as calculated

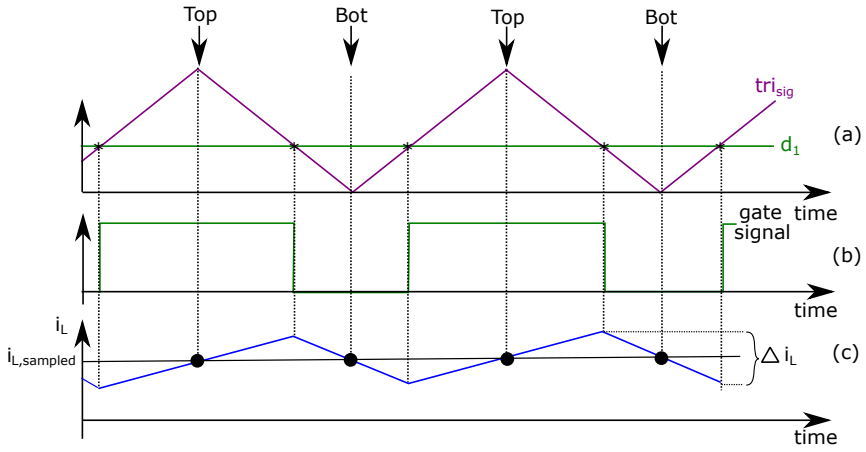


Figure D.1: (a) dual-slope carrier wave and duty cycle. (b) Gate signal. (c) Ideal inductor waveform. Inspiration from [26, p.881]

in Eq. (D.1).

$$PropagationDelay = \frac{1 + Resolution}{f_{ADC}} = \frac{1 + 12 - bit}{32/2Mhz} = 0.8125\mu s \qquad \text{(D.1)}$$

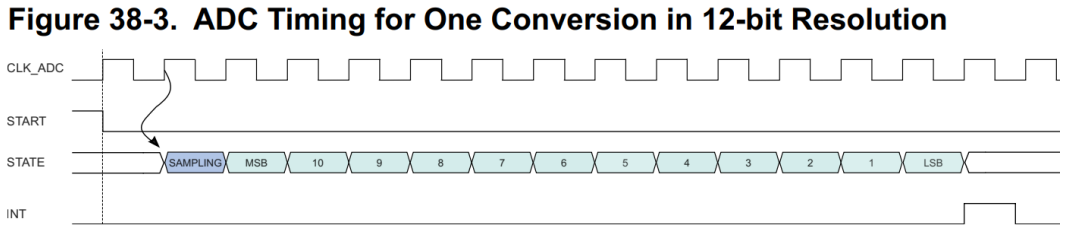


Figure D.2: Single ADC conversion timing, from [26, p.979]

The deterministic control loop of the MCU executes at a frequency of 2kHz. When the control loop executes it will pull the most recent sample and reference from the memory and do the controls. In worst-case scenario the deterministic loop will execute right before a new sample is taken. By this logic the worst case scenario delay from sampling the signal and using it in control is one PER of the PWM.
The D/A conversion is of equal importance as the A/D conversion. The CC0 register can be updated on an interrupt basis, that is, whenever the PWM register is updated the gate signal will be changed a full PWM period later, at the latest. The PWM frequency is 20 kHz, so the longest delay on the control input is 1/20 kHz. Since the PWM is simulated with a carrier wave it will inhibit the same delay as in the real implementation.

Quantization error

Putting the control input delay aside, the control input resolution should also be investigated. The clock used for the PWM is running at 24 Mhz with no pre-scaler using dual-slope PWM. To get 20 kHz switching frequency the period value is set to 600 ticks, this calculation is shown in Eq. (D.2). The PWM register can be set to any integer between 0 to 600 corresponding to a duty cycle between 0 and 1, meaning this is the resolution of the PWM.

$$f_{sw} = \frac{f_{clk}}{PER \cdot 2} \Leftrightarrow PER = \frac{f_{clk}}{f_{sw} \cdot 2} \rightarrow \frac{24e6Hz}{20e3Hz \cdot 2} = 600 \tag{D.2}$$

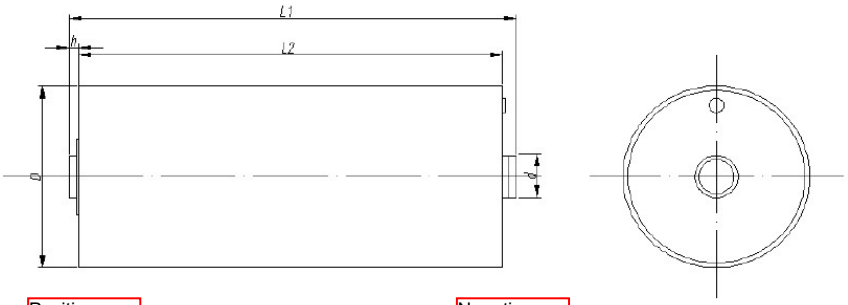
Appendix E

Super capacitor cells data sheet

超级电容器

UCR27V1500

项目	参数					
Nominal Capacitance 额定容量, F	1500					
Rated Voltage 标称电压, V	2.7					
Surge Voltage 浪涌电压，V	2.9					
Final Discharging Voltage 放电终止电压，V	0					
Max. Charging/Discharging Current 最大充/放电电流，A	1100					
DC Internal Resistance (ESR) 直流内阻,mΩ	0.6					
Weight 重量, g	330					
Max. Stored Energy 最大储存能量，KJ	4.89					
Cycle Lifetime 循环寿命, Cycles	≥1,000,000					
Lifetime under High Temperature 高温负荷寿命	容量保持率＞80% 内阻＜160%	65℃，1500h				Capacitance > 80% × Nominal ESR < 160%
Operation Temperature Range 工作温度范围, ℃	-40～+65					
Storage Temperature Range 储存温度范围, ℃	-40～+70					
Size 尺寸, mm	L1	L2	D	d	h	
	88	82	60.5	14	3	



Positive Electrode

Negative Electrode

上海奥威科技开发有限公司
地址：上海市浦东新区张江郭守敬路 188 号
邮编：201203 电话：021-50802888
传真：021-38953296
邮箱：sales@aowei.com

Figure E.1