Advanced Accelerated Test of Power Modules

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Master Thesis

Contents

Chapter 2

Power Cycling Test

For industrial applications, varied load conditions under different thermal environments could induce kinds of stress for the same module. To make sure that the adopted power electronic device could stay reliable under specific conditions within the required lifetime, the relevant tests should be conducted to justify. Generally, there are two types of cycling capability tests: the junction temperature ΔT_j-related power cycling (PC) test, and the solder joint and case temperature ΔT_c-related thermal cycling (TC) test.

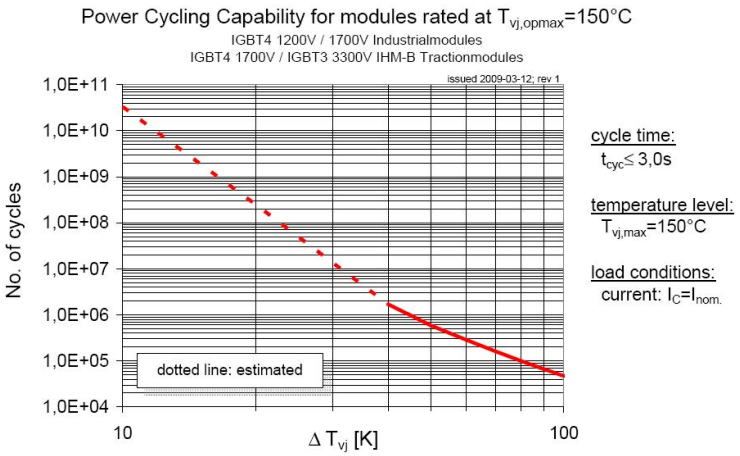


Figure 2.1: IGBT power module Power cycling capability graph, taken from Infineon FP50R06KE3. On the horizontal axis is the variation of the junction temperature between on an off-state of the module. On vertical axis is the number of cycles to failure

In order to test the robustness of the bond wires, the power modules have been subjected to power cycling tests. By having i.e lifetime information derived

from power cycling tests, the robustness can be evaluated quantitatively. Examples shown as in Fig 2.1. To generate such curves, the DUT (device under test) will be tested till its failure. In this chapter, basic physical and theoretical background will be reviewed regarding the power cycling test.

2.1 Prerequisites

The test approach chosen was to keep current and cooling constant during the experiment. Consequently, as the modules are aging, both, chip and baseplate temperature increase over time. In the first few minutes (first hundreds of seconds) the module is heating up. After this phase, the temperature more or less stabilizes for some time. The temperatures during this stable time range are used for the lifetime estimations. At a certain point in time, significant aging can be observed, leading to a significant increase in the case and junction temperature.

Several definitions regarding the power cycling test should be clarified before further explanation:

- Definition of T_j

The junction temperature T_j is the temperature of the semiconductor junction region, which can only be determined by indirect calculation or measurements like small current injecting method.

- Definition of T_{jmax}

The maximum junction temperature is the maximum allowed value for the device to be reached during the thermal cycles during the test. Higher the maximum junction temperature, the higher the stress could occur on the module, which will decrease the number of cycles to failure.

- Definition of t_{on}

The turn-on time is the period during which the device will be in conducting mode and power losses generated, with a steady junction temperature increase. The longer the turn-on time, the higher the temperature increased, and the derivative stress to the module, which will also decrease the number of cycles to failure. The typical t_{on} time could be set from milliseconds to a seconds range.

- Definition of t_{off}

The turn-off time is the period without current conducting, for heat dissipation in power module. The t_{off} can be adjusted so that the T_j will decrease to a certain level to achieve the desired ΔT_j. The typical t_{off} time could be set from milliseconds to a seconds range.

- Definition of t_{cyc}

The time t_{cyc} is the period of one power cycle, which is composed of t_{on} and t_{off}. The typical t_{cyc} time could be set from milliseconds to a seconds range.

- Definition of D

D, or duty cycle (%), is the t_{on} over t_{cyc} ratio, which can be adjusted to achieve the desired ΔT_j.

Obviously, each set of ΔT_j and T_{jmax} will result in different lifetime expectations. During accelerated testing, the power module under test is stressed actively by injecting a constant current into the device, which is turned off after a certain t_{on}. During the device heats up and cools down during a period t_{off} at which no current is injected. Often the duty cycle D of such pulses is chosen to e 0.5 with a frequency in the range of few Hz. The power losses P dissipated in the chip is given by the product of collector-emitter I and collector-emitter voltage V_{ce}.

$$P = I \cdot V_{CE} \tag{2.1}$$

The temperature of the chip increases over time t due to the Joule heating during the current pulse, according to its thermal impedance Z_{th}, which will be discussed in the next section.

$$\Delta T_j = Z_{th(t)} \cdot P \tag{2.2}$$

If the length of current pulse is long enough, temperature reaches steady state, temperature rise can be calculated based on Eq.(2.3).

$$\Delta T_j = R_{th} \cdot P \tag{2.3}$$

For short pulses (below 1s) the case temperature T_c (measured with the built-in NTC resistor of the modules or embedded thermocouple) does not vary significantly.

2.2 Thermal resistance determination

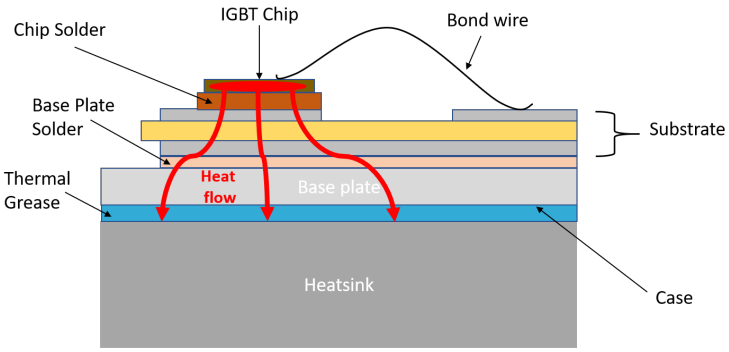


Figure 2.2: Heat generation in IGBT modules

In IGBT modules, the switching and conducting loss is the heat source generated in chips. From the chip, generated heat will be dissipated through multiple layers to the heat sink, as shown in Fig 2.2. The heat flow path is decided by the thermal resistance, which is mot a material property, but very dependent on the specific device or structure.

To compute the ΔT_j in Eq. (2.3) the thermal resistance has to be known. In practice, both the temperature and power loss can be experimentally measured. By heating up the chip till the thermal equilibrium state and then turn to off state to let it cool down, a cooling down curve can be extracted, which contains the information of thermal resistance[3]. While at the same time, reading the value directly from the data-sheet can be another way. The IGBT module manufacturer provides a thermal impedance Z_{th} graph (Fig2.4) which allows us to derive the effective thermal resistance for a given duty cycle and switching frequency.

The thermal resistance is usually given and calculated according to Eq.(2.4). In the shown graph, thermal impedance is given from IGBT chip to the case of the power module.

$$Z_{t_{hjc}} = \frac{T_j - T_{case}}{P} \tag{2.4}$$

With T_j = junction temperature; T_{case} = case temperature; P = power loss / heat flow rate between two points.

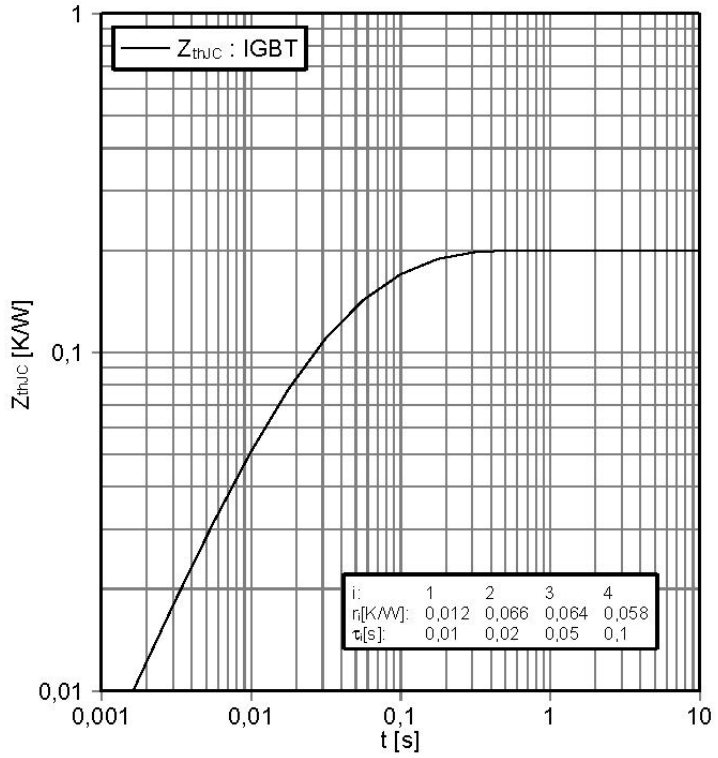


Figure 2.3: Transient thermal impedance (Infineon FP50R06KE3)

With the given fitting values in the graph, a fourth order Foster thermal model can be built to represent the heat transfer through the power module.

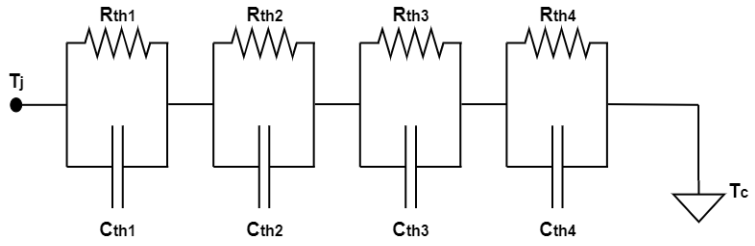


Figure 2.4: Foster Model of Infineon FP50R06KE3, with its partial thermal resistances and its corresponding thermal capacitances.

As long as the Foster model or the fitting function is clear, by assuming a certain temperature value of the baseplate (T_c) and the possible power loss, the highest temperature (T_j) can be calculated through the function.

2.3 On-state resistance determination

It is of vital importance to know the on-state resistance of the IGBT module as a function of time when performing the power cycling test, in order to know the load current at the beginning. Since the suppliers' data sheet usually provides only a few data points, sometimes it is just not sufficient.

Also for the later FE simulation, to simulate the conducting performance of the IGBT chip, silicon's temperature-dependent electrical conductivity is required, which is also related to the on-state resistance of the power module. For details of this part will be explained in the next chapter.

Hence, measurements should be performed before the power cycling test in order to study the temperature dependency of the on-state resistance.

2.4 Test control strategy

The control strategy applied to the power cycling test could have an important influence on the final lifetime of the module under repeated temperature swings. According to the study of [4], the corresponding lifetime results can vary by a factor of 3 when different control strategies are used.

Four different control strategies with detailed explanations are shown as below:

- t_{on}=const. and t_{off}=const.

This control strategy keeps the t_{on} and t_{off} constant throughout the test, as no compensation on the degradation effects, the temperature swing will increase continuously due to the reason of decreased thermal impedance. By the end of the power cycling test (power module failed), dissipated power will increase.

- ΔT_c=const.

This control strategy will keep the case temperature swing constant by adjusting the t_{on} and t_{off} times separately. Power dissipation will increase due to degradation and on- and off- time will decrease.

- P_V=const.

This control strategy requires constant on- and off- time together with the constant power losses. Temperature swing will increase, which lead to a change of the gate voltage, gate voltage will increase to guarantee a constant power loss.

- ΔT_j=const.

This control strategy will keep the junction temperature constant, till the end of life, which will lead to a large decrease of on-time at the end compared with the initial value, indicates that degradation effects being compensated, further with the result of quite prolonged lifetime. Worth mentioning, at the final phase of the cycling test, when on-time has been reduced to mS-scale and can't be shortened further, the temperature swing control will fail.

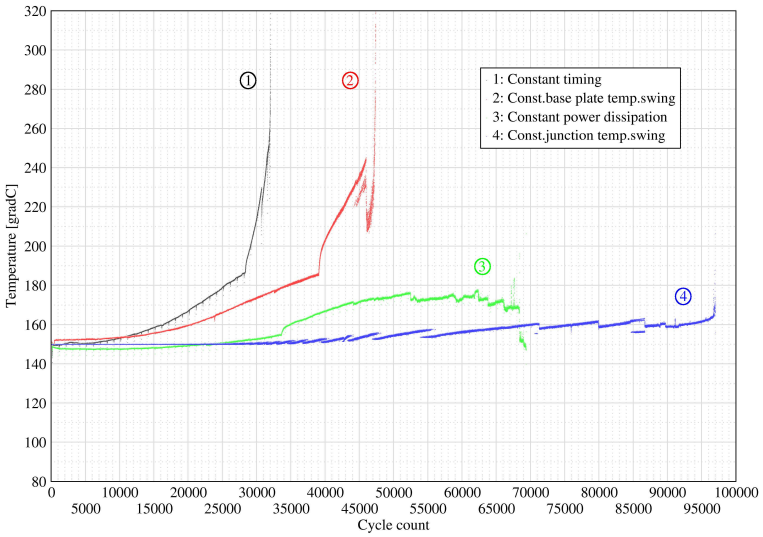


Figure 2.5: Evolution of maximum junction temperature for all four different control strategies during PC. Taken from [4]

In Fig 2.5, the evolution of the maximum junction temperature adopted with four varied control strategies during the power cycling test are presented. Also from this figure the number of cycles to failure is also revealed.

From the above-presented power cycling test result, the conclusion has been drawn that the constant timing control is the harshest control strategy as there has no compensation for the degradation effects, and derives the shortest lifetime. The second harsh control strategy is the constant base plate temperature swing control due to the fact that it ignores the cooling environment change. Next comes with the constant power dissipation, it eliminates the increasing power loss caused by thermal impedance increase (degradation) or V_{ce} increase (bond wire failure). The least hard control strategy with the highest number of cycles to failure is the constant junction temperature control, for the reason of reduced stress and its ignoring of device degradation, this strategy could lead to three times longer lifetime compared to the constant timing control [4].

2.5 Failure criteria for wire bond failures

During the power cycling, different parameters can be set as good failure precursors, shown as below.

- R_{th} increased significantly (around 20% - 30%)
- On-state voltage increase of 5%-10%, as observed in fast power cycling

2.6 Qualification of power cycling test

As the main purpose of running the power cycling tests is to find out the lifetime of the power module used for dedicated applications, it is important to be aware of the possible parameters or ways of "influencing" the lifetime derived from the PC test.

In the earlier days temperature swing has been considered as the only parameter relevant to lifetime. In [5] the first time it has been proposed that the medium temperature if the temperature swing could also impact the result of lifetime. In [6] more parameters have been confirmed to have impacts on the number of cycles to failure: load pulse duration, the bond wire diameter, bond wire/chip interconnection current density, and the chip's voltage blocking capability.

The other ways of "influencing" or "improving" the number of cycles to failure can also involve:

- raise the failure criterion (choose the larger value in section 2.5)
- use lower temperature levels for T_{max}.
- choose the constant junction temperature swing control strategy.
- reduce the stress on bond wire connections by partly generating the heat by switching losses. As the consequence, with the temperature swing, lower currents will be applied, thus lower stress on the bond wires.

Thus it is always necessary to clarify the conditions, applied failure criteria, and control strategy, etc, to evaluate the real lifetime rather than simply trusting the depicted high number of cycles to failure on the datasheet.

2.7 Lifetime models

As mentioned before, in general, the accelerated stress tests are performed to estimate and determine in advance the lifetime of power modules. Due to the fact that the relevant failure mechanisms are thermal or temperature related (bond wire lift-off and solder failure), the thermal modelling should been seen as the core part of the lifetime prediction. In another way, the main principle of lifetime modeling is based on the number of cycles to failure, N_f, which is related to the corresponding temperature profile in the conducted PC or Tc tests.

There are mainly two types of lifetime modelling approaches: empirical lifetime models and physics-based lifetime models[7].

2.7.1 Empirical lifetime model

By having large data sets from power cycling tests based on years experience, empirical models can be deduced. The empirical lifetime models express the lifetime in terms of number of cycles to failure, N_f. All the N_f dependent parameters such as temperature swing, media temperature of the temperature swing, load current period, chip's voltage blocking capability, etc, are described in the empirical lifetime models.

For instance, since 1999 the Coffin-Mansion-Arrhenius model became popular to determine the lifetime for standard power modules through the LESIT program[8][9]. In which the different failure mechanisms were not distinguished.

$$N_F = A \cdot \Delta T_j^{\alpha} \cdot exp(\frac{E_a}{k_b \cdot T_m}) \tag{2.5}$$

where k_b =1.380 $\cdot 10^{-23}$ J/K. According to Coffin and Mansion the expected number of cycles to failure N_f is proportional to the temperature variation Δ T_j. Further, through the exponential Arrhenius factor, the dependency of the activation energy E_a = 9.89 $\cdot 10^{-20}$ J is included with respect to the median junction temperature T_m. This leaves the parameter A and α to be retrieved via fitting from the experimentally gained data.

Many studies on the empirical lifetime model files have been done and some approaches could already separate the failure modes and build up the individual empirical lifetime model [10]. By separating the failure modes, it helped to make more accurate lifetime predictions based on experiences.

2.7.2 Physics based lifetime model

Different from empirical lifetime model, the physics based lifetime modeling requires knowledge of failure and deformation mechanisms, so that the stress and strain evolution is modeled and directly correlated to the number of cycles to failure, N_f.

In practice, the direct measurements of stress and strain in the power modules can be quite tricky, for some parts, this could be done by using the high resolution measuring methods like infrared and scanning electron microscopy, which is neither easy-to-use nor cheap. And for some locations like in the interconnection of bond wire and IGBT chip, which is not reachable for direct measurement. Another way could be adopted by using the stress-strain simulation via computational mechanics,e.g. Finite Element Simulation (FEM). However, the physics based modelling by FEM requires detailed knowledge of material and geometry details which are not easy to get access to. One alternative for FEM has been mentioned in [7], which is based on a numerical approach.

One example of the physics-based lifetime modelling approach is the work done by O.Schilling et al. in [11]. The physics-based lifetime model of which mainly focus on the failure of Al bond wires.

Chapter 4

Results and Discussion

4.1 Mesh Refinement Study

FEM is based on the discretization of the geometry into small units called mesh elements. The finite element mesh serves mainly two purposes: to represent the solution field and the geometry.

If more mesh elements are used, this could lead to a more accurate approximation and solution. However, at the same time, it also means that consuming longer solution time and more memory for the hardware is required. So a big part of the work is to do the trade-off and end up with a mesh that is fine enough to resolve the geometry and solution field while at the same time not running out of the memory.

In terms of numerical stability, the mesh should result in a well-conditioned stiffness matrix, which largely depends on the size and shape of the mesh elements.

In the process of growing element size, elements of poor quality may be created, and that's when it might be a good idea to take a look at the Mesh Statistics window, which could give a quick overview of the mesh. As the quality of the mesh elements is a good indication. Minimum and average quality also presented. It also gives the histogram plot of element quality to give a quick overview of the distribution of elements. The histogram in the Mesh Statistics window will give us a visual of the quality of the mesh, which can be a quick way to see if we need to change the overall mesh sizes in some way.

For all element quality results, a quality of 1 is the best possible and it indicates an optimal element in the chosen quality measure. At the other end of the interval, 0 represents a degenerated element [14]. There are no absolute numbers to present for what the quality should be, as different physics and solvers may have different

mesh quality requirement.

Shown as Fig4.1, on the bond wire/silicon chip interface, by adopting the free triangular mesh shape and define the mesh size to be extremely fine, an element quality of 0.854 has been reached.

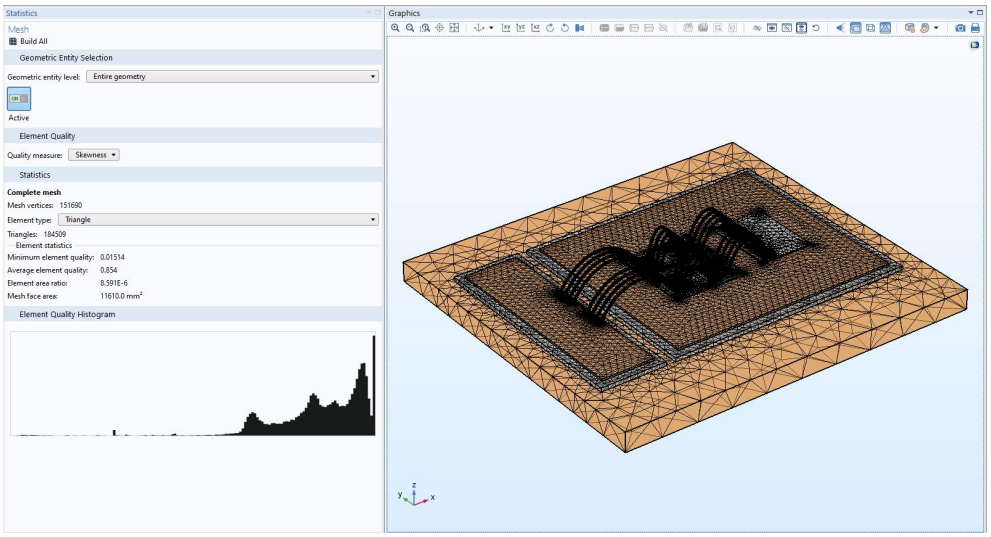
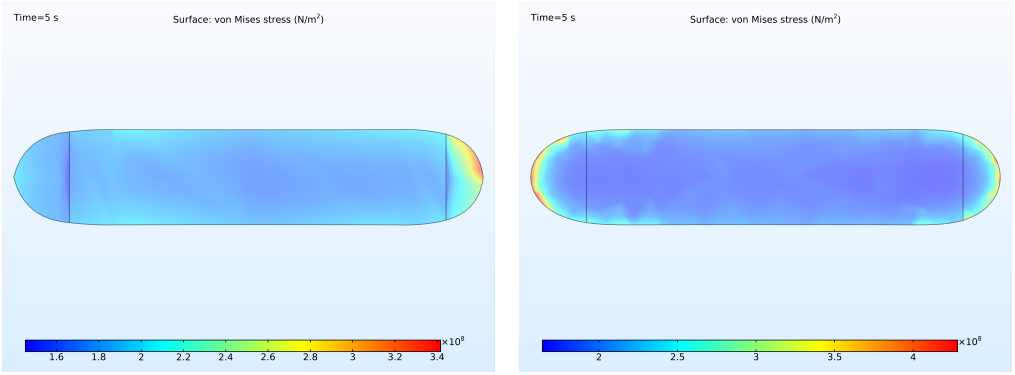


Figure 4.1: Mesh statistics and the associated mesh used in the simulation

As it has been mentioned before, it is of vital importance to know which part of the geometry could be set to have low-quality elements and where the mesh size should be changed. In some cases, a couple of low-quality elements may be okay if they are located in a part of the model with less importance, while in other cases, one low-quality element may lead to convergence problems.

To work out the best mesh setting for the whole geometry, a step-by-step strategy has been adopted by starting up with the most concerning part of the simulation, which in our case is the interconnection part. Then comes to the bond wire part which is secondary important as its displacement is in research interest. Also due to the fact that the bond wire is directly related to the interface. Lastly, the remaining geometric entity mesh quality is considered.

By setting the mesh individually for each part of the geometry, a group of data sets at each mesh size has been generated and ready for comparison. Show in Fig 4.2, the von Mises Stress distribution on the interface has been chosen as the indicator of the mesh quality influence. One set to be coarser while another set to be extremely fine. By having the initial setting in other aspects, the difference of the result seems to be dramatic.



(a) coarser (b) extremely fine

Figure 4.2: Stress distribution result with different mesh sizes

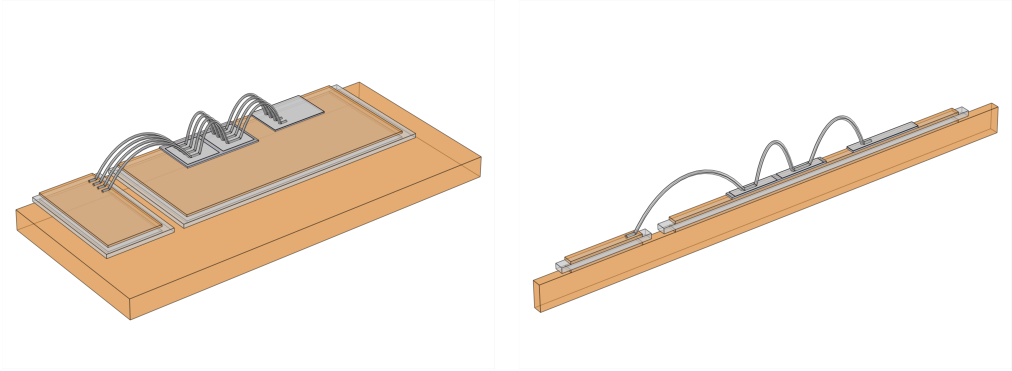
The main weak point for the specific load conditions and module type can be found at the edge and corners of the interface in Fig4.2 (b), while in another result, weak points are only shown in one side of the interface and the stress region is comparatively smaller, due to the coarser mesh setting.

4.2 Sub-model technique

As mentioned before, the computational demand of the FE simulations mainly comes from the mesh density and simulation time duration. When mesh density is high and simulation has to run for a relatively long period of time, ways must be figured out to reduce the simulation load and shorten the completion time.

In FE simulations, for many cases, modeling a large structure in order to properly prescribe the boundary conditions is required. However, the critical part may be local and occupy only a small region of the model. For many different publications, the sub-model technique has been proven to be useful, especially in microelectronic applications[15] [16] [17].

The usage of the sub-model technique for the IGBT power module under power cycling conditions is evaluated in this thesis. For the comparison, two sub-models were generated. One used a half symmetrical structure, while another one with only one bond wire left on the module as the bond wire being the most critical part of the power cycling test, shown in Fig4.3



(a) Half geometry sub-model (b) One bondwire sub-model

Figure 4.3: IGBT sub-model

In the sub-modeling technique, the first step will be to analyze the behavior of the whole model. With well-tuned mesh and applied boundary conditions and loads, some results like temperature, displacement, etc, those globally accurate results, can be calculated. While at the same time, some derivatives such as strains, may not be accurate enough locally. And that's when the sub-model should put into application. Cut the critical part out from the global geometry to generate the sub-model. In case the results of the global model didn't give an accurate presentation, the cut of the sub-model should be sufficiently far away from the critical points. As shown in Fig4.4, the right side of the IGBT module has been cut out align the symmetrical line and the purple color in the sub-model denotes the interface that cut the global model.

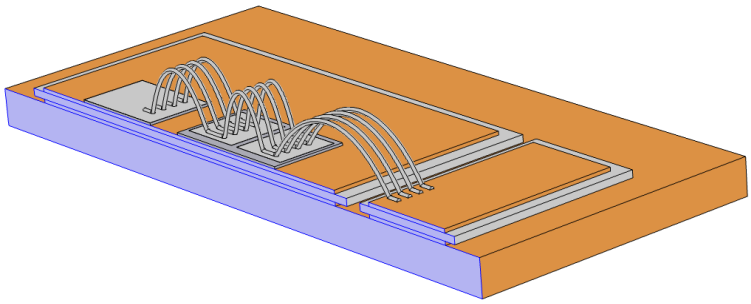


Figure 4.4: Boundary conditions of the sub-model

The results of the global model are prescribed to the sub-model by specifying boundary conditions with field variables that are applied to the cutting interfaces. For our specific case, the purple-colored interface are applied with the below-listed

boundary condition due to the fact that the sub-model is strictly the half symmetrical part of the global model:

- Solid Mechanics: Fixed Constraint
- Heat Transfer in Solids: Thermal insulation

Since the sub-model is a small part of the full model, a finer mesh can be adopted, making it possible to receive a higher resolution of the critical part. Finally, the sub-model is resolved for the equivalent load cases as the global model, to work out the desired result.

For the specific case, the global model consists of 33095 mesh elements, and the computational time was 9h 31min 8s, while the sub-model with a fine mesh consists of 25653 mesh elements, the computational time is much shorter (3h 37min 2s) under the same boundary conditions and loads, meanwhile, more accurate results are received in the critical part. In the comparison between von Mises stresses on the interface in a global model and a sub-model. The global model underestimates with about 20%.

The simulation shows that the sub-model can be useful for the specific model, which is used for the IGBT module under power cycling conditions. It is possible to reduce the computing time and hard disk space demand.

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