Design and Performance Analysis of a High-Power-Density PFC Converter

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Abstract:

With the global power consumption accelerated lately, it is becoming more and more relevant to find efficient power supplies. The inherent advantages of power factor correction over other converters are its high power factor and low input current harmonic distortion. Interleaving techniques present several advantages: low input current ripple, improved power handling capabilities at greater than 90% efficiency and faster transient response to load changes. A study on the effect upon EMI filter and optimization has to be considered under such operating conditions. In this project, the focus is on the design and optimization of an interleaved PFC converter using Dual In-Line Intelligent Power Modules. Different current operation modes (CCM, DCM and QCM) are investigated in order to analyze its influence on PFC converter performance withthe goal of optimizing the EMI filter size and improving the power density of a 1 kW single-phase 2-channel interleaved PFC boost converter.

Preface

This report has been developed as part of the Master's Thesis of project group PED4-1044 during the 4^{th} semester of MsC in Energy Engineering in the specialisation of Power Electronics and Drives at Aalborg University. The analysis and design of PFC boost converter focused in optimizing the EMI filter performance by implementing different modulation and interleaving techniques is described in this project. Literature references are included according to IEEE standard. LaTeX is used for documenting the project work and simulations are carried out in *PLECS* and *MATLAB*. The hardware prototyping of the PFC converter is developed in *Altium Designer*.

We would like to thank our supervisors Pooya Davari and Francesco Iannuzzo for their support and valuable input throughout the entire semester which has provided us help and knowledge to succesfully develop this project. We would also like to thank our couples, family and friends for being always by our side giving us support when we most needed.

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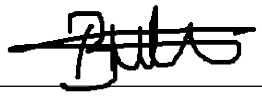

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Summary

In recent years, the demand for high power density converters in motor and household applications has been in constant increase. Power factor correction boost converter is predominating among all AC-DC power supplies. However, the applications in which is implemented, demand for high-power density, mainly due to available space and cost. Interleaved Boost PFC, on the other hand, has proven the ability in increasing PFC power densities, reducing the overall volume of the design. Moreover, manufacturers propose Dual-in-line Intelligent Power Modules (DIPIPM), in downsized packages in order to further reduce the design.

In this project, the main emphasis is put on the design of 1kW interleaved PFC converter using DIPPFC module from *Mitsubishi*™. Investigation under different current modulation modes and the use of these to reduce the volume of converter boost inductor is presented. For that, a PCB design is formulated taking into consideration PFC boost converter component sizing and control design. Furthermore, for voltage and current control purposes, PCB implementation of sensing circuits has been done. Considering the goal of high power density, sensors arrangement, and size were reviewed. Moreover, an EMI DM filter optimization in terms of volume and number of stages, for the PFC to be compliant with the EMI standard CISPR 11 Class A and B is carried out.

Analysis of the overall performance of two-channel interleaved PFC with respect to boost inductor design parameters selection in account for continuous, discontinuous and quasi-continuous conduction modes, shows the variation in magnetic volume. Comparison for the three current modulations techniques and benefits of using un-conventional phase shift are evaluated through simulations.

Finally, the conclusion is that using mixed conduction mode, advantages of CCM and DCM can be combined. In addition, interleaving benefits can be exploited in order to achieve high power density when it comes to overall size of the converter. Mixed conduction mode is representing an attractive solution. There are practical aspects in optimizing for volume all the main components, therefore making them suitable for high-power density applications.

Nomeclature

AC	Alternating Current
ACMC	Average Current Mode Control
BW	Bandwidth
BR	Bridge Rectifier
CCM	Continuous Conduction Mode
CrCM	Critical Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
DIPIPM	Dual-In-Line Package Intelligent Power Module
DIPPFC	Dual-In-Line Package Power-Factor-Correction
DPWM	Discrete Pulse-Width-Modulation
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
GaN	Gallium Nitride
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated-Gate Bipolar Transistor
LISN	Line Impedance Stabilization Network
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OC	Over-current
PCB	Printed Circuit Board
PFC	Power Factor Correction
PWM	Pulse-Width Modulation
QCM	Quasi-continuous Conduction Mode
QP	Quasi-peak
Si	Silicon
SiC	Silicon Carbide

SMT	Surface Mount Technology
SSM	Small Signal Model
TF	Transfer Function
UV	Under-voltage
WBG	Wide Band Gap
DM	Differential mode
CM	Common mode

Symbols:

A	Area
C	Capacitance
D	Duty cycle
d	Derivative
f	Frequency
$G(s)$	Transfer function
H	Height
I	Current
Kp, Ki	Gain
L	Inductance or Lenght depending on context
M_p	Overshoot
P	Power
R	Resistance
s	Laplace operator
T	Period or Temperature depending on context
t	Time
V	Voltage or Volume depending on context
W	Width
τ	Time constant

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Chapter 1

Introduction

1.1 Background and Motivation

Power quality is one of the major concerns during the design process of front-end converters. As most of the power electronic equipment is connected to the utility grid, AC to DC conversion is required. The rectification process is widely used in applications such as power supplies, air conditioners, battery charges, electric vehicles and photovoltaic applications, among others [1]. This electrical conversion is usually achieved using power converters consisting of a diode rectifier followed by a large capacitor as shown in Figure 1.1. The conventional AC rectification approach has some undesirable side effects in the grid due to the non-sinusoidal line current that is drawn by the converter. As a result, a large amount of harmonic content appears in the AC line current.

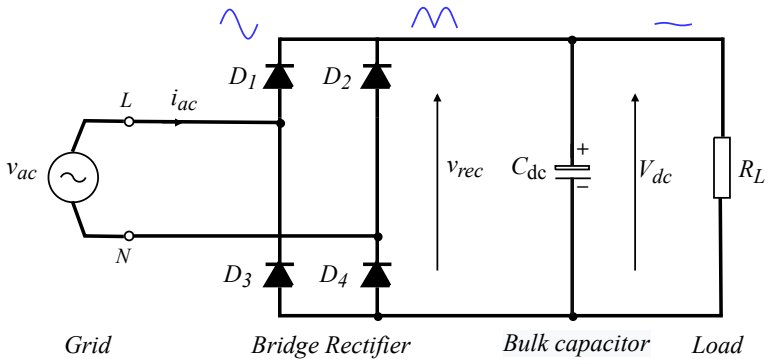


Figure 1.1: Conventional AC-DC rectification using full-wave rectifier and bulk capacitor.

Figures 1.2 and 1.3 show the line current $i_{ac}(t)$ and voltage $v_{ac}(t)$ waveforms together with the current harmonics for the conventional rectification approach. The line current presents discontinuous pulses because the diode rectifier conducts only for short periods

of time. From the current spectrum, the magnitude of the low order odd harmonics is quite significant in comparison to the fundamental (70% - 97%).

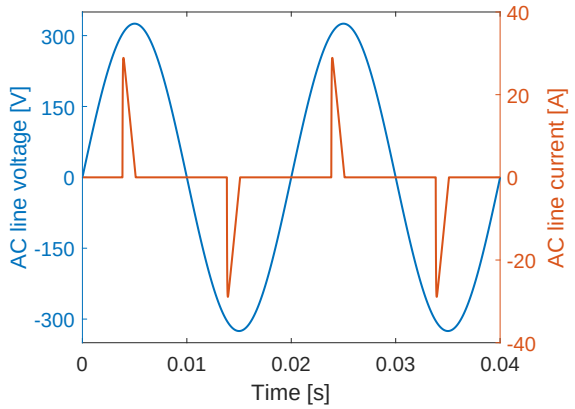


Figure 1.2: AC line voltage $v_{ac}(t)$ and current $i_{ac}(t)$ using the conventional rectification.

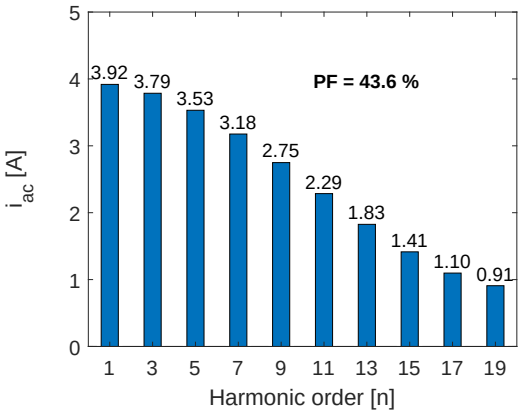


Figure 1.3: Line current spectrum using the conventional rectification.

High current harmonics have severe consequences such as system voltage distortions, reduced efficiency and possible damage of nearby electronic apparatus connected to the grid [1]. Governments worldwide are tightening regulations to limit the amount of harmonic content generated by electronic equipment connected to the mains by creating international harmonic standards, i.e., IEC-61000-3-2, IEC 1000-3-2 [1, 2].

In order to limit the conducted emissions to fulfill the harmonic standards, active power factor correction (PFC) converters are implemented. They consist of a pulse-width modulated (PWM) converter placed between the bridge rectifier and the load. Power factor (PF) is a figure of merit that relates the active power (P) and the aparent power (S) in order to measure the effectiveness of energy transmission from the AC source to the load [1].

$$PF = \frac{P}{S} = \frac{V_{1,rms} \cdot I_{1,rms} \cdot cos(\phi)}{V_{rms} \cdot I_{rms}} \tag{1.1}$$

Assuming the input rms voltage is ideal sinusoidal without harmonics ($V_{rms} = V_{1,rms}$), the previous expression can be written as the product of two factors: displacement (k_{DPF}) and distortion (k_D) power factor.

$$k_{DPF} = cos(\phi) \quad ; \quad k_D = \frac{I_{1,rms}}{I_{rms}} \tag{1.2}$$

k_{DPF} is used to describe the phase difference between the fundamental voltage and current whereas k_D accounts for the current harmonics present in the input rms current (I_{rms}) [1, 3].

Total harmonic distortion (THD) is used to numerically describe the amount of distortion present in the line current, thus it is directly related to k_D as [1],

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} {I_n}^2}}{I_{1,rms}} \quad \rightarrow \quad k_D = \frac{1}{\sqrt{1+(THD)^2}} \tag{1.3}$$

Therefore, k_D is used to find the relationship between PF and THD as in Equation 1.4. The ideal case is to obtain unity power factor which is only achieved when the input current is perfectly sinusoidal ($THD = 0$) and in phase with the AC input voltage ($\cos(\phi) = 1$) [1, 2, 4].

$$PF = k_D \cdot k_{DPF} = \frac{1}{\sqrt{1+(THD)^2}} \cdot cos(\phi) \tag{1.4}$$

In real applications unity power factor is never achieved due to the presence of energy storage devices such as capacitors and inductors [1]. However, by placing active PFC converters between source and load power factors higher than 0.99 can be obtained.

Figure 1.4 illustrates the boost PFC converter, one of the most common topologies used in PFC applications with power rating greater than 300 W [3]. Boost converters are preferred because the input is continuously connected to the power source through the inductor (L_b). This means that the current does not experience high di/dt which allows to easily shape the input current, by controlling the switching device (S_b), achieving low THD. Moreover, as the universal line voltage ($85 - 265$ $Vrms$) varies sinusoidally up to a peak voltage of 375 V, in order to obtain a DC link voltage of 380V or more a step-up converter is needed [4].

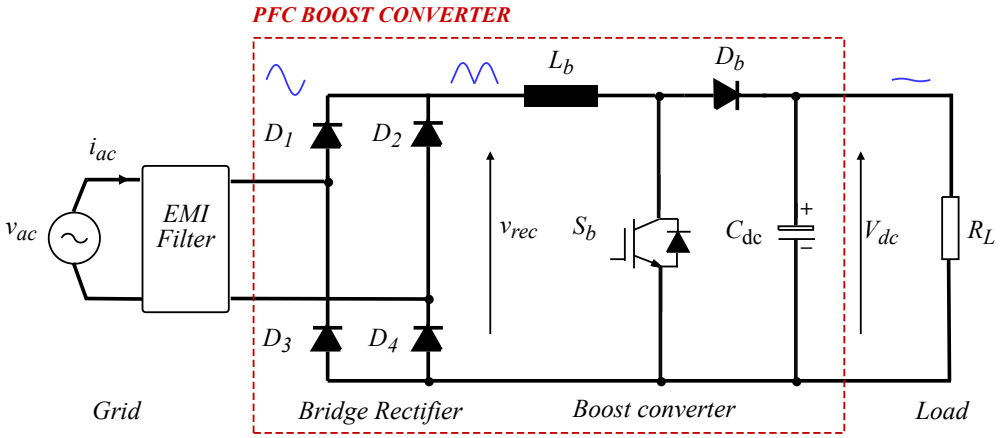


Figure 1.4: AC-DC rectification using single-phase boost PFC converter.

In every active PFC converter, an Electromagnetic Interference (EMI) filter is placed between the grid and the PFC converter to reduce the amount of high-frequency conducted emissions that is generated due to the high-switched frequency current [5]. The size of the EMI filter contributes largely with the overall size of the PFC converter, hence minimizing the EMI filter volume is important for high power density designs.

Figures 1.5 and 1.6 show that active PFC leads to a higher power factor and a significant reduction of the line current harmonics as the line current is sinusoidal and in phase with the AC voltage. Only the third order harmonic is present which is around 2% of the fundamental, thus fulfilling the standard requirements.

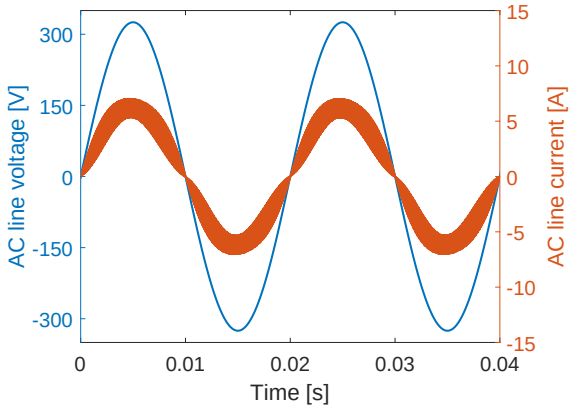


Figure 1.5: AC line voltage $v_{ac}(t)$ and current $i_{ac}(t)$ using single-phase boost PFC converter.

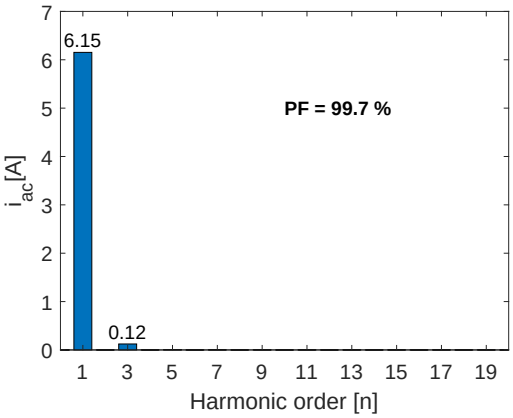


Figure 1.6: Line current spectrum using single-phase boost PFC converter.

Active PFC solutions are preferred rather than passive rectification because they highly improve the power capability by reducing the line current harmonics. Moreover, they permit to obtain accurate DC bus voltage regulation with improved dynamic characteristics [1, 3]. It is, therefore, of great importance to optimize the performance of these PFC converters. A common approach for improving PFC converters performance is to interleaved several boost cells in order to reduce the level of EMI injected into the grid [5]. Interleaving has, among other merits, the ease of implementation and reduction in components size as the inductor current is interleaved, reducing the inductor power loss. Furthermore, when the two stages are operated out-of-phase, the equivalent current ripple on the converter input and DC-link capacitor is significantly reduced [6]. Figure 1.7 shows the circuit diagram of a single-phase two-channel interleaved PFC boost converter.

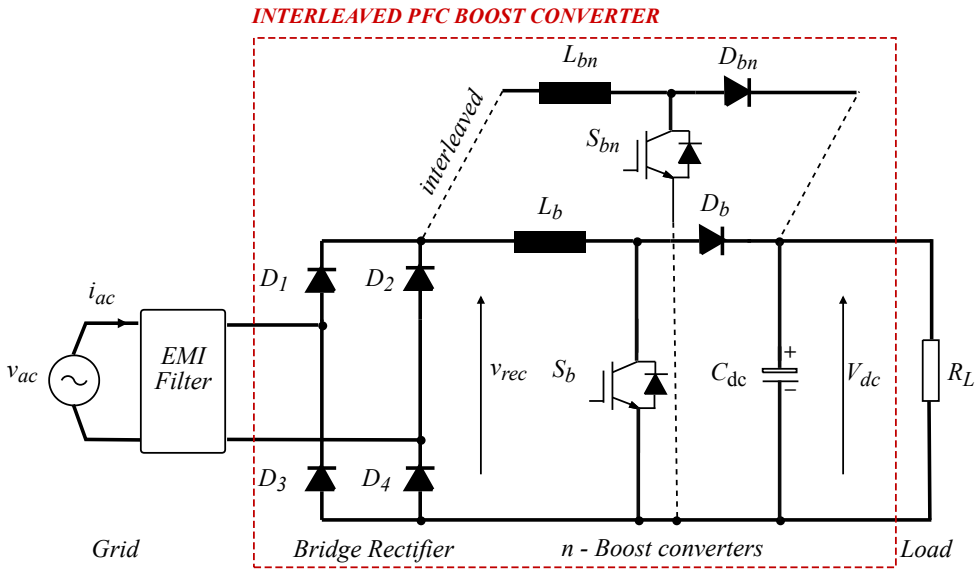


Figure 1.7: AC-DC rectification using n-channel interleaved PFC boost converter.

1.2 Types of inductor current operation modes

The inductor operating mode is an important factor when designing a PFC converter. In applications in the range of $300 - 600\ W$ power levels or less, discontinuous conduction mode (DCM) is typically used. For power levels above 300 W, the continuous conduction mode (CCM) is preferred. The operation at the *boundary* of CCM and DCM is called critical conduction mode (CrCM). Mixed-mode current operation is a combination of CCM and DCM and it is usually referred as quasi-continuous conduction mode (QCM). In the following, the advantages and drawbacks of each current modulation are briefly discussed.

Continuous conduction mode (CCM)

CCM results in lower peak currents handled by the power switch and consequently, eases the input EMI filtering, as there are no major and fast changes in the input current waveform [7]. The low current ripples translate into reduced boost inductor losses. Nevertheless, one of the disadvantages of CCM is that the switching losses (i.e., turn-on losses) increase due to the reverse recovery characteristics of the boost diode. However, with the use of recent new semiconductor devices technologies, CCM operation is still attractive, in particular, SiC Schottky diodes that can eliminate this turn-on losses due to their no reverse recovery behaviour. Lastly, the size of the boost inductor is slightly larger in CCM, because only a part of stored energy is delivered to the output in each switching cycle.

Discontinuous conduction mode (DCM)

The energy stored in the boost inductor is equivalent to the energy required by the load for one switching period, plus an amount that compensates for converter losses. In this mode of operation, the inductor current is zero during certain intervals in a switching period. Due to the low inductance value in DCM, the energy stored in the inductor depletes to zero before the end of each switching cycle, resulting in discontinuous operation. In contrast to CCM, this current modulation results in higher boost inductor losses due to a significant increase in input current ripple. The benefit of DCM is the reduction in the turn-on losses of the switches operated at zero-current-switching (ZCS) conditions.

Critical conduction mode (CrCM)

When the inductor operates in CrCM, the current hits zero at the end of an off interval but it does not remain in zero. Therefore, by the time the stage switch is turned on, the current is zero and it results in no losses due to boost diode reverse recovery behaviour. Compared to CCM, a smaller inductance will be required which means that the inductor volume is lower. In order to achieve this current operation, a variable switching frequency for the converter is required. Another drawback is the increase in switching and conduction losses do to the high current ripple as in DCM, and also in the boost inductor losses.

Quasi-continuous conduction mode (QCM)

This current waveform corresponds to some intervals working in DCM and some in CCM. The inductor current ripple gradually changes going from fully DCM to CCM. Even if a PFC converter is designed to work in CCM, at low line input voltages or low output power levels the inductor current will start to operate in DCM near the zero crossings of the line voltage [8]. The transition from CCM to DCM will occur when reducing the output power level and it will be governed by the QCM mode of operation. Operating the boost inductor in this mode, it could combine the advantages of the aforementioned current modes.

1.3 Dual-in-Line Package Intelligent Power Modules for PFC

In order to achieve high power density and efficiency, with an easy controllability and most importantly, compactness, many manufacturers propose intelligent power modules (IPM) solutions. IPMs incorporate the power switches with their dedicated gate driver and protection circuits together. The leading of the top five vendors in the IPM market from 2016 to 2020 is Mitsubishi Electric^{TM},which is also the pioneer of the Dual-In-Line Package Intelligent Power Module (DIPIPM) concept, introduced in 1997 [9, 10]. This concept contributed significantly to the miniaturization and energy-savings in power electronics systems, important aspects in home-appliances such as air conditioners, washing machines and motor drive applications. One of the continuously developed packages,

Super mini DIPIPM through-hole device, covers a high range of current ratings and it is highlighted by giving the choice between silicon (Si) IGBT and silicon carbide (SiC) devices. With SiC MOSFET as switching device, the use of DIPIPM can realize low loss and downsized peripheral components. Having in its structure an insulated sheet, facilitates the implementation of a heatsink [11].

Figure 1.8 shows the current Mitsubishi DIPIPM line-up depicted in terms of power ratings and sizes. The Super mini DIPIPM family includes interleaved configurations suitable for PFC applications. Hybrid modules, consisting of a Si IGBT and and SiC diode, or full SiC modules with voltage and current ratings of 600 V and 20 A are widely used in white goods. With these specifications, the DIPPFC module makes a good candidate for this project work.

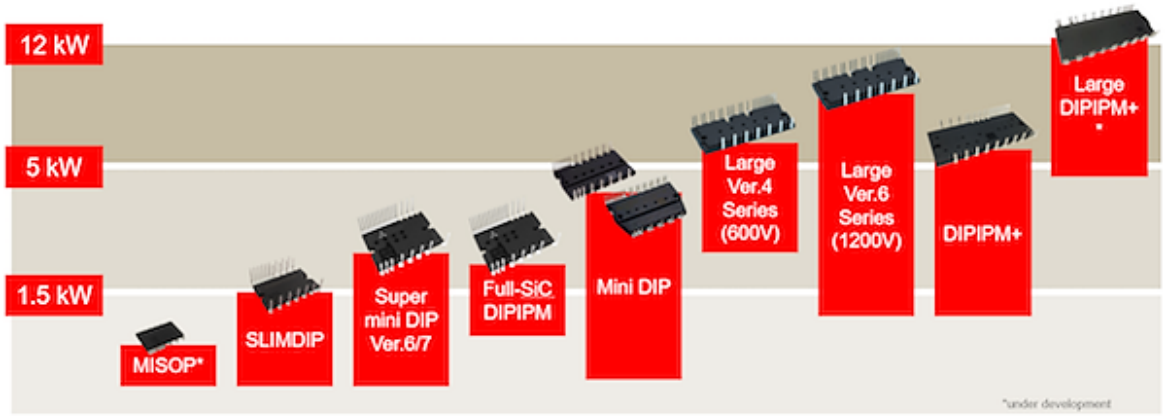


Figure 1.8: Mitsubishi current DIPIPM lineup [12].

1.4 Scope of the project

The aim of this thesis is to analyze the effect of different types of current modulation techniques on the performance of active PFC boost converters. CCM and DCM operation has been widely investigated in previous works. The effect of partial CCM operation, also known as quasi-continuous conduction mode (QCM), on the design of EMI filters for PFC converters is to be analyzed in detail in this project. In order to determine if QCM operation is a feasible solution to improve efficiency and power density of PFC converters, a comparison with the other two modulation techniques will be performed. In addition, due to the continuous increase in power capability demand, the benefits of interleaving parallel boost cells will be investigated as a potential measure to optimize EMI filter volume. This project will benefit from recent intelligent PFC power module products from Mitsubishi Electric^{TM} which include interleaved boost cells and gate drivers in the same package aiming to increase power density.

1.4.1 Problem statement

Analyzing the influence of different current modulation and interleaving techniques on the design of single-phase PFC boost converter in order to achieve high performance and power density including the EMI filter and boost inductor optimization.

1.4.2 Objectives

- Analysis of impact of three different current modulation techniques (CCM, DCM and QCM) on boost PFC and EMI filter component sizing.
- Development of an optimized EMI filter design methodology for single and interleaved boost PFC based on CISPR 11 standard for Class A and Class B equipment.
- Implementation of closed-loop digital control for three current operating modes for both single and interleaved topologies and analysis of the effect of load dynamics.
- Investigation of influence of smart current modulation over wide range of power levels for single and interleaved boost PFC.
- Design and hardware prototyping of single-phase interleaved boost PFC converter.

1.5 Specifications

Table 1.1 shows the specifications for the interleaved PFC boost converter.

Specifications of 1 kW PFC interleaved converter		
	Parameter	Value
Nominal input rms voltage	V_{in}	230 VAC
AC line input frequency	f_{line}	50 Hz
Switching frequency	f_{sw}	28 kHz
Nominal output voltage	V_o	400 VDC
Nominal output current	I_o	2.5 A
Output power range	P_o	100 - 1000 W
Maximum voltage ripple	$\Delta V_{o,pk-pk}$	10 [V]
Hold-up time	t_{hold}	16.6 ms @$V_o = 340V$
Power factor at rated power	PF	> 0.99

Table 1.1: Electrical specifications.

1.6 Thesis outline

The organization of the thesis is as follows.

Chapter 2 presents the design of the boost inductor and output capacitor for the three different current operating modes. The effect of loading profile on component sizing is analyzed as well as some of the benefits of interleaving several boost cells (i.e., input current ripple cancellation).

Chapter 3 firstly introduces the mathematical model of the boost converter based on the state-space averaging technique. Then, the digital closed-loop controller is designed for the three conduction modes (CCM, QCM and DCM). The effect of load dynamics on the system's time response is analyzed through *PLECS* simulations.

In **Chapter 4** the design of a single-phase two-channel interleaved PFC boost converter is presented. The component sizing of sensors, components for signal conditioning for the DSP and converter thermal model is introduced in this chapter. This chapter ends with the PCB layout and calculation of PFC converter power density.

Chapter 5 is dedicated to the EMI filter design for the three current operating modes. The goal is to find the optimum filter component values that will provide the required attenuation aiming for reduction in total converter volume. The filter volume optimization is based on the required attenuation according to CISPR11 standard and the the optimum number of filter stages.

In **Chapter 6** the performance of the two-channel interleaved converter is analyzed. An optimization of the boost inductor volume is performed in regards to k_{ripple} for CCM operation and angle α for QCM operation. A comparison of the total volume and power loss for CCM, QCM and DCM and different phase-shift angles between the interleaved cells is done to determine which current modulation technique and, under which conditions, leads to improved efficiency and volume.

Lastly, in **Chapter 7** the conclussions of the project work and some suggestions for future research are presented.

Chapter 2

Interleaved PFC boost converter

In the design of a 1 kW interleaved PFC boost converter having the specifications mentioned in Table 1.1, several steps are involved. This chapter starts with the benefits of implementing interleaving techniques. Then the boost inductor design for single-channel and two-channel PFC converter according to operation in the different current modes is carried out. The output capacitor design is also included and finally the simulations results used to verify the design are shown.

Figure 2.1 shows the circuit diagram of a two-channel PFC boost converter with the constituent blocks. As shown, both channels share the input current i_L and are connected to the DC-link capacitor C_{dc}. In the control of this converter, the PWM signals are usually shifted by 180°. The phase shifting results in input current ripple cancellation, thus making this topology ideal for PFC applications [13].

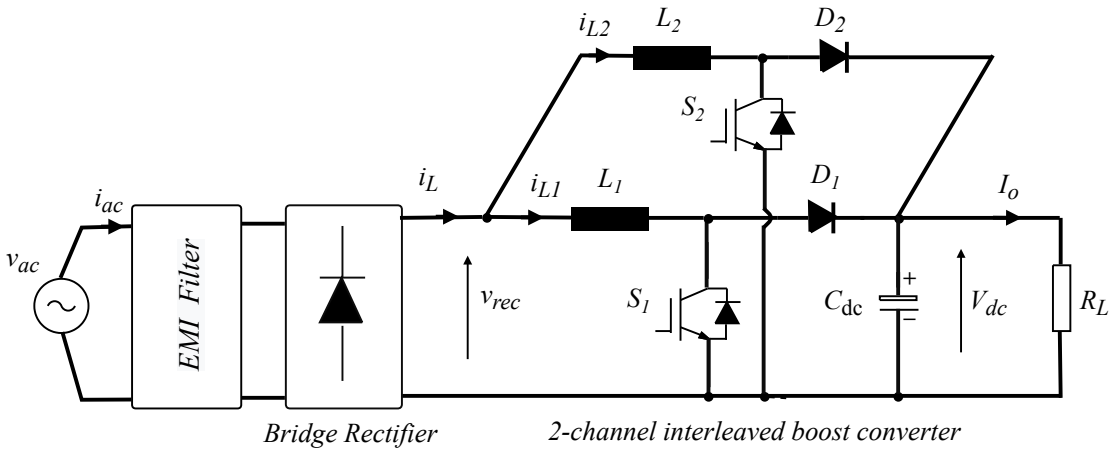


Figure 2.1: Two stages interleaved PFC boost converter diagram

Moreover, by sharing the load current in two phases, the RMS current stress on devices is diminished, and consequently the overall efficiency can be improved. This allows for selection of reduced components size, eventually leading to a cost effective power switch and boost diode which results in higher reliability of the power supply.

2.1 Input current ripple cancellation

In order to evidence one of the most important benefits of interleaving, in this section, the effect of current ripple cancellation is shown. Considering the circuit diagram in Figure 2.1, the functional states of the switches, noted as S1 and S2, and an sketch of the inductor current waveforms (i_{L1} and i_{L2}) together with the rectified input current (i_L) are shown in Figure 2.2.

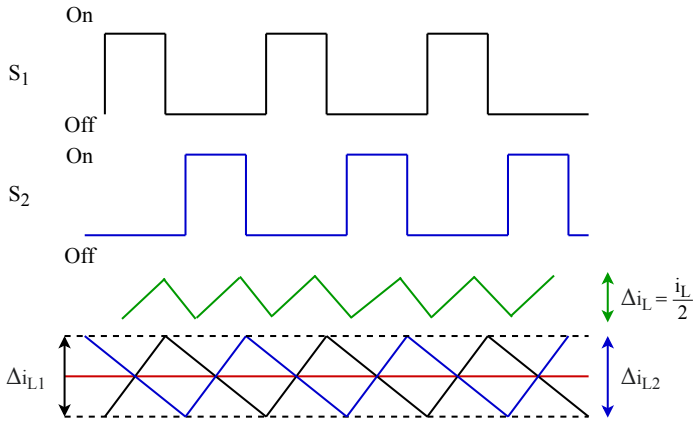


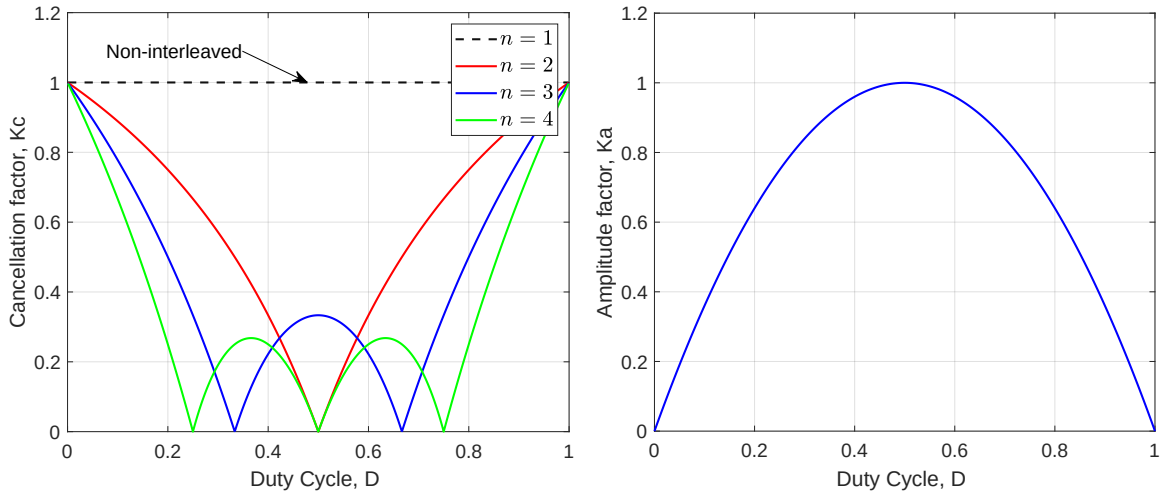
Figure 2.2: Interleaved boost stage on/off switch signals and resulting inductor current waveform

In PFC converters the duty cycle varies accordingly to changes in line phase angle and input voltage. For the so called high line, it will vary from 100% downwards. The cancellation factor K_C is defined as the ratio of the ripple magnitude of the interleaved converter to the magnitude of the ripple in one individual phase or converter ($K_C = \Delta_{i_L}/\Delta i_{L_1}$). Due to the duty cycle variation in PFC converters, the ripple cancellation does not occur in every part of the line cycle. K_C can be then expressed as a function of the duty cycle [14]:

$$K_C(D) = \frac{1-2D}{1-D} \quad if \quad D \leqslant 0.5 \tag{2.1}$$

$$K_C(D) = \frac{2D-1}{D} \quad if \quad D > 0.5 \tag{2.2}$$

In order to describe the net interleaved ripple amplitude, Equation 2.2 is graphically depicted in Figure 2.3a. The input ripple current cancellation for up to n = 4 interleaved cells is shown, highlighting the duty cycles at which the current ripple cancellation is maximum according to the number of interleaved channels. In comparison to single-channel, the ripple current of the two-channel interleaved converter is improved over the full duty cycle range. Especially, at D = 0.5 duty cycle, a ripple-free current can be obtained. In figure 2.3b, the amplitude factor K_a represents the amplitude of a single boost cell in respect to the duty ratio.



(a) Cancellation factor, K_c

(b) Amplitude factor, K_a

Figure 2.3: Input current ripple cancellation (a) and amplitude (b) effect as a function of duty cycle for $n = 1, .., 4$ interleaved stages operating in CCM.

Furthermore, in order to show the outstanding benefit of interleaving in terms of both ripple elimination factor K_c and amplitude factor K_a more clearly, a third factor is defined. This factor, K_{cr} is the expression of the net ripple produced by interleaving n channels with regards of the amplitude of the single channel ripple. It is called normalized factor. It is depicted as in Figure 2.4. Here, emphasis is put on the fact that the amplitude of the combined ripples when comes to multiple stages, never exceeds that of an single unit.

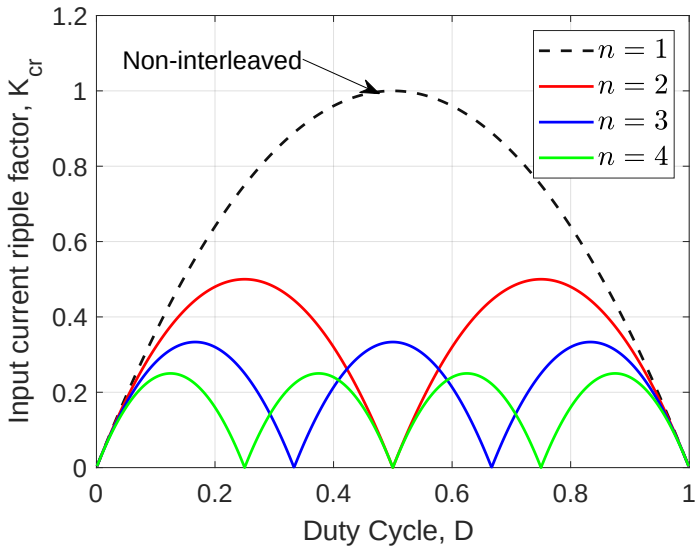


Figure 2.4: Normalized input current ripple as a function of duty cycle for $n = 1,..,4$ interleaved stages operating in CCM, $K_{cr} = K_c \cdot K_a$.

Other aspect is the energy stored in the inductor. It is defined as in Equation 2.3 where L is the boost inductance and I is the input current [15]:

$$E = \frac{1}{2} \cdot L \cdot I^2 \tag{2.3}$$

When interleaving two channels, the input current is shared between the two paralleled inductors, therefore the total inductor energy is expressed in Equation 2.4. It is observed that in order to keep total constant energy storage in comparison to a non-interleaved converter, the inductance of each the interleaved cells should be doubled ($L_{int} = 2 \cdot L_{single}$).

$$E_{int} = \frac{1}{2} \cdot L_{int} \cdot \left(\frac{I_{in,rms}}{2}\right)^2 + \frac{1}{2} \cdot L_{int} \cdot \left(\frac{I_{in,rms}}{2}\right)^2 = \frac{1}{4} \cdot L_{int} \cdot I_{in,rms}^2 \tag{2.4}$$

This can translate into a reduction of inductor volume for each of the interleaved stage, since the energy storage requirement for each inductor is halved compared to the energy stored in a single unit, considering the same power level and switching frequency. Nevertheless, the reduction in energy storage does not always directly translate into magnetic volume reduction, the volume being influenced by another factors as well, such as the magnetic cores that are selected, as will be shown in the dedicated chapter of this work. Eventually, a reduction in size of up to 30% by interleaving is expected, as studies show [14].

2.2 Boost inductor design

The overall performance and size of a PFC converter is affected by the design and selection of the magnetic components. Therefore, the design starts with the boost inductor which inductance value is dependent on the current operating mode (CCM,DCM or QCM), the switching frequency and the different load conditions.

The PFC converter specifications are summarized in Table 1.1. The boost inductor is designed to operate in either CCM, QCM or DCM at rated power ($P_o = 1\ kW$) in order to obtain a constant DC output voltage of $V_o = 400\ V$ for a line input voltage of $V_{in,rms} = 230\ V$. Thus, the nominal output current of the converter is $I_o = P_o/V_o = 2.5\ A$ which corresponds to a resistive load of $R_L = 160\ \Omega$ at rated power. In the following, the efficiency of the converter is assumed to be $\eta = 100\%$. The rms and peak line input current can then be calculated as:

$$I_{in,rms} = \frac{P_o}{\eta} \cdot V_{in\_RMS} = 4.34\ A \quad ; \quad I_{in,pk} = \sqrt{2} \cdot I_{in,rms} = 6.15\ A \tag{2.5}$$

2.2.1 CCM operation

In CCM, the inductor current i_L remains above zero for the switching period T_s. This mode of operation is illustrated in Figure 2.5. The ripple factor, k_{ripple}, relates the peak-to-peak inductor current with the local average current at one specific point, $k_{ripple} = \Delta i_L \backslash i_{L,avg}$. It is an important factor to consider as it will shape the current in the input and output capacitor of the PFC boost converter stage.

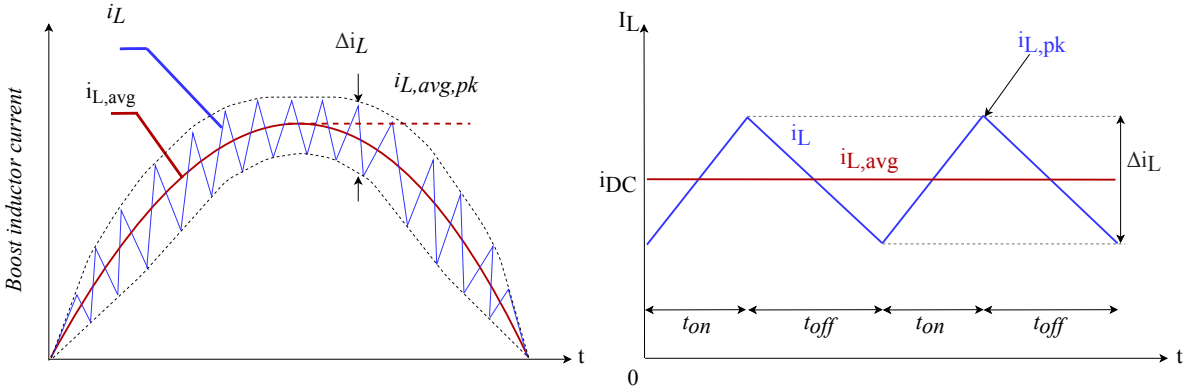


Figure 2.5: *Left:* CCM inductor current i_L and average current $i_{L,avg}$. *Right:* Zoomed view showing AC peak-to-peak current Δi_L detail.

Hence, the maximum peak-to-peak current ripple is expressed as [2]:

$$\Delta i_{L,max} = k_{ripple} \cdot i_{L,avg} \tag{2.6}$$

For CCM, typical values of k_{ripple} are in the range of 20% to 40% of the average input current [16]. The boost inductor average current in a non-interleaved PFC converter corresponds to the rectified line current as shown in Equation 2.7, where θ is the phase angle at which the maximum current ripple occurs.

$$i_{L,avg} = \mid i_{in} \mid \; = \mid I_{in,pk} \cdot sin(\theta) \mid \tag{2.7}$$

Figure 2.4 shows that for a single-channel PFC converter, the maximum ripple occurs when the duty cycle is $D = 0.5$. From the gain ratio of the converter operating in CCM, it is shown that it corresponds to:

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \quad \rightarrow \quad V_{in} = \frac{V_o}{2} \tag{2.8}$$

Substituting this relation in the expression of the line input voltage, $V_{in} = V_{in,pk} \cdot sin(\theta)$, it is found that maximum ripple in CCM takes place at $\theta = 38^{\circ}$. This way $\Delta i_{L,max}$ can be calculated from Equations 2.7 and 2.6. With this, one can proceed with the inductor voltage equation in order to obtain the required inductance in CCM. When the power switch of the boost stage is conducting the inductor voltage V_L is:

$$V_L = V_{in} = L \cdot \frac{\Delta I_L}{D \cdot T_s} \tag{2.9}$$

By replacing Equation 2.8, which corresponds to D=0.5, and rearranging the previous expression the minimum inductance that guarantees CCM operation is:

$$L_{CCM} \geqslant \frac{V_o}{4 \cdot \Delta i_{L,max} \cdot f_{sw}} \tag{2.10}$$

For an interleaved configuration, the CCM inductor size is determined similarly as for the non-interleaved exemplification above. Equation 2.10 can be employed. One key difference is that input current is halved, due to its sharing between the two inductors therefore, the peak-to-peak ripple calculation becomes :

$$\Delta i_{Lmax,int} = k_{ripple} \cdot i_{Lavg,int} \tag{2.11}$$

where the inductor average current is now calculated as the input peak current divided by the number of interleaved phases n:

$$i_{Lavg,int} = \frac{I_{in,pk}}{n} \cdot sin(\theta) \tag{2.12}$$

2.2.2 DCM operation

When the current through the inductor reaches zero and holds in zero for the remaining time of the switching period, the PFC converter is operated in discontinuous conduction mode. DCM may also occur when the output load power decreases, assuming a constant input voltage and duty cycle [17]. In Figure 2.6 the DCM inductor current waveform is depicted as i_L. When the power switch of the converter is off, the energy stored previously in the inductor is transferred to the output capacitor and the load. Hence, the inductor current drops from its peak towards zero. When the amount of energy required by the load is low, there are situations when this can be delivered to the load from the inductor in an shorter time than the switching period, resulting in the period where the current is zero. Unlike with CCM, the inductor discharges completely by the end of a commutation cycle. From the figure it is seen that the peak-to-peak ripple Δi_L is twice the average current.

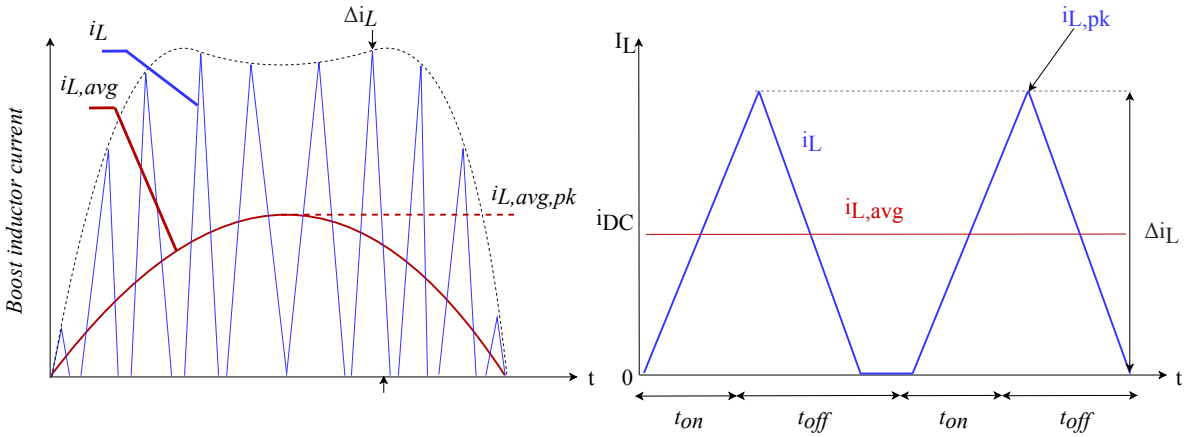


Figure 2.6: *Left:* DCM inductor current i_L and average current $i_{L,avg}$. *Right:* Zoomed view showing AC peak-to-peak current Δi_L detail.

In order to ensure that the converter operates over the entire half-line cycle in DCM, the point where the boundary between CCM and DCM occurs is analyzed. For instance, if a PFC converter is operating in DCM and there is a significant increase in load power level, the inductor current will start working in CCM at $\theta = 90^\circ$. Therefore, the local average current is chosen at this point, which is the point where the current ripple should hit zero, maintaining it at the boundary, not getting out of DCM.

$$\Delta i_{L,max} = 2 \cdot i_{L,avg} \quad , \; where \quad i_{L,avg} = I_{in,pk} \cdot sin(\theta) \tag{2.13}$$

The maximum inductance to keep the converter in DCM operation is found applying volt-second balance resulting in the expression of Equation 2.14.

$$L_{DCM} \leqslant \frac{V_{in,pk} \cdot (1 - \frac{V_{in,pk} \cdot sin(\pi/2)}{V_o})}{\Delta i_{L,max} \cdot f_{sw}} \tag{2.14}$$

This corresponds to the boundary, thus, it is advisable to select an inductance lower than this value to have some margin in case of load changes or inductance variation. Using Equation 2.14 for calculating the required inductance for an interleaved topology having two boost cells, same criteria applies: the current is shared among the boost inductors. Hence, replacing $\Delta i_{Lmax.int} = 2 \cdot I_{in,pk}/n$, with n being the number of cells, one can obtain the needed inductance value for multiple superimposed stages.

2.2.3 QCM operation

Mixed-conduction mode occurs when the boost PFC converter operates in both CCM and DCM during a single line cycle. In this work, this is referred to as Quasi-continuous conduction mode. The waveform of the inductor current for such a half-cycle is exemplified in the left of Figure 2.7. The current i_L detail is presented in the Figure 2.7 to the right . Here the point where the current waveform moves from DCM to CCM is defined as α, which is the boundary between the two current modulation modes. For a full DCM operation this angle was, as seen in previous section, θ equivalent of 90° degree, the midpoint of the rectified input voltage sinusoid. Angle α is defined as a point different to the value of θ. In order to define α and choose it optimum value, optimization is discussed in Chapter 6.

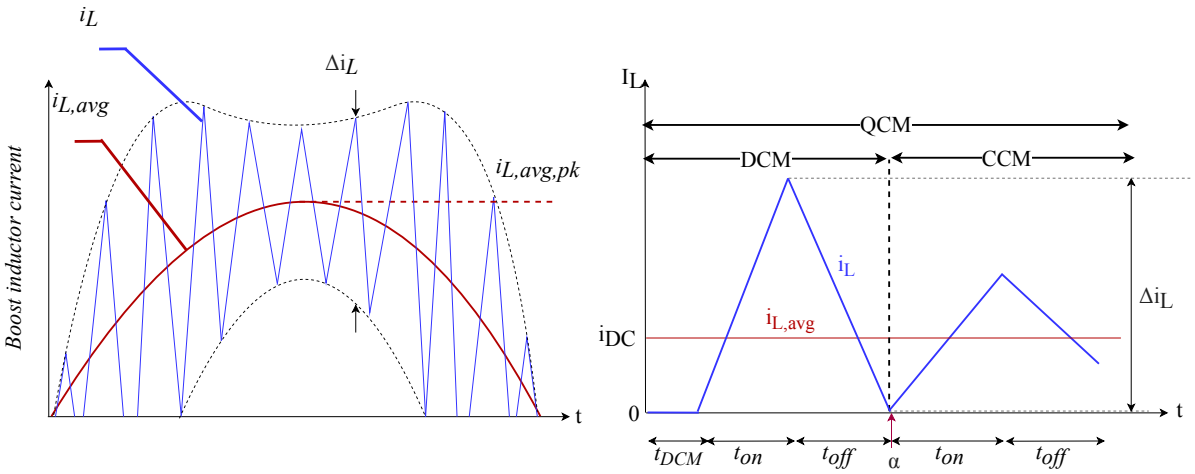


Figure 2.7: *Left:* CCM inductor current i_L and average current $i_{L,avg}$. *Right:* Zoomed view showing AC peak-to-peak current Δi_L detail.

In order to size the inductor to have a DCM behaviour up to a specified point only, from which, approaching to the middle of the waveform, it presents a CCM characteristic, the same equation as for DCM inductance sizing can be used as a starting point, taking into account the difference in the duty cycle.

$$D = 1 - \frac{V_{in}}{V_o} = 1 - \frac{\sqrt{2} \cdot V_{in,rms} \cdot \sin \alpha}{V_o} \tag{2.15}$$

$$L_{QCM} = \frac{V_{in,pk} \cdot (1 - \frac{V_{in,pk} \cdot \sin\alpha}{V_o})}{\Delta i_{L,max} \cdot f_{sw}} \tag{2.16}$$

Considering the same angle α as the point where the transition from one operating mode to the other occurs, the values for converter topology with two boost braches can be obtained using Equation 2.16, for L_{QCM}, with the important difference in $\Delta i_{L,max}$ considered for the shared current as mentioned at the end of DCM section.

2.3 Output capacitor design

The sizing the output bulk capacitor, C_{dc} in Figure 2.1, is done in this section based on the specifications in Table 1.5. The hold-up time (t_{hold}) and the output voltage ripple (ΔV_o) are defined as design requirements. Many technical notes [4, 18, 19] show the derivation of t_{hold} starting from the energy equation for a capacitor. Therefore, just a general definition of the hold-up time as an important parameter for switched-mode power supplies, as it is the case of the PFC boost converter. The hold-up time, usually measured in milliseconds, refers to the time that the power supply will maintain the output voltage within the specified range when the input supply power is chopped. The hold-up time and the peak-to-peak voltage ripple are inserted in the following equations [4]:

$$C_{dc} \geqslant \frac{2 \cdot P_o \cdot t_{hold}}{V_o^2 - V_{o.min}^2} \tag{2.17}$$

$$C_{dc} \geqslant \frac{P_o}{2 \cdot \pi \cdot f_{line} \cdot \Delta V_o \cdot V_o} \tag{2.18}$$

where P_o is the rated output power (1 kW), t_{hold} is the hold-up time (16.6 ms) f_{line} is the fundamental frequency (50 Hz), V_o is the DC output voltage (400 V), ΔV_o is the maximum allowed output voltage ripple (10 V) and $V_{o,min}$ is the minimum output voltage (340 V). Clubbing in the corresponding values, the output capacitor value is chosen to be the maximum resulting from the Equations 2.17 and 2.18.

$$C_{dc} = max(747\mu F, 800\mu F) \rightarrow C_{dc} = 800\mu F \tag{2.19}$$

2.4 Effect of loading profile on component sizing

Continuous mode inductor current can easily transition into discontinuous mode of operation under light load conditions [3]. In order to ensure the CCM operation over a wide range of the loading profile (i.e., 20% to 100%), the minimum required inductance value calculated using Equation 2.10 should be evaluated. Considering a minimum load as 20%

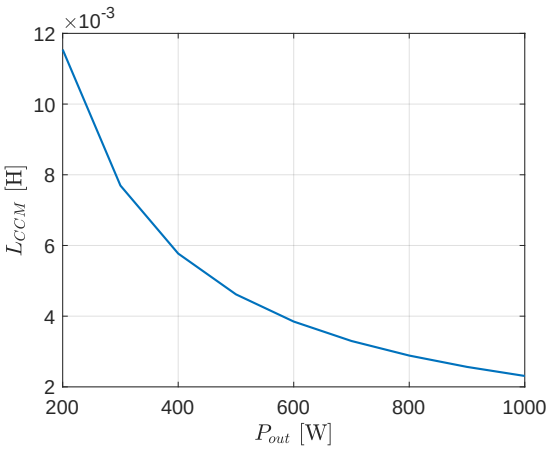
out of the rated output power P_o and the maximum switching frequency f_{sw} as in Table 1.1, the minimum inductance in CCM is written as function of output power as follows:

$$I_{in,rms} = \frac{P_o}{V_{in,rms} \cdot \eta} \tag{2.20}$$

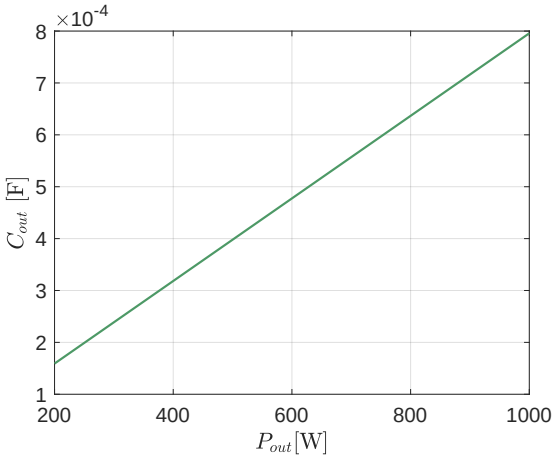
$$I_{in,avg} = \frac{2 \cdot \sqrt{2}}{\pi} \cdot I_{in,rms} \tag{2.21}$$

$$\Delta i_{L,max} = k_{ripple} \cdot I_{in,avg} \tag{2.22}$$

$$L_{CCM_{min}} = \frac{D \cdot (1 - D)}{f_{sw} \cdot \Delta i_{L,max}} \tag{2.23}$$



(a) Variation of L_{CCM} inductance value as function of different output power levels



(b) Variation of C_{out} inductance value as function of different output power levels

Figure 2.8: Effect of loading profile on boost inductance and dc-link capacitance

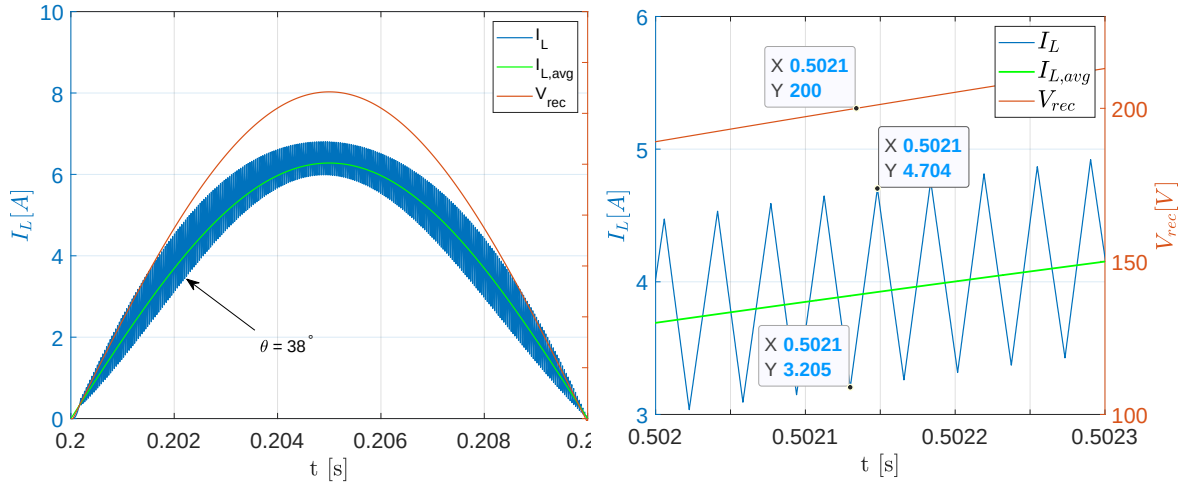
The impact of load on the minimum inductance value necessary to avoid losing CCM operation is shown in Figure 2.8a. Here, as the power level increases, the minimum inductance value, designed for the same input converter parameters and same current ripple factor k_{ripple}, decreases. This is due to the fact that for the same current and voltage input, when the power required at the output is lower, higher ripple will be present on the inductor, so it will require a much higher value of inductance to ensure CCM operatio, characterized by a lower peak-to-peak ripple, is still maintained. When it comes to the output capacitance, as the load demand increases, a higher capacitance value is required in order to deliver the needed output voltage and current as seen from Equations 2.17-2.18.

2.5 Analytical and simulation results

This section is intended to validate the boost inductor design in CCM, QCM and DCM. Following the steps presented in subsections 2.2.1, 2.2.2 and 2.2.3, the final results for PFC converter with single and two-channel interleaved PFC converter are presented.

2.5.1 PFC converter single stage and interleaved, operated in CCM

Making use of Equation 2.10 and input parameters from Table 1.1, the minimum inductance value in order to operate the PFC single boost unit in CCM, is found to be $L_{CCM} = 2.4\ [mH]$, designed for the worst case scenario, when the maximum inductor current ripple occurs. It is important to ensure that the inductor will remain in CCM, finding the angle θ, in order to validate the maximum current ripple $\Delta i_{L,max}$. In Figure 2.9a the previously obtainted phase angle θ is pointed out at the corresponding time t. The time is obtained by translating the angle to time in seconds, in order to verify that in simulation, the point where the maximum peak-to-peak current through inductor is expected and its value are correctly derived from calculations. Hence, by zooming in the corresponding area, Figure 2.9b is obtained. The cursors indicate the value of the minimum and maximum peak at $t = 0.5021$ [s], when the input voltage noted as V_{rec}, stating for rectified voltage, is half of the maximum design output voltage, 200 [V] as indicated by the data tip. The simulated peak-to-peak ripple is found to be 1.5 [A].

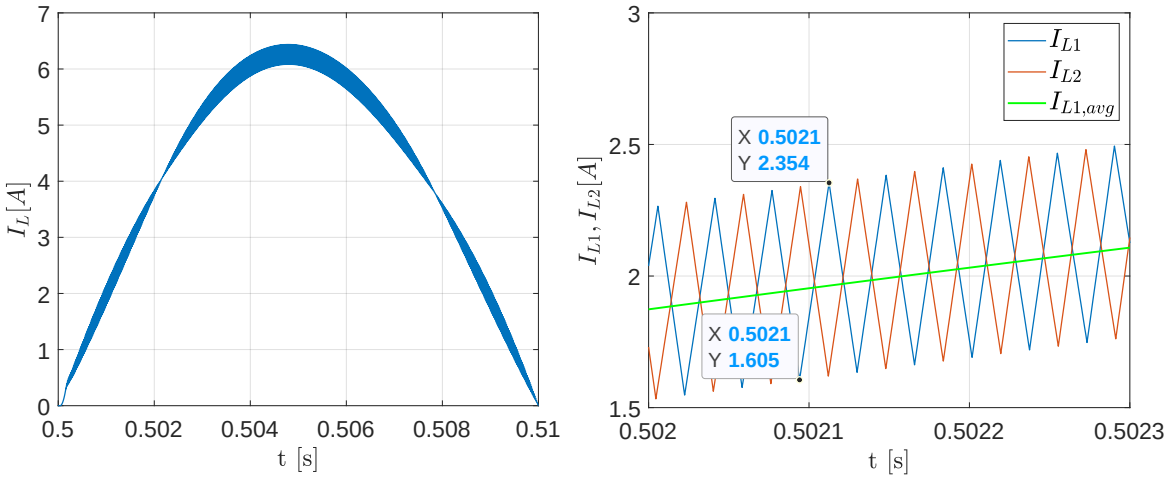


(a) CCM single.

(b) CCM single zoom for $\Delta i_{L,max}$ validation.

Figure 2.9: (a) Simulated CCM boost inductor current for single stage PFC converter (L = 2.4 mH) and the rectfied voltage V_{rec} on one half line cycle and (b) detailed view of maximum peak-to-peak current in inductor at angle $\theta = 38°$.

For the interleaved case, same analysis is applied, and based on Equations 2.10-2.12, the boost inductor designed for the same ripple factor as for single, is found to be $L_{CCM_{interleaved}} = 4.8\ [mH]$. In Figure 2.10a, the current at the input of the two inductors is shown I_L, which is the rectified current. It can be observed that the ripple in the current envelope is lower. A closer look is taken to the inductor currents in interleaved I_{L1} and I_{L2}. The equivalent $\Delta i_{L,max}$ is the difference between the Y axis values of the data tips in Figure 2.10b. The resultant value is found to be 0.749 [A], which is half of the ripple seen by the inductor in Figure 2.9b, due to the current sharing between the two inductors. Here stands out the fact that the resultant ripple is halved for two superimposed inductors, keeping the same ripple factor as for single stage converter, k_{ripple} as design reference.



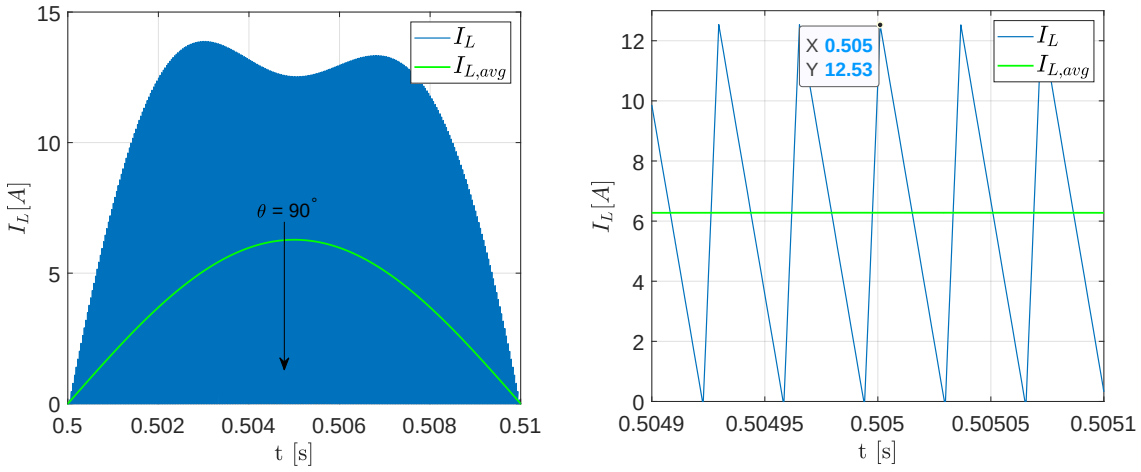
(a) CCM interleaved.

(b) CCM interleaved zoom for $\Delta i_{L1,max}$ validation.

Figure 2.10: (a) Simulated CCM boost input inductor current I_L for interleaved PFC converter (L = 4.8 mH) and (b) detailed view of maximum peak-to-peak current of I_{L1} and I_{L2} at $\theta = 38°$.

2.5.2 PFC converter single stage and interleaved, operated in DCM

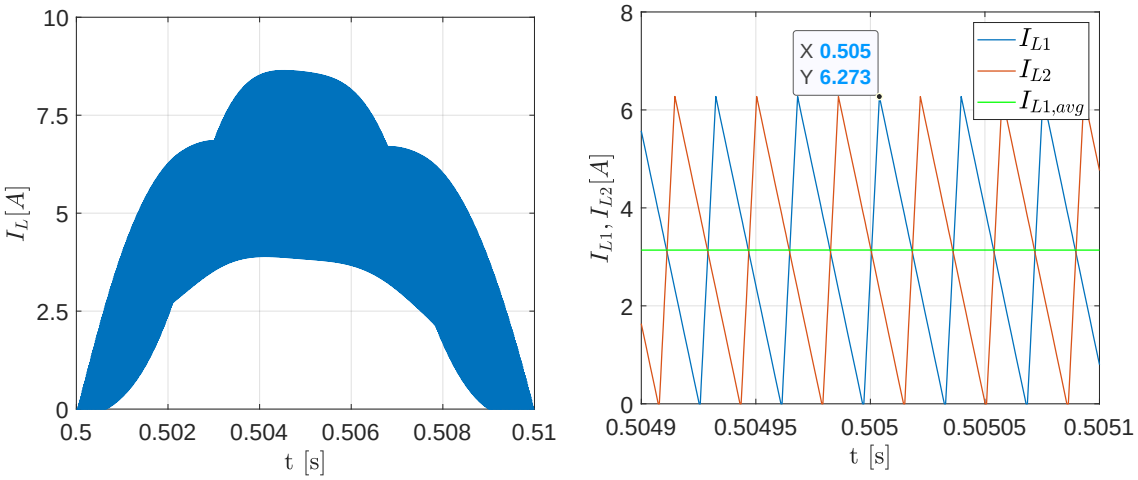
Figure 2.11 shows the results of simulated PFC converter under discontinuous mode. For this, numerical results obtained from Equation 2.14, $L_{DCM} = 0.176\ [mH]$ and $L_{DCM_{interleaved}} = 0.35\ [mH]$ are used in simulation. Figure 2.11a shows the inductor current waveform envelope in DCM and its average value $i_{L,avg}$. To check that the converter is in DCM at the design point of $\theta = 90°$, a zoom in is taken in Figure 2.11b. Here, the specific current waveform presenting discontinuities, by holding in zero, for a time before the next switching cycle. Also, the maximum ripple is found to be, in simulation 12.53 [A], which is around twice the line input peak current. In Figure 2.12a I_L, input current for the interleaved PFC converter in DCM is shown. In Figure 2.12b it can be observed, that the current ripple is half of the ripple in case of non-interleaving.



(a) DCM single.

(b) DCM single zoom for $\Delta i_{L,max}$ validation.

Figure 2.11: (a) Simulated DCM boost inductor current for single stage PFC converter (L = 0.176 mH) and (b) detailed view of maximum current ripple at $\theta = 90°$.



(a) DCM interleaved.

(b) DCM interleaved zoom for $\Delta i_{L1,max}$ validation.

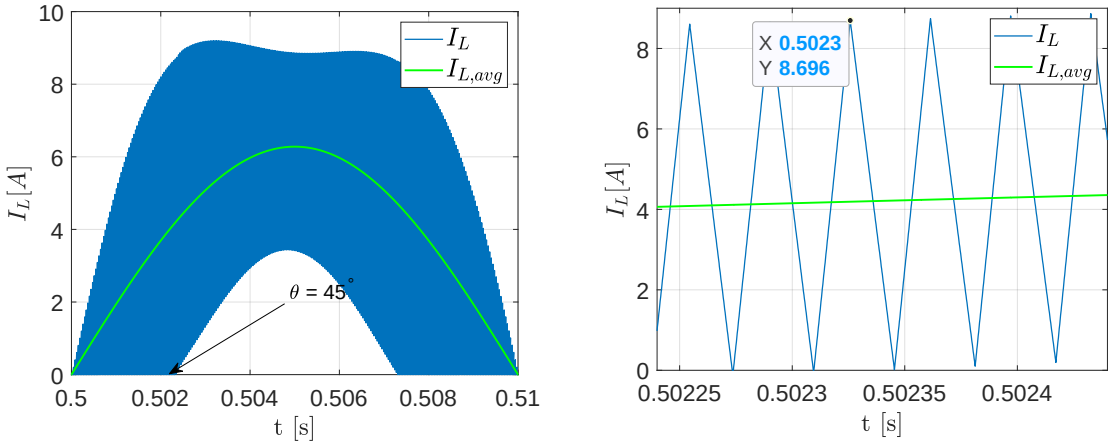
Figure 2.12: (a) Simulated DCM boost inductor current for interleaved PFC converter (L = 0.35 mH) and (b) detailed view of maximum peak-to-peak current of I_{L1} and I_{L2} at $\theta = 90°$.

2.5.3 PFC converter single stage and interleaved, operated in QCM

QCM operation is analyzed using the obtained inductance value for both topologies using Equation 2.16. Figure below shows the single stage PFC inductor current in mixed conduction mode. In Figure 2.13a, the arrow is pointing the moment when transition from one mode to the other occurs, at the chosen angle α away from 90°, which is the midpoint of

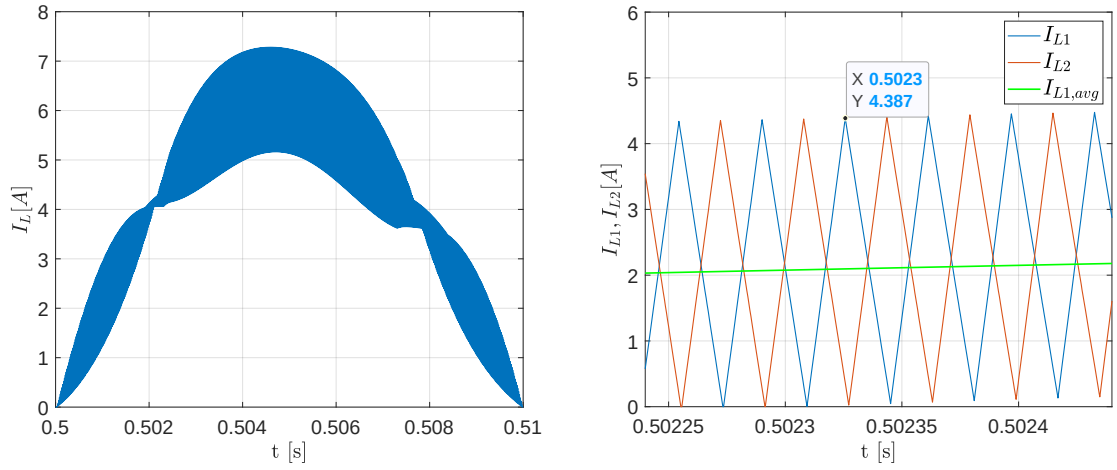
the half-cycle. At this point, the ripple is the largest appearing during the energy transfer. Hence, this boundary point is verified in simulation and magnified in Figure 2.13b.

Rectified current over half line cycle for two-channel interleaved PFC converter is shown in Figure 2.14a. In order to ensure the design has been properly made, to verify the numerical solutions and the chosen angle ($\alpha = 45°$), the corresponding time is derived as follows: $t\ [s] = \alpha/(2 \times \pi \times f_{line})$. When it comes to the case of two parallel inductors, the current ripple in the inductor is halved, as shown in Figure 2.14b.



(a) QCM single. **(b)** QCM single zoom for $\Delta i_{L,max}$ validation.

Figure 2.13: (a) Simulated QCM boost inductor current for single stage PFC converter (L = 0.4 mH) and (b) detailed view of maximum current ripple at $\alpha = 45°$.



(a) QCM interleaved. **(b)** QCM interleaved zoom for $\Delta i_{L1,max}$ validation.

Figure 2.14: (a) Simulated QCM boost inductor current for interleaved PFC converter (L = 0.8 mH) PFC boost converter and (b) detailed view of maximum current ripple at $\alpha = 45°$.

A comparison between the calculated values for $\Delta i_{L,max}$ and values obtained from simulations is shown in Table 2.1. It is seen that the error between numerical and simulated results is not significant. Thus, simulations results prove that the obtained inductance values for each of the three different current modulation techniques are valid.

As it was mentioned in this chapter, CCM presents the lowest inductor current ripple while DCM the highest. The lower the current ripple is the higher the inductance required which translates into an increase in boost inductor volume but a reduction in EMI filter size. On the other hand, if higher current ripple is accepted for the design the inductance will be smaller although as consequence the EMI filter volume will experience an increase. The simulation results for QCM show intermediate results which makes this current modulation technique interesting for further analysis.

Single	CCM (L = 2.4 mH)	QCM (L = 0.4 mH)	DCM (L = 0.176 mH)
$\Delta i_{L,max}$ numerical	1.51	8.68	12.3
$\Delta i_{L,max}$ simulation	1.5	8.696	12.53
Interleaved	CCM (L = 4.8 mH)	QCM (L = 0.8 mH)	DCM (L = 0.35 mH)
$\Delta i_{L,max}$ numerical	0.756	4.34	6.15
$\Delta i_{L,max}$ simulation	0.749	4.387	6.273

Table 2.1: Summary of PFC numerical and simulation results for $\Delta_{iL,max}$ in CCM, QCM and DCM.

Chapter 3

Digital control of interleaved boost PFC working in CCM, QCM and DCM

During the design process of every digital controller the first step is to obtain a mathematical model of the system under study. For this, *State Space Averaging technique* is applied to obtain the transfer functions that characterize the dynamics of the converter. Once the model is verified, the PFC controller structure is introduced and the design procedure is explained. Finally, the closed-loop response of a 1 kW two-phase interleaved boost PFC converter is analyzed for changes in load dynamics.

3.1 Small-signal model of the boost converter

State-space averaging is a common approach for obtaining a small-signal model (SSM) of the converter. SSMs are time-invariant for a set of working conditions which eases the controller design [1]. Although in PFC converters the input varies sinuoidally, it is possible to obtain the controller's parameters based on the SSM. This is because the converter operates with a slowly moving operating point which implies that the electrical variables exhibit only small variations during one switching period due to the switching frequency being higher than the line frequency ($f_{sw} >> f_{line}$) [20]. All channels of interleaved PFC converters can be controlled independently due to the presence of a switching device in each of them. Thus, an individual controller is used for each channel and only the SSM of a single boost converter is required for designing the controller. Equation 3.1 shows the general expression of state-space equations [1].

$$\begin{aligned} K \cdot \dot{x}(t) &= A \cdot x(t) + B \cdot u(t) \\ y(t) &= C \cdot x(t) + E \cdot u(t) \end{aligned} \tag{3.1}$$

where $x(t) = [i_L(t) \quad v_C(t)]^T$ are the state variables, $u(t) = [v_{in}(t)]$ the input signal and $y(t)$ is any output signal of interest to compute.

Figure 3.1 depicts the equivalent circuit diagram of an ideal non-synchronous boost converter. The power switch and the diode are assumed ideal and the parasitic components are neglected in order to simplify the analysis. The converter has two modes of operation which will be referred as *Mode* 1 when the switch is conducting and *Mode* 2 when the diode is conducting current as shown in Figure 3.2a and 3.2b, respectively.

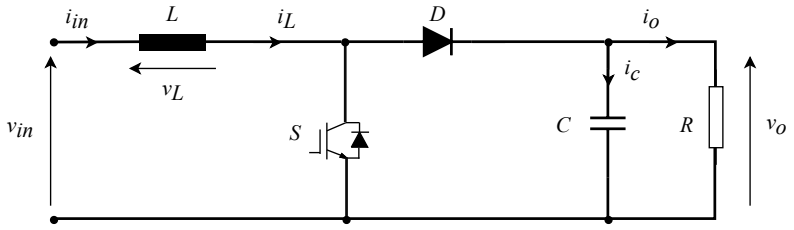
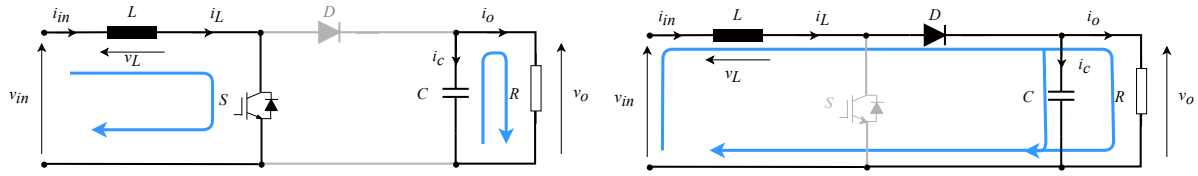


Figure 3.1: Electrical circuit diagram of an ideal non-synchronous boost converter.



(a) Switch Q is ON - *Mode 1*.

(b) Switch Q is OFF - *Mode 2*.

Figure 3.2: Electrical circuit diagram for the two modes of operation of ideal boost converter.

The state-equations for each mode of operation are found from the expressions for inductor voltage and capacitor current, shown in Equation 3.2, by analizing the circuits.

$$v_L(t) = L \cdot \frac{di_L(t)}{dt} \quad ; \quad i_c(t) = C \cdot \frac{dv_c(t)}{dt} \tag{3.2}$$

Mode 1

$$\underbrace{\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}}_{K} \cdot \frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 \\ 0 & -1/R \end{bmatrix}}_{A_1} \cdot \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 1 \\ 0 \end{bmatrix}}_{B_1} \cdot \begin{bmatrix} v_{in}(t) \end{bmatrix} \tag{3.3}$$

Mode 2

$$\underbrace{\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}}_{K} \cdot \frac{d}{dt} \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & -1 \\ 1 & -1/R \end{bmatrix}}_{A_2} \cdot \begin{bmatrix} i_L(t) \\ v_c(t) \end{bmatrix} + \underbrace{\begin{bmatrix} 1 \\ 0 \end{bmatrix}}_{B_2} \cdot \begin{bmatrix} v_{in}(t) \end{bmatrix} \tag{3.4}$$

Equilibrium point

Averaging the state-space equations over one switching period the state matrixes A and B are found. The equilibrium operating point X ($\dot{x}(t) = 0$) is shown in Equation 3.5 from which the voltage and current gain ratios of the boost converter are obtained.

$$X = -A^{-1} \cdot B \cdot U \quad \rightarrow \quad \frac{V_o}{V_{in}} = \frac{1}{1-D} \quad ; \quad \frac{I_o}{I_{in}} = 1 - D \tag{3.5}$$

Small-signal model

In order to obtain a linear model, small AC perturbations are imposed around the equilibrium point. Assuming small perturbations, the small signal linear model is [1]:

$$K \cdot \dot{\hat{x}}(t) = A \cdot \hat{x}(t) + B \cdot \hat{u}(t) + [(A_1 - A_2) \cdot X + (B_1 - B_2) \cdot U] \cdot \hat{d}(t) \tag{3.6}$$

Substituting the state-space matrixes in the previous expression, the SSM of the boost converter is obtained in Equations 3.7 and 3.8.

$$\hat{v}_L(t) = L \cdot \frac{d\hat{i}_L(t)}{dt} = -D \cdot \hat{v}_o(t) + \hat{v}_{in}(t) + V_o \cdot \hat{d}(t) \tag{3.7}$$

$$\hat{i}_c(t) = C \cdot \frac{d\hat{v}_c(t)}{dt} = (1-D) \cdot \hat{i}_L(t) - \frac{\hat{v}_o(t)}{R} + \hat{v}_{in}(t) - I_L \cdot \hat{d}(t) \tag{3.8}$$

Transfer functions

The SSM is expressed in the frequency domain in order to find the transfer functions (TF) required for the controller design. The control-to-output TF, $G_{vd}(s)$ and the control-to-inductor current TF, $G_{id}(s)$ are derived by setting $\hat{u}(s) = 0$ as shown in Equation 3.10.

$$\hat{x(s)} = (sI - A)^{-1} \cdot B \cdot \hat{u(s)} + (sI - A)^{-1} \cdot [(A_1 - A_2) \cdot X + (B_1 - B_2) \cdot U] \cdot \hat{d(s)} \tag{3.9}$$

$$G_{vd}(s) = \left.\frac{\hat{v_o}(s)}{\hat{d}(s)}\right|_{\hat{u}(s)=0} \quad ; \quad G_{id}(s) = \left.\frac{\hat{i_L}(s)}{\hat{d}(s)}\right|_{\hat{u}(s)=0} \tag{3.10}$$

$G_{id}(s)$ is required for the current controller design and for DC-link voltage regulation the voltage-to-current TF, $G_{vi}(s)$, is found from $G_{vd}(s)$ and $G_{id}(s)$ as:

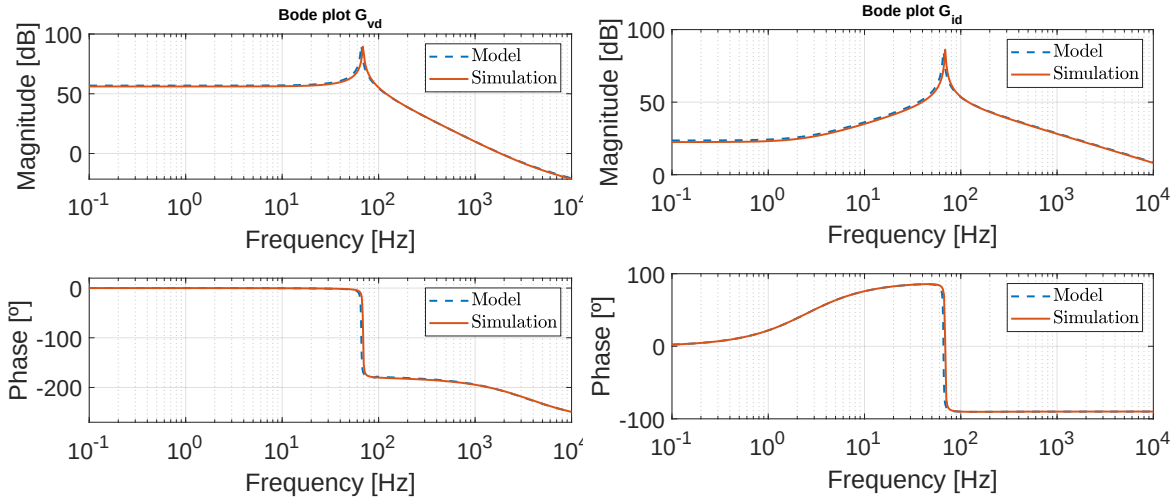
$$G_{vi}(s) = \frac{\hat{v_o}(s)}{\hat{i_L}(s)} = \frac{G_{vd}(s)}{G_{id}(s)} \tag{3.11}$$

These TFs are shown in Equation 3.12, where $D' = 1 - D$. A comparison of the bode plots obtained in simulation and the ones resulting from Equation 3.12 is shown in Figure 3.3.

$$G_{vd}(s) = \frac{V_o LC}{D'} \cdot \frac{1 - \frac{I_L L}{V_o D'} \cdot s}{s^2 + \frac{1}{RC} \cdot s + \frac{D'^2}{LC}}$$

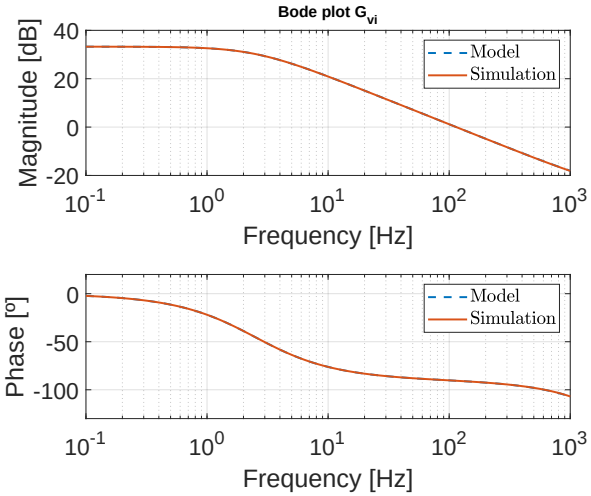
$$G_{id}(s) = \frac{L}{V_o} \cdot \frac{s + \frac{1}{RC} + \frac{I_L D'}{V_o C}}{s^2 + \frac{1}{RC} \cdot s + \frac{D'^2}{LC}} \tag{3.12}$$

$$G_{vi}(s) = \frac{V_o^2 \cdot C}{D'} \cdot \frac{1 - \frac{I_L \cdot L}{V_o \cdot D'} \cdot s}{s + \frac{1}{RC} + \frac{I_L D'}{V_o C}}$$



(a) $G_{vd}(s)$.

(b) $G_{id}(s)$.



(c) $G_{vi}(s)$.

Figure 3.3: Verification of small-signal model of the boost converter.

The model of the boost converter is validated by running AC sweep simulations in *PLECs* to obtain the open-loop frequency response of the system. It is observed that in the three cases the derived model accurately tracks the simulated results for all the frequency range. Therefore, the validity of the boost small-signal model is verified. Once the model is verified, the next section will present the PFC controller structure.

3.2 PFC Controller structure

There are two methods for deriving discrete controllers known as indirect and direct methods [21]. In the direct method the controller is designed directly in the z-domain. The indirect method, commonly named as *Digital Redesign Approach*, consists on designing the controller in the s-domain and, applying discretization techniques, the digital controller is indirectly determined. In this project the indirect approach is selected as the wide knowledge on continuous-time systems eases the design in the frequency domain analysis.

Figure 3.4 shows the block diagram of the digital control scheme for implementation in a Digital Signal Processor (DSP). The main goal of a PFC controller is to achieve accurate output voltage regulation and low line current distortion (high PF). One of the most popular control methods for achieving this goal because of its good dynamic performance, robustness and simplicity is known as average current mode control (ACMC) [3, 8, 22].

ACMC principle is to control the average inductor current to be proportional to the rectified input voltage and, consequently, it will force the line current to be sinusoidal and in phase with the line voltage [8, 23]. From Figure 3.4, it is observed that five feedback signals need to be monitored for implementation of the cascaded digital controller. These are the inductor current for channel 1 (i_{L1}) and channel 2 (i_{L2}), the output voltage (V_o), the ac line ($v_{ac,L}$) and neutral voltages ($v_{ac,N}$). All these currents and voltages are sensed and sent to the DSP in order to be processed by the ADCs.

The cascaded controller consists of two high-bandwidth inner current loops and a low-bandwidth outer voltage loop. The latter is used for regulating the DC bus voltage while the inner control loops are used for controlling the input current in order to maintain high power factor [3, 23]. The sensed output voltage is compared with a constant voltage reference (i.e., $V_{o,ref} = 400\ V$) and the error is fed to the outer voltage controller $G_v(z)$ to generate the reference for the inner current loops. The current reference $i_{L,ref}$ must have the same shape as the rectified voltage in order to force the input current, before the rectifier, to be sinusoidal. Therefore, a multiplier is used to generate the current reference by multiplying the rectified mains voltage by the output of the voltage controller. The rectified voltage is obtained from the difference between the line and the neutral voltages in order to be processed by the DSP.

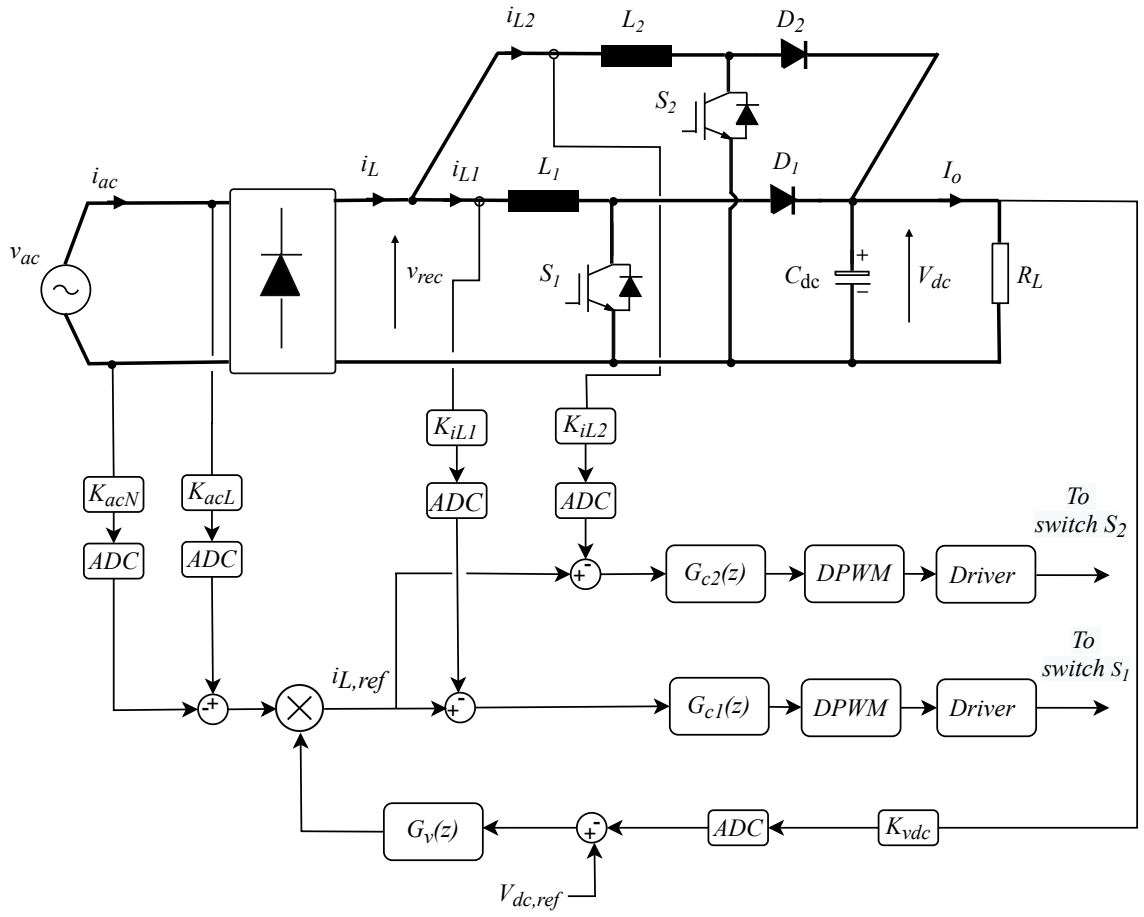


Figure 3.4: Block circuit diagram of digital control of two-phase interleaved PFC boost converter.

The output of each of the inner current controllers is the duty cycle command which is processed by a discrete PWM module ($DPWM$) in order to generate the pulses to drive the gate of the switching devices, S_1 and S_2. In the conventional PFC control of interleaved converters each channel operates with a phase shift of $\frac{360^\circ}{n}$, where n is the number of interleaved cells [23]. The DPWM of one of the interleaved levels generates the gate pulses by comparing the duty cycle with a triangular waveform switching at $f_{sw} = 28\ kHz$. In a similar way the second DPWM sends the gate pulses to the driver of S_2 which operates with a phase shift of 180° with respect to S_1.

In the following subsections the requirements for each of the control loops and the design procedure for obtaining the discrete controllers $G_v(z)$, $G_{c1}(z)$ and $G_{c2}(z)$ is explained. The controllers for the three current modes (CCM, QCM, DCM) are designed in a similar manner. The detailed explanation for the CCM controller design will be shown and, in Table 3.2, the controller parameter's obtained for each current modulation are shown.

3.2.1 Current controller design

The inner current loop bandwidth should be much higher than the BW of the outer voltage controller in order to avoid interactions between the control loops. $i_{L,ref}$ is a rectified waveform with frequency $2 \cdot f_{line} = 100\ Hz$. Hence, to accurately track the current reference, the current controller should have wide BW. According to [24], accurate tracking is achieved by selecting the crossover frequency in the range: $2 \cdot f_{line} \leqslant f_c < f_{sw}/2$.

The crossover frequency for the current controller is chosen to be $f_c = 8\ kHz$, when switching at 28 kHz, in order to obtain a fast dynamic performance of the inductor current. Also, the overshoot should not exceed 20% ($M_p < 20$ %) in order to avoid high peak transient currents for sudden load changes. $G_{c1}(s)$ and $G_{c2}(s)$ have the same parameters and are designed based on the bode plot response of the uncompensated loop by applying frequency response analysis. The controllers are designed in *MATLAB/Sisotool* environment by tuning the controller parameters. Equation 3.13 shows the obtained PI controller that fulfills the current controller requirements for CCM.

$$G_{c1}(s) = G_{c2}(s) = Kp, c + \frac{K_{i,c}}{s} = 0.595 + \frac{9494}{s} \tag{3.13}$$

Figure 3.5 shows the open-loop bode plots for the uncompensated ($T_{u,i}(s) = G_{id}(s)$) and compensated loop ($T_{c,i}(s) = G_{id}(s) \cdot G_{c1}(s)$). $T_{c,i}(s)$ has high low-frequency gain in comparison with $T_{u,i}(s)$ and the resultant BW is reduced to 8 kHz. Moreover, the phase margin is $PM = 72.1^{\circ}$ which leads to a maximum overshoot of $M_{p,c} = 16.5\%$.

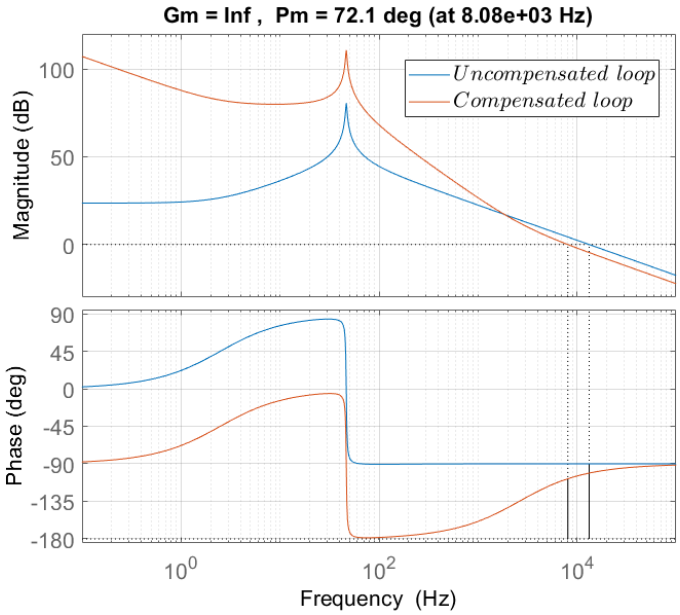


Figure 3.5: Bode diagram compensated and uncompensated current control loop.

Since the controller is to be implemented in a DSP, it is necessary to perform the discretization of the continuous controller. The bilinear transformation, also known as Tustin method, is applied to $G_{c1}(s)$ to derive the discrete current controllers.

$$G_{c1}(z) = G_{c2}(z) = G_{c1}\left(s = \frac{2}{T_s} \cdot \frac{z-1}{z+1}\right) = \frac{0.665 \cdot z - 0.495}{z-1} \tag{3.14}$$

When implementing the digital redesign approach, special attention is given to the computational time delay and the selection of sampling frequency (f_s) used during the discretization process. The selection of f_s is based on the highest BW of the system according to the Nyquist criterion. It states that the sampling frequency should be greater than at least twice the highest system's frequency to be sampled [21]. In order to avoid aliasing, a good choice is to select the sampling period in the range:

$$5 \cdot f_c \leqslant f_s \leqslant 100 \cdot f_c \;\rightarrow\; 40kHz \leqslant f_s \leqslant 800kHz \tag{3.15}$$

where $f_c = 8\ kHz$ is the crossover frequency of the fastest loop in the system. A sampling frequency of 56 kHz ($f_s = 2 \cdot f_{sw}$) is selected and the delay caused by the sampling time, the computation time of the ADCs and the time for the duty cycle update of the DPWMs also needs to be considered [25]. A delay of one sampling period ($T_{delay} = T_s$) is included when verifying the discrete controller in simulation.

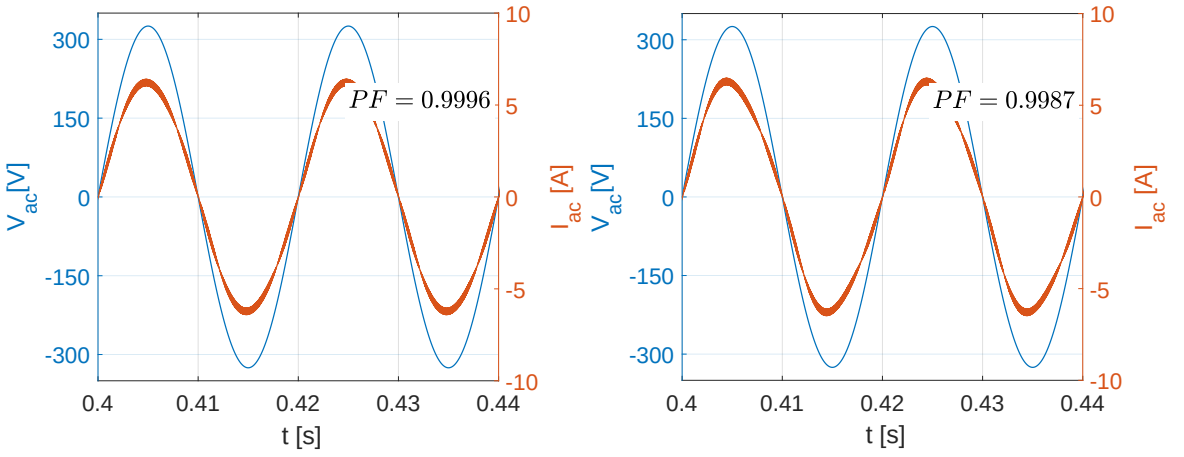
3.2.2 Voltage controller design

The voltage loop must be slow enough (i.e., low-bandwidth) to minimize the line current distortion but, at the same time, the controller should be able to track the output voltage reference fast enough for step changes in load [3, 8, 22]. Due to the presence a second-harmonic component (100 Hz) in the output voltage, the voltage controller BW is usually restricted to a maximum of 20 Hz (typically in the range $10 - 20$ Hz) [22].

However, it exists a strong trade-off between high PF and fast output voltage transient response [26]. The faster the voltage controller is, the higher the distortion in the line current. Therefore, the controller parameters were found by iterations in simulations in order to obtain an appropiate BW.

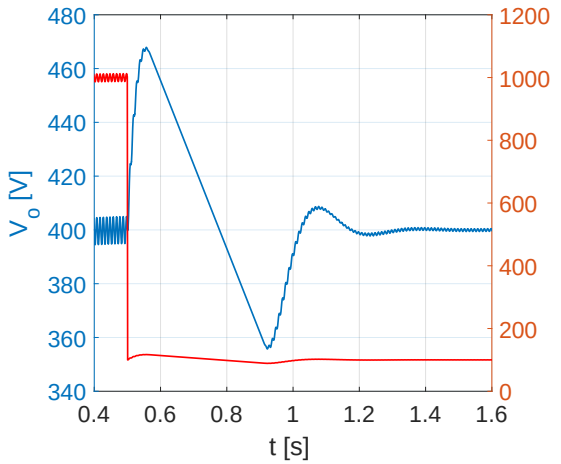
This is reflected in Figure 3.6 where a comparison of PF and output voltage regulation is shown for two different voltage controller's BW (i.e., 3Hz and 8Hz). If the BW of the voltage controller is lowered, the line current is more in phase with the line voltage resulting in higher PF. However, the output voltage variation is very significant when a sudden step change from $P_o = 1000\ W$ to $P_o = 100\ W$ is applied (worst case scenario). Figure 3.6c shows that with $BW_v = 3Hz$ the transient peak voltage is approximately 470 V, exceeding the rating of the DC-link capacitors. Also, the time the output voltage takes to stabilize is around one second while with $BW_v = 8Hz$ it is reduced to approximately 0.3

seconds. The consequence of having a faster system is that the line current is distorted, as shown in the current bending of Figure 3.6a. If the BW is increased beyond 8 Hz the PF is significantly reduced even though fast voltage regulation is obtained. Therefore, a compromise between PF and system speed need to be accepted. It was found that selecting $BW_v = 8\ Hz$ gives good transient response without significantly affecting the PF. The maximum overshoot requirement is set to $M_{p,v} = 10\%$ in order to ensure that the transient voltage will not exceed the DC-link capacitors rating, which is 450 V.

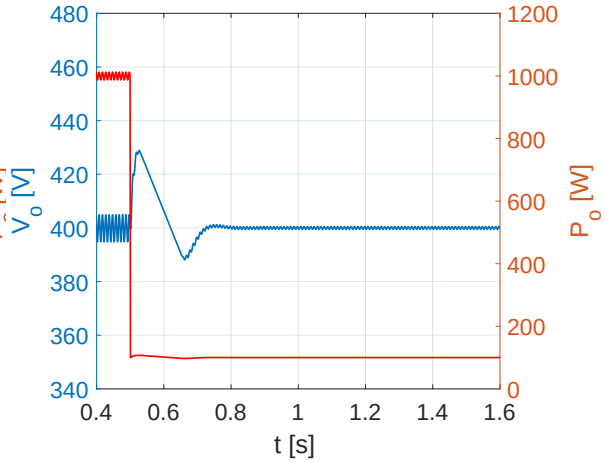


(a) $v_{ac}(t)$ and $i_{ac}(t)$ @ $BW_v = 3\ Hz$.

(b) $v_{ac}(t)$ and $i_{ac}(t)$ @ $BW_v = 8\ Hz$.



(c) V_o and P_o @ $BW_v = 3\ Hz$.



(d) V_o and P_o @ $BW_v = 8\ Hz$.

Figure 3.6: Comparison of PF and output voltage response to load from 100%-10% rated power with voltage controller bandwidth of 3 Hz and 8 Hz.

Table 3.1 summarizes the parameters used for defining the design operating point and also the current and voltage controller requirements.

Parameters for PFC controller design		
Operating conditions	Parameter	Value
Input voltage	V_{in}	230 V
Output voltage	V_o	400 V
Output power	P_o	1 kW
Switching frequency	f_{sw}	28 kHz
Sampling frequency	f_s	56 kHz
Controller requirements	Parameter	Value
Bandwidth current loop	BW_c	8 kHz
Bandwidth voltage loop	BW_v	8 Hz
Max. overshoot current loop	$M_{p,c}$	20 %
Max. overshoot voltage loop	$M_{p,v}$	10 %

Table 3.1: Electrical parameters and requirements for PFC controller design.

With the voltage loop requirements defined, the block diagram of the cascaded controller is depicted in Figure 3.7. The closed-loop transfer function of the inner current loop is included in the plant for the voltage controller design ($G_{v,plant} = G_{cl,i} \cdot G_{vi}$). Note the saturation block after the voltage controller which is essential in order to limit the current reference command I_{ref}. This is due to the big difference that exists in large signal transient (i.e., startup) between the measured output voltage V_o and the reference $V_{o,ref}$ [25]. This huge difference might result in a very high current command which could exceed the current rating of the electronic devices and damage the converter.

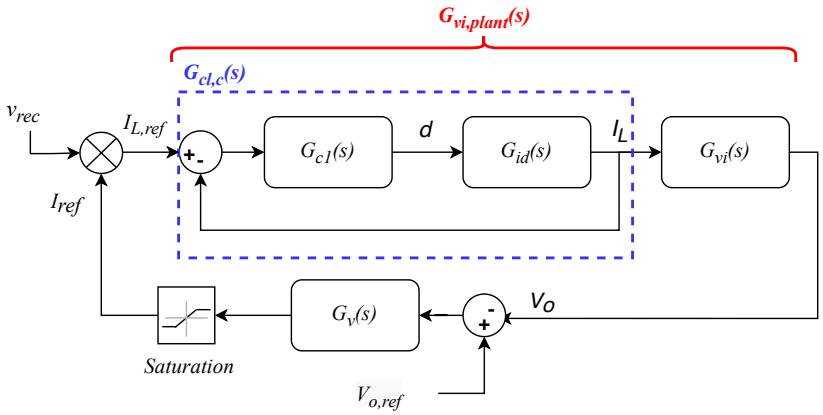


Figure 3.7: Block diagram of the cascaded controller showing the current and voltage loops.

In Equation 3.16 the PI voltage controller which meets the design requirements for working in CCM is shown. Applying Tustin transformation, the voltage controller is discretized resulting in the digital controller of Equation 3.17.

$$G_v(s) = Kp, v + \frac{K_{i,v}}{s} = 0.06 + \frac{2.112}{s} \tag{3.16}$$

$$G_v(z) = G_v\left(s = \frac{2}{T_s} \cdot \frac{z-1}{z+1}\right) = \frac{0.06 \cdot z - 0.059}{z-1} \tag{3.17}$$

The open-loop response of the compensated and uncompensated loop is depicted in Figure 3.8. It is seen that the BW has been decreased in comparison with the uncompensated loop and the crossover frequency is at $f_c = 8Hz$. The maximum overshoot requirement is also satisfied resulting in $M_{p,v} = 9.56\%$ which corresponds to $PM = 72^\circ$.

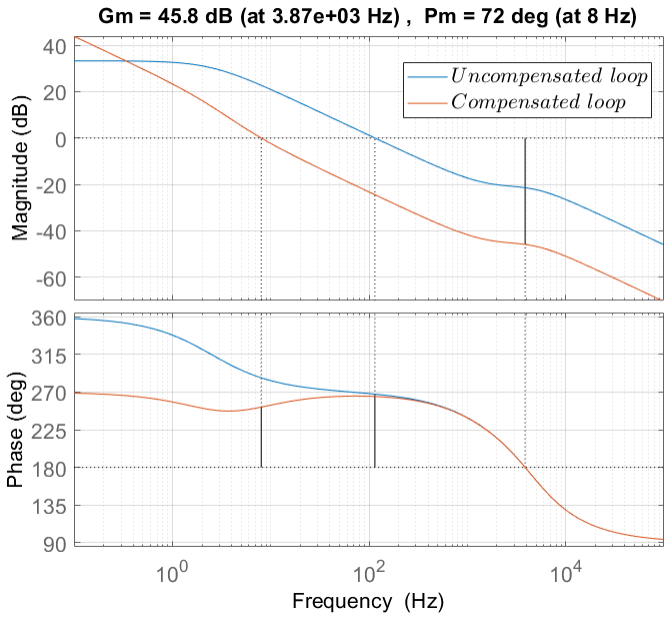


Figure 3.8: Bode diagram compensated and uncompensated voltage control loop.

3.3 Simulation results

As mentioned previously, the controllers for QCM and DCM operation were designed following the same procedure but with a different value of inductance for the plant TFs. In Table 3.2, the resulting current and voltage controller parameters are shown.

PFC controller parameters			
	CCM (L = 4.8 mH)	QCM (L = 0.8 mH)	DCM (L = 0.35 mH)
$K_{p,c}$	0.595	0.1	0.04
$K_{i,c}$	9494	1594	652
$K_{p,v}$	0.06	0.06	0.06
$K_{i,v}$	2.112	2.112	2.112

Table 3.2: PFC controller parameters for CCM, QCM and DCM.

The digital controller is verified by simulations for different load changes in order to validate the PFC converter dynamic performance through the full power range ($100 - 1000\ W$). The two-channel interleaved boost PFC is simulated with the corresponding controller parameters for CCM, QCM and DCM from Table 3.2. The simulation is done in the three cases for the following loading profile:

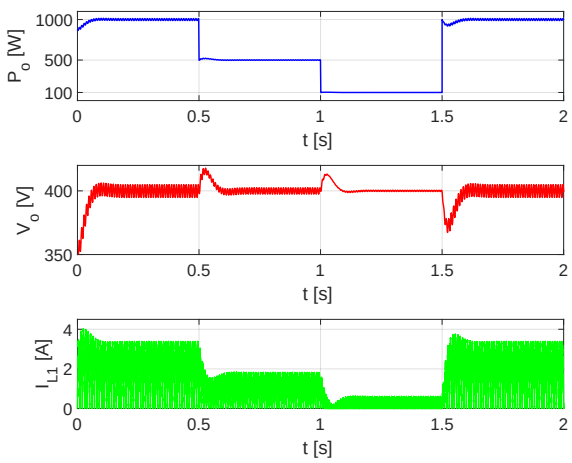
- Initially, $t = 0$, the interleaved PFC converter is running at full-load, $P_o = 1\ kW$.
- At instant $t = 0.5\ s$ a step change from full-load to half-load is applied, $P_o = 500\ W$.
- Then, at $t = 1\ s$ the load is increased to work at 10 % of rated power, $P_o = 100\ W$.
- Finally, a load change $10 - 100\%$ of rated power is applied at $t = 1.5\ s$, $P_o = 1\ kW$.

By comparing the simulation results for CCM, QCM and DCM, the corresponding transient response in each case is the same. This is because the parameters of the controllers are designed to maintain the same bandwidth in order to compare its performance. The controller's requirements are specified in Table 3.1.

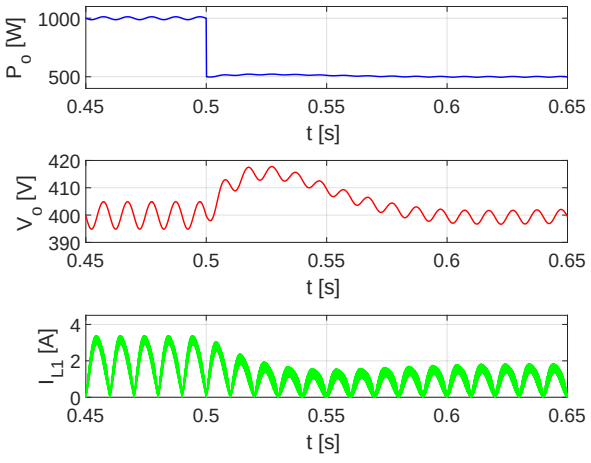
Figures 3.9, 3.11 and 3.14 show the simulated response of the two-channel interleaved boost PFC converter with ACMC digital controller implemented working in CCM, QCM and DCM, respectively. The controllers are designed at full load according to the specifications in Table 1.1.

CCM

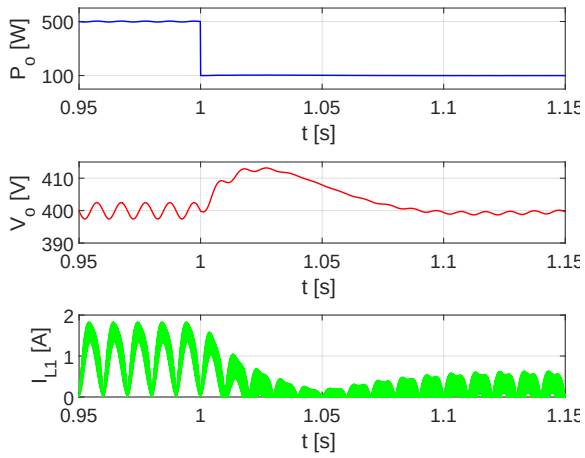
Figure 3.9 shows the step changes in output power and the output voltage and inductor current response to these changes in load for a two-channel interleaved PFC converter designed to operate in CCM. A zoomed view of the transient responses is depicted in Figures 3.9b - 3.9d showing that the current controller is able to control the inductor current to work in CCM for a wide range of output power levels (i.e., up to half of the rated load). However, at 10% of rated output the selected inductance value ($L_{CCM} = 4.8mH$) is not enough to keep the converter in CCM which is why maintaining CCM operation at low powers is not feasible as the inductance required would lead to a huge inductor.



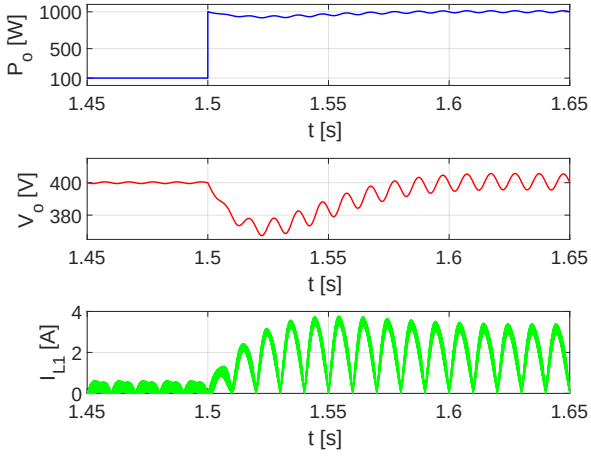
(a) P_o, V_o and I_{L1}.



(b) Zoom transient $1000 - 500$ W.



(c) Zoom transient $500 - 100$ W.

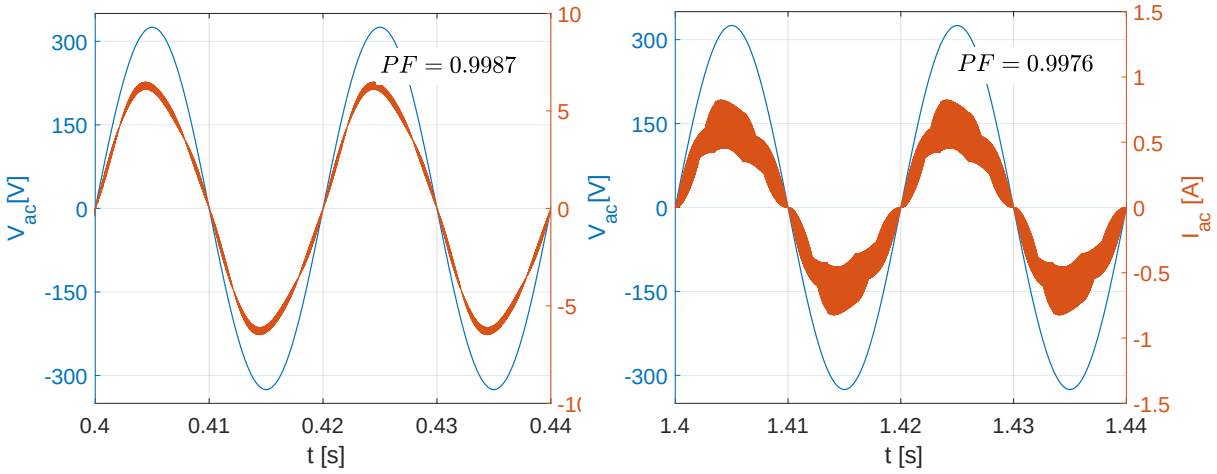


(d) Zoom transient $100 - 1000$ W.

Figure 3.9: Output power, output voltage and inductor current for CCM two-channel interleaved PFC under step load changes (a) 100% - 50% - 10% - 100% showing a zoom view of (b)-(d) the step transient response, based on the specifications of Table 1.1.

It is shown from the simulations that in the three cases (CCM, QCM and DCM) the maximum output voltage variation is 27.3 V ($M_p = 6.8\%$) which takes place for a load step from $100 - 1000$ W. This fulfills the maximum 10% overshoot requirement for the voltage compensator. For this maximum load variation the settling time is $T_{settling} = 93ms$, following the 2% criterion. Therefore, the voltage controller can regulate fast enough the output voltage at 400 V for increase and decrease of output power level. Also, the overshoot of the inductor current is lower than the requirement of 20%.

Figure 3.10 shows the AC line input voltage and current during two line cycles in order to verify the power factor correction at full and low power conditions. Figure 3.10a shows that the line current and voltage are in phase and, at full load, the power factor is $PF = 0.9987$ while at 10% load, Figure 3.10b, it slightly decreases to $PF = 0.9976$.



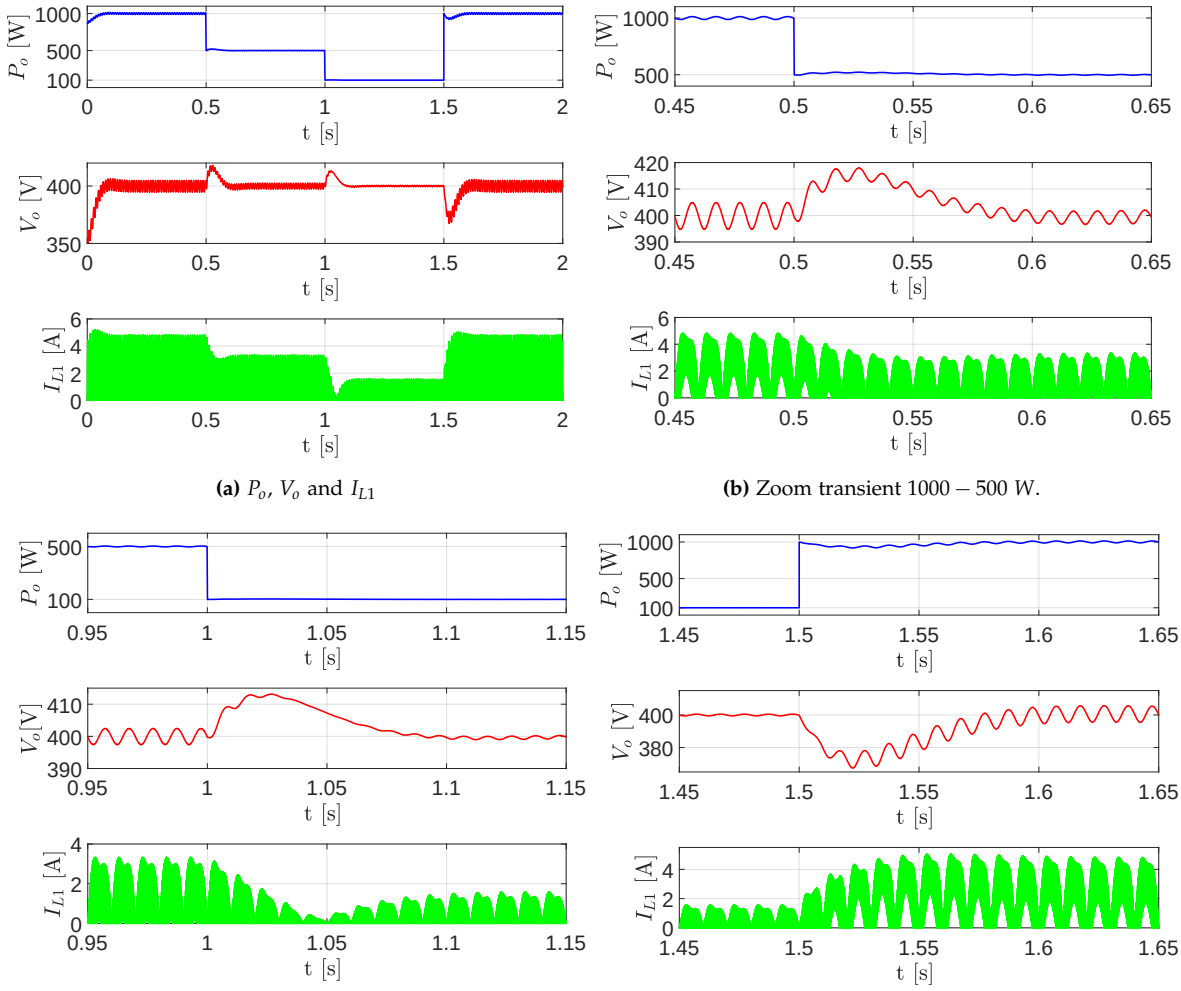
(a) $v_{ac}(t)$ and $i_{ac}(t)$ @ 100% load.

(b) $v_{ac}(t)$ and $i_{ac}(t)$ @ 10% load.

Figure 3.10: Line voltage and current at (a) 100% and (b) 10 % rated load for CCM two-channel interleaved PFC, based on the specifications of Table 1.1.

QCM

For the case of QCM it is seen that at rated load the inductor current is partial CCM going towards full DCM operation as the load decreases. At rated load the inductor current is in the mixed conduction mode working half of the line cycle in CCM and the other half in DCM. This is because the inductor in QCM was designed to start operating in CCM at $\alpha = 45^{\circ}$. As mentioned previously, the dynamic response is the same for the three current modulation as the controllers have the same requirements and the system specifications stated in Table 1.1.



(a) P_o, V_o and I_{L1}

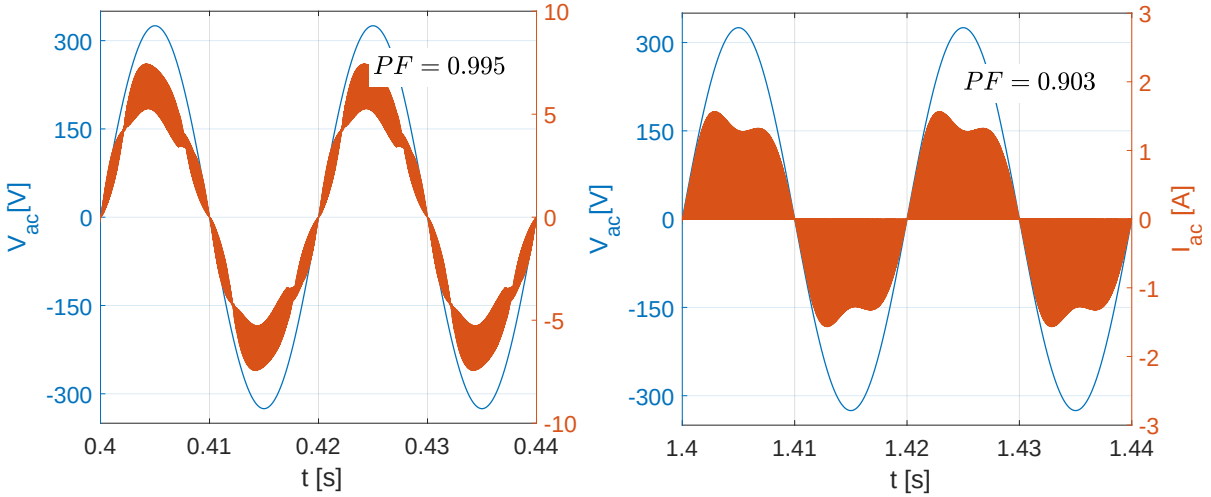
(b) Zoom transient $1000 - 500$ W.

(c) Zoom transient $500 - 100$ W.

(d) Zoom transient $100 - 1000$ W.

Figure 3.11: Output power, output voltage and inductor current for QCM two-channel interleaved PFC under step load changes (a) 100% - 50% - 10% - 100% showing a zoom view of (b)-(d) the step transient response, based on the specifications of Table 1.1.

As shown in Figure 3.12, when the system is designed to operate in QCM, the resulting line current presents higher ripple than in CCM. Nevertheless, the PFC controller is still able to force the line current to be in phase with the line voltage. As expected the power factor is higher at $P_o = 1000$ W than at $P_o = 100$ W as the input current presents higher distortion due to the increase in ripple input current when working in DCM.



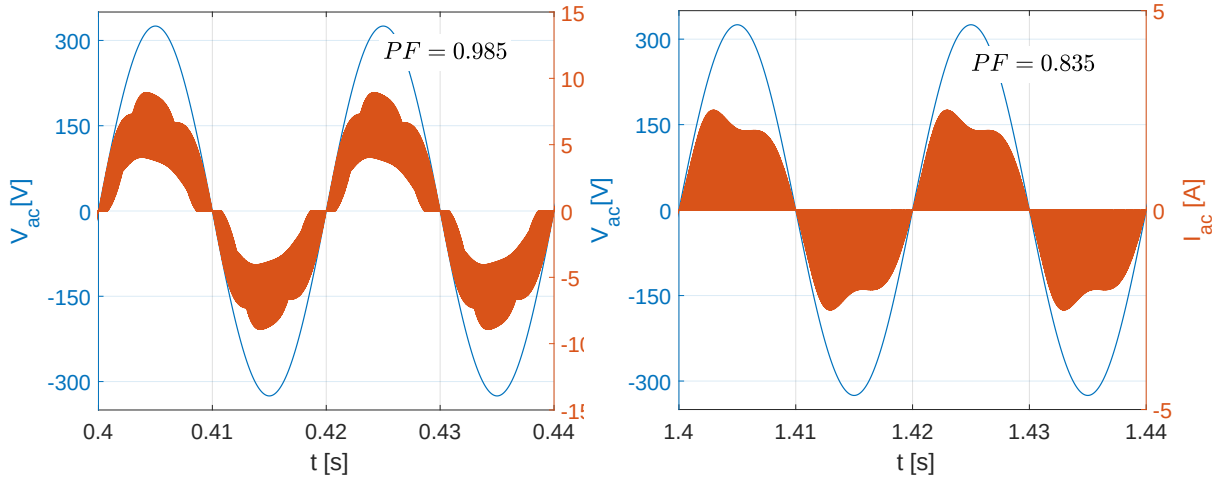
(a) $v_{ac}(t)$ and $i_{ac}(t)$ @ 100% load.

(b) $v_{ac}(t)$ and $i_{ac}(t)$ @ 10% load.

Figure 3.12: Line voltage and current at (e) 100% and (f) 10 % rated load for QCM two-channel interleaved PFC, based on the specifications of Table 1.1.

DCM

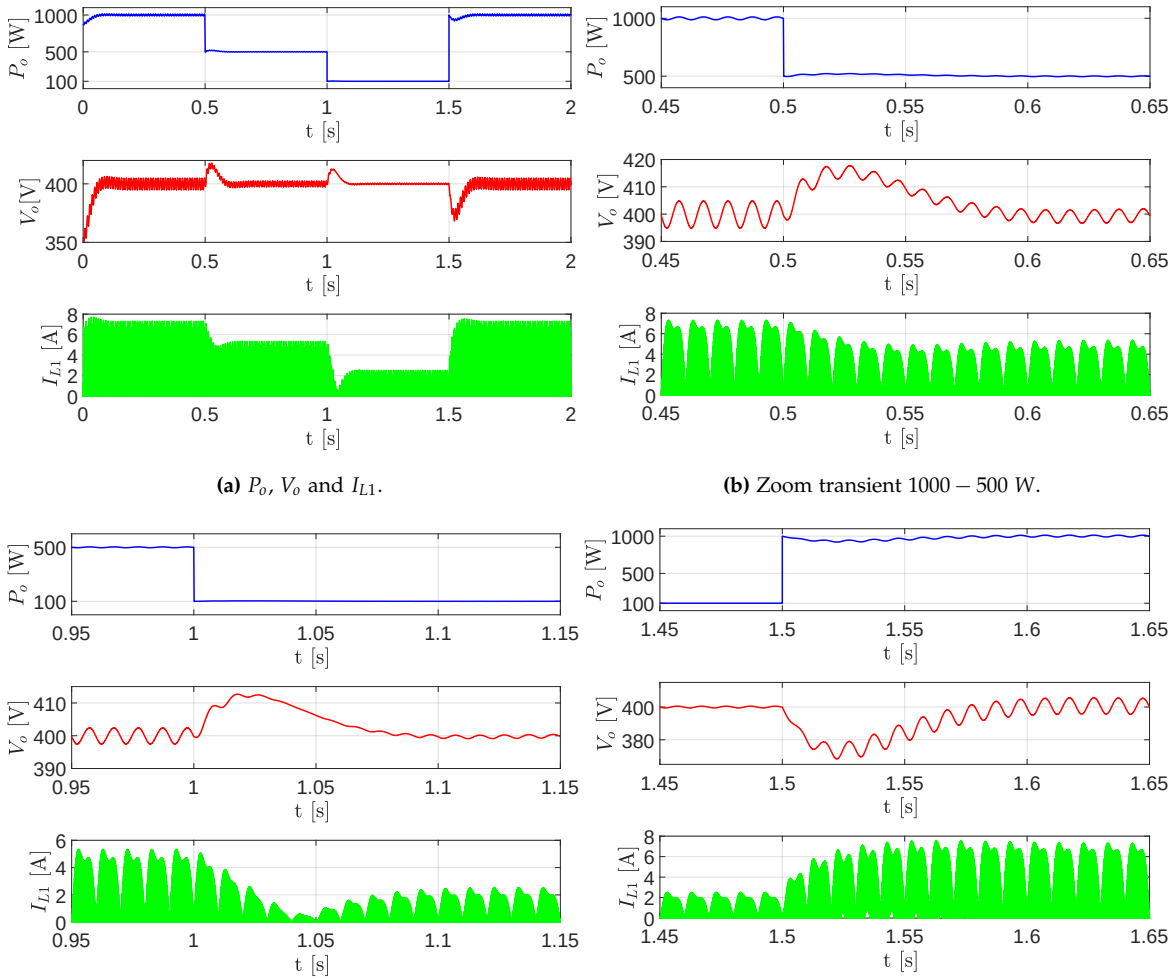
Figure 3.13 shows that the resulting PF is lower than in CCM and QCM due to the high peaks due to the discontinuous inductor current. However, the controller is able lo put in phase the AC current with the voltage. Figure 3.14 shows that for all power levels the converter operates in DCM as the minimum inductance was selected at rated power.



(a) $v_{ac}(t)$ and $i_{ac}(t)$ @ 100% load.

(b) $v_{ac}(t)$ and $i_{ac}(t)$ @ 10% load.

Figure 3.13: Line voltage and current at (e) 100% and (f) 10 % rated load for DCM two-channel interleaved PFC, based on the specifications of Table 1.1.



(a) P_o, V_o and I_{L1}.

(b) Zoom transient $1000 - 500$ W.

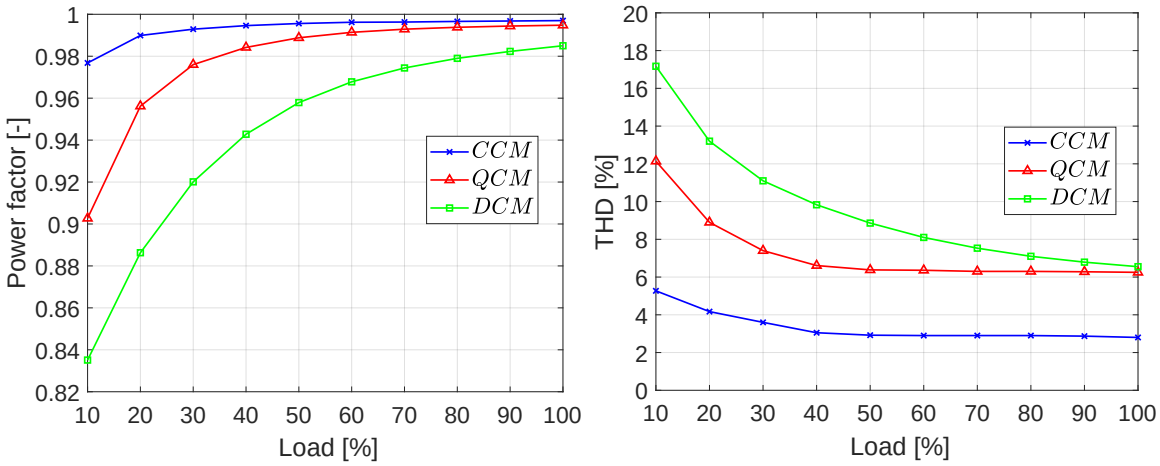
(c) Zoom transient $500 - 100$ W.

(d) Zoom transient $100 - 1000$ W.

Figure 3.14: Output power, output voltage and inductor current for DCM two-channel interleaved PFC under step load changes (a) 100% - 50% - 10% - 100% showing a zoom view of (b)-(d) the step transient response.

A comparison of PF and THD achieved using each current modulation is depicted in Figures 6.12a and 6.12b, respectively. Simulations are carried out for different load conditions from $10 - 100\%$ of rated power. It can be seen that the PF is lower at low load conditions while it increases towards full load in the three cases with CCM yielding the best performance in regards to PF. Although in the medium to high load range the PF of CCM and QCM is comparable as in both cases it is higher than 0.99.

On the other hand, the THD is more significant at light loads while it achieves its minimum at rated power $P_o = 1\ kW$. Due to the high switching ripple in the inductor current when working in DCM and QCM the THD is higher than CCM.



(a) PF vs Load

(b) THD vs Load

Figure 3.15: Comparison of PF and THD for two-channel interleaved PFC working in CCM, QCM and DCM.

Therefore, CCM gives the best performance in regards to PF and THD over the full load range. However, other factors need to be considered for a fair comparison between this modulations techniques such as the EMI filter required, boost inductor volume and the total converter efficiency and power density.

Chapter 4

PCB design of interleaved boost PFC

This chapter covers the component selection for the interleaved boost PFC converter under study. This includes the components needed for signal processing, the capacitors for high-frequency noise filtering, RC snnubers and sensors. Also the heatsink selection based on an analytical power loss calculation and thermal model is introduced. Lastly, some PCB layout considerations for the 1 kW two-channel interlaved PFC converter are presented.

4.1 DIPIPM for PFC applications

The use of intelligent power modules in PFC applications, also known as Dual-In-Line Package Power Factor Correction (DIPPFC), has become an area of interest for harmonic suppression of power supply of inverters [27]. This is due to several reasons:

- Very compact design as it integrates two interleaved boost cells and its corresponding driver circuitry in the same package. Figure 4.1 shows the Super mini hybrid DIPPFC (Si IGBTs/ SiC diodes) used for this project which size is only $38mm\ x\ 24mm$.
- The use of wide band gap (WBG) materials for the power devices allows high speed operation and reduction of overall losses. The Super mini DIPIPM series from Mitsubishi has full SiC chopper circuits up to 40 kHz and also hybrid modules up to 30 kHz switching frequency.
- DIPPFC includes protection and system control features as fault detection of over-current (OC) in IGBTs and under-voltage (UV) of control supply.
- The package flatness surface area eases the implementation of the heatsink and it can be placed on top of several discrete packages connected in parallel to obtain higher number of interleaved channels.

Figure 4.1 shows the application circuit with the internal block diagram of the hybrid DIPPFC. The Low-Voltage IC (LV IC) receives as input the PWM signals from the microprocessor and the integrated drivers generate the gating signals for the IGBTs. It also sends a fault output signal to the DSP when an OC or UV event occurs.

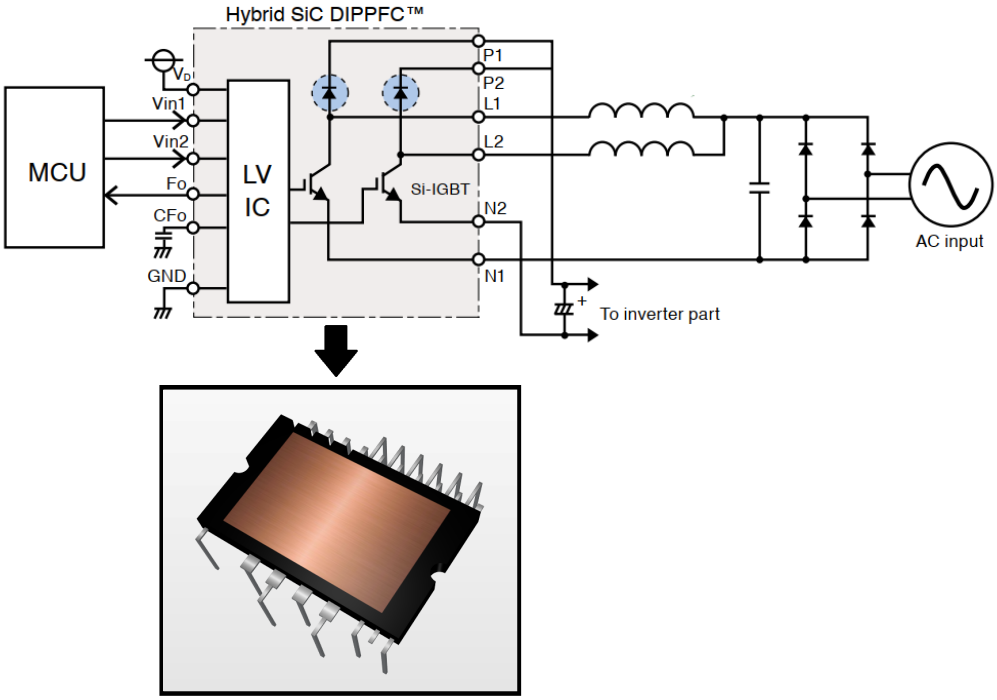


Figure 4.1: Two-channel interleaved PFC circuit configuration for hybrid DIPPFC from Mitsubishi [27].

4.1.1 Signal processing

From the interleaved PFC circuit schematic in Appendix **??**, the external components included for signal processing are shown. These can be divided in three modules: PWM filter, Fault detection and Control supply, listed below.

- **PWM filter** module consists of the input interface circuit between the microprocessor and the DIPPFC. PWM signals are pulses with varying duty cycle which have several harmonics present in their spectrum. Thus, two first-order low-pass filters (LPF), $R4 - C6$ and $R5 - C7$, are used to prevent high frequency noise in the gating signal [28]. The selection of the cut-off frequency f_c is a trade-off between frequency attenuation and driver transient response. It is decided to select f_c one decade over the maximum harmonic of the PWM signal (i.e., 3rd harmonic).

- **Fault output detection** module is referred to the components used for protection. It consists of two shunt resistors, R_1 and R_2, used to measure the current through the IGBTs in order to detect if the current goes beyond its rating. The sensed voltage of the resistors is fed back to the LVIC to output a low pulse F_o to the DSP, in case of OC. RC filters, $R_6 - C_9$ and $R_7 - C_{10}$, are placed in the feedback to ensure the operation of the OC protection.

- **Control supply** module includes a ceramic capacitor $C_3 = 1nF$ and an electrolytic capacitor $C_4 = 100\mu F$ placed in parallel for noise reduction of the control supply voltage ($V_D = 15\ V$). These capacitors should have good high-frequency characteristics in order to remove the high-frequency components of the control signal and obtain an stable supply for the drivers. Also a zener diode Z_1 is added for protection against surge voltages at the control supply input pin of the DIPPFC.

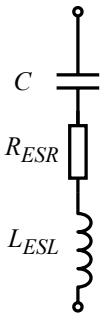
4.1.2 Capacitors selection

Electrolytic capacitors are commonly used as filters at the output of power converters for limiting fluctuations in the DC bus due to their high capacitance for energy storage. The drawback of electrolytic capacitors is their inherent large Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) which leads to poorer response at high frequencies. These parameters are part of the capacitor equivalent model shown in Figure 4.2. High ESR will lead to increase in power losses ($P_{dis,C} = R_{ESR} \cdot I_c^2$) while the spikes that appear in the output voltage are mainly caused by the ESL. This is because the capacitor starts loosing its capacitance behaviour at the point determined by the resonance frequency (f_r) and the EMI that results from switching noise is higher. The influence of ESR and ESL in the impedance characteristics of electrolytic and film capacitors is depicted in Figure 4.3 for comparison purposes.

The value of R_{ESR} corresponds to the impedance at the resonant frequency and it is significantly reduced for film capacitors. When the frequency exceeds the resonant frequency, defined in Equation 4.1, the impedance starts increasing and the capacitor's behaviour changes to inductive. From the definition of f_r it is shown that lower values of capacitance and L_{ESL} lead to an increase in resonant frequency which is required for reducing high-frequency noise.

$$f_r = \frac{1}{2 \cdot \pi \sqrt{L_{ESL} \cdot C}} \tag{4.1}$$

Film capacitors are preferred for removing noise and electrolytic capacitors for low-frequency due to its inherent higher energy density [29]. A very common practice is to obtain the required DC-link capacitance by paralleling electrolytic and film capacitors in order to exploit the advantages of both. This way it is possible to obtain low impedance over a wide range of frequency and large capacitance for energy storage.



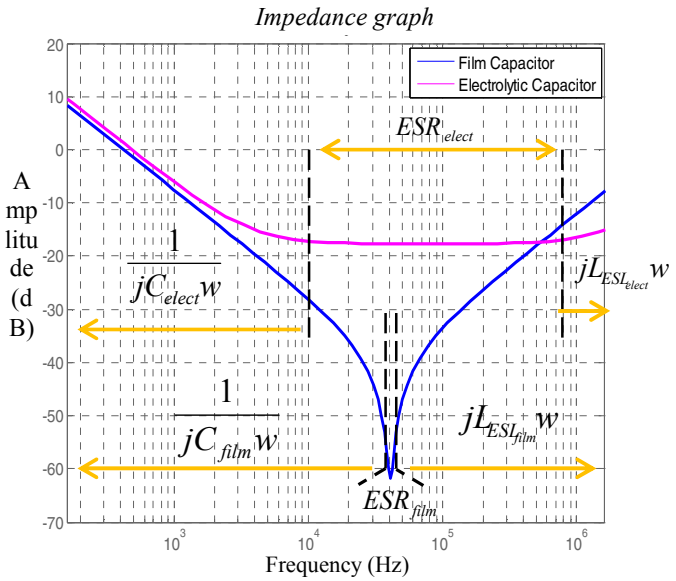


Figure 4.2: Capacitor equivalent model. **Figure 4.3:** Impedance characteristics of electrolytic and film caps [30].

The required DC-link capacitance is $C_o = 800\ \mu F$. Figure 4.4 shows the simulated output voltage V_o when using two 470 μF electrolytic capacitors in parallel in order to obtain overall lower ESR and allow the RMS ripple current to be spread across them.

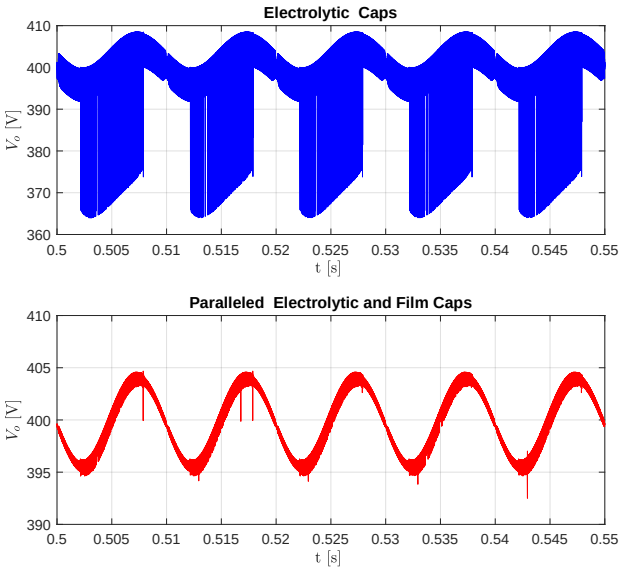


Figure 4.4: Simulated output voltage $V_o(t)$ with *Top*: $2x470\mu F$ electrolytic capacitors and *Bottom*: $2x470\mu F$ electrolytic capacitors in parallel with $1x5\mu F$ and $2x0.1\mu F$ film capacitors.

High voltage spikes appear due to the previously mentioned shortcomings. Thus, with the purpose of reducing EMI, it is found that a combination of three film capacitors ($1x5\mu F$ and $2x0.1\mu F$) in parallel with the electrolytic capacitors results in a significant reduction of the voltage spikes.

It is also recommended to include a capacitor at the output of the bridge rectifier as shown in Figure 4.1. The purpose of this capacitor is to prevent high-frequency noise coming from the rectified voltage to reaching the DIPPFC. Care must be taken when selecting this capacitor because a high capacitance can cause a significant phase-shift at the fundamental frequency which may result in worse PFC [31]. Due to the advantages of film capacitors, it was decided to use a $33nF$ film capacitor ($C_5 = 33\ nF$) which was verified by simulation that did not cause a significant delay to affect the PFC converter operation.

4.1.3 Inrush current protection

The presence of internal capacitance connected across the input and output of the PFC boost converter requires high-peak current for charging these capacitors when the system is initially powered, termed as inrush current. If not considered, it can reduce the power converter reliability, as it can exceed the current rating of connectors, PCB traces and nominal load. There are different methods for mitigating the inrush current either implemented in hardware or by control digitally. In this project, the inrush current protection is implemented in hardware by placing a 600 V diode (D1 in schematic Appendix **??** between the output of the bridge rectifier and the output capacitor bank. This way during start-up the inrush diode $D1$ will conduct and charge the output capacitor before the switching devices start operating.

4.1.4 RC snubbers

In order to reduce voltage and current spikes appearing in power devices during switching operations, snubber circuits are used. The most common topology consists of an RC network connected in parallel with the switching device. Besides limiting dI/dt and dV/dt, RC snubbers also help to reduce the switching losses and the EMI caused by voltage and current ringing [32]. Four basic RC snubbers are included in the design for the two IGBTs and the two diodes of the interleaved boost PFC.

The sizing of the snubbers is done following analytical approximations which lead to an acceptable "first guess" of the value of R_s and C_s according to [32]. Typical values for the snubber capacitor C_s are chosen in the range of $3 - 10$ times the capacitance being damped, $3 \cdot C_{oss} \leqslant C_s \leqslant 10 \cdot C_{oss}$, for the case of an IGBT (i.e., junction capacitance C_T for diodes). Higher C_s yields to improved damping although also an increase of the power dissipated in R_s. Thus, it was decided to select $C_s = 10 \cdot C_{oss}$ and then calculate the power dissipation in R_s ($P_{R_s} = C_s \cdot V_{ce}^2 \cdot f_{sw}$) to find the power rating for R_s selection.

V_{ce} is also subject to ringing for which it is preferred to use low impedance capacitors, mainly low ESL. Ceramic capacitors are used for the snubber capacitors due to their high

self-resonant frequency. The ringing frequency f_o and the characteristic impedance Z_o of the network are expressed in Equation 4.2. $L_{parasitic}$ accounts for the parasitic internal inductance of the IGBT and the parasitic inductance due to PCB layout.

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{parasitic} \cdot C_s}} \quad ; \quad Z_o = \sqrt{\frac{L_{parasitic}}{C_s + C_{oss}}} \tag{4.2}$$

The selection of R_s will influence the peak voltage seen by the IGBT. Usually, R_s is selected based on the characteristic impedance, $Zo \leqslant R_s \leqslant 2 \cdot Z_o$, in order to obtain $V_{ce,pk} < 2 \cdot V_{DC}$. $R_s = 1.4 \cdot Z_o$ is selected and the time constant of the RC network is analyzed and the snubber resized if required. As a rule of thumb, $\tau_{max,R_sC_s} \leqslant 0.1 \cdot t_{on,min}$ in order to ensure that the voltage across Cs is approximately zero during the turn-on of the switch. Similarly, for the design of the RC snubbers for the two boost diodes, the same process was followed but considering the junction capacitance C_T for the selections of C_s.

4.2 Sensors

This section provides an overview of the design of the current sensors, input and output voltage sensors required for the PFC controller. In order to ensure physical modularity these sensors are implemented in separate PCBs and are connected to the main PCB using board-to-board connectors.

4.2.1 Current sensor

PFC converters demand a sinusoidal input current in phase with the input voltage, hence the inductor current must be accurately measured and reproduced. The current of each interleaved boost inductor, i_{L1} and i_{L2} need to be sensed for the inner current control loop. Moreover, the rectified i_{rec} current is also monitored. In normal operating conditions, the peak input current I_{in_pk} is 6.15 A. Peak to peak current is then 12.3 A. So, including a safety margin, a current sensor with nominal current of 15 A (RMS) has been chosen.

In this work, CMS3015 Highly Dynamic Magneto Resistive Current Sensor from *SENSITEC GmBH* with high bandwidth is used, enabling the current control to be performed at high dynamics. Current sensing network is shown in Schematic A.1. The circuit configuration is suggested in current sensor datasheet [33]. The current sensor requires of a bipolar 15 V power supply. To prevent voltage drops in situations of sudden load changes the sensor is buffered by 47 μF electrolytic capacitors, C1 and C2. Additionally, two more ceramic capacitors, C3 and C4, are added for noise rejection in parallel with C1 and C2 respectively. The current sensor's internal structure results in a compensation current proportional to the magnetic field gradient caused by the primary current. The internal burden resistor of the current sensor converts the compensation current into an accurate output voltage, available on pin 5 of the sensor. The typical accuracy of the sensor is ± 0.6 % of I_{PN}, magneto-resistive current sensor primary current [33].

To improve the frequency response, an RC-filter is recommended to be connected between ground and the output voltage signal V_{out}. Furthermore, a 3 V zener diode is considered for over-voltage protection of the DSP.

4.2.2 AC voltage sensor

Two voltage dividers are used to sense the AC voltage needed for the outer voltage control loop as shown in Figure 3.4. The voltage divider role is to scale down input voltage to correspond to the maximum ADC input voltage indicated in the datasheet of the targeted DSP [34]. When measuring the AC input voltage the resultant waveform would require to be shifted up by an Operational Amplifier (OP AMP), as micro-controllers cannot read negative values. In order to simplify this process and discard the use of OP AMPs and its effects on the case of power density, the two voltage measurements are made separately and internally added up in the DSP to reconstruct the rectified voltage waveform. The schematic of the AC voltage sensor is shown in schematic A - Figure A.2.

Considering the peak voltage of the input AC (325 V), and the fact that for each input signal, the divider must accommodate the output signal to the ADC measurement range of 0 to 3 V, multiple resistors in series are used, due to the maximum allowable voltage across each resistor. First, for low power dissipation, two 430 kΩ are selected for the line and neutral voltage feedback divider upper resistors, R_1 and R_2, R_4 and R_5 respectively. Next, the lower resistors for the voltage dividers (R_3 and R_6) can be calculated as [35]:

$$R_{3,6} = \frac{V_{ADC,max} \cdot R_{upper}}{V_{ac,max} - V_{ADC,max}} \approx 8\ k\Omega \tag{4.3}$$

Once the resistors for the voltage dividers are selected, the resulting voltage to the analog ADC input is calculated to verify that is the range 0-3 V:

$$V_{ADC,in} = V_{ac,L} \cdot \frac{R_3}{R_{Total}} \approx 2.7\ V \tag{4.4}$$

Moreover, a low pass filter must be used to ensure no frequency components greater than half the DSP sampling frequency are fed to the ADC. Consequently, small ceramic capacitors, C_1 and C_2, are used in parallel with R_3 and R_4. Zener diodes are also added for protecting the DSP of voltage surges.

4.2.3 DC voltage sensor

In a similar manner to one for the input voltage sensing, the DC output voltage divider is designed to sense the output voltage of the boost PFC converter. The output voltage of the designed PFC converter is 400 V. Schematic diagram of the DC voltage divider is shown in schematic A - Figure A.3.

The DC voltage divider resistances R_1, R_2, R_3, are selected to attenuate the output voltage to the quantity $V_{ADC,max}$, which has a maximum voltage 3 V. Resistances of R_1 =

$R_2 = 1M\Omega$ and $R_3 = 13\,k\Omega$ are selected for a maximum measurable DC output voltage of 410 VDC, including the allowed voltage ripple. The ADC input voltage with the selected components is:

$$V_{ADC,in} = V_{DC} \cdot \frac{R_3}{R_{total}} \approx 2.7\ V \tag{4.5}$$

Including a margin in order to protect the DSP in case of output over-voltage, a zener diode is also included in the DC voltage divider Z_1 and a filter capacitor $C_1 = 10\,nF$ in parallel with the lower resistor R_3.

4.3 Heatsink design

Temperature is an important factor in all electronic applications due to its influence in the total power loss of the system. Conduction and switching losses can heat up the power devices above their maximum junction temperature (T_j), and cause failures in performance. Therefore, thermal management should be determined at the board layout design stage. In this section, losses of semiconductor devices are calculated in order to obtain the thermal model and select an appropriate heat sink for the design. In the following, the power loss calculation is performed considering the maximum voltage and current ratings of the devices at $T_{j,max} = 125^{\circ}C$ in order to be in the safe area as power losses usually increase with temperature.

4.3.1 Power losses in bridge rectifier

For this project design 600 V diode bridge rectifier (BR) is selected in order to have a good margin against mains surge voltages. Using a rectifier with high rated current, 25 A in this case, allows lower forward voltage drop V_f, which reduces the total power dissipation. The power dissipated in one of the diodes in a bridge rectifier is obtained from the following expression [18]:

$$P_{diode} = V_{th} \cdot I_{in\_avg,BR} + R_{diode} \cdot I_{in\_rms,BR} \tag{4.6}$$

where V_{th} is the threshold voltage, R_{diode} the dynamic resistance of the diode, $I_{in\_avg,BR}$ the average current flowing through the BR and $I_{in\_rms,BR}$ the BR input rms current.

Assuming the converter efficiency is $\eta = 100\%$, the current in one of the bridge rectifier arms is half the input current. Thus, $I_{in\_avg,BR}$ and $I_{in\_rms,BR}$ are calculated based on the line rms current, $I_{in,rms}$, arer found in Equation 4.8

$$I_{in,rms} = \frac{P_o}{\eta \cdot V_{in,rms}} \tag{4.7}$$

$$I_{in\_rms,BR} = \frac{I_{in,rms}}{2} \quad ; \quad I_{in\_avg,BR} = \frac{\sqrt{2} \cdot I_{in,rms}}{\pi} \tag{4.8}$$

From bridge rectifier datasheet [36] instantaneous forward voltage vs forward current characteristic, the diode resistance is found out to be $R_{diode} = \frac{\Delta V_f}{\Delta I_f}$.

Once the losses in one of the diodes is calculated, the bridge rectifier power loss is:

$$P_{BR} = 4 \cdot P_{diode} \tag{4.9}$$

4.3.2 Power losses in DIPPFC

Figure 4.5, the internal structure of the Super Mini DIPIPM module family is shown. The power switch and boost diode share the heatsink, as they are integrated in the same package. This section derives the power losses in the IGBTs and diodes of the DIPPFC.

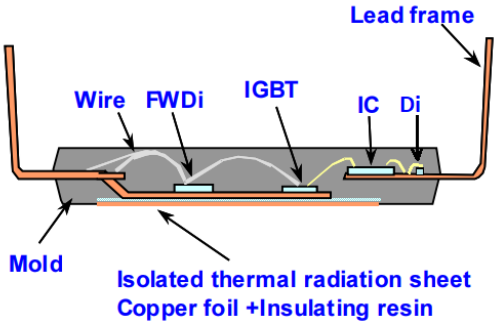


Figure 4.5: Internal cross-section structure of Super Mini DIPIPM from Mitsubishi [12]

Conduction losses occur when the power device is in ON state, conducting current. Equation 4.10 is used to determine the conduction loss of one IGBT, where D is the duty cycle, V_{CE_sat} is the collector-emitter saturation voltage and I_c the collector current. From the datasheet, $V_{ce\_sat} = 2.6\,V$ @$I_c = 20\,A$ and junction temperature $T_j = 125°C$. Then, V_{ce_sat} in other conditions than specified in module electrical characteristics, can be calculated by using linear interpolation.

$$P_{S_{cond}} = D \cdot V_{ce\_sat} \cdot I_c \tag{4.10}$$

The diode conduction losses can be calculated using Equation 4.11, where I_f and V_f are the diode forward current and voltage. These are also obtained by linear interpolation with respect to the datasheet values of $V_f = 1.9\,V$@$I_f = 20\,A$.

$$P_{Di_{cond}} = (1 - D) \cdot I_f \cdot V_f \tag{4.11}$$

The total conduction losses of one boost cell of the PFC converter are:

$$P_{cond,total} = P_{S_{cond}} + P_{Di_{cond}} \tag{4.12}$$

On the other hand, switching losses depend on many parameters and on the particular switching waveform, which is influenced by many factors, such as driving current, gate resistors, threshold voltage, parasitic capacitance. The switching losses due to the IGBT commutation occurring at turn-on and turn-off is expressed in Equation 4.13, where f_{sw} is switching frequency, E_{on} and E_{off} represent energy dissipation corresponding to power switch turn on and turn off.

$$P_{sw} = f_{sw} \cdot (E_{on} + E_{off}) \tag{4.13}$$

$$E_{on} = \frac{t_{on}}{2} \cdot I_{c\_pk} \cdot V_{ce\_pk} + Q_{rr} \cdot V_{ce,pk} \tag{4.14}$$

$$E_{off} = \frac{t_{off}}{2} \cdot I_{c\_pk} \cdot V_{ce\_pk} \tag{4.15}$$

The second term in the expression for E_{on} is to account for the effect of boost diode reverse recovery charge Q_{rr} that put stress upon the switching transistor. The reverse recovery charge for the diode can be found, using the typical reverse recovery time of the encapsulated boost diodes, $t_{rr} = 0.05\ \mu s$ and the reverse recovery current $I_{rr} = 2.5\ A$.

$$Q_{rr} = \frac{1}{2} \cdot t_{rr} \cdot I_{rr} \tag{4.16}$$

By using the available datasheet information and Equations 4.12-4.13, accounting for the two diodes and two IGBTs encapsulated in the power module, the total power dissipation in the DIPPFC is given by:

$$P_{total,DIPPFC} = 2 \cdot (P_{cond} + P_{sw}) \tag{4.17}$$

4.3.3 Thermal model

The IGBTs and boost diodes share the same heat sink, as shown in Figure 4.5. In order to reduce the area and make the design more compact, the same heat sink is also used for the bridge rectifier. Hence, the total power losses that need to be included in the model is obtained by summing up the bridge rectifier losses with the DIPPFC power losses. This operation results in a final power dissipation of:

$$P_{dissipation} = P_{total,DIPPFC} + P_{BR} \approx 40\ W \tag{4.18}$$

By applying electrical and thermal analogy, the thermal model of the interleaved PFC converter is shown in Figure 4.6. P_{IGBT}, P_{diode} and P_{BR} state for the total power dissipation in the IGBTs, diodes and bridge rectifier, respectively. $R_{\Theta JC}$ in the junction to case thermal resistance, $R_{\Theta TIM}$ is the thermal interface material (i.e., thermal grease) thermal resistance and $R_{\Theta HSA}$ is the heatsink to ambient thermal resistance. T_j and T_C are the junction and case temperature of the device.

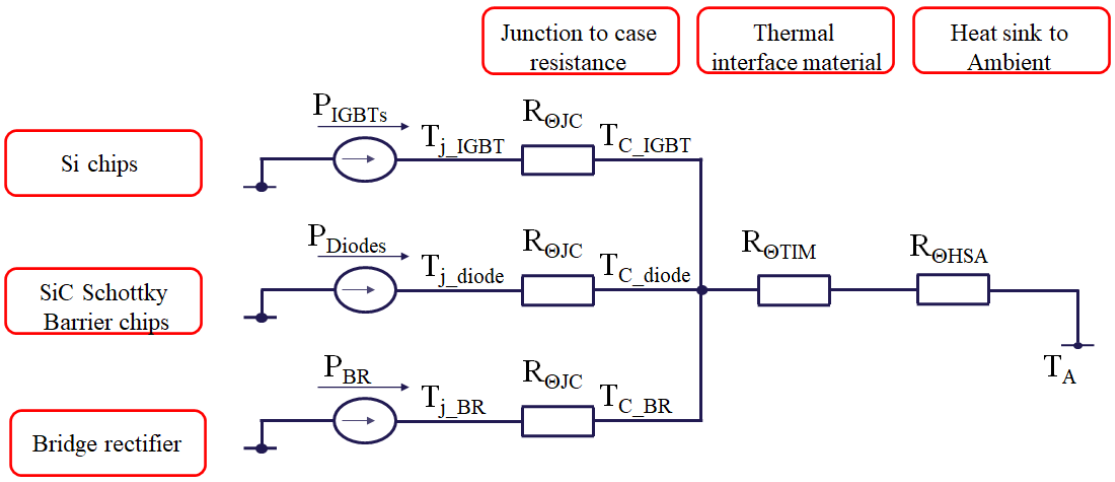


Figure 4.6: Thermal model for the two-channel interleaved PFC converter.

In order to find the thermal resistance of the heatsink, required for efficient heat dissipation, the following parameters are used:

$$T_j = 125^{\circ}C;\ T_A = 50^{\circ}C \tag{4.19}$$

$$R_{\Theta JC\_IGBT} = 1\ ^{\circ}C/W\ (per\ chip) \rightarrow R_{\Theta JC\_IGBT\_eq} = 0.5\ ^{\circ}C/W \tag{4.20}$$

$$R_{\Theta JC\_D} = 1.8\ ^{\circ}C/W\ (per\ chip) \rightarrow R_{\Theta JC\_D\_eq} = 0.9\ ^{\circ}C/W \tag{4.21}$$

$$R_{\Theta JC\_BR} = 1.4\ ^{\circ}C/W \tag{4.22}$$

Neglecting the thermal interface material resistance which is usually a low value (i.e. 0.3 K/W), heat-sink to ambient resistance can be found as follows:

$$T_j = P_{dissipation} \cdot (R_{\Theta JC,total} + R_{\Theta HSA}) + T_A \tag{4.23}$$

,where $R_{\Theta JC,total}$ is the total junction to case resistance that is be calculated from each components $R_{\Theta JC}$ resistors in parallel, as in Figure 4.6.

$$R_{\Theta HSA} = \frac{T_j - T_A}{P_{dissipation}} - R_{\Theta JC,total} = 1.6\ ^{\circ}C/W \tag{4.24}$$

Eventually, for this project a laboratory available heatsink is used. A rectangular aluminium heatsink with fan, with thermal resistance of 0.68 K/W, $100mm\ x\ 50mm\ x50mm$, PCB Mount from Fischer Elektronik is used. Maximum junction temperature $T_{j,max}$ during stationary operation for each device is then verified using the thermal resistance of the selected heat sink. The temperature of the heatsink, in order to dissipate $P_{dissipation} = 40\ W$ and assuming $T_A = 50^{\circ}C$, results in $T_{HS} = 73.5^{\circ}C$. The resulting T_j per IGBT is around $88^{\circ}C$, while for each boost diode it is $78.7^{\circ}C$. For the bridge rectifier it results in $78.6^{\circ}C$. Hence, the heat sink design is checked in order to keep the devices under the maximum allowed junction temperature of $T_{j,max} = 125^{\circ}C$.

4.3.4 PFC converter efficiency

The thermal model is simulated in *PLECS* by adding to the electrical simulation a heatsink together with its thermal resistance, $R_{\Theta HSA} = 0.68\ K/W$, and a constant voltage source that represents the ambient temperature, $T_A = 50^{\circ}C$. From Figure 4.7 it is seen that the heatsink is placed on top of the two boost choppers and the bridge rectifier as it will absorb the switching and conduction losses of the components within its boundary [37]. A heat flow meter, W_m, is included to measure the power dissipated by the heatsink.

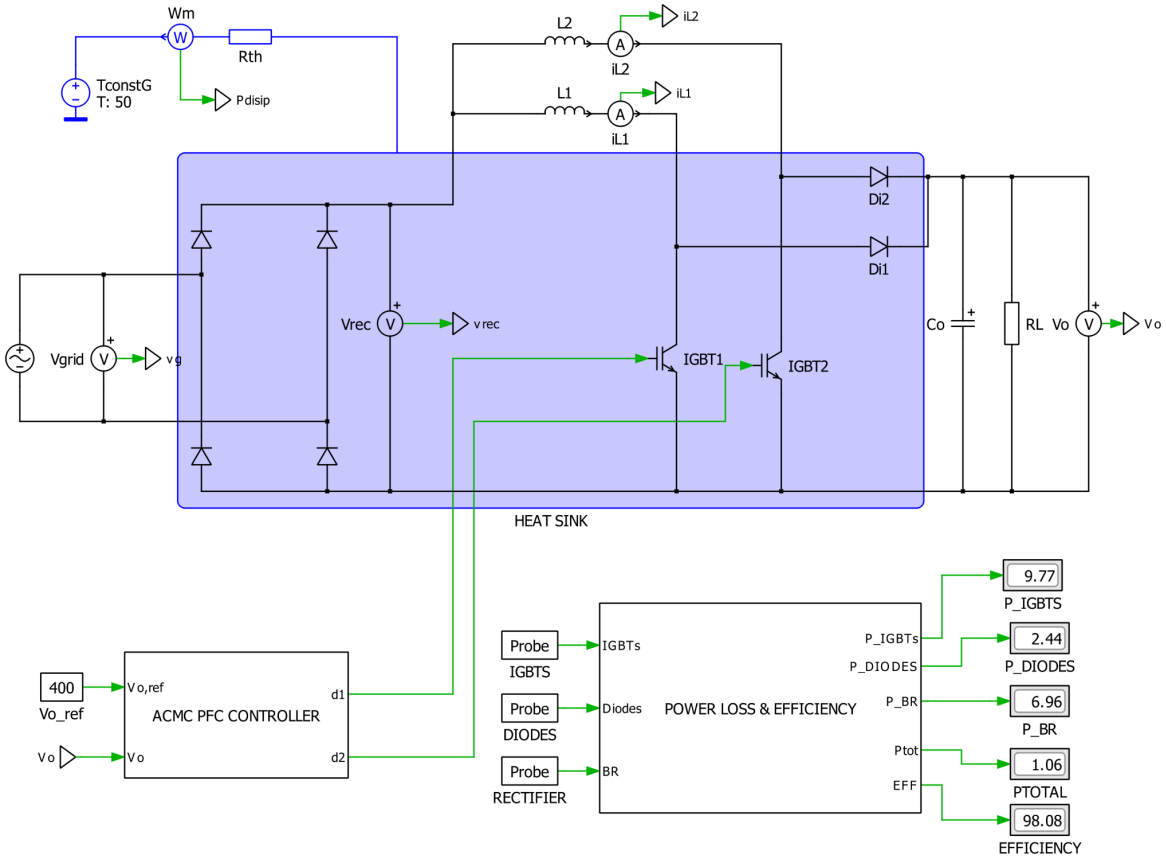


Figure 4.7: Thermal model in *PLECS* of the two-channel interleaved PFC converter for simulation of efficiency, power losses and temperature distribution in the semiconductor devices.

Switching and conduction losses are included a thermal description in terms of look up tables as shown in Figure 4.8. As an example, the thermal description of one IGBT will include the characteristic curves from the device's datasheet (top graphs) for E_{on} and E_{off} to simulate P_{sw}. For the IGBT conduction losses, the graph that relates $V_{CE,sat}$ with I_c is included (left bottom graph). The right bottom graph shows the boost diode forward characteristics at different T_J and it is used for computing the diode conduction losses. The

diode reverse recovery loss which takes place when the diode is reversed biased is added to the turn-on losses of the IGBT, based on Equation 4.14. Finally, the thermal impedance of each device is also included in order to obtain its junction temperature.

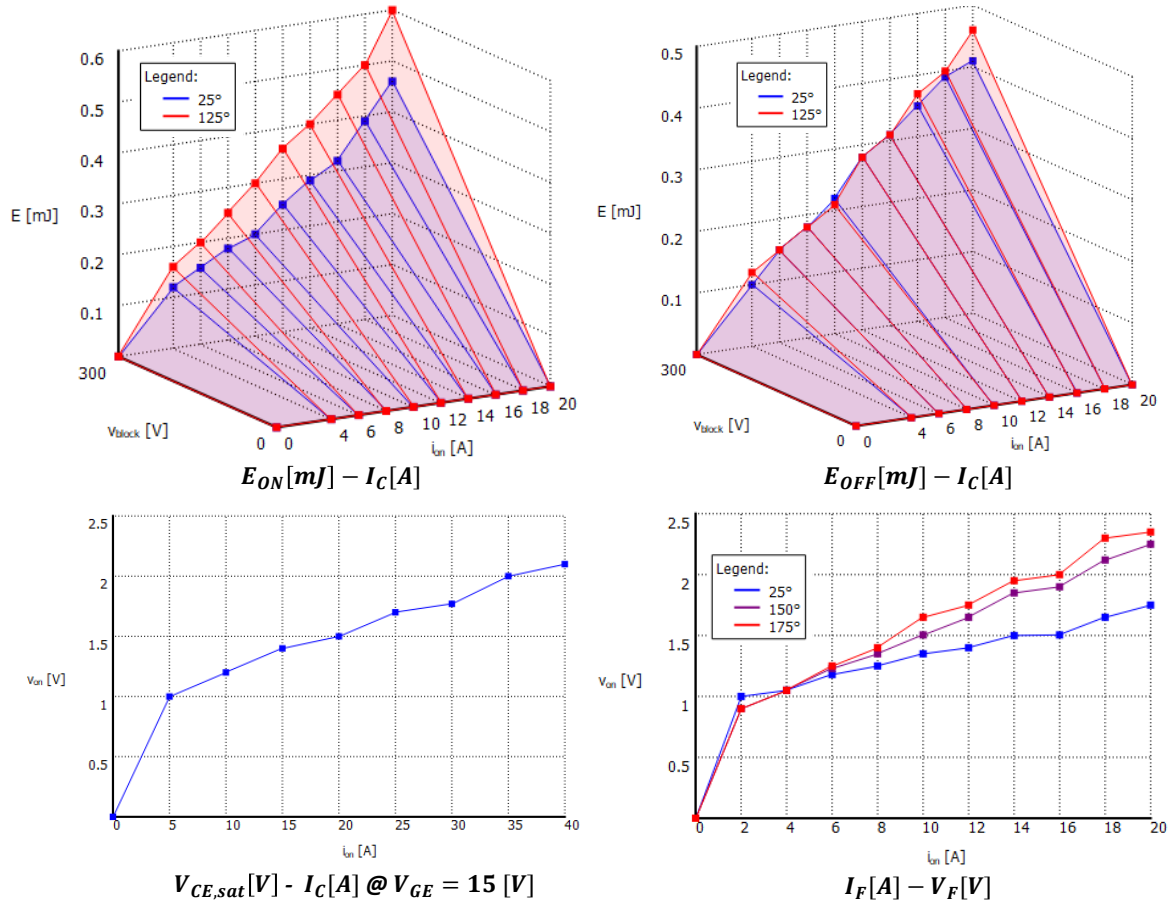
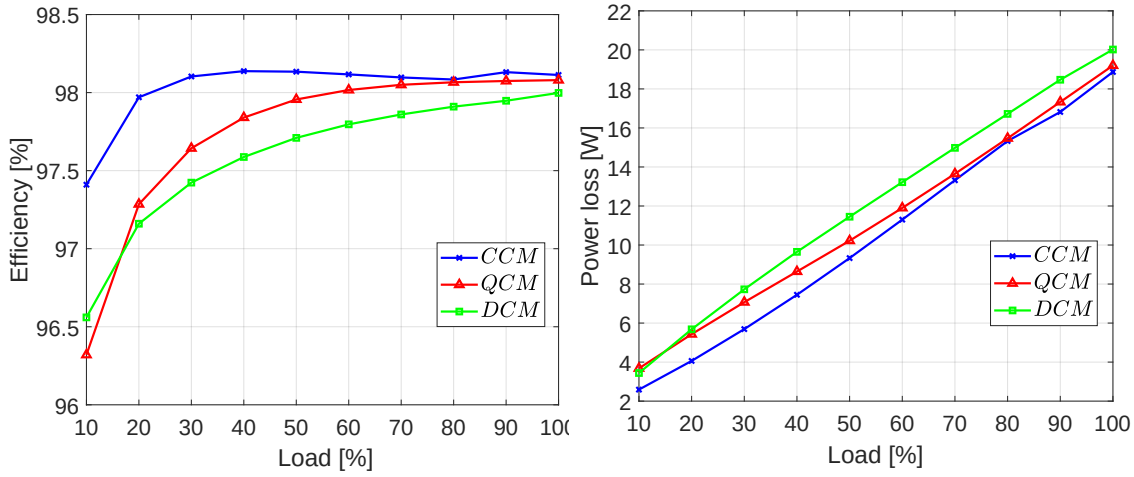


Figure 4.8: IGBT and diode characteristic curves used to create the look up tables for power losses simulation.

The datasheet of the DIPPFC from Mitsubishi, does not provide the internal device's characteristic curves which means that exact look up tables could not be included in the thermal simulation. Instead, semiconductor devices from competitors with similar characteristics were used. In Figure 4.9 the efficiency and total power loss from 10-100% rated power is shown for the converter operating in CCM, QCM and DCM. At this point only the losses in the semiconductor devices are considered for the calculation of the converter efficiency. In Chapter 5 the boost inductor and DM EMI filter inductors power losses will be included. The efficiency, η, is calculated as follows.

$$\eta\ [\%] = \frac{P_{in} - P_{total}}{P_{in}} \cdot 100 \quad , \textit{where} \quad P_{total} = P_{IGBT} + P_{diode} + P_{BR} \tag{4.25}$$



(a) Efficiency vs Load

(b) Power Loss vs Load

Figure 4.9: Two-channel interleaved PFC converter efficiency and total power loss in semiconductor devices for output power varying from 10-100% rated power in CCM, QCM and DCM .

Table 4.1 shows the different contributions in power loss and the corresponding T_J of IGBTs, boost diodes and bridge rectifier for CCM, QCM and DCM at rated power. It is seen that the IGBTs power losses are around 50% of the total power loss while the diodes contribute with 15% and the bridge rectifier with 35% of total power loss.

Power Loss and Junction Temperature at Full Load								
	P_{IGBT}	P_{diode}	P_{BR}	P_{total}	$T_{J,IGBT}$	$T_{J,diode}$	$T_{J,BR}$	T_{HS}
CCM	9.46W	2.44W	6.96W	18.87W	66.8°C	64°C	63.6°C	62°C
QCM	9.78W	2.46W	6.96W	19.2W	67.12°C	64.17°C	63.97°C	62.48°C
DCM	10.77W	2.63W	6.62W	20.02W	69°C	65.9°C	65.25°C	63.6°C

Table 4.1: Comparison simulated power loss and junction temperature of semiconductor devices and heatsink in a two-channel interleaved PFC converter operating in CCM, QCM and DCM.

Although in QCM and DCM the IGBT turn-on losses are reduced in comparison to CCM due to the zero-current switching, the results do not show significant differences in power loss. This might be due to the fact that the SiC boost diodes of the DIPPFC have low reverse recovery loss. Thus, the reduction in switching losses is not significant and there is an increase in conduction losses because of higher peak currents resulting in slightly higher losses in QCM and DCM operation. This is reflected in the efficiency graph of Figure 4.9, looking at rated power, which results in approximately same efficiency of 98% in the three cases. At 10% rated power the maximum difference in efficiency between CCM and QCM is 1.1%. Therefore, in regards to efficiency, the three current modulation techniques are comparable for the two-channel interleaved PFC converter under study.

4.4 PCB layout

A two-layer PCB was designed for the 1 kW two-channel interleaved PFC under study. This section presents some important considerations during the design of the PCB layout in order to minimize the generation of EMI.

4.4.1 Layout considerations

- Track inductance is minimized by making the tracks as wide and short as possible. The minimum width is determined by the current carrying capacity and the maximum allowed temperature rise. It is also important to maximize the electrical clearance between conductors which is determined by the peak voltage. The minimum track width and clearance was obtained based on IPC-2221A standard [38].

- Power ground (GND) and control ground (AGND) are connected at a single point, denoted as N in the schematic, in order to avoid malfunctioning due to fluctuations at the power ground. A 0 Ω resistor is placed in this track to isolate the analog and digital circuits. The power stage is physically separated from the control stage to prevent electromagnetic coupling that high currents and voltages may induce in the control stage.

- It is good practice to include ground planes which allow to minimize the return path of the signals. The current flowing through the conductor will flow in the ground plane directly underneath thus, achieving minimum loop area. A ground plane associated to AGND is used in both top and bottom layer for the control stage. Similarly, a ground plane linked to GND is used for the power stage.

- The wiring inductance around the external shunt resistors, used to detect overcurrent in the IGBTs, is minimized by making the connection to the corresponding DIPPFC pins as short as possible. This is done to avoid surge voltages reaching the internal LVIC of the module and causing OC level fluctuation and IGBT malfunction.

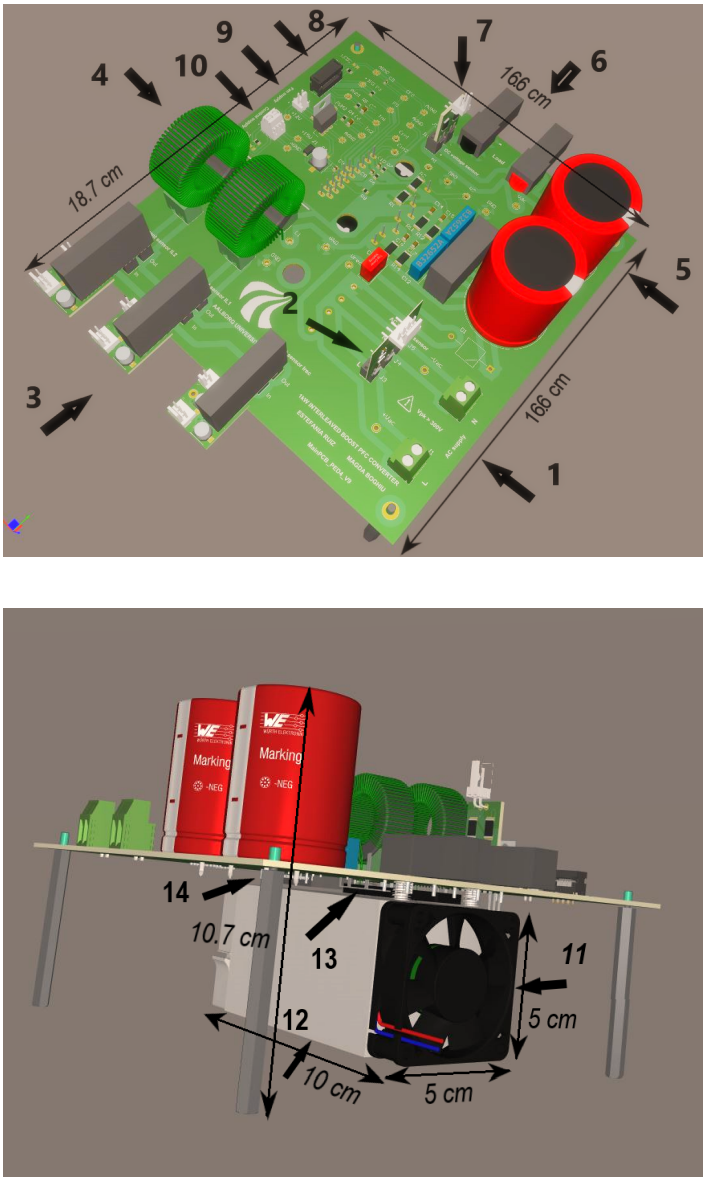
- To guarantee the performance of the snubbers the wiring lenght should be kept as short as possible. If the RC snubbers are located far from the switch terminals, the track inductance may be significant enough that the snubber cannot suppress the spikes and result in destruction of the DIPPFC.

- Every capacitor used for noise filtering should be located as close as possible to the corresponding DIPPFC pins in order to ensure high-frequency noise reduction.

- Magnetic components, in this case inductors, radiate strong magnetic fields which may induce current in nearby conductors yielding to undesired voltages [3]. Therefore, sufficient electrical clearance was left between the inductors and also the current sensors, which are magneto resistive, and the rest of components in the PCB.

4.4.2 1 kW interleaved boost PFC converter prototype

A prototype is developed in order to test the feasibility of the design. Therefore, components are spread out across the PCB in order to facilitate the testing process. Test points are inserted close to all the signals of interest for debugging purposes. Current and voltage sensors are designed in separate PCBs and connected to the main PCB using board-to-board connectors. This is done in order to be able to change the sensors if necessary without modifying the main PCB layout. Figure 4.10 shows the 3D view of the prototype. The designed was verified and this prototype has been later been implemented in this project as seen in Figure C.2



Rf. Nr	Device
1	AC supply connectors
2	External AC voltage sensor
3	External Current sensors
4	Boost inductors
5	DC link capacitors
6	DC load connectors
7	DC voltage sensor
8	DSP connector
9	Fan power supply connector
10	Control supply connector
11	12V Fan
12	0.68 K/W Heatsink
13	DIPPFC
14	Bridge rectifier

Figure 4.10: Top and bottom side 3D view of the PCB showing dimension and components listed in the table.

4.4.3 PFC converter power density

The power density is calculated by dividing the output power by the total volume resulting from the product of the maximum length, width and height of the converter.

$$Power\ density = \frac{Output\ Power}{Total\ Volume} = \frac{P_o}{L \cdot W \cdot H}\ [kW/dm^3] \tag{4.26}$$

The total converter volume is calculated based on the size the converter would have

in a commercial PFC converter. In this project a prototype was develop in order to ease the testing process but in a final product all the components will be stack together on a multi-layer PCB. Therefore, the power density of the converter is found by adding the individual component's volume and the PCB volume. These components are: EMI filter, boost inductors, DC-link capacitors, current sensors, voltage sensors, DIPPFC, bridge rectifier, linear regulator, fan and heatsink.

At this stage the EMI filter is not included in the PCB although it will be considered in the power density calculation. The filter and boost inductor volume will vary based on the current modulation implemented. Therefore, the power density is found for CCM, QCM and DCM operation for comparison. EMI filter and boost inductor boxed volume are obtained from the results that are presented in following chapters.

$$Power\ density\ CCM = \frac{Output\ Power}{Total\ Volume\ CCM} = \frac{1000}{469.27} = 2.13\ kW/dm^3 \tag{4.27}$$

$$Power\ density\ QCM = \frac{Output\ Power}{Total\ Volume\ QCM} = \frac{1000}{443.9} = 2.25\ kW/dm^3 \tag{4.28}$$

$$Power\ density\ DCM = \frac{Output\ Power}{Total\ Volume\ DCM} = \frac{1000}{439.8} = 2.27\ kW/dm^3 \tag{4.29}$$

Chapter 5

Differential Mode EMI filter

Due to the high-frequency current switching in Switched-Mode Power Supplies (SMPS), high-frequency conducted emissions appear. So is the case of PFC, which requires of design of an EMI filter in order to fulfill the regulatory standards and to protect the mains from these emissions. Generally, for the design of the input filter there are two important noise sources, differential-mode (DM), and common-mode noise (CM). DM noise is a voltage differential that appears between the line and neutral of a power circuit, therefore the associated transients have direct path into sensitive circuit components, resulting in system performance degradation. A major contributor to DM noise is the high-frequency switching of SMPS. On the other hand, CM noise most typically appears as a transient voltage between both of the circuit power path lines and ground. Hence, the noise is common to all the lines with respect to a ground, originating from capacitive coupling of DM signals. This type of noise is most often a concern in sensitive analog and digital circuits [39]. Moreover, the DM filter is a major contributor to EMI filter size thus, in order to achieve high power density design, the focus of this project will be laid only on DM noise. Figure 5.1 shows a DM EMI filter circuit structure that can have up to n_f LC filter stages.

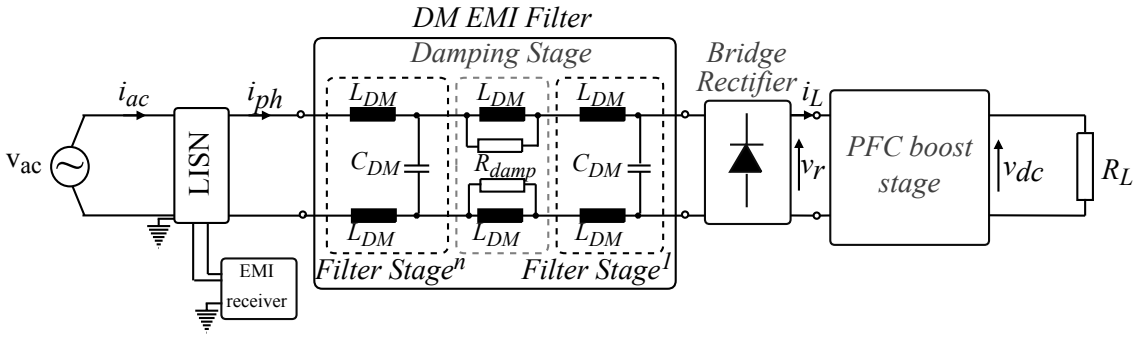


Figure 5.1: Circuit diagram of a PFC converter showing the DM EMI filter.

CISPR noise emission limits, shown in Figure 5.2, are divided in two frequency bands: Band A ($9\ kHz - 150\ kHz$) and Band B ($150\ kHz - 30\ MHz$). Band B is the regulated range while for Band A only some products are regulated by the standard. In this work, DM EMI filter design considering single switch and interleaved PFC topology to fulfill CISPR 11 standard for Class A and Class B equipment is investigated.

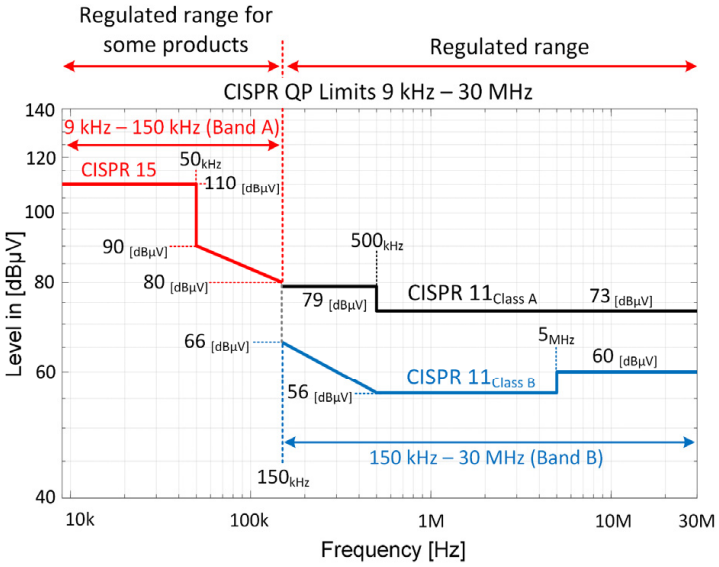


Figure 5.2: CISPR Quasi-Peak (QP) limits for 9 kHz - 30 MHz frequency range [40].

In order to fulfill CISPR11 standard, a DM filter has to be placed the input of the PFC converter. This filter has to deliver the required attenuation, also called insertion loss, at the design frequency f_D. An estimation of the attenuation for high frequencies ($f > 150\ kHz$) is given by [41]:

$$Att_{LC} = \frac{1}{(2 \cdot \pi \cdot f_D)^{2n_f} \cdot L_{DM}^{n_f} \cdot C_{DM}^{n_f}} \geqslant Att_{req}(f_D) \tag{5.1}$$

where, Att_{LC} is the attenuation of an LC filter having n_f filter stages and which passive components L_{DM} and C_{DM} of each stage have equal values, in order to lead to a minimal filter volume [41]. The attenuation delivered by the input filter has to be larger than the required attenuation. As seen in Equation 5.1, for a certain design frequency and attenuation requirement, an optimal selection of L_{DM} and C_{DM} needs to be done. Consequently, a DM EMI filter optimization with respect to filter components volume is conducted first.

5.1 Differential mode EMI filter optimization

There is a lot of research work being done [2],[5],[41] in the area of DM EMI filter analysis for PFC converter, as they are widely used. In these references, a minimization of the filter volume is performed by using interpolated volumetric parameters, based on volumes that can be calculated from manufacturers datasheets. The volume of the passive components has to be estimated with the final goal to evaluate the filter performance and size. In this section, volumetric parameters of filter capacitors C_{DM} and inductors L_{DM} are derived.

5.1.1 Capacitor volume optimization

Differential mode filter capacitors, C_{DM}, are placed between line and neutral, to protect against differential mode interference. The voltage rating of C_{DM} needs to be higher than the peak voltages of the application considering the mains RMS voltage of 230 V. As a rule of thumb, these peak voltage need to lower than 4.3 times input voltage [42] (i.e. 230 V $\cdot$ 4.3 gives approximately 1000 V). Hence, the sub-category of class X capacitors, used for general-purpose applications, Class X2 capacitors, with peak voltage $\leqslant$ 2500 V, from different brands have been evaluated.

Capacitors from manufacturers *Vishay*, *Panasonic*, *Kemet*, *TDK* and *Wurth* with corresponding AC rms voltage level 275 V, 305 V and 310 V are investigated. Two different materials are considered: Metallized Polypropylene (MKP) and Metallized Polyester (MKT). Datasheets from these manufacturers are used in order to retrieve the set of available capacitances and their dimensions, in order to calculate the boxed volume and approximate a general volume for the capacitor, according to [41],

$$V_{C_{DM}} = k_{C1} \cdot C_{DM} \cdot V_{in,pk}^2 + k_{C2} \tag{5.2}$$

where k_{C1} describes the proportionality of capacitor volume and the stored energy, and k_{C2} is a voltage dependent factor, $V_{in,pk}$ is the peak of the capacitor rated voltage [5].

The above equation is based on the fact that the capacitance and the breakdown voltage depends on its geometric and material parameters [43]:

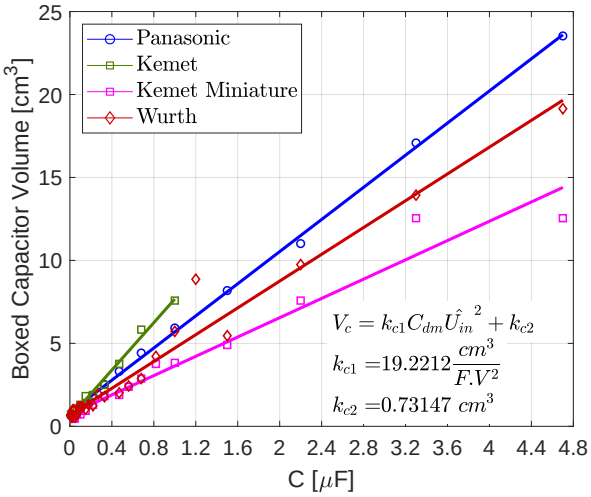
$$C = \frac{\epsilon \cdot A}{d} \quad ; \quad E_{br} = \frac{V}{d} \tag{5.3}$$

The capacitance C increases with the area A of the plates and with the permittivity ϵ of the dielectric material, and discreases with the distance between the plates d. The capacitor voltage V, depends on breakdown electric field E_{br} and d. Substituting Equation 5.3 in the capacitor volume (V_C) expression it is shown that:

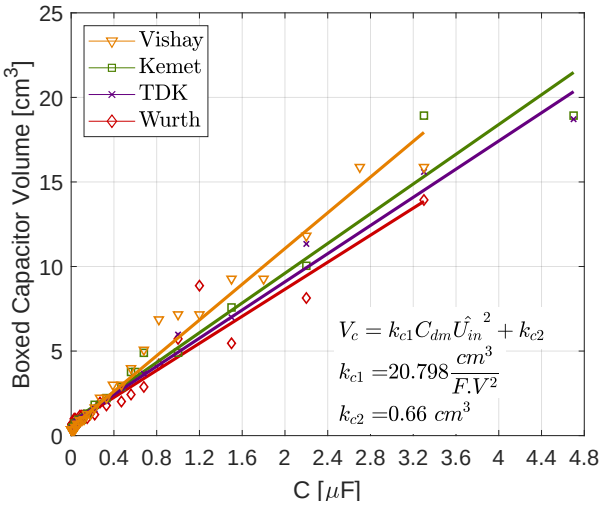
$$V_C = A \cdot d \quad \propto \quad C \cdot V^2 \tag{5.4}$$

Therefore, volume calculations utilizing Equation 5.2 are effectuated for the mentioned manufacturers, and a comparison between them is done in order to find out the optimum

capacitor volume for each voltage rating. The markers in figures indicate the relation between each capacitance value C_{DM} and its volume in the range of up to 4.7 μF for MKP materials (Figure 5.3) and 2.2 μF for MKT capacitors (Figure 5.4). The line represent the estimated fitted volume in Equation 5.2.

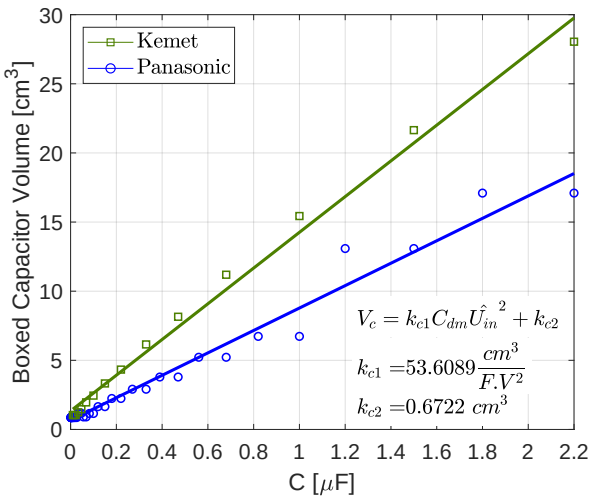


(a) MKP 275 VAC RMS rated capacitors

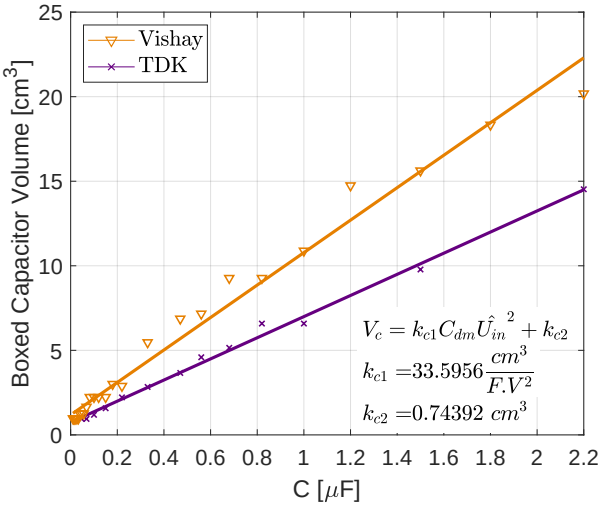


(b) MKP 305 VAC RMS (TDK) and 310 VAC RMS rated capacitors

Figure 5.3: Metallized Polypropylene (MKP) Class X2 capacitors volume approximation for DM filter capacitors and the minimum volumetric parameters k_{c1} and k_{c2} with: a) 275 $V-rms$ b) 305, 310 $V-rms$



(a) MKT 275 VAC RMS rated capacitors



(b) MKT 305 VAC RMS (TDK) and 310 VAC RMS rated capacitors

Figure 5.4: Metallized Polyester (MKT) Class X2 capacitors volume approximation for DM filter capacitors and the minimum volumetric parameters k_{c1} and k_{c2} with: a) 275 $V-rms$ b) 305, 310 $V-rms$

Figure 5.3a represents the comparison of capacitors from manufacturers having the

same rating of 275 Vac. The minimum volumetric parameters $k_{C1} = 19.2212$ and $k_{C2} = 0.73147$ are obtained for *Kemet miniature package*. It is to notice that there has been found a datasheet for *Kemet* where the range of capacitance values is only up to $1\mu F$ and no special miniaturized package. If it is to consider this, then for 275 Vac, *Wurth* would give the minimum volumetric parameters. When voltage rating of 305 Vac and 310 Vac are compared, the minimum resulting volume is given by *Wurth*, as seen in Figure 5.3b. Fewer manufacturers having MKT class X2 capacitors were found. These are compared in Figure 5.4, again for the different voltage ratings. In this case, the resulting minimum parameters corresponds to *Panasonic* (275 Vac) and *TDK* (305 Vac). As the goal is to minimize the DM EMI filter volume, the mini-package from *Kemet miniature* rated at 275 Vac is included as reference for the design because it gives the lowest volume of all the selected capacitors.

It is interesting to analyze how the volume of the EMI filter will be affected when using ceramic capacitors. Thus, 250 Vac rated Multilayer Ceramic Capacitors of Class X2 from *Murata* are also considered and shown in Figure 5.5. The volume of a 56000 pF was accommodated in order to create the same capacitance range of up to 4.7 μF for the purpose of comparison with film capacitors.

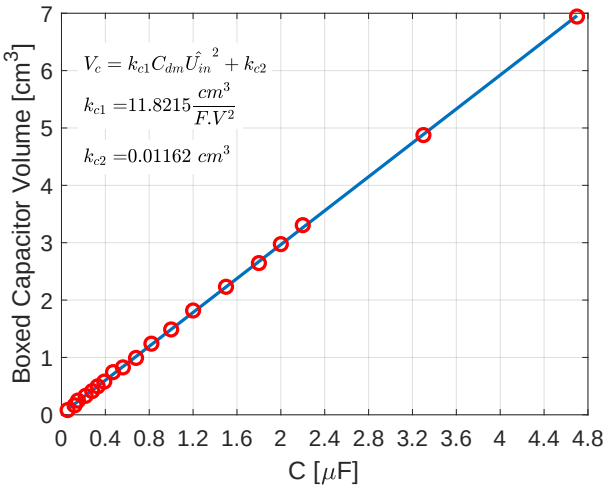


Figure 5.5: Multi Layer Ceramic Class X2 capacitor volume approximation for DM filter capacitors and volumetric parameters for each capacitance, k_{c1} and k_{c2}, 250 $V - rms$ rated

This option could significantly reduce the boxed capacitor volume, by employing multiple of these capacitors in parallel in order to achieve a given capacitance. The volume is halved in comparison to *Kemet miniature* for all the capacitance range. However, a high amount of ceramic capacitors will be required in parallel to obtain the same capacitance than with only one film capacitor. Therefore, this solution is not further considered in this work but it would be an interesting option to consider for future research.

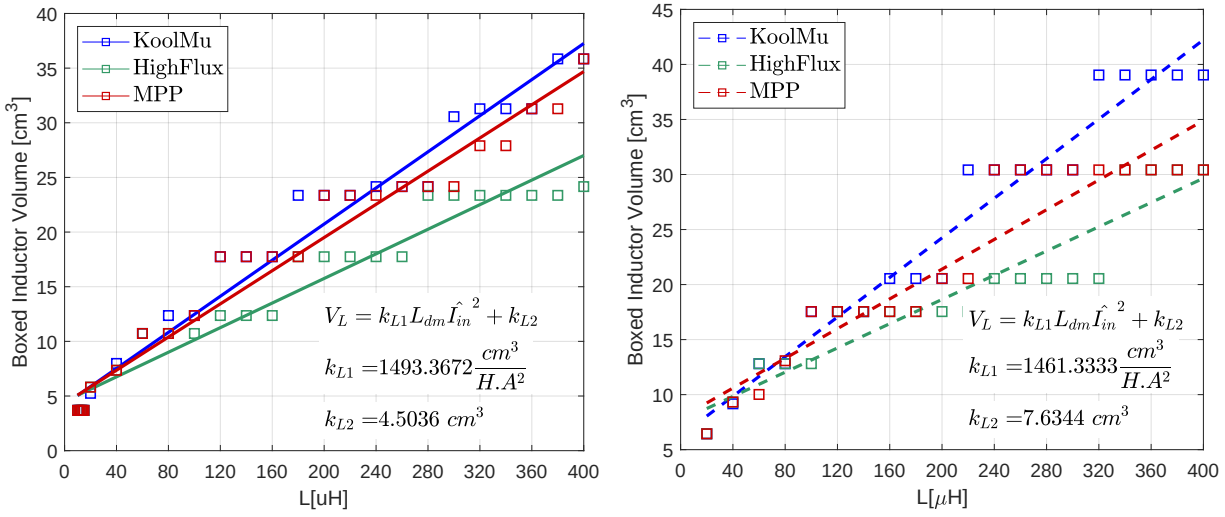
5.1.2 Inductor volume optimization

The volume of the DM EMI filter inductor, L_{DM}, is given as [5, 41, 43]:

$$V_{L_{DM}} = k_{L1} \cdot L_{DM} \cdot I_{in,pk}^2 + k_{L2} \tag{5.5}$$

where, k_{L1} amd k_{L2} are the inductor volumetric parameters, representing the slope that describes the proportionality between inductance L_{DM} and $V_{L_{DM}}$, and the line intercept , respectively. The equation is obtained considering the fact that the volume of an inductor is proportional to the stored energy, $\frac{1}{2} \cdot L \cdot I_{in,pk}^2$. In this work, toroidal powder cores from *Magnetics* are considered for three different core materials: *Kool Mμ*, High Flux and Molybdenum Permalloy Powder (*MPP*).

The volume of the differential mode inductor can be estimated and the core type that gives the minimum volume is chosen. In Figure 5.6, results of fitting the inductances in the range of 10 to 400 μH and their corresponding boxed volume, are presented. The displayed parameters k_{L1} and k_{L2} are the minimum out of all the considered material.



(a) One core.

(b) Two stacked cores.

Figure 5.6: Inductor boxed-volume approximation for DM filter inductances using *Magnetics* toroid cores in dependence on the inductance value

For instance, in Figure 5.6a, inductors based on *High Flux* cores will end up in a lower boxed volume than the others. This is also stated in the manufacturer catalogue [44], that for the smallest core size in a DC bias dominated design, High Flux should be used since it has the highest flux capacity. Moreover, in order to investigate the option of stacking cores to increase the inductance value for the same outer diameter of the core and maintaining the path length, the inductance values and the boxed volume for two stacked cores are shown in Figure 5.6b. Stacking cores will increase the cross section (Ae) by the multiple of the number of cores in the stack. This permits fewer turns and greater power-handling

capability. However, comparing the Figures 5.6a and 5.6b, the volumes of two stack core is not much higher than the volume of one stack core, so in some designs could be beneficial to stack cores. In this work, optimization in regards to minimum volume is pursued, hence, evaluating the results, one stack core is employed for further analysis.

5.2 Differential mode EMI filter design

Once the volumetric parameters k_{c1}, k_{C2}, k_{L1} and k_{L2} are obtained, the filter components values that lead to minimum volume are found in this section.

5.2.1 Optimum DM filter inductance and capacitance values

The total volume of the DM filter is expressed as,

$$V_f = 2 \cdot (n_f + 1) \cdot V_{L_{DM}} + n_f \cdot V_{C_{DM}} \tag{5.6}$$

The term $(n_f + 1)$ accounts for the damping inductor L_d. The total volume of the filter inductors is multiplied by 2 because in PFC converters the CM and DM noise are partially mixed due to the presence of the bridge rectifie. It is common to split L_{DM} into two equal parts in the line and neutral in order to provide symmetry for CM noise propagation [5]. From Equation 5.1, L_{DM} is obtained as:

$$L_{DM} = \frac{1}{(2 \cdot \pi \cdot f_D)^2 \cdot \sqrt[n_f]{Att_{req,LC}} \cdot C_{DM}} \tag{5.7}$$

Then, by substitution of L_{DM} in Equation 5.6, a relation between the filter volume, C_{DM}, L_{DM}, $Att_{req,LC}$ and n_f is obtained. The DM EMI filter optimized component values are obtained by minimizing the filter volume function in Equation 5.6. This is done by deriving V_f with respect to C_{DM} and equalizing the expression to zero.

$$\frac{\partial V_f}{\partial C_{DM}} = 0 \quad \rightarrow \quad min. \tag{5.8}$$

By solving Equation 5.8 for C_{DM} and substituting in Equation 5.7 for obtaining L_{DM}, the optimum DM filter component values are expressed as:

$$C_{DM,opt} = \frac{I_{in,pk}}{U_{in,pk} \cdot (2 \cdot \pi \cdot f_D) \cdot \sqrt[2n_f]{Att_{req,LC}}} \cdot \sqrt{\frac{(n_f + 1) \cdot k_{L1}}{2 \cdot n_f \cdot k_{C1}}} \tag{5.9}$$

$$L_{DM,opt} = \frac{V_{in,pk}}{I_{in,pk} \cdot (2 \cdot \pi \cdot f_D) \cdot \sqrt[2n_f]{Att_{req,LC}}} \cdot \sqrt{\frac{n_f \cdot k_{C1}}{2 \cdot (n_f + 1) \cdot k_{L1}}} \tag{5.10}$$

Substuting Equations 5.9-5.10 in the DM EMI filter volume function yields to the optimum filter volume, shown in Equation 5.11.

$$V_{f,opt} = 2 \cdot (n_f + 1) \cdot \underbrace{(k_{L1} \cdot L_{DM,opt} \cdot I_{in,pk}^2 + k_{L2})}_{V_{L_{DM,opt}}} + n_f \cdot \underbrace{(k_{C1} \cdot C_{DM,opt} \cdot V_{in,pk}^2 + k_{C2})}_{V_{C_{DM,opt}}} \tag{5.11}$$

The DM EMI filter cut-off frequency is expressed in Equation 5.13. It is a good index to evaluate the size of the filter as it is seen that the higher the value of $L_{DM} \cdot C_{DM}$ the lower is the filter cut-off frequency. Higher values of capacitance and inductance implies bigger components, thus, low cut-off filter frequency implies larger filter. It is desired to obtain an EMI filter with large cut-off frequency in order to reduce the filter volume. This is achieved by making $L_{DM} \cdot C_{DM}$ minimum.

$$f_{c,LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{DM} \cdot C_{DM}}} \tag{5.12}$$

5.2.2 Damping stage

The DM EMI filter damping stage, shown in Figure 5.1, is used to limit the peak output filter impedance. There exists different topologies for this purpose, being the RL networks the most common ones which provide sufficient damping with minimum losses and reduced oscillations around the filter resonant frequency [45]. In this project, the R_dL_d series damping topology is implemented which consist of a parallel connected RL network in series with the DM EMI filter. R_d provides the necessary damping while L_d is used to reduce the power dissipation in R_d by providing a dc bypass. The value of R_d that leads to optimum damping is [45]:

$$R_d = \sqrt{\frac{L_{DM}}{C_{DM}}} \cdot \sqrt{\frac{2 \cdot (1+k)}{(2+k) \cdot (4+3 \cdot k)}} \qquad ,where \quad k = \frac{L_d}{L_{DM}} \tag{5.13}$$

The damping stage significantly contributes to the EMI filter size and cost. This is because L_d must handle the rms input current which is achieved using a large inductor. It has been shown in [46] that choosing $L_d = L_{DM}$ leads to a good compromise between total filter volume and damping. Thus, knowing the factor $k = 1$ and the optimum values of filter inductance and capacitance, the damping resistor can be sized. The size of R_d has beeen neglected and only the size of *Ld* is included in the total filter volume.

5.2.3 Optimum number of filter stages

The optimum number of filter stages $n_{f,opt}$, for an specific attenuation requirement at a design frequency, is found from Equation 5.11 by differentiating with respect to n_f and equalizing to zero [5]. In Figure 5.7, the variation of DM EMI filter boxed volume with

the required attenuation for different number of filter stages is shown. It is observed that implementing one filter stage only leads to minimal volume for attenuation lower than 50 dB. From this point, one filter stage will imply a significant increase in the total filter volume in comparison with higher number of stages. For a required attenuation in the range 50 dB $< Att_{req,LC} <$ 97 dB two filter stages yield to minimum filter volume. For higher attenuation required, $n_f = 3$ is preferred in order to minimize the volume. However, the designer should find a compromise between optimum volume and cost as the higher the number of filter stages the more expensive the PFC converter becomes.

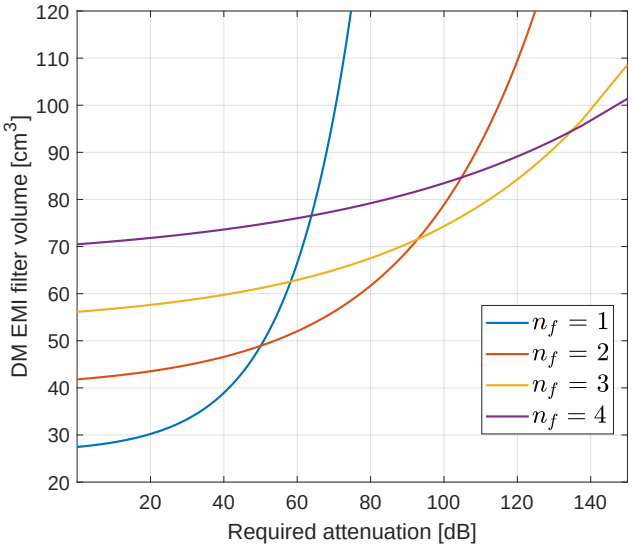


Figure 5.7: Total DM EMI filter boxed volume as a function of the required attenuation for different number of filter stages, $n_f = 1, .., 4$.

5.3 Differential mode EMI noise measurement

Measurement of conducted emissions is achieved by using a Line Impedance Stabilization Network (LISN) connected to an EMI receiver as depicted in Figure 5.1 at the beginning of the chapter. Implementing the LISN and EMI receiver model virtually, helps to optimize the filter parameters at the design stage.

This is a crucial step for determining the required attenuation the EMI filter needs to provide at the design frequency. The design frequency f_D has an influence in the total filter volume and, also in the selection of the number of filter stages to be implemented, as it will determine the required attenuation based on the first multiple of the switching frequency that appears in the Band B frequency range (150 $kHz - 30$ MHz). Hence, if $f_{sw} \geqslant 150$ kHz, f_D will coincide with f_{sw} whereas if $f_{sw} < 150$ kHz the design frequency for a n-interleaved PFC converter is calculated as follows [5]:

$$f_D = m \cdot n \cdot f_{sw} \quad , where \quad m = ceil\left(\frac{150\ kHz}{n \cdot f_{sw}}\right) \tag{5.14}$$

In the case under study, the switching frequency is $f_{sw} = 28\ kHz$ and the number of interleaved boost cells is $n = 2$ which results in a factor of $m = 3$. Thus, the design frequency is $f_D = 168\ kHz$, the 6^{th} multiple of the switching frequency. The required attenuation at the design frequency is expressed, based on the measured conducted emissions, in Equation 5.15 [40].

$$Att_{req,LC}(f_D) = U_{QP,max}(f_D)[dB\mu V] - CISPR_{Limit}(f_D)[dB\mu V] + Margin[dB] \tag{5.15}$$

$U_{QP,max}$ is the peak noise emission that appears at $f_D = 168\ kHz$, $CISPR_{Limit}$ is the noise limit stablished by CISPR11 standard and, the last term, is a margin that is added to account for the components tolerances which is commonly selected to be 6 dB [5]. The procedure for the estimation of $U_{QP,max}$ is explained in the following subsections.

5.3.1 Line Impedance Stabilization Network - LISN

LISN, also called Artifical Mains Network (AMN) in latest IEC standards, main functions are decoupling between the mains and high frequency coming from the power converter, fixing an impedance for line and ground currents and allowing repeatable measurements [40]. The LISN is placed between the AC line and the PFC converter in order to stablish a known impedance over the frequency range $150kHz - 30MHz$. To guarantee impedance mismatch, the LISN presents a low impedance path at the mains side while a high impedance path is stablished from the load to ground. The voltage drop in the LISN resistor will be the measured conducted noise voltage $U_{meas}(t)$.

5.3.2 EMI receiver

The voltage drop $U_{meas}(t)$ is processed by the EMI receiver in order to separate the CM and DM noise. EMI receiver is represented by a 50 Ω impedance paralleled to the LISN resistance [40]. The DM EMI noise is predicted using quasi-peak (QP) detector which measures the repetitive peak noise energy. Figure 5.8 shows the CISPR11 standard for both *Class A* and *Class B* equipment and also illustrates the procedure for QP-voltage detection according to [2]. The EMI receiver converts the measured voltage from time domain to frequency domain, $U_{meas}(f)$, using Faster Fourier Transformation (FFT). Then, a bandpass filter, with specific resolution bandwidth RBW, is applied to $U_{meas}(f)$ around a sweep frequency f_{sweep}, as shown in Figure 5.8b. For the frequency band of interest (Band B) the bandwidth of the filter is $RBW = 9\ kHz$ [40].

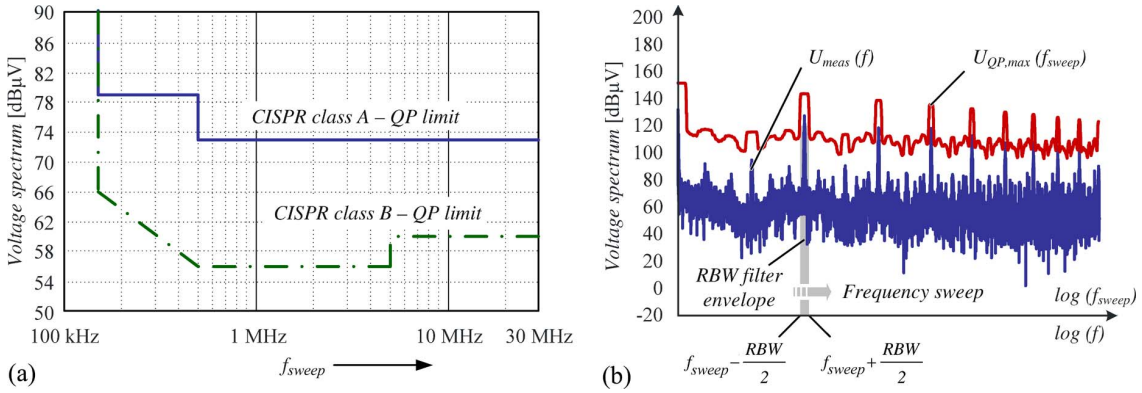


Figure 5.8: (a) CISPR11 limits for QP-detection for Class A and CLass B equipment. (b) Quasi-peak measurement procedure. [2]

The quasi-peak EMI emission can be predicted using the following equation [2][40]:

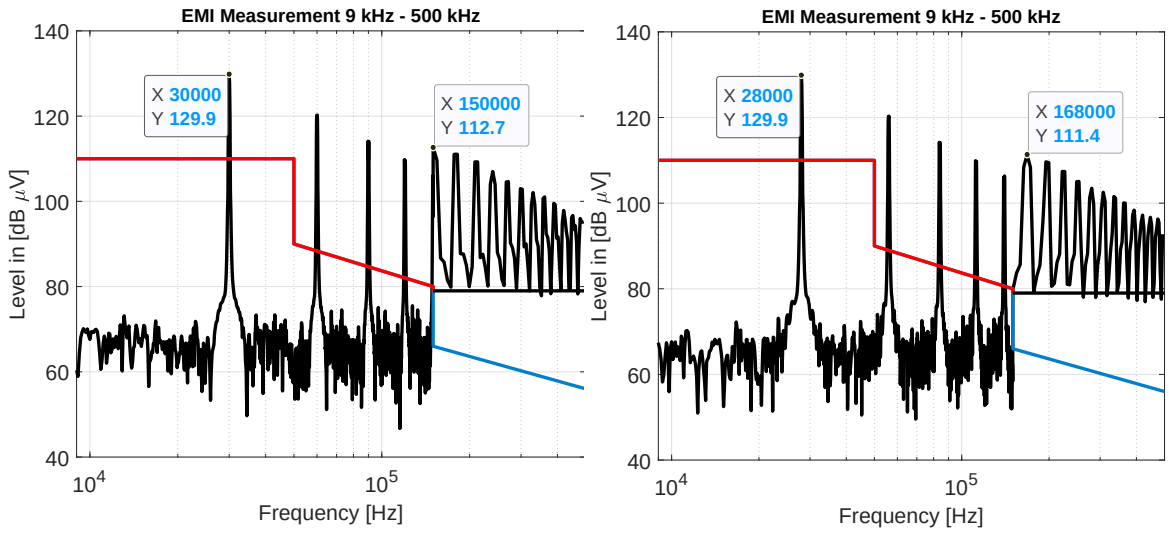
$$U_{QP,max}(f_{sweep})[dB\mu V] = 20 \cdot log\Big[\frac{1}{1\mu V}\sum_{f=f_{sweep}-RBW/2}^{f=f_{sweep}+RBW/2} U_{meas}(f)\Big] \tag{5.16}$$

This is the worst case scenario as it linearly adds the peak noises and it results in slightly over dimensioned EMI filters [2]. However, this is not seen as a drawback because it gives a margin for the system uncertainties (i.e., components tolerances). The maximum quasi-peak voltage at the design frequency, $U_{QP,max}(f_D = 168\ kHz)$, is inserted in Equation 5.15 to obtain the required attenuation for the DM EMI filter.

5.3.3 Effect of switching frequency selection on DM EMI noise

The DIPPFC interleaved converter used in this project has a recommended switching frequency operation of 30 kHz. However, switching at this frequency is not advisable from the point of view of EMI. The reason is that when designing an EMI filter for Band B (150 $kHz - 30\ MHz$), the design frequency f_d is taken as the first appearing peak from 150kHz. The measurement of the quasi-peak voltage is measured using a 9 kHz bandwidth according to standard CISPR 16 [47].

Therefore, special attention is given to the selection of switching frequency below 150 kHz in order to avoid that any harmonic falls in the region $(150 \pm 4.5)\ kHz$. In order reduce the required attenuation for the DM EMI filter design it is recommended to select a switching frequency which harmonics are sub-multiples of $140kHz$ in order to add an extra margin [47]. Figures 5.9a-5.9b show the simulation results obtained with $f_{sw} = 30\ kHz$ and $f_{sw} = 28\ kHz$, respectively.



(a) $f_{sw} = 30\ kHz$ **(b)** $f_{sw} = 28\ kHz$

Figure 5.9: EMI noise simulation results for single-channel boost PFC converter obtained for two different switching frequencies (a) 30 kHz and (b) 28 kHz.

It is observed that the first appearing peak in Band B appears exactly at 150 kHz if the switching frequency is selected to be 30 kHz. The magnitude of the noise emission is higher than in the case of switching at 28 kHz. This means that the required attenuation for the EMI filter is reduced 1.3 dB by choosing a slightly lower f_{sw} which will shift the design frequency away from 154.5 kHz. The size of the filter will be reduced regardless of the modulation technique employed. Therefore, a switching frequency of 28 kHz is selected for the design in order to reduce the EMI filter volume.

Chapter 6

Analysis of two-channel interleaved PFC performance

Further theoretical and simulation analysis is carried out in order to evaluate and optimize the overall performance of the interleaved PFC converter. Important design variables that affect the size and capability of the converter are the different boost inductor current operation modes, maximum allowed inductor current ripple factor k_{ripple} and the angle α where the transition between CCM and DCM mode occurs in the case of QCM. Finally, regarding the input EMI filter, other converter operational parameters such a phase-shift control of the interleaved branches is investigated.

6.1 Boost inductor volume optimization

Optimum boost inductor volume as a function of inductor ripple factor and angle α is evaluated. For CCM operation, k_{ripple} is varied in the range of 0.1 to 1 in Equation 2.6 and α from 10° to 90° in Equation 2.16 for QCM in order to obtain the analogue inductance value range. The obtained inductance values range, the rms inductor current, the maximum inductor current ripple $\Delta_{I,max}$ and the switching frequency f_{sw} are eventually inserted in the Magnetics® Inductor Design tool, which is an aid for selecting powder cores. This tool uses a design algorithm intended to specify the smallest design package size for the given input parameters. However, core catalogue [44] is checked and iterative steps are made in order to ensure that the suggested core by the tool is the one that provides the minimum volume, having the constraint in winding factor (typically 40%). This tool is employed as it gives a good approximation of finished outer diameter and height of wound toroidal core at a design operating point, which are used to calculate the boxed volume of the inductor.

In principle, the ripple factor k_{ripple} will have an influence on the inductor volume and appearing losses, therefore it should be carefully selected. In the literature, several of these aspects are well covered and boost inductor volume optimization methods are proposed [2]. However, the methods concern only interleaved PFC converter under CCM

and DCM operation. Notably, in this work, QCM inductor boost volume and power losses are explored. MPP, High Flux and Kool Mμ® powder core materials with permeabilites of 60 and 125 were selected, and two stacked cores were also considered in the analysis.

6.1.1 Inductor volume variation with k_{ripple} in CCM

Non-interleaved PFC converter

Figure E.1 in Appendix E shows the boost inductor volume as a function of k_{ripple} for the three core materials and different number of stacked core and permeabilities. From each material in Subfigures E.1a, E.1b, E.1c, some that resulted in minimized dimensions have been chosen. Notably, MPP powder core was not selected because the resulting volume dependence on ripple factor curve, lays in between the other two materials and MPP cores cost is much higher than Kool Mu and High Flux.

The powder cores and permeability that give the best volume are selected and compared in Figure 6.1. It can be observed that the magnetic volume, and in relation, the inductance, decreases as the maximum allowed current ripple increases. From the results, one core of $\mu = 60$ and two stack core of $\mu = 125$ from High Flux powder cores give lower volume than Kool Mu cores. Although when selecting the magnetic core for a design, if the same material gives the minimum volume then the permeability and/or the number of stacked cores needs to be considered. For $k_{ripple} > 0.5$, 2 stacked cores give minimum volume but it will also yield to an increase in cost in comparison to one core.

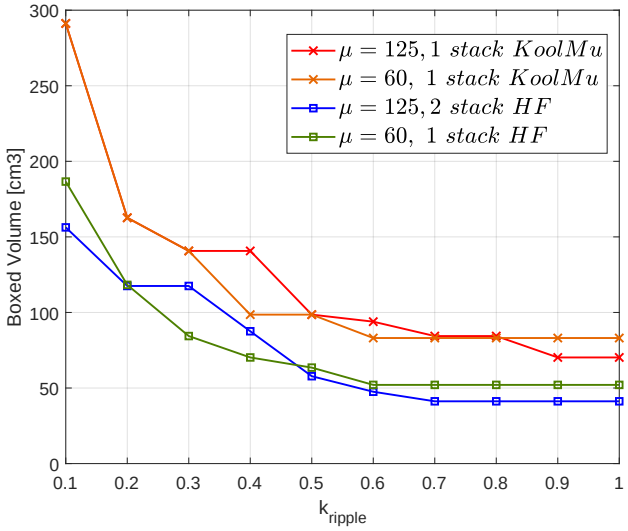


Figure 6.1: Non-interleaved PFC converter - Comparison of boost inductor volume in CCM for the optimum Kool Mu and High-Flux cores, obtained from *Magnetics'* Powder Cores, varying k_{ripple}.

Two-channel interleaved PFC converter

Core materials with permeabilities that resulted in minimum volume in the case of non-interleaved PFC converter driven in CCM (Kool Mu 60μ and High-flux 60μ) according to Figure 6.1 are further investigated for the case of two boost interleaved PFC. In Figure 6.2, the results obtained for boost inductor volume as function of ripple factor are traced. It can be observed that overall volume per inductor is reduced, as one interleaving boost inductors benefit is the equal share of input current. High Flux cores based inductors, with permeability of 60 have the lowest boxed volume in the entire range of k_{ripple}. It can also be seen that there is a tradeoff between the optimum current ripple factor value in achieving a reduced in size boost inductor.

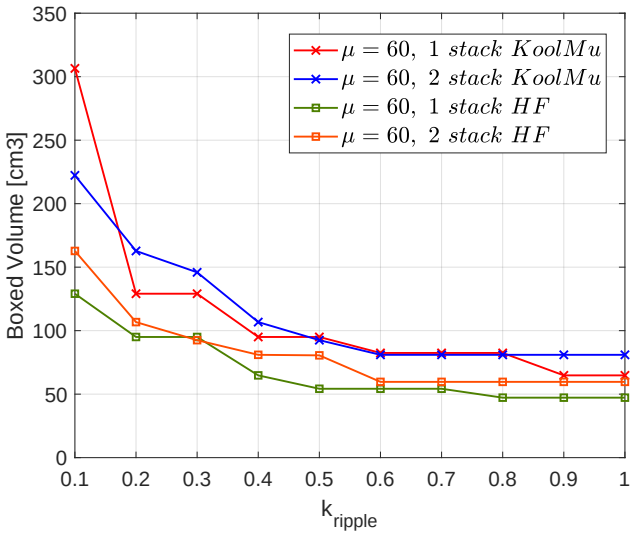


Figure 6.2: Two-channel interleaved PFC converter - Comparison of boost inductors total volume in CCM for Kool Mu and High-Flux cores with permeability 60 and different number of stack cores, obtained from *Magnetics'* Powder Cores, varying k_{ripple}.

Nevertheless, in order to have a decisive point of view in selecting the optimal k_{ripple} for the application, boost magnetic component losses need to be regarded as an important factor. For this purpose, the core and copper losses need to be found. Inductor Design tool from *Magnetics*® provides core and copper losses for each design. However, the tool algorithm regards the input current as a sinusoidal current, hence the accuracy in the case of core losses is affected. This fact is due to the non-sinusoidal flux-density (B) waveform given the presence of PFC power switch, and the resulting switched current waveform. For the case of core losses, the well known Steinmetz equation gives a good approximation when it comes to sinusoidal waveform. As in present case, there is the improved General Steinmetz Equation (iGSE) in a simplified form, that is employed in order to obtain a more

accurate estimation of inductor core losses [2], [48]:

$$P_{core,v} = k_i \cdot f_{sw} \cdot \Delta B^{(a-b)} \sum \left(\frac{U_{L_{dc,j}}}{N \cdot A_e} \right)^b \Delta t_j \tag{6.1}$$

$$k_i = \frac{k}{2^{(a+1)} \cdot \pi^{(b-1)} (0.2761 + \frac{1.7061}{b+1.354})} \tag{6.2}$$

where N is the number of turns, $U_{L_{dc,j}}$ is the voltage across the PFC boost inductor over one switching time interval Δt_j, A_e is the cross section area of the core, a,b and k are factors found in the core datasheets. Eventually, final core losses based on the adapted Steinmetz equation can be calculated as in Equation 6.3 with l_e being the effective magnetic path length and N_c the number of stacked cores [48].

$$P_{core} = l_e A_e N_c P_{core_v} \tag{6.3}$$

The copper losses, Pcu, comprise of resistive lossed $P_{cu,dc}$ due to the winding resistance and eddy-current losses $P_{cu,edd}$ due to skin and proximity effects [48]. The DC copper losses are found in Equation 6.4 where I_L is the inductor DC current and $R_{L,dc}$ is the dc resistance of the windings calculated from Equation 6.5.

$$P_{cu,dc} = I_L^2 R_{L,dc} \tag{6.4}$$

$$R_{L,dc} = \rho_{cu} \cdot l_{cu} / A_{cu} \tag{6.5}$$

Considering copper conductor and its diameter, the length l_{cu} can be calculated as follows:

$$l_{cu} = MLT \cdot N \qquad ; \qquad MLT = 0.8 \cdot (OD + 2 \cdot HT) \tag{6.6}$$

, where MLT is the Mean Length Turn for a toroidal core, N is the number of turns, OD the outer diameter and HT the height of the core.

Inserting the required Steinmetz parameters (a,b,k), from datasheet, for High Flux material with permeability of 60 considering a frequency $f_{sw} > 25\ kHz$, in Equations 6.1 to 6.3, the core losses are obtained. Figure 6.3, depicts core and copper losses in 6.3a and the total sum of these in 6.3b.

Observing the trend of total boost inductor losses 6.3b , they decrease fast with current ripple and reach a minimum value at a certain k_{ripple} value, then they slowly start to increase. When at low current ripple values, as the current ripple increases, the inductance value decreases allowing the choice of a smaller core, resulting in lower core and copper losses, until the current ripple becomes high enough to generate higher core and copper losses, therefore the slight icnrease in curve.

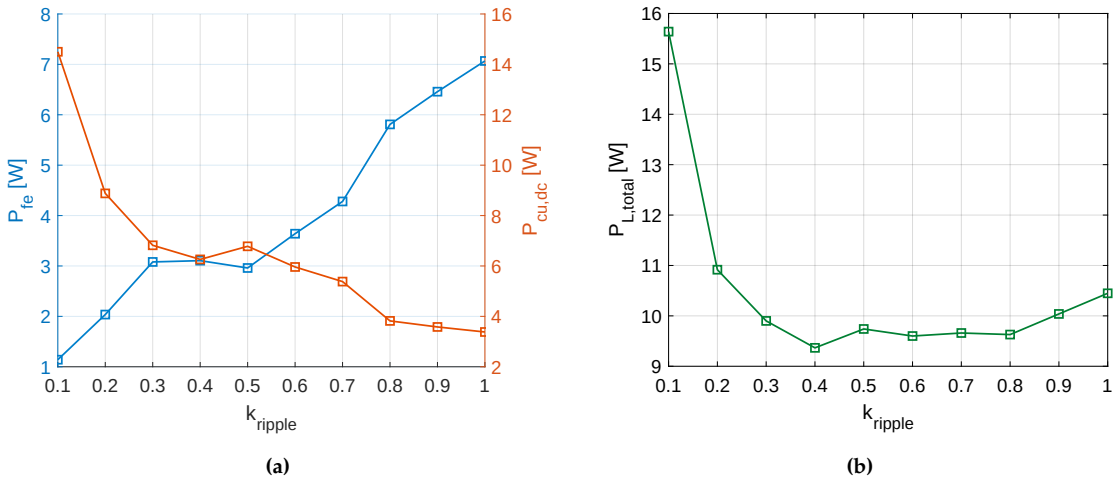


Figure 6.3: Two-channel interleaved PFC converter - inductor losses in CCM for High-Flux cores with permeability 60, obtained from *Magnetics*' Powder Cores, varying k_{ripple}.

Comparison interleaved and non-interleaved PFC converter in CCM

Considering the total power losses in the single and interleaved topology of the converter and the total inductor volume (multiplied by a factor of two in the case of two interleaved boost inductors), Figure 6.4 shows the dependence of these on k_{ripple}. A reduction in the total boost inductor volume is obtained by interleaving. However there is a slight increase in the total power loss, as the number of cores is doubled in the case of interleaved.

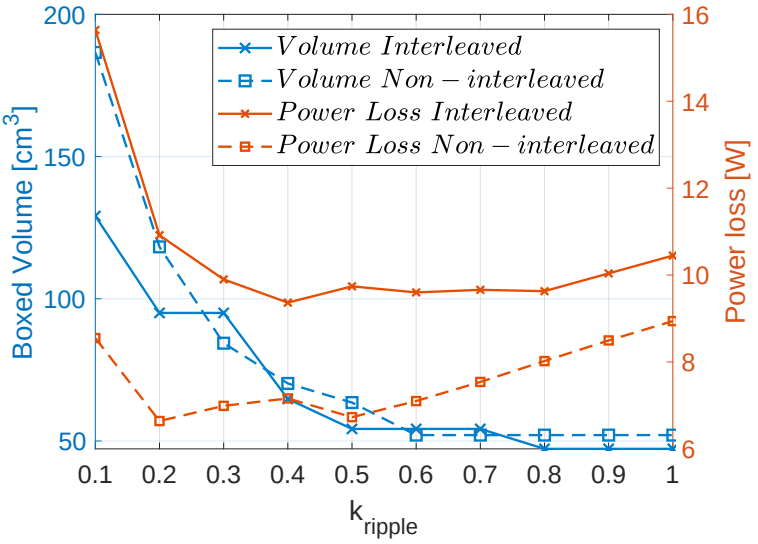


Figure 6.4: Comparison boost inductor volume and power loss at rated load in CCM of two-channel interleaved and non-interleaved PFC converter using one stack core of High-Flux, $\mu = 60$.

6.1.2 Inductor volume variation with angle α in QCM

Boost inductor volume with the variation of the point (angle) where, in mixed-conduction mode, the transition from CCM to DCM occurs, is investigated. Considering the same approach as for the CCM case, the non-interleaved and interleaved configurations conditions were used in order to obtain inductance values, find optimal cores and used the inductor design tool to obtain the boxed volume. Considering inductors based on core materials as in Figure E.2 in Appendix E, materials with the properties that resulted in minimized volumes, are selected for further analogy.

Non-interleaved PFC converter

In Figure E.2, it is shown how the boxed volume of the boost inductor is diminished as the design angle α is incremented. Operation of the boost inductor in QCM, when the angle is at 10° results in more period when the inductor current waveform is in CCM than in DCM. Consequently, the boxed volume at this point is higher than, at $\alpha = 60^{\circ}$, where, as the mixed conduction mode current will be more in DCM, and as the angle approaches towards $\alpha = 90^{\circ}$, the QCM current waveform will resemble more DCM operation. As the ripple current is higher in DCM than in CCM, meaning that more ripple factor is present, the inductor will be smaller in order to allow this current ripple.

High Flux (HF) one core of 60μ representing the green line on the graph have similar trend as for 125μ two stacked cores. There is an evident volume reduction using these cores, comparable with Kool Mu cores.

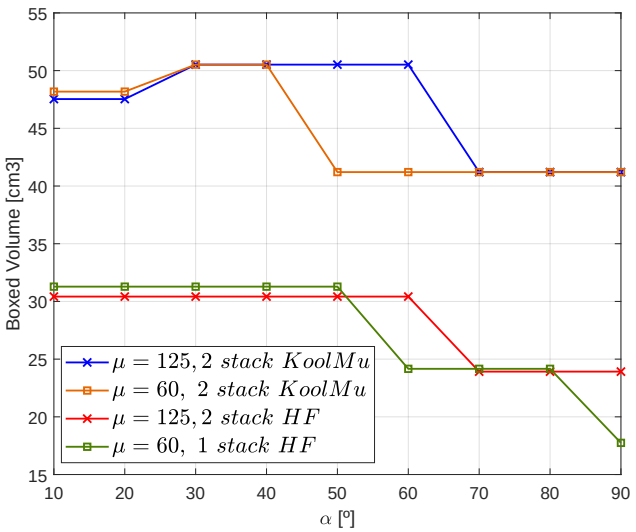


Figure 6.5: Non-interleaved PFC converter - Comparison of boost inductor volume and total losses in QCM for the optimum Kool Mu and High-Flux cores, obtained from *Magnetics*' Powder Cores, varying angle α.

Two-channel interleaved PFC converter in QCM

When in comes to interleaving two boost inductors, the total magnetic boxed volume is shown in Figure 6.6. There are not significant differences to the volume resulting in 6.6, but interleaving benefits need to be weighed. It is also noticeably that different permeabilities for the same materials are selected in the case of interleaved topology, as these resulted in lower volume. Hence, overall conclusion is that cores of High Flux contribute to volume optimization, and this volume drops considerably when QCM operation at around $\alpha = 60^{\circ}$ is selected. However, for a better conclusion, losses generated by the inductor under QCM opeartion have to be determined. For this purpose, making use of Equations 6.1 to 6.3, power losses are estimated and the obtained results are represtented in Figure 6.7. In the graphical representation of volume dependence on α shown in Figure 6.7, only *HF* cores are selected subsequently to previous observations. In contrast to volume obtained for a single inductor in QCM, using two interleaved inductors provide a fairly volume reduction in cm^3. Yet, there is a trade-off between volume reduction and total power losses augmentation. It must be considered that these losses are estimated only, as the current curves are piece-wise linear. Power loss in interleaved are slightly greater than in non interleaved, for example, at $\alpha = 60^{\circ}$, a difference of around 5 W considering total looses and the fact that they are due to presence of two inductors, can be acceptable as it compensates in other aspects such as reduced power losses and stress in boost power switches.

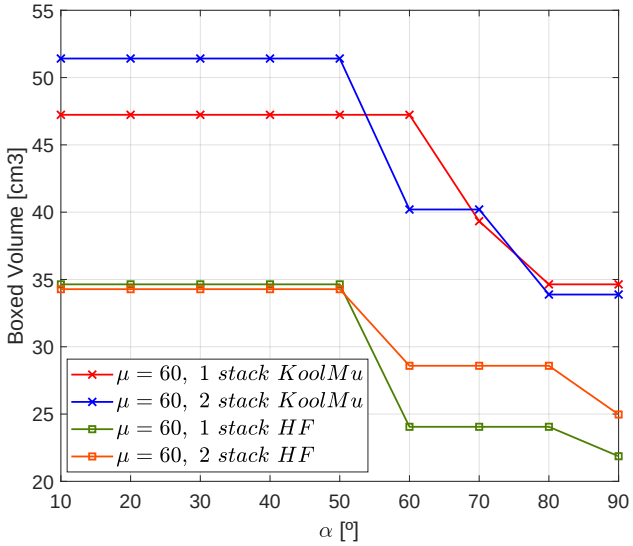


Figure 6.6: Two-channel interleaved PFC converter - Comparison of boost inductors total volume in QCM for Kool Mu and High-Flux cores with permeability 60 and different number of stack cores, obtained from *Magnetics'* Powder Cores, varying angle α.

Comparison interleaved and non-interleaved PFC converter

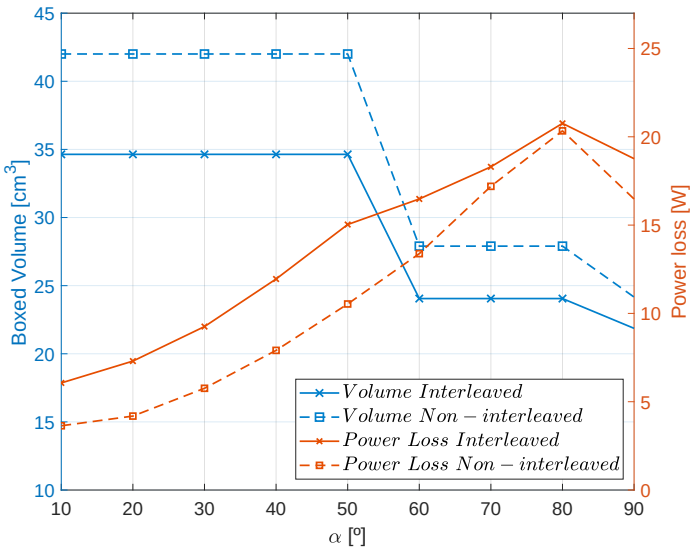


Figure 6.7: Comparison boost inductor volume and power loss in QCM of two-channel interleaved and non-interleaved PFC converter using one stack core of High-Flux, $\mu = 60$.

6.2 Selection of optimum k_{ripple} and α

The scope of this project is analyzing the performance of two channel interleaved PFC converter. Hereby, optimization of inductor boost volume for interleaved case in CCM and QCM which also involves DCM to some extent ($\alpha = 90°$), and input DM filter, are required in order to achieve a minimum total volume. The compromise for the selection of the optimum k_{ripple} and α regarding total volume and total inductor losses is shown.

Interleaved CCM

Interleaved PFC in CCM mode final results are collected together in Figure 6.8 below. Operating conditions are rated power, the fixed switching frequency according to project specifications. The curve of DM EMI filter volume (i.e. green curve in figure) is based on optimization made before according to the mapped most favorable number of stages in Chapter 5. It can be seen that as k_{ripple} increases, the inductance volume curve strongly descends, while DM EMI input filter volume curve experience only a small raise. Thus, in the range of 10% to 40% of k_{ripple}, the total volume is considerably large, while in the range after, it remains constant for the most part. Taking a closer look to the total losses, it is important to observe that the best operation point is not that which minimizes the inductor volume, rather, that which presents an overall good performance without

allowing too much increment in losses and that effects less in the EMI filter volume. For the design in case, a $k_{ripple} = 0.5$ is chosen.

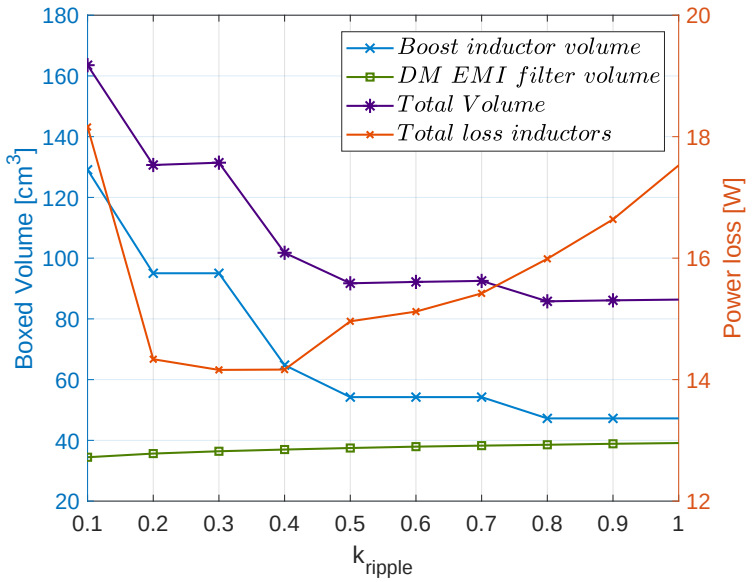


Figure 6.8: Boost inductor, DM EMI filter and total volume compared against power loss in boost and EMI filter inductors of two-channel interleaved PFC converter using one stack core of High-Flux, $\mu = 60$, varying k_{ripple}.

Interleaved QCM

In the case of QCM mode, there is seemingly a reduction in boost inductor volume compared to CCM. However, there is an apparent increase in total loss, that could affect the overall efficiency of the converter. In this regard, careful selection of angle α has to be made. From Figure 6.9, the point where the mixed conduction mode of operation becomes DCM, is at $\alpha = 90°$. Relatively, this is also the transition point where the total volume is fully minimized, the total loss is maximized.

As a consequence, a trade-off between efficiency and power density (i.e. reduction of volume) arise. In the application at hand, the objectives efficiency and high power density are weighted. In order to justify a selection, an operating point where the inductor losses do not affect the overall efficiency and at the same time, the input filter volume and boost inductor volume reduction is not compromised, a selection of $\alpha = 60°$ becomes satisfactory.

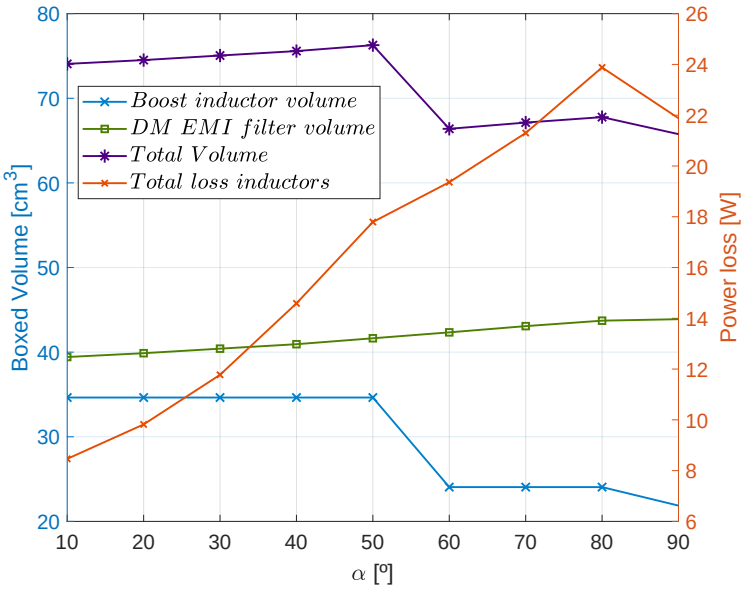


Figure 6.9: Boost inductor, DM EMI filter and total volume compared against power loss in boost and EMI filter inductors of two-channel interleaved PFC converter using one stack core of High-Flux, $\mu = 60$, varying angle α.

Comparison CCM, QCM and DCM

Resuming the important parameters obtained as a result of values selected in previous sections, for ripple ratio and mode transition point expressed in degrees, α, Table 6.1 is completed. A better insight can be acquired in how the different operating points influence in volume, losses, power factor and consequently, in converter efficiency and power density. It is important to mention that selecting as optimum $k_{ripple} = 0.5$ and $\alpha = 60^{\circ}$ the aim is for minimum volume more than lower power loss. For choosed values of ripple factor the inductance in CCM becomes 3.8 mH, while using alpha angle of 60° in QCM and 90° for DCM, inductance values of 0.56 mH and 0.35 mH are obtained. The reciprocal of inductance in terms of volume is given in table as V_L. Filter volume V_f is calculated also based on the number of filter stages selection from the graph in Figure 5.7 for estimated required attenuation via simulation. Resulted that two filter stages in DM are required in all three current modulation modes, since the required attenuation is slightly above 50 dB. QCM becomes more relevant as the power factor is nearly the same as for CCM, and the approximated power losses are giving a midpoint, still below those given by DCM. There is also a power density increase when using QCM with respect to CCM, due to a reduction of around 27% in comparison to CCM mainly because of boost inductor size reduction.

Taking into account the total inductor volume volume $V_{L,total} = V_L + V_f$, this reduction can be calculated as follows:

$$\%\ reduction\ V_{L,total} = \left(\frac{V_{L,total}(CCM) - V_{L,total}(QCM)}{V_{L,total}(CCM)} \right) \times 100 = 27.6167\% \tag{6.7}$$

Therefore, even though EMI filter is larger in QCM and DCM the overall PFC converter volume is reduced.

Comparison simulation results for the three current modulations			
	CCM	QCM	DCM
Boost inductance, L	3.8 mH	0.56 mH	0.35 mH
Boost inductor volume, V_L	54.24 cm^3	24.05 cm^3	21.87 cm^3
DM EMI filter volume, V_f	37.48 cm^3	42.34 cm^3	43.89 cm^3
Number of filter stages, n_f	2	2	2
Total boost inductor and filter volume, $V_{L,total}$	91.72 cm^3	66.39 cm^3	65.76 cm^3
Power loss boost and filter inductors, P_L	14.96 W	19.36 W	21.88 W
Power loss semiconductor devices, P_{switch}	20.22 W	19.7 W	20.02 W
Power factor, PF	0.9977	0.9930	0.9855
Converter efficiency, η	96.48 %	96.1 %	95.81 %
Power density, PD	2.13 W/cm^3	2.25 W/cm^3	2.27 W/cm^3

Table 6.1: Comparison simulated results at rated load, based on selection of optimum k_{ripple} and α, in a two-channel interleaved PFC converter operating in CCM, QCM and DCM.

6.3 DM EMI noise simulations

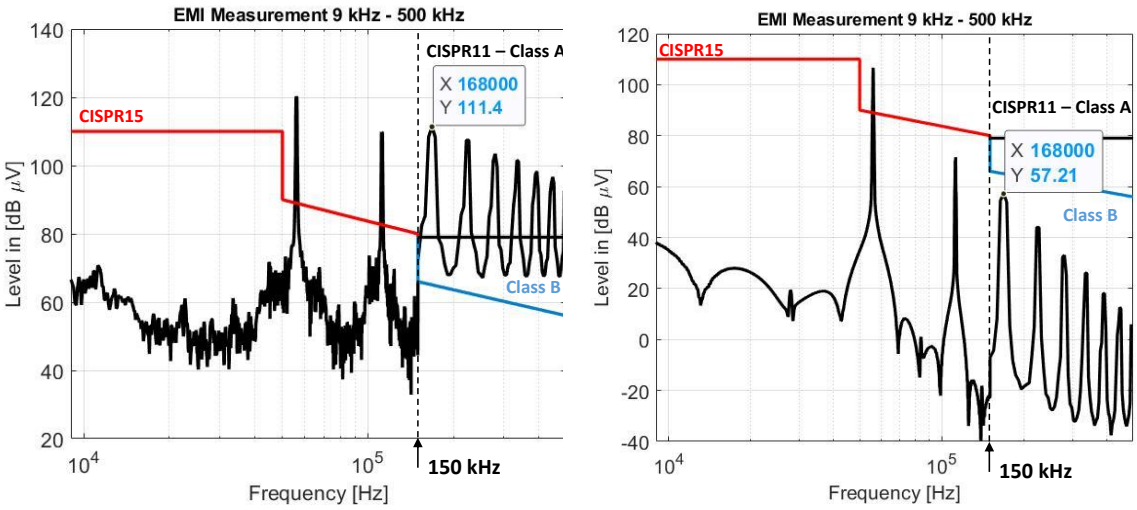
Based on the selected parameters that determine the minimum boost inductor volume from the previous sections ($\alpha = 60^\circ$ and $k_{ripple} = 0.5$), the optimum component values of the EMI filter are found for each current operating mode following the procedure explained in Chapter 5. The goal is to design a DM EMI filter for the regulated frequency range of Band B for both *Class A* and *Class B* equipment. The CISPR11 QP standard is more restrictive for Class B, as shown in Figure 5.2, therefore the attenuation required by the filter is calculated using the limit for CISPR11-*ClassB* which is 65 dB at the design frequency ($f_D = 168\ kHz$) while for *Class A* it is 79 dB. This will ensure that the high-frequency noise emissions will be below both limits. The DM EMI filter parameters are summarized in Table 6.2. As expected, the attenuation required is higher in QCM and DCM in comparison to CCM operation due to the increase in current ripple and the discontinuous current waveforms. This is reflected in higher filter component values which means lower cut-off frequency and consequently, larger EMI filter size.

DM EMI filter parameters for the three current modulations			
	CCM	QCM	DCM
Design frequency, f_D	68 kHz	68 kHz	68 kHz
Quasi-peak voltage, $U_{QP,max}$	111.4 $dB\mu V$	126.4 $dB\mu V$	130.6 $dB\mu V$
Attenuation required, $Att_{req,LC}$	52.4 dB	67.4 dB	71.1 dB
DM EMI filter inductance, L_{dm}	18 μH	28 μH	30.5 μH
DM EMI filter capacitance, C_{dm}	560 nF	820 nF	1000 nF
Damping inductance, L_d	18 μH	28 μH	30.5 μH
Damping resistance, R_d	2.5 Ω	2.5 Ω	2.5 Ω

Table 6.2: DM EMI filter parameters used for running the simulations.

Simulations are conducted to verify that the DM EMI filter is able to provide the attenuation required to fulfill standard CISPR11. Figures 6.10, 6.11 and 6.12 show the conducted emissions, obtained using quasi-peak detection method, of a two-channel interleaved PFC converter working in CCM, QCM and DCM, respectively. In subfigures (a), the noise spectrum that results without the EMI filter implemented shows that the noise peaks are well above the standard. This emphasizes the need of an EMI filter for reduction of the conducted emissions generated by the PFC converter. By implementing the DM EMI filter, using the parameters from Table 6.2, the simulation results are shown in subfigures (b). It is observed that the noise peak voltages satisfy the CISPR11 standard limits for both *Class A* and *Class B* equipment.

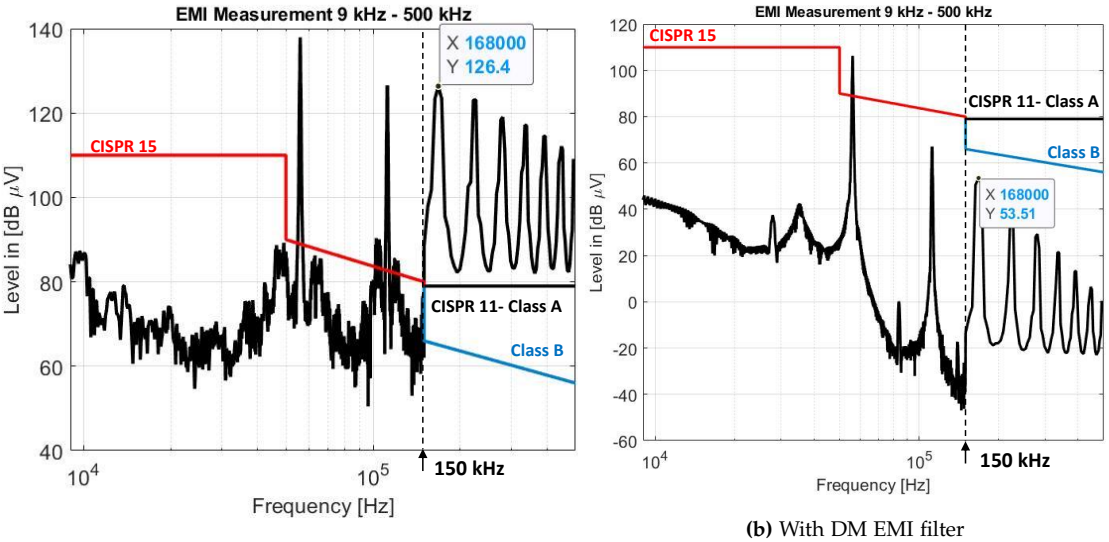
It is interesting to note that the emissions do not comply with CISPR15 standard in Band A ($9\ kHz - 150\ kHz$). The second order harmonic at $56\ kHz$ exceeds the standard QP limit in the three current modulations. This is because the EMI filter was designed to meet Band B QP limits. However, if it is necessary to comply with CISPR15 standard one possible way to reduce the emissions below $150\ kHz$ is to add a capacitor in parallel with the original capacitor C_{DM} in order to provide the extra attenuation to satisfy the QP limits over all the frequency range [40].



(a) Without DM EMI filter

(b) With DM EMI filter

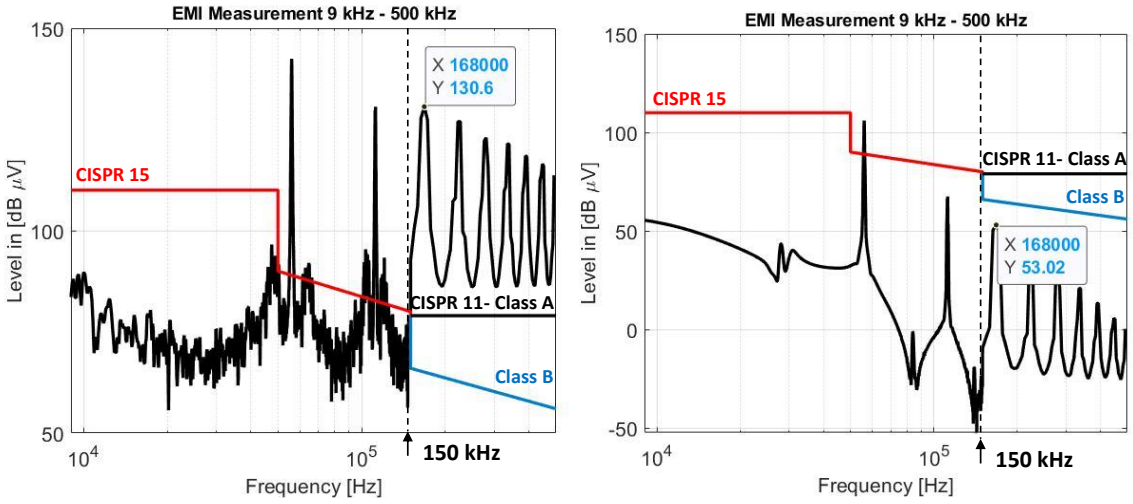
Figure 6.10: Conducted emissions in the range 9 $kHz - 500$ kHz for two-channel interleaved PFC converter operating in CCM at full load..



(a) Without DM EMI filter

(b) With DM EMI filter

Figure 6.11: Conducted emissions in the range 9 $kHz - 500$ kHz for two-channel interleaved PFC converter operating in QCM at full load.

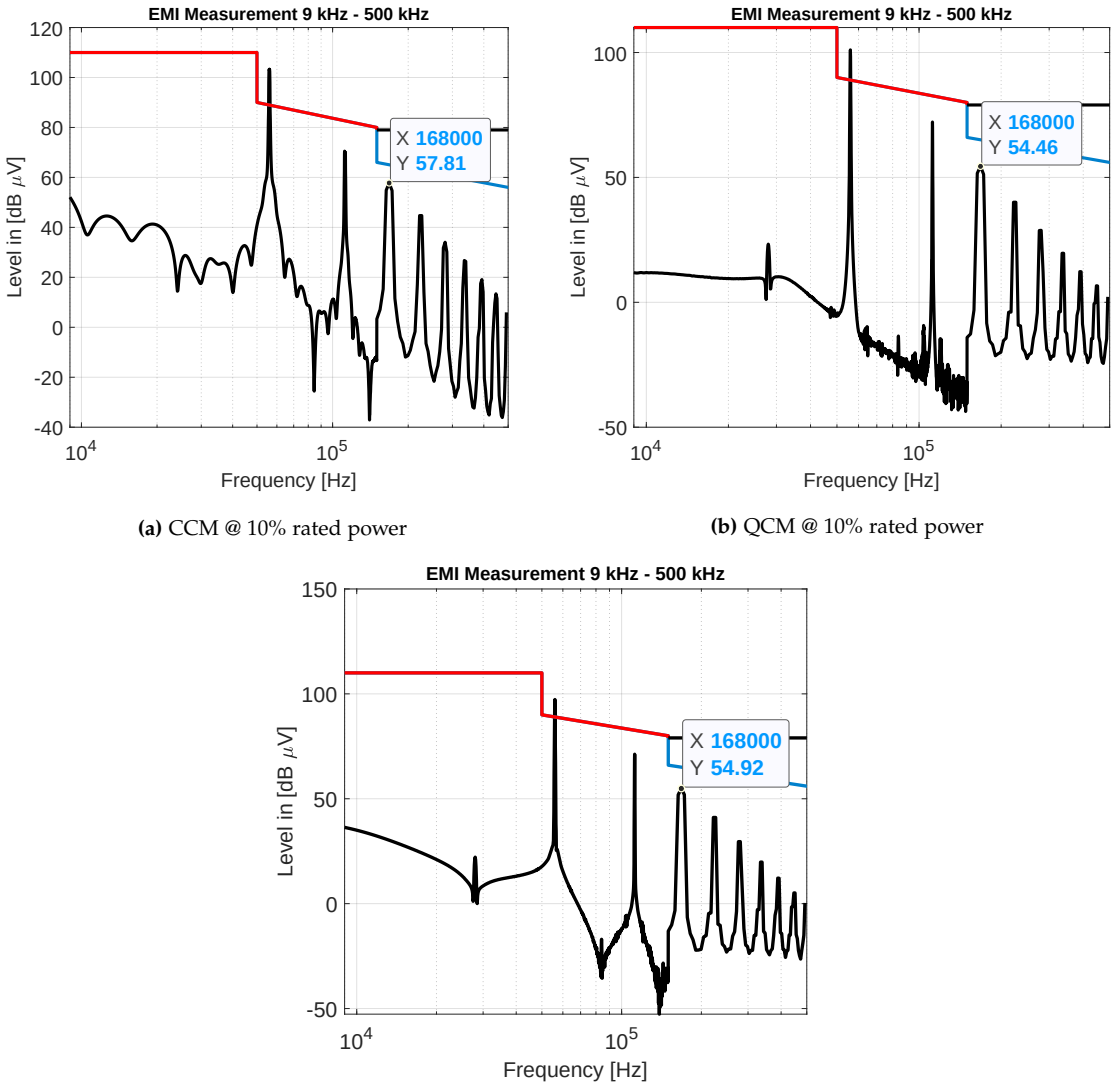


(a) Without DM EMI filter

(b) With DM EMI filter

Figure 6.12: Conducted emissions in the range 9 $kHz - 500$ kHz for two-channel interleaved PFC converter operating in DCM at full load.

The performance of the EMI filter at lower load conditions should also be considered as the input current will get more discontinuous with higher current ripple which means that the noise emissions will increase at the design frequency f_D. As the EMI filter was designed at rated power $P_o = 1$ kW it must be verified that it can still fulfill the CISPR11 QP limits for the worst case that will be the lowest power level (10% $P_o = 100$ W). If the high frequency conducted emissions exceed the limits the filter component values would need to be modified. Figure 6.13 shows that in the three current modulation techniques, when reducing the output power level, the conducted emissions are higher. Nevertheless, the DM EMI filter is able to maintain the noise peaks under the QP-limit for Band B.



(a) CCM @ 10% rated power

(b) QCM @ 10% rated power

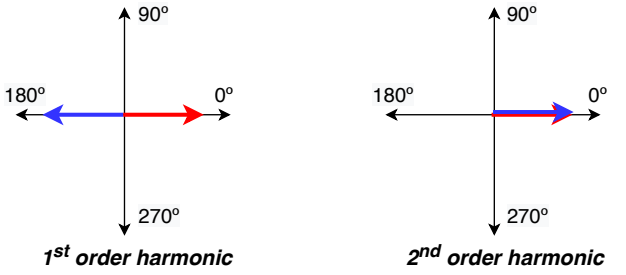
(c) DCM @ 10% rated power

Figure 6.13: Simulation results for CCM, QCM and DCM of noise emissions in the range 9 $kHz - 500\ kHz$ at 10% rated power, $P_o = 100\ W$.

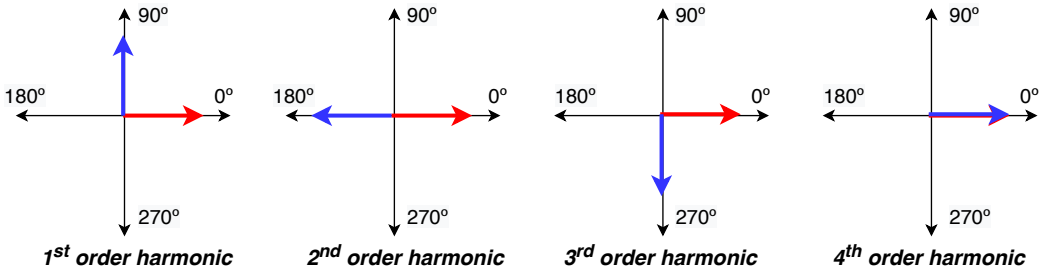
6.4 Unconventional phase-shift control

Up to this point only the conventional interleaving scheme has been considered. In this control scheme the two interleaved boost cells operate at $\gamma = 180^{\circ}$ phase-shift. However, interleaving does not always imply reduction of the DM EMI filter size. This will highly depend on the selection of the switching frequency because f_{sw} will determine the design frequency f_D for the EMI filter in the regulated range $150\ kHz - 30\ MHz$. For instance, a non-interleaved topology may have the same f_D as an interleaved topology which will lead to no benefit, from the point of view of minimizing the EMI filter volume, when implementing conventional interleaving control.

As proposed in [49], it is possible to implement different phase-shift control techniques to obtain reduction of the EMI filter size, in comparison to non-interleaved PFC converter, without the need to modify f_{sw}. This is illustrated in the noise phasor diagrams of Figure 6.14.



(a) Phase-shift angle $\gamma = 180^{\circ}$



(b) Phase-shift angle $\gamma = 90^{\circ}$

Figure 6.14: Noise phasor diagram for (a) conventional and (b) unconventional phase-shift control for two-channel interleaved topology.

From the phasor diagram of the conventional interleaved scheme in Figure 6.14a, it is seen that the 1^{st} order harmonic gets cancelled whereas for the 2^{nd} harmonic the noise sources are in phase and they add together. This means that, using a phase-shift of $\gamma =$

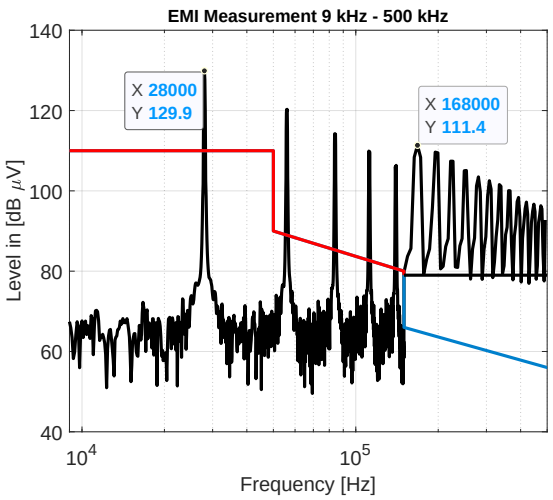
180° between the inductor currents, yields to cancellation of the odd harmonics while the even harmonics remain the same as in non-interleaved.

On the other hand, if instead phase-shift of $\gamma = 90^\circ$ is implemented, the 1^{st} and 3^{rd} order harmonic magnitudes are reduced. The 2^{nd} harmonic will be cancelled out as it is at opposite phase and the 4^{th} harmonic is added up. This process is repeated for the higher order harmonics. Thus, 90° phase-shift control allows reduction of the noise magnitude of the odd harmonics. The 2^{th}, 6^{th}, 10^{th}... order harmonics are cancelled while the $4^{th}, 8^{th}, 12^{th}$... order harmonics remain the same as non-interleaved scheme [49].

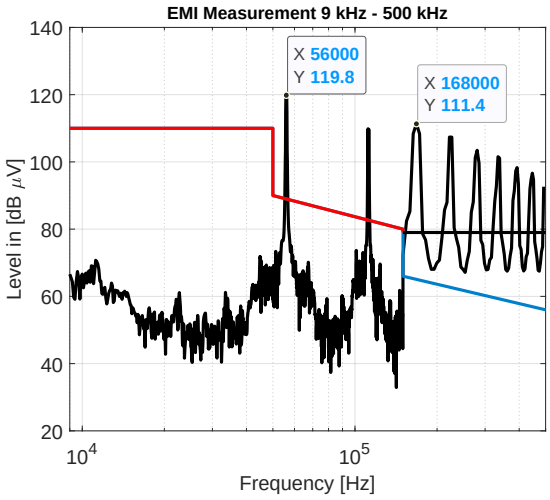
This phase-shift control scheme is implemented for the two-channel interleaved PFC converter under study. The reason why 90° phase-shift is selected instead of 180° or other different angles is the design frequency at which the EMI filter needs to provide the required attenuation. As $f_{sw} = 28\ kHz$, the first noise peak appearing beyond 150 kHz is the 6^{th} order harmonic ($f_D = 6 \cdot f_{sw} = 168\ kHz$). This means that the conventional control scheme will not lead to smaller EMI filter, in comparison to the non-interleaved PFC converter, because only the odd harmonics are cancelled. However, as has been shown that 90° phase-shift allows the cancellation of the 6^{th} harmonic, the first peak after 150 kHz will be the 7^{th} order harmonic which has lower magnitude. This is verified by simulations with the results being depicted in Figure 6.15.

As an example, only the simulation results for two-channel interleaved PFC converter operating in CCM are shown and the final reduction in EMI filter size and resulting power density are summarized in Table 6.3. Figure 6.15a corresponds to the quasi-peak noise spectrum of a non-interleaved converter as the phase-shift is $\gamma = 0^\circ$. It is seen that all the multiples of the switching frequency are present in the spectrum. The design frequencies corresponding to Band A and Band B frequency range are highlighted. Comparing with the simulation result of Figure 6.15b (conventional scheme), only the even harmonics are present in the noise emissions because using phase-shift of 180° allows cancellation of the odd harmonics. The design frequency for Band B is the same in both cases ($f_D = 168\ kHz$) resulting in equal required attenuation for the DM EMI filter ($Att_{req,LC} = 111.4 - 65 + 6 = 52.4\ dB$). Hence, in this case interleaving is not beneficial for minimizing EMI filter volume.

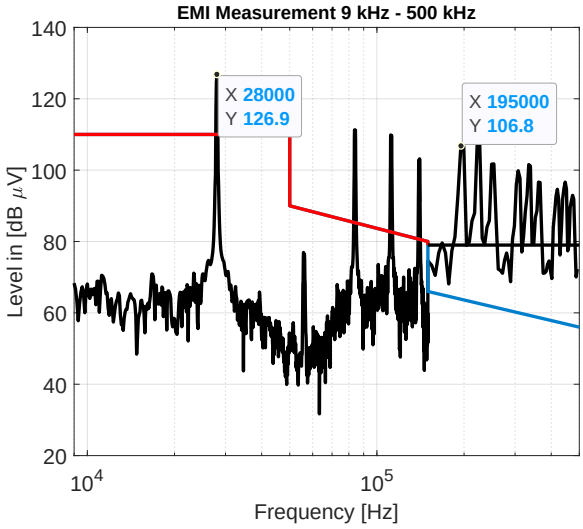
On the other hand, if instead 90° phase-shift is applied the 6^{th} order harmonic is cancelled as seen in Figure 6.15c. Therefore, the design frequency will be chosen at the next appearing peak, $f_D = 7 \cdot f_{sw}$, resulting in a reduction of the harmonic magnitude. In this case the required attenuation is $Att_{req} = 106.8 - 64 + 6 = 48.8\ dB$. Moreover, the design frequency for Band A is at $f_{sw} = 28\ kHz$ which corresponds to the first order harmonic and indeed the peak voltage is reduced 3 dB with respect to the non-interleaved operation. The size of the EMI filter is also reduced compared to the conventional interleaving scheme because the first peak appears before 50 kHz where the CISPR15 standard requirement is not that restrictive as at $f_D = 56\ kHz$. This way, it has been proof by simulations that for the two-channel interleaved PFC converter analyzed in this work interleaving at 90° phase-shift provides more benefits than using the conventional control scheme.



(a) Phase-shift angle $\gamma = 0^{\circ}$.



(b) Phase-shift angle $\gamma = 180^{\circ}$



(c) Phase-shift angle $\gamma = 90^{\circ}$

Figure 6.15: Simulation results of noise emissions in the range 9 $kHz - 500$ kHz using different phase-shift angles for a two-channel interleaved PFC converter operating in CCM.

Table 6.3 summarizes the results obtained implementing the three different phase-shift angles ($0^{\circ}, 180^{\circ}$ and 90°) in order to compare the EMI filter total volume and power density achieved with non-interleaved, conventional interleaved and non-conventional interleaved control schemes. The results are obtained at full rated power $P_o = 1\ kW$ operation in CCM, QCM and DCM. Extracting relevant volumetric values, there are no significant differences between interleaved and single arrangement when the first mentioned is at $\gamma = 180^{\circ}$, results begin to differentiate more when using the non-conventional scheme.

Comparison volumes and power density for different phase-shift angles			
Non-interleaved - $\gamma = 0^{\circ}$	CCM	QCM	DCM
DM EMI filter volume, V_f	37.48 cm^3	42.34 cm^3	43.89 cm^3
Total boost inductor and filter volume, V_{total}	100.98 cm^3	70.25 cm^3	68.05 cm^3
Total converter volume, V_{conv}	478.52 cm^3	447.78 cm^3	445.60 cm^3
Power density, PD	2.08 W/cm^3	2.23 W/cm^3	2.244 W/cm^3
Interleaved - $\gamma = 180^{\circ}$			
DM EMI filter volume, V_f	37.48 cm^3	42.34 cm^3	43.89 cm^3
Total boost inductor and filter volume, V_{total}	91.72 cm^3	66.39 cm^3	65.76 cm^3
Total converter volume, V_{conv}	469.26 cm^3	443.93 cm^3	443.3 cm^3
Power density, PD	2.130 W/cm^3	2.250 W/cm^3	2.270 W/cm^3
Interleaved - $\gamma = 90^{\circ}$			
DM EMI filter volume, V_f	34.18 cm^3	38.67 cm^3	38.96 cm^3
Total boost inductor and filter volume, V_{total}	88.42 cm^3	62.72 cm^3	60.83 cm^3
Total converter volume, V_{conv}	465.96 cm^3	440.26 cm^3	438.38 cm^3
Power density, PD	2.147 kW/dm^3	2.273 kW/dm^3	2.281 kW/dm^3

Table 6.3: Comparison volumes and power density for three different phase-shift angles in a PFC converter operating in CCM, QCM and DCM.

Thus, reduction in volumes considering the three cases of current modulation, are briefly discussed below, using unconventional $\gamma = 90^{\circ}$:

- There is a 26.2 % reduction of total converter volume with respect to non-interleaved for CCM, compared to only 19.4 % in conventional phase displacement
- In QCM operation, the converter volume is reduced 1.68 % with respect to non-interleaved compared against 0.8 % reduction using the conventional scheme.
- For DCM a reduction of 1.6% is obtained with respect to non-interleaved while a volume reduction of 0.5% is achieved with non-conventional control.

To put in evidence the QCM technique relative to CCM, the converter volume drops around 6 % with a reduction of approximately 30% in the total inductors volume for the three different phase-shift angles. This results in an improvement of the converter power density when operating in QCM while the total converter efficiency is not significantly reduced as shown in Table 6.1. It is observed that operating in QCM, with angle $\alpha = 60^{\circ}$, does not show significant differences with DCM operation. The analysis of the interleaved PFC boost converter has proof the feasibility of implementing QCM modulation to greatly reduce the inductor boost size and increase the power density of the PFC converter.

Chapter 7

Conclusion and future work

7.1 Conclusion

Interleaved PFC converters are widely used nowadays with the goal of achieving both high efficiency and high power density. In this work, emphasis is put on design and performance determination of a two-channel interleaved boost PFC converter operated under three current modulation techniques, CCM, DCM and QCM. Largely due to operation in this modes, component sizing is affected. Interleaving adds different benefits in reducing the components volume leading to an increase in power density.

In order to evaluate such scenario, analytical derivation of components and implementation of a two-channel interleaved is described. A first validation of component sizing was conducted via simulations. It has been shown that analytical parameters (angle θ, for CCM and DCM, α in QCM) for inductance derivation that keep the converter functioning at specified operating points in the three current modes were appropriately selected.

As an important part of PFC converter, DM EMI filter component volume optimization and virtual measurement of EMI noise is addressed. In this regard, noise filtering capacitors and inductors (C_{DM} and L_{DM}) volume optimization proposed in literature was studied and implemented in this work.

Afterward, the optimum boost inductor was addressed through an optimization procedure consisting in iterative searching for the three different materials (Kool Mu, High Flux and MPP) at two permeabilities of 60 and 125. It was concluded that for the design at hand, High Flux cores with permeability 60 gives the minimum volume in all the cases. This helped to selection of k_{ripple} and α, for CCM and QCM respectively, non-interleaved and interleaved configurations, by analyzing the variation of boost inductor volume with these. Eventually, with all the information necessary, inductor current ripple factor for converter driven in CCM was found as optimum at $k_{ripple} = 0.5$, and for partial CCM and partial DCM, namely QCM, the angle $\alpha = 60^{\circ}$ where the transition between the mixed modes occurs, are found to be best choice made considering that, a compromise between efficiency and high power density needs to be accepted for the cur-

rent application, aiming for compact design and efficient power conversion. Subsequently, a final efficiency prediction and power density could be obtained, including the volume of input filter in the total, final power density calculation. It is found that the power density and efficiency, considering semiconductor power losses and inductors losses, in CCM is $PD_{CCM} = 2.13\ kW/dm^3$ and $\eta_{CCM} = 96.48\%$. For QCM operation it results in $PD_{QCM} = 2.25\ kW/dm^3$ and $\eta_{QCM} = 96.1\%$.

Conclusions derived are that depending on different current operation modes, component selection and PFC boost topology case, if non-interleaved or interleaved and phase shift angle between interleaved cells, the overall performance of the converter is affected.

Finally, statement of results from examination of single-phase two-channel interleaved PFC boost converter performance highlight the potential of quasi-continuous conduction mode (QCM) to increase the overall performance and power density, while total converter efficiency is mostly maintained.

7.2 Future work

In this section, future work is suggested, in order to improve or to implement objectives that were out of the scope of the work carried out in this thesis. Different scenarios, which, due to the limited time period of the a semester, have not been investigated, are proposed as follows:

- For this work, a Hybrid Si IGBT - SiC boost diode DIPPFC from Super Mini family packages was considered. However, with the developed test setup, there is a Full SiC DIPPFC module available, matching the same footprint and design considerations are transferable to the use of last mentioned power module. According to Mitsubishi [27], full SiC DIPPFC allows 45% power loss reduction compared to Hybrid module, making it worthy of investigation.

- In the DM EMI Filter design and volume optimization, film capacitors that gave the minimum volume (i.e. Kemet) data was used in calculations. However, as mentioned in Chapter 5, multilayer ceramic capacitors from muRata could be considered for further research and implementation in the filter design, as they could provide lower volume.

- Industry state of the art propose efficient microcontroller unit controlled high power PFC, by employing two phase current modulation [50]. The main idea is to control the converter operation according to the load power percentage %. If output power drops below 50 % of the peak power, the converter operates in DCM, otherwise, at high powers it operates in quasi-resonant mode. This approach need to be analyzed for further improvements in terms of converter efficiency, by changing the modulation modes according to the load power.

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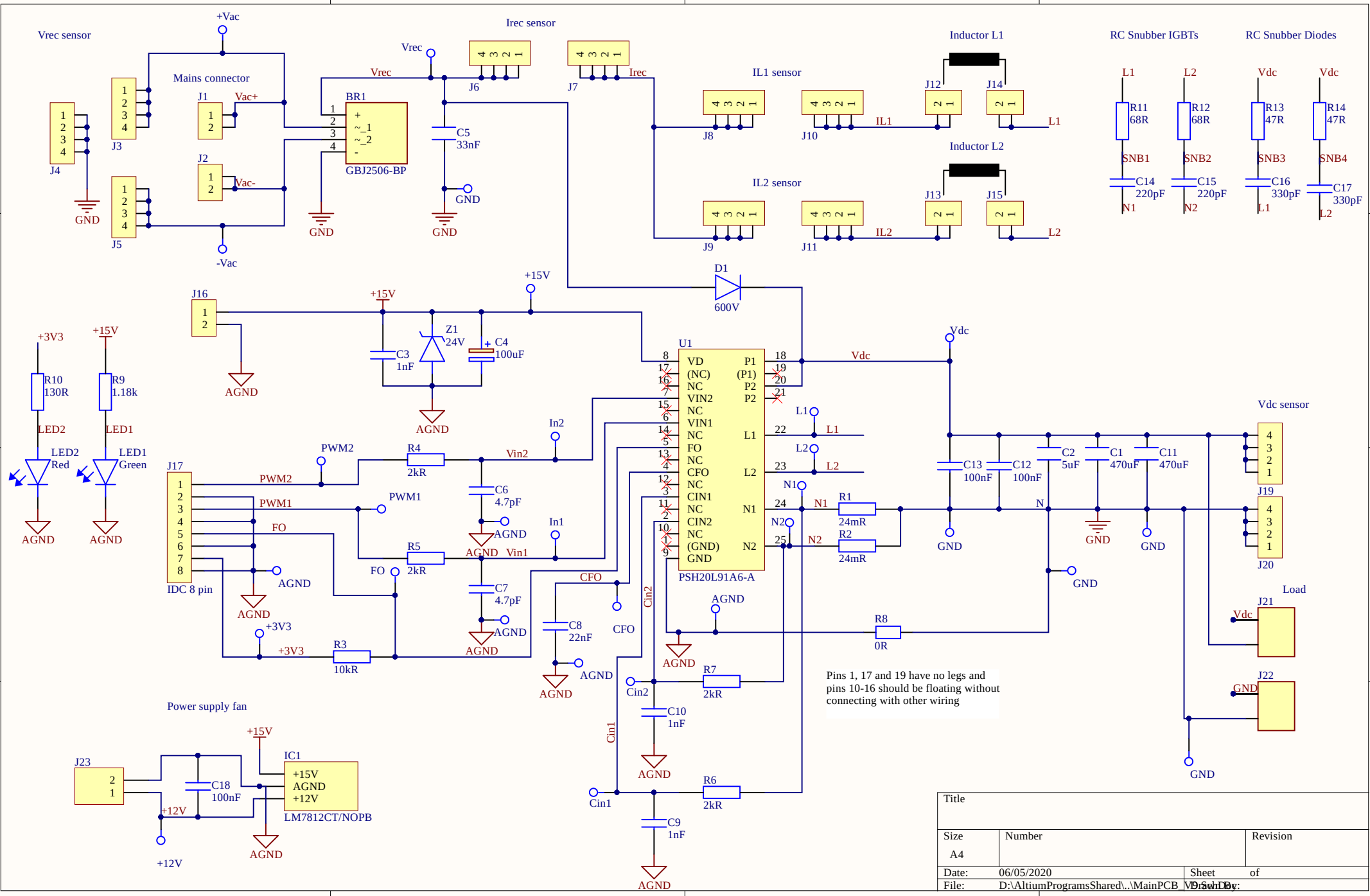
Appendix A

PCB Schematics

Figure A.0: Two-channel interleaved PFC (PSH20L91A6-A module) converter schematic for the application Main PCB:


Vrec sensor
+Vac
Mains connector
J1
Vac+
J2
Vac-
J3
J4
J5
-Vac
GND
BR1
GBJ2506-BP
Vrec
Irec sensor
J6
J7
Irec
C5
33nF
IL1 sensor
IL2 sensor
J8
J9
J10
J11
IL1
IL2
Inductor L1
Inductor L2
J12
J13
J14
J15
L1
L2
RC Snubber IGBTs
RC Snubber Diodes
R11
68R
R12
68R
R13
47R
R14
47R
SNB1
SNB2
SNB3
SNB4
C14
220pF
C15
220pF
C16
330pF
C17
330pF
N1
N2
Vdc
D1
600V
+15V
+3V3
J16
AGND
C3
1nF
Z1
24V
C4
100uF
U1
VD
(NC)
NC
VIN2
NC
VIN1
NC
FO
NC
CFO
NC
CIN1
NC
CIN2
NC
(GND)
GND
P1
(P1)
P2
P2
L1
L2
N1
N2
PSH20L91A6-A
R10
130R
R9
1.18k
LED2
LED1
LED2
Red
LED1
Green
J17
IDC 8 pin
PWM2
PWM1
FO
R4
2kR
R5
2kR
R3
10kR
Vin2
Vin1
In2
In1
C6
4.7pF
C7
4.7pF
R1
24mR
R2
24mR
C13
100nF
C12
100nF
C2
5uF
C1
470uF
C11
470uF
Vdc sensor
J19
J20
J21
J22
Load
R8
0R
CFO
Cin2
Cin1
C8
22nF
C10
1nF
C9
1nF
R7
2kR
R6
2kR
Pins 1, 17 and 19 have no legs and pins 10-16 should be floating without connecting with other wiring
Power supply fan
J23
C18
100nF
IC1
+15V
AGND
+12V
LM7812CT/NOPB
Title
Size
A4
Number
Revision
Date:
06/05/2020
Sheet
of
File:
D:\AltiumProgramsShared\..\MainPCB_V3.SchDoc
Drawn By:

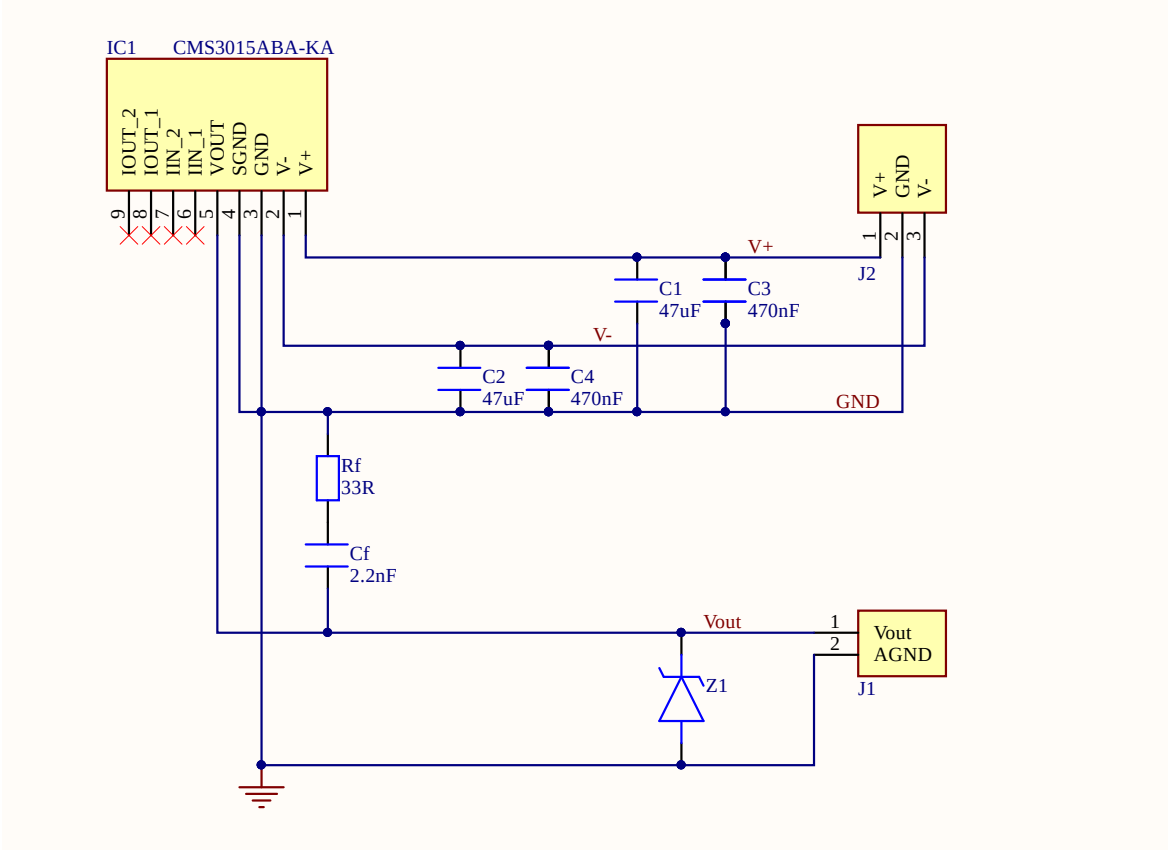


Figure A.1: CMS3015 Schematic for rectified input current and inductor currents, denoted as I_{rec} sensor and I_{L1}, I_{L2} sensor respectively, on the main converter schematic

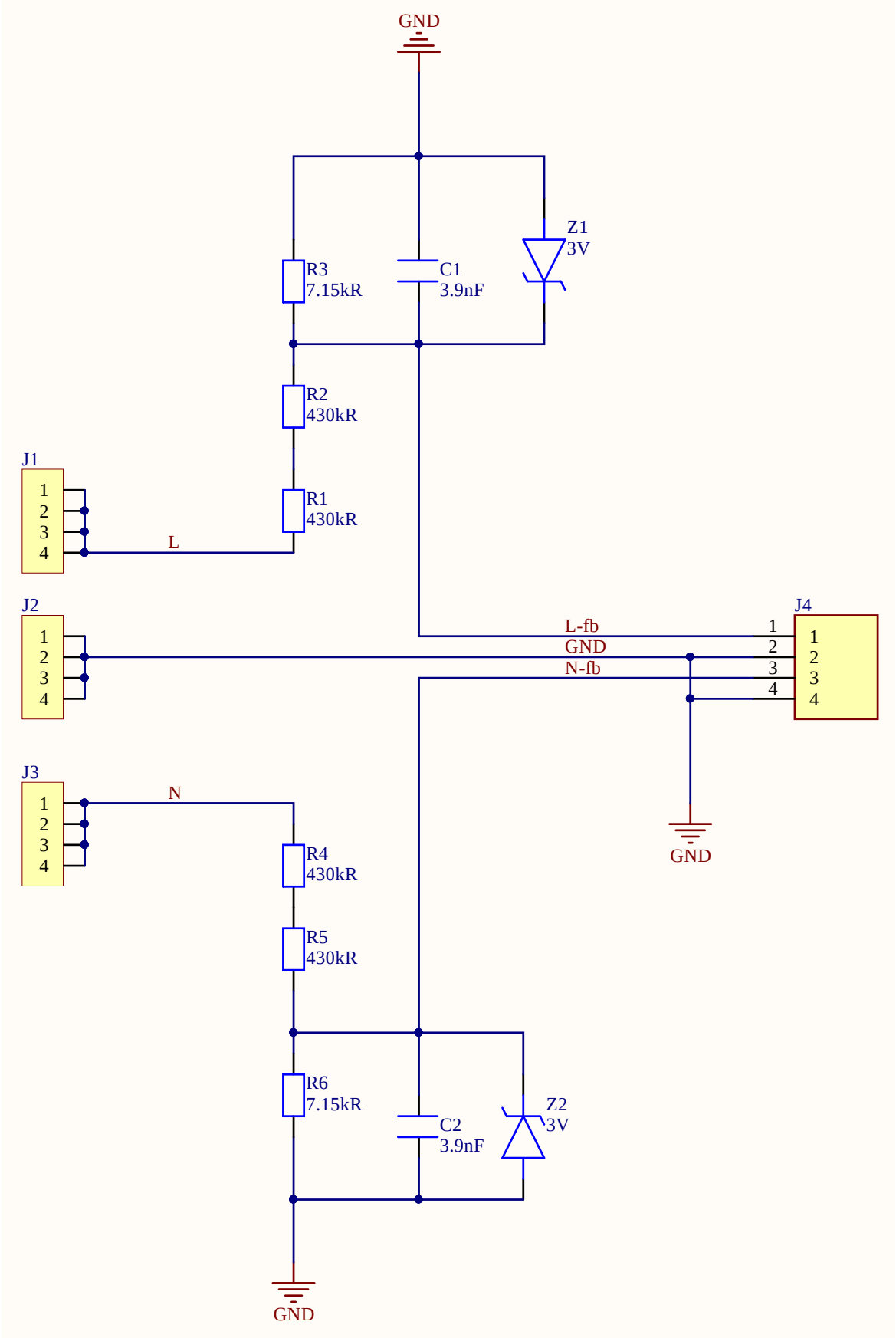


Figure A.2: AC voltage divider for line and neutral AC input voltage sensing network

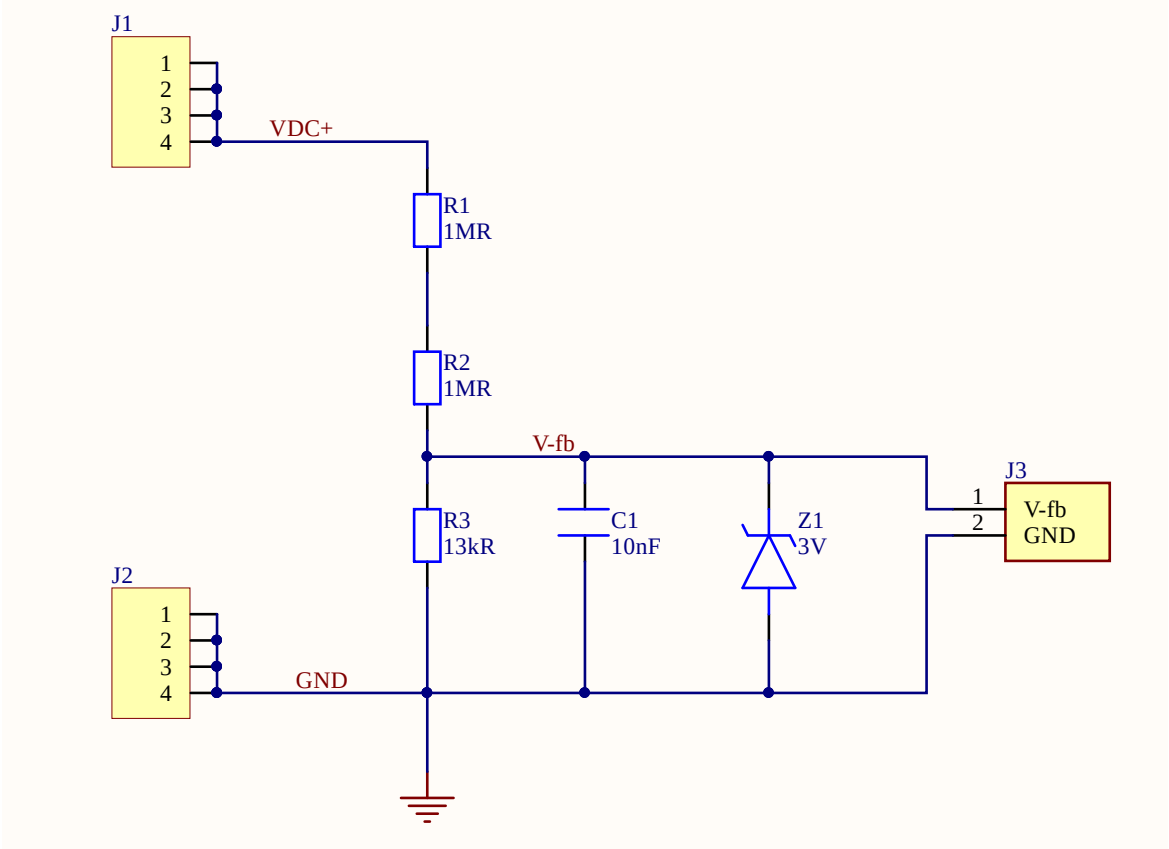


Figure A.3: DC voltage divider for VDC output voltage sensing network

Appendix B

PCB Layouts

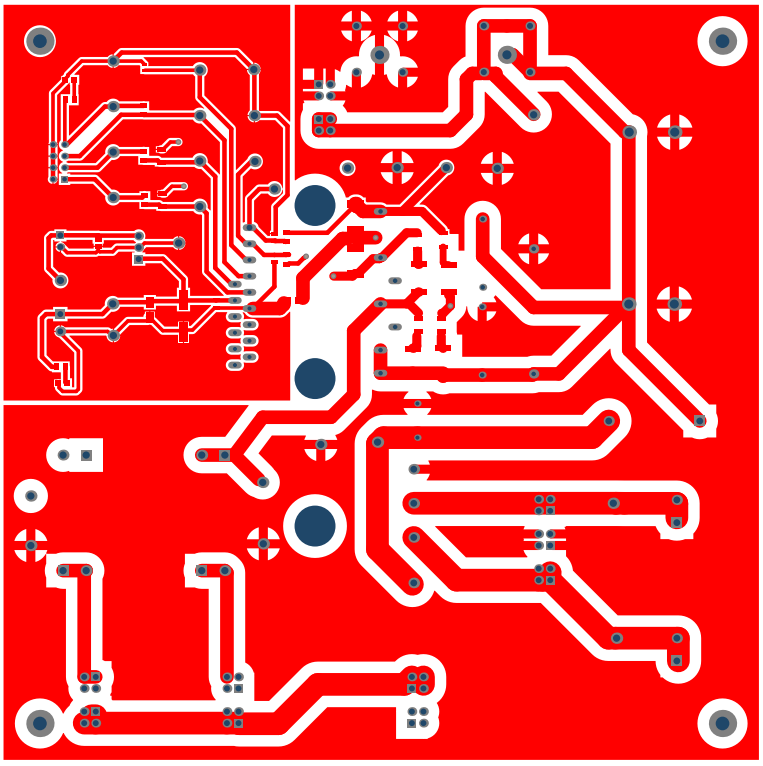


Figure B.1: Top layer of the Main PCB.

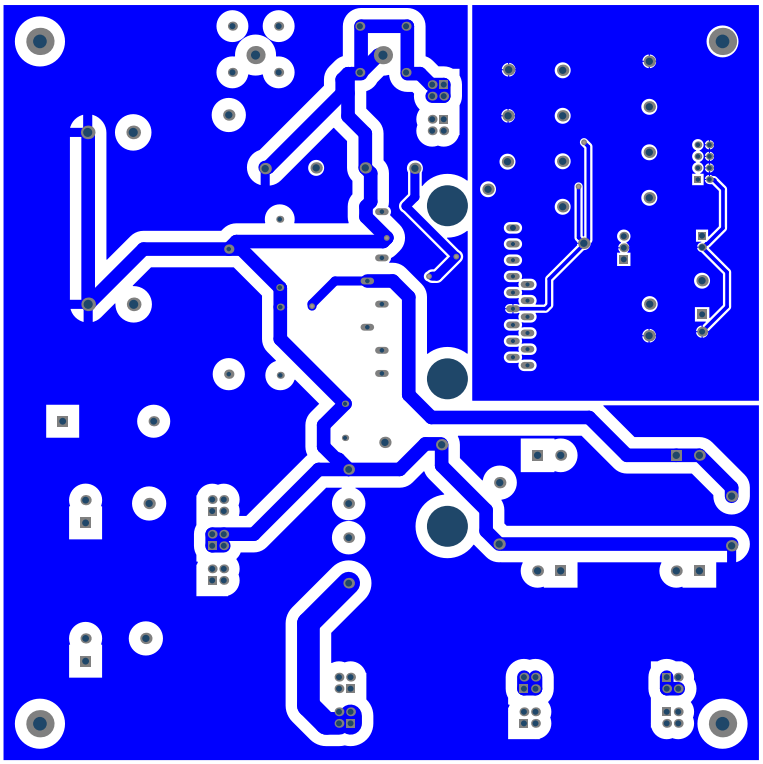
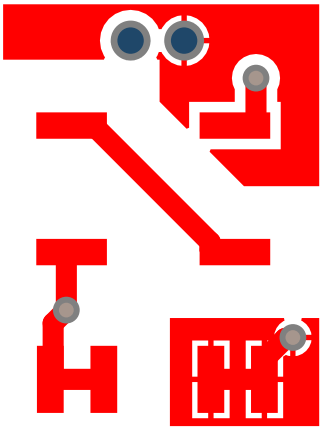
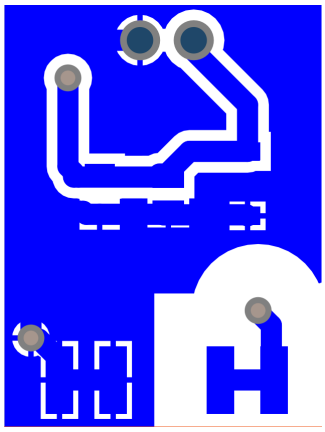


Figure B.2: Bottom layer of the Main PCB.

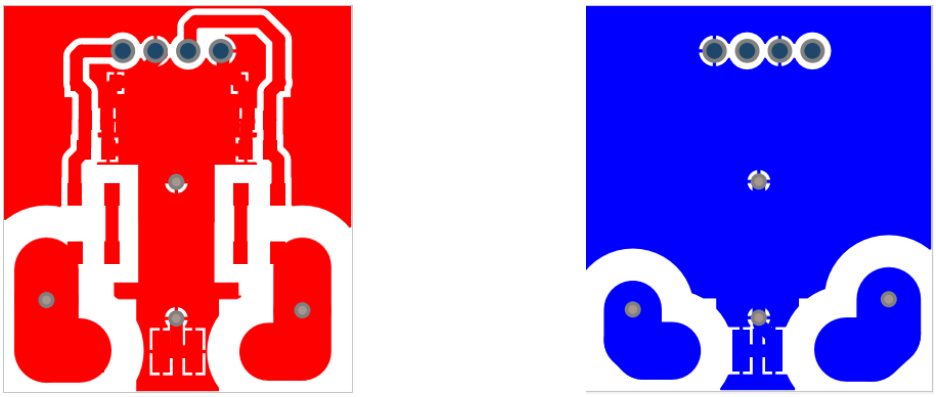


(a) Top layer.



(b) Bottom layer.

Figure B.3: DC voltage sensor PCB layout.



(a) Top layer.

(b) Bottom layer.

Figure B.4: AC voltage sensor PCB layout.

(a) Top layer.

(b) Bottom layer.

Figure B.5: Current sensor PCB layout.

Appendix C

Test setup

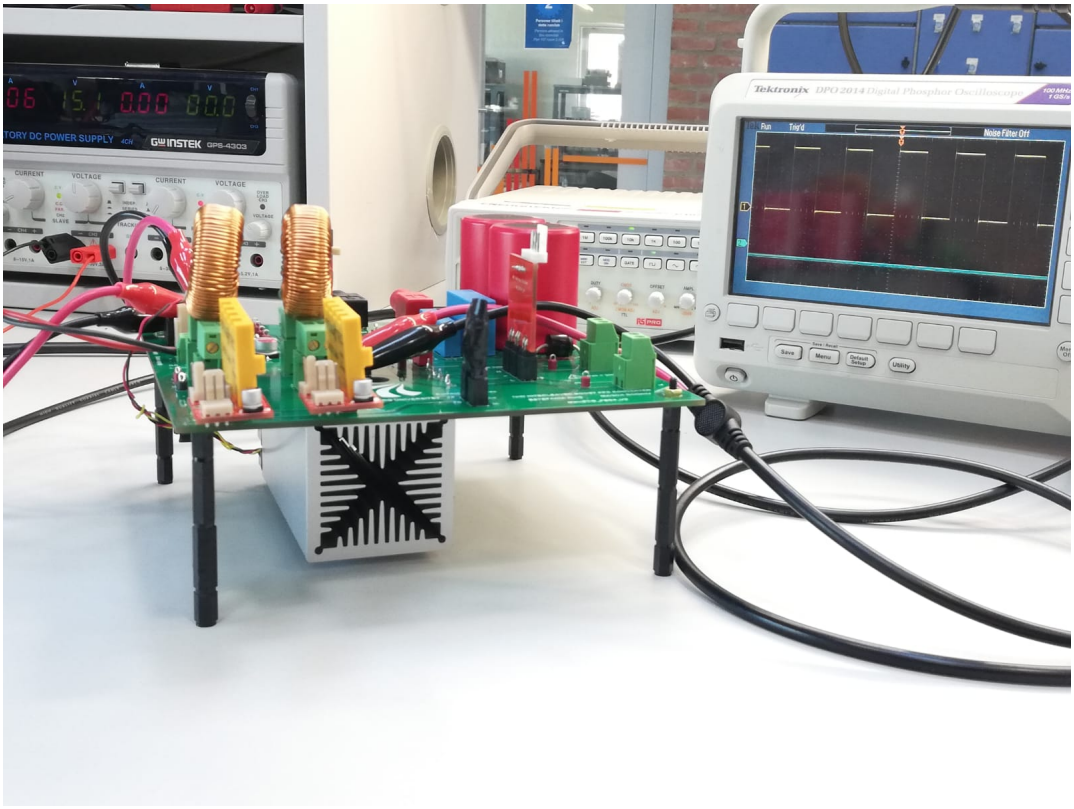


Figure C.1: Test setup for 1kW two-channel interleaved PFC converter

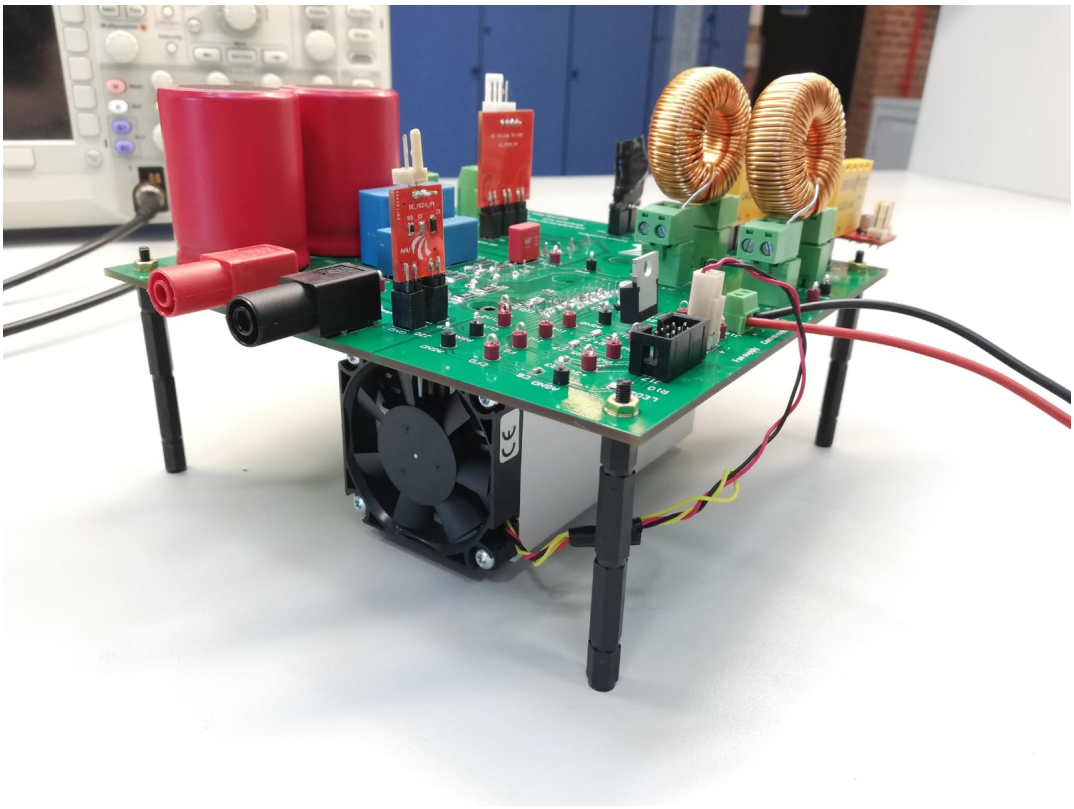
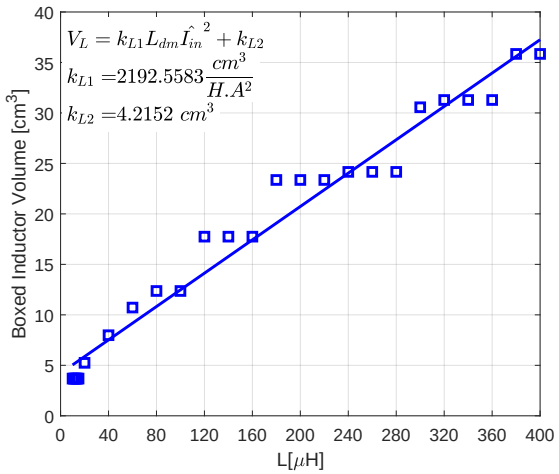


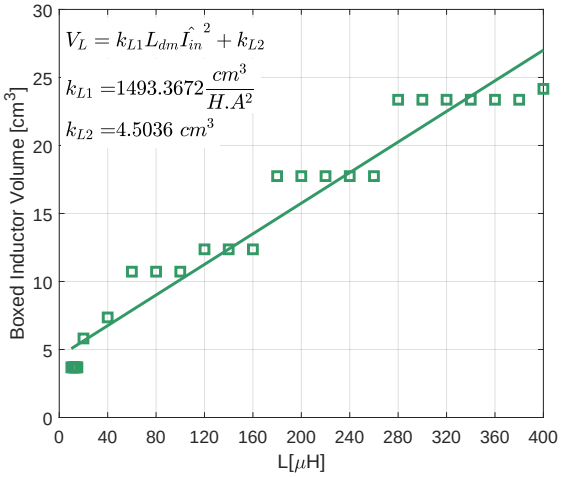
Figure C.2: 1kW two-channel interleaved PFC converter PCB side-view, with heat-sink and sensing PCBs (red)

Appendix D

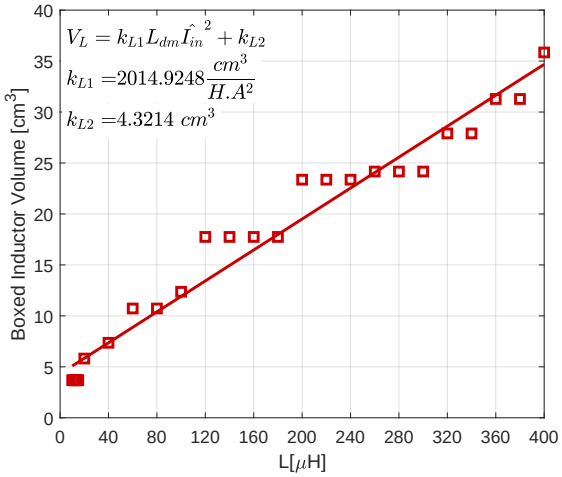
DM EMI inductor optimization



(a) KMU

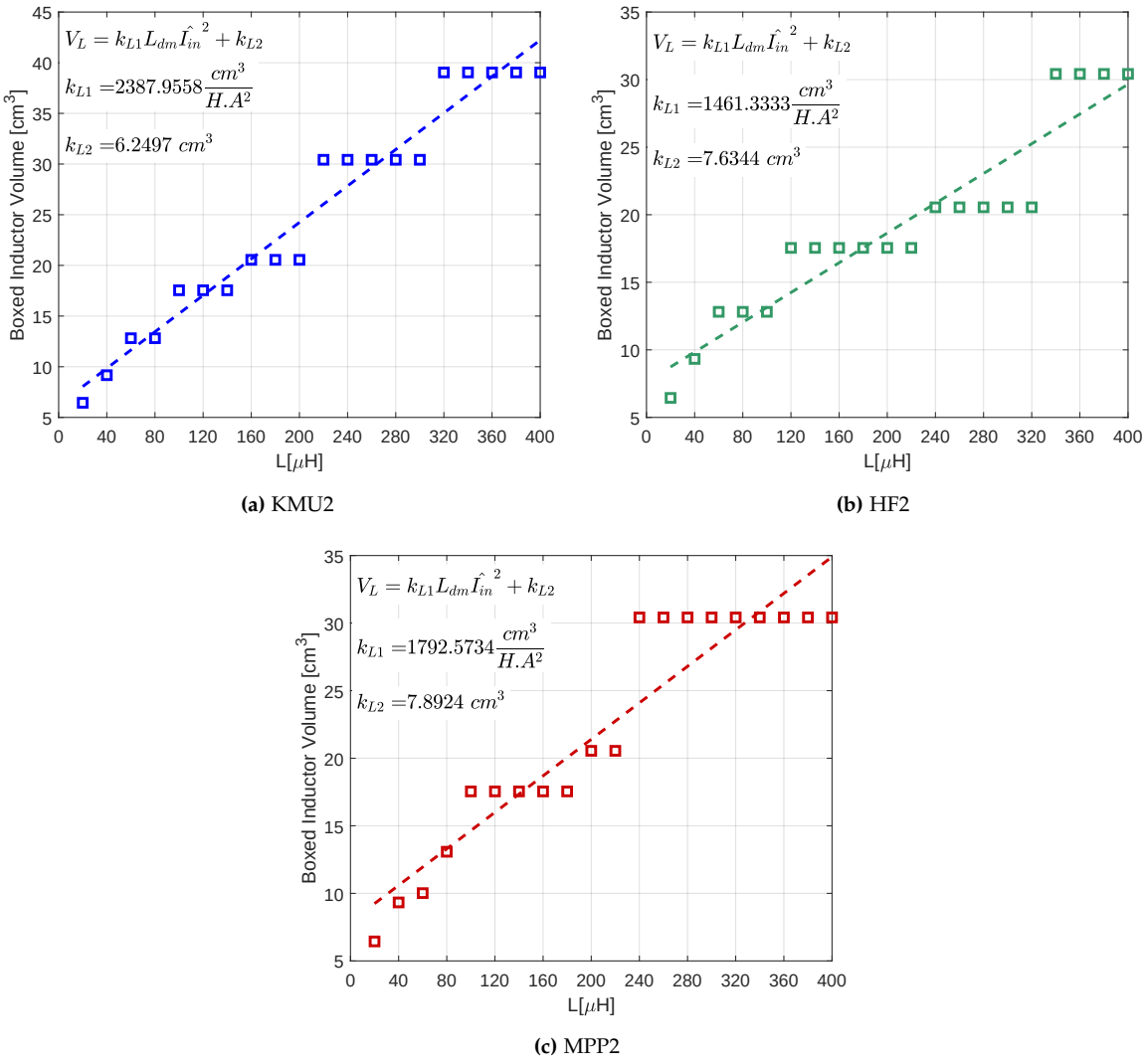


(b) HF



(c) MPP

Figure D.1: Inductor boxed-volume approximation for DM filter inductances using *Magnetics* toroid cores in dependence on the inductance value



(a) KMU2

(b) HF2

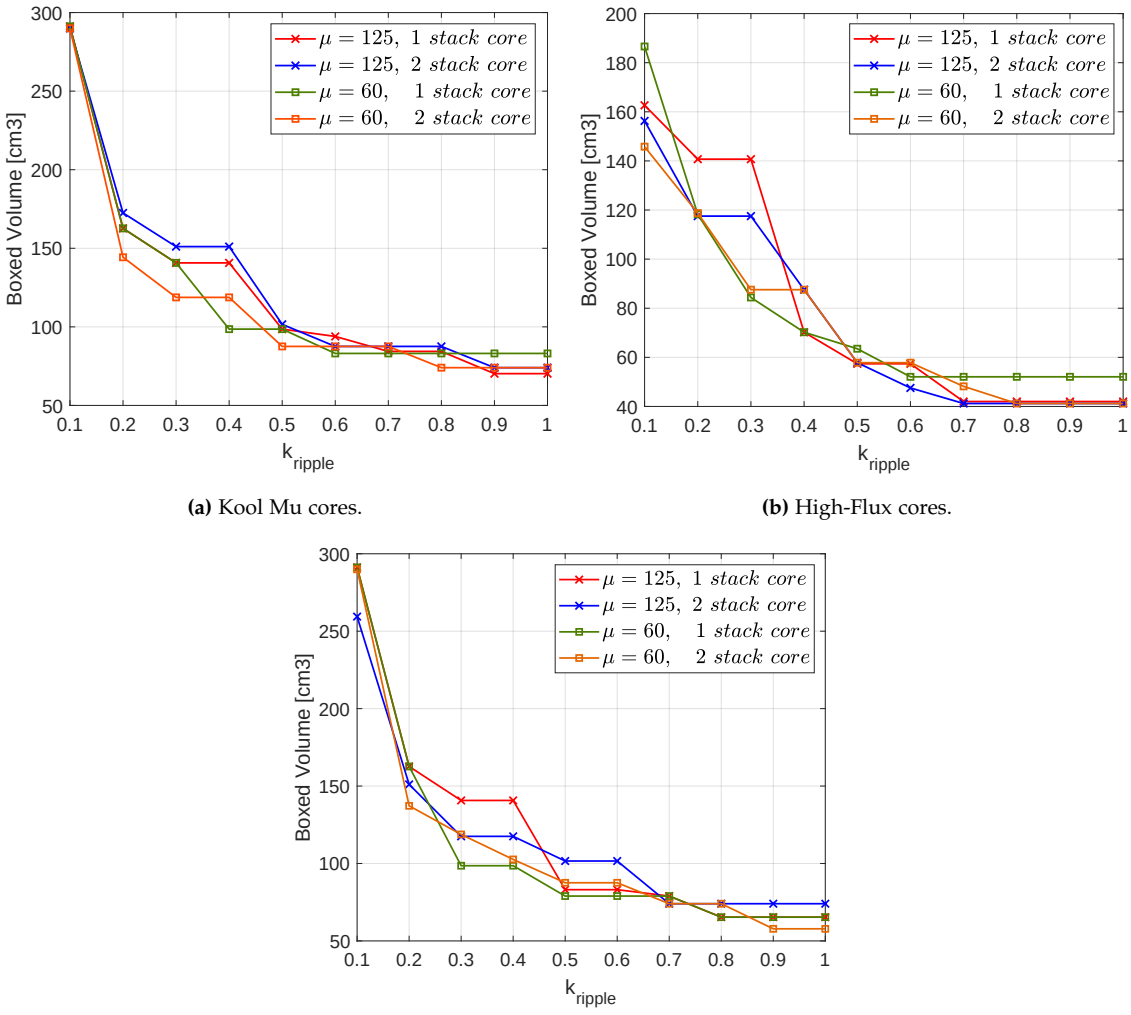
(c) MPP2

Figure D.2: Inductor boxed-volume approximation for DM filter inductances using *Magnetics* toroid two stacked cores in dependence on the inductance value

Appendix E

Boost inductor optimization

E.1 Non-interleaved PFC converter in CCM



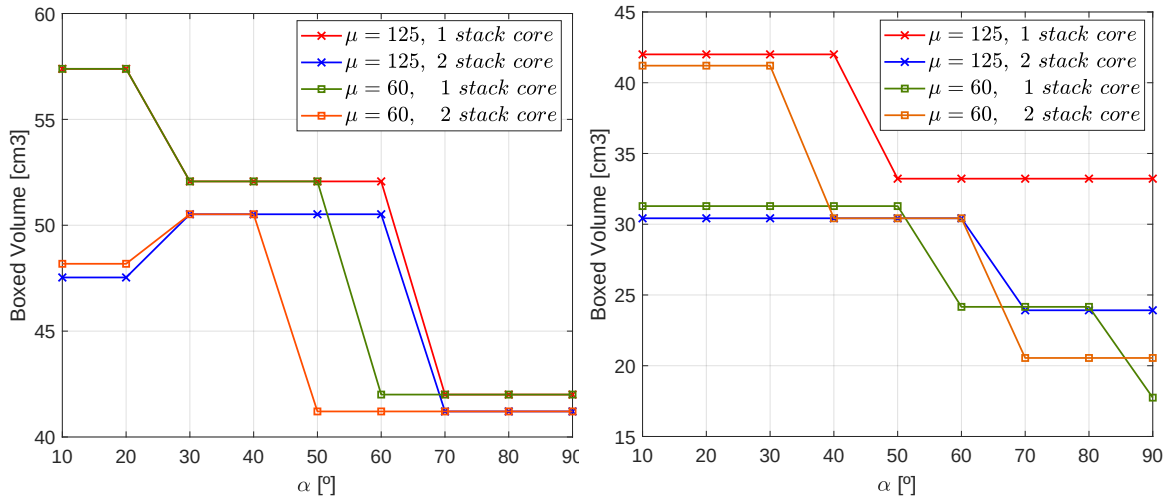
(a) Kool Mu cores.

(b) High-Flux cores.

(c) MPP cores.

Figure E.1: Non-interleaved PFC converter - Minimum boost inductor volume in CCM for three different core materials, permeabilities and number of stack cores, obtained from *Magnetics'* Powder Cores, varying k_{ripple}.

E.2 Non-interleaved PFC converter in QCM



(a) Kool Mu cores.

(b) High-Flux cores.

Figure E.2: Non-interleaved PFC converter - Minimum boost inductor volume in QCM for two different core materials, permeabilities and number of stack cores, obtained from *Magnetics'* Powder Cores, varying angle α.