Performance Evaluation of Medium Voltage DC-DC Converters based on 10kV SiC MOSFETS for Energy Storage Systems

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Master Thesis
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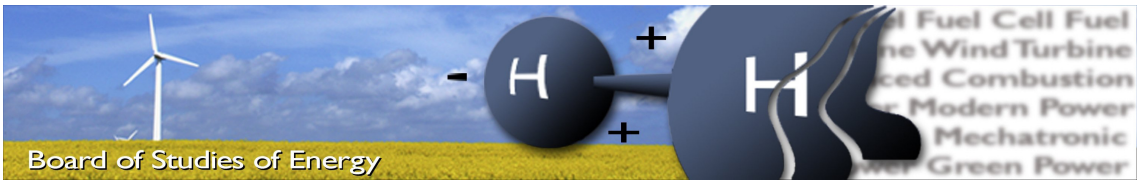

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SYNOPSIS: Nowadays, the electric energy which is generated by renewable energy sources, is mostly transmitted through AC grids. However, the development within the field of power electronics has raised the question whether the DC systems could replace the AC grids given the estimated higher efficiency. In application areas, such as wind parks, the collection of energy is made on a medium voltage AC grid and therefore, the heavy filters and transformers are present. In this project, it is investigated whether a medium voltage DC collector grid combined with medium voltage DC-DC converters can be part of a future DC grid structure, which could also reduce the size of the bulky elements. Here, two medium voltage DC-DC topologies, based on 10kV SiC MOSFETS, were examined for energy storage systems. Analytic models of the converters were developed and their operation was verified via simulations. Next, a comparison between the two converters, led to the selection of building one for further exploration.

Pages, total: 82
Appendix: A-B

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Summary

Nowadays, the electric energy which is generated by renewable energy sources, is mostly transmitted to the consumers through AC electric grids. However, the development within the field of power electronics has raised the question whether the DC systems and technology could replace the existing AC electric grids, as it is estimated that a more efficient transmission of the produced electric energy is feasible to be achieved. In some application areas, such as offshore wind farms, DC transmission has already been realized and additionally, high voltage DC levels are adopted for lower power losses. Nevertheless, the collection of energy, in the intermediate stage, is made on a medium voltage AC grid and therefore, the heavy filters and transformers are still present. Hence, in this project, it is investigated whether a medium voltage DC collector grid combined with medium voltage DC-DC converters can be part of a future conceivable DC grid structure, which could omit or reduce the size of the bulky elements. Here, two medium voltage DC-DC converter topologies, based on 10kV SiC MOSFETS power modules, which are the phase shift buck-derived and the single active bridge, are examined for energy storage applications.

In the beginning, the mathematical modeling of the two converters is developed through equivalent AC circuits, detailed equations and characteristic waveforms under continuous conduction mode. Moreover, the phase shift pulse width modulation scheme is implemented, for controlling the output power of the converters and for achieving soft-switching conditions, resulting to highly efficient converters. The conditions under which the soft-switching capability is lost, is also discussed.

Afterwards, the hardware design of the converters is explained in detail. The parts of the converters setup are analyzed and their design process is presented. Next, by obtaining the exact parameters from the aforementioned design procedure, the operation of the converters is verified through simulations in LTSpice. The simulation models contain a 6kV DC input voltage, a full-bridge inverter, a transformer which steps down the voltage at 800V, a rectifier bridge, a filter stage and a 50kW output load. A comparison between the two topologies, based on specific criteria, led to the selection of building the buck-derived converter in the laboratory for further exploration.

Finally, several experiments were conducted, which verified the shape of the waveforms that was predicted in theory as well as the proper design of the individual components. The experimental data was evaluated and it was compared to the simulated outcome, proving the consistency between experiments and simulations.

Keywords: medium voltage, DC-DC converter, phase shift pulse width modulation, single active bridge, phase shift buck-derived, soft-switching

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Finally, I would like to express my sincerest gratitude to my family members for the moral and economic support that they provided to me in order to complete my studies.

Preface

Reading Guide

It is recommended to the reader to start by reading the Appendix part. Each chapter is introduced and finished by a short paragraph. These paragraphs are introductions and partial conclusions for the given chapters. Lower case letters will denote the time varying quantities while upper case letters the average or constant values. There will appear source references through the report. These references will be collected in a source list at the end of the report. The reference method used in the report is the Harvard Method which means that the reference is placed in the text with following notation [Number which refer to Author etc.]. If the reference contains multiple sources, then each source is separated by comma. The references refer to the list of sources where books is stated with author, title, publisher, edition and year of publication while web pages is stated with author, web address, title and the point of time that indicates the last visit at the web page. Equations, tables and figures are numbered in accordance with the given chapter, i.e. Figure 1.2 is the second figure in chapter one. Explanatory text for figures and tables is located beneath the given tables and figures.

Nomenclature

AAU	Aalborg University
AC	Alternating Current
BMS	Battery Management System
D	Duty Cycle
DC	Direct Current
DSP	Digital Signal Processor
ESR	Equivalent Series Resistance
ESS	Energy Storage Systems
EV	Electric Vehicle
GaN	Gallium Nitride
HVDC	High Voltage Direct Current
LiC	Lithium-ion Capacitor
LV	Low Voltage
MFT	Medium Frequency Transformer
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
MV	Medium Voltage
MVAC	Medium Voltage Alternating Current
MVDC	Medium Voltage Direct Current
PCB	Printed Circuit Board
PV	Photovoltaic
RES	Renewable Energy Sources
RMS	Root Mean Square
SiC	Silicon Carbide
UPS	Uninterrupted Power Supply
WBG	Wide Band-Gap
ZVS	Zero Voltage Switching

Δi	Current ripple	[A]
ϕ	Phase Shift Angle	[°]
C	Capacitance	[F]
f_s	Switching frequency	[Hz]
I	Current	[A]
L	Inductance	[H]
P	Power	[W]
R	Resistance	[Ω]
t	Time	[s]
T_s	Switching period	[s]
V	Voltage	[V]

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Introduction 1

In this chapter the motivation around DC systems is introduced and the potential need for medium voltage (MV) and high power converters is explained. The focus will be on MV DC-DC converters and some potential application cases of these converters will be presented and discussed. Finally, some challenges that occur on DC systems will be stated.

1.1 Motivation for DC technology

Nowadays, there is an increasing demand for carbon dioxide emission reduction in order to balance the greenhouse effect. By burning fossil fuels like coal and oil for the electric energy production, the carbon dioxide levels rise, having a negative impact on the greenhouse effect. The renewable energy sources (RES), such as photovoltaic and wind parks, offer an alternative and more eco-friendly technology compared to fossil fuels and many countries choose that direction for the electric energy generation. For instance, Denmark moves to strenghten the renewable energy goals, introducing a new energy policy which requires at least 50% of the energy demands, to come from RES by 2030 [23]. Consequently, higher penetration of renewables has been observed the last decades.

But these RES are widely spread through the electrical distribution network and since they are placed far away from the city centres, the transmission of the generated electric energy becomes essential. Today, AC is mainly used for this transmission. Also, the engineers soon realised that the transformation to higher voltage levels is important to efficiently transmit electric energy over long distances and that is how most of the RES are connected to the grid today [43]. However, the advances on the power electronics field, allow the efficient voltage conversion to DC as well, raising the question whether DC systems and technology could replace AC in some applications.

The AC systems are widely used today, as they are more reliable, they are well-studied through the decades and the 50/60Hz transformers have a very high efficiency. However, traditional AC presents main drawbacks like the reactive power demand, as well as skin and proximity effects in the cables, which reduce the overall efficiency of such a grid. For example, the reactive currents, which come from the reactive impedance of the lines or cables, generate significant amount of losses, especially if the transmission line/cable is long enough. Long cables do exist in an offshore to onshore connection in the wind farm applications today. On the other hand, in DC systems, the converters allow active power flow control and the reactive power demand along with the skin and proximity effects are not present rendering DC grids advantageous in some cases [44].

Finally, there are numerous applications in which DC connection is already implemented. On a low voltage level ($\leq$ 1.5kV) , DC is promoted for data and telecommunication centers as servers and IT equipment behave as DC loads [43], whereas the connection via long cables of an offshore wind farm to onshore, can be made on a high voltage DC (HVDC) level ($\geq$ 100kV) [4]. Therefore, one can assume that MV level/high power applications can benefit similarly from DC and many researchers work intensively towards that direction [43], [45]. The focus on this master thesis will be on the MV DC-DC converters and their significance will be better understood through the next section, where the potential implementation area of such converters will be covered.

1.2 Medium Voltage DC-DC Converters Application Areas

MV DC-DC Converters could be applied in various application cases. Some of them are introduced in the following. The focus will be on the applications that are presented in Figure 1.1. So, according to the figure, these converters could be part of three big categories, namely the renewable energy systems, fields of industry and transportation.

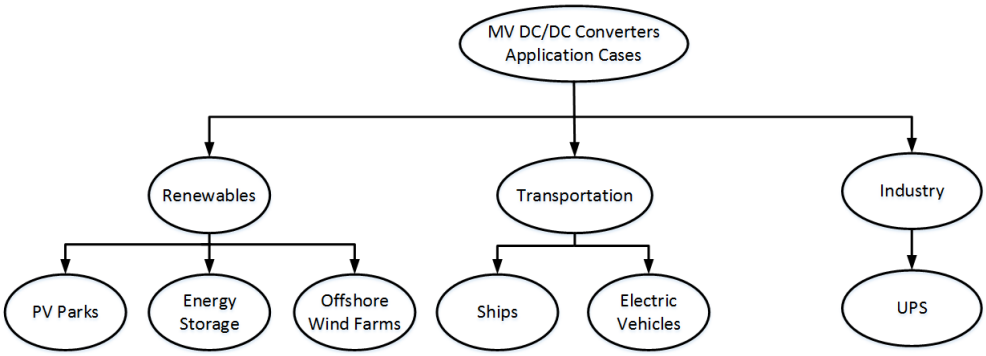

Figure 1.1. Medium voltage DC/DC converters application cases

1.2.1 Offshore Wind farms

Nowadays, there is a trend to implement HVDC transmission with long distance submarine cable of more 200km length, to connect the offshore with the land [27]. Nevertheless, MVAC collection grid is used instead of DC in the intermediate stage of the energy delivery. The power capacity of the offshore-wind electricity generation increases. In fact, it will exceed the 10MW power rating in a few years [10]. This rise of the power ratings, leads to higher currents in the MVAC collection grid and longer distances between the wind turbines resulting to high power losses on the cables [10]. Additionally, MVAC and HVAC long cable connections are prone to cause resonances due to the cable capacitance. This affects the stability of the control system of the power electronics [22]. Consequently, as HVDC transmission is adopted, there is an initiative to replace the MVAC collection grid with a MVDC collection grid and all these problems could be overcome [35].

A typical schematic of the existing AC offshore collector grid is shown in Figure 1.2 [43]. Only one wind turbine in the line diagram is shown for simplicity. The wind energy transmission to the shore is done via a transformer and a rectifier. Since the wind turbines operate at a variable frequency, a converter stage is needed for connecting the wind turbines to the MVAC grid. Another major problem of this configuration is, as the MVAC grid

operates at 50/60 Hz, the filter stage after the DC-AC converter and the transformers are quite heavy occupying a lot of space which is not desired.

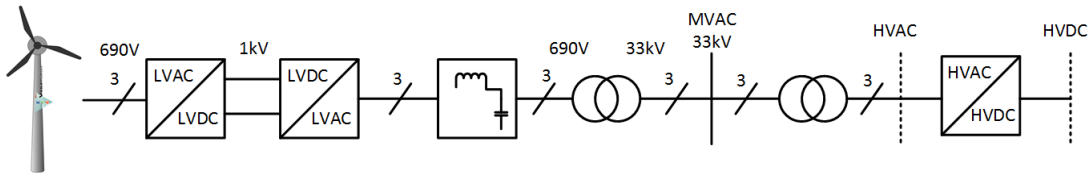

Figure 1.2. Typical AC offshore collector grid

In some offshore wind connections, the HVDC connection scheme as illustrated in Figure 1.2, has been already implemented. In the project *BorWin1*, one of the most remote offshore wind farm clusters in the world is connected to the German grid by a ±150 kV HVDC system, while in the project *DolWin2*, the wind farms are connected with AC cables to a HVDC converter station installed on an offshore platform in the North Sea [4].

However, another approach for connecting the offshore wind farm to the HVDC collection grid is stated in [27], where a MVDC collector grid is used instead of an AC. As a result, the inverter and the filter stages can be removed. The transformers are incorporated into the DC-DC converters and as they operate under a higher frequency, their volume drops significantly. In Figure 1.3, a possible topology for offshore wind farms is illustrated.

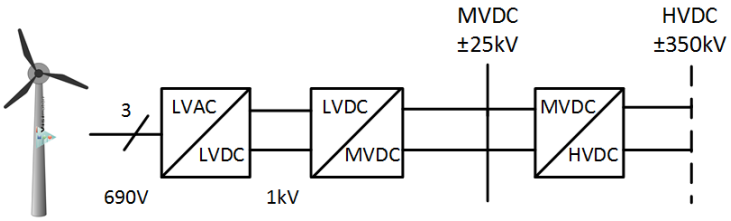

Figure 1.3. Possible DC offshore collector grid

1.2.2 Photovoltaic Parks

Today, the output of a PV plant is a low DC voltage, no more than 1kV, and it is connected to a medium voltage distribution network of around 20kV through an inverter and a transformer, as shown in Figure 1.4 [45].

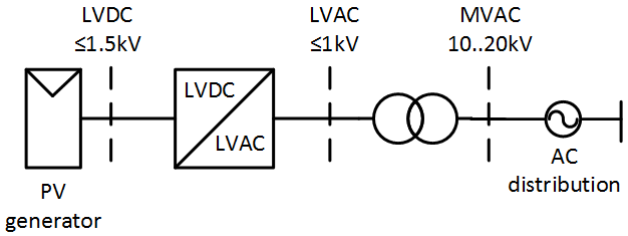

Figure 1.4. Conventional PV plant topology

In general, a PV park consists of a large number of PV generators, so it is desired to increase the power of each sub-unit in order to decrease the system costs [45]. But raising

the power without changing the existing low voltage level it leads to higher currents. As a result, the thermal losses rise and higher copper diameter for the cables has to be realized.

It is expected that the output power of a PV module will grow in the future and therefore, the voltage level of the system could be raised too [45]. This fact, will reduce the transmission losses [44]. For instance, a conceivable future PV plant topology is depicted in Figure 1.5 [45]. As it is clearly observed, a MVDC collection grid is present. Due to the MVDC grid the cable diameters can be small and the transformer size is reduced, ending up with a reduced overall cost according to the authors of the article [45].

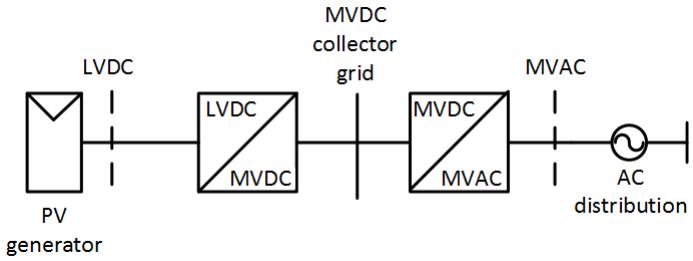

Figure 1.5. Future PV plant topology

1.2.3 Energy Storage Systems in Photovoltaic and Wind Applications

Many power applications require an intermediate energy storage system. Nowadays, energy storage systems are quite attractive, as the penetration of renewable energy sources, such as photovoltaics and wind turbines, constantly rises. As a result, this surplus of energy, can be stored in ESS [25]. Previously, the implementation of the MV DC/DC converters was discussed in a MVDC grid context. Hence, if wind turbine and photovoltaic parks will be connected to a MVDC collection grid, an interface is required from the low voltage level of any energy storage element ($\leq$ 1kV) to MV level. It is easy now, to make a step forward in our thoughts and imagine a MVDC converter that it is connected to the MVDC grid and will allow the storage of the extra energy, in an energy storage element. This element could be a battery or an ultracapacitor. In addition, the MV DC/DC converter can be considered bidirectional, namely the power flow is allowed in both directions, and this extra energy could be fed back into the grid to support it in case of power demand (grid forming conditions).

1.2.4 Electric Vehicles Batteries Chargers and UPS Systems

The charging of the EV batteries from the 50Hz supply grid is discussed in many research papers. An appropriate configuration is illustrated in Figure 1.6 [24]. The EV is plugged into the utility grid and it is charged. The bi-directional DC/DC converter provides galvanic isolation and adjusts the voltage level. The electric vehicles chargers are limited to a power level of 3.4kW, due to the 16A current limitations in domestic applications [26]. Consequently, the charging time of the batteries lies in the range of 5 to 6 hours. Also, there is a limitation in serial connection between batteries, and consequently the voltage can not be further increased with the existing battery technology ($\leq$ 600V on today's EVs). In addition, the BMS would become more complex.

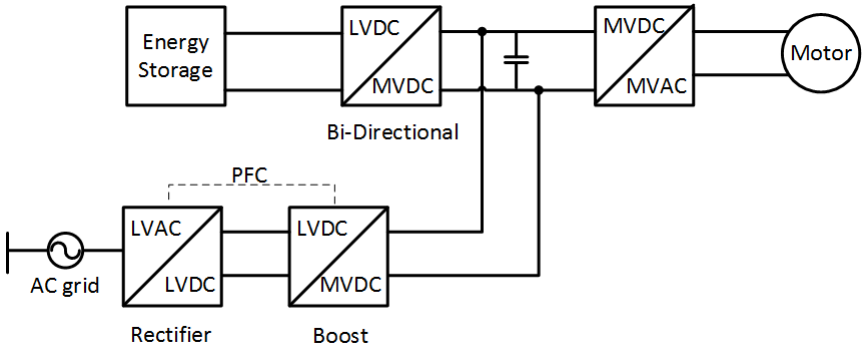

Figure 1.6. Plug-in electric vehicle configuration

To overcome this disadvantage, high power/MV converters are proposed to charge the energy storage element in much shorter time at an autonomous station [26]. For instance, in [24], a 20kW bi-directional DC-DC converter is realized, for an input voltage of 300V and an output voltage of 800V. Hence, by establishing a MV DC-DC converter all the above restrictions may vanish.

A similar kind of application where energy storage is useful is at the uninterrupted power supplies (UPS). A UPS system would be connected to the HVDC or MVDC bus as it is shown in Figure 1.7 [32] where the isolated bi-directional converter would regulate the voltage on the storage element. In [38] a low power application of 2.5kW for a UPS system was investigated and a bi-directional DC/DC converter was proposed.

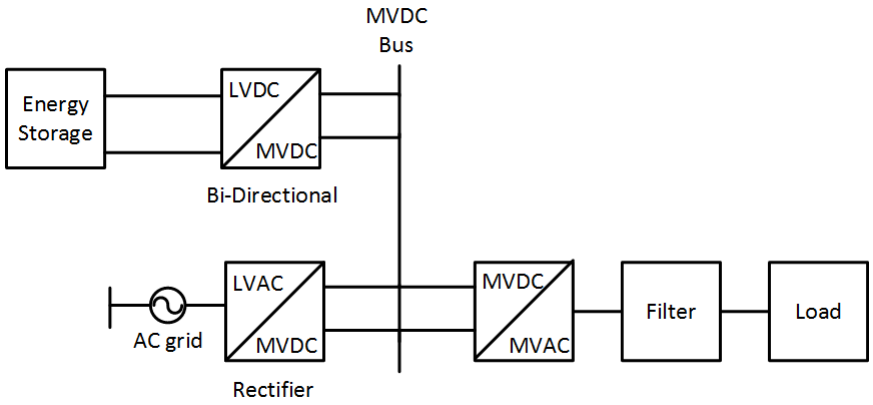

Figure 1.7. Isolated bi-directional DC/DC converter in UPS system

1.2.5 Marine Industry

A special application of the MV converters is the field of ship grids where DC-distribution grid is proposed. Today, MVAC grids are used on the ship but already, a low and medium voltage DC-distribution has been investigated [2],[3] and a possible on-board DC grid is illustrated in Figure 1.8. By using DC-distribution it is no longer required to maintain a fixed electric frequency for the engines of the ship and as a result, they can rotate at a variable speed. Consequently, the best operating point could be achieved for maximum fuel efficiency [3]. Finally, on a DC grid context, the transformers can be omitted. Transformers typically weigh 4500 kgs or more and they occupy more than $5m^3$ of ship space [6] factors

that are very crucial as the space and the weight of a ship are limited. In [6], a MVDC grid is realized and the transformers were completely excluded.

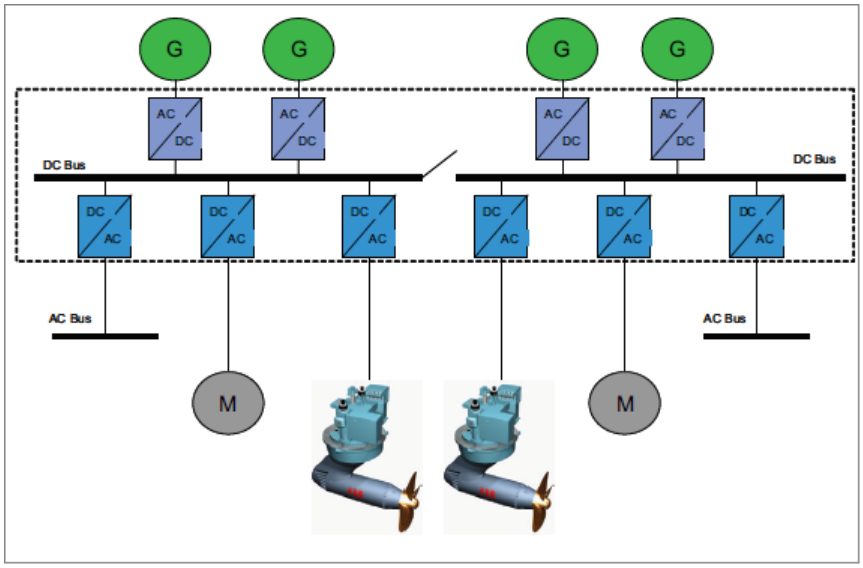

Figure 1.8. On-board DC grid [2]

1.3 DC Grids and Medium Voltage Converters Challenges

Although the DC grids seem promising over the existing AC, they present some significant challenges which will be, briefly, introduced here.

An important issue that needs to be addressed on the MVDC grids and on the DC grids in general, is the protective system of such systems. It is well-known that AC currents are by nature far simpler to break due to their natural zero-crossing every half cycle. Although DC circuit breakers do exist to some extent, they are more complex, larger and more expensive than the AC circuit breakers. Several efforts have been put by researchers in order to overcome these difficulties and topologies for current breaking on DC systems have been already proposed [9], [37]. However, the challenge of the current breaking on the MVDC or HVDC applications is still active. Additionally, technical challenges such as the DC grids stability issues and reliability or business challenges due to the fact that the DC grids are an unthreaded territory, are still present.

Finally, the reason why there is an open discussion for MV converters and their potential advantages, is the development on the semiconductor materials which offered the possibility for MV blocking devices (SiC). Nevertheless, these materials are still new, expensive and not well explored in terms of reliability. More challenges on MV converters, and especially on MV DC-DC converters, will be described in Chapter 2.

1.4 Conclusion

In this chapter, the motivation for a DC technology was presented and, more specific, towards the MVDC concept. The advantages of the MVDC over MVAC for some of the applications mentioned previously, are summarised in Table 1.1. Finally, the most

important challenges of the DC grids that need to be solved were, briefly, stated. In Chapter 2, the focus will be on the MV DC-DC converters, which are key components in a MVDC grid context, and the state of the art technology that led to MV DC-DC converters will be explored.

	Existing AC/MVAC grids problems	Future DC/MVDC grid solution
Offshore Wind Farms	• Power electronics control systems instabilities due to cable resonance • Heavy filters and transformers • Significant amount of losses due to reactive currents on the long cables	• No resonance problems in DC • Omission of the filters and inverter stages/reduced size transformers • No reactive currents
PV Parks	• Transformers present • Due to the desired power increase of a PV plant, high currents (big thermal losses and large copper diameter for the cables) occur if the voltage level remains unchanged • PV plants power rise does not allow the increase of the power of the transformers at the existing high transformer ratios as physical limits will be reached [45]	• Reduced size transformers • The voltage level increases and cables diameter can be small • No such a problem here
Ships Grids	• Large transformers weigh a lot and occupy space • Fixed electric frequency of the engines	• Transformers absent or reduced in size • Variable speed of the engines on a DC grid context which leads to less fuel consumption

Table 1.1. DC/MVDC grid solutions on some application areas

State of the Art 2

In this chapter the state of the art technology that helps towards the development of the high power MV DC-DC converters is presented. The technological improvements on the key components of a MV DC-DC converter are discussed and the various topologies that have been studied in literature are shown. In addition, challenges and limitations of today's existing technology for developing MV converters are stated.

2.1 Wide Band Gap Devices

Nowadays, most of the semiconductors are based on silicon (Si), but over the last years, the increasing demand for semiconductors with a higher performance, has matured the silicon technology and new types of semiconductors have been created based on silicon carbide (SiC) and Gallium Nitride (GaN). These materials are well-known as wide band-gap (WBG). In many applications, the WBG materials are preferable over conventional Si [8], [33], [28] given that they have some significant advantages [36], [1]. In this thesis, SiC MOSFETS will be used for the development of the MV DC-DC converters, so it is reasonable to state here some of the main advantages/identities of the SiC material and SiC MOSFETS in general:

- **Higher energy bandgap than Si:** This identity leads to smaller intrinsic leakage currents than that of a silicon and this allows the operation of the semiconductors on higher temperatures than the usual ones ($T_{max} \approx 150^oC$ for the Si). This is an important characteristic as the cooling system of the WBG becomes much smaller in size and weight.

- **Improved reverse recovery characteristics for SiC MOSFETS:** In SiC MOSFETS, the reverse recovery current becomes smaller compared to Si MOSFETS. Therefore, the switching losses as well as the electromagnetic interference (EMI) are diminished.

- **SiC Higher Electric Breakdown Field than Si:** The electric breakdown field defines the amount of electric field that the semiconductor can withstand before breakdown. This quantity is approximately eight to ten times larger for the SiC than Si . Due to this fact, the WBG devices can block much higher voltages given that the breakdown voltage is proportional to the square of the electric breakdown field. The high blocking voltage is the main identity which renders the SiC-based semiconductor devices suitable for the design of MV converters. Today's SiC technology devices can withstand over 10kV. Additionally, these devices occupy less volume as the volume depends on the critical electric field.

- **Lower conduction resistance for SiC MOSFETS:** Moreover, the WBG devices present lower drain to source resistance. This is due to the fact that for the same blocking voltage, approximately 100 times more doping can be made in SiC compared to Si. Higher doping means higher conductivity and therefore less resistance. As a result, the conduction losses are decreased in SiC devices.

However, the material process of SiC is more complex, the cost is still high and the reliability of the SiC devices is still under investigation and these are some of the important factors that do not allow the wide use of SiC devices.

2.2 Medium Voltage DC-DC Converters Topologies

In the literature, different converter topologies have been investigated. These converters, can be separated into two big categories, isolated and non-isolated according to galvanic isolation condition.

2.2.1 Non-Isolated DC-DC Converters

One obvious direction for constructing MV DC/DC converters, is to use the well-known topologies like the synchronous boost converter which is shown in Figure 2.1. The traditional Si-based switches could be replaced by SiC semiconductors. In [45], this circuit was studied and constructed for a 28kW power rating, an input voltage of 3.5kV and an output voltage of 8.5kV showing up an efficiency of 98.5%. Also, SiC MOSFETS were used with 10kV blocking voltage and 10A drain current which is the technology that exists nowadays. A disadvantage of this circuit is that it can not produce a big voltage ratio between input and output, given that for a large duty cycle the efficiency of the boost circuit is reduced significantly [39]. In [14], two boost converters were placed in a cascaded arrangement in order to step-up the input voltage. The input voltage is the wind turbine output which is rectified. The specific topology was evaluated for an HVDC transmission application.

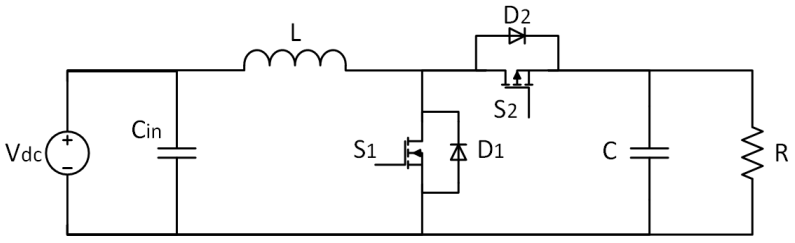

Figure 2.1. Synchronous boost converter

In [14], a hybrid topology has been examined, which consists of a boost and a buck/boost in series and it is presented in Figure 2.2.

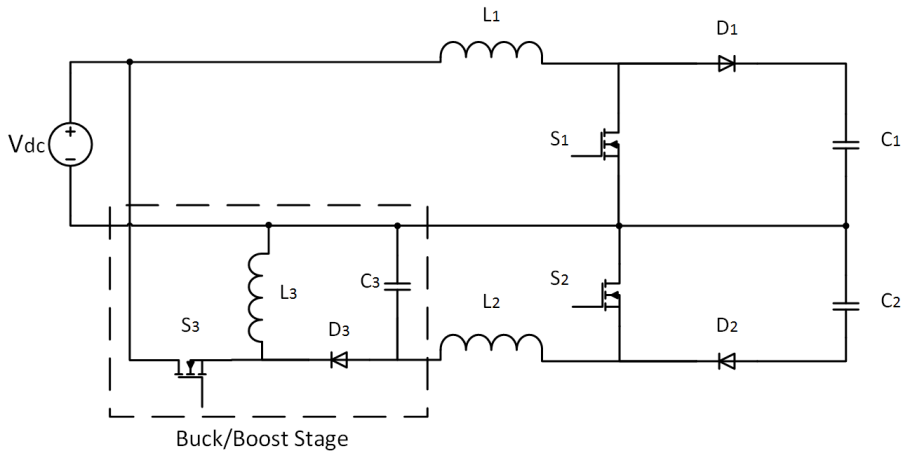

Figure 2.2. Hybrid boost and buck-boost converter

This arrangement aims to achieves high step-up conversion ratio without using a transformer. The circuit is compared to other suggested topologies for HVDC transmission in an offshore wind farm application. The authors end up that this topology would be suitable for high-power/high-gain offshore wind applications, especially when SiC devices would be broadly available, as the diodes reverse recovery losses will be diminished. However, many simplifications were made which affect the efficiency of this circuit in reality. Some of them are, the neglect of the switching losses and snubbers whereas all devices were considered ideal. In fact, the losses of this circuit would be slightly higher in a possible MVDC grid compared to today's AC grid although the use of this converter and the DC grid would reduce the magnetic components and the weight of the cables [44].

In [30], a resonant step-up converter is proposed for high power application which is illustrated in Fig 2.3. This is a current source converter.

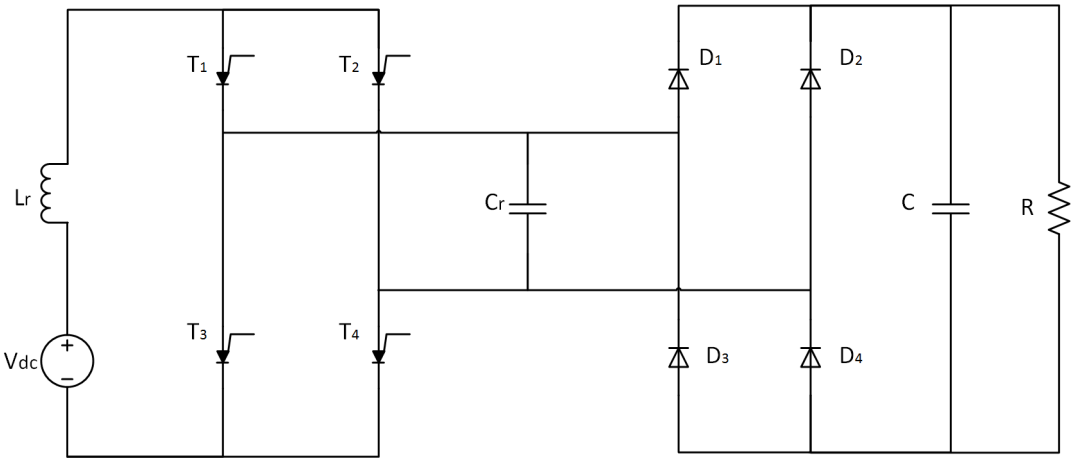

Figure 2.3. Resonant (RS) boost converter

It has been demonstrated that this converter can achieve very high step-up gains within a megawatt range test system [30]. One of the advantages of this circuit is that it offers soft switching for all switches and diodes, reducing the total losses. The voltage of the capacitor C_r is positive when T_1 and T_4 are on and negative when T_3 and T_2 are activated.

Also, all switches should have reverse blocking capability, but turn-off capability is not required [30]. Hence, thyristors can be used. A bi-directional version of this circuit is also proposed in [30].

Another transformerless approach can be found on [11] and again it is about a resonant step-up converter for offshore wind energy systems which is depicted in Figure 2.4. This converter can achieve soft switching for all the diodes and switches and low-voltage-rated active switches can be adopted. This arrangement works as an $m + 1$ times step-up converter where m is the number of positive modular cells respectively. In Figure 2.4 a voltage rise of three times the input voltage is feasible given that there are two positive modular cells. The basic modular cell consists of two diodes a filter capacitor, a resonant capacitor and a resonant inductor (red dashed line rectangular). The MOSFETS are controlled complementary with 0.5 duty cycle.

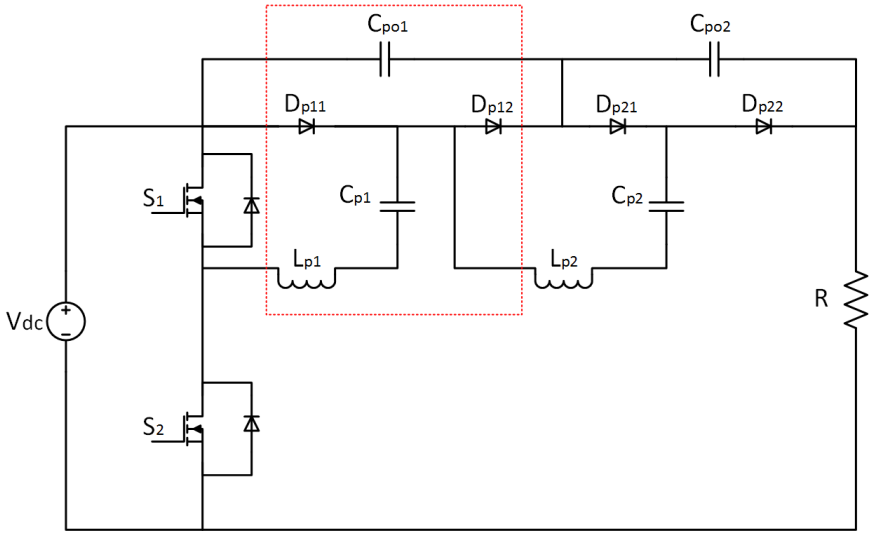

Figure 2.4. Resonant switched-capacitor (RSC) boost converter

The circuit works as follows: Before S_2 turns on, the currents through the inductors L_{p1}, L_{p2} reach zero value. During $[t_0, t_1]$ time interval (see Figure 2.5), the current through S_2 increases and therefore the device can turn on under zero current conditions. It is clearly observed that there are two resonant loops. One consists of $V_{DC}, D_{p11}, C_{p1}, L_{p1}, S_2$ and the other one is composed by $V_{DC}, C_{po1}, D_{p21}, C_{p2}, L_{p2}, C_{p1}, L_{p1}, S_2$. The resonance frequency is the same for the two loops given that $L_{p1} = L_{p2}$ and $C_{p1} = C_{p2}$. At t_1 the currents through L_{p1}, L_{p2} decrease to zero after half resonant period and the currents through S_2, D_{p11}, D_{p21} also fall to zero resulting to a turn off under zero current for S_2. By observing Figure 2.5, similar statements can be made for the interval $[t_1, t_2]$ where transistor S_1 is on. At the end of the half switching period, all the currents of the resonant inductors reach zero amperes when the switching frequency is equal to the resonance frequency and as a result soft switching is achieved. All the filter capacitors (C_{po1}, C_{po2}) and the input voltage source power the load.

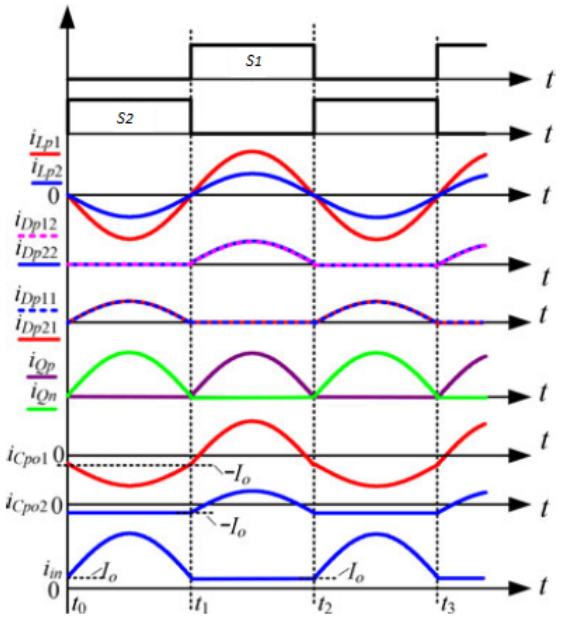

Figure 2.5. Idealised waveforms of the RSC boost converter [11]

This topology can be expanded to have also n negative modular cells for an increased output voltage as it shown in Figure 2.6. The output voltage will be $m + n + 1$ times the input voltage. In [11], an 8 to 40kV converter was built. According to the authors of this article, by using this topology the switching losses are dropped significantly, the switching frequency can be increased and the overall volume of the system is less than the respective volume that the hybrid boost and buck-boost or RS converter presents [44].

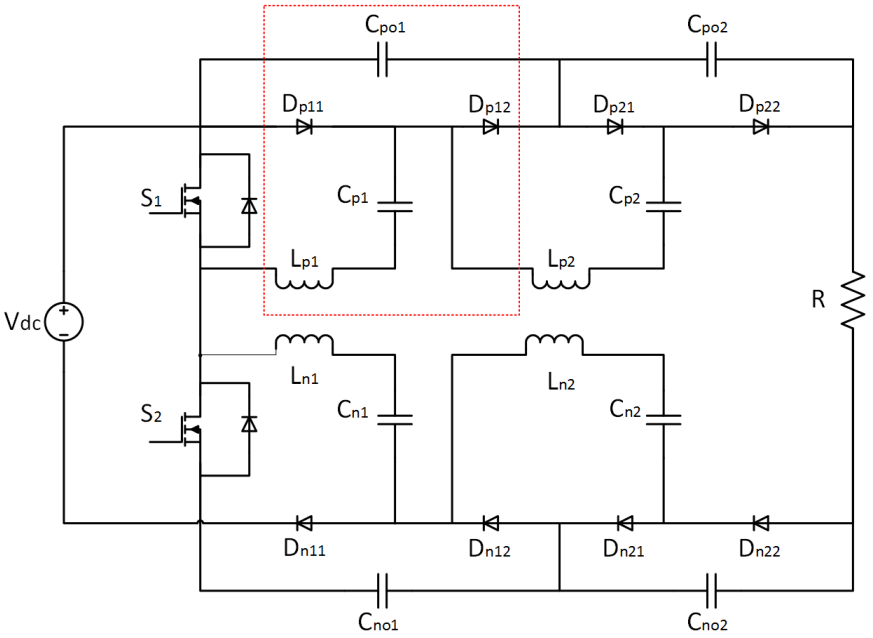

Figure 2.6. RSC boost converter with two positive and two negative modular cells

2.2.2 Isolated DC-DC Converters

Some of the main drawbacks of the aforementioned topologies are the limited operating duty cycle range as well as the complexity because, in order to obtain large voltage ratios, one should add more components like on the RSC converter (Figure 2.3). To handle these disadvantages, other circuit arrangements have been already suggested in literature and these are the isolated DC-DC converters. This type of converters, contains a medium frequency transformer for achieving even higher voltage ratios and galvanic isolation.

An example of these topologies is the LLC resonant converter which is shown in Figure 2.7 and it is studied in [18] for stepping down a 6.5kV input voltage to 3.3kV output voltage. The inductors L_σ and L_m are the transformer leakage and magnetizing inductances respectively. A capacitor C_r is placed in series with the transformer to create resonance conditions. The advantages of this circuit are: wide output voltage regulation range, reduction of switching losses on the primary side in a wide load range through zero voltage switching and zero current switching on the secondary diode rectifier [18]. This circuit was evaluated in high power applications using IGBTs in [18] and [17] and it was considered suitable for these applications due to the previously mentioned advantages.

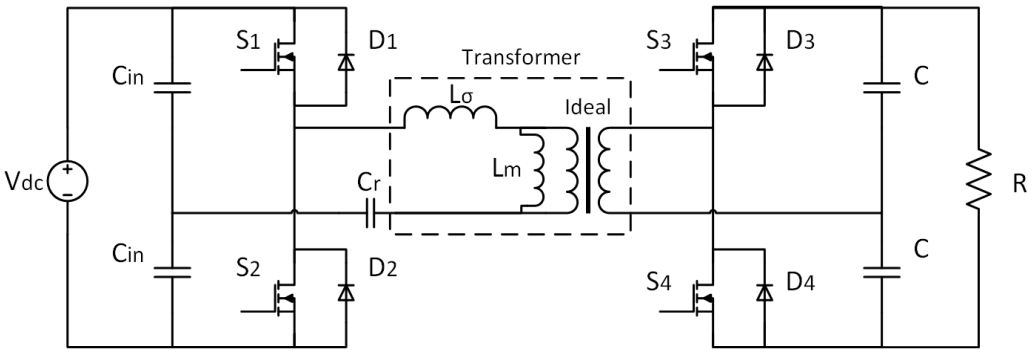

Figure 2.7. LLC resonant converter

Another well-known topology which is proposed in [15], is the dual-active bridge (DAB) converter in Figure 2.8.

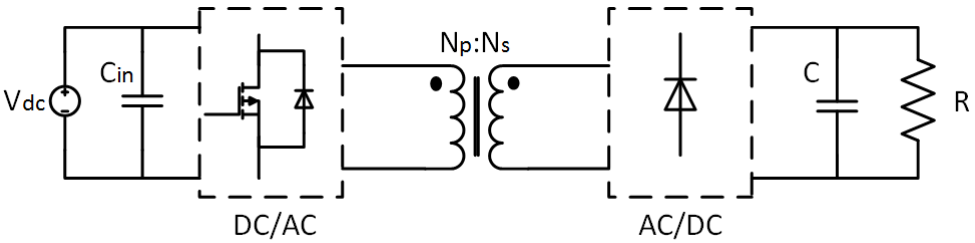

Figure 2.8. DAB converter

The DC-AC and AC-DC converters can be one-phase or three phase. The three phase topology offers some advantages over the single phase such as reduced filter RMS currents and possible redundant operation by the two additional phase legs [15]. This converter can be easily adjusted to be uni-directional, using diodes or bi-directional, using transistors

depending on the application case. The transformer is non-ideal and its leakage inductance is in fact the power transfer element. In recent years, the DAB seems a very promising converter for medium voltage and high power applications, as the advances in new power device (SiC, GaN) and magnetic core materials (e.g nanocrystalline) lead to a more efficient topology [47].

A step-down uni-directional version of the DAB will be examined in this thesis which is usually called Single Active Bridge (SAB). Moreover, in order to avoid the use of a high capacitance value output capacitor on the SAB, a DC inductor can be placed in the output, creating a second order filter. This buck-derived topology, will also be discussed and compared to the SAB.

A final topology that will be presented, is shown in Figure 2.9 and it consists of a half-bridge DC/AC converter along with a neutral-point clamped (NPC). This circuit is investigated in [44]. To increase the output voltage of such a converter many cells are placed in series/parallel configuration, where the power flow and the output voltage are shared between the different levels [44].

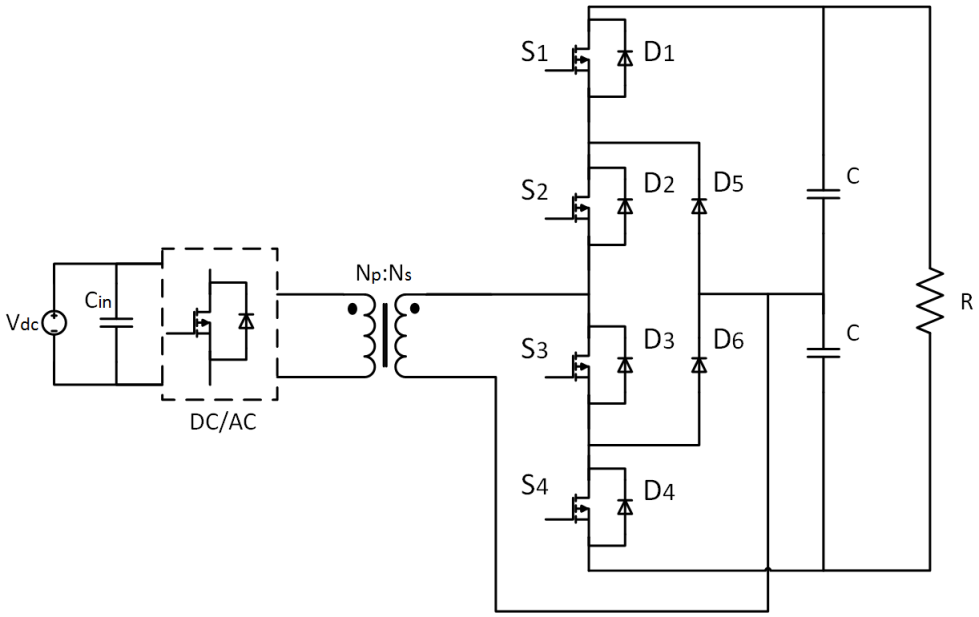

Figure 2.9. DAB converter with half-bridge and NPC

2.3 Medium Frequency Transformers

One of the key components of the isolated high power DC-DC converters is the medium frequency transformer (MFT) which offers galvanic isolation and step up/down of the different voltage levels. The weight and physical dimensions of an MFT are critical factors for the design of the isolated DC/DC converters. It is also well-known, that the size of a MFT decreases as the operating frequency increases and this reduction implies higher power density through the transformer windings and different design requirements compared to those that are used to the conventional 50Hz transformers [41]. In Figure 2.10, a photo is illustrated, to clearly show the effects of the increased operating frequency on the size of a transformer.

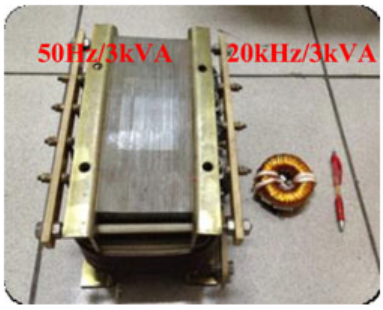

Figure 2.10. Comparative photo of 50Hz and 20kHz transformers [47]

Although the MFT have many opportunities, their weak point is their design procedures and that is why they are not applied in today's medium voltage grids. Consequently, a lot of effort has been put in order to optimize the design of such a transformer which presents some challenges due to their higher operating frequency.

First of all, different materials for the transformer core have been investigated, such as silicon steel, ferrites, amorphous materials and nanocrystalline [41],[16]. The latter material presents some interesting identities compared to the other ones, such as fairly high density of magnetic flow, low losses at medium frequencies (around 5kHz) and good thermal properties [34] rendering them a good option for the MFT design. In [7], [31] and [20], the above materials were used in the MFT design presenting an efficiency of over 98%. It should be noted that the evaluation of the transformer losses should be done in an actual power converter context. For example, in [41], a DAB converter is implemented and the MFT efficiency is extracted.

Moreover, the design process that is proposed by various authors is made by using different optimization algorithms. In some medium frequency transformers, the design procedures are hidden inside genetic algorithms whereas the design procedures with nanocrystalline materials are barely available to the open literature [41]. Consequently, a more systematic approach for solving the transformer design issue, should be considered.

2.4 Energy Storage Elements

The high-power MV DC/DC converters that will be built for this project, are destined for supplying an energy storage unit in the output. So, it is reasonable to investigate, briefly, the state of the art technology in the field of energy storage elements.

There are several ways, nowadays, for energy storage such as the fuel cells, the conventional capacitors, the batteries as well as the ultracapacitors (or supercapacitors). A comparison in terms of energy and power density between all of them, is shown in Figure 2.11.

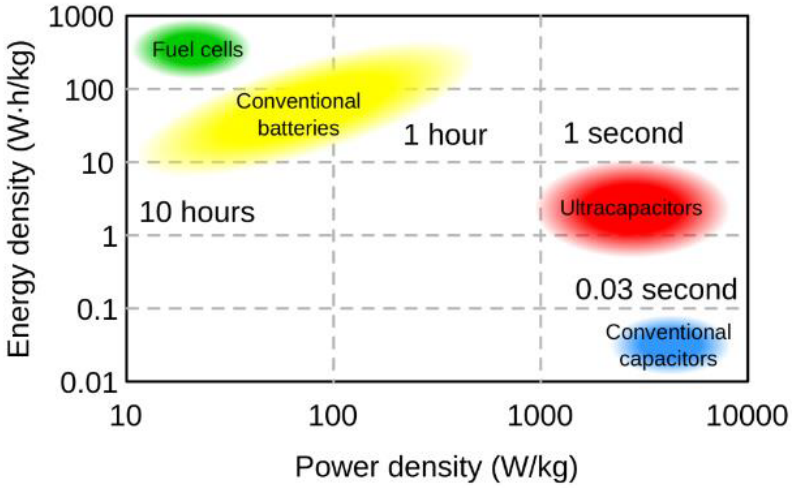

Figure 2.11. Power & energy density comparison between battery & ultracapacitors [40]

According to the figure, the two dominating ways for energy storage are the batteries and the ultracapacitors. The battery presents high energy density, slow charge and discharge process and low power density. Moreover, it degrades over time and it constitutes a slow and steady energy supplier [40]. On the other hand, the ultracapacitor shows fast charge and discharge time, high power density, low energy density and no loss of storage capability [40].

The ultracapacitor is a type of capacitor, capable of holding much more electrical charge than a standard capacitor and it has a high capacitance value. Nevertheless, it is limited to low voltages. Although, batteries and ultracapacitors may seem similar, there is a fundamental difference between them. In an ultracapacitor, the potential energy is stored in an electric field, while in a battery, it is stored in a chemical form. Further analysis into the physics of these storage units is out of the scope of this thesis.

There are plenty of battery and supercapacitor types. A specific type of ultracapacitor which seems promising is the Lithium-ion Capacitor (LiC). Potential applications are in the field of wind power generation systems, UPS or PV systems which require high energy and power density as well as durability. However, the ESS that use Li-ion batteries are by far the most widely used systems [21] and in electromobility the Lead-acid and Lithium-ion Phosphate batteries dominate as the primary power source. As a result, the selection between the two, is heavily dependent on the application case and its requirements.

2.5 Conclusion

In this chapter, the state of the art technology that aids towards the high power MV DC-DC converters technology was presented. The analysis started from the semiconductor point of view. Next, it went through the already examined MV DC-DC topologies and the MFT design of the isolated topologies. Finally, the possible energy storage units of such a converter was, shortly, discussed. Also, some of the challenges and limitations that occur by implementing MV DC-DC converters in a MVDC grid context were stated. To sum up, some of the challenges are:

- The WBG devices incorporation in MV converters. Still, the WBG are under investigation, in terms of reliability and performance, and they are not widely accepted and used by the industry.
- The selection of the appropriate MV DC-DC converter topology for each application case.
- The medium frequency transformer design in case of an isolated MV DC-DC converter topology is a topic that needs attention and investigation.

Regarding the limitations on constructing MV DC-DC converters:

- The current rating of the WBG devices on a medium voltage level is low nowadays, compared to the Si, but it is estimated that this drawback will be overcome soon. For instance, the 6.5kV Si modules can easily handle hundreds of amperes, whereas the 10kV SiC MOSFETS dies are not able to manage more than 10-20 amperes at the moment.
- The cost of these materials is higher than the conventional Si rendering the use of these devices restricted in the industry.
- Additionally, there is an open debate if a DC grid is preferable over the conventional AC that are dominant today. Therefore, the development of MV DC-DC is slow and limited.

Problem Statement 3

In this chapter, the project is analyzed and formulated, and the methodology along with the main limitations are presented.

3.1 Analysis

This project demonstrates the development of a medium voltage DC-DC converter based on 10kV SiC MOSFETS for charging an energy storage unit. The design and comparison of two candidate medium voltage DC-DC converters that were selected, is essential part of the thesis scope. Verification of the design and operation of the converters using digital tools is also made. Finally, the two candidate topologies are compared by various means and one of them is proposed for the energy storage application.

3.2 Formulation

The goal of this thesis is to propose a high-power and medium voltage step-down DC-DC converter topology for charging a battery, using the 10kV SiC MOSFETS modules that researchers from AAU designed. Special requirements are the scalability and the high efficiency of the suggested circuit. For this, two candidate topologies are compared and one of them is proposed for energy storage purposes. The schematics of the suggested DC-DC converters are depicted in Figure 3.1 and in Figure 3.2 respectively. The first one is the Single Active Bridge (SAB) and the other one is a buck-derived topology. They consist of a DC input voltage, a DC-AC unit, a transformer, a rectifier, a filter stage and a load. The only difference between these circuits, in terms of components, is only the output filter inductor which is absent on the SAB.

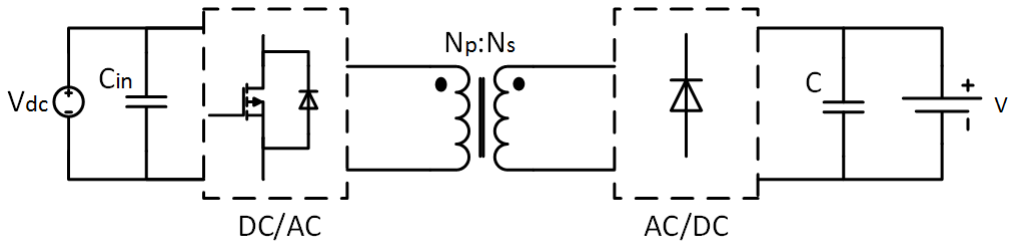

Figure 3.1. Uni-directional medium voltage SAB DC-DC converter

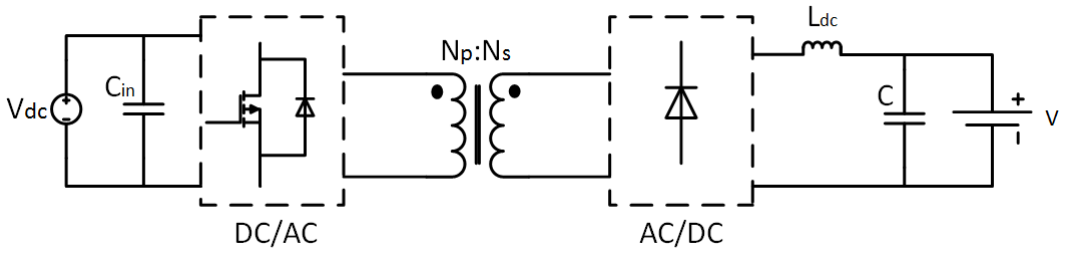

Figure 3.2. Uni-directional medium voltage DC-DC buck-derived converter

A medium frequency transformer is included in both circuits. This comes from the fact that, galvanic isolation and high voltage transformation are required. Similar circuits have been already proposed for low power applications but the question is, if they are applicable for a high power MV application.

Consequently, the general hypothesis is the following:

It is possible to connect batteries to MV grid and use SiC devices in a MV DC-DC converter with galvanic isolation to achieve this.

The 10kV SiC power modules that were provided for this project, are fully designed and packaged at AAU. The power modules had not been used previously in a DC-DC converter context and therefore another hypothesis of the medium voltage research team is that

It is possible to build a DC-DC converter with the specific 10kV SiC power modules that were designed and packaged at AAU.

The converter specifications are tabulated in Table 3.1, where P stands for the nominal power level, V_{dc} for the input DC voltage and V for the battery voltage in the output.

Parameter	Value
P [kW]	50
V_{dc} [kV]	6
V [kV]	0.8

Table 3.1. Medium voltage DC-DC converter specifications

3.3 Methodology

The methodology of this project follows the standard pattern for solving an engineering problem. To begin with, an extensive research on the subject has been conducted in order to fully understand the topic and its scope. The research included a deep literature investigation as well as interaction with the supervisor. After collecting all the necessary information, two possible topologies are proposed and a theoretical analysis is developed via mathematical equations in order to predict the behavior of the DC-DC converters. Afterwards, simulation models for both converters have been developed in LTSpice, to observe their performance. Through the simulations, the two converters are compared, based on specific factors, and one of them is considered as suitable for the application

given the requirements. Experiments have been carried out after building the proposed converter in the laboratory. In the end, the simulated along with the experimental results are evaluated and compared.

3.4 Limitations

In this project, some limitations were present since the beginning of the project and they are listed below:

- The control of the low voltage side stays out of the scope. Consequently, unidirectional DC-DC step down converters are studied and only the high voltage side is controlled.
- The construction of the transformer was assigned to a company as the transformer design would be time-consuming for a master thesis time limit.
- A certain time was required to get accustomed to LTSpice, Altium Designer and DSP programming.
- The low laboratory experience of the author on constructing a high power converter setup was also a general limit, which needed to be overcome, and delayed some of the processes.

Mathematical Modeling of the Converters 4

In this chapter the mathematical modeling of the two converter topologies is carried out in order to predict and understand their operation. Additionally, it will be shown how the output voltage is controlled through the phase shift pulse width modulation technique and how this scheme

4.1 Buck-Derived DC-DC Converter Topology

The converter topology is depicted in Fig 4.1. The input stage consists of the DC voltage supply V_{dc} along with the DC-link capacitors C. Then, a full-bridge inverter is present, which outputs a 3-level ($-V_{dc}$, 0, V_{dc}) or a 2-level ($-V_{dc}$, V_{dc}) pulsating AC waveform. The SiC MOSFETS of the single phase full bridge contain their equivalent parasitic capacitance in parallel for achieving soft-switching conditions. Afterwards, The AC waveform is stepped down by a factor N_s/N_p due to the transformer. Next, it is rectified and through a second order filter, a reduced output voltage and current ripple on the load R is achieved.

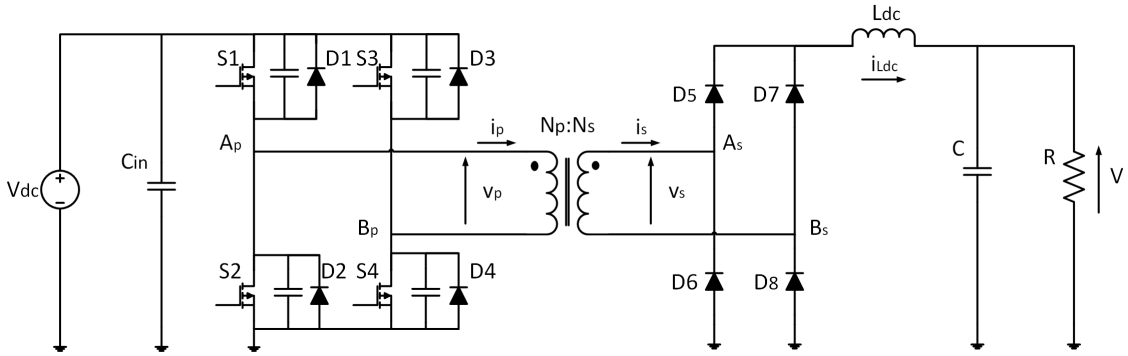

Figure 4.1. Uni-directional medium voltage DC/DC buck-derived converter

4.2 Phase Shift Principle

Phase shift pulse width modulation is a technique for controlling the pulse width of the output voltage of the full-bridge inverter (v_p) and by implementing this method, ZVS can be achieved during the switching instants of the MOSFETS.

As a first step, the duty cycle D should be defined in order to have consistency on the converter modeling. For that purpose, the Figure 4.2 will be used where the phase shift

switching principle is demonstrated. In this switching scheme, the width of the pulses is kept the same around half a switching period and this time interval is larger than the

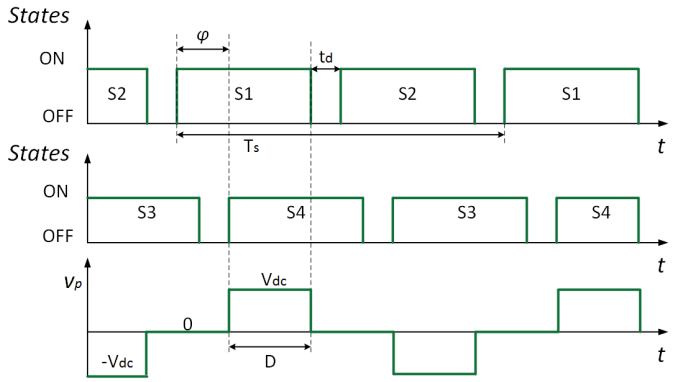

Figure 4.2. Phase shift switching scheme

conduction time of each diagonal pair as it is shown in Figure 4.2. The switches $S1$ and $S2$ form the leading leg while $S3$ and $S4$ constitute the lagging one. A small delay time (dead time) t_d is inserted for avoiding potential short-circuit conditions of the DC-link due to the series connected transistors of the two legs. For maximum utilisation of the switches, t_d should be very small compared to the switching period.

The voltage across the primary winding v_p changes, by varying the phase shift angle ϕ. An increase in the angle ϕ will call for a lower voltage whereas a decrease will step up the voltage. The length of one voltage pulse can be extracted using the Figure 4.2 and it is:

$$t_{pulse} = D \cdot \frac{T_s}{2} = \frac{T_s}{2} - t_d - t_\phi \tag{4.1}$$

4.3 Buck-Derived DC-DC Converter Modeling

4.3.1 Operating Conditions

In this section a detailed explanation will be given, regarding the ZVS buck-derived converter. In order to represent the behaviour of the converter via analytic equations, an equivalent circuit is used which is shown in Figure 4.3. The input voltage of the simplified equivalent circuit is the output of the half-bridge v_p, namely a periodic and pulsating waveform with three levels $(-V_{dc}, 0, V_{dc})$ or two $(-V_{dc}, V_{dc})$ depending on the phase shift angle. Afterwards, through the transformer it is scaled down to a pulsating waveform with levels $(-nV_{dc}, 0, nV_{dc})$ or $(-nV_{dc}, nV_{dc})$. Next, the secondary voltage v_s is rectified (V_{rect}) and through a second order filter it is smoothed. The rectified voltage V_{rect} presents two levels $(0, nV_{dc})$. The output voltage V can be considered as constant, assuming small ripple approximation.

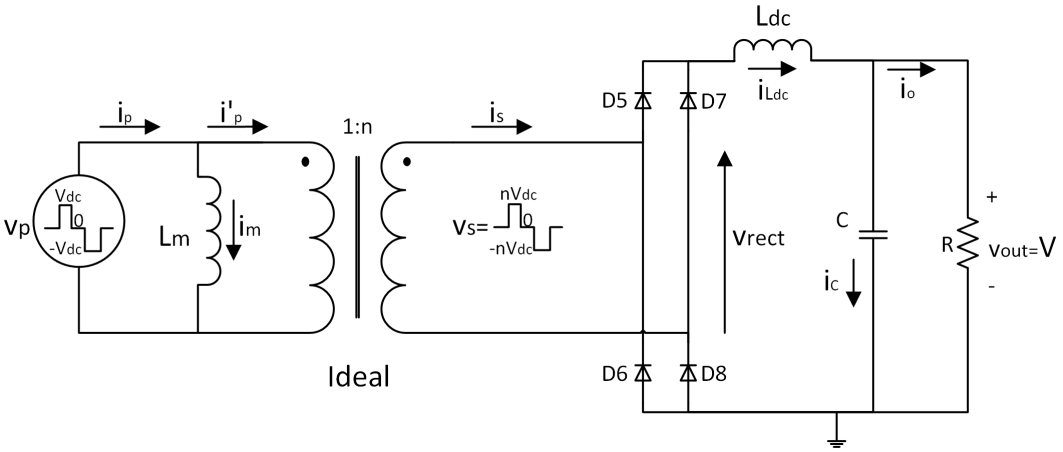

Figure 4.3. Simplified AC equivalent circuit for the buck-derived DC-DC converter

The transformer model that ignores the leakage inductance will be used for the next analysis as it is assumed that the leakage inductance value is much lower compared to the value of the DC output filter inductor. The explanation covers one half cycle in CCM and it is separated in the following time intervals.

- $t_0 < t < t_1$: In this time interval, the diagonal switches $S1$, $S4$ along with the diodes $D5$, $D8$ conduct (Figure 4.4). The primary winding of the transformer v_p is charged by the input voltage V_{dc} and the primary winding current rises from i_{p0} to $i_{p,peak}$ as it is shown in Figure 4.5. In the low voltage side one can state given that $v_p = V_{dc}$ for this time interval:

$$v_{L_{dc}} = nV_{dc} - V \Rightarrow \frac{di_{L_{dc}}}{dt} = \frac{nV_{dc} - V}{L_{dc}} = \frac{di_s}{dt} \tag{4.2}$$

because $i_{L_{dc}} = i_s$ in that interval. Moreover, it is known that the reflection of the primary current to the secondary winding is $i_s = i_p/n$. Hence, the primary winding current slope is obtained as:

$$\frac{di_p}{dt} = \frac{n(nV_{dc} - V)}{L_{dc}} \tag{4.3}$$

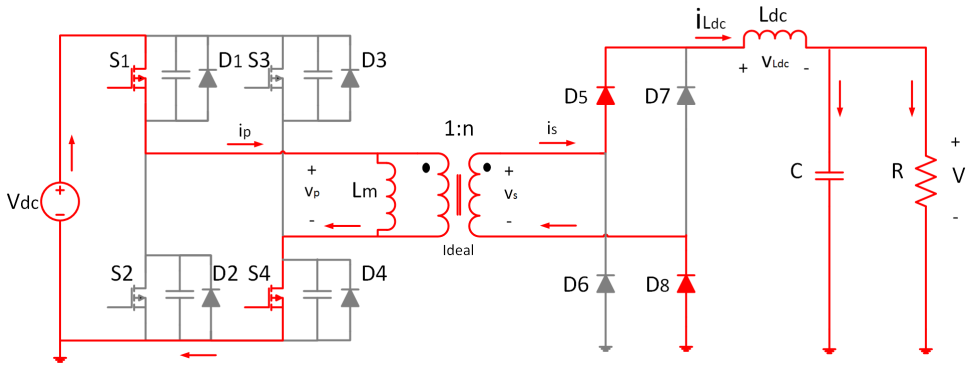

Figure 4.4. Equivalent circuit at $t_0 < t < t_1$

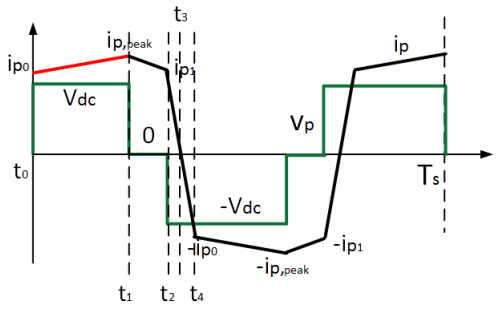

Figure 4.5. Primary winding current i_p along with the primary voltage v_p at $t_0 < t < t_1$

- $t = t_1$: The first resonant transition occurs at this time instant (Figure 4.6). The $S1$ switch is still on while $S4$ stops conducting. The current that was flowing through the diagonal switch pair $S1$ and $S4$ does not stop directly, but instead it passes through the capacitors $C4$ and $C3$ (Figure 4.7) resulting to a lossless turn-off of the $S4$ device. The capacitor $C4$ charges up to the DC-link voltage V_{dc} while $C3$ discharges to zero volt. This zero voltage of $C3$ constitutes the voltage across the semiconductor $S3$ equal to zero. In fact it is not exactly zero, but equal to the voltage drop of the anti-parallel diode which starts to conduct during this abrupt transition. Therefore, the switch is able to turn on without losses (ZVS). Finally, a relation can be derived for the slope of the capacitors voltage. By observing that $i_{C_3} = i_{C_4} = i_p/2$ and $C_3 = C_4 = C$ and by using the well-known equation for the capacitors currents we can obtain:

$$\frac{dV}{dt} = \frac{1}{2C} \cdot i_p \tag{4.4}$$

  This is an important relation for deriving the dv/dt that the device will experience. However, the MOSFET parallel capacitance varies over time, but for simplicity it was assumed as a constant quantity in Equation (4.4).

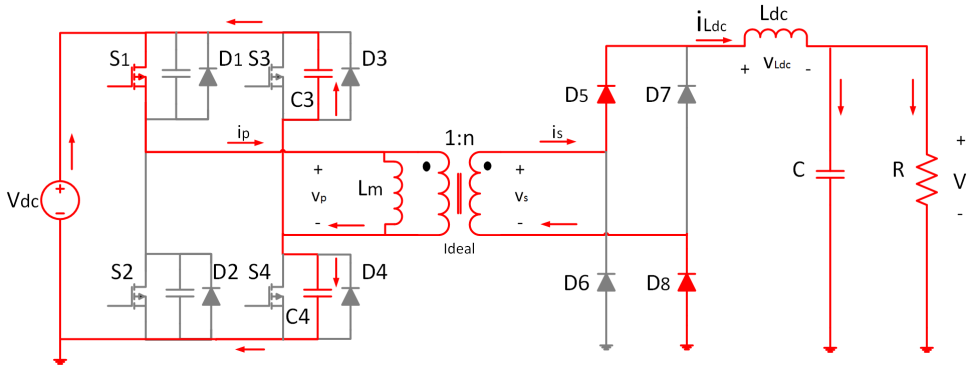

Figure 4.6. Equivalent circuit at $t = t_1$

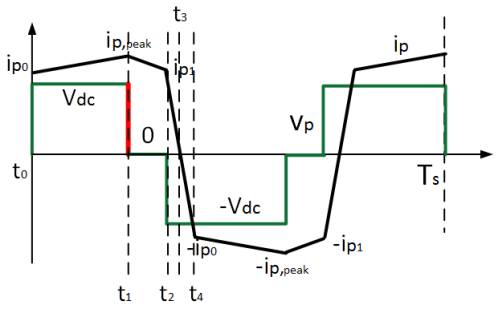

Figure 4.7. Primary winding current i_p along with the primary voltage v_p at $t = t_1$

- $t_1 < t < t_2$: During that interval $S1$ is still on while the diode $D3$ is forced to conduct as the anode presents a higher potential than the cathode (Figure 4.8). In fact, the current splits into $D3$ and $S3$ as the MOSFETS are able to conduct in a reverse direction (source to drain) and it drops from $i_{p,peak}$ to i_{p1}. The primary winding current slope (Figure 4.9) can be obtained after reflecting the quantities L_{dc}, V on the primary side we have:

$$\frac{di_p}{dt} = \frac{\frac{-V}{n}}{\frac{L_{dc}}{n^2}} = \frac{-nV}{L_{dc}} \tag{4.5}$$

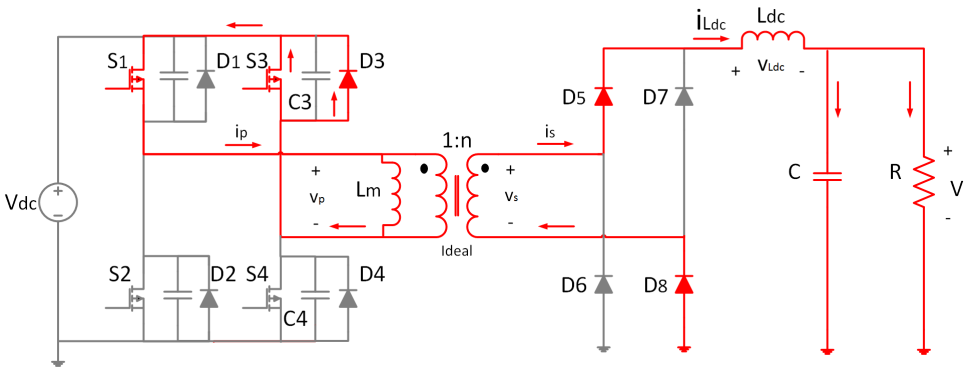

Figure 4.8. Equivalent circuit at $t_1 < t < t_2$

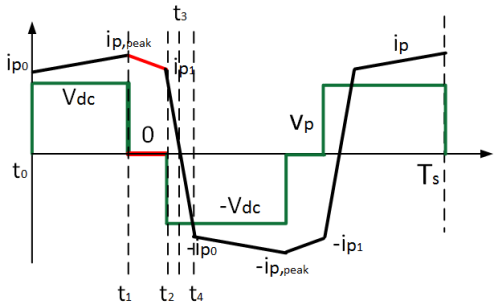

Figure 4.9. Primary winding current i_p along with the primary voltage v_p at $t_1 < t < t_2$

- $t = t_2$: The second resonant transition happens at that time moment. In Figure 4.10 the conducting elements are shown and in Figure 4.11 the primary voltage transition state is illustrated. The $S1$ switch turns off and as the primary current is still positive, the current flows through the $C1$ and $C2$ capacitors. Now, the voltage across the $S2$ device reaches zero, and the MOSFET can turn on without losses. It should be noted that there is a time instant when all the diodes of the output bridge are forward-biased resulting to a short-circuited secondary winding as the voltage across the leakage inductor equals to $-V_{dc}$.

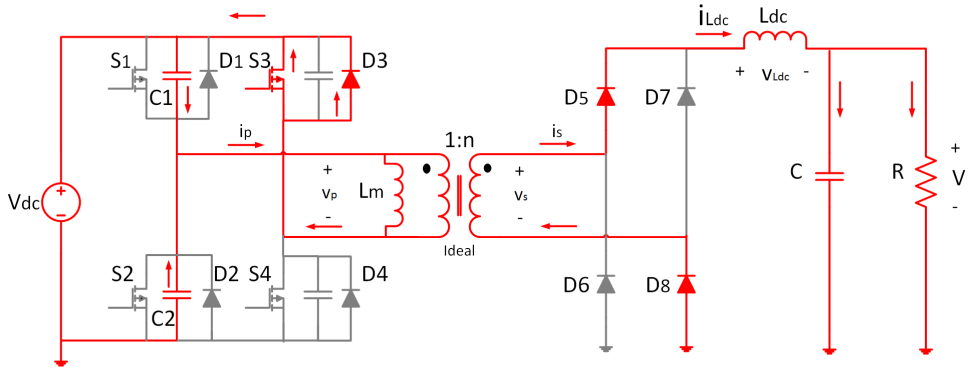

Figure 4.10. Equivalent circuit at $t = t_2$

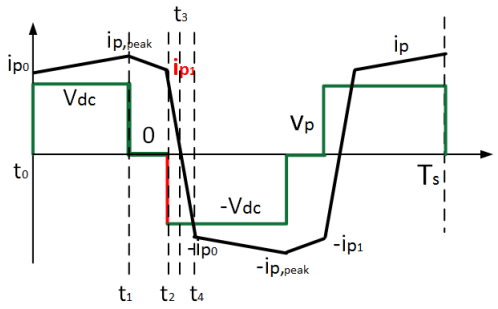

Figure 4.11. Primary winding current i_p along with the primary voltage v_p at $t = t_2$

- $t_2 < t < t_3$: Now, $-V_{dc}$ voltage is applied to the primary winding, the secondary is still short-circuited and the primary winding current falls from i_{p1} to zero. The diodes $D2$ and $D3$ are forward biased as the primary current is still positive (Figures 4.12, 4.13). The MOSFET $S2$ is able to be activated under zero voltage (ZVS). The primary winding current rate is determined, now, by the leakage inductor L_σ and that is why it is not ignored in this time period and it is drawn in Figure 4.12. Therefore:

$$\frac{di_p}{dt} = -\frac{V_{dc}}{L_\sigma} \tag{4.6}$$

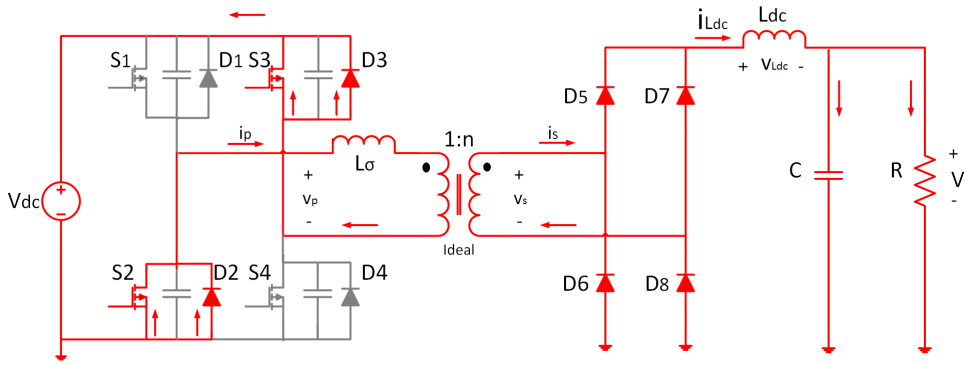

Figure 4.12. Equivalent circuit at $t_2 < t < t_3$

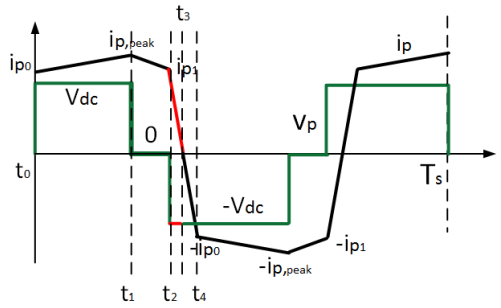

Figure 4.13. Primary winding current i_p along with the primary voltage v_p at $t_2 < t < t_3$

- $t_3 < t < t_4$: The final interval of a half cycle happens now. The devices $S2$ and $S3$ conduct and the primary winding current is reversed (Figures 4.14 and 4.15). At $t = t_4$, the current that was passing through the anti-parallel diodes $D5$ and $D8$ goes to zero and the output inductor L_{dc} starts to store energy again.

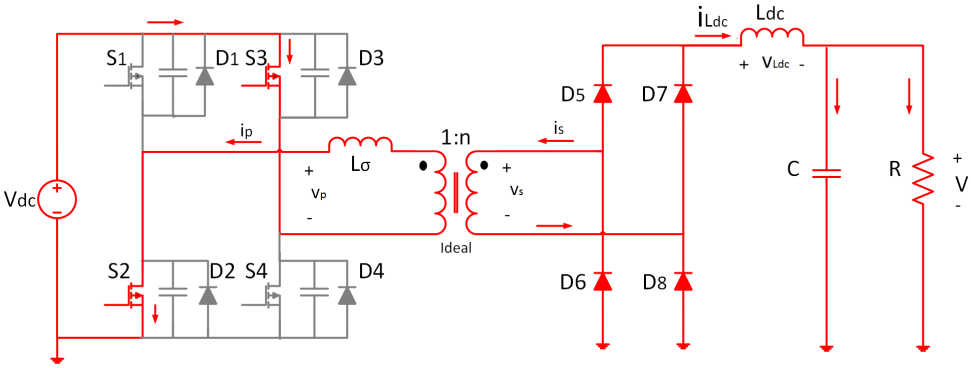

Figure 4.14. Equivalent circuit at $t_3 < t < t_4$

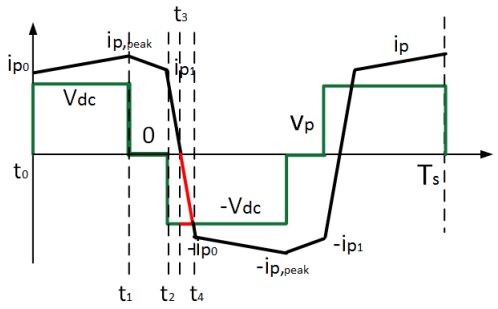

Figure 4.15. Primary winding current i_p along with the primary voltage v_p at $t_3 < t < t_4$

By using the Figure 4.3 some more details can be stated for this converter.

- During the first switching mode, the switches S_1, S_4 are on for time DT_s, applying $V_{dc}DT_s$ volts-seconds to the magnetizing inductor and hence to the primary winding. So, the voltage across the magnetizing inductance will be:

$$v_{L_m} = V_{dc} \Rightarrow L_m \frac{di_m}{dt} = V_{dc} \Rightarrow \frac{di_m}{dt} = \frac{V_{dc}}{L_m} \tag{4.7}$$

  According to (4.7) the magnetizing current increases with a positive constant slope.

- During the second switching mode, the transistors S_2, S_3 conduct applying $-V_{dc}DT_s$ to the primary. Here, the rate of change in the magnetizing current will be:

$$\frac{di_m}{dt} = -\frac{V_{dc}}{L_m} \tag{4.8}$$

- When $v_p = 0$, the output inductor L_{dc} discharges and the magnetizing current will remain constant. At this case, the switches S_1 and D_3 or S_3, D_1 are on in order to maintain the current flow and provide zero voltage on the primary winding.

Regarding the voltage of the secondary winding, it follows the ratio of the transformer, namely

$$v_s = v_p \cdot \frac{N_s}{N_p} = n \cdot v_p \tag{4.9}$$

where $n < 1$ for the case of the buck converter.

All the above are summarized in Figure 4.16 where the basic waveforms of the converter are shown and assuming zero voltage drop on the semiconductor devices. The converter operates in CCM and the output inductor current has a ripple of Δi value.

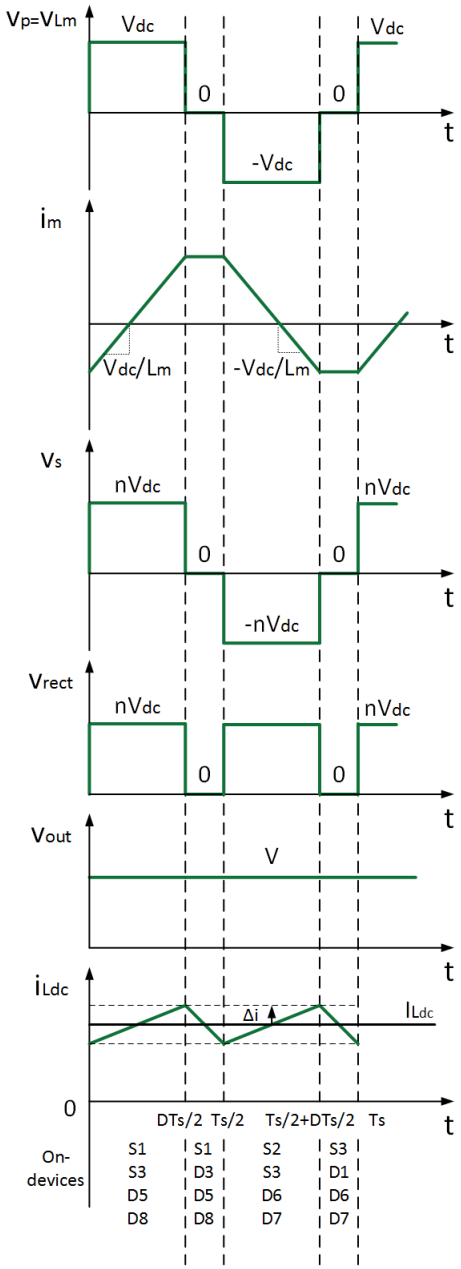

Figure 4.16. Buck-derived DC-DC converter waveforms

Observing the schematic in Figure 4.3, the voltage across the output inductor will be:

$$v_{L_{dc}} = v_{rect} - V \tag{4.10}$$

Applying volt-seconds balance to the output inductance it is obtained that:

$$< v_{L_{dc}} >= 0 \Leftrightarrow \frac{1}{T_s/2} \int_0^{T_s/2} v_{L_{dc}}(t) = 0 \tag{4.11}$$

$$\Leftrightarrow (nV_{dc} - V)DT_s + (-V)(1-D)T_s = 0 \tag{4.12}$$

$$\Leftrightarrow nV_{dc}D = V \tag{4.13}$$

$$\Leftrightarrow D = \frac{V}{nV_{dc}} \tag{4.14}$$

Equation (4.14) denotes the transfer function of the circuit. It should be noted that the secondary winding voltage presents a time delay compared to the primary winding voltage and as a result, it lasts a shorter time period than D. More specific, when the primary winding voltage rises from zero to V_{dc}, the secondary winding voltage does not increase from zero to nV_{dc} directly, but instead it stays at zero volt for a small time period. This is due to the secondary winding that remains short circuited in order to deliver the current to the output. This time shift usually is referred as effective duty ratio D_{eff}. In [5], an analytic approach for deriving this effective duty ratio of the secondary winding is given. Therefore, D_{eff} should be entered in 4.14 and not D, but given that this time delay is tiny compared to the duty cycle, it was neglected for the whole above analysis and $D = D_{eff}$ was considered.

4.3.2 Zero Voltage Switching Condition

However, in order to ensure ZVS conditions, the energy stored in the leakage inductor L_σ just before the transition at $t = t_2$ (Figure 4.11) should be greater than the energy stored in the resonant capacitor which is parallel to the MOSFET [5]. Hence, the following condition stands for ZVS:

$$\frac{1}{2}L_\sigma i_{p1}^2 \geq \frac{1}{2}CV_{dc}^2 \tag{4.15}$$

Solving with respect to i_{p1} we obtain:

$$i_{p1} \geq V_{dc} \cdot \sqrt{\frac{C}{L_\sigma}} \tag{4.16}$$

At this time instant the leakage inductor is the element that supplies energy to charge $C1$ and discharge $C2$. That is why the energy stored in it should be larger.

But the primary winding current heavily depends on the load current. Consequently, at light loads the ZVS condition tends not to be satisfied and the converter ends up to operate under hard switching mode. Some calculations can be made for extracting the critical load current for ensuring ZVS conditions. Placing the secondary current i_s instead of i_p in the Figure 4.9 and referring to the Equation 4.5 we have:

$$\frac{i_{s1} - i_{s,peak}}{(1-D)\frac{Ts}{2}} = -\frac{V}{L_{dc}} \Rightarrow i_{s1} = i_{s,peak} - \frac{V}{L_{dc}}(1-D)\frac{Ts}{2} \tag{4.17}$$

In fact, the current $i_{L_{dc}}$ through the DC output inductor, is just a rectified version of the secondary winding current. Moreover, $i_s = i_{L_{dc}}$ during the previous time interval when the output inductor charges. Hence, by using the Figure 4.16, the quantity $i_{s,peak}$ can be rewritten as:

$$i_{s,peak} = I_{L_{dc}} + \frac{\Delta i}{2} \tag{4.18}$$

where Δi is the inductor current ripple. Inserting Equation 4.18 into the Equation 4.17 we take:

$$I_{L_{dc}} = i_{s1} - \frac{\Delta i}{2} + \frac{V}{L_{dc}}(1-D)\frac{Ts}{2} \tag{4.19}$$

Finally, using the Equation 4.16 and reflecting the secondary winding current value i_{s1} to the primary winding current value i_{p1}, the required output current for ensuring ZVS is obtained:

$$I_{L_{dc}} \geq \frac{V_{dc}}{n} \cdot \sqrt{\frac{C}{L_\sigma}} - \frac{\Delta i}{2} + \frac{V}{L_{dc}}(1-D)\frac{Ts}{2} \tag{4.20}$$

4.4 Single Active Bridge Converter Topology

The single active bridge (SAB) converter is presented in this section. The actual schematic of this circuit is shown in Figure 4.17.

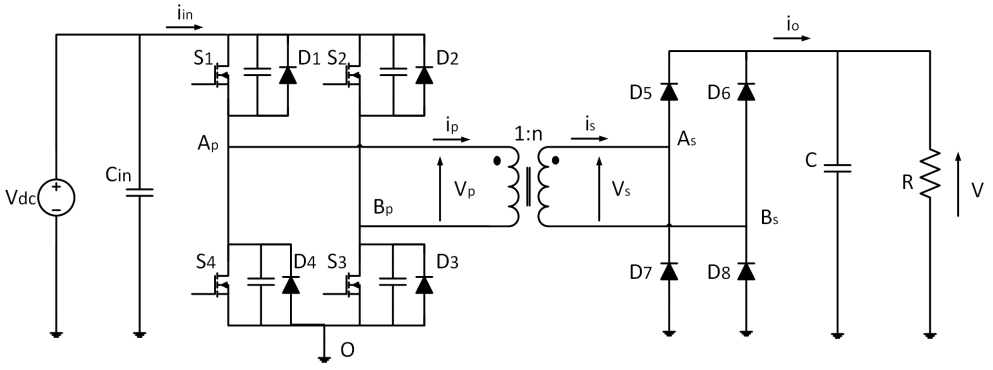

Figure 4.17. Schematic of the SAB converter

Component-wise, the difference of the SAB compared to the buck-derived topology, is only the output filter inductor which is absent in a SAB converter. Consequently, only the output capacitor plays the role of filtering the load current and voltage. This converter can also operate under soft-switching conditions.

4.5 Single Active Bridge Converter Modeling

The operating waveforms of this topology are shown in Figure 4.18. Three operating modes are presented, denoted as I, II, III on the graph. Also, the devices that conduct during each time interval are indicated.

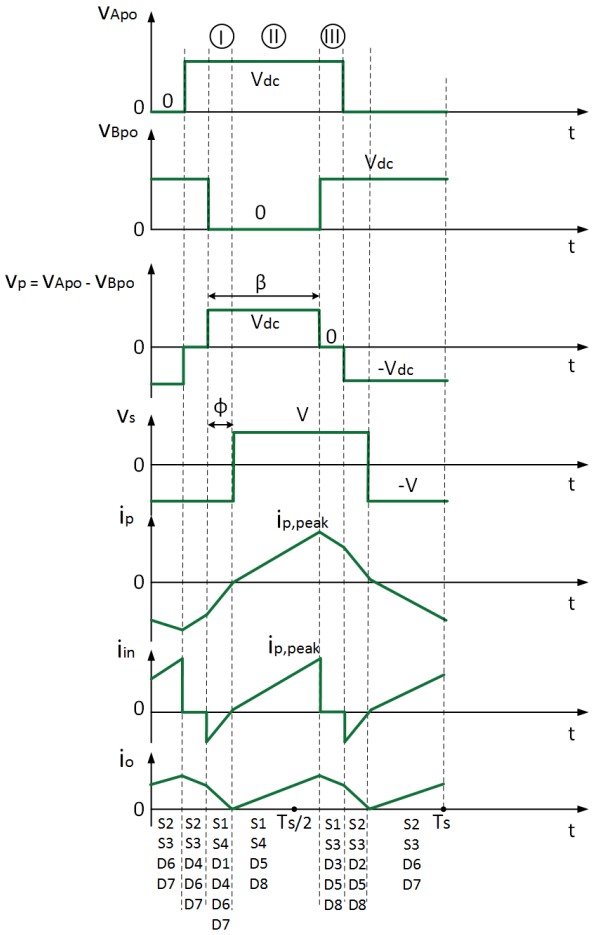

Figure 4.18. Operating waveforms of the SAB [15]

It can be seen, that soft switching is obtained by ensuring that MOSFET turn-on, only happens when its anti-parallel diode conducts. The circuit operation is similar with the buck-derived topology in terms of the ZVS conditions, so it will not be explained further. The biggest problem of this topology seems to be the large ripple current that flows through the output filter capacitor as well as the high current stress of semiconcuctors [15].

For modeling this converter, a different approach has to be followed compared to the buck-derived one. In this topology, the leakage inductance of the transformer, should not be discarded as previously. Therefore, assuming a very large magnetizing inductance, negligible current flows through it at high frequencies, and the transformer is modeled only by its primary-referred equivalent leakage inductance. The following primary-referred equivalent circuit in Figure 4.19, simplifies the analysis of the SAB where L_σ stands for the total primary-referred equivalent leakage inductance of the transformer and V' for the primary-referred output voltage.

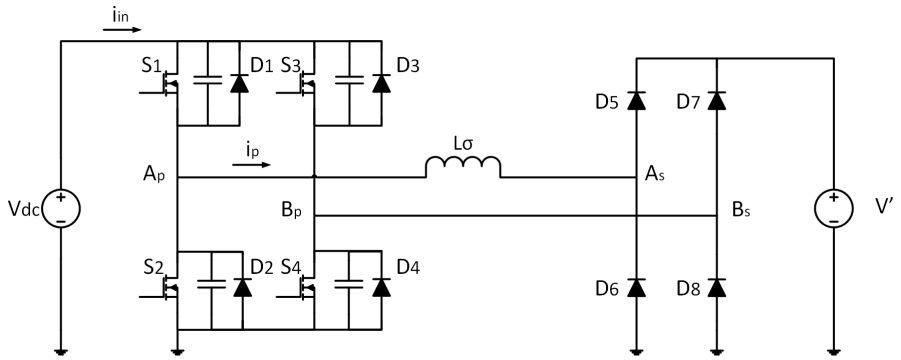

Figure 4.19. Primary-referred equivalent circuit for the SAB [15]

- Mode I: The primary winding voltage is positive and the secondary winding voltage is negative in this interval. So:

$$\frac{di_p}{dt} = \frac{V_{dc} + V'}{L_\sigma} \tag{4.21}$$

- Mode II: Now, the current is positive. Also the primary winding along with the secondary winding voltages are positive. Hence:

$$\frac{di_p}{dt} = \frac{V_{dc} - V'}{L_\sigma} \tag{4.22}$$

- Mode III: Here, the primary winding voltage is zero while the secondary winding voltage is positive. The inductor current equals to:

$$\frac{di_p}{dt} = \frac{-V'}{L_\sigma} \tag{4.23}$$

Additionally, according to [15], the following expressions can be extracted for the phase shift ϕ and power transfer P_0 at a given voltage pulse width β, d and T_s:

$$\phi = \frac{1}{2}(\beta - d\pi) \tag{4.24}$$

$$P_o = V_{dc} I_{in} = \frac{d V_{dc}^2 T_s}{8\pi L_\sigma}\left[2\beta - \pi d^2 - \frac{\beta^2}{\pi}\right] \tag{4.25}$$

where I_{in} is the average value of the input current i_{in} and d is the DC conversion ratio and it equals to:

$$d = \frac{V'}{V_{dc}} \tag{4.26}$$

From Equation (4.25) it is obvious that the power transfer capability is inverse proportional to the total leakage inductance and switching frequency.

Finally, in [15], it is proven that the maximum transfer power occurs when $\beta = 180^o$. As a result, the above equations are modified to the following ones:

$$\phi = \frac{1}{2}\pi(1-d) \tag{4.27}$$

$$P_o = \frac{V_{dc}^2 T_s}{8L_\sigma} d\left[1-d^2\right] \tag{4.28}$$

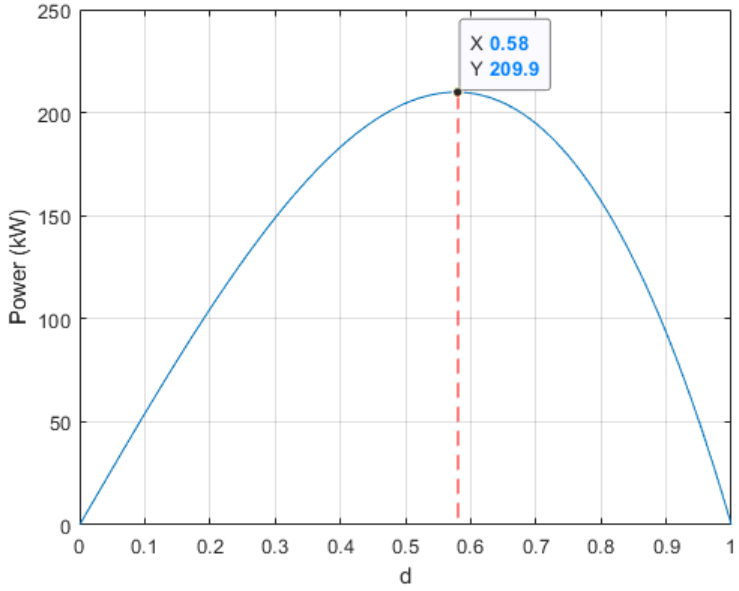

Figure 4.20. Power transfer capability curve

Now, if we plug into Equation 4.28, the values for V_{dc}, T_s, L_σ, the maximum power transfer capability for the converter of the specific project can be obtained. The maximum power occurs at $d = 0.58$ and it equals to 210kW approximately.

Another interpretation of the circuit in Figure 4.19 is depicted in Figure 4.21. The AC primary winding voltage is connected to the AC secondary winding voltage via the inductance L. The structure is similar to that of a synchronous machine connected to the grid through the line impedance [42]. If transistors would be present in the output bridge, bidirectional power flow could be feasible and therefore the active and reactive power could be controlled by varying the magnitude and the phase relationship between the AC output voltages [42].

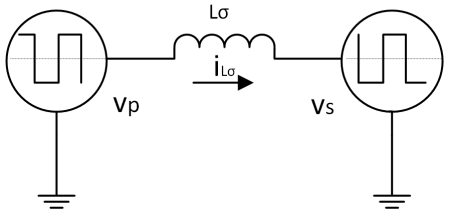

Figure 4.21. SAB AC equivalent circuit

4.6 Conclusion

In this chapter, the mathematical modeling of the two medium voltage DC/DC converters was presented through equivalent circuits, detailed equations and characteristic waveforms under continuous conduction mode. Also, the phase shift principle was discussed for the control of the converters output power. Moreover, the soft-switching conditions were explained and how these are achieved in these converters for obtaining higher efficiency. The information that was acquired through this analysis, will be used to design the converters in the next chapter.

Hardware Design of the Converters Setup 5

In this chapter, the hardware of the converters setup will be presented. The setup of the converters will be separated into its main parts and each of them will be further analysed.

5.1 Design Parts of the Converters

After gaining some insight on the converters operation, the next step was to consider the parts that need to be designed and built afterwards in the lab. In order to have a fair comparison between the two topologies, only the output filter inductor will be the different part. By observing the Figure 4.1, the buck-derived converter consists of the following parts that need to be considered:

1. DC-link capacitors
2. High voltage side full-bridge inverter
3. Medium Frequency Transformer
4. Low voltage side diode bridge
5. Output filter
6. Digital Signal Processor

5.1.1 DC-link Capacitors

Figure 5.1. Image of the DC-link capacitor bank

The DC-link busbar that it is going to be used is illustrated in Figure 5.1. Two capacitors of 50μF are placed in series creating a mid-point and resulting to a total capacitance of

25μF for the input filter. The busbar has aluminum plates and a sandwiched layout which is preferred for a low stray inductance from the DC-link to the power module.

For safety reasons, the discharge of the DC-link capacitors is also considered. For this, a relay mechanism is used which is shown in Figure 5.2 and a simplified schematic of the relay is presented in Figure 5.3. It consists of two resistors R_1 and R_2 of 1.2kΩ and a relay S. The discharge time constant will be $\tau = 1.2k\Omega \cdot 25\mu F = 30ms$.

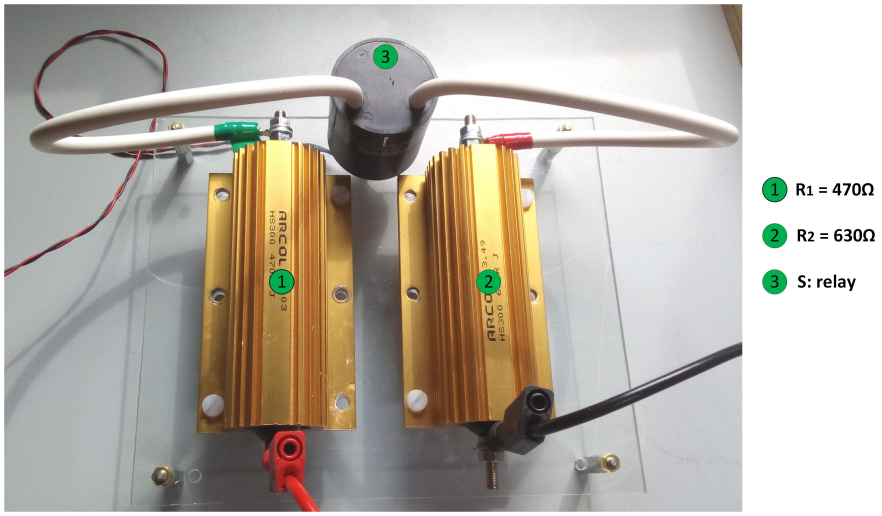

Figure 5.2. Photograph of the relay protection

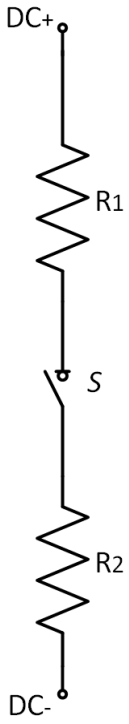

Figure 5.3. Simplified schematic of the relay protection

5.1.2 High Voltage Side Full-Bridge Inverter

The 10kV SiC MOSFET power module that it is going to be used for the converters is depicted in Figure 5.4. This is a half-bridge power module with 3rd generation Wolfspeed 10kV/17A SiC MOSFET dies which was designed and packaged at the Department of Energy Technology of Aalborg University. An important improvement of the 3rd generation die is that it presents higher gate to source threshold voltage and this change offers less immunity to noise and parasitic turn on [29]. The designed DBC layout along with the higher robustness of the MOSFET die allow a switching speed of $21kV/\mu s$ [29]. In [29], there is a detailed explanation about the packaging process that was followed for minimum parasitic capacitances. Two of these power modules connected to the DC-link capacitors will constitute the full-bridge inverter.

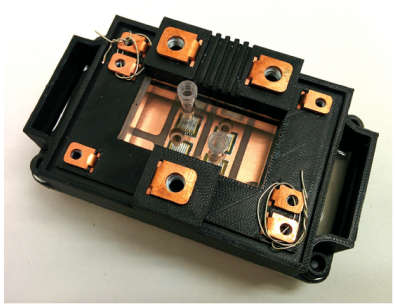

Figure 5.4. Photograph of the 10kV SiC power module [29]

A gate driver is required in order to drive the half-bridge power module. For this, a gate driver has been designed at the Department of Energy Technology of Aalborg University with low isolation capacitance regulated DC-DC power supply and an active Miller clamping circuit [12]. A top view of the circuit is illustrated in Figure 5.5.

Figure 5.5. Image of a gate driver circuit [12]

This gate driver design, faces two main problems that occur at medium voltage SiC power modules and they will be described briefly. First of all, the mid-point in half-bridge power module experiences high dV/dt during switching transients. The isolation barriers inside the power module and interfacing circuitry which experiences the dV/dt, introduce the common mode current due to capacitive coupling [13]. The main path for this current is through the isolation barrier of the DC-DC power supply of the high side gate driver circuit as shown in Figure 5.6. Consequently, this current has to be mitigated, for maintaining a reliable operation of the gate driver. This is done by minimizing the isolation capacitance C_{iso}.

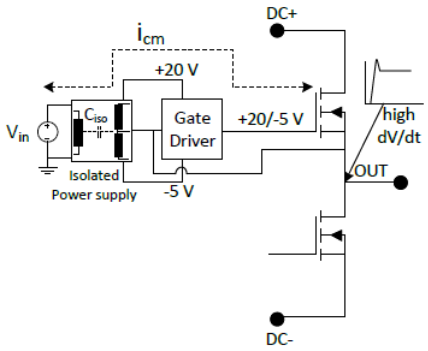

Figure 5.6. Illustration of the common mode current path [13]

Furthermore, the high dV/dt switching transients may result to unwanted turn on in a half bridge power module due to the Miller effect during the turn on process of the complementary switch [46]. To avoid this, an active Miller clamp circuit is designed and incorporated into the gate driver [13].

5.1.3 Medium Frequency Transformer

Although the complete transformer design and construction was assigned to a company, some design requirements were set to the engineers. Hence, a personal meeting with the RND engineers was arranged to discuss about the transformer details. The first design requirements that were given to them along with the transformer specifications are listed in Table 5.1.

Primary/Secondary rms current (A)	8.33/62.5
Primary/Secondary voltage (kV)	6/0.8
Power rating (kVA)	50
Switching Frequency (kHz)	2.5
Primary/Secondary number of turns	150/20
Primary Leakage Inductance (μH)	≤ 300
Primary Magnetizing Inductance (mH)	150
Primary/Secondary winding capacitance (pF)	$\leq 20/\leq 1100$
Core Material	Nanocrystalline

Table 5.1. Initial medium frequency transformer specifications

These design requirements were the result of literature investigation on the topic of medium frequency transformers for medium voltage DC-DC converters and an iterative process between simulations and rough calculations by hand, until the desired requirements to be achieved.

More specific, Equation (4.28) was used to derive a pair of values between the leakage inductance and the switching frequency, keeping in mind that low leakage inductance value is required for a high power transfer capability. Next, nanocrystalline material was chosen for the core, given that it presents some critical identities for low core losses, as it

was discussed in Section 2.3. Moreover, the formula below was used for an estimation of the self-inductance of the primary winding

$$L = \mu_0 \frac{N^2 A}{l_{air}} \tag{5.1}$$

where μ_0 is the magnetic permeability of free space, N is the number of turns, A is the inner core area and l_{air} stands for the length of the air gap. Assuming a specific rough value for the ratio A/l_{air} the magnetizing inductance value was extracted as a first step.

Also, by knowing that the transformer presents parasitic capacitances across and between its windings (see Figure A.2), unwanted resonances will occur on the primary and secondary winding voltages and therefore low winding and inter-winding capacitances should be realized for the transformer. Through simulations, desired winding capacitance values for the primary and secondary windings are below $20pF$ and $1100pF$ respectively, for mitigating the ringing of the windings voltage.

However, the company ended up with different design specifications which are tabulated in Table 5.2. It can be easily observed, that the final specifications of the transformer are quite dissimilar. Moreover, the transformer that the company constructed is depicted in Figure 5.7.

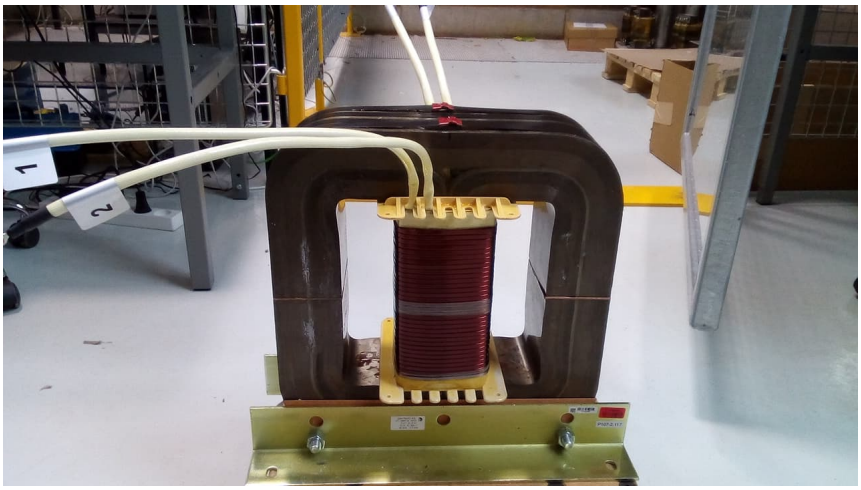

Figure 5.7. Photograph of the medium frequency transformer

Primary/Secondary number of turns	245/33
Primary/Secondary Leakage Inductance (mH)	1.65/0.03
Primary/Secondary Magnetizing Inductance (mH)	330/6
Primary/Secondary winding capacitance (pF)	77/4244
Primary/Secondary winding resistance (Ω)	1.3/0.023
Inter-winding capacitance (pF)	227
Core Material	Amorphous

Table 5.2. Final medium frequency transformer specifications

According to the company, during the ordering period the nanocrystalline material was out of stock. Consequently, given that the time limitation for a master thesis is strict, the next option was the Ferromagnetic Amorphous Alloy material for the transformer core which also shares the same main characteristics with the nanocrystalline.

The number of turns is larger and therefore higher windings resistance and leakage inductance value are expected. The capacitance of the windings is also larger than the predicted ones. However, the magnetizing inductance is quite high which means that the magnetizing inductance will draw a very small current resulting to lower core losses.

It should be noticed that the values inserted in Table 5.2, are the ones that were actually measured in the lab after testing the transformer. The transformer parameters were obtained using the Keysight E4990A impedance analyzer. More specific, the following three measurement methods were followed to extract the main transformer elements:

- The primary inductance was measured directly by keeping the secondary open and connecting the instrument across the connectors of the primary (*CONN 1*, *CONN 2*) as shown in Figure 5.8. Note, that the primary inductance measurement result includes the effects of the winding capacitance. The equivalent circuit analysis function of the impedance analyzer returned the individual values for inductance (L_p), resistance ($R_{\sigma p}$) and capacitance (C_p) of the primary winding. The same process was followed for measuring the respective quantities of the secondary. However, the magnetizing inductance value depends on the magnetizing current that flows through it and the impedance analyzer applies only a small amount of current. Hence, different magnetizing value should be expected during real operation.

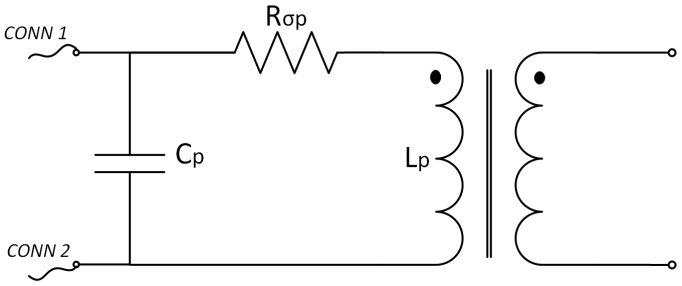

Figure 5.8. Primary inductance measurement

- The primary leakage inductance is obtained by shorting the secondary with the lowest possible impedance and measuring the inductance of the primary as shown in Figure 5.9. Moreover, The primary is shorted and the secondary winding leakage inductance is found.

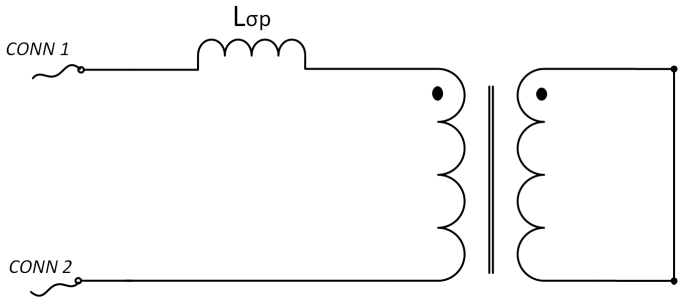

Figure 5.9. Primary leakage inductance measurement

- Regarding the inter-winding capacitance C_m, it can be measured as it is illustrated in Figure 5.10.

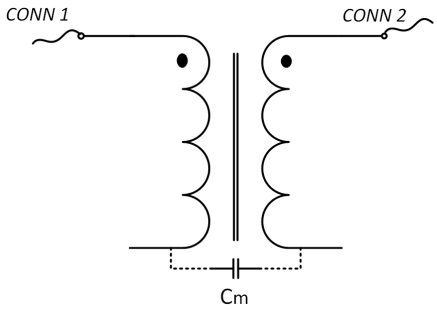

Figure 5.10. Inter-winding capacitance measurement

- The turns ration N_s/N_p can be easily calculated after having measured the primary and secondary inductance L_p, L_s respectively, by using the formula

$$L_s = \left(\frac{N_s}{N_p}\right)^2 \cdot L_p \tag{5.2}$$

Hence, $N_s/N_p \approx 0.1348$. Then, the number of turns of the secondary winding were easily counted and they are found to be $N_s = 33$. Finally $N_p = 245$.

5.1.4 Low Voltage Side Diode Bridge

For the low voltage side, a rectifier stage had to be designed and built on a PCB. In the buck-derived topology, high voltage spikes occur across the diodes. This comes from the fact that the leakage inductance of the secondary winding is connected, essentially, in series with the diodes and a voltage across it appears during the turn off process of the diode. As a result, a protection circuit should be realized for this topology. For this, a RCD type of snubber is chosen and later, it will be shown how this circuit is incorporated into the actual topology. It should be noted that the snubber circuit is not needed for the single active bridge topology. This is an advantage of the SAB converter over the buck-derived.

The first step towards the PCB design process was to estimate the power consumption of the diodes along with the snubber in order to select the appropriate heatsink. For this, the buck-derived was simulated in LTSpice under nominal conditions and the power

dissipation of the rectifier and the snubber was extracted. It was found to be more than a half a kilowatt. This is a quite big amount of consumption for a PCB and dangerous enough for the junction temperature of the diodes. Hence, a large heatsink would be required. An obvious solution was to insert more diodes in parallel per each arm of the bridge for a better thermal stress distribution. The diode that is selected, is the LSIC2SD120E40CC, a SiC Shottky diode rated at 1.2kV and 40A at 150°C whose circuit diagram is illustrated in Figure 5.11. In the next, the term "diode component" is assigned to the LSIC2SD120E40CC as it contains internally two diodes and they are both used in the parallel configuration scheme described above.

Also, the forward voltage drop as well as the on resistance of the diode component at 125°C has been taken into account for the simulations. By placing two diode components per each arm, the power dissipation of the rectifier and the snubber fell to around 250W which means a fifty percent reduction on the power dissipation.

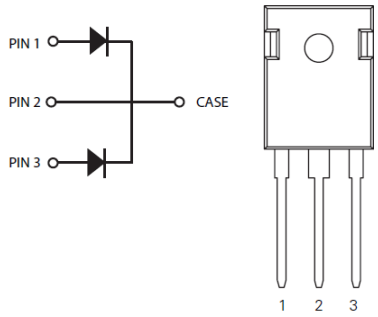

Figure 5.11. Circuit diagram of the diode component

Afterwards, a thermal circuit in PLECS (Figure 5.13) was made in order to justify that the temperature rise across the junction of a single diode component lies into a safe range. In Figure 5.12, the simplified equivalent thermal circuit that it is going to be used is shown for one semiconductor. Between junction and ambient, three thermal resistances can model the temperature drop. The total thermal resistance between junction and ambient is given by

$$R_{JA} = R_{JC} + R_{CS} + R_{JSA} \tag{5.3}$$

where R_{JC}, R_{CS}, R_{SA}, denote the thermal resistance between junction to case, case to sink and sink to ambient respectively. Therefore, the temperature of the junction of the diode component can be estimated by

$$T_J = R_{JA} \cdot P_{loss} + T_A \tag{5.4}$$

where P_{loss} stands for the power loss of the semiconductor and T_A for the ambient temperature.

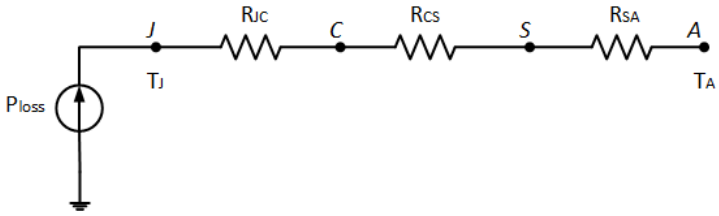

Figure 5.12. Equivalent thermal model

Hence, the circuit of Figure 5.12, is expanded to cover the total number of the eight diode components (two per each arm). In Figure 5.13, P_{diode} indicates the simulated power consumption of a diode component and R_{jc} is the junction to case thermal resistance which was found through the datasheet. For the R_{cs} which is the case to sink thermal resistance a typical value that is suggested for the TO-247 package was inserted. The R_{sa} can be extracted from the datasheet of the heatsink and T_A is fixed at 25°C. Then, the eight diode components are connected together to form the total equivalent thermal circuit.

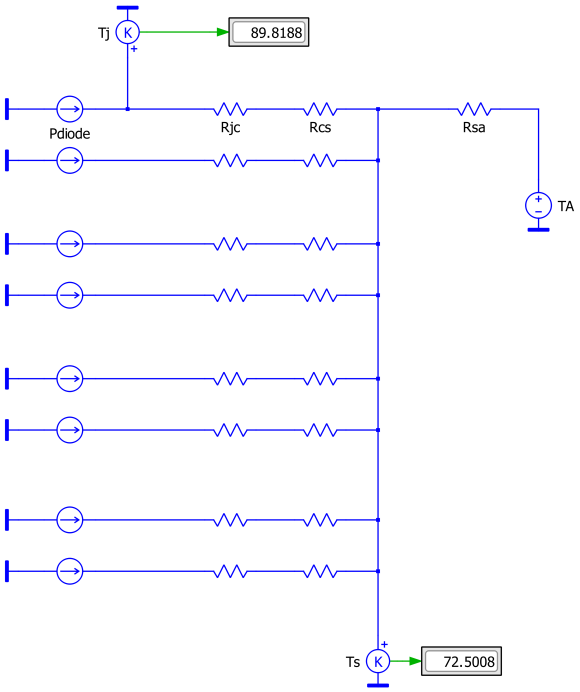

Figure 5.13. Thermal circuit of the diode bridge

The junction temperature reaches, roughly, 90°C, a value which is much lower than the maximum junction temperature that the diode component is able to withstand (175°C).

The parameters of the thermal model can be found in Table 5.3

Parameter	Value
P_{diode} $[W]$	24.74
R_{jc} [°C/W]	0.6
R_{cs} [°C/W]	0.1
R_{sa} [°C/W]	0.24
T_A [°C]	25

Table 5.3. Parameters of the simplified equivalent thermal circuit

Regarding the value and the model of the components of the snubber they are listed in Table 5.4. Also, the heatsink that it was used is shown.

Parameter	Value	Model
R $[k\Omega]$	22	TE Connectivity SQM5 Series
C $[nF]$	100	AVX 1825AC104KAZ2A
D	-	LSIC2SD120E40CC
Heatsink	-	Fisher Electronik LA 9

Table 5.4. Parameters of the snubber circuit

After the appropriate selection of the heatsink, the next step was to continue with the PCB design. For this, Altium Designer was used. The schematic of the rectifier and the snubber is depicted in Figure 5.14. Four capacitors are placed in parallel forming a 400nF total capacitance. Moreover, the resistor bank consists of five parallel branches each one of them with three resistors in series and the total resistance ends up to be $13.2k\Omega$. This resistor bank configuration was chosen because each of the resistors is rated at $22k\Omega/5$W which means that they can withstand a voltage of around 330V and as a result they can endure the 800V of the low voltage side.

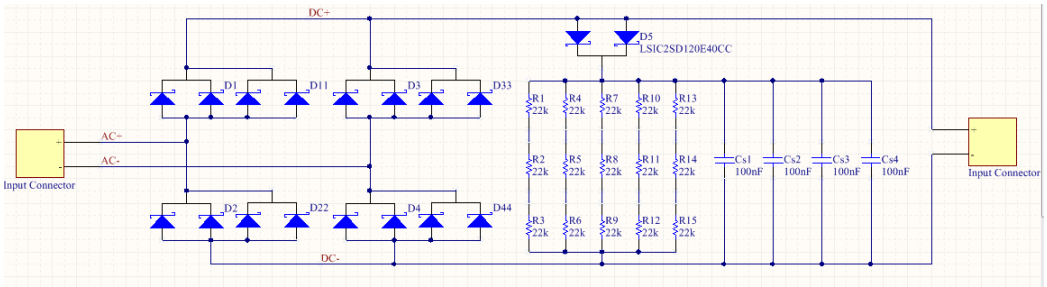

Figure 5.14. Schematic of the rectifier

The PCB layout can be seen in Figures 5.15 and 5.16. The connections to the AC-connection port are made through the bottom layer. Consequently, in order to have a more reliable connection, a slot was placed as it is seen in the bottom left of Figure 5.15.

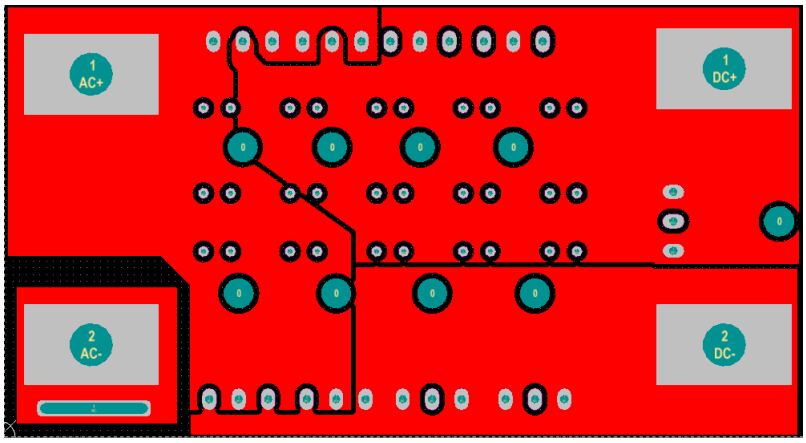

Figure 5.15. Image of the top layer of the PCB

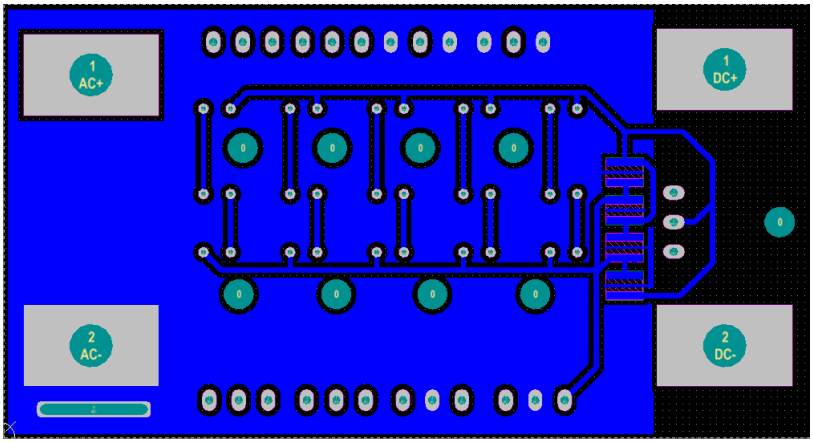

Figure 5.16. Image of the bottom layer of the PCB

The final PCB along with the heatsink where it was placed, are illustrated in Figure 5.17 and in Figure 5.18. It was fully designed, constructed and soldered in the Department of Energy Technology of Aalborg University. Given that it is a high current PCB (62A nominal case), the thickest option for the copper was used. AAU laboratory provides a copper thickness of 105μm. It is also clearly observed, that the PCB is poured at most of its area with copper.

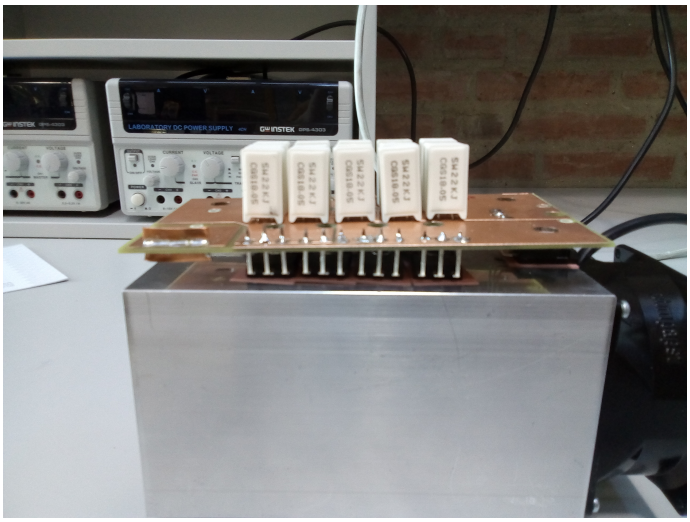

Figure 5.17. Side view of the diode bridge

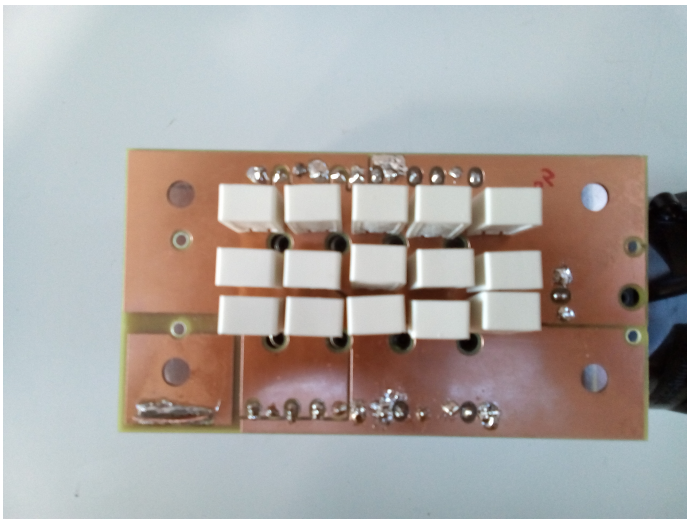

Figure 5.18. Top view of the diode bridge

5.1.5 Output Filter

The output filter is an essential part of any power converter. It improves the quality of the output by reducing the voltage and current ripple produced during the conversion. Usually, in a DC-DC converter case, a second order filter consisting of an inductor in series with the load and a capacitor placed in parallel with the load, play the role of filtering the output. The inductor is responsible for suppressing the voltage ripple, whereas the capacitor diminishes the output current ripple.

According to the Figure 4.3, the voltage across the inductor is

$$v_{L_{dc}} = v_{rect} - V \tag{5.5}$$

and by observing the Figure 4.16 it can be seen that $v_{rect} = nV_{dc}$ when the output inductor charges.

Consequently, we get

$$L_{dc}\frac{di_{L_{dc}}}{dt} = nV_{dc} - V \tag{5.6}$$

Additionally, assuming that the inductor charges and discharges almost linearly an approximate formula can be extracted for the required inductance of the output DC inductor

$$L_{dc}\frac{2\Delta i}{\Delta t} = nV_{dc} - V \Rightarrow L_{dc} = \frac{(nV_{dc} - V)DT_s}{2 \cdot 2\Delta i} \tag{5.7}$$

because the change in the inductor current $i_{L_{dc}}$ equals to $2\Delta i$ during the time interval $DT_s/2$ as it is seen in Figure 4.16. Also, $\Delta i = 0.2I_{L_{dc}}$ to $0.4I_{L_{dc}}$, where $I_{L_{dc}}$ is the DC component of the output inductor current, namely the current ripple has been considered between 20% to 40% a typical range for the filter inductor on a DC-DC converter. In addition, $I_{L_{dc}} = V/R$ as the DC component of the output capacitor is zero in steady state. All the quantities are known and therefore, the required inductance can be extracted.

The Power Electronics Systems Laboratory provided a DC inductor with an inductance value of 6mH and a current rating of 20A which is illustrated in Figure 5.19. So, in order to provide 62A, the nominal current rating of the output stage, four inductors have to be connected in parallel. Also, the resistance of the single inductor was measured and found to be 0.1Ω.

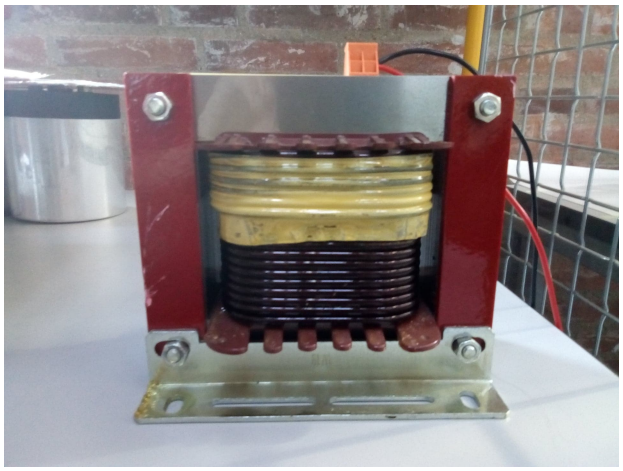

Figure 5.19. Photograph of the output filter DC inductor

Regarding the value of the output filter capacitance now, the following statements can be made. First of all, applying Kirchhoff's Current Law to the output node of Figure 4.3 we get

$$i_{L_{dc}} = i_C + \frac{V}{R} \tag{5.8}$$

Differentiating the above equation we take that the slope of the inductor current is the same with the slope of the capacitor current. Moreover, in Figure 5.20 the capacitor current along with the capacitor voltage are shown. It is assumed that the voltage ripple is small

and therefore all of the AC component of inductor current flows through the capacitor. The current is positive for a quarter of a period and due to this, the capacitor voltage lies between its minimum and maximum value during this interval.

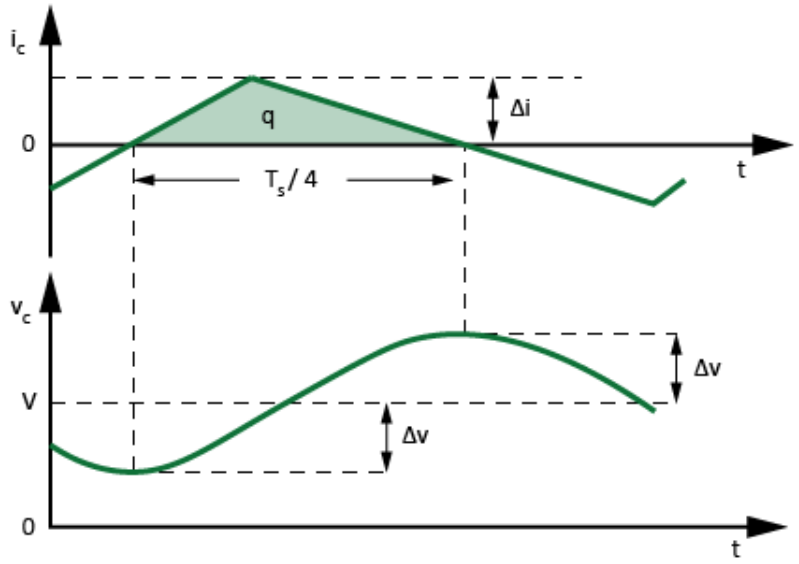

Figure 5.20. Capacitor current (top) and capacitor voltage (bottom) [19]

The total charge q that it is stored across the capacitor is

$$q = C \cdot 2\Delta v \tag{5.9}$$

where ΔV stands for the voltage ripple of the filter capacitor.

But the charge q can also be given from the area of the triangle which is above the t-axis. Hence,

$$q = \frac{1}{2}\Delta i \frac{T_s}{4} \tag{5.10}$$

Eliminating q and solving with respect to ΔV we get

$$\Delta v = \frac{\Delta i T_s}{16C} \tag{5.11}$$

So, the voltage ripple is analogous to the current ripple level. It should also be noted that in reality the voltage ripple further rises due to the equivalent series resistance (ESR) of the capacitor. For this project, an output voltage ripple of less than 5% was considered as acceptable.

The Power Electronics Systems Laboratory provided an output filter DC capacitor bank. It consists of six film capacitors of 450μF/1.2kV in a parallel configuration forming a total capacitance of 2.7mF with an ESR of 0.3mΩ. The capacitor bank is depicted in Figure 5.21.

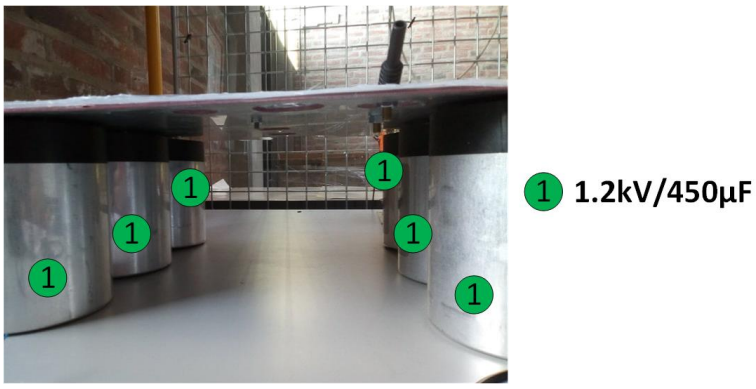

Figure 5.21. Side view of the output filter capacitors

The simulations prove that the value of the output capacitor and inductor, provide the required current and voltage ripple levels, but this will be shown later in chapter 6.

5.1.6 Digital Signal Processor

The generation of the pulses for the gates of the power modules is done via the interface board that is depicted in Figure 5.22. The DSP that is used is the TMS320F28379D from Texas Instruments. Code Composer Studio (CCS) software is used for the coding part.

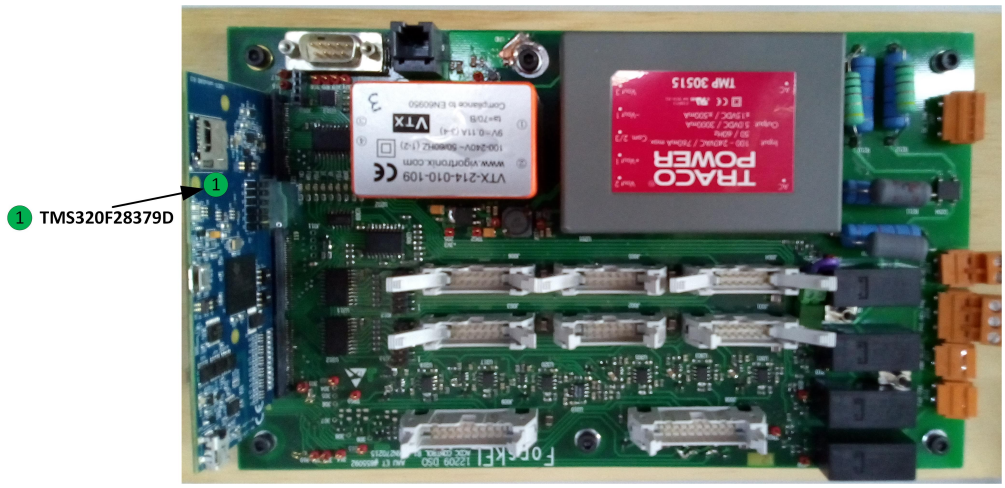

Figure 5.22. Photograph of the control board and the DSP

The deadtime interval that is chosen for a safe operation, is 2μs which is 0.5% of the selected switching period (400μs). In Figure 5.23, the 2μs deadtime is illustrated.

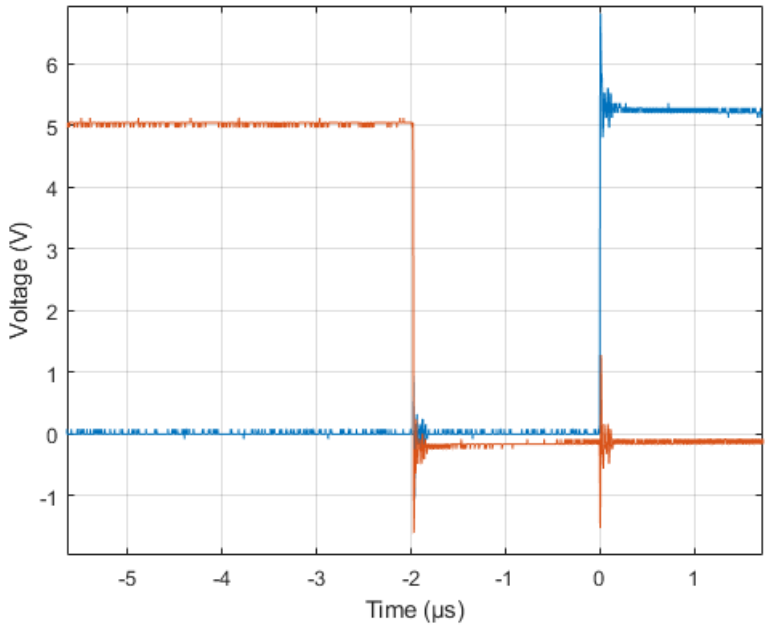

Figure 5.23. Deadtime illustration

Afterwards, the phase shift of the pulses was implemented through CCS and the result is shown in Figure 5.24. It also becomes noticeable that the duty cycle of the generated pulses is 50%. A final comment is that quite big spikes occur during the switching instants of the pulses. This might be because the measurement was made by using a passive probe, which adds capacitance, and as a result dv/dt. Later, in chapter 7, it will be seen that no spikes appear on the gate to source voltage of the power module.

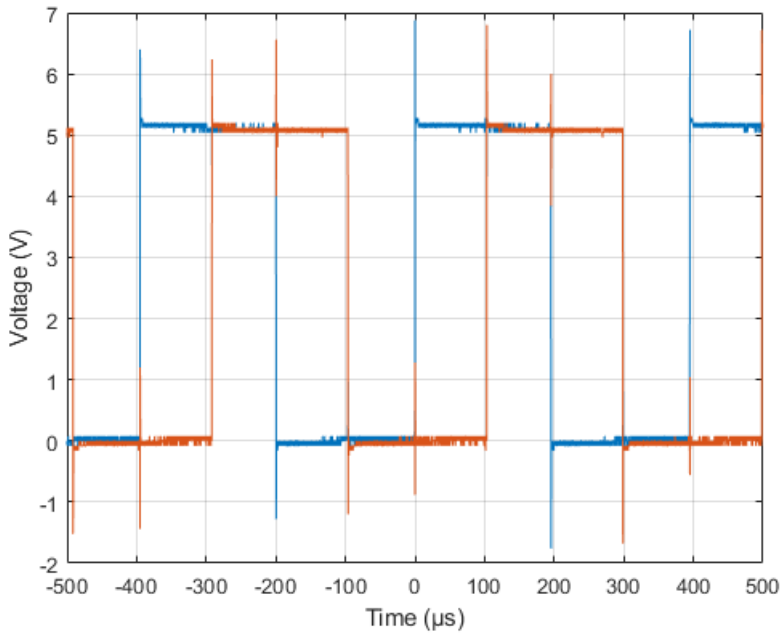

Figure 5.24. Phase shift of 90°

5.2 Conclusion

In this chapter, the hardware of the setup was described and presented in detail. In the next chapter, where the simulations will be shown, the exact design parameters of this chapter will be used for more realistic results.

Simulations of the Medium Voltage DC-DC Converters 6

After analyzing the operation of the circuits through mathematical equations, the next step is to simulate the converters in a simulation software. By doing this, a better understanding of the converters operation is achieved and the mathematical modeling is verified. After simulating both converters, a proper comparison between them is made, and one of them is chosen to be built in the laboratory. Therefore, through the simulations, the performance of the converters is predicted in some extent. LTSpice software is used for the simulations.

6.1 Buck-derived Converter Simulation

First of all, the buck-derived topology will be simulated. The whole topology is depicted in Figure 6.1. It consists of the DC input voltage along with the DC-link capacitor (*A.*), the DC/AC converter along with the PWM control scheme (*B.*), the transformer equivalent model (*C.*), the diode bridge with the RCD snubber included (*D.*) and finally, the output LC filter (*E.*) together with the load resistor. The load resistor emulates the battery.

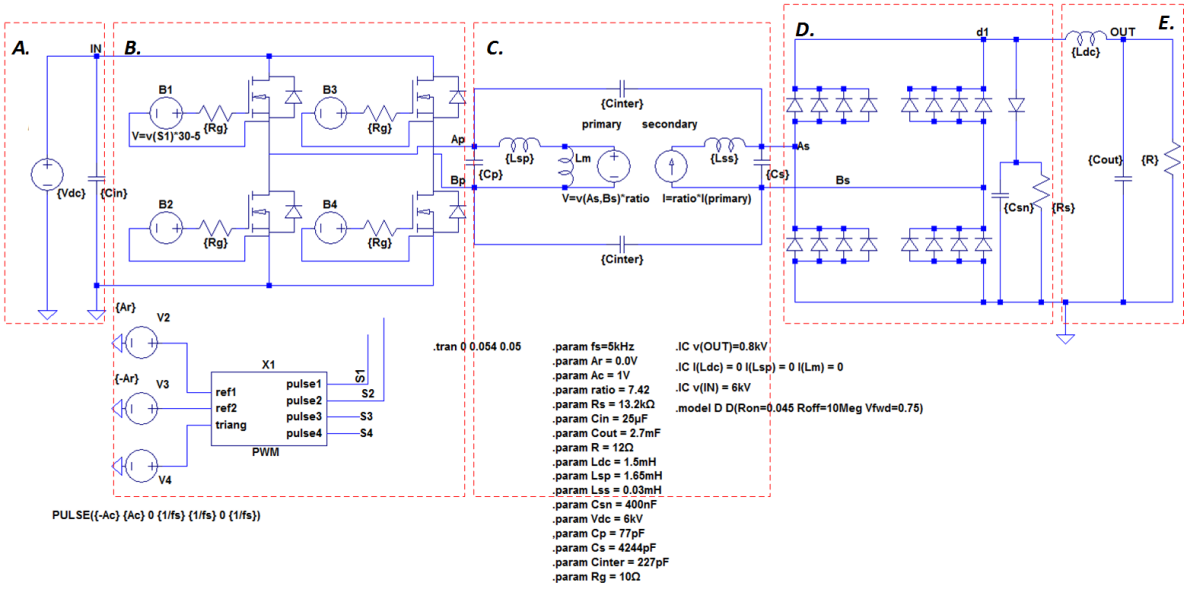

Figure 6.1. Simulation schematic of the buck-derived topology

The PWM is implemented according to the phase shift principle as described in part B of the Appendix part. Hence, the controlled parameter is not the duty cycle, which remains constant for both topologies at 50%, but the phase relationship between the legs. The

switching frequency of the converters is chosen at 2.5kHz and the dead-time interval at 2μs.

For the rest of the chapter, in order to clarify the quantities that will be illustrated in the next figures, the Table 6.1 is made. In the column "Electrical Quantity", current, voltage or power of a component is entered. In the column "Component/Nodes", the component or the nodes that the respective quantity is referring to in the simulation schematic of the Figure 6.1 is inserted. Therefore, the table below is filled as follows:

Electrical Quantity	**Component/Nodes**
MOSFET Current	Current through S1 MOSFET
MOSFET Voltage	Voltage across IN, A_p
Diode Current	Current into $d1$
Diode Voltage	Voltage across $As, d1$
MOSFET pulse	Switching state of S1 MOSFET
Primary winding leakage current	Current through L_{sp}
Magnetizing current	Current through L_m
Primary winding voltage	Voltage across A_p, B_p
Secondary winding voltage	Voltage across A_s, B_s
Output inductor current	Current through L_{dc}
Output voltage	Voltage at node OUT
Primary winding leakage voltage	Voltage across L_{sp}
Input Power	Power through V_{dc}
Output Power	Power through R

Table 6.1. Electrical quantities for plotting

In the beginning, the buck-derived topology is simulated and the phase shift ϕ is set to zero. The reason why the zero phase shift case was implemented, is to evaluate and verify the quality of some important characteristic waveforms of the components under maximum power transfer.

In Figure 6.2, the MOSFET current and voltage along with the diode current and voltage are shown in steady state. As it was already mentioned, huge spikes across the diodes were expected and they indeed appeared in the simulations, taking values of three times higher than the nominal voltage. The snubber achieves to vanish the voltage spikes. However, the oscillations during the off state of the diode are quite harsh. Moreover, the current spikes during the on process of the diode current, present a safe overshoot of around 10%. Finally, the peak current values of the semiconductors along with the RMS values, lie inside the safe operating region and consequently there is no danger for a failure and over-stress conditions.

Afterwards, it was examined if the converter operates under soft switching conditions as it was predicted in the mathematical modeling of the converter. In order to verify this, the Figure 6.3 is used. It is clearly observed, that during the on transition of the MOSFET the equivalent parallel MOSFET capacitance discharges and the voltage across the capacitor takes the value of the forward voltage drop of the anti-parallel diode. As a result, ZVS occurs as the voltage across the switch reaches almost zero before the

pulse arrives. ZVS conditions are also met during the turn off process. It should also be noted, that the LTSpice MOSFET model contains, internally, the parasitics of the specific packaged module that it is going to be used for the experimental setup for more accurate evaluation.

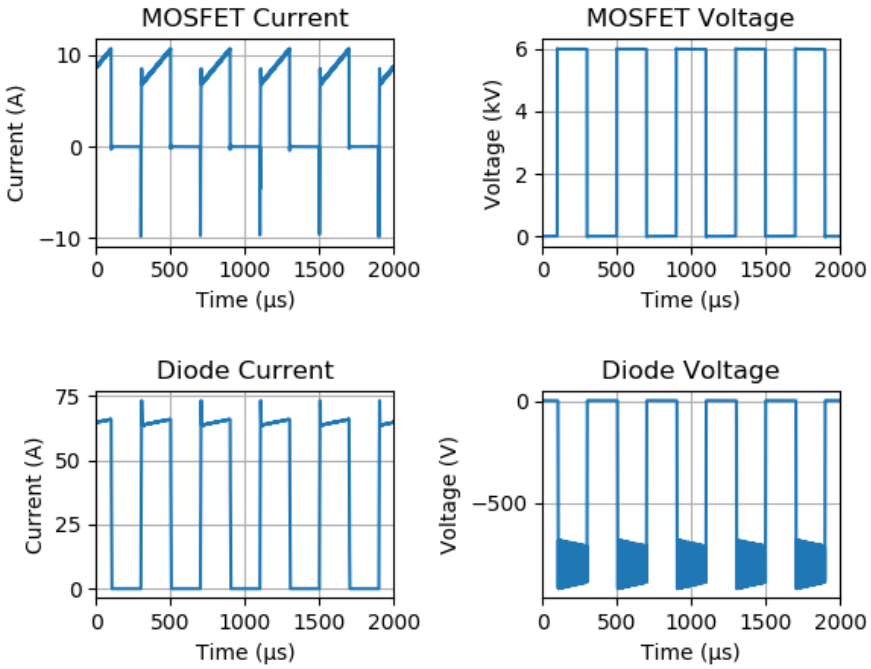

Figure 6.2. Waveforms of the switches for the buck-derived and $\phi = 0°$

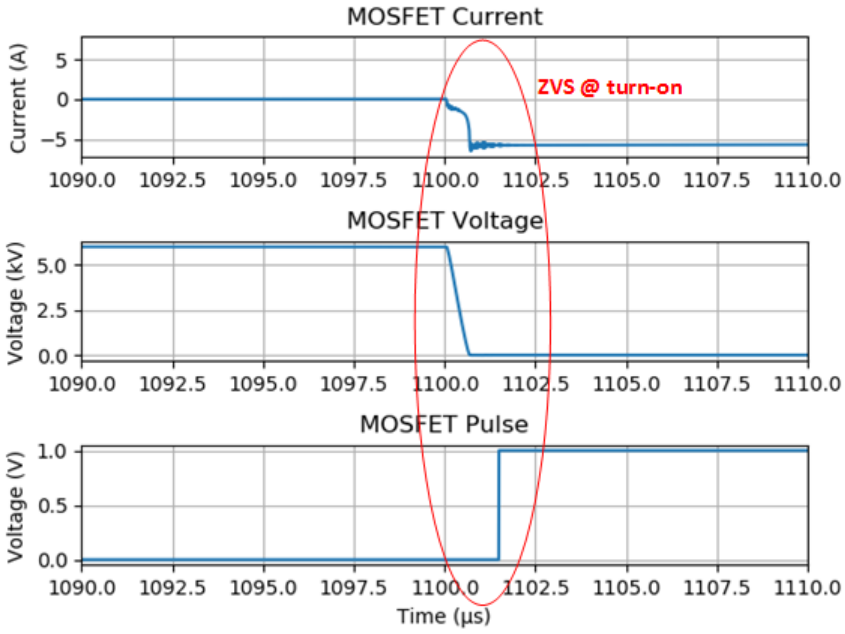

Figure 6.3. ZVS demonstration during turn on for the buck-derived

Next, in Figure 6.4, some characteristic waveforms of the transformer are shown. More specific, the following quantities are presented; the primary winding leakage current, the magnetizing current and the voltages across the primary and secondary winding.

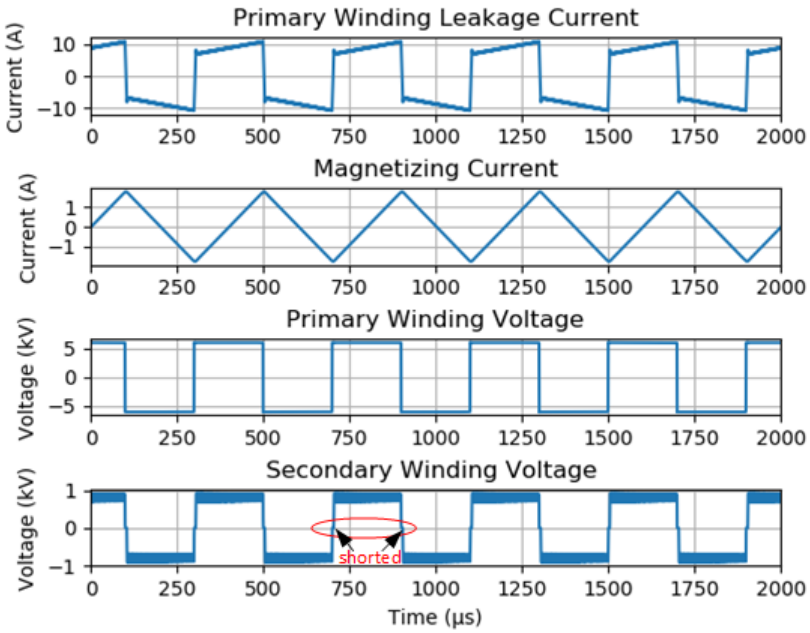

Figure 6.4. Transformer waveforms for the buck-derived and $\phi = 0°$

When the voltage across the primary is 6kV, the primary winding leakage inductor current charges whereas it discharges when the voltage of the primary winding is -6kV. During the transitions from -6kV to 6kV and the opposite, there is a small time interval (around 4μs) where the secondary winding is short circuited, a fact that proves the theory of Chapter 4. This happens because the primary winding leakage inductor suddenly charges up to the DC-link voltage value and therefore the secondary winding has to become short-circuited to deliver the amount of current. The input power is zero during this time period. Moreover, the magnetizing current, presents fairly small peak values (around 1.75A) and a mean value of around zero amperes. Finally, the effect of the parasitic capacitances of the transformer windings is clearly observed on the secondary winding voltage which presents heavy oscillations. That is why, careful design of the transformer parasitic capacitances should be considered.

Finally, the input and output power along with the output inductor current and the output voltage are presented in Figure 6.5. The mean input and output powers are 51.014kW and 50.404kW resulting to an overall efficiency of 98.8%. The core losses of the transformer are not taken into account in the simulation model, so one should expect a lower efficiency. The output voltage ripple is around 2% while the inductor current ripple is 1.81%. Both values satisfy the requirements set in Chapter 5 for the ripple levels. The output voltage does not reach exactly the nominal output voltage of 800V as the converter operates in an open loop fashion.

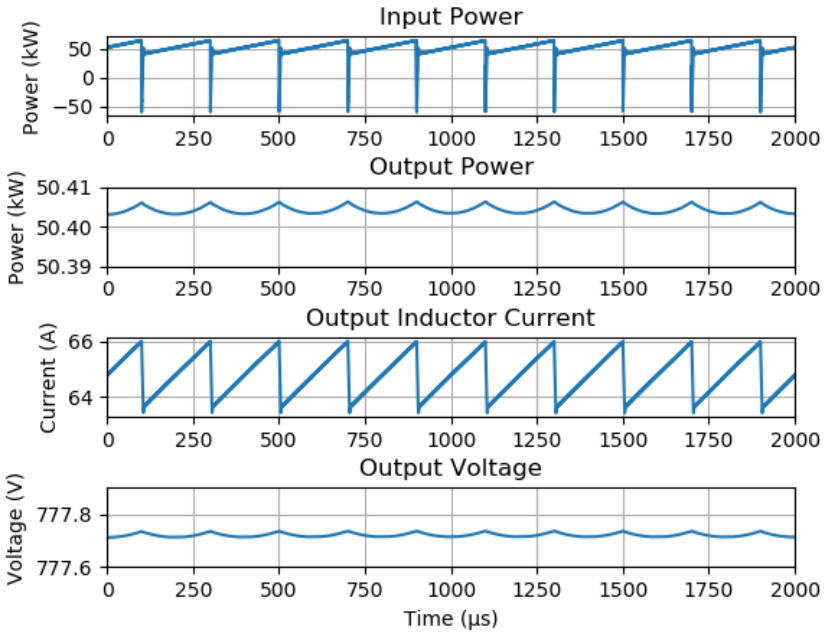

Figure 6.5. Waveforms for the buck-derived and $\phi = 0°$

Afterwards, the phase relationship between the legs was set to $\phi = 90°$ resulting to a leading and lagging leg. In Figure 6.6, the 90 degrees phase shift and its effect on the transformer windings voltage is depicted. A zero-voltage level is added on the windings voltage where zero power delivery occurs during that interval.

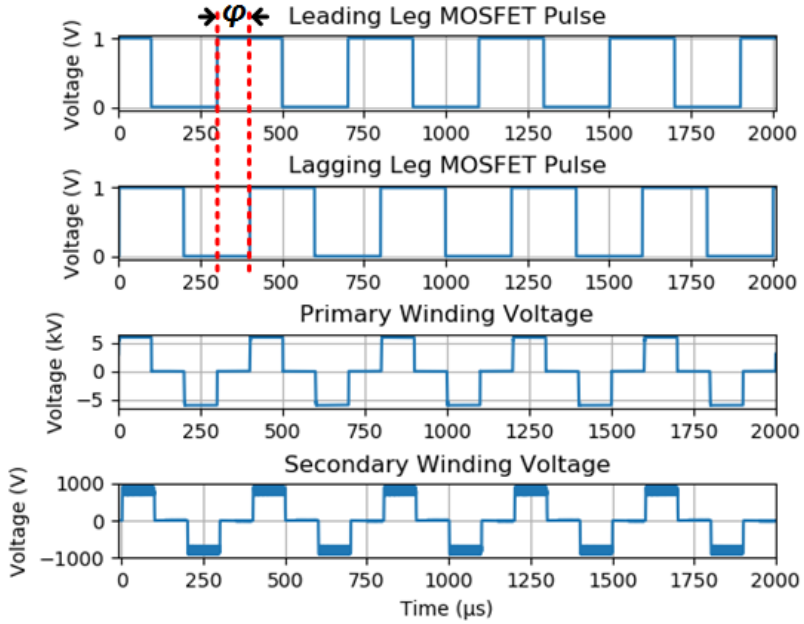

Figure 6.6. Phase shift effect for the buck-derived and $\phi = 90°$

The converter presents an average input power of 13.063kW and an output power equal to 12.832kW resulting to a total efficiency of 98.2%. In addition, the output voltage ripple lie into the acceptable limits whereas the output inductor current ripple reaches 40 percent a value that it is in the upper acceptable bound. So, careful consideration should be made about the inductor ripple at lower voltage levels.

Finally, in Figure 6.7, one period of operation is shown for the case that $\phi = 90°$. When the primary winding voltage equals to the DC-link voltage (6kV), the current through the primary winding leakage inductor charges while during the zero voltage level time period, the leakage inductor can either charge or discharge. A primary winding voltage of minus the DC-link voltage, causes the current through the leakage inductor to discharge. Also, during the primary winding voltage transitions between the different levels, high voltages appear across the leakage inductor as the leakage inductance experiences the DC link voltage across it, as it is shown inside the red ellipses of Figure 6.7. The rough oscillations of the primary winding leakage voltage when the voltage across the primary is either plus or minus the DC-link voltage, come from the primary winding parasitic capacitance which forms essentially a resonant circuit along with the leakage inductance.

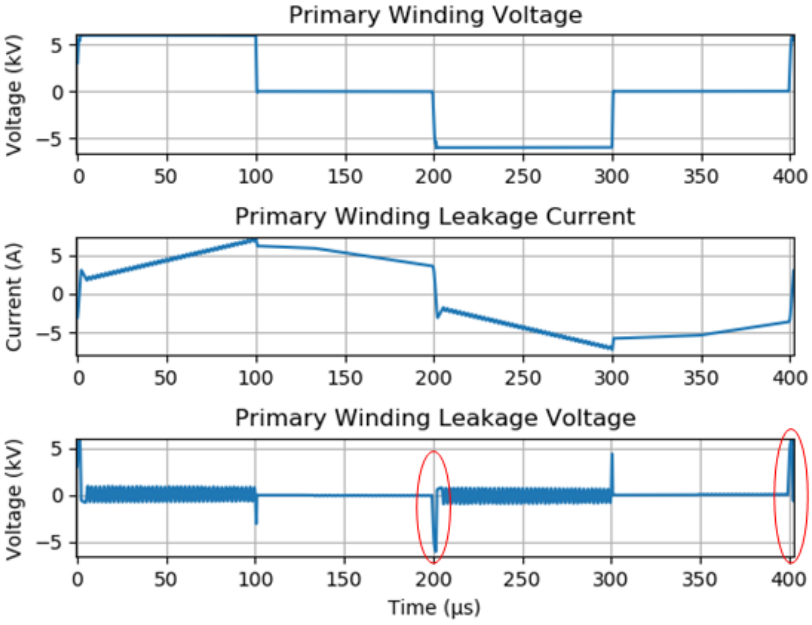

Figure 6.7. Primary winding leakage inductor performance during one switching period for the buck-derived and $\phi = 90°$

6.2 Single Active Bridge Converter Simulation

Afterwards, the single active bridge was simulated. Its schematic is imaged in Figure 6.8. The output filter inductor and the snubber circuit is missing now. This converter also operates under soft switching conditions presenting a high efficiency at high power levels.

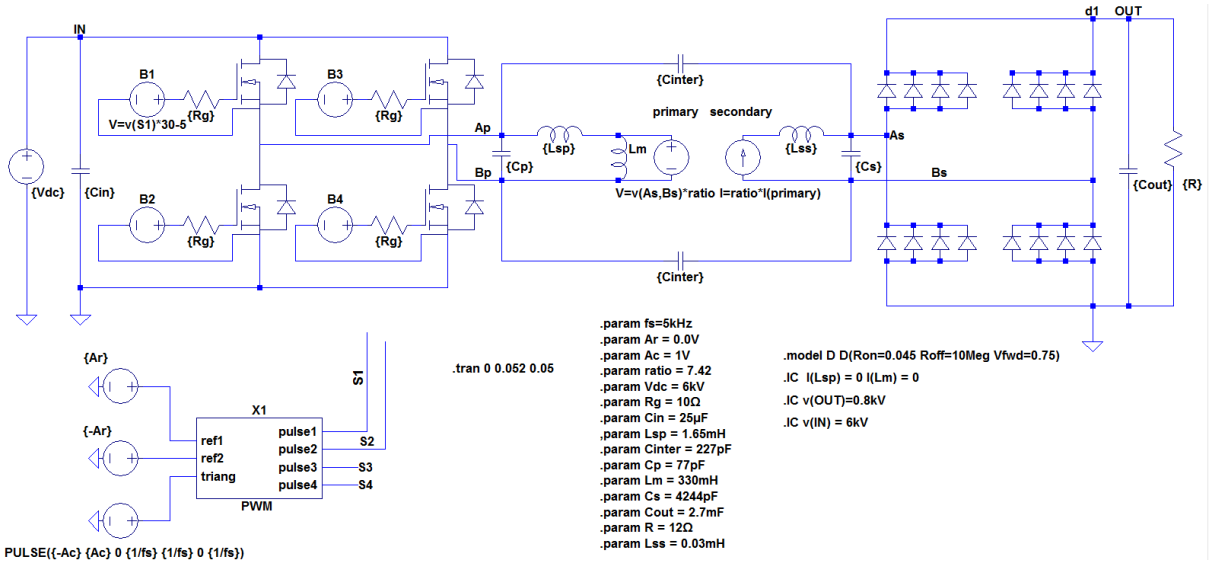

Figure 6.8. Simulation schematic of the single active bridge topology

The switches waveforms, namely the MOSFET current, the diode current and the voltage across both of them, are shown for the case that $\phi = 0°$. Maximum output power occurs, and therefore the stress on the semiconductors can be observed.

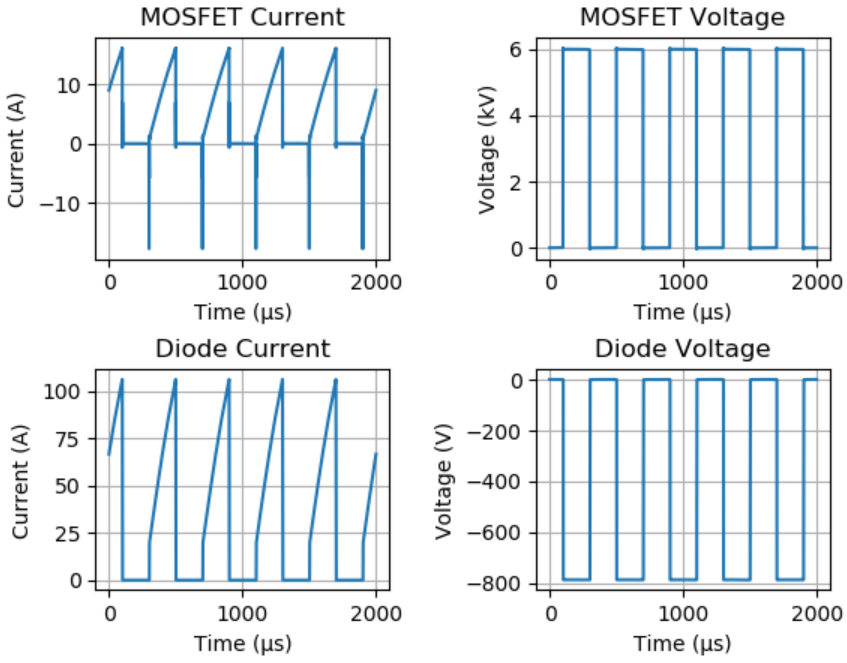

Figure 6.9. Waveforms of the switches for the SAB and $\phi = 0°$

By comparing the Figures 6.2 and 6.9, one can observe higher current stress for both the diodes and the MOSFET. Especially for the MOSFET, the maximum current reaches around 16A, a value which is pretty close to the rated 17A of the examined MOSFET. Regarding the total diode current for an arm, it increases around 40%. On the other hand, the heavy oscillations on the diode voltage during the off state are not present in the SAB indicating that the snubber circuit is not required for this converter.

In addition, in Figure 6.10, the input and output power along with the primary winding leakage current and output voltage are illustrated. The output is slightly higher than the buck-derived topology by around 1kW, but this does not affect the general evaluation. Consequently, it becomes noticeable that the mean output power is 51.555kW while the mean input power equals to 51.906kW resulting to a total efficiency of 99.3%. The output voltage ripple is very low, whereas the primary winding leakage current 9.88A RMS, a value which is out of the limits of the transformer design (8.33A RMS).

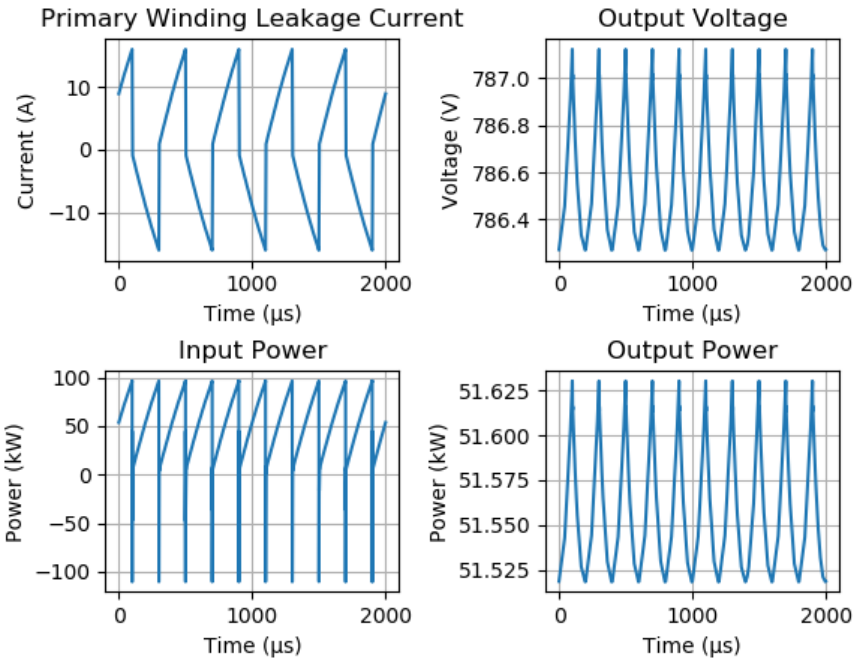

Figure 6.10. Waveforms for the SAB and $\phi = 0°$

Finally, the phase shift is set to $\phi = 90°$ as before. The results of some important waveforms are presented in Figure 6.11. It is clearly observed that the primary winding leakage current is forced to lie into the discontinuous conduction mode (DCM). Furthermore, the secondary winding voltage experiences severe ringing conditions during the primary winding voltage abrupt transitions. This is a direct consequence of the high secondary winding parasitic capacitance. Another interesting observation, is that the output voltage only dropped 50V approximately, comparing to the $\phi = 0°$ case. In fact, in order to reach an output power equal to the one that we had in the buck-derived for $\phi = 90°$, the phase shift should be around $\phi = 160°$. This means, that the primary winding leakage inductor becomes even more discontinuous and it presents an RMS current value of around 12A, namely 44% higher than the rated. Hence, the control of the output power in a wide operating range

becomes difficult in this topology. Moreover, the efficiency drops to 88%.

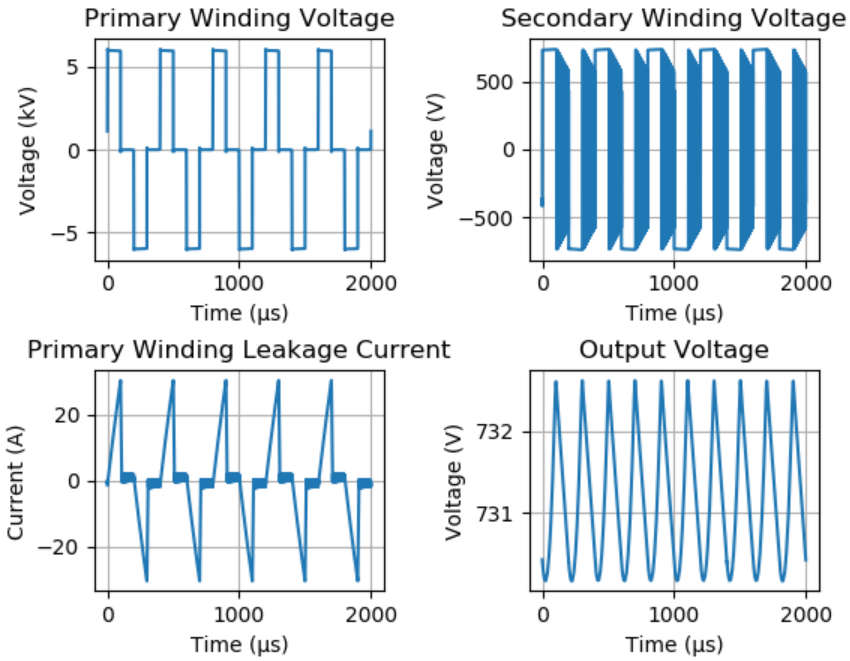

Figure 6.11. Waveforms for the SAB and $\phi = 90°$

6.3 Conclusion

In this chapter, the simulation results for the two candidate topologies were presented in order to identify the advantages and disadvantages of both topologies and evaluate them. It is more reasonable to collect all the information acquired above, in a compact form and that is what is done in Table 6.2. On the left column, some indices are set to assess the two topologies. In the middle and the right column, the assessment of the buck-derived and the single active bridge based on these indices is made. Given the requirements that were set by the Medium Voltage research team, namely the scalability, the control capability of the output voltage in a wide range, the stress on the 10kV SiC MOSFETS and the high efficiency of the proposed converter, the buck-derived topology is considered as suitable. In the next chapter, the setup of the phase shift ZVS buck-derived converter will be presented and some experiments will be made. Finally, through the simulations, the importance of a good design of the medium frequency transformer was highlighted as the parasitic capacitances and inductances of the transformer caused some resonance problems.

Converter Type	Buck-derived	Single Active Bridge (SAB)
Efficiency	Much higher at light loads	Slightly higher at heavy loads
MOSFET current stress	• Low peak values; RMS inside the rated limits for $\phi = 0°$ • Lower peak values and RMS inside the rated limits for lower output voltages	• High peak values; RMS close to the rated limits for $\phi = 0°$ • Higher peak values and RMS out of the rated limits for lower output voltages
Output capacitor stress	Small RMS current value	Large RMS current value
Output voltage control capability	Easy to control and wide output voltage range operating in CCM	Difficult to control for low output voltages; heavy DCM conditions as ϕ rises
Output voltage ripple	Inside the acceptable limits	Inside the acceptable limits
DC Inductor Current ripple	Inside the acceptable limits at rated power; lies outside the limits at half of the rated output voltage	-
Transformer Performance	Harsh oscillations of the secondary winding voltage during the power delivery intervals	Heavy resonance oscillations of the secondary winding during the transition states of the voltage
Snubber Protection	Present	Absent

Table 6.2. Comparison of the simulation results between the buck-derived and SAB converter

Experimental Setup 7

In this section, the experimental setup of the phase shift buck-derived converter that was built in the Power Electronics Systems Laboratory of AAU will be discussed and shown through pictures. Moreover, some experimental data will be demonstrated and compared with the simulated.

7.1 Description of the setup

A principal diagram of the whole setup is pictured in Figure 7.1. The notation C_1 and C_2 stands for the primary winding leakage and the output inductor current measurements respectively, whereas v_p, v_s, v denote the primary winding, secondary winding and output voltage measurements respectively. Also, $OSC1, OSC2$ in the figure, means "Oscilloscope 1" and "Oscilloscope 2" respectively. The principal diagram is supported by some more explanatory images of the actual setup which are shown in Figures 7.2 to 7.6.

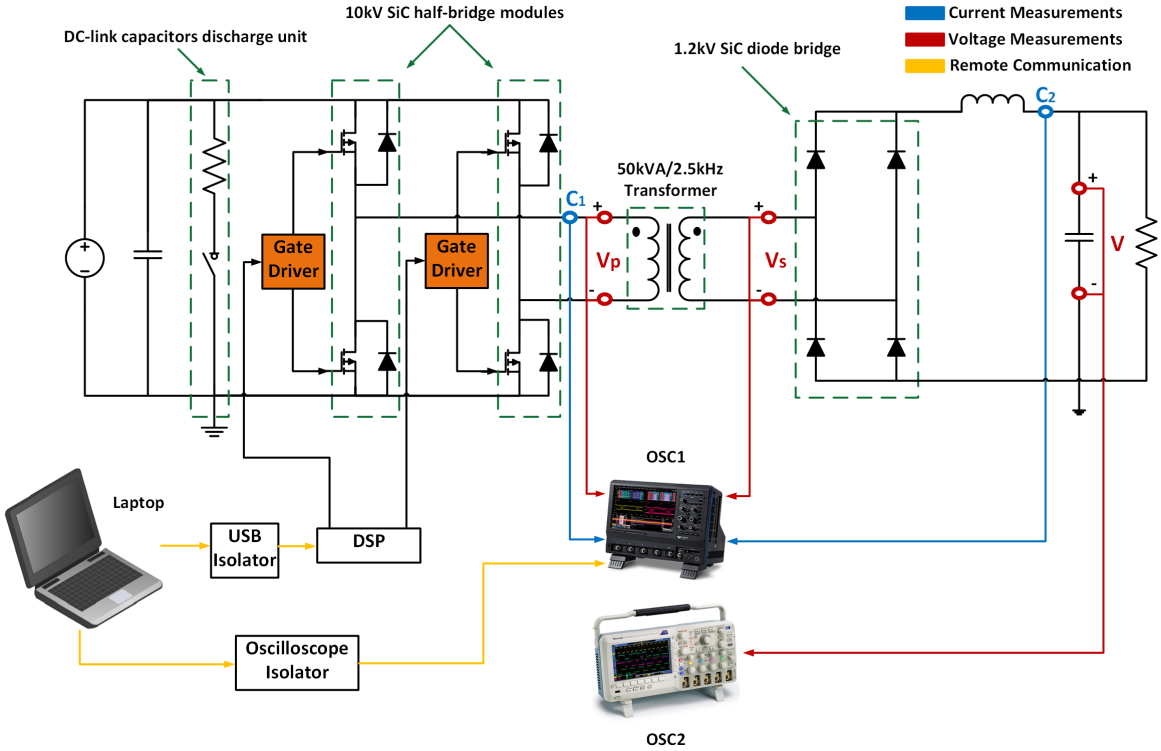

Figure 7.1. Principal diagram of the experimental setup

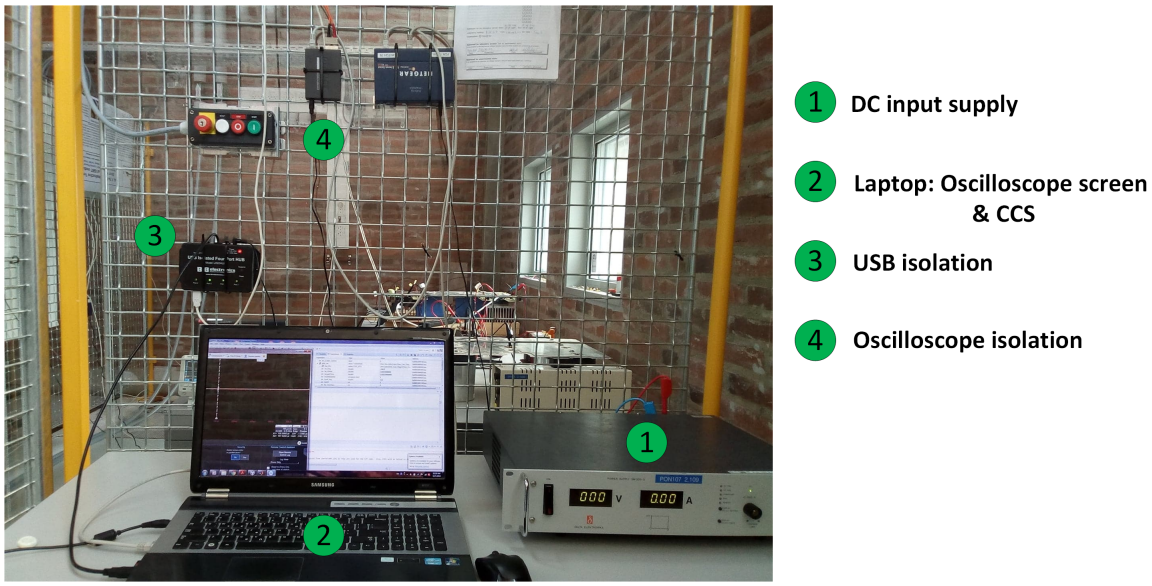

Figure 7.2. Image of the setup outside the cage

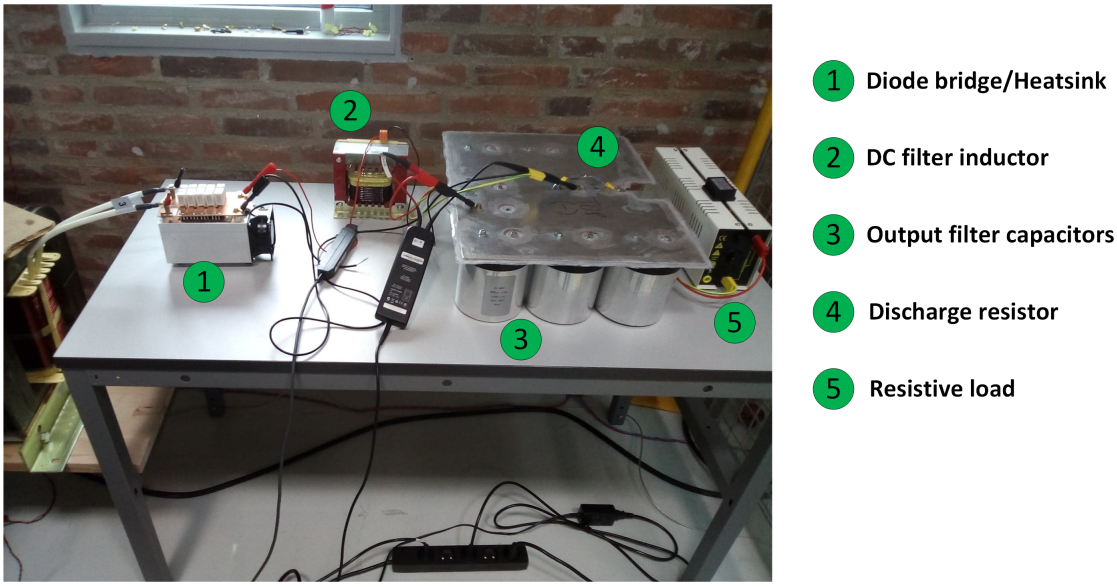

Figure 7.3. Image of the low voltage side of the setup

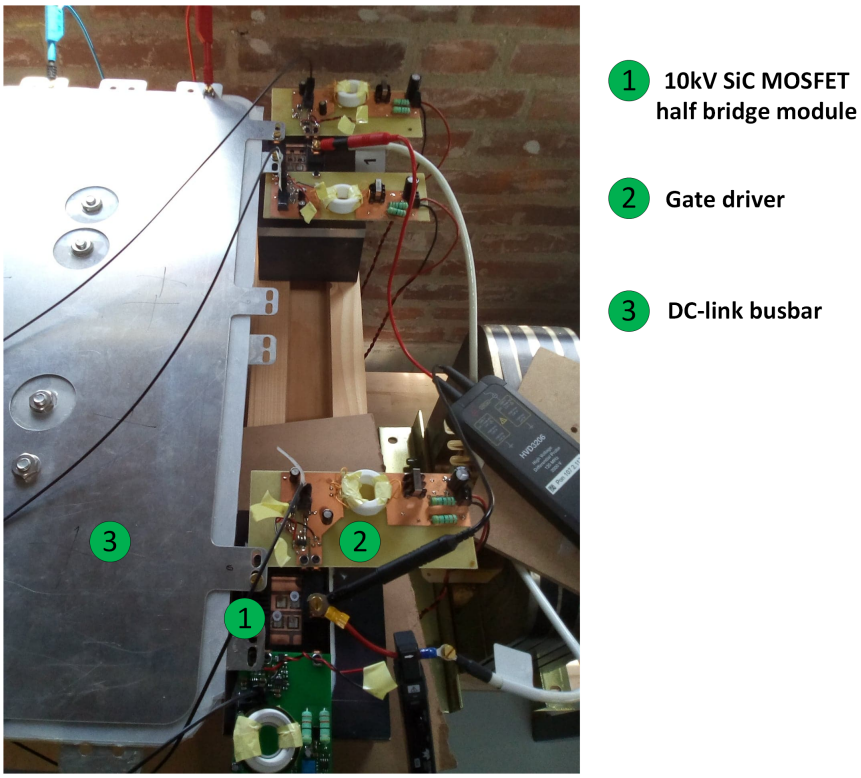

Figure 7.4. Image of the medium voltage side (a)

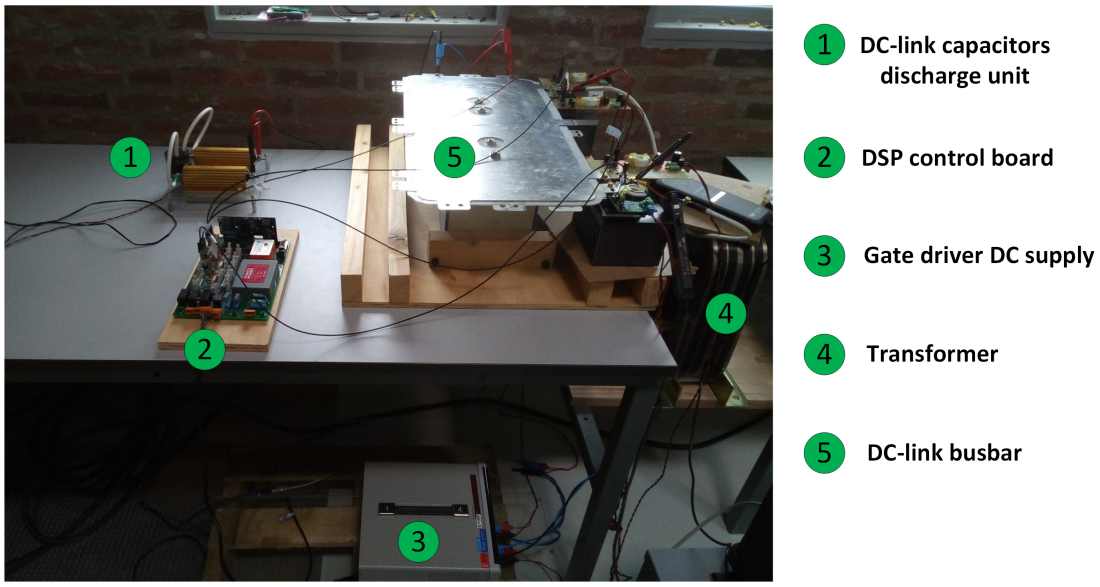

Figure 7.5. Image of the medium voltage side (b)

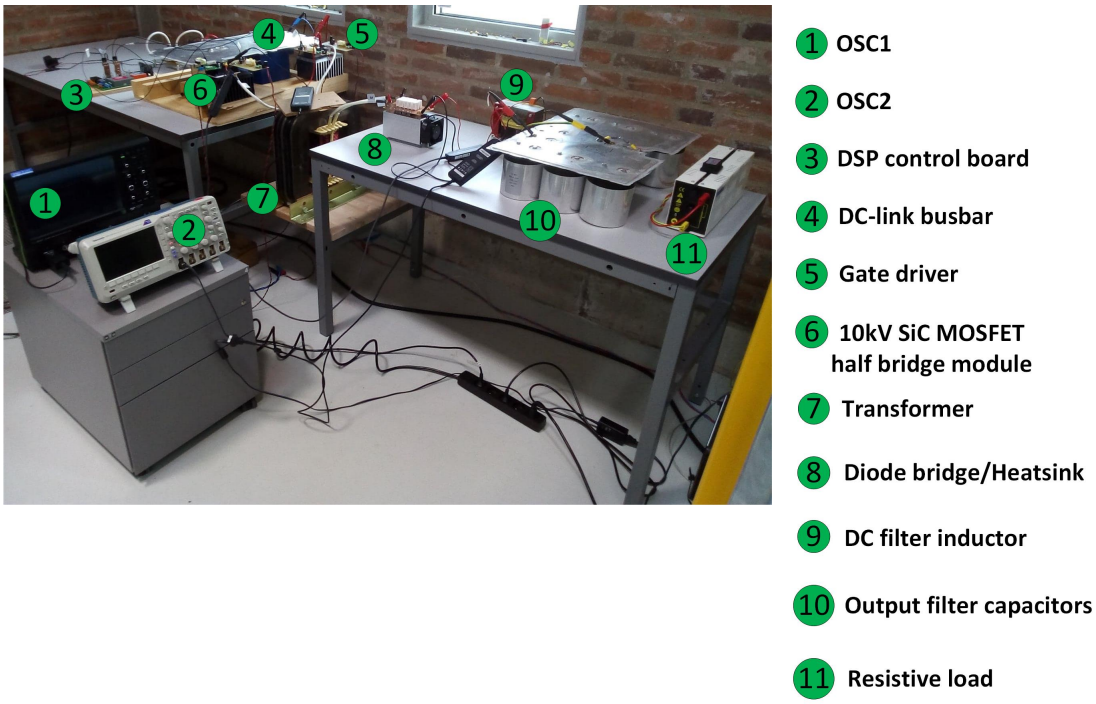

Figure 7.6. Image of the setup inside the cage

7.2 Experimental results

Given that there was no previous experience with the 10kV SiC power modules running on a real DC-DC converter situation, some intermediate steps were followed before connecting a load in the output. First of all, the gate drivers must output a proper voltage of +20V/-5V during the turn on and turn off respectively and this is the first thing that was examined. The deadtime interval along with the phase shift between the legs should be validated and this is what is illustrated in Figures 7.7 and 7.8. The deadtime interval is slightly less than $2\mu s$ as the turn on and turn off can not be done instantly and there is a delay. Hence, The power modules switch well, with 0.5 duty cycle and phase shift of 90 degrees and the next step could be followed.

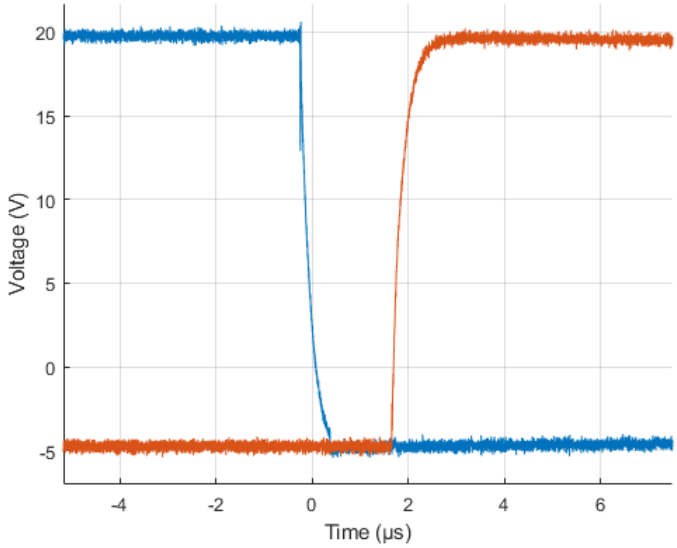

Figure 7.7. Gate to source voltage deadtime demonstration

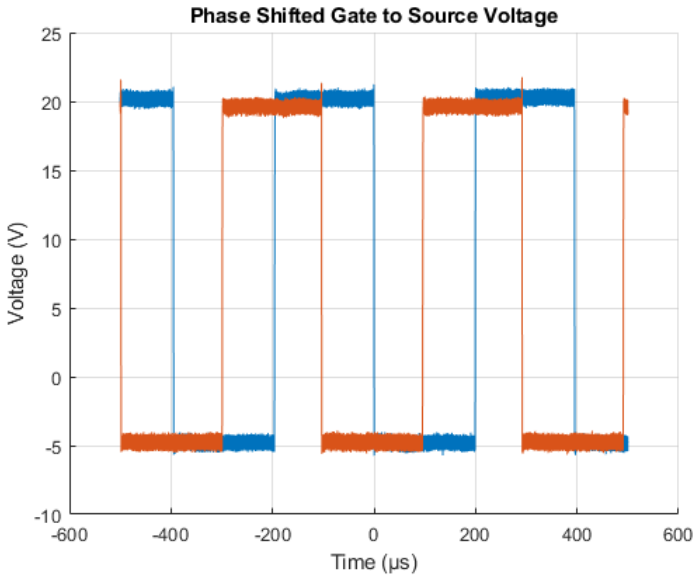

Figure 7.8. Phase shifted gate to source voltage

Afterwards, the system ran with the secondary winding of the transformer left open. This is done in order to test the behaviour of the transformer, namely the voltage ratio between the windings as well as the parasitic effects of the windings capacitances. In Figure 7.9 the results of the windings voltage are depicted. A 50V DC voltage is applied to the primary. A 14% percent overshoot on the primary winding is observed whereas on the secondary winding huge voltage spikes (at most 6 times high) appeared. The most reasonable explanation is that this effect comes from the parasitic secondary winding capacitance.

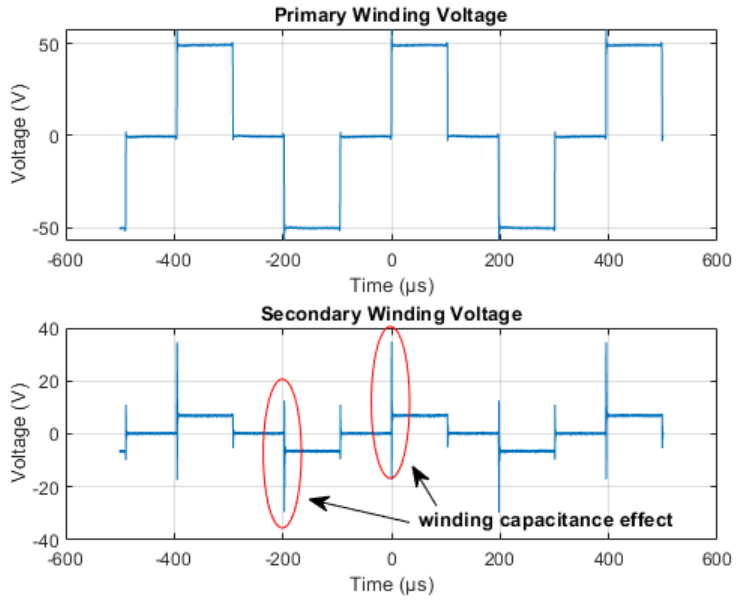

Figure 7.9. Voltage of the windings with the secondary left open

Next, the rectifier stage and the LC filter were connected. By doing this, the diode bridge along with the snubber circuit and the LC filter action will be evaluated. In Figure 7.10 the primary winding along with the secondary winding voltages are presented for an applied input DC voltage of 100V. By comparing Figure 7.10 and Figure 7.9 we can see that the snubber circuit achieves to diminish the big voltage spikes of the secondary, but then some resonance issues appeared during the transition of the secondary winding to zero volts. However, it was estimated that this resonance will disappear when the resistive load will be connected in the output. Later on, it will be shown that indeed this happened.

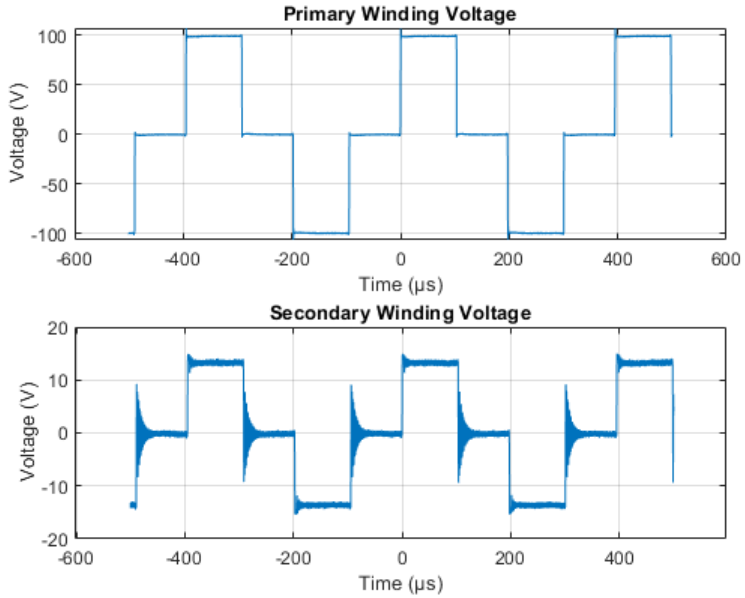

Figure 7.10. Windings voltage with the rectifier and filter connected under 100V input voltage

After finishing these intermediate tests for evaluating the operation of the components, an output resistive load of 11.8Ω was connected to the output. The current limit of the DC supply was set to 0.1A and the input voltage increases to 240V. In Figures 7.11 and 7.12 the experimental along with the simulated results for the voltage across the windings are imaged for the same load and input voltage. Moreover, the current through the primary winding leakage inductor and the output inductor, is illustrated in Figures 7.13 and 7.14 from the experiment and simulation respectively.

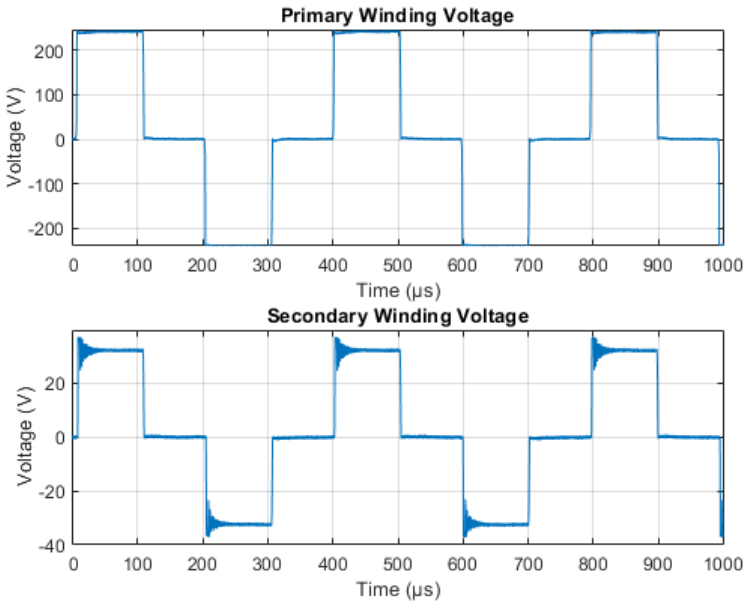

Figure 7.11. Experimental voltage waveforms of the windings at 240V input voltage

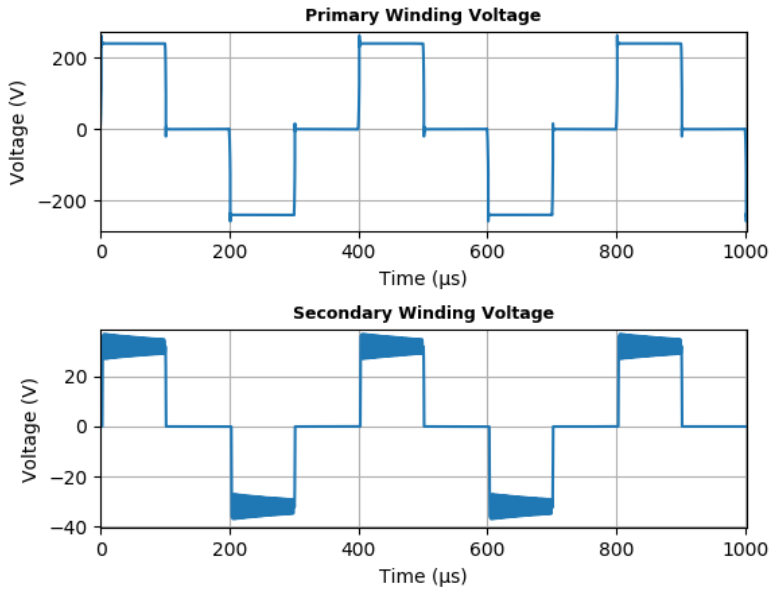

Figure 7.12. Simulated voltage waveforms at 240V input voltage

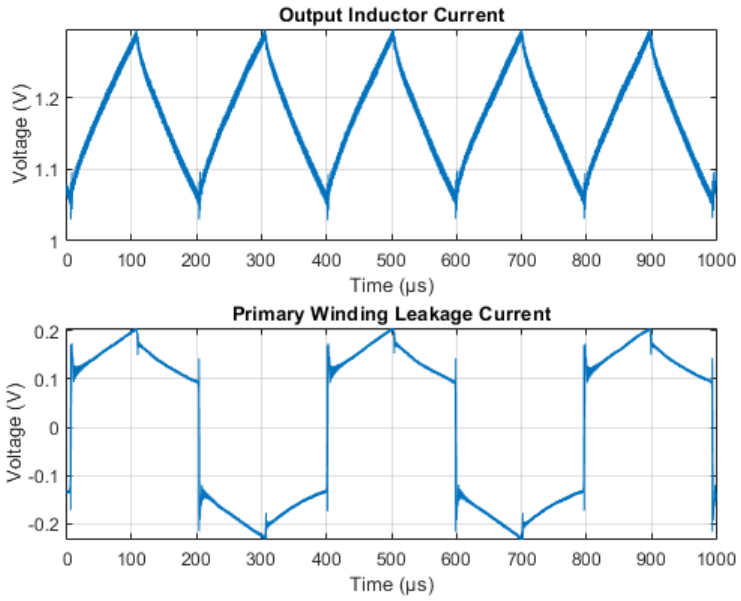

Figure 7.13. Experimental current waveforms at 240V input voltage

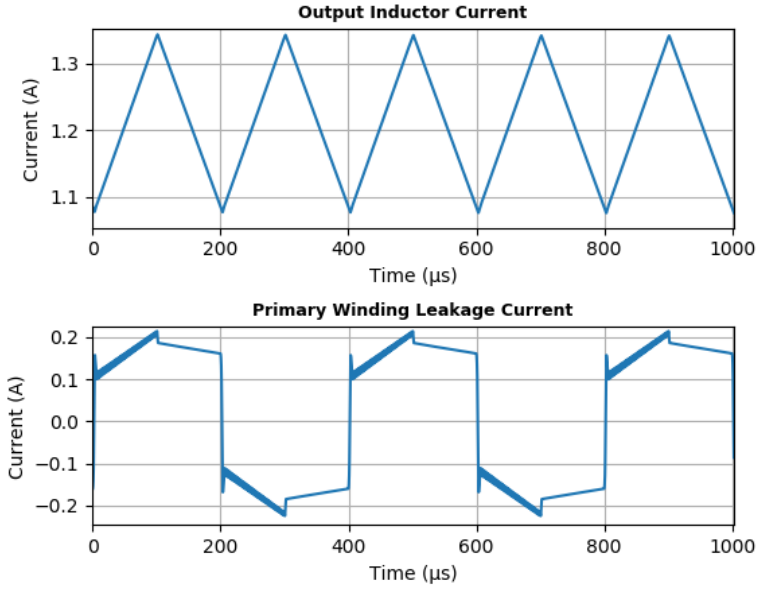

Figure 7.14. Simulated current waveforms at 240V input voltage

By observing the simulated and the experimental results, it is apparent that there is a quite good consistency between them. Regarding the voltages of the windings, the big difference is that the simulated secondary winding voltage presents more severe oscillations compared to the experimental. This is an indication that the parasitic capacitances may present lower values in reality at this voltage level and they were probably overestimated inside the simulation model. In addition, only 5V (15%) overshoot is noticed on the experimental secondary winding voltage and 0.025ms are required for the ringing to be vanished during the voltage transition. The output voltage of the converter was measured at 12.4V, while

the simulated was found to be 14.2V.

7.3 Conclusion

In this chapter, the full setup of the phase shift buck-derived converter that was built in the laboratory was presented through explanatory images. Several experiments were conducted, which verified: the shape of the waveforms that was predicted in theory, the accuracy of the simulation models and the proper function of the individual hardware components.

Conclusion 8

In the beginning of the project an extensive research on the topic was conducted, highlighting the motivation around DC systems and technology as well as the importance of the medium voltage/high power converters on a future conceivable DC electric grid. The focus was on medium voltage DC-DC converters and some potential application areas of such converters were presented. Moreover, several challenges for implementing a DC grid were underlined and in the end, the potential benefits of a medium voltage DC collector grid over a medium voltage AC collector grid, which exists today, were stated.

Then, the state of the art technology that helps towards the development of a medium voltage DC-DC converter was introduced. Additionally, different medium voltage DC-DC topologies were shown. Limitations and challenges for developing medium voltage converters were also discussed.

Through the literature investigation, two medium voltage DC-DC converters were chosen to be compared in case of an energy storage application, which are the phase shift buck-derived and the single active bridge converter. The nominal ratings were 50kW output power, 6kV input voltage and 800V output voltage. Special requirements for the proposed converter, were the scalability and the high efficiency. The main hypotheses of the project were, first of all, that a medium voltage DC-DC converter based on the 10kV SiC MOSFETS that were designed and packaged at Aalborg University, is feasible to be built and second of all, that it can be connected to a medium voltage DC grid for energy storage purposes.

Afterwards, the converters were analyzed in theory, through mathematical equations and equivalent AC circuits in order to predict and understand their operation. In addition, the phase shift PWM principle and how this scheme helps the soft switching conditions to be achieved was explained.

Next, the hardware design of the converters was presented. Each part of the final setup was analyzed in detail and the design process was extensively revealed. The exact design parameters were later used in the simulation models.

The next step was the simulation of the converters, where the main comparison between the candidate topologies was made. The transformer that was used for stepping down the voltage, was modeled to contain its parasitic elements for a more realistic simulation model. Moreover, the SiC MOSFET includes all the parasitics of the package for a more accurate evaluation. Although the single active bridge presented 0.5% higher efficiency under nominal power, the current stress across the 10kV SiC modules was outside of the safe operating area. Furthermore, the control capability of the output power is limited on

the single active bridge. Therefore, given the requirements and a fair comparison based on specific indices, the phase shift buck-derived topology was chosen to be built in the Power Electronics Systems Laboratory of Aalborg University.

Several experiments were made in the laboratory under low voltage levels and the experimental results were compared to the simulated data, showing a quite good consistency between the two and proving the proper operation of each part of the converter.

Finally, although the medium voltage levels were not reached in the experiments, for testing the power modules in conditions close to the breakdown voltage, the first important and fundamental step towards that direction was made through this master thesis. A real DC-DC converter, based on the 10kV SiC power modules that were designed at AAU, was built in the Power Electronics Systems Laboratory. By making some modifications on the hardware of the setup, the voltage rise can be easily achieved in a next stage.

Future Work 9

Through the discussion of the previous chapter the important conclusions have been extracted. However, many things can be considered as part of the future work:

- Given that the system operates well under low voltage levels, the next step is to go to the medium voltage level to test the SiC MOSFET power modules close to the breakdown voltage. In order to do this, special protection measurements have to be taken into account. Overcurrent protection needs to be incorporated into the hardware setup. If an overcurrent condition is detected, a command to the DSP to deactivate the MOSFET pulses must be given.
- When the system is safe to be operated at medium voltage level, efficiency extraction at many working points could be made and be compared with the simulated efficiency.
- A part that needs also to be addressed, are the copper losses of the transformer which are not discussed. A simulation model for the transformer copper losses could be developed for a more accurate estimation of the power losses of the buck-derived converter.
- Closed loop control could also be implemented for obtaining the maximum efficiency for any operating point. Typical proportional-integral current closed loop control could be an option.
- As the soft-switching conditions tend to be lost under light loads, the investigation of the soft-switching boundaries would be interesting for further exploration.
- More effort should be put on the modeling of the transformer parasitics, as they depend on the current that it flows through it.
- A battery load should also be realized in the future, for controlling the charging or the discharging.
- Given that bi-directional power flow is almost mandatory for the energy storage systems, transistors could also be considered for the low voltage side instead of diodes.

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Transformer Models A

Through the report, different transformer models are used for either modeling or simulation purposes. The first model is depicted in Figure A.1 and it is the physical model of the transformer.

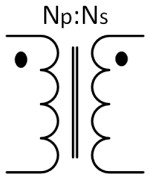

Figure A.1. Physical model of the transformer

This notation implies that the transformer is not ideal and its equivalent circuit is illustrated in Figure A.2. It contains the leakage inductances of the primary and secondary, $L_{\sigma p}$ and $L_{\sigma s}$ along with their resistances $R_{\sigma p}$, $R_{\sigma s}$ respectively. Also, the magnetization flux is created via the magnetization inductance L_m which is placed across the primary winding. The parasitic distributed capacitances of the windings C_p, C_s along with the inter-winding capacitance C_{inter} are present and they are of high importance as they heavily affect the converters performance. The magnetizing resistor which is placed in parallel with the magnetizing inductance is discarded. Finally, the symbol n, stands for the ratio of the transformer, namely $n = N_s/N_p$, where N_p and N_s denote the number of turns of the primary and secondary winding respectively. This model is used for the simulations of the converters.

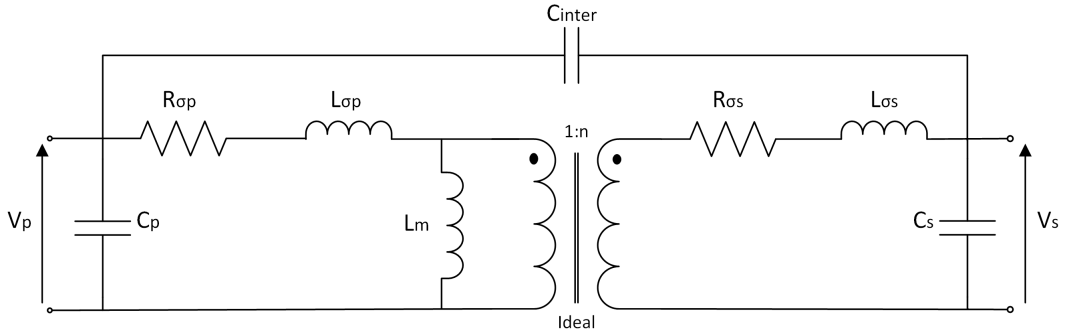

Figure A.2. Equivalent circuit of the physical model of the transformer

A simplified version of the previous model is shown in Figure A.3. Here, the magnetising inductance along with the ideal version of the transformer form the equivalent circuit,

namely the parasitics of the transformer are discarded. This circuit is used for the mathematical modeling of the buck-derived topology.

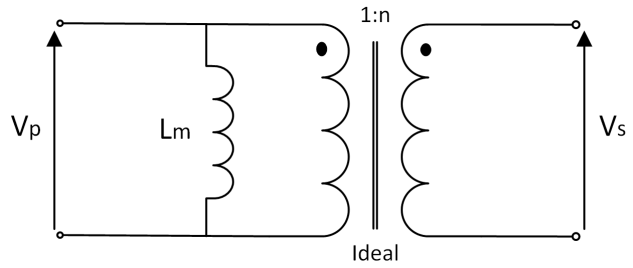

Figure A.3. Transformer equivalent circuit for modeling purposes

Phase Shift Pulse Width Modulation

B

In order to achieve soft switching conditions for the converters of this project, the phase shift PWM scheme is developed. Here, it is shown how this is achieved in LTSpice for a 90 degrees phase shift ($\phi = 90°$) and 0.5 duty cycle at a switching period of $T_s = 400\mu s$. The duty cycle always remains constant at 50%. Afterwards, the implementation of a 2μs deadtime interval is presented.

Whenever the full bridge inverter is appeared in this project, the notation of the Figure B.1 is assumed for the MOSFETS. Therefore $S1, S2$ form the leading leg and $S3, S4$ the lagging one.

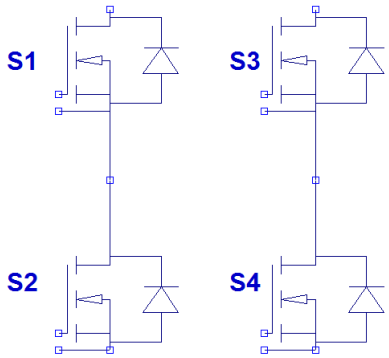

Figure B.1. Notation of the MOSFETS on the simulation schematics

In Figure B.2 the PWM scheme is shown and it works as follows: First of all, a sawtooth waveform (tri) from zero to one every 400μs is created. Then, it is compared with a constant 0.5 reference value (ref). When ref is greater than tri the $S1$ pulse is on, while it is off when the condition does not hold. For the generation of the $S4$ pulse, another sawtooth ($tri\ shifted$) from zero to 0.75 is produced. This waveform stops at $\frac{3T_s}{4}$ and between the interval $\frac{3T_s}{4}$ and T_s it equals to zero. Afterwards, it is compared with a constant reference value which is the half of the ref value, namely 0.25. When 0.25 is less than $tri\ shifted$, $S4$ is on and off on the opposite case. Of course, the same phase shift is applied to $S2$ and $S3$. Finally, every value of the phase shift ϕ can be obtained, by adjusting the maximum value of the $tri\ shifted$ and the reference value of the $B1$ source

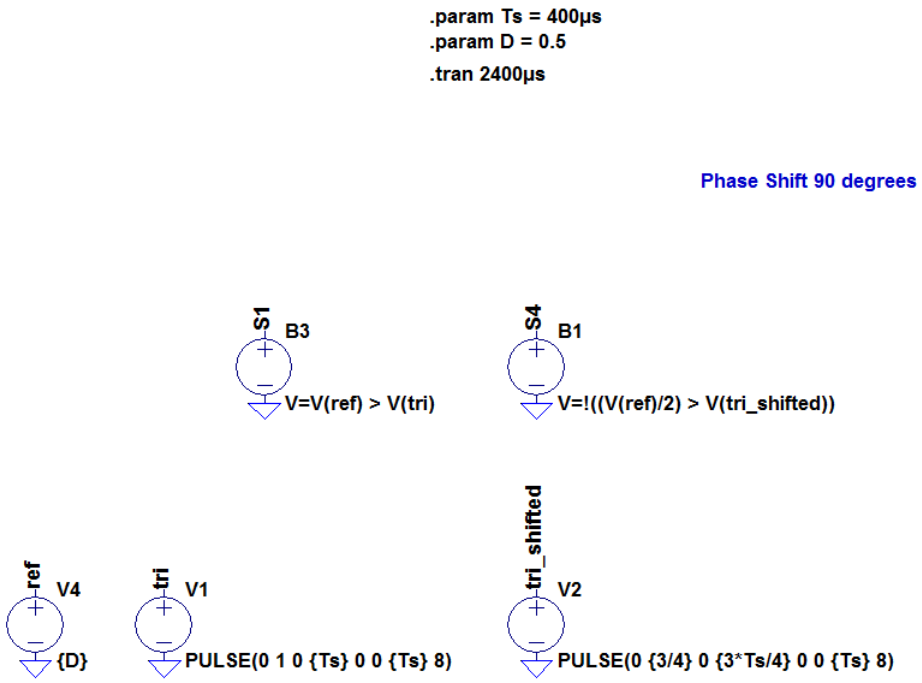

Figure B.2. Phase shift PWM implementation in LTSpice

After producing the appropriate phase shift, the deadtime interval is considered. In Figure B.3, the principal schematic of the deadtime implementation is illustrated. Here, $S1$ and $S2$ are the MOSFET pulses of the first leg and they constitute the inputs into the first Schmitt trigger. Later, through a RC circuit with a time constant of $2\mu s$ $S1$ is delayed during turn on. A diode in parallel is placed, which is on during the turn off transition of the pulse providing a current path during this short interval. This results to a delay during turn off too. $S2$ pulse follows the same concept, but it goes through the inverted output of the Schmitt trigger as the signals are complementary.

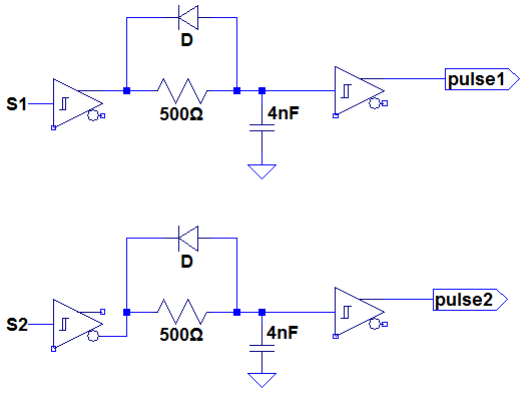

Figure B.3. Deadtime implementation in LTSpice

It is underlined that the previous figures were principal, presenting the main ideas to the reader of how deadtime and phase shift can be obtained for only a pair of pulses. In the real simulation models, the above considerations are combined for all the MOSFETS of the full bridge and the final signals are sent to their gates.