Application Study for a Modern Circuit Breaker

Project Report
PED4-1046

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STUDENT REPORT

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Application Study for a Modern Circuit Breaker

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Participant(s):
Víctor Aragón Caminero
Waqas Aslam Chema

Supervisor(s):
Stig Munk-Nielsen
Amin Hajizadeh
Anders Maarbjerg

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Abstract:

DC microgrids are getting more and more used to distribute energy in more efficient way. Nonetheless, the protection of DC circuits against current faults becomes challenging due to the absence of zero current cross. Typical current Solid State topologies present high on-state losses. Hence, The present master's thesis pursues the construction and experimental validation of a Solid State Circuit Breaker featuring a significant loss decrease in comparison with an IGBT breaker of similar power range. This Modern Circuit Breaker topology unites the strengths of different semiconductor devices in expense of augmenting its control complexity. Therefore, a simple control strategy is proposed.

Nomenclature

Abbreviations

CB	Circuit Breaker
DUT	Design Under Test
$EWEA$	European Wind Energy Association
FMS	Fast Mechanical Switch
HCB	Hybrid Circuit Breaker
$HVDC$	High Voltage Direct Current
$LVDC$	Low Voltage Direct Current
MCB	Mechanical Circuit Breaker
MOV	Metal Oxide Varistor
$MVDC$	Medium Voltage Direct Current
$nMOS$	N-Channel MOSFET
$pMOS$	P-Channel MOSFET
SAS	Semiconductor Accessory Switch
SCR	Silicon Control Rectifier
$SSCB$	Solid State Circuit Breaker
STS	Semiconductor Transfer Switch

Physical Magnitudes

η	Effeciency
$\eta_{IGBT_{OFF}}$	Effeciency When IGBT Off

$\eta_{IGBT_{ON}}$	Effeciency When IGBT On
D_Z	Zener Diode
I_A	Anode Current
I_D	Drain Current
I_{GT}	Maximum Triggering Current
I_G	Gate Current
P_b	Blocking Losses
P_c	Conduction Losses
P_{sw}	Switching Losses
$R_{DS_{ON}}$	On-State Resistance
R_f	Fault Resistor
R_{Goff}	Turn-off Gate Resistor
R_{Gon}	Turn-on Gate Resistor
R_G	Gate Resistor
R_L	Load Resistor
R_{PD}	Pull-down Resistor
r_T	Slope Resistance
T_A	Ambient Temperature
T_c	Case Temperature
T_j	Chip Temperature
T_s	Heat Sink Temperature
V_{CC}	Supply Voltage
V_{GT}	Maximum Triggering Voltage
V_T	Threshold Voltage

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Preface

Aalborg University, May 31, 2019

Author 1
<varago17@student.aau.dk>

Author 2
<wcheee17@student.aau.dk>

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Chapter 1

Introduction

The first chapter introduces DC grid as an alternative way of energy distribution and presents technical challenges when it comes to protection of DC power systems. The problem in this thesis is to develop an DC breaker able to overcome this obstacles. To begin with, existing solutions to the problem are examined by identifying their weaknesses and strengths. To conclude the chapter, three recent topologies featuring reduced on-state power losses are reviewed.

For the last decades, an ever-growing demand for cleaner and renewable energy [2] along with a growing usage of DC appliances [13] - e.g. computer, smart phone, smart TV, electric mobility - has triggered questions such as: Is the current electric distribution grid the optimal architecture for this new scenario?

A power loss study comparing an AC grid versus its DC equivalent is developed in [32]. The analysis finds that the DC distribution system improved in efficiency when the amount of DC loads surpassed the 20% in a mixed load system.

In the generation plane, e.g. Danish consumed electricity (Figure 1.2) means a 18% of the total energy production. In the hypothetical case that road transportation is substituted by electric mobility - performing double efficiency and consuming DC power - only half of its energy share would have to be covered by electric means. Figure 1.1 illustrates this idea.

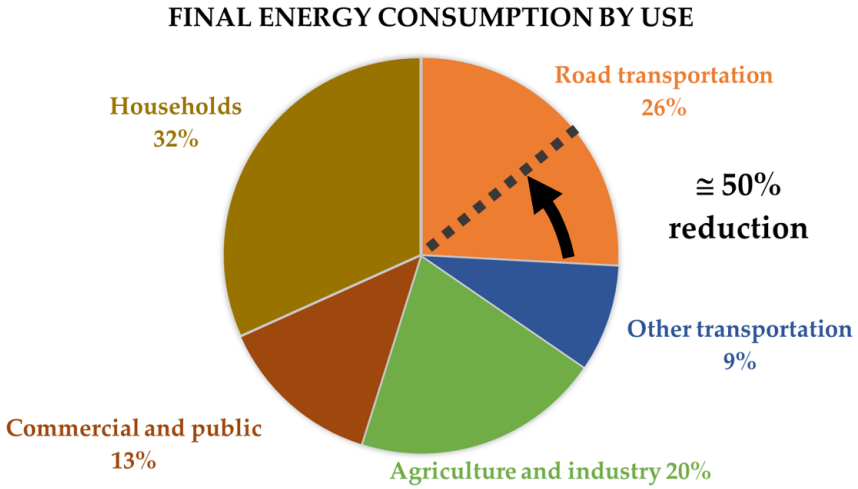

Figure 1.1: Energy consumption by use - Denmark 2016 [1]

Consequently, this situation would practically mean the end of the oil combustion - see Figure 1.2 - along with the associated benefit for health and slow down of the Global Warming. Nonetheless, electricity production must be doubled to meet the existent demand. All in all, the measure would suppose around a 13% energy saving for the danish case as observed in Figure 1.1.

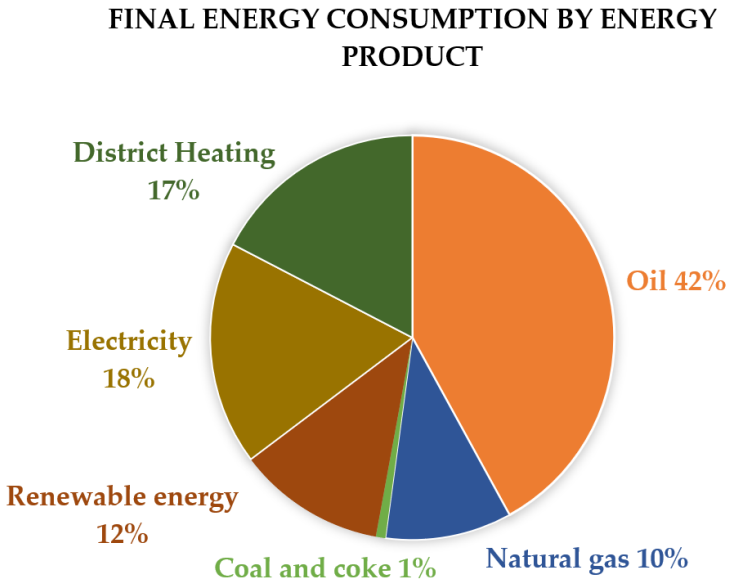

Figure 1.2: Energy consumption by energy product in Denmark in year 2016 [1]

Moreover, refinement and diversification in fuel cells, solar, and wind power are

also motivating this change since the first two directly produce DC voltage [32]. Figure 1.3 depicts the electricity production in Denmark. A clear growth is observed regarding renewable generation - light blue bars.

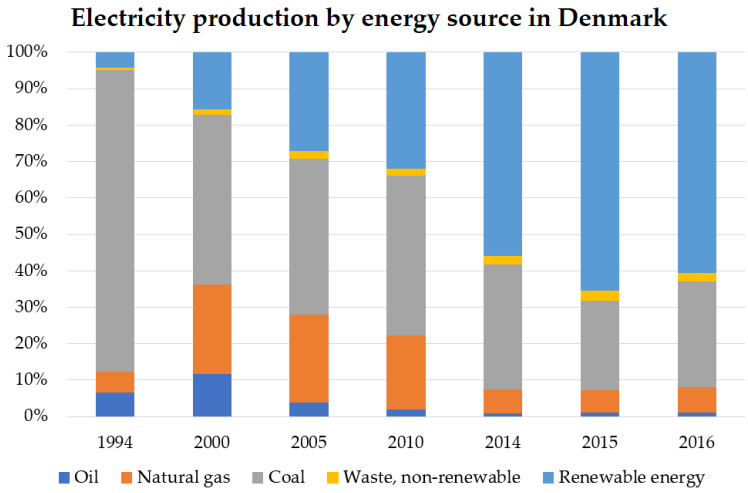

Figure 1.3: Evolution of the Danish electricity production [1]

Although producing AC, wind power needs to be converted to DC to untie the frequency of the generated electricity from the variable speed of the wind. Therefore, avoiding the conversion back to AC may mean savings. Furthermore, looking at next ten year road-map presented by the European Wind Energy Association (EWEA), the expansion of DC Grids due to offshore wind power is undeniable.

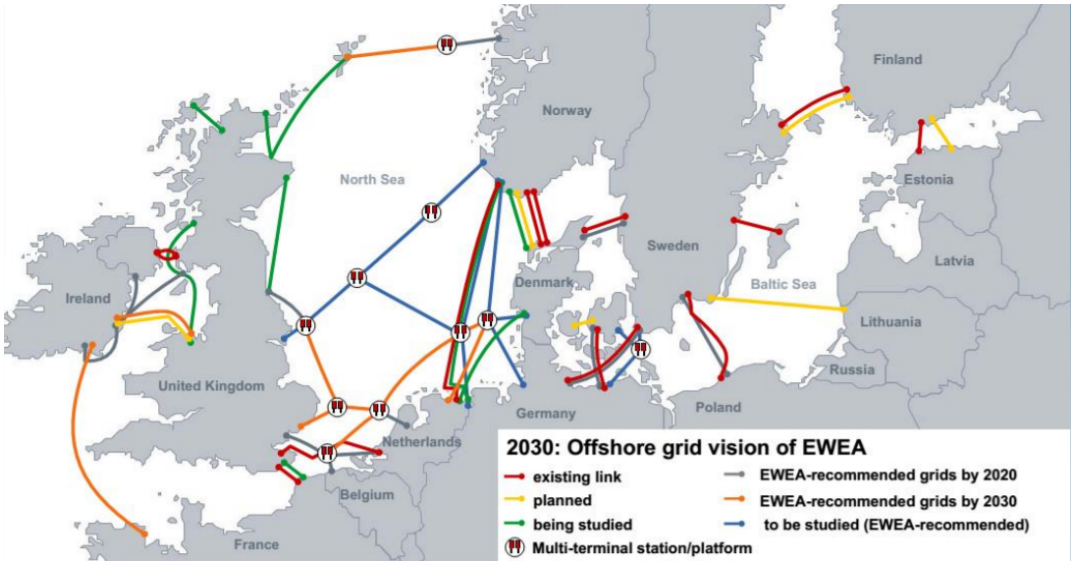

Figure 1.4: Offshore DC grid recommendation for 2030, North of Europe [12]

In the transportation level, HVDC lines are commonly used to efficiently connect distant regions presenting problems of frequency synchronization and also extend grids to islands and peninsulas through submarine cables when aerial lines are not feasible. Figure 1.5 shows HVDC panorama for Europe. The red links represent existing links, the green are under construction and the blue are planned links.

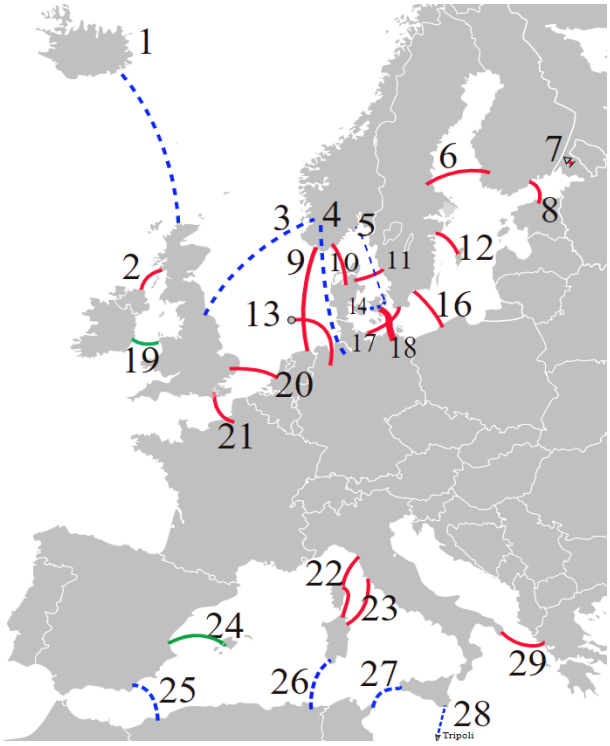

Figure 1.5: HVDC links. Red: existing, Green: under construction, Blue: planned. [31]

In the last situation, DC grid is used to avoid the underwater capacitive effect that increase the distributed power losses along the link [36], [3].
Regarding the end-use of electric consumption, approximately 40% - 50% of the global share corresponds to electric motors used in industrial production, household machinery, electric mobility [33]. In spite of using AC to work, modern drive systems begin to incorporate power electronic converters - which typical structure consists of DC-Link + Power inverter + Drive - to efficiently control the delivered torque and speed. Counting on a DC grid, a rectifier is saved once again.

An important challenge, however, stays latent when ensuring integrity and reliability of DC power systems. In contrast to AC, DC lacks zero current cross since they always provide their nominal constant voltage. This fact naturally induces a growing current under load increase or fault scenarios. Moreover, if a high loading condition and a small circuit inductance are met, large amplitude and sudden increase in the current will respectively take place [14], [15]. Two obvious but decisive parameters to have into account are therefore, the equivalent DC voltage and the capacity in case of energy storage systems. While the first one defines the magnitude of the fault current, the second one determines how long the fault will persist.

Nowadays, whenever there is need for efficient power conversion, electronic converters based on semiconductor devices are normally the way to go. Compared with mechanical parts - e.g. mechanical switches, cables or passive loads - semiconductor maximum ratings are much more unfavourable - e.g. 1.2 kV IGBT module conducting at room temperature can only withstand 3 times its nominal current during no more than 125 μs before the module fails. That is, the maximum admissible junction temperature is reached at that load level in that time frame [27],[6]. Therefore, any kind of solution able to detect and break a fault before the current is too big or the duration is too long will be a subject of study.

1.1 Micro-Grid Systems

The advantages of DC grid over AC grid are well established in previous section as well as, why the short-circuit protection of DC system is still a considerable challenge. The aim of this section is to provide a short overview on DC microgrid and the types of short-circuit faults that can occur in them. This will help to better devise a solution for the short-circuit fault condition.

A microgrid is a distributed power generation system having its own protective devices, energy sources, loads and energy storage capacity. It is capable of islanding and grid connection operations. They can be widely categorized into AC, DC and Hybrid AC-DC [8].

DC microgrids are further classified according to their rated voltage into high (HVDC), medium (MVDC) and low voltage (LVDC), respectively [25]. Table 1.1 illustrates the power, voltage and cable lengths for each of the voltage categories.

	HVDC	MVDC	LVDC
Power (MW)	>250	>250-0.1	< 0.1
Voltage (KV)	600-30	30-1.5	1.5-0.12
Cable length (Km)	>100	100-10	< 10

Table 1.1: Characteristics of DC microgrids according to voltage category [25]

DC microgrids may consist of wind energy systems, photovoltaic systems and energy storage systems. These different energy systems and loads can be connected in several configurations, e.g., signal bus topology, multi-bus topology and reconfigurable topology [9]. A typical signal bus DC microgrid is shown in Figure 1.6 [8].

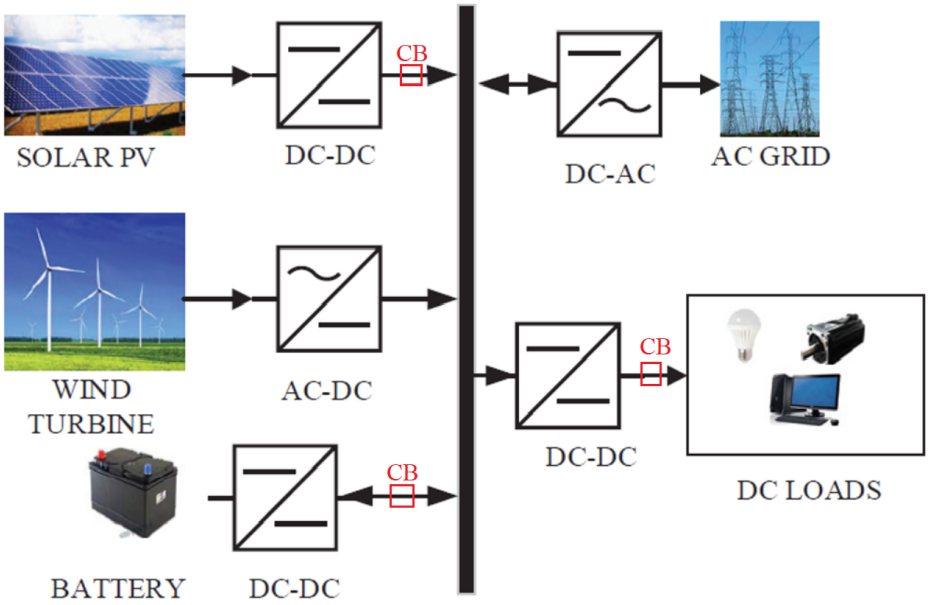

Figure 1.6: Signal bus microgrid with circuit breakers (CB) installed in each of its branches

1.2 Current Protections

Among an extend variety of protections found in the literature, two big families can be realized: one-time passive devices (**fuses**) and reusable active devices (**circuit breakers**).

1.2.1 Fuses

A fuse consists i.e. of a wire that melts when a specific current flow passes through it. It is comprised of an insulated body with an embedded wire and two terminals. They are made of high-conductivity materials e.g. copper, aluminum, etc. which confers them very low conduction losses. These and their reduced cost make them extensively used as current protection in electric circuits. However, when semiconductor protection is required, limited protection range is observed. As commented before, semiconductor survivability is highly limited by their maximum junction temperature which obliges to use ultra-fast fuses with body indentations (necks) to achieve a quick melting. Since the packages in these sort of fuses are reduced, the operating temperatures are elevated obliging to use higher melting point materials. This fact skews the protection capability to the high current or short-circuit range. [10].

1.2.2 Circuit Breakers

Circuit breakers (CB) present an extended protection range compared to fuses. That is, they protect in the overcurrent range, where fast fuses cannot. They typically consist of 3 parts: sensor, actuator and switch. Their operation is simple: if a fault is detected by the sensor, the switch is actuated to clear the fault current by opening the electric circuit, i.e. blocking the active source voltage. As opposed to fuses, circuit breakers can avoid parts replacements. Nonetheless, excepting normally-on JFETS and coupled-inductor topologies, they require external supplies for their operation and a reset mechanism to restart the conduction [26], [7].
Many circuit breakers are found in the literature according to design limitations, voltage class, excitation type and in summary, the specific application subject of current protection. In addition, two main strategies can be observed whether the focus is set on amplitude or time limiting the fault current [24].

1.3 Summary of Protections

Among the most cited, 3 families stand out: Electro-mechanical (EMCB), Solid State (SSCB) and Hybrid (HCB). Table 1.2 shows the main strengths and weaknesses for each of these current protection technologies.

Type	Technology	Advantages	Disadvantages
Only-use	Fuse	lowest losses	slow acting limited current range
Reusable	MCB	low losses, better current range	arcing, slow acting
	SSCB	fast acting, no arcing	high losses, high cost
	HCB	low losses, no arcing	slow acting, high cost

Table 1.2: Advantages and disadvantages of existing current protections

Reviewing the table above, fuses must be disregarded if overload protection is to be considered. Among the three reusable technologies, MCB may be discarded in low inductance DC systems due to their slow time response. Regarding performance (acting time and arcing), SSCB and HCB get better results than MCB since both can achieve zero arcing and the acting time is improved specially in the SSCB case. Anyway, the target application will determine whether to use Solid State technology which drastically reduces the acting time but drawing back overall's efficiency or HCB is the way to go which means bigger fault current handling without altering the system efficiency.

1.4 Recent Schemes

In an attempt to find efficient current protections for low impedance systems e.g. energy storage systems, 3 recent circuit breaker configurations are reviewed [24]. For each of the schemes, 4 sub-figures are shown. The first one depicts the protection itself whereas the 3 remaining explain the protection mechanism from normal conduction (0) to MOV discharge (2).

1.4.1 Scheme A - Solid State Assisted Turn Off breaker

The first scheme, showed in Figure 1.7, is a hybrid circuit breaker composed by a Fast Mechanical Switch (FMS) in parallel with a capacitor plus anti-parallel thyristors. A Metal Oxide Varistor (MOV) is also connected in parallel in order to dissipate the magnetic energy stored in the line inductance.

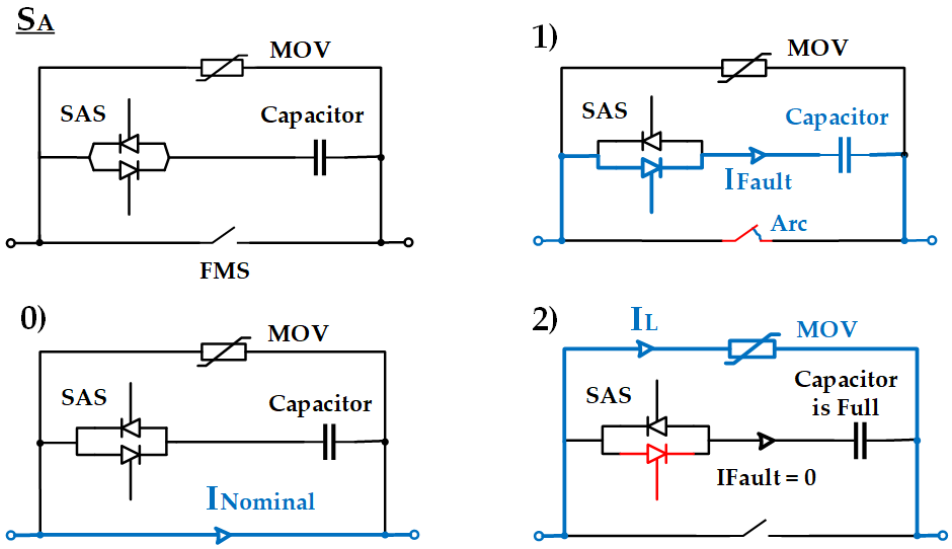

Figure 1.7: 0) Normal condition: FMS is closed; 1) Fault condition: FMS in red is open; 2) Capacitor is charged so the thyristor begins to block the voltage. MOV: Metal Oxide Varistor, SAS: Semiconductor Accessary Switch, FMS: Fast Mechanical Switch

When a fault is detected the FMS opens to commutate the current to the anti-parallel tyristor branch. Once the capacitor is fully charged, the current becomes zero setting the thyristor into blocking state. Lastly, the over-voltage generated by the line inductance is dissipated through the MOV.

1.4.2 Scheme B - Hybrid No Arcing Breaker

Another hybrid breaker is presented in the second scheme. In contrast to the previous topology, here the FMS is opened while no current is passing through.

Therefore, arcing is prevented.

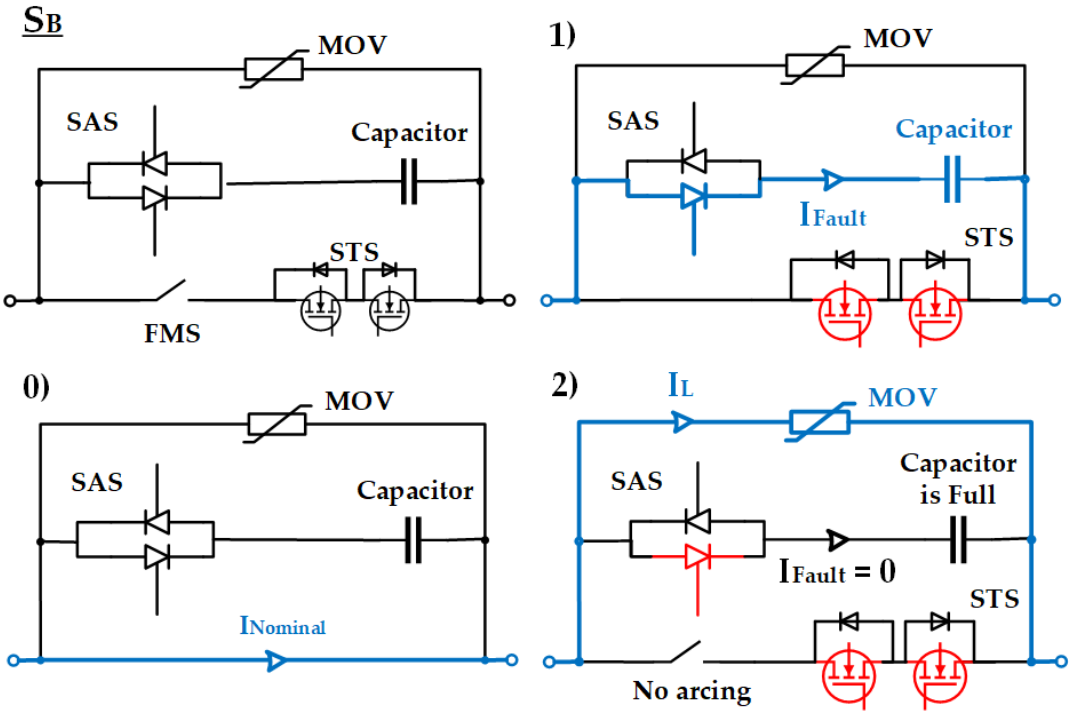

Figure 1.8: 0) Normal condition: FMS is closed; 1) Fault condition: a fault signal switches off the STS what commutates the fault current to the thyristor branch; 2) The same fault signal opens (with the corresponding delay) the FMS. Meanwhile, the thyristor started blocking once the capacitor became fully charged; MOV: Metal Oxide Varistor, SAS: Semiconductor Accessary Switch, FMS: Fast Mechanical Switch, STS: Semiconductor Transfer Switch

This is done by including a Semiconductor Transfer Switch (STS) that commutes the fault current to the thyristor branch when a fault is detected. Similarly as before, the fault is blocked by the thyristors and the line inductance is discharged through the MOV.

1.4.3 Scheme C - Full Solid State Breaker

Scheme 3 is a Solid State Circuit Breaker. Here the FMS is replaced with two anti-parallel thyristors which provide lower on-state conduction losses than IGBTS or MOSFETS. The second branch is composed by a bidirectional solid state switch though anti-parallel thyristors + capacitors would allow an unattended turn-off of the SAS.

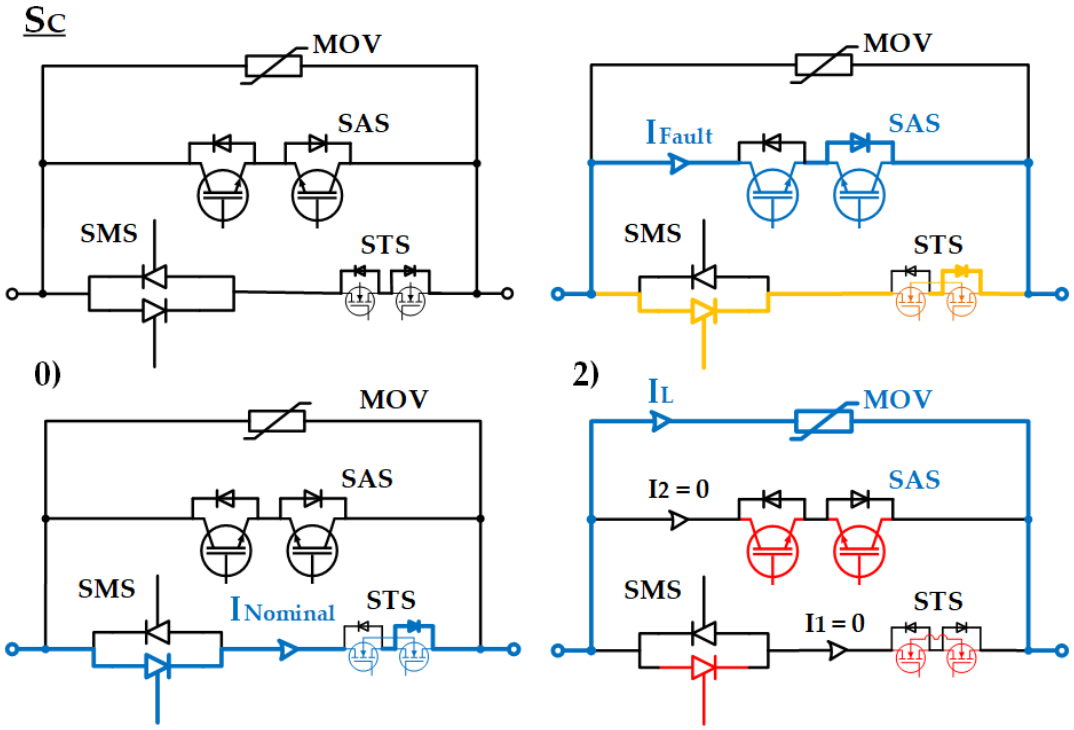

Figure 1.9: 0) Normal condition: SMS and STS in conduction; 1) STS turning off: fading current (yellow line) in main branch; 2) Note that SAS must be turned off only after the thyristor is blocking (I1=0 and then I2=0); MOV: Metal Oxide Varistor, SAS: Semiconductor Accessary Switch, STS: Semiconductor Transfer Switch

In '0)' the lower thyristor is turned on and both MOSFETS (STS) are on as well. Then, a fault is detected in what makes the STS turn off. '1)' is showing the turn-off transient when some of the fault current (in yellow) is still in the main branch. The SAS should be already on to directly start the conduction in the secondary branch. Once the current is zero in the main branch '3)', the thyristors enter into blocking mode enabling the SAS to be turned off and discharging the corresponding overvoltage in the MOV. It is crucial that the SAS is turned off after the thyristor is off. Otherwise the STS would blown up since its breakdown voltage was chosen to be minimum in order to provide ultra-low conduction losses.
As an alternative the SAS could be replaced with the anti-parallel thyristors plus capacitor as in schemes A and B.

1.5 Summary

The first chapter has introduced DC grid as an efficient way of energy distribution, generation and overseas transportation. Some examples were provided supporting this thesis e.g. the danish case, HVDC link map, etc. and the microgrid configu-

ration was presented. Afterwards, the protection challenges occurring in this DC grids were exposed (no zero current cross) and common protections used in the past were reviewed. After the identification of the main challenges to be overcome, i.e. (high power loss and low overvoltage handling capability), the research conducted the focus of this project to some recent circuit breaker topologies pursuing efficient protection in the medium voltage range.

Chapter 2

Problem Statement and Objective

2.1 Context

The present project can be framed into the area of electric system protection against overload and short-circuit faults. As outlined in the introduction, DC Microgrids are increasingly utilized to distribute electric energy. However, efficient protection against DC faults is still under research [4].

2.2 Definition

Current Solid State Circuit Breakers based on IGBT/MOSFET power switches present high on-state losses and limited forward blocking voltage capability for future medium voltage DC microgrids.

2.3 Research Question

The following thesis aims to find out whether a coordination of different switch technologies improves above-mentioned problems in Solid State Breakers.

2.4 Goal and Approach

This report and laboratory work pursue the experimental validation of the third SSCB scheme reviewed in Chapter 1 when protecting a generic circuit in a DC Microgrid.
On that direction, a prototype will be designed, constructed and tested in order to perform a technical comparison with a typical IGBT breaker of equivalent power range.

2.5 Limitations

A proof of concept in the low voltage range will be aimed to set up a simple framework of study and development. Table 1.2 shows the limitations of this work.

Electrical	
Supplies	External
Voltage class	Low voltage (16 VDC)
Power rating in conduction	640 W
Maximum non-repititive fault current	$\approx 100A$
Dynamics	
Breaking time	1us-1ms
Thermal	
Heat evacuation	Conduction (Heatsink)
Equilibrium temperature	67 °C
Dimensions and Mounting Style	
Max. Volume	$1m^3$
Max. Weight	5 kg
Mounting Style	Power Modules + PCB

Table 2.1: Prototype limitations

Chapter 3

System Background

This chapter presents the theoretical foundations of this project and the resulting prototype. First, a classification of electric faults presented setting the focus into DC systems. Next, the system under consideration is exposed. In the last section, the mathematical expressions explaining efficiency, performance and response for the topology object of study - Figure 1.9 - which will be designed in Chapter 5.

3.1 Electric Faults

The term fault is used in electrical engineering to refer to an abnormal change in the current flowing through an electrical circuit. According to this change, the fault can be generaly classified in three groups [17], [11].

1. **Open Circuit Fault**
   Given a failure, e.g. exceeded conductor temperature, the current flow from source to load may be undesirably interrupted.

2. **Overload Fault**
   This sort of fault can address a sudden load decrease or a supply increase. In any of the cases, the nominal current is exceeded.

3. **Short-circuit Fault**
   The current ramps up suddenly putting in danger the electric system and its surroundings. A physical contact between supply and return conductors is a common cause of short-circuit fault. At this point, only two times the equivalent resistance from supply to fault location limits the current.

A more specific classification can be done by looking at the current waveform when the fault takes place. Therefore, if a constant current (Direct Current) is running through the system while the fault occurs, the fault will be cataloged as 'DC fault'

whereas, if the current waveform is alternating, the fault is considered an 'AC fault'.

3.1.1 DC Short-circuit Faults

Now, setting the focus into DC short-circuit faults, Figure 3.1 illustrates the current shape along time for different types of DC sources.

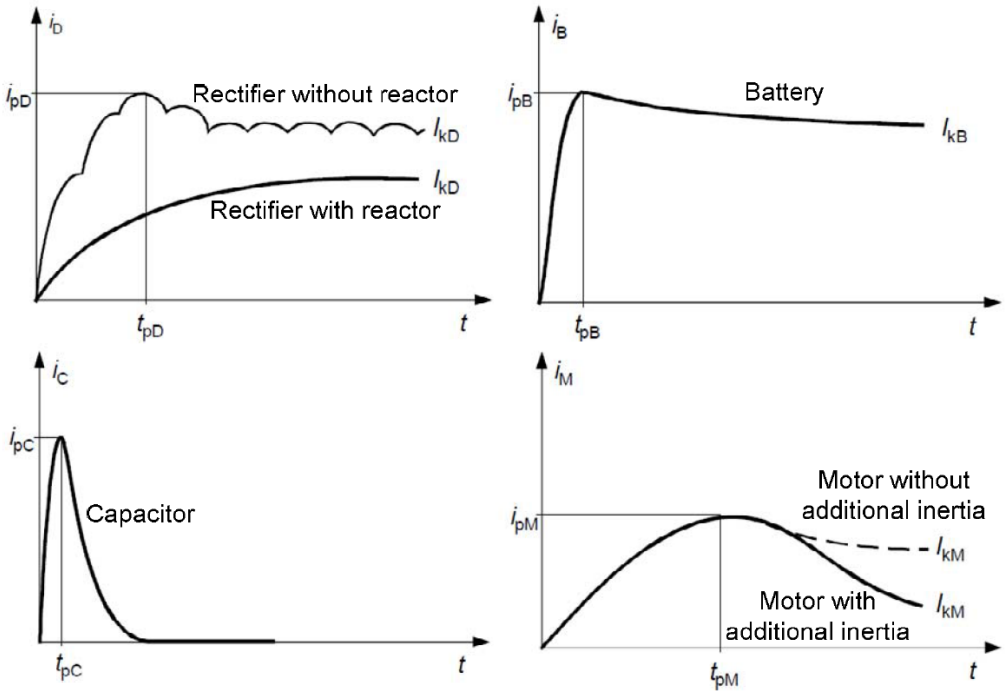

Figure 3.1: Short-circuit waveforms for a) rectifier, b) battery, c) capacitor, d) motor [16].

Fault Locations

DC systems may experience two types of short-circuit faults: line to line and line to ground. Line to ground faults are less serious as compared to line to line faults but they are likely to occur more often in the distribution systems [9]. The line to line fault occurs when the negative and positive lines of DC system is short circuited, hence the voltage doubles if lines are symmetrical, while line to ground fault arises when either positive or negative line get short circuited with ground [5]. Figure 3.2 shows both faults scenarios.

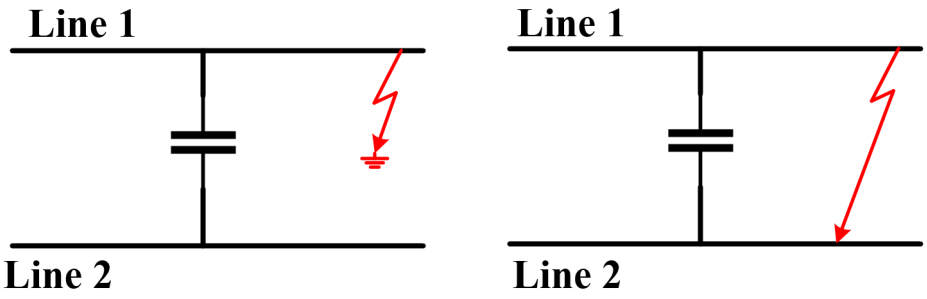

Figure 3.2: (a) Line-ground fault in DC bus, (b): Line-line fault condition in DC bus

Line to ground faults can have either low or high fault impedance, whereas line to line faults normally have low impedance [9]. Furthermore, short-circuit faults at different locations in DC system will have different implications. The active sources present in the system contribute to the total short-circuit current depending on the impedance between active source and fault locations. Thus, the identification of possible fault locations is very important before designing a protection system.

3.2 Full Solid State Circuit Breaker

After analyzing the three topologies reviewed in the introduction, finally scheme C was selected for two reasons. First, no mechanical switch is used to break the current ergo no replacements should be required. Second, it is the fastest of the three in breaking the current which may increase the safety an reliability of whole system.

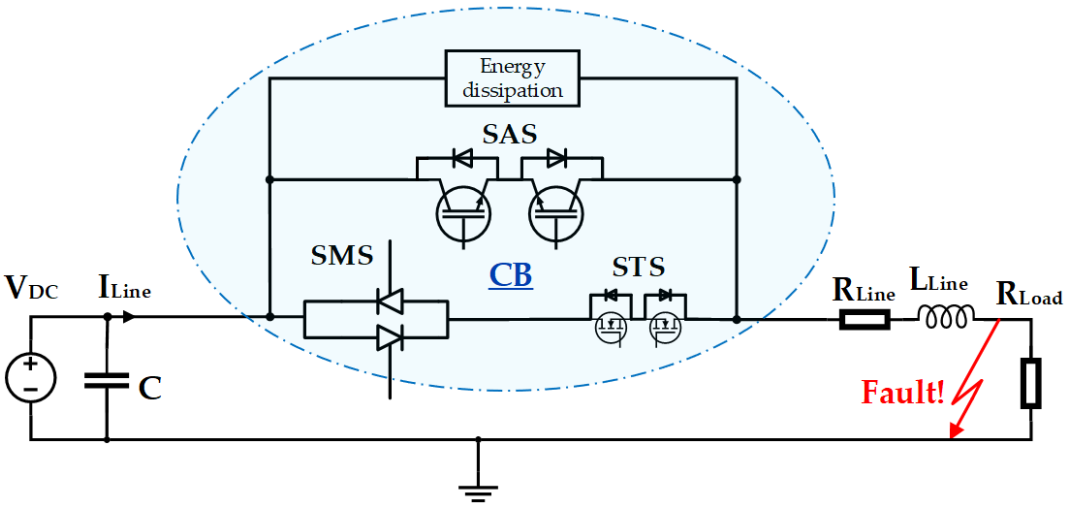

Figure 3.3: Selected circuit breaker protecting a microgrid circuit based on a DC source, a line inductance and a resistive load

This section deals with the physical foundations of the proposed circuit breaker - device inside the light blue ellipse - showed above.

3.2.1 Electrical Efficiency

The calculation of power losses for the new circuit breaker is immediate once a working prototype is up an running:

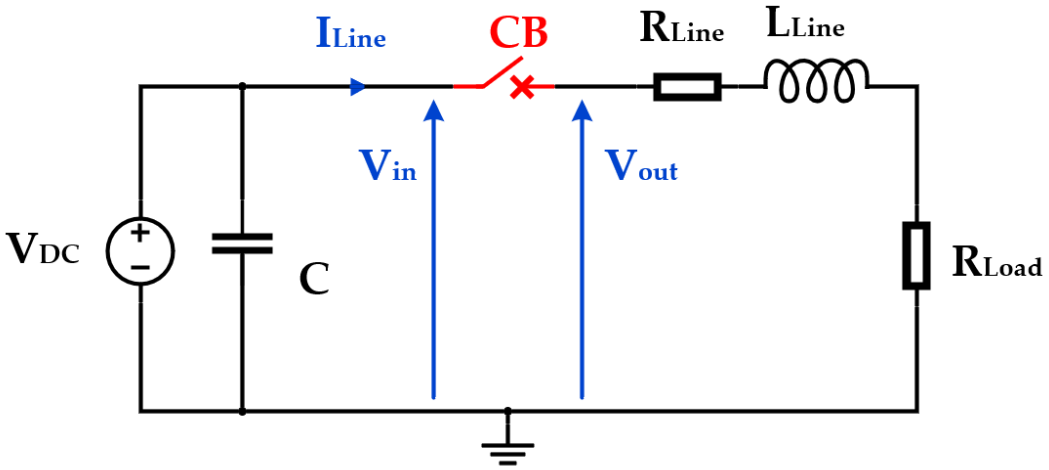

Figure 3.4: Location of the measurements

$$\left.\begin{aligned} P_{In} &= V_{In}\, I_{Line} \\ P_{Out} &= V_{Out}\, I_{Line} \end{aligned}\right\} \quad \begin{aligned} \eta &= \frac{P_{Out}}{P_{In}} \\ P_{Loss} &= P_{In} - P_{Out} \end{aligned}$$

Figure 3.5

However, to know before spending time and money that the efficiency will comply the demand, it is convenient to obtain it by mathematical means. Knowing the switch parameters (provided by manufacturers) and a steady state current specification, the losses in the switches may be independently computed.

MOSFET losses

MOSFETs losses derivation are based on [22] and may be calculated as the sum of three different powers:

1. Conduction losses (Pc)
2. Switching losses (Psw)
3. Blocking losses (Pb)

Due to the nature of the application - a circuit breaker - Psw can be neglected for the switching loss will only take place once in a long period of time. Pb occurs due to a small leakage current-flow whenever the semiconductor is set into blocking mode. The value of this currents is so small that the term can be neglected as well when computing to the overall losses.

For an estimated junction temperature and a demanded current will a corresponding $R_{DS_{ON}}$ may be obtained from datasheets or experimentally. Multiplying by the drain current, the voltage drop is calculated:

$$U_{DS} = R_{DS_{ON}} I_D \tag{3.1}$$

Then, the instantaneous conduction losses of the MOSFETS are obtained multiplying this voltage drop by the drain current.

$$p_{CM}(t) = u_{DS} i_D(t) = R_{DS_{ON}} i_D^2(t) dt \tag{3.2}$$

Also, the average power may be expressed as

$$P_{CM} = \frac{1}{T_2 - T_1} \int_{T_1}^{T_2} R_{DS_{ON}} i_D^2(t) \tag{3.3}$$

for any T1 and T2 where T2 > T1.

Then, taking into account that

$$I_{D_{RMS}} = \sqrt{\frac{1}{T_2 - T_1} \int_{T_1}^{T_2} {i_D}^2 (t)\, dt} \tag{3.4}$$

The average power may be rewritten as:

$$P_{CM} = R_{DS_{ON}} I_{D_{RMS}}^2 \tag{3.5}$$

Since the MOSFET is working in a DC micro-grid and the current through the inductance is constant after few milliseconds $i_D(t) = I_D$ and the RMS value of a time constant function is equal to itself $RMS(I_D) = I_D$, the following expression is obtained:

$$P_{CM} = R_{DS_{ON}} I_D^2 \tag{3.6}$$

The voltage drop across the in-built diode may be approximated by the equivalent source plus series resistance model:

$$u_D(i_D) = u_{D0} + R_D i_F \tag{3.7}$$

To obtain the instantaneous conduction losses in the diode only remains to multiply by the current:

$$p_{CD}(t) = u_D(t) i_F(t) = u_{D0} i_F(t) + R_D I_F^2 \tag{3.8}$$

Finally, considering steady-state is reached, the expression before may be rewritten as follows:

$$P_{CD} = U_{D0} I_F + R_D I_F^2 \tag{3.9}$$

Thyristor losses

The derivation of the on-state losses in the thyristor has being consulted from [30]. Here the thyristor is modeled similarly as the MOSFET diode before. So, provided the threshold voltage $V_{T(TO)}$ and the slope resistance r_T, the instantaneous power and the average power are respectively obtained for a DC application as follows:

$$P_T = v_{T(TO)}(t)i_T(t) + r_T i_T^2(t) \tag{3.10}$$

And under steady state is may be re-written like:

$$P_T = V_{T(TO)}I_T + r_T I_T^2 \tag{3.11}$$

IGBT

In DC steady-state the next expression is considered:

$$P_I = V_{CE_{ON}}I_{C_{av}} + r_C I_{C_{RMS}}^2 \tag{3.12}$$

Similarly, for the external anti-parallel diode:

$$P_d = V_D I_D + r_D I_D^2 \tag{3.13}$$

Snubber Resistor

The impedance of the snubber branch will be high enough compared to the other branches so no power will be dissipated during normal conduction. Only during the fault event, the following power will be dissipated:

$$p_{R_{snubber}} = R_{snubber} i_{snubber}(t)^{\,2} \tag{3.14}$$

where $i_{snubber}(t)$ describes a decreasing exponential waveform. To obtain the average power dissipation, the expression below can again be used:

$$P_{R_{snubber}} = R_{snubber} I_{RMS_{snubber}}^2 \tag{3.15}$$

3.2.2 Thermal Management

The thermal dimension of the circuit breaker plays an important role for ensuring its integrity and estimating its power losses.

First, as a necessary condition, the junction temperature in any of the switches must not surpass - neither in steady nor transient state - the maximum admitted

temperature specified by the manufacturer. By steady state it is meant the time while the breaker is conducting an steady-state DC current from generator to load terminals. Transient state on the other hand, relates to turn-on, turn-off and load variations. In essence, anytime that voltage and current changes.

Secondly, the expected steady state temperature should be fixed in order to calculate breaker's expected efficiency since the electrical parameters of the switches are temperature dependant. A proper refrigeration system must be therefore considered to not surpass the decided steady state junction temperature. Figure 3.6 depicts the thermal model of a power module using an electrical analogy. In it is observed how the generated heat Q - mostly evacuated by conduction through a heatsink - modeled as a current source, and the temperatures in each module component are represented by an electrical potential with respect to ground, namely ambient temperature.

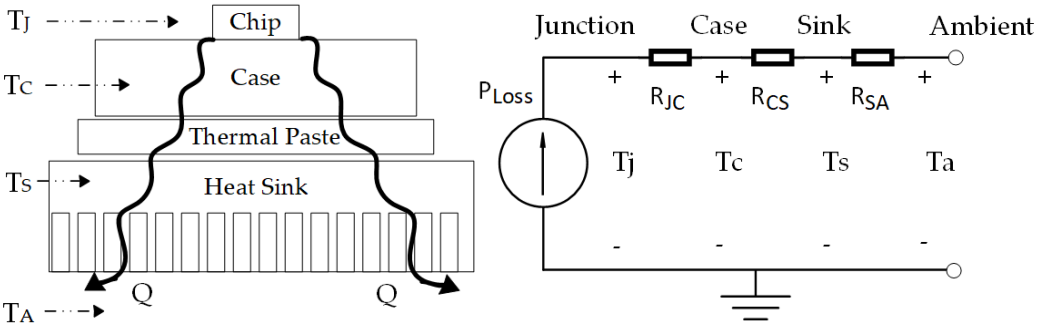

Figure 3.6: Typical power module (left). Steady state thermal model (right).

An equivalent thermal resistance can be obtained as it is done in electric theory:

$$R_{JA} = R_{JC} + R_{CS} + R_{SA} \tag{3.16}$$

Knowing the differential between junction and ambient temperatures, the power loss P_{loss} of the switch at its maximum admissible junction temperature T_J and the thermal resistances R_{JC}, R_{CS}, the maximum allowed thermal resistance of the solution heatsink R_{CS} is derived below:

$$R_{SA} = (T_J - T_A)/P_{loss} - (R_{JC} + R_{CS}) \tag{3.17}$$

Where the power loss is the sum of the switching and conduction losses at T_J or T_VJ in case of thyristors.

$$P_{loss} = P_{sw} + P_{cond} \tag{3.18}$$

From the equation above, the P_{sw} term can be neglected for the object of a circuit breaker is to switch only once. Thus, the equation can be fairly approximated to:

$$P_{loss} \approx P_{cond} \tag{3.19}$$

Overall, a heatsink featuring a lower R_{SA} than the one derived should be attached to the switch.

3.2.3 Gate Drivers

To reliably turn on and off the power switches comprising the breaker, three gate driver circuits will be designed in Chapter 5. As for the present section, the driver topologies used in each case and the way they influence the switch commutation are studied.

MOSFET/IGBTs basic gate driver

The minimum requirements for a MOSFEST/IGBT gate driver can be roughly summarized in the next two tasks:

1. Provide a sufficient gate voltage above the source.
2. Ensure that the input capacitance of the switch is charged by applying a certain current.

The simplest circuit to drive a MOSFET or IGBT is depicted in Figure 3.7.

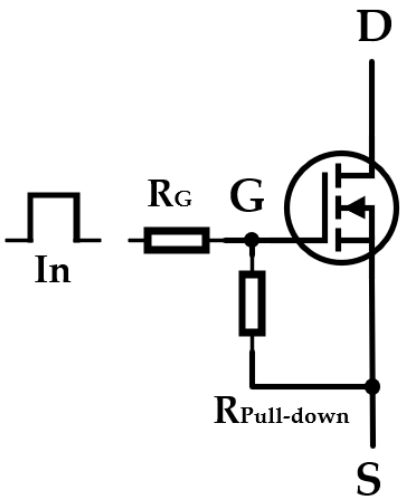

Figure 3.7: Essential gate driver circuit to drive a voltage controlled switch. V_{IN}: voltage provided by the gate driver. R_G: gate resistor. R_{PD}: gate pull-down resistor [34].

- IN represents the voltage provided by the driver. To turn the switch on, it must be higher than V_{th} in order to establish a conduction channel from drain to source. On the other hand, it must be lower than V_{th} to ensure it turns off.
- R_{PD} is a pull-down resistor. It sets the gate to zero voltage when the voltage input (IN) is floating.
- R_G is the gate resistor. It defines how fast the input capacitance is charged and affects to the switching loss of the device. The lower it is, the the faster the commutation is done. However, if too low, unwanted ringings may transmit to the output characteristics.

// // **Selected gate driver**

Among numerous gate driver circuits available in the literature [34], a photocoupler with floating power supplies is utilized due to its simple implementation the ubication of the breaker within the microgrid circut (right after the DC source). This fact implies the source/emitter is above the circuit ground for either MOSFET and IGBT common-source switches. Technically speaking, they are high-side switches and this practically implies that the voltage threshold may not be high enough to turn on these switches. Among popular circuits found in the literature, the Bootstrap or the one selected, are able to overcome this challenge. Finally, since single gate drivers are used, the photocoupler + external supplies solution was chosen.

Figure 3.8 illustrates this driver configuration:

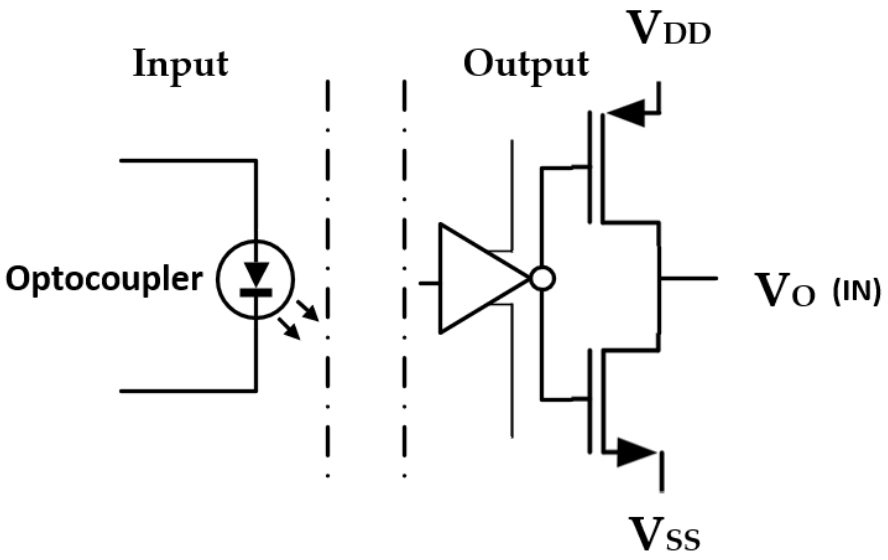

Figure 3.8: Isolated gate driver providing electric isolation between input and output. V_{DD}: positive power supply, V_{SS}: negative power supply

To the left of the gate driver there is a optocoupler. When the control circuit or directly a sensor excite it by applying a voltage difference between its terminals, it provides a light or radio-frequency signal that excites a photo-transistor or photo diode showed as a triangle (a transistor susceptible of electromagnetic biasing). This light modifies the carrier distribution in the transistor junction to make it commute. Depending on the driver specification it can be normally off or normally on. The PMOS + NMOS transistors showed on the figure, allow to use single or dual supply. In single supply V_{DD} is a positive voltage and V_{SS} is the ground while in dual V_{SS} can be selected to be negative. This provides a safety margin in case the source voltage rises as in a high-side switch may occur.

Gate resistors and Peak Currents

The gate resistor plays a determining role in the behaviour of the driven switch. On the one hand, the maximum peak current flowing through the gate driver should not be exceeded to ensure the integrity of the component. So, if to turn on the device, the driver sources a current $I_{G(Charge)}$, this current should not exceed I_{OH}. Conversely, when the switch is turned off, the driver sinks a current $I_{G(Disharge)}$ to discharge the parasitic capacitances $I_{G(Disharge)} < I_{OL}$. Next circuit illustrates

how to come up with a proper gate resistor based o the maximum allowed current specified by the manufacturer:

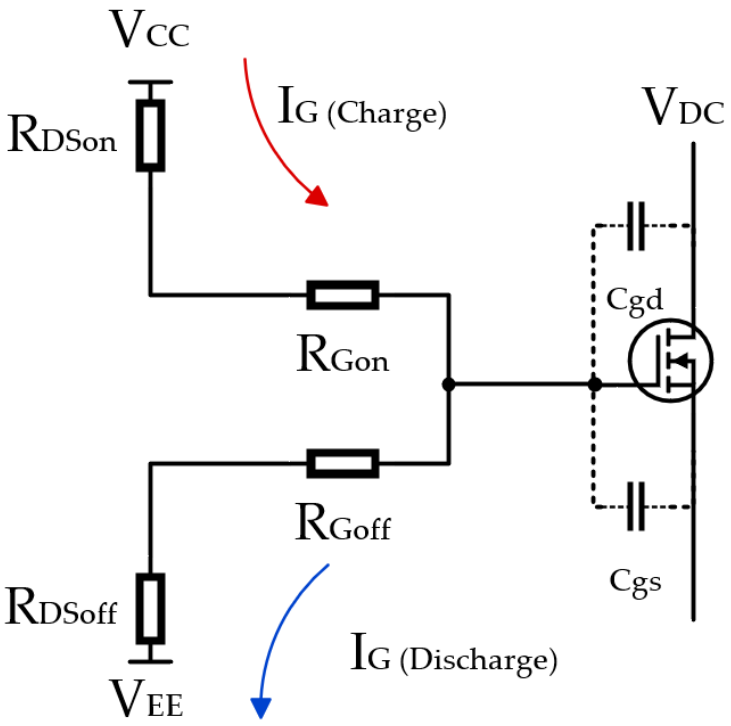

Figure 3.9: Gate currents for charging and discharging modes [20].

Then, looking up I_{OH}, I_{OL} and R_{DSon}, R_{DSoff} in the driver's datasheet, The minimum gate resistors may be calculated as follows:

$$R_{Gon} < \frac{V_{CC} - V_{EE}}{I_{OH}} - R_{DSon} \tag{3.20}$$

$$R_{Goff} < \frac{V_{CC} - V_{EE}}{I_{OL}} - R_{DSoff} \tag{3.21}$$

where R_{DSon}, R_{DSoff} are the conduction resistances for nMOS and pMOS transistors at the output of the gate driver, respectively.

Thyristor Gate Driver

The thyristor is a current-controlled device. Hence, a current must be supplied between gate and cathode terminals to enable a current-flow from anode to cathode [37].
On the other side, thyristors cannot be turned off by unbiasing the gate. Only

when the anode current becomes zero it will be certain that the thyristor is off. Figure 3.10 conceptually shows how to drive a thyristor.

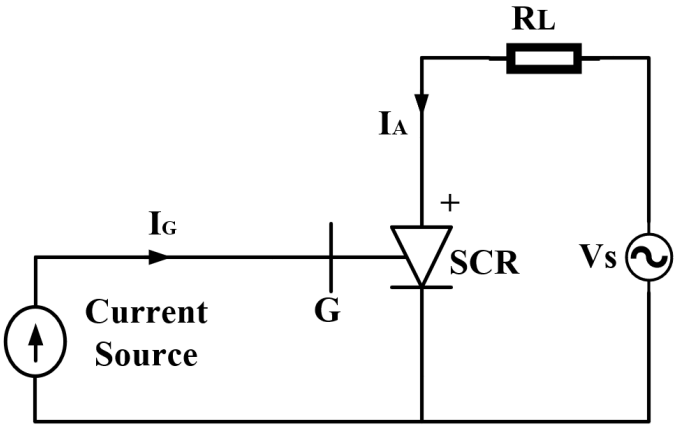

Figure 3.10: Thyristor gate driver concept

Next, two ways to drive a thyristor are shown:

Optocoupler Circuit

In Figure 3.11 an optoisolator is used to drive the thyristor gate providing electrical isolation between power circuitry and control circuitry (gate driver). When a pulse voltage is applied to the input of the optocoupler, the light emmiting diode D_1 turns on the photo-triac (secondary side) which enables to inject the necessary current-flow to turn on the thyristor. The magnitude of the gate current is controlled by choosing the appropriate gate resistor. R_G is selected not to surpass neither the maximum current handling capability of the optocoupler nor the maximum trigger current I_{GT} and voltage V_{GT} of the power switch [29].

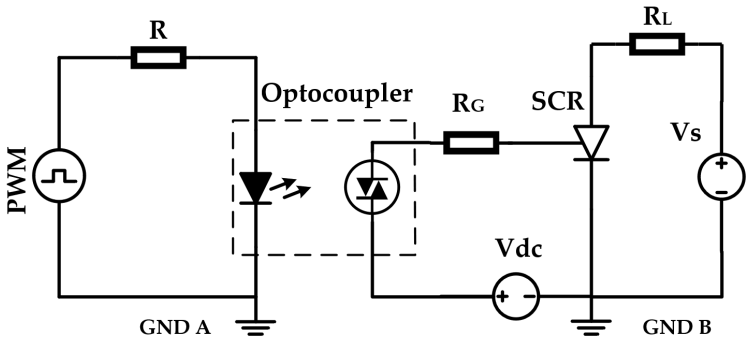

Figure 3.11: Optocoupler gate drivers

Pulse Transformer Circuit

A pulse transformer-based thyristor driving arrangement is shown in Figure 3.12. When a pulse with adequate voltage is applied to switching transistor T_s, transistor saturates, and the DC voltage appears across the primary side of the transformer. This voltage induces a pulse voltage across the secondary side which switches on the thyristor.

The series branch of diodes D_z and D_f across the primary side of the transformer demagnetizes the primary magnetizing current at turn off and prevent saturation [37]. R limits the secondary current into SCR gate and limit the current to protect the switching transistor T_s. The secondary transformer resistor R_G decreases the impedance from gate to cathode which helps to improve dv/dt capability. Moreover, diode D_r assists to counter the possible reverse gate voltage breakdown after T_s is switched off. The transformer duty cycle must satisfy $t_{off}V_z \geq t_{on}V_s$ to reset the core [37].

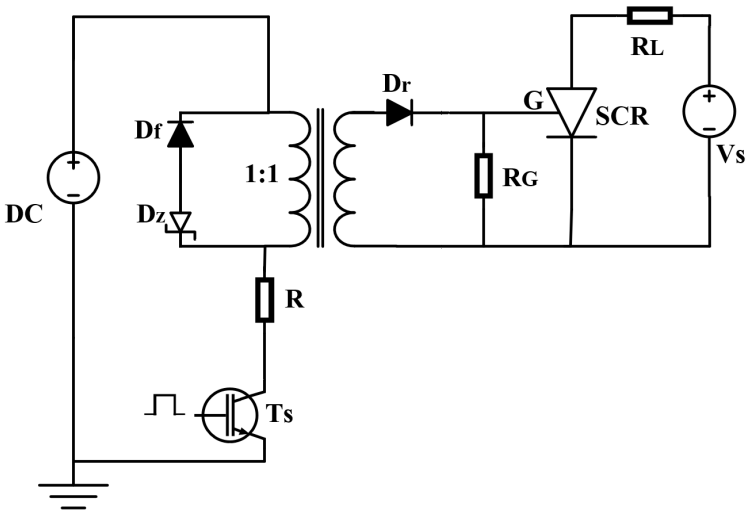

Figure 3.12: Pulse transformer based thyristor gate driver circuit

3.2.4 Power Discharge and Overvoltage Protection

When the breaker finally stops the conduction (as was planned), two issues need to be solved:

1. Maintain the power balance

The inductor storages energy in form of current during the conduction state of the breaker. In order to empty that energy (take the current to zero), some other

part of the circuit must take the lead. These parts are called snubbers, energy dissipation elements, surge arresters, varistors, etc. Their mission consists in getting rid of that energy by thermal means. There are other types of snubbers called regenerative snubbers. These ones instead of balancing the power through heat exchange they do it by charging another subsystem with capacity to get that energy.

2. Moderate the overvoltage

According to the voltage across the inductor equation

$$V_L = L\frac{di}{dt} \tag{3.22}$$

three parameters define the overvoltage that the system suffers at the breaking instant:

1. The system inductance **L**.
2. The magnitude of the dc current at the interruption time **di**.
3. How fast the current is interrupted **dt**.

Two solutions to both problems were found in the literature:

A. RC Snubber
B. Metal Oxide Varistor (MOV)

Figure 3.13 clearly shows what happens when the breaker switches interrupt their current path.

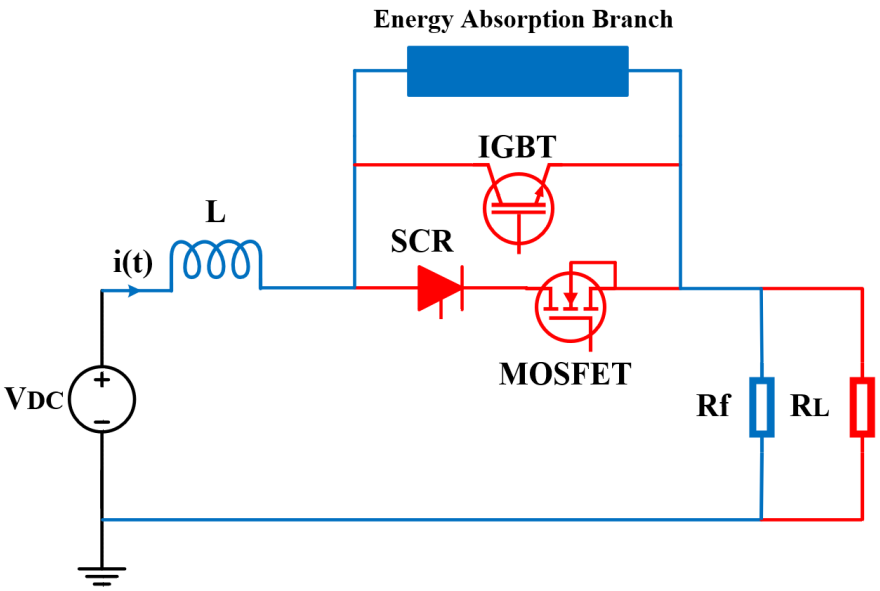

Figure 3.13: Last state of the CB. Blue: new current path, Red: no current-flow. Unidirectional case is shown to more easily show the concept

A. RC Snubber

Snubber circuits are used to suppress the voltage spikes caused by the system inductance when the power semiconductor switch turns off. A common circuit is the RC snubber [18]. Figure 3.14 particularizes the energy absorption branch shown in Figure 3.13 with an RC snubber while the power switches are represented by a symbolic circuit breaker (CB).

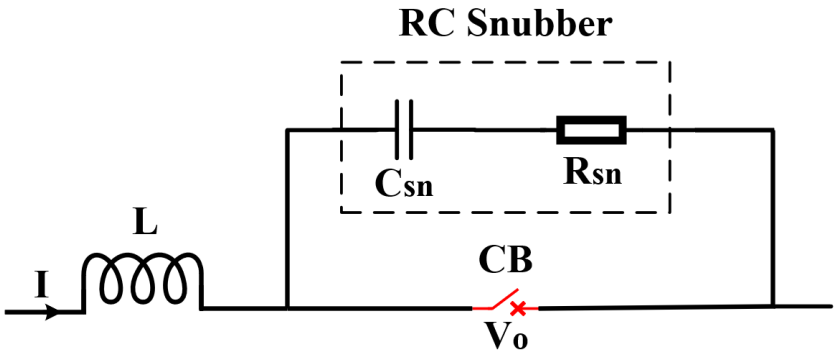

Figure 3.14: Unidirectional solid state circuit breaker

The worst-case peak current (negligible source impedance) can be calculated as:

$$I_{PK} = \frac{V_o}{R_{sn}} \tag{3.23}$$

Where V_o is open circuit voltage and R_{sn} is the snubber resistor.

The $\frac{dv}{dt}$ of the system can be formulated as:

$$I_{pk} = C_{sn}\frac{dv}{dt} \tag{3.24}$$

Substituting Equation 3.23 into Equation 3.24 the necessary $\frac{dv}{dt}$ rating of the capacitor is obtained:

$$\frac{dv}{dt} = \frac{V_o C_{sn}}{R_{sn}} \tag{3.25}$$

Now, to obtain a proper capacitance value for the snubber capacitor, The energy stored in the capacitor must be greater than the energy in the in the system inductance [18].

$$\frac{1}{2}C_{sn}V_o^2 > \frac{1}{2}LI^2 \tag{3.26}$$

Finally as a design recommendation, it is proposed in [18] that the capacitance is selected so as the power dissipated in the resistor is not higher to the half of the resistor power rating.

B. Metal Oxide Varistor

Metal Oxide Varistor (MOVs) is normally used as well to protect components against over voltages as lightning surges. MOV damps the overvoltage by producing the counter voltage. In DC SSCB application, the MOV may be essential component to protect the power switches. The MOV exhibits very nonlinear current voltage characteristics. Its resistance depends on the voltage. Under nominal system voltage condition, it blocks current flow while at high voltage levels MOV starts to conduct the current.

In CB application, the varistor is used to limit the transient recovery voltage (TRV) or so called overvolage. Limiting the TRV means absorbing the accumulated energy in the system's inductance. The nonlinear V-I characteristics of MOV with three operating regions is shown in Figure 3.15

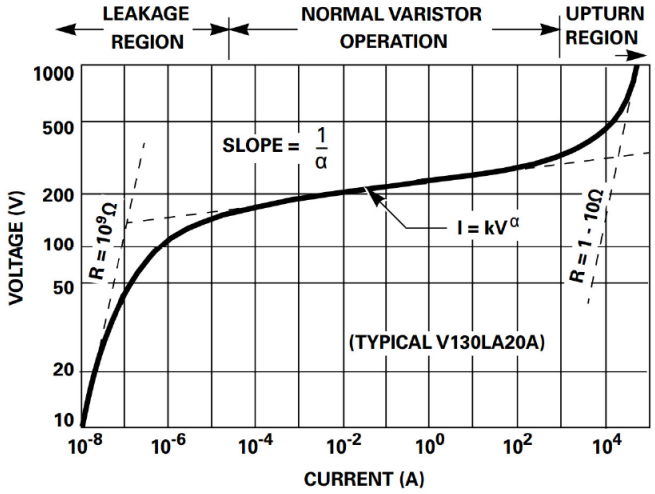

Figure 3.15: V-I characteristics in three regions,plotted in log-log scale [19]

Leakage Region

In this region as shown in Figure 3.15, the MOV behaves like a large linear resistor only conducting small current when applied low voltage across to it.

Normal Varistor Operation

During normal varistor operation, marginal increase in the voltage produces high rise of current. The MOV should be operated in this region to dissipate the energy after the breaking of SSCB.

Upturn Region

Further increase in the voltage across the MOV leads it to operate in upturn region. Here, it behaves like a small resistor and produces excessive heat which may thermally destroy the component[19]. This region should be avoided in designing the MOV.

The V-I characteristics in all regions can be expressed as [19]:

$$I_{mov} = KV_{mov}^{\alpha} \tag{3.27}$$

Where:

- I_{mov} represents current through MOV [A]
- v_{mov} is the voltage across MOV [V]

- K is ceramic material constant [S]
- α is exponent of non-linearity

When the fault current, I_{fault} reaches its peak value (time t_2), the MOV gets starts dissipating the energy. This fact imply a gradual decrease on the current until it reaches to zero, at time t_{mov}. During this period the MOV clamps the overvoltage to protect the CB from TRV (Transient Recovery Voltage). The time t_{mov} depends upon the peak value of the fault current and the line inductance of the system. Figure 3.16 illustrates MOV's V-I behavior from activation t_2 to zero current t_{mov}.

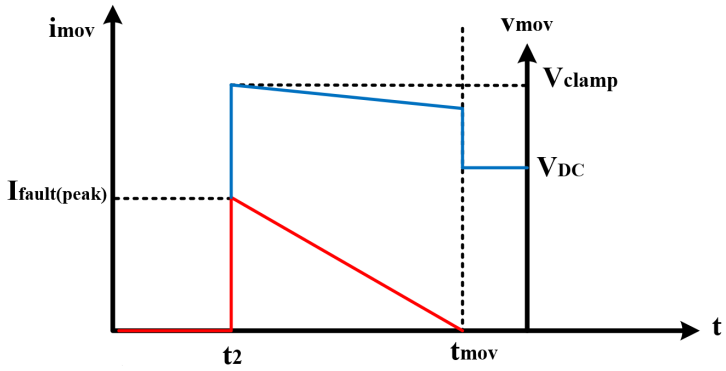

Figure 3.16: Activation of MOV

The time of zero current may be calculated as follows:

$$t_{mov} = \frac{L_{line} I_{fault}(peak)}{V_{clamp} - V_{DC}} \tag{3.28}$$

The energy absorbed by the MOV can be written as [19]

$$E_{mov} = \int_{t_2}^{t_{mov}} v_{mov}.i_{mov}\ dt \tag{3.29}$$

Defining each term as:

- E_{mov} energy absorbed by MOV W
- v_{mov} voltage drop across MOV V
- i_{mov} current through MOV A
- t_{mov} energy dissipation time s

To select a MOV according to the specific requirements, the maximum allowable energy absorption capability, maximum device temperature and maximum average power dissipation can be found in the data-sheet.

3.2.5 Series RLC Circuit Response

In Section 3.2.4 overvoltage protection solutions for SSCB are described in detail. If the RC snubber circuit is required to protect the switching device from overvoltage and to drive the fault current to zero. In each stage of SSCB operation, the different RLC equivalent circuits will be formed. So, the analysis the selected SB topology response, a general way to analysis RLC circuit is very important.

In the final stage of CB operation, a series RLC circuit is formed (See Figure 3.13). In this section the general way to analyze RLC circuit will be discussed and how its parameters effect the overall design. The general RLC series circuit schematic is shown in Figure 3.17.

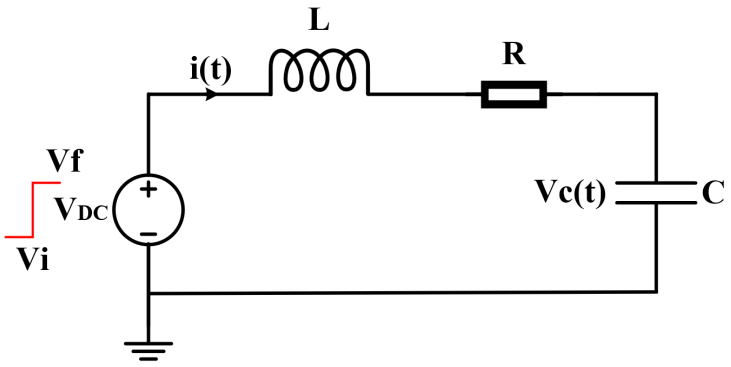

Figure 3.17: An RLC series circuit schematic

Applying Kirchhoff's Voltage Law (KVL), the voltage and current in the circuit can be written as follows [35]:

$$V_{DC} = v_c + Ri + L\frac{di}{dt} \tag{3.30}$$

$$i = C\frac{dv_c}{dt}. \tag{3.31}$$

After substituting the current $'i(t)'$ expression in equation 3.30:

$$V_{DC} = v_c(t) + RC\frac{dv_c(t)}{dt} + LC\frac{d^2v_c(t)}{dt^2} \tag{3.32}$$

This equation is second order differential equation with constant parameters. The complete solution of the system is the combination of transient response $v_{tr}(t)$ and steady state response $v_{ssr}(t)$.

The final time domain solution can be written as:

$$v_c\,(t) = v_{tr}\,(t) + v_{ssr}\,(t) \tag{3.33}$$

$$v_c(t) = \left(A_1 e^{s_1 t} + A_2 e^{s_2 t}\right) + A \tag{3.34}$$

Since the system is LTI, the nature of steady state response is the same as a forcing function $'A'$, which is the final source voltage V_f, in the case of RLC circuit. The transient response of the system dies out as $t \to \infty$ and $R > 0$. The transient solution can be obtained by solving the homogeneous differential equation. The homogeneous equation can be written as:

$$0 = v_c(t) + RC\frac{dv_c(t)}{dt} + LC\frac{d^2v_c(t)}{dt^2} \tag{3.35}$$

$$0 = \frac{1}{LC}v_c(t) + \frac{R}{L}\frac{dv_c(t)}{dt} + \frac{d^2v_c(t)}{dt^2} \tag{3.36}$$

$$x\frac{d^2v_c(t)}{dt^2} + y\frac{dv_c(t)}{dt} + zv_c(t) = 0 \tag{3.37}$$

After using the operator $s = \frac{d}{dt}$, $s^2 = \frac{d^2}{dt^2}$, equation 3.37 becomes:

$$xs^2 + ys + z = 0 \tag{3.38}$$

Where:

$x = 1$, $y = \frac{R}{L}$ and $z = \frac{1}{LC}$
The roots of the characteristic equation can be derived as [35]:

$$s_1 = \left(-\frac{y}{2x} + \frac{1}{x}\sqrt{\left(\frac{y}{2}\right)^2 - xz}\right) = \left(-\frac{R}{2L} + \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}\right) \tag{3.39}$$

$$s_2 = \left(-\frac{y}{2x} - \frac{1}{x}\sqrt{\left(\frac{y}{2}\right)^2 - xz}\right) = \left(-\frac{R}{2L} - \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC}}\right) \tag{3.40}$$

Depending upon the RLC components values, the roots of characteristic equation are classified in three categories.

- Over-damped response, when $\left(\frac{R}{2L}\right)^2 - \frac{1}{LC} > 0$
- Critically-damped response, when $\left(\frac{R}{2L}\right)^2 - \frac{1}{LC} = 0$
- Under-damped response, when $\left(\frac{R}{2L}\right)^2 - \frac{1}{LC} < 0$

The complete mathematically derivation of transient and steady state response of RLC series circuit in figure 3.17 is presented in appendix D. The response of the second order RLC circuit under different damping ratios can be seen in Figure 3.18

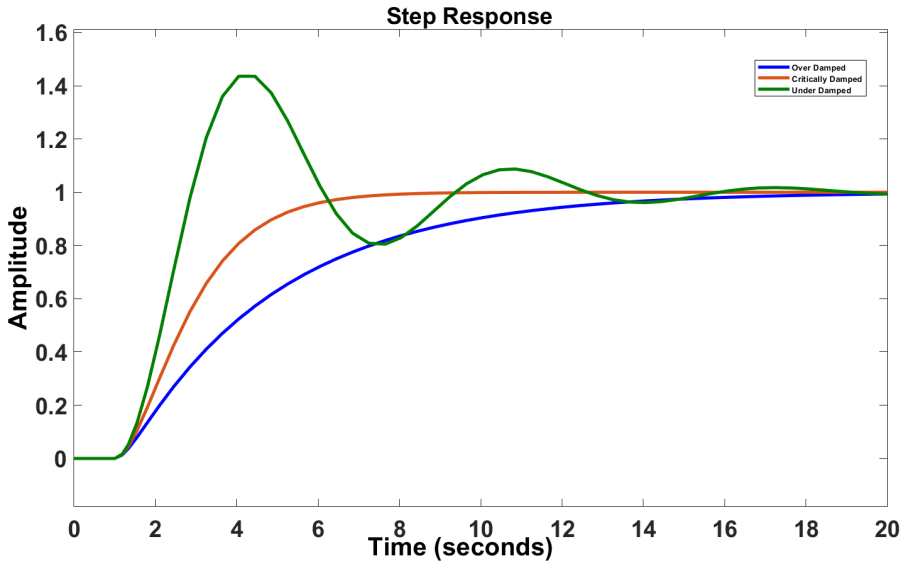

Figure 3.18: Over-Damped, Critically-Damped and Under-Damped response of series RLC circuit

Summary

A brief but to the point definition of electric fault and different classifications were provided setting the scope in DC systems as microgrids.

Next, the theoretical core of the project was developed, from the physics and hardware foundations to the software programming, passing through the conceptual coordination strategy of the switches that was elucidated thanks the understanding of the topology and simulation investigation.

First of all, the theoretical efficiency of the breaker is calculated from the different diagrams provided by the manufacturers of the switches. An objective current is fixed to do so and thus, being able to obtain the required heatsinks for all the devices.

Secondly, basic theory about gate drivers is provided based on professional application notes. Some gate driver circuits are discussed and the most convenient for the application are finally chosen in each case. Calculation methodology is presented to properly design MOSFET, IGBT and thyristor gate driver.

Finally, two solutions to dissipate the energy and attenuate the overvoltage in SSCB are derived and RLC series circuit is analyzed to find out the response of the system after the IGBTs turn off.

Chapter 4

Electrical Modeling

In this chapter, an early conception of the prototype is modeled and simulated in LTSpice software. To observe its behaviour, the circuit breaker is placed into a fault test-circuit that consists of four elements: DC source, line inductance, constant resistor and a time variable resistor. The last element will be used to simulate fault events within a single phase microgrid circuit.

4.1 Overall system

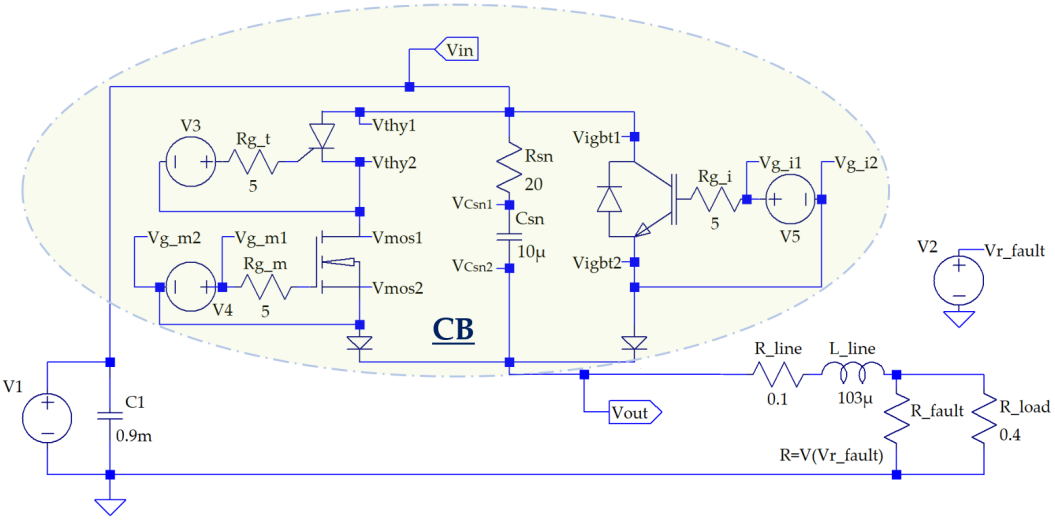

Figure 4.1: Single-phase microgrid circuit. Modern circuit breaker inside the oval

Figure 4.1 depicts the totality of the system under consideration: main circuit coming with new CB inside the dotted oval.

The next section explains the test circuit in detail while the rest of them will focus on the CB itself. That is, what is the control strategy and how is its performance: time response, dissipation of the fault, and conduction loss under an emulated DC fault.

4.2 Test Circuit

Before commencing the design of the circuit breaker a circuit able to emulate faults in a microgrid circuit is modeled in Figure 4.2. To simply model this application, a cascade connection between a generator and a consumer terminal is modeled. Table 4.1 clarifies the different components modeling each part of the circuit in reality.

Reality	Modeling
Generator terminal	V1, C1
Line	R_{line}, L_{line}
Consumer terminal	R_{load}

Table 4.1: Equivalence between reality and model

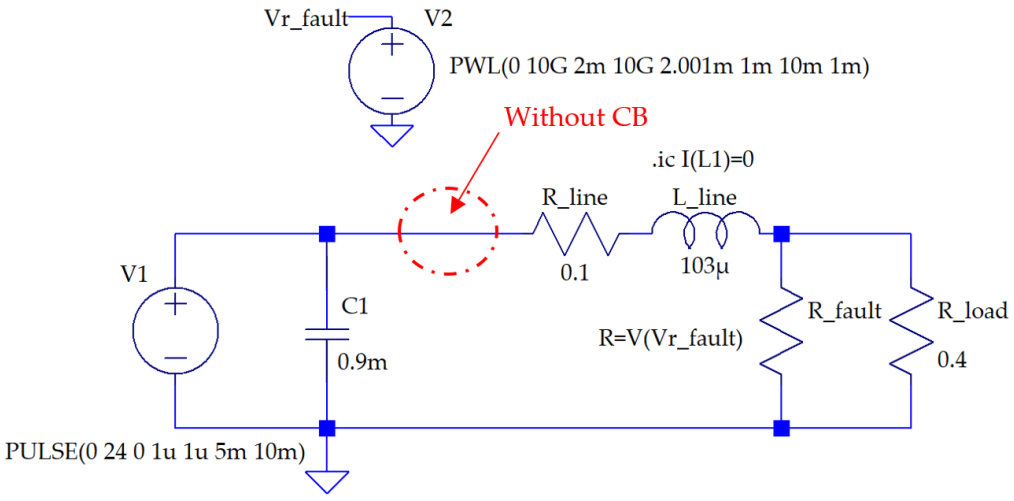

Figure 4.2: Circuit modeling a pole-to-ground fault between two terminals in a low voltage microgrid. From left to right: generator, line and consumer (R_{load}). The red oval indicates the circuit breaker is not included in the circuit.

4.2.1 Generator terminal

A 16 Volt DC source parallel connected to a equivalent capacitance of 0.9 μF is used to model this terminal. This big capacitance provides the necessary energy to develop the short-circuit current when the fault is generated. A 10 kΩ resistor is connected short-circuiting the capacitor to ensure its discharge when the circuit is powered off.

4.2.2 Line

The line is modeled by a a 103 μH air inductor representing the equivalent inductance for a 60 m (gone and return) line conductor. Also, a 0.1 Ω resistor representing the equivalent concentrated resistance for the inductor. A 16mm^2 aluminum conductor is considered.

4.2.3 Consumer terminal

An 0.4 Ω resistor is used to model this microgrid terminal in order to obtain an steady-state current of 40 A while no fault is present in the circuit.

4.2.4 Creating a fault

In the experimental tests, a MOSFET will create the fault events by short circuiting the load. For the LTSpice simulation though, a time variable resistor R_{fault} in parallel with R_{load} is a simple way to model this. In order to vary the resistance, the piece-wise linear voltage source $V2$ is identified with the resistor by the expression $R = V(Vr_{fault})$. Next, V2 is configured to behave first as a big resistor, e.g. 10 G. Then, when a steady state current is reached at 2 ms, the value is changed to perform as an small resistor - 1 mΩ. Figure 4.3 shows the resulting waveforms to illustrate this behaviour. The waveforms correspond to the circuit depicted in Figure 4.2.

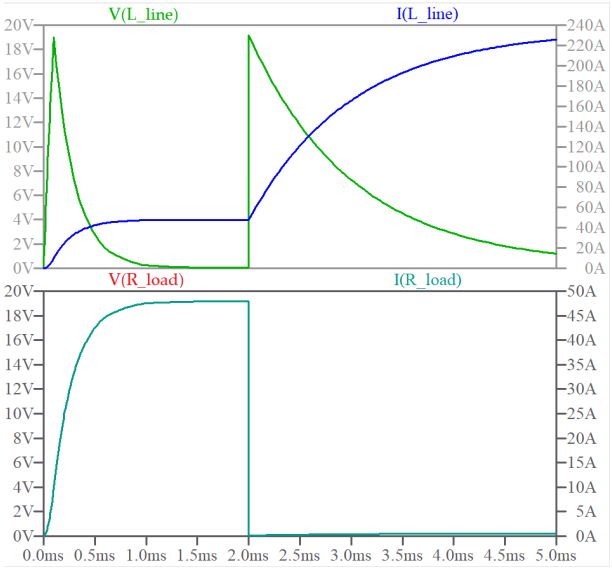

Figure 4.3: Fault beginning at 2ms. Voltage and current waveforms across: up) the line inductor, down) the resistive load

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4.3 Circuit breaker

The following section models the proposed breaker topology. In order to simplify its representation, only the positive switches and the active diodes of the complementary MOSFET and IGBT are shown. Since the exact switches to be implemented in the prototype are still unknown, available models of approximated ratings are used. Figure 4.4 shows a functional model of circuit breaker.

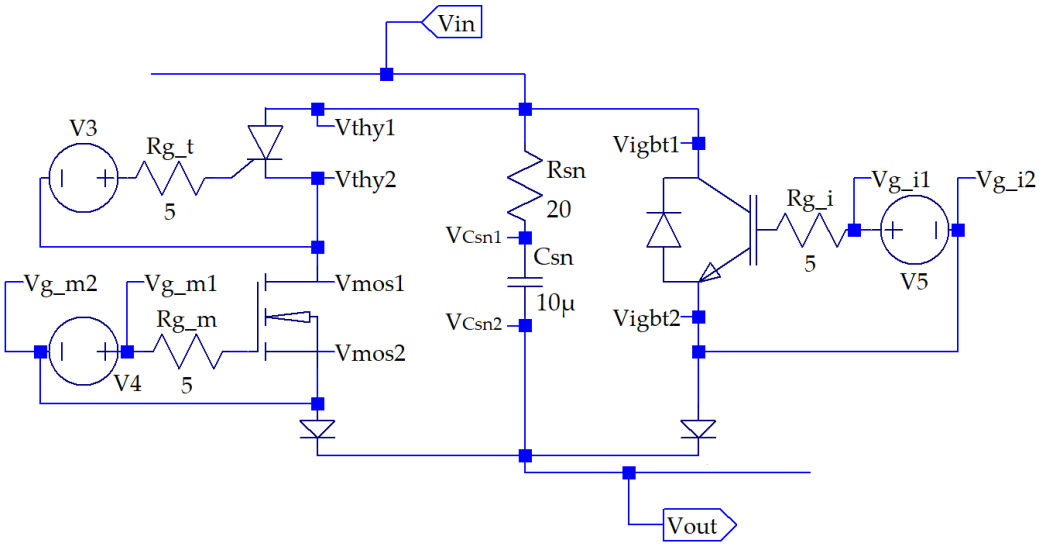

Figure 4.4: Functional model of the circuit breaker

4.3.1 Control strategy

The control strategy was introduced in Chapter 1. However, remains uncertain how the avalanche breakdown is avoided when turning off the MOSFETs. Figure 4.5 exposes the coordinated sequence the three switches may perform in order to overcome this problem. In essence, the maneuver consists in fast-switching the MOSFETs off and on in order to avoid the overvoltage. The thyristor therefore will absorb the overvoltage together with the IGBTs.

The red trace (Vg_m) illustrates how the MOSFET is turned off at 2.008 ms and turned on at 2.012 ms. In this Δt it commutes the current to the IGBT branch and subsequently turns on so no overvoltage is suffered. Simultaneously, the thyristor bias is removed to ensure no current flow circulates again in the main branch after the MOSFET is turned on.

Finally, the IGBTs turn off to stop the fault in approximately 30 μs after fault detection. The following waveforms correspond to the main circuit (Figure 4.2) and the breaker circuit (Figure 4.4).

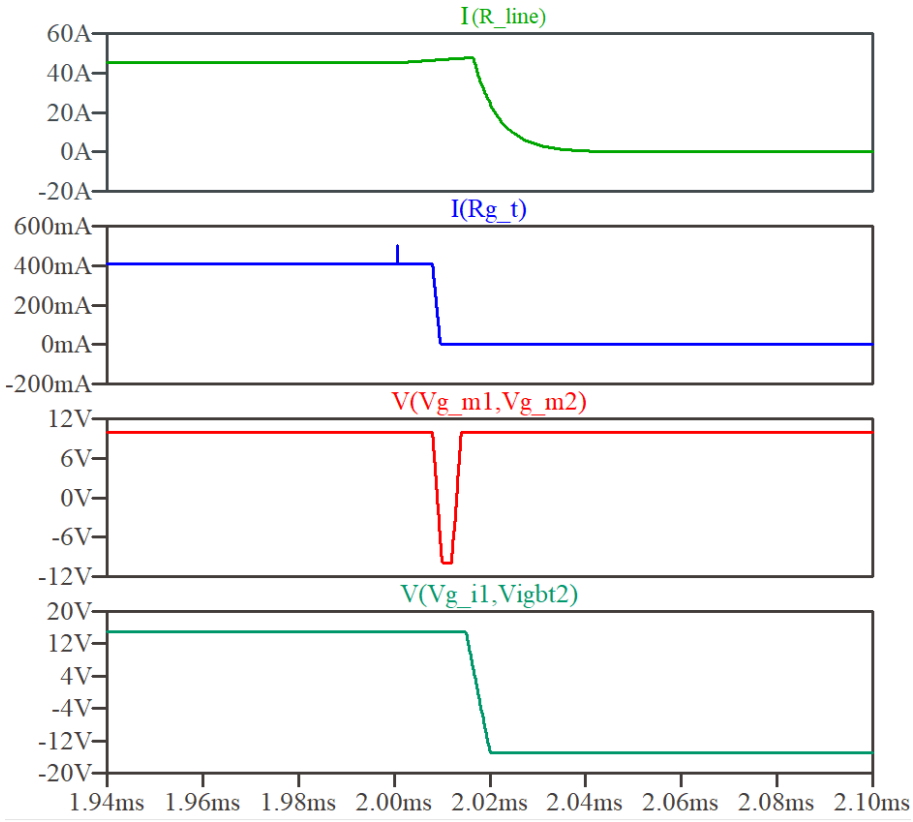

Figure 4.5: Bias waveforms. From top to bottom: line current, thyristor I_g, MOSFET V_{gs}, IGBT V_{ge}

The next section will explain how the the energy stored in the inductor dissipated and how do the breaker voltages and currents look when the fault and the switch coordination strategy takes place.

4.4 Time response

Once modeled the test circuit and the circuit breaker, the next step is to check out the temporal response of the system when a fault is generated and the CB is on the loop. Special interest deserves the branch which is responsible for dissipating the energy when the circuit breaks.

4.4.1 Snubber branch

Looking at Figure 4.4 the middle branch contains a 20 Ω resistor and a 10 μF capacitor. The function of this branch is to dissipate through R_{sn} the energy accumulated in the line inductor when breaking the fault through the circuit when the IGBTs are

turned off. Furthemore, make sure there is no current-flow through the breaker by fully charging C_{sn}. Figure 4.6 illustrates this behaviour. Alternatively, Metal oxide varistors can be used on this purpose as well. However, the activation region begings when the overvoltage is much higher than the the present application with a DC-Link of 16 V.

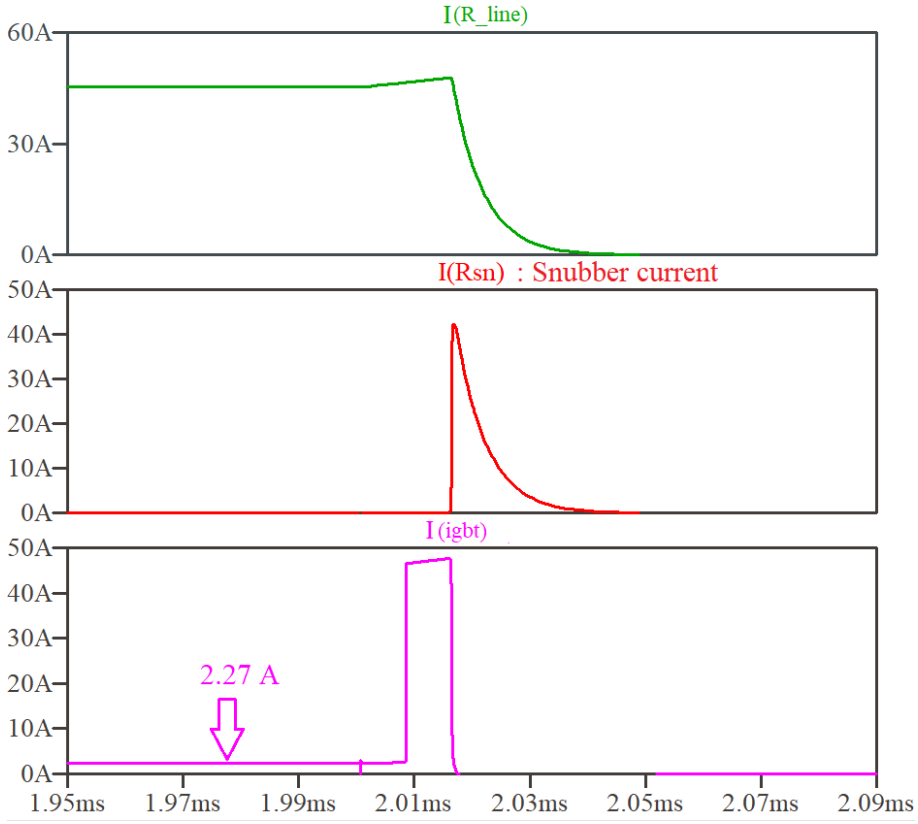

Figure 4.6: Green = line current, red = Snubber current, Magenta = IGBT current. Static consumption of 2.27 A

As seen in Figure 4.6, the IGBT has an static consumption of 2.27 A. This may be avoided by turning it off during normal operation. Nonetheless, efficiency-wise it supposes a little improvement since the efficiency goes slightly above the 95% as compared to when the IGBT is left turned off. Figures 4.7 and 4.8 shows the input and output powers obtained from the software for the two different commutation strategies:

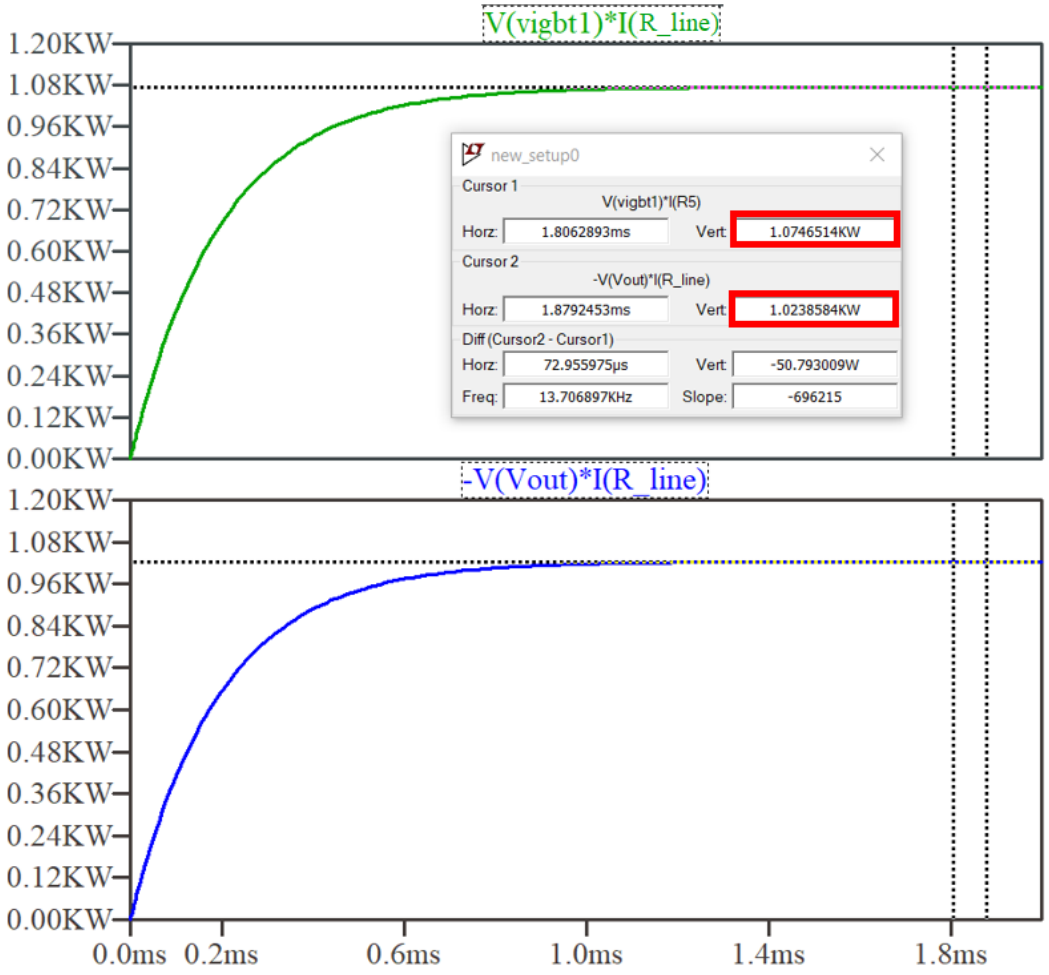

Figure 4.7: Steady-state power loss if the IGBTs stay conducting

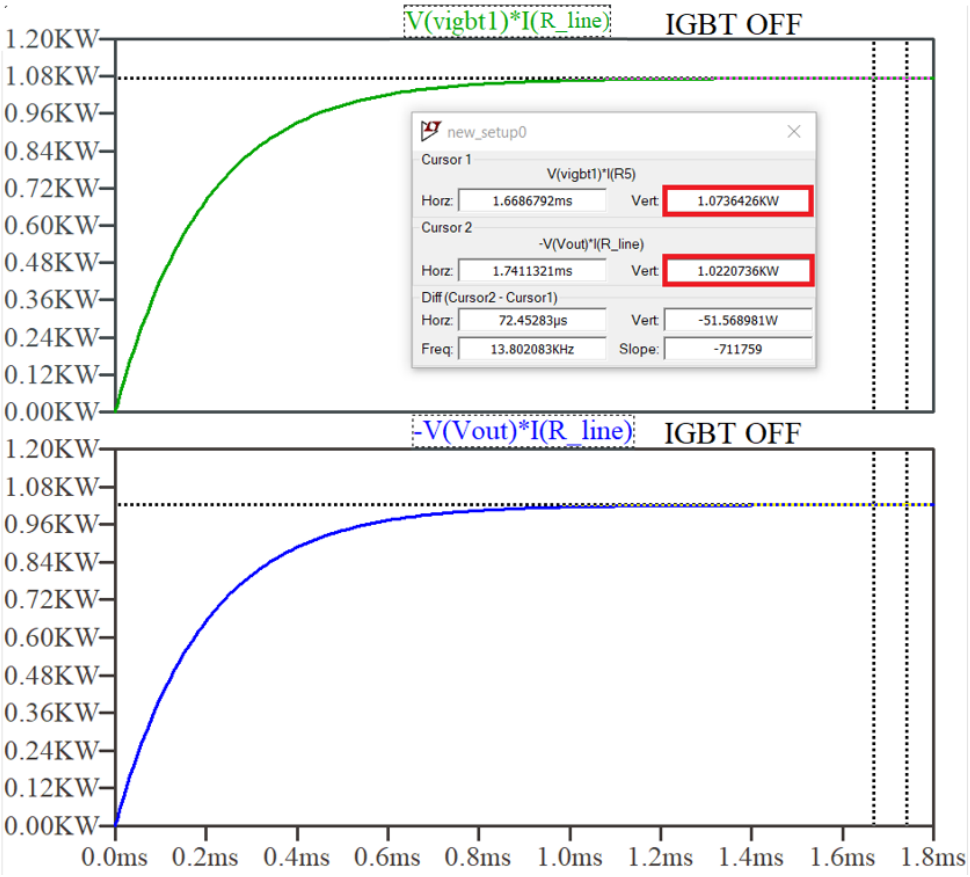

Figure 4.8: Steady-state power loss if the IGBTs remain open until the fault occurs

Calculating the efficiency for both cases:

$$\eta = \frac{P_{out}}{P_{in}} \times 100 \tag{4.1}$$

$$\eta_{IGBTs_{ON}} = \frac{1.02385}{1.07465} \times 100 = 95\% \tag{4.2}$$

$$\eta_{IGBTs_{OFF}} = \frac{1.02207}{1.07364} \times 100 = 95\% \tag{4.3}$$

4.4.2 Voltage and currents of interest

Four important observations may be extracted looking at Figure 4.9 which depicts the waveforms from the circuit opening this chapter. From upper to lower plot pane:

1. The current is breaked in around 25 μs

2. The thyristor experience a considerable overvoltage (close to 900 V). More preoccupying though may be the high dV/dt observed which can lead to its unwanted turn on.

3. The overvoltage in the MOSFET is way below its breakdown voltage. This seems to indicate that a fast turn on may be an effective way to protect the MOSFETs.

4. The IGBTs take the lead when the MOSFETS are turned off and on. Eventually, they are turned off after 8 μs.

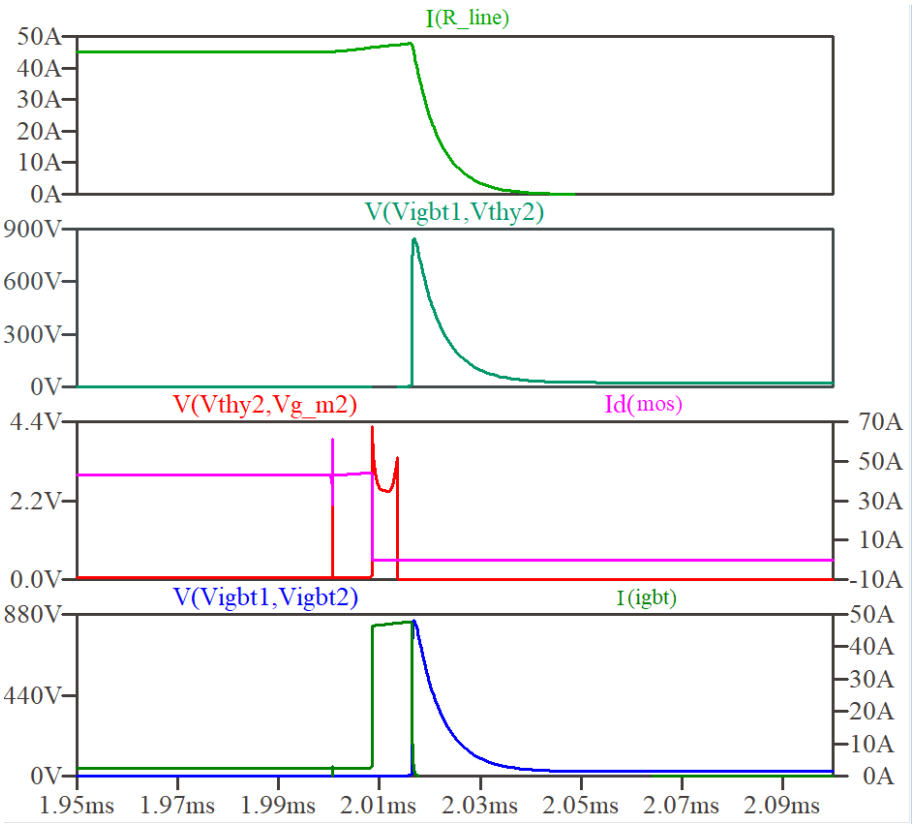

Figure 4.9: Voltages and currents in the circuit breaker

4.4.3 Summary

Chapter 4 has been helpful to quickly observe in a functional way how the topology behaves. In that way it has served as a backup and a reference to know what coordination strategy is the most interesting from a good performance and a minimal point of view.

At the very first, the overall system is presented. Then, each of its parts are are decomposed and explained part by part to create the big picture.

First, the test circuit is presented as the microgrid circuit subject of current protection. Next, a way to emulate faults in LTSpice is exposed. Moving forward, the circuit breaker schematic is depicted along with the gate signals of each device for a concrete emulated fault and a concrete coordination strategy of the switches. Finally, the resulting waveforms are exposed waiting to be confirmed by experimental tests.

Chapter 5

Prototype Design

The following chapter develops a reasoned component selection subject to the mathematical expressions derived in Chapter 3 and the test circuit showed in Chapter 4. The decisions taken in this phase will primary focus in the correct operation of the prototype. Safety margins will be applied throughout the design.

5.1 Switches Selection

The selection of the switches comes defined by the topology and the limitation table stated in Chapter 2.

Nonetheless, in order to minimize the conduction losses, a reduced $R_{DS_{on}}$ IRF100P219 MOSFET [21] and a low P_{loss} MCC162-18io Thyristor module [23] are aquired for the first branch of the breaker. In the second branch, two common source IGBTs modules are re-utilized from the past project. This IGBT modules at the same time will be the rival to beat in the experiments chapter.

5.2 Conduction Losses

In the section, a estimation of the conduction losses at the maximum permitted temperature for each switch is calculated as way to dimension the necesary heatsinks.

Looking into the datasheets, the following parameters are obtained under a maximum admissible junction temperature T_J of 175 ºC for the MOSFET and a maximum admissible virtual juntion temperature T_{VJ} of 125 ºC for the thyristors. The steady state DC current during conduction is finally set to 40 A to keep the heatsink dimensions reasonable.

Switch	Parameter	Test Conditions	Value	Units
MOSFETs	$R_{DS_{on}}$	T_J = 175 °C, I = 40 A	2.24	$m\Omega$
	V_{SD}		0.65	V
	r_d		0.43	$m\Omega$
Thyristors	V_{T0}	T_{VJ} = 125 °C	0.88	V
	r_T		1.15	$m\Omega$
IGBTs	$V_{CE_{ON}}$	T_J = 175 °C, I = 40 A	1.4	V
	r_I		17	$m\Omega$
	V_F		1.4	$m\Omega$
	r_d		7	$m\Omega$

Table 5.1: Switch conduction parameters under maximum admissible junction temperatures

Using the expressions formulated in Chapter 3, the conduction losses for the prototype may be evaluated as follows:

5.2.1 MOSFETs

On-state losses due to R_{DSon}:

$$P_{R_{DSon}} = R_{DSon} I_{D_{RMS}}^2 \tag{5.1}$$

$$P_{R_{DSon}} = 2.8 \times 10^{-3} \times 40^2 = 4.5\ W \tag{5.2}$$

Complementary in-built diode on-state:

$$P_d = V_{SD} I_S + r_d I_S^2 \tag{5.3}$$

$$P_d = 0.65 \times 40 + 4.3^{-4} \times 40\ 2 = 26 + 0.688 = 27\ W \tag{5.4}$$

Overall losses in the MOSFET:

$$P_{MOS} = P_{R_{DSon}} + P_d = 4.5 + 27 = 32\ W \tag{5.5}$$

5.2.2 Thyristors

On-state thyristor losses:

$$P_T = V_{T(TO)} i_T + r_T i_T^2 \tag{5.6}$$

$$P_T = 0.88 \times 40 + 1.15 \times 10^{-3} \times 40^2 = 35.2 + 1.84 = 37\ W \tag{5.7}$$

5.2.3 IGBTs

There are two options regarding the IGBTs. One is to leave them off during conduction so no power loss is developed. The other - keeping them on - could also be efficient if their $V_{CE_{ON}}$ is higher than the MOSFETs plus Thyristors branch which normally will be the case.

However, the same IGBT module needs to be tested in order to perform the comparison with the new CB design. Thus, the IGBT breaker on-state losses are calculated below:

$$P_{CI} = (V_{CE_{ON}} + V_F)I + (r_I + r_d)I^2 \tag{5.8}$$

$$P_{CI} = (1.4 + 1.4) \times 40 + ((17 + 7) \times 10^{-3}) \times 40^2 = 112 + 38 \approx 150\ W \tag{5.9}$$

5.3 Heatsinks Selection

The following thermal parameters together with the power losses calculated above permit to estimate the heatsink maximum thermal impedance ensuring that $T_{J_{max}}$ and $T_{VJ_{max}}$ are not surpassed. A maximum ambient temperature is set to 50 ºC instead of the expected 25 ºC of the room lab in order increase the robustness of the design:

Switch	Parameter	Observations	Value	Units
MOSFET	R_{JC} R_{CS}	Maximum value Insulation pad	0.44 0.4	K/W
Thyristor	R_{JC} R_{CS}	Conduction angle d = DC	0.155 0.07	K/W
IGBTs	$R_{JC_{Eq}}$ R_{CS}	Steady state	0.166 0.1	K/W

Table 5.2: Thermal parameters

5.3.1 MOSFETs

Recalling the formulas derived in the background chapter:

$$R_{SA} = (T_J - T_A)/P_{loss} - (R_{JC} + R_{CS}) \tag{5.10}$$

and assuming that the steady state DC current is unidirectional, two cases must be considered.

Conducting MOSFET

The necessary heatsink for the MOSFET conducting the current must regard only the power losses due to $R_{DS_{ON}}$. Therefore, substituting this power loss in Equation 5.1 R_{SA} is found:

$$R_{SA} = (175 - 50)/4.48 - (0.44 + 0.4) = 27.06\ K/W \tag{5.11}$$

Blocking MOSFET

This package will heat up due to the conducting diode. Accordingly, the maximum R_{SA} will yield:

$$R_{SA} = (175 - 50)/26.69 - (0.44 + 0.4) = 3.84\ K/W \tag{5.12}$$

In light of these thermal impedances and aiming to build a bidirectional breaker, the solution heatsink result should feature a R_{SA} lower than 3.84 ºC/W. However, willing to use the existing stock in the lab, a fitting SK64 featuring a 4.1 ºC/W thermal impedance is attached to each MOSFET. The manufacturer datasheet can be consulted in Appendix A.

In addition, since the prototype will be in a controlled environment (the ambient temperature will not exceed 40 ºC in the lab) and the maximum thermal resistance is reached at 43 ºC, the heatsink is considered as sufficient.

5.3.2 Thyristors

The thyristor module acquired consist of two anti-parallel thyristors embedded in the same power package. Therefore, an only heatsink is mounted on its back and its conduction losses are owned to one of them.

Recalling the expressions derived in the background chapter

$$R_{SA} = (T_J - T_A)/P_{loss} - (R_{JC} + R_{CS}) \tag{5.13}$$

and substituting values, it yields:

$$R_{SA} = (125 - 25)/37.04 - (0.155 + 0.07) = 2.47\ K/W \tag{5.14}$$

This time a 350AB heatsink featuring 1.5 K/W R_{SA} is attached to the anti-parallel thyristor module. Its datasheet can be is found in Appendix A.

5.3.3 IGBTs

The heatsink installed in the re-utilized IGBT modules overheated in excess when testing it at 40 ADC. Hence, a new heatsink is calculated below.

In this case two modules of IGBT + diode share the same heatsink. The R_{JC} the thermal impedance of the IGBT junction to case is 0.28 K/W and the diode junction to case is 0.41 K/W. Calculating the equivalent parallel thermal impedance and applying the formula described in the background, the minimum heatsink is calculated:

$$R_{JC_{Eq}} = (1/R_{JC_I} + 1/R_{JC_d})^{-1} = 0.166\ K/W \tag{5.15}$$

$$R_{SA} = (T_J - T_A)/P_{loss} - (R_{JC_{Eq}} + R_{CS}) \tag{5.16}$$

$$R_{SA} = (125 - 25)/150 - (0.166 + 0.1) = 0.56\ K/W \tag{5.17}$$

Using a 350AB heatsink with 60 mm of lenght and forced cooling, a thermal impedance of 0.5 K/W is achieved to comply with requirement.

5.4 Detection Board

The detection board, shown in Figure 5.1, consist in 3 stages. From left to right: detection, latch and MOSFETs/IGBTs drivers. The detection is done by current reference. Thus, the voltage drop across a shunt resistor on the secondary winding of a LEM sensor is compared to reference voltages which are tweaked by variable resistors. Its electric schematic can be found in Appendix B.

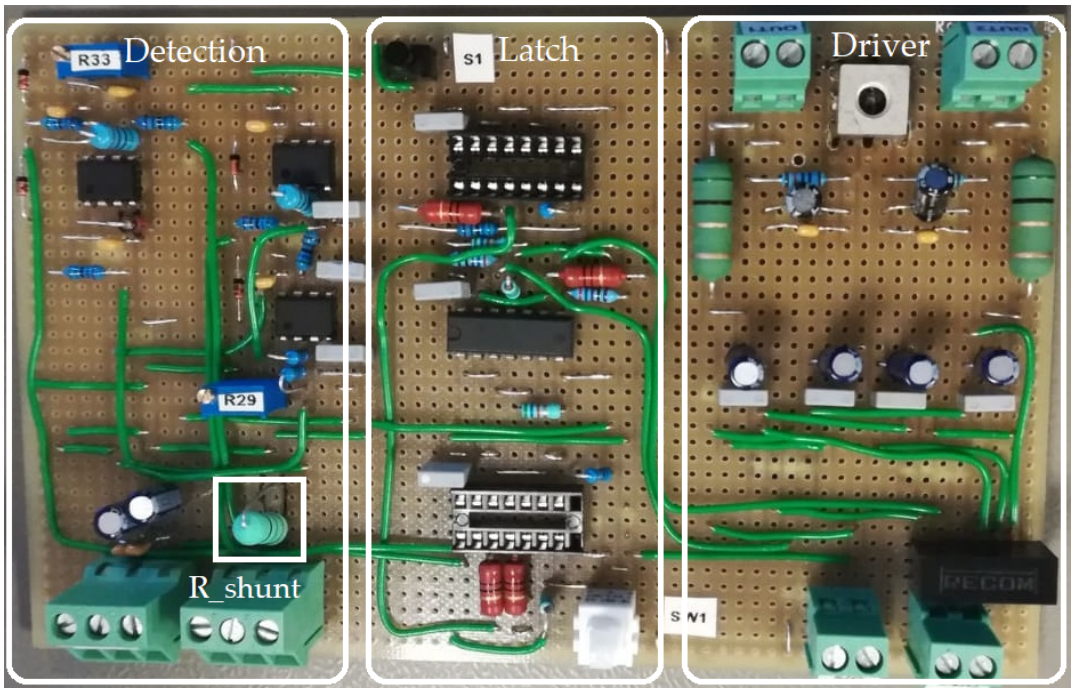

Figure 5.1: Detection board

For the first device under testing - the IGBT breaker - it drives the IGBT modules. In the second DUT - the modern circuit breaker - it will be used to drive the MOSFET power board instead. Hence, for driving the IGBTs, a twin driver stage is manufactured at AAU lab. The only variations are found in V_{GS} level and the gate resistors R_G.

5.5 MOSFET Power Board

A power PCB is manufactured at AAU to create a power path for the chosen discrete common source MOSFETs. Figure 5.2 shows its result.

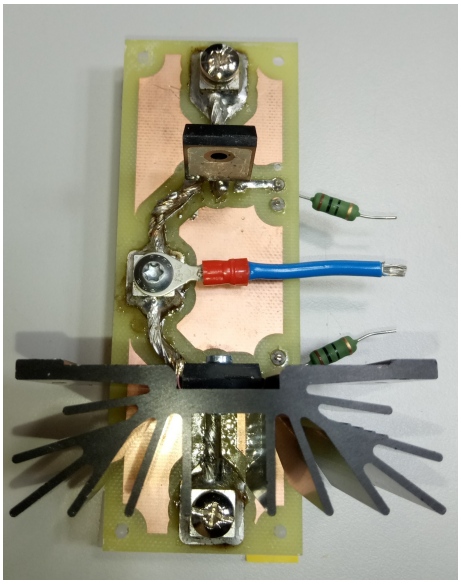

Figure 5.2: Common-source power MOSFET circuit

5.6 Thyristor Driver

To simplify the control, only one thyristor is connected (unidirectional case). A 5 volt PWM signal is generated with an Arduino microcontroller to excite the light emitting diode in the optocoupler. Below it is depicted the electric diagram of the thyristor gate driver circuit with a set of resistors complying with both optocoupler and SCR datasheet specifications. Afterwards, the calculations are exposed.

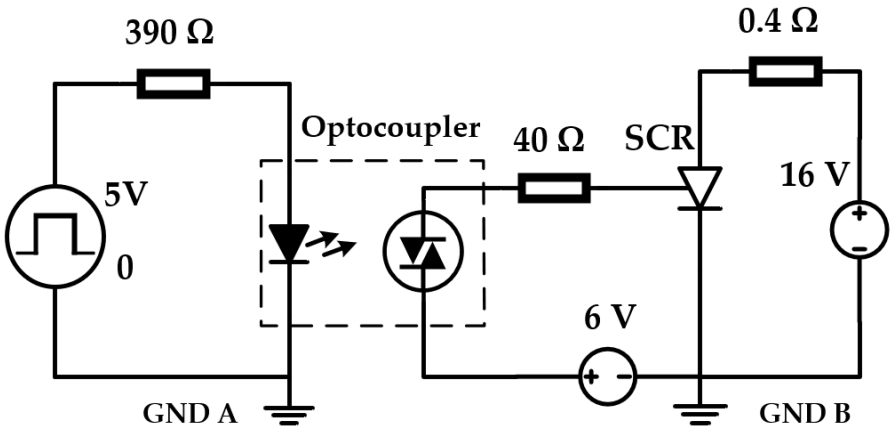

Figure 5.3: SCR gate driver test circuit

LED limiting resistor

Since I_{max} and V_F are specified in the datasheet, KVL can be written down in order to solve for R_{LED}:

$$V_{ON_{PWM}} = R_{LED} \times I_{LED} + V_{F_{LED}} \tag{5.18}$$

$$R_{LED} = \frac{V_{ON_{PWM}} - V_{F_{LED}}}{I_{LED}} = 380\ \Omega \tag{5.19}$$

Gate resistor

The cathode to anode gate loop is formed by a 6 V DC source, the optocoupler output and a limiting gate resistor. Solving for the resistor and knowing the maximum admissible trigger current $I_{GT} = 150\ mA$ and the phototriac voltage drop $v_{F_{Triac}} = 1V$, the following calculations are obtained:

$$V_D = V_{F_{Triac}} + R_G \times I_{GT} + V_{GT} \tag{5.20}$$

$$R_G = \frac{6 - 1 - 1.5}{0.1} = 35\ \Omega \approx 40\Omega \tag{5.21}$$

The calculated gate driver circuit is implemented below in Figure 5.6

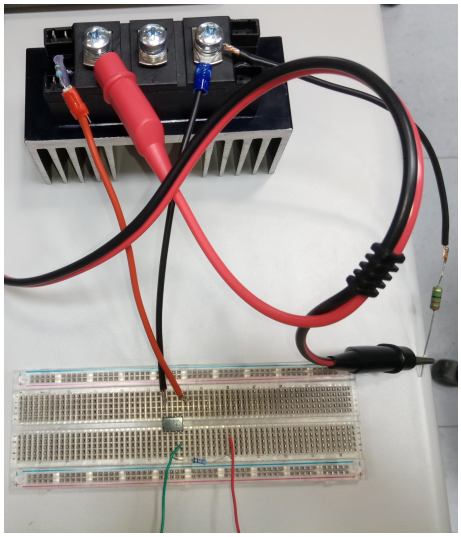

Figure 5.4: SCR gate driver based on optocoupler

5.7 IGBTs Driver Board

This PCB is a copy of the driving stage within the detection board. Its mission consists in driving the IGBTs. It uses a signal from an Arduino to control the on/off state of the IGBTS. The board design is shown below:

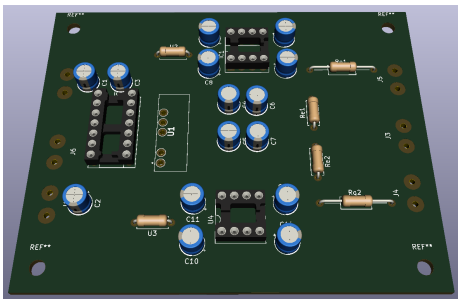

Figure 5.5: Design of the IGBT driver board

And the real implementation as well:

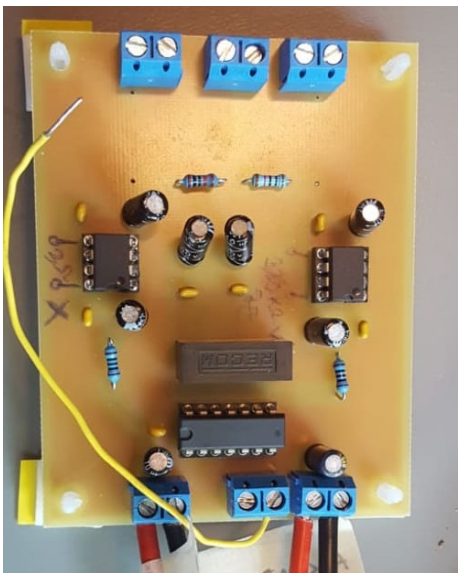

Figure 5.6: IGBT driver board. The green and yellow cables conduct the control signal from Arduino to the board.

The board schematic can be consulted in Appendix B.

5.8 RC Snubber Calculations

Hereby, R and C are calculated according to the derivation shown in Chapter 3 Figure 3.14.

So, the snubber resistor R_{sn} can be calculated by using 3.23:

$$R_{sn} = \frac{Overvoltage}{Current} = \frac{800}{40} = 20\Omega \tag{5.22}$$

The Overvoltage value is taken from the simulation - Figure 4.9. The snubber capacitor $C_{sn} = 10\mu$F satisfies the equation 3.26 as:

$$C > \frac{LI^2}{V_o^2} \tag{5.23}$$

$$10e-06 > \frac{(103e-6)(40)^2}{(800)^2} \implies 10e-06 > 2.5e-08 \tag{5.24}$$

5.8.1 RLC Series Circuit Impulse Response

The mathematical and simulated responses of the resulting RLC circuit when the IGBTs turn off are compared for the same initial values hereby.

- $R = 20$ Ohms
- $L = 103\mu$H
- $C = 10\mu$F

R and C were selected to provide a overdamped system with fast clearing time in the LTSpice simulation.

On the other hand, from the mathematical response obtained in Matlab it is seen that the voltage impulse response starts decaying from the peak value of 25 V and settles to 16 V in 10 ms. The current impulse response settles in 0.7 ms

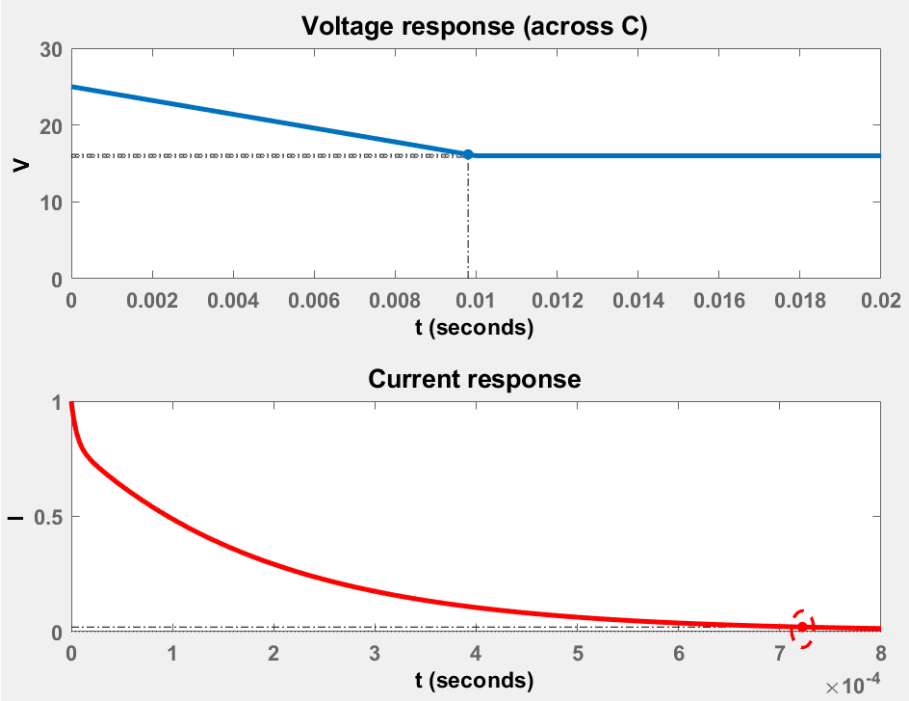

Figure 5.7: Impulse response of the RLC circuit

However, comparing with the simulation, the results does not match. It seems that two different things are being compared. Probably the way the fault is simulated is not regarded in the mathematical model. Also, the emulated fault in LTSpice may not have nothing to do with an unitary impulse.

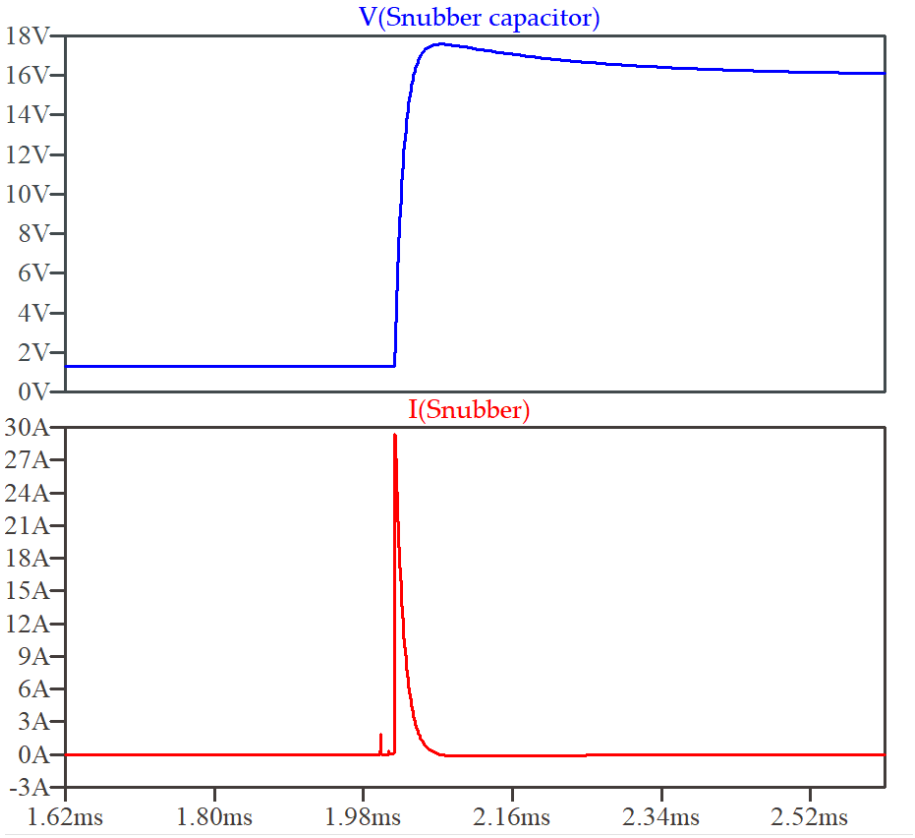

Figure 5.8: Response simulation of the CB (snubber branch)

5.9 Re-connection DC Relay

Due to safety concerns, a DC relay may be connected in series with the depicted breaker in order to provide a zero voltage differential when the breaker has tripped due to a fault. Such a way, safe access to the breaker is permitted if repairs are required. The relay is considered in the code as well.

5.10 Main Controller

A control program is coded in Arduino to perform the desired coordination strategy for the breaker switches (the same as in Chapter 4). The code can be found in Figure C.2 within the Appendix C.

5.11 Summary

In Chapter 5 a set of switches were chosen to develop minimum conduction losses. These ones were theoretically calculated according to the expressions derived in the background and with these values, the minimum heatsinks for each switch were calculated and installed.

Next, an available PCB used for fault detection as well as for driving the MOSFETs is presented.

A MOSFET power board is designed and manufactured. Continuing with the hardware, the IGBT and thyristor gate driver are calculated.

Finally the RC snubber is verified by calculation and the unitary impulse response for the equivalent RLC circuit is depicted. The Arduino program controlling the breaker switches is included as well.

Chapter 6

Experimental Tests

In this chapter both circuit breakers are tested under a steady-state current of 40 A and the same experimental fault. The first goal will consist of validating the mathematical models applied in the previous chapter. The second goal on the other side, elucidate the advantages and disadvantages of the Modern Breaker versus the IGBT breaker.

6.1 Test Bench

The same setup as shown in Chapter 4 is put together in the lab.

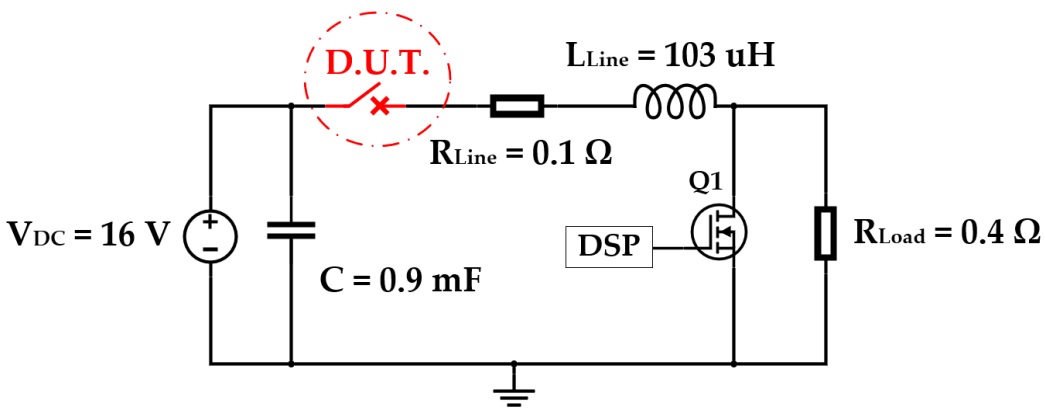

Figure 6.1: Common setup. In the red spot will be connected the corresponding circuit breaker under testing

6.2 Steady state test

For this experiment the device under test is set into conduction mode until the thermal equilibrium is reached. In that moment, the input and output powers are acquired with an oscilloscope to get breaker's losses and efficiency.
The equilibrium temperature will be written down to know how far is the equilibrium temperature from the the maximum admited temperature.

Conduction losses (experimental)

An oscilloscope (OSC) is used to acquire the instantaneous values of the voltage at input and output of the circuit breaker as well as the instantaneous current through the line. Hence, making use of the fundamental definition of average power [28]:

$$P = \frac{1}{T}\int_0^T v(t)i(t)dt \tag{6.1}$$

and the power loss script found in Appendix C, the experimental power losses and the efficiency will be obtained.

IGBT Breaker

6.2.1 D.U.T. - A, IGBT Breaker

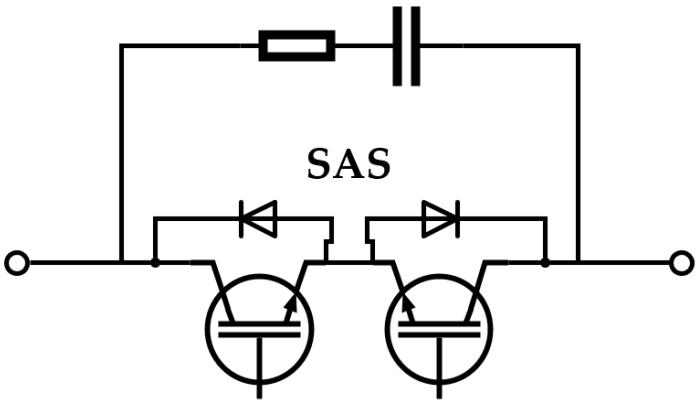

Figure 6.2: Power circuit of the IGBT Breaker

The operation junction temperatures were calculated from the T_C measurement at the thermal equilibrium. Since IGBT and diode voltage drop were close and the

case temperatures of both modules were almost the same, only one case temperature was acquired for both of the modules. The value obtained was T_C = 66°C. Given this measurement, the new junction temperatures are obtained as follows:

$$T_{J_I} = P_{loss_I} R_{JC_I} + T_C = 160\Delta 0.28 + 66 = 111^oC \tag{6.2}$$

$$T_{J_d} = P_{loss_d} R_{JC_d} + T_C = 160\Delta 0.42 + 66 = 133^oC \tag{6.3}$$

From the script the following results are obtained:

$$P_{loss} = 160W \tag{6.4}$$

$$\eta = 83.85\% \tag{6.5}$$

6.3 Modern Breaker (D.U.T. - B)

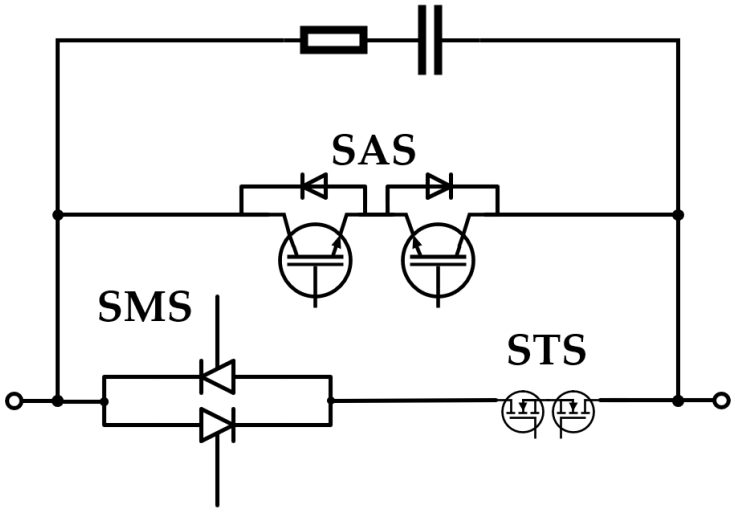

Figure 6.3: Power circuit of the Modern Breaker

6.4 Comparison table

DUT	P_{loss} (W)	η %
IGBT Breaker	160	83.85
Modern Breaker		

Chapter 7

Conclusions

As presented in the introduction of this project, numerous examples suggest that DC grid provides a more efficient management of the electric energy versus the present AC model. This fact sustains the interest on further developing DC circuit breakers which are necessary for ensuring safety and consistency of DC microgrids. Fuses cannot protect in the overvoltage range and mechanical switches require maintenance due to the arcing that takes place in the turn off. Also present slow clearing times.

Nonetheless, typical MOSFET/IGBTS SSCBs exhibit high on-state losses and if the voltage rating is elevated, the above-mentioned increase significantly. As a consequence, alternative topologies as the one occupying this project were investigated since they seem to improve it in a significant way. Thereby, the research question of this project was formulated.

In definitive, a topology satisfying two important motivations was found: 1) It reduces the conduction losses, 2) It increases the Voltage and Power levels.

For this project, the validation of the first is the nearest goal to reach due to the complexity of the topology. In that way, the low voltage approach was pursued from the beginning.

Special focus was set in finding a simple testbench: resistive load connected to a DC source through a line inductance. Also, availability to create faults in the order of few microseconds to test the reaction times of the breaker.

From Chapters 3 and 5, the conduction losses for the IGBT breaker where successfully obtained with reasonable deviation from theory to experiment. 150 W at $T_J = 175^oC$ vs 160 W at $T_J \approx 120^oC$, respectively.

In Chapter 4 the test circuit (a microgrid circuit) was properly modeled and a way to model faults was applied to obtain results under the desired conditions. Also, MOVs and RCD circuits were tested in the simulation. The overvoltage levels were not big so RCDs were utilized due to better dissipation results. MOVs merely worked in their active region due to the turn off of the IGBTs.

A coordination strategy consisting in a fast turn-off and turn-on of the MOSFET prevented the MOSFET from experience almost any overvoltage (5 V) while the thyristor got almost 900 V. Although the LTSpice simulation should be trustful, experimental validation has to be done to verify this.

Chapter 6 was not concluded due to component failures the week before the delivery date: 2 IGBTs and 2 DC/DCs. Nonetheless, the completion of the Chapter will be pursued until the oral exam. That means, to get the modern breaker experimental efficiency and compare it with the theoretically calculated. Secondly, obtain the relevant waveforms when clearing a DC fault for both IGBT and Modern Breaker.

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Appendix A

Datasheets

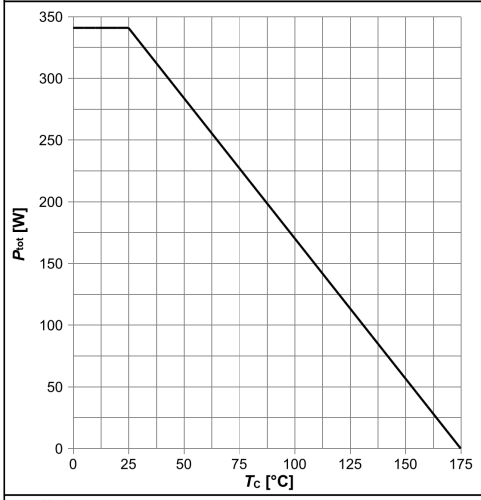
Hereby, the manufacturer diagrams from the selected power switches are extracted.

A.1 Discrete MOSFET

IR MOSFET - StrongIRFET™
IRF100P219

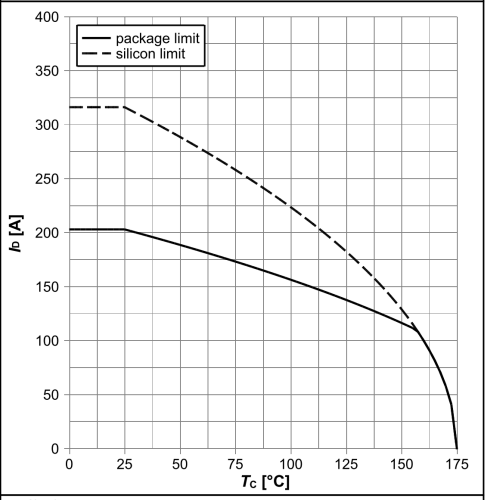
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



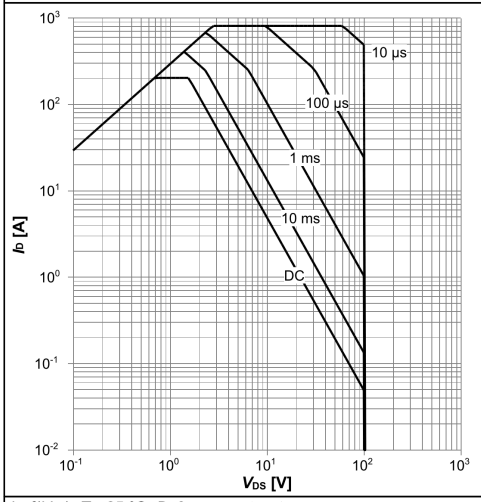
$P_{tot}=f(T_C)$

Diagram 2: Drain current



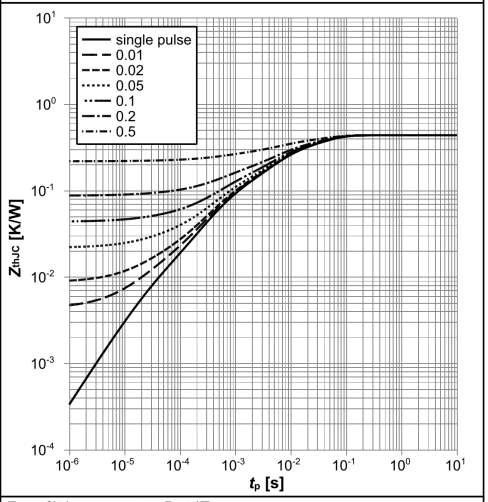
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

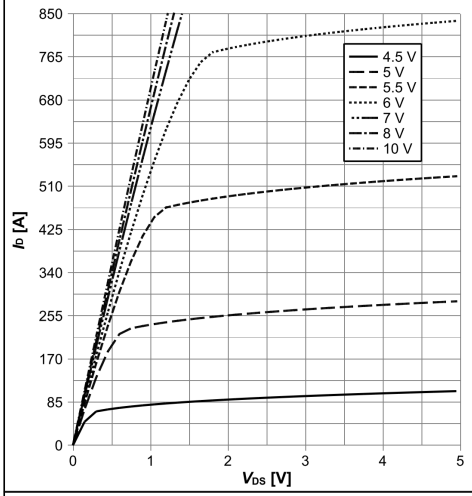
Diagram 4: Max. transient thermal impedance



$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

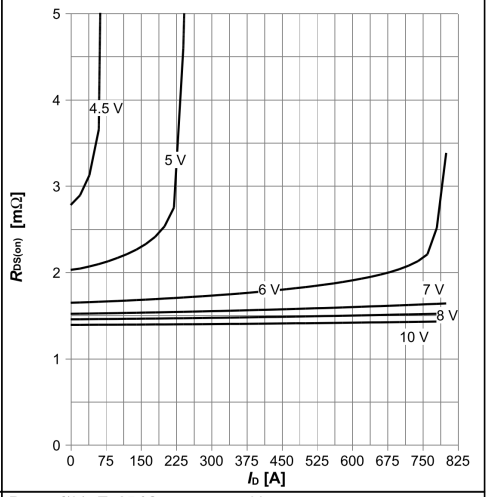
Figure A.1: Mosfet manufacturer diagram **[infineon_mosfet]**

Diagram 5: Typ. output characteristics



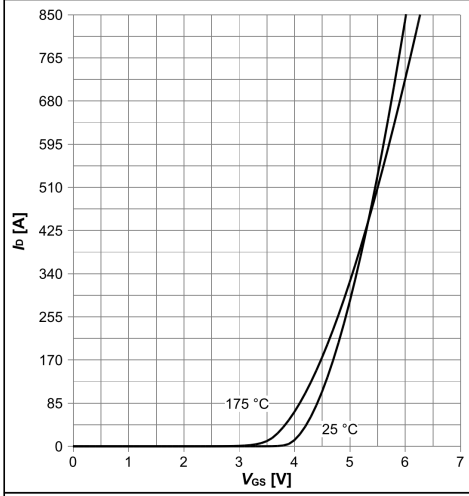
$I_D=f(V_{DS})$, T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



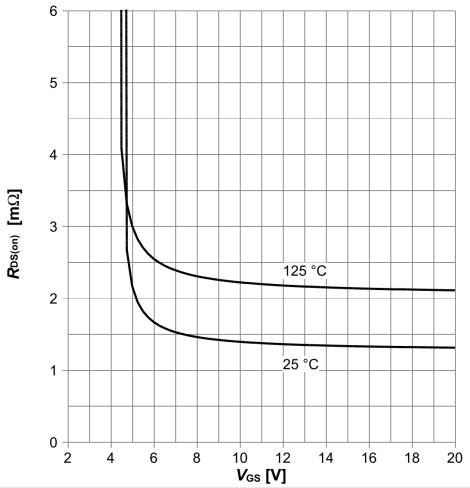
$R_{DS(on)}=f(I_D)$, T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



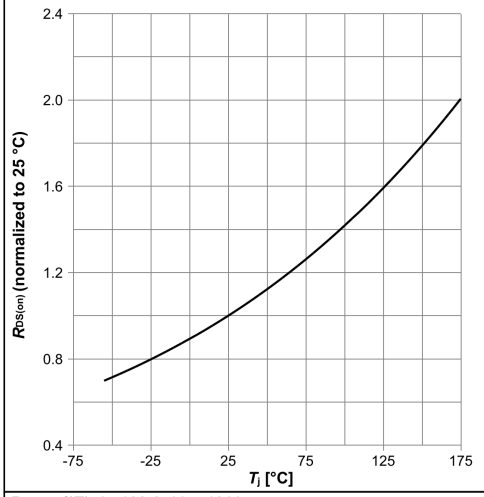
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



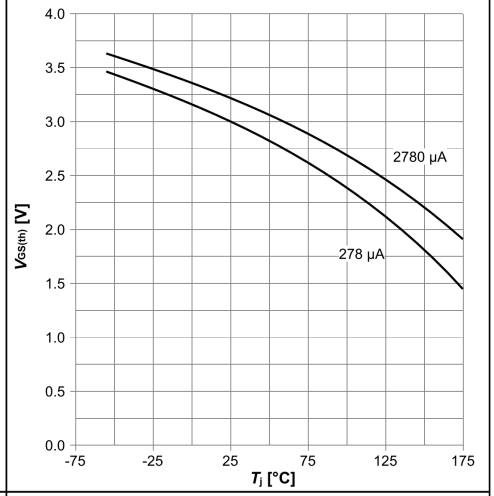
$R_{DS(on)}=f(V_{GS})$, I_D=100 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



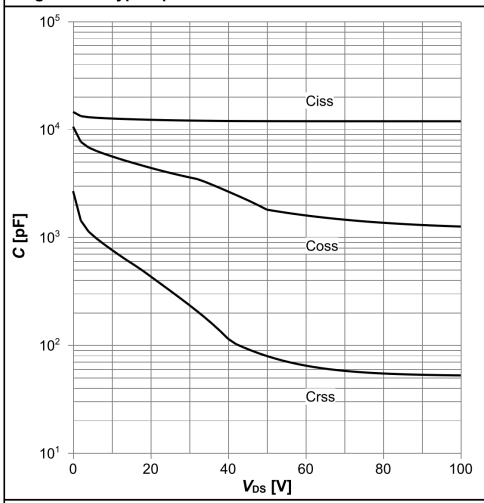
$R_{DS(on)}$=f(T_j), I_D=100 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



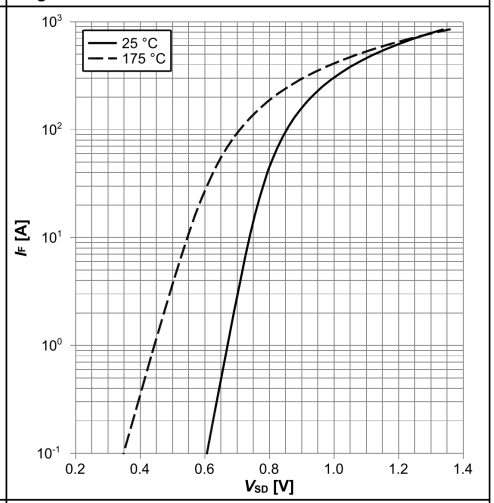
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



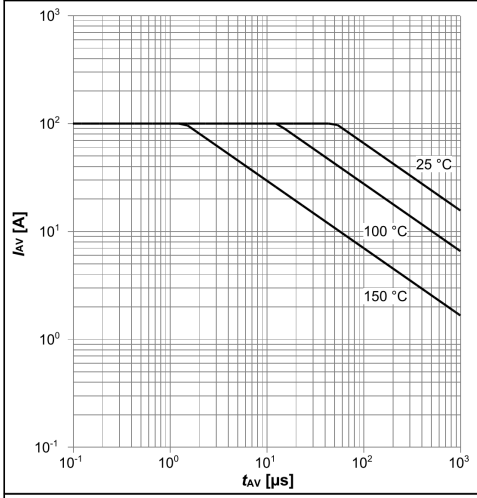
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



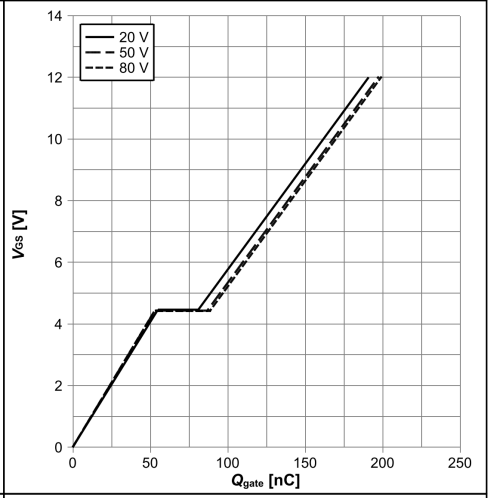
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



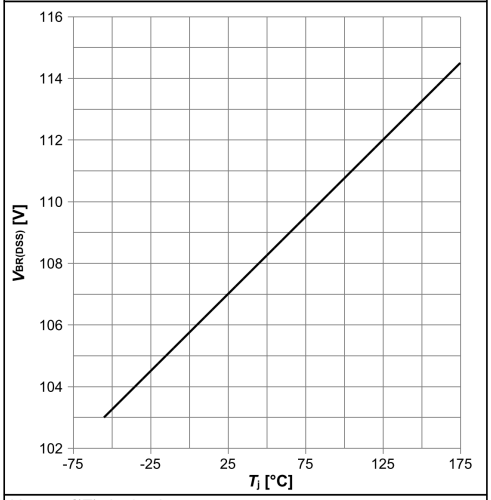
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



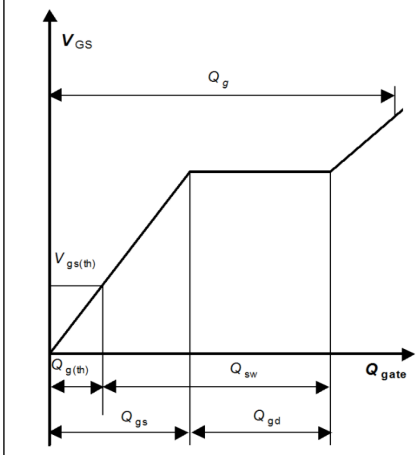
$V_{GS}=f(Q_{gate})$, $I_D=100$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



A.2 Anti-parallel thyristor module

IXYS **MCC162-18io1**

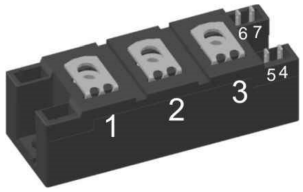
Thyristor Module

V_{RRM} = 2x 1800 V
I_{TAV} = 181 A
V_T = 1.03 V

Phase leg

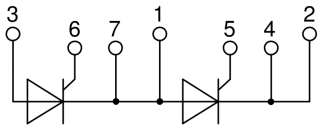
Part number

MCC162-18io1



Backside: isolated

E72873



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability
- Direct Copper Bonded Al2O3-ceramic

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: Y4

- Isolation Voltage: 3600 V~
- Industry standard outline
- RoHS compliant
- Soldering pins for PCB mounting
- Base plate: DCB ceramic
- Reduced weight
- Advanced power cycling

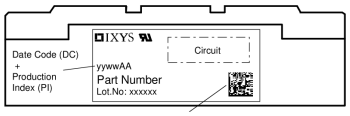
Figure A.2: Thyristor manufacturer diagrams [23]

IXYS **MCC162-18io1**

Thyristor				Ratings			
Symbol	Definition	Conditions		min.	typ.	max.	Unit
$V_{RSM/DSM}$	*max. non-repetitive reverse/forward blocking voltage*		T_{VJ} = 25°C			1900	V
$V_{RRM/DRM}$	*max. repetitive reverse/forward blocking voltage*		T_{VJ} = 25°C			1800	V
$I_{R/D}$	*reverse current, drain current*	$V_{R/D}$ = 1800 V	T_{VJ} = 25°C			300	µA
		$V_{R/D}$ = 1800 V	T_{VJ} = 125°C			10	mA
V_T	*forward voltage drop*	I_T = 150 A	T_{VJ} = 25°C			1.09	V
		I_T = 300 A				1.25	V
		I_T = 150 A	T_{VJ} = 125°C			1.03	V
		I_T = 300 A				1.25	V
I_{TAV}	*average forward current*	T_C = 85°C	T_{VJ} = 125°C			181	A
$I_{T(RMS)}$	*RMS forward current*	180° sine				300	A
V_{T0}	*threshold voltage* } *for power loss calculation only*		T_{VJ} = 125°C			0.88	V
r_T	*slope resistance* }					1.15	mΩ
R_{thJC}	*thermal resistance junction to case*					0.155	K/W
R_{thCH}	*thermal resistance case to heatsink*				0.070		K/W
P_{tot}	*total power dissipation*		T_C = 25°C			645	W
I_{TSM}	*max. forward surge current*	t = 10 ms; (50 Hz), sine	T_{VJ} = 45°C			6.00	kA
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			6.48	kA
		t = 10 ms; (50 Hz), sine	T_{VJ} = 125°C			5.10	kA
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			5.51	kA
I^2t	*value for fusing*	t = 10 ms; (50 Hz), sine	T_{VJ} = 45°C			180.0	kA²s
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			174.7	kA²s
		t = 10 ms; (50 Hz), sine	T_{VJ} = 125°C			130.1	kA²s
		t = 8,3 ms; (60 Hz), sine	V_R = 0 V			126.3	kA²s
C_J	*junction capacitance*	V_R = 400 V f = 1 MHz	T_{VJ} = 25°C		273		pF
P_{GM}	*max. gate power dissipation*	t_P = 30 µs	T_C = 125°C			120	W
		t_P = 500 µs				60	W
P_{GAV}	*average gate power dissipation*					8	W
$(di/dt)_{cr}$	*critical rate of rise of current*	T_{VJ} = 125 °C; f = 50 Hz repetitive,	I_T = 540 A			150	A/µs
		t_P = 200 µs; di_G/dt = 0.5 A/µs;					
		I_G = 0.5 A; V = ⅔ V_{DRM} non-repet.,	I_T = 180 A			500	A/µs
$(dv/dt)_{cr}$	*critical rate of rise of voltage*	V = ⅔ V_{DRM}	T_{VJ} = 125°C			1000	V/µs
		R_{GK} = ∞; method 1 (linear voltage rise)					
V_{GT}	*gate trigger voltage*	V_D = 6 V	T_{VJ} = 25°C			2.5	V
			T_{VJ} = -40°C			2.6	V
I_{GT}	*gate trigger current*	V_D = 6 V	T_{VJ} = 25°C			150	mA
			T_{VJ} = -40°C			200	mA
V_{GD}	*gate non-trigger voltage*	V_D = ⅔ V_{DRM}	T_{VJ} = 125°C			0.2	V
I_{GD}	*gate non-trigger current*					10	mA
I_L	*latching current*	t_p = 30 µs	T_{VJ} = 25°C			300	mA
		I_G = 0.5 A; di_G/dt = 0.5 A/µs					
I_H	*holding current*	V_D = 6 V R_{GK} = ∞	T_{VJ} = 25°C			200	mA
t_{gd}	*gate controlled delay time*	V_D = ½ V_{DRM}	T_{VJ} = 25°C			2	µs
		I_G = 0.5 A; di_G/dt = 0.5 A/µs					
t_q	*turn-off time*	V_R = 100 V; I_T = 300 A; V = ⅔ V_{DRM}	T_{VJ} = 100 °C		150		µs
		di/dt = 10 A/µs dv/dt = 20 V/µs	t_p = 200 µs				

IXYS **MCC162-18io1**

Package Y4				Ratings			
Symbol	**Definition**	**Conditions**		**min.**	**typ.**	**max.**	**Unit**
I_{RMS}	*RMS current*	per terminal				300	A
T_{VJ}	*virtual junction temperature*			-40		125	°C
T_{op}	*operation temperature*			-40		100	°C
T_{stg}	*storage temperature*			-40		125	°C
Weight					150		g
M_D	*mounting torque*			2.25		2.75	Nm
M_T	*terminal torque*			4.5		5.5	Nm
$d_{Spp/App}$	*creepage distance on surface | striking distance through air*	*terminal to terminal*	14.0	10.0			mm
$d_{Spb/Apb}$		*terminal to backside*	16.0	16.0			mm
V_{ISOL}	*isolation voltage*	t = 1 second	50/60 Hz, RMS; I_{ISOL} ≤ 1 mA	3600			V
		t = 1 minute		3000			V



Data Matrix: *part no.* (1-19), DC + *PI* (20-25), *lot.no.#* (26-31), *blank* (32), *serial no.#* (33-36)

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	MCC162-18io1	MCC162-18io1	Box	6	454613

Equivalent Circuits for Simulation ** on die level* T_{VJ} = 125 °C

Thyristor

$V_{0\,max}$	*threshold voltage*	0.88	V
$R_{0\,max}$	*slope resistance **	0.8	mΩ

Thyristor

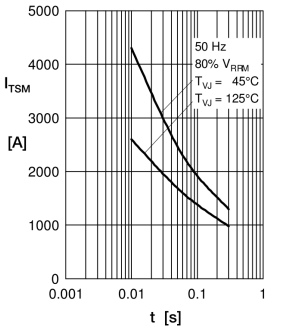


Fig. 1 Surge overload current I_{TSM}, I_{FSM}: Crest value, t: duration

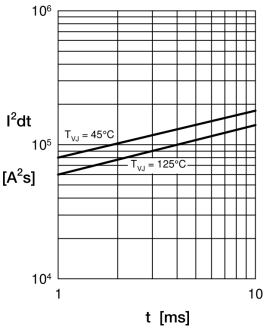


Fig. 2 I^2t versus time (1-10 ms)

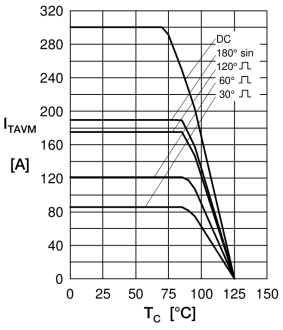


Fig. 3 Max. forward current at case temperature

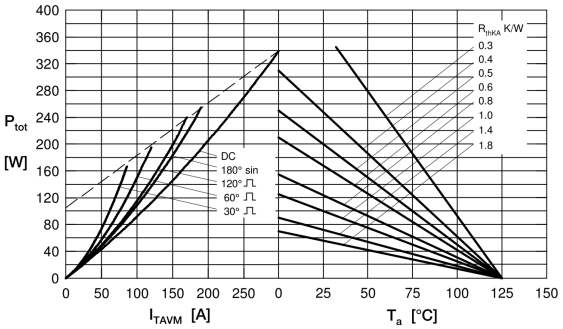


Fig. 4 Power dissipation vs. on-state current & ambient temperature (per thyristor or diode)

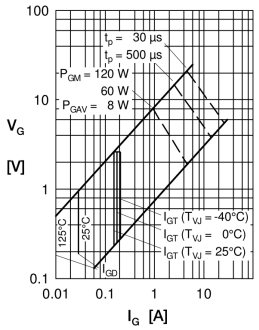


Fig. 5 Gate trigger characteristics

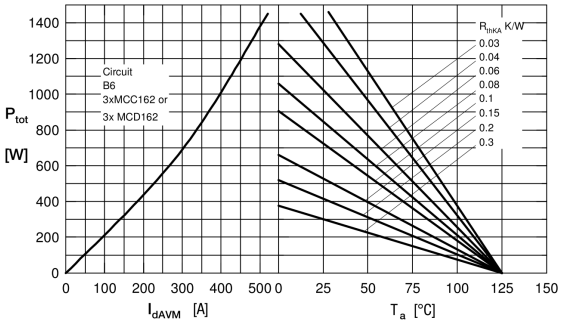


Fig. 6 Three phase rectifier bridge: Power dissipation versus direct output current and ambient temperature

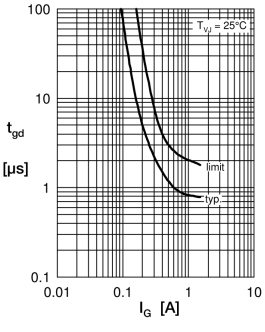


Fig. 7 Gate trigger delay time

Thyristor

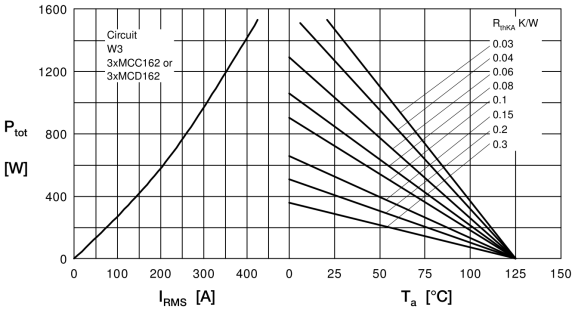
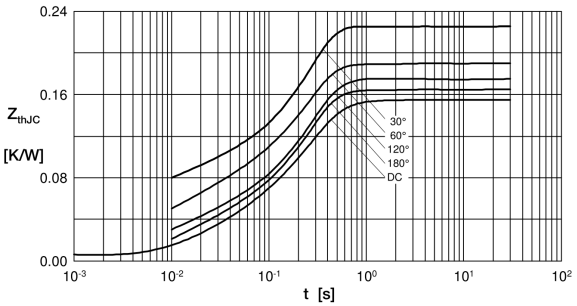


Fig. 8 Three phase AC-controller: Power dissipation versus RMS output current and ambient temperature



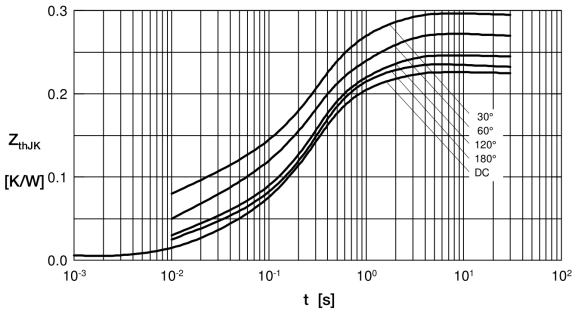
R_{thJC} for various conduction angles d:

d	R_{thJC} [K/W]
DC	0.155
180°	0.167
120°	0.176
60°	0.197
30°	0.227

Constants for Z_{thJC} calculation:

i	R_{thi} [K/W]	t_i [s]
1	0.0072	0.001
2	0.0188	0.080
3	0.1290	0.200

Fig. 9 Transient thermal impedance junction to case (per thyristor/diode)



R_{thJK} for various conduction angles d:

d	R_{thJK} [K/W]
DC	0.225
180°	0.237
120°	0.246
60°	0.267
30°	0.297

Constants for Z_{thJK} calculation:

i	R_{thi} [K/W]	t_i [s]
1	0.0072	0.001
2	0.0188	0.080
3	0.1290	0.200
4	0.0700	1.000

Fig. 10 Transient thermal impedance junction to heatsink (per thyristor/diode)

A.3 IGBT module

Typical Performance Curves **APT100GN120JDQ4**

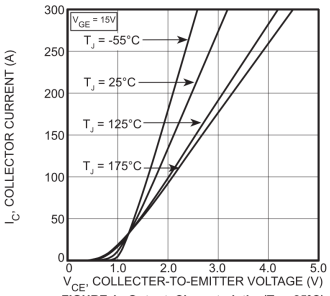


FIGURE 1, Output Characteristics(T_J = 25°C)

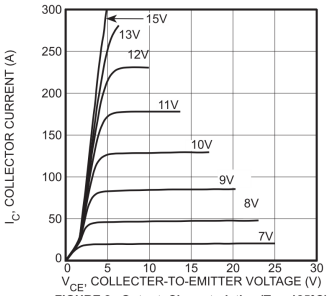


FIGURE 2, Output Characteristics (T_J = 125°C)

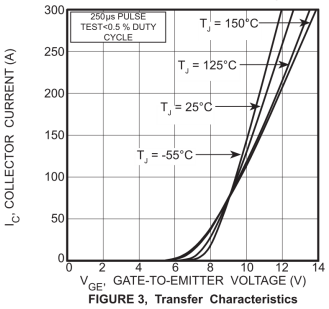


FIGURE 3, Transfer Characteristics

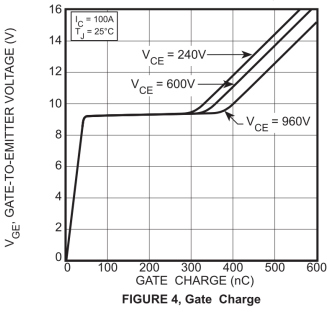


FIGURE 4, Gate Charge

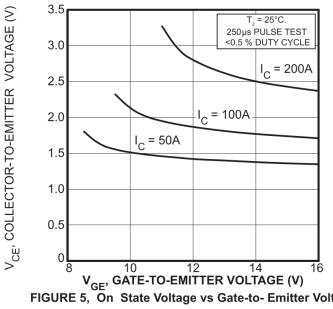


FIGURE 5, On State Voltage vs Gate-to- Emitter Voltage

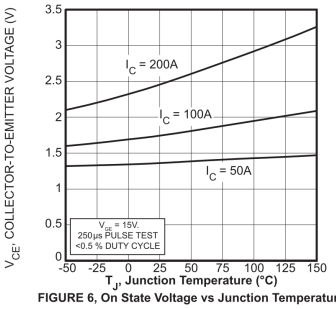


FIGURE 6, On State Voltage vs Junction Temperature

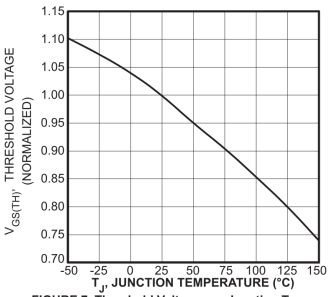


FIGURE 7, Threshold Voltage vs. Junction Temperature

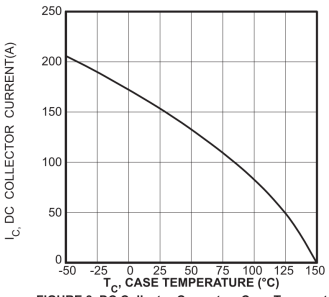


FIGURE 8, DC Collector Current vs Case Temperature

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Typical Performance Curves **APT100GN120JDQ4**

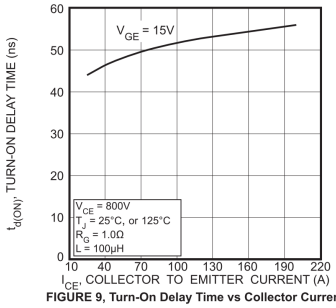

FIGURE 9, Turn-On Delay Time vs Collector Current

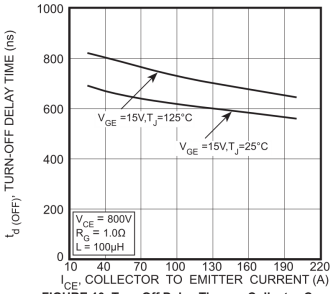

FIGURE 10, Turn-Off Delay Time vs Collector Current

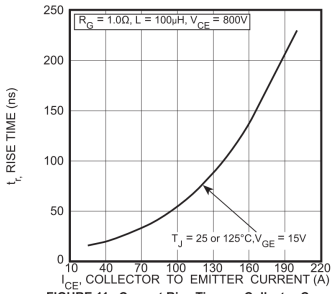

FIGURE 11, Current Rise Time vs Collector Current

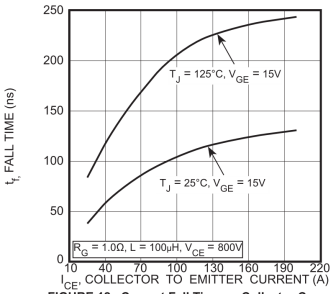

FIGURE 12, Current Fall Time vs Collector Current

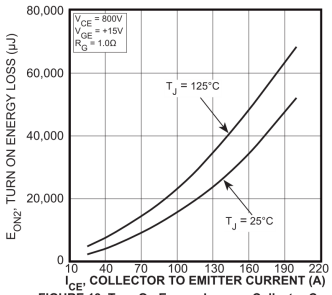

FIGURE 13, Turn-On Energy Loss vs Collector Current

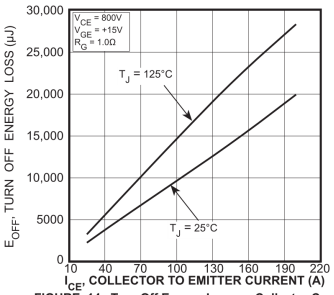

FIGURE 14, Turn Off Energy Loss vs Collector Current

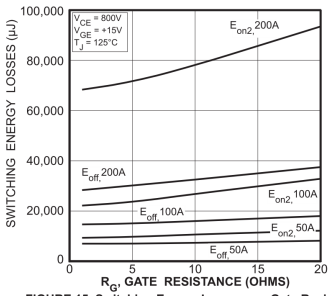

FIGURE 15, Switching Energy Losses vs. Gate Resistance

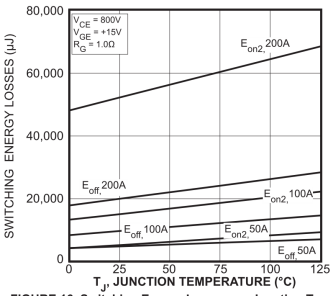

FIGURE 16, Switching Energy Losses vs Junction Temperature

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Typical Performance Curves **APT100GN120JDQ4**

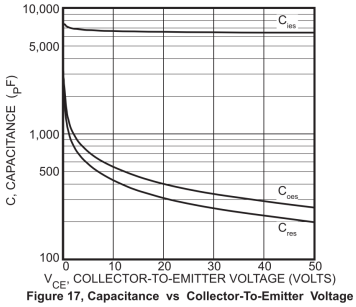

Figure 17, Capacitance vs Collector-To-Emitter Voltage

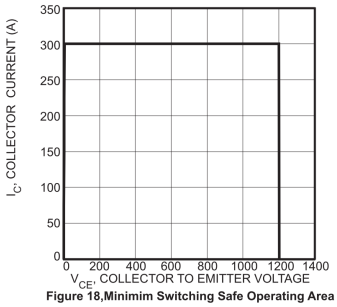

Figure 18,Minimim Switching Safe Operating Area

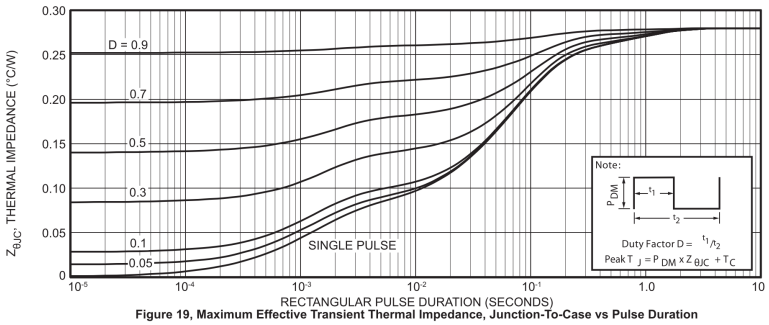

Figure 19, Maximum Effective Transient Thermal Impedance, Junction-To-Case vs Pulse Duration

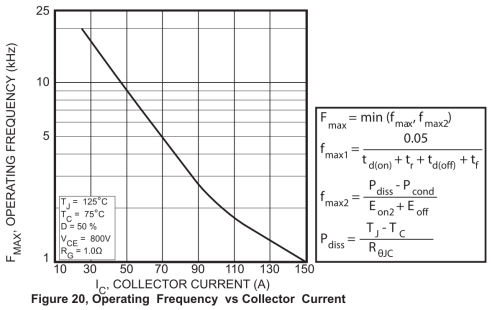

Figure 20, Operating Frequency vs Collector Current

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Typical Performance Curves **APT100GN120JDQ4**

ULTRAFAST SOFT RECOVERY ANTI-PARALLEL DIODE

MAXIMUM RATINGS All Ratings: T_C = 25°C unless otherwise specified.

Symbol	Characteristic / Test Conditions	APT100GN120JRDQ4	Unit
$I_{F(AV)}$	Maximum Average Forward Current (T_C = 88°C, Duty Cycle = 0.5)	100	Amps
$I_{F(RMS)}$	RMS Forward Current (Square wave, 50% duty)	127	
I_{FSM}	Non-Repetitive Forward Surge Current (T_J = 45°C, 8.3 ms)	1000	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions		Min	Type	Max	Unit
V_F	Forward Voltage	I_F = 100A		2.4	3.0	Volts
		I_F = 150A		2.65		
		I_F = 100A, T_J = 125°C		1.8		

DYNAMIC CHARACTERISTICS

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
t_{rr}	Reverse Recovery Time	I_F = 1A, di_F/dt = -100A/µs, V_R = 30V, T_J = 25°C	-	45	-	ns
t_{rr}	Reverse Recovery Time	I_F = 100A, di_F/dt = -200A/µs V_R = 800V, T_C = 25°C	-	385	-	
Q_{rr}	Reverse Recovery Charge		-	1055	-	nC
I_{RRM}	Maximum Reverse Recovery Current		-	6	-	Amps
t_{rr}	Reverse Recovery Time	I_F = 100A, di_F/dt = -200A/µs V_R = 800V, T_C = 125°C	-	480	-	ns
Q_{rr}	Reverse Recovery Charge		-	5240	-	nC
I_{RRM}	Maximum Reverse Recovery Current		-	19	-	Amps
t_{rr}	Reverse Recovery Time	I_F = 60A, di_F/dt = -1000A/µs V_R = 800V, T_C = 125°C	-	210	-	ns
Q_{rr}	Reverse Recovery Charge		-	9345	-	nC
I_{RRM}	Maximum Reverse Recovery Current		-	70	-	Amps

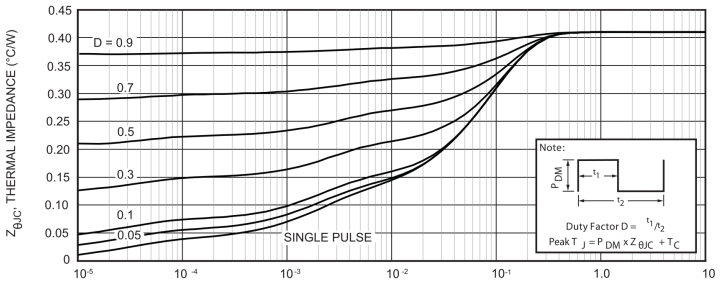

FIGURE 24. MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs. PULSE DURATION

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Typical Perfromance Curves **APT100GN120JDQ4**

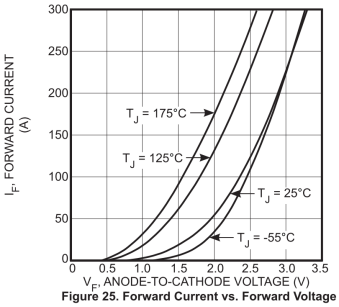

Figure 25. Forward Current vs. Forward Voltage

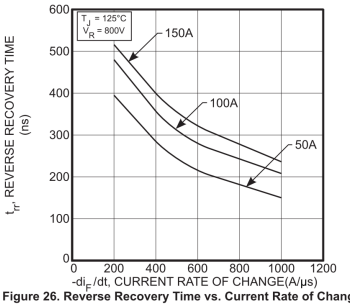

Figure 26. Reverse Recovery Time vs. Current Rate of Change

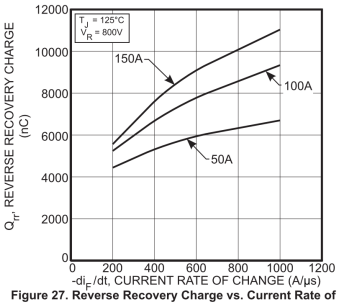

Figure 27. Reverse Recovery Charge vs. Current Rate of Change

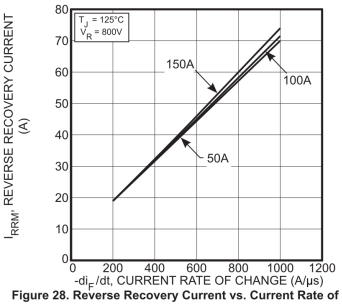

Figure 28. Reverse Recovery Current vs. Current Rate of Change

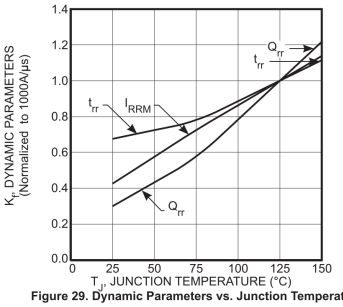

Figure 29. Dynamic Parameters vs. Junction Temperature

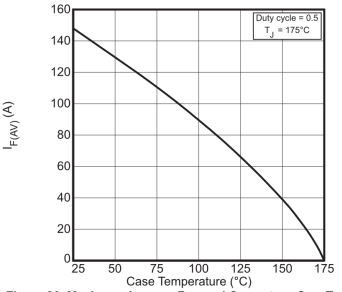

Figure 30. Maximum Average Forward Current vs. CaseTemperature

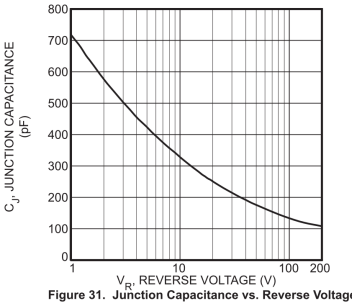

Figure 31. Junction Capacitance vs. Reverse Voltage

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A.4 Heatsinks

fischer elektronik

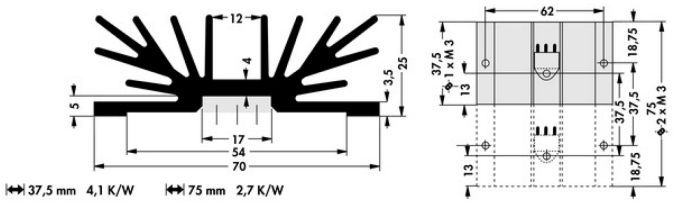
Data sheet Product SK 64 37,5 1 x M3 SA

Profile heatsinks and fluid coolers>Standard extruded heatsinks
70 x 25 mm, for transistor-designs TO 220 und TOP 3

Features

thermal resistance:	**2.7 - 4.1 K/W**
drilling pattern:	**1xM3**
surface:	**black anodised**
height:	**25 mm**
width:	**70 mm**
length:	**37.5 mm**
plate thickness:	**4 mm**

Technical Drawing



Fischer Elektronik GmbH & Co. KG
DEUTSCHLAND • GERMANY • ALLEMAGNE
Nottebohmstraße 28
58511 Lüdenscheid
Telefon +49 2351 435-0
Telefax +49 2351 45754
info@fischerelektronik.de
www.fischerelektronik.de

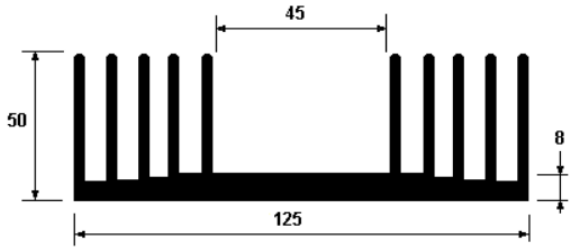
Figure A.3: Attached heatsink to the discrete Mosfets

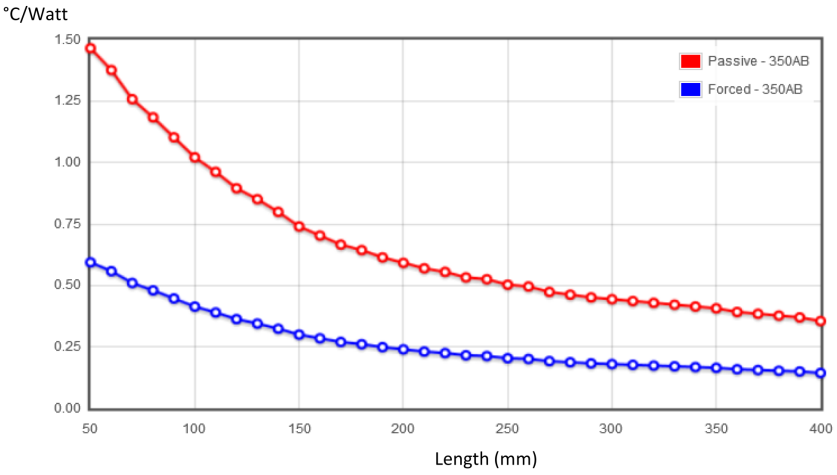
ABL
aluminium components

Telephone +44 (0) 121 789 8686
Fax (Sales) +44 (0) 121 789 8778
Fax (Admin) +44 (0) 121 789 9696

sales@ablcomponents.co.uk

350AB





Thermal Resistance is calculated based on a distributed heat load and vertically mounted fins anodised heatsink with a 60°C temperature.
Under general operating conditions the thermal mounting arrangement of the device is not know and therefore the figures should be used as a guide to selection.
We recommend that the effectiveness of any heatsink is tested in the specific operating environment in which it will be subjected.
Drawing above is for illustration purposes only. If any further information is required please contact us.

BS EN ISO 9001 : 2008

Figure A.4: Attached heatsink to the anti-parallel thyristor module

Appendix B

Schematics

B.1 Detection Board

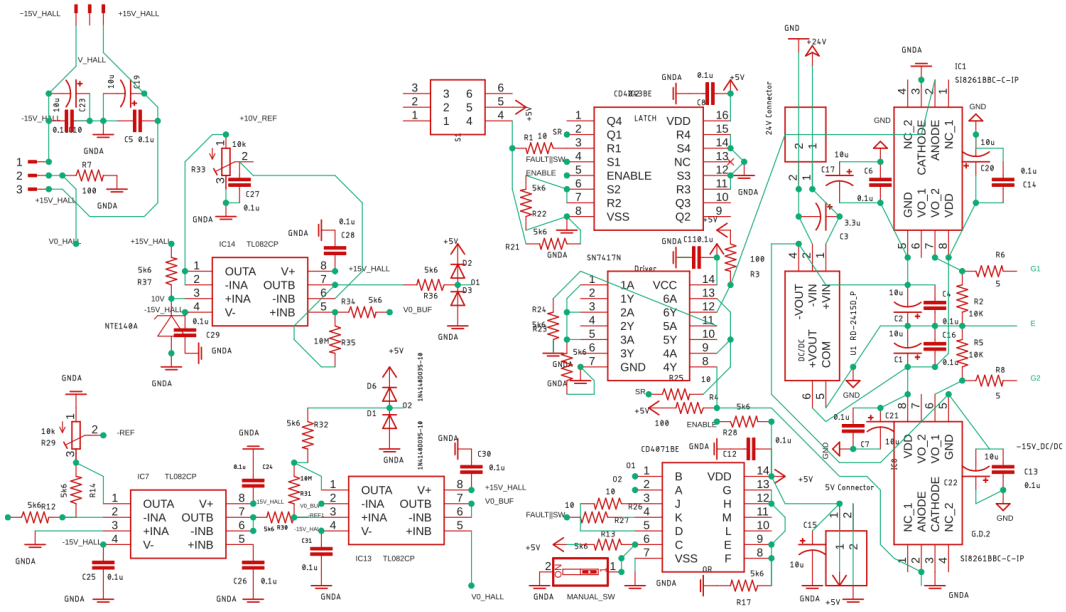


Figure B.1

B.2 IGBTs Driver Board

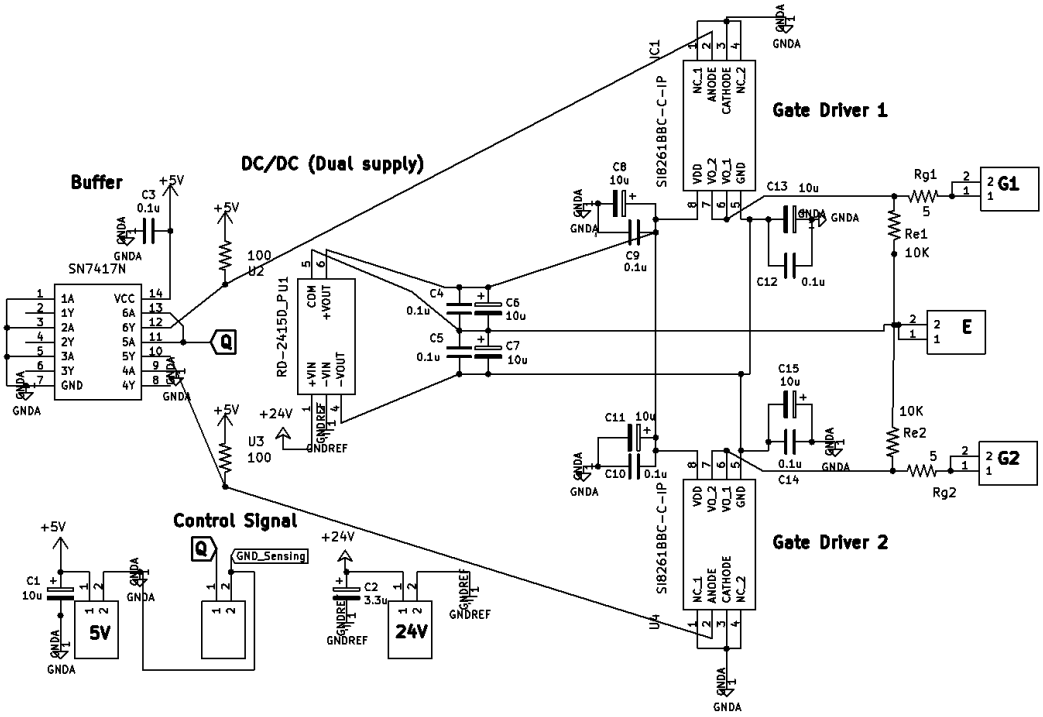


Figure B.2: Input Q corresponds to digital output 8 in Arduino board

Appendix C

Scripts

C.1 Power loss and Efficiency from OSC

```
clear all
clc
format long;
%Read csv file from row 17 col 0
Data = csvread('T0003ALL.csv',17,0);

%Extract all the data for t>=0. (t,input voltage, output voltage and
%current)

t=Data(:,1);t=t(t>0);
v1=Data(:,2);v1=v1(v1>0);
v2=Data(:,3);v2=v2(v2>0);
i=Data(:,4);i=i(i>0);

%Calculate input and output instantaneous powers
p1=v1.*i;
p2=v2.*i;

%Compute average input and output powers
P1=sum(p1)/length(t);
P2=sum(p2)/length(t);

%Ploss and Efficiency of the DUT
Ploss=P1-P2
ef_100=100*(P2/P1)
```

Figure C.1: Conduction losses and efficiency calculation from OSC data. Matlab M.file screen-shot

C.2 Modern Circuit Breaker ino

```
// Modern Circuit Breaker
// Author: Víctor Aragón Caminero
// 31-05-2019
#define READ(port,pin) ((PIN ## port & (1<<pin)) != 0)
#define SET(port,pin) PORT ## port |= (1<<pin)
#define CLEAR(port,pin) PORT ## port &= ~(1<<pin)

//Fault input
int faultPin=2;
int faultState=0;

//Turn on thyristor
int startChar = 0;
const int pulsePin = 5;// pin for the optocoupler pulse
int pulseState = 0;
long previousMicros = 0;
long pulsePeriod = 4;// 1us

//MOS and IGBT outputs
int pinMOS=9;
int pinIGBT=4;

void setup() {
  Serial.begin(9600);
  Serial.println("Press 1 to start-up the thyristor");
  pinMode(faultPin, INPUT);
  pinMode(pulsePin, OUTPUT);
  pinMode(pinMOS, OUTPUT);
  pinMode(pinIGBT, OUTPUT);
  attachInterrupt(digitalPinToInterrupt(faultPin),Fault,RISING);
}
```

Figure C.2: Arduino code for controlling the Modern Circuit Breaker - part1

```
void Fault()  //RISING edge interruption
{
  if(startChar==1)
  {
    faultState=1;
  }
}

void loop() {

  while(startChar!=1)
  {startChar=Serial.parseInt();}

  if(faultState==1){

    delayMicroseconds(4);
    SET(B,1);//reset MOSFET
    delayMicroseconds(8);
    CLEAR(B,0);//Give time enough to the MOSFET to turn on and clear the fault

    delayMicroseconds(25);//wait for the inductor to be discharged
    SET(D,3); //reset the rely (open mains)
    delay(5); //apply reset current for 5 ms (double winding latching relay) NO
    CLEAR(D,3); //stop the current

  }
```

Figure C.3: Arduino code for controlling the Modern Circuit Breaker - part2

```
  delayMicroseconds(25);//wait for the inductor to be discharged
  SET(D,3); //reset the rely (open mains)
  delay(5); //apply reset current for 5 ms (double winding latching relay) NO
  CLEAR(D,3); //stop the current

 }

 else{
 unsigned long currentMicros = micros();
 if(currentMicros - previousMicros > pulsePeriod) {
  previousMicros = currentMicros;
  if (pulseState == 0)
   { SET(D,4);        //Set the relay (close it)
     SET(B,1);        //Reset the MOSFETS
     SET(D,5);        //Turn on the Thyristor
   pulseState = 1;}
  else{
   CLEAR(D,4);       //stop the rely setting current
   CLEAR(B,1);       //stop MOSFET reset
   CLEAR(D,5);       //stop Thyristor gate pulse
     SET(B,0);}      //Turn on the IGBTs

  // pulseState = 0;}
   }
  }
}
```

Figure C.4: Arduino code for controlling the Modern Circuit Breaker - part3

Appendix D

RLC Response

D.0.1 Case 1: Over damped response

In the case of overdamped response, the characteristic equation has roots with distinct negative real parts. The transient solution of the overdamped system can be written as:

$$v_{tr}(t) = \left(A_1 e^{s_1 t} + A_2 e^{s_2 t}\right) \tag{D.1}$$

An overdamped system responds slowly to any changes in the input because the exponential terms with root s_1 decays to zero slowly as compared to second exponential term with root s_2. The value of the constant terms A_1 and A_2 can be found from the initial conditions of the system. The speed of the system response can be evaluated with damping ratio which is defined as:

$$\zeta = \frac{actual\ damping}{critical\ damping} = \frac{y}{2\sqrt{xz}} = \frac{\frac{R}{L}}{\frac{2}{\sqrt{LC}}} > 1 \tag{D.2}$$

To determine A_1 and A_2, the initials conditions $v_c(0)$ and $\frac{dv_c(0)}{dt}$ would be used. In any case:

$$v_c(0) = V_i \tag{D.3}$$

Where V_i is the initial source voltage.

$$\frac{dv_c(0)}{dt} = \frac{i_c(t)}{C} \tag{D.4}$$

The capacitor current $i_c(0)$ is not known necessarily since the capacitor current can change abruptly. However, in the case of series RLC circuit $i_c(t)$ is equal to inductor current $i_L(t)$ that cannot change abruptly.

So, the intial conditions can be evaluated as:

$$\frac{dv_c(t)}{dt} = \frac{i_L(t)}{C} \tag{D.5}$$

This condition is true for normal RLC series circuit that is excited with step voltage but in the case of CB the initial inductor current $i_L(t)$ before the turning off would be different than zero.

The final expression for $v_c(t)$ for over-damped system can be written as:

$$v_c(t) = (V_i - V_f)\left(\frac{e^{s_1 t}}{1 - \frac{s_1}{s_2}} + \frac{e^{s_2 t}}{1 - \frac{s_2}{s_1}}\right) + V_f \tag{D.6}$$

D.0.2 Case 2: Critically damped response

In this case, the roots of the characteristic equation are same with negative real parts which implies that the transient response of the system would be like:

$$v_{tr}(t) = (A_1 t + A_2)e^{st}, \;\; where\ s = -\frac{R}{2L} \tag{D.7}$$

The term $A_2 e^{st}$ decays exponentially with time and becomes zero as $t \to \infty$ but in the beginning, second term $A_1 t e^{st}$ starts to increase from its zero value to its maximum value and then finally decays to zero. This response is the quickest without any overshoot. The damping ratio in this case is:

$$\zeta = \frac{y}{2\sqrt{xz}} = \frac{\frac{R}{L}}{\frac{2}{\sqrt{LC}}} = 1 \tag{D.8}$$

The complete solution of critically damped system can be formulated as:

$$v_c(t) = (A_1 t + A_2)e^{st} + V_f \tag{D.9}$$

After using initial conditions to evaluate A_1 and A_2, equation D.9 becomes:

$$v_c(t) = (V_i - V_f)(1 + st)e^{st} + V_f \tag{D.10}$$

D.0.3 Case 3: Under damped response

For under damped response, the roots are complex conjugates which can be written as:

$$s_1 = \left(-\frac{R}{2L} + j\sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}\right) \tag{D.11}$$

$$s_1 = \left(-\alpha + j\sqrt{{\omega_0}^2 - \alpha^2}\right) = -\alpha + j\omega_d \tag{D.12}$$

$$s_2 = \left(-\frac{R}{2L} - j\sqrt{\frac{1}{LC} - \left(\frac{R}{2L}\right)^2}\right) \tag{D.13}$$

$$s_2 = \left(-\alpha - j\sqrt{{\omega_0}^2 - \alpha^2}\right) == -\alpha - j\omega_d \tag{D.14}$$

Where $\omega_d = \sqrt{{\omega_0}^2 - \alpha^2}$ is the damping frequency. In this case, damping ratio can be written as:

$$\zeta = \frac{\frac{R}{L}}{\frac{2}{\sqrt{LC}}} < 1 \tag{D.15}$$

The natural response of the system becomes:

$$v_{tr}(t) = \left(A_1 e^{s_1 t} + A_2 e^{s_2 t}\right) \tag{D.16}$$

$$v_{tr}(t) = A_1 e^{(-\alpha + j\omega_d)t} + A_2 e^{(-\alpha - j\omega_d)t} \tag{D.17}$$

After using the Euler's identity and further simplification, equation D.17 can be expressed as:

$$v_{tr}(t) = e^{-\alpha t}[(A1 + A_2)cos(\omega_d t) + j(A1 - A2)sin(\omega_d t)] \tag{D.18}$$

The total response of the system can be written as:

$$v_c(t) = e^{-\alpha t}[B_1 \cos(\omega_d t) + jB_2 \sin(\omega_d t)] + Vf \tag{D.19}$$

There exists oscillation in the response.The voltage changes from V_i to V_f, but wiggle back and forth few times in this process. The oscillation dies out according to the damping factor about over 5-time constants, where time constant $\tau = \frac{1}{\alpha}$. After evaluating the initial conditions to find out B_1 and B_2, the final system response can be written as:

$$v_c(t) = \left(V_i - V_f\right) e^{-\alpha t}[\cos(\omega_d t) + \frac{\alpha}{\omega_d} \sin(\omega_d t)] + Vf \tag{D.20}$$