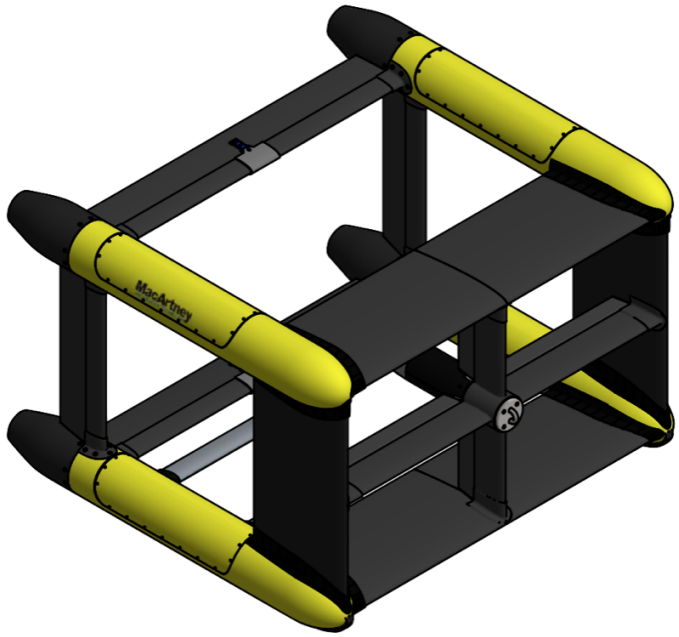
Design of a DC/DC Converter for Power Transmission to a ROTV

Power Convertion



Master Thesis Report by
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Abstract:

MacArtney A/S specialize in subsea technology and manufacture a Remote Operated Towed Vehicle (ROTV). The ROTV is powered through an tow cable, which can be up to 3,5 km long. Due to restrictions on MacArtney's current design, a shortage of power supplied to the ROTV is encountered. A new high step-down DC/DC converter is proposed, which will step 1000 V down to 48 and provide an output power of 1500 W. Converter topologies are compared and the Synchronous Buck Converter (SBC) is chosen. An extended analysis is carried out to determine parameter and component sizes. A more practical approach is carried out, to investigate the converters parasitic elements and challenges of the switching stage. Open-loop simulation is conducted in SPICE software, to investigate potential issues before physical implementation. Using an average model, a control unit is designed and simulation is conducted, which shows good transient behaviour as load and input voltage varies. In the experiment setup, many challenges where discovered, which led to multiple failures of MOSFETs and driver. The route of cause is expected to be parasitic elements in the prototype setup, and lag of protection of MOSFETs and driver. For future work, a Printed Circuit Board (PCB) must be considered.

Preface

This master thesis is written by Christian Lindquist. The project proposal is titled *Design of a DC/DC Converter for Power Transmission to a ROTV*. The project is written during the 4nd semester of the master degree in Offshore Energy Systems at Aalborg University Esbjerg (AAUE), 2019.

The author would like to extend a special thanks to MacArtney A/S and their electrical engineering department for providing resources for this project. The author hopes that the research conducted will be beneficial for the company.

The project is carried out to meet curriculum learning criteria. To meet these, the author seeks to implement knowledge from previous semesters and subjects.

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1 Introduction

1.1 Problem Description

MacArtney is a company that specializes in underwater technology with over 40 years of experience. The company produces and sells a variety of specialized and custom equipment to the industries of oil and gas, renewable energy, defense, civil engineering, and ocean science. One of MacArtney's products is a Remote Operated Towed Vehicle (ROTV), as can be seen in figure 1.1.

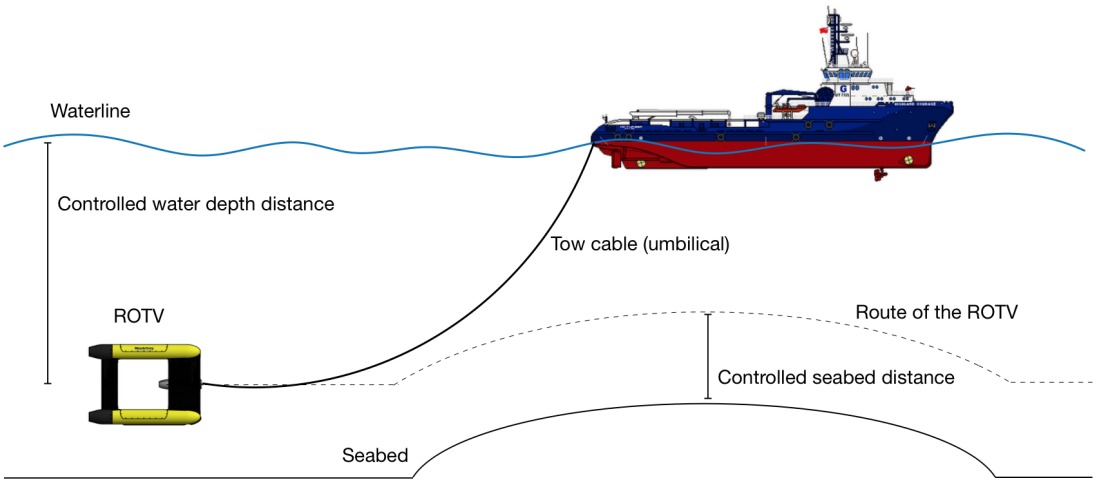


Figure 1.1: Operative principle of the ROTV (Not to scale) [1]

The ROTV is a specially designed platform which, as the name implies, is towed behind a marine vessel. Specialized sensors can be attached to the platform depending on the customer's needs. Two types exist, called FOCUS and TRIAXUS. A FOCUS vehicle is designed to stabilize itself at a controlled water depth or distance from the seabed. A TRIAXUS vehicle has an increased flaps area making it better for undulation within a water column. The ROTV is towed behind a marine vessel with a speed of 2-10 $knots$. The tow cable, called umbilical, is 2000-3500 m, depending on the type and operation.

MacArtney is experiencing problems with supplying enough power to the ROTV. Technological advancements in the sensors supplied by subcontractors create a higher power requirement. MacActney's existing equipment, which is based on a 30-year-old design, have a hard time keeping up with this power demand. Figure 1.2 illustrates the power transmission network to the ROTV.
Figure 1.2a illustrates the setup, where the topside provides DC power and fiber communication through a control unit to a winch. Through the winch, the power and fiber

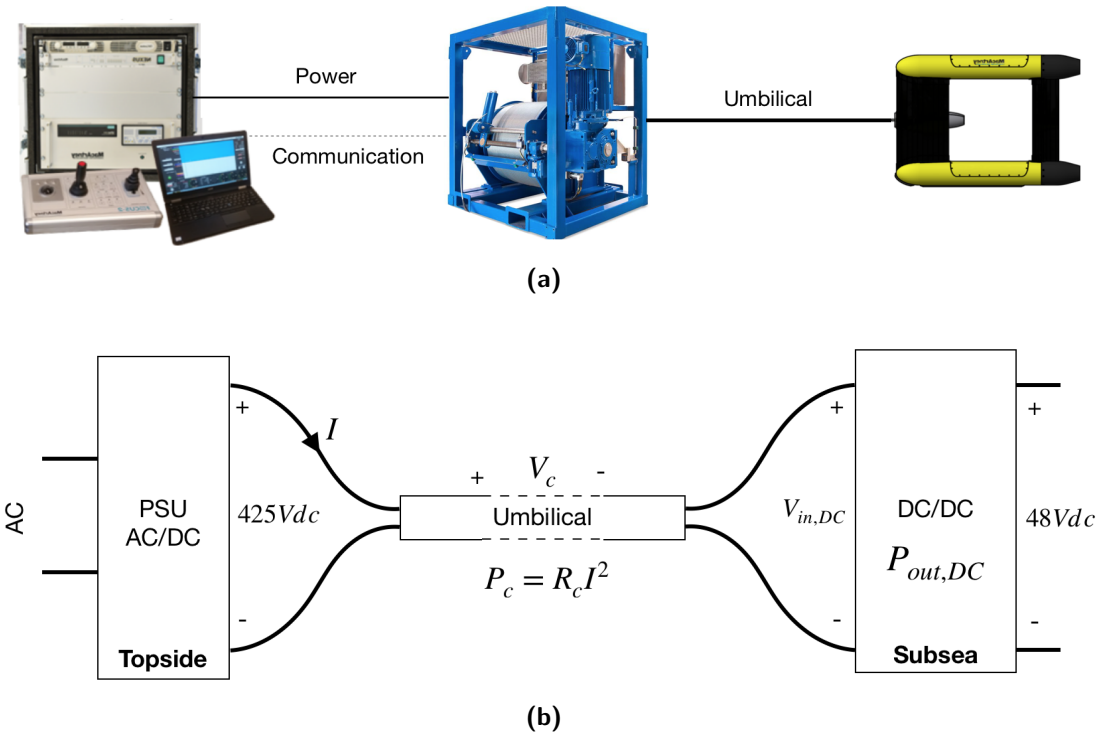


Figure 1.2: ROTV power transmission

are merged into the umbilical, and lastly connected to the ROTV. Following is a list of the present power transmission equipment.

Topside PSU: From Genesys TDK Gen600-2,6. It can deliver 600 V at 2,6 A, but is limited to 425 V. Other types are available which can supply a higher current.

Umbilical: MacArtney's fiber optic tow cable type 118440. It has an electrical DC resistance of $R_c = 13{,}5\ \Omega/km$.

DC/DC converter From Vicor, Maxi 375 V input (input DC voltage range 250-425 V) and output 48 V. It has 400 W of power at the output with an efficiency of $\eta_{maxi} =$ 87-88,3 %. Depending on power demand, multiple Maxi converters can be installed.

Figure 1.2b shows a block diagram of the power transmission. Today, the topside PSU DC voltage is limited to 425 V because the DC/DC converter subsea input voltage $V_{in,DC}$ can handle between 250-425 V. If a large load is connected to the DC/DC converter, it is possible that $V_{in,DC}$ will decrease to the value of 250 V. Using Ohm's law, the limitation of this setup is determined. Take note of the efficiency of the DC/DC converter.

$$V_{PSU} = V_c + V_{in,DC} = 2R_c Il + V_{in,DC} \qquad [V] \tag{1.1}$$

$$P_{DC/DC} = V_{in,DC} I\eta \qquad [W] \tag{1.2}$$

Setting V_{PSU} = 425 V, $V_{in,DC}$ = 250 V, R_c = 13,5 Ω/km, η = 0,87 and l = 2000 - 3500 m. The maximum available power can then be calculated with respect to the umbilical length (l) $P_{out,DC}$ = 705 - 403 W.

MacArtney is in search of a solution, which will give $P_{out,DC}$ = 1500 W to keep up with the demand. Nowadays, MacArtney uses a step-up step-down AC solution, but due to volume restrictions at subsea, this setup is not ideal.

Another solution, which is omitting the power transmission in the umbilical, is investigated in [1]. Here, energy is produced onboard the ROTV by extracting the kinetic energy in the water flow near the ROTV into electrical energy through use of water turbines. If the ROTV is towed through the water at high speed e.g. 10 $knots$, four small water turbines of 14 cm in diameter can produce over 1800 W of power. However, the same four turbines will only produce 14 W of power at 2 $knots$. The inconsistency of power production determined by the vessel speed is the biggest disadvantage of this technology.

A more consistent solution is to redesign the power transmission through the umbilical. One possibility is to design a custom DC/DC converter subsea, replacing the existing Vicor module. New parameters can then be determined specifically to fit MacArtney's equipment and needs. The output voltage must still remain at 48 V to power the mainboard, sensors, and other DC/DC converters, and it must be able to output 1500 W of power. The next parameter to determine is the input voltage $V_{in,DC}$. As the current in the umbilical introduces a voltage drop and power loss, limiting this parameter is beneficial. To keep the power constant, the voltage must increase. The voltage is limited by the existing hardware, such as the slip ring and the umbilical, which is both rated at 1000 V. The maximum V_{PSU} is then 1000 V. See the illustration of the new power transmission in figure 1.3.

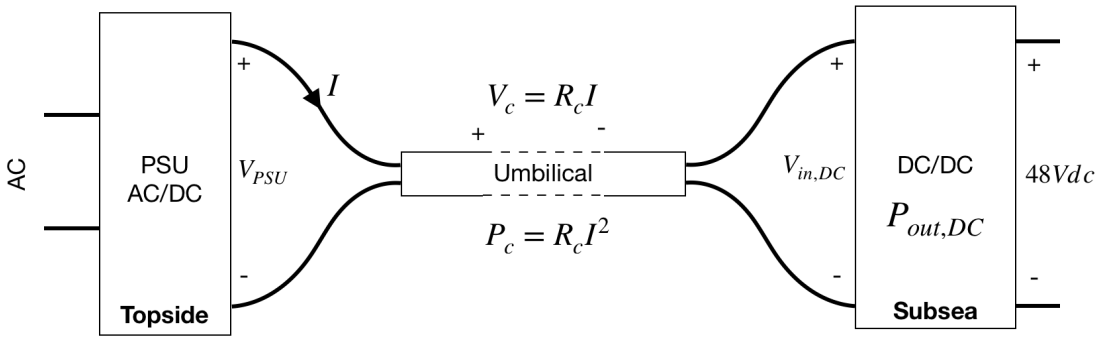


Figure 1.3: Proposed power transmission

With the given parameters, the DC/DC converter's specifications can be determined. When power demand $P_{out,DC}$ is low, current I is low and $V_{in,DC} = V_{PSU}$, but when $P_{out,DC}$ = 1500 W, the converter's input voltage can be calculated (using an arbitrary converter efficiency η = 90 % and l = 3500 m).

$$V_{PSU} = 2R_c lI + V_{in,DC} = 2R_c lI + \frac{P_{out,DC}}{I\eta} \quad \rightarrow \quad I = 2 \quad [A] \tag{1.3}$$

$$V_{in,DC} = V_{PSU} - 2R_c lI = 800 \qquad [V] \tag{1.4}$$

As variation in load changes the input voltage, the converter must be able to handle input voltage fluctuations as well as variation in load.

If interested the literature [1], is describing the power supply problem more thorough. The research is based around the same problem, but another solution is investigated.

1.2 Criteria

MacArtney has special criteria regarding design parameters. Some parameters are strict and must be prioritized. Following, is a list of criteria for the design of the converter.

I. It must be prioritized to design the converter to be as compact as possible.

II. Output voltage ripple should be less or equal to a Vicor converter. Its voltage ripple ΔV_o is typically 200 mV (see appendix A.1 for datasheet).

III. Efficiency is not a priority, which means that the topside power supply has unlimited power.

IV. The converter should be designed as a stand-alone unit, which can operate with and without the umbilical connected.

V. The converter should be designed for a maximum input voltage of 1000 V, an output voltage of 48 V, and output power ranging from 10-1500 W.

VI. The components must be "off-the-shelf" products.

1.3 Thesis Objective

The objective of this thesis is to design a 1000 V to 48 V step-down DC/DC converter. The converter must be able to maintain a constant output voltage under load and input voltage variation. It must deliver up to 1500 W of power at the output side. The chosen topology will be selected, analyzed, and simulated. During the design process, the size of the components will be determined and a full setup will be simulated and tested via experimental work.

1.4 Thesis Outline

The chapters are organized as following.

- Chapter 2 describe the topologies of step down converters.

- Chapter 3 analysis the synchronous buck converter's power stage.
- Chapter 4 describe the key factors in the switching stage.
- Chapter 5 determine the parameters and component size of the synchronous buck converter.
- Chapter 6 presents simulation in open-loop and shows possible challenges of the switching stage.
- Chapter 7 describe the control design methods and derive an average model.
- Chapter 8 presents closed-loop simulation at transient response.
- Chapter 9 presents the experimental setup and the experiments conducted.

1.5 Tools

MATLAB, Simulink, and LTspice are used as calculation and simulation tools. LTspice is a Simulation Program with Integrated Circuit Emphasis (SPICE) software that enables analog circuit simulations, and it is used to verify the open-loop response. It can implement models of semiconductors to make a more accurate simulation. Simulink offers good control simulation when verifying the closed-loop system.

2 Step-Down DC/DC Converters

This chapter describes the basic principles of a step-down converter and presents different topologies.

2.1 Converter Operation Principles

A converter in terms of power electronics is a module or piece of hardware that transforms a given input to a regulated output. It can also be referred to as a power supply. In electronics, the conversion parameter is typically stated e.g. AC/AC, AC/DC, DC/AC, or DC/DC. For a step-down DC/DC converter, two types exist.

The first one is a linear regulator, which is illustrated in figure 2.1. It consists of a transistor which controls the current I_o, resulting in a regulated voltage across the load R_o. In principle, a linear regulator works as a voltage divider, where the V_{CE} sets the output voltage $V_o = V_i - V_{CE}$.

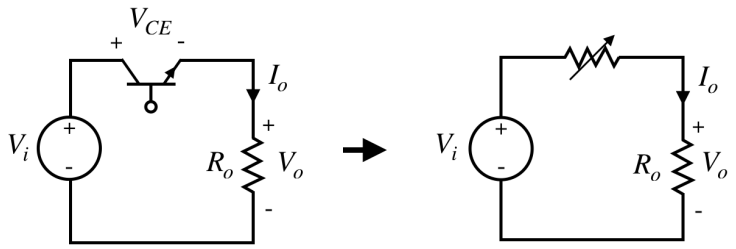


Figure 2.1: Linear regulator

The biggest drawback of a linear regulator is its inefficiency since power absorbed by the load is given as $V_o I_o$, and power absorbed in the transistor is $V_{CE} I_o$. If the step-down ratio increases, the efficiency decreases. Because of the low efficiency, the linear regulator is typically only used for output power below 25 W [2][3], which cannot fulfill the given criteria.

The second type is called a Switch Mode Power Supply (SMPS), which typically has a much higher efficiency [2][3]. A basic SMPS is illustrated in figure 2.2. Connected in series with the load is a switch $S1$, typically a power semiconductor, which is able to connect and disconnect the power source to the load. This sequence, with a constant frequency, is called Pulse Width Modulation (PWM). It is indicated by the blue line in figure 2.2, assuming an ideal switch.

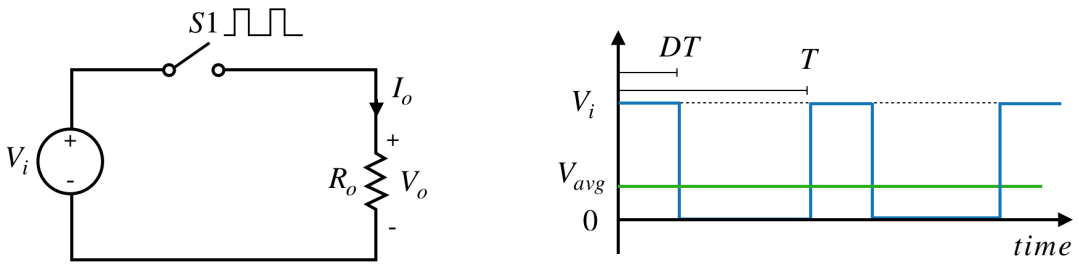


Figure 2.2: Circuit illustration of SMPS

The average voltage across the load will be determined by the width of the pulse, called the duty cycle $D = t_{on}/T$. Theoretically, D can range from 0 to 1. T is the period of one cycle, where the switching frequency can be found by $f = 1/T$. From the duty cycle, the average voltage can be determined by $V_{avg} = DV_i$.

The circuit in figure 2.2 is not compatible with all electronic devices because of the pulsed output voltage. Some electronic devices are sensitive to voltage fluctuation. As a solution, a low-pass filter can be connected after the switch, consisting of an inductor and capacitor, see figure 2.3.

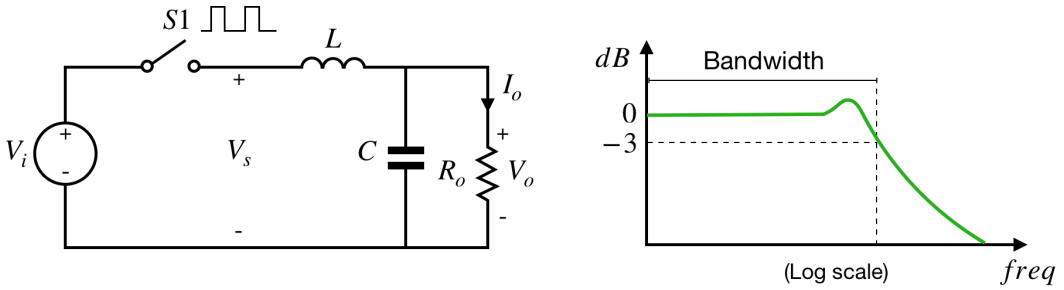


Figure 2.3: Circuit illustration of SMPS with LC filter

The $L - C - R$ circuit purpose is to smooth out the pulsed input signal to the filter, providing a steady low voltage ripple as output. The circuit forms a second-order system with the following transfer function.

$$\frac{V_o(s)}{V_s(s)} = \frac{1/LC}{s^2 + (1/R_oC)s + 1/LC} \tag{2.1}$$

The corresponding bode diagram is illustrated in figure 2.3. The sizes of L and C determine the crossover frequency of the system, which is closely related to the bandwidth. In this case, the bandwidth is where the system's frequency response crosses -3 dB, equivalent to an approximate decrease of 30 % in amplitude and 50 % in power.

The circuit illustrated in figure 2.3 is at risk of not functioning properly and introduces some dangerous voltage spikes. The inductor is resisting the current flow through itself, and sudden current changes induces voltage spikes, seen by its governing equation.

$$V_L = L\frac{di_L}{dt} = L\frac{\Delta i_l}{\Delta t} \tag{2.2}$$

When switch $S1$ turns OFF and disconnect the current flow, Δi_l increases, while Δt is small. This introduces a large voltage drop across the inductor, and $V_L \to \infty$. A solution to this is to generate another current path when $S1$ turns OFF. in figure 2.4, a diode is added to generate this path.

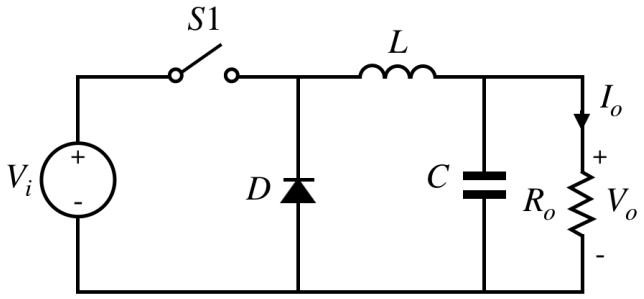


Figure 2.4: Circuit illustration of basic buck converter

Whenever $S1$ turns OFF, the diode becomes forward-biased, and it allows the current to flow through it. The figure illustrates the circuit of the most simple step-down converter, also called a buck converter. Ideally, the average output V_o can be directly derived by the duty cycle. The voltage conversion ratio of M can be determined.

$$M = \frac{V_o}{V_i} = D \qquad [V] \tag{2.3}$$

2.2 Step-Down Converter Topologies

Advancements in electronic devices and processors have caused an increase in popularity of the DC/DC converters. Due to their simple design and well-known dynamics, it is the preferred power supply unit. Within the field of DC/DC converters, there exists a research area for high step-down converters. Their main objective is to improve efficiency and extend the duty cycle at the lower end, resulting in an increase in control margin. Literature [4] and [5] present some of the different topologies for a high step-down converter. Some of them are very similar to the simple buck converter presented in section 2.1. In [4], an improved interleaved converter is presented. It reduces voltage stress and improves efficiency, but it also adds components and complexity to the converter. Its structure also extends the duty cycle. In [5], several one-switch topologies are presented. Two of the converter circuits are illustrated in figure 2.5 and figure 2.6.
The converters have extended the duty cycle, specially designed for high step-down converters. The voltage conversion ratio is presented in the figure caption. Eight different topologies are compared in [4], where figure 2.5 have a voltage conversion ratio close the conventional buck converter in figure 2.4. The circuit in figure 2.6 has the most extended voltage conversion ratio. The voltage conversion ratio over duty cycle is illustrated in figure 2.7.

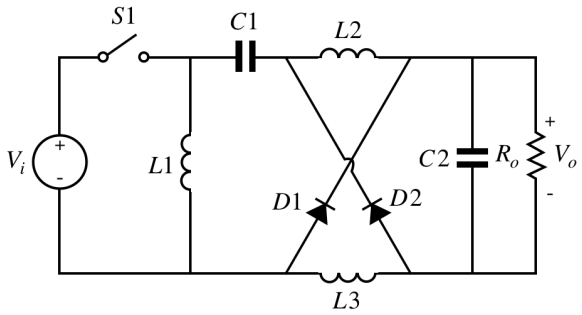


Figure 2.5: Quadratic-buck converter $M = \frac{D}{2(1-D)}$

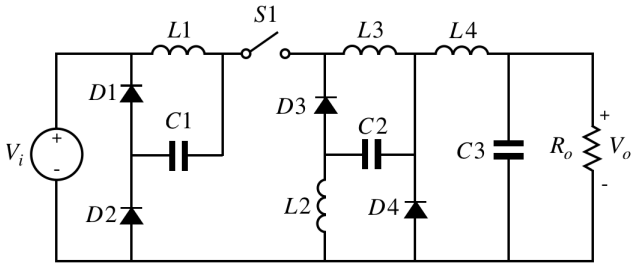


Figure 2.6: Quadratic modified Zeta converter $M = \frac{D^2}{2-D}$

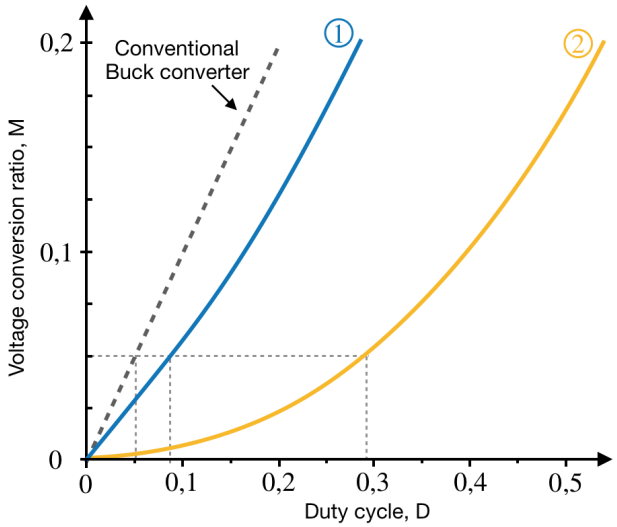


Figure 2.7: Voltage conversion over duty cycle. ① is figure 2.5 and ② is figure 2.6

For a voltage conversion of approximately 5 % ($48/1000 = 4,8$), the duty cycle can be extended from 5 % of a conventional buck converter to approximately 10 % of the circuit using the converter depicted in figure 2.5 or even to approximately 30 % with the circuit in figure 2.6. The extended duty cycle is preferable to an increased control margin, but it comes with a cost of circuit complexity and added components.

A simulation is conducted where the topologies are compared. The parameters are V_i = 42 V, V_o = 5 V and P_o = 50 W. For the circuit in figure 2.5 this resulted in an efficiency of 87,8 %, and for the circuit in figure 2.6 an efficiency of 84,5 % is determined.

The topologies from [4] are only analyzed in Continuous Conduction Mode (CCM), which is where the current in the inductors always flows. In Discontinuous Conduction Mode (DCM) the current falls to zero during one switching period and stays at zero before another period begins, see figure 2.8. This typically occurs at light loads.

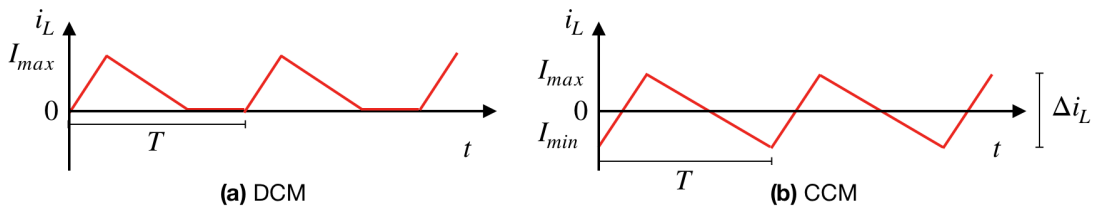


Figure 2.8: Two operation modes of a converter. Discontinuous Conduction Mode (DCM) (a) and Continuous Conduction Mode (CCM) (b)

Switching between the two modes can complicate control as the dynamics of the system changes, and in the conventional buck converter, the duty cycle decreases. Converters are typically designed to stay in CCM, which results in minimum sizes for the inductor, which with high current ratings can be difficult to find.

A solution is to have a controllable transistor instead of a diode, which also allows the current in the inductor to flow in the other direction (negative) as shown in figure 2.8(b). For the topologies in [4], a deeper analysis must be carried out, to determine which topologies can take advantages of this modification. This thesis will not investigate these modifications.

An alternative solution is called a Synchronous Buck Converter (SBC). This is basically a conventional buck converter but the diode is replaced with a controllable transistor. This topology utilizes the minimum components required and as it always operates in CCM, the control is simple for a wide load range. The disadvantage is that is suffering from high voltage and currents stresses and minimal control margin. In [6], the SBC is compared against the conventional buck converter and an isolated buck converter. The SBC shows high efficiency at light loads but decreases with a deeper slope compared to the other topologies mentioned. The efficiency is around 97 % at 50 W and 94 % at 350 W.

As stated in section 1.2, criteria I is to design a compact converter. The SBC is chosen, because of its simplicity, fewer component and that it operates in CCM at all time.

2.3 The Synchronous Buck Converter

The SBC has become popular in high power low voltage applications because a semiconductor has a much lower voltage drop compared to a diode [7][3]. This is due to

semiconductors' low ON resistance $R_{DS,ON}$. It makes for a more efficient converter, and it also simplifies the dynamics of the circuit because it stays in CCM. Figure 2.9 illustrates a SBC. The disadvantage is that it has lower efficiency at light loads due to the negative current [7][2].

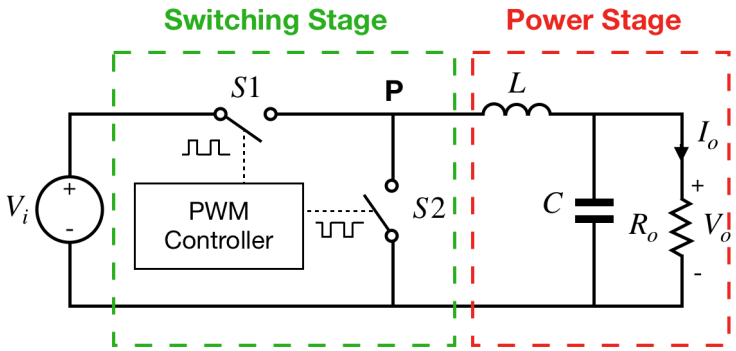


Figure 2.9: Illustration of the synchronous buck converter

When analyzing, the converter is split up into two stages, referred to as switching and power stage. The power stage is the low-pass filter explained in section 2.1. The switching stage will be described in chapter 4.

3 Power Stage

Throughout this chapter, an ideal and practical analysis of the power stage is carried out. This involves investigating the behavior of the inductor and capacitor and determining the equations to estimate their size.

3.1 Ideal Analysis

In an ideal analysis, the following assumptions are made [3][2]:

- The circuit is operated in steady state.
- The switches are ideal, meaning that note P of the circuit in figure 2.9 is a perfect square wave.
- Switching losses are negligible.
- Passive components are linear.

The analysis is carried out by analyzing the circuit in two stages. First, when $S1$ is ON and $S2$ OFF, from $0 < t < DT$, see figure 3.1(a). Second, when $S1$ is OFF and $S2$ ON, from $DT < t < T$ see figure 3.1(b)

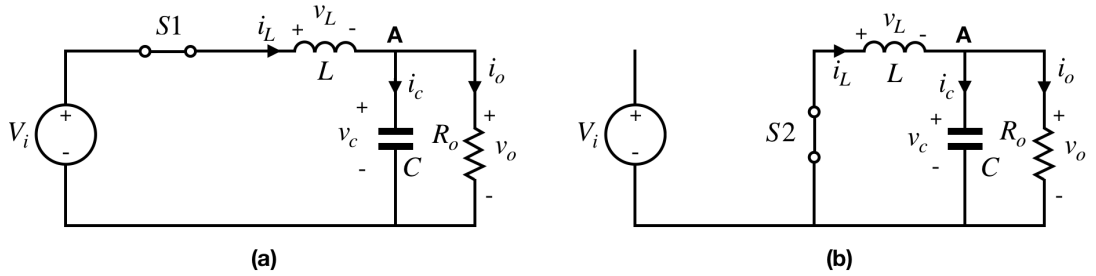


Figure 3.1: Equivalent circuit for switch $S1$ ON (a) and OFF (b)

3.1.1 Analysis Through the Inductor Current

The analysis is carried out by investigating the current ripple in the inductor. In steady state, the inductor average voltage and net current are zero.

0 < t < DT:

Using the Kirchhoff's Voltage Law (KVL) in the circuit in figure 3.1(a).

$$V_i = v_L + V_o = L\frac{di_l}{dt} + V_o \qquad [V] \tag{3.1}$$

The equation can be rearranged to express the change in current in the inductor over time.

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} = \frac{V_i - V_o}{L} \tag{3.2}$$

Because $V_i > V_o$, the current will positively increase over the time $\Delta t = DT$, see figure 3.2. The values of V_i, V_o, and L determine the slope of the current.

Eq. (3.2) can be expressed as the change in current.

$$(\Delta i_L)_{rise} = \left(\frac{V_i - V_o}{L}\right) DT \tag{3.3}$$

With a fixed slope, the only parameter that can change the amplitude of the current ripple is the ON time, seen in eq. (3.3).

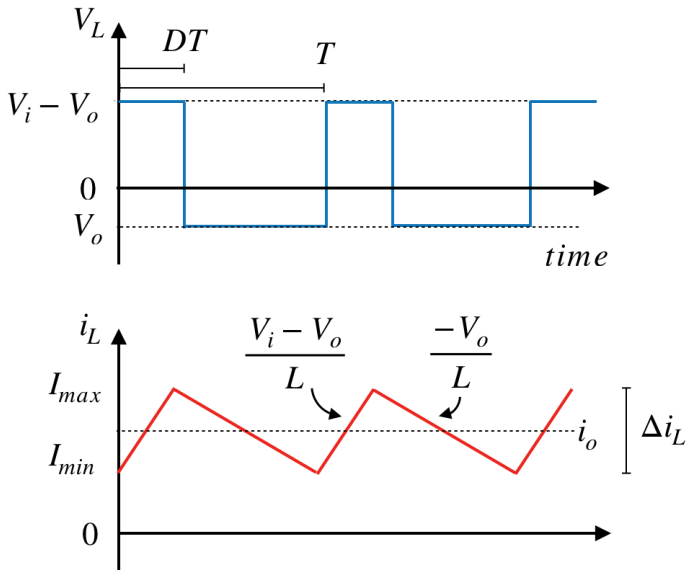


Figure 3.2: Inductor waveform

DT < t < T:

Using the KVL in the circuit in figure 3.1(b).

$$0 = v_L + V_o \quad \rightarrow \quad v_L = -V_o = L\frac{di_l}{dt} \qquad [V] \tag{3.4}$$

The equation can be rearranged to express the current change.

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} = \frac{-V_o}{L} \tag{3.5}$$

$-V_o < 0$, so the current will decrease with a slope of $-V_o/L$, see figure 3.2. The current ripple can also be expressed in this interval.

$$(\Delta i_L)_{fall} = \left(\frac{-V_o}{L}\right)(1-D)T \tag{3.6}$$

In steady state, the net current change is to be zero, so eq. (3.3) and (3.6) can be expressed as follows.

$$(\Delta i_L)_{rise} + (\Delta i_L)_{fall} = 0 \tag{3.7}$$

$$\left(\frac{V_i - V_o}{L}\right)DT + \left(\frac{-V_o}{L}\right)(1-D)T = 0 \tag{3.8}$$

By solving for V_o, the voltage conversion $V_o = V_i D$, presented in eq. (2.3), is validated.

Eq. (3.3) can be rearranged to give an expression of the inductor size with respect to the current ripple.

$$L = \frac{V_o(1-D)}{\Delta i_L f} \tag{3.9}$$

When estimating the inductor size, V_o and D are typically fixed values, and Δi_L and f are variables. The components' size will be estimated in section 5.

3.1.2 Output Voltage Ripple

Where the inductor restricts current, a capacitor restricts voltage. The capacitor in parallel with the output has the purpose to smooth out the voltage and can be designed to have a specific voltage ripple.

Using the Kirchhoff's Current Law (KCL) for node A of the circuit in figure 3.1(a) and isolating for the capacitor current i_C.

$$i_L = i_C + i_o \quad \rightarrow \quad i_C = i_L - i_o \qquad [A] \tag{3.10}$$

The current flowing into the capacitor is the inductor current subtracted by the load current. As shown in figure 3.2, the inductor current consists of an average DC component and an AC component. If the impedance of the capacitor branch is much lower than the load branch, then the load ripple is small and can be neglected. In this case, the DC component is subtracted from capacitor current, leaving only the AC as seen in figure 3.3. This means that the capacitor is charging, when the current is positive, and discharging, when the current is negative. The change of charge in the capacitor is given by the following.

$$\Delta Q = C\Delta V_o \quad \text{or} \quad \Delta Q = i_C \Delta t \qquad [C] \tag{3.11}$$

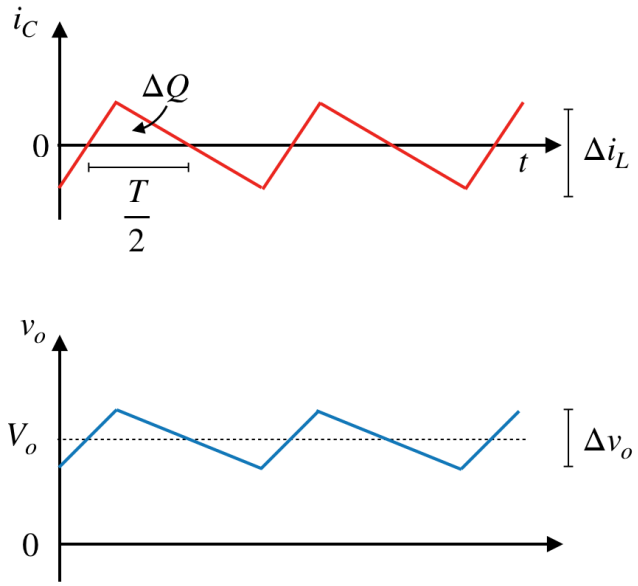


Figure 3.3: Capacitor ripple

The change of charge is equal to the area under the curve, which is also equal to the area formed by the negative current. Since the ripple has a magnitude of Δi_L and a positive charge equal to half the switching period, the ΔQ can be calculated.

$$\Delta Q = \frac{1}{2}\left(\frac{T}{2}\right)\left(\frac{\Delta i_L}{2}\right) = \frac{T\Delta i_L}{8} \qquad [C] \tag{3.12}$$

Inserting Δi_L from eq. (3.6) into eq. (3.13) and solving for the capacitance C.

$$\Delta Q = \frac{T\Delta i_L}{8} \quad \rightarrow \quad \Delta V_o = \frac{T\Delta i_L}{8C} \tag{3.13}$$

$$\Delta V_o = \frac{V_o(1-D)}{8LCf^2} \qquad [V] \tag{3.14}$$

$$C = \frac{1-D}{8L(\Delta V_o/V_o)f^2} \qquad [F] \tag{3.15}$$

Compared to the inductor, which is independent of the capacitor, the size of the capacitor depends on the inductor size. This is because the size of the inductor determines the AC current ripple.

3.2 Practical Parameters

In the real world, the components of the power stage cannot be assumed ideal. The inductor and capacitor include parasitic components, which will be presented in this section. These values can be found in any real component datasheet. A more accurate circuit with resistance values in series with the inductor and capacitor is illustrated in

figure 3.4. These resistances are referred to as parasitic elements or Equivalent Series Resistance (ESR).

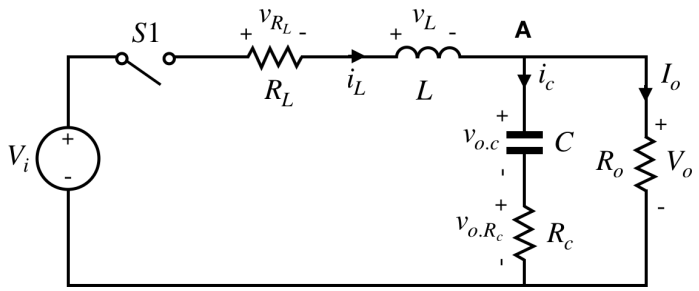


Figure 3.4: Power stage circuit with series resistance

3.2.1 Inductor

The first parameter to be aware of is that the inductor also has a small series resistance, stated as a DC resistance in a datasheet. This affects the current ripple by decreasing it because it decreases the slope of the current. This can be seen by using the KVL of the circuit in figure 3.4.

$$V_i = i_L R_L + L\frac{di_l}{dt} + V_o \qquad [V] \tag{3.16}$$

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} = \frac{V_i - i_L R_L - V_o}{L} \tag{3.17}$$

The slope of eq.(3.17) has decreased compared to the ideal slope of the current in eq. (3.2). With Δt being constant, then Δi_L will decrease. Nevertheless, the series resistance also introduces a power loss in the inductor equal to

$$p_{L.Loss} = R_L i_L^2 \tag{3.18}$$

A small Δi_L in steady state is a preferred design criterion, however, power losses are not. Real components will always have this series resistance, but manufacturers try to decrease the value.

The second parameter to be aware of is saturation current. Power inductors, which are designed for high currents and used in SMPS, consist of a wire wounded around a soft magnetic material, e.g. ferrite or iron [8]. The flow of a current in the wire will induce a magnetic field in the core. Increasing the magnetic field strength H will increase the flux density B in the inductor until the core saturates, see figure 3.5.
When the current exceeds the saturation current, a significant decrease in inductance happens. An inductor must be chosen so that the saturation current is above the peak current in the circuit.

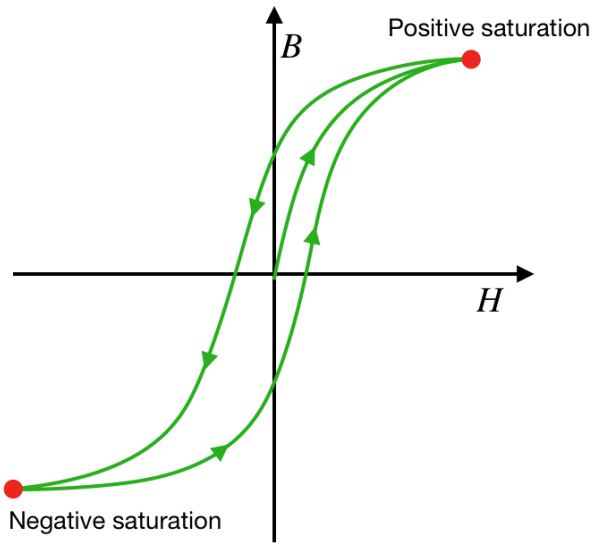


Figure 3.5: Magnetic hysteresis loop or B-H curve

The third parameter is the frequency. The inductor is tested by the manufacturer at a specific frequency, which is typically given in the datasheet. If the inductor is to be operated at another frequency, the manufacturer sometimes presents an inductance over frequency chart. The chart will indicate at which frequency the inductance will change. An inductor must be chosen to operate properly within the circuits operation frequency and below its self-resonance frequency.

3.2.2 Capacitor

As there exists a series of resistance in the inductor, as does there in the capacitor, seen in figure 3.4. In the buck converter circuit, R_L does not have a significant influence on the output voltage, but the R_c does. This resistance has the disadvantages of increasing the voltage ripple ΔV_o and power loss. It is shown in section 3.1.2 that the current through the capacitor branch is the AC current ripple in the inductor. Take that the same current ripple flows through the R_c, then the ripple $\Delta V_{o,R_c}$ can be determined using eq. (3.6).

$$\Delta V_{o,R_c} = R_c \Delta i_L = \frac{R_c V_o (1-D)}{Lf} \tag{3.19}$$

A conservative total voltage ripple ΔV_o can then be estimated.

$$\Delta V_o \approx \Delta V_{o,c} + \Delta V_{o,R_c} = \frac{V_o(1-D)}{8LCf^2} + \frac{R_c V_o (1-D)}{Lf} \qquad [V] \tag{3.20}$$

In some cases, the ESR is the dominant part of eq. (3.20), which is why it is good practice to always oversize the capacitor. As capacitor size increases, the ESR decreases [2]. Different types of capacitors exit on the market, where electrolytic capacitors are

commonly used in SMPS because of their broad range in size. Though a ceramic capacitor has the lowest ESR, it is typically sized below 1 μF.

Another parameter to be aware of is the maximum RMS current that the capacitor can deliver. This is also stated in the datasheet and tested for a specific temperature.

For both the inductor and capacitor, it is also important to be aware of how the components' parameters will change at different temperatures. Often, the manufacturer provides a chart for the change in parameters depending on temperature or current.

4 Switching Stage

The next part of the SBC is the switching stage, shown in figure 2.9. This part consists of two switches and a PWM controller. In chapter 3, the power stage analysis was carried out based on ideal switches. This chapter will describe the non-ideal parts of power switches and how to design a switching circuit.

Several types of power switches can be applied, but when talking about SMPS, Metal-Oxide Field-Effect Transistors (MOSFET) are the typical choice. MOSFET is voltage controlled and can operate at high switching speeds. The MOSFET is chosen as the semiconductor switch of the SBC.

A MOSFET has three terminals to connect to, called gate G, drain D, and source S. By applying a voltage to the gate, the switch will open and allow current to flow between drain and source. A MOSFET is a voltage controlled switch, which means that it does not need a continuous ON current to function [9][10]. This is because the gate is isolated from the conducting silicon. Within the MOSFET family, two types exists, and they are referred to as P- or N-channel MOSFETs.

4.1 High- and Low-side MOSFET

Switches and their driver are generally characterized by their placement in a circuit, either being a high- or low-side switch. A MOSFET with its source terminal connected to ground is referred to as a low-side MOSFET, and if the terminal is not connected to ground, its called a high-side MOSFET. A typical configuration with both a high- and low-side MOSFET is shown in figure 4.1(a).
A low-side N-channel MOSFET M_1 can simply have a pulse driver directly connected to its gate, as they share the same potential. A high-side N-channel MOSFET M_2 has a floating source terminal, which means that obtaining a finite V_{GS} voltage can be very difficult. The N-channel drive circuit will be described in section 4.4. To simplify the driver circuit, a P-channel MOSFET can replace the high-side switch $M1$, see figure 4.1(b). A P-channel is activated with a negative potential of V_{GS}. P-channel MOSFETs are not very common, and they are only available in a limited range due to their inefficient parameters compared to the N-channel MOSFET. Even though the N-channel MOSFET's high-side driver circuit is more complex, it is the preferred type, and it is therefore selected for both switches of the SBC. The rest of the analysis will only focus on the N-channel MOSFET.

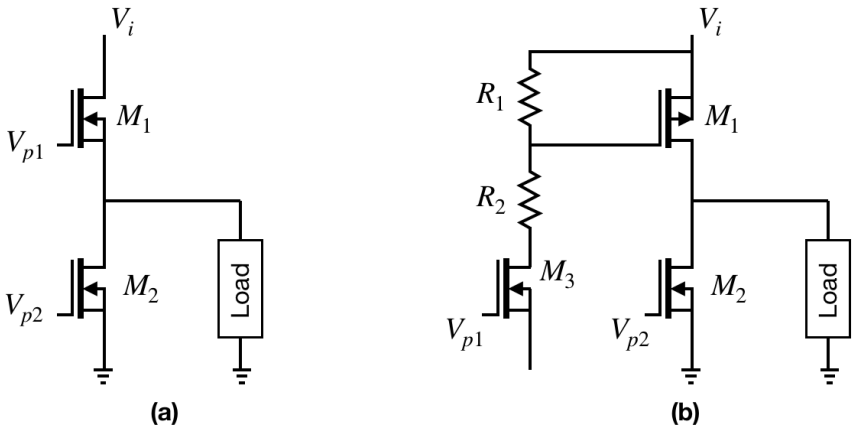


Figure 4.1: (a) High and low side MOSFET. (b) Example of P-channel MOSFET driver circuit

4.2 Switch Procedure

Different models of MOSFETs are available depending on how advanced and complex the model should be. Manufacturers sometimes provide a model of their MOSFET in SPICE. A model used when investigating the switching properties is shown in figure 4.2. Here, the most important parameters are gate resistance and internal capacitance between the MOSFET terminals. The values are typically given in the datasheet indirectly as C_{RSS}, C_{ISS}, and C_{OSS}, which can be recalculated to the actual capacitance.

$$C_{GD} = C_{RSS} \tag{4.1}$$
$$C_{GS} = C_{ISS} - C_{RSS} \tag{4.2}$$
$$C_{DS} = C_{OSS} - C_{RSS} \tag{4.3}$$

Even though a MOSFET is said to be voltage controlled, a pulse of current flowing into the gate is necessary in any switching cycle due to the capacitance. Charging a capacitor is given by the following.

$$Q = \int idt = CV \qquad [C] \tag{4.4}$$

The switching procedure at turn-ON is illustrated in figure 4.2, and is split up into four steps. The circuit illustrates three capacitors, which are linked between the MOSFET's connectors. Going into the gate is an external resistor R_G and an internal resistor $R_{g,i}$. In the first step, a voltage is applied at V_{DRV} but must be less than the gate-source breakdown voltage. Current I_G is flowing into the gate and is mostly charging the C_{GS} capacitor. This period is called the turn-on delay. When the voltage threshold V_{TH} has been reached, the next period begins. This is the linear region, where the drain current I_D starts to flow proportional to V_{GS}. The drain-source voltage stays unchanged throughout this period. The third period is where the miller-plateau is reached, and I_D is at its maximum. Here, the drain-source voltage starts to drop, but the gate current and voltage stay unchanged. When drain-source voltage reaches zero, the MOSFET is fully conducting, and the rise of V_{GS} determines the on-resistance of the MOSFET.

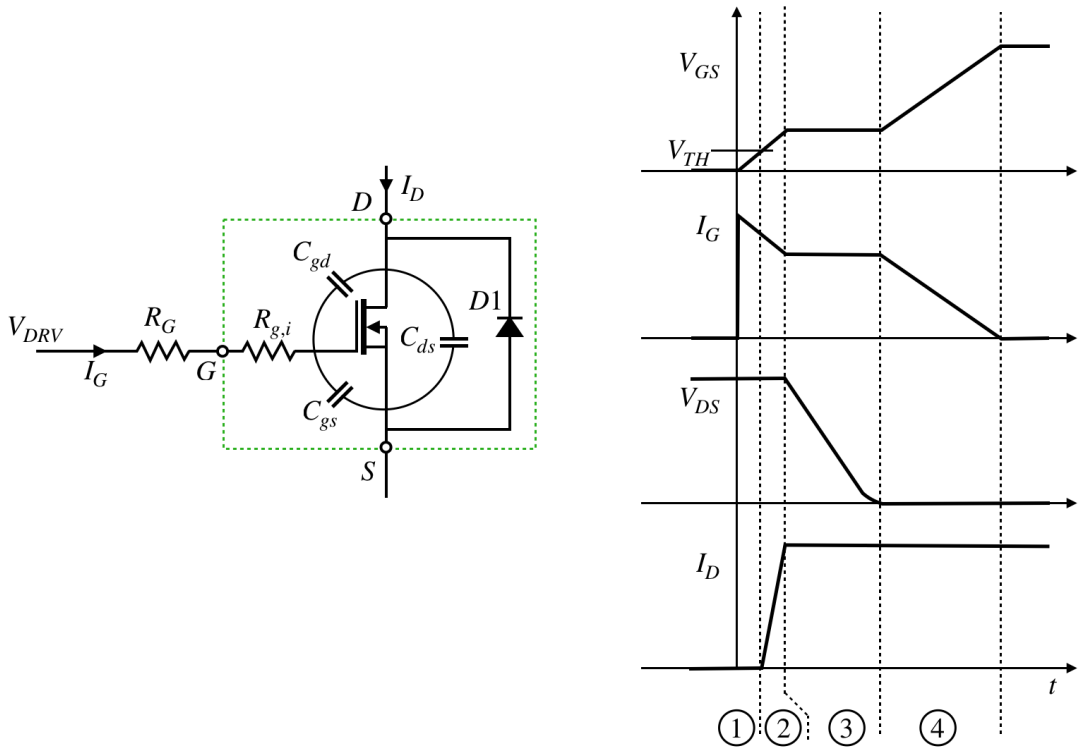


Figure 4.2: Equivalent MOSFET circuit and turn-on procedure

Thus the gate current goes to zero completing the turn-ON procedure. At turn-OFF, the procedure is reversed.

The individual steps, and the time it takes to reach them, can be very challenging to determine and may not be necessary. In a MOSFET's datasheet, manufacturers provide a total gate charge value Q_G. This involves all the charges required to fully open the MOSFET. The gate charge is tested at a specific condition given in the datasheet. Be aware that some parameters are voltage-, temperature-, and frequency-depending.

At turn-ON, the current is flowing into the gate to charge the capacitors, which will be discharged at turn-OFF. This introduces a power loss and can be determined by calculating the energy provided by the driver. The energy supplied can be determined.

$$E_G = \int V_{GS} i_g dt \qquad [J] \tag{4.5}$$

Note that the gate current i_G can be expressed by the gate charge from eq. (4.4).

$$E_G = \int V_{GS} \frac{dQ_G}{dt} dt = V_{GS} dQ_G \qquad [J] \tag{4.6}$$

For the specific MOSFET, manufacturers provide a chart which shows the relationship between gate-source voltage and total gate charge. This is illustrated in figure 4.3.
The V_{GS} will rise until it reaches V_{DRV}. The Q_G is depending on V_{DRV} and V_{DS}, where some conditions are given in the datasheet. The total area within the gray box is the

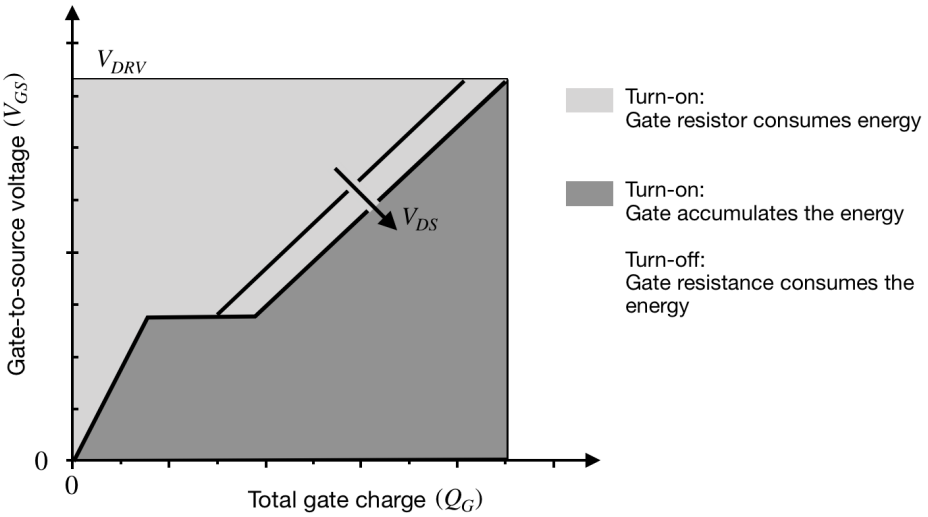


Figure 4.3: MOSFET total gate charge chart [10]

supplied energy, where some is dissipated in the gate resistance. The average power loss caused by the switching is then defined as the energy consumed over how often this event occurs, which in return is determined by the switching frequency f.

$$P_G = E_G f = V_{DRV} Q_G f \qquad [W] \tag{4.7}$$

The switching losses are proportional to the switching frequency, which is a factor that must be taken into consideration during the design process.

Another switching loss takes place during the switching procedure and is related to the load and the voltage across the device. Figure 4.4 illustrates part of the switching procedure in figure 4.2. Whenever the voltage at the gate exceeds the voltage threshold, the current between drain and source starts to flow, but the voltage V_{DS} stays unchanged, seen in step 2. This introduces a power loss P_{SW} with a positive slope [11].
When I_D has reaches the load current, V_{DS} falls, resulting in a decrease in power loss, seen in step 3. The power loss in step 2 and 3 is proportional to the time it takes to complete these steps. The power loss can be determined by calculating the area under the power loss curve in figure 4.4. This happens both at turn-ON and turn-OFF of the MOSFET.

$$P_{SW} = V_{DS} I_D f (t_2 + t_3) \qquad [W] \tag{4.8}$$

As in the gate power loss in eq. (4.7), the switching losses are frequency depending. Losses also depend on how fast the switching completes its cycle, which again depends on I_G.

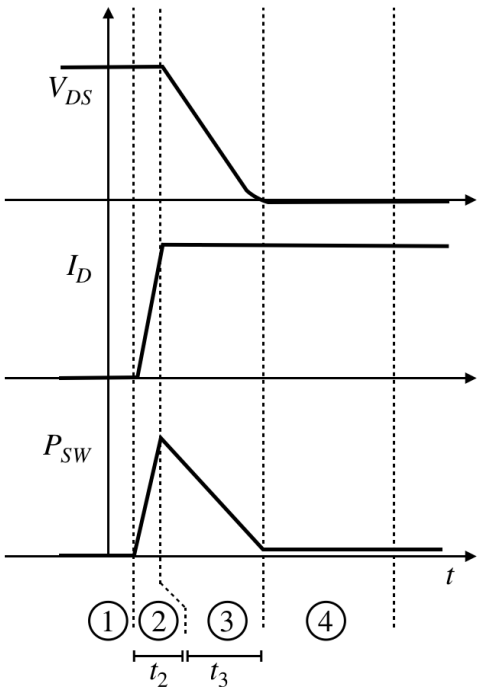


Figure 4.4: Chart of MOSFET switching losses

4.3 Gate Resistor

The gate resistor is a very important component to dimension correctly. As described in section 4.2, a pulse of current is flowing into the MOSFET gate to turn it ON. The amplitude of the current is restricted by its internal resistance $R_{g,i}$ and external gate resistance R_G. Although the I_G pulse in figure 4.2 is difficult to determine, the peak current seen in step 1 can be determined by Ohm's law $I_{G,peak} = V_{DRV}/(R_G + R_{g,i})$. Lowering R_G will decrease the switching time and decrease power losses. However, by decreasing R_G, an increase in ringing voltage across drain and source is induced. This must be carefully considered as the ringing can damage the MOSFET or lead to devise failure.

4.4 Gate Drivers

As described in section 4.2, applying a voltage at the MOSFET gate, above the threshold voltage, will turn ON the switch and allow current to flow between drain and source. Typically, a MOSFET is controlled by a processor which operates at a logic level and can only supply 3,3 to 5 V with limited current. Some MOSFETs' threshold voltage is low enough to be operated directly by a processor, and this is called "logic level MOSFETs". As the rated V_{DS} and I_D increases, as does the V_{GS}, which means, that a processor can no longer provide the necessary gate voltage or current. A MOSFET gate driver can then be implemented between the processor and MOSFET. The driver can operate at much higher voltages and currents, and it comes in several configurations. An example is a basic N-channel MOSFET drive circuit, seen in figure 4.5.

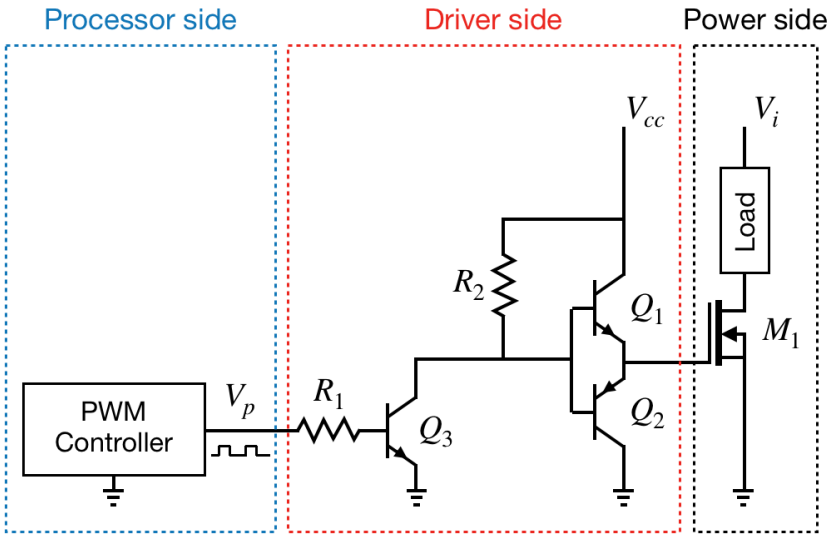


Figure 4.5: MOSFET drive circuit

The circuit consists of a processor-, driver-, and power-side. The processor, in this case, only provides a PWM signal to the drive circuit. The drive circuit is specially designed based on the MOSFET parameters and configuration, in this case, a low-side setup. The circuit consists of three Bipolar Junction Transistors (BJT), where Q_1 and Q_2 is forming what is called a push-pull configuration [3]. Q_3 act as a buffer to source and sink the required current for activating the push-pull circuit. Q_1-Q_3 can also be replaced with MOSFETs. The power side is typically operating at much higher voltages and currents than the driver side, referred to the power stage of the SBC. Nowadays, the driver side is implemented in an Integrated Circuit (IC) chip.

The high-side MOSFET, as explained in section 4.1, is more complicated to control. The high-side MOSFET needs a finite V_{GS}, but with a floating source terminal, a floating driver is necessary. One method is to use a bootstrap circuit [12][13]. The circuit is illustrated in figure 4.6 for the high-side MOSFET M_1. The driver circuit of the low-side MOSFET M_2 is basically the same as in figure 4.5. Both drivers use a push-pull setup, implemented in an IC.

The bootstrap circuit consists of a resistor R_{boot}, a diode D, and a capacitor C_{boot}. The capacitor acts as floating energy storage and should be able to provide the necessary gate charge of the MOSFET. V_{cc} is the driver side's power supply and is chosen based on the driver used and the V_{GS} rating of the MOSFETs. When M_1 is OFF and M_2 is ON, C_{boot} is charging as M_2 pulls the negative terminal of the capacitor to ground. When M_1 is ON and M_2 is OFF, C_{boot} is discharging some of its energy to the gate of M_1. Because C_{boot} is disconnected from ground, the V_{GS} of M_1 is the voltage (V_{BS}) across C_{boot}. As C_{boot} charges when M_1 is OFF, its ON time can be restricted. Since the duty cycle is very low in this case, this is not of concern. When discharging C_{boot}, its voltage will drop. Based on the total charge and the desired voltage ripple, the bootstrap capacitor can be determined.

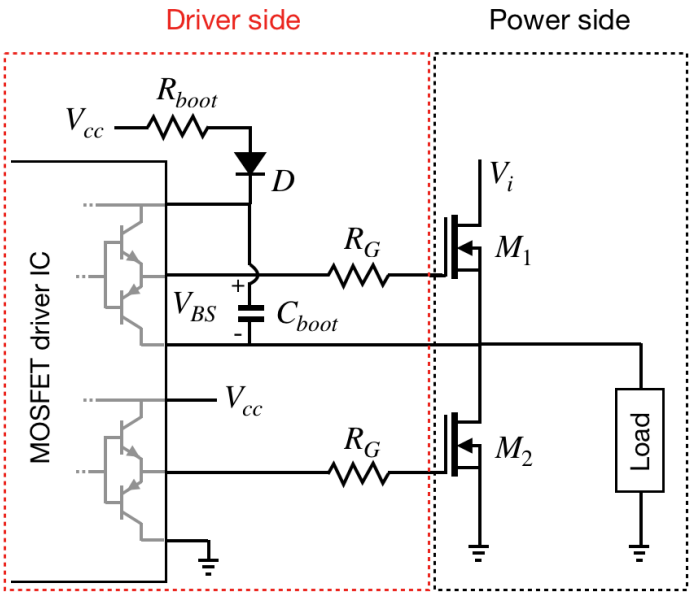


Figure 4.6: Dual high- and low-side MOSFET drive circuit

$$C_{boot} > \frac{Q_{TOT}}{\Delta V_{BS}} \qquad [F] \tag{4.9}$$

Q_{TOT} consists of the MOSFET gate charge and current leakages (I_{QBS}) flowing into the driver IC. This is typically given in the driver's datasheet as "quiescent V_{BS} supply current". The total capacitor charge can be determined.

$$Q_{TOT} = Q_G + I_{QBS} T_{off} = Q_G + \frac{I_{QBS}(1-D)}{f} \qquad [C] \tag{4.10}$$

It is always a good idea to oversize the capacitor. In [12] it is recommended to factor the size by 5 if it is an electrolytic capacitor.

5 Parameter and Component Selection

Determining the different parameters and variables in a SMPS is challenging, and it is an iterative process. Many of the parameters are interacting and unknown parameters, such as parasitic elements, can make the design process more complex. This chapter presents the challenges and determine the parameters and components. As criteria VI given in section 1.2 is off-the-shelf components, references to local and widely known electronic suppliers will be done e.g. RS components, Mouser, and Farnell. Datasheets of different components is available in appendix A.1.

5.1 Bulk Capacitor

Throughout chapter 3, the power supply to the converter has been modeled as an ideal one. In practice, the voltage and current of the power supply is limited by its rated power. A power supply will take some time to recover after e.g. a sudden change in load. This is called load regulation. In another situation, if the converter is asking for a high current, but the power supply is only rated for e.g. half that amount, the power supply will saturate, and the voltage will drop. To counteract this, the converter must have an energy bank at the input, which can be done using a capacitor. This is also referred to as a bulk capacitor, see figure 5.1.

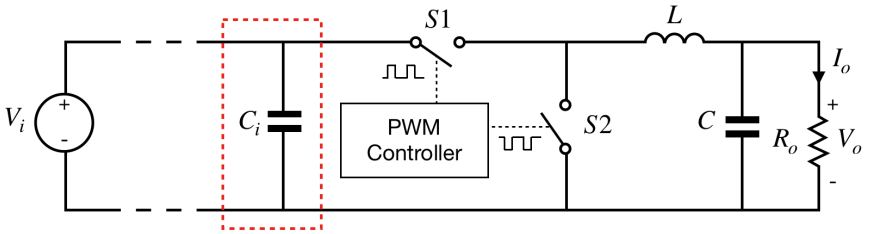


Figure 5.1: Bulk capacitor at the converter's input

To give an idea of the size of the bulk capacitor, the eq. (3.13) can be utilized. Δt is the time the capacitor needs to deliver the required load current I_o. This results in a capacitor charge and can be rearranged according to the duty cycle and frequency.

$$\Delta Q = \frac{I_o D}{f} \qquad [C] \tag{5.1}$$

The bulk capacitor size can then be determined in regards to the voltage ripple that can be tolerated at the input. This is given by the following.

$$C = \frac{I_o D/f}{\Delta V} \qquad [C] \tag{5.2}$$

E.g. with a power demand of 1500 W and a step-down conversion from 1000 V to 48 V, the resulting load current will be 30 A, and a duty cycle of approximately 0,05. E.g. a $\Delta V = 1\ V$ will result in a capacitor of 30 μF with $f = 100\ kHz$. Typically, the bulk capacitor is oversized to ensure that it can provide the required current.

5.2 Switching Frequency

As described in chapter 4 and 3, the switching frequency is a parameter that affects the component size of the power stage and the power loss in the switching stage. Typically, the switching frequency is above 20 kHz to avoid audio noise [3]. In addition, if the components are exclusively sized according to the switching frequency, then the switching frequency also determines the bandwidth of the converter. As the switching frequency determines so many other parameters, it must be fixed, even though finding it can be an iterative process. As switching losses in the MOSFET can be significant, a relatively low switching frequency of 100 kHz is chosen.

5.3 MOSFET and Driver Side

When choosing the MOSFETs and their drive circuit, voltage rating must be considered. According to the switching scheme of the converter described in section 3.1, the low side MOSFET's rated voltage from drain to source must be above 1000 V. Another factor is its rated current, which must be above the maximum rated power of the converter. At 1500 W of power, the output current I_o is approximately 30 A, which will flow through the MOSFET as well. These values are also referred to as voltage and current device stress. Both high and low side MOSFETs are selected to be the same, as they nearly experience the same amount of stress.

The chosen type of MOSFET is SCT3080KL from ROHM Semiconductor, with a rated voltage and current of 1200 V and 31 A. This type is designed for SMPS and other high power applications.

The gate drive circuit, as explained in section 4.4, is simple for the low-side MOSFET, but challenging for the high-side MOSFET. This is why an IC drive is typically used. An IR2213 high- and low-side driver from International Rectifier is chosen, which is fully operational up to 1200 V. It is designed to be compatible with a bootstrap circuit, and it can be operated with 3,3 V logic. It utilizes the push-pull circuit explained in section 4.4.

5.4 Power Stage

Criterion II in section 1.2 sets the output voltage ripple to be maximum 200 mV. The inductor and capacitor must be sized to meet this criterion. In section 3.2.2, the magnitude of the voltage ripple was given according to the capacitor size and its ESR. For some types of the capacitor, the ESR will be the dominant parameter, which then sets a limit on the inductor current ripple. Using eq. (3.9) and (3.15), the inductor and capacitor size can be determined without the parasitic components, using the parameters given in table 5.1. The Δi_L is set to an arbitrary value to begin with.

Table 5.1: Converter parameters

Parameter	V_o	D	f	ΔV_o	Δi_L
Value	48 V	0,048	100 kHz	200 mV	4 A

$$L = \frac{V_o(1-D)}{\Delta i_L f} = 114 \qquad [\mu H] \tag{5.3}$$

$$C = \frac{1-D}{8L(\Delta V_o/V_o)f^2} = 25 \qquad [\mu F] \tag{5.4}$$

The value calculated in eq. (5.4) seeks to ensure that the ripple does not exceed 200 mV, but with an ESR, the ripple will increase. To counteract this, the capacitor can be oversized, so the dominant part of the ripple is obtained by the inductor ripple current and ESR of the capacitor. The capacitor is oversized by a factor of 4, making 100 μF. With $\Delta i_L = 4\ A$, a capacitor with an ESR of less than $Rc = \Delta V_o/\Delta i_L = 50\ m\Omega$ must be found which can also supply a current ripple RMS of $I_{RMS} = \Delta i_L/2\sqrt{3} = 1{,}15\ A$. As 100 μF is a relatively low value, the market provides a wide variety of sizes, which can be configured to give the calculated ESR and capacitance.
Remember that to deliver an output power of 1500 W, the output side must be able to let around 30 A flow, which is conducted by the inductor. Finding a power inductor that can handle 30 A with the given size is very challenging. In appendix A.1, two datasheets for an inductor are presented from Tamura and Vishay. Both provide a power inductor which can handle around 30 A with 100-150 μH. The saturation current is above rated, and it has a low ESR.

The power stage components and sizes are chosen to be:

$$L = 150\mu H \qquad R_L = 13m\Omega \qquad C = 100\mu F \qquad R_c = 50m\Omega$$

6 SPICE Simulation and Thermal Properties

This chapter presents an open-loop simulation in LTspice and a thermal evaluation of the circuit. Here, a simple heat transfer analysis is conducted. Simulation file can be found in appendix A.4. In chapter 7, the capacitance will be changed to $C = 4700\ \mu F$ due to better control performance, so this value will also be used in this simulation.

6.1 Open-loop Simulation

To simulate the IC driver IR2213 as best as possible, two push-pull circuits are implemented in LTspice, driven by a pulse generator. The high-side MOSFET M_1 is powered by the bootstrap circuit, and the setup is shown in figure 6.1. A model of the SCT3080KL MOSFET could not be determined, instead, a STW11NM80 MOSFET is used, which is available via the LTspice library. The STW11NM80 MOSFET is only rated at 800 V, so the input voltage is decreased. The diode D is also chosen in the library and rated at 800 V. The switching frequency, inductor, and capacitor size is determined in chapter 5.

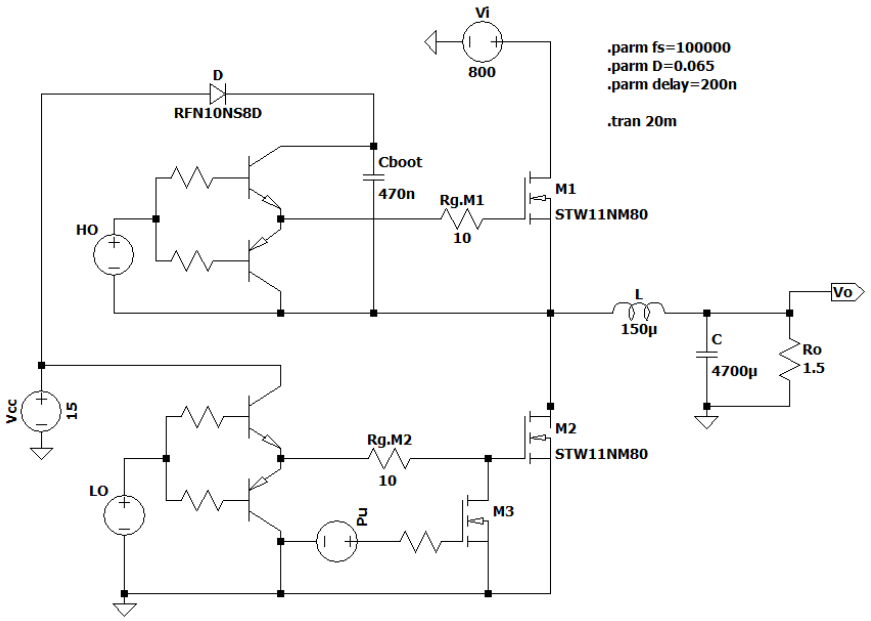


Figure 6.1: LTspice circuit setup

Parameters such as duty cycle and output resistance are adjusted to get 48 V and 1500 W of output power. At maximum power, the output voltage and inductor current ripple are verified, see figure 6.2.

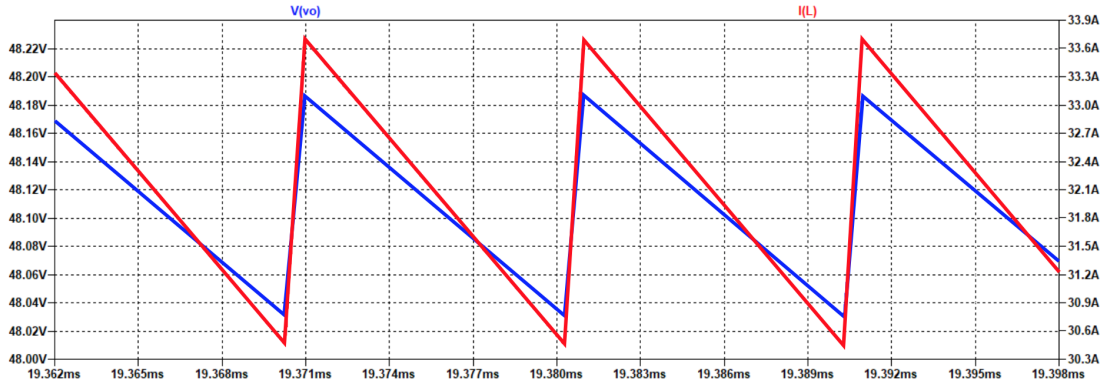


Figure 6.2: Output voltage V_o and inductor current i_L

The output voltage ripple ΔV_o is less than 200 mV, which fulfills the criterion. The inductor ripple Δi_L is less than 4 A as expected.

The model of the MOSFETs incorporates the terminal capacitance presented in section 4.2. The switching pattern can then be observed. As it takes time for the MOSFETs to conduct current, the two pulse signals HO and LO, must have a deadtime d between them. This is to make sure that they are not conducting current at the same time. Figure 6.3 illustrates to two pulse signals.

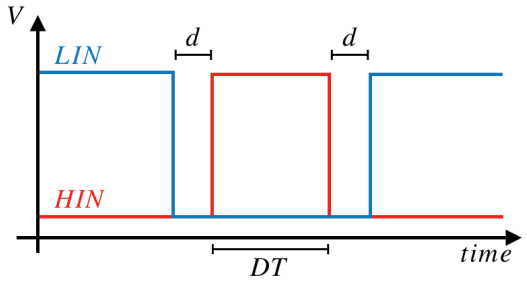


Figure 6.3: PWM signal from processor with deadtime

In chapter 9, a minimum deadtime of the IR2213 is found to be around $d = 200\ ns$. The gate voltages V_{gs} and currents I_g can be seen in figure 6.4.
First, M_2 turns OFF by taking $V_{gs.M2}$ to zero, which discharges the gate capacitance, seen as $I_{g.M2}$. Next, M_1 turns ON by increasing $V_{gs.M1}$ and charging the gate capacitance. Observing the current flow of the M_2 drain terminal, it can be determined if the MOSFETs are open at the same time. To prevent this, the deadtime can be increased, or the gate resistance can be decreased.

When driving a half-bridge setup as in the SBC, a phenomenon called self-turn-on can be forced at the low-side MOSFET. This can be observed in figure 6.4 for $I_{g.M2}$ at

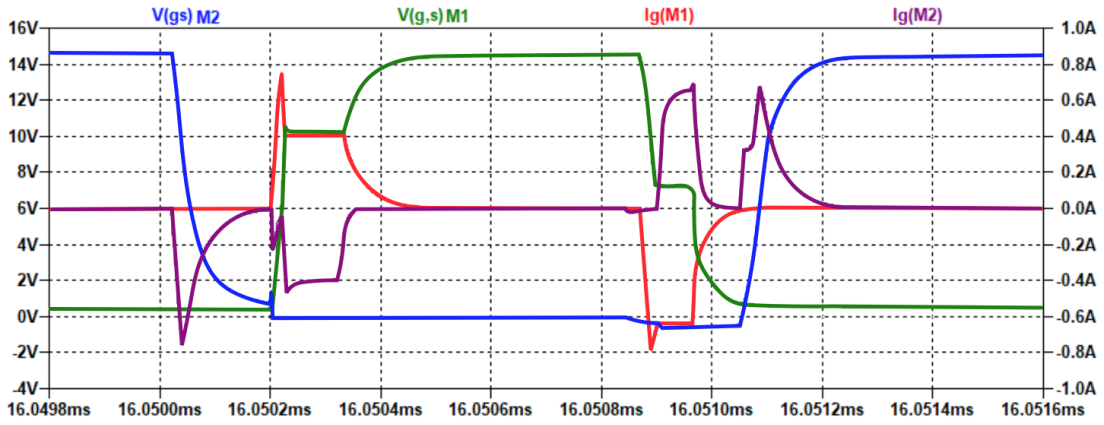


Figure 6.4: V_{GS} and I_G for M_1 and M_2

time 16,0502 ms. Here, $I_{g.M2}$ spikes as M_1 turns ON. This is due to the gate-drain capacitance C_{gd}. As M_1 turns ON, the voltage V_S rises quickly over a short time. Noted by C_{gd}, this induces a current flow, which flows through the gate resistor. This is marked by the red line in figure 6.5 [14].

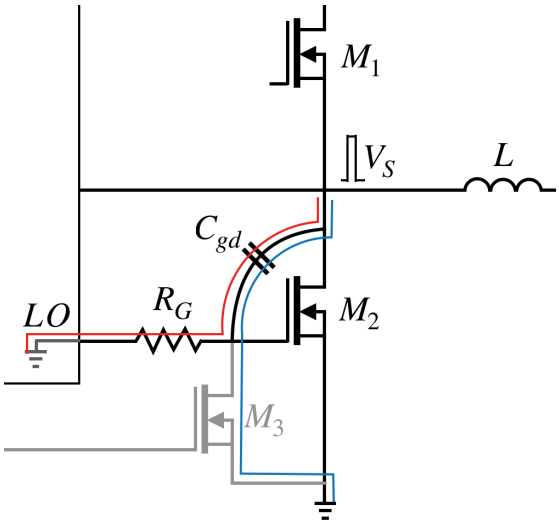


Figure 6.5: Circuit illustration of the self-turn-on phenomenon

The current flowing through R_G induces a voltage on the gate, which, if exceeding the threshold voltage, could turn M_2 ON momentarily. A quick solution is to generate another current path, as is done by the MOSFET M_3 in figures 6.5 and 6.1. The implementation of M_3 is why $V_{gs.M2}$ in figure 6.4 does not rise.

This phenomenon must be taken into consideration when designing the actual setup.

6.2 SBC Efficiency

Through the simulation in LTspice, it is possible to estimate the SBC's efficiency. This is done by measuring the power extracted from the input supply V_i and measuring the output power P_o over the output resistance R_o. The duty cycle and R_o are adjusted to give an output voltage of 48 V. Measurement is done at steady-state and average power. Figure 6.6 shows the efficiency over output load.

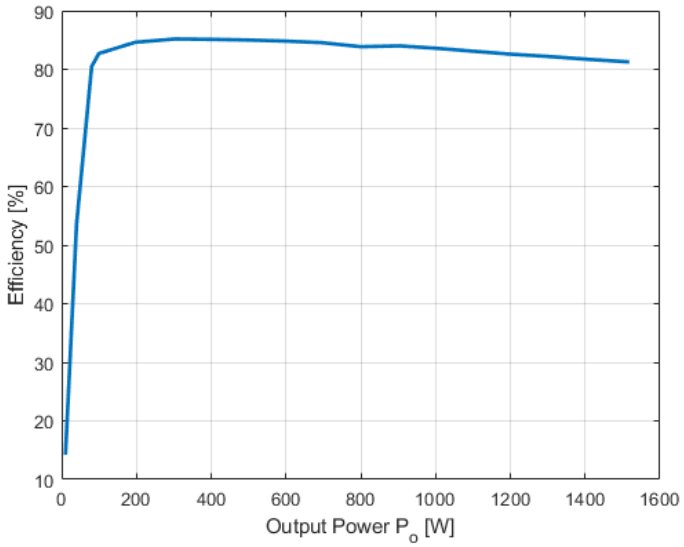


Figure 6.6: SBC efficiency over output load

For light loads under 100 W, the SBC is not very efficient, but at values higher than this, it stays above 80 % consistently until full load.

6.3 Thermal Dissipation

The SBC must be encapsulated in a cylinder, called a bottle, as it is going underwater. The SBC must then dissipate all of the heat generated through the shell of the bottle. For good heat transfer, the bottle can be constructed out of aluminum. The highest heat dissipation is at full load, where it needs to dissipate 350 W with the parameters used in the simulation in figure 6.1. In table 6.1, the heat generated by the different components is presented (determined through simulation).

Table 6.1: Power dissipated in each component

	Power loss P_l	**MOSFET** M_1	**MOSFET** M_2	**Inductor** L	**Capacitor** C
Power	350 W	230 W	105 W	12 W	50 mW
Percentage	-	65 %	30 %	3,4 %	>0,1 %

M_1 is producing 65 % of the heat generated in the SBC. As described in section 4.2, the power losses in a MOSFET is determined by the switching frequency and gate current. For M_1, the switching losses are greater than the conduction losses. If the gate

resistance is changed to 6 Ω of the circuit in figure 6.1, the switching procedure time goes from 300 ns to 200 ns, and the new switching power loss is found to be 167 W. In practice, the lowest possible gate resistance should be chosen in order to minimize power losses. For M_2, L, and C, components with smaller ON resistance or ESR must be found to reduce the power loss.

In thermodynamics, the power transfer in steady-state can be determined through the following equation [15].

$$\dot{Q} = \frac{T_1 - T_2}{R_{tot}} \qquad [W] \tag{6.1}$$

where $\dot{Q}$ is the heat transfer, T_1 and T_2 indicate the temperature, and R_{tot} is the total thermal resistance. The thermal resistance from junction to case of the MOSFET SCT3080KL is $R_{th,JC} = 0{,}91\ C°/W$ in the most extreme case. At the operation depth of the ROTV, the temperature is around 2 $C°$. With a maximum junction temperature of 175 $C°$, that would give a power dissipation of 190 W. The thermal resistance will increase as the water cannot be in direct contact with the MOSFET. The MOSFETs must be mounted to the bottle in order to improve the heat transfer. To dissipate more power, a new MOSFET must be found. The "big brother" of the SCT3080KL is called SCT3022KL (see appendix A.1) and has a thermal resistance of $R_{th,JC} = 0{,}35\ C°/W$. This means that it can dissipate 432 W under the same conditions.

As an example, the power dissipation of a MOSFET directly connected to the bottle is shown in figure 6.7. The thermal network consists of the junction to case resistance $R_{th,JC}$, bottle resistance R_b, and convection in the water R_w.

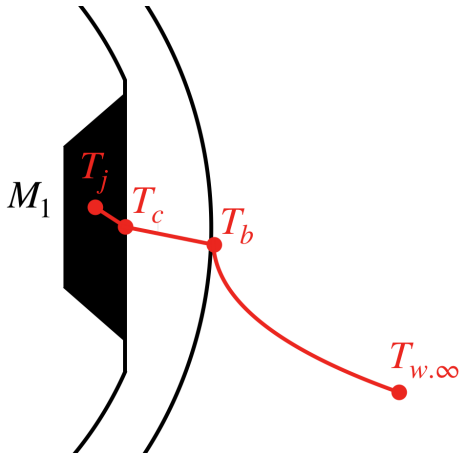


Figure 6.7: Thermal network from MOSFET to water

The setup can be simulated or a simplified analysis can be conducted by using eq. 6.1. Nevertheless, to obtain the best heat transfer, the devices that grow warm must be as close to the outer surface of the bottle as possible. The surface area of the warmer parts must be increased. Good circulation of air within the bottle and water on the outside are also beneficial.

7 Control

This chapter starts by determining the dynamic model of the SBC. Next a control unit is designed fulfilling control criterion's. MATLAB files, containing control calculation can be found in appendix A.3.

7.1 Model of the SBC

Determining a dynamic model of the SBC is necessary to observe the behavior of the converter and to obtain a suitable control unit. One popular technique is called State-space averaging, which establishes a good model for steady-state analysis and dynamic behavior [16][17][18]. It is required that the natural frequency of the system is much smaller than the switching frequency.

For simplification purposes, the following state-space averaging model is based on the ideal SBC from section 3.1. A more practical model with parasitic elements will be determined afterwards.

Firstly, the system must be identified and the state equations are written based on one switching cycle. Figure 7.1 illustrates the equivalent circuit for when the high-side switch $S1$ is ON and when $S1$ is OFF.

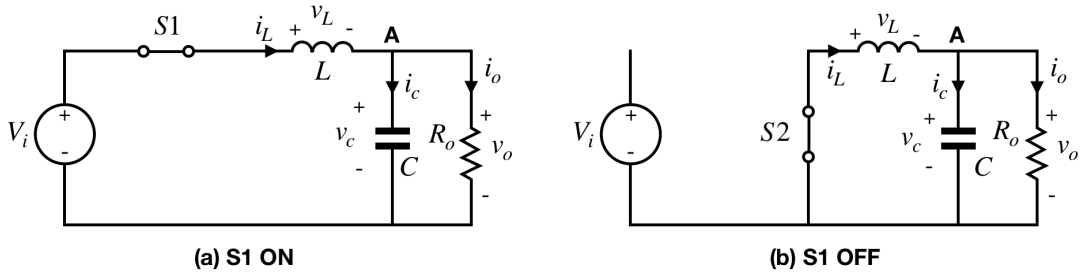


Figure 7.1: Equivalent circuit during one period

The following are the state equations.

$$\frac{di_L}{dt} = \dot{i_L} = \frac{1}{L}V_i - \frac{1}{L}v_c \tag{7.1}$$

$$\frac{dv_c}{dt} = \dot{v_c} = \frac{1}{C}i_L - \frac{1}{CR_o}v_c \tag{7.2}$$

The state equations can be configured into a state-space model corresponding to each of the two periods in figure 7.1 where the states $x = \begin{bmatrix} i_L & v_c \end{bmatrix}^{-1}$.

For when $S1$ is ON:

$$\dot{x} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_o C} \end{bmatrix} x + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_i = A_{ON} x + B_{ON} V_i \tag{7.3}$$

and when $S1$ is OFF:

$$\dot{x} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{R_o C} \end{bmatrix} x + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_i = A_{OFF} x + B_{OFF} V_i \tag{7.4}$$

where the output for both eq. (7.3) and (7.4) is

$$y = \begin{bmatrix} 0 & 1 \end{bmatrix} x \tag{7.5}$$

In this circuit, the capacitor voltage v_c is equal to the output voltage V_o. Following the state-space average model steps in [16] and [18], the averaging is obtained by weighting eq. (7.3) and (7.4) by the duty cycle d.

$$\dot{x} = [A_{ON} d + A_{OFF}(1-d)]x + [B_{ON} d + B_{OFF}(1-d)]V_i \tag{7.6}$$

A small AC perturbation component is added to the states.

$$x = x + \hat{x} \quad d = D + \hat{d} \tag{7.7}$$

Making $\dot{x} = 0$ and setting all perturbations to zero, the small signal model can be determined. As a relation between the duty cycle and output voltage is of interest, a transfer function can be determined from the state-space model. In [18], the state-space averaging model of a buck converter in CCM is presented and gives a transfer function for the system.

$$\frac{V_o(s)}{d(s)} = V_i \frac{1/LC}{s^2 + (1/RC)s + 1/LC} \tag{7.8}$$

By dividing V_i on both sides and considering a new input variable called $V_{in}(s) = d(s)V_i$ is obtained and the transfer function can be rewritten.

$$\frac{V_o(s)}{V_{in}(s)} = \frac{1/LC}{s^2 + (1/R_o C)s + 1/LC} \tag{7.9}$$

Eq. (7.9) corresponds to the transfer function of the low-pass filter presented in section 2.1 eq. (2.1), which is the power stage of the SBC. It is illustrated in figure 7.2(a). This means that a model with parasitic elements can be more easily determined by writing the Laplace equations of the circuit in figure 7.2(b).
Firstly, the impedance network of the capacitor, ESR, and load can be computed in a parallel configuration.

$$Z_c = \frac{1}{sC} + R_c \qquad Z_o = R_o \qquad Z_L = R_L + sL \tag{7.10}$$

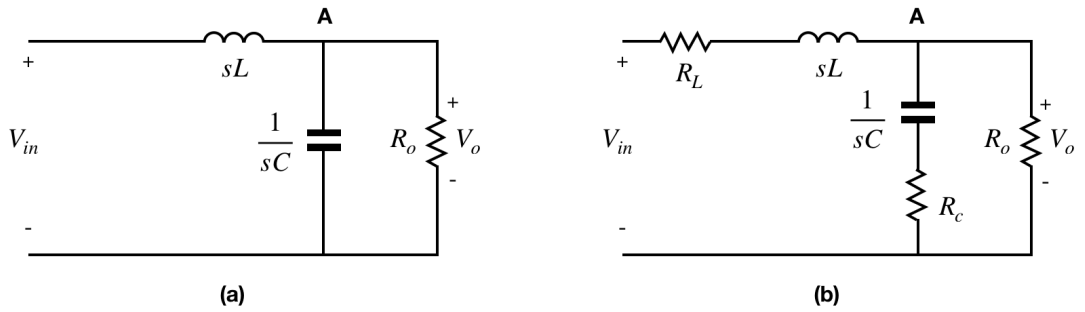


Figure 7.2: Laplace transform of the components

$$Z_{c,o} = \frac{Z_c Z_o}{Z_c + Z_o} \tag{7.11}$$

To obtain the relation output over input, the principle of a voltage divider can be used.

$$\frac{V_o(s)}{V_{in}(s)} = \frac{Z_{c,o}}{Z_L + Z_{c,o}} \tag{7.12}$$

Extracting this transfer function gives a second-order system with a zero

$$\frac{V_o(s)}{V_{in}(s)} = \frac{(R_c s + 1/C)k}{s^2 + as + b} \tag{7.13}$$

where

$$k = \frac{R_o}{L(R_o + R_c)}$$
$$a = \frac{CR_oR_L + CR_oR_c + CR_LR_c + L}{CL(R_o + R_c)}$$
$$b = \frac{R_o + R_L}{CL(R_o + R_c)}$$

The control design will be based on the worst-case scenario, and as the load can change, the least stable system must be found. With the component size given in section 5.4, the bode diagram of the system at 10 and 1500 W of power is shown in figure 7.3.
The phase margin is smallest at light loads, which is then chosen as control design plant. 10 W of power is equivalent to a load of $R_o = 230\Omega$. The transfer function of the SBC then becomes the following.

$$G(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{(333,3s + 6,665e7)k}{s^2 + 463,3s + 6,666e7} \tag{7.14}$$

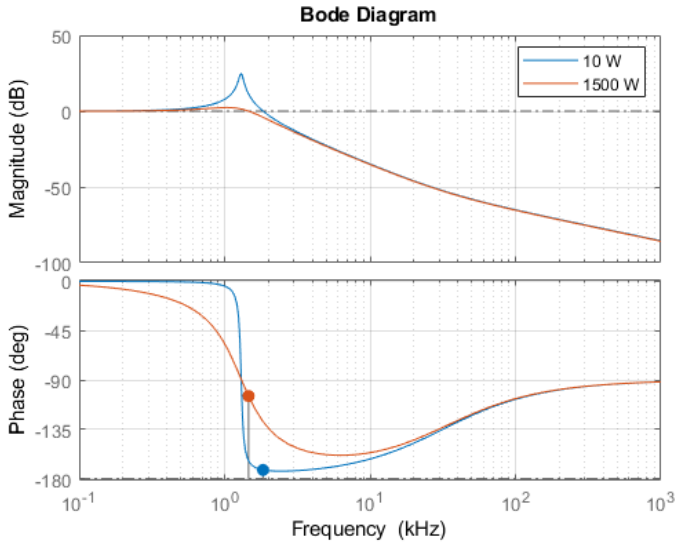


Figure 7.3: Bode diagram of the SBC with output power equal to 10 and 1500 W

7.2 Control Criteria

The converter must meet some criteria given by MacArtney. These are based on their existing converter from Vicor, the limitations of their equipment, and what they advertise. The control loop must meet the following criteria.

- The steady-state error must be less or equal to 1 %.
- Worst-case scenario, the phase margin must be over 45° and have a gain margin less than -6 dB [19][20].

7.3 Control Design

The control design process will use the frequency-response design method. This is carried out mainly by the use of the bode diagrams. Firstly, the system of $G(s)$ is analyzed to see if compensation is necessary. The bode diagram of the model of eq. (7.14) is shown in figure 7.4.
As expected by a low-pass filter configuration, the system is around 0 dB at the low frequencies, and $-\infty$ dB at the high frequencies. The bandwidth of the system is determined by the size of inductor and capacitor, which in this case is around 2 kHz. The zero, caused by the capacitor ESR, is located at the high frequencies, making it more prone to sensor noise. Only for the system $G(s)$ the closed-loop system is stable, but with very low stability margin with a phase margin of 7,89°. This not only shows a slow transient response but also large oscillations.

First, the system must be checked to see if it fulfills the first criterion of a steady-state error of less than 1 %. Since $G(s)$ has no pole at the origin, it is then a Type 0 system.

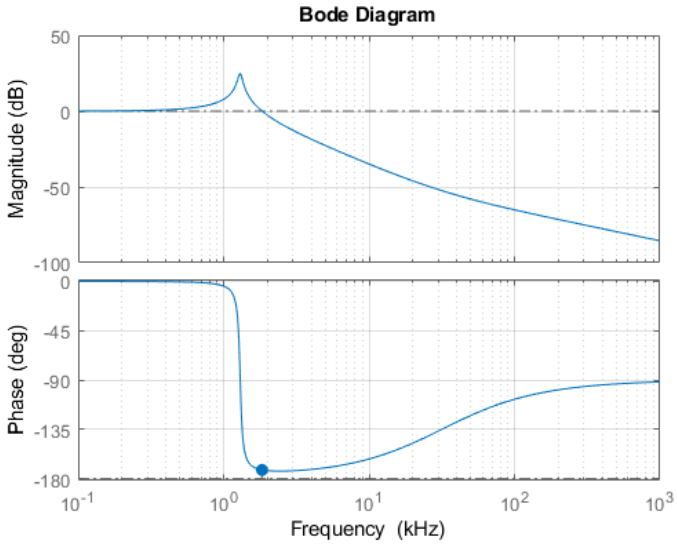


Figure 7.4: Bode diagram of the SBC $G(s)$

With a step input, this means that the steady-state error is a finite value. This value can easily be found by utilizing the Final Value Theorem [19].

$$e_{ss} = \lim_{s \to 0} s \left[\frac{1}{1 + G(s)} \right] R(s) = 0,5 \tag{7.15}$$

where $R(s)$ is a step input, equivalent to $1/s$. The steady-state error of 50 % does not fulfill the criterion, which means that the system needs compensation.

As the criterion is not zero steady-state error, K can be found for a steady-state error of 1 %. This will raise the magnitude plot of the bode diagram and thereby increase the crossover frequency. It must then be considered if the phase margin has increased sufficiently enough. If the phase margin is too small, a lead compensator can increase it around a specified frequency with only a small change in the magnitude plot. It is important to consider the final control structure, as this can affect the steady-state error. The lead compensator has the following structure.

$$D(s) = \frac{Ts + 1}{\alpha Ts + 1} \quad \alpha < 1 \tag{7.16}$$

The structure is essential as it must be incorporated into eq. (7.15) to find the gain K. As $D(0) = 1$, it is shown that the lead compensator does not change steady-state error. The gain K can be found by inserting the control structure in eq. (7.15) and setting $e_{ss} = 0,01$.

$$e_{ss} = \lim_{s \to 0} s \left[\frac{1}{1 + KD(s)G(s)} \right] R(s) = 0,01 \quad \rightarrow \quad K \approx 100 \tag{7.17}$$

The closed-loop system, including the gain K, can be computed.

$$G_{cl}(s) = \frac{KG(s)}{1 + KG(s)} \tag{7.18}$$

The bode diagram of $KG(s)$ and $G(s)$ is shown in figure 7.5a together with the step response in figure 7.7b.

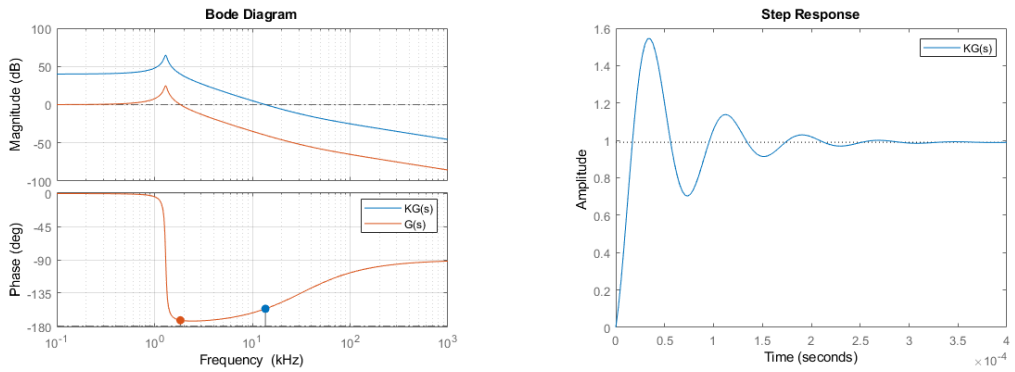


Figure 7.5: System response of $KG(s)$ control configuration

The steady-state error criterion has been met, which is also verified by the step response with a DC gain of 0,99. As expected, the magnitude plot has lifted and the phase margin has increased to 23,5°, which is getting closer to meet the next criterion of a phase margin of more than 45°. To increase the phase margin, a lead compensator is designed. To get a better understanding of the lead compensator, a bode diagram of $D(s)$ is illustrated in figure 7.6.

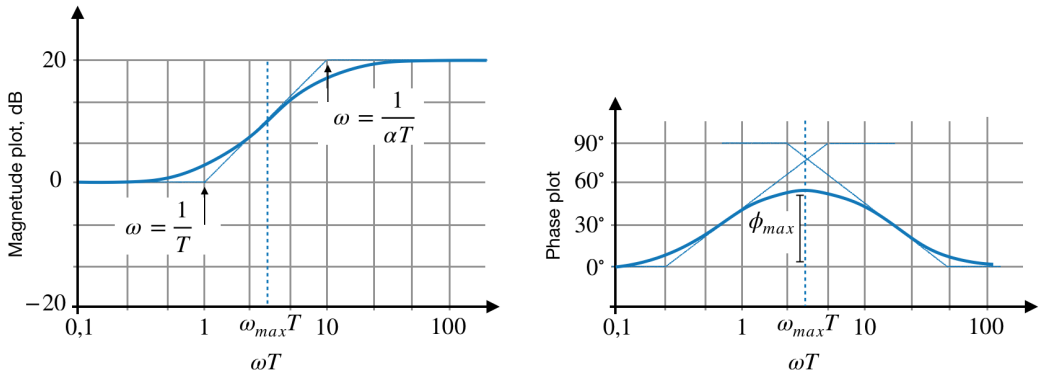


Figure 7.6: Bode diagram of lead compensator. Here $\alpha = 1/10$ [19]

The lead compensator is made up of a zero and a pole, and the distance between them determine the maximum phase lift ϕ_{max} located at ω_{max}. An extra ϕ_{max}=30° is necessary to exceed 45°. As the crossover frequency is expected to increase, ω_{max} is chosen to be 100.000 rad/s or 16 kHz. With ϕ_{max} and ω_{max} chosen, T and α can be determined.

$$\alpha = \frac{1 - sin(\phi_{max})}{1 + sin(\phi_{max})} = 0,33 \tag{7.19}$$

$$T = \frac{1}{\omega_{max}\sqrt{\alpha}} = 1,7321 \cdot 10^{-5} \tag{7.20}$$

The lead compensator becomes:

$$D(s) = \frac{1,7321 \cdot 10^{-5}s + 1}{5,773 \cdot 10^{-6}s + 1} \tag{7.21}$$

The bode diagram of $G(s)$, $KG(s)$, and $KD(s)G(s)$ is shown in figure 7.5a together with the step response in figure 7.7b.

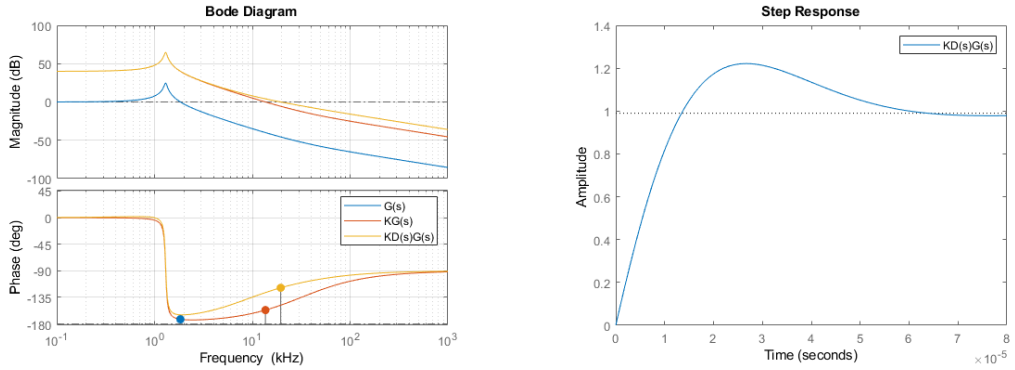


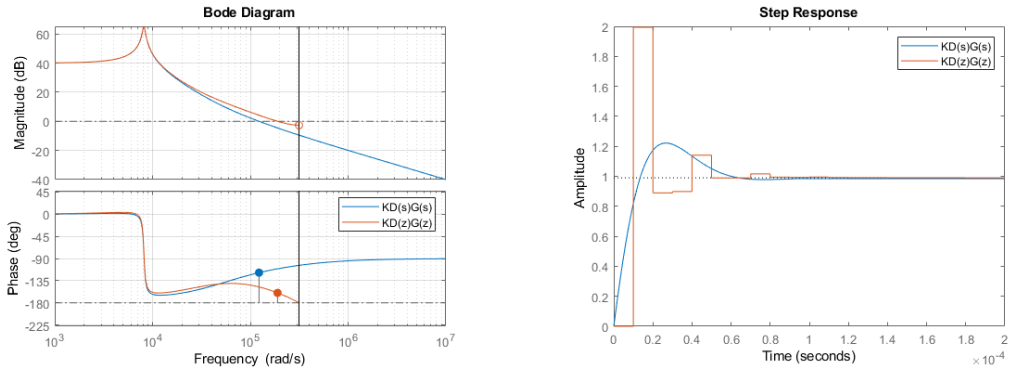
Figure 7.7: System response of $KD(s)G(s)$ control configuration

The phase has been lifted and results in a phase margin of 61,2°. The crossover frequency has increased from 13,6 kHz to 19,5 kHz. Both criteria of a steady-state error of 1 % and a phase margin larger than 45° has now been achieved.

To implement the controller on a digital device, it must be transformed into the z domain, which works with discrete signals rather than continuous time. A discrete controller can be designed from a discrete system or by transforming a continuous controller into the discrete domain, which is done in this case. A sample time T_s must be chosen, which determines how fast the controller acts on its feedback. If the sample rate is too slow, performance will be lost. In SMPSs, the switching frequency determines how often a change can excite the system, which sets the maximum sample rate. To start, the sample rate is chosen to be ω_s = 100.000 Hz, which is also the switching frequency. Using MATLAB and the zero-order hold method, $D(s)$ is transformed into z-domain. Figure 7.8 shows the bode diagram and step response of the system in continuous and discrete time.

$$D(z) = \frac{3z - 2.177}{z - 0.1769} \qquad T_s = \frac{1}{\omega_s} \tag{7.22}$$

It is clear from figure 7.8b, that the sample rate is too slow to match the performance of the continuous system. One solution to this is to increase the switching frequency,



(a) **(b)**

Figure 7.8: System response of $KD(z)G(z)$ control configuration

but this may lead to a re-evaluation of the inductor and capacitor size, not to mention increased switching losses.

Another solution is to increase the capacitor size, which is already small-sized compared to the inductor. This will change the dynamics of the system by increasing the damping and slowing the system down. With a new capacitor size of $C = 4700\ \mu F$, a new plant model can be determined called $H(s)$. The bode diagram of the system can be seen in figure 7.9

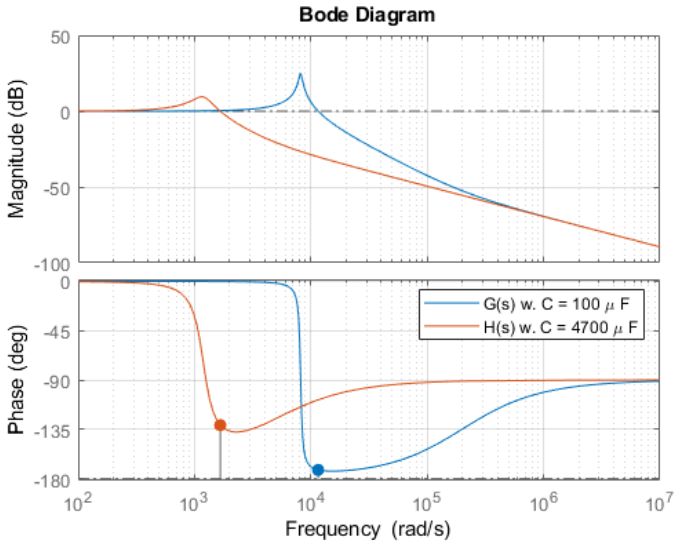
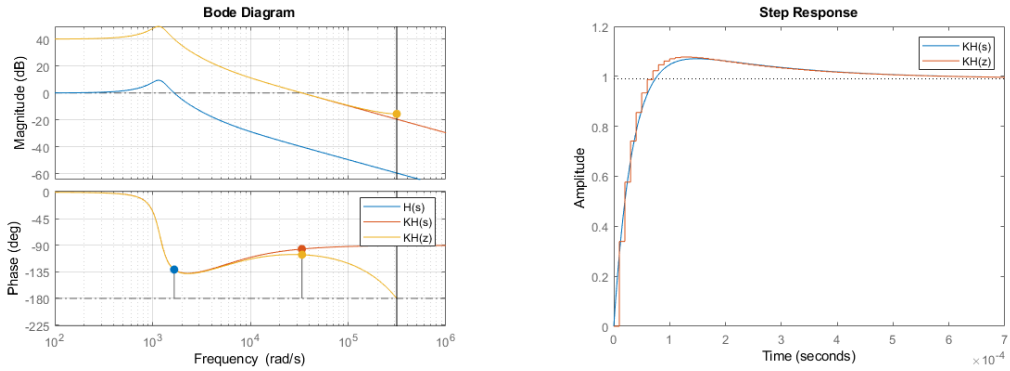


Figure 7.9: Bode diagram with new capacitance value

With an increased capacitance, the phase margin also increases to 48,7°, which makes it more stable. The K found in eq. 7.17 stays unchanged to give a steady-state error of 1 %. The control loop is transformed into z-domain again with $\omega_s = 100.000\ Hz$. Figure 7.10 shows the response of both the continuous and discrete system.



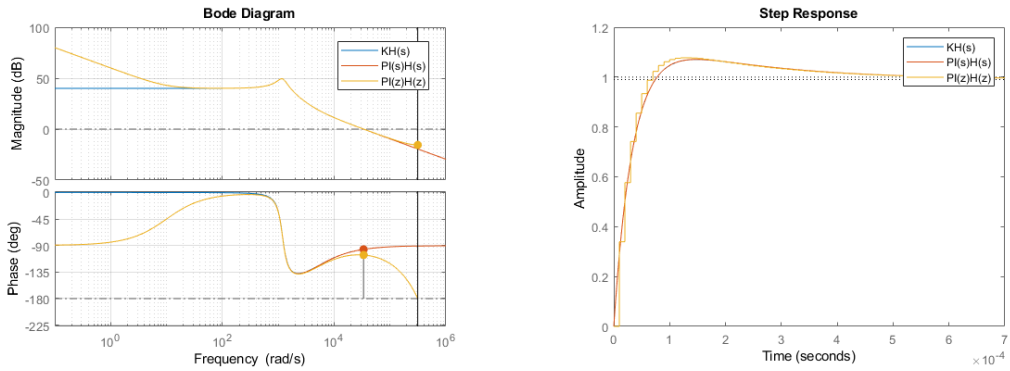
(a) **(b)**

Figure 7.10: System response of $KH(s)$ control configuration with $C = 4700\ \mu F$

Because of the increase in capacitance, the system has already now fulfilled all the criteria, as the phase margin has increased to 83,5°. The discrete control loop also shows good performance of $H(s)$. With little effort, the control loop can perform even better with a PI controller. For this system, it will only improve steady-state error by inserting a pole at zero frequency. To have nearly the same performance of $KH(s)$, the PI controller will have the following transfer function (both in continuous and discrete time).

$$PI(s) = \frac{100s + 1000}{s} \qquad PI(z) = \frac{100z - 99,99}{z - 1} \tag{7.23}$$

Figure 7.11 shows the system response with the $PI(s)H(s)$ configuration.



(a) **(b)**

Figure 7.11: System response of $PI(s)H(s)$ control configuration

The system has nearly the same performance but will have 0 % steady-state error, with the PI controller. The SBC will be simulated with the PI controller in chapter 8.

8 Simulation of SBC

This chapter simulates the SBC in MATLAB's simulation environment called Simulink. The simulation will be performed using a simple block diagram and using the library from Simulink with electronic components called *powerlib*. As the SBC should be compatible with and without an umbilical (see criteria IV in section 1.2), a brief description of the umbilical's effect will be covered. The converter will be disturbed with a change in input voltage and load. MATLAB simulation files can be found in appendix A.3.

8.1 The Umbilical

A simulation of the umbilical is carried out to investigate the properties of the umbilical and its effect on the converter. Figure 8.1 shows the simulation setup. A resistance load R_o is switched in with a pulse of 100 kHz and a duty cycle of 5 %. This simulates the load of the converter. C_i is the input bulk capacitor of 100 nF.

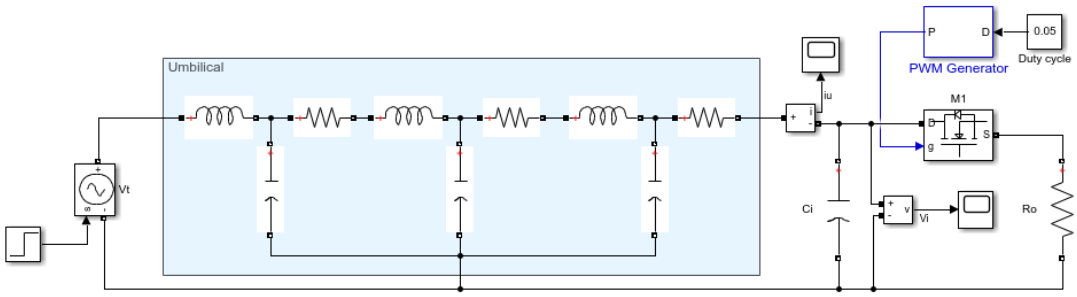
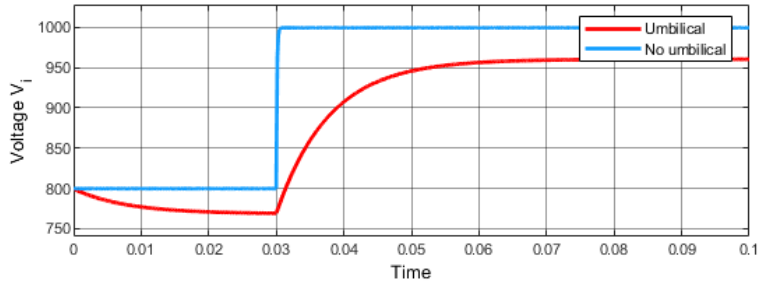


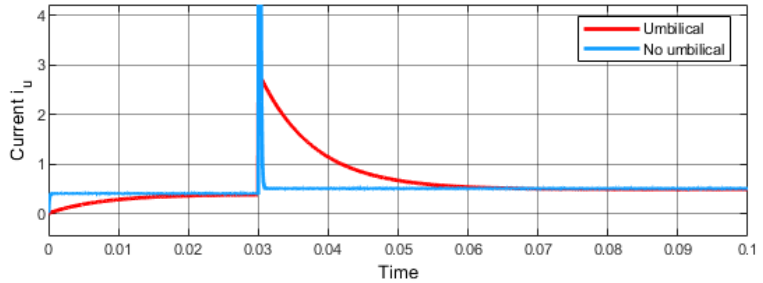
Figure 8.1: Electronic circuit of a 3 km umbilical

The umbilical electrical components are made up of inductance, capacitance, and resistance. The specific parameters are given for the umbilical to be 0,25 mH, 100 nF, and 27 Ω (see appendix A.1). The parameters are given per kilometer, which results in the configuration in figure 8.1 for a 3 km umbilical.

A simulation will be carried out to measure the input voltage V_i in order to investigate the effect of the umbilical. The topside power supply V_t will step from 800 to 1000 V. The result can be seen in figure 8.2.
In practice, the topside power supply will have some maximum ratings which cannot be exceeded. As an example, it could be rated at 3000 W and 1000 V, which would make a maximum current of 3 A. In the Simulink environment, it is not possible to implement a saturation current of a supply block, which is why the current of the no umbilical



(a) Input voltage to the converter V_i



(b) Current i_u

Figure 8.2: Voltage and current result with and without an umbilical

in figure 8.2b peaks at 200 A. Though with the umbilical, the input voltage slowly decreases and increases because of the resistance in the umbilical. As V_t steps from 800 to 1000 V, the C_i is charging, which is indicated in figure 8.2b at 0,03 s. The resistance of the umbilical restricts the current flow to charge C_i resulting in a steady increase in V_i.

Even though the voltage step of V_i with no umbilical is not realistic, as it is asking for 200 A, it will still respond quicker than with the umbilical. In practice, i_u with no umbilical, it will saturate at the maximum rating of topside power supply. The SBC must be capable of load and voltage regulating in the most extreme case. The results in figure 8.2, shows that this is with no umbilical attached. The transient response simulation in section 8.2.2 will be conducted with no umbilical.

8.2 Simulation of SBC

Two different simulation setups are presented; One using the *powerlib* environment in Simulink, and the other by building a block diagram from the governing equations given in section 7.1. In the block diagram setup, the system response of load and input voltage variation can easily be obtained. In the *powerlib* setup, the umbilical and MOSFETs can be implemented to investigate the steady state. In both setups, the feedback control loop is identical and is shown in figure 8.3.
The control loop consists of the feedback from the output voltage V_o where sensor noise is added as white noise. The noise has an amplitude of $\pm$ 50-100 mV. The $PI(z)$ controller is implemented with a small delay. The delay is set to 230 ns and is a signal delay between input and output of the IR2213 IC, see datasheet in appendix

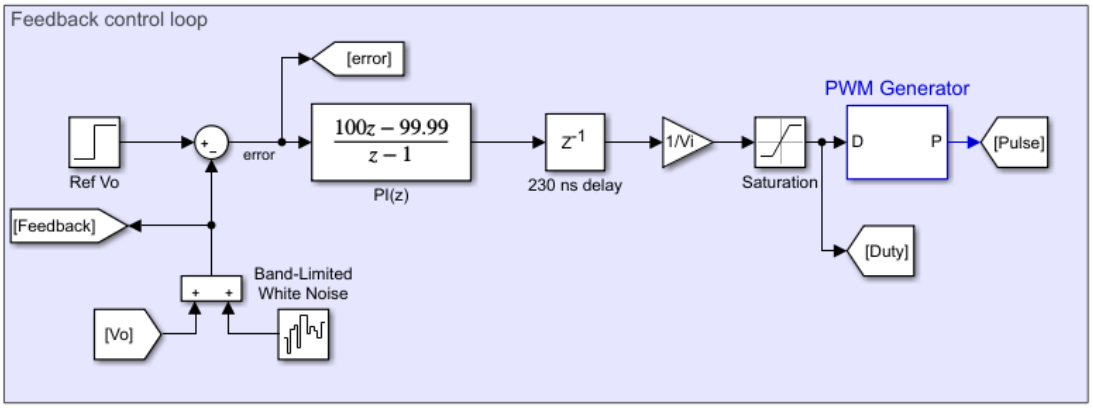


Figure 8.3: Feedback control loop

A.1. Because of the assumption that the input to the model can be seen as an average value, see section 7.1, the output of the controller is input voltage V_i and must be represented as a duty cycle. This is done by dividing the output of the controller with V_t. A saturation block ensures that the duty cycle is $0 < D < 1$ before entering a PWM generator. The PWM generator generates a pulse with a switching frequency of $f = 100\ kHz$.

8.2.1 Steady-state

In steady-state, the criteria of the voltage ripple ΔV_o and steady-state error e_{ss} are validated. Figure 8.4 shows the simulation setup.

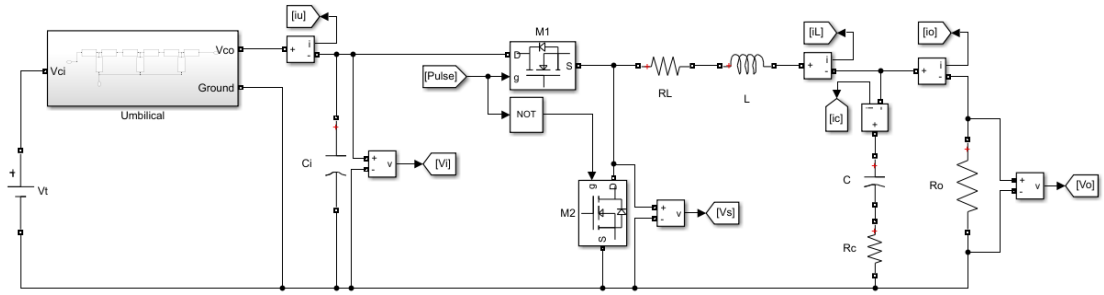


Figure 8.4: Converter simulation using *powerlib*

It consists of the topside power supply V_t, the umbilical of 3 km, the bulk capacitor C_i, and the configuration of the SBC. To validate the criterion of the buck converter and validate component size, the system is simulated at light load 10 W and full load 1500 W. Figure 8.5 shows the results of output voltage and inductor current.

The control and converter configuration shows good results with an output voltage ripple of less than 200 mV and a steady-state error of less than 1 % in average. The current ripple is less than 4 A, as expected, with an inductor of 150 μH.

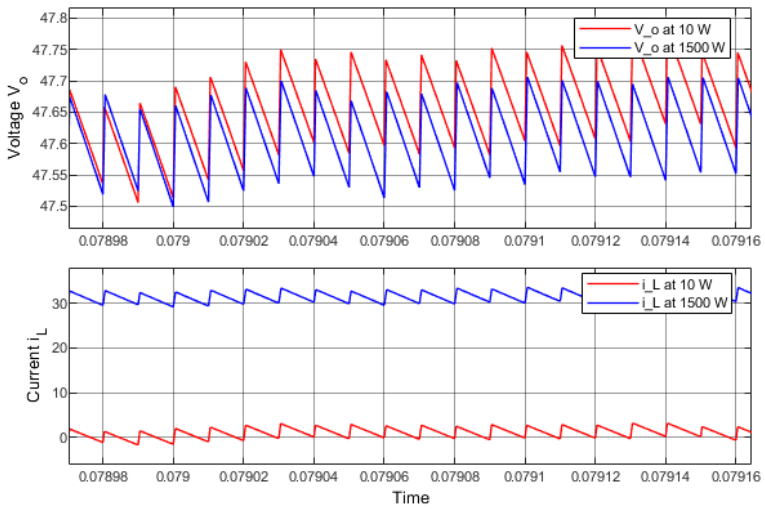


Figure 8.5: Steady-state of output voltage and inductor current

8.2.2 Transient Response

It is of interest to see the transient response of a load variation and a voltage input variation. In this setup, there is no umbilical, and the bulk capacitor C_i is assumed to be very large. Figure 8.6 shows a block diagram of the SBC with the same governing equations that determined the model $H(s)$.

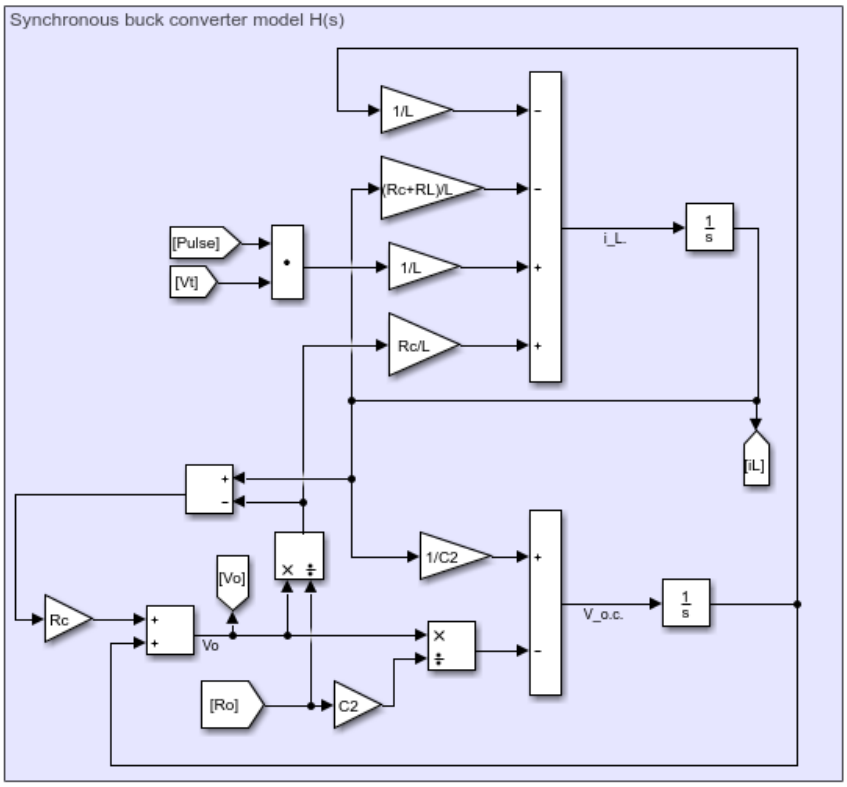


Figure 8.6: Block diagram of the SBC

In this setup, the input voltage V_t and load R_o can be changed independently. A simulation is carried out to see the transient response of the converter going from light load 10 W to full load 1500 W. Another transient will be initiated where the input voltage goes from 1000 V to 800 V. Figure 8.7 shows the response for output voltage, inductor current, and duty cycle. The load transient is initiated at time 0,028 s and the voltage at time 0,0286 s.

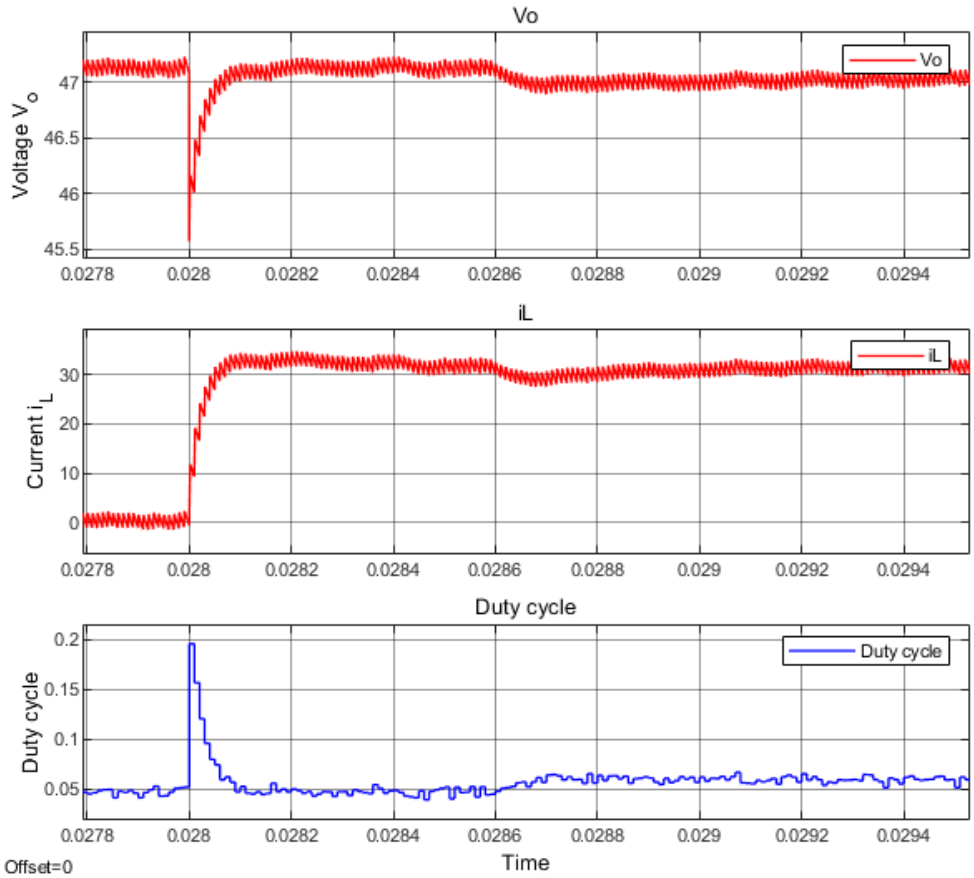


Figure 8.7: 10 W to 1500 W load transient at time 0,028 s. 1000 V to 800 V input voltage transient response at time 0,0286 s

The controller shows very good response with fast transient and a small undershoot of approximately 1,5 V. In practice, a load change of almost 1500 W is not realistic, but to investigate the tendency a load change of 500 W is simulated. This resulted in a voltage drop of only 500 mV. So the pattern is clear, that for every 100 W of load change, a voltage change of 100 mV is induced.

The voltage change at time 0,0286 s has no sudden effect on the system, but results in a small decrease in the output voltage of 1,5 V. This voltage will over time reach 48 V as the steady-state error is zero. The reverse transient response is shown in figure 8.8, where the transient goes from full load to no load and from 800 V to 1000 V.
It is clear that the duty cycle saturates at which point the controller is out of function. It basically closes the high-side MOSFET and waits until the output voltage falls below a specific value. This is where the conventional buck converter lacks in control margin,

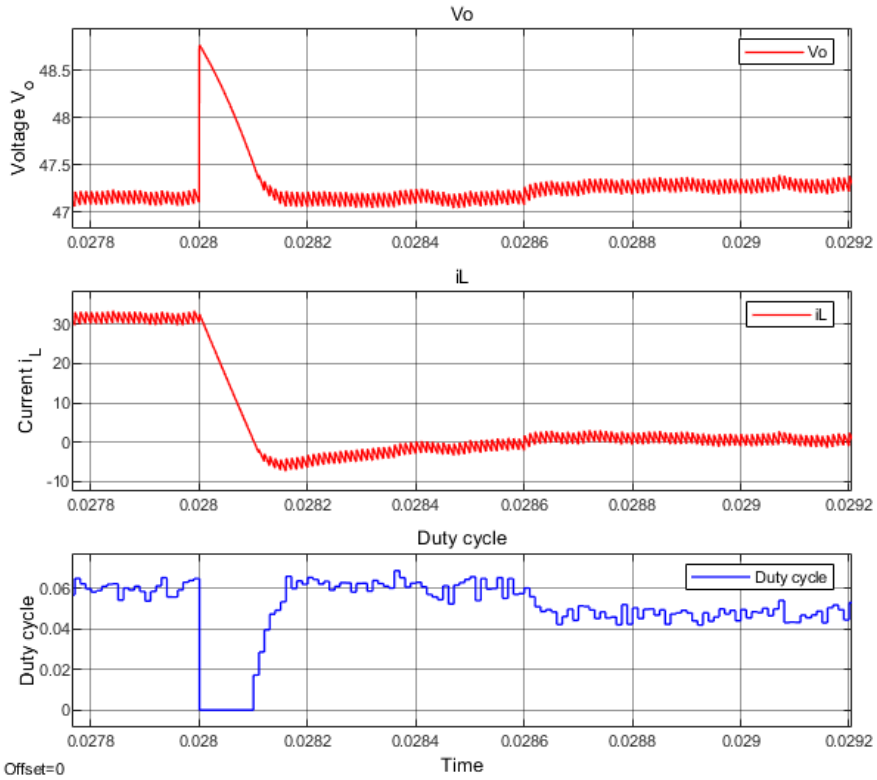


Figure 8.8: 1500 W to 10 W load transient at time 0,028 s. 800 V to 1000 V input voltage transient response at time 0,0286 s

but as mentioned before, it is highly unrealistic to see a load change of 1500 W. It is found that it has a good transient response at load changes of less than 500 W.

9 Experiment

With a SPICE simulation verifying the open-loop ripple, and switching behaviour, together with a full closed-loop simulation, the SBC is to build into a physical system. The responses determined in the simulations is to be compared to an actual setup. But building and testing a physical setup is challenging; It can result in multiple failures and is time-consuming. As a full voltage (1000 V) and load range (1500 W) test did not successfully occur, due to device failure, this chapter will focus on the many tests conducted in search of a solution. The experiments are only conducted in open-loop. In the end, the different observations will be discussed.

9.1 Setup

In chapter 5, different components was determined and selected, such as the SCT3080KL MOSFETs and IR2213 driver IC. These are fixed hardware throughout every experiment. The components of the power stage are selected based on MacArtney's electronic inventory and differ from the calculated values in section 5.4. Nevertheless, the circuit setup can be seen in figure 9.1. Figure 9.2 shows the physical setup.

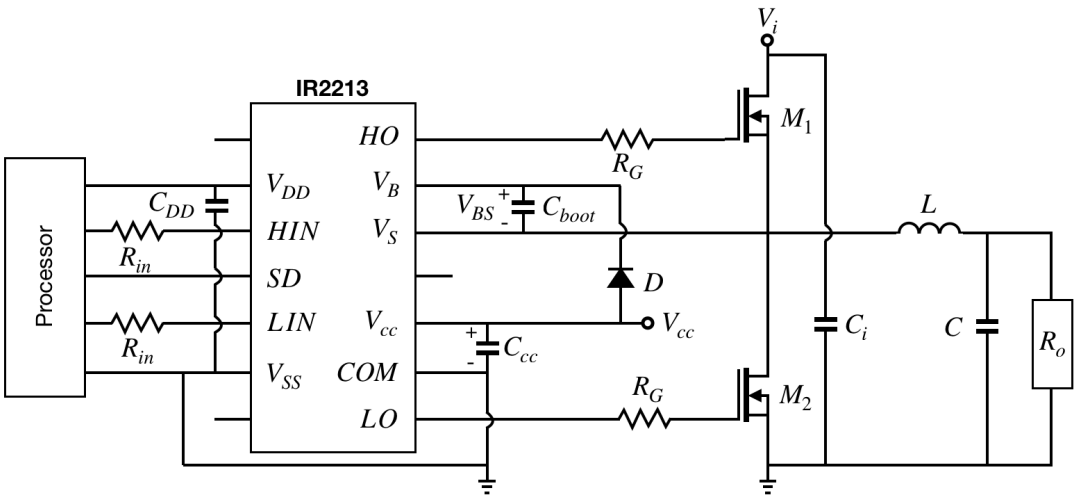
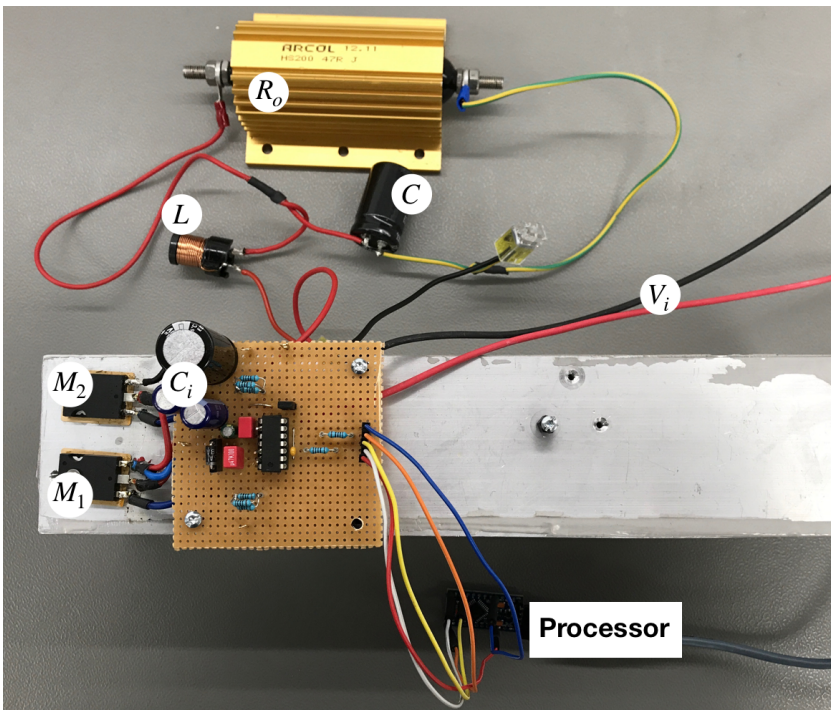
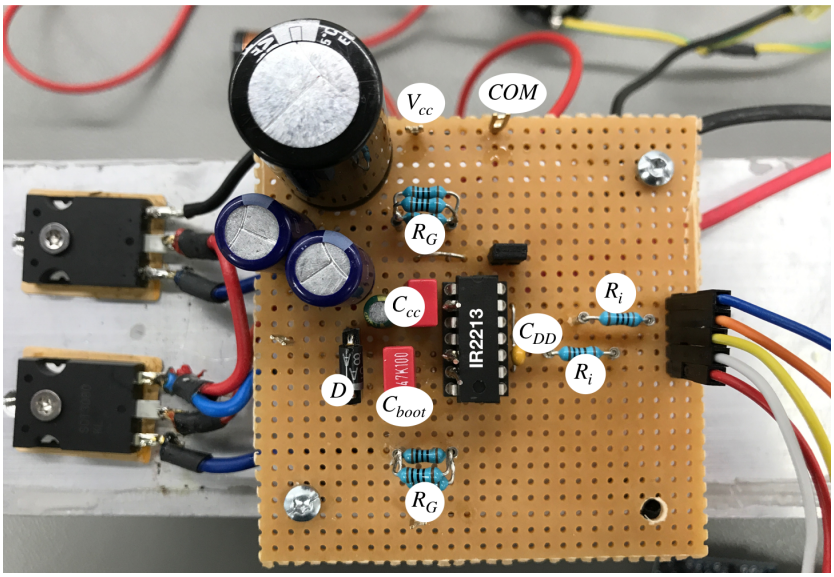


Figure 9.1: Circuit diagram of the synchronous buck converter

The IR2213 IC and MOSFETs will be briefly explained in section 9.2. As the SBC has two active switches, two PWM signals must be generated by the processor. The two PWM signals must be complementary and synchronous. The experiments are only conducted in open-loop, which means that less powerful processors are used, e.g. the Arduino Pro



(a) Power circuit



(b) Driver circuit

Figure 9.2: Picture of real physical setup

Mini and Due. These boards have internal timers, which can be set using registers, making it possible to operate at much higher frequencies than the default. Figure 9.3 shows the code needed to generate two synchronous PWM signals complimentary of each other on an Arduino Due. The frequency f ($T = 1/f$), duty cycle D, and deadtime d are set to 100 kHz, 5 %, and 5 % of the duty cycle, respectively.

In a preliminary experiment, it is observed that when the processor creates two PWM

```
void setup() {
  // put your setup code here, to run once:

  REG_PMC_PCER1 |= PMC_PCER1_PID36;                  // Enable PWM.
  REG_PIOC_ABSR |= PIO_ABSR_P5 | PIO_ABSR_P4;        // Set PWM pin perhipheral type B for pin 36 and 37.
  REG_PIOC_PDR |= PIO_PDR_P5 | PIO_PDR_P4;           // Set PWM pin 36 and 37 to an output.

  REG_PWM_CLK = PWM_CLK_PREA(0) | PWM_CLK_DIVA(1);   // Set the PWM clock rate to 84MHz (Master clock).
  REG_PWM_CMR1 = PWM_CMR_CPRE_CLKA| PWM_CMR_DTE;     // Setting the clock source as CLKA (84MHz) and enabling deadtime.
  REG_PWM_CPRD1 = 840;                               // Set the PWM frequency 84MHz/(840) = 100kHz
  REG_PWM_CDTY1 = 42;                                // Set the PWM duty cycle to 5% - 840*0,05=42
  REG_PWM_DT1 = PWM_DT_DTH(2) | PWM_DT_DTL(2);       // Setting deadtime to 5 % of the duty cycle 42*0,05 = 2
  REG_PWM_ENA = PWM_ENA_CHID1;                       // Enable the PWM channe

}

void loop() {
  // put your main code here, to run repeatedly:


}
```

Figure 9.3: Arduino Due enabling PWM registers

signals with zero deadtime, the IR2213 IC automatically sets a default deadtime to around 180-210 ns. It reduces the duty cycle at the output of the IC from approximately 5 to 3%. This can easily be adjusted by increasing the REG_PWM_CDTY1 number in the code. The deadtime is set to 10 % of a 5 %-duty cycle with a switching frequency of 100 kHz. This makes d=50 ns, and increases the IC default deadtime to 220-250 ns. The following experiments are conducted with a deadtime equal to the default of the IC, 180-210 ns.

9.2 MOSFET and Driver IC

The IR2213 IC has three signals from the processor and a logic level power connection. The signals consist of two synchronous PWM signals HIN and LIN, as well as a shutdown signal SD. The driver side is configured with an internal push-pull as explained in section 4.4. Exceeding the maximum ratings of the devices can cause damage to the IR2213 IC or SCT3080KL MOSFET. Table 9.1 lists these ratings. The values are given with respect to COM.

Table 9.1: Absolute maximum rating of IR2213 IC, see appendix A.1

Symbol	Definition	Min.	Max	Unit
V_B	High-side floating supply voltage	-0,3	1225	
V_S	High-side floating supply offset voltage	$V_B - 25$	$V_B + 0,3$	
V_{HO}	High-side floating output voltage	$V_S - 0,3$	$V_B + 0,3$	V
V_{LO}	Low-side output voltage	-0,3	$V_{CC} + 0,3$	
V_{CC}	Low-side fixed supply voltage	-0,3	25	

The voltage limits of the floating power supply can be rewritten. .

$$V_B - V_S < 25 \quad V_B - V_S > -0,3 \tag{9.1}$$

$$V_{HO} - V_S > -0,3 \quad V_{HO} - V_B < 0,3 \tag{9.2}$$

Application notes are published by the manufacturer of the IR2213, which explains and outlines various recommendation for different setups by applying their product. These can be found in appendix A.2.

The SCT3080KL MOSFET is a high-power switch with the absolute maximum rating provided in table 9.2.

Table 9.2: Absolute maximum rating of the SCT3080KL MOSFET, see appendix A.1

Symbol	Definition	Value	Unit
V_{DSS}	Drain to source voltage	1200	V
I_D	Continuous drain current	31	A
V_{GSS}	Gate-source voltage	-4 to 22	V

9.3 Experiments Conducted

Measurements are carried out using an oscilloscope with a 10x probe with reference to ground (COM) unless otherwise specified. The applied parameters of each experiment are listed in table 9.3 unless otherwise specified.

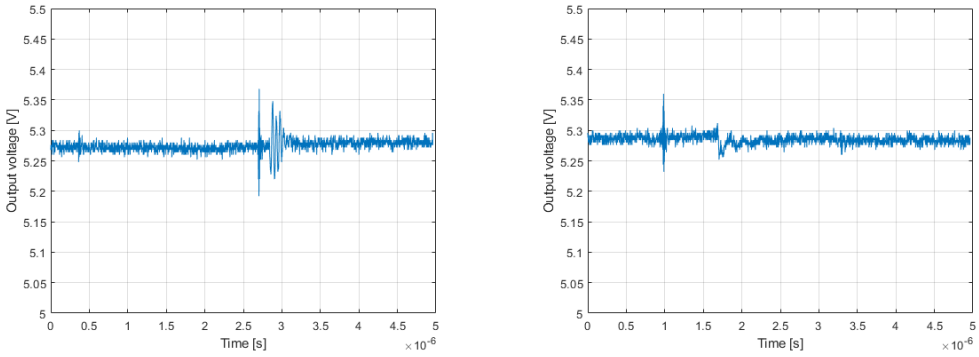
Table 9.3: Experiment parameters

Parameter	R_o	L	C	C_i	C_{cc}	C_{boot}
Value	9,7 Ω	330 μH	2200 μF	2,2 μF	22 μF	470 nF
Parameter	V_{cc}	V_{DD}	D	C_{DD}	R_{in}	R_G
Value	15 V	3,3-5 V	IN5408	100 nF	1000 Ω	33 Ω

Setup failure is typically caused by damage to the high-side MOSFET or permanent damage to the driver IC.The experiments seek to investigate potential causes of failure.

9.3.1 Probe Measurement Technique

Measurements of the output voltage shows significant voltage spikes in the switching transition. Figure 9.4 depicts the phenomenon.
The spikes are detected both when the high-side MOSFET M_1 turns ON and OFF, and becomes more significant when V_i or the load increases. Changing components does not aid to reduce the phenomenon, and therefore a new probe technique is tested. By shortening the probe ground wire, the phenomenon is significantly reduced. Figure 9.5 illustrates the extended ground wire with the corresponding result depicted in figure 9.4. The result of the shorter ground wire can be seen in figure 9.6.
The experiments show that an extended ground wire or reference signal can cause measurement error or noise. If unexpected voltage spikes are visible, a short probe reference wire is likely to ensure correct measurement.



(a) M_1 ON **(b)** M_1 OFF

Figure 9.4: Output voltage ripple

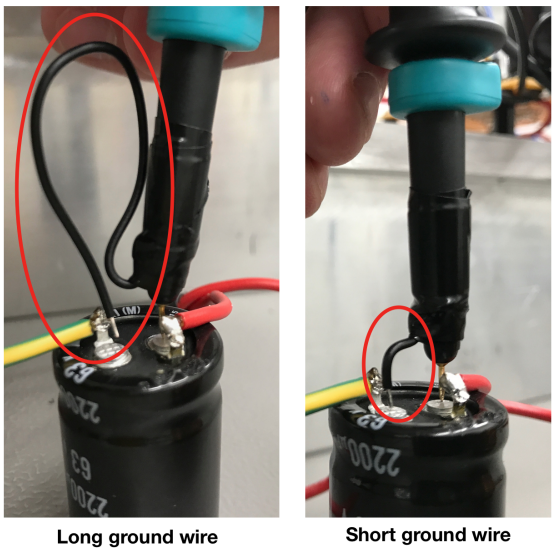
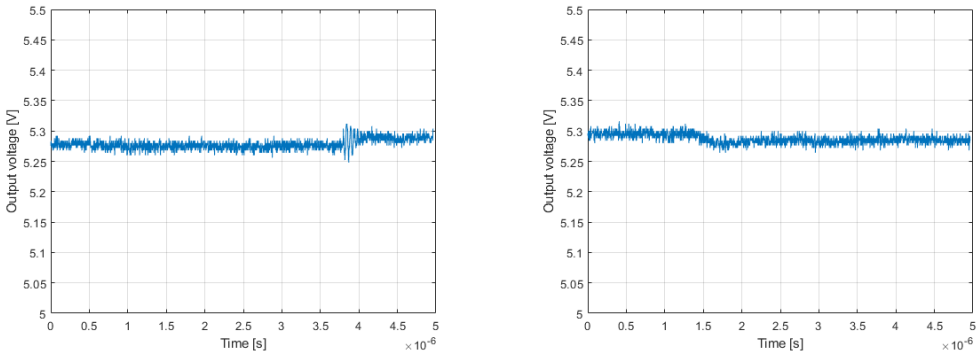


Figure 9.5: Different lengths of probe ground wire



(a) M_1 ON **(b)** M_1 OFF

Figure 9.6: Output voltage ripple

9.3.2 Gate Resistor

As the gate resistance determines the switching speed of the MOSFETs, and also introduces ringing, the effect is investigated. The voltage at the source terminal M_1, which is also equal to V_S of the IC, is measured. Input voltage V_i is held constant at 100 V, but the gate resistance R_G changes from 10-50 Ω. The results can be seen in figure 9.7.

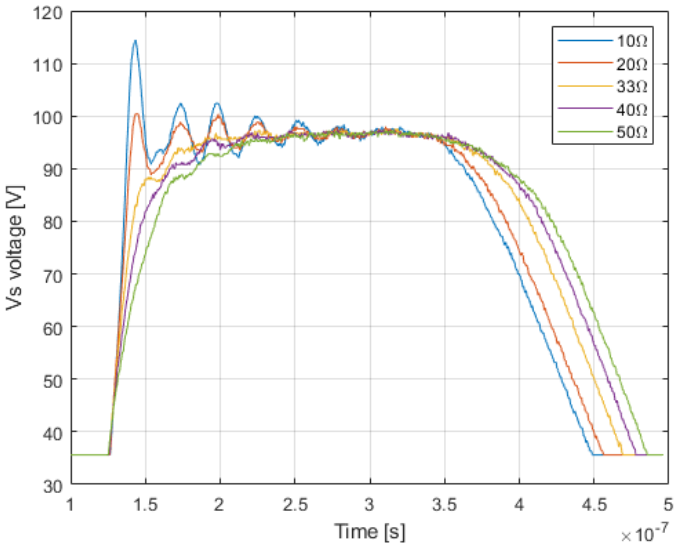


Figure 9.7: V_S voltage as a result of changing R_G, $V_i = 100\ V$

A $R_G = 10\ \Omega$ introduces large overshoots of nearly 15 % and large oscillation. Increasing to 33 Ω, the ringing reduces significantly. This slows the turn-ON and turn-OFF time of the MOSFET, but it is a compromise between speed, stability, and device stress. $R_G = 33\ \Omega$ will be used throughout the rest of the experiments.

9.3.3 Investigating V_S Undershoot

The IR2213 and the high-side MOSFET M_1 are prone to damage if the input voltage exceeds a specific value. It is not known in which order the devices fail or which device is causing the failure. It is observed that with an input voltage over 300 V and the parameters given in table 9.3, the circuit has the potential to cause a failure. The application note published by the manufacturer of the IR2213 IC warns against V_S transient and undershoot (see appendix A.2 for Managing Transients in Control IC Driven Power Stages). The IC is designed to work with a half bridge setup, as in this SBC. As the high-side MOSFET M_1 is activated with a voltage on the gate and reference to the source terminal, the IC must be connected to this point. This pin is called V_S and can be seen in figure 9.1. Except for COM, this is the only non-isolated connection from the low voltage driver circuit to the high voltage and power circuits. As wires are not ideal, a small amount of parasitic inductance is present between all of the devices in the circuit (L_{D1}, L_{S1}, L_{S2}, and L_{D2}). In the power stage, this can be seen between the two MOSFETs, see figure 9.8.

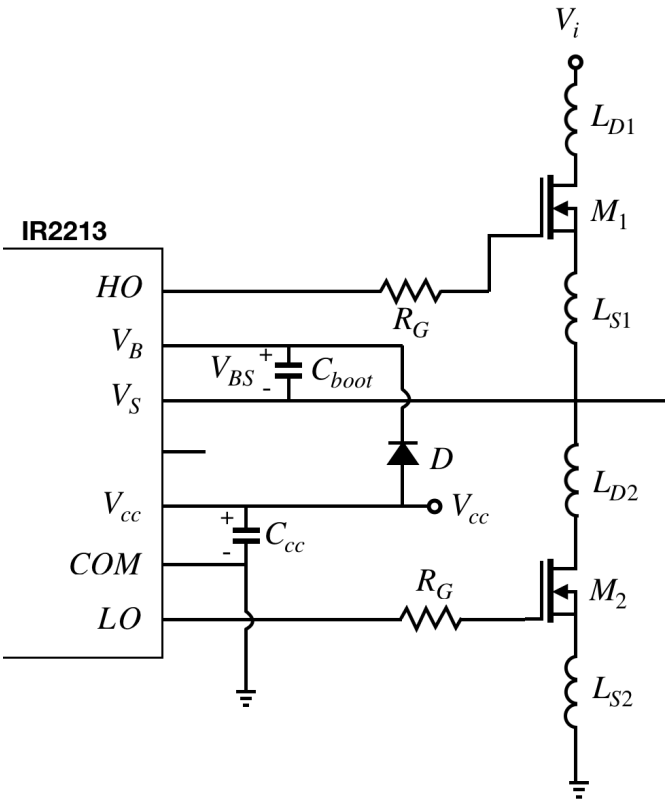
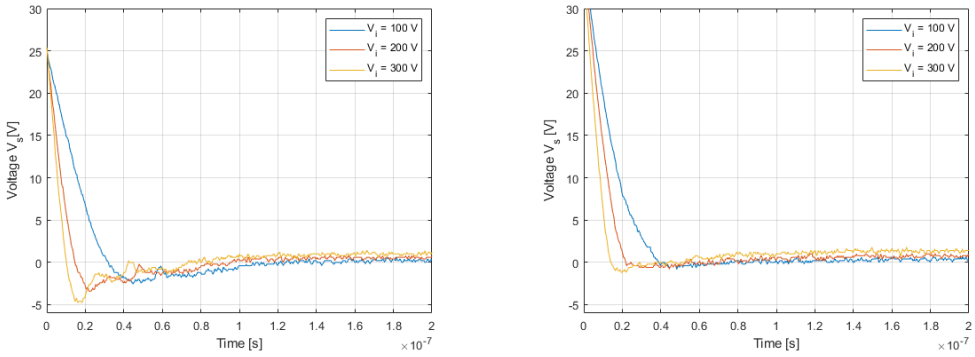


Figure 9.8: Parasitic inductance within a half bridge setup

This means that all the wires act like small inductors with the following dynamic equation.

$$V_L = -L\frac{di_L}{dt} \tag{9.3}$$

In a SMPS, where high voltage and current are switched ON and OFF continuously, large voltage spikes are present. Whenever M_1 is ON, a high current is flowing into the power stage. When M_1 is turned OFF, the high current goes from max value to zero in a small amount of time. In an inductor, see eq. (9.3), this induces a negative voltage drop across the inductor. Even though the inductance of a wire is small, it is sometimes enough to cause a significant negative voltage. To investigate this phenomenon, the voltage at V_S is measured directly on the IC pin to obtain the most precise data. By increasing the input voltage, the V_S voltage changes as seen in figure 9.9a.
Figure 9.9a shows the V_S transition when going from V_i to zero. As V_i increases from 100 V to 300 V, the undershoot goes from -2,6 V to -4,8 V. The IC has a protection feature that latches the high-side driver of the IC whenever a undershoot of -5 V is detected. The IC un-latch to normal when the undershoot surpasses -5 V again. This protection is never detected during the experiments, but as previously mentioned, when V_i exceeds 300 V, the IC is at risk of failing. Completing this experiment, the IC and M_1 were damaged at 350 V. The application note explains a scenario, where latching can damage the circuit instead of protecting it.



(a) Without D_S **(b)** With D_S installed

Figure 9.9: V_S undershoot detection against input voltage

To reduce the undershoot, the manufacturer recommends using thick wires, avoid interconnections, and place the MOSFETs and driver IC as close to each other as possible. On a Printed Circuit Board (PCB) design, these recommendations are more successfully achieved than with a prototype setup.

Another solution is to clamp the voltage across the IC with a diode D_S from COM to V_S, as seen in figure 9.10.

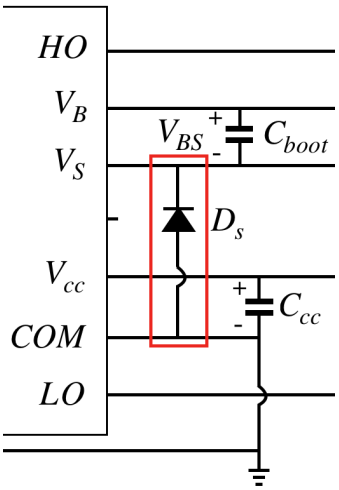


Figure 9.10: Installing of clamp diode D_s

This diode will conduct if a undershoot of more than the forward voltage of the diode is present. The selected diode is a 1N4007, which has a breakdown voltage of 1000 V, and a forward voltage drop of 1,1 V (see appendix A.1 for datasheet).

The results of the new installed diode D_S can be seen in figure 9.9b. The undershoot decreases significantly. As V_i increases from 100 V to 300 V, the undershoot goes from -0,8 V to -1,1 V.

Regarding projection of the IR2213 IC, the diode clamps a potential undershoot on pin V_S. Because of this implementation it is possible to increase the input voltage to above 300 V without detecting a faliure.

9.3.4 Maximum Ratings of V_{BS}

There is another potential issue of the V_S undershoot, which is explained in section 9.3.3. The issue is that the difference between V_B and V_S can potentially exceed the maximum rating of the IR2213 IC. A typical response of undershooting can be seen in figure 9.11.

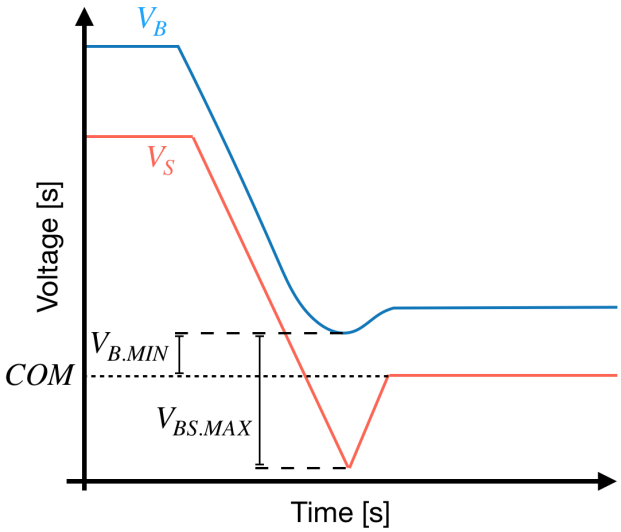


Figure 9.11: V_S and V_B response to undershoot

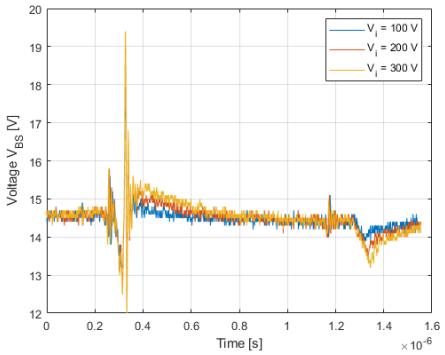
With the diode D_S installed, the minimum voltage of V_S is approximately minus the diodes forward voltage. The V_B follows V_S but can deviate at transitions.

This experiment measures the $V_{BS} = V_B - V_S$ voltage using a differential probe. The D_S diode is installed, the parameters of table 9.3 are applied, and the input increases from 100 to 300 V. The measurement is carried out directly on the IR2213 IC V_B and V_S pin. The results are shown in figure 9.12a.
At approximately time $0,2 \cdot 10^{-6}$, the MOSFET M_1 turns ON and at time $1,3 \cdot 10^{-6}$ it turns OFF. At turn-OFF, a small drop is detected due to the deviation of V_S and V_B at the transition. A significant voltage spike is also detected at the turn-ON of M_1. The maximum and minimum value of the voltage spike can be viewed in table 9.4.

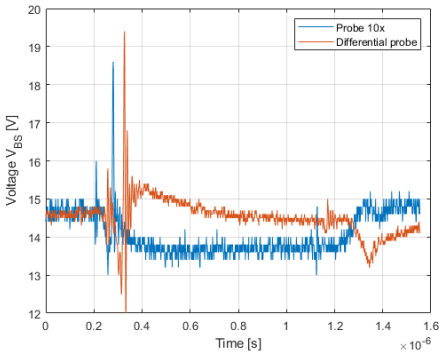
Table 9.4: Maximum and minimum values of V_{BS} voltage at different input voltages

V_i	**Min**	**Max**
100 V	13,0 V	18,3 V
200 V	12,3 V	19,2 V
300 V	12,0 V	19,4 V

As the input voltage increases, the maximum values of V_{BS} increases as well, and the minimum value stays at 12-13 V. These spikes are introduced because of a large de-



(a) V_{BS} over different input voltage



(b) Differential against probe 10x at $V_i = 300\ V$

Figure 9.12: Measurement of V_{BS}

viation between V_B and V_S. In section 9.2, the absolute maximum rating of the IC is presented and must be between $-0,3 < V_{BS} < 25$. Nevertheless, the rating is not exceeded.

Figure 9.12b shows a measurement at $V_i = 300\ V$ using the differential probe and a probe 10x. The differential probe measurements are greater compared to those of the probe 10x. This can be due to the long reference wires, as is explained in section 9.3.1. As no maximum ratings are exceeded, the measurement of the differential probe is accepted. As V_{BS} do not exceed its maximum rating, it is not likely that V_{BS} can cause any failure.

9.4 Discussion

The MOSFET and IC are at risk of damaged under certain conditions. It is investigated whether the cause is that the maximum ratings are exceeded. In section 9.3.3, a significant under-voltage of the V_S pin is detected. The IC is supposed to latch when $V_S <$ -5 V, but this is never detected. Instead, the IC is damaged. Installing the diode D_S results in a significant improvement. The V_{BS} is also investigated, but it does not exceed any maximum ratings. The improvement of installing the diode features good results, and allows for an increase of V_i to 600 V without failure. A new R_o of 47 Ω is used during this increase in input voltage. At $V_i =$ 650, V both MOSFETs are damaged, but the IC continues to be operational. Since V_{DSS} is 650 V and I_D is 0,7 A ($I_D = V_{DSS}/R_G$), they are unlikely to be the cause of the damage as the MOSFET's maximum ratings are well above those values, see table 9.2. Another possible cause is the gate-source voltage, which must not exceed $-4 < V_{GSS} < 22$. This could potentially damage the device.

10 Discussion

This chapter is concerned with the many factors and problems encountered in the report. Choosing the optimal topology for this DC/DC conversion is difficult, because many factors are adjustable. This makes the decision process challenging. The disadvantage of the SBC is that it needs to operate at an extremely low duty cycle compared to other topologies presented in section 2.2. Device stresses, component numbers, operation mode, and complexity are some of the factors that must be considered. The SBC has high device stresses, which makes it difficult to determine a proper inductor size. However, it is more straightforward to identify MOSFETs that ranges up to 1700 V and can deliver high currents. Components are found at Mouser, RS Components, and Farnell. No significant issues are found during the design of the SBC.

In section 5, the components and parameters of the SBC are determined. As mentioned in this section, this is typically an iterative process as some parameters are difficult to determine before testing the system. The switching frequency can, in theory, be restricted by the MOSFET's turn-ON and OFF time and power losses. The power losses determine how much heat must be transferred away from the device. As the enclosure of the SBC is not fixed, no limitation on power loss is given. But MacArtney mentions that 200-350 W of heat can be challenging to dissipate. Components like the gate resistors must be selected so as to not affect the system with large osculation but must also ensure fast switching procedure. The optimal operation point can be determined by adjusting the gate resistor and switching frequency. This will affect the power loss, components size, and control dynamics. A switching frequency of 100 kHz is chosen to keep power losses low.

The inductor size is the most difficult component to determine. This is not due to a complicated equation, but rather because not many inductors above 100 μH exists with the given current rating as of-the-self products. Here, increasing the switching frequency will benefit the process.

A problem is encountered during the control design process in chapter 7 as the controller is designed to respond quicker, than what it is capable of. The sample rate, when discretizing the controller, is restricted by the switching frequency. Instead of redesigning the controller and risk complicating the control design, the system bandwidth is decreased by increasing the output capacitor size. This benefits the system as it becomes more stable without a control unit. Another way to explain this is that the charge of the new capacitor has increased, so that it can more easily compensate for a load change. Through simulation it is found that the control unit is capable of maintaining 48 V at the output whenever a load or input voltage change is detected. Note that steady-state

error is zero. However, it takes a long time for the output to reach 48 V, which can be seen in the figures in section 8.2.2. At one point during simulation, the voltage change exceeds the steady-state error criteria of 1 %. This must be verified in an actual setup to determine if it poses a problem.

When it comes to implementation and experimental setup, many challenges and problems were observed. The IR2213 IC driver and MOSFETs were damaged multiple times during testing. Application notes from the manufacturer of the IC were utilized. Several experiments were conducted to investigate potential problems. When working with SMPS, it is good practice and recommended to place the switching stage components as close to each other as possible. In a prototype setup, this is very difficult. With the current setup in chapter 9, long wires are connecting the components. This introduces small values of inductance around the circuit, which can be problematic for the switching stage. A clamping diode was found to protect the IR2213 IC against an undershoot. With the clamping diode installed, another failure is detected, and both MOSFETs were damaged. It is expected that the gate-source voltage experiences an undershoot which exceed -4 V. With the presented setup, it was not possible to get the SBC to function at full voltage and load. For future work, a proper Printed Circuit Board (PCB) must be designed to decrease parasitic elements and place components as close to each other as possible. A protection circuit must also be considered as clamping diodes can aid against undershooting.

11 Conclusion

In accordance with the thesis objective in section 1.3, several topologies of SMPSs are described and presented. A Synchronous Buck Converter is analyzed in two stages called switching and power. Based on the analysis of the switching and power stage, it is possible to dimension the size of the components of the SBC. A control unit is determined which fulfills the given criteria. Though a small control margin can be a potential issue when tested on a physical setup. Simulation in LTspice and Simulink shows good steady-state and transient response behavior. It was not possible to get a physical system running satisfactorily, as the switching stage lags protection and research. Future research must be done on the physical setup and how to protect the components.

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A Appendix

The following documentation is attached in a Zip file containing corresponding folders.

A.1 Datasheets

Including documents:

- Diode IN4007
- IR2213 IC driver
- Parameters of Tow cable
- SCT3022KL
- SCT3080KL
- Tamura inductor
- Tow cable
- Vicor converter
- Vishay inductor
- Vishay saturation current

A.2 Application Notes

Including documents:

- Bootstrap Network Analysis
- HV Floating MOS-Gate Driver ICs
- Managing Transients in Control IC Driven Power Stages

A.3 MATLAB & Simulink

Including documents:

- *BuckConverter.slx* - SBC setup using *powerlib*. Run *ControlCalculation.m* before use.
- *BuckConverterBlocks.slx* - SBC in block diagrams. Run *ControlCalculation.m* before use.
- *ControlCalculation.m* - Component selection and control design.
- *Figure_generator.m* - Plots graphs of the experiments using the data in the Workspace folder.
- *Workspaces* - Data from experiments.

A.4 SPICE Simulation

Including documents:

- *SynchBuckConverter.asc* - SBC SPICE simulation.