Battery Tester

Test System to Verify the Reliability of Lithium Ion Batteries under Pulse Charge and Discharge Conditions

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Synopsis:

An surge in electrification of both transportation and energy sector has lead to an increased investment in battery technology development and mass production. As a result, the price per kWh for lithium ion batteries has dropped significantly, making this battery technology a feasible competitor with respect to energy storage. The integration of lithium ion batteries into new application areas has raised the need to develop test setup capable of performing accelerated life time test of the batteries, in order to prolong the lifespan of the batteries, since none or limited amount of data is available, depending on the application area of interest.
This report has investigated possible topologies suitable for testing batteries under pulsed charge and discharge operation. Two topologies were evaluated and discussed and as a result it was decided to build a prototype. the performance of the prototype showed a great potential and it was concluded that a further study would be necessary in order to make a final conclusion.

Summary

Research within the field of battery diagnostics is of growing interest, due to the incremental implementation of lithium ion batteries into the transportation and energy sector. Global warming has been a hot topic the last decades and batteries are considered as a vital piece of the puzzle when it comes to building the foundation, that will enable an accelerated transistion towards a more sustainable future, for generations to come.

The importance of battery diagnostics of lithium ion batteries is vital, in order to ensure successful implementation of lithium ion batteries into new application areas, hence prolonging the life time and reducing cost.

This thesis investigates the physicals aspect of battery diagnostics, striving to develop, build and test equipment necessary to stress test batteries. Implementing batteries into fields that have not yet been exploited, has the downside of every other frontier, namely the absence of references and experience within the field of interest.

In collaboration with KK Wind Solutions, specifications has been provided for this thesis, describing the operational conditions of a battery system of interest. The desired output of this thesis is to use the specifications provided to design a test system capable of performing accelerated testing of lithium ion batteries, with the purpose of mapping and predicting the performance of the batteries, in order to optimize the system and reduce cost.

Project objectives were made in order to facilitate the process of finding a solution. The objectives were to investigate different converter topologies and systematically investigate the capabilities and limitation, with respect to the specifications provided, through computational calculation and simulation. Once a suitable candidate was found a prototype was made and tested systematically to validate the performance.

As a result, it was possible to find candidate made from a configuration of multiple h-bridges, which has the capability of testing multiple lithium ion battery cells simultaneously, using an intelligent current control scheme to control the current used to stress test the batteries. The test results showed high resemblance, with respect to the specification provided, hence making it a candidate worth investigating as it show great potential.

Furthermore, an analysis was made stating some of the problems encountered, that needs further improvement before making a final judgement. Suggestions has been made, stating possible solutions, revolving around closed loop control implementation, DSP code optimization and system configuration to fine tune the performance according to the specifications provided. Based on the analysis made throughout the thesis, and the suggestion made with respect to improved performance, it is believed that candidate presented is capable of performing according to the specifications provided.

Preface

Acknowledgement

Foremost, I would like to convey my gratitude to both my supervisors Prof. Francesco Iannuzzu and Asst. Prof. Dao Zhou for the substantial amount of support, motivation and knowledge, that they have provided throughout the extend of the entire project. Their guidance has been a true inspiration for me and I could not have asked for better advisors.

Besides my supervisors I would like to thank Res. Asst. Martin Bendix Fogsgaard for providing constructive feedback and encouragement. His input to the project has been highly appreciated.

A special thanks also goes to Anders Eggert Maarbjerg, Lorand Bede and Bjørn Rannestad from KK Wind Solutions, for giving me the opportunity to be part of such an exiting project. They have been providing an extensive amount of support, including a visit at their headquarter in Ikast, skype meetings, mail and phone correspondence and components for the test setup. Their support and engagement has been a great motivation.

Finally I would like to thank Walter Neumayr, Mads Lund and Frank Rosenbeck for providing practical and insightful knowledge during construction of the test setup.

Reading Guide

Each chapter is introduced by a short paragraph written in *italic* form. These paragraphs are introductions for the given chapters. There will appear source references through the report. These references will be collected in a source list at the end of the report. The reference method used in the report is the Harvard Method which means that the reference is placed in the text with following notation [Surname, Year]. If the reference contains multiple sources, then each source is separated by comma. The references refer to the list of sources where books is stated with author, title, publisher, edition and year of publication while web pages is stated with author, web address, title and the point of time that indicates the last visit at the web page. Equations, tables and figures are numbered in accordance with the given chapter, i.e. Figure 1.2 is the second figure in chapter one. Explanatory text for figures and tables is located beneath the given tables and figures.

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Nomenclature

AC	Alternate Current	
ADC	Analog to Digital Converter	
BMS	Battery Management System	
CC	Constant Current	
CCS	Code Composer Studio	
CV	Constant Voltage	
DC	Direct Current	
DCM	Discontinuous Conduction Mode	
DSP	Digital Signal Processor	
EV	Electric Vehicle	
IC	Integrated Circuit	
KVL	Kirchhoffs Voltage Law	
OCV	Open Circuit Voltage	
PLL	Phase Locked Loop	
PM	Permanent Magnet	
PWM	Pulse Width Modulation	
SoC	State of Charge	
SPWM	Sinusoidal Pulse Width Modulation	
SVPWM	Space Vector Pulse Width Modulation	
THD	Total Harmonic Distortion	
η	Efficiency	[%]
R	Resistance	[Ω]
$\mathcal{E}$	EMF	[Vt]
B	Magnetic Flux Density	[Wb]
C	Capacitance	[F]
D	Duty Cycle	[-]

E	Energy	[Wh]
f	Frequency	[Hz]
H	Magnetic Field	[T]
I	Current	[A]
K	Constant	[-]
L	Inductance	[H]
P	Power	[W]
Q	Charge	[C]
t	Time constant	[s]
V	Voltage	[V]

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1 Introduction

1.1 Background

An increased interest within battery driven systems has occurred during the last couple of years. Examples of such battery driven system could be electrical vehicles (EV´s), or electrified transportation in general, including bikes, skateboard, scooters, etc. Other battery driven system of high interest is a more stationary implementation and refers to energy storage systems, such as the Tesla Power Wall.

Numerous battery technologies exist and they all have different characteristics. Choosing a suitable battery technology for a certain application is typically done based on two parameters. One being the specific energy expressed in Wh/kg and the other being the specific power expressed in W/kg. A comparison of different battery technologies can be seen in the ragone plot, illustrated in Figure 1.1.

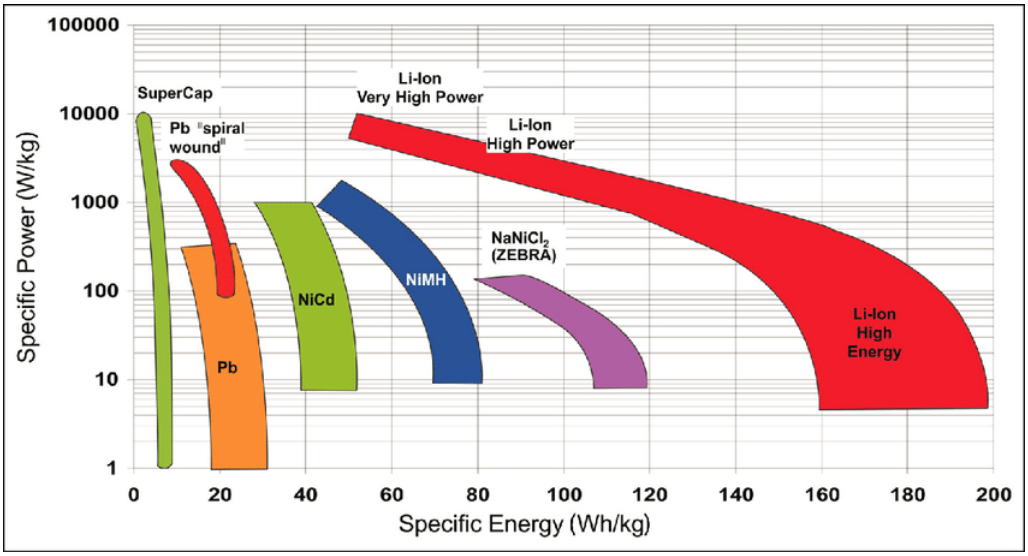


Figure 1.1: Comparison of specific power and specific energy between different battery technologies [Budde-Meiwes et al., 2013].

From Figure 1.1 it can bee seen that the lithium ion technology has the highest value with respect to specific energy, which is why this technology has been chosen for battery driven systems, such as EV's, as range is an important factor.

The increased interest in battery driven system has resulted in big investment within battery development and mass production, which has lead to a decreasing tendency in cost per kWh, as illustrated in Figure 1.2.

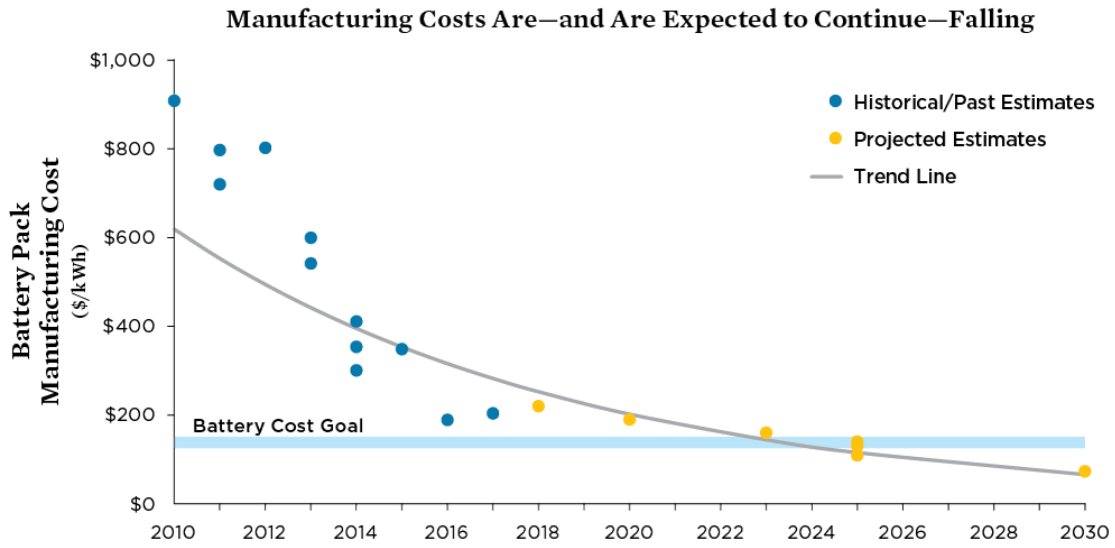


Figure 1.2: Battery pack manufacturing cost tendency and prediction in $/kWh for lithium ion battery packs [David Reichmuth, 2017].

The lower price tag per kWh of batteries has made batteries a economical feasible solution with respect to renewable energy storage and the advantages it offers.

Advantages of Batteries Used for Energy Storage:

- High frequency response compared to traditional grid stabilizing methods, such as mechanical turbines.
- Optimized integration and utilization of fluctuating renewable energy sources, such as photo voltaic systems and wind turbines.
- Reduce peak load which reduces the size and cost of the utility grid.
- Possibility of extending the lifetime of batteries used for electric vehicles by using them for energy storage, as capacity decreases, making them unsuitable for EV´s.

Other forms of energy storage already exist, such as pumped hydroelectric storage. However, this form of energy storage is rather limited from a geographical point of view, as it requires a landscape with high elevation differences.

With reference to the statement mentioning capacity degradation, it is important to extend the life time of the batteries, for them to be an economical competitive solution that can help face out the use of fossil fuels used within the transportation and energy sector.

1.2 Problem Analysis

1.2.1 Lithium Ion Battery

Being able to extend the life time of lithium ion batteries, requires a fundamental understanding of the battery structure, including electrical, chemical an mechanical properties.

A simple structural and operating description of a lithium ion battery can be made from the following four elements. Electricity in a lithium ion battery is generated through chemical

reactions of lithium and the following four elements all needs to be present within a lithium ion cell structure in order to create such a chemical reaction [SDI, 2016].

- **Cathode:** Is the positive electrode of the cell, and is made out of lithium and a oxidized material, which creates an active material that determines the voltage and capacity of the battery depending on amount of lithium used and type of oxidizing material. Lithium is an unstable substance in its element form, hence it is paired with another material to become stable.
- **Anode:** Is the negative electrode of the cell, and is made out of an active material that enables electric current to flow trough an external circuit and absorb/release lithium ions from/to the cathode depending on the power flow direction.
- **Electrolyte:** Is a medium located between the cathode and the anode that allows the movement of ions only, not electrons.
- **Separator:** Is a physical barrier that prevents direct flow of electrons from cathode to anode, which would cause short circuit.

1.2.2 Charging Strategies

Since batteries are used to store and release energy, it is important to investigate the practicality of this process to fully understand the nature of the batteries.

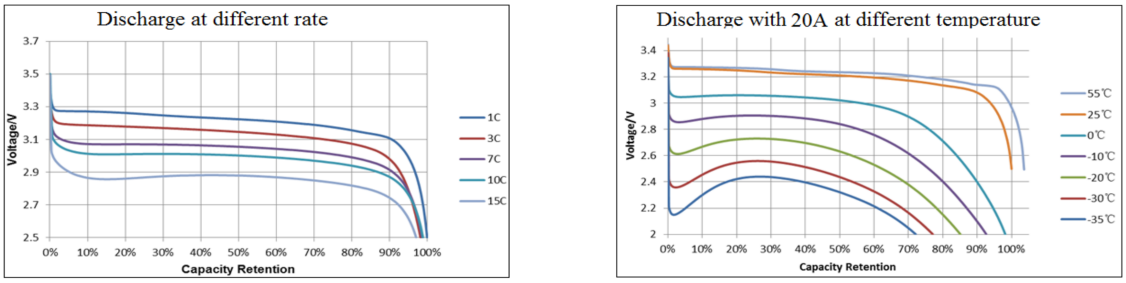
Constant Current (CC)/Constant Voltage (CV)

This charging strategy is a combination of two different strategies, as indicated by the name, and is commonly used to charge lithium ion batteries. Only one strategy is used at the time and knowing when to choose one over the other depends on the state of charge (SoC) of the battery.

The SoC indicates the amount of charge in a battery ranging from 0-100 %. Various method of determining the SoC exist, whereas the most common method is to measure the battery open circuit voltage (OCV), as it decreased during discharge and vice versa. The measured open circuit voltage is compared with a characteristic discharge curve, stating the battery voltage at different discharge rates with constant temperature or different temperatures and constant discharge rate, as illustrated in Figure 1.3.

The CC charging strategy is utilized when having a low SoC and OCV and is used until a specified OCV is reached. When a specified OCV is reached the CV charging strategy is utilized, keeping a constant voltage while lowering the current. Lowering the current, serves the purpose of protecting the battery, as it can cause permanent damage to the battery if it is overcharged. Looking at the OCV characteristics in Figure 1.3a, it can be see that the OCV voltage changes exponentially at low and high state of charge, hence it is important to charge slowly to keep track of the OCV.

Since current decreases whenever a certain maximum voltage is reached, so does the power flow, which has a negative impact on charging time [Cope and Podrazhansky, 1999].



(a) Constant temperature.

(b) Constant discharge rate.

Figure 1.3: Discharge curves at different discharge rates at constant temperature **(a)** and discharge curves at constant discharge rate at different temperature **(b)**, taken from Appendix A.

Comparing the voltage of both graphs, it can be seen that higher temperature result in lower charge rate and vice versa. Furthermore, it is interesting to observe that capacity loss occurs at low temperature caused by a voltage offset of $\approx$ 1V from the highest voltage rating.

Since higher current result in higher temperature it is an advantage to perform thermal management of batteries as it can improve both charge speed and available capacity.

Pulse Charging

As the name of this charging strategy indicates, it utilizes current pulses to charge and discharge batteries. Pulse charging is characterized by a discontinuous power flow, since the current flow is interrupted by small breaks. These breaks is referred to as resting periods and serves the purpose of allowing higher charge current than other charging strategies such as the CC/CV charging strategy. From the discharge curves presented in Figure 1.3, it was observed that high current rates causes noticeable voltage offsets and that higher temperature decreases charging rate. Therefore, implementing resting periods through the pulse charging strategy, allows the battery to cool down and stabilise the voltage, when applying a high current. Applying a high current through pulses would result in an average current higher than normal for the same time period. Higher average current at higher voltage yields higher power, which in the end reduces charging time [Cope and Podrazhansky, 1999].

1.2.3 Battery Degradation Diagnostics

Figure 1.4 presents a schematic overview of the causes and effects of different degradation mechanisms and associated degradation modes, which is based on a study within the field of degradation diagnostics of lithium ion batteries[Birkl et al., 2017].

The study investigates, what causes effect the capacity and power fade seen in lithium ion batteries. From Figure 1.4 it is observed that current load at high and low SoC and high temperature are the most damaging causes that effect mostly capacity , but also power fade. Measuring and controlling these parameters is therefore a good starting point in order to enhance the performance of lithium ion batteries.

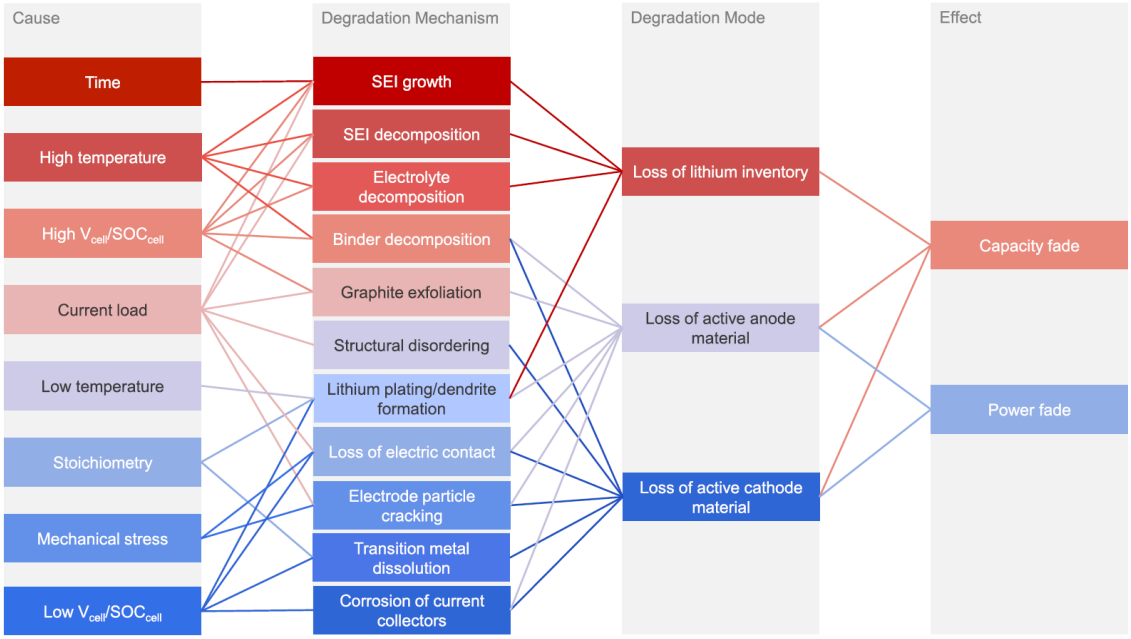


Figure 1.4: Cause and effect of degradation mechanisms and associated degradation modes[Birkl et al., 2017]

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This project is made in collaborating with KK Wind Solutions, who are interested in product development that utilized lithium ion batteries as energy storing devices that are integrated into the grid. Since the application of lithium ion batteries are broad and constantly evolving, it can be difficult to predict the performance off the batteries when implementing the technology into a knew application, since the amount of comparable data is either limited or non existing. The following test specifications, listed in Table 1.1, has been provided by KK Wind Solutions, representing the conditions of which the system is intended to be operated.

Charge Rate	**Discharge Rate**	**Pulse Duration**
$100A/\mu s$	$25A/\mu s$	$100\mu s - 10ms$

Table 1.1: Test setup specifications.

Based on the analysis made in Section 1.2 and the specifications listed in Table 1.1, it would be of interest to build a test setup capable of stress testing the batteries, under pulsed operation, in an accelerated manner, to generate relevant and comparable data that can be used to optimize the operation of the application of interest.

Problem Statement 2

Based on the analysis, made in Chapter 1, it is possible to frame the following problem statement for this master's thesis.

How can a system, with charge and discharge rate capabilities of $100A/\mu s$ *and* $25A/\mu s$ *and pulse duration of 100µs - 10ms be designed, to perform accelerated lifetime test of lithium ion batteries used under pulsed operation.*

2.0.1 Project Objectives

In order to reach a conclusion, following objectives has been listed to facilitate an answer to the problem statement made.

- Identify a suitable converter topology capable of performing according to the specification made in Table 1.1.
- Use Matlab and Simulink to model and evaluate the converter topology.
- Make a prototype of the selected topology.
- Perform test of the prototype according to the specifications made and validate the performance of the prototype by comparing simulated and measured results.

Limitations and Assumptions

Following limitations and assumptions has been made in order to keep the scope of the project within the time frame of the project.

- *The components for the setup are assumed to be ideal.*
- *No controller will be designed, hence the converter topology will operate under open loop control.*
- *A simple battery model will be utilized in order to focus on the topology selection and operation.*

Battery Tester 3

This chapter presents the general structure of a traditional battery charger and states the requirements of the test setup needed for the pulse charge and discharge test. Furthermore an analysis is made with respect to choice of topology capable of accommodate the stated requirements.

3.1 General Charger Structure

Figure 3.1 illustrated a general structure of a fast charger, consisting of the grid as a power source, a filter to filter out harmonics, a rectifier/inverter that converts AC into DC and vice versa, a DC-DC converter that regulates the DC voltage to match the voltage of the load a battery/capacitor that gets either discharged or charged. The power flow of such a setup can be bi-directional, meaning that both the grid and load can act as a power source or a load respectively.

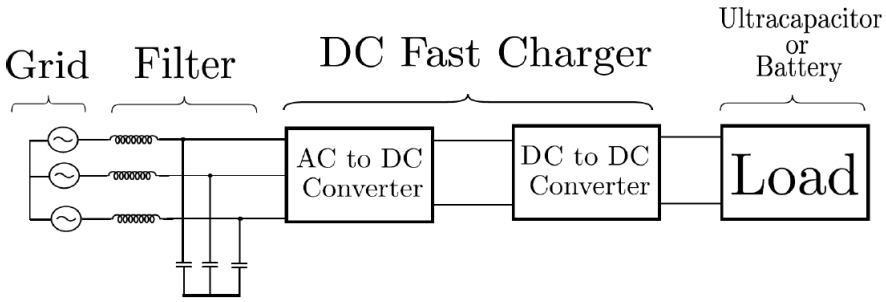


Figure 3.1: Simple block diagram of typical fast charger structure [Channegowda et al., 2015].

3.2 Test Setup Requirements

To be able to design a test setup capable of performing pulse charge and discharge test, it is necessary to state the requirements. Following requirements has been set for the test setup, and is an extended list based on the requirements provided by KK Wind Solutions.

- Capable of delivering ± 200A
- Capable of changing current stress from ± 10A - 200A
- Capable of charging at at $100A/\mu s$ rate
- Capable of discharging at $25A/\mu s$ rate
- Capable of controlling the gradient $\partial i/\partial t$
- Capable of pulse duration of 100μs - 10ms

- Capable of circulating energy between two batteries

The requirements listed above describes the functionality of the test setup, which purpose is to evaluate the reliability of batteries used under pulsed operation. To make the evaluation and test process as efficient and simple as possible, it is essential to be able to perform test in a smart and fast manner without compromising the quality of the test results. Being able to circulate energy by discharging one battery and use it to charge another battery, makes it possible to test two batteries at once, making the test process efficient with respect to both time and energy conservation.

Additional requirement have been made based on current profiles provided by KK Wind solutions, with respect to the shape of the current pulses. Figure 3.2 illustrates the shape of the current pulses, which can be described as symmetrical pulses of different magnitude, where the magnitude is determined by a 100 Hz rectified sinusoidal envelope with a magnitude of 200A. The converter used for the test setup should therefore be able to modulate such a current pulse pattern.

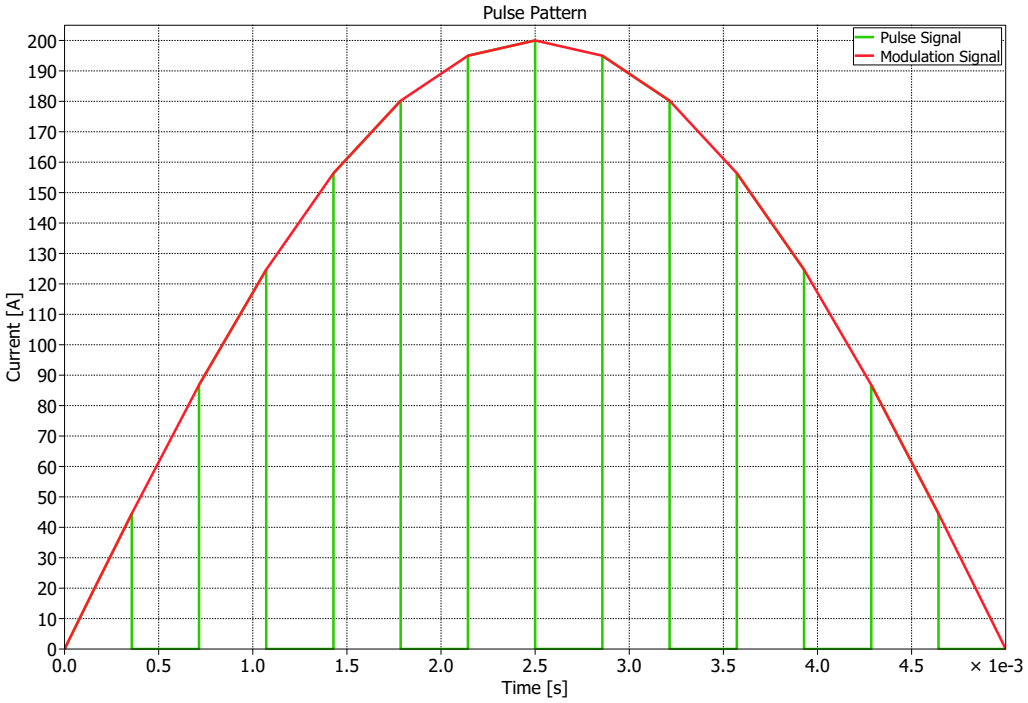


Figure 3.2: Desired pulse pattern for battery charge and discharge current.

3.3 Bi-Directional Buck-Boost Converter

It has been stated that it is of interest to develop a system capable of circulating power between two batteries, as it would allow the user to test two batteries at once, hence reducing the time spend on testing.

Drawing inspiration from Figure3.1 and keeping in mind that batteries only operates in the direct current (DC) environment and not the alternate current (AC), a test setup could

be made out of a four switch bi-directional buck-boost topology, as illustrated in Figure 3.3 [S.R and Rasu, 2015].

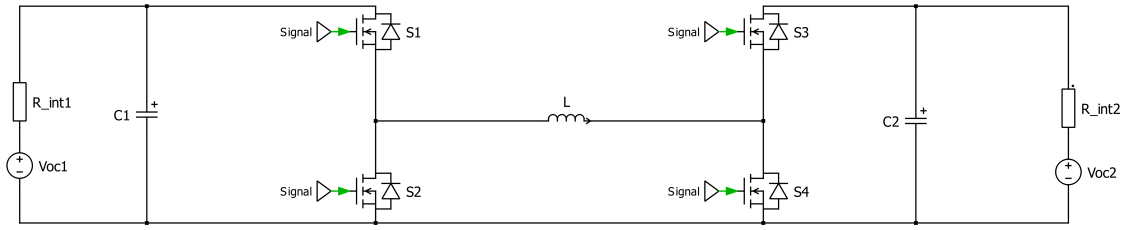


Figure 3.3: 4-switch bi-directional buck-boost converter schematic.

The benefit of of using the batteries, both as a load and a source has the major advantage of keeping the whole test setup out of the AC environment. This simplifies the test setup since no AC/DC converter is needed.

From the schematic, illustrated in Figure 3.3, it can be seen that only 4 switches is needed to make the system work. The following table shows the different operation modes of the converter and the switch signal needed to operate at a specific mode.

3.3.1 Operating Mode

Table 3.1 states 2 different operating modes of the bi-directional buck-boost converter and the corresponding switch signals, where D is the duty cycle, also known as the time of which the switch is on during one switching period, as illustrated in Figure 3.4

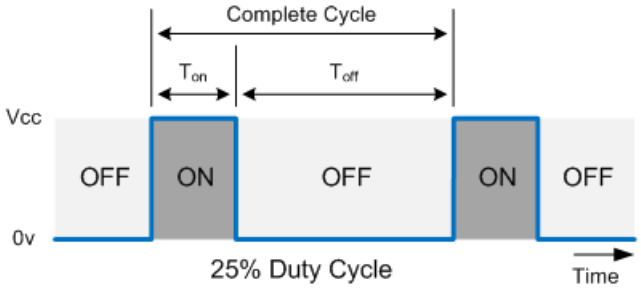


Figure 3.4: Graphical representation of duty cycle [AspenCore, 2019].

Operation Mode	**S1**	**S2**	**S3**	**S4**
Buck	D	1-D	ON	OFF
Boost	ON	OFF	1-D	D

Table 3.1: Switch operation of the four switch bi-directional buck-boost converter.

The duty cycle for each operating mode can be found using Equation 3.1 and 3.2 respectively [Instruments, 2019c].

$$D_{buck} = \frac{V_{out}}{V_{in}} \tag{3.1}$$

$$D_{boost} = 1 - \frac{V_{in}}{V_{out}} \tag{3.2}$$

3.3.2 Electrical Battery Model

In order to evaluate the electrical performance of the battery it is necessary to make an electrical model representing the characteristics of the battery. Several different models exist and varies in complexity depending on the desired accuracy. Since the goal of this project is to develop a test setup with the capabilities of pulse charging and discharging batteries, it is desired to utilize a simple model representation of the battery. A brief overview of different battery models, and its purposes, will be presented throughout this section.

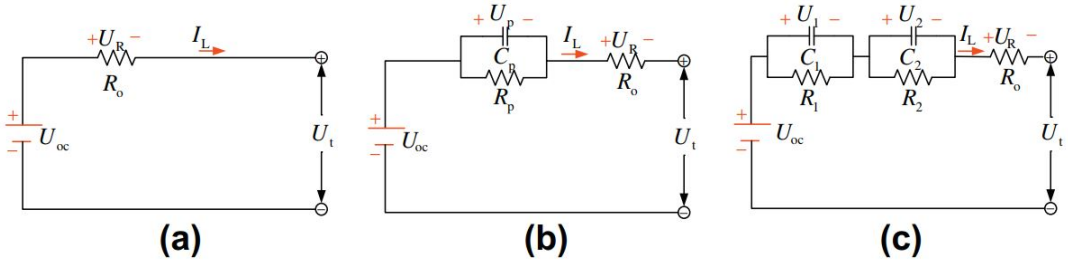


Figure 3.5: Schematic diagram representations of three different battery circuit models. (a) The *Rint* Model,(b) The *Thevenin* Model,(c) The *RD* Model [He et al., 2012].

Figure 3.5 shows three of the most common battery circuit models, where an extra layer of complexity is added to the previous model, starting from left going right.

The Rint Model is the most simple model and is represented by a open circuit DC voltage (U_{oc}) and an internal series resistance (R_0). The model does not include any time depended circuit components such as inductors or capacitors and can only be used to analyse the static response of the battery. The OCV (U_{oc}) can be obtained from the data sheet of the battery, described by a fixed nominal value, or estimated using the discharge curve, as will be explained later. The series resistance (R_0) can also be obtained from the data sheet of the battery.

The Thevenin Model adds a parallel RC network in series with the Rint Model, which makes this model suitable to analyse the dynamic response of the battery. Adding a RC network increases the complexity of the model as the parameters of the network can not be identified using the data sheet of the battery. To obtain values for the parameters of the RC circuit, it is necessary to perform either offline or online parameter identification which utilized mathematical models and methods to estimate the unknown parameters of the model[He et al., 2012].

The main difference between offline and online parameter identification is that the offline method utilizes and process data that has already been collected, whereas the online method utilizes and process data obtained during operation, making the parameter estimation time depended. That is why the offline method is considered less accurate compared to the online method, as the parameters can be affected by external and internal factors, such as temperature [Rahimi-Eichi et al., 2014].

The last of the three model represented in Figure 3.5 is the FD model. This models adds and additional parallel RC circuit to the Rint model, which means that two separate RC networks are added in series with the internal resistance (R_0). The purpose of the additional RC network is to increase the accuracy of the model, as it is possible to split and describe the parameters/mechanisms of the battery into individual parts, resulting in a more accurate behavioral representation. However, introducing another RC network, also increases the complexity of the model[He et al., 2012].

Since it is not part of the scope of this project to investigate the dynamic behavior of the battery and perform parameter identification, the Rint model has been chosen due to its simplicity and the benefit of having the parameters needed for the model, listed in Appendix A. Table 3.2 lists the parameters needed for the Rint model.

Parameter	Value
V_{oc}	3.19 [V]
R_{int}	0.7± 0.1 [mΩ]

Table 3.2: Battery parameters used for the Rint model.

3.3.3 Open Circuit Voltage and State of Charge Estimation

As stated previously, the OCV of the battery (V_{oc}) can be obtained from the data sheet directly as a constant value, but can also be calculated based on the discharge curve of the batteries used for this project, illustrated in Figure 3.6.

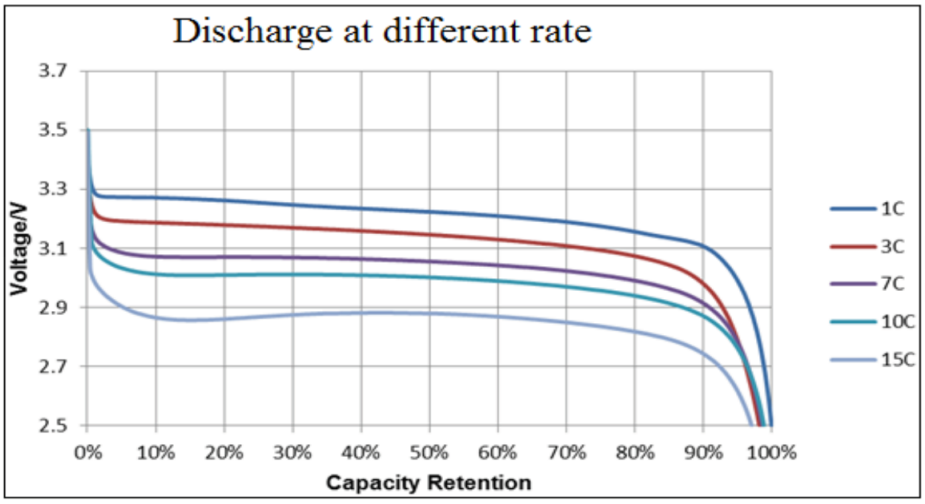


Figure 3.6: Discharge curve of battery cell at different discharge rates and temperature of 25°C taken from Appendix A.

It can be seen that the battery OCV drops accordingly with the SoC, and that the discharge rate (C) has a significant impact on the average voltage during the discharge period. The nominal discharge rate, represented by 1C, is typically reflected by the battery capacity and is defined as the rate of which the battery is discharged within a time period of one hour. The capacity of the battery cell associated with the discharge characteristics represented in Figure 3.6 is 20Ah, hence the magnitude of the discharge current when discharging at

1C rate is equal to 20A. Based on the characteristics of the discharge curve the cell voltage ,during charge and discharge, can be used to determine the state of charge. It should be noted, that the relation between (V_{oc}) and SoC also depends heavily upon temperature, as stated in Chapter 1. The temperature of the batteries at all time is therefore assumed so be at constant room temperature of 25°C

Using an online tool called *'WebPlotDigitizer'* that makes it possible to extract data points from a PDF and importing that data set into matlab, the following equation has been estimated using the curve fitting tool.

$$\begin{aligned} V_{oc} = 0.3505 \cdot SoC^9 + 0.3257 \cdot SoC^8 - 0.7756 \cdot SoC^7 - 0.7048 \cdot SoC^6 \\ +0.5728 \cdot SoC^5 + 0.4571 \cdot SoC^4 - 0.1418 \cdot SoC^3 - 0.1254 \cdot Soc^2 \\ +0.0471 \cdot SoC + 3.063 \end{aligned} \tag{3.3}$$

Equation 3.3 is based on a 9_{th} degree polynomial function, as it gave the best fit possible.

The definition of a n_{th} degree polynomial is stated by Equation 3.4

$$Pn = a_n \cdot x^n + a_{n-1} \cdot x^{n-1} + .. + a_2 \cdot x^2 + a \cdot x + a_0 \tag{3.4}$$

Plotting Equation 3.3, illustrated in Figure 3.7, it can be seen that the curve fitting tool manage to find a relative good fit across the entire range, except when the battery reaches a 93-100% SoC. Operating the batteries within this range would make it difficult to know the exact state of charge, which would cause possible errors with respect to test result analysis, as the operating point would differ from what would be expected, making it difficult to compare test results, hence it should be avoided.

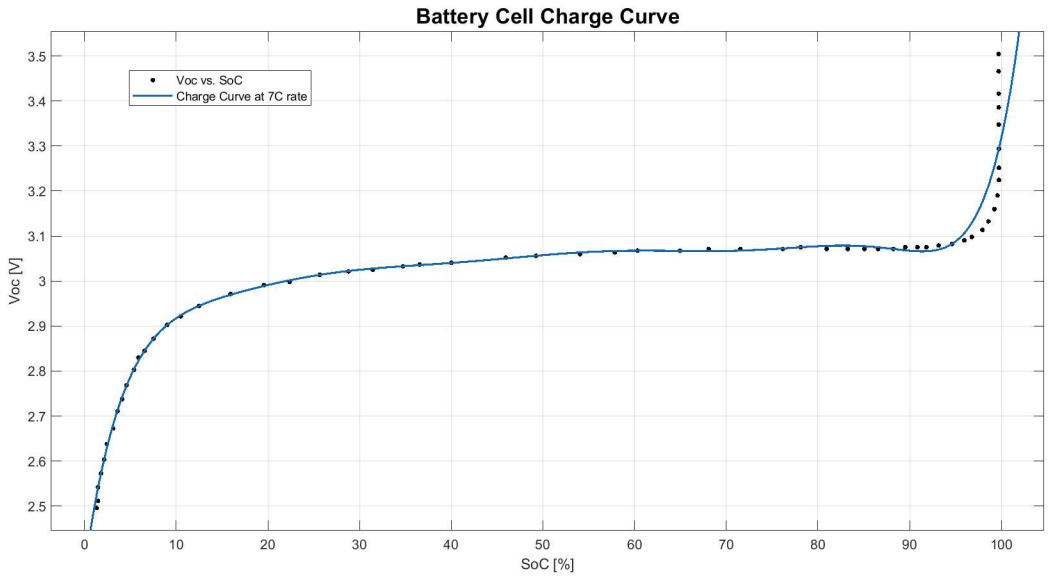


Figure 3.7: Charge curve of battery cell, based on extracted data point from Figure 3.6 and estimated using Matlab Curve Fitting Tool.

As mentioned earlier the OCV is significantly affected by the magnitude of the current and temperature, which makes it even more difficult to estimate the SoC. Using a lookup table containing the (V_{oc}) vs. temperature could be made to resolve this problem, but would depend on accurate temperature measurement.

A better way of keeping track of the SoC of the battery cell, would be to perform simple coulomb counting starting from a battery cell voltage below the 93% SoC, described by Equation 3.3 [Ng et al., 2009].

A coulomb is a SI-unit describing the electrical charge and is defines as the amount of charge delivered by 1 amp during a time period of 1 second. Performing coulomb counting therefore simply means to integrate the current going in and out of the battery and add it to the initial value of charge, as stated by Equation 3.5.

$$Q = \int_{t0}^{t} \cdot I_{batt} + Q_0 \tag{3.5}$$

Knowing the charge Q, it is possible to obtain the SoC if the nominal charge (Q_{nom}) is know, as stated by Equation 3.6.

$$SoC = \frac{\int_{t0}^{t} \cdot I + Q_0}{Q_{nom}} \cdot 100\% \tag{3.6}$$

The disadvantage of this method is that it suffers from drifting, as it depends on 100% correct current measurements, which would result in an offset when operating over longer periods of time. It should therefore be reset, by measuring the voltage prior to test start.

The operating modes of the bi-directional buck-boost converter was stated in Table 3.1, along with the corresponding duty cycle definition of each mode stated by Equation 3.1 and 3.2. From equation 3.2 it can be seen that the output voltage has to be higher than the input voltage, in order to operate in boost mode. From Figure 3.7 it can be seen that the open circuit voltage of the battery has an almost constant value in the range of 20-90% SoC. Utilizing two batteries in the test setup to act, both has a load and a source, means that the input and output voltage would be almost identically, assuming that the batteries are not charged or discharged outside the 20-90% SoC range. However, in order to charge a battery it is necessary to charge at a higher voltage than the (V_{oc}). The maximum charge voltage can be found in Appendix A and is rated at 3.75V. This means that the converter would always operate in boost mode.

3.3.4 Converter Parameters

Based on the OCV characteristics, it has been stated that the converter will only be operated in boost mode. In order to evaluate whether or not the performance of the bi-directional buck-boost converter is suitable for the test setup, it is necessary to estimate the converter parameters.

First step is to calculate the duty cycle using Equation 3.11, which utilized the maximum input voltage in order to determine the minimum duty cycle. Since the batteries has an internal resistance, it can be difficult to define the exact input and output voltage of the converter, as these values changes depending on the current going in and out of the battery.

However, assuming a 100% efficiency of the converter and defining the maximum current going out of the battery acting a a source to be 200A, it is possible to estimate both the input and output voltages, using the following set of equations.

The power balance of a boost converter is given by Equation 3.7, stating that the output power of the converter is always equal or less than the input power, depending on the amount of losses, expressed by the efficiency.

$$P_{in} = \frac{P_{out}}{\eta} \tag{3.7}$$

The input and output voltage can be defined as stated by Equation 3.8 and 3.9, which is derived from the equivalent electrical circuit of the battery, represented by the Rint model, illustrated in Figure 3.5, using kirchhoff's current law (KVL).

$$V_{in} = V_{oc} - R_{int} \cdot I_{in} \tag{3.8}$$

$$V_{out} = V_{oc} + R_{int} \cdot I_{out} \tag{3.9}$$

Applying, both the assumption of 100% converter efficiency and the definition of the input and output voltage stated in Equation 3.8 and 3.9, Equation 3.7 can be written as stated by Equation 3.10.

$$(V_{oc} - R_{int} \cdot I_{in}) \cdot I_{in} = (V_{oc} + R_{int} \cdot I_{out}) \cdot I_{out} \tag{3.10}$$

Solving for (I_{out}) in Equation 3.10, using the definition of the input current of 200A and the battery parameters from Table 3.2, it is possible to estimate the input and output voltages, as stated by Equation 3.8 and 3.9.

The values obtained from Equation 3.8, 3.9 and 3.10 are listed in Table 3.3, where (V_{in}) and (V_{out}) are used in Equation 3.11 to estimate the duty cycle.

Parameter	I_{out}	V_{in}	V_{out}
Value	184 A	3.05 V	3.32 V

Table 3.3: Calculated battery parameters,

$$D_{boost} = 1 - \frac{V_{in} \cdot \eta}{V_{out}} = 1 - \frac{3.045\text{V} \cdot 100\%}{3.32\text{V}} = 8\% \tag{3.11}$$

It can be seen that relative low difference in voltage between the input and output voltage, results in a low duty cycle, which could limit the switching frequency, depending on the turn-on and turn-off time of the transistor.

Next step is to estimate a minimum value of the inductor, using equation 3.12 [Instruments, 2019c]. The inductor value is based on the switching frequency (f_{sw}), the current ripple, given by the coefficient (K_{ind}), representing the amount of current ripple relative to (I_{out}) and the relation between (V_{in}) and (V_{out}). A switching frequency of 100 kHz, along with a (K_{ind}) value of 10% is chosen to minimize current ripple.

$$L \geq \frac{V_{in}^2 \cdot (V_{out} - V_{in})}{f_{sw} \cdot K_{ind} \cdot I_{out} \cdot V_{out}^2} = \frac{3.05\text{V}^2 \cdot (3.32\text{V} - 3.05\text{V})}{100 \cdot 10^3\text{Hz} \cdot 0.1 \cdot 184\text{A} \cdot 3.32\text{V}^2} = 12.4\mu\text{H} \tag{3.12}$$

Finally it is possible to estimate the minimum value of the output capacitor, to limit the output voltage ripple across the battery, using Equation 3.13 [Instruments, 2019c].The amount of voltage ripple relative to the output voltage, represented by the coefficient (K_{cap}), is chosen to be max 0.1% in order to avoid unwanted stress of the battery.

$$C_{out,min} = \frac{I_{out} \cdot D_{boost}}{f_{sw} \cdot V_{out} \cdot K_{cap}} = \frac{184\text{A} \cdot 0.08}{100 \cdot 10^3\text{Hz} \cdot 3.32\text{V} \cdot 0.001} = 4.5\text{mF} \tag{3.13}$$

Equation 3.11, 3.12 and 3.13 are all used to estimate initial values for the components of the converter and can always be tuned based on the simulation results.

Having calculated the parameters of the converter, it is possible to implement Equation 3.3, 3.5 and 3.6 into the model, to simulate the change in OCV during operation.

Figure 3.8 illustrates the change in OCV of the two batteries, where one of the batteries operates as a source and is therefore discharging and the other is acting as a load and is therefore charging correspondingly. It can be seen that the OCV of the discharging battery is dropping and vice versa, when looking at the charging battery, hence indicating that the converter is operating in boost mode.

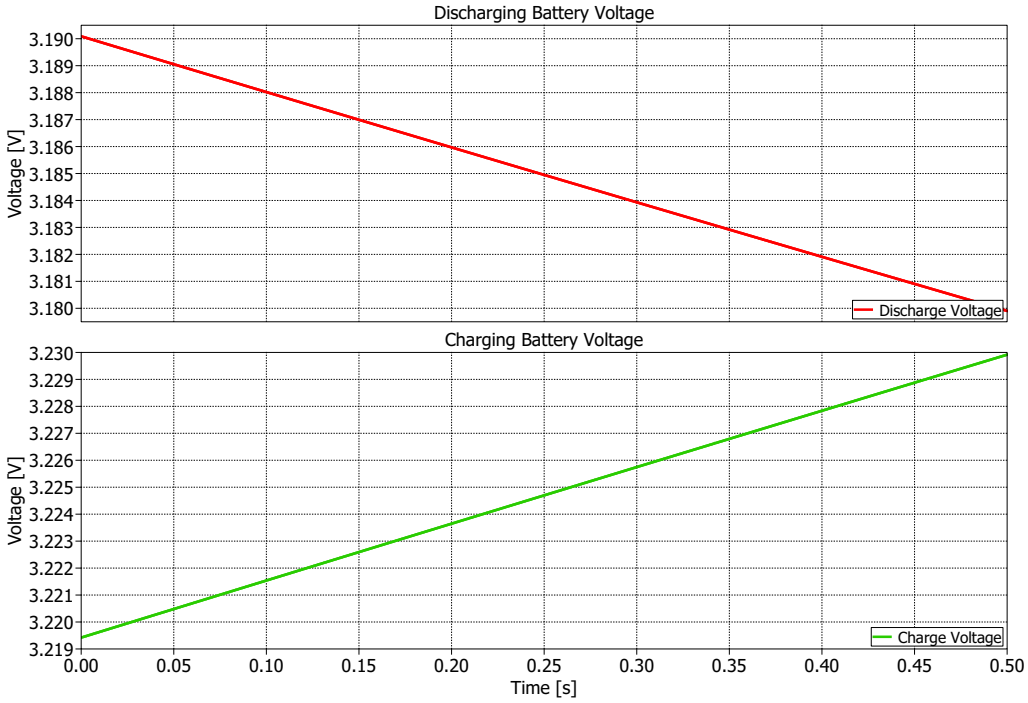


Figure 3.8: Battery voltages during charge and discharge operation at an initial SoC of 87% and 87.5% .

To validate whether or not the bi-directional buck-boost converter is suitable for the test setup, it is necessary to evaluate the current response. Figure 3.9 shows the charging current response of the converter at different converter parameter configuration, with the purpose of illustrating whether or not this topology is suitable for a battery test setup.

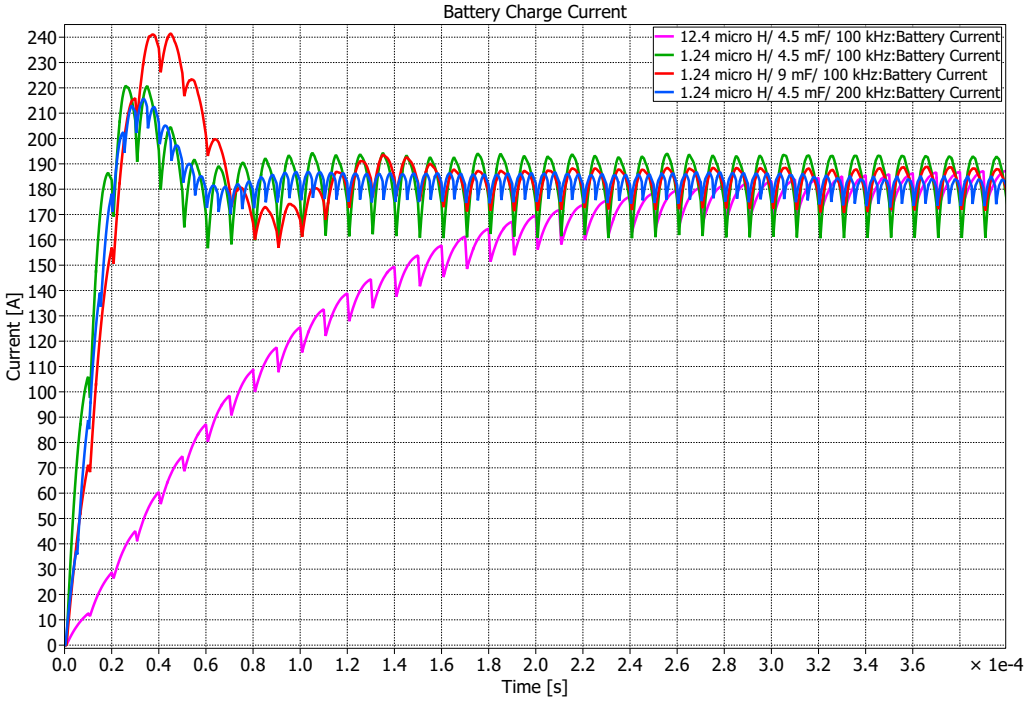


Figure 3.9: Current response at different hardware and switching frequency configurations.

From Figure 3.9 it can be seen that none of the current response curves satisfies the requirement made with respect to a current response of $100A/\mu s$. However, modifications has been made to the initial estimated design, represented by the purple response, in order to improve the response.

First the inductance was reduced by a factor of teen, represented by the green response, which had a positive effect on the response time. However, it also increased the current ripple, as expected, since the inductance describes the relation between the induced voltage and the rate of change of the current.

In order to reduce the voltage ripple across the battery, caused by the increased current ripple, the capacitor was increased by a factor of two, illustrated by the red response. However, this had a negative effect on the current response time, making it slower than before.

Another way of reducing the ripple, instead of increasing the value of the capacitor, would be to increase the switching frequency. The effect of increasing the switching frequency by a factor of two and keeping the original value of the capacitor, is illustrated by the blue response. It can be seen, that increasing the switching frequency, rather than the capacitor value is better with respect to response time. However, as stated earlier, none of the current responses is even near the requirement of a current response of $100A/\mu s$, which is why this topology is not suitable for the battery test setup, when looking at the current response.

3.3.5 Energy Balance

Since it is desired to perform power cycling using two batteries, it would be interesting two estimate the losses during operation, in order to evaluate whether or not it is a good idea to perform test using this configuration.

Transistor Losses

Due to the low operating voltage of the converter and high frequencies operation, it is decided to use mosfets as transistors [Semiconductor, 2019].

Equation 3.14 states the total losses of the mosfets, divided into three sub-categories, namely the conduction losses (P_{cond}), the switching loses (P_{sw}) and the gate losses (P_g) [Instruments, 2019b].

$$P_{fet(total)} = P_{cond} + P_{sw} + P_g \tag{3.14}$$

The conduction losses can be estimated using Equation 3.15, which represents the losses accruing when the transistor is turned on, hence conducting.

$$P_{cond} = R_{ds_{on}} \cdot I^2_{sw_{rms}} = 0.72\text{m}\Omega \cdot 200\text{A}^2 = 28.80\text{W} \tag{3.15}$$

From Table 3.1 it can be seen that three out of four switching are conducting during boost mode operation. Two of the switches conduct complimentary, which means that the total conduction loss is equal to that of two mosfets conducting continuously, hence 57.60W.

Next step is to estimate the switching losses using Equation 3.16, which represents the losses caused by the time it takes to charge and discharge the mosfet.

$$P_{sw} = V_{in} \cdot I_{out} \cdot f_{sw} \cdot \frac{Q_{gs} + Q_{gd}}{I_g} \tag{3.16}$$

Re-writing Equation 3.16, the switching losses can be estimated using the turn-on delay time ($t_{d(on)}$), turn-off delay time ($t_{d(off)}$), rise time (t_r) and fall time (t_f), obtained form the data sheet of the mosfet [Semiconductor, 2019], using Equation 3.17.

$$P_{sw} = V_{in} \cdot I_{out} \cdot f_{sw} \cdot ((t_{d(on)} + t_r) + (t_{d(off)} + t_f)) \tag{3.17}$$

$$P_{sw} = 3.05\text{V} \cdot 200\text{A} \cdot 100 \cdot 10^3\text{Hz} \cdot ((21\text{ns} + 42\text{ns}) + (288\text{ns} + 101\text{ns})) = 27.57\text{W}$$

The switching losses only apply to the switches that are switching on an off during one switching period an does therefore only apply for two of the 3 switches being used, hence a total switching loss of 54.14W.

The final step is to calculate the losses of the gate driver circuit itself, using Equation 3.18 and the values of the maximum total gate charge ($Q_{total,max}$) and gate voltage (V_g).

$$P_g = Q_{g(total)} \cdot V_g \cdot f_{sw} = 203\text{nC} \cdot 10\text{V} \cdot 100 \cdot 10^3\text{Hz} = 0.20\text{W} \tag{3.18}$$

The magnitude of the gate driver losses are insignificant, compared to the conduction and switching losses, but is a loss that is applied across all three transistors as they are all operated, hence a total gate driver loss of 0.60W.

Adding the individual transistor losses, results in the following total transistor loss.

$$P_{fet(total)} = 57.60\text{W}+54.14\text{W}+0.60\text{W}=112.34\text{W}$$

Battery losses

Besides the transistor losses, the batteries also experience losses due to the internal resistance, which can be estimated using Equation 3.19

$$P_{batt} = R_{int} \cdot I_{rms}^2 \tag{3.19}$$

$$P_{batt,(source)} = 0.7\text{m}\Omega \cdot 200\text{A}^2 = 28.0\text{W}$$

$$P_{batt,(load)} = 0.7\text{m}\Omega \cdot 184\text{A}^2 = 23.7\text{W}$$

Adding both the transistor losses and the battery losses, results in the following total estimated loss.

$$P_{loss,total} = P_{fet,(total)} + P_{batt,(source)} + P_{batt,(load)} \tag{3.20}$$

$$P_{loss,total} = 112.34\text{W} + 28.0\text{W} + 23.7\,W = 164.04\text{W}$$

Using Equation 3.21, the efficiency of the test setup can be estimated.

$$\eta = \frac{P_{in} - P_{loss,total}}{P_{in}} \cdot 100\% \tag{3.21}$$

$$\eta = \frac{(3.19\text{V} \cdot 200\text{A}) - 164.04\text{W}}{(3.19\text{V} \cdot 200\text{A})} \cdot 100\% = 74.29\%$$

This means that approximately 25% of the energy is lost during operation, which limits the time duration of the test. Knowing the losses and the battery capacity, it is possible to estimate how long it takes to discharge both batteries completely due to losses, using Equation 3.22.

$$t_{test} = \frac{E_{cap,batt}}{P_{loss,total}} \tag{3.22}$$

$$t_{test} = \frac{3.19\text{V} \cdot 20\text{Ah}}{164.04\text{W}} \approx 23\text{min}$$

It can be seen that it only takes approximately 23 min to fully discharge both batteries, assuming 100% SoC at the start of the test. Increasing the time period of the test cycle can be done by supplying the losses through an external power supply or by adding multiple mosfets in parallel to decrease conduction losses. However, adding more mosfets does not affect the switching losses, which stays the same since switching frequency and current are linearly dependent as stated by Equation 3.17, hence limiting the maximum achievable efficiency.

Since losses are inevitable, due to switching and internal resistance of the battery, it would be interesting to supply the losses externally in order to have the opportunity to cycle the batteries at at fixed SoC.

3.4 Modulation Technique

One of the requirements for the test setup was to have the capability to output current pulse patterns, resembling the one represented in Figure3.2. This section will present the modulation technique implemented in order to achieve such pulse pattern.

Figure 3.10 illustrates a graphical representation of the signal modulation strategy, implemented in the bi-directional buck-boost converter topology, with the goal of replicating the pulse pattern presented in Figure 3.2.

The modulation strategy can be divided into two parts. The first part is represented by the top graph in Figure 3.10, where a modulation signal (rectified 100 Hz sinusoidal signal) compared with a high frequency carrier signal (triangular signal), which creates a Pulse Width Modulation (PWM) signal in the middle of Figure 3.10. However, feeding this PWM signal to the switches, would create a rectified sinusoidal current through the battery. In order to create the desired pulses an additional PWM signal is introduced, which runs at a lower frequency of the one already created. The additional PWM signal is set to run at a fixed duty cycle of 50% and is used to chop the high frequency PWM signal, which results in the symmetrical PWM signal illustrated in the bottom graph in Figure 3.10. The number of pulses can be increased or decreased by increasing or lowering the switching frequency of the low frequency PWM signal used to chop.

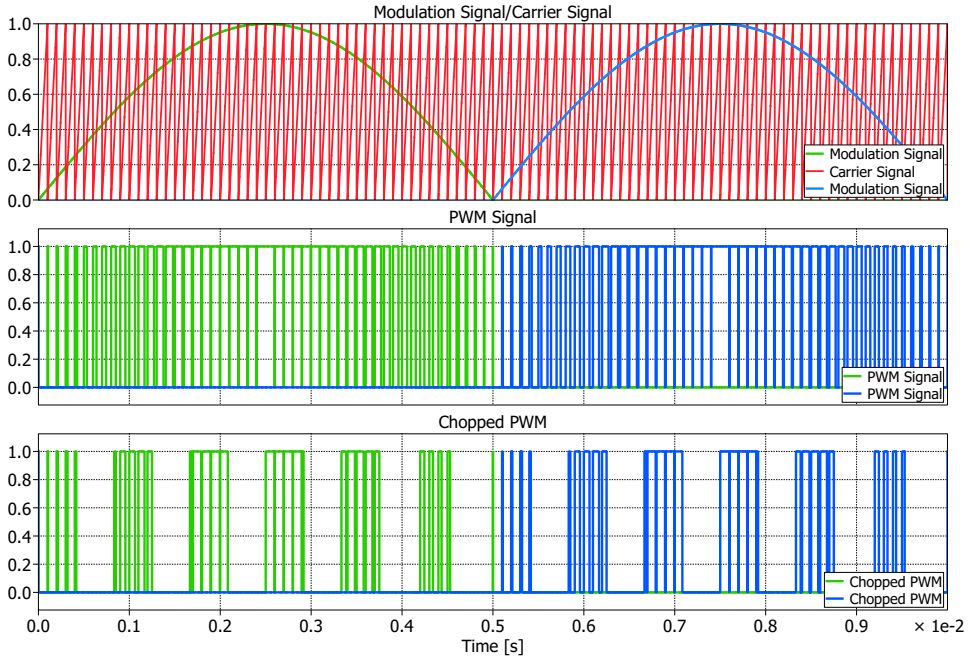


Figure 3.10: Graphical representation of the signal modulation strategy used for the bi-directional buck-boost converter.

Figure 3.11 shows the modulated current output response of the bi-directional buck-boost converter obtained using the signal modulation strategy explained earlier and illustrated in Figure 3.10.

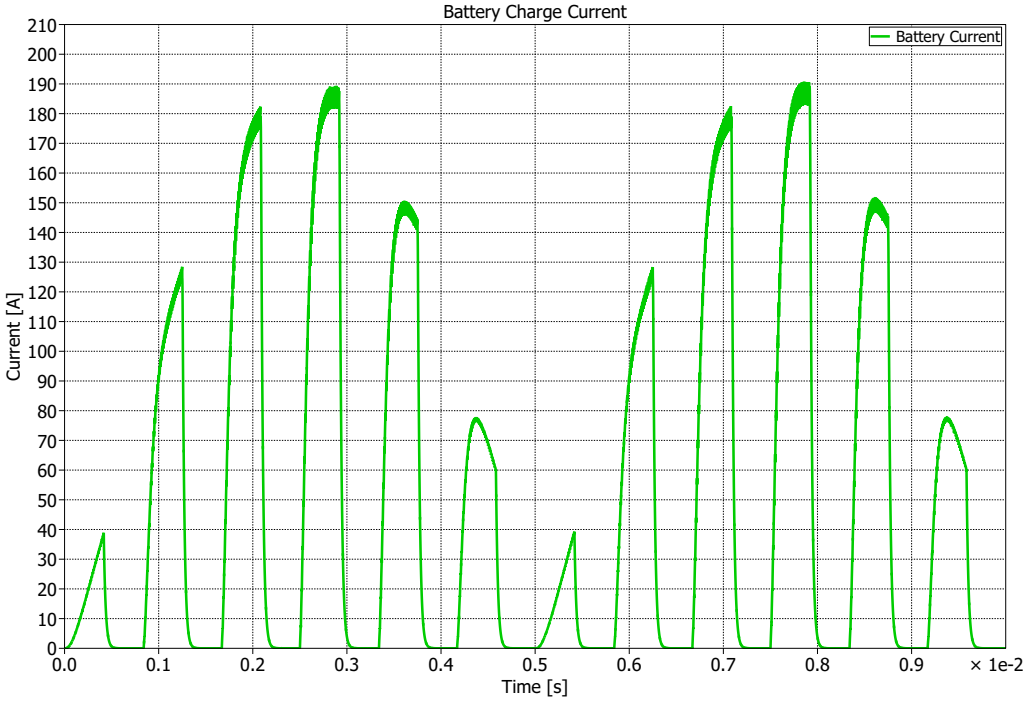


Figure 3.11: Current pulse pattern.

It can be seen that the bi-directional buck-boost converter topology is capable of generating a current pulse pattern, resembling the one specified in the specification and illustrated in Figure 3.2. However, it still underperforms with respect to the time response, as was also stated by Figure 3.9. It should be noted, that a better representation of the pulse pattern would be possible to achieve through fine tuning of the converter parameters.

3.4.1 Discussion and Conclusion

Evaluating the performance of the bi-directional buck-boost converter with respect to the requirements made in Section 3.2, it was discovered that the topology was able to be configured, such that the batteries would be able to power cycle the energy from one battery to another. Furthermore, it was possible to modulate the control signals of the transistors, such that a current pulse pattern of the converter, resembled the one presented in Figure 3.2. A schematic representation of the PLECS model can be found in Appendix B.

However, two limitations were discovered, one of them being a slow time response, which could not be resolved as it would result in high ripples, that would cause undesirable stress to the battery, as it is only desired to stress the batteries through controlled charge and discharge pulses.

The other limitation was encountered when estimating the losses during operation of the converter. It was discovered that approximately 25% of the energy would be lost through conduction and switching losses, thereby loosing the benefit of power cycling, as an external

power source would be needed to operate the test setup, not only for a longer period of time, but also at a fixed SoC. However, adding an external power supply would resolve this issues, hence making the slow current response the only limitation.

Being aware of these limitation, it is decided to look at other topologies capable of resolving the limitations encountered with the bi-directional buck-boost converter.

3.5 Hybrid H-Bridge Converter

This section introduces a hybrid h-bridge converter topology, which is proposed as a suitable configuration for the battery test setup, based on the limitations encountered through the analysis of the bi-directional buck-boost converter, presented in Section 3.3.

Figure 3.12, illustrates a schematic representation of the proposed configuration. It can be seen that the topology consist of a full bridge single phase inverter module and two additional h-bridge modules, each containing one battery, represented by the Rint model. Furthermore, a DC power supply has been added to compensate for losses during operation and to act as a source, used to generate the sinusoidal current, representing the envelope containing the current pulses, illustrated in Figure 3.2.

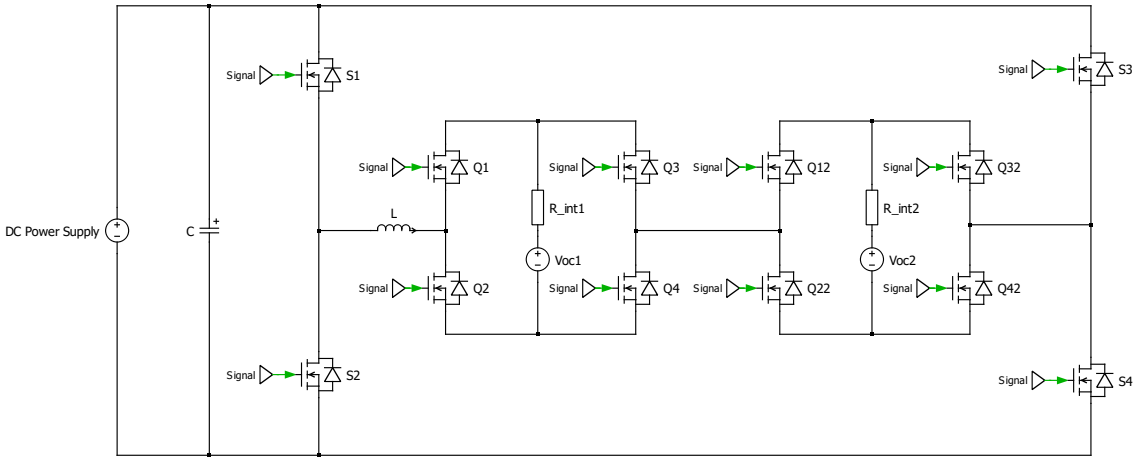


Figure 3.12: Schematic representation of Hybrid H-Bridge converter.

Based on experience from the previous topology, it could be seen that it was possible to generate the desired pulse pattern, using the proposed modulation technique. However, it was also concluded that the response time did not meet the requirement, as it would result in high ripple that would stress the batteries in an unwanted way. The slow response time was caused by the passive components used to smooth the high frequency signal generated by the active components.

Having only four switches available had the benefit of simplicity with respect to control, but also a limitations with respect to modulation, since the same switches had to perform both high frequency signal generation and low frequency signal chopping, causing the inductor current to fall to zero, hence resulting in a slow response. Introducing additional switches to the test setup would have the downside of increasing complexity, but could resolve the problem related to the slow response time, by distributing the modulation signals out on

several switches and implementing intelligent current control, to prevent the test setup from running in discontinuous conduction mode (DCM).

3.5.1 Single Phase Inverter

The purpose of the single phase inverter is to create a sinusoidal current at a desired amplitude and frequency, which represent the envelope, shaping the current pulse pattern illustrated in Figure 3.2. Table 3.4 shows the switch operations of the inverter, indicating a diagonal and complimentary switch operation of two switch pairs, in order to generate a sinusoidal current, oscillating around a baseline equal to zero.

Operation Mode	**S1**	**S2**	**S3**	**S4**
Positive Sine Wave	ON	OFF	OFF	ON
Negative Sine Wave	OFF	ON	ON	OFF

Table 3.4: Switch operation of inverter.

Modulation Technique

The Sinusoidal Pulse Width Modulation (SPWM) technique is utilized to generate the control signals necessary for the single phase inverter. This modulation technique is similar to the one used for the bi-directional buck-boost converter, where a modulation signal at fundamental frequency is compared with a high frequency carrier signal, used to sample an generate a PWM signal with varying duty cycle, as illustrated in Figure 3.13

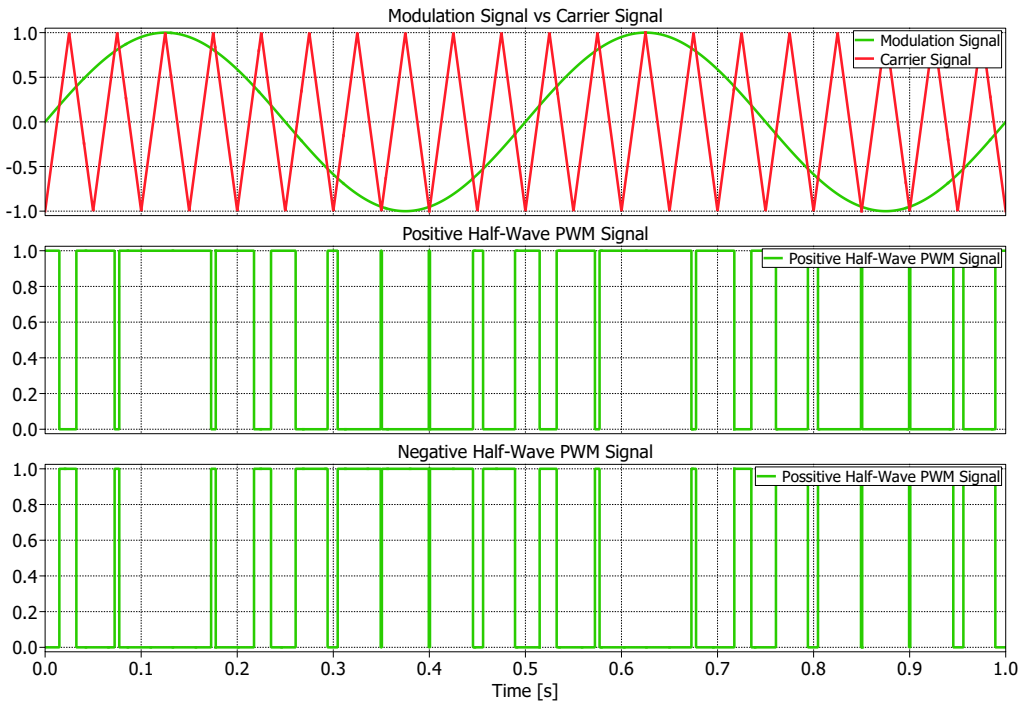


Figure 3.13: Graphical illustration of the SPWM technique.

Applying the positive half-wave PWM signal to switch S1 and S4 and the negative half-wave PWM signal to switch S2 and S3, would create a sinusoidal current through the inductor.

3.5.2 H-Bridge

The purpose of the h-bridge module containing a battery module is numerous and varies depending on mode of operation, which is to either charge, discharge or bypass the battery within the module. However, the main purpose is to chop the current generated by the inverter module, through high frequency PWM switching, at a relative lower switching frequency, to generate charging or discharging current pulses.

In order to be able to operate in any of the three modes of operation, it is necessary to create a control scheme for each mode, that takes into account, both the changing polarity of the sinusoidal current and the requirement of creating a pulse pattern, resembling the one illustrated in Figure 3.2.

Modulation Technique

The modulation technique utilized to create the pulse pattern of interest, is a to use a PWM signal that runs at a fixed duty cycle of 50% ,to create symmetrical pulses, and at a lower frequency of the one used for the carrier signal of the inverter, to chop the sinusoidal current. The Inductor current is measured and utilized as a control signal for the switches to deal with changing polarity of the current, thereby ensuring correct operation conditions at any given operation mode. Table 3.5 illustrates the switch operation during charging and bypass mode, of the h-bridge module containing switch Q1 - Q4.

Operation Mode	**Q1**	**Q2**	**Q3**	**Q4**
Charging $I_L > 0$	ON	OFF	OFF	ON
Bypass $I_L > 0$	ON	OFF	ON	OFF
Charging $I_L < 0$	OFF	ON	ON	OFF
Bypass $I_L < 0$	OFF	ON	OFF	ON

Table 3.5: Switch operation during charging.

The switching signals necessary to operate in charging mode is illustrated in Table 3.6 and 3.7 respectively, depending on the polarity of the inductor current (I_L).

Switch Pulse Signal	**Q1**	**Q2**	**Q3**	**Q4**
1.0 Duty	X			
0 Duty		X		
0.5 Duty				X
0.5 Duty + Delay			X	

Table 3.6: Switch pulse signal during charging at $I_L > 0$.

Switch Pulse Signal	**Q1**	**Q2**	**Q3**	**Q4**
1.0 Duty		X		
0 Duty	X			
0.5 Duty			X	
0.5 Duty + Delay				X

Table 3.7: Switch Pulse signal during charging at $I_L < 0$.

It is important to notice the delay added to one of the 50% duty cycle signals, which is important as this is the signal that allows current to bypass the battery, as it is only of interest to charge the battery using a chopped sinusoidal current and not a fully sinusoidal current. The delay is defined as stated by Equation 3.23, when applying a chopping signal of 50% duty cycle.

$$t_{delay} = \frac{1}{2 \cdot f_{sw}} \tag{3.23}$$

Table 3.8 illustrates the switch operation during discharging and bypass mode, of the h-bridge module containing switch Q12 - Q42.

Operation Mode	**Q1**	**Q2**	**Q3**	**Q4**
Discharging $I_L > 0$	OFF	ON	ON	OFF
Bypass $I_L > 0$	OFF	ON	OFF	ON
Discharging $I_L < 0$	ON	OFF	OFF	ON
Bypass $I_L < 0$	ON	OFF	ON	OFF

Table 3.8: Switch Operation during discharge.

Table 3.9 and 3.10 illustrates the switching signal necessary to operate in discharge mode. Comparing with the signals in Table 3.6 and 3.7, it can be seen that the exact same signals are applied to the switches, with the only difference being the period of which they are applied, as indicated by the polarity of (I_L).

Switch Pulse Signal	**Q1**	**Q2**	**Q3**	**Q4**
1.0 Duty		X		
0 Duty	X			
0.5 Duty			X	
0.5 Duty + Delay				X

Table 3.9: Switch pulse signal during discharge at $I_L > 0$.

Switch Pulse Signal	**Q1**	**Q2**	**Q3**	**Q4**
1.0 Duty	X			
0 Duty		X		
0.5 Duty				X
0.5 Duty + Delay			X	

Table 3.10: Switch pulse signal during discharge at $I_L < 0$.

Table 3.11 shows the switching pattern, necessary to fully bypass a battery module, independent of the polarity of (I_L).

Switch Pulse Signal	**Q1**	**Q2**	**Q3**	**Q4**
1.0 Duty	X			X
0 Duty		X	X	

Table 3.11: Switch pulse signal during full bypass

All of the tables use the leftmost h-bridge module illustrated in Figure 3.12 as a reference, but the exact same signals can be applied to additional h-bridge modules, simply by following the structure of the reference module containing switch Q1 - Q4.

3.6 Model Implementation

Figure 3.14 shows the current response of the inductor and the batteries, where one battery is operated in charging mode and the other in discharging mode, using the control strategy stated in Section 3.5.1 and 3.5.2.

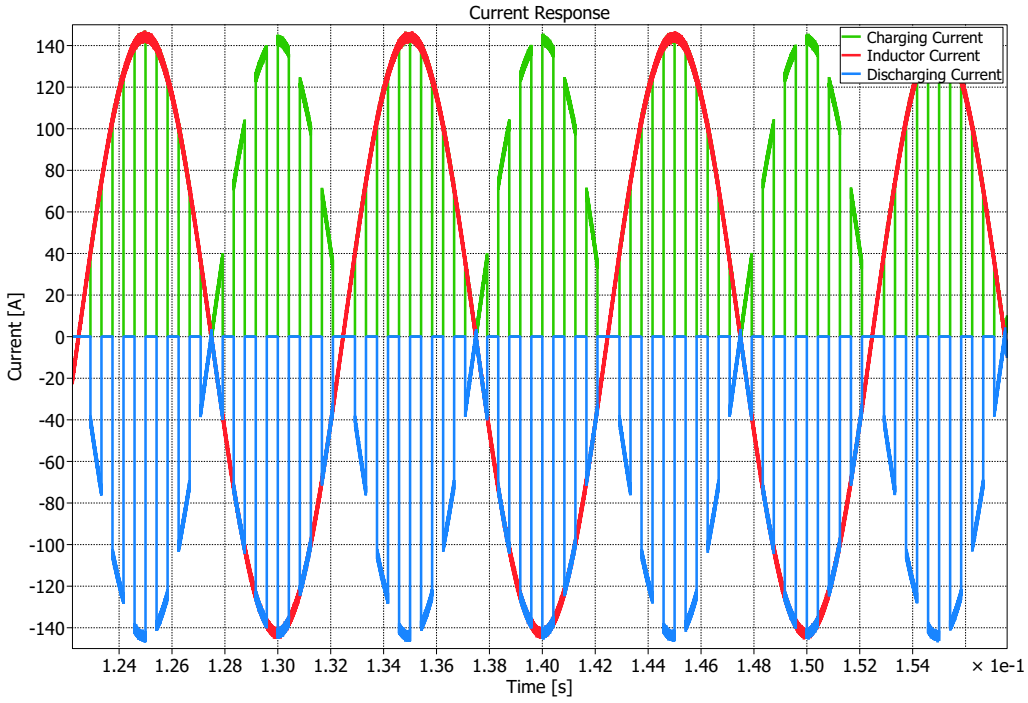


Figure 3.14: Current response of Hybrid H-Bridge using SPWM and PWM chopping.

It can be seen that the topology is able to generate both a sinusoidal current and charge and discharge current patterns, resembling the one illustrated in Figure 3.2.

Figure 3.15 represent a full section of the pulse pattern used to charge the battery. Evaluating the response it can be seen that implementing additional switches has resolved

the issue, with respect to slow response time. However, it should be noted that the current response is ideal, since ideal components are used, hence the limitation of the current response is the turn-on and turn-off time of the mosfets implemented in the h-bridge modules containing the battery modules.

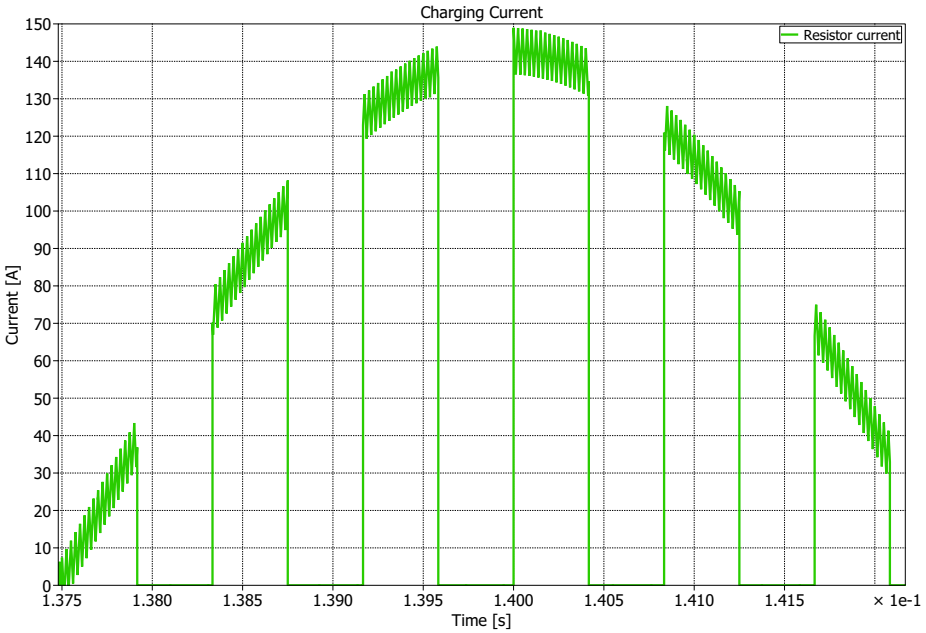


Figure 3.15: Ideal charging current response.

3.6.1 Discussion and Conclusion

Evaluating the performance of the hybrid h-bridge topology, it can be seen that implementing additional switches along with intelligent current control has made a faster response time achievable, compared to the previous topology. Furthermore, it has been possible to keep the ability to generate the desired pulse pattern and at the same time implemented an external power supply, that can be used to compensate for losses during operation. A schematic representation of the PLECS model can be found in Appendix C.

Being able to compensate for losses gives the opportunity to test the batteries for a longer period of time and at a desired SoC, as stated earlier. The combination of series connected batteries with individual h-bridge modules and intelligent current control, gives the opportunity to add several batteries to the system, which in theory, should only be limited by the power output of the DC power supply, with respect to losses. The only disadvantage of this topology, compared to the previous one, is the increased complexity associated with the increased number of switches, introduced by the h-bridge modules containing the batteries.

Based on the performance of the hybrid h-bridge converter and its capability to resolve the problems encountered with the bi-directional buck-boost converter, it is decided to proceed with the hybrid h-bridge topology and build a physical test setup, to validate its performance.

Testing 4

This chapter will present the steps involved when building the test setup based on the topology discussed in Section 3.5. Since the topology consist of multiple sections that are controlled individual, it is intended build and test each section of the setup individually, before joining the sections that makes the full setup. Applying such a systematically approach, increases safety and decreases time spend on debugging, hence making the test process more efficient.

Due to the limited time frame of this project, it is not possible to design and build the test setup from scratch, hence the best solution is to use existing component to establish a proof of concept. Utilizing existing components for the test setup has the benefit of eliminating time spend on design and construction, but has the disadvantage of increasing limitations, since the components are not designed specifically for the test setup, hence compromises must be made to accommodate the ratings and characteristics of the components available.

The purpose of the test setup is therefore to verify whether or not this topology is capable of generating the desired charge/discharge pulse pattern profile, illustrated in Figure 3.2.

4.1 Test Setup Layout

Figure 4.1 illustrates a schematic representation of the main test setup circuitry and the corresponding sub circuits, including characteristics.

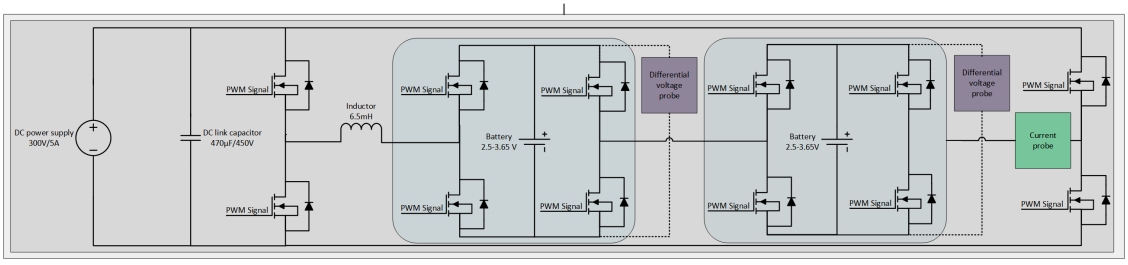


Figure 4.1: Schematic representation of main test setup.

From the schematic it can be seen that the main circuitry is divided into four circuits illustrated by 3 different colors used to distinguish the type and purpose of each circuit. A brief functional description of each circuit is given below.

Light blue: Represents two identical h-bridge modules, each containing one batter cell, and serves the purpose of controlling the current going in, out or bypassing the battery, using intelligent current control.

Dark grey: Represents a h-bridge module with similar characteristics as those used to control the current across the battery. This h-bridge is used as a full bridge single phase inverter, and serves the purpose of generating a sinusoidal current, used to shape the current pulses going into the battery, hence it contains a DC power supply, a DC link capacitor and an inductor instead of a battery.

Green: Represents the current probe used to measure the inductor current.

Purple: Represents the differential voltage probes used to measure the voltage across each battery cell.

Light grey: Represents the entire main circuitry used to generate and control the current used to stress the batteries.

The main circuit contains the necessary active an passive components needed to generate and control the circuit, along with equipment necessary to monitor both inductor current and battery voltages.However, in order to operate, an ancillary circuit needs to be implemented. The purpose of the ancillary circuit is to provide the interface and control signals needed to control and monitor the main circuit. The structure of the ancillary circuit is illustrated in Figure 4.2.

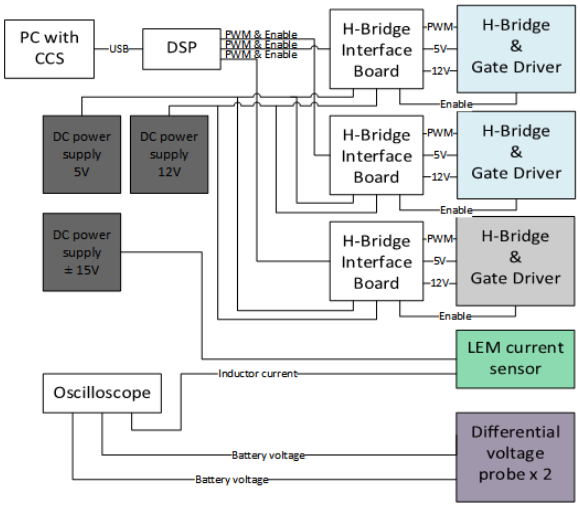


Figure 4.2: Schematic representation of the ancillary circuit.

From the figure it can be seen that the ancillary circuit consist of several elements. A brief functional description of each element is given below.

PC with CCS and Matlab/Simulink: Represents the visual interface, which is used to generate code capable of generating a desired PWM signal. The code necessary to produce the desired PWM signals is made using a matlab add-on called (Embedded Coder Support Package for Texas Instruments C2000 Processors). The support package provides a user friendly approach, with respect to programming of micro processors for those with limited knowledge within programming and enables fast implementation for test and build of prototype setup. The code is developed in simulink using block diagrams and exported to code composer studio (CCS), which compiles and deploys the code onto the micro processor where it is executed.

DSP: Represents the digital signal processor (DSP), where the generated code is deployed onto and executed. The specific DSP used for this project is the (TMS320F28335 Experimenter Kit), which have the following hardware features [Instruments, 2019a]:

- Control card that contains the DSP.
- Docking station for the control card.
- USB that enables real time in system programming and debugging,
- Header pin access to control card signals - including digital I/O and analog inputs.
- Breadboard area for customize routing/prototyping.
- Board power can be supplied either by USB cable or 5V barrel supply.

H-Bridge Interface Board: Represents the link between the DSP and the gate driver circuit, which serves the purpose of transmitting the output PWM signal from the DSP to the receiver of the gate drive circuit, along with external DC power, required to power these Integrate Circuits (IC's) consisting of the transmitter,receiver and gate driver.

Oscilloscope: Represent the interface used to receive, log and display the inductor current and battery voltage measurements, used to evaluate the performance of the test setup.

4.1.1 Ratings and Characteristics

As stated in the beginning of the chapter, it has been decided to use existing components for the setup, rather than custom made, due to the limited time frame. The component ratings and characteristics are as stated below.

DC power supply:

- 300V
- 5A

Load inductor:

- $6.5mH$
- 20A

The purpose of the load inductor is to shape the current representing the sinusoidal envelope, as stated in Section 3.5.1. It can be seen that two essential ratings are listed, with respect to the inductor, namely the inductance and the current rating.

The importance of knowing the inductance when designing an inverter is seen when referring to Equation 4.1 and 4.2[Ned Mohan, 2003].

$$V_L = L \cdot \frac{\partial i}{\partial t} \tag{4.1}$$

From Equation 4.1 it can be seen that the that the inductance serves multiple purposes, and can be used to either reduce current ripple, decrease switching frequency or applied voltage if increased.

Assuming a pure inductive load, Equation 4.2 can be used to calculate the current through the inductor.

$$I_L = \frac{V_L}{X_L} = \frac{V_L}{2 \cdot \pi \cdot f \cdot L} \tag{4.2}$$

It can be seen that the inductor can be used to either decrease the fundamental frequency of the current, increase the applied voltage or decrease the magnitude of the current.

The current rating of the inductor refers to the gauge wire amp rating and should not be exceed as it will cause permanent damage to the inductor. The current rating can can also be referred to as the saturation current and is the current level at which the magnetic core is fully magnetized, hence applying additional external magnetic field (H) will not result in higher magnetic flux density (B). As the core of the inductor reaches saturation it no longer behaves linearly but gets a non-linear characteristic, which is unwanted as it introduces harmonics, when used in AC circuits.

Since the inductance of the inductor used for the test setup is fixed along with the current limit, certain constrains are introduced into the system, which respect to applied voltage (V_{dc}), fundamental frequency (f_f) and switching frequency (f_{sw}).

DC link capacitor:

- $470\mu F$
- 450V

The purpose of the DC link capacitor is to supply constant DC link voltage by removing ripple caused by rectification, when converting AC to DC. However, since a DC power supply is used for the test setup it is assumed that the DC link voltage is constant. The purpose of the capacitor for the test setup presented in Figure 4.1 therefore mainly serves the purpose of protecting the DC power supply by storing energy and providing pulsating currents drawn by the inductor,hence keeping a constant DC-link voltage.

Equation 4.3 shows the effect of the capacitance on the relation between current pulse amplitude and duration, when a specified voltage ripple is defined [Ned Mohan, 2003].

$$I_C(t) = C \cdot \frac{\partial V(t)}{\partial t} \tag{4.3}$$

Having a fixed capacitance value for the test setup along along with a maximum current rating for the inductor, therefore limits the switching frequency with respect to voltage ripple.

H-bridge module:

- 63V at 1000nH DC link inductance
- 100A rms with passive cooling
- 1kHz at 1000nH DC link inductance and 100A rms

The ratings of the h-bridge modules used are rated values that ensures safe operation of the module and are based on system characteristics such as stray inductance and cooling capability, which are both limiting factors. The boards are provided by KK Wind Solutions.

Inductance not only exist in inductors but does also appear in wires and component leads that have current running through them, which creates magnetic fields. Inductance related to wires and components leads are referred to as stray inductance and is unwanted in a system as it can result in high voltage spikes across the switching devices, also called inductive kickback, which may exceed the rated voltage, hence damaging the device.

Equation 4.4, states Faraday's Law and shows the relation between the induced voltage relative to the change in magnetic flux. Rewriting Equation 4.4 by expressing the flux in terms of inductance and current, as stated by Equation 4.5,it is possible to get an expression that clearly shows the effect of inductance with respect to applied voltage and switching frequency, when operating at high current levels [Ned Mohan, 2003].

$$\mathcal{E} = -\frac{\partial \phi_B}{\partial t} \tag{4.4}$$

$$V = L \cdot \frac{\partial i}{\partial t} \tag{4.5}$$

Reducing stray inductance is therefore important if it is desired to switch at high frequency without damaging the switching device. However, stray inductance can not be avoided completely, hence a compromise must be made between maximum current and switching frequency.

Another way of avoiding damage to the switching device caused by inductive kickback, is to build a protecting circuit across it, referred to as a snubber circuit, which "snub" the phenomena occurring across the switching device [Erickson, 2004].

Figure 4.3 illustrates one of the most used snubber topologies, that is categorized as a passive and dissipating voltage snubber circuit, as it is made out of a capacitor and resistor and does not store and recycle the energy absorbed during switching transistion.

Figure 4.3: Schematic representation of the ancillary circuit.

Numerous snubber circuit topologies exist and can be designed in a smart manner to increase efficiency and ensure safe operation by limit $(\delta i/\delta t)$, $(\delta v/\delta t)$ and recycle energy stored during stitching transition. However, adding snubber circuits also increased complexity and price, hence an analysis should be made in order to determine whether or not a snubber is necessary. Such an analysis is beyond the scope of this project and will be saved for further work.

The snubber circuit is only active during the switching transitions, which is either turn-on or turn-off. The losses of the RC snubber topology can therefore bee estimated using Equation 4.6 [Erickson, 2004].

$$P_{loss,(RC)} = C \cdot V_{dc}^2 \cdot f_{sw} \tag{4.6}$$

The h-bridge modules provided for the test setup includes snubber circuits for protection, which limits the switching frequency of the module, since switching frequency is

proportional to power losses as stated by Equation 4.6, hence the board will heat up which could cause permanent damage.

Removing the snubber circuit would would resolve the problem related to limited switching frequency, but could damage the mosfets of the h-bridge which are only rated at 100V, hence the snubber circuit should not be removed.

Based on the knowledge acquired about stray inductance and snubber circuitry, it is possible to configure and manipulate the test setup in order to achieve a desirable output, without exceeding the ratings of the h-bridge modules, as stated below.

- *Reduce stray inductance of DC link by shortening current path and minimizing current loops.*
- *Increase switching frequency gradually and monitor temperature, while performing active cooling of the h-bridge module.*
- *Increase load inductance in order to lower switching frequency.*

4.2 Test Setup Operating Point

Based on the component characteristics it is possible to define the the operating point of the test setup by defining the voltage ripple and estimating the current through the inductor. The operating point is determined by external variables which can be adjusted, and refers to the DC link voltage (V_{dc}), fundamental frequency(f_f) and switching frequency(f_{sw}).

Defining a DC link voltage of 50V (V_{dc}), in order to stay below the operating point of the h-bridge module, along with a maximum inductor current of 5A ($I_{L(peak)}$), it is possible to estimate the fundamental frequency using Equation 4.1 and 4.7 [Ned Mohan, 2003].

$$V_L = V_{dc} = V_{ac(peak)} \tag{4.7}$$

$$f_f = \frac{V_{ac(peak)}}{2 \cdot \pi \cdot L \cdot I_{L(peak)}} = \frac{50V}{2 \cdot \pi \cdot 6.5mH \cdot 5A} \approx 245Hz$$

Finally the maximum switching frequency (f_{sw}) can be estimated using Equation 4.3 and 4.8 along with a definition of a maximum voltage ripple of 1% and a modulation index equal to unity.

$$I_{C(peak)} = I_{L(peak)} \tag{4.8}$$

$$\partial t = C \cdot \frac{\partial v_{peak}}{I_{C(peak)}} = 470\mu F \cdot \frac{50V \cdot 0.01}{5A} = 47\mu s$$

Having defined a modulation index equal to unity it is possible to estimate the switching frequency based on the current pulse duration calculated above.

Since the DC link voltage is not fixed, but can be adjusted, it is of interest to keep the modulation index at unity to maximize the output voltage while minimizing the Total Harmonic Distortion (THD), since the inverter is operating in the linear region.

Furthermore,it is know that the maximum voltage amplitude of a full bridge single phase inverter operating at a modulation index equal to unity is 78.5% of the applied DC link voltage [Alenka Hren, 2018].

Having calculated a pulse duration of $47\mu s$, it is possible to calculate the switching frequency of the inverter module, represented by the (dark grey) area in Figure 4.1.

$$f_{sw} = \frac{100\%}{78.5\% \cdot 47\mu s} \approx 27.1kHz$$

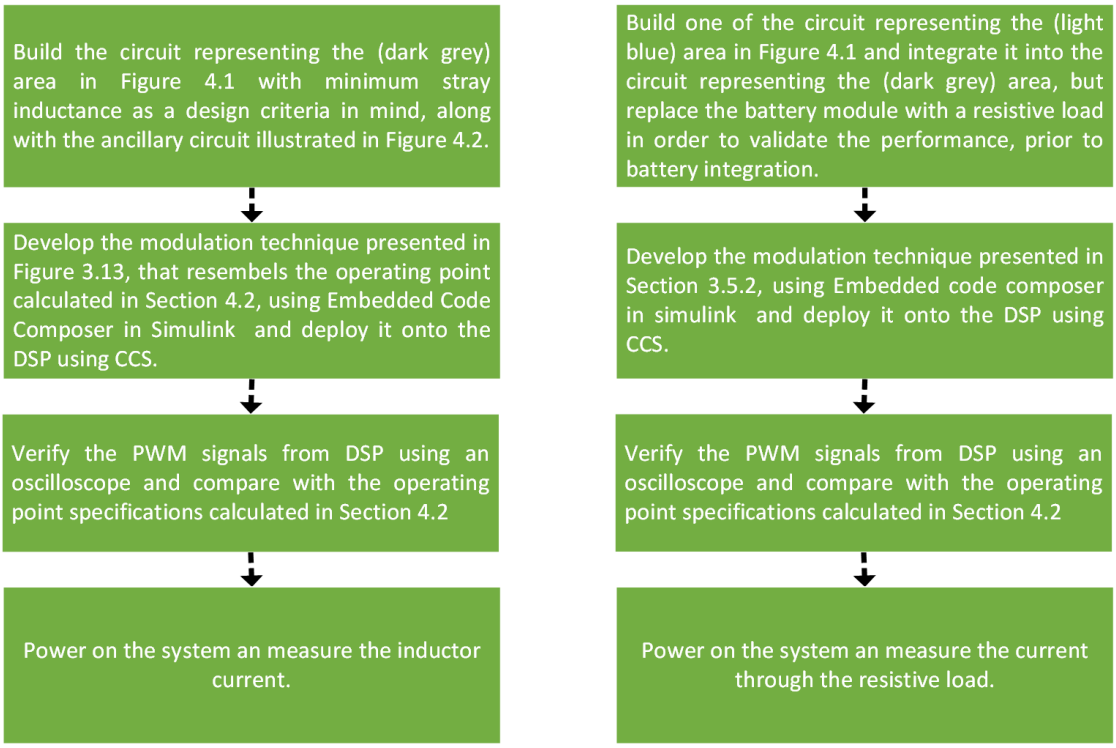
The frequency of the PWM signal for the h-bridge modules represented by the (light blue) area in Figure 4.1, that are used to chop the current can be increased or decreased depending on the number of desired pulses within the sine envelope, as stated in Section 3.4 and illustrated in Figure 3.15.

The frequency of the PWM signals used to chop the current is chosen to be ten times (f_f), hence resulting in five pulses within the sine envelope.

4.3 Methodology

It has been stated in the beginning of this chapter, that it is of interest to apply a systematically approach, when it comes to test an verification of the test setup, in order to increase safety and decrease time spend on debugging in case something goes wrong.

Figure 4.4 illustrates two flow diagrams, that shows the steps of which the system is going to be build and tested in a chronologically order, with safety and efficiency in mind.



(a) Flow diagram h-bridge inverter module. (b) Flow diagram h-bridge battery module.

Figure 4.4: Flow diagram representation of test procedure for both the h-bridge module serving as a full bridge single phase inverter (a) and the h-bridge module containing one battery cell (b).

When both test are concluded based on satisfactory operating performance, the final test setup represented by the (light grey) area in Figure 4.1 can be build, hence adding the last h-bridge module.

4.4 Code for DSP PWM implementation

In this section a short and practical walk through of how the code, capable of generating PWM signals for the DSP, is generated using embedded code composer in simulink, hence enabling others to manipulate and develop code for different PWM configurations.

4.4.1 Modulation Technique Implementation

From Figure 4.5 it can be seen that the carrier signal is defined by specifying the shape of the signal. The shape is defined in the field stating the counting mode. The counting

mode is specified as 'up', which means that the signal is shaped as a saw tooth signal.

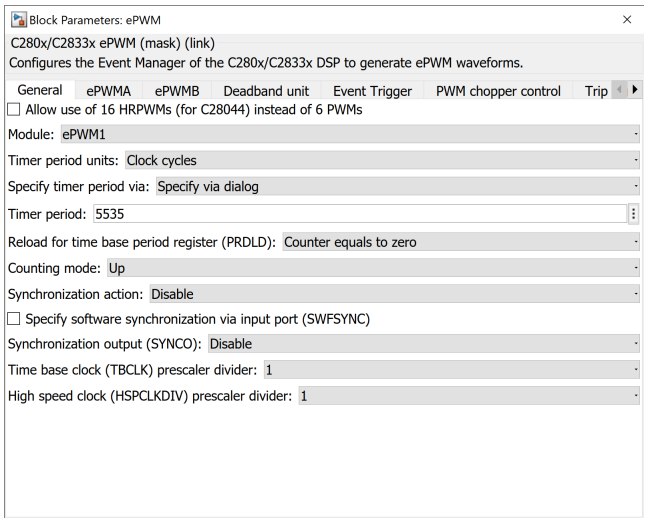


Figure 4.5: Configuration of carrier signal used for SPWM modulation.

In order to specify a desired switching frequency, defined as the 'Timer period' it has to be converted into clock cycles, as stated by Equation 4.9.

$$t_{clock} = \frac{\text{CLK}}{f \cdot \text{TBCLKD} \cdot \text{HSPCLKDIV}} \tag{4.9}$$

The definition of the parameters used in Equation 4.9 are stated below:

CLK:

Represents the Clock frequency of the DSP which is 150MHz.

TBCLK:

Represents the Time Base Clock Divider which is a constant used to tune the conversion between seconds and clock cycles.

HSPCLKDIV:

Represent the High Speed Time Base Clock Divider which is an additional constant used to improve tuning of the conversion between seconds and clock cycles.

The following switching frequency expressed in clock cycles is calculated using Equation 4.9.

$$t_{sw(clock)} = \frac{150\text{MHz}}{27.1\text{kHz} \cdot 1 \cdot 1} \approx 5535$$

The initial switching frequency has been set to 27.1kHz, as stated in Section 4.2 and can be changed simply by recalculating the clock cycles using Equation 4.9. It should be noted that the value of the switching frequency represented by clock cycles has to be an integer value.

From Figure 4.6 it can be seen that the modulation signal is defined using the field stating the 'CMPA units','Specify CMPA via' and 'CMPA intial value'. CMPA represents

the reference signal, which is specified through an input port that receives a sinusoidal modulation signal at a desired frequency and amplitude, which is specified in simulink. The CMPA unit is specified in percentages instead of clock cycles for quick and simple manipulation of the modulation index.

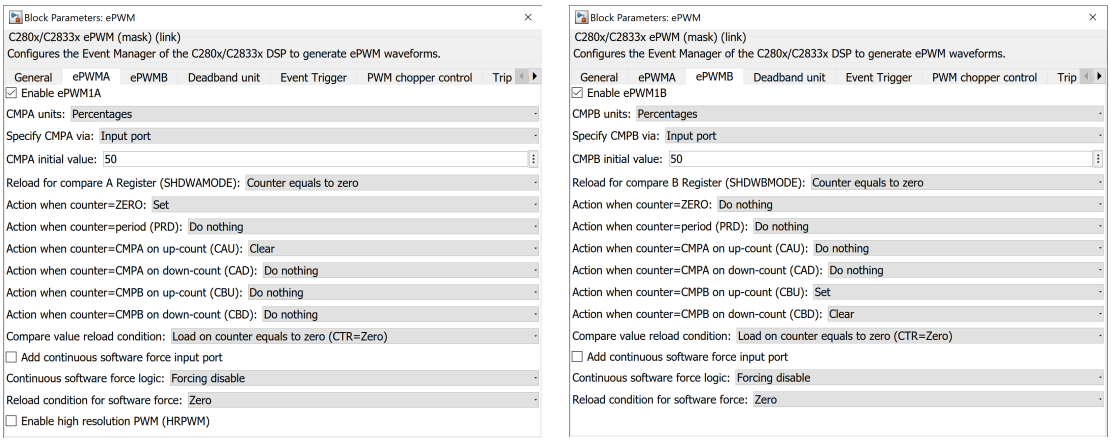


Figure 4.6: Configuration of modulation signal and SPWM modulation technique.

Since the DSP processes discrete signals, it is important to feed a sample based signal to the input port, representing the CMPA value. For SPWM modulation a sample based sine wave is feed to the input port and for regular PWM a constant between 0-100 is chosen depending on the desired duty cycle.

The modulation technique is implemented through complimentary trigger configuration defined by the fields stating 'Action when counter', which produces two complimentary PWM signals.

The first PWM signal (ePWMA) is set to trigger (set) when the saw tooth carrier signal is equal to zero and trigger once again (clear) when the carrier signal is equal to the modulation signal.

The second PWM signal (ePWMB) is set to trigger (set) when the carrier signal is equal to the modulation signal and trigger once again (clear) when the carrier signal has reached its maximum value and drops to zero.

4.4.2 Dead Time Implementation

When operating the h-bridge using complimentary PWM signals it it important to implement dead time, due to the turn-on and turn-off characteristics of the transistors. Figure 3.15 shows an ideal current response based on the assumption that the transistors turn on and off instantaneously. However, this is not the case as transistors suffers from turn-on and turn-off time caused by the time it takes to charge and discharge the gate capacitors. Driving a h-bridge using complementary PWM signals without dead time implementation would therefore create a low resistive path between the high and low side, since either the high or the low side would be switched on while the other is still discharging. This is also refereed to as 'shoot through' and is a undesirable phenomena as it causes excessive damage to both the transistors and power supply.

The gate drivers of the h-bridge module used for the test setup have build in dead time, hence there is no need to program dead time onto the DSP.

In case it is desired to implement dead time through programming of the DSP, it can be estimated using Equation 4.10.

$$t_{dt} = t_{on} + t_{off} = (t_{d(on)+t_r}) + (t_{d(off)+t_f}) \tag{4.10}$$

$$t_{dt} = (21\text{ns} + 11\text{ns}) + (49\text{ns} + 38\text{ns}) = 119\text{ns}$$

The time parameters used in Equation 4.10 can be found in Appendix D which represent the time it takes to fully turn on and turn off the transistor used for the test setup prototype.

The following dead time expressed in clock cycles is calculated using Equation 4.9.

$$t_{dt(clock)} = \frac{150\text{MHz}}{\frac{1}{119\text{ns}} \cdot 1 \cdot 1} = 28.5$$

Figure 4.7 illustrates the configuration of the dead time.

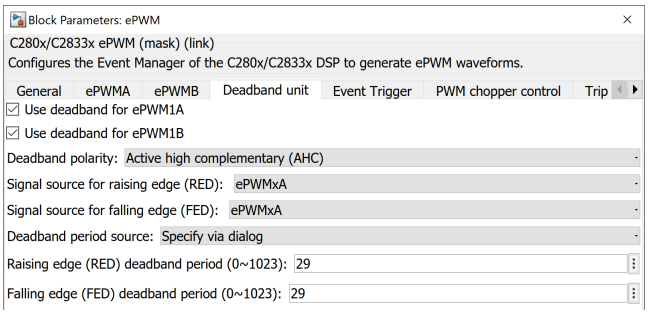


Figure 4.7: Configuration of dead time.

Since the dead time can only be specified by an integer value, it should be rounded up to avoid the risk of 'shoot through'.

Utilizing the information described above with respect to configuration of the SPWM technique on the DSP, it is possible to configure the modulation technique used for the intelligent current control of the h-bridge modules containing the batteries cells. A walk through of that configuration will therefore not be made.

4.5 Laboratory Test Setup

Based on the schematic representation of the test setup, illustrated in Figure 4.1 and 4.2, along with the explanatory purpose of each sub circuit and components, it is possible to build the physical setup illustrated in Figure 4.8.

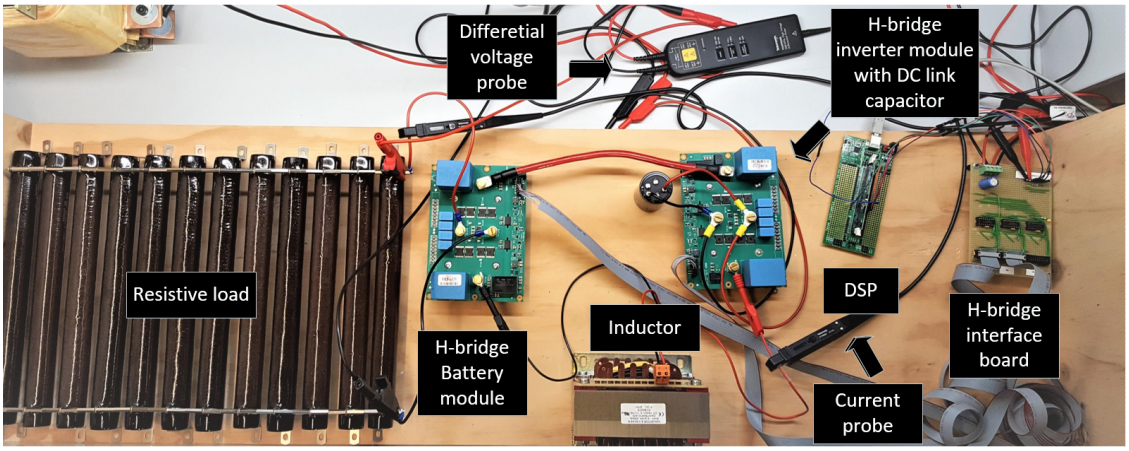


Figure 4.8: Physical test setup prototype.

The From Figure 4.8 it can be seen that only two h-bridge boards are present, due to malfunction of the third board. Furthermore it should be noted that a DC power supply of 300V/5A is feeding power to the DC link of the h-bridge inverter board. An additional two-channel DC power supply is also used to supply 5V and 12V respectively, to power the IC's found on both the h-bridge interface and module boards.

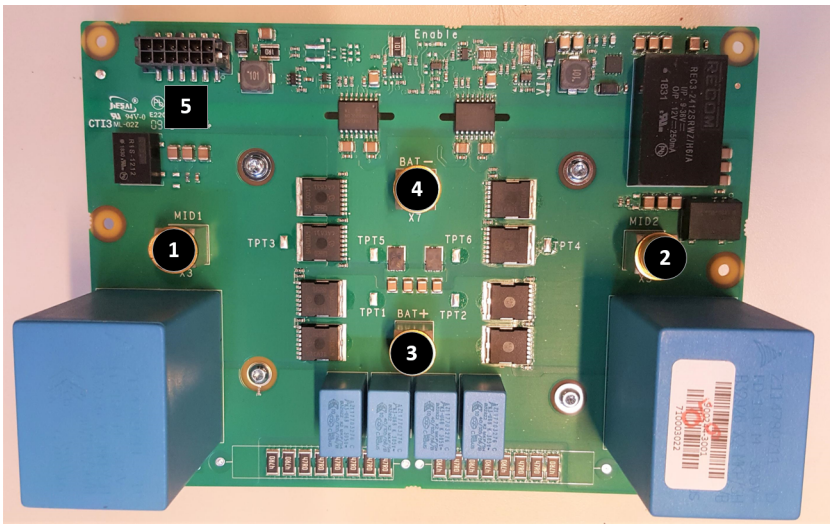


Figure 4.9: H-bridge module provided by KK Wind Solutions.

Figure 4.9 shows a close up of the h-bridge board, provided by KK Wind Solutions, which is used both as an inverter module and battery module. The picture includes five marks, that is intended to provide reference points, to facilitate a short functional explanation of the board.

Point (1) and (2) are the connection point between the high and low side (middle point) of each leg of the h-bridge and is the points where the inductor and h-bridge battery modules are connected in series.

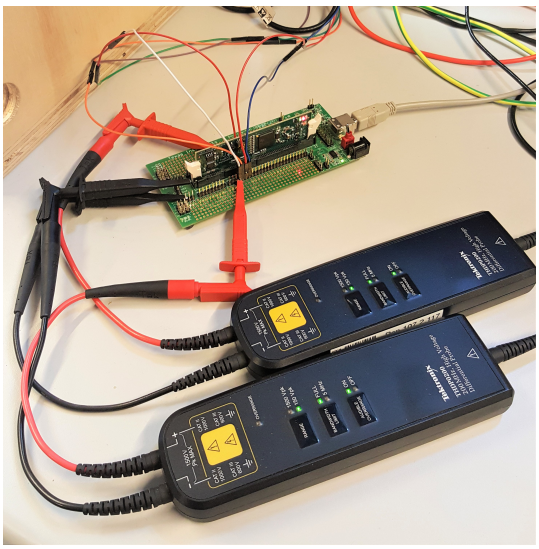
Point (3) and (4) are the connection points, that connects the high and low side of the h-bridge module and are the points where the DC power supply or the battery cells are connected, depending on the board configuration.

Point (5) is connected to the h-bridge interface board and provides 5V and 12V, along with both PWM and enable signals, necessary to power and drive the IC's on the board.

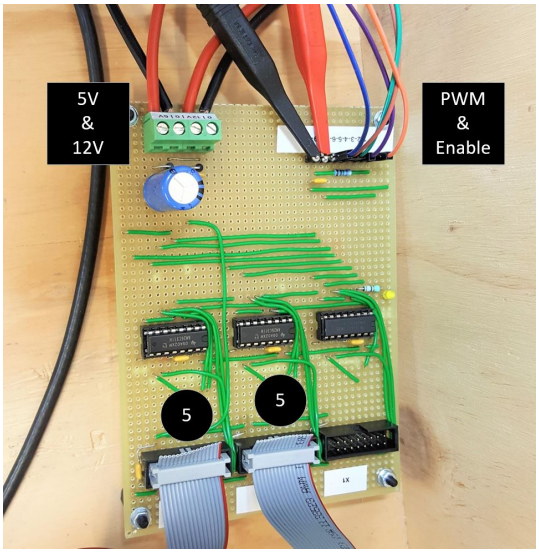
Figure 4.10 shows to pictures related to the ancillary circutry of the test setup. Figure 4.10a shows the test and validation of the PWM and enable signals, generated through simulink and executed using CCS.

The signals are verified, using two differential voltages probes,connected to an oscilloscope. The probes are connected to ground and the output pin of interest on the DSP. Two differential voltage probes are utilized to validate the complimentary SPWM signals for the inverter module, as it would be impossible to validate, measuring one at a time.

Figure 4.10b shows the h-bridge interface board, which is connected to the DSP and a two-channel power supply. The DC power and DSP signals are transmitted to the h-bridge boards through the output terminals labeled with the number (5), which corresponds to the label in Figure 4.9.



(a) DSP and differential voltage probes.



(b) H-bridge interface board.

Figure 4.10: Test and validation of ancillary circuitry, consisting of DSP (a) and h-bridge interface board (b) before test.

From the pictures, it can be seen that two out of three output terminals are connected. One of the two reasons for this, is that one of the h-bridge board were malfunctioning and could therefore not be utilized, as explained earlier. The second reason is related to signal disturbance. During validation of the DSP signals, a problem was encountered with respect to signal interference, which caused the DSP signal to oscillate.

Through systematically debugging it was discovered that the input of the the rightmost output terminal was shorted with the output port in the middle. An easy fix was to shift the signals from the rightmost output port to the leftmost.

4.6 Results

Having build the setup and validated the output signals from the DSP, it is possible to proceed to the testing face in accordance with the methodology presented in Section 4.3.

Figure 4.11 shows the current through the inductive load of the inverter module when switching at 27.1 kHz, at a desired frequency of 245 Hz, as specified in Section 4.2.

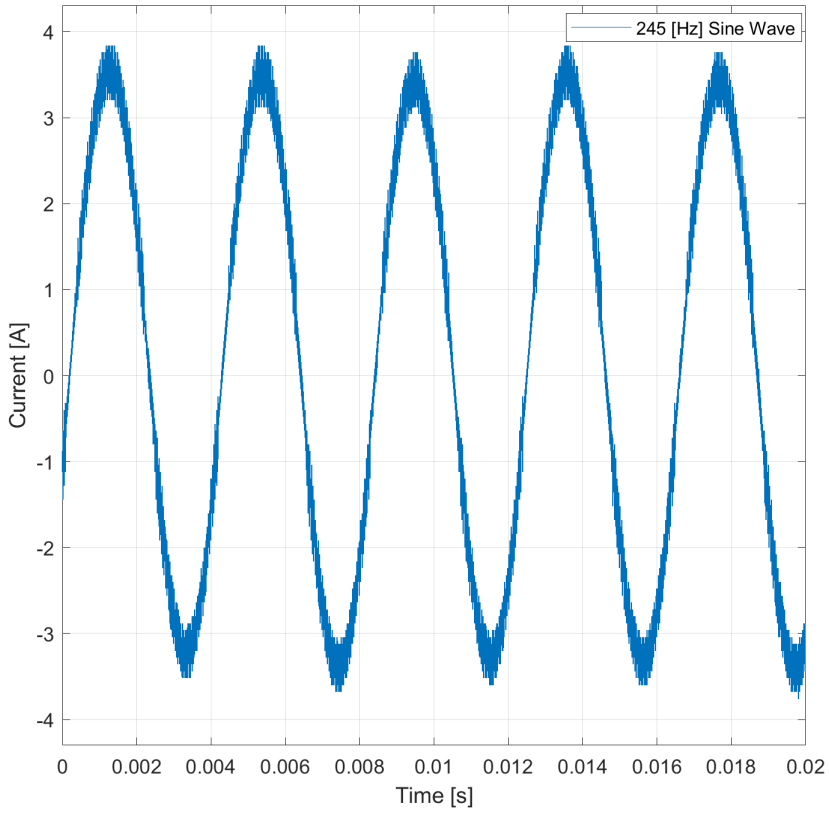


Figure 4.11: Current measurement during test of the h-bridge inverter module.

The applied DC link voltage during the test is 50V, which is also in accordance with the specifications made in Section 4.2. However, looking at the amplitude of the sinusoidal current, it can be seen that the amplitude is lower than the specified amplitude of 5A. This could be explained, based on the assumption of having a pure reactive load, which is highly unlikely. The assumption was made in order to estimate the worst case scenario, with respect to current amplitude, hence some resistance must be present in the system, which increases the AC circuit impedance and thereby lowers the current.

The purpose of the test setup is to evaluate whether or not the hybrid h-bridge topology

is capable of generating a current pattern that resembles the one illustrated in Figure 3.2, hence the amplitude of the current is less relevant. Therefore it is decided to proceed to the next phase, based on a satisfactory shape of the sinusoidal current illustrated in Figure 4.11.

Next phase in the test procedure according to the Figure 4.4b, is to build and test the performance of the h-bridge battery module, used to chop the sinusoidal current, and create the pulses, intended for charging and discharging.

Figure 4.12 illustrates the current response during test of the h-bridge battery module.

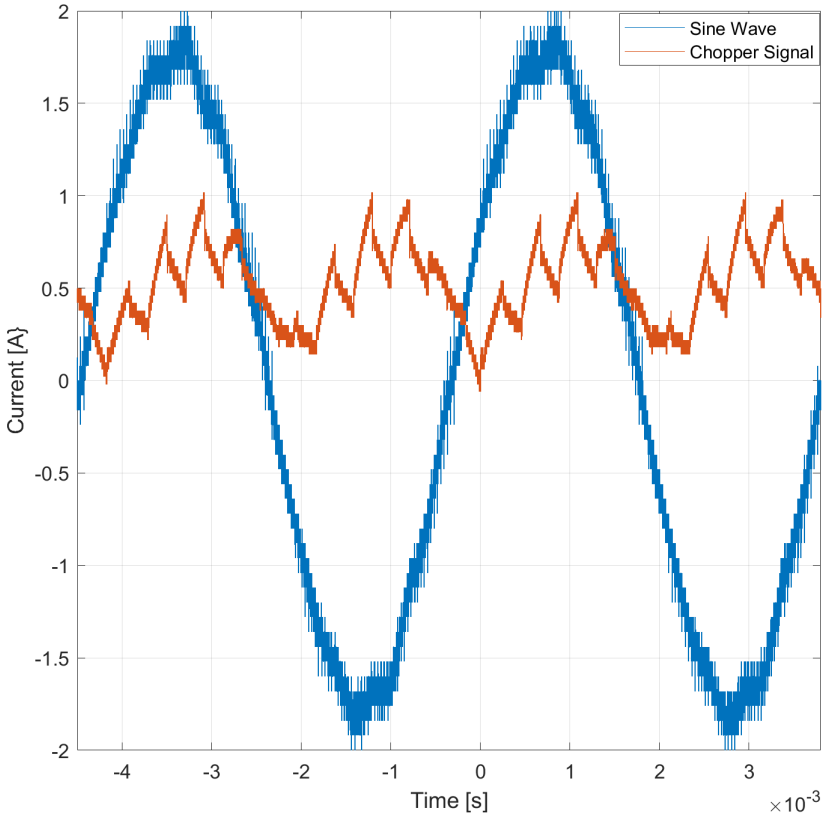


Figure 4.12: Current response at high resistive/inductive load.

In order to understand what is going on and why, a reference is made to Figure 4.8, which illustrates a rather chunky resistive load. The resistive load consist of 12 high power resistors rated at 15Ω each, as other resistors found in the laboratory were only rated at 5W. Initially it was chosen to only use one of the resistors as a load, which gave the results illustrated in Figure 4.12. A low current was expected due to the rather big load, but the response was not.

Inspecting the resistive load, it was discovered that it had inductive characteristics which explains the response, hence the remaining resistors was added in parallel to lower the inductance.

Figure 4.13 shows the test result from the test of the h-bridge battery module, after the modification made to the load, where a sinusoidal current at approximately 240 Hz and a pulse charging pattern at approximately 2.4 kHz is illustrated.

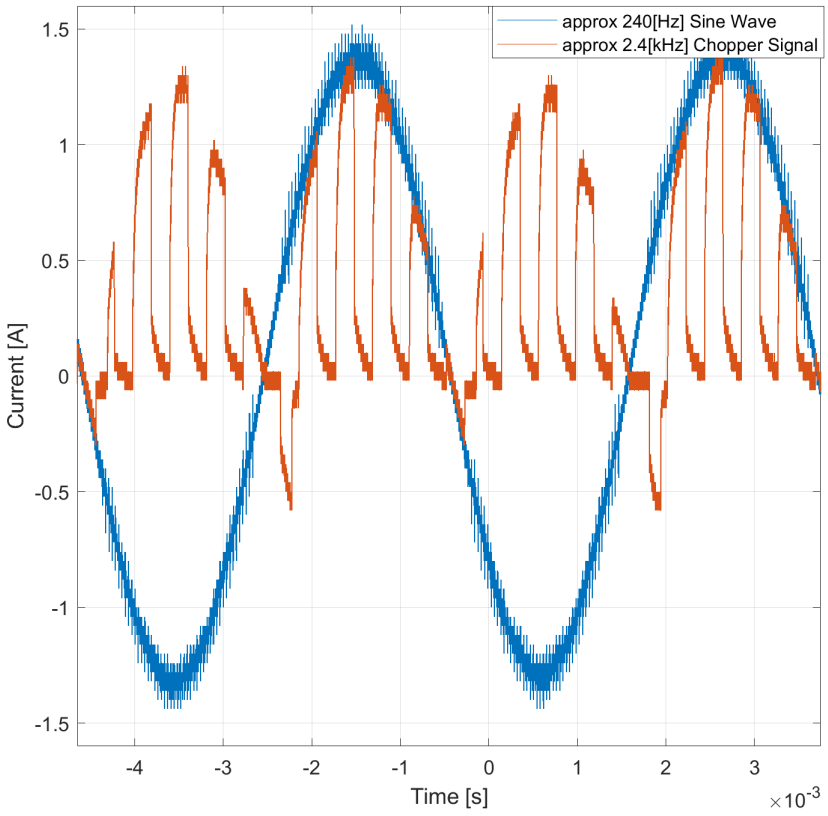


Figure 4.13: Current measurement during test of the h-bridge battery module.

Comparing Figure 4.13 with Figure 3.2, that illustrates the desired pulse pattern, it is clear to see the similarity, hence the performance of the h-bridge battery module is evaluated as satisfactory. Furthermore, it can be seen that lowering the inductance by parallel connecting the high power resistors, had the desired effect.

However, some deviation is present and should be discussed shortly as it is important in order to ensure correct operation of the test setup. In Figure 4.13 it can be seen that some pulses are negative, compared to the rest. This is caused by small phase and frequency difference between the sinusoidal current and the intelligent current control, that chops the sinusoidal current and creates the pulses.

Due to limited time and experience with programming of the DSP, an assumption was made with respect to the phase and frequency of the sinusoidal current. The assumption was made that both the phase and frequency was constant, as it would have required to implement an analog to digital converter (ADC) in order to measure the polarity of the current and use that as a trigger, instead of relying on phase synchronisation.

Using the polarity of the sinusoidal current as a trigger is the original idea, which is

presented in Section 3.5.2, but could be replaced using phase locked loop (PLL) instead. Implementing PLL would make it possible to use the existing code and remove the necessity of implementing an ADC.

Variations in frequency also occurred and are assumed to be related to the output of the DSP. Resolving this problem could be be done through optimization of the generated code for the DSP.

The test results illustrated in Figure 4.13 are obtained at low DC link voltage, which shows a symmetrical sinusoidal current. However, increasing the DC link voltage introduces an offset, as illustrated in Figure 4.14.

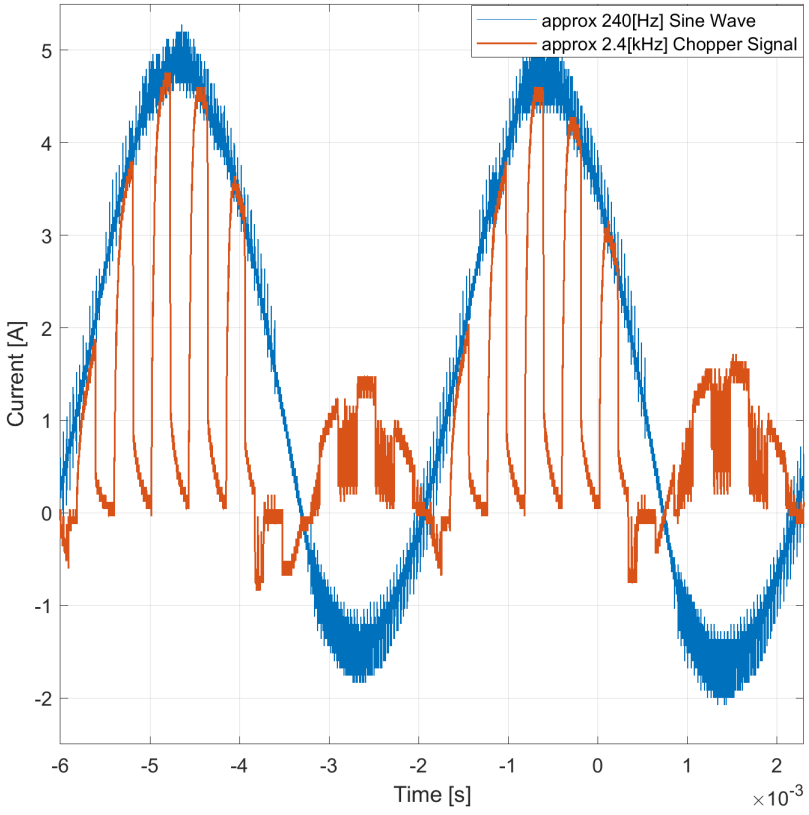


Figure 4.14: Current offset error.

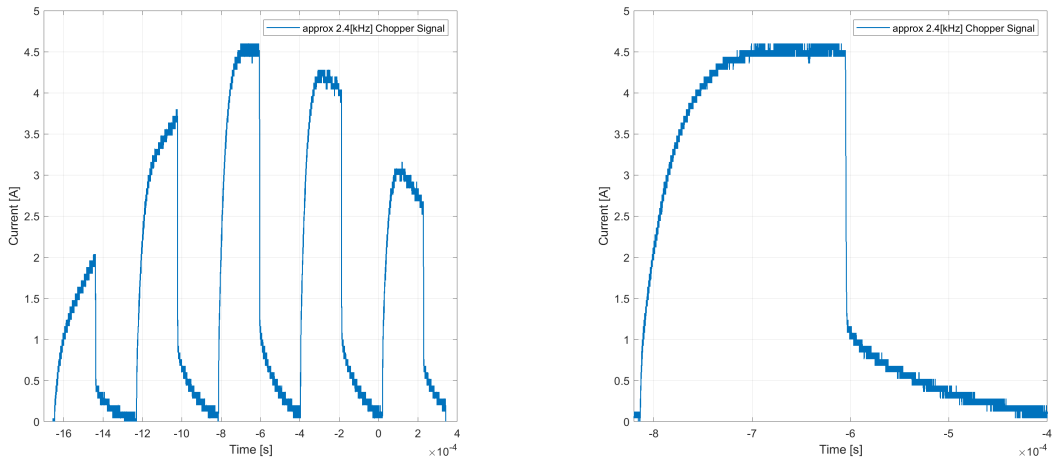
As it can been seen, the offset has a great negative influence on the amplitude of the current charging pulses, which is unwanted. The error occurs due to the fact that the setup is operated under open loop conditions, hence a controller should be designed to eliminate this error.

In order to fully evaluate the performance of the hybrid h-bridge it is necessary to inspect the shape, symmetry and slope of the current pulses, illustrates in Figure 4.15.

Looking at Figure 4.15a it is clear to see that the amplitude of the current pulse pattern has the amplitude and shape, resembling a rectified sinusoidal envelope, along with a

symmetrical 50% duty cycle distribution. Inspecting Figure 4.15b it can be seen that the current response dos not comply with the requirements stated in Section 3.2.

However, based on the knowledge obtain through inspection of the resistive load and the simulation results presented in Section 3.5, it should be possible to make the current response faster by reducing the inductance at the DC link of the h-bridge battery module.



(a) Charging current pulse pattern.

(b) Single current pulse.

Figure 4.15: Current measurement during test of h-bridge battery module

Conclusion 5

In Chapter 1 the background for this project was presented, stating how an accelerated transistion towards an electrified transportation and energy sector has had a positive impact on lithium ion battery manufacturing cost, hence lowering the price tag per kWh. Several points were listed, stating the advantages of implementing batteries into the energy sector to serve as energy storing devices. One of those advantages being a better integration of renewable energy sources, such as wind turbines.

Finally, the importance and necessity of prolonging the battery life time and performance were pointed out, in order to enhance its competitivity.

A short overview of lithium ion battery structure, charging strategies and battery degradation diagnostics were presented, to showcase the fields of interest when talking about battery lifetime and performance. Based on these and the requests and wishes from KK Wind Solutions, it was decided to design a test setup capable of stress testing lithium ion batteries, in order to map the performance and estimate the life time.

Based on the test setup requirements, specified i collaboration with KK Wind Solutions, two topologies were investigated as possible candidates, with the capability to perform according to the requirements made in Section 3.2.

The first topology was a traditionally four switch buck boost converter, that was intended to operate solely in boost mode, due to the OCV characteristics of the lithium ion batteries. The topology was configured, such that two batteries were connected in parallel, hence exploiting power circulation with the goal of eliminating the need of external power. The topology was capable of replicating a pulse pattern of high resemblance to the one specified in Figure 3.2.

However, it was discovered that the topology did not comply with the requirement made, with respect to $(\partial i/\partial t)$, caused by the inductor and the fact that the topology had to operate at DCM to generate the specified pulse pattern. Furthermore, a need to supply power to the system was found necessary, in order to test the batteries at constant SoC, since losses will always be present. Based on the analysis of the four switch buck boost converter, it was concluded to find another topology as a candidate for the test setup.

From the analysis and limitations of the four switch buck boost converter, a new topology was introduced, namely the hybrid h-bridge converter. The converter resolved the problem of the four switch buck boost converter, as it utilizes three different h-bridge module, which are divided into to categories. The first category is dedicated to the h-bridge inverter module, which is utilized to generate a sinusoidal current that shapes the envelope of the current pattern, illustrates in Figure 3.2, meanwhile supplying external power to the

system to compensate for losses. The other category is dedicated to the h-bridge battery module, which is utilized to chop the sinusoidal current, hence eliminating the slow current response, encountered during analysis of the four switch buck boost converter, as it does not suffer from the limitations of operating in DCM mode in order to replicate the specified current pattern. A benefit and downside of the hybrid h-bridge is the increased amount of transistors, which increases flexibility but at the same time also the complexity of the system, in terms of operation control.

An intelligent current control scheme was developed and based on the performance of the hybrid h-bridge it was decided to build a prototype of the topology and perform a physical test to validate the performance.

Due to the limited time frame of the project, it was decided to build a prototype capable of making a prove of concept, rather than designing a system from scratch, capable of operating at according to the requirements stated in Section 3.2. Furthermore, some assumption were made, stating that the system would operate under open loop control and that no BMS system would be designed, hence no batteries have been tested, but have been replaced with resistive loads, due to safety.

Prior to testing, an overview of the prototype test setup, methodology and operating condition, were made to provide a systematical approach, as stated in Chapter 4. Based on the instructions made in Chapter 4, it was possible to perform the test, necessary to validate the performance of the hybrid h-bridge topology.

Evaluating the test results, based on the analysis and discussion made throughout Section 4.6, it can be concluded that the hybrid h-bridge topology is a candidate worth investigating as it shows great potential, when comparing its performance to the requirements stated in Section 3.2. Several suggestions have been pointed out throughout Section 4.6, which would enhance the performance of the hybrid h-bridge topology, hence make it comply with the requirements. The suggestions mainly revolves around closed loop control and PLL implementation to eliminate steady state errors and phase shift. A reduction of inductance and change of gate resistance have also been suggested to improve $(\partial i/\partial t)$. A further study would therefore be necessary in order to fully validate the hybrid h-bridge topology as a suitable candidate for the test setup.

Further Work 6

The scope of this project has been to investigate suitable converter topologies, looking at limitations and possibilities, and develop a corresponding control strategy, that is capable of charging and discharging lithium ion batteries according to specifications made in Section 3.2. However, designing such system has multiple aspect and is difficult to fit within one single project, hence a short summary is presented in this chapter, highlighting possible areas of investigation for further work.

6.1 Rated System Design

A thorough system design should be performed, in order to ensure reliable, correct and safe operation of the test setup at rated conditions. It has been pointed out, that the test setup, which has been build for this project only serves the purpose of demonstrating, whether or not the chosen topology is a suitable topology for pulse charging and discharging according to the specifications made.

6.2 Closed Loop Control

This project has not focused on controller design, hence the system has been operated under open loop conditions. Evaluating the performance of the test setup, has pointed out the necessity of closed loop control to remove any steady state error and reduce oscillation, as it has a great influence on both the shape and amplitude of the charge and discharge pulses.

To ensure that the battery is either charging or discharging at specified time intervals set by the operator, it is necessary to implement either PLL or a ADC converter to measure the polarity of of the current. This is crucial, since the intelligent current control of the h-bridge modules, containing the battery cells, is based on either knowing the exact phase or polarity of the sinusoidal current. Any offset would cause the battery to constantly switch between charging and discharging, hence alternating the current profile applied to the battery cell.

6.3 Modulation

Only the SPWM modulation technique has been introduced in this project, along with the choice of operating within the linear range, hence not operating above a modulation index greater than unity. It could be interesting to investigate other modulation techniques,

such as Space Vector Pulse Width Modulation (SVPWM), along with overmodulation and evaluate the pros and cons, with respect to increased voltage, complexity and THD.

6.4 BMS Design

A brief introduction to battery charging strategies along with voltage characteristics compared to SoC, has been made in Section 1.2.2. It was stated that it can cause permanent damage to a battery cell if it is overcharged, hence exceeding the voltage limit of the battery cell. In order to prevent this, it is necessary to design and implement a Battery Management System (BMS), to protect the battery cell, by monitoring and tracking the voltage and SoC of the battery.

6.5 Battery Diagnostician

The purpose of the test setup is to perform accelerated life time test and reliability analysis of the battery cells. A battery diagnostician strategy should therefore be developed, in order to determine which parameters should be measured in order to evaluate health and performance of the battery cells. Figure 1.4, illustrates some causes and their effects on both capacity and power fade, and could therefore be used as a good starting point.

6.6 Thermal Management

It would be interesting to look into thermal management, both with respect to the test setup and the battery cell.

The test setup is is rated to run at high amp-rate which could lead to high losses depending on the efficiency of the test setup. Therefore, it would be interesting to look at thermal management, as it is essential to prolong the lifetime and enhance reliability and performance of the test setup.

Thermal management of the batteries is also interesting, since temperature control of the battery can be used as a stress parameter, to simulate both hot and cold operating environment.

6.7 Charge and Discharge Rate (di/dt)

A further study should be made with respect to the slope of the charge and discharge current pulses, in order to ensure the specified requirements stated in Table 1.1.

Possible areas of interest would be to look into they stray inductance between h-bridge board and battery cell, as this have a negative impact on the slope. Another area of interest would be the gate resistance of the mosfets, which has an influence on the turn-on time.

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Battery Data Sheet A

中航锂电(洛阳)有限公司 CHINA AVIATION LITHIUM BATTERY CO., LTD.	产品规格书 Specification	版本号 Version Number：G/0 发行日期 Circulation Date：2016-7-20

产 品 规 格 书
Product Specification

方形锂离子电池

Prismatic lithium Ion Battery

型号：L148F20

Model: L148F20

中航锂电（洛阳）有限公司

China Aviation Lithium Battery (Luoyang) Co., Ltd.

4. 产品性能 Product Performance

4.1 技术参数 Technical Parameters

序号 NO.	项目 Items		参数说明 Parameter	备注 Remark
1	额定容量 Nominal Capacity		20Ah	标准放电 Standard Discharge
2	最小容量 Minimal Capacity		20Ah	标准放电 Standard Discharge
3	工作电压 Work Voltage		2.5~3.65V	
4	内阻（Ac. 1kHz） Internal Resistance（Ac. 1kHz）		0.7±0.1mΩ	新电池、30%SOC Fresh Cell、30%SOC
5	充电时间 Charging Time	标准充电 Standard Charge	~2h	参考值 Reference Value
		快速充电 Fast Charge	~0.5h	
6	推荐SOC使用窗口 Recommended SOC Window	SOC ： 10%~90%		
7	工作温度 Operating Temperature	充电温度 Charging Temperature	0~45°C	参考第 4.2 节 Refer to section 4.2
		放电温度 Discharging Temperature	-20~55°C	参考第 4.4 节 Refer to section 4.4
8	电池重量 Weight		0.65±0.03 kg	
9	壳体材料 Shell Material		铝 Aluminium	

4.2 充电模式 Charging Model

序号 NO.	参数 Parameter	规格 Values	备注 Notice
4.2.1	标准充电模式 Standard Charging Model	室温下，以10A恒流持续充电至单体电池电压3.65V，然后在3.65V下恒压持续充电直至电流下限≤1A At room temperature, charged to 3.65V at a constant current of 10A, and then, changed continuously with constant voltage of 3.65V until the current was not more than 1A.	

中航锂电(洛阳)有限公司 CHINA AVIATION LITHIUM BATTERY CO., LTD.	产品规格书 Specification	版本号 Version Number：G/0 发行日期 Circulation Date：2016-7-20

附录 Appendix:

1.单体电池常温放电典型曲线图

A typical curve of single battery discharged at room temperature.

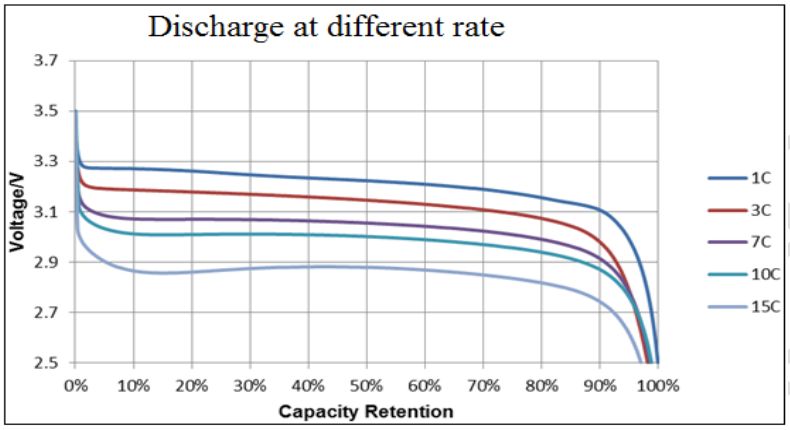


图 1. L148F20 常温放电曲线

Graph1. Discharge curve of L148F20 at room temperature

2. 单体电池不同温度 20A 放电典型曲线图

A typical curve of single battery discharged with 20A at different temperature.

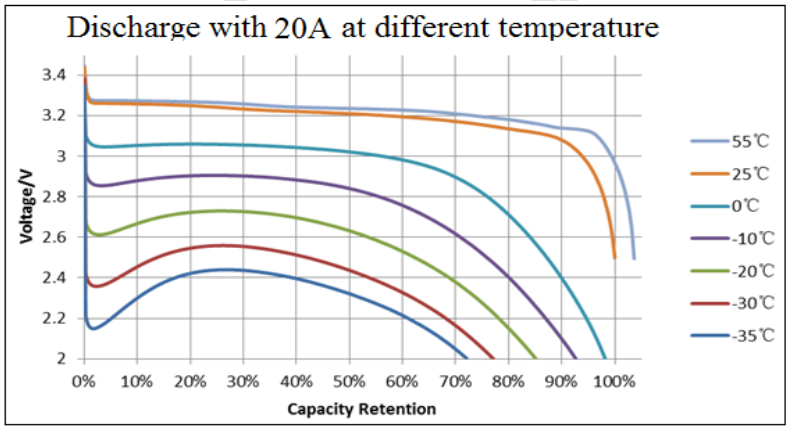


图 2. L148F20 不同温度放电曲线

Graph2. Discharge curves of L148F20 at different temperatures

3. 单体电池 3000 次循环图

3000 times cycling curve of single cell

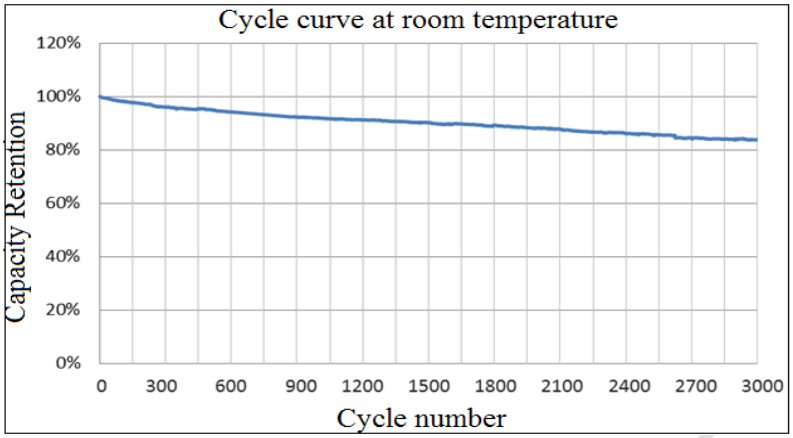
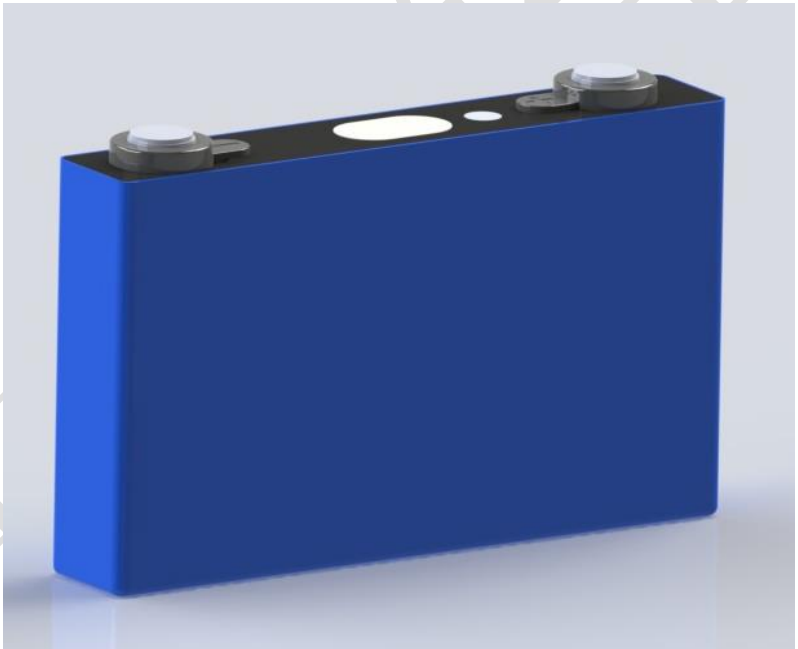


图 3. L148F20 常温循环曲线

Graph3. cycling curves of L148F20 at room temperatures

4. 单体电池立体效果图

3D effect picture of the battery

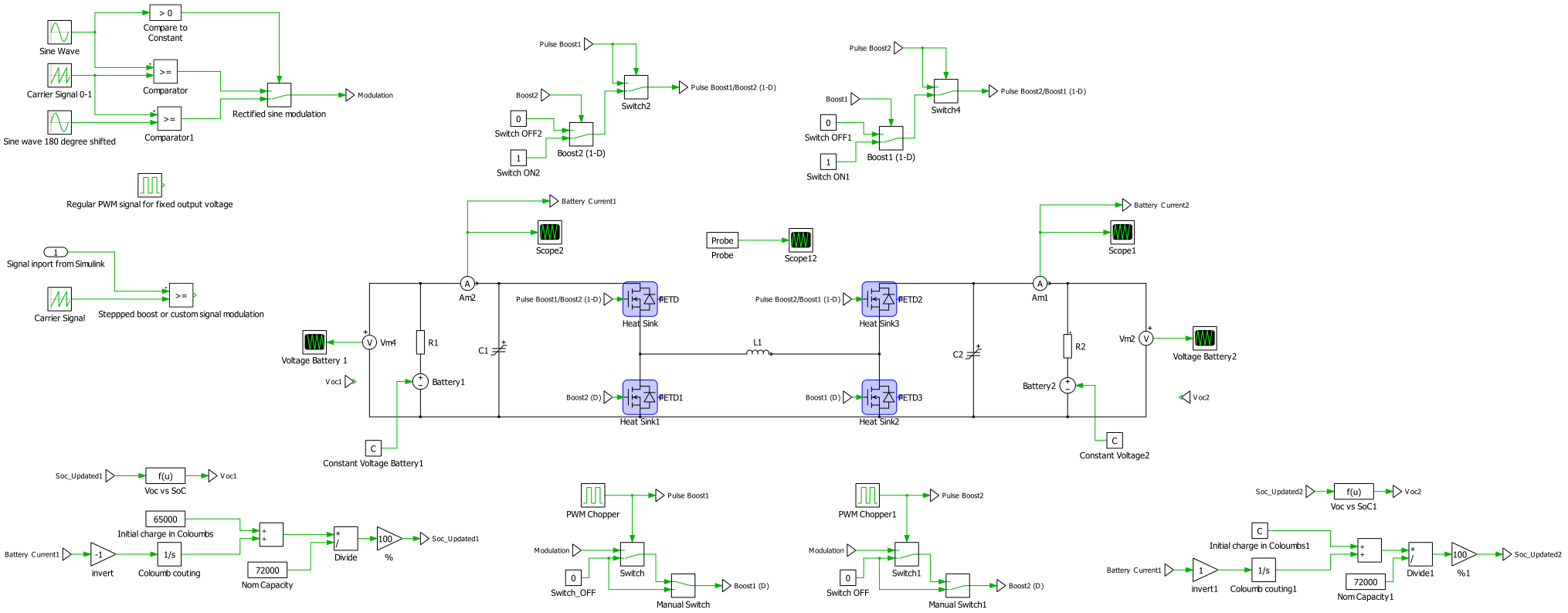


注：单体电池警示标签的内容会根据电池的认证情况和使用区域而变化，确切内容请咨询销售人员。

Notes: The content of warning labels will slightly modified according to different certification and application regions of battery. For more details, please contact the sales staff.

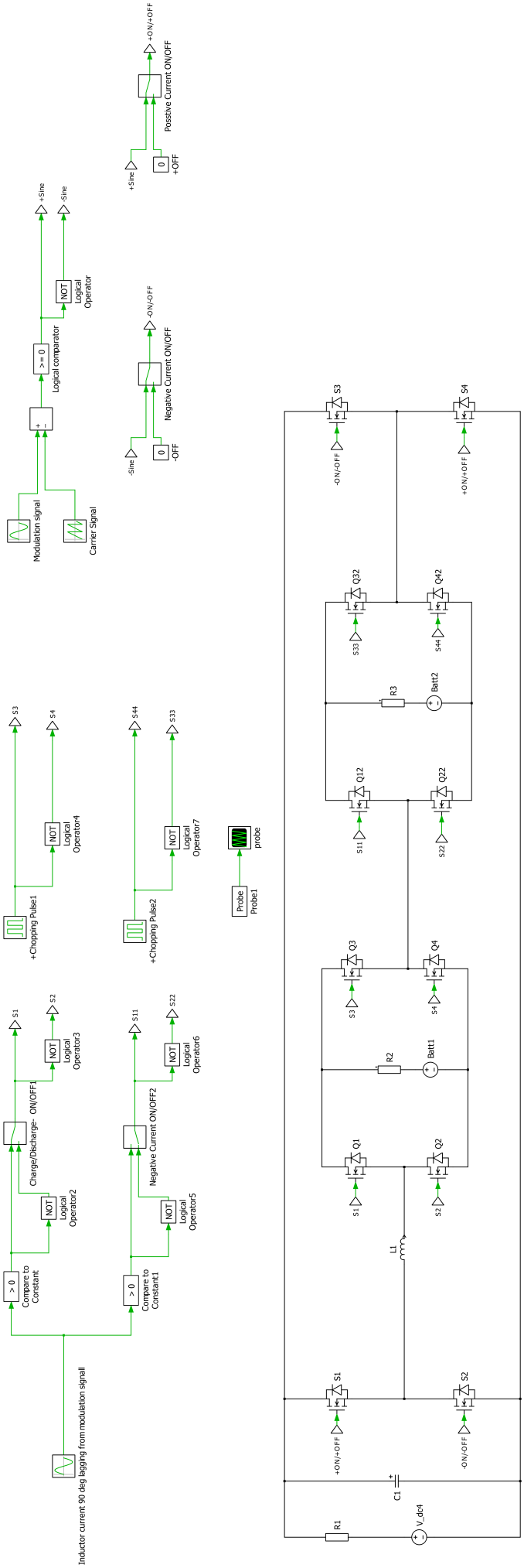
Bi-directional buck-boost converter plecs model schematic

B


Sine Wave
Compare to Constant
> 0
Carrier Signal 0-1
Comparator
>=
Sine wave 180 degree shifted
Comparator1
Rectified sine modulation
Modulation
Regular PWM signal for fixed output voltage
Signal inport from Simulink
Carrier Signal
Steppped boost or custom signal modulation
Pulse Boost1
Boost2
Switch OFF2
Switch ON2
Boost2 (1-D)
Switch2
Pulse Boost1/Boost2 (1-D)
Pulse Boost2
Boost1
Switch OFF1
Switch ON1
Boost1 (1-D)
Switch4
Pulse Boost2/Boost1 (1-D)
Battery Current1
Scope2
Probe
Scope12
Battery Current2
Scope1
Am2
Am1
Pulse Boost1/Boost2 (1-D)
ETD
Heat Sink
Pulse Boost2/Boost1 (1-D)
ETD2
Heat Sink3
Voltage Battery 1
Vm4
R1
C1
Voc1
Battery1
L1
C2
R2
Vm2
Voltage Battery2
Boost2 (D)
ETD1
Heat Sink1
Boost1 (D)
ETD3
Heat Sink2
Battery2
Voc2
C
Constant Voltage Battery1
Constant Voltage2
Soc_Updated1
f(u)
Voc vs SoC
65000
Initial charge in Coloumbs
Battery Current1
-1
invert
1/s
Coloumb couting
72000
Nom Capacity
Divide
100
%
Soc_Updated1
PWM Chopper
Pulse Boost1
Modulation
Switch
0
Switch_OFF
Manual Switch
Boost1 (D)
PWM Chopper1
Pulse Boost2
Switch1
Switch OFF
Manual Switch1
Boost2 (D)
Soc_Updated2
Voc vs SoC1
Voc2
Initial charge in Coloumbs1
Battery Current1
1
invert1
1/s
Coloumb couting1
72000
Nom Capacity1
Divide1
100
%1
Soc_Updated2

Hybrid h-bridge converter plecs model schematic

C


+ON/+OFF
Posstive Current ON/OFF
+Sine
0
+OFF
-ON/-OFF
Negative Current ON/OFF
-Sine
0
-OFF
+Sine
-Sine
NOT
Logical Operator
>= 0
Logical comparator
+ -
Modulation signal
Carrier Signal
S3
S4
NOT
Logical Operator4
+Chopping Pulse1
S44
S33
NOT
Logical Operator7
+Chopping Pulse2
probe
Probe
Probe1
S1
S2
NOT
Logical Operator3
Charge/Discharge- ON/OFF1
NOT
Logical Operator2
> 0
Compare to Constant
S11
S22
NOT
Logical Operator6
Negative Current ON/OFF2
NOT
Logical Operator5
> 0
Compare to Constant1
Inductor current 90 deg lagging from modulation signall
S3
S4
-ON/-OFF
+ON/+OFF
Q32
Q42
S33
S44
R3
Batt2
Q12
Q22
S11
S22
Q3
Q4
S3
S4
R2
Batt1
Q1
Q2
S1
S2
L1
S1
S2
+ON/+OFF
-ON/-OFF
C1
R1
V_dc4

Transistor data sheet D

IAUT260N10S5N019

OptiMOS™-5 Power-Transistor

AEC Qualified

RoHS

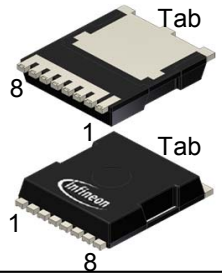
Product Summary

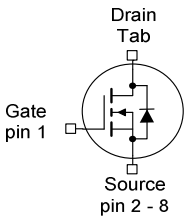
V_{DS}	100	V
$R_{DS(on)}$	1.9	mΩ
I_D	260	A

Features

- N-channel - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- Ultra low Rds(on)
- 100% Avalanche tested

P/G-HSOF-8-1





Type	Package	Marking
IAUT260N10S5N019	P/G-HSOF-8-1	5N10019

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25°C, V_{GS}=10V	260	A
		T_C=100 °C, V_{GS}=10 V[1)]	197	
Pulsed drain current[1)]	$I_{D,pulse}$	T_C=25 °C	1040	
Avalanche energy, single pulse[1)]	E_{AS}	I_D=130 A	400	mJ
Avalanche current, single pulse	I_{AS}	-	260	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	T_C=25 °C	300	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

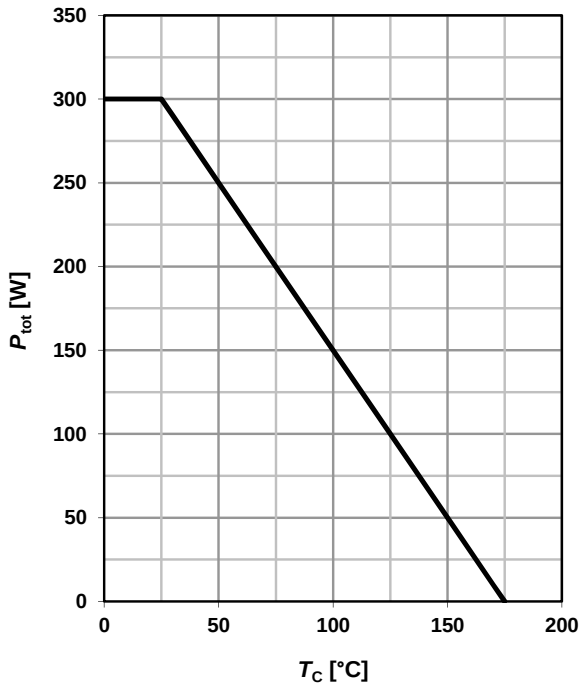
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics[1]						
Thermal resistance, junction - case	R_{thJC}	-	-	-	0.5	K/W
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=210 µA	2.2	3.0	3.8	
Zero gate voltage drain current	I_{DSS}	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=50 V, V_{GS}=0 V, T_j=85 °C[1]	-	1	20	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=6 V, I_D=75 A	-	2.0	2.5	mΩ
		V_{GS}=10 V, I_D=100 A	-	1.6	1.9	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[1]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz	-	9100	11830	pF
Output capacitance	C_{oss}		-	1462	1900	
Reverse transfer capacitance	C_{rss}		-	61	92	
Turn-on delay time	$t_{d(on)}$	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, R_G=3.5 Ω	-	21	-	ns
Rise time	t_r		-	11	-	
Turn-off delay time	$t_{d(off)}$		-	49	-	
Fall time	t_f		-	38	-	
Gate Charge Characteristics[1]						
Gate to source charge	Q_{gs}	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V	-	41	54	nC
Gate to drain charge	Q_{gd}		-	28	42	
Gate charge total	Q_g		-	128	166	
Gate plateau voltage	$V_{plateau}$		-	4.8	-	V
Reverse Diode						
Diode continous forward current[1]	I_S	T_C=25 °C	-	-	260	A
Diode pulse current[1]	$I_{S,pulse}$		-	-	1040	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=100 A, T_j=25 °C	-	0.9	1.3	V
Reverse recovery time[1]	t_{rr}	V_R=50 V, I_F=50A, di_F/dt=100 A/µs	-	80	-	ns
Reverse recovery charge[1]	Q_{rr}		-	180	-	nC

[1] Defined by design. Not subject to production test.

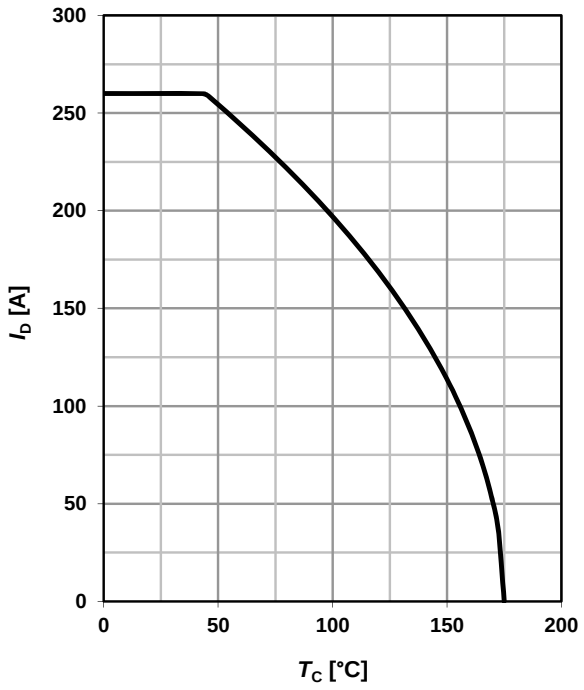
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



2 Drain current

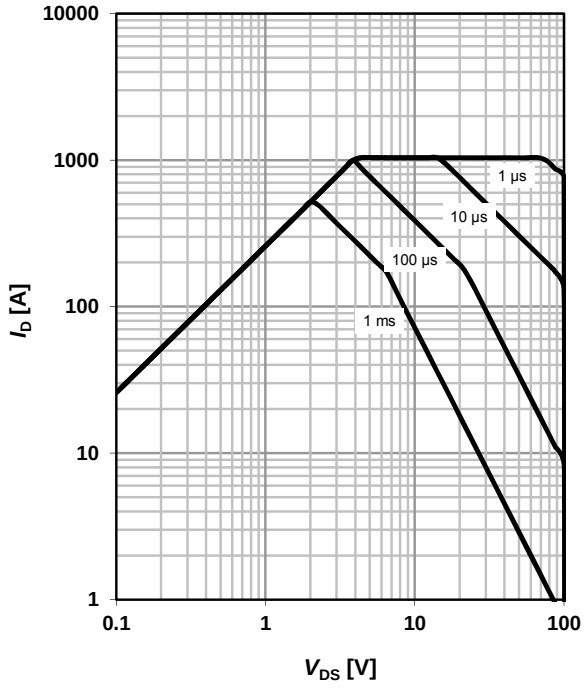
$I_D = f(T_C)$; $V_{GS} \geq 6$ V



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$

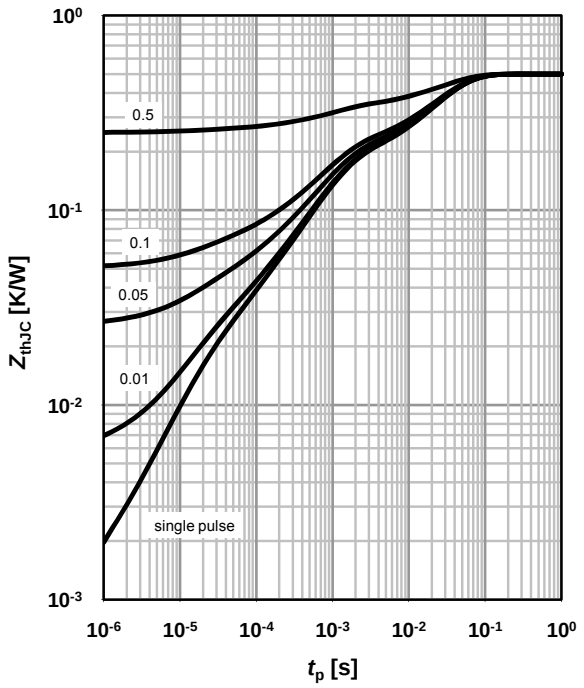
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

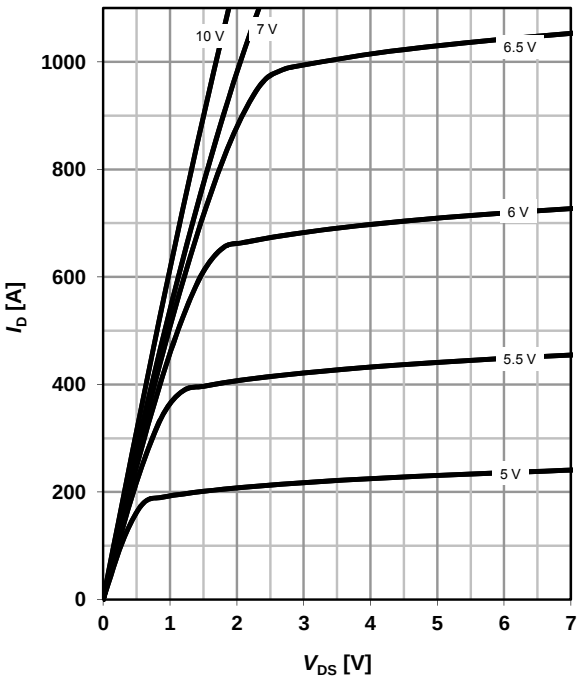
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C

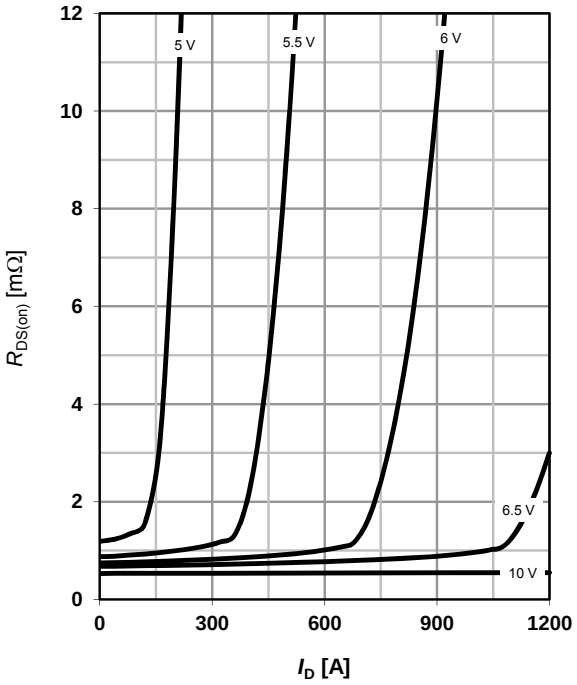
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = (I_D)$; $T_j = 25$ °C

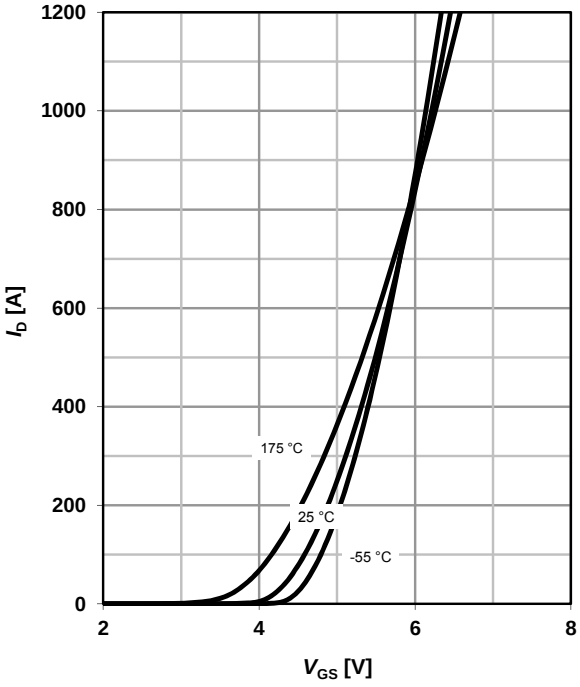
parameter: V_{GS}



7 Typ. transfer characteristics

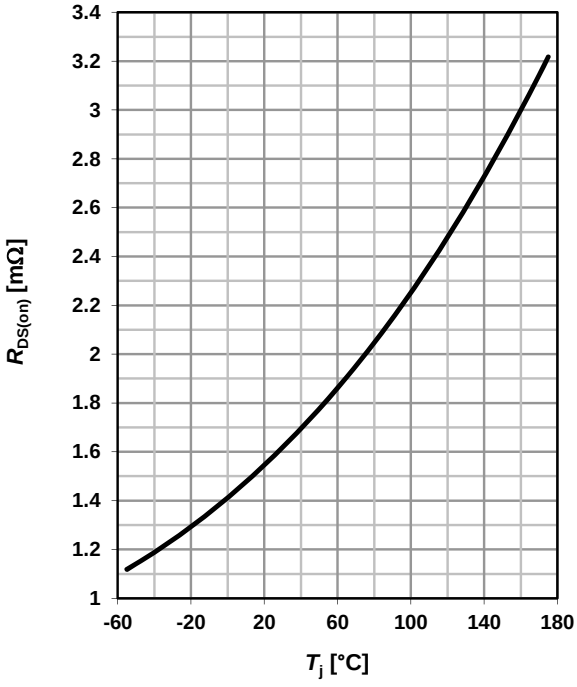
$I_D = f(V_{GS})$; $V_{DS} = 6$V

parameter: T_j



8 Typ. drain-source on-state resistance

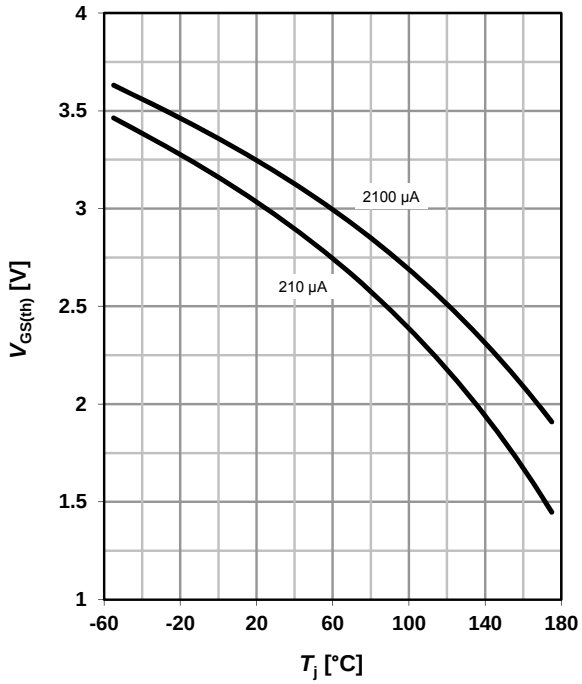
$R_{DS(on)} = f(T_j)$; $I_D = 100$ A; $V_{GS} = 10$ V



9 Typ. gate threshold voltage

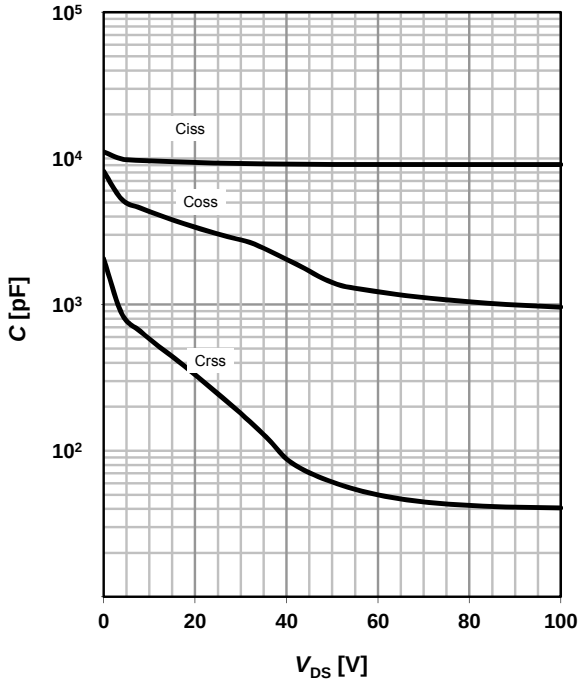
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

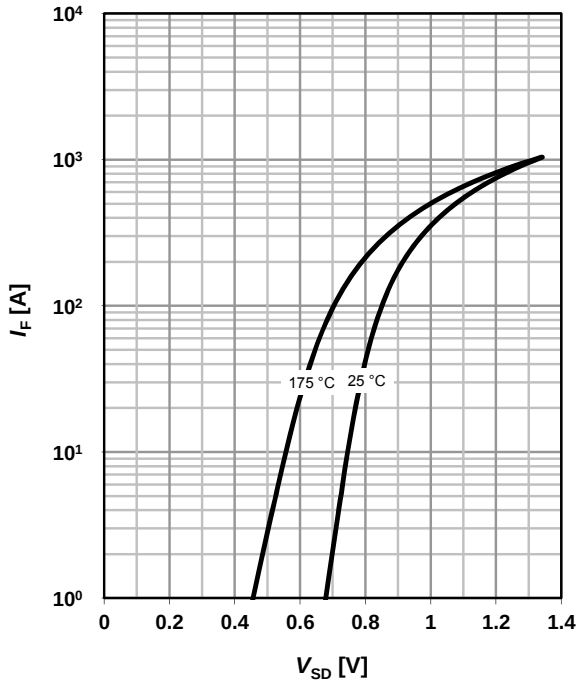
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristicis

IF = f(V_{SD})

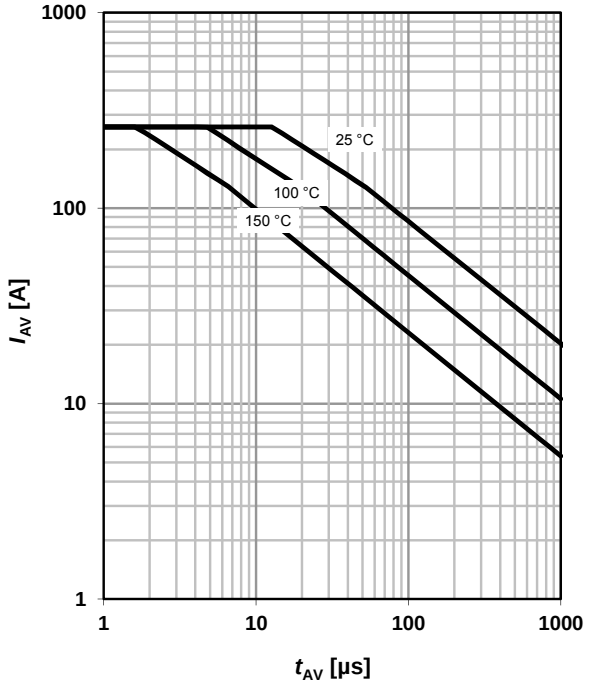
parameter: T_j



12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$

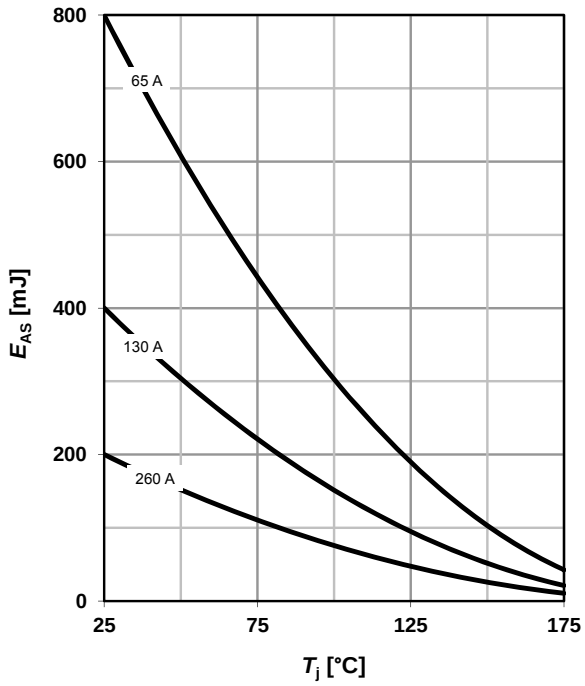
parameter: $T_{j(start)}$



13 Typical avalanche energy

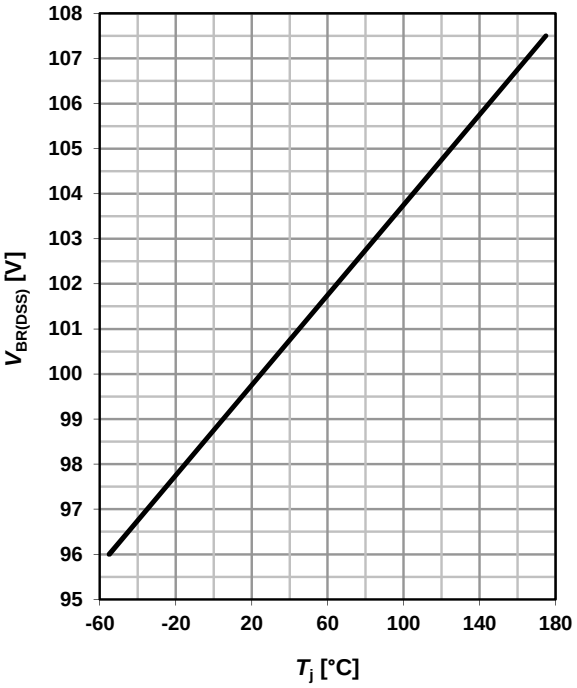
$E_{AS} = f(T_j)$

parameter: I_D



14 Drain-source breakdown voltage

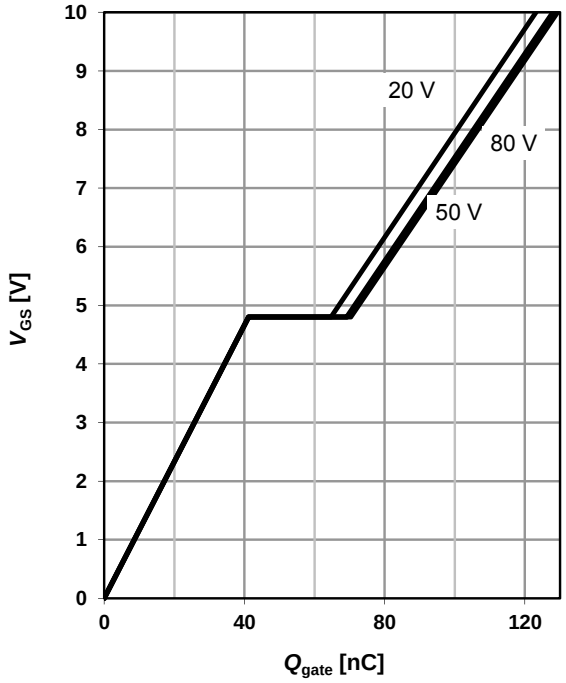
$V_{BR(DSS)} = f(T_j)$; I_{D_typ} = 1 mA



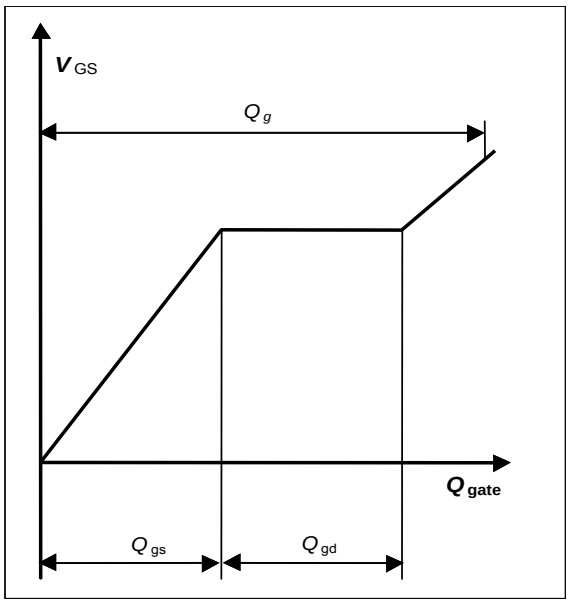
15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; I_D = 100 A pulsed

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Version 1.0	2017-10-02	Final Data Sheet