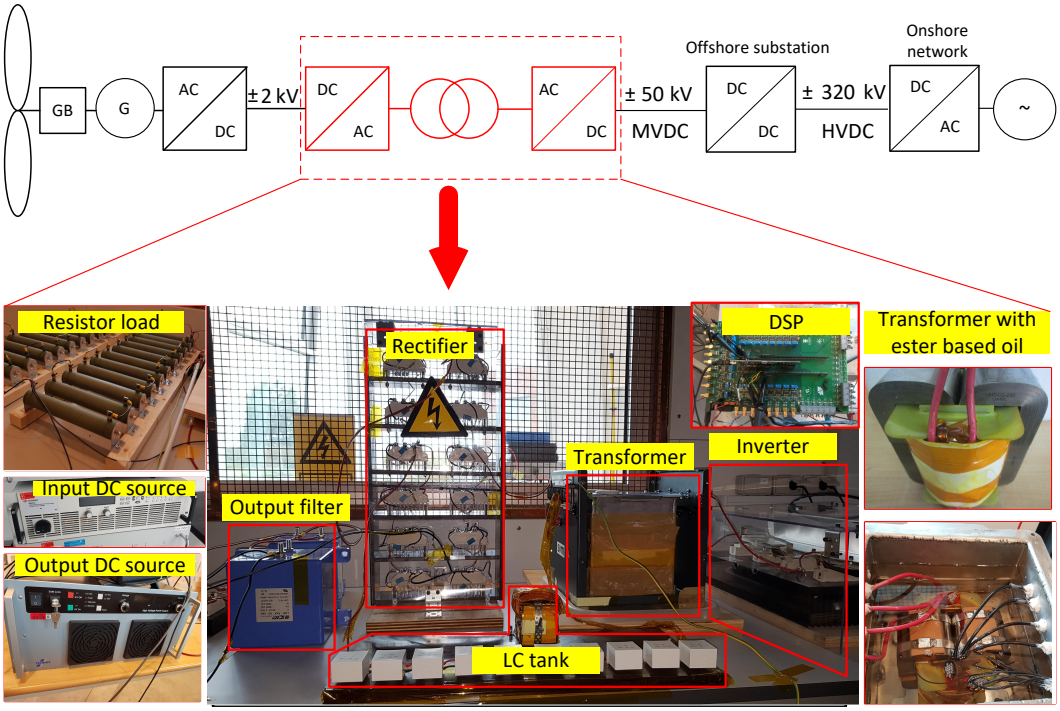
Impact of Turbine Converter Control on Wind Farm with DC Collection Grid



Master thesis report

WPS4-1050

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Abstract:

This thesis presents a control strategy for a DC/DC resonant converter for offshore WT application. The main objective is to obtain fast and accurate power tracking. The control architecture is based on a feedforward developed by linearization of the power to frequency equations. The method used contains an algorithm that obtains the right switching frequency from a look-up table in order to follow the reference power. Results obtained by simulation on a lossless 10MW converter show a good performance on the whole operating range during power and output voltage steps. Moreover, the controller is able to reject output voltage harmonics and has a proper set-point tracking bandwidth. The validation of the control structure is performed on a 10kW and 5kV output voltage laboratory setup. Experimental results reflect a favorable matching but arise further issues such as: proper MV measurement, non-idealities and output choke impact. Furthermore, the need of a low gain compensator in parallel is necessary to avoid steady-state error when the resolution of the feedforward is reduced.

Contents

List of Figures

List of Tables

Glossary

α, β	Conducting space angles	[rad]
ω_c	Crossover angular frequency	[rad/s]
ω_r	Resonant angular frequency	[rad/s]
ω_{rs}	Ratio between resonant and switching angular frequency	[rad/s]
ω_s	Switching angular frequency	[rad/s]
C_f	Filter capacitance	[F]
C_r	Resonant tank capacitance	[F]
$D_{5,6,7,8}$	Diodes of the rectifier	[–]
FF	Feed forward	[–]
$FF + PI_{GS}$	Feed forward with gain schedulling PI	[–]
$FF + PI_K$	Feed forward with constant PI	[–]
f_r	Resonant frequency	[Hz]
f_s	Switching frequency	[Hz]
f_{sw_op}	Operating point switching frequency	[Hz]
f_{sw_ss}	Small signal switching frequency	[Hz]
G_{plants}	Transfer function of the plant	[A/Hz]
i_n	Output filter current	[A]
k_f	Slope on the frequency axis	[W/Hz]
k_v	slope on the voltage axis	[W/V]
I_o	Output rectifier current	[A]
$I_{o,avg}$	Averaged output rectifier current	[A]
i_r	Resonant tank current	[A]
L_f	Filter inductance	[H]
L_m	Magnetizing inductance	[H]
L_r	Resonant tank inductance	[H]
N_1	Number of winding turns on the primary side of transformer	[–]
N_2	Number of winding turns on the secondary side of transformer	[–]
P_{base}	Linearized power on the voltage aixs	[W]
P_{lin}	Base power points	[W]
P_o	Output power	[W]
P_{ref}	Reference power	[W]
q	Tank capacitor charge	[C]
R_c	Filter capacitor resistance	[Ω]
R_L	Filter inductor resistance	[Ω]
$T_{1,2,3,4}$	Switches of the inverter	[–]
T_r	Resonant period	[s]
$T_s = T_{sw}$	Switching period	[s]
$V_c = V_{cr}$	Tank capacitor voltage	[V]
V_g	Primary transformer voltage	[V]
V_g'	Secondary transformer voltage	[V]
V_{LVDC}	Low DC voltage	[V]
V_{MVDC}	Medium DC voltage	[V]
V_o	Output rectifier voltage	[V]
Z_r	Resonant impedance	[Ω]

Chapter 1

Introduction

The demand of renewable energy sources for the future has increased the number of WTs installed across the globe as reflects the IEA [1]. Currently, the majority of WPP are placed onshore, however, offshore wind farms have rapidly grown in the recent years [2]. The main advantages for it are high and stable wind speeds, enabling the use of larger WTs compared to those commonly used on inland. Moreover, the distance of offshore WPP's from land and the freedom from constructional obstacles allow the development of wind farms with higher number of turbines than onshore WPP's [3].

On the other hand, there are technical challenges about how to deliver the energy to the onshore network. Traditional HVAC transmission systems have higher costs as power level and distance to the onshore network increase compared to HVDC, according to some studies in [4] and [5]. In addition, as an improvement for HVDC submarine cables with MVAC collection grid used in some farms, MVDC collection grids could reduce material costs and increase efficiency [6].

Following the purpose of installing a MVDC collection grid, a DC/DC converter to step up the voltage with high turns ratio is needed. High availability, efficiency and power density are all targets for an offshore WT converter. For these requirements a resonant converter for DC WT could fill the gap as this design paper introduces [7]. Instead of using resonant converters with a hard switching topology as in [8], this thesis analyses a new resonant converter being investigated at Aalborg University [9] [10].

This converter, called SRC#, differs from typical series resonant converters by placing the resonant LC tank from the primary side of the transformer to the secondary side. The converter is operated with a novel method of operation, entitled pulse removal technique, characterized by variable frequency and phase shift modulation in the subresonant region [7]. This mode of operation reduces the transformer size by 50% while losses are kept below 1.5% from zero to nominal power, due to soft-switching characteristics [11].

The main interest of the DC/DC converter for WT applications is power and input DC link voltage control to allow working on the MPPT of the generator and avoid component stress during output voltage fluctuations. Therefore, variable frequency control is needed. This thesis focuses on the design and impact of the close control for this converter topology on a 10MW converter simulation model and the validation of it on a scaled-down setup of 10kW and 5kV output voltage located in [12].

1.1 Problem Formulation

As there are still many uncertainties regarding control and design of a wind farm with DC collection network, beside the impact of converter topology on efficiency, bill of materials and others, it's crucial to determine the impact of DC/DC converter control during steady state, set-point tracking bandwidth and dynamic operation. The performance on the MV side DC link during output voltage harmonics, output voltage steps and output voltage sag are also important factors to consider. The main objective of this project is to design, implement and test an optimal control for this particular converter that is able to achieve fast and accurate power tracking.

1.2 Thesis structure

The structure of this thesis is as following:

- Chapter 2 presents the converter mode of operation and conduction modes that occur under different conditions. Following, the steady state operation power equations are derived from it.
- Chapter 3 explains the design procedure for the feedforward control block and its laboratory implementation. Afterwards, the small signal model of the SRC# is introduced and the design criteria for the PI tuning process.
- Chapter 4 shows the controller performance under different tests by simulation on the 10MW lossless converter such as: Steady-state error, set-point tracking bandwidth, power steps, output voltage steps, output voltage disturbances and output voltage sags.
- Chapter 5 validates the controller performance under different tests by a laboratory implementation and simulation on a 10kW scaled-down converter.
- Chapter 6 exposes the discussion based on the results obtained with different scenarios and controllers. Finally, Chapter 7 explains the conclusions of this thesis.

1.3 Case Study

As mentioned in the introduction, HVDC collection could have great advantages compared to HVAC collection, however, this technology is still immature and many aspects are required to be analyzed such as high-power DC circuit breakers and high-power DC/DC converters topologies together with a control system that fulfill steady-state and dynamic requirements. [6]

In Figure 1.1 the structure of the DC collection grid is represented. A cluster of DC wind turbines feed energy into the MVDC $\pm 50kV$ with submarine cables through a DC/DC converter that steps up the voltage. The off-shore substation is the responsible of maintaining constant the MVDC voltage on the $\pm 50kV$ side, which is then elevated to HVDC $\pm 320kV$ to an eventual DC/AC onshore substation that is connected into the main supply grid.

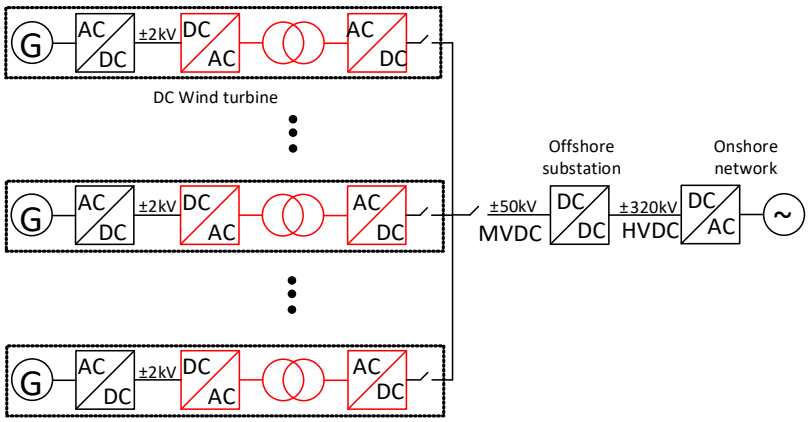


Figure 1.1: Cluster of DC wind turbines connected to a $\pm 50kV$ MVDC collection

The SRC# is composed by a controlled LV inverter, a medium-frequency transformer, a resonant LC tank, a passive MV rectifier and, an output filter, see Figure 1.2. The SRC# is responsible of controlling the input DC link by sending the right power reference. Voltage and current are input signals being fed into the control, and the output of it is a variable switching frequency.

The controller is tested on an electrical simulator for the real 10MW application and on a 10kW laboratory setup for the validation. Specifications of each case are represented in Table 1.1.

Table 1.1: Operating condition of the 10 MW converter model and the scaled down 10 kW setup

	$P_{nominal}$	f_{sw}	V_{in}	V_{out}
Electrical circuit simulator (Plecs)	10 MW	[0-1000] Hz	4 kV	100 kV
Laboratory setup	10 kW	[0-1000] Hz	500 V	5000 V

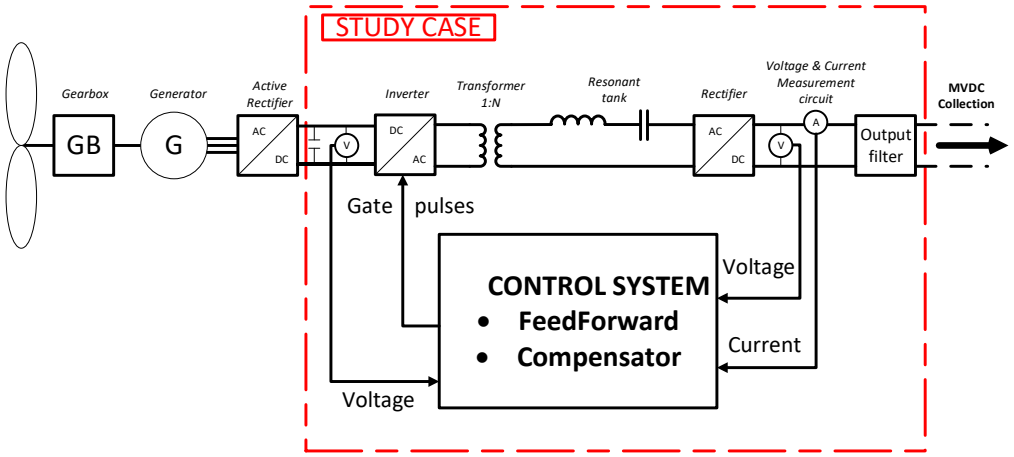


Figure 1.2: System of the study case

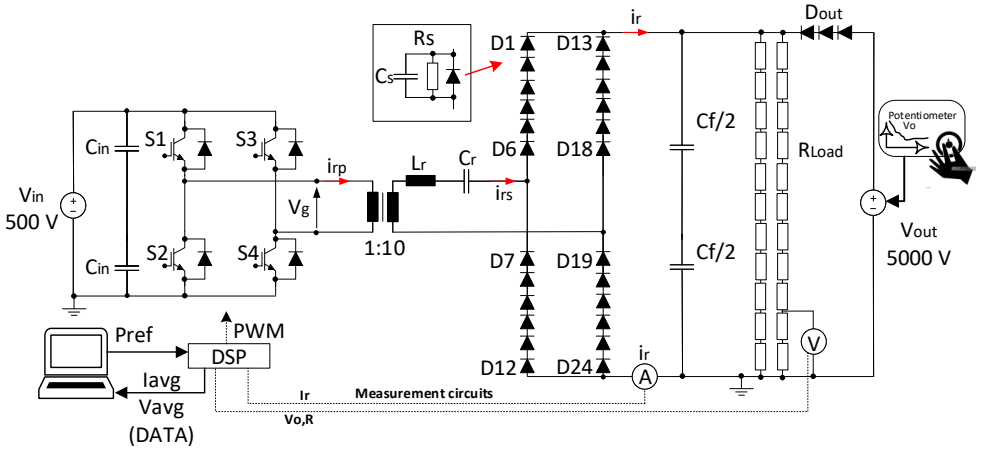


Figure 1.3: Laboratory setup components

The study case of the laboratory setup in Figure 1.3 is composed by:

- Input DC voltage source with grounded outlet
- Two input filter capacitor connected in series
- An inverter assembled with four controlled IGBT modules
- An oil insulated medium-frequency transformer with grounded case.
- A resonant tank composed by an inductor in series with a capacitor.
- A rectifier composed by 12 diodes per leg, each having a RC voltage balancing circuit connected in parallel.

- An output DC voltage source grounded by the outlet

Other related laboratory details can be found in Appendix A.

1.4 Project Limitations

- The whole turbine system is not implemented in the laboratory setup. Therefore, an input DC voltage source is employed to simplify the emulation of the blades, gearbox and, generator.
- An output DC voltage source is used to emulate the MVDC network, considering the off-shore substation responsible for keeping the voltage constant.
- The design of the converter for 10MW specifications was provided.
- The scaled-down 10kW laboratory setup placed in MV laboratory, at Aalborg University, was already built and designed. In section B.1 the laboratory limitations for the particular test are explained.

1.5 Scope of Work

- Understanding of the converter design, operation, conduction modes, power flow analysis and small signal analysis.
- Design, implementation and test of a control system on an ideal lossless converter for 10MW application on an electrical simulator.
- Characterization of a 10kW and 5kV output voltage laboratory setup including nonideal components, measurement circuits, modulator and A/D conversion.
- Implementation, validation and test of the control technique , on the laboratory setup and on an electrical simulator.
- Evaluation, discussion and future work proposal based on the obtained results.

Chapter 2

Converter Model for SRC#

First, this chapter presents the SRC# operation principle: the pulse removal technique. It is explained how the pulses are generated and for which purpose. After, the conduction modes and current shape, that derive from the operation conditions, are briefly explained. Finally, the power flow equations used from 0 to 1pu output power in DCM region and CCM are presented.

2.1 Converter Operation and Conduction Modes

The condition under which the resonant converter presented in chapter 1 is operating is in the sub-resonant region $f_{sw} < fr$. The reasons behind it, presented in [13], are ZCS for switches in the V_{in} LV side (IGBT's) and on the V_{out} MV side (line frequency diodes) which result in lower switching losses.

The pulse removal technique consists on applying the same V_{in} pulse length on the transformer regardless of the switching frequency, as a consequence of a constant phase shift. As a result, by controlling the number of pulses, switching frequency, the output power can be controlled. The switches pair S1/S2 (leading leg) and S3/S4 (lagging leg), in Figure 2.1 a), operate at constant duty cycle, set at 50%. The phase shift is applied between the leading leg (S1/S2) and lagging leg (S3/S4), with a duration of half the LC tank resonant period. In this way the ZCS is achieved since the operating frequency f_{sw} is always lower than the resonant f_r. The resultant applied voltage to the transformer at different switching frequencies is shown in Figure 2.1 b) (black line). When the input voltage is applied a resonant cycle on the current (red line) occurs and turns off naturally before the applied voltage is finished. As it can be observed, the magnetizing current (blue line) is symmetric in all frequency range due to 50% duty cycle.

With the pulse technique mentioned above, the transformer is excited with V_{in} when S1/S2 are conducting followed by a zero period when S1 is ON and S3 turns off. This excitation of the transformer is mirrored when S2 and S4 are conducting,

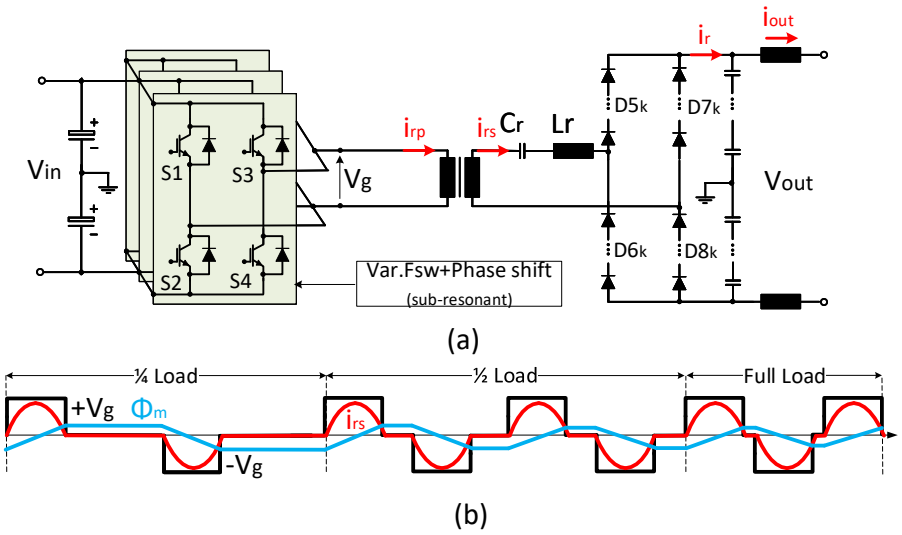


Figure 2.1: a) Structure of the SRC# b) Applied voltage on the secondary side of the transformer (black), secondary current (red) and magnetizing current (blue). Increase of switching frequency, increase number of pulses and, as a result, increase of the output power

followed by S4 turn off. In this way, symmetry is achieved, avoiding saturation of the transformer. The conduction modes that result with this operation of the converter are four:

- DCM1. Occurs in the entire range between 0 to f_r when after a resonant cycle "T1", the capacitor voltage V_{cr} in the resonant tank is lower than the output voltage and therefore a zero period "X" appears until the next resonant cycle is applied Figure 2.2 a).

- DCM2. Occurs when the voltage across the capacitor of the LC tank V_{cr} after a resonant cycle "T1" is higher than V_{out} and starts to get discharged in period "Q1". However, the frequency range where it happens is $0 < f_{sw} < f_r/2$ as two complete half resonant cycles are not possible above $f_r/2$ and therefore it can be observed a zero period "X" only in this range Figure 2.2 b).

- CCM1-Hybrid. Following the description of DCM2, when the voltage across the capacitor is higher than V_{out} after a pulse is applied, and in the frequency range $f_r/2 < f_{sw} < f_r$, the resonant cycle "Q1" will not finish before "T2" period starts, therefore the resonant cycle "T1/T2" start from a non-zero current Figure 2.2. c)

- CCM1. When having sufficient ΔV between input and output and at high frequency, the capacitor voltage after a resonant cycle will eventually become $V_{cr} > V'_{in} + V_{out}$, then another conduction period will appear after the

zero current crossing during a resonant cycle, called "D1" where the resonant capacitor starts to get discharged when the input voltage is still applied followed by the "Q1" period described by CCM1-Hybrid. Figure 2.2 d)

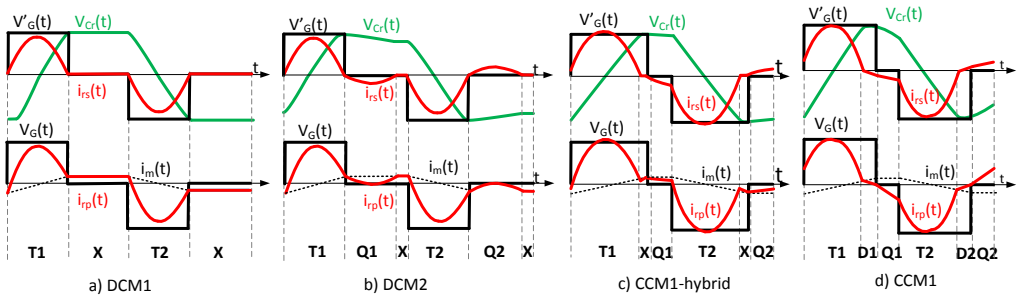


Figure 2.2: Conduction modes of the SRC#. Top figures: reflected input voltage V'_G (black), capacitor voltage V_{cr} (green), secondary current i_{rs} (red). Bottom figures: input voltage V_G (black), primary current i_{rp} (red), magnetizing current i_m (dashed black)

Further details regarding the choice of operating conditions, details on the subintervals for conduction modes and equivalent circuits are explained on [13].

As a summary, the chosen mode of operation has the characteristics in Table 2.1 which have to be considered for the controller design in the next chapters. The switching frequency as a control variable will imply that the controller has to be designed in a proper manner to be able to work in the linear region of DCM and non-linear region of CCM. Furthermore, the consideration of ΔV as another factor of conduction mode boundary variable has to be taken into account.

Table 2.1: Converter operation characteristics based on the design of the IGBT's pulses

Characteristic	Value	Reason
Variable switching frequency	[0-1000Hz]	Control the number of pulses in order to control the output power
Constant phase shift	$1/(2 \cdot f_r)$	Allow the resonant cycle to have a ZCS in all operating range
Constant duty cycle	0.5	Achieve symmetry on voltage and currents, especially the magnetizing current

2.2 Steady State Operation

DCM

When considering the power equations for the DCM region, the area of the current during a switching interval has to be analyzed. This can be performed by looking at the charge on the capacitor q which is charged by the tank current during a half cycle in Equation 2.1.

$$I_{out} =< |i_r| >_{T_s} = 2 \cdot q \cdot f_{sw} \tag{2.1}$$

The output current is then related to the resonant capacitor charge. At the peak current of the capacitor, its charge is related with capacitor voltage as following:

$$q = 2 \cdot C_r \cdot V_{Cr} \tag{2.2}$$

It can be then described the output current average in relation to the capacitor voltage:

$$i_{out} = 4 \cdot C_r \cdot V_{Cr} \cdot f_{sw} \tag{2.3}$$

Therefore, by knowing that the voltage across the capacitor is equal to the output voltage after a resonant cycle "T1" for DCM1, and, after the "Q1" period for DCM2, it can be derived the power flow equation as:

$$P_{out} = V_{out} I_{out} = 4 \cdot f_{sw} \cdot C_r \cdot N \cdot V_{in} \cdot V_{out} \tag{2.4}$$

As shown in the Figure 2.3, the relation between output power and frequency is linear in the DCM region and its valid for both DCM1 and DCM2. Moreover, regarding DCM2, when V_{out} decreases, the averaged current after a switching cycle remains constant but since the output voltage is lower the output power decreases linearly.

CCM1-Hybrid

As described in section 2.1, when there is a voltage difference between V'_{in} and V_{out} and the switching frequency is higher than half of the resonant frequency, in the conduction period "Q1" the secondary current does not cross zero, so the resonant cycle starts from a non-zero current. Due to this fact the power flow analysis needs to be performed differently looking at the state variables value at the end of each conduction interval.

The mathematical model describing the equations at each conduction interval for CCM1-hybrid is explained in Appendix C and is developed through discrete time modelling. From the state space model of the SRC# it can be seen that the output current i_{out} becomes a non-linear function of some state variables shown in Equation C.19. Therefore, a linearization need to be performed in order to evaluate the equations.

In [14] the state plane analysis methodology was applied to develop an expression to obtain the operating points for the state variables. This derivation is shown section C.2, where it can be obtained the voltage across the capacitor shown in Equation 2.5 and current on the inductor Equation C.47 at the end of each switching interval. Both inductor current and capacitor voltage initial conditions at the beginning of each conduction period, increase with the switching frequency which result in a higher current that is not linear.

$$V_{Cr,1(k)} = \frac{V_g \cdot V_o \cdot [1 + cos((2 - \omega_{rs})\pi)]}{2V_o - V_g \cdot [1 - cos((2 - \omega_{rs})\pi)]} \tag{2.5}$$

Where $\omega_{rs} = f_r / f_{sw}$.

Since the output current can be approximated at its mean value due to the filter inductor, it can be related the charge on the capacitor in each event to the peak value of the capacitor voltage in Equation 2.6:

$$Io = 4 \cdot C_r \cdot V_{Cr,1(k)} \cdot f_s \tag{2.6}$$

Finally, after having the equation of the output current depending on the capacitor voltage, the output power for CCM1-Hybrid can be described as:

$$P_{out} = V_{out} \cdot I_{out} = 4 \cdot C_r \cdot f_s \cdot \frac{V_g \cdot V_o \cdot [1 + cos(2 - \omega_{rs})\pi)]}{2V_o - V_g \cdot [1 - cos((2 - \omega_{rs})\pi)]} \tag{2.7}$$

The relation between power and frequency for CCM1 becomes more non-linear than CCM1-Hybrid since another conduction period appears. The power to frequency relation in this conduction mode is derived in [13] but is not used in this thesis since its high non-linearity make it not favourable to operate with.

In Figure 2.3 the curves relating output power and frequency for different ΔV are represented. The black line shows the DCM1 curve when $\Delta V = 0\%$ from

0 to 1pu output power. It can be clearly seen that if the voltage difference increases, the power delivered at the DCM2 region (light green) and at the begining of CCM1-Hybrid (blue) is lower than the DCM1. However, as the switching frequency approaches nominal values, when ΔV increases so does the output power at the end of CCM1-Hybrid region reaching higher values than DCM1. In order to reach nominal power it is not necessary to operate at the CCM1 region and therefore it is not needed to included in the converter model.

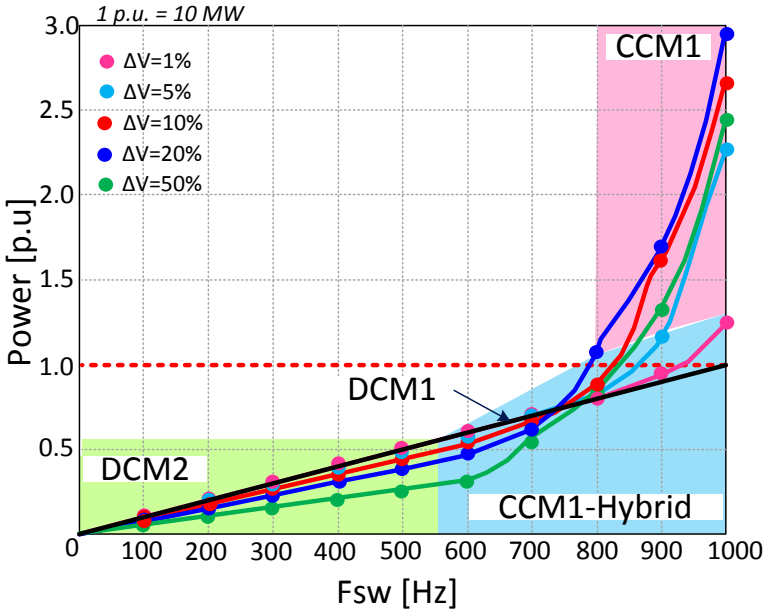


Figure 2.3: Relation between switching frequency and output power at different ΔV

Chapter 3

Converter Control Design

In this chapter is presented the control strategy implemented for this converter's topology. Two different control systems have been analyzed. First, a FeedForward (FF) controller, see section 3.1. Then, due to variable switching frequency operation of the converter, the same FF controller is implemented with a gain scheduling PI controller that varies its gain values along the switching frequency.

The power control requirements followed for the design of the implemented controllers are of qualitative nature. A fast and accurate power tracking is required during different case scenarios. Moreover, the least impact of the implemented controllers on the MVDC network is required such as, good output voltage harmonics rejection and optimal performance during output voltage sags on the MVDC collection.

3.1 Feedforward design

The feedforward implemented for this converter's topology is designed to give a proper switching operating frequency to the modulator for power control of the converter. In this way, the desired reference power (P_{ref}) can be delivered to the grid at a specific operating point defined by the voltage difference between V_{in} and V_{out} .

Without considering the operation in CCM1-hybrid, it can be seen in Figure 2.3 that in DCM operation there is a linear relationship between power and the input variables (f_{sw}, V_{out}, V_{in}). So, the FF during DCM operation can be designed directly from the power equation Equation 2.1, with frequency as output, see Equation 3.1.

$$f_{sw,FF,DCM} = \frac{P_{ref}}{4 \cdot N \cdot Cr \cdot V_{in} \cdot V_{out}} \tag{3.1}$$

However, due to the complexity and non-linearity of the analytical equations during CCM1-hybrid operations (Equation 2.7), it is challenging to implement an

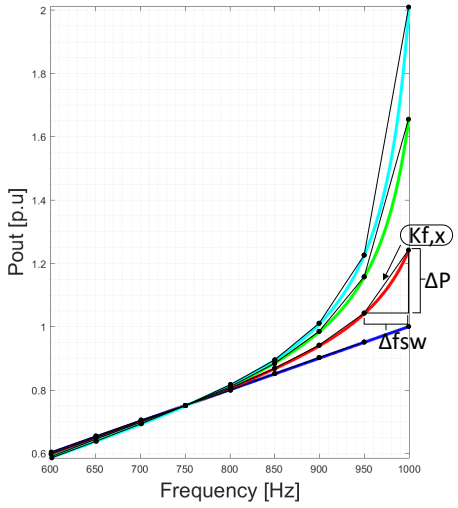
inverse function for the FF that relates back switching frequency from power, output voltage and input voltage levels. Therefore, the FF is generated by linearization of the power curves obtained from state plane analysis of the analytical equations CCM1-hybrid operations, see section 2.2.

The FF has been designed with search algorithm on a 2D look-up table generated from the linearization of the power curves during CCM1-hybrid. The operating conditions of the FF are presented in Table 3.1.

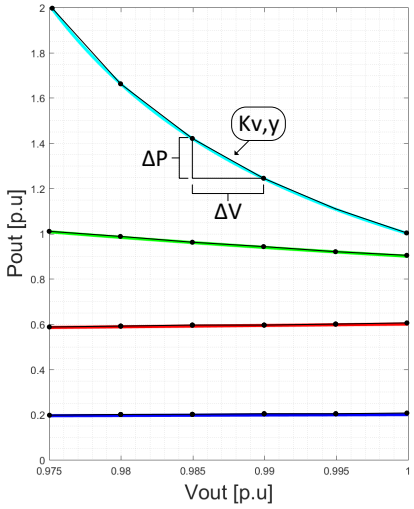
Table 3.1: Operating conditions of the linearized FF implemented in the ideal 10 MW converter

	f_{sw} [Hz]	V_{out} [kV]	V_{base} [kV]	P_{base} [MW]
Ideal	[600-1000]	[97.5-100]	100	10

As example, in Figure 3.1a is depicted the linearization of the power curves at four different output voltage levels. In Figure 3.1b is also illustrated the power curves' linearization along the output voltage at four different operating switching frequencies.



(a) Linearization of power curves along the switching frequency
Blue: $V_{out} = 1$ p.u Red: $V_{out} = 0.99$ p.u
Green: $V_{out} = 0.98$ p.u Cyan: $V_{out} = 0.975$ p.u



(b) Linearization of power curves along the output voltage
Blue: $f_{sw} = 600$ Hz Red: $f_{sw} = 750$ Hz
Green: $f_{sw} = 900$ Hz Cyan: $f_{sw} = 1000$ Hz

The variables of this linearization used for controller in the FF search algorithm are:

- $P_{lin}[x, y]$: a matrix of power levels in the linearization points of the power curves, see black dots in Figure 3.1a and Figure 3.1b

- $f_{sw,lin}[x]$: a vector of switching frequencies defined by the linearization steps along the switching frequency direction, x axis in Figure 3.1a
- $V_{out,lin}[y]$: a vector of output voltage levels defined by the linearization steps along the output voltage direction, x axis in Figure 3.1b
- $Kf,x[y]$: a vector of slopes along the switching frequency for each linearization step, see straight black lines in Figure 3.1a. One vector for each output voltage linearization level.
- $Kv,y[x]$: a vector of slopes along the voltage difference for each linearization step, see straight black lines in Figure 3.1b. One vector for each switching frequency linearization level.

Where x and y represent the different indexes for each segment of the linearized power curves, see Figure 3.1a and Figure 3.1b. The x is the index along f_{sw} and, y is the index along V_{out}.

In particular, Kf,x and Kv,y are calculated by simple linear equations:

$$Kf,x = \frac{\Delta P}{\Delta f_{sw}} \tag{3.2}$$

$$Kv,y = \frac{\Delta P}{\Delta V} \tag{3.3}$$

Meanwhile, P_{lin}, $f_{sw,lin}$ and, $V_{out,lin}$ are obtained directly from the ideal power curves.

In order to have a better idea of the working principle of the FF search algorithm, a 3D plot of the power curves along the switching frequency and the output voltage is depicted in Figure 3.2.

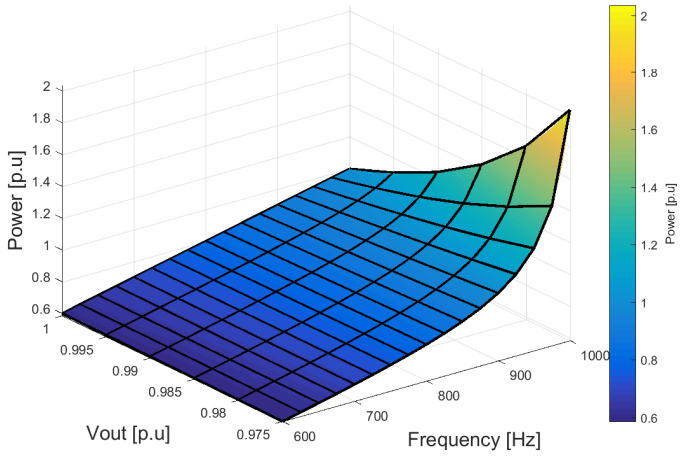


Figure 3.2: Linearization of power curves for the implementation of the Feedforward
Colored surface: Ideal power curves every 20 V difference
Black lines: Linearized power curves every 25 Hz and 500 V linearization steps

The figure shows the surface obtained from the power curves generated and its linearization.

In Figure 3.2, Kf, x and Kv, y are the slopes of the black lines along f_{sw} and V_{out} respectively. Meanwhile, the matrix P_{lin} is depicted as the cross point between the black lines in Figure 3.2. Each line that varies with the frequency is at one specific constant operating output voltage. On the other hand, each line along the output voltage axis is at constant frequency. Therefore, the linearized map presented in Figure 3.2 is composed by power curves at constant frequency and, power curves at constant output voltage.

The operating principle of the FF search algorithm is based on an iterative search along first, the output voltage then, the linearized power levels. In this way, the power area where P_{ref} resides can be found, see Figure 3.3. Finally, knowing all the four points and slopes of the area, the exact f_{sw} is calculated and given to the modulator for power-frequency converter control.

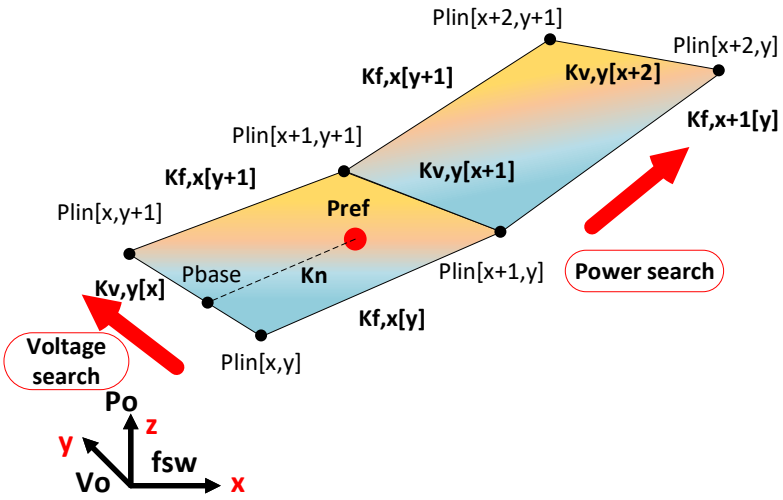


Figure 3.3: Zoomed view of Figure 3.2 for the implementation of the feedforward control and search algorithm principle

The equations Equation 3.4, Equation 3.5 and Equation 3.6 are used in the search algorithm, and its operating principle is explained in the following diagram, see Figure 3.4.

$$P_{base} = P_{lin}[x, y] + (V_{out} - V_{out,lin}[y]) \cdot Kv, y[x] \tag{3.4}$$

$$Kn = Kf, x[y] + \frac{V_{out} - V_{out,lin}[y]}{V_{out,lin}[y+1] - V_{out,lin}[y]} \cdot (Kf, x[y] - Kf, x[y+1]) \tag{3.5}$$

$$f_{sw} = f_{sw,lin}[x] + \frac{P_{ref} - P_{base}}{Kn} \tag{3.6}$$

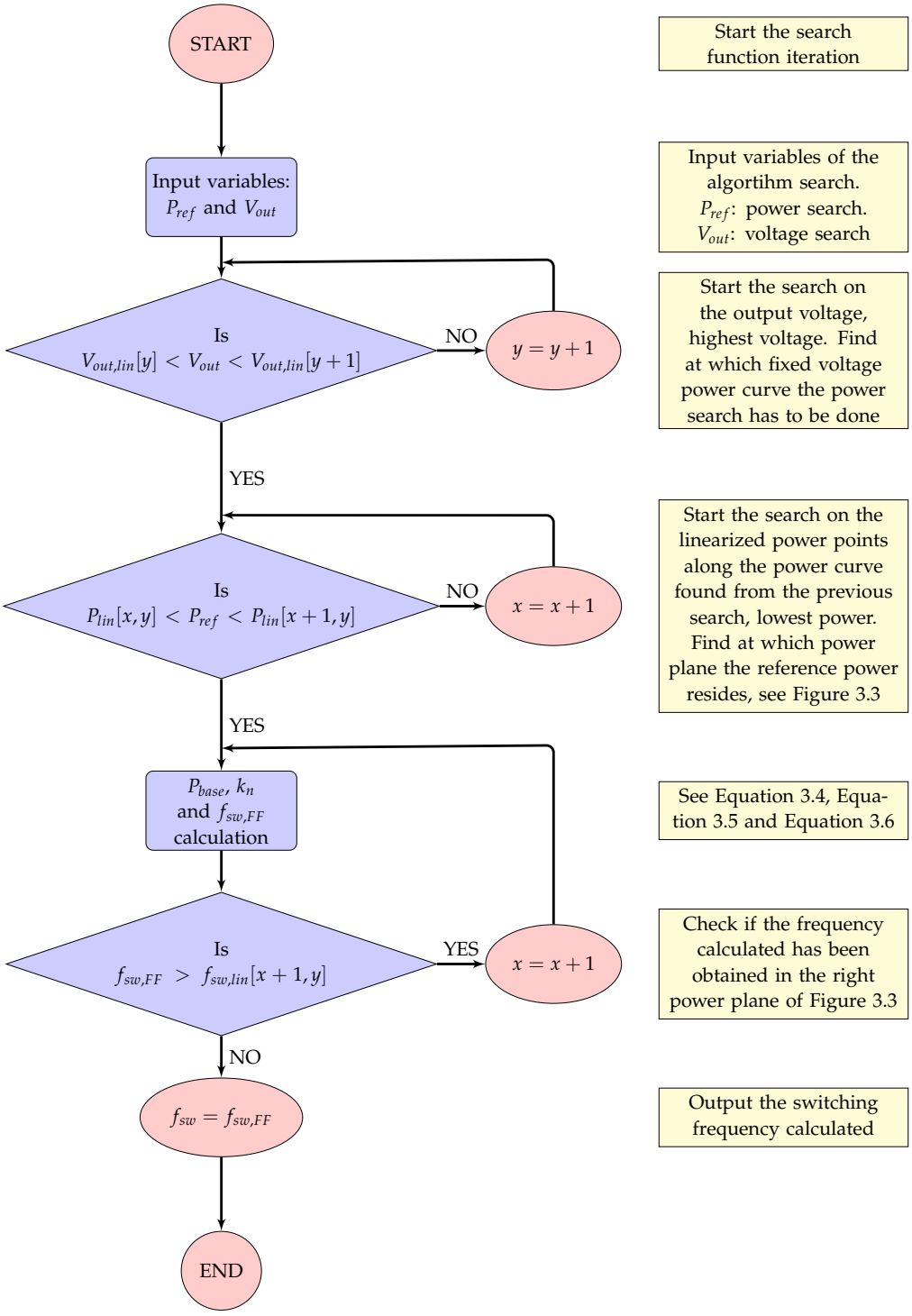


Figure 3.4: FF search algorithm working principle

3.1.1 Laboratory implementation

The implementation of the FF in the laboratory is slightly different from the ideal one, basically due to difficulties on obtaining the analytical equations of a real setup that generate the necessary power curves and take into account all the non-idealities and uncertainties. The power curves used by the FF controller have been obtained by experimental data, see Appendix B.

The obtained power curves and the generated surface for the FF implemented in the laboratory is shown in Figure 3.5.

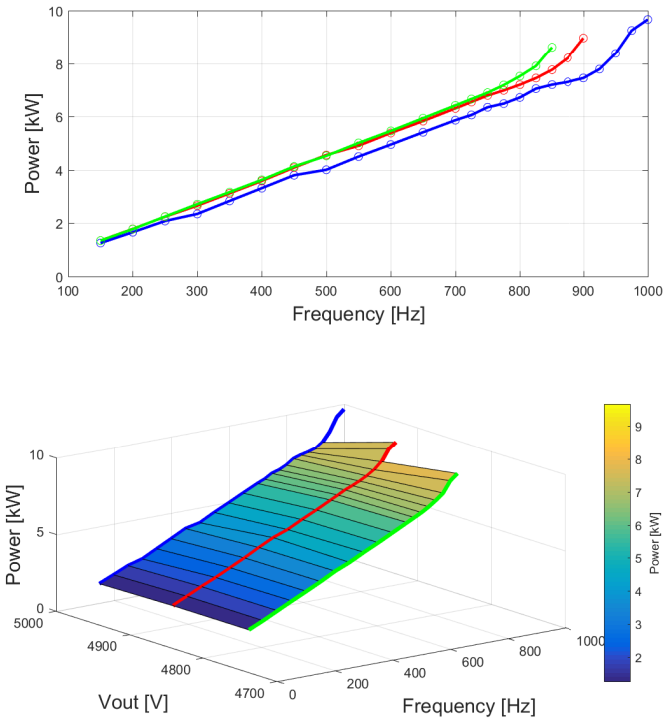


Figure 3.5: Experimental power curves (top) obtained at three different output voltage levels. Generated power surface for the implementation of the FF in the laboratory (bottom). Blue: 5000 V, Red: 4900 V, Green: 4797 V.

Therefore, the boundary operating conditions of the FF implemented in the laboratory setup are presented in Table 3.2.

Table 3.2: Operating conditions of the FF implemented in the 10 kW laboratory setup

	f_{sw} [Hz]	V_{out} [V]	P_{max} [W]
Laboratory	[0-1000]	[4797, 4900, 5000]	[9005, 9334, 9665]

Finally, the block diagram representing the converter and the FF controller is illustrated in Figure 3.6.

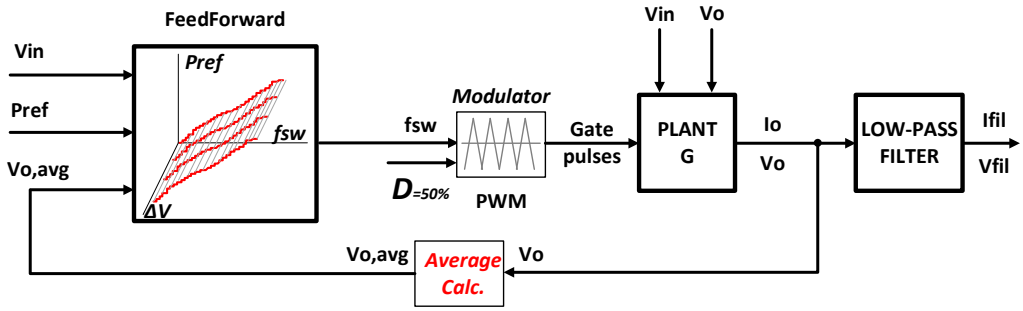


Figure 3.6: Diagram block of the system with implemented FF

3.2 Small Signal model of SRC#

The design of the implemented PI controller is based on the small signal model of the SRC#. From the non-linear equations of tank current, tank voltage and output current, the plant transfer function G_{plant} that relates output current and switching frequency can be obtained. [14] In particular, G_{plant} can be found through the linearization of the SRC# state-space model evaluated around specific operating points, see section C.1.

The obtained transfer functions, G_{plant}, are second order biproper systems [15] where, close to DCM operation (around 600 Hz), the poles and the zeros are placed to almost cancel each other. Therefore, transfer functions close to that boundary operating mode can be considered as gains, zero order systems, see blue curve in Figure 3.7.

Moreover, in the whole DCM region operation, due to the linearity between power and input variables, the same transfer function was considered. The structure of the obtained transfer functions is shown in Equation 3.7.

$$G_{plant}(s) = \frac{Io}{f_{sw}}\bigg|_{\tilde{V}_{in}=0,\tilde{V}_o=0} = \frac{a_0 \cdot s^2 + a_1 \cdot s + a_2}{b_0 \cdot s^2 + b_1 \cdot s + b_2} \tag{3.7}$$

In order to validate the transfer functions, a comparison between analytical simulations (Matlab) and electrical simulation (Plecs) has been made, see Table 3.3. A 1 Hz step has been applied in both simulation tools at three different operating frequencies and, the step on the averaged current has been recorded. The percentage error between the two results,shown in Table 3.3, is always lower than 0.3% absolute value. Therefore, the obtained transfer functions present a good match with electrical simulations.

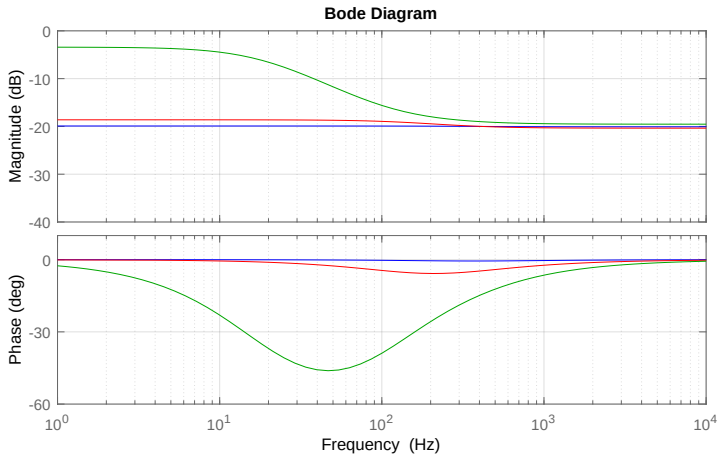


Figure 3.7: Frequency response of G_{plant} (I_o/f_{sw}). Blue: $f_{sw} = 600$ Hz, Red: $f_{sw} = 800$ Hz, Green: $f_{sw} = 1000$ Hz. $V_{in} = 4$ kV, $V_o = 99$ kV

Table 3.3: Validation of the transfer functions frequency response by comparison between Matlab and Plecs simulations

V_{out} [kV]	f_{sw} [Hz]	Matlab [A]	Plecs [A]	Error [%]
99.0	600	0.101022	0.101031	0.0089
	800	0.11726	0.1172	-0.0512
	1000	0.675358	0.673378	-0.2931
99.9	600	0.100102	0.100101	-0.0005
	800	0.101663	0.101659	-0.0036
	1000	0.137923	0.137703	-0.1594

3.3 PI controller design

In order to reduce the eventual steady-state error coming from the FF, a gain scheduling PI controller has been designed in parallel, see Figure 3.8.

The choice of the gain parameters of the PI are based on the open loop Bode design. Due to difficulties to obtain the transfer function of the implemented FF, its influence has been considered as a gain that brings the static gain of each open loop frequency response to 0 dB, see Figure 3.9.

Three specifications of the open loop frequency response have been followed for the PI controller design: high gain at low frequency, a high positive phase margin and an optimum crossover frequency to obtain the best trade-off between transient response and stability.

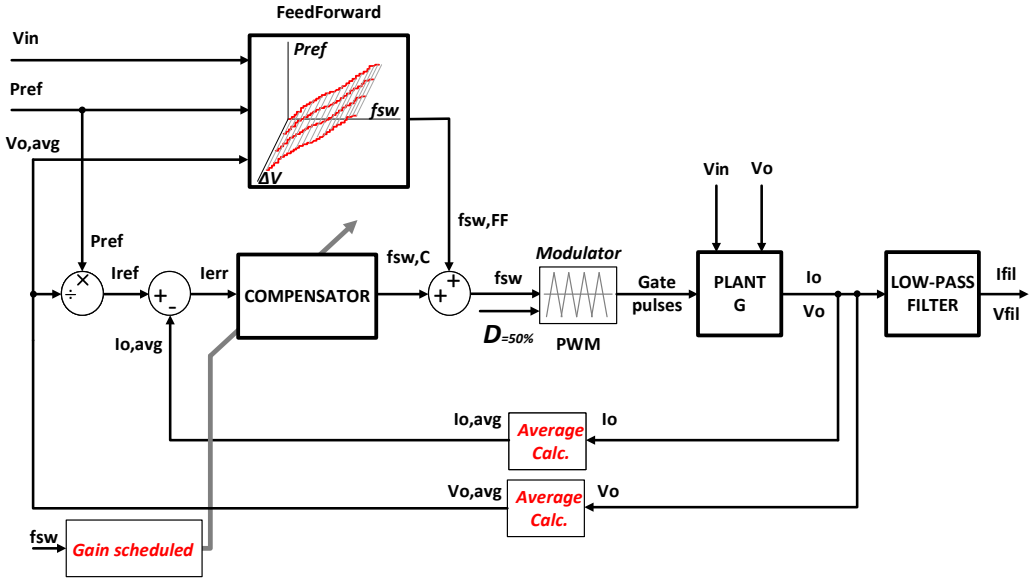


Figure 3.8: Diagram block of the system with FF and gain scheduling PI compensator implemented

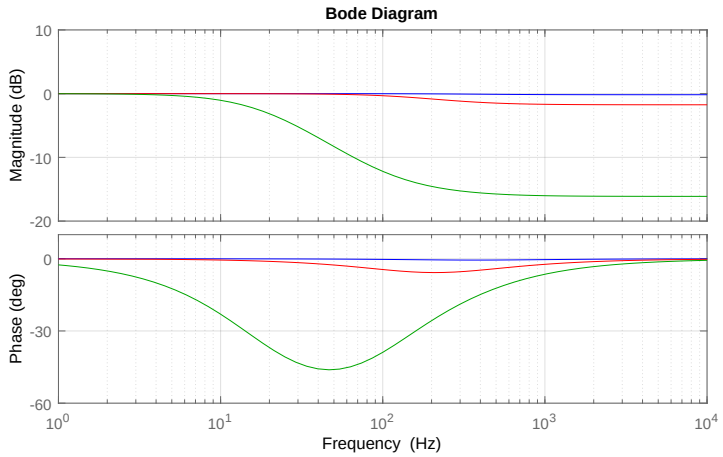


Figure 3.9: Frequency response of the plant G with FF included (I_o/f_{sw}). Blue: $f_{sw} = 600$ Hz, Red: $f_{sw} = 800$ Hz, Green: $f_{sw} = 1000$ Hz. $V_{in} = 4$ kV, $V_o = 99$ kV

In order to achieve those specifications, from common control theory knowledge [16] [17], the crossover frequency has been chosen to be always 1/10 the switching operating frequency. Therefore, due to variable operating switching frequency, the K_p and K_i parameters change along the whole range of operation of the converter, see Figure 3.10.

By achieving those specifications, the expected closed-loop control performances are: stability and low steady-state error. [18] [15]

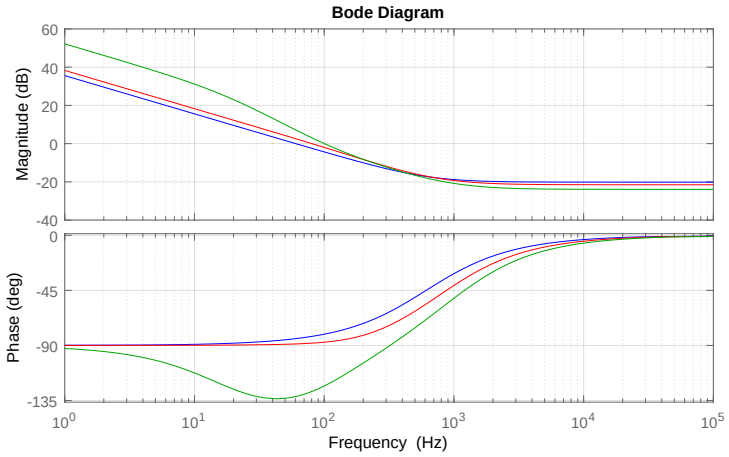


Figure 3.10: Frequency response of G plus FF plus PI_{GS} (I_o / I_{err}). Blue: $f_{sw} = 600$ Hz, Red: $f_{sw} = 800$ Hz, Green: $f_{sw} = 1000$ Hz. $V_{in} = 4$ kV, $V_o = 99$ kV

Chapter 4

Control performance

The 10 MW ideal converter model tested in the following chapter is presented in Figure 4.1. The parameter values of the ideal circuit components are shown in Table 4.1.

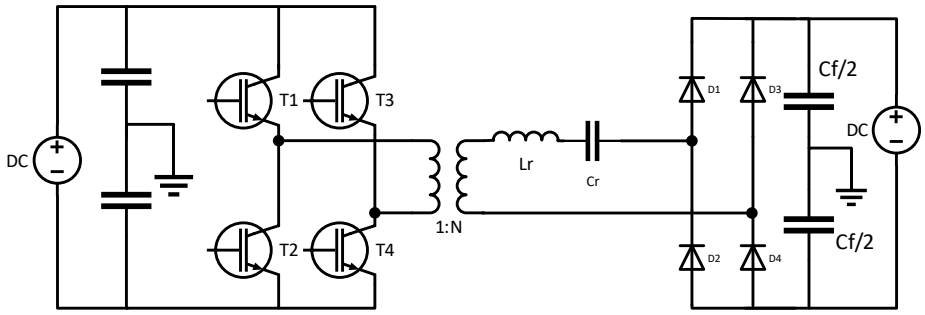


Figure 4.1: Ideal 10 kW converter circuit

Table 4.1: Parameters values of the ideal circuit components

Component	Value
Resonant inductor (L_r)	78.1 mH
Resonant capacitor (C_r)	0.25 μF
Transformer turns ratio (N)	25
Filter capacitor (C_f)	25 μF

In the following chapter are presented the steady-state and dynamic performances of the implemented controller during different tests.

All the results presented in the following chapter are obtained through simulations in Plecs on the 10MW converter model with ideal components.

4.1 Steady-state performance

The test performed for steady-state performance and, the placement of the current and voltage sensors are illustrated in Figure 4.2.

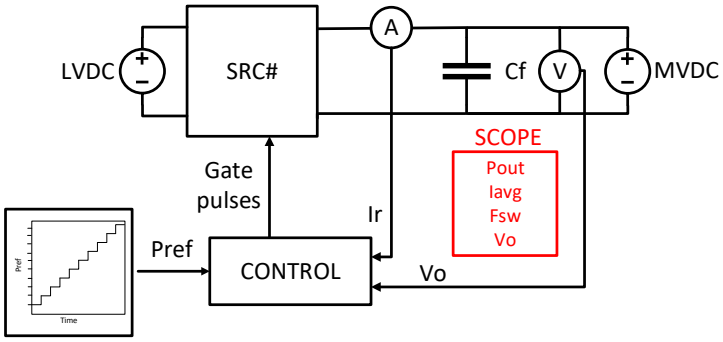


Figure 4.2: Steady-state performance test and position of sensors

The steady-state performance test shows the error between a reference power and the output power of the controlled converter. The steady-state error at each MW level is shown comparing FF and $FF + PI_{GS}$. As it can be seen in Table 5.1 the accuracy of the FF is high even at the non-linear region (10MW, $V_{out} = 98kV$) and, therefore the compensator action is low. The error at all operating points, always lower than 0.1%, validates the power equation for the DCM region shown in Equation 2.4 and the linearization for the FF look up table made from the equation in Equation 2.7.

Table 4.2: Steady-state error between output power and reference power for FF and FF+GS

Reference Power [MW]	Error [%]		Frequency [Hz]	
	FF	FF+PI_{GS}	FF	FF+PI_{GS}
1	-0.0004	-0.0004	102.04	102.04
2	-0.0004	-0.0004	204.08	204.08
3	-0.0004	-0.0004	306.12	306.12
4	-0.0004	-0.0004	408.16	408.16
5	-0.0004	-0.0004	510.20	510.20
6	-0.0207	-0.0207	611.53	611.53
7	-0.0149	-0.0149	707.06	707.06
8	-0.0024	0.0013	791.82	791.82
9	0.0937	0.0307	859.57	859.28
10	0.093	0.0722	906.98	906.60

4.2 Set-point tracking bandwidth

The test performed for set-point tracking bandwidth and, the placement of the current and voltage sensors are illustrated in Figure 4.3.

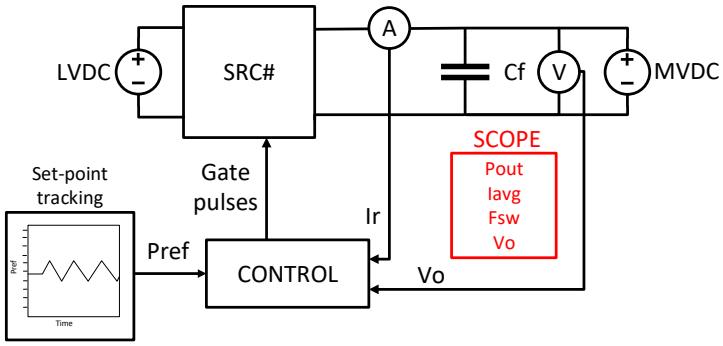


Figure 4.3: Set-point tracking bandwidth test and position of sensors

The set-point tracking bandwidth test consist on applying a triangular set-point with a certain amplitude at different frequencies. The amplitude is set to 0.25MW and the frequency range between 2Hz to 300Hz.

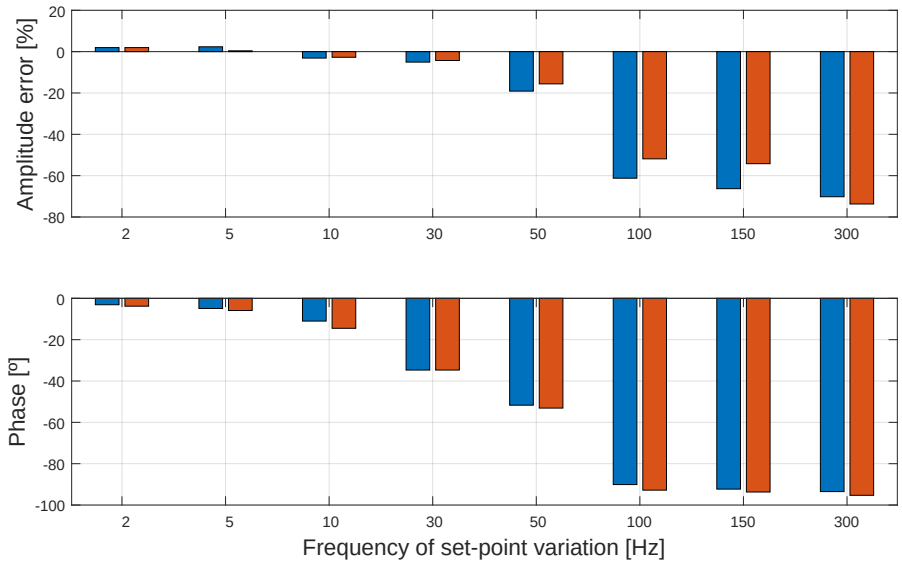


Figure 4.4: Amplitude and phase of output power compared to the reference
Blue: FF Red: FF + PI_{GS}

The first test in Figure 4.4 is performed at 9.75MW base power with a $\Delta V =$

$99kV$. The amplitude error is calculated as in Equation 4.1, and represents the relative error between the output power amplitude and set-point. The phase is represented as the output power in respect to the reference in the bar diagram, therefore negative values indicate that the output power is lagging.

The relative amplitude error at low frequencies is kept below 3%, which implies a good bandwidth tracking up to 30Hz, and when the ratio $f_{sw}/f_{set-point}$ starts to decrease the output power is able to follow up to 60% of the amplitude value at frequencies higher than 100Hz. The phase lag increases as the set-point frequency increases and reaches around 90°.

$$AmplitudeError[\%] = \frac{Amplitude_{Pout} - Amplitude_{Setpoint}}{Amplitude_{Setpoint}} \cdot 100 \tag{4.1}$$

4.3 Dynamic performance

The dynamic tests performed in the ideal 10 MW Plecs model of the converter are power steps and outptut voltage steps. The following results show how the converter with the implemented controllers respond during step variations on the reference power or the output voltage.

4.3.1 Power steps

The test performed for power step performance and, the placement of the current and voltage sensors are illustrated in Figure 4.5.

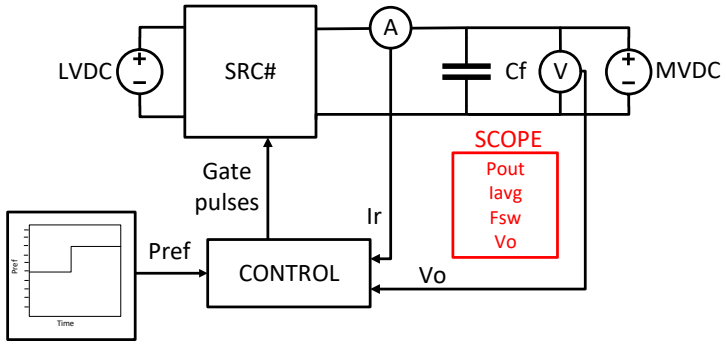


Figure 4.5: Power step dynamic test and position of sensors

The presented results in this section show the performance of the FF and the FF gain scheduling PI at different operating conditions, see Figures 4.6.

First, a power step of 0.5MW is applied when the converter is operating in DCM (power step from 2.5 MW to 3.0 MW), see Figure 4.6 (left). Then, the same power step is tested during boundary operating conditions of the converter so, when the

converter's mode operation changes from DCM to CCM (power step from 5.5 MW to 6.0 MW), see Figure 4.6 (right). Finally, the power step dynamic performance of the converter operating in CCM1-Hybrid is shown in Figure 4.6 (bottom).

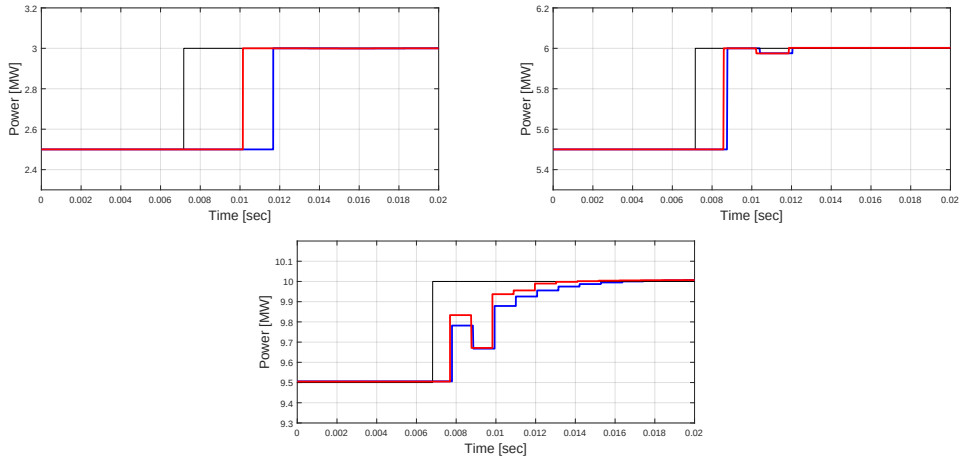


Figure 4.6: Converter's dynamic performance during power steps-up. Comparison between the implemented controllers.

Blue: FF Red: $FF + PI_{GS}$ Black: P_{ref}

As already seen from the steady-state performance, either for the power step dynamic performance there is a low compensator reaction, see Figure 4.6.

Moreover, it can be seen that both power step dynamic performances of the implemented controllers present no steady-state error, no overshoot and, minimum rise time and, minimum settling time. Those characteristics are typical of a dead-beat controller [18].

Only in figure Figure 4.6 (right), there is a visible difference between the FF (blue) and, the FF plus gain scheduling PI. The reason is due to the higher frequency correction given by the compensator at high frequencies, see Figure 4.7 (right). On the other hand, at lower frequencies, any correction is given by the gain scheduling PI, see Figure 4.7 (left).

In Figure 4.7, both cases and both controllers present a time delay between the reference power and frequency correction. In particular, this delay always last less than one operating switching period. Therefore, the only reason why this time lag happen is because the step on the reference power has been applied in the middle of a switching period.

4.3.2 Voltage steps

The test performed for output voltage step performance and, the placement of the current and voltage sensors are illustrated in Figure 4.8.

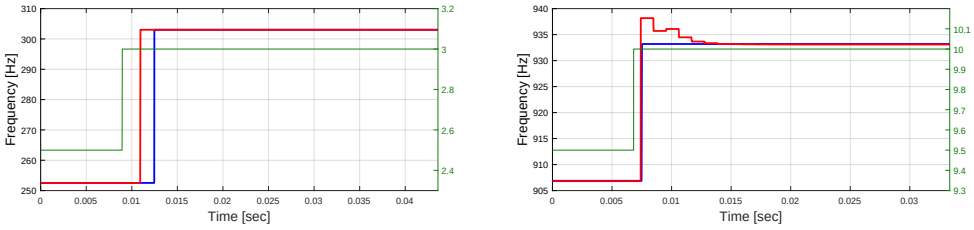


Figure 4.7: Comparison of the frequency correction given by the FF and $FF + C_{GS}$ at low (left) and high (right) frequency

Blue: FF Red: FF + C_{GS} Green: P_{ref}

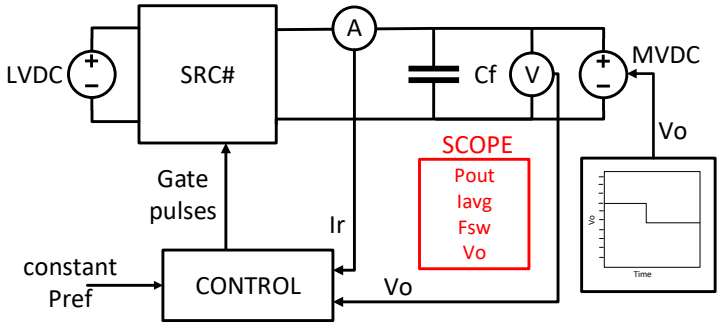


Figure 4.8: Voltage step dynamic test and position of sensors

In the following results, the dynamic performance of the implemented controllers during an output voltage down-step of 2 kV is presented in Figure 4.9. The applied output voltage goes from 99.9 kV to 97.9 kV and it is applied when the converter is operating at full power, 10 MW.

In both cases, the implemented controllers give a negative frequency correction in order to reach the desired reference power also, when the voltage difference between input and output has been increased, see Figure 4.10. Moreover, it can be seen the different frequency correction given by the controllers during an output voltage step-down, Figure 4.10.

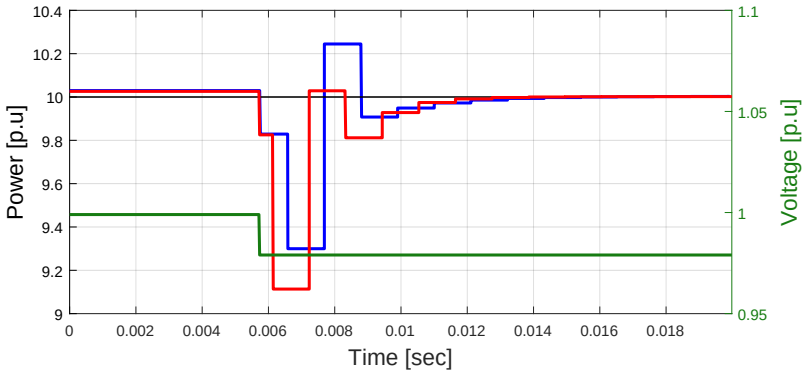


Figure 4.9: Converter's dynamic performance during output voltage step-down. Comparison between the implemented controllers.

Blue: FF Red: FF + PI_{GS} Black: P_{ref}

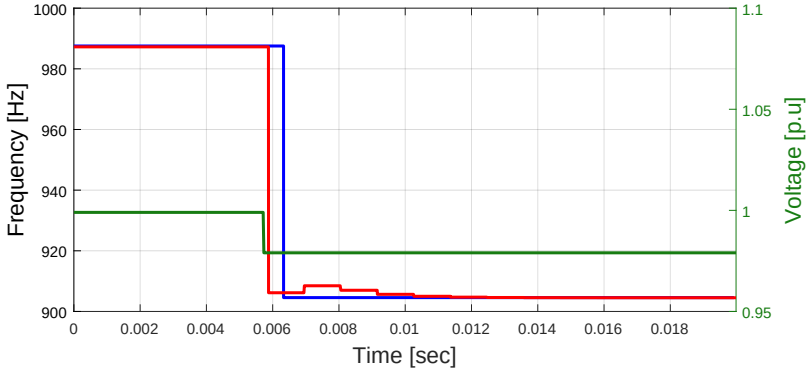


Figure 4.10: Comparison of the frequency correction given by the FF and $FF + C_{GS}$ during a voltage down-step

Blue: FF Red: $FF + PI_{GS}$ Green: V_{out}

4.4 Harmonic rejection

The test performed for output voltage harmonic rejection performance and, the placement of the current and voltage sensors are illustrated in Figure 4.11.

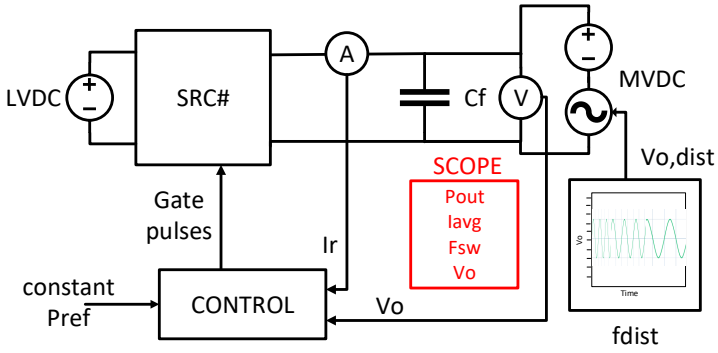


Figure 4.11: Output voltage disturbance test and position of sensors

The harmonic rejection test consist on applying an output AC sine voltage disturbance of 0.5% Vout amplitude on top of the MVDC voltage level with a variable range of frequencies between 2 to 300Hz. Afterwards, observe if the converter and controller are able to keep the reference power constant by reporting the amplitude and phase of the output current compared to the reference. The first reference point is at 5MW and $V_{out} = 99.2kV$ where the converter is operating in conduction mode DCM2, identified as a linear region. In Figure 4.12 is compared the plant reaction in open loop (in blue) with the FF control technique and FF with GS.

The second reference point is at nominal power 10MW and $V_{out} = 99.2kV$ where the converter is operating in conduction mode CCM1-hybrid, identified as a non-linear region. Shown in the bar diagram in Figure 4.13 the controller is able to keep the output power with a lower amplitude than the response of the plant (open loop, in blue) until 150Hz disturbance frequency. Since this test is performed in the non-linear region, the amplitude of the open loop response is higher compared to the previous test at 5MW.

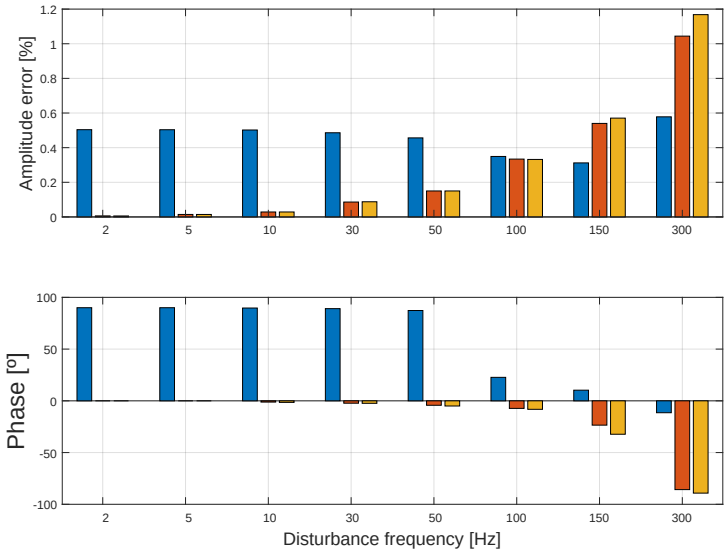


Figure 4.12: Amplitude error [%] of the output current respect to current reference for a output voltage disturbance of amplitude $V_{dist} = 0.5\%Vout$ and frequency range from [2 to 300Hz]. Phase lag [º] of output current respect to reference current.

Blue: Open Loop Orange: FF Yellow: FF + PI_{GS}

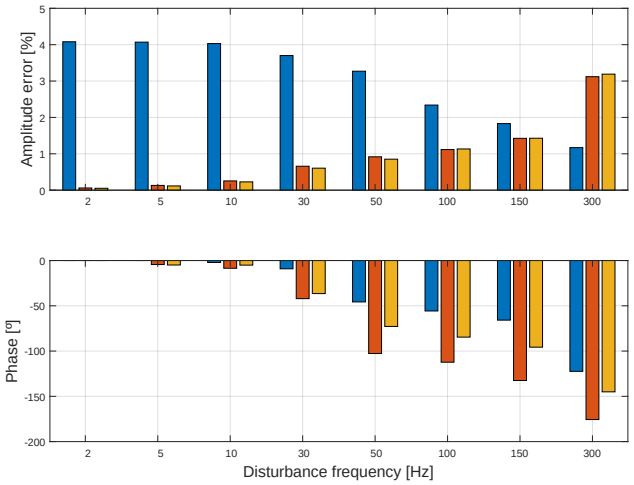


Figure 4.13: Amplitude error [%] respect to 10MW reference power when applying a voltage disturbance on the output of amplitude $V_{dist} = 0.5\%Vout$ and frequency range from [2 to 300Hz]. Phase lag [º] of output current respect to reference current.

Blue: Open Loop Orange: FF Yellow: FF + PI_{GS}

4.5 Output voltage sag

The test performed for output voltage sag performance and, the placement of the current and voltage sensors are illustrated in Figure 4.8.

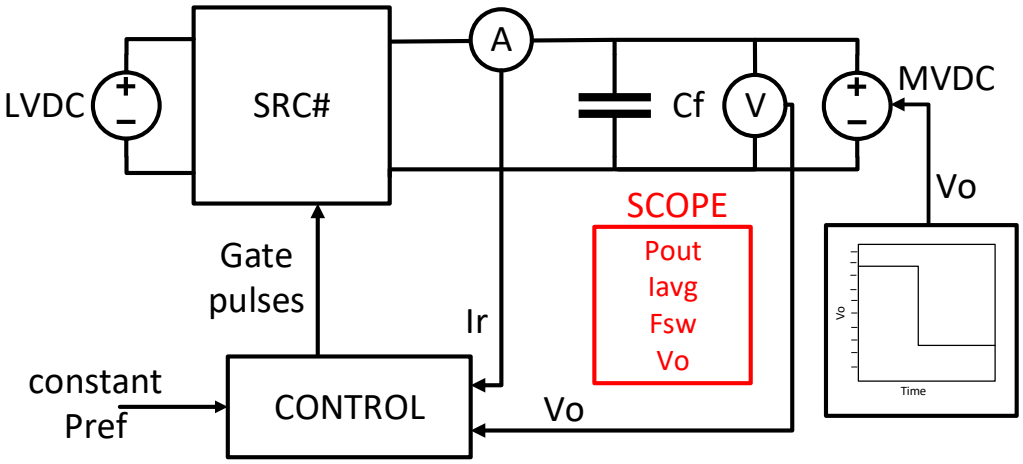


Figure 4.14: Output voltage sag test and position of sensors

The output voltage drop test consists on setting a current limitation for the controller when the output voltage drops suddenly, and goes out of the FF (and converter) boundaries causing a high current. In that case the purpose of our controller is no longer control the power but set a limitation on the current that does not damage the converter until the output voltage is restored. In Figure 4.15 is shown the difference between having a current limitation or not.

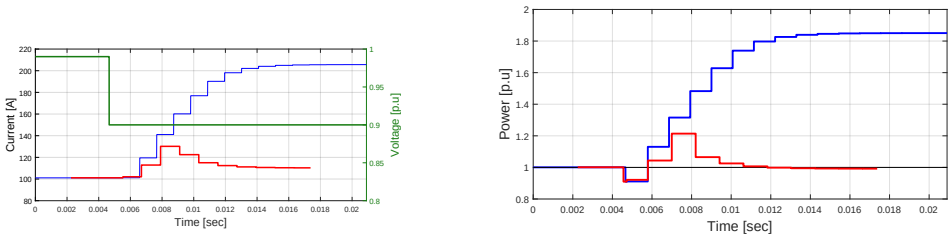


Figure 4.15: Comparison between power reactions of the converter in open loop and with the FF controller with current limiter, when a negative output voltage drop occurs, 9000 V

Blue: Open loop, current (top), power (bottom) Red: FF with limiter, current (top), power (bottom)
Black: P_{ref} Green: V_{out}

4.6 Filter inductor impact

The test performed to analyze the output choke impact and, the placement of the current and voltage sensors are illustrated in Figure 4.16.

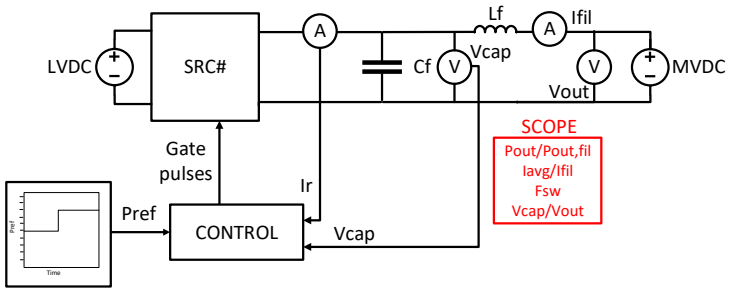


Figure 4.16: Filter inductor impact test and position of sensors

When the inductor is placed on the output it is important to investigate its effect. Since the converter is operated at variable frequency between 0 to 1kHz, the resonant frequency of the filter should be reasonably low so it does not amplify the rectified current pulsating at twice the switching frequency.

The resonant frequency of an LC filter is given by Equation 4.2

$$f_r = \frac{1}{2 \cdot \pi \sqrt{L_f \cdot C_f}} \tag{4.2}$$

In this test an inductor of 1.2 mH and capacitor of 25μF with a resonant frequency of 29 Hz.

As it can be seen in Figure 4.17 during a power step at 4.5MW to 5MW in open loop, oscillations at 29Hz on the voltage across the capacitor cause oscillations of low amplitude on the rectified current and high amplitude on the output of the filter.

However, as it can be seen in Figure 4.18 the FF reacts with a frequency correction overcome this oscillation positively.

On the other hand, when a step is applied at high power, 10MW, in Figure 4.19 it can be seen that the open loop response looks like a first order response and the voltage across the capacitor only has one oscillation, which results on a better response compared to the reaction of the FF to this oscillation respect of the output power of the filter, see Figure 4.20.

In conclusion, since some operating frequencies are close to the resonant of the low-pass filter is important to consider the effect of the filter on the output power to attenuate the oscillations coming from this one when a change in power or voltage is applied.

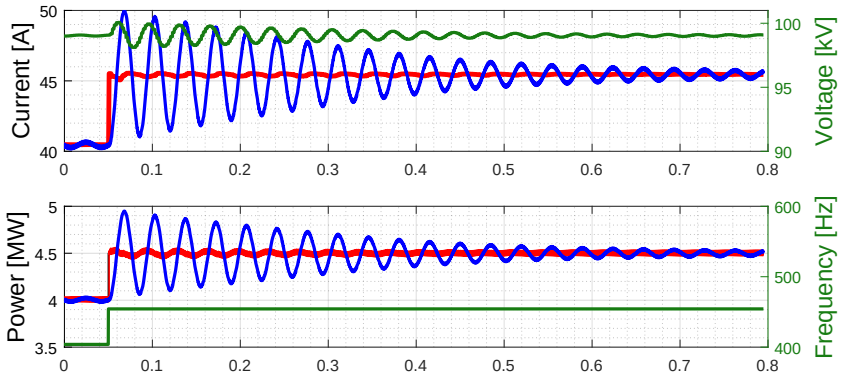


Figure 4.17: Open loop response to a power step from 4 MW to 4.5 MW when an inductor is placed on the output. Red: Iavg (top), Pavg (bottom), Blue: Ifil (top), Pfil (bottom), Green: Vout (top), f_{sw} (bottom)

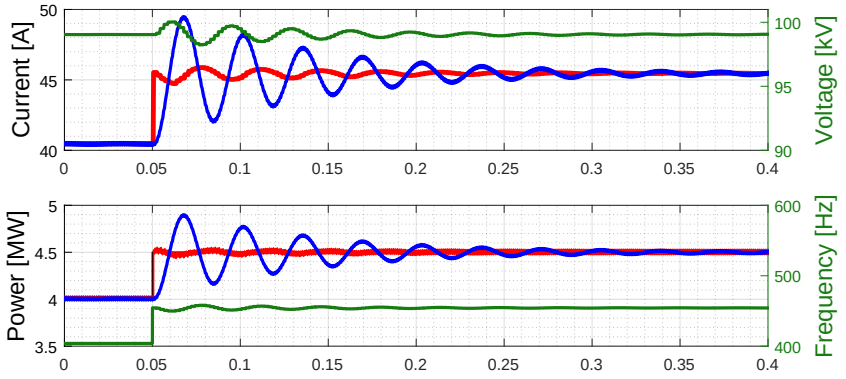


Figure 4.18: FF response to a power step from 4 MW to 4.5 MW when an inductor is placed on the output

Red: Iavg (top), Pavg (bottom) Blue: Ifil (top), Pfil (bottom) Green: Vout (top), f_{sw} (bottom)

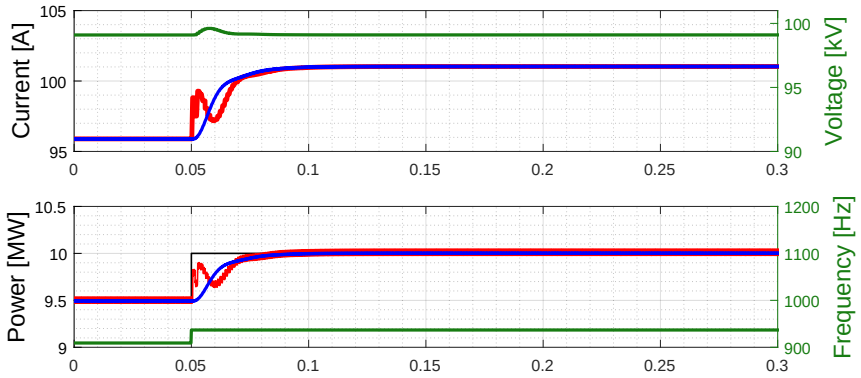


Figure 4.19: Open loop response to a power step from 9.5MW to 10MW when an inductor is placed on the output

Red: Iavg (top), Pavg (bottom) Blue: Ifil (top), Pfil (bottom) Green: Vout (top), f_{sw} (bottom)

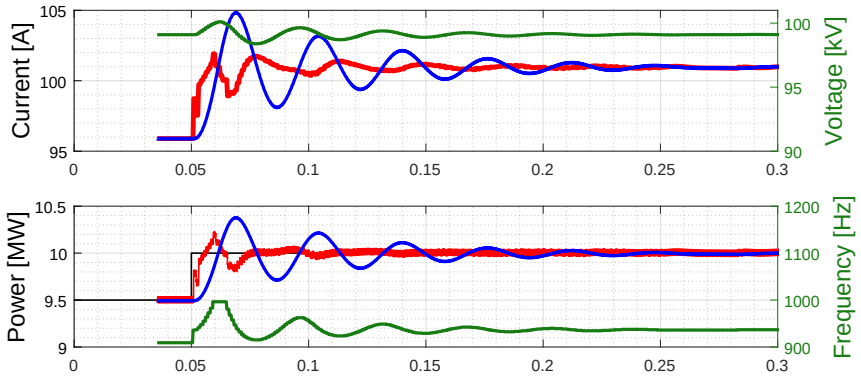


Figure 4.20: FF response to a power step from 9.5MW to 10MW when an inductor is placed on the output.

Red: Iavg (top), Pavg (bottom) Blue: Ifil (top), Pfil (bottom) Green: Vout (top), f_{sw} (bottom)

Chapter 5

Experimental results

In this chapter, the experimental results obtained from the scaled down 10 kW setup are presented. The procedures followed in the laboratory are explained in Appendix B.

Moreover, laboratory limitations are presented in Appendix B. The results from the set-point tracking bandwidth and the harmonic rejection tests are obtained from Plecs simulations of a circuit representative of the non-ideal 10 kW laboratory setup, see Figure 5.1

The circuit presented in the previous sections chapter 4 is a lossless model with ideal components. However, the 10kW scaled-down setup at Aalborg University contains non-idealities that are important to consider when building a simulation model to validate the results, see Figure 5.1.

The model of the sources, IGBT's, transformer and diodes can be found in Appendix A. The components that have been characterized with non-idealities are the following:

- Inverter: losses caused by the IGBT's are modelled as resistors
- Transformer: the medium frequency transformer contains several elements that have to be considered such as leakge inductance, winding resistances and magnetizing inductance.
- Resonant inductor: since the resonant inductor is hand-winded a stray capacitance is placed in parallel.
- Snubber circuit and diodes: the diodes used have a certain reverse recovery characteristics that is important to include. Moreover, the snubber circuit contains a resistor and capacitor in parallel which also affect the waveforms.

The non-ideal parameter values considered in the electrical circuit simulator (Plecs) are shown and analyzed in Appendix A where, it has been characterized

the 10 kW laboratory setup. The result of nonidealities on the current waveforms is represented in subsection A.1.3.

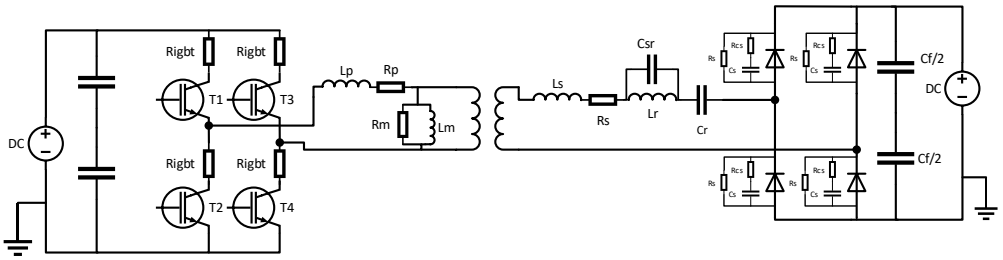


Figure 5.1: Non-ideal circuit converter circuit

The relation between output power and switching frequency for the laboratory setup cannot be determined by the analytical expressions developed in chapter 2.

Therefore, as already illustrated in Figure 3.5, the power curves used for the FF implementation in the 10 kW laboratory setup are obtained through experimental data. Moreover, the operating conditions of the FF are defined in Table 3.2.

5.1 Steady state performance

The steady-state performance test compares the output power to the set-point power given to the controller. In Figure 5.2 results for two different output voltage levels are tested; the above graph is at 4.9kV and the one below is at 4.95kV. The procedure followed during the laboratory tests for the steady-state performance is explained in subsection B.2.1. In general, the FF lacks accuracy at some reference power levels due to its linearization reaching steady-state errors between 0.2% to 8%. On the other hand, close loop tests show steady-state errors from 0% to 0.4% with no significant difference between the gain scheduling PI and constant PI.

In Table 5.1 the steady-state error at each kW level is shown respect to the reference power and to the non-ideal Plecs model with 4.9kV output voltage. On the right column the switching frequency value is compared among the three control techniques:

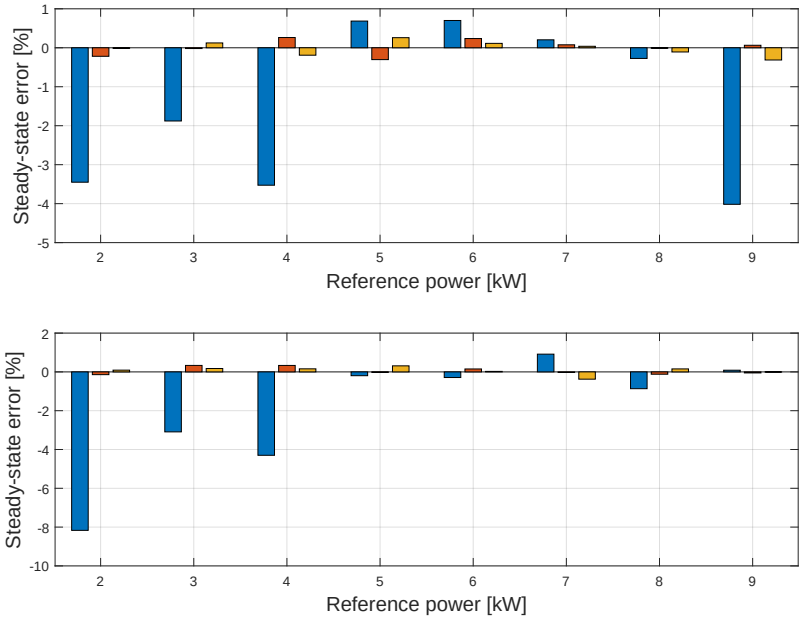


Figure 5.2: Bar diagram of the steady-state errors between reference and output power. On top bar diagram for 4.9kV operating point and on the bottom 4.95kV.

Blue: FF Red: FF + PI_K Red: FF + PI_{GS}

Table 5.1: Steady-state error between output power and reference power for each control technique at 4.9kV output voltage

P_{ref} [W]	Error [%]			Frequency [Hz]		
	FF (Plecs)	FF+PI_K (Plecs)	FF+PI_{GS} (Plecs)	FF	FF+PI_K	FF+PI_{GS}
2000	-3.450 (-3.008)	-0.219 (-0.19)	-0.013 (0.130)	223.2	236.0	236.1
3000	-1.879 (-1.951)	-0.020 (-0.04)	0.124 (0.341)	336.8	336.7	335.2
4000	-3.527 -1.667	0.263 (-0.03)	-0.191 (-0.122)	441.3	451.0	449.3
5000	0.685 (-1.502)	-0.304 (-0.02)	0.259 -0.081	559.8	553.2	550.0
6000	0.700 (-1.687)	0.237 (-0.312)	0.113 (0.102)	667.8	663.3	658.1
7000	0.204 (-2.018)	0.076 (0.03)	0.038 (-0.187)	777.0	771.9	767.4
8000	-0.274 (-0.410)	-0.011 (-0.21)	-0.108 (-0.092)	863.2	867.3	861.8
9000	-4.017 (-2.889)	0.064 (0.438)	-0.314 (-0.121)	902.2	923.1	920.8

In Table 5.2 the steady-state error at each kW level is shown respect to the reference power and to the non-ideal Plecs model with 4.95kV output voltage.

Table 5.2: Steady-state error between output power and reference power for each control technique at 4.95kV output voltage

P_{ref} [W]	Error [%]			Frequency [Hz]		
	FF (Plecs)	FF+PI_K (Plecs)	FF+PI_{GS} (Plecs)	FF	FF+PI_K	FF+PI_{GS}
2000	-8.168 (-3.582)	-0.142 (-0.12)	0.091 (-0.15)	233.6	265.3	265.9
3000	-3.092 (-3.014)	0.334 (0.15)	0.175 (-0.3)	356.9	364.8	364.0
4000	-4.299 (-3.33)	0.333 (-0.16)	0.158 (-0.7)	468.1	488.8	487.7
5000	-0.196 (-0.208)	-0.023 (-0.05)	0.312 (0.04)	588.8	590.2	587.4
6000	-0.290 (-2.519)	0.151 (-0.06)	0.026 (0.13)	697.7	698.3	696.4
7000	0.915 (-0.7143)	-0.029 (0.17)	-0.375 (0.19)	808.0	794.7	795.3
8000	-0.866 (-0.417)	-0.120 (0.26)	0.154 (-0.05)	903.2	903.9	903.5
9000	0.087 (-0.64)	-0.053 (-0.12)	-0.007 (-0.25)	951.1	948.7	950.5

5.2 Set-point tracking bandwith

The set-point tracking bandwidth test shows simulated data about amplitude and phase lag [1] compared to reference power when applying a power disturbance with a triangular set-point change ($V_o = 4.9kV$), see Figure 5.3. The amplitude of the set-point tracking is 250W and the frequency range from 2 to 300Hz. In subsection B.3.4, the test procedure followed for the set-point tracking bandwidth test is described.

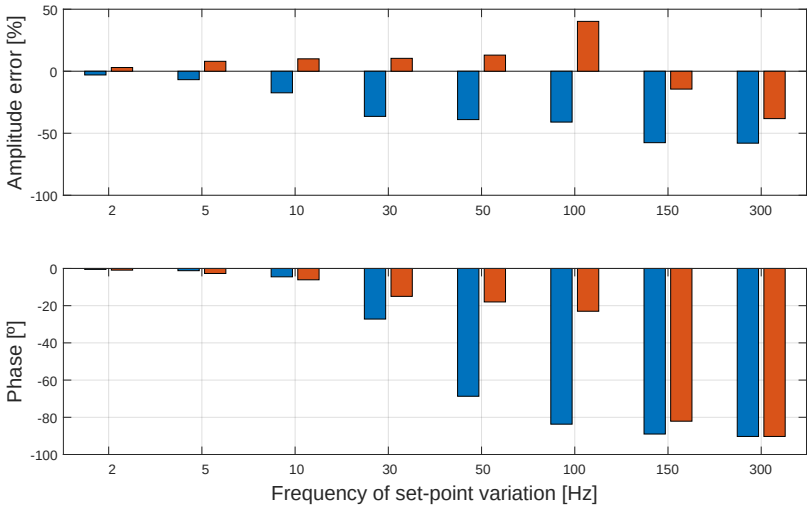


Figure 5.3: Set-point tracking bandwith at 8500W base power, without inductor. Amplitude and phase between output power and reference power. Simulation results. Blue: FF ; Red: FF + PI_{GS}

[1] The rectified power amplitude and phase was not measured due to lack of running the test with time measuring in the DSP, however the results with the filter can be found in subsection B.3.4

5.3 Dynamic performance

In order to test the dynamic performances of the implemented controllers, the inductor of the output filter is removed. In this way, there is no resonance influence from the output filter and the dynamic performances of the converter itself with the implemented controllers can be seen.

Two different dynamic tests have been considered in the experimental results shown below. First, three power steps-up have been performed, see 5.3.1. Then, also three output voltage ramps-down are presented in 5.3.2, one for each implemented controller.

The procedures and steps followed in order to obtain the presented laboratory results are described and explained in subsection B.2.2 and subsection B.2.3.

Moreover, a comparison between the experimental results obtained in the laboratory and the simulations collected with the non-ideal circuit implemented in Plecs is presented for each considered dynamic.

5.3.1 Power steps

The following results show the dynamic performance of the implemented controllers during power step-up at three different operating conditions, see Figure 5.4, Figure 5.5 and Figure 5.6.

These test want to show how the three implemented controllers respond to power step-up of 500 W during three different conduction mode of the converter. First, a step-up from 2500 W to 3000 W, when the converter is operating in DCM, see Figure 5.4.

Relevant performance characteristics are presented for each tested controller in Table 5.3, Table 5.4 and Table 5.5. The settling time T_s is obtained when the steady-state power level stay within a tolerance of 2% of the steady-state power reached during those power steps [cite something]. The rising time, T_r, is calculated by standard definition of this parameter [cite something], the time period at which the signal change from 10% to 90% of its final value. Finally, the percentage overshoot (PO), if present, is shown for each implemented controller in Table 5.3, Table 5.4 and Table 5.5.

In Figure 5.4 can be seen the dynamic performance of the implemented controllers during a 500 W power step in DCM operation, experimental results on the top and simulation results on the bottom. From Figure 5.4, it can be seen that the FF has a faster response but, never reaches the reference power value. On the other hand, both FF + PI_K and FF + PI_{GS} are able to follow the reference power. Moreover, it can be seen that the FF + PI_{GS} presents a faster transient compared to the one with FF + PI_K but, with more overshoot, see Table 5.3.

Then, the converter has been tested around a boundary zone between DCM and CCM. So, a power step from 5600 W to 6100 W is presented in Figure 5.5.

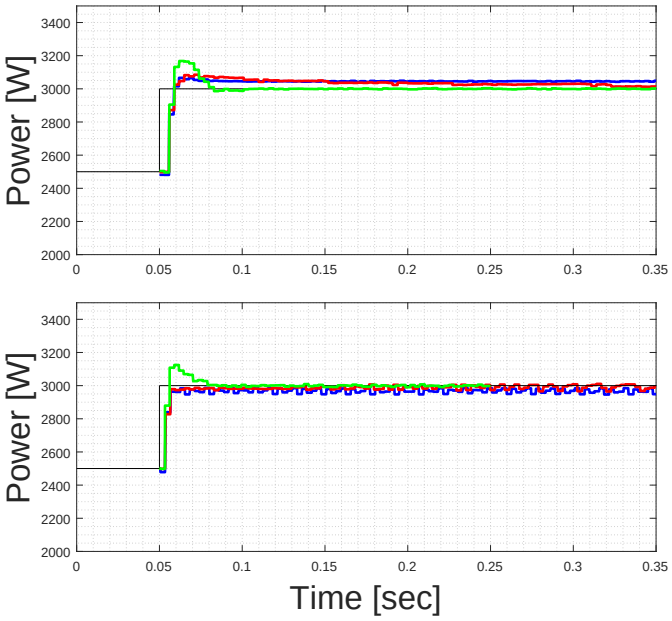


Figure 5.4: Comparison of power dynamics between the implemented controllers during a 500 W power step-up [2500W $\rightarrow$ 3000W]. Laboratory results (top); Plecs simulation results (bottom)

Blue: FF Red: FF + C Green: FF + PI_{GS} Black: Reference power

Table 5.3: Dynamic performance during power step-up [2500W $\rightarrow$ 3000W]. Comparison between the controller implemented

Controller	Overshoot [%] (Plecs)	T_s [ms] (Plecs)	T_r [ms] (Plecs)
FF	0.69 (0)	8.9 (6.66)	2.94 (2.94)
FF + C	2.79 (0)	176.98 (6.61)	2.98 (2.93)
FF + PI_{GS}	5.59 (3.91)	29.99 (20.40)	2.98 (2.82)

Regarding the FF performance, blue curves, the output power does not follow the reference power either after the power step is applied and, either before. When the FF plus PI_K is implemented, red curves in Figure 5.5, the dynamic performance during a power step is improved compared to the FF one. The output power reaches with good and fast transient the power reference specified (6100 kW). On the other hand, when the PI_{GS} is implemented, see green curves, the dynamic performance presents overshoot of 3.49% and a longer transient compared to the case with FF + PI_K.

Finally, a power step from 8000 W to 8500 W, when the converter is in CCM, see Figure 5.6. In this case, the FF presents good dynamic performances, see Table 5.5. Meanwhile, the FF + PI_K has the slowest transient compared to the other cases, FF and FF + PI_{GS}. Regarding the FF + PI_{GS}, the power reaches the reference value faster than the case with PI_K, see Figure 5.6. On the other hand, the transient

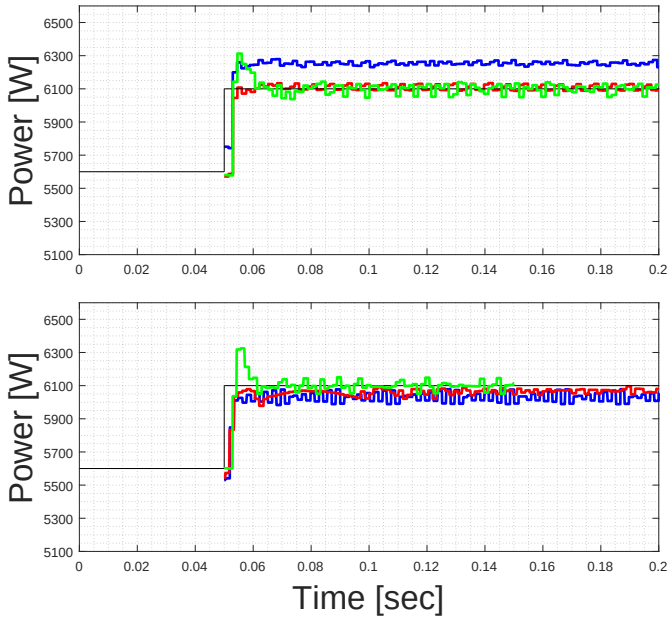


Figure 5.5: Comparison of power dynamics between the implemented controllers during a 500 W power step-up [5600W $\rightarrow$ 6100W]. Laboratory results (top); Plecs simulation results (bottom)

Blue: FF Red: FF + C Green: FF + PI_{GS} Black: Reference power

Table 5.4: Dynamic performance during power step-up [5600W $\rightarrow$ 6100W]. Comparison between the implemented controllers

Controller	Overshoot [%] (Plecs)	T_s [ms] (Plecs)	T_r [ms] (Plecs)
FF	0.42 (0)	2.98 (3.42)	1.46 (1.47)
FF + C	0.47 (0)	3.06 (13.6)	1.50 (11.7)
FF + PI_{GS}	3.49 (3.56)	24.3 (8.56)	1.5 (1.40)

presents higher overshoot and ringing at a frequency of 140 Hz, see Figure 5.6.

Table 5.5: Dynamic performance during power step-up [8000W $\rightarrow$ 8500W]. Comparison between the controller implemented

Controller	Overshoot [%] (Plecs)	T_s [ms] (Plecs)	T_r [ms] (Plecs)
FF	0.23 (0.98)	3.44 (3.02)	9.1 (3.38)
FF + C	0.0 (0.97)	122 (4.02)	144.7 (5.6)
FF + PI_{GS}	3.27 (X)	33.8 (X)	3.34 (X)

In Figure 5.4, Figure 5.5 and Figure 5.6 can be seen oscillations when the transients are finished. Those oscillations are related to the sampling jitter coming from an asynchronous sampling of the measured currents, see Figure 5.7. The figure on the left shows the measured averaged currents when is present a constant 100 kHz ADC sampling. In this case, the measured currents present oscillations. On the

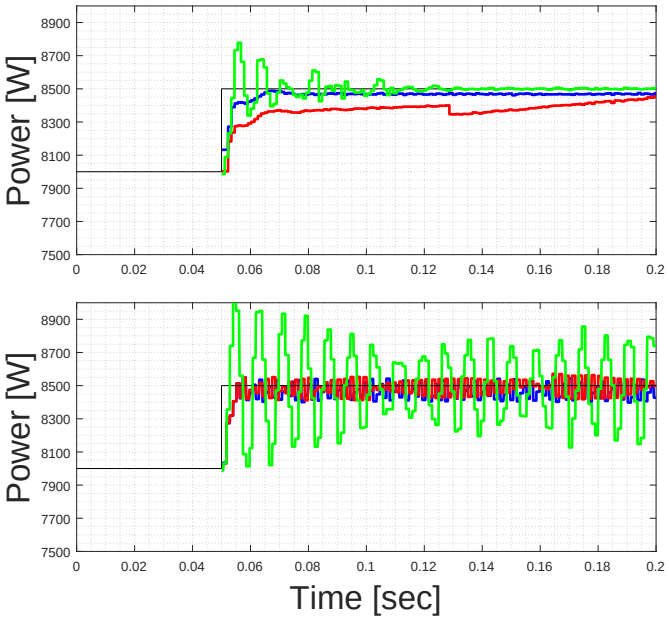


Figure 5.6: Comparison of power dynamics between the implemented controllers during a 500 W power step-up [$8000W \rightarrow 8500W$]. Laboratory results (top); Plecs simulation results (bottom)

Blue: FF Red: FF + C Green: FF + PI_{GS} Black: Reference power

other hand, right plot of Figure 5.7, a synchronous variable ADC sampling has been implemented in the Plecs electrical circuit simulator and designed to obtain 200 samples per switching period, regardless the switching frequency. In this way, it can be seen in Figure 5.7 (right) that, no oscillations in the measured currents are present.

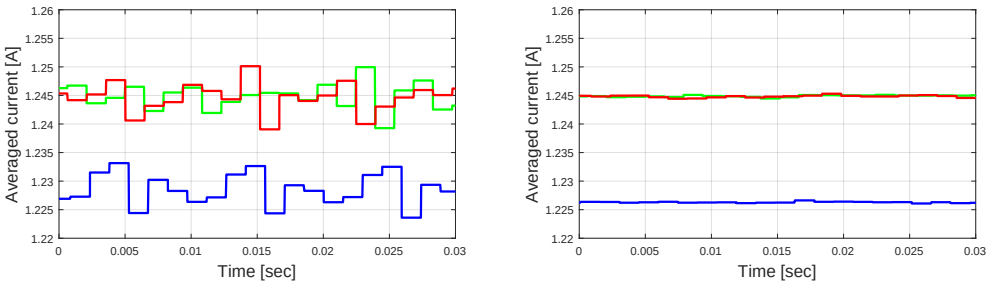


Figure 5.7: Simluation results of the comparison between measured averaged rectified current when an asynchronous ADC sampling (left) and a synchronous ADC sampling (right) are implemented.

Blue: FF Red: FF + C Green: FF + PI_{GS} Black: Reference power

Results from Figure 5.4, Figure 5.5, Figure 5.6 and Table 5.3, Table 5.4 and, Table 5.5 show a good match between the experimental results and the Plecs sim-

ulation results. Only exception are the results at high power, see Figure 5.6, when the converter operates in the non-linear region CCM1-Hybrid.

5.3.2 Output voltage ramp down

The results from the figures below show the dynamic performance of the implemented controllers during output voltage ramps-down. These tests are performed in order to see if the converter is able to maintain the reference power also during a deviation in the output voltage.

Step on the output voltage are not considered for the experimental results. Instead, ramps down on the output voltage has been tested because the output voltage applied from the source (section A.1) has been defined manually through the knob voltage regulator. Moreover, due to this experimental limitation, each controller has been tested with different variations applied on the output voltage.

For each implemented controller, the output voltage and the average rectified current with its reference value are illustrated at the top of each figure. Then, the calculated power responses are presented for each implemented controller at the bottom of each figure.

The reference power is set to 2000 W because, it has been seen during the laboratory tests that, the averaged output voltage measured by the DSP starts to increase with the switching frequency, see Figure B.7, Figure B.8 and, Figure B.9. The reason is the processing time of the implemented FF search algorithm that, starts to increase when searching high powers. This because, the search starts from the lowest reference power, see section 3.1. Therefore, during the search, some ADC sampling values for the voltage measurement are skipped. Moreover, by increasing the switching frequency, the switching period is reduced so, the time that the FF has to make the search, more relevant sampling values are skipped.

In Figure 5.8 are illustrated the dynamics of the FF during a ramp-down in the output voltage. In this case, the output voltage ramp reaches a final value outside the FF operating region. Therefore, the measured output voltage from the DSP is limited at 4797 V (lowest output voltage of the FF operating region).

From the power curve in Figure 5.8, it can be seen that the FF is not able to reach the reference power during a ramp-down in the output voltage. Particularly, the error comes first, from the accuracy of the FF and second, the saturation of the measured output voltage. A similar behaviour can be seen from the Plecs simulation results, see Figure 5.8 (right).

In Figure 5.9 are depicted the dynamic performance of the FF + PI_K. It can be seen that the correction of the compensator allows the output power to reach its reference value in around 0.4 seconds. Also in this case, the Plecs simulation results shown in Figure 5.9 (right) match with the experimental ones.

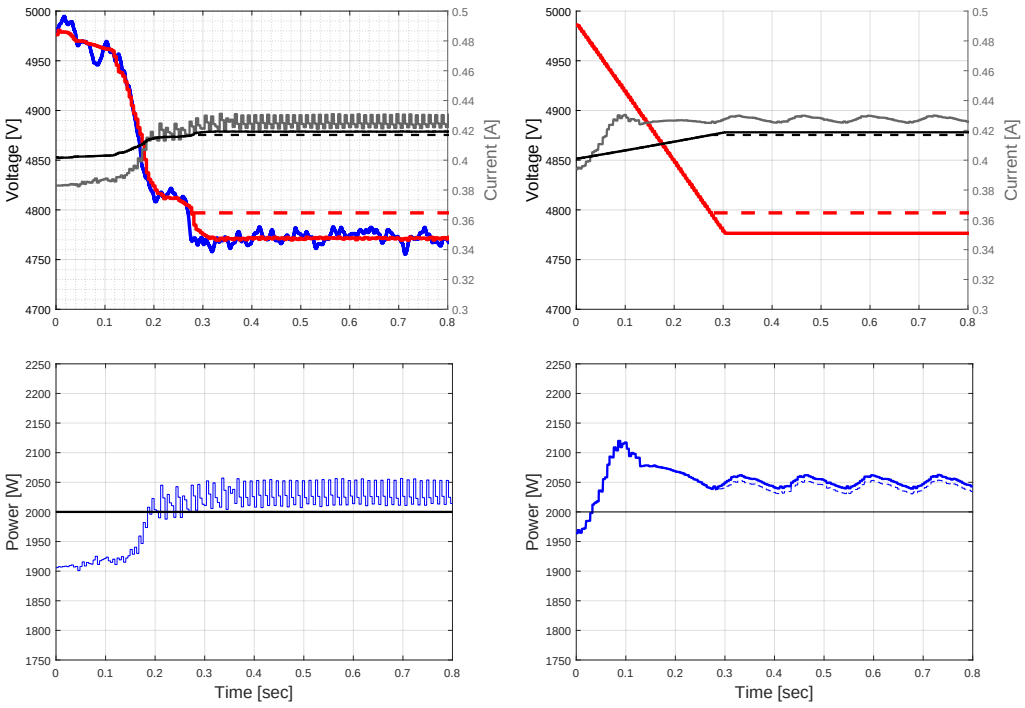


Figure 5.8: Experimental (left) ans simulation (right) results of the FF dynamic performance during voltage ramp down

Blue: V_o (Top), P (Bottom) Red: $V_{o,avg}$ Grey: $I_{r,avg}$
Red dashed: Limited $V_{o,avg}$, DSP Black: I_{ref} (Top), P_{ref} (Bottom) Black dashed: Limited I_ref

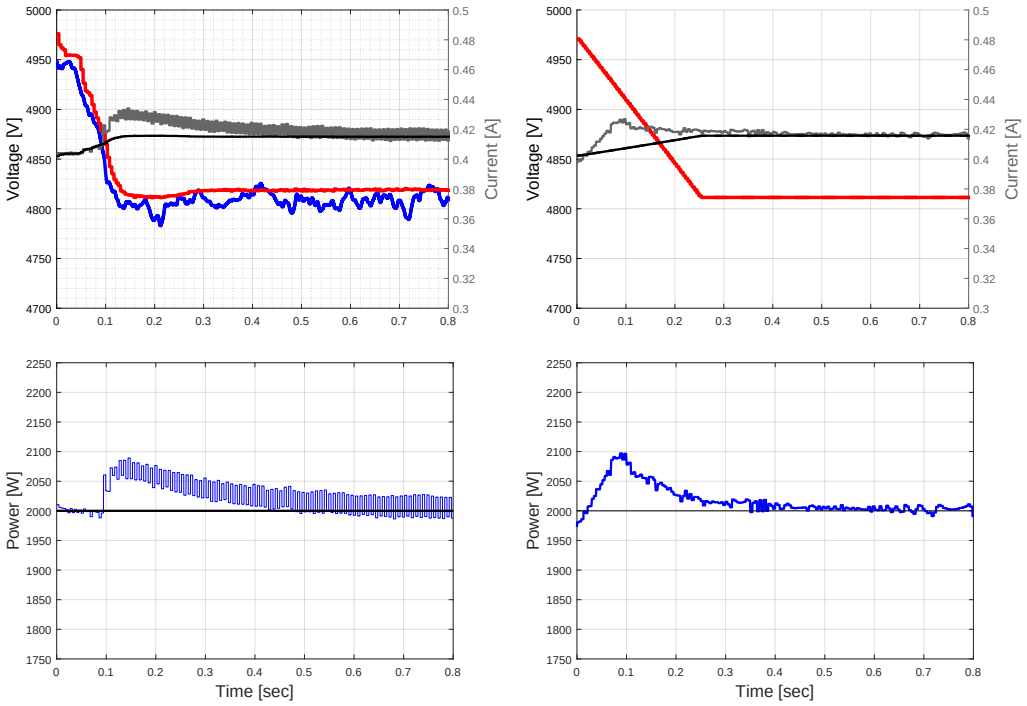


Figure 5.9: Experimental (left) ans simulation (right) results of the FF + PI$_K$ dynamic performance during voltage ramp down

Blue: V_o (Top), P_o (Bottom) Red: $V_{o,avg}$
Grey: $I_{r,avg}$ Black: I_{ref} (Top), P_{ref} (Bottom)

Finally, the dynamic performance of the FF + PI$_{GS}$ has been tested, see Figure 5.10. From the bottom plot of Figure 5.10, it can be seen that the output power follows properly the reference power, faster than the case with FF + PI$_K$.

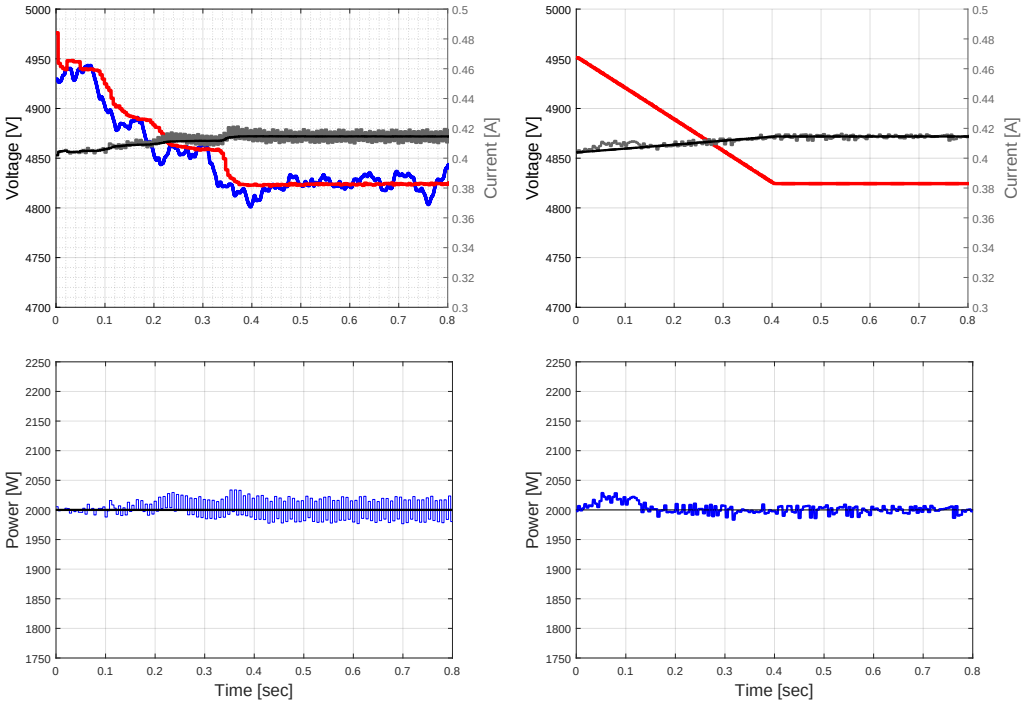


Figure 5.10: Experimental (left) and simulation (right) results of the FF + PI_{GS} dynamic performance during voltage ramp down

Blue: V_o (Top), P_o (Bottom) Red: $V_{o,avg}$
Grey: $I_{r,avg}$ Black: I_{ref} (Top), P_{ref} (Bottom)

5.4 Harmonic rejection

The harmonic rejection test is performed by Plecs simulations due to some laboratory limitations explained in Appendix B. The procedure used consists on applying a 0.5%Vout amplitude with a sine on top of the 5kV output DC voltage. The range of frequencies tested are from 2 to 300Hz. In Figure 5.11 the bar diagram shows the amplitude error and phase lag at 5kW power reference. The open loop response to the disturbance is a high amplitude of 4% at low frequencies and gets attenuated as the disturbance frequency increases. On the other hand, the FF is able to reject the harmonics on the output voltage with an error of 1% along the whole frequencies disturbance range (2 to 300 Hz), see red bars in Figure 5.11. When the PI_{GS} is added to the FF, the amplitude error at 2, 5 and 10 Hz is reduced compared to the FF case, see yellow bars in Figure 5.11. However, when the applied disturbance frequency is higher than 10 Hz, the compensator starts to have a negative effect on the harmonic rejection performance of the FF.

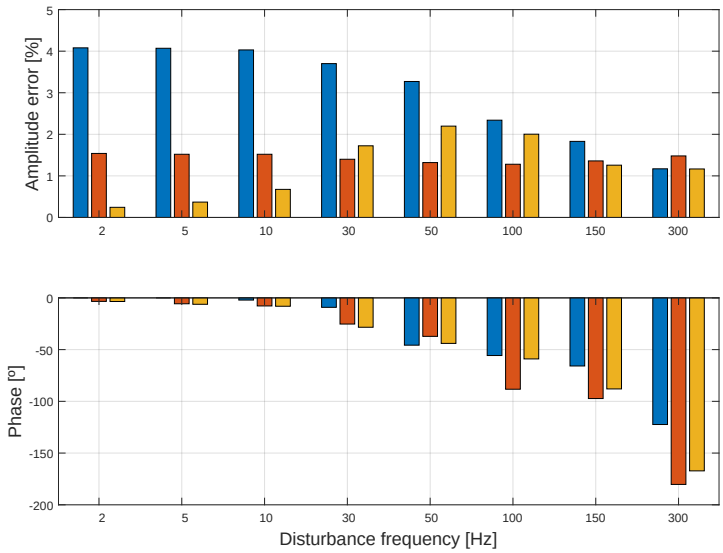


Figure 5.11: Amplitude error [%] respect to 5kW reference power when applying a voltage disturbance on the output of amplitude $V_{dist} = 0.5\%Vout$ and frequency range from [2 to 300Hz]. Phase lag [º] of output current respect to reference current. Blue: Open Loop ; Orange: Feedforward; Yellow: Feedforward + PI_{GS}

In the second test at 8kW reference power Figure 5.12, the bar diagram has similar shape than at 5kW. However, the harmonic rejection at low frequencies performs slightly better and the compensator starts to have bad performance at higher frequencies compared to the previous bar diagram at 5kW.

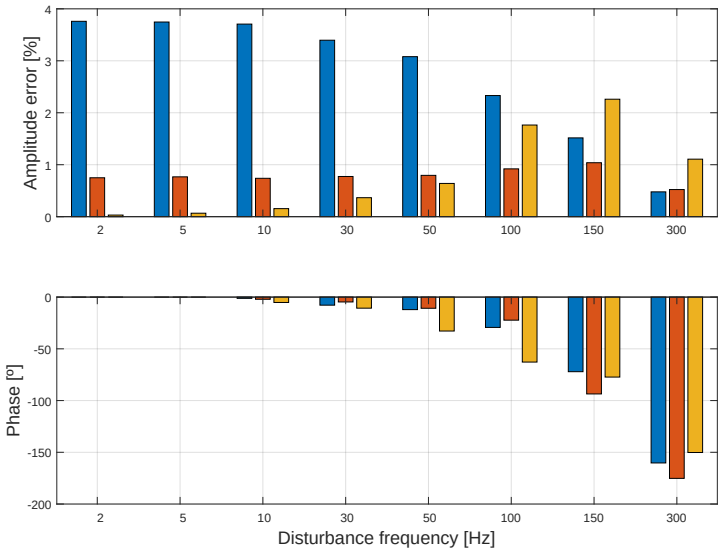


Figure 5.12: Amplitude error [%] respect to 8kW reference power when applying a voltage disturbance on the output of amplitude $V_{dist} = 0.5\% Vout$ and frequency range from [2 to 300Hz]. Phase lag [º] of output current respect to reference current. Blue: Open Loop ; Orange: Feedforward; Yellow: Feedforward + PI_{GS}

Chapter 6

Discussion

6.1 Close loop control for a DC/DC converter

In [19] and [20], the SRC is proposed as a DC/DC transformer that adapts the input and output DC voltages to control power for traction applications. The circuit is operated in sub-resonant mode, at constant frequency and open loop. However, for a WT converter application it is important to maintain the input DC link constant to allow the turbine side to work on its MPPT, avoid heavy non-linear CCM1 region and components stress when output voltage fluctuations occur. For these reasons, power tracking needs to be achieved with closed loop control that varies the switching frequency.

6.2 10 MW ideal converter results

6.2.1 Control strategy performance

From the steady-state and dynamic results of the 10 MW ideal converter, the FF controller presents good performance such as zero steady-state error, no overshoot, no undershoot, minimum rising and minimum settling time. Those characteristics are typical from a dead-beat controller [18]. Therefore, the implemented compensator in parallel, a gain scheduling (PI_{GS}) is not giving any relevant improvement to the steady-state and dynamic performances compared to the FF control system, see section 4.1 and section 4.3.

The bandwidth of the set-point tracking can be considered to be from 0 to around 30Hz, see section 4.2. Further on with the set-point frequency f_{sp}, the amplitude of the output power is lower than the reference and, the phase lag increases from 0 to 90 degrees. As the ratio f_{sw}/f_{sp} decreases, the controller reads less reference power points per cycle and, therefore, cannot follow correctly. The effect of the compensator is low but can be appreciate it between frequencies from 50Hz to

150Hz.

When a voltage disturbance is applied at low frequencies on the MVDC network, the plant reacts with an output current that oscillates leading 90° the reference current on DCM region and, lagging 90° in CCM region, see section 4.4. The amplitude of this oscillation gets attenuated as the disturbance frequency increases. The open loop response at DCM region shown in Figure 4.12 has maximum amplitude of 0.5% while in CCM1-Hybrid region in Figure 4.13 the amplitude reaches 4%. Therefore, the plant is more susceptible to give high amplitude oscillations when voltage disturbances happen at nominal power.

The reaction of the control to a voltage disturbance presents harmonics attenuation in the frequency range from 0 to 100Hz since the FF is fast enough to keep the reference constant. However, when the ratio between f_{sw}/f_{dist} decreases the controller it is not able to keep the reference power constant. At high frequency disturbances [150-300Hz], the controller reaction is causing higher oscillations than the open loop response. Therefore, a digital filtering on the output voltage measurement should be considered to reduce this issue. The effect of the compensator on harmonics rejection is negligible as its performance is similar to the FF control.

6.2.2 Impact of the output choke

The choke placed on the output of the converter is primarily needed for short-circuit protection. It is also used to smooth the output current in order to obtain a DC current. Since the operating switching frequency range is between [0-1000Hz] and the resonant frequency of the filter at 30Hz, oscillations appear during dynamics. This can be seen in section 4.6, where open loop power steps at low frequency cause 30Hz oscillations with long transients. On the other hand, at high frequency a step on the power in open loop has a first order response without oscillations. When the FF is included during a step at low power, the frequency correction giving by it helps reducing the transient. However, at high frequency, the effect of the FF results on a slightly worse performance than open loop.

It is therefore important to consider the design and impact of the choke for the control depending on the switching frequency in order to get the best output power response possible.

6.3 10 kW nonideal converter results

6.3.1 Validation of the controller design

Regarding the steady-state and dynamic results obtained from the experimental setup, due to the inaccuracy of the implemented FF, it can be seen a clear improvement given by the compensator. Moreover, in order to see the need of a gain

scheduling compensator, a PI controller with constant gains (PI_K) has been also tested.

From the steady-state analysis, the FF has steady-state errors in the range of 0.2% to 8%. Meanwhile, when a compensator is added to the system, the errors decrease in the range of 0.05% to 0.3%, see Figure 5.2.

From the power step results, subsection 5.3.1, it can be seen that a PI_{GS} that varies its gains with the switching frequency has a faster response than a PI_K, see Figure 5.4 and Figure 5.6. On the other hand, the transient of the FF + PI_{GS} during a power step presents more overshoot compared to the FF + PI_K.

The same analysis can be made for the output voltage ramp-down tests, see subsection 5.3.2. It can be seen how the FF controller is not able to follow the reference power during a specific output voltage ramp-down, see Figure 5.8. Meanwhile, when the PI_K is added to the system, it is shown in Figure 5.9 that the compensator correction brings the output power to its reference value, also when a ramp-down on the output voltage is applied. Finally, when the PI_{GS} is implemented, the output power reaches its reference value faster than the case with constant PI controller, see Figure 5.10.

Concluding, from the experimental power dynamic results, the converter with the FF presents faster transients compared to the other two controllers. However, the FF lacks of steady-state accuracy which, it is improved by both implemented PI controllers.

6.3.2 Controller implementation

The implementation of the control strategy on a real laboratory setup has faced some challenges summarized in section B.1. Since nonidealities on a laboratory setup are unavoidable, the FF look up table was obtained by experimental data, which resulted in a "low resolution" FF with only 3 curves. For future purposes, one could derive an analytical expression between power and frequency that includes nonideal components to emulate the ideal converter results. The need of a compensator when the FF has lower resolution increases. For this reason, a characterization of the plant with FF should be done to optimize the compensator response.

Other important aspects are the voltage measurement circuit and current measurement circuit, which are a key components for voltage and current input signals to the controller. During the semester thesis inaccurate calibrations have led to repetition of experiments multiple times. In addition, the asynchronous ADC causes jitter which translates into wrong measurements being fed into the DSP and oscillations on the output current are generated. The fact of not disposing a bidirectional output voltage source brings about the need of a resistive load and placement of a diode. Due to this issue, output voltage disturbances or other related test are difficult to execute.

Chapter 7

Conclusions

This master thesis has investigated control aspects for a high power resonant converter. The optimal control architecture is based on a FF obtained by linearization of the non-linear power to frequency equations. Based on the results achieved on the simulation model, the control strategy has the characteristics of dead-beat performance.

The power tracking is accurate in the whole range of operation, from 0 to nominal power. The set-point bandwidth is favorable at low frequencies ($< 30Hz$), therefore, its suitable for wind power applications due to the considerable inertia of a WT.

Moreover, during voltage changes on the MVDC grid, the converter with the implemented FF is able to maintain the reference power with a short transient response. If a voltage dip occurs, the current is limited to avoid damage on the converter components. The rejection of output voltage disturbances shows an amplification on the output current at perturbation frequencies higher than 150Hz, caused by fast switching frequency correction. On the other hand, at lower frequencies, the harmonic rejection is achieved.

However, the implementation of a control system on a real setup brings challenges for controller design such as losses and non-idealites. Therefore, the FF is designed from experimental data and has lower resolution. As a result, the accuracy of the FF decreases and, a compensator is needed to reach proper power tracking. Additionally, due to the variable operating switching frequency, the compensator response needs to be gain scheduled. Experimental and simulation results from the non-ideal converter show poorer performance of the FF compared to the lossless converter model. Nonetheless, the inaccuracy of the FF is overcome with the compensator help.

Concluding, the chosen requirements for a high power DC-DC converter are achieved with the presented control strategy. Furthermore, the laboratory tests performed prove the FF design methodology presented in the thesis. However,

practical challenges of a real setup lead to further research on output choke impact, verification of output voltage harmonic rejection and, MV measurement circuit implementation.

7.1 Future work

- Development of the power to frequency curves that includes non-idealities present in the resonant tank, the medium frequency transformer and, the snubber circuit;
- Optimization of the FF search algorithm;
- Design of the compensator based on a experimental characterization of the plant and FF;
- Further investigation of the output choke impact on the control performance;
- Implementation of a setup with a bidirectional output voltage source in order to emulate a more realistic approach;
- Improvement on the measurement circuit design to achieve higher sensitivity;
- Validation of harmonic rejection, output voltage sag and further research such as short-circuit test;

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Appendix A

Open Loop Characterization

A.1 Circuit Characteristics

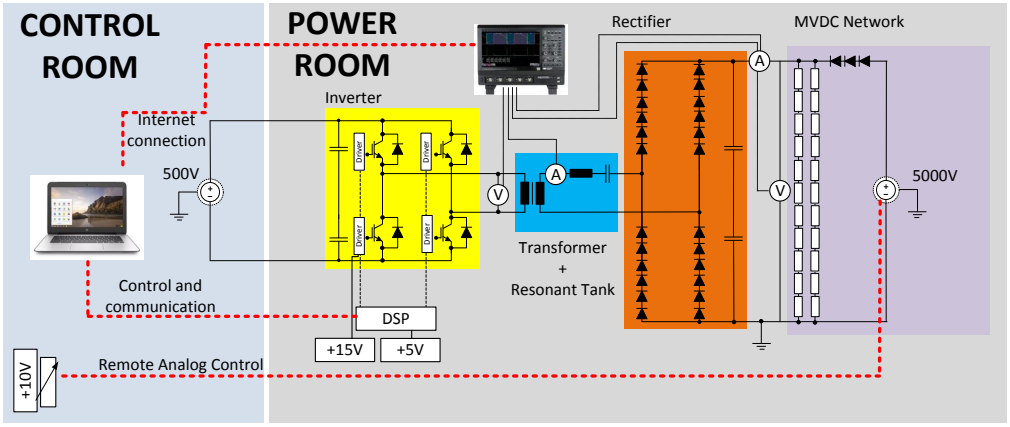


Figure A.1: Equivalent circuit of the laboratory 10 kW setup [10]

The laboratory setup used in this project and located in the MV laboratory at Aalborg University is illustrated in Figure A.1. Several voltage sources are required to run the setup in the proper way. The two GW Instek GPS-4303 sources are needed to supply 5 V to the DSP and 15 V to the gate drivers. Regarding the input and output voltages, KEYSIGHT N8957A and TECHNIX SR5KV-10kW have been used, respectively.

The model names of the equipment utilized for the laboratory work and their nominal values are presented in Table A.1, Table A.2 and Table A.3.

Table A.1: Voltage sources of the 10kW laboratory setup

Device	Nameplate	Nominal V [V]	Nominal I [A]	Nominal P [W]
Input DC source	KEYSIGHT N8957A	1500	30	15000
Output DC source	TECHNIX SR5KV-10KW	5000	2	10000
Gate Driver source	GW Instek GPS-4303	30	3	90
DSP source	GW Instek GPS-4303	30	3	90

The inverter of the laboratory setup is composed by two IGBT (SKM150GAR12T4, see Table A.2) which are controlled by the DSP output gate pulses. Regarding the output rectifier, in order to withstand the 5 kV output voltage, each leg of the rectifier is composed by twelve diodes in series. The nominal characteristics of each rectifier diode are shown in Table A.2.

Table A.2: Electronic Devices used in the 10kW laboratory setup

Device	Model	Characteristics
IGBT	SKM150GAR12T4	$1200V$, $150A$ [1]
Diode	SKKD16/46	1600 V, 45 A
Gate driver adaptor board	Board 1 Skyper 32Pro R	
Gate driver	Skyper 32Pro R	

The measurement equipment used for the open loop characterization is shown in Table A.3.

Table A.3: Measurement equipment used in the 10kW laboratory setup

Equipment	Model
Oscilloscope	Teledyne LeCroy HDO 4054
High voltage differential probe	Teledyne LeCroy ADP305, 6kV
Current probe	Tektronix TCP202A
Current measurement circuit	Built
Voltage measurement circuit	Built

A.1.1 Components parameters

The values of the passive elements present in the 10kW laboratory setup are illustrated in Table A.4. The inductance, L_r, and the capacitance, C_r, located in the resonant tank of the converter give a resonant frequency value of $1139.7Hz$. The input and output filter of the converter are both composed by two capacitor in series, see Figure A.1, and the equivalent series capacitance values are shown in Table A.4.

[1] $R_{CE}: 6.7m\Omega(25°C) to 10m\Omega(150°C)$

Moreover, in order to minimize overvoltages in the rectifier diodes, which usually occur during the turn-off, a snubber circuit has been implemented for each diode in the output rectifier of the converter, see Figure A.2. The parameter's values for the snubber circuits used in the 10 kW laboratory setup are shown in Table A.4.

Finally, the load of the laboratory setup is composed by two parallel leg of eleven resistor (R_l, see Table A.4) each therefore, the equivalent load resistance value is 2585Ω.

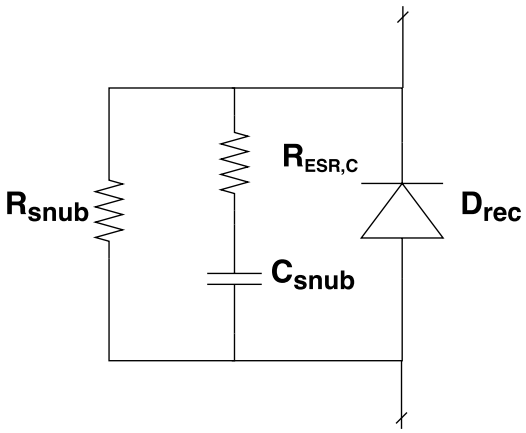


Figure A.2: Equivalent circuit of the snubber circuit in parallel with each rectifier diodes, non idealities included

Table A.4: Passive Elements

Component	Value
Resonant inductance, L_r	$137mH$
Resonant capacitance, C_r	$0.1\mu F$
Input filter capacitance, C_{in}	$3.3mF$
Output filter capacitance, C_f	$25\mu F$
Transformer turn ratio, N	$N_s : N_p = 10$
Snubber resistance, R_{snub}	$300k\Omega$
Snubber capacitance, C_{snub}	$1nF$
Load resistance, R_l	470Ω

A.1.2 Non Ideal Parameters

The equivalent circuit of the transformer for the 10 kW laboratory setup is illustrated in Figure A.3 where, the non ideal parameters values such as winding resistances, leakage inductances and magnetizing inductance are shown in Table A.5.

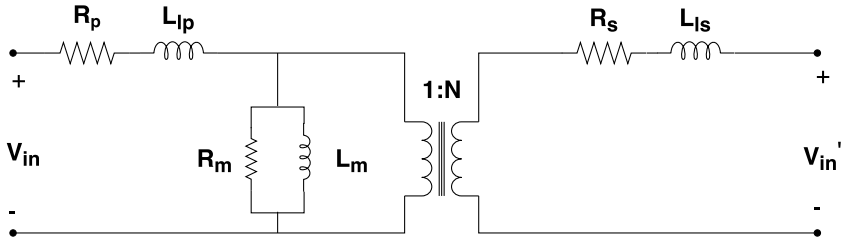


Figure A.3: Equivalent circuit of the transformer, non idealities included

Table A.5: Parameter values of the transformer

Parameter	Value
Turns ratio, N	10.22
Primary windings resistance, R_p	$48.43m\Omega$
Secondary windings resistance, R_s	5.08Ω
Leakage primary inductance, L_{lp}	$125\mu H$
Leakage secondary inductance, L_{ls}	$125mH$
Magnetizing inductance, L_m	$17.9mH$ [2]
Magnetizing resistance, R_m	$1.7k\Omega$

Moreover, the calculated equivalent series resistance (ESR) of the resonant tank and the snubber capacitor are presented in Table A.6.

Table A.6: Non ideal parameters

Parameter	Value
Busbar resistance on IGBTs	Neglectable
Screws resistance on IGBTs	Neglectable
ESR of the resonant tank	2.2Ω
ESR of the snubber capacitor	$1m\Omega$

[2]Calculated from magnetizing current waveforms

A.1.3 Nonidealities impact on the current

The impact of the transformer nonidealities on the primary current can be seen in Figure A.4 a) to c). Moreover, the reverse recovery of the diodes impact is illustrated in Figure A.4. Finally, oscillations caused at 18kHz between the resonant inductor and the snubber capacitance is depicted in Figure A.4 e) and the oscillations at 90kHz between the resonant inductor and its own stray capacitance in Figure A.4 f)

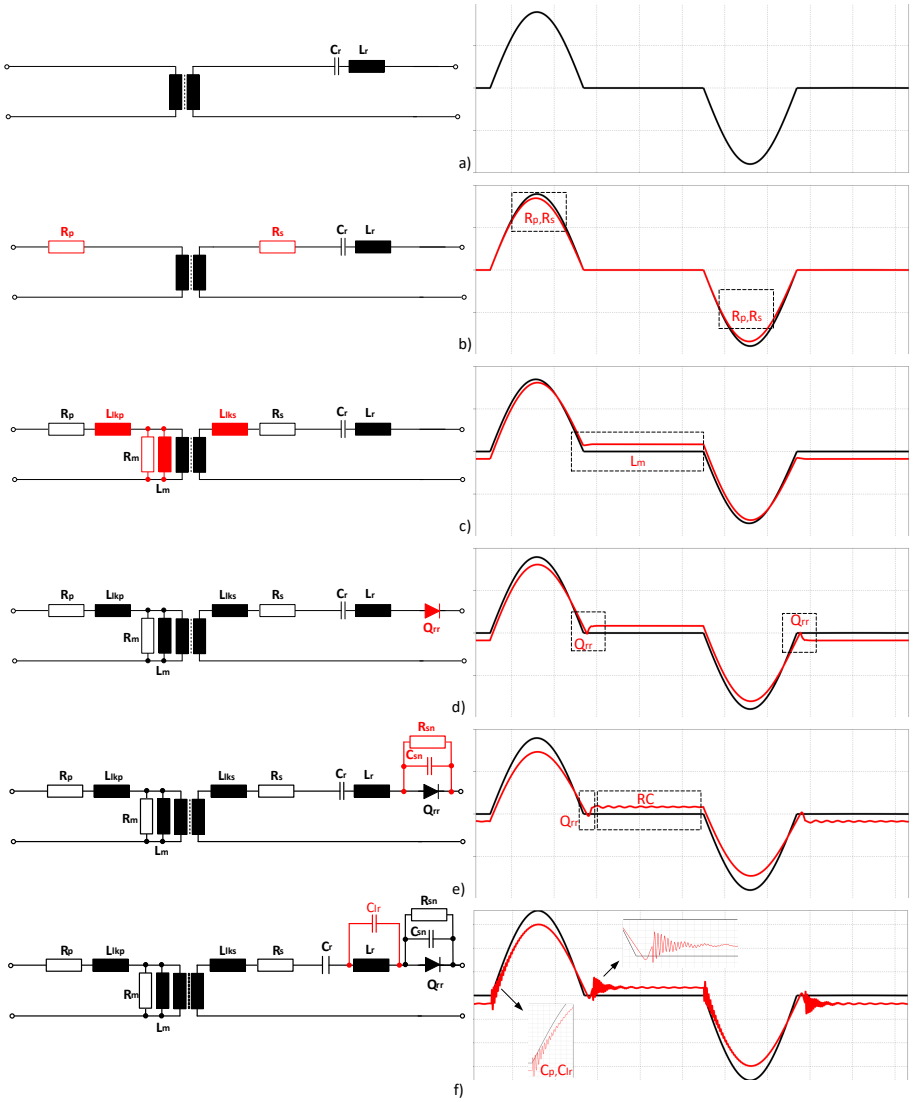


Figure A.4: Transition of primary current waveforms from lossless converter model to nonideal converter [21]

After the characterisation of the nonideal components is identified, a non ideal simulation model for 10kW is made based on the laboratory parameters. In Figure A.5 a comparison between laboratory current and voltage on the primary respect to the simulation Plecs model is shown. As it can be seen the phenomena described in Figure A.4 is visible and has a good matching with the simulation model built in Plecs.

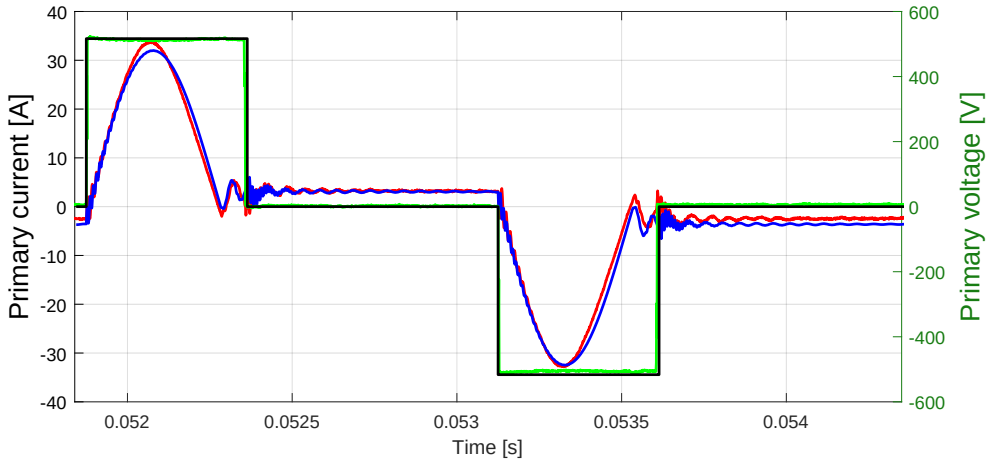


Figure A.5: Comparison between laboratory primary current and voltage respect to Plecs simulator model

Blue: Simulation primary current Red: Laboratory primary current
Black: Simulation primary voltage Green: Laboratory primary voltage

A.2 Measurements and control characterization

A.2.1 Sensors characterization

The sensors needed to control the converter are placed to collect the output voltage and the rectified current. A diagram with sensor position is shown in Figure A.6.

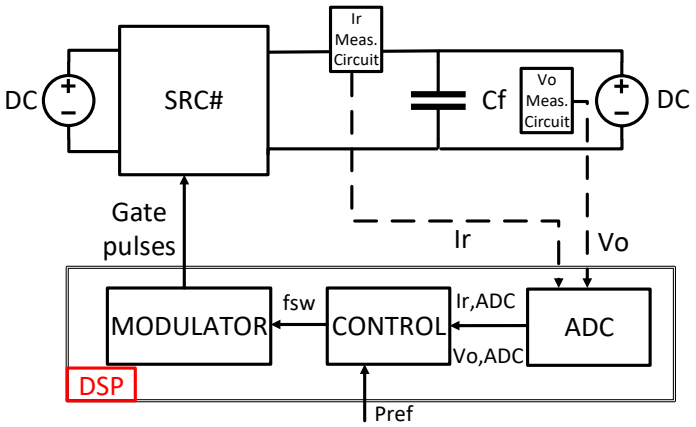


Figure A.6: Diagram of current and voltage measurement circuits

Output current sensor

The output current sensor transforms the rectified current with a high turn ratio transformer and a resistor in parallel, and, through an analog circuit scaler an analog signal between 0-3.3 V is being sent to the DSP Figure A.7. To avoid a possible electrical breakdown on the insulation, the current sensor is placed on the negative path of the rectified current.

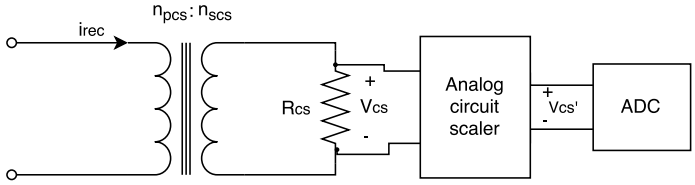


Figure A.7: Output current sensor equivalent circuit to the DSP

Table A.7: Parameters for current sensor circuit

n_{pcs}	n_{scs}	R_{cs} [ohm]
5	1000	100

The rectified current i_{rec} can be calculated with the relation in Equation A.1, and actual parameters are shown in Table A.7:

$$i_{rec} = (\frac{V_{cs}}{R_{cs}}) \cdot (\frac{n_{scs}}{n_{pcs}}) \tag{A.1}$$

The A/D conversion in the DSP transforms analog input signals into digital and viceversa, see A.2.2.

Output voltage sensor

The output voltage sensor transforms the output voltage across one resistor in the bank load with a high turn ratio transformer that scales down the voltage. With a parallel resistor on the secondary and through an analog circuit scaler, an analog signal between [0-3.3 V] is being sent to the DSP as it can be seen in Figure A.8.

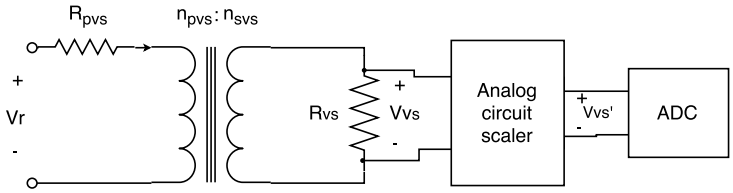


Figure A.8: Output voltage sensor equivalent circuit to the DSP

In order to find V_r, first the equivalent resistor of the measurement circuit is defined by Equation A.2:

$$R_{eqvs} = R_{pvs} + R_{vs} \cdot (\frac{n_{scs}}{n_{pcs}})^2 \tag{A.2}$$

Therefore, V_r can be calculated as in Equation A.3:

$$V_r = i_{pvs} \cdot R_{eqvs} = (\frac{V_{vs}}{R_{cs}}) \cdot (\frac{n_{scs}}{n_{pcs}}) \cdot R_{eqvs} \tag{A.3}$$

Where V_{vs} is the voltage at the analog circuit scaler terminals. Parameters for the voltage measurement circuit are shown in Table A.8:

Table A.8: Parameters for voltage sensor circuit

n_{pvs}	n_{svs}	R_{vs} [ohm]	R_{pvs} [ohm]
25000	1000	200	60000

The output voltage sensor is placed across one of the resistors in the bank load as shown in Figure A.9. Since the setup is composed by 11 resistors in series the equation that relates the V_r and V_{out} is described in Equation A.4.

$$V_{out} = V_r \cdot \frac{\sum_{n=1}^{10} R_n + \frac{R_{11} \cdot R_{eqvs}}{R_{11} + R_{eqvs}}}{\frac{R_{11} \cdot R_{eqvs}}{R_{11} + R_{eqvs}}} \tag{A.4}$$

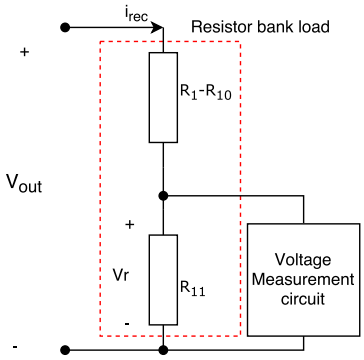


Figure A.9: Position of output voltage measurement in the load voltage divider

A.2.2 Digital Signal Processor

A digital signal processor (DSP), model TMS302F28379D, is used to implement the control algorithm in charge of generating the gate signals and the analog-to-digital (A/D) conversions of the scaled down measured values (I_{rec}, V_o).

TMS320F28379D Dual-Core Delfino^{TM} Microcontroller is a 32-bit controller designed for advanced closed-loop control application [22]. The main DSP code is composed by a loop which is interrupted by the ADC interrupt and the PWM interrupt, see Figure A.10 . Those interrupts are signals that causes the main loop to pause and shift to a different piece of code known as an interrupt service routine (ISR). The ADC interrupt is responsible to calculate the analog level of the digital measured variables and, update a summed value for each sampled data. On the other side, the PWM interrupt is in charge to make the average of the measured variables, implement the eventual controller frequency correction, update the PWM period of both gate inverter pulses. In Figure A.10 is represented the work flow of the DSP code implemented in the 10 kW laboratory setup.

PWM characterization

Three enhanced pulse width modulator (ePWM) modules are necessary to generate the gate pulses and the A/D conversions. All the ePWM modules are synchronized with the clock frequency of 200 MHz (f_{SYSCLK}) and, through specific registers, each module can be configured at a desired PWM frequency (f_{PWM}) and operating mode, see table.

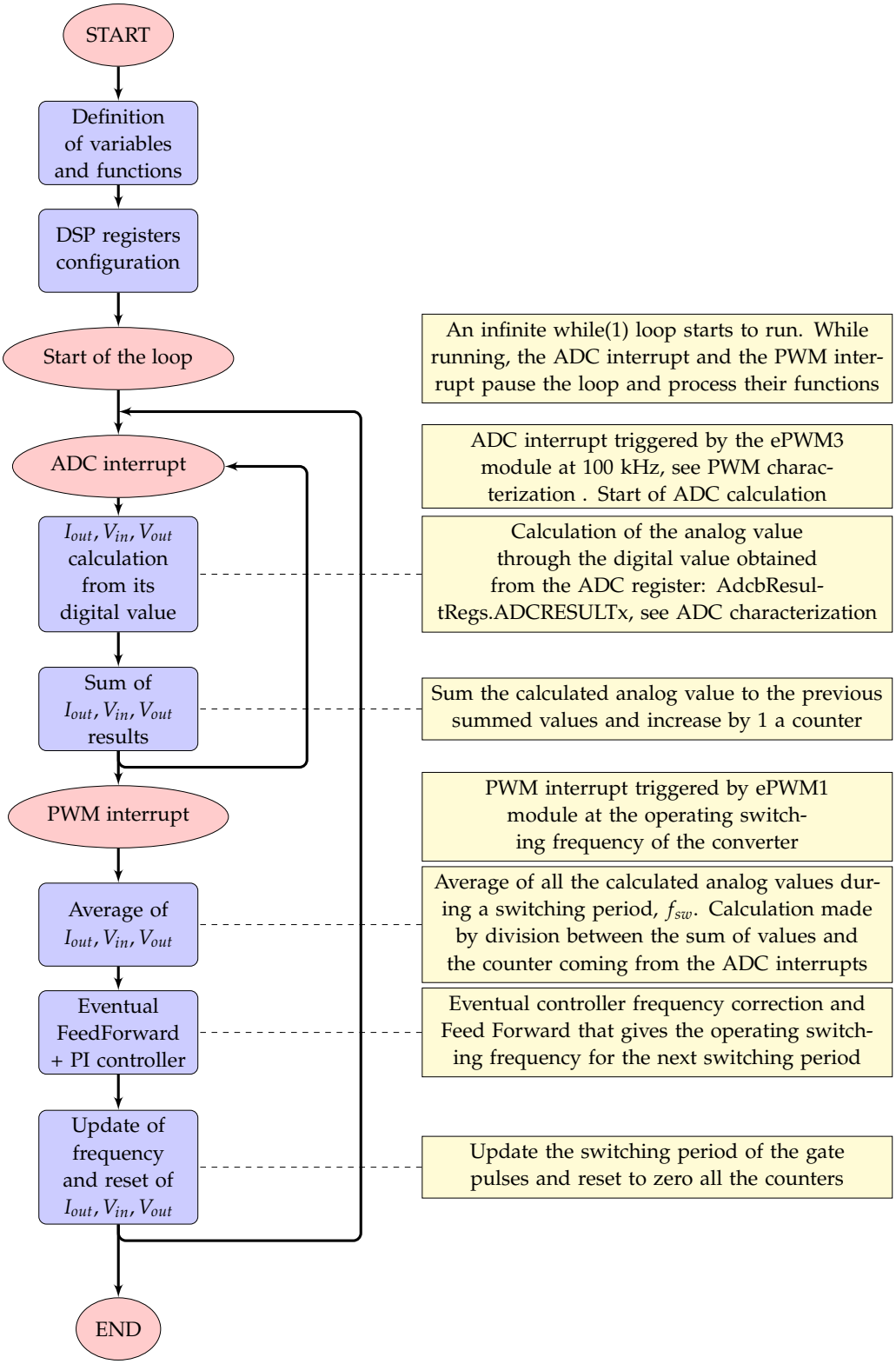


Figure A.10: DSP script working principle

The operating principle of each ePWM consists of a comparison between an integer counter (TBCTR) increasing at a specific frequency (f_{TBCLK}) and a fixed configurable reference (CMPA). The counter is working in up-down count mode (CTRMODE) therefore, TBCTR goes from 0 to its highest level and then back to 0 again in one PWM period (T_{PWM}), see Figure A.11. All three ePWM modules work with the same operating principle and, the output of each ePWM is defined when TBCTR reach the same level of CMPA. The EPWM output is low when $TBCTR = CMPA$ on down-count mode and is high when the same happen on up-count mode.

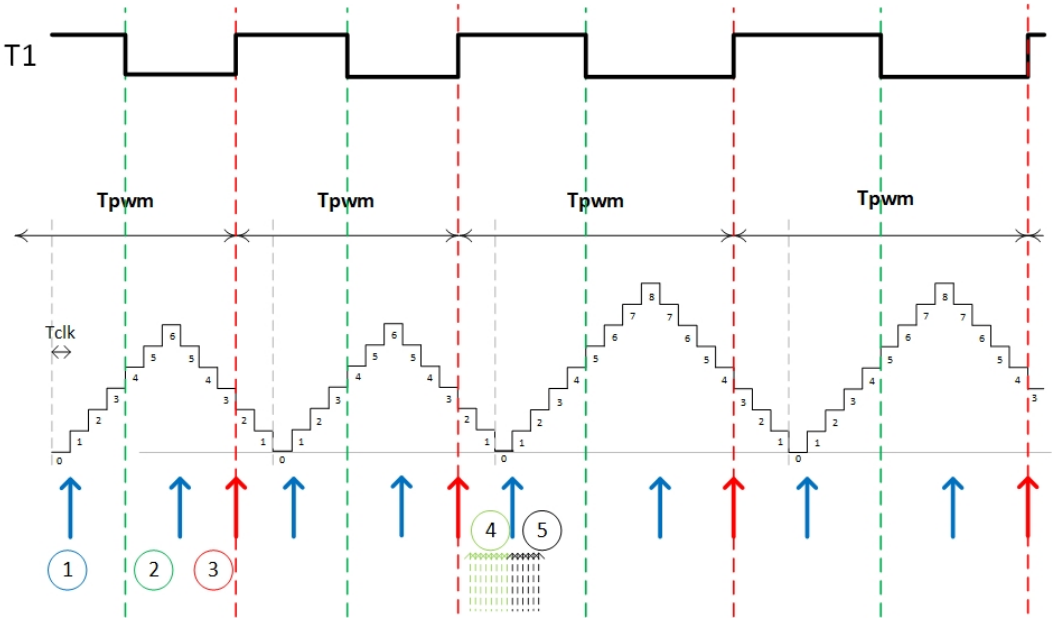


Figure A.11: Operating principle of the ePWM on the DSP

The desired frequency of the PWM pulses is configured by deciding f_{TBCLK} and setting a specific value on the Time Base Period register (TBPRD) which, it represents the highest value that TBCTR can arrive. The PWM frequency is then calculated with Equation A.5.

$$f_{PWM} = \frac{f_{TBCLK}}{2 \cdot TBPRD} \tag{A.5}$$

where f_{TBCLK} is obtained from f_{SYSCLK} and three scaling factors, see Equation A.6.

- EPWMCLKDIV: EPWM Clock Divide Select
- CLKDIV: Time Base Clock Pre-Scale Bits
- HSPCLKDIV: High Speed Time Base Clock Pre-Scale Bits

$$f_{TBCLK} = \frac{f_{SYSCLK}}{EPWMCLKDIV \cdot CLKDIV \cdot HSPCLKDIV} \tag{A.6}$$

As example, Figure A.11 illustrates the mode of operation of the ePWM1 module that generates the gate signals for the first leg of the inverter.

In Table A.9, the function and the switching frequency of each ePWM modules is defined. ePWM1 and ePWM3 are generating the interrupts for the averaging and the ADC conversion respectively.

Table A.9: ePWM modules characteristics

Module	Function	TBPRD	Dividers	Switching Frequency	Trigger Interrupt
ePWM1	Master Inverter Leg pulses	$[0-10^4]$	/10	$[0-1000]Hz$	Down-count mode
ePWM2	Slave Inverter Leg pulses	$[0-10^4]$	/10	$[0-1000]Hz$	No trigger
ePWM3	ADC conversion pulses	1000	/1	100 kHz	Down-count mode

A/D characterization

The ADC module of the DSP is a sucessive approximation (SAR) style ADC with configurable resolution of 16 bits or 12 bits and it consists of a single sample-and-hold (S/H) circuit.[refMANUAL.DSP] The operating conditions for the A/D used in the laboratory setup are:

- 12-bits resolution
- Single-ended mode
- Synchronous operation
- Sampling frequency: $100kHz$, from the ePWM3 interrupts
- Sample-hold acquisition time: $75ns$

The mode of operation of a SAR style ADC can be summarized as following. The analog input variable is held on a track/hold circuit for a period of time that last enough to let the binary search algorithm to end. The N-bit register is responsible to set v_{ADC} in order to be compared with v_{IN}. First, the register is initialized to give half of the reference voltage, $V_{REF} = 3V$. If v_{IN} is higher than v_{ADC}, the output of the comparator is high and the MSB of the register is kept high. On the other hand, if v_{IN} is lower than v_{ADC}, the output is low and the MSB is set low. The iteration then move to the next bit down and another comparison is made until the SAR logic reaches the LSB of the N-bit register. Once the last bit is set, the ADC conversion is complete and the output is available from the N-bit register.

In order to implement the ADC conversion on the DSP, the analog variable that need to be converted into digital has to be scaled down to a voltage value between

0 V and 3 V, see subsection A.2.1. The ADC is set to 12-bits resolution which it means that the digitalized value can vary from 0 to 4095 therefore, Equation A.7 gives the conversion between the analog value and the digitalized one.

$$ANALOG = CAL_y - DIGITAL \cdot \frac{3}{2^{12} - 1} \cdot CAL_x \tag{A.7}$$

Where CAL_y and CAL_x are calibration parameters for offset and slope respectively.

Appendix B

Laboratory test procedures

The laboratory test procedures for each analyses case used in chapter 5 are explained here in detail. Moreover, tests performed with some limitations are shown in subsection B.3.2 in order to extract its valuable information and as a reference for future improvements.

B.1 Experimental setup challenges

Up to four iterations have been performed for each type of test in order to reach satisfactory results that are meaningful to validate our control strategy. In general, the lack of experience regarding laboratory work on a 10kW and 5kV setup, and, the complexity of the converter have been the main reasons. Some of the challenges faced are briefly presented here:

- Nonidealities impact:
  - Difficulty to derive a mathematical model including the nonidealities, therefore experimental data was used.
  - Relate ideal ΔV to the laboratory ΔV when frequency dependent components change its behaviour and cause different voltage drops.
  - Non desired oscillations due to stray capacitance on the resonant inductor and snubber capacitance.
- Sensitivity of the protection for the output voltage source when exceeding 5kV
- The need of a resistive load on the output due to the lack of a bidirectional output voltage source.
- Inaccuracy of the measurement circuits and long connection cables to the DSP

- Limit on the DSP memory when recording data or extending the look up table for the FF.
- Asynchronous ADC that causes oscillations due to the jitter.
- Inability to test voltage steps or proper voltage ramps due the use of a manual regulator (potenciometer) to set the voltage.
- Inability to test voltage disturbances due to the lack of a serial connection with the output voltage source. Moreover, load disturbances were tried but the relays could not withstand.

B.2 Laboratory procedures for the results

B.2.1 Steady-state performance

The steady-state performance test has been carried out as depicted in Figure B.1. The main purpose of this test was to determine the accuracy of the FF and compare it to a close loop system such as $FF + PI_K$ and $FF + PI_{GS}$. To reach this goal data was recorded at each kW set-point power reference and analyzed afterwards, with an output voltage set constant at 4.9kV and 4.95kV respectively for each test.

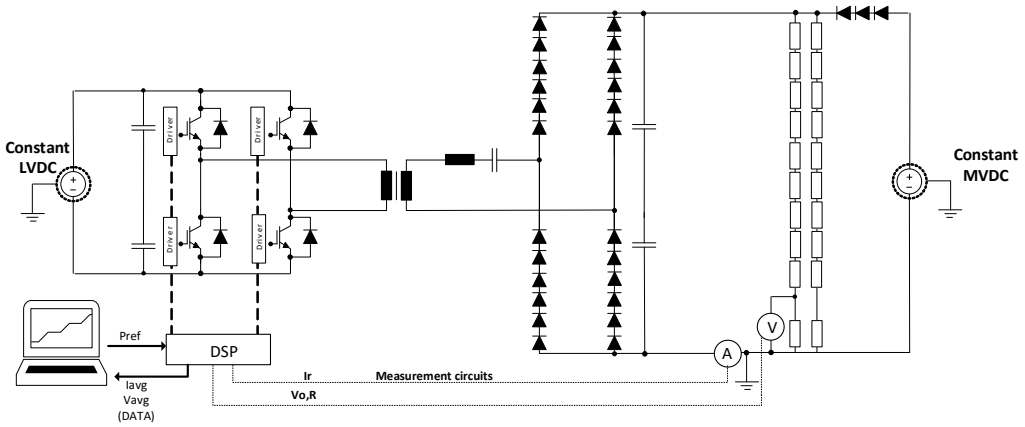


Figure B.1: Probes and measurement circuit positions for the steady-state test

Data recorded from the DSP:

- Output current averaged every switching cycle
- Switching frequency

Data recorded from the oscilloscope:

- Output voltage

Another test not depicted in the results chapter to analyze the steady-state performance during power ramps when an inductor is included is shown here:

B.2.2 Power steps

The power steps test performed in the laboratory followed the approach in Figure B.2. A change in the reference power is applied through the DSP which then is captured on the oscilloscope. The output voltage was kept constant at 4.9kV during the test. When the change in the power is applied a vector of 250 values of recorded data for DSP is created and then copied into the local PC while running the converter. A GPIO pin that gives an impulse from the DSP was set in order to record the timing of the power step on the oscilloscope.

Data recorded from the DSP:

- Output current averaged every switching cycle
- Switching frequency

Data recorded from the oscilloscope:

- Output voltage
- GPIO pin (impulse signal from the DSP) to record time

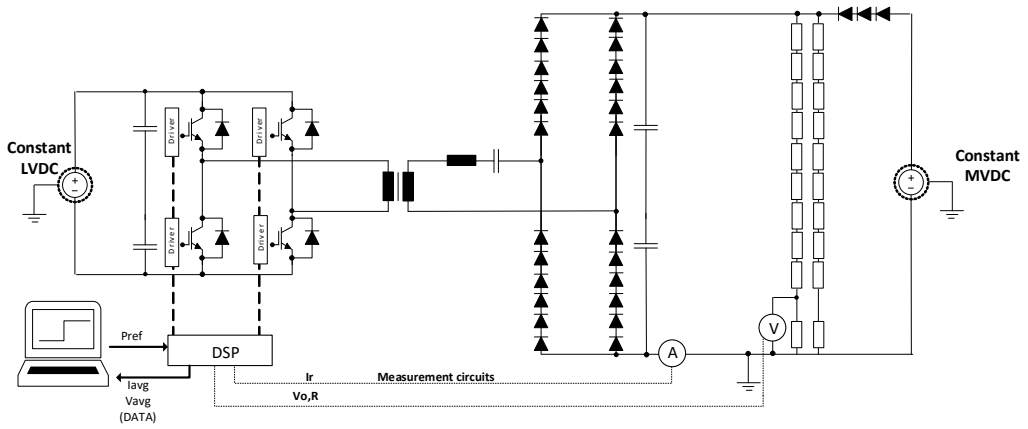


Figure B.2: Probes and measurement circuit positions for the power step test

B.2.3 Voltage ramp

The output voltage ramp test is depicted in Figure B.3. Only ramps down were tested in order to not trip the MV laboratory protection. The procedure followed this steps: A control strategy was on steady-steady at a specific reference power and 10 values were continuously recorded, then a "trigger" on the DSP voltage was set in order so when this would be activated the DSP would record the data up to the 250 values. A GPIO pin that gives an impulse from the DSP was set in order to record the timing of the voltage ramp on the oscilloscope. The reference power for this test was set constant at 2.5kW.

Data recorded from the DSP:

- Output current averaged every switching cycle
- Output voltage averaged every switching cycle
- Switching frequency

Data recorded from the oscilloscope:

- Output voltage
- GPIO pin (impulse signal from the DSP) to record time

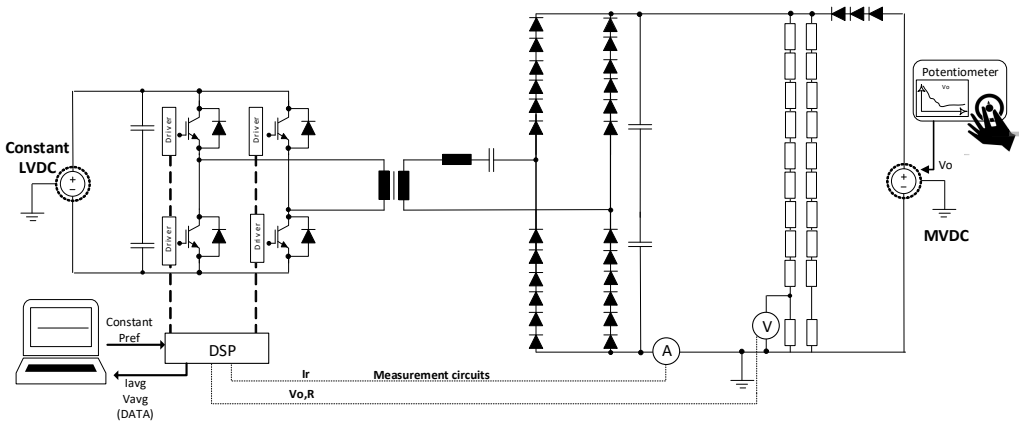


Figure B.3: Probes and measurement circuit positions for the voltage ramp test

B.3 Laboratory test with limitations

B.3.1 Power ramps

A test performing power ramps from 2kW to 8kW with slopes of 2kW/s was made with each type of controller. The approach for this test is shown in Figure B.4. In this test an inductor on the output was placed in order to record data from the oscilloscope since the DSP recording is limited to 250 samples.

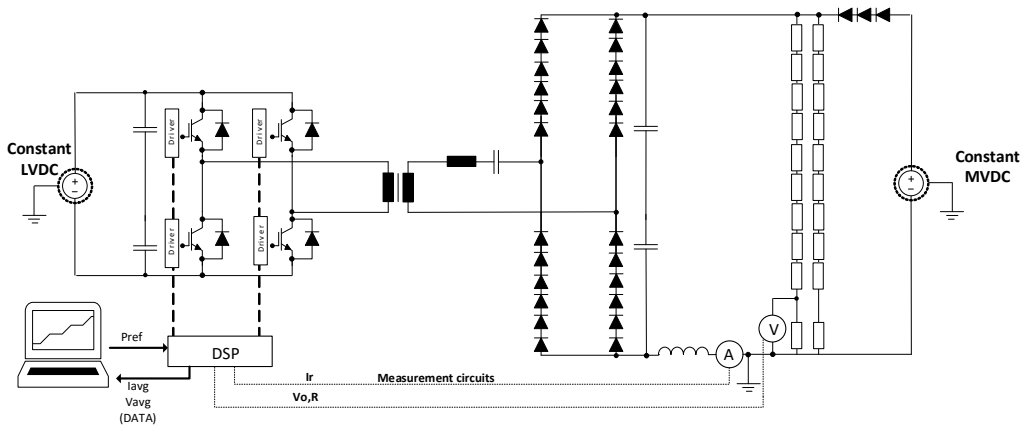
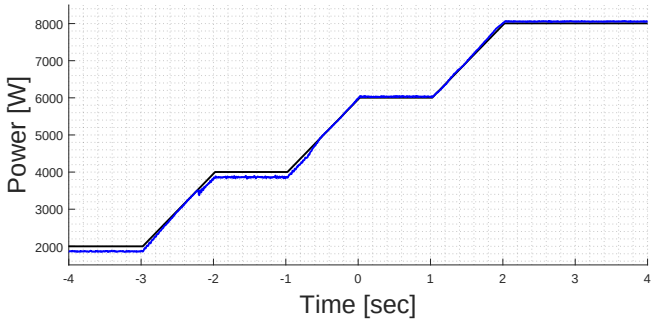
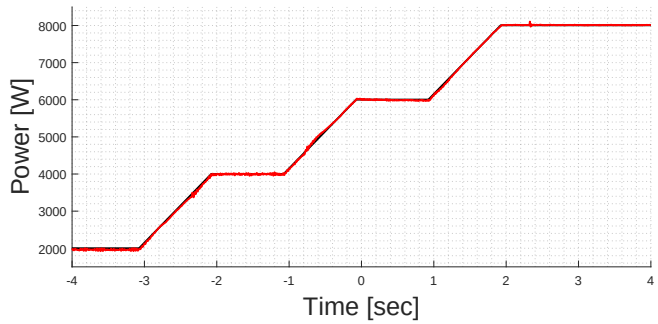


Figure B.4: Probes and measurement circuit positions for the power ramp test

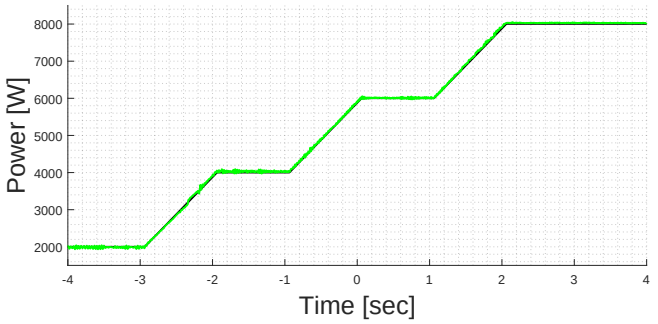
As it can be seen in Figure B.5a the FF steady-state error is present at low power but is able to follow the ramps up which implies that the linearization performed is accurate enough. On the other hand, both closed loop tests with a compensator in Figure B.6a and Figure B.6b follow the reference power nicely with low error.



(a) Power ramp test with FF control. Output power (blue) and reference power (black)



(a) Power ramp test with $FF + PI_K$ control. Output power (red) and reference power (black)



(b) Power ramp test with $FF + PI_{GS}$ control. Output power (green) and reference power (black)

B.3.2 Voltage ramps

With the procedure described in subsection B.2.3 and showed in Figure B.3 another test at 8kW was performed. However, an issue was detected on the voltage measurement circuit when running the DSP code with the algorithm for FF and compensator. The averaged output voltage was calculating higher values than the ones measured from the oscilloscope. However, this issue did not happen when the converter was ran open loop and the measurement circuit worked correctly.

According of how the search algorithm is built, at low power reference, the look up table makes the search faster than at high power. Moreover,the switching period at low power is higher than at high power. This two factors cause that the ratio between processing time and switching time increase significantly. For this reason, the suspicion is that the number of samples for the voltage average for the DSP are reduced while the total sum of collected voltages remains the same. As a result, at high power and with the FF loop working the averaged output voltage is higher than what should be.

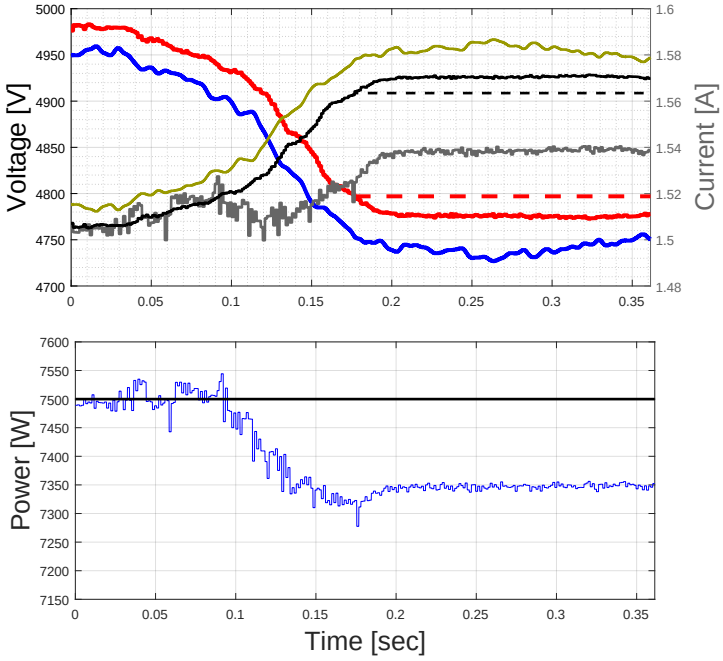


Figure B.7: Experimental results of the FF dynamic performance during voltage ramp down. SRC# operated in CCM1-Hybrid

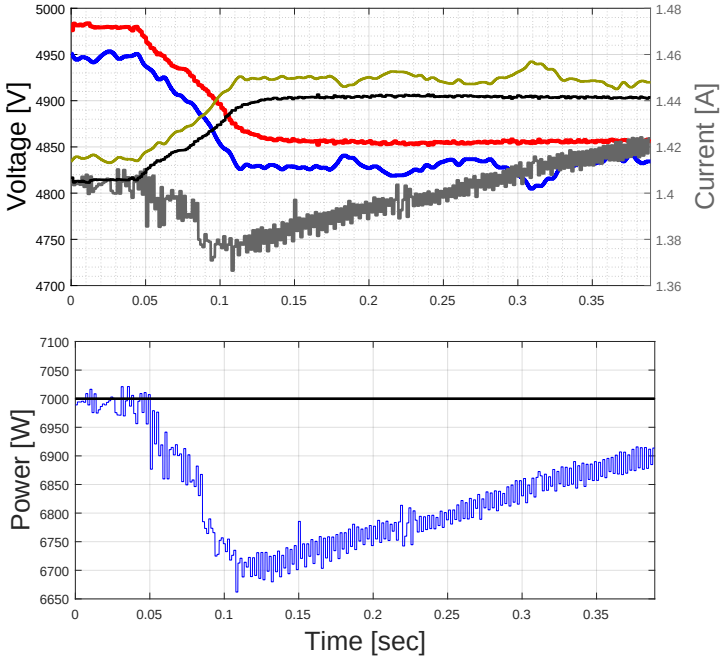


Figure B.8: Experimental results of the FF + PI_K dynamic performance during voltage ramp down. SRC# operated in CCM1-Hybrid

Blue: V_o, oscilloscope (Top), P_o (Bottom) Red: $V_{o,avg}$, DSP
Black: I_{ref} (Top), P_{ref} (Bottom) Grey: $I_{o,avg}$, DSP

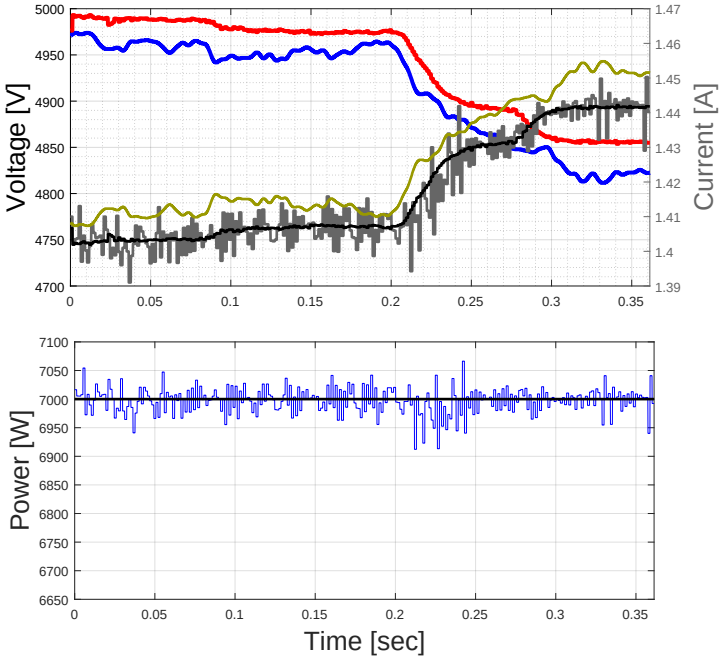


Figure B.9: Experimental results of the FF + PI_{GS} dynamic performance during voltage ramp down. SRC# operated in CCM1-Hybrid

Blue: V_o, oscilloscope (Top), P_o (Bottom) Red: $V_{o,avg}$, DSP
Black: I_{ref} (Top), P_{ref} (Bottom) Grey: $I_{o,avg}$, DSP

B.3.3 Voltage disturbance

The voltage disturbance test did not succeed to obtain any relevant data to prove the output voltage harmonics rejection predicted from simulations in section 5.4. One possibility could be to program the output voltage source with a serial connection in order to try to generate a sine signal on top of the 5kV DC, however this was not performed. Instead a load disturbance trial was intended to "emulate" a voltage disturbance on the output so the action of the controller could be seen. This test was tried according to Figure B.10, trying both to short one of the load resistors with an IGBT and a contactor. However, due to the sensitivity of the laboratory protection and not proper switch no relevant data was acquired.

B.3.4 Set-point tracking bandwidth

The set-point tracking bandwidth test consisted on comparing the output power to a triangular reference power in amplitude and phase for a certain range of frequencies from 2 to 50Hz. However, this test was performed with an inductor on

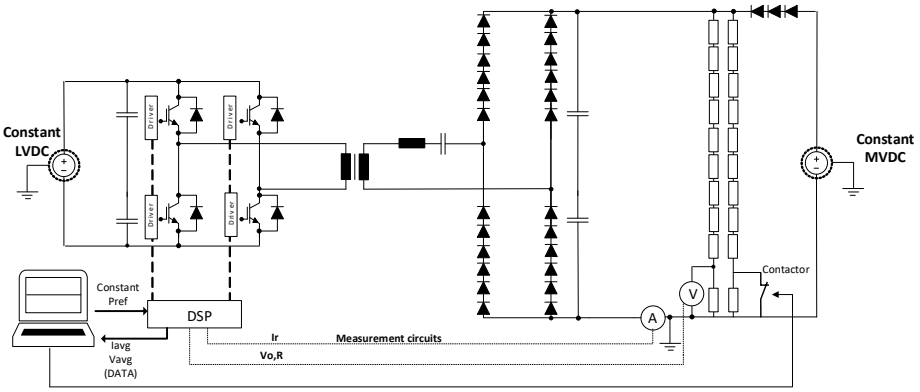


Figure B.10: Probes and measurement circuit positions for voltage disturbance test

the output and the data collected does not represent the bandwidth tracking of the plant and controller but, also with the filter included.

Even if the procedure does not correspond to what was performed in simulation in section 5.2 some valuable information can be extracted and future improvements can be done based on this.

The amplitude error is calculated respect to the total value of the peak of the triangular. As it can be seen in Figure B.12 when applying a triangular reference power at low frequencies the output power has low error in all three cases. The error decreases as the base power is higher. However, when the set-point tracking frequency is at the resonant of the filter the amplitude of the output power (after the filter) is amplified significantly and becomes low again at 50Hz. One significant finding is that the impact of the gain scheduling PI to the output power of the filter is amplifying the error when frequencies are high.

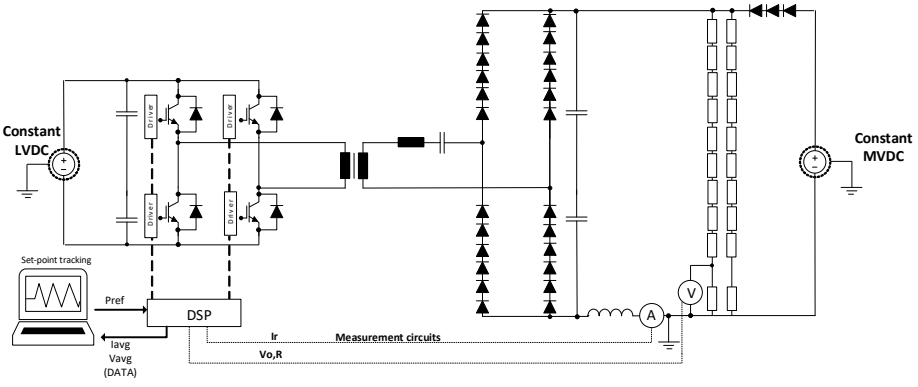
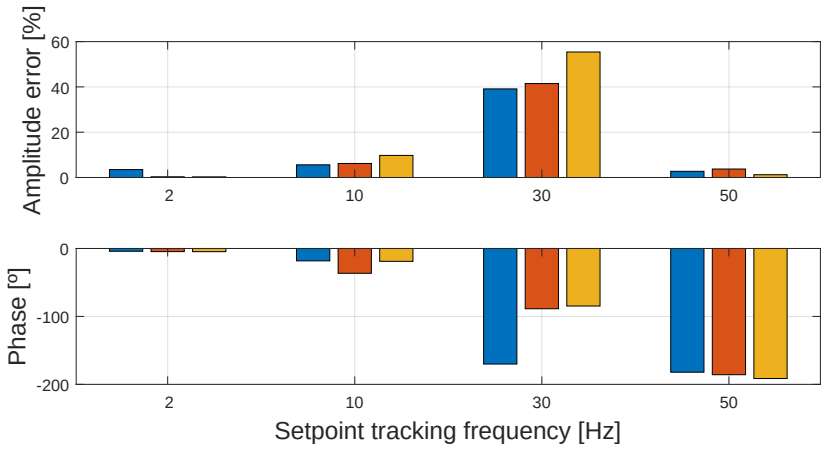
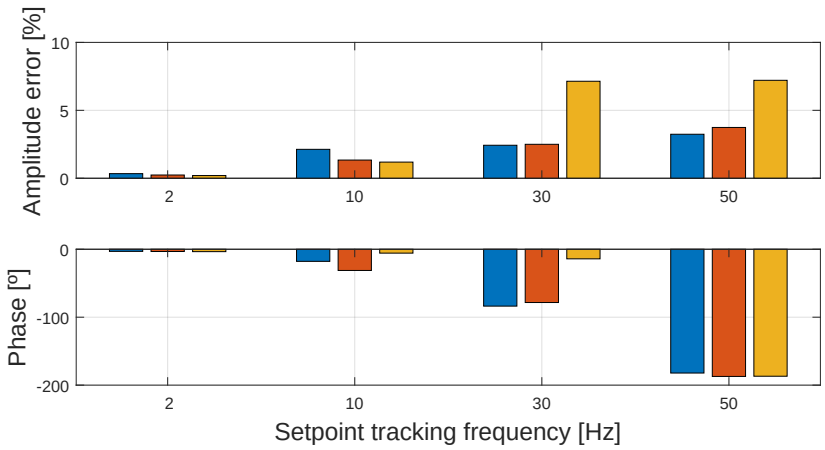


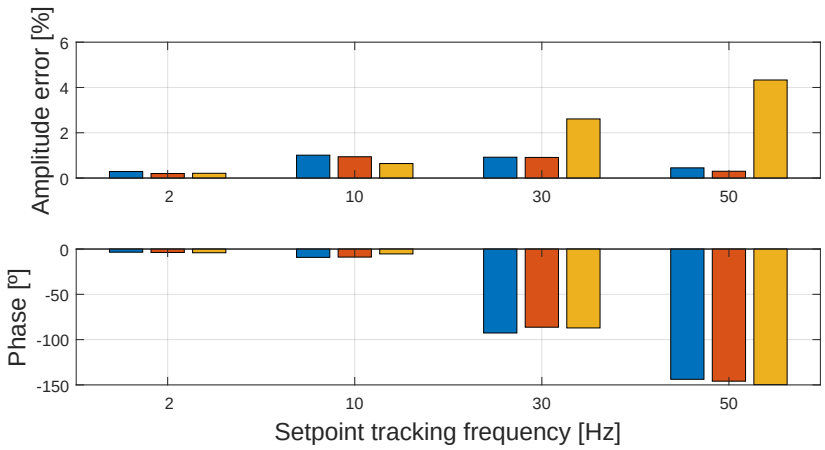
Figure B.11: Probes and measurement circuit positions for the set-point tracking bandwidth test with filter inductor



(a) Set-point tracking bandwidth at 2500W base power. Experimental results



(b) Set-point tracking bandwidth at 5600W base power. Experimental results



(c) Set-point tracking bandwidth at 8500W base power. Experimental results

Figure B.12: Amplitude and phase between output power and reference power
Blue: FF Red: FF + PI Yellow: FF + PI_{GS}

Appendix C

Derivation of the mathematical model

From previous work from the authors of this thesis, presented in [14] [1], it is developed the mathematical model of the SRC# operating in CCM1-hybrid. Moreover, the derivation of the small-signal model of the SRC# is briefly described. In particular, the followed method is based on means of discrete time modeling technique, state plane analysis and, linearization of state-space model.

C.1 Mathematical model of the SRC#

The mathematical model is obtained by evaluating the considered state variables between two different circuit states, see Figure C.1 and Figure C.2.

Where the first event, k, presents three sub-intervals:

- $t_{0(k)}$-$t_{1(k)}$, sub-interval T_1: T_1 and T_4 are ON
- $t_{0(k)}$-$t_{1(k)}$, sub-interval X: no conduction
- $t_{0(k)}$-$t_{1(k)}$, sub-interval Q_1: D_1 and T_3 are ON

The second event, k+1, presents three sub-intervals:

- $t_{0(k+1)}$-$t_{1(k+1)}$, sub-interval T_2: T_2 and T_3 are ON
- $t_{0(k+1)}$-$t_{1(k+1)}$, sub-interval X: no conduction
- $t_{0(k+1)}$-$t_{1(k+1)}$, sub-interval Q_2: D_2 and T_4 are ON

The current flow for each considered sub-interval is shown in Figure C.2. The state variables of the SRC# are the current and the voltage across the resonant tank, V_{Cr} and I_r respectively.

A small ripple approximation has been made by considering the input and output voltages constant during each sub-interval of events k and k+1. Therefore, equivalent circuits for each considered interval are illustrated in Figure C.3.

[1] It may not be easily accessible for non AAU members and need to ask the AAU project bank responsible, that is the reason why many contents are presented in this Appendix C

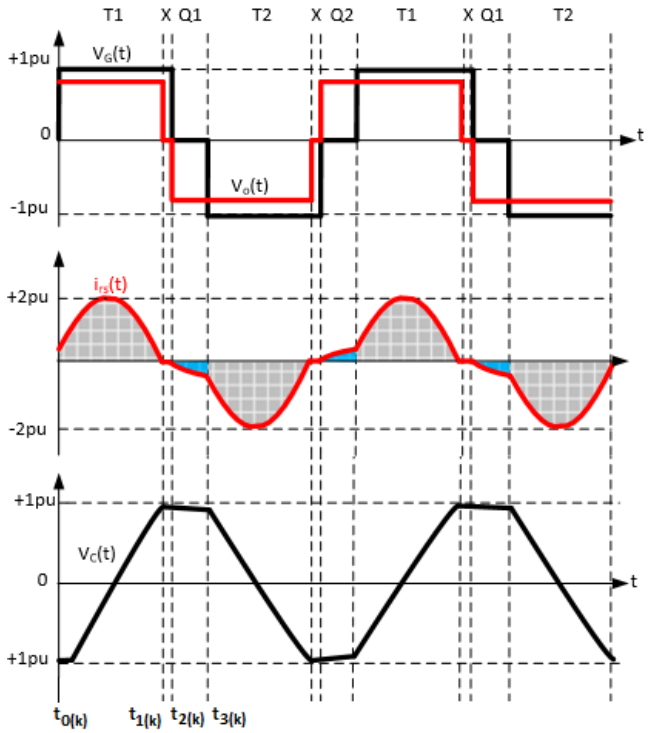


Figure C.1: Input voltage, output voltage, resonant current and tank voltage waveforms during CCM1-Hybrid [13]

From Figure C.3a, T_1 sub-interval, relevant circuit equations are obtained, see Equation C.1 and Equation C.2 .

$$v_g = L_r \frac{di_r}{dt} + v_{cr} + v_o \tag{C.1}$$

$$i_r = C_r \frac{dv_{cr}}{dt} \tag{C.2}$$

where: $v_g = V_{g,0(k)}$ $v_o 0 = V_{o,0(k)}$

By solving those equations, the expressions for the voltage across the tank capacitor and the resonant current are obtained.

$$\begin{aligned} v_{Cr} =& V_{g,0(k)} - \left(V_{g,0(k)} - V_{o,0(k)} - V_{Cr,0(k)}\right) cos(\omega_r t') \\ &+ I_{r,0(k)} Z_r sin(\omega_r t') - V_{o,0(k)} \end{aligned} \tag{C.3}$$

$$i_r = \frac{1}{Z_r}\left(V_{g,0(k)} - V_{o,0(k)} - V_{Cr,0(k)}\right) sin(\omega_r t') + I_{r,0(k)} cos(\omega_r t') \tag{C.4}$$

where: $Z_r = \sqrt{\frac{L_r}{C_r}}$; $\omega_r = \frac{1}{\sqrt{L_r C_r}}$ and, $t' = t - t_{0(k)}$

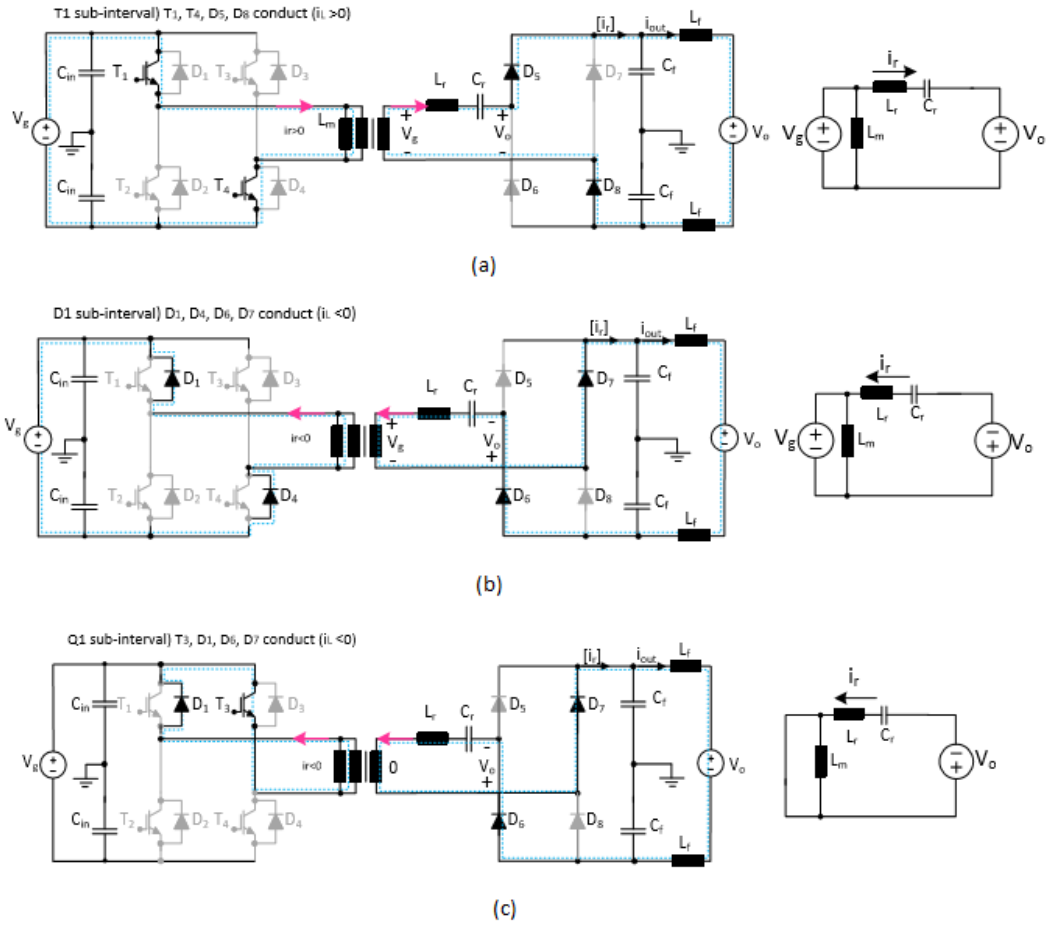
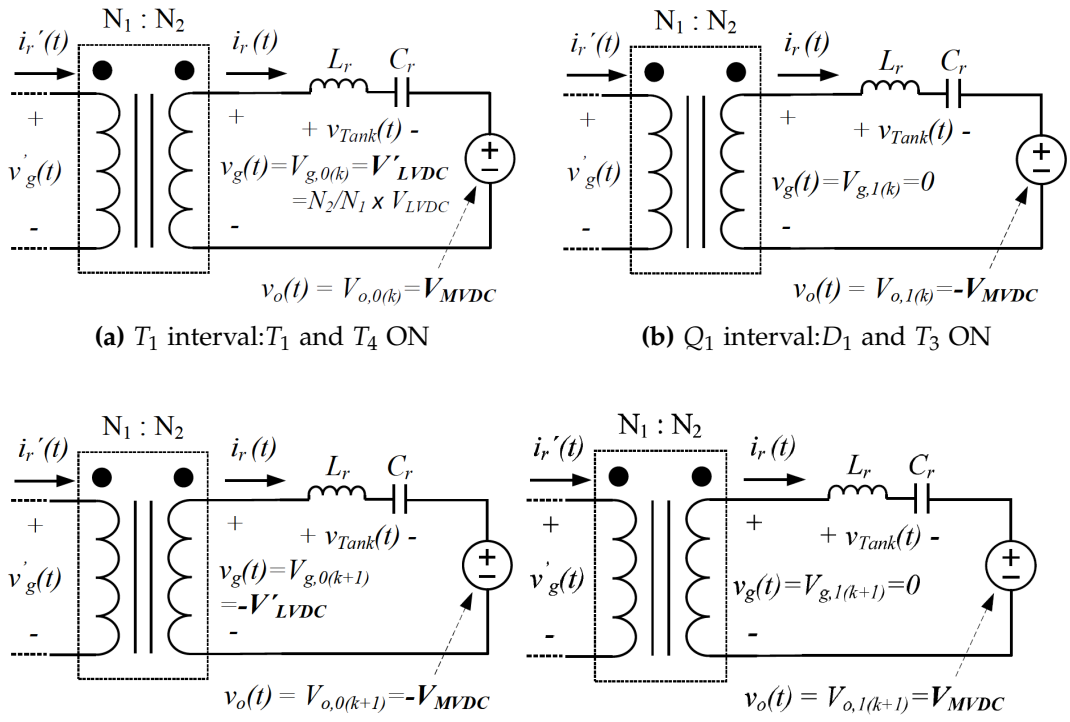


Figure C.2: Sub-intervals equivalent circuits during CCM1-Hybrid [13]

A sinusoidal current starts to flow at the resonant frequency until it reaches zero, causing the natural turn off of the IGBTs at $t_{1(k)}$ time instant. Therefore, the relationship between the state variables at the beginning and at the end of T_1 sub-interval can be found.

When: $t = t_{1(k)} \quad \Rightarrow t' = t_{1(k)} - t_{0(k)}$, $v_{Cr}(t_{1(k)}) = V_{Cr,1(k)}$, and $i_r(t_{1(k)}) = 0$

$$\begin{aligned} V_{Cr,1(k)} =& V_{g,0(k)} - \left(V_{g,0(k)} - V_{o,0(k)} - V_{Cr,0(k)}\right) cos(\omega_{rs}\beta_k) \\ &+ I_{r,0(k)} Z_r sin(\omega_{rs}\beta_k) - V_{o,0(k)} \end{aligned} \tag{C.5}$$



(a) T_1 interval:T_1 and T_4 ON

(b) Q_1 interval:D_1 and T_3 ON

(c) T_2 interval:T_2 and T_3 ON

(d) Q_2 interval:D_2 and T_4 ON

Figure C.3: Equivalent circuits during different sub-intervals of the SRC # in CCM1-Hybrid [10]

$$0 = \frac{1}{Z_r}\left(V_{g,0(k)} - V_{o,0(k)} - V_{Cr,0(k)}\right) sin(\omega_r t_{1(k)}) + I_{r,0(k)} cos(\omega_r t_{1(k)}) \tag{C.6}$$

$$tan(\omega_{rs}\beta_k) = -\frac{Z_r I_{r,0}}{V_{g,0(k)} - V_{o,0(k)} - V_{Cr,0(k)}} \tag{C.7}$$

where: $\omega_s(t_{1(k)} - t_{0(k)}) = \beta_k$, $\omega_r(t_{1(k)} - t_{0(k)}) = \frac{\omega_r}{\omega_s}\beta_k = \omega_{rs}\beta_k$

During the next interval, X, the rectifier diode bridge is reverse biased until the switch T_3 turns on, at the time instant $t_{2(k)}$. Then, no current flows through the tank and, the voltage across the capacitor stays constant during X sub-interval:

When: $t = t_{2(k)} \Rightarrow v_{Cr}(t_{2(k)}) = V_{Cr,2(k)} = V_{Cr,1(k)}$, $i_r(t_{3(k)}) = I_{r,3(k)} = I_{r,2(k)} = 0$

And, according to the pulse removal control technique:

$$\omega_s \cdot (t_{2(k)} - t_{1(k)}) = \omega_s \cdot (\frac{T_r}{2} - \beta_k) = \frac{\pi - \beta}{\omega_{rs}} \tag{C.8}$$

Finally, at the time instant $t_{2(k)}$, T_3 turns ON and starts to conduct. As a result, zero voltage is applied to the turbine side of the converter and a negative current starts to increase. So, the equivalent circuit in Figure C.3b is considered and, by Kirchoff's voltage law:
For $t_{2(k)} \leq t \leq t_{3(k)}$ (D_1, T_3 ON)

$$0 = L_r \frac{di_r}{dt} + v_{Cr} - v_o \tag{C.9}$$

$$i_r = C_r \frac{dv_{cr}}{dt} \tag{C.10}$$

From solution of the above equations,

$$v_{Cr}(t') = \left(V_{o,1(k)} + V_{Cr,1(k)}\right) cos(\omega_r t') - V_{o,1(k)} \tag{C.11}$$

$$i_r(t') = -\frac{1}{Z_r}\left(V_{o,1(k)} + V_{Cr,1(k)}\right) sin(\omega_r t') \tag{C.12}$$

$t' = t - t_{2(k)}$

Therefore, at the time instants $t_{3(k)}$:
When: $t = t_{3(k)} \quad \Rightarrow t' = t_{3(k)} - t_{2(k)}$, $v_{Cr}(t_{3(k)}) = V_{Cr,3(k)}$, $i_r(t_{3(k)}) = I_{r,3(k)}$

also,
$\omega_s(t_{3(k)} - t_{2(k)}) = \alpha_k$
$\omega_r(t_{3(k)} - t_{2(k)}) = \frac{\omega_r}{\omega_s}\alpha_k = \omega_{rs}\alpha_k$

$$I_{r,3(k)} = -\frac{1}{Z_r}\left(V_{o,1(k)} + V_{Cr,1(k)}\right) sin(\omega_{rs}\alpha_k) \tag{C.13}$$

Replacing Equation C.5 in Equation C.13, and considering $V_{o,1(k)} = -V_{o,0(k)}$:

$$\begin{aligned} I_{r,3(k)} = \frac{1}{Z_r}(V_{o,0(k)} - V_{g,0(k)} + (V_{g,0(k)} - V_{o,0(k)} - V_{Cr,0(k)}) \cdot cos(\omega_{rs}\beta_k) \\ - I_{r,0(k)} Z_r \cdot sin(\omega_{rs}\beta_k) + V_{o,0(k)}) \cdot sin(\omega_{rs}\alpha_k) \end{aligned} \tag{C.14}$$

$$\begin{aligned} I_{r,3(k)} = & - sin(\omega_{rs}\beta_k) \cdot sin(\omega_{rs}\alpha_k) \cdot I_{r,0(k)} \\ & - \frac{1}{Z_r} cos(\omega_{rs}\beta_k) \cdot sin(\omega_{rs}\alpha_k) \cdot V_{Cr,0(k)} \\ & + \left(\frac{2}{Z_r} sin(\omega_{rs}\alpha_k) - \frac{1}{Z_r} cos(\omega_{rs}\beta_k) \cdot sin(\omega_{rs}\alpha_k) \right) \cdot V_{o,0(k)} \\ & + \left(-\frac{1}{Z_r} sin(\omega_{rs}\alpha_k) + \frac{1}{Z_r} cos(\omega_{rs}\beta_k) \cdot sin(\omega_{rs}\alpha_k) \right) \cdot V_{g,0(k)} \end{aligned} \tag{C.15}$$

$$\begin{aligned} V_{Cr,3(k)} = & Z_r \cdot sin(\omega_{rs}\beta_k) \cdot cos(\omega_{rs}\alpha) \cdot I_{r,0(k)} \\ & + cos(\omega_{rs}\beta_k) \cdot cos(\omega_{rs}\alpha) \cdot V_{Cr,0(k)} \\ & + (-2 \cdot cos(\omega_{rs}\alpha) + cos(\omega_{rs}\beta_k) \cdot cos(\omega_{rs}\alpha) + 1) \cdot V_{o,0(k)} \\ & + (cos(\omega_{rs}\alpha) - cos(\omega_{rs}\beta_k) \cdot cos(\omega_{rs}\alpha)) \cdot V_{g,0(k)} \end{aligned} \tag{C.16}$$

The output current is found assuming that it is equal to its mean value during each event k or k+1. Therefore:

$$\begin{aligned} i_o = \frac{1}{t_{3(k)} - t_{0(k)}} \Bigg[& \int_{t_{0(k)}}^{t_{1(k)}} \left(\frac{1}{Z_r}(V_{g,0(k)} - V_{o,0(k)} - V_{Cr,0(k)}) \cdot sin(\omega_r t) + I_{r,0(k)} \cdot cos(\omega_r t) \right) dt \\ & + \int_{t_{2(k)}}^{t_{3(k)}} -\frac{1}{Z_r}(V_{Cr,2} - V_{o,0(k)}) \cdot sin[\omega_r (t - t_{2(k)})] dt \Bigg] \end{aligned} \tag{C.17}$$

if $\theta_s = \omega_s t, \quad \gamma_k = \pi$

$$\begin{aligned} i_o = \frac{1}{\gamma_k \cdot Z_r} \Bigg[& \int_0^{\beta_k} \left((V_{g,0(k)} - V_{o,0(k)} - V_{Cr,0(k)}) \cdot sin(\omega_{rs}\theta_s) + I_{r,0(k)} \cdot cos(\omega_{rs}\theta_s) \right) d\theta_s \\ & - \int_{\frac{\pi}{\omega_{rs}}}^{\pi} (V_{Cr,1} - V_{o,0(k)}) \cdot sin[\omega_{rs}(\theta_s - \beta_k)] d\theta_s \Bigg] \end{aligned} \tag{C.18}$$

$$
\begin{aligned}
i_o = \frac{1}{\gamma_k \cdot \omega_{rs} \cdot Z_r} \Big\{ & Z_r \left[sin(\omega_{rs}\beta_k) + sin(\omega_{rs}\beta_k)(1 - cos(\omega_{rs}\alpha_k)) \right] \cdot I_{r,0(k)} \\
& + \left[cos(\omega_{rs}\beta_k) \cdot (1 - cos(\omega_{rs}\alpha_k)) - (1 - cos(\omega_{rs}\beta_k)) \right] \cdot V_{Cr,0(k)} \\
& + \left[(cos(\omega_{rs}\beta_k) - 2) \cdot (1 - cos(\omega_{rs}\alpha_k)) - (1 - cos(\omega_{rs}\beta_k)) \right] \cdot V_{o,0(k)} \\
& + \left[(1 - cos(\omega_{rs}\beta_k)) \cdot (1 - cos(\omega_{rs}\alpha_k)) + (1 - cos(\omega_{rs}\beta_k)) \right] \cdot V_{g,0(k)} \Big\}
\end{aligned}
\tag{C.19}
$$

The following event $(k+1)$ is described by the same equations, but with reverse polarities, so the following choice of state variables of the state space model is valid:

$$x_{1(k)} = I_{r,0(k)}; \qquad x_{2(k)} = V_{Cr,0(k)} \tag{C.20}$$

$$x_{1(k+1)} = -I_{r,2(k)}; \qquad x_{2(k+1)} = -V_{Cr,2(k)} \tag{C.21}$$

In order to develop a continuous time model for the state variables, the time derivatives of the state variables are set equal to the incremental ratio of the discrete state variables during each event:

$$\dot{x}_i(k) = \frac{x_{i(k+1)} - x_{i(k)}}{t_{0(k+1)} - t_{0(k)}} = \frac{2}{T_s} \cdot (x_{i(k+1)} - x_{i(k)}) \tag{C.22}$$

Where T_s is the switching period.
By considering the voltage across the tank capacitor and resonant current as continuous:

$$I_{r,0(k+1)} = I_{r,3(k)}; \qquad V_{Cr,0(k+1)} = V_{Cr,3(k)} \tag{C.23}$$

Substituting definitions C.20-C.21 into the expressions C.15-C.16, and by using Equation C.22, the continuous state space model of equations C.24-C.30 is obtained. Removing the subscripts, the output equation C.32 is obtained directly by Equation C.19.

$$\begin{aligned}\dot{x}_1 =& \frac{2}{T_s} \cdot \Big\{ [sin(\omega_{rs}\beta) \cdot sin(\omega_{rs}\alpha) - 1] \cdot x_1 \\ &+ \frac{1}{Z_r} cos(\omega_{rs}\beta) \cdot sin(\omega_{rs}\alpha) \cdot x_2 \\ &- \left[\frac{2}{Z_r} sin(\omega_{rs}\alpha) - \frac{1}{Z_r} cos(\omega_{rs}\beta) \cdot sin(\omega_{rs}\alpha) \right] \cdot V_o \\ &+ \left[\frac{1}{Z_r} sin(\omega_{rs}\alpha) - \frac{1}{Z_r} cos(\omega_{rs}\beta) \cdot sin(\omega_{rs}\alpha) \right] \cdot V_g \Big\} \\ &= f_1(x_1, x_2, V_g, V_o, f_s)\end{aligned} \tag{C.24}$$

$$\begin{aligned}\dot{x}_2 =& \frac{2}{T_s} \cdot \Big\{ -Z_r \cdot sin(\omega_{rs}\beta) \cdot cos(\omega_{rs}\alpha) \cdot x_1 \\ &- [cos(\omega_{rs}\beta) \cdot cos(\omega_{rs}\alpha) + 1] \cdot x_2 \\ &+ [2cos(\omega_{rs}\alpha) - cos(\omega_{rs}\beta) cos(\omega_{rs}\alpha) - 1] \cdot V_o \\ &+ [-cos(\omega_{rs}\alpha) + cos(\omega_{rs}\beta) \cdot cos(\omega_{rs}\alpha)] \cdot V_g \Big\} \\ &= f_2(x_1, x_2, V_g, V_o, f_s)\end{aligned} \tag{C.25}$$

where:

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{C.26}$$

$$\omega_r = \frac{1}{\sqrt{L_r C_r}} \tag{C.27}$$

$$\omega_{rs} = \frac{\omega_r}{\omega_s} = \frac{f_r}{f_s} \tag{C.28}$$

$$tan(\omega_{rs}\beta) = -\frac{Z_r x_1}{V_g - V_o - x_2} \tag{C.29}$$

$$\alpha = \pi - \frac{\pi}{\omega_{rs}} \tag{C.30}$$

Particular attention is needed for Equation C.29, defining the conduction angle of the IGBTs T_1 and T_4 during event k. This value should be always in the range:

$$0 \leq \beta \leq \frac{\pi}{\omega_{rs}} \tag{C.31}$$

For the output current equation, the following result is obtained considering the output current constant and equal to its mean value during each event:

$$\begin{aligned} i_o = \frac{1}{\pi \cdot \omega_{rs} \cdot Zr} \{ & [sin(\omega_{rs}\beta) \cdot (2 - cos(\omega_{rs}\alpha))] \cdot Z_r \cdot x_1 \\ & + [-1 + 2cos(\omega_{rs}\beta) - cos(\omega_{rs}\beta) \cdot cos(\omega_{rs}\alpha))] \cdot x_2 \\ & + [-3 + 2 \cdot cos(\omega_{rs}\beta) + 2 \cdot cos(\omega_{rs}\alpha) - cos(\omega_{rs}\beta) \cdot cos(\omega_{rs}\alpha)] \cdot V_o \\ & + [2 \cdot (1 - cos(\omega_{rs}\beta)) - cos(\omega_{rs}\alpha) + cos(\omega_{rs}\beta) \cdot cos(\omega_{rs}\alpha)] \cdot V_g \} \\ & = f_o(x_1, x_2, V_g, V_o, f_s) \end{aligned} \tag{C.32}$$

Equations from C.24 to C.30 represent the state space model of SRC#. Approximations leading to this model are here recollected:

- Effect of magnetizing inductance of the transformer is neglected;
- Small ripple approximation: voltages applied on the turbine side and on the grid side are considered as constant during each event as well as the current delivered in the grid side is considered equal to its mean value during each event;

C.2 State plane analysis

The model developed in the previous Appendix C, and described by state-space Equation C.24 and Equation C.30 together with Equation C.32, is heavily nonlinear. The state plane analysis of the converter can be performed to obtain the operating points, reducing steady state relations between state and input variables to simple geometry.

The converter has only two state variables, the voltage across the resonant capacitor (v_{Cr}) and the tank current flowing through the inductor (i_r). A state plane using v_{Cr} and $Z_r \cdot i_r$ as orthogonal axis can be set, where Z_r is defined in Equation C.26.

Consider first the sub-interval (T_1, T_4) ON, during the event k. By the solution of equations of resonant capacitor voltage and inductor current, it results that the system evolution outlines a circular trajectory in the defined state plane, centered in $C_{0(k)}$ and of radius $R_{0(k)}$:

$$C_{0(k)} = (V_{g,0(k)} - V_{o,0(k)}, 0) \tag{C.33}$$

$$R_{0(k)} = \sqrt{\left(V_{g,0(k)} - V_{o,0(k)} - V_{Cr,0(k)}\right)^2 + \left(Z_r \cdot I_{r,0(k)}\right)^2} \tag{C.34}$$

The trajectory is the circumference sector, starting from $(V_{Cr,0(k)}, I_{r,0(k)})$ and crossing the capacitor voltage axis ($i_r = 0$). The angle spanned by this trajectory, seen from the center $C_{0(k)}$ is:

$$\omega_r \cdot (t_{1(k)} - t_{0(k)}) = \omega_{rs} \cdot \beta_k \tag{C.35}$$

An example for the developed study case and steady state conditions is portrayed in Figure C.4. Here a high voltage difference between the voltages on the two sides of the transformer of the converter is used in order to highlight the trajectory shape.

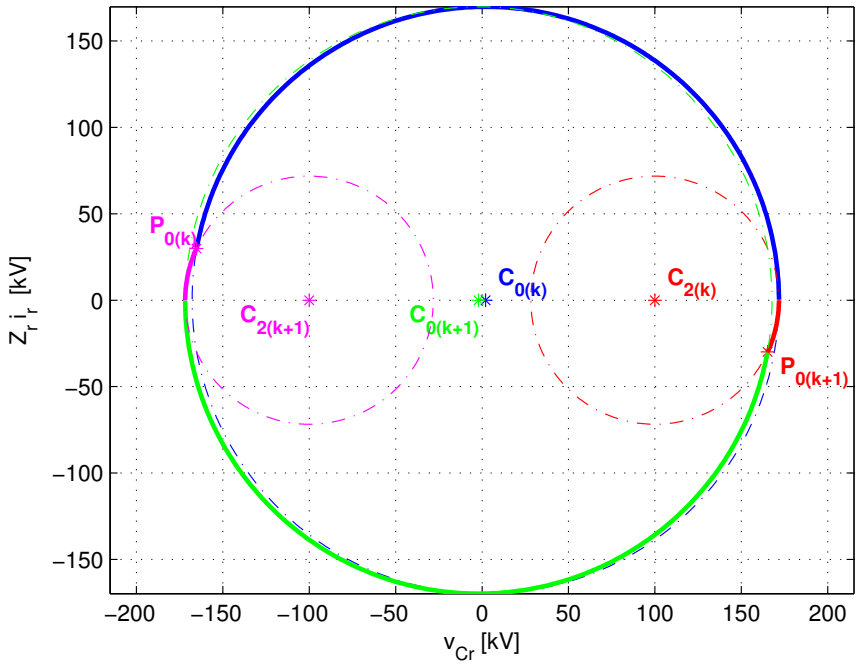


Figure C.4: Trajectory in the State Space of study case SRC# in Steady State Operation. - $V_g = 4000V$; $V_o = 99kV$; $f_s = 1000Hz$

When the current becomes zero, there is a sub-interval of non-conduction due to the reverse biasing of the diode bridge. During this sub-interval the current keeps being zero, and the resonant capacitor is not being charged or discharged, thus it keeps its voltage value. A new change in state variables occurs in the next sub-interval (D_1, T_3) ON. Solving the equations from it, the outlined trajectory in the state plane ends up being again a circumference sector, centered in $C_{2(k)}$ and of radius $R_{2(k)}$:

$$C_{2(k)} = (V_{o,2(k)}, 0) \tag{C.36}$$

$$R_{2(k)} = |V_{o,2(k)} + V_{Cr,2(k)}| \tag{C.37}$$

This circumference sector lasts from the point $(V_{Cr,1(k)}, 0)$ until the point $P_{0(k+1)}$, representing the starting point for the representation of the following $k+1$ event. Spanned angle, respect to the center $C_{2(k)}$ is:

$$\omega_r \cdot (t_{3(k)} - t_{2(k)}) = \omega_{rs} \cdot \alpha_k \tag{C.38}$$

The trajectory in the state plane has to be a closed curve in steady state conditions, as shown in Figure C.4. The closed shape of the trajectory fix the value of the voltage across the capacitor when the current makes a zero crossing. Consider the triangle ABC, shown in the following Figure C.5.

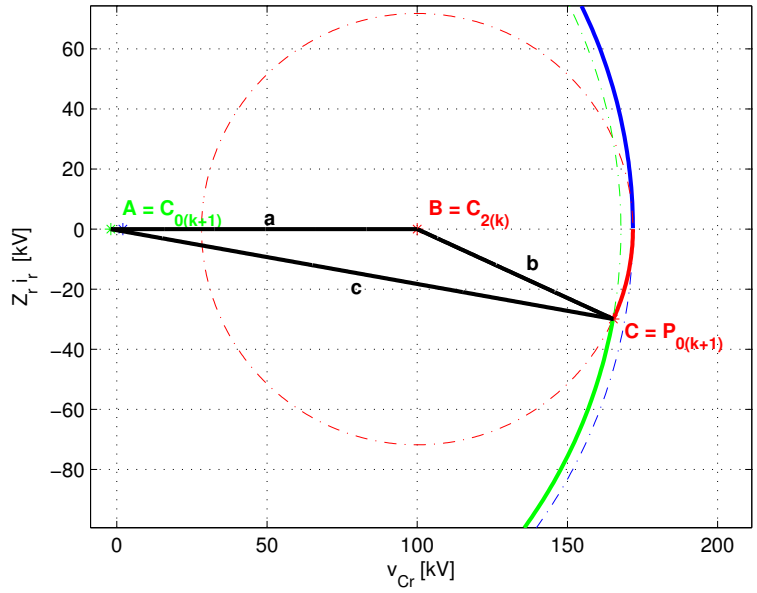


Figure C.5: Particular of the state space trajectory of SRC#, operating in steady state: $V_g = 4000V$; $V_o = 100kV$; $f_s = 1000Hz$

The vertices are defined as follows:

$$A = C_{0(k+1)}; \qquad B = C_{2(k)}; \qquad C = P_{0(k+1)} \tag{C.39}$$

The dimensions of the three sides of the highlighted triangle are defined as:

$$a = |\overline{AB}| = V_g \tag{C.40}$$

$$b = |\overline{BC}| = V_{Cr,1(k)} - V_o \tag{C.41}$$

$$c = |\overline{AC}| = V_{Cr,1(k)} - V_g + V_o \tag{C.42}$$

Moreover, by inspection of the same Figure C.5:

$$\widehat{CAB} = \pi - \omega_{rs} \cdot \beta \tag{C.43}$$

$$\widehat{ABC} = \pi - \omega_{rs} \cdot \alpha = \pi \cdot (2 - \omega_{rs}) \tag{C.44}$$

$$\widehat{ACB} = \pi - \widehat{CAB} - \widehat{ABC} \tag{C.45}$$

By Carnot's theorem the voltage across the capacitor when the current approaches zero is a well-known function of the constant input variables:

$$V_{Cr,1(k)} = \frac{V_g \cdot V_o \cdot [1 + cos(2 - \omega_{rs})\pi)]}{2V_o - V_g \cdot [1 - cos((2 - \omega_{rs})\pi)]} \tag{C.46}$$

The output current, due to the effect of the filter that will be present on the grid side, can be approximated by its mean value in each event. The stored charge in the capacitor in each event is linked to the peak value of the capacitor voltage itself by Equation 2.2. Thus following result is valid:

$$Io = 4C_r V_{Cr,1(k)} f_s \tag{C.47}$$

Trigonometric considerations lead also to the knowledge of $V_{Cr,0(k)}$ and $I_{r,0(k)}$ for fixed input variables:

$$V_{Cr,0(k)} = -(V_o + (V_{Cr,1(k)} - V_o)) \cdot cos(\omega_{rs}\alpha) \tag{C.48}$$

$$I_{r,0(k)} = \frac{(V_{Cr,1(k)} - V_o) sin(\omega_{rs}\alpha)}{Z_r} \tag{C.49}$$