2-Dimensional Control of VSC-HVDC

Master Thesis

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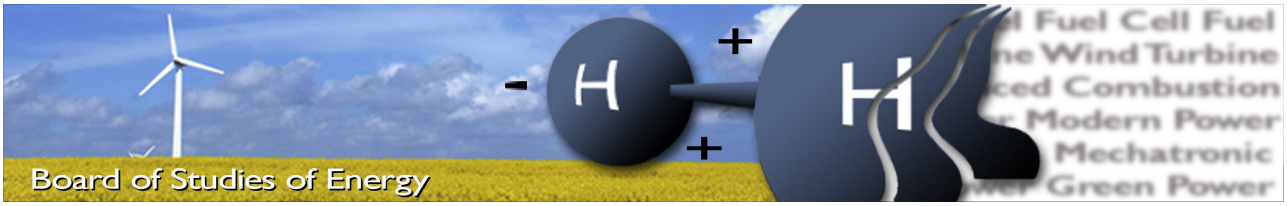

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In a conventional VSC-HVDC control structure is was observed that when performing an uncontrolled switching between control modes in the 1-D control structure, transients would be present. This thesis had the objective of developing a 2-D upper level control structure without a switch between the control modes to achieve a seamless switching. To evaluate the performance, the 2-D controller were compared with the 1-D controllers response as a reference. Tests showed that for PtP-HVDC and 3-terminal HVDC, the 2-D controller were able to achieve a seamless switching for all cases with negligible oscillation. Other factors observed was that 2-D in some cases had a slower response, but at the same time containing less transients in its response.

Pages, total including appendix:	119
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Preface

The Master Thesis concludes the 4th semester of the M.Sc. in Electrical Power Systems and High Voltage Engineering at the Department of Energy Technology at Aalborg University. The Thesis was conducted in the period from February 2nd to June 1st 2018. The project concerns Testing and design of a new upper level control structure for the voltage source converter for a Point-to-Pint and a 3-treminal multi terminal HVDC system

Acknowledgement

We would like to give credit to several people who were involved during the MSc thesis which were providing feedback in the form of supervisor meetings, helping and leading us in the right direction towards completion of the thesis. We would like to acknowledge Aalborg University and the Energy Department. We would like to express our gratitude to our supervisors Fillipe f. da silva and Roni Irnawan For giving us the opportunity to explore the field within HVDC technologies and power systems We would like to thank them for their advice and guidance despite their often tight time schedule and we appreciate the regular follow up during throughout the thesis.

Abbrevation

Index	Description
1-D Control	1-dimensional upper level control scheme
2-D Control	Two-dimensional upper level control scheme
Bm	Bus-bar
Cm-A1	Converter station
Cm-C1	Converter station
Cm-B2	Converter station
Cm-B3	Converter station
Cm-F1	Converter station
DCS1	Test system developed by Cigre
DCS2	Test system developed by Cigre
HVAC	High voltage alternating current
HVDC	High voltage direct current
IGBT	Insulated Gate Bipolar Transistor
LCC	Line commutated converter
MTDC	Multi-terminal HVDC
MMC	Multi-Level Modular Converter
NLC	Nearest level control
OWF	Offshore wind farm
PCC	Point of Common Coupling
PLL	Phase lock loop
PtP	Point-to-Point
PWM	Pulse Width Modulation
RES	Renewable Energy Sources
SPWM	Sinusoidal PWM
SM	Sub-Module
VSC	Voltage Source Converter

Symbol	Description	Notation
α	alpha	-
β	beta	-
$1/k_v$	Droop slope	$\frac{\Delta P}{\Delta V}$
C_{cell}	Cell capacitance	F
d	delta	-
e_t	Error in a function of time	-
$\overline{f}$	Space vector	-
f	frequency	Hz
f_s	switching frequency	Hz
K_v	Droop constant	$\frac{kV}{MW}$
K_i	Integral gain	-
K_p	Proportional gain	-
T_i	Reset time	
L_{arm}	Arm inductance	H
I, i	Current	A
m_a	Amplitude modulation	-
N_{SM}	Number of sub modules in a converter	-
P_{ac}	Active power	W
P^*	Power reference	MW
Q_{ac}	Reactive power	VAr
R	Resistance	Ω
S_{MMC}	Apparent power of the converter	-
t	Time	s
V_{dc}	DC Voltage	V
V_{ac}	AC Voltage	V
V^*	Reference voltage	V
V_s	Voltage potential AC terminal	-
V_d	DC leg voltage	-
V_{cell}	Cell voltage signal	-
v_{tri}	Triangular voltage signal	-
$v_{control}$	sinusoidal signal	-
V_c	Capacitor voltage	-
V_{SM}	Sub module voltage	-

Summary

The increased focus on limiting global warming and wish to reduce greenhouse gas emissions have led to an increased focus on renewable energy sources (RES)[1]. Offshore wind farms are one of these RES. Offshore wind power implies long distance transmission of power, where HVDC has been proven to be the most beneficial technology [2, 3]. The voltage source converter technology (VSC) is the best option when wanting to transmit power from an OWF over a long distance [4, 4, 5]. VSC-based HVDC implies the use of a modular-multilevel converter (MMC) technology. The upper level control structure which is most often used in VSC-HVDC transmission is the current vector control. The current vector control strategy use reference frame transformation to change three phase AC systems into two constant DC signals.

The control structure of the conventional upper level control [6] consists of four loops divided into the d-axis (V_{dc}, P_{ac} loops), and q-axis loop (V_{ac} and Q_{ac} loops) control. In some situations it could be necessary for the system operator to switch the control mode from for example V_{dc} to P_{ac} control. An uncontrolled switching between these control loops cause transients in the system. The main goal for this thesis is therefore to propose a new upper level control scheme based on a 2-dimensional structure, (referred to as the 2-D controller). The 2-D upper level control strategy is based on making V_{dc} and P_{ac} in the d-axis and V_{ac} and Q_{ac} in the q-axis dependent on each other. The four loops in the conventional upper level control scheme (from now referred to as the 1-D control scheme) is therefore reduced from four to two loops. Each loop will consist of only one PI controller, hence tuning will be needed to find proposed gains. The operation of the 2-D controller will be compared to the 1-D controller to validate its performance.

The d-axis and q-axis control loops in the 1-D and 2-D controller were evaluated for different test cases when only one converter was connected to an ideal voltage source or open terminals. The test cases investigated the response of the 2-D controller when applying a step, droop control and how the controller worked to keep the limits set in the controller. The results from the test cases validated that the 2-D controller upper level scheme worked correctly, while at the same time finding advantages and drawbacks of the two control strategies.

To validate that the 2-D controller could operate in a more realistic scenario, it was tested in a PtP HVDC link and in a 3-terminal MTDC system. Some of the different test cases were seamless switching and fault analysis. The results showed that the 2-D controller will be able to perform seamless switching both in a PtP-HVDC link and a 3-terminal MTDC system. Other factors observed was that the 2-D controller in some cases had a slower response than the 1-D, but at the same time the 2-D controller has less transients in the response. The 2-D

controller with the proposed tuning gains showed a good performance of keeping the limits set in the controller during a fault.

Contents

Chapter 1

Introduction

Due to the worlds increased focus on limiting global warming and wanting to reduce the amount of green house gas (GHG) emissions, more attention has been drawn to the development and use of renewable energy sources (RES) [1]. Wind energy technology is currently one of the leading RES technologies due to its mature technology and large scale of wind resources. According to [7] the wind power penetration level is only expected to increase in the future making it an important renewable energy resource for the world. Most of the wind farms existing today are placed onshore, but due to good wind conditions, small impacts on the environment and a reduction of construction costs at offshore locations, it is wanted to increase the amount of offshore wind farms (OWFs) in the future [7]. Both the size of the wind farms and the distance to the shore is expected to increase. This implies the importance of investigating in technology for transmission and control of bulk power transmitted over longer distances from large OWFs.

The two alternatives for transmission of power are HVAC and HVDC technology. A comparison between these technologies are depicted in Figure 1.1.

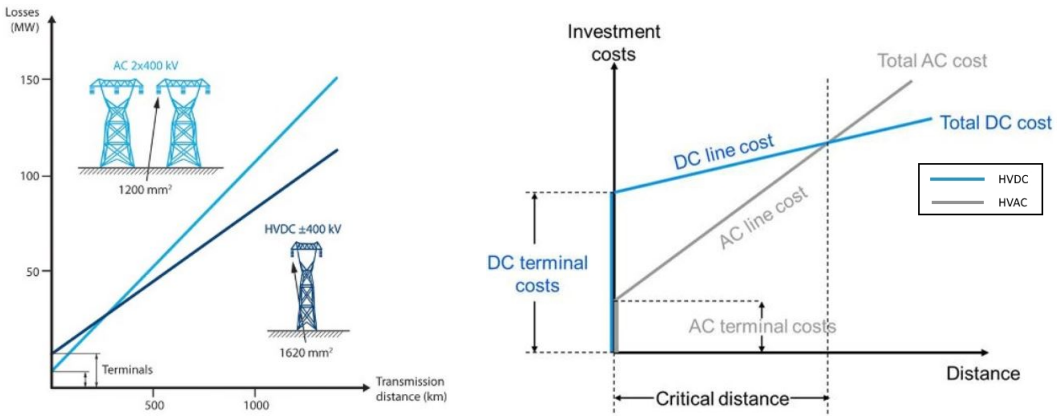

Figure 1.1: The figure to the left shows a comparison of the losses between HVAC and HVDC. The figure to the right depicts the cost comparison between HVDC and HVAC [8]

The figure to the left shows losses plotted against transmission distance. It can be observed that for longer distances after a certain break-even distance, HVDC will have lower power losses than HVAC. This implement that HVDC is the most cost efficient solution for transferring power over distance that is greater than the break-even distance[2]. The figure to the right shows that HVDC has higher converter station investment costs than HVAC. [3] states that the onshore converter station costs for a 1000 MW VSC-HVDC system is 110 M€. As a comparison the HVAC onshore converter station with the same power rating costs 28 M€. Despite the higher investment costs for HVDC it can be seen that above a certain distance, "break-even distance", HVDC will have lower losses and total costs, hence giving it being the most feasible economical option for a long distance high voltage transmission [2].

Other advantages are that HVDC does not have problems with reactive power compensation. In HVAC cables the reactive power needs to be compensated due to the high capacitance in the cables. The need for reactive power compensation limits the maximum length of the power cable, hence the transmission distance. HVDC inherit the possibility for asynchronous connection of AC grids with different magnitude and/or frequency, as-well as an easier control of active power in the system [2]. As a small conclusion, the most efficient and economical way of transmitting large amount of energy over long distances is by using HVDC technology.

1.1 VSC-HVDC Technology

Nowadays HVDC links can be implemented as either VSC-HVDC or LCC-HVDC also known as HVDC-classic. The HVDC-classic is based on thyristor technology and is widely used across the world for distributing bulk of power. The LCC-HVDC technology has some drawbacks regarding that black-start capability and connection to weak offshore grids becomes difficult. The LCC technology needs to be connected to a strong AC grid since converters require a stable commutation voltage across its thyristors which limits HVDC-classic to onshore power-transmission. The limitations of HVDC-classic makes placement of offshore converters impossible. Another factor is that the size of the offshore converter station is large and it weighs a lot which is not good in cooperation with offshore placement, hence leading to a high economical expense[4, 4, 5].

Regarding VSC-HVDC, the first commercial VSC-HVDC project was commissioned in Gotland, Sweden in the year of 1999[9]. Since then, there have been a big development in projects including the VSC strategy. VSC-HVDC is based on the use of self-commutating switches (often IGBT technology). In a VSC, the DC voltage polarity is kept constant and it is the polarity of the DC current that changes the direction of the power flow. It uses pulse width modulation (PWM) techniques in order to control the gate switching frequency of the IGBT [10]. VSC-HVDC also allows for independent control of reactive and active power.

Until recently, the 2-level converter was most commonly used for VSC-HVDC, but with advances in power electronics technology the modular multilevel converter (MMC) structure has gained more and more attention. These two converter types will be explained more in detail in chapter 2.

The main advantages of using VSC-HVDC compared to the classic-HVDC technology are according to [11, 12] :

- The possibility to have independent control of active (P_{ac}) and reactive power (Q_{ac})

- Control of the voltage in the AC voltage while the transmitted active power is kept constant, improves power quality
- The instant reversal of power flow happens because of a reversal in DC current direction and not the DC voltage polarity. This allows for using XLPE cables.
- Black-start capability, VSC-HVDC has the ability of operating a no-load condition (i.e no current is flowing) to restore power to a AC network.
- Better suited for multi-terminal connection
- Smaller footprint of converter stations (better suited for offshore wind-farms) i.e less harmonic content in the AC waveform leading to less filtering to obtain a close to sinusoidal AC waveform.

Figure 1.2 depicts a generic point-to-point (PtP) configuration of a VSC-HVDC link. As it can be seen the VSC-HVDC consists of two VSC stations and a DC cable connection consisting of 1 or more lines for power transmission. Both converters are connected to equivalent AC grids. The DC side of the converter has a capacitor which stabilizes the DC voltage. The size of the capacitor is reduced when a higher switching frequency is applied. The phase reactor stabilizes the AC current and also reduces the harmonic components in the current, which occurs because of the converter switching. The configuration of the HVDC link is a symmetric monopole. In a symmetric monopole configuration the grounding is placed in between the two lines of transmission so that no DC current flows trough ground.

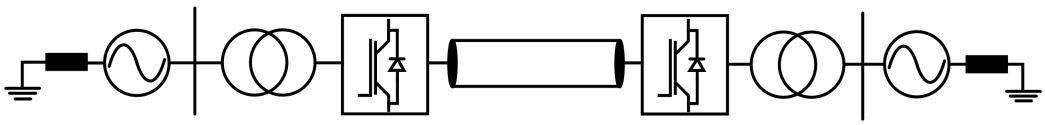

Figure 1.2: PtP-Configuration of two eqvivalent grids trough a VSC-HVDC transmission system [1]

In order to have a functioning HVDC system one converter has to operate in rectifier-mode and one in inverter-mode. During normal conditions both converter stations control active and reactive power independent of the other converter station. But still the active power in the DC cables has to be balanced, hence the active power entering the HVDC link has to be the same as the output power (neglecting power losses). To have this power balance one of the stations have to control the DC voltage V_{dc}, while the other one controls the active power P_{ac} [13]. To maintain the voltage amplitude in the adjacent grid, reactive power (Q_{ac})- and AC voltage (V_{ac}) control is used to support the grid.

The performance of the VSC-HVDC system does not only rely on the efficiency of the converters but also on how the system is controlled. The control mode used for VSC-HVDC is often the current vector control. The current vector control strategy uses reference frame transformation to change three phase AC systems into constant two phase DC signals. It has two control loops upper level control loop, and the lower level control loop. The upper level control loop consists of four control loops controlling active power, DC voltage, AC voltage and reactive power. The upper level control is responsible for sending a current reference to the lower level control loop. The lower level control, manages the switching states of the converters and monitors the voltage reference of the grid[14].

As stated in [6] the upper level control can either be connected to an AC system with active synchronous generation known as a non-islanded system, or it can be connected to an isolated or weak AC system known as an islanded system. This thesis will consider a non-islanded connection of the upper level control. The main objective will be to optimize the upper level controls for the control scheme of the VSC-HVDC system.

When VSC-HVDC is used to distribute power to other converters present in the DC grid, a control which can control a constant voltage-, constant power or a droop control can be enforced to the onshore converters to provide the necessary amount of power to ensure a stable voltage at the DC side and at the same time ensuring a stable voltage and power-factor(PF) at the AC side where the HVDC link is connected. Converter stations which has this type of controls are usually onshore converters (i.e converters that are connected a larger area). For offshore converter stations used to connect OWFs to the HVDC grid, control-schemes are not used due to that it is wanted to transmit all of its power production to the grid.

Nowadays, an increasing number of VSC-HVDC links are planned or already in operation. The feasibility of connecting planned HVDC links to existing HVDC links, which naturally is transformed to a multi-terminal HVDC grid (MTDC). The objective the MTDC network is to create secure an efficient interconnection of several HVDC links in the near future, participating in a gradual DC grid development. A MTDC system consists of either three or more terminals. Figure 1.3 shows the configuration of a 3-terminal symmetric monopole MTDC system.

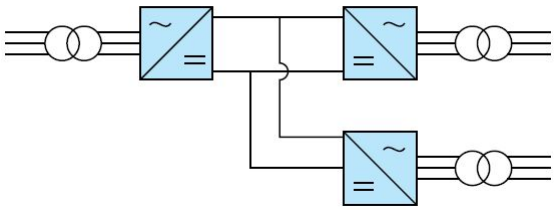

Figure 1.3: 3-terminal MTDC system based on symmetric monopole configuration [15]

The control of the MTDC grid should ensure that the DC grid is strong and reliable and also that it can support its connected AC grids properly. If a fault occurs in a MTDC grid, the part where the fault happens will be isolated and the power flow will instead be directed through the healthy DC grid [16].

Examples of MTDC systems that have been proven feasible are the 3-terminal system between Corsica (France) and Sardinia (Italy), and the Quebec - New England 3-terminal system which is located onshore between Canada and USA [10].

1.2 Scope of Work

The scope of this thesis is to design a 2-dimensional (2-D) controller for use in VSC-HVDC networks. The study in this thesis will use a power system software named PSCAD/EMTDC. The CIGRE B4 test group have designed a PtP HVDC link model (DCS1) and a 4-terminal MTDC system (DCS2). The configuration of the upper level control scheme used in the

mentioned test systems developed by CIGRE can be found in [6]. The upper level control scheme will be used as a reference for simulations this thesis. For convenience it will be referred to as the 1-D controller due to its 1-dimensional configuration.

The upper level control of the DCS1 and DCS2 test systems are based on a current vector control scheme. In the upper level control configuration of that a switch is needed to change the control state between P_{ac} control and V_{dc} control, as well as between Q_{ac} control and V_{ac} control. The problem with conducting an uncontrolled switching between the control loops is that it cause transients in the system. A simulation showing the transients during an uncontrolled switching can be seen in Figure 1.4. The simulation was performed by switching converter Cm-A1 from P_{ac} to V_{dc} control, and the converter Cm-C1 from V_{dc} to P_{ac} control in an HVDC link. The switching was performed at the same time for both control loops.

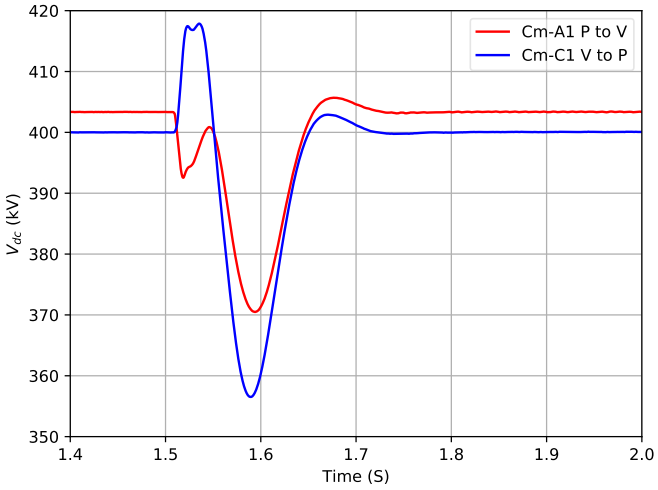

Figure 1.4: Voltage transient during switching of control loops

The figure shows that an uncontrolled switching between the control loops can cause transients in the system that in this case lasts for around 0.2 seconds. To avoid this situation, the dispatch control operator has to manually operate a switch between the two control loops (i.e. P_{ac} and V_{dc} / Q_{ac} and V_{ac}). Switching between the control loops can only be conducted when the currents in the two loops are approximately at the same value. This is important in order to avoid over-current and over-voltage situations[17].

This thesis proposes a new upper level control scheme that can replace the 1-D control scheme developed by CIGRE in the [6]. The goal for the new controller will be to have a seamless switching between the control loops. In the proposed control scheme a droop control will be implemented to control the four controllers. This means that the control loops P_{ac} and V_{dc} will be dependent on each-other, and the Q_{ac} and V_{ac} loops will be dependent on each other in a 2-dimensional plane. The conventional CIGRE system contains four, 1-dimensional (1-D) control loops. By making the control loops dependent on each other the four 1-D control loops will be reduced to two 2-D control loops. Figure 1.5 and Figure 1.6 depicts how the number of control loops are reduced.

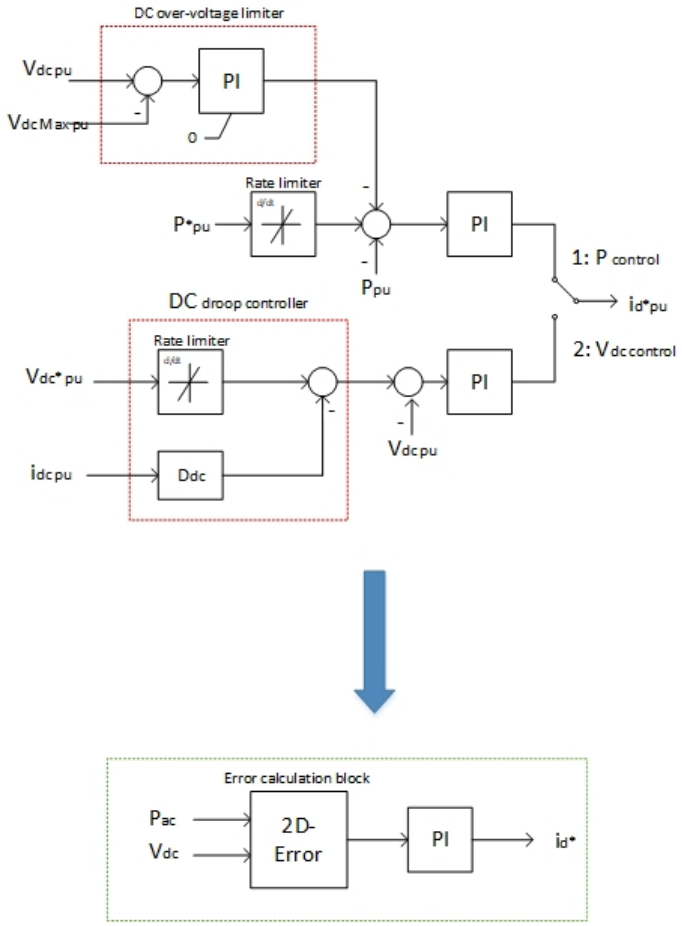

Figure 1.5: Conventional and the proposed 2D-controller for P and V_{dc} control

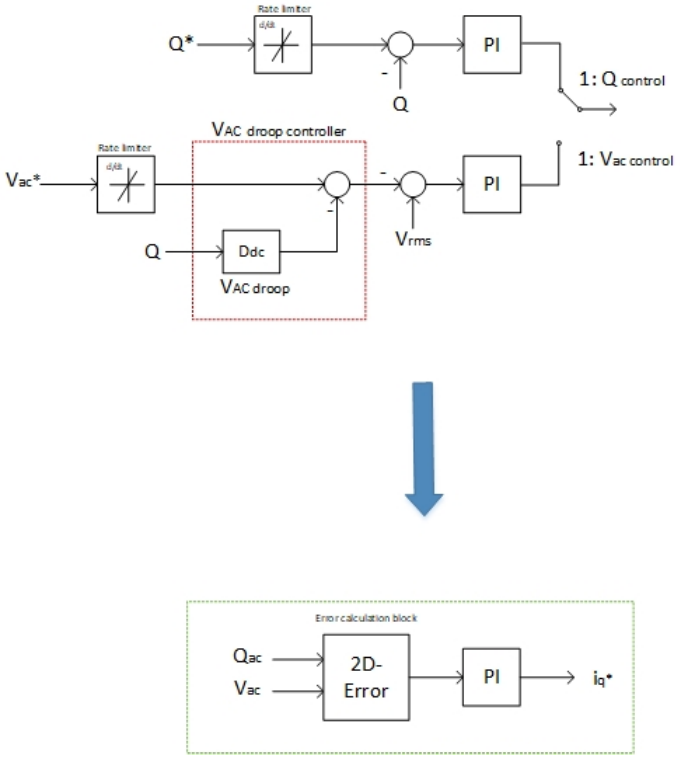

Figure 1.6: Reduction of the reactive power and V_{ac} loop

As illustrated, a simplification of the 1-D system into the 2-D control system proposed in the green square. It can be seen that the switch between the V_{dc} and P_{ac} lops and the Q_{ac} and V_{ac} is eliminated, hopefully creating a seamless switching between the control loops. Another factor is that the 2-D controller will reduce the number of PI controllers in the upper level control structure. It is wanted to have one PI controller in the d-axis control loop, and one in the q-axis loop. This implies that the DC over voltage limiter loop which contains one PI controller will be eliminated. The goal is to instead create a new 2-D error calculation block as seen on Figure 1.5 and Figure 1.6, which contains an algorithm that will calculate the error between in the system. The error block should also contain limits for DC voltage, active power, reactive power and AC voltage. Reducing to only one PI controller for each control loop should lead to a shorter processing time, and a faster response if PI controllers placed in cascade are eliminated. A reduction in the number of PI controllers will also lead to less controllers that need to be tuned which means that the control will be easier to implement. The system will also have a higher reliability since there will be less components in the system.

The performance of the d- and q-axis loop in the 2-D controller has to be compared and verified with the performance of the 1-D controller. This will be conducted for ideal conditions. The 2-D controller will also be tested for its performance compared to the 1-D during non-ideal conditions in a PtP- and 3-terminal HVDC system. The goal of the testing in to verify that the 2-D controller can operate according to the 1-D controller. It is also wanted to investigate the advantages and drawbacks with the 2-D controller compared to

the 1-D controller.

1.2.1 Main Objectives

The objectives of the thesis will be conducted in the following steps listed as bullet points:

- Do a literature survey and get a deeper understanding of how the upper level control of VSC and the tuning of PI controllers works.
- **Design a 2-dimensional controller that will achieve seamless switching**
- **Create a new upper level control scheme in PSCAD**
  - Develop a 2-D control loop that will operate to control P_{ac} and V_{dc}
  - Tune the PI controller to obtain tuning parameters working for P_{ac}, V_{dc} and DC voltage droop control
  - Develop a 2-D control loop that will operate to control Q_{ac} and V_{ac}
  - Tune the PI controller obtain tuning parameters working for Q_{ac} and V_{ac},
  - Verify the operation of the d- axis and q-axis control loops by testing them for one converter during ideal conditions
- **Test and performance of the d-axis control loop of the 1-D and 2-D controller in a PtP and 3-terminal HVDC system and compare the performance**
  - Seamless switching
  - 3-phase to ground fault
  - DC voltage droop control
  - Permanent outage of one converter
- Evaluate and discuss the advantages/drawbacks of the 2-D controller compared to the 1-D

1.3 Limitations

- The only tuning parameters evaluated for use in the 1-D controller are the ones obtained from [6].
- The results of the 2-D controller will be evaluated for an equivalent grid.
- The q-axis control loop will not be tested for a PtP HVDC link or a 3-terminal MTDC system.
- The upper level control scheme for the 2-D controller do not contain a method to implement the decoupled current controller
- Gain scheduling will not be implemented for the 2-D controller

Chapter 2

Topology and Operation of the Voltage Source Converter

This chapter presents the basic topology and operation of a voltage source converter (VSC). First, the 2-level converter is presented and the PWM technique is described. Then the topology and operation of the half bridge MMC is explained. In the end the nearest level control (NLC) is presented.

2.1 2-level Converter

The most simple converter topology of a VSC is the 2-level converter. The 2-level converter can be used to explain the basic operation principle of a VSC. Figure 2.1 depicts a 2-level converter with 3 phase legs. A 2-level converter can work either as a rectifier or an inverter, by changing the direction of the current. The capacitor in the converter works as a short term energy storage to keep the DC voltage constant between switching. The inductance connected in series between the midpoints of the phase leg and the the AC terminals ensures to maintain a constant current on the AC side in between phase leg commutations [18].

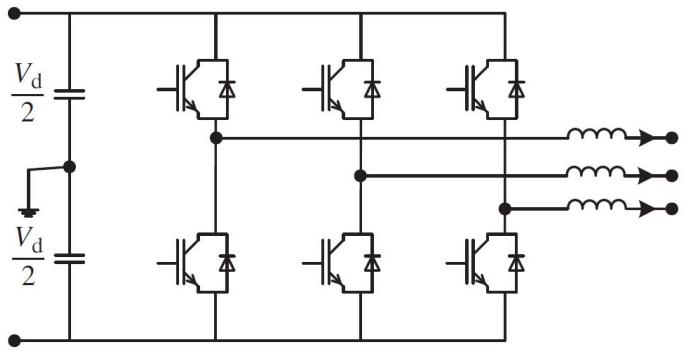

Figure 2.1: Configuration of a 2-level converter with 3-phase legs[18]

The switching sequence of a 2-level converter is shown in Figure 2.2 and can be used to explain the switching sequence of a 2-level converter. In the switching sequence, the AC-current is going in the same direction as indicated by the arrow on the figure. As seen in figure (a) the sequence starts with the upper switch conducting. The potential at the AC terminal, denoted as V_s, is now the same as the positive DC leg $+\frac{V_d}{2}$. Then in (b), the switch is turned off and the current will pass trough the lower diode. When the current is fully commutated to the lower diode as shown in (c), the voltage potential at the AC terminal will be negative $-\frac{V_d}{2}$. To make it possible to change the direction of the phase current, the lower switch is turned on after a delay named "blanking time". The blanking time makes sure that both switches are not in the on state at the same time which could damage the converter. To get a positive DC terminal potential again, the current is commutated from the lower diode to the upper switch as seen in (d). When the lower diode turns off, the DC terminal voltage is the same as in figure (a) and the cycle is repeated [18].

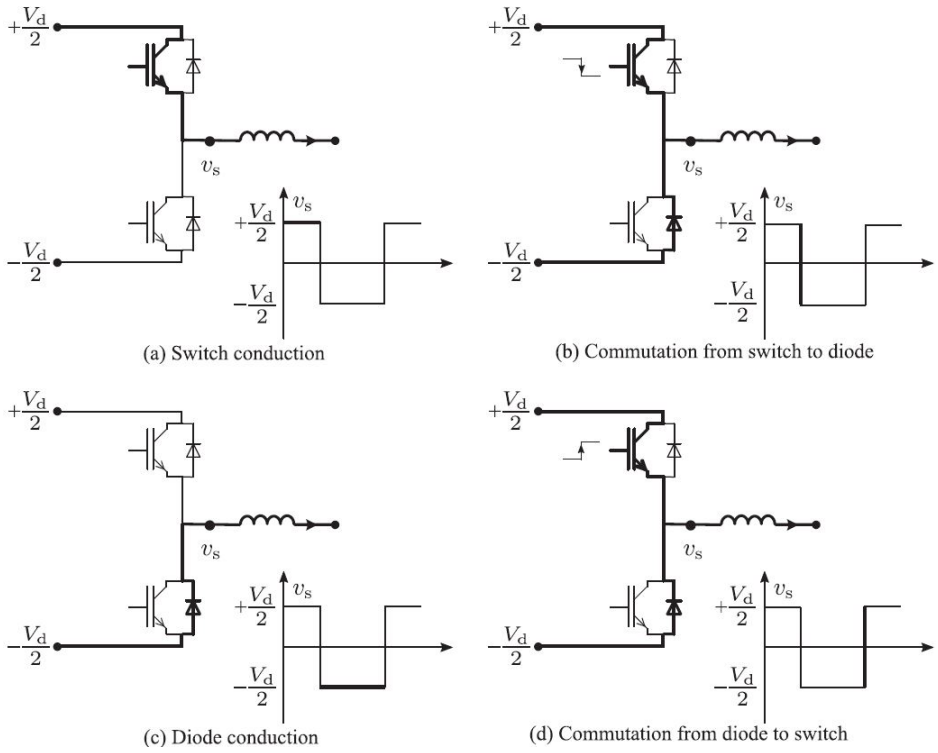

Figure 2.2: Switching sequence of a 2-level converter [18]

If the direction of the current had been in the opposite direction of what is indicated in Figure 2.2, the sequence would be the same except that the current would be commutating between the upper diode and the lower switch in (a). The potential at the AC terminal can be calculated by equation[18]:

$$V_s = s\frac{V_d}{2} \tag{2.1}$$

Here, s is denoted as +1 when the phase leg is connected to the positive DC terminal

and -1 when connected to the negative terminal.

2.1.1 Sinusoidal Pulse Width Modulation

A modulation technique that is used for controlling the output voltage of a power converter is sinusoidal pulse width modulation (SPWM). The goal is to have a sinusoidal output of the converter where it is possible to control the magnitude and frequency. The principle of SPWM is presented in Figure 2.3. The sinusoidal voltage waveform is created by comparing a triangular waveform v_{tri} (often named carrier waveform) with a sinusoidal waveform/control signal (v_{con}) at the wanted frequency.

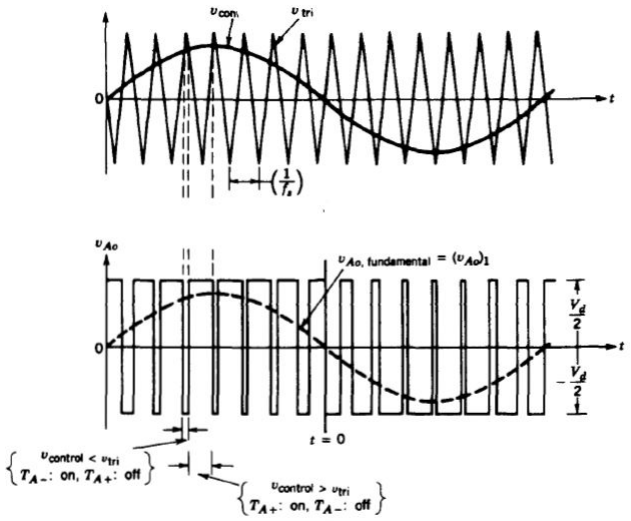

Figure 2.3: Sinusoidal pulse width modulation waveforms [18]

It is the modulating frequency f_1 of v_{con} that verify if the output voltage is not a clean sinusoidal waveform. The amplitude modulation can be expressed by the peak value of the two signals in Equation 2.2.

$$m_a = \frac{v_{con}}{v_{tri}} \tag{2.2}$$

v_{tri} determines the switching frequency (f_s) of the converter. If the frequency of v_{tri} is of an odd multiple integer of the fundamental frequency, no even harmonics will exist in the waveform. In a balanced three phase AC system all zero sequence components (third, ninth...etc.) will be eliminated in the line voltages [11, 19]

The 2-level converter has drawbacks with power losses because of a high switching frequency leading to high amounts of harmonics and a low efficiency. Another drawback of the 2-level converter is that if it is wanted to increase the power rating, more and more IGBTs have to be connected in series[11].

2.2 Topology and Operation of the Half-Bridge MMC

The two main topologies of the MMC used for VSC-HVDC today are named half bridge and full-bridge. The half bridge MMC topology is the one that will be considered in this thesis. In the half bridge, sub-modules (SMs) are assumed to be ideal voltage sources always having a constant voltage at the DC terminals. Figure 2.4 (a) present the topology of a three phase half bridge MMC and (b) shows the configuration of how a SM is designed[11, 18].

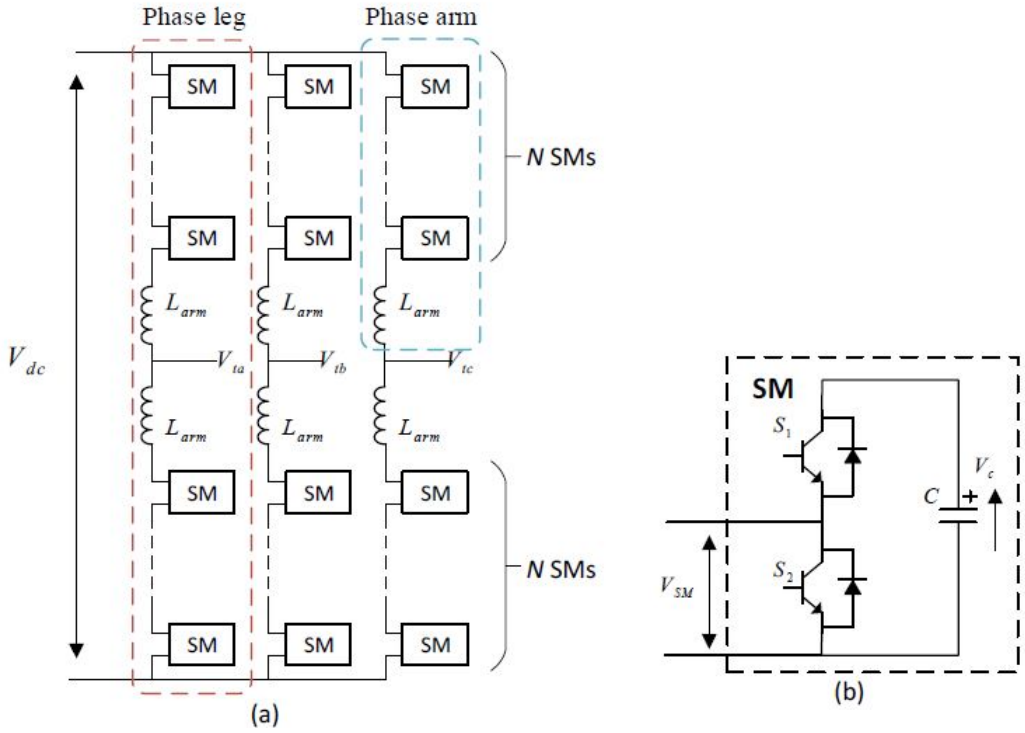

Figure 2.4: (a) shows the topology of a half bridge MMC with N SMs, while (b) presents the configuration of a SM[20]

As can be seen on the figure the converter has three phase legs, where each phase leg has one positive and one negative phase arm. The phase arms consists of a number of SMs in a string which again is connected in series. The SM contains two IGBTs, each connected across a freewheeling diode and in parallel with a capacitor)[18]. The freewheeling diode has the purpose of reducing over voltages (voltage spikes) due to the reverse recovery current at turn-off [19]. The capacitor should have a large capacitance and high voltage capability to maintain a stable voltage during commutation. The arm inductors are important for reducing the circulating current harmonics that occurs due to the SM switching[11]. The AC terminal is connected to the midpoint of the converter in the interconnection of the two arm inductors [21].

There are three operating states of the SM that exist, namely "inserted", "bypassed" and "blocked". The switching sequence of a SM is explained by using Figure 2.5 and is the following: In "inserted", (ON state) S1 is on and S2 is off. The output voltage of the

SM, V_{SM} is in this state equal to the capacitor voltage V_c. The capacitor will charge with positive current and discharge with negative current. If "bypassed", (OFF state) the lower switch S2 is on and S1 is off. V_{SM} is zero and the voltage of the capacitor is constant. When the switching state is "blocking", both S1 and S2 are off meaning that the current can only conduct trough the freewheeling diodes. In this state capacitors will charge with positive currents, but it should ideally not discharge with negative currents [21]. The output voltage of the SM can explained by equation:

$$V_{SM} = sV_c \tag{2.3}$$

Where V_c is the capacitor voltage, s can be either 0 or 1, 0 if bypassed and 1 if inserted.

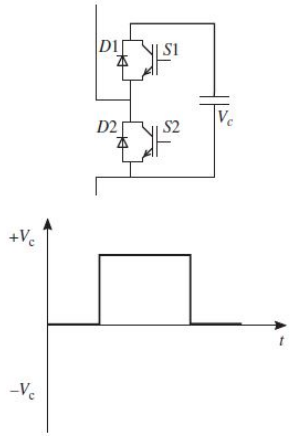

Figure 2.5: Upper and lower SM string voltages during one cycle[18]

By connecting SMs in series forming a string it is possible for the converter to operate with a higher terminal voltage since the voltage level is depending on how many SMs connected. Converters designed for high voltage can contain strings with hundreds of SMs connected in series. Using a high level of SMs will result in a more complex converter with more levels where each level will be smaller in size creating an almost sinusoidal output voltage [18, 21]. A MMC with N SMs per arm has N+1 number of phase voltage levels[20]. The number of voltage levels and output voltage is depicted in Figure 2.6.

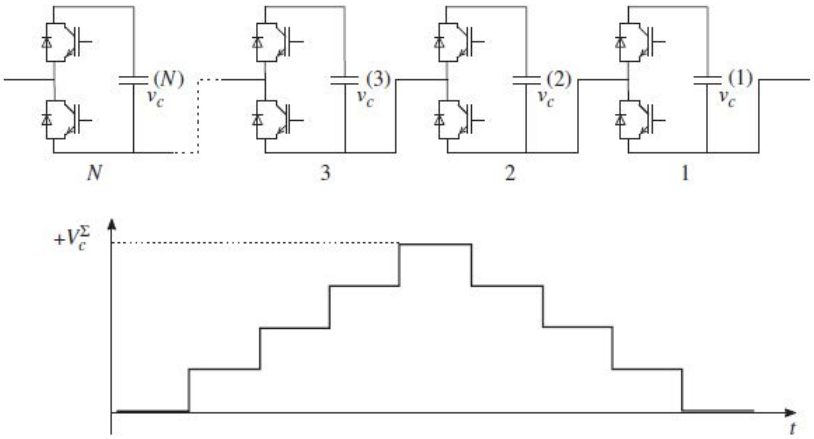

Figure 2.6: Possible voltage levels for a half bridge string[18]

2.2.1 Nearest Level Control

A modulation technique that will be used for the half-bridge MMC in this thesis is the nearest level control (NLC). NLC is a good modulation method when operating with converters that has a high number of SMs per phase arm. This makes the AC voltage being generated as steps leading to less commutations each semiconductor and lower switching losses. Because of the high number of SMs in each phase arm, the low frequency harmonics and the filter requirements becomes lower. The sampling time in the NLC can either be fixed or variable.

When the NLC operates with a fixed sampling time the variation between the voltage steps will make the voltage output deviate from the desired AC waveform. It is important that the sampling time is low so the variation in the AC voltage is only one step and not multiple steps. The reference voltage is then approximated to the nearest level that is available. This behaviour can be seen in Figure 2.7[18, 22].

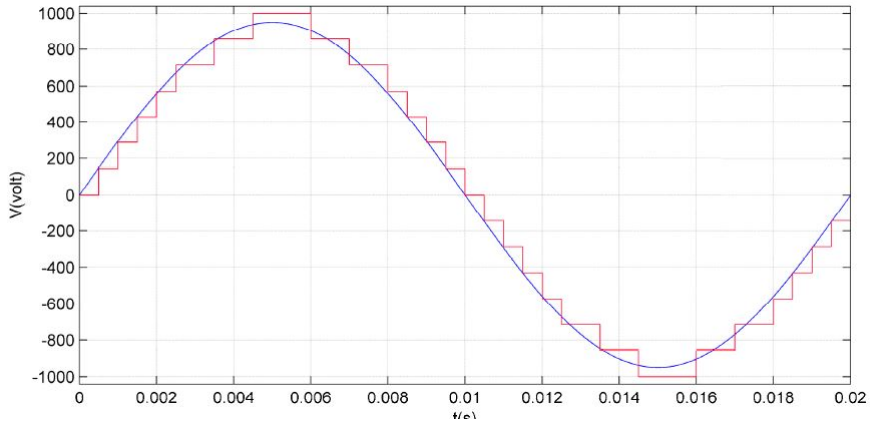

Figure 2.7: NLC with fixed sampling period. The sinusoidal reference is marked in blue and the generated voltage is red[22]

When operating with a variable sampling period, the switching in the between the levels occurs when the sinusoidal reference exceeds the "middle" value between the two levels. An example of this can be seen on Figure 2.8. This method has the advantage of balancing the capacitor voltage in each SM[18, 22].

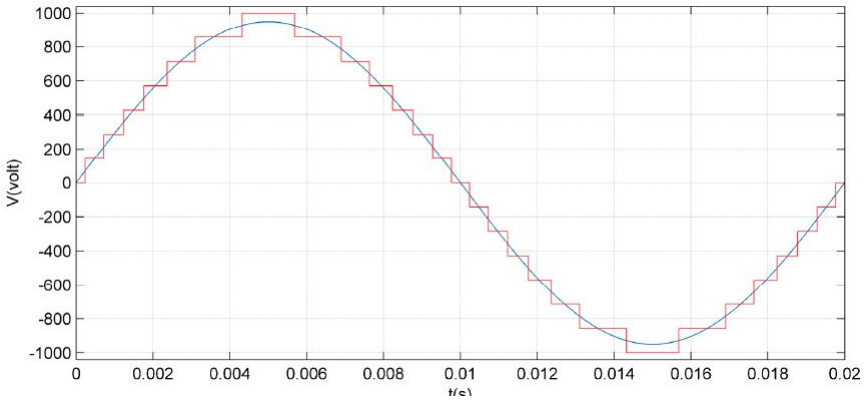

Figure 2.8: NLC with varied sampling period. The sinusoidal reference is marked in blue and the generated voltage is red[22]

Chapter 3

System and Control of VSC-HVDC Systems

This chapter introduces the upper level control structure, and the theory for control modes used for the VSC control scheme. First the hierarchy and upper level control scheme for the 1-D controller is described. Then the current vector control scheme is explained followed by the PI-controller. At last, three voltage control schemes are explained, namely DC voltage droop control, master-slave strategy and the AC voltage droop.

3.1 Control of VSC-HVDC systems

The control structure of a VSC-HVDC can be separated into the following three levels, dispatch control, upper level control and lower level control. Figure 3.1 illustrates the control hierarchy with dispatch control being the control on top sending the dispatch settings onto the upper level control, from here signals are further distributed down the the lower level controls. According to [6] the definition of the dispatch controller is; "the control mode refers to how functionality of the converter is operated, DC voltage control, power control of frequency, and AC voltage control vs. reactive power Q or power factor control". The dispatch control is responsible for changing control settings at the converter terminals when it is needed, and provides the reference signals, P_{ac}, V_{dc}, Q_{ac}, and V_{ac} for the upper level control [6]. For the four control modes, P_{ac} control the converter will be set as rectifier/inverter to inject/consume to/from the grid, also known as a slave bus in the master-slave control structure. In V_{dc} control the converter is set as maintaining a fixed voltage in the DC grid, making the V_{dc} as a control mode that can inject/withdraw power to maintain a stable DC grid, also known as a master bus in the master-slave control strategy.

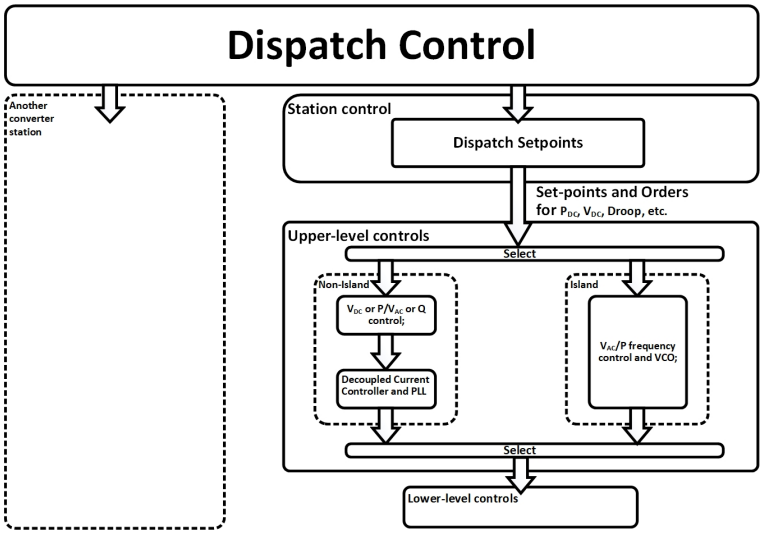

Figure 3.1: Control hierarchy of the non-islanded VSC controls [6]

The upper level control receives orders/set-points from the dispatch control and provides reference signals to the lower level controls. The configuration of the controller is changed based on if the control is connected to a non-islanded or islanded system. The non-islanded control mode is used when the converter is connected to an AC system with active synchronous generation. Figure 3.3 shows the standard upper level control scheme configuration when using current vector control [6].

3.1.1 Upper Level Control

When looking into the upper level control scheme it is of big help to represent the different control modes of the control scheme to understand their behaviour. Figure 3.2 depicts a VSC converter connected to a equivalent grid. The figure displays where the parameters P_{ac}, V_{dc}, Q_{dc} and V_{ac} are measured and fed into the control of the VSC [23, 24].

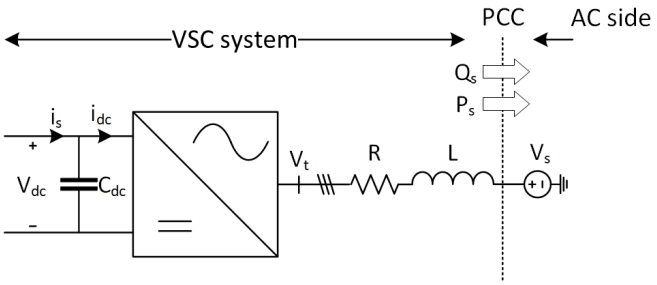

Figure 3.2: VSC connected to a passive network

In the the figure V_s represent grid voltage, V_t converter voltage, P_{ac} active power flow, Q_{ac} reactive power flow, the RL filter, the DC capacitor C_{dc} and V_{dc} which measures the DC voltage level at the DC side of the converter. Because of the VSC capability of controlling

the current in both d-axis (i_d) and q-axis (i_q). The control scheme is divided where the d-axis controls V_{dc} and P_{ac} produces reference for i_d and in q-axis control where Q_{ac} or V_{ac} provides a reference for i_q. This Control scheme is conducted by implementing a current vector control[23, 24].

The upper level control structure for VSC for the 1-D controller used by CIGRE [6] is depicted in Figure 3.3. The figure displays the control loops for d-axis and q-axis and that the reference signals i_d^* and i_1^* is further distributed to the decoupled current controller.

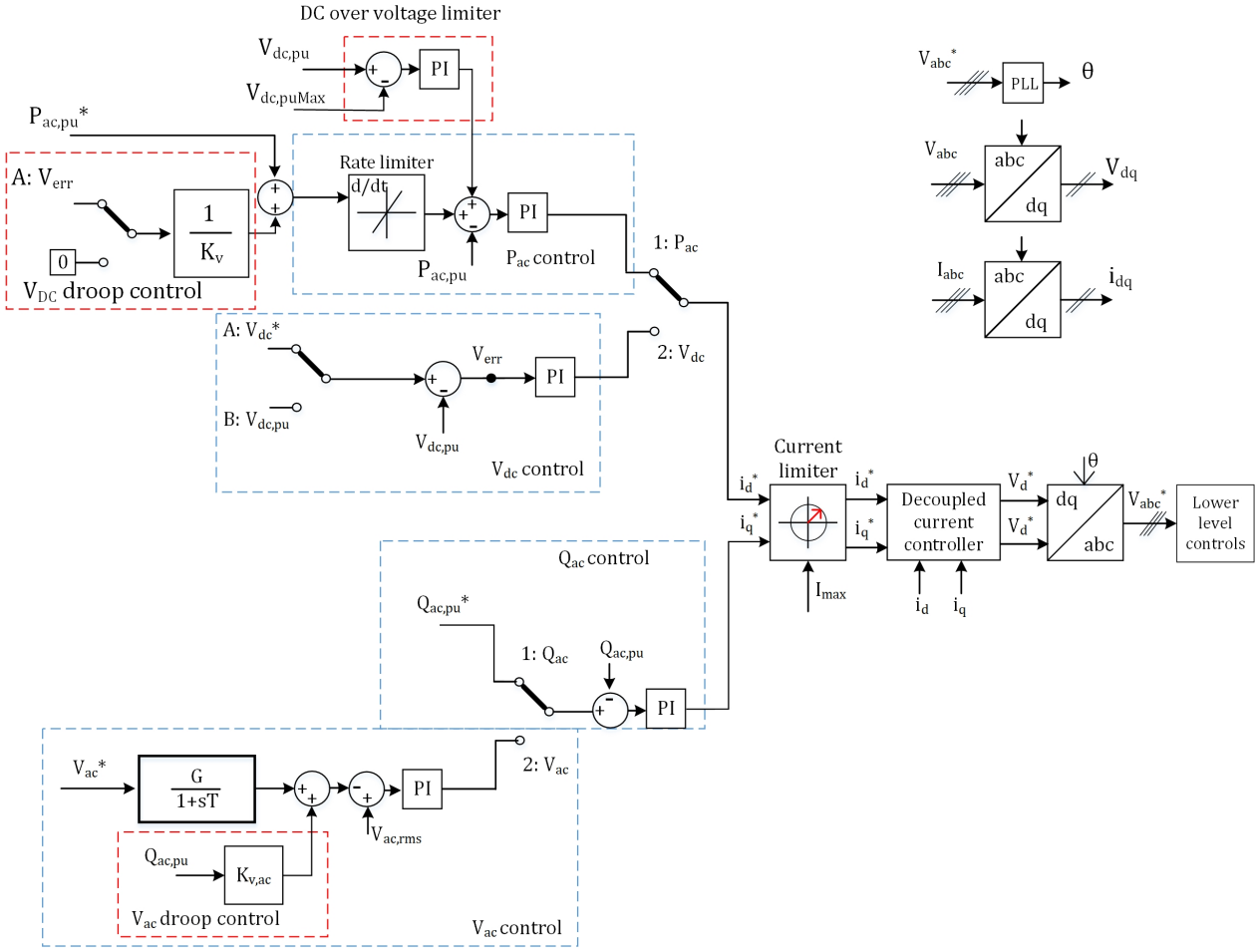

Figure 3.3: The upper level control structure for VSC[6]

The control structure shows for the d-axis control loop that if the control mode is set to operate as V_{dc} control, the control loop will use V_{dc}^* and subtract $V_{dc,pu}$, where the difference (error) V_{err} will be passed on to the PI controller. When the control mode is set to P_{ac} control the switch shown in P_{ac} control loop will be set to state B, which will eliminate the droop control term. When the controller operates in P_{ac} control the difference between P_{ac}^* and $P_{ac,pu}$ will be sent as the error into the PI controller. If the control mode is set as DC voltage droop control, the switch choosing between V_{dc} and P_{ac} will be set to P_{ac} and the

switch in P_{ac} control be set to state B, here the V_{dc_err} will be multiplied with $\frac{1}{K_v}$. $V_{dc_err}\frac{1}{K_v}$ is then added together with $P_{ac,pu}$ before the error is sent to the PI-controller. The result of this addition is then subtracted by $P^*_{ac,pu}$. This means that the error passed on to the PI-controller in droop control mode for d-axis can be expressed by Equation 3.1 and for q-axis in Equation 3.2:

$$error_{DC,droop} = (V^*_{dc,pu} - V_{dc,pu})\frac{1}{K_v} + (P^*_{ac,pu} - P_{ac,pu}) \tag{3.1}$$

$$error_{AC,droop} = V_{ac,rms} - (V^*_{ac} + K_{v,ac} \cdot Q_{ac,pu}) \tag{3.2}$$

The q-axis loop is presented as a cascaded system. When the control mode is operating in Q_{ac} control the error is the difference between $Q^*_{ac,pu}$ and $Q_{ac,pu}$. In V_{ac} control it can be seen that both V_{ac} and $Q_{ac,pu}$ are inputs in the V_{ac} loop where both values are subtracted from the $V_{ac,rms}$. Since V_{ac} and Q_{ac} are measured at the same PCC as shown in Figure 3.2, the operation of the V_{ac} loop can evaluated in a way so that the V_{ac} control provides a "reference" for the reactive power control. The reactive power control will then adjust its behaviour after the value of the V_{ac}. In AC droop control the same principle will work as for the V_{ac} control, it is just that the $Q_{ac,pu}$ will be multiplied by the droop constant K_v.

The i^*_q and i^*_d provided by the d-axis and q-axis control loops are then sent into a decoupled current controller. The decoupled current controller will allow control of both i_d and i_q individually. Hence it is possible to control both P_{ac} and Q_{ac} individually which are sent into the grid to contribute to a stable grid voltage and power angle[6].

3.2 Current Vector Control

Current vector control is a common method to control VSC-HVDC systems. The method represents 3-phase signals as 2-static signals in a 2-dimensional system known as d-q reference frame. It also has the possibility for independent control of active and reactive power. This allows for the use of PI controllers to remove static errors [14]

The transformation from three phase signals to two phase rotating signals in a 2 axis, 2 dimensional system is represented by the following steps:

- Transformation from the stationary abc reference frame (three phase signals) to the stationary $\alpha\beta$ reference frame, also named Clark transformation
- Transformation from the stationary $\alpha\beta$ reference frame to the synchronously rotating d-q reference frame, also referred to as Parks transformation

In current vector control, the currents i^*_d and i^*_q can be controlled separately. The current i^*_d controls either active power or DC voltage, while i^*_q regulates Q into a strong grid or supports with AC voltage when connected to a weak grid[25]. To control both i_d and i_q separately, two equivalent circuits can be obtained from Figure 3.2, which is depicted in Figure 3.4.

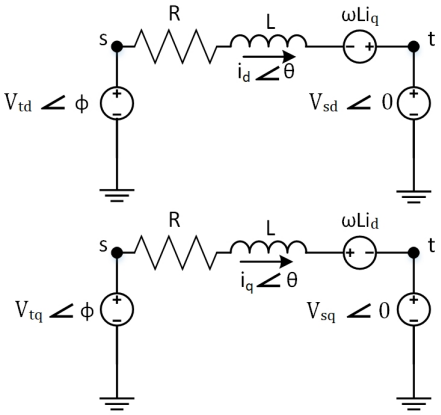

Figure 3.4: (a) Equivalent circuit for calculating the active and reactive power[23]

The equivalent circuits can be used to obtain equations for P_{ac} and Q_{ac} as Equation 3.3 and Equation 3.4.

$$P_{dq} = \frac{3}{2} V_{td} i_d \tag{3.3}$$

$$Q_{dq} = -\frac{3}{2} V_{td} i_q \tag{3.4}$$

As it can be observed, V_{sq} do not appear in the equations since V_t is always aligned with the V_{td} to ensure a stable system[23].

The reference currents i_d^* and i_q^* are then sent to a current limiter block. The current limiter limits the magnitude of the current to i_{max}. Figure 3.5 shows how the current limiter limits the reference currents i_d^* and i_q^* and are sent to the decoupled current controller. The decoupled current controller generates the reference voltages V_d^* and V_q^* and sends them to the reference frame transformation block, where the voltage is synchronized with the angle from the PLL. The reference voltage V_{abc} is then sent to the lower level controls [6].

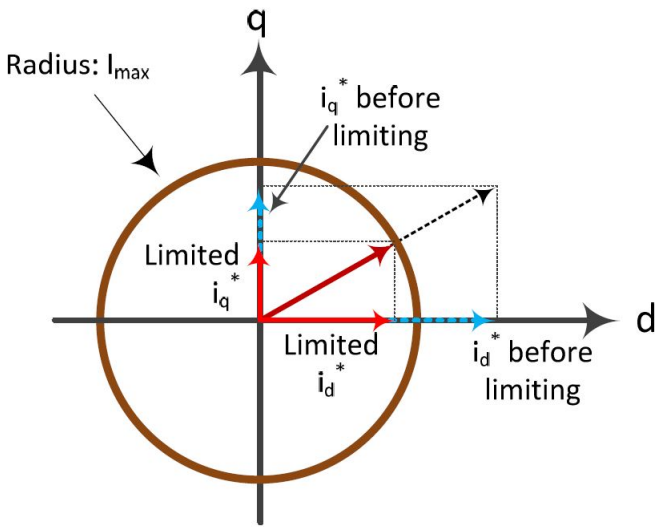

Figure 3.5: Current limiting scheme showing how the reference currents i_d and i_q are limited [6]

3.2.1 Clarks Transformation

In this transformation the three phase signals are represented as a 3-axis, 2 dimensional plane namely stationary abc reference frame. Each axis in the 3-axis plane are placed with 120° between each other. This is also illustrated by the following equations. The representation of abc reference frame displayed together with the stationary $\alpha\beta$ reference frame is shown in Figure 3.6

$$f_a = f_{peak}cos(\omega t)$$
$$f_b = f_{peak}cos(\omega t - 120°)$$
$$f_c = f_{peak}cos(\omega t + 120°)$$

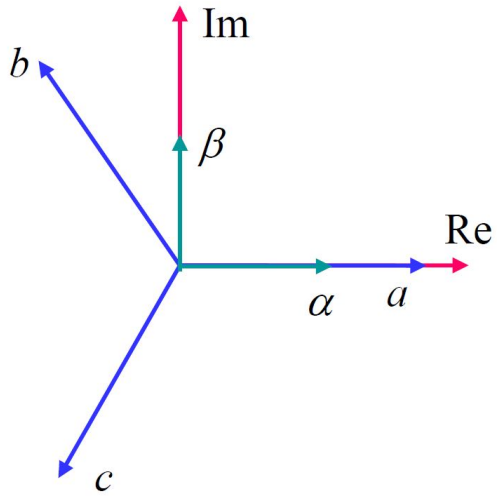

Figure 3.6: Representation of the abc and $\alpha\beta$ in the same coordinate system

It can be seen in the figure that the α axis is aligned with the real axis and the β axis is aligned with the imaginary axis with 90° separation between the axes.

The Clarks transformation from abc to $\alpha\beta$ reference frame is:

$$\begin{bmatrix} f_\alpha \\ f_\beta \\ 0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix}$$

3.2.2 Parks Transformation

The $\alpha\beta$ reference frame can be transformed into a rotating d-q reference frame by using Park/inverse Park transformation. In the d-q frame the d-axis is aligned with the real axis and the q-axis is always 90° projected from the d-axis at all times. The d-q frame is synchronized with the grid the voltage and currents will appear as constant d-q frame vectors as can be seen in Figure 3.7 [23, 25].

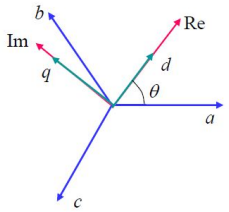

Figure 3.7: Representation of the rotating d-q reference frame [26]

When transforming from $\alpha\beta$ to d-q reference frame the angle between the α axis and the d-axis is used. The voltage vector position is expressed by:

$$\theta = tan^{-1}(\frac{V_\beta}{V_\alpha}) \tag{3.5}$$

V_α and V_β are the voltage components of the $\alpha\beta$ reference frame. This angle is important for having independent control of active and reactive power.

The parks transformation matrix from $\alpha\beta$ to d-q frame is shown in:

$$\begin{bmatrix} f_d \\ f_q \\ f_0 \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta & 0 \\ -sin\theta & cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} f_\alpha \\ f_\beta \\ f_0 \end{bmatrix}$$

In Equation 3.5, the value of θ is obtained by using the phase lock loop (PLL) technique [14]. The PLL tracks the phase angle of the AC grid, and gives a reference signal to the converter controller in order to synchronize with the grid [11]. In the PLL, it is chosen to set the voltage vector of phase-a equal to the d-axis at a point of common coupling (PCC), since the PLL operates in steady state. The phase lock loop should be locked onto the phase-a vector at the PCC. PCC represents where the VSC is physically connected to the ac grid. [25].

3.3 PI Controller

Since PI controllers are often used in control loops and some places in the VSC control structure, it is of good knowledge to understand its behaviour and how to perform tuning of a PI controller. This section presents the PI controller followed by its transfer function and tuning.

The objective of a PI controller is to remove the difference between a set-point and a desired steady-state (S.S) value. The PI controller consists of a proportional (P) and an integral (I) gain. These two controller gains are both multiplied with the error of the system. If the I-term in a PI controller is set to zero, the PI controller is equal to the P controller. A drawback with the P-controller is that it will not have the ability to remove steady state errors completely from the system. With a PI controller this problem is solved since the I-term is used to integrate the error over time and remove its steady-state error during operation.

A representation of the PI controller as a block diagram is depicted in Figure 3.8. The PI controller is set to control an actuator/plant which represent the actual system a PI controller is set to control. It can be seen that the PI-controller operates as a feedback loop, which means that the controller will go in a loop until the error between the reference and the measured value is eliminated.

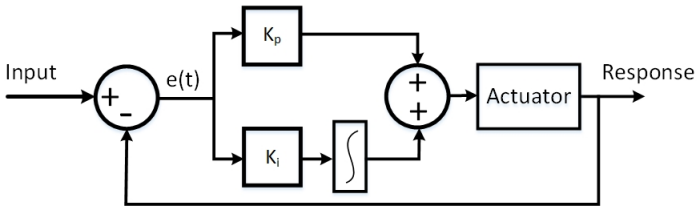

Figure 3.8: Generic representation of a PI controller

The block diagram of the PI controller can be represented as the in Equation 3.6. It is first expressed in the time domain, then transformed and represented in the Laplace domain.

$$\begin{aligned} g(t) &= e(t) \cdot K_p + K_i \int e(t) \cdot dt \\ &\Downarrow \\ &\mathcal{F}\{g(t)\} \\ &\Downarrow \\ G(s) &= K_p + \frac{K_i}{s} = K_p + \frac{1}{T_i s} \end{aligned} \tag{3.6}$$

Here, K_p represents the proportional gain, K_i represents the integration gain. When tuning, having a high K_p will create a large change in the output for a given change in the error. A too large K_p can make the system unstable. On the other hand, a small K_p makes the system less sensitive meaning that it will have a small response to a large input error. A too low K_p can create a situation where the system does not manage to respond good enough to system disturbances[27].

T_i is a constant that is used to describe how much weight that should be put onto the integral factor compared to the proportional part. It is important to notice that $K_i = \frac{1}{T_i}$ meaning that a higher T_i gives a small contribution from the integral part, and a lower T_i gives a higher contribution. The size of T_i is important for how fast the error can be removed. If T_i is set to infinite, the contribution from the integral term will be zero. The higher the T_i the longer the time to reach the final value. A too low T_i can lead to oscillations and an unstable system. The tuning of the PI controller is based on adjusting the values of K_p and T_i[14, 28, 29].

3.3.1 PI Controller Tuning

It is important to implement the correct tuning gains in the PI controller in order to make it work properly. In a HVDC system, the PI controller should be tuned as a compromise between how fast the response should be, how stable the system is going to be during a small disturbance and how robust it is towards large disturbances in the signal. The outer loop should be tuned to towards stability and to have the best regulation (little disturbance). The outer voltage loop should also work to stabilize the DC voltage, hence this is how the PI controller should be tuned. The inner control loop should be tuned to have a fast response. When PI controllers are arranged in a cascaded arrangement, the outer loop should be so slow that it will always be able to read a S.S value from the inner PI controller, hence normally it should be 10 times slower than the inner control loop[14].

3.3.2 Evaluation of a 2.Order System

The objective of this subsection is to present and explain important factors when evaluating the performance of a PI-controller and tune to it correctly. A generic transfer function for a

2.order system in the Laplace domain can be defined as Equation 3.7 [30]:

$$Y(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + 1} R(s) \tag{3.7}$$

Here, ω_n is the natural frequency, ζ is the damping coefficient which can be decided based on the wanted performance within the operating range of the system, R(s) is the output, and Y(s) is the input. To evaluate the performance of a 2.order system, the unit step response shown in Figure 3.9 can be used.

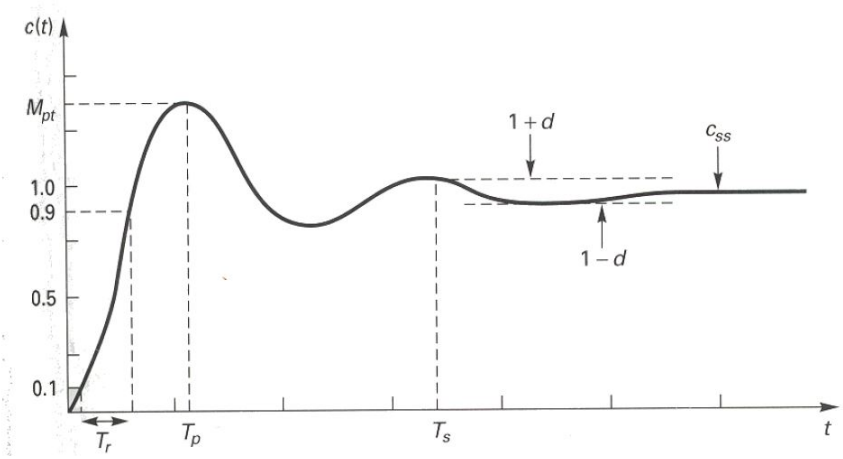

Figure 3.9: Unit step response for a 2.order system showing different terms as rise time, peak amplitude and final value [31]

The parameter T_r represents the rise time of the system and is according to [31] referred to as "the time it takes for a response to rise from 10 % of its final value to 90% of its final value". C_{ss} is the final value of the response. The peak value is denoted as M_{pt}, and T_p is the time it takes to reach this peak value. The overshoot is defined in percentage as the difference between the peak value and the final value, as can also be seen in the equation below[30]:

$$Overshoot = \frac{M_{Pt} - C_{ss}}{C_{ss}} \cdot 100 \tag{3.8}$$

The settling time T_s is according to [30] defined as "the time required to for the system to settle within a certain percentage delta ("d") of the input amplitude". The delta (d) can be seen in Figure 3.9 as the area 1-d, and 1+d. For a 2.order system it is wanted to find the T_s when it is approximately 1% or 2% of the final value. To have the system settle at its final value within 2% around 4 time constants are needed. This Equation 3.9 where T_s can be calculated by the 2% criteria [30, 31].

$$T_s = 4\tau = \frac{4}{\zeta\omega_n} \tag{3.9}$$

All parameters described above can be used to evaluate the performance of the 2.order system. Especially the overshoot and T_s are important parameters for evaluating stability and speed.

The parameter ζ is known as the damping coefficient and can be determined based on what response is wanted from the system. The definition of all parameters are based on an under-damped system. In an under-damped system $0 < \zeta < 1$, in un-damped system $\zeta = 0$,$\zeta = 1$ gives a critically damped system and $\zeta > 1$ leads to an over-damped system. Figure 3.10 shows different step responses for a 2.order system using various values for ζ. It can be seen that the there is a higher overshoot and also more oscillations when using a ζ equal to 0.2, while ζ equal to 2 the signal use more time to reach the reference value. The natural frequency ω_n is defined as [30, 31]:

$$\omega_n = 2\pi f \tag{3.10}$$

Where f is 50 Hz and the natural frequency of the system.

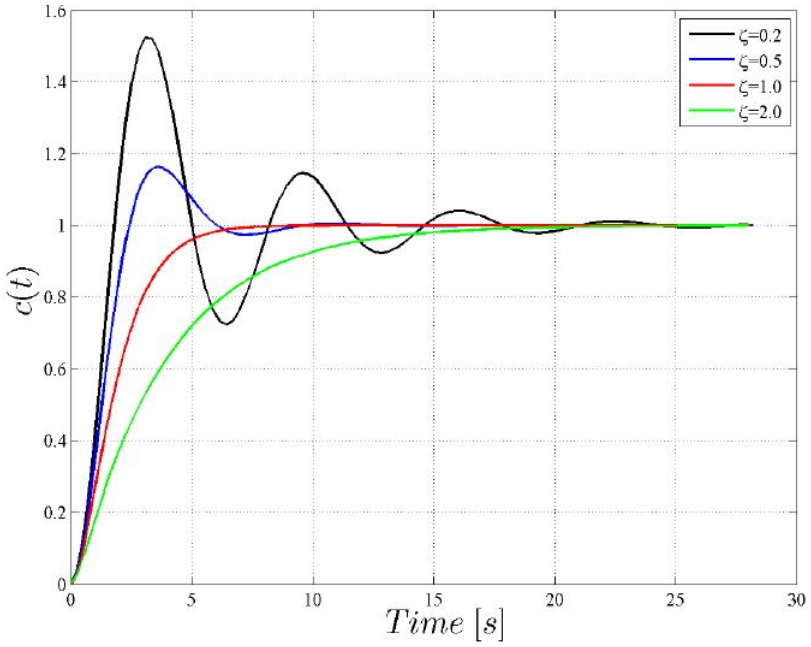

Figure 3.10: Step response for a 2.order system using different values for ζ [32]

3.3.3 Controller Tuning of the DC Voltage Loop

The method used to tune the PI controllers in the upper level control of the 1-D controller is proposed by Akkari [16]. The DC voltage loop can be represented by Figure 3.11 as a block diagram .

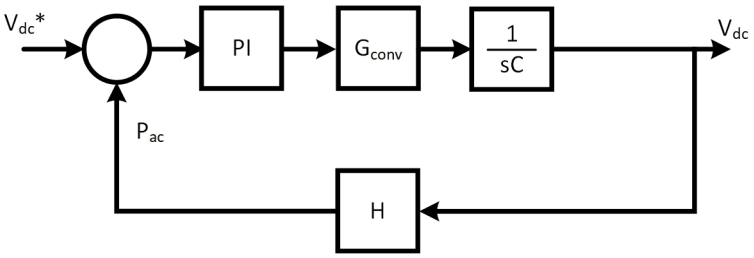

Figure 3.11: DC voltage loop

As it can be seen from the block diagram, the transfer function for the DC loop can be obtained by multiplying the function of the PI controller with the converter and the plant. In order to avoid disturbances with the control loops in series (outer and inner control loops), the outer control loop is usually set as 10 times slower than the inner control (i.e current control), so that the inner control loop is able to complete its loop before the outer control loop. This means that when calculating the transfer function of the DC loop, the inner control can be neglected. The V_{dc} PI control loop will be represented on the following form:

$$G_{V_{dc}}(s) = K_{pV_{dc}} + \frac{K_{iV_{dc}}}{s} \tag{3.11}$$

The transfer function of the plant is $\frac{1}{sC}$ and the converter is represented as a gain with the value of 1. The "sensor" H is used to transform the measured value into a value that can be used in order to calculate the error sent to the PI controller. In this case H has the value of 1.

The closed loop function of the system is:

$$\frac{Vdc}{Vdc,ref} = \frac{G_{PI}G_{conv}G_{plant}H}{1 + G_{PI}G_{conv}G_{plant}H}$$

The transfer function of the DC loop then becomes:

$$\frac{V_{dc}}{V_{dc,ref}}(s) = \frac{1 + \frac{K_{p,V_{dc}}}{k_{i,V_{dc}}}s}{1 + \frac{K_{pV_{dc}}}{K_{iV_{dc}}}s + \frac{C_{dc}}{K_{iV_{dc}}}s^2}$$

The tuning parameters can then be extracted by comparing the transfer function of the DC loop with the second order system transfer function from Equation 3.7. The equations for tuning K_p and T_i in the DC voltage loop is shown below:

$$K_{i,V_{dc}} = \omega_n^2 C_{dc,eq}$$
$$K_{p,V_{dc}} = 2\zeta\omega_n C_{dc,eq}$$

3.3.4 Controller Tuning of AC Power Loop

The principle of the tuning method proposed by Akkari [16] has also been used to obtain the transfer function of the P_{ac} control loop. The P_{ac} control loop is depicted in Figure 3.12.

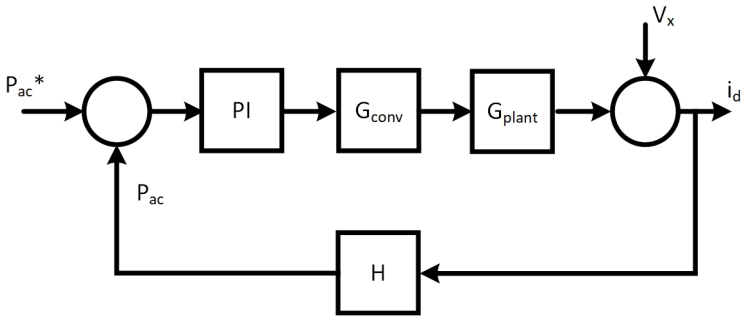

Figure 3.12: Active power loop

By using the PI control loop as shown in section 3.3, the PI control loop can be expressed as the following:

$$G_{P_{ac}} = K_{pP_{ac}} + \frac{K_{iP_{ac}}}{s} \tag{3.12}$$

as well as, H represent a gain which transform i_d into P_{ac} which is equal to 1 pu. It is important to notice that H represent the measured voltage in the system. The transfer function of G_{conv}, which represent the impedance of the low-pass filter is:

$$G_{conv} = \frac{1}{1+Ts} \tag{3.13}$$

Due to the design process the noise from V_x as shown in Figure 3.12 is considered as zero. By combining the gains to create and to obtain a closed loop transfer function, the total transfer function becomes:

$$\frac{i_d}{P_{ac}*} = \frac{G_{P_{ac}} G_{plant} G_{conv} H}{1 + G_{PI} G_{plant} G_{conv} H} \tag{3.14}$$

$$\tag{3.15}$$

From Equation 3.14, the controller gains K_p and K_i can be obtained and is as follows

$$K_{pP_{ac}} = \frac{2\zeta\omega_n}{L} - 1$$

$$K_{iP_{ac}} = \frac{\omega_n^2}{L}$$

Manual Tuning of the PI Controller

There are several ways of tuning a PI-controller, one method that does not require any calculations or equations is the manual tuning method of the PI-controller. The fastest loop (i.e. shortest settling time) is the one adjusted first by either increasing or reducing K_p and T_i. Then the response of the loop is analyzed (by evaluating the parameters explained in subsection 3.3.2 and if it is not good enough, the tuning parameters has to be adjusted and a new simulation has to be conducted. According to [27] there are some rules of thumb when tuning the PI-controller by the trial and error method:

- If the response is oscillating too much then reduce K_p or increase T_i
- If the response time is to long when conducting a step then reduce T_i
- If the dynamic deviation is to big, increase K_p

3.3.5 Integrator Wind-up

For a PI controller where saturation occurs, anti-windup can be implemented to avoid such phenomena where the system cannot respond to changes due to where the signal value has reached beyond the saturation point. Without this action the controller cannot perform any changes in the system before it has moved away from the saturation point. As shown in Figure 3.13, the response time is reduced when such improvement is added to the system. The controller can therefore respond to changes even though the signal value appears outside of the saturation point of the system (i.e. response time of the system Δt is reduced). [28, 33]

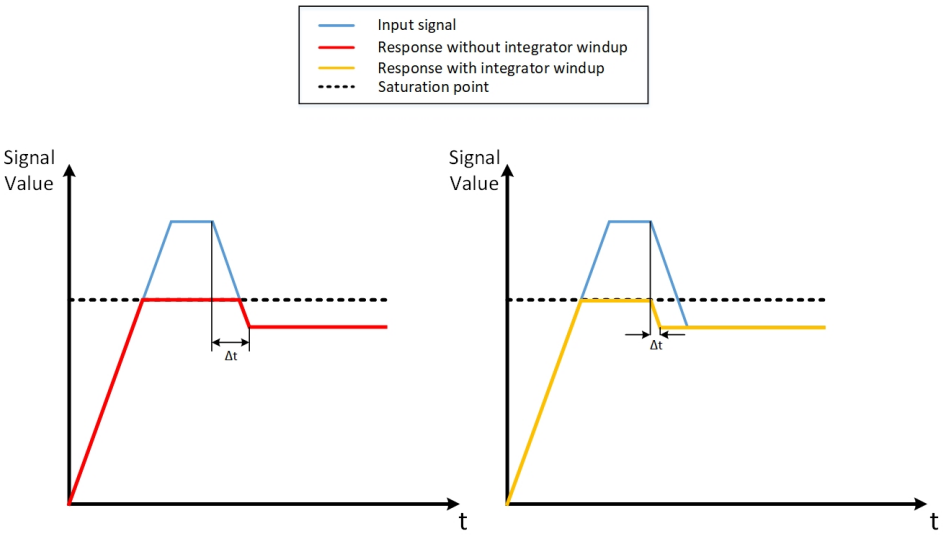

Figure 3.13: Graphical representation of the function of a Integral wind-up

As illustrated in the figure, Δt become reduced when an integrator wind-up is added to the system. A presentation of this addition when implemented in the system is presented in Figure 3.14.

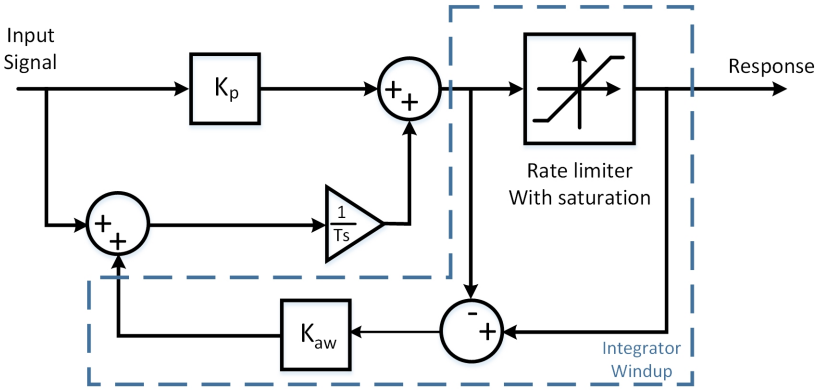

Figure 3.14: Circuit representation of the function of the Integrated integral action added to the PI controller

As depicted, a signal before and after the rate limiter is measured, when these values are not equal, the difference is multiplied with the anti-windup constant and added to the I integrator term to amplify the integrator gain, this will create a behaviour as already illustrated in Figure 3.13

3.4 Voltage Control Methods

Several strategies exist for controlling the voltage. The ones important for this thesis are mentioned here to give an overview of how the methods work.

3.4.1 Master-Slave Strategy

This control strategy is a proposed strategy for controlling power flow within a MTDC system. A control mode which is built on conventional PtP-HVDC control[34]. In a DC network V_{dc} is the signal that will be held as a reference to control and maintain power flow between converters.

The master-slave strategy works with the slave bus operating as a passive load/generation, while the master-station operate to ensure power balance of the system by injecting/consuming power to stabilize the system. The master bus will ensure to control V_{dc}. This means that if V_{dc} decreases, the master converter will inject power to maintain a stable grid, while a slave bus will control a constant power in either inverter/rectifier mode at its PCC. A drawback of the method is that if the master converter is disconnected/trips, the entire system will break down. Also the choice of which converter station that is going to be chosen as the master station will depend on the converters ability to deal with large large power deviations which leads to that the station with the highest power rating to become the master station [35].

3.4.2 DC Voltage Droop Control

The DC voltage droop control is a proposed control strategy that can be used in a MTDC system. This control strategy can be implemented for all the converters present in the dc

grid, meaning that two or more of the converters in the system can contribute to power sharing in the DC grid. the converters that is present will se this as disturbance and will automatically try to stabilize the DC grid.

The droop constant which is implemented in the droop control can dictate the behaviour of the droop slope. By changing the steepness of the droop slope it is possible to change the control mode of converters in the MTDC system. Figure 3.15 depicts these three modes of operation. For voltage control shown in (c) the droop constant has a value of zero, hence the only change will be the power. For power control shown in (b) a fixed power injection/withdrawal in power is conducted no matter the change in DC voltage during operation the droop constant value is ∞ and only the voltage will change. In (a) the converter is in droop control and both the power and the voltage will be controlled at the same time. When the voltage reference in converter is changed the power reference will change accordingly to the droop slope to maintain the stability of the DC grid. This is done by moving the operational point according to the droop slope. The dot on the slopes illustrates the operating point of the converter [36].

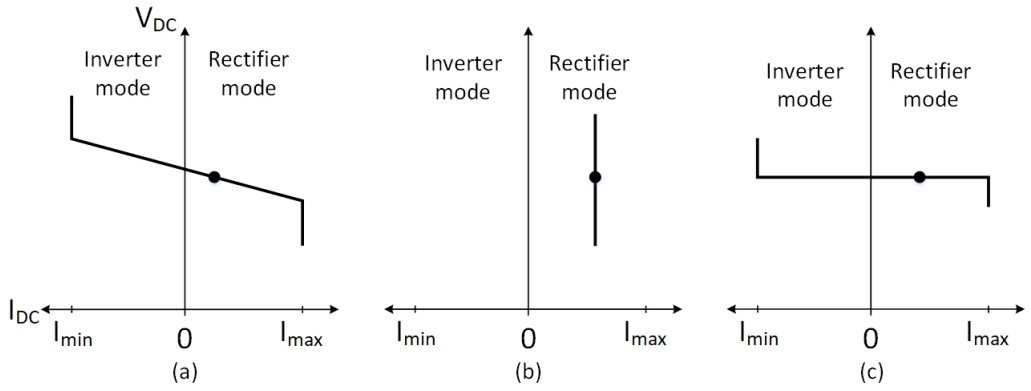

Figure 3.15: (a) Droop control (b) Fixed power flow control (c) Constant voltage control [36]

Equation 3.16 defines how to calculate the power sharing of each converter in the DC system [36].

$$P_{ac} = P^*_{ac} - \frac{1}{K_v}(V_{dc} - V^*_{dc}) \tag{3.16}$$

Where K_v is the droop coefficient, P_{ac^*} is the active power measured at the PCC, (*) is used as notation for reference value. The droop constant is expressed in $\frac{kV}{MW}$. The reference point of the converter is defined as the voltage level when operating in no-load condition (i.e when the converter is neither consuming nor providing active power to the grid).

The droop constant dictates the power sharing in a way so that the converter with the lowest droop constant (K_v) will contribute most to the power sharing within the system and vice versa. This is because the converter with the lowest droop constant will contribute more to the DC voltage control [37]. If there is an outage of one converter in the MTDC system when operating in the droop control strategy, the converter with droop control will be able to participate to voltage control and power stability in the DC grid leading to a higher robustness of the MTDC system [36, 37].

3.4.3 AC Voltage Droop Control

The droop slope in the AC voltage droop control is shown in Figure 3.16. As illustrated, the droop slope of the V_{ac} control is similar to the one of the V_{dc} one. The AC voltage droop is used when two control systems are connected to the same bus. Then the two controllers can adjust the injection or withdrawing of reactive power according to each other. The AC voltage droop is used when the system operates together with converters on the AC side. It is also used for operating with other providers of reactive power which works as AC voltage regulators. If a bus has two or more devices that controls AC voltage it is important that controls are properly coordinated [6].

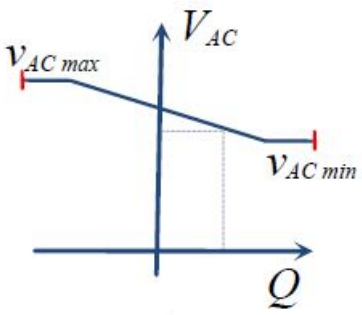

Figure 3.16: V_{ac} droop control [6]

The steepness of the slope shown in Figure 3.16 can be represented as a droop constant, where the inverse of the constant becomes the behaviour of the slope and can be represented as in Equation 3.17:

$$K_{v,AC} = \frac{V_{ACmax} - V_{ACmin}}{Q_{ACmax} - Q_{ACmin}} \tag{3.17}$$

Where $K_{v,AC}$ represent the droop constant in kV/MW, V_{ac} represent AC voltage level as kV and Q_{ac} the reactive power in MW.

In order to obtain the operational boundaries of the reactive power control, it is of good idea look at the operation area of the VSC converter displayed as P/Q diagram, [15] present a HVDC light (VSC) converter in P/Q axis. This P/Q diagram is depicted in Figure 3.17.

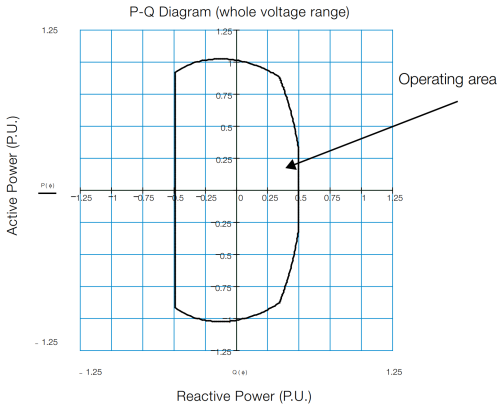

Figure 3.17: P/Q diagram of a VSC [15]

From the figure it can be observed that for a HVDC light converter the range of reactive power operation is defined as ± 0.5 pu of the converter rating, this will be kept as limits during testing and evaluation in the thesis.

Chapter 4

Design, Test and Validation of the 2-D Upper Level Control Scheme

This chapter presents the 2-D upper level control scheme. First it presents the theory behind the error block and how it is designed. This includes the calculation method, limitations, and a visual representation of the error block. In order to validate that the operation of the 2-D upper level control is correct, it is compared with the 1-D controller. Two test setups used for simulations is then presented next. The d-axis control loop will be tested and evaluated. The first case tested is done in order to check if response of the 1-D and 2-D controller is equal when operating in V_{dc} and P_{ac} control implemented with the same tuning gains. Then a trial and error method will be used in order to obtain proposed tuning parameters that can be used for both V_{dc} and P_{ac} control. The proposed tuning parameters will be compared with the ones obtained for the 1-D controller. Then a comparison of the 2-D and 1-D controller operating in droop control using both proposed gains and the 1-D gains. At last it will be validated that the limitations in the d-axis control loop works, meaning that the voltage and power should not exceed their limits. When the d-axis control loop is verified, the same tests for the q-axis control loop will be presented.

As previously explained in section 1.2 and shown in Figure 1.4 it was found that transients are present when performing an uncontrolled switching between the control loops in the 1-D controller. Since these transients can create problems with over-voltage in the system, it is therefore wanted to develop a new controller which can achieve seamless switching between the control loops. The new controller will consist of an error block that will calculate the error passed on to the PI-controller. The inputs to the error block can either be V_{dc} and P_{ac} or V_{ac} and Q_{ac}. It is wanted to only use one PI controller in the d-axis loop, and one in the q-axis loop. This means that the input signals to the error block has to be dependent on each other working as a 2-dimensional scheme, hence it is named 2-D controller.

Currently, little scientific research has been published on the topic of seamless switching between the control loops in a VSC-HVDC control strategy. In fact, the only article found that proposes a control scheme for seamless switching is [38]. The article propose a method which includes 6 parameters needed to be changed, α,β, γ, a, b and c. These parameters can be adjusted to represent the different control modes. There are several conditions for the parameters that determines if the controller operates in constant voltage, power or droop

control. To compare, in the 2-D controller proposed in this thesis it is only needed to adjust the value of a slope by changing 4 parameters; x1,x2,y1,y2. In fact, the results from [38] are not compared to any other control system to ensure that the proposed seamless control is working. It does not show a control system solution for the Q_{ac} and V_{ac} loop, which is something the 2-D control scheme provides. It is also showed in [38] that the switch will be present in the system causing a minor transient when switching. However in the 2-D control structure the switch is removed.

4.1 2-D Upper Level Control Structure

The main component of the 2-D upper-level scheme is the 2-D error block. The purpose of the 2-D error-block is to generate a reference point based on the given set points (x1,y1) and (x2,y2) located in a 2-dimensional plane. The vector that is generated between these two coordinates represent a reference line that the measured coordinated will be projected on. The distance between the generated coordinate on this line and the measured point (x3,y3) represents the error that will be passed on to the PI controller. A representation of the control structure is depicted in Figure 4.1. The 2-D error block is represented for the d-axis control loop with V_{dc} and P_{ac} as input signals. The same applies for the q-axis control loop were V_{ac} and Q_{ac} are input signals to the 2-D error block.

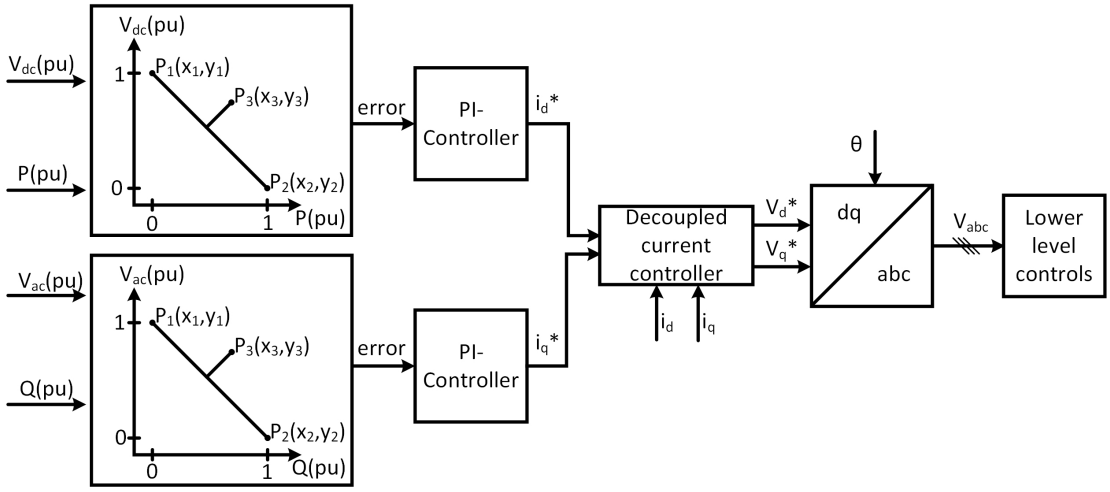

Figure 4.1: Proposed 2-dimensional upper level control scheme

When comparing the 2-D upper level control structure with the 1-D upper level control structure seen in Figure 3.3, is can be observed that there is a reduction of control loops and that the switch between the control modes is removed. In order to test the 2-D control, 1-D will be used as a reference to validate if the 2-D control operate when tested for the same scenarios as the 1-D.

4.1.1 Design of the 2-D Error Block

The error block will work in a way so that the two measured values sent as inputs to the error block will be compared with the reference value and the error between these two parameter will be computed. The computed error will then be sent to a PI controller which has the purpose of eliminating the error. To create the error block, an algorithm was developed in order to calculate the magnitude of the error and implemented as a FORTRAN code in a new block in PSCAD/EMTDC.

The design of the 2-D error block is based on the use of coordinates. The coordinates in x-axis (x1,x2) will control active power or reactive power, while the coordinates in y-axis (y1,y2) will control the AC or DC voltage. Together the coordinates will operate as a reference line where the gradient of the line determines the control operation of the converter. A visual representation of the 2-D error block is displayed in Figure 4.2.

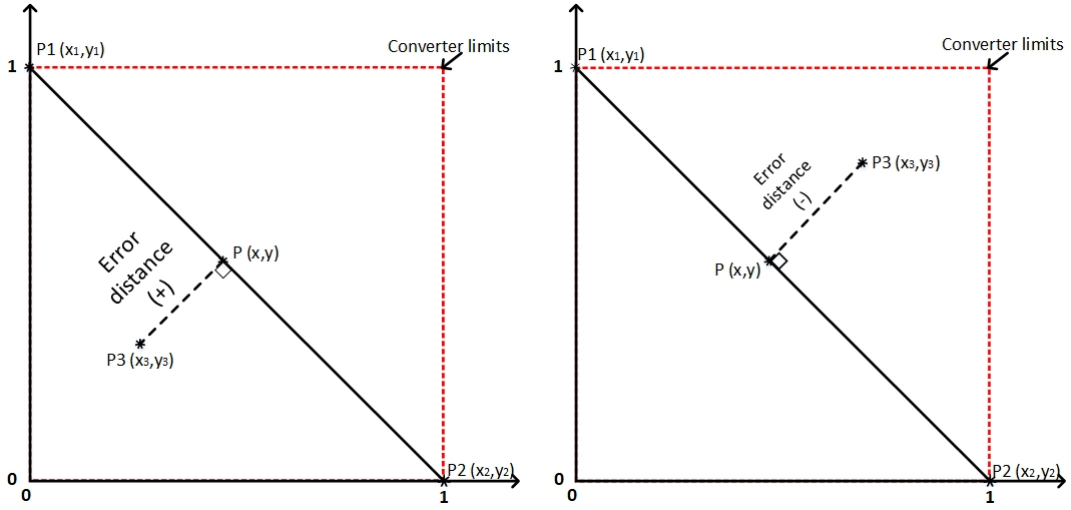

Figure 4.2: Schematic of error block showing how the error is positive or negative depending on which side of the droop line it is

As seen on the figure, the coordinates are given as points; P1(x1,y1), P2(x2,y2), P3(x3,y3) and P(x,y). The error is calculated as the shortest distance between the measured input values (P3) and a reflected point on the droop line (P). The calculation method ensures that the error will always be calculated as the perpendicular distance between the measured values and the reflected point when the converter is operating within its limits. The calculation method is described more in section B.1 and is shown as a FORTRAN code in subsection B.2.1. It can also be seen that the error will have a polarity depending on if it is on the left or right side of the reference line. The polarity of the error is important so the PI controller knows if it should add or subtract in order to reduce the error. The behaviour of the PI controller is illustrated in Figure 4.3.

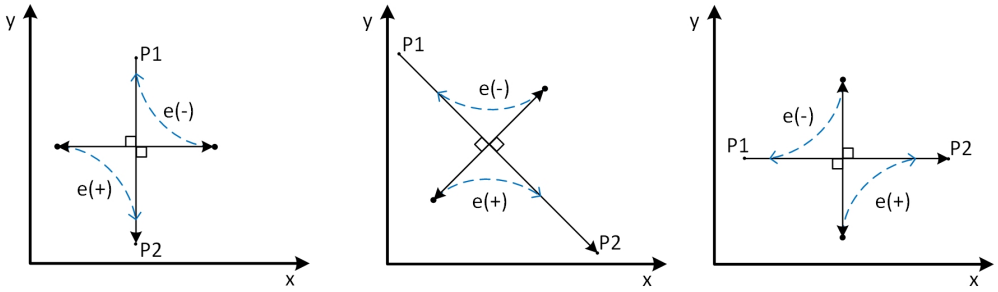

Figure 4.3: Operation of the PI controller when reducing the error between the measured values and the reflected point on the reference line

As seen on Figure 4.2, the red "box" is used to illustrate the operating limits of the controller. The limits for x1 and x2 are determined by the active /reactive power limits of the converter, while the voltage y1 and y2 limits are decided by the DC and AC voltage. The operating limits of the converters in the system are obtained from [6]. The base data for all converters used for simulations in this thesis are shown in Table A.2. The limits for the converters and the system are shown in Table 4.1.

Table 4.1: Limitations of the converters in per-unit

Parameters	**Limitations**	
	Upper [pu]	Lower [pu]
V_{dc} [kV]	1.05	0.95
P_{ac} [MW]	1	-1
V_{ac} [kV]	1.05	0.95
Q_{ac} [MVAr]	0.5	-0.5

The limits of the converter were normalized in order to have the correct scaling in x and y direction. The limits were presented as 0 or 1. As an example, in x-direction for the active power, -800 MW will be represented as 0, and 800 MW as 1. In y-direction for the DC voltage, 0 is represented as 380 kV and 1 as 420 kV. The calculation to normalize the values in both x- and y-axis are presented in Equation 4.1

$$\begin{aligned} X_{scale} &= \frac{x_3 + UpperP}{DeltaP} \\ Y_{scale} &= \frac{y_3 - LowerV}{DeltaV} \end{aligned} \tag{4.1}$$

Here, UpperP is the upper limit of the active or reactive power. DeltaP is the difference

between the upper and the lower value in the active/reactive power. LowerV is the lowest voltage limit while DeltaV is the difference between the upper and lower voltage limit. Since it should be possible to implement the 2-D controller and its algorithm for different HVDC systems, the limits are put as parameters in the algorithm. This is further explained in section B.2.

In a situation where the measured points operates outside the red "box", another method to calculate the error will be used. When the error is located outside the converter limits in x-direction the error will be calculated as the distance between the x-limit (0 or 1) and P3 as depicted in Figure 4.4. If the error is outside the converter limits in y-direction the error will be calculated as the distance between the y-limitation (0 and 1) and P3 as shown in Figure 4.4 (b).

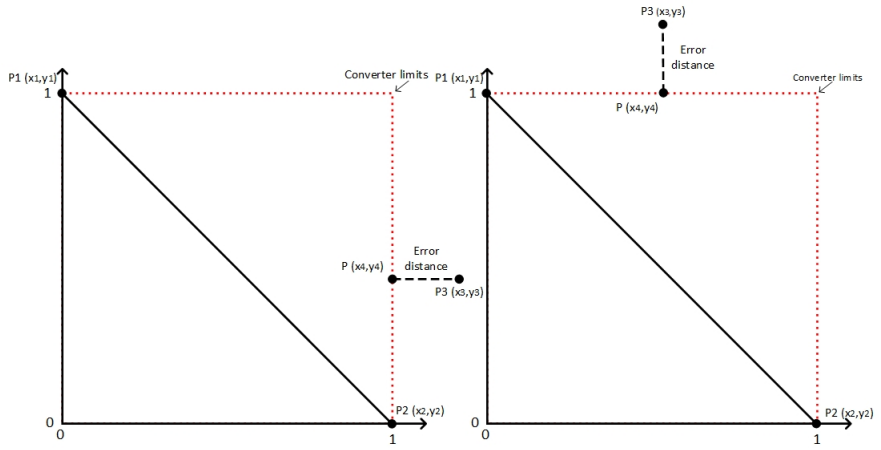

Figure 4.4: The figure to the left (a) shows the error distance in x-direction while figure(b) to the right shows the calculation of the error distance in y-direction

If a case occurs where the measured values are outside both the x- and y-limits the algorithm will prioritize how to reduce the error. This means that it will first reduce the error in one direction, then reduce it in the other. In the algorithm developed for this thesis it is decided to reduce the error first in y-direction, then in the x-direction.

Figure 4.5 presents a flowchart in order to give a better overview of the error block concept and the logic behind it.

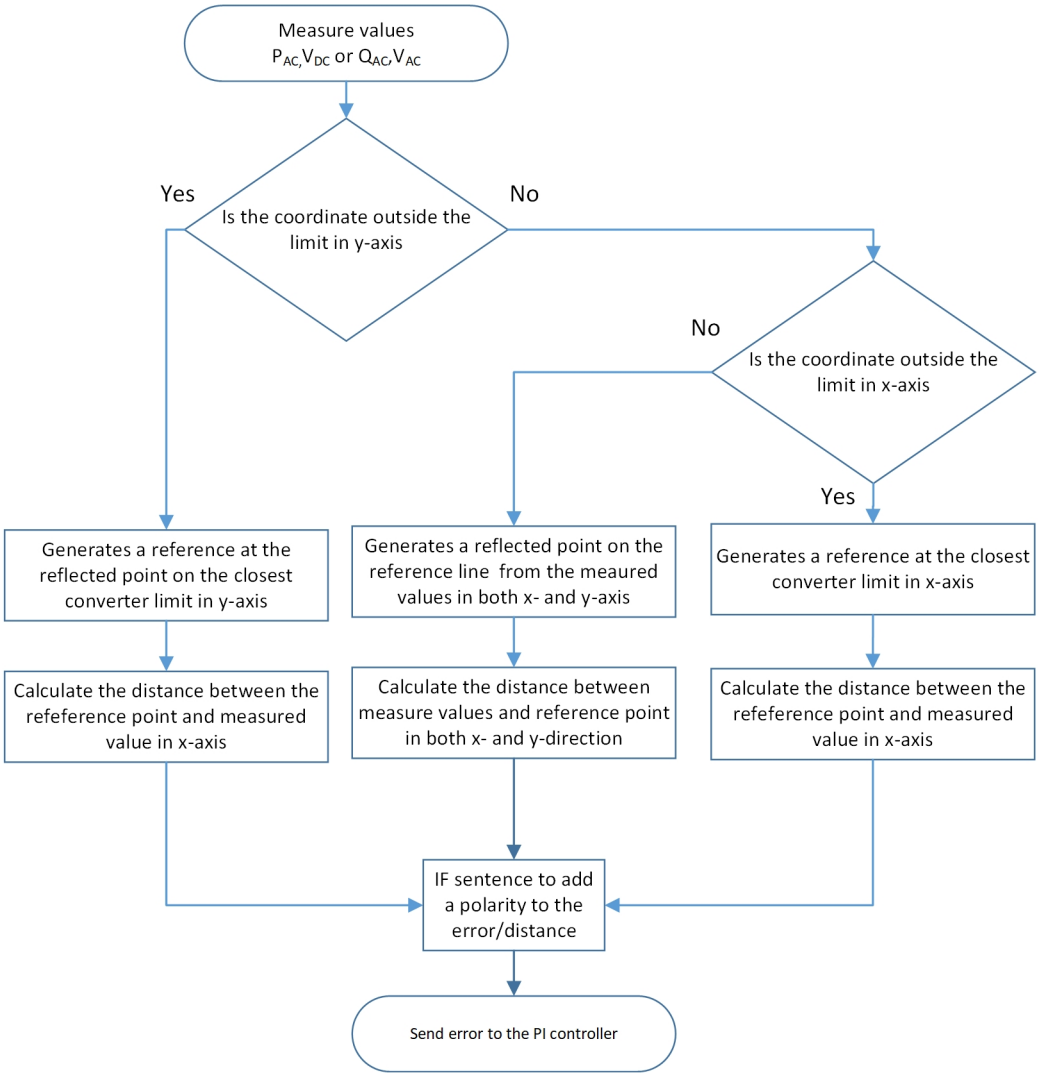

Figure 4.5: Flowchart representing the logic of the 2-D-error block

As depicted in the flowchart, the logic of the algorithm works in a way that measured values sent from the system are inputs to the error block. In the error block, the system operator can set the wanted reference values for example power or voltage references. The reference values are set as a droop slope, and the measured values will be projected on this slope. The error is calculated as the shortest distance between the measured values and the projected point on the droop line. The error is then processed to the PI controller. If the projected point is located outside of the converter limits, the error will be calculated as the distance from measured point to the limit.

4.1.2 Comparison of the Calculation Method in the 1-D And 2-D Controller

In order to fully understand the principle of the 2-D error block it will be of good knowledge to know how the 1-D error is calculated. The way the 1-D controller calculates the error when operating in DC and AC droop control is defined in Equation 3.1 and Equation 3.2. When operating in droop control, it was shown in Equation 3.1 and Equation 3.2 and section B.1 that the error in the 1-D and 2-D controller are not calculated the same way. This is because the 2-D controller calculates a perpendicular value from the measured values to the reference droop line.

In the 1-D controller the error is calculated as the distance in x-direction from the droop line. In the d-axis loop this means that the error will be larger for the 1-D controller compared to the 2-D. Since a PI controller will work faster to reduce a larger error it is expected that the 1-D controller will have a faster response in DC voltage droop control. On the other hand, when operating in the AC droop control it is expected that 2-D will obtain a faster response than that of the 1-D controller. Figure 4.6 depicts how the error is processed for (a) 2-D droop control, (b) 1-D DC droop control and (c) 1-D AC droop control, The figure is presented in a normalized value in order to show more clearly how the error is calculated since, x-axis is of grater range than that of the y-axis, making it hard to give a clear picture if real values were presented.

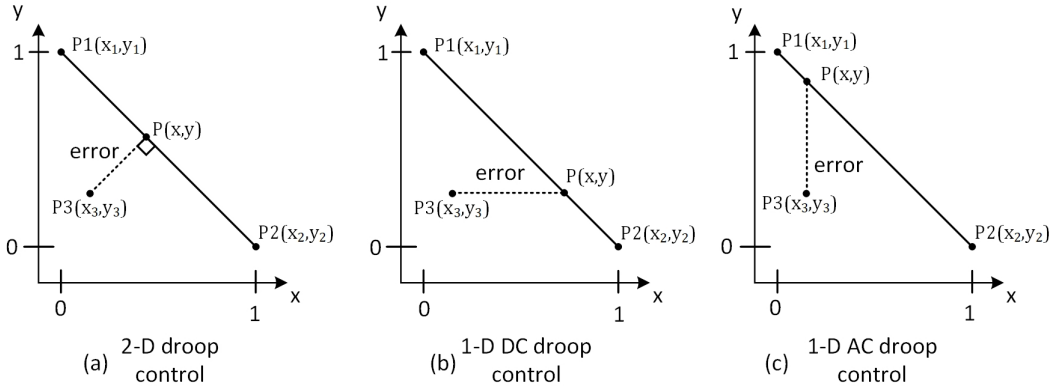

Figure 4.6: Difference between calculation method of the error in 1-D control and 2-D control

4.2 Configuration of the Test Systems

To verify the operation of the 2-D controller it is wanted to test its performance for the following cases:

- A step response when operating in the control modes V_{dc}, P_{ac}, V_{ac} and Q_{ac} has to be conducted. Since the error is calculated in the same way for the 1-D and 2-D controller the response of the step should be the same. If the response is equal the tuning parameters used in the 1-D controller obtained from the CIGRE manual [6] could be used for the 2-D controller as well.

- Since there is only one PI-controller in the d-axis and q-axis of the 2-D controller, a trial and error tuning of each of the PI controller has to be performed to find proposed gains that can work for V_{dc}, P_{ac}, V_{ac}, Q_{ac}, DC and AC voltage droop control.
- Because the error in the droop is calculated differently for the 1-D and 2-D controller it is wanted to test the d-axis and q-axis control loops in droop control.
- Validate voltage and power limits for the constant control modes V_{dc}, P_{ac}, V_{ac} and Q_{ac} to verify if the previously explained limitation concept works

To be able to test the previously mentioned cases, two test configurations has to be designed. Because of the VSC ability to perform voltage control in no-load condition, a test system for this condition where created, meaning that for V_{dc} control the converter will operate as open terminal to create an ideal situation without disturbance from other converters or generation units that are present in a real power system. This configuration is presented in Figure 4.7.

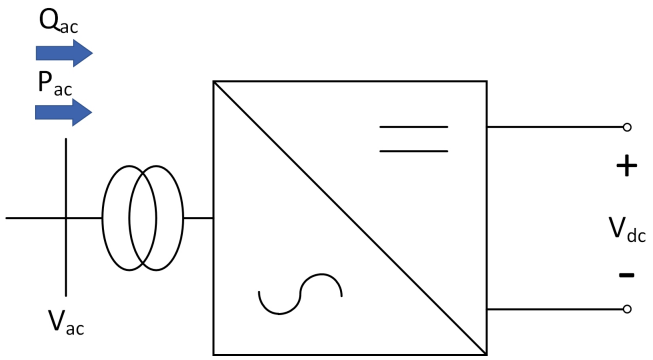

Figure 4.7: Configuration for simulations for converter operating in V_{dc} control

When a system is in P_{ac} control the system will be dependent on a voltage source to maintain a constant voltage in the DC grid, without a voltage source in the system or at least one unit in a larger grid that provide some sort of power control. Since this describes a slave in the master-slave control scheme, the converter will be connected to an ideal case with a voltage source with grounding in the middle and a R_{dc} which will represent a pure cable resistance connected to the terminals of the converter. Figure 4.8 depicts this configuration for the converter when operating in constant power control. In this configuration the converter is connected to a DC voltage source representing $\pm$ 400 kV and two resistances R_{dc} of 5 ohm.

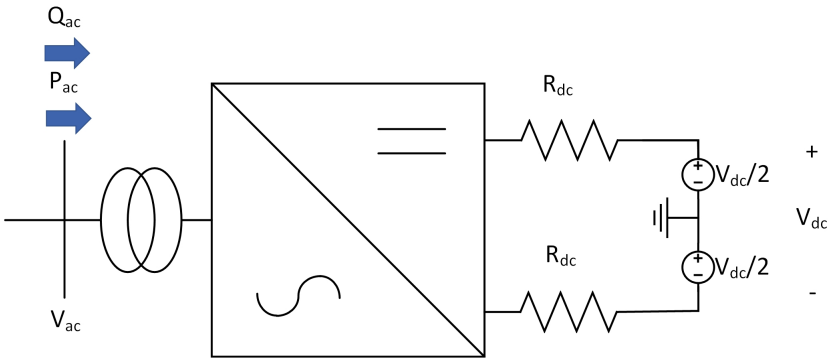

Figure 4.8: Scheme for P-control simulation with one converter connected to two voltage sources and two resistances

4.3 Validation of the d-axis Control Loop

The results in this section are presented in order to validate the d-axis control loop in the 2-D upper level control scheme. The results in the d-axis control loop of the 2-D controller will be compared with the results for the d-axis loop in the 1-D controller. The reason for comparing with the 1-D controller is that the performance of the 1-D controller is already validated to work. If the 2-D controller will work in the same way as the 1-D, then it can be proven that the operation of the 2-D controller is correct.

4.3.1 Response Comparison of The Controllers in the d-axis loop

When operating in V_{dc} and P_{ac} control, the error will be calculated in the same way for the 1-D and the 2-D controller. When the error is equal, it is expected that the response should be the same when comparing the controllers. It is therefore wanted to apply a step in the voltage when the controller operates in V_{dc} control, and a step in power when operating in P_{ac} control.

To compare the response of the 1-D controller and the 2-D controller, both were simulated using equal tuning parameters obtained from [6]. It should be noted that these tuning parameters are considered as extremes. The goal of the simulation was to have the same response for the 1-D controller and the 2-D controller when using the same tuning parameters as the 1-D controller. An equal response will mean that the tuning parameters obtained from [6] developed by using Akkaris method [16], can be applied in the 2-D control as well. Table 4.2 shows the data used for simulations.

Table 4.2: Data for simulations evaluating the response when in V_{dc} and P_{ac} control

Control Mode	K_p	T_i
V_{dc}	8	0.00367
P_{ac}	0	0.0303

Response when Controllers are set to Constant DC Voltage Control

The following simulations are conducted using the configuration depicted in Figure 4.7 and by implementing the tuning parameters for V_{dc} from Table 4.2. The goal of the simulation is to have an equal voltage response for the 1-D controller and the 2-D controller. An increase or decrease in the voltage is applied to check that the controllers have the same response for different voltages.

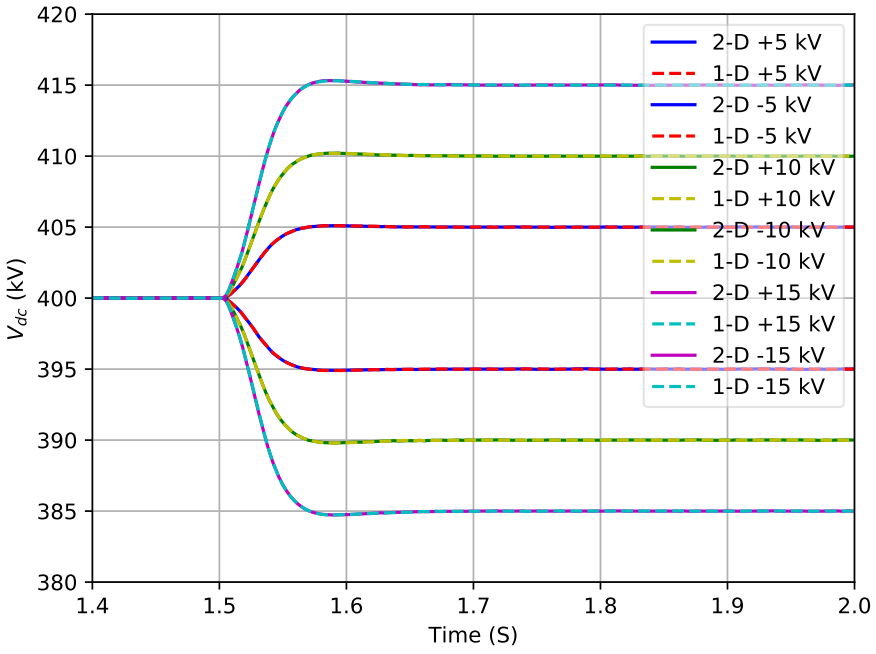

Figure 4.9: Comparison of the two controllers when having different steps in voltage at 1.5 second

When analyzing the results it can be seen that both controllers have an equal voltage response when different voltage steps are applied in the system. This means that the tuning parameters used in the 1-D controller for the constant V_{dc} control can be applied for the 2-D controller. The settling time for the voltage response is approximately 0.15 seconds.

Response when Controllers are set to Constant Power Control

Another simulation was conducted to check if the K_p and T_i used for tuning the P_{ac} control in the 1-D model could be used in the PI for the active power loop of the 2-D controller. The tuning parameters used for simulation are shown in Table 4.2 and the configuration for testing is depicted in Figure 4.8. The results from applying different steps of increase and decrease in power are depicted in Figure 4.10.

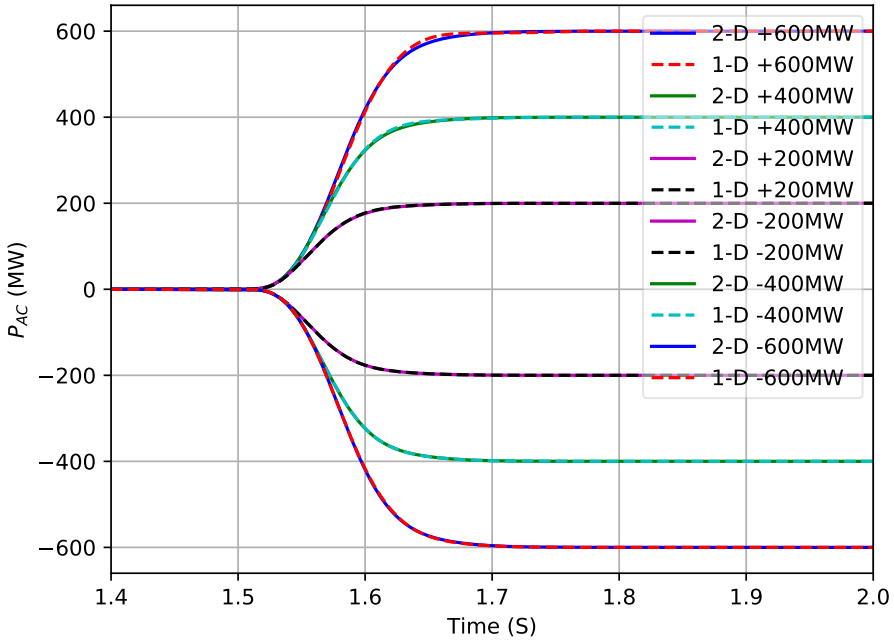

Figure 4.10: Comparison of the two controllers with a power increase of 200 MW occurring at 1.5 seconds

It can be seen that the response in power are equal for both controllers. This implies that the tuning parameters from CIGRE [6] can also be applied for the 2-D controller. The settling time of the power control is around 0.2 seconds, hence the voltage loop has a faster response than the power loop. The P_{ac} control has no overshoot and the increase of power is smooth for all steps. As a small conclusion it can be validated that an equal response when operating in V_{dc} or P_{ac} control.

4.3.2 Evaluation of Tuning Parameters for the d-axis Control Loop

It was discovered in the subsection 4.3.1, that the tuning parameters of the 1-D control can be used in the 2-D control when operating in constant V_{dc} and constant P_{ac} control. The new challenge is to determine how to tune the PI controller in the d-axis loop to obtain tuning parameters that can work for both the V_{dc} and the P_{ac} loop. This is especially important for the droop control where P_{ac} and V_{dc} will be dependent on each other. If it is difficult to find tuning parameters that works perfect for both loops, a compromise has to be made.

As stated in [6], P_{ac} loop has a K_p=0, while in V_{dc} control K_p=8. It should be noted that these tuning parameters are considered as extremes. This gives a range of $0<K_p<8$ for finding a proposed K_p that can work for both control modes. The same applies for the T_i, where P_{ac} control has a T_i=0.0303, and V_{dc} control has a T_i=0.00367. The range of the T_i then becomes $0.00367<T_i<0.0303$.

To investigate if it is possible to have a combination of the "extremes", meaning the highest/lowest values in the range of K_p and T_i, the scenarios listed in Table 4.3 were tested.

Table 4.3: Scenarios for different combination of tuning parameters

Scenario	K_p	T_i
1	8	0.00367
2	8	0.0303
3	0	0.00367
4	0	0.0303

The scenarios were first tested in V_{dc} control where a step of 5 kV was applied at 1.5 seconds. The results of the step can be seen in Figure 4.11. It was made sure that all scenarios were in steady state before the step was applied.

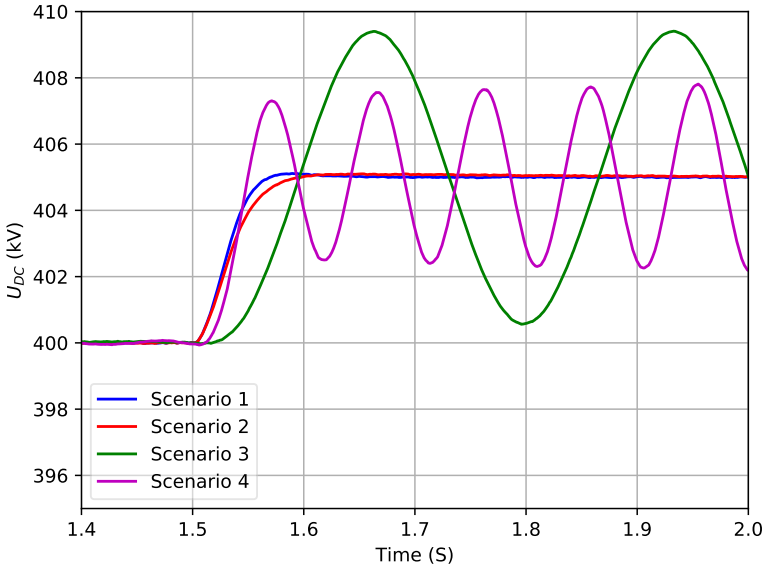

Figure 4.11: Step response comparison of DC voltage control

Scenario 1 has the best performance when operating in V_{dc} control, having a slightly shorter settling time. The responses of Scenario 3 and Scenario 4 are unstable with high oscillations around the reference value. The simulation shows that using tuning parameters designed for P_{ac} control when operating in V_{dc} control results in an unstable response. It is changing the value of K_p in the V_{dc} loop that affects the response most, while keeping K_p=8 and changing T_i results in a stable response but with a difference in the settling time. Another interesting discovery is that when using a high K_p the system will not be sensitive to a change in T_i. On the other hand, using a small value for K_p makes the system more sensitive to a change in T_i.

The tuning parameters in Table 4.3 were used in the power control simulations. Figure 4.12 illustrates the response of the constant power control having a step from 100 MW to 400 MW.

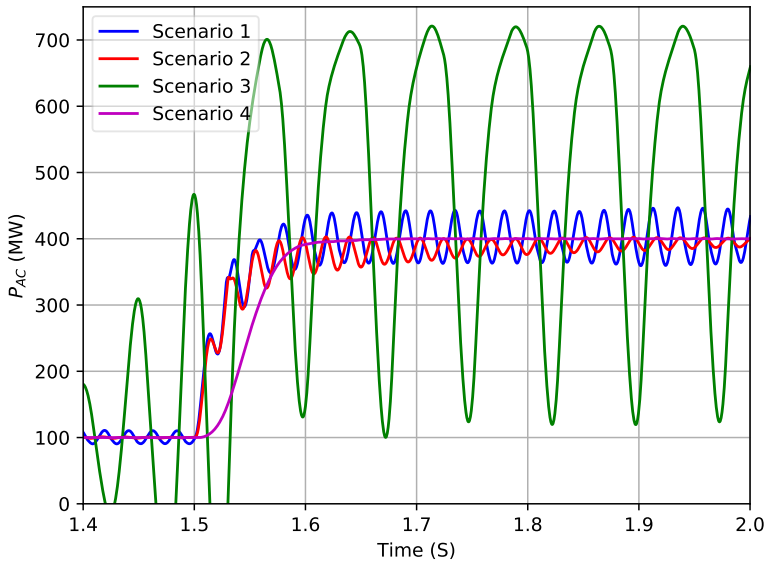

Figure 4.12: Step response comparison of active power control using the two P-control tuning parameters

It can be seen that Scenario 4, which use the P_{ac} tuning parameters has the best response. For Scenario 1 and Scenario 2, the response has the same behaviour as Scenario 4, but both signals are oscillating. In Scenario 1 the oscillations are in steady state, while they are decreasing in Scenario 2. For Scenario 3, the signal has high oscillations around the reference value compared to the other scenarios which means that using the K_p proposed by AKKARI for the P_{ac} loop gives an unstable response. Evaluating scenario 1, 2 and 3 it does not look like the P_{ac} loop is that sensitive to a change in K_p. On the other hand, a change in T_i has a big effect on the response. An example of this can be obtained by analyzing Scenario 3 and Scenario 4. In these two scenarios the value of K_p is equal, but the T_i is changed. For Scenario 3 this gives high oscillations around the reference value while in Scenario 4 the signal is completely smooth. This implies that for the P_{ac} controller it is more critical to have a high change in T_i than in K_p.

4.3.3 Trial and Error Procedure to Find Proposed Tuning Parameters For The PI Controller In The d-axis Control Loop

Since the d-axis control loop in the 2-D controller only contains one PI controller which has to work for P_{ac}, V_{dc} and DC voltage droop control it is wanted to find proposed tuning parameters that works for all three control modes. The trial and error was performed by first evaluating K_p in the V_{dc} loop then for the the P_{ac} loop. The sequence of how the tuning

was performed can be seen in Figure A.3. The sequence of how the K_p and T_i are tested is important because even though they are to individual parameters, they still have an effect on each other. The range for testing is $0<K_p<8$ and $0.00367<T_i<0.0303$. As previously described, it is wanted to tune the controller to have a low overshoot while at the same time having a fast response.

Changing the Value of Kp while Keeping Ti Constant

Figure 4.13 depicts the response in V_{dc} when conducting a step of 5 kV. In each simulation the value of K_p is changed while the T_i value is kept constant. The tuning parameters used and a more detailed overview of the results are shown in Table 4.4 displayed as 5 different scenarios.

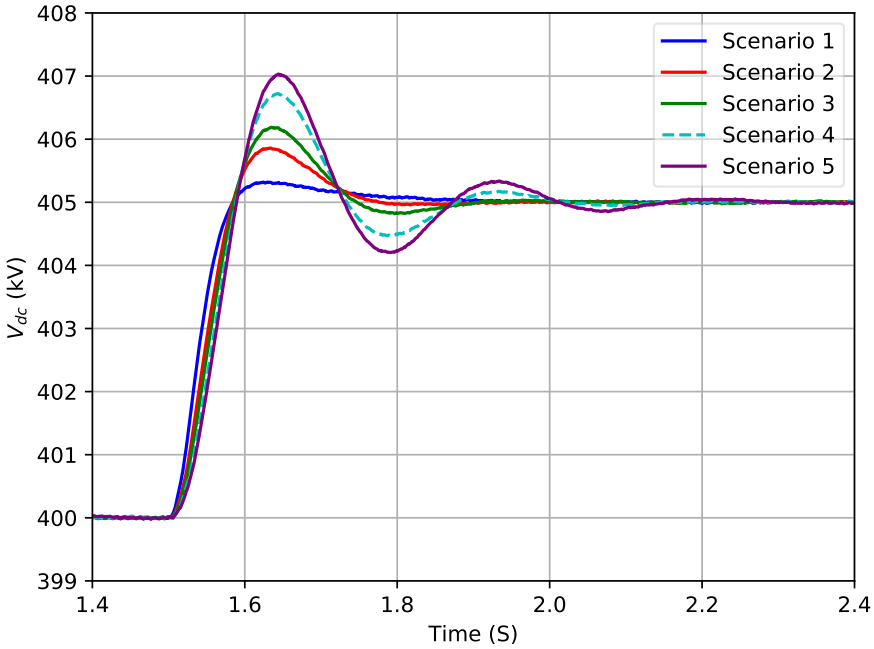

Figure 4.13: How the K_p parameter affect V_{dc} control with a T_i of 0.0303

Table 4.4: How the K_p parameter affect V_{dc} control with a T_i of 0.0303

Scenario	Over-shoot	T_s	K_p	T_i	T_r	T_p
1	6.48%	0.6	4	0.0303	0.04	0.1244
2	17.2%	0.5	2	0.0303	0.04	0.1344
3	24%	0.46	1.5	0.0303	0.04	0.1444
4	34.5%	0.44	1	0.0303	0.04	0.1444
5	40.6%	0.434	0.8	0.0303	0.04	0.1444

Table 4.4 shows that the lower the K_p value, the higher the overshoot is which also results in a longer settling time. The table values show that the T_r and T_p are almost equal for the different values of K_p and it is the overshoot and the settling time that are the most important factors. It is wanted to have a low overshoot while at the same time having as fast response as possible. This implies that for the V_{dc} control a high K_p within the range is the best choice. But, since the tuning parameters also has to fit the P_{ac} control, the parameters has to be simulated for the power as well.

To check the response in power when changing K_p and keeping T_i constant at 0.0303 a step of 200 MW was applied to the system. Figure 4.14 depicts the response in power for 5 different scenarios. The settings for each scenario and a list of the most important factors observed from the simulation result is shown in Table 4.5.

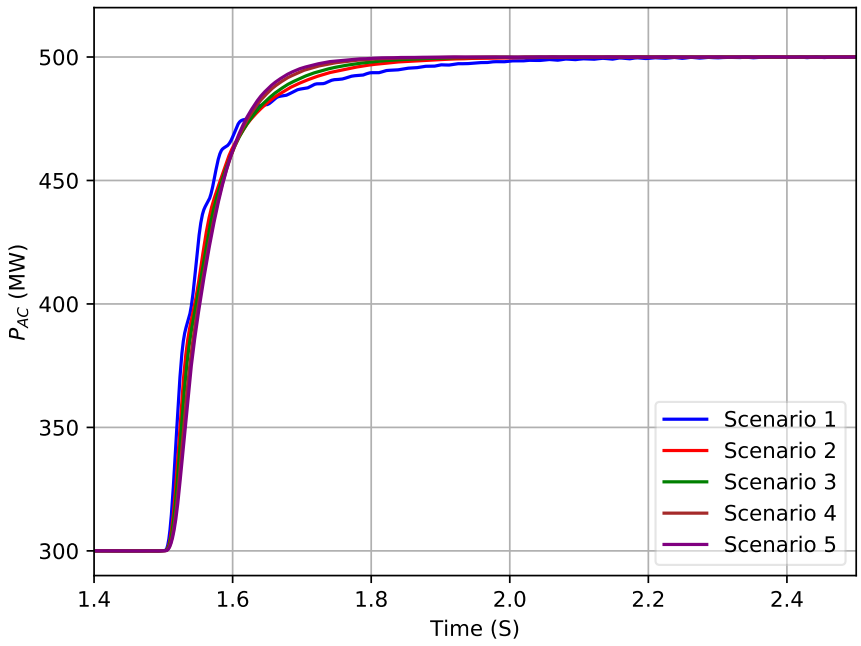

Figure 4.14: How the common PI parameters affect the P control with a Ti of 0.0303

Table 4.5: How various K_p values affect P_{ac} control with T_i constant at 0.0303

Scenario	Over-shoot	T_s	K_p	T_i	T_r	T_p
1	-	0.7	4	0.0303	0.116	0.7
2	-	0.7	2	0.0303	0.126	0.7
3	-	0.6	1.5	0.0303	0.12	0.6
4	-	0.6	1	0.0303	0.111	0.6
5	-	0.45	0.8	0.0303	0.106	0.45

It can be seen from the figure that scenario 1, which has the highest K_p value contains the most oscillating waveform. When observing the table values for scenario 1 to 4, T_s is decreasing with a lower K_p value, even though the difference is not big. There is also not much difference in the values of T_r and T_p. For scenario 5 which has the lowest K_p value T_s is the shortest. A lower value of K_p leads to a more smoother and faster response, hence a low K_p is desired when operating in P_{ac} control.

Since the V_{dc} control requires a higher value of K_p and the P_{ac} wants a lower value, a compromise has to be made. This is why 1.5 is chosen as a value for K_p since the waveform in P_{ac} control is still smooth and at the same time V_{dc} control will have a not have that high of an overshoot in the system.

Keeping Kp Constant while Changing the Value of Ti

The following simulations focus on the effect of changing the value of T_i parameter while maintaining a $K_p = 1.5$. For the P_{ac} control it is wanted to have a T_i at around 0.0303. But since the T_i in the V_{dc} control is 0.00367, it is wanted to test how the P_{ac} control works for lower values of T_i. Figure 4.15 depicts the response in power when conducting a 500 MW step while changing the values of T_i. Table 4.6 lists 6 scenarios and the parameters used for simulations as well as important factors extracted from the results.

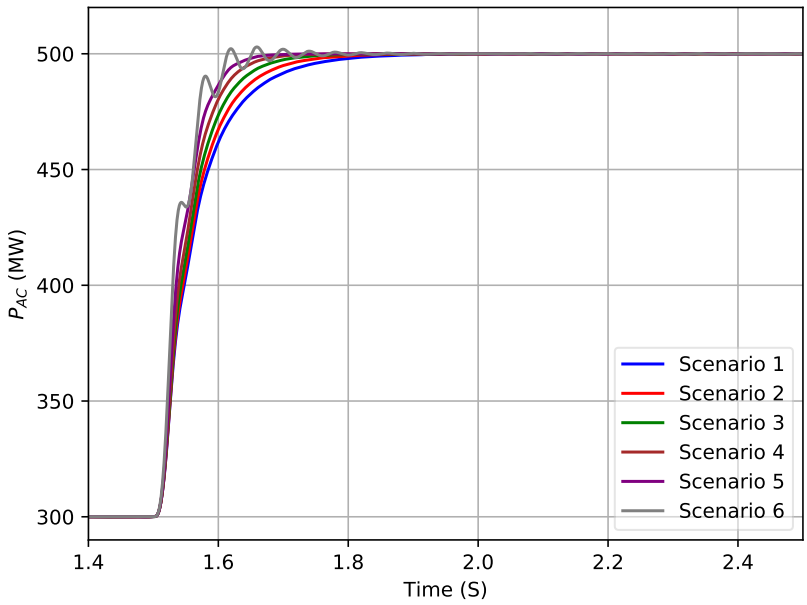

Figure 4.15: How the T_i parameter affect the P_{ac} control with a K_p equal to 1.5

Table 4.6: How the T_i parameter affect the P_{ac} control with a K_p equal to 1.5

Scenario	Overshoot	T_s	K_p	T_i	T_r	T_p
1	-	0.6	1.5	0.0303	0.12	0.6
2	-	0.65	1.5	0.025	0.106	0.55
3	-	0.45	1.5	0.02	0.092	0.45
4	-	0.35	1.5	0.015	0.079	0.35
5	-	0.275	1.5	0.01	0.068	0.275
6	2.5%	0.5	1.5	0.005	0.054	0.159

The figure shows that a low T_i as in scenario 6 makes the signal oscillate which should be avoided. Another observation is that a lower value of T_i will reduce the T_s, T_r and T_p values. This implies that a lower value of T_i will give a faster response, but it can create oscillations in the signal. It is therefore necessary to test the same T_i parameters in the V_{dc} control.

To check the response when conducting a 5 kV step in the V_{dc} control the parameters presented in Table 4.7 are used. The response of the voltage step is depicted in Figure 4.16 where Table 4.7 present detailed values obtained from the simulation.

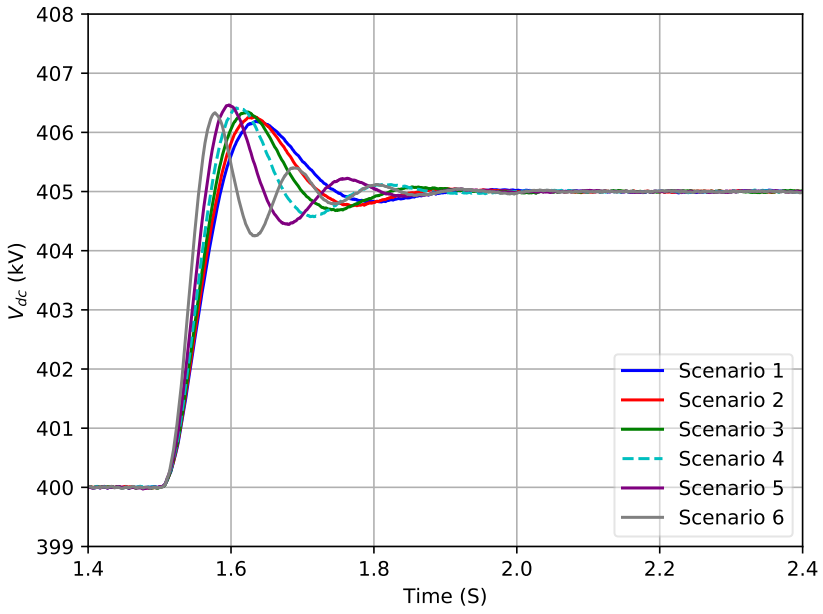

Figure 4.16: How T_i affects V_{dc} control with a K_p equal to 1.5

Table 4.7: How T_i affects V_{dc} control with a K_p equal to 1.5

Scenario	Overshoot	T_s	K_p	T_i	T_r	T_p
1	24%	0.464	1.5	0.0303	0.04	0.1344
2	25,3%	0.402	1.5	0.025	0.038	0.1336
3	26.9%	0.358	1.5	0.02	0.035	0.1236
4	28.4%	0.314	1.5	0.015	0.0317	0.1136
5	29.27%	0.262	1.5	0.01	0.0275	0.098
6	26.64%	0.304	1.5	0.005	0.0224	0.0778

With the same parameters conducted for P_{ac} control in V_{dc} control it can be observed that the scenarios with a high T_i will cause the lowest overshoot and be more damped compared to the scenarios with a low T_i. Even though scenario 1 has the highest T_s, T_r and T_p, it has the lowest overshoot, which is considered to be the most critical factor. The difference in T_s when reducing T_i is not that big, meaning that a reduction in T_i does not affect the T_s by much. A lower T_i in P_{ac} control will also lead to more oscillations in in the, hence T_i with the lowest overshoot and lowest content of oscillations have the biggest effect on the choice of the best fit for T_i. A T_i=0.0303 is therefore chosen.

To summarize the discoveries from the simulations, K_p= 1.5 and T_i= 0.0303 will be chosen as settings for the PI controller in the d-axis control loop.

4.3.4 Validation of the Proposed Tuning Parameters

To validate the PI-tuning parameters obtained from subsection 4.3.3, the 2-D controller using the proposed tuning gains were compared with the 1-D controller using the tuning parameters from [6]. Table 4.8 shows the combination of tuning parameters tested for the V_{dc} and P_{ac} loop.

Table 4.8: Tuning parameters used for simulations

Type of Control	Converter-control	K_p	T_i
P_{ac} control	Scenario 1	0	0.0303
	Scenario 2	1.5	0.0303
V_{dc} Control	Scenario 1	8	0.00367
	Scenario 2	1.5	0.0303

Figure 4.17 shows the response in voltage when applying a 5 kV step in the voltage at 1.5 seconds in V_{dc} control.

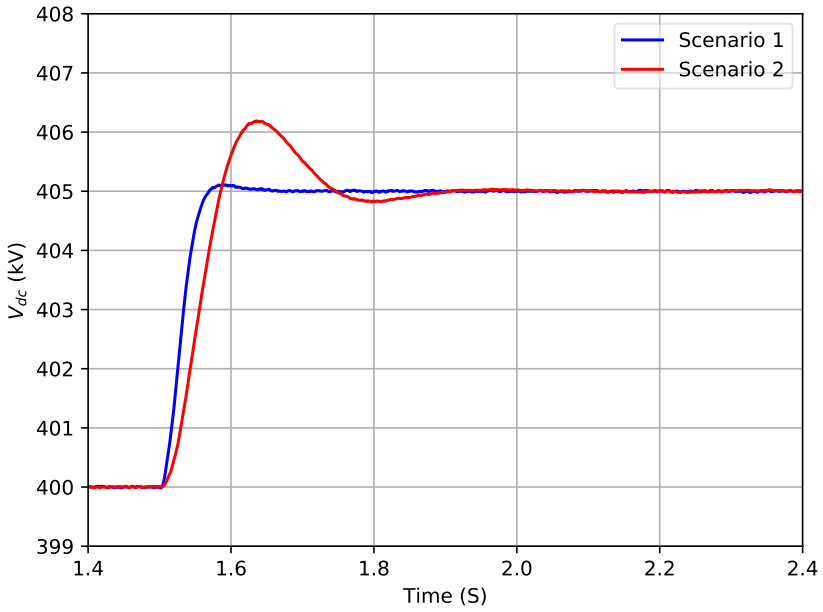

Figure 4.17: Comparison of the proposed tuning parameters and the 1-D control tuning parameters in V_{dc} control

The results show that in V_{dc} control, scenario 2 has a higher overshoot and a longer settling time than scenario 1. This means that the response will be slower for the 2-D controller when using proposed tuning gains in the V_{dc} control. This is because the K_p have been reduced from 8 to 1.5 for the voltage loop, which means that the response will be less aggressive. When comparing with scenario 1, it can be seen that scenario 1 will have a faster response and almost no overshoot.

Figure 4.18 shows the response in power when conducting a step of 500 MW when operating in P_{ac} control.

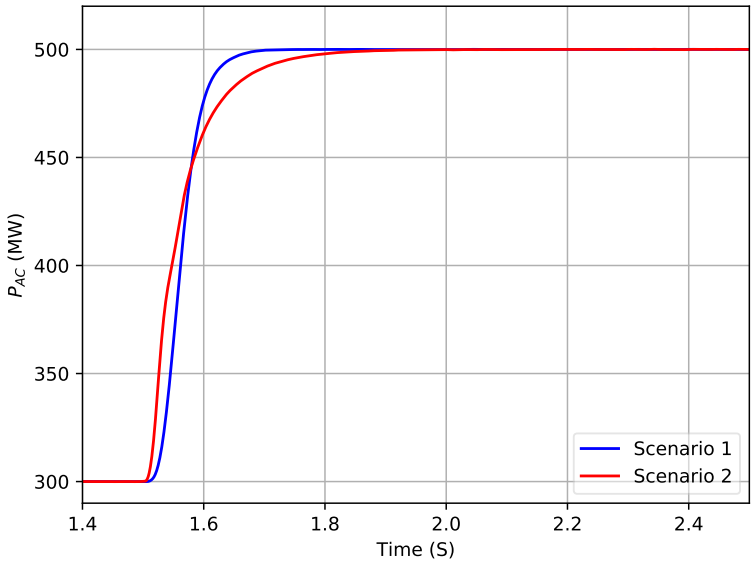

Figure 4.18: Comparison of the proposed tuning parameters and the 1-D control tuning parameters in P_{ac} control

The response of the power shows that scenario 1 has a faster response than scenario 2. None of the responses has an overshoot so it will only be the settling time that is the most important factor.

To summarize, using the 1-D gains gives a faster response when operating in V_{dc} and P_{ac} control than using the proposed gains. The advantage with using the proposed tuning parameters is that there is no need to change the gains when switching the control mode. As mentioned, this advantage will have a drawback with the response becoming slower.

4.3.5 Evaluation of the Response when Operating in Droop Control

This section presents the results from applying the same droop constant in the 1-D and 2-D controller. Table 4.9 shows the settings used for simulations. The droop value is calculated by using equation Equation 3.16, where the value is based on trying to make the converter take as much power and voltage as possible. Another factor is that $\frac{1}{K_v}$=20 gives a droop slope of 45 degrees, which is in the middle of P_{ac} and V_{dc} control. Having a 45 degrees slope should mean that the converter should supply half of the power it is set to. It should also be noted that the proposed values for K_p and T_i are the ones used for scenario 2 obtained from subsection 4.3.4. The reason why scenario 3 uses the same tuning parameters as the 1-D controller is to check how the response is by using equal tuning parameters for the droop simulations. Since the error is not calculated in the same way when the controller operates in droop control for the 2-D controller and the 1-D controller, the response should not be equal.

Table 4.9: Settings of the 1-D and 2-D controller used for droop simulations

Scenario	Tuning parameters		1-D settings	2-D settings
	K_p	T_i	$\frac{1}{K_v}$ $[\frac{MW}{kV}]$	$\frac{x_2-x_1}{y_2-y_1}$
1	0	0.0303	20	$\frac{(380-420)}{800-(-800))}$
2	1.5	0.0303	20	$\frac{(380-420)}{800-(-800))}$
3	0	0.0303	20	$\frac{(380-420)}{800-(-800))}$

The power in the converter set to droop control set to do a step from 0 to 500 MW, and the V_{dc} reference value is 400 kV. The setup used for the simulation is Figure 4.8.

The response in the droop can be seen in Figure 4.19. The step is plotted as normalized values in order to see the behaviour of the droop step. In the scaling, 0.5 represents 0 MW and 0 kV, while 0.656 represents 406 kV and 253 MW.

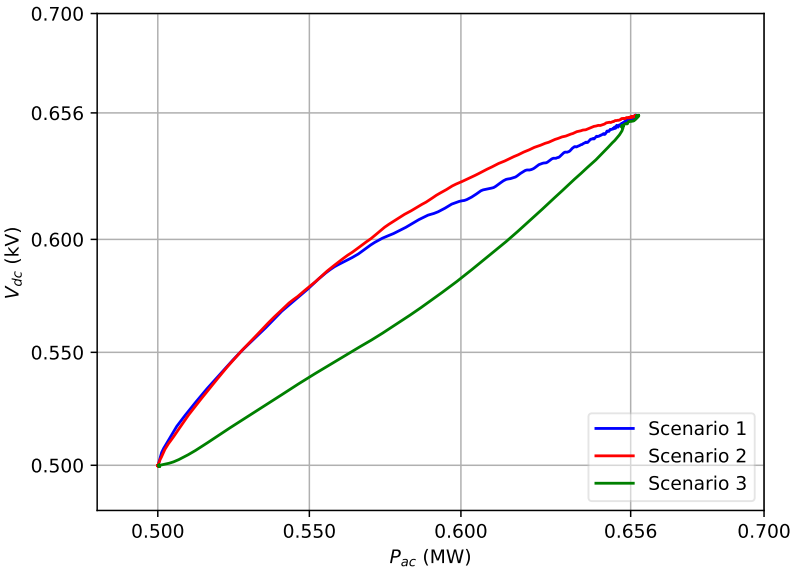

Figure 4.19: Comparison of the controllers and tuning gains when conducting a step in the droop slope of 500MW with $\frac{1}{K_v}$=20

The reason why the droop is directed from left to right is because it is only connected to a voltage source. This means that the step in power will be conducted in the converter which is set in droop control. The step of the droop slope will behave as explained in Figure A.2.

When comparing scenario 1 and scenario 3 which use the same value for K_p, it can be seen that the droop response is not the equal. This means that when operating in droop control, the response will not be the same for the 1-D and 2-D controller even though the tuning parameters are the equal. For scenario 1 and scenario 2, it can be seen that using different tuning parameters in the 2-D controller does not make the response differ much.

Even though the response of the droop is different all three scenarios have the same start and end points. It was also attempted to add a scenario 4 where the proposed tuning parameters were implemented for the 1-D controller. The result from this simulation is described in subsection A.6.1. The results from scenario 4 shows that the 1-D controller is more sensitive to a change in tuning parameters than the 2-D controller.

The response in voltage is shown in Figure 4.20 when applying a step in power of 500 MW. The most important factors of the simulation are listed in Table 4.10.

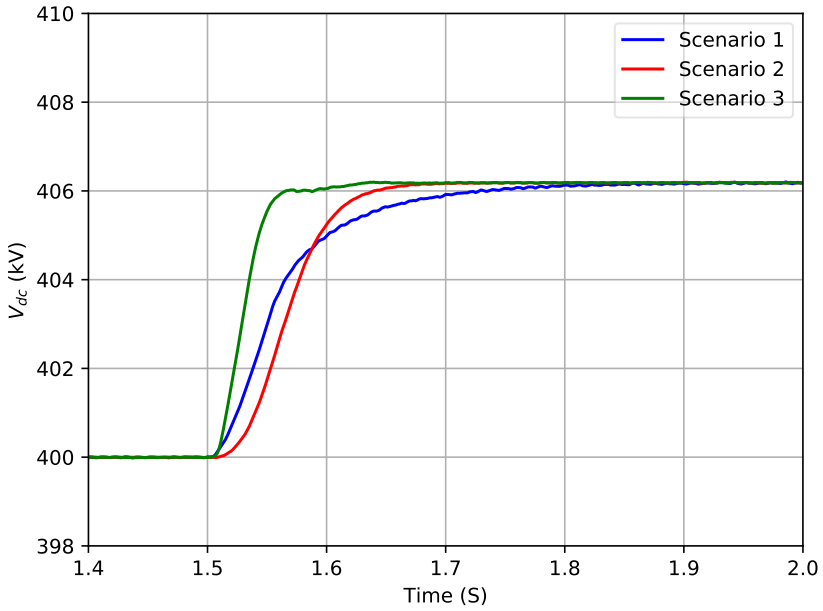

Figure 4.20: Voltage response when both controllers are in droop control mode

Table 4.10: Values extracted from the voltage response simulation

Scenario	K_p	T_i	T_s [s]	**Overshoot**
Scenario 1	0	0.0303	0.35	-
Scenario 2	1.5	0.0303	0.2	-
Scenario 3	0	0.0303	0.14	-

The results show that scenario 3 has a shorter settling time than the other two scenarios. Since scenario 2 and scenario 3 have the same tuning parameters, it means that the 2-D controller will be slower than the 1-D controller when using the same tuning parameters. The reason why the 1-D controller has a faster response than the 2-D controller is because the error is calculated differently in the two controllers. Due to that the error will be larger according to 4.2 will make the PI respond faster when given an larger error.

The response of the power response of the droop step is depicted in Figure 4.21 and the most important data are displayed in Table 4.11.

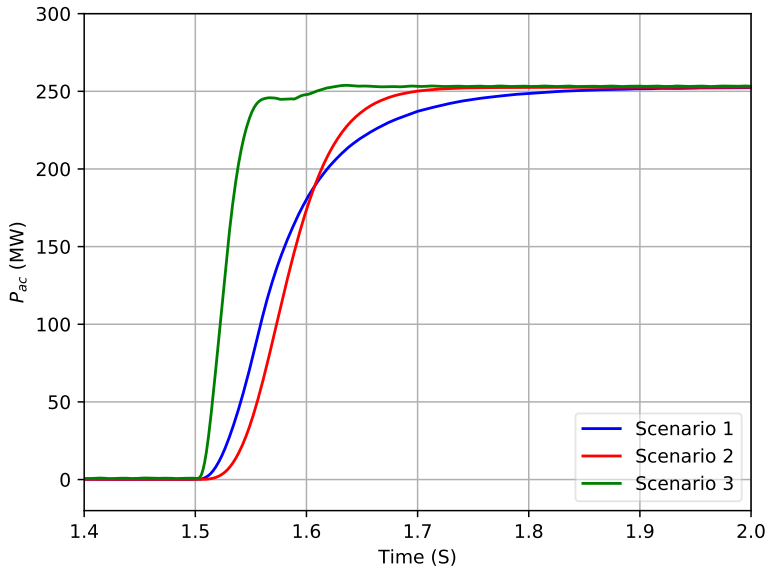

Figure 4.21: Power response when both controllers are in droop control mode

Table 4.11: Data obtained from the power step response

Scenario	K_p	T_i	T_s [s]	**Overshoot**
Scenario 1	0	0.0303	0.36	-
Scenario 2	1.5	0.0303	0.24	-
Scenario 3	0	0.0303	0.16	-

The power step was set to 500 MW, but as previously mentioned the droop constant is chosen so that the converter will supply half of the increase in power. All scenarios reach the same value of the power. Scenario 3 is has the shortest settling time followed by scenario 2. Scenario 1 which has the highest value of K_p has the slowest response.

To summarize the observations from the droop slope results it can be stated that the 1-D controller has a faster response than the 2-D controller when operating in droop control. This is not only due to the tuning parameters, but also because the error is calculated in a different way for the droop in the 2-D controller than in the 1-D controller. The 2-D controller is more robust to a change in the tuning parameters compared to the 1-D. When implementing the proposed tuning gains in the 1-D controller the signal started to oscillate. Even though the proposed tuning parameters have a slower response than the ones for the 1-D controller, they still work to give a stable response.

4.3.6 Validation of The Voltage and Power Limits for the 2-D Controller

The previous simulations have been conducted with steps in voltage and power that has been operating within the limits of the controller. The simulations in this subsection are conducted in order to validate that the converter will not operate outside the "box" containing the limits for power and voltage in the 2-D controller. This was also described in section 4.1. The data showing the limitations used in the following simulations are shown in Table 4.12.

Table 4.12: Settings used for simulating the limits of the 2-D controller

Control mode	**Upper limit**	**Lower limit**	K_p	T_i
V_{dc}	420	380	8	0.00367
P_{ac}	800	-800	0	0.0303

The following simulations are conducted in order to try to exceed the voltage and power limits of the 2-D controller when the algorithm will make sure for this does not happen. The setup used for the simulation are displayed in Figure 4.7. To try to exceed the voltage limits of the system an increase/decrease of ± 22 kV was applied when operating at a reference voltage of 400 kV. The data used for simulations are shown in Table 4.12. The response when conducting a ± 22 kV step in voltage is depicted in Figure 4.22

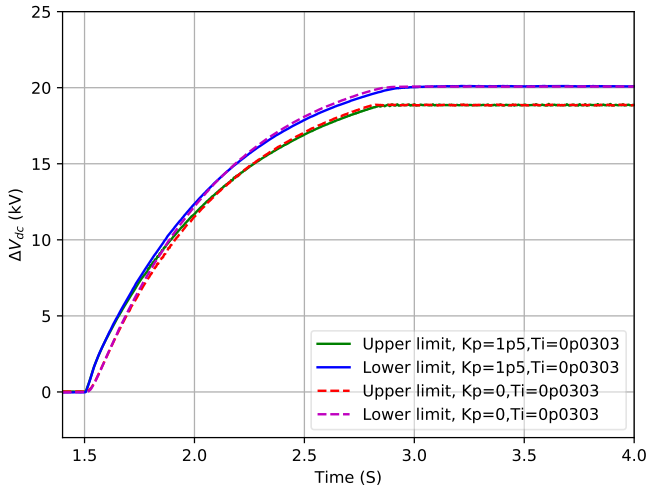

Figure 4.22: Effect of the limitation algorithm on the voltage when operating in V_{dc} control and conducting a ± 22 kV step V_{dc} control

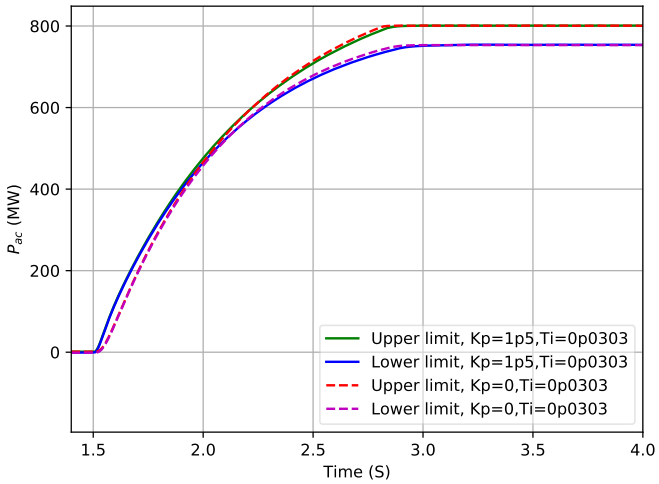

Figure 4.23: Effect of the limitation algorithm on the power when there is a ± 22 kV step operating in V_{dc} control

The response of applying a 22kV step in V_{dc} control shows that the lower limit is reached and the control will keep the voltage from moving outside of its lower limit. For the upper limit, the voltage level will be limited before it hits the upper limit. This is because the power response reach its upper limit before the voltage, hence the power will limit the voltage. It can also be seen that using the proposed tuning gains in the 2-D controller gives the same response as when using the 1-D ones.

Another simulation was conducted in order to validate if the 2-D controller algorithm worked to keep the limits of the box when operating in P_{ac} control. The tuning parameters used are the ones for P_{ac} control in Table 4.12. The setup used for the simulation is Figure 4.8. To exceed the upper limit, a step from 0 to ± 820 was applied to go beyond the upper and lower limit for the power. The responses of the power step are shown in Figure 4.24 and Figure 4.25

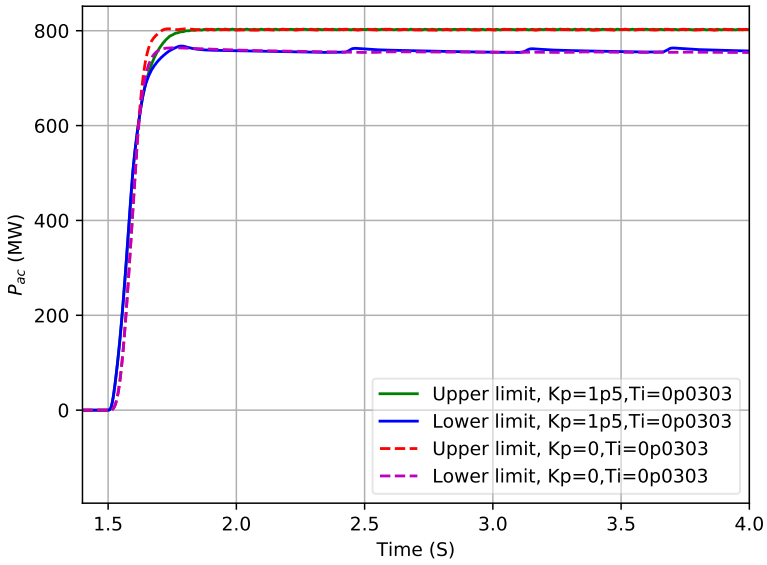

Figure 4.24: Effects of limitation algorithm on the power response when operating in P_{ac} control

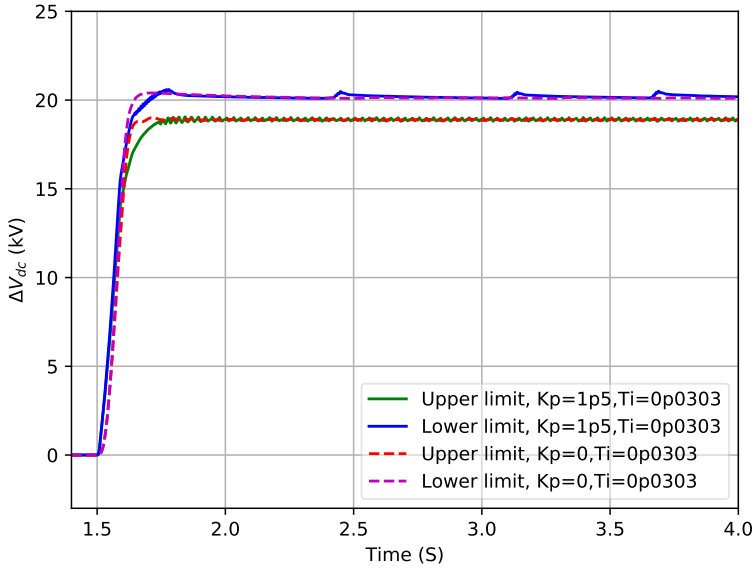

Figure 4.25: Effects of the limitation algorithm on the voltage response when operating in P_{ac} control

As seen for the power response when a step is implemented to move outside the upper

limit it is found that the upper limit will be kept at 800 MW trough-out the simulations.The lower limit of the P_{ac} control is limited at around 750MW.The lower limit will experience negligible oscillations during operation. It is believed that this occurs due to that P_{ac} control will always try to reach 800 MW but at the same time moves outside of the lower voltage limit which will go on throughout the simulation. Another factor that can be seen is that the response is almost equal regardless of the tuning gains implemented. This means that the proposed tuning parameters works to limit the power and voltage.

4.4 Validation of the q-axis Control Loop

In the previous section, section 4.3, the operation of the 2-D controller was validated in the d-axis. In this section it is wanted to validate the 2-D controller operation for the q-axis control loop. The 2-D controller will be compared with the 1-D controller for the same cases as the d-axis control loop.

4.4.1 Adapting The AC Grid To q-axis Simulations By Calculating Different Short Circuit Ratios

In order to test the Q_{ac} and V_{ac} loops the parameters of the AC systems has to be changed. This is because it is wanted to test the 2-D controller in an offshore converter station. Since an offshore converter station never will be connected to a strong AC grid, the parameters of the AC grid will be changed by using different short-circuit ratios (SCR) for the simulations. The SCR is also changed in order to investigate how the strength of the AC grid affects the q-axis control loop in the 2-D controller. The short circuit ratio is the ratio between the AC and the DC grid and it is an important parameter for measuring the strength of the AC system. The characteristics of the AC network connected to the HVDC grid is important for how the HVDC system will operate. AC systems that create problems with operation are usually named weak. But a weak AC system can be divided in two different aspects[11]:

- Systems with high impedance, leads to power transfer limitation and voltage stability problems
- Systems with low inertia, where a deviation of frequency cause concerns

It is the systems with high impedance that gives the most problems for the stability of HVDC systems. The strength of the AC network compared to the HVDC network is an important factor for HVDC operational challenges [11]. To make the test system suitable for q-axis simulations 3 different SCRs were calculated. The calculations are shown in subsection B.3.1. According to [11] the classification of the SCR is as depicted in Table 4.13.

Table 4.13: Classification of SCR [11]

SCR	Classification	Operating difficulties
SCR > 3	Strong system	No operating problems
$2 <$ SCR < 3	Weak AC system	Operating difficulties can be expected. Some special controls are required
SCR $= V_{ac}$	Very weak AC system	Serious operating difficulties can be expected. Very few HVDC systems operate with this low SCR

4.4.2 Changing The Control Structure of the 1-D Controller q-axis Loop To Be Comparable With The 2-D Controller q-axis Loop

Another thing that has to be changed before being able to simulate the q-axis loop is the control structure of the 1-D controller. As was shown in Figure 3.3) the DCS1 CIGRE model has a cascaded structure for the q-axis control loop. Since the 2-D controller does not contain any cascaded PI controllers, the configuration of the q-axis loop will be changed to be comparable to the 2-D system. The change in configuration from the cascaded q-axis loop to the non-cascaded is illustrated in Figure 4.26. The upper figure (a) depicts the cascaded AC loops and how the system is rearranged into figure (b) as a non-cascaded system.

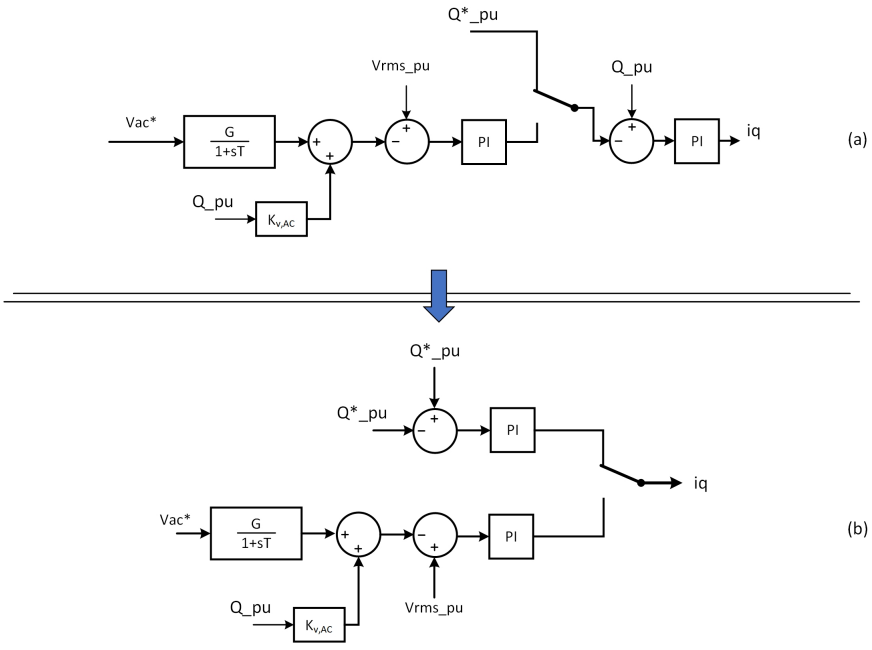

Figure 4.26: The upper figure (a) shows the configuration of the cascaded q-axis loop, while the lower figure (b) shows the non-cascaded q-axis loop (b)[6]

As seen in Figure 4.26 (a) it is equal to the q-axis loop displayed in Figure 3.3. By changing the configuration from a cascaded system to a non-cascaded one, the values of the

tuning parameters K_p and T_i for the d-axis control loop will change as well. The new tuning parameters are obtained from [6] and are shown in Table 4.14

Table 4.14: Tuning parameter for a non-cascaded system obtained from [6]

Control mode	K_p	T_i
Q_{ac}	0	0.0303
V_{ac}	0	0.0333

It would also be a possibility to change the configuration of the 2-D controller to a cascaded one, but as explained further in subsection A.6.2 this will eliminate the advantage with having only one PI-controller in the q-axis control loop.

4.4.3 Response Comparison of the Controllers in the q-axis Loop

To validate the operation of the q-axis control loop, the response of the 1-D and 2-D controller are compared for Q_{ac} and V_{ac} control when conducting a step. As for the d-axis control loop, if the response of the controllers are equal it means that the tuning parameters obtained from [6] can be applied for the q-axis in the 2-D controller. The tuning parameters used for simulating Q_{ac} and V_{ac} control are listed in Table 4.14.

Constant Reactive Power Control

As previously explained in subsection 4.4.1 the AC grid will be adjusted to have different SCR when simulating the q-axis loop. This is to investigate how using different SCR values for the AC grid affects the response in the system. The parameters used to simulate Q_{ac} control are displayed in Table 4.15. The SCR values are chosen in order to have different strengths of the AC grid. The procedure for calculating the different SCR can be found in section B.3.

Table 4.15: SCR parameters for the AC loop

Grid strength (SCR)	R_1 [Ω]	R_2 [Ω]	**L** [**H**]
38.11	0.48	1000	0.015
4	4.49	9528.86	0.1429
2.5	7.18	15244	0.2285

Figure 4.27 illustrates the response when having a step of -50 MVAr in reactive power performed at 1.5 seconds.

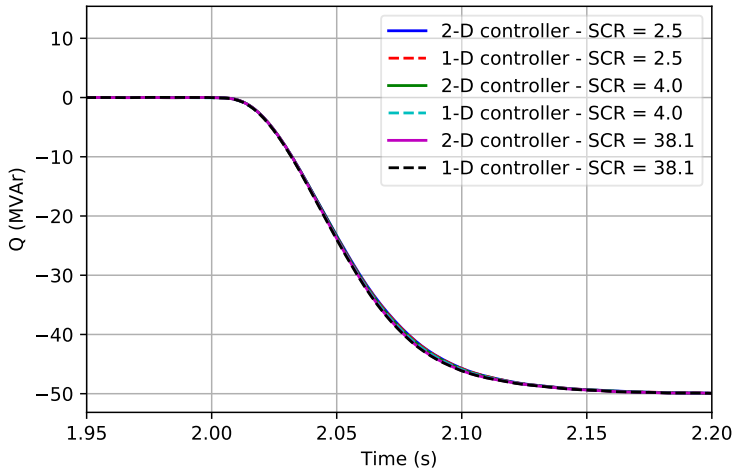

Figure 4.27: Reactive power behaviour of 2-D and 1-D controller in a weak grid

The results from the simulations show that the response of the reactive power is equal in the 2-D and 1-D controller. This means that the same tuning parameters as used for the Q_{ac} loop in the 1-D controller (the ones obtained from [6]) can be applied for the PI-controller in the 2-D controller. Another observation is that the reactive power response is not affected by the SCR value in the AC grid.

Since the Q_{ac} loop is not affected by having different values of SCR it is interesting to investigate the response of V_{ac} for the same simulation. Figure 4.28 displays the response in V_{ac} to a 50 MVAr change in power when the controller is set as Q_{ac} control.

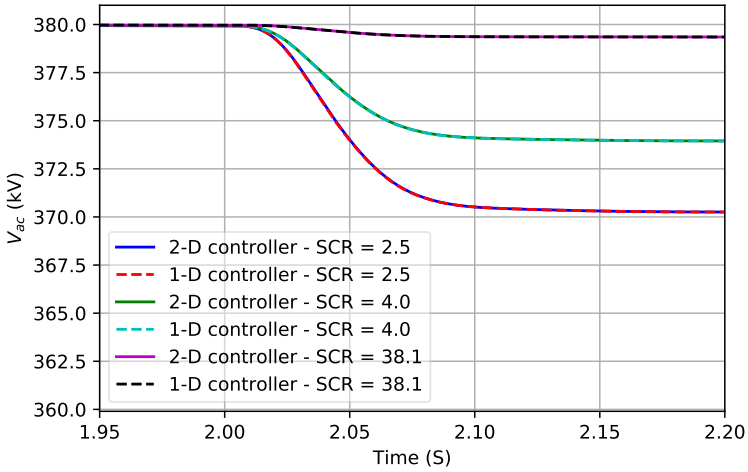

Figure 4.28: AC voltage behaviour of a step in reactive power

The 1-D and 2-D controllers have an equal behaviour in the V_{ac} response as well. It can be seen that the response in V_{ac} is varies according to the value of the SCR. For a high SCR, the grid is strong and the voltage will not drop with a big value when conducting a step in Q_{ac}. On the other hand, for a low SCR the drop in V_{ac} becomes larger. This is because a change in Q_{ac} will have a higher impact on the response of V_{ac} in a AC grid with low SCR. This implies that the lower the SCR, the less change in Q_{ac} is needed to have a change in the response of V_{ac}. Another thing to observe is that the 2-D controller has a good operation also when connected to AC grids with different SCR.

Constant AC Voltage Control

It is wanted to evaluate the response of the 2-D controller when conducting a step of 1.9 kV in the AC voltage applied at t=2s to check if the 1-D and 2-D response are equal. The V_{ac} loops was tested for AC grids with three different SCR all displayed in Table 4.15 and the tuning parameters used for simulation are shown in Table 4.14. If the response in the 2-D and the 1-D controller are equal, it means that tuning parameters obtained from [6] can be applied for the V_{ac} loop as well. The response of a step in the AC voltage is shown on Figure 4.29.

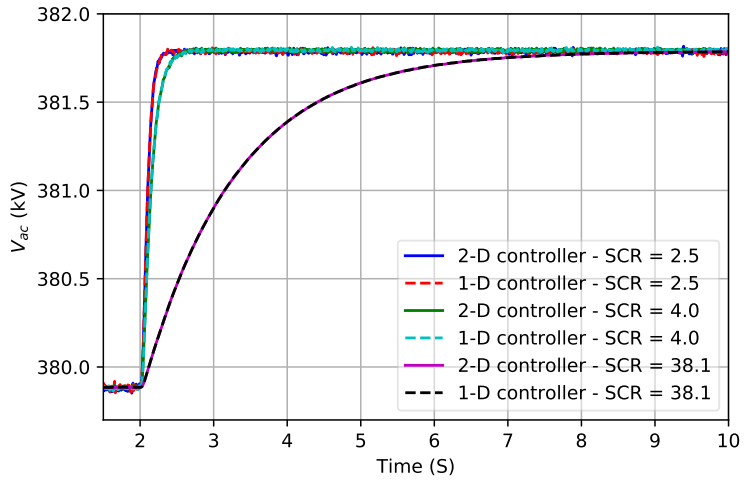

Figure 4.29: AC voltage response of the 2-D and 1-D controller for three different SCR

It can be seen that when making a step in voltage, the response of the 1-D and 2-D controller are equal. However, oscillations can be seen in the signal of the 1-D controller when it has a SCR of 2.5 and 4.0. This means that for a grid with a low SCR, the 2-D controller will have the same response as the 1-D controller but the signal of the 1-D controller will contain oscillations. Another factor is that a higher SCR will lead to a longer settling time of the response. This is because it takes more time to do a change in V_{ac} in a grid with a high SCR since it will require more reactive power to acquire the change. It can be seen that for lower SCR the response time is shorter.

4.4.4 Trial and Error Using Different Ti to Optimize the Response for a AC Droop Control

Since the response of V_{ac} and Q_{ac} are equal in both the 1-D and 2-D controller, it is wanted to test droop control in the q-axis loop. Since the q-axis loop only will have one PI-controller it is needed to find proposed tuning parameters that will work for both V_{ac} and Q_{ac} control. To find the proposed gains a trial and error method was conducted.

Since the original tuning parameters obtained from [6] and shown in Table 4.2 have the same value for K_p, only a new value for T_i has to be obtained. The range of T_i is small, varying between the two "extreme" values from $0.0303 < T_i < 0.0333$. A smaller range implies an easier search for a proposed T_i parameter. The scenarios used for testing the different T_i parameters are listed in Table 4.16. When operating in V_{ac} control a step op 1.9 kV was applied. The trial and error was conducted for a SCR of 2.5. This was because, as found in subsubsection 4.4.3, the Q_{ac}, and V_{ac} loops are more sensitive to a change when connected to a AC grid with low SCR. If the proposed tuning parameters works for a grid with low SCR, they should also operate good for a grid with high SCR. The T_i was first tested for the V_{ac} loop, then for the Q_{ac} control. The procedure for testing is also displayed in the flowchart shown in section A.4. The voltage response when tuning the T_i in the V_{ac} loop is depicted in Figure 4.30. The Q_{ac} is shown in Figure A.8.

Table 4.16: Test scenario for both V_{ac} and Q_{ac} control

Scenario	K_p	T_i
1	0	0.0303
2	0	0.0313
3	0	0.0323
4	0	0.0333

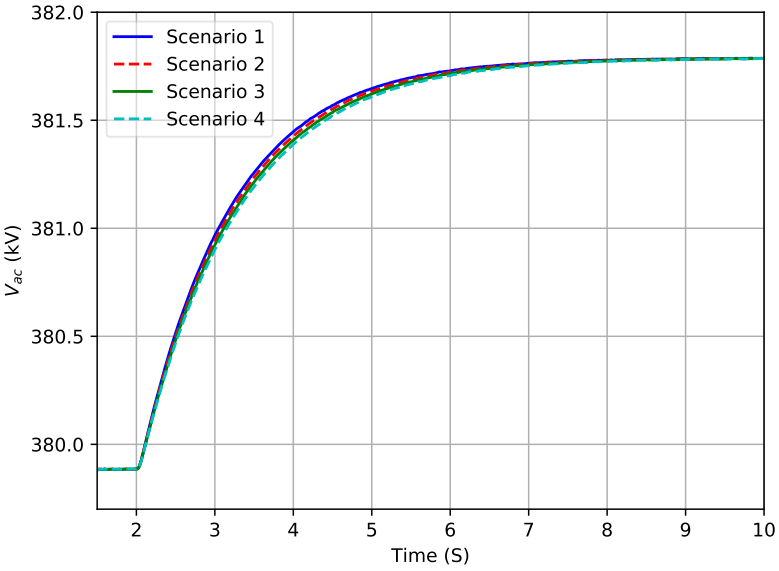

Figure 4.30: Keeping K_p constant while changing T_i in the V_{ac} loop

The observations from testing different T_i for constant V_{ac} control show that the response of the different T_i are similar. The two extremes, scenario 1 and 4 will not have a big impact on the response of the signal. However what can be found is that scenario 4 will be the best choice for V_{ac} control. This is because it has the shortest settling time. This still has to be evaluated for the Q_{ac} control as well since it is wanted to obtain tuning parameters that works for both loops.

The data used for simulating the Q_{ac} loops is presented in Table 4.16 and the reactive power response can be seen in Figure 4.31. The AC voltage response of the tuning is depicted in Figure A.9.

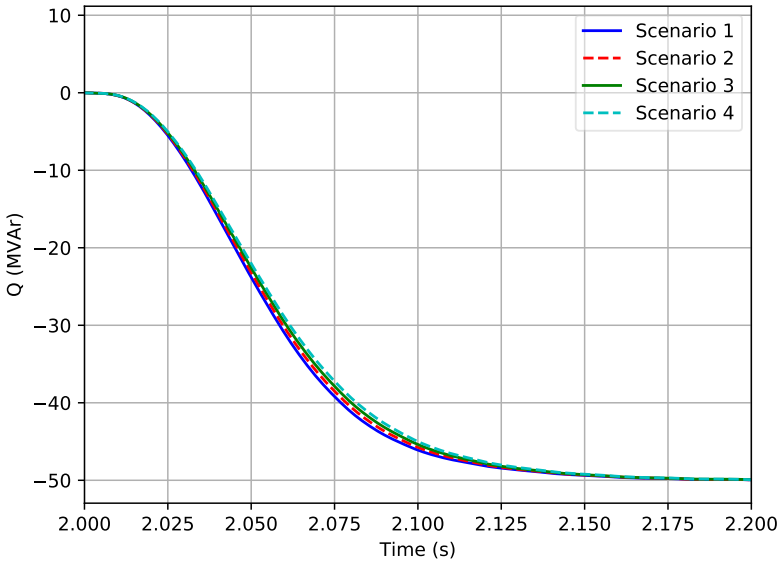

Figure 4.31: Q_{ac} control T_i sweep Q_{ac} response

It can be seen that the effects on changing T_i in the Q_{ac} is not creating a big difference in the response. The two extreme parameters will not have major effects to the system. However, the opposite effects of what was found for the V_{ac} control occurs for Q_{ac} control. In Q_{ac} control, scenario 1 is the best fit for the system with having the shortest settling time.

The results from the trial and error testing shows that Scenario 4 is the best in V_{ac} control, while scenario 1 is the best option for Q_{ac} control. Since the tuning parameters have to work for both loops, a compromise is made with choosing the proposed $T_i = 0.0323$. This means that the proposed tuning parameters for the q-axis loop is K_p=0, and T_i=0.0323.

4.4.5 Droop Control Comparison of the 1-D and 2-D Controllers for the q-axis Control Loop

In order to validate the AC droop control a comparison of the response for the 1-D and 2-D controller is presented. It is wanted to analyze the response of the controllers when operating in droop control using different tuning parameters. Since the error is calculated in a different way for the 1-D and 2-D controller it is not expected that the response will be equal, even though the same tuning parameters are applied in the controllers. As seen in subsection 4.1.2, the error should be greater for the 2-D controller when operating in the q-axis control. This implies that the response of the 2-D controller will cause the PI controller to have faster response than the 1-D controller. The tuning parameters and the droop constant used for the AC droop simulations are listed in Table 4.17 where the droop constants are calculated by using Equation 3.17. The SCR of the AC grid during simulations is 2.5 and the step applied in V_{ac} is 19 kV.

Table 4.17: Parameters used for testing droop control in the q-axis control loop

Control	K_p	T_i	K_v
1-D	0	0.0333	0.0475
2-D	0	0.0333	$\frac{399-361}{400-(-400)}$
2-D	0	0.0323	$\frac{399-361}{400-(-400)}$

The reason why the 2-D controller is tested for the same gains as the 1-D, and also the proposed tuning parameters is to evaluate which controller of the 1-D and 2-D that has the fastest response. The droop results from the AC droop control simulation is shown in Figure 4.32.

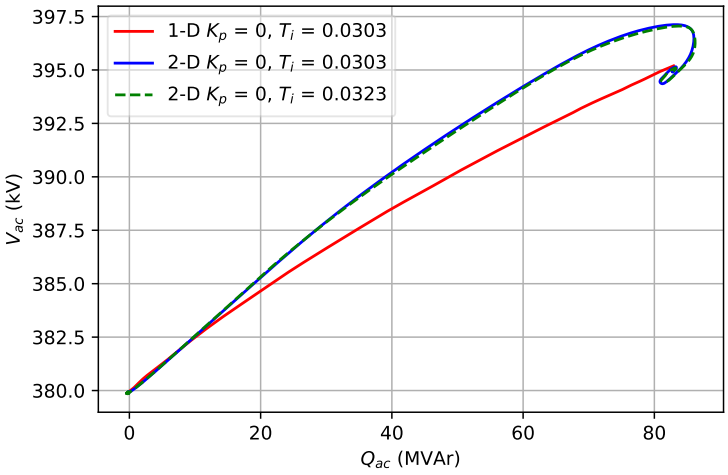

Figure 4.32: Illustration of a step in the droop slope by applying a step of plus 19 kV in V_{ac} at t=1.5

It can be seen that the response is different for the 1-D and 2-D controller. As for the droop control in the d-axis, the results above illustrates a step in the droop slope, and not the real droop slope. The step in the 1-D droop slope has a more stable response than the 2-D. The "loop" that can be seen for the droop in the 2-D controller right before it settles at the same reference as the 1-D is due to the overshoot in the response.

To analyze the response of the droop step, Figure 4.33 shows the Q_{ac} response and Figure 4.34 displays the response in V_{ac}.

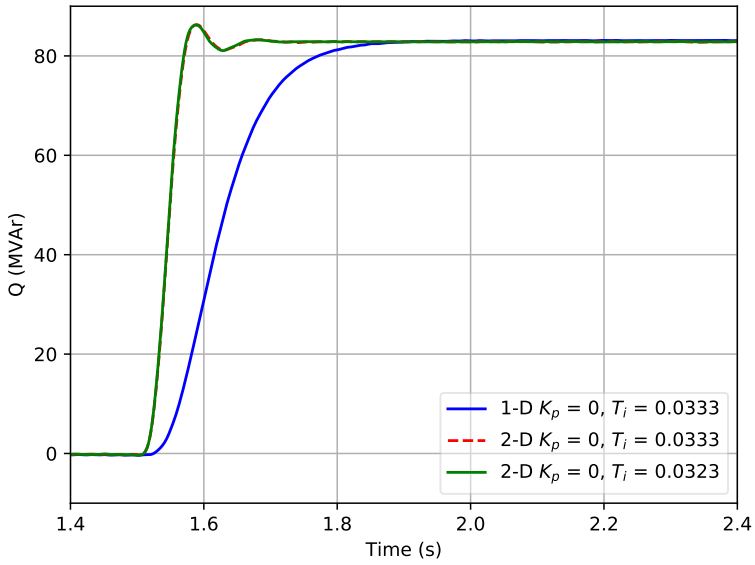

Figure 4.33: Response in the Q_{ac} when applying a 19 kV in V_{ac} at t=1.5

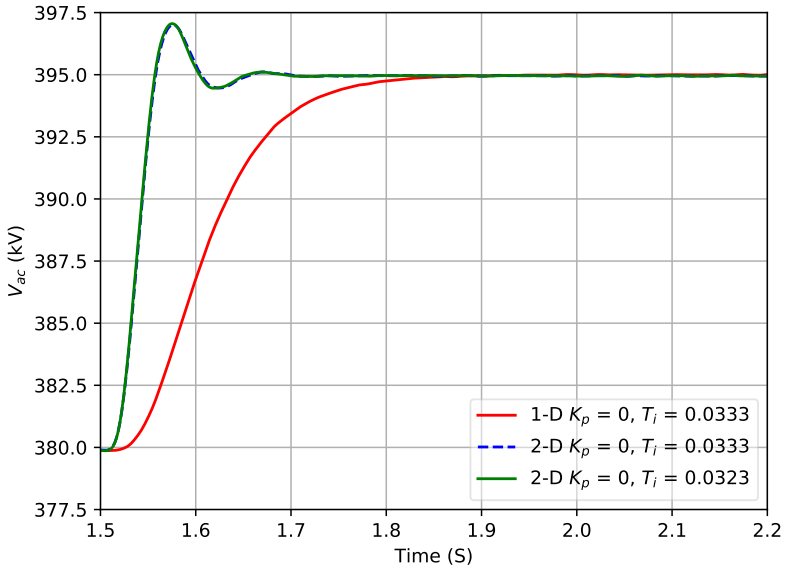

Figure 4.34: Response in the V_{ac} when applying a 19 kV in V_{ac} at t=1.5

It can be seen in the response for Q_{ac} and V_{ac} that the response in the 1-D and the 2-D controller is not equal. This is because the calculation of the error is different, as previously

mentioned. The Q_{ac} response show that the 2-D controller will have a faster response than the 1-D. Another thing to notice is that the 2-D controller will have an overshoot before settling at the reference value which is something the 1-D controller does not have.

The reason for a faster response for the 2-D controller the error given to the PI will be larger since the measured Q_{ac} will be amplified with the droop constant causing a larger error, however in the d-axis loop it was discovered the opposite effect, this is because the error in the d-axis control loop the error is multiplied with the inverse of its droop constant.

4.4.6 Reactive Power and AC voltage Limit Comparison of the 1-D and 2-D Control

The following simulations are conducted in order to validate that the response of the 2-D controller will stay within the limits ("limitation box"), when conducting a step in V_{ac}. The V_{ac} step applied is 19 kV and the simulation is conducted with an AC grid with a SCR of 2.5. By performing a step in reactive power it is possible to evaluate how the voltage limits and reactive power limits will affect the step-response of Q_{ac} and V_{ac} control. The following simulations are conducted in order to evaluate how the limitation algorithm will work to keep the Q_{ac} and V_{ac} within the limitation "box". Table 4.18 shows the tuning parameters used in Q_{ac} control.

Table 4.18: Limits and tuning parameters used for simulation

Control mode	**Upper limit**	**Lower limit**	K_p	T_i
Q_{ac}	400	-400	0	0.0303
V_{ac}	399	361	0	0.0333

Figure 4.36 and Figure 4.35 displays the response when various steps of reactive power are applied when operating in Q_{ac} control. The limits are not tested for operation in the V_{ac} control loop since Q_{ac} and V_{ac} are dependent on each other. This means that a step in Q_{ac} will also affect the V_{ac} response where it is possible to see if the response is within the limits.

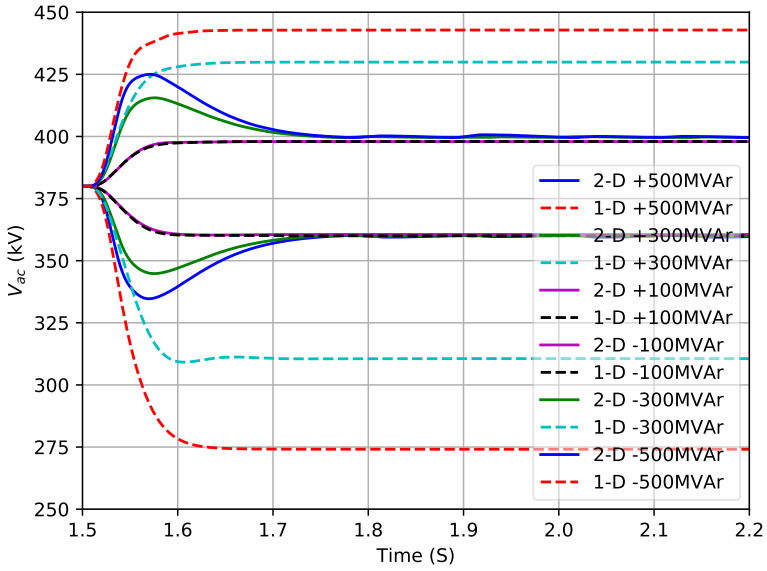

Figure 4.35: Validation of the limitation algorithm, and comparison of the controllers when applying various reactive power steps operating in Q_{ac} control

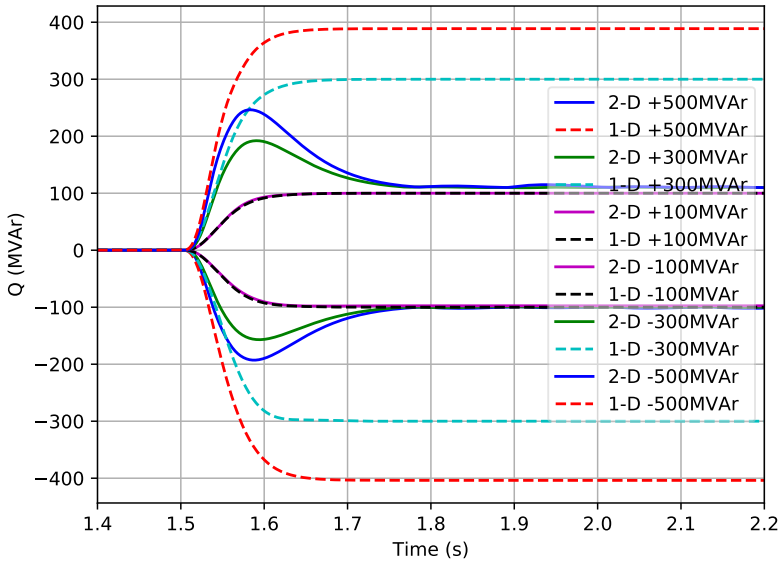

Figure 4.36: Validation of the limitation algorithm, and comparison of the controllers when applying various reactive power steps operating in Q_{ac} control

The results show that the response for the 1-D and 2-D controllers are different. For the 1-D controller, the V_{ac} response is not limited by the upper and lower limit. For example, for a step of ± 500 MVAr and ± 300 MVAr the 1-D response will go above the voltage limit and stay at that value. When comparing with the AC voltage in the 2-D controller it can be seen that the 2-D response is limited by the upper and lower limit. The response will have an overshoot before it reaches steady state at the upper and lower limit of the AC voltage. This implies that the response in the V_{ac} loop will be limited by the V_{ac} limitation before being limited by the Q_{ac} limitations. This is the reason the 2-D controller stops at 100 MVAr in the reactive power. The 1-D controller will only be limited by the Q_{ac} limits due to a "hard limiter", which contains limits for the reactive power and also the current limitations in the PI controller. Since the 1-D upper level control scheme does not contain any limits for V_{ac}, it will require a grid with a higher SCR than 2.5. However the 2-D controller manages to operate within the limits when connected to an AC grid with a low SCR.

Chapter 5

Results from Testing the 2-D controller in a PtP and MTDC System

The results presented in this chapter are performed to test the 2-D controller for scenarios were converters are connected as either a PtP-HVDC- or 3-terminal MTDC system. The 2-D controller is tested to verify if it can achieve seamless switching in a PtP-HVDC link. Then, the 2-D controller is evaluated when 3-phase faults are applied at the AC side of each converter in a PtP-HVDC system. This is done to check if the 2-D operates to keep the voltage and power limits during a fault. The PtP-HVDC link will then be expanded into a 3-terminal MTDC system to test the response of how P_{ac}, V_{dc} and droop control operates for 2-D control compared to the 1-D control. Further it is investigated how the controllers respond to switching between converter modes in a 3-terminal system. In the end, the 2-D and 1-D controller are tested for two different faults in a 3-terminal system. The configuration of the test systems used for simulations can be seen in section A.5

Since the faults are applied at the AC side of the converter it should be noted that the AC grid is modelled as an equivalent grid. The SCR used for the different grids in the fault simulations are presented in Table 5.1. The classification of the SCR is given in Table 4.13 and the parameters are listed in Table B.5.

Table 5.1: SCR for the AC grids of the different converter stations

	Cm-A1	Cm-C1	Cm-B2	Cm-B3	Cm-F1
SCR	38.1	12	38.3	25.5	4.77

5.1 Seamless Switching of d-axis Control Loop in a PtP-HVDC System

It is believed that the 2-D controller has a seamless switching because it only consists of one control loop for V_{dc} and P_{ac}. This means that there is no need for switching control mode by using a switch, the control mode is instead switched by adjusting the gradient of the slope.

As previously addressed in Figure 1.4, when conducting an uncontrolled switching in the 1-D controller, transients are present in the response. One goal for developing the 2-D controller was that these switching transients should be eliminated by obtaining a seamless switching between the control modes. Seamless switching will make it possible to switch when ever it is needed.

The parameters used for simulations are shown in Table 5.2. The arrows in the table indicates a change in control mode and tuning parameters. By performing switching, the parameters are changed accordingly. When performing a manual switching from P_{ac} to V_{dc}, K_p is changed from 0 to 8, and T_i from 0.0303 to 0.00367 and vice versa. Cm-C1 is set as P_{ac} control, supplying 300 MW to Cm-A1 which operates in V_{dc} control. It should be noted that the uncontrolled switching between control modes is performed at approximately 1.5 seconds.

Table 5.2: Data for seamless switching simulations showing the switching of control mode and the change in tuning parameters before and after switching

Control mode switching	K_p	T_i
$P_{ac} \rightarrow V_{dc}$	$0 \rightarrow 8$	0.0303→0.00367
$V_{dc} \rightarrow P_{ac}$	$8 \rightarrow 0$	0.00367→0.0303

Figure 5.1 and Figure 5.2 depicts the responses in power and voltage for the 1-D and 2-D controller when switching from P_{ac} to V_{dc} control.

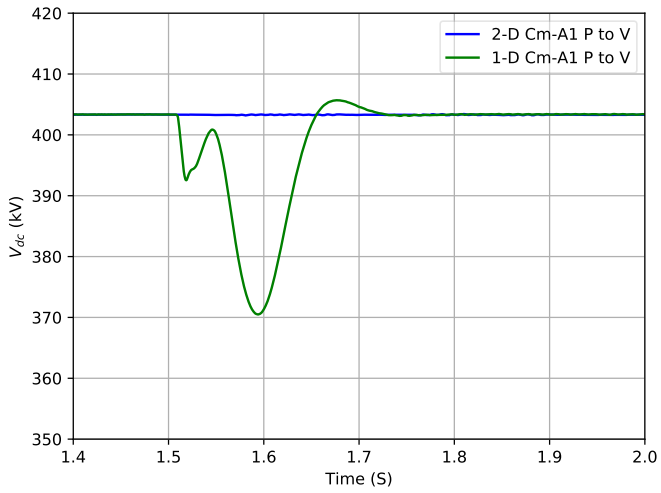

Figure 5.1: Comparison of the response in voltage when switching from P_{ac} control to V_{dc} control in the HVDC link

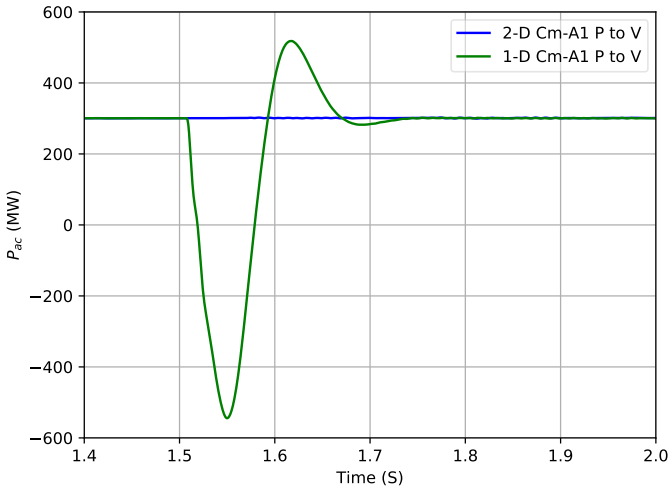

Figure 5.2: Comparison of the response in power when switching from P_{ac} control to V_{dc} control in the HVDC link

When analyzing the response of the voltage for the 1-D controller, it can be seen that the voltage transient decreases all the way down to 370 kV. Since the transient is in a negative direction it is not critical. The voltage response of the 2-D controller shows that a seamless switching is obtained. It can be seen that the response of the 2-D controller contains oscillations after switching, these oscillations can be neglected due to their amplitude.

For the power response, the results show that switching cause a transient in the 1-D

controller of ΔP of 846 MW, from 300 MW to -546 MW. When comparing the 1-D with the 2-D control response, it shows that 2-D manage to achieve a seamless switching between the control loops. To summarize, the voltage and power responses show that seamless switching is obtained for the 2-D controller when switching from P_{ac} to V_{dc} control.

Figure 5.3 and Figure 5.4 depicts the response in DC voltage and power when switching from V_{dc} to P_{ac} control in the 1-D and 2-D controller. The simulation is carried out in the same manner as when switching from P_{ac} to V_{dc}. The data used for simulations are shown in Table 5.2.

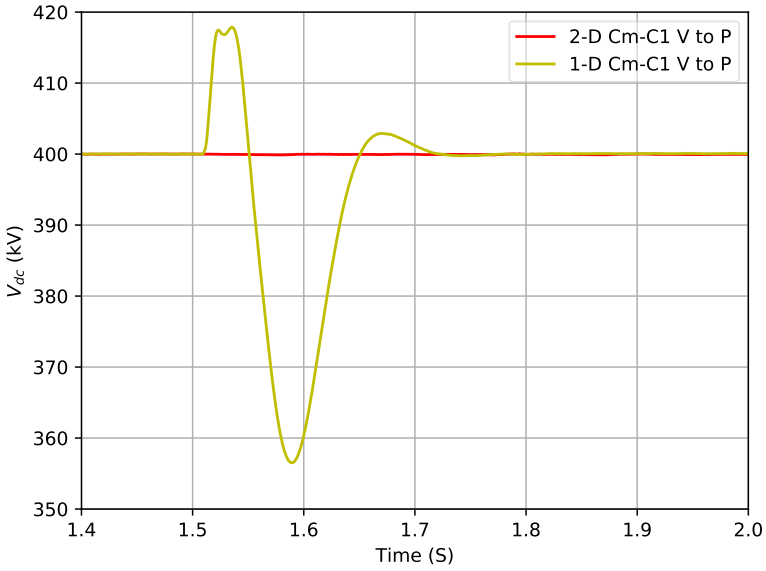

Figure 5.3: Comparison of the response in voltage when switching from V_{dc} to P_{ac} control

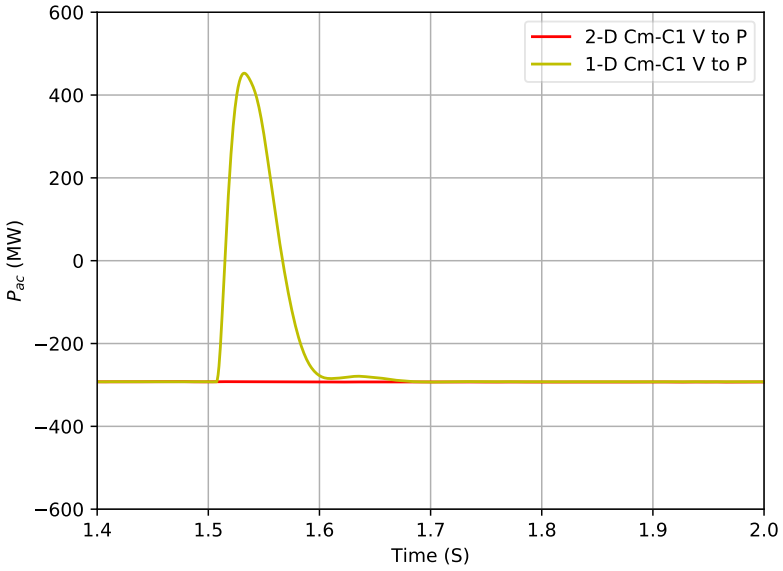

Figure 5.4: Comparison of the response in the power when switching from V_{dc} to P_{ac} control

The results from the switching show that there will be transients present in the voltage and power response of the 1-D controller. Also in this case, the 2-D controller is unaffected by switching from V_{dc} to P_{ac} control.

The results shows that a 2-D controller will eliminate the problem with transients when switching between both control modes in the d-axis control loop. The switching is seamless regardless if the control mode is changed from P_{ac} control to V_{dc} or vice versa. Making seamless switching possible creates new possibilities for the system operator which now has the chance to change control modes whenever it is needed.

5.2 Fault Analysis of PtP-HVDC link

To evaluate the operation of the 2-D controller when a fault is applied in the AC bus-bar at the converter station in the PtP-HVDC link. In the following simulations, the 2-D controller will be simulated in a PtP-HVDC link where one converter will operate as V_{dc} control and the other in P_{ac} control. The tuning parameters used for the simulations are shown in Table 5.3.

Table 5.3: Data used for simulation of a 3-phase fault applied on a 2-terminal HVDC system

Controller	K_p	T_i
2-D	0	0.0303
2-D	1.5	0.0303
1-D	0	0.0303

One simulation was conducted for the 1-D controller and two for the 2-D controller. This was done to see how 1-D and 2-D controller behaves when using the same tuning parameters. The second scenario for 2-D was conducted to evaluate how the proposed tuning parameters will respond to a fault compared to the 1-D controller. The fault scenarios applied to the HVDC link are:

- 3-phase fault on Ba-A1 to cause an outage of Cm-A1
- 3-phase fault on B0-C1 to cause an outage of Cm-C1

5.2.1 3-Phase to Ground Fault on Ba-A1

In this simulation a 3-phase to ground fault is applied at Ba-A1 causing an outage of Cm-A1. The duration of the fault is 500 ms, the fault is applied at approximately t=1.5s and released at t=2s. The data used for simulations is presented in Table 5.3. When the fault is applied, the 2-D controller should work to keep the voltage within the converter limits of the system. This was previously tested for voltage and power limits in subsection 4.3.6. Figure 5.5 depicts the fault location in the HVDC system. During the simulation, Cm-A1 is set as V_{dc} control and Cm-C1 is set to P_{ac} control. Cm-C1 should in this simulation operate in rectifier mode supplying the system with 400 MW. Figure 5.6 and Figure 5.7 depicts the voltage and power response during the 3-phase to ground fault.

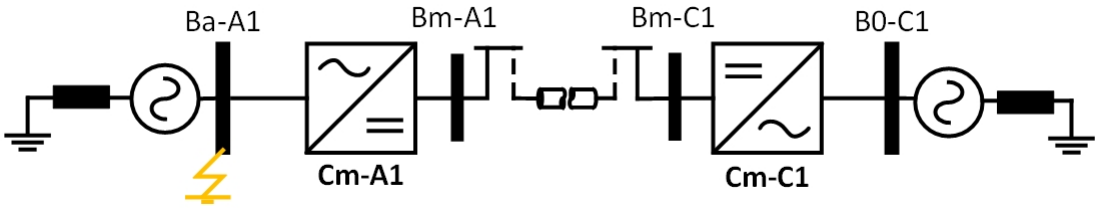

Figure 5.5: Location of the 3-phase to ground fault applied at Ba-A1

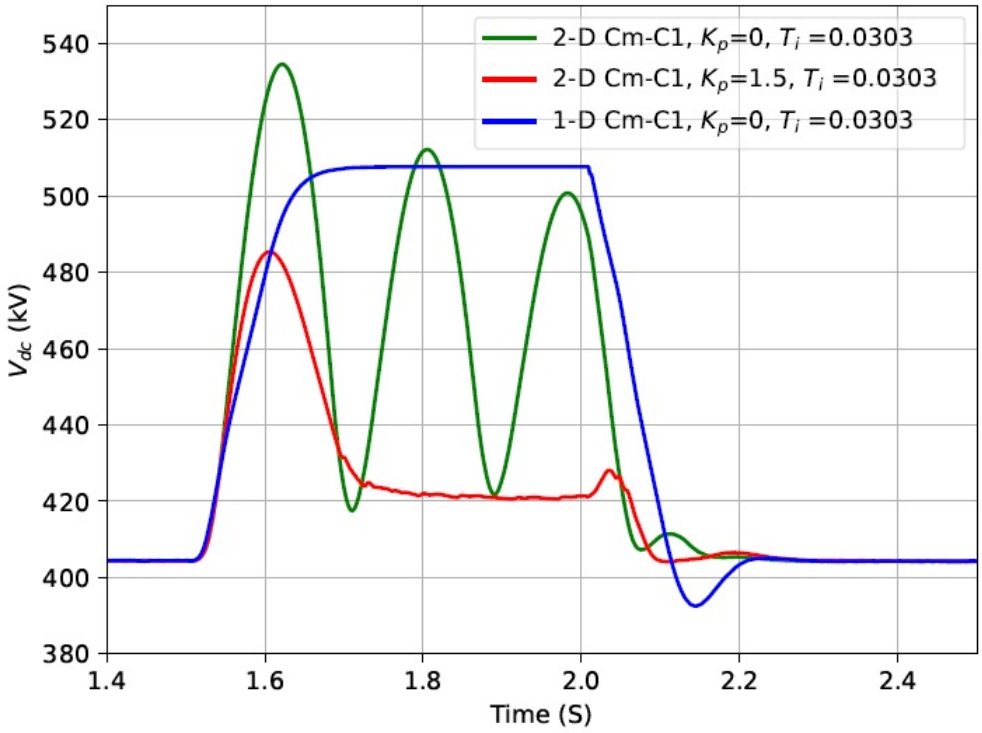

Figure 5.6: Voltage response of Cm-C1 when a 3-phase fault is applied at Ba-A1 to have an outage of Cm-A1. The green signal shows the 2-D controller using 1-D tuning gains, the red signal is the 2-D with proposed tuning gains and the blue shows the 1-D controller

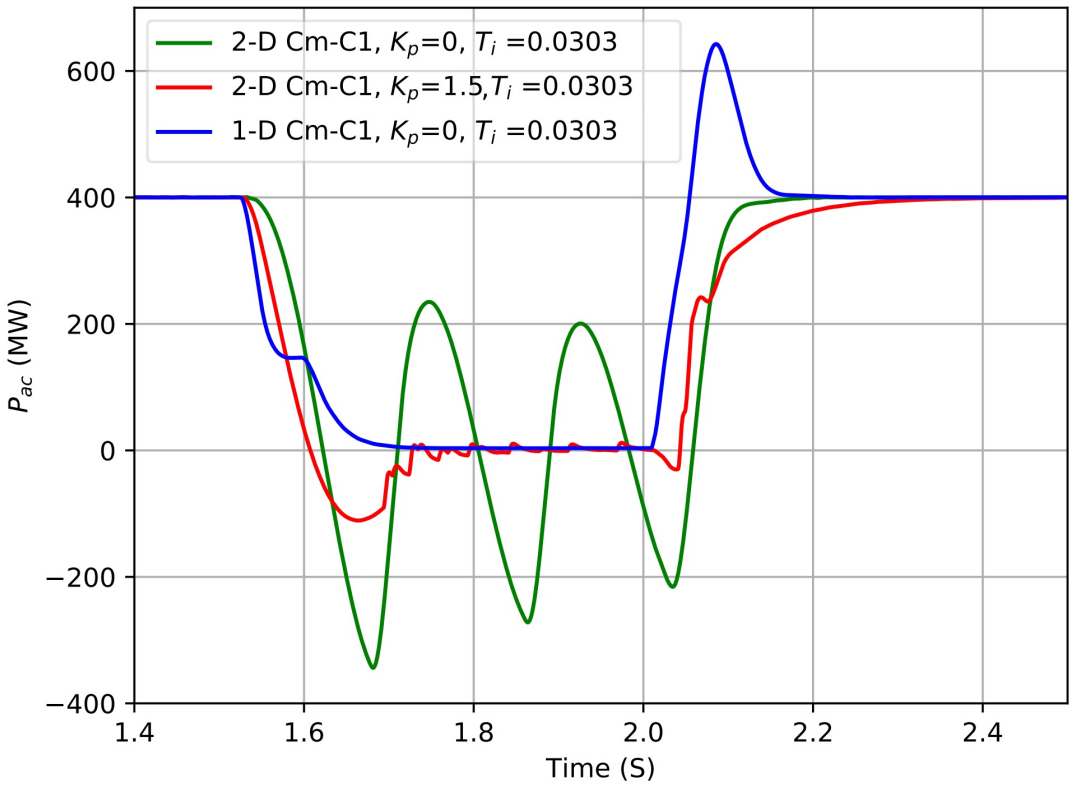

Figure 5.7: Response in power of Cm-C1 when a 3-phase fault is applied at Ba-A1 to have an outage at Cm-A1.The green signal shows the 2-D controller using 1-D tuning gains, the red signal is the 2-D with proposed tuning gains and the blue shows the 1-D controller

The results show that when the 2-D controller is using the 1-D tuning parameters, the response of the 2-D controller becomes unstable. For the whole duration of the fault the 2-D controller with 1-D gains is operating to reduce the voltage transient by controlling the voltage back to the control limits. But, it can be seen that the response will not be stable until the fault is released. The transients occur because the measured values are located above the voltage limit, meaning that the error is measured as the distance from the operating point to the voltage limit. This implies that the controller is operating in V_{dc} control when trying to stay at the limit. As discovered in subsection 4.3.2 when using P_{ac} tuning parameters in V_{dc} control operation, the response becomes unstable.

When comparing with the results from the 1-D controller, the 1-D has a smooth signal reaching a voltage level of 507 kV until the fault is released. A difference from the 1-D controller compared to the 2-D controller is that it will not operate to reduce the voltage transient to the limit during the fault. Observing the response for the 2-D controller when it operates using the proposed tuning parameters, the highest value of the voltage is 483 kV. As illustrated for the 2-D controller with proposed gains, the control operates to reduce the voltage transient to the limits during the fault. After approximately 0.1 seconds the voltage

is reducing its value, and after 0.25 seconds the voltage is kept at 420 for the rest of the fault time.

A proposal of another way to control the response is to implement gain scheduling in the 2-D controller. This would mean that e.g if the voltage goes above the limits, the tuning parameters would change to the ones that work best for V_{dc} control. But this will require more research to be validated.

5.2.2 3-phase to Ground Fault Applied at B0-C1

In the following results a 3-phase fault is applied at bus-bar B0-C1 to cause an outage of Cm-C1. The fault is applied at approximately t=1.5s with a duration of 500 ms. The location of the fault is shown in Figure 5.8. The settings for the simulation are shown in Table 5.3.

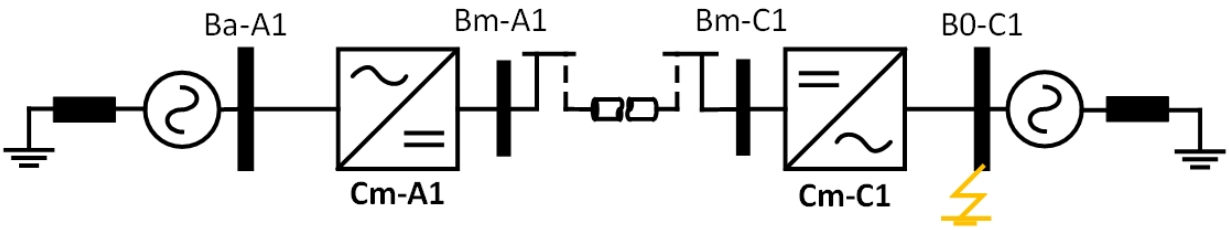

Figure 5.8: Location of 3-phase to ground fault at bus B0-C1

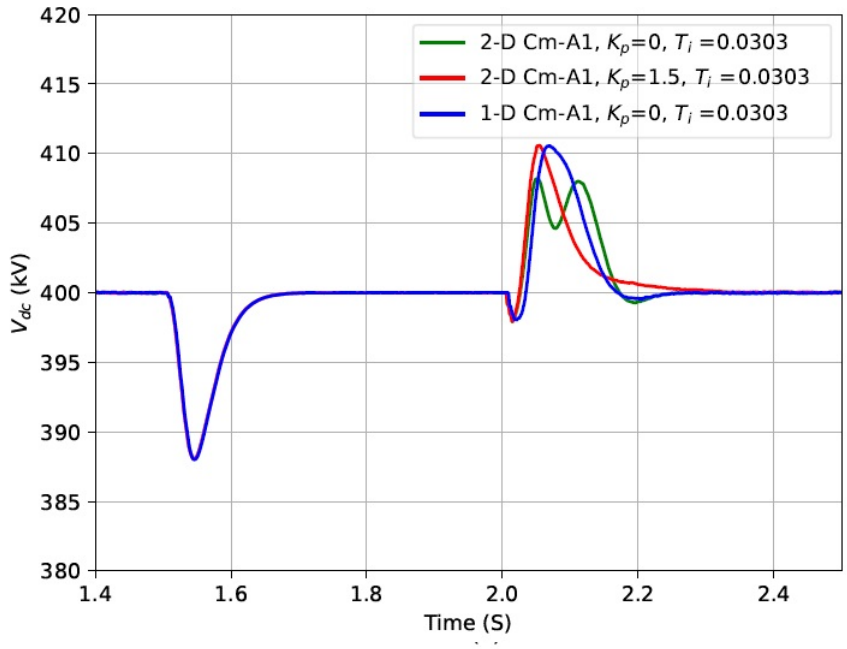

Figure 5.9: Voltage response in Cm-A1 when applying a 3-phase to ground fault at bus B0-C1

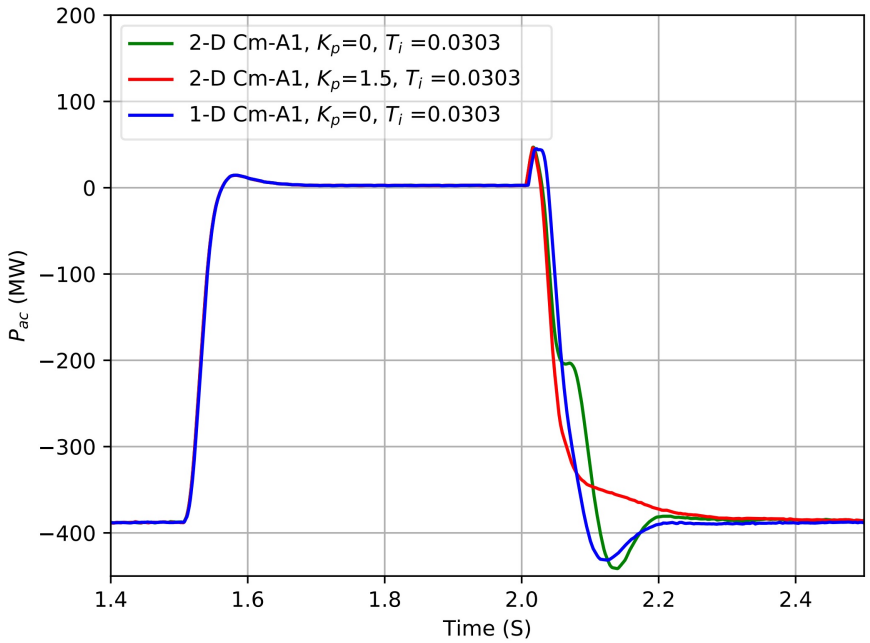

Figure 5.10: Power response in Cm-A1 when applying a 3-phase to ground fault at bus B0-C1

The results show that an outage of Cm-C1 does not create as high peak in the voltage as when a fault is disconnecting Cm-A1. The response of the 2-D controller with the 1-D tuning parameters will become unstable with a maximum voltage of 408 kV. The 2-D controller using proposed tuning parameters has a peak of 410.5 kV. When comparing with the response of the 1-D controller, it has an almost equal spike in the voltage of 410.5 kV. The responses look almost the same, but the 2-D controller with 1-D tuning gains has a higher settling time when the fault is released than the other two test scenarios.

The power the response is almost equal in all simulation results. Where the 2-D controller use proposed tuning gains will not cause overshoot in the response at the time when the fault is released. The control ensures that the power goes to 0 MW, and that it goes back to 400 MW when the fault is released. These simulations show that an outage of Cm-A1 is more critical than an outage of Cm-C1.

5.3 Droop Control Comparison Between the Controllers in a MTDC system

The goal for the simulations in this subsection is to analyze how different droop constants affects the response of the 1-D and 2-D controller. Table 5.4 presents the tuning parameters, and the values for each of the different droop constants expressed as $\frac{1}{K_v}$ in pu values. For this case, Cm-B2 and Cm-B3 are set in DC droop control while Cm-F1 is set to ramp up the power from -200 to 200 MW. It should be noted that this is not a realistic case and is done to investigate the droop characteristic during a ramp-up in power. The V_{dc} reference value is 400 kV. In order to compare and test the performance of the droop slope, three different droop constants were selected. Two extreme values, (scenario 2 and scenario 3) were chosen to represent the droop characteristic when operating close to V_{dc} or P_{ac} control. Scenario 1 is chosen to represent a droop slope in between these two extreme values.

Table 5.4: Data used for the different droop slopes in the 1-D and the 2-D controllers

Scenario	1-D settings $\frac{1}{k_v}\frac{MW}{kV}]$	2-D settings $\frac{x_2-x_1}{y_2-y_1}$
1	20	$\frac{(800-(-800))/800}{(380-420)/400}$
2	7.14	$\frac{(250-(-250))/800}{(382.5-417.5)/400}$
3	80	$\frac{(800-(-800))/800}{(395-405)/400}$
K_p	0	1.5
T_i	0.0303	0.0303

The response of the droop slope in scenario 1 is depicted in Figure 5.11, scenario 2 in Figure 5.12 and scenario 3 in Figure 5.13.

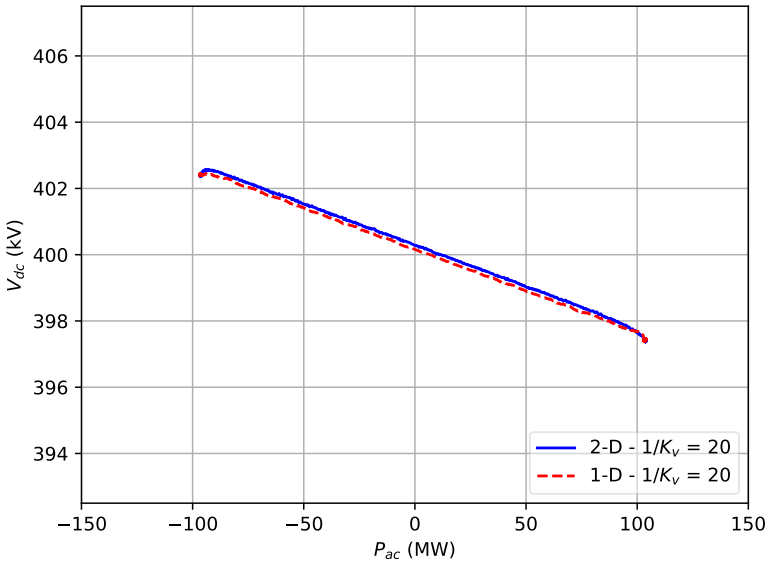

Figure 5.11: Scenario 1 - Comparison of the droop slope characteristic for the 1-D and 2-D controller

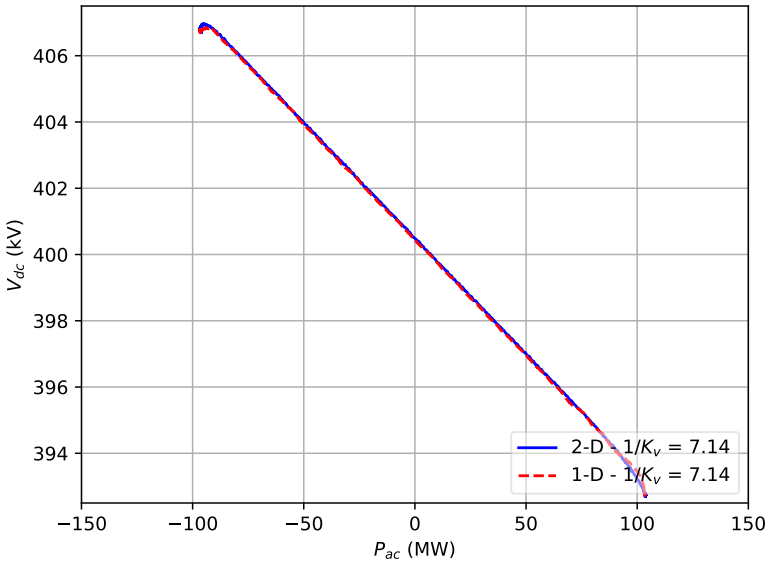

Figure 5.12: Scenario 2 - Comparison of the droop slope characteristic for the 1-D and 2-D controller

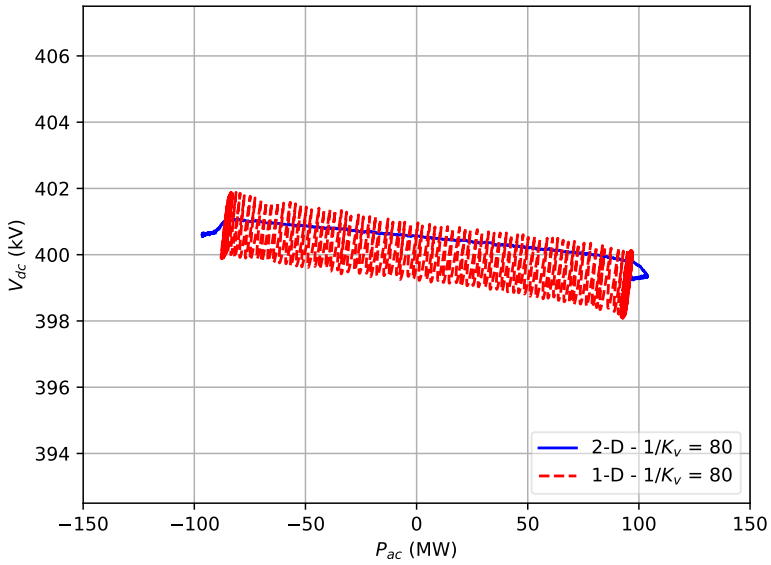

Figure 5.13: Scenario 3 - Comparison of the droop slope characteristic for the 1-D and 2-D controller

The results obtained from scenario 1 shows that 1-D and 2-D obtain an equal droop characteristic and the responses are almost on top of each other. Scenario 2, which represents a high K_v, it can be observed that steeper the curve the more overlapping the responses will be. For scenario 3 which is implemented with a low K_v the slope is almost horizontal it can be seen that the 1-D controller becomes unstable, but it will have the same droop characteristic as the 2-D. The instability in the 1-D droop slope is caused two reasons.

The first one is when the droop slope is close to operating as V_{dc} control, the 1-D will become unstable since the tuning gains are the ones used for P_{ac} control. The instability when using P_{ac} gains in V_{dc} control has previously been tested, and is presented in Figure 4.11. The other reason is that the calculation method of the error is different for the two controllers when operating in droop. For the 1-D controller this means than an almost horizontal droop slope will lead to a large error since it calculates the error in x-direction. A larger error will make the PI controller operate faster, in this case the PI controller will be more sensitive to a small change in y-direction. Since a small change in y-direction leads to a big change in x-direction. However the oscillations will not be present in the droop slope of the 2-D controller. This is because the 2-D controller use one set of tuning gains that can operate for V_{dc}, P_{ac} and droop control. Another factor is that the error in the 2-D is calculated in both x- and y-axis direction sending a smaller error to the PI controller.

5.3.1 Switching Between Control Modes in a 3-terminal MTDC System

In this simulation, the 3-terminal system is first set as master slave control meaning that one converter is set as a master station while the rest are operating as slave buses. The master-slave strategy was explained in subsection 3.4.1. In order to evaluate how a switching between the control modes in a MTDC system, two of the converters are switched from the master-slave strategy to the DC voltage droop control. This is done to evaluate the response and verify if seamless switching is possible for the 2-D controller in a 3-terminal system. The switching between the control modes is an uncontrolled switching.

The parameters used for this power flow analysis are listed in Table 5.5. The table shows that the control mode of Cm-B2 and Cm-B3 is switched to droop control during operation. It also contains the tuning parameters used for the simulation. The reason why the tuning gains is only changed for Cm-B2 is that 1-D controller use the same gains for P_{ac} and droop control. Figure 5.14 shows the voltage response while Figure 5.15 depicts the response in power. Only Cm-B2 is evaluated in these results since it has the most significant response compared to Cm-B3. Cm-F1 is not evaluated because it is always producing 300 MW. Before switching, Cm-B3 is set to operate in inverter mode, consuming 700 MW. Cm-B2 is set as the master station providing 400 MW to Cm-B3 plus cable losses of both Cm-F1 and Cm-B2, since Cm-F1 is providing a fixed amount of power to the DC grid.

Table 5.5: Simulation parameters for switching between control modes in a 3-terminal MTDC system

Controller	Converter	Control mode	K_p	T_i	Droop constant
1-D	Cm-B2	$V_{dc} \rightarrow$ Droop	8→0	0.00367 → 0.0303	20
	Cm-B3	$P_{ac} \rightarrow$ Droop	0	0.0303	13.333
	Cm-F1	P_{ac}	0	0.0303	-
2-D	Cm-B2	$V_{dc} \rightarrow$ Droop	1.5	0.0303	$\frac{(420-380)/400}{(-800-800))/800}$
	Cm-B3	$P_{ac} \rightarrow$ Droop	1.5	0.0303	$\frac{(420-380)/400}{(-800-800))/800}$
	Cm-F1	P_{ac}	0	0.0303	-

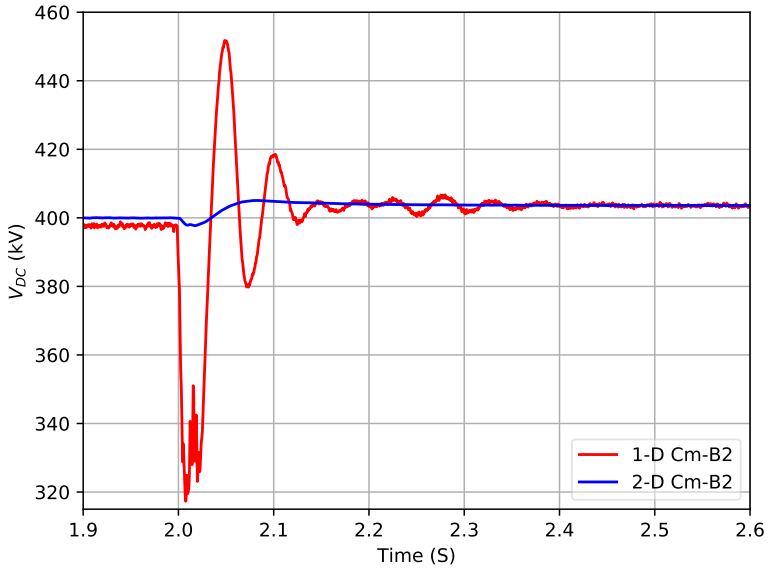

Figure 5.14: DC response of Cm-B2 when control mode is switched from V_{dc} to DC voltage droop control

The most significant response appear when performing an uncontrolled switching from master- to droop control. For the voltage response it can be seen that the switching between control modes cause a transient in the voltage for the 1-D controller. The highest transients has a peak value of around Δ50 kV. A such high peak in the voltage can cause breakdown in the DC cables over time, if control modes are changed often. The 2-D controller does not experience any oscillations in the voltage response during the switching. However, the response of the 2-D controller show a small dip in the voltage immediately after the switching is performed. The voltage then increased due to the change of operation (converter is now operating in DC voltage droop control). The reason why the response of the 2-D controller is not unaffected by the switching is because a change in power flow will occur when more than one converter is switched to droop control.

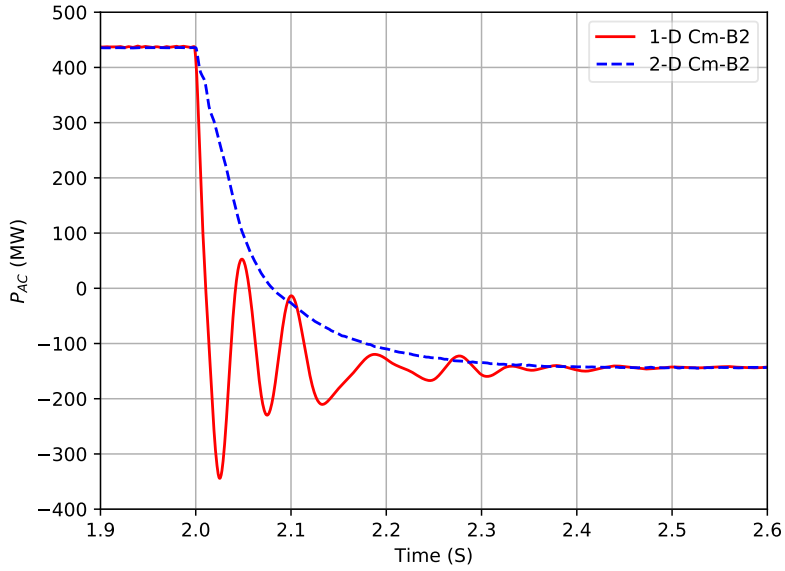

Figure 5.15: Power flow response of Cm-B2 when control mode is switched from V_{dc} to DC voltage droop control

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The power flow show that the 2-D controller has a response with only negligible oscillations, while the 1-D controller has an oscillating response. Even though the 1-D controller has oscillations, the T_s is almost equal for the two controllers. The reason why the power is decreasing after switching is because the change in power flow then two converters are switched from master-slave to DC droop control. The results show that the 2-D controller has a switching response with negligible oscillations in the power when the control modes are changed. A seamless switching in the 3-terminal system will give the system operator the possibility to change the operation strategy of the MTDC system whenever it is needed.

5.4 Fault Analysis of 3-Terminal MTDC System

The two cases were tested for the 2-D controller in order to evaluate its performance when a fault is applied in a 3-terminal MTDC system:

- 3-phase fault resulting in an outage of Cm-B3
- Permanent outage of Cm-F1

The goal with these simulations is to see how the 2-D controller operates when a fault is applied to one of the converters in the MTDC compared to the 1-D controller. The faults are applied to a MTDC system system operating in either DC voltage droop control or the master-slave strategy.

5.4.1 3-Phase to Ground Fault Applied at Ba-B3 to Cause an Outage of Cm-B3

The 3-phase to ground fault applied at approximately t=2 seconds to cause an outage of Cm-B3. The settings used for the simulation are presented in Table 5.6. Figure 5.16 depicts the location of the fault in the MTDC network. The simulation is conducted in order to evaluate how Cm-F1 and Cm-B2 reacts to an outage of Cm-B3. Since both Cm-B2 and Cm-B3 are equipped with droop control, an outage of Cm-B3 should make Cm-B2 contribute to the power consumption. This is because Cm-F1 will keep supplying power even though there is an outage of Cm-B3.

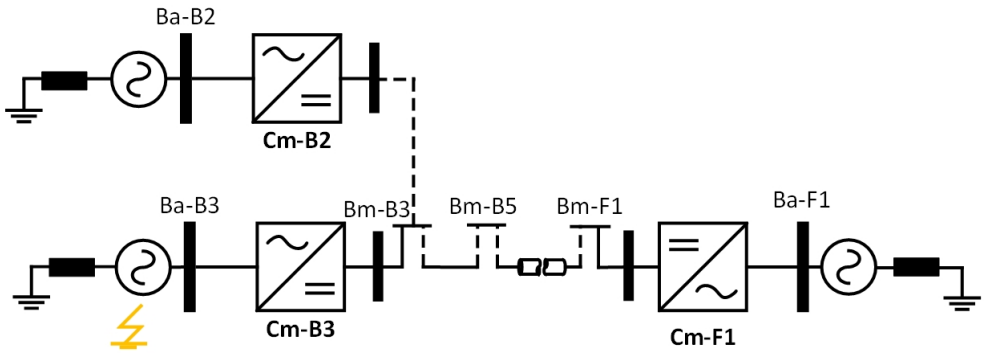

Figure 5.16: Location of 3-phase to ground fault at Ba-B3 in the 3-terminal MTDC system

Table 5.6 displays the simulation parameters for both 1-D and 2-D controllers. The value of $\frac{1}{K_v}$ is chosen in order to make Cm-B2 and Cm-B3 take as much power and voltage as possible, and since the droop slope was proven to be stable in section 5.3. The values of the droop constants are chosen to have an equal power sharing in the system.

Table 5.6: Data used for MTDC 3-phase to ground fault

Overall settings			1-D control settings			2-D control settings		
Converter	P^*_{ac} [MW]	**Control mode**	K_p	T_i	$\frac{1}{K_v}$	K_p	T_i	$\frac{x_2-x_1}{y_2-y_1}$
Cm-B2	0	Droop	0	0.0303	20	1.5	0.0303	$\frac{(800-(-800))/800}{(380-420)/400}$
Cm-B3	0	Droop	0	0.0303	13.33	1.5	0.0303	$\frac{(800-(-800))/800}{(380-420)/400}$
Cm-F1	400	P_{ac}	0	0.0303	-	1.5	0.0303	-

Figure 5.17 represents power flow response and Figure 5.18 depicts the voltage response, when a 3-phase fault to ground occurs at Ba-B3.

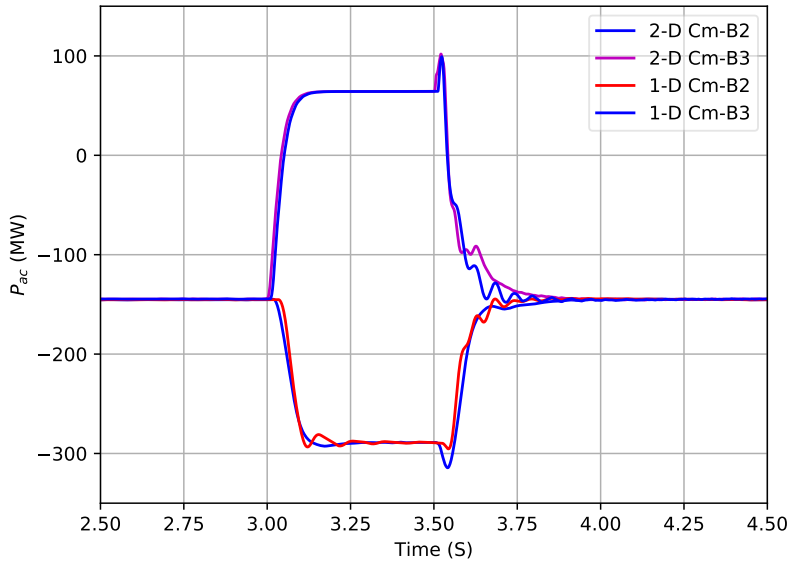

Figure 5.17: Power response of Cm-B2 and Cm-B3 when having a 3-phase to ground fault applied to have an outage of Cm-B3 for 500 ms

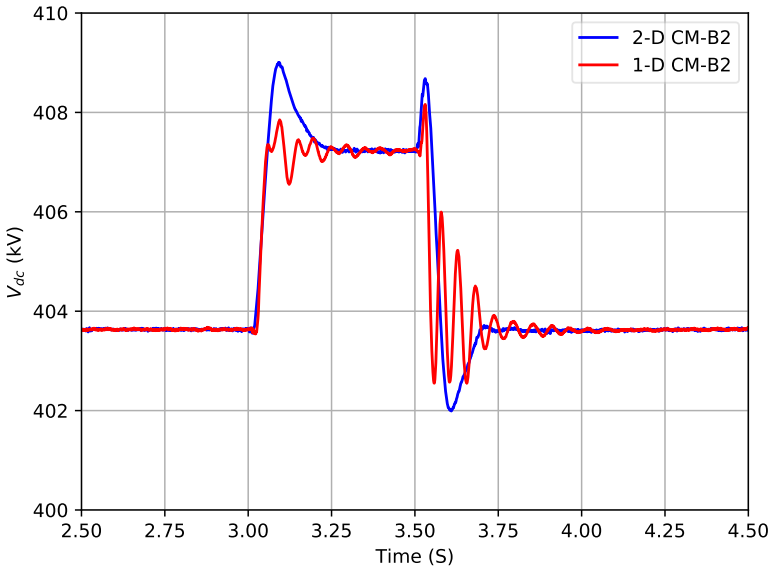

Figure 5.18: Voltage response of Cm-B2 and Cm-B3 when having a 3-phase to ground fault applied to have an outage of Cm-B3 for 500 ms. Cm-B3 is the upper blue curve, while Cm-B2 is the lower blue curve

As seen in the power flow response, Cm-B2 will compensate for the outage of Cm-B3 by consuming more of the power during the time of the fault. This means that an outage of Cm-B3 will not have a big impact on the generation from Cm-F1. Another factor to evaluate is that the 2-D controller has less oscillations in the response for both power and voltage. Especially the voltage response of the 1-D controller starts oscillating as soon as the fault is applied. The magnitude of the oscillations of the 1-D controller decrease with time as the PI controller operates to remove the error. The 2-D controller voltage response contains negligible oscillations, but has a peak in the voltage with a value of around 7.5 kV at the moment when the fault is released. Since the time duration and magnitude of the peak is small, it will be not critical.

After the fault is cleared, Cm-B3 will start to energize which cause a response containing transients. The reason for this transient is that when the fault is cleared Cm-B3 will start to consume power. Since Cm-B2 is already operating to consume power, Cm-B2 and Cm-B3 will "fight" each other creating a peak right after switching.

5.4.2 Permanent Fault Applied at Bm-F1 with Cm-B2 and Cm-B3 in Droop Control

In this test scenario a permanent trip of Ba-F1 is performed at t=2s. Cm-F1 will be disconnected from both AC grid and the DC grid at the same time when the fault is applied. The MTDC system is set to operate in DC droop control strategy during the simulation.

Two scenarios are simulated where the droop constants have different values, as can be seen in Table 5.7. As the droop slope in Figure 5.11 shows, the response of the power and voltage when using $\frac{1}{K_v} = 20$, Cm-B2 should have a stable response in voltage and power. Cm-B2 and Cm-B3 are set to operate in droop control. Cm-F1 is operating in P_{ac} control supplying the grid with 500 MW.

Table 5.7: Settings for simulating a permanent outage of Cm-F1 in a MTDC system with droop control strategy

	Overall settings		**1-D control settings**			**2-D control settings**		
	Converter	**Control mode**	K_p	T_i	$\frac{1}{Kv}$	K_p	T_i	$\frac{x_2-x_1}{y_2-y_1}$
Scenario 1	Cm-B2	Droop	0	0.0303	20	1.5	0.0303	$\frac{(800-(-800))/800}{(380-420)/400}$
	Cm-B3	Droop	0	0.0303	13.33	1.5	0.0303	$\frac{(800-(-800))/800}{(380-420)/400}$
	Cm-F1	P_{ac}	0	0.0303	-	1.5	0.0303	-

The location of the fault is shown in Figure 5.19. Figure 5.20 and Figure 5.21 displays the response of Cm-B2 when a permanent fault is applied at Ba-F1 to cause an outage of Cm-F1.

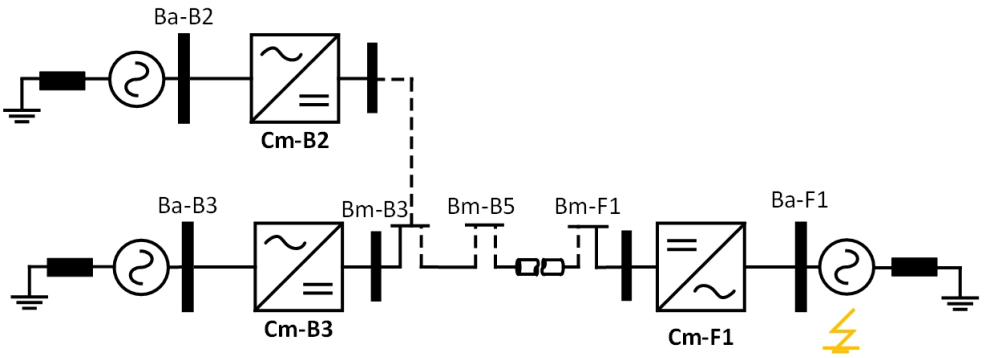

Figure 5.19: Fault location for the trip of Cm-F1

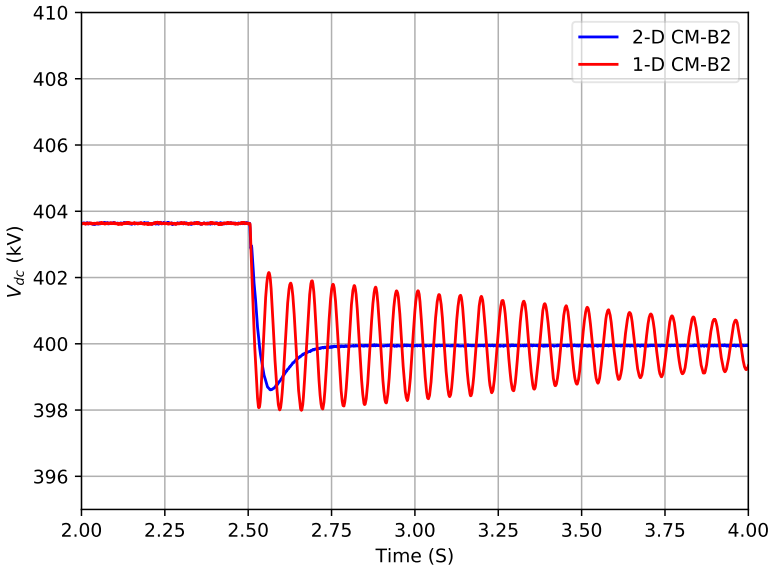

Figure 5.20: Response in the voltage of Cm-B2 during an a permanent fault applied at Cm-F1

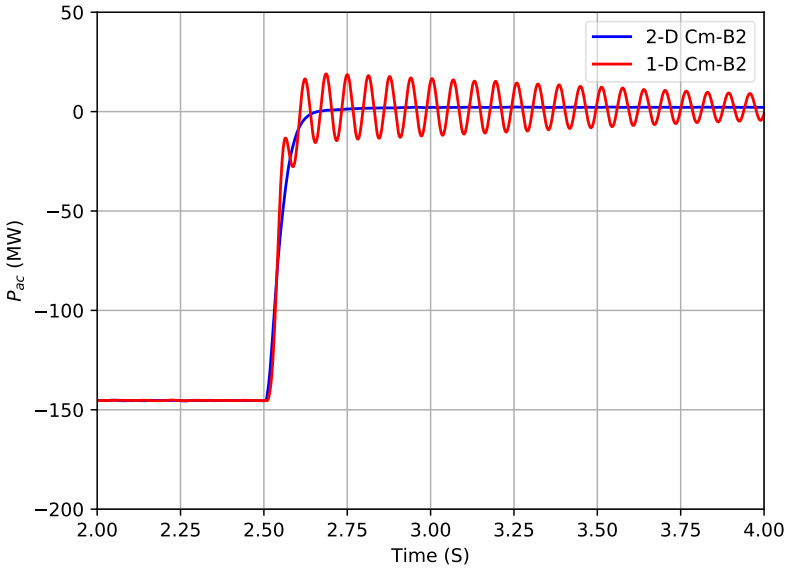

Figure 5.21: Power response when a 3-phase fault is applied to the AC grid connected to Cm-A1

When analyzing the response in the voltage, 2-D controller will experience an overshoot around 2.5 kV before the voltage stabilizes after 0.25 seconds at 400 kV. The response of the 2-D controller only contains negligible oscillations. However for the 1-D controller, the response show that the voltage becomes unstable immediately when a fault is applied at Ba-F1. However, the response of the 1-D controller will operate to reach steady state. It is believed that the reason for an unstable response in the 1-D controller is either because the size of the error will make the PI controller behave unstable. The other reason could be that the tuning parameters implemented in the 1-D controller can cause a negative effect keeping the PI controller from operating at it best to remove the error.

Outage of Cm-F1 in a MTDC System where a Master-Slave Strategy is Implemented

Before a fault is applied to the system, Cm-F1 is set in P_{ac} control providing 300 MW to the grid. Cm-B3 is set in P_{ac} control consuming 700 MW. Cm-B2 is set in V_{dc} control. A fault is applied to cause an outage of Cm-F1 at approximately t=2.8 seconds leaving Cm-B2 to provide the power to Cm-B3. The controller settings for the converters are listed in Table 5.8. The goal of the simulation is to see how Cm-B2 and Cm-B3 will respond to permanent outage of a generation unit in the MTDC system. As it was seen in subsection 5.4.2 when the system is set in droop control, the 2-D controller has a good operation for the applied fault. It is therefore interesting to investigate the 2-D controller response compared to the 1-D controller in a master-slave strategy. Figure 5.22 depict power flow response and Figure 5.23 shows the voltage response during this type of fault.

Table 5.8: Control parameters for the MTDC system during a permanent outage of Cm-F1

Control	Converter station	Cm-B2	Cm-B3	Cm-F1
1-D and 2-D	Control mode	V_{dc}	P_{ac}	P_{ac}
1-D	K_p	8	0	0
	T_i	0.00367	0.0303	0.0303
2-D	K_p	1.5	1.5	0
	T_i	0.0303	0.0303	0.0303

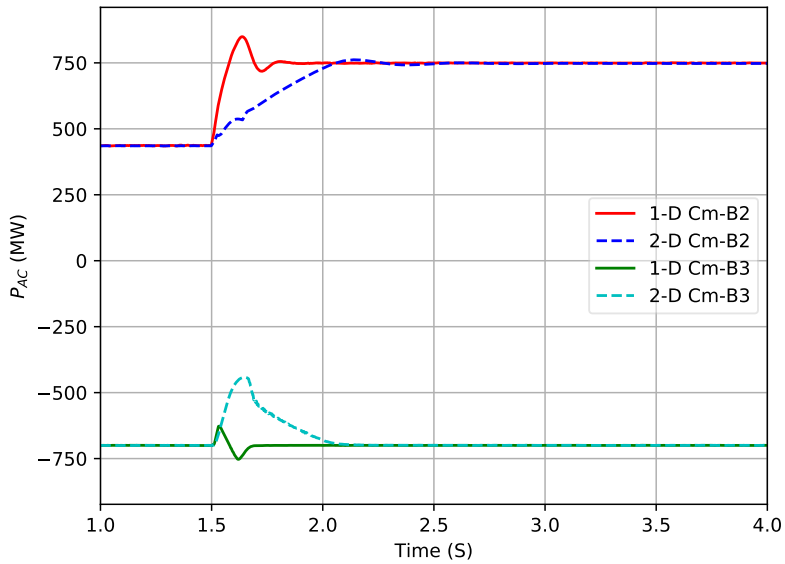

Figure 5.22: Power flow in Cm-B2 and Cm-B3 after a permanent outage of Cm-F1

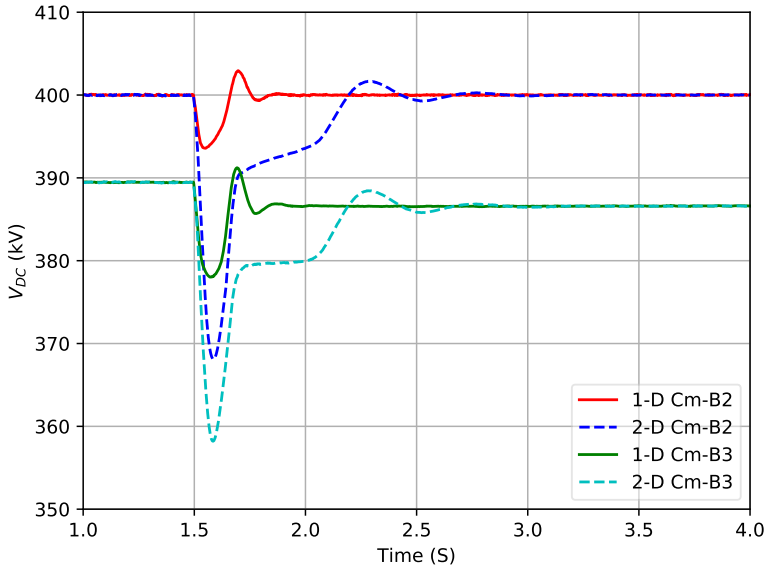

Figure 5.23: Voltage response in Cm-B2 and Cm-B3 after a permanent outage of Cm-F1

It can be observed in the power flow response that the settling time of 1-D is shorter than for the 2-D controller. This is because the 1-D controller use the gains which was obtained from the CIGRE manual, while the 2-D controller operates with the proposed gains for all control modes. Therefore, the 1-D will react faster than the 2-D controller which was also the case seen in subsection 4.3.2. The different tuning parameters cause the 2-D to react slower to the power change leading to a greater dip in power. However when observing the voltage behaviour it can be observed that a dip in voltage of the 2-D controller has a higher negative dip than that of the 1-D controller. Since it is more severe for the system to experience a high positive peak in the voltage, the negative dip is not seen as a critical problem.

Chapter 6

Conclusion

This thesis had the objective of developing a 2-D upper level control scheme for use in a VSC-HVDC system. The goal of developing the 2-D controller was to achieve seamless switching, and to reduce the number of control loops in the upper level control structure. To validate the performance of the 2-D controller, it was tested and compared to a 1-D controller used as reference. The testing to validate the 2-D controller showed that it had an equal response when compared to the 1-D tested during normal conditions where the power was ramped up. This meant that the same tuning parameters could be used in the 1-D and the 2-D controller. It should be noted that the tuning parameters used in the 1-D controller was considered as extreme values.

The tuning of the d-axis loop was more time consuming than tuning the q-axis since it had a larger range between the extreme values, while the range between the extremes in the q-axis was small. The 2-D controller was tuned to obtain two set of proposed tuning parameters that would work for V_{dc}, P_{ac} control and Q_{ac}, V_{ac} control. Since it only used one set of tuning parameters in each control loop it was more stable than the 1-D controller, which changes gains according to the control mode it operates in. As a consequence of only having one set of tuning parameters for the d- and q axis control loops, the 2-D will have a slower response than the 1-D. The only exception was when testing AC droop control where the 2-D controller had a faster response than the 1-D. It was also observed that the response of the 1-D controller became unstable when operating in DC droop control with the proposed gains of the 2-D controller. This implied that the 1-D controller would not be able to operate with the same change in tuning parameters as the 2-D controller. It was validated that the 2-D controller would not operate outside the control limits.

To evaluate the performance of the 2-D controller during non-ideal conditions, the 2-D controller was implemented in a PtP and 3-terminal HVDC system. The results from performing an uncontrolled switching showed that the 2-D controller achieved a seamless switching, were only negligible transients were present. The response of the 1-D and 2-D controller when operating as droop control in a 3-terminal MTDC system showed that both controllers followed the same droop characteristic. The 2-D controller showed a stable response for all the tested scenarios, while the droop slope of the 1-D controller became unstable when a low droop constant was implemented.

The observations from the fault analysis of a 3-phase to ground fault showed that in a

PtP system the 2-D controller worked to reduce the operating point to the control limits during the fault. The 2-D controller had a shorter settling time than the 1-D when the fault was cleared. For a 3-terminal MTDC system operating in droop control that will experience an outage of a converter station, the 2-D controller was proven to have a stable response and a shorter settling time than the 1-D controller. However, if a fault was applied to have an outage of a slave bus in a master-slave control strategy, the 2-D controller had a longer settling time and higher transients than the 1-D.

In order to give a better overview of the advantages/drawbacks of the 1-D and 2-D controller Table 6.1 displays a summary of the conclusion.

Table 6.1: Table showing advantages/disadvantages of the 1-D and 2-D controller

Ability/Performance	**2-D Controller**	**1-D Controller**
Response when operating in V_{dc}, P_{ac}, Q_{ac} ,V_{ac}	Equal to the 1-D controller, no further tuning needed	Equal to the 2-D controller
Tuning of PI controller needed to find proposed tuning parameters	Tuning is needed since controller only operates with one set of gains for d- and q-axis	No tuning is needed, controller will change gains when switching.
DC voltage droop control response	Slower response due to the error calculation method	Faster response due to the error calculation method
AC voltage droop control response	Faster response due to the error calculation method	Slower response due to the error calculation method
Transients during uncontrolled switching	Seamless switching is achieved when switching between control loops - Switching can be performed whenever it is needed	Does not have seamless switching. Response contains transients that could damage the system
Ability to keep the V_{dc} within its limits during a fault	Operates to reduce the voltage to the limit during a fault	Voltage goes outside the limits during a fault. Controller does not operate to reduce voltage for the duration of the fault
Performance when operating in DC voltage droop in a 3-terminal system	No oscillations in response of the droop slope in the range of droop constants tested	Oscillations in droop slope when using low value of K_v
Transients during uncontrolled switching between control loops in a 3-terminal system	Only contains negligible transients when switching between control loops	Transients present during switching
Performance when a fault is applied in a 3-terminal system	**Droop control:** Negligable transients present, shorter settling time and stable response **Master-slave strategy:** longer settling time and higher transient	**Droop control:** Transients present in response longer settling time, unstable response **Master-slave strategy:** shorter settling time and lower transients

6.1 Future Work

- Implement inner current control into the 2-D control scheme. If the current control could be implemented in the 2-D upper level control scheme, this would reduce the number of PI controllers even more.
- Expand the MTDC system to a 4 or 5 terminal one in order check if seamless switching can still be provided when more converters are present in the MTDC system
- In this thesis the 2-D controller was evaluated for an equivalent grid. Therefore it would be necessary to test connected to a more realistic grid
- Test the 2-D controller for more faults. This is to validate that the 2-D controller will work for all types of faults, and not only 3 phase fault or a trip of one converter which is the cases presented in this thesis
- Test the q-axis control loop for faults and seamless switching
- Implement gain scheduling in the 2-D controller
- Test the 2-D controller for adaptive droop control

Appendix A

System Design and Theory

A.1 Maximum Voltage

The cables of the DC system has to be able to withstand over-voltage for a short period of time during operation of a system. It is the HVDC controls that will work to control the over-voltage. [39] concludes after conducting several simulations that a voltage profile like the one in Figure A.1 should be used for a HVDC system. This means that the system can withstand a voltage of 1.25 p.u (500 kV for this system) for 50 ms. While it can withstand an over-voltage of 1.20 pu (480 kV) for 2950 ms. This means that it is possible to have an overshoot in the DC voltage of maximum 1.25 p.u. for a short duration of time. [39]

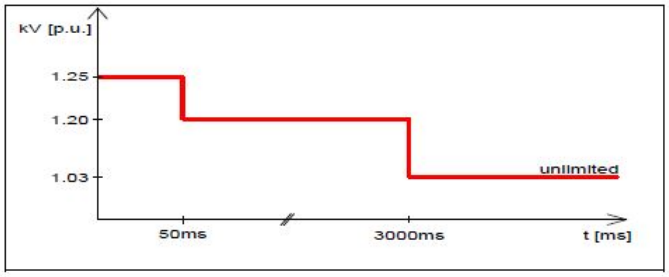

Figure A.1: DC voltage profile for a converter in a point to point system [39]

A.2 System Parameters

This section presents the different parameters used in the conventional PtP-HVDC link. Table A.1 presents PI tuning parameters for the CIGRE model. Table 4.1 presents the converter limits of the converters in the system.

Table A.1: Tuning parameters in CIGRE DCS1 test system

Control mode	K_p	T_i
V_{dc}	8	0.00367
P_{ac}	0	0.0303
V_{ac}	1	0.1
Q_{ac}	0	0.0303

Table A.2: Base data for the converters

Parameters	**Cm-A1**	**Cm-C1**	**Cm-B2**	**Cm-B3**	**Cm-F1**
$V_{dc,base}$ [kV]	400	400	400	400	400
$P_{ac,base}$ [MW]	800	800	800	800	800
$V_{ac,base}$ [kV]	380	145	380	380	145
$Q_{ac,base}$ [MVAr]	800	800	800	800	800

A.3 Behavior of the reference line during a step

When conducting a step in power or voltage in the set-point of the converter, the droop slope will move accordingly. The behaviour of the droop slopes can be seen in Figure A.2. In Figure A.2a, the controller is in P_{ac} control and a step in the power is conducted. This means that the slope should move in the x-direction. Figure A.2b depicts the behaviour of the slope when having a power step in DC voltage droop control. The new reference slope will only move in x-direction because of the power step, but the new reference will be moving up in both y-direction and x-direction. In Figure A.2c the controller is in V_{dc} control with a step being made in the voltage direction. This means that the new reference slope will only move in y-direction.

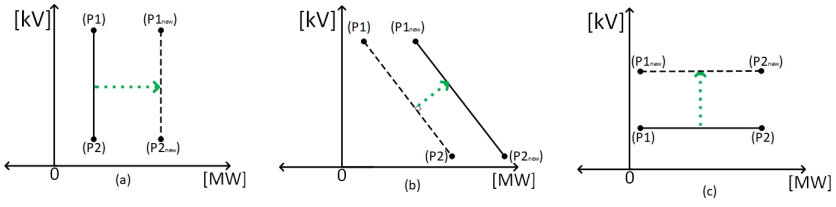

Figure A.2: Figure (a) shows power step in P_{ac} control, (b) illustrates a step in power for P_{ac} control and (c) depicts a step in voltage for V_{dc} control

A.4 Determining the Tuning Procedure for the Proposed Tuning Gains

Figure A.3 shows the logic for how the proposed tuning parameters are obtained

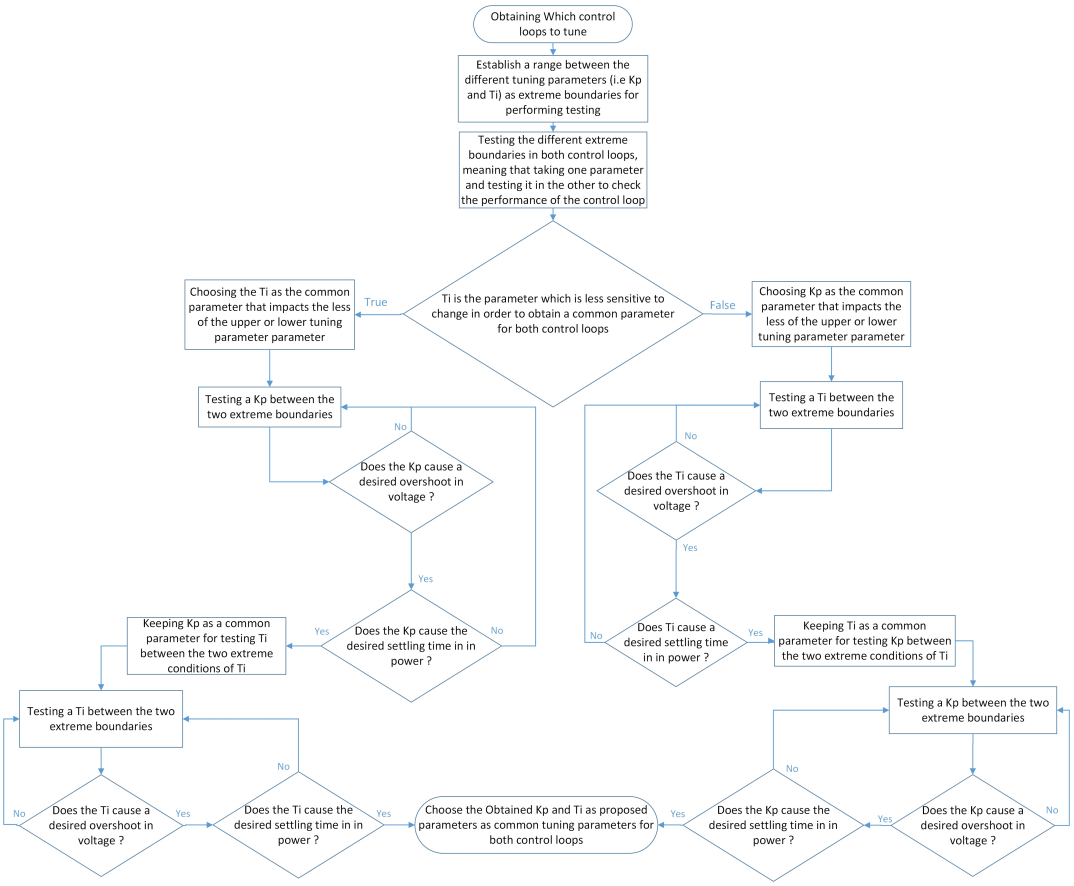

Figure A.3: A logic which present how the proposed tuning parameters are obtained

The procedure is based on obtaining which parameter to tune first and how to start, first the two extremes for both T_i and K_p, meaning that the K_p of each control loops are set as the extremes, then both control modes are tested to find which parameter that can be set as a fixed value to obtain the other. meaning that if T_i is the parameter that will give less contribution to change with in the system response, this value will be chosen. T_i is then set to obtain a proposed K_p, then when K_p satisfy the given conditions for both voltage and power, the K_p will be set as a fixed value in order to the proposed parameter T_i. However if K_p was the parameter that was influencing the response in both control loops, K_p will be chosen as first fixed value and the procedure will be almost identical, just that first K_p will be fixed to obtain the proposed T_i, then the proposed T_i will be set as a fixed value to obtain a proposed K_p.

A.5 Test Systems

As previously mentioned the 1-D upper level control scheme developed by CIGRE will be used as a reference for the operation and performance of the 2-D controller. The 1-D upper level control structure is depicted in Figure 3.3. The tuning parameters used in the 1-D control are calculated in [16] and are shown in Table A.1.

Figure A.4 depicts a general schematic of the CIGRE PtP-system.

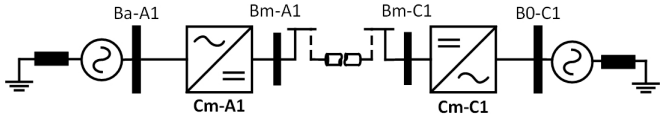

Figure A.4: HVDC point to point system used for simulations

The 2-D controller will also be tested for the use in a 3-terminal MTDC system as depicted in Figure A.5.

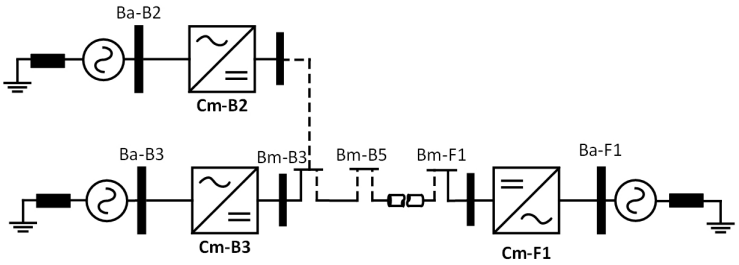

Figure A.5: 3-terminal MTDC system used for simulations

A.6 System Design

A.6.1 Droop slope

Figure A.6 shows the response when conducting a step in the droop slope including scenario 4. In scenario 4 the proposed tuning parameters K_p=1.5 and T_i=0.0303 are implemented in the 1-D controller.

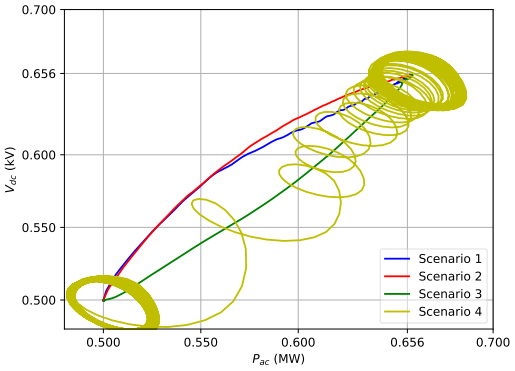

Figure A.6: Response when conducting a step in the droop slope including scenario 4

It can be seen that the response of the 1-D controller when using the proposed tuning parameters becomes unstable.

A.6.2 q-axis Control Loop

When comparing the cascaded 1-D, q-axis control loop with the cascaded version of the 2-D controller q-axis loop, as depicted in Figure A.7 two 2-D error blocks has to be implemented. One 2-D error block will control V_{ac} producing a Q_{ac} reference to the other 2-D error block operating in Q_{ac} control. This means that also two PI controllers have to be implemented in the cascaded 2-D system. Another factor is that if the outer controller (2-D block V_{ac}) is operating in droop control, it will create a reference for the Q_{ac} 2-D controller. In this case the droop will just operate as a constant Q_{ac} controller with a changing reference according to what the system needs at all times. Figure A.7 (a) shows the cascaded 2-D control structure, while Figure A.7 (b) shows the non-cascaded 2-D control structure.

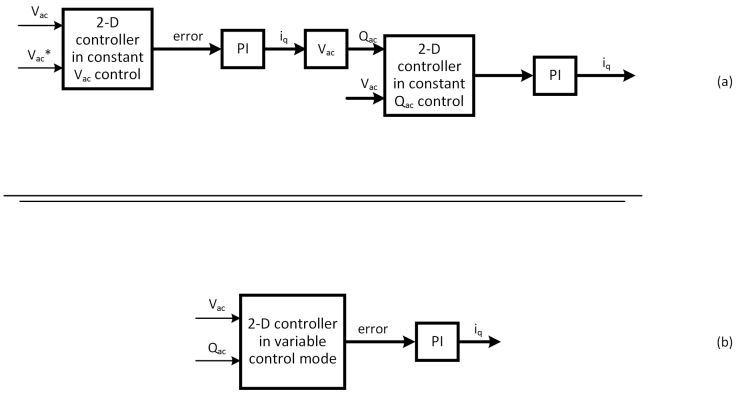

Figure A.7: Cascaded 2-D control structure(a) and non cascaded 2-D control structure (b)

As depicted when transforming the system from a non-cascaded system (b) to the CIGRE AC control system (a), more PI controllers need to be added. As well as when there exists

a cascaded control system, the PI in the outer loop will need to be slower than the inner, forcing the complete systems total response time to increase. Since a cascaded 2-D structure will remove the advantages of the non-cascaded 2-D controller, it will not be used in this thesis. This means that the non cascaded 1-D q-axis loop shown in Figure 4.26 (b) will be used to compare the q-axis loop of the 1-D and 2-D controllers.

A.6.3 Trial and error tuning for the q-axis loop

Figure A.8 displays the response in , Figure A.9 show the results from the trial and error tuning.

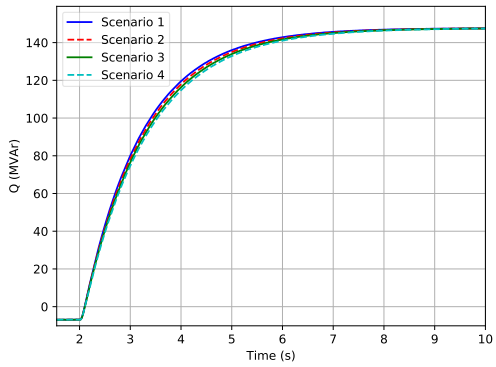

Figure A.8: Vac control Ti sweep Qac response

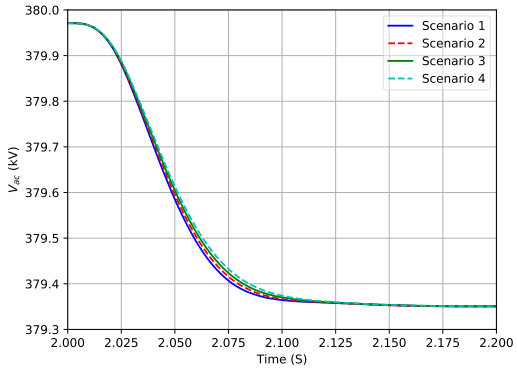

Figure A.9: Q_{ac} control T_i sweep AC response

Appendix B

Calculations

This appendix presents how the the 2D-error calculations has been performed, followed by a FORTRAN code, which was implemented the PSCAD/EMTDC software.

B.1 Calculating the Error

Equations used for calculation of the 2 dimensional error in the "2D-error block". The calculation of the error is based on the dot product vector calculation for vector a and b, which is placed perpendicular on each other. Figure B.1 shows a representation of two vectors perpendicular to each other.

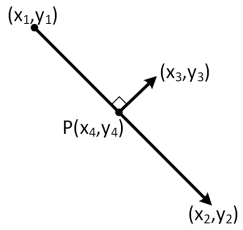

Figure B.1: vectors in a two dimensional plane

The projected point (x,y) on the vector from (x_1, y_1) to (x_2, y_2), where the vector (x,y) is perpendicular to (x_3, y_3) can be calculated by

$$\vec{a} \cdot \vec{b} = |a||b| \cos \phi = 0 \tag{B.1}$$

where:

$$\begin{aligned} a &= \langle x_2 - x_1, y_2 - y_1 \rangle \\ b &= \langle (x_2 - x_1) \cdot t + x_1 - x_3, (y_2 - y_1) \cdot t + y_1 - y_3 \rangle \end{aligned} \tag{B.2}$$

By inserting Equation B.2 into Equation B.1 it can be obtained that

$$\vec{a} \cdot \vec{b} = a_x \cdot b_x + a_y \cdot b_y = 0 \tag{B.3}$$

where subscript represent and that "t" which represent where on the line the point is projected, becomes

$$t = \frac{(x_3 - x_1)(x_2 - x_1) + (y_3 - y_1)(y_2 - y_1)}{(x_2 - x_1)^2 + (y_2 - y_1)^2} \tag{B.4}$$

The projected point will then be:

$$P = ((x_2 - x_1)t + x_1), ((y_2 - y_1)t + y_1) \tag{B.5}$$

Where

$$P_x = x_4 = (x_2 - x_1)t + x_1$$
$$P_y = y_4 = (y_2 - y_1)t + y_1$$

This will form the new vector which is perpendicular to the vector to be:

$$\vec{e} = \langle x_3 - x_4, y_3 - y_4 \rangle \tag{B.6}$$

The new vector $\vec{e}$ represents the error which is then going to be sent to the PI, the length of this vector will represent the length of the vector between (x,y) and (x_3, y_3) and will therefore become

$$|e| = \sqrt{e_x^2 + e_y^2} \tag{B.7}$$

B.2 Implementation of Errorblock in PSCAD

To make the error block suitable for use in HVDC systems with different converter ratings the ratings are put as parameters in the script. This is done in order to make it more easy to change the parameters if the ratings of the systems are changed. Table B.1 shows the names of the parameters.

Table B.1: System data for the 2-D error block

Name	**P**/V_{dc}	**Q**/V_{ac}
Pbase	800	800
DeltaP	1600	800
Vbase	400	380
DeltaV	40	38
Vlower	380	361
Pupper	800	400

Pbase is the base power/reactive power of the converter, while DeltaP is the total range of the active and reactive power. Vbase is the base voltage (dc or ac) of the system, and Delta V is the range of the maximum and minimum voltage limits. Vlower and Pupper are set as parameters in order to normalize the active,reactive power and the ac, and dc voltages.

B.2.1 Script in FORTRAN

Here the 2-D block script is presented, where it contain the logic for calculating a two-dimensional error, which is sent to a PI controller.

```
#LOCAL REAL, xlim1, xlim2, ylim1, ylim2, p1x, p2x, pPac, p1y, p2y, pVdc,
#LOCAL REAL, zx, zy, t, px, py, avvikx, avviky, avvik_d
xlim1=0.0
xlim2=1.0
ylim1=1.0
ylim2=0.0
p1x=($x1 + $UpperPlim )/($DeltaPac)
p2x=($x2 + $UpperPlim )/($DeltaPac)
pPac =($Pac + $UpperPlim)/($DeltaPac)
p1y=($y1-$LowerVdclim)/$DeltaVdc
p2y=($y2-$LowerVdclim)/$DeltaVdc
pVdc=($Vdc-$LowerVdclim)/$DeltaVdc
zx=p2x-p1x
zy=p2y-p1y
t=(((pPac-p1x)*zx)+((pVdc-p1y)*zy))/((zx**2)+(zy**2))
px=zx*t+p1x
py=zy*t+p1y
IF (px .LT. xlim1) THEN
dx=xlim1-px
ELSE IF (px .GT. xlim2) THEN
dx=xlim2-px
END IF
IF (py .GT. ylim1) THEN
dy=ylim1-py
ELSE IF (py .LT. ylim2) THEN
dy=ylim2-py
END IF
avvikx=0
avviky=0
IF (pVdc .GT. ylim1) THEN
avviky = pVdc-ylim1
ELSE IF (pVdc .LT. ylim2) THEN
avviky = pVdc-ylim2
ELSE IF (pPac .LT. xlim1) THEN
avvikx = pPac-xlim1
ELSE IF (pPac .GT. xlim2) THEN
avvikx = pPac-xlim2
ELSE
avvikx = pPac-px
avviky = pVdc-py
END IF
avvikxpu=(avvikx*$DeltaPac)/$Pbase
avvikypu=(avviky*$DeltaVdc)/$Vdcbase
```

```
avvik_d=SQRT((avvikxpu**2)+(avvikypu**2))
$Error=avvik_d
IF ($Dcontrol.GT.0.5) THEN
IF((avvikxpu .GE. -1.0E-6).AND.(avvikypu .GE. -1.0E-6)) THEN
$Error=avvik_d*(-1.0)
END IF
ELSE
IF ((avvikxpu .GE. -1.0E-6).AND.(avvikypu.LE. 1.0E-6)) THEN
$Error=avvik_d*(-1.0)
END IF
END IF
```

B.3 DC Resistance Calculation

In this section, the procedure of calculating the cable resistance R_{dc} is presented. Figure 4.8 illustrates a configuration for testing the system in P-control. R_{dc} is calculated in the following steps:

First the DC current I_{dc} needs to be obtained and it can be calculated by:

$$\begin{aligned} I_{dc} &= \frac{P_{ac}}{Vdc} \\ &= \frac{800MW}{400kV} \\ &= 2kA \end{aligned} \tag{B.8}$$

From this the cable resistance can be obtained: To calculate the value of R_{dc}, by using Ohms law:

$$\begin{aligned} R_{dctot} &= \frac{\Delta V}{I_{dc}} \\ &\frac{20kV}{2kA} \\ &= 10\Omega \end{aligned} \tag{B.9}$$

Since R_{dctot} represents the total resistance in the DC cables, it has to be divided by two since the DC connection is cructed with two cable connections (i.e a positive and a negative terminal). Hence

$$\begin{aligned} R_{dc} &= \frac{R_{dctot}}{2} \\ &= 5\Omega \end{aligned} \tag{B.10}$$

B.3.1 SCR for the CIGRE test system

To evaluate the strength of the AC network in the CIGRE DSC1/DSC2 test systems the SCR ratio was calculated. Figure B.2 depicts the AC system with a single-line diagram of

the equivalent network. In order to check the q-axis loop, the SCR will be changed to create a system with a weak grid to evaluate response of the 1-D and 2-D controller during different grid conditions. The impedance parameters are given in Table B.2

The SCR can be calculated by Equation B.11

$$SCR = \frac{V_{sLL}^2}{z_s P_{dc}} \tag{B.11}$$

Here, P_{dc} represents the rated power of the converter. z_s is the impedance of the closest bus that has a fixed AC voltage during normal conditions and it can take maximum rated converter power. V_{sLL} is the line to line rms voltage of the AC grid [11].

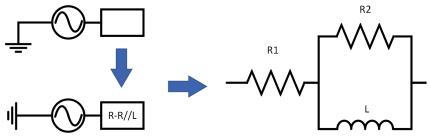

Figure B.2: Equivalent network representation, modeled as an R-R//L impedance

component	value
R1	0.48 [Ω]
R2	1000 [Ω]
L	0.015 [H]

Table B.2: Original CIGRE test system parameters [6]

By using Equation B.11 and the equation for calculating the total impedance (Z_{tot}) of a series plus parallel connection of the R-R//L circuit represented in Figure B.2 the equation for Z_s becomes

$$Z_{tot} = R1 + X_{paralell} = R1 + \frac{R2 \cdot jX_L}{R2 + jX_L} \tag{B.12}$$

By inserting the values from Table B.2 into Equation B.12:

$$\begin{aligned} Z_s &= 0.48 + 4.712\angle 89.73 \\ &\cong 0.48 + j4.712 \\ &= 4.736\angle 5.82 \end{aligned} \tag{B.13}$$

Which give an X/R ratio of

$$\frac{X}{R} \cong 10 \tag{B.14}$$

Implementing the value obtained from Equation B.13 into Equation B.11:

$$SCR = \frac{V_{sLL}^2}{Z_s \cdot P_{dc}} = 38.11$$

An SCR = 38.11 will equal to a strong network, referring to Table 4.13 which implies "no operating problems".

B.3.2 Transforming an equivalent network to match a weak grid

In order to make the AC grid for simulation a weak grid, Equation B.11 is used. P_{dc} of the system is 800 MW, V_{sLL} is 380 kV. Since it is wanted to have a weak AC grid to see the response of the AC control loops, Equation B.11 is rearranged and the impedance of the weak grid can be calculated as shown below:

$$z_s = \frac{V_{sLL}^2}{SCR \cdot P_{dc}} = \frac{(380 \cdot 10^3)^2[V^2]}{2.5 \cdot 800 \cdot 10^6[W]} = 72.2\Omega$$

To get an $Z_s = 72.2$, a reverse calculation of Equation B.12 has to be done where

$$72.2 = \sqrt{R^2 + X_{Parallel}^2}$$

by implementing Equation B.14 into the equation

$$R1 = 7.18[\Omega]$$
$$X_{parallel} = 71.8[\Omega]$$

From this it is possible to find both L and R2 in the parallel connection, by knowing that the angle should be kept constant as the same system, when downgrading the system to a weak grid, the same $\frac{X}{R}$-ratio for the strong system should be kept when reducing the strength within the grid. $\frac{X}{R}$-ratio becomes

$$\frac{X_{L-old}}{R_{old}} = \frac{2\pi * 50 * 0.015}{1000} = 4.712 * 10^{-3}$$

The reactance for the parallel connection can be calculated from:

$$L = \frac{X_{parallel}}{\omega} = 0.2285[H] \tag{B.15}$$

From this, a new R2 can be calculated since it is known that the angle ratio of both systems has to be equal, which will give:

$$\frac{\omega L}{R2} = 4.712 \cdot 10^{-3}$$

Giving:

$$R2 = 15244[\Omega]$$

As a summary of the calculated values is presented in Table B.3

component	value
Z_s	72.2 [Ω]
R1	7.18 [Ω]
R2	15244 [Ω]
L	0.2285 [H]

Table B.3: SCR = 2.5 system parameters

B.3.3 Transforming an equivalent network to match an almost strong grid

A SCR = 4 has been chosen in order to create an equivalent impedance which will represent a almost weak grid. The term "almost strong grid" has been mentioned to represent a system which is strong, but at the same time it is close to a weak system. The procedure is identical that of the example shown in subsection B.3.2, hence table values for this system is presented in Table B.4

component	value
SCR	4.0 [-]
Z_s	45.125 [Ω]
R1	4.49 [Ω]
$X_{Paralell}$	44.9 [Ω]
R2	9528.86 [Ω]
L	0.1429 [H]

Table B.4: Almost weak grid system parameters

B.3.4 SCR ratios for different AC grids

To perform the various it is a good idea to understand the strength of each equivalent AC grids which is connected to the converter that is preseted. The method used for the calculation is presented in subsection B.3.1 and the SCR values along with the parameters for calculation is given in the Table B.5

Converter station	Cm-A1	Cm-C1	Cm-F1	Cm-B2	Cm-B3
SCR [-]	38.11	12	4.77	38.3	25.5
V_{s_LL} [kV]	380	230	380	380	380
P_{dc} [MW]	800	800	800	800	1200
$Z_s[\Omega]$	4.736	5.51	4.77	4.71	4.71
R1 [Ω]	0.48	0.333	0.333	0.48	0.48
$X_{Paralell}[\Omega]$	4.71	5.5	5.5	4.71	4.71
R2 [Ω]	1000	1000	1000	1000	1000
L [H]	0.015	0.0175	0.0175	0.015	0.015

Table B.5: AC grid HVDC system parameters

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