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Performance Assessment of A 3L-ANPC Based on GaN Technology

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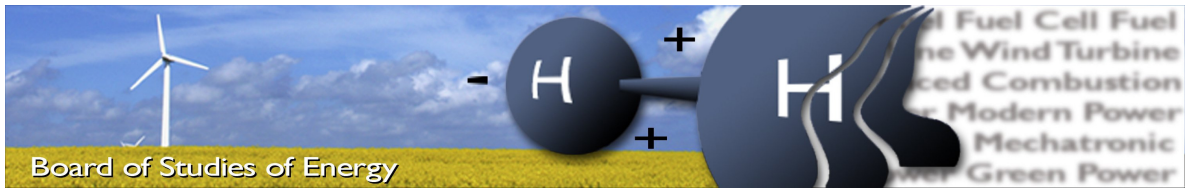

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SYNOPSIS:

Nowadays, the power electronics converter design is challenged with a request of highly efficient and compact converters for various applications, especially photovoltaic (PV) systems. To tackle this, the research community and the industry have almost fully exploited the Silicon technology, leading to the development of new power transistors. The GaN HEMTs can be promising power devices to replace the traditional IGBTs and MOSFETs. Therefore, the performances of converters based on such a technology should be assessed to validate their effectiveness in terms of efficiency and compactness. Moreover, among the available converter topologies , the performance of the three-level NPC family can be enhanced with the GaN HEMTs. In light of the above, in this thesis, the performance of a GaN-based three-level Active Neutral Point Clamped (3L-ANPC) converter is assessed in terms of power losses, volume impact of passive components, and output distortions for both single-phase and three-phase operation. Simulations and experiments have been performed.

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Preface

This thesis report summarizes the work that has been carried out during the 9^{th} and 10^{th} semesters of the Master of Science in Power Electronics and Drives. The project proposal "Performance assessment of a 3L-ANPC based on GaN technology" has been chosen by the author among the long-thesis project proposal available in Fall 2017. The project topic is the continuation of a project started by Prof. Francesco Iannuzzo and Assoc. Prof. Yongheng Yang in cooperation with Dr. Emre Gurpinar from Nottingham University, in 2016.

The project deals with the performance assessment of a GaN-based three-level ANPC inverter, in order to validate the concept of introducing the WBG in renewable-based Power Electronic converters. Given the topic, the work on the project has been relevant in the education of the author. Indeed, it has been in general an important experience from several point of view. Starting with the unique opportunity of working with the relatively new devices such as the GaN transistors, the thesis allowed the author to strength his knowledge in:

- Three-level inverter operation and its modulation strategies;
- GaN-based converter challenges and issues;
- Converter characterization;
- Cooling system design;
- Common-mode analysis;
- EMI identification.

In conclusion, the author would like to give a special thanks to the supervisors Prof. Francesco Iannuzzo and Assoc. Prof. Yongheng Yang for their guidance, availability and support during all the work. An additional thanks is addressed to Assoc.

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Nomenclature

Acronyms Specification

Acronym	Specification
ANPC	Active Neutral Point Clamped
CMTI	Common Mode Transient Immunity
CMV	Common Mode Voltage
DSP	Digital Signal Processor
EMI	Electro-Magnetic Interference
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FFT	Fast Fourier Transform
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
NPC	Proportional Integral
PCB	Printed Circuit Board
RMS	Root Mean Squared
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
TIM	Thermal Interface Material
VSVM	Virtual Space Vector Modulation
WBG	Wide Band-Gap

Symbols Specification

Symbol	Specification	Unit
P	Active power	W
V	Voltage	V
B	Flux density	T
T	Temperature	$^{\circ}C$
I	Current	A
Z	Impedance	Ω
L	Inductance	H
R	Resistance	Ω
C	Capacitance	F
d	Duty Cycle	-
f	Frequency	Hz
T	Period	s
m	Modulation index	-
ω	Angular frequency	$^{rad}/_{s}$
Vol	Volume	m^3

Contents

Part I

Chapter 1

Introduction

1.1 Background

The increasing demand of clean energy sources has led to a high penetration of renewable energy sources in the past years. Among various renewable sources, the most popular ones are solar and wind power, with a percentage of 15% and 24% in respect to the total renewable energy production, respectively [1]. The harmonious integration of these clean energy sources with the existing power systems, poses new challenges that involve the distribution and generation systems. Indeed, a more distributed generation system requires a dedicated grid management along with an intelligent power conversion. Nowadays, these challenges are being overcome with an intensive use of Power Electronics (**PE**) converters, which should be flexible, controllable, efficient, and reliable.

A typical grid-connected system is exemplified in Fig. 1.1. The core part of such a system is the power electronic converter, which is required to provide bidirectional power flow. The conversion should ideally comply the following requirements:

- The output current Total Harmonic Distortion (**THD**) should be kept as low as possible, under a limit according to the standard;
- The conversion should be efficient, lowering the converter losses due to switching and conduction behaviours;
- The converter should be reliable (i.e. long lifetime) to maintain a low maintenance rate.

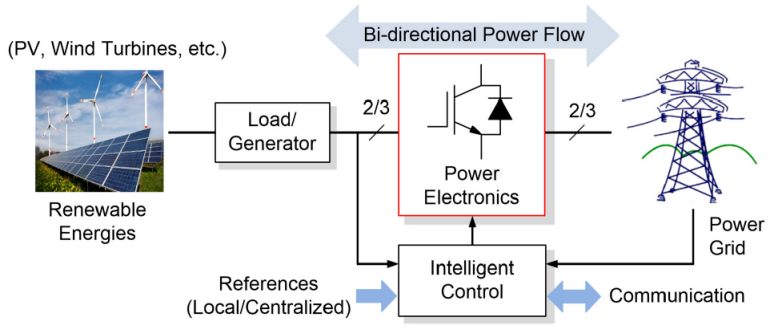


Fig. 1.1: Typical scheme of a renewable power generation system [2].

As known, the higher the switching frequency is, the lower the THD will be. Consequently, the output filter size can be smaller. Therefore, to fulfil the first requirement, a high switching frequency will be desirable. However, a high switching frequency, certainly increases the losses due to the non-ideal switching of the transistors, and this conflicts with the first requirement, leading to a trade-off between the two. Overcoming this issue has led to an extensive exploitation of the traditional Silicon (**Si**) technology.

A step forward has been moved with the introduction of Wide-Band Gap (**WBG**) materials, which show superior characteristics compared to Si [3]. However, there are not many commercial WBG power devices available on the market. The Silicon Carbide (**SiC**) and the Gallium Nitride (**GaN**) and their characteristics, compared to the Si ones, are shown in Fig. 1.2. It is revealed that the key advantage of the WBG devices is the high electron velocity, which allows to greatly increase the turn-on and turn-off times. As known, the dissipated power due to switching is proportional to the sum of the turn-on and turn-off times. Thus, a reduction of the switching count can effectively improve the efficiency of the system while increasing the switching frequency for a better THD. In addition, the WBG power devices can withstand higher voltages and, in particular, the SiC power switches, can operate at a higher junction temperature.

For low voltage applications such as residential photovoltaic (**PV**) systems and high-speed motor drives, the best candidates are the normally-off GaN High Electron Mobility Transistor (**HEMT**). They have been released on market by Panasonic and GaN Systems Inc. with a 600 V and 650 V blocking voltage, respectively [4]. Such devices have been used to implement synchronous DC/DC converters, three-phase inverters, and resonant converters. In the literature, excellent results in term of switching losses and conduction losses were observed with the application of GaN HEMT devices [5]-[6]. In [5], a three-phase inverter based on the GaN technology has achieved a 99.3%

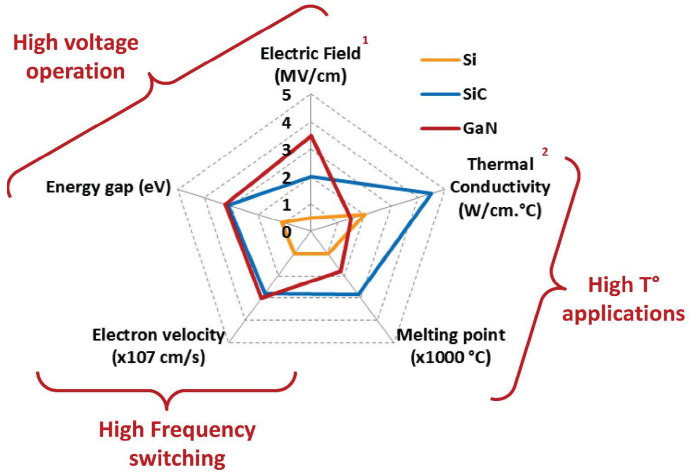


Fig. 1.2: Schematic representation of the characteristics of the WBG devices compared to the traditional Si devices [3].

efficiency at 900 W and 16 kHz switching frequency. In the same range of efficiency, in [6], a peak efficiency of 99.2% at 1.4 kW output power has been reached. From the reliability point of view, a reliability-driven comparison between Si-based and GaN-based PV inverters has been shown in [7]. Other results in term of trade-off among switching frequency, filter design, and efficiency have been shown in [8].

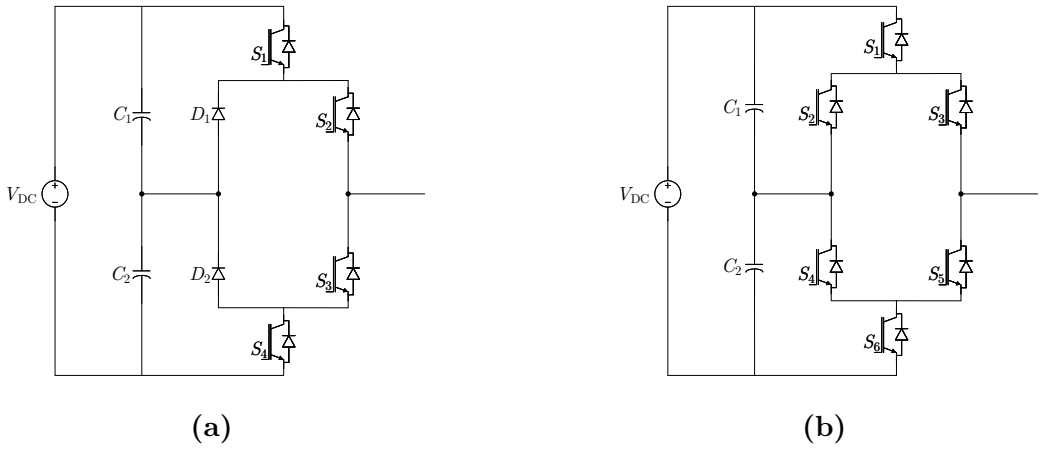
A concern when designing converters with GaN-based devices is about the voltage stress across the switching devices. The voltage stress affects the switching losses, the reliability of the converter, and the EMI generation. Moreover, the maximum blocking voltage obtainable nowadays with the GaN technology is 650 V, and thus it is necessary to lower the DC-link voltage accordingly. For three-phase grid-connected PV systems, the desirable DC-link voltage should be above 650 V for the connection to the 230 V line-voltage grid. This would lead the converter to work at the boundaries of its Self Operating Area (**SOA**) in terms of voltage stress. A solution might be to connect two GaN transistors in series, in order to divide the drain-source voltage by a half, and consequently reduce the stress on each device. In two-level inverters, it means that eight switches should be adopted in each phase, leading to a higher cost and a higher complexity of the gate driver circuitry. As to be discussed later, the employment of multi-level topologies can easily solve this problem, and also introducing several additional benefits.

Besides the properties of the WBG, different topologies have been investigated to maximize the performance of such transistors combining the benefits of topologies and modulation techniques. Although the outstanding performances of the WBG can be

attained with the traditional two-level inverters, some more benefits can be obtained by means of multi-level topologies. For instance, the three-level Neutral Point Clamped (**3L-NPC**) is one of the most widespread multi-level convertertes in renewable applications, because of the good trade-off between the benefits and the number of active devices. Compared to the two-level inverters, the main advantages of the three-level NPC inverter are [9]:

- Reduced voltage stresses across the switching devices, as the DC link voltage is divided between two switches connected in series;
- The multi-level output voltage allows to reduce the filtering requirements, since the harmonic content is lower;
- Besides the reduced stress, the lower voltage across the transistor reduces the losses, increasing the converter efficiency;
- In the case of PV applications, the safety requirements related to the leakage current can be satisfied without the isolation transformer though modulation.

An improved topology of the traditional three-level NPC inverter is the three-level Active Neutral Point Clamped (**3L-ANPC**). In such a topology, the diodes are replaced with active switches, significantly reducing the switching losses when compared with the NPC. Moreover, the active control of the neutral point allows some important features like the DC-link capacitor voltage balancing, Common Mode Voltage (**CMV**) reduction and stress balancing among the switches. The 3L-NPC and the 3L-ANPC are shown in Fig. 1.3



(a) **(b)**

Fig. 1.3: Three-level inverter phase-leg schematic: *(a)* the Neutral Point Clamped (**NPC**) topology and *(b)* the Active Neutral Point Clamped (**ANPC**) inverter.

This thesis is based on the work proposed in [4] and [10], where a 3L-ANPC inverter for PV applications has been designed using 650 V GaN HEMT devices with a maximum current of 30 A. This means that such an inverter can deliver a maximum power of 5 kW per single-phase cell and three cells can be stacked to form a 15 kW three-phase system. The scope of this thesis is to integrate the work already done on this topic with a performance assessment in both single- and three-phase operation mode. The details of the project motivations, the limitation, and the outline are given in the next section.

1.2 Problem Formulation and Thesis Objectives

As aforementioned, the work related to the proposed GaN-based 3L-ANPC inverter has been shown in [4] and [10], which is mainly focused on the switching performances of such an inverter. This thesis aims to integrate the previous work with an analysis of the performances from different viewpoints:

- Quantification of conduction and switching losses;
- Volume occupied by passive components;
- Stressess on active devices;
- Evaluation of the output distortion.

These performances are relevant to assess whether the WBG-based three-level inverter is a viable way to achieve the goals stated in the previous section. Therefore, the motivation or the main research question of this thesis can be summarized as:

"Can GaN transistors improve the performances of a 3L-ANPC grid-connected PV application? And from what aspects?"

To answer this question, the performances need to be evaluated considering the output power, switching frequency, and modulation strategy. To give an indication of how the output power affects the performances, different power levels from 1 kW to the maximum power of 5 kW are explored. Moreover, the switching frequency has been varied from 50 kHz to 200 kHz, especially to evaluate its impact on the output filter volume and the device stresses. Different modulation techniques have been explored only in the three-phase operation mode, since in the previous work the single-phase modulation has been thoroughly analysed.

In addition to the performance evaluation, the EMI aspect is also crucial in this application. Clearly, the high switching speed of the GaN-based transistors introduces challenges in the converter design. These issues should be addressed due to the high $^{di}/_{dt}$ and $^{dv}/_{dt}$, and thus the parasitic inductance and capacitance can create problems, respectively. As known, these parasitics are present everywhere in the converter PCB and more efforts should be devoted. For this reason, the 3L-ANPC inverter has been specifically designed in order to reduce the parasitics of the PCB layout. In [10], the design of the ultra-low inductance commutation loop was presented along with experimental results. In the same paper, a simulation analysis has led to the conclusion that EMI issues appear because of the capacitive coupling between the inner layers of the four-layers PCB. It is worth to mention that the layer stack of the PCB examined in that case was thin. This has led to a high capacitance stressed by the high $^{dv}/_{dt}$, introducing cross-talking between the logical circuits of the overlapped devices. For this reason, a different layer stack has to be employed and the presence of the EMI has to be verified. If still exist, different solutions should be investigated. Another EMI issue is related to the introduction of the cooling system. As it will be explained later, the combination of a thermal interface material and the metallic heatinks introduces a capacitive coupling among the switches which allows the circulation of the common-mode current. Therefore, the impact of this potential EMI source should be investigated through simulations.

1.3 Project limitations

The analysis presented is based on the scenario of a PV system with a maximum power of 5 kW and 700 V DC-link voltage connected to the low-voltage (LV) grid (230 V_{RMS}, 50 Hz) that can be either a single- or three-phase. Such a system is depicted in Fig. 1.4 and the main characteristics are listed in Table 1.1.

$\mathbf{P_{out,max}}$	5 kW single-phase and 15 kW three-phase
$\mathbf{V_{DC}}$	700 V
$\mathbf{V_{line}}$	230 V_{RMS}
$\mathbf{f_{line}}$	50 Hz
$\mathbf{f_{sw}}$	50 kHz to 200 kHz

Tab. 1.1: Nominal parameters of the considered inverter.

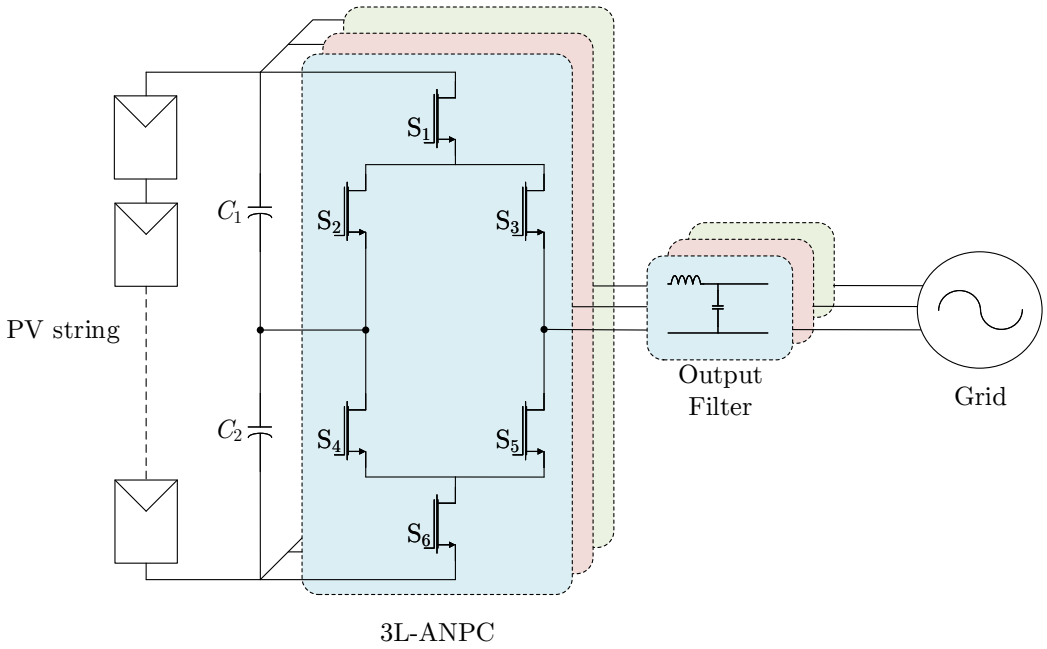


Fig. 1.4: Overall scheme of the considered hypothetical scenario.

Despite the scenario, the system has been simplified in order to carry out the analysis in the most effective way focusing on the performance:

- The grid has been replaced with a resistive load connected through an LC filter;

- Since the system is operating in open-loop, the control has not been considered;
- An ideal DC source is assumed.

The answer to the main research question of this thesis has been shaped along the chapters of this thesis. It is divided in two major parts: 1) a theoretical and introductory part and 2) the performance assessment. In the first part, after an introduction of the GaN HEMT characteristics, the 3L-ANPC is introduced in both single-phase and three-phase operation modes along with the relative modulation techniques. In the second part, the hardware is described and the switching performance is validated by simulations and experiments. The volume impact of the passive components is analysed in Chapter 5. Afterwards, the results are shown and the models are validated partly with experimental tests. The thesis is then closed by concluding remarks and further research perspectives.

Chapter 2

GaN-based Three-level ANPC Converter

The aim of this chapter is to overview the three-level converter, starting with the Neutral Point Clamped (**3L-NPC**) converter and then discussing the Active NPC (**3L-ANPC**) converter. Firstly the GaN-based power transistors are briefly analysed in support of the thesis motivation. Then, the 3L-ANPC is analysed in its single-phase mode, and then the analysis is extended to the three-phase version. The focus is put on the general topology aspects with different modulation strategies.

2.1 Background

The 3L-NPC inverter was introduced by Nabae *et al.* in 1981 [11]. The 3L-NPC is able to provide three voltage levels by the connection to the mid-point of the DC-link. Such a connection is provided by two diodes, as shown in Fig. 2.1. Because of the multilevel output voltage, the 3L-NPC presents better performances when compared to the traditional two-level converters, e.g., low power losses, low THD, and small output filter. The advantages and drawbacks of the two- and three-level inverters are summarized in Table 2.1. The three output voltage levels are denoted by P, 0 and N; the current paths for each state are shown in Fig. 2.2. To obtain such an output, the switches can have 12 different states, as summarized in Table 2.2, where "0" and "1" indicate the *on* and *off* state, respectively.

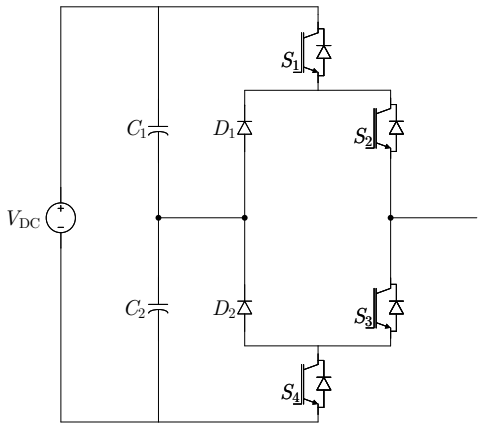


Fig. 2.1: Single-phase leg of a 3L-NPC inverter.

	Two-level	**Three-level**
Gate driver	+	–
PWM algorithms	+	–
DC Link voltage balancing	N/A	– –
Output filter size	–	++
THD	–	++
Switches blocking voltage	– –	++
Losses (switching and conduction)	– –	++

Tab. 2.1: Comparison between two-level and three-level inverters. The positive aspects are graded with a "+" while the negative one with a "-".

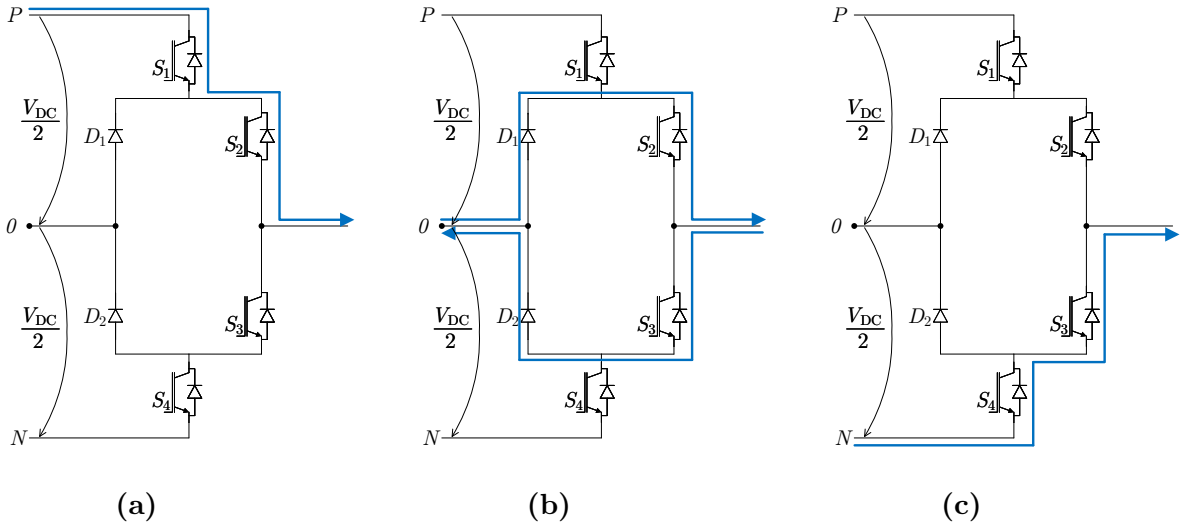


Fig. 2.2: Three output voltage states: *(a)* the "P" state, *(b)* the "0" state and *(c)* the "N" state. The blue arrows indicate the current path.

	S_1	S_2	S_3	S_4
State "P"	1	1	0	0
State "0"	0	1	1	0
State "N"	0	0	1	1

Tab. 2.2: Switch states for a single-phase leg of the NPC.

These states can be generated through the Pulse-Width Modulation (**PWM**), which can be chosen among several options. For the single-phase operation, a modulation strategy can be the Sinusoidal PWM (**SPWM**), while for the three-phase NPC, available modulation techniques can be the classical carrier-based SPWM strategies or more sophisticated Space Vector Modulation (**SVM**) strategies (and their variants).

The unequal distribution of power losses is the main structural drawback of the NPC [12], which leads to a complicated thermal management and a poor exploitation of the full performances of the employed transistors because of the uneven stress distribution [13]. To overcome this issue, the neutral point clamping diodes (e.g. D_1 and D_2 in Fig. 2.1) can be replaced with active power switches [13]. The resultant circuit is depicted in Fig. 2.3.

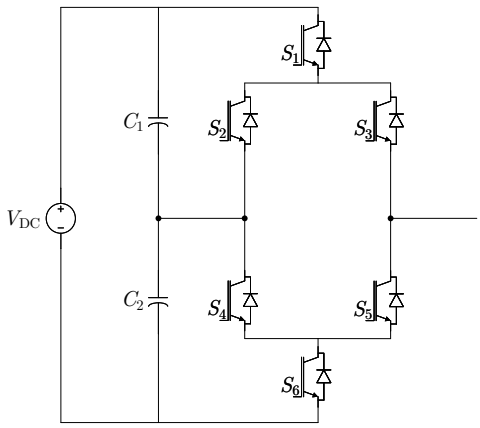


Fig. 2.3: Single-phase leg of a 3L-ANPC inverter.

The adoption of two more active power switches introduces 18 more states in contrast to the 3L-NPC ones. The additional states increase the degrees of freedom to develop modulation techniques. In Table 2.3, 36 states are described using the same logic as for the NPC states. It can be observed that there are more possibilities to generate zero states.

	S_1	S_2	S_3	S_4	S_5	S_6
State "P"	1	0	1	1	0	0
State "0U2"	0	1	1	0	0	0
State "0U1"	0	1	1	0	0	1
State "0L1"	1	0	0	1	1	0
State "0L2"	0	0	0	1	1	0
State "N"	0	1	0	0	1	1

Tab. 2.3: Switching states of the 3L-ANPC inverter.

The commutation between the presented states is defined with the modulation technique. In the following sections, the modulation strategy for the single-phase and three-phase versions are described. First, the GaN power devices are briefly introduced.

2.2 Gallium Nitride Power Devices

As mentioned, the Si-based transistors have reached their technological maturity and, for the coming challenges of PE converters, a new efficient and cost-effective technology is needed. Among the possible solutions, the WBG technologies are promising since they allow increasing the efficiency even with a higher switching frequency and operating junction temperature. In Table 2.4, the main characteristics of the WBG technology (i.e., SiC and GaN) are compared with the Si technology. The high electron-mobility of the GaN and the band-gap indicate that the GaN transistor can allow high switching speeds, while the critical field reveals that the GaN transistor can be more compact compared to a Si-based transistor of the same voltage rating. Another advantage of GaN transistors is the low on-state resistance. As shown in Fig. 2.4, the GaN crystal may theoretically allow to build switches with a very low on resistance for a crystal layer of a mm^2 [14].

In addition to the mentioned favourable aspects of the GaN-based HEMTs, they present several disadvantage and challenges for their integration in power converters. From a thermal management point of view, the low thermal conductivity of the GaN crystal does not allow to efficiently dissipate the heat generated by the losses. For this reason, the maximum power delivered with such transistors is highly limited by this drawback. The challenges of the integration in existing power converter topologies are related to the EMI. Actually, the high switching speed is the root cause of

Parameter	Unit	Silicon	GaN	SiC
Band Gap	eV	1.12	3.39	3.26
Critical Field	MV/cm	0.23	3.3	2.2
Electron mobility	$cm^2/V \cdot s$	1400	1500	950
Permittivity		11.8	9	9.7
Thermal conductivity	$W/cm \cdot K$	1.5	1.3	3.8

Tab. 2.4: Material properties of Silicon, Gallium Nitride (GaN) and Silicon Carbide (SiC) [14].

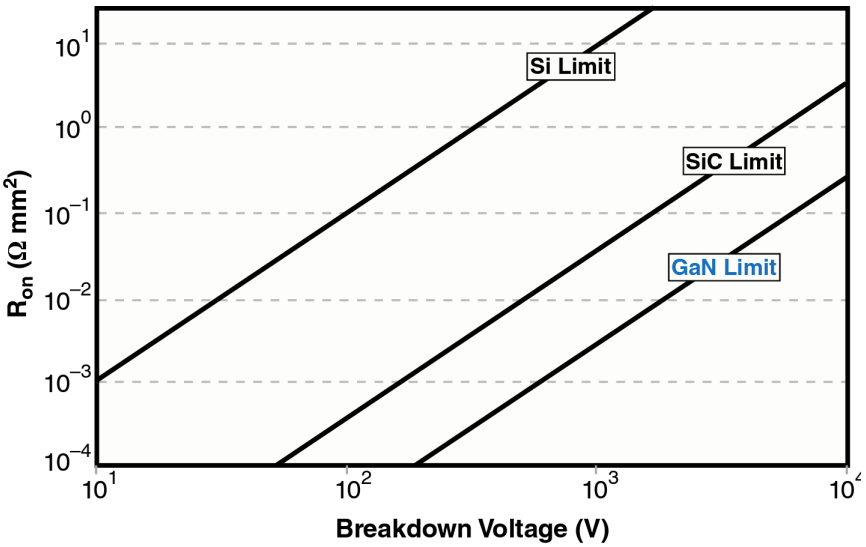


Fig. 2.4: Theoretical on-state resistance per mm^2 of crystal. [14].

several undesirable effects such as drain-source voltage overshoots and gate driver instability. The cause of the former is based on the existence of parasitic inductances in the transistor packaging and the PCB copper trace. From the packaging point of view, the GaN HEMT producers have introduced several Surface-Mounted Device (**SMD**) solution, allowing to reach stray inductances in the order of the nano-Henry [15]. Regarding the PCB, it is a main challenge for the PCB designers, who have to carefully reduce the copper traces length and exploit effects such as field cancellation between conductors which carry opposite currents. On the gate driver side, since the threshold voltage is very low compared to Si and SiC transistors, the layout design and the component selection should be carefully designed. Additionally, the high switching speed enhances the well-known Miller effect during turn-on and turn-off procedures. To overcome these issues, separated turn-on and off resistors combined with low-impedance paths for the Miller current have to be introduced in the gate driver design. Lastly,

the GaN HEMTs are capable of the reverse conduction for gate-source voltages below the threshold. Although this "diode-like" behaviour allows to avoid the introduction of anti-parallel diodes and practically cancels the reverse recovery effects, the GaN transistor have significant conduction losses in the reverse condition. Moreover, these losses increase as the gate-voltage goes below the threshold. Therefore, using bipolar gate drivers to avoid the Miller turn-on effect can effectively increase the conduction losses during dead-time in half-bridge applications [14].

2.3 Modulation Schemes

2.3.1 Single-phase modulation scheme

Given the benefits of the NPC inverter, it is worth to analyse and explore the possibilities of this topology applied to the single-phase mode of operation. Although the 3L-NPC inverter has been originally developed for three-phase systems to handle high power, it is also applicable for single-phase systems. In [16], a half-bridge solution has been tested in single-phase applications. According to [16], even the number of active switches is higher than that of the two-level converters, this transformerless solution can reduce cost and weight in filters and increase the overall efficiency when WBG transistors are used. On the other hand, since it is a half-bridge, the required DC-link voltage must be at least twice the grid voltage amplitude.

In [16], a novel modulation technique is proposed for a single-phase SiC-based 3L-ANPC inverter. With the proposed technique, the switching states are arranged in order to minimize the switching and conduction losses. The four output states given in Table 2.3 are shown in Fig. 2.5, where the two zero-states are shown. During the positive half of the reference voltage, the output is connected to the positive rail of the DC-link through S_1, which is modulated, and S_3 is kept on during all the positive states. The output current flows from the DC-link to the load through the two series switches. Although S_4 is turned on during this state, no current is flowing through it. The reason why S_4 is on is to keep the drain-source voltage of S_5 and S_6 clamped to $\frac{V_{DC}}{2}$. The state "0" while S_1 is off is provided by switching S_2, S_5, S_3 and S_4 on. This arrangement creates a parallel path for the current that is flowing from the neutral point to the load. This method ensures low conduction losses during the zero states, since the current is shared between two series-connected GaN HEMTs. In a similar manner, the negative-current zero state is provided. Regarding the negative half of the

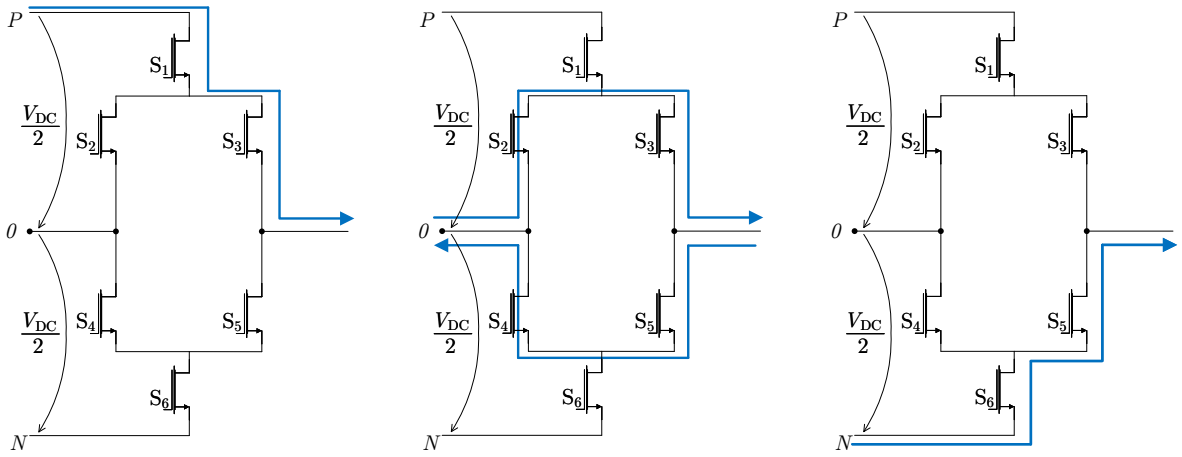


Fig. 2.5: Three output voltage states: *(a)* the "P" state, *(b)* the "0" state and *(c)* the "N" state. The blue arrows indicate the current path.

reference voltage ("N" state), the switches involved are S_6 and S_5, following the same logic of the "P" state.

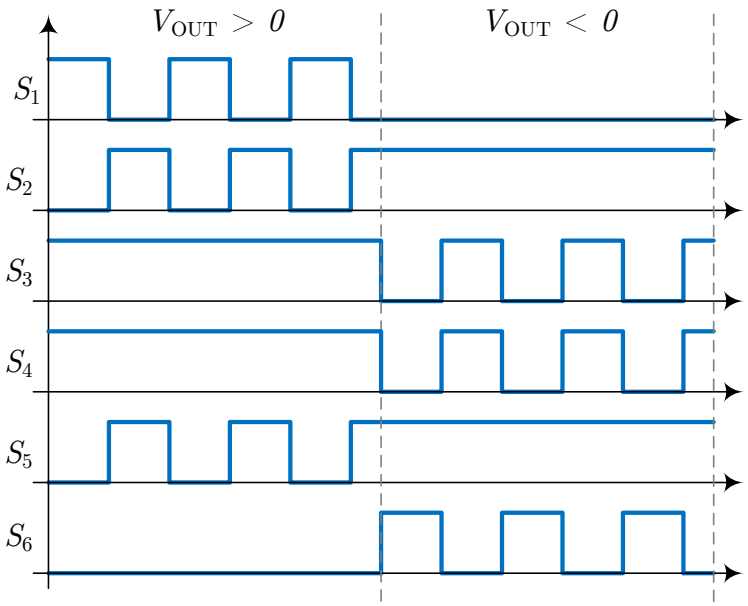


Fig. 2.6: Gate signals of a single-phase leg following the method proposed in [16].

During a switching period, three devices are commutated. This results in low

switching losses, since two devices are turned on during the Zero Voltage Switching (**ZVS**). Taking the positive state as example, S_3 and S_4 are kept ON during the half cycle of the reference voltage, while S_2 and S_5 are turned ON while the drain-source voltage is zero. Therefore, this modulation strategy achieves low switching and conduction losses due to the ZVS and the parallel conduction, respectively.

Based on the mentioned assumptions, the only two switches directly related to the PWM generation are S_1 and S_6 for the positive and negative half-cycle respectively. These PWM signals are generated using a carrier-based SPWM, as shown in Fig. 2.7. The peculiarity of this strategy is the use of two level-shifted carrier waveforms. The comparison of the positive half of the reference voltage with the positive carrier generates the gate signal of the positive-rail switch S_1. In a similar way, the negative half-cycle is compared with the negative carrier, and then the gate signal for S_6 is generated. This strategy can be easily implemented on digital micro-controllers. In fact, once the signals for S_1 and S_6 are obtained, the signals for the inner switches (from S_2 to S_5) can be generated following a logical-negation scheme. The switches S_2 and S_5 are the negation of the signal of S_1, while S_3 and S_4 are the negation of S_6. This method allows to simplify the hardware for the dead-time and the gate signal for the whole phase-leg. The boolean logic is summarized in Table 2.5.

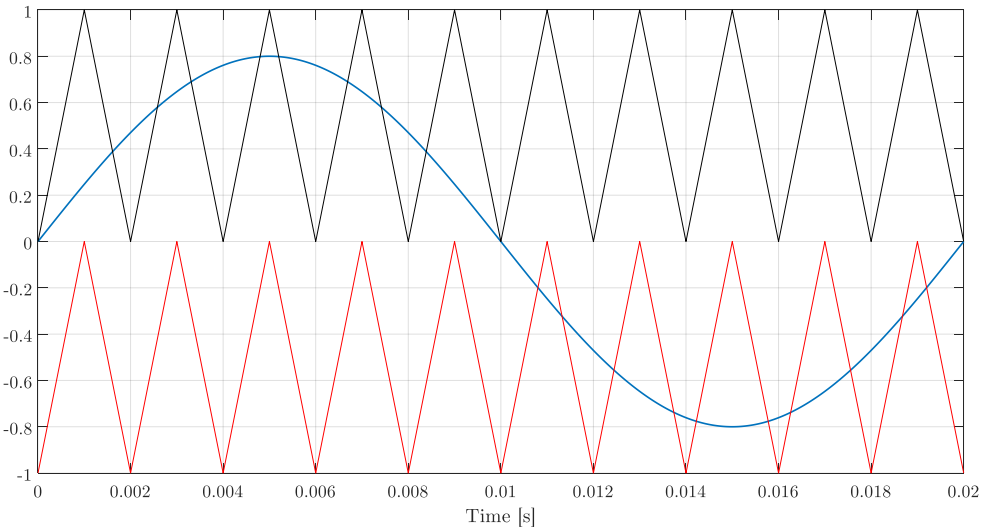


Fig. 2.7: Level-shifted SPWM strategy. The black waveform is the positive carrier while the red one is the negative one. The blue waveform is the reference voltage.

$\mathbf{S_1}$	PWM
$\mathbf{S_2}$	$\overline{S_1}$
$\mathbf{S_3}$	$\overline{S_6}$
$\mathbf{S_4}$	$\overline{S_6}$
$\mathbf{S_5}$	$\overline{S_1}$
$\mathbf{S_6}$	PWM

Tab. 2.5: Gate signals generation logic.

2.3.2 Three-phase modulation schemes

Compared to the single-phase configuration, the three-phase configuration gives the possibility to employ different modulation techniques in order to reduce the switching losses, increase the exploitation of the DC-link voltage, and improve the voltage balancing of the neutral point. The latter is a well known drawback of the three-level inverter. To overcome this issue, several solutions are available nowadays. One is to add extra hardware to the circuit, however increasing cost and complexity. [17], [18]. The other solution is related to the modulation strategy.

In the literature, several PWM strategies have been proposed such as SPWM, Selective Harmonic Elimination PWM (**SHEPWM**), and SVM. The latter, compared to SPWM and SHEPWM, maintains the benefits as:

- Small ripple in the output current;
- High DC voltage exploitation;
- Easy implementation on micro-controllers.

Hence, the SVM has gained more attention and several improvements have been added to the original SVM strategy in order to overcome the high common mode voltages and neutral-point (**NP**) balancing. A SVM control strategy to balance the NP has been presented for a five-level NPC inverter in [19] and [20], which can be extended to the 3L-NPC as well. These two methods are based on the Nearest Three Vectors (**NTV**) principle, which is that are not capable of balancing the NP under a high modulation index and low power factor. To overcome this issue, a new Space Vector Diagram (**SVD**) can be drawn by means of virtual space vectors. These virtual vectors are a linear combination of real vectors of the SVD and are capable of controlling the NP

under various modulation indexes and power factors. Such a modulation strategy, called Virtual Space Vector Modulation (**VSVM**), has been presented in [21], where it has been shown that this method is capable of balancing the NP but with high harmonics. In [22], the same modulation has been improved with an optimized harmonic performance. The SVM and VSVM are implemented and compared in terms of the NP balancing, DC-link voltage ripple, and output harmonic distortion.

Space Vector Modulation

The space vector concept is illustrated in Fig. 2.8. There are 27 vectors divided into large, medium, small, and zero vectors. The large vectors create six sections, from A to F. Each section can be further divided into four triangular regions, i.e., A0 to A3. The reference vector V_{ref} is characterized by its magnitude and phase. V_{ref} can be synthesised in each switching period by the nearest three vectors. For example, if the vector V_{ref} is in the triangle A2, the reference vector will be synthesized by the vectors V_{M0}, V_{S0} and V_Z corresponding to the states P0N, P00 and (000). The four types of

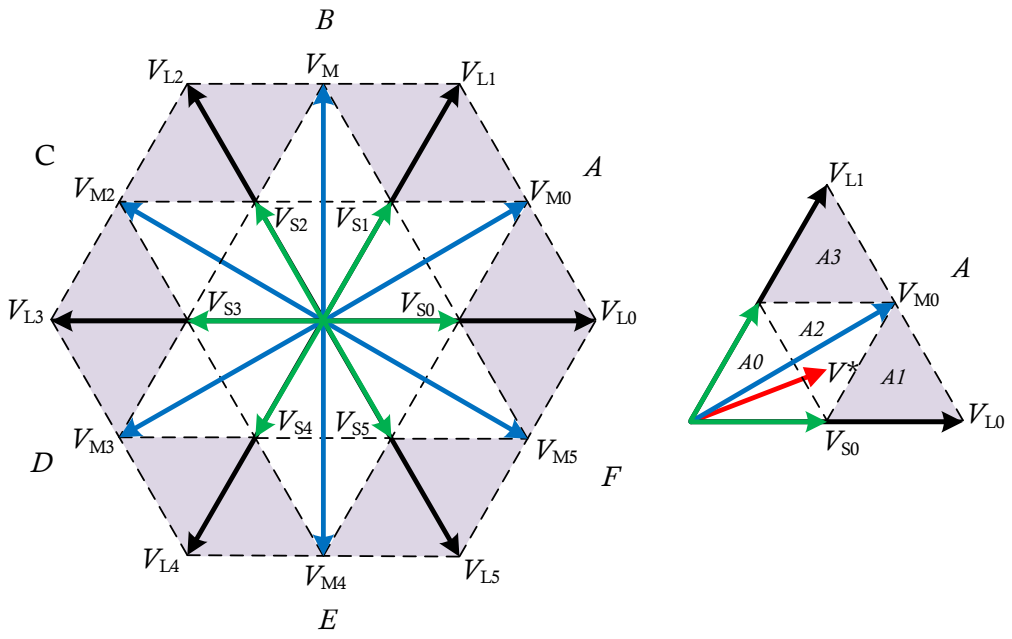


Fig. 2.8: Space vector diagram of the SVM applied to a 3L-ANPC. On the right, details of Section A.

vectors have different effects on the NP balancing [23]:

- Since they connect each phase to the positive or negative rail, the large (V_{Lx}) and zero (V_Z) vectors do not affect the NP;
- The medium vectors (V_{Mx}) connect one phase to the NP, and therefore they affect the NP balancing;
- The small vectors (V_{Sx}) have the same function of the medium vectors. They are divided into negative and positive small vectors.

Clearly, both the medium and the small vectors affect the NP. The medium vectors have a stronger impact when the modulation index is high, and the small vectors that have more impacts when the modulation index is low. The effect of the negative and positive small vectors is opposite, and therefore the NP balancing is based on the manipulation of a pair of small vectors. Since not in all the regions are present two pairs of small vectors, the NP balancing can be obtained only under certain modulation indexes and reference angles (i.e., white coloured region) [23]. The VSVM, as to be explained later, introduces another pair of small vectors in each region [23].

In this thesis, the SVM is generated using the zero sequence voltage injection. As discussed in [24] for a two-level inverter, the injection of a third-harmonic triangular wave in the reference voltage, achieves the same result as if the look-up table SVM is implemented. This allows to greatly reduce the computational burden when compared with the look-up table-based implementation. To generate the voltage reference, the zero sequence voltage is calculated as:

$$v_{zs}^{*} = -[(1 - 2k_0) + k_0 V_{max} + (1 - k_0) V_{min}] \tag{2.1}$$

where V_{max} and V_{min} are the maximum and minimum of the three-phase set of reference voltages. The constant k_0 represents how the zero vector is divided at the end and the beginning of the switching period. For a symmetrical SVM, the factor k_0 is selected as 0.5. Then, 2.1 can be simplified as:

$$v_{zs}^{*} = -0.5 \cdot (V_{max} + V_{min}) \tag{2.2}$$

The duty cycles for the three phases are then calculated with the following equations:

$$v_{a}^{*} = v_a + v_{zs}^{*} \tag{2.3}$$

$$v_b^* = v_b + v_{zs}^* \tag{2.4}$$

$$v_c* = v_c + v_{zs}^* \tag{2.5}$$

To obtain the gate signals for the switches S_1 and S_2, the calculated references are compared with two level-shifted carrier waveforms, as shown in Fig. 2.9.

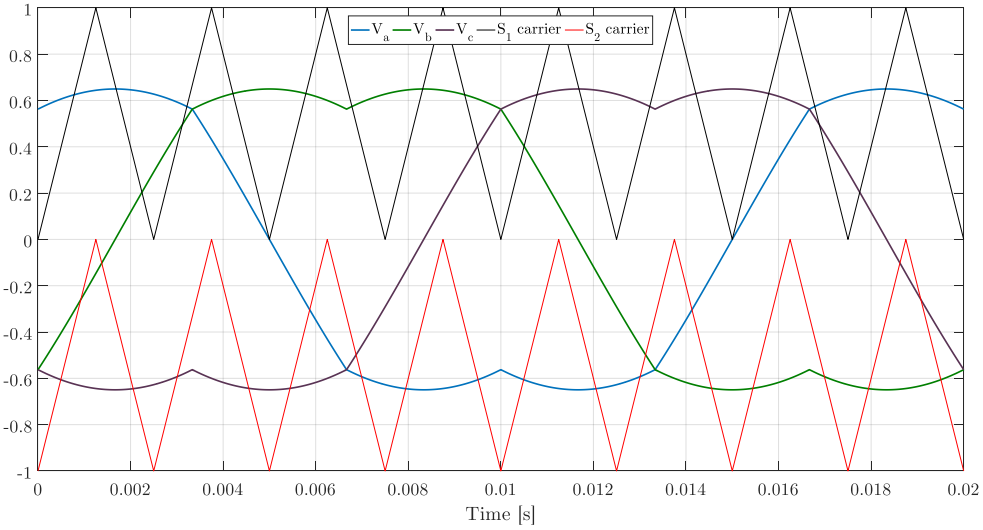


Fig. 2.9: Result of the zero sequence injection for the carrier-based PWM.

Virtual Space Vector Modulation

The issue related to the NP unbalancing relies on the reduction of the NP current. The average of the NP current over one switching period must be zero in order balance the neutral point. Seen from the SVM SVD, it is known that over one switching period, the amount of the NP current introduced by the small vectors is not enough to compensate the amount introduced by the medium vectors. To achieve the reduction of the NP current, a new set of vectors are introduced in [21]. These vectors are the linear combination of certain vectors. Such vectors are shown in Fig. 2.10 for the first sextant of the SVD. The virtual vectors V_{Z0}, V_{ZSx}, V_{ZMx} and V_{ZLx} can guarantee that the average NP current is zero over one switching period. This definition is supported by the following [21]:

- V_{Z0} corresponds to the switching state 000, where the NP current $i_0 = 0$;
- V_{ZSx} is obtained by combining two switching states that generate the same amplitude of i_0 but have an opposite sign. This cancels out the average current over one switching period;
- V_{ZMx} is the result of the combination of three switching states whose total contribution to i_0 is equal to zero ($i_a + i_b + i_c = 0$);
- V_{ZLx} is composed by the combination of states that define V_{Lx} with $i_0 = 0$.

In [21], it has been demonstrated that this modulation is capable of controlling the NP voltage but with high harmonic distortions. An improvement is introduced in [22], where an optimization problem has been solved to reduce the THD while controlling the NP voltage. If one takes the first sextant of the three-level inverter SVD, it can

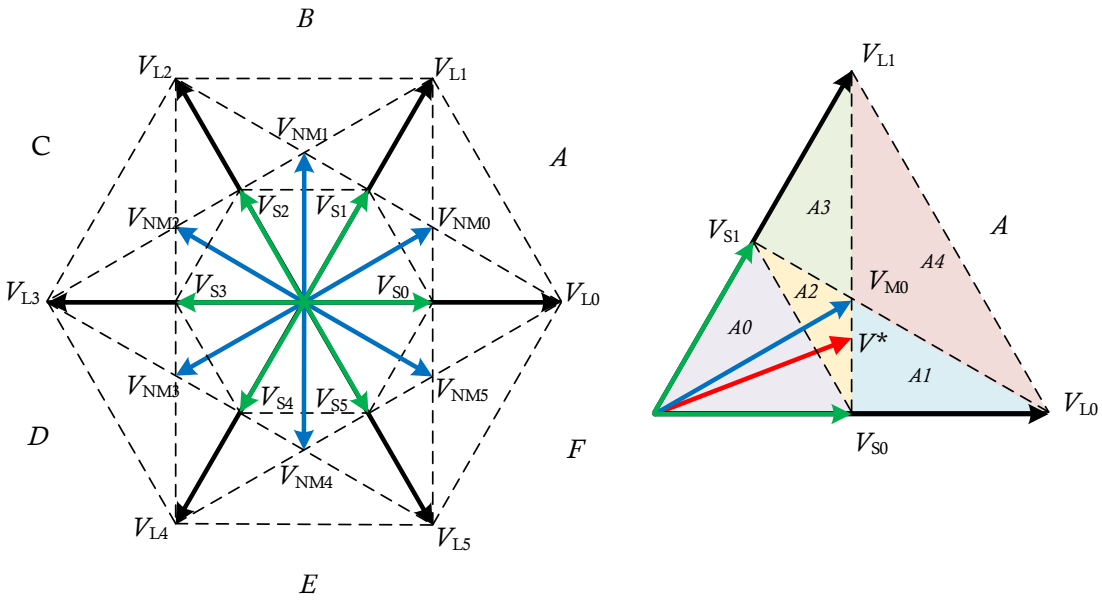


Fig. 2.10: Space vector diagram of the generalized VSVM applied to a 3L-ANPC. On the right, details of Section A.

be noticed that it contains all the modulation techniques based on the Nearest-Three-Vector (**NTV**) principle. As shown in Fig. 2.10, the vectors can be expressed as a

function of the set of coefficients r_x and the switching states of the 3L-ANPC, which are defined in Eq.s (2.6-2.9)for the Section A:

$$V_{S0} = r_1 \cdot V_{POO} + r_2 \cdot V_{ONN} \tag{2.6}$$

$$V_{S2} = r_3 \cdot V_{PPO} + r_4 \cdot V_{OON} \tag{2.7}$$

$$V_{M0} = r_5 \cdot V_{ONN} + r_6 \cdot V_{PON} + r_7 \cdot V_{PPO} \tag{2.8}$$

Depending on the value of such coefficients, the NTV modulations can be obtained:

- if $r_5 = r_7 = 0$, the NTV is obtained;
- in case of $r_1 = r_2 = r_3 = r_4 = \frac{1}{2}$ and $r_5 = r_6 = r_7 = \frac{1}{3}$, the NVTV is obtained.

With this generalization, an optimization problem can be written in order to calculate the optimal set of coefficients $r_{x,k}$. The objective function is to minimize the output voltage distortion, while the constraints are the conditions in which the NP current is zero. In the literature, this problem is set and solved using a state-space model of the three-level NPC in the *dq0* reference frame. In such a reference frame, six optimal duty cycles are obtained. The three duty ratios d_{pd}, d_{pq} and d_{p0} are related to the connection of the positive rail of the DC-link to the output. In the same way, d_{nd}, d_{nq} and d_{n0} are the duty ratios of the connection of the negative rail to the output. These duty ratios can be easily transformed into the *abc* frame using the inverse Park inverse transformation and then used for modulation.

The solution of the optimization problem gives the following equations, which depend on the fundamental angle $\theta = \omega t$, the power factor ϕ, the modulation index m and a factor K:

$$d_{pq} = -K \cdot sin(3\theta) \tag{2.9}$$

$$d_{pd} = tan(\phi) \cdot d_{pq} + m/\sqrt{2} \tag{2.10}$$

$$d_{nd} = d_{pd} - \sqrt{2} \cdot m \tag{2.11}$$

$$d_{nq} = d_{pq} \tag{2.12}$$

$$\begin{cases} d_{p0} = \sqrt{2} \cdot (-d_{pd} \cdot cos(\theta + 2\pi/3) + d_{pq} \cdot sin(\theta + 2\pi/3)), & \theta \leq 2\pi/3 \\ d_{p0} = \sqrt{2} \cdot (-d_{pd} \cdot cos(\theta) + d_{pq} \cdot sin(\theta)), & 2\pi/3 < \theta \leq 4\pi/3 \\ d_{p0} = \sqrt{2} \cdot (-d_{pd} \cdot cos(\theta - 2\pi/3) + d_{pq} \cdot sin(\theta - 2\pi/3)), & \theta > 4\pi/3 \end{cases} \tag{2.13}$$

$$\begin{cases} d_{n0} = \sqrt{2} \cdot (-d_{nd} \cdot cos(\theta) + d_{nq} \cdot sin(\theta)), & \theta \leq \pi/3, \theta > 5\pi/3 \\ d_{n0} = \sqrt{2} \cdot (-d_{nd} \cdot cos(\theta - 2\pi/3) + d_{nq} \cdot sin(\theta - 2\pi/3)), & \pi/3 < \theta \leq \pi \\ d_{n0} = \sqrt{2} \cdot (-d_{nd} \cdot cos(\theta + 2\pi/3) + d_{nq} \cdot sin(\theta + 2\pi/3)), & \pi < \theta \leq 5\pi/3 \end{cases} \tag{2.14}$$

Among the above equations, the crucial aspect is the definition of the factor K. It is limited between [0, K_{max}], where K_{max} is the limit above which the duty ratios go above 1, i.e., over-modulation. The optimum value of K is directly related to the distortion of the output voltage. In [22], it is analytically expressed as a function of the modulation index and the power factor. The analytical expression gives a plane where three regions can be identified, in which various K values are valid. This plane is shown in Fig. 2.11, where the regions A, B and C are highlighted. Given that the boundaries are defined by

$$\begin{aligned} m_{AB} &= 0.5 \\ m_{BC} &= 0.75 + 0.213 \cdot [1 - sin(|\phi|)] \end{aligned}$$

and then, K can be calculated as:

$$K = 0.25 \cdot m^2 \cdot cos(\phi), \text{ in region A} \tag{2.15}$$

$$K = 0.25 \cdot m \cdot \left(1 - \frac{|\phi|}{\pi/2}\right), \text{ in region B} \tag{2.16}$$

$$K = \frac{1.53 \cdot (1 - m) \cdot [1 - sin(|\phi|)]}{|\phi| + 0.24}, \text{ in region C} \tag{2.17}$$

As mentioned previouslt, the optimization leads to a general solution of the NTV modulations. This generalization relies on the factor K, if $K = 0$, the regular VSVM is implemented. In Fig. 2.12, the duty cycles for phase-a with $K = 0$ and the optimized K for $m = 0.7$ and $\phi = 30°$ are plotted. In this case, since the references for the positive and negative connection are already calculated, the carriers are phase-shifted in the same range between [0, -1]. To compare the modulation strategies, the Fast Fourier Transform (**FFT**) results of the 3L-ANPC converter with the three modulation strategies are shown in Figs. 2.13, 2.14 and 2.15 for SVM, VSVM and Optimized VSVM respectively. The THD have been calculated. It can be observed that the improved VSVM is the best option since it gives a THD comparable with the SVM along with the reduced voltage oscillations on the input voltage.

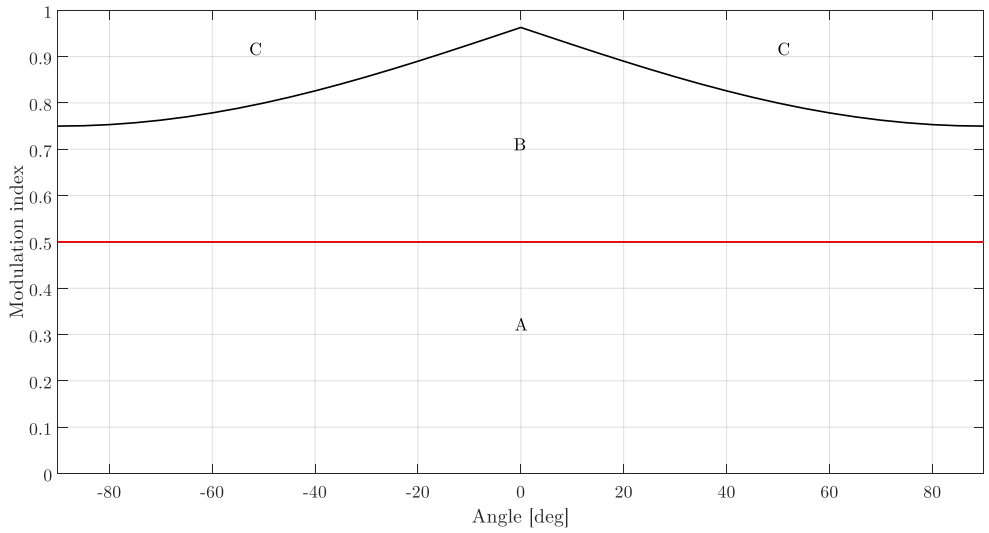


Fig. 2.11: Regions for the approximation for the optimum value of K.

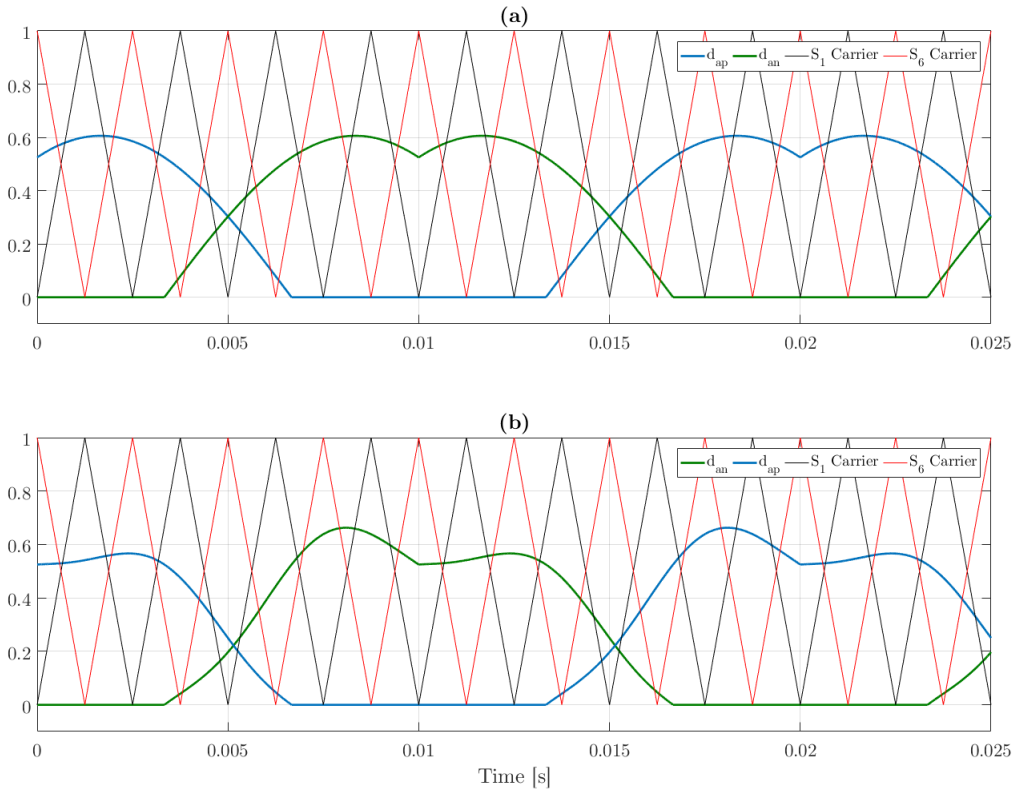


Fig. 2.12: Duty cycles obtained in the case of $m = 0.7$ and $\phi = 30°$: *(a)* the VSVM and *(b)* the optimized VSVM.

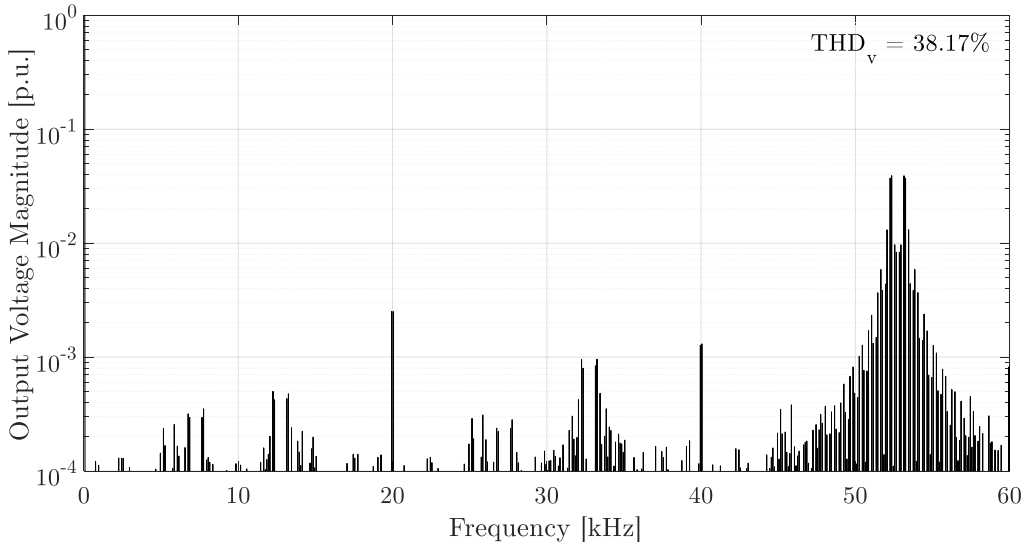


Fig. 2.13: FFT analysis of the output voltage when the SVM strategy is adopted.

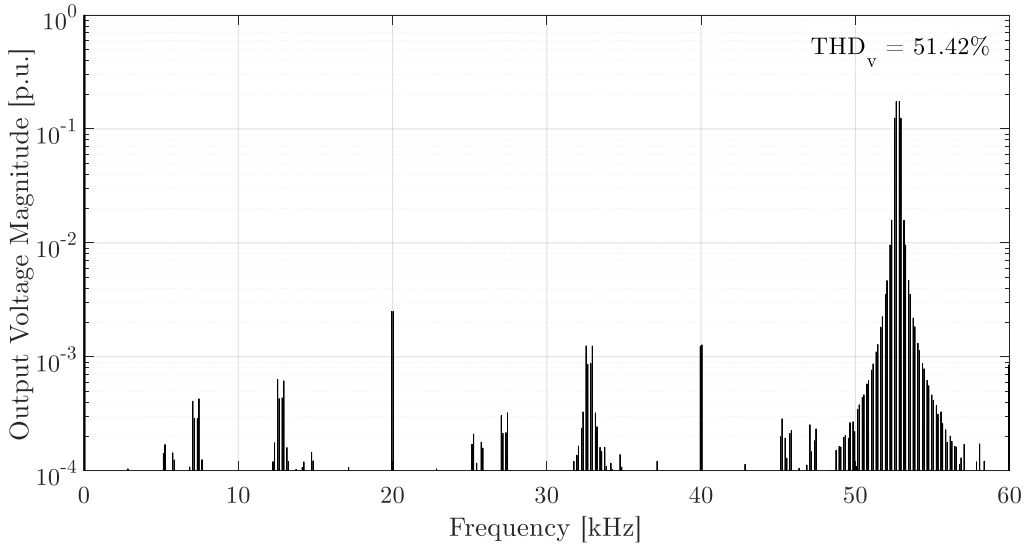


Fig. 2.14: FFT analysis of the output voltage when the VSVM strategy is adopted.

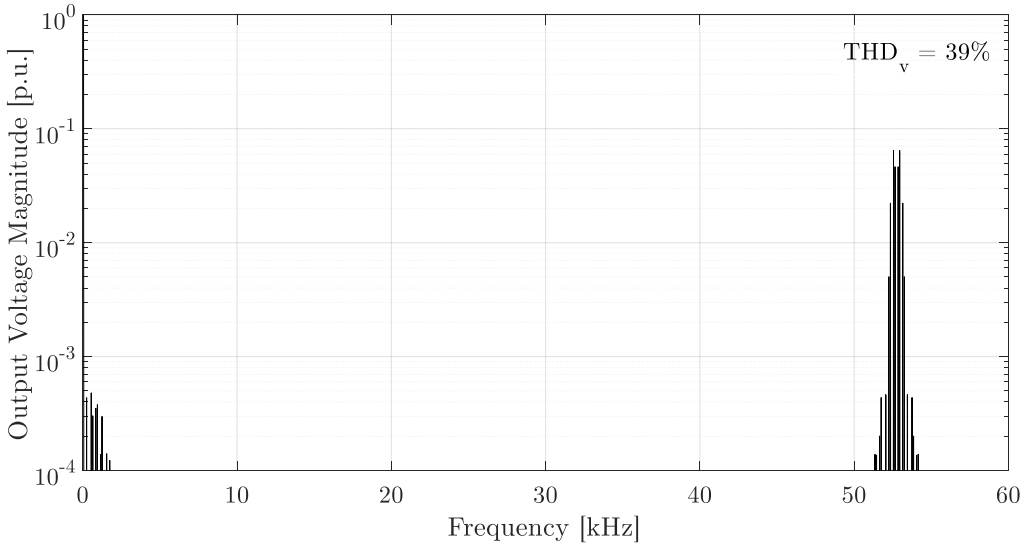


Fig. 2.15: FFT analysis of the output voltage when the optimized VSVM strategy is adopted.

Part II

Chapter 3

Hardware System and Preliminary Evaluation

In the pages of this chapter, the design of the passive elements such as DC-link capacitor and output filter is proposed with the aim of estimate the total converter's volume. Afterwards, the converter is analysed in all its part: gate driver, commutation loop and switching performance with common-mode analysis as well.

3.1 Cooling System Design

The conduction and switching losses are responsible of the junction temperature increasing in the power devices. The temperature is the most critical aspect that has to be considered in designing power converters since it has a strong impact on the lifetime and the performance of the power devices. Besides leading to immediate and irreversible device failure if the maximum temperature is exceeded, the junction temperature is the principal stressor in long-term device failure. Indeed, according to the Coffin-Manson law, the number of cycles to failure is dependent on the mean junction temperature over one cycle, the temperature difference within one cycle and the number of cycles [25]. From the performance point of view, among the several electrical parameters which are temperature dependent, the most relevant is the on-state resistance. In fact, the higher is the temperature the higher the $R_{DS(on)}$ is, and this consequently leads to an increase in the conduction losses. To keep the junction temperature inside safe and reliable boundaries, a cooling system is needed. It is usually composed by an heat-sink which provides low thermal resistance allowing the heat to be easily transferred to the

ambient. In case the thermal power that needs to be dissipated is high, the heat-sink is combined with a forced air convection system. In case of very high power, the heat-sink is composed by pipes in which a coolant is pumped [26]. For the power target of the considered converter, only the natural and air forced convection are considered in this thesis. Analysing the designed converter, the maximum base area of the heat-sink cannot exceed $50x50\ mm$, because of the fixing holes position and the maximum space available on the board. For these reasons, the volume analysis has been carried out looking at the total height of the cooling system in order to give an indication of the cumbersomeness of the proposed solution.

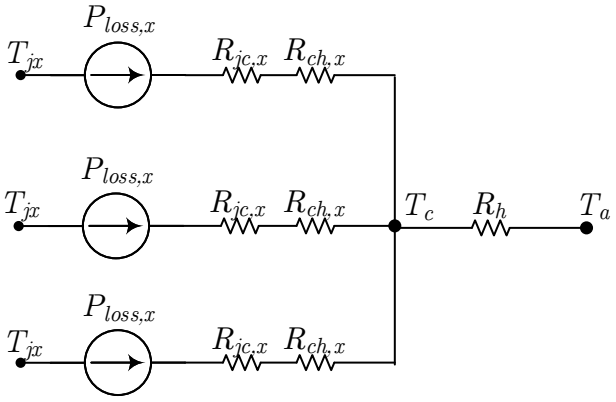


Fig. 3.1: Equivalent thermal circuit for one heatsink. The subscript x indicates the number of the switch.

In order to design the proper cooling system, the maximum thermal resistance has to be calculated given the power losses and the thermal impedance of the transistor's case. Since the maximum power transfer happens in steady-state, the thermal capacitances are not considered in the design. The system analysis can be simplified using the electrical equivalence of thermal components such as power sources, thermal impedances, and temperature difference. The equivalent electrical circuit is composed by a current source, total junction to case resistance and total resistance case to heat-sink. As shown in Fig. 3.1, each heatsink is mounted on a group of three devices: S_1, S_2 and S_3 for the top-side and S_4, S_5 and S_6 for the bottom-side. Although the two heatsinks are joint together by metal screws, the analysis is simplified assuming that there is no thermal correlation between the two. The total thermal resistance can be

expressed as follows:

$$R_h = \frac{T_c - T_a}{P_{loss}} \tag{3.1}$$

where T_c is the desired case temperature, T_a is the ambient temperature and P_{loss} is the total power loss that needs to be dissipated by the heat-sink, namely the sum of the switching and conduction losses of the three devices connected to the heatsink. For the power considered in this case, the conduction losses are predominant respect to the switching one, therefore the power loss is assumed as equal to the maximum value all over the frequency range. Regarding the case temperature, it is selected as $80°C$ in order to keep the junction temperature in a reasonable region and avoid that the peak temperature goes above the limit of $150°C$ imposed by GaN Systems Inc.. Using the approximation proposed in [8], the volume of a naturally cooled heatsink can be calculated:

$$Vol = 286.71 \cdot R_{th}^{-1.468} \tag{3.2}$$

Leading to a volume of 3045 cm^3 for each heatsink. If the calculated volume is normalized to the defined base area, the height of the heatsink can be calculated as:

$$h = \frac{Vol}{A_b} \tag{3.3}$$

where A_b is the base area of $50x50$ mm. A market survey of the available finned heatsink with the desired A_b has revealed that the maximum available height for such base size is 50 mm, while the required height for the calculated thermal resistance is 112.5 cm. Thus, to reduce the height of the heatsink, the forced convection is necessary. The addition of a fan combined with a heatsink helps indeed in reducing the thermal resistance while keeping the total volume of the cooling system low. The reduction of the thermal resistance depends on the flow speed v, and characteristic curves are usually provided by the heatsink manufacturer from which the thermal resistance can be extracted as function of the employed fan. The fan thermal performances can be quantified by looking at the flow rate Q. The two quantities, flow speed and flow rate, are related by:

$$Q = A_d \cdot v \cdot 60 \tag{3.4}$$

where A_d is the duct area of the fan. Usually the flow speed is indicated in $^{v}/_{m}$ and the flow rate in $^{m^3}/_{h}$, this explains the constant 60 in Eq. 3.4. For this analysis, three different commercial heatsinks with the required base area have been taken from the Fischer Elektronic [27] product database, with heigths of 25 mm, 40 mm and 50 mm.

For these models, the curves $R_{th} - v$ have been plotted with solid lines in Fig. 3.2 using hyperbolic curve fitting of the data given by the manufacturer. Regarding the fan, three heights have been taken from Delta Electronics [28] and Sanyo Denki [29] products: 10 mm, 15 mm and 28 mm. It results that the only feasible option is the combination of a 50 mm heatsink with a 28 mm fan with a flow rate of 54.03 $^{m^3}/_{hr}$. With this solution, the total height of the cooling system is 78 mm which is 30% smaller than the one in natural convection, leading to a total volume for each heatsink of 195 cm^3.

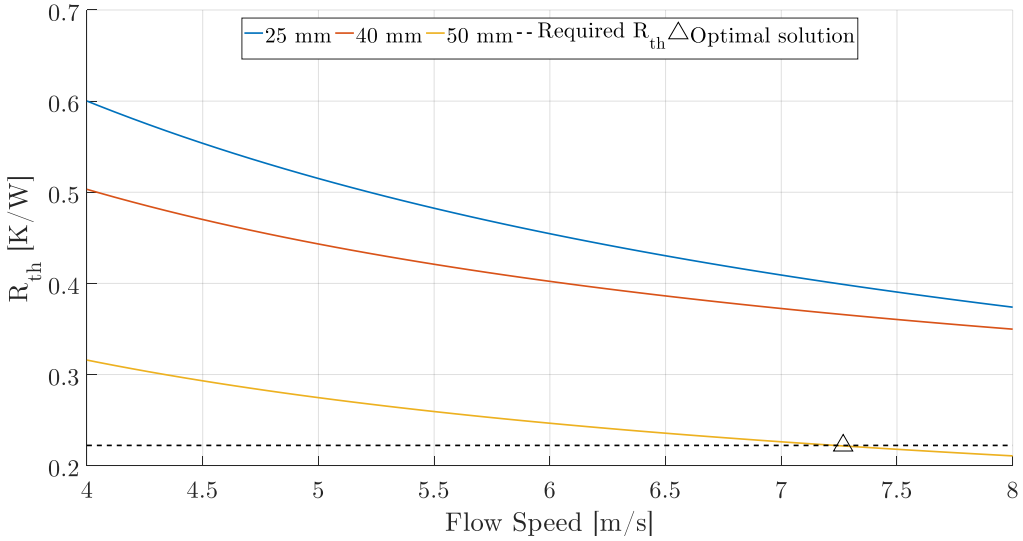


Fig. 3.2: Selection of the heatsink height and the fan.

3.2 DC-link Capacitor selection

3.2.1 Single-Phase

As known, the instantaneous power in single-phase has a pulsation at a frequency that is double the line frequency. This power fluctuation has the DC-link voltage ripple as a consequence and, if too high, can result in higher output voltage distortion. To overcome this problem, a capacitance is inserted between the DC source and the DC/AC converter. This capacitance acts as an energy storage, being charged in half cycle and discharged in the second half. The selection of this capacitance needs to be done

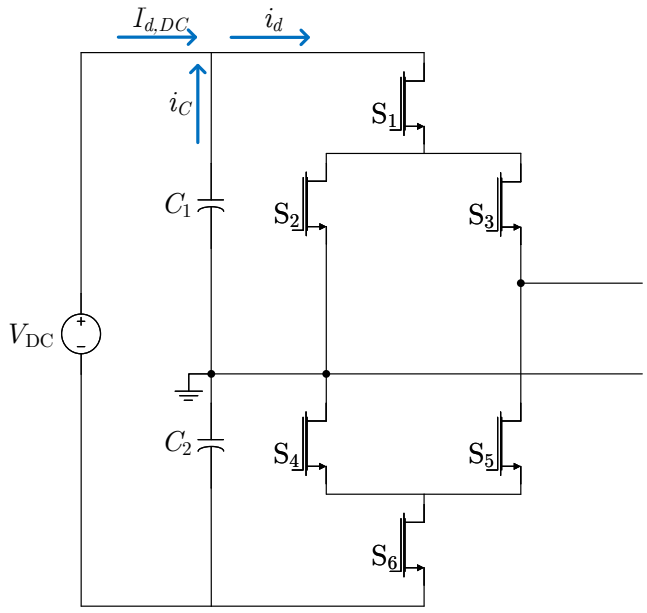


Fig. 3.3: Single-phase 3L-ANPC schematic with DC-link currents paths.

accordingly with the output power, maximum voltage ripple allowed and maximum RMS current that flows into the DC Link capacitor. In case of an ANPC single-phase inverter, the DC buffer connection is composed by two capacitances of equal value, connected to the positive and negative rails of the DC-link and the neutral point, as shown in Fig. 3.3. The current i_d is composed by two terms: a DC term provided by the DC supply and an AC term, provided by the capacitor. The energy balance of each capacitor happens within one fundamental cycle. For example, examining the upper capacitor's energy balance, it releases energy to the load during the positive half-wave of the fundamental and it is charged during the negative half-wave. Assuming that there are no losses in the inverter and the power factor is equal to 1, the input power can be equalized to the output power [30]:

$$p_{in}(t) = p_{out}(t) = \frac{\widehat{V}\widehat{I}}{2} + \frac{\widehat{V}\widehat{I}}{2} \cdot cos(2\omega t) = P + Pcos(2\omega t) \tag{3.5}$$

The part of the total power that has to be provided by the capacitor is the term $Pcos(2\omega t)$. This power can be equalized to the derivative in time of the energy stored in the capacitor:

$$Pcos(2\omega t) = \frac{1}{2} C_{dc} \frac{d(v_c(t)^2)}{dt} \tag{3.6}$$

By solving the differential equation, the capacitance expression becomes:

$$C_{dc} = \frac{\widehat{I}V_{dc}}{4V_{pp}^2\omega} \cdot [1 - cos^2(2\pi\omega)] \tag{3.7}$$

where V_{pp} is the maximum peak-to-peak voltage, which usually is set to be 5% of the nominal voltage. Using the nominal parameters indicated in Table. 1.1, 5 mF for each branch are needed, with a RMS current of 7.5 A. For such a capacitance value, the electrolytic capacitor solution is the most compact, due to its higher capacitance density and low cost when compared to other technologies [31]. As an example, the EPCOS B43513 has been selected in order to have a general idea about the volume and the performance of an Al-cap of this size. The selected model with a voltage rating of 450 V is available in single capacitors of 1000 μF with soldering leads. In Table 3.1 the main characteristics of this model are listed. To reach the necessary 5 mF, two capacitor banks of 5 capacitors in parallel for each bank is necessary. Connecting in parallel the five capacitors allow to reduce the total ESR to 20 $m\Omega$, reducing the total losses of the DC-link buffer. Another benefit of the paralleling multiple capacitor is the reduction of the ESL. Indeed, since this converter works with high $^{di}/_{dt}$, a high inductance would be summed with the commutation loop inductance. In this case, the total ESL seen by the commutation loop is 4 nH. Additionally, the current stress on the single capacitors is reduced by factor of 5, leading to a RMS current for each capacitor of circa 1.9 A.

$\mathbf{C_{DC}}$	1000 μF
$\mathbf{V_{DC}}$	450 V
$\mathbf{I_{max}}$	9.45 A
ESR	100 $m\Omega$
ESL	20 nH
Volume	100.5 cm^3

Tab. 3.1: EPCOS B43513 capacitor parameters [32].

As expected, the total volume of the capacitor banks is high, namely 1005 cm^3, having a significant impact on the overall volume and on the power density of the converter. A viable solution for single-phase application to increase the compactness of the DC-link buffer would be the use of an active power buffer, which allows the use of MPPF capacitor decreasing the overall volume and increasing the reliability of the

system [33],[31].

3.2.2 Three-Phase

The sizing of the DC-link capacitor is crucial for the three-phase operation as well. Besides the effect of the voltage ripple on the output distortion, the impact of the capacitor volume is high when a compact system is required. For this reason, different modulation strategies have been explored finding the one that allows to use the smallest capacitance. In this subsection, the design analysis for the SVM is exposed, since is the worse case scenario for the DC-link sizing because of its inability to balance the capacitors voltages.

In this section, the method proposed in [34] is applied to calculate the capacitance as function of the instantaneous capacitor current expression. Analysing the circuit of Fig. 3.4, the current i_d is the current of the upper switches of phase a,b and c. i_d is composed by two term: an AC term $i_{d,C}$ which is provided by the DC-link capacitor, and a DC term $i_{d,DC}$ provided by the DC source.

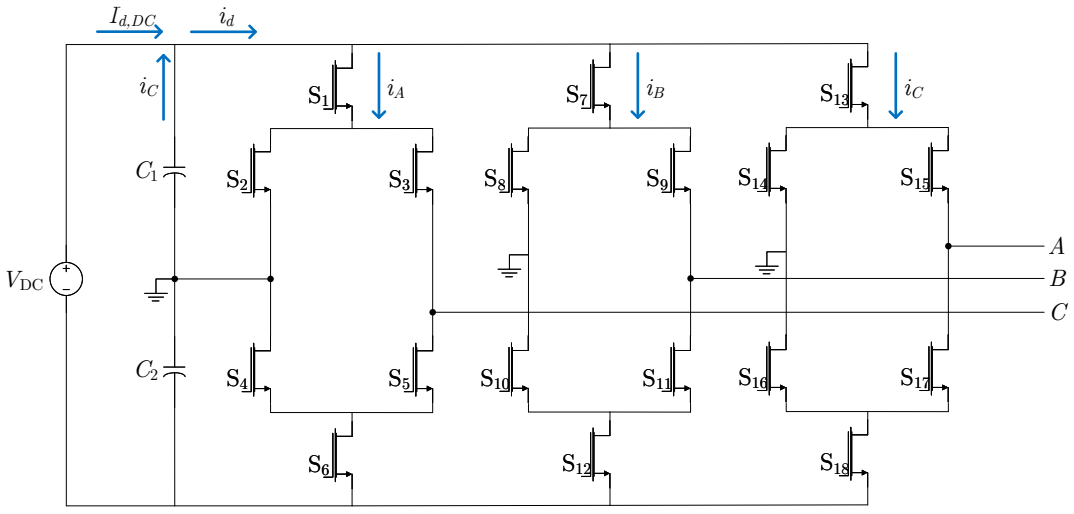


Fig. 3.4: Three-phase 3L-ANPC schematic with DC-link currents paths.

The output phase voltage are function of the duty cycle d_x, where x can be replaced by the phase a,b or c. In SVM, the duty cycles are expressed as:

$$d_x = m \cdot cos(\theta + \theta_x) - v_{zs} \tag{3.8}$$

where v_{zs} is the zero-sequence injected to obtain the SVM and θ_x is 0 for phase a, $^{2\pi}/_{3}$ for phase b and $^{2\pi}/_{3}$ for phase c. It can be proven that the instantaneous waveform of i_d has a low-frequency component with period $^{1}/_{3 \cdot f_{line}}$, therefore the analysis is restricted to this interval. Such an interval can be divided into three sectors:

$$\begin{cases} \text{I} = \frac{\pi}{6} \geq \theta < \frac{\pi}{3} \\ \text{II} = \frac{\pi}{3} \geq \theta < \frac{2\pi}{3} \\ \text{III} = \frac{2\pi}{3} \geq \theta < \frac{5\pi}{6} \end{cases} \tag{3.9}$$

Defined the duty cycles, the current i_d can be written as:

$$i_d = i_A \cdot d_A \cdot (S_A) + i_B \cdot d_B \cdot (S_B) + i_C \cdot d_C \cdot (S_C) \tag{3.10}$$

where S_x can assume two values: 1 when the duty cycle is positive and 0 when negative. The DC source current can then be expressed as:

$$I_{d,DC} = \frac{3}{2\pi} \left(\int_{\pi/6}^{\pi/3} i_{d,DC}(\theta) d\theta + \int_{\pi/3}^{2\pi/3} i_{d,DC}(\theta) d\theta + \int_{2\pi/3}^{5\pi/6} i_{d,DC}(\theta) d\theta \right) \tag{3.11}$$

where $i_{d,DC}(\theta)$ is the average current in every switching period within the section (i.e. I, II or III). Looking at Fig. 3.5 where the section I is taken as example, $i_{d,DC}(\theta)$ can be generally expressed as:

$$i_{d,DC}(\theta) = f_{sw} \left(\sum T_{intk} i_{d,intk} \right) \tag{3.12}$$

To calculate the necessary capacitance, the capacitor charge exchange is:

$$dQ = i_{d,C}(\theta) d\theta \tag{3.13}$$

Integrating both terms of 3.13, the instantaneous expression of the charge Q can be obtained. The peak-to-peak value of the charge is proportionally related to the peak-to-peak voltage, leading to the following expression to calculate the total capacitance:

$$C = \frac{Q_{pp}}{\Delta V_{pp,max}} = \frac{2 \cdot Q_{pp}}{0.05 \cdot V_{DC}} = 200 \ \mu F \tag{3.14}$$

where V_{DC} is the full DC-link voltage of 700 V. On each phase leg board are installed

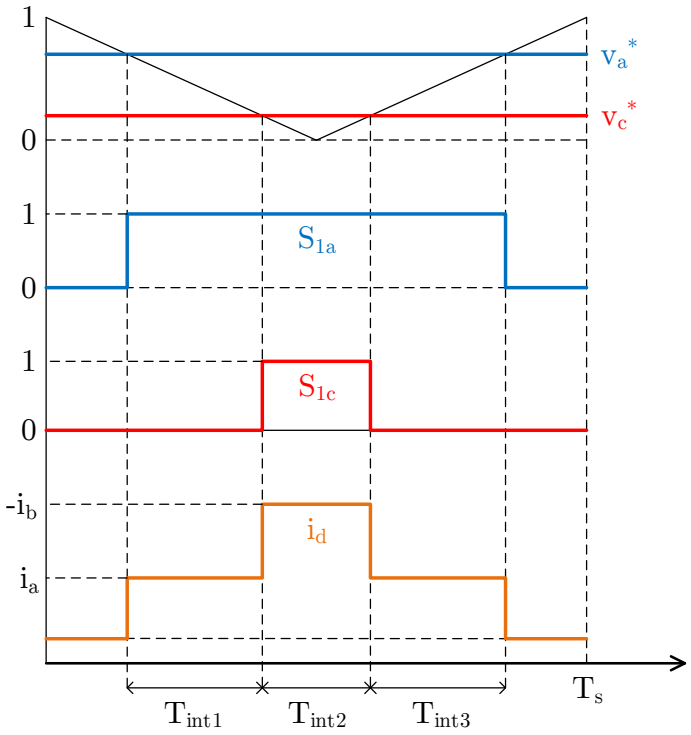


Fig. 3.5: Switching cycle analysis for the current i_d in Sector I.

two capacitors of 21 μF with a total of 63 μF for the three-phase system. Therefore, the needed capacitance is decreased to 137 μF and a suitable commercial capacitor has to be found. As described in [31], the most reliable capacitor technology is the Metallized Polypropylene Film Capacitors (**MPPF-C**), at the expenses of the capacitance density. Even this, since the necessary capacitance value is low, a reliable solution is preferable to a compact but poorly reliable solution (i.e. Al-caps). From EPCOS catalogue [35], a 65 μF capacitor from the series B32678 has been selected to form two small capacitor banks of two capacitors each. The characteristics of this capacitor are listed in Table. 3.2. As for the single-phase case, the paralleling of two capacitors leads to the reduction by a factor of two of the ESL, ESR and RMS current with the related and already mentioned benefits. The total volume of the capacitor bank is 620 cm^3

$\mathbf{C_{DC}}$	65 μF
$\mathbf{V_{DC}}$	450 V
$\mathbf{I_{max}}$	48 A
ESR	1.6 $m\Omega$
ESL	20 nH
Volume	155 cm^3

Tab. 3.2: EPCOS B32678 65 μF capacitor parameters [35].

Regarding the VSVM and the Optimized VSVM, has been shown in Sec. 2.3.2 that, with these strategies smaller DC-link voltage oscillations occur when compared with the SVM, allowing the use of a smaller capacitance. Therefore, these modulations have been tested with the minimum capacitance of 63 μF and it is verified the positive impact on the DC-link buffer volume of them.

3.3 Output Filter Design

Another element which has a strong impact on the overall volume is the output filter. The need of an output filter in inverter application is to filter out the unwanted harmonics that are naturally present in the output of power electronic converters. These unwanted harmonics are primarily generated by the switching and the harmonic spectrum may differ between different modulation strategies. However, the injection of current harmonics in the grid is permitted to some extent. The amount of allowed harmonics is defined by the grid codes in terms of amplitude of each harmonic or in terms of THD. An example of harmonic injection limits is the IEEE-519 standard, which defines the maximum allowed amplitude of each harmonic for different Short Circuit Ratio. In order to fulfil the grid codes (i.e. IEEE-519), an high order output filter is preferable to a simple L filter, since the attenuation of high-frequency harmonics is more effective in the former. The LC filter of Fig. 3.6 is a second order filter which gives a $^{-40dB}/_{dec}$ for frequencies above the resonance frequency. The first element that needs to be designed in a LC filter is the converter-side inductance. Its value is inversely proportional to the allowed current ripple on the converter-side current:

$$L_f = \frac{V_{DC}}{8 \cdot f_{sw} \cdot \Delta i} \tag{3.15}$$

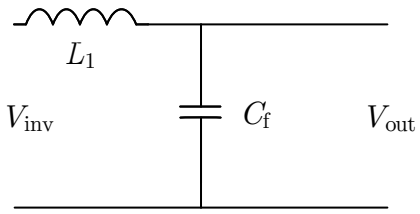


Fig. 3.6: Circuit scheme of the LC filter.

$$L_f = \frac{V_{DC}}{24 \cdot f_{sw} \cdot \Delta i} \tag{3.16}$$

where Eqs. 3.15 and 3.16 are the expression for single and three-phase three-level inverters respectively. The term Δi is the amount of current ripple allowed, which is usually set as 20% of the output current. This choice is made as trade-off between the maximum current switched by the transistors and the amount of ripple accepted at the output of the filter. The filter capacitance is calculated depending on the filter inductance:

$$C_f = \frac{1}{(2\pi \cdot f_{sw})^2 \cdot L_f \cdot k_{att}} \tag{3.17}$$

The attenuating factor k_{att} has to be chosen to provide proper damping at the switching frequency and ensure that the resonance frequency does not coincide with the switching frequency, to avoid unwanted amplification of the switching ripple [8].

In order to estimate the volume occupied by the filter, the volume of the inductor and the capacitor needs to be approximated. For an inductor, its volume can be approximated by the formula [36]:

$$V_L = k_L \cdot A_p^{\frac{3}{4}} \tag{3.18}$$

where k_L is an experimentally defined volume constant and A_p is the so-called area-product and it is calculated as [36]:

$$A_p = \left[\frac{\sqrt{1+\gamma} \cdot K_i \cdot L_f \cdot \widehat{I^2}}{B_{max} \cdot K_t \cdot \sqrt{k_u \Delta T}} \right]^{\frac{8}{7}} \tag{3.19}$$

where γ is the ratio between the core losses and the copper losses, which is usually assumed as zero in the cases where the flux ripple is negligible. B_{max} is the maximum

γ	$\mathbf{K_i}$	$\mathbf{K_t}$	$\mathbf{K_u}$	$\mathbf{\Delta T}$ $[°C]$
0.03	$\sqrt{2}$	$48.2 \cdot 10^3$	0.8	60

Tab. 3.3: Constants used to calculate the area-product of an inductor.

flux density, $\widehat{I^2}$ is the peak current, L_f is the inductance and ΔT is the temperature rise in the windings. All the constants are listed in Table 3.3. Regarding B_{max}, it can be calculated using the approximation [8]:

$$B_{max} = |1.111 \cdot 10^4 \cdot f_{sw}^{-0.3104} - 132.3| \cdot 10^{-3} \tag{3.20}$$

which is valid for switching frequencies between 25 and 200 kHz. The capacitor volume follows a linear equation:

$$V_C = k_c \cdot C_f \cdot V_{nom}^2 \tag{3.21}$$

where V_{nom} is the nominal capacitor voltage, C_f is the calculated capacitance and k_c is the capacitor volume constant and can be extracted from commercial products datasheets. For output filter applications, the most suitable capacitor are the X capacitors, since they are connected between phase and neutral of the output. As suggested in [8], the EPCOS MKP339-X2 series is the one with the lower k_c, namely 60.

Using Eqs. 3.15, 3.16 and 3.17, the filter parameters have been calculated and the filter volume has been calculated for both single and three-phase operation. As expected, the total filter volume decreases with the increasing of the switching frequency. A peculiar aspect is that the impact of the capacitance on the overall volume is ten times smaller than the inductance in single-phase operations. This means that with a small increase in volume, the output distortion performances can be significantly improved when compared with a simple inductive filter. The total volume varying the switching frequency in single-phase operation is shown in Fig. 3.7

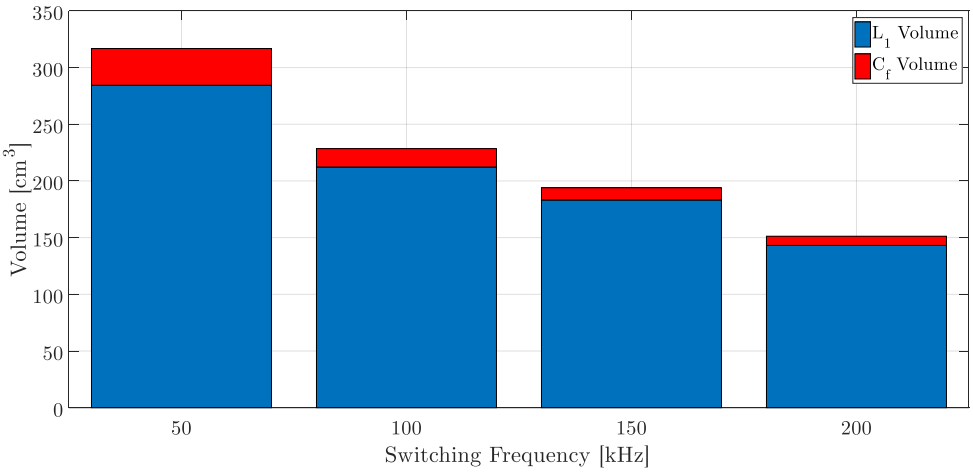


Fig. 3.7: Comparison of total volume and the capacitance impact for the different switching frequencies considered in single-phase operation.

Regarding the three-phase operation, the impact of the capacitance on the overall volume is equally shared with the inductor for 50 kHz, while increasing the switching frequency L_f volume is predominant. Despite this, the use of LC filter remains a better choice also for high switching frequencies instead of a simple L filter. The bar chart of the phase-leg filter volume is shown in Fig. 3.8.

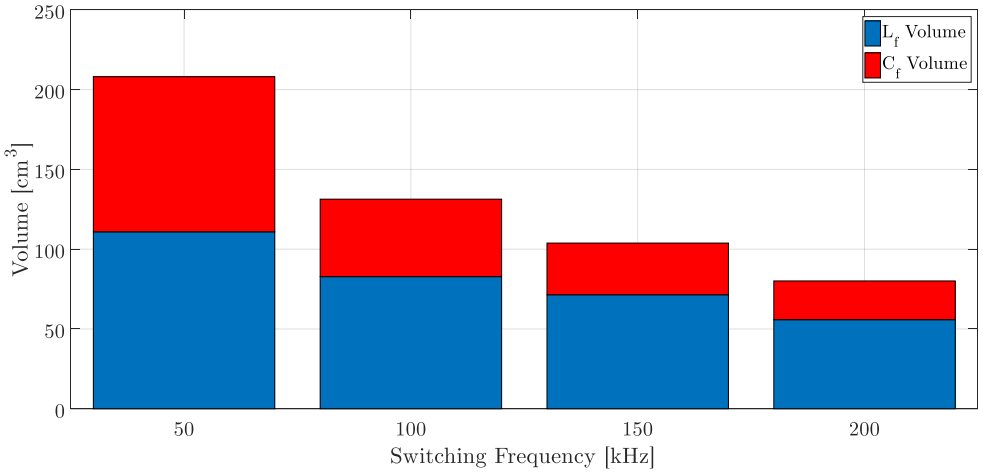


Fig. 3.8: Comparison of phase-leg filter volume and the capacitance impact for the different switching frequencies considered in three-phase operation.

With the calculated volumes of cooling system, DC-link capacitors and output filter, an estimation of the overall volume of the converter can be done. Firstly, the

single-phase operation mode is analysed. In Fig. 3.9a can be seen that over the frequency range, the most voluminous part is occupied by the DC-link. Moreover, between the 50 kHz and 200 kHz switching frequency the volume of the output filter is halved. As mentioned, the increasing of the switching frequency does not have a particular impact on the heatsink volume, since the thermal resistance required for the different frequencies has a small variation.

Regarding the three-phase configuration, the volume composition has the cooling system as predominant. Indeed, the DC-link volume has a very low impact when compared with the single-phase operation. The output filter has a slightly greater reduction over the frequency variation compared to the single-phase, which is a bit more than halved from 50 kHz to 200 kHz.

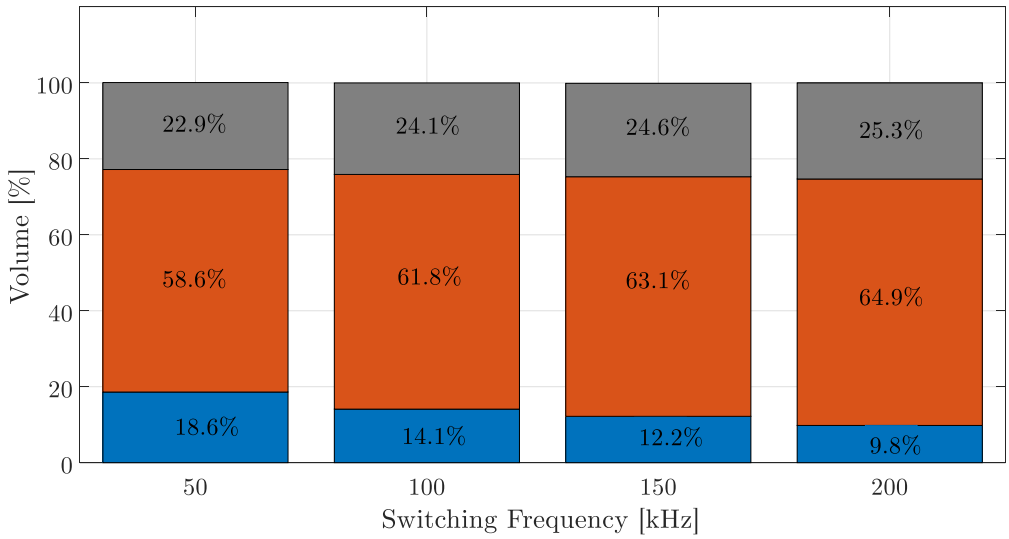
From this analysis has emerged that the only system component that varies with the switching frequency is the output filter. It has been demonstrated that the cooling system has almost no variation in the volume increasing the switching frequency. This is partially due to the predominance of the conduction losses for such a high delivered power. On the other hand, this is due to the effectiveness of the forced convected cooling system that allows to have a low thermal resistance for a small heatsink volume.

3.4 Gate Driver and Commutation Analysis

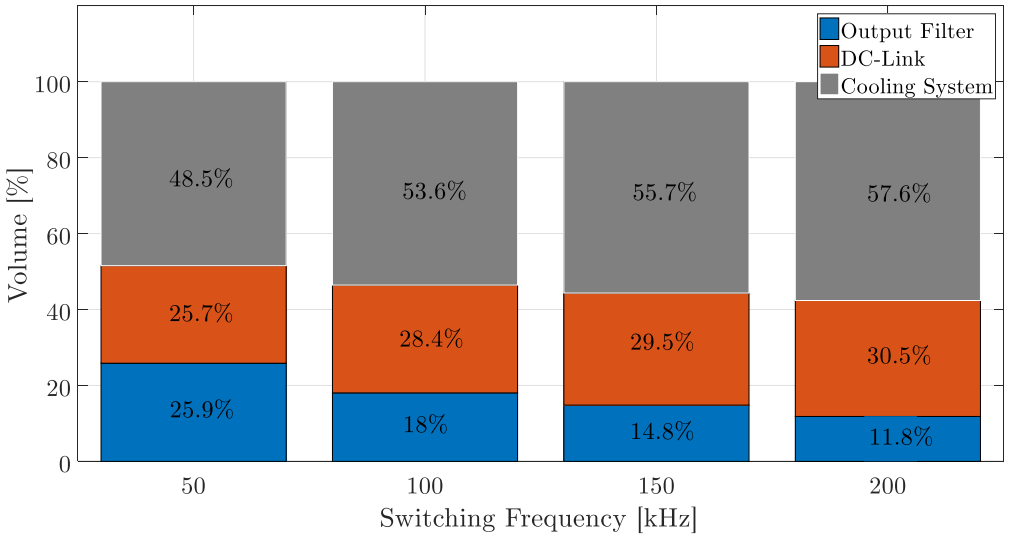
To better understand the operation of the designed three-level inverter, a thorough description of its parts is given hereafter. The description starts with the low-voltage side, namely the control interfaces and the gate driver. Then, the switching loop is described and the previous analysis of the parasitic inductances is reported.

3.4.1 GaN Systems GS66508T

As mentioned in Chapter 1, the 650 V GaN HEMT is the best candidates for low-voltage PV applications, as the purpose of the developed inverter. GaN Systems released this transistor with two current ratings: 60 A and 30 A. The latter is the one chosen for this 5 kW application, whose product number is GS66508T. This device is built with the patented packaging technology named GaN_{PX}. The peculiarity of this laminated packaging is the very low stray inductance of 0.4 nH and the possibility to exclude the PCB from the thermal impedance, thanks to its top-cooling structure. The main



(a)



(b)

Fig. 3.9: Overall volume partition: in *(a)* single-phase converter is presented, while in *(b)* the three-phase converter.

electrical characteristics of the device are listed in Table 3.4.

Drain-Source Voltage (V_{DS})	650 V
Continuous Drain Current (I_{DS})	30 A @ 100°C
Drain-Source On-State Resistance ($R_{DS,on}$)	55 $m\Omega$ @ 25°C 129 $m\Omega$ @ 100°C
Input Capacitance (C_{ISS})	260 pF
Output Capacitance (C_{OSS})	65 pF
Reverse Transfer (C_{RSS})	2 pF
Gate Charge (Q_G)	5.8 nC
Min. Gate Threshold Voltage (V_{th})	1.7 V
Gate-Source Voltage (V_{GS})	$-10\ to + 7\ V$
Maximum Junction Temperature (T_j)	150°C
Reverse Recovery Charge (Q_{RR})	0 nC
Package Stray Inductance (L_σ)	0.4 nH
Device Package	GaN_{PX}

Tab. 3.4: GS66508T GaN HEMT parameters.

Loss Model

The performance analysis is primarily based on the evaluation of the switching and conduction losses, and therefore a loss model is needed. In the following, an analytical background for the losses calculation is given in a general form valid in both single and three-phase with any modulation strategy. The conduction losses in a MOSFET are expressed in two different ways for the forward conduction and the reverse conduction. As described in Sec. 2.2, the GaN HEMT are capable of reverse conduction but with the addition of a voltage drop which depends on the gate-source voltage applied. The reverse conduction happens only during the dead-time, when both the complimentary devices are turned off to avoid shoot-through. Let's define the drain current as equal to the output current during the switching event of interest:

$$i_D(t) = i_{out} = \widehat{I} \cdot sin(\omega t - \phi) \tag{3.22}$$

where ϕ is the load angle in case of non unity power factor. To quantify the conduction time, the duty cycle has to be defined as in Eqs. 3.23 and 3.24 for the active and zero state respectively:

$$D_a(t) = M \cdot sin(\omega t) \tag{3.23}$$

$$D_z(t) = 1 - M \cdot sin(\omega t) \tag{3.24}$$

The conduction losses are dependent from the voltage drop across the device and the drain current. The voltage drop during forward conduction is:

$$v_{on}(t) = R_{DS,on} \cdot i_D(t) \tag{3.25}$$

The forward conduction losses generated over one fundamental period can be calculated as:

$$P_{cond,x} = \frac{1}{T} \int_0^T R_{DS,on} \cdot i_D^2(t) \cdot D_x(t)\ dt \tag{3.26}$$

where x can indicate either the active state or zero state. Therefore, the total conduction losses for each switch can be calculated according to the states defined by the modulation technique used. Additionally, it is worth to calculate the losses during dead-time as well. The voltage drop in reverse conduction during the dead-time is:

$$v_{on,dt}(t) = V_f + R_{DS,on} \cdot i_D(t) \tag{3.27}$$

where V_f is the voltage drop of the diode-like behaviour, which is dependent from the applied gate-source voltage during off-state. Given the voltage drop, the conduction loss during dead-time is expressed then as:

$$P_{cond,dt} = \frac{1}{T} \int_0^T v_{on,dt}(t) \cdot i_D(t) \cdot 2 \cdot t_{dt} \cdot f_{sw}\ dt \tag{3.28}$$

where t_{dt} is the dead-time and f_{sw} the switching frequency. Regarding the switching losses, they are dependent from the switching energy which can be either obtained from datasheet parameters, experimental measurement or simulation models. Assuming that the switching frequency is much greater than the fundamental frequency, the switching losses can be calculated as [37]:

$$P_{sw} = \frac{f_{sw}}{T} \int_0^T e_{on}(i_D(t)) + e_{off}(i_D(t))\ dt \tag{3.29}$$

where e_{on} and e_{off} are the turn-on and turn-off switching energies respectively. From Eqs. 3.26 and 3.29 it results clear that the temperature dependency of the parameters is not taken into account, leading to a non-trivial error in the calculation. Moreover, the analytical solution for each switching state and for different modulation technique

and number of phase has a great computational burden. A more precise and efficient way to calculate the losses is the use of the simulation engine of the software PLECS, which allows to perform the loss calculation taking into account the temperature effect, the modulation technique impact and so on. Therefore, an accurate model of the GS66508T has been implemented on PLECS along with the thermal path of the switches and the cooling system proposed in Sec. 3.1. The switching energies have been calculated through the model built in LTSpice, which includes an accurate model of the GaN HEMTs provided by GaN Systems, the commutation loop inductances and a detailed model of the gate driver circuit. The simulation has been ran varying three key parameters:

- given that the temperature at the nominal operating point is unknown, the junction temperature has assumed the following values: $25°C$, $75°C$, $100°C$, $150°C$;
- the nominal DC-link voltage is known from the project specifications and is 350 V for each switching cell. Therefore, the voltages on the simulations span from 300 V to 400 V, in order to have sufficient point for possible transient in voltage due to the DC-link voltage oscillations;
- the current has been varied from 1 A to maximum continuous drain-source current of 30 A.

The numerical results obtained from the LTSpice simulations are related to the instantaneous power during turn-on and turn-off events. These results have been imported in MATLAB and integrate over time, since for the simulation the switching energy losses are necessary. An example of a curve calculated and imported in PLECS is shown in Fig. 3.10 for the case of $V_{DS} = 350\ V$ and $T_j = 25°C$. The simulation engine of PLECS will interpolates between junction temperatures, drain-source voltages and drain currents.

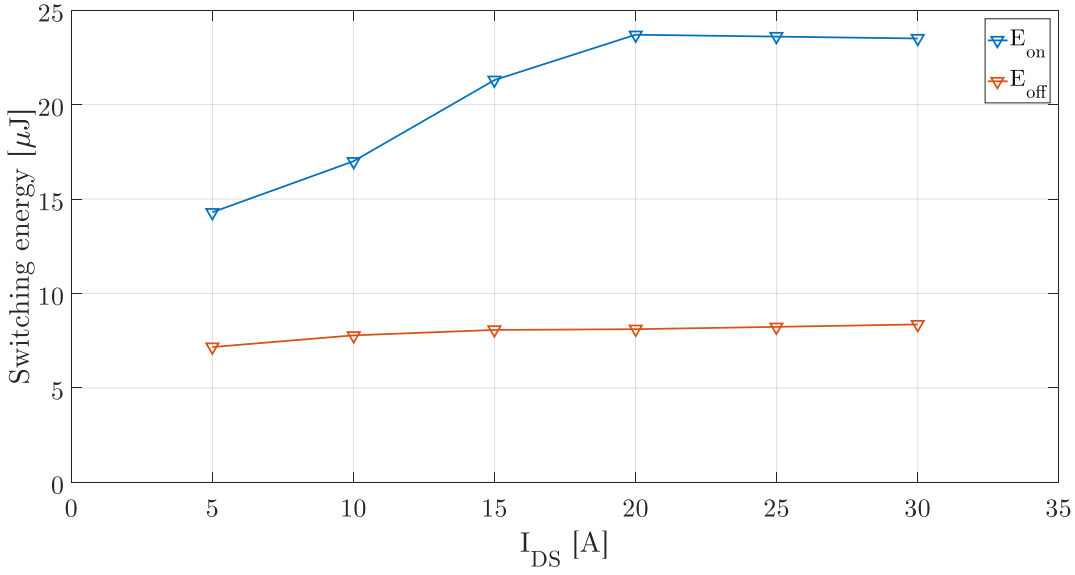
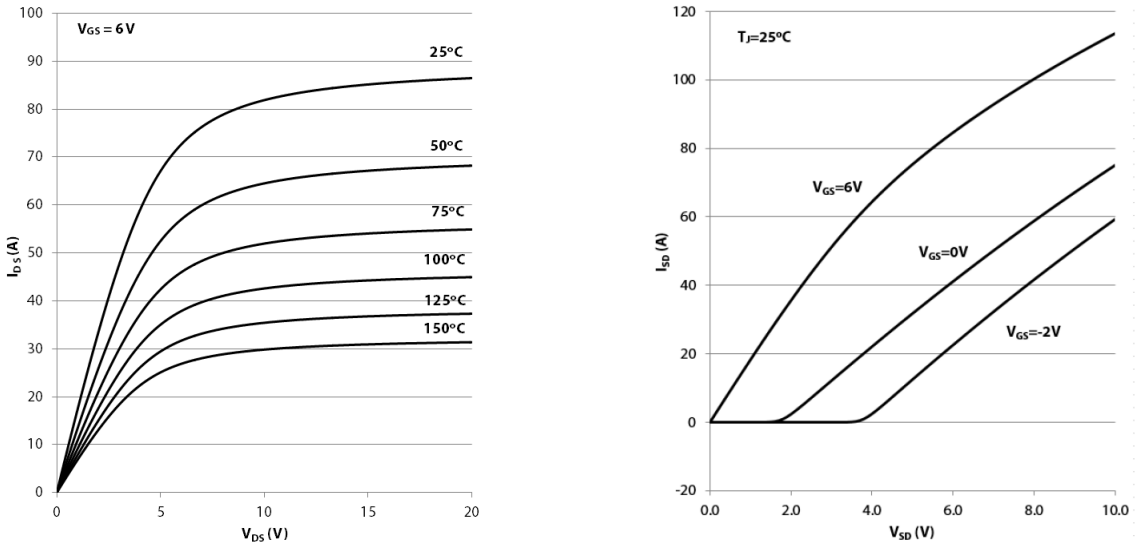


Fig. 3.10: Turn-on and turn-off energies with $V_{DS} = 350\ V$ and $T_j = 25°C$.

The approach to estimate the conduction losses is simpler with respect to the switching ones. Since in the operating region the group of curves $V_{DS} - I_{DS}$ is linear, few data-point have been extrapolated from the data-sheet plots of Fig. 3.11a and 3.11b which are related to the forward conduction and reverse conduction respectively.



(a) **(b)**

Fig. 3.11: On-resistance as function of the junction temperature in forward conduction in *(a)* and reverse conduction in *(b)*.

Regarding the thermal model of the GaN HEMT, an equivalent model is provided by GaN Systems [15]. The thermal characteristics of the transistor are expressed exploiting the equivalence with the electrical domain. In the provided model, the equivalent electrical circuit follows the Cauer model and the schematic is shown in Fig. 3.12. The thermal impedances details are listed in Table 3.5 along with the device layer which is modelled with.

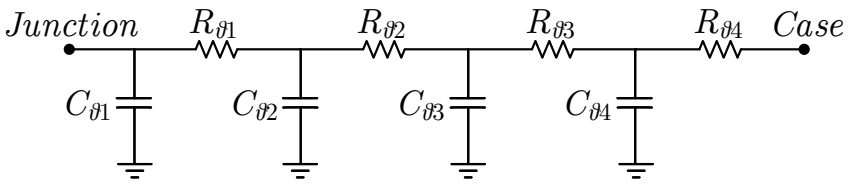


Fig. 3.12: Cauer model of the thermal structure of the GS66508T The impedance values are listed in Table 3.5.

Branch	$\mathbf{R}_\theta$ $[\frac{\mathbf{^\circ C}}{\mathbf{W}}]$	$\mathbf{C}_\theta$ $[\frac{\mathbf{W \cdot s}}{\mathbf{^\circ C}}]$	**Device Layer**
1	0.011	$4.25e^{-5}$	GaN
2	0.231	$2.96e^{-3}$	Si
3	0.237	$6.65e^{-4}$	Attachment
4	0.021	$1.01e^{-4}$	Cu base

Tab. 3.5: Thermal impedance value of the GaN System GS66508T[15].

3.4.2 Gate driver and control interface

As mentioned in Sec. 2.2, the GaN HEMTs have very low threshold voltage and input capacitance C_{iss} compared to the Si-MOSFETs or IGBTs. Therefore, a low inductance gate driver is needed. Moreover, given that the $^{dV}/_{dt}$ is high, the cross-talking between the commutating devices immunity must be sufficiently high.

The gate driver implemented for this application is isolated and its structure is shown in Fig. 3.13. The modulation signals are generated with a Digital Signal Processor (**DSP**). The model chosen for this project is the Texas Instrument TMDSCNCD28379D, which provides 24 PWM channels that allow to rapidly extend the configuration to three-phase. Moreover, the maximum clock frequency is 200 MHz,

which allows a fine placement of the PWM pulses and dead-time. The signals generated are transferred to the inverter through optical fibres, in order to provide galvanic isolation between the power stage and the control stage. For this purpose, the DSP is directly connected to a primary interface board, provided with optical transmitter elements. The optical fibre link is then connected to a secondary receiving board, connected to the power board. The signal coming from the optical receivers is fed to a Silicon Lab Si861x signal isolator, with 50 $^{dV}/_{\mu s}$ CMTI and 10 ns propagation delay. Additionally, this device provides also electrical isolation between input and output up to 5 kV_{RMS}.

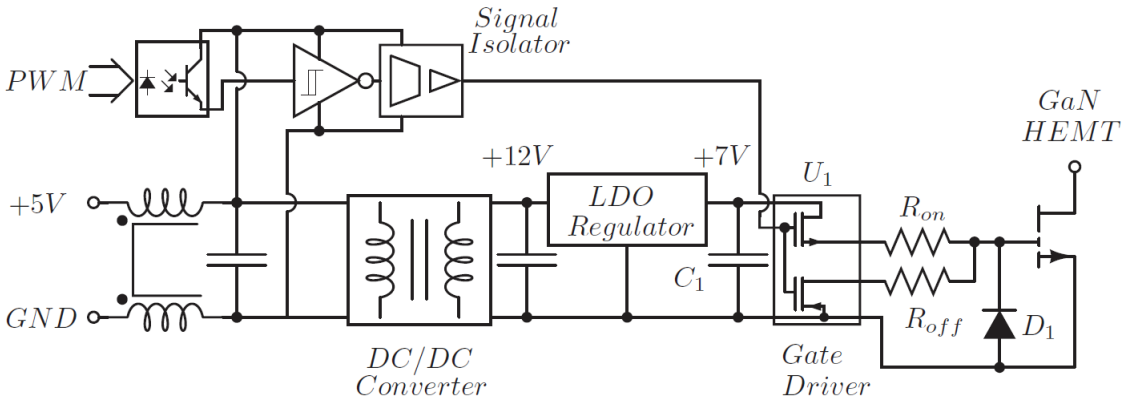


Fig. 3.13: Gate driver schematic [16].

The gate driver is powered via isolated DC/DC converters. These converters are capable to deliver up to 1 W with +12 V output. The electrical isolation of these devices is 3 kV_{DC} and the coupling capacitance between primary and secondary side is 30 pF. It is worth to be mentioned that at this time, isolated DC/DC converter with lower coupling capacitance are available, feature that would improve the reduction of common-mode current due to the steep voltage transients of the GaN HEMT.

The output of +12 V is then lowered by low-dropout (**LDO**) voltage regulators. In the original design, the output voltage was set to +7 V according to the requirements given by the manufacturer of the GaN HEMT. This requirement is changed overtime, the required voltage now is +6 V in order to extend the current capability of the switches. Therefore, on the updated setup used in this thesis, the gate driver voltage in on-state has been set to +6 V, acting on the feedback resistors of the LDO voltage regulator.

The selected gate driver is the UCC27511 from Texas Instruments, which provides

a split output for turn-on and turn-off processes. This feature allows to have two different gate resistor for the two transitions, giving the possibility to adjust the slew rate differently and improve the Miller effect immunity. The current capability is 4 A and 8 A for turn-on and turn-off, respectively. The turn-off resistor R_{off} is selected smaller than the turn-on R_{on}. In this situation, R_{off} provides a low impedance path for the Miller current during positive $^{dV}/_{dt}$, while for the negative one this current flows through the high impedance path created by R_{on}. The latter situation leads to negative spikes on the gate voltage that may exceed the limit given in the data-sheet damaging the device. To avoid this unfavourable situation, a clamping diode is placed across the gate and source pins, providing a path for the Miller current during the negative $^{dV}/_{dt}$. In the provided design, the values for R_{on} and R_{off} are set to 15 Ω and 1.5 Ω respectively.

As mentioned, the main challenge in designing this gate driver is to reduce the inductance. For this purpose, the gate driver and the gate input pins of the device must be as close as possible. Moreover, the selected components such as resistors, capacitors and IC have been chosen with a small footprint (i.e. 0603), to further decrease the loop inductance. Each gate driver is placed onto two layers, one for the supply and signal and one for the ground plane. The PCB layout is shown in Fig. 3.14 where the top layer and inner layer are highlighted along with the components placement.

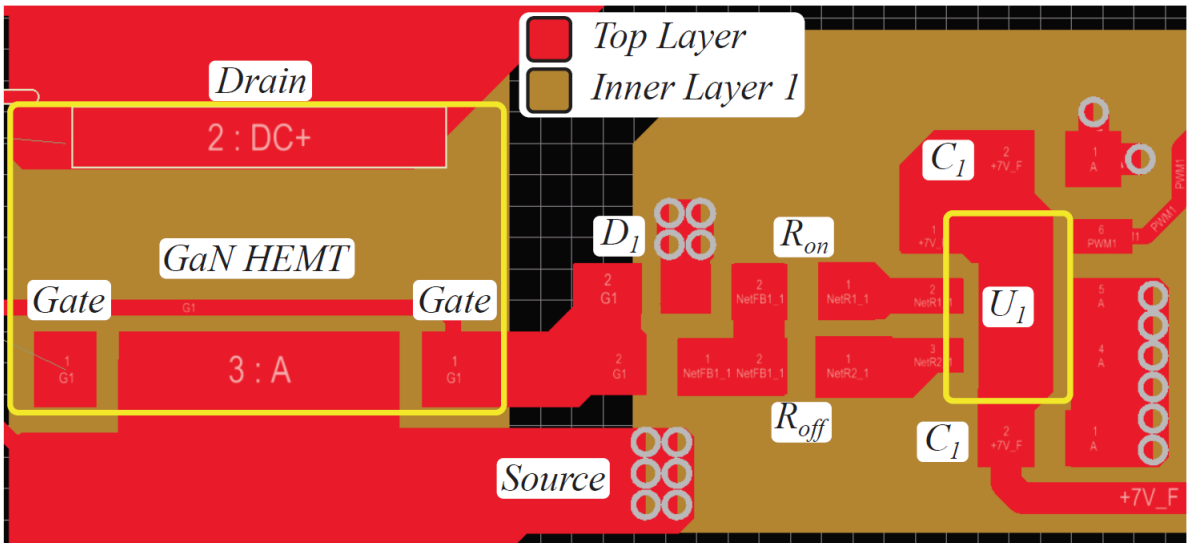


Fig. 3.14: PCB layout of the designed gate driver [16].

3.4.3 Commutation Loop

In Chapter 2 the output states of the 3L-ANPC are described. According to the selected switching pattern, the resulting commutation loops for the transition from positive to upper neutral and positive to lower neutral can be defined as depicted in Fig. 3.15a. It result clear that the transition from the negative to the two neutral states follows the same loop but involving S_6 instead of S_1. /par The commutation loop inductance

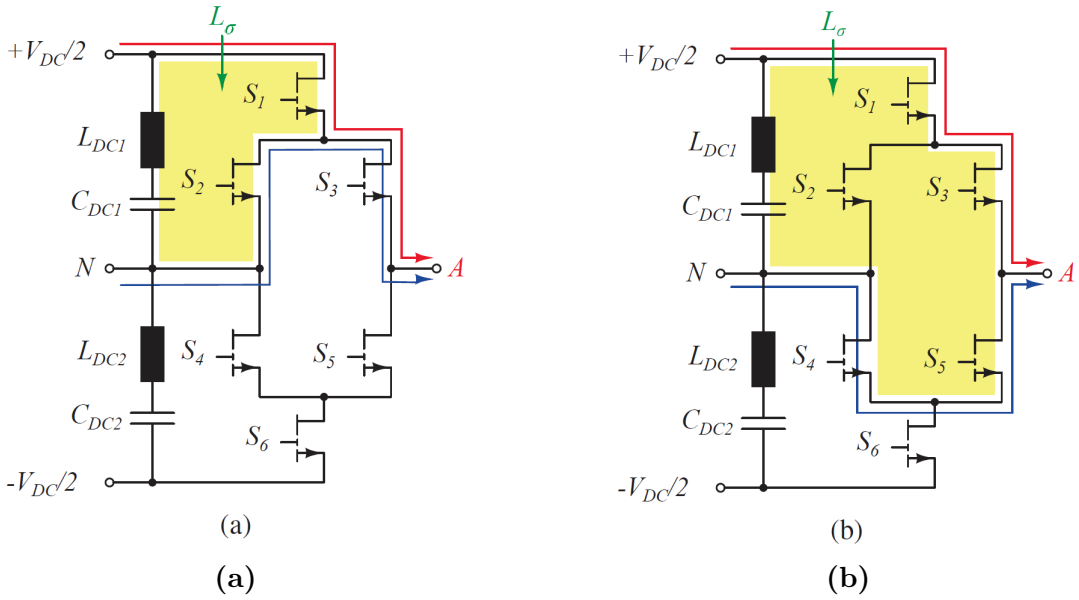


Fig. 3.15: Two commutation loops: *(a)* from positive to upper neutral state and *(b)* from positive to lower neutral state [4].

is formed by the PCB copper trace inductance and the self-inductance of the DC-link capacitors. Such inductance has to be minimized in order to reduce the voltage overshoot during switching and therefore reduce the EMI and switching losses. The self-inductance of the capacitors can be easily reduced paralleling several capacitors, (i.e. ceramic or film capacitors). Regarding the trace inductance, it can be minimized placing the switching devices as close as possible and overlapping copper planes that carry opposite currents in order to obtain field cancellation.

The packaging inductance plays an important role as well. From the GaN HEMT parameters shown in Sec. 3.4, it can be seen that the stray inductance of these devices is 0.4 nH, namely almost 17.5 times smaller than the traditional TO-220 package [4]. Bearing in mind the mentioned requirements for a low-inductance loop, the resulting design proposed in [4] is shown in Fig. 3.16. In this configuration, the phase-leg has

been divided into top and bottom sides which comprise S_1, S_2, and S_3 for the top, and S_4, S_5, and S_6 for the bottom side. With this arrangement, a four-layer PCB is required. Indeed, the top and bottom layers host the switches, the DC-link capacitors and the gate driver components while the inner layers provide the return paths for the neutral point connection. In this way, all the components are placed very close and the neutral point in the inner layers allow the field cancellation.

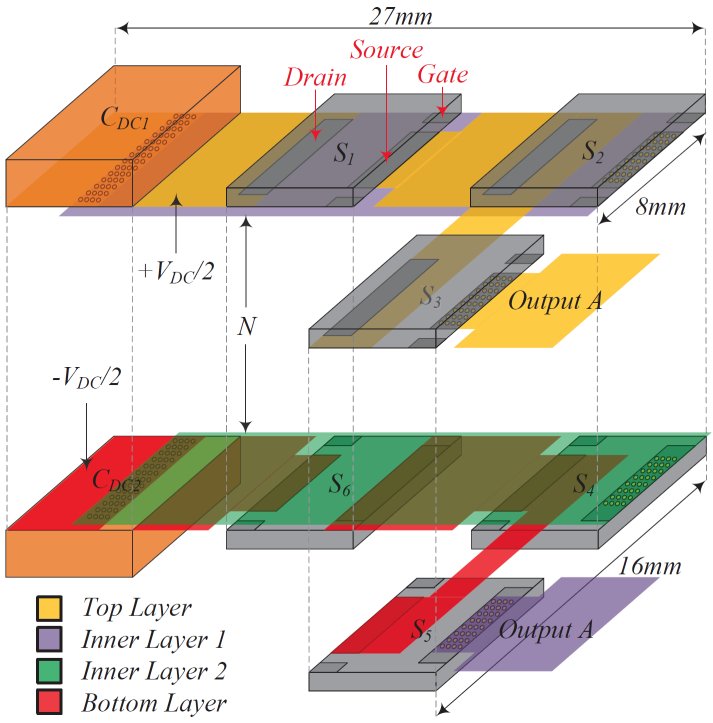


Fig. 3.16: PCB arrangement of the GaN HEMT and the decoupling capacitors[4].

A novel method to calculate the trace inductance in fast-switching application is proposed in [38]. The peculiarity of this method is that it allows to obtain a rather precise estimation instead of using finite element simulations. Referring to the notation of Fig. 3.16, L_σ can be then calculated using the proposed method:

$$L_\sigma = \mu_0 \frac{e}{w} l \left(\frac{1}{1 + \frac{e}{w}} + 0.024 \right) \tag{3.30}$$

where μ_0 is the free space permeability, l and w are length and width respectively, and e is the distance between the two copper traces involved in the field cancellation. L_σ for the two commutation loops shown in Fig. 3.15 can be then calculated using the GaN stray inductance (0.4 nH), the CeraLink capacitor ESL (2.5 nH) and the geometrical

dimension of each trace. The total inductance for the case in 3.15a is 3.8 nH and for 3.15b is 6.41 nH. Thanks to the symmetry of the PCB arrangement, the same values are valid for the negative states. From the presented value, it results clear that the switching loop inductances are effectively ultra-low and allow high-speed switching.

3.4.4 Switching Performances

In this section the switching performances of the 3L-ANPC converter are assessed. To simplify the analysis, the converter has been tested in synchronous buck DC/DC converter configuration. The switches involved in this configuration are S_4, S_5 and S_6. Precisely, S_4 and S_6 are synchronous pulse-width modulated, with a dead-time of 200 ns. Since the switch S_5 should be kept on during the switching cycle, it has been replaced with a copper foil in order to avoid useless conduction losses. The DC-link voltage has been set to 400 V and the power delivered to a resistive load is 1 kW. In Fig. 3.17, the output current along with the switches drain-source voltage is shown with a switching frequency of 50 kHz. Regarding the drain current of the devices, it has not been measured since the use of shunt resistances would introduce an additional inductance to the loop, to the detriment of the performances.

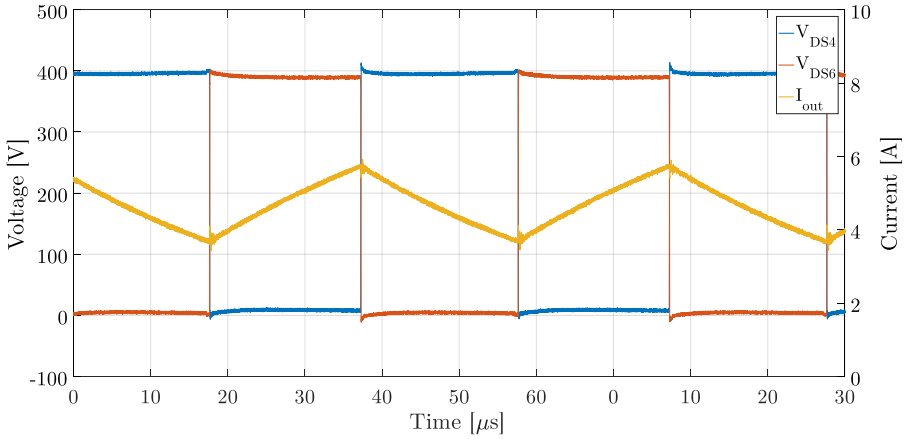
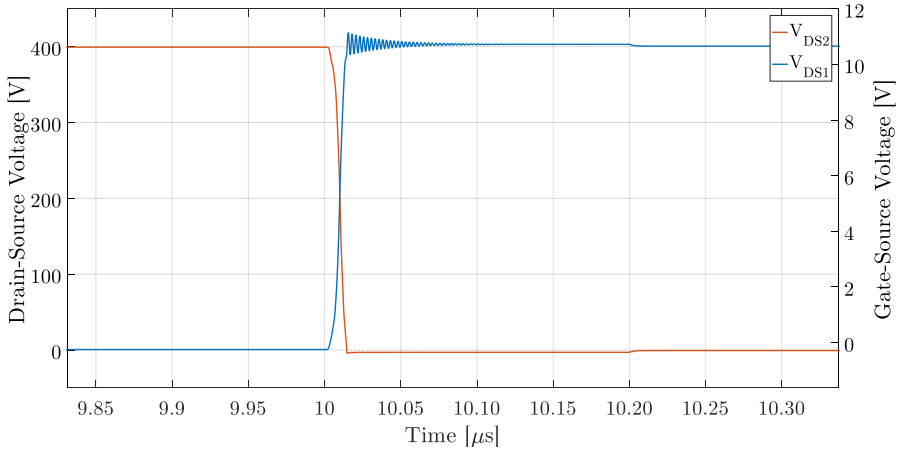


Fig. 3.17: Experimental result of the synchronous buck configuration test.

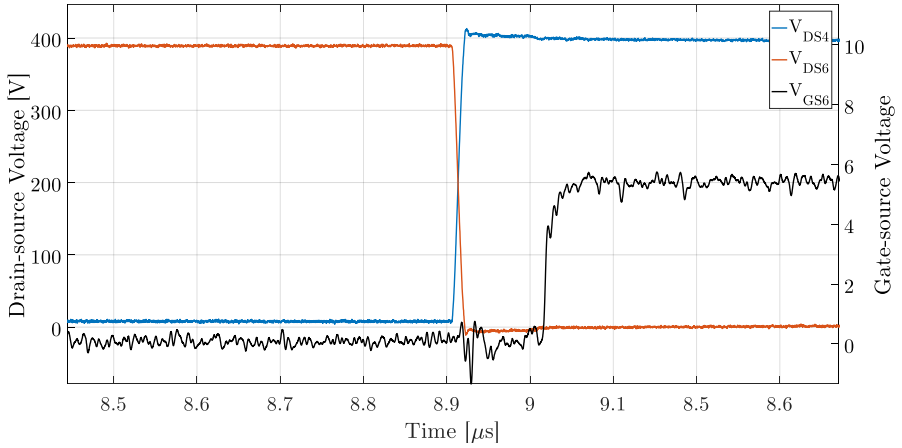
This same configuration has been implemented on a simulation model with the software LTspice and it has been validated through experimental results. On the simulation model, the loop inductances calculated in Sec. 3.4.3 are included along with the parasitic inductance of the DC-link capacitors. To reduce the computational burden on

the simulation model, the gate driver has been simplified as the turn off path is created by means of a diode in anti-parallel to the turn-on resistor. In this way, the slew rates are differentiated without compromising the efficacy of the simulation.

The two responses are shown in Fig. 3.18a 3.18b from simulations and experimental respectively. Examining closely the transient, the turn-on and turn-off of the two devices happens in 10.3 ns on simulation and 11 ns experimentally. Regarding the voltage overshoot, it results being 418.5 V on simulation and 413.2 V on the real setup. The rise time and the voltage overshoots confirm that the calculation of the parasitic inductances of the PCB traces reflects the reality. The only difference on the drain-source voltages is the ringing present on the simulation. It is not visible in the real measurement since its frequency is around 400 MHz, above the bandwidth of the differential probes used to perform this measurement. However, this ringing is due to the interaction of the stray inductance of the GaN and the output capacitance C_{oss}. The output current has been increased to evaluate the voltage overshoot across the GaN HEMTs. Starting from 5 A up to 30 , the voltage overshoot across S_1 has been measured from the validated simulation model with the nominal DC-link voltage of 350 V. The maximum overshoot occurs with $I_{DS} = 30$ A and it is equal to $V_{DS,peak} = 387.5$ V, namely 10% more than the nominal voltage.



(a)



(b)

Fig. 3.18: Result of the switching test in DC/DC configuration: in textit(a) from the LTSpice model while in *(b)* from the experimental setup.

The overshoot in the drain-source voltage has been analysed in the experimental setup as well. The drain-source voltage has been varied between 60 V and 150 V and the drain current from 1 A to 5 A. These low parameter has been used since this test has been performed prior the validation of the entire system. From this test, has turned out that the voltage overshoot decreased with the increasing of the drain-source voltage, as it is shown in Fig. 3.19. Moreover, the trend of the measured values can be approximated better as linear for voltage higher than 100 V. This behaviour can find an explanation looking at the behaviour of the parasitic capacitances of the GaN

HEMT at the variation of the voltage. As it can be seen in Fig. 3.20, the output capacitance decreases with the increasing of the drain-source voltage and this means that, the oscillations generated by the resonant tank composed by the stray inductance of the devices and such capacitance are smaller in amplitude for lower capacitance value. This means that any forecast about the voltage overshoot is more reliable for voltage higher than 100 V for this specific case.

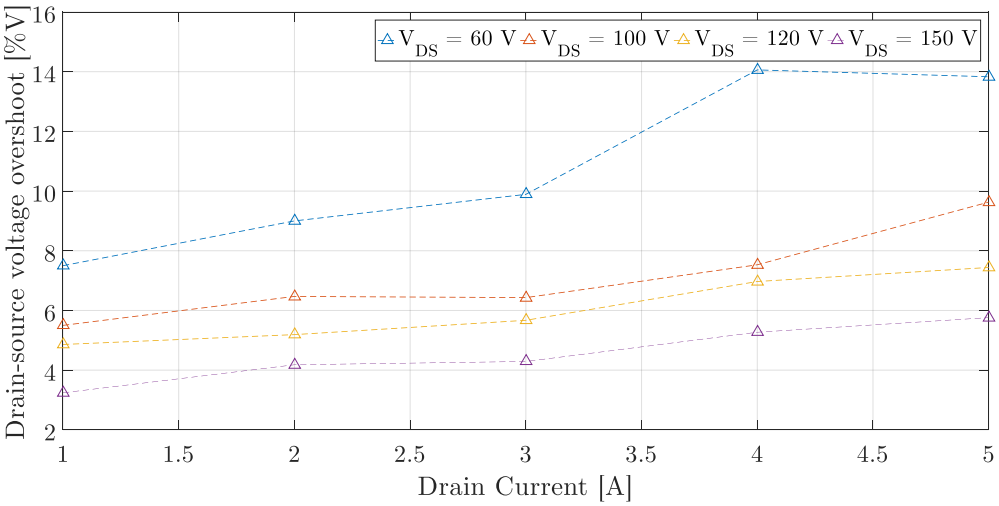


Fig. 3.19: Trend of the voltage overshoot increasing the drain current and the drain-source voltage.

Common-mode analysis

Due to the overlapping of the inner layers of the proposed PCB arrangement, a common mode analysis have been done and presented in [4]. In the previous work, the capacitance created by the overlap of two gate driver's ground plane was calculated. The four capacitances identified are calculated with the formula:

$$C_S = \frac{A \cdot k \cdot \epsilon_0}{d} \tag{3.31}$$

where A is the area of the gate drivers ground planes, k is the dielectric constant of FR4, ϵ_0 the permittivity of air and d is the thickness of the FR4 layer. In the presented work, a thin layer stack with $d = 0.127\ mm$ was used, while in this thesis a thicker layer stack with $d = 0.44\ mm$ has been selected. The old and the updated values are

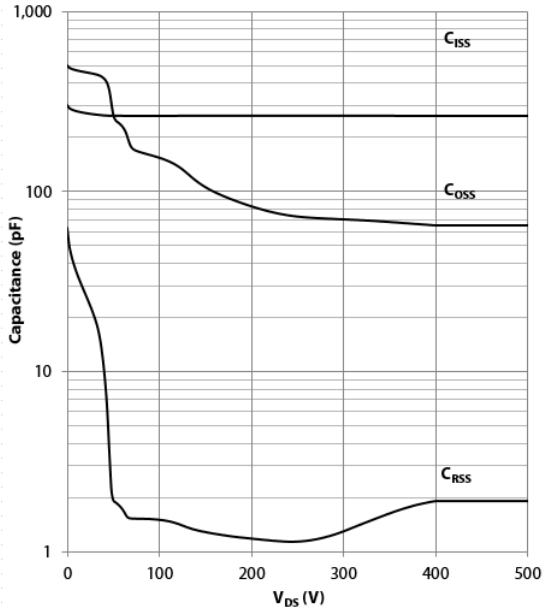


Fig. 3.20: Parasitic capacitances of the GS66508T for different drain-source voltages [15].

listed in Table 3.6 and one can see that the capacitance in the new solution are almost 8.5 times smaller than the previous solution. A new common-mode analysis has been performed, using the circuit in Fig. 3.21. The result of this simulation is shown in Fig 3.22 and when compared with the results shown in [4], the common-mode current amplitude is greatly improved.

	Layer stack used in [4]	**New layer stack**
$\mathbf{C_{S1}}$	57.4 pF	16.5 pF
$\mathbf{C_{S2}}$	43 pF	12.4 pF
$\mathbf{C_{S3}}$	44.7 pF	12.9 pF
$\mathbf{C_{S4}}$	17 pF	4.7 pF

Tab. 3.6: Summary of the previous and updated coupling capacitances.

Beside the coupling capacitance reduction, in a possible design update also the isolated DC/DC converters can be updated. Indeed, at the moment are available on the market isolated converter with a capacitance of 10 pF as maximum value [39] in contrast to the 30 pF of the used solution. This would mean that the common-mode current that can flow through the non-isolated side is reduced and the logic circuit would not be affected by cross-talking between the overlapped devices.

Another potential path for the circulation of common-mode currents is the capaci-

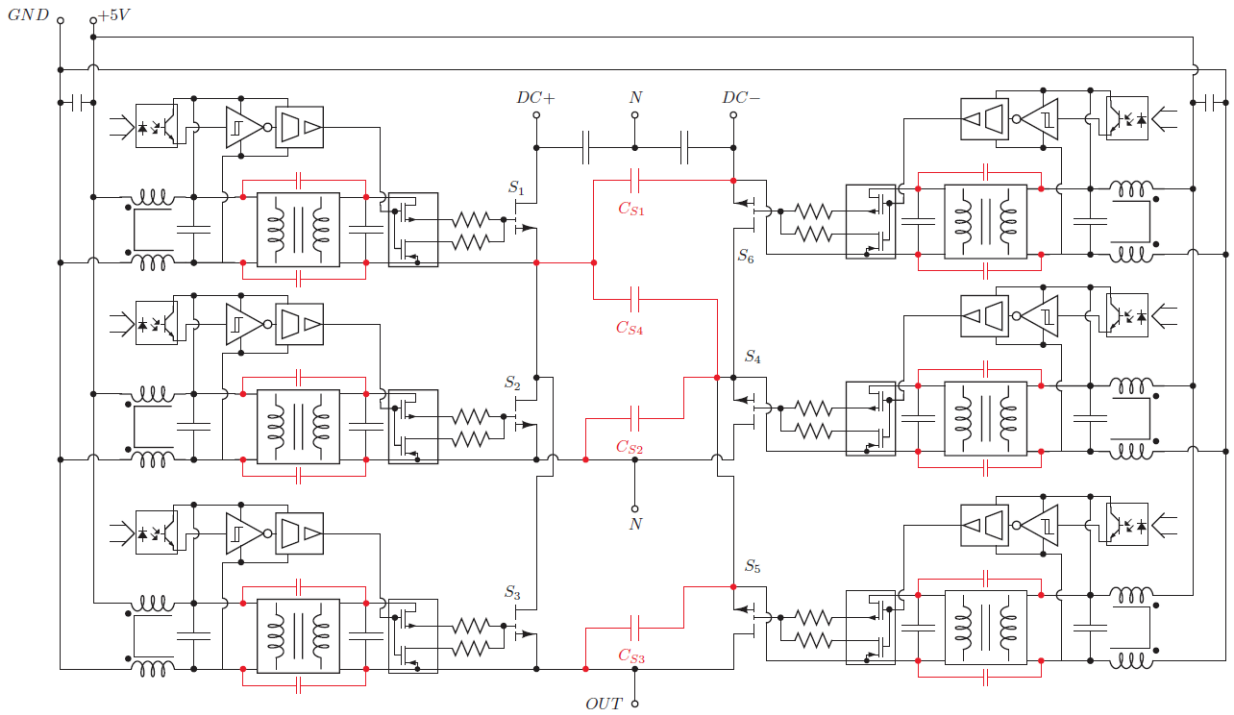


Fig. 3.21: Common-mode analysis equivalent circuit [4].

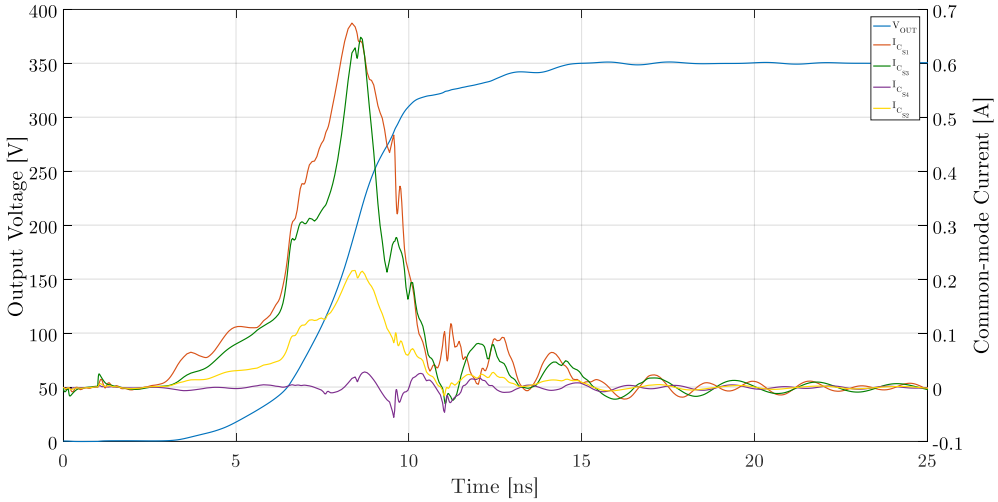


Fig. 3.22: Common-mode analysis result with the new set of coupling capacitances.

tive coupling between the heatsinks and the GaN HEMTs, having the TIM as dielectric. In this thesis, the SilPad2000 from Bergquist as been selected as TIM, looking at the best thermal conductivity while having the lowest coupling capacitance possible. Using the parameters given for such TIM of Table. 3.7, the parasitic capacitance has been

Thickness	0.38	mm
Continuous temperature	-60 to 200	$°C$
$V_{breakdown}$	4	kV_{rms}
Dielectric constant	4	
Volume resistivity	10^{11}	$\Omega \cdot m$
Thermal conductivity	3.5	$^{W}/_{m \cdot K}$

Tab. 3.7: Bergquist SilPad-2000 characteristics [40].

calculated as:

$$C_{Sx} = \frac{A \cdot k \cdot \epsilon_0}{d} = 1.87\ pF \tag{3.32}$$

From the arrangement depicted in Fig. 3.23, an equivalent electrical circuit can be drawn. Such circuit is shown in Fig. 3.24, where the blue components indicate the parasitic elements and the two heatsinks. For a step in the output voltage, the current that flows in each capacitor has been analysed in two cases: with grounded and ungrounded heatsinks. From the simulation test it has emerged that even though in case of grounded heatsink the peak of the common mode current is higher than in the ungrounded heatsink, there is no current flowing through the capacitances related to the switched S_6 and S_4, which are in this case turned off. This means that grounding the heatsink might be relevant in reducing the flow of common mode current through devices in opposite state of gate voltage. The result of this analysis is shown in Fig. 3.25a and Fig. 3.25b for the grounded and ungrounded heatsink respectively.

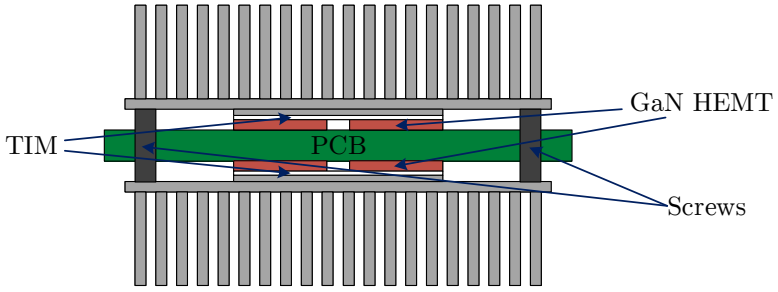


Fig. 3.23: Joint view of the heatsinks, the TIM and the GaN HEMT.

Among the aims of this project, there is the evaluation of the compactness performance of the GaN-based 3L-ANPC. In the following, the several aspects that have a relevant impact on the inverter volume are analysed and the results are compared for different switching frequencies.

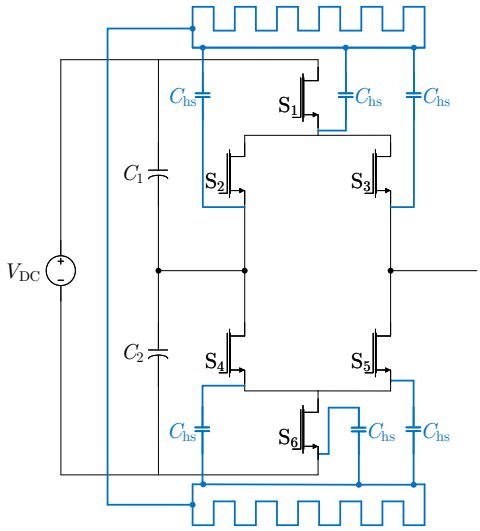
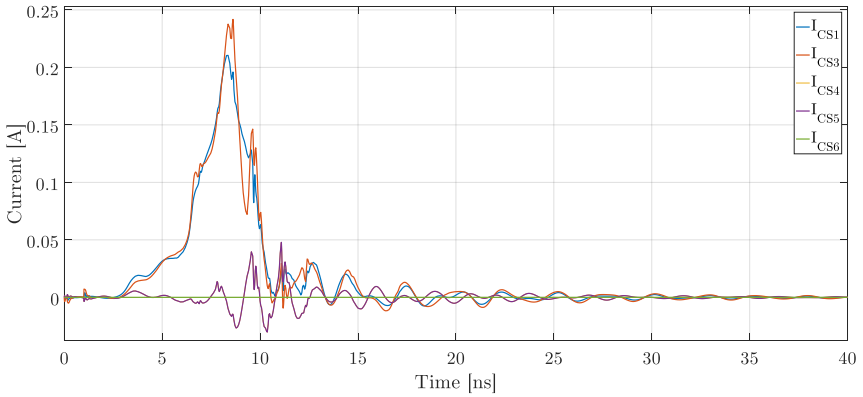
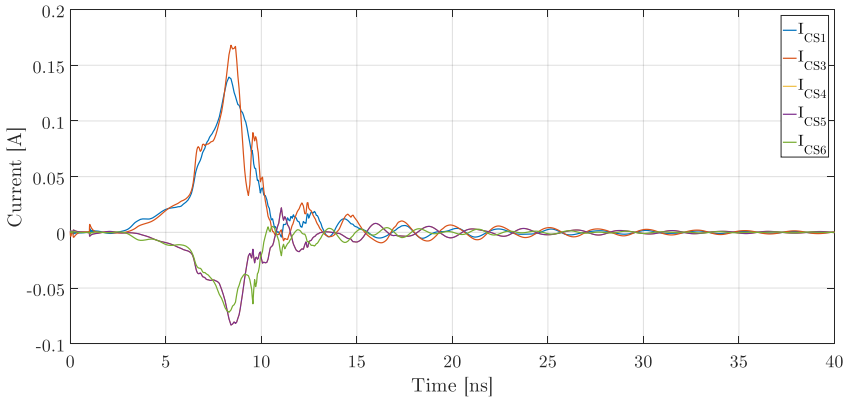


Fig. 3.24: Simplified schematic of the capacitive coupling between the GaN HEMTs and the heat sinks. The heat sinks and the equivalent capacitances are highlighted in blue.



(a)



(b)

Fig. 3.25: Common-mode current analysis in the capacitive coupling between switches and heatsinks. In *(a)* the heatsink has been connected to ground while in *(b)* is ungrounded.

Chapter 4

Performance Assessment

In this chapter, the core of the thesis work results are presented. The performance assessment goes through the simulation results first, where all the power levels are analysed in both single-phase and three-phase. Lastly, the chapter is closed with the presentation of experimental results that validate both the electrical and the thermal model developed in PLECS and used in the simulation work.

4.1 Simulation Results

In this chapter the performance of both single-phase and three-phase 3L-ANPC inverter are assessed by means simulation analysis. The aim of this assessment is to evaluate how the efficiency, power losses distribution and junction temperatures vary, varying the output power. Due to the symmetry of the 3L-ANPC structure, the power loss and junction temperature has been analysed for only the upper switches, i.e. S_1, S_2 and S_3. Since several aspect are valid in both single and three-phase, some of the consideration exposed in single-phase are naturally extended to three-phase.

Before proceeding with the analysis of the inverter operation mode, a consideration about the dead-time has to be pointed out. As known, on the sinusoidal operation the dead-time has a strong impact on the distortion of the output current. Indeed, if it is too large, a voltage error and a high amount of 5^{th} harmonic can be present. Increasing the switching frequency this effect is enhanced, making necessary a compensation of this effect. Such compensation can be open-loop based or feedback based. In this

thesis, the open-loop compensation has been adopted, and it is calculated as:

$$m_i = \frac{2 \cdot \widehat{V}_{line}}{V_{DC}} \cdot cos(\omega t) \tag{4.1}$$

and becomes, after the insertion of the compensation term:

$$m_{i,comp} = \frac{2 \cdot \widehat{V}_{line} \cdot \left(1 + 2 \cdot \frac{t_d}{T_{sw}}\right)}{V_{DC}} \cdot cos(\omega t) \tag{4.2}$$

It is worth to point out that the compensation is effective only below $f_{sw} < 150\ kHz$, above which the modulation index becomes greater than one. This suggest that, in case the switching frequency has to be increased above this range, the dead-time has to be decreased. The decreasing of the dead-time involves the reduction of switching times, introducing more challenges from the EMI point of view.

In the following analysis, the inverter performance is evaluated varying the output power and keeping the switching frequency as 50 kHz.

4.1.1 Single-Phase Operation

This section is focused on the performance assessment of the single-phase operation with the modulation strategy proposed in [16]. The output voltage and current at the nominal power of 5 kW and switching frequency of 50 kHz are shown in Fig. 4.1. The RMS value of the output voltage is 230 V_{RMS} and this confirms that the dead-time compensation is effective without leading to overmodulation. From the output current distortion point of view, the THD of the current with the designed LC filter is 1%. It is higher than the THD calculated analytically in Sec. 3.3 due to the introduction of the DC-link oscillations, the dead-time and the voltage drop across the devices. Regarding the DC-link voltage oscillations, the designed DC-link capacitance has been included in the simulation model and the voltage ripple of 14.5 V_{pp} respects the design constraint of 5% of half DC-link voltage.

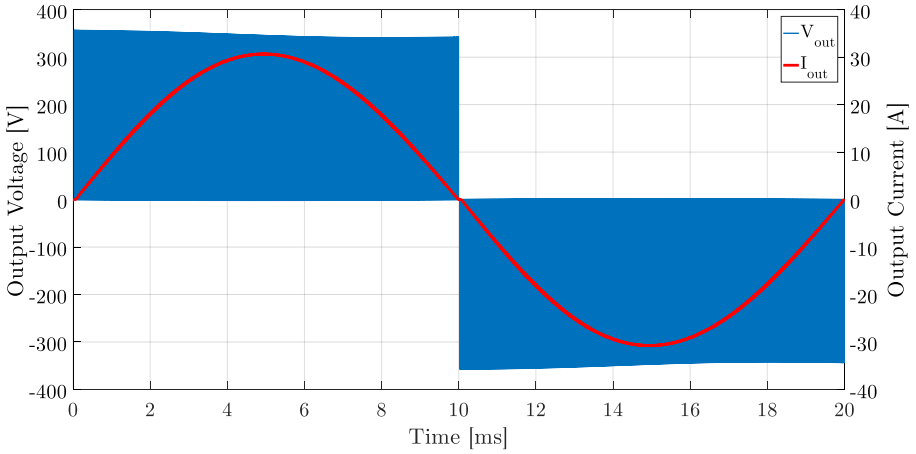


Fig. 4.1: Output voltage and current in single-phase operation at the nominal power of 5 kW and $f_{sw} = 50\ kHz$.

The efficiency of the inverter has been evaluated varying the output power. Increasing the output power, the efficiency drops from almost 99% of 1 kW power to 95% at nominal power. The main responsible of this degradation in performance are the conduction losses, which are predominant at high output power. Indeed, this can be seen in Fig. 4.3 where the losses composition has been plotted. The trend of the inverter efficiency at the variation of the output power is shown in Fig. 4.2.

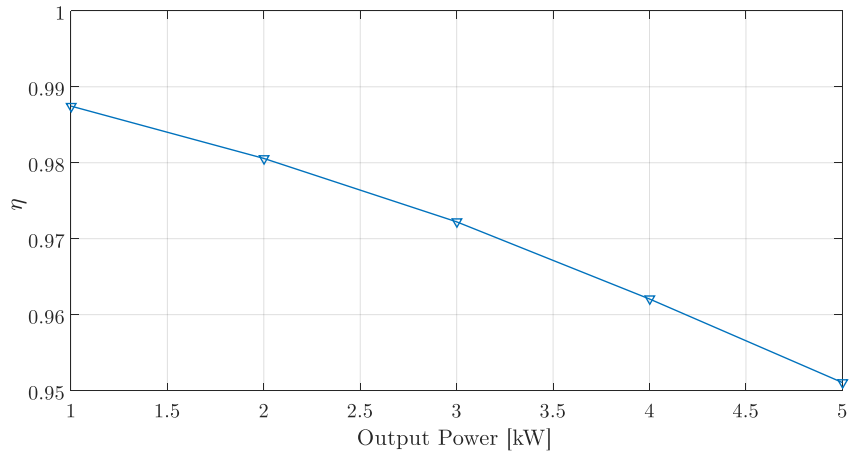


Fig. 4.2: Trend of inverter efficiency varying the output power. The switching frequency in this case is 50 kHz

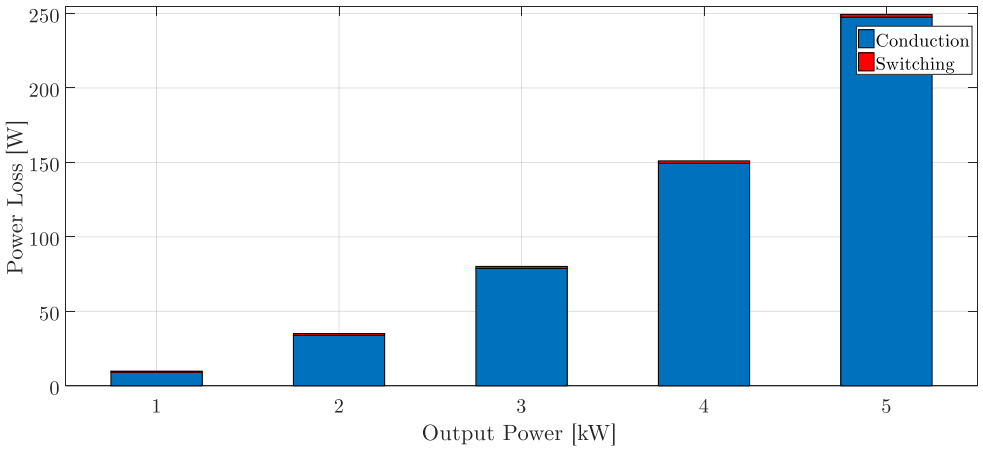


Fig. 4.3: Power losses at the different power levels. The loss part of conduction and switching loss is differentiated.

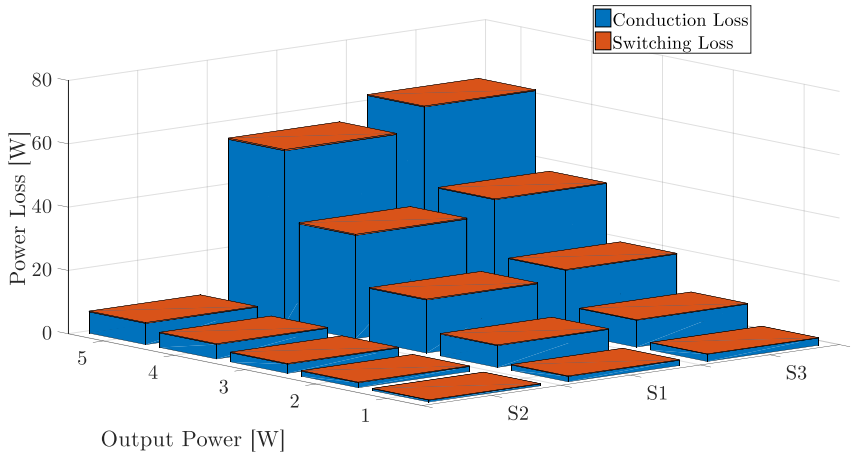


Fig. 4.4: Power losses distribution among the upper switches S_1 S_2 and S_3.

An aspect that is worth to be analysed is how the losses are distributed among the switches. The switches that are involved in the biggest part of the losses are S_1 and S_3, while S_2 is the least lossy, as shown in Fig. 4.4, and this discrepancy increases along with the output power. This reflects a limitation of the modulation strategy at high power, which helps in reducing the losses but is weak from the distribution point of view. This is confirmed also by the mean junction temperature and its variation, shown in Fig. 4.5 and 4.6 respectively. As can be seen, S_1 and S_3 are the most stressed and this makes them the devices most likely inclined to failure than S_2. This aspect can be

improved by implementing different modulation strategies, such as the one proposed in [41] which allows to evenly distribute the stress among the three switches by introducing a modulation of S_2 (or S_5) during the negative half-cycle (or positive half-cycle).

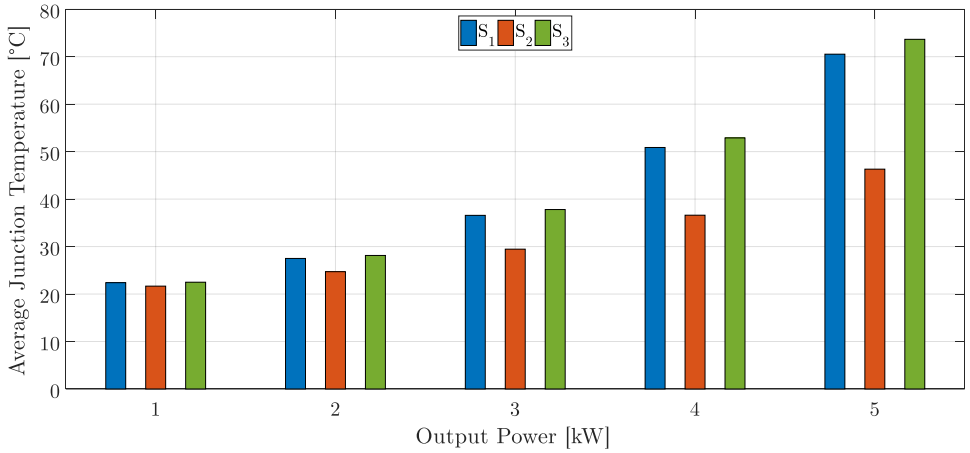


Fig. 4.5: Average junction temperature of the upper switches S_1 S_2 and S_3 varying the output power.

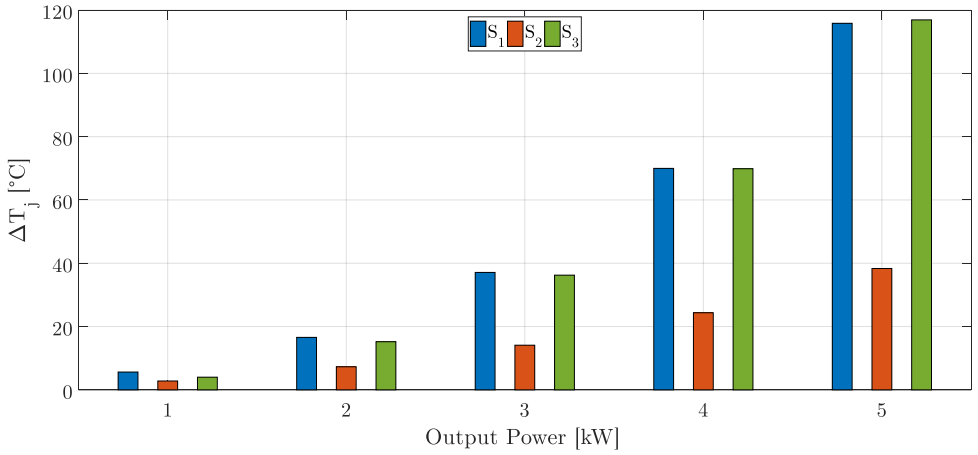


Fig. 4.6: Junction temperature variation of the upper switches S_1 S_2 and S_3 varying the output power.

The variation of the efficiency varying the output power and the switching frequency is shown in Fig. 4.7. As expected, the increasing of both switching frequency and output power degrade the efficiency. The peculiar aspect is that at high power,

the effect of increasing the switching frequency has a small impact on the efficiency degradation, due to the predominance of the conduction losses over the switching ones.

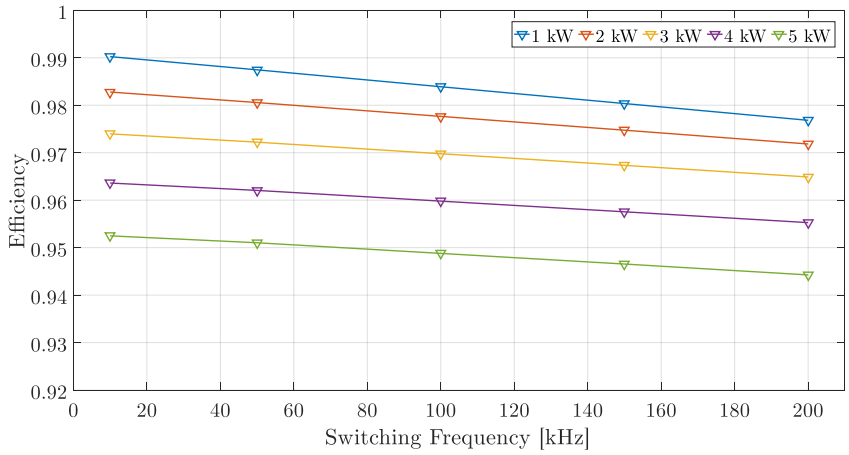


Fig. 4.7: Efficiency variation for output power and switching frequency increasing.

4.1.2 Three-Phase Operation

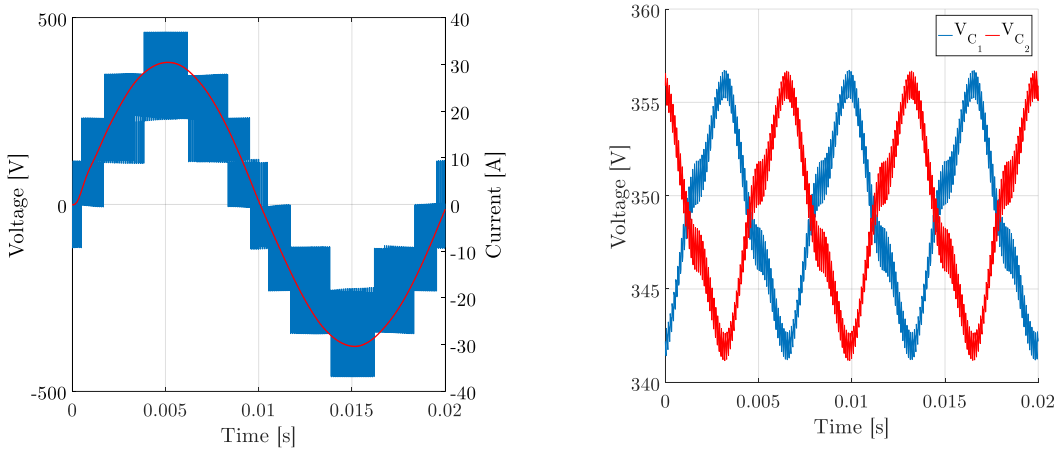
The performance analysis in three-phase operation mode has been carried out comparing the three different modulation techniques keeping the same power and switching frequency. This choice has been made in order to identify which has the best performance in terms of output distortion, DC-link buffer volume, losses and thermal stress on the components. In particular, each assessment is focused on a single leg assuming that the same behaviour can be extended to the remaining phases.

The first part of this assessment is related to the electrical performances. This assessment is conducted at the nominal condition (i.e. 5 kW $f_{sw} = 50$ kHz) for the three modulation strategies considered: SVM, VSVM and Optimized VSVM. In order to compare the performances of the three modulation techniques, several figures of merit are taken into account. The first is related to the output current quality evaluating the THD with the designed LC filter. The lowest current distortion is obtained with the SVM with a THD of 0.422%, result that is in accordance with what discussed in Sec. 2.3.2. Regarding the DC-link voltage oscillations, the simulations have been ran with the same DC-link capacitance of 200 μF, which is the value calculated for the worse case scenario of SVM. In this case, the best performances are obtained with the VSVM, which allows to have a voltage ripple of 0.5% of the nominal DC bus voltage. Thus,

	SVM	**VSVM**	**Optimized VSVM**
$\mathbf{THD_i}$ [%]	0.422	1.37	0.38
$\mathbf{\Delta V_{DC}}$ $[\mathbf{V_{pp}}]$	14.16	1.821	4.723
$\mathbf{C_{DC}}$ $[\mu F]$	200	200	200
η [%]	95.10	94.99	95.04

Tab. 4.1: Summary of the modulation techniques performance comparison.

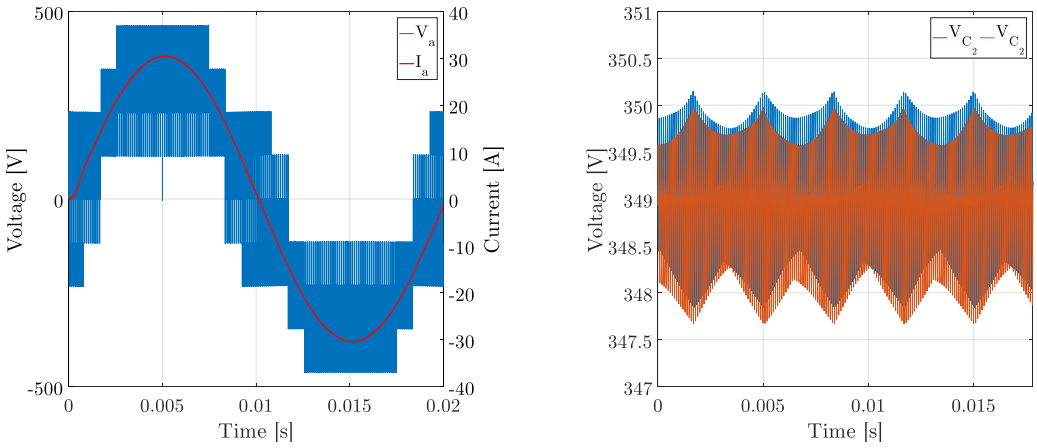
this implies that choosing this modulation technique the DC-link capacitance can be reduced by at least ten times. The last performance figure of merit evaluated is the efficiency. The variation between the modulation techniques is slight: 95.10% for the SVM, 94.99% for VSVM and 95.04 for Optimized VSVM. To sum up, the performances of the SVM and Optimized VSVM are almost equivalent in terms of output distortion and efficiency, while the simple VSVM has worse performances in these senses. On the other hand, the VSVM allows to sensibly reduce the DC buffer size. All the evaluated parameters are summed up in Table 4.1, while the output quantities along with the DC-link voltage oscillations are shown in Fig. 4.8, 4.9 and 4.10 respectively. The second



(a) **(b)**

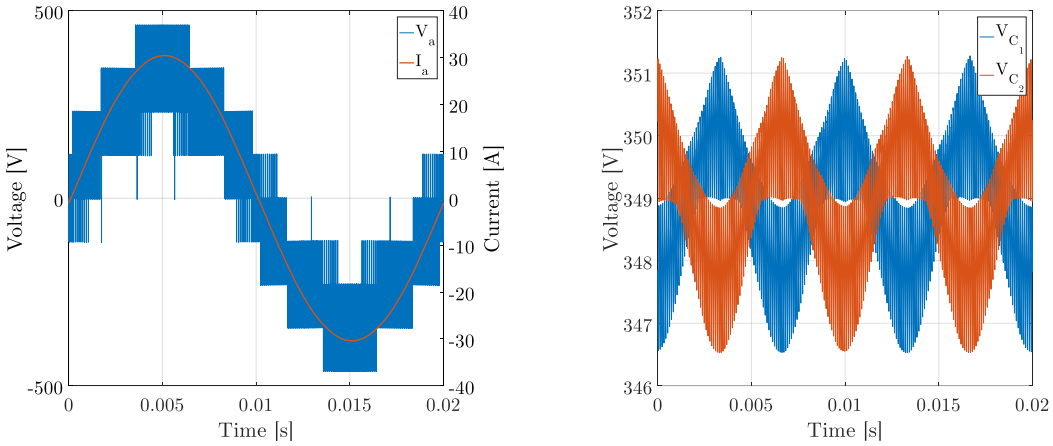
Fig. 4.8: Space Vector Modulation waveforms. In *(a)*, the phase voltage and current and in *(b)* the DC-link voltage oscillations.

part is related to the losses and thermal stress analysis for the different modulation techniques. As the previous part of the assessment, the output power is kept as nominal with a switching frequency of 50 kHz in order to simplify the analysis and identify the most effective modulation. As the efficiencies suggest, the modulation with the lowest



(a) **(b)**

Fig. 4.9: Virtual Space Vector Modulation waveforms. In *(a)*, the phase voltage and current and in *(b)* the DC-link voltage oscillations.



(a) **(b)**

Fig. 4.10: Optimized VSVM waveforms. In *(a)*, the phase voltage and current and in *(b)* the DC-link voltage oscillations.

losses is the SVM. Particularly, the conduction losses of SVM and Optimized VSVM are slightly different, while in the VSVM both conduction and switching losses are higher compared to the other two techniques. This results are summarized in Fig. 4.11.

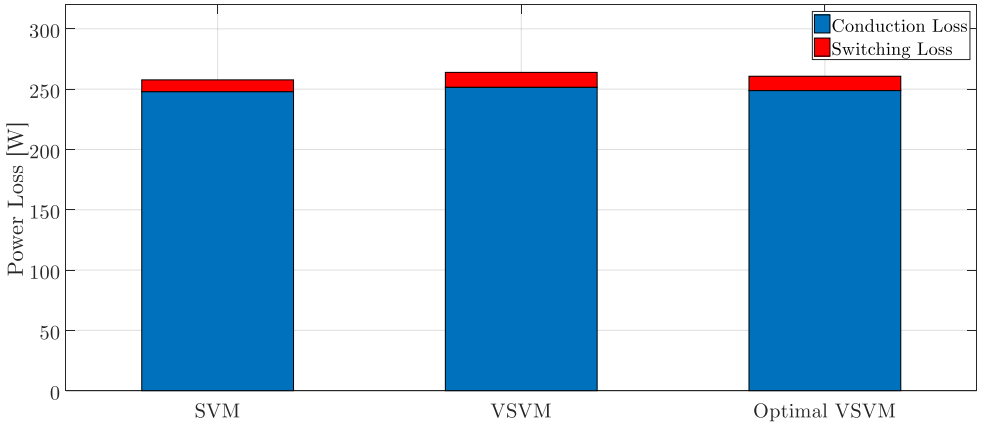


Fig. 4.11: Losses comparison between the modulation techniques at nominal power and $f_{sw} = 50\ kHz$.

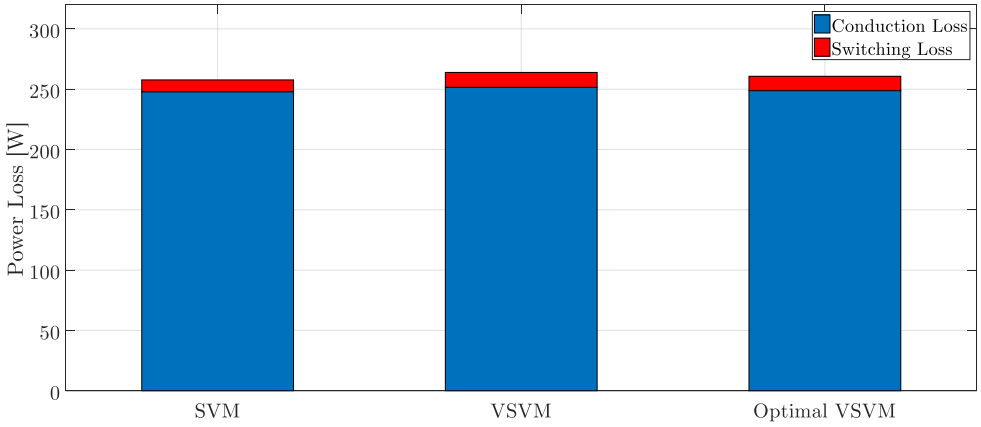


Fig. 4.12: Losses distribution among the upper-side switches S_1,S_2 and S_3 at nominal power and $f_{sw} = 50\ kHz$.

The losses distribution is useful to understand how the stress is distributed among the switches. The data shown in Fig. 4.12 underline the same weakness recorded in single-phase operation mode, namely that losses are mostly concentrated on S_1 and S_3, leaving S_2 with the lower amount of both switching and conduction losses. This happens for all the modulation techniques, with a slight variation in that follows the trend of shown in Fig. 4.11, where the SVM is the most efficient. A better way to clarify how the stress is distributed among the switches is to analyse the average junction temperature and its variation ΔT_j over one fundamental cycle. As can be seen from Fig. 4.13,

the VSVM is the modulation that involves the highest thermal stress on S_1 and S_3 when compared to the others, while S_2 has the same mean junction temperature in all the three cases. The last figure of merit of relevance from the reliability point of view is the junction temperature variation. In Fig. 4.14 the three cases are shown, and it results clear that from this point of view the least stressful modulation is the Optimal VSVM with the lowest ΔT_j for the most stressed devices. On the other hand, the temperature difference of S_2 is the highest compared to the other strategies, even though the difference between the latter switch is still huge. From this point of view, the SVM and VSVM are comparable regarding the stress on S_1 and S_3, while in the SVM the stress on S_2 is the lowest.

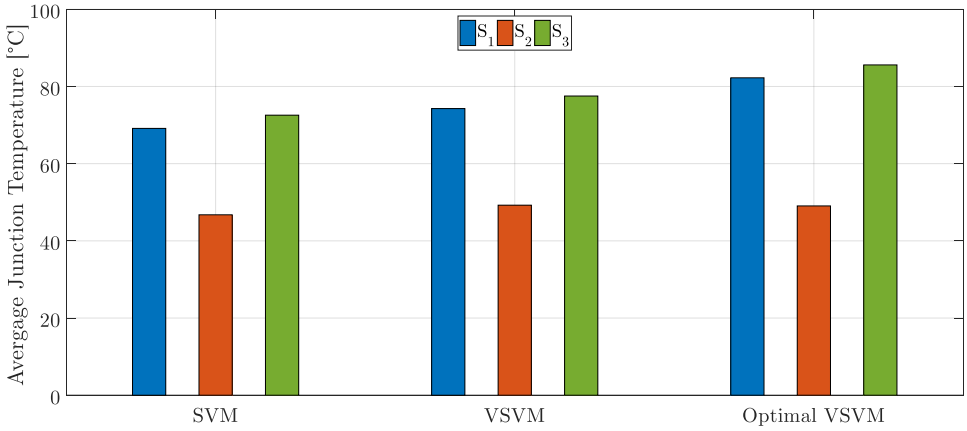


Fig. 4.13: Average junction temperature on the upper-side switches of each leg. It is plotted for the different modulation techniques.

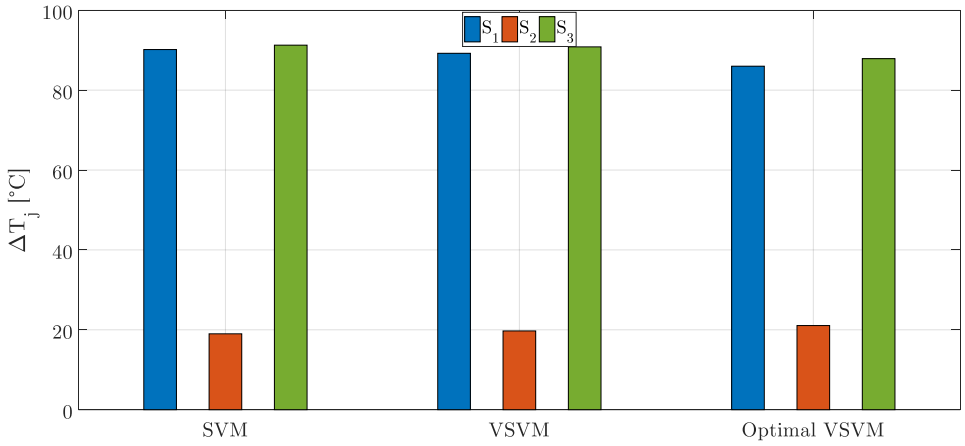


Fig. 4.14: Temperature stress in terms of ΔT_j for the different modulation strategies and the considered switches of each leg.

4.2 Test-rig Description

The test-rig has been built in the Student Electrical Laboratory in Aalborg University. The system is composed by a DC supply from Delta Elektronika, with a maximum voltage of 600 V and current of 10 A. The low voltage boards, such as optical interfaces, gate driver and cooling system, are supplied via a low-voltage laboratory supply with isolated outputs. As load, a parallel-connected system of resistor has been used, where each resistor can withstand a maximum current of 10 A. The temperature measurement has been performed using an EtherCAT-based OpSens equipment with low-frequency optical fibres. Both the DSP and the OpSens interface are controlled through PC. The whole system is summarized in the functional schematic of Fig. 4.15 In the following subsections, the details of the cooling system and the over-current protection are given.

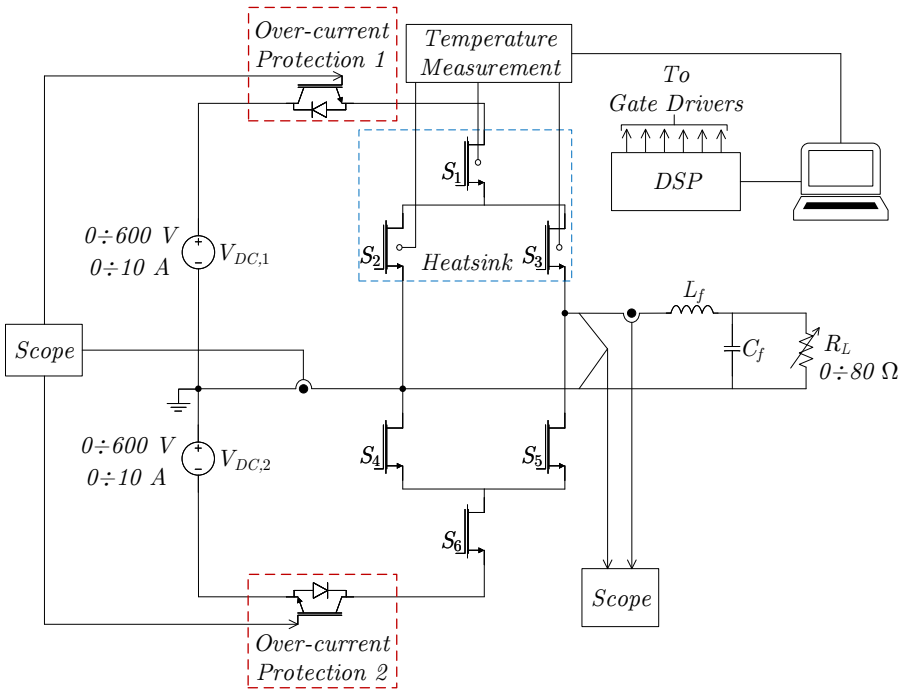


Fig. 4.15: Functional schematic of the test-rig employed in the experiments.

4.2.1 Cooling System

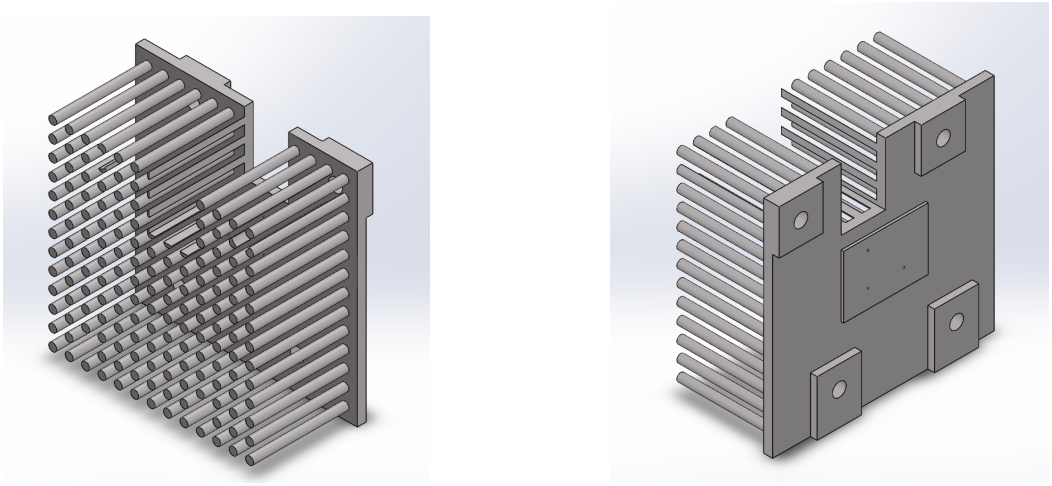
As stated in Sec. 3.1, in order to operate the designed inverter at high power, a cooling system is needed. The GaN HEMT employed in this project are top-cooled, through a surface which is electrically connected to the source pin. For this reason, the heatsink must be interfaced with the transistors through a Thermal Interface Material (**TIM**), in order to guarantee thermal connection avoiding any electrical contact. More details about the TIM selection are given in the following. Since the transistors are placed on the two sides of the PCB, two heatsinks are necessary. To fix them on the PCB, the holes of the bottom-side heat-sink are threaded allowing the two heat-sinks to be fixed together.

Beside the thermal and electrical constraints, also the geometrical aspects must be taken into account during the selection of the proper heat-sink. Moreover, the selected heatsink must be customized to better fit with the PCB and the components. Given the available space on the PCB, the maximum length and width of the horizontal area is defined as $50 \times 50\ mm$. Regarding the height, the solution available on the market at the moment is $25\ mm$ with 169 cylindrical fins. Since the heatsink covers the gate

Dimensions	$50x50x10.5\ mm$
Flow rate	$19\ {}^{m^3}/_{h}$
Supply voltage	$12\ V$
Power consumption	$1.44\ W$

Tab. 4.2: Fan characteristics.

driver components, which are taller than the GaN HEMT, the contact interface must be extruded from the bottom of the heatsink. Lastly, the temperature measurement is a key part of this thesis. To perform it, optical thermal transducer are used, and three holes of 1 mm diameter are realized on both the heatsink and the TIM. The customized heatsink is shown in Fig. 4.16 in two different projections. To provide an adequately low thermal resistance, the heatsinks are paired with two fans, whose characteristics are give in Table 4.2. This combination of fan plus heatsink does not allow to carry out experiments at the full power of 5 kW , since the total thermal resistance is around $0.75{}^{K}/_{W}$, which is higher than the one requested for the nominal power.

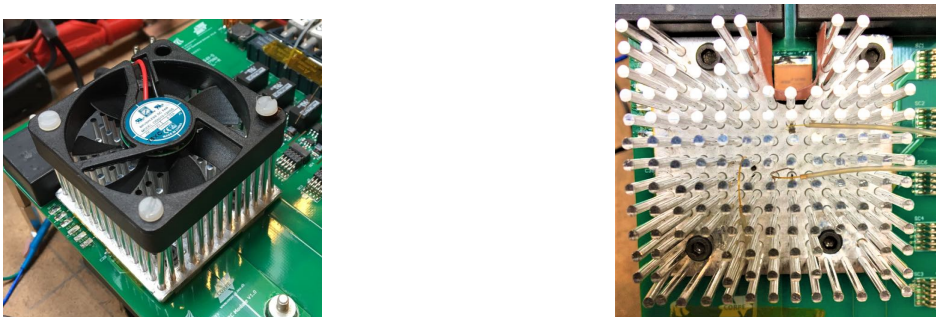


(a) **(b)**

Fig. 4.16: Two views of the customized heat-sink: *(a)* top view and *(b)* bottom view.

As emerged from the common-mode analysis of Sec. 3.4.4, the thermal interface material acts as dielectric between the heatsink and the top-cooling surface of the GaNs. Therefore, a trade-off to maximise the thermal flux and reduce the common-mode current amplitude is necessary and the Bergquist Sil-Pad2000 has been selected and employed in the actual cooling system, and its parameters are given in Table 3.7. The proposed cooling system along with the arrangement of the temperature measurement

are shown in Fig. 4.17a and 4.17b.



(a) **(b)**

Fig. 4.17: Picture of the overall cooling system in *(a)* and a detail of the temperature measurement in *(b)*.

4.2.2 Over-current Protection

In order to carry out the experiments in a safe way, an over-current protection has been developed. Basically, this protection is composed by two high-power IGBTs (i.e. 1.2 kV,80 A) which are connected in series between the DC-link capacitors and the converter board. These IGBTs are normally on during regular operations and turned-off when a fault occurs. The state of the IGBTs is controlled by the output trigger of an oscilloscope. This choice has been made in order to provide maximum flexibility in the selection of the maximum current threshold and to keep the overall system as simple as possible.

The oscilloscope signal is a step which is kept on until the oscilloscope is set to single shot waiting for a new trigger signal. This would mean that, if the oscilloscope had direct control on the IGBT state, it may close the circuit when the fault is still present. To overcome this issue, a manual reset of the fault has been provided. The flip-flop can be reset in two ways: through manual push button or with a signal from the digital controller. The latter is isolated from the protection board through optical fibre cable. Beside the control of the IGBTs state, the output of the latch is connected to the digital controller, in order to stop the modulation and reset the generation of the reference signal. Moreover, two status led indicate whether a fault has been detected or the system can run in case of normal conditions.

From the implementation point of view, the latch flip-flop has been realized using two CMOS-based NAND logic gates. Additionally, all the signals from and to the DSP

are delivered through optical fibre and the oscilloscope is separated from the power stage through an optical isolated gate driver. The gate driver on the power side is supplied by a step-up isolated DC/DC converter, which steps the voltage from the 5 V of the logical circuit to the 15 V of the gate driver. A functional scheme of the overall system is shown in Fig. 4.18 and a picture of one board is presented in Fig. 4.19.

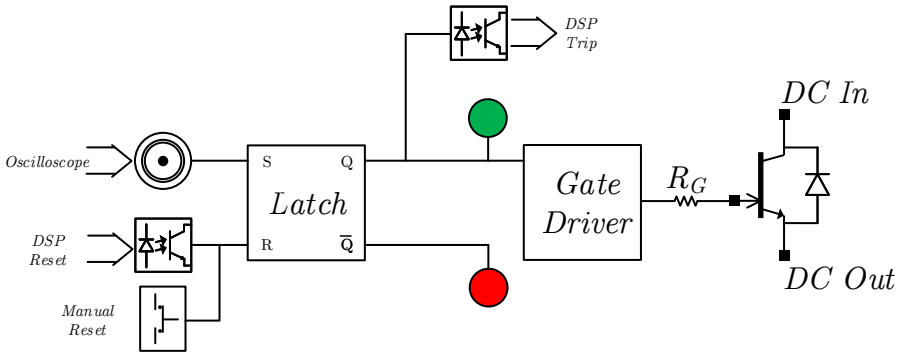


Fig. 4.18: Functional scheme of the designed over-current protection.

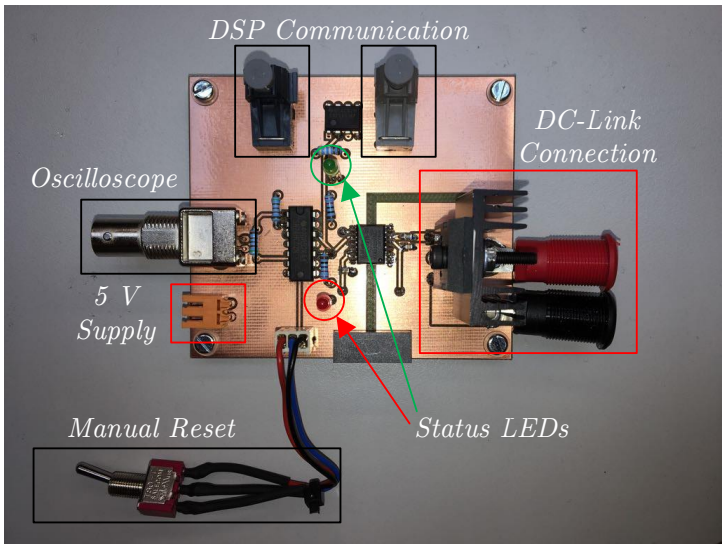


Fig. 4.19: Picture of the over-current protection board.

4.3 Experimental Results

4.3.1 DC/DC Test

As anticipated in Sec. 4.3.1, the first tests of the converter operation have been performed in synchronous buck converter. In this cases, the switches used are S_4 and S_6, while S_5 has been short-circuited in order to avoid that the high temperature caused by the continuous conduction of the latter would affect the temperature measurement. Such tests have been carried out in two conditions: the first with the aim of evaluating the temperature behaviour and the switching losses impact and the second to evaluate the switching performances of the converter. The first test has been conducted varying the load and the switching frequency. The load has been varied in order to obtain output currents from 3 to 5 A with a DC-link voltage of 100 V, duty cycle of 0.5 and switching frequencies of 25 and 50 kHz. During this test, the case temperature of the involved switches have been measured and plotted in Fig. 4.20. As it can be seen, since the switching and conduction losses are supposed to be equally distributed between the two switches due to the duty cycle of 0.5, there is a important difference in the two temperatures. To avoid that this difference would be amplified by the temperature offset between the two optical probes, such offset has been compensated in the measurement equipment. Therefore, the reason of this relevant difference can be addressed to the different copper traces where the two switches are landed. Indeed, the switch with the higher case temperature is S_4, is placed on a smaller copper trace compared to S_6, which is soldered on a copper trace which includes all the negative DC rail and the CeraLink capacitors. Additionally, the switching frequency has been doubled from 25 to 50 kHz and the temperature has an irrelevant variation, which has not been plotted to keep the readability of the plot clear. Despite the low impact of the switching losses on the temperature rising, it results clear that a cooling system is crucial for the proper functioning of the converter. Indeed, with only 5 A of output current, the case temperature of the hotter device reaches 124°C which may result in a junction temperature highly likely close to the maximum allowed temperature of 150°C.

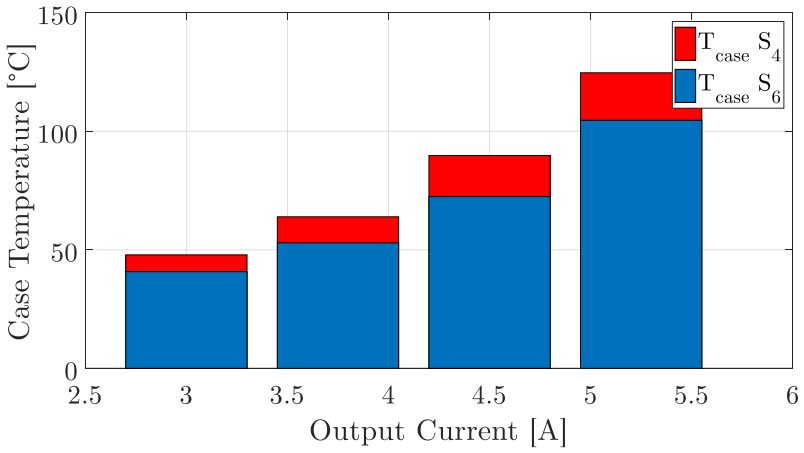
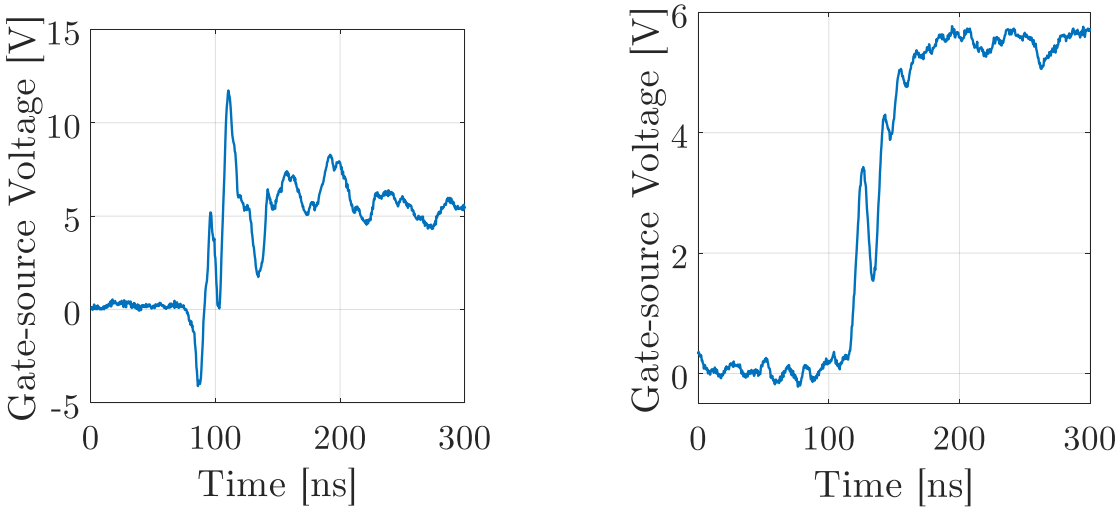


Fig. 4.20: Temperature trend varying the output current in synchronous buck configuration. The DC-link voltage is 100 V and the switching frequency is 50 kHz.

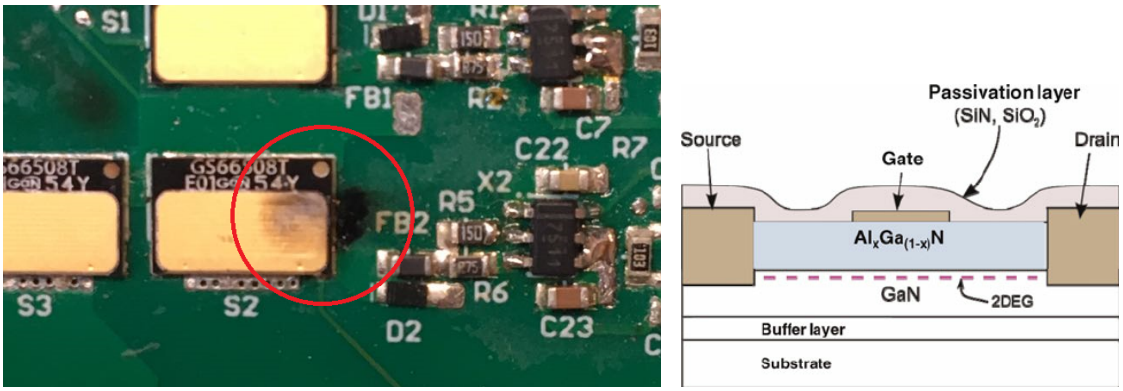
While performing this test, several failure have happened on the gate of the GaN HEMT. The result of this failure is a short-circuiting of the gate-source and it is visually identifiable by a burnt part, as shown in Fig. 4.22a. This failures have been investigated and the cause has been addressed to the type of differential probe used. When the failure happened, the differential probe was an high-voltage probe P5200A from Tektronix. The cause is that such probe introduce a small load seen on the gate-source terminal, leading to oscillations of high amplitude on the rising edge of V_{GS}, as shown in Fig. 4.21a. Looking at the overshoot of the gate voltage, it results clear that it goes way above the maximum allowed voltage of 10 V leading to failure of the devices. Therefore, a different probe solution have been adopted, opting for a optically isolated differential probe which provides almost no-load on the gate-source pins and leading to the V_{GS} waveform of Fig. 4.21b. Both measurement have been performed with several V_{DS} voltages but hereafter only the case of $V_{DS} = 125\ V$ is shown.

Regarding the mentioned second test, the configuration has been changed introducing an output inductance of 915 μH, in order to smooth the output current and evaluate the behaviour of the converter while switching inductive currents. This test has been carried out with the introduction of the heatsink described in Subsec. 4.2.1 and the temperature has been monitored to avoid overheating of the devices. The output current along with the switches drain-source voltages are shown in Fig. 4.23, from where the ability of the converter to operate with an output power of 1 kW at 400 V_{DC} can be appreciated.



(a) **(b)**

Fig. 4.21: Gate-source voltages measured with a non-isolated differential probe Tektronix P5200A(*(a)*) and isolated differential probe LeCroy HVFO103(*(b)*).



(a) **(b)**

Fig. 4.22: Picture of the failed device (*(a)*) along with a generic structure of a GaN HEMT in *(b)* [42]. The structure indicates that the burnt part is in correspondence of the gate layer.

Analysing the gate-source voltage, high oscillations have been measured and shown in Fig. 4.24a. These high oscillations may resemble a Miller turn-on, since they happens after the dead-time when the other device is turning on. These oscillations have been investigated and different turn-off resistor have been tried, along with small capacitances across gate and source, being ineffective. A further investigation of the problem has been carried out measuring connecting both the two tips of the differential

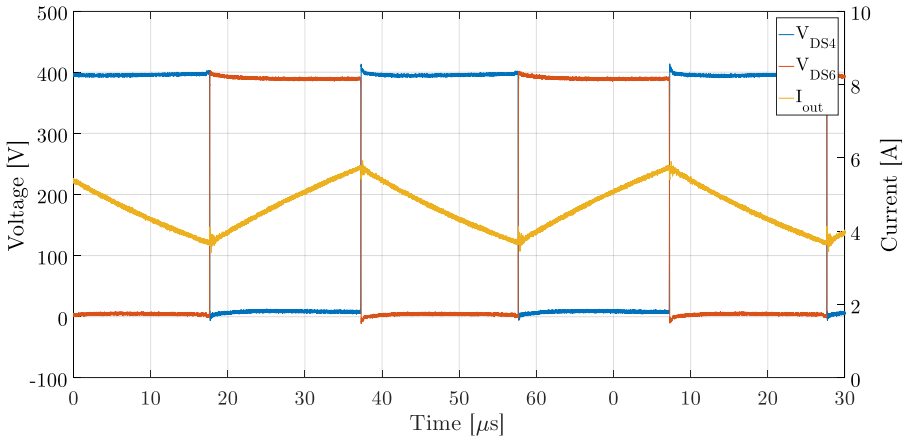


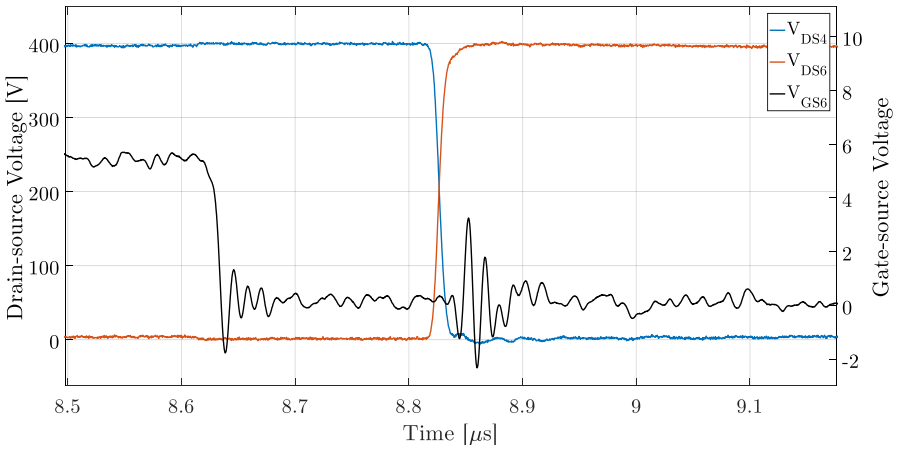
Fig. 4.23: Experimental result of the synchronous buck configuration test.

	$\mathbf{S_4}$	$\mathbf{S_6}$
Simulation	$26.10°C$	$26.10°C$
Experiment	$25.50°C$	$26.75°C$

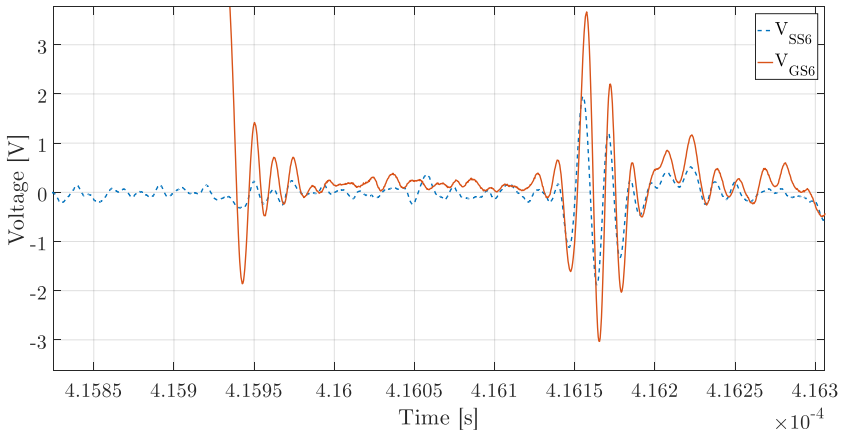
Tab. 4.3: Comparison of the temperature measurement from the simulation model and experiments in DC/DC configuration.

probe on the source pin of the same device. This test has revealed that this oscillations come from radiated noise captured by the probe leads, since the same oscillations occur on the "differential" measurement of the same source pin. The result of this test is shown in Fig. 4.24b with the dashed blue line. Since the two signals are randomly shifted (90° shifting in the figure shown), it has been impossible to subtract the signal in the real-time measurement and consequently cancel out this oscillations. However, the origin of this noise has not been found and this is leaved to further investigation of the problem.

Regarding the case temperatures, they have been measured with the system described in Sec. 4.2. As mentioned, the temperatures measured in this DC/DC test are only for S_4 and S_6. The result obtained are compared with the ones from the simulation model in Table 4.3, where can be seen that despite a slight error, the temperature trend foreseen during the simulation is confirmed. Such error is due to the fact that the TIM thermal resistance varies greatly varying the pressure applied on it when fixed. Additionally, the positioning of the thermocouples tips cannot be precisely controlled due to the small space available.



(a)



(b)

Fig. 4.24: Experimental measurement of the gate-source voltage during turn-off. In *(a)* the oscillations resemble the Miller effect. In *(b)*, the source-source voltage has been measured (blue dashed line) and the oscillations compared with the one seen on the gate-source voltage (orange solid line)

4.3.2 Inverter Operation

The inverter operation has been tested experimentally in single-phase configuration only. This test has been conducted increasing stepwise the DC-link voltage, monitoring the gate voltage of overlapped components (i.e. S_1 and S_6) in order to verify that the cross-talking problem has been solved by increasing the thickness of the board. For each step of voltage, the load has been varied with the aim of increasing the output

current. During all these steps, the case temperature of the upper switches has been monitored. The maximum full DC-link voltage that has been possible to reach is 400 V; for higher values, failures of the CeraLink capacitor have been experienced. Regarding the maximum current reached, it has been limited by the available power supply to 10 A. The output voltage along with the pre-filter current are shown in Fig. 4.25, with a switching frequency of 50 kHz, and the relative temperature are listed in Table 4.4 in comparison with the result from the simulation model. From these results, the simulation thermal model is validated and the capability of switching at relatively high frequency with low losses and devices stress is confirmed as well.

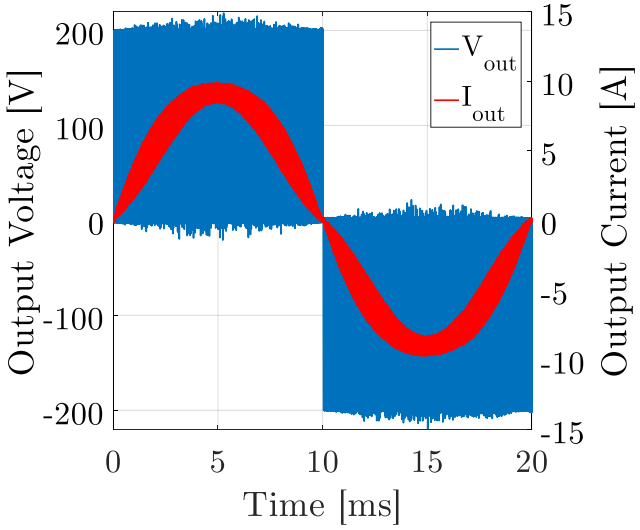


Fig. 4.25: Output voltage and pre-filter current in DC/AC configuration from the experimental result with a switching frequency of 50 kHz and $V_{DC} = 400\ V$.

	$\mathbf{S_1}$	$\mathbf{S_2}$	$\mathbf{S_3}$
Simulation	28.8°C	28.3°C	29°C
Experiment	29.15°C	28.7°C	29.3°C

Tab. 4.4: Comparison of the temperature measurement from the simulation model and experiments in AC/DC configuration.

Chapter 5

Conclusion and Future Work

5.1 Summary

The work of this thesis has been focused on the performance assessment of a 3L-ANPC inverter in single and three-phase operations. Before the assessment, an analysis of the topology and the viable modulation techniques have been presented in order to give an overview of the operation principles behind the converter under study. In the second part, the hardware has been analysed and the DC-link along with the output filter have been designed and selected. The aim of this is to assess the performances in terms of total volume in order to deduct the power density of the proposed inverter. From this study, in the single-phase configuration, the most cumbersome element is the DC-link buffer (usually, bulky capacitors). The second aspect emerged is that the volume occupied by the cooling system, which is more than 50% of the overall volume.

From the simulation results, the minor impact of the switching losses confirms the outstanding performances of the GaN HEMT for high-frequency applications when compared to the traditional Si-based MOSFET and IGBT. Regarding the loss distribution, it has been shown that with the studied modulation strategies, the switching losses are reduced to the detriment of the conduction losses. In fact, there are some switches which are kept ON during an entire half-cycle of the fundamental, leading to an increase in temperature of those ON switches. From this result, it is clear that the stress is not equally distributed among the switching cells. It has been shown that some switches, such as S_2 and S_5, are poorly stressed when compared to the remaining switches. This is due to the pulse pattern used for the inner switches of the phase-leg. Lastly, it has been shown that the optimized VSVM is able to provide a small ripple on the DC-link

voltage while keeping the output current distortion in the same range of the SVM. The latter has been shown to be unable to keep the voltage oscillation low as the other modulations do. Moreover, the dead-time effects on the current distortion have been described. It has been demonstrated that the open-loop compensation is ineffective at high switching frequencies (i.e., $\geq 150\ kHz$), since it leads to over-modulation.

The experiments have shown the outstanding switching performances of the GaN HEMT. It has been shown that the drain-source voltage can switch from 0 to the DC-link voltage in less than 12 ns with a little overshoot. This possibility is ensured by the ultra-low inductance commutation loop designed in [4]. Moreover, the commutation loop calculation has been validated through comparison of the simulation and experimental results. The gate driver performances have been proven to be good, even though two measurement problems have been experienced. The first issue is related to the use of a non-isolated differential probe, which has led to gate failures. This problem has been overcome using an optically isolated differential probe. The second measurement problem is the false Miller effect experienced on gate voltage measurements. This issue has been addressed to the radiated EMI captured by the differential probe. Regarding the DC/AC operation, they have been explored only in single-phase configuration and with a limited power and DC-link voltage, due to the several failures on the decoupling capacitors. The reason of such failures can be addressed to several causes. Firstly, the soldering technique of such capacitors is somewhat relevant in this case. Given the physical structure of these capacitors, a bend in the board or in the capacitor itself may lead to physical damage of the dielectric and, for voltages higher than 200 V, it may cause electric arc and destroy the capacitor. Another reason can be found in the temperature the capacitor may reach during the soldering procedure. The reason behind this is that, since the capacitor is landed on large copper planes, the local temperature that may be reached is higher than the maximum one. To support these considerations, the result of the failure is shown in the picture of Fig. 5.1, where the capacitor is clearly mechanically damaged on one lead, with a detachment from the dielectric. However, the good performances of the GaN HEMT are confirmed for the DC/AC configuration as well, leaving further research room for higher power applications.

5.2 Future Work

Starting from the work presented in this thesis, several aspect can be improved in the future work. The first aspect is the analysis of the modulation technique. It has

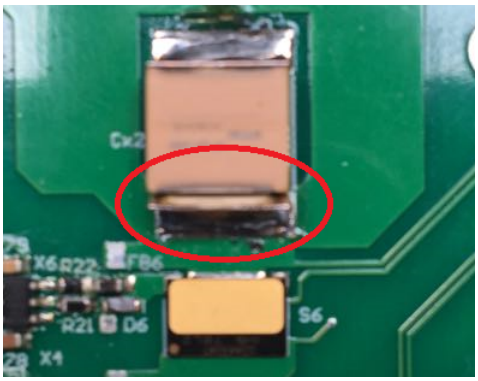


Fig. 5.1: Capacitor failure when the DC-link voltage has been increased to 300 V.

been shown that the implemented modulation strategies have the strong limitation of unequally sharing the stress among the switching devices, and thereby reducing the potential of the ANPC inverter in this sense. Therefore, different pulse patterns of the inner switches can be explored and tested, like the one proposed in [41], which is able to distribute the stress among all the switches. This improvement can be introduced in both single-phase and three-phase operation modes.

The second aspect that might be analysed in the future is the common-mode current reduction in order to provide a more reliable converter. In particular, the effect of the heatsink grounding can be explored for both conducted and radiated EMI. Moreover, the PCB layout may be modified by introducing a copper layer in order to break the capacitive coupling between the ground planes of the overlapped gate drivers. Additionally, further investigation of the root cause of the presented high voltage-related failures is needed in order to make the converter operate at the nominal voltage and power. Finally, the impact of the soldering technique on the converter reliability may be crucial. Since the GaN HEMTs are highly sensitive to ESD and temperature swings, the soldering profile and the placement method of the components may play an important role in the converter reliability.

The dead-band represents a limitation for the switching frequencies higher than 150 kHz. Therefore, in order to exploit the low harmonic distortion provided by the high switching frequency, a study to reduce the dead-time shall be carried out. Furthermore, this would effectively benefit to the efficiency, decreasing the conduction losses caused by the reverse conduction during the dead-time. Besides, an experimental evaluation of the converter efficiency and a validation of the loss model is necessary as well.

Regarding the passive components, several aspects can be improved and implemented. For instance, a huge improvement can be introduced on the DC-link buffer in single-phase operation. It is possible to reduce the DC-link buffer size by using an active buffer. In addition, the output filter can be realized and implemented on the test setup by exploring the feasibility of spiral inductor solutions. Due to the high switching frequency, the inductor values are very small and therefore air-core spiral inductors may be a viable solution to improve the compactness of the filter.

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