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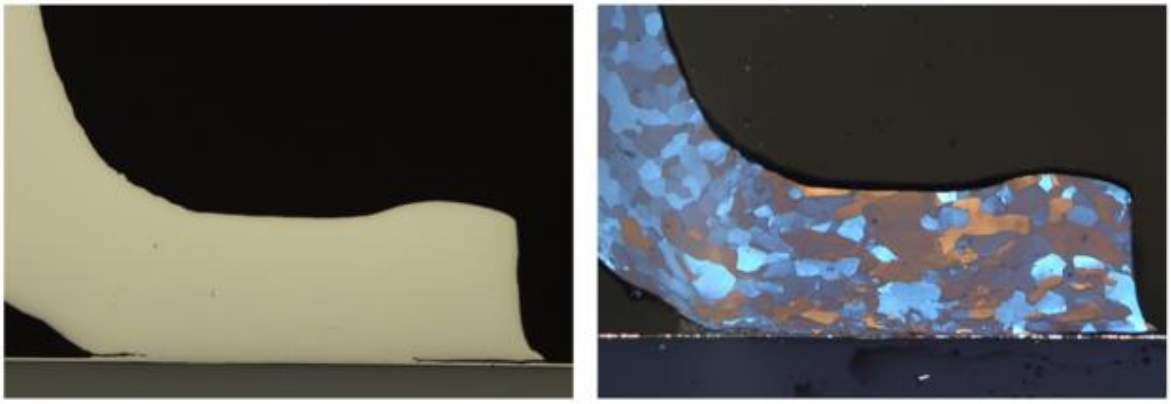
Comparative Study of Wire Bond Degradation Under Power and Mechanical Cycling Tests



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Synopsis:

This project aims to compare failure development in wire bonds of IGBT modules subjected to traditional active temperature cycling (ATC) and pure mechanical high-frequency share loads (MC). Micro-sectioning and optical microscopy are employed to examine the crack formation and development in the bonds. For both cycling methods atypical crack propagation paths are seen which is likely due to poor bonding quality. The crack propagation rate appears similar for low to moderate cycled wires, although large deviations are seen for each cycling method. Some discrepancies in the bond fracturing rate close to estimated end-of-life is observed for MC wires. These differences requires further investigation.

Resumé

IGBT-baserede effektmoduler anvendes inden for mange forskellige områder. På grund af krav til pålideligheden af disse moduler og deres levetid på mellem 10-30 år, er producenterne nødt til at undersøge, hvornår og hvordan modulerne fejler gennem en række forskellige accelererede tests. En af de tests, der ofte benyttes til at undersøge f.eks. nedbrydning af wire bonds er aktiv termisk cycling (ATC), hvor der induceres temperatursvingninger via elektriske effekttab i modulet ved drift drift. Denne cycling metode tager ofte flere uger at gennemføre, hvorfor det i denne rapport undersøges, hvorvidt ren mekanisk cycling (MC) kan anvendes som et alternativ. Mekanisk cycling er markant hurtigere end ATC og tager typisk under et minut.

Dette projekt baserer sig på en række moduler, hvoraf nogle er cyclet via ATC og andre via MC. Efterfølgende er der udført micro-sectioning, hvor der lægges et snit gennem wire bondet, hvorefter det via optisk mikroskopi er muligt at undersøge dannelsen og udbredelsen af revner som følge af eksempelvis fatigue. Nogle af prøverne, både ATC og MC, er efterfølgende blevet udsat for electro-etching, der fremkalder kornstrukturen i Al-wiren, som herefter kan undersøges via optisk mikroskopi med polariseret lys.

Det er ved undersøgelsen observeret, at revnerne i ATC-modulerne spredte sig under interfacet mellem metalisering og wire, hvilket er meget atypisk. Dette forventes at skyldes en dårlig kvalitet af wire bondet. For MC-modulerne forplantede revnerne sig i større grad i wire-materialet, hvilket er i overensstemmelse med, hvad der normalt ville forventes. Undersøgelser af kornstrukturen for modulerne afslørede, at der ikke var noget refinement område med mindre korn, der styrker

bondet, i ATC wires, mens der var et mere tydeligt refinement område for MC wires. Derudover sås der generelt mindre korn i wiren for MC-modulerne. Dette kan indikere, at MC medfører en rekonstruktion af kornstrukturen i wiren.

Preface

This project is carried out by 10th semester Nanomaterials and Nanophysics student, Steffen Buhrkal-Donau, from the Department of Materials and Production at Aalborg University in the period from September 1st 2016 to May 15th 2018.

Steffen Buhrkal-Donau

Readers Guide

This report is divided into chapters, sections and subsections. The chapters are numbered x, sections are x.y and subsections are x.y.z, e.g. the subsection two of the third section in chapter one is numbered 1.3.2. Equations, figures and tables are abbreviated as Eq., Fig. and Tab., respectively, and numbered by the chapter they are in, so the third equation in chapter four will be Eq. 4.3. When referring to a specific part of the report, chapters and sections are abbreviated as Chap. Sec., respectively.

References to sources are listed in the last page of the report with names, title, publisher and year. Each source has a reference number #, which is listed as [#] whenever the source is used for a particular section.

List of Abbreviations

ATC	Active temperature cycling
CTE	Coefficient of thermal expansion
DCB	Direct copper bonded
DUT	Device under testing
EOL	End of life
FEM	Finite element method
IGBT	Insulated gate bipolar transistor
MC	Mechanical cycling
MOSFET	Metal-oxide-semiconductor field-effect transistor
PTC	Passive temperature cycling
PoF	Physics-of-failure
US	Ultrasonic

Contents

1 Introduction

Insulated gate bipolar transistors (IGBT) are used in a wide range of applications from consumer electronics such as chargers for mobile phones and laptops to high power electronics used in aviation, the automotive industry and in power generation and distribution. Accordingly, the requirements for the devices have a large span. The voltage can vary from a few hundreds of volts in battery chargers to several kilovolts when used in wind turbines etc. Similarly, the currents can vary from a few amperes to kiloamperes. Furthermore, the surrounding environment varies from indoor to off-shore conditions. It is expected that the devices will perform within product specifications in a reliable way under all these different conditions. For high power modules the expected lifetime is often between 10 and 30 years [1, 2].

To ensure the reliability of components, manufacturers have to carry out tests to proof the longevity of the device. Under normal circumstances, evidence that the device is suitable for the application it was made for, would take as long as the lifetime of the device. This is obviously not practical due to the long lifetime of the devices, why accelerated tests are used. One commonly used accelerated method for testing the reliability of wire bonds and solders is active temperature cycling (ATC). This test induces temperature swings causing thermo-mechanical stress in junctions between materials of different coefficients of thermal expansion (CTE). The temperature difference during ATC is higher than what would be expected for the device to experience in the field, causing the acceleration of the degradation of the device. With this increased temperature swing the cycling of the device to end of life (EOL) will take weeks instead of years [3, 4]. The risk of this approach is that under accelerated test conditions different types of failure mechanisms can be introduced compared to the ordinary operation conditions. Therefore, one needs

carefully look into the physics-of-failure and related key stressors.

Even though ATC is significantly accelerated compared to field conditions, it is still a time consuming process. Therefore, even faster methods for cycling of devices are of interest. One such method for cycling of wire bonds using pure mechanical load is proposed in [5]. This mechanical cycling (MC) method can have cycling frequencies of several kilohertz, allowing for cycling to EOL in seconds. This has the potential to save both time and money when testing reliability of wire bonds of new devices. However, a better understanding of how this cycling method compares to real life conditions is needed, in order for this method to be useful. The aim of this work is to compare the degradation of the wire bond during MC to those formed during traditional ATC. Furthermore, it is examined if the crack growth rate follows what is expected from physical models. Thereby, it is examined whether MC is suitable for replacing the much more time consuming ATC for lifetime prediction of wire bonds.

2 Failures of Power Modules

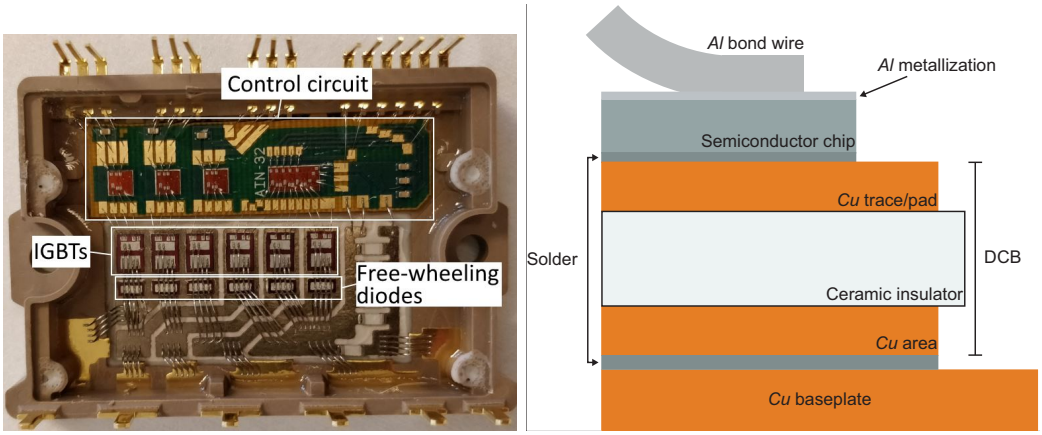
This chapter describes the layout and main components of IGBT power modules along with modes of operation, various failure mechanisms and different types of accelerated tests used to estimate the EOL of power modules.

2.1 Layout and Main Components of a Power Module

The main purpose of a power module is to handle high electrical power. For that, three main properties should be considered: Current handling, blocking voltage and power dissipation. Today IGBT modules are most commonly used, as they have a high blocking voltage and good current handling capabilities.

One of the most commonly used types of power modules is the wire bonded IGBT module. This type of device typically consists of several sections of IGBTs and free-wheeling diodes mounted on a base plate and packed in a plastic housing, as seen in Fig. 2.1 a. Almost all power modules, including both IGBT and MOSFET (metal-oxide-semiconductor field-effect transistor) modules, contain free-wheeling diodes, that are connected anti-parallel to the transistor. The purpose of the free-wheeling diode is to give the reverse inductive currents, that occur during switching, a path to run and thereby preventing reverse voltage spikes. The only active components of an IGBT power module are the IGBTs and the free-wheeling diodes. Aside from the active components, a power module consists of numerous in-active components that are responsible for optimizing operation

conditions for, and ensuring good electrical contact to the active components, thus ensuring high performance and reliability of the module [1, 4].



(a) **(b)**

Figure 2.1 A top-view of an opened IGBT power module with control circuit, IGBTs and free-wheeling diodes (a). The layered structure of an IGBT module is seen in (b).

The main purpose of the plastic housing is to ensure both mechanical stability and high tensile strength of the module during operation, as well as ensuring electrical insulation and protection against environmental factors such as dust and moisture.

Apart from the active power handling chips, some modules also contain a control circuit. The main purpose of the control circuit is to control the gate. Apart from gate drivers, the control circuit can contain a number of different protection systems, such as over current protection, short circuit protection, under current protection and overheating protection. By continuously doing electrical and temperature measurements on the IGBTs, it is possible to take action in case an error occurs, to prevent damage to the modules [6].

The silicon chips are mounted on a direct copper bonded (DCB) substrate using a conducting solder. A tin-silver solder (SnAg) or a tin-lead solder (SnPb) is commonly used. However, due to environmental and health impacts of lead-based solders, silver based solders are getting still more popular. A vacuum soldering process is used in order to prevent the formation of air pockets in the solder layer, that will increase the thermal resistance, which may cause early failure of the device [3, 4, 7].

The DCB substrate consists of two copper layers separated by a dielectric ceramic,

commonly Al_2O_3 or AlN. The ceramics are used due to their low thermal resistance compared to polymer insulators. Furthermore, there is a greater mismatch of CTE between copper and a polymer insulator, than between copper and a ceramic insulator. The copper surfaces may be nickel-plated for protection against the formation of copper sulfide (CuS), which is conductive and can spread along the electric field and cause short circuit, causing the device to fail. In the top Cu layer of the DCB substrate trenches separate the Cu layer into different current tracks, to which terminals can be attached to get electrical contact with the environment. The DCB substrate has to provide both electrical insulation and thermal connection between the power components and the cooling medium, as well as conduct current from the power components via copper tracks. The DCB substrate may be mounted on a copper baseplate using a similar solder as used for the chips [3]. This layered structure can bee seen in Fig. 2.1 b.

Apart from the Cu tracks of the DCB and the chip solder, electrical connections for the load current within the module are established using heavy Al bond wires. These are ultrasonically (US) bonded to a thin Al metallization layer, that ensures good electrical contact with the chip, and the Cu tracks of the DCB substrate. They normally consist of 99.99 % Al and have a thickness between 100-500 µm. Thin bond wires are used for connections that do not carry the load current, such as gate connections. These typically consist of 99 % Al and 1 % Si and have a thickness between 17-100 µm. The bonding process is carried out at room temperature with frequencies ranging from 40-100 kHz. During the bonding only limited temperature changes occur. The bonding process is believed to be a solid state process consisting of a series of overlapping processes:

1. The applied force from the wedge causes hardening of the wire.
2. The yield and tensile strength of the Al wire is decreased due to the US vibrations (US softening).
3. The two previous processes cause deformation of the wire, which enables diffusion and removal of impurities.
4. US hardening of the wire occurs after the US softening.

The combination of all of these processes results in an adhesion process ending in a polycrystalline interface [3, 8].

On top of the active components, filling the entire plastic housing, is a soft silicone mould. The silicone mould fills up the space around the other components

of the power module in the plastic housing serving as further protection against the environment. Furthermore, as the voltage drop between nearby components within the module can exceed the breakdown voltage of air, the silicone gel serves as a dielectric, preventing short-circuit due to dielectric breakdown [2, 3, 4].

2.1.1 IGBT Architecture and Modes of Operation

The structure of an IGBT is very similar to that of a MOSFET, however there is an extra highly doped P^+ region at the drain (called collector for IGBTs), as seen in Fig. 2.2. For IGBTs the notation for the cathode is emitter and the anode is called the collector, as it is for bipolar junction transistors.

Considering the IGBT structure in Fig. 2.2 b, where the emitter voltage (V_e) is lower than the collector voltage (V_c), i.e. the collector-emitter voltage $V_{ce} = V_c - V_e > 0$, and there is either negative or no potential to the gate ($V_g \leq 0$), the IGBT is in forward blocking mode. Here the pn-junction J_2 seen in Fig. 2.2 b is reverse biased and thereby blocking the current. The junctions J_1 and J_3 are forward biased and are therefore not contributing to the current blocking.

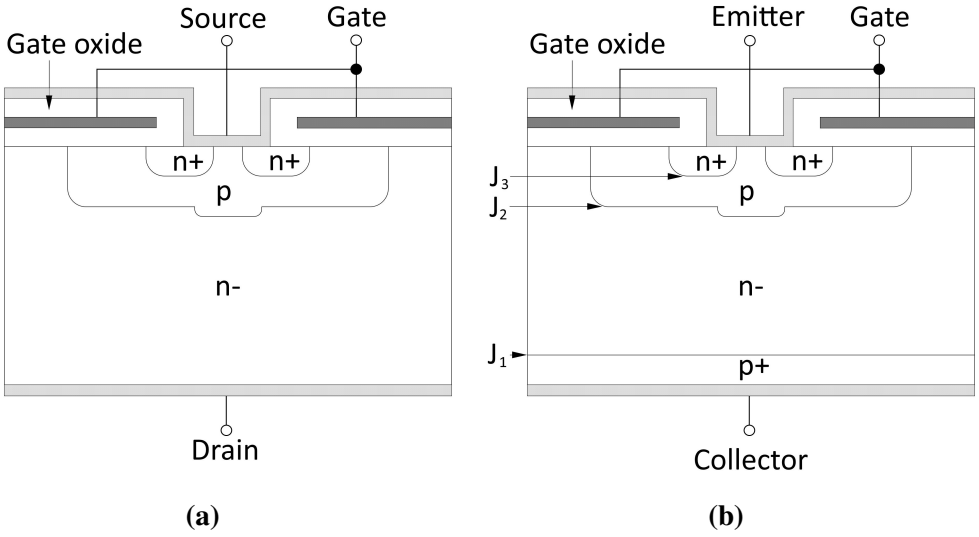
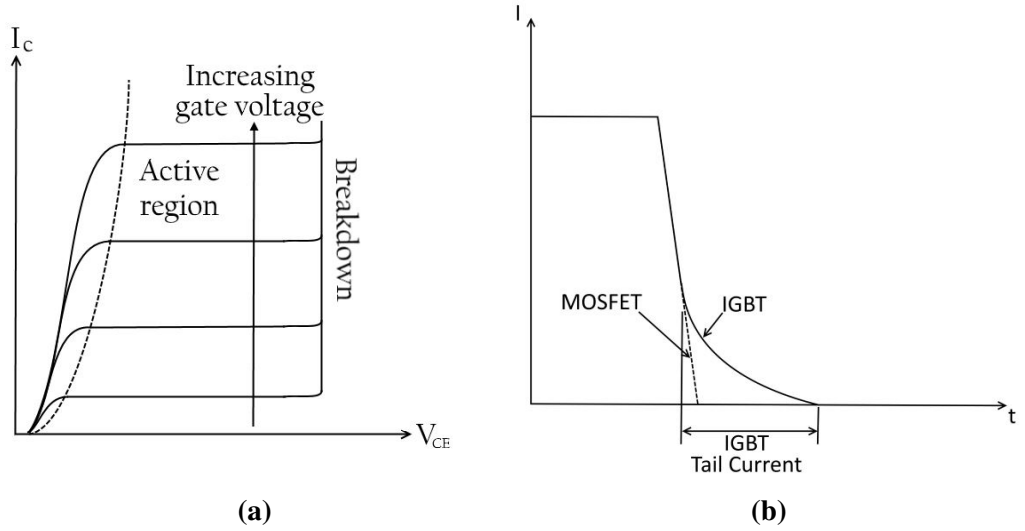


Figure 2.2 The structure of a vertical MOSFET (a) and IGBT (b).

Applying a positive voltage higher than the threshold voltage to the gate causes an inversion channel to form in the p-region under the gate. This allows electrons to flow from the n^+-region to the n^--region (drift zone). From here the electrons

can flow through the forward biased junction J_3 into the p^+ region and finally to the collector. The flow of electrons from the emitter to the drift zone causes the potential in the drift zone to drop, causing holes to flow from the p^+-region into the drift zone. This flow of holes will under normal operating conditions be sufficient to ensure a hole concentration in the drift zone several orders of magnitude higher than the dopant concentration in the drift zone. This in turn causes even more electrons to flow from the n^+-region to the drift zone to ensure charge neutrality. The high flow of charge carriers to the low doped drift zone causes the resistance in the drift zone to drop dramatically. This process is called conduction modulation, and causes the voltage drop across an IGBT to be significantly reduced.

If the gate voltage (V_g) is insufficient, the inversion channel is weak, causing a lower number of electrons to flow to the drift zone, increasing the voltage drop across the IGBT. When this happens the IGBT is operating in the active region of it characteristic curve, seen in Fig. 2.3 a. While operating in the active region there are significant power losses in the IGBT, which over time will destroy it. Therefore, it is important to avoid to operate in the active region apart from during switching.



(a) **(b)**

Figure 2.3 The characteristic curve of an IGBT at different gate voltages is seen in (a). The difference between the turn-off characteristics of a MOSFET without tail current and an IGBT with tail current is seen in (b).

When the gate voltage is turned off, the inversion channel is closed and the electrons cannot flow from the n^+-region at the emitter to the n^- drift zone. Due to the high concentration of charge carriers in the drift zone at this point in time, a

current will continue to be for some time after the gate is turned off. Electrons will be flowing from the drift zone into the P^+-region at the collector and the holes will flow into the lower doped P-region at the emitter side. As the charge carrier concentration is going down, the current flow comes to a standstill, and the remaining charge carriers will be removed by recombination. The turn-off of an IGBT can therefore be divided into a MOSFET-like phase, with a rapid drop in current as the inversion channel is closed, and a bipolar phase forming a tail-current with a slower decreasing current, as seen in Fig. 2.3 b. This tail-current causes greater turn-off losses in IGBTs compared to power MOSFETs. When the gate is turned off ($V_g \leq 0$) and the emitter potential is higher than the collector potential ($V_{ce} < 0$) the IGBT is in reverse blocking mode. Here the pn-junctions J_1 and J_3 are blocking the current as they are reverse biased. The blocking capability for reverse blocking is not necessarily the same as for forward blocking [3].

2.2 Failure Mechanisms

During operation, a number of factors will contribute to material ageing and fatigue and thus to the eventual failure of a power module [1]. To improve lifetime and performance of power systems, knowledge of these processes is of great importance. The typical types of failure mechanisms depend on the different types of modules and the application; e.g. wire bond degradation, reconstruction of metallization and solder fatigue are the dominant failure mechanisms of multichip high-power IGBT modules [2, 9]. For all these mechanisms, thermo-mechanical stresses, which are developed in the multilayer structures of devices due to difference in CTE, play a very important role. Therefore, key issues of these stresses are described below.

2.2.1 Thermo-Mechanical Stress

During operation any power semiconductor device will be subject to temperature swings due to electrical losses in the devices [10]. As different materials in the layered structure of power devices have different CTE (α), thermo-mechanical stresses occur at the interfaces leading to fatigue [10, 11, 12].

Thermo-mechanical stress between Al and Si gives rise to both wire lift-off and metallization reconstruction. Properties relevant to thermo-mechanical stress between Al and Si are listed in Tab. 2.1. As Si is brittle it will behave elastic, while

Al is ductile with a low yield stress, and is thus assumed to behave elastic/ideal plastic under temperature variations. The resulting plastic strain in the Al gives rise to the failure of wire bonds in power semiconductor devices. A basic understanding of the strains can be gained using a simple two-layer model, as shown in Fig. 2.4 [10].

		Si	Al
CTE	α [10^{-6}/K]	2.8	23.5
Youngs modulus	E [GPa]	168	70
Yield stress	σ_y[MPa]		20

Table 2.1 Selected material properties for Al and Si [10].

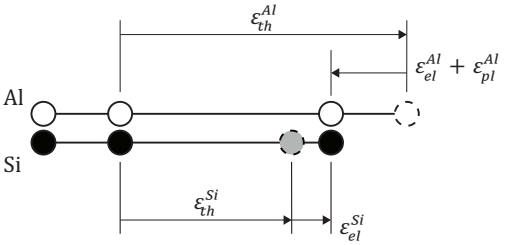


Figure 2.4 A simple model of an Al/Si interface heated up; inspired from [10].

Separately, the Si and Al would expand differently under thermal heating due to the difference in CTE, however, as they are connected the total strain in the Si and the Al will evolve as shown in Fig. 2.4. This can be described mathematically as:

$$\varepsilon_{th}^{Al} - \left(\varepsilon_{el}^{Al} + \varepsilon_{pl}^{Al}\right) = \varepsilon_{th}^{Si} + \varepsilon_{el}^{Si} \quad \Rightarrow \quad \varepsilon_{pl}^{Al} = \left(\varepsilon_{th}^{Al} - \varepsilon_{th}^{Si}\right) - \left(\varepsilon_{el}^{Al} + \varepsilon_{el}^{Si}\right) \tag{2.1}$$

where ε_{th} describes the strain in the free state and ε_{el} corresponds to the elastic strain. The first part on the right of Eq.2.1 can be written in terms of α for Si (α^{Si}) and for Al (α^{Al}) and the temperature change (ΔT).

The elastic strains (ε_{el}) can be described by Hooke's law using the yield stress for Al (σ^{Al}) and Young's modulus (E) for the two materials [13, chapter 6]. The yield stress for Al is the maximum stress that can arise in either the Si or the Al, which is used to determine the strain under plastic deformation:

$$\varepsilon_{pl}^{Al} = \left(\alpha^{Al} - \alpha^{Si}\right)\Delta T - \left(\frac{\sigma^{Al}}{E^{Si}} + \frac{\sigma^{Al}}{E^{Al}}\right) \tag{2.2}$$

In the case of Al and Si, the second term of Eq. 2.2 describing elastic strain is much smaller than the first term describing the thermal strain; thus, for very low temperature changes it can be neglected, reducing Eq. 2.2 to [14]:

$$\varepsilon_{pl}^{Al} = \left(\alpha^{Al} - \alpha^{Si}\right)\Delta T \tag{2.3}$$

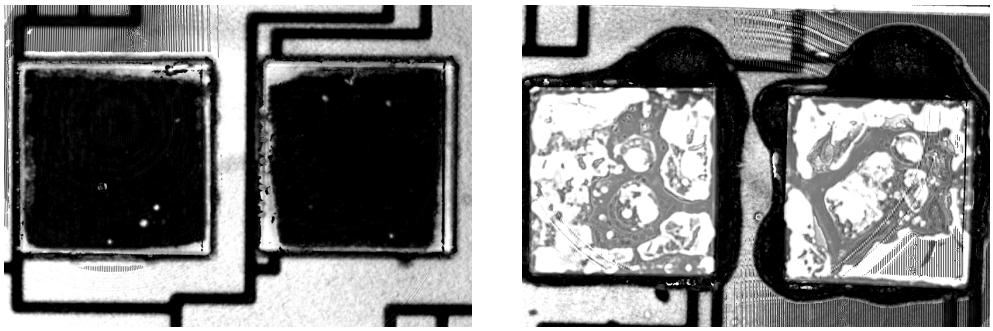
Eq. 2.2 states that the plastic strain is the difference between the thermal strain and the elastic deformation of Al and Si, however this is only an aproximation.

In reality it is a multi-axial state and real ductile materials do not behave linearly. Therefore, the real stresses and strains have to be calculated using numerical methods such as finite element method (FEM) [1].

2.2.2 Solder Fatigue and Solder Voids

As mentioned in Sec. 2.1, a SnAg- or SnPb-based solder is used to attach the Si chips to the DCB, and to attach the DCB to the baseplate. These solder layers experience periodical thermal stress during operation causing fatigue related degradation of the solder. Three types of strain occur during the cycling: Creep, elastic strain and plastic strain; according to [15] creep is the main contributor to solder degradation. The degradation of the solder causes delamination, cracks and voids in the solder. In Fig. 2.5 acoustic microscope images of a mint solder (Fig. 2.5 a) and a solder with voids after temperature cycling (Fig. 2.5 b) is seen. As mentioned in Sec. 2.1, these formation voids from gaseous inclusions can be minimized using a vacuum soldering process. This is of great importance, as these voids will increase in size during thermal cycles and they can promote crack initiation at the edge and corners of the die/DCB. Crack formation and delamination will initiate at the border of the solder joint, where the stress is the greatest, and are further promoted by sharp corners of the Si chip or DCB. In [16] it has been shown, both experimentally and numerically, that the solder lifetime is both dependant on ΔT and T_{mean}. Furthermore, a larger area of solder increases the stress in the solder, promoting solder degradation, and the rate of temperature change influences the stress distribution and relaxation, as creep is rate dependant.

The degradation of the solder layers will cause a decrease in thermal conductivity between the active components and the heat sink, resulting in higher peak temperatures. Furthermore, as the chip solder also acts as an electrical connection between the active components and the DCB substrate, degradation of this layer can also increase the electrical resistance [2, 15, 16, 17, 18].

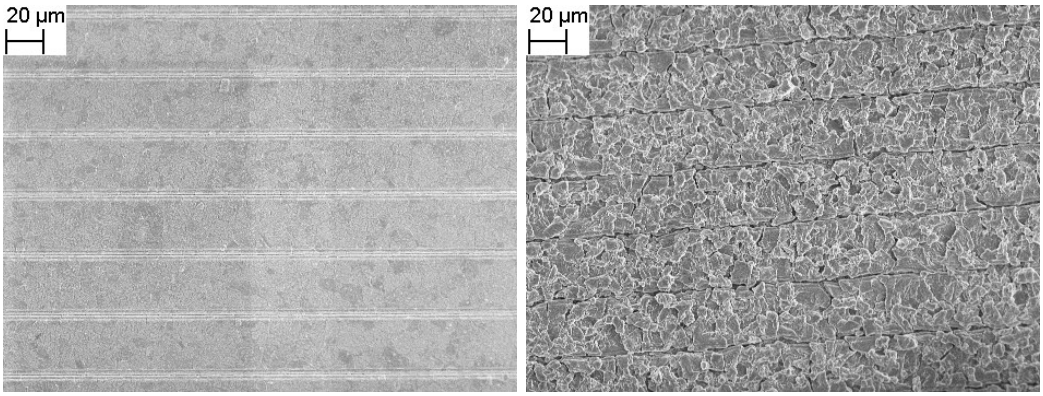


(a) **(b)**

Figure 2.5 Acoustic microscope images of a new solder (a) and a solder with voids after temperature cycling (b).

2.2.3 Aluminium Metallization Reconstruction

In typical power modules, Si chips are covered by a few micrometer thick Al metallization layers which provide electrical connection across the die and serve for making wire bonds. The large mismatch in CTE between Al and Si causes periodical compressive and tensile stress in the Al metallization during thermal cycling. These stresses can exceed the yield stress of Al. In IGBT modules this leads to the occurrence of plastic deformation at the grain boundary which can cause extrusion of Al grains, cavitation effects at grain boundaries and crack formations in the metallization. This causes roughening of the metallization surface, which can be seen in Fig. 2.6, showing the metallization of a mint IGBT (Fig. 2.6 a), and the metallization of an IGBT that has been subjected to ATC (Fig. 2.6 b). Metallization reconstruction reduces the effective cross-section of the metallization, causing an increase of the sheet resistance of the Al layer. This contributes to the increase in V_{CE} for an increasing number of cycles. In cases of severe metallization reconstruction, interruption of single emitter windows can occur, causing the loss of connection to IGBT cells. This leads to an uneven current density in the metallization, with critical areas where the current density can get sufficiently high for melting and electromigration to occur. As the reconstruction of the metallization causes the resistance to increase, it will cause the power dissipation to increase too. Therefore the temperature swings will also increase, accelerating both the metallization reconstruction and other failure modes, such as wire bond degradation [1, 2, 19].



(a) **(b)**

Figure 2.6 Metallization of a mint IGBT (a), and an IGBT after ATC (b).

2.2.4 Burnout Failures

Burnout failure is often seen as the final consequence of wear out, or due to random events such as cosmic radiation. Often in burnout there is a short circuit, where a large current flows through parts of the device while supporting the full line voltage. Sustaining this short circuit current for a long time rapidly leads to thermal runaway. When this happens the current spikes in the range of 100 kA, causing most of the capacitive energy in the device to be released in a few hundreds of nanoseconds, resulting in a peak power of up to 100 MW. All of this energy is dissipated by ohmic heating mainly in the Al wires and the Si chips. This causes an adiabatic heating process and evaporation of the Al wires, causing a shock wave in the silicone gel, destroying the device.

There can be a number of different reasons for a shourt circuit to form such as inhomogeneous current sharing, which can be caused by multiple wire lift-offs, overheating due to degradation of solder, leading to poor thermal contact to the heat sink, damages to the DCB substrate or cosmic radiation [1, 2].

2.2.5 Wire Bond Fatigue

Wire bond fatigue is related to the structural degradation of the wire/metallization interface due to thermo-mechanical stress. This type of failure can be subdivided into heel cracking, which is caused by repeated flexure of the wire due to ohmic self heating, and wire lift-off caused by a CTE-mismatch at the Al/Si-interface as

described in Sec. 2.2.1. Wire bond fatigue is seen as a low cyclic stress with a progressive degradation over time which keeps the device functional until a catastrophic failure. As wire lift-off is the dominating type of wire bond fatigue in modern power modules, this will be the focus of this section [20].

During operation of the device, the plastic strain caused by thermo-mechanical stress leads to the development of cracks. Typically, crack formation originates near the bond wire termination, which is seen in Fig. 2.7 a, as the stress in this area is higher due to the limited expansion freedom. Furthermore, imperfect bonding can lead to crack initiation sites at the edges of the bonding area. Fig. 2.7 b and Fig. 2.7 c show the heel and toe of a wire bond on a mint IGBT. The heel bond (Fig. 2.7 b) shows a close to ideal bond termination, where the toe (Fig. 2.7 c) shows a possible initiation site for cracks to start forming [20].

Apart from the high stress and possible initiation sites at the wire-metallization interface, another reason for cracks to form here is that the interface can be weakened due to oxides and other impurities trapped in the interface during the US bonding [10]. These defects can be seen in the interface both near the heel and toe of the mint IGBT wire bond seen in Fig. 2.7 b and Fig. 2.7 c.

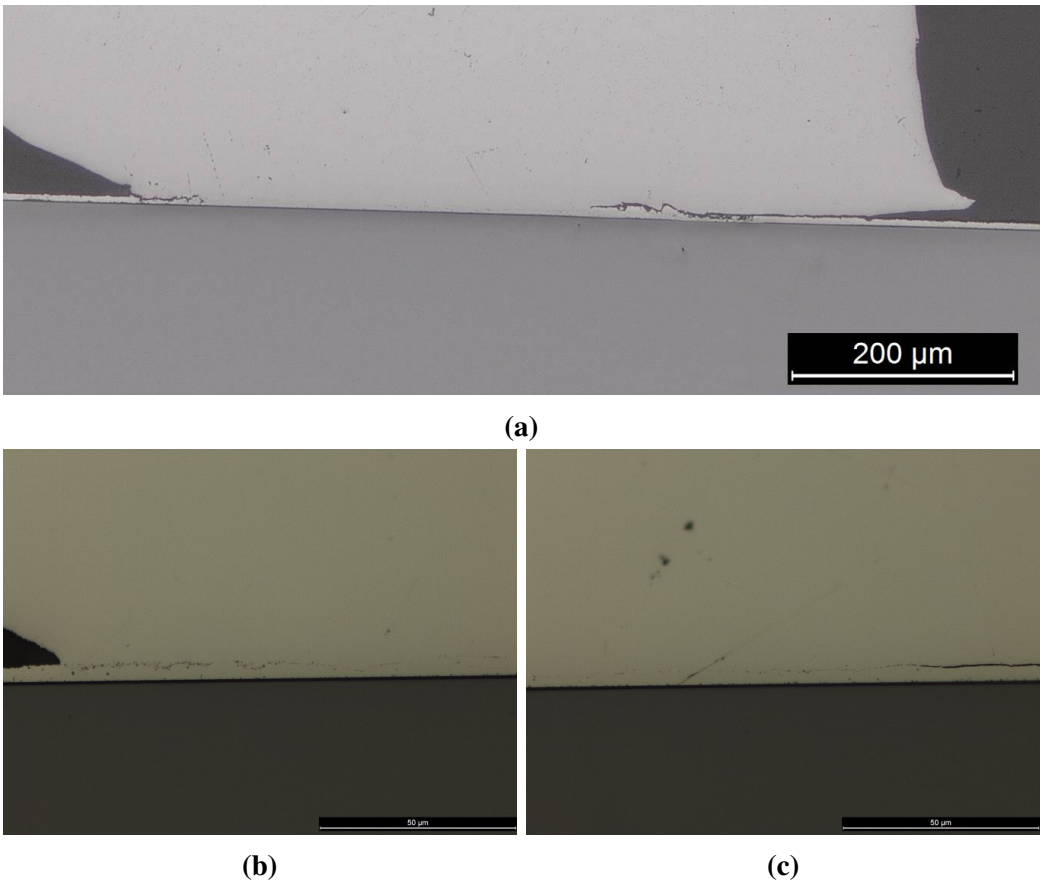
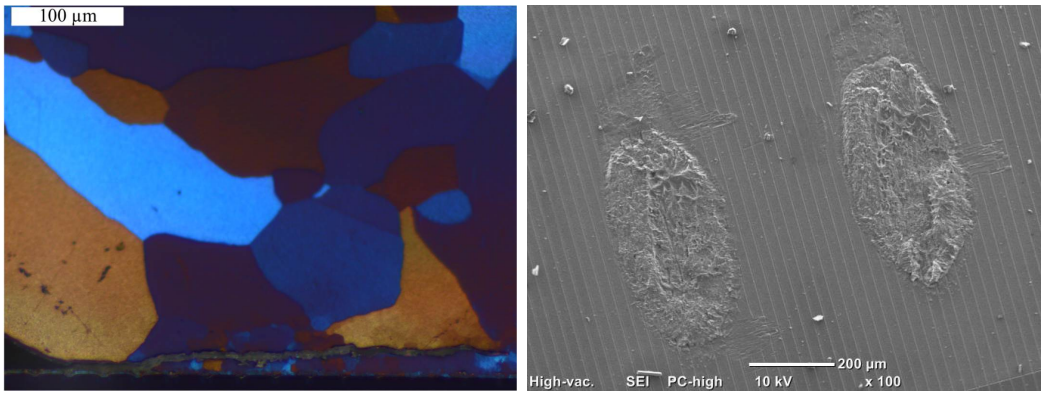


Figure 2.7 IGBT showing cracks initiating from both heel and toe after ATC **(c)**. Heel **(b)** and toe **(c)** of a mint IGBT.

After initiation, the crack propagates into the wire itself. This is due to hardening of the Al near the interface caused by the US bonding process, which causes a large degree of deformation to occur near the interface, resulting in a decrease in grain size and thereby hardening of the material, as seen in Fig. 2.8 a [10, 21]. This hardened area near the interface is called the refinement area. The 3D shape of the refinement area has previously been shown to roughly span half an ellipsoid [10]. Studies of the grain structure show three different fracture types: Delamination, where the wire material separates from the metallization, intergranular fracture, where the crack propagates between grains and transgranular, where cracks go through the grains. It was observed that delamination occured mainly in the beginning of the crack development, after whitch intergranular fracture occurred and towards the end both trans- and intergranular fractures occurred [20].



(a) **(b)**

Figure 2.8 Crack propagating above smaller grains in the refinement area **(a)**. Elliptic footprint after wire lift-off **(b)**.

Eventually the cracks will meet around the center of the wire resulting in complete lift-off of the wire. After lift-off, wire residue will be seen on the metallization in an elliptic footprint as seen in Fig. 2.8 b. These leftovers of wire material on the metallization confirm that the fracturing occurs not exactly at the interface but through the boundary of the refinement area in the wire.

2.3 Lifetime Estimation of Wire Bonds

Different models for estimating the wire bond lifetime in power modules have been proposed. The most commonly used plastic strain based model is the Coffin-Manson model, relating the number of cycles before a wire lift-off (N_f) to the plastic strain (ε_{pl}):

$$N_f \propto \left(\varepsilon_{pl}\right)^{-n} \tag{2.4}$$

where n is a positive number. By combining Eq. 2.4 and Eq. 2.3 from Sec. 2.2.1, N_f can be found as a function of ΔT:

$$N_f = a\,(\Delta T)^{-n} \tag{2.5}$$

The coefficients a and n can either be estimated from numerical simulations or be obtained from experimental measurements of real cycled devices. This model allows for estimation of lifetime of a device based on either ATC or PTC (passive temperature cycling) tests [2]. The Coffin-Manson model is built on the assumption that ΔT is the sole stressor. This, however, is not the case, as other factors

such as wire geometry, composition and structure also affect the lifetime. Deviations in production quality is also an important parameter. Several expansions have been made to the Coffin-Manson model to try and accommodate some of these factors. These terms take into account the mean junction temperature ($T_{j,m}$), the wire bond aspect ratio, pulse duration and chip thickness. With all of these extra terms, the main stressor will still be ΔT or T_{mean}. The extra terms contain a number of component related parameters, why a large number of accelerated tests is needed to provide reliable results [1, 2, 22, 23]. Another big problem is that the reliability data obtained for one type of device is not transferable to another model, moreover, even hardly transferable to the same type of device operating under different conditions.

2.3.1 Physics-of-Failure

Another approach suggested in last years is physics-of-failure (PoF) analysis [24, 25, 26]. PoF Is based on the analysis of key factors leading to fatigue and failure applying physics knowledge about structure, composition and properties of materials used for device production as well as phenomena and effects taking place in the devices during operation. To utilize such approach for given components, devices or systems one needs to obtain clear physical understanding of the failure mechanism and accumulate systematic data about change of material properties, structure etc. This data is then used to build advanced models, which can for example utilize finite element analysis approach and predict development of failure. Thus, PoF approach can provide a deeper understanding of the reliability aspects and it can be easier transferred to different load conditions and different power devices for which the lifetime must be estimated. A good example of a PoF method is presented in [27] for wire bond fatigue, where a computational model for a section of a power module is developed, the key factors affecting wire bond fatigue under power cycling are estimated and the damage accumulation is predicted. The model is verified by comprehensive physical analysis of wire bond degradation [28].

An important part of analysis of wire bond fatigue in PoF approach is the Paris' law. This is based on fracture mechanics and describes the crack growth (da) per cycle (dN) using the strain density factor range ΔK_ε[1] [29]:

$$\frac{da}{dN} = C\,(\Delta K_\varepsilon)^n \tag{2.6}$$

[1]The stress intensity factor (K) is used to predict the stress state near the tip of a crack.

where C and n are material constants determined from empirical data. ΔK_ε is dependant on the temperature load and can be calculated using FEM. In order to use this model to predict the number of cycles to failure of a wire bond a critical length, defining the length a crack can propagate, before the bond is considered to have failed, is selected [29]. Using this approach, one can put physics background into the analysis of crack development and wire lift-off, and compare different test methods.

2.4 Accelerated Tests

Due to the long lifetime of power devices under normal field conformal stress conditions (10-30 years), reliability testing under these conditions are not an option. Therefore a number of accelerated cycling methods have been developed. These accelerated tests can be used to estimate the expected functionality during the entire lifetime of the device. Depending on what failure mechanism is desired to examine, different tests are used [4]. A number of these tests are breafly described below.

2.4.1 Thermal Cycling Methods

In order to estimate failures due to thermo-mechanical stress, such as solder fatigue and wire lift-off, PTC or ATC is commonly used. These tests work by inducing temperature swings and gradients in the power modules causing thermo-mechanical fatigue. During these accelerated tests the temperature swings and gradients are typically higher than what will occur during field use, allowing for testing until EOL within weeks instead of decades [30]. This might however give rise to material related mechanisms normally not seen on devices in the field [1].

Passive Temperature Cycling (PTC)

During PTC the device is heated and cooled passively by the environment which is usually done simply by exposing the device to temperature variations. PTC has a long cycling period varying between 15 minutes up to one hour. The long cycling time is necessary to ensure that the entire device has reached the desired temperature. During PTC the temperature distribution throughout the device is

spatially homogeneous [1, 31].

As the entire device is heated (and cooled) during PTC, one of the main advantages compared to ATC is that PTC allows for the examination of the thermo-mechanical robustness of the entire device rather than just the components heated during operation [1].

Active Temperature Cycling (ATC)

Compared to passive temperature cycling ATC is a closer resemblance to the real-life conditions. During ATC the device is heated due to on-state losses from either AC or more commonly for IGBT- and MOSFET-based modules pulsed DC [1]. Under testing the device is normally mounted on a heat sink as in real application [4]. The heat sink can either be based on air-cooling or liquid-cooling, where liquid-cooling systems are more complicated but also more effective, allowing for a higher maximum cycling frequency.

When the device is conducting the load current (I_{load}) the temperature will increase. After the time (t_{on}) when the maximum junction temperature (T_{high}) is reached, the current is switched off causing the chip to cool down. The chip will be cooling for the time (t_{off}), until it reaches a minimal junction temperature (T_{low}) thus completing the cycle. In the beginning of the heating and cooling period, the rate of change in temperature is higher than approaching the end of the heating and cooling periods, as seen in Fig.2.9 [1]. T_{high} and T_{low} define the characteristic parameters for ATC: The temperature swing (ΔT_j) as given by Eq. 2.7 and the medium temperature (T_m) defined by Eq. 2.8 [4].

$$\Delta T_j = T_{high} - T_{low} \tag{2.7}$$

$$T_m = T_{low} + \frac{T_{high} - T_{low}}{2} \tag{2.8}$$

Compared to passive temperature cycling ATC has a short cycling time of typically 0,2 seconds to 1 minute [31]. Apart from the high load current a low measuring current (I_m) can be applied, which is used for measurements of electrical thermo-sensitive parameters, allowing for estimations of the junction temperature (T_j) during the test [32].

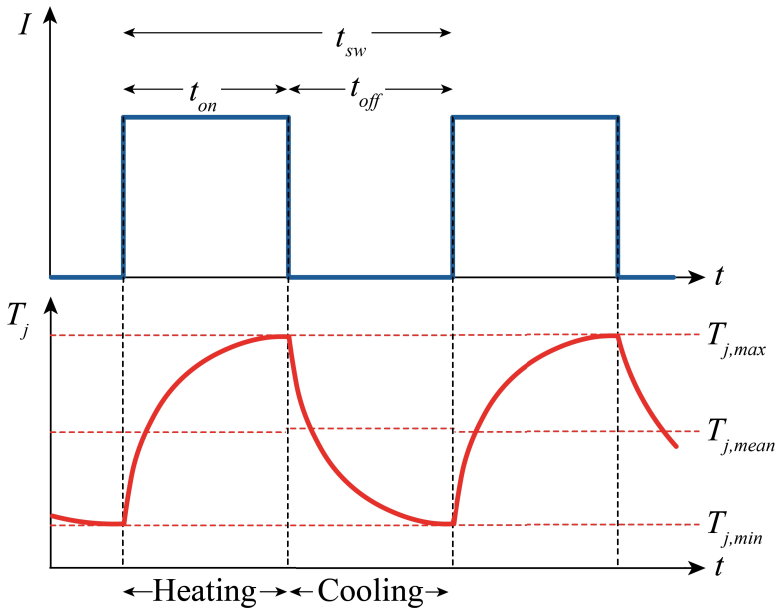


Figure 2.9 Example of changing T_j due to pulsed DC current.

There are several different control strategies with the most commonly used being keeping t_{on} and t_{off} constant along with the load current (I_{load}). During the test $T_{j,min}$, $T_{j,max}$ and ΔT_j will change due to the degradation of the device with no compensation from the control strategy. This approach has the closest resemblance to field conditions. Other approaches include keeping the change in heat sink temperature (ΔT_c) constant, keeping power losses (P_v) constant or keeping ΔT_j constant [31].

During ATC different parameters can be monitored. Two of these parameters, the thermal resistance between the junction and baseplate (R_{th}) and the on-state voltage (V_{ce} for IGBTs), are considered to be good indicators of ageing in power devices, and are therefore monitored. The on-state voltage is an indicator for wire bonds' degradation and lift-off. Wire lift-off can be seen as a stepwise increase in the on-state voltage. R_{th} indicates the state of the solder. When fractures appear in the solder it will modify the heat transfer from the chip to the baseplate. R_{th} can be calculated from the power dissipation P_d as:

$$R_{th} = \frac{T_{j\,max} - T_c}{P_d} = \frac{T_{j\,max} - T_c}{V_{ce\,sat}\,(I_{load} + I_m)} \tag{2.9}$$

T_c is normally measured using a thermocouple glued to the baseplate. For measur-

ing T_j there are several approaches. For close moulded packages direct measurement of the temperature is not an option. Therefore thermo-sensitive parameters are used. These can be measured either by monitoring on-state voltage and current or by I_m. In the case of open modules with access to the die, T_j can be measured directly on the chip surface. This can be done either by a thermocouple, an optic fibre with crystal sensors (either GaAs or phosphor) or an infrared camera; the infrared camera has the advantage of being fast, precise and not in contact with the die. The temperature is measured over the entire module, which is useful as it gives a first evaluation of the temperature distribution in the module. As thermocouples are in contact with the chip, poor thermal contact can greatly influence the accuracy and response time using thermocouples. Optical fibres allow for precise measurement of the temperature and do not require thermal contact. The response time is however slightly higher than that of thermocouples [31].

ATC allows for online monitoring of temperature and electrical data during each cycle leading to the estimation of the module lifetime based on a predetermined EOL criteria. If for instance the observed values increase more 20 % the EOL criteria is met and the corresponding number of cycles for failure (N_f) defines the lifetime of the device [1, 31].

2.4.2 Other Tests

Aside from thermal cycling methods various other accelerated test methods exist; some of these are briefly described in the following.

High Temperature Reverse Bias Test

This test is used to verify the long-term stability of the chips' leakage currents. During this test the device is stressed with a reverse voltage at or just below the reverse blocking capability of the device at an ambient temperature near the operational limit of the device. While no degradation in the bulk silicon is expected during these conditions, the test is able to reveal weaknesses and degradation effects at the chip edges and in the passivation layer at the chip surface. The device is considered failed if the leakage current under normal circumstances has increased too much after the test.

A similar test is performed, just with high humidity, to examine humidity related degradation processes. Even though the active components and wires of the device

is completely embedded in a silicone soft mould humidity can affect the device, as the silicone soft mould is highly permeable for humidity [4].

High Temperature Gate Stress Test

In order to test the stability of the gate leakage current a high temperature gate stress test can be used. As the gate voltage limit is around ±20 V over a gate of less than 100 nm the electric field can reach 2 MV/cm. In order for the gate to handle such a high field there has to be no defects and only a very low concentration surface charge is tolerable. The test is performed by applying a voltage at the maximum limit of the gate oxide and heating the device to the maximum operational temperature. During the test the gate leakage current has to be stable and sufficiently low. Apart from ensuring no defects in the oxide, this test ensures that no contaminants have been introduced to the device under assembly, as this would lead to surface ions that would increase the gate leakage current.

3 Experimental Part

The following sections describe how the modules used for this work have been cycled and later processed for imaging.

3.1 Devices Under Testing

The devices under testing (DUT) studied in this work are commercial power modules rated for a maximum collector-emitter voltage of 600 V and a maximum collector current of DC 30 A. Every module consists of six sections of an IGBT and a free-wheeling diode soldered to a DCB. Each chip has an Al metallization layer and four heavy Al bond wires. The module is not mounted on a baseplate. The device also contains a control chip. A top view of the device after the top plastic cover is removed is seen in Fig. 3.1.

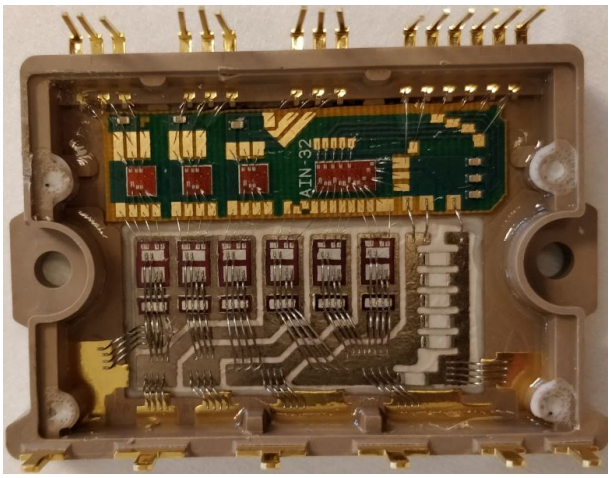
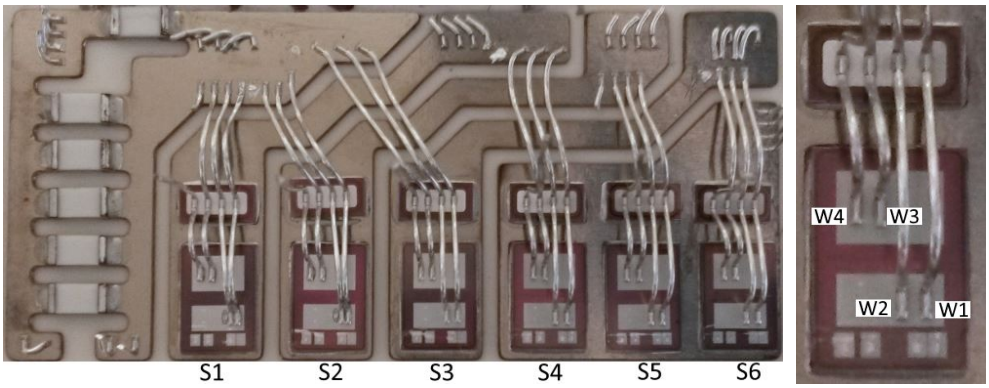


Figure 3.1 Top view of the device studied for the current work.

The modules are named P# for active power test and M# for mechanically cycled cases. Each of the six sections is numbered as S1-S6 as seen in Fig. 3.2 a. The four wires on each of the sections are numbered as W1-W4 as seen in Fig. 3.2 b. Thereby any wire can be referred to by a module number, a section number and a wire number as ”M/P# S# W#”, e.g. power cycled module one second section first wire is ”P1 S2 W1”.



(a) **(b)**

Figure 3.2 The numbering of sections (a) and wires (b).

3.2 Cycling of Device Under Testing

Two different cycling methods were used to provoke wire bond degradation during this project, ATC and pure mechanical cycling.

3.2.1 Active Temperature Cycling (ATC)

The control strategy used for ATC of samples in this project is constant t_{on} and t_{off}, constant DC load current (I_{load}) during the on-state and constant cooling. This means that the on-state voltage (V_{on}), mean temperature T_{mean} and temperature difference (ΔT) will change during the cycling. The temperature was continuously monitored throughout the cycling test using an optical fibre temperature sensor (OTG-F-10 with response time of 10 ms). In stead of turning the current on and off, the current was alternated between two IGBTs (one in either end of the device, to minimize coupling between the transistors). Because one transistor is in on-state while the other is in off-state, t_{on} and t_{off} had to be equal for the two transistors to be cycled under similar conditions. The cycling conditions for the ATC are presented in Tab. 3.1 and the evolution of V_{ce} during the cycling tests can be found in Fig: 3.3.

Table 3.1 Cycling conditions for ATC.

Module Section	I_{on} (A)	t_{on}/t_{off} [s]	T_{min}/T_{max} [°C]	ΔT [°C]	Cycles	Increase of V_{ce} [%]
P1 S1	23	1.5/1.5	60/100	40	149×10^3	6.44
P1 S6	23	1.5/1.5	60/100	40	149×10^3	6.31
P2 S1	22	1.5/1.5	60/100	40	406×10^3	2.38
P2 S6	22	1.5/1.5	20/100	40	406×10^3	6.93
P3 S1	18	2.5/2.5	50/110	60	444×10^3	1.85
P3 S6	18	2.5/2.5	50/110	60	444×10^3	2.16

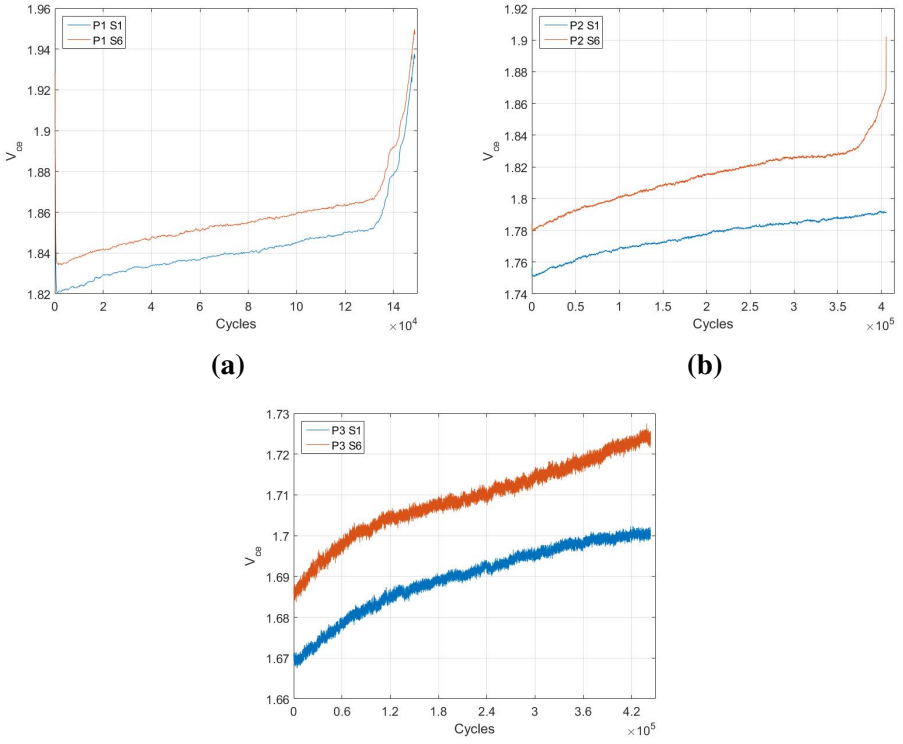


Figure 3.3 The evolution of V_{ce} during ATC tests for P1 (a), P2 (b) and P3 (c).

3.2.2 Mechanical Cycling (MC)

Mechanical cycling was carried out in the group of Golta Khatibi at Technical University of Vienna in the frameworks of running collaboration [14]. This is a high frequency mechanical fatigue procedure used as an alternative for ATC when studying bond wire fatigue [5]. This approach makes it possible to utilize a large span of frequencies, from under one Hz and up to tens of kHz. This allows for very fast cycling compared to ATC, where each cycle normally takes several seconds. MC will only evoke wire bond degradation and not any other failure mode, such as solder fatigue and metallization reconstruction, as traditional temperature cycling would. While this is different from field conditions, it allows for studying one failure mode, without it being affected by other failure modes.

Even though it is possible to perform the cycling at very high frequencies, this might result in a different degree of degradation compared to devices from real operational conditions. Determination of proper cycling frequencies is required.

When determining the proper frequency it will be a compromise between the time spend on cycling and the risk of deviations in the results [9].

In practice, the shear load is applied by clamping the wedge area of the bonds with a gripping tool and vibrating it along the direction of the wedge, parallel to the substrate, while the substrate is fixed on a vacuum stage. A piezoelectric actor is used to move the gripping tool, causing the displacement load. A differential laser Doppler vibrometer measures the displacement of the tip of the grippers and the edge of the IGBT chip. The wire is clamped around roughly half of the wire width. The clamping force of the gripping tool causes deformation of the wire. Tests where the wire is glued to the tip instead of gripped have been made, to determine if this deformation had any affect on the lifetime of the wire bond. These showed similar results for both methods, indicating that the deformation of the upper part of the wire has no significant impact on the lifetime of the wire bond [9]. In order to prevent re-bonding and grinding, a small tensile load of 0.2 N is applied in the z-direction. The set-up is illustrated in Fig. 3.4.

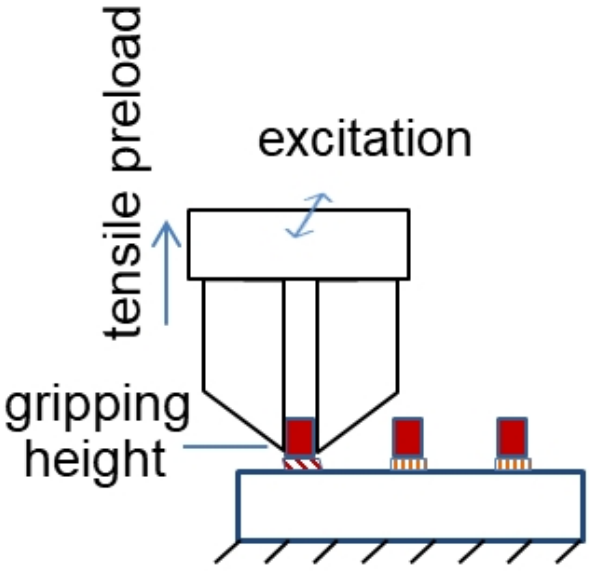


Figure 3.4 Illustration of the set-up used for MC.

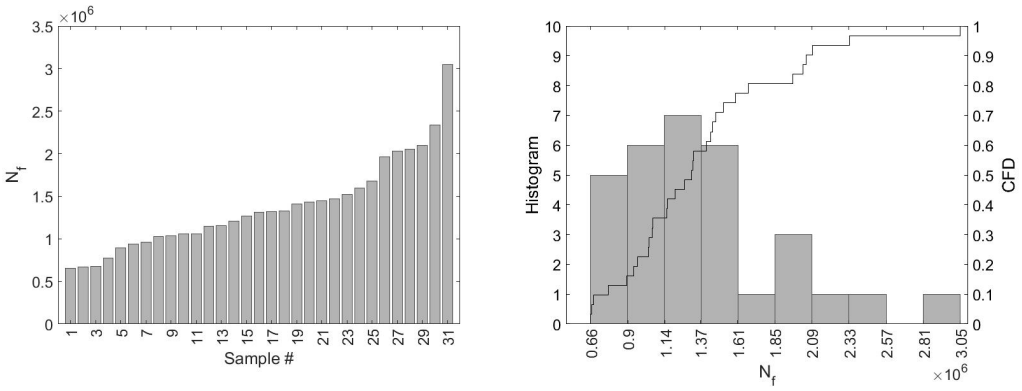
MC simulates the cyclic shear stresses at bonding interfaces caused by varying temperature, by mechanically inducing a similar cyclic shear load in the wire bond. This shear load causes fatigue cracks to initiate at the bonding interface and propagate and, depending on the applied displacement amplitude and the time of the test, eventually causing wire lift-off. The shear strain at the interface between Al and Si ($\Delta\varepsilon$), as defined in Eq. 3.1, is related to the temperature change (ΔT)

through the difference in CTE of Al and Si ($\Delta\alpha$), as described in Sec. 2.2.1 Eq. 2.3.

$$\Delta\varepsilon \approx \underbrace{(\alpha_{Al} - \alpha_{Si})}_{\Delta\alpha} \Delta T \tag{3.1}$$

This can be related to a mechanically induced shear force, as the shear stress (τ) is given as $\tau = \frac{F}{A}$, where F is the applied force and A is the interface area. F can be found by measurements of acceleration of the chip with respect to the gripping tool as $F = m\,a$, where m is the mass of the chip and a is the acceleration. This shear stress is related to the shear strain through the shear modulus ($G = 27.8\,\text{GPa}$ for Al [33]) as $\Delta\varepsilon = \Delta\tau/G$ [34].

For this project a displacement amplitude of 225 nm was used and the samples were cycled at a frequency of ~60 kHz. 31 wires were cycled to EOL, resulting in the data illustrated in Fig. 3.5. EOL (wire lift-off) was found to between 1,2-1.3 $\times 10^6$ cycles; this is further mentioned as 100 % EOL. This pretty high variation in EOL is probably related to differences in production quality of wire bonds. The deviation ranges from 10 % failed at 8×10^5 cycles and 90 % failed at 2×10^6 cycles.



(a) **(b)**

Figure 3.5 Number of cycles to failure (N_f) for 31 mechanically cycled wire bonds (a) and a histogram and cumulated frequency distribution of N_f for these wire bonds (b).

For wire bonds examined in current work, the cycling was stopped at different points prior to the expected failure. The number of cycles for each sample can be found in Tab. 3.2.

Table 3.2 Number of cycles for MC modules.

Module Section	% of EOL	Module Section	% of EOL	Module Section	% of EOL
M6 S1	100	M7 S1	80	M12 S1	100
M6 S2	100	M7 S2	80	M12 S2	10
M6 S3	30	M7 S3	100	M12 S3	20
M6 S4	30	M7 S4	80	M12 S4	30
M6 S5	60	M7 S5	95	M12 S5	50
M6 S6	60	M7 S6	95	M12 S6	70

3.3 Micro-sectioning

In order to obtain a cross-sectional view of the wire bond, micro-sectioning was performed. The process of micro-sectioning can be divided into two parts: Macroscopic cutting to separate the module into individual sections followed by microscopic grinding/polishing to remove DCB substrate, reaching the center of the wire and smoothing the surface. In this project a section consists of an IGBT and a free-wheeling diode. The following steps are performed during the macroscopic cutting:

- The cover from the plastic housing is removed and the silicon gel is dissolved using silicone remover.
- The wires connecting the DCB to the housing and control circuit are cut and the DCB along with the active components are removed from the housing.
- The DCB and the active components are cast into epoxy for protection.
- The individual sections are separated using a diamond wet cut blade and the sections are individually cast into epoxy with the DCB facing down.

The following steps are performed during microscopic grinding/polishing:

- The DCB and the chip solder are removed using SiC wet grinding paper for the Cu and solder, and a diamond grinding disc.

- The sections are recast, this time with the first wire of interest facing down.
- SiC wet grinding paper is used to remove material until the center of the desired wire is reached (finishing with 4000-grit).
- The surface is polished, initially with 3 µm diamond suspension, ending with OPu until the desired smoothness is reached.

After completing the micro-sectioning, cracks can be observed using optical microscopy. In order to see the grain structure, the grains have to be developed using electro-etching.

3.4 Grain Development by Electro-Etching

After micro-sectioning, in order to promote the Al grain structure, the samples were anodized in Barker's reagent. The reagent was made from 5 mL 48 wt % HBF_4 in H_2O diluted in 195 mL H_2O. In order to get electrical contact to the sample, a hole was drilled into the epoxy reaching a Cu contact attached to diode end of the fourth wire in the sample. A screw was screwed into the hole, connecting with the Cu contact. The sample was then held in the reagent, so that the screw was not in direct contact with the solution. A cathode of a thin non-reactive metal plate was placed in the solution too. An illustration of the set-up can be seen in Fig. 3.6. A potential of 10 V was used to drive the reaction. During the reaction the solution was stirred using a magnetic stirrer. The necessary reaction time varied slightly from sample to sample, but most of the samples were done after just under 2 min.

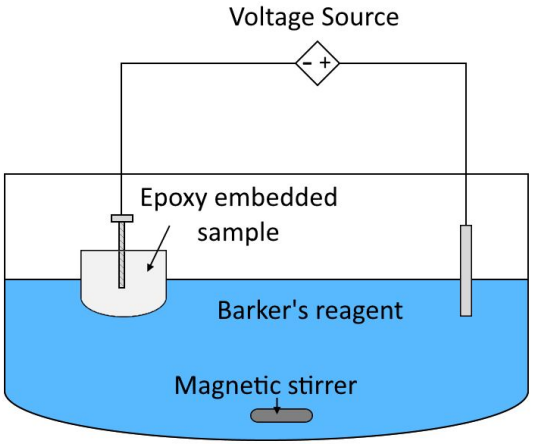


Figure 3.6 Illustration of the set-up used for the anodizing process used to devolop grain structure in Al wires.

When the Al is used as an anode in a Barker's reagent, an oxide layer grows on the Al surface. The oxide growth is dependant on the grain orientation, different oxide thickness and roughness is seen between different orientated grains. These differences cause different colors to appear when looking at the sample through a microscope using a polarized light source.

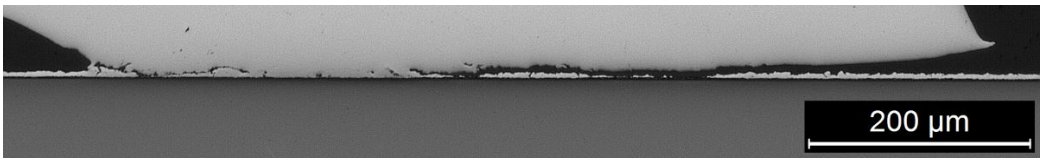
4 Results and Discussion

After micro-sectioning it is possible to see the crack propagation at the wire-bond interface using an optical microscope. In the following sections the obtained results from first the ATC samples and then the MC samples are presented and discussed. Finally, results from the two methods are compared.

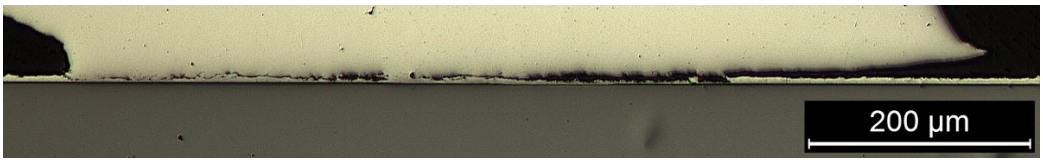
4.1 Crack Propagation in ATC Devices

Two sections of each module were cycled. The cycling conditions can be found in Tab. 3.1 in Sec. 3.2.

Normally a device is considered to enter the failure mode related to wire lift-off at an increase of 5 % in V_{ce}. Three sections are cycled beyond this point: P1 S1 (6.44 %), P1 S6 (6.31 %) and P2 S6 (6.93 %). Due to the high increase in V_{ce} of these sections, it is expected to see wire lift-off or wires that are very close to lift-off. This is the case for P1 S1 W1 (Fig. 4.1 a), P1 S1 W2 (Fig. 4.1 b), P2 S6 W1 (Fig. 4.1 e) and P2 S6 W2 (Fig. 4.1 f). The wires of P1 S1 still have a very small contact area intact, whereas for P2 S6 one can see a complete detachment.

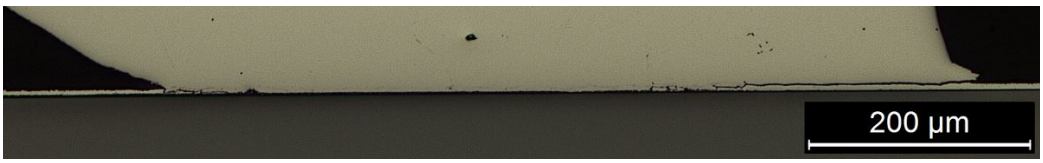


(a) P1 S1 W1 (ΔV_{ce}=6.44 %).



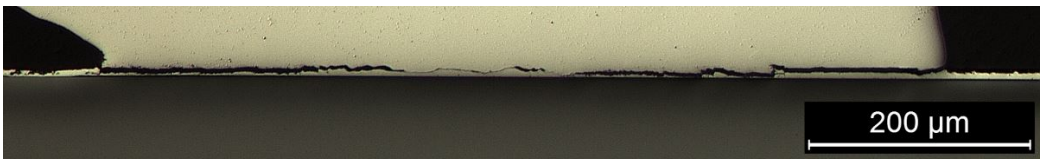
(b) P1 S1 W2 (ΔV_{ce}=6.44 %).

(c) P1 S6 W1 (ΔV_{ce}=6.31 %).



(d) P1 S6 W2 (ΔV_{ce}=6.31 %).

(e) P2 S6 W1 (ΔV_{ce}=6.93 %).



(f) P2 S6 W2 (ΔV_{ce}=6.93 %).

Figure 4.1 Optical microscope images of ATC wire bonds for IGBTs cycled to ΔV_{ce} >5 %.

Despite the high increase in V_{ce} in P1 S6 the wire bonds of both W1 (Fig. 4.1 c) and W2 (Fig. 4.1 d) have a large contact area left. As only two out of four wires were examined it might be due to severe degradation of the remaining two wire bonds. However, when examining the rapid increase in V_{ce} towards the end of the

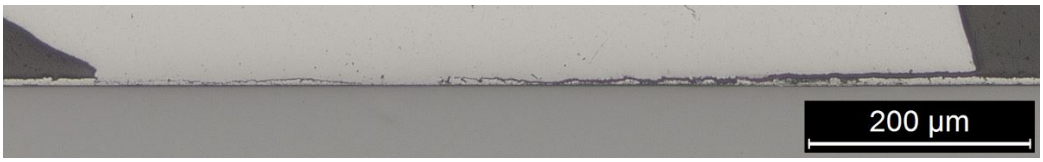
cycling test (Fig. 3.3 b), it is found that V_{ce} seems to increase continuously, and not in steps as would be expected in case of wire lift-off (seen in Fig. 3.3 a). This, along with the low degree of degradation of the wire bonds that have been examined, indicates that the reason for the high increase in V_{ce} might lie elsewhere, e.g. metallization degradation.

In Fig. 4.1 a – d the remaining contact area is near the center of the bond (slightly shifted to the heel side), indicating that the cracks propagate from both ends of the bond towards the center. The same is seen in wires cycled to a lesser degree (Fig. 4.2). The shift towards the heel might be due to temperature gradients, causing a difference in the stresses at the heel and toe. Furthermore, The quality of the bond might be uneven across the bonding interface.

The other sections of the modules exposed to ATC had an increase in V_{ce} ranging from 1.85 % for P3 S1 to 2.38 % for P2 S1. As this is a relatively low increase in V_{ce}, a low degree of degradation of the wire bonds is expected. This is the case for P3 S1 and S6 where cracks are seen propagating from both heel and toe but still showing a large intact area. P2 S1 on the other hand shows severe degradation with W1 (Fig. 4.2 a) being very close to lift-off and W2 (Fig. 4.2 b) seems to have lift-off. This is highly unexpected, as the electrical data indicates only moderate degradation. This can be related to the large variations in production quality of the wire bonds, thus, leading to high difference in degradation rates.

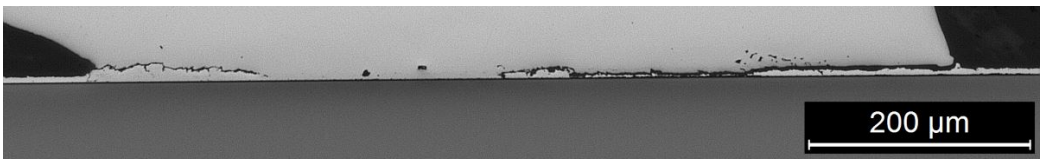
It has been suggested that the remaining contact area normalized with the wire height as a function of the number of cycles should follow Paris' law (Eq. 2.6) [35]. In order to tell if this relation is present here, more data of similar cycling conditions is needed.

When looking at the path of the cracks, it is found that the cracks propagate mainly between the metallization and the wire or in the metallization. At some places it even seems that the crack develops along the metallization-chip interface. This is seen in at least parts of all examined wire bonds. In a few of the interfaces (P3 S1 W1 seen in Fig. 4.2 c at the heel and P1 S6 W2 seen in Fig. 4.1 c at the toe) the cracks propagate in the wire. The fact that the cracks mainly propagate through the metallization-wire interface, or through the chip metallization is unusual. Typically it would be expected that the crack would follow the boundary between the original grain structure of the wire and its refinement area formed under the bonding process [8]. Cracks have been observed propargating 10 – 20 µm above the wire-metallization interface along this refinement area [10].

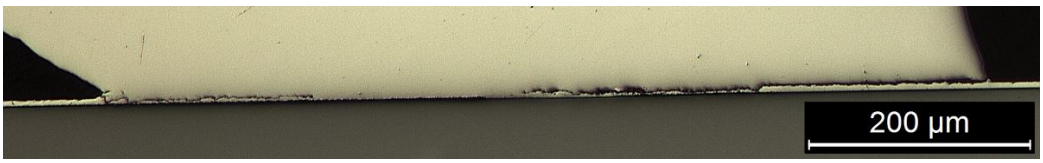


(a) P2 S1 W1 (ΔV_{ce}=2.38 %).

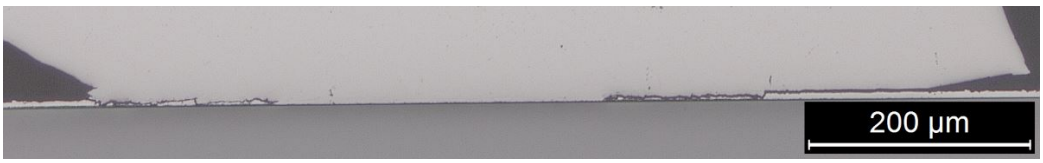
(b) P2 S1 W2 (ΔV_{ce}=2.38 %).



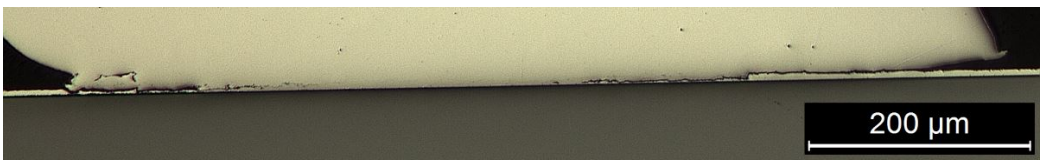
(c) P3 S1 W1 (ΔV_{ce}=1.85 %).



(d) P3 S1 W2 (ΔV_{ce}=1.85 %).



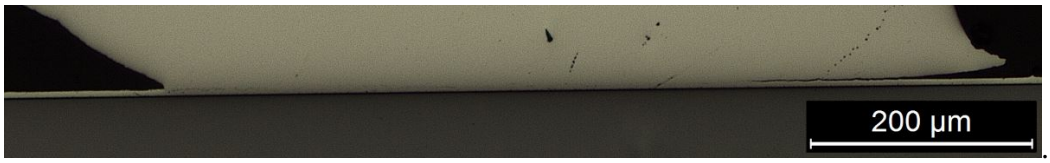
(e) P3 S6 W1 (ΔV_{ce}=2.16 %).



(f) P3 S6 W2 (ΔV_{ce}=2.16 %).

Figure 4.2 Optical microscope images of ATC wire bonds for IGBTs cycled to ΔV_{ce} <5 %.

By closely examining the wire bond of a mint IGBT (Fig. 4.3) defects (dark spots) along the wire-metallization interface can be seen. Similar defects can be found in all the samples examined, indicating that the unusual path of the cracks might be due to poor bond quality.



(a)

(b)

Figure 4.3 Optical microscope images of a mint IGBT wire bond. (a) shows the entire wire bond while (b) shows the heel at greater magnification.

In order to examine the refinement area electro-etching was used to develop the grain structure on some of the wires. This showed that the grains are smaller near the interface, however they are still relatively large and no clear boundary between large and small grains is seen. Cracks do not tend to go above smaller grains but propagate in between or below. This all shows that the refinement area in the wires examined is very weak if at all present. As the cracks propagate mainly between metallization and wire or in the metallization, intergranular fracturing is seen. No clear trans-granular fractures have been observed as it has been in other work [20].

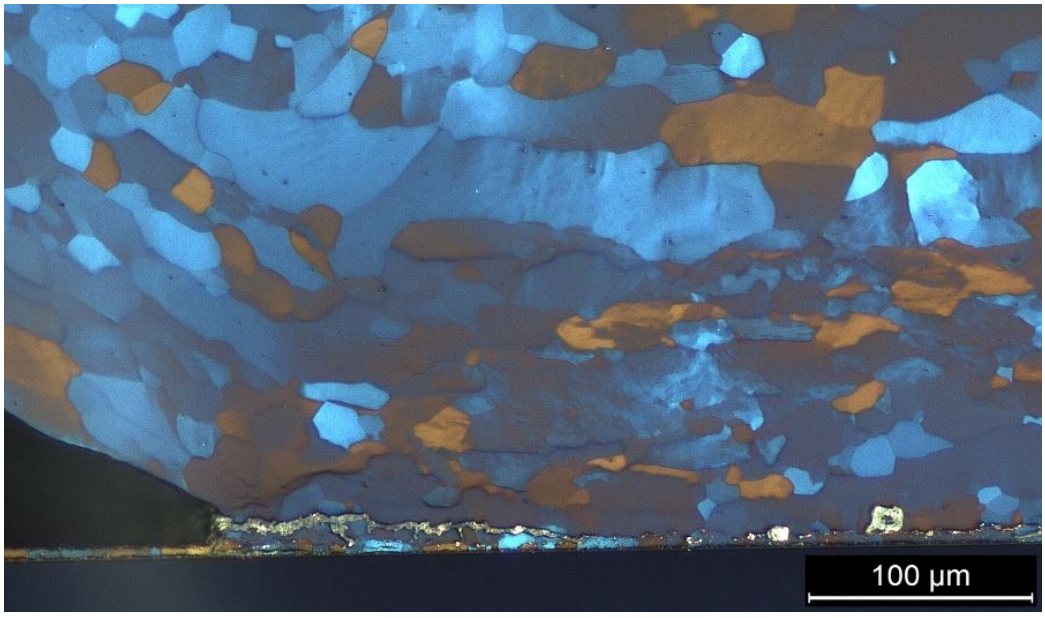


Figure 4.4 Grain structure of P3 S1 W1 at the heel of the IGBT wire bond.

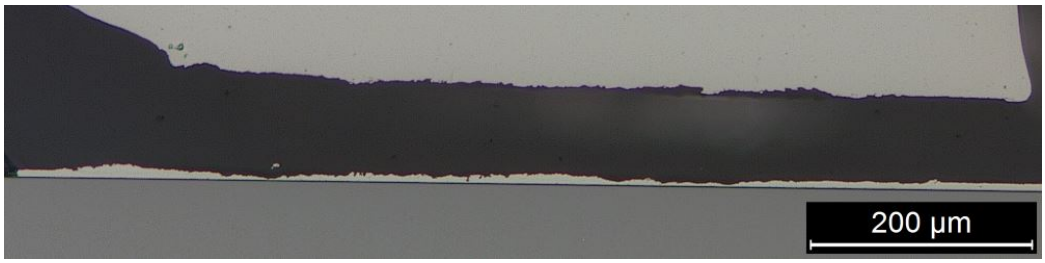
To summarize, for ATC it has been found that the cracks propagate mainly in the wire-metallization interface, in the metallization or in the metallization-chip interface, which is unlike what has been seen in previous studies, where the cracks tend to propagate just above the refinement area in the wire material. Defects have been found in the wire-metallization interface both for mint and cycled wires, which could be the reason for the unexpected fracture path.

The grain structure does not show any clear refinement area near the interface, as is normally seen in US bonded wires. This further indicates that the fracture path might be due to poor bonding conditions. It is expected that an optimization of the bonding conditions could significantly increase the lifetime of these wire bonds, and would result in a more traditional fracture path.

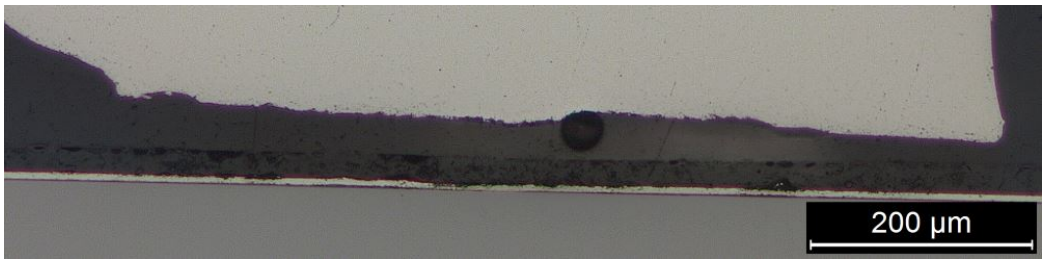
More data of ATC wire bonds is needed in order to conclude on the crack propagation rate.

4.2 Crack Propagation in MC Devices

For MC every wire within a section has been cycled similarly, while the sections have been cycled to a different number of cycles, indicated as the percentage to expected EOL as listed in Tab. 3.2 in Sec. 3.2.2. The sections M6 S1, M6 S2, M7 S3 and M12 S1 have been cycled to 100 % of expected EOL why it is expected to see lift-off of most of the wires of these sections. This is in fact the case for every wire examined on these sections (example in Fig. 4.5 a for M7 S3 W1). Lift-off is also seen in all examined wires of M7 S5 and M7 S6 (M7 S6 W1 is seen in Fig. 4.5 b) cycled to 95 % of EOL. Due to the variation in EOL of the 31 wires used to determine the expected EOL, it would be expected to see some wires that have not failed when cycled to expected EOL. The fact that 12 wires cycled to 95 % and 100 % of expected EOL, all show lift-off indicates that the expected lifetime might be too high.



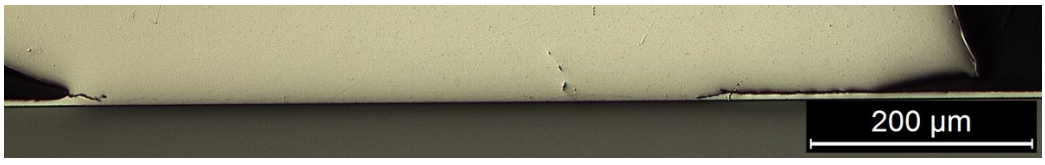
(a) M7 S3 W1 (100 %).



(b) M7 S6 W1 (95 %).

Figure 4.5 Optical microscope images showing wire lift-off seen after MC to 100 % (a) and 95 % (b) of expected EOL.

M7 S1, S2 and S4 were all cycled to 80 % of EOL. Here it would be expected to see a large degree of damage to the wire bond, and it would not be unexpected to see wire lift-off in one of the wires, as according to the data from the 31 wires tested to EOL, just over 20 % of wires would have failed at 80 % of expected EOL. However, when examening the wire bonds of these samples there is a lot of intact contact area between the chip and wire. Examples of this are seen in Fig. 4.6.



(a) M7 S1 W2 (80 %).

(b) M7 S2 W1 (80 %).

Figure 4.6 Optical images of MC wires cycled to 80 %.

Wires cycled to between 10-70 % show increasing crack growth for an increasing number of cycles, as would be expected. This can be seen in Fig. 4.7 a – c showing wire bonds cycled to 10, 30 and 60 % of expected EOL. One wire at 50 % of EOL had lifted off.

(a) M12 S2 W2 (10 %).

(b) M6 S3 W1 (30 %).

(c) M6 S6 W1 (60 %).

Figure 4.7 Optical microscope images of wire bonds cycled to 10 % (a), 30 % (b) and 60 % (c) of expected EOL.

The fractures of MC are more opened compared to those of ATC. This is clearly seen both at the heel and toe fracture in Fig. 4.7 c. This could be due to the small pre-load applied perpendicular to the interface, used to prevent grinding and re-bonding during the cycling.

For the rest of the wires cycled from 10 % to 70 % of EOL, the remaining contact width (d_c) was measured and normalized with their measured hight (d_h) and plotted against the percentage of expected EOL (Fig. 4.8). Imprecisions in the position of the wire cross sections examined will affect d_c. This can be accomodated by normalization by d_h as suggested in [35].

As suggested in [35] one could fit the data with a power function. However due to the large deviation, especially at a high number of cycles, for data obtained in this work, and the small data-pool the fit is not that good. The large deviation also means that a lot of other functions can be fitted to the data with similar precision. In fact an exponential fit is better for this data, and a linear fit is only slightly

worse, as is shown in Fig. 4.8. Therefore it is impossible to confirm or contradict if the wire degradation follows a power function as it has been suggested.

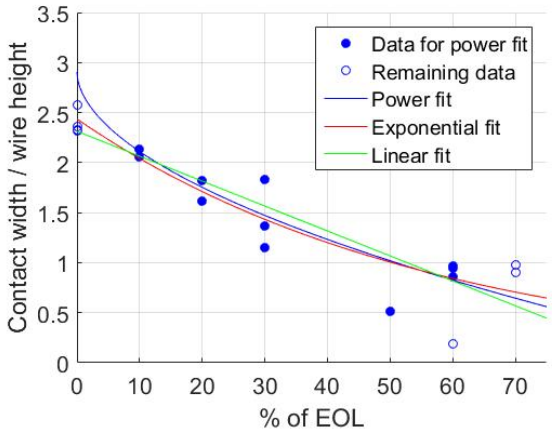
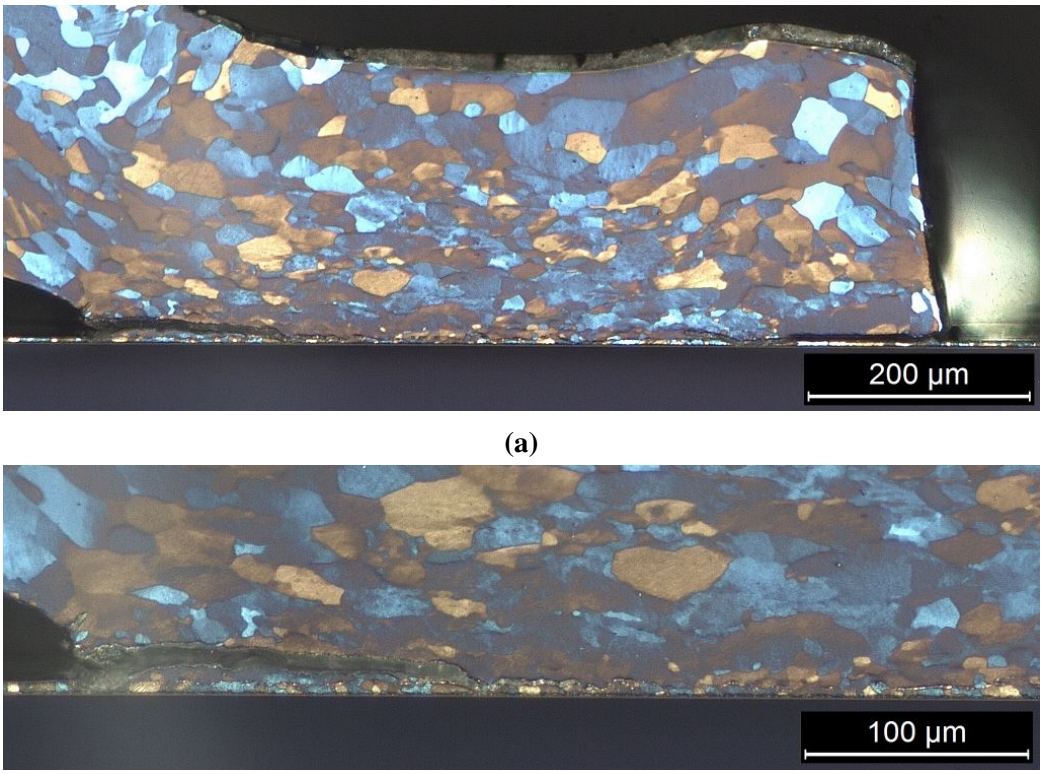


Figure 4.8 The ratio between the remaining contact length and the wire height plotted against number of cycles in percentage of expected EOL, along with different fits.

When looking at the fracture path, both delamination, where the fracture occurs in the interface between metallization and wire and between the metallization and the chip, is seen. However, a larger part of the fracturing occurs in the wire material too (e.g. Fig. 4.7 c at the toe), as it is seen in well-bonded wires with a good refinement area.

When looking at the grain structure, smaller grains are found all over the wire compared to those found in ATC samples, indicating that the MC process might cause grain reconstruction. This can be seen in Fig. 4.9 a. The reconstruction could also be a consequence of the deformation of the wire caused by the applied force from the gripping tool, however the reconstruction is seen in the entire wire height, and not only in the top part where the wire is deformed by the gripping. When looking near the wire-chip interface even smaller grains can be seen (Fig. 4.9 b). This could indicate that the MC process is generating a refinement area during the cycling. This could affect the fracture path so more propagation occurs in the wire material compared to the ATC samples, as the MC might cause strengthening of the material just at the interface.



(a)

(b)

Figure 4.9 Optical microscope images of MC wire bond after electro-etching. The entire wire bond is seen in (a) and the heel is seen at greater magnification in (b).

To summarize, for MC it is found that while some crack propagation occurs in the wire-metallization interface, the metallization or in the metallization-chip interface, more fractures propagate in the wire material compared to what is seen for the ATC samples.

When looking at the grain structure, it is found that the grains are smaller than those seen in ATC throughout the wire height, indicating that the MC process could cause grain reconstruction. Near the interface even smaller grains are seen, which could indicate that the MC process generates a refinement area. This could also explain the difference in the fracture path between ATC and MC, as the MC process might harden the material near the interface, strengthening the bond and causing the fracture to propagate into the wire material. This will not happen during normal operation, why this could be an issue for using MC to estimate wire bond life time. Changing the cycling parameters e.g. lowering the frequency could have an effect on this reconstruction.

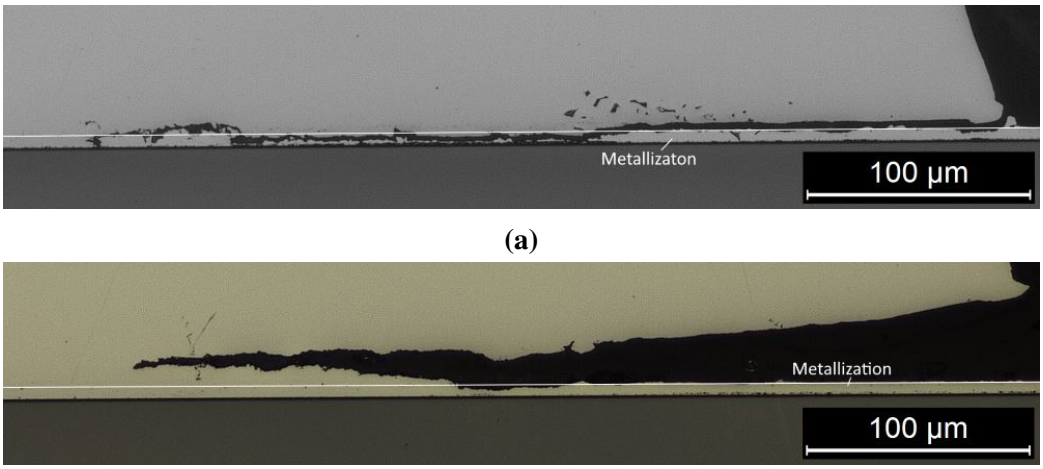
When looking at the remaining contact area normalized with the wire height, plotted against the number of cycles (Fig. 4.8), one could fit it with a power function as suggested in [35]. However, the large deviation and the small data-pool give a poor fit and other functions could be used to fit the data just as well if not better. Therefore it can neither be confirmed nor rejected that the the normalized contact area will follow a power function while plotted as a function of the number of cycles.

4.3 Comparison of ATC and MC

Differences in both fracture path and grain structure is seen when comparing results from ATC and MC. Furthermore, the fracture of MC is more opened than that of ATC, which could be due to the small pre-load perpendicular to the interface, used to prevent grinding and re-bonding during MC.

The fracture path of MC samples propagates more in the wire material compared to ATC, where cracks mainly propagate in or below the interface of the wire and metallization. This difference is clearly seen when comparing Fig. 4.10 a for an ATC wire bond and Fig. 4.10 b for an MC wire bond. The white line indicates the wire-metallization interface, and it is clearly seen that for the ATC wire the crack propagates mainly below or on the line, while for the MC wire, the crack propagates on or above the line.

Furthermore, when comparing Fig. 4.10 a and Fig. 4.10 b it can be seen that the fracture of Fig. 4.10 b (MC) is more opened than that of Fig. 4.10 a (ATC).

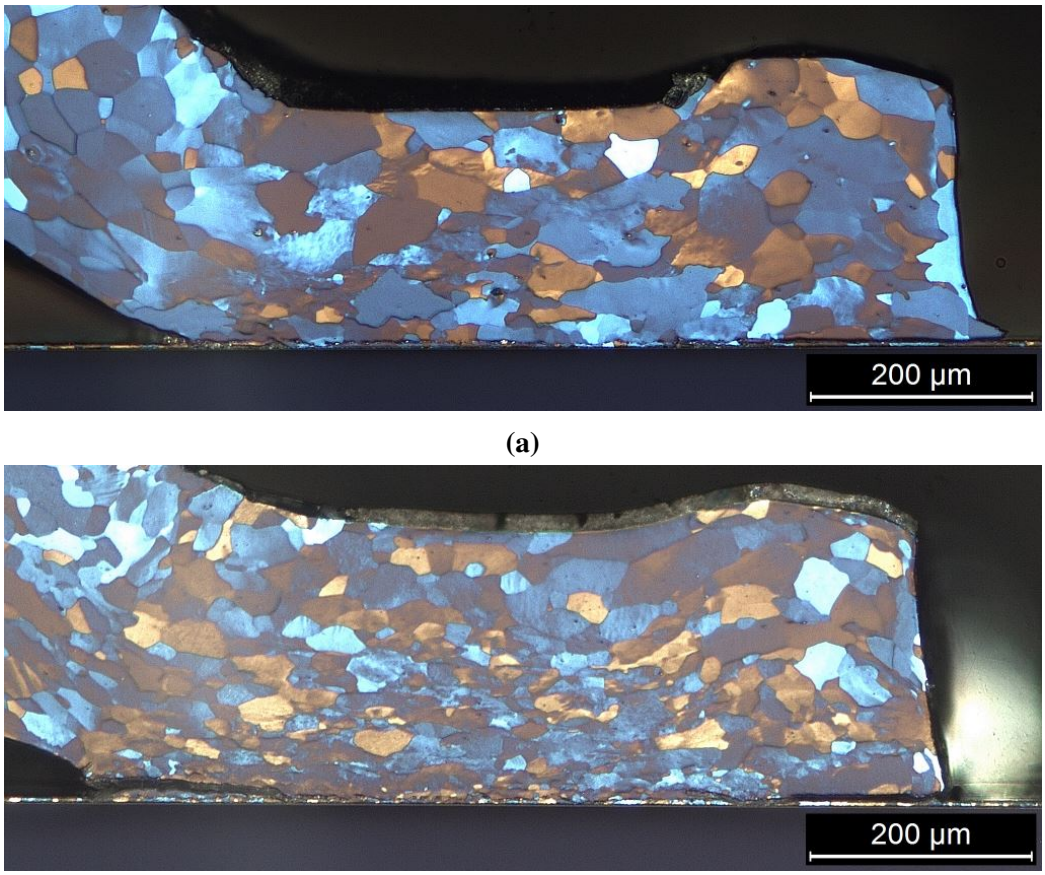


(a)

(b)

Figure 4.10 Optical microscope images showing crack propagation with respect to the wire-metallization interface of an ATC (a) and MC (b) bond wire.

MC samples tend to have smaller grains than ATC samples, which indicates that the MC process might cause grain reconstruction in the wires. This difference is seen throughout the wire height. This difference is clearly seen comparing Fig. 4.11 a (ATC) to Fig 4.11 b (MC), where the grains in Fig. 4.11 b in general seems smaller than those seen in Fig. 4.11 a. This is even more pronounced near the chip at the center of the bond, where the grains are significanty smaller than any of the grains seen in the ATC wire. The very small grains near the chip surface could indicate that the MC process causes the formation or enhancement of the refinement area, and thereby strengthening the bond, causing the crack to propagate in the wire material. This could be an issue for using MC to estimate the wire bond life time, as this reconstruction would not occur during normal operation.



(a)

(b)

Figure 4.11 Optical images showing the grain structure of an ATC (a) and MC (b) bond wire.

To summarize, it is found that the path of the crack for ATC samples mainly go at or below the wire-metallization interface, while for MC samples it mainly propagates at or above this interface.

The cracks of the MC wires are more opened than those of ATC wires, which could be due to the pre-load perpendicular to the interface, applied during MC to prevent grinding and re-bonding.

The grain structure of the wires are also different, with the MC wires having more smaller grains and what looks like a larger refinement area with smaller grains than what is found in ATC wires. This difference in grain size is suspected to be due to grain reconstruction during MC, and may be the reason for the differences in the fracture path.

In order to compare the fracture propagation rate, more data is needed for both cycling methods. The reconstruction occurring during MC could affect the lifetime of the bond, why this may be an issue for using MC to estimate lifetime of wire bonds operating at field conditions. Changing cycling conditions such as cycling frequency could have an effect on the amount of reconstruction caused by MC. More research into the affect of MC on the wire bond is needed in order for this to be a reliable method for lifetime estimation of wire bonds.

5 Conclusion

In order to compare the degradation of wire bonds exposed to ATC and MC, micro-sectioning was used to analyse the crack development in ATC and MC wire bonds. For further comparison between the two cycling methods, some samples were electro-etched in order to develop the grain structure.

For ATC it was found that the fracture path did not follow the expected path in the wire material, but rather propagated in the wire-metallization interface, in the metallization or in the metallization-chip interface. Defects were found in the wire-metallization interface for both mint and cycled devices, which could be the reason for the unexpected crack development. Furthermore, by examining the grain structure of the wire-metallization interfaces, it was found that there was very little to no refinement area formed at the wire bonds. The defects found at the interface along with the missing refinement area indicate that the unexpected fracture path could be due to poor US bonding of the wires. In order to conclude on the rate of crack development for ATC devices more cycled modules need to be produced and investigated.

Examination of the fracture path for MC devices showed some fracturing occurring in or below the wire-metallization interface, however, a tendency for the crack to develop more in the wire material was seen. This could be due to the small pre-load applied perpendicular to the interface to prevent grinding and re-bonding during cycling. The cracks also had a tendency to be more opened compared to the pwer cycled modules which can also be due to this pre-load. Examination of the grain structure of the MC wires showed smaller grains for the entire wire height compared to the ATC wires. This indicates that the MC process might cause grain reconstruction. Even smaller grains were observed near the chip, indicating

that the cycling could be forming or strengthening already present refinement areas. This generation of refinement area could also explain the difference between crack path between ATC and MC wires. Further research into grain reconstruction during MC and its effect on the lifetime is needed, in order for MC to be a useful tool for wire bond lifetime estimation.

It has been suggested that the ratio between remaining contact width and the measured wire height should be dependant on the number of cycles with a power law. It has not been possible to neither confirm nor reject this, as the deviation of the data was to large and there were insufficient data.

It can be concluded that for the MC cycling conditions used for samples examined in this work, the crack development tendencies are similar to those found for the ATC devices for the earlier and moderate stages of lifetime. However, the MC devices cycled closer to EOL show some differences in the lift-off development compared to the power cycling. Thus, it is still necessary to resolve whether this discrepancy is related to the procedure of MC leading to damage accumulation different to that of ATC or rather the large deviation in production quality which can lead to significant differences in the fatigue processes from batch to batch of the modules. This further investigation could help in the final conclusion on the acceptance of the mechanical cycling accelerated test for the reliability evaluation of wire bonds.

Bibliography

[1] Kristian Bonderup Pedersen. *IGBT Module Reliability - Physics of Failure Based Characterization and Modelling*. PhD thesis, Aalborg University, 2014.

[2] Mauro Ciappa. Selected failure mechanisms of modern power modules. *Microelectronics Reliability*, 42:653–667, 2002.

[3] Andreas Volke and Michael Hornkamp. *IGBT modules - Technologies, driver and application*. Infineon Technologies AG, 2017.

[4] Josef Lutz, Heinrich Schlangenotto, Uwe Scheuermann, and Rik De Doncker. *Semiconductor Power Devices - Physics, Characteristics, Reliability*. Springer, 2011.

[5] Golta Khatibi, Martin Lederer, Bernhard Czerny, Agnieszka Betzwar Kotas, and Brigitte Weiss. A New Approach for Eevaluation of Fatigue Life of Al Wire Bonds in Power Electronics. Technical report, Faculty of Physics, University of Vienna, 2014.

[6] *Fuji IGBT-IPM Application Manual*.

[7] I. F. Kovačevič, U. Drofenik, and J. W. Kolar. New Physical Model for Lifetime Estimation of Power Modules. In *The 2010 International Power Electronics Conference*, 2010.

[8] Kristian Bonderup Pedersen, David Benning, Peter Kjær Kristensen, Vladimir N. Popok, and Kjeld Pedersen. Interface structure and strength

of ultrasonically wedge bonded heavy aluminium wires in Si-based power modules. *Journal of Materials Science: Materials in Electronics*, 25:2863–2871, 2014.

[9] B. Czerny and G. Khatibi. Interface reliability and lifetime prediction of heavy aluminum wire bonds. *Microelectronics Reliability*, 58:54–72, 2016.

[10] Jens Goehre, Martin Schneider-Ramelow, Ute Geißler, and Klaus-Dieter Lang. Interface Degradation of Al Heavy Wire Bonds on Power Semiconductors during Active Power Cycling measured by the Shear Test. In *CIPS 2010*, 2010.

[11] Yizhou Lu, Student Member, and Aris Christou. Lifetime Estimation of Insulated Gate Bipolar Transistor Modules Using Two-Step Bayesian Estimation. *IEEE Transactions on Device and Materials Reliability*, 17:414–421, 2017.

[12] Pramod Ghimire, Kristian Bonderup Pedersen, Angel Ruiz de Vega, Bjørn Rannestadrn Rannestad, Stig Munk-Nielsen, and Paul Bach Thøgersen. A real time measurement of junction temperature variation in high power IGBT modules for wind power converter application. In *CIPS 2014*, pages 42–47, 2014.

[13] Jacob Lubliner and Panayiotis Papadopoulos. *Introduction to Solid Mechanics - An Integrated Approach*. Springer, 2017.

[14] G. Khatibia, M. Lederera, B. Weissa, T. Lichtb, J. Bernardic, and H. Danningerd. Accelerated Mechanical Fatigue Testing and Lifetime of Interconnects in Microelectronics. *Procedia Engineering*, 2(1):511–519, 2010.

[15] W. D. Zhuang, P. C. Chang, F. Y. Chou, and R. K. Shiue. Effect of solder creep on the Reliability of large area die attachment. *Micrielectrinics Reliability*, 41:2011–2021, 2001.

[16] Mounira Bouarroudj, Zoubir Khatir, Jean-Pierre Ousten, and Stéphane Lefebvre. Temperature-Level Effect on Solder Lifetime During Thermal Cycling of Power Modules. *IEEE Transactions on Device and Materials Reliability*, 8:471–477, 2008.

[17] Bing Ji, Xueguan Song, Wenping Cao, Volker Pickert, Yihua Hu, John William Mackersie, and Gareth Pierce. In Situ Diagnostics and Prognostics of Solder Fatigue in IGBT Modules for Electric Vehicle Drives. *IEEE Transactions on Power Electronics*, 30:1535–1543, 2015.

[18] Dimosthenis C. Katsis and Jacobus Daniel van Wyk. Void-Induced Thermal Impedance in Power Semiconductor Modules: Some Transient Temperature Effects. *IEEE Transactions on Industry Applications*, 39:1239–1246, 2003.

[19] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech*. Fast Power Cycling Test for IGBT Modules in Traction Application. In *Proceedings of Second International Conference on Power Electronics and Drive Systems*, 1997.

[20] Kristian Bonderup Pedersen, Lotte Haxen Østergaard, Peter Kjær Kristensen, Pramod Ghimire, Vladimir N. Popok, and Kjeld Pedersen. Degradation Evolution in High Power IGBT Modules Subjected to Sinusoidal Current Load. *Materials in Electronics*, VOL. 27(No. 2):1938–1945, February 2016.

[21] Niels Hansen. Hall-Petch relation and boundary strengthening. *Scripta Materialia*, 51:801–806, 2014.

[22] Hua Lu, Chris Bailey, and Chunyan Yin. Design for reliability of power electronics modules. *Microelectronics Reliability*, 49:1250–1255, 2009.

[23] Li Yang, Pearl A. Agyakwa, and C. Mark Johnson. Physics-of-Failure Lifetime Prediction Models for Wire Bond Interconnects in Power Electronic Modules. *IEEE Transactions on Device and Materials Reliability*, pages 9–17, 2013.

[24] H.Wang, M. Liserre, and F. Blaabjerg. Toward reliable power electronics: Challenges, design tools, and opportunities. *IEEE Industrial Electronics Magazine*, vol. 7(No. 2):17–26, 2013.

[25] Huai Wang, Marco Liserre, Frede Blaabjerg, Peter de Place Rimmen, John B. Jacobsen, Thorkild Kvisgaard, and Jorn Landkildehus. Transitioning to Physics-of-Failure as a Reliability Driver in Power Electronics. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2:97–114, 2014.

[26] Michael Pecht and Gu Jie. Physics-of-failure-based prognostics for electronic products. *Transactions of the Institute of Measurements & Control*, 31:309–322, 2009.

[27] Kristian Bonderup Pedersen and Kjeld Pedersen. Dynamic Modelling Method of Electro-Thermo-Mechanical Degradation in IGBT Modules. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 31:975–986, 2016.

[28] Vladimir N. Popok, Kristian B. Pedersen, Peter K. Kristensen, and Kjeld Pedersen. Comprehensive physical analysis of bond wire interfaces in power modules. *Microelectronics Reliability*, 58:58–64, 2016.

[29] N. Pugno, M. Ciavarellab, P. Cornettia, and A. Carpinteri. A generalized Paris' law for fatigue crack growth. *Journal of the Mechanics and Physics of Solids*, 54:1333–1349, 2006.

[30] Christian Herold, Jörg Franke, Riteshkumar Bhojani, Andre Schleicher, and Josef Lutz. Requirements in power cycling for precise lifetime estimation. *Microelectronics Reliability*, 58:82–89, 2016.

[31] C. Durand, M. Klingler, D. Coutellier, and H. Naceur. Power Cycling Reliability of Power Module: A Survey. *IEEE Transactions on Device and Materials Reliability*, 16:80–97, 2016.

[32] Yvan Avenas, Laurent Dupont, and Zoubir Khatir. Temperature Measurement of Power Semiconductor Devices by Thermo-Sensitive Electrical Parameters - A Review. *IEEE Transactions on Power Electronics*, 27:3081–3092, 2012.

[33] W. Martienssen and H. Warlimont, editors. *Springer Handbook of Condensed Matter and Materials Data*. Springer, 2005.

[34] G. Khatibia, M. Lederera, B. Weissa, T. Lichtb, J. Bernardic, and H. Danningerd. Accelerated Mechanical Fatigue Testing and Lifetime of Interconnects in Microelectronics. *ScienceDirect*, 2:511–519, 2010.

[35] Kristian Bonderup Pedersen amd Dennis A. Nielsen, Bernhard Czerny, Golta Khatibi, Francesco Iannuzzo, Vladimir N. Popok, and Kjeld Pedersen. Wire bond degradation under thermo- and pure mechanical loading. *Microelectronics Reliability*, 76-77:373–377, 2017.