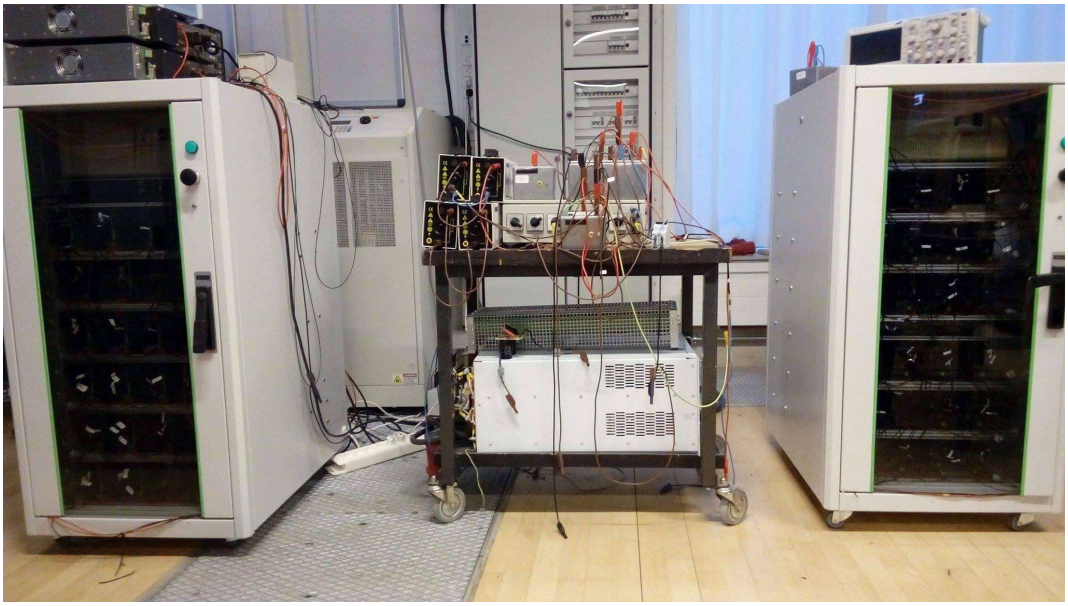
Analysis of the Back-to-Back MMC focusing on the DC-Link Voltage Ripple Reduction and Fault Conditions



Master Thesis

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STUDENT REPORT

Title:
Analysis of the Back-to-Back MMC focusing on the DC-Link Voltage Ripple Reduction and Fault Conditions

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Abstract:

This project intends to analyse the methods for voltage ripple reduction in the MMC in a back-to-back configuration. For that, a description of the main components of the MMC are presented with thorough details. The DC-Link ripple is evaluated and three different techniques to reduce it are proposed. The methods are : (a) Use of DC-Link capacitance, (b) Use of space-vector modulation technique and (c) Undermodulating the inverter. The results are verified using both theoretical calculations and simulation results. Moreover, the system is analysed under fault conditions: AC, DC and internal faults. The stress levels to which the system components will be subjected to during each unabated fault conditions are presented. The fault current paths during each fault conditions are presented. A strategy to protect the converter during these faults based on the converter design, AC breakers and distributed braking chopper solution are proposed.

By signing this document, each member of the group confirms that all participated in the project work and thereby all members are collectively liable for the content of the report.

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Preface

Analysis of the Back-to-Back MMC focusing on the DC-Link riple reduction and fault conditions is written as a part of the Master Thesis conducted at the department of Energy technology in Aalborg University by group EPSH 4-1032 and PED4-1040 during the period from 1st of February 2017 till 1st of June 2017.

The report has been written in Latex and the simulations are performed in PLECS. The references are documented in the bibliography and are cited in the thesis according to the IEEE citation standards. The variables used in the thesis are defined in the nomenclature.

0.1 Acknowledgement

The authors will like to express their deepest gratitude to their supervisors: Associate professor Sanjay K. Chaudhary, Prof. Remus Teodorescu and Lars Helle from Aalborg University for their guidance, motivation and profound knowledge. We are highly grateful to our supervisors for being available for us and imbibing in us the confidence and courage to complete the assigned tasks with the highest possible quality. We highly appreciate the willingness and patience of the supervisors for being available for regular meetings and providing valuable feedbacks. We would also like to thank our supervisors for the reviewing of the thesis and the submitted paper.

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Nomenclature

Table 1: Variables-1

Symbol	Description
v_d	DC-link voltage
m	Modulation Index
C_d	DC-link capacitor
W_{rated}	Rated Energy requirement for the MMC
$W_{ratedth}$	Rated Energy requirement for the MMC with THI
v_c	Internal voltage
v_u	Upper arm voltage
v_l	Lower arm voltage
i_s	Output current
i_c	Circulating current
v_{sth}	Output voltage with third-order harmonic injection
v_s	Output voltage
k_{max}	maximum allowable capacitor ripple
M	number of phases
V_s	Line-to-Line voltage
p	Active Power
Q	Reactive power
f_g	Grid frequency
$\widehat{V}_s$	Peak output voltage
$\widehat{I}_s$	Peak output current
ω_1	Instantaneous angular frequency
S_{base}	Base apparent power
V_{base}	Base output voltage
I_{base}	Base output current
$Vsub_{base}$	Base submodule arm voltage
$Iarm_{base}$	Base arm current

Table 2: Variables-2

Symbol	Description
V_{dbase}	Base DC-link voltage
I_{dbase}	Base DC-link current
$Wrec_{base}$	Base rated energy
$\overline{\nu_{cu,l}^{\Sigma}}$	Average sum capacitor voltage per arm
$V_{c,n}$	Average submodle capacitor voltage
W_{sub}	Nominal energy storage in each submodule
$v_{cu,l}^{i}$	Submodule voltage on each submodule
k_{dc}	Time average of the submodule energy
$W_{u,l}$	Total energy storage per arm
ΔW_{max}	Excess energy storage
W_{max}	Maximum energy storage
φ	Power angle
$\vec{s}$	Vector (optimization)
$\widehat{s}$	Normalized vector (optimization)
v_a	AC-bus voltage
L	Arm inductance
R	Parasitic arm resistance
$n_{u,l}^{i}$	Submodule insertion index
$v_{cu,l}^{i}$	Capacitor voltage in submodule i
C	Submodule capacitance
$v_s^{\star}$	Output voltage reference
$v_c^{\star}$	Internal voltage reference
W_{Δ}	Imbalance stored energy
W_{Σ}	Stored energy per phase
$W_{u,l}$	Stored energy per arm
$W_{\Sigma 0}$	Mean value of the stored energy
$W_{\Delta 0}$	Mean value of the energy stored imbalance
R_{SM}	Breaking Resistor of the chopper
P	Rated active power
R, Y *and* B	3 phases of AC power
Z_f	Fault impedance
I_L	Load current during single line to ground fault
Z^+	Positive sequence impedance
Z^-	Negative sequence impedance
Z^0	Zero sequence impedance
V_F	Fault Voltage
I_f	Fault current flowing through the fault path

Table 3: Variables-3

Symbol	Description
I_a^0	Zero sequence current
I_a^+	Positive sequence current
I_a^-	Negative sequence current
v_{cumax}	$1.1 \times (v_d/\mathrm{N})$
v_{dref}	DC-Link reference voltage (1 p.u.)
P_D	DC-side input power
P	Active Power Output
$V(t)$	Instantaneous voltage at time=t
V_R	Voltage across resistor
V_L	Voltage across inductor
V_C	Voltage across capacitor
s_1, s_2	roots of the quadratic equation
ω^0	Natural frequency
α	Damping Attenuation
A_1 *and* A_2	Boundary conditions
C_{eq}	Equivalent capacitance in the circuit
L_{eq}	Equivalent inductance in the circuit
ω	Resonant frequency
τ	Time constant
θ	Phase Angle
I_0	Original state of capacitor current
j	represents the three phases (a,b and c) of the MMC
$idcf$	DC Fault current
i_{dfrec}	DC fault current flowing from the rectifier into the DC-Link fault
i_{dfinv}	DC fault current flowing from the inverter into the DC-Link fault
i_{df}	DC fault current

Table 4: Acronyms

Symbol	Description
HVDC	High Voltage Direct Current
MMC	Modular Multilevel Converters
p.u.	per unit
AC	Alternating Current
DC	Direct Current
$\frac{d}{dt}$	First derivative
$\frac{d^2}{dt^2}$	Second derivative
VSC	Voltage Source Converter
Und	Undermodulation
sine	Sinusoidal
IGBT	Isolated gate bipolar transistor
KLV	Kirchhoff voltage law
SLG	Single Line to Ground Fault
DLG	Double Line to Ground Fault
TLG	Triple Line to Ground Fault
CLCC	Cell level chopper control
THI	Third-Harmonic Injection

Table 5: Control variables

Symbol	Description
α_f	Corner frequency of voltage filter
α_d	DC-bus voltage control loop bandwidth
$\alpha_i d$	Dc-bus voltage integrator bandwidth
K_p	Proportion Gain
α_c	PR controller bandwidth
α_h	Resonant bandwidth
$K_h = 2$	Resonant gain

Chapter 1

Introduction

The advent of electrical energy has unveiled the beginning of a new era in the history of the world. Electrical energy was earlier considered only for lighting applications, however the world soon started acknowledging its wide arsenal of abilities. The second industrial revolution set the use of electricity instead of steam as the main sources of energy in the industries. Since then the widespread use of electricity has been increasing the generation and transmission power ratings in order to satisfy the growing public demand.

The most recent technology for high power transmission and conversion is now aiming into the High Voltage Direct Current (HVDC) lines controlled by Modular Multilevel Converters (MMC).

1.1 Background

The year 2015 was a stellar year for the renewable energy industry, culminating into the milepost Paris Agreement in Decemeber 2015 [1]. At this Paris climate conference (COP21), the first ever universally binding global climate deal was adopted by 195 countries [2]. The EU has been spearheading the international efforts towards the global climate deal and had a major contribution in the success of the Paris conference [2]. The EU was the first major member to submit their intended contribution, in which they mentioned their goal to reduce emissions by 40% by 2030. The Paris Agreement believes that wind power will play a major role in the completely decarbonised electric supply before the year 2050 [3].As quoted in the Global Wind Energy Outlook 2015, until 2030 wind power could reach 2,111 GW and supply up to 20% of the global electricity. This will help to reduce CO_2 emissions by more than 3.3 billion tonnes per year [3]. Since the year 2001, there has been a consistent increase in the wind power production in the global market as can be seen from **Figure 1.1**. These statistics were released by the Global Wind

Energy Council (GWEC) in their Global Wind Statistics February 2017 edition. [4]

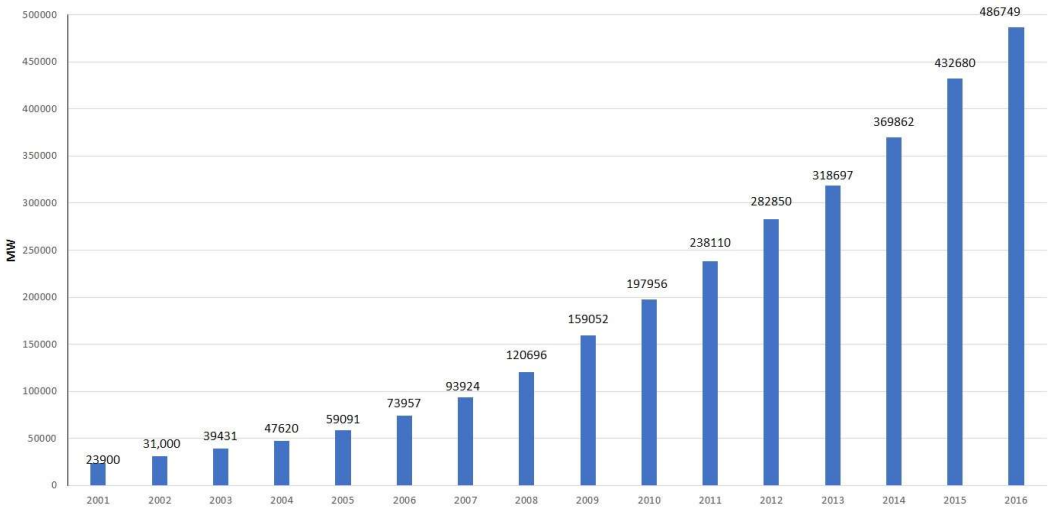
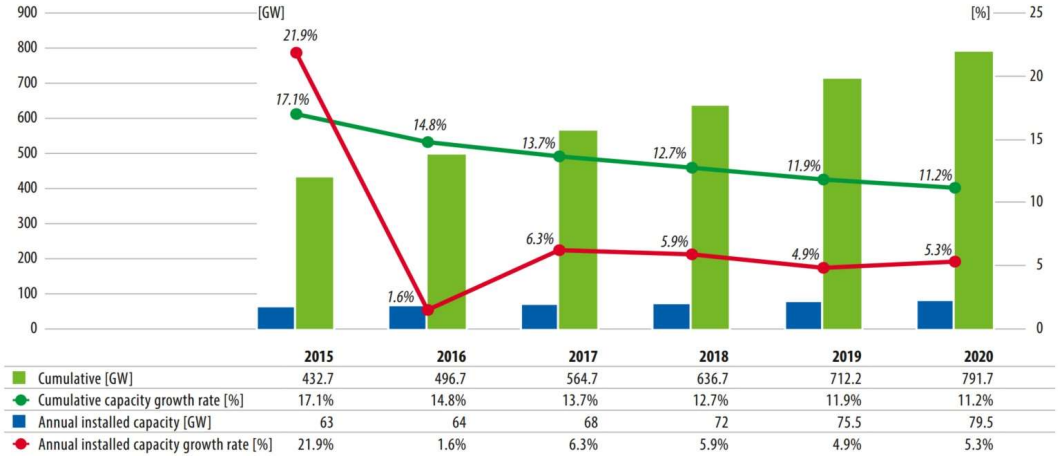


Figure 1.1: Global Cumulative Installed Wind Capacity 2001-2016 [5]

The long term targets adopted by 195 countries in the Paris convention to adopt a 100% emissions free power sector by 2050, means that the energy sector will be dominated by the renewable sources of energy in the near future. Among the renewable sources of energy, the wind and solar power will dominate due to lack of competition [1]. As per GEWC's Global wind Report on Annual Market update-2015, the prices of wind and Solar power have gone down, thereby creating better conditions for renewable energy to be competitive in the energy market. China, the leading producer of wind power based electricity [5] is lowering its Feed-in tariff(FIT) this year and will do it again in 2018, indicating that the wind power will have even better scope in the competitive energy market [1].

The market forecast for wind power also looks very promishing as can be seen from **Figure 1.2**. This figure shows the expected proliferation in the cumulative capacity of the global wind power energy in the upcoming years. The data is also corroborated by the emergence of new potential markets in Asia, Latin America, Eastern Europe and Africa.

Asia is the largest market for wind power industry with China leading and followed by India. The top ten cumulative wind power capacity until december 2015 can be seen from **Figure 1.3** [1]. Asia will continue to dominate the period from 2016 to 2020 capturing atleast 50% of the global market. [1] According to the American Wind Energy Association (AWEA), North America is also a potential market for wind power energy with over 20,000 MW of wind capacity under construction or in advanced development and more than 3,700 MW of new announcements



	2015	2016	2017	2018	2019	2020
Cumulative [GW]	432.7	496.7	564.7	636.7	712.2	791.7
Cumulative capacity growth rate [%]	17.1%	14.8%	13.7%	12.7%	11.9%	11.2%
Annual installed capacity [GW]	63	64	68	72	75.5	79.5
Annual installed capacity growth rate [%]	21.9%	1.6%	6.3%	5.9%	4.9%	5.3%

Figure 1.2: Global Wind Market Forecast For 2016-2020 [1]

made in the third quater of 2016. The leading contributors being Vestas and GE [6].

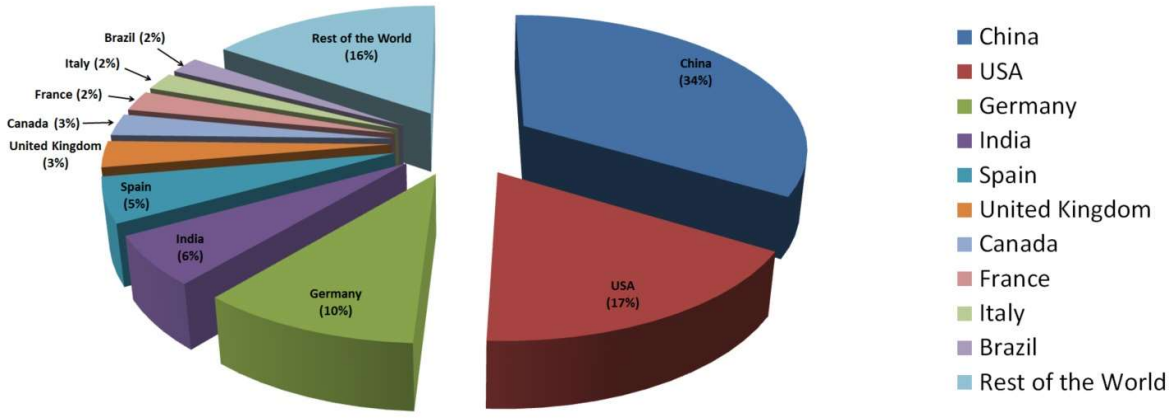


Figure 1.3: Cumulative Capacity as on Dec 2015 [1]

The European Union has been at the forefront in the efforts to integrate more renewable sources into its energy system. They have set a target of integrating atleast 27% of the renewables sources into their energy system by the year 2030 [7]. The European Wind Energy Association now known as Wind Europe, states that on-shore wind power is the cheapest way of energy production in Europe. Off-shore wind is also reducing its cost at a very quick pace. The European Union boasts that 3 out of the 5 largest turbine manufacturing companies in the world are European companies [8]. The Wind Europe Annual Report-2016, states that the

Wind Power is recently the 2^{nd} largest energy generating capacity. The increasing penetration of the wind power in the european energy market can be seen from figure **Figure 1.4**. In 2016, the renewable energy sources contributed to 86% of EU's power capacity. As can be seen from figure 1.5, wind power is the most dominant renewable sources of energy in Europe. Germany remains the country with the largest installed wind power capacity in the EU countries [8],[9].

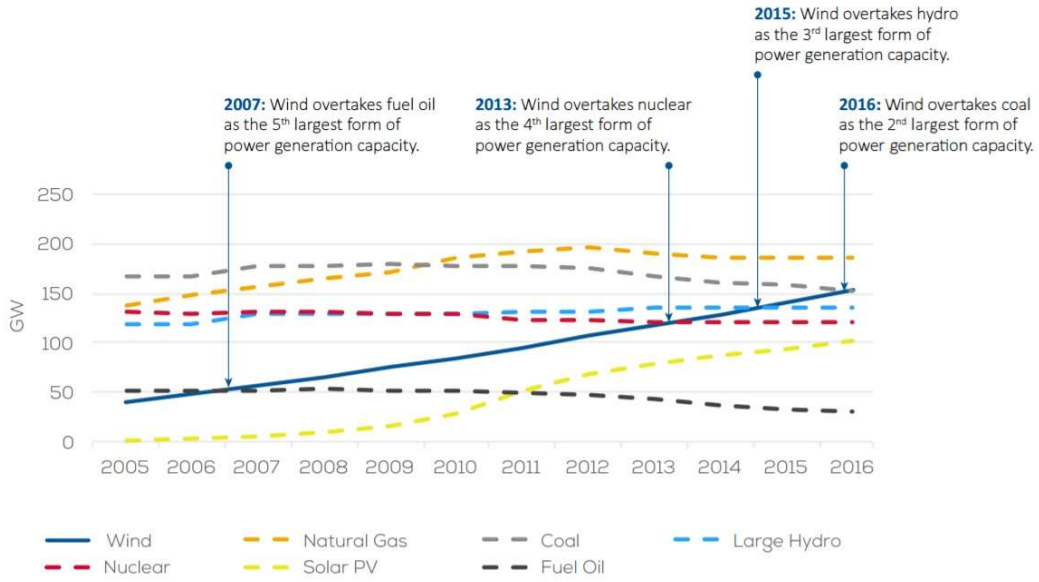


Figure 1.4: Cumulative Power Capacity in the European Union 2005-2016 [8]

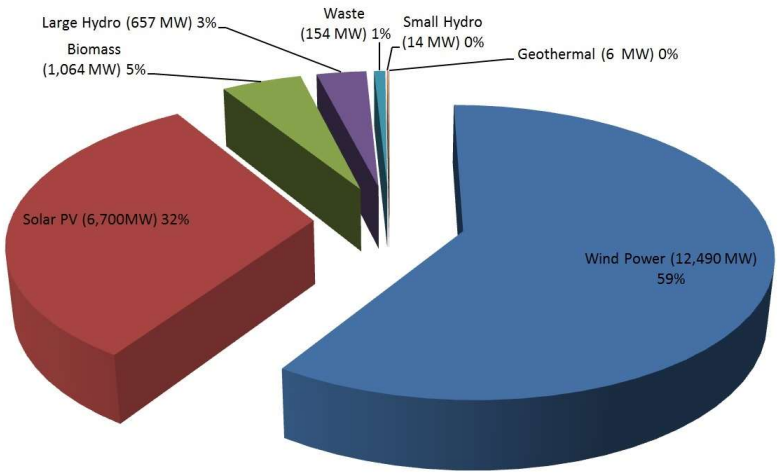


Figure 1.5: Share of EU's energy generation by renewable sources of energy in 2016 [9]

Denmark also has huge potential for wind power. 42% of Denmark's electricity was covered by wind energy in 2015. The danish government aims to get 50% of its electricity from wind energy by 2020 and 100% from renewable energy by 2050. Denmark has once again demonstrated the remarkable strength of its wind resource, producing 98 GWh of energy from wind turbines over a 24-hour period on February 22, 2017. This produced 104% of the country's energy demand [7]. However, Denmark's wind production record achievement was on July 10, 2015, when it produced 140% of the country's energy demand [7]. In 2016, Denmark has the highest wind penetration rate (37%) among all the EU member countries. It can be seen from figure 1.6 [9].

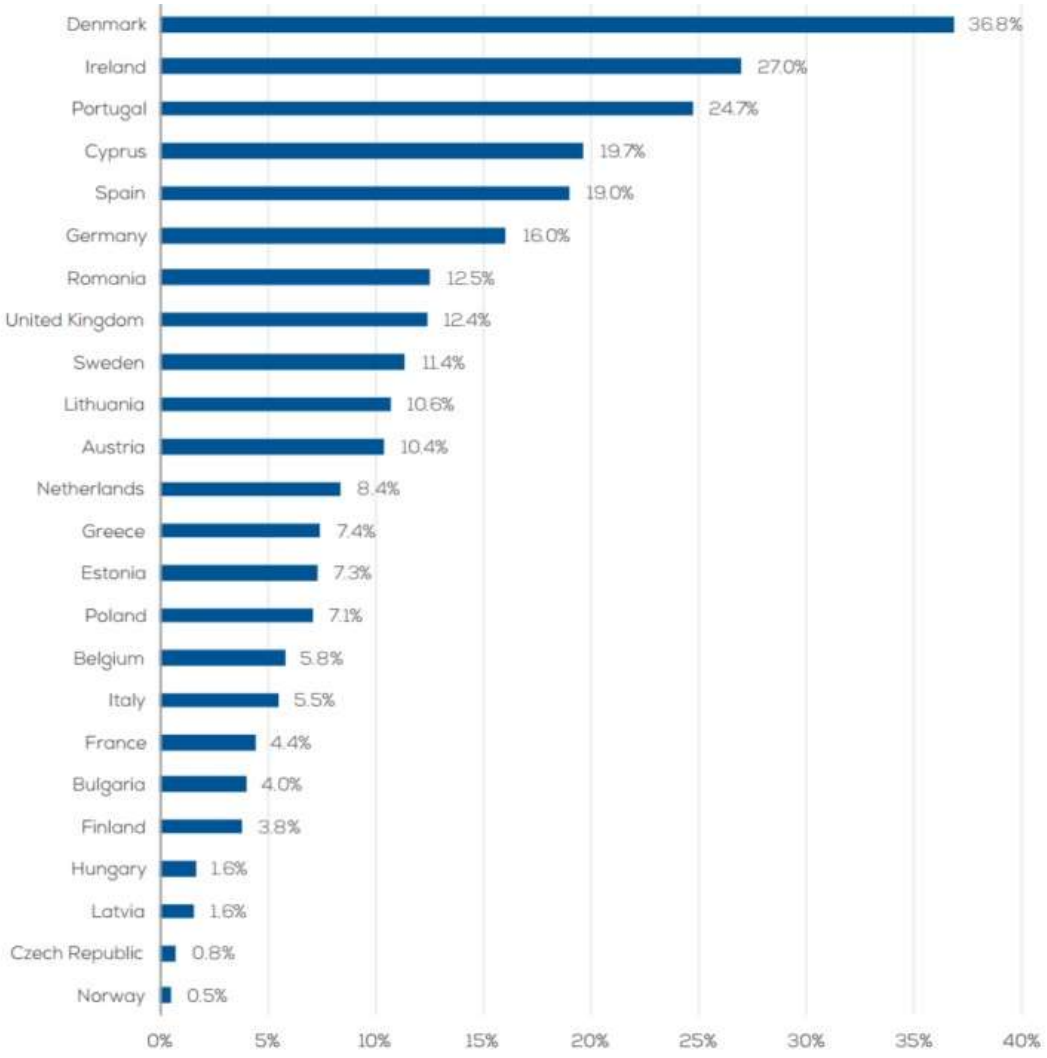


Figure 1.6: Wind penetration rates in European countries [9]

1.2 State of the Art

With the increasing demand in the wind power sector, the power ratings of the wind turbines are also increasing. Recently, on December 01, 2016, danish manufacturer MHI Vestas announced that its new 9 MW prototype in Osterild wind turbines test field has broken the long standing energy production record for a commercially available off-shore turbine by producing approximately 216 MWh within a 24 hour period [10], [11]. Also Siemens Wind Power is investing hugely in research and it has helped to manufacture their new 8 MW wind turbine for off-shore application. It is expected to enter service off the west coast of Denmark in spring 2017. High demand of wind power energy has lead to the escalation in the size of the wind turbines and now wind power industries are looking into medium/high voltage transmission to increase the efficiency. However, smaller transformer stations/ transformerless transmissions are preferred in order to reduce the space constraint in the nacelle. Thus the industries have started to resort to the technology of using Modular Multilevel Converters for medium to high voltage power transmissions. SVC Plus from Siemens, is a good example of the use of this latest technology in power transmissions[12].

1.2.1 Modular Multilevel Converter

The early multilevel converters used diode clamped converters [13] and flying capacitor converters [14]. They took advantage of the principle of a split dc-link, thereby making it capable of producing additional ac-voltage levels. However to increase the modularity and the scalability of the converters, a new type has been developed, known as the cascaded multilevel converter. These converters are based on a more modular approach where the converters are constituted of sub-modules or cells, that comprises of a capacitor and semiconductor devices that when added, increase the voltage capability.

Until the year of 2003, cascaded converters were not completely modular as they needed to incorporate other complementary features. Then [15] presented the MMC with half-bridge sub-module topology. It is comprised of strings of sub-modules/cells that allow for AC/DC conversion and at the same time improve the voltage scalability and harmonic performance. Another advantage of the MMC is the reduced operating frequency when compared to 2-level VSC counterpart, this translates into the reduction of power losses as well as diminishing in the temperature stress on the semiconductor devices. Thus shifting the converter constrain to the safe operation area (SOA). Due to its construction, MMC also presents an inherent redundancy, an ability that allows to increase the reliability of the system. [16]

1.2.1.1 Developments in MMC

MMCs with half bridge sub-module topology was first proposed in 2003 by Rainer Marquardt [15] and was first commercially implemented in the Trans Bay cable project in San Francisco[17][1]. This project by Siemens marked the first commercial use of MMC.
Since then, many research and development efforts have been done into the MMC technology. Improvement in its performance can be achieved by maintaining equal energy in both the arms in a leg. This can be implemented by controlling the switching of the sub-modules. For this reason, [18] and [19] mentions the use of PS-PWM technique to generate switching signals for the IGBTs in the sub-modules. They also discuss the reduction in the harmonics of the output voltage and the circulating current by changing the displacement angle. This displacement angle helps to adjust the phase shift between the carrier signals in the upper and lower arms.

The arm energy unbalance in the three legs causes the circulating current to flow within the MMC. The circulating current has no effect on the output voltage and current, but it has a detrimental effect on the system as it increases the RMS value of the arm current, thereby increasing the converter losses and power ratings of the semi-conductor devices. To reduce the circulating currents, [19] describes the use of cascaded PI and P controllers for average and balancing voltage control respectively for the half bridge sub-module configuration. In [20], the circulating currents flowing through the MMC phase legs are analyzed and then a circulating current controller is proposesd, which uses Park's Transformation to convert the three phase alternating circulating currents into two DC components. This is an advantage as PI controllers are better in tracking DC signals. This strategy helps to reduce the circulating current's amplitude to the fundamental component's amplitude from 35% to 1% [20].

The AC circulating current can also be suppressed without transforming them into DC components. In [21], the authors have used PS-PWM technique and Proportional Resonant (PR) control to eliminate the double frequency current component from the system. This controller increases the ability of the system to track the real and the reactive power reference. It also helps to effectively eliminate the second harmonic component of the arm current.

In [22], the energy stored in the sub-module capacitors due to the circulating currents flowing through them is observed. It also suggests a method to calculate the highest magnitude of the circulating current that can flow through the circuit

[1]This is a 85 km underwater cable from San Francisco until Pittsburg. It can transmit 400 MWs of power at a DC voltage of $\pm$200 kV.The system was operational in November 2010.

and thereby proposes the size of the arm inductor.

MMCs have found huge application due to its ability to harness power from off-shore and on-shore wind power plants. Off-shore wind turbines must be connected to the onshore power transmission systems. Earlier HVAC was used, but with the introduction of HVDC, the latter is more preferable. In [23], the working of a wind power plant with a back-to-back MMC based HVDC link is discussed. It states clearly the independence of the reactive and active power supply in the system. It considers also a L-G fault condition, to demonstrate the behaviour of the MMC during fault condition. In [24], the influence of the HVDC cable on the working of the MMC can be seen. An energy based control strategy has been proposed and it makes use of the concept of energy balance in the MMC. The control strategy also takes into consideration the effect of the DC bus cable.

The MMC sub-modules can have a full bridge topology as well. In [25], the paper describes the use of the full bridge sub-module configuration for MMC. They also propose the use of average and balancing voltage controllers. However, it proposes the use of an internal current controller as well that makes use of the damping coefficient. They also use the load angle compensation to control the output voltage in case of same frequency conversion.

With the passage of time, newer and more advanced technologies are emerging. One such technology is the hybrid MMC. In [26] the paper suggests the use of parallel hybrid MMC and proposed the injection of zero sequence voltage based predictive control strategy to control the power flow and thereby minimising the ripple in the dc current.

1.3 Main Objectives

The first objective of this thesis is to design a three-phase Back-to-Back MMC rated at 10MW, 6KV. The system will transfer energy from a generating station to a grid. Since, the focus of the project is the transfer of energy between the generating station and the grid, so the generating station is considered as a steady source. The thesis encompasses the following objectives:

- In-depth study and formulation of the mathematical modelling, operating principles and internal control of the MMC for back-2-back configuration.
- Analysis of the effect of DC-Link capacitance on the system under steady state conditions. Investigate different techniques to reduce/eliminate the DC-Link capacitor
- Analysis of the system performance during the AC, DC and internal faults.
- Investigation of protective measures to prevent the system from severe damages that can be caused by the faults.

- Investigation of the use of DC choppers to limit the sub-module capacitor voltages to pre-defined voltage limits.
- Submission of a paper based on fault analysis and preventive measures for the IECON 2017, IEEE conference.

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1.4 Limitations

The main objectives of this project is the implementation of DC-choppers and reducing the DC-Link capacitance, thereby providing steady state stable operation. The limitations of this project are as follows:

- The Master Thesis is for one semester, therefore the time available for the thesis is restricted to just 4 months.
- The evaluation of the simulated results could only be validated using theoretical results.
- The LVRT operations is not being considered in the project.

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1.5 Outline of thesis

The project is divided into 5 chapters. The chapters are briefly described as follows:

- Chapter 2, introduces the three phase MMC to explain the dynamic behaviour of the converter under normal operation condition. It states the controllers used in the project and describes in details the functionality of each controller.
- Chapter 3, describes the base values for the system parameters. Then the chapter explains the design of the MMC components:choice of the number of sub-modules, choice of the sub-modules capacitance , choice of the arm inductor and the energy contained in the MMC. The grid parameters are defined and a comparison between the strong grid and the weak grid is presented. The transfomer parameters are also defined in this chapter. The system behaviour under steady state condition is presented.
- Chapter 4, presents three different techniques to reduce the DC-Link ripples. A comparison among them is presented.

- Chapter 5, introduces the different types of faults that the power system can encounter. The faults comprises of AC faults: Single Line-to-Ground fault, Double Line-to-Ground fault and Triple Line-to-fault. Then it discusses the DC faults: Pole-to-Pole faults and Pole-to-fault. Then the effect of the internal faults in the system is discussed. Finally, protective measure are presented to prevent the severe damage on the system during faults.

Chapter 2

Dynamics and Control of MMC

This chapter discusses the fundamentals of the dynamics of the MMC. Furthermore, the principles of average model used in this project for simulation purpose are also covered. In the end of the chapter a detail description of the controllers used in the Back-to-Back MMC are presented.

2.1 MMC Fundamentals

A three phase schematic is shown in figure .The MMC can operate for any number of phases. However, in this project a three phase operation of MMC has been observed. The MMC comprises of sub-modules which help to split the dc link. These sub-modules are also known as cells. These cells are connected in series. The sub-modules can have different topologies: a) Half bridge topology and b) Full bridge topology.

A half bridge topology is capable of producing two states of output voltage : 0 or +V, where V is the voltage generated by the DC capacitor in the topology. Thus every valve acts as controllable and unipolar voltage cource. However, with full bridge topology, it is possible for converters to produce three states of voltage:0, +V and -V, thus providing a bipolar voltage source. Though, full bridge rectifiers have the benefit of providing bipolar voltage source but they also come with the disadvantage of using more IGBT's[27]. However, full bridge topology helps in suppressing the dc faults, unlike converters with half bridge topology[28]. However this project makes use of half bridge topology because it requires half the number of semi-conductors devices that are used by full bridge topology. Therefore rendering it to be cheaper and easier to control, when compared to the full bridge topology[27].

Each sub-modules with half-bridge topology contains a DC storage capacitor (C_{sm}), two controlled semiconductor devices, which are generally IGBTs and two anti-parallel diodes. As can be seen from the figure, it can be deduced that the switches should work complementary to each other in order to avoid short circuit of the capacitor. Each phase in a MMC is called a leg and each leg is comprised of 2 arms:upper and lower arms. Each arm consists of N number of sub-modules. As can be seen from figure, the upper arm is connected to the postive polarity and the lower arm is connected to the negative polarity of the DC bus. The AC side is connected with the grid through a galvanicly isolated transformer. This transformer helps to step up or step down the voltage level as per the voltage rating of the converter and the grid. This grounding of the neutral point of the star connected side of the transformer helps to isolate the zero sequence current from the circuit. Each arm also consists of an arm inductor. This inductor (L) acts like a low pass filter to attenuate the high frequency current component flowing through it.

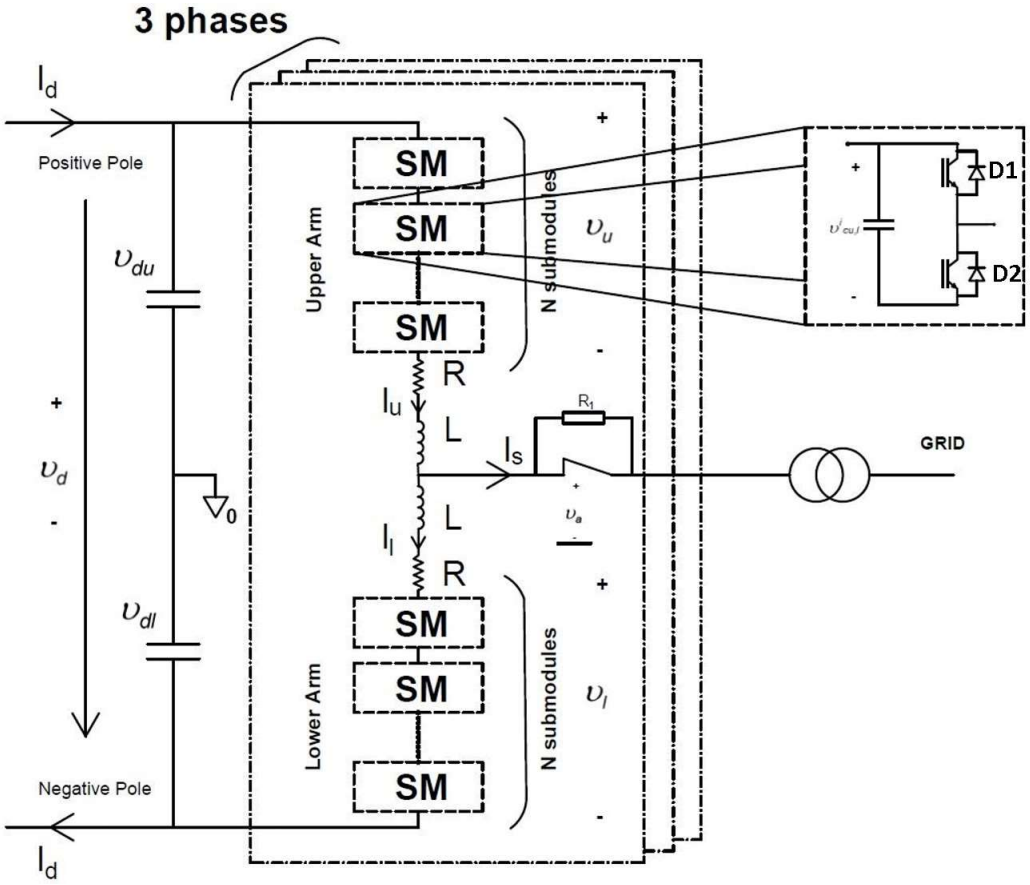

Figure 2.1: MMC circuit diagram

The mathematical modelling of the MMC gives a better understanding of the dynamic behaviour of the MMC [16]. As can be seen from **Figure 2.1**, the upper and lower arms are identically and share the DC bus voltage equally as can be seen from **Equation (2.1)**.

$$v_{cu,l}^{\Sigma} = \frac{v_d}{2} \tag{2.1}$$

The output currents $i_{s\phi}$ are the ac-side phase currents driven by the inner electromotive force (EMF) $v_{s\phi}$ of each leg. Similar the circulating currents $i_{c\phi}$ are the average currents of each phase leg, driven by the voltage $v_{c\phi}$. These quantities are represented as:

$$i_{s\phi} = i_{u\phi} - i_{l\phi} \qquad and \qquad i_{c\phi} = \frac{i_{u\phi} + i_{l\phi}}{2} \tag{2.2}$$

$$v_{s\phi} = \frac{v_{l\phi} - v_{u\phi}}{2} \qquad and \qquad v_{c\phi} = \frac{v_{l\phi} + v_{u\phi}}{2} \tag{2.3}$$

As can be seen from the figure , the lower and upper arm current can be defined in terms of the output sinusoidal current and circulating current as:

$$i_u = \frac{i_s}{2} + i_c \qquad and \qquad i_l = -\frac{i_s}{2} + i_c \tag{2.4}$$

Under balance AC-side conditions a single MMC is generally considered to have a dc component in the arm current of:

$$\overline{i_u} = \overline{i_l} = \overline{i_c} = \frac{i_{dc}}{3} \tag{2.5}$$

The same is desired for the circulating current ensuring an operation with the converter losses and the rms arm currents at a minimum.

In **Figure 2.1** a simplified diagram corresponding to the upper and lower arm current paths of the MMC for an arbitrary phase leg is presented. Applying the Kirchhoff voltage Law (KVL) to both the arms the dynamic relation of the currents are obtained as:

$$\frac{v_d}{2} - v_{u\phi} - Ri_{u\phi} - L\frac{di_{u\phi}}{dt} - v_a = 0 \tag{2.6}$$

$$-\frac{v_d}{2} + v_{l\phi} + Ri_{l\phi} + L\frac{di_{l\phi}}{dt} - v_a = 0 \tag{2.7}$$

From the previous equations, respectively adding and subtracting **Equation (2.5)** to **Equation (2.6)** and including the relations presented in **Equation (2.3)** and **Equation (2.4)**, yields:

$$\frac{L}{2}\frac{di_s}{dt} = v_s - v_a - \frac{R}{2}i_s \tag{2.8}$$

$$L\frac{di_c}{dt} = \frac{V_d}{2} - v_c - Ri_c \tag{2.9}$$

From these relations is now possible to understand the role of v_s and v_c in driving i_s and i_c respectively. Furthermore, for i_c to be a completely dc signal it should be controlled as:

$$v_c = \frac{v_d}{2} - Ri_c \approx \frac{v_d}{2} \tag{2.10}$$

2.2 Average Model

The MMC operation accounts for many semiconductor devices, mainly IGBTs, that are used in the system switching process. Simulating these dynamics is a rather slow and tedious process as a reduced time step is needed. In order to overcome this drawbacks a solution employing an average model can be employed and so reducing the simulation time at the expense of accuracy.

Considering the sub-modules to be inserted $n^i_{u,l}$=1 or bypassed $n^i_{u,l}$=0 the arm voltage can be expressed in terms of the insertion indices as:

$$v_{u,l} = \sum_{i=1}^{N} n^i_{u,l} v^i_{cu,l} \tag{2.11}$$

Furthermore, from **Figure 2.1** the arm voltage are consider to be equal, which is further ensured by the arm balancing control **Section 2.5.4**, and so the upper and lower arm voltage can be approximated as:

$$v_{u,l} = \sum_{i=1}^{N} n^i_{u,l} v^i_{u,l} \approx \sum_{i=1}^{N} n^i_{u,l} \frac{v^{\Sigma}_{cu,l}}{N} = \frac{v^{\Sigma}_{cu,l}}{N} \sum_{i=1}^{N} n^i_{u,l} \tag{2.12}$$

Introducing to the last equation the concept of the per-arm insertion indices, the arm voltages can be finally approximated as:

$$v_{u,l} = n_{u,l} v^{\Sigma}_{cu,l} \tag{2.13}$$

v_s and v_c can now be represented in an average way, combining **Equation (2.23)** and **Equation (2.13)**:

$$v_s = \frac{-n_u v^{\Sigma}_{cu} + n_l v^{\Sigma}_{cl}}{2} \qquad v_c = \frac{n_u v^{\Sigma}_{cu} + n_l v^{\Sigma}_{cl}}{2} \tag{2.14}$$

The dynamic relation of the currents expressed in a average basis can be obtained substituting in **Equation (2.6)** and **Equation (2.7)** the expression of v_s and v_c from **Equation (2.14)** yielding:

$$\frac{L}{2}\frac{di_s}{dt} = \frac{-n_u v_{cu}^{\Sigma} + n_l v_{cl}^{\Sigma}}{2} - v_a - \frac{R}{2}i_s \qquad L\frac{di_c}{dt} = \frac{v_d}{2} - \frac{n_u v_{cu}^{\Sigma} + n_l v_{cl}^{\Sigma}}{2} - Ri_c \quad (2.15)$$

The average principle can be further extended to the capacitor voltages. Considering the capacitor derivative equation, each capacitor voltage is expressed as:

$$C\frac{dv_{cu,l}^{i}}{dt} = n_{u,l}^{i} i_{u,l} \qquad i = 1, 2, ..., N. \quad (2.16)$$

In an arm with N capacitors:

$$\frac{C}{N}\frac{dv_{cu,l}^{\Sigma}}{dt} = n_{u,l} i_{u,l} \quad (2.17)$$

Expressing i_s and i_c according to the relation in 2.4:

$$\frac{C}{N}\frac{dv_{cu}^{\Sigma}}{dt} = n_u\left(\frac{i_s}{2} + i_c\right) \qquad \frac{C}{N}\frac{dv_{cl}^{\Sigma}}{dt} = n_l\left(\frac{i_s}{2} + i_c\right) \quad (2.18)$$

Summarizing, the dynamic behaviour of the MMC considering and average approach can be expressed with **Equation (2.18)** and **Equation (2.15)** for four state variables i_s, i_c, v_{cu}^{Σ} and v_{cl}^{Σ}.
The average principle is also useful for controller design. This is accomplished by an appropriated selection of the insertion indices. Normally, a reference of $v_s^{\star}$ and $v_c^{\star}$ respectively the output and internal voltages is available. After that by respectively adding and subtracting the two relations from **Equation (2.14)** and including the ideal insertion indices, yields:

$$n_u = \frac{v_c^{\star} - v_s^{\star}}{v_c^{\Sigma} u} \qquad n_l = \frac{v_c^{\star} + v_s^{\star}}{v_c^{\Sigma} l} \quad (2.19)$$

2.3 Capacitor Voltage Ripple

The submodule capacitor is one of the biggest constrain in the MMC system. Being fundamental for the energy conversion process, it is also one of the most costly components and one of the least reliable. For the design of the capacitor it accounts the mean voltage values as well the resultant ripple. In order to maintain it at a minimum value as possible the acceptable ripple is often consider not to surpass 10% of the mean sum capacitor voltage.
In order to proper infer the submodules capacitor ripple the derived average model

can be use. For that, substituting **Equation (2.19)** in **Equation (2.18)** and then multiply both sides of the equations by v_{cu}^{Σ} and v_{cl}^{Σ} yields:

$$\frac{C}{2N}\frac{d(v_c^{\Sigma}u)^2}{dt} = (v_c^{\star} - v_s^{\star})\left(\frac{i_s}{2} + i_c\right) \quad \frac{C}{2N}\frac{d(v_c^{\Sigma}u)^2}{dt} = (v_c^{\star} - v_s^{\star})\left(-\frac{i_s}{2} + i_c\right) \tag{2.20}$$

The first side of the equation is the arm energy, represented in the general form as:

$$W_{u,l} = \frac{C(v_{cu,l}^{\Sigma})^2}{2N} \tag{2.21}$$

For calculating the ripple, the concept of per-phase $W_{\Sigma} = W_u + W_l$ and imbalance $W_{\Delta} = W_u - W_l$ energy can be introduced. By adding and subtracting the two relations in **Equation (2.20)** the following is obtain:

$$\frac{dW_{\Sigma}}{dt} = 2v_c^{\star}i_c - v_s^{\star}i_s \qquad \frac{dW_{\Delta}}{dt} = v_c^{\star}i_s - 2v_s^{\star}i_c \tag{2.22}$$

In order to quantify this relations lets assume:

- $v_c^{\star}$=$\frac{v_d}{2}$
- $v_s^{\star}$=$\widehat{V}_s \cos\omega_1 t$
- i_s=$\widehat{I}_s \cos(\omega_1 t - \varphi)$
- i_c=pure dc

Substituting on **Equation (2.22)** the previous assumptions, yields:

$$\frac{W_{\Sigma}}{dt} = v_d i_c - \frac{\widehat{V}_s\widehat{I}_s}{2}\cos\varphi - \frac{\widehat{V}_s\widehat{I}_s}{2}\cos(2\omega_1 t - \varphi) \tag{2.23}$$

$$\frac{W_{\Delta}}{dt} = \frac{v_d\widehat{I}_s}{2}\cos(\omega_1 t - \varphi) - 2\widehat{V}_s i_c \cos_1 t \tag{2.24}$$

Integrating this previous equations:

$$W_{\Sigma} = W_{\Sigma 0} - \frac{\widehat{V}_s\widehat{I}_s}{4\omega_1}\sin(2\omega_1 t - \varphi) \tag{2.25}$$

$$W_{\Delta} = W_{\Delta 0} + \frac{v_d\widehat{I}_s}{2\omega_1}\sin(\omega_1 t - \varphi) - \frac{2\widehat{V}_s i_c}{\omega_1}\sin\omega_1 t \tag{2.26}$$

From this last equations is possible to infer that the $W_{\Sigma 0}$ and $W_{\Delta 0}$ are the mean energy values while the other components of the equations refer to the energy ripple. Moreover, the total energy ripple consists of two components: one of fundamental frequency coming from $W_{\Delta 0}$ and other of twice the fundamental frequency from $W_{\Sigma 0}$.

2.4 DC-BUS Dynamics

As mentioned in **Equation (2.5)** the arm currents should add up to the dc-bus current in steady state. This phenomenon may lead to ac-components and ripple to be present in the Dc-bus, which usually is intended to be constant. The relation between the Dc-bus capacitor C_d and the arm current of all phases is translated by:

$$2C_d \frac{dv_{du,l}}{dt} = i_d - \sum_{k=1}^{M} i_{u,l}^k \tag{2.27}$$

For a better understanding of the concept the pole-to-pole dc-bus voltage $v_d = v_{du} + v_{dl}$ and imbalance $v_d^\Delta = v_{du} - v_{dl}$ are again presented. By respectively adding and subtracting the two relation on **Equation (2.27)** for the upper and lower arms and using **Equation (2.4)** the following is obtained:

$$C_d \frac{dv_d}{dt} = i_d - \sum_{k=1}^{M} i_c^k \qquad\qquad C_d \frac{dv_d^\Delta}{dt} = \frac{1}{2} i_d - \sum_{k=1}^{M} i_s^k \tag{2.28}$$

From the first relation in **Equation (2.28)** it is observed that if i_c can be controlled to an almost constant value, v_d can maintain a almost constant pole-to-pole voltage. This when compared to a two-level VSC is seen as an advantage, as no pulsations with twice the fundamental frequency appear on the dc bus. From the second relation in **Equation (2.28)** it is possible to observe that as long as the phase output current add to zero no unbalance appears on the dc bus voltage. This allows the assumption that $v_d^\Delta = 0$ and so:

$$v_{du} = -v_{dl} = \frac{v_d}{2} \tag{2.29}$$

Considering the first equation in **Equation (2.28)** it is possible to observe the effect of the circulating current in the dc-bus dynamics. This circulating current guarantees the transfer of energy between the sub-modules capacitance and the dc-link, represented by:

$$\frac{C}{N} \frac{d(v_{cu}^\Sigma + v_{cl}^\Sigma)}{dt} = n_u \left(\frac{i_s}{2} + i_c \right) + n_l \left(-\frac{i_s}{2} + i_c \right) \tag{2.30}$$

Introducing the simplification $v_c^\Sigma = v_{cu}^\Sigma + v_{cl}^\Sigma$ and also through **Equation (2.19)**, yields:

$$\frac{C}{N} \frac{dv_c^\Sigma}{dt} = -\frac{v_s^\star i_s}{v_d} + i_c \tag{2.31}$$

Averaging **Equation (2.31)** and assuming i_c to be pure dc, is obtained:

$$\frac{C}{N} \frac{dv_c^\Sigma}{dt} = -\frac{\overline{v_s^\star i_s}}{v_d} + i_c \tag{2.32}$$

Since it is considered that the dynamics of this control is much faster than the evolve of v_d the substitution $v_c^{\Sigma} \longrightarrow 2v_d$ can be performed:

$$\frac{2C}{N}\frac{dv_c}{dt} = -\frac{P}{Mv_d} + i_c \tag{2.33}$$

Going back to **Equation (2.28)**, assuming balance phase legs $\sum_{M}^{k=1} i_c^k = Mi_c$ resulting in:

$$C_d\frac{dv_d}{dt} = i_d - Mi_c \tag{2.34}$$

Eliminating i_c in **Equation (2.33)** and **Equation (2.34)** results in:

$$\left(C_d + \frac{2MC}{N}\right)\frac{v_d}{dt} = i_d - \frac{P}{v_d} \tag{2.35}$$

This last equation demonstrates the contribution of the dc-bus capacitance and also the submodules capacitance into the dc-bus dynamics.

2.5 Control of MMC

The general control of an MMC can be observed on figure:

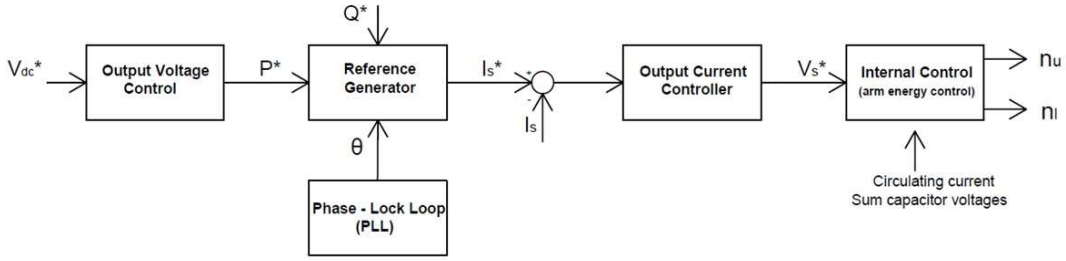

Figure 2.2: Standart MMC control scheme

The control is basically divided into five blocks:

- *Output Voltage Control*: Has the objective of controlling the Dc-bus voltage outputting a current reference. This controller is only present in rectifier mode, otherwise a single active power reference is presented.
- *Reference Generator*: Has the objective of transforming the power references into an output current reference. This block is associated with a dq to alfa-beta referential and so the need of PLL.
- *Phase Lock Loop (PLL)*: Use to track the grid angle and the amplitude of the positive and negative sequences.
- *Output Current Controller*:Converts the output current reference originated from the reference generator block into a voltage output reference.
- *Internal Control*:The internal control has the objective of transforming the output of the current controller into the insertion indices of each arm. This also includes a control of the circulating current and of the sum capacitor voltages.

2.5.1 Output Voltage Control

For regulating the DC-bus voltage **Equation (2.35)** can be utilize. As mentioned before this equations reflects the dc-bus dynamics considering both the dc-bus capacitance and also the sub-modules capacitances:

$$\left(C_d + \frac{2MC}{N}\right)\frac{v_d}{dt} = i_d - \frac{P}{v_d} \tag{2.36}$$

Now, multiplying both sides of the equations by v_d and also considering $C_d^{'}$=C_d + C, yields:

$$C_d^{'} v_d \frac{dv_d}{dt} = v_d i_d - P \Longrightarrow \frac{C_d^{'}}{2}\frac{dv_d^2}{dt} - P \tag{2.37}$$

Introducing the dc-bus energy: $W_d = \frac{C_d^{'} v_d^2}{2}$ and $P_d = v_d i_d$, yields:

$$\frac{dW_d}{dt} = P_d - P \tag{2.38}$$

Considering now that the controller is fast enough to track the reference, the PI controller is expressed as:

$$P^{\star} = \alpha_d (W_d - W_d^{\star})\left(1 + \frac{\alpha_{id}}{s}\right) \tag{2.39}$$

For the selection of α_d and $\alpha_i d$ they were made considering:

$$\alpha_i d < \frac{\alpha_d}{2} \tag{2.40}$$

$$\alpha_d < \omega_1 \tag{2.41}$$

A block diagram of the output voltage controller can be observed on figure 2.8. Besides the aforementioned described elements, others may be needed to secure the correct control:

- $H_p(s)$ filter presented on the v_d path is used to suppress the ripple and high frequency disturbances.
- $|V_a^F|$ Due to the PLL synchronization $v_a = |v_a|$. Moreover, the PLL filters the multiple frequency components which also makes possible $|v_a|$=$|v_a^F|$
- An anti-windup feedback of the error is necessary

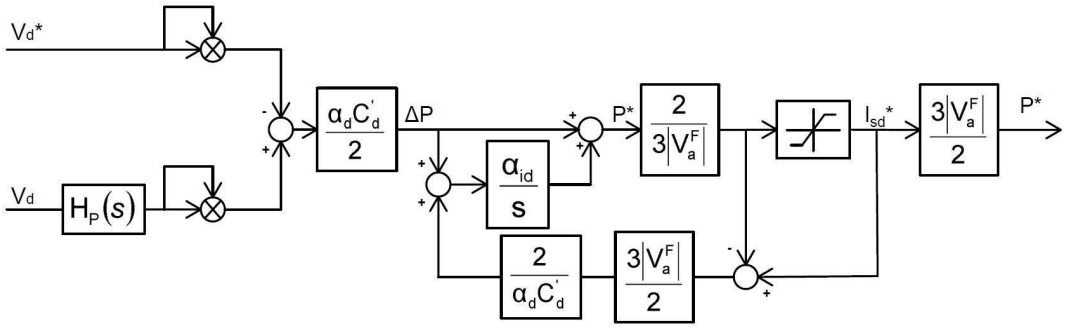

Figure 2.3: Output voltage controller

2.5.2 Reference Generator

The reference generator creates the current references from active and reactive power references. This is possible by equation which directly relates the d-axis current with active power and q-axis current with reactive power:

$$i_s^\star d = \frac{2}{3|V_a^F|}P^\star \qquad i_s^\star d = -\frac{2}{3|V_a^F|}Q^\star \tag{2.42}$$

This dq current references are then transform in an alfa-beta reference frame in synchrony with the grid angle, which is ensure by the PLL block. Figure 2.4 presents the block diagram illustrating the reference generator. It is possible to observe three different possibilities for this controller: "PSI-default", "PSI-LVRT" and "MSI-LVRT". This first is used when the MMC is operating under normal conditions while the other two when a fault occurs. Under this last assumption the system can inject positive or both positive and negative sequence current and so allowing for Low Voltage Ride Through (LVRT).

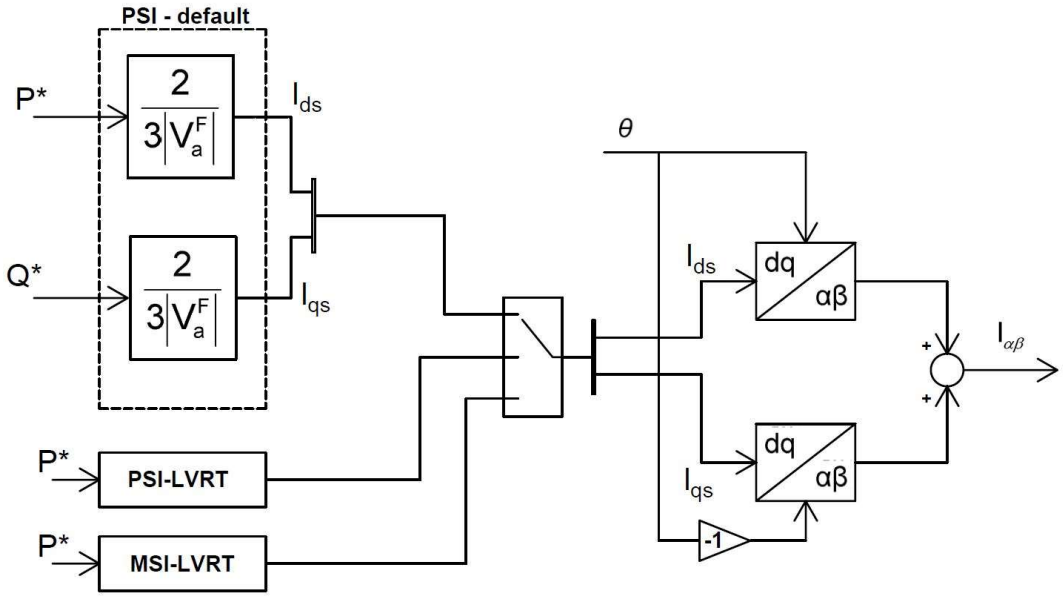

Figure 2.4: Reference Generator

2.5.3 Output Current Control

2.5.3.1 Limitations of PI controllers

Proportional-Integral controllers have found huge application , when it is desirable to track a constant signal. This can be observed by analysing the behaviour of the PI controller with the current through the inductor, being the control parameter. In this case, the internal resistance and control time are considered negligible. The PI controller takes the inductor current as input and generates the reference voltage v as output, which is the voltage applied across the inductor. i^* represents the reference current and i represents the actual current flowing through the inductor.

The schematic of this PI controller can be seen from **Figure 2.5**

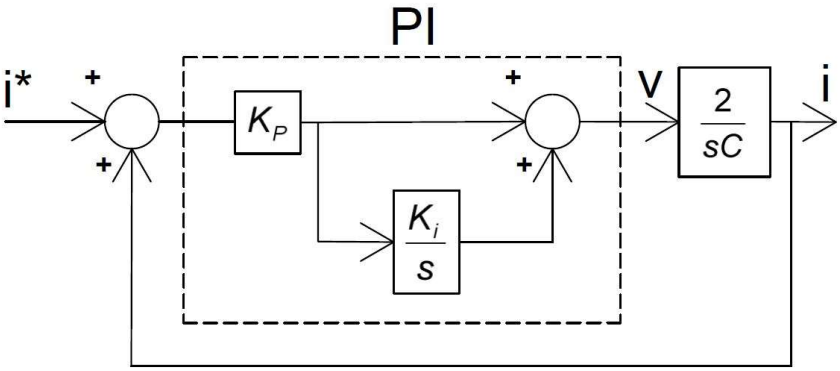

Figure 2.5: PI controller to control the current i through an inductor

The closed loop transfer function can be represented by:

$$G_c(s) = \frac{K_p s + K_i}{s^2 L + K_p s + ki} \tag{2.43}$$

From **Equation (2.43)**, it can be deduced that for zero static error, the value of $|G_c|$ should be equal to 1. It is only under this circumstance, that i will be able to follow i^*, i.e. i=i^*. In frequency domain 's' is replaced by '$j\omega$'. **Equation (2.43)** can be rewritten in the frequency domain as can be seen from **Equation (2.44)**.

$$G_c(j\omega) = \frac{K_i + j\omega K_p}{k_i + j\omega k_p - \omega^2 L} \tag{2.44}$$

Now, it can be clearly seen that only when ω is 0, then $|G_c(j\omega)|$=1. Thus it can be concluded that the PI controller cannot track a sinusoidal signal without steady state errors because for a sinusoidal signal $\omega \neq 0$ and thus $|G_c(j\omega)| \neq 1$ and arg$G_c|(j\omega)| \neq 0$.

This led to the development of PR controllers.

2.5.3.2 Resonant Controllers

In a PR controller, the 'P' acts like the proportional controller and 'R' behaves like the band pass filter about the angular frequency $h\omega$. The transfer function of the resonant controller can be represented by **Equation (2.45)**.

$$H_h(s) = \frac{K_h(scos\phi_h - h\omega_1 sin\phi_h)}{s^2 + \alpha_h s + (h\omega_1)^2} \tag{2.45}$$

where subscriptth represents the harmonic i.e. the multiples of the fundamental frequency, k_h is the gain, α_h is the bandwidth and ϕ_h is the compensation angle.The

resonant filter works like a band pass filter about the angular frequency $h\omega_1$. In order to observe the ability of the resonant controller to be able to follow sinusoidal signals, 's' is replaced by 'jω' in **Equation (2.45)** to obtain **Equation (2.46)**.

$$H_h(j\omega_1) = \frac{K_h(jh\omega_1 cos\phi_h - h\omega_1 sin\phi_h}{(jh\omega_1)^2 + \alpha_h jh\omega_1 + (h\omega_1)^2} = \frac{K_h(\cos\phi_h + j\sin\phi_h)}{\alpha_h} = \frac{K_h e^{j\alpha_h}}{\alpha_h} \tag{2.46}$$

Now, if $K_h = \alpha_h$ and $\alpha_h = 0$, then $H_h(jhw_1) = 1$ at a frequency of hw_1 is presented without amplitude or phase shift.

Other characteristics of resonant filters are:

- Considering h=0, **Equation (2.45)** is simplified to a low-pass filter

$$H_0 = \frac{K_0 \cos\phi_0}{s + \alpha_0} \tag{2.47}$$

  Where $K_0 = \alpha_0$ and $\phi_0 = 0$ yields a static gain $H_0(0) = 1$.

- Considering Zero bandwidth, $\alpha_h = 0$

$$H_h(s) = \frac{K_h(scos\phi_h - h\omega_1 sin\phi_h)}{s^2 + \alpha_h s + (h\omega_1)^2} \tag{2.48}$$

  A zero bandwidth resonant filter is considered the resonant part of a PR controller. This type of filter has infinite gain for $s = jh\omega_1$, while and integrator has infinite gain of s=0.

2.5.3.3 Output Current Controller Design

In **Figure 2.6** it is observed the complete structure of the implemented output current controller. It comprises of a PR controller, which acts on the difference between the reference and measured values of the output current. This controller also comprises of a saturation block to limit v_s^{*0} and an anti-windup. The last part of the controller is a SIN/SV block which allows for the output voltage to be referenced in a sinusoidal or spacevector modulation. This feature is later investigated in chapter 4.

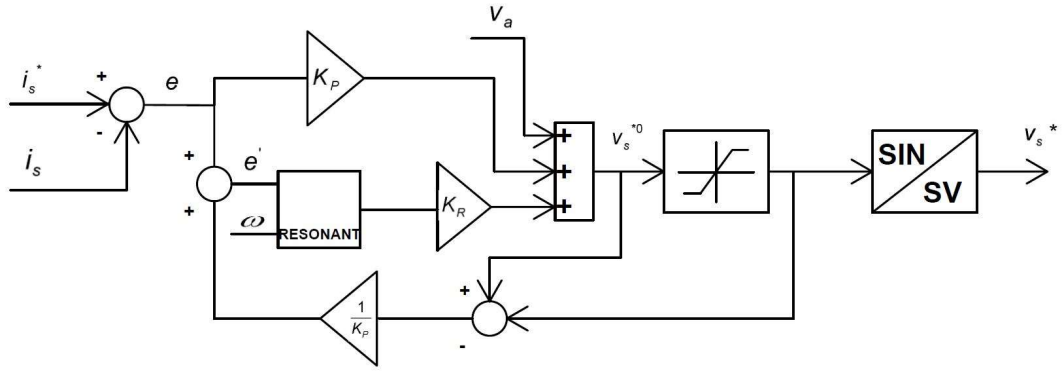

Figure 2.6: PI controller to control the current i through an inductor

The resonant part in **Figure 2.6** can be seen in detail in **Figure ??**.

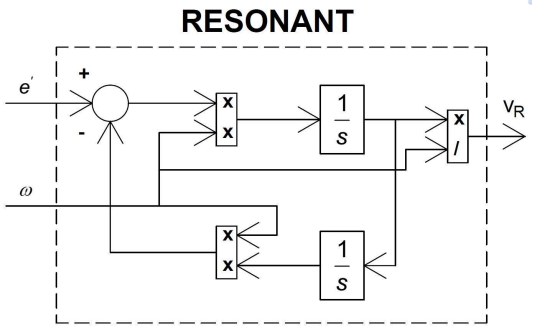

Figure 2.7: PI controller to control the current i through an inductor

The resonant part is based on **Equation (2.45)** considering zero bandwidth $\alpha_h = 0$, also with no phase shift $\phi_h = 0$. This is also known as a second-order generalized integrator (SOGI).

2.5.4 Arm balancing (Internal control)

The arm balancing/ internal comprised of a voltage control and a circulating current controller. It has the objective of balancing the arms of the MMC. This is accomplished by controlling i_c ideally to $P/(Mv_d)$ and the sum capacitor voltages to v_d.

2.5.4.1 Voltage Control

The voltage control is the mechanism, that through the selection of the insertion index, ensures the sum capacitor voltages to equal a common mean value of v_d.
There are four different types of voltage control methods: Direct voltage control, closed-loop voltage control, open-loop voltage control and Hybrid voltage control

all with their pros and cons but with common final result.
In this project the direct voltage control is preferred figure 2.8. Substituting in the denominator of equation 2.19 by v_d, yields:

$$n_u = \frac{v_c^\star - v_s^\star}{v_d} \qquad n_l = \frac{v_c^\star + v_s^\star}{v_d} \tag{2.49}$$

The direct voltage control is characterized by an asymptomatically stable system with presence of parasitic components, which can be suppressed by a proper circulating current control [16].

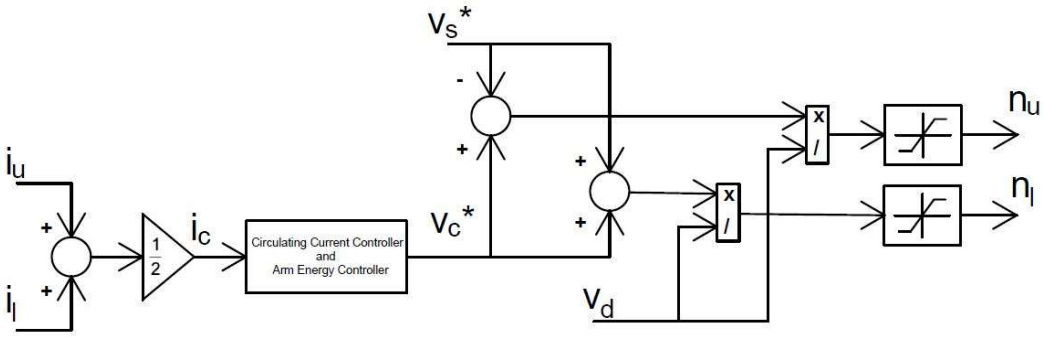

Figure 2.8: Voltage control

2.5.4.2 Circulating Current Control

As previously mentioned the circulating current controller is the second part of the arm balancing control. This controller congregates the arm energy controller and output a v_c reference which is then forward to the voltage control as can be seen in **Figure 2.9**.

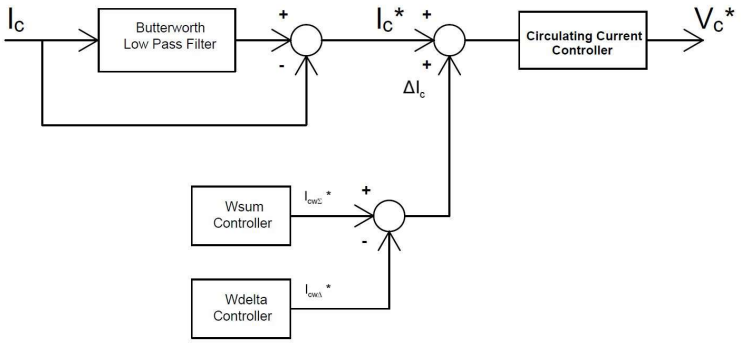

Figure 2.9: Complete block of the circulating current controller

The circulating current dynamics are expressed by **Equation (2.9)** as:

$$L\frac{di_c}{dt} = \frac{V_d}{2} - v_c - Ri_c \Longrightarrow i_c = \frac{1}{sL+R}\left(\frac{v_d}{2} - v_c\right) \tag{2.50}$$

The circulating current controller is comprised of a PR controller, which converts an error, $(i_c^\star - i_c)$ to produce $v_c^\star$. Also, a term $v_d/2 - Ri_c^\star$ is added to compensate for the resistive voltage drop. This yields the following control law.

$$v_c^\star = \frac{v_d}{2} - Ri_c^\star - R_a\left(1 + \frac{s}{s^2+\omega_1^2}\right)(i_c^\star - i_c) \tag{2.51}$$

Where $s/s^2 + \omega_1^2$ is the resonant part included both for 50Hz and 100Hz components. The reason for this the PR controller to be tuned for this two frequencies is observed in **Equation (2.23)** and **Equation (2.24)**. To this control law an integrative term is also added to eliminate any steady state error. This controller has the final structure presented in **Figure 2.10**:

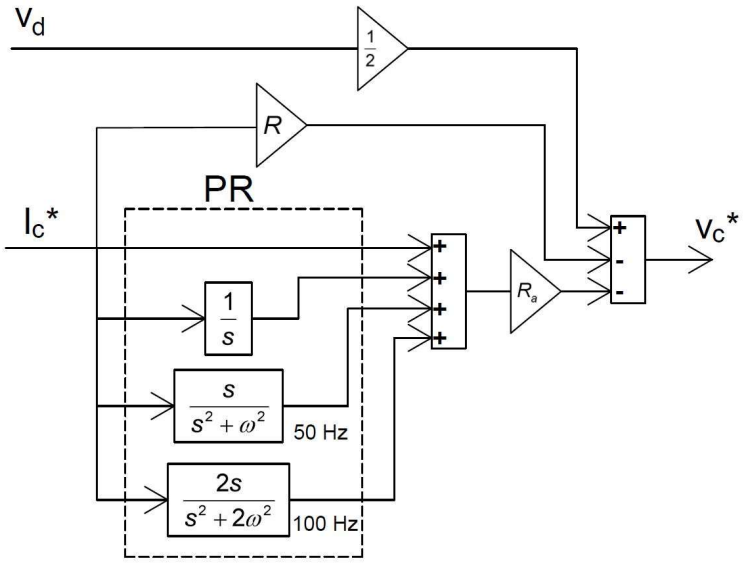

Figure 2.10: Circulating current controller

As mentioned before, the circulating currents is the mean of transfer energy within the arms and so balancing the capacitor voltages. In order for this controller to correctly balance the MMC, two other controllers must be introduced, i.e. the energy sum and delta controllers. Revising equation **Equation (2.22)**, repeated for convenience.

$$\frac{dW_\Sigma}{dt} = 2v_c^\star i_c - v_s^\star i_s \qquad \frac{dW_\Delta}{dt} = v_c^\star i_s - 2v_s^\star i_c \tag{2.52}$$

By controlling W_Σ and W_Δ to respectively $W_{\Sigma 0}$ and 0, the mean value of v_{cu}^{Σ} and v_{cl}^{Σ} can then be controlled to v_d.

The W_{sum} and W_{delta} controllers are based on the energy level of each arm. This energy level is compared to a reference $W_{\Sigma 0}$ and 0 respectively which by the means of a P gain output a dc reference of circulating current. Also on this controller a band stop filter tuned for 50 Hz and 100 Hz components is present. This controllers can be observed on both **Figure 2.11** and **Figure 2.12**.

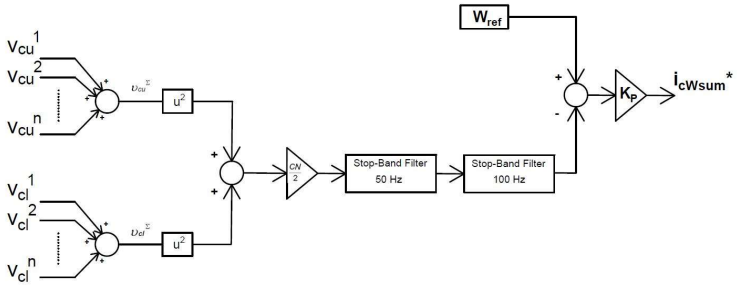

Figure 2.11: Block diagram of the W_{sum} controller

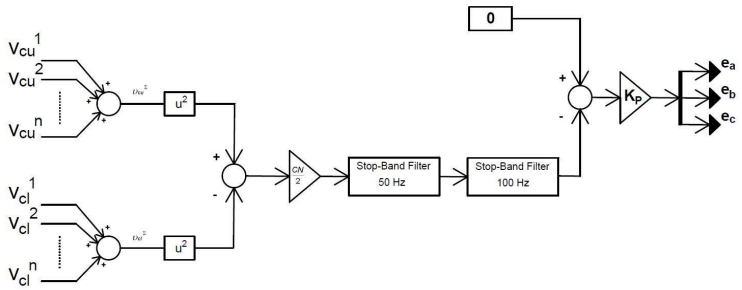

Figure 2.12: Block diagram of the W_{delta} controller

The W_{delta} control has an addition feature. This controller, as mentioned before, outputs a dc current reference. This current reference is then transformed in a 50 Hz component following the strategy in **Figure 2.13**. This strategy was presented in [29] and implemented in [30].

The concept behind it, is to "move" active power in order to balance the arms of the MMC. For that each phase of the circulating current will have three different components. This components are phase shifted between each other by $+90°$ and $-90°$. The objective is to combine this three components to form a vector that opposites to the unbalance in the system. The three components on each phase are defined as:

$$i^*_{ca1} = e_a \cos(\omega t) + \frac{1}{\sqrt{3}} e_b \cos(\omega t + \frac{\pi}{2}) + \frac{1}{\sqrt{3}} e_c \cos(\omega t - \frac{\pi}{2}) \tag{2.53}$$

$$i^*_{ca2} = e_b \cos(\omega t - \frac{2\pi}{3}) + \frac{1}{\sqrt{3}} e_a \cos(\omega t - \frac{7\pi}{6}) + \frac{1}{\sqrt{3}} e_c \cos(\omega t - \frac{\pi}{6}) \tag{2.54}$$

$$i^*_{ca3} = e_c \cos(\omega t + \frac{2\pi}{3}) + \frac{1}{\sqrt{3}} e_a \cos(\omega t + \frac{7\pi}{6}) + \frac{1}{\sqrt{3}} e_b \cos(\omega t + \frac{\pi}{6}) \tag{2.55}$$

With this strategy, three components representing the difference between the upper and lower capacitor voltages of each of three legs (e_a, e_b, e_c) are introduced into each phase of the circulating current. This allows not just to balance the energy in each leg individually but also the MMC together. The complete implementation can be observed on **Figure 2.13**.

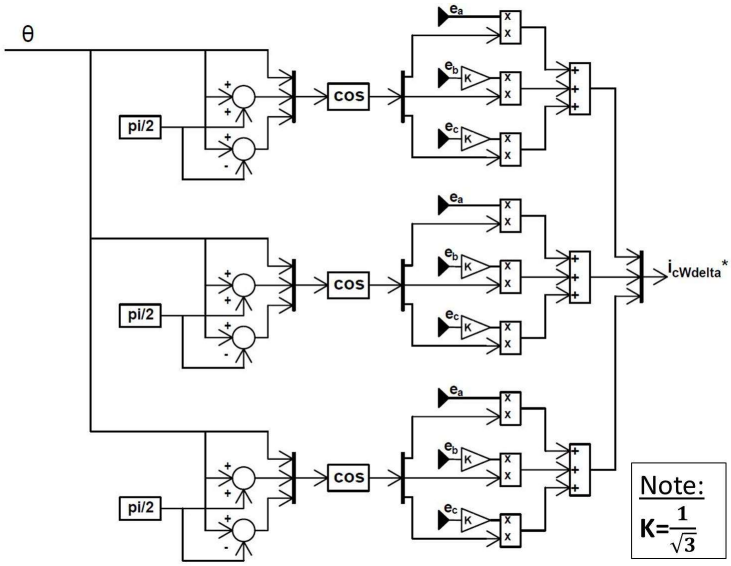

Figure 2.13: Complete implementation of balance strategy.

Chapter 3

Dimension and Control of MMC

This chapter presents an overview of the main circuit design used to model the back-to-back MMC. Furthermore, the control tunning technique based in SiSO-tool is commented and the main aspects adressed.

3.1 System Design

The design of the main components of the MMC structure is of grate importance. Besides the desire of having an optimum performance, often other considerations as the oversize and cost of the components are as important.

3.1.1 Main Input Data

The intent of this work is to project a medium voltage system capable of connecting the generation to the grid. For that a back-to-back system was design based on the Modular Multilevel Converters technology. From figure 3.1 it is possible to observe the projeted system. Is constituted by two MMCs operating in rectifier and inverter mode. The MMC operating as rectifier has the objective of maintain and controlling the dc-link voltage, while the inverter to control the need for active and reactive power. The interconnection to the grid is guaranteed by a delta-star transformer with the star side connected to ground.

The system has the following initial parameters:

$M = 3$	(number of phases)
$V_s = 6\ kV$	(line-to-line voltage)
$P = 10\ MW$	(active power required)
$Q = 6.5\ Mvar$	(reactive power required)
$f_g = 50\ Hz$	(grid frequency)

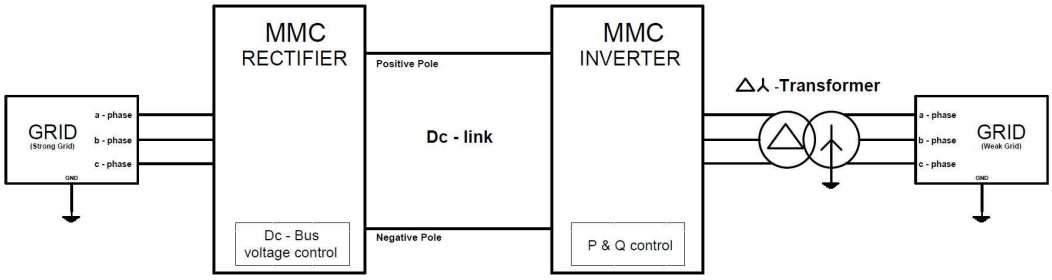

Figure 3.1: Schematic of the projected system.

From this initial data other parameters can be obtained. The peak output voltage, Dc-link voltage, peak output current and rated frequency will later on be used to design the system.

$$\widehat{V}_s = \frac{6kV}{\sqrt{3}} \times \sqrt{2} = 4.9\ kV \tag{3.1}$$

$$v_d = 2 \times \widehat{V}_s = 9.8\ kV \tag{3.2}$$

$$\widehat{I}_s = \frac{\sqrt{2}S}{3\widehat{V}_s} = 1.623\ kA \tag{3.3}$$

$$\omega_1 = 2\pi \cdot 50\ rad/s \tag{3.4}$$

3.1.1.1 Bases Quantities

The per unit bases are defined as follows:

$$S_{base} = 11.92\ MVA \tag{3.5}$$

$$V_{base} = 4.9\ kV \tag{3.6}$$

$$I_{base} = 1.623\ kA \tag{3.7}$$

$$Vsub_{base} = 9.8\ kV \tag{3.8}$$

$$Iarm_{base} = 1.02\ kA \tag{3.9}$$

$$V_{dbase} = 9.8\ kV \tag{3.10}$$

$$I_{dbase} = 1.02\ kA \tag{3.11}$$

$$Wrec_{base} = 300\ kJ \tag{3.12}$$

3.1.2 MMC design

3.1.2.1 Choice of the number of submodules

The choice of the number of submodules is a key aspect in desgin any MMC. This selection is not straightforward as several aspects have to be evaluated to ensure a proper and safe operation of the system. The procedure used in this project for selecting the number of submodules follows [16]. In this procedure three vital parameters need to be known:

1. The Average sum capacitor voltage per arm $\overline{v^{\Sigma}_{cu,l}}$, can be approximate to the rated dc-side pole-to-pole voltage $V_{d,n}$:

$$\overline{v^{\Sigma}_{cu,l}} = V_{d,n} = 9.8\ kV \tag{3.13}$$

2. The Average submodule capacitor voltage, $V_{c,n}$ is determine considering mainly the submodule reliability due to cosmic ray and the submodule capacitor voltage ripples.

   - The cosmic radiation effect localizes in the silicon lattice of the semiconductor devices, ultimately this leads to device de-rating precipitating the process of thermal runaway. In order to avoid such phenomenon the semiconductor devices normally operate at lower voltage ratings. In [16] an example of a semiconductor device rated at 4.5kV operating with a dc-link voltage of 2.8kV was used as a guide line. Considering a Infineon IGBT Power Module of 1700 kV / 1400A [31] and following the same principle:

   $$V_{c,n} = 1.7\ kV \longrightarrow 1\ kV \tag{3.14}$$

   Note: For further information on cosmic ray phenomenon references [16] and [32] can be consulted.

   - The submodule capacitor voltage ripples has been considered in this project as $\pm 10\%$. For that reason the average submodule capacitor voltage can be further calculated as:

   $$V_{c,n} = 1\ kV \times 0.9 = 900V \tag{3.15}$$

3. The number of submodules, N can now be calculated as:

$$N = \frac{\overline{v^{\Sigma}_{cu,l}}}{V_{c,n}} \approx 11 \tag{3.16}$$

3.1.2.2 Choice of submodules capacitance

The choice of the submodule capacitance often implies a trade-off. On one side a High value of capacitance results in a high cost of the MMC system and on the other hand a low value of capacitance results in a high ripple. For this reason an optimum choice for the submodule capacitance is fundamental for a successful design. The procedure used in this project to select this capacitance follows [33]. The nominal energy storage in one submodule capacitor is given, with i being the submodule number, by:

$$W_{sub} = \frac{1}{2}C(v^i_{cu,l})^2 \tag{3.17}$$

Where C is the submodule capacitance and $v^i_{cu,l}$ given by:

$$v^i_{cu,l} = \frac{v_d}{N} \tag{3.18}$$

The total energy storage per arm considering N submodules is then expressed as:

$$W_{u,l} = \frac{N}{2}C(v^i_{cu,l})^2 \tag{3.19}$$

A new concept needed to introduce for design the submodule capacitance is the time average of the submodule energy k_{dc}. The factor k_{dc} relates the nominal submodule voltage and the voltage that is related with the time average of the storage energy in the submodules. This yields:

$$v^i_{cu,l} = k_{dc}\frac{v_d}{N} \tag{3.20}$$

Merging **Equation (3.19)** and **Equation (3.20)** expresses the energy in each arm of the MMC as function of the new factor k_{dc}, as:

$$W_{u,l} = \frac{1}{2}\frac{C}{N}k^2_{dc}V^2_d \tag{3.21}$$

Other concept related to the capacitor ripple is k_{max}. This factor defines the maximum allowed instantaneous capacitor voltage and is expressed as:

$$v^i_{cu,l} \leqslant k_{max}\frac{v_d}{N} \tag{3.22}$$

With this the maximum energy storage in a submodule is defined by **Equation (3.19)** and **Equation (3.22)** as:

$$W_{max} = \frac{1}{2}\frac{C}{N}k^2_{max}V^2_d \tag{3.23}$$

The maximum excess energy that can be storage in each arm is defined as:

$$\Delta W_{max} = W_{max} - W_{u,l} \longrightarrow \Delta W_{max} = \frac{1}{2}\frac{C}{N}V_d^2(k_{max}^2 - k_{dc}^2) \tag{3.24}$$

Solving **Equation (3.23)** for C and substituting in **Equation (3.24)** the minimum energy storage capability for each arm is found:

$$W_{max} \geqslant \frac{k_{max}^2}{k_{max}^2 - k_{dc}^2}\Delta W_{max} \tag{3.25}$$

This last formula is the base to design any submodule capacitance. It also gives insight on the constrains inherent for any system. This constraints can be determine for a sinusoidal voltage reference or a third harmonic voltage reference as:

1. The excess energy storage ΔW_{max} can be calculated considering an energy variation with a sinusoidal voltage reference or with a third-order harmonic injection.

Sinusoidal Voltage Reference
With a sinusoidal voltage reference the upper and lower arm voltages can be determine as:

$$v_u = \frac{v_d}{2} - \frac{v_d}{2}m\cos(\omega_1 t) \tag{3.26}$$

$$v_l = \frac{v_d}{2} + \frac{v_d}{2}m\cos(\omega_1 t) \tag{3.27}$$

The arm currents, disregarding harmonic content on the circulating current, can be expressed as:

$$i_u = \frac{\widehat{I}_s}{4}m\cos(\varphi) + \frac{\widehat{I}_s}{4}m\cos(\omega_1 t - \varphi) \tag{3.28}$$

$$i_l = \frac{\widehat{I}_s}{4}m\cos(\varphi) - \frac{\widehat{I}_s}{4}m\cos(\omega_1 t - \varphi) \tag{3.29}$$

The instantaneous power in each arm is given by the product of **Equation (3.26)** with **Equation (3.28)** and **Equation (3.27)** with **Equation (3.29)**

$$p_u = \frac{v_d\widehat{I}_s}{8}[2\cos(\omega_1 t - \varphi) - m\cos(2\omega_1 t - \varphi) - m^2\cos(\omega_1 t)\cos(\varphi)] \tag{3.30}$$

$$p_l = -\frac{v_d\widehat{I}_s}{8}[2\cos(\omega_1 t - \varphi) + m\cos(2\omega_1 t - \varphi) - m^2\cos(\omega_1 t)\cos(\varphi)] \tag{3.31}$$

Integrating **Equation (3.30)** and **Equation (3.31)**, including:

$$v_d = \frac{2\widehat{V}_s}{m} \tag{3.32}$$

Yields the energy variation in the upper and lower arm:

$$e_u = \frac{S}{12m\omega_1 t}[4\sin(\omega_1 t - \varphi) - m\sin(2\omega_1 t - \varphi) - 2m^2\sin(\omega_1 t)\cos(\varphi)] \quad (3.33)$$

$$e_l = -\frac{S}{12m\omega_1 t}[4\sin(\omega_1 t - \varphi) + m\sin(2\omega_1 t - \varphi) - 2m^2\sin(\omega_1 t)\cos(\varphi)] \quad (3.34)$$

Where S is the total apparent power:

$$S = \frac{3}{2}\widehat{V}_s\widehat{I}_s \quad (3.35)$$

The excess energy storage is then obtained as the peak value of the energy variation.

$$\Delta W_{max} = max(e_u) \quad (3.36)$$

Third Harmonic Voltage Reference

With a third harmonic order injection in the reference output voltage $v_s^\star$, the operation capability of the MMC can be increased. Under this condition the upper and lower arm voltages can be determine as:

$$v_u^{th} = \frac{v_d}{2} - \frac{v_d}{2}m\cos(\omega_1 t) + \frac{v_d}{12}m\cos(3\omega_1 t) \quad (3.37)$$

$$v_l^{th} = \frac{v_d}{2} + \frac{v_d}{2}m\cos(\omega_1 t) - \frac{v_d}{12}m\cos(3\omega_1 t) \quad (3.38)$$

The instantaneous power in each arm for third harmonic injection is now given as the product of **Equation (3.37)** and **Equation (3.38)** with **Equation (3.28)** and **Equation (3.29)** respectively, yielding:

$$p_u^{th} = p_u + \frac{v_d\widehat{I}_s}{48}m^2\cos(3\omega_1 t)\cos(\varphi) + \frac{v_d\widehat{I}_s}{24}m\cos(3\omega_1 t)\cos(\omega_1 t - \varphi) \quad (3.39)$$

$$p_l^{th} = p_l - \frac{v_d\widehat{I}_s}{48}m^2\cos(3\omega_1 t)\cos(\varphi) + \frac{v_d\widehat{I}_s}{24}m\cos(3\omega_1 t)\cos(\omega_1 t - \varphi) \quad (3.40)$$

Integrating the previous expressions and substituting v_d by **Equation (3.32)**, yields the energy variations in the upper and lower arm as:

$$e_u^{th} = e_u + \frac{S}{12\omega_1 t}[\frac{m}{9}\sin(3\omega_1 t)cos(\varphi) + \frac{1}{12}\sin(4\omega_1 t - \varphi) + \frac{1}{6}\sin(2\omega_1 t + \varphi)] \quad (3.41)$$

$$e_l^{th} = e_l - \frac{S}{12\omega_1 t}[\frac{m}{9}\sin(3\omega_1 t)cos(\varphi) - \frac{1}{12}\sin(4\omega_1 t - \varphi) - \frac{1}{6}\sin(2\omega_1 t + \varphi)] \tag{3.42}$$

The excess energy storage is then obtained as the peak value of the energy variation.

$$\Delta W_{max}^{th} = max(e_u^{th}) \tag{3.43}$$

2. The relation between the voltage and the energy stored in the arm can be related as:

$$e_{arm} = \frac{N}{2}C\left(\frac{v_{cu,l}^{\Sigma}}{N}\right)^2 \tag{3.44}$$

The instantaneous value of the energy storage in each arm can be represented as $W_{u,l}$ and is alternating component e_u

$$W_{u,l} + e_u \geqslant \frac{C}{2N}v_u^2 \tag{3.45}$$

$$W_{u,l} + e_l \geqslant \frac{C}{2N}v_l^2 \tag{3.46}$$

Now substituting $W_{u,l}$ with **Equation (3.21)** and C with **Equation (3.24)**, yields:

$$\frac{k_d^2 c\Delta W_{max}}{k_{max}^2 - k_d^2 c} + e_u \geqslant \frac{\Delta v_u^2}{V_d^2(k_{max}^2 k_{dc}^2)} \tag{3.47}$$

$$\frac{k_d^2 c\Delta W_{max}}{k_{max}^2 - k_d^2 c} + e_l \geqslant \frac{\Delta v_l^2}{V_d^2(k_{max}^2 k_{dc}^2)} \tag{3.48}$$

solving for k_{dc}

$$k_{dc} \geqslant \sqrt{\frac{n_u^2 - e_{v,u}^2 k_{max}^2}{1 - e_{v,u}}} \tag{3.49}$$

$$k_{dc} \geqslant \sqrt{\frac{n_l^2 - e_{v,l}^2 k_{max}^2}{1 - e_{v,l}}} \tag{3.50}$$

Where,

$$n_u = \frac{v_u}{v_d} \qquad n_l = \frac{v_l}{v_d} \tag{3.51}$$

$$e_{v,u} = \frac{e_u}{\Delta W_{max}} \qquad e_{v,l} = \frac{e_l}{\Delta W_{max}} \tag{3.52}$$

3. The value of k_{max} is related with the maximum allowed ripple, in this project a $\pm 10\%$ is considered and so:

$$k_{max} = 1.1 \tag{3.53}$$

Now is possible to calculate the minimum energy requirement. Substituting in **Equation (3.25)**, respectively **Equation (3.49)**, **Equation (3.36)** and **Equation (3.53)**, yields:

$$W_{max} = \frac{k_{max}^2 \Delta W_{max}}{k_{max}^2 - max\left(\frac{n_u^2 - e_{v,u}^2 k_{max}^2}{1 - e_{v,u}}\right)} \tag{3.54}$$

Finally is possible to express the energy storage requirement as function of the total energy per transferred, VA as:

$$W_{rated} = \frac{6}{S} W_{max} \tag{3.55}$$

It is common to assume a rated energy $W_{rated} = 30kJ/MVA$ for an MMC system transferring exclusively active power. In the case of this project the system has the need to transfer both active and reactive power and so a different value of rated energy is needed. For that reason **Equation (3.55)** was plotted for different values of modulation index and power factor angle as can be seen from **Figure 3.2** and **Figure 3.3**.

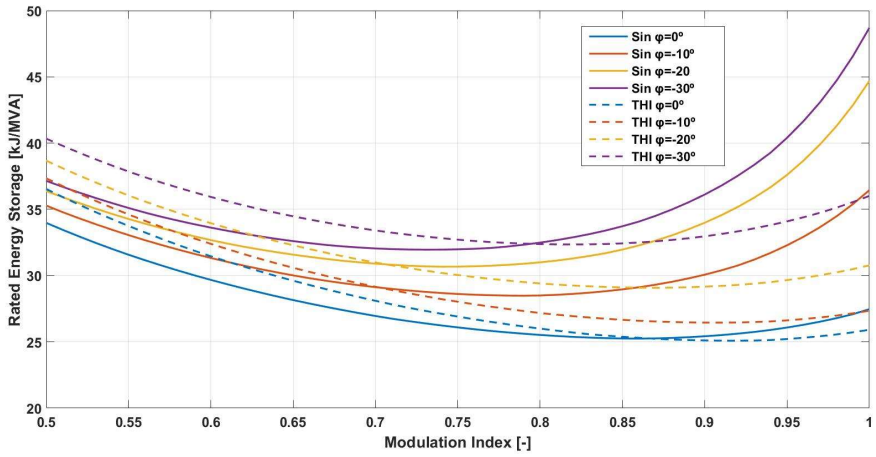

Figure 3.2: Energy storage capability W_{rated} per transferred VA for a converter consuming reactive power. Considering both sinusoidal and third harmonic voltage reference.

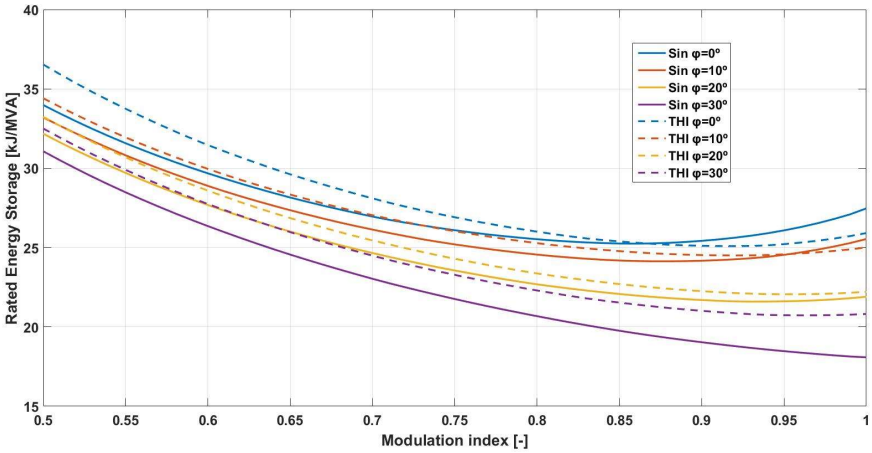

Figure 3.3: Energy storage capability W_{rated} per transferred VA for a converter generating reactive power. Considering both sinusoidal and third harmonic voltage reference.

It can be observed that for a power angle negative, the energy storage requirements increase as function of the modulation index and of the power factor. For a sinusoidal voltage reference the energy requirement also increases when compared to a third harmonic voltage reference. At this power factor the converter is considered to be consuming reactive power.
Now, for a positive power angle, the converter is considered to be generating reactive power. Under this conditions an opposite phenomenon but with smaller magnitude is presented. The usage of third harmonic voltage reference increases the necessity for a higher energy requirements.
It is now possible to determine the energy storage necessity for the system. Considering a MMC with a unit modulation index ($m = 1$) a capacitor ripple of $\pm 10\%$ ($k_{max} = 1,1$) and a sinusoidal voltage reference "SIN". The Back-to-Back MMC has to exchange both active and reactive power, yielding a power angle close to 32°. Looking closer to **Figure 3.2** a rated energy value of $W_{rated} = 49\, kJ/MVA$ is obtained.

After the energy requirements are known the total arm capacitance can be calculated as:

$$C_{arm} = \frac{2NW_{rated}(\frac{S}{6})}{v_d^2} = 24.3mF \tag{3.56}$$

3.1.2.3 Choice of arm inductors

The arm inductors are normally dry-type air-core reactors as it presents several benefits: constant inductance, absence of oil and simple insulation to ground [16]. One of the objectives in using arm inductors is to limit high frequency harmonics.

For that reason the arm inductors normally have a reduced value. Another benefit on using arm inductors is to limit the high surge current during fault conditions [34]:

- When the submodules of the MMC are equiped with auxiliary circuits, like bypass thyristors, to limit the dc-side faults the system can operate with rather lower values of inductance in the range of 0.05 p.u.
- When the submodules of the MMC do not have any auxiliary circuits to limit the fault currents then a value of arm inductance should be high enough. This normally yields a value in between 0.1 to 0.15 p.u.

For this project another approach was conducted. First different arm inductor values ranging from 0.06 p.u until 1.2 p.u were tested and the THD value presented in i_s was registered **Figure 3.4**. Through an optimization process the best value was choose.

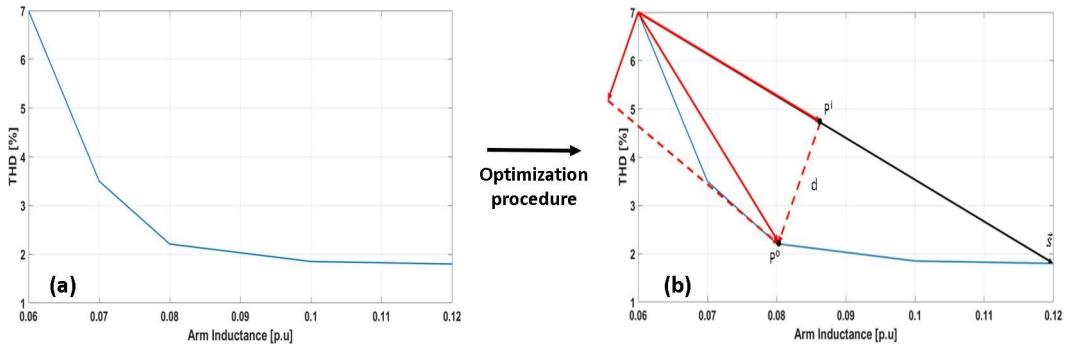

Figure 3.4: (a) Total Harmonic Distortion (THD) as a function of the arm inductance, (b) Optimization procedure

This optimization process is based on the "Direct Pareto Front (PF)" [35]. It finds the maximum distance d between the points of the curve P^o and the vector $\vec{s}$, such that:

$$d = |p^o - (p^o \cdot \widehat{s})\widehat{s}| \tag{3.57}$$

Where, $\widehat{s}$ denotates the normalized vector:

$$\widehat{s} = \frac{s}{|s|} \tag{3.58}$$

With this method it was possible to obtain an optimum point for the arm inductance of $L = 0.08p.u.$ In order to better understand the effect of the arm inductance in the operation of the MMC Figure 3.5 is presented.

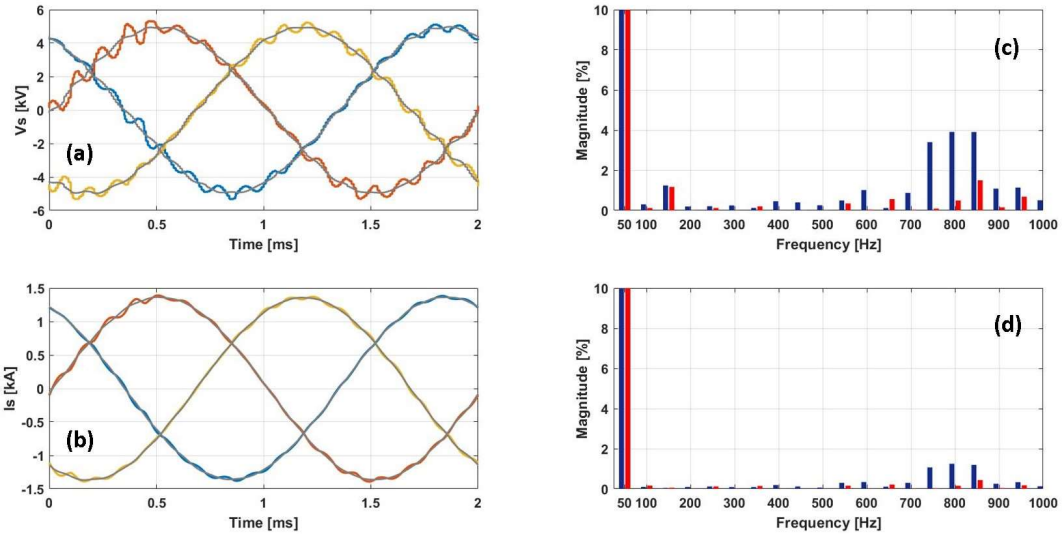

Figure 3.5: Comparison between the effect of the arm inductor for a value of L=0.06 p.u (coloured) and L=0.08 p.u (grey): (a)v_s, (b) i_s. Comparison of the harmonic content for L=0.06 p.u (blue) and L=0.08 p.u (red): (c) v_s and (d) i_s

Figure 3.5 illustrates the effect of the arm inductance on v_s and i_s. Two scenarios are considered $L = 0.06p.u$ and $L = 0.08p.u$. With a higher arm inductance the high frequency harmonics diminish. This has a direct effect into v_s and i_s waveform, reducing their oscillations. The opposite is observed for lower values of arm inductance where a high presence of oscillations are present on v_s and i_s waveform.

3.1.2.4 Design of arm resistance

The system losses in the arm inductors and in the submodules are modeled as a resistance in the arm. This parasitic resistance in this project was considered to be 10% of the arm reactance.

3.1.3 Grid parameters

On this section the grid design is presented. In this project two different grids were considered. Since the focus is on the energy conversion of the B2B-MMC, the generation side in this case the rectifier is not defined. For this reason no special modelling of the generation is defined, and so a strong grid (> >SCR) is considered. On the other hand, the inverter side at where the grid is connected through a point of common coupling (PCC), is considered to be a weak grid (SCR=5) and so a more realistic scenario is presented. Other element studied in this project is a delta-star transformer connecting the inverter to the grid. This transformer has the main objective of eliminating the third-harmonic in the system by grounding the star side of the transformer.

3.1.3.1 Strong vs Weak grid

The grid operates at nominal voltage rating thus can be represented as a Thevenin equivalent. The Thevenin impedance can then be represented by:

$$L_g = \frac{\widehat{V}_s}{\widehat{I}_s \omega_1 SCR} \tag{3.59}$$

$$R_g = 10\% Z_{gbase} \tag{3.60}$$

As can be observed from **Equation (3.59)** the grid inductance is directly related with the Short Circuit Ration (SCR). A grid with lower SCR is considered to have poor voltage regulation, originating voltage stability problems. The same can be observed in **Figure 3.6** were the impact of a scenario with low and high SCR is presented. For low SCR **Figure 3.6** (a) and (b), V_s and I_s presents higher oscillations. For high SCR **Figure 3.6** (c) and (d) the opposite phenomenon is presented.

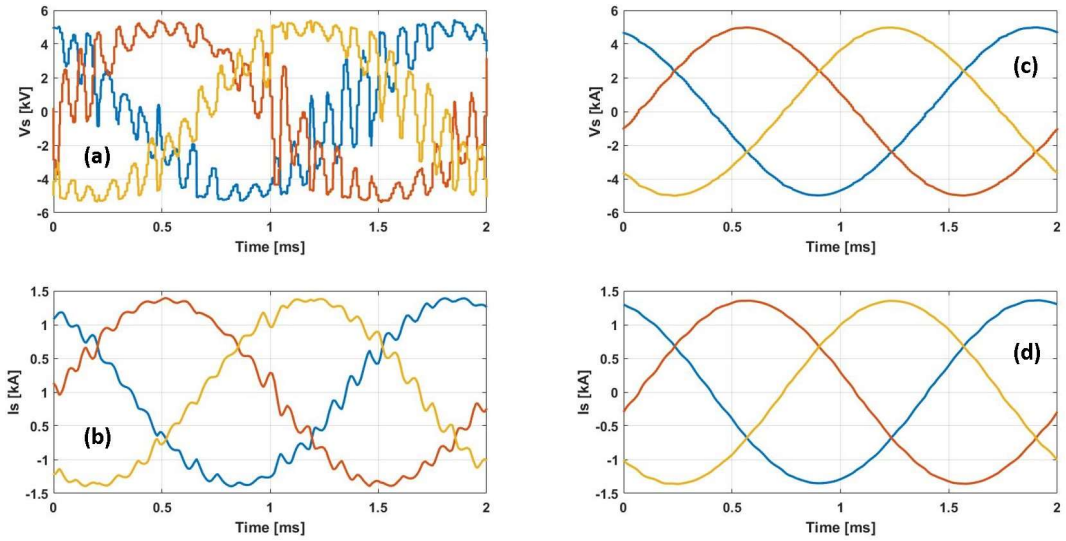

Figure 3.6: Comparison between week grid(SCR=5): (a) and (b) and strong grid (SCR=100): (c) and (d)

Since one of the objective of this projects is to simulate the occurrence of faults a grid with high SCR is not suitable, as it fails to represents this phenomenon. For this reason the grid was simulated with SCR=5 and an extended parameter tuning was required.

3.1.3.2 Transformer

The transformer inductance L_t is considered to be 6% of the voltage drop [36]. The calculation of the transformer inductance can be seen from **Equation (3.61)**. The values of the base quantities (I_{base} and V_{base}) can be found in **Section 3.1.1.1**.

$$\begin{aligned} 6\% = \frac{Voltage\ \ drop\ \ across\ \ transformer}{Rated\ \ Base\ \ voltage} \times 100\% \\ \Rightarrow \mathrm{I}_{base} \times 2 \times \pi \times 50 \times L_t = 0.06 \times \mathrm{V}_{base} \\ \Rightarrow \mathrm{L}_t = 0.577\mathrm{mH} \end{aligned} \tag{3.61}$$

The transformer is an inductive component, but to represent its copper losses, a resistance is modelled which has 0.6% voltage drop across it. In power transformers, the magnetization current is less than 1 % of the rated value. Therefore, the effect of the magnetizing current is excluded.

The transformer is delta-star connected. Thus the primary side phase voltage is $\sqrt{3}$ times the secondary side phase voltage. The secondary side voltage is also 30 $^\circ$ phase shifted compared to the primary side voltage.

3.2 Control Tunning

For this project the Back-to-Back system was tunned considering the following procedure:

1. Decouple the two MMCs: connect respectively the rectifier to a current source with rated current in parallel with a resistance for fixing the rated dc-voltage. To the inverter should be connected a dc-source with rated dc-voltage.

2. With the system decoupled, SISO-tool can be used to provide a starting point for the tunning process and to access the system stability.

3.2.1 Output Voltage Control

As mentioned previously this controller has the objective of controlling the dc-bus voltage. The parameters governing the Output Voltage controller are the following:

$\alpha_f = 100$	Corner frequency in [rad/s]
$\alpha_d = 250$	Control-loop bandwidth [rad/s]
$\alpha_i d = \frac{\alpha_d}{8}$	Integrator bandwidth [rad/s]
$C_{eq} = Cd + \frac{C}{N}$	Equivalent capacitance [F]
$K_p = \alpha_d \frac{C_{eq}}{2}$	Proportional gain

Where α_f is the corner frequency of the low pass filter. The PI controller is characterized by the P and I bandwidth, respectively α_d and α_{id}. The proportional gain K_p is a function of the equivalent capacitance C_{eq} and its self bandwidth.
In order to proper analysed the output voltage controller a SISOtool approach was followed. Since all the controllers on an MMC relate to each other a decouple is necessary, for that a transfer function representing the "PLANT" for each individual controller is needed.
Remembering **Equation (2.37)** and considering a fast controller then:

$$v_d i_d - P = P^\star \Longrightarrow \frac{v_d^2}{P^\star} = \frac{2}{sC'} \tag{3.62}$$

Now adding to the plant transfer function, the PI controller and also a butterworth second order low pass filter, yields the following control loop architecture:

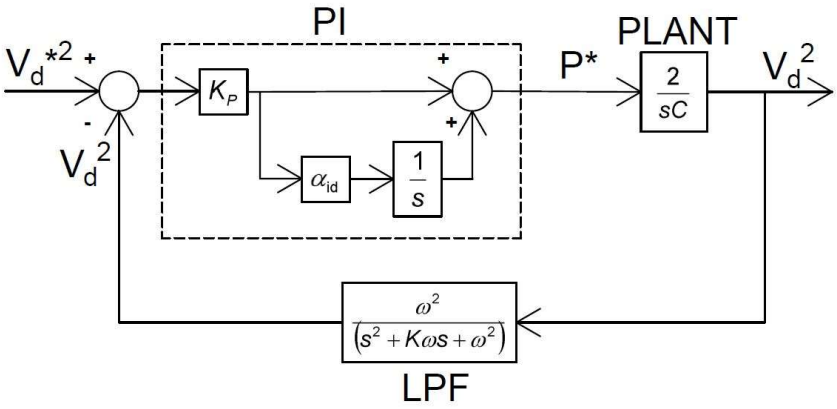

Figure 3.7: Control loop architecture used in SISOtool to analyze the output voltage controler

It is now possible to infer the stability of the DC-bus controller. On **Figure 3.8** the bode diagram for the open-loop DC-bus controller is depicted. The system is stable with a gain and phase margin of 8.59 dB and 33.4° respectively.

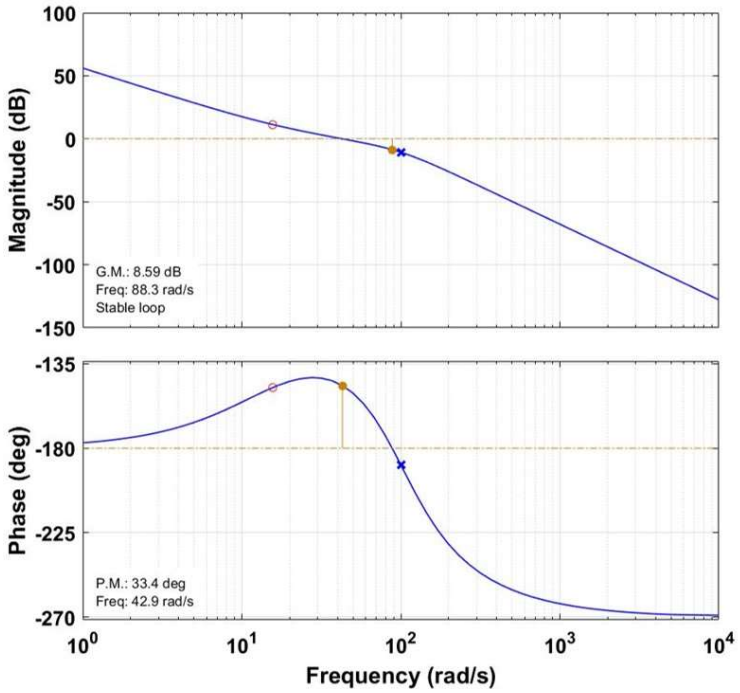

Figure 3.8: Bode diagram of DC-bus voltage controller

3.2.2 PR controller

The tunning process of the PR controller is presented in this section. The parameters governing the PR controller are the following:

$\alpha_c = 2000/800$	PR controller bandwidth [rad/s]
$\alpha_h = 50$	R-part bandwidth [rad/s]
$K_P = \alpha_c \times (\frac{L}{2} + L_g + L_T)$	P gain
$K_h = 2\alpha_h K_P$	R gain

Where α_c is the closed-loop bandwidth of the system and α_h the bandwidth of the resonant integrator. K_P and K_h are respectively the proportional and resonant gains of the controller. This gains are calculated by the arm and grid inductance and, when present, the transformer inductance.
As before for analysing the system SISO-tool was again used. For these the transfer function of a PR controller explained on **Section 2.5.3** was used. Moreover, a transfer function representing the PLANT is added. It is considered as the contribution of the arm inductance and parasitic resistance. This control architecture can be observed on **Figure 3.9**.

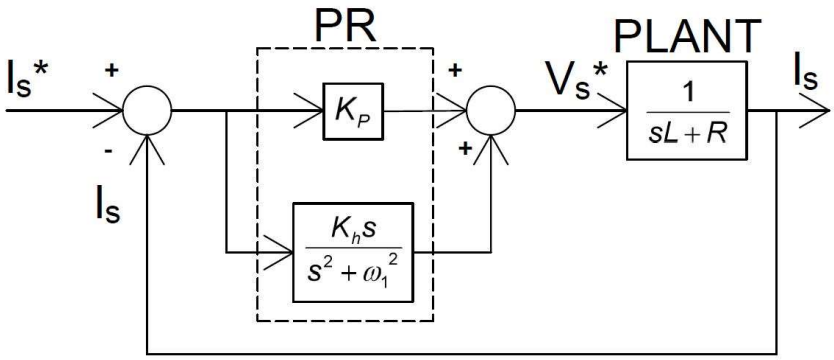

Figure 3.9: Control loop architecture used in SISOtool to analyze the PR controller

As can be seen for the schematic in the beginning of this section, α_c has two different values. This values depend if the MMC is present on a strong or weak grid **Section 3.1.3.1**. The direct effect of this is the reduction of the closed-loop bandwidth for grids with lower SCR. For further evaluation, the root locus assessing the stability of the system for two different values of α_c is presented. It is possible to observe that both MMCs are stable presenting infinite gain margin and similarly phase margins of 87.1° and 86.2° respectively.

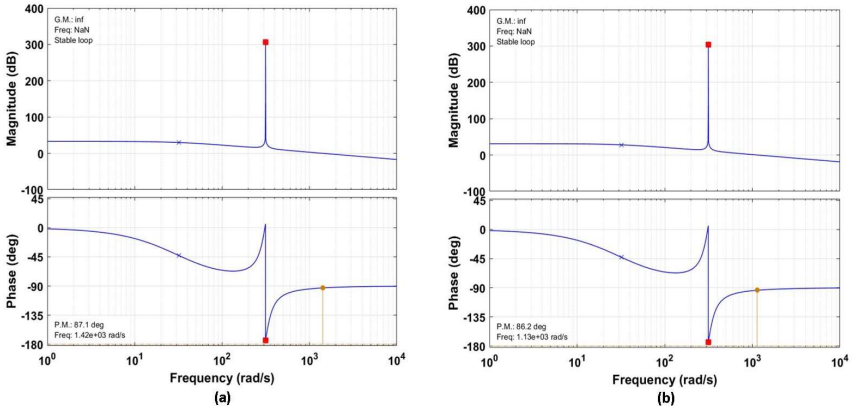

Figure 3.10: Bode diagram of the open loop PR controller: (a) inverter (b) rectifier.

3.2.3 Circulating current controller

The circulating current controller is the most complex of the controllers presented so far. The parameters governing the circulating current controller are the following:

$R_a = 2$	"Active resistance" for circulating current controller
$\alpha_2 = 200$	R-part bandwidth [rad/s]
$K_2 = 2\alpha_2$	R gain for 100 Hz (h=2)
$K_1 = 2K_2$	R gain for 50 Hz (h=1)
$K_0 = \frac{K_2}{10}$	R gain for dc component (h=0)

Where, R_a is the P gain of the PR controller used in the circulating current. It is often refer as an "active resistance" or "virtual resistance". This PR controller has three resonant parts for the DC, 50Hz and 100 Hz components of the circulating current **Section 2.5.4.2**. For that three different gains: K_2, K_1 and K_0 are presented. The control architecture used on sisotool can be observed on **Figure 3.11**. It is first comprised of a butterworth second order low pass filter serving to eliminate the harmonic content, as input on the control structure. Moreover the PR controller for the different harmonic orders is presented. As in the case of the PR controller, the same transfer function considering the arm inductance and resistance are considered.

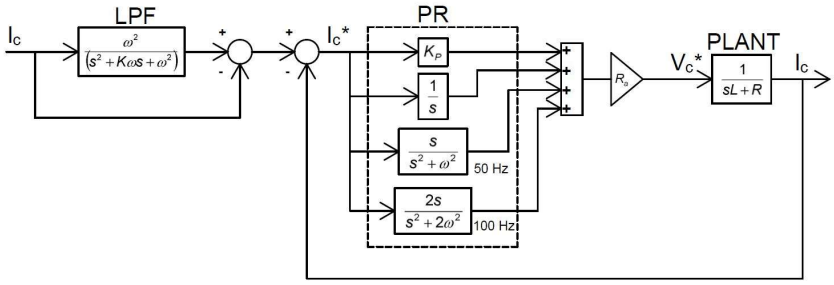

Figure 3.11: Bode diagram of the open loop PR controller: (a) inverter (b) rectifier.

From **Figure 3.12** the open loop bode diagram of the controller is presented. The system presents stability with a infinite gain and phase margin of 89.4°.

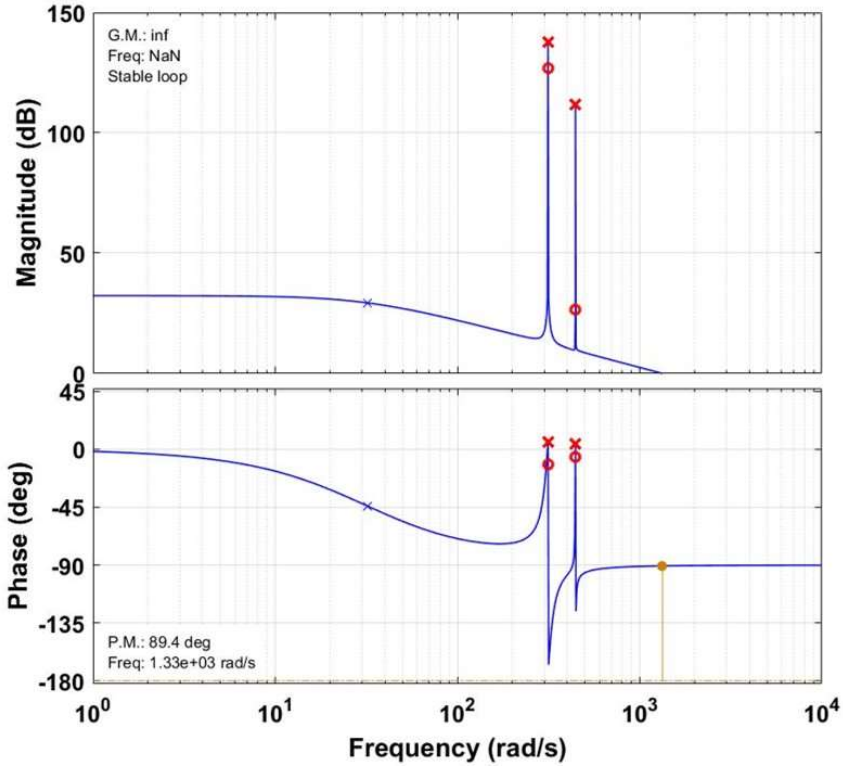

Figure 3.12: Bode diagram of the open loop PR controller: (a) inverter (b) rectifier.

3.3 Steady State Operation of the Back-to-Back MMC

The project focuses on the operation of the MMC in the steady state conditions whose system parameters are defined in **Section 3.1.1**. The active power reference P, changes at the rate of 1 p.u. per second and reactive power Q, changes at the rate of 20 p.u. per second. This can be seen from **Figure 3.13**

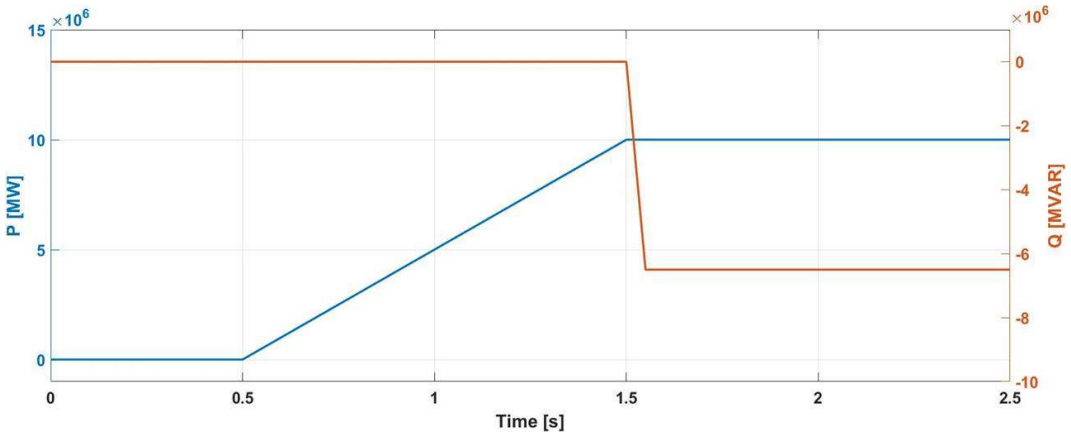

Figure 3.13: The variation in active and reactive power

In this section, the steady state analysis is performed over a time duration of 1 second in the time interval of 1.9s and 2.0s. The variation of v_d and i_d during this interval can be seen from **Figure 3.14**. It can be seen that the voltage ripples in v_d does not violate the voltage restrictions of $\pm 5\%$.

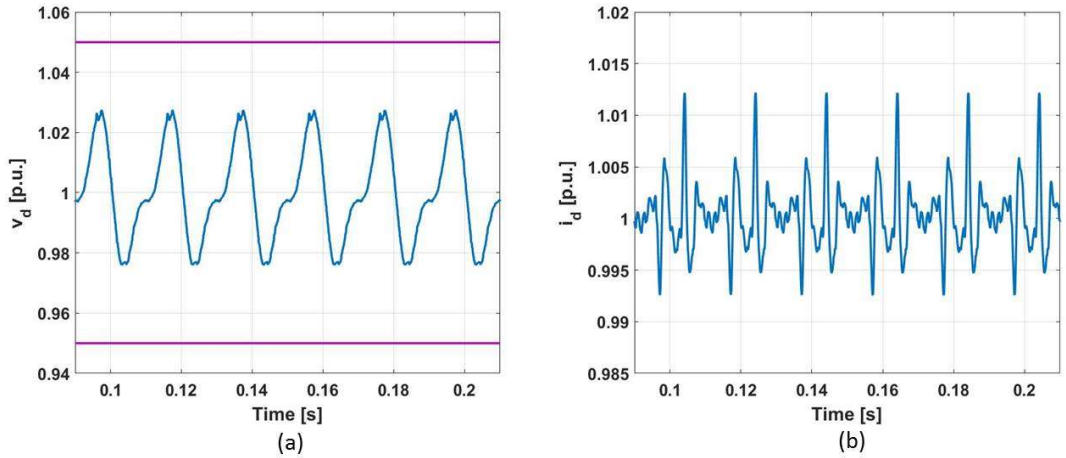

Figure 3.14: (a) DC-Link voltage v_d, (b) DC-Link current i_d during steady state condition

The AC voltage and current at the rectifier and the inverter terminals can be

seen from the **Figure 3.15**. The rectifier is connected to a strong grid of SCR =100 and the inverter is connecetd to a weak grid of SCR=5. **Figure 3.15**(c) shows that there is a voltage drop in v_S when power is transferred from the inverter to the weak grid. This drop in voltage arrises from the inductance on the arms of the MMC and on the transformer. However, this effect is not visible during the interaction of the rectifier and the grid connected to it because the rectifier is connected to the strong grid, which does not allow the change in the ac three-phase voltage. However, to transfer the same amount of active power the three-phase ac current magnitude increases over its nominal value to compensate for the reduced voltage.

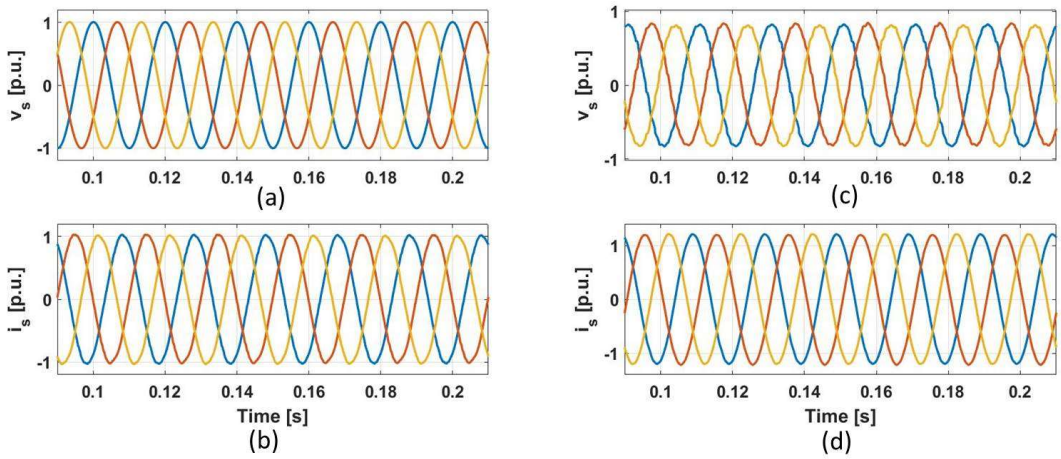

Figure 3.15: (a) Rectifier 3-Phase voltage, (b) Rectifier 3-Phase current, (c) Inverter 3-Phase voltage, (d) Inverter 3-Phase current during steady state condition.

The variation in the the upper arm and lower arm voltage and current under steady-state condition can be seen from **Figure 3.16**. It can be seen that the upper arm and lower arm quantities are 180° phase shifted. The ripples in the arm capacitor voltages increases with the reduction in power factor. However, the ripples are within the defined voltage violation limits of $\pm$ 10%. The reduction in power factor causes an asymmetry evident when compared the arm capacitor voltage waveforms of rectifier and inverter. of the rectifier and invert in the positive and negative half cycle. [16]

The ripples in the capacitor voltages have been reduced by decreasing the energy imbalance between the arms in each leg. As can be seen from **Figure 3.17**(a), (b), (c) and (d) that the energy difference between the arms is considered zero. This further corroborates the decrease in the magnitude of the circulating current seen from **Figure 3.17**(e) and (f).

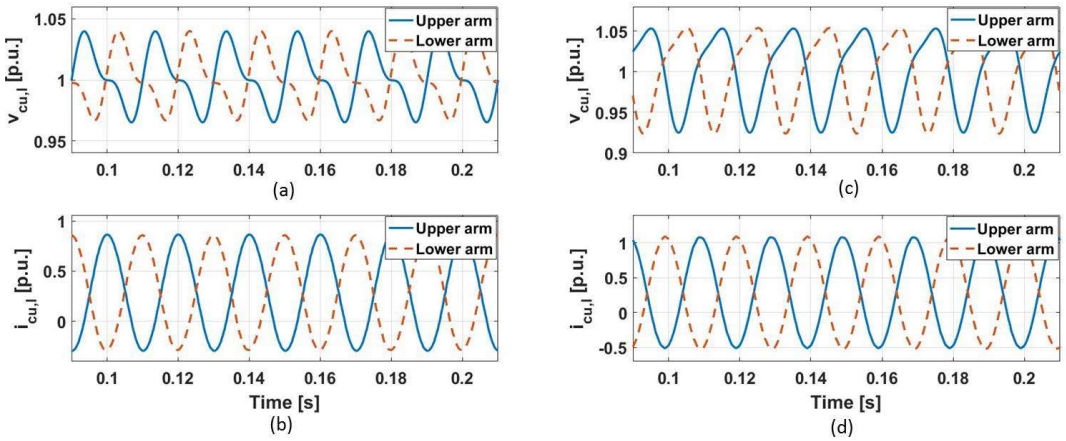

Figure 3.16: (a) Rectifier upper and lower arm voltage, (b) Rectifier upper and lower arm current, Inverter upper and lower arm voltage, (d) Inverter upper and lower arm current during steady state condition

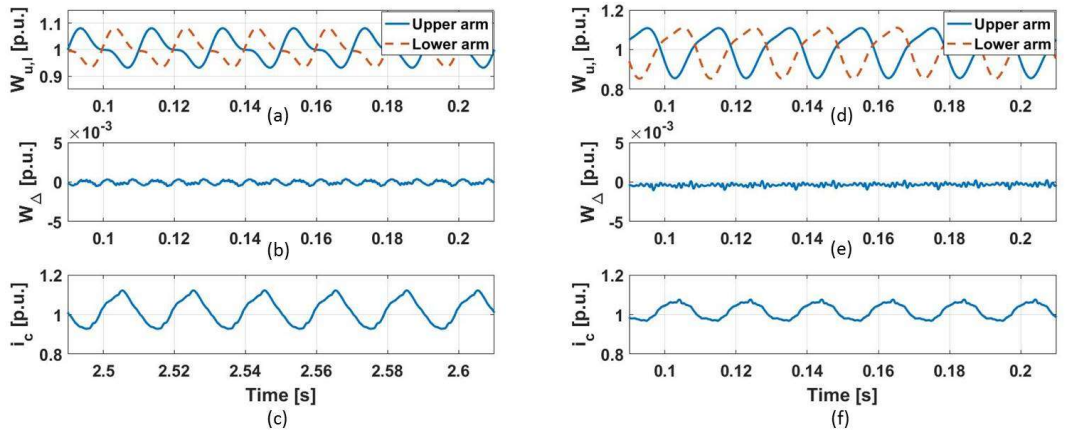

Figure 3.17: (a) Rectifier upper and lower arm energy, (b) Rectifier arm energy difference,(c) Rectifier circulating current, (d) Inverter upper and lower arm energy, , (e) Inverter arm energy difference and (f) Inverter circulating current during steady state condition

Chapter 4

DC-Link Ripple Analysis

In this chapter an analysis of the DC-Link ripple is presented. Moreover, three different techniques to reduce the DC-Link voltage ripple are presented based on the DC-Link dynamic equation. In this chapter the three methods are analysed and a final comparison among them is presented.

4.1 Introduction

In a classical 2-level VSC, capacitors are connect in the DC-Link. This allows the converter to store energy in the DC-Link itself and thereby helping in the DC-bus voltage control. In an MMC on the other hand, capacitors are placed inside the converter making the DC-Link free from any other elements besides the DC-cable [37].

These displacement of the capacitor location leads to a weaker dc-link, more susceptible to fluctuations. This fluctuations affect both the DC-Link voltage and current influencing the system performance. Moreover, these causes excess stress in the semiconductor devices and submodules capacitance. [24].

In these project three different methods are used to reduce the DC-Link ripple. These methods are derived based on the DC-bus dynamic equation described in section 2.4 by **Equation (??)** and repeated here for convenience:

$$\left(C_d + \frac{2MC}{N}\right)\frac{dv_d}{dt} = i_d - \frac{P}{v_d} \tag{4.1}$$

Rearranging the **Equation (4.1)**, yields:

$$\frac{dv_d}{dt} = \frac{\left(i_d - \frac{P}{v_d}\right)}{\left(C_d + \frac{2MC}{N}\right)} \tag{4.2}$$

It is now possible to directly relate the variables that can reduce the DC-bus voltage ripple:

- Increasing the capacitance of the MMC or the capacitance in the DC-Link.
- Undermodulate the system (m<1), by increasing v_d this originates a higher active power reference $P^\star$, due to the adopted control strategy **Section 2.5.1**.
- Utilization of space vector modulation in $v_s^\star$, this results in the reduction of the number of inserted submodules. Which then leads to the increases in the total capacitance of the MMC.

4.2 DC-Link Capacitance

The first method analysed to reduce the DC-Link ripple and often used in power converters, is to include a capacitor in the DC-Link. In two level VSC this is a common practice required to guarantee a stable DC-voltage level. On the MMC, the same principle can be employed.

In order to analyse the effect of the DC-Link capacitor on the system a test is performed for different values of DC-Link capacitance ranging from 0 μF to 250 μF. Considering for a MMC system with a unit modulation index ($m = 1$), a capacitor ripple of $\pm 10\%$ ($k_{max} = 1,1$), the energy requirement for a sinusoidal voltage references can be respectively calculated from **Figure 3.2** as $W_{rated} = 49kJ/MVA$.

In **Figure 4.1**, it is possible to observe the reduction in the DC-Link ripple with the increase in capacitance. For a situation without any DC-Link capacitance the ripple is of the order of 2.7%. As the value of C_d increases the ripples in v_d reduces until 1.3% and 0.6 % for a capacitor value of 62.5 μF and 250 μF or 3 kJ and 12 kJ respectively.

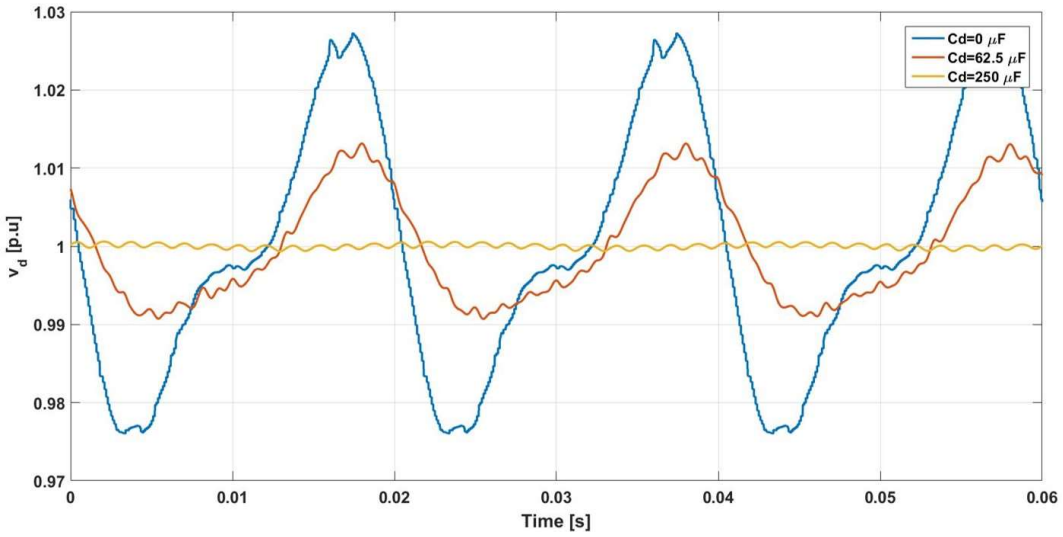

Figure 4.1: Comparison of the effect of different DC-Link capacitor values ranging from 0μF to 250μF, on the dc-link voltage.

In **Figure 4.2**, a continuation of the previous analysis is presented. The DC-Link voltage ripple is shown as a function of the DC-Link capacitor. It can be observed that the ripple percentage reduces with the increase in the Dc-Link capacitance. This phenomenon comes in agreement to the concept which was previously stated.

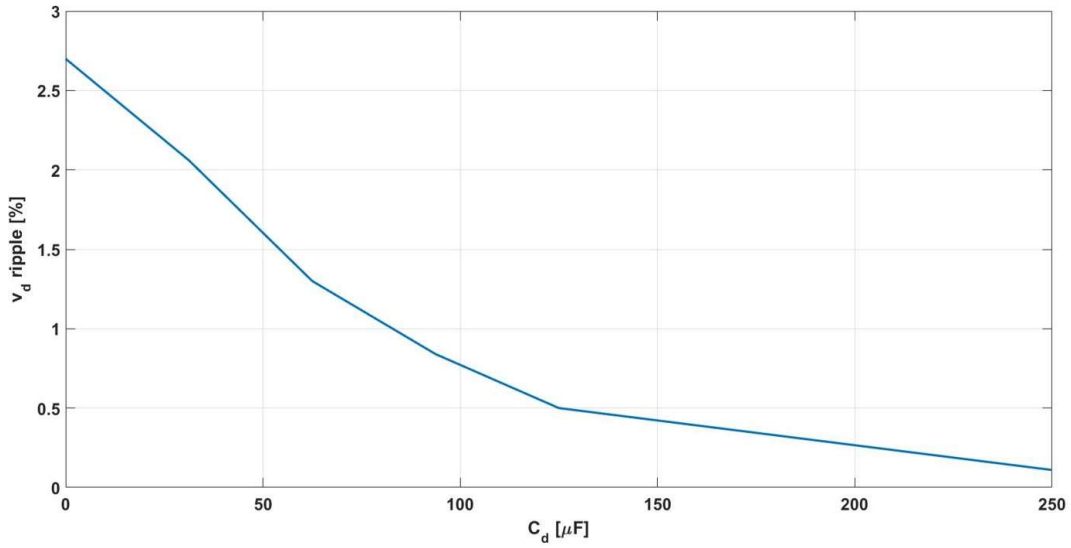

Figure 4.2: Dc-link ripple in percentage as function of the dc-link capacitance.

Another interesting analysis is to understand the effect, this ripple reduction technique has on the capacitor voltages. For that **Figure 4.3** presents the upper submodule capacitor voltages for both rectifier and inverter. It is easy to conclude the minor effect this ripple reduction technique has over the submodule capacitors voltages.

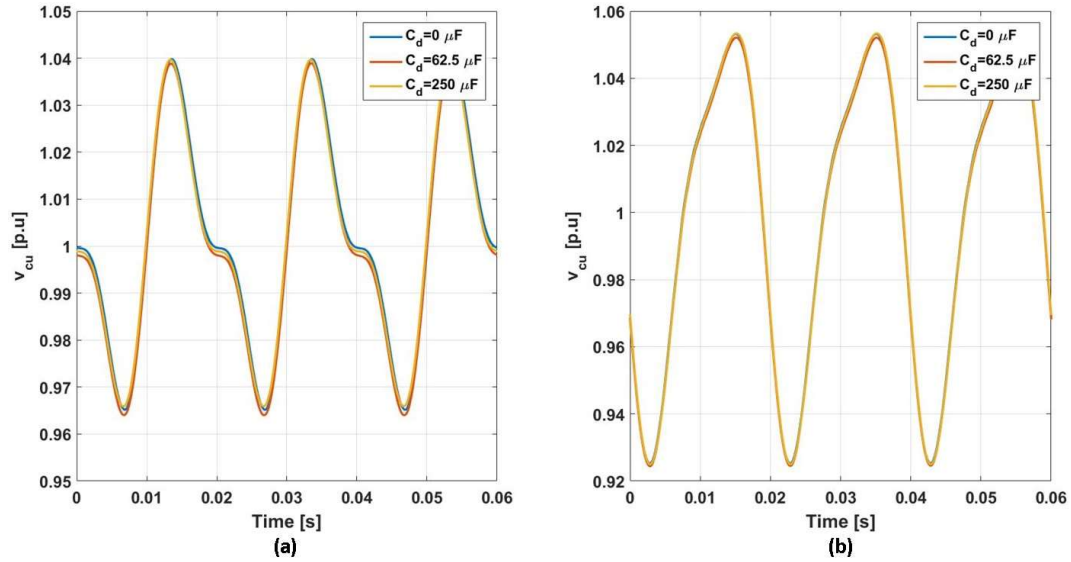

Figure 4.3: Submodule capacitor voltages for different DC-Link capacitor values: (a) Rectifier (b) Inverter.

In order to better understand the effect of the reduction in the DC-Link voltage fluctuations in the system, the circulating current can be observed. **Figure 4.4** presents the harmonic spectrum of the circulating current for both rectifier and inverter for three different cases: no DC-Link capacitor, 62.5 μF and 250 μF. It is possible to observe that as the capacitance increases, the 50 Hz, 100 Hz and 150 Hz components tends to decrease.

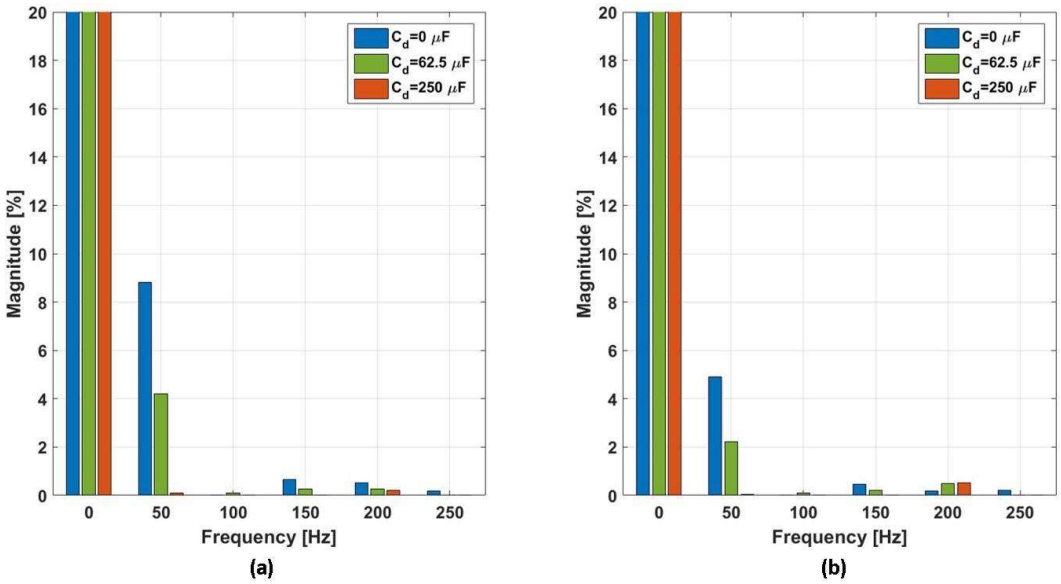

Figure 4.4: Circulating current harmonic spectrum for different values of capacitance: (a) Rectifier and (b) Inverter.

The harmonics in the circulating current can be further decomposed as:

- Dc component: one third of the dc-link current
- 50 Hz component: coming from the type of controller used in this project **Section 2.5.4.2**.
- 100+ Hz components: arise from the unbalance in the arm voltages.

It is now easy to relate the decrease in the harmonic content in the circulating current. This current is driven by the voltages between the upper and lower arms, which are more stable due to the introduction of the dc-link capacitor. This is caused by the opposition of C_d to the dv_d/dt and so reducing the ripples in the system.

$$v_c = \frac{v_u + v_l}{2} \tag{4.3}$$

Revising now **Equation (2.18)** the submodule capacitors ripple can be related both with i_s and i_c. It is then fair to assume that a reduction in the harmonic content of i_c, should reduce the submodule capacitor voltage ripples. But from **Figure 4.2** it is observed that the voltage ripples are minorly affected. An explanation for this phenomenon is that the impact of the circulating current in the capacitor voltage ripple is less when compared to i_s. Thus a decrease in i_c barely affects in the submodule capacitor voltage ripples.

4.3 Sinusoidal vs Third-Harmonic voltage reference

In the control architecture, as explained in **Section 2.5.3**, the output of the PR controller sets the output voltage reference to serve as input to the internal controller. This voltage reference can be sinusoidal or in a space vector modulation. This modulation technique is implemented with the "min-max method":

$$v^{\star}_{sth} = v^{\star}_{s} - \frac{max(v_{a,b,c}) + min(v_{a,b,c})}{2} \tag{4.4}$$

With $v_{a,b,c}$ being the phase voltages a,b and c. The subtraction of the common mode voltage from v_s allows for a third order harmonic injection in the phase voltage. By using this method, it is possible to increase the scalability of the system and thereby reducing the magnitude of the output voltage reference by a factor of about 0.866. This reduction theoretically helps in reducing the DC-bus voltage. [38]

In order to analyse the third harmonic effect on the system, a comparison between a sinusoidal voltage reference and a third-harmonic injected sinusoidal voltage reference is presented. Considering a modulation index of 1, a sub-module capacitor voltage ripple of $\pm 10\%$ ($k_{max} = 1.1$), the energy requirement for a sinusoidal and third-harmonic injected sinusoidal voltage references can be calculated from **Figure 3.2** as $W_{rated} = 49kJ/MVA$ and $W_{ratedth} = 36kJ/MVA$ respectively.

On **Figure 4.5** the effect of the space vector modulation with respect to a sinusoidal voltage reference can be depicted. It is possible to observe the reduction in the DC-bus voltage ripple from 2.7% to 1.5% **Figure 4.5** (a). This ripple reduction arises mainly from the diminishing in magnitude of the 50 Hz and 100 Hz voltage components **Figure 4.5** (b).

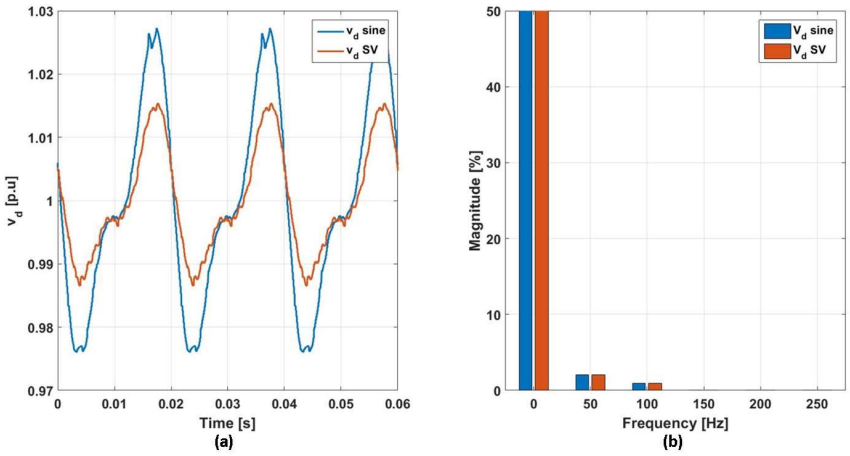

Figure 4.5: Comparison between sine and SV: (a) DC-Link voltage and (b) DC-Link voltage harmonic spectrum

Figure 4.6 illustrates the effect of the two different voltage references in the sub-module capacitors' voltages. As can be observed from **Figure 4.6** (a), (b), the space vector modulation increases the sub-module capacitor ripples on the rectifier and inverter sides to 5.1% and 7.1% respectively. This increase is due to an increase in the 50 Hz and 100Hz component and also the appearance of 150 Hz and 200 Hz voltage components **Figure 4.6** (c), (d).

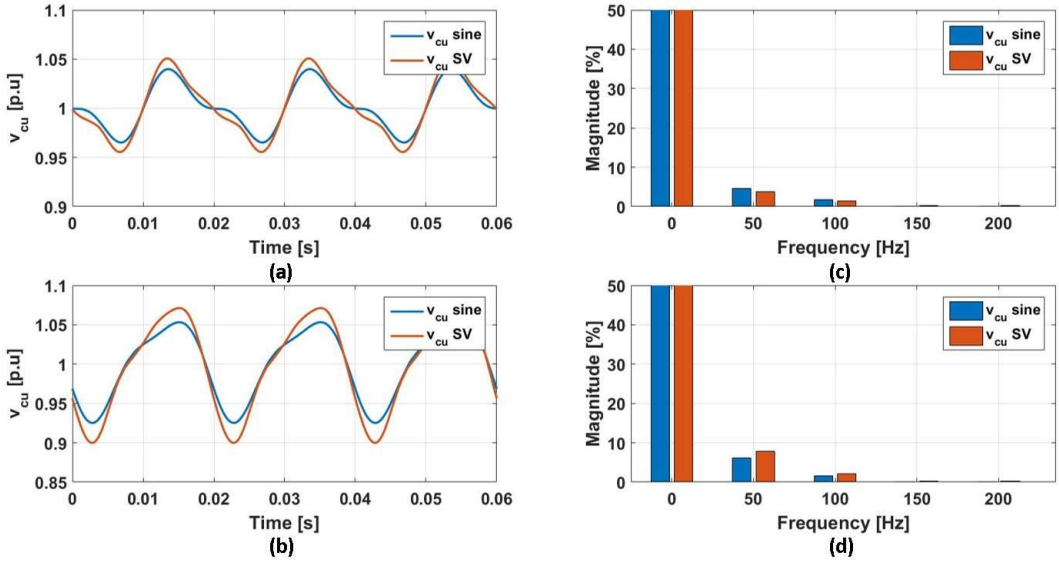

Figure 4.6: Comparison between SIN and SV: submodule capacitor voltage (a) Rectifier, (b) Inverter and (c) and (d) Correspondent harmonic spectrum

This appearance of the third and fourth order harmonics is a characteristic of the space vector modulation. This phenomenon can be explained from the following analysis, considering the explanation for the upper arm:

$$W_u = \frac{C}{2N} {v^{\Sigma}_{cu,l}}^2 \Longrightarrow v^{\Sigma}_{cu} = \sqrt{\frac{2N}{C} W_u} \tag{4.5}$$

now considering:

$$W_u = \frac{W_{\Sigma o} + \Delta W_{\Sigma} + \Delta W_{\Delta}}{2} \tag{4.6}$$

and the dc component to be:

$$W_{\Sigma o} = \frac{C v_d^2}{N} \tag{4.7}$$

yields,

$$v^{\Sigma}_{cu} = \sqrt{v_d^2 + \frac{N}{C}(\Delta W_{\Sigma} + \Delta W_{\Delta})} \tag{4.8}$$

Now considering the ripple to be much smaller then v_d

$$v^{\Sigma}_{cu} = v_d + \sqrt{\frac{N}{C}(\Delta W_{\Sigma} + \Delta W_{\Delta})} \approx v_d + \frac{N}{2C v_d}(\Delta W_{\Sigma} + \Delta W_{\Delta}) \tag{4.9}$$

It is now possible to relate the sum capacitor voltage per arm with the submodules' energy ripple. As previously mentioned in a space vector voltage reference the injection of third harmonic component will originate third and fourth order harmonics in the energy ripple. This relation is then obtained by including in **Equation (2.25)** and **Equation (2.26)** respectively the third harmonic component:

$$\Delta W_{\Sigma} = -\frac{\widehat{V}_s \widehat{I}_s}{4\omega_1} \sin(2\omega_1 t - \varphi) + \frac{1}{6}\frac{\widehat{V}_s \widehat{I}_s}{4\omega_1} \sin(2\omega_1 t + \varphi) + \frac{1}{6}\frac{\widehat{V}_s \widehat{I}_s}{8\omega_1} \sin(4\omega_1 t - \varphi) \tag{4.10}$$

$$\Delta W_{\Delta} = \frac{v_d \widehat{I}_s}{2\omega_1} \sin(\omega_1 t - \varphi) - \frac{2\widehat{V}_s i_c}{\omega_1} \sin(\omega_1 t) + \frac{1}{6}\frac{2\widehat{V}_s i_c}{3\omega_1} \sin(3\omega_1 t) \tag{4.11}$$

In **Figure 4.7**, it is possible to observe the circulating current with sinsusoidal and space vector voltage reference. As in the previous case **Section 4.2**, the reduction in the DC-Link voltage oscillations reduce the harmonic content when compared to a sinusoidal voltage reference.

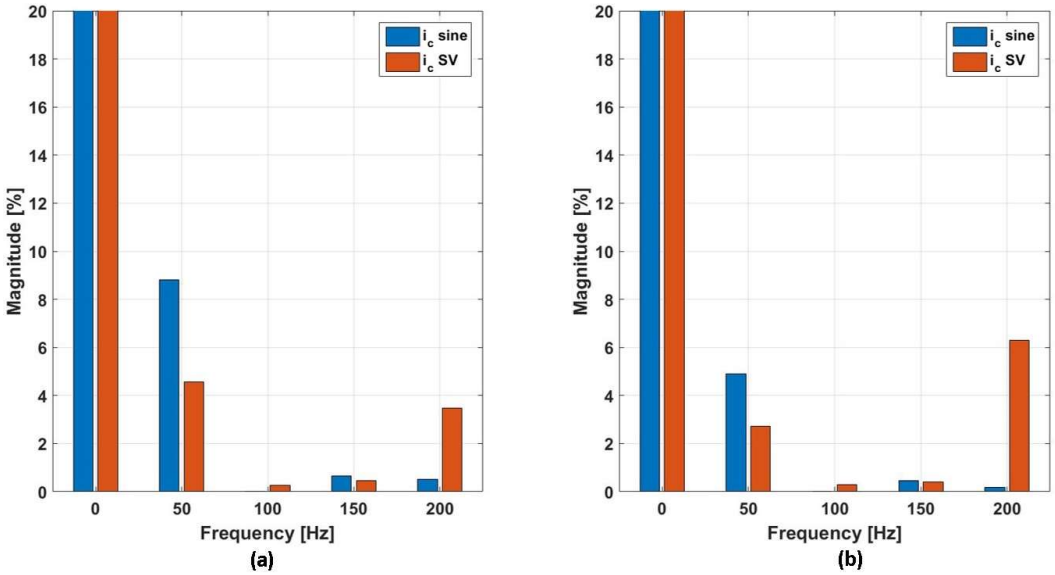

Figure 4.7: Comparison between sine and SV:(a) rectifier and (b) inverter

4.4 Undermodulation

The last proposed method to reduce the DC-Link ripple is to undermodulate the system. This can be obtained by increasing the DC-Link voltage reference as can be seen from **Equation (4.12)**

$$m = \frac{2\widehat{V}_s}{v_d} \tag{4.12}$$

The effect of the undermodulation is tested by comparing the system operating with a modulation index of m=1 and m=0.9 for a sinusoisal voltage reference. Under this conditions the rated energy for both these situations is $W_{rated} = 49kJ/MVA$ and $W_{rated} = 37kJ/MVA$ respectively as illustrated from figure **Figure 3.2**.

In **Figure 4.8**, a comparison between the DC-Link voltage for m=1 and m=0.9 can be observed. It is possible to observe the reduction in the ripple from 2.7% to 2% **Figure 4.8** (a). This reduction is caused by the reduction in the 50 Hz and 100 Hz components of the DC-Link voltage **Figure 4.8** (b).

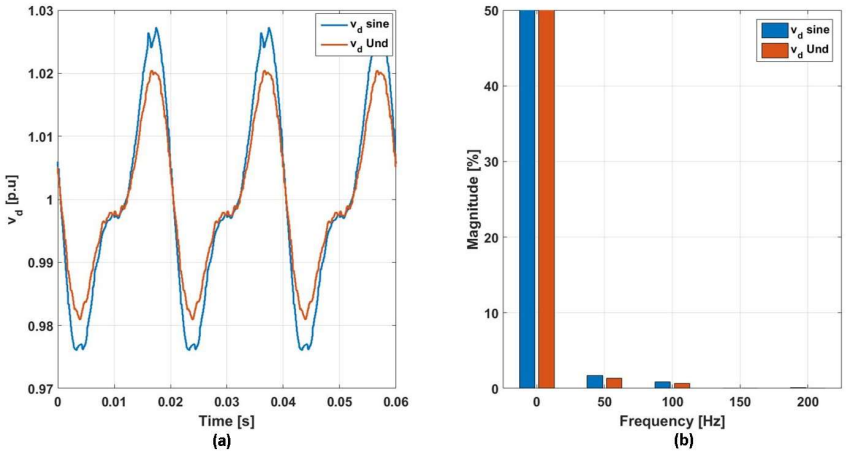

Figure 4.8: Comparison between modulation of m=1 and m=0.9:(a) dc-link voltage and (b) DC-Link voltage harmonic spectrum

On the other hand, **Figure 4.9** presents the effect of the undermodulation on the submodule capacitor voltages. It is observed that the sub-module capacitor voltage ripples increases, which is originated by the reduction in the rated energy that such modulation index requires, which subsequently reduces the size of the sub-module capacitor. Nevertheless, the requirement of a maximum of 10% ripple is still accomplished.

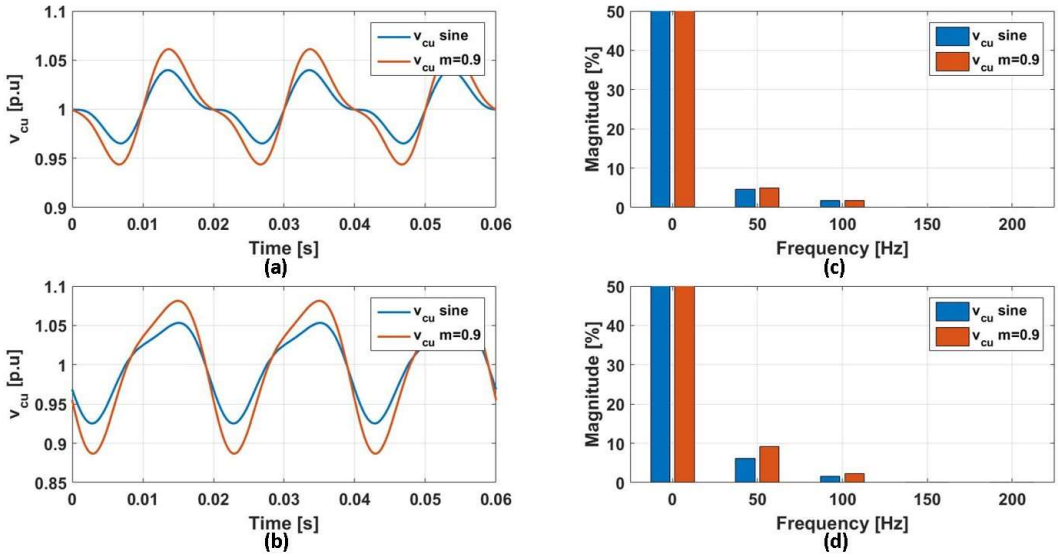

Figure 4.9: Comparison between modulation m=1 and m=0.9: sub-module capacitor voltage (a) rectifier, (b) inverter and correspondent harmonic spectrum (c) and (d)

In **Figure 4.10** the harmonic spectrum of the circulating current is presented for two modulation index of m=0.9 and m=1. In accordance with the previously stated that the circulating current harmonics decrease with the reduction in the DC-Link voltage ripples caused by the lower modulation index of m=0.9.

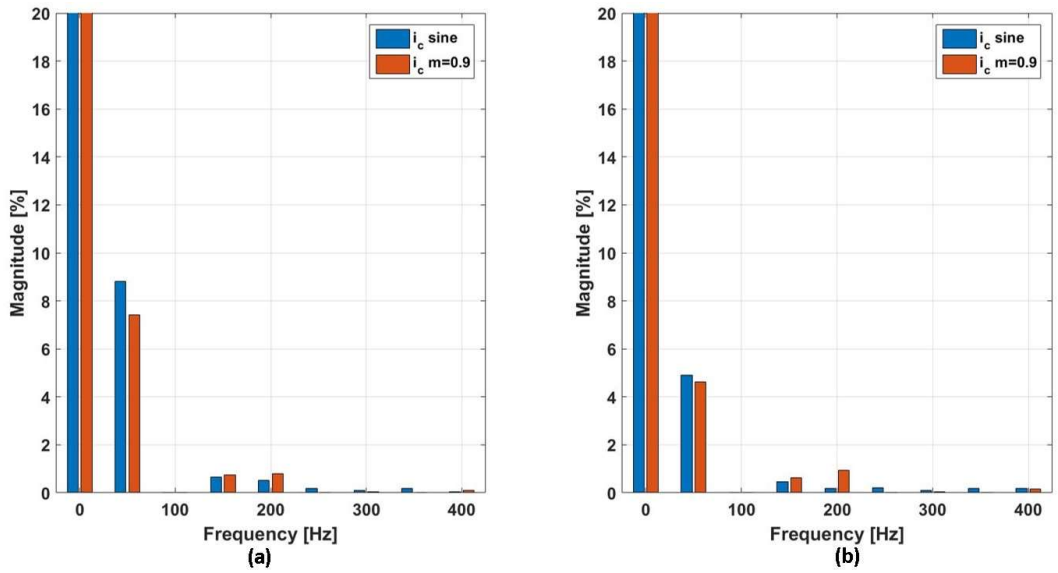

Figure 4.10: Circulating current harmonics comparison for m=1 and m=0.9:(a) rectifier and (b) inverter

4.5 Conclusion

As a short review, the three presented methods succeed to reduce the DC-bus ripple by a relevant margin. However, due to the different energy requirements, the submodule voltage ripples have increased in two of the methods. Despite that, the $\pm 10\%$ ripple is still guaranteed. Moreover, a reduction in the circulating current harmonics evincing the improvements in the system balancing was observed. Despite that, it was no major improvements in the sub-module capacitor voltage ripples.

In **Table 4.1** an overview of the different techniques with their pros and cons are presented.

Table 4.1: Overview of the three presented methods to reduce the DC-link ripple

Ripple reduction technique	**Vdc ripple reduction**	**Pros**	**Cons**
Space Vector	2.7% to 1.5%	inexpensive/ allows to increase voltage output	Need for supression of third harmonic components
DC-Link Capacitor	2.7% to 0.6%	Ripple reduction scalability	Expensive solution
Undermodulation	2.7% to 2%	Easy to implement	Overdimension of the system

From **Table 4.1**, it can be seen that the three methods help in reducing the DC-Link voltage ripple. However, the implementation of the DC-Link capacitor and the undermodulation incurs higher cost. While with C_d the cost arrises from the capacitor itself, with undermodulation the system has to be design for higher ratings. An increase in the number of submodules is expected increasing the overall cost. Spacevector is a more viable option among the three methods because it does not incur in higher costs of implementation and can also help in generating higher voltage output. In this project, since the DC-Link voltage ripples are within the defined limits of $\pm 5\%$. Therefore, there was no need to resort to any of the mentioned techniques.

Chapter 5

Power System Fault Condition Analysis

This chapter gives an introduction into the three-phase systems. In this chapter detailed analysis of the Back-2-Back MMC under fault conditions are done. The faults observed comprises of DC fault, grid side AC fault and internal faults in the MMC. The fault mitigation technique is also discussed in this chapter

5.1 Fault Analysis

The power system is designed to work under the rated conditions and accordingly the electrical equipments with the defined ratings are installed. The occurrence of faults in the power system induces the flow of massive current, which is higher than the rated current, through the electrical equipments. This causes severe damage to the system equipment, which further leads to the change of the equipment incurring more cost. It also leads to interruption of power supply. Therefore, the analysis of fault is an integral part of power systems because it helps to determine the causes that have led to the failure of the devices and the system. The analysis of the faults also helps to define the preventive measures in order to protect the system during such undesirable situations. The analysis of faults is instrumental in determining the normal operation safety measures and the protection system required by the system. However, the faults vary in the level of their severity. It depends on the location of the short-circuit, the impedance of the system, the fault current path and the operation system voltage. Short-circuits involving ground are more severe compared to their non-grounded counterparts. Therefore, in AC faults only faults involving ground are discussed.

5.1.1 Tripping Conditions

This is a very important component of the fault analysis in the power system. The power system tripping conditions should be designed as such that it should not only save the system equipment during fault condition but also avoid unnecessary shutdown of the system during transient-temporary fault conditions. The failure in the operation of the tripping system will lead to both time and financial losses. The sub-modules, semi-conductor devices and the inductor are all placed in the arm of the MMC. The arm currents of magnitude higher than the allowed level flowing through the circuit will cause severe damage on all the fundamental components of the MMC. Therefore, the tripping conditions for the system are based on the MMC arm currents. The tripping conditions used in this project are defined as follows:

- Overcurrent Protection : The overcurrent protection observes the arm currents in the MMC. It will trip the system if the arm currents are $\geq$ 1.5 p.u. over a period of 5 cycles.
- Instantaneous-Trip Protection : This protection also observes the arm currents in the MMC. It will generate tripping signals if the arm currents are $>$ 2p.u.

5.1.2 Choppers/ Braking Resistors

The choppers are important for back-to-back power conversion systems. During abnormal conditions, when the grid voltage drops, the energy stored in the arm capacitors increase, which leads to rise in the arm capacitor voltages, sometimes leading to the violation of the voltage limits. However, the chopper will help to dissipate the excess energy from the arm capacitors. The choppers can be either implemented in the DC-Link or in each sub-module. The implementation of the choppers in the DC-Link for MV and HV operations will require a connection of a number of series connected conventional braking choppers. This project discusses MV operations and the braking chopper must comprise of a number of series connected choppers in the form of diodes and energy dissipating resistors. The implementation of which is difficult to realise. In this project, the choppers are implemented in the half-bridge sub-modules of the MMCs. However, the use of average model **Section 2.2**, allows the possibility of representation of the choppers on each arm, which can be seen from **Figure 5.1**(a) [39].

The braking resistor R_{SM} in the chopper is designed to dissipate 1 p.u. power for a second as can be seen from **Equation (5.1)**.

$$R_{SM} = \frac{v_{cu,l}^2}{P} \tag{5.1}$$

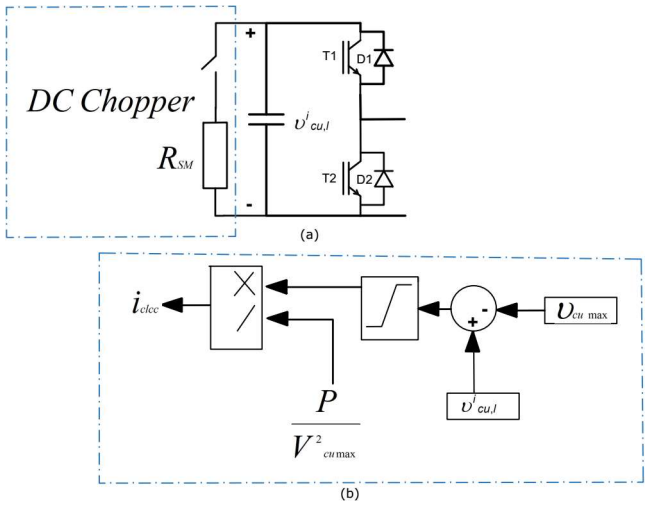

Figure 5.1: (a) Braking resistor in each sub-module configuration, (b) Equivalent representation of the braking resistor used

However, the project uses an equivalent model to represent the braking resistor as can be seen from **Figure 5.1**(b). The model is based on the working principle of the DC choppers to limit the increase of voltage on the sub-module capacitors. In this project, whenever the sub-module capacitor voltage is higher than the defined limits of 1.1 p.u. (v_{cumax}), current i_{clcc} will be injected from the CLCC, which is represented in **Figure 5.1**(b), into the sub-module capacitors. But this current will be in a direction opposite to the direction of the arm currents flowing through the sub-module capacitors. This will reduce the net current flowing through the capacitor and thereby limit the voltage at the sub-module capacitors to 1.1 p.u.

5.1.3 Single Line-to-Ground Fault

This is one of the most common fault seen in the power system. In this, one phase gets connected to the ground and establishes a low impedance path for the current. The schematic of the Single Line-to-Ground can be seen from **Figure 5.2**.

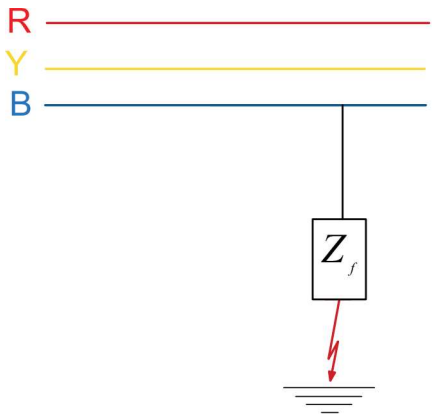

Figure 5.2: Single-Phase to Ground fault

Since, it is an unsymmetrical fault, thus the analysis of the unbalanced power system is done with the use of symmetrical components. The Three-phase circuit under fault condition is shown in **Figure 5.3**. The parameters of the circuit have been obtained from **Chapter 3 Dimension and Control of MMC**. The fault fault between the phase and the ground is considered as 0.16 p.u.[36]. The three-phase power system describing symmetrical and unsymmetrical faults have been profoundly explained in **Appendix A 1**.

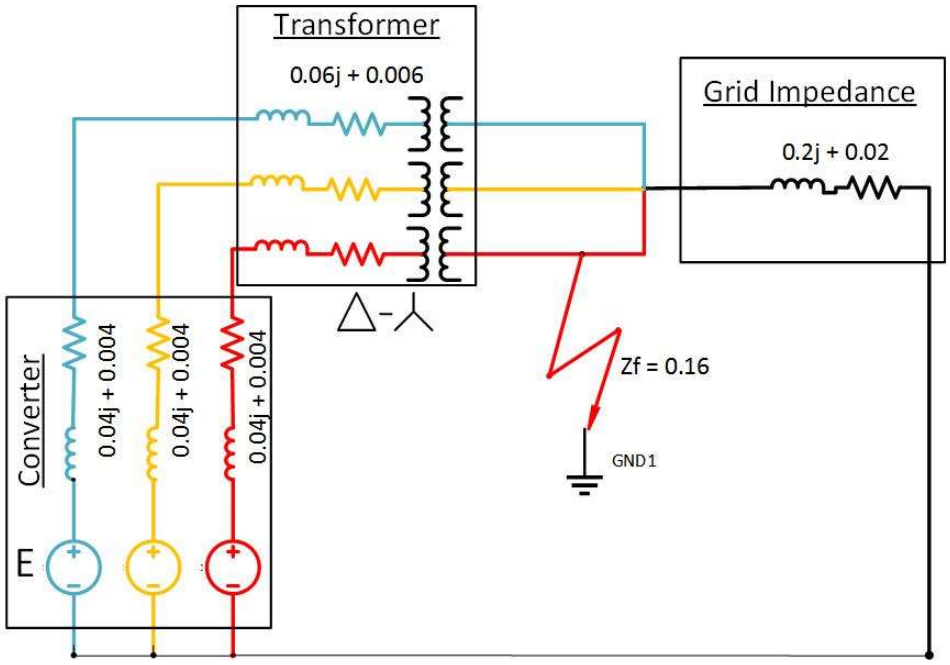

Figure 5.3: Detailed representation of single-Phase to Ground fault

Transforming the three-phase system into a single line diagram makes the analysis easier. Thus, the single line diagram for the system can be seen from **Figure 5.4**.

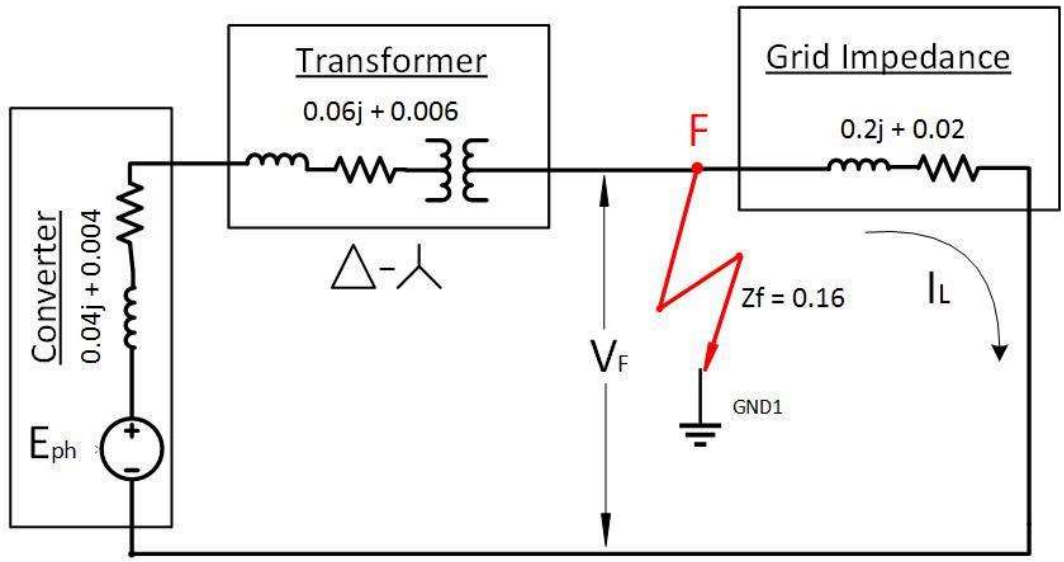

Figure 5.4: Single line diagram of single-Phase to Ground fault

The prefault line rms voltage at the converter terminal is considered to be $1\underline{/0^\circ}$ p.u. A 10% voltage drop across the phase reactors and the transformer together with 6.5 Mvar lagging reactive power will account for 0.86 p.u. voltage at the fault point. Therefore V_F is $0.86\underline{/0^\circ}$ p.u. The impedance on looking in at point F in **Figure 5.4** is 0.01+j0.1 p.u. on the left of point 'F' in parallel with 0.02+j0.2 p.u. Thus the positive and negative sequence impedance (Z^+ and Z^-, respectively) can be calculated using the **Equation (5.2)**.

$$\begin{aligned} Z^+ \; AND \; Z^- &= \frac{(0.01 + j0.1) \times (0.02 + j0.2)}{(0.01 + j0.1) + (0.02 + j0.2)} \\ &= 0.0067 + j0.067 = 0.067\underline{/84.29^\circ} \end{aligned} \tag{5.2}$$

The Z^+ and Z^-derived in **Equation (5.2)** is the impedance to the flow of both positive and negative sequence currents respectively. However, it is not the same for zero sequence impedance. The zero sequence impedance encounters an open circuit to the left of the transformer. Since the star side of the transformer is grounded, thus the zero sequence impedance can be seen in **Figure 5.5**.

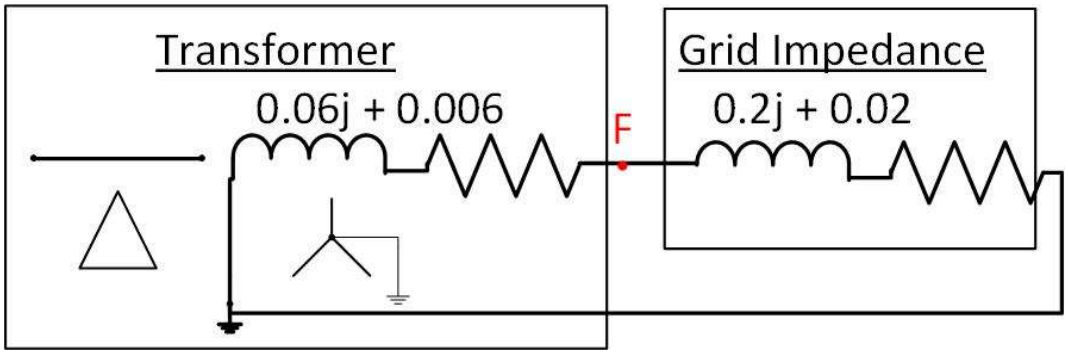

Figure 5.5: Zero sequence impedance

Therefore, the zero sequence impedance comprises of the parallel connection of the grid impedance and the transformer impedance. This can be obtained using the **Equation (5.3)**

$$\begin{aligned} Z^0 &= \frac{(0.006 + j0.06) \times (0.02 + j0.2)}{(0.006 + j0.06) + (0.02 + j0.2)} \\ &= 0.0464\underline{/84.29^\circ} = 0.00462 + j0.0462 \end{aligned} \tag{5.3}$$

The fault impedance(Z_F) is 0.165 p.u. An impedance of $3Z_F$ is in series with the positive, negative and zero sequence impedances. The over all circuit in terms of symmetrical components is given by **Figure 5.6**.

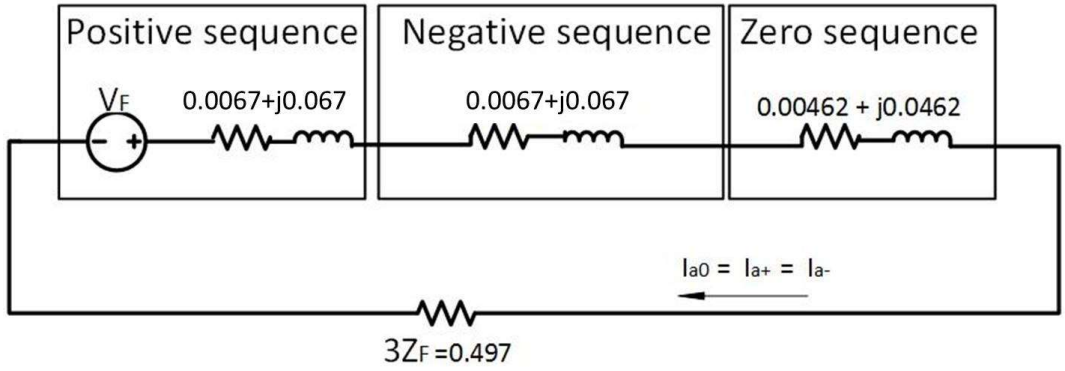

Figure 5.6: Sequence network for Single-line to Ground fault

The total impedance of the sequence network is given by **Equation (5.4)**.

$$\begin{aligned} Z^t &= Z^0 + Z^+ + Z^- + 3Z_F \\ &= 0.0067 + j0.067 + 0.0067 + j0.067 + 0.00462 + j0.0462 + 0.497 \\ &= 0.5456\underline{/19.22^\circ} \\ &= 0.52 + j0.18 \end{aligned} \tag{5.4}$$

The positive, negative and zero sequence current flowing through the circuit is given by **Equation (5.5)**.

$$\begin{aligned} I_a^0 = I_a^+ = I_a^- = \frac{V_F}{Z_t} &= \frac{0.86\underline{/0^\circ}}{(0.52 + j0.18)} \\ &= 1.478 - j0.511 = 1.56\underline{/-19.09^\circ} \end{aligned} \tag{5.5}$$

The fault current flowing in the circuit is defined in equation 5.6

$$\begin{aligned} I_f &= 3 \times I_a^+ = \frac{3 \times \sqrt{2} \times 0.95\underline{/-19.22^\circ}}{\sqrt{3}} \\ I_f &= 3.82\underline{/-19.09^\circ} \end{aligned} \tag{5.6}$$

The fault current output of the simulation can be see from **Figure 5.7**. The simulated value of the fault current is 3.88 p.u. and that corresponds to 3.82 p.u., which is the same as obtained from the theoretical calculation provided in **Equation (5.6)**.

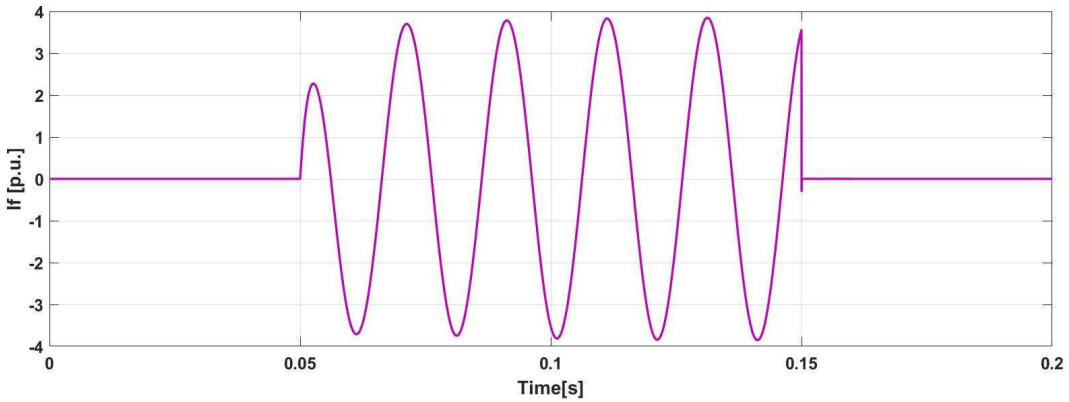

Figure 5.7: Fault current for Single-line to Ground fault

Figure 5.8 shows the variation in v_d, i_d, v_s and i_s for both rectifier and inverter. It can be clearly seen that the fault in the inverter side does not have any significant impact on the rectifier side AC voltage and current and they remain almost at their nominal values. However, the AC voltage v_s, in the inverter changes, with the faulted phase having only 0.31 p.u peak phase voltage and the other two phases have 0.725 and 0.79 p.u. respectively. The inverter side AC current i_s, which is

controlled by the output current controller defined in **Section 2.5.3**, reaches a maximum value of 1.43 p.u. during the fault duration from 0.1s to 0.2s. The DC-Link voltage has 2% ripple and is well within the voltage violation limit of $\pm 5\%$. The power input in the DC side from the rectifier and the inverter power output can be seen from **Figure 5.9**

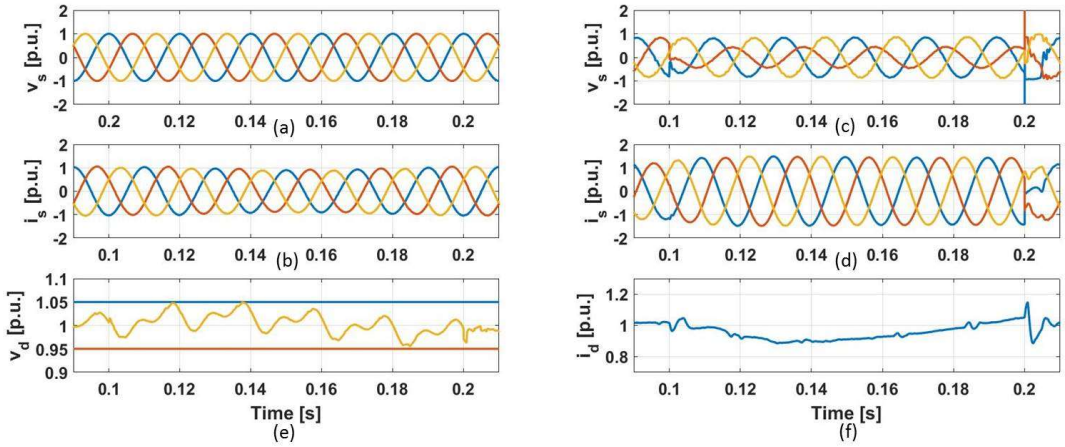

Figure 5.8: (a) Rectifier ac voltage, (b) Rectifier ac current, (c) Inverter ac voltage, (d) Inverter ac current, (e) DC-Link voltage and (f) Dc-Link current for the fault duration duration from 0.1 s to 0.2s

The power input in the DC side from the rectifier and the inverter power output can be seen from **Figure 5.9**. During the faulted condition, the power output from the MMC decreases slightly until 0.9 p.u. and then regains steady state operation within 0.3 seconds after the clearance of the fault. This is because the active power reference generated by the output voltage controller defined in **Section 2.5.1** is a function of the difference between v_{dref} and v_d. During fault on the inverter side, the inverter AC current i_s will increase. The increase in the inverter current will increase the inverter arm currents **Equation (2.4)**. The increase in the arm currents will lead to increased energy stored in the capacitors **Equation (2.17)**. This will increase the voltage in the sub-module capacitors above 1 p.u. This phenomena will also be reflected in the DC-Link voltage, which will cause the DC-Link voltage to increase above 1 p.u. However, the PI controller in the output voltage control will try to maintain v_d at 1 p.u. The PI controller will try to maintain v_d at 1 p.u. However, in the process to maintain v_d at 1 p.u., the dynamics of the PI controller will decrease v_d to even lower values for a few milli-seconds before reaching its steady state value.. Since P_D is a function of the difference between v_{dref} and v_d. Therefore, with the decrease in v_d, P_D will also decrease.

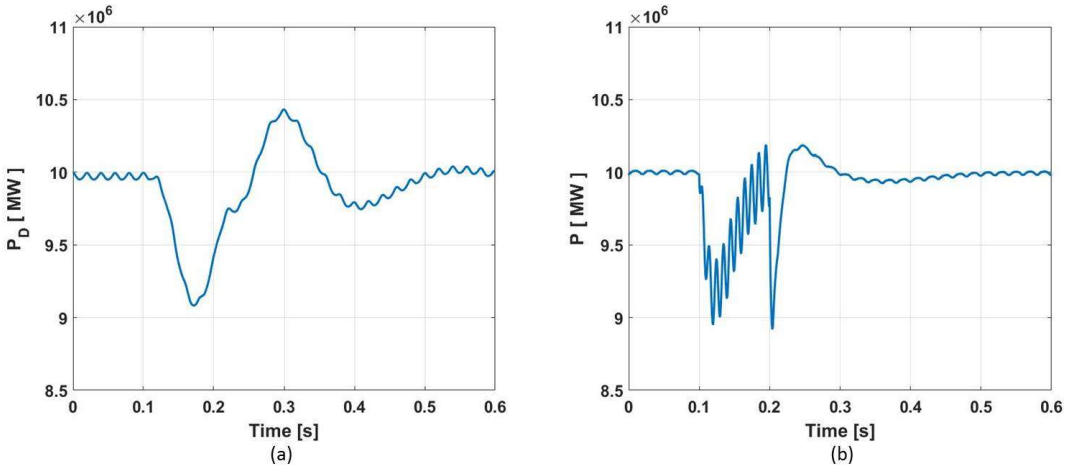

Figure 5.9: (a) DC side input Power and (b) Inverter active power output for the fault duration duration from 0.1 s to 0.2s

Figure 5.10 shows the variation in v_{cu} and i_{cu} for both rectifier and inverter. The rectifier side i_{cu} and v_{cu} is not affected much from the AC fault in the side of the inverter because of the presence of the DC-Link voltage controller installed in the rectifier, which is explained in detail in **Section 2.5.1** in **Chapter 2 Dynamics and Control of MMC**. As explained in the previous paragraph, the controller continuously tracks the DC-Link voltage and generates the power refrence for the rectifier. Thus, when the DC-Link voltage reduces, The power reference generated will be lower than 1 p.u. This will reduce the rectifier arm currents below 1 p.u. With the relation obtained between the DC-Link voltage and arm capacitor voltages obtained in **Section 2.1**, the rectifier sub-module voltages also reduces as a response to the reduction in the DC-Link voltage.

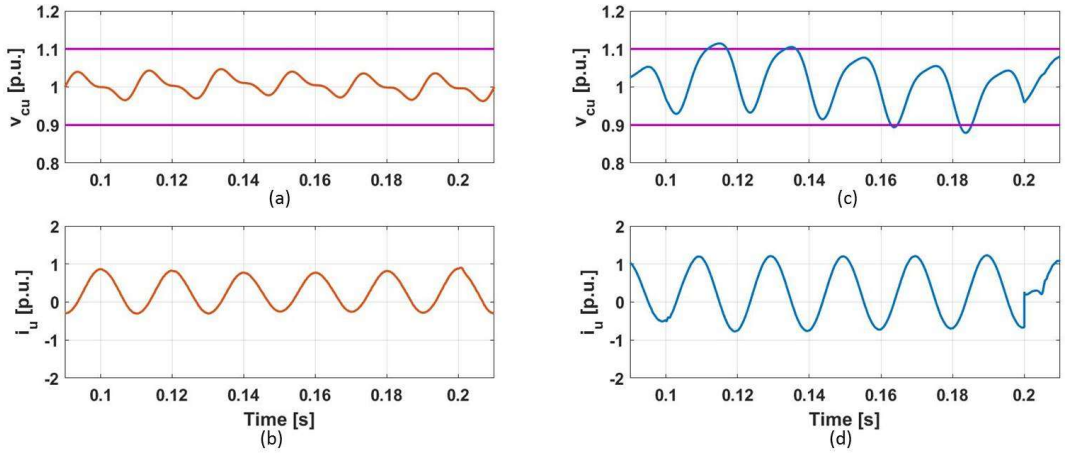

Figure 5.10: (a) Rectifier upper arm voltage, (b) Rectifier upper arm current, (c) Inverter upper arm voltage, (d) Inverter upper arm current for the fault duration duration from 0.1 s to 0.2s

However, it can be seen that i_{cu} in the side of the inverter has higher peaks of 1.46 p.u. which is very close to the tripping conditions, which are defined in **Section 5.1.1** that states, for tripping i_{cu} must be $>$ 1.5 p.u. over a period of 5 cycles. It can be seen that v_{cu} in the side of the inverter is slightly above 1.1 p.u. for an instant of time between 0.1s and 0.2s. Choppers are used to chop-off this extra voltage from the arm capacitor voltages, thereby limiting the arm capacitor voltages to 1.1 p.u. This effect can be observed in **Section 5.1.3.2**. The working of the choppers is explained in **Section 5.1.2**.

5.1.3.1 Benefits of using capacitance during fault conditions

As discussed in **Section 4.2** in **Chapter 4 DC-Link Ripple Analysis** that the use of capacitor will help to reduce the ripples in the DC-Link voltage. The DC-Link capacitor is able to reduce the ripple in the DC-Link voltage even during the fault condition as can be seen from **Figure 5.11**.

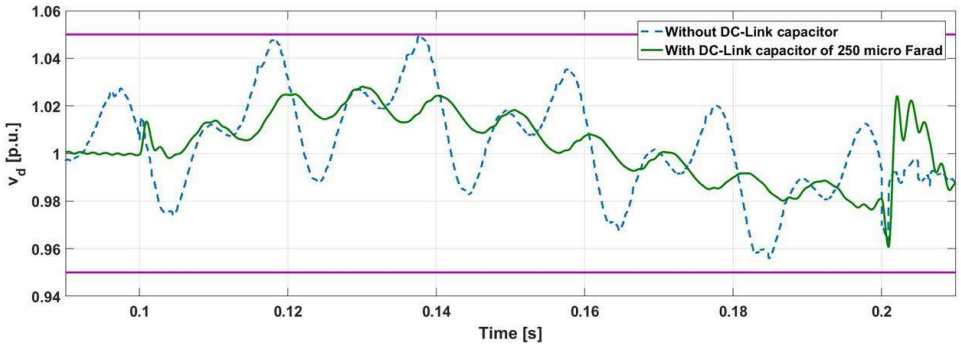

Figure 5.11: The effect of DC-Link capacitor on Vdc

5.1.3.2 Benefits of using DC Choppers

The choppers will help to reduce the excess energy accumulation in the arm capacitors as described in **Section 5.1.2**. Therefore, the implementation of the choppers in the system will help to limit the arm sub-module capacitors' voltage to 1.1 p.u. during SLG. This effect can be seen from **Figure 5.12**, where during the SLG fault condition, the arm capacitor voltages are above 1.1 p.u between the time interval of 0.11s and 0.15s. But with the implementation of the DC choppers, the arm capacitor voltages are restricted to 1.1 p.u. This will reduce the level of voltage stress on the sub-modules. The unabated energy deposition into the capacitors during fault conditions will finally lead to the severe damage of the capacitors. This will have detrimental effect on the performance and financial aspects of the system. This effect is more clearly visible during Double Line-to-Ground fault and Triple Line-to-Ground described in **Section 5.1.4** and **Section 5.1.5** respectively.

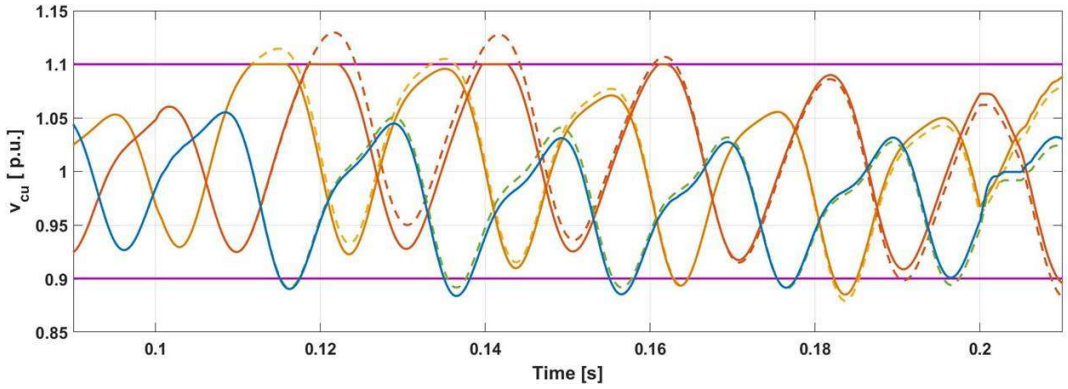

Figure 5.12: The effect of DC choppers during Single Line-to-Ground fault, the 'solid (–)' signals represent the arm voltages with the DC choppers and the ' dashed (- -) ' signals represent the arm voltages without DC choppers.

5.1.4 Double Line to Ground Fault

This is a severe type of unsymmetrical fault. In this type of fault, two phases are involved in the fault with the ground. The fault occurs by the short-circuit between the phases and the ground as can be seen from **Figure 5.13**. The fault impedance between the phases and the ground is considered as 0.16 p.u. The short-circuit between the two lines causes high current to flow through the lines and into the ground.

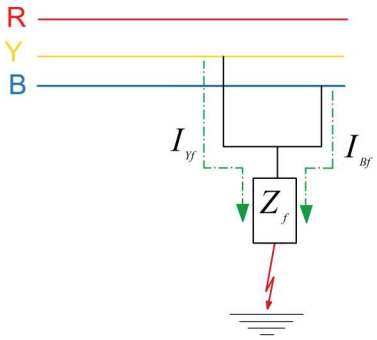

Figure 5.13: Line-to-Line ground fault for fault condition from 0.1 s to 0.2s

During fault condition, the inverter AC currents and the inverter arm currents can increase until 6.28 p.u, unless the system is blocked or isolated. The rectifier side grid voltage does not vary much because it is connected to a strong grid. The rectifier arm currents decrease because of the output voltage controller. The principle of the output voltage controller **Section 2.5.1** and its effect on the rectifier during fault conditions is explained in the case of SLG in **Section 5.1.3**. This limits the AC input current in the rectifier. This can be seen from **Figure 5.14**.

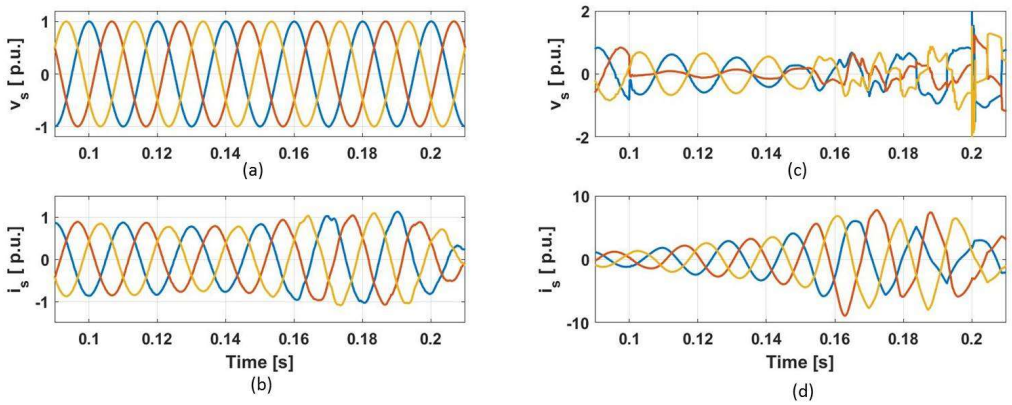

Figure 5.14: (a) Rectifier side AC voltage, (b) Rectifier side AC current, (c) Inverter side AC voltage, (d) Inverter side AC current during the Line-to-Line ground fault for fault duration from 0.1 s to 0.2s

Figure 5.15 shows the variation in $v_{cu,l}$ and $i_{u,l}$ for both rectifier and inverter. It can be seen that the inverter arm capacitor voltages will have higher voltage fluctuations and violate the 1.1 p.u. voltage limit. However, the problem of over-voltage on the arm capacitors is limited to 1.1 p.u. by the use of DC- choppers and the results can be seen in **Section 5.1.4.1**.The effect of the fault on the side of the inverter does not effect the rectifier side arm currents as already stated earlier in **Section 5.1.3**.

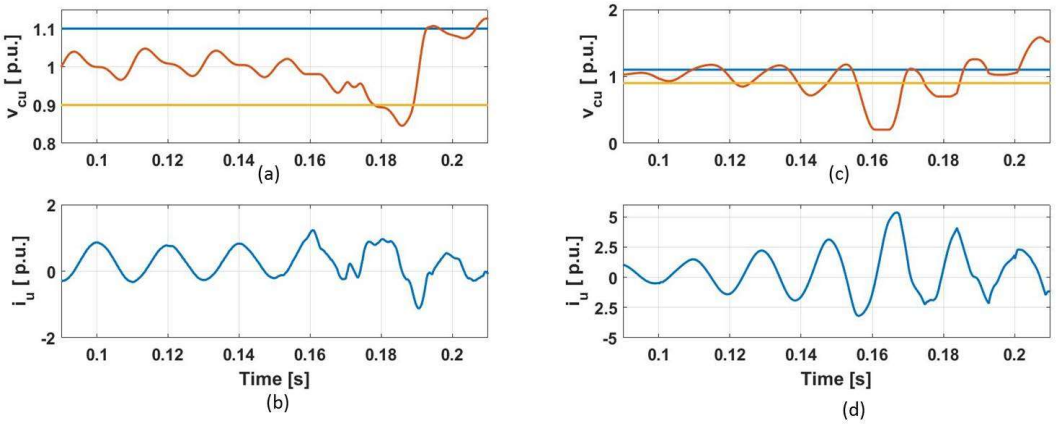

Figure 5.15: (a) Rectifier side sub-modules voltage, (b) Rectifier side arm current, (c) Inverter side sub-modules voltage, (d) Inverter side arm current during the Line-to-Line ground fault for fault condition from 0.1s to 0.2s

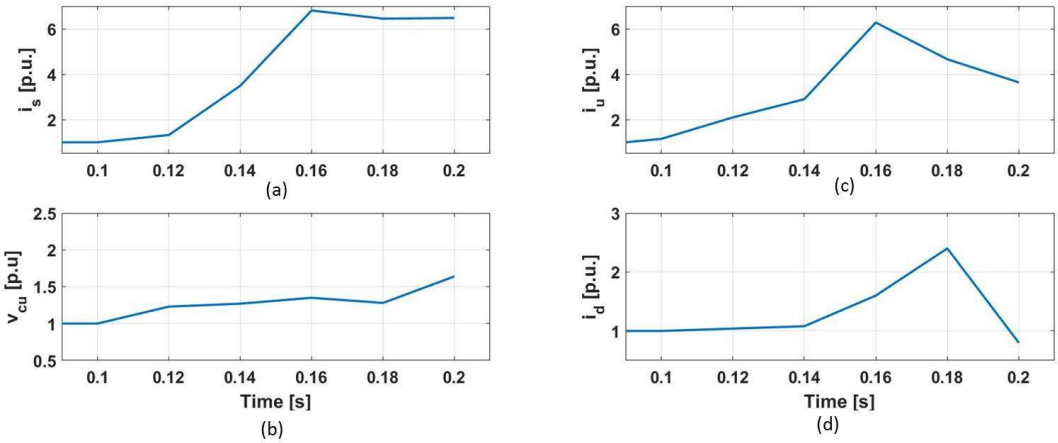

Figure 5.16: (a) Inverter AC currents, (b) Inverter arm currents, (c) Inverter upper arm capacitor voltages, (d) The DC-Link current

The stress levels on the arm components, DC-Link and the AC network components can be seen from **Figure 5.16**. From the analysis, it is evident that the

protection system will detect the fault because $i_{u,l}$ and i_s increases to 6.28 $\times$ rated value and violates the tripping conditions. Thus, the protection system will generate an *instantaneous blocking* signal. which will block the converters and the AC circuit breakers will isolate the system after a delay time of 0.1s from the time of fault detection, thereby protecting the system from encountering further damages. The results can be seen in **Section 5.1.4.1**.

5.1.4.1 Preventive measures taken during LLG fault

When the current flowing through the arms increase above the tripping limits defined for the arm currents, the system will get blocked and the AC circuit breaker will isolate the faulted grid from the back-to-back MMC. But, this will lead to energy accumulation in the inverter because of the continuous flow of power from the rectifier, which will inflict further damage on the inverter components. Therefore, during a fault in the inverter side, the rectifier should also be isolated from its corresponding grid.

However, the AC breakers are considered to isolate the system after a delay 0.1s from the time of fault detection. [40]. Therefore, during this interval of 0.1s, the rectifier and the inverter are both blocked, which means that all the switches are open and the only conduction path is through the diodes, which cannot be controlled. However in this case, since the diode $D2$ **Figure 2.1** is reverse biased, thus there is no current flowing in the sub-modules of the rectifier and the inverter. The moment, the back-to-back MMC is blocked, the capacitor in the submodules in the rectifier will retain its nominal voltage and diode $D1$ in rectifier will never turn on during this condition. Thus, the rectifier side grid will not be able to feed the fault. In the inverter, the capacitors are isolated, thus it will maintain its nominal voltage and diode D_1 will always be reverse biased. Since the inverter AC side voltage is lower than the DC-Link voltage, so the diode D_2 will also be reverse biased. Thus, it can be concluded that during an AC fault, when the system is blocked, the current stops flowing in the back-to-back MMC because the diode rectifier cannot work like an inverter.

The DC choppers implemented in the sub-modules help to limit the arm capacitor voltages within 1.1 p.u. The results of this protection scheme can be seen from **Figure 5.17**. The system detects that the inverter arm current exceeds 2 p.u. at t=0.125s and the fault detection signal is generated at the same instant. The system will be blocked at the same instant i.e. at t=0.125s, but the tripping will occur at t=0.225, which is a delay of 0.1s as has been mentioned earlier. Thus, the system is isolated from the fault. As can be seen from **Figure 5.17**(b) that after t=0.125s, current stops flowing through the arms. **Figure 5.17**(f) shows that the inverter diodes $D1$ and D_2 are always turned off and no current flows through the

inverter arms. The DC choppers effectively chops-off v_{cu} and limits it to 1.1 p.u. Then at t=0.225s, the AC breakers on both sides on the back-to-back MMC trips, isolating the system.

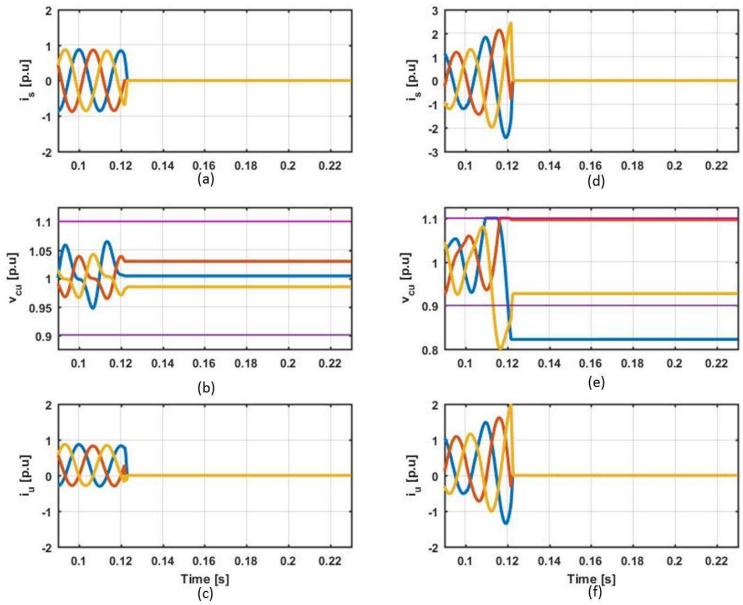

Figure 5.17: (a) Rectifier AC current, (b) Rectifier arm capacitor voltage, (c) Rectifier arm currents, (d) Inverter AC current, (e) Inverter arm capacitor voltage, (f) Inverter arm currents.

5.1.5 Three Phase to Ground Fault

This is a symmetrical fault and is one of the most severe type of fault in the AC power system. Thus an analysis of this is highly required to verify that the ratings of the circuit breakers are adequate enough to interrupt the fault current. **Figure 5.18** shows the variation in i_s, i_u and v_{cu} during the duration of the three-phase fault. It can be seen that i_s in the side of the inverter can increase to 12.01 p.u. This increase in inverter AC current will increase the inverter arm currents to 9.07 p.u., which will activate the instantaneous blocking of the system and the system will be blocked as described in **Section 5.1.1** and the AC breakers will isolate the system with a delay of 0.1s. The arm voltages in the inverter are also above 1.1 p.u. However, with the help of DC choppers as described in **Section 5.1.2**, it will be restricted to 1.1 p.u. The rectifier side AC current and arm currents decreases during the fault because the power transferred from the rectifier is reduced by the output voltage controller, whose working principle is defined in **Section 2.5.1** in **Chapter 2 Dynamics and Control of MMC**.

The level of stress as a function of time, experienced by the arm components

and the AC side components can be seen from **Figure 5.19**. This three-phase fault will cause huge stress on the components of the power system. **Figure 5.19**, if the system doesn't trip.

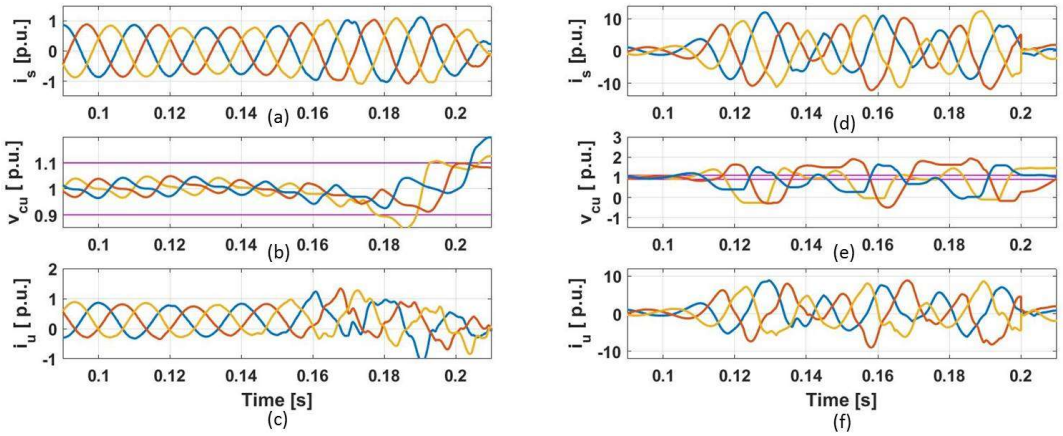

Figure 5.18: (a) Rectifier AC current, (b) Rectifier arm current, (c) Rectifier arm capacitor voltages, (d) Inverter AC current, (e) Inverter arm current and (f) Rectifier arm capacitor voltages, during the three phase ground fault condition from 0.1s to 0.2s

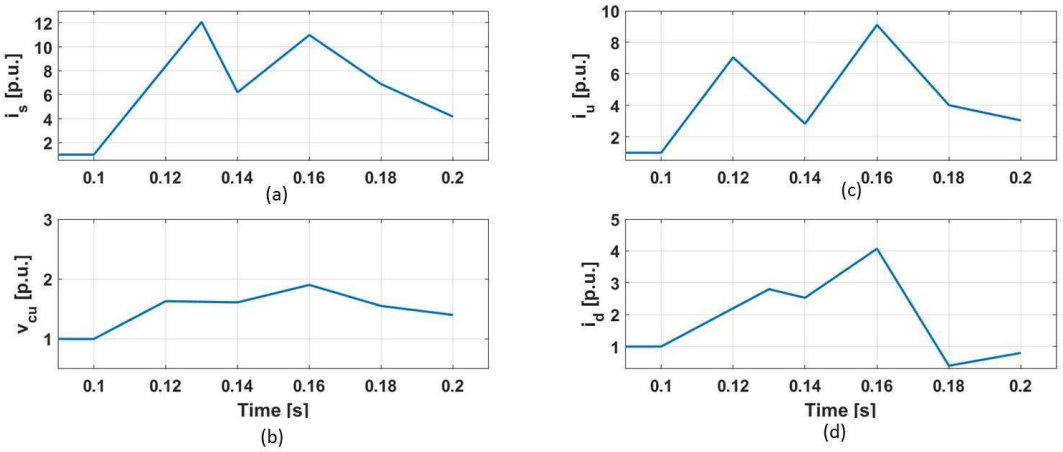

Figure 5.19: (a) Inverter AC currents, (b) Inverter arm currents, (c) Inverter upper arm capacitor voltages, (d) The DC-Link current during the three phase ground fault condition from 0.1s to 0.2s

5.1.5.1 Protection Scheme

As can be seen from **Figure 5.19** that the arm current rise above 2 p.u. within 0.002s, thus the instantaneous trip signal will be generated by te system. The protection system will work in the similar way as describe in **Section 5.1.4.1**. It will first block the system and then the AC breakers will isolate the system after a delay of 0.1s.

As explained in **Section 5.1.4.1**, that the arm currents will stop flowing through the arms and the sub-module capacitors will maintain its nominal voltage. This effect can be seen from **Figure 5.20**.

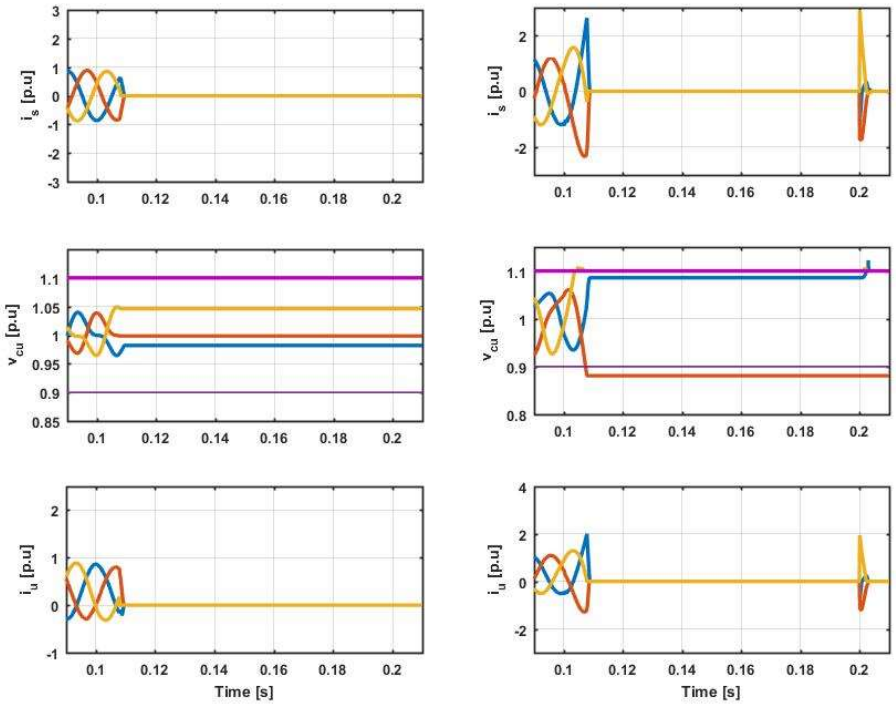

Figure 5.20: (a) Rectifier AC currents, (b) Rectifier upper arm capacitor voltages, (c) Rectifier upper arm currents, (d) Inverter AC currents, (e) Inverter upper arm capacitor voltages, (f) Inverterer upper arm currents fault condition from 0.1s to 0.2s

5.2 DC Fault in the Power System

5.2.1 Analysis of the power system before blocking caused due to pole-to-pole fault

This fault occurs on the DC-Link. When the fault occurs, then both the converter stations inject high current into the system. The bridge current is comprised of the current flowing through the capacitor of the switched-on sub-module that discharges through the upper switch T_1. The unstoppable rectifier action of the diode bridge will also allow current to flow into the DC fault through the switched-off sub module's diode D_2. Pole to pole fault resembles an AC three-phase short-circuit. After few milliseconds, though the sub-module capacitors stop discharging but the AC grid continues to inject current into the fault as can be seen from **Figure 5.21**. The representation can be further simplified to **Figure 5.23**[41].

The RLC circuit can be represented using the **Equation (5.7)**.

$$\begin{aligned} V(t) &= V_R + V_L + V_C \\ &= RI(t) + L\frac{dI}{dt} + \frac{1}{C} \end{aligned} \tag{5.7}$$

The **Equation (5.8)** is obtained by differentiating **Equation (5.7)** with respect to't'.

$$\begin{aligned} \frac{d^2}{dt^2}I(t) + \frac{R}{L}\frac{d}{dt}I(t) + \frac{1}{LC}I(t) &= 0 \\ s^2 + 2\alpha s + w_0^2 &= 0 \end{aligned} \tag{5.8}$$

The roots of the **Equation (5.8)** is defined in **Equation (5.9)**

$$\begin{aligned} s_1 &= -\alpha + \sqrt{\alpha^2 - w_0^2} \\ s_2 &= -\alpha - \sqrt{\alpha^2 - w_0^2} \end{aligned} \tag{5.9}$$

where, A_1 and A_2 define the boundary conditions. The capacitor voltage is defined in **Equation (5.10)**.

$$v_c = A_1 e^{s_1 t} + A_2 e^{s_2 t} \tag{5.10}$$

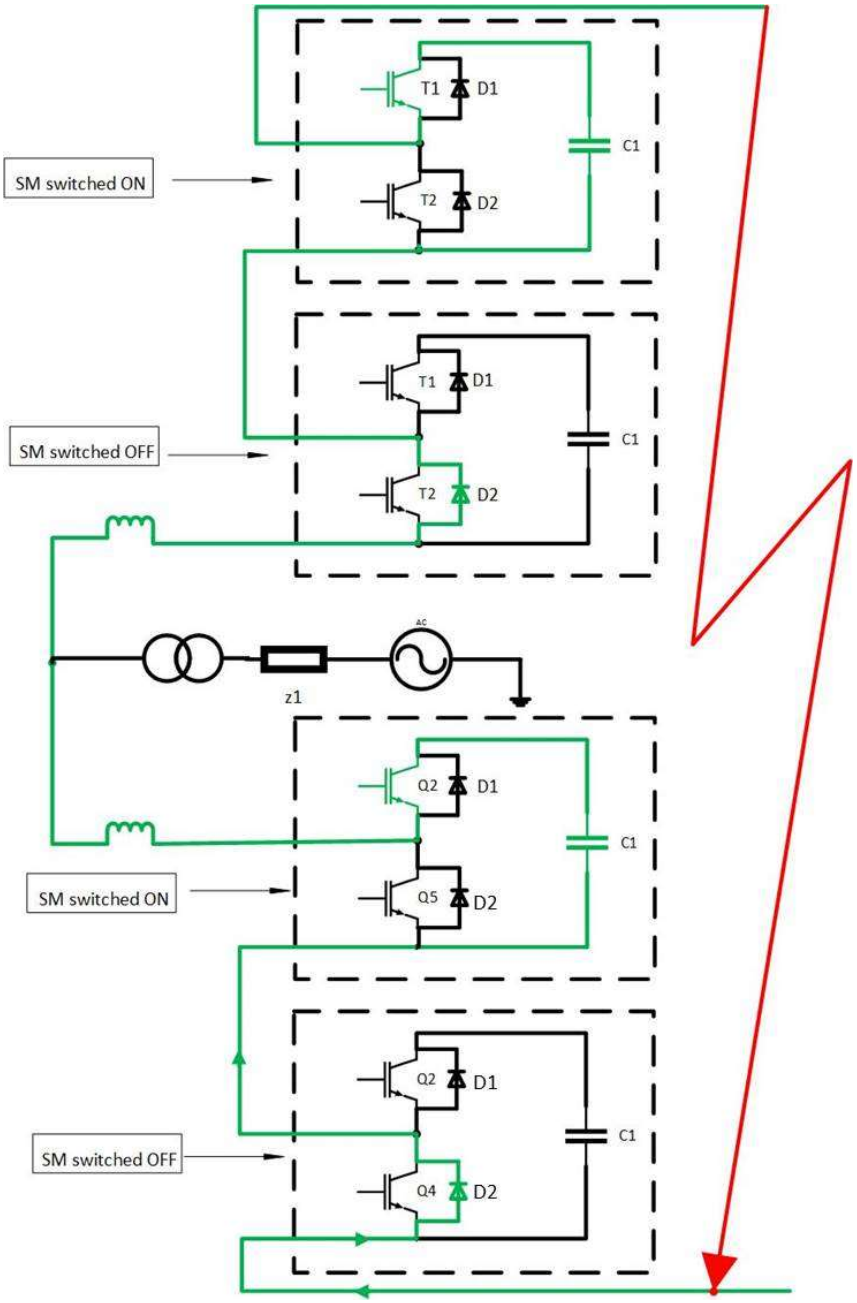

Figure 5.21: The fault current path during DC-Link fault (Pole-to-Pole)

The original states of v_c and i_c are defined in **Equation (5.11)**.

$$\begin{aligned} v_c(0+) &= v_c(0-) = V_{dc} \\ i_c(0+) &= i_c(0-) = -c_{eq}\frac{dv_c}{dt} = I_0 \end{aligned} \tag{5.11}$$

The values of A_1 and A_2 are defined in **Equation (5.12)**.

$$\begin{aligned} v_c(0+) &= A_1 \\ \frac{dv_c(0+)}{dt} &= \frac{-A_1}{\tau} + \omega A_2 \\ A_1 &= V_{dc} \\ A_2 &= \frac{V_{dc}}{\tau\omega} - \frac{I_0}{\omega C_{eq}} \end{aligned} \tag{5.12}$$

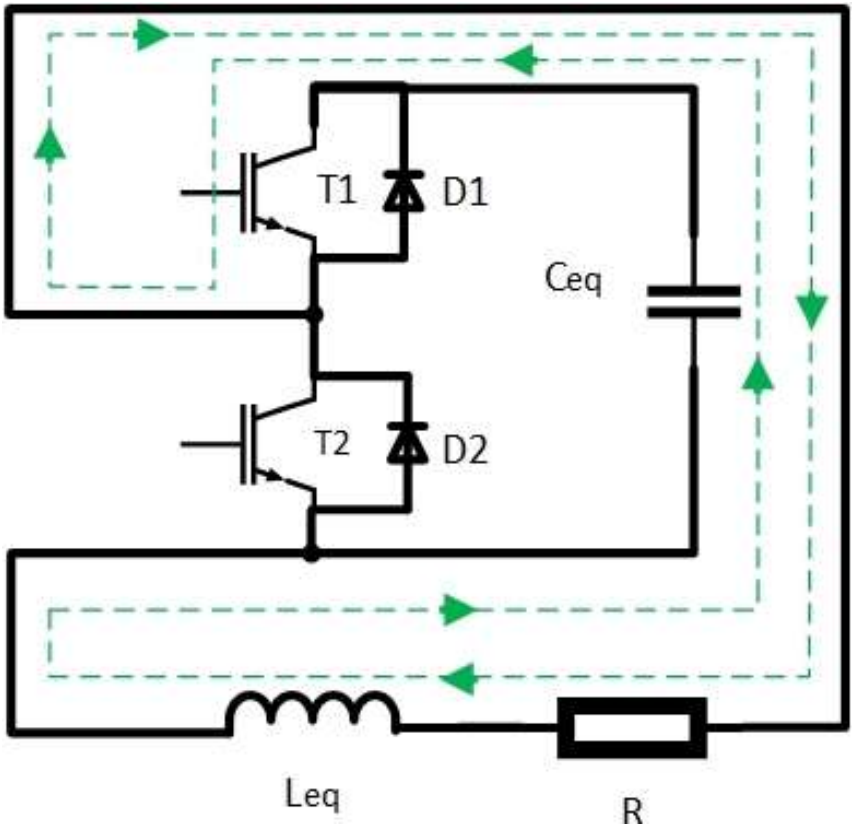

Figure 5.22: The equivalent diagram of MMC during DC-Link fault (Pole-to-Pole)

However, since the system is an underdamped system, therefore the capacitor voltage takes the form described in **Equation (5.13)**

$$v_c = e^{\frac{-t}{\tau}}(A_1 cos\omega t + A_2 sin\omega t) \tag{5.13}$$

Substituting the value of A_1 and A_2 defined in **Equation (5.12)** in **Equation (5.13)**, we get

$$v_c = e^{\frac{-t}{\tau}}\left[v_{dc} cos\omega t + \frac{v_{dc}}{\tau\omega} sin\omega t - \frac{I_0}{\omega C_{eq}} sin\omega t\right] \tag{5.14}$$

The parameters are defined in **Equation (5.15)**

$$\begin{aligned} \tau &= \frac{2L_{eq}}{R} \\ \omega_0 &= \sqrt{\frac{1}{L_{eq}C_{eq}}} \\ \omega &= \sqrt{\frac{1}{L_{eq}C_{eq}} - (\frac{R}{2L_{eq}}^2)} \\ tan(\theta) &= \omega\tau \\ \omega &= \sqrt{(\omega_0)^2 - \frac{1}{(\tau)}^2} \\ sin(\theta) &= \frac{\omega}{\omega_0} \\ cos(\theta) &= \frac{1}{\tau\omega} \\ sin(\theta + \omega t) &= sin(\theta).cos(\omega t) + cos(\theta).sin(\omega t) \end{aligned} \tag{5.15}$$

Multiplying and dividing **Equation (5.14)** by ω_0 and substituting the values of sinθ and cosθ obtained from **Equation (5.15)**, we get

$$\begin{aligned} v_c &= e^{\frac{-t}{\tau}}\Big[\frac{v_{dc}\,\omega_0\,\tau\,sin(\theta)\,cos(\omega t)}{\tau\,\omega} + \frac{(\omega_0\tau)v_{dc}}{\tau\omega \times (\omega_0\tau)}sin(\omega t) - \frac{I_0}{\omega C_{eq}}sin(\omega t)\Big] \\ v_c &= e^{\frac{-t}{\tau}}\Big[\frac{v_{dc}\omega_0 sin(\omega t + \theta)}{\omega} - \frac{I_0}{\omega C_{eq}}sin(\omega t)\Big] \end{aligned} \tag{5.16}$$

Since R<<2 $\sqrt{(L_{eq}/C_{eq})}$, which means $\tau \to \infty$

$$\theta = arctan(\omega\tau) =\to 90^\circ,\ cos(90^\circ) = 0\ and\ sin(90^\circ) = 1. \tag{5.17}$$

Therefore, **Equation (5.16)** can be re-written as in **Equation (5.18)**

$$v_c = e^{\frac{-t}{\tau}}\Big[\,v_{dc}\,cos(\omega t) - \frac{I_0}{\omega C_{eq}}sin(\omega\,t)\Big] \tag{5.18}$$

The current through the capacitor can be seen from **Equation (5.19)**

$$\begin{aligned} i_c &= -C_{eq}\frac{dv_c}{dt} \\ &= \Big[\frac{e^{\frac{-t}{\tau}}}{\tau}\,v_{dc}\,C_{eq}\,cos(\omega t) + e^{\frac{-t}{\tau}}\,v_{dc}\,C_{eq}\,sin(\omega t).\omega - \frac{I_0}{\omega\tau}sin(\omega\,t) + I_0\,e^{\frac{-t}{\tau}}\,cos(\omega\,t)\Big] \end{aligned} \tag{5.19}$$

Since $\tau \to \infty$, therefore terms containing $\frac{1}{\tau} \to 0$.

Therefore, the capacitor current can be finally represented as in **Equation (5.20)**

$$i_c = e^{\frac{-t}{\tau}} \Big[v_{dc}\, C_{eq}\, sin(\omega t)\, \omega + I_0\, cos(\omega\, t) \Big] \tag{5.20}$$

Therefore the peak value of the capacitor current can be defined as given in **Equation (5.21)**

$$i_{cp} = \sqrt{\frac{C_{eq}}{L_{eq}}\, v_{dc}^2 + I_0^2} \tag{5.21}$$

The value of L_{eq} is 2L. The value of C_{eq} is a variable quantity. The value of the C_{eq} is defined as a value that varies between $\frac{C}{n}$ and $\frac{C}{2n}$. The lower limit $\frac{C}{n}$ corresponds to the situation, where only half the number of sub-modules are inserted into the system. This indicates that no more switching of sub-modules takes place after the fault occurs and only n capacitors discharge. The upper limit $\frac{C}{2n}$ means that all the capacitors in the leg are discharging. Therefore, the fault current is expected to vary within the current limits defined by these limits. The dc faults current I_{dcf} is same as the current flowing through all the three-phase upper arms or the lower arms as describe in **Equation (5.22)**[42].

$$i_{dcf} = \sum_{j=a,b,c} I_{jU} = \sum_{j=a,b,c} I_{jL} \tag{5.22}$$

$$I_{jU} = I_{jL} = i_{cp} \tag{5.23}$$

$$\sqrt{\frac{C}{2nL}\, v_{dc}^2 + I_0^2} \leq i_{jU} \leq \sqrt{\frac{C}{nL}\, v_{dc}^2 + I_0^2} \tag{5.24}$$

$$\begin{aligned} &\sum_{j=a,b,c} \sqrt{\frac{C}{2nL}\, v_{dc}^2 + I_0^2} \leq i_{dcf} \leq \sum_{j=a,b,c} \sqrt{\frac{C}{nL}\, v_{dc}^2 + I_0^2} \\ \implies &\ 25,613A\ (25.1106\, p.u.) \ \leq i_{dcf} \leq \ \ 36,048A\ (35.3416\, p.u.) \end{aligned} \tag{5.25}$$

The fault current as obtained from the simulation can be seen in **Figure 5.23**. The fault current from the simulation is seen to have the maximum value of 36.88 p.u. which is same as the value predicted by the theoretical calculation given in **Equation (5.25)**.

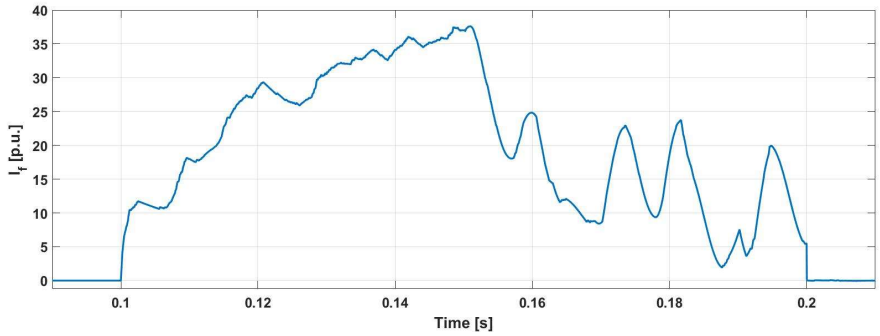

Figure 5.23: The fault current flowing through between the two DC-poles during DC-Link Pole-to-Pole fault

The path of the current flowing from the rectifier and inverter into the faulted DC-Link can be seen from **Figure 5.24** and the magnitude of the currents can be seen from **Figure 5.25**.The grid on the rectifier side is a strong grid and the grid on the inverter is a weak grid. Therefore, during the DC fault the strong grid supplies more current compared to the weak grid.

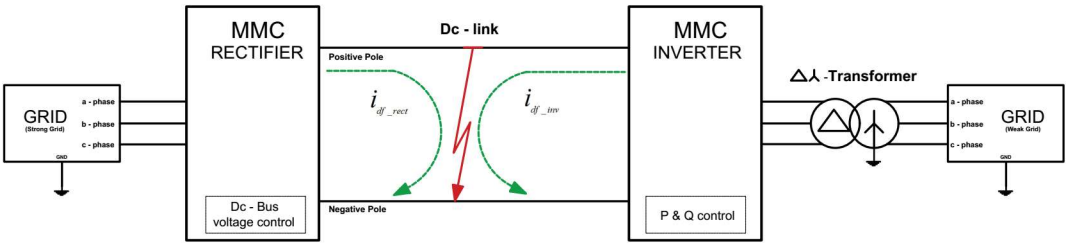

Figure 5.24: The flow of current into the faulted area during DC-Link pole-to-pole fault

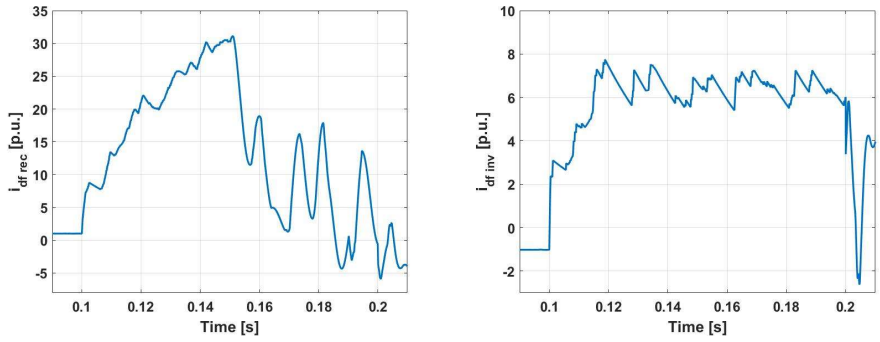

Figure 5.25: (a)Current flowing from the rectifier to the fault, (b) Current flowing from the inverter to the fault during DC-Link pole-to-pole fault

Figure 5.26 shows the variation in rectifier AC current and upper arm current

and inverter AC current and upper arm current. v_d will drop to zero and this renders the system non-functional.

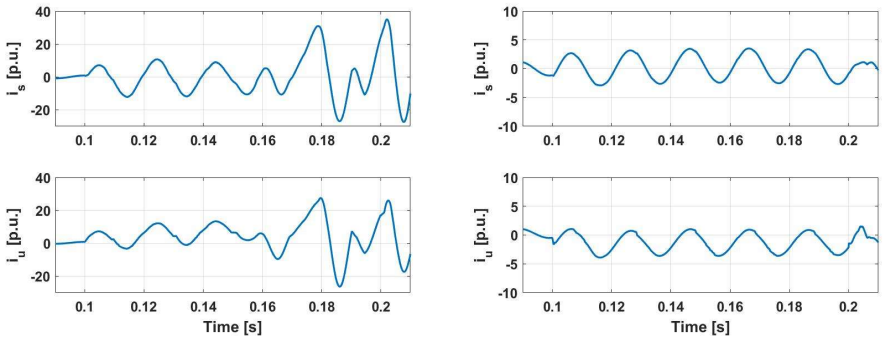

Figure 5.26: (a) Rectifier AC current, (b) Rectifier arm current, (c) Inverter AC current and (d) Inverter arm current during the fault duration 0.1s to 0.2s

The stress level experienced by the arm and AC circuit components can be seen from **Figure 5.27**.

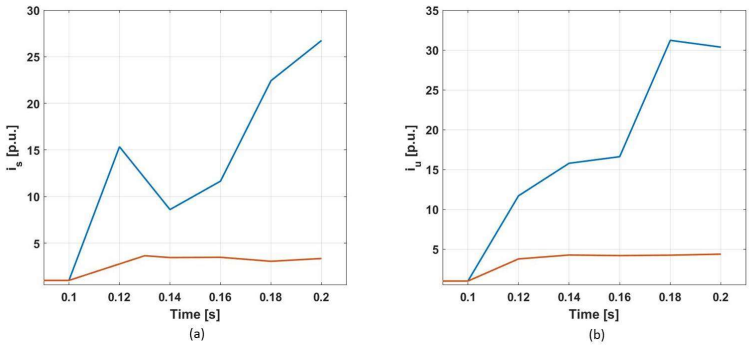

Figure 5.27: (a) Rectifier(blue) and inverter(orange) AC current, (b) Rectifier(blue) and inverter(orange) arm current, during the fault duration 0.1s to 0.2s

Thus it can be concluded that the system will be non-functional, the moment the fault occurs. However, it is very important to shutdown the system in order to save the equipments of the power system. The system will be blocked and the AC breaker will operate after 0.1s of the fault detection. The effect of the system blocking and tripping can be seen next **Section 5.2.1.1**.

5.2.1.1 The Protection Scheme

The occurrence of the DC Pole-to-Pole and Pole-to-ground fault will increase the current flowing through the arm to magnitudes above 2 p.u. within 0.002s and this will trigger the fault detection signal and the MMCs will be blocked immediately.

However, the diodes $D2$ in both the rectifier and inverter side will continue to transfer power from the AC side to the DC side. The path of which can be seen in **Figure 5.28**.

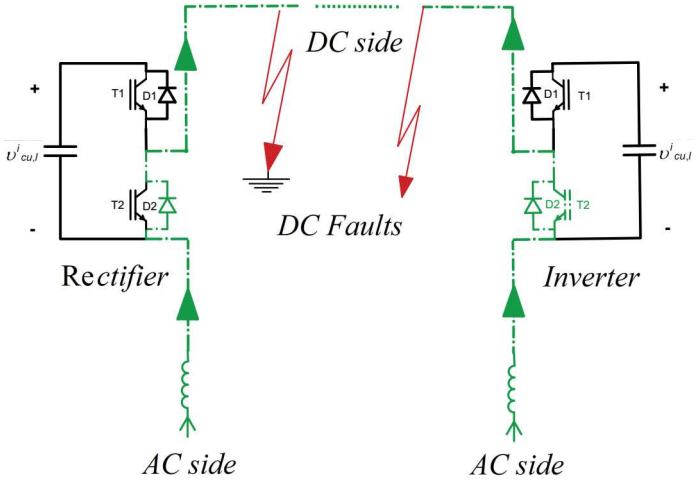

Figure 5.28: (a) The path (green) of the current through the system during the fault duration 0.1s to 0.2s

The effect of the system blocking and AC breakers tripping on the system can be seen from **Figure 5.29**. The AC current flowing through the rectifier increases in magnitude and is much higher than the current flowing from the inverter side to feed the DC fault. This is because the Grid on the rectifier side is a strong grid and the grid on the inverter side is a weak grid. The analysis is focused on the dynamics in the upper arm. The lower arm follows the same dynamics as the upper arm. The upper arm current will only flow during the positive half cycle for both the rectifier and the inverter as can be seen from **Figure 5.29**(e) and (f). The inverter current is flowing in the direction opposite to its convention and that is the reason why the **Figure 5.29**(f) shows negative half cycle. The blocking of the system during the DC fault will make the diode $D1$ reverse biased because the sub-module capacitors are charged to their nominal voltage and the DC-bus voltage has reduced to zero volts. The conduction of the diode $D2$ will bypass the submodule capacitors. Thus during the DC fault, the sub-module capacitors will be isolated and will retain their nominal voltage.

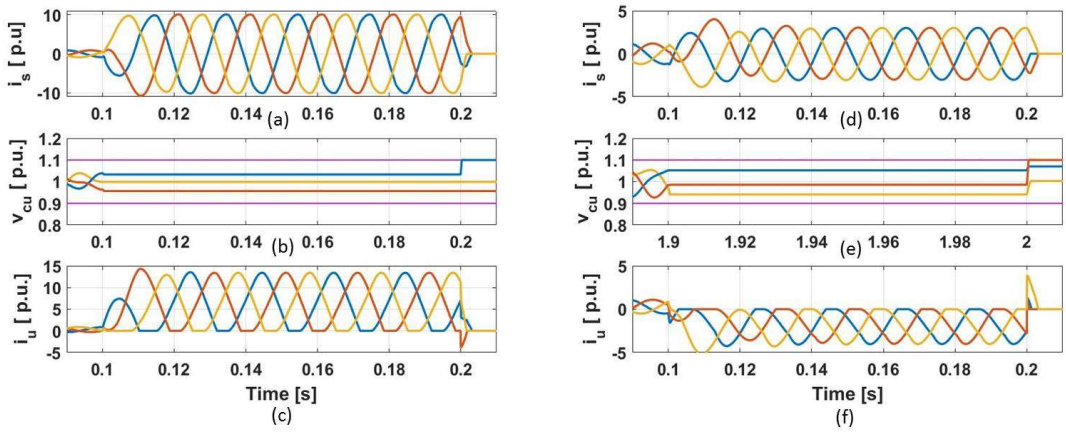

Figure 5.29: (a) Rectifier AC current, (b) Rectifier arm capacitor voltages, (c) Rectifier arm current, (d)Inverter AC current, (e) Inverter arm capacitor voltages and (f) Inverter arm current during the fault duration 0.1s to 0.2s

5.2.1.2 Effect of the arm inductance during DC Pole-to-Pole

During AC faults, the currents stop flowing through the system after the converters have been blocked. However, as discussed in **Section 5.2.1.1** that the arm currents will continue to feed the DC pole-to-pole fault through the uncontrolled diode bridge. The breakers also isolate the system after a delay of 0.1s after the detection of the fault. During this 0.1s, the system may suffer sever damage. However, the damage can be minimized by reducing the arm currents. The arm currents can be reduced by increasing the size of the arm inductor in each arm. The effect of the arm inductor on the arm current flowing through it can be seen from **Figure 5.30**.

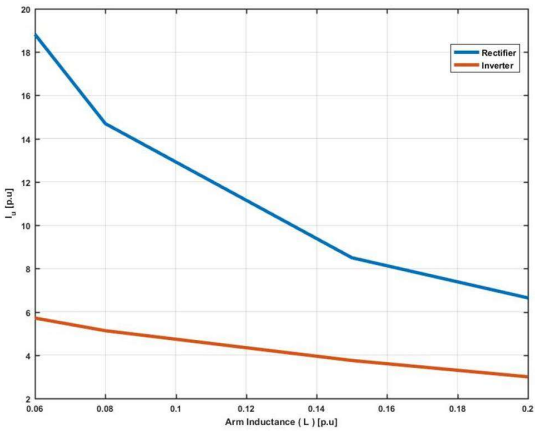

Figure 5.30: Effect of the arm inductance during DC pole-to-pole fault

5.2.2 Analysis of the power system before blocking caused due to pole-to-ground fault

The Back-to-Back MMC model along with the fault currents during a pole-to-ground fault are displayed in the **Figure 5.31**. As can be seen from **Figure 5.31** that during a DC pole-to-ground fault, the fault current from the rectifier and inverter flow into the faulted ground and is circulated back to the system through the common ground path available in the power generation. The faulted current loop did not find a closed path from the inverter side because the primary side windings of the transformer has delta configuration, which is devoid of any grounding possibilities.

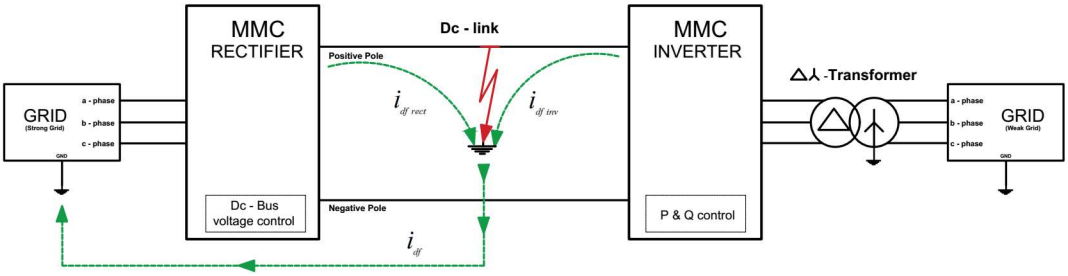

Figure 5.31: The Back-to-Back MMC configuration during the DC pole-ground fault. The dotted green lines(- -) represent the fault current path.

The behaviour of the faulted current can be seen from **Figure 5.32** and it can be seen that the fault current flowing from the rectifier and the inverter into the fault displayed in **Figure 5.33** sum up to give the fault current displayed in **Figure 5.32**.

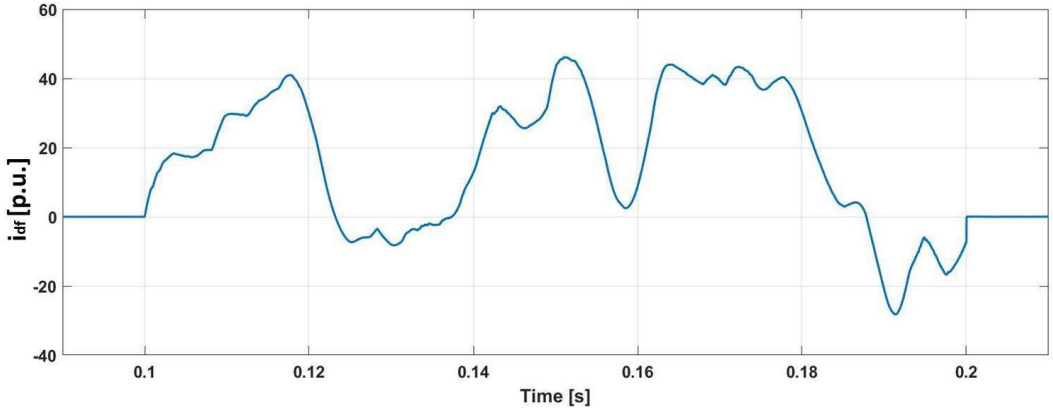

Figure 5.32: The fault current flowing to the ground during a DC pole-to-ground fault.

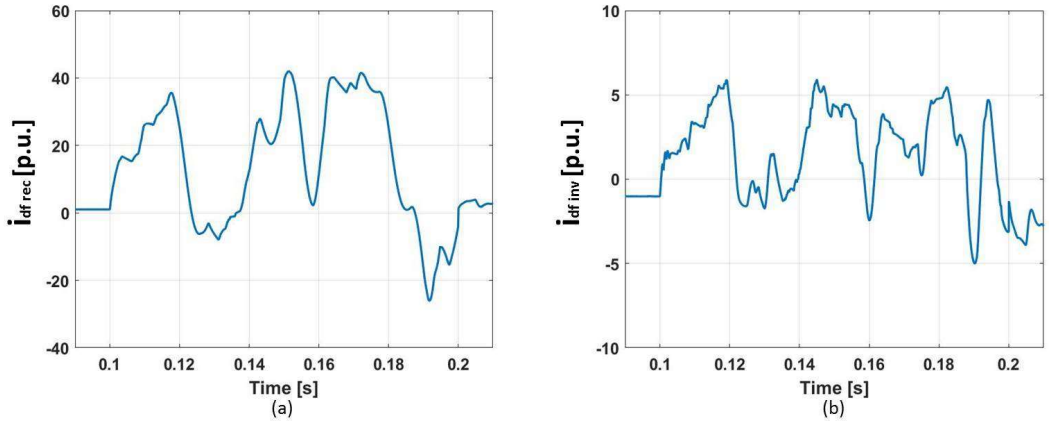

Figure 5.33: (a)The current flowing from the rectifier to the ground during a DC pole-to-ground fault, (b)The current flowing from the inverter to the ground during a DC pole-to-ground fault

Figure 5.34 shows the variation in rectifier AC current, rectifier arm current, inverter AC current and inverter arm current. v_d reaches very low voltages up to 0 V, therefore, the system is unable to work under DC pole-to-ground fault. Moreover, the high fault current flowing in the system will cause severe damage to the system equipments. Thus, the system has must be isolated as soon as possible during the occurrence of the DC pole-to-ground fault. The electrical stress exerted on the components during a DC pole-to-ground fault can be seen from **Figure 5.35**.

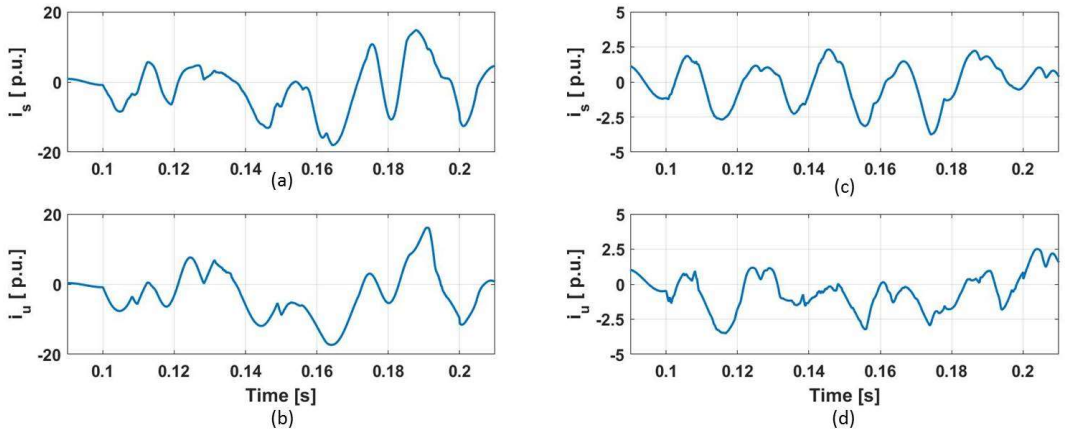

Figure 5.34: (a) Rectifier AC current, (b) Rectifier arm current (c) Inverter AC current and (d) Inverter arm current during the fault duration from 0.1s to 0.2s

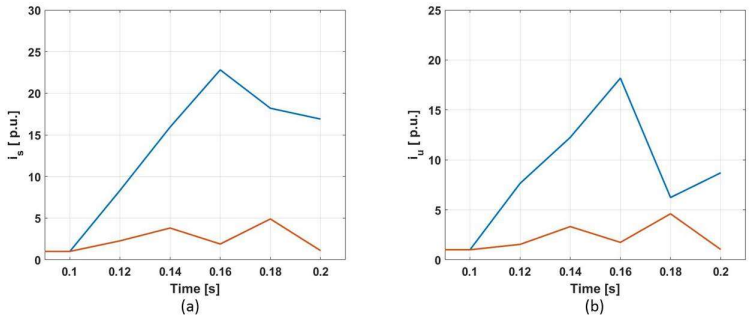

Figure 5.35: (a) Rectifier(blue) and inverter(orange) AC current, (b) Rectifier(blue) and inverter(orange) arm current, during the fault duration 0.1s to 0.2s

The high arm currents will trigger the instantaneous blocking of the converter and it will be isolated from the grids using the AC breakers. This can be seen in **Section 5.2.2.1**

5.2.2.1 The Protection Scheme against DC-Link Pole-to-Ground Fault

The behaviour of the system during the DC-Link Pole-to-Ground fault is explained in **Section 5.2.1.1** and the current paths during the fault can be seen from **Figure 5.28**.

As described in **Section 5.2.1.1** that the detection of the fault will immediately block the system and the AC breakers will operate with a delay of 0.1s and will isolate the system from the AC grids. The **Figure 5.36** shows the variation in the electrical parameters of the system.

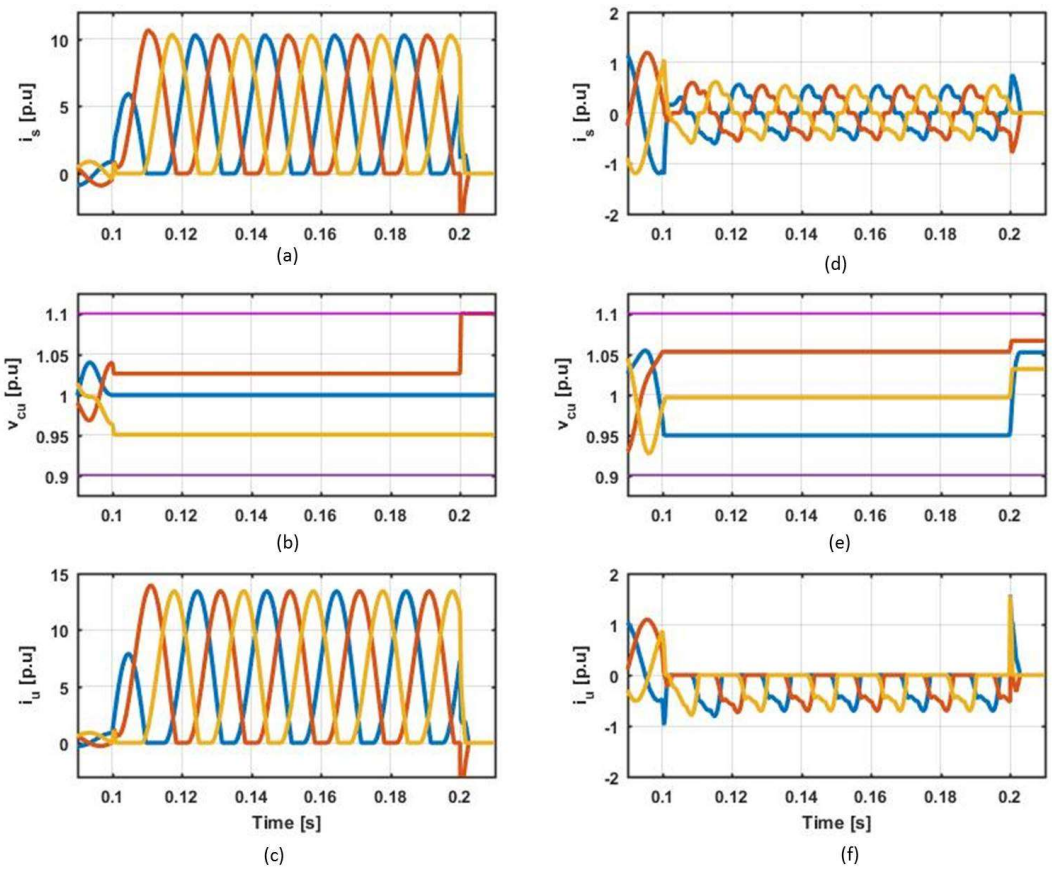

Figure 5.36: (a) Rectifier AC current, (b) Rectifier arm current (c) Inverter AC current and (d) Inverter arm current during the fault duration from 0.1s to 0.2s

5.3 Internal Fault in the Power System

The internal faults are caused due to components shorting to the ground. This can lead to the damage of the electrical equipments in the sub-modules and cause hindrance to the working of the MMC. Therefore, it is very important to analyse the effect of the internal faults on the system.

5.3.1 Internal fault in the rectifier

Figure 5.37 represents the internal fault condition in the MMC-rectifier along with the depicted current path. It can be seen that during the fault condition, current will flow into the faulted area from both the rectifier and the inverter, unless the system is blocked.

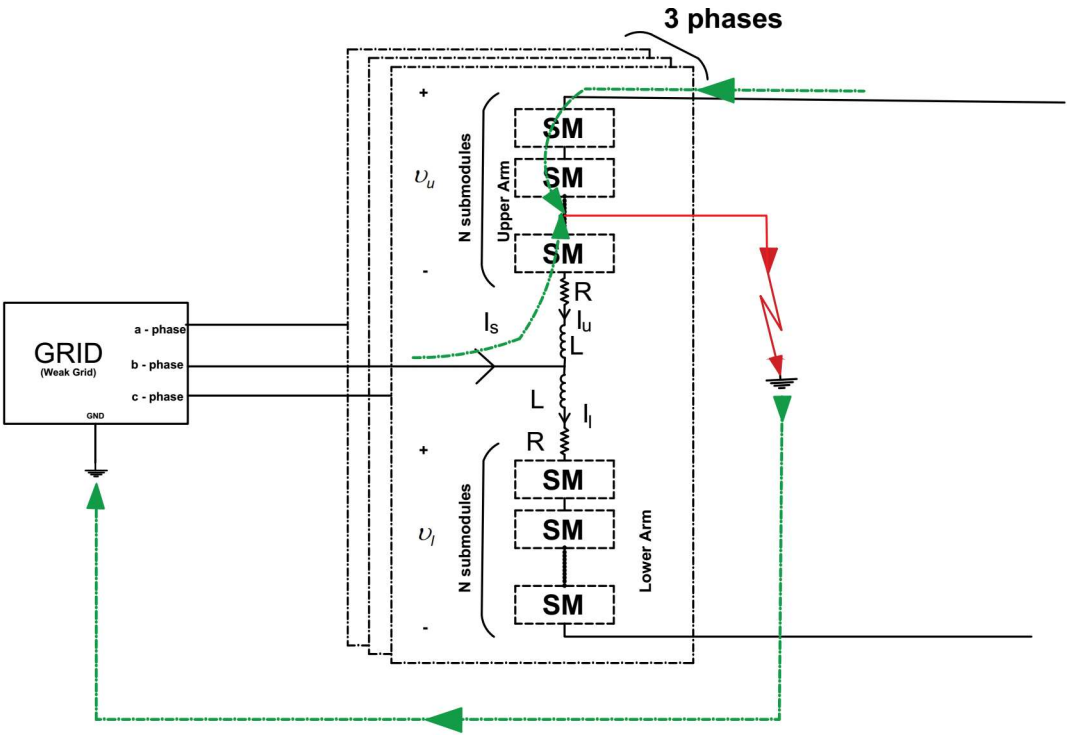

Figure 5.37: Internal fault on the rectifier and the fault current paths

The system experiences huge oscillations in i_d, $i_{cu,l}$, i_s, v_d, $v_{cu,l}$ and W_{sum}. The variations in the magnitude increases with time. **Figure 5.38**, **Figure 5.39** and **Figure 5.40** show the rectifier, DC-Link and inverter parameters' stress levels respectively, when there is an internal fault in one of the phases in the rectifier and the converter is neither blocked nor isolated.

From **Figure 5.38**(a), it can be seen that the AC current input increases during the fault condition and reaches a peak value of 10 p.u. This leads to the increase in the arm currents. It can be seen from **Figure 5.38**(b) that the arm current also increases to a peak value of 17.8 p.u. The high current flowing in the arm causes increased arm capacitor voltages**Figure 5.38**(c). This will cause an increased energy level in the capacitor, which can be seen from **Figure 5.38**(d). The similar effect is seen in the inverter in **Figure 5.40**, but with reduced magnitude of the parameters because it is connected to the weak grid.

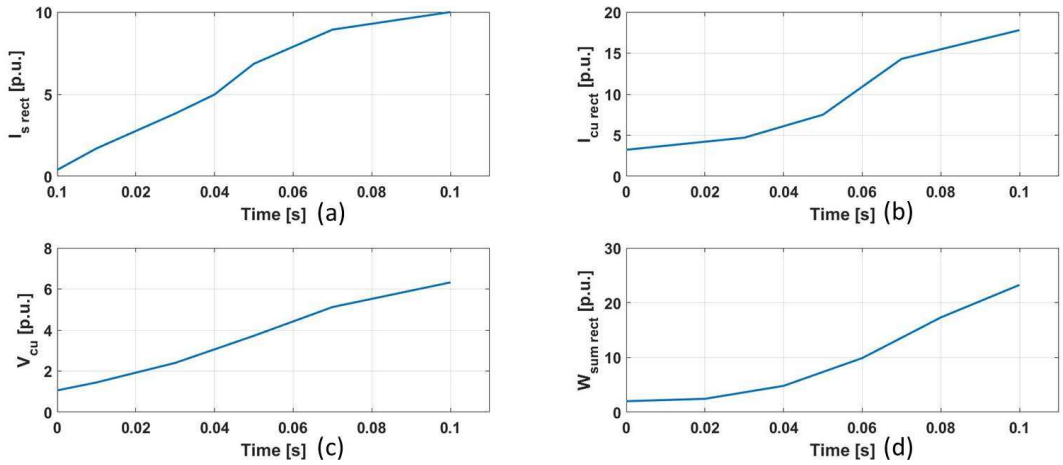

Figure 5.38: Internal Faults rectifier parameters :(a) AC current from rectifier, (b) Current flowing in one of the upper arms of the rectifier, (c) The voltage of the upper arm submodules and (d) The variation in the energy stored in each arm

The increased voltages on the sub-modules will lead to higher DC-Link voltages as can be seen from **Figure 5.39**(a). The fault will cause current from the inverter to flow into the faulted area in the rectifier through the DC-Link, thereby increasing the DC-Link current with the passage of time during the event of the fault **Figure 5.39**(b).

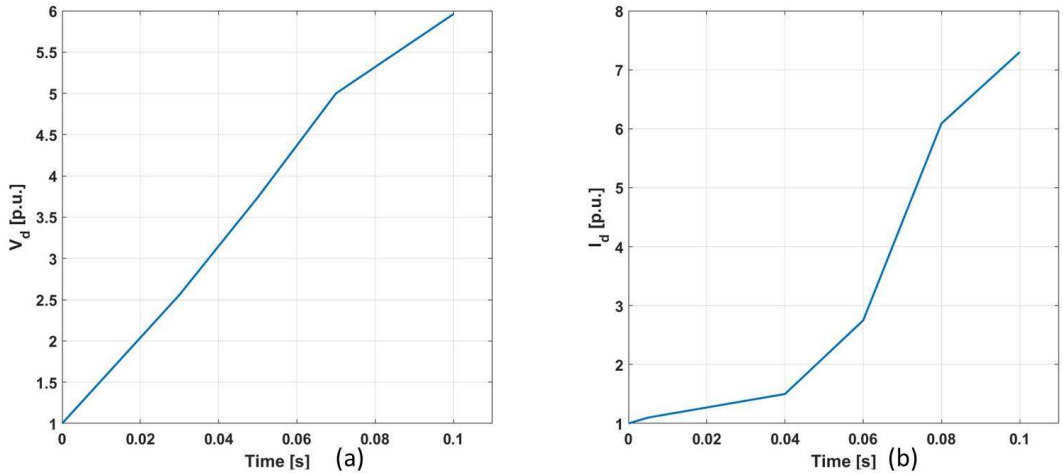

Figure 5.39: Internal Faults DC parameters: (a) DC-Link voltage, (b) DC-Link current

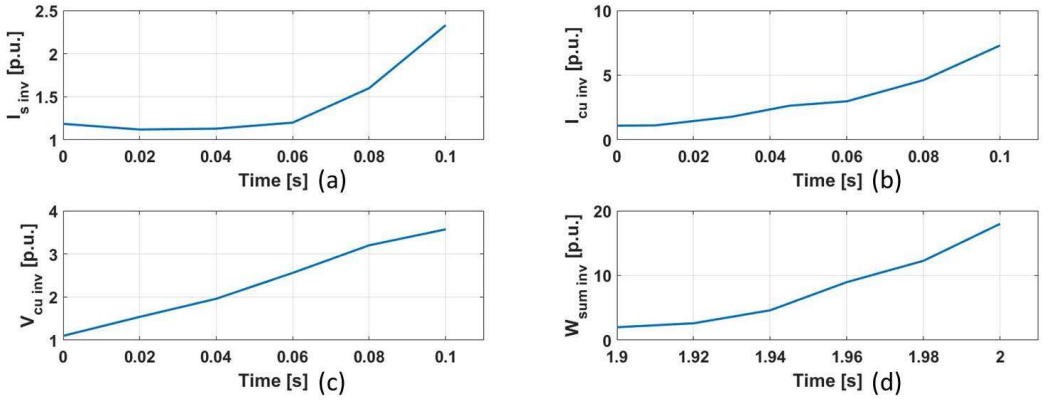

Figure 5.40: Internal Faults inverter parameters :(a) AC current from rectifier, (b) Inverter upper arm current, (c) Inverter upper arm sub-module capacitor voltages and (d) The variation in the energy stored in each arm

5.3.1.1 The Protection Scheme

The high arm currents flowing in the system during the fault condition will be detected by the protective mechanism of the system and the system will be blocked and the AC breakers will isolate the system with a delay of 0.1s. During this time interval of 0.1s, the number of sub-modules that will suffer damage will depend on the location of the fault in the arm. N_{up} sub-modules will be safe during this blocked stage and N_{down} sub-modules will be stressed as can be seen from **Figure 5.41**. The DC-Link current cannot flow backwards into the fault as the diode D_1 in the sub-modules (N_{up}), which are between the fault location and the DC-Link, gets reverse biased, when the converter is blocked. Thus, no current flows through these sub-modules and they are safe during an internal fault. But the sub-modules (N_{down}) between the fault location and the AC side, will still conduct through diode D_2 and through this path, the grid on the rectifier side will feed power to the fault. Since the fault current flows through this path, so these sub-modules(N_{down}) are most vulnerable to suffer damage during an internal fault.

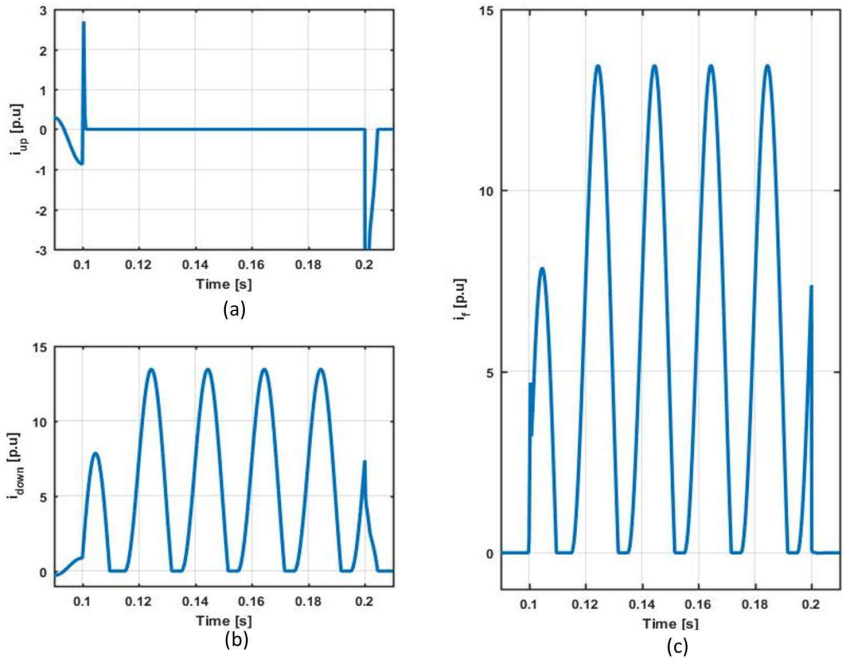

Figure 5.41: (a) Current flowing through sub-modules N_{up}, (b) Current flowing through sub-modules N_{down} and (c) Fault current flowing through the faulted line during an internal fault with the converters in blocked state

The blocking of the converters will stop the flow of the AC current into the system from the DC-Link, thereby making the inverter arm current and AC current zero as explained in **Section 5.1.3**. Thus, the capacitors in the sub-modules of the inverter and the rectfier will retain its nominal voltage and will be disconnected from the circuit as can be seen from **Figure 5.42**(b) and (e). The arm current through the N_{down} sub-modules of the faulted phase will flow during its positive half cycle, but there will be no current flowing from the other phases into the fault because the diodes in N_{up} sub-modules of the faulted phase are reverse biased. This behaviour of the rectifier arm currents can be seen from **Figure 5.42**(e).

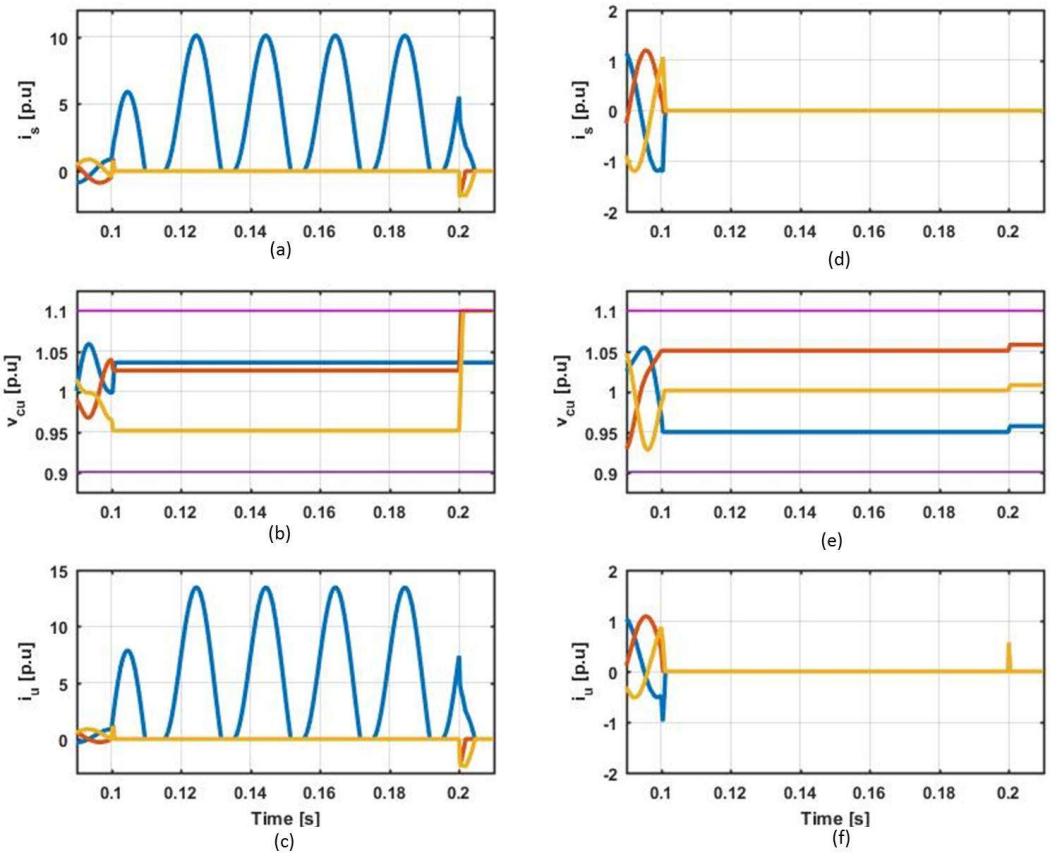

Figure 5.42: (a) Rectifier AC currents, (b) Rectfier sub-module capacitor voltages, (c) Rectifier arm currents (until fault location), (d) Inverter AC currents, (e) Inverter sub-module capacitor voltages and (f) Inverter arm currents

Chapter 6

Conclusion and Future Work

6.1 Conclusion

The project focuses on investigating the behaviour of the Back-to-Back MMC under steady state and fault conditions for medium voltage operations. Throughout the thesis several findings were encountered.

- Attention was given to the design of the MMC. The choice of the sub-module capacitance is based on the energy requirement of the MMCs. These energy requirements depends on several parameters as: (a) Modulation index, (b) Power angle , (c) Capacitor ripple and (d) Modulation technique. The size of the arm inductor is determined by observing the effect of the size of arm inductor on i_s THD and using the optimization process *Direct Pareto Front* an optimum size of the arm inductor is chosen. It was concluded that by this optimization in the size of the components, the cost of the passive components in the MMC can be minimized.

- The DC-Link voltage ripple is observed and three techniques have been suggested to reduce the DC-Link voltage ripple. The three techniques being: (a) Introduction of DC-Link capacitor, (b) Use of space vector modulation and (c) Under-modulation of the inverter. All this technique successfully reduce the DC-Link voltage ripple. Thus, it can be concluded that with proper design and control, the Dc-Link capacitor can be avoided.

- The behaviour of the Back-to-Back MMC is analysed during faults: (a) AC, (b) DC and (c) Internal faults. The preventive measures for the system during the fault conditions are discussed. It was observed that during single line-to-ground fault with a fault impedance of 0.16 p.u., the system did not trip. However, the increase of the sub-module capacitor voltage was limited to 1.1 p.u. by the use of the chopper. The double line-to-ground fault

and triple line-to-ground fault causes high currents to flow in the arms of the MMCs. A protection strategy was derived comprising of: (a) The DC chopper, which does not allow the sub-module capacitor voltages to go beyond 1.1 p.u., (b) The converters are blocked to prevent high arm currents from flowing through the sub-modules and (c) The system is isolated using AC breakers. By simulation verification, it was concluded that the protection strategy is effective.

- The DC faults are also discussed :(a) DC-Link pole-to-pole and (b) DC-Link pole-to-ground. These faults are bolted faults. During the DC faults, the effect of the arm inductor on the arm current is observed. The analysis can help to optimize the size of the inductor.
- The internal faults are analysed and it is observed that during an internal fault, the sub-modules of the faulted phase that are between the fault location and the DC-Link do not suffer damage. It is concluded that the sub-modules of the faulted phase that are between the fault location and the AC side are under severe stress until the time when the AC breakers isolate the system.

6.2 Future Work

- This thesis uses average model of the Back-to-Back MMC. However, the behaviour of the system can be better represented using the switching models.
- Validation of the proposed DC-Link voltage ripple reduction techniques and the fault protection methods in the laboratory.

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Appendix A

1

A.1 Three-Phase Power Systems

Three phase power systems represent a set of three oscillating quantities which have defined phase differences among them. As per the convention, the phases are defined as phase a, b and c. The phases b and c lags phase a by $120^{\circ}(2\pi/3)$ and $240^{\circ}(4\pi/3)$ respectively.The three-phase voltages can be represented as given in equation A.1.

$$\begin{aligned} \nu_a &= \widehat{V}_a cos(\omega t + \phi) \\ \nu_b &= \widehat{V}_a cos(\omega t - 2\pi/3 + \phi) \\ \nu_c &= \widehat{V}_a cos(\omega t - 4\pi/3 + \phi) \end{aligned} \tag{A.1}$$

The voltages ν_a, ν_b, ν_c are the instantaneous phase voltages. $\widehat{V}_a$, $\widehat{V}_b$, $\widehat{V}_c$ are the peak values of the phase voltages and ϕ is the power factor angle. The power system can be both balanced and unbalanced.

A.1.1 Balanced Power Systems

Balanced power systems are defined as three-phase systems, where the oscillating three-phase quantities have the same peak value and have an equal phase shift of 120 $^{\circ}$ among them.

A balanced three-phase power system has the following attributes:

- The sum of the instantaneous values of the three-phase quantities is zero : ν_a+ν_b+ν_c=0 ; $\forall$ t
  Since, the sum of the instantaneous values is zero in a three-phase system, so the neutral return path for the current can be avoided.

- The sum of the square of the instantaneous values of the three-phase quantities is constant : $(\nu_a)^2$+$(\nu_b)^2$+$(\nu_c)^2$= constant ; $\forall$ t

This implies that the three-phase balanced power system is capable of delivering constant power at all time.

A.1.2 Unbalanced Power Systems

An unbalanced power system is a result of faulted power system. The fault may occur due to numerous reasons: failure of insulation at any point, contact of live wires, short-circuit of line and the cabinet, etc. The reasons for faults in the power system could be many and every fault has detrimental effect on the power system. The effect of short-circuit on a power system depends on the level of the fault which is also proportional to the number of phases involved in the short-circuit fault.

Faults are catogorised as:

- Symmetrical faults
- Unsymmetrical faults

A.1.2.1 Symmetrical faults

This is a typical three-phase fault, where all the three-phases are either short-circuited with or without ground as can be seen from figure A.1. These kind of faults are balanced in nature, which means that the phases are displaced by an equal angle of 120 $^{\circ}$ from each other. Hence, they are also known as symmetrical faults. These faults are the most severe faults observed in a power system because it involves the largest current to flow through the system. However, the occurence of such faults are also less, compared to other unsymmetrical faults.

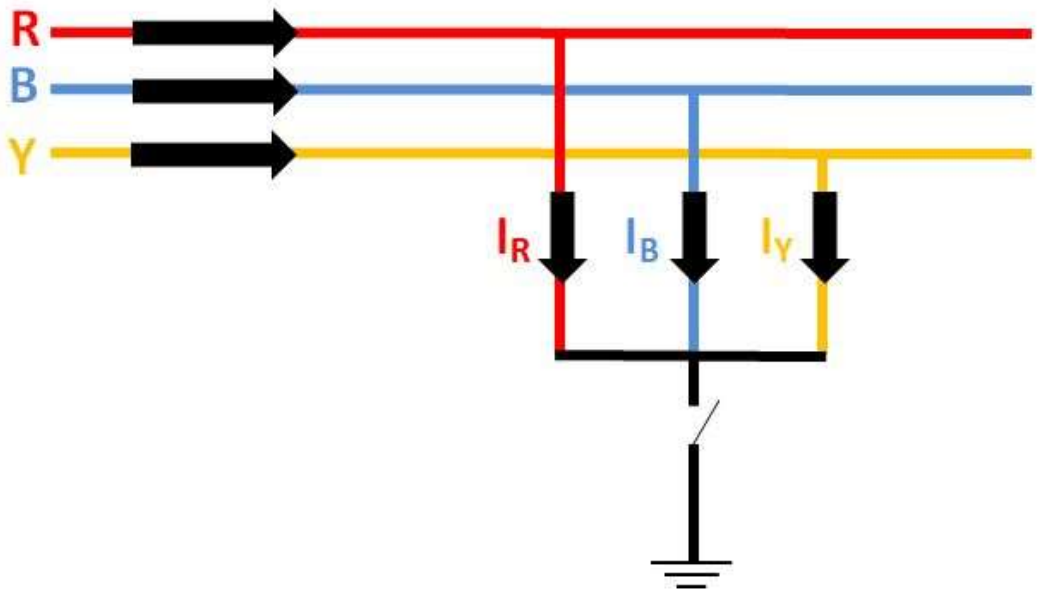

Figure A.1: Symmetrical Faults

A.1.2.2 Unsymmetrical faults

The unsymmetrical faults involve only one or two phases. Thus the three phase power system becomes unbalanced. Equation A.2 relates the unbalanced conditions with the three-phase power system impedances. These faults can be catagorised as:

- Single line-to-ground fault(LG)
- Line-to-line fault (LL)
- Double Line-to-ground fault (LLG)

A single line-to-ground fault is considered to be the mildest fault compared to the other faults in the three phase power system. These unsymmetrical faults analysis becomes tedious and time consuming due to lack of symmetry. Therefore, symmetrical components are used to represent the unsymmetrical faults. This makes the analysis easier.

$$Z_a \neq Z_b \neq Z_C \quad ; \quad Z_{ab} \neq Z_{bc} \neq Z_{ca} \tag{A.2}$$

There are three symmetrical components: (a) Positive, (b) Negative and (c) Zero sequence components. These can be seen from figure A.2. The positive sequence components have the same phase shift as the normal rotating field. The negative sequence components have phase rotation in the sequence opposite ot the normal

rotating field and the zero sequence components are a set of components which has no phase shift among the three phases. Negative sequence components flow in the system only during an unbalance in the system that can be caused either by power system unbalance or varied loading of the lines.

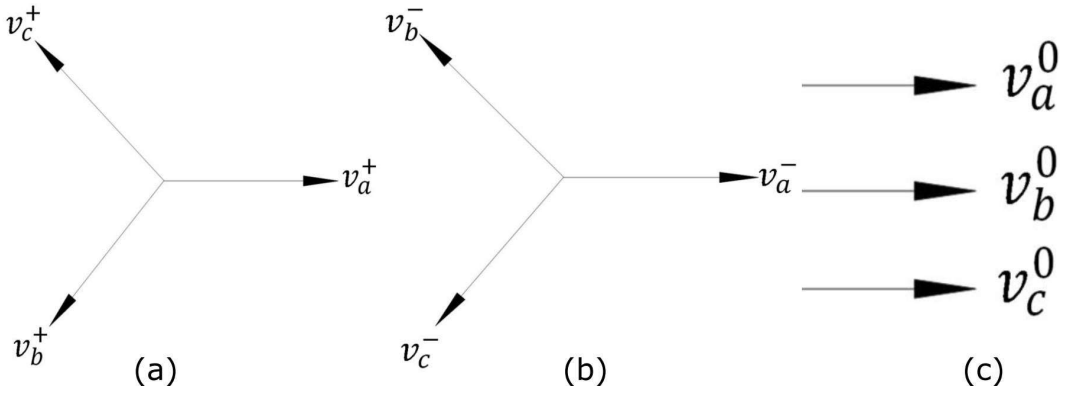

Figure A.2: Symmetrical components: (a) Positive sequence, (b) Negative Sequence, (c) Zero Sequence

The zero sequence current flows in the circuit only if the potential of the two grounds in the system is not the same. The earth/ground potential varies from place to place and it is DC in nature. This potential difference leads to the flow of zero-sequence currents in the circuit. Therefore, the most important factor for the flow of zero-sequence components in the power system is the existence of ground. Secondly, the zero-sequence currents flow due to potential difference between the two grounds, which confirms the need for two grounds to complete the circuit. Thus, the effect of the zero-sequence components can be seen only during a faulted condition and that too, only on the star-connected side of the transformer, whose star-side neutral is connected to the ground. This is also the reason for the non-existence of zero-sequence components in the delta connected terminals of the transformer. Figure A.3 shows the transformer connection for zero sequence path [36].

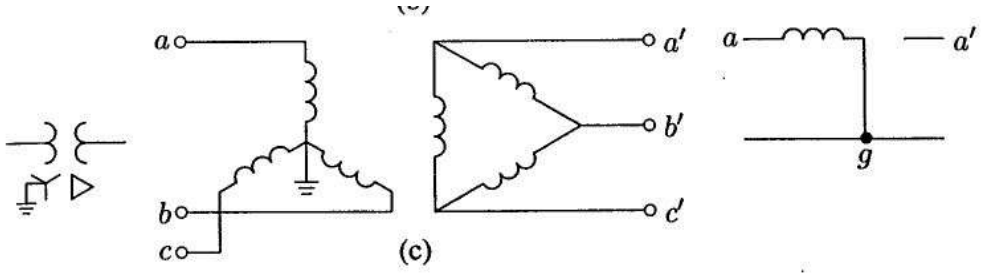

Figure A.3: Zero sequence star-delta transformer connection

The positive sequence components can be seen from equation A.3

$$\begin{aligned} v_a^+ &= \widehat{V}_{+1}\, cos(\omega t + \phi_{+1}) \\ v_b^+ &= \widehat{V}_{+1}\, cos(\omega t - 2\pi/3 + \phi_{+1}) \\ v_c^+ &= \widehat{V}_{+1}\, cos(\omega t - 4\pi/3 + \phi_{+1}) \end{aligned} \tag{A.3}$$

The neagtive sequence components can be seen from equation A.4

$$\begin{aligned} v_a^- &= \widehat{V}_{-1}\, cos(\omega t + \phi_{-1}) \\ v_b^- &= \widehat{V}_{-1}\, cos(\omega t - 4\pi/3 + \phi_{-1}) \\ v_c^- &= \widehat{V}_{-1}\, cos(\omega t - 2\pi/3 + \phi_{-1}) \end{aligned} \tag{A.4}$$

The zero sequence components can be seen from from equation A.5

$$\begin{aligned} v_a^0 &= \widehat{V}_0\, cos(\omega t + \phi_0) \\ v_b^0 &= \widehat{V}_0\, cos(\omega t + \phi_0) \\ v_c^0 &= \widehat{V}_0\, cos(\omega t + \phi_0) \end{aligned} \tag{A.5}$$

Similar to three phase voltages, the three phase currents are also represented in terms of the symmetrical components as can be seen from equation A.6.

$$\begin{aligned} I_a &= I_a^0 + I_a^+ + I_a^- \\ I_b &= I_b^0 + I_b^+ + I_b^- \\ I_c &= I_c^0 + I_b^+ + I_c^- \end{aligned} \tag{A.6}$$

The equation A.8 is an expression of equation A.6 in terms 'a', where 'a' is given by equation A.7.

$$a = 1\underline{/120^\circ} \tag{A.7}$$

$$\begin{aligned} I_a &= I_a^0 + I_a^+ + I_a^- \\ I_b &= I_a^0 + a^2 I_a^+ + a I_a^- \\ I_c &= I_a^0 + a I_a^+ + a^2 I_a^- \end{aligned} \tag{A.8}$$

Equation A.8 can also be expressed as equation A.9

$$I_{a,b,c} = [A] * I^{0,+,-} \tag{A.9}$$

Matrix [A] is defined in equation A.10

$$[A] = \begin{pmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{pmatrix} \tag{A.10}$$

The symmetrical components are expressed in terms of the phase quantities in equation A.11.

$$\begin{aligned} I_a^0 &= \frac{1}{3}(I_a + I_b + I_c) \\ I_a^+ &= \frac{1}{3}(I_a + aI_b + a^2 I_c) \\ I_a^- &= \frac{1}{3}(I_a + a^2 I_b + aI_c) \end{aligned} \tag{A.11}$$

As it can be clearly seen from equation A.11 that the zero sequence component is one-third of the phase quantities, so if the phase quantities sum to zero, then the zero sequence component also seizes to flow in the three-phase system. However, it might flow in the neutral-ground connection, but will not effect the power system[36].

The total unbalanced power in the power system can be easily calculated using the symmetrical components as given by equation A.12

$$S_{3\phi} = V^{a,b,c^T} \times I^{a,b,c^*} \tag{A.12}$$

Equation A.12 can be further expressed in equation A.13, which is in terms of matrix [A] defined in equation A.10.

$$S_{3\phi} = ([A] \times V^{0,+,-})^T \times ([A] \times I^{0,+,-})^* \tag{A.13}$$

$$\begin{aligned} S_{3\phi} &= 3 \times ([V^{0,+,-})^T \times (I^{0,+,-})^* \\ &= 3V_a^0 I_a^{0*} + 3V_a^+ I_a^{+*} + 3V_a^- I_a^{-*} \end{aligned} \tag{A.14}$$