Aalborg University

Master Thesis

FEM simulation of IGBTs under short circuit operations

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PED4-1044

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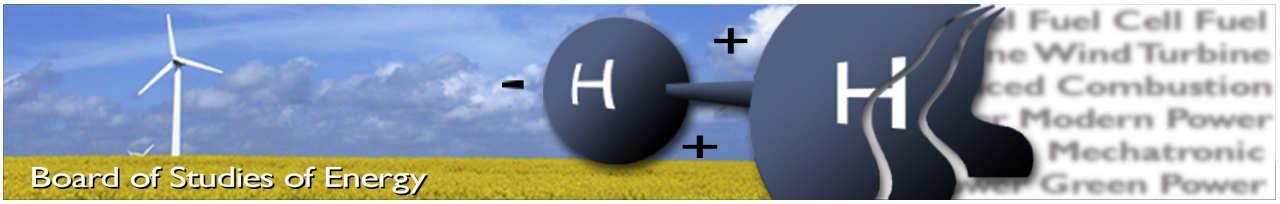

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SYNOPSIS:

IGBTs are the backbone of modern low, medium and high power converters. One of the most sever operational conditions that these encounter is the short circuit failure and during this it has been observed that gate-emitter voltage oscillations occur threatening the robustness of the device.
For studying these oscillations, an IGBT model was created in TCAD FEM environment and its operation under both static and transient behavior was studied. Afterwards, the model was used for simulating the device under short circuit conditions and a sensitivity analysis to the stray elements associated to the device was performed. The conditions for such oscillations to occur have been identified and the effect of each element was studied.
Keywords: Short-Circuit failure, Gate Voltage Oscillations, TCAD simulation

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By signing this document, each member of the group confirms that all group members have participated in the project work, and thereby all members are collectively liable for the contents of the report. Furthermore, all group members confirm that the report does not include plagiarism.

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Chapter 1

Introduction

IGBTs are nowadays the backbone of the modern low, medium and high power converters. The main advantage of such devices are the fact that they combine a high input impedance (MOS-Gate controlled) with the low on-state resistance of a bipolar device. This stems from the fact that the IGBT is essentially a MOSFET transistor in a Darlington configuration with a PNP BJT transistor. This is achieved by developing a semiconductor device that contains 4 doping regions as shown in Figure 1.1, where a vertical topology of a typical IGBT is shown.

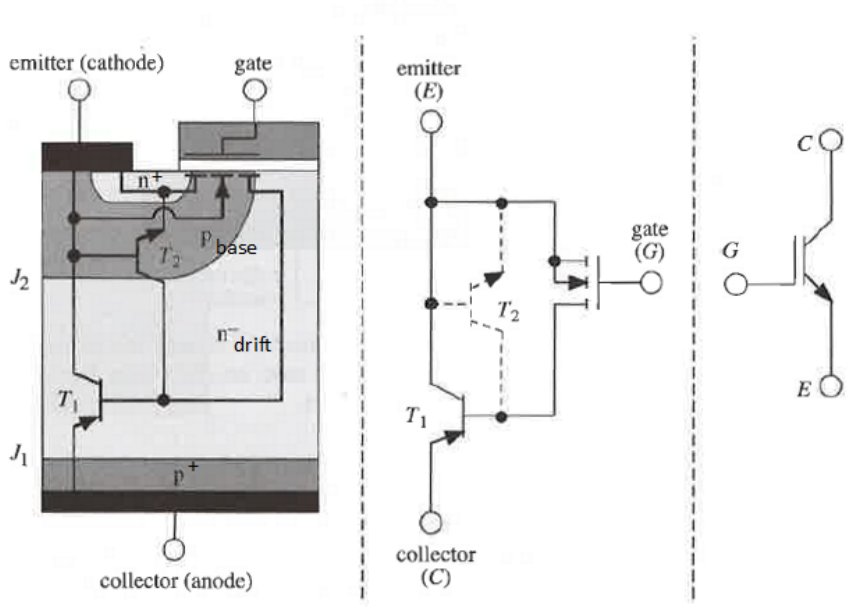


FIGURE 1.1: Typical IGBT design and its equivalent electrical circuit [1].

It can be seen from the IGBT cross-section in Figure 1.1, that a MOSFET transistor is formed consisting of the N^+ (Source), the P_{Base} (Channel) and N_{Drift} region (Drain). A PNP transistor is also formed, consisting of the P_{Base} region (Collector), the N_{Drift} region

(Base) and the P^+ region (Emitter) and together, connected in a Darlington configuration, they form the IGBT.

Due to combining the advantages of both MOSFETs and BJTs, this semiconductor device is the preferred choice for power electronics applications. In Figure 1.2 it can be seen that IGBTs occupy the market needs with the highest demand (industrial and traction applications) and thus making these devices the most commonly used for developing power converters.

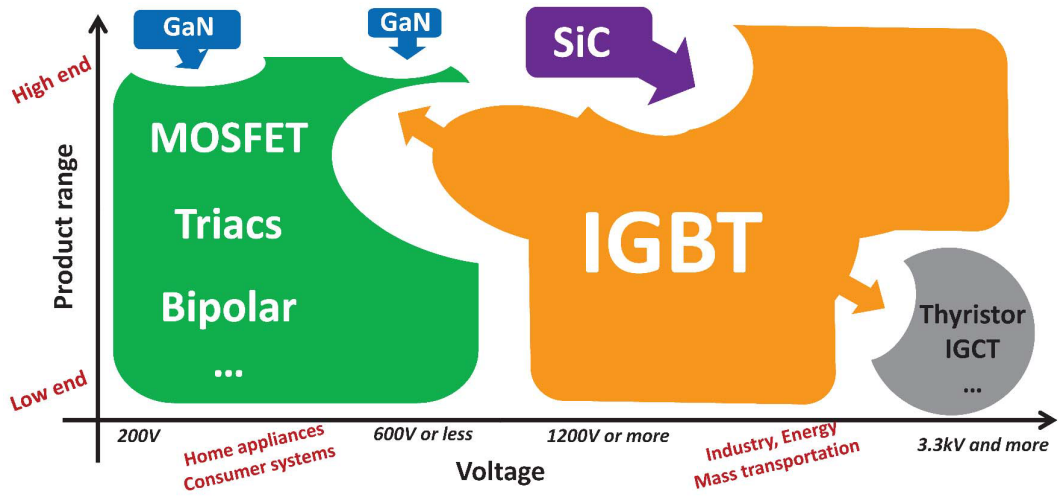
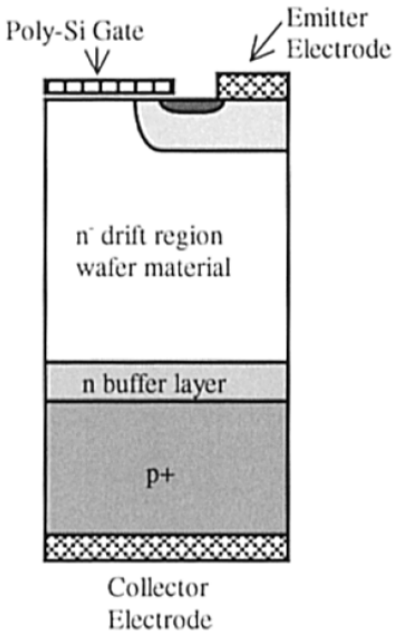


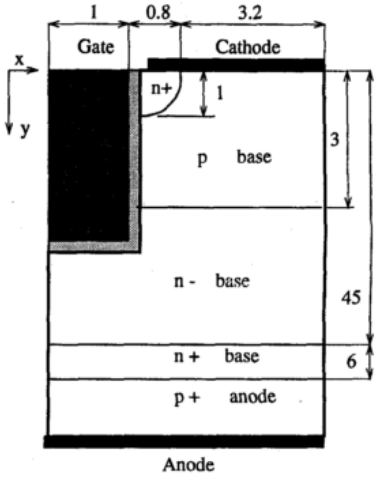
FIGURE 1.2: Power handling devices and their share in the power managing applications [2].

It is due to this large market for IGBTs that a great effort is put in increasing the power rating capability of these devices, while reducing the turn on and off switching losses. Additionally, the blocking voltage capability is a crucial parameter as with IGBTs being able to handle higher voltages, the number of IGBTs required to be placed in series for supporting higher blocking voltages can be reduced. This way, the cost of medium voltage converters is reduced alongside with the voltage sharing issues that occur in such chain topologies. Towards these improvements an extensive research has been done in the past, leading to different IGBT geometrical designs.

The two main geometrical variations that differ from the classical IGBT as presented in Figure 1.1 will be described briefly here. For creating an IGBT that can have a higher blocking capability, it is required for the N_{Drift} layer to support the electric field developed across this region. This is achieved by increasing the drift region width and therefore reducing the electric field across the J2 PN junction shown in Figure 1.1. However, some design trade-offs must be taken into account, for instance, the on-state losses increase with the increase of the width. In order to optimize the device behavior, a buffer N^+ layer is introduced between the drift and P^+ layer as shown in Figure 1.3a achieving this way a smaller drift layer width for supporting the same blocking voltage [4]. Thus, an IGBT with smaller on-state losses could be developed. The classical IGBT is called non punch through (NPT) whereas the newly introduced is called punch through (PT).



(A) The punch through IGBT geometry [6].



(B) Trench gate IGBT geometry [5].

FIGURE 1.3: Geometrical variations of IGBTs.

A second geometrical difference with which an IGBT can be manufactured has to do with the gate oxide geometry. The gate oxide can be horizontal as shown previously or vertical as shown in Figure 1.3b, resulting thus to the formation of the Trench Gate IGBT. The advantages of this topology has to do with the reduced channel losses, smaller on-state voltage drop and has an increased safe operational area [5]. The way that such advantages over the usual design appear, will be described later in Chapter 2.

These specific topological differences to the common IGBT design are presented hereby, as the IGBT which has been designed during this thesis is a Trench Gate Punch Through IGBT.

1.1 IGBT as part of a converter

As mentioned above, IGBTs are the most common semiconductor devices used in power converters and also they are the most critical element alongside the capacitors in a power electronics system as presented in Figure 1.4. For this reason, an extensive research is being conducted in identifying the failure mechanisms and working towards mitigating them.

Common lifetime degradation factors are the high electric field generated within this device, as during a switching cycle they are put in blocking mode, supporting the full DC-bus voltage in 2-level converters or a fraction of it in higher level converters. The electric field acts as activator for impurities that are contained within the IGBT and with the progress of time these are accumulated in vulnerable parts of it, such as the gate oxide.

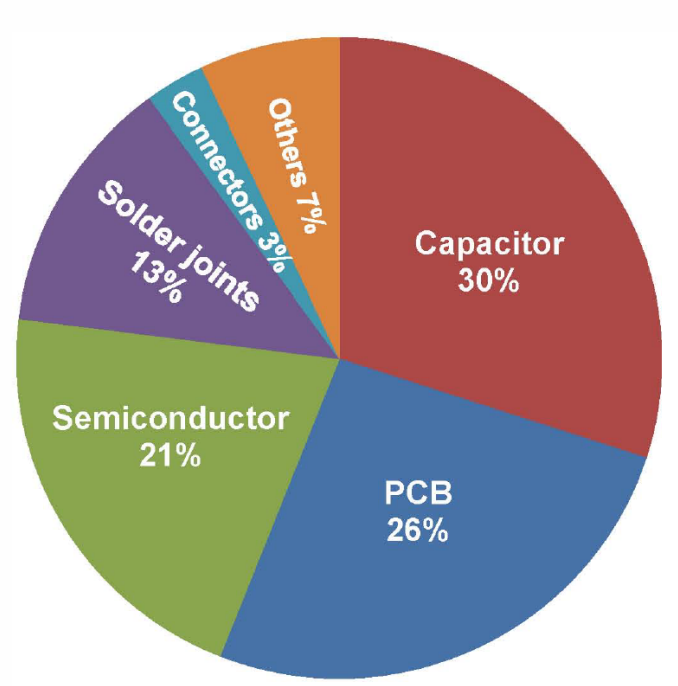


FIGURE 1.4: Failure percentage of components in power electronics systems [3].

Another usual mechanism affecting the lifetime of the IGBT has to do with the self-heating effect due to internal losses. The temperature increases the activation mechanism discussed above, but also due to the device operating in switching mode, as the power through the IGBT cycles, a temperature cycling is occurring. This has as an effect, the mechanical stress of the device itself, but also of the parts that are attached to the device, such as the bond-wires and the solder connection of the die to the base plate of the module which encapsulates it.

One operational mode that stress the IGBT both thermally as well as by generating a high electrical field across the device is the short circuit failure [7]. Such failure can occur across the load or by failing to switch off one of the IGBTs in an H-Bridge topology, before turning on the second one. In both those cases, the IGBT is turned on under the full DC-bias voltage. During this mode a high current appears through the IGBT resulting to a rapid heat up. It is required from the industry for the IGBTs to be capable of successfully enduring at least 10 μs of short circuit current and successfully switching off within this duration of time [1]. The short-circuit behavior is occupying a large portion of the current thesis and will be presented in Chapter 3. In the same chapter, the operation of the IGBT under normal switching conditions will be presented, as a verification that the modeled device fits well the behavior of the real device. This assures that the two devices will have similar behavior under short circuit mode.

During short circuit failure mode, the obvious mechanism that results in the deterioration of the lifetime of the IGBT has to do with the high rise of temperature in localized spots resulting to high carrier generation [7]. Devices have been designed to be able to withstand

a high number of short circuit failures, as long as these are terminated within $10\mu s$. Apart from the heating effect that takes place during short circuit, it has been observed that high frequency oscillations occur superimposed to the gate-emitter voltage (V_{GE}) [8]. Such oscillations can cause the V_{GE} voltage to obtain values above the maximum rated ones, stressing the gate oxide and causing its breakdown. Such a behavior jeopardizes the ruggedness of the IGBTs against short circuit failures, resulting to failures before the end-of-lifetime of the device. Although this phenomenon has been studied for more than 10 years, the cause that triggers these oscillations has not been identified. This thesis aims towards aiding the research conducted at Aalborg University in identifying the triggering mechanism.

1.2 Problem statement and Objectives

The reliability of the semiconductor devices utilized in a switch mode converter is of paramount importance for industrial converters and more importantly power electronic systems that are placed in locations with limited access. The most commonly used device is currently the IGBT and its degradation mechanisms have been and are currently heavily investigated. One of the most stressful conditions under which an IGBT is placed is the short circuit failure at which high power is dissipated within the device. This means that the device must have a high robustness against these conditions.

More importantly, during short circuit failure cases, oscillations have been observed at the gate - emitter voltage which can cause the instant failure of the gate oxide, having a catastrophic effect to the IGBTs. It is important to develop gate drivers that can prevent the triggering of such oscillations, increasing, thus, further the reliability of the IGBTs. In order to work towards this direction, the identification of the oscillation origin is of great importance.

This thesis targets towards creating an IGBT model that will be able to be used in this direction by the ongoing research conducted at Aalborg University.

1.3 Limitations

The project at hand was subjected to certain limitations that can be seen below:

- The actual model of the IGBT was not available, therefore a model was developed based on datasheet values. The model has been taken from the TCAD library and modified to match the behavior of a 3.3 kV IGBT.
- Lack of knowledge on the geometrical properties and doping profiles of the targeted IGBT.

- Complexity of the modeled device led to omit the inclusion of non-ideal elements appeareaing on an actual IGBT, i.e. doping impurities, gate oxide charge traps etc.
- Complexity of the device and the project at hand led to disregard self-heating phenomena.

1.4 Personal Goals

The personal goals for this project are listed below:

- Obtain comprehensive understanding of TCAD FEM simulations.
- Enrich my knowledge regarding the operation mechanisms of an IGBT.
- Understand the failing mechanisms occurring on an IGBT, specifically under short-circuit conditions.
- Deliver a thesis of high scientific standard.

1.5 Organization of the report

This thesis is divided into 5 chapters. In this chapter an introduction on IGBTs is performed; the basic operational principles as well as the main reliability concerns are presented. Afterwards, in Chapter 2 the process for developing the IGBT model is presented. Here, an analysis for the chosen parameters is provided alongside the static performance of the modeled device. The transient characteristics of the developed device both under normal and abnormal conditions are provided in Chapter 3 and an extended analysis regarding the operation under short-circuit failure is given. In Chapter 4 the gate voltage oscillations are discussed and a sensitivity analysis on the stray parameters apparent on every IGBT is performed towards triggering such gate voltage oscillations. Finally, in Chapter 5, a summary of the work performed during this thesis is provided as well as suggestions for future work. In Appendix A the code written for simulating the device under all various conditions is provided, optimized for performing each task.

Chapter 2

Determination of the IGBT model

The end-goal of the thesis is to create an IGBT model for simulating the device under normal and abnormal conditions. Special focus is given on the simulation of short circuit conditions. The reliability of high power transistors against short circuit faults is of high priority for the safe operation of a converter. The robustness under such conditions and the possible triggering failure mechanism of high frequency oscillations at the gate-emitter voltage is of great importance. Therefore, towards gaining deeper knowledge on the behavior of the IGBT under such conditions, FEM simulations are performed.

During short circuit, gate voltage oscillations are systematically observed and it is intended through these simulations to gain insight regarding the cause of appearance. Such a simulation can also provide details on the operation of the IGBT that would be impossible to be obtained experimentally (i.e. Electric Field, Hole and Electron current dissociation etc.).

The IGBT simulated consists of a half-IGBT cell that was used for characterizing the behavior of a 3.3 kV IGBT. The approach was to create a Trench Gate Punch Through IGBT which was calibrated to fit the characteristics of the single cell planar IGBT 5SMX 12M3300 from ABB. The idea is to have a device with similar characteristics but with different internal geometry, in order to investigate the difference on the short circuit behavior and to allow for further investigation on how the geometry of the oxide affects the generated oscillations. In order to define a device that has similar characteristics as the planar IGBT, a series of steps were followed, as these will be described in this chapter.

An overview of the difference between the planar and trench gate IGBTs has been presented briefly in the introduction, but it will be described more in depth hereby. As shown before, the gate oxide is placed on a vertical direction, on the borders of the P_{Base} region. This way, the MOSFET channel is formed alongside the vertical oxide with the length of the channel being larger compared to the planar gate geometry. With the increase of the length, the conductivity modulation is improved, a higher carrier injection is thus achieved leading to the reduction of the on-state resistance [4]. This improvement to the on-state voltage

drop does not affect the turn-off tail current behavior. It has also been reported that trench gate IGBTs have a higher breakdown voltage, in comparison to the planar ones [9]. Finally, the safe operation area of the trench gate IGBT is increased, as due to the lower channel resistance, a thyristor latch-up occurs under more sever occasions.

2.1 Introduction to the TCAD Sentaurus Software

For the modeling of the IGBT device and characterization of the device under various conditions, which is the main goal of the present thesis, the Sentaurus suit will be utilized. Sentaurus suit offered by Synopsys is a TCAD (Technology Computer-Aided Design) suit for performing semiconductor physics FEM (finite element) simulations. A brief presentation of this suit will be provided hereby. In this suit the ability to create a simulation chain that starts with the simulation of the fabrication process up to ultimately evaluating the thermal, optical and electrical behavior of the device under complex electrical circuit configurations is provided allowing thus to fully comprehend the internal mechanisms of a complex semiconductor device.

For this purpose, the suit consists of various programs each of which performs a certain task in the simulation link. The tools that have been used during the current thesis are presented briefly here.

- *Sentaurus Structure Editor:* With this tool, 2D and 3D semiconductor structures can be created by two means, a graphical user interface (GUI) or by scripting. Additionally to that, the doping profiles are defined and the meshing of the device for performing the finite element simulation is determined. Finally, a TDR grid file is generated, which contains the necessary information for the geometrical properties, doping concentrations and device meshing [10].
- *Sentaurus Device:* This software is used for simulating the electrical behavior of the semiconductor device, generated by the previously described software. It is possible to simulate the device under three different conditions (i.e., single device, single device with external circuit or multiple devices connected to auxiliary circuit elements), as depicted in Figure 2.1. For determining the device currents, voltages and internal characteristics, the device equations have to be solved. For this process, an extensive set of models for device physics and effects in semiconductor devices (drift-diffusion, thermodynamic and hydrodynamic models) are available [11].
- *Sentaurus Visual and Inspect:* Sentaurus Visual and Sentaurus Inspect allow for the visualization of the data that have been simulated by Sentaurus Device. The data can be plotted and stored in comma separated values for post-simulation analysis. With

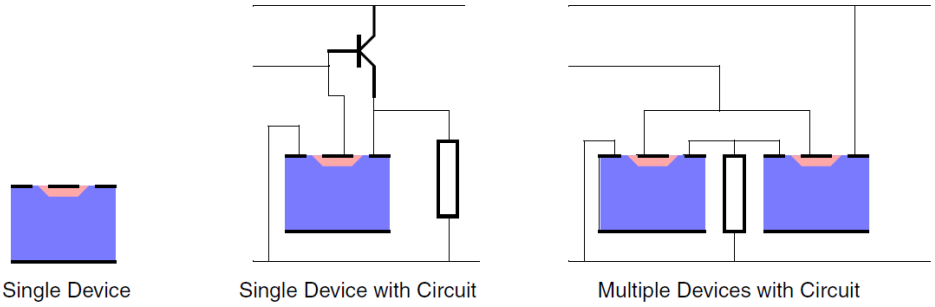


FIGURE 2.1: The three types of circuit simulation possibilities within Sentaurus Device.

the Visual tool, it is also possible to plot the desired characteristics alongside a device cross-section and determine how certain parameters evolve along 2 or 3 dimensions (depending on how many axis are being simulated) [12, 13].

- *Sentaurus Workbench:* It consists of a graphical environment in which the above mentioned tools can be displayed and executed. In this way, the user is able to visualize all the information about the simulated device in a more organized way.

Although TCAD includes a multitude of different programs, such as for simulating the manufacturing process for a semiconductor device, for analyzing its optical properties and more, only the aforementioned tools have been used in the current thesis.

2.2 The base model utilized for generating the IGBT model

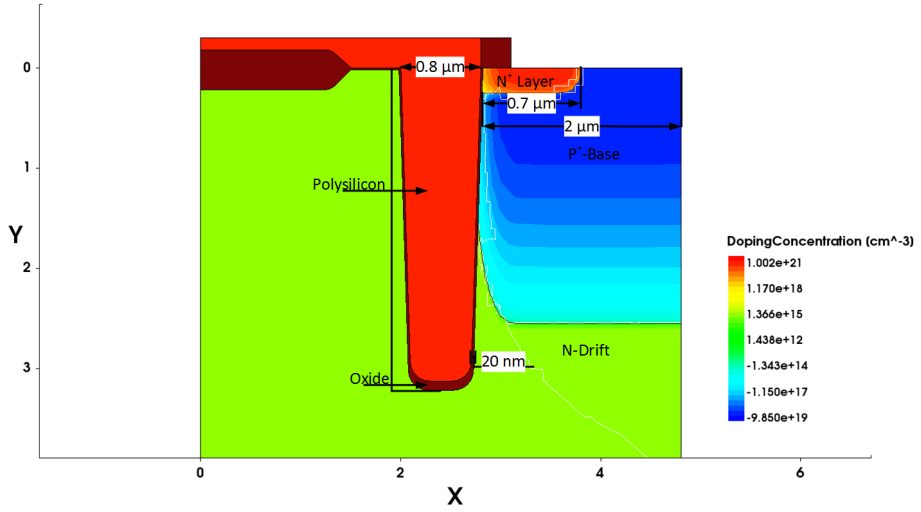
At the starting point of this work, the main circuit and design parameters of the planar 3.3 kV IGBT from ABB were unknown. Therefore a Trench Gate IGBT with similar electrical characteristics to the real device has been developed during this master thesis. This approach is followed for two main of reasons. Firstly, this IGBT model is being used in the ongoing research regarding the short-circuit behavior, thus a comparative evaluation of the mechanisms governing each of the IGBTs will be able to be performed. Secondly, the manufacturing characteristics and model of the planar IGBT are confidential to ABB and therefore these data are not available for creating an accurate model identical to that of the original device. Therefore, an IGBT is developed solemnly based on the datasheet data publicly available. The original device is a single chip IGBT with a die area of 109.8 mm^2, a blocking capability of 3.3 kV and a nominal current rating of 50 A.

For developing the IGBT according to the above specifications, a demo model of the Sentaurus TCAD suit [14] was utilized and modified accordingly and will be briefly presented here. A cross section of the demo device is depicted in Figure 2.2. It is a Trench Gate Punch Through IGBT, in a half cell topology for allowing the simulation to be performed faster.

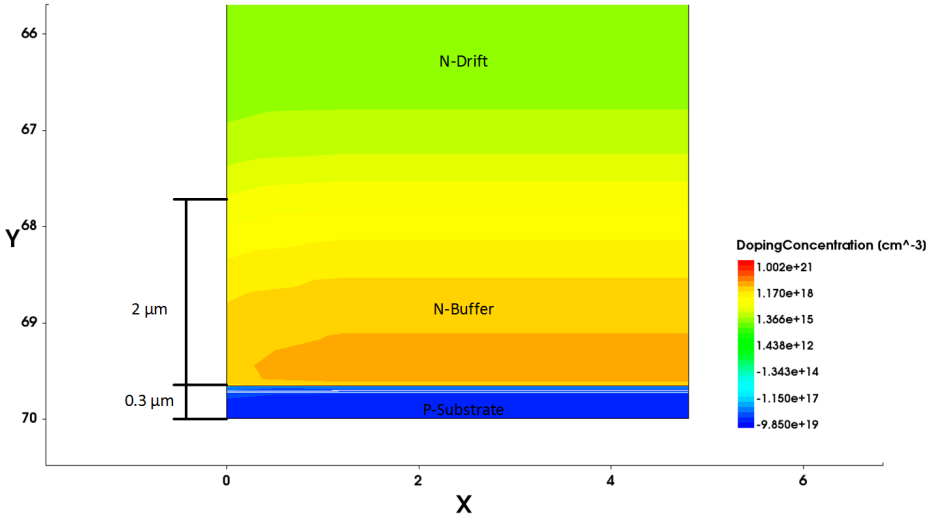
Its static characteristics are presented in Figure 2.3 and from these, we can deduce that it is a device able to block up to 250 V (Figure 2.3c), rated for approximately 40 - 60 A collector current (Figure 2.3b) and with a threshold voltage of 2.5 V (Figure 2.3a). The total width of the device is 70 μm and the doping profiles for each of the regions are presented in Table 2.1.

TABLE 2.1: Doping profiles of the demo device.

Region	Doping (cm^{-3})
N^+ region	10^{21}
P_{Base} region	1.2×10^{21}
N_{Drift} region	10^{13}
N_{Buffer} region	10^{19}
P^+ region	10^{20}



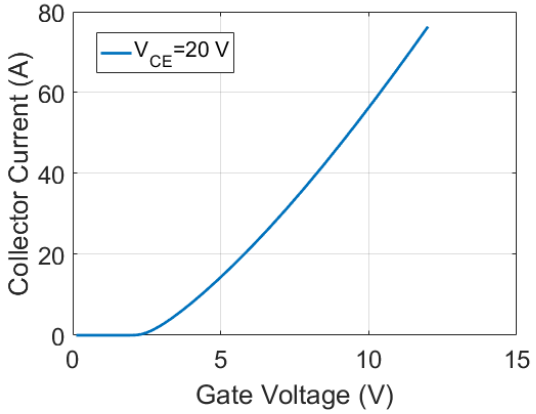
(A) Emitter side of the demo TCAD IGBT.



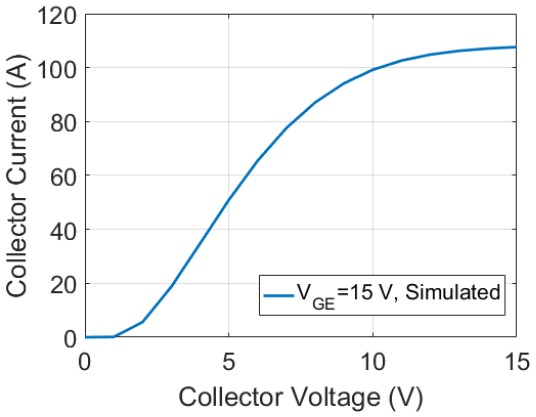
(B) Collector side of the demo TCAD IGBT.

FIGURE 2.2: Demo TCAD IGBT model, geometrical properties.

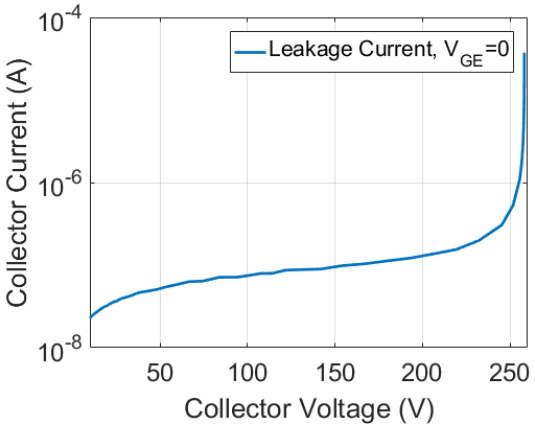
It becomes obvious from the presentation of the demo device, that it's characteristics are far from the desired single cell model, with the desired blocking voltage being more than one



(A) Collector current versus gate-emitter voltage.



(B) Collector current versus collector-emitter voltage.



(C) Leakage Current

FIGURE 2.3: Static characteristics for temperature of 300 K of the Demo TCAD IGBT model.

order of magnitude higher and although the nominal current is around the value of the demo model, the on-state voltage drop for this device for collector current of 50 A is far higher than the desired one. It will also become apparent in the next section that a substantial mismatch is present for the threshold voltage. For these reasons, based on this model, an extensive series of iterations were performed for fitting the characteristics of the 3.3 kV IGBT device. The process followed towards achieving this goal will be presented in the next sections. It will become clear to the reader that the initial model, the demo one, and the final IGBT model will have only in common the Trench structure, but all the doping profiles and the rest of the geometries had to be altered.

2.3 Blocking Capability Characterization

Initially, the N-drift region was altered, aiming for a higher voltage rated device, since the demo device is a low voltage one. The idea that was followed was to find the appropriate combination of doping concentration of the N-drift region and its width up to the point that

the the device would be able to support 3.3 kV. The blocking capability of the device is easy to be defined by finding a good combination between N-drift width and doping, however, the resulting IGBT may not be well optimized in terms of on-state characteristics. This is because the doping concentration of the drift region also affects the on-state characteristics. Additionally to that, the electric field at the punch-through region is key factor to the turn-off tail current time constant. Therefore, extensive iterations were performed for defining the combination of those two parameters.

When the device is in the blocking state, there are three junction regions as seen in Figure 2.4. Junctions J1 and J3 are forward biased and only junction J2 is reverse biased, determining the blocking capability of the device. The maximum electric field that a silicon PN junction can support is 3 10^5 V/cm at a temperature of 300 K, at which an electron multiplication process (avalanche) takes place [4]. A second phenomenon that takes place during the breakdown of the IGBT is the punch-through breakdown, occurring when the depletion layer width penetrates into the emitter contact, resulting to injection of holes from the emitter towards the collector [15].

The two main parameters that define the forward blocking capability of an IGBT are the drift region doping and the drift region width. The maximum electric field in a parallel plate topology, for a constant voltage, is decreasing as the distance of the plates is increasing. According to Poisson's law the electrical field generated by the charge distribution in the drift region due to the donor concentration creates a linearly increasing electrical field, $\frac{E}{dx} = \frac{qN_D}{\varepsilon_0 \varepsilon_s}$, where E is the electric field in the drift region, q the electron charge, N_D the donor concentration, ε_0 the vacuum permittivity and ε_s the silicon relative permittivity. By integration of the previous equation, it is obtained that the maximum electric field appearing due to the charge concentration in the drift region, is dependent both on the donor concentration as well as the width of the drift region according to $E_{max} = \frac{qN_D}{\varepsilon_0 \varepsilon_s} W$. Therefore, it can be seen that the maximum electric field appearing in the bulk silicon region is increasing with the increase of the doping concentration of the drift region and decreases with the width (W) of the drift region, up to a certain point since the effect of the width to the Poisson equation has also to be accounted for. This is a simplified approach to the breakdown mechanism, as this mechanism is much more complex, taking into account the doping of the other regions, as well as the charge life times and electron and hole mobilities.

A complete analysis of the breakdown mechanism is out of the scope of this report and the above analysis is given in order to present the qualitative effect of the two dominant factors to the characterization of the blocking voltage. The approach that was followed in order to create a device capable of blocking 3.3 kV, was to keep constant the drift doping concentration, to the value of 1.24×10^{13} phosphor atoms cm^{-3}, a reasonable doping concentration for which a good on-state voltage drop was achieved with the combination of the N-buffer and P^+-substrate doping concentrations. Afterwards, the width of the drift region

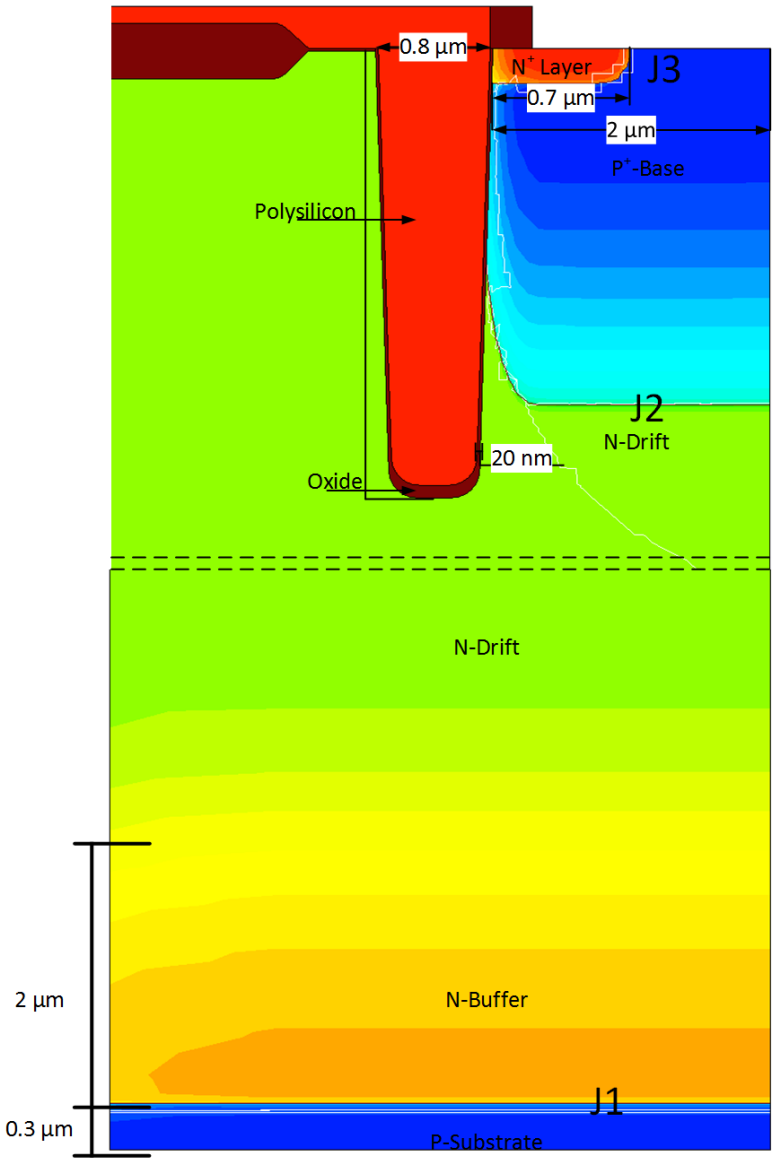


FIGURE 2.4: The three PN junctions apparent on an IGBT.

was increased, until the desired blocking capability was achieved and further beyond, as the electric field value at the buffer region during the blocking state showed to affect the turn-off characteristics. Finally, the total width of the device was set at 325 μm.

The leakage current versus collector-emitter voltage, when the device is in the off-state is shown in Figure 2.5, where it can clearly be seen that after $V_{CE} = 4560$ V a sharp rising of the collector current is initiated. The breakdown voltage is substantially higher than the rated blocking voltage of the target device, allowing for the device to operate well up to 3.3 kV without any initiation of the breakdown mechanisms. The electric field at the rated V_{CE} voltage of 3.3 kV can also be seen in Figure 2.6. This field is depicted in the vertical path on the device which starts from the emitter contact, far from the gate trench and the

device limits, in order to avoid the interference due to edge effects, and ends at the P^+-substrate region at the collector terminal. It can be seen that the electrical field shapes in a trapezoidal way as presented in the literature [16] for a punch-through device. For generating these results, the simulation code generated is given in the appendix, subsection A.2.1.

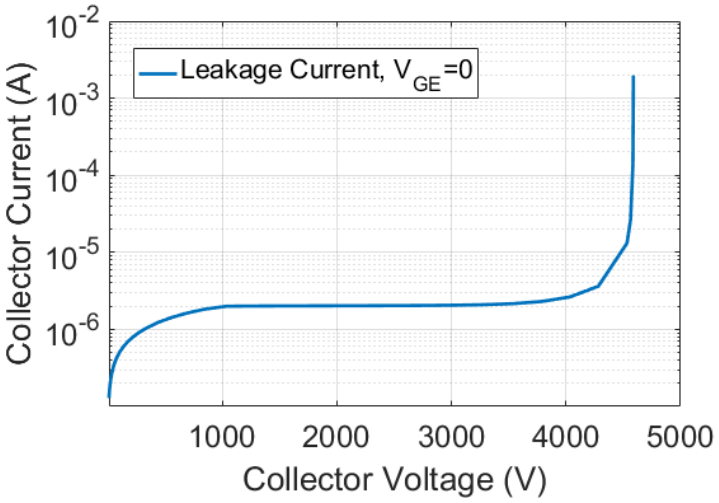


FIGURE 2.5: Collector current with rising voltage, when the IGBT is in the off-state.

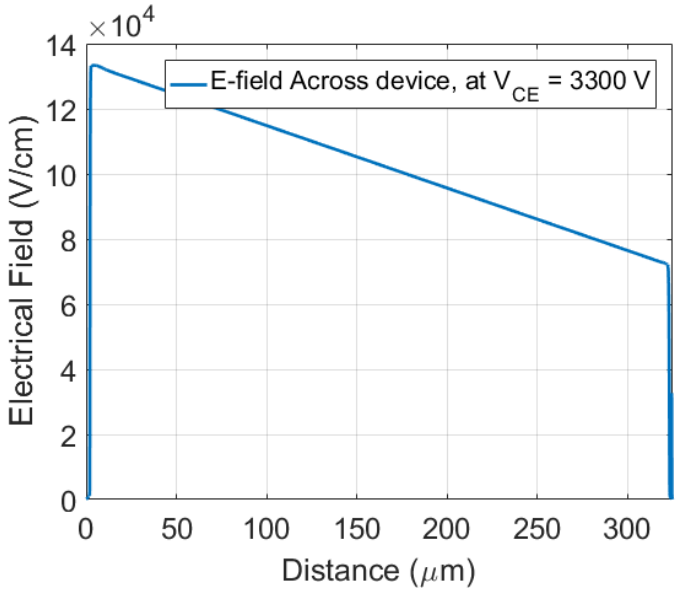


FIGURE 2.6: Electric field across a vertical path of the device.

If the electric field is obtained across the line that crosses also the J3 junction, close to the gate trench, it can be seen that it obtains high values. For the breakdown voltage, as seen in Figure 2.7, the electric field reaches a magnitude close to the silicon junction breakdown limit and at this high E-field value, the avalanche mechanism results to the increase of the current.

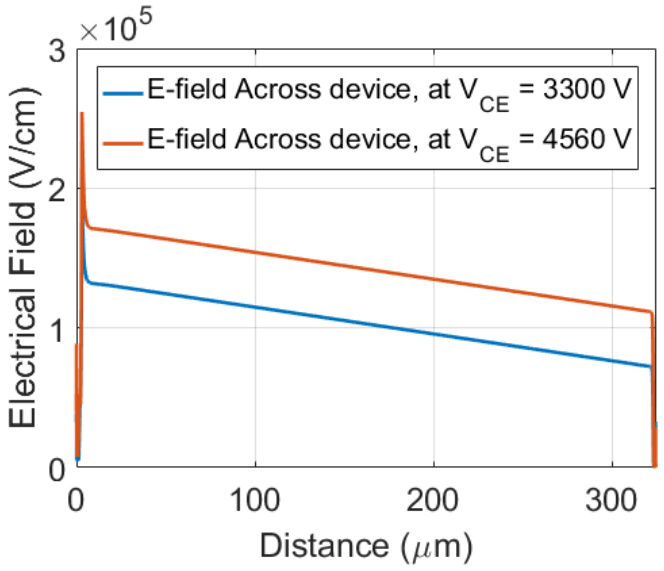


FIGURE 2.7: Electric field across a vertical path of the device, tangent to the gate trench.

2.4 Threshold Voltage Characterization

As it was shown in the introduction, it can be assumed that the IGBT is modeled as a N-MOSFET connected with a PNP BJT in a Darligton configuration as seen in Figure 1.1. Then, the threshold voltage as well as the the correlation of the collector current to the gate-emitter voltage for a specific collector-emitter voltage ($I_C - V_{GE}$) is dependent mainly by the MOSFET characteristics. For this reason, in the current analysis only the MOSFET part of the IGBT is studied.

When the gate-emitter voltage is well above the threshold voltage of the MOS-channel, the channel emits electrons through the inversion layer at the P^+_{base} into the N-Drift region. The MOS-channel is generated when the surface potential at the P^+_{base} area is greater than 2 times the balk potential ψ_B increased by the surface charge divided by the gate oxide capacitance, Q_s/C_{ox}. Also, the work function between the gate metal and the the semiconductor, ϕ_{MS}, must be taken into account, and therefore, the threshold voltage equation becomes [4],

$$V_{th} = \phi_{MS} + 2\psi_B + \frac{Q_s}{C_{ox}} \tag{2.1}$$

This equation is a general equation when no impurities between the oxide and the P^+_{base} region are apparent, which is the case for the simulated IGBT model. Such impurities exist in real IGBTs and include charge in the $Si - SiO_2$ interface in the form of fixed charge, interface-state charge and mobile ion charge.

From the application of Poisson's equation at the P^+_{base} region, the bulk potential is calculated to be,

$$\psi_B = \frac{kT}{q} ln \frac{N_A}{n_i} \tag{2.2}$$

and the surface charge is given by the equation,

$$Q_s = \sqrt{4\varepsilon_0 \varepsilon_s kT N_A ln(N_A/n_i)} \tag{2.3}$$

The oxide is given as the capacitance per unit area and is,

$$C_{ox} = \frac{\varepsilon_0 \varepsilon_{ox}}{t_{ox}} \tag{2.4}$$

where ε_{ox} is the dielectric constant of the SiO_2 and t_{ox} is the thickness of the gate oxide.

By substituting in Equation 2.1, the Equations 2.2, 2.3 and 2.4 the equation for the threshold voltage becomes,

$$V_{th} = \phi_{MS} + \frac{2kT}{q} ln \frac{N_A}{n_i} + \frac{t_{ox}\sqrt{4\varepsilon_0 \varepsilon_s kT N_A ln(N_A/n_i)}}{\varepsilon_0 \varepsilon_{ox}} \tag{2.5}$$

where k is the Boltzmann constant, T the temperature in K, q the elementary charge, N_A the acceptor concentration of the P^+_{base} region and n_i the intrinsic carrier concentration.

A thorough analysis of the derivation of the aforementioned equations will not be performed and can be found in literature [1, 4]. The threshold voltage equation (Equation 2.5) is presented, in order to show that, for a specific temperature, the threshold voltage is primarily controlled by only two factors, the acceptor doping of the P^+_{base} and the oxide thickness, increasing with the increase of both factors.

For fitting the 3.3kV IGBT device, the gate oxide was set to be $t_{ox} = 50\ nm$, which is a typical value for devices of this power rating, and therefore the acceptor doping concentration was adjusted accordingly until the threshold voltage matched the targeted device. This was achieved at a concentration of $P^+_{base} = 8 \times 10^{19}$ arsenic atoms cm^{-3}. Figure 2.8 shows that the simulated IGBT model matches the data acquired from the device datasheet. In Figure 2.9 the $I_C - V_{GE}$ curves are shown for different P^+_{base} region concentrations, showing the strong dependency between the doping concentration and the threshold value as it can be seen in Equation 2.5. The code for simulating the behavior of the device for constant V_{CE} voltage, while sweeping the V_{GE} voltage, can be found in the appendix, subsection A.2.2.

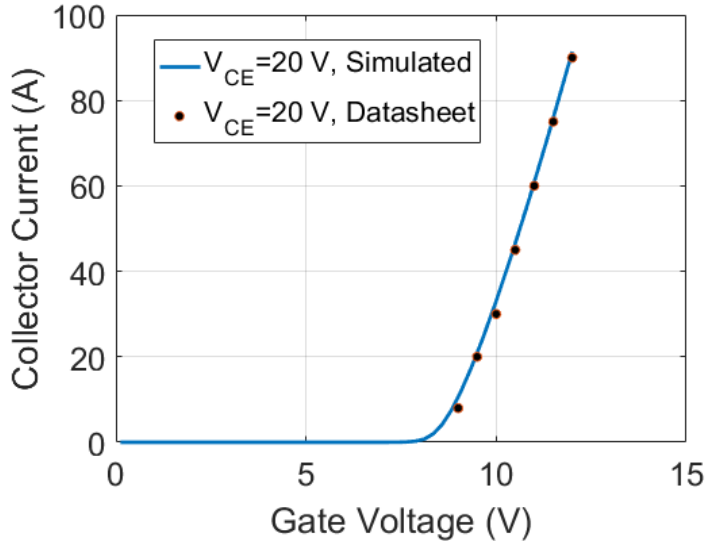


FIGURE 2.8: The collector current (I_C) versus the gate voltage (V_G) for temperature of 300K.

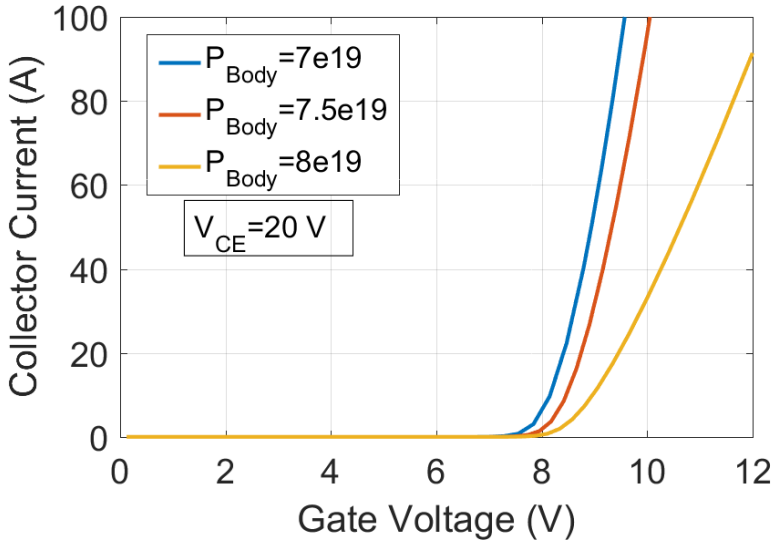


FIGURE 2.9: The collector current (I_C) vs the gate voltage (V_G) for temperature of 300K.

Additionally, in Figure 2.10 the transconductance of the device is presented hereby, which is relevant to the transient characteristics of the device.

2.5 On-state behavior Characterization

For analyzing the on-state behavior of the IGBT, it will be modeled as a N-MOSFET connected with an PNP BJT in a Darligton configuration, as before. In the case where only the PNP bipolar transistor part of the IGBT is considered, the equation that describes the relationship between the collector and the base current of the PNP is given

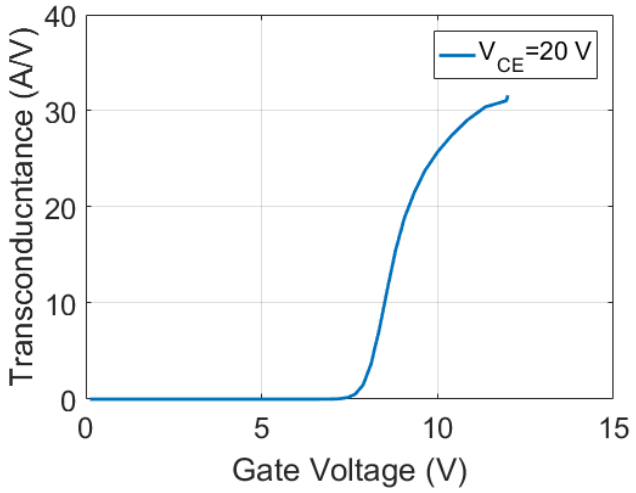


FIGURE 2.10: Transconductance of the simulated 3.3 kV IGBT for temperature of 300 K.

as $I_{C,PNP} = \frac{\alpha_{PNP}}{1-\alpha_{PNP}} I_{B,PNP}$, with α_{PNP} being the PNP efficiency, with the collector of the PNP transistor being the emitter of the IGBT. From the equivalent electrical circuit as depicted in Figure 1.1, $I_{E,IGBT} = I_{C,PNP} + I_{B,PNP} = \frac{1}{1-\alpha_{PNP}}$, therefore by assuming constant base current regulated only by the N-MOSFET, an increase to the efficiency results to increase in the IGBT emitter current.

The efficiency of the PNP transistor, also called common-base current gain, is given by three factors, the Emitter injection efficiency (γ), the Base transport factor (α_T), which is the dominant factor for the efficiency [16] and the Collector multiplication factor (M), which for small V_{CB} voltage can be neglected. The equation that correlates those three factors is $\alpha_{PNP} = \gamma \alpha_T M$. The coefficient γ is given by the following equation [1, 4],

$$\gamma = 1 - \frac{D_E}{D_p} \frac{N_B}{N_E} \frac{W}{L_E} \tag{2.6}$$

where D_E is the electron diffusion coefficients in the emitter and D_p the hole diffusion coefficient, N_B and N_E the doping concentrations of the base and the emitter respectively, W the width of the base and L_E the electron diffusion length in the emitter.

The Base transport factor (α_T) is related to the base characteristics according to the equation,

$$\alpha_T = 1 - \frac{W^2}{2L_B^2} \tag{2.7}$$

with L_B being the the electron diffusion length in the base.

By assuming that varying the emitter doping concentration within small margins, the rest of the parameters remain unchanged, it can be derived that an increase in the emitter (collector for the IGBT) doping density results to an increase of the PNP efficiency. Therefore, for

the same external conditions of the IGBT, such an increase indicates an increase in the collector emitter current, which can be seen in Figure 2.11. With this in mind, the acceptor concentration in the P^+ substrate region of the IGBT is one of the dominant variables determining the I_C - V_{CE} characteristics of the simulated IGBT.

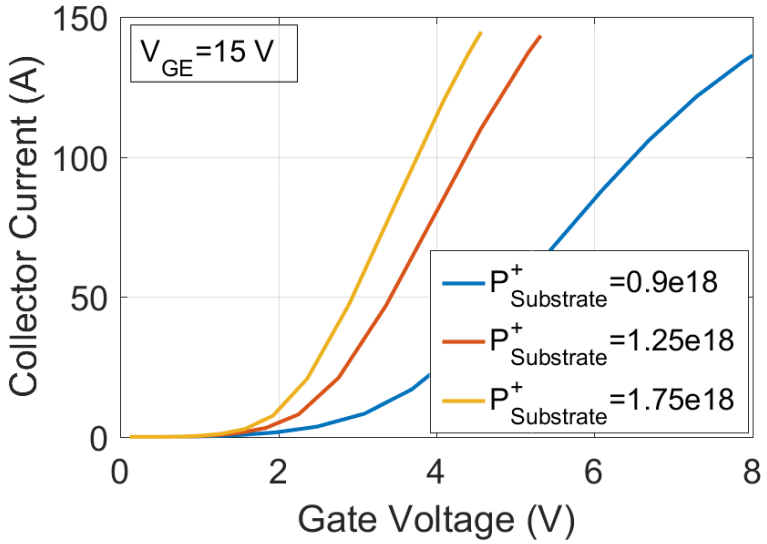


FIGURE 2.11: The collector current (I_C) vs the collector voltage (V_C) for various doping concentrations.

The above analysis is true for non-punch-through (NPT) IGBT designs, as in this case no buffer layer is apparent, determining the transport factor from the IGBT collector side towards the drift region. As discussed above, the transport factor a_T is a crucial parameter in determining the PNP efficiency (a_{PNP}). The PNP efficiency alongside the buffer layer role in recombining the minority carriers indicate that the N-buffer layer and P-substrate layer doping concentrations cannot be decided, without taking the switching characteristics under consideration. The additional role of the N-buffer layer to the turn off characteristic, and more importantly on the tail current and its effect in the carrier recombination can be summarized in Equation 2.8 where the carrier lifetime is taken into account [17],

$$i_C(t) = i_C(0) exp \frac{(a_{PNP} - 1)t}{\tau_D a_{PNP}} \tag{2.8}$$

where, τ_D is the drift area carrier lifetime.

In Equation 2.8, it can be seen that the turn-off tail current, as it relies in the recombination of the minority carriers, it is influenced by the carrier lifetime on the drift region. This is an additional factor for characterizing the turn-off transient response. On the other hand, the carrier lifetime is a key factor to the on-state voltage drop, its reduction resulting to the increase of the on-state losses, as shown by the Figure 2.12. In this figure, only the maximum hole lifetime was altered resulting to a mean hole lifetime as calculated by Equation 2.9. The turn-off time was extracted from the simulations that are being described in section 3.1.

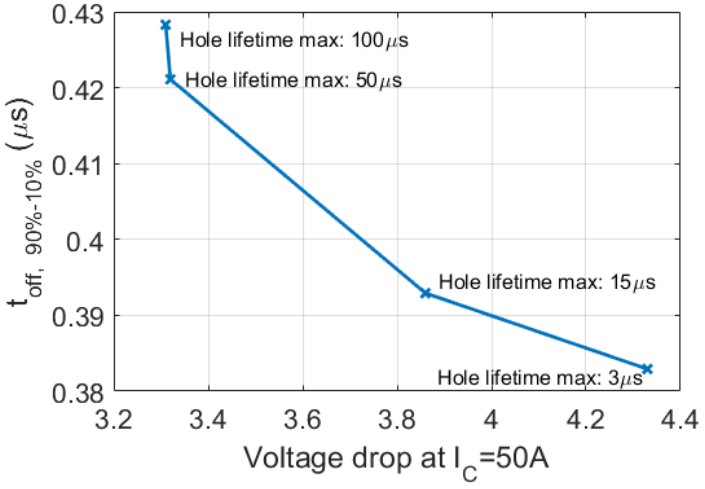


FIGURE 2.12: Effect of carrier lifetime to the on-state voltage drop and turn-off time.

Additionally to the above, the area of the IGBT cell is a crucial parameter to be defined in order to design a device capable of handling the same current levels as the targeted device with similar on-state losses. The designing of the device is taking place in the 2D domain, so in order to add depth to the model, Sentaurus is assuming automatically a 1 μm of depth. In order to achieve the desired area, equal to the target die area, A=109.8 mm^2, a piece of code is added at the simulation level called "AreaFactor", which represents the area multiplication factor. The value of the multiplier is another parameter to be determined and is of significant importance for the correct representation of the device behavior. Increasing the area only by a multiplier could be viewed as paralleling a high number of IGBT cells with the default depth of 1 μm. This way, the IGBT capacitances (C_{CE}, C_{GE} and C_{CG}) are also placed in parallel, increasing in direct analogy with the "AreaFactor". It is for this reason that it was chosen before determining the value of this multiplier, to increase the cell breadth from 4.5 μm (demo device) to 25 μm, reducing thus the multiplier needed for achieving the same die area to 4.4×10^6.

The number of parameters responsible for the on-state behavior, as well as the the effect that each of these parameters have to the transient characteristics, makes the determination of those quite cumbersome. The determination of the final value for each of these parameters required an extensive number of iterations and reevaluation of the performance of the transient and static behavior of the device. Finally, after all the parameters have been determined, the on-state behavior of the designed IGBT is presented in Figure 2.13. The code for simulating the behavior of the device for constant V_{GE} voltage, while sweeping the V_{CE} voltage can be found in the appendix, subsection A.2.3.

Figure 2.13 also shows that for a gate voltage at $V_{GE} = 15$ V the collector current saturates at approximately 205A. This value is important for the following short circuit analysis, as the device operates in the saturation region during short circuit.

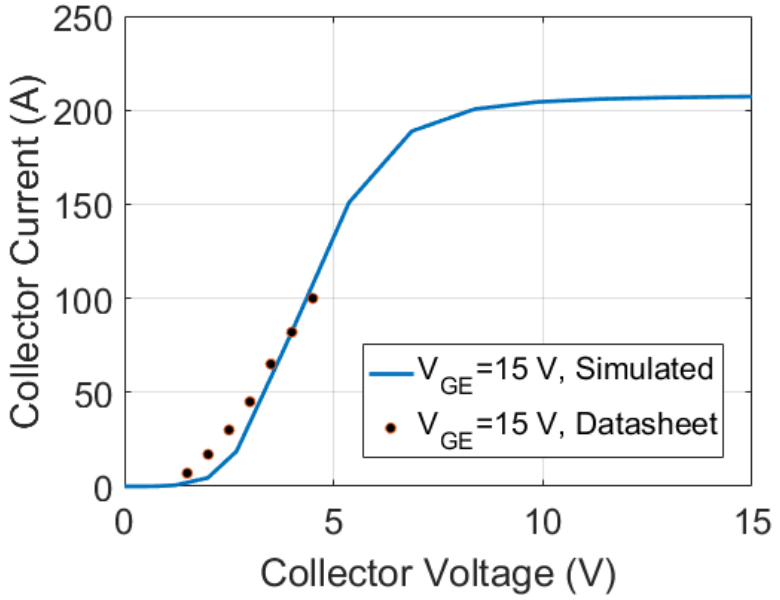


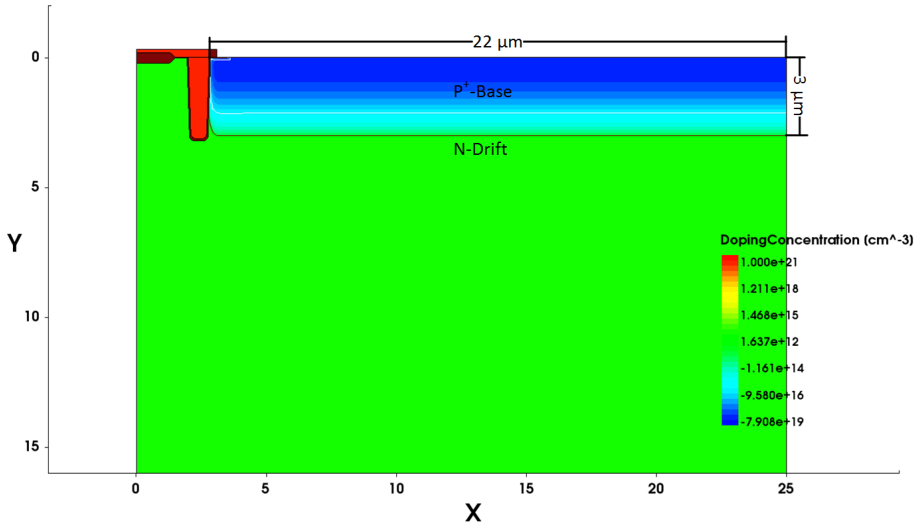
FIGURE 2.13: The collector current (I_C) versus the collector voltage (V_C) for temperature of 300 K.

2.6 Device Overview

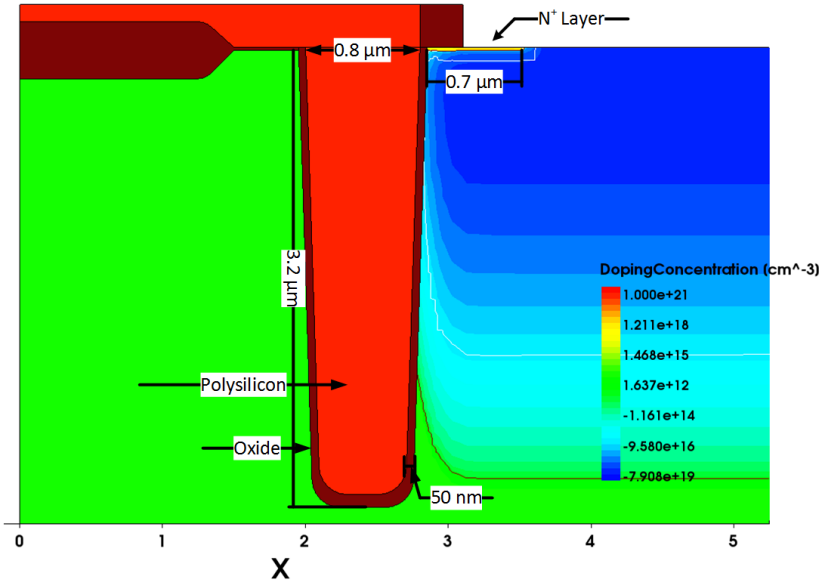
According to the analysis conducted on the previous sections, an IGBT was designed approximating the characteristics of the planar IGBT (5SMX 12M3300) and is that model that will be used for the short circuit simulations that will be presented in the following chapters. The geometrical properties of the developed device are depicted in Figure 2.14. The oxide thickness was increased to 50 nm as shown in Figure 2.14b, the breadth of the cell was increased to 25 μm as presented in Figure 2.14a and the total width of the IGBT cell was increased to 325 μm as indicated in Figure 2.14c.

The properties of the device, regarding its doping concentrations are presented in Table 2.2. It has to be noted that for determining the doping concentrations, the transient behavior of the device was also taken into consideration. The graphs for fitting the transient behavior of the modeled device to that of the 3.3 kV planar IGBT were obtained from simulations performed at Aalborg University, which have previously been fitted to the real device. The doping values that are presented here were chosen not only for simulating static characteristics similar to the target device, but also for achieving similar turn-on and turn-off transient times, as this will be discussed in the next chapter.

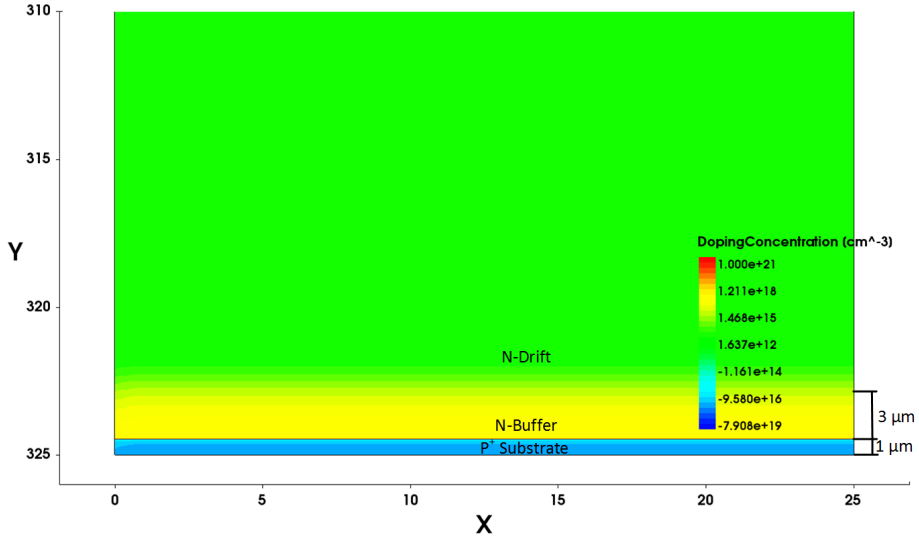
The carrier lifetime is an additional parameter that controls the on-state behavior of the device as well as the turn-off current tail of the device. In the developed model, the carrier lifetime is not constant throughout the entire device, but is dependent to the doping concentration according to the Scharfetter relation, Equation 2.9.



(A) Emitter side of the designed IGBT.



(B) Trench gate focus of the designed IGBT.



(C) Collector side of the designed IGBT.

FIGURE 2.14: Designed IGBT, geometrical properties.

TABLE 2.2: Doping profiles of the designed device.

Region	Doping (cm^{-3})
N^+ region	8.056×10^{19}
P_{Base} region	8×10^{19}
N_{Drift} region	1.24×10^{13}
N_{Buffer} region	4×10^{17}
P^+ region	1.25×10^{18}

$$\tau_{lifetime} = \tau_{min} + \frac{\tau_{max} - \tau_{min}}{1 + \frac{N_A + N_D}{N_{ref}}} \tag{2.9}$$

where τ_{min} is a minimum lifetime allowed as a carrier lifetime, τ_{max} the constant lifetime utilized when no doping dependency is chosen, N_A the acceptor concentration, N_D the donor concentration and N_{ref} a reference doping concentration deduced from experimental data.

The default value for N_{ref} both for holes and electrons is 1×10^{16} cm^{-3}. For both carriers, as τ_{min} was chosen 0, whereas for holes the value of τ_{max} was evaluated to be 50 μs and for electrons 10 μs.

With all the above parameters defined, the IGBT model was established and simulations regarding its behavior in time under normal and short circuit conditions will be performed in the following chapters.

Chapter 3

Transient behavior of the IGBT under normal and short circuit conditions

Short circuit failure mode is an operation mode of the IGBT at which it operates under saturation current at voltages many orders of magnitude higher than the on-state voltage drop, during normal operation. Before evaluating the short circuit performance though, it is important to assure that the characteristics of the developed device are similar to the targeted one, not only regarding to the static performance, but also to the transient. This way, the good fitting of the device characteristics in total (both static and transient) is assured. Thus, good correlation of the developed model in terms of short circuit behavior to the targeted one can be expected.

3.1 Transient Behavior characterization

The IGBT that will be used for the simulations hereafter was defined in the previous chapter and its static characteristics were presented in full. For obtaining the complete picture of the performance of the device under normal conditions, the transient behavior of the IGBT will be presented.

The common setup used for experimentally evaluating the turn-on and turn-off curves of a power device, is called double pulse test. This setup is presented in Figure 3.1 and it's operation will be described here briefly.

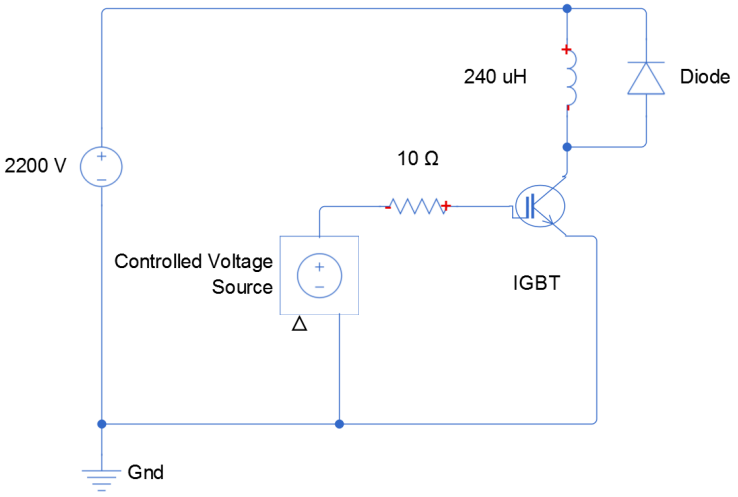
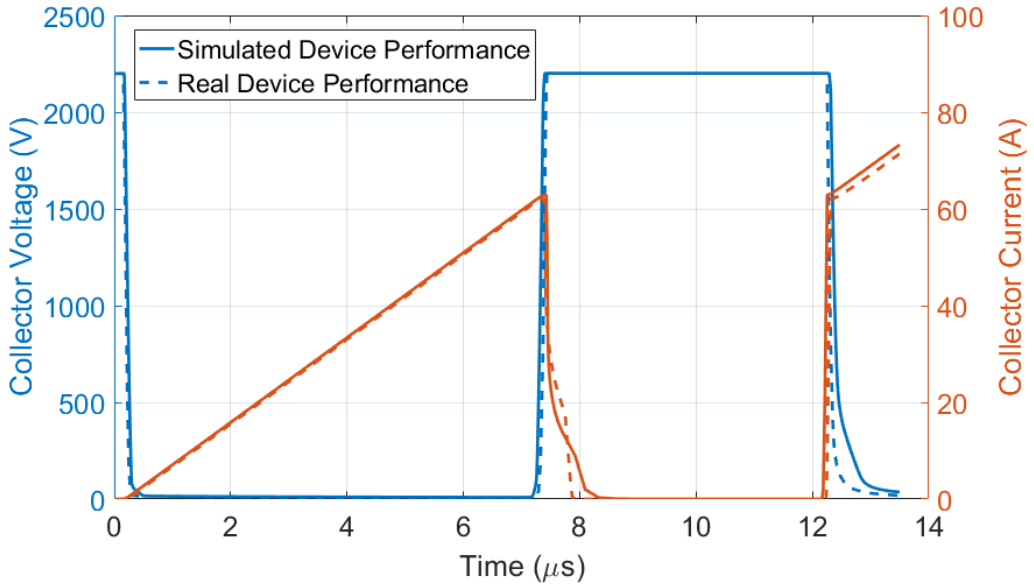


FIGURE 3.1: Schematic of the double pulse test setup.

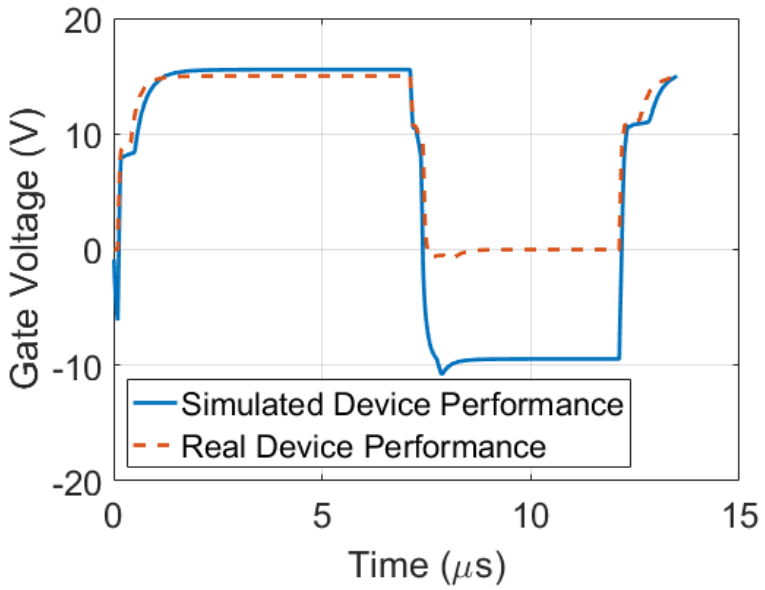
When the IGBT is first turned on, current is building up in the inductor according to $I_C = \frac{1}{L} \int_0^{t_{pulse}} V_{DC} dt$, when no internal losses to the IGBT are assumed. When the first pulse at the gate terminal goes lower than the threshold voltage, the IGBT is turning off, providing thus the turn-off curves. While the device is in the off state, the current flows through the diode, practically maintaining its value as at the moment of the switching. When the second pulse is provided at the gate terminal, the device is turned on under full load and the turn-on curves are extracted.

It can be seen that no stray elements (stray inductance and resistance) have been included in the simulation scheme, allowing thus to fully evaluate the performance of the generated model. Also, the diode has been modeled as an ideal non-linear element with infinite resistance when in the off state and zero when in the on state.

For evaluating the switching characteristics, the device was simulated under DC-link of 2200 V, a voltage level of approximately 65% of the rated voltage. The gate resistance and the load inductance have been chosen as shown in Figure 3.1. The results of the simulated device alongside the switching characteristics of the target device for this DC-link voltage are shown in Figure 3.2. The code for generating the graph for the transient behavior of the modeled device can be found in the appendix, subsection A.3.1.



(A) Collector voltage and current transient behavior.



(B) Gate voltage transient behavior.

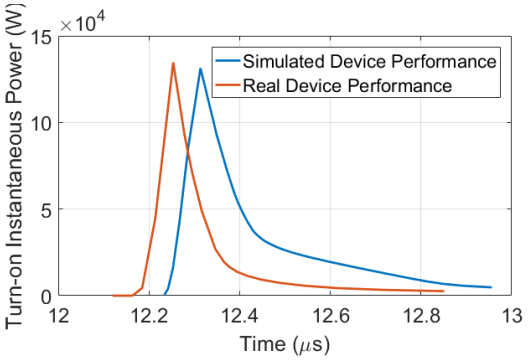
FIGURE 3.2: Switching behavior of the simulated and targeted device for temperature of 300 K.

In those two graphs, a series of remarks can be made. Initially, it can be noticed in Figure 3.2b that the transient response of the gate-emitter voltage matches well that of the targeted device. The plateau appears at the same voltage level as was expected, since a good match regarding the threshold voltage was verified at the previous chapter. It can also be noticed that for the turn-on part, the turn-on of the target device is occurring sooner, as seen both in Figure 3.2a as well as Figure 3.2b. This indicates a bigger gate-emitter and gate-collector capacitance in the modeled device.

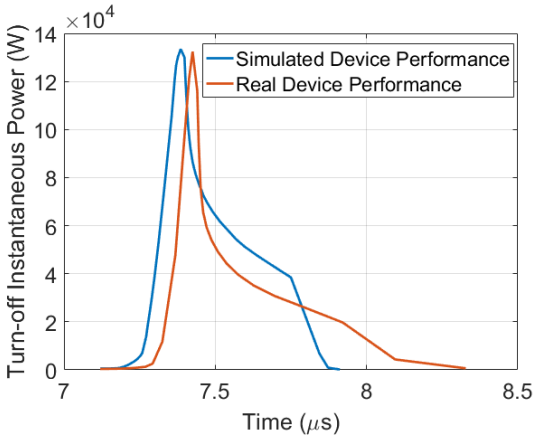
Regarding the turn-on behavior of the modeled device, it can be seen that the V_{CE} voltage is dropping with a higher time constant, indicating a higher collector-emitter capacitance. As for the turn-off behavior, it can be seen that although an extensive series of iterations to the IGBT characteristics was performed for matching the tail current to that of the target device, predominantly to the carrier lifetime and the N-buffer layer doping concentration, a compromise was achieved for the on-state static characteristics and the tail current decay rate.

At this voltage level, a short presentation of the switching energy for this device will be also provided here. Due to the finite time required for the collector current and the V_{CE} voltage to transit from their initial to the final value, i.e. voltage falling and current rising during the turn-on process and vice versa during the turn-off process, an amount of energy is dissipated in the form of heat within the device. This energy is a crucial parameter for a power device, since it is this one that determines the maximum switching frequency of such a device.

The switching losses during the transient behavior for both devices are shown in Figure 3.3. By integration of these two graphs, the turn-on energy of the simulated device is evaluated at $E_{on} = 23.6$ mJ and the turn-off energy, $E_{off} = 33.4$ mJ.



(A) Turn-on switching instantaneous power.



(B) Turn-off switching instantaneous power.

FIGURE 3.3: Switching losses for temperature of 300 K.

3.1.1 Carrier Distribution and Electric Field

During the switching process, two physical mechanisms result to the device being turned on and off. The first one has to do with the conductivity modulation, where the device is flooded with holes and electrons and the second one with the carrier extraction and recombination. These two mechanisms will be analyzed here stepwise along the two switching processes. For this analysis, the same double pulse test discussed above is used, in which several points through the turn-on and turn-off process will be evaluated (Figure 3.4). For each point, the

hole and electron carrier concentrations will be presented alongside the electric field across the IGBT.

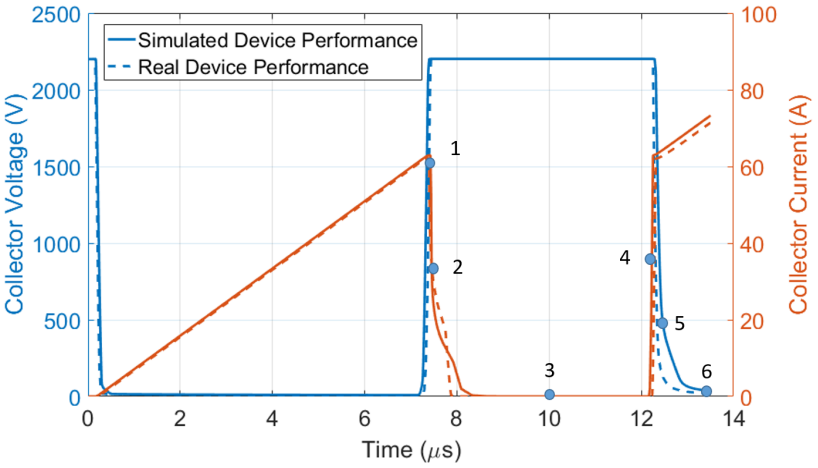


FIGURE 3.4: Points on the transient graph for analyzing the switching procedure.

Point 1:

This phase begins with the application of a gate-emitter voltage value below the threshold voltage of the device, the V_{CE} voltage has already risen close to the DC-link voltage without the current having fallen from its on-state value of 60 A. This point lies at the end of the Miller capacitance C_{GC} charging. It can be seen that the excess carrier concentration at the drift region starts to sweep out and therefore the electric field builds up and gradually penetrates across the drift region until it finds its punch through level. The vertical cross-section for all the following figures is at x=11 μm, approximately in the middle of the emitter contact.

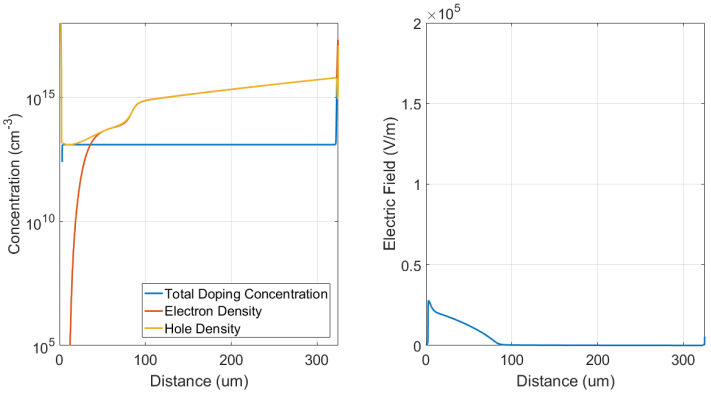


FIGURE 3.5: Hole and electron densities on the left and the corresponding electric field on the right. The device is turning-off (point 1 in Figure 3.4).

Point 2:

The voltage across the IGBT has fully risen to the DC-link potential and the freewheeling diode is conducting. The electric field is developing further towards the collector side and at this point the collector current is determined solemnly by the remaining charge and the recombination rate of holes and electrons. This is the point where the tail current is appearing. The remaining charge to be recombined can be seen in Figure 3.6. The tail current decay rate is governed by the lifetime of the carriers and at the end of this process the device will be at its off state.

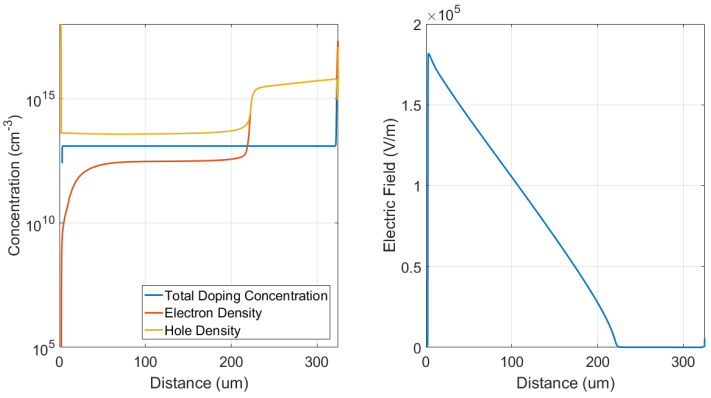


FIGURE 3.6: Hole and electron densities on the left and the corresponding electric field on the right. The device is turning-off (point 2 in Figure 3.4).

Point 3:

The device is now in the off-state. The electric field has the trapezoidal shape shown in the previous chapter, corresponding to the punch-through characteristic of the IGBT. The drift region is depleted of charge as can be seen in the figure below in which the carrier concentrations are below the background doping concentration of the drift region. An electron current through the gate channel is required for the device to enter again its conductive state.

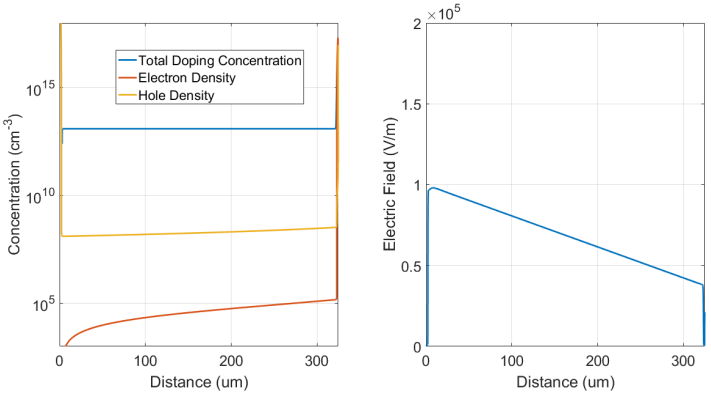


FIGURE 3.7: Hole and electron densities on the left and the corresponding electric field on the right. The device is in the off state (point 3 in Figure 3.4).

Point 4:

At this phase the device begins its turn-on processes, the current begins to flow across the device until it reaches its on-state value. The electrons injected through the MOS-channel into the drift region trigger the injection of holes from the collector towards the drift region. The current conduction path has not fully been flooded with holes and therefore the electric field is developed across the complete IGBT.

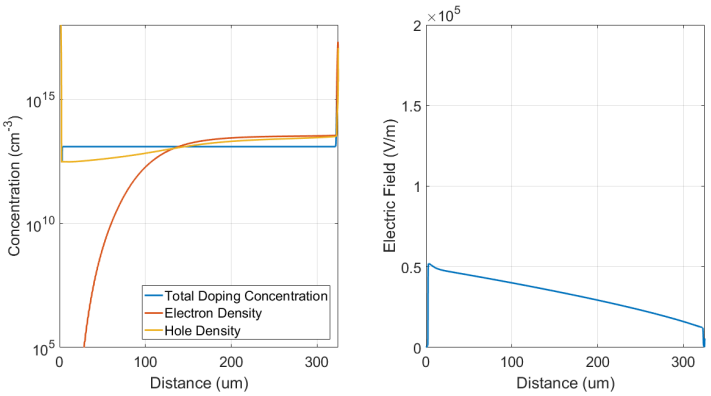


FIGURE 3.8: Hole and electron densities on the left and the corresponding electric field on the right. The device is turning-on (point 4 in Figure 3.4).

Point 5:

At this point the current has already reached its on-state value and V_{CE} voltage drops due to the discharging of the Miller capacitor C_{GC}. The electric field across the device is being reduced significantly and the excess carrier concentration within the device has formed a complete conduction path.

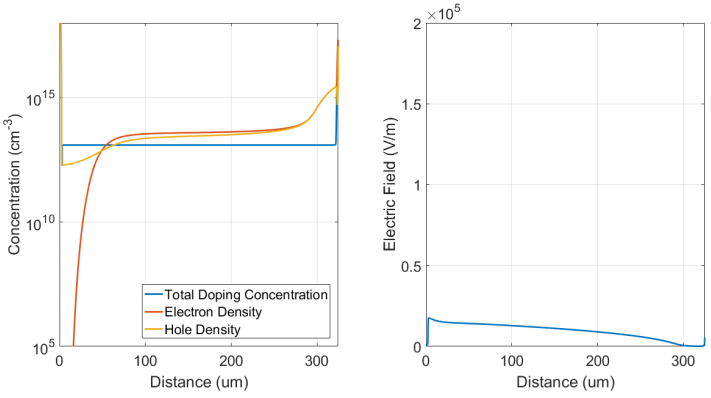


FIGURE 3.9: Hole and electron densities on the left and the corresponding electric field on the right. The device is turning-on (point 5 in Figure 3.4).

Point 6:

The device is completely in its on-state. The V_{CE} has taken its saturation on-state value and the electric field within the device is developed only due to this voltage. The conductive path

within the drift region is fully formulated and an equilibrium is achieved within the electron and hole concentration, $n \backsimeq h$. In Figure 3.11 the current density within the device for the emitter side is provided. The device is in the on-state and it can be observed that the higher density appears at the MOS-channel. This is expected since the full base current of the PNP transistor is passing through this channel, which is tangent to the gate oxide and has a sub μm thickness. The current in the emitter side of the IGBT is allowed to flow through a bigger area, dropping thus the current density from 1000 A/cm^{-3} at the MOS-channel to less than 10 A/cm^{-3}.

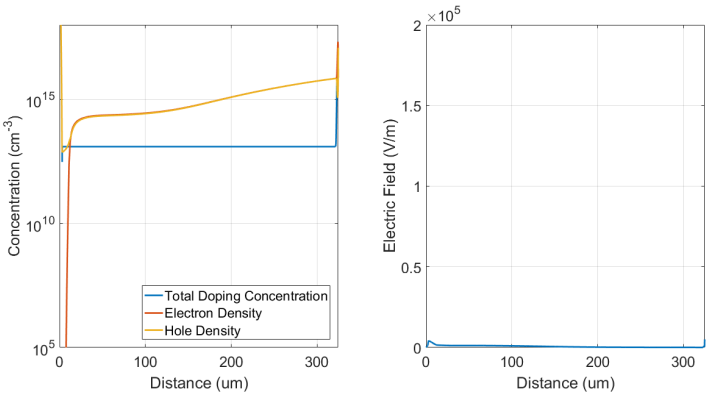


FIGURE 3.10: Hole and electron densities on the left and the corresponding electric field on the right. The device is in the on state (point 6 in Figure 3.4).

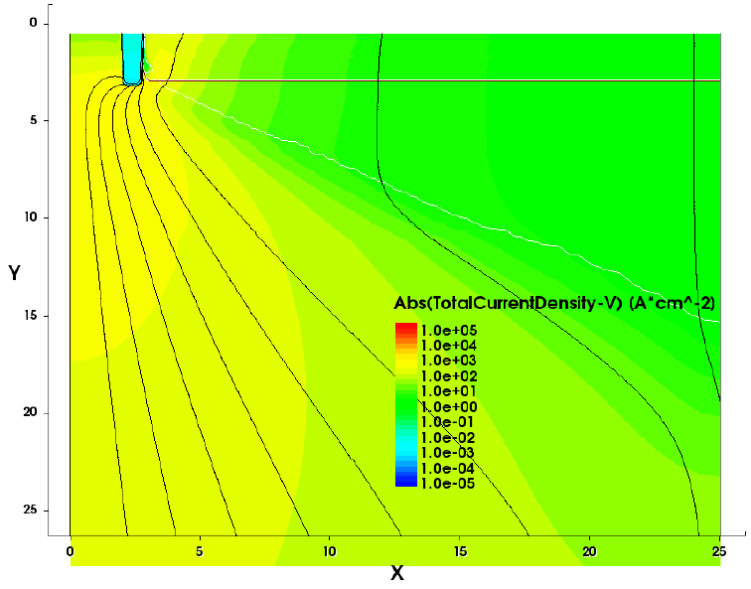


FIGURE 3.11: Current Density within the device. The device is in the on state (point 6 in Figure 3.4).

3.2 Short Circuit operation

Short circuit operations are very crucial for high power IGBT devices, as both high current and high voltage conditions are applied for several microseconds (i.e., typically less than 10 μs). Two types of operation modes can be observed during short circuit conditions, the Hard Switching Failure (HSF) and the Failure Under Load (FUL). In the first case, the short circuit appears before the IGBT is switched on and the collector current rises from 0. In the second case the failure occurs while the load was under nominal current and the collector current rises from this value [7]. In both cases, a significant amount of power is dissipated within the IGBTs, resulting to a rapid temperature increase. For the analysis that will be performed hereafter, only the HSF case will be considered.

Under short circuit, the device is operating in the saturation mode, since the collector emitter voltage is much higher than the small on-state voltage drop. At this case, the current is limited only by the V_{GE} voltage value and it is this limiting factor that makes the IGBTs robust against short circuit currents, at least for a limited amount of time [18]. During this operational mode, the behavior of the device is strongly determined by the stray elements and more importantly the stray inductances. The inductances in series to the collector and the emitter of the device are the ones determining the current rising rates, and the inductance in series with the gate terminal determines possible gate emitter voltage overshoots. Since the device is operating in saturation mode, the V_{GE} overshoots have a great impact in the allowed current through the device and consecutively the power dissipated.

For the above reasons, for performing short circuit simulations, in contrast to the transient analysis described earlier, stray elements will be included to the analysis. Additionally, towards investigating the occurrence of gate voltage oscillations, it is the stray elements in conjunction with the device capacitive behavior that determine the amplitude and frequency. It has to be noted here, that due to the power dissipated within the IGBT, a significant temperature rise takes place. This has as an effect, the reduction of the transconductance and therefore the decrease of the saturation current within the duration of the short circuit. For the simulations that will be performed here and in the next chapter, the self-heating effect has been omitted, reducing thus the complexity of the system and allowing to focus on the electrical behavior under constant room temperature.

The elements that have been chosen to be included for the simulations can be seen in the Figure 3.12, and this is due to indications that it is those elements that have a strong influence towards the appearance of oscillations, as it will be discussed in the next chapter.

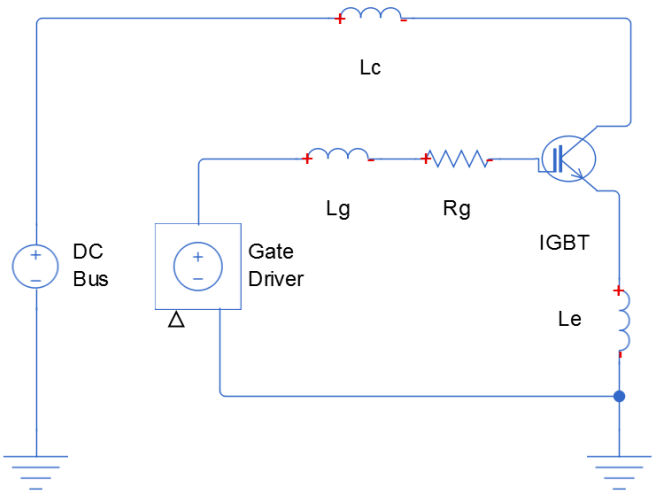


FIGURE 3.12: Schematic of the short circuit simulations including the stray elements.

It can be seen that the elements included for the short circuit simulations are only the collector, emitter and gate inductance. Additionally, the gate resistance is also included as was done in the previous section.

For simplifying the presentation of the short circuit behavior, the gate and emitter stray inductances will be omitted. These elements and their effect in the short circuit behavior will be introduced in the next chapter, where a sensitivity analysis to the values of these elements is performed, towards identifying the oscillatory conditions.

The gate resistance was chosen to be 1 Ω, a value around the commonly used values for high power IGBTs, and the collector inductance was chosen to be 200 nH. This was chosen for two reasons, it has been experimentally observed that for a 1 kA IGBT a collector-emitter inductance is approximately 10 nH, therefore if it is assumed that this IGBT module is fabricated by placing IGBT dies in parallel, for our device (50 A rated) it would require 20. Therefore, by following this rule of thumb, it can be assumed that an appropriate collector stray inductance would be 200 nH. A similar result can be found by following the same logic on the results for the stray inductance experimentally evaluated in [8].

The results of the device operating under short circuit are depicted in the figures that follow. It can be seen that due to the device operating under high V_{CE} voltage (at least two orders of magnitude higher than the nominal voltage drop), the collector current takes regardless of the level of the V_{CE} the saturation value of 205 A, dictated only by the V_{GE} voltage, as it was presented in Figure 2.13. If this saturation capability was not present, the current value would ramp limited only by the internal resistance and stray inductance and the current value during steady state would be a function of the V_{CE} voltage. This is the reason, why IGBTs and MOSFETs are favored, when short circuit failure mode is considered. For the short circuit plots that follow, the duration is set at $t_{SC} = 10\mu s$. During the turn-on and

turn-off phases, a voltage overshoot appears depending on the inductance of the short-circuit loop and the applied DC-link voltage.

As it was said before, the self-heating effect has not been taken into account for the device operation, although a significant amount of power is dissipated within the device during this mode of operation. This, according to the device's temperature coefficient would result to a change in the transconductance as the temperature of the device is increasing. It can be seen in the figures, that for our case the transconductance remains constant throughout the short circuit operation resulting to constant current through the device, once the transient phenomena have been settled.

It can be seen in the figures that a device that operates as desired under short circuit has been developed and that during this operational mode, the effect of stray elements is also included. This is a milestone for performing electrical sensitivity analysis in the next chapter, where the appropriate stray elements are investigated that lead to gate voltage oscillations under short circuit. For simulating the short circuit behavior of the device as well as for the electrical investigation that will be performed in the next chapter, the code as shown in subsection A.3.2 has been developed.

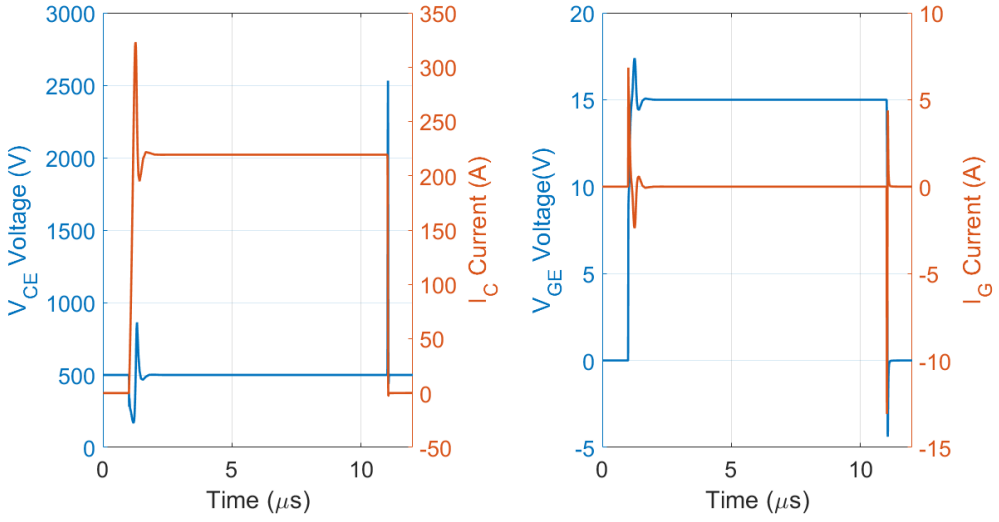


FIGURE 3.13: Short circuit performance of the device for DC-link voltage of 500 V.

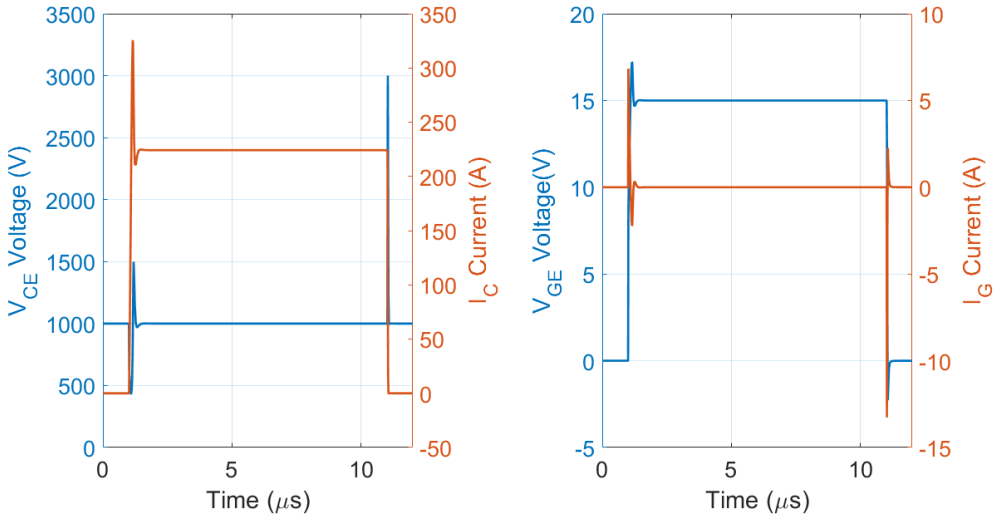


FIGURE 3.14: Short circuit performance of the device for DC-link voltage of 1000 V.

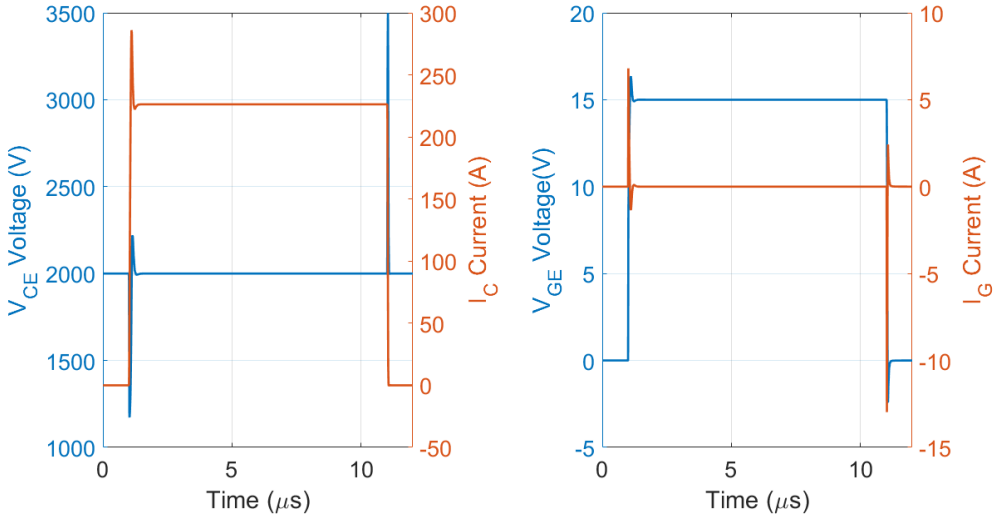


FIGURE 3.15: Short circuit performance of the device for DC-link voltage of 2000 V.

Indicatively, for the case of short-circuit operation under 1000 V of DC-bias, the hole and electron densities as well as the electric field across the device are presented in Figure 3.17 at the time instance of t=5 μs. The main difference that can be observed comparing this case to that of the device operating under normal conditions (Figure 3.11) is that here, although the device is fully conducting, a substantial electric field is developed across it. This is a result of the high collector-emitter voltage appearing across the device during its conduction. Moreover, in the current density depicted in Figure 3.17, it can be observed that a higher current density appears across the gate oxide. This is an indication of the accumulation of positive carriers under the gate side, which as will be discussed later, plays a significant role in the evolution of the gate voltage oscillations.

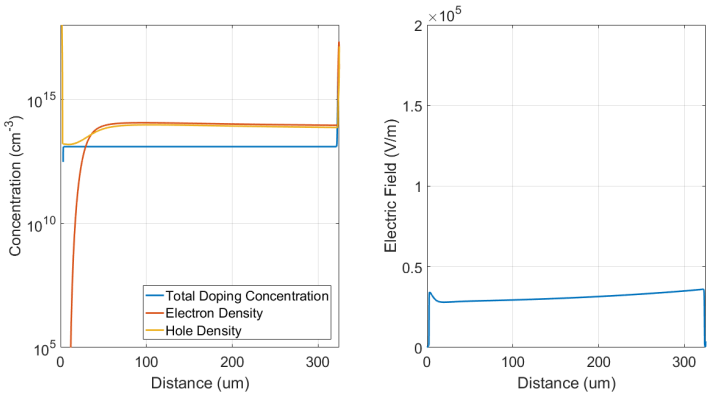


FIGURE 3.16: Hole and electron densities on the left and the corresponding electric field on the right, cross-section at x=11 μm. The device is operating at V_{DC}=1000 V and is fully in the on state.

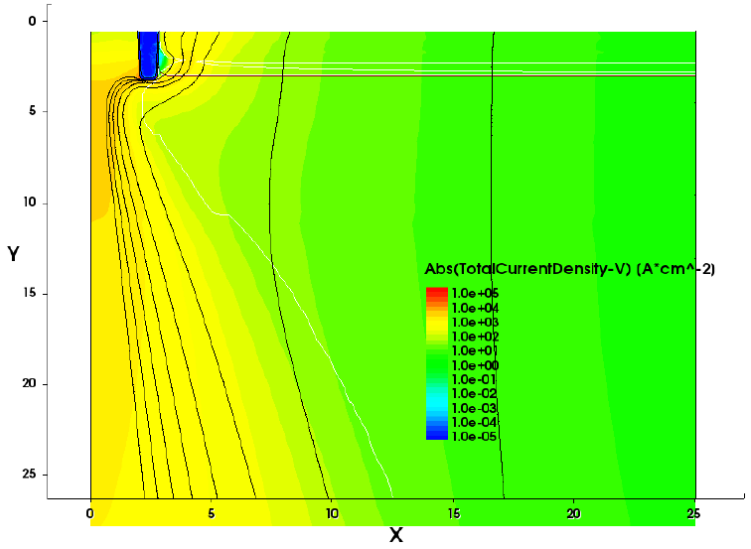


FIGURE 3.17: Current Density within the device. The device is operating at V_{DC}=1000 V and is in the on state.

Chapter 4

High Frequency Oscillations under short-circuit conditions

Lifetime requirements in modern power electronic systems dictate the need for devices to be robust against abnormal operational conditions such as short circuit. Gate voltage oscillations, occurring during short circuit conditions, pose a reliability threat to the robustness of IGBTs. Such oscillations lead to premature catastrophic failure of the gate oxide due to their amplitude becoming larger and larger, as it will be presented later. Additionally, such oscillations can be the cause for high Electromagnetic Interference (EMI) [19], as high amplitude oscillations in the MHz range on the collector voltage and current appear, due to the gate voltage oscillating.

It has been observed experimentally that such oscillations occur spontaneously and their amplitude increases with time, which points towards an instability mechanism [8]. Although the triggering mechanism of the oscillations has not been identified yet [20], several hypothesis have been proposed in the literature. The most widely described instability mechanism is associated with the negative gate capacitance [20–22].

The negative gate capacitance is associated with the accumulation of positive carriers under the gate side, which is the case when the device operates under short circuit. It is defined as the decrease of gate charge Q_G under positive V_{GE} when the collector-emitter voltage is constant, i.e. $-\frac{dQ_G}{dV_{GE}}\Big|_{V_{CE}=const}$. Under high collector voltage, the drift region obtains higher potential than the gate-emitter one. Thus, the holes injected from the collector P^+ region can flow towards the channel formed between the N^+ region in the emitter side and the N_{drift} region at the P_{Base} region. Therefore, negative charges are induced and accumulated in the gate electrode, meaning that the total gate charge is reduced. This charge reduction is higher when the gate voltage is increased due to the increased hole current through the IGBT. Therefore, it is derived that with increasing V_{GE} the gate charge drops, which corresponds to the negative sign in the gate capacitance equation given above. It has been shown that the

negative gate capacitance has an increased value as the collector-emitter voltage increases [21].

The negative gate capacitance can be interpreted as a positive feedback loop [19]. This is due to the gate resistor - gate capacitor circuit having a negative time constant, $\tau = -R_G \times C_{neg}$ resulting to a system where instead of exponentially dampening the occurring oscillations, these are exponentially magnified.

The above analysis explains the phenomenon where the occurring gate oscillations diverge in time reaching values which result to the gate oxide breakdown. On the other hand, this does not explain the triggering mechanism which leads to the spontaneous appearance of the oscillations as observed in [8]. The identification of this mechanism is a currently on going research at Aalborg University.

4.1 Frequency dependent transconductance

An indicator of the aforementioned positive feedback and its instability effect can be given by the analysis of the IGBT transconductance, $g_m(\omega)$ and its frequency dependence. An AC analysis to the IGBT was performed for observing the small signal transconductance value and the results are depicted in Figure 4.1.

As can be seen in this figure, the transconductance for frequencies between 10 - 100 MHz becomes negative for V_{CE} voltages up to 1000 V. More specifically, for a voltage of 350 V a peak negative transconductance appears at 30 MHz, for 500 V at 40 MHz and at 1000 V at 60 MHz.

The fact that the transconductance changes sign indicates that a 180° phase shift is introduced in the transconductance for these frequencies. This means that for a positive collector-emitter current the gate voltage has a negative ΔV_G which in series increases the collector current resulting thus to an amplification mechanism. The fact that the capacitance C_{GC} depends on V_{CE} can be associated with the increase in the frequency at which the transconductance becomes negative as the V_{CE} increases.

Through observing this phenomenon, it can be concluded that an amplification mechanism is apparent for the designed IGBT. Thus, it can be said that the IGBT designed is prone to gate oscillations which as discussed in [19, 20] certain conditions are required to be met for these to appear and fully develop. These involve the collector voltage, gate resistance as well as the stray inductances appearing inevitably in series to the collector, emitter and gate terminals. A sensitivity analysis is performed in the sections below towards identifying the conditions that allow for the gate oscillations to occur.

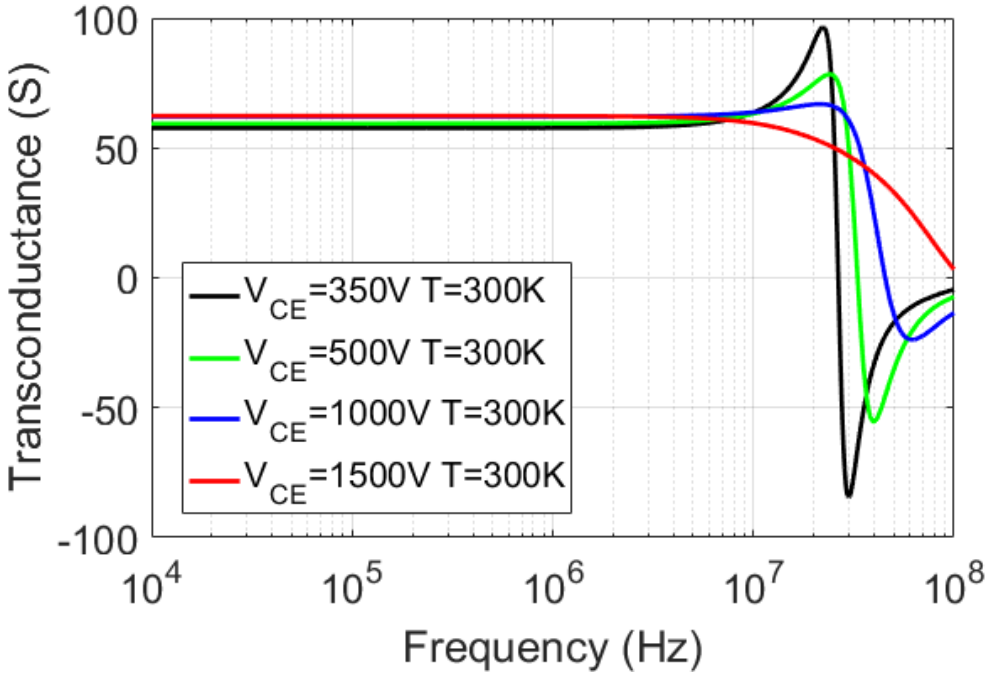


FIGURE 4.1: Schematic of the short circuit simulations including the stray elements.

4.2 Electrical sensitivity investigation - single cell

It has been described in the literature that gate voltage oscillations occur for specific short circuit testing conditions. In [8] it has been observed that for lower V_{CE} voltages the IGBT is more prone towards oscillations, which coincides with the results observed in Figure 4.1. In [23], it has been observed that as the collector stray inductance is reduced, the previously recorded oscillations do not appear. In [24], an in-depth analysis is performed, on the effect of the emitter stray inductance towards the appearance of such oscillations. In the same study, the gate resistance is also a factor that is taken into account towards finding the cases where oscillations appear.

The above indicate that the circuit stray elements, present during the experimental short circuit conditions, play an important role for the occurrence of gate voltage oscillations. For this reason, a sensitivity analysis regarding the factors that lead the IGBT into an unstable behavior is performed. The short circuit simulation topology used for the following sensitivity analysis is depicted in Figure 3.12.

4.2.1 Emitter Inductance

In [24], the emitter inductance has been presented as the triggering factor for the oscillation occurrence. Considering the short circuit simulation topology depicted in Figure 3.12, the collector inductance L_C, as justified before, is evaluated at 200 nH and the gate resistance R_G at 1 Ω, as higher gate resistor values have been shown to suppress the appearance of

oscillations. The collector voltage has been set at $V_{CE} = 500$ V, as in the Figure 4.1 this voltage was shown to be within the voltage levels capable of triggering oscillations. The gate inductance is evaluated for $L_G = 20$ nH, as this value is a common value of gate inductance, measured for an 1 kA device in [8]. For these conditions, the emitter inductance L_E is varied.

In [24], it is suggested that the higher the emitter inductance, the higher the gate resistor range at which oscillations can occur. Here, the sensitivity analysis for the emitter inductance ranged from 10 to 80 nH. More specifically, the inductance values for which simulations have been performed are $L_E = [$ 10 nH, 20 nH, 30 nH, 40 nH, 60 nH & 80 nH $]$.

It has been observed that for emitter inductance values at 10 and 20 nH, no oscillations appeared. As the inductance increased further, oscillations started to appear, which increased in amplitude, as the inductance increased. For the aforementioned conditions, the smallest emitter inductance for which oscillations appeared is that of $L_E = 30$ nH, and for this case the results are presented hereby.

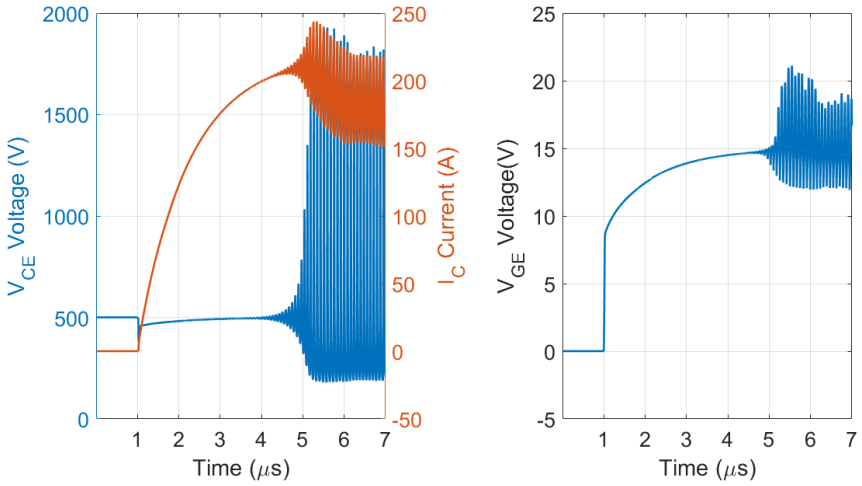


FIGURE 4.2: Emitter inductance sensitivity results for L_E at 30 nH.

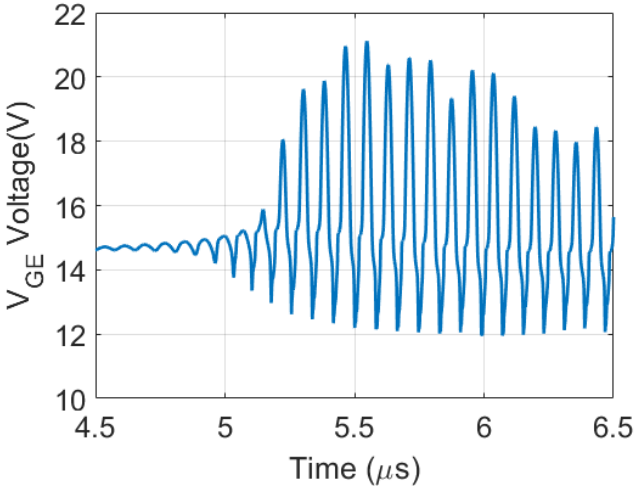


FIGURE 4.3: Closer look at the emitter inductance sensitivity results for L_E at 30 nH.

It can be observed that for this case the gate-emitter voltage barely exceeds the critical value of 20 V, provided by the manufacturer as the maximum rated value. As the inductance increases the V_{GE} voltage obtains higher values, becoming thus a threat to the oxide. In Figure 4.4 the peak value versus the inductance is presented and it can be seen that even for an emitter inductance of 40 nH, the V_{GE} voltage is well above the rated value.

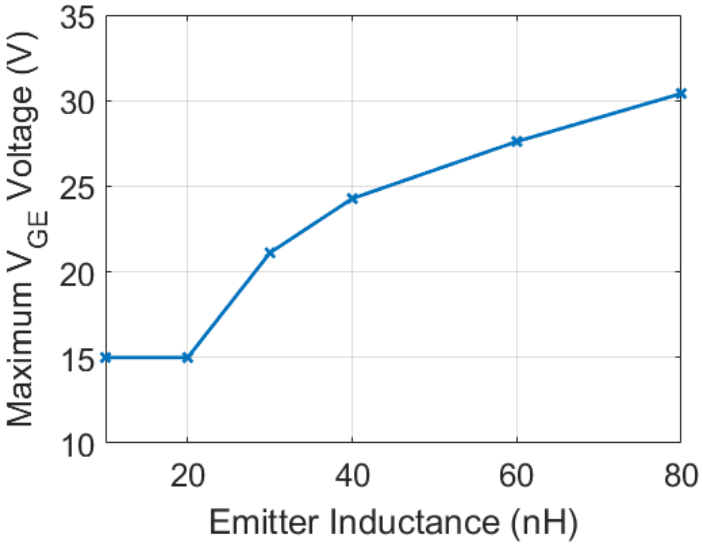


FIGURE 4.4: Effect of the emitter inductance to the maximum V_{GE} voltage value.

In Figure 4.3, the positive feedback mechanism described above can be observed in action, as small oscillations with an amplitude of around 0.5 V peak-to-peak appearing at t=4.5 μs get amplified to increasing values. The frequency of these oscillations is common for all the emitter inductance values discussed above, approximately 12.5 MHz. This frequency is fairly close to the value for which the transconductance at a voltage of 500 V has the peak negative transconductance value.

In the next subsection, two critical values of emitter inductance are investigated, that of L_E = 20 nH for which no oscillations were observed and therefore observe the impact of the remaining circuit elements in triggering the oscillations. Also the value of L_E= 30 nH is utilized, and therefore observing if the remaining circuit elements can have a dampening effect to this phenomenon.

4.2.2 Gate resistance and inductance

For the values presented above for the emitter inductance, the gate inductance and resistance were modified, investigating their effect to the oscillations. In [25] the gate inductance is presented as an oscillation triggering parameter when dies are paralleled. Also, the gate resistance has been previously identified as a critical parameter playing an important role on the oscillation mechanism [24].

First, the gate inductance is varied in the range of 0 nH to 80 nH. For the case of $L_E = 20$ nH, where previously no oscillation appeared, regardless of the value of the gate inductance, no oscillations were triggered. When increasing the emitter inductance to the value of 30 nH, as was expected from the results presented above, oscillations appeared superimposed to the V_{GE} voltage of 15 V.

The results of the parametric evaluation of the gate inductance for the case of L_E=30 nH can be observed in Figure 4.5. It can be seen that the maximum value of the V_{GE} voltage remains approximately constant. With a first glance at the results it can be deduced that as the inductance increases, the delay of the occurring oscillations is increasing.

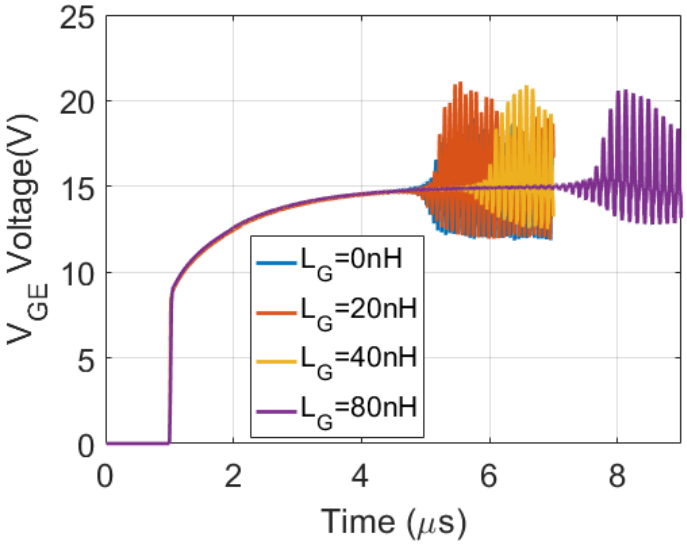


FIGURE 4.5: V_{GE} voltage for various gate inductance values, L_E=30 nH.

Additionally to the above, with the increase of the gate inductance, it has been observed that the fundamental frequency of the oscillations increases. This effect is depicted in Figure 4.6 where the rest of the circuit elements have remained unchanged, for the case of L_E=30 nH shown above.

Considering that the only substantial effect of the gate inductance is the decrease of the oscillation frequency, it was decided, for the following simulations, that the gate inductance would be omitted. This decision was based on the fact that without the inclusion of this inductance, the oscillation frequency approaches closer to the frequency at which the negative transconductance peak for the case of 500 V occurs. This way, a closer correlation of the oscillation frequency of the results obtained hereafter to the results shown in Figure 4.1 can be expected.

Regarding the gate resistance, the gate resistor has been parametrized in the range of 1 $m\Omega$ - 10 Ω. This big range allows to take into account possible cases in the operation of an IGBT,

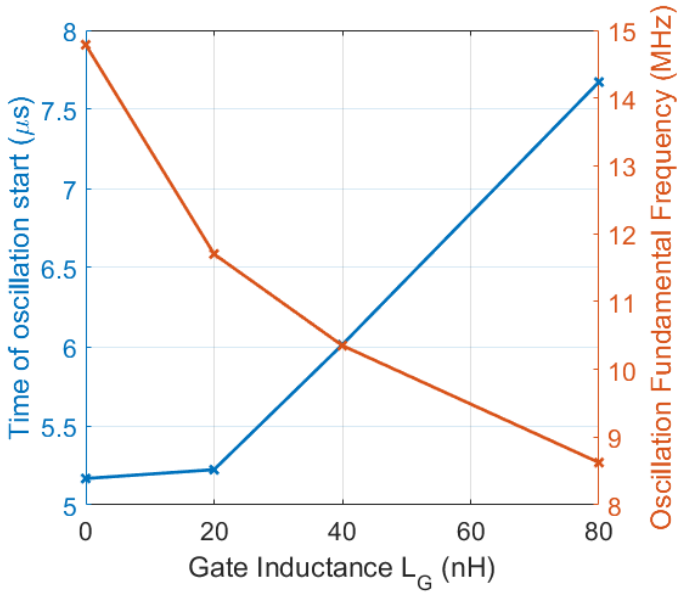
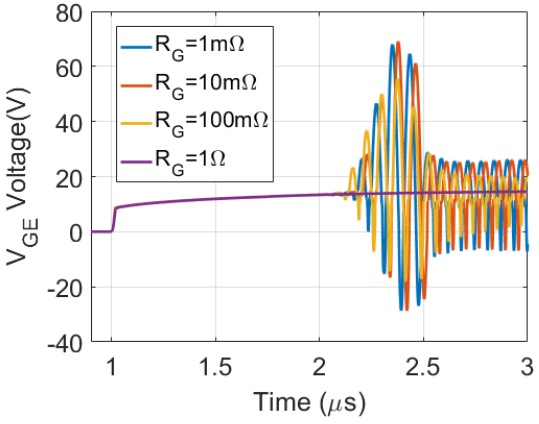


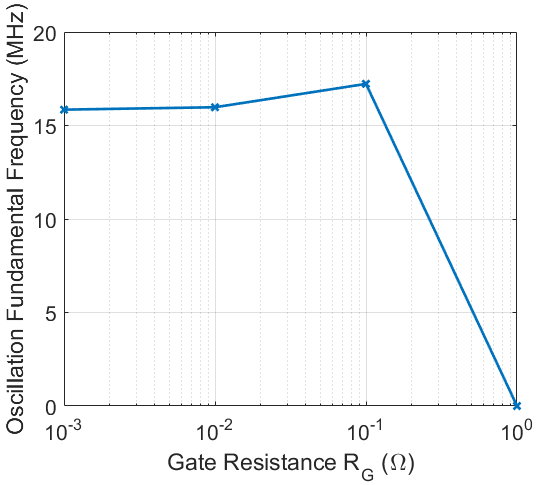
FIGURE 4.6: Effect of the gate inductance to oscillation time occurrence and frequency.

when no external resistor is assumed and the gate driver is connected directly to the gate terminals, up to high external gate resistor.

For the case of L_E=20 nH, it was previously observed that for gate resistance of 1 Ω no oscillations occurred. As the resistance assumed lower values, even for R_G=100 $m\Omega$, oscillations appeared in the V_{GE} voltage. This verifies the strong correlation of the gate resistance in the appearance of oscillations as was discussed in [24]. The effect of the different gate resistances on the occurring oscillation as well as the oscillation fundamental frequency are depicted in Figure 4.7.



(A) The V_{GE} voltage oscillations for different gate resistances.

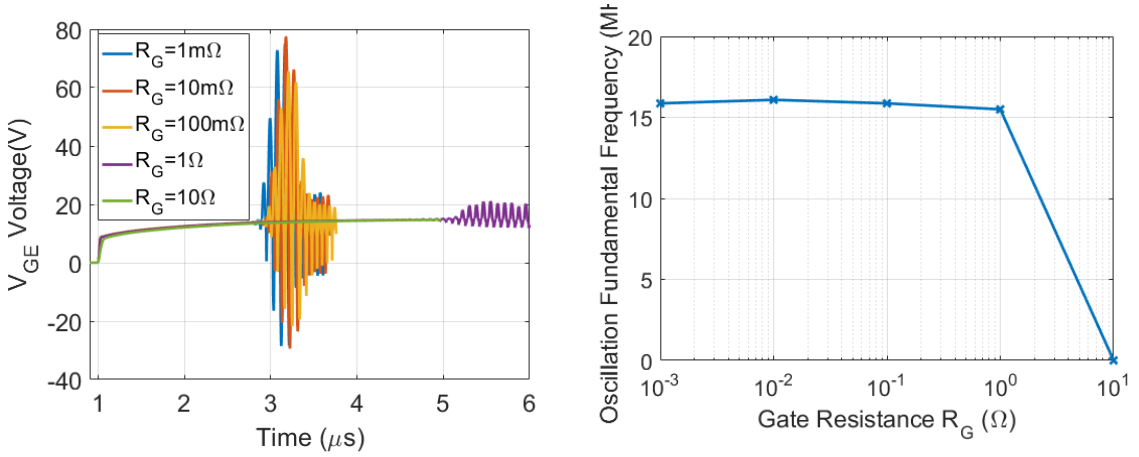


(B) Fundamental frequency of V_{GE} voltage oscillations for different gate resistances.

FIGURE 4.7: The effect of the gate resistances on the V_{GE} voltage oscillations for L_E=20 nH.

It can be seen in Figure 4.7, that the oscillations for both the cases of $R_G = 1\ m\Omega$ and 10 $m\Omega$, the maximum V_{GE} voltage as well as the oscillation frequency have similar values. When the the resistance is increased to 100 $m\Omega$ the peak V_{GE} voltage level is lowered but the fundamental frequency is increasing from 15.8 to 17.2 MHz.

For the case of L_E=30 nH, it was previously observed that for gate resistance of 1 Ω, the occurring oscillations have small amplitude and the V_{GE} voltage barely exceeds the 20 V. For lower gate resistances the maximum peak voltage exceeded the 60 V for all the cases, threatening thus the integrity of the gate oxide. When the resistance increased to 10 Ω, no oscillations appeared. The gate-emitter voltage oscillations for different gate resistors as well as the oscillation fundamental frequency are depicted in Figure 4.8.



(A) The V_{GE} voltage oscillations for different gate resistances.

(B) Fundamental frequency of V_{GE} voltage oscillations for different gate resistances.

FIGURE 4.8: The effect of the gate resistances on the V_{GE} voltage oscillations for L_E=30 nH.

For this second case, the oscillation frequency, for all the cases as seen in Figure 4.8b, remained close to the frequency value of 15.8 MHz, with it varying slightly form 16 MHz at $R_G = 10\ m\Omega$ to 15.6 MHz for $R_G = 1\ \Omega$. The results presented for the two cases above indicate that the gate resistance has a minimal effect on the oscillation frequency.

Due to the gate resistance having such a significant role both in the occurrence of oscillations as well as the peak value that these assume, the chosen value of this resistance should not only take into account the switching losses but also the robustness of the IGBT against short circuit operation. For the following simulations, the choice of $R_G = 1\Omega$ is made, as this value is a common choice when designing power converters. Also, this is chosen in order for the case of L_E= 20nH to have an oscillation free behavior and, thus, perform a consistent study on the effect of the two remaining parameters.

4.2.3 Collector inductance

The collector inductance as much as the V_{DC}-bus voltage were discussed in literature to influence the appearance or not of oscillations. In [8], it was shown that for lower collector inductances for the same device, the gate oscillations would not occur. Additionally, it was shown above that the feedback mechanism is highly dependent on the V_{CE} voltage, as this affects both the value of the Miller capacitance and the negative capacitance effect. Therefore, both those variables have been investigated towards finding the values that would favor the appearance of oscillations.

Firstly, the collector inductance was parametrized within a wide range of 0 to 1200 nH. The case for gate inductance of 0 nH and emitter inductance of 20 nH was taken into account and the gate resistance was set at 1 Ω as discussed above. It was shown that for these conditions, no oscillations were triggered, regardless of the L_C value within this range.

For the second case of emitter inductance at 30 nH and the rest of the stray elements as given for the previous case, the collector inductance was parametrized in the range of 0 to 1200 nH. For this case, and L_C=200 nH, it was previously established that oscillations occur. Therefore, it is investigated how the collector inductance affects the oscillations and for which values these oscillations are not triggered.

It was found that oscillations occurred for values of L_C=50 - 200 nH, whereas for the case where this inductance was omitted (L_C=0 nH) it was observed that no oscillations appeared. This indicates that there is a minimum inductance below which the device is not threatened by oscillations, which coincides with the observation made in [8], where after lowering this inductance the oscillatory behavior of the device ceased. This can be observed in the results showed in Figure 4.9. Additionally, it can be seen that for inductance values higher than 400 nH, the oscillations did not appear.

The effect of the collector inductance regarding the frequency and the amplitude of the oscillations can be observed in Figure 4.10. The range of the L_C inductance value for which oscillations appear can be clearly identified as 50 - 200 nH. Also, it is observed that within this range, the higher the inductance, the smaller the oscillation amplitude and for the case of L_C=200 nH this barely exceeds the 20 V. Finally, with the increase of the inductance, the oscillation frequency becomes smaller, which resembles the operation of a common L-C oscillator.

During the design of power electronic systems it is desirable to reduce the stray inductances in order to avoid voltage overshoots during the turn-off of the IGBT. If this could be reduced lower than the minimum value for which oscillations occur, the device could be safe from oscillations during short circuit.

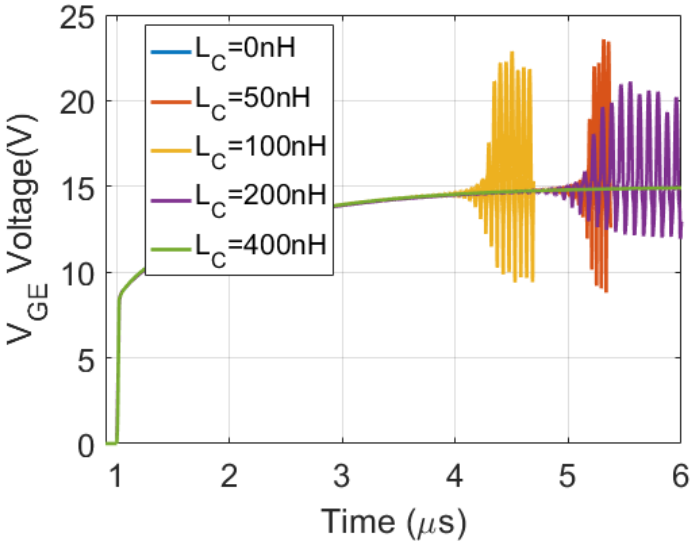
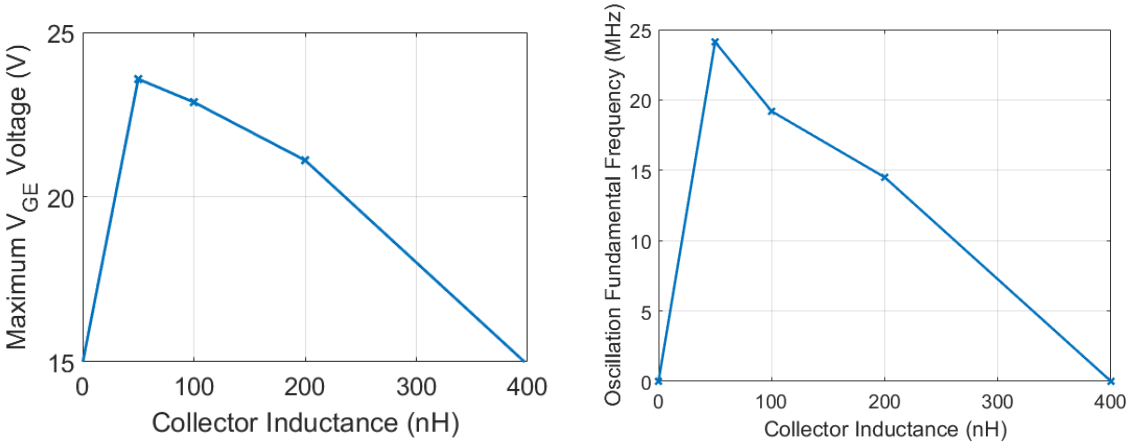


FIGURE 4.9: Gate voltage oscillations for different collector inductances and L_E=30 nH.



(A) The maximum V_{GE} voltage for different L_C values.

(B) Fundamental frequency of V_{GE} voltage oscillations for different L_C values.

FIGURE 4.10: The effect of the collector inductance on the V_{GE} voltage oscillations for L_E=30 nH.

4.2.4 Collector-emitter voltage

The last sensitivity analysis regarding the oscillatory behavior was performed on the V_{DC}-bus voltage, as it was shown earlier that it affects both the negative transconductance value as well as its occurring frequency. For showing the triggering and dampening effect of the voltage to the oscillations, two cases were simulated and are presented hereafter. For the first case, the emitter inductance is set at L_E =20 nH and for the second case, L_E =30 nH. For both the cases the stray elements chosen are L_C=200 nH, R_G=1 Ω and L_G= 0 nH; the V_{DC}-bus voltage was increased from 100 to 2500 V.

For the first case, for V_{DC}-bus voltage of 500 V, no oscillations were observed and the same was observed as the voltage obtained higher values. As the voltage decreased, though,

oscillations occurred. The oscillations for this emitter inductance for voltage levels smaller than 500 V are presented in Figure 4.11. It was shown earlier, that the V_{CE} voltage regulates the frequency for which the transconductance becomes negative. Therefore, it is of interest to observe the frequency component of the occurring oscillations for the different voltage levels. For this reason, a Fourier transformation was performed and the results are depicted in Figure 4.12.

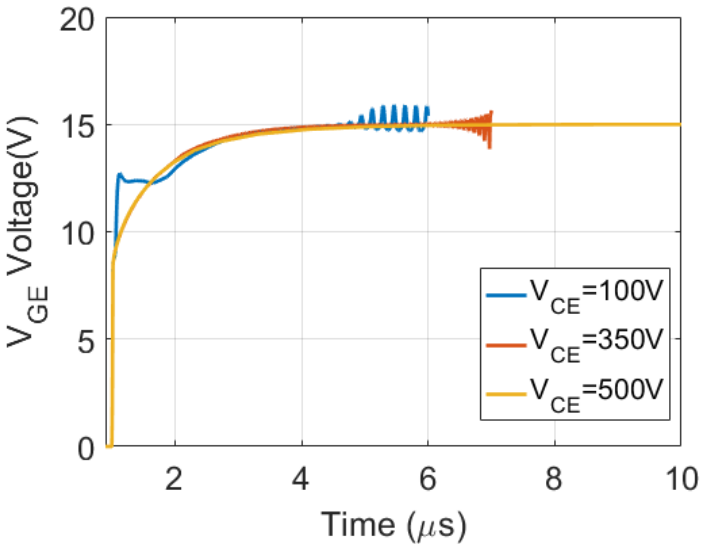
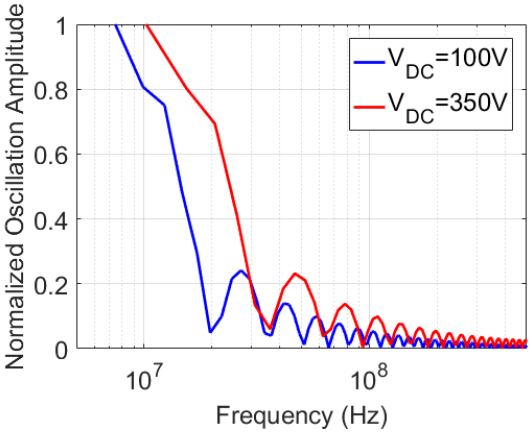
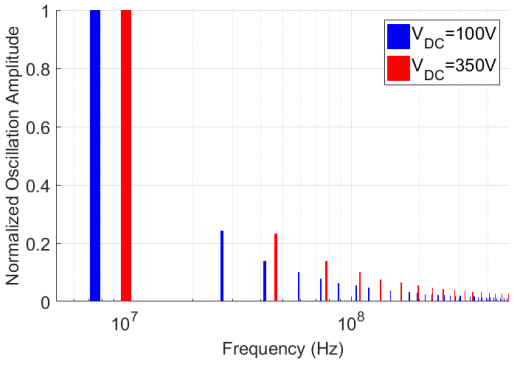


FIGURE 4.11: Gate voltage oscillations for L_E=20 nH for different DC-bus voltage levels.



(A) Harmonic component of the oscillations.



(B) Peak value of each harmonic component.

FIGURE 4.12: Fourier transformation of the oscillations for the case of L_E=20 nH for different DC-bus voltage levels.

It can be seen, that as the DC-bus voltage increases, the frequency of the fundamental harmonic of the occurring oscillations increases accordingly. This can be justified by the fact that the gate-collector capacitance decreases with the increase of the collector-emitter voltage and such a behavior is expected also by the transconductance presented in Figure 4.1. This will become more clear in the next case.

For the second case, oscillations were already apparent for voltage level of 500 V, therefore it was expected for those to be present for lower V_{CE} voltages too. For higher voltage levels, oscillations occurred up to V_{CE} =1500 V whereas thereafter these ceased to occur. This voltage dependency is depicted in Figure 4.13. Again a Fourier transformation was performed for each signal and the strong dependency of the oscillation frequency to the V_{CE} voltage is presented in Figure 4.14.

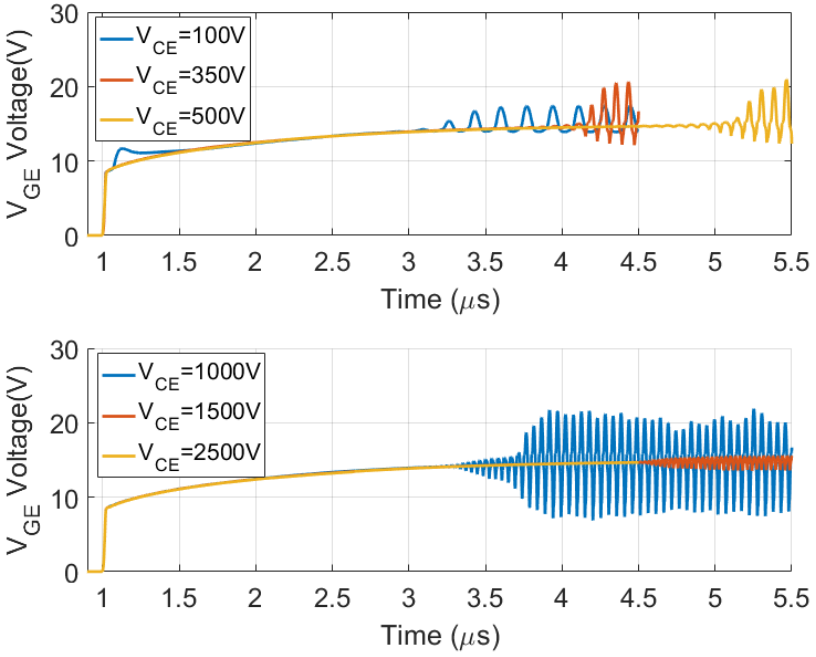
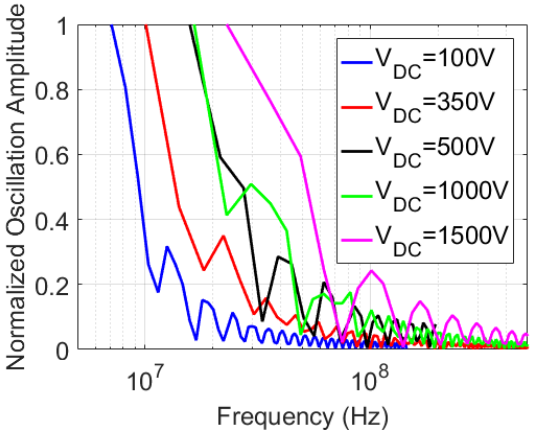
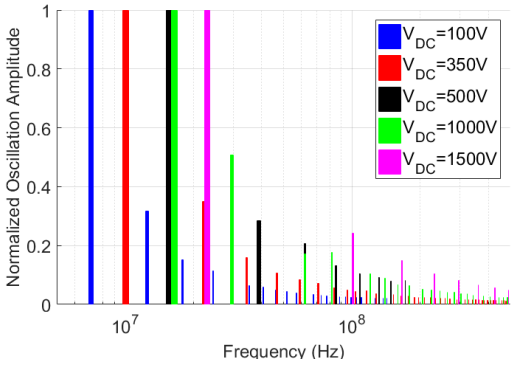


FIGURE 4.13: Gate voltage oscillations for L_E=30 nH for different DC-bus voltage levels.



(A) Harmonic component of the oscillations.



(B) Peak value of each harmonic component.

FIGURE 4.14: Fourier transformation of the oscillations for the case of L_E=30 nH for different DC-bus voltage levels.

It can be observed, that as the DC-bus voltage increases, the frequency of the fundamental harmonic of the occurring oscillations increases accordingly. The frequency of the fundamental component ranges form 7 MHz for the case of V_{CE} =100 V up to 23 MHz when

V_{CE} =1500 V.

From the above analysis it becomes clear to the reader, that a multitude of parameters determine not only the oscillation occurrence, but also the maximum value that it obtains as well as the oscillation frequency. The electrical circuit for which the electrical sensitivity was performed, as presented in Figure 3.12, represents the basic stray elements appearing on a simple TO-220 or similar package, which is the typical packaging for single die power devices. This circuit was chosen due to incorporating only the most critical elements that can assist towards the appearance of oscillations. Also, it is chosen to coincide with the circuit presented in [23], where this is utilized also towards identifying the conditions for which gate voltage oscillations occur. Stray capacitances, although usually small in value, could also be involved in triggering oscillations and their inclusion could yield to different conditions at which oscillations would be triggered.

4.3 Electrical sensitivity investigation - cells in parallel

In [20] and [24], it is discussed that although gate voltage oscillations during short circuit operation have been observed for single cell IGBTs, when a single die is concerned, the triggering mechanism does not always appear. For single cells that have not presented oscillatory behavior, as indicated in both those researches, when these were parallelized, a gate voltage instability appeared which lead to high V_{GE} amplitudes.

Bearing the above in mind, the simulation of two devices in parallel is performed here, to study the oscillations for two cells in parallel. For this study, two cases are being simulated, the first for conditions where no oscillations appeared for single cell topology and the second for conditions where such oscillations were previously observed. Therefore, the values chosen for the simulation are the following 1) L_E=20 nH, L_C=200 nH, R_G=1 Ω and L_G=0 nH, 2) L_E=30 nH, L_C=200 nH, R_G=1 Ω and L_G=0 nH, with the V_{DC}-bus voltage set at 500 V for both cases. The simulation circuit is depicted in Figure 4.15.

For the first case, where previously no oscillations have been observed, it can be seen that the paralleling of the two devices was not sufficient for entering an oscillatory state. The collector currents, V_{CE} and V_{GE} voltages for each individual IGBT are identical to each other and are presented in Figure 4.16.

For the second case, where L_E=30 nH, oscillations appeared at both V_{GE} voltages of each device. These where fully in phase and absolutely identical not only to each other, but also to that of the single cell simulation under the same conditions. Indicatively the results are presented for this case in Figure 4.17. It is possible that it is not the paralleling of the cells itself that creates the instability for the cells that previously did not present an oscillatory behavior, but the stray element difference between the two devices.

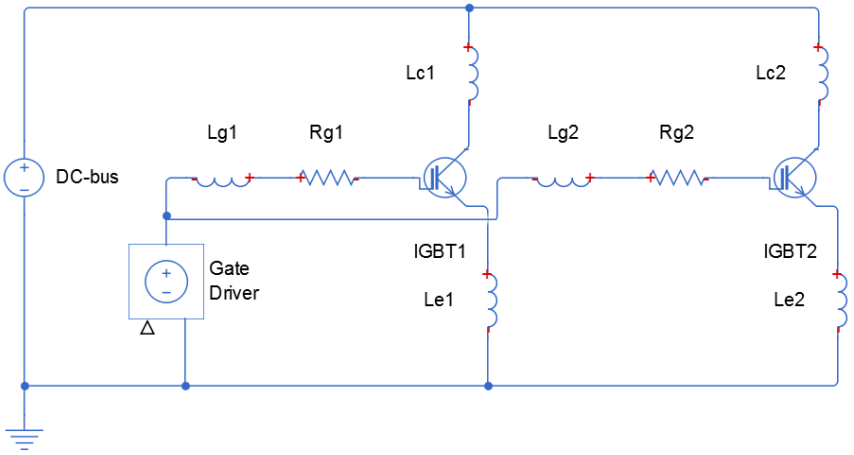


FIGURE 4.15: Electrical circuit of simulation for two IGBT cells in parallel.

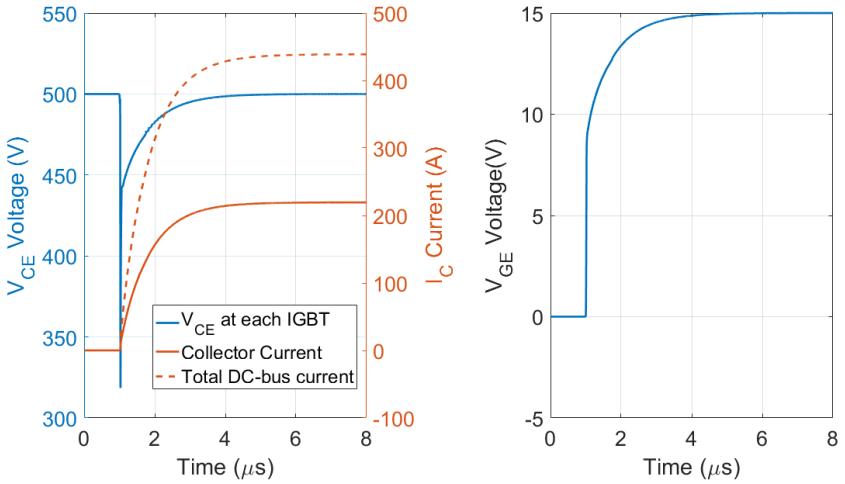


FIGURE 4.16: Total short-circuit performance for case (1) with two paralleled IGBTs.

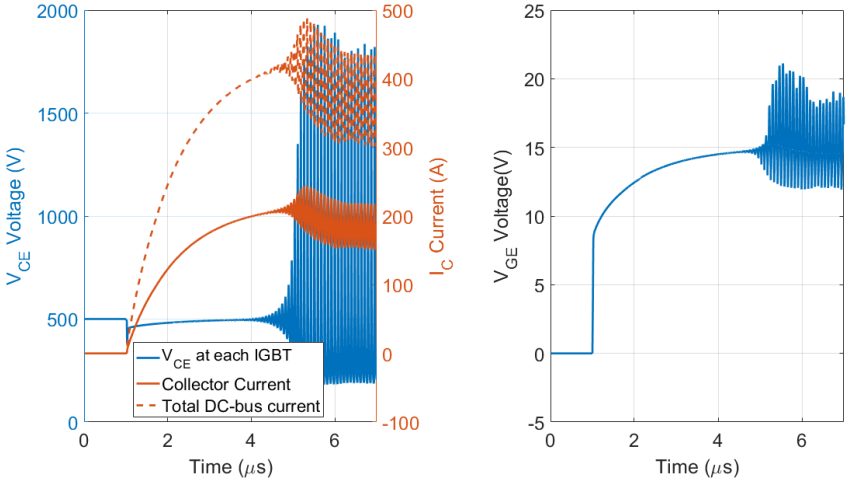


FIGURE 4.17: Total short-circuit performance for case (2) with two paralleled IGBTs.

4.4 Sensitivity analysis summary

From the completion of the sensitivity analysis, the contribution of each element in the V_{GE} voltage oscillations and their characteristics became apparent. It was observed that a major contributor to their triggering is the the emitter inductance and that it affects not only the triggering but also the amplitude, as it was shown in Figure 4.4. Equally important role plays the gate resistance in the same attributes, i.e. triggering and amplitude. The inductance appearing between the gate driver and the IGBT (L_G) showed to have no effect regarding the triggering of oscillations, but it significantly affected the fundamental frequency and the time delay of such oscillations. Therefore, it could become a design element for delaying the oscillation occurrence further than the 10 μs window. Finally, the collector inductance was shown to significantly affect the V_{GE} voltage oscillations, as such oscillations appeared within a certain range of this inductance and it was suggested that there exists a minimum inductance, below which no oscillations occur. Also as the L_C inductance increased, it was observed that both the amplitude and the oscillation frequency were reduced. Increasing the inductance further than a certain value showed to prevent the triggering of oscillations.

Usually power electronic systems are configured for operating under a certain DC-bus voltage, but when this is not the case, the operation range of the system should be taken under serious consideration. This is due to smaller V_{CE} voltages showing to assist the triggering of oscillations. Additionally, the V_{CE} voltage significantly controls the oscillation frequency which increases as the voltage increases. This could become an EMI hazard for the systems in the vicinity of the system.

It is usual to place in parallel to the IGBTs certain snubbing circuits, for reducing the transient over-voltages occurring during the turn-off of the device. The effect of those circuits which usually consist of at least a capacitor, have not be taken in to account in the current study. Such circuits could assist towards mitigating the effect of the V_{GE} voltage oscillations.

It has been observed that during the operation of the device under short circuit, before oscillations occur in the V_{GE} voltage, oscillations appear in the V_{G-gnd} and V_{E-gnd}. At the beginning, these are in phase and have equal amplitudes and therefore the device appears to be operating normally (V_{CE} voltage and I_C current under no oscillations). As these get amplified a slight amplitude mismatch was observed which leads to oscillations appearing in the V_{GE} voltage. This in series leads to the V_{CE} voltage and I_C current to oscillate. This phenomenon can be observed in Figure 4.18.

By applying a high pass filter to the data of V_{G-gnd} and V_{E-gnd} voltages, in order to eliminate the DC-component of each signal and allow easier comparison, the amplitude mismatch becomes clear. The results after the application of the filter can be viewed in Figure 4.19. Since the passive elements included to the circuit of the IGBT (stray inductances and inherent IGBT capacitances C_{CE}, C_{GC} and C_{GE}) cannot have an amplification effect to the V_{G-gnd}

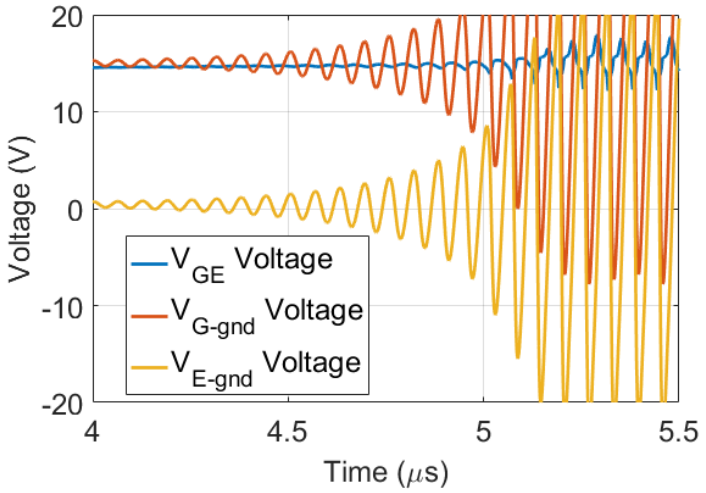


FIGURE 4.18: V_{G-gnd} and V_{E-gnd} voltages resulting to oscillations on the V_{GE} voltage.

voltage, it can be assumed that it is the transfer function of the IGBT itself that shows and amplification behavior for the frequency at which V_{G-gnd} and V_{E-gnd} voltages oscillate.

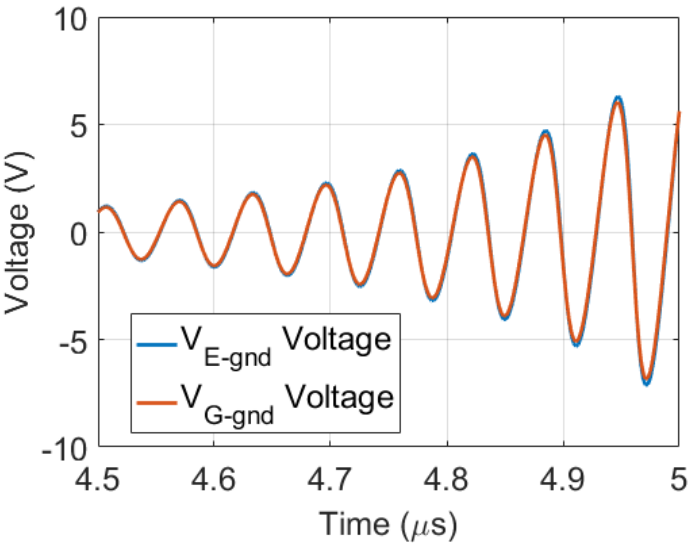


FIGURE 4.19: High pass filter on V_{G-gnd} and V_{E-gnd} voltages.

Chapter 5

Conclusions

5.1 Conclusions

The aim of the thesis was to develop an IGBT model that will aid the research conducted at Aalborg University regarding the mechanisms involved in the operation of an IGBT during short circuit failure. During this thesis, the model of a Trench Gate Punch Through IGBT was developed. This model was developed to have similar electrical performance to the 5SMX 12M3300 from ABB.

The IGBT model was developed within the Sentaurus TCAD environment, a program dedicated for semiconductor physics FEM simulations. Valuable knowledge has been obtained regarding FEM simulations as well as the physics involved in the operation of an IGBT. For the developed model, static and transient characteristics have been evaluated in depth and a comparison to the characteristics of the target IGBT from ABB was performed.

The short circuit operation of the IGBT was analyzed and afterwards a sensitivity analysis towards identifying the conditions where gate voltage oscillations can occur was conducted. During this sensitivity analysis, which took into account the collector, emitter and gate inductance as well as gate resistance and V_{DC}-bus voltage, it was found out that for specific cases, oscillations occur. These, depending on the stray element values, obtain levels that could damage the gate oxide. An extensive investigations of these parameters was performed and the effect of each regarding the occurrence of oscillations as well as their effect on the amplitude and frequency was presented. The positive feedback mechanism was observed in action as small oscillations were amplified fast, obtaining high values.

It is of paramount importance, when designing power electronics systems where high lifetime is required, that the short circuit oscillations are taken into account. For this reason, a study must be performed in calculating the stray elements of the system and according to those the appropriate value of gate resistance must be chosen. So, it can be assured that the conditions

leading to high gate-emitter voltages are not met and the premature failure of the IGBTs is avoided. This becomes a cumbersome designing process as various failure modes have to be considered, such as two IGBTs in one phase leg being simultaneously conducting or the load being short circuited, but in the long run this can assure high lifetime operation of the system.

5.2 Future Work

The IGBT model presented in this thesis was created towards finding the appropriate conditions for which gate voltage oscillations under short circuit operation would occur. This was done for assisting the on going research conducted by Aalborg University towards identifying the triggering mechanisms for the occurrence of such oscillations. A model suitable for studying these oscillations was created and can be used during the ongoing research.

For identifying the triggering mechanisms, it is important to perform a thorough observation of the internal characteristics of the device, such as the hole and electron movement, their densities and the electric field across the device, for various time instances (oscillation-free operation, initial phase of oscillations and the full cycle of an oscillation). This is the reason for choosing TCAD FEM environment for creating the model and performing the device simulations, since it allows for investigation of the internal properties of the device. Moreover, a comparative assessment of the triggering conditions for the modeled device and the targeted one has to be performed, and thus understand how the gate oxide geometry affects the triggering of the oscillations.

The designed model does not incorporate non-idealities such as impurities in the different regions of the IGBT. Such impurities occur in real IGBTs, due to the non perfect manufacturing process. Also, during the manufacturing process of the gate oxide, oxide charge traps occur, which affect the threshold voltage of an IGBT and have been associated with the low gate oxide reliability of the newly developed SiC devices. Such, elements that alter the operation of the device from the ideal case should be incorporated in this model and an analysis should be performed investigating if and how these affect the operation of the device under short circuit.

Appendix A

Code for generating and simulating the electrical behavior of the IGBT

A.1 Defining and generating the IGBT - Sentaurus Structure Editor

```
;-----------------------------------------------------------------
; Structure definition
;-----------------------------------------------------------------
(sdegeo:set-default-boolean "BAB")

(sdegeo:create-polygon (list
  (position 2.0 0.0 0)
  (position 2.1 3.13 0)
  (position 2.7 3.13 0)
  (position 2.8 0.0 0)
  (position 2.0 0.0 0))
  "PolySi" "R.PolyGate")

(sdegeo:fillet-2d (find-vertex-id (position 2.1 3.13 0)) 0.2)
(sdegeo:fillet-2d (find-vertex-id (position 2.7 3.13 0)) 0.2)

(sdegeo:create-polygon (list
  (position 1.95 0.00 0)
  (position 2.05 3.22 0)
  (position 2.75 3.22 0)
  (position 2.85 0.00 0)
  (position 1.95 0.00 0))
  "Oxide" "R.Gox")

```

```
25 (sdegeo:fillet-2d (find-vertex-id (position 2.05 3.22 0)) 0.2)
26 (sdegeo:fillet-2d (find-vertex-id (position 2.75 3.22 0)) 0.2)
27
28 (sdegeo:create-polygon (list
29   (position 2.00  0.02 0)
30   (position 1.50  0.02 0)
31   (position 1.30  0.22 0)
32   (position 0.00  0.22 0)
33   (position 0.00 -0.18 0)
34   (position 1.30 -0.18 0)
35   (position 1.50  0.00 0)
36   (position 2.00  0.00 0)
37   (position 2.00  0.02 0))
38   "Oxide" "R.LOCOS")
39
40 (sdegeo:fillet-2d (find-vertex-id (position 1.3  0.22 0)) 0.15)
41 (sdegeo:fillet-2d (find-vertex-id (position 1.3 -0.18 0)) 0.15)
42
43 (sdegeo:create-rectangle
44   (position 2.8 -0.3 0.0 )  (position 3.1 0.0 0.0 ) "Oxide"
     "R.Spacer" )
45 (sdegeo:create-rectangle
46   (position 0.0  0.0 0.0 )  (position 2.8 -0.3 0.0 ) "PolySi"
     "R.PolyCont" )
47 (sdegeo:create-rectangle
48   (position 0.0  0.0 0.0 )  (position 25 @len@ 0.0 ) "Silicon"
     "R.Si" )
49
50 (sdegeo:define-contact-set "Emitter"   4  (color:rgb 1 0 0 ) "##"
     )
51 (sdegeo:define-contact-set "Collector" 4  (color:rgb 1 0 0 ) "##"
     )
52 (sdegeo:define-contact-set "Gate"      4  (color:rgb 1 0 0 ) "##"
     )
53
54 (sdegeo:define-2d-contact (find-edge-id (position 3.5  0.0 0.0))
     "Emitter")
55 (sdegeo:define-2d-contact (find-edge-id (position 3.5 @len@ 0.0))
     "Collector")
56 (sdegeo:define-2d-contact (find-edge-id (position 1.0 -0.3 0.0))
     "Gate")
57 ;-----------------------------------------------------------------
58 ; Profiles
59 ;-----------------------------------------------------------------
60
```

```
(sdedr:define-constant-profile "Const.Substrate"
 "PhosphorusActiveConcentration" @ndrift@ )
(sdedr:define-constant-profile-material "PlaceCD.Substrate"
 "Const.Substrate" "Silicon" )

(sdedr:define-constant-profile "Const.PolyGate"
 "PhosphorusActiveConcentration" 1e+21 )
(sdedr:define-constant-profile-material "PlaceCD.PolyGate"
 "Const.PolyGate" "PolySi" )

(sdedr:define-refinement-window "BaseLine.pbody" "Line"
 (position 3.0 0.0 0.0)
 (position 25.5 0.0 0.0) )
(sdedr:define-gaussian-profile "Impl.pbodyprof"
 "BoronActiveConcentration"
 "PeakPos" 0.1  "PeakVal" @pbody@
 "ValueAtDepth" 1e17  "Depth" 2
 "Erf"  "Length" 0.1)
(sdedr:define-analytical-profile-placement "Impl.pbody"
 "Impl.pbodyprof" "BaseLine.pbody" "Positive" "NoReplace" "Eval")

(sdedr:define-refinement-window "BaseLine.nplus" "Line"
 (position 3.0 0.0 0.0)
 (position 3.7 0.0 0.0) )
(sdedr:define-gaussian-profile "Impl.nplusprof"
 "ArsenicActiveConcentration"
 "PeakPos" 0.0  "PeakVal" @nplus@
 "ValueAtDepth" 1e17  "Depth" 0.5
 "Erf"  "Length" 0.1)
(sdedr:define-analytical-profile-placement "Impl.nplus"
 "Impl.nplusprof" "BaseLine.nplus" "Positive" "NoReplace" "Eval")

(sdedr:define-refinement-window "BaseLine.fieldstop" "Line"
 (position 0.0 @len@ 0.0)
 (position 25.5 @len@ 0.0) )
(sdedr:define-gaussian-profile "Impl.fieldstopprof"
 "ArsenicActiveConcentration"
 "PeakPos" 0.2  "PeakVal" @nbuffer@
 "ValueAtDepth" @ndrift@  "Depth" 3.0
 "Erf"  "Length" 0.1)
(sdedr:define-analytical-profile-placement "Impl.fieldstop"
 "Impl.fieldstopprof" "BaseLine.fieldstop" "Negative" "NoReplace"
   "Eval")

(sdedr:define-refinement-window "BaseLine.collector" "Line"
```

```
105   (position 0.0 @len@ 0.0)
106   (position 25.5 @len@ 0.0) )
107  (sedr:define-gaussian-profile "Impl.collectorprof"
108   "BoronActiveConcentration"
109   "PeakPos" 0.1  "PeakVal" @pem@
110   "ValueAtDepth" 1e17  "Depth" 0.7
111   "Erf"  "Length" 0.1)
112  (sedr:define-analytical-profile-placement "Impl.collector"
113   "Impl.collectorprof" "BaseLine.collector" "Negative" "NoReplace"
        "Eval")
114
115  ;-----------------------------------------------------------------
116  ; Meshing
117  ;-----------------------------------------------------------------
118
119  (sedr:define-refinement-window "RW.SiTop"
120   "Rectangle"
121   (position 0.0 0.0 0.0 )
122   (position 25 6.0 0.0 ))
123  (sedr:define-refinement-size "Ref.SiTop"
124    0.301 0.3751
125    0.05  0.05 )
126  (sedr:define-refinement-function "Ref.SiTop"
127   "DopingConcentration" "MaxTransDiff" 1)
128  (sedr:define-refinement-placement "RefPlace.SiTop"
129   "Ref.SiTop" "RW.SiTop" )
130
131  (sedr:define-refinement-window "RW.SiMid"
132   "Rectangle"
133   (position 0.0  6.0 0.0 )
134   (position 25 10.0 0.0 ))
135  (sedr:define-refinement-size "Ref.SiMid"
136    0.601   0.751
137    0.03    0.03 )
138  (sedr:define-refinement-function "Ref.SiMid"
139   "DopingConcentration" "MaxTransDiff" 1)
140  (sedr:define-refinement-placement "RefPlace.SiMid"
141   "Ref.SiMid" "RW.SiMid" )
142
143  (sedr:define-refinement-window "RW.SiBot"
144   "Rectangle"
145   (position 0.0 10.0 0.0 )
146   (position 25 @len@ 0.0 ))
147  (sedr:define-refinement-size "Ref.SiBot"
148    1.201 2.001
```

```
149    0.05   0.05 )
150  (sedr:define-refinement-function "Ref.SiBot"
151   "DopingConcentration" "MaxTransDiff" 1)
152  (sedr:define-refinement-placement "RefPlace.SiBot"
153   "Ref.SiBot" "RW.SiBot" )
154
155  (sedr:define-refinement-window "RW.TrBot"
156   "Rectangle"
157   (position 1.8 1.5 0.0 )
158   (position 3.3 4.0 0.0 ))
159  (sedr:define-refinement-size "Ref.TrBot"
160    0.1   0.1
161    0.05 0.05)
162  (sedr:define-refinement-function "Ref.TrBot"
163   "DopingConcentration" "MaxTransDiff" 1)
164  (sedr:define-refinement-placement "RefPlace.TrBot"
165   "Ref.TrBot" "RW.TrBot" )
166
167  ;-----------------------------------------------------------------
168  ; Meshing Offseting
169  ;-----------------------------------------------------------------
170  (sdenoffset:create-global
171   "usebox" 2
172   "maxangle" 180
173   "maxconnect" 1000000
174   "background" ""
175   "options" ""
176   "triangulate" 0
177   "recoverholes" 1
178   "hglobal" 5
179   "hlocal" 0
180   "factor" 1.3
181   "subdivide" 0
182   "terminateline" 3
183   "maxedgelength" 5
184   "maxlevel" 10)
185
186  (sdenoffset:create-noffset-block "region" "R.Si"
187   "maxedgelength" 5
188   "maxlevel" 10)
189
190   (sdenoffset:create-noffset-block "region" "R.Gox"
191   "maxedgelength" 5
192   "maxlevel" 2)
193
```

```
(sdenoffset:create-noffset-block "region" "R.PolyGate"
 "maxedgelength" 0.25
 "maxlevel" 4)

(sdenoffset:create-noffset-interface "region" "R.Si" "R.Gox"
 "hlocal" 0.0015
 "factor" 1.5
)

(sdenoffset:create-noffset-interface "region" "R.Gox" "R.Si"
 "hlocal" 0.01
 "factor" 1.5
)

(sdenoffset:create-noffset-interface "region" "R.PolyGate" "R.Gox"
 "hlocal" 0.003
 "factor" 1.5
)

;-----------------------------------------------------------------
; Saving BND file
(sdeio:save-tdr-bnd (get-body-list) "@tdrboundary/o@")

; Save CMD file
(sdedr:write-cmd-file "@commands/o@")
(system:command "snmesh -offset n@node@_msh")
```

A.2 Determining the static characteristics for the IGBT

A.2.1 Evaluating the blocking voltage capability

```
File {
    Grid= "@tdr@"
    Parameters= "@parameter@"
    Plot= "@tdrdat@"
    Current= "@plot@"
    Output= "@log@"
}

Electrode {
{ Name="Emitter" Voltage=0.0 }
{ Name="Collector" Voltage=0.0 }
{ Name="Gate" Voltage=0 }
}
```

```
14 Physics {
15 AreaFactor = 4.4e6
16    Temperature= @Temp@
17    EffectiveIntrinsicDensity(BandGapNarrowing (Slotboom))
18
19 Mobility (
20       PhuMob
21       HighFieldSaturation
22       Enormal
23    )
24    Recombination (
25       SRH(DopingDependence TempDependence)
26       Auger
27       Avalanche (Lackner)
28    )
29 }
30 Physics(
31 MaterialInterface="Silicon/Oxide") {
32 Traps((FixedCharge Conc=0))
33 }
34
35 Plot {
36 eDensity hDensity eCurrent hCurrent
37 equasiFermi hquasiFermi
38 ElectricField eEparallel hEparallel
39 Potential SpaceCharge
40 SRHRecombination Auger AvalancheGeneration
41 eMobility hMobility eVelocity hVelocity
42 Doping DonorConcentration AcceptorConcentration
43 }
44
45 Math {
46 Extrapolate
47 RelErrControl
48 Iterations=40
49 }
50
51 Solve {
52 # initial Gate voltage Vge=0.0V
53 Poisson
54 Coupled { Poisson Electron }
55 Coupled { Poisson Electron Hole}
56 Save (FilePrefix="vg0")
57
58 # second curve
```

```
59 Load(FilePrefix="vg0")
60 NewCurrentPrefix="vBV_"
61 Quasistationary
62 (InitialStep=0.01 Maxstep=0.1 MinStep=1e-10
63 Goal{ name="Collector" voltage=@Vcmax@ }
64 )
65 {Coupled {Poisson Electron Hole  }
66 }
67 }
```

A.2.2 Evaluating the threshold voltage and device transconductance

```
1  File {
2     Grid= "@tdr@"
3     Parameters= "@parameter@"
4     Plot= "@tdrdat@"
5     Current= "@plot@"
6     Output= "@log@"
7  }
8
9  Electrode {
10    { Name="Gate"      Voltage= 0 }
11    { Name="Emitter"   Voltage= 0 }
12    { Name="Collector" Voltage= 0 }
13 }
14
15 Physics {
16    AreaFactor = 4.4e6
17    Temperature= @Temp@
18    EffectiveIntrinsicDensity(BandGapNarrowing (Slotboom))
19 }
20
21 Physics(Material="Silicon"){
22    Mobility (
23       PhuMob
24       HighFieldSaturation
25       Enormal
26    )
27    Recombination (
28       SRH(DopingDependence TempDependence)
29       Auger
30    )
31 }
32
33  Physics (MaterialInterface="Oxide/Silicon") {
```

```
34      Traps(FixedCharge Conc= 0.0)
35     }
36
37     Math {
38     Extrapolate
39     Number_of_threads= 4
40  }
41
42  Insert= "PlotSection_des.cmd"
43  Insert= "MathSection_des.cmd"
44
45  Solve {
46     Poisson
47     Coupled { Poisson Electron Hole }
48
49     Quasistationary (
50        InitialStep= 1e-2 Increment= 1.35
51        MinStep= 1e-5 MaxStep= 0.5
52        Goal { Name= Collector Value=@Vc@ }
53     ){ Coupled { Poisson Electron Hole } }
54
55     NewCurrentPrefix="IcVg_"
56     Quasistationary (
57        InitialStep= 1e-2 Increment= 1.35
58        MinStep= 1e-9 MaxStep= 0.05
59        Goal { Name= Gate Value=@Vg@ }
60     ){ Coupled { Poisson Electron Hole } }
61  }
```

A.2.3 Evaluating the on-state voltage drop

```
1   File {
2      Grid= "@tdr@"
3      Parameters= "@parameter@"
4      Plot= "@tdrdat@"
5      Current= "@plot@"
6      Output= "@log@"
7   }
8
9   Electrode {
10  { Name="Emitter" Voltage=0.0 }
11  { Name="Collector" Voltage=0.0 }
12  { Name="Gate" Voltage=15.0}
13  }
14  Physics {
```

```
AreaFactor = 4.4e6
   Temperature= @Temp@
   EffectiveIntrinsicDensity(BandGapNarrowing (Slotboom))

Mobility (
      PhuMob
      HighFieldSaturation
      Enormal
   )
   Recombination (
      SRH(DopingDependence TempDependence)
      Auger
      Avalanche (Lackner)
   )
}
Physics(
MaterialInterface="Silicon/Oxide") {
Traps((FixedCharge Conc=0))
}

Plot {
eDensity hDensity eCurrent hCurrent
equasiFermi hquasiFermi
ElectricField eEparallel hEparallel
Potential SpaceCharge
SRHRecombination Auger AvalancheGeneration
eMobility hMobility eVelocity hVelocity
Doping DonorConcentration AcceptorConcentration
}

Math {
Extrapolate
RelErrControl
Iterations=40
}

Solve {
# initial Gate voltage Vge=0.0V
Poisson
Coupled { Poisson Electron }
Coupled { Poisson Electron Hole }
Save (FilePrefix="vg0")

# ramp Gate and save solutions:
# second Gate voltage Vge=15.0V
```

```
Quasistationary
(InitialStep=0.1 Maxstep=0.1 MinStep=0.01
Goal { name="Gate" voltage=15 } )
{ Coupled { Poisson Electron Hole   } }
Save(FilePrefix="vg15")

# second curve
Load(FilePrefix="vg15")
NewCurrentPrefix="vc15_"
Quasistationary
(InitialStep=0.01 Maxstep=0.1 MinStep=0.0001
Goal{ name="Collector" voltage=15.0 }
)
{Coupled {Poisson Electron Hole  }
}
}
```

A.3 Simulating the dynamic behavior of the device

A.3.1 Double Pulse Test - Switching Characteristcs

```
######################################################################
# Transient Double-Pulse Switching Simulation
######################################################################

!(
set DG      0        ;#-- quantum corr is on, when 1

set PULSE "(0.0    -10
1.0e-7 -10
1.1e-7 @VgMax@
@<tON_s + 1.1e-7>@ @VgMax@
@<tON_s + 1.2e-7>@ -10
@<tON_s + 1.2e-7 + tOFF_s>@ -10
@<tON_s + 1.3e-7 + tOFF_s>@ @VgMax@
@<2*tON_s + 1.3e-7 + tOFF_s>@ @VgMax@
@<2*tON_s + 1.4e-7 + tOFF_s>@ -10
@<2*tON_s + 1.4e-7 + 2*tOFF_s>@ @VgMax@
@<3*tON_s + 1.4e-7 + 2*tOFF_s>@ -10
1.0    -10)"

set EQN0       "Poisson Electron Hole"
set EQN1       "Poisson Electron Hole Circuit Contact"
set DGEQ       "eQuantumPotential"
```

```
24
25 set EQNS       "$EQN1"
26 set DF         "GradQuasiFermi"
27
28 if {!$DG} {set DGEQ " "}
29 set EQNS  "$EQNS $DGEQ"
30
31 )!
32
33 *---------------------------------------------------------------*
34 Dessis IGBT {
35
36 File {
37 grid      = "@tdr@"
38 current   = "@plot@"
39 plot      = "@tdrdat@"
40 parameter = "@parameter@"
41 }
42
43 Electrode {
44 { name="Collector" voltage=0.0 }
45 { name="Emitter"   voltage=0.0 }
46 { name="Gate"      voltage=0.0 }
47 }
48
49 Physics{
50 AreaFactor = 4.4e6
51 Temperature = @Temp@
52 EffectiveIntrinsicDensity( OldSlotboom )
53 Fermi
54 }
55
56 Physics (Material="Silicon") {
57 Fermi
58 Mobility(
59 PhuMob
60 Enormal
61 HighFieldSaturation( !(puts -nonewline $DF)! )
62 )
63 Recombination(
64 SRH(DopingDependence)
65 SRH(
66 ElectricField (
67 Lifetime = Schenk
68 DensityCorrection = Local
```

```
)
)
Auger
Avalanche( !(puts -nonewline $DF)! )
)
}

Physics (MaterialInterface="Oxide/Silicon") {
Traps(FixedCharge Conc= 0.0)
}
}

*-----------------------------------------------------------------*
File {
Output= "@log@"
}

Insert = "PlotSection_des.cmd"

Math {
Extrapolate
Derivatives
Notdamped=50
Iterations=12
-metalConductivity
AvalDerivatives
RelErrControl
Transient=BE
NoCheckTransientError
Digits            = 6
eDrForceRefDens   = 1e12
hDrForceRefDens   = 1e12

RHSmin=1e-20
Number_of_threads= 4
}

System {
IGBT trans (Emitter=e  Gate=g Collector=c)
Vsource_pset vc  (nc 0)  { dc = 0 }
Vsource_pset ve  (e 0)   { dc = 0 }

Vsource_pset vg  (ng 0)  { pwl = !( puts $PULSE )! }

Diode_pset dd (c nc) { }   # Resistive Load
```

```
Inductor_pset lc (nc c)  { inductance = @Lc@ }   # Inductive Load
Resistor_pset rg (ng g)  { resistance = @Rg@ }   # Gate Resistance

Set (0=0)
Initialize(g=0, c=0)
Plot (time() v(g) v(c) v(nc) v(ng))
Plot "n@node@" (time() v(g) v(c) v(nc) v(ng))
}

Solve {
*- Creating initial guess:
Coupled { poisson }
Coupled(Iterations=100 LineSearchDamping=1e-4){ Poisson !(puts
    -nonewline $DGEQ)! }
Coupled(Iterations=100 LineSearchDamping=1e-4){ Poisson !(puts
    -nonewline $DGEQ)! Electron Hole }

*- Ramp Drain
Unset(d)
Quasistationary (
InitialStep=1e-3 MinStep=1e-5 MaxStep=0.5
Increment=1.45 Decrement=2.1
Goal { Parameter= vd.dc Value=@Vdd@ }
){ Coupled { !(puts -nonewline $EQN1)! } }
Coupled { !(puts -nonewline $EQNS)! }

NewCurrentPrefix="Trans_"

Transient (
InitialTime=0 FinalTime= 15e-06
InitialStep=1e-8 MinStep=1e-15 MaxStep=1e-4
Increment= 1.35 Decrement= 2.1
){ Coupled { !(puts -nonewline $EQNS)! }
}
}
```

A.3.2 Short circuit test and gate oscillation investigation

```
######################################################################
# Short Circuit Type-1 Simulation
######################################################################

!(
set DG      0          ;#-- quantum corr is on, when 1

```

```
set EQN0        "Poisson Electron Hole"
set EQN1        "Poisson Electron Hole Circuit Contact"
set DGEQ        "eQuantumPotential hQuantumPotential"

set EQNS       "$EQN1"
set DF         "GradQuasiFermi"

if {!$DG} {set DGEQ " "}
set EQNS  "$EQNS $DGEQ"
)!
*-------------------------------------------------------------------*
Dessis IGBT {

File {
Grid     = "@tdr@"
Parameter= "@parameter@"
Current  = "@plot@"
Plot     = "@tdrdat@"
}

Electrode {
{ name="Collector" voltage=0.0 }
{ name="Emitter"   voltage=0.0 }
{ name="Gate"      voltage=0.0 }
}

Physics{
AreaFactor = 4.4e6
Temperature = 300
EffectiveIntrinsicDensity( OldSlotboom )
Fermi
}

Physics (Material="Silicon") {
Fermi
Mobility(
PhuMob
Enormal
HighFieldSaturation( !(puts -nonewline $DF)! )
)
Recombination(
SRH( DopingDep TempDependence)
Auger
Avalanche( !(puts -nonewline $DF)! )
)
```

```
}

Physics (MaterialInterface="Oxide/Silicon") {
Traps(FixedCharge Conc= 0.0)
}
}

*-------------------------------------------------------------------*
File {
Output= "@log@"
}

Insert = "PlotSection_des.cmd"

math {  RelErrcontrol
NoAutomaticCircuitContact
Transient = BE
derivatives
Extrapolate
NumberOfThreads = 4
}

System {
IGBT trans (Emitter=e  Gate=g Collector=c)

Vsource_pset vc  (nc 0)  { dc = 0 }
Vsource_pset ve  (ne 0)  { dc = 0 }
Vsource_pset vg  (ng 0)  { pulse = (0 15 1e-6 1e-8 1e-8 11e-6
   50e-6) }

Inductor_pset lc (nc c)  { inductance = @lc@ }
Inductor_pset lg (ng gr)   { inductance = @lg@ }
Resistor_pset rg (gr g)  { resistance = @Rgsc@ } # Gate Resistance
Inductor_pset le (e ne)   { inductance = @lesc@ }

set(0=0)
initialize(g=0, c=0)
Plot (time() v(g) v(c) v(ng) i(lc c)  v(gr))
Plot "n@node@" (time() v(g) v(c) v(ng) i(lc c) v(gr))
}

Solve {
*- Creating initial guess:
Coupled { poisson }
```

```
96  Coupled(Iterations=100 LineSearchDamping=1e-4){ Poisson !(puts
       -nonewline $DGEQ)! }
97  Coupled(Iterations=100 LineSearchDamping=1e-4){ Poisson !(puts
       -nonewline $DGEQ)! Electron Hole }
98
99  *- Ramp Collector
100 unset(c)
101 Quasistationary (
102 InitialStep=1e-3 MinStep=1e-5 MaxStep=0.5
103 Increment= 1.45 Decrement= 2.1
104 Goal { Parameter= vd.dc Value=@Vsc@ }
105 ){ Coupled { !(puts -nonewline $EQN1)! } }
106 Coupled { !(puts -nonewline $EQNS)! }
107
108 NewCurrentPrefix="SC_"
109 Transient (
110 InitialTime=0 FinalTime=13e-6
111 InitialStep=1e-8 MinStep=1e-15 MaxStep=2e-5
112 Increment= 1.35 Decrement= 2.1
113 ){ Coupled (digits=3 iterations=12 notdamped=50) { !(puts
       -nonewline $EQNS)! }
114 }
115 }
```

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