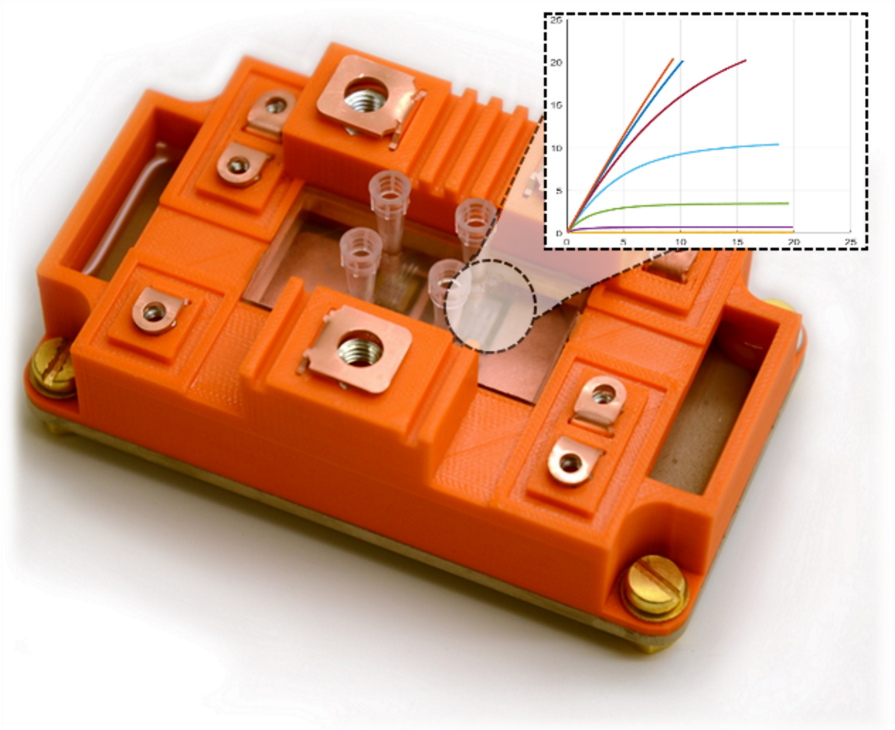
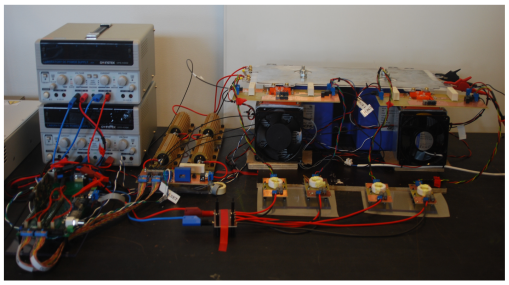
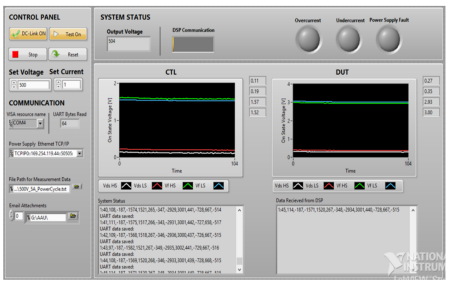
Power Cycle Test Bench for Accelerated Life Testing of 10 kV SiC MOSFETs

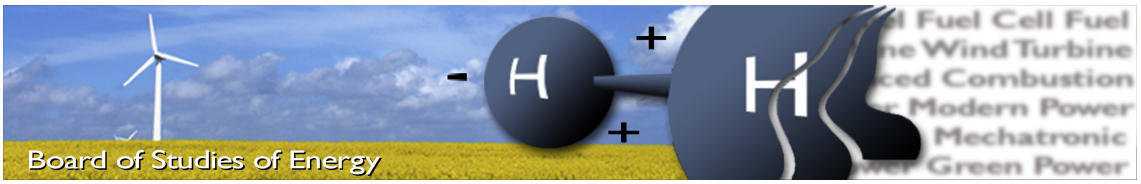






AALBORG UNIVERSITY
STUDENT REPORT

Master Thesis
Group PED4-1041
Department of Energy Technology
June 1st 2016



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Abstract:

Recent advancement in the area of medium voltage SiC MOSFETs are approaching the maturity level necessary for practical applications and emerging as a potential competitor for Si IGBTs. However since the SiC MOSFET manufacturing process are different from Si production and limited application related experience are available for the reliability of SiC devices. Investigating the defect growth and failure modes in an application relevant environment for SiC are therefore a necessity. A power cycling test-bench for medium voltage has therefore been built to expose SiC Modules to temperature swings during AC operation. The performance of the test-bench is thoroughly verified. The module tested consist of first generation 10 kV SiC MOSFETs and diode dies, packaged at Aalborg University. A detailed infant characterization of the SiC module is performed for post mortem fault behaviour investigation. During power cycling tests the conduction voltages of the SiC dies are measured for monitoring degradation and used as an indicator for state of health.

By signing this document, each member of the group confirms that all group members have participated in the project work, and thereby all members are collectively liable for the contents of the report. Furthermore, all group members confirm that the report does not include plagiarism.

Preface

This report serves as documentation for the the work performed during the Master thesis in Power Electronics and Drives at the School of Engineering and Science, Aalborg University. The Master thesis is a short thesis expanding over a time period of 4 months.

Acknowledgements

Authors would like to express their deepest gratitude to their supervisor Prof. Stig Munk - Nielsen for his constant guidance, continuous support and encouragement. Authors are grateful to Assoc. Prof. Szymon Beczkowski, Assoc. Prof. Christian Uhrenfeldt and PhD Emanuel - Petre Eni for their inputs and valuable technical discussions during the project work. Authors would also like to thank IEPE for providing necessary test equipments for the project work.

Finally author's heartfelt appreciation go towards their family, friends and colleagues for their continuous support, motivation and help during the Thesis work.

Reading guide

In the report, sources are referred to using the Harvard Method ([number]). Additional information about the sources is found in the bibliography in the end of the report, listed by author in alphabetic order. If jumped to a reference, pressing "ALT + Left Arrow" simultaneous will return the reader to the last visited page. A CD is attached to the report. When referring to content on the CD the icon, is used along with a footnote containing the path of the material on the CD.

Figures and Tables are labeled by Chapter.number of Figure/Table. Equations are labelled similarly but in parenthesis, so that (4.1) indicates the 1st equation of Chapter 4. Sources of Figures and Tables are shown in the caption. If no source is present, the Figure or Table is constructed by the group.

Contents

Summary

Recent trend is towards achieving high power density and efficiency in power electronics converters and WBG devices are promising candidates to provide the performance required. Recent advancement in the area of medium voltage SiC MOSFETs are approaching the maturity level necessary for practical applications and emerging as a potential competitor for Si IGBTs. However, reliability related data in an application relevant environment for newly developed medium voltage SiC MOSFETs are not available. Therefore, this thesis work is carried out with an aim to investigate the reliability of 10 kV SiC MOSFETs. To carry out the accelerated life testing a medium voltage power cycling test bench with necessary safety protection and dedicated LabVIEW interface was designed. On state conduction voltages of MOSFETs and diodes are measured for monitoring degradation during accelerated wear out test. The 10kV/10A SiC MOSFET half bridge power modules used for the experimental work are packaged at the Department of Energy Technology, AAU. The modules are manufactured in two configurations: with and without external anti - parallel JBS diode.

An initial analysis of known failure modes and behaviour of Silicon and Silicon Carbide devices has been performed. The analysis provided knowledge of which electrical parameters being effect by the different failure modes and the necessity of a detailed characterization of a module before and after stress. The characterization data can be used for determining the fault behaviour produced and locating the root cause responsible for the failure.

A simulation based study was carried for the medium power cycling test bench. With the purpose of designing a controller and determine the distribution of the current stress level on the power modules. A Complete design and development of the hardware such as gate driver incorporating V_{ds} and V_f monitoring circuit, isolated gate driver power supply, protection circuit and DC - Link busbar has been performed.

An experimental validation of the designed power cycle test bench with a duration of 2 hours has been performed, proving its functionality. This includes documentation on controller stability of the power cycle test bench and conduction voltage measurement results at low voltage for minimum temperature stress on the devices. During the project work infant device characterization was performed. Based on the characterization data, a brief comparison between half bridge module consisting of Gen.1 and discrete Gen.3 SiC MOSFET die is presented. The comparison shows indications of improvement for preventing some of the new failure modes present in SiC MOSFET as for example reduced gate bias needed for operating with low on-state resistance and a decreased in on-state resistance and forward voltage indicating improvement in preventing stacking faults. The characterization data obtained can be utilised for device modelling and to investigate the

fault behaviour after degradation of the module.

Test results for power cycling performed at low voltage level shows a consistent measured conduction and forward voltage. The values of measurements during power cycling is in good coherence with the characterization performed in a curve tracer before power cycling. The test results includes the die surface temperature measurements of MOSFETs and diodes during power cycling for validating the stress levels exerted on the modules.

With the testbench operation validated and a detailed infant characterization of the modules being performed, the final step and future work will be to increase the voltage until an operation point is achieved within the temperature limit of the packaged module. When that operation point is defined a continuous power cycling will be executed until conduction or forward voltage measurements indicate wear out degradation.

Table of symbols

Table 1. Table of symbols used in the report.

Symbol	Unit	Name
BW	Hz	Bandwidth
C	F	Capacitance
C_p	F	Parellel parasitic capacitance
C_W	F	Inter winding capacitance
D	-	Duty cycle
E	J	Energy
f_{sw}	Hz	Switching frequency
i	A	Current
i_d	A	Drain current
i_f	A	Forward current
L	H	Inductance
N	-	Number of windings
P	W	Power
R	Ω	Resistance
R_g	Ω	Gate resistance
R_{ds-on}	Ω	Drain - source on state resistance
t	s	Time
T_{sw}	s	Switching period
T_{smp}	s	Sampling period
V	V	Voltage
V_{dc}	V	DC - Link voltage
V_{ds}	V	Drain - Source voltage
V_{gs}	V	Gate - Source voltage
V_{gs-th}	V	Gate - Source threshold voltage
V_f	V	Forward voltage
N_f	-	Number of cycles to failure
ΔT	° C	Temperature difference

Table of abbreviations

Table 2. Table of abbreviations used in the report.

Abbreviation	**Long Form**
ADC	Analog to Digital Converter
ALT	Accelerated Lifetime Test
BPD	Basal Plane Dislocations
CTE	Coefficient of Thermal Expansion
CTL	Control
DBC	Direct Bonded Copper
DFIG	Doubly Fed Induction Generator
DSP	Digital Signal Processor
DUT	Device Under Test
ESR	Equivalent Series Resistor
HS	High Side
IC	Integrated Circuit
JBS	Junction Barrier Schottky
PWM	Pulse Width Modulation
IGBT	Insulated Gate Bipolar Transistor
LS	Low Side
LSB	Least Significant Bit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTBF	Mean Time Between Failures
PCB	Printed Circuit Board
PoF	Physics of Failure
PR	Proportional Resonant
RBD	Reliability Block Diagram
SF	Stacking fault
Si	Silicon
SiC	Silicon Carbide
TDDB	Time Dependent Dielectric Breakdown
WBG	Wide Band Gap

Chapter 1

Introduction

Continuous growth of power electronics used in wind turbines since 1980s initiated a shift from DFIG to full scale power converters around 2005 [13]. Full scale power converters are larger and requires higher power density semiconductors with high modularity and reliability. Until now the predominant semiconductor devices used for high power converters are Silicon (Si) IGBTs. Si IGBTs conduction losses consists of an on-state saturation voltage V_{CE_sat} and an on-state resistance. As IGBTs offer low on state resistance and saturation voltage, the resulting conduction losses for IGBTs are lower compared to Si MOSFETs. The Si IGBT provides medium voltage withstand capability and high thermal conductivity which combined with low conduction losses ensures a high power density. The draw back of using IGBTs are the relatively large switching losses when compared to MOSFETs. For example, energy dissipation during each switching cycle is 0.32 mJ for a Si IGBT [17] compared to 0.051 mJ for a Si MOSFET [18] both with 600 V and 10 A of ratings. Recent development in the area of wide bandgap (WBG) devices and in particular medium voltage SiC MOSFETs is a potential competitor of IGBTs and an expected replacement in high frequency and high power conversion applications. SiC MOSFETs has several advantages compared to Silicon counterparts, one of which is more than three times the thermal conductivity. Combining the increase in thermal conductivity with the low switching losses, low on state resistance and ten times the breakdown field strength, the SiC MOSFETs can provide a higher power density compared to Si IGBTs. The values taken as a reference is for the Silicon Carbide material 4H-SiC [35] and it indicates that SiC excels over Si as a semiconductor material. A calculation of the power densities for Silicon and Silicon carbide dies has been graphically illustrated in Figure 1.1.

Figure 1.1 illustrates the limitation of the silicon power semiconductor devices. The Silicon carbide modules obtain approximately six times the power density of their silicon counterparts together with breakdown voltages above 10 kV. The significant increase in power density and breakdown voltages indicates the increase of modularity obtained with the SiC technology. The SiC MOSFET therefore becomes a very plausible candidate for replacing the Si IGBT. Another advantage of replacing IGBTs with MOSFETs is the increase in switching frequency which will reduce the size of magnetic components and filter requirements to fulfil the grid codes of total harmonic distortion (THD).

Since the SiC MOSFET manufacturing process are different from Si production and the defect level for SiC is much higher and limited application related experience are available for SiC devices. The defect growth and failure modes must be investigated in an application relevant environment, stressing SiC devices and identifying defect growth and failures not found in todays Si devices.

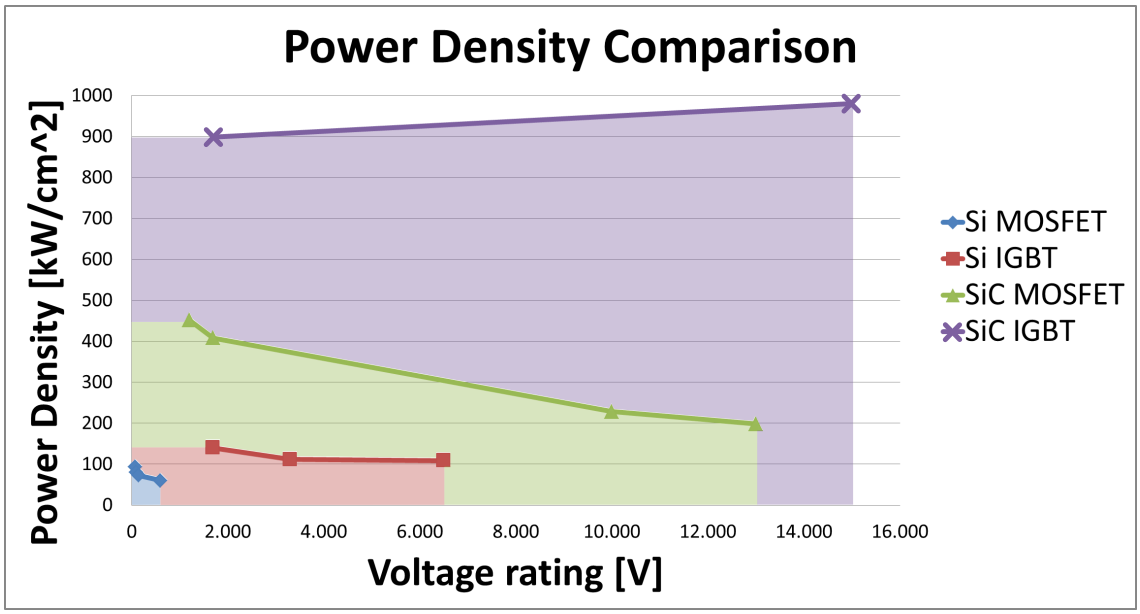


Figure 1.1. Power density for semiconductor dies as a function of rated breakdown voltage. Si MOSFET [24], Si IGBT: [1], [25], SiC MOSFET: [6], [44], SiC IGBT: [37]

The main objective of the project will therefore be to perform an accelerated lifetime test (ALT) with the goal of stressing the module by power cycling it until a degradation failure mechanism occur. A failure caused by degradation is an end-of-life failure, which will occur with an increasing failure rate. The life-time and failure rate can generally be explained by a bathtub curve as seen in Figure 1.2.

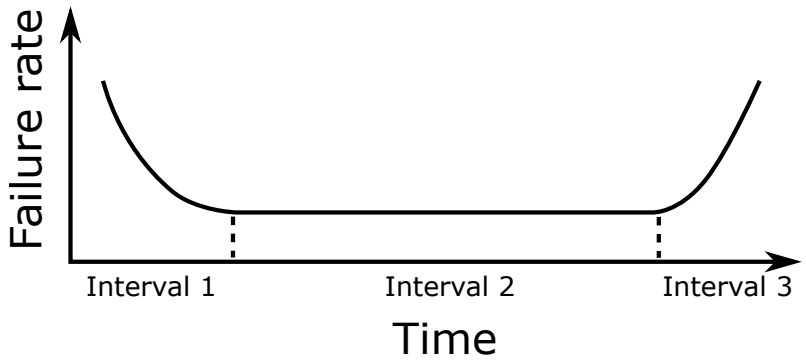


Figure 1.2. Bathtub curve illustrating the hazard function of a component.

The bathtub curve are split into three intervals, describing the failure rate during its lifetime [15,p. 9]. The three intervals are explained in the following three bullet points.

- **Interval 1:** The interval are representing the infant mortalities occurring due to quality control issues and has a decreasing failure rate over time. Burn-in tests are performed to screen for infant mortalities.
- **Interval 2:** The second interval is called useful life time period. The failure rate is dominated by random failures such as overcurrent, overvoltage or short circuit failures. The failure rate is widely assumed to be constant during the interval.

- **Interval 3:** The third interval describes the degradation failures at the end-of-life period. The failure rate is increasing due to the degradation caused by accumulated damage.

The third interval will be the main focus of the project. The ALT will be performed to accelerate the SiC module to the end-of-life (corresponds to Interval 3 of a bathtub curve). The ALT will be performed using a power cycling and V_{ds} measurement for state-of-health monitoring. The ALT will provide information about the MTBF and the location of the fault for accessing and improving the reliability of a SiC module. An approach to access the reliability is using a Reliability Block Diagram (RBD). The reliability block diagram is a graphical presentation of how failures effects the reliability of a component. An example of a RBD for a converter from a point of view of power semiconductor module is specified in Figure 1.3. If the path from die to converter is obstructed due to any fault, the component will fail. Parallel connecting blocks as is performed with bond wires will increase the redundancy of the system and its reliability [30].

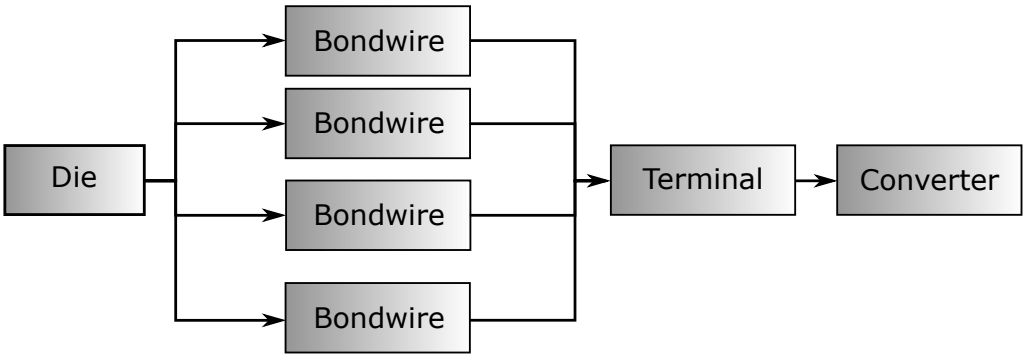


Figure 1.3. Reliability block diagram of a semiconductor die

Inside a bond wire packaged module, several aluminium bond wire are often put in parallel to create a low resistance path from the semiconductor die to the terminals of the module. One of the weak links in the reliability block diagram seen in Figure 1.3 have been the bond wires for Si modules [15,p. 90-99]. If a bond wire is disconnected due to a fault, the remaining bond wires will experience a higher stress level and the degradation rate of the module increases. If all bond wires are disconnected the path from die to converter will be obstructed and the converter will experience a fatal fault and no longer function.

The SiC modules which will be tested in the project are in a half bridge configuration as presented in Figure 1.4.

As can be seen in Figure 1.4, the external diode used for bypassing the intrinsic diode occupies physical space inside the module, space which could have been used for a MOSFET. CREE recommends to bypass the intrinsic/body diode for Generation 1 SiC MOSFET, however for the Generation 3 SiC MOSFET this is no longer a requirement. The ALT test will therefore be performed without external SiC JBS diode to utilize the SiC MOSFET intrinsic diode. The space occupied by the external diode can now be utilized by a MOSFET (in parallel connection) to increase the power density of the module. The obtained knowledge regarding its effect on reliability is crucial for accessing its feasibility. If using the intrinsic diode decrease the reliability significantly, the increase

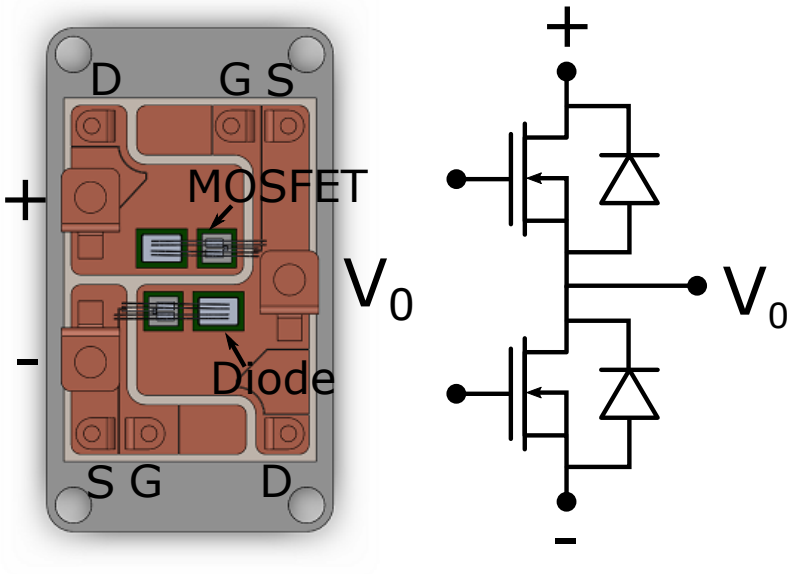


Figure 1.4. Schematic and SolidWorks drawing of physical construction of a half bridge module with external diode. SolidWork drawing is made by Szymon Beczkowski.

in power density will not be a cost-effective solution due to the time consumption and high expenses related to maintenance and repairs [5].

Before a problem statement will be formulated, a state of the art review of the failure mechanisms related to wire bonded modules will be presented for Silicon semiconductor devices, due to the limited experimentally proven knowledge of failure mechanism in Silicon Carbide modules. The expected failure mechanism will be used to methodically investigate the modules after power cycling to locate the failure.

1.1 Failure Mechanism of wire bonded modules

A ranking of importance for different stress factors has been established, giving an overview of which factors is crucial for the degradation of the components inside a semiconductor device. The overview is given in Table 1.1 [15].

Table 1.1. Focus point matrix in reliability for semiconductors, LASJ - Large Area Solder Joint, level of importance in descending order: **X**, X, x [15]

Stressors	Die	LASJ	Bond wire
Temperature Swing δT	**X**	**X**	**X**
Mean Temperature T	X	X	X
Temperature derivative dT/dt	x	x	x
Chok / Vibration	x		

From Table 1.1 it can be seen that temperature swing is the most important stress factor effecting the reliability of a die and its electrical connections. Based on the knowledge regarding stress factors it is chosen to perform power cycling introducing temperature swings. From Table 1.1 it is presented that the rate of temperature swings are not as important as the magnitude of temperature swing, when stressing the device. The average

mean temperature however has an considerable effect on the reliability and is an important parameter to quantify.

A power cycling test will therefore be used to induce temperature swings by means of conduction losses. Since semiconductors for wind turbines typically are developed with a targeted lifetime of 20 years [15], an accelerated life time test is needed. The accelerated life time test will be performed by inflicting an increased magnitude of stress on the semiconductor, to reduce the number of cycles before failure. The principle of an ALT is to increase the stress level to a magnitude at which no abnormal failure mechanisms occurs with the goal of minimizing the time at which the devices is tested. The ALT can be graphically illustrated by a Stress-Life curve as given in Figure 1.5 [33].

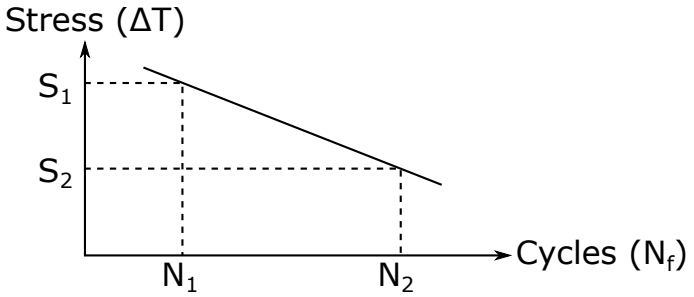


Figure 1.5. Stress-Life curve illustrating the increased rate of accumulated damage with increased stress magnitude.

High magnitudes of temperature swing is then used to expose the weakest links in the reliability block diagram, to evaluate on the reliability of the SiC device and locate the limiting factors for achieving higher reliability. With the knowledge of the important stress factors and the objective of an ALT, the next step is therefore narrowing down the focus to the failures expected. To do so an investigation of the physics of failures (PoF) for the bond wire Silicon devices will be discussed in the following section, for identifying the weak link present in the module and the tests needed to do so.

1.1.1 Physics of Failure

Before presenting the knowledge of failure mechanism for bond wire Silicon modules, a brief description of the power module packaging will be presented. The general cross sectional structure of a wire bonded module can be seen in Figure 1.6 together with a photograph of a module in Figure 1.7.

The bond wire module consists of a die, which can be of different types of semiconductors for example a diode or a MOSFET. The anode of the diode or drain of the MOSFET is soldered onto a plane of copper which can be electrically isolated from the heat sink using a ceramic. The ceramic is covered with copper on both sides enabling it to be soldered to a copper baseplate and thereby achieving a low thermal resistance between die and heat sink [26]. The gate, source or cathode are connected to its terminal using bond wires consisting of Aluminium for high current application. The bond wires are connected to the die or copper using ultrasonic wedge bonding [32,p.8]. The terminals of the module are connected to a copper plane using ultrasonic welding ensuring a strong connection

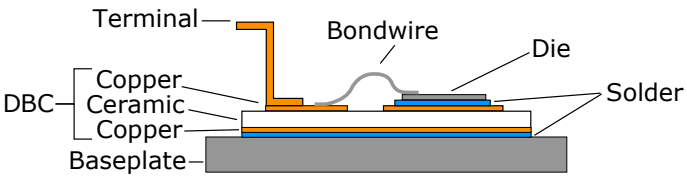


Figure 1.6. Basic structure of a wire bonded module.

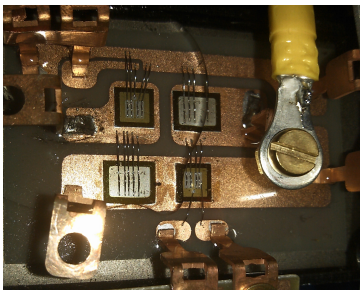


Figure 1.7. Photograph of an earlier version of the 10 kV SiC bond wire module

between the terminal and copper plane without the use of adhesive, similar to the bond wire connection.

The failure mechanism of wire bonded Silicon modules has been comprehensively studied [26], [5], [36]. The failure mechanism for Silicon modules will be presented in the following section, to obtain a methodical way of diagnosing the different failure types based on their fault behaviour. The different failure types and their cause will be presented together with their behaviour and the possible methods of observing these, resulting in a systematic way of fault diagnosing the SiC modules based on available knowledge from Si modules.

Bond wire cracking/lift off

In a typical power electronics module there are many bond wires making electrical interconnection from the power device to substrate, from the substrate to the external connectors, from the power device to the external connectors as well as between power devices. Bond wire cracking or lift off is a fault which disconnects the electrical connection of the bond wire from die or copper plane. The fault can result in malfunction of the specific device or increased stress of the remaining bond wires which will advance the rate of degradation. Many bond wires are bonded to a semiconductor or copper plane and will experience the temperature swings caused by the power dissipation in the power devices and due to the self heating as a result of ohmic drop. The temperature swings produces shear stress between bond wire and the semiconductor producing mechanical fatigue, resulting in heel cracking or lift off. The shear stress is caused by the difference in coefficient of thermal expansion (CTE) [15]. The location of the fault can be observed in Figure 1.6 between the bond wire and die.

Explanation: Expl
Bond wire lift off is categorised as an open-circuit failure and usually occurs due to large temperature swings at the bond wire terminations bonded onto the device. Bond wire lift off from the copper plane is not occurring often compared to at the die due to lower temperature swings present at the copper plane and bond wire connection. Several bond wires are often placed in parallel meaning the failure might not be immediately fatal for the converter, however the stress of the remaining bond wires will increase. The increased stress will advance the degradation unavoidably resulting in a malfunction. The main mechanism of bond wire lift off is related to the mismatch between the Aluminium and

Silicon coefficients of thermal expansion (CTEs) [36]. Since there is a mismatch of CTEs between Silicon Carbide and Aluminium as well, the fault is also expected to be present for a SiC module. The bond wire heel cracking is a flexure fatigue, which results due to the expansion and contraction of the bond wire when subjected to temperature swings. One of the important factor is the bond wire loop height as it determines the angle at the heel of a bond wire. Also, module encapsulation plays a role in a bond wire heel cracking. [15] Statistically bond wire heel cracking is occurring after a higher number of temperature cycles than bond wire lift off.

Table 1.2. Table with coefficient of thermal expansion, [5], [45].

Material	CTE
Aluminium (Al)	$23.5 \cdot 10^{-6} K^{-1}$
Copper (Cu)	$17.5 \cdot 10^{-6} K^{-1}$
Silicon (Si)	$2.6 \cdot 10^{-6} K^{-1}$
Silicon Carbide (4H-SiC)	$3.2 \cdot 10^{-6} K^{-1}$

Fault Behaviour: β
When a bond wire cracks or lifts off the overall cross sectional area used for conduction will be reduced, increasing the resistance of the connecting path. The increased resistance will introduce an increase in the drain-source voltage and power dissipation during on state. The increased power dissipation will introduce larger temperatures and increase the rate of degradation for the device.

Observation: σ
The failure can be observed by measuring the on state drain-source voltage, increased temperature or by a visual inspection of the bond wires which could be performed using an acoustic microscope.

Die solder fatigue

The functions of the solder between die and direct bonded copper (DBC) are to provide an electrical and thermal conduction path with low resistance. Normal operation of the module will produce large temperature variations between die and baseplate. The temperature variations will produce mechanical stress due to CTEs mismatch causing the formation of voids and cracks from present voids or impurities. Special care is therefore taken to minimize the formation of voids during the packaging process to ensure low thermal resistance and preventing solder fatigue. The die solder fatigue could be a dominant failure for the SiC devices due to the increased allowed operating temperature for the dies reaching a theoretical limit of $600°C$ [38]. No packaging today can however take full advantage of the thermal capabilities of the SiC dies.

Explanation: Expl
The temperature variations between die and DBC causes residual stress due to CTE mismatch. The residual stress causes fatigue of the solder layer producing voids and cracks increasing the thermal and electrical conduction resistance.

Fault Behaviour: β
If a crack or a void would emerge a result could be obstruction of the heat path, creating

large local temperature gradients. The electrical resistance might also increase due to voids and cracks, changing the current distribution and increasing the drain-source on state voltage of the MOSFET or forward voltage of the diode. The worst case would be a reduction in thermal conductivity without the increase of electrical resistance, since a temperature increase of the junction will be present.

Observation: σ
The cracks and voids can be observed by taking an image using a Scanning Acoustic Microscope. The fault can also be observed as a local temperature increase or increased conduction voltage of diode or MOSFET.

Gate oxide film deterioration

The gate oxide film is a dielectric layer separating the gate terminal of a MOSFET from the source as can be seen in Figure 1.8. The failure of the oxide film can either be caused by an infant defect or deterioration. If an infant defect is present in the oxide film it will result in an early failure. Continuous application of a gate-source voltage within its rating for an extended period of time can also cause breakdown. This type of failure is referred to as time dependent dielectric breakdown (TDDB) with the most important factor of failure being high-temperature bias [28].

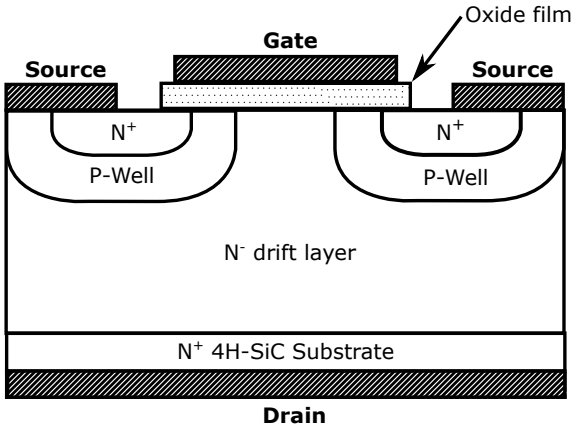


Figure 1.8. Structure of a SiC DMOSFET.

Explanation: Expl
When the on state gate-source voltage is applied, a high electric field stress will be present across the oxide film. A high electric field stress applied will implant electrons in the oxide film. These electrons are refereed to as hot electrons and will generate more electrons and positive holes. The electrons implanted in the oxide film will cause high local electrical fields which eventually will lead to dielectric breakdown of the gate oxide film.

Fault Behaviour: β
The deterioration of the oxide film layer can result in a drift of the gate-source threshold voltage V_{th}. A recent publication investigating the voltage drift for second generation SiC MOSFET dies present result for a maximum voltage drift of 280 mV with a gate-source voltage of 20 V for 1000 hours. When the positive bias is removed the ΔV_{GS-th} rapidly reverses indicating stable threshold voltage under normal switching operation [3]. The

deterioration of the gate oxide film could also increase the gate leakage current.

Observation: σ
A measurement of the drain-current can be measured during a sweep of gate-source voltage. However to determine weather a drift occurs or not an infant measurement of the threshold voltage is needed. Gate leakage current can be measured using a curve tracer, however infant measurement for reference is also needed for comparison.

Stacking Faults

The formation of stacking faults is due to the hexagonal crystal structure in Silicon-carbide. This is a new failure mechanism since silicon has a diamond-cubic structure. The crystal structure of the Silicon-carbide is not as strong resulting in basal plane dislocations (BPDs) are travelling through the thickness of the drift-layer to the surface of the wafer. The BPD is a displacement of the crystal structure resulting in the formation of stacking faults (SFs) which increases the on-state resistance of the MOSFET, the forward voltage of the diode and the leakage current. The formation of SF can be significantly reduced by using a drift-layer with a low density of BPDs (LBPD). The change from Gen. 1 to the new generation should be the use of LBPD enabling the use of the intrinsic diode. The failure mechanism was observed in 1 Gen. 10 kV SiC MOSFET with a DC current conducted through the intrinsic diode. [2]

Explanation: Expl
The BPD occurs during forward conduction and are causing the formation of SF which increases the conduction voltage of both diode and MOSFET. The physical explanation of why is still under debate, however the effect of the failure and is behaviour is not. [2]

Fault Behaviour: β
The energy causing the activation of the dislocation glide is provided during conduction of the intrinsic diode. The effect of dislocation glides are the formation of SFs which are increasing the leakage current, on-state resistance of the MOSFET and the forward voltage drop of the intrinsic diode. The increase of R_{DS-ON} can be seen in Figure 1.9 under a DC current stress of the intrinsic diode.

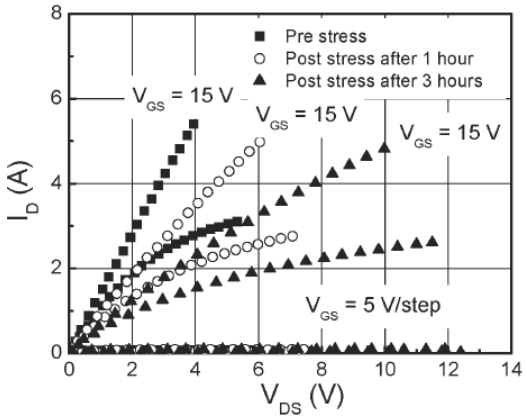


Figure 1.9. V_{DS} and I_D characteristics for a 1st gen. SiC MOSFET with stressed intrinsic diode. [2]

Observation: σ
The Failure mechanism can be observed as an increased in on-state resistance R_{ds-on} which can be measured using the conduction voltage, if the voltage is known prior to stress. An increase in the conduction voltage of the intrinsic diode or as an increased leakage current compared to initial value.

Voltage drop in gate driver output

The voltage drop of the gate driver is categories as when the on state or off state voltage reduced in magnitude causing increased rise and fall times or gate-source resistance. The increase in rise and fall times can produce short circuit failures leading to destruction of the module. The increase in gate-source resistance can result in thermal run away due to excessive conduction losses.

Explanation: Expl
The gate driver output voltage can drop due to different malfunction in the gate driver and isolated DC/DC converter. If the gate-source positive bias drops below 15 V the SiC MOSFET will not exhibit a low on resistance. The gate-source positive bias is therefore recommended to be 18 V to ensure low R_{ds-on} and thereby low conduction losses to prevent thermal run away [35].

Fault Behaviour: β
The fault will present it self as increased rise and fall times, increase R_{ds-on}, drain-source on state voltage and increased temperature variations of the SiC MOSFET. The fault can be observed at the output connection of the DC/DC converter or at the gate-source as a reduced voltage.

Observation: σ
The fault can be observed by measuring the output voltage of the isolated DC/DC converter and gate-source voltage, as an increase in V_{ds-on} or increased junction temperature swings.

1.2 Problem statement

In this section two hypothesis will be presented, for which the the rest of the report will move towards the answer. The hypothesis is established based on the knowledge obtained and presented in the earlier sections of this chapter.

1.2.1 Objective and Scope

The main objective of the project is to investigate the reliability of the intrinsic diode for the Generation 1 and Generation 3 10 kV SiC MOSFET. A power cycling test bench will be utilised to perform an accelerated lifetime test by introducing temperature gradients. The power losses will then be used to explain temperature measurements performed on the surface of the die. A detailed characterization of the module will be performed utilizing a curve tracer for explaining future fault behaviour present by the modules after degradation. Comparison of a Gen. 1 and Gen. 3 MOSFET will be performed for investigating improvements in next generation dies. Degradation of the Gen. 1 SiC MOSFET will be experimentally monitored using the V_{ds-on} and V_f as an indication of the state of health for the power module. The following two hypothesis is presented in the bullet points below.

- **Hypothesis 1:** The Generation 3 SiC MOSFET has improved body diode performance, enabling a reliable operation as compared to Generation 1 SiC MOSFET.
- **Hypothesis 2:** The degradation of SiC MOSFET can be analysed by using a V_{ds_on} measurement as a state of health monitoring.

To answer the hypothesis, a number of task has to be completed. These task are used as a guideline for the project work.

Sub Tasks

- Building a Power Cycling test bench with necessary protection.
- Design a gate driver incorporating the V_{ds} measurement circuit.
- Design a controller and implement measurement routines for state of health monitoring
- Verify temperature variation during accelerated life testing (ALT)
- Analyse SiC modules fault behaviour utilizing a curvetracer before and after stress.

1.2.2 Limitation

The project has limitation due to available lab equipment and a limited time frame.

- The power cycling will be performed at 5 kV due to limitation of the DC link capacitors voltage rating.
- A packaged power module containing Gen. 3 10 kV SiC dies is not yet available.

Chapter 2

Power cycling test bench

This chapter aims to provide information to the reader on the design of Power Cycle Test bench. Performing the ALT (Accelerated Life Testing) on 10 kV SiC MOSFET will require a test bench capable of operating at medium voltages with necessary safety protections and gate driver circuit incorporating MOSFET V_{ds-on} and diode V_f measurement circuit. Moreover, to stress the devices under controlled environment and to obtain the desired temperature swing current controller should also be designed. Current controller design and stability region determination is important to prevent over current and ensure that current will follow the desired reference. Knowledge of the Device stress distribution in a test bench is required so that the desired stress level can be achieved specifically on the device under test (DUT). Inverter non-linear characteristics with focus on the voltage error introduced by the deadtime is discussed and compensation technique to prevent the distortion in the output voltage is presented. Measurement technique implemented to obtain the device conduction voltage is discussed at the end of this section.

2.1 Working Principle

For the power cycling test setup an H bridge converter topology is used as shown in Figure 2.1. The load inductor L consists of a ferrite core and air coil inductor. Main objective of the test set up is to stress the device under a repeated thermal cycling inducing the temperature swing ΔT_j at device junction. Desired temperature swing ΔT_j at the junction can be obtained by controlling the amplitude and fundamental frequency of the load current cycled through the power modules. The device blocking voltage and amplitude of the load current is kept below the nominal rating of the power module. With this approach a similar stresses and operating condition that a power module would experience in real life application can be exerted under accelerated conditions. The test setup consists of two half bridge power modules utilizing 10 kV SiC MOSFETs and potentially JBS diodes. Each of these converter legs are referred to as Control (CTL) or device under test (DUT). The DUT leg is modulated using a sinusoidal voltage reference and the CTL leg is modulated using a feedback control loop including a proportional-resonance controller and a feed forward of the DUT voltage reference. The power cycling until wear out is expected to have a duration of one to two weeks before the DUT module reaches a certain level of degradation indicating an upcoming failure. This approach provides an economical way of assessing the reliability of the device as the power source needs to supply the power losses of the semiconductor devices and the inductor. The outcome of the power cycling test is the number of cycles to failure N_f which can be used in models for lifetime estimation or identifying the limiting factors of the reliability for the device.

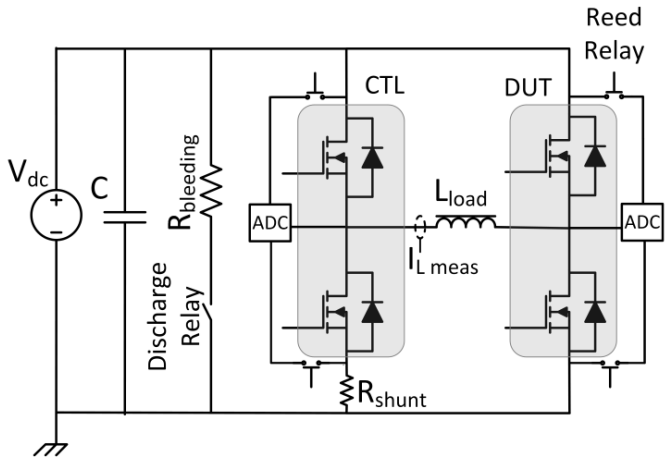


Figure 2.1. H bridge converter topology

It is important to identify the current stress distribution of the MOSFETs and diodes respectively to understand and investigate the root cause of failure presenting it self. An analysis of the relative current stress distribution is therefore performed in the following section to quantify the stress distribution under different operating conditions and how to control it.

2.2 Current Stress Distribution

As discussed before, the goal is to access the reliability of SiC MOSFET with focus on the new failure mechanism of the intrinsic diode. Therefore, it is important to apply stress on the intrinsic diode of the MOSFET in DUT during the ALT. In the test setup, this can be done by controlling the current to conduct primarily through an intrinsic diode during a switching period. This can be achieved by controlling the duty cycle of the CTL module and/or changing the angle of the current (θ_{shift}) in a full bridge configuration as presented in Figure 2.1. [1]

[1] `PLECS\stress_distribution.plecs`

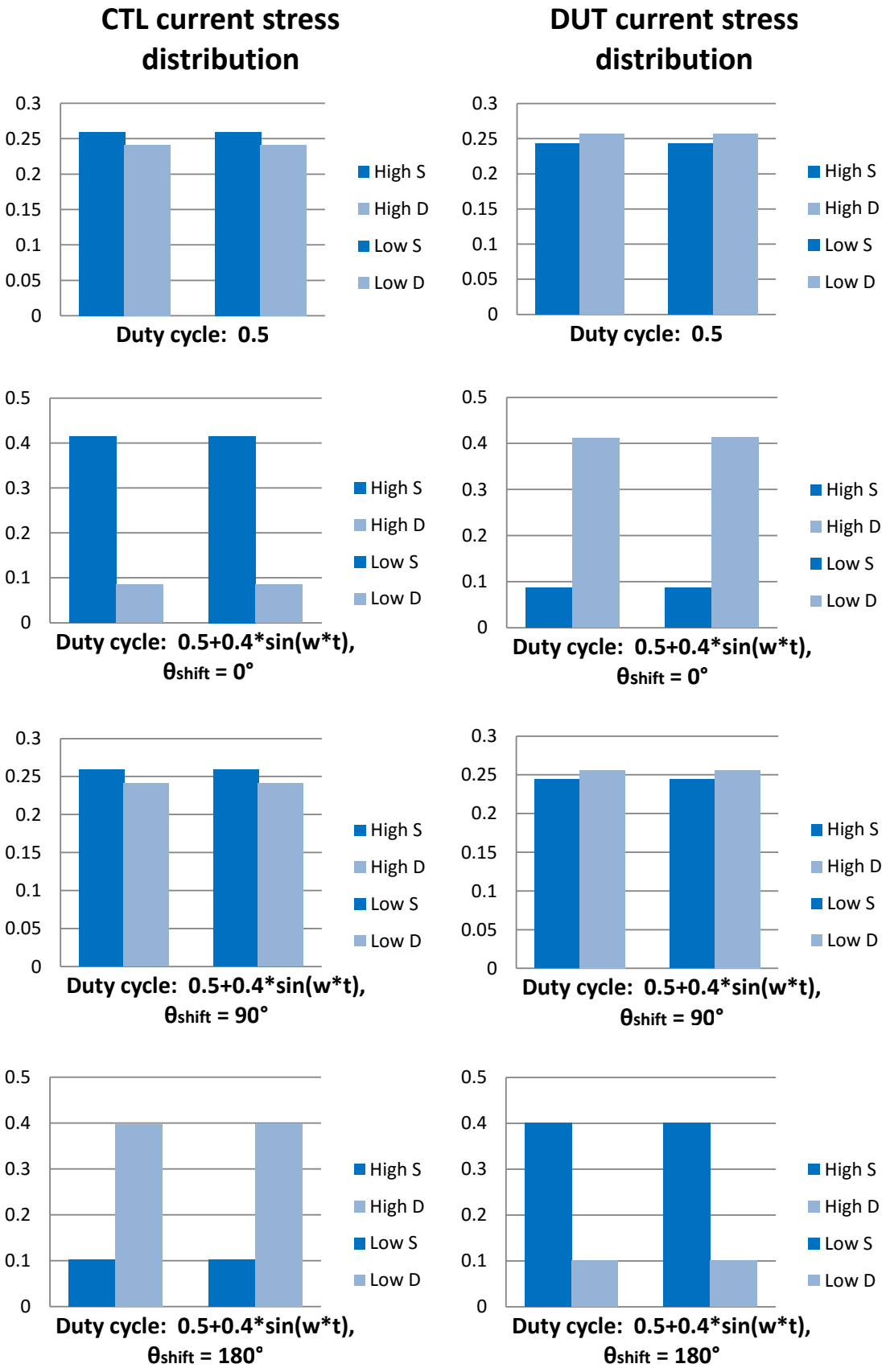


Figure 2.2. Current stress distribution in a CTL and DUT half bridge modules as a function of duty cycle and angle of current

The relative current stress distribution for MOSFETs and intrinsic diode in CTL and DUT module as a function of duty cycle and current angle is presented in Figure 2.2. The following bullet points will explain the distribution under the cases presented in the figure.

- For a duty cycle D = 0.5 the current conducts through MOSFET and intrinsic diode for approximately equal amounts of time during a switching period in both leg of the converter. Meaning that, the stress experienced by MOSFET and intrinsic diode is approximately similar for both CTL and DUT module.
- In the case when duty cycle D = $0.5 + 0.4 * \sin(\omega_0 t)$ and $\theta_{shift} = 0°$., current conducts mainly through MOSFET of CTL module and diode of DUT module. In this case, the intrinsic diode in the DUT will experience higher stress compared to MOSFET.
- From figure it can be seen that MOSFET and diodes in CTL and DUT are stressed approximately equal on both leg of the converter when D = $0.5 + 0.4 * \sin(\omega_0 t)$ and $\theta_{shift} = 90°$. Almost similar stress distribution will be obtained for the cases when D = 0.5, D = $0.5 + 0.4 * \sin(\omega_0 t)$ and $\theta_{shift} = 270°$.
- For the case when D = $0.5 + 0.4 * \sin(\omega_0 t)$ and $\theta_{shift} = 180°$, MOSFET of CTL and intrinsic diode on DUT module will experience minimum stress. The stress distribution in this case is almost opposite compared to previous case, when D = $0.5 + 0.4 * \sin(\omega_0 t)$ and $\theta_{shift} = 0°$.

For the stress distribution presented above, the switch is bypassed when conducting current through the external and intrinsic diodes. In reality the gate signal to the switch is high meaning a current sharing between MOSFET and diodes will be present during PWM switching. This is however neglected due to values of R_{ds-on} and V_f not being available at the time. However it gives an indication of the time duration for which current flows from source to drain.

2.3 Control

As described in the previous section the objective is to control the amplitude and frequency of the current through the load and devices.

In order to control the load current which is dependent to the voltage appearing across the load inductor, the output voltage from each of the half bridge needs to be controlled to meet the demanded current reference. One of the leg (DUT module) is controlled in an open loop configuration and the another leg (CTL module) is controlled by a current controller.

Due to the voltage reference being a sinusoidal, the current controller is implemented using a PR - Proportional Resonant controller. A PR controller was chosen due to its ability to track the sinusoidal reference with zero stationary error. A block diagram for physical converter control loop is shown in Figure 2.3 together with its simplified equivalent. The block diagram is simplified for tuning the controller, determining the stability and response of the system using root locus analysis.

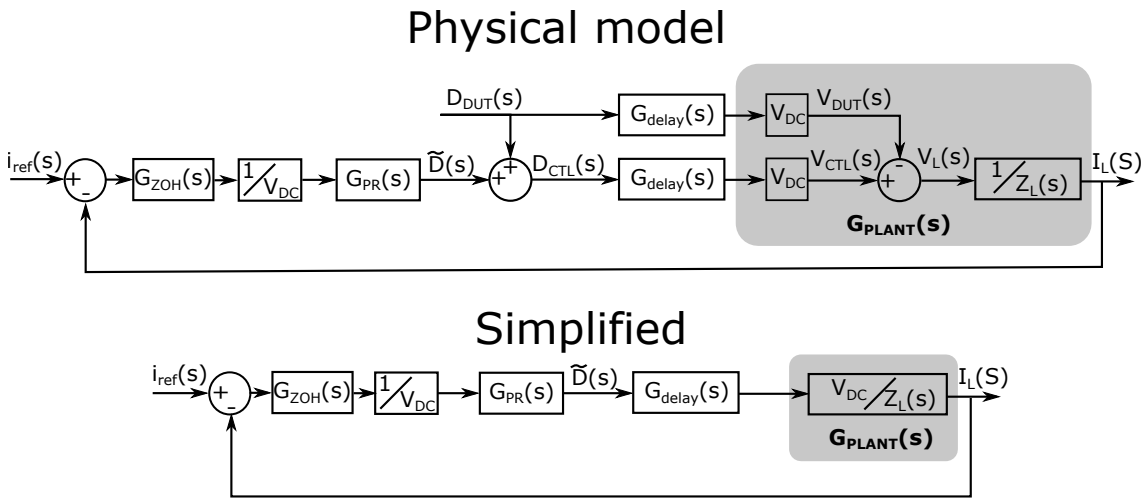


Figure 2.3. Block diagram: Current control loop

For a given system, plant is the load inductor L_{load}. Practical inductor consist of a parasitic series resistance and parallel capacitance. The resulting impedance Z_L in the laplace can be expressed as seen in (2.1) and (2.2).

$$Z_L(s) = (R + s \cdot L) || \frac{1}{s \cdot C_p} \Rightarrow Z_L(s) = \frac{(R + s \cdot L) \cdot \frac{1}{s \cdot C_p}}{R + s \cdot L + \frac{1}{C_p}} \tag{2.1}$$

$$Z_L(s) = \frac{R + s \cdot L}{s^2 \cdot L \cdot C_p + s \cdot R \cdot C_p + 1} \tag{2.2}$$

For the sake of simplicity the parallel parasitic capacitance of the inductor which is approximately equal to 3 pF is not considered for the modelling. The load inductor is therefore modelled as a series combination of an inductor and resistance. Excluding the capacitance of the inductor is allowable due to it generating a resonance peak in the MHz range and the test bench is operating with a maximum sampling frequency of 40 kHz. The response produced by the parasitic capacitance is therefore far outside the bandwidth of the controller and will not effect the stability of the system. The simplified expression can be seen in (2.3)

$$Z_L(s) = R + s \cdot L \tag{2.3}$$

From the equation above the plant transfer function which is the transfer function of the load current to the duty cycle difference can be expressed as given in (2.4).

$$G_{plant}(s) = \frac{i_L(s)}{\widetilde{D}(s)} = \frac{V_{DC}}{R + s \cdot L} \tag{2.4}$$

When a control is implemented digitally the effect of the delay due to the computation and PWM has to be taken into consideration. The computation delay is the time duration from the sampling instant to the PWM reference update instant and it is half a switching period in the case of double update - when sampling are performed at the beginning and in the middle of a switching period. [27]. The PWM delay is inserted due to the ZOH (zero order hold effect) which keeps the PWM reference constant and it accounts for half sampling period. The s-domain transfer function for the computation delay is expressed in (2.5)

$$G_{delay}(s) = \frac{V_L(s)}{\widetilde{D}(s)} = e^{-s \cdot T_s} \tag{2.5}$$

The PWM delay can be modelled by ZOH. The transfer function for ZOH in s- domain is given in (2.6).

$$G_{zoh}(s) = \frac{1 - e^{-s \cdot T_{smp}}}{s} \tag{2.6}$$

Where, T_{smp} $(1/f_{smp}, f_{smp} = sampling \quad frequency)$ is one sampling period.

The Proportional resonant PR controller with proportional gain K_p and resonance gain K_h in frequency domain is defined as stated in (2.7).

$$G_{PR}(s) = \frac{\widetilde{D}(s)}{i_e(s)} = K_p + \frac{K_h \cdot s}{s^2 + \omega_0^2} \tag{2.7}$$

The PR controller provides an infinite gain for the frequencies ω_0 also called resonance frequency and a gain determined by K_P outside this frequency. The controller can track the ac reference with zero stationary error.

The error obtained by subtracting the measured current form the sinusoidal current reference is fed to the PR controller. The voltage signal is then generated for the CTL module by summation of the DUT duty cycle and PR controller output.

From the block diagram in 2.3 the open loop transfer function or the transfer function of the forward path is given in (2.8).

$$G_{ol} = \frac{i_L(s)}{i_e(s)} = G_{zoh}(s) \cdot G_{PR}(s) \cdot G_{delay}(s) \cdot G_{plant}(s) \tag{2.8}$$

Where, $i_e = i^*_{ref}(s) - i_L(s)$ is the current error.

Now, with the knowledge of the system transfer function in s-domain the system transfer functions can be transformed into z - domain. For the PR controller the discretization strategy used is a Tustin transform with pre-wrapping and is commonly used strategy for

digital implementation of PR controller. [29],[42]. This results in an equivalent discrete time transfer function expressed as given in (2.9)

$$G_c(z) = K_p \cdot \left[1 + \frac{1}{T_r} \cdot \frac{\sin(\omega_0 T_{smp})}{2\omega_0} \cdot \frac{z^2 - 1}{z^2 - 2z\cos(\omega_0 T_{smp}) + 1}\right] \tag{2.9}$$

Where T_r is the resonant time constant and $K_h = \frac{K_p}{T_r}$

The plant transfer function G_{plant} is transferred into z - domain using ZOH, combining the $G_{ZOH}(s)$ and $G_{plant}(s)$ into $G_{plant}(z)$. The resulting transfer function is given in (2.10).

$$G_{plant}(z) = \frac{1}{L} \cdot \frac{z-1}{z} \cdot z \cdot \frac{1 - e^{\frac{-R}{L}T_{smp}}}{(z-1)(z - e^{\frac{-R}{L}T_{smp})}} \tag{2.10}$$

Transfer function for the computation delay G_{delay} can be expressed as (2.11) by modelling it as a ZOH.

$$G_{delay}(z) = z^{-1} \tag{2.11}$$

These transfer functions can be combined to obtain the open loop or forward path transfer function of the system. The open loop transfer function can then be expressed as presented in (2.12).

$$G_{ol}(z) = G_{delay}(z) \cdot G_{PR}(z) \cdot G_{plant}(z) \tag{2.12}$$

This open loop transfer function stability and dynamics will be analysed using control system analysis techniques such as root locus and dynamic response.

The transfer function discretization and root locus analysis is performed using a MATLAB. Figure 2.5 shows the root locus for the system. From the root locus it can be seen that the system is stable and poles of the system remains inside the unit circle until too large gain is applied. The system response to the sinusoidal input with amplitude $10A$ and frequency of $5Hz$ is plotted in Figure 2.6 for the parameters listed in Table 2.1. It can be seen that the input reaches the reference within 0.18 s with almost no overshoot. For laboratory implementation a PR controller for 1 Hz is designed in a similar fashion to enable higher temperature swings during power cycling test.

A bode plot for the designed PR controller is presnted in Figure 2.4. As can be seen from the magnitude plot of the figure that a PR controller provides high gain at the resonance frequency of 5 Hz and almost no or very low gain outside resonance frequency.

Table 2.1. Parameter

Symbol	Value	Unit
L	10.35	mH
C_p	2.8	pF
R	5.6	Ω
T_s	25	μs
K_p	10	–
K_h	500	–

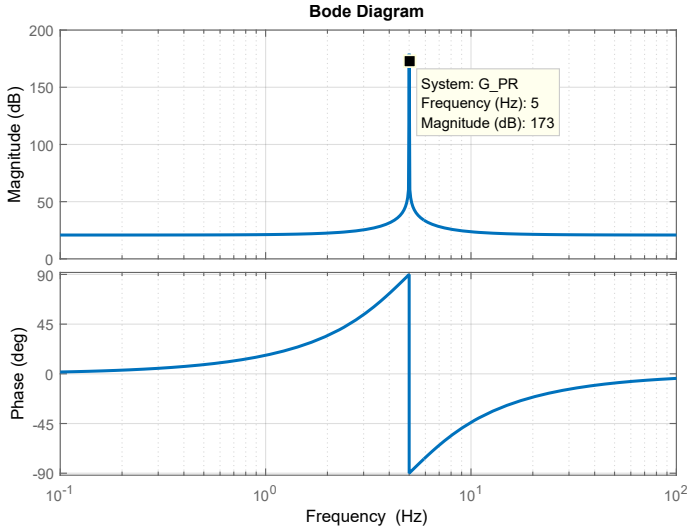


Figure 2.4. Bode plot for PR controller with resonance frequency of 5 Hz

A root locus analysis is performed for the discretized system with system parameters presented in Table 2.1. A root loci presented in Figure 2.5 provides the information on the stability of the system. Data tip in the figure corresponds to the maximum gain of 38.8 after which the system becomes unstable as the poles of the transfer function tends to move outside the unit circle.

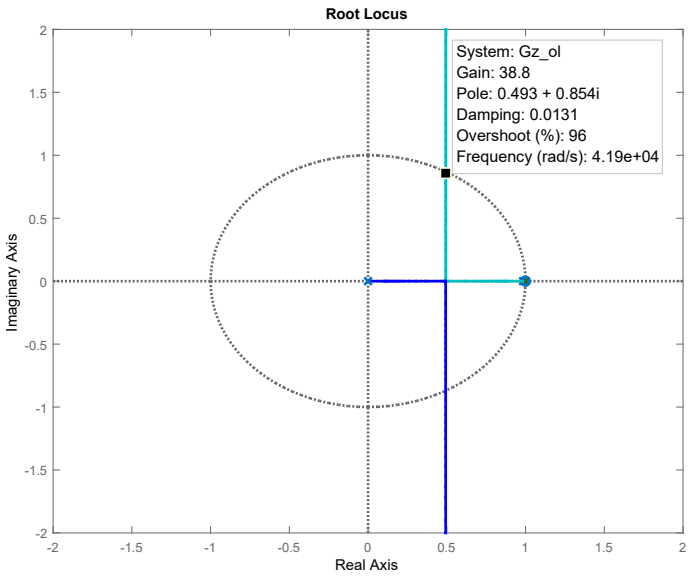


Figure 2.5. Root Locus Analysis

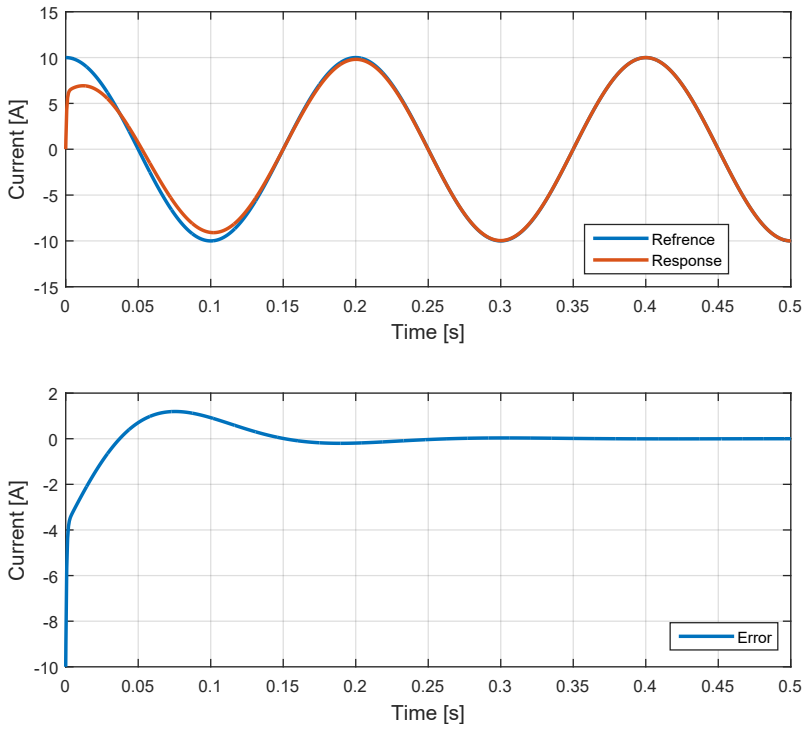


Figure 2.6. System response and error for sinusoidal input of amplitude 10 A and frequency 5 Hz

The implementation of the control for PLECS simulation can be seen in Figure 2.7. [2]

[2] \PLECS\power_cycling_discrete.plecs

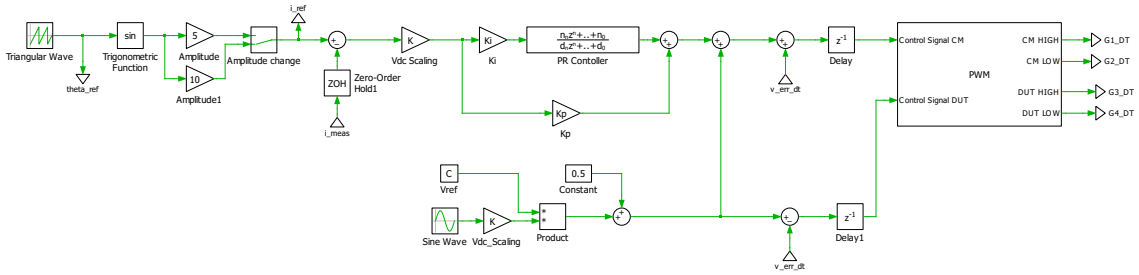


Figure 2.7. Discretized control system for the PLECS simulation

The simulated load and reference current for the PLECS simulation are depicted in Figure 2.8. As can be seen in the figure the simulated load current follows the reference with no error and reaches reference at 0.18 s which corresponds to the verification performed for a system response to the sinusoidal waveform in Figure 2.6. To test the robustness of the system a step change is applied at time $t = 0.82s$. As can be seen in the case of amplitude change the measured current catches the reference and no overshoot in the current is present.

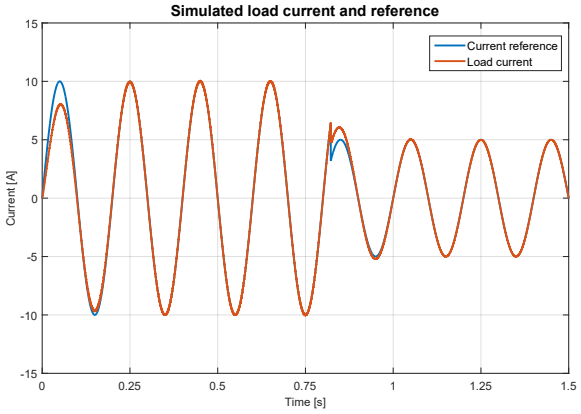


Figure 2.8. PLECS Simulation Results for simulated reference and load current.

2.4 Deadtime Voltage Error Compensation

In practice, finite turn on/off times associated with the power semiconductor switch can cause a shoot through of DC - link due to cross conduction. To prevent the shoot through of the DC link due to conduction overlap, finite amount of time delay generally referred to as deadtime or blanking time is inserted between the gate signals of a High Side and Low Side switches of an inverter leg. This inserted deadtime causes distortion of the output voltage for an inverter. Required deadtime is determined based on the rise and fall time of the switching device.

There are several other factors which causes the distortion in the standard PWM inverter output voltage such as: finite turn on/off time and on state voltage drop of power semiconductor switches, snubber/parallel parasitic capacitance. Amongst these, the voltage error introduced due to the deadtime corresponds to a major portion of the total voltage error.

For sake of simplicity, the effect of deadtime on output voltage waveform is presented in this text considering one leg of a standard two level inverter. This analysis holds true for the remaining legs of an inverter circuit. The gate signals and output voltage waveform during a switching period for the ideal case without deadtime and one with deadtime are presented in Figure 2.9.

How this voltage error is introduced due to the deadtime is presented in the text below. The analysis of voltage error is based on the switching states and current direction presented in Figure 2.10
First the case when current is positive (i>0) meaning that current is flowing outward of the inverter leg considered.

- **Case I: i > 0 & HS switch turns off**
  In the first case, it is considered that the high side (HS) switch changes its state form ON to OFF and low side (LS) from OFF to ON. During deadtime both HS and LS switches are off and current will conduct through LS diode due to the direction of the current flow. This causes the output voltage of the leg V_{AO} to clamp at the negative DC-link voltage, which is similar to the ideal case. This indicates that there is no voltage error present during this instant.
- **Case II: i > 0 & HS switch turns on**
  In the second case, it is considered that the HS switch changes its state form OFF to ON and LS switch form ON to OFF. During deadtime both HS and LS switches are off and current will conduct through LS diode due to the direction of the current flow. This causes the output voltage of the leg V_{AO} to clamp at the negative DC-link voltage, which would have been V_{dc} in ideal case. This indicates that there is negative voltage error during this time period.

Now, the case when current is negative (i<0) i.e current is flowing inward of the inverter leg is considered.

- **Case III: i < 0 & HS switch turns off**
  In the third case, it is considered that the HS switch changes its state form ON to

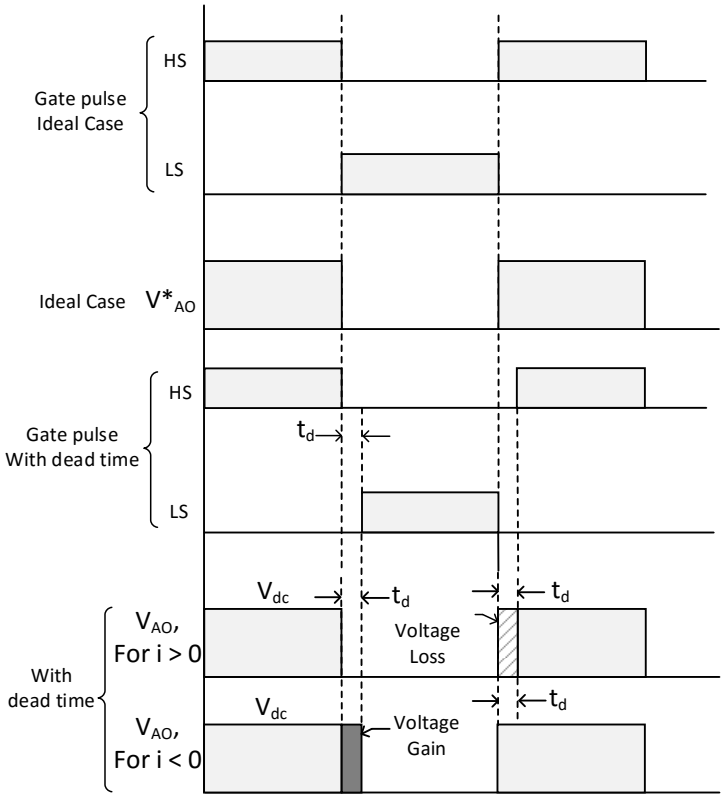


Figure 2.9. Effect of deadtime on gate signals and output voltages

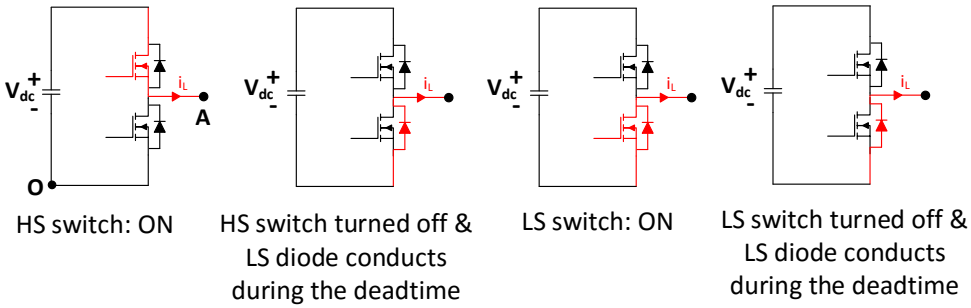


Figure 2.10. Switching sequence for one leg of an inverter

OFF and LS switch form OFF to ON. During deadtime both HS and LS switches are off and current will conduct through HS diode due to the direction of the current flow. This causes the output voltage of the leg V_{AO} to clamp at the positive DC-link voltage, which would have been clamped to negative DC link in the ideal case. This indicates that there is a positive voltage error at this instant.

- **Case IV: i $<$ 0 & HS switch turns on**
  In the last case, it is considered that the HS switch changes its state form OFF to ON and LS switch form ON to OFF. During deadtime both HS and LS switches are off and current will conduct through HS diode due to the direction of the current flow. This causes the output voltage of the leg V_{AO} to clamp at the positive DC-link

voltage, which is similar to the ideal case indicating no voltage error is present.

The polarity of the voltage error due to deadtime is dependant on the direction of the current, DC - link voltage and inserted deadtime. The voltage error introduced by deadtime can be expressed by the equation presented in (2.13).

$$V_{error} = (V_{AO})_{ideal} - (V_{AO})_{actual} \tag{2.13}$$

By averaging voltage error over one switching period, the change in output voltage based on the direction of the current can be obtained and is expressed in the equations presented in (2.14).

$$\Delta V_{AO} = \begin{cases} +\frac{V_{dc} \cdot t_d}{T_{sw}}, & \text{for } i > 0 \\ -\frac{V_{dc} \cdot t_d}{T_{sw}}, & \text{for } i < 0 \end{cases} \tag{2.14}$$

Where, V_{dc} = DC - link voltage, t_d = deadtime, $T_{sw} = 1/f_{sw}$ = switching period.

Applying similar analysis to the remaining leg of a single phase full bridge inverter of Figure 2.10. Recognizing that the direction of the current in the opposite leg is reversed compared to previous. The voltage error for the opposite leg is given in (2.15).

$$\Delta V_{BO} = \begin{cases} -\frac{V_{dc} \cdot t_d}{T_{sw}}, & \text{for } i > 0 \\ +\frac{V_{dc} \cdot t_d}{T_{sw}}, & \text{for } i < 0 \end{cases} \tag{2.15}$$

In order to compensate for the voltage error introduced by the deadtime, based on equation estimated voltage error is added to the control signal of each leg. Simulation results for the full bridge inverter is shown in Figure 2.11 and 2.12 with and without deadtime compensation. The simulation is performed with DC link voltage $V_{dc} = 5000$, switching frquency $f_{sw} = 20$ kHz and deadtime of 1 μs. It can be seen that, without deadtime compensation the output voltage is distorted due to the inserted voltage error. It should be noted that the deadtime voltage error is proportional to the DC link voltage and as the DC link voltage used for the simulation is 5 kV the voltage error due to inserted deadtime and distortion in current and voltage waveforms pronounced. However, when deadtime compensation is implemented the current follows the reference with no voltage error due to deadtime being compensated.

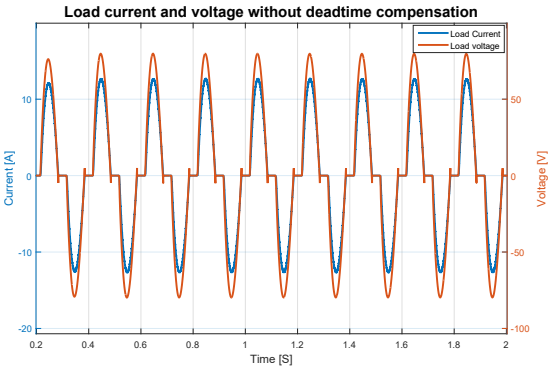


Figure 2.11. Simulated Load voltage and current - Without deadtime compensation

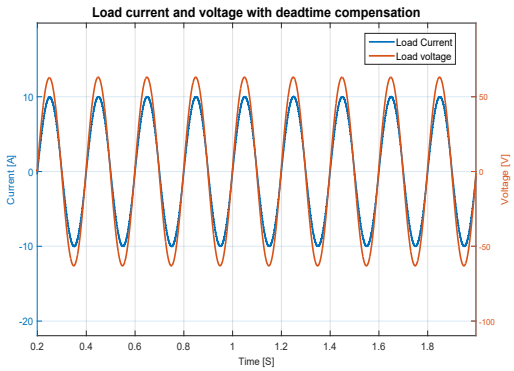


Figure 2.12. Simulated Load voltage and current With deadtime compensation

2.5 Conduction voltage measurement technique

There are several measurement techniques available for device conduction voltage measurements and can be broadly classified into two categories: (i) online (ii) offline measurement. [14]

For this project a reed relay based offline measurement technique [4] is utilized and therefore online measurement techniques are not presented in this report. A conduction voltage measurement circuit should fulfil the basic requirements. One of which is the isolation of the measurement circuit to protect the ADC from the high voltages when the power device MOSFET/diode is in blocking stage. The reed relay used for the measurement circuit offers a 10 kV isolation which is in the range of the maximum blocking voltage of the device whose conduction voltage are going to be measured. Isolation requirement for the measurement circuit can also be fulfilled using solid state devices. However the measurement circuit based on the reed relay is simple to implement and economical compared to the circuit utilizing a solid state device. Moreover the solid state device based solution will require calibration as the electrical parameters of the device are dependent on several other factors.

On the other hand the relay based solution also has limitations. The operate/release time of reed relay is 3 ms. For the converter switching at 20 kHz the online measurement can not be performed using reed relays due to their slow reaction time. For this reason they are not suitable for conduction voltage monitoring in an online measurement routine. Also for the offline measurement converter PWM switching operation needs to be halted. Therefore, in the offline measurements the device junction temperature are lower compared to online operation. Although for the laboratory Accelerated Life Testing and monitoring the conduction voltage measurement as a state of health monitoring, an offline reed relay based technique is a suitable choice. In this section a brief description about the measurement routine will be presented. For this project, the V_{ds-on} and diode V_f measurements are performed for monitoring the level of degradation for the Silicon Carbide modules. The measurements are expected to be crucial for detecting the state of health of the module since several failure mechanisms advancements should be observable using the conduction voltage as was documented in Section 1.1.1. The measurements are conducted offline

using the schematic introduced in Section 2.1.

After a predetermined number of thermal cycles are conducted, the power cycle operation is halted and the offline measurement routines will be initiated. The objectives are to measure the on state V_{ds} of the MOSFETs and forward voltage drop V_f for the intrinsic/external diodes respectively. Before the measuring routines are initiated the PWM signals from the DSP are disabled and PWM ports on the DSP are configured to function as output ports to control the gate signals individually for the measuring routines. After the measuring routines are performed the PWM ports are re enabled and the converter resumes its power cycle operation.

The measurement routine consists of four different states. During each state, three of the eight switching sequence [(a) - (h)] are initiated and one V_{ds-on} and V_f measurement are acquired. The measurement routines are shown in Figure 2.13.

The way in which each switching sequence are executed and measurements acquired during the corresponding state are presented in 2.2. A load current profile during the measuring routine is depicted in Figure 2.14.

Table 2.2. Measuring routine switching sequence (a)-(h) for V_{ds-on} and V_f monitoring

Device	Sequence
CTL H MOSFET & DUT H Diode	(a),(b),(c)
DUT H MOSFET & CTL H Diode	(e),(f),(g)
DUT L MOSFET & CTL L Diode	(a),(d),(c)
CTL L MOSFET & DUT L Diode	(e),(h),(g)

In the text below theory for one out of four sequences is explained as the later ones are comparable to the one presented below.

2.5.1 Measurement routine

As discussed before, each measurement routine consist of a three switching states during which one V_{ds-on} and V_f measurements are acquired. The first sequence is initiated by turning on CTL high side MOSFET and DUT low side MOSFET. During this state the current will be ramped up through the load inductor as shown in 2.13 -(a). The time period to ramp up is determined based on the desired peak current magnitude at the end of ramp up period. The time period is calculated using (2.16).

$$t_{ramp-up} = L_{load} \cdot \frac{di}{V_{dc}} \tag{2.16}$$

Where, L_{load} = Load inductance, V_{dc} = DC link voltage, di = i_{pk} - i_0, $t_{ramp-up}$ = ramp up time duration

After the ramp up period, DUT LS MOSFET is turned off and the load current free-wheels through CTL HS MOSFET and DUT high side diode. During this state the measurement relays are turned on to perform the measurements of V_{ds-on} for CTL HS MOSFET and (V_f) of DUT HS diode as shown in 2.13 - (b). A time delay of 3 ms before the relays

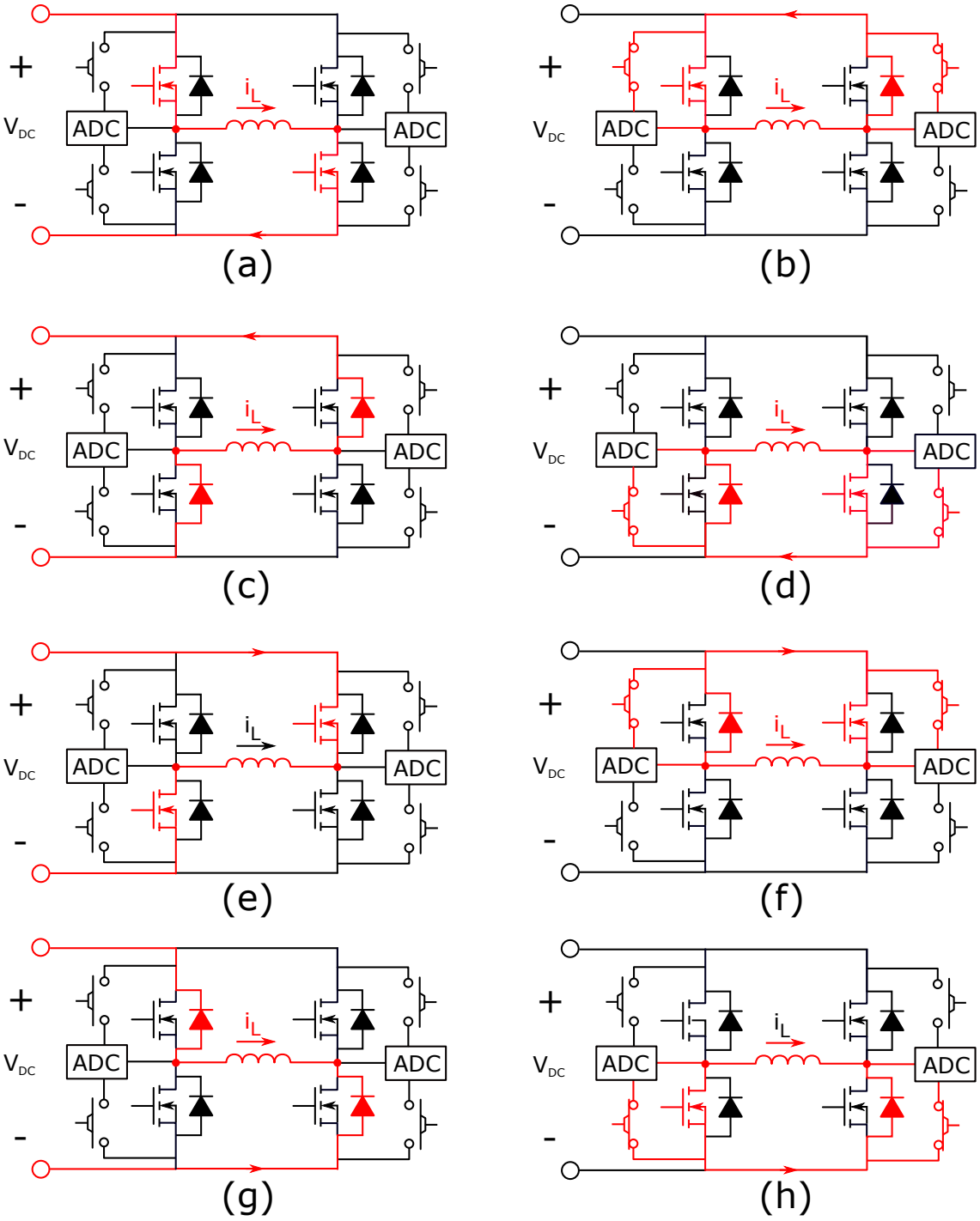


Figure 2.13. Measurement routine switching sequences (a) - (h)

are conducting is present after which the start of conversion for the ADC will be initiated as depicted in Figure 2.14. The time delay is present due to the relative large turn on time for the read relays before they are fully conducting. ADC acquires a fast series of 20 samples during the free-wheeling period and an average value of the samples is stored in a buffer. After, the series of samples are acquired the relay is disconnected and CTL HS MOSFET is turned off as shown in 2.13 - (c). During the last state, the load inductor will be demagnetized resulting in the current reaching a value of zero at the end of this

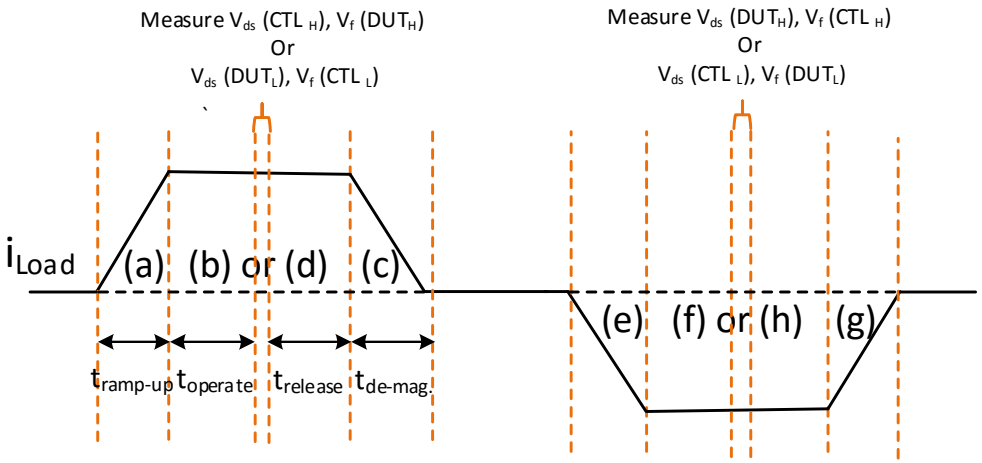


Figure 2.14. Load Current profile during a measurement routine

period.

Similarly, three other measurements are executed to acquire conduction voltages on the remaining MOSFETs and diodes in an H-bridge converter.

2.6 Conduction voltage and load current measurement circuit

The analog to digital conversion of a measured voltage signal is required for two cases. Firstly, a load current needs to be measured and converted into the digital domain in order to provide a feedback for the digital current control loop. Secondly, the V_{ds} and V_f data for the devices in the setup are sampled and stored for condition monitoring.

The analog to digital conversion are performed using 14 - bit AD7367 ADC. AD7367 is a dual channel ADC and can be configured to accept bipolar voltages of ± 5 V, ± 10 V. A 14 - bit ADC provides resolution of 2^{14} = 16,384. So, this can ideally resolve voltage difference as small as 0.61 mV and 1.22 mV for bipolar input voltages of ±5 V and ± 10 V respectively 2.17. LSB size for a 14- bit ADC is given by,

$$\text{LSB size (mV)} = \frac{\text{Input range}}{2^{14}} \tag{2.17}$$

Input range = 10 V, 20 V for input voltages of ± 5 V and ± 10 V respectively.

Transfer characteristics for AD7367 is depicted in Figure 2.15 below.

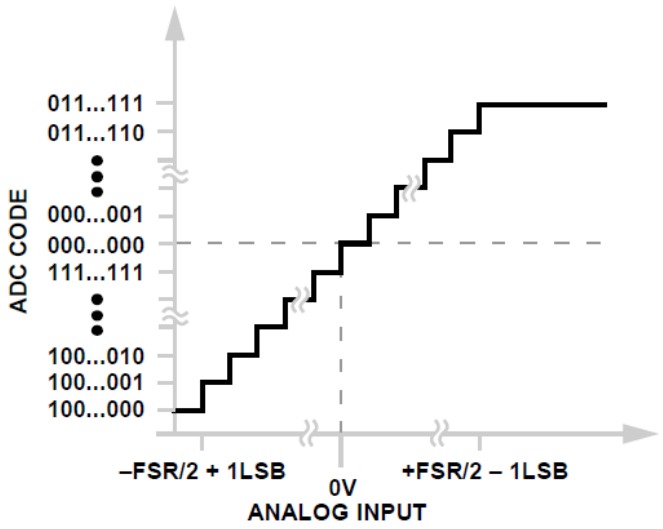


Figure 2.15. Transfer characteristics for AD7367 [11]

2.6.1 Load current measurement

A load current measurement is performed using current transducer LEM LA 55-P. This current transducer has a measuring range of ±70 A and a conversion ratio K_n of 1:1000. The output current from current transducer is sensed by measuring the voltage across a measuring resistance. The voltage is supplied to the analog input pin of AD7367. Analog to digital conversion is initiated by providing a $\overline{CS}$ (conversion start) signal to AD7367. $\overline{CS}$ is an active low signal meaning that the conversion is initiated at the falling edge of $\overline{CS}$. A conversion time of 680 ns for the AD7367 is needed after which the data is available to read. The 14 clock cycles needed for transmitting the 14 bits are provide by the DSP to SCLK pin of the ADC. the data is read serially on the respective DOUT (digital output) pin of the ADC. The sampled data is then scaled in the DSP to obtain actual value as shown in 2.18.

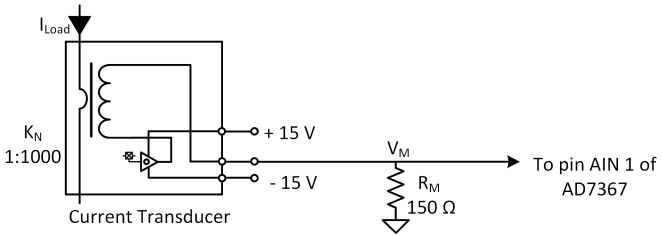


Figure 2.16. Load current measurement

$$\text{Measured load current} = \frac{\text{ADC Data}}{R_m \cdot K_n \cdot N_p} \cdot (\text{ LSBsize}) \tag{2.18}$$

V_m = voltage across measuring resistance, R_m = measuring resistance K_n = Current transducer conversion ratio, N_p = Number of turns in primary

Figure 2.17. Measured $\overline{CS}$ and SYSCLK signal

2.6.2 Conduction voltage measurement

For the V_{ds-on} and V_f monitoring circuit, conduction voltage for the high side device is measured on one analog input channel and similarly the voltages for low side device is measured on the remaining analog input channel. This allows sampling of data using a single dual channel ADC for the half bridge module. To initiate the conversion on ADC similar procedure as explained in previous text is performed. But in this case the data for both analog input channels are read serially on a single digital output pin by providing 28 pulses on SCLK pin of AD7367. This allows to transmit the data from the gate driver board to DSP on a common optical transmitter. Once the data is read from the ADC it is scaled in the DSP to obtain actual value as shown in 2.19.

$$\text{Measured conduction voltage} = \text{ ADC Data} \cdot \text{LSB size} \tag{2.19}$$

Chapter 3

Experimental Setup

A setup capable of power cycling Silicon Carbide modules at medium voltages and rated current is not available, one should therefore be built. A power cycling testbench includes a protection circuit ensuring discharge of DC-link capacitor for human safety, isolation between testbench and operator, gate driver with conduction voltage measurement circuit, power modules, busbar and load inductor. All parts presented are crucial for the functionality and protection of testbench and personal. An overall principal diagram is presented in Figure 3.1.

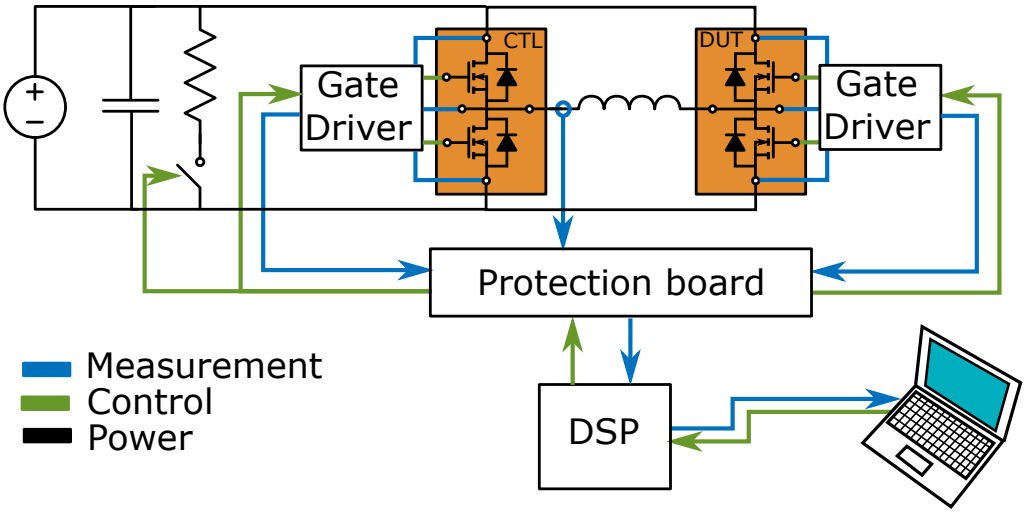
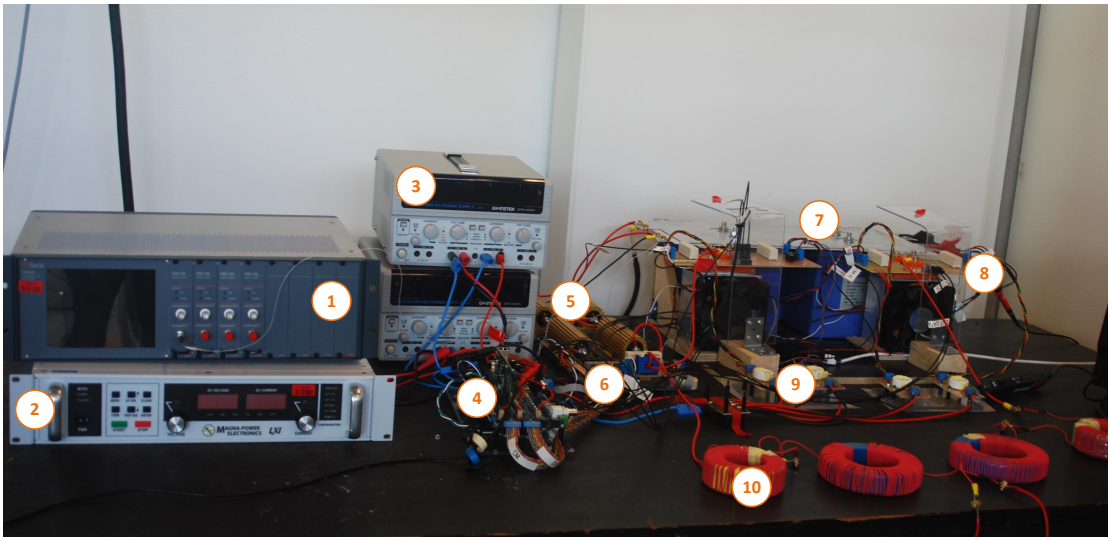


Figure 3.1. Power cycle testbench with signal overview.

Communication to the testbench is performed using a laptop to control the voltage source with an ethernet and the DSP using USB connection. A program in the laptop called LabVIEW is controlling the power cycling and displaying the measured results. The protection board provides control of the bleeding resistor for capacitor discharge, over current protection and isolation of the PWM signals from the DSP. The Gate driver boards are designed to perform offline measurement of the on-state voltage across MOSFETs and diodes which are sent to the laptop through the DSP.

A picture of the physical testbench with the load inductor can be seen in Figure3.2.

The following sections will briefly present the crucial parts of the test bench and its main objectives. The parts developed during the project will include a reference to the Appendix covering circuit schematics of the PCB layouts.

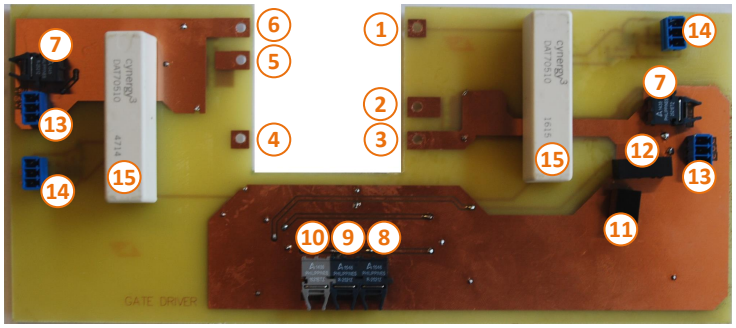


1. Signal Conditioner for fiber optic temperature measurement
2. 6 kW Power Supply for DC - Link
3. Laboratory power supply
4. DSP interface board
5. Bleeding resistor
6. Protection board
7. Busbar assembly & DC-Link capacitor
8. Gate driver PCB mounted on power module
9. Isolated DC/DC power supply for gate driver
10. Ferrite core load inductor

Figure 3.2. Picture of power cycling test bench.

3.1 Gate Driver

A gate driver is needed for driving the SiC MOSFETs Half bridge modules and to measure the drain-source and forward voltage during conduction. A PCB is therefore designed and developed as can be seen in Figure 3.3 and Figure 3.4.



1. Pad - HS Drain
2. Pad - HS Gate
3. Pad - HS Source
4. Pad - LS Drain
5. Pad - LS Gate
6. Pad - LS Source
7. Optic Receiver for Gate Signal
8. Optic Receiver for ADC SYSCLK
9. Optic Receiver for ADC CONVST
10. Optic Transmitter for ADC DATA
11. DC – DC power supply +5 V
12. DC - DC isolated power supply +/- 12 V
13. Supply voltage gate driver +19 V/-4.5 V
14. +5 V supply & relay control signal
15. 10 kV isolated reed relay (NO type)

Figure 3.3. Gate driver with V_{ds-on} and V_f measurement circuit.(Top view)

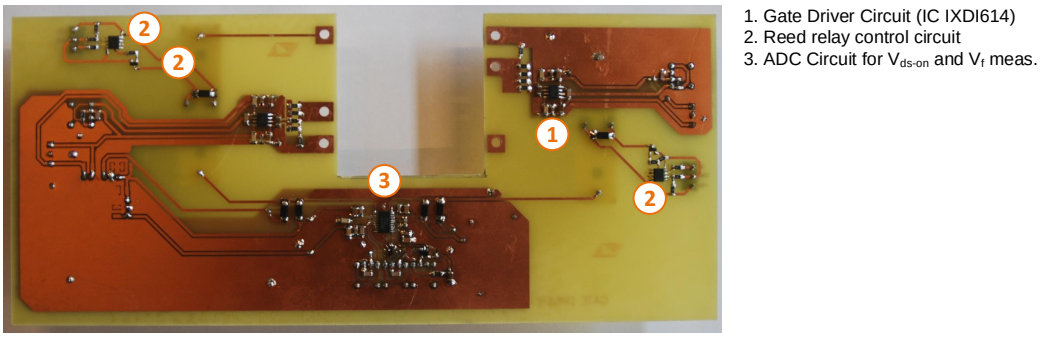


Figure 3.4. Gate driver with V_{ds-on} and V_f measurement circuit. (Bottom view)

The white blocks seen in Figure 3.3 are 10 kV isolated NO (Normally Off type) relays. The relay are used to connect the ADC during the measurement routine for acquiring the conduction voltages. The relays are slow and has a coil operate and release time of 3 ms. The measurement are initiated and transferred using optic transmitters and receivers to obtain isolation between power and control circuit.

The Gate driver circuit is designed to be compact and positioned near the gate-source terminals to ensure low switching loop inductance. A gate resistance of $R_g = 12\ \Omega$ is chosen. The positive and negative bias voltages used to drive the MOSFETs are determined by the output voltage a of isolated DC/DC converter. A more detailed description of the Gate driver circuit can be found in Appendix C.

The DC/DC converters utilizes a Flyback topology. One of the important criteria for the galvanic isolated converted is a very low coupling capacitance since high dv/dt is present during operation. The isolation capacitance achieved for the Flyback transformers are within the range of $4 - 5$ pF. The output voltages of the Flyback is 19V and -4.5 V compared to its common point. The designed isolated DC/DC converter can be seen in Figure 3.5

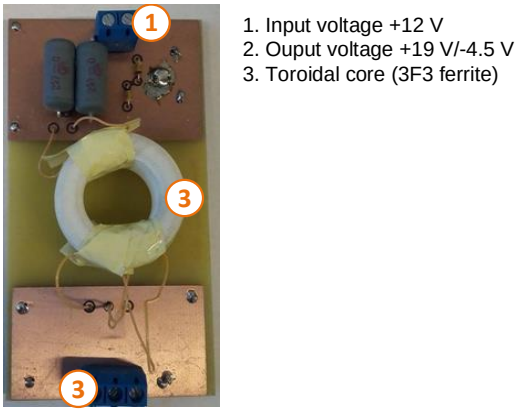


Figure 3.5. Isolated power supply for gate driver - Flyback converter with low coupling capacitance.

Some of the important parameters and values for the Gate driver circuit is collected in

Table 3.1. The values presented provides important information about the expected on-state resistance, ADC resolution and common mode current rejection.

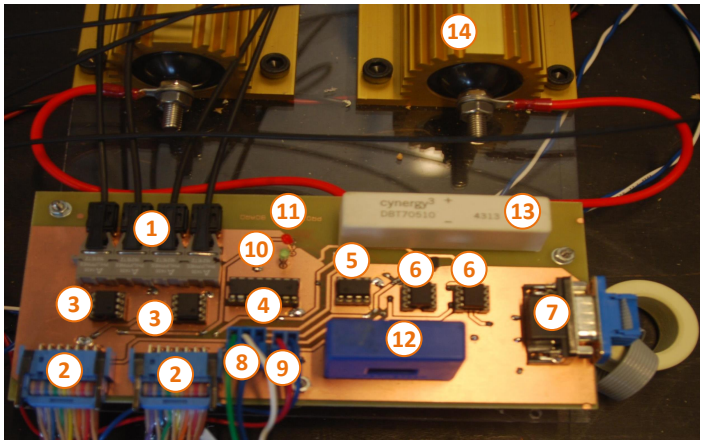
Table 3.1. Selected properties for gate driver circuit

Parameter	**Value**
High potential V_h	19 V
Low potential V_l	-4.5 V
Gate Resistance R_G	12 Ω
Inter winding Capacitance C_W	4-5 pF
Operate time $t_{operate}$	3 ms
ADC Resolution	1.22 mV

From Table 3.1 the gate-source high potential can be identified to be at 19 V which is below the rating of 20 V and above 14 V ensuring low R_{ds-on}. The isolation capacitance is at max 5 pF ensuring good rejection of common mode currents. The least significant bit of the ADC represent an increment of 1.22 mV, concluding digits of less than a mV being a misleading representation of accuracy. The results of conduction voltages are therefore transferred with four digits, equivalent to an accuracy of 1 mV. The next section will present the protection board and main purpose of it is to protect the testbench and operating personal.

3.2 Protection

The main purposes of the protection board are to deactivate the PWM signal and discharge the DC link capacitor when a fault occurs or the cage to the testbench is open. A picture of the protection board can be seen in Figure 3.6.



1. Optic Transmitter for Gate Signals
2. Gate Signals DSP → Protection Board
3. Voltage comparator
4. S – R Latch
5. Logic Gate AND
6. Logic Gate NAND
7. Supply voltage for LEM & Current Measurement: DSP → Protection Board
8. Supply Voltage +5 V
9. Enable, Reset & Relay discharge signal
10. LED Indicator (green) Enable
11. LED Indicator (red) Fault
12. LEM current transducer (LA 55 P)
13. 10 kV isolated relay (NC type)
14. Bleeding resistor

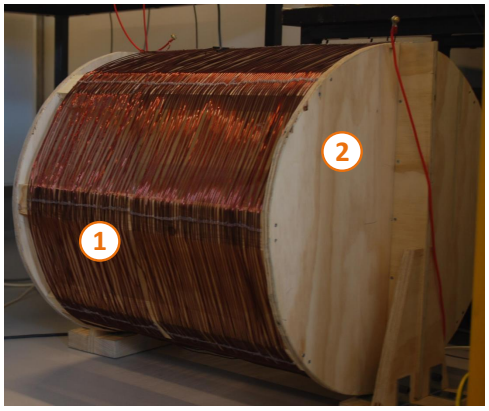
Figure 3.6. Protection board with over current protection and capacitor discharge relay.

The protection board are converting four electrical PWM signals to optic signal for obtaining isolation. The PWM signals are enabled utilizing a logic circuit providing external deactivation and over/under current protection. A discharge relay for the bleed resistors is present on the protection board providing external control of discharge but also ensures the discharge of the DC link capacitor if no voltage supply is present, which

is the case when the cage door is open. These features for the protection board are crucial for personal safety but also for protecting the devices if an unexpected failure causing high currents occur.

3.3 Inductor

The load inductor used for power cycling has a low parasitic capacitance and consist of high frequency materials such as ferrite or air. The low parasitic capacitance of the inductor is desired to minimize the inrush current during switching transients. The Air coil build for the project can be seen in Figure 3.7.



1. Windings – 0.75 mm copper wire mm (coil dia 600 mm, length 500 mm)
2. Wooden coil former

Figure 3.7. Air Core Inductor.

The inductance of the coil is proportional to the turns squared and its cross sectional area, whereas it is inversely proportional to the magnetic path length of the coil. Based on this, a solenoid air coil having a large cross sectional area and small coil length was the criteria to achieve higher inductance. The solenoid air coil is wound on a wooden coil former which has a length of 500 mm and diameter of 600 mm. A number of 137 turns were achieved resulting in an expected inductance of 8.6 mH using Wheeler's approximation for a solenoid air coil given in 3.1.[43]

$$L(\mu H) = \frac{1}{25.4} \cdot \frac{r^2 \cdot N^2}{(9 \cdot r + 10 \cdot l)} \tag{3.1}$$

Where, l = length of the coil in mm, r = radius of the coil in mm, N = Number of turns

The inductance, series resistance and parasitic capacitance values obtained for the solenoid air coil and ferrite inductor are presented in Table 3.2. The values are obtained using an impedance analyser to measure the frequency response at which an equivalent circuit is fitted to. Measured impedance response for ferrite core and air coil inductor can be seen in Figure 3.8 and Figure 3.9.

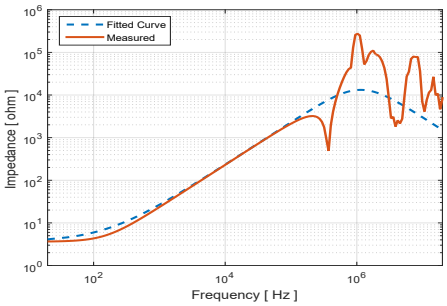


Figure 3.8. Impedance response ferrite core inductor

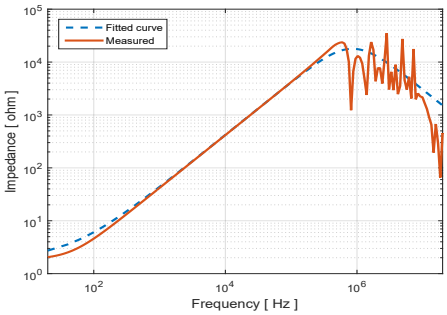


Figure 3.9. Impedance response of an air coil

Table 3.2. Table with values for Air coil and Ferrite inductor

Parameter	Air coil	Ferrite inductor
Inductance	6.66 mH	3.69 mH
Resistance	1.89 Ω	3.66 Ω
Capacitance	5.24 pF	6.13 pF

3.4 LabVIEW Interface

Main purpose of creating a LabVIEW interface is to facilitate user with an ease of test bench operation and real time monitoring of the measurement data. The front panel view of LabVIEW interface is shown in Figure 3.10. As can be seen in Figure 3.10, the LabVIEW interface front panel includes user specified inputs/control and graphical display/indicator. The user control includes 'DC - Link On', 'Test On', 'Stop' and 'Reset' buttons. The user inputs available from the front panel is power supply voltage selection, file path selection, selection for USB and Ethernet based serial communication.

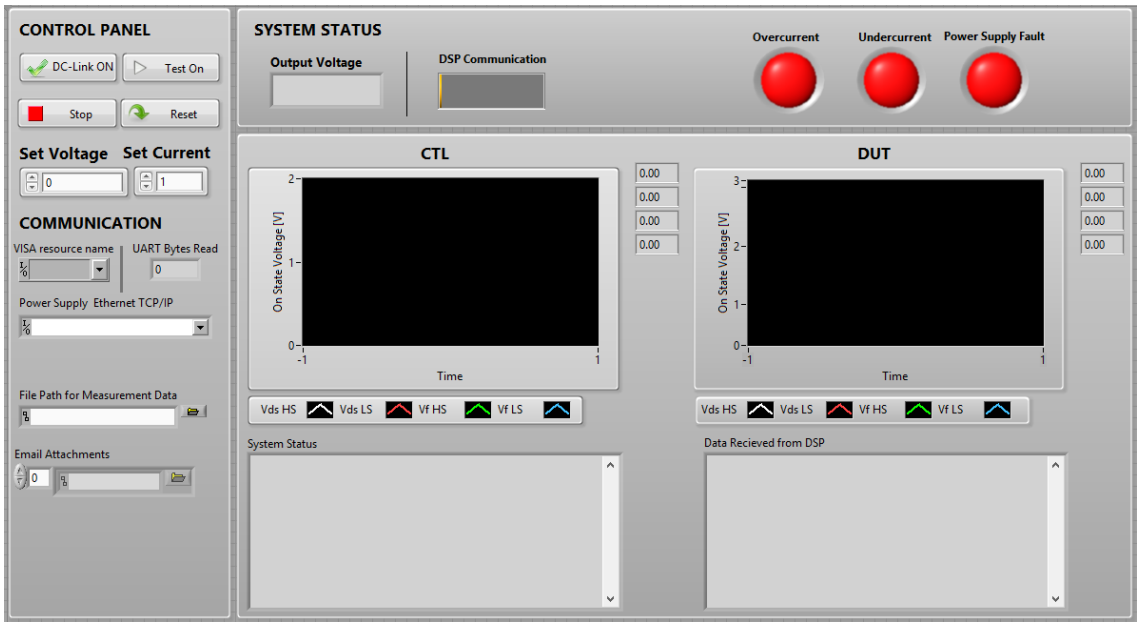


Figure 3.10. Image of the LabVIEW interface front panel

The interface front panel displays the status of the system by means of LED indicators such as Over current, Under current and Power Supply fault. Moreover, the sampled data for MOSFET V_{ds-on} and diode V_f are displayed on the waveform chart for both DUT and CTL module. The display window below shows the data transmitted to the DSP based on the user command provide from LabVIEW interface and also the data received from the LabVIEW interface.

The basic structure of the LabVIEW programming is presented in Figure 3.11 in the form of a flowchart. Once the LabVIEW program is running it continuously checks for the user inputs from the front panel and any data received from the DSP. Whenever the program is initiated for the first time the DC Link On and Stop are initialised to logic false. Function of each of these user control/input and graphical display/indicator on LabVIEW front panel is presented in the text below.

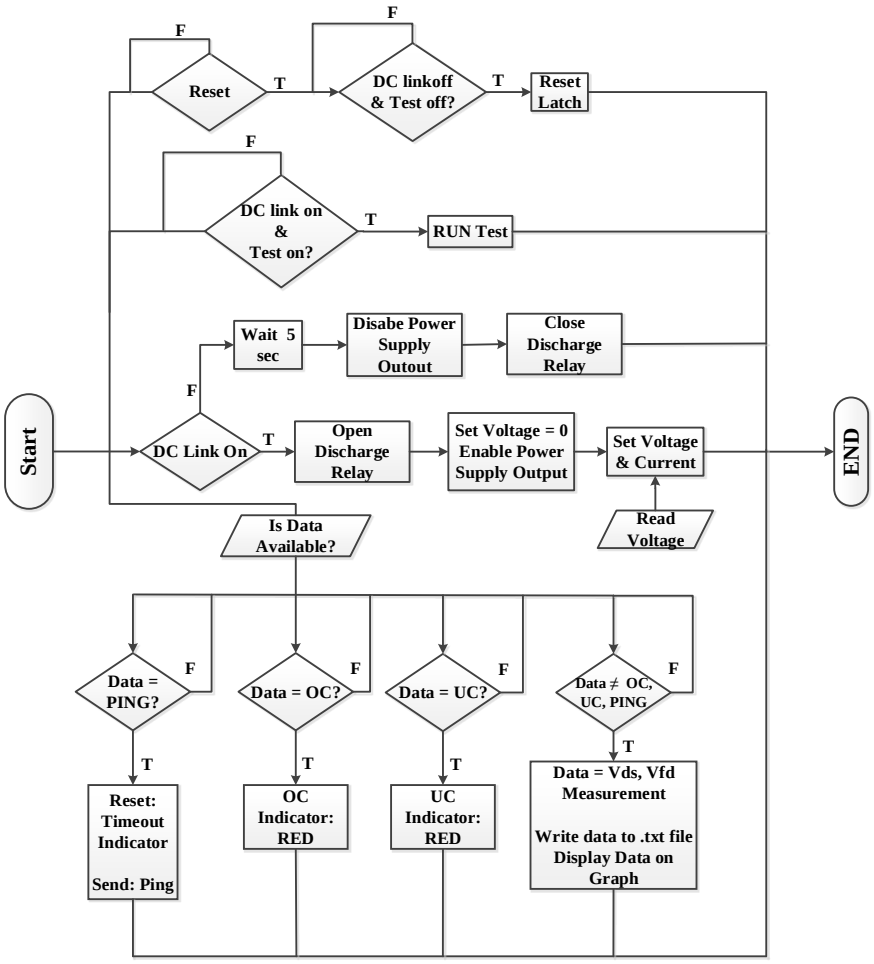


Figure 3.11. Flowchart of LabVIEW programming

Communication between the Power Supply and DSP uses the USB and Ethernet communication protocol respectively. The basic communication and data exchange between the user interface, DSP and Power Supply is depicted in Figure 3.12

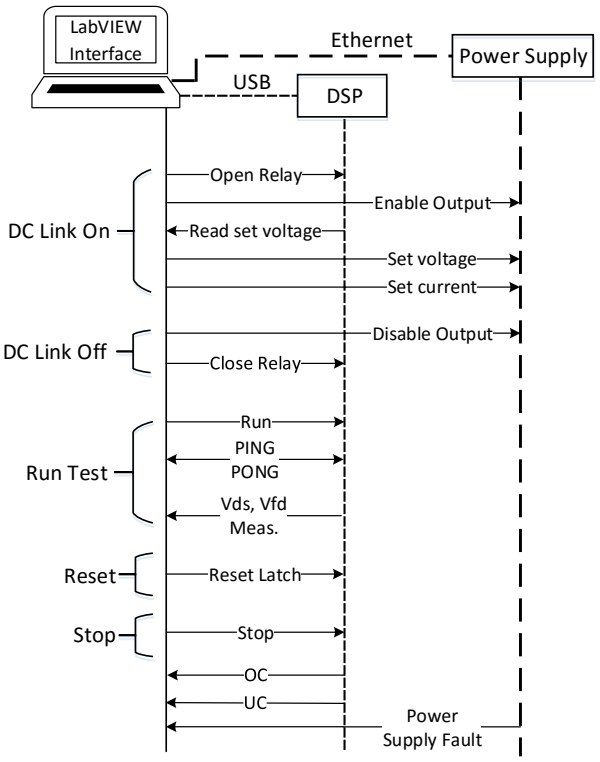


Figure 3.12. Communication and data exchange between LabVIEW - PowerSupply & DSP

Note: DC link ON, Test ON and Stop buttons, when pressed the state of the button is changed and remains there until pressed again. Whereas, the RESET button state is latched when released.

User Input & Controls

- **DC - Link On:** Upon pressing the DC - Link On a message 'OPENRELAY' is sent to DSP in the form of string to open the discharge relay. Once the data is received on the DSP, an output port which controls turn on and off of relay is set to high in order to open the discharge relay. Once the message has been sent and relay is Open, DC power supply output is enabled with a set voltage of zero. The instant after the power supply is enabled the voltage is raised upto the voltage level set by the user in Set Voltage input on LabVIEW interface.

  On the other hand when DC - Link On is turned off, power supply output is disabled. Once power supply output is disabled, message 'CLOSERELAY' is sent to DSP in the form of a string after a delay of 5 seconds. Upon receiving the string CLOSERELAY, an ouput port which controls the turn on/off of relay is set to logic level low in order to close the relay. The DC link capacitor is de-energized through bleeding resistor.
- **Test On** The power cycle test can be initiated by pressing the Test On button on the front panel. If the DC Link is turned on and Test On button is pressed, LabVIEW will send a message 'RUN' to the DSP to run the Power Cycling test.

Power cycling will be halted when Test On is pressed again. This is performed by sending a string 'STOP' to the DSP from LabVIEW.

- **Stop** On pressing the Stop button, LabVIEW program will be closed and exit from the main loop. Pressing Stop will only have effect when the DC link is not energized and power supply is turned off.
- **Reset** Upon pressing the reset button, message RESETLATCH will be sent to DSP in the form of string. This will make the output port connected to S-R latch go low and set to high again, clearing the over or under current fault. Pressing Reset will have no action unless the test is at halt, DC link is de energized and power supply is turned off.
- **Set Voltage** LabVIEW continuously checks for the Set Voltage input from the user, so that voltage can be controlled by user at any point of time. Also, the voltage can be increased in steps when initially energizing the DC link to desired voltage level.
- **USB COM Port** Using this dropdown menu, user can specify the USB communication port of the PC/Laptop which is running the LabVIEW interface. This is required to establish communication between the LabVIEW and DSP.
- **Power Supply TCP/IP Adress** Using this dropdown menu the user can specify the TCP/IP adress of the Power Supply. This is necessary to establish ethernet communication between the LabVIEW interface and Power Supply.
- **File Path** The user interface is configured to save the measurement data to a .txt file and send the measurement data via an email in the form of attachment. The file path for the text file and email attachment can be selected form the drop down list menu on the front panel. Email and server settings can be configured according to the user requirement in the block diagram.

Graphical Display & Indicators

- **DC - Link Voltage** It displays the instantaneous value of the voltage being measured on the power supply.
- **DSP Communication** When the power cycling test is turned on, the DSP sends a string 'PING' to the LabVIEW. When the string of data 'PING' is received on the LabVIEW, message 'PONG' is sent to DSP again. This series of sequence is performed at every 30 seconds. If DSP fails to receive a 'PONG' command from the LabVIEW interface within 90 seconds the Power Cycling test will be halted. The time bar on the user interface front panel will reset every time the 'PONG' is received which displays the status of USB communication between the LabVIEW and DSP.
- **Overcurrent and Undercurrent** The OC and UC trip signlas from protection board are sent to input ports of the DSP. It continuously monitors the logic level on these ports. Whenever the OC or UC trip occurs it sends the string of data 'OC' or 'UC' to LabVIEW. Which is then displayed by turning on the Over current LED indicator to red. Similar technique is performed for the Under Current fault.
- **Power Supply fault** Power Supply fault indicator will turn to red, if power supply voltage deviates within ± 10 % of the set voltage.
- **Waveform Chart CTL & DUT** The conduction voltages for CTL and DUT module are displayed on the waveform chart of the front screen. The column on the right hand side of the chart displays the latest measurement of the conduction

voltages. Whenever the measurement routine is initiated the sampled data during the measurement routine is sent to the LabVIEW in the form of sting of data. These data includes time at which measurement is performed, current magnitude at which the measurement was conducted, the on state drain -source voltage and diode forward voltage for CTL and DUT.

- **Text Window** The data exchanged between the LabVIEW and DSP during the test or action initiated on Front Panel by the user are displayed in the form of text.

3.5 Summary

Test bench overview along with a brief description about the gate driver design, power circuit protection, isolated DC DC supply, load inductor design was presented in this chapter. A labview interface and its functionality is discussed. Once the setup is built a verification of the testbech is required to ensure the functionality of the setup. This verification includes the test of gate driver circuit, measurement circuit, current controller and communication with LabVIEW interface and DC - link power supply.

Chapter 4

Experimental Validation

After the design phase, verification of the test bench is performed. First, the gate driver circuit and conduction voltage measurement circuit is tested. Calculation and verification of the deadtime between the high side and low side gate signals of a half bridge module is carried out. Along with this the functionality of the LabVIEW interface and protection board is also verified. Once the gate driver, measurement circuit and protection board verification is performed a measurement routine and current controller tests are carried out at low voltage level. The power cycling test is performed for a short duration of time and conduction voltage measurement acquired during power cycling are analysed.

To sum up, this chapter presents the verification of the power cycle test bench and brief analysis of the measurement data acquired during the different stages of experimental validation.

4.1 Deadtime determination and verification

The minimum deadtime required is important to determine for preventing short circuit of the high and low side switches. The minimum required deadtime is determined by the maximum propagation delay difference and device turn on/off delay difference. Firstly the propagation delay difference from the gate driver IC is determined by utilizing the datasheet values [12]. The difference between the maximum and minimum propagation delay is calculated in (4.1).

$$\Delta t_{propagation} = 70ns - 50ns = 20ns \tag{4.1}$$

The next step is then to determine the delay difference between turn on and off of the SiC MOSFETs. To do so values for the capacitance and gate resistances are needed. The capacitance values will be presented in the upcoming section 5.1.3. However the results will be utilized in this section.

The turn on time delay present for a SiC module is determined by the time until which the gate-source potential reaches its threshold voltage. The threshold voltage is specified at 1 mA of current being conducted and is at 2.6 V. The initial voltage of the Gate is approximately -4.5 V and the Gate high voltage is 19 V. The voltage values can be used together with the input capacitance value and gate resistance to calculate the time delay

until which the SiC MOSFET will start conducting current as seen in (4.2).

$$t_{d(on)} = \frac{R_g \cdot C_{iss}}{-ln(\frac{V_{gs-th}-V_L}{V_H-V_L})} = \frac{12\Omega \cdot 6.2nF}{-ln(\frac{2.6V+4.5V}{19V+4.5V})} = 62.2ns \tag{4.2}$$

With the turn on time delay calculated, the following calculation will be performed to obtain the turn off delays resulting in a time difference needed for the deadtime.

Initially when turning off the SiC MOSFET the gate-source voltage has to decrease to its value of $V_{gs}(I_0)$. For the scenario investigated here, the current value chosen is the MOSFET rating of 10 A which yields an approximate gate-source voltage of 7 V as shown in section 5.1.2. The time until which the gate-source voltage reaches its I_0 limit is calculated in (4.3).

$$t_{d(off)} = \frac{R_g \cdot C_{iss}}{-ln(\frac{V_{gs}(I_0)-V_H}{V_L-V_H})} = \frac{12\Omega \cdot 6.2nF}{-ln(\frac{7V-19V}{-4.5V-19V})} = 110.7ns \tag{4.3}$$

When the gate-source voltage have reached a voltage of 7 V, The drain-source voltage will gradually increase, meaning the gate-drain capacitance is being charge from approximately 0 to 5 kV before reducing the current by pulling the gate-source voltage below its threshold. The current charging the drain-source capacitance C_{rss} should be calculated to determine the time until it is charged to 5 kV. Under the specific scenario a constant current will flow which is determined by the gate resistance R_g, $V_{gs}(I_0)$ and low gate driver voltage as seen in (4.4).

$$i_g = \frac{V_{gs}(I_0) - V_L}{R_G} = \frac{7V + 4.5V}{12\Omega} = 0.96A \tag{4.4}$$

The constant gate current will increase the voltage across the gate-drain capacitance and gradually increase the voltage across the MOSFET. The time until the drain-source voltage of the MOSFET is the full DC link voltage is calculated in (4.5).

$$t_{rv} = \frac{C \cdot dV}{I_g} = \frac{68pF \cdot 5kV}{0.96A} = 354.2ns \tag{4.5}$$

It should be noted that the capacitance used for calculating the time until V_{DS} is 5 kV is determined using the gate-drain capacitance of 100 V meaning a safety margin is present since the capacitance is reduced to half when above 1 kV. Combining the turn off delay times and subtracting the turn on delay, a time difference needed for preventing short circuit can be calculated as presented in (4.6)

$$\Delta t_d = t_{d(off)} + t_{rv} - t_{d(on)} = 354.2ns + 110.7ns - 62.2ns = 402.7ns \tag{4.6}$$

By adding the maximum difference of propagation delay from the gate driver, a minimum deadtime can be calculated as in (4.7)

$$\check{t}_{deadtime} = \Delta t_{propagation} + \Delta t_d = 20ns + 402.7ns = 422.7ns \tag{4.7}$$

However since both MOSFET at the instant of cross over will withstand the full DC link voltage during this instant, no short circuit will occur since they are not fully conducting. A safety margin has been implemented by setting the deadtime to $1\mu s$ meaning the complementary switch fully off before the opposite start conducting. A minimum deadtime of 422.7 ns is needed and a deadtime of $1\mu s$ has been chosen. The safety margin by a factor of 2 provides safety for variations in the capacitance values and threshold voltages due to temperature.

Before mounting the gate driver board on the power module the functionality of the gate driver board was tested. The gate signals directly measured on the gate-source pad of the gate driver are presented in Figure 4.1. It can be seen that during high and low state the output voltage is +19 V and -4.3 V respectively. This validates the functionality of the Flyback converter and Gate driver circuit. It can be seen that the deadtime for the High side and Low side gate signals for each leg is 1 μs.

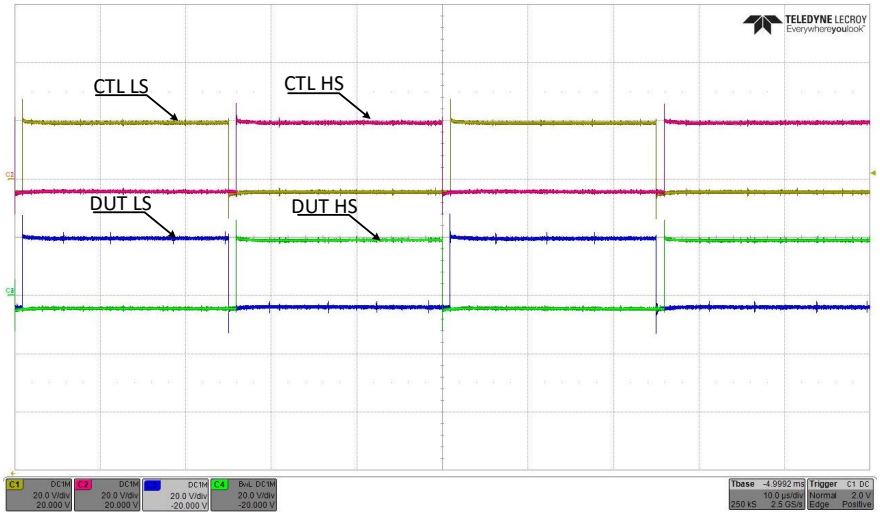


Figure 4.1. Measured Gate signal for CTL and DUT with duty cyle D = 0.5 and deadtime = 1μs

The power cycling can then be performed with confirmation that cross conduction will not occur.

4.2 Validation of conduction voltage measurement

A test was performed to verify the conduction voltage being measured by the measurement circuit on the gate driver PCB and displaying it on a LabVIEW interface. Gate driver board was detached from the module and a DC voltage of 4 V is applied across the drain

- source pads of the gate driver board. At particular time only one HS or LS gate - source pads are supplied with 4 V across it,whereas the rest are shorted and a measurement routine is initiated. This procedure is performed on High Side and Low Side drain - source terminals on both CTL and DUT gate drivers boards. Figure 4.2 shows the screen shot of the interface waveform chart display. As can be seen the measurement test data being sampled on the gate driver PCBs. V_{ds-on} and V_f for low side MOSFETs and diode measurements are referred to the positive ground. Therefore, the ADC measures negative voltage for low side V_{ds-on} and positive diode for forward voltage V_f. A LabVIEW interface is configured to scale all the measurement to positive values to display it on waveform chart. Also, the measurements displayed here in Figure 4.2 on LabVIEW interface are flipped due to the voltage being applied externally on the drain-source pad.

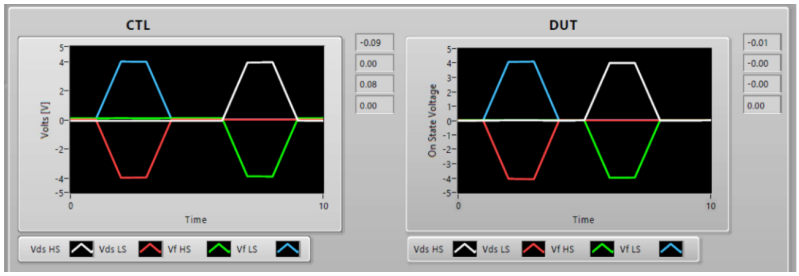


Figure 4.2. Verification of conduction voltage measurement on LabVIEW interface.

4.3 Experimental verification of measurement routine

Now, it has been verified that the ADC measurement is functioning and LabVIEW interface is displaying the correct data, the measurement routine can be performed. To perform the measurement routine DC link voltage was set to 200 V. The desired current magnitude at the end of the ramp up period was chosen to be 8 A. With DC link voltage of 200 V and load inductance of 10.35 mH, the ramp up time was chosen to be 414 μs based on Equation 2.16. The measured DC link voltage and load current during the measurement routine are displayed in Figure 4.3.

A zoomed view of the first measurement is presented in the Figure 4.4

It can be seen that the current is ramped up to 7.5 A during the first measurement. When comparing the load current profile during the free-wheeling period to the one presented in Figure 2.14 it can be observed that there is a steep decrease in current magnitude and current reaches zero during the free wheeling period. This is due to resistance of the load inductor, high V_{ds-on} of SiC MOSFETs and V_f of intrinsic/SiC JBS diode. The current decreasing to zero is not a problem due to one of the switches during the measurement routines is conducting ensuring the potential being clamped, protecting the ADC circuit. After the 1st measurement there is drop in DC link voltage of 20 V repeating itself in each consecutive measurement. At the end of the measuring routine the DC-link voltage drops to 134 V. Due to this the current magnitude at the end of ramp up period is not consistent for the subsequent measurement and decreases gradually as the measurement routine progresses. This is due to the DC link capacitor being discharged during the ramp up period when load current increases to approximately 8 A. Moreover the energy stored

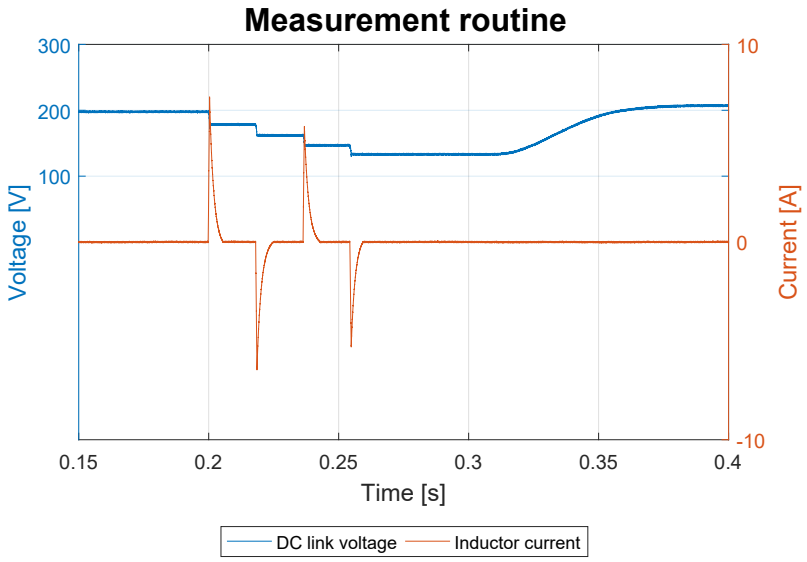


Figure 4.3. Measured inductor current and DC link voltage during measurement routine.

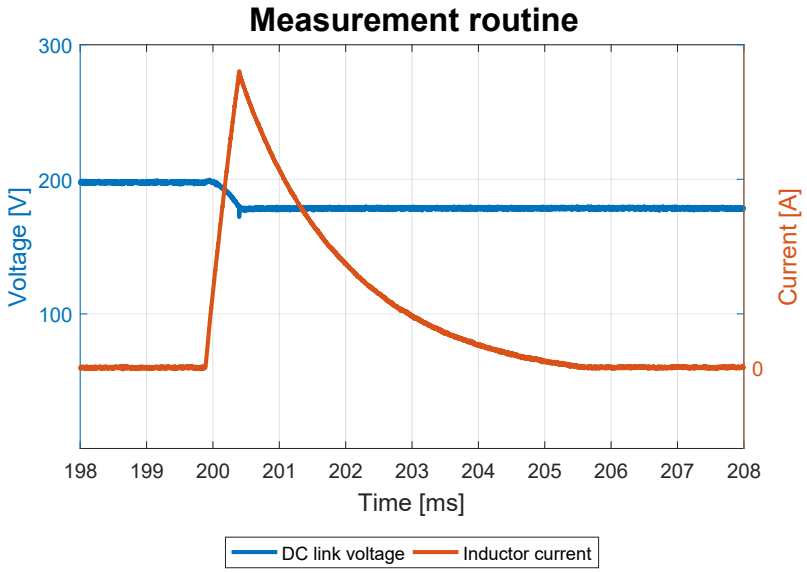


Figure 4.4. Zoomed view of inductor current and DC link voltage of the first measurement during measurement routine.

in the load inductor is proportional to current squared $\frac{1}{2} \cdot L \cdot I^2$ and the energy stored in the capacitor is proportional to voltage squared based on $\frac{1}{2} \cdot C \cdot V^2$. Meaning that when the DC link voltage is increased to the actual test voltage of 5 kV and maintaining a current ramp up of 8 A, no significant voltage drop will be present in the DC link voltage. There is a delay of 10 ms between each measurements and a delay of 1 s inserted after the measurement routine before the power cycling is initiated.

4.4 Experimental verification of controller and dead time compensation

Before the power cycling can be performed it is important to check the performance of the controller. The controller design and discrete realization of the controller as presented in Appendix D.1 is tested. To test the controller initially a current reference with a fundamental frequency of 5 Hz and peak amplitude of 1 A is provided to the controller. The DUT duty is set to 0.5 during the test. The test was performed with and without dead time compensation to investigate the effect of the parallel parasitic capacitance on the voltage error present. The results for both the cases are presented in Figure 4.5 and 4.6 respectively. As can be seen in Figure 4.1, when deadtime compensation is applied there is a distoration in the current waveform. This is contradictory to the simulation results being present in the Section 2.4. The reason for the distortion in the measured load current waveform in this case is due over compensation. Whereas, the PLECS simulation being performed without considering the device parasitics. The voltage error introduced by the parasitic parallel capacitors across the device has an opposite effect to the voltage error introduced by the deadtime. The voltage error introduced by the capacitors depends on the capacitance value, current magnitude, deadtime and DC link voltage. During the deadtime output voltage from an inverter leg does not change instantaneously but depends on the rate of charging/discharging of the parallel parasitic capacitor.

When deadtime compensation is removed the distortion in the current waveform is not present and measured current follows the reference with good accuracy.

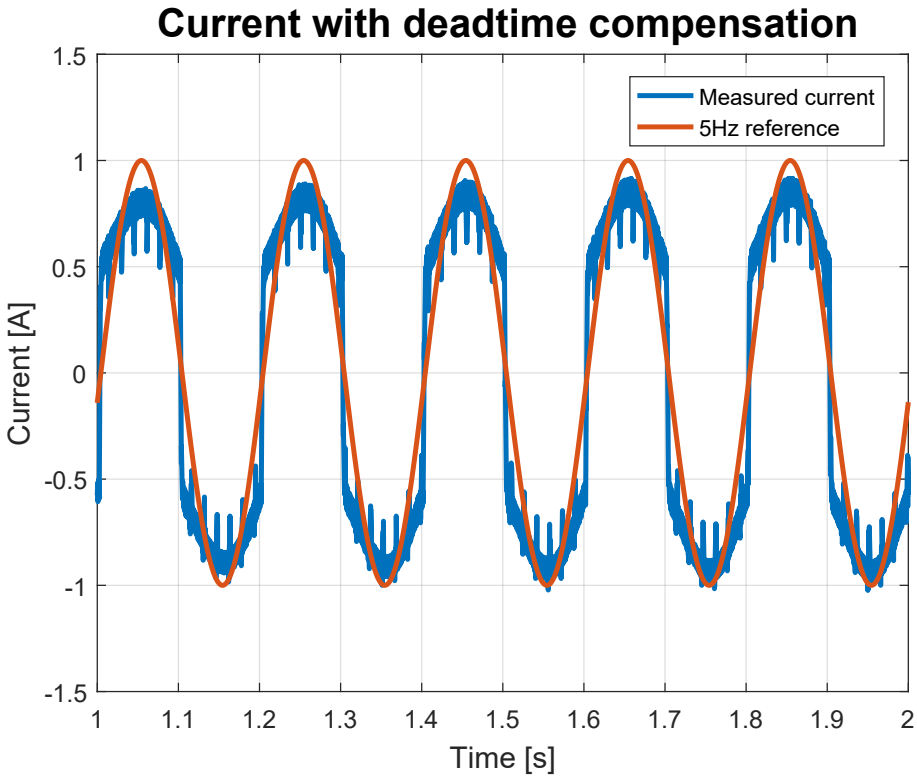


Figure 4.5. Measured inductor current with deadtime compensation compared to a 5 Hz reference.

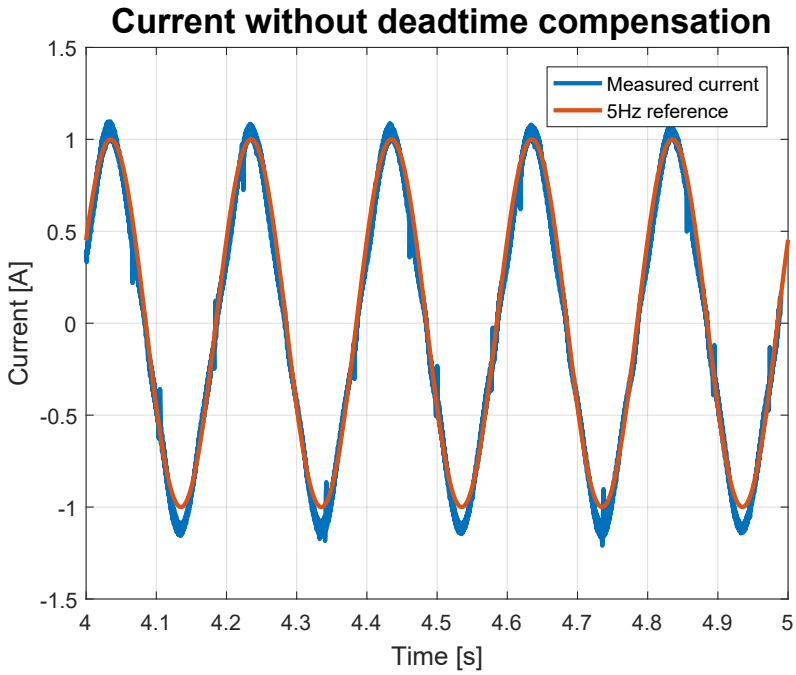


Figure 4.6. Measured inductor current with no deadtime compensation compared to a reference

4.5 Controller response for 5 A reference

Now, for this test the DC-link voltage raised to 500 V and the current reference with a frequency of 1 Hz and 5 A is applied to the controller. The PR controller is tuned for 1 Hz with gains Kp = 10 and Ki = 250. The measured load current and reference is presented in 4.7. The waveforms are captured from the instant where power cycling is initiated. Although, for such applications the dynamics of the controller are not of primary importance. It can be seen that the measured load current settles to reference within the first quarter of the fundamental cycle. Also, the measured load current follows the reference precisely with no steady state error and overshoot.

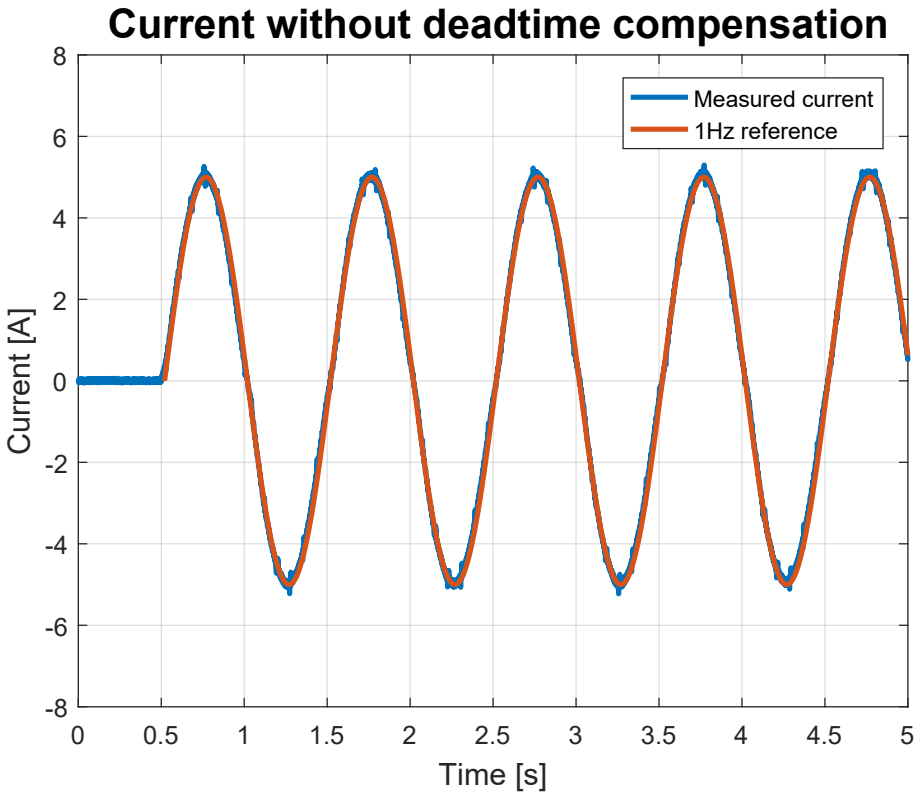


Figure 4.7. Steady state zoom for measured current and reference.

4.6 Low voltage verification

Now, as the control and measurement routine is verified. The continuous operation is performed, where controller is set to power cycle with the current reference magnitude of 1 A and frequency of 5 Hz. At every 30 seconds the power cycling operation is halted and measurement routine is initiated. In between two consecutive measurement routine there are 150 cycles within 30 second interval for 5 Hz current. The test was stopped after 12 measurements are acquired. This corresponds to the power cycling duration of the 360 s and total number of 1800 cycles. The result for the conduction voltages for both CTL and DUT module are presented in the Figure 4.8 and 4.9 respectively.

As can be seen there is no significant deviation in the acquired measurement data during the test. The average of these 12 samples of conduction voltages are presented in Table 4.1 below. It can be seen that the Forward voltage drop for the DUT HS (3.0281 V) and LS diode (2.9417 V) is higher than that of the CTL HS (1.5661 V) and LS (1.5013 V) module. This is expected as the DUT module does not contain an external diode in parallel with the MOSFETs and therefore uses its intrinsic diode which has a higher forward voltage drop as can be seen from V_f - I_f characteristics presented in Section 5.1.1, Figure 5.12. The on state drain source voltage measurement for both modules are in the range of (0.1554 V to 0.3494 V). Also in the case when CTL HS and LS MOSFET on state drain - source voltage measurement is performed the current free-wheels through the respective intrinsic diode of DUT module. Due to higher voltage drop of the intrinsic diode the current decays faster. Meaning that the current at which the measurement is performed is lower than for the DUT switch measurements. A small deviation is present

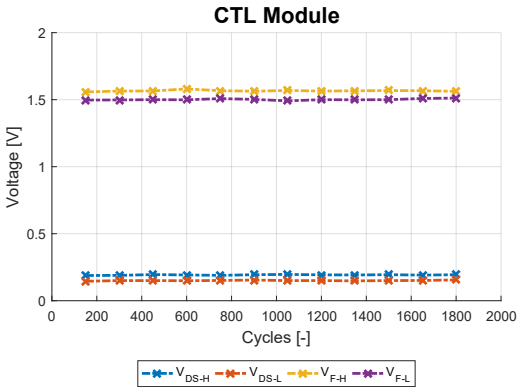


Figure 4.8. Measured conduction voltages for the CTL module with a DC link voltage of 200 V

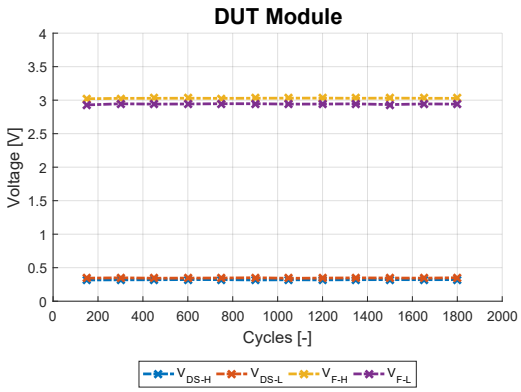


Figure 4.9. Measured conduction voltages for the DUT module with a DC link voltage of 200 V

in the HS and LS device conduction voltages. This can be because all the measurements are not performed at the exact same current due to the voltage drop on DC-link during measurements and small deviations in the R_{ds-on} and V_f of the devices.

Table 4.1. Measurement verification - Average of conduction voltages during 12 measurement routines

Module	V_{ds} **HS**	V_{ds} **LS**	V_{fd} **HS**	V_{fd} **LS**
CTL	0.1923 V	0.1502 V	1.5661 V	1.5013 V
DUT	0.3202 V	0.3460 V	3.0281 V	2.9417 V

During the test the temperature measurement was also performed on a high side MOSFET dies for both CTL and DUT module. The mean temperature was stable at approximately 26° for both CTL and DUT and no temperature swing was observed. Moreover, for the actual test the frequency of the current reference was changed to 1 Hz from 5 Hz to maximize the temperature swing. This will also provide better accuracy for the temperature sensor due to the sampling frequency of the temperature measurement being 1 kHz. A peak surface temperature for the dies of $80°C$ will be the limit to ensure temperatures below melting point of the die solder at $120°C$. The switching frequency will be lowered to 10 kHz to limit the mean temperature when switching at higher higher DC link voltages.

Chapter 5

Characterization and Power Cycling Results

This Chapter will include the results obtained for 10 kV SiC modules with Gen. 1 dies and a discrete Gen. 3 MOSFET. The results are summarised into two parts.

In the first part, power semiconductor device characterization for a 10 kV SiC MOSFETs half bridge power modules with and without external SiC diode will be presented. These test results includes: (i) V_{ds} - I_d, V_{gs} - I_d characteristics, capacitance measurements, determination of gate-source threshold voltage (V_{gs-th}) and gate leakage current I_{lkg}(ii) diode $I_f - V_f$ characteristics for MOSFETs intrinsic and intrinsic+external diodes. All characterizations are performed utilizing the curve tracer shown in Figure 5.1 with the wire fixture in Figure 5.2. All the characterization are performed at an ambient temperature of 24°C.

Figure 5.1. Image of the curver tracer utilized for characterizing power modules. Keysight Technologies B1506A

Figure 5.2. Image of the wire fixture and power module inside the curve tracer.

Key observations along with comparison for both of these modules are presented. Characterization is performed for Gen.3 10 kV SiC MOSFET discrete die with a purpose of investigating the improvements in next generation. A comparison for Gen. 3 and Gen. 1 SiC MOSFET is presented showing improvements in on-state resistance R_{ds-on} and forward voltage drop V_f of intrinsic diode.

Second part presents the test data from the power cycling test performed at reduced temperature stress levels. The results includes surface temperature measurements for MOSFETs and diode dies. The tests are analysed based on a profile of temperature swings and mean temperature measurements. The conduction voltage V_{ds} and V_f measurements for both CTL and DUT module are presented with statistical analysis. Finally, chapter ends with a brief summary and key findings based on the acquired experimental test results.

5.1 Infant Power Module characterization

A detailed characterization of the infant Half bridge module is necessary for identifying fault behaviour of the module after power cycling. The fault behaviour observed would ideally point towards a specific root cause of failure which can be experimentally proven. The characterization of the module before stress is therefore crucial for identifying the behaviour produced by the fault but also to verify its functionality.

The infant characterization are performed for all dies in two half bridge modules packaged with & without external diode, but only a selection of results will be presented in the report. The datasheet characterization of a Gen. 1 10kV 10A SiC MOSFET will be presented. Half bridge power module M3x1 containing external SiC diode can be seen in Figure 5.3. Whereas, module M3x3 is a half bridge power module without external diode. The names presented are given to the module during production and are therefore kept for future identification.

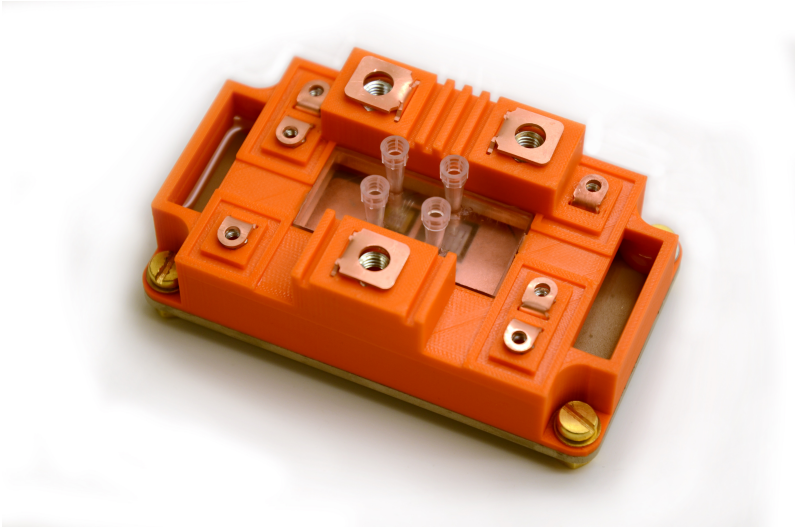


Figure 5.3. Package half-bridge module containing Gen. 1 SiC dies, made by Christian Uhrenfeldt, Szymon Beczkowski and Stig Munk-Nielsen at the Department of Energy Technology, at AAU.

The following sections will present analysis of the characterization measurement performed for a low side MOSFET ending in a comparison to a high side MOSFET which are identical dies in the same Half bridge module. The section ends with a comparison of Half bridge module M3x3 to M3x1 containing external diodes.

5.1.1 I-V Characteristics

The I-V Characteristics are presented as the conduction voltage of the MOSFET and intrinsic diode. The I_d is measured with a sweep in V_{ds} - at different gate biases, V_{gs}. The measurements provides information of R_{ds-on} at different gate-source voltages. The measurement also provides a minimum requirement of gate bias needed for operation with low conduction losses. The I_d - V_{ds} characteristics for V_{gs} of 0-12 V can be seen in Figure 5.4. It can be identified that a V_{gs} bias of 12 V is needed to operate in the Ohmic region for the rated current of 10 A. The on-state resistance gradually decreases as the V_{gs} increases to its maximum rating of 20 V as can be seen in Figure 5.5.

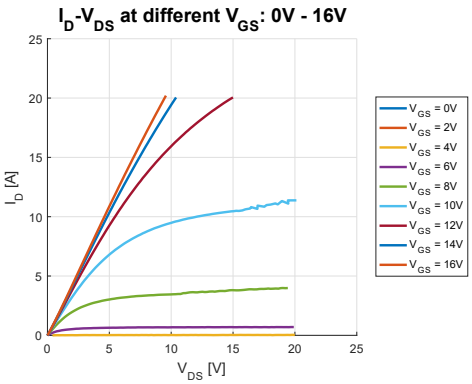


Figure 5.4. I-V Curves sweep at different Gate-Source voltage (0-12V)

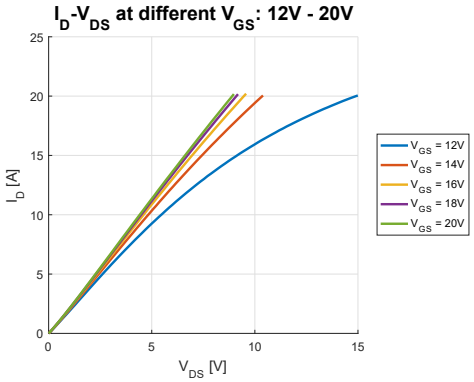


Figure 5.5. I-V Curves sweep at different Gate-Source voltage (10-20V)

Based on the measurements performed, a V_{gs} of 14 V or higher should be applied to have a low on-state resistance. The on state resistance from 14 V to 20 V of gate bias is presented in Table 5.1.

Table 5.1. On-state resistances at different Gate-Source voltage levels

Gate-Source voltage V_{gs}	On-state resistance R_{ds-on}
14 V	518 mΩ
16 V	474 mΩ
18 V	455 mΩ
20 V	445 mΩ

Preliminary datasheet from the device manufacturer specifies $R_{ds-on} = 500$ mΩ at $V_{gs} = 20$ V and $I_d = 10$ A. The positive gate bias of 19 V for the gate driver is therefore above the limit of 14 V and will ensure a low on-state resistance during conduction.

Measurements of the forward voltage for the intrinsic diode can be seen in Figure 5.6. A piecewise linear approximation of the measurements is performed for calculating the threshold voltage.

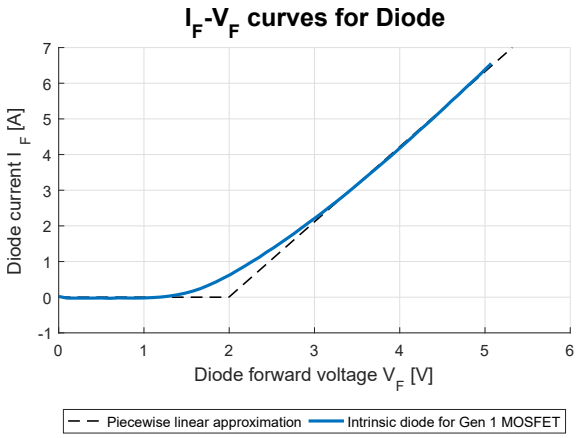


Figure 5.6. Intrinsic diode measurement Gen. 1 MOSFET

The threshold and forward voltage for the diode is specified in Table 5.2. It should be noted that the threshold voltage is obtained from a piecewise linear approximation from [3 V : 5 V] and the forward voltage is obtained from measured data.

Table 5.2. Caption of some sort

Specification	Voltage
V_t	2.00 V
V_f(6 A)	4.84 V

The I-V characteristics presented in this section will be used for fault behaviour investigation at the end of power cycling. The I-V characteristics are very important for the fault behaviour investigation since several expected failure mechanisms should be observable by comparison. The measurement can also be used for modelling the SiC MOSFET behaviour.

5.1.2 Gate threshold voltage

The purpose of investigating the gate threshold voltage is to determine weather a drift in voltage occurs or not. A drift in the threshold voltage can be an indication of gate oxide film deterioration and stacking faults. A generalised criteria for drain current at the gate threshold voltage is not established and even changes between datasheets of the same manufacturer [8], [9], [10]. The drain current criteria for the gate threshold voltage will in this report be specified as $I_d = 1$ mA. A graph of the gate-source threshold voltage will however be presented when discussed in detail as in this section. The gate-source voltage sweep for threshold determination are presented in Figure 5.7 and Figure 5.8.

From Figure 5.7 the $V_{ds} = 1$ V can be seen to reach its saturation at a gate-source voltage of approximately 12 V limiting the drain current to 1.6 A whereas at $V_{ds} = 40$ V the drain current limit was reached before a gate-source voltage of 11 V. The gate threshold voltage can be determined utilizing the data presented in Figure 5.8. The readings are combined in Table 5.3.

The threshold voltage will not only be compared using the 1 mA criteria since the slope

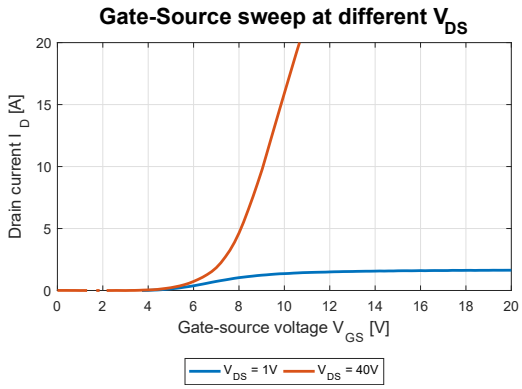


Figure 5.7. Gate-source voltage sweep for different V_{ds}

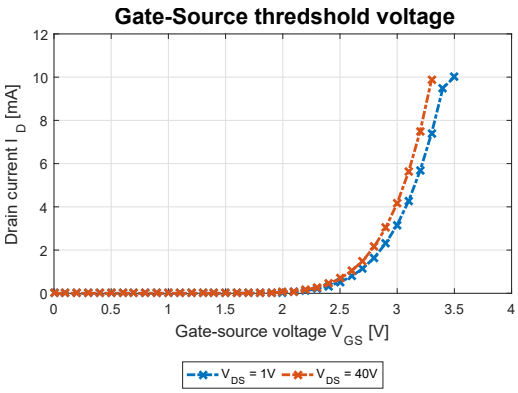


Figure 5.8. Gate-source voltage threshold identification using the 1 mA criteria

Table 5.3. Table of Gate-Source threshold voltages

Method	Gate-Source threshold V_{gs-th}
1 mA Criteria ($V_{ds} = 40$ V)	2.6 V
1 mA Criteria ($V_{ds} = 1$ V)	2.7 V
Steepest descent	7.3V

and knee of curve can deviate simultaneously making the 1 mA criteria a misleading point of reference. The comparison will therefore be drawn on 1 mA criteria as well as general curve properties as presented in Figure 5.7.

5.1.3 Capacitance

The capacitance of the packaged module are of major importance to rise and fall times and initial inrush currents during switching. The output capacitance contributes to the turn on switching losses due to the initial inrush current generated by the high dv/dt present due to fast switching transients. Capacitance values can also provide information about state of health of the devices since a degradation could manifest itself in reducing the capacitance value as is seen for capacitors [15,p.76]. The capacitance measurements are presented in Figure 5.1.3 as a function of V_{ds} up to 3 kV.

The capacitance values are extracted at three point of 100 V, 1 kV and 3 kV which is presented in Table 5.4.

Table 5.4. Capacitance of low side MOSFET at 100 V, 1 kV, 3 kV and 100 kHz

Capacitance			
V_{DS}	100 V	1 kV	3 kV
Input Capacitance (C_{iss})	6.198 nF	6.141 nF	6.107 nF
Output Capacitance (C_{oss})	277 pF	130 pF	99 pF
Reverse Transfer Capacitance (C_{rss})	68 pF	35 pF	28 pF

The capacitance presented in Table 5.4 are related to the capacitance values between Drain, Source and Gate as presented in (5.1). During turn-on and off transients the capacitance C_{rss} has to be charge or discharge for approximately the full V_{ds} and are

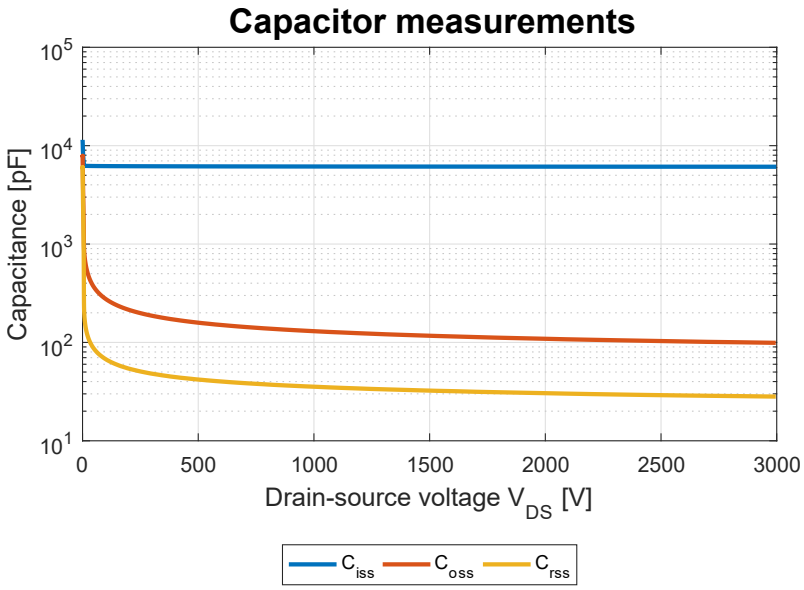


Figure 5.9. Capacitance measurements of Generation 1 MOSFET, low side (A).

determining the rise and fall times of the device. The output capacitance C_{oss} are a large contributor to turn on losses due to the fast switching transient and high dv/dt resulting in large inrush current of the complementary MOSFET. The input capacitance C_{iss} is determining the delay until which the MOSFET reaches its threshold voltage and starts dropping the drain-source voltage.

$$C_{iss} = C_{GS} + C_{GD} \qquad C_{oss} = C_{GD} + C_{DS} \qquad C_{rss} = C_{GD} \tag{5.1}$$

The capacitance therefore contains important properties for the MOSFET switching operation and could also utilized for investigating possible failure mechanisms and their effect on its performance.

5.1.4 Gate leakage current

The leakage current is measured for obtaining a reference for comparison when studying the fault behaviour of a degraded module. Increased leakage current can be an indication of stacking faults and deterioration in the gate-oxide film. The leakage current measurement is presented in Figure 5.10.

The absolute magnitude of leakage current are in the range of 100 pA. The measurements presented here are determining an infant level of leakage current which can be used for comparing a degraded module.

5.1.5 Comparison to high side MOSFET

A comparison for selected parameters of the high and low side MOSFET will be presented in this section. The purpose of comparing the two MOSFETs will be to determine weather a significant deviation between different dies and location are present. Information

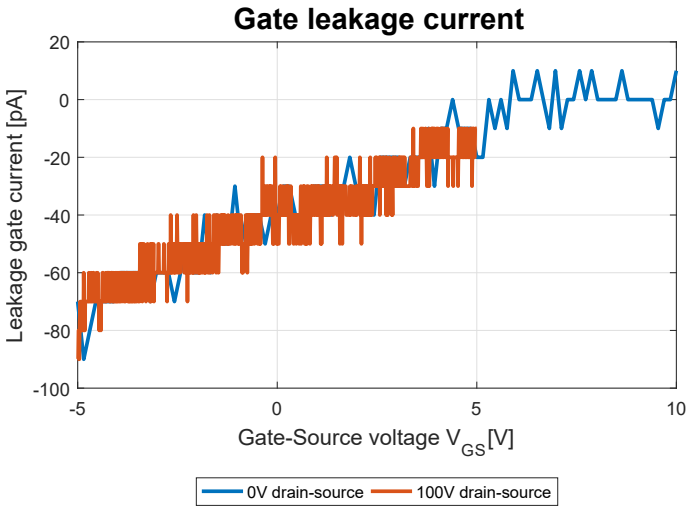


Figure 5.10. Gate leakage current at different drain-source voltages

about fluctuations in properties from one die to another might be useful for explaining or determining if a MOSFET is predisposition to fail early on. The comparison for selected parameters are provide in Table 5.6.

Table 5.5. Comparison of high (B) and low (A) side MOSFET for module M3x3.

Halfbridge Module without external diode		
	Low	High
Capacitance (3 kV)		
Input Capacitance (C_{iss})	6.107 nF	6,103 nF
Output Capacitance (C_{oss})	99 pF	149 pF
Reverse Transfer Capacitance (C_{rss})	28 pF	11 pF
Resistance		
V_{ds} = 16 V	474 mΩ	449 mΩ
V_{ds} = 18 V	455 mΩ	429 mΩ
V_{ds} = 20 V	445 mΩ	418 mΩ
Threshold		
Forward voltage V_f (6 A)	4.84 V	4.55 V
Gate Voltage $V_{gs-th}(V_{ds} = 40V, I_d = 1mA)$	2.6 V	2.6 V

From Table 5.6 it can be seen that a significant difference in C_{oss} and C_{rss} are present between the complementary MOSFETs. However since limited samples and capacitance difference of pF is present, the physical location in the module and deviation of die can not be excluded as explanations of the deviation. In the next section a brief comparison to the Half bridge module with external diode will be drawn. Initial expected deviations are output capacitance and forward voltage due to the parallel diode.

5.1.6 Comparison between Half bridge modules

The comparison between the two half bridges will be performed to identify the difference between the two modules. Module M3x1 are with external diodes where the module M3x3 as presented in previous section is without. The two Half bridge configurations have been

compared and no significant deviation of gate-source threshold voltage, on-state resistance and gate leakage current are present and will therefore not be used for further discussion.

The $I_f - V_f$ curves for the module M3x1 is presented in Figure 5.11. The threshold voltage differs from 2.0 V to 1.56 V when comparing to the module M3x3, graphically illustrated in Figure 5.12.

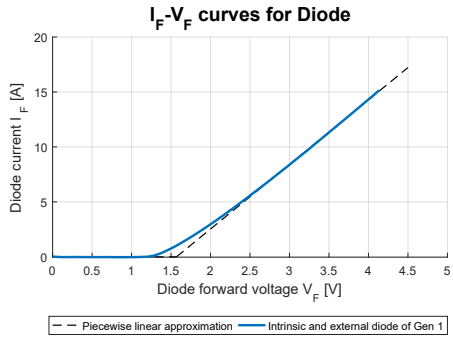


Figure 5.11. Diode characteristics with external and intrinsic diode.

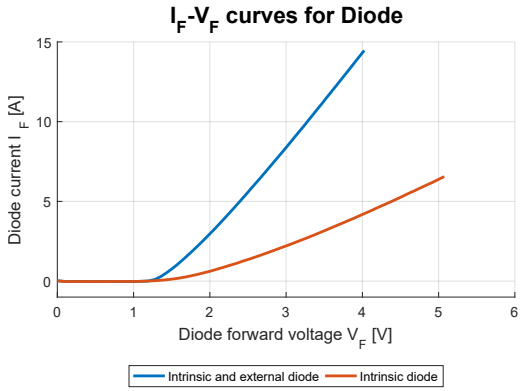


Figure 5.12. Comparison of diode characteristic with and without external diode.

It can be seen from Figure 5.12 that with an external diode, the intrinsic diode will be forward biased and conduct a fraction of current. With a current I_f of 8 A for example approximately 2 A of the current will be conducted through the intrinsic diode , which are not completely bypassed.

The capacitance measurement of the two modules are presented in Table 5.6. The Input and Reverse transfer capacitance of both modules are comparable, which were also expected due to no change of the MOSFETs. The output capacitance for M3x1 has increased for high and low side when comparing to M3x3 as expected due to the parasitic capacitance of the external diode.

Table 5.6. Comparison of Half bridge modules with external diode (M3x1) and without (M3x3)

Halfbridge module comparison				
	M3x1		**M3x3**	
Capacitance (3 kV)	Low	High	Low	High
Input Capacitance (C_{iss})	6.098 nF	6.081 nF	6.107 nF	6,103 nF
Output Capacitance (C_{oss})	157 pF	177 pF	99 pF	149 pF
Reverse Transfer Capacitance (C_{rss})	27 pF	16 pF	28 pF	11 pF

With the characterization for the two modules utilized, the results can be used for comparison of the modules after degradation and hopefully provide information about new failure modes and behaviours or confirming the presence of persisting failures from Si devices.

5.2 Discrete Gen. 3 MOSFET

The purpose of this section is to present the result for the discrete Gen. 3 SiC MOSFET and compare it to the Gen. 1. The comparison will present improvements of the Gen. 3 die and compare it to the fault behaviour documented in section 1.1. The discrete package Gen. 3 SiC MOSFET can be seen in Figure 5.13.

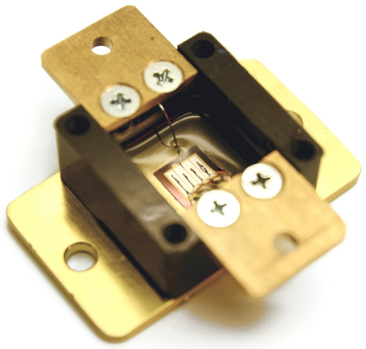


Figure 5.13. Discrete package of Gen. 3 10 kV SiC MOSFET, made by Christian Uhrenfeldt, Szymon Beczkowski and Stig Munk-Nielsen at the Department of Energy Technology, at AAU.

The I-V characterisitcs for the Gen. 3 MOSFET die is presented in Figure 5.14 and Figure 5.15. The resistance value might vary due to the comparison are performed between a package module and a discrete package.

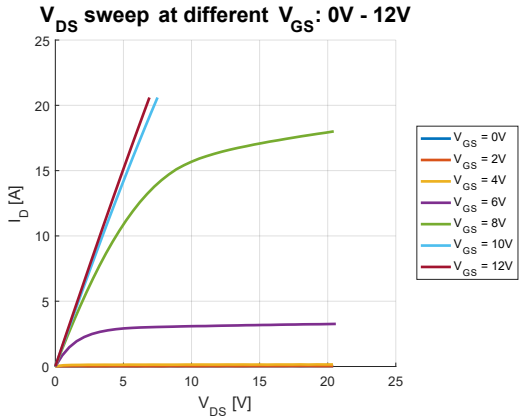


Figure 5.14. I-V Curves sweep at different Gate-Source voltage (0-12V)

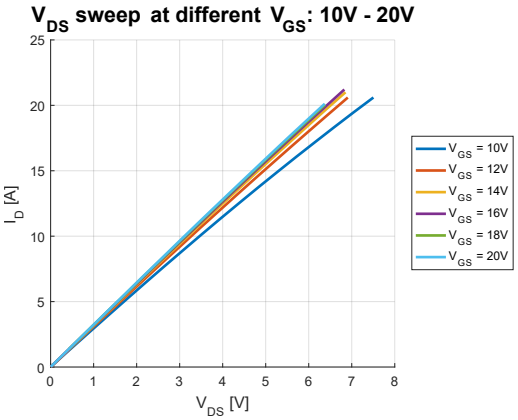


Figure 5.15. I-V Curves sweep at different Gate-Source voltage (10-20V)

If Figure 5.15 is compared to the ohmic region of the Gen. 1 MOSFET it can be identified that the Gen. 3 MOSFET enters the Ohmic region at 10 V compared to the 14 V of the first generation. For a more detailed comparison on-state resistance values for both generation dies are combined in Table 5.7.

From Table 5.7 it can be seen that a lower gate-source voltage is required to enter the

Table 5.7. On-state resistances comparison for generation 1 and 3 MOSFET dies.

Gate-Source voltage V_{gs}	On-state resistance R_{ds-on}	
	Generation 3	Generation 1
10 V	365 mΩ	-
12 V	336 mΩ	-
14 V	327 mΩ	518 mΩ
16 V	322 mΩ	474 mΩ
18 V	319 mΩ	455 mΩ
20 V	317 mΩ	445 mΩ

ohmic conduction region for the Gen. 3 MOSFET. A decrease in the gate-source voltage would reduce the electric field strength across the oxide layer and reduce the rate of degradation as was discussed in the Section 1.1 as a failure mechanism. Furthermore the on state resistance for the discrete Gen. 3 die is 29 % less than for the package module with the Gen. 1 die. Lower temperature swings or increased current capability could be achieved for the Gen. 3 die since a lower conduction resistance is identified.

The on-state resistance of the MOSFET are decreased in the Gen. 3. However a new failure mechanism of the intrinsic diode for a MOSFET has been documented. The I-V characteristics of the diode are therefore interesting to analyse and identify difference from Gen. 1 to Gen. 3. The I-V characteristic for the intrinsic diode can be seen in Figure 5.16.

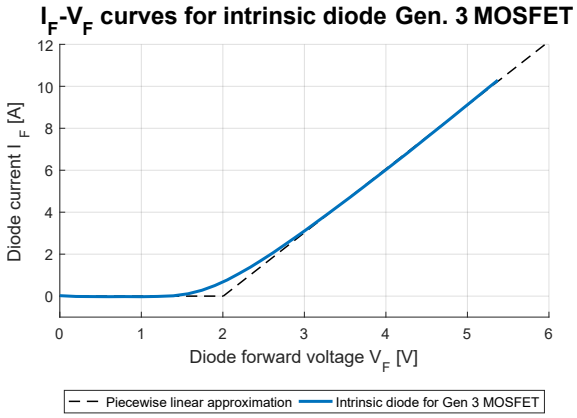


Figure 5.16. Intrinsic diode measurement of Gen. 3 MOSFET.

To provide points of comparison, values for threshold and forward voltage at 6 A has been combined for Gen. 1 and Gen. 3 in Table 5.8.

Table 5.8. Comparison of 1 and 3 generation intrinsic diodes.

Specification	Voltage	
	Generation 3	Generation 1
V_t	2.00 V	2.00 V
V_f(6 A)	3.99 V	4.84 V

Forward characteristics of the intrinsic diode shows a threshold of 2 V for both generation which is higher than the threshold voltage of 1.56 V measured for the module with an

external diode. The forward voltage of the Gen. 3 diode has decreased from 4.84 V to 3.99 V which in good coherence with the on-state resistance decrease as presented earlier in this section. The reduced conduction resistance could be an indication of the drift-layer having a low density of BPDs, previously presented as the cause of a failure mechanism called stacking faults. A change can therefore be identified, indicating a possible improvement in preventing the formation of stacking faults.

A comparison between capacitance measurement of Gen. 1 and 3 will not be performed, since the packaging of the die will have a significant impact on the value and no conclusion can be drawn from it. A similar threshold voltage for the discrete 3 generation die and the packaged 1 generation were measured of 2.6 V for $I_d = 1$ mA and $V_{ds} = 40$ V. No significant difference in leakage current was measured as well and will therefore likewise not be presented.

5.3 Die Surface Temperature Monitoring

The mean temperature and temperature swings are measured on the surface of the die utilizing an optic fiber temperature measurement. The purpose for measuring the temperature is to obtain information about stress level imposed on the dies together with information about their thermal performance. The measurements are also a safety precaution for preventing overheating of the SiC module under power cycling. The temperature measurements are performed by inserting the optic fiber through a channel formed in the module. Inside the module a small amount of thermal paste is present to ensure a good thermal conduction between the temperature sensitive crystal and the die. The inserted optic fiber, channel and module can bee seen in Figure 5.17.

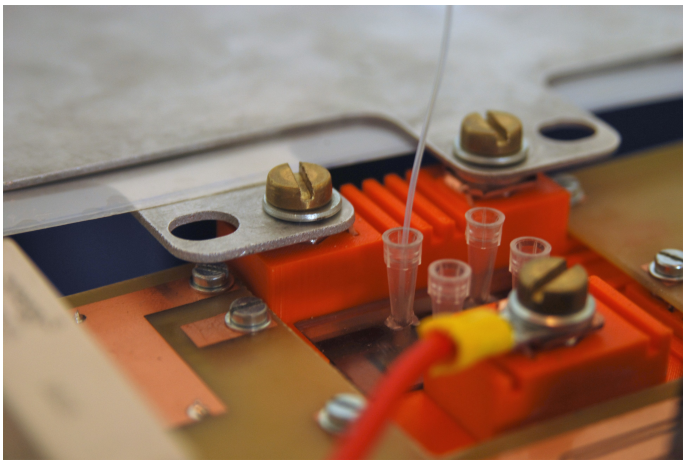


Figure 5.17. Optic fiber inserted in power module - for die surface temperature measurement.

The optic fiber is being held by a stand to establish a straight insertion. Even with a stand the insertion and thermal connection is varying, a few iterations of insertion are therefore needed for capturing the thermal swings. The absolute value of the temperature swing are therefore coupled with a degree of uncertainty. The sampling frequency of the temperature measurements is 1 kHz and the fundamental current waveform is 1 Hz. The instantaneous temperature increase due to switching loses can therefore not be measured but only its

mean value. The temperature swing produced by the 1 Hz current however can be measured with the optic fiber. The next sections will present temperature measurements of MOSFET and diodes for CTL and DUT modules. Temperature measurement of all dies provides information about the dies mean temperature and temperature swings. The measurements provides the information of which dies to observe when setting the limitations of the stress levels applied during power cycling. The ambient temperature during measurements were approximately $24°C$.

5.3.1 CTL Switches

The temperature measurement presented in this section is for the upper and lower switch of the CTL module with external diodes. The temperature measurements are performed at $V_{dc} = 500$ V,$f_{sw} = 20$ kHz, $\widehat{I_L} = 5$ A and a fundamental frequency of 1 Hz. The temperature variations can be seen in Figure 5.18. From the figure an amplitude of the temperature swings can be identified to be $2.4°C$ and a mean temperature of $28°C$.

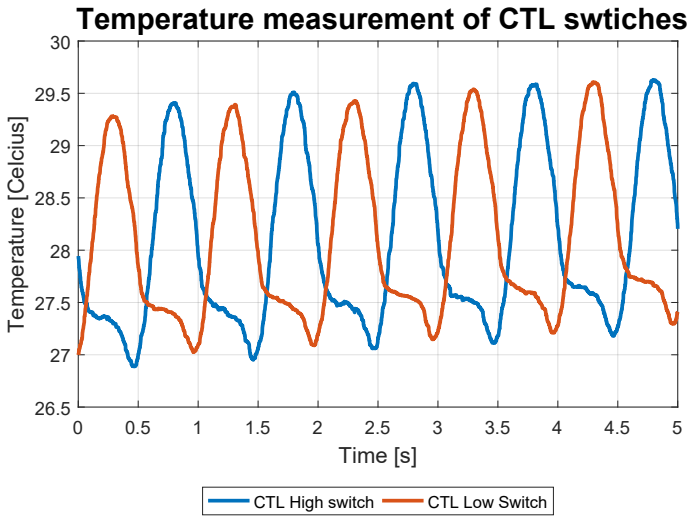


Figure 5.18. Temperature measurement of CTL high and low switch during 5A of power cycling.

As can be seen from Figure 5.18 a pure sinusoidal temperature swing is not obtained. If CTL low switch is taken as an example, it can be identified that the temperature increases and decreases, following the reference of the current. When the current becomes positive, meaning the High switch and external low diode conducts, a plateau of the low switch temperature can be identified. The plateau could be caused by the MOSFET and intrinsic diode not being bypassed by the external diode as were presented in Section 5.1.6. The current passing through the MOSFET and intrinsic diode will produce a power dissipation. The temperature drop at the end of the 1 Hz period could be explained by the current approaching 0 at the end of its fundamental cycle.

When analysing the figure it should be remembered that the test is performed at 0.5 duty cycle meaning that if a fundamental voltage sinusoidal is added the stress will be redistributed as presented earlier in Section 2.2. The intrinsic diode can not be completely bypassed, however the time which it conducts relative to the complementary switch can be controlled.

5.3.2 CTL Switch and diode

A comparison of the temperature swing between diode and switch are of big importance when considering the limiting factor for the current carrying capability of the module. The temperature for low switch and low diode is measured for identifying the temperature swing during power cycling. The measured temperature variation is presented in Figure 5.19

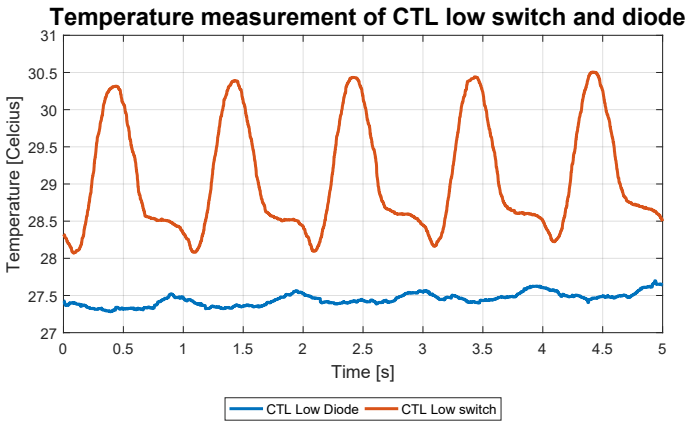


Figure 5.19. Temperature measurement of CTL High MOSFET and external diode.

From Figure 5.19 low temperature swings of the diode is present compared to the switch. An explanation for the lower temperature swings could be found in the fact that the external diode does not conduct the full current and the larger surface area of the die. However the temperature variations measured are very low so an imperfect thermal connection between diode die surface and optic fiber could also be an explanation.

5.3.3 CTL vs DUT Switches

The temperature of CTL and DUT low switch are measured. The temperature swing for the DUT consists of a 2 Hz signal due to the switch and intrinsic diode of the MOSFET conducting during a fundamental cycle. The temperature swings are presented in Figure 5.20.

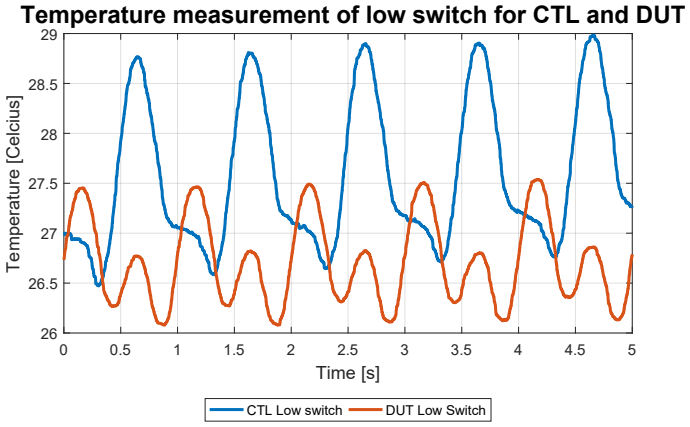


Figure 5.20. Temperature measurement of CTL and DUT low switch.

The low switch of CTL and DUT is measured, meaning the MOSFET will conduct current opposite each other during a cycle. From Figure 5.20 a temperature increase can be identified for the DUT low switch when CTL low switch is conducted, the temperature increase is due to the conduction of the intrinsic diode and the MOSFET. It can be identified that the DUT has two temperature swing during a 1 Hz period and has lower temperature swings. The lower temperature swing can be explained by the fact that power is dissipated twice during a cycle. The temperature swing of the DUT MOSFET are measured to an amplitude of $1.4°C$. The mean temperature for the DUT was expected to be higher than for the CTL due to intrinsic diode conducting and dissipating power.

5.3.4 DUT Switches

The measurement for the DUT switches showed an initial offset in temperature measurements of $0.75°C$. The initial offset has been added to the measurement presented in Figure 5.21.

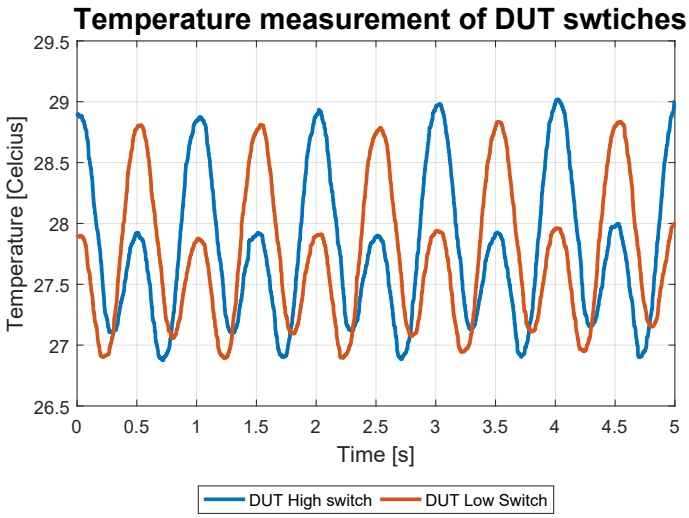


Figure 5.21. Temperature measurement of DUT low and high switch.

A temperature swing of $2.0°C$ are observed for both high and low MOSFET. It can be seen form the temperature measurements that two temperature swings are present during one fundamental cycle of conducted current. This is also expected since the intrinsic diode is conducting a larger fraction of the current and the power dissipation is therefore increased when an external diode is not present. The power dissipation of the intrinsic diode produced a temperature swing of $1.0°C$. From the temperature measurements of both CTL and DUT it can be identified that the two switches operate at approximately the same temperature when conducting 5 A of current, switching at 500 V and with a Duty cycle of 0.5. Due to the low temperature swings, mean value difference compared to the ambient temperature and the offset seen for the DUT high and low switch measurements some uncertainty is associated with the temperature measurement. One temperature measurement of a switch from CTL and DUT will therefore be monitored to ensure a safe operating temperature during medium voltage power cycling.

5.4 Power Cycling Test Results

Before determining the operating point for the power cycling a selection of the maximum allowed deviation of conduction voltages needs to be chosen. The limits of conduction voltages are set to halt the test bench, if the module is expected to be at its end of life. The measurement deviations are investigated at 500 V and 5 A to minimize the temperature stress exerted on the module while determining the measurement deviations. A maximum temperature swing of $2.5°C$ and a mean temperature of $28.1°C$ was previously measured for this operating point, verifying low thermal stress experienced by the modules.

5.4.1 Distribution of conduction voltage

A 105 samples were taken to determine the variation of the conduction voltages for all dies. The total duration of the power cycling test performed was approximately 2 hours and 60 fundamental cycles of current were present between each measurement. This yields a time of 1 minute between consecutive measurement routine. The measured conduction voltages during the power cycling CTL and DUT module can be seen in Figure 5.22 and 5.23 respectively.

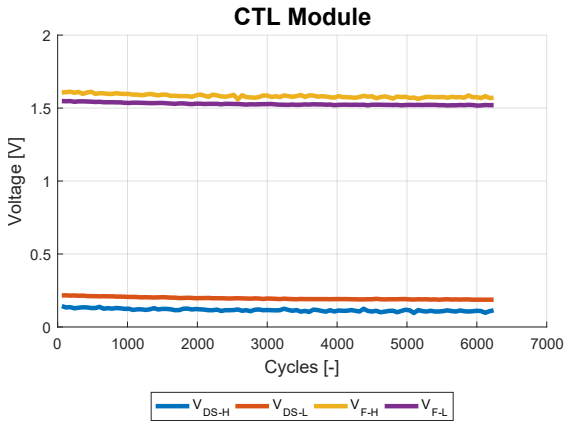


Figure 5.22. Measured conduction voltages for the CTL module during 500 V, 5 A power cycling

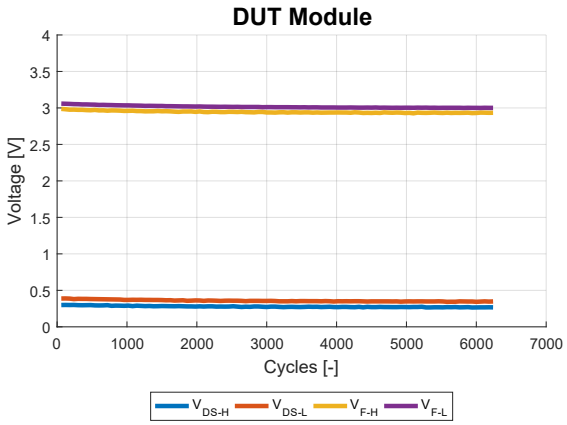


Figure 5.23. Measured conduction voltages for the DUT module during 500 V, 5 A power cycling

When comparing Figure 5.22 and 5.23 two distinctions are important to identify. The first being a difference between the forward voltages measured from CTL module to DUT, the difference in voltages were also expected based on the measurements previously presented since the intrinsic diode has a higher threshold voltage and forward voltage when compared to the module with external diode. Another thing to observe is that the conduction voltage of the switches are lower for CTL when compared to the DUT, the reason for the voltage difference is a deviation in the current magnitude at the instant of the sampling. The intrinsic diode provides a higher voltage drop, decreasing the current through the inductor more rapidly and the current during the instant of the measurement is therefore less than when the DUT switch is measured.

With the difference in voltage amplitude been addressed, the deviation of measurement can be analysed. To do so the mean (μ), standard deviation (σ) and maximum deviation

are calculated. The standard deviation can be calculated as seen in 5.2.

$$\sigma(x) = \sqrt{\frac{\sum_{n=1}^{N}((x(n) - \mu)^2)}{N}} \tag{5.2}$$

N '= Total number of Samples, x(n) = n^{th} sample Where, n = 1,...,N

The result from calculation can be seen in Table 5.9.

Table 5.9. Statistic data of the offline measurement routine during power cycling at 500 V and 5 A. HS = High Switch, LS = Low Switch, HD = High Diode, LD = Low Diode.

Device		**Mean (μ)**	**Standard deviation (σ)**	**Max - Mean**	**Mean - Min**
CTL	**HS**	0.1162 V	8.3445 mV	27 mV	20 mV
	LS	0.1963 V	9.1583 mV	21 mV	9 mV
	HD	1.5831 V	3.6184 mV	29 mV	23 mV
	LD	1.5278 V	8.0009 mV	20 mV	11 mV
DUT	**HS**	0.2777 V	9.3963 mV	22 mV	13 mV
	LS	0.3579 V	11.8021 mV	31 mV	15 mV
	HD	2.9450 V	13.5934 mV	42 mV	19 mV
	LD	3.0160 V	15.5345 mV	43 mV	16 mV

A criteria as a 99% confidence interval for the measurement being a fault behaviour and not a measurement deviation is however not a desirable criteria for the test to be halted, since many thousands of sample will be performed during power cycling. However it is desirable to use the cumulative distribution function to provide a visual interpretation of the data. The cumulative distribution for a measurement performed of a diode and a switch is therefore presented for both CTL and DUT, which can be seen in Figure 5.24 and Figure 5.25 respectively with the upper and lower limit of measurement marked with dashed lines.

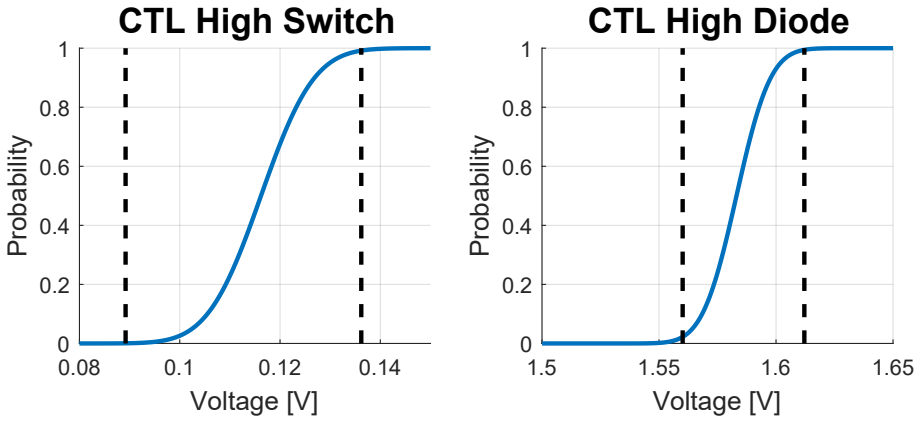


Figure 5.24. Cumulative probability function for measured conduction voltages of the CTL module.

A maximum voltage deviation from mean is 43 mV and a total variation from max to min of 61 mV are measured. What can be concluded from the measurement presented in

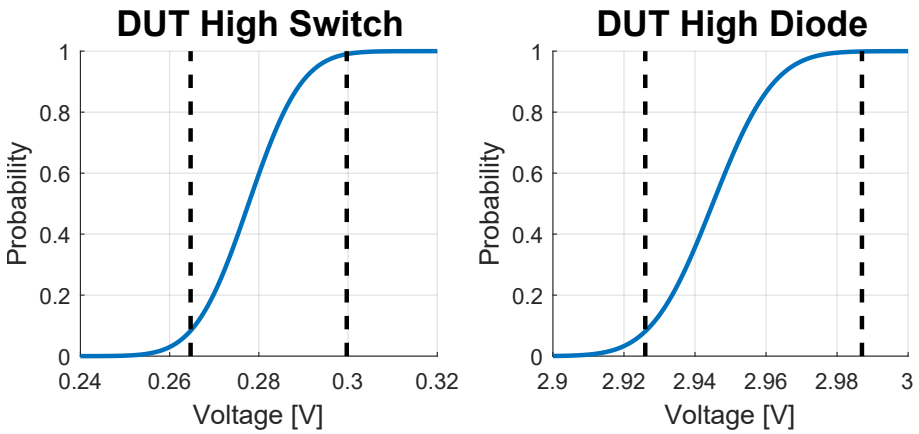


Figure 5.25. Cumulative probability function for measured conduction voltages of the DUT module.

Figure 5.24 and 5.25 are that individual reference or mean value for each switch and diode has to assigned due to variation in die resistance and the deviation in current during free wheeling.

The conduction voltage of the the dies also changes over time, an explanation of the deviation can be found in the change of current at the point of measurement and temperature effect on die resistance. From the measurement performed it can be identified that the current gradually decreases during cycling until it slowly settles on a value. The behaviour can be identified by the current measured during sampling and conduction voltage for a switch as shown in Figure 5.26. The gradually decreasing current during measurement is common for all sequences of the measurement routine.

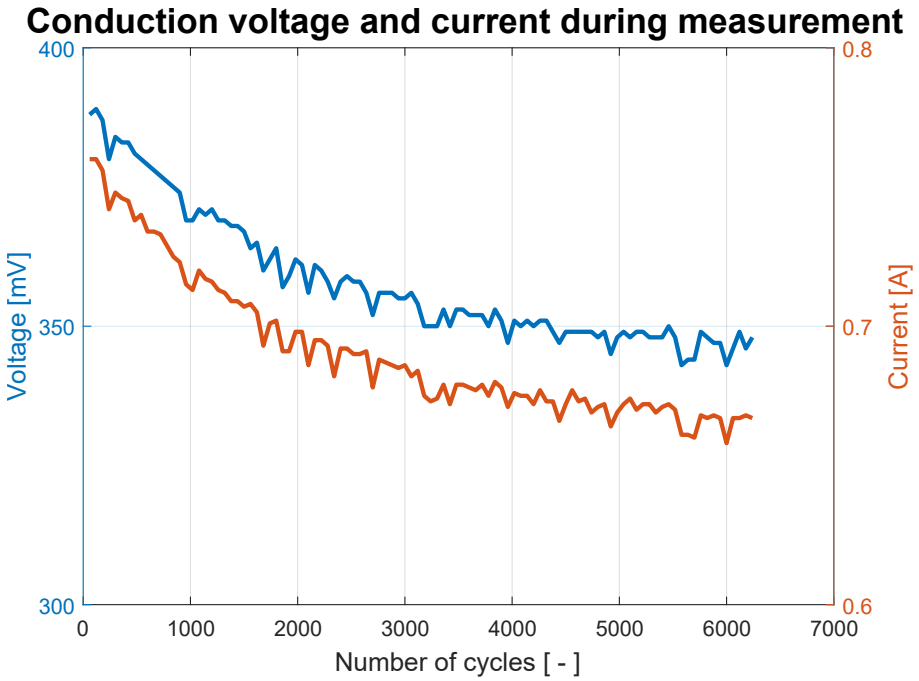


Figure 5.26. Conduction voltage measurement of DUT module low switch and current during third measurement routine.

A clear identification of the linear relationship between current and conduction voltage during measurement can be seen in Figure 5.26. The behaviour for all switch conduction voltage and currents are similar. The slow drop in current could be explained due to the increase in ambient temperature. The ambient temperature increase could produce losses due to a positive temperature coefficient of forward voltage for the diodes and increase in MOSFET on-state resistance. The increase in forward voltage and on-state resistance would decrease the current to a lower value and that could explain the gradual reduction of the current as shown in Section 4.3. The switch temperature of CTL was measured during the power cycling test and it reaches a mean temperature of $30°C$ and temperature swings of $2.7°C$ verifying low thermal stress exerted on MOSFETs.

5.5 Summary

Characterization data for the half bridge power modules will be utilised for the device modeling and investigating the fault behaviour after the accelerated wear out test. The device capacitance measurements provides useful information on device switching characteristics and basis for determining the gate drive requirements for a MOSFET. Device on state resistance and diode forward voltage obtained from $V_{ds} - I_d$ and $V_f - I_d$ characteristics could later be utilised to calculate the conduction losses for a device at given operating condition. Furthermore, no significant deviation in the device parameters were observed for different MOSFET and diode dies.

Characterization of Gen.3 discrete dies shows significant reduction in the on state resistance and the gate - source voltage at which MOSFETs enters the ohmic region. Reduced on state resistance will lower conduction losses and lower gate - source bias requirement will ensure the lower stress of the gate oxide film layer.

The power cycling test lasting for 2 hours presents reliable operation of the test bench and consistency in acquired conduction voltage measurements. One thing that was observed is the gradual decrease in the measuring current during first 6000 cycles of load current. This deviation can be due to the thermal dependency of the system. After the temperature on the power module reaches steady state and homogeneous temperature is established, no significant deviation is observed in the measurements. Temperature measurements and swings for the MOSFET and diode dies show a good coherence with a fundamental cycle of the current and power dissipation due to the conduction losses on respective dies.

Chapter 6

Conclusion

A power cycle test bench capable of operating at 5 kV with necessary protection and dedicated LabVIEW user interface is designed. The functionallity of the test bench is experientially validated at low voltage level during the project. A gate driver circuit with high common mode noise immunity and incorporated V_{ds-on} and V_f offline measuring circuit is designed and implemented.

Test data obtained during the characterization of packaged power module utilizing Gen. 1 and discrete Gen. 3 10 kV SiC MOSFETs were analysed and a brief comparison between these two dies are presented. Key observations are the lower on state resistance and significant reduction in the gate-source voltage at which MOSFET enters into an ohmic region. The later also indicates that the gate-source voltage to drive the SiC MOSFET shows tendency to reduce in the next generation dies. Forward voltage drop for the intrinsic diode is lower for the Gen. 3 MOSFET compared to Gen. 1 indicating reduced BPD in the newer generation reducing the formation of stacking faults. Diode I-V characteristics for a power module with and without diode SiC JBS diode is presented, which shows that the intrinsic diode will not be bypassed completely and is conducting a fraction of current. The data for the infant module characterization will be utilised to analyse the data obtained from the wear out test and fault behaviour after degradation.

Temperature measurements are performed on the die surface during power cycling, utilizing a fiber optic temperature sensor. A temperature measurement on the MOSFET die on a module with external diode experience higher temperature swings compared to the one without external diode under similar stress level of current. Utilizing the intrinsic diode results in temperature swing of twice the fundamental frequency of current, lowering the magnitude of temperature swings. However the mean temperature for both dies show correlation at low voltage. Furthermore a plateau in the temperature measurement for the MOSFET with external diode indicates power dissipation in MOSFET and intrinsic diode due to current sharing.

Power cycling test at 500 V and 5 A for a time duration of 2 hours has been performed. Statistical analysis of the measurements has been performed for the acquired conduction voltages. Finally, the discussion and future improvements are presented in the following section.

Chapter 7

Discussion

In this section a discussion will be presented for the future work, challenges and measurements. The chapter will be split into different topics of discussion addressing a particular issue.

Measurement Routine

An issue during measurement routine is the decaying current within the operating time of the reed relays. The relatively high conduction voltages of the MOSFETs, diodes and series resistance of the inductor produces a voltage across the load inductor which gradually decreases the current. This could be a potential issue since the voltage measurements are being used as an indication of the state of health of the power module. An increase in conduction or forward voltage could be obscured by the decrease in measuring current. However the effect on current will be dependent on the overall resistance and inductance of the system and might therefore still be detectable by monitoring the conduction voltage. Some possible improvements will be discussed to address this issue.

The first possible improvement could be to reduce the resistance of the inductors and increase the inductance. The decrease in resistance will produce a lower voltage drop across the inductor and thereby a slower decay of current.

A second possible improvement would be to calculate the on state resistance for a state of health monitoring, however using the resistance is not possible for diodes due the threshold voltage. A determination of permissible deviation from measured $I_f - V_f$ could be a solution for monitoring the state of health for diodes.

A third possible improvement could be to change the measurement routine from a double pulse test, to a constant current control. A PI controller could then be used for controller the opposing half bridge maintaining a constant current through a switch which can be measured by the ADC. The limitation of this method would however exclude the measurement of diode forward voltage. No changes to the setup is required except change in execution of measurement routine in DSP. The state of health for the intrinsic diode can still be monitored since an increase in drift-layer resistance could be observed by measuring the conduction voltage of the MOSFET.

Uncertainity in temperature measurement

Some uncertainties are related to the temperature measurements. One of the assumptions made is that the internal temperature of the die is close to the measured surface

temperature. This assumption is however only correct if a low thermal resistance is present between die and the temperature sensor. The optic fibers are very thin and should be gently inserted to prevent bending. If the fiber is bend a poor contact between die and fiber could be the results. Another uncertainty is that a small amount of encapsulation material could have gathered and filled the channel intended for the fiber obstructing the path to die. These uncertainties are however aimed to be reduced by measuring both high and low side of the module verifying coherence in mean temperature and swings. Low temperature swings have been introduced so far for the 10 kV SiC power modules and more results at higher levels of power dissipation is therefore required for evaluating the degree of uncertainty present for the temperature measurements.

Mean temperature of MOSFET dies

One interesting aspect that has not yet been fully investigated is the mean temperature difference between the MOSFET dies with and without external diodes. Accessing the power dissipation of the two power modules is not a straight forward task since it is depending on different factors. The power module without external diode will have higher power dissipation during conduction due to the high forward voltage of the intrinsic diode. The switching losses for the module without external diode would however be smaller due to a lower parasitic output capacitance. The lower output capacitance will decrease the inrush current magnitude and thereby the switching losses. The balance of mean temperature will therefore depend on the current being conducted through the devices and their switching frequency.

Appendix A

Busbar design

A custom - made busbar is designed for a packaged SiC half brige power module. The busbar utilizing a sandwiched layout is preferred to obtain low stray inductance from DC - link capacitor to power module. The capacitors used are two parallel connected 50 μF low ESR Polypropylene thin film capacitors with a rated DC voltage of 5 kV [16]. The busbar is built with an Aluminium plate which symmetry enables it to be flipped, obtaining the correct terminal distance between the high - low potential. A top view of the busbar can be seen in Figure A.1.

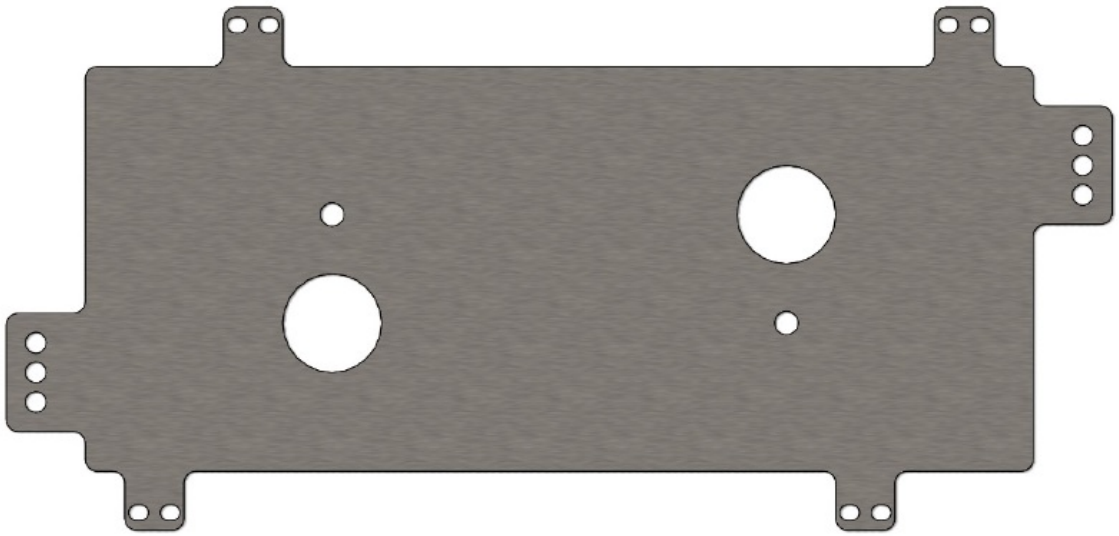


Figure A.1. SolidWorks image of a designed busbar.

The full assembly of the busbar was created in SolidWorks for a verification of dimensions and a graphical representation. The assembly can be seen in Figure A.2 with the capacitors and a insulation sheet of mylar included. A .DWG file with the dimensions of the busbar for production is located on the attached CD [1]. It should be noted that the file is made on a student license and must therefore only be used in accordance to the terms and conditions.

[1] `SolidWorks\Busbar_ plate_ v2.DWG`

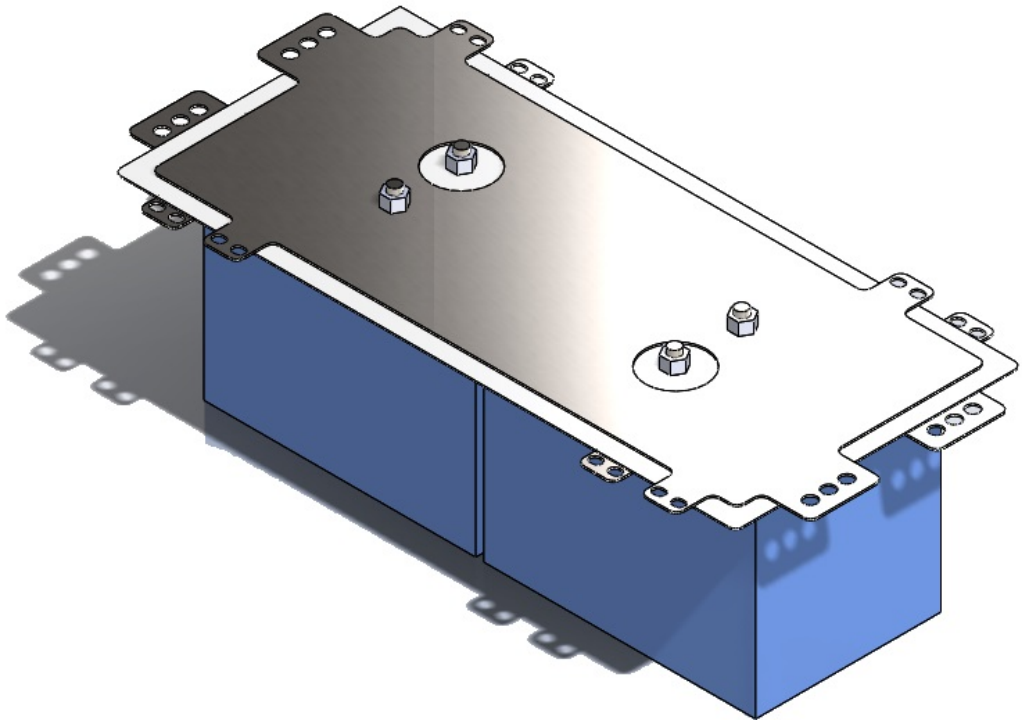


Figure A.2. Busbar assembly in SolidWorks

Appendix B

Protection Board

The two main objectives of the protection board are to ensure discharge of the capacitors if the door to the experimental setup is opened and to disable the PWM pulses if the current limits are exceeded. The protection board is therefore developed to protect the devices used in experimental setup and its operators. The following section will include a description of the main components in the protection board and how the functionality is achieved.

B.1 DC - link discharge

The DC - link discharge is a safety mechanism. The circuit provides remote control of the discharge relay and automatic discharge of the capacitor when the cage for the test setup is open. The reed relay DAT070510[40] used is normally closed meaning if a power failure occurs the capacitors will be discharged. The schematic of the discharge circuit can be seen in Figure B.1. A pull down resistor is placed between the MOSFET gate signal and ground ensuring low gate-source voltage if the DSP is accidentally disconnected.

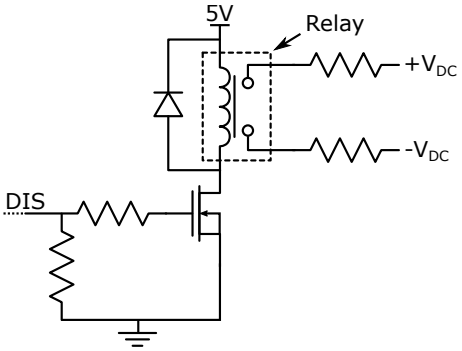


Figure B.1. Schematic of DC - link discharge circuit.

The two parallel connected capacitors [16] will be discharged through bleeding resistors with a series resistance value of 4 $k\Omega$. From the values of capacitance and resistance the time until discharge to 10 V from the full DC link voltage of 5 kV can be calculated as presented in Equation B.1.

$$t_{discharge} = -R \cdot C \cdot ln(\frac{V(t)}{V_0}) = -4k\Omega \cdot 100\mu F \cdot ln(\frac{10V}{5kV}) = 2.49s \tag{B.1}$$

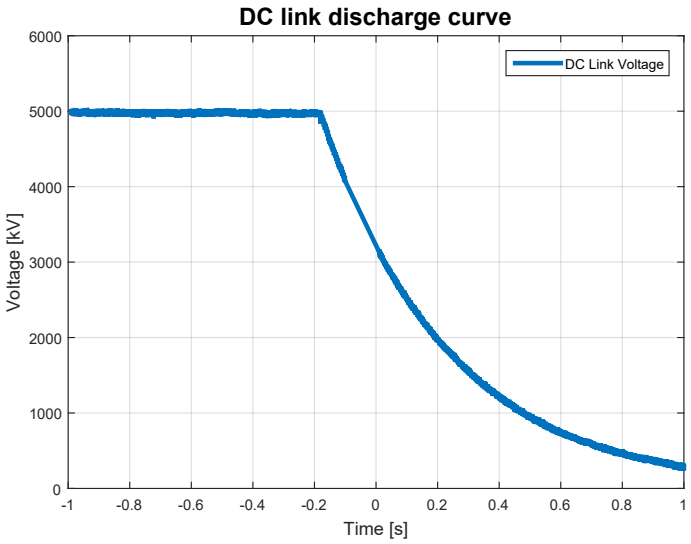


Figure B.2. Discharge curve for DC - link capacitor.

The time until discharge for the DC link is 2.5 s ensuring rapid discharge of the capacitors. before or when the cage is opened. This safety feature provides a protection of the personal operating the experimental setup.

B.2 Over and Under Current Protection

The objective for the current protection is to disable the PWM signal when an over or under current limit is exceeded to protect the equipment from excessive temperatures. PWM is disabled by pulling the signal Q low. The current measurement is converted into a voltage V_{meas} using a LEM current transducer [23] and a sensing resistor. The over and under current references are set by voltage dividers, which are then compared to the measured voltage using an op-amp. The over and under current signals are combined using an AND logic, output of which is connected to a S-R Lacth keeping the signal low until the current limit is not exceeded and the setup has been reset by the operator. The over current schematic is shown in Figure B.3 besides the truth table of the S-R Latch in Table B.2. The current limits were set to $\pm 12A$ and validated experimentally .

The current protection is designed in such a way that if a potential goes low, it will be

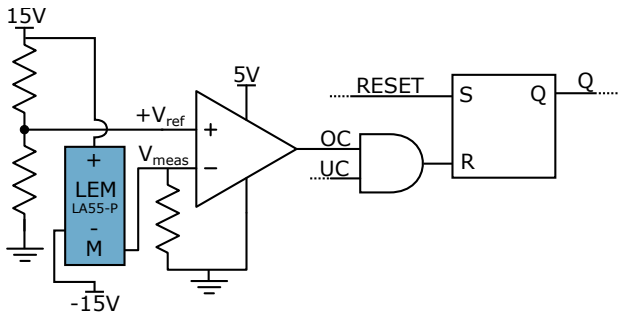


Figure B.3. Principal schematic of over current protection.

S	R	Q
0	0	1
0	1	1
1	0	0
1	1	no change

Table B.1. Truth table of the S-R latch [39]

interpreted as a fault and the PWM signals will be disabled. The output signal Q is used to disable the PWM as will be presented in the following section.

B.3 Optic PWM Generation

Three input signals are utilised for a PWM generation. The first input signal Q is high if no faults are present, the Q is combined in an AND logic with the enable signal (EN) from the DSP outputting the EN_PWM signal. The PWM pulse for each MOSFET is then combined with EN_PWM in a NAND logic sending the signal through an optic transmitter to the gate driver board. The schematic can be seen in Figure B.4.

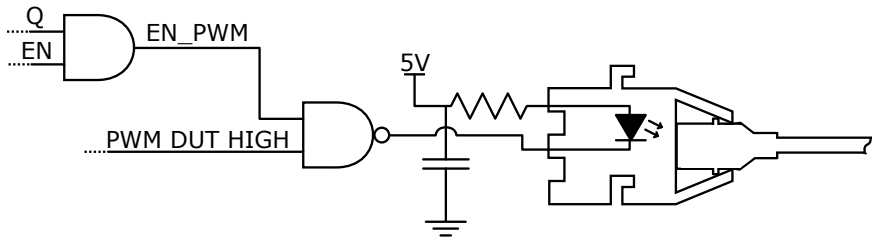


Figure B.4. Schematic of optic PWM generation with fault protection.

The optic fiber link is used to obtain isolation from the DSP to the H-bridge converter. The inversion of the optic signal will be performed at the gate driver IC, ensuring low gate signal in the case of disconnection of an optic cable. The feature is chosen to prevent possible short circuit failures.

Schematic layout for the protection board PCB can be seen in Figure B.5.

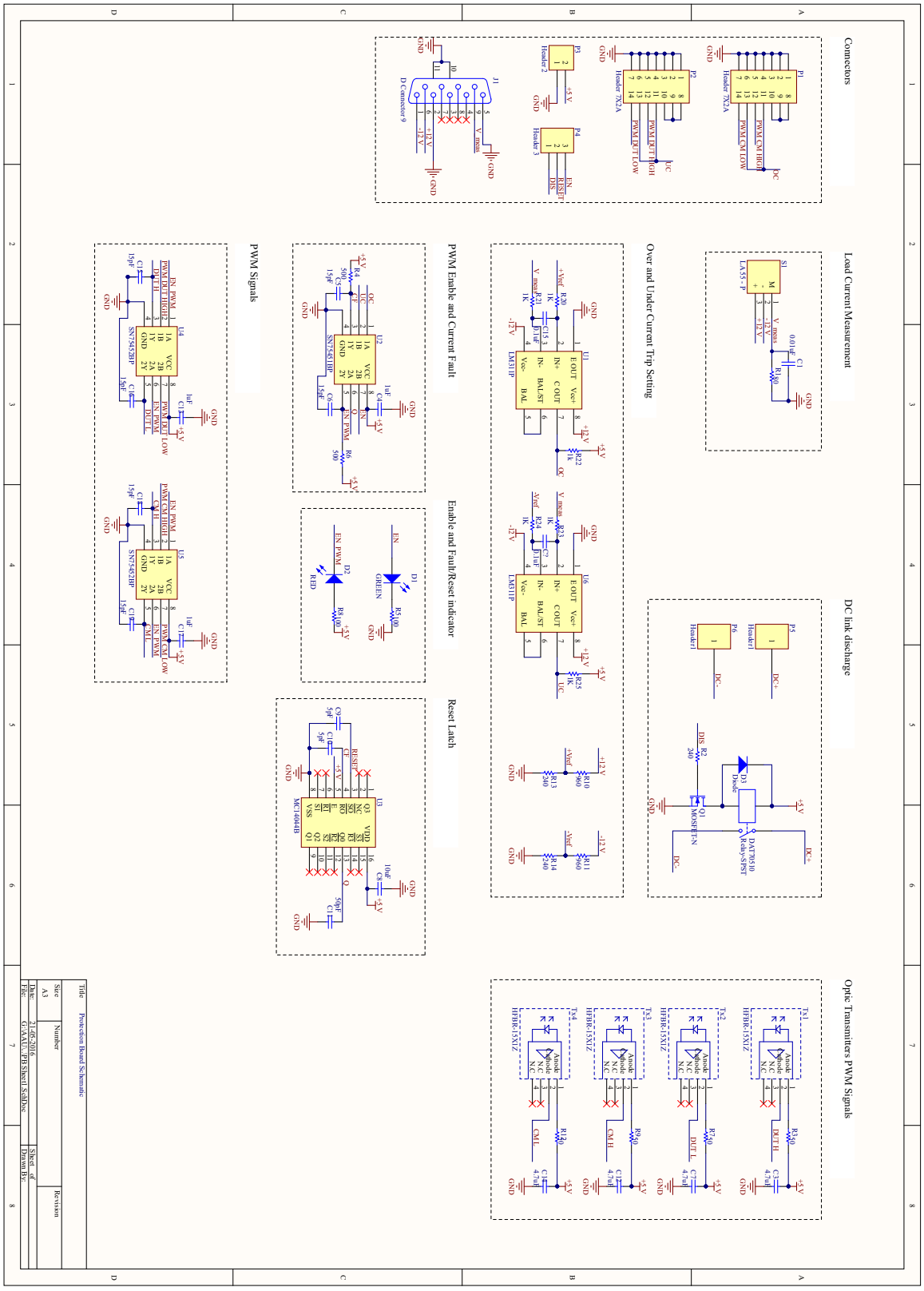


Figure B.5. Schematic of the protection board.

The circuit for protection board is populated on a two layer PCB. Top and bottom view of the protection board PCB can be seen in Figure B.6 and B.7 respectively.

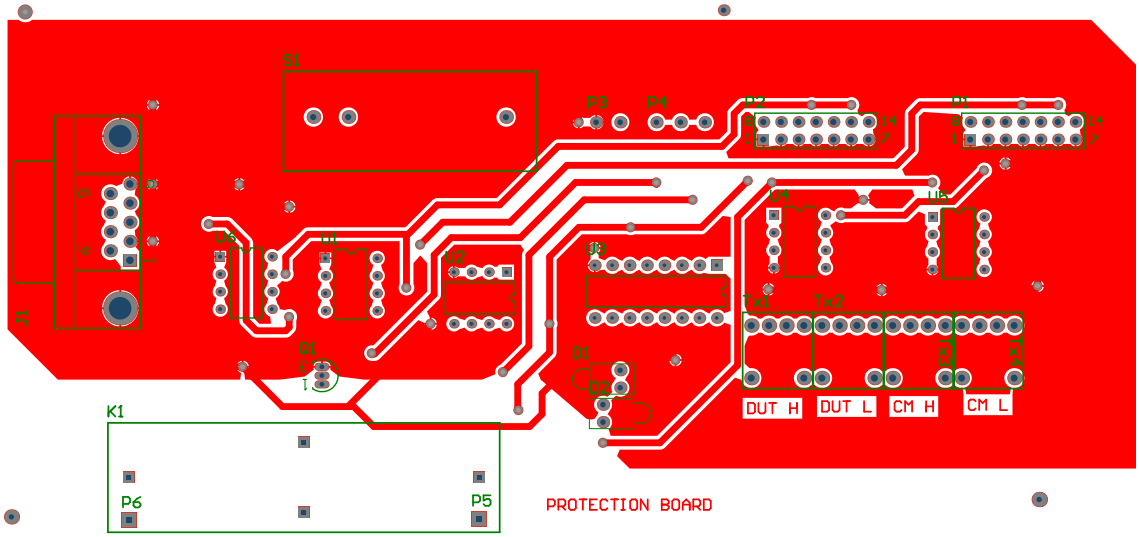


Figure B.6. Top layer - protection board.

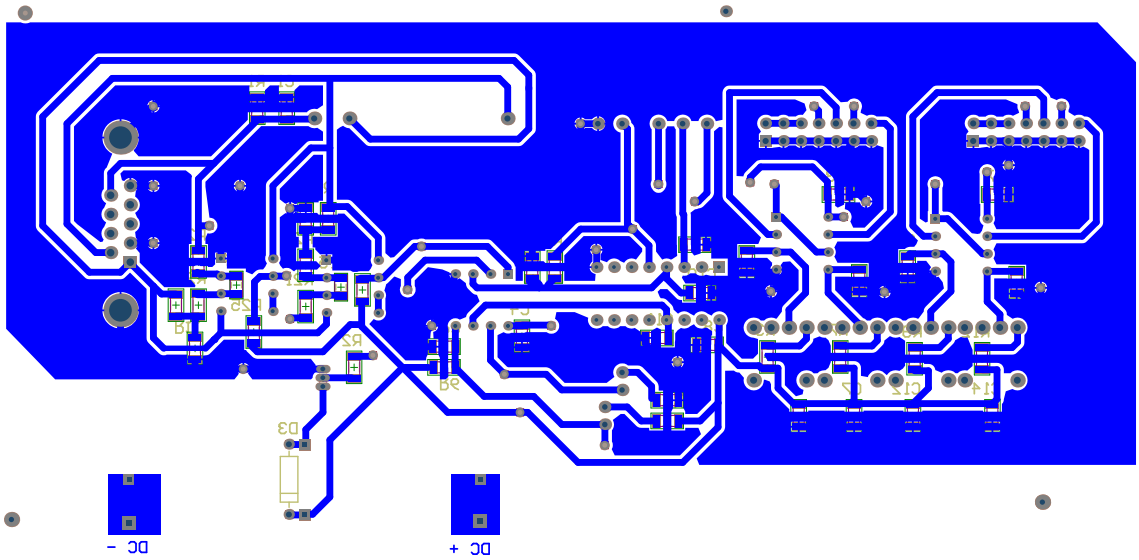


Figure B.7. Bottom layer - protection board.

Schematic of the protection board prepared in Software: Altium Designer is located on the attached CD [1].

[1] \Altium\Protection board

Appendix C

Gate driver

The gate driver PCB incorporating the offline V_{ds} and V_f monitoring circuit was developed for a packaged SiC MOSFET half bridge power module. The following section will include a brief description of the gate driver and reed relay based offline conduction voltage measurement circuit.

C.1 Gate Drive circuit

Figure C.1 shows the schematic of the gate driver circuit. To drive the MOSFET a gate driver IC IXDI614 [12] from IXYS is used. High speed gate driver with fast switching transitions is required when switching power semiconductor device at higher frequencies with a voltage rise/fall time of few hundred of ns. The IXDI614 is an ultra fast inverting gate driver capable to source/sink 14 A of peak current while producing rise/fall times of less than 30 ns. In order to drive SiC MOSFET with Positive gate bias of +19 V and negative gate bias of -4.5 V, the gate driver IC is supplied with +19 V and -4.5 V on VCC and GND pin respectively. Power supply for the gate driver IC is provided by the isolated DC-DC converter. The DC-DC power supply has a dual output voltages of +19 V and -4.5 V and is isolated for 10 kV. Also, the isolation capacitance between the primary and secondary winding is 4.7 pF measured on impedance analyser [41]. A low isolation capacitance is required in order to attenuate the common mode currents in the circuit due to high dv/dt switching transients. Additional DC-DC converter TMA2412D [31] and R-78E5.0 [34] are used to obtain ±12 V and +5 V respectively, which is required for the ADC.

Gate signal from the protection board is then received by an optic receiver on the gate driver circuit board and is then provided to the input pin of the gate driver IC. To isolate the power and control circuit optic fiber links are used. The output of the gate driver IC is connected to the gate of the SiC MOSFET with a 12 Ω of gate resistance. The gate driver circuit board is directly mounted on the power module with gate driver IC and gate resistance placed close to the gate - source terminal of the SiC MOSFET. This will reduce the switching loop inductance by reducing the copper trace length from the gate - source terminal to output pin of the gate driver IC. Decoupling capacitors are placed between the output terminal of the gate driver IC and source.

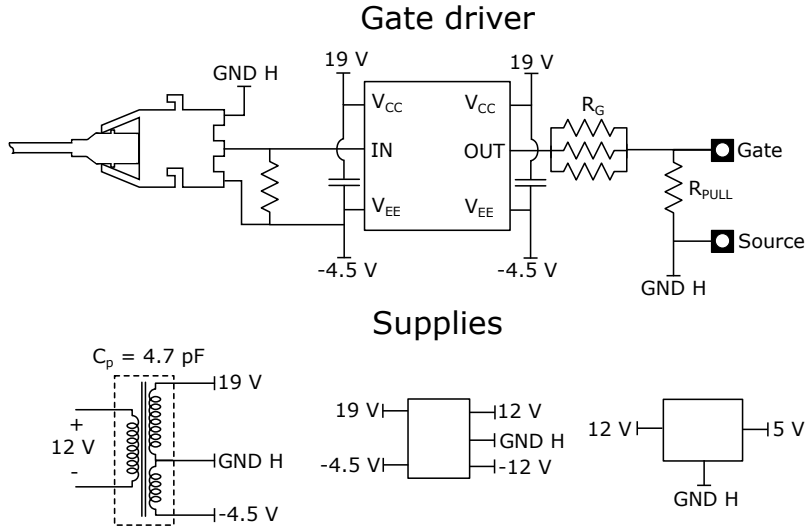


Figure C.1. Schematic of the gate driver circuit

C.2 Measurement Circuit

To measure the on state voltage drop of MOSFETs and forward voltage drop of diode relay based off-line measurement circuit is used. The schematic layout of the measurement circuit is depicted in Figure C.2. The main purpose of the measurement circuit is to measure the on-state device voltage drop and convert the measured analog quantity into the digital domain so that the test data can be used and analysed on later stage. Another objective is to provide isolation between the measurement and the power circuit when MOSFETs/diodes are not conducting and are in blocking state.

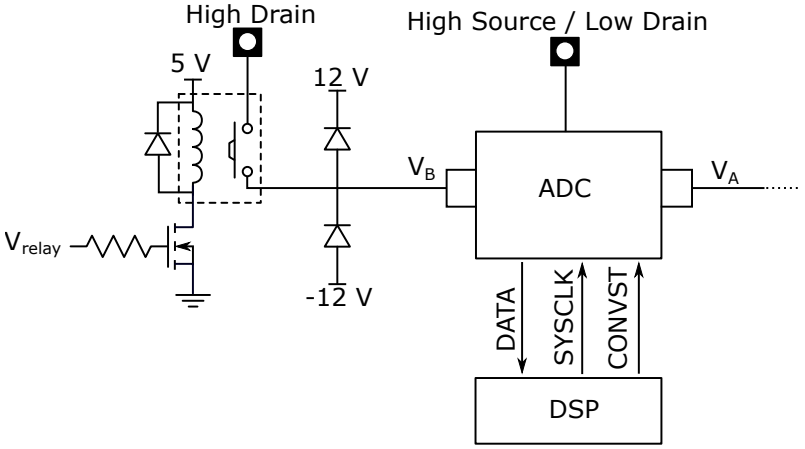


Figure C.2. Schematic of the off-line relay based measurement circuit

To provide the isolation between the power circuit and measurement circuit a reed relay is used. The relay used is DAT70510F [7] providing 10 kV isolation between the two contact terminals and is normally off type. To perform the measurement a 14 - bit ADC AD7367 [11] is used. The ADC is dual channel biolar ADC and is supplied with ±12 V. +5 V for the ADC cores. One of the terminals of the reed relay is connected to the drain of the

HS MOSFET and Analog input channel 1 (AIN1) of the ADC respectively. Whereas, for the low side MOSFET relay is connected between the source and Analog input channel 2 (AIN2) of the ADC. Meaning that measurement for both high side and low side devices in a half bridge is carried out using a dual channel ADC with the midpoint (output terminal) of the half-bridge module being connected to AGND pin of ADC . Conversion start, clock signals and data read is received using the optic link to provide isolation between the control and power circuit. The relay is controlled by connecting a 2N70002 N -channel MOSFET in series with a relay coil. This series connected MOSFET is controlled by gate signals transferred form the DSP through wired connection, as there is no need for isolation due to no physical connection between relay contacts and relay coil.

Schematic layout for the gate driver PCB can be seen in Figure C.3.

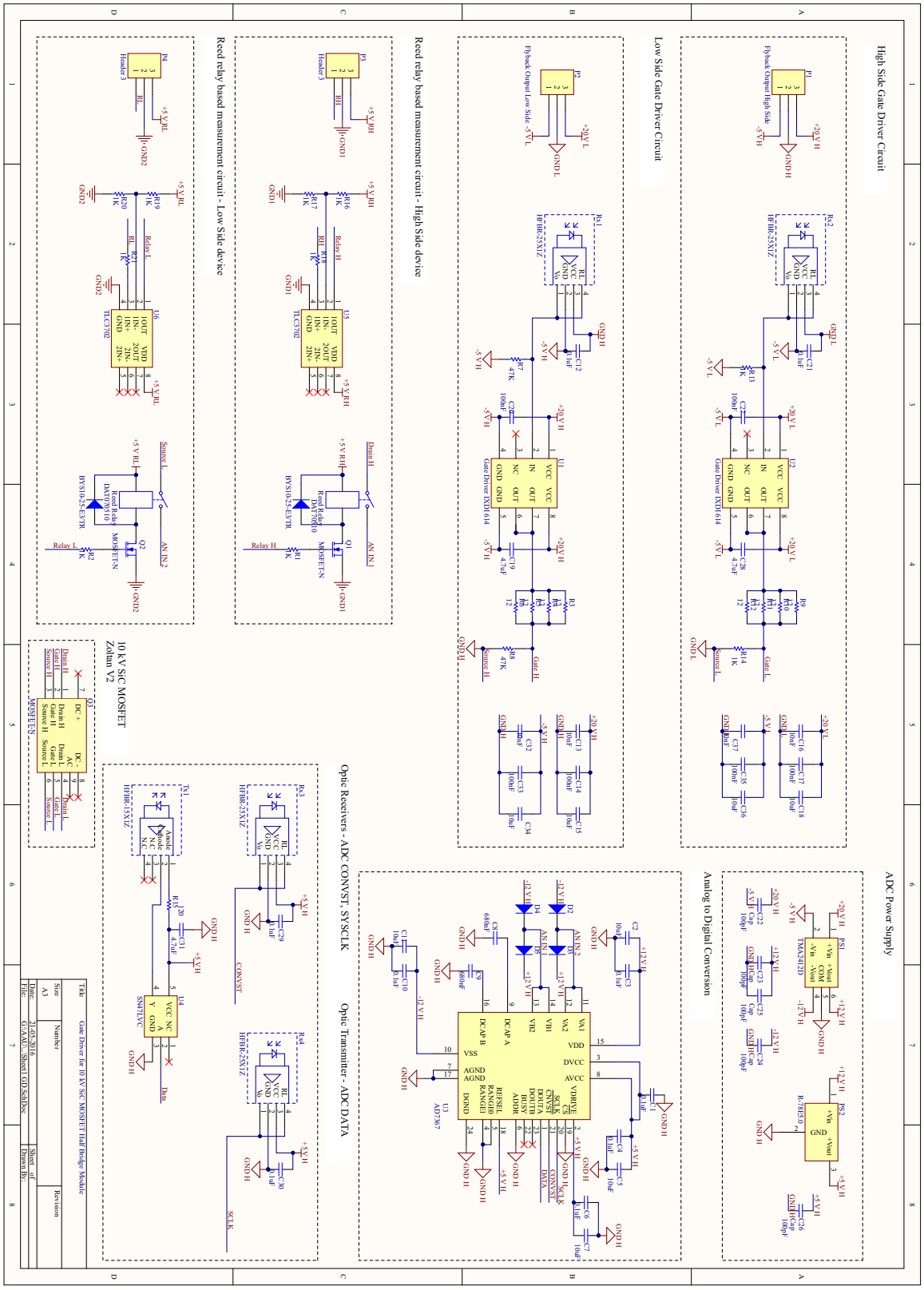


Figure C.3. Schematic of the gate driver circuit.

The gate driver circuit and off-line reed relay based on state voltage monitoring circuit is populated on the two layer PCB. Top and bottom layer of the gate driver PCB can be seen in C.4 and C.5 respectively.

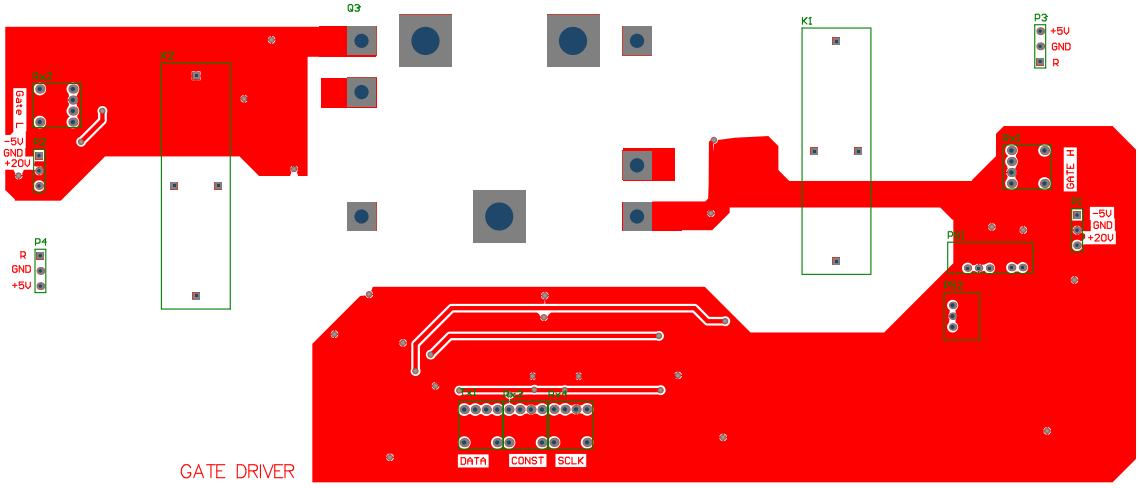


Figure C.4. Top layer - gate driver circuit.

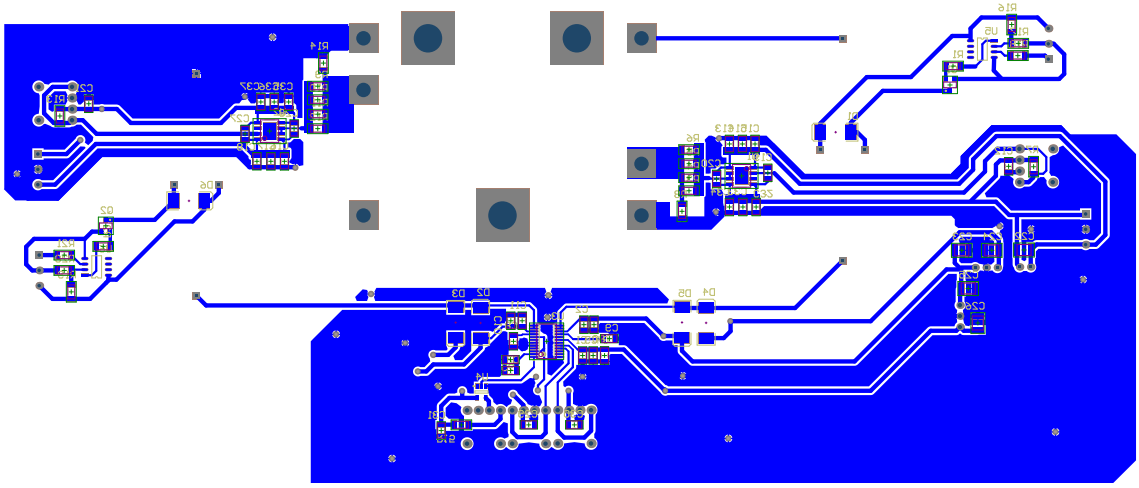


Figure C.5. Bottom layer - gate driver circuit.

Schematic of the gate driver PCB prepared in Software: Altium Designer is located on the attached CD [1].

[1] \Altium\Gate Driver

Appendix D

DSP

Microcontroller used for this project is F28M36PC2 [21] from Texas Instruments. This microcontroller is multicore system on chip unit with an independent communication and real time control subsystem. The communication subsystem is based on the Cortex ARM M3 CPU and real time control subsystem is based on the 32 - bit floating point C28 CPU. Maximum system clock frequency for C28 and M3 is 150 MHz and 125 MHz respectively.

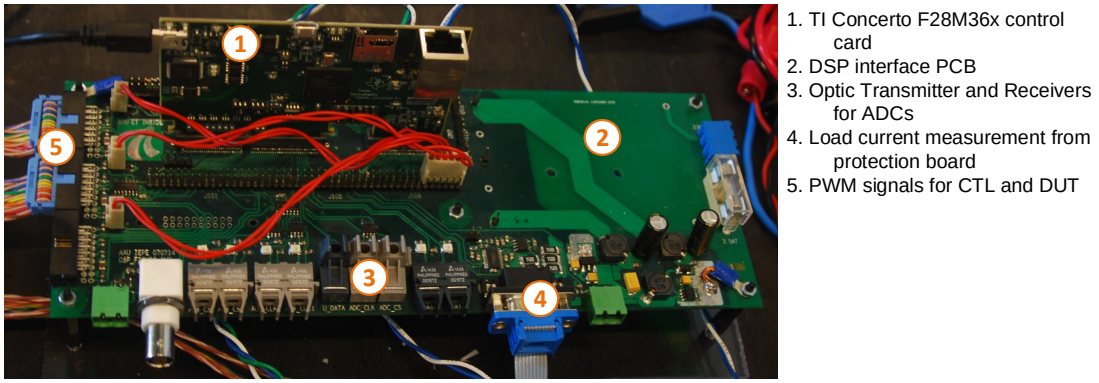


Figure D.1. Texas Instruments F28M36PC2 control card and interface PCB

D.1 C28 Programming

This section presents a brief description regarding DSP implementation of the Current Control, configuration of the ePWM sub module, dead time generation and measurement routine.

D.1.1 Digital implementation of PR Controller

As discussed in Section 2.2 a PR controller is utilised to implement the current control in a power cycle test setup. A discrete form of a PR controller is presented in Equation D.5. Here, input to the controller is an error signal E(k) and output is the control signal U(k).

$$G_c(z) = K_p \cdot \left[1 + \frac{1}{T_r} \frac{\sin(\omega_0 T_{smp})}{2\omega_0} \frac{z^2 - 1}{z^2 - 2z\cos(\omega_0 T_{smp}) + 1}\right] \tag{D.1}$$

Now, obtaining difference equation for a transfer function in Equation D.1 yields,

$$\frac{U(k)}{E(k)} = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{1 - a_1 \cdot z^{-1} - a_2 \cdot z^{-2}} \tag{D.2}$$

Where,

$$b0 = K_p + K_i \cdot \frac{\sin(\omega_0 T_{smp})}{2\omega_0}, b1 = -2 \cdot K_p \cdot \cos(\omega_0 T_{smp}), b2 = K_p - K_i \cdot \frac{\sin(\omega_0 T_{smp})}{2\omega_0}$$

$$a1 = 2 \cdot \cos(\omega_0 T_{smp}), a2 = -1$$

Rewriting EquationD.2 in terms of U(k),

$$U(k) = b_0 E(k) + b_1 E(k) z^{-1} + b_2 E(k) z^{-2} + a_1 U(k) z^{-1} + a_2 U(k) z^{-2} \tag{D.3}$$

In Equation D.3 z^{-n} where n = 0, 1, 2 represents the n^{th} sample before the present sample.

$$U(k) = b_0 E(k) + b_1 E(k-1) + b_2 E(k-2) + a_1 U(k-1) + a_2 U(k-2) \tag{D.4}$$

Based on previous analysis, digital implementation of the current control loop is presented in the Listing D.1.

Listing D.1. Digital implementation of a PR current controller

```
//////////////////////////
// Current Control
//////////////////////////

Theta += fref*TWO_PI*Ts;          // calculate angle, here Ts = 1/fsw/2;
Theta = fmod(Theta, TWO_PI);      // Set angle between 0-two_pi

I_ref = I_M*sin(Theta+I_phase); // Current Reference
I_error =  (I_ref - I_DUT)/vdc; // Controller Input and Vdc Scaling

// PR Controller
ctrl_out = b_zero * I_error + b_one * I_error_old + b_two * I_error_pre
+ a_one * ctrl_out_old + a_two * ctrl_out_pre;
I_error_pre = I_error_old;
I_error_old = I_error;
ctrl_out_pre = ctrl_out_old;
ctrl_out_old = ctrl_out;

DUT_duty = 0.5*vref_buff/vdc*sin(Theta)+0.5;
// DUT has constant duty if Vref_buff = 0
// DUT has Alternating duty if Vref_buff = 1 -> Vdc
CTL_duty = DUT_duty + ctrl_out;

// Dead time compensation
CTL_duty = CTL_duty + sign(I_ref)*Td_comp;   //Td_comp = fsw*T_deadtime
DUT_duty = DUT_duty - sign(I_ref)*Td_comp;
```

D.1.2 Pulse Width Modulation

Pulse Width Modulation (PWM) is performed using an ePWM (Enhanced Pulse Width Modulation) module in the microcontroller. The ePWM peripheral performs the Digital to Analog conversion (DAC), where the analog value is equivalent to the duty cycle. This ePWM module can be setup by configuring sub modules within the ePWM module.

In a PWM, the carrier signal is compared with the control signal which then generates a corresponding high or low signal on a compare event.

In C28 CPU, frequency of the carrier signal is determined by setting up the time based period (TBPRD) register and the mode of the time base counter. Here the time base period counter is set to an Up - Down Count mode.

In an up-down count mode the time base period register value is chosen based on the desired switching frequency and time based clock (T_{BCLK}) [20].

$$T_{sw} = 2 \cdot TBPRD \cdot T_{BCLK} \quad Where, f_{sw} = \frac{1}{T_{sw}} \tag{D.5}$$

$$TBPRD = \frac{T_{sw}}{2 \cdot T_{BCLK}} \quad \Rightarrow \quad TBPRD = \frac{150 \cdot 10^6}{20 \cdot 10^3 \cdot 2}$$

Here, time based clock T_{BCLK} is a pre-scaled version of the system clock frequency SYSCLK. The T_{BCLK} for the C28 CPU is set to be equal to the SYSCLK which is 150 MHz. For, a f_{PWM} = 20 kHz Equation D.5 results in a time based value of 3750 with $T_{BCLK} = \frac{1}{150MHz}$. The sampling is performed twice a period. Once at the beginning and the middle of each switching period to reduce the effect of noise due to switching transients. This corresponds to the instants, when TBPRD = 0 and TBPRD = 3750.

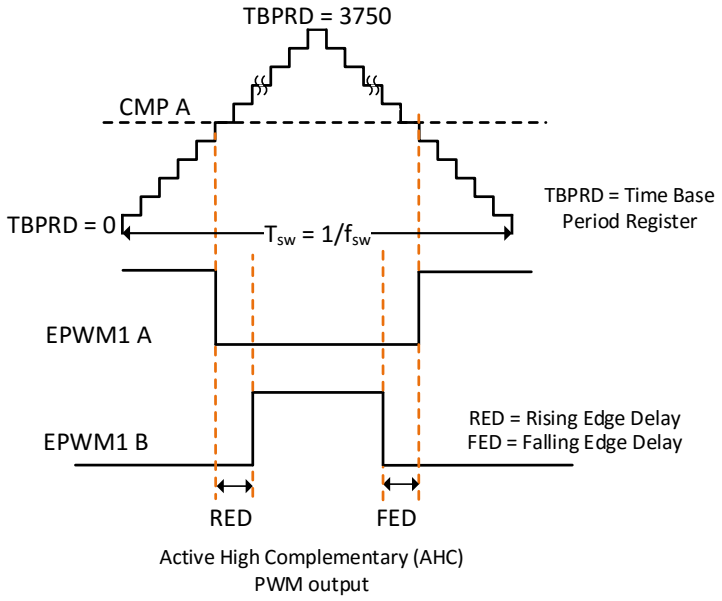


Figure D.2. Pulse Width Modulation

The instantaneous value of the control signal is transferred to the compare (CMPx) register of the Counter-Compare submodule. When the value of time base period register is equal to the value in compare (CMPx) register, the output is set high or low depending on the direction of the counter. In this case the output is set low during the up count and set high during the down count. Meaning that the duty cycle is set by the value in CMPx register and is active high that is, high time is proportional to CMPx value.

As can be seen in Listing D.2 duty control signals for the CTL module which is the output of PR controller and control signal for DUT module. The output is scaled with TBPRD before they can be compared into the CMPx register in the ePWM module. To prevent over modulation control variables are limited within the max - min (3750 - 0) value of TBPRD register. Once the values are transferred, the ePWM outputs a PWM signal based on the instantaneous value of the duty cycle on compare event.

Listing D.2. C code for Pulse Width Modulation

```
CTL_duty = EPWM_TIMER_TBPRD*CTL_duty; // Convert to TBPRD
// Protection (Saturaion Limit Avoids overmodulation)
        if (CTL_duty > EPWM_TIMER_TBPRD) CTL_duty = EPWM_TIMER_TBPRD;
        if (CTL_duty < 0) CTL_duty = 0;

DUT_duty = EPWM_TIMER_TBPRD*DUT_duty; // Convert to TBPRD
// Protection (Saturaion Limit Avoids overmodulation)
        if (DUT_duty > EPWM_TIMER_TBPRD) DUT_duty = EPWM_TIMER_TBPRD;
        if (DUT_duty < 0) DUT_duty = 0;

// LED D2 Blink for visual Control Loop Run State
        if (count_LED++>(FSW)){
                count_LED = 0;
// Toggle LED bit -> C28 control loop - Running
GpioG1DataRegs.GPBTOGGLE.bit.GPIO34 = 1;
```

```
        }

        // Set PWM Duty Cycles for CTL
        EPwm1Regs.CMPA.half.CMPA = (int)(CTL_duty);
        // Set PWM Duty Cycles for DUT
        EPwm2Regs.CMPA.half.CMPA = (int)(DUT_duty);
```

The deadtime between the PWM signals for one leg of an inverter is provided by programming the Dead-Band submodule. The dead band polarity is set as an Active High Complimentary (AHC). The PWM ouput signals for one leg of an inverter in an AHC configuration are depicted in Figure D.2. In the figure the rising edge delay (RED) and falling edge delay (FED) can be set independently by programming the DBFED and DBRED registers of the Dead-Band submodule. These DBRED and DBFED registers and their value determines the number of time base clock period TBCLK a signal edge is delayed by [19]. The DBFED and DBRED are programmed to set the RED and FED (deadtime) of 1 μs.

$$FED = DBFED \cdot T_{TBCLK} \qquad RED = DBRED \cdot T_{TBCLK} \tag{D.6}$$

Equation D.6 yields DBFED and DBRED value of 150 for $T_{TBCLK} = \frac{1}{150MHz}$, FED = RED = 1 μs.

As discussed before the PWM is configured in Active High Complimentary mode with carrier frequency of 20 kHz and deadtime of 1μs. An example of configuration of one of the ePWM submodule is presented in Listing D.3.

Listing D.3. C script for ePWM configuration

```
        void Init_EPwm1()
{
        // Time base registers
        EPwm1Regs.TBPRD = EPWM_TIMER_TBPRD; // Set the timer period
        EPwm1Regs.TBPHS.half.TBPHS = 0;      // Set Phase register to zero
        EPwm1Regs.TBCTR = 0;                  // clear TB counter

        EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN; //Symmetrical Up Down Counter
        EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;         //Phase loading disabled
        EPwm1Regs.TBCTL.bit.PRDLD = TB_IMMEDIATE;   //Immediate load of duty cycle
        EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO;    //Sync down-stram module
        EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;       //TBCLK = SYSCLK (150 MHz)
        EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;

        // Set up shadow register and load mode
        EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
        EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO_PRD; //load on CTR = Zero and
                                                  //CTR = PRD (double update)

        // Set compare values
        EPwm1Regs.CMPA.half.CMPA = EPWM_TIMER_TBPRD/2; // Half of time base period
        // Set actions
        EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR; // Clear at Up Count, on compare event
        EPwm1Regs.AQCTLA.bit.CAD = AQ_SET;   // Set at Down Count, on compare event

        // Setup deadband
         EPwm1Regs.DBCTL.bit.OUT_MODE = DB_FULL_ENABLE; // Dead band fully enabled
                                                 (i.e. Both RED and FED active)
         EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;// Active High Complementary
```

```
        EPwm1Regs.DBCTL.bit.IN_MODE = DBA_ALL;
        EPwm1Regs.DBRED = EPWMLDB;
        EPwm1Regs.DBFED = EPWMLDB;

        // Setup triggers for ADC interrupt in Zero (only by EPwm1)
        // Generate two interrupts during a switching period (double update)
        // Set SOCA for ADC during Zero event
        EPwm1Regs.ETSEL.bit.SOCAEN  = 1;        // Enable SOCA
        EPwm1Regs.ETSEL.bit.SOCASEL = ET_CTR_ZERO;    // Select SOCA on Zero event
                                                      //(TBCTR = 0x0000)
        EPwm1Regs.ETPS.bit.SOCAPRD  = 1;       // Generate interrupt on each period

        // Set SOCB for ADC during Max event
        EPwm1Regs.ETSEL.bit.SOCBEN  = 1;        // Enable SOCB
        EPwm1Regs.ETSEL.bit.SOCBSEL = ET_CTR_PRD; // Select SOCB on MAX event
                                                  //(TBCTR = TBPRD)
        EPwm1Regs.ETPS.bit.SOCBPRD  = 1;  // Generate interrupt on each period
}
```

D.1.3 Measurement Routine

The offline reed relay based conduction voltage measurement technique and measurement routine is presented in Section 2.5. Now, implementation of measurement routine in the DSP is presented in this section.

The timer is set inside the ADC interrupt generated twice a switching period and keeps tracks of time (seconds, minutes, hours). In the interrupt when the time is matched with predetermined time value, the variable Measurement_Routine in Listing D.4 is set to one. The code for the measurement routine is placed in an infinite loop which checks for this condition continuously. As soon as the condition is met the power cycling operation is halted and measurement routine is initiated. Before initialization of the measurement routine the PWM ports are changed to general purpose output ports. All the output pins are pulled low which will ensure the MOSFETs in a converter are turned off before initializing the routine. C code showing one of the measurement routine is presented in Listing D.4 with necessary comments. First CTL HS and DUT LS MOSFETs are turned on for the time equal to the ramp up period. After the ramp up period the DUT LS MOSFET is turned off, corresponding relays are turned on after delay a of 1 μs. As can be seen in the code, before the read operation is performed a ADC delay of 3 ms is provided in between. This time corresponds to the operate time of the relay which is approximately 3 ms with a diode fitted relay [7]. Once relays are turned on the conversion start and read operation is performed on the ADC. This operation is performed for 20 samples. These 20 measurements taken during the free-wheeling period are averaged and stored into the buffer. After this operation the relays are turned off. A delay of 3 ms is provide before the turn on of CTL HS MOSFET is initiated. This delay corresponds to the release time, which is approximately 2 ms [7]. The measurement data is transferred to M3 processor at the end of measurement routine. The data is then displayed on a LabVIEW interface. Data transfer between PC and LabVIEW uses USB serial communication.

Listing D.4. C code implementation of measurement routine

```
        if (Measure_Routine == 1){
        PWM_Disable(); // disable PWM

        // intialize pwm pins as gpios
```

```
DSP28x_usDelay((Uint32)(30*1-6));
ePWM1toGPIO();
ePWM2toGPIO();

// Clear all PWM ports (Safety Precautions)
CTL_HIGH_OFF();
CTL_LOW_OFF();
DUT_HIGH_OFF();
DUT_LOW_OFF();

// Wait for current to fall
Delay_ms(5000); //delay of 5s

//////////////////
// CTL HS - DUT HD //          (CTL High Switch - DUT High Diode)
//////////////////
// Ramp current

CTL_HIGH_ON(); // Turn on CTL HS
DUT_LOW_ON();  // Turn on DUT LS
Delay_us((Uint32)ramptime_us);  // ramptime = L*di/Vdc
DUT_LOW_OFF(); // Turn off DUT LS
// Delay for relay
Delay_us((Uint32)relay_delay);
// Turn on measurement relays
MEASURERELAYCTL_HIGH_ON();
MEASURERELAYDUT_HIGH_ON();
Delay_ms(3);  // Wait 3 ms for relays to turn on

// Acquier a fast series of samples
for (sample_count=0;sample_count<SAMPLESIZE;sample_count++){
// Measure on state voltages
SampleDataADCs();
ReadSerialADCs(); // VA
I_Meas1Buf[sample_count] = Scale_Current_Measurement(I_ADC_Buffer_DUT);

ReadSerialADCs(); // VB
CTL_VdsHighBuf[sample_count] = Scale_Vds_Measurement(Vds_ADC_Buffer_CTL);
DUT_VfHighBuf[sample_count] = Scale_Vds_Measurement(ADC_Buffer_DUT);
        }

I_Meas1 = average(I_Meas1Buf);
CTL_VdsHigh = average(CTL_VdsHighBuf);
DUT_VfHigh = average(DUT_VfHighBuf);

// Turn off measurement relays.
MEASURERELAYCTL_HIGH_OFF();
MEASURERELAYDUT_HIGH_OFF();
Delay_ms(3); // Wait 3 ms for relays to turn on

// Turn off CTL HS
CTL_HIGH_OFF();

// Wait for current to fall
Delay_ms(10); // Delay of 10 ms
```

D.2 M3 Programming

M3 processor is programmed to handle the data transfer with LabVIEW interface via serial communication. This serial communication uses USB protocol and configured using a Universal Asynchronous Transmitter/Receiver (UART) module available in M3 processor.

The UART configuration used is: Baud rate = 115200, data length of 8 bits, one stop bit, no parity and base port address = zero(UART0) [22]. C code for UART configuration is presented in Listing D.5

Listing D.5. C code for UART configuration

```
// Configure UART0 for USB communication
//(Baud rate = 115200, Data Bits = 8, Stop bits = 1, Parity = None)
UARTConfigSetExpClk(UART0_BASE, SysCtlClockGet(SYSTEM_CLOCK_SPEED), 115200,
  (UART_CONFIG_WLEN_8 | UART_CONFIG_STOP_ONE | UART_CONFIG_PAR_NONE));
```

The UART module consists of two 16 entry FIFOs: one for transmit and one for receive respectively. C code for enabling transmit and receive interrupts for base port (PORT0) is presented in Listing D.6.

Listing D.6. While loop to check for the data received

```
// Enable UART0 interrupt
IntRegister(INT_UART0, UART0IntHandler);
IntEnable(INT_UART0);
UARTIntEnable(UART0_BASE, UART_INT_RX | UART_INT_RT);
```

A UARTCharsAvail() function in while loop as presented in Listing D.7 continuously checks for the data received on the receive FIFO at given base port address. This data is sent in the form of an array of characters from the LabVIEW interface. When data is available CPU enters the while loop where function UARTCharNonBlocking() reads a character from the receive FIFO for specified port. Received data is stored in a variable UART_read_data[ ] defined as datatype char.

Listing D.7. C code for enabling transmit and recieve interrupt

```
while(UARTCharsAvail(UART0_BASE))
{
    UART_read_data[UART_datashifter++] = UARTCharGetNonBlocking(UART0_BASE);
}
```

The array of characters is then compared to the predefined string in M3 C code. Whenever the condition is met for the compare event, specific action is initiated. For example upon receiving a string 'RUN', M3 will set a flag on a memory location shared between C28 and M3 CPUs. When flag is set by M3, C28 will enter the control loop and initiate power cycling test.

For example when a string of a character RUN\n is received from LabVIEW, the condition for if loop execution presented in Listing D.8 will be true. In LabVIEW program \n at the end of a string indicates a null termination determining the last visible character of that particular string. Comparison of string is performed using a function strncmp(). This function compares two strings from which, one of the string is the data read from the USB and another is a predefined string in M3. Function sizeof() will return the number of elements in an array by taking size of an entire array and dividing it by the size of a single element. The memeset() function will set each character in the array to zero and flag is set before it exits the If loop.

Listing D.8. C code example of string comparison

```
// Is buffered data == "RUN\n"?
```

```
if(strncmp(UART_read_data,MSG_RUN,sizeof(MSG_RUN) / sizeof(MSG_RUN[0])) == 0)
{ memset(&UART_read_data[0], 0, sizeof(UART_read_data)
    / sizeof(UART_read_data[0]));
    UART_datashifter = 0;
    M3_to_C28_Start[0] = 1;
    }
```

Similarly, other strings such as 'OPENRELAY', 'CLOSERELAY', 'STOP', 'RESET-LATCH' will initiate the opening/closing of discharge relay, running and halting power cycle test and reset the latch on the protection board respectively. This was the communication from LabVIEW interface to M3.

M3 to LabVIEW communication includes: conduction voltage measurement data transfer at the end of each measuring routine. These data consists of on-state conduction voltages for the DUT and CTL module and time of measurement. It also sends overCurrent and underCurrent fault indication to the LabVIEW interface based on the logic state of the GPIO ports connected to OC and UC signals on protection board. To assure that a LabVIEW and DSP communication is not interrupted a string 'PING' and 'PONG' is exchanged at interval of 30 seconds. If M3 does not receive the string 'PONG' from LabVIEW within 90 seconds power cycling will be halted.

To write the data on UART a printf() function is ude. C code example for sending a OC and UC are lsited in Lsiting D.9.

Listing D.9. Writting data on UART

```
// Overcurrent send
if (C28_to_M3_OC[0] == 1 && send_OC == 1){
        UARTprintf("OC");
        send_OC = 0;
}
if (C28_to_M3_OC[0] == 0)        send_OC = 1;

// Undercurrent send
if (C28_to_M3_UC[0] == 1 && send_UC == 1){
        UARTprintf("UC");
        send_UC = 0;
}
```

DSP C code programming files compatible with Code Composer Studio 6.1.0 software is located on the CD [1].

D.3 Communication Overview

A functional diagram and flowchart of LabVIEW program is presented in Section 3.4. In this section a brief description regarding communication protocol used in the LabVIEW interface are presented.

D.3.1 USB communication: LabVIEW - DSP

Serial communication for the LabVIEW interface is configured using a VISA (Virtual instrument Software Architecture). LabVIEW - VISA palettes can be configured

[1] \DSP

to communicate with instrument buses including USB and Ethernet communication. Screenshot of USB communication setup in LabVIEW is presented in Figure D.3.

It can be seen in the Figure D.3, similar configuration for the USB protocol as shown in the Appendix D.2 in DSP code is used (Baud rate = 115200, data bits = 8, stop bits = 1 and parity = none). In the VISA resource name field the user should specify USB communication port of the PC on which the LabVIEW interface is running. This can be done using the dropdown list on the user interface front panel. LabVIEW continuously checks for the available data at the port in a while loop. When the data is available a program enters into a case structure. Once a program enters into the case structure a sequence presented in a LabVIEW flow diagram - Figure 3.11 is executed.

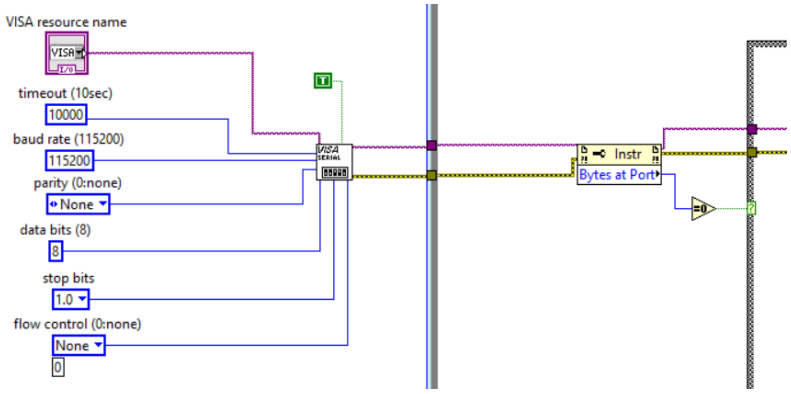


Figure D.3. Configuration of USB communication in LabVIEW

D.3.2 Ethernet communication: LabVIEW DC - Link power supply

An Ethernet communication is used to control DC-Link Power Supply. A LabVIEW driver library available from the power supply the manufacturer is used to establish communication and control of the power supply.

A screen shot of the communication setup for the Power Supply is presented in Figure D.4. In the VISA resource name field the user can specify the TCP/IP address of the Power Supply. This can be done using the drop-down list on the UI front panel. The three yellow palates are the intialization, reset control and over current/under current protection for the power supply. Once the connection to the power supply is established, the program will enter a while loop and executes the case structures as presented in Figure 3.11 LabVIEW program flow diagram.

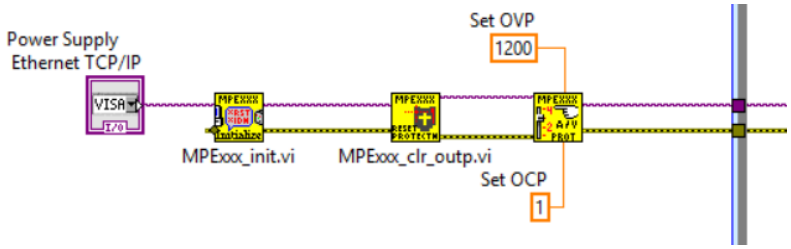


Figure D.4. Configuration of Ethernet Communication in LabVIEW for DC - Link Power Supply

D.3.3 Email server setup

An email service in user interface is configured using SMTP Email VI available in LabVIEW. A screen shot of the email setup is presented in Figure D.5.

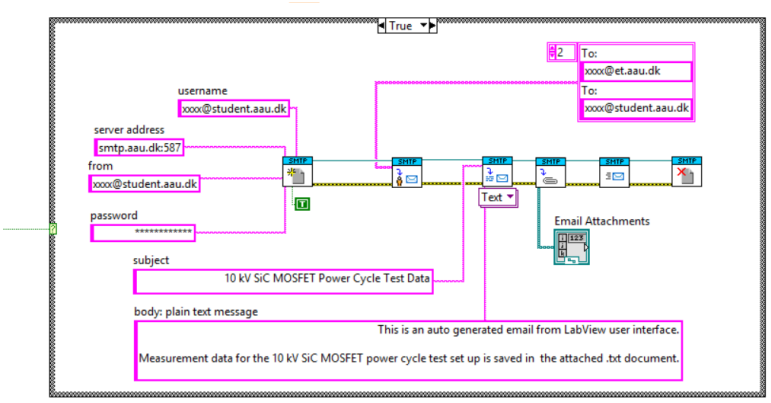


Figure D.5. Configuration for Email in LabVIEW

In this case the email service is configured using an AAU email SMTP server. The user can specify an attachment to the email using the interface front panel. LabVIEW will execute the case structure at every predefined time interval set and an email will be sent to the user with an attachment consisting measurement data.

LabVIEW program for the test set-up user interface is located on the CD [2].

[2] \LabVIEW\10kV Power Cycle.vi

Appendix E

Poster

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Power Cycle Test Bench for Accelerated Life Testing of 10 kV SiC MOSFETs

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IEPE Workshop: June 1-2, 2016

Test – Bench Overview:

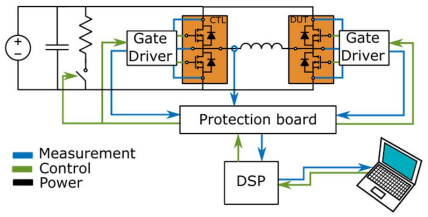

Fig. 1: Power cycle test-bench with an overview of power circuit and control signals
* CTL / DUT – 10 kV SiC MOSFET half bridge module with / without external SiC JBS diode

Abstract:

SiC MOSFET manufacturing process are different compared to their Si counterparts and limited application related experience is available for medium voltage SiC MOSFETs. A necessity for investigating the defect growth and failure modes in an application relevant environment arises. A power cycling test-bench has therefore been designed to expose SiC module to temperature swings during AC operation at medium voltages. A detailed infant characterization of the SiC modules are performed for post mortem fault behaviour investigation. During power cycling the conduction voltages of the SiC MOSFETs and diodes are measured for monitoring degradation and used as a state of health indicator. Die surface temperatures are monitored using fiber optics for an identification of the mean temperature and temperature swings.

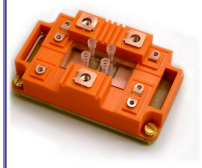

Fig. 2: 10 kV SiC MOSFET Half bridge Power Module, made by CHU, SBE.

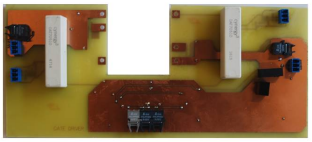

Fig. 3: Gate driver for SiC MOSFET Half bridge power module.

Fig. 4: DC –DC isolated power supply with dual o/p voltages

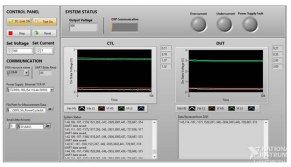

Fig. 5: LabVIEW user interface

Infant Device Characterization:

- Characterization of the power module before the accelerated life testing will be analyzed to later identify fault behavior and drift in parameters.

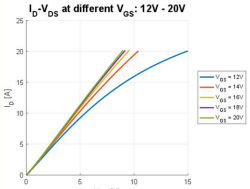

Fig. 6: I-V Characterisitcs for determining on-state resistnace

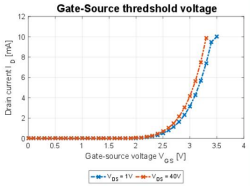

Fig. 7: Gate-Source threshold voltage

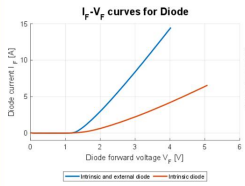

Fig. 8: Forward characterisitic for MOSFET intirinsic and external 10 kV JBS diode

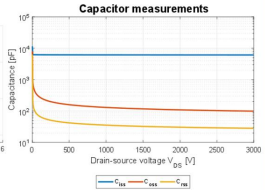

Fig. 9: Capacitance measurements of MOSFET in packaged power module

Test-Bench Verification:

- Experimental verification of controller and test bench at low power.
- Measured device conduction voltages during power cycling using an offline relay based measurement technique.

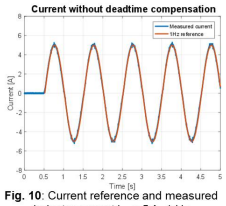

Fig. 10: Current reference and measured inductor current I_{pk} = 5 A, 1 Hz

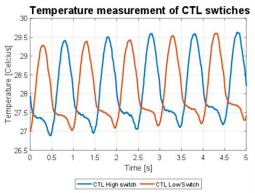

Fig. 11: MOSFET temperature swings during power cycling for module with external diode

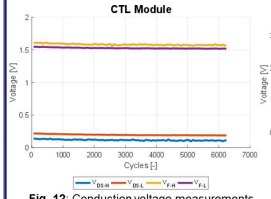

Fig. 12: Conduction voltage measurements - CTL module

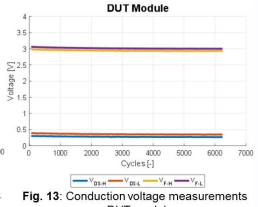

Fig. 13: Conduction voltage measurements – DUT module

Status & Future Challenges:

- Infant device characterization and experimental validation of designed power cycle test-bench is performed. An accelerated life testing will be carried out with aim to investigate the reliability of Gen.1 and Gen.3 - 10 kV SiC MOSFETs intrinsic diode.
- Test bench DC link voltage is currently being gradually raised while monitoring temperature swings and mean temperature to determine the operating point. Test up to 1 kV and peak current of 5 A has been performed.

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Appendix F

Attached CD

The attached CD contains essential files used in the project. The following table lists the most important files, and are sorted by the program used to open them.

Simulation-files	**Filepath**
Current stress distribution	\PLECS\stress_distribution.plecs
Testbench with control	\PLECS\power_cycling_discrete.plecs
Schematic-files	**Filepath**
Protection Board	\Altium\Protection board
Gate Driver	\Altium\Gate Driver
SolidWorks-files	**Filepath**
Busbar	\SolidWorks\Busbar_ plate_ v2.DWG
Additional-files	
	Filepath
DSP Code	\DSP
LabVIEW interface	\LabVIEW\10kV Power Cycle.vi
Poster	\Poster.pdf

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