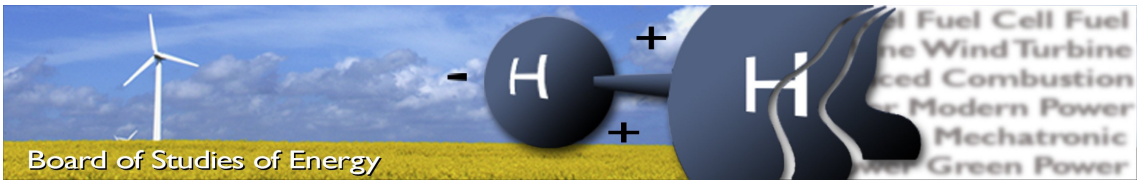
Master's Thesis

Power Supply Prototype using SiC MOSFETs for Energization of Electrostatic Precipitators

Asger Bjørn Jørgensen
Simon Dyhr Sønderskov

Master of Science (M.Sc.) in Engineering
Power Electronics and Drives
School of Engineering and Science
Aalborg University
June 1st 2016



Title:	Power supply prototype using SiC MOSFETs for energization of electrostatic precipitators
Semester:	10th semester
Project period:	February 2nd - June 1st, 2016
ECTS:	30
Supervisors:	Szymon Beczkowski and Benoît Bidoggia
Project group:	PED4-1045

Asger Bjørn Jørgensen

Simon Dyhr Sønderskov

Copies:	6
Pages:	119
Appendix:	A - G
Supplements:	Attached CD

Abstract

Electrostatic precipitators (ESPs) are used in industrial processes to remove particles from fumes. They require high-voltage power supplies. The commonly adopted technologies are based on silicon thyristor or IGBT switching sets. The emergence of Silicon Carbide (SiC) offers potential benefits in the power supply design for ESPs. The synchronous boost converter topology is chosen, and by operation in discontinuous conduction mode (DCM) turn-on losses are eliminated. The topology requires voltage balancing of series connected SiC MOSFETs, for which only limited research currently exists. Many serialization techniques turn on/off all switches simultaneously. The fast switching and high blocking voltages of SiC devices, tend to cause overshoot, ringing and difficulty in voltage balancing. A circuit structure is chosen which features a cascaded switching sequence. The circuit is designed using a modular layout and is tested in the laboratory in a double pulse test. Compared with existing research, the number of series connected devices is extended and voltage balancing is improved. However, during DCM operation with a switching frequency of 50 kHz, the voltage balancing of the circuit is degraded. The origin of voltage imbalances is investigated and future improvements are suggested.

By signing this document, each member of the group confirms that all group members have participated in the project work, and thereby all members are collectively liable for the contents of the report. Furthermore, all group members confirm that the report does not include plagiarism.

Preface

This report is written by Asger Bjørn Jørgensen and Simon Dyhr Sønderskov. It is submitted as the Master thesis for the M.Sc. in Energy Engineering with a specialization in Power Electronics and Drives at the School of Enginering and Science, Aalborg University. The work presented in the report has been carried out during the period from the 2nd of February to the 1st of June, 2016. The project is supervised by Szymon Beczkowski (Associate Professor, Department of Energy Technology, Aalborg University) and Benoît Bidoggia (Electrical R&D Engineer, FLSmidth Airtech A/S).

Reading Guide

The report is divided into 9 chapters and 6 appendices. Figures, tables and equations are numbered by chapter, thus Figure 2.1 denotes the first figure of the second chapter. Equations are denoted in parentheses, i.e. (2.2) is referring to the second equation of Chapter 2.

Literature is cited using the Harvard method, which lists the author followed by the year of publication. All references are listed alphabetically by author in the Bibliography in the end of the report.

The attached CD contains a digital version of this report as well as relevant simulation models, test measurements and other material. When referring to a file located on the CD, the image "  " is used. The CD path for the file is written in a footnote on the same page. If this is a digital version of the thesis, the CD content may be found in the attached .zip file.

Contents

Summary **v**

Table of Symbols **viii**

Table of Abbreviations **ix**

1 Introduction **1**
1.1 Operation of ESPs . . . 2
1.2 Traditional ESP energization . . . 6
1.3 Emergence of wide band gap devices . . . 7

2 Problem statement **9**
2.1 Objectives . . . 9
2.2 Resources . . . 9
2.3 Outline . . . 10

3 Converter Topology and Operating Modes **11**
3.1 Topology . . . 11
3.2 Operating Point . . . 17
3.3 Control Strategy . . . 22

4 Series Connection of SiC MOSFETs **27**
4.1 Methods for series connection of devices . . . 27
4.2 Selection of method . . . 32
4.3 Analysis of gate drive operation . . . 32
4.4 Simulation and RCD-selection . . . 34

5 PCB Development and Test Setup Design **39**
5.1 Design for modularity . . . 39
5.2 Gate drive supply . . . 41
5.3 Description of test setup . . . 43

6 Double Pulse Test Results **47**
6.1 Analysis of switching transients . . . 47
6.2 Improving switching speed . . . 51

7 Voltage Balancing during Converter Operation **59**
7.1 DCM operation test results . . . 60
7.2 Improving voltage balancing . . . 63
7.3 Final results . . . 64

8 Discussion **69**

9 Conclusion **71**

Bibliography **73**

A Losses **77**
A.1 Continuous Conduction Mode Zero (CCM_0) 77
A.2 Positive Discontinuous Conduction Mode (DCM_+) 81

B Control Derivation **83**
B.1 Continuous Time Transfer Function 83
B.2 Controller Design 85
B.3 PLECS Simulation 87

C LabVIEW Description **89**
C.1 Programming of FPGA 90
C.2 Power supply control 92

D PCB Schematics **95**

E PCB Layouts **105**

F Poster **115**

G CD Attachment **119**

Summary

Electrostatic precipitators (ESPs) are used in industrial processes to remove particles from fumes. ESPs offer effective filtering for the largest range of particle sizes, have low pressure loss and work equally well for wet and dry conditions. High-voltage power supplies are used for energization of ESPs. The commonly adopted technologies are based on Silicon (Si) thyristor or IGBT switching sets. The emergence of Silicon Carbide (SiC) MOSFET devices offer potential advantages in power supplies used for operation of ESPs, compared with current Si solutions. Faster switching time and reduced losses allows for higher switching frequencies, enabling faster voltage recovery in the event of sparking. A power supply prototype using series-connected SiC MOSFETs is designed and tested.

The synchronous boost topology allows for bidirectional power flow, using a minimum amount of components. The synchronous boost topology is analyzed and the losses in its semiconducting devices are evaluated for several commercially available SiC MOSFETs. Operating the synchronous boost converter in discontinuous conduction mode (DCM) eliminates turn-on losses. A control structure which combines operating modes to maintain bidirectional power flow is presented and simulated in PLECS.

The topology requires voltage balancing of series connected SiC MOSFETs, for which only limited research currently exists. Many serialization techniques turn on/off all switches simultaneously. The high voltage ratings and fast switching speeds of SiC MOSFETs pose additional issues to the circuit design. Larger values of $\mathrm{d}v/\mathrm{d}t$ introduce higher amounts of voltage overshoot and ringing. A circuit structure is chosen which features a cascaded switching sequence.

A laboratory setup is build for testing the string of series connected SiC MOSFETs in a double pulse test. The setup is operated by a NI cRIO-9030, remotely controlled from a host PC running LabVIEW. The double pulse test shows good transient response, no overshoot and good voltage balancing during turn on/off of four series connected SiC MOSFETs. This performance comes at the cost of increased switching time. Modifications to decrease switching time are tested experimentally, which successfully reduces the turn-on speed of the circuit.

Voltage balancing of the string is tested in a boost converter operating in DCM mode at a switching frequency of 50 kHz. Results show the voltage balancing capabilities are degraded under these conditions. The origin of voltage imbalances are analyzed and solutions are tested experimentally. Additional improvements are suggested but not verified experimentally. Further use of the serialization technique is discussed in regards to its prospects in a full scale power supply for energization of ESPs.

Table of symbols

Table 1. Table of symbols used in the report.

Symbol	Unit	Name
C	F	Capacitance
D	-	Average duty cycle
d	-	Instantaneous duty cycle
E	J	Energy
f	Hz	Frequency
I	A	DC current
i	A	Instantaneous current
L	H	Inductance
M	-	Conversion ratio
V	V	DC Voltage
v	V	Instantaneous voltage
P	W	Average Power
p	W	Instantaneous power
s	-	Laplace variable
T	s	Period
T_z	s	Sample time
t	s	Continuous time
z	-	Discrete Z-domain variable
λ_0	-	Normalized output current
τ	s	Time constant
τ_D	-	Normalized deadtime

The most commonly used symbols throughout the report are listed in Table 1. Symbols listed in Table 1 that have supplementary subscripts are further explained in the context in which they appear.

Additionally to the symbols shown in the Table of Symbols, some notations will occur in the report. The notations are shown in Table 2 and are shown using the arbitrary variable, y. Combinations of more than one notation may occur. Furthermore subscripts are used to specify a specific property of the variable. Further explanation of the variable will be stated in the context.

Table 2. Table of notations used in the report.

Notation	**Description**
Δy	Change in value
$\langle y \rangle$	Switching period average
$\widetilde{y}$	Small signal variation
$\widehat{y}$	Maximum value
$\check{y}$	Minimum value
$y(s)$	Laplace transformation
$y(z)$	Z-domain transformation

Table of abbreviations

Abbreviation	Long Form
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
DUT	Device under test
DPT	Double Pulse Test
EMI	Electromagnetic Interference
ESP	Electrostatic Precipitator
FOFO	First On First Off
FPGA	Field-Programmable Gate Array
GaN	Gallium Nitride
GUI	Graphical User Interface
HV	High Voltage
IE	Intermittent Energization
I/O	Input/Output
IGBT	Insulated-Gate Bipolar Transistor
LHP	Left Half Plane
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
NI	National Instruments
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
RC	Resistor-Capacitor
RCD	Resistor-Capacitor-Diode
RHP	Right Half Plane
Si	Silicon
SiC	Silicon Carbide
SVBP	Static Voltage Balancing Performance
SMD	Surface Mounted Device
ZOH	Zero Order Hold

Chapter 1

Introduction

Stricter environmental legislations, aimed at decreasing pollution impacts and health risks, produce tightened regulations and standards governing the emission of particles from industrial processes. Particulates of sizes less than 10 μm can cause disease. Due to their small size, such particles do not easily settle to the ground by gravity and stay in the air for days. Effective filtering is required to reduce the emission of particles from industry to its surrounding areas and the air. [Grass and Fischer, 2014]

Several filter types are available as shown in Figure 1.1. Filters are classified into inertial separation, wet collection, fabric filtration and electrostatic precipitation [Parker, 1997, p. 9].

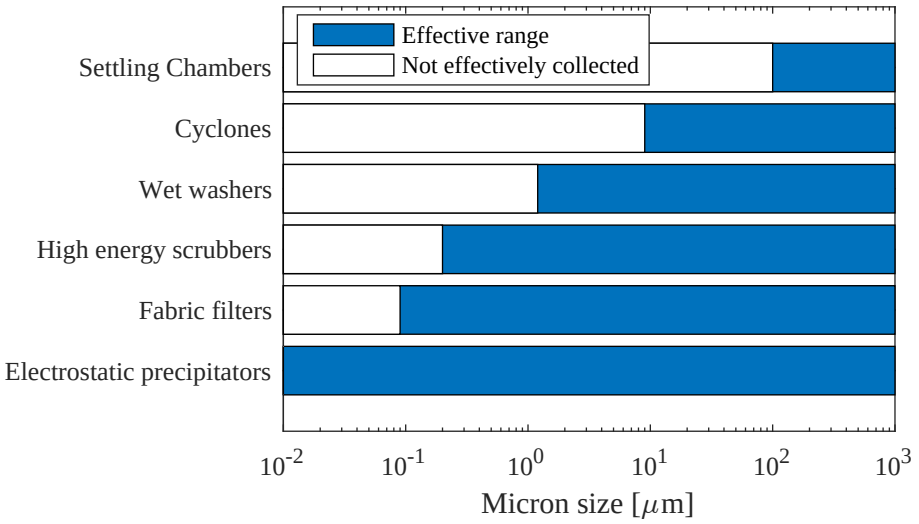


Figure 1.1. Particle size range over which reasonable collection efficiency is achieved by several filter types. Reproduced from [Parker, 1997, p. 3].

Filters utilizing inertial separation i.e. settling chambers and cyclones, have limited filtering efficiency for small particle sizes. Settling chambers depend on gravity to let dust settle in hoppers as the air moves from the inlet to the outlet nozzle. This is a low cost solution with little maintenance, but lacks collection effectiveness for small particles. Cyclones increase the particle size collection range for inertial separators. Cyclones utilize a rotating air flow in a cylindrical vessel. Dense particles have higher inertia creating a flow path of larger radius, which results in an impact with the cylinder wall. Particles are collected at the bottom of the cylinder by the force of gravity. This limits the effective collection range to particles larger than 10 μm [Vasarevicius, 2012]. Inertial separators suffer from high pressure loss, causing difficulty in filtration of the large airflows

encountered in industrial applications, such as coal fired power plants and cement kilns.

Wet collectors, i.e. wet washers and high energy scrubbers, operate by impact between particles and liquid. Wet washers operate by leading air through a chamber with several spray nozzles. The pollutants are dissolved or carried away by the liquid, which is typically water. This enables the wet washers to filter some gaseous pollutants. The particle size range is further increased by high energy scrubbers, where the spray is replaced by a highly turbulent liquid flow. The wet collectors suffer from high pressure loss, large water usage and the air pollution problem is converted to a water pollution problem. [Parker, 1997, p. 3]

An effective filtration type is the fabric filter, as highlighted by Figure 1.1. The polluted air stream is passed through a membrane which filters particulates. Build-up of deposited particulate creates a layer which enables collection of particles with a much smaller diameter than the membrane pore size. The fabric filter has advantageous particle size range. To maintain a low operating pressure drop it is necessary to periodically remove the deposit layer on the membrane, by vibration or reverse air purging. The filter bags are made of various fabrics depending on operating conditions such as temperature, acid resistance and tensile strength [Vasarevicius, 2012, p. 34]. This limits the adaptability of the filter and its disadvantages include pressure loss build-up, fabric temperature limitations, fire risk and incapability of filtering sticky/wet dusts. Fabric filters must be replaced to ensure emission compliance, which adds maintenance costs.

The electrostatic precipitator (ESP) is the type of filter which effectively collects the largest range of particle sizes. A section of an ESP is shown in Figure 1.2. It consists of discharge electrodes placed along the direction of air flow. The electrodes are energized by high voltage (HV). Corona discharge occurs in proximity of the sharp discharge electrode where the electric field is strongest. Particles that pass the electrode are ionized as they receive an electric charge. The charged particles are moved towards collecting plates, placed parallel to the electrodes, by Coulomb forces [Mizuno, 2000]. Collecting plates are periodically cleaned by mechanical means such as hammers acting on the collecting plates.

ESPs offer effective filtering for the largest range of particle sizes, have low pressure loss and work equally well for wet and dry conditions. The ESP is capable of operating at high temperatures, which is an advantage compared with fabric filters. Maintenance of ESPs is low and lifetime exceeds 20 years. They suffer from relatively high initial costs and the efficiency is sensitive to dust resistivity, requiring feedback control systems to regulate the electrical operating conditions of the ESP. For large scale industrial applications the ESP is superior to other filtering types [Parker, 1997, p. 9].

1.1 Operation of ESPs

The following section summarizes the electrical operation of ESPs as described in literature. Some limitations and challenges faced when operating the ESPs are highlighted.

The discharge electrode is normally operated at negative polarity. The corona initiation voltage and the electrical breakdown occur at higher voltage for negative polarities than for positive. The result is higher electrical fields strengths which allows more effective

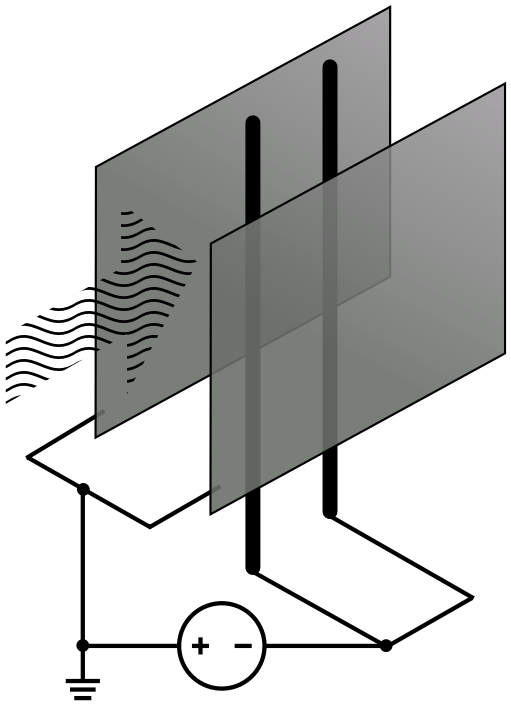


Figure 1.2. Principle diagram of an electrostatic precipitator.

filtering. Discharge electrodes are energized by a negative HV, while the collecting plates are grounded [Parker, 1997, p. 31].

ESPs are divided into sections, such as the one shown in Figure 1.2, placed both serially and in parallel to one another. The voltage of each section is changed depending on the operating conditions such as dust loading and particle sizes. This is shown in Figure 1.3, for the first and the last sections of the ESP. The corona onset voltage is larger for the first section.

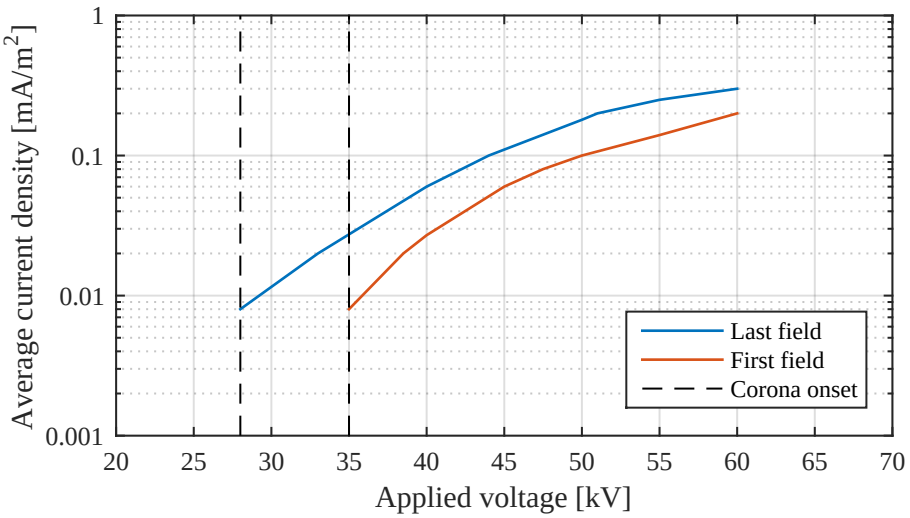


Figure 1.3. i-v characteristics for the first and the last section of an ESP under normal dust loading operating conditions. Reproduced from [Parker, 1997].

Under conditions of large particle concentration the corona is suppressed or quenched totally. If sections are operated from the same supply, a high voltage on the first section could cause excessive corona or even sparking on the latter sections. In consequence all sections must be operated at the same lowered voltage which causes lowered corona power and a resulting loss of precipitator efficiency [Parker, 1997, p. 200]. Further reductions in spark voltage level occurs due to localized constructional effects including: misalignment of electrodes, vibration of electrodes and excessive dust build-up. This highlights that entire ESPs should not be energized from a single supply unit for effective operation. The maximum efficiency is obtained if each electrode is energized by its own supply. The reason for not using this solution is economic, as the total cost is lower with more sections connected to the same supply unit. Insulation costs are lower with fewer supply units and the physical space required is reduced.

Traditionally ESPs were energized by DC voltages. Since the 1980s methods of AC rippled and pulsed voltages have been applied. The purpose is to save energy and the method has proved to have improved collection effectiveness for high resistivity dusts [Parker, 1997, p. 210]. The peak voltage of the pulsed voltage is higher than the DC voltage spark level. AC ripples are usually at mains frequency or multiples below. Durations of pulsed voltages range from ms to μs. Figure 1.4 shows typically applied voltages to ESPs i.e. DC voltages, AC rippled and pulsed. The three types are used for filtering of low-, medium- and high resistivity dusts, respectively.

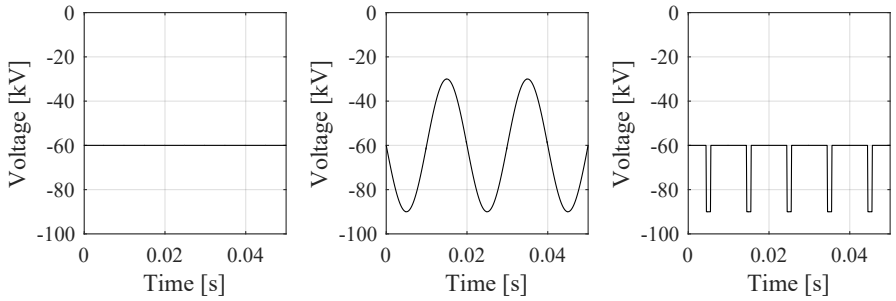


Figure 1.4. Typical applied voltages to ESPs. From left to right DC-voltage, AC ripple and pulses.

Figure 1.5 shows the dust emissions from two plants having low and high resistivity dusts. The filters have DC voltage and intermittent energization (IE) applied. IE is a method which has characteristics of both AC ripple and pulsed voltages. The method is a result of thyristor set power supplies, as will be further explained in Section 1.2, by only passing some rectified AC half cycles. Figure 1.5 highlights that sufficiently high DC voltage and ripple/pulsed voltages are required simultaneously to effectively filter both low and high resistivity dusts. For large industrial ESPs efficient power supplies of semiconducting switches or LC oscillators are used to rapidly supply and recover the energy in the ESP capacitance. Bidirectional power flow of the ESP is essential to obtain high efficiencies. [Mizuno, 2000, p. 621]

The occurrence of sparks in the ESP is a stochastic process, meaning the statistical probability of sparking is distributed around the spark voltage. For effective filtering the applied average voltage of the ESP is close to the spark voltage level. During operation

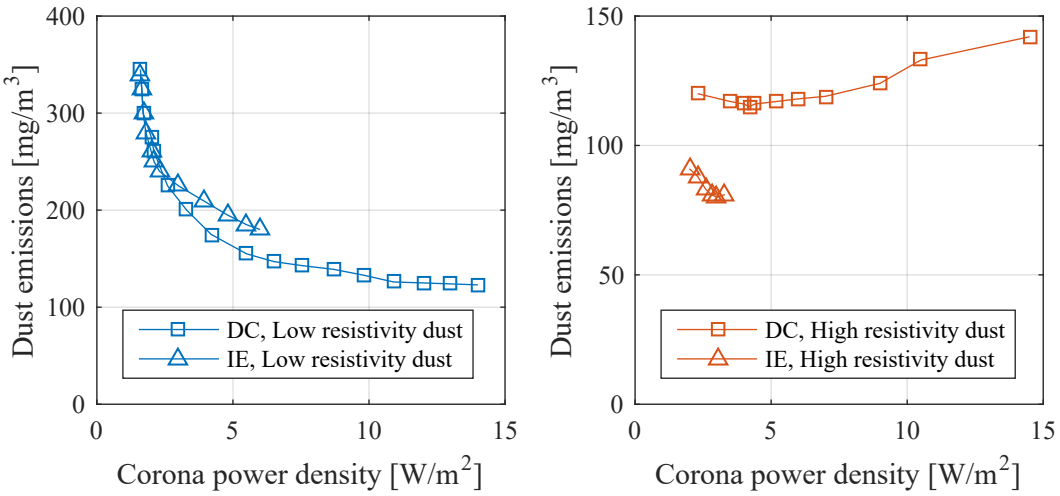


Figure 1.5. Dust emissions as a function of the corona power under DC voltage and IE for both low and high resistivity conditions. Data set from [Parker, 1997, p. 215].

the spark limit may vary, therefore sparks cannot always be avoided [Grass et al., 2002]. A typical control technique is shown in Figure 1.6. The reference for the mean current is continuously increased to ensure effective filtering despite changes in operating conditions. At some point the voltage reaches the spark limit and the current is reduced by a setback value. For a constant sparking level this control strategy causes a spark rate. The control parameters rate of rise and setback determine the spark rate. To maintain effective filtering i.e. high corona power, during varying conditions the rate of rise should be high or the setback should be low. This produces a high spark rate, for which an upper limit exists. A too high spark rate reduces the lifetime of the ESP due to erosion at the points of sparking [Parker, 1997, p. 223]. Depending on the construction and power supply of the ESP a finite voltage recovery time exists. During voltage recovery filter effectiveness is subpar. Thus the effectiveness of the ESP is dependent on the speed of recovery following a spark.

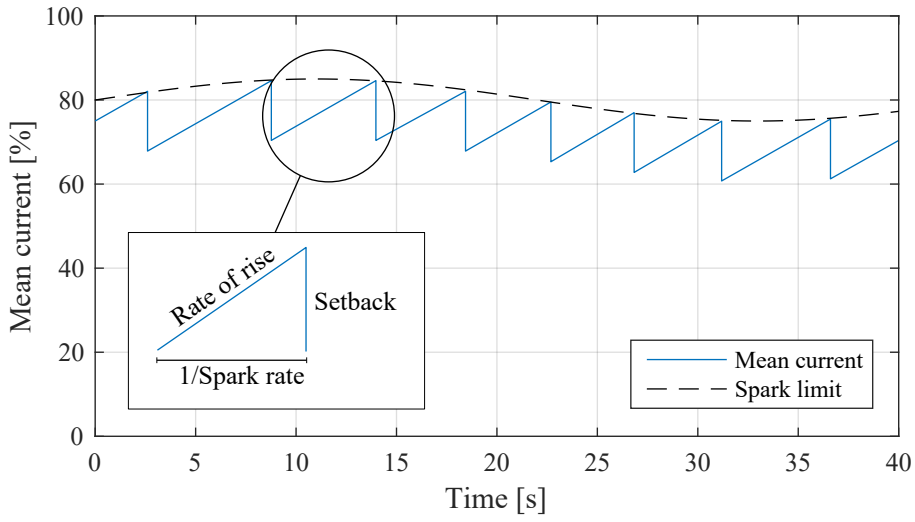


Figure 1.6. Basic control strategy for the precipitator current.

1.2 Traditional ESP energization

A common HV power supply for ESPs, which is still in use today due to its simplicity, is the line-commutated thyristor power supply, shown for a single phase in Figure 1.7. The thyristors operate at the line frequency of 50-60 Hz. The voltage on the ESP is controlled by the firing angle of the thyristors. This causes a control delay in the range of 10 ms. Thyristor based power supplies use a method known as intermittent energization. The principle is to suppress a certain number of the rectified AC half-cycles, equivalent to a firing angle of 180° [Grass et al., 2002]. This limits the duration of the pulse to a minimum of several milliseconds, which decreases the maximum peak voltage without triggering a spark. Due to the dependency of the AC half-cycles the voltage recovery time is also limited to tens of milliseconds depending on the severity of the spark. Following the discussion of Section 1.1 this results in a lowered effectiveness of the ESP.

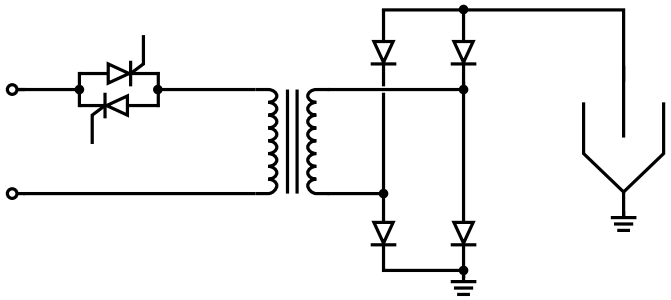


Figure 1.7. Conventional line-commutated thyristor power supply.

A schematic for a state of the art power supply used in ESPs is shown in Figure 1.8. This power supply utilizes hard switching of silicon (Si) IGBT switches for operation and control. These operate at switching frequencies of 1-4 kHz, reducing the delay of control to 250-1000 μs. This allows for faster voltage recovery following a spark. The size of the HV transformer is reduced by moving it to the high frequency side of the inverter bridge. Smaller dimensional requirements both saves costs and allows for greater sectionalization of the ESP. As highlighted in Section 1.1 this allows for improved filtering. The shift from thyristors to IGBTs in ESP power supplies is advantageous as it allows for higher power density of the supply and faster voltage recovery. [Grass et al., 2002]

A high turns ratio of the HV transformer is commonly used to achieve high voltage on the output, which causes difficulty in maintaining low parasitic capacitances and inductances.

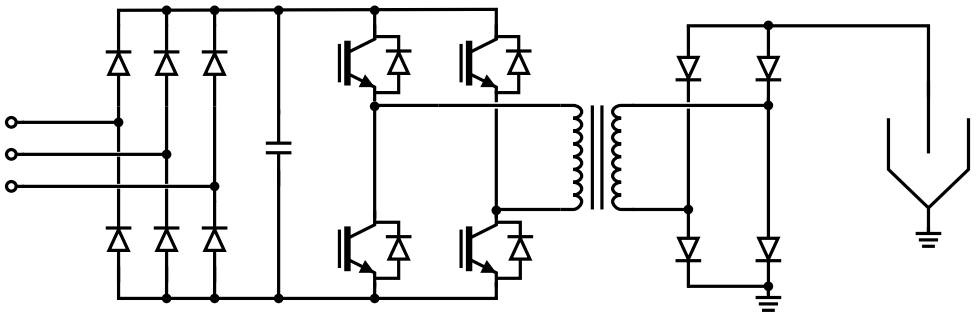


Figure 1.8. ESP Power supply based on hard switching of Si IGBT switches.

Hard switching of the IGBT-based topology on a HV transformer with excessive parasitics, have shown significant deviations from expected system behaviour and decreased efficiency.

Resonant converters lessens the requirements of the HV transformer by incorporating the parasitics as a resonant tank in the converter design, as shown in Figure 1.9. Additionally, a major advantage of the resonant converter is that it enables soft-switching of the IGBTs. This reduces the switching losses and allows the switching frequency to be increased above 30 kHz. Resonant converters further reduce the required size of the HV transformer and allows faster voltage recovery. A drawback is that variable frequency control of resonant converters puts difficulty in the design of magnetic components and electromagnetic interference filtering. An upper limit for the switching frequency exists, which limits the variable frequency control mode. Dynamic operating conditions forces the resonant converter to operate in duty cycle mode instead of variable frequency. In conclusion when compared to the hard-switched IGBT bridge, increased switching frequency and lower requirements in the HV transformer are benefits of the resonant converter but comes at the cost of significantly increased complexity in converter design and control. [Soeiro et al., 2013]

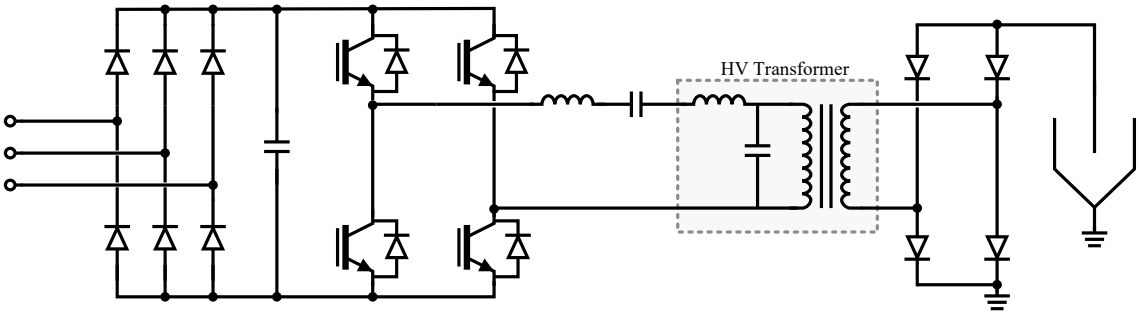


Figure 1.9. Resonance LCC converter used for energization of ESPs.

1.3 Emergence of wide band gap devices

The power supplies presented in previous sections are based on Si devices. The Si IGBT is preferred to the Si thyristor because of its increased controllability. To reach higher blocking voltages devices are connected in series. Si IGBTs are rated at a few thousand volts, which requires fewer devices in series when compared to Si MOSFETs, rated at only a few hundred volts.

Emergence of wide band gap devices such as silicon carbide (SiC) and gallium nitride (GaN) offers advantages when compared with Si. Selected characteristics of Si, SiC and GaN are shown in Table 1.1.

Both SiC and GaN have higher bandgap, electric field breakdown and saturated electron velocity when compared to Si. This results in higher operating levels, faster switching times and reduced conduction losses [Li et al., 2014]. The thermal conductivity of SiC is higher than Si and GaN. This suggests that SiC devices can be operated at higher power levels as they more easily dissipate the produced losses. Alternatively for similar power levels the required cooling of SiC devices is reduced, allowing more compact design. SiC devices pose a potential in several power electronic applications [Wu et al., 2014]. The

Table 1.1. Selected physical characteristics of Si, SiC and GaN. [Jain, 2003] and [Kaminski and Hilt, 2012]

Property	**Unit**	**Si**	**4H-SiC**	**GaN**
Bandgap	$[\,\mathrm{eV}]$	1.12	3.26	3.39 to 3.45
Electric Field Breakdown	$\left[\frac{\mathrm{kV}}{\mathrm{mm}}\right]$	30	220	200 to 330
Thermal Conductivity	$\left[\frac{\mathrm{W}}{\mathrm{mm}\cdot\mathrm{K}}\right]$	15	49	13 to 30
Saturated Electron Drift Velocity	$\left[\frac{\mathrm{mm}}{\mu\mathrm{s}}\right]$	100	200	220

slightly higher switching speed of GaN is useful in high frequency low power integrated circuits [Kaminski and Hilt, 2012].

For comparison, Si IGBT modules are rated up to few thousand volts, i.e. 4500 V for Infineon FZ1200R45HL3, with rise and fall times of 500-700 ns. Novel 10 kV SiC MOSFETs by CREE/Wolfspeed are currently in development and undergoing tests, with experimentally verified rise and fall times of less than 150 ns [Das et al., 2011]. Commercially available SiC MOSFETs are currently rated at 1.2 kV/1.7 kV, with rise and fall times typically in the range of 20-80 ns.

SiC MOSFETs offer potential advantages in power supplies used for operation of ESPs, compared with current Si IGBT solutions. Faster switching time and reduced losses allows for higher switching frequencies, enabling faster voltage recovery in the event of sparking. The blocking voltage reduces the required number of devices in series which lowers dimensional requirements. This benefits the possibility of higher sectionalization in the ESP, offering more effective filtering as stated in Section 1.1. Because higher voltages are achieved with fewer devices, a possibility is to remove the bulky HV transformer used to step up the voltage. Instead the series-connected SiC MOSFET devices may be connected directly at the output voltage level.

However, the high voltage ratings and fast switching speeds of SiC MOSFETs pose additional issues to the circuit design. Larger values of $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ introduce higher amounts of voltage noise and ringing [Li et al., 2014]. Additionally, fast switching puts further demand on voltage balancing techniques for series connected devices. These issues are to be investigated for the integration of SiC MOSFETs in modern high voltage power supply units.

Chapter 2

Problem statement

The problem statement is given by FLSmidth Airtech A/S for master students on "Power Electronics and Drives" at Aalborg University. ESPs are used in industrial processes to remove particles from fumes. They require high-voltage power supplies and the commonly adopted technologies are based on Si thyristor or IGBT switching sets. The emergence of SiC offers potential benefits in the power supply design for ESPs. However, this requires voltage balancing of series connected SiC MOSFETs, for which only limited research currently exists. The project aims at investigating methods for series connection of SiC MOSFETs, and experimentally evaluate the performance of a suitable method.

2.1 Objectives

The objectives of the project are

- Choosing a converter topology and operating mode of a medium voltage transformerless DC/DC converter using SiC MOSFETs for an ESP application. The system should be designed for a small scale ESP having the following characteristics
  - Rated output voltage: 6 kV
  - Rated output current: 17 mA
  - ESP capacitance: 17 nF
  - Bidirectional power flow for rapid charge/discharge of ESP
- Selection of a suitable method for series connecting SiC MOSFETs
- Experimentally evaluate the performance of the chosen serialization method in a double pulse test setup
- Experimentally evaluate the performance of the serialization method operating in the chosen DC/DC converter topology

2.2 Resources

To fulfill the objectives, the following resources were available

- 49 mH high voltage air coil inductor
- National Instruments (NI) CompactRIO 9030
- 10 kV Magna-Power XR100000-0.20 power supply

Additional laboratory equipment, such as low voltage power supplies, oscilloscopes and voltage probes, are also available during the project.

2.3 Outline

The following section lists the chapters of the report, documenting the work done to solve the objectives.

Chapter 3 Converter Topology and Operating Modes: A DC/DC bidirectional converter topology is chosen, and its circuit states and operation modes are derived analytically. Losses of semiconducting devices in the circuit are estimated to choose components used for the experimental setup. A control concept is proposed and simulated using PLECS.

Chapter 4 Series Connection of SiC MOSFETs: A literature study is done on serialization methods for SiC MOSFETs. Advantages and disadvantages of each method are compared and a suitable method is chosen for further investigation. The operation of the chosen method is analytically evaluated and is verified by a simulation in LTSpice IV.

Chapter 5 PCB Development and Test Setup Design: This chapter presents the design concept used for building the proposed serialization method. The chapter also documents the hardware used in the test setup to enable experimental tests.

Chapter 6 Double Pulse Test Results: Experimental results of the serialization method in a double pulse test are presented. The performance of the serialization method is evaluated and operation of the circuit is analyzed. Modifications to the hardware are implemented and tested experimentally.

Chapter 7 Voltage Balancing during Converter Operation: The performance of the designed series connection of SiC MOSFET is tested when operated as a switch in the proposed DC/DC converter topology.

Chapter 8 Discussion: Advantages and disadvantages of the designed circuitry are discussed in regard to future use.

Chapter 9 Conclusion: A conclusion of the project work is presented.

Chapter 3

Converter Topology and Operating Modes

This chapter presents an analysis of the chosen converter topology, a loss estimation to choose suitable components and simulation of the converter. The circuit analysis is based on [Erickson and Maksomovic, 2001] and the converter operating modes are analyzed following the work of [Bidoggia et al., 2012].

3.1 Topology

The chosen topology is the synchronous boost converter as depicted in Figure 3.1. The synchronous boost topology allows for bidirectional power flow, using a minimum amount of components. Several switches are depicted in series as the high voltage requirements of the ESP can not be met by a single switch.

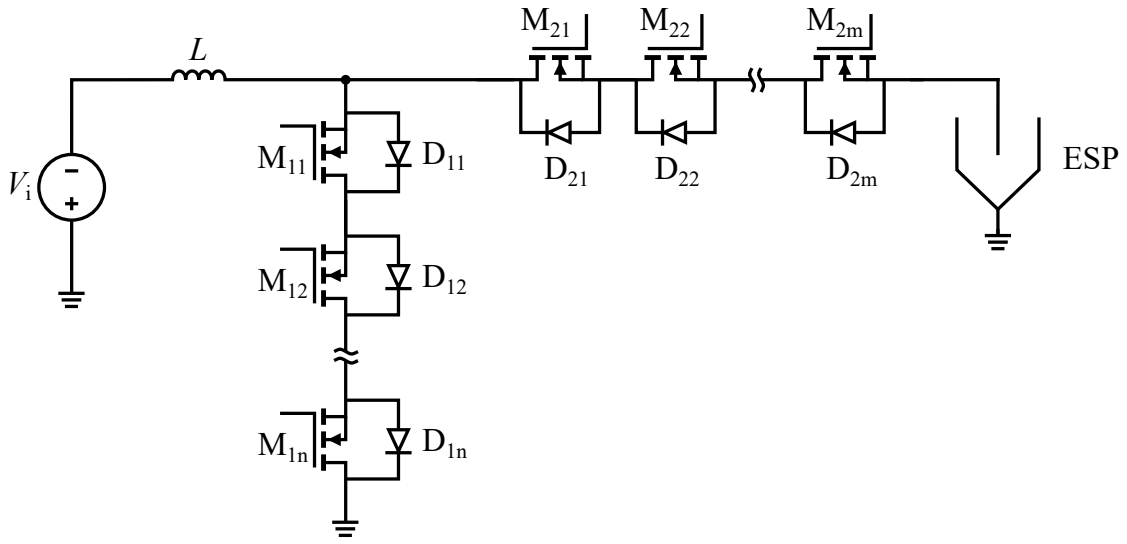


Figure 3.1. Synchronous boost converter topology with ESP load.

For the purpose of the following analysis the string of switches: S_{11}, S_{12}, ..., S_{1n} are treated as a single ideal switch with an anti parallel ideal diode and the same goes for the switches S_{21}, S_{22}, ..., S_{2m}. Also the ESP is modeled as an RC load. This circuit representation is depicted in Figure 3.2 where conventions regarding positive current directions and voltage polarities are defined.

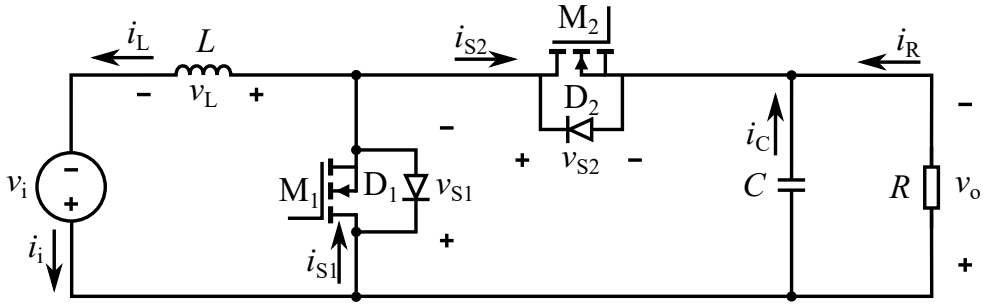


Figure 3.2. Simplified circuit representation of the synchronous boost converter and ESP load.

3.1.1 States

The circuit diagram of Figure 3.2 contains four switching devices, assuming that the MOSFET and anti parallel diode are considered as two independent devices. Each device has two states: 'on' and 'off', which means that the circuit can assume $2^4 = 16$ different states. However, during normal operation, the two switches should never be on at the same time, since it would result in a short circuit over the ESP, which would mean a voltage drop and hence a reduced filtering efficiency.

Considering only the MOSFETs, the circuit has three practical states: A, B, and C, as depicted in Figure 3.3. In state A, M_1 is on and M_2 is off. In the case of ideal devices D_1 is off, in a practical case, however, the state of D_1 depends on the direction and magnitude of the current through the switch (i_{S1}). Since $v_i < v_o$, D_2 is reverse biased and will be off. In state B, M_1 is off and M_2 is on. Similarly to state A the state of D_2 depends on the direction and magnitude of i_{S2}. D_1 is reverse biased by v_o. Finally in state C, neither MOSFET is conducting. Instead either D_1 or D_2 is conducting, depending on the inductor current direction. If the inductor current is zero, none of the diodes are conducting. Therefore state C is split into three sub-states: C_+ (for $i_L > 0$), C_- (for $i_L < 0$), and C_0 (for $i_L = 0$). This is summarized in Table 3.1.

In state A, M_1 is conducting meaning that the voltage drop on the inductor is v_i. When

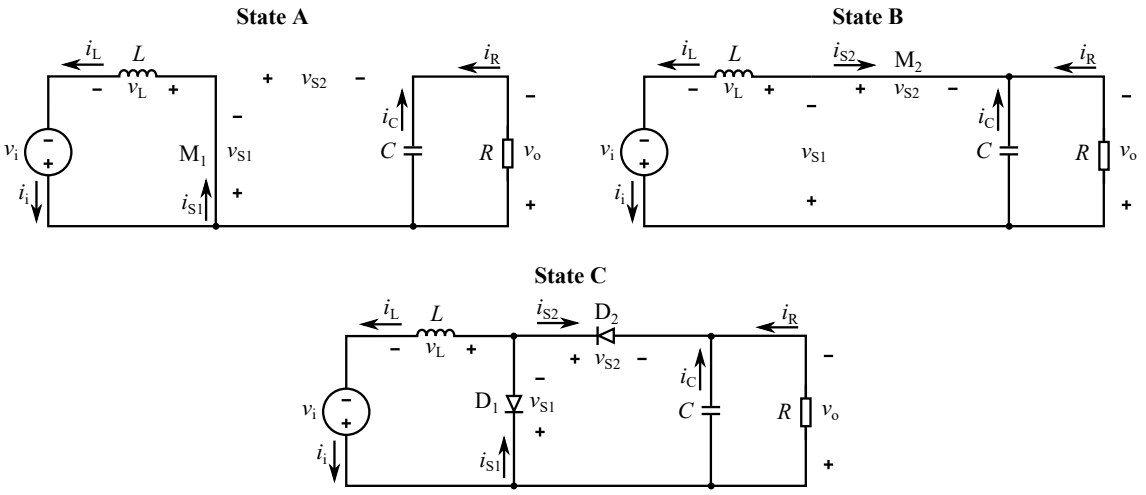


Figure 3.3. Circuit representation of practical converter states.

Table 3.1. Converter States. 0 and 1 refer to the device on and off state, respectively.

	$\mathbf{M}_1$	$\mathbf{M}_2$	$\mathbf{D}_1$	$\mathbf{D}_2$	i_L
A	1	0	0	0	
B	0	1	0	0	
$\mathbf{C}_-$	0	0	1	0	< 0
$\mathbf{C}_+$	0	0	0	1	> 0
$\mathbf{C}_0$	0	0	0	0	$= 0$

assuming the input voltage is constant within a switching cycle ($v_\mathrm{i} = V_\mathrm{i}$), this gives rise to a change in current through the inductor described by

$$i_\mathrm{L} = \frac{1}{L}\int v_\mathrm{L}\mathrm{d}t = \frac{V_\mathrm{i}}{L}t + i_\mathrm{L}(t_0) \tag{3.1}$$

where $i_\mathrm{L}(t_0)$ is the initial value of i_L at $t = t_0$. From Figure 3.3 it can be seen that S_2 is blocking the output voltage and that S_1 is conducting the inductor current. Also the capacitor current circulates through the resistor.

Similar analysis is conducted for the remaining states and the expressions are summarized in Table 3.2.

Table 3.2. Voltages and currents of converter states.

State	v_L	i_L	v_S1	i_S1	v_S2	i_S2	i_C
A	V_i	$\frac{V_\mathrm{i}}{L}t + i_\mathrm{L}(t_0)$	0	i_L	V_o	0	$-\frac{V_\mathrm{o}}{R}$
B	$V_\mathrm{i} - V_\mathrm{o}$	$\frac{V_\mathrm{i}-V_\mathrm{o}}{L}t + i_\mathrm{L}(t_0)$	V_o	0	0	$-i_\mathrm{L}$	$i_\mathrm{L} - \frac{V_\mathrm{o}}{R}$
C_+	$V_\mathrm{i} - V_\mathrm{o}$	$\frac{V_\mathrm{i}-V_\mathrm{o}}{L}t + i_\mathrm{L}(t_0)$	V_o	0	0	$-i_\mathrm{L}$	$i_\mathrm{L} - \frac{V_\mathrm{o}}{R}$
C_-	V_i	$\frac{V_\mathrm{i}}{L}t + i_\mathrm{L}(t_0)$	0	i_L	V_o	0	$-\frac{V_\mathrm{o}}{R}$
C_0	0	0	V_i	0	$V_\mathrm{o} - V_\mathrm{i}$	0	$-\frac{V_\mathrm{o}}{R}$

3.1.2 Operating Modes

The gate signals for M_1 and M_2 for one switching period, T_s, are sketched in Figure 3.4. The duty cycle, D, defines the on time of M_1, i.e. it conducts for $(D - \tau_\mathrm{D})T_\mathrm{s}$, where τ_D is the normalized dead time ($\frac{T_\mathrm{D}}{T_\mathrm{s}}$) and T_s is the switching period. As indicated in the figure, this switching scheme gives an inherent sequence of states: C, A, C, B.

In total seven operating modes exist, defined from the inductor current waveform: three continuous conduction modes (CCM) and four discontinuous conduction modes (DCM). CCM is defined as a mode where the inductor is continuously conducting current, whereas DCM contains a period in which the inductor current is zero. The seven modes are:

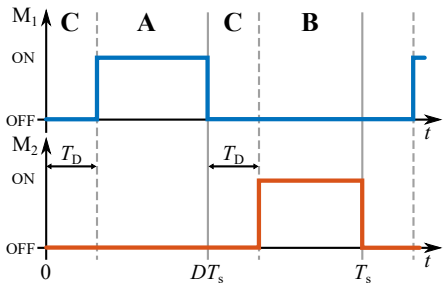


Figure 3.4. Switching signals for switch one and switch two.

CCM+, DCM2+, DCM1+, CCM0, DCM1-, DCM2-, and CCM-. The modes, represented by inductor voltage waveforms and current waveforms, are depicted in Figure 3.5, which also shows the waveforms at the boundaries between the different operating modes. The boundaries are denoted as L2+, L1+, L0+, L0-, L1-, and L2-, where L2+ defines the boundary between CCM+ and DCM2+, L1+ defines the boundary between DCM2+ and DCM1+ and so forth.

Conversion Ratios

The conversion ratio of the converter is defined as $M = \frac{v_o}{v_i}$. The converter operates in one of its three CCM modes for the majority of operating conditions, because the normalized dead time τ_D is generally only a fraction of the duty cycle, D. In the case of no dead time, only the three CCM modes remain. For the CCM modes, the conversion ratio is a direct consequence of the duty cycle and is found from the inductor volt-second balance:

$$\langle v_L \rangle = 0 \tag{3.2}$$

For the case of CCM+ the volt-second balance is

$$\begin{aligned} \langle v_L \rangle &= \frac{1}{T_s}\left((v_i - v_o)\tau_D T_s + v_i(D - \tau_D)T_s + (v_i - v_o)(1 - D)T_s\right) \\ &= v_i - v_o(1 - D + \tau_D) = 0 \end{aligned} \tag{3.3}$$

Which rearranges to the conversion ratio of (3.4). Similar analysis leads to the expressions for the CCM0 and CCM- conversion ratios of (3.5) and (3.6), respectively.

$$M_{CCM+}(D) = \frac{1}{1 - D + \tau_D} \tag{3.4}$$

$$M_{CCM0}(D) = \frac{1}{1 - D} \tag{3.5}$$

$$M_{CCM-}(D) = \frac{1}{1 - D - \tau_D} \tag{3.6}$$

From (3.4)-(3.6) it is evident that the CCM+ and CCM- mode conversion ratios depend on the dead time, whereas CCM0 conversion ratio is independent of τ_D. A voltage feedback controller is added to correct the conversion ratio as the converter enters a new operating mode. From a control point of view it is advantageous that the conversion ratio of CCM modes during steady state operation is only dependent on D and τ_D.

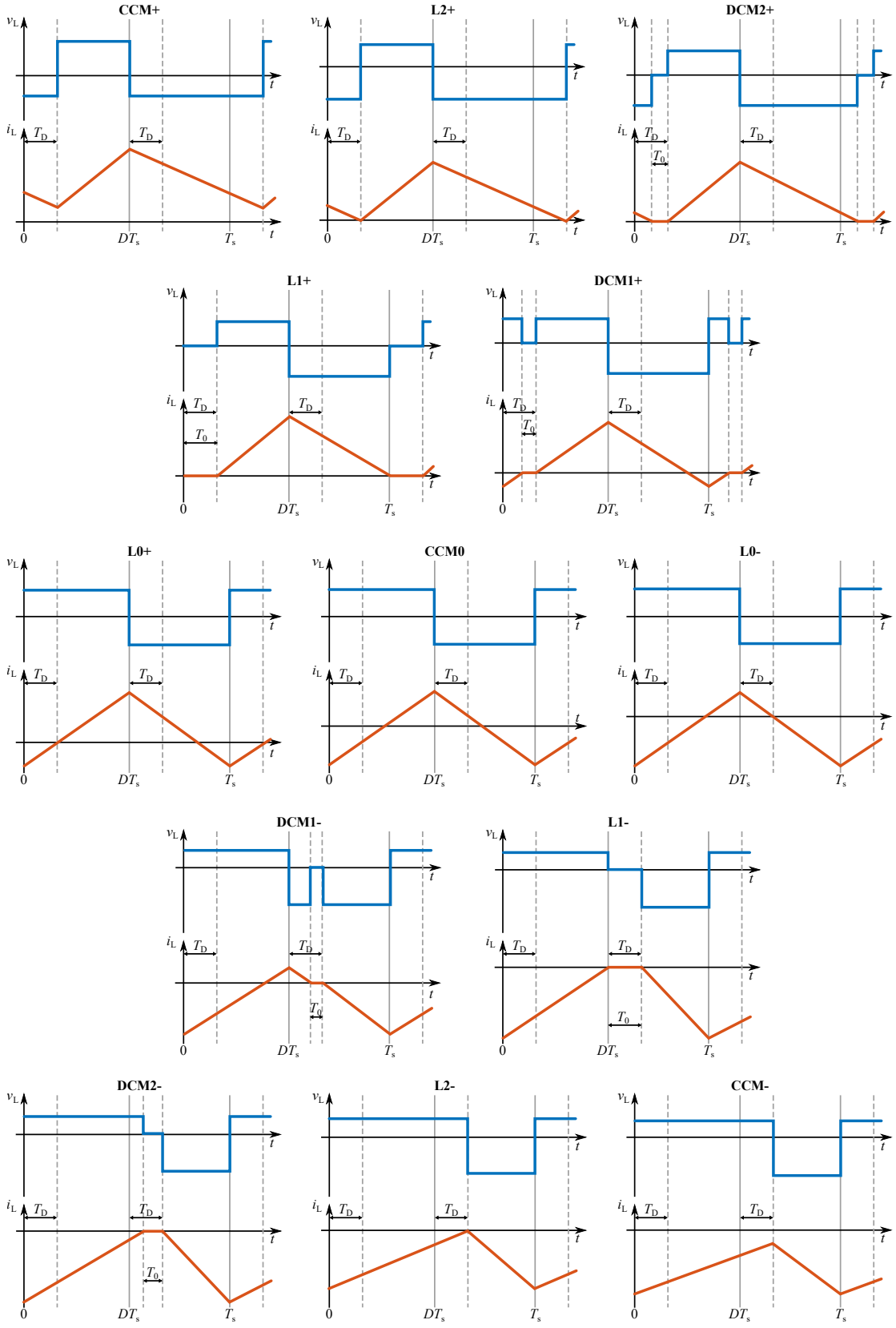


Figure 3.5. Synchronous boost converter inductor voltage and current for different operating modes.

Mode Boundaries

The boundaries between operating modes occur at a specific output current, I_o. For example when in CCM+, if the output current drops, it means a drop in inductor current ($\langle i_\mathrm{L} \rangle = MI_\mathrm{o}$). If the I_o-drop causes the inductor current to reach zero within the dead time period, D_2 will stop conducting and the converter will enter the C_0 state and will operate in DCM2+.

The boundary expressions are derived by realizing that the negated average S_2 current is equal to the average output current ($-\langle i_{\mathrm{S}2} \rangle = I_\mathrm{o}$). For the boundary between CCM+ and DCM2+ (L2+), D_2 is conducting the inductor current in both the dead time periods and M_2 is conducting the inductor current during the fourth period (state B). Hence

$$\langle i_{\mathrm{S}2} \rangle = \frac{1}{T_\mathrm{s}} \left(\int_0^{T_\mathrm{D}} -i_\mathrm{L} \mathrm{d}t + \int_{DT_\mathrm{s}}^{T_\mathrm{s}} -i_\mathrm{L} \mathrm{d}t \right) = -\frac{1}{T_\mathrm{s}} \int_{DT_\mathrm{s}}^{T_\mathrm{s}+T_\mathrm{D}} i_\mathrm{L} \mathrm{d}t \tag{3.7}$$

From the L2+ graph of Figure 3.5 it can be seen that the inductor current falls from its maximum value ($\widehat{I}_\mathrm{L}$) to zero during the time interval $t = [DT_\mathrm{s} : T_\mathrm{s} + T_\mathrm{D}]$, hence (3.7) is simplified to the geometric relation:

$$\langle i_{\mathrm{S}2} \rangle = -\frac{1}{2} \widehat{I}_\mathrm{L} (1 - D + \tau_\mathrm{D}) = -I_\mathrm{o} \tag{3.8}$$

where

$$\widehat{I}_\mathrm{L} = \frac{V_\mathrm{i}}{L} (D - \tau_\mathrm{D}) T_\mathrm{s} \tag{3.9}$$

Combining (3.8) and (3.9) yields

$$\frac{I_\mathrm{o}}{\frac{V_\mathrm{i} T_\mathrm{s}}{2L}} = (1 - D + \tau_\mathrm{D})(D - \tau_\mathrm{D}) \tag{3.10}$$

For simplicity the normalized output current is defined as

$$\lambda_\mathrm{o} = \frac{I_\mathrm{o}}{\frac{V_\mathrm{i} T_\mathrm{s}}{2L}} \tag{3.11}$$

The boundaries are summarized in (3.12)-(3.17).

$$\lambda_{\mathrm{o},2+}(D) = (1 - D + \tau_\mathrm{D})(D - \tau_\mathrm{D}) \tag{3.12}$$
$$\lambda_{\mathrm{o},1+}(D) = (1 - D)(D - \tau_\mathrm{D}) \tag{3.13}$$
$$\lambda_{\mathrm{o},0+}(D) = (1 - D)(D - 2\tau_\mathrm{D}) \tag{3.14}$$
$$\lambda_{\mathrm{o},0-}(D) = -(1 - D - 2\tau_\mathrm{D})D \tag{3.15}$$
$$\lambda_{\mathrm{o},1-}(D) = -(1 - D - \tau_\mathrm{D})D \tag{3.16}$$
$$\lambda_{\mathrm{o},2-}(D) = -(1 - D - \tau_\mathrm{D})(D + \tau_\mathrm{D}) \tag{3.17}$$

The mode boundaries are visualized in Figure 3.6, for τ_D equal to 0.05. It shows that the window for control inside the DCM modes is very narrow. A slight change in operating conditions causes the converter to enter one of the CCM operating modes.

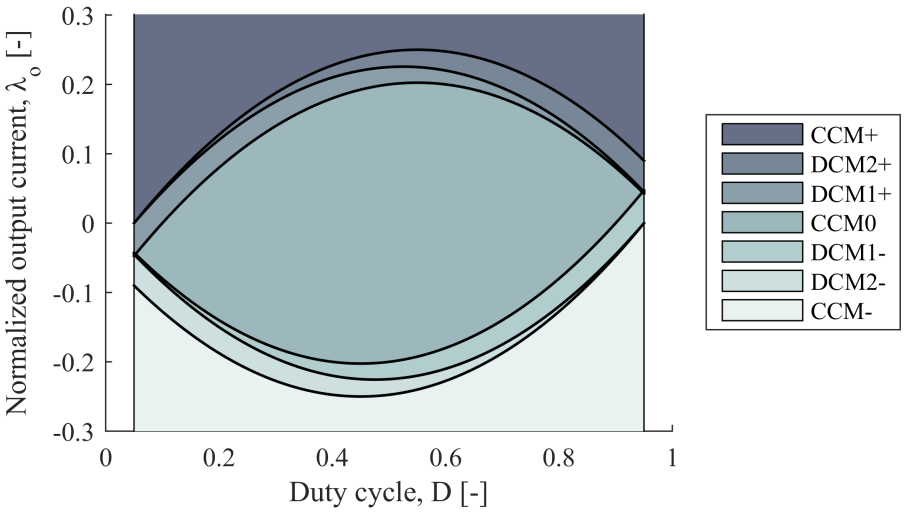


Figure 3.6. Synchronous boost operating mode boundaries.

3.2 Operating Point

The defined converter ratings of Section 2.1 implies a load resistance of

$$R = \frac{V}{I} = \frac{6\,\mathrm{kV}}{17\,\mathrm{mA}} = 353\,\mathrm{k\Omega} \tag{3.18}$$

The nominal operating voltage is assumed to be 5 kV, which for the same dust conditions, i.e. load resistance gives a nominal current of 14.2 mA.

The available input inductor has an inductance of 49 mH and the switching frequency is chosen to 50 kHz as a starting point. This frequency is chosen because it allows for fast control of the converter, and therefore faster voltage recovery than possible with traditional solutions, as presented in Section 1.2. However, a final choice of switching frequency depends on the switching speed, losses and voltage balancing of the serialization method, which is investigated in Chapter 4. The chosen parameters and the nominal operating point give a normalized output current of

$$\lambda_\mathrm{o} = \frac{I_\mathrm{o}}{\frac{V_\mathrm{i}}{2Lf_\mathrm{s}}} = \frac{14.2\,\mathrm{mA}}{\frac{1\,\mathrm{kV}}{2 \cdot 49\,\mathrm{mH} \cdot 50\,\mathrm{kHz}}} = 0.070 \tag{3.19}$$

From Figure 3.6 it can be seen that at this λ_o, the largest duty cycle range and thereby the largest control range occurs in the CCM_0 mode. This operating mode will be analyzed in terms of losses.

3.2.1 Loss Analysis

The purpose of this section is to choose a suitable switching device for the converter topology. The loss analysis is based on approximate switching waveforms. The chosen devices and relevant device parameters are listed in Table 3.3.

The inductor current is shown in Figure 3.7. It is conducted by different devices during the switching period. The device which conducts the current is highlighted in the figure

Table 3.3. Device parameters.

Parameter	ROHM SCT2H12NZ	CREE C2M1000170D	ROHM SCT2450KE	CREE C2M0280120D
V_{dss}	1.7 kV	1.7 kV	1.2 kV	1.2 kV
$V_{(\text{plateau})}$	10.5 V	12.1 V	10.5 V	9.2 V
$V_{\text{gs(th)}}$	1.6 V	2.0 V	1.6 V	2.0 V
V_{F}	4.3 V	3.3 V	4.3 V	3.3 V
I_{rr}	1.1	6.5 A	1.4	4 A
$\frac{\text{d}i_{\text{R}}}{\text{d}t}$	0.3 $\frac{\text{A}}{\text{ns}}$	1.2 $\frac{\text{A}}{\text{ns}}$	0.11 $\frac{\text{A}}{\text{ns}}$	1 $\frac{\text{A}}{\text{ns}}$
t_{rr}	21	20 ns	19 ns	24 ns
$R_{\text{ds,on}}$	1.15 Ω	1.00 Ω	0.45 Ω	0.28 Ω
R_{g}	64.0 Ω	24.8 Ω	25.0 Ω	11.4 Ω
C_{gs}	178.0 pF	198.7 pF	459.0 pF	256.0 pF
C_{gd}	6.0 pF	1.3 pF	4.0 pF	3.0 pF

by different colors. Each switch is treated as two separate devices: the MOSFET, M, and the body diode, D, because the modeling of losses associated with the two are different.

The losses are split into two categories: conduction loss and switching loss. The losses associated with CCM_0 are conduction loss of M_1, M_2, D_1 and D_2, as well as turn-off loss of M_1 and M_2 and reverse recovery of D_1 and D_2. There are no turn-on loss in this mode, since the diodes are conducting at MOSFET turn-on, hence the turn-on occurs at negligible voltage.

The derivation of the losses is presented in Appendix A and the resulting equations are listed in (3.20)-(3.27).

$$P_{\text{M1,cond}} = \frac{D-\tau_{\text{D}}}{3}\left(I_{\text{x}}^2 + I_{\text{x}}\hat{I}_{\text{L}} + \hat{I}_{\text{L}}^2\right) R_{\text{ds,on}} \tag{3.20}$$

$$P_{\text{M2,cond}} = \frac{1-D-\tau_{\text{D}}}{3}\left(\check{I}_{\text{L}}^2 + \check{I}_{\text{L}}I_{\text{y}} + I_{\text{y}}^2\right) R_{\text{ds,on}} \tag{3.21}$$

$$P_{\text{D1,cond}} = -\frac{1}{2}\left(\check{I}_{\text{L}} + I_{\text{x}}\right)\tau_{\text{D}}V_{\text{F}} \tag{3.22}$$

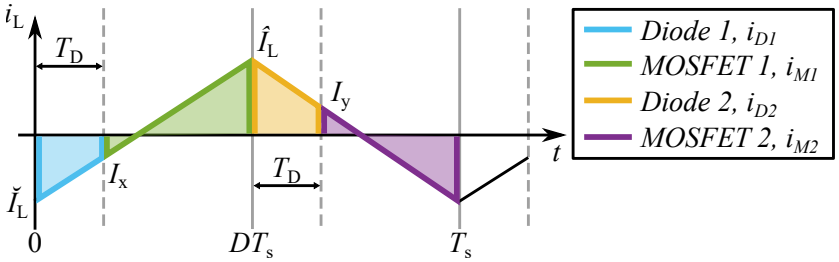


Figure 3.7. Indication of which semiconducting devices conduct during each time interval.

$$P_{\mathrm{D2,cond}} = \frac{1}{2}\left(\hat{I}_{\mathrm{L}} + I_{\mathrm{y}}\right)\tau_{\mathrm{D}} V_{\mathrm{F}} \tag{3.23}$$

$$P_{\mathrm{M1,sw}} = \frac{1}{2} V_{\mathrm{o}} \hat{I}_{\mathrm{L}} R_{\mathrm{g}} C_{\mathrm{gd}} \left(\frac{V_{\mathrm{o}} - \hat{I}_{\mathrm{L}} R_{\mathrm{ds,on}}}{V_{(\mathrm{plateau})}} - \left(1 + \frac{C_{\mathrm{gs}}}{C_{\mathrm{gd}}}\right) \ln\left(\frac{V_{\mathrm{gs(th)}}}{V_{(\mathrm{plateau})}}\right)\right) f_{\mathrm{s}} \tag{3.24}$$

$$P_{\mathrm{M2,sw}} = -\frac{1}{2} V_{\mathrm{o}} \check{I}_{\mathrm{L}} R_{\mathrm{g}} C_{\mathrm{gd}} \left(\frac{V_{\mathrm{o}} + \check{I}_{\mathrm{L}} R_{\mathrm{ds,on}}}{V_{(\mathrm{plateau})}} - \left(1 + \frac{C_{\mathrm{gs}}}{C_{\mathrm{gd}}}\right) \ln\left(\frac{V_{\mathrm{gs(th)}}}{V_{(\mathrm{plateau})}}\right)\right) f_{\mathrm{s}} \tag{3.25}$$

$$P_{\mathrm{D1,rr}} = \frac{1}{6} V_{\mathrm{o}} I_{\mathrm{rr}} \left(t_{\mathrm{rr}} - \frac{I_{\mathrm{rr}}}{\frac{\mathrm{d}i_{\mathrm{R}}}{\mathrm{d}t}} \right) f_{\mathrm{s}} \tag{3.26}$$

$$P_{\mathrm{D2,rr}} = \frac{1}{6} V_{\mathrm{o}} I_{\mathrm{rr}} \left(t_{\mathrm{rr}} - \frac{I_{\mathrm{rr}}}{\frac{\mathrm{d}i_{\mathrm{R}}}{\mathrm{d}t}} \right) f_{\mathrm{s}} \tag{3.27}$$

Loss Comparison

The losses are evaluated for each of the devices presented in Table 3.3. The evaluation is done at the values listed in Table 3.4.

Table 3.4. Operating point used for CCM loss estimation.

V_{i}	V_{o}	f_{s}	τ_{D}	I_{o}	D	$\hat{I}_{\mathrm{L}}$	$\check{I}_{\mathrm{L}}$
1 kV	5 kV	50 kHz	0.05	14.2 mA	0.8	233 mA	-94 mA

If the 1.7 kV devices are used a minimum of four devices should be serialized to handle the full output voltage of the converter. However if the 1.2 kV devices are used six switches in series are needed. This has been accounted for in the loss calculation. It is assumed that all switches in series turn on/off simultaneously at the speed of a single device and that they share the voltage equally. The result of the loss calculation is shown in Figure 3.8.

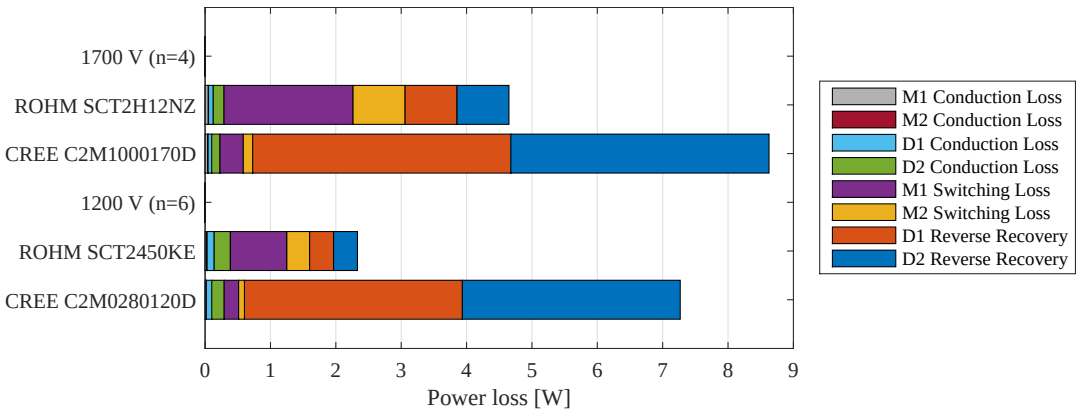


Figure 3.8. Loss estimation in CCM_0 for a range of commercially available SiC MOSFETs.

The configuration which experiences the lowest loss is the six serialized 1.2 kV ROHM SCT2450KE. Next best is the four serialized SCT2H12NZ. Generally the CREE devices have higher losses, mainly due to the high reverse recovery loss of the body diodes.

The relative losses of each switch is calculated in (3.28).

$$Loss = \frac{P_{\text{loss}}}{V_{\text{o}} I_{\text{o}} + P_{\text{loss}}} \times 100\% = \begin{cases} 9.5\% & , \text{ for } \text{C2M0280120D} \\ 3.2\% & , \text{ for } \text{SCT2450KE} \\ 11.1\% & , \text{ for } \text{C2M1000170D} \\ 6.3\% & , \text{ for } \text{SCT2H12NZ} \end{cases} \tag{3.28}$$

The losses constitute a large percentage of the output power. One way to decrease the losses is to operate the converter in discontinuous conduction mode, where some of the dominating switching losses are mitigated.

3.2.2 Discontinuous Conduction Mode

Although the duty cycle range, where the converter operates in DCM, is narrow (Figure 3.6), this range can be extended. This is accomplished by actively turning off M_2 when the current reaches zero. In practice this requires a zero-current detection circuit. It transforms the region of CCM_0 with $\lambda_0 > 0$ into a mode denoted DCM_+.

The inductor current for DCM_+ is illustrated in Figure 3.9, where the different colors indicate the conducting device.

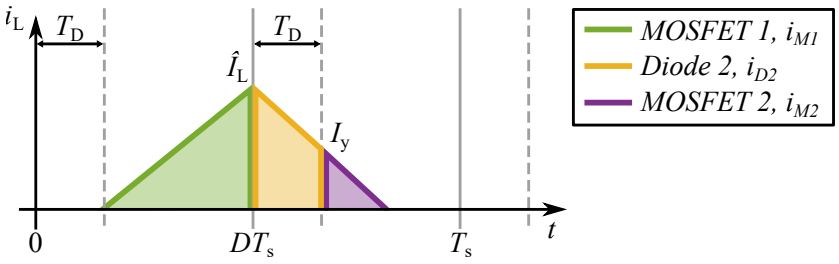


Figure 3.9. Indication of conducting semiconductor device during DCM_+.

The losses that occur are conduction loss in M_1, M_2 and D_2, switching loss in M_1 and reverse recovery loss in D_2. I.e. there is no conduction loss or switching loss in D_1 and no switching loss in M_2.

The loss derivation is presented in Appendix A and the equations are summarized in (3.29)-(3.33).

$$P_{\text{M1,cond}} = \frac{1}{3}(D - \tau_{\text{D}})\hat{I}_{\text{L}}^2 R_{\text{ds,on}} \tag{3.29}$$

$$P_{\text{M2,cond}} = \frac{1}{3}\left(-\frac{V_{\text{i}}}{V_{\text{i}} - V_{\text{o}}} D - \tau_{\text{D}}\right) I_{\text{y}}^2 R_{\text{ds,on}} \tag{3.30}$$

$$P_{\text{D2,cond}} = \frac{1}{2}(\hat{I}_{\text{L}} + I_{\text{y}})\tau_{\text{D}} V_{\text{F}} \tag{3.31}$$

$$P_{\text{M1,sw}} = \frac{1}{2} V_{\text{o}} \hat{I}_{\text{L}} R_{\text{g}} C_{\text{gd}} \left(\frac{V_{\text{o}} - \hat{I}_{\text{L}} R_{\text{ds,on}}}{V_{(\text{plateau})}} - \left(1 + \frac{C_{\text{gs}}}{C_{\text{gd}}}\right) \ln\left(\frac{V_{\text{gs(th)}}}{V_{(\text{plateau})}}\right)\right) f_{\text{s}} \tag{3.32}$$

$$P_{\text{D2,rr}} = \frac{1}{6}(V_{\text{i}} - V_{\text{o}}) I_{\text{rr}} \left(t_{\text{rr}} - \frac{I_{\text{rr}}}{\frac{\text{d}i_{\text{R}}}{\text{d}t}}\right) f_{\text{s}} \tag{3.33}$$

The losses are computed using the operating point listed in Table 3.5 and the results are shown in Figure 3.10. Again the ROHM devices have less loss than the CREE devices, which are dominated by diode reverse recovery. The relative losses of each switch are

$$Loss = \frac{P_{\text{loss}}}{V_{\text{o}} I_{\text{o}} + P_{\text{loss}}} \times 100\% = \begin{cases} 4.4\% & , \text{ for } \text{C2M0280120D} \\ 2.2\% & , \text{ for } \text{SCT2450KE} \\ 5.1\% & , \text{ for } \text{C2M1000170D} \\ 3.8\% & , \text{ for } \text{SCT2H12NZ} \end{cases} \tag{3.34}$$

Table 3.5. Operating point used for DCM_+ loss estimation.

V_{i}	V_{o}	f_{s}	τ_{D}	I_{o}	D	$\widehat{I}_{\text{L}}$
1 kV	5 kV	50 kHz	0.05	14.2 mA	0.52	213 mA

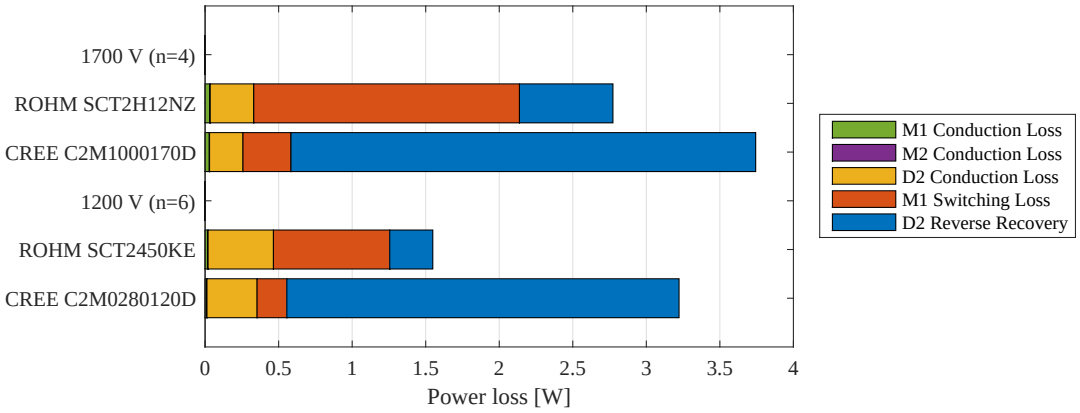


Figure 3.10. Loss estimation in DCM_+ for a range of commercially available SiC MOSFETs.

3.2.3 Variable operating conditions

The previous loss analysis was based on the nominal operating point. However the dust conditions and loading may change over time, meaning that the effective output resistance may vary. This implies a changing operating point, as was described in Section 1.1. Therefore the losses for changing operating conditions are presented in this section.

The plots of Figure 3.11 show the losses of the different components at different operating conditions, represented by output current (i_{o}). The output voltage is kept constant at the nominal 5 kV for this analysis.

For the entire current range (0 to 17 mA), the ROHM devices are superior to the CREE devices. However, this changes for larger current values, which are not treated here, because it is beyond the rated output current. In the CCM_0 mode, the power loss level is almost constant for changing current. This means that the efficiency is very poor at low current values and improves as the current increases. In the DCM_+ mode the losses are always lower than the corresponding losses in CCM_0.

The conclusion is that for the specified operating range the converter should work in DCM_+ mode, because of the lower losses when compared with CCM_0. The device chosen

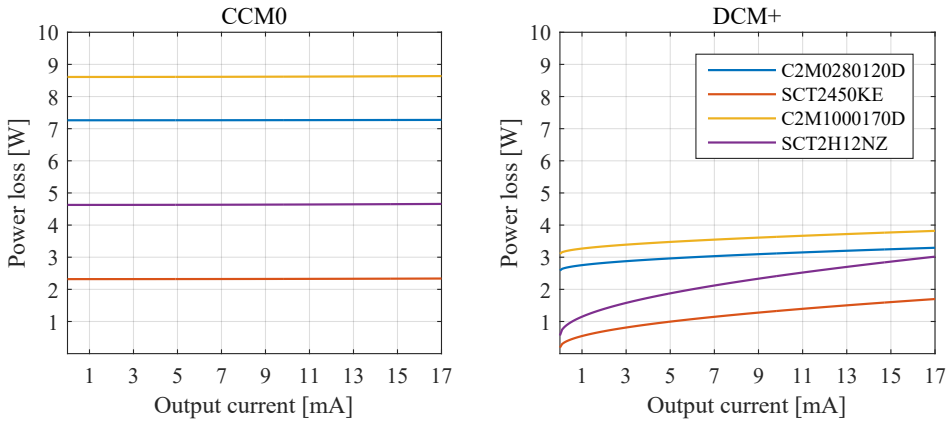


Figure 3.11. Switching and conduction loss of different components versus operating conditions for CCM_0 and DCM_+.

for further use in the project is the ROHM SCT2H12NZ because of its relatively low losses, while it only requires four devices in series to reach the rated voltage.

3.3 Control Strategy

Although the losses are reduced in DCM operation, the bidirectional functionality of the converter is lost, since it is essentially operated as a unidirectional boost converter. However it is possible to obtain bidirectional operation through a control strategy, which alternates between DCM_+ when power is supplied to the load and CCM_- when power should be extracted from the load. The concept for this control strategy is explained in this section and verified through simulation.

The control structure is visualized in Figure 3.12. The output voltage is subtracted from the voltage reference to give the error, which is fed into the controller. The controller depends on the desired mode, i.e. DCM_+ or CCM_-. The zero order hold (ZOH) models the hold of the discrete time duty cycle. A saturation block limits the duty cycle between the minimum and maximum allowable value. The duty cycle is then compared to a triangular waveform to convert it into a pulse width modulation (PWM) signal for S_1. This PWM signal is inverted for S_2. Dead time is applied to both PWM signals. A zero-current detection signal turns off the PWM for S_1 through an AND gate.

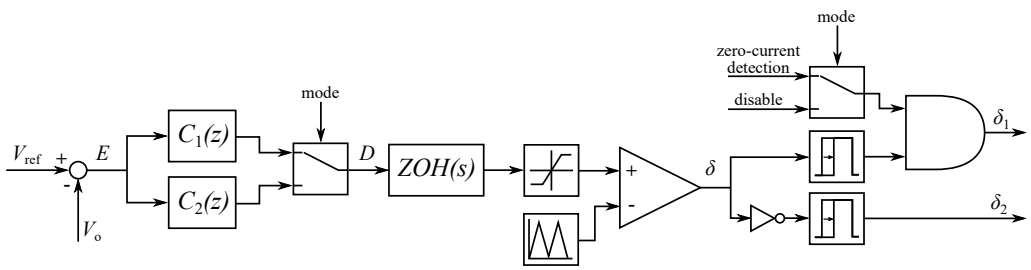


Figure 3.12. Control structure.

3.3.1 Controller

When designing the controller, $C(z)$, Figure 3.12 is simplified as shown in Figure 3.13. This is a standard feedback loop where G_{dv} is the control-to-output transfer function. A delay is introduced due to the fact that a change in duty cycle is not updated until the next switching period.

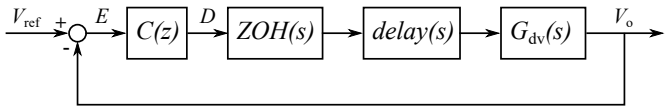


Figure 3.13. Simplified control structure.

G_{dv} is derived and discretized in Appendix B. The resulting discrete transfer function, including the zero order hold and the delay is

$$G_{\mathrm{dv}}(z) = \begin{cases} \dfrac{62.3}{z(z-0.989)} & , \text{ for } \mathrm{DCM}_+ \\ \dfrac{-320.8(z+0.49)}{z(z^2-1.98z+0.10)} & , \text{ for } \mathrm{CCM}_- \end{cases} \tag{3.35}$$

The controllers are designed in Appendix B using Ragazzinis method, where the desired closed loop transfer function, $F(z)$ is defined and the controller is designed to obtain this response. The desired closed loop transfer function is

$$F(z) = \begin{cases} \dfrac{b_0}{z(z-p_1)} & , \text{ for } \mathrm{DCM}_+ \\ \dfrac{b_0(z-z_1)}{z^2(z-p_1)} & , \text{ for } \mathrm{CCM}_- \end{cases} \tag{3.36}$$

In DCM_+ the desired transfer function is a second order response with one pole at zero in order to obtain a proper controller transfer function. In CCM_- the G_{dv} zero in the left half plane (LHP) is included in $F(z)$, since it will cause oscillations if canceled. The order of the denominator is increased by one due to the higher order of G_{dv}. b_0 is chosen to give zero steady state error and p_1 is determined to give the desired time constant, which is equal to the sample time, $T_{\mathrm{z}} = 20$ μs.

The controller transfer function is thus calculated directly by

$$C(z) = \frac{1}{G_{\mathrm{dv}}(z)} \frac{F(z)}{1-F(z)} = \begin{cases} \dfrac{0.0101z(z-0.99)}{(z-1)(z+0.63)} & , \text{ for } \mathrm{DCM}_+ \\ \dfrac{-0.0013z(z^2-1.98z+0.10)}{(z-1)(z^2+0.63z+0.21)} & , \text{ for } \mathrm{CCM}_- \end{cases} \tag{3.37}$$

3.3.2 Simulation

A PLECS simulation is constructed based on the circuit diagram of Figure 3.2 and the control diagram of Figure 3.12. The simulation is included on the attached CD [1].

A voltage of 2.5 kV with superimposed voltage pulses of 2.5 kV is fed to the system as the reference voltage. The resulting voltage and current waveforms are depicted in Figure 3.14. On the left hand side a zoomed view of a constant reference region is shown. The inductor current shows clearly the DCM operation.

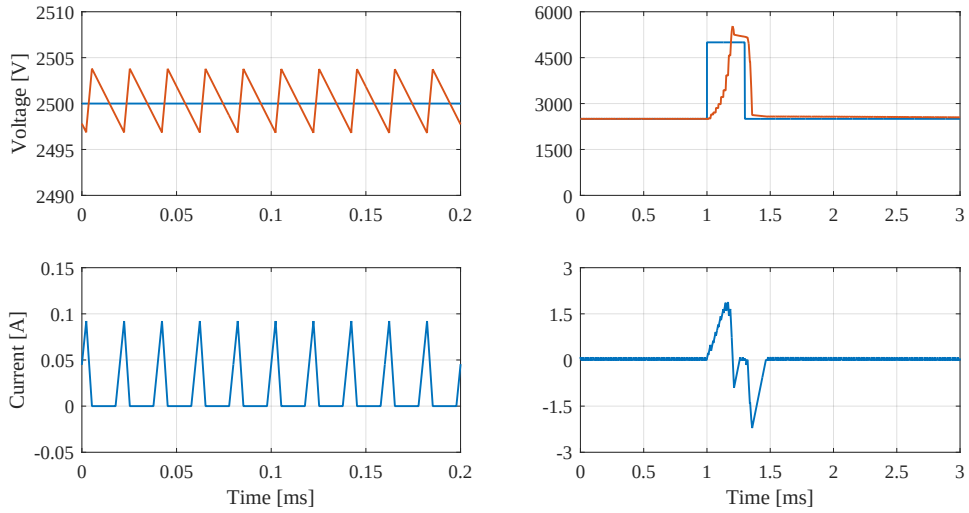


Figure 3.14. Simulated voltage (top) and current (bottom) waveforms for constant reference voltage (left) and pulsed voltage reference (right)

On the right a voltage pulse is shown. In order for the converter to deliver enough energy to the load to rapidly increase the voltage, the converter enters CCM_+, which can be seen in the current plot in Figure 3.14. However the CCM_+ mode of the synchronous boost converter has an inherent right half plane (RHP) zero, which causes the voltage to spike to 8 kV when the duty cycle is suddenly decreased. Because of this effect the controller gain is reduced by a factor of 0.05, which limits the voltage spike to 5.5 kV as shown in Figure 3.14.

Right Half Plane Zero

When the voltage becomes higher than the reference, the controller decreases the duty cycle. In CCM_+ this causes an initial increase in the energy delivered to the load instead of the expected decrease. This is due to the occurrence of a right half plane (RHP) zero in the CCM_+ transfer function. The electrical explanation of this phenomenon is that the integral of the current conducted by S_2, shown in Figure 3.15, is the charge delivered to the ESP.

If the voltage of the output is measured as being too high, the duty cycle must be decreased as seen from (3.4)-(3.6). However, as depicted in Figure 3.15, when the duty cycle is

[1] /PLECS/

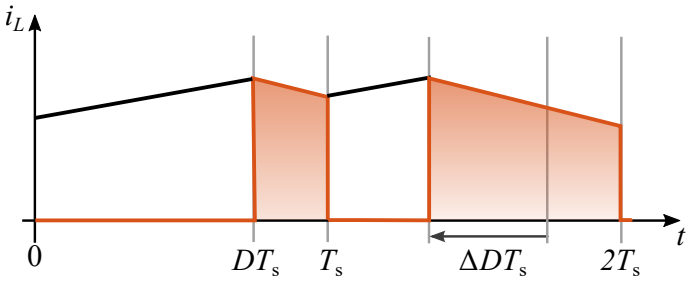


Figure 3.15. A decrease in duty cycle of the synchronous boost in CCM_+ causes an initial increase in output voltage.

decreased in the following switching cycle, by ΔD, the amount of charge delivered to the output is initially increased resulting in increased output voltage. This behaviour is the effect of a RHP zero in the control to output voltage transfer function. [Lynch, 2006]

The conclusion of the PLECS simulation is that bidirectional power flow is possible, even when CCM_0 ($\lambda_0 > 0$) is substituted with DCM_+. The voltage spike due to CCM_+ is not an issue caused by the forced DCM_+ operation, but is an effect of the increased continuous inductor current to rapidly charge the voltage of the output.

Chapter 4

Series Connection of SiC MOSFETs

Series connection of semiconducting devices is used to increase the blocking voltage of a switch. Deviations in device parameters, mismatching of gate driving signals or both, result in an unequal distribution of voltage across a string of devices. This leads to unequal power loss distribution or failure of devices which are exceeding their individual blocking voltage. Additional circuitry is required to distribute voltages equally among the devices during both transients and steady state operation.

Passive circuitry of resistors in parallel with each device is used to compensate for voltage imbalances during steady state operation. This solution is superior in performance, cost and size [Dimopoulos and Munk-Nielsen, 2013]. Transient voltage balancing is more challenging and numerous techniques are proposed to compensate voltage imbalances during turn-on and turn-off. However, simultaneously achieving a fast, efficient and high voltage blocking switch based on a string of devices is difficult to attain.

4.1 Methods for series connection of devices

The following section investigates suitable techniques for serialization of SiC MOSFETs. A literature study of serialization methods is performed. Most methods available in research describes methods to serialize Si IGBT devices, but the performance of each method for SiC MOSFETs is presented when available. A suitable method is chosen for use in this project, its operation is explained and component values are calculated.

4.1.1 Passive snubber circuits

The passive snubber circuit is the most popular technique used for series operation of devices [Shammas et al., 2006]. A resistor-capacitor (RC) or resistor-capacitor-diode (RCD) circuit is connected in parallel with each device, as shown in Figure 4.1. The snubber circuit shapes the transient waveform of each device to minimise voltage imbalances, but slightly increases the switching time. Passive snubbers reduce switching losses within each device by shaping of the waveforms, but some losses are moved to the snubber circuit itself. Its simple design and straight-forward implementation is advantageous and offers high reliability.

The method is tested by [Vechalapu et al., 2015] for two series connected 1.7 kV SiC MOSFETs in a double pulse test (DPT). A DPT consists of a device under test (DUT)

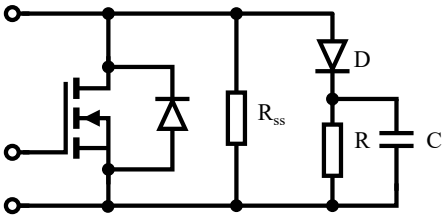


Figure 4.1. Passive RCD snubbers are used to shape switching trasients of series connected devices, while resistors ensure steady state voltage balancing.

in series with a parallel connection of an inductor and a free-wheeling diode (For this case the DUT is the string of series connected SiC MOSFETs). In the DPT the current is ramped up through the inductor to a predetermined level. By turning the DUT on and off, the inductor current is switched through the DUT. This reveals the waveforms during switching. Waveforms are analyzed to reveal switching times and losses of the device, used to evaluate the performance of the switch. The RCD snubber results in good transient behaviour with reduced oscillation and voltage imbalances. The results of [Vechalapu et al., 2015] are shown in Figure 4.2. The static voltage balancing performance ($SVBP$) is evaluated by comparing each switch voltage (v_j) with the desired off-state voltage of each switch:

$$SVBP(j) = \frac{v_j}{\frac{1}{n}\sum_{j=1}^{n} v_j} \tag{4.1}$$

where n is the number of serialized switches. The voltage over switch one in the off state is 928 V and the voltage on switch two is 840 V, meaning that switch one is blocking 105% of what it should, i.e. 884 V (half of the full voltage), and switch two is blocking 95% of what it should. Compared with results without a snubber, the $SVBP$ is corrected from 118 % and 82 % of switch one and two, respectively. However, the main focus of the paper is on reduction of voltage overshoot and oscillations during switching transients.

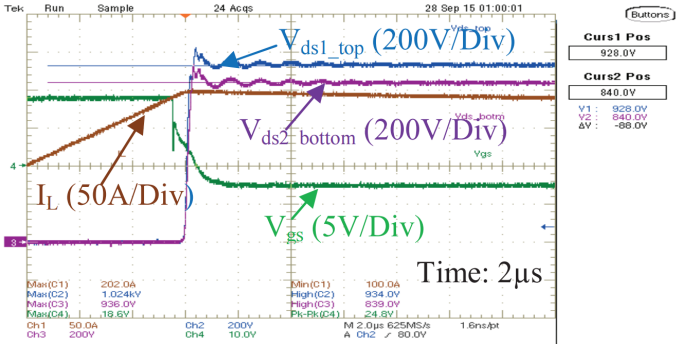


Figure 4.2. Turn off transient of two serialized SiC MOSFETs with snubbers [Vechalapu et al., 2015].

A method is proposed by [Wu et al., 2014], which uses RCD snubbers for balancing of transients. In this method the external driving signals for each stacked device is replaced by a cascaded structure using only a single external gate signal to turn on the bottom device. This technique removes the requirement of isolated and synchronous gate driving

signals for each series connected device. Therefore the string of series connected devices can be extended or reduced without any modifications to the control circuits. [Wu et al., 2014] test a string of three serialized 1.2 kV SiC MOSFETs in a DPT with a DC-link voltage of 2.4 kV. The results are shown in Figure 4.3. The voltage waveform of switch three (V_{dsQ3}) has been estimated from the original data in Figure 4.3, this has been done by subtracting the switch one and switch two waveforms from the full voltage waveform. Switch one, two, and three are blocking 650 V, 590 V, and 1070 V, respectively just before the turn-on of Figure 4.3(right). This corresponds to $SVBP$ of 84%, 77%, and 139% of the expected 770 V.

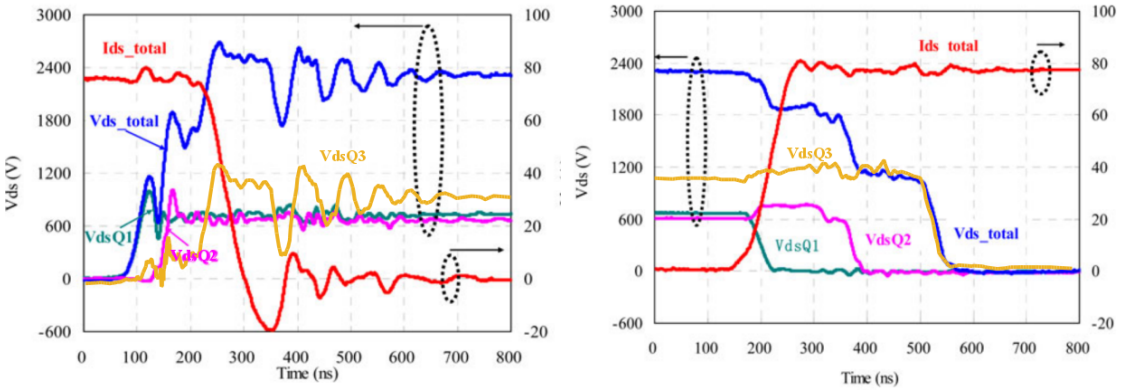


Figure 4.3. Turn-off (left) and turn-on (right) waveforms obtained by [Wu et al., 2014]. The voltage waveform of switch 3 (VdsQ3) has been added to the graphs.

4.1.2 Voltage clamping methods

The voltage clamping method uses zener diodes to limit the voltage across each switching device [Shammas et al., 2006]. The method is simple and uses no complex analogue circuits or control structures, as shown in Figure 4.4. An advantage is that if no voltage imbalances are present, the circuit will not interfere, thus the speed and losses are not altered [Chitta et al., 1997].

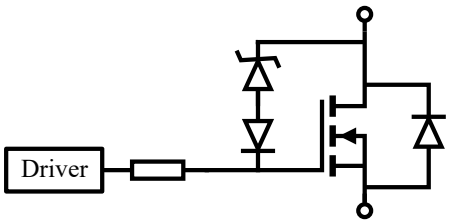


Figure 4.4. Zener diodes connected across the switch clamps the voltage.

No literature has been found which uses this solution for stacking SiC MOSFETs. An issue is that a device which turns on faster than the others, will be clamped at every switching cycle and experience a substantially higher power loss. However, it is not only the switching device itself which experiences higher stresses. Repetitive breakdown of the zener diodes causes current flow into the gate driving circuit. An advanced circuit is suggested in [Rüedi et al., 2009] to handle the repetitive current flows through the clamping

element. Even with the better current handling capabilities, the voltage clamping solution is still suggested as mainly operating as a protection feature rather than a means of balancing voltages across multiple devices. For this reason it can be argued that this method does not solve the issue of unbalanced devices, but mostly acts as a protection circuitry which is added as an additional feature of a gate drive circuit.

4.1.3 Active gate control methods

Active gate control methods are used to effectively control the transients of switching devices. Through closed-loop feedback the gate voltage is set to follow a voltage reference, as shown in Figure 4.5. A master-slave approach is presented in [Shao et al., 2013] where the voltage of the master device is used as a reference for the slave. The approach exhibits good transient performance, but the connection of more than two devices makes the control complex. Another approach decouples the devices and all stacked devices follow a common voltage reference profile. Good transient performance is shown in [He et al., 2011], without substantially increasing the overall energy loss. The cost and complexity of the circuitry is high, and requires high-speed and high-precision analog/digital circuitry for each stacked device [Shammas et al., 2006]. Si IGBTs typically have transient rise/fall times of 300 - 600 ns, while new commercially available SiC MOSFETs are in the range of 20-100 ns. The faster transients increases requirements for the feedback control circuitry and timing of control signals.

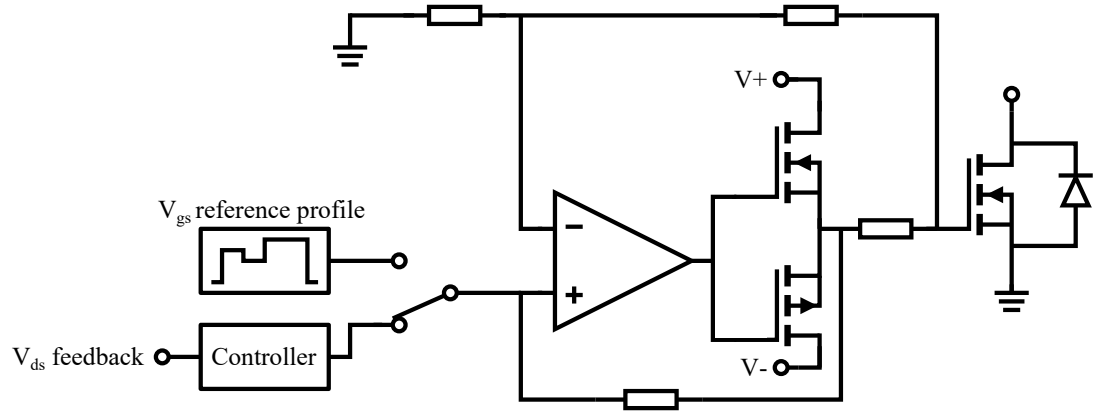


Figure 4.5. Active gate control scheme following either a reference voltage profile or feedback from a master device.

Active gate control is presented in [Palmer et al., 2015] to connect two SiC MOSFETs in series. The method proves to effectively remove voltage imbalances between the SiC MOSFETs in a DPT as seen from Figure 4.6, hence the static balancing is near perfect. However, the time it takes for balancing the voltages is above 5 μs, which is rather slow compared to the switching transients of a single device. The fast transients in the control signals induce unattractive ringing of the drain-source voltages, which is concluded to possibly cause issues if the string of switches is extended.

A similar approach is used in [Riazmontazer et al., 2015] for a single SiC MOSFET in a DPT. Results indicate that active gate voltage control of a SiC is possible. By adjusting $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ of the switching transients the oscillations during turn-on and turn-off are reduced, but in return switching time and losses increase substantially.

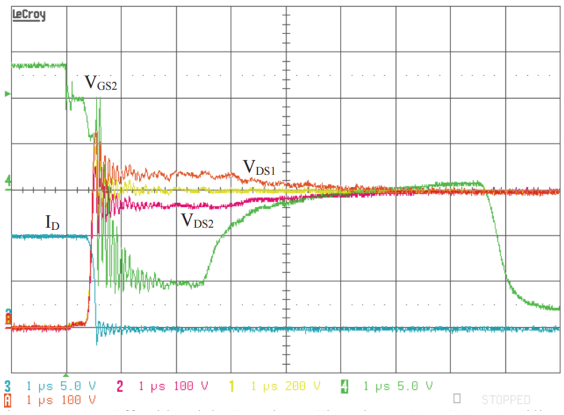


Figure 4.6. Turn-off transient of two serialized SiC MOSFETs with active gate control [Palmer et al., 2015]

4.1.4 Gate signal balancing

A method to balance the voltage and current of each distinct gate driver unit is presented in [Dimopoulos and Munk-Nielsen, 2013]. The method uses transformer cores to magnetically couple all the gate wires. This attenuates the effect of asynchronous gate drive signals without lengthening the total commutation time. The main disadvantage is that the method does not cope with deviating parameters of the device. The circuit may become bulky by the introduction of transformer cores within the gate drive circuit itself [Shammas et al., 2006], which generally is preferred to have as small a current loop as possible. The performance is limited as new parasitic components are introduced. Parasitic capacitance between transformer windings cause common mode currents to distort the gate balancing [Dimopoulos and Munk-Nielsen, 2013]. An issue which is likely to increase due to the faster switching speed and higher voltages per stacked device of SiC MOSFETs.

The parasitic coupling between gate signals is removed by a gate signal delay control scheme presented in [Abbate et al., 2010]. In this method the off-state voltage is measured and fed back to a digital control system which adjusts the gate signals. A switch which turns off faster has its gate signal slightly delayed to follow the other switches with slower characteristics, as illustrated in Figure 4.7.

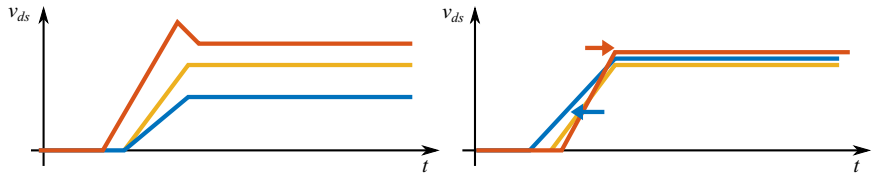


Figure 4.7. Adjusting delay of gate signals ensures balanced voltage during transient and steady state.

The advantage is that the overall commutation time is not increased, and that the gate driver circuit does not experience increased losses. The disadvantage is that it requires accurate and high speed measuring circuits, and the timing of the gate signals must have low jitter between each switching cycle. Compared with other methods the complexity of the control circuits is high, which in turn threatens the reliability of the

system [Shammas et al., 2006]. No literature has been found which uses these solutions for stacking SiC MOSFETs.

4.2 Selection of method

It is decided to use the RCD snubber based solution proposed in [Wu et al., 2014] utilizing the cascaded driving structure with only a single external gate signal. The reason is that the snubber based solutions show superior performance in regards to balancing transients and reducing oscillations of series connected SiC MOSFETs. Furthermore the complexity of the control circuit is simpler, potentially securing a more reliable and robust circuit. Also, the circuit offers a modular structure, as more switches can be inserted in the string without making any modifications to the control circuit. This allows the system to be extended if it should be used at higher voltage levels later on.

The poor static voltage balancing in the results presented by [Wu et al., 2014], is an issue which is to be solved. However, limited description of the problem and sizing of the components in the circuit is presented in the paper. Solving the issue requires a full investigation of the circuit operation, and dimensioning of components.

Another disadvantage of the method is the increased switching speed, compared with driving all switches simultaneously with synchronized gate signals. However, one of the main issues of SiC MOSFETs is to handle and reduce the oscillations caused by the high $\mathrm{d}v/\mathrm{d}t$. This is highlighted in [Palmer et al., 2015] where the fast transients cause oscillations, which are continuously increased as more devices are connected in series. The main purpose of the active gate control of a single SiC MOSFET in [Riazmontazer et al., 2015] is to control and decrease the $\mathrm{d}v/\mathrm{d}t$ to reduce oscillations and electromagnetic interference (EMI). [Vechalapu et al., 2015] shows that an increased RC-constant (which increases switching time) effectively reduces the switching turn-off losses because oscillations are damped. Keeping a constant $\mathrm{d}v/\mathrm{d}t$ similar to one switch, instead of adding the $\mathrm{d}v/\mathrm{d}t$ together for all switches, as illustrated in Figure 4.8, may prove to reduce voltage overshoot and oscillation issues reported as one of the factors limiting the series connection of SiC MOSFETs.

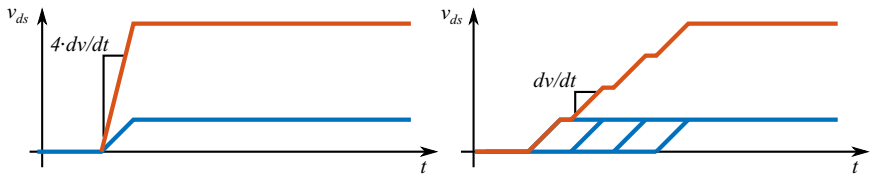


Figure 4.8. All switches turning off simultanously (left) produces large dv/dt, compared with cascaded turn off keeping constant dv/dt.

4.3 Analysis of gate drive operation

The following section explains the operation of the chosen series connection method. The gate drive circuit proposed in [Wu et al., 2014] is shown in Figure 4.9. The string is extended to include a total of four switches connected in series.

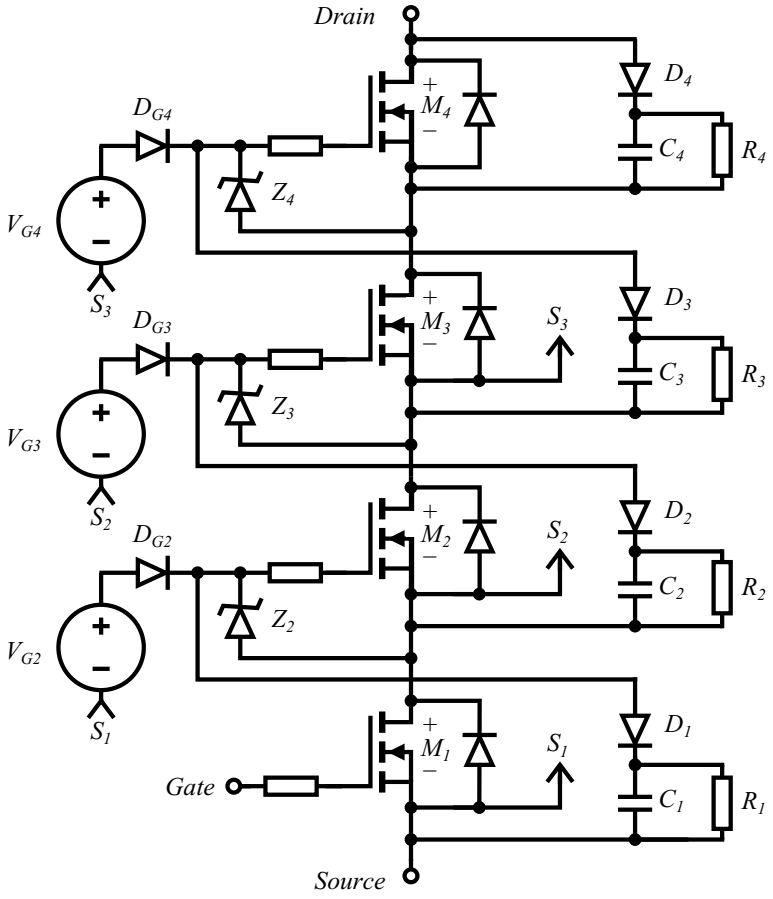


Figure 4.9. Series connected switches with a single external gate driver.

4.3.1 Turn-on sequence

State 1 Initially all the SiC MOSFETs are turned off. All clamping capacitors C_1, C_2, C_3 and C_4 are charged to one fourth of the total voltage across the string, because of the static voltage balancing resistors R_1, R_2, R_3 and R_4. The gate drive diode D_{G2} is reverse biased by the voltage $V_{\mathrm{G2}} + V_{\mathrm{Z2}} - V_{\mathrm{M1}}$, D_{G3} is reverse biased by $V_{\mathrm{G3}} + V_{\mathrm{Z3}} - V_{\mathrm{M2}}$ and D_{G4} is reverse biased by $V_{\mathrm{G4}} + V_{\mathrm{Z4}} - V_{\mathrm{M3}}$. A positive drive signal is now given to the gate of M_1.

State 2 The voltage across M_1 starts to decrease, and the stored charge in the junction capacitance of D_{G2} discharges through Z_2. The voltage of the zener Z_2 gradually increases, but has not yet reached the gate-source threshold voltage of M_2.

State 3 As $V_{\mathrm{G2}} - V_{\mathrm{D2}} - V_{\mathrm{M1}}$ becomes higher than the gate-source threshold voltage of M_2, it starts to turn on and its voltage gradually decreases. Now the junction capacitance of D_{G3} discharges through Z_3, which gradually increases the gate-source voltage of M_3, but not yet above its threshold.

State 4 The voltage $V_{\mathrm{G3}} - V_{\mathrm{D3}} - V_{\mathrm{M2}}$ is now higher than the gate-source threshold voltage of M_3, which now starts to turn on and its voltage drops. The junction capacitance of

D_{G4} discharges through Z_4, increasing the gate-source voltage of M_4, but it has not yet crossed the threshold voltage.

State 5 M_4 turns on when the voltage $V_{G4} - V_{D4} - V_{M3}$ becomes higher than its gate-source threshold voltage. After M_4 is completely turned on the turn-on process of the whole circuit is over.

4.3.2 Turn-off sequence

State 6 All the SiC MOSFETs are in their on state and a current flows from the drain to the source terminal. There is still a voltage stored on capacitors C_1, C_2, C_3 and C_4, but they are slowly discharging through the parallel resistors R_1, R_2, R_3 and R_4, respectively. A negative drive signal is given to the gate of M_1.

State 7 The voltage across M_1 starts to increase. The voltage of zener Z_1 decreases, but $V_{G2} - V_{D2} - V_{M1}$ is still higher than the gate-source threshold voltage of M_2.

State 8 As $V_{G2} - V_{D2} - V_{M1}$ drops below the gate-source threshold voltage, M_2 turns off and Z_2 is forward biased. C_1 starts being charged through D_1. The voltage across zener Z_3 begins to decrease, but because $V_{G3} - V_{D3} - V_{M2}$ is still above the threshold voltage M_3 has not yet started to turn off.

State 9 The gate-source voltage of M_3 drops below its threshold, and starts to turn off. Z_3 is forward biased. Z_4 decreases, but M_4 is still above its gate-source threshold voltage.

State 10 Voltage V_{M3} continuously rises and $V_{G4} - V_{D4} - V_{M3}$ becomes lower than the gate-source threshold voltage of M_4. M_4 starts to turn off. Zener Z_4 is forward biased and ensures M_4 turns off completely. At this state the gate drive diodes D_{Gj} are all reverse biased by the voltage $V_{Gj} + V_{Zj} - V_{M(j-1)}$ for $j = 2, 3, 4$. The voltages across all MOSFETs are balanced by the resistors R_1, R_2, R_3 and R_4.

4.4 Simulation and RCD-selection

In the following section the gate drive circuit is simulated using LTSpice IV[1]. The LTSpice schematic used for the simulation, using a model of the ROHM SCT2H12NZ SiC MOSFET is available on the CD [2]. In this way the circuit is examined using actual component values and properties, including SiC MOSFET delays and rise/fall times.

The waveforms of turn off and turn on are shown in Figure 4.10 and 4.11, respectively. This highlights how the switches turn on and off cascaded. The total turn on and off time is increased by the rise/fall time of each switch as well as the turn on/off delay times.

The RCD snubber is designed in the following manner. In general the RCD snubber should be able to withstand the voltage across each switch. The switching currents and voltages

[1] Available for download at http://www.linear.com/designtools/software/#LTspice

[2] `LTSpice/voltage_cascaded_dpt.asc`

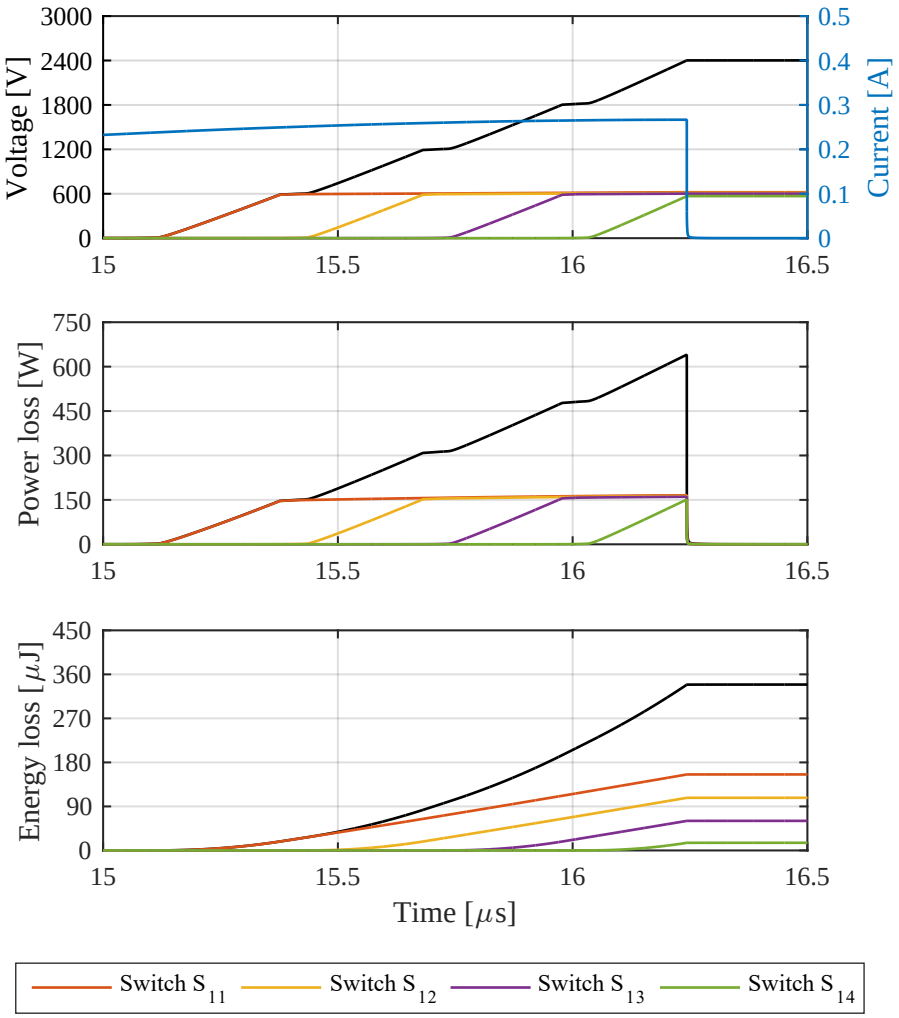


Figure 4.10. Voltage, current, power loss and energy loss as function of time during turn off.

through the circuit have fast transients, thus it is preferred to minimize inductance by using SMD components for a compact design.

Ideally the capacitor holds a constant voltage, which is equally divided between each switch in the string. However, during turn-off as soon as the driven MOSFET M_1 is completely turned off, the current of the inductor starts to conduct through its RCD snubber. The current is conducted through the snubber circuit until all of the remaining MOSFETs are off. The first switch in the string turns off first and its RCD snubber therefore experiences the current for the longest period.

Likewise, during turn-on current starts to flow as soon as the driven MOSFET is turned on. This current is conducted through the RCD snubber of the MOSFETs that are still off. Thus in this case it is the last MOSFET in the string which experiences the largest increase in capacitor voltage.

The capacitor value must be chosen in such a way that the voltage does not increase too much to cause unwanted voltage spikes during the switching transient. Ultimately, the

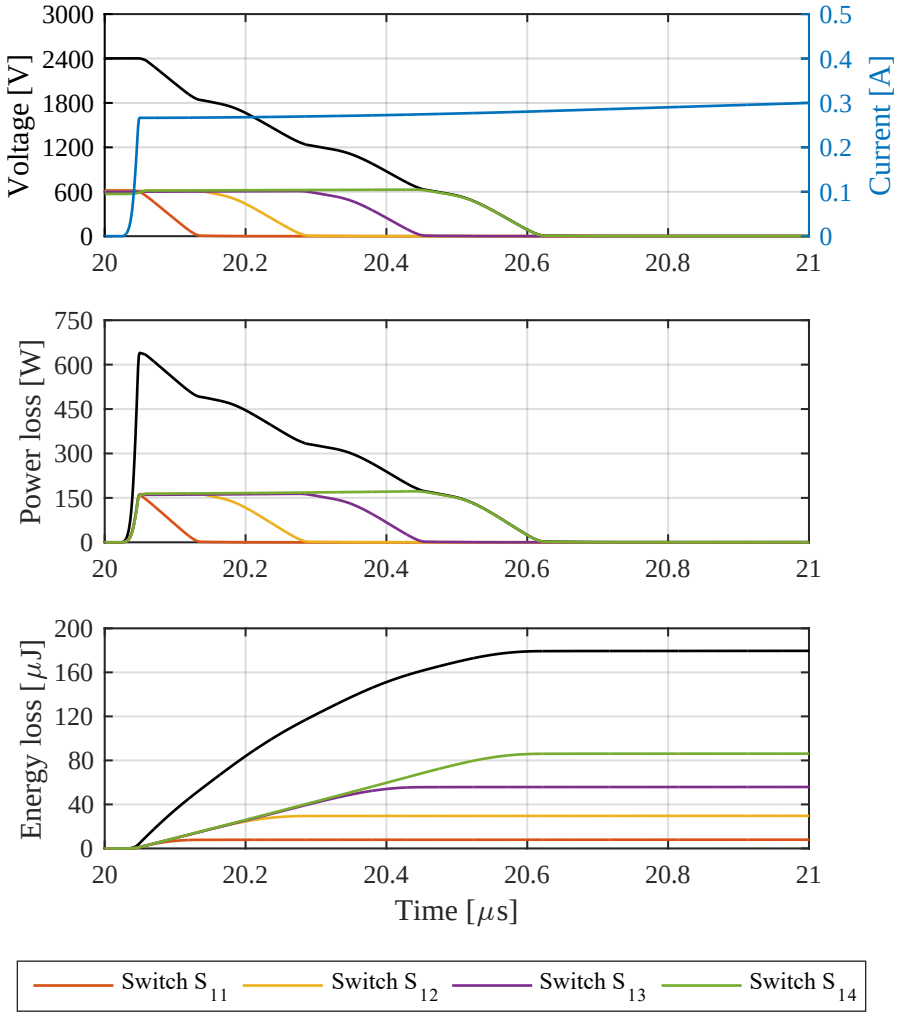


Figure 4.11. Voltage, current, power loss and energy loss as function of time during turn on.

capacitance must be high enough to ensure that voltage does not increase to a level which violates the breakdown voltage of the switch. The capacitor should also be large enough to not drop significantly in voltage during the MOSFET on period, but from the LTSpice simulations this is found to be less of an issue, because the resistor in parallel is large. Shown in Figure 4.10 is that the time from M_1 is completely off and until the end of the switching period is 880 ns. At the operating point determined in Chapter 3, the current at the transition is $\widehat{I}_{\mathrm{L}} = 213$ mA. A voltage increase of 25 V is deemed acceptable for the operation of the circuit. Assuming that the current is constant during the 880 ns, the required capacitance is calculated as.

$$C \geqslant \widehat{I}_{\mathrm{L}} \cdot \frac{\Delta t}{\Delta V} = 213\,\mathrm{mA} \cdot \frac{880\,\mathrm{ns}}{25\,\mathrm{V}} = 7.5\,\mathrm{nF} \tag{4.2}$$

This capacitance is achieved by three 22 nF C1808V223KDRACTU[3] SMD capacitors from Kemet in series. These have an internal voltage rating of 1000 V per device, but because the package is 1808 SMD, three are connected in series to avoid sparking between

[3]Datasheet available at http://docs-europe.electrocomponents.com/webdocs/1140/0900766b8114086f.pdf

soldering pads, that are only separated by 3 mm. In [John Kuffel, 2000,p. 83] the electric breakdown of air is given for negative voltages 3.36 kV/mm (for reference conditions temperature 20°C and air pressure 101.3 kPa). By a safety factor of eleven a minimum clearance of 300 V/mm is used in the entire layout. By connecting three 3 mm gaps in series a voltage rating of minimum 2700 V is obtained per device.

The resistor in the RCD-snubber ensures the voltage balancing in the off state. Any voltage imbalances on the capacitors due to the delay in switching are balanced. Thus a capacitor having a larger voltage dissipates its power through the resistor to return to balance. For the resistors three high voltage 0.5 W 2010 SMD resistors from Bourns CHV-series[4] are used, combined for a total resistance of 420 kΩ. The resistors are connected in parallel with the capacitors which hold a near constant voltage. For the simulation results presented in Figure 4.10 and 4.11, this results in an average power loss of

$$P = \frac{V^2}{R} = \frac{(600\,\mathrm{V})^2}{420 \cdot 10^3 \Omega} = 0.85\,\mathrm{W} \tag{4.3}$$

which is equal to 56 % of their rated power dissipation level. A lowered resistance value results in a larger power dissipation and a larger current through the snubber circuits during the off period. This means that voltage imbalances (either over or under the balanced voltage level) are attenuated faster as the resistance of the snubber is reduced.

Because of the rapid switching in the gate drive and snubber circuits fast switching Si diodes are chosen for both the gate drive diodes and the snubber diodes ($\mathrm{D}_{\mathrm{G}j}$ and D_j for $j = 2, 3, 4$ in Figure 4.9). Two 1200 V STTH112[5] diodes from STMicroelectronics are connected in series to fulfil the voltage rating. These diodes are chosen because of a relatively low reverse recovery current of $I_{\mathrm{rr}} = 0.25$ A. The STTH112 is a cheaper alternative to SiC Schottky diodes, which was also considered because of its fast transients, low reverse recovery and voltage capability.

[4]Datasheet available at http://docs-europe.electrocomponents.com/webdocs/13ff/0900766b813ff008.pdf
[5]Datasheet available at http://docs-europe.electrocomponents.com/webdocs/07bd/0900766b807bd120.pdf

Chapter 5

PCB Development and Test Setup Design

A method of series connecting SiC MOSFETs has been proposed in Chapter 4. Printed Circuit Boards (PCBs) are developed and tested, to evaluate the performance of the method experimentally. In the following chapter two main issues concerning the PCB development is treated. A modular layout structure is presented in Section 5.1. The gate driving technique presented in Chapter 4, requires supplied voltages at the gate of each SiC MOSFET. A discussion of available techniques to supply this voltage is given in Section 5.2. In Section 5.3 a description of the test setup is given. This highlights what auxiliary equipment and components are used to make the test setup operate, and what has been done to ensure safe operation.

5.1 Design for modularity

The concept of a modular design is to divide a complex system into smaller sub-systems. Units in a modular system are developed independently, while still fulfilling the overall functionality of the system. The series of switches presented in Section 4.3 have a structure which can be split into different parts that each fulfill a certain feature in the circuit. The choice to "design for modularity" adds an extra dimension to the development of the circuit, which must be incorporated early in the design process. But it has several advantages both during the development of a prototype and if the converter architecture is to be expanded for future use in an industrial application.

Modularity enables faster product development and allows larger variety in the function of the product [Vasawade et al., 2015]. This means that the sub-systems can be designed and developed one at a time and tested independently. If an error is detected in the design, only that sub-system needs to be modified, without the requirement for the entire system to be redone. Modularity allows each sub-system to be upgraded independently if features within that sub-system are to be improved. This is also an important feature for industry, as an existing system can have parts upgraded and improved, without having to reinstall an entire converter.

If designed for fast disassembly, a modular system also ensures ease of maintainability. This ensures that a failure is corrected relatively easy by replacement of a defective module, rather than replacing the entire unit [Foster, 2013,p. 199]. This is advantageous during the prototyping phase, because errors or faults inevitably occur. For industrial applications it also results in easier logistics, because the spare parts holding is reduced. Only a

number of smaller sub-modules need to be kept in stock, instead of keeping full systems as replacements [O'Connor and Kleyner, 2012,p. 152].

5.1.1 PCB layout concept

It is identified that the string of series connected switches can be divided into two kinds of sub-systems. The switch which is driven by a gate driving signal is one sub-system, while each remaining switch in the string is another type (further on labelled as "Non-driven", because they are not given an external drive signal). A concept diagram of the connections required between each module is illustrated in Figure 5.1.

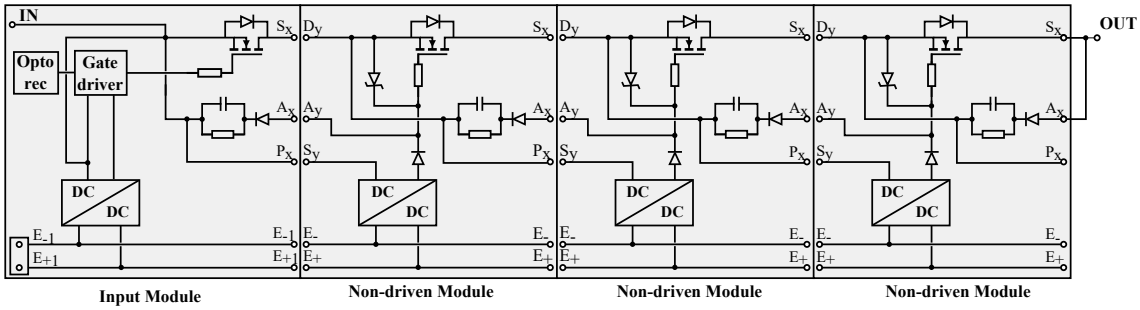


Figure 5.1. Concept drawing of the proposed modular PCB layout structure.

The string of devices can be extended during development. Thus initially the input module can be tested on its own, and during development of non-driven modules the string can be extended and tested. The non-driven modules are connected by bolts at the terminal points. A three-dimensional view of a non-driven board is developed using the PCB-editor KiCAD, as shown in Figure 5.2. The SiC MOSFET in its TO-3PFM package is located on the bottom-layer of the board. All PCB schematics and layouts developed in KiCAD are attached in Appendix D and E, respectively. Shown in Figure 5.1 and 5.2 is that voltages for the gates are supplied using DC/DC converters. The choice of this method is described in Section 5.2.

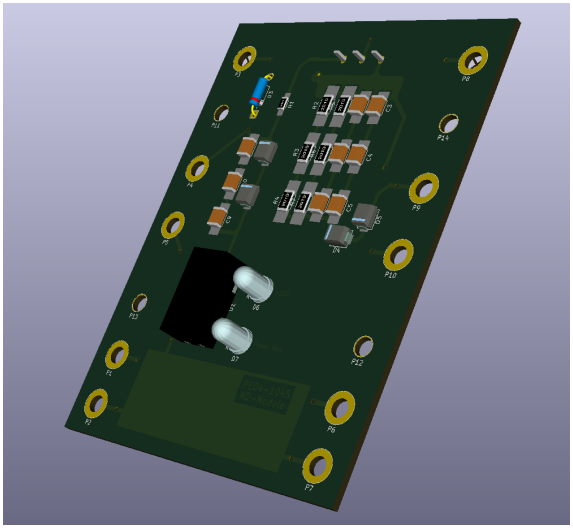


Figure 5.2. KiCAD 3D view of a Non-driven module.

5.2 Gate drive supply

The voltage supplies connected to the gate drive diodes in Figure 4.9, need a means of power source on their own. Each voltage supply is referred to different points, meaning that each source must be electrically isolated. The following section describes different solutions to the problem which have been considered for use in the project. The fast switching of relatively high voltage levels requires the solutions to exhibit high voltage isolation levels and low parasitic capacitance.

5.2.1 Commercially available DC/DC supplies

A solution is to use commercially available isolated DC/DC supplies, which are at a size allowing them to be directly integrated on the PCB. Murata Power Solutions, Traco Power and RECOM all offer DC/DC converters, such as the one shown in Figure 5.3, with isolation voltages in the range of 5 to 10 kV and parasitic capacitances of 4 to 20 pF.

Figure 5.3. RECOM R12P215SP isolated DC/DC power supply.

Increasing the isolation voltage and keeping the parasitic capacitance low requires a custom built solution. This is also required, if it is considered to expand the string of series connected switches to voltages more than the rated 6 kV for this project.

5.2.2 Flyback converter

Having the degree of freedom of choosing the voltage isolation level and parasitic capacitance, while maintaining a low complexity and cost can be achieved by building a flyback DC/DC converter, as shown in 5.4. By using such a design high voltage isolation levels can be achieved. The parasitic capacitance is shown to be kept as low as 10 pF, while still maintaining a relatively compact design [Nguyen-Duy et al., 2014].

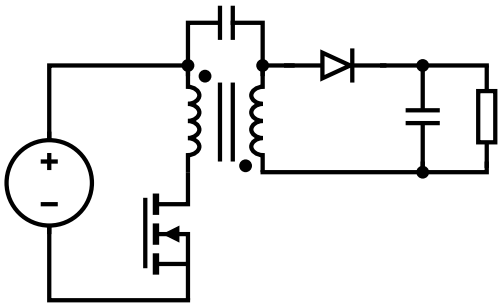


Figure 5.4. A DC/DC Flyback converter ensures high voltage isolation and low parasitic capacitance.

The advantage is that it only needs a single switch to be driven, and commercially available ICs, such as the LT8302, controls the switch without external gate drive signals. If two strings of four series connected switches are to be powered, a total of eight flyback converters are to be constructed. One way of reducing the required number of flyback converters, is to use the primary winding for several cores. Then a single primary winding is led through several cores, each with its own secondary output. An issue with this approach is that the leakage inductance in the primary side circuit increases with each added output. The switch is in series with this leakage inductance, which induces voltage spikes at each switching. For a single core at low power the voltage spikes are attenuated by a snubber circuit, but the voltage spikes can pose an issue as both power and inductances increase. The issue of voltage spikes is solved by using a two switch flyback topology. The complexity is increased because of the added switch, which also requires isolated driving signal [Murthy-Bellur and Kazimierczuk, 2010].

5.2.3 Power amplifier

The flyback topologies in Section 5.2.2 implies unidirectional magnetic flux in the transformer core. Such a solution does not fully utilize the core material. A full-bridge structure as shown in Figure 5.5 has the feature of bidirectional magnetic flux, which utilizes the magnetic core material, and suffer less from voltage spikes. The inductor of Figure 5.5 represents the primary side winding, which is fed through several transformer cores. On the secondary side of each core, a full-wave rectifier bridge produces a DC-voltage for the gate drive. [Nguyen-Duy et al., 2014]

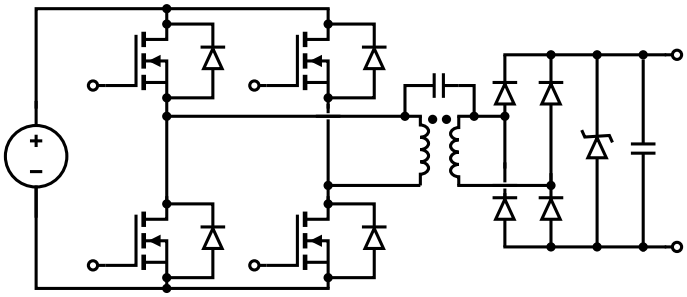


Figure 5.5. A fullbridge triangular current generator utilizes the core flux efficiently.

5.2.4 Selection of method

For the voltage rating at 6 kV the commercially available DC/DC supplies are within the range. A DC/DC supply such as the R12P215S/P[1] by RECOM has a parasitic capacitance rated from 1.5 pF to maximum 10 pF, and is tested for an isolation voltage of 6.4 kV. This isolation level is within the required for this project, and the parasitic capacitance is as low as reported for the custom built flyback solution. Additionally, the DC/DC solution is faster in development, when compared with custom built flyback or power amplifier solution. For this project the main focus is on the gate driving mechanism itself, and not on the gate drive supply. However, for expanding the operating voltage in the future an alternative supply mechanism must be implemented, but is beyond the requirements for this project.

[1]Datasheet available at http://www.farnell.com/datasheets/1842295.pdf

The string of MOSFETs is built using the designed modular structure as described in Section 5.1, and its gate voltages are supplied with the DC/DC supplies. A photograph of the finished string is shown in Figure 5.6

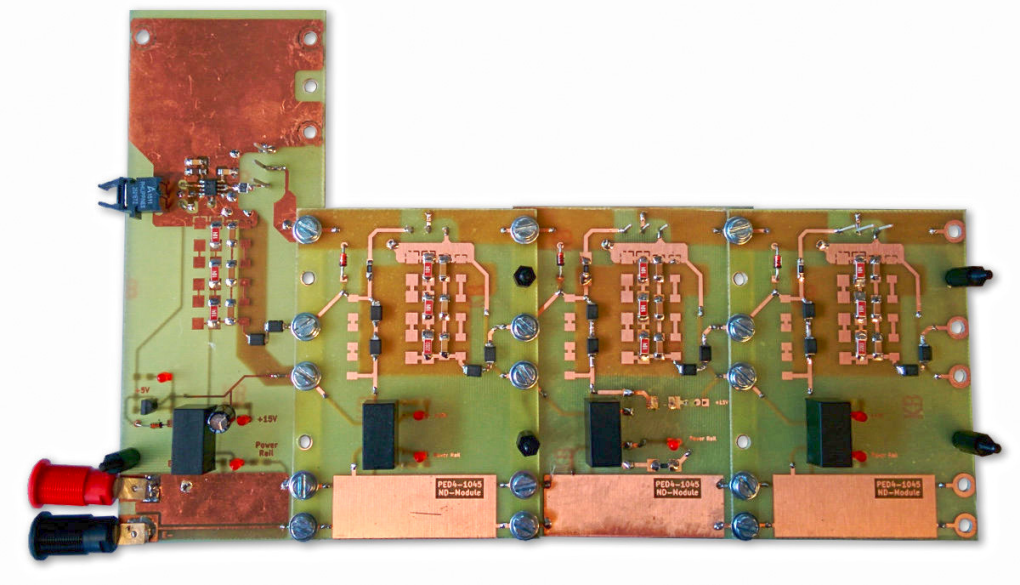


Figure 5.6. A photograph of the series connected SiC MOSFETs designed for modularity.

5.3 Description of test setup

The following section describes the laboratory test setup, its components and how they are interconnected. The test setup is described for the DPT, as used in Chapter 6. A diagram of the setup is shown in Figure 5.7.

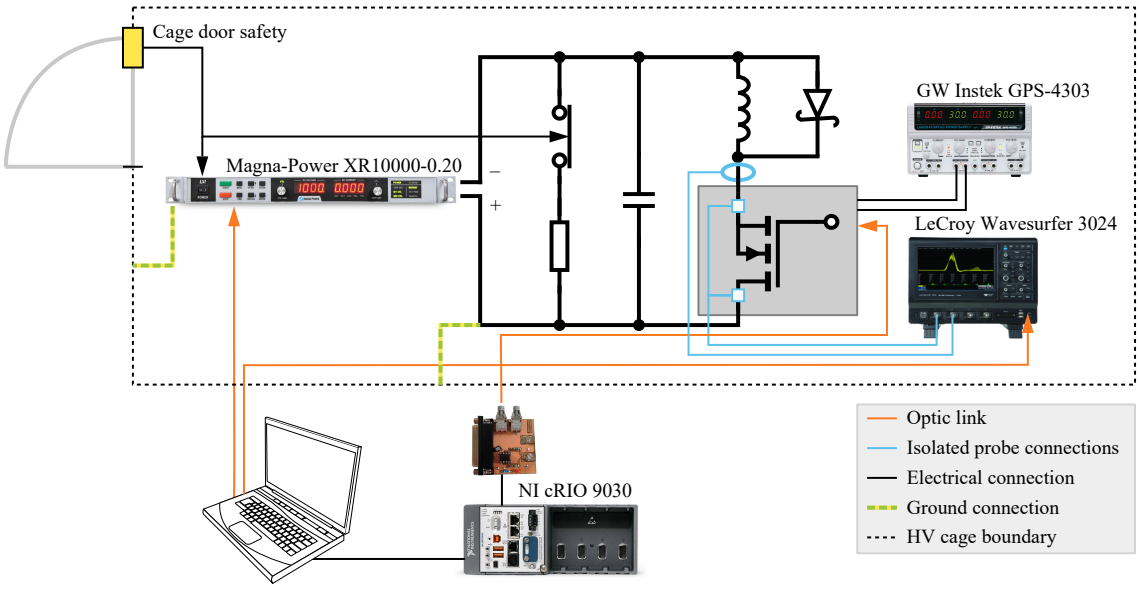


Figure 5.7. Diagram of the test setup used for the DPT.

A Magna-Power XR10000-0.20 delivers power to the main circuit of the test setup, and is designed for outputting negative voltage polarity. The power supply is connected to a DC-link busbar with a capacitor, to ensure a stable voltage supply for the DPT. In parallel to the capacitor is a discharging circuit. The Magna-Power supply and the discharging circuit is connected to the grid through a circuit breaker, controlled by the door to the high voltage cage. When the cage door is opened the circuit breaker opens and power is disconnected to the Magna-Power and the relay in the discharging circuit.

Connected to the DC-link is a high voltage inductor, with SiC Schottky diodes in parallel. This is connected in series with the tested MOSFET string. The gate supplies of the MOSFETs are powered by 12 V from a GW Instek GPS-4303 supply. Current and voltages of the MOSFET strings are measured by a LeCroy Wavesurfer 3024 oscilloscope. The test setup is controlled from outside the high voltage cage by a PC running LabVIEW. The PC is connected by Ethernet to the Magna-Power supply to power up the setup, through an optical link. The Ethernet-optical interface connection is achieved through a Korenix Jetcon 1501. The PC also sends input to the NI CompactRIO 9030 field-programmable gate array (FPGA) to output the gate signals for the MOSFET. The gate signals to the MOSFET board are also optically isolated. The Magna-Power supply and the NI cRIO are both controlled from a common LabVIEW program running on the PC. To acquire waveform data the PC is connected through Ethernet to the LeCroy Wavesurfer 3024 through a link which is optically isolated.

5.3.1 Power supply, DC-link and discharge

The Magna-Power XR10000-0.20 is capable of delivering a negative voltage up to 10 kV at an average current of 0.2 A. The power supply is controlled through Ethernet from the LabVIEW program running on the host PC, and is explained in detail in Appendix C.2. The high voltage cable to the power supply has a length of 3 m. To reduce stray inductance the power supply is connected to a DC-busbar. Additionally, this ensures that higher instantaneous currents can be supplied to the setup, without triggering the over current protection of the power supply. The capacitor connected to the DC-busbar is a E50.S34-204NTO with a capacitance of 202 μF and rated at a voltage of 3600 V.

The discharging circuit consists of four Arcol HS300 power resistors connected in series with a total resistance of 2300 Ω, each rated at a voltage of 2.5 kV. The high voltage relay is a Gigavac G62B741, rated at 25 kV and operated with a coil voltage of 12 V. The relay is normally-closed, which ensures that when power is disconnected the DC-link capacitor discharges through the power resistors. The door to the cage is locked while the setup is powered.

5.3.2 NI CompactRIO-9030

An NI CompactRIO-9030 is used to generate the gate signals for the MOSFET. This is done by programming the FPGA, as described in Appendix C.1.2. The program is developed using LabVIEW and is compiled to the FPGA, which during the test is also controllable from the host PC. The output of the gate signals is done through a NI 9401 digital input/output (I/O) module. The gate signals should be electrically isolated for safety reasons and to minimize noise. The MOSFET board inside the cage has an optic

receiver. An optic transmitting board, as shown in Figure 5.8, is developed to generate the optic gate signal. The schematic is attached in Appendix D. The transmitting board is supplied with 5 V from an external GW Instek GPS-4303 power supply. The board is mounted directly on the NI 9401 through a 25-pin DSUB connector.

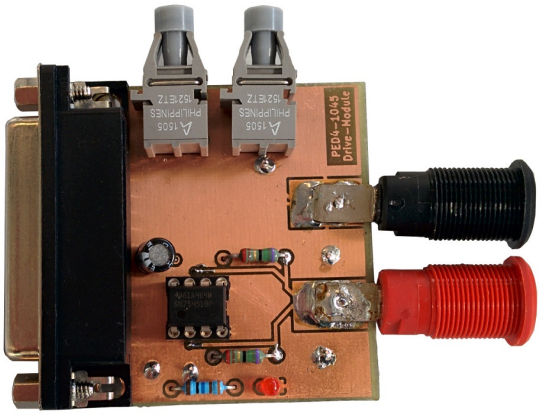


Figure 5.8. An optic link transmitter board with 25-pin DSUB connector for the NI 9041 digital I/O module.

5.3.3 Inductor and Schottky diodes

A high voltage inductor of 49 mH is supplied for the project by FLSmidth Airtech A/S, as shown in Figure 5.9.

Figure 5.9. Photo of the 49 mH high voltage air-coil inductor.

The inductor is an air coil, constructed for high voltage isolation and low parasitic capacitance. An air coil is advantageous because the performance of such an inductor is less affected by the current it caries or the frequency. Inductors utilizing ferrite materials suffer from core losses at increasing frequencies. Thus the fast switching dynamics (and the oscillations they produce) might be affected by non-linearities in the performance of the inductor. Additionally, ferrite materials saturate as magnetic flux density increases.

For the DPT, the free-wheeling diode consists of two 1.7 kV SiC CREE C3D10170 Schottky diodes connected in series. The advantage of using SiC Schottky diodes is that the reverse recovery current is low. A large reverse recovery current during the switching could substantially impact the current measured during the switching transients in the DPT. The load capacitance of the SiC Schottky diodes are varying in the range 41-827 pF, this relatively low capacitance helps fast turn on/off and reduces its influence on the results obtained of the SiC MOSFET string during the DPT.

Chapter 6

Double Pulse Test Results

The following chapter evaluates the performance of the voltage balancing capabilities of the selected serialization technique. The measured waveforms are compared with the results of the simulation in Chapter 4.

6.1 Analysis of switching transients

A DPT is done using the test setup presented in Chapter 5. A test is done at a voltage level of 2400 V, and the inductor current is ramped up to 250 mA. The turn-off drain-source voltage, drain current and energy loss is shown in Figure 6.1.

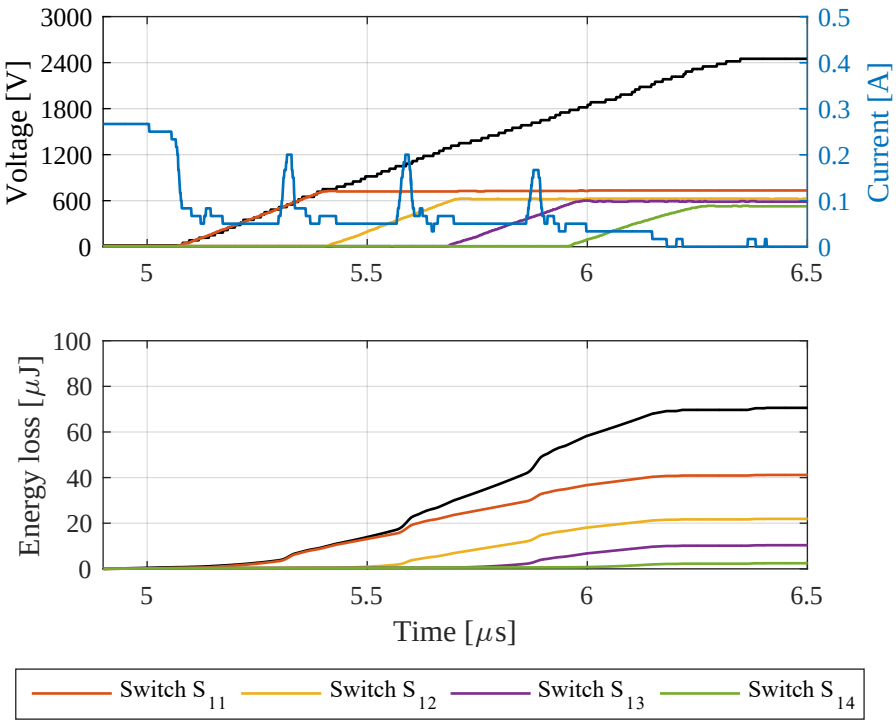


Figure 6.1. Voltage, drain current and energy loss as function of time during turn off.

The circuit shows that the voltage balancing capabilities of the circuit are good, and matches the performance of the simulation results in Chapter 4. There is no overshoot of the drain-source voltages. The full V_{ds}-voltage of the string of switches keep a constant $\mathrm{d}v/\mathrm{d}t$ as desired.

There is a small deviation in the off-state voltages of the devices, which is also reflected at the end of the turn off. Switch S_{11} holds the highest voltage of 730 V or 30 % of the full voltage (SVBP of 120 %), while S_{14} holds the lowest voltage of 533 V or 22 % of the full voltage (SVBP of 88 %). This is an improvement to the results presented by [Wu et al., 2014], which had highest and lowest SVBP of 139 % and 77 %.

Voltages are stored in the snubber capacitors, and therefore it is also at this voltage level that the MOSFETs return to at the end of their turn off. However, the voltage of the individual MOSFETs have a level of uncertainty, because of a potential influence of measuring probes. The full V_{ds} voltage is measured using a ground-referenced 4 kV LeCroy PPE high voltage probe, with an input to ground impedance of 50 MΩ. A Tektronix P5200A differential probe is used to measure the individual MOSFET voltages. This probe has an input impedance between the measurement points of 10 MΩ and an input to ground impedance of 5 MΩ. According to the datasheet, the SiC MOSFET have an off-resistance of 17 MΩ, but it is in parallel to the 420 kΩ snubber resistance, which is equivalent to a drain-source resistance to 410 kΩ. The complication is that the measured voltages, might be influenced by the measurement probes themselves, thus the "original state" without influence of probes is not known.

To reduce the influence that the measurement probes might have on the system, the following procedure is used to obtain the results. The 4 kV LeCroy PPE probe measures the full V_{ds} during all tests, so that the probe impedance on the entire string is the same during all tests. Individual MOSFET measurements are done using the differential probe, which is moved to the next MOSFET for the following test. Thus the measurements of Figure 6.1 is the result of a total of 4 subsequent double pulse tests, with individual MOSFET voltage measurements superimposed. It is verified that the full V_{ds} measurement is the same for all 4 tests. Despite the effort, the individual MOSFET measurements might still be influenced by the measurement probes.

A difference between the results of Figure 6.1 and the simulation in Figure 4.10, is that the drain current is not kept linearly increasing during the entire turn-off. This results in the energy loss being higher in the simulation when compared with the test results. This inconsistency in results is investigated in the following section.

6.1.1 Common mode current

It is investigated why the drain current is not the same as in the simulation. The main difference is that in the simulation ideal voltage supplies have been used to supply the gate drive. For this reason, in the simulation all gate currents are supplied differentially, leaving the drain and source currents equal, as shown to the left in Figure 6.2. Ideally this is also the wanted behaviour for the DC/DC supplies, as they are galvanic isolated. However, due to the parasitic capacitances another common mode loop is available, as shown to the right in Figure 6.2. During switching transients high $\mathrm{d}v/\mathrm{d}t$ cause currents to flow through the parasitic capacitance of the DC/DC supply. The result is that the drain and source current are not necessarily equal.

The current measurement is moved to the source side of the switch string. Subtracting the drain current from the source current highlights the amount of common mode current

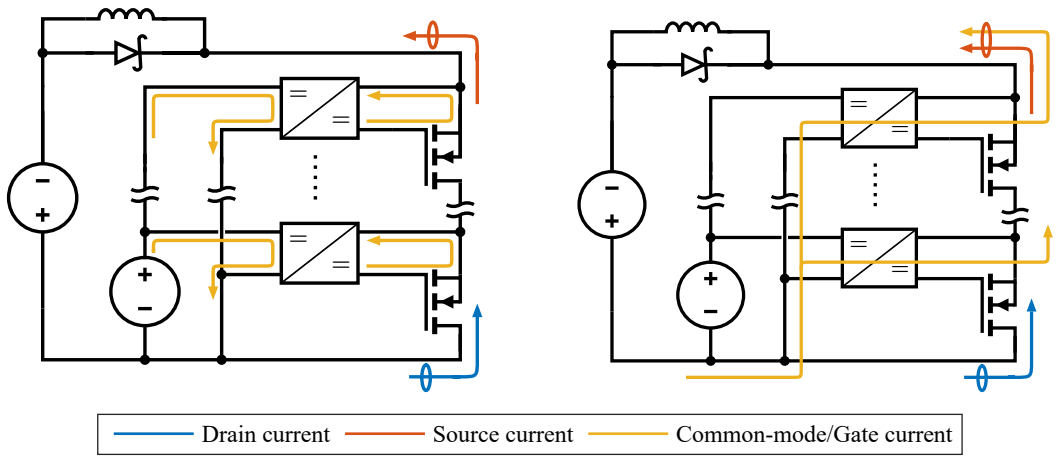


Figure 6.2. Differential current path (left) and the common mode current path (right).

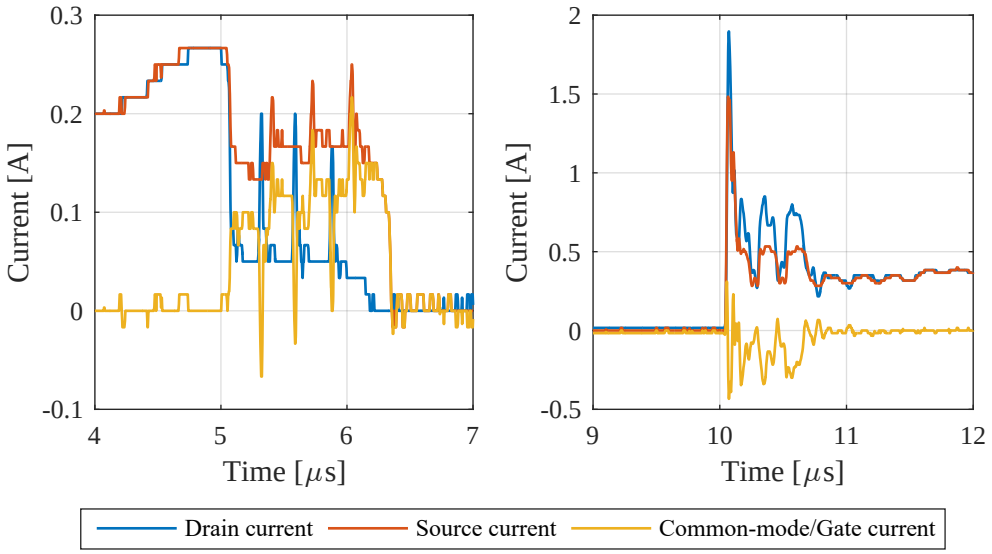


Figure 6.3. Drain, Source and Common mode currents during turn off (left) and turn on (right).

flowing through the circuit during switching transients, as shown in Figure 6.3.

Modelling the coupling is rather complex, as it depends on both magnetic and capacitive coupling in the DC/DC supplies. Those quantities are not described in the datasheet, and therefore it is difficult to include the coupling in the simulation results.

In the setup, common mode choke cores are inserted to attenuate the common mode currents. Effective solving of the root cause is to lower the parasitic capacitance of the supplies. Solutions include custom built supplies as mentioned in Section 5.2, but no further work is done on the issue in this project.

6.1.2 Turn-on transients

Turn on transients of drain-source voltage and currents are shown in Figure 6.4. Similar to the simulation results, the experimental results show good voltage balancing capabilities,

and also show similar timing of switching. Before the current starts rising, voltage differences between each device is observed, as was the case for turn-off. However, as soon as a larger current starts flowing through the RCD-snubber circuit, the voltage balancing becomes substantially higher during the remaining transition period. Initially in the turn-on a large current spike is seen due to the discharge of the parasitic drain-source capacitance of the first MOSFET. Similarly, for the remaining non-driven MOSFETs spikes are visible, but compared with the initial spike they are lower in magnitude but longer in duration.

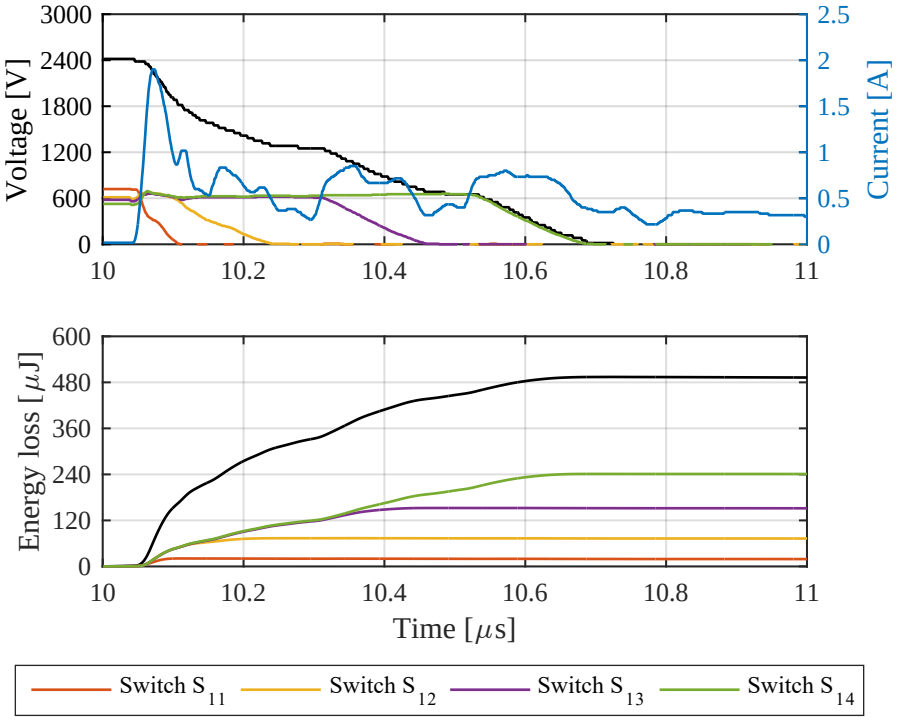


Figure 6.4. Voltage, drain current and energy loss as function of time during turn on

An issue is that the total switching time is around 700 ns. This is also an issue for the turn-off transient, which has a total switching time of 1300 ns. For this reason the gate-source voltages of Figure 6.5 are inspected, to gain greater insight of the circuit and possibly reveal issues.

Before turn-off it is noted that the gate-source voltage of the three non-driven switches are 1.4 V lower than the driven switch. This is because of the forward voltage drop of the two diodes in the path from DC/DC to gate of the MOSFETs. During turn-off the gate signals are delayed by roughly 300 ns per switch. The gate-source voltages during turn-on exhibits more ringing and overshoot when compared to the turn-off. The oscillations are largest at the beginning of the turn-on, which coincides with the current spike shown in Figure 6.4.

In the following section the problem of slow switching speeds are further investigated and possible solutions are tested experimentally.

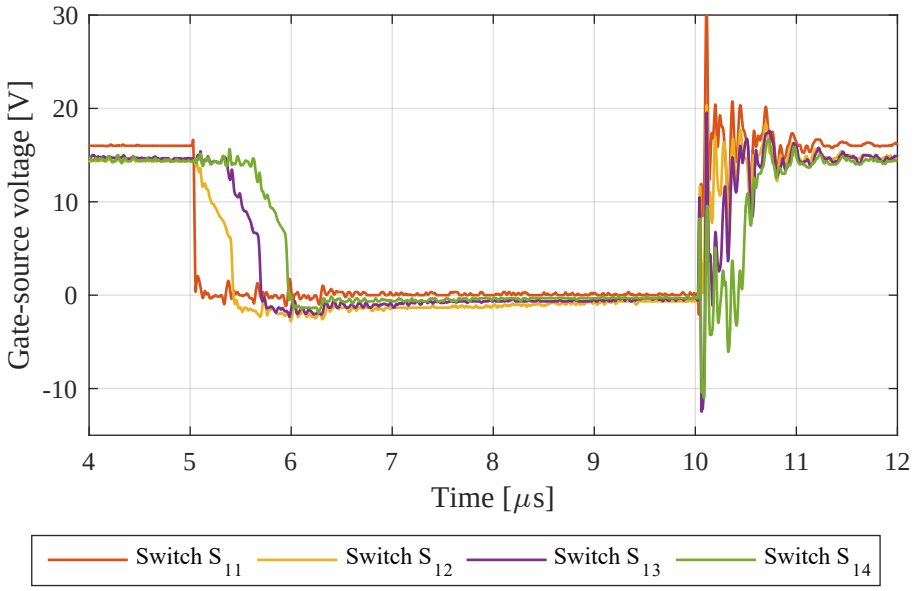


Figure 6.5. Gate-source voltages of the four switches in the string during the double pulse test.

6.2 Improving switching speed

To gain greater insight of how the circuit operates, a test is carried out where the current conducted through the circuit is changed from the initial 250 mA. The turn-off speed with various current levels is shown in Figure 6.6.

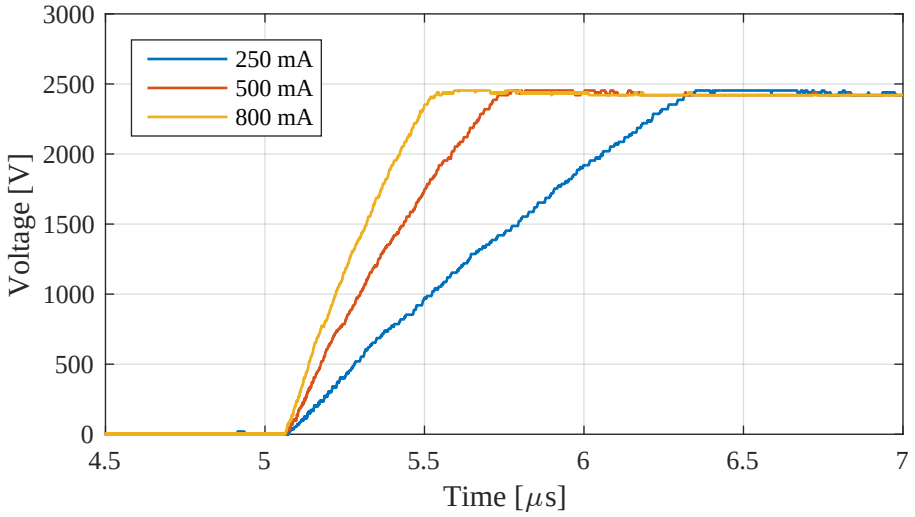


Figure 6.6. Turn-off voltage waveforms for different current levels.

Results show that a larger current conducted through the circuit gives faster switching speed at turn off. Current goes from being conducted through the MOSFETs to being conducted by the diodes in the snubber and by the zener diodes. The hypothesis is that the diodes enter their forward biased mode faster, because a larger current discharges the junction capacitances faster. To increase the turn-off speed the diodes should be forward biased faster.

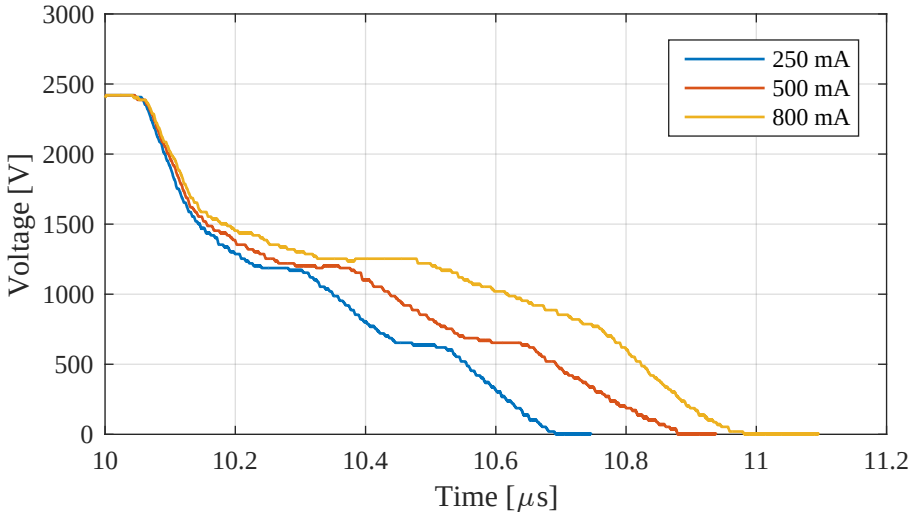


Figure 6.7. Turn-on voltage waveforms for different current levels.

Likewise, turn-on speed at different current levels are shown in Figure 6.7. Larger current levels slow down the switching speed of the circuit. The initial shape of the waveform shows that the first MOSFET turns on at the same speed, after which the waveforms start to break apart. After the first switch starts conducting, the current starts flowing through the RCD-snubber and the zener diode. But for the following switch to turn on, the zener diode must become reverse biased to provide 15 V for the gate. The diodes have a fixed $\mathrm{d}i_{\mathrm{rr}}/\mathrm{d}t$ (50 A/μs for the STTH112 snubber diodes), and thus a larger conducted current increases the delay. To make the turn-on faster, it must be ensured that the zener diode quickly becomes reverse biased at 15 V.

The circuit has been investigated at various current levels, which change the behavior of the circuit. However, the switch is to be used in an application which results in a given current level. It cannot be changed independently to suit the circuit better. Thus, changes to the hardware must be implemented to speed up the transients. The following subsections investigate modifications to the circuit with the purpose of reducing turn-on and turn-off time.

6.2.1 Speed-Up Capacitors

A solution to speed up the turn-on is proposed in [Wu et al., 2014]. The solution uses additional capacitance, $\mathrm{C_{spd}}$, on the gate drive diode to ensure the zener diode enters reverse biased mode faster, as shown in Figure 6.8.

During the off state current is conducted through the RCD-snubbers and forward biasing the zener diode. By Kirchoff's voltage law the voltage of $\mathrm{D_{G2}}$ in the off-state is $v_{\mathrm{DG2}} = V_{\mathrm{G2}} + V_{\mathrm{fZ2}} - v_{\mathrm{M1}}$, where V_{fZ2} is the forward voltage of the zener diode. V_{G2} is fixed at 15 V, thus the voltage of the diode is mainly dependent on the voltage of the MOSFET, v_{M1}. When $\mathrm{M_1}$ turns on, current is conducted through it and its voltage drops, and inherently v_{DG2} drops. For the voltage to drop, its junction capacitance must

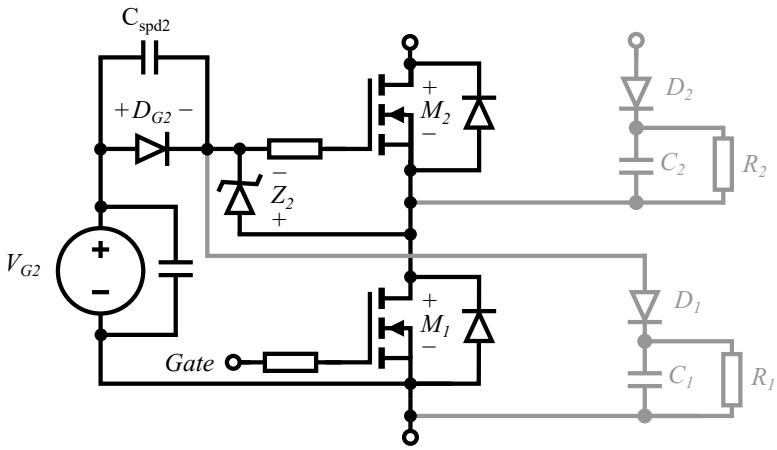


Figure 6.8. Diagram showing the placement of the speed-up cap, C_{spd}, in the gate driving circuit.

be discharged through the zener diode[1]. Increasing the junction capacitance to a large enough value, ensures that Z_2 becomes reverse biased at the gate-source threshold voltage of M_2, before M_1 is completely turned on itself. The purpose of the supply V_{G2} then solely becomes to maintain the gate-source voltage at 15 V after the switching transition.

The full V_{ds} voltage of the circuit during turn-on is shown in Figure 6.9. The tested capacitor values are 0 pF, 33 pF, 83 pF and 333 pF, created by a combination of series connecting three 1 nF and 100 pF Murata GRM 1206 SMD capacitors each rated at 1 kV.

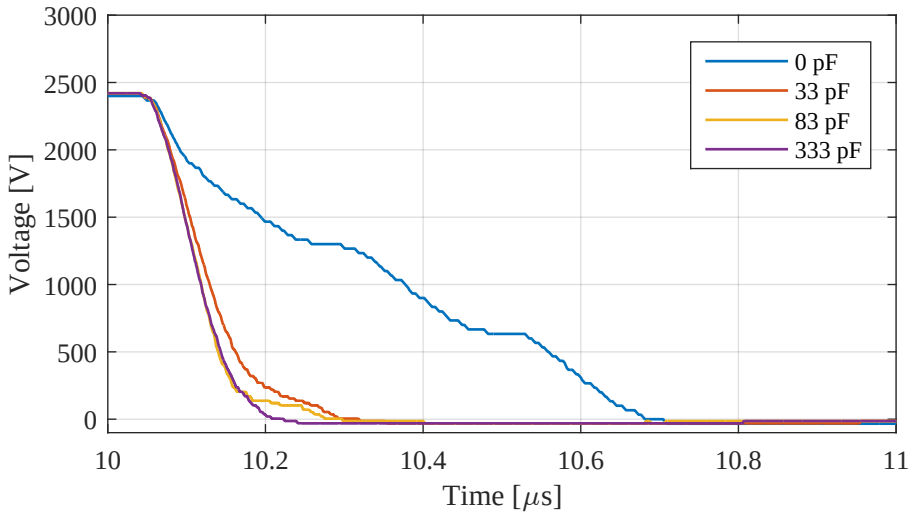


Figure 6.9. Turn-on voltage waveforms for different values of speed up capacitor.

Results show that the addition of 33 pF changes the total turn-on time from 700 ns to 300 ns. Increasing the speed up capacitance further speeds up the circuit to a maximum of 333 pF, which results in a total turn on time of 250 ns.

[1]The current cannot be conducted through the RCD snubber. The capacitor C_1 has stored the off-state voltage, so as soon as the voltage of M_1 drops, Kirchoff's voltage law dictates that D_1 must be reverse biased when evaluating the loop containing RCD-snubber, V_{G2} and D_{G2}.

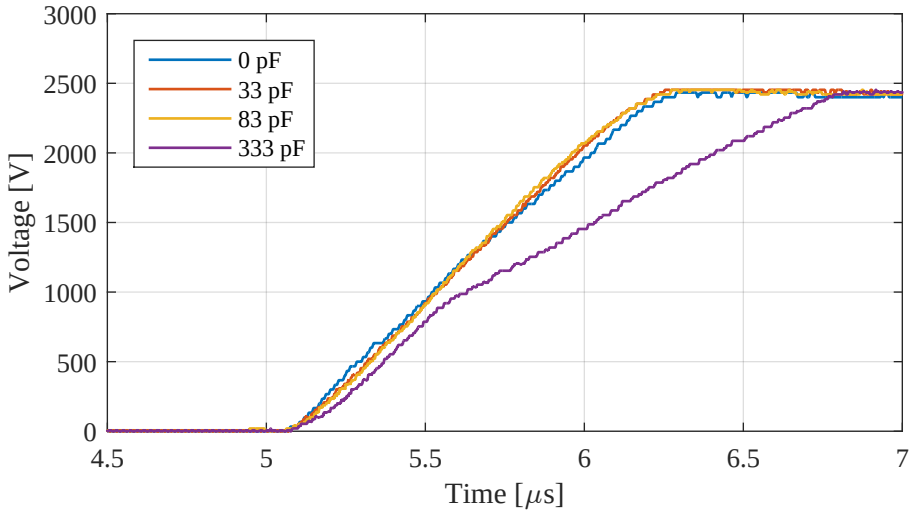


Figure 6.10. Turn-off voltage waveforms for different values of speed up capacitor.

The turn-off waveforms for the different speed up capacitances are shown in Figure 6.10. Results reveal that increasing the capacitance also increases the turn off time. An effect which is undesireable. The reason is that during turn-off the zener is forward biased, meaning that increasing the capacitance across the diode is equivalent to increasing the drain-source capacitance of the MOSFET (As the path enclosed by M_1, V_{G2}, C_{spd2} and Z_2 in Figure 6.8). This also means that the switching speed of switch 4 is not changed significantly. At speed up capacitances of 33 pF and 83 pF its influence on the turn off speed is indistinguishable from the case of no speed up capacitance. The hypothesis is confirmed by looking at the waveforms of Figure 6.11, showing individual turn off voltages with $C_{spd} = 33$ pF. This shows how the turn off time of the last switch is left unaffected. Also visible from the figure is how the common mode current changes the drain-current waveform as the dv/dt changes, as described in Section 6.1.1.

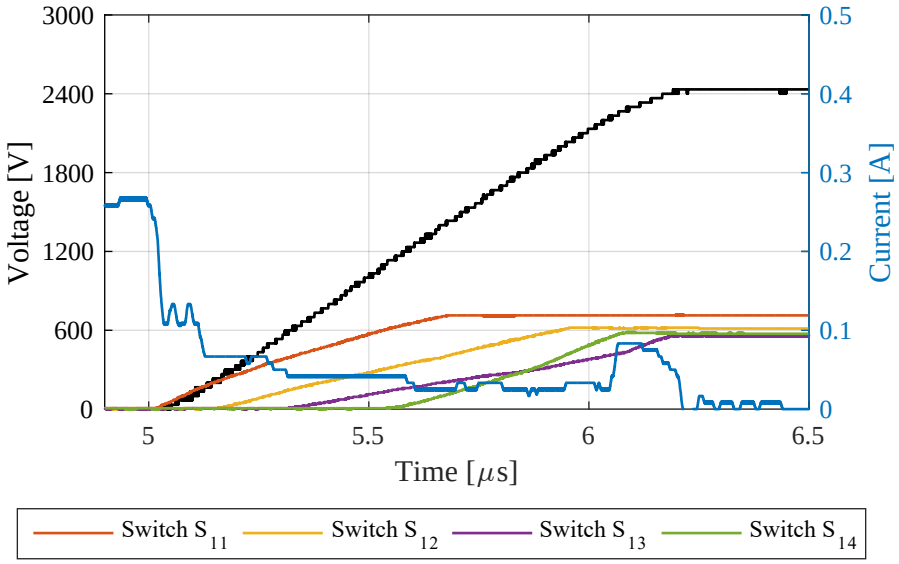


Figure 6.11. Voltages and drain current during turn off with $C_{spd} = 33$ pF.

When compared to a speed-up capacitance of 33 pF, increasing it to 83 pF does not further reduce turn-on time. 333 pF significantly increases the turn-off speed of 450 ns, because $\mathrm{d}v/\mathrm{d}t$ of switches 1, 2 and 3 is further slowed. In conclusion, a speed-up capacitance of 33 pF is chosen for further circuit operation. This reduces the turn-on time from 700 ns to 300 ns, without having a significant impact on the turn-off speed. The performance of the voltage balancing between switches is left unaltered by the circuit modification, and still has no overshoot of voltage.

The effect on the gate-signals due to the speed-up capacitance is shown in 6.12. When compared with Figure 6.5, the turn-on signal is more strongly defined and exhibits faster switching and less ringing. It also shows that the delay between switches during turn-off is now only 200 ns (instead of around 300 ns), but the added drain-source capacitance results in the total turn-off time being unaltered.

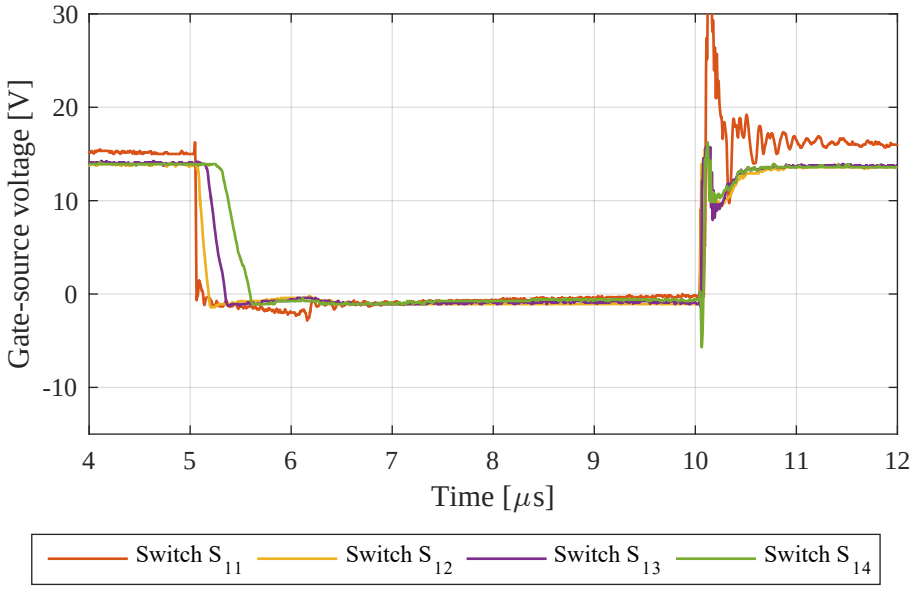


Figure 6.12. Gate-source voltages of the four switches in the string during the double pulse test with $C_{\mathrm{spd}} = 33$ pF.

6.2.2 Faster forward-bias of zener

A hypothesis from analysing the results of Section 6.2, is that faster forward biasing of the zener diode leads to faster turn-off of the string of MOSFETs. A modification to the zener circuit is proposed with the goal of faster forward-bias. The modification, shown in Figure 6.13, involves connecting a diode in parallel with the zener diode. The diode should have a lower forward voltage to ensure that it conducts first, and in general faster dynamics such as lower junction capacitance and forward recovery time is preferred.

Analysing the diagram the diode should not interfere with the operation of the zener in the reverse biased region, but ensure faster forward biasing. However, two consequences are noted which could result in a slower response of the circuit. An additional diode in parallel increases the junction capacitance, which for the same current, results in a slower change of voltage. This could potentially slow down both turn on and turn off. A lower forward voltage could potentially slow down the turn off of the MOSFET itself. To turn

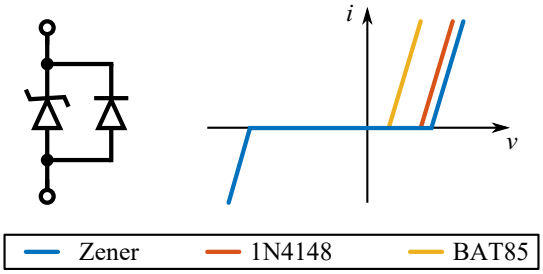


Figure 6.13. A diode in parallel with the zener modifies its forward voltage.

off the MOSFET the zener/diode-connection is forward biased, meaning that the v_{gs} of the MOSFET is equal to the forward voltage. Larger negative voltages on the gate have been documented to speed up the turn off of a MOSFET, and thus the reduced forward voltage could result in slower turn off.

The addition of a diode in parallel with the zener is tested in the laboratory. Two diodes are tested in parallel with the zener. An 1N4148 fast switching signal diode with a measured forward voltage of $V_F = 0.6$ V and a BAT85 Schottky diode with $V_F = 0.25$ V. The results of voltage turn-off with the different diodes in parallel are shown in Figure 6.14. Also, results of turn-on, shown in Figure 6.15, does not indicate that the addition of a diode has an influence on the turn on of the switch.

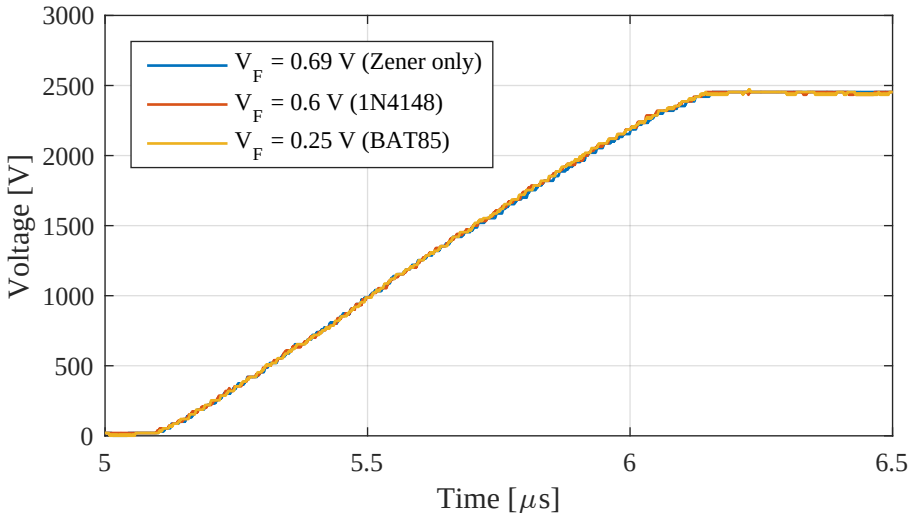


Figure 6.14. Turn-off voltage waveforms with different diodes in parallel with the zener.

Results show that the switching speed is not influenced by the addition of a diode. During the tests it is verified that the addition of the BAT85 Schottky diode has reduced the forward voltage of the zener-connection, meaning that the gate source voltage during turn-off is increased from around -0.7 V to -0.3 V, and maintained the reverse biased voltage at 15 V. Despite the slight change in voltage level, the shape and speed of the gate-source voltages does not change. No other modifications have been tried to speed up the turn-off.

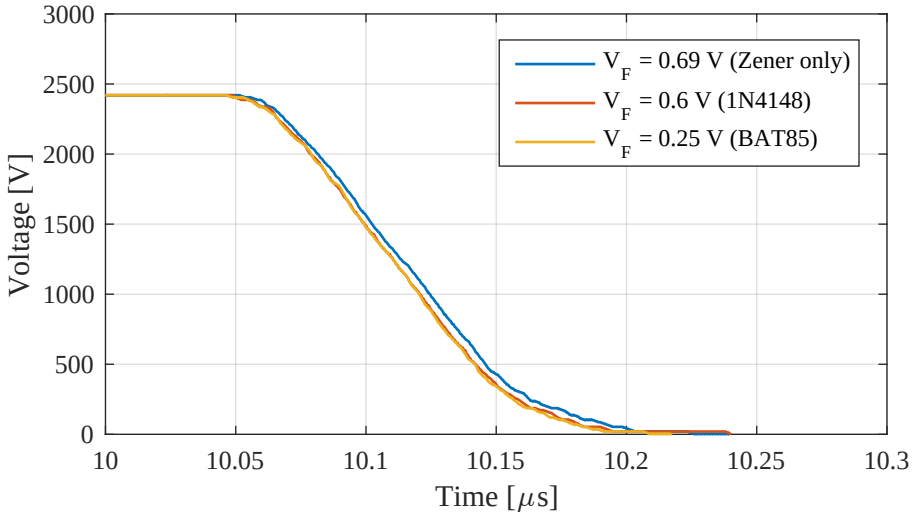


Figure 6.15. Turn-on voltage waveforms with different diodes in parallel with the zener.

Chapter 7

Voltage Balancing during Converter Operation

The following chapter presents the performance of the voltage balancing capability of the MOSFET string when operated as a switch in the synchronous boost converter, as presented in Chapter 3. In literature the series connection of SiC MOSFETs is benchmarked with the DPT. The performance of the voltage balancing capabilities during continuous switching is not available for other serialization methods, and thus the results obtained in this chapter can not be directly compared with other solutions. However, deviations from the DPT results obtained in Chapter 6 will be highlighted and discussed.

The control strategy proposed mainly utilizes operating mode DCM_+. The test setup presented in Chapter 5 is slightly modified. The Schottky diode is rearranged for a boost converter configuration, as shown in Figure 7.1.

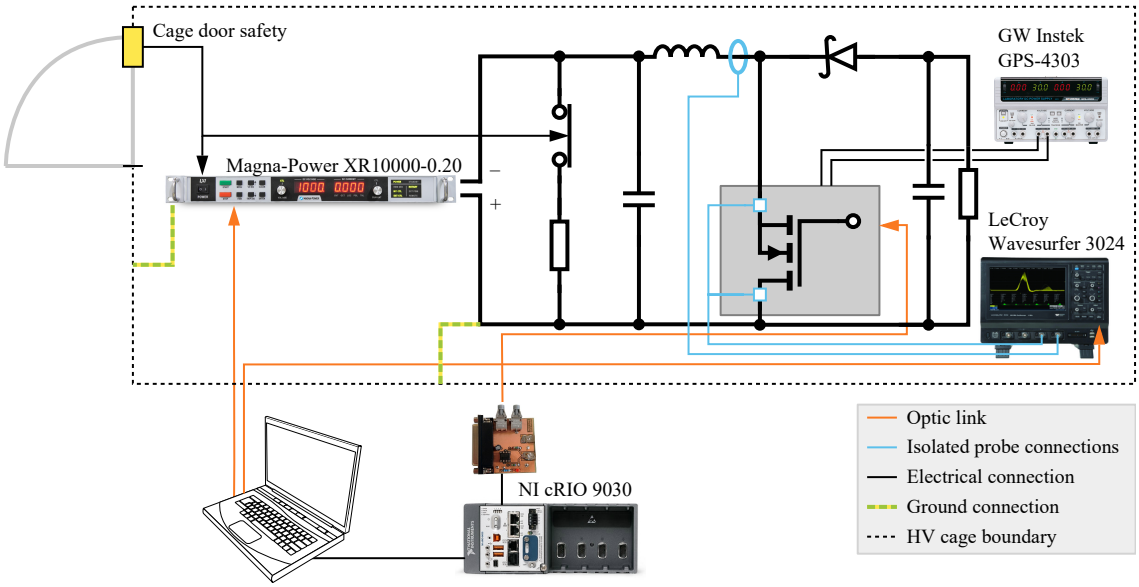


Figure 7.1. Diagram of the circuit used to test the series connection under DCM converter operation.

An RC-load is added as the output. The output capacitance is made of six 3.3 nF (total of 19.8 nF) ceramic 615R100GAD33 capacitors by Vishay[1] in parallel, each rated for 10 kV. The output resistors are seven 47 kΩ Arcol HS50[2] with a voltage rating of 1.25 kV

[1]Datasheet available at http://www.mouser.com/ds/2/427/615r-205494.pdf
[2]Datasheet available at http://www.farnell.com/datasheets/1927175.pdf

and power dissipation level of 50 W each. The number of resistors in either series and parallel depend on the desired voltage and power dissipation level.

7.1 DCM operation test results

The voltage across the switch for the test is lowered, because voltage balancing capabilities are seen to be lowered when switched continuously. By an input voltage v_i = 600 V, duty cycle of D = 0.45 and switching frequency f_s = 50 kHz the output voltage becomes v_o = 1200 V. The drain source voltage of each switch and the inductor current is measured as shown in Figure 7.2. For this test the same snubber resistance of 420 kΩ, snubber capacitance of 8.8 nF and speed-up capacitance of 33 pF is used, as was the case in Chapter 6.

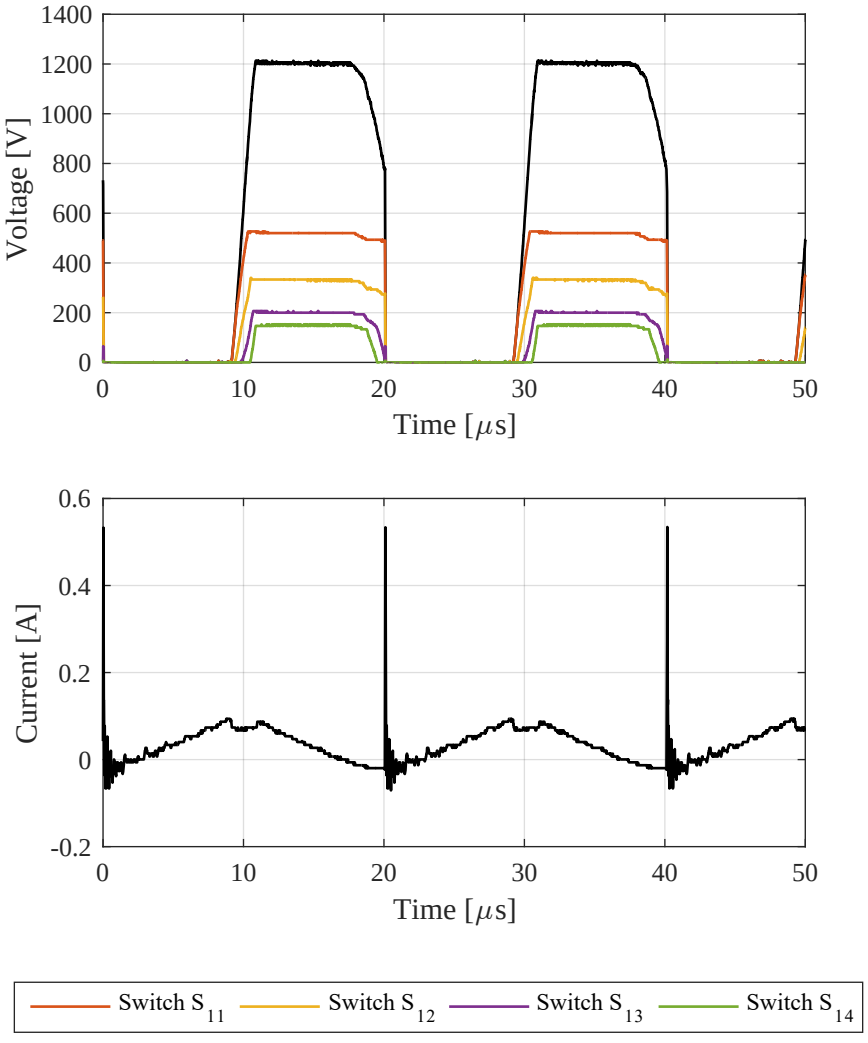


Figure 7.2. Drain-source voltages and inductor current with snubber resistance of 420 kΩ.

The voltage balancing is worsened when compared with the DPT of Chapter 6. Switch S_{11} holds most of the voltage with 520 V equal to 43 % of the full voltage ($SVBP$ of 173 %), while switch S_{14} takes the least voltage with 153 V ($SVBP$ of 51 %). From the figure

it is seen that as the current crosses zero, the voltage of the switches starts to drop. In Chapter 4 it was analyzed that the circuit exhibits a First On First Off (FOFO) sequence, i.e. switch 1 turns on first and also turns off first. However, just before the switch is turned on the voltages of each switch start to drop simultaneously. This phenomenon is investigated further in the following section.

7.1.1 Influence of parasitics in DCM

The switching frequency is reduced to $f_s = 10$ kHz, to get a better view of what happens after the current reaches zero. The drain-source voltages and inductor current are shown in Figure 7.3.

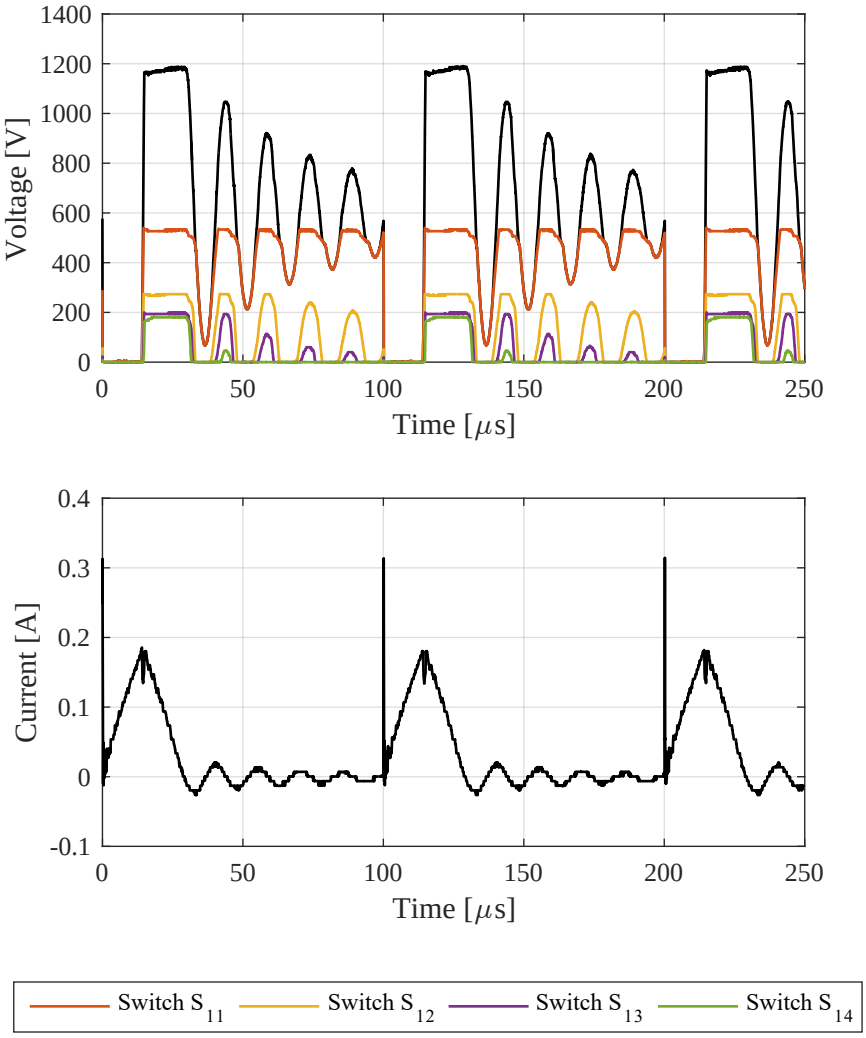


Figure 7.3. Drain-source voltages and inductor current with $R_s = 420$ kΩ and $f_s = 10$ kHz.

It is seen that the voltage drop of the switches is due to voltage oscillations as the current crosses zero. The phenomenon is described by [Gusseme et al., 2007], and is caused by the parasitic capacitive elements of the diode and switch. Just as the current reaches zero, at the transition between state B and C in Figure 7.4. The input voltage v_i is kept constant because of the large input capacitor, but the voltage on the string of switches is $v_\mathrm{s} = v_\mathrm{o}$.

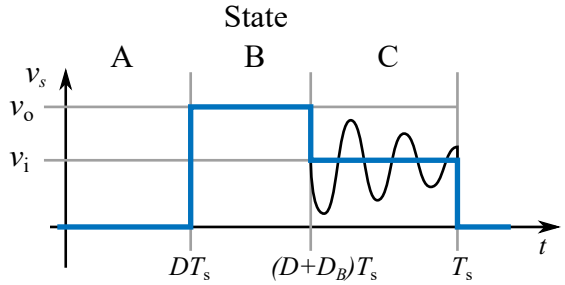


Figure 7.4. Switch voltage during the three states in DCM operation mode.

Thus the voltages on those two capacitors are not in equilibrium and oscillatory transients occur. A case is presented in [Gusseme et al., 2007], when the input capacitance is much larger than the parasitic capacitance of the switch and diode, as is the case for this project. Then the input voltage is assumed constant, and the switch voltage as a function of time is given by:

$$v_{\mathrm{s}}(t) = v_{\mathrm{i}} + (v_{\mathrm{o}} - v_{\mathrm{i}}) \cdot \cos(\omega_{\mathrm{n}}(t - (D + D_{\mathrm{B}})T_{\mathrm{s}})) \tag{7.1}$$

where $D_{\mathrm{B}}T_{\mathrm{s}}$ is the duration of state B and ω_n is the natural angular velocity defined by

$$\omega_{\mathrm{n}} = \frac{1}{\sqrt{LC_{\mathrm{n}}}} \tag{7.2}$$

where C_{n} is the sum of the switch and diode capacitance. The inductance is $L = 49$ mH. The frequency of oscillation from Figure 7.3 is 67 kHz. Calculating the expected capacitance of switch and diode connections, C_{n} is

$$C = \frac{1}{L(2\pi f)^2} = \frac{1}{49\,\mathrm{mH} \cdot (2 \cdot \pi \cdot 67\,\mathrm{kHz})^2} = 115\,\mathrm{pF} \tag{7.3}$$

However, equations (7.1)-(7.3) uses an approximation of constant capacitance values. The datasheet of the Schottky diode and SiC MOSFET reveal that the capacitance changes with voltage and is highly non-linear.

The implication of this is that the voltage balancing is not improved by lowering the frequency. Switch S_{11} holds 527 V, while S_{14} holds 180 V. During turn-on and turn-off transients current is conducted through the snubber capacitors, resulting in unequal charging. During the period of state B, the output voltage v_{o} is across the switch, conducting current through the snubber capacitors and their parallel resistors, to ensure unequal voltages are balanced. There are mainly two means to obtain voltage balance before the next switching transient. Lowering the snubber resistance increases the current conducted which ensures that imbalances are evened out quicker, but this also results in higher power loss in the snubber circuit. Alternatively, increasing the duration of state B ensures a longer time for snubber capacitors to be either charged or discharged to obtain voltage balance. However, decreasing the switching frequency in DCM mainly increases the duration of state C, in which no effective balancing occurs.

7.2 Improving voltage balancing

The hypothesis for improved voltage balancing includes higher power loss in the snubber resistance and increased duration of state B. In Section 7.2.1 the effect of higher power loss in the snubber resistance is investigated. As was shown in Figure 7.3, when operated in DCM a reduction of frequency does not significantly increase the duration of state B. However, for CCM_+ only states A and B exist, ensuring that the ineffective state C is eliminated. The influence on the voltage balancing when operating the converter in CCM_+ is investigated in Section 7.2.2.

7.2.1 Lowering snubber resistance

For the following tests the snubber resistance is reduced from 420 kΩ to 150 kΩ. For an expected voltage balance of 300 V per device, this increases the power loss in the snubber resistance from 0.2 W to 0.6 W per switch. Besides this change, the test is performed with the same conditions as done in Section 7.1.

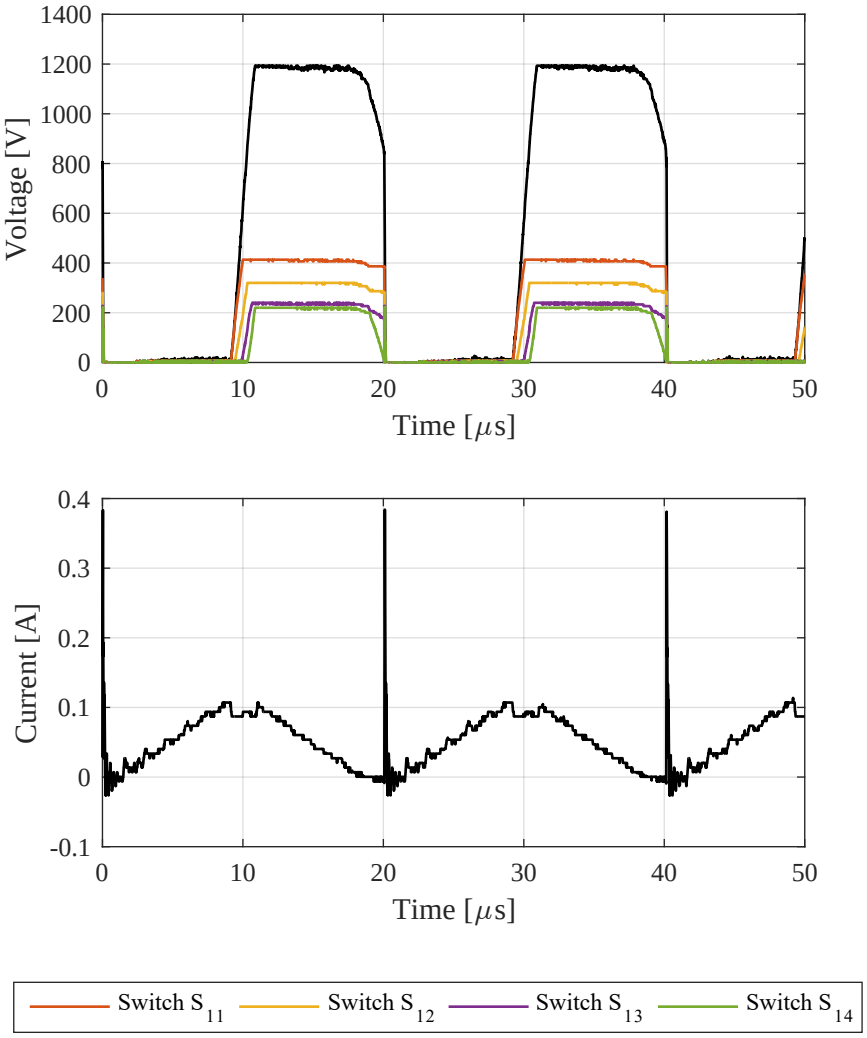


Figure 7.5. Drain-source voltages and inductor current with $R_s = 150$ kΩ.

The results show that the switch S_{11} now holds the maximum voltage of 407 V ($SVBP$ = 135 %), while the minimum voltage is kept by S_{14} at 220 V ($SVBP$ = 73 %). When compared to the results presented in Figure 7.2 where snubber resistance R = 420 kΩ, the voltage balancing has been improved. The switch which holds the maximum voltage has been reduced from 520 V to 407 V. This result supports the hypothesis that higher power loss ensures better balancing.

7.2.2 Operating mode

It was found that for CCM a reduced switching frequency extends the duration for which the circuit is in state B, where effective voltage balancing occurs. In Chapter 3 the two modes DCM_+ and CCM_0 were considered for further use in the project, but DCM_+ was used as it results in reduced losses. In the following section it is investigated how the operating mode DCM_+ or CCM influences the voltage balancing of the converter. However, one issue is that only a single series connected SiC MOSFET string is developed, meaning that the CCM_0 mode is not possible. As an alternative it is investigated how well the CCM_+ mode behaves. Similarly this mode only consists of state A and B, and transition between states includes that the switch is hard switched. This ensures from a voltage balancing point of view that the FOFO-sequence is maintained.

To force the converter into CCM_+ mode the average inductor current is increased by lowering the input voltage to v_i = 400 V. For v_o = 1200 V a duty cycle D = 0.69 is used. Besides this change all other parameters are kept the same as presented for Section 7.2.1. The drain-source voltage waveforms and currents are shown in Figure 7.6.

The switch which takes the maximum voltage is switch S_{11} at 400 V ($SVBP$ = 133 %), while the minimum is S_{13} at 227 V ($SVBP$ = 76 %). When compared to the results in the previous section, a change of mode from DCM_+ to CCM_+ has improved the voltage balancing slightly. However, the time at which the two modes stay in state B is not equal, and therefore results cannot be compared directly.

From this investigation, the conclusion is that CCM_+ does not result in a significantly better voltage balancing when compared to DCM_+. However, the perspective is that by using CCM_+, the switching frequency can be reduced to further increase the voltage balancing of the switch.

No further tests are presented for the CCM_+ mode. The performance of the voltage balancing at lower frequencies in CCM_+ is of great interest, but it was found difficult to keep the converter in this operating mode when reducing the frequency.

7.3 Final results

Now that the voltage balancing has been improved, a final test is performed for DCM where the voltage magnitudes are increased. The input voltage is increased to v_i = 1200 V, and by setting the duty cycle D = 0.21 the output voltage becomes v_o = 2450 V. The snubber resistance is changed to R = 330 kΩ, meaning that if each switch is perfectly balanced a power loss of 1.1 W in each snubber resistance is expected. To account for the higher output voltage the output resistance is increased to 188 kΩ, resulting in the

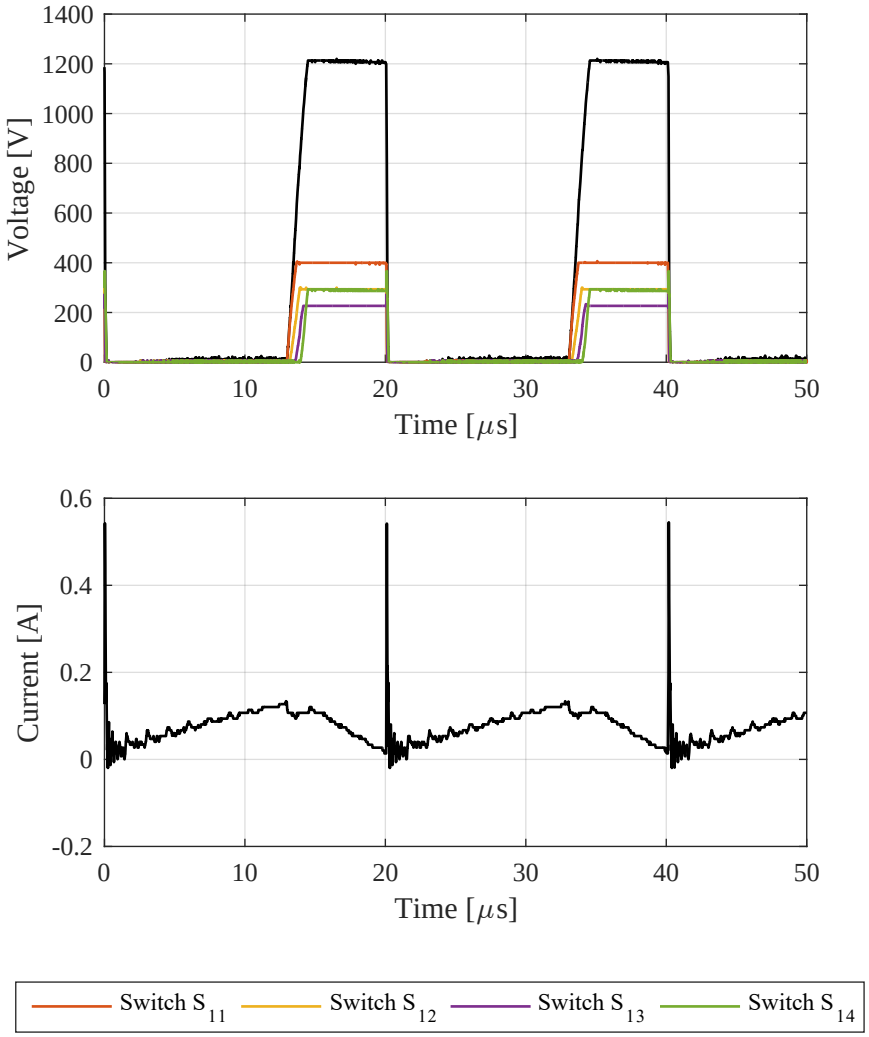


Figure 7.6. Drain-source voltages and inductor current with $R_s = 150$ kΩ and operation in CCM.

output power to be 31 W. The results of drain-source voltage per switch and the inductor current are shown in Figure 7.7.

The oscillations during state C are still clearly visible. Also evident from the figure is that the oscillations cause the current to start from a non-zero value. Due to the oscillations the turn-on loss can no longer be considered negligible. Evaluating the voltage balancing it is seen that switch S_{13} holds the minimum voltage of 450 V ($SVBP = 75\%$). Switch S_{11} holds a maximum of 866 V ($SVBP = 144\%$). The power loss in the snubber resistance of this switch is 2.2 W. The snubber resistance consists of six 2010 SMD packages resulting in a total power rating of 3 W. Compared with the output power of 31 W, the power loss of 2.2 W for just the snubber resistance of a single switch is substantial. This highlights that simply reducing the resistance is not a feasible solution if efficiency is important.

Compared with the DPT results of Chapter 6, also done at 2400 V, the voltage balancing during 50 kHz DCM_+ operation is degraded. The switch, which is holding the maximum

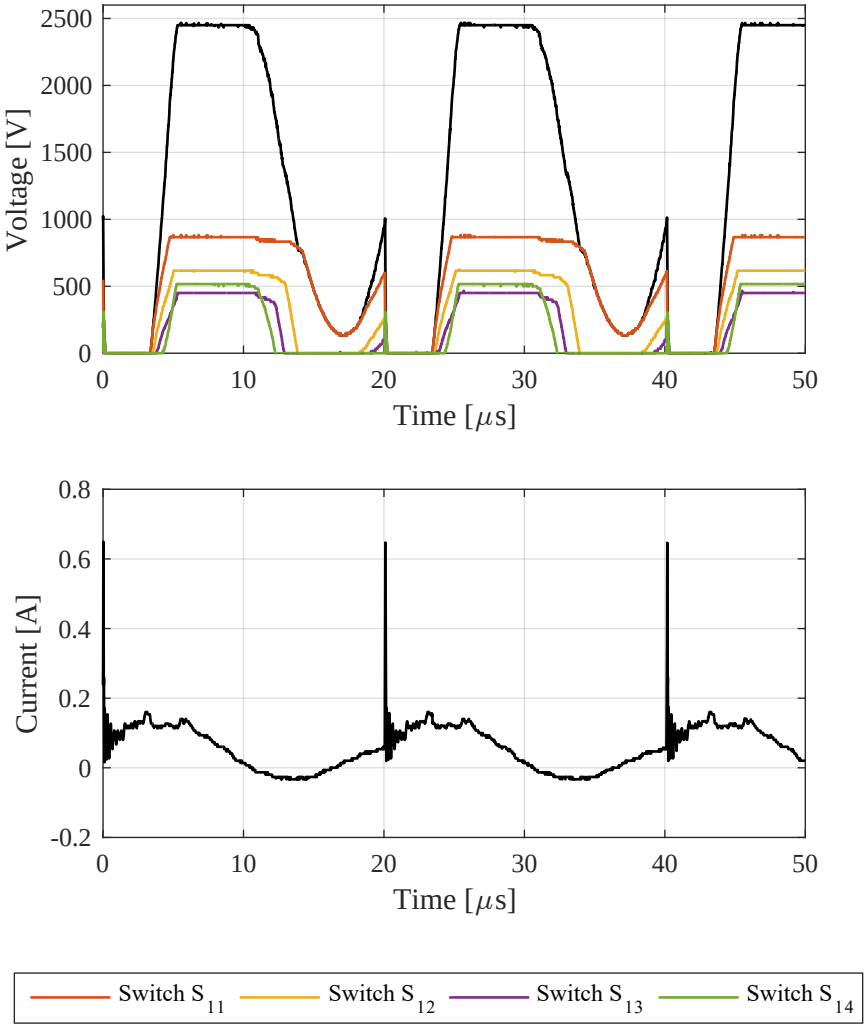


Figure 7.7. Drain-source voltages and inductor current with $R_s = 330$ kΩ.

voltage, held 730 V (119% $SVBP$) in the double pulse test compared to the 866 V (141% $SVBP$) in the DCM$_+$ test. However, the obtained voltage balancing is also compared with the results of [Wu et al., 2014]. This article showed voltage balancing of three switches in a DPT using the same cascaded driving structure. The switch taking up the most voltage had 1070 V of an expected 770 V (139 % $SVBP$). Thus, in this case similar voltage balancing has been obtained with a total of four switches, and switched at a frequency of 50 kHz.

7.3.1 Future work

In Section 7.2.1 it was shown that voltage balancing is improved by allowing higher power loss in the snubber circuit. This solution have proven effective to some degree. However, in terms of efficiency this option is not feasible to solve all issues. Reduction of frequency increases the time at which static balancing ensures that switches share the voltage evenly. However, as was shown in Section 7.1.1, reduction of frequency does not substantially improve voltage balancing in DCM$_+$. Because the voltage across the switch decreases

from v_o to v_i as the circuit changes state from B to C, no effective balancing occurs during state C.

To further improve the voltage balancing during converter operation, a suggestion is to change the operating mode to CCM_0, at the expense of increased switching losses. The operating mode CCM_0 consists of only states A and B, which in turn means that a reduction of frequency results in an increased duration of state B. CCM_0 requires bidirectional current flow, and therefore another string of series connected SiC MOSFETs must be developed to replace the Schottky diode used in Figure 7.1. The other switch also requires a board with gate driving signals. The gate driving board for the switch S_{21} is denoted as an "output module". The concept diagram of two strings of SiC MOSFETs, is shown in Figure 7.8. This concept is also developed having a modular layout structure, following the design philosophy presented in Section 5.1. The "non-driven" modules are the same as previously shown, the only new module is the output module. KiCAD schematics and PCB layouts for the output module is included in Appendix D and E, respectively.

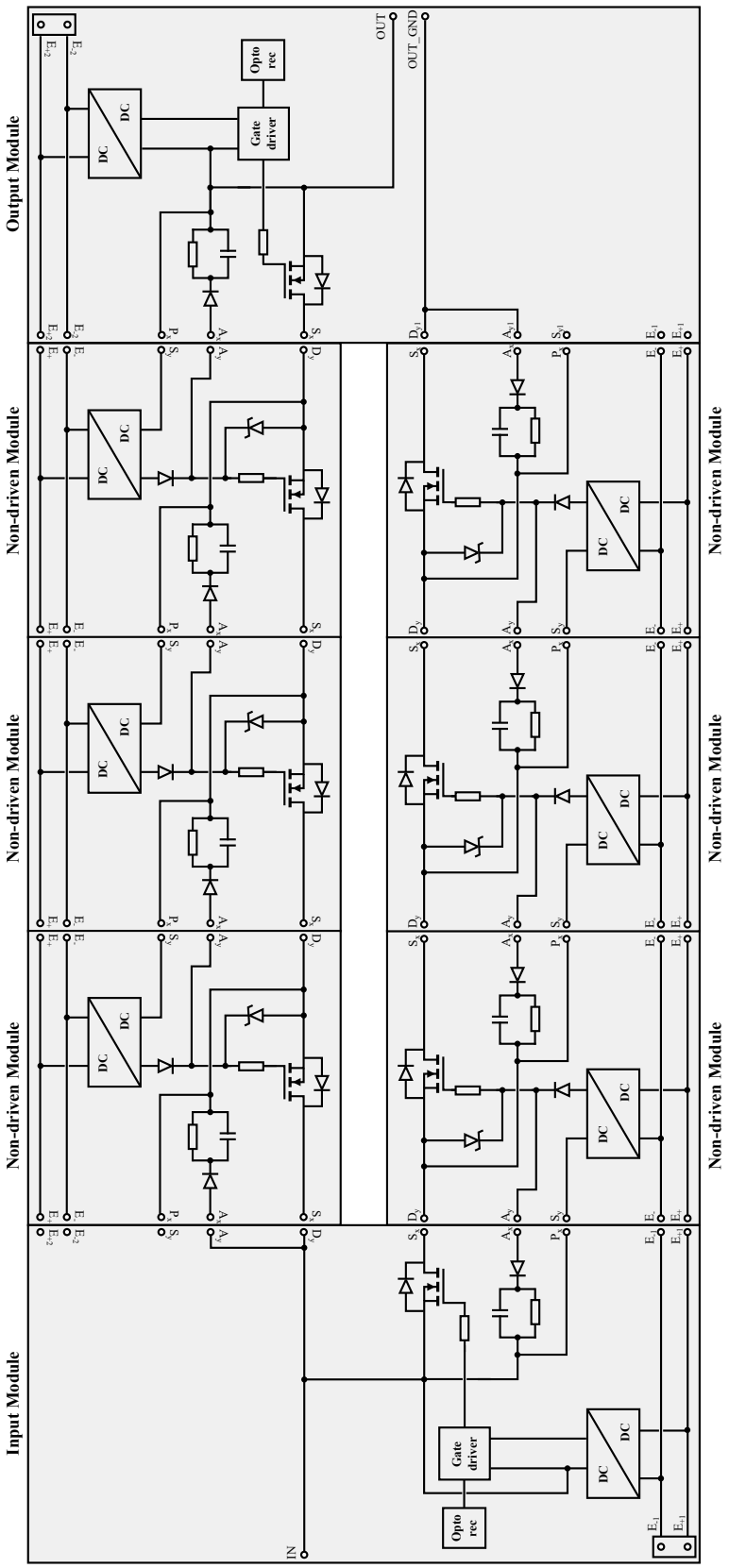


Figure 7.8. Concept diagram of a modular layout featuring two strings of SiC MOSFETs.

Chapter 8

Discussion

This project has mainly addressed the problem of series connecting four SiC MOSFETs for the purpose of supplying a small scale ESP.

The serialization method that was tested in this project utilizes cascaded switching of the serialized devices. The constant voltage slope during transients mitigates the oscillation issues of other serialization methods. However the cascaded switching results in increased switching time for each additional device in the string.

Analysis and tests of the serialization method revealed that the transients can be sped up. Higher current in the circuit substantially speeds up the turn-off transients and the use of speed up capacitors in the circuit allows for faster turn-on transients. The speed up capacitor adds a degree of freedom in the circuit design, i.e. its value can be changed to compensate for changing current levels. A full scale ESP requires more energy for energization, resulting in a larger current in the circuit which would speed up the switching transients.

In a full scale ESP the blocking voltage requirements is in the order of 80 kV, hence a string would require more than fifty of the 1.7 kV devices, which were used in this project. The switching time of such a string would be very long and would limit the possible switching frequency, which could deem this method unfeasible. However, the alternative of turning on/off all fifty SiC MOSFETs simultaneously could prove troublesome, with device switching speeds of 20-100 ns. The issues of high $\mathrm{d}v/\mathrm{d}t$, voltage ringing, number of required synchronous gate signals and voltage balancing increase manyfold.

A hybrid solution with the cascaded switching method combined with one of the other voltage balancing methods, might be a solution to this problem. Such a solution would consist of serialized modules that are balanced using for instance the gate signal balancing technique. Each of the modules would consist of a string of cascaded devices as treated in this project. The modules are then switched simultaneously. The voltage across each module is balanced by controlling the delay of gate signal using the gate signal balancing technique.

If the SiC technology continues to increase the device voltage ratings into the 10-20 kV range, it might be feasible to use five to twelve devices serialized exclusively using the cascaded method to obtain a total string voltage in the range of 80 kV.

Chapter 9

Conclusion

Silicon carbide (SiC) based switch mode power supplies offer a number of improvements to conventional electrostatic precipitator (ESP) energization including higher controllablity and faster voltage recovery after spark occurrence. The purpose of this project was to investigate the challenges of SiC converter design in the context of the ESP application. The main challenge is the serialization of devices, which is the main topic of this thesis. A small scale case of the ESP application was treated: 6 kV, 17 mA output rating.

A suitable converter topology, the synchronous boost, was analyzed in terms of circuit states and operating modes. The losses of the CCM_0 mode, which is the inherent mode of the nominal operating point, were estimated for a number of commercially available SiC devices. The losses are reduced in the unidirectional DCM_+ mode. In this mode ROHM devices are superior to the CREE devices, with losses of 2.2% and 5.1% for 1.2 kV and 1.7 kV device, respectively. A conceptual PLECS simulation proves how bidirectional power flow is maintained through an adaptive control structure.

A literature survey of different methods for serializing semiconductor devices was conducted. The survey showed that limited research has been done in the serialization of SiC MOSFETs. A number of obstacles need to be solved when serializing, e.g. voltage overshoot during switching transients and static as well as dynamic voltage balancing. One method that mitigates the voltage overshoot issues is described in literature. The method uses a cascaded turn-on and turn-off concept which maintains the same voltage slope for an extended string of devices. A compromise of the method is increased switching time.

A string of four serialized 1.7 kV SiC MOSFETs was constructed. The string is based on the cascaded switching concept, where only one device of the string is actively driven with a gate signal. The string was constructed in a modular structure, consisting of several PCBs each containing one MOSFET and driving circuit. This means that the string is easily modified to contain more or less serialized devices. The driving voltage of the devices are supplied by isolated DC/DC converters. A CompactRIO 9030 from National Instruments supplies the gate signal for the driven switch. The programming was developed in LabVIEW, which is used to control the test setup.

The performance of the string was tested in a double pulse test (DPT), which revealed the switching transient current and voltage waveforms as well as the static voltage balancing performance. The tests were conducted at a full string voltage of 2.4 kV and current levels in the range of 250 mA. The DPT showed cascaded voltage waveform with no voltage overshoot or oscillation and good voltage balancing, i.e. switch one held 30% of

the full voltage and switch four held 22%. This voltage balancing performance is better than presented for similar research, while the number of series connected devices has been extended from three to four devices. The switching time of the string was substantially higher than the switching time of a single device. The turn-off and turn-on times are approximately 1.4 μs and 0.7 μs, respectively. Methods for reducing the switching times were investigated and it was found that speed-up capacitors can substantially reduce the turn-on time to under 0.3 μs. However large speed-up capacitors will increase the turn-off time. It was found that a value of 33 pF gives a faster turn-on while maintaining the same turn-off time. Methods for decreasing the turn-off time were investigated, but were ineffective.

The performance of the string was evaluated in a boost converter operating in DCM. Tests showed a worsening of the voltage balancing compared to the DPTs. Switch one held 43% of the full voltage and switch four held only 12%. This is an inherent problem of the DCM mode. It was revealed that the zero current period in DCM causes large oscillations in the string voltage. It was shown that increasing the power loss in the snubber leads to better voltage balancing. Increasing the loss with a factor of three (from 0.2 W to 0.6 W per switch) the voltage of switch one was 32% of the full voltage and switch four was 18%. Suggestions to improve the voltage balancing are proposed, but not verified experimentally.

Bibliography

Abbate, Busatto, and Iannuzzo, **Sept 2010**. C. Abbate, G. Busatto, and F. Iannuzzo. *High-Voltage, High-Performance Switch Using Series-Connected IGBTs.* IEEE Transactions on Power Electronics, 25(9), 2450–2459, 2010. ISSN 0885-8993. doi: 10.1109/TPEL.2010.2049272.

Bidoggia, Maheshwari, Nielsen, Munk-Nielsen, and Blaabjerg, **Oct 2012**. B. Bidoggia, R. Maheshwari, R. Ø Nielsen, S. Munk-Nielsen, and F. Blaabjerg. Steady-state analysis of dead-time effect on bidirectional buck converters. In *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, pages 792–797, Oct 2012. doi: 10.1109/IECON.2012.6388650.

Chitta, Hong, and Torrey, **Oct 1997**. V. Chitta, Soonwook Hong, and D. A. Torrey. Series connection of IGBTs with active voltage balancing. In *Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE*, volume 2, pages 961–967 vol.2, Oct 1997. doi: 10.1109/IAS.1997.628977.

Das, Capell, Grider, Leslie, Ostop, Raju, Schutten, Nasadoski, and Hefner, **Sept 2011**. M. K. Das, C. Capell, D. E. Grider, S. Leslie, J. Ostop, R. Raju, M. Schutten, J. Nasadoski, and A. Hefner. 10 kV, 120 A SiC half H-bridge power MOSFET modules suitable for high frequency, medium voltage applications. In *2011 IEEE Energy Conversion Congress and Exposition*, pages 2689–2692, Sept 2011. doi: 10.1109/ECCE.2011.6064129.

Dimopoulos and Munk-Nielsen, **Sept 2013**. E. Dimopoulos and S. Munk-Nielsen. Serializing off-the-shelf MOSFETs by magnetically coupling their gate electrodes. In *Power Electronics and Applications (EPE), 2013 15th European Conference on*, pages 1–11, Sept 2013. doi: 10.1109/EPE.2013.6634485.

Erickson and Maksomovic, **2001**. Erickson and Maksomovic. *Fundamentals of Power Electronics.* Springer, 2nd edition, 2001.

Foster, **2013**. S. Thomas Foster. *Managing Quality Integrating the Supply Chain.* Pearson Education Limited, fifth edition, 2013.

Grass and Fischer, **Oct 2014**. N. Grass and T. Fischer. High voltage power supply and control technologies for electrostatic precipitators in biomass applications. In *Industry Applications Society Annual Meeting, 2014 IEEE*, pages 1–4, Oct 2014. doi: 10.1109/IAS.2014.6978357.

Grass, Hartmann, and Klockner, **Oct 2002**. N. Grass, W. Hartmann, and M. Klockner. Application of different types of high voltage supplies on industrial

electrostatic precipitators. In *Industry Applications Conference, 2002. 37th IAS Annual Meeting. Conference Record of the*, volume 1, pages 270–276 vol.1, Oct 2002. doi: 10.1109/IAS.2002.1044099.

Gusseme, Sype, Bossche, and Melkebeek, **April 2007**. K. De Gusseme, D. M. Van de Sype, A. P. M. Van den Bossche, and J. A. Melkebeek. *Input-Current Distortion of CCM Boost PFC Converters Operated in DCM*. IEEE Transactions on Industrial Electronics, 54(2), 858–865, 2007. ISSN 0278-0046. doi: 10.1109/TIE.2007.892252.

He, Palmer, Zhang, Snook, and Wang, **Aug 2011**. W. He, P. Palmer, X. Zhang, M. Snook, and Z. Wang. IGBT series connection under Active Voltage Control. In *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, pages 1–9, Aug 2011.

Jain, **2003**. Heena Jain. *Comparison of wide-bandgap semiconductors for Power Electronics Applications*. Recent Advances in Microwave Theory and Applications, 2008. MICROWAVE 2008, pages 878–881, 2003.

John Kuffel, E. Kuffel, **2000**. W. S. Zaengl John Kuffel, E. Kuffel. *High Voltage Engineering Fundamentals*. Newnes. Newnes, 2 edition, 2000. ISBN 9780750636346,0-7506-3634-3.

Kaminski and Hilt, **March 2012**. N. Kaminski and O. Hilt. SiC and GaN Devices - Competition or Coexistence? In *Integrated Power Electronics Systems (CIPS), 2012 7th International Conference on*, pages 1–11, March 2012.

Katupituya, **October 2015**. Jay Katupituya. *Design of Controllers - Direct Methods*. Lecture given on "Modelling and Control of mechatronic system" at University of New South Wales, 2015.

Li, Munk-Nielsen, Beczkowski, and Wang, **Sept 2014**. Helong Li, S. Munk-Nielsen, S. Beczkowski, and Xiongfei Wang. SiC MOSFETs based split output half bridge inverter: Current commutation mechanism and efficiency analysis. In *Energy Conversion Congress and Exposition (ECCE), 2014 IEEE*, pages 1581–1588, Sept 2014. doi: 10.1109/ECCE.2014.6953607.

Lynch, **2006**. Brian T. Lynch. *Under the Hood of a DC/DC Boost converter*, 2006. URL `http://www.ti.com/download/trng/docs/seminar/Topic_3_Lynch.pdf`.

Mizuno, **Oct 2000**. A. Mizuno. *Electrostatic precipitation*. Dielectrics and Electrical Insulation, IEEE Transactions on, 7(5), 615–624, 2000. ISSN 1070-9878. doi: 10.1109/94.879357.

Mohan, Undeland, and Robbins, **2003**. Mohan, Undeland, and Robbins. *Power Electronics*. John Wiley & Sons, Inc., 3rd edition, 2003.

Murthy-Bellur and Kazimierczuk, **May 2010**. D. Murthy-Bellur and M. K. Kazimierczuk. Two-switch flyback-forward PWM DC-DC converter with reduced switch voltage stress. In *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, pages 3705–3708, May 2010. doi: 10.1109/ISCAS.2010.5537766.

Nguyen-Duy, Ouyang, Knott, and Andersen, **Aug 2014**. K. Nguyen-Duy, Z. Ouyang, A. Knott, and M. A. E. Andersen. Minimization of the transformer inter-winding parasitic capacitance for modular stacking power supply applications. In *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, pages 1–10, Aug 2014. doi: 10.1109/EPE.2014.6910843.

O'Connor and Kleyner, **2012**. Patrick D. T. O'Connor and Andre Kleyner. *Practical Reliability Engineering*. John Wiley & Sons, Ltd., fifth edition, 2012.

Palmer, Zhang, and Zhang, **Nov 2015**. P. R. Palmer, J. Zhang, and X. Zhang. SiC MOSFETs connected in series with active voltage control. In *Wide Bandgap Power Devices and Applications (WiPDA), 2015 IEEE 3rd Workshop on*, pages 60–65, Nov 2015. doi: 10.1109/WiPDA.2015.7369274.

Parker, **1997**. K. R. Parker. *Applied Electrostatic Precipitation*. Chapman and Hall, 1st edition, 1997.

Philips and Parr, **2011**. Charles L. Philips and John M. Parr. *Feedback Control Systems*. Prentice Hall, 5th edition, 2011.

Rüedi, Thalheim, and Garcia, **2009**. Heinz Rüedi, Jan Thalheim, and Olivier Garcia. *Advantages of Advanced Active Clamping*. Power Electronics Europe, (8), 2009.

Riazmontazer, Rahnamaee, Mojab, Mehrnami, Mazumder, and Zefran, **March 2015**. H. Riazmontazer, A. Rahnamaee, A. Mojab, S. Mehrnami, S. K. Mazumder, and M. Zefran. Closed-loop control of switching transition of SiC MOSFETs. In *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE*, pages 782–788, March 2015. doi: 10.1109/APEC.2015.7104438.

Shammas, Withanage, and Chamund, **Feb 2006**. N. Y. A. Shammas, R. Withanage, and D. Chamund. *Review of series and parallel connection of IGBTs*. IEEE Proceedings - Circuits, Devices and Systems, 153(1), 34–39, 2006. ISSN 1350-2409. doi: 10.1049/ip-cds:20050053.

Shao, Liu, Wang, and Li, **Oct 2013**. Xianqing Shao, Congwei Liu, Ping Wang, and Zhengxi Li. A hybrid voltage balancing method for series connected IGBTs. In *Electrical Machines and Systems (ICEMS), 2013 International Conference on*, pages 2138–2142, Oct 2013. doi: 10.1109/ICEMS.2013.6713207.

Soeiro, Muhlethaler, Linner, Ranstad, and Kolar, **November 2013**. T.B. Soeiro, J. Muhlethaler, J. Linner, P. Ranstad, and J.W. Kolar. *Automated Design of a High-Power High-Frequency LCC Resonant Converter for Electrostatic Precipitators*. IEEE Transactions on Industrial Electronics, 60(11), 4805–4819, 2013. ISSN 0278-0046. doi: 10.1109/TIE.2012.2227897.

Vasarevicius, **2012**. Saulius Vasarevicius. *Comparison of different air treatment methods with palsma treatment*. PlasTEP 3rd Summer School and Trainings, 2012. URL `http://www.plastep.eu/fileadmin/dateien/Events/2012/20716-27_Summer_School/6._Vasarevicius_Air_Treatment_PlasTEP_2012.pdf`.

Vasawade, Deshmukh, and Kulkarni, **Feb 2015**. R. Vasawade, B. Deshmukh, and V. Kulkarni. Modularity in design: A review. In *Technologies for Sustainable Development (ICTSD), 2015 International Conference on*, pages 1–4, Feb 2015. doi: 10.1109/ICTSD.2015.7095892.

Vechalapu, Bhattacharya, and Aleoiza, **Nov 2015**. K. Vechalapu, S. Bhattacharya, and E. Aleoiza. Performance evaluation of series connected 1700V SiC MOSFET devices. In *Wide Bandgap Power Devices and Applications (WiPDA), 2015 IEEE 3rd Workshop on*, pages 184–191, Nov 2015. doi: 10.1109/WiPDA.2015.7369327.

Wu, Cheng, Xiao, and Sheng, **May 2014**. Xinke Wu, Shidong Cheng, Qiang Xiao, and Kuang Sheng. *A 3600 V/80 A Series–Parallel-Connected Silicon Carbide MOSFETs Module With a Single External Gate Driver*. Power Electronics, IEEE Transactions on, 29(5), 2296–2306, 2014. ISSN 0885-8993. doi: 10.1109/TPEL.2013.2287382.

Appendix A

Losses

This appendix presents the derivation of the loss governing equations of CCM_0 and DCM_+ modes.

A.1 Continuous Conduction Mode Zero (CCM_0)

The losses are split in two parts: conduction loss and switching loss. In CCM_0 the conduction losses occur in M_1, M_2, D_1 and D_2 and the switching losses contain M_1 and M_2 turn-off as well as D_1 and D_2 reverse recovery. Turn-on losses of M_1 and M_2 are neglected as when they turn-on D_1 and D_2 are already forward biased.

Conduction Loss

The conduction losses occur when each device is conducting current. In this state the MOSFETs are modeled by its on-state resistance and the diode is modeled by its forward voltage drop. Thus the equation governing the conduction loss is

$$P_{\text{cond}} = P_{\text{M1,cond}} + P_{\text{M2,cond}} + P_{\text{D1,cond}} + P_{\text{D2,cond}} \tag{A.1}$$

where

$$P_{\text{M1,cond}} = i^2_{\text{M1,RMS}} R_{\text{ds,on}} \tag{A.2}$$
$$P_{\text{M2,cond}} = i^2_{\text{M2,RMS}} R_{\text{ds,on}} \tag{A.3}$$
$$P_{\text{D1,cond}} = \langle i_{\text{D1}} \rangle V_{\text{F}} \tag{A.4}$$
$$P_{\text{D2,cond}} = \langle i_{\text{D2}} \rangle V_{\text{F}} \tag{A.5}$$

To estimate the conduction losses of the MOSFETs, two things are needed: The RMS current conducted by the MOSFET and the on-state resistance of the MOSFET. The on-state resistance is found from the device datasheets and the RMS current is calculated from the waveforms depicted in Figure 3.7 and the general piecewise formula [Erickson and Maksomovic, 2001]:

$$i_{\text{RMS}} = \sqrt{\sum_{k=1}^{n} D_k u_k} \tag{A.6}$$

where D_k is the normalized time period of the segment k and u_k is the contribution of segment k. The MOSFET current waveforms are both piecewise linear with zero segments

and each contains one trapezoidal segment. The contribution of a trapezoidal segment is given by

$$u_k = \frac{1}{3}(I_1^2 + I_1 I_2 + I_2^2) \tag{A.7}$$

where I_1 and I_2 are the maximum and minimum value of the trapezoid, respectively.

For M_1 I_2 is the maximum inductor current, $\widehat{I}_L$, and I_1 is equal to I_x given by

$$I_x = \frac{V_i}{L} T_D + \check{I}_L \tag{A.8}$$

For M_2 I_1 is the minimum inductor current, $\check{I}_L$, and I_2 is equal to I_y given by

$$I_y = \frac{V_i - V_o}{L} T_D + \widehat{I}_L \tag{A.9}$$

Applying these expressions to (A.7) and (A.6) gives the RMS current expressions:

$$i_{M1,RMS} = \sqrt{\frac{D - \tau_D}{3}\left(I_x^2 + I_x \widehat{I}_L + \widehat{I}_L^2\right)} \tag{A.10}$$

$$i_{M2,RMS} = \sqrt{\frac{1 - D - \tau_D}{3}\left(\check{I}_L^2 + \check{I}_L I_y + I_y^2\right)} \tag{A.11}$$

The conduction loss of the diodes are determined from the average diode current and the on-state voltage drop of the diode. The average diode currents are determined by geometric analysis:

$$\langle i_{D1} \rangle = \frac{1}{T_s}\int_0^{T_s} i_{D1} \mathrm{d}t = \frac{1}{T_s}\left(\frac{\left(-\check{I}_L\right) + \left(-I_x\right)}{2} T_D\right) = -\frac{1}{2}\left(\check{I}_L + I_x\right)\tau_D \tag{A.12}$$

$$\langle i_{D2} \rangle = \frac{1}{T_s}\int_0^{T_s} i_{D2} \mathrm{d}t = \frac{1}{T_s}\left(\frac{\widehat{I}_L + I_y}{2} T_D\right) = \frac{1}{2}\left(\widehat{I}_L + I_y\right)\tau_D \tag{A.13}$$

Switching Loss

The MOSFET switching losses occur when the switches turn off, i.e. at $t = DT_s$ and at $t = T_s$ for M_1 and M_2 respectively. The turn off voltage and current waveforms are approximated as depicted in Figure A.1 [Mohan et al., 2003].

From Figure A.1, the turn-off energy is calculated by

$$E_{off} = \frac{1}{2} V_d I_d (t_{rv} + t_{fi}) \tag{A.14}$$

where t_{rv} is the voltage rise time and t_{fi} is the current fall time.

During t_{rv} the gate current is given by

$$i_g = \frac{v_{Rg}}{R_g} = C_{gd}\frac{\mathrm{d}v_{gd}}{\mathrm{d}t} \approx C_{gd}\frac{\Delta v_{gd}}{t_{rv}} \Rightarrow \tag{A.15}$$

$$\frac{V_{gg} - v_{gs}}{R_g} = C_{gd}\frac{\Delta v_{gs} - \Delta v_{ds}}{t_{rv}} \tag{A.16}$$

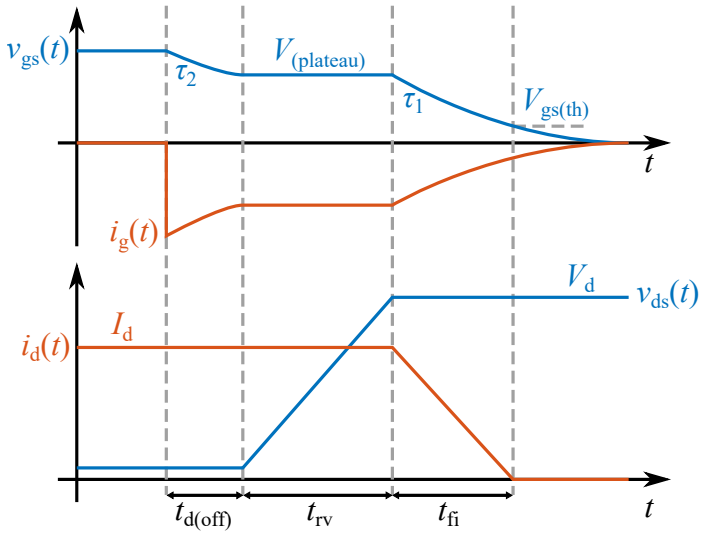


Figure A.1. Approximated voltage and current waveforms during turn-off.

where v_{Rg} is the voltage drop on the gate resistance (R_g) which is equal to the difference between the supplied voltage (V_{gg}) and the gate-source voltage. The applied voltage during t_{rv} is zero and the gate-source voltage is constant at the Miller-plateau, hence

$$\frac{-V_{(plateau)}}{R_g} = C_{gd}\frac{-\Delta v_{ds}}{t_{rv}} \Rightarrow \tag{A.17}$$

$$t_{rv} = C_{gd}R_g\frac{\Delta v_{ds}}{V_{(plateau)}} \tag{A.18}$$

The drain-source voltage changes from the on-state voltage to the off-state voltage:

$$\Delta v_{ds} = V_d - I_d R_{ds,on} \tag{A.19}$$

During t_{fi} the gate-source voltage drops exponentially from $V_{(plateau)}$ to zero:

$$v_{gs}(t) = A\left(1 - e^{-\frac{t}{\tau_1}}\right) + B \tag{A.20}$$

The constants A and B are found from the boundary conditions:

$$\left.\begin{aligned} v_{gs}(0) &= V_{(plateau)} \\ v_{gs}(\infty) &= 0 \end{aligned}\right\} \Rightarrow \begin{cases} A &= -V_{(plateau)} \\ B &= V_{(plateau)} \end{cases} \tag{A.21}$$

The time constant, τ_1 is given by

$$\tau_1 = R_g(C_{gd} + C_{gs}) \tag{A.22}$$

At $t = t_{fi}$ the gate-source voltage has reached the gate threshold voltage, $V_{gs(th)}$:

$$v_{gs}(t_{fi}) = V_{gs(th)} = -V_{(plateau)}\left(1 - e^{-\frac{t_{fi}}{R_g(C_{gd}+C_{gs})}}\right) + V_{(plateau)} \Rightarrow \tag{A.23}$$

$$t_{fi} = -R_g(C_{gd} + C_{gs})\ln\left(\frac{V_{gs(th)}}{V_{(plateau)}}\right) \tag{A.24}$$

Thus the current fall time is determined by (A.24).

For M_1 the current drops to zero from the maximum inductor current, $\widehat{I}_L$ and for M_2 the initial current value is $-\breve{I}_L$. For both switches the voltage rises to the output voltage, V_o. Thus the switching losses of the MOSFETs are given by

$$P_{M1,sw} = \frac{1}{2} V_o \widehat{I}_L (t_{tv} - t_{fi}) f_s \tag{A.25}$$

$$P_{M2,sw} = -\frac{1}{2} V_o \breve{I}_L (t_{tv} - t_{fi}) f_s \tag{A.26}$$

At turn-off, the body diode of the MOSFET experiences reverse recovery, where the built up charge in the diode is removed by the negative voltage applied to the diode. The reverse recovery waveforms of a diode, are shown as dotted lines in Figure A.2, with piecewise linear approximations indicated by solid lines.

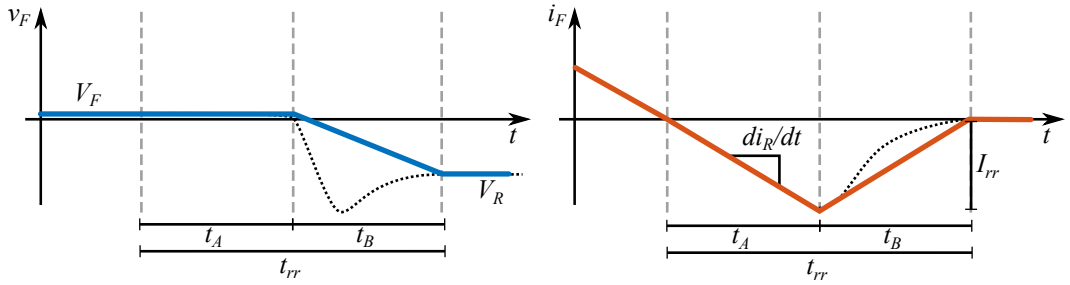


Figure A.2. Diode reverse recovery. Dashed lines show general waveforms, while solid are the linear approximations used for calculations.

The total reverse recovery time, t_{rr}, is made up by two time periods t_A and t_B. From the figure the time t_A is calculated as

$$I_{rr} = \left(\frac{di_R}{dt}\right) \cdot t_A \qquad \Rightarrow \qquad t_A = \frac{I_{rr}}{\left(\frac{di_R}{dt}\right)} \tag{A.27}$$

Thus the time period, t_B in which the dominant reverse recovery losses occur is calculated by

$$t_B = t_{rr} - \frac{I_{rr}}{\frac{di_R}{dt}} \tag{A.28}$$

During t_B the current is approximated by the line $i(t) = -\frac{I_{rr}}{t_B} t + I_{rr}$ and the voltage by $v(t) = \frac{V_R}{t_B} t$, which is why the power loss during t_B is given by

$$p(t) = -\frac{V_R I_{rr}}{t_B^2} t^2 + \frac{V_R I_{rr}}{t_B} t \tag{A.29}$$

The average power loss over the switching period, due to reverse recovery of the diode, is calculated by the energy loss during t_B times the switching frequency:

$$\begin{aligned} P_{D,rr} = E_{rr} f_s &= \left(\int_0^{t_B} \left(-\frac{V_R I_{rr}}{t_B^2} t^2 + \frac{V_R I_{rr}}{t_B} t \right) dt \right) f_s \\ &= \frac{1}{6} V_R I_{rr} t_B f_s \end{aligned} \tag{A.30}$$

For both D_1 and D_2, the blocking voltage V_R is equal to the output voltage, V_o, hence the reverse recovery loss of each of the diodes are

$$P_{D1,rr} = \frac{1}{6} V_o I_{rr} t_B f_s \tag{A.31}$$

$$P_{D2,rr} = \frac{1}{6} V_o I_{rr} t_B f_s \tag{A.32}$$

A.2 Positive Discontinuous Conduction Mode (DCM$_+$)

The losses in DCM$_+$ are limited to conduction loss in M_1, M_2 and D_2 and switching loss in M_1 (turn-off) and reverse recovery in D_2.

A.2.1 Conduction Loss

The governing equations for the conduction loss remain (A.1)-(A.5).

$$P_{cond} = P_{M1,cond} + P_{M2,cond} + P_{D1,cond} + P_{D2,cond} \tag{A.1 revisited}$$

where

$$P_{M1,cond} = i^2_{M1,RMS} R_{ds,on} \tag{A.2 revisited}$$

$$P_{M2,cond} = i^2_{M2,RMS} R_{ds,on} \tag{A.3 revisited}$$

$$P_{D2,cond} = \langle i_{D2} \rangle V_F \tag{A.5 revisited}$$

The MOSFET RMS currents in DCM$_+$ are

$$i_{M1,RMS} = \sqrt{\frac{D - \tau_D}{3} \widehat{I}_L^2} = \sqrt{\frac{D - \tau_D}{3}} \widehat{I}_L \tag{A.33}$$

$$i_{M2,RMS} = \sqrt{\frac{D_B - \tau_D}{3} I_y^2} = \sqrt{\frac{D_B - \tau_D}{3}} I_y \tag{A.34}$$

where

$$D_B = -\widehat{I}_L \frac{L}{T_s(V_i - V_o)} = -\frac{V_i}{V_i - V_o}(D - \tau_D) \tag{A.35}$$

The average D_2 current is given by

$$\langle i_{D2} \rangle = \frac{1}{2}(\widehat{I}_L + I_y)\tau_D \tag{A.36}$$

A.2.2 Switching Loss

The M_1 switching loss is the same in DCM$_+$ as for CCM$_0$, i.e.

$$P_{M1,sw} = \frac{1}{2} V_o \widehat{I}_L R_g C_{gd} \left(\frac{V_o - \widehat{I}_L R_{ds,on}}{V_{(plateau)}} - \left(1 + \frac{C_{gs}}{C_{gd}}\right) \ln\left(\frac{V_{gs(th)}}{V_{(plateau)}}\right) \right) f_s \tag{A.37}$$

D_2 is reverse biased by $V_i - V_o$ and the loss is therefore

$$P_{D2,rr} = \frac{1}{6}(V_i - V_o) I_{rr} \left(t_{rr} - \frac{I_{rr}}{\frac{di_R}{dt}} \right) f_s \tag{A.38}$$

Appendix B

Control Derivation

This appendix presents the derivation of continuous time transfer functions of the converter. The continuous time transfer functions are converted to discrete time transfer functions and controllers are designed.

B.1 Continuous Time Transfer Function

The system will normally operate in one of two mode: DCM_+ and CCM_-. The continuous time transfer function of the two modes are different. Each are derived in this section.

B.1.1 DCM_+

The average output current in DCM_+ is given by

$$\langle i_\mathrm{o}\rangle = \frac{1}{T_\mathrm{s}}\left(\frac{1}{2}\widehat{I}_\mathrm{L} d_\mathrm{B}\right) = -\frac{\langle v_\mathrm{i}\rangle^2\langle d\rangle^2 T_\mathrm{s}}{2L(\langle v_\mathrm{i}\rangle - \langle v_\mathrm{o}\rangle)} \tag{B.1}$$

where

$$\widehat{I}_\mathrm{L} = \frac{\langle v_\mathrm{i}\rangle}{L}\langle d\rangle T_\mathrm{s}$$
$$d_\mathrm{B} = -\frac{\langle v_\mathrm{i}\rangle}{\langle v_\mathrm{i}\rangle - \langle v_\mathrm{o}\rangle}\langle d\rangle$$

The small signal output current, $(\widetilde{i_\mathrm{o}})$ is found by linearization using Taylor series expansion at the operating point $\langle v_\mathrm{i}\rangle = V_\mathrm{i}, \langle d\rangle = D, \langle v_\mathrm{o}\rangle = V_\mathrm{o}$:

$$\widetilde{i_\mathrm{o}} = \left.\frac{\partial\langle i_\mathrm{o}\rangle}{\partial\langle v_\mathrm{i}\rangle}\right|_{\substack{\langle v_\mathrm{i}\rangle=V_\mathrm{i}\\ \langle v_\mathrm{o}\rangle=V_\mathrm{o}\\ \langle d\rangle=D}} \widetilde{v_\mathrm{i}} + \left.\frac{\partial\langle i_\mathrm{o}\rangle}{\partial\langle v_\mathrm{o}\rangle}\right|_{\substack{\langle v_\mathrm{i}\rangle=V_\mathrm{i}\\ \langle v_\mathrm{o}\rangle=V_\mathrm{o}\\ \langle d\rangle=D}} \widetilde{v_\mathrm{o}} + \left.\frac{\partial\langle i_\mathrm{o}\rangle}{\partial\langle d\rangle}\right|_{\substack{\langle v_\mathrm{i}\rangle=V_\mathrm{i}\\ \langle v_\mathrm{o}\rangle=V_\mathrm{o}\\ \langle d\rangle=D}} \widetilde{d} \tag{B.2}$$

$$= -\frac{V_\mathrm{i}D^2T_\mathrm{s}(V_\mathrm{i}-2V_\mathrm{o})}{2L(V_\mathrm{i}-V_\mathrm{o})^2}\widetilde{v_\mathrm{i}} - \frac{V_\mathrm{i}^2DT_\mathrm{s}}{L(V_\mathrm{i}-V_\mathrm{o})}\widetilde{d} - \frac{V_\mathrm{i}^2D^2T_\mathrm{s}}{2L(V_\mathrm{i}-V_\mathrm{o})^2}\widetilde{v_\mathrm{o}} \tag{B.3}$$

The output current is determined from the output voltage and the RC load:

$$\widetilde{i_\mathrm{o}} = \frac{\widetilde{v_\mathrm{o}}}{R} + C\frac{\mathrm{d}\widetilde{v_\mathrm{o}}}{\mathrm{d}t} \quad \xrightarrow{\mathscr{L}} \quad \widetilde{i_\mathrm{o}} = \left(\frac{1}{R} + Cs\right)\widetilde{v_\mathrm{o}} \tag{B.4}$$

In the Laplace domain (B.3) becomes

$$\left[Cs + \frac{1}{R} + \frac{V_\mathrm{i}^2D^2T_\mathrm{s}}{2L(V_\mathrm{i}-V_\mathrm{o})^2}\right]\widetilde{v_\mathrm{o}} = \left[\frac{V_\mathrm{i}D^2T_\mathrm{s}(V_\mathrm{i}-2V_\mathrm{o})}{2L(V_\mathrm{i}-V_\mathrm{o})}\right]\widetilde{v_\mathrm{i}} - \left[\frac{V_\mathrm{i}^2DT_\mathrm{s}}{L(V_\mathrm{i}-V_\mathrm{o})}\right]\widetilde{d} \tag{B.5}$$

The control-to-output transfer function is determined from (B.5), by regarding the input voltage small signal pertubation as zero, i.e.

$$G_{\mathrm{vo}}(s) = \left.\frac{\widetilde{v_{\mathrm{o}}}}{\widetilde{d}}\right|_{\widetilde{v_{\mathrm{i}}}=0} = \frac{-\frac{V_{\mathrm{i}}^2 D T_{\mathrm{s}}}{LC(V_{\mathrm{i}}-V_{\mathrm{o}}}}{s+\frac{1}{RC}+\frac{V_{\mathrm{i}}^2 D^2 T_{\mathrm{s}}}{2LC(V_{\mathrm{i}}-V_{\mathrm{o}})^2}} = \frac{K}{s-p} \tag{B.6}$$

where

$$K = -\frac{V_{\mathrm{i}}^2 D T_{\mathrm{s}}}{LC(V_{\mathrm{i}}-V_{\mathrm{o}}}$$
$$p = -\frac{1}{RC}+\frac{V_{\mathrm{i}}^2 D^2 T_{\mathrm{s}}}{2LC(V_{\mathrm{i}}-V_{\mathrm{o}})^2}$$

At the operating point of Table 3.5 in Section 3.2.2 the transfer function is

$$G_{\mathrm{vo}}(s) = \frac{3.1\times 10^6}{(s+554.9)} \tag{B.7}$$

This is a first order transfer function with a gain of 3.1×10^6 and a pole at 554.9.

B.1.2 CCM_

In CCM_ a slightly different approach is used to find the control-to-output transfer function. The average inductor voltage and capacitor current equations are analyzed:

$$\langle v_{\mathrm{L}}\rangle = \frac{1}{T_{\mathrm{s}}}(\langle v_{\mathrm{i}}\rangle\langle d\rangle T_{\mathrm{s}} + (\langle v_{\mathrm{i}}\rangle - \langle v_{\mathrm{o}}\rangle)(1-\langle d\rangle)T_{\mathrm{s}}) = \langle v_{\mathrm{i}}\rangle - \langle v_{\mathrm{o}}\rangle(1-\langle d\rangle) \tag{B.8}$$

$$\langle i_{\mathrm{C}}\rangle = \frac{1}{T_{\mathrm{s}}}\left(-\frac{\langle v_{\mathrm{o}}\rangle}{R}\langle d\rangle T_{\mathrm{s}} + \left(\langle i_{\mathrm{L}}\rangle - \frac{\langle v_{\mathrm{o}}\rangle}{R}\right)(1-\langle d\rangle)T_{\mathrm{s}}\right) = \langle i_{\mathrm{L}}\rangle(1-\langle d\rangle) - \frac{\langle v_{\mathrm{o}}\rangle}{R} \tag{B.9}$$

To linearise the time variant expressions are replaced with a quiescent part and a small signal perturbation ($\langle y\rangle = Y + \widetilde{y}$). The parentheses are multiplied. Terms including only quiescent parts are ignored. Second order terms ($\widetilde{y}^2$) are likewise ignored. (B.10) and (B.11) are obtained.

$$\widetilde{v_{\mathrm{L}}} = \widetilde{v_{\mathrm{i}}} - (1-D)\widetilde{v_{\mathrm{o}}} - V_{\mathrm{o}}\widetilde{d} = L\frac{\mathrm{d}\widetilde{i_{\mathrm{L}}}}{\mathrm{d}t} \tag{B.10}$$

$$\widetilde{i_{\mathrm{C}}} = (1-D)\widetilde{i_{\mathrm{L}}} - I_{\mathrm{L}}\widetilde{d} - \frac{1}{R}\widetilde{v_{\mathrm{o}}} = C\frac{\mathrm{d}\widetilde{v_{\mathrm{o}}}}{\mathrm{d}t} \tag{B.11}$$

(B.10) and (B.11) are converted to the Laplace domain, $\widetilde{i_{\mathrm{L}}}$ is isolated and the two equations are combined:

$$\widetilde{i_{\mathrm{L}}} = \frac{1}{Ls}\left(\widetilde{v_{\mathrm{i}}} - (1-D)\widetilde{v_{\mathrm{o}}} - V_{\mathrm{o}}\widetilde{d}\right) \tag{B.12}$$

$$Cs\widetilde{v_{\mathrm{o}}} = \frac{1-D}{Ls}\left(\widetilde{v_{\mathrm{i}}} - (1-D)\widetilde{v_{\mathrm{o}}} - V_{\mathrm{o}}\widetilde{d}\right) - I_{\mathrm{L}}\widetilde{d} - \frac{1}{R}\widetilde{v_{\mathrm{o}}} \tag{B.13}$$

$$\Rightarrow \left[Cs + \frac{(1-D)^2}{Ls} + \frac{1}{R}\right]\widetilde{v_{\mathrm{o}}} = \left[\frac{1-D}{Ls}\right]\widetilde{v_{\mathrm{i}}} - \left[\frac{V_{\mathrm{o}}(1-D)}{Ls} + I_{\mathrm{L}}\right]\widetilde{d} \tag{B.14}$$

Now the control-to-output transfer function is determined:

$$G_{\mathrm{vo}}(s) = \left.\frac{\widetilde{v_{\mathrm{o}}}}{\widetilde{d}}\right|_{\widetilde{v_{\mathrm{i}}}=0} = \frac{-\frac{I_{\mathrm{L}}}{C}s - \frac{V_{\mathrm{o}}(1-D)}{LC}}{s^2+\frac{1}{RC}s+\frac{(1-D)^2}{LC}} = \frac{K(s+z_1)}{(s-p_1)(s-p_2)} \tag{B.15}$$

where

$$K = -\frac{I_{\mathrm{L}}}{C}$$
$$z_1 = \frac{I_{\mathrm{L}} V_{\mathrm{o}}(1-D)}{L}$$
$$p_1 = \frac{1}{2RC} + \sqrt{\frac{1}{(RC)^2} - 4\frac{(1-D)^2}{LC}}$$
$$p_2 = \frac{1}{2RC} - \sqrt{\frac{1}{(RC)^2} - 4\frac{(1-D)^2}{LC}}$$

At the given operating point this becomes

$$G_{\mathrm{vo}}(s) = \frac{-4.1 \times 10^6 (s + 2.9 \times 10^5)}{(s^2 + 163.4s + 4.8 \times 10^7)} \tag{B.16}$$

In CCM_ the continuous time transfer function is of second order.

B.2 Controller Design

The method used for designing the controller is the direct method also known as Ragazzini's method [Katupituya, 2015]. The method is based on the general feedback control structure shown in Figure B.1 consisting of a plant, $G_{\mathrm{p}}(z)$ and a controller, $C(z)$. The output signal (C) is compared to the reference (R) to give an error value (E), which is fed to the controller that acts on the plant to give the output.

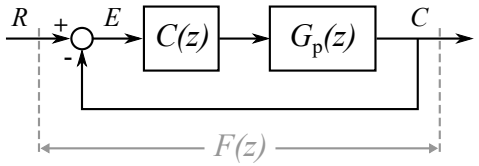


Figure B.1. General feedback control loop.

This loop is simplified to a single expression called the closed loop transfer function ($F(z)$), which is given by

$$F(z) = \frac{C(z)G_{\mathrm{p}}(z)}{1 + C(z)G_{\mathrm{p}}(z)} \tag{B.17}$$

In the direct method the idea is that the plant is known, thus by establishing a desired closed loop transfer function, the controller can be determined directly from (B.17), i.e.

$$C(z) = \frac{1}{G_{\mathrm{p}}(z)} \frac{F(z)}{1 - F(z)} \tag{B.18}$$

In the case of this project the desired closed loop transfer function should have the characteristics of a first order response, i.e. the form

$$F(z) = \frac{b_0}{z - p_1} \tag{B.19}$$

where b_0 is the gain and p_1 is the location of the pole. The pole location is determined by the time constant that is wanted. For a fast response the desired time constant is set to the sample time, T_z, which corresponds to a pole location of

$$p_1 = \mathrm{e}^{-\frac{T_\mathrm{z}}{T_\mathrm{z}}} = \mathrm{e}^{-1} \approx 0.37 \tag{B.20}$$

the gain is determined so that it gives zero steady state error, i.e.

$$F(z)|_{z=1} = 1 \tag{B.21}$$

B.2.1 DCM$_+$

The first step in the controller design is obtaining the plant transfer function. The continuous time transfer function of (B.6) is discretized. Also the zero order hold (ZOH) which converts the discrete time values to a continuous signal and a delay is included in the plant transfer function. The delay represents the time delay between the controller calculates a new duty cycle value until it is actually updated at the next switching period. The continuous time transfer functions of the ZOH and the delay are

$$ZOH(s) = \frac{1 - \mathrm{e}^{-sT_\mathrm{z}}}{s} \tag{B.22}$$

$$delay(s) = \mathrm{e}^{-sT_\mathrm{z}} \tag{B.23}$$

Then the discretized transfer function is found using partial fraction expansion and lookup tables [Philips and Parr, 2011].

$$G_\mathrm{vo}(z) = \mathcal{Z}\left\{ZOH(s)delay(s)G_\mathrm{vo}(s)\right\} = \mathcal{Z}\left\{\frac{1 - \mathrm{e}^{-sT_\mathrm{z}}}{s}\mathrm{e}^{-sT_\mathrm{z}}\frac{K}{s-p}\right\} \tag{B.24}$$

$$= \frac{K\left(\mathrm{e}^{pT_\mathrm{z}} - 1\right)}{z\left(\mathrm{e}^{pT_\mathrm{z}} - z\right)} \tag{B.25}$$

Inserting numbers yields

$$G_\mathrm{vo}(z) = \frac{62.3}{z(z - 0.989)} \tag{B.26}$$

In the discretized version, the order of the transfer function is increased by one. This must be reflected in the closed loop transfer function to fulfil the causality constraint, i.e. the closed loop transfer function must be of the same or higher order as the plant. Otherwise, the controller requires access to future error values, which is not possible. The causality constraint is ensured by introducing a pole in $z = 0$ to $F(z)$:

$$F(z) = \frac{b_0}{z(z - p_1)} \tag{B.27}$$

The pole location is unchanged and b_0 is found by

$$1 = F(z)|_{z=1} = \frac{b_0}{1 - p_1} \quad \Rightarrow \quad b_0 = 1 - p_1 \approx 0.63 \tag{B.28}$$

Now $C(z)$ is determined from (B.18):

$$C(z) = \frac{1}{\frac{62.3}{z(z-0.99)}} \cdot \frac{\frac{0.63}{z(z-0.37)}}{1 - \frac{0.63}{z(z-0.37)}} = \frac{0.01z(z-0.99)}{(z-1)(z+0.63)} \tag{B.29}$$

B.2.2 CCM_

A similar approach is used for the CCM_ controller. The discrete time plant transfer function is

$$G_{\mathrm{vo}}(z) = \mathcal{Z}\left\{\frac{1-\mathrm{e}^{-sT_{\mathrm{z}}}}{s}\mathrm{e}^{-sT_{\mathrm{z}}}\frac{K(s+z_1)}{(s-p_1)(s-p_2)}\right\} = \frac{-321(z+0.49)}{z(z^2-1.98z+0.10)} \tag{B.30}$$

This transfer function has a third order denominator which means that a double pole at $z = 0$ must be included in the closed loop transfer function. Also the transfer function has a zero location in the left half plane (LHP). If this zero is canceled, there will be a permanent branch at this location which will cause oscillation. Therefore the LHP zero must be included in the closed loop transfer function if this is to be avoided. Hence $F(z)$ becomes

$$F(z) = \frac{b_0(z+0.49)}{z^2(z-0.37)} \tag{B.31}$$

Again $C(z)$ is determined directly from the desired closed loop response and the plant:

$$C(z) = \frac{-0.0013z(z^2-1.98z+0.10)}{(z-1)(z^2+0.63z+0.21)} \tag{B.32}$$

B.3 PLECS Simulation

A PLECS simulation is conducted to verify the control strategy and design described in Section 3.3.2 and Section B.2. The simulation schematic is shown in Figure B.2. The converter is modeled with ideal components, i.e. on-state voltages, series resistances or parasitics are not modeled. The control is implemented based on the principle of Figure 3.12.

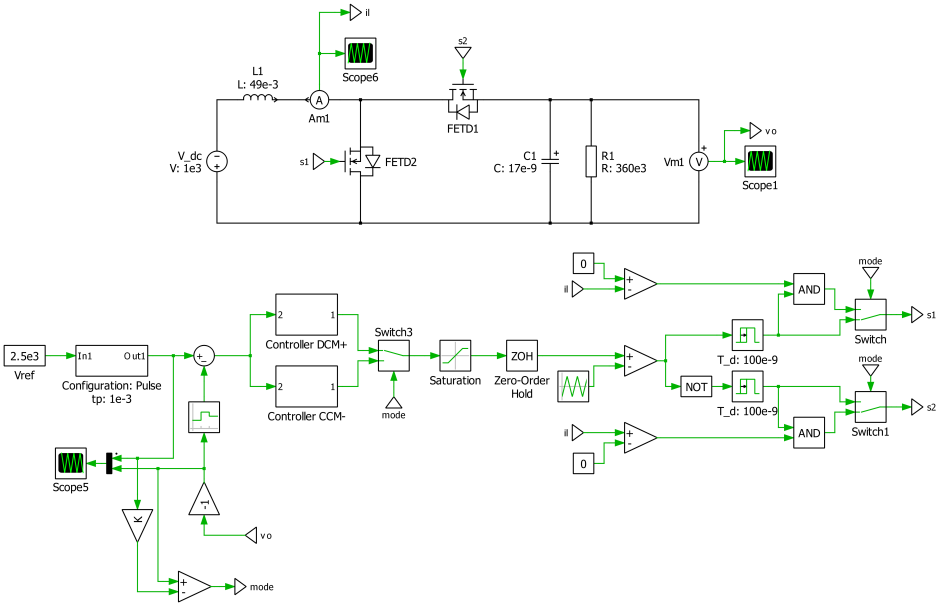


Figure B.2. PLECS simulation schematic.

Appendix C

LabVIEW Description

The control of the experimental setup is done on a compactRIO 9030 by National Instruments, as shown in Figure C.1. The compactRIO includes an field-programmable gate array (FPGA) offering fast access to input/output (I/O) hardware modules, enabling generation of gate signals. Actions are run in parallel which ensures low jitter in timing between each iteration. The FPGA is programmed in LabVIEW and the program is synthesized into a bitfile configuring the hardware layout of the FPGA. This renders the platform flexible and allows it to be easily reconfigured between tests. Additionally, for safety reasons the experimental setup is placed inside a test cage, and must therefore be controlled remotely. Communication between a LabVIEW Graphical User Interface (GUI) on the PC and the compactRIO is made relatively easy through its shared variables.

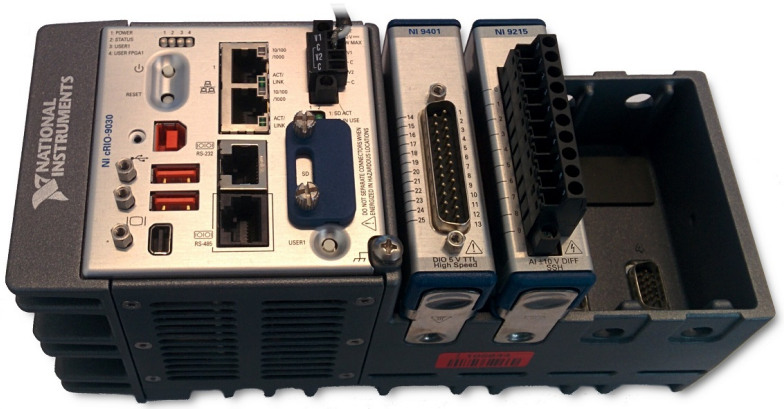


Figure C.1. Picture of the NI cRIO-9030 used to control the test setup.

The LabVIEW VIs presented in this chapter, which are located on the attached CD [1], require the following software (or newer) to be installed on the host PC (preferably installed in the following order to ensure compatibility).

- LabVIEW 2015 (32-bit)
- LabVIEW 2015 FPGA Module
- LabVIEW 2015 Real-Time module
- LabVIEW 2015 FPGA Xilinx Tools
- NI CompactRIO 15.0
- LabVIEW driver for Magna-Power DC power supplies [2]

[1] `/labview/`
[2] Available for download at http://www.magna-power.com/support/download-center#Drivers

C.1 Programming of FPGA

The following section includes a description of some of the most important features programmed in the FPGA unit of the CompactRIO. A general description of the functionality of the block diagrams are given. For some of the block diagrams a detailed description is given, but can be omitted for the reader who is more concerned with the overall functionality, rather than how the programming is done in LabVIEW.

C.1.1 Generation of gate signals

The following subsection describes how to program the FPGA to output gate signals for the MOSFET strings. This requires precise timing. The block diagram used to generate ticks used for timing in each switching period is shown in Figure C.2, and runs in a large main-loop on the FPGA. In summary Figure C.2 is a clock cycle counter, which resets every time the counter reaches the value of "`period ticks`". The FPGA runs on a 40 MHz clock, thus to ensure a 50 kHz switching period, the period ticks must be set to $\frac{40\,\text{MHz}}{50\,\text{kHz}} = 800$.

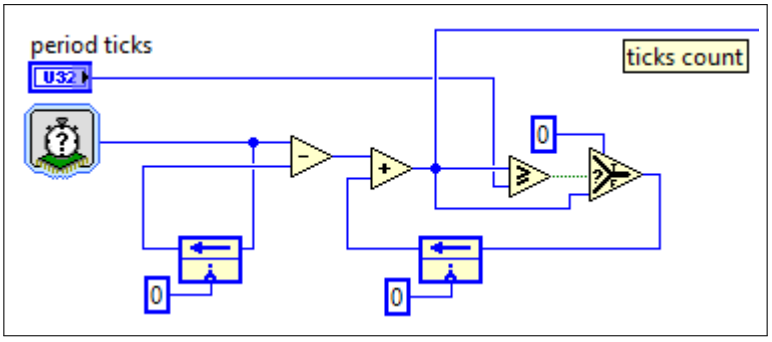


Figure C.2. LabVIEW blockdiagram to supply the counter ticks used for the timing of control.

Detailed description of Figure C.2 Shift registers of Figure C.2 are all initialized to zero. The clock signal furthest to the left of Figure C.2 is a 32-bit unsigned integer which continuously counts clock ticks. This value is subtracted with a value from a shift-register. The output of the subtraction are number of new ticks since previous loop execution. These new ticks are either accumulated or reset to zero. The choice of this depends on the true/false selection block. If the accumulated ticks exceed the value of "`period ticks`" it will be reset to zero, otherwise the ticks are accumulated.

Figure C.3 shows how gate signals are generated, when dead time and duty cycle are specified from the GUI. The ticks counter, which is the output of Figure C.2, is used for all of the comparisons. The gate signal of PWM channel 1 is high when the ticks counter is within the limits of the duty cycle and dead time, which are all converted to tick values. PWM channel 2 is high when the tick counter is within the value of the duty cycle and until the end of the switching period, but delayed by the value of the dead time. The boolean value of PWM channel 1 and 2 are fed to the digital I/O module.

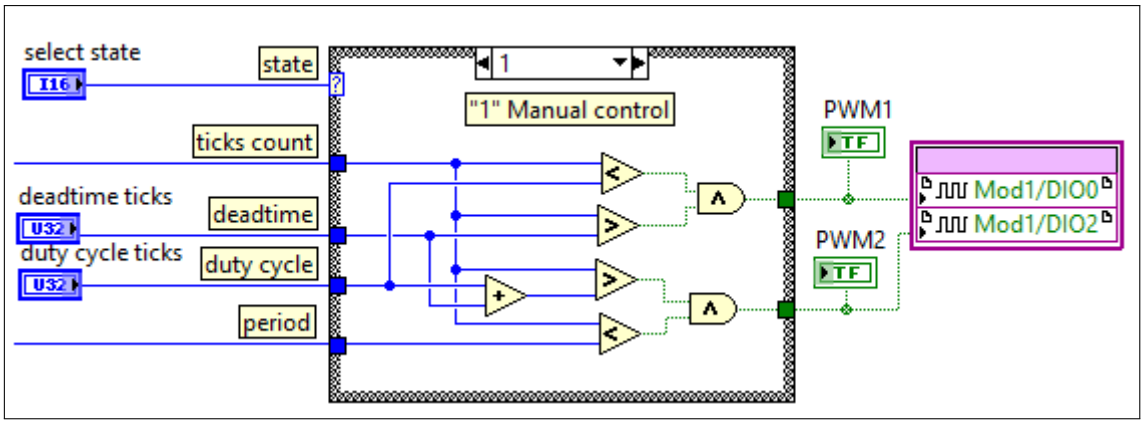


Figure C.3. LabVIEW blockdiagram to generate gate signals.

C.1.2 Double pulse test

For the double pulse test a single sequence of gate signals needs to be executed before the output is kept low. The LabVIEW blockdiagram for this is shown in Figure C.4. When enabled from the GUI the FPGA turns the output signal on for a time t_1, then off for t_2, on again for t_3, after which it keeps the output off.

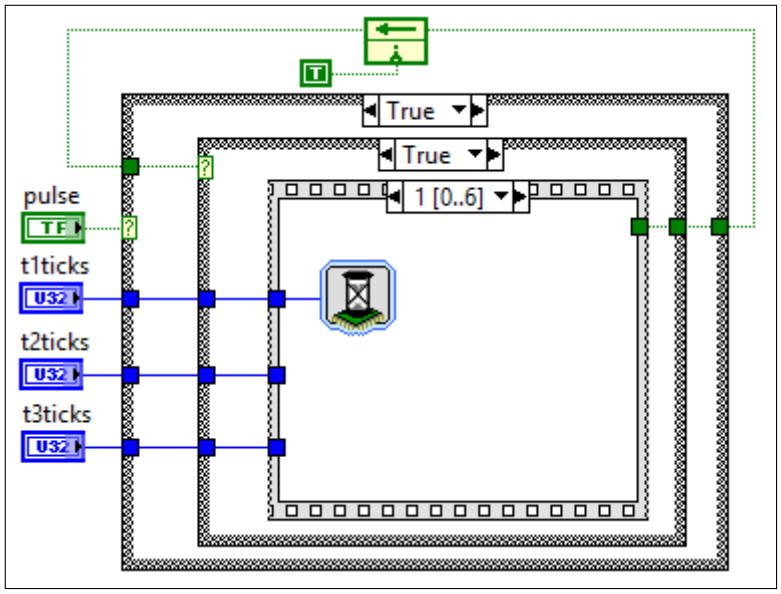


Figure C.4. LabVIEW blockdiagram to generate gate signal for the double pulse test.

Detailed description of Figure C.4 Once "`Pulse`" is pressed the outer case structure becomes true. The feedback node is initialized with "`True`", meaning that the inner case structure is enabled. This case structure contains a stacked sequence of digital output controls followed by a delay structure in the following sequence frame. Once all frames of the stacked sequence are executed, the outer feedback loop is set to "`False`", ensuring that the pulse is only generated a single time.

C.2 Power supply control

A Magna Power supply is used to power the setup, and is controlled through Ethernet interface from a host PC. By installing "LabVIEW driver for Magna-Power DC power supplies" it is possible to integrate the control of the supplies directly in the LabVIEW host program.

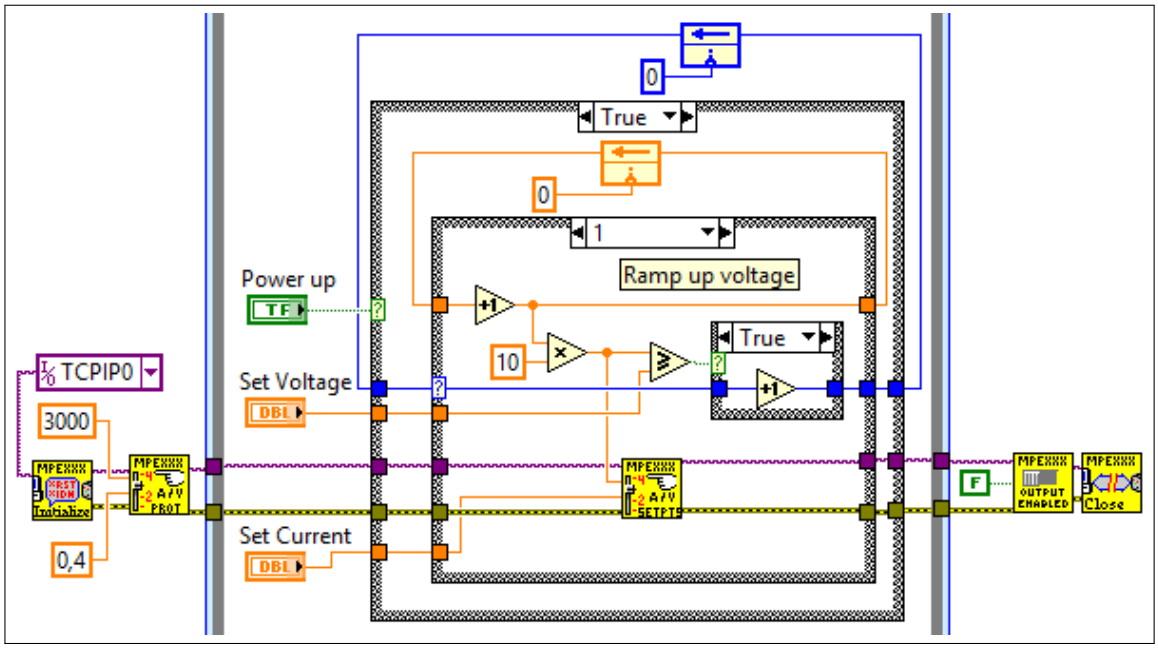


Figure C.5. LabVIEW blockdiagram to control the Magna power supply.

The LabVIEW block diagram shown in Figure C.5, uses the Magna power supply control blocks labelled "`MPEXXX`". In summary the block diagram connects to the power supply. The power supply has an over current protection mechanism, which means that if initially the voltage is set to a too high value, a large current is drawn from the power supply to charge the DC-link. This triggers the over current protection and the power supply enters a fault state. For this reason a loop is run which increases the voltage at each iteration until the desired voltage level is reached. The power supply is turned off by the user on the GUI or if an error occurs which stops the main loop from running.

Detailed description of Figure C.5 Before entering the timed loop structure, the program connects to the Magna power supply with the specified IP address. The IP address can be found through NI MAX as a remote system (or if this fails a "Remote Interface Panel" is available at the Magna power supply website[a], which scans the network for available Magna power supplies and the IP can be read). Next the over current and over voltage protection values are set. Inside the timed loop structure, the power supply is turned on when the "`Power up`" button on the GUI is pressed, which sets the outer boolean structure to true. In the true state there is an inner case structure which iterates through three states. The feedback node (blue) initializes with value 0, in which the power supply is turned on and continues to state two, which is shown in Figure 1.8. Here the voltage setpoint is increased by a value of 10 V at every

iteration by incrementing the inner feedback node (orange). This continues until the voltage is at the value contained in the "`Set voltage`" GUI-control input, at which the "$\geqslant$" structure becomes true and the inner case structure continues to its next state. In this state the voltage is simply monitored and displayed on the GUI. If the loop is stopped the power supply is turned off and the connection to it is closed.

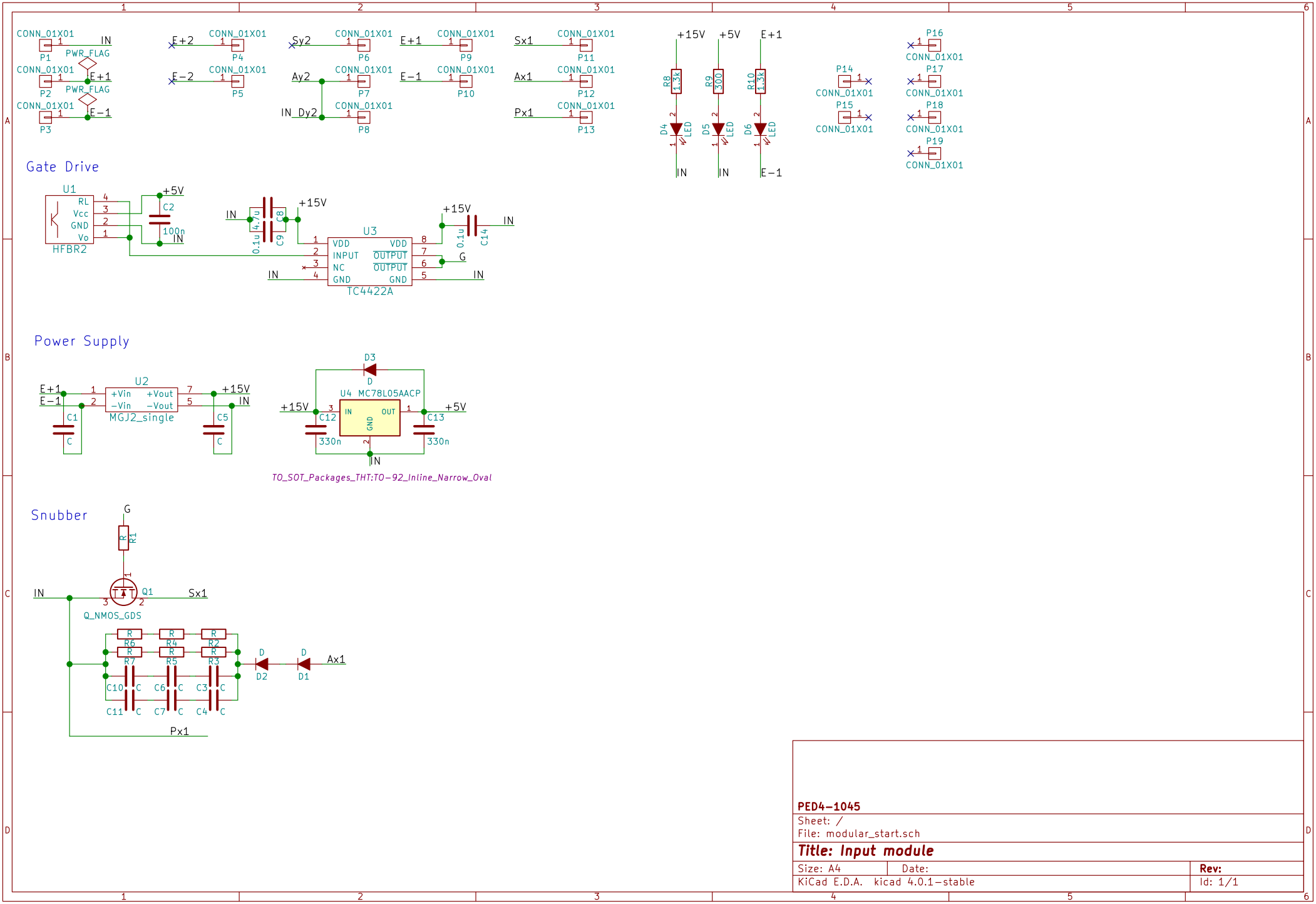
[a] Available at http://www.magna-power.com/files/software/ris_panel/ris_panel_1.25.zip

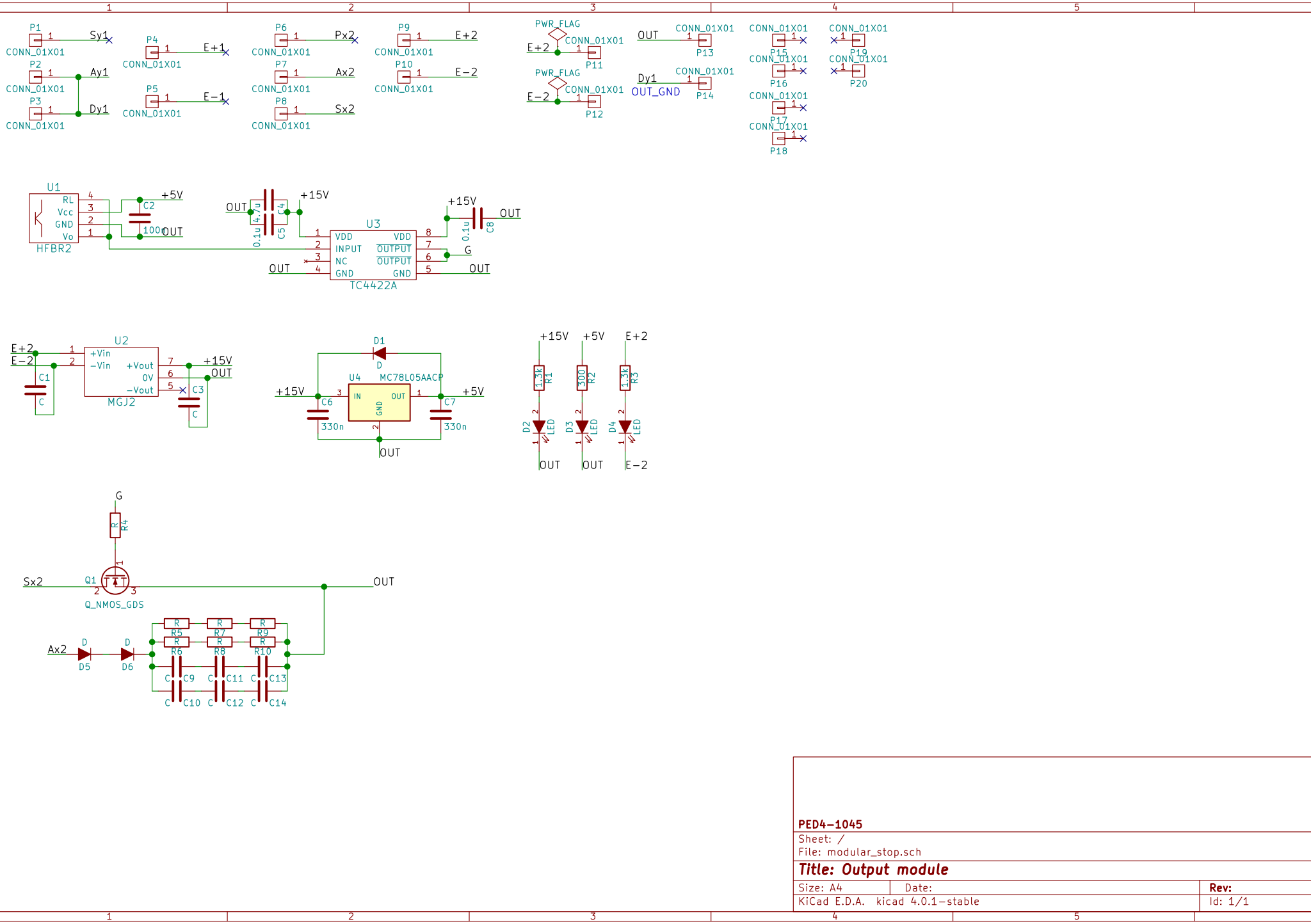
Appendix D

PCB Schematics

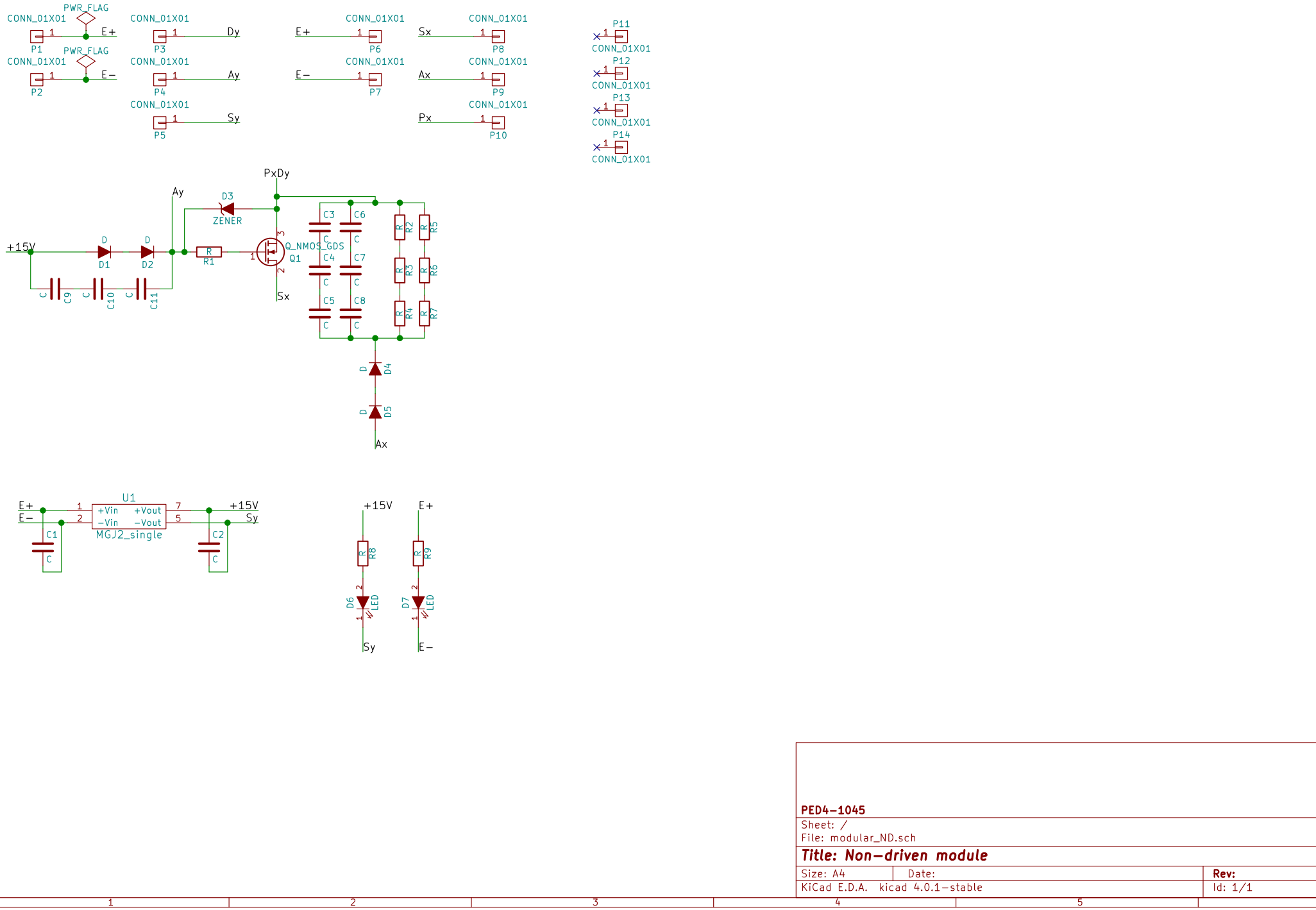
PCBs are designed in KiCAD. The schematics of the input module, output module, non-driven modules and driver module are included in this appendix. The schematics are also available on the attached CD [1]

[1] /KiCAD/


CONN_01X01
P1
IN
PWR_FLAG
P2
E+1
P3
E-1
E+2
P4
E-2
P5
Sy2
P6
Ay2
P7
IN_Dy2
P8
E+1
P9
E-1
P10
Sx1
P11
Ax1
P12
Px1
P13
+15V
+5V
R8
1.3k
R9
300
R10
1.3k
D4
D5
D6
LED
P14
P15
P16
P17
P18
P19
Gate Drive
U1
HFBR2
RL
Vcc
GND
Vo
C2
100n
C8
4.7u
C9
0.1u
U3
TC4422A
VDD
INPUT
NC
OUTPUT
C14
G
Power Supply
U2
MGJ2_single
+Vin
-Vin
+Vout
-Vout
C1
C5
D3
U4 MC78L05AACP
IN
OUT
GND
C12
330n
C13
TO_SOT_Packages_THT:TO-92_Inline_Narrow_Oval
Snubber
R1
Q1
Q_NMOS_GDS
Sx1
R6
R4
R2
R7
R5
R3
D2
D1
Ax1
C10
C6
C3
C11
C7
C4
Px1
PED4-1045
Sheet: /
File: modular_start.sch
Title: Input module
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 4.0.1-stable
Id: 1/1



PED4-1045		
Sheet: /		
File: modular_stop.sch		
Title: Output module		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 4.0.1-stable		Id: 1/1

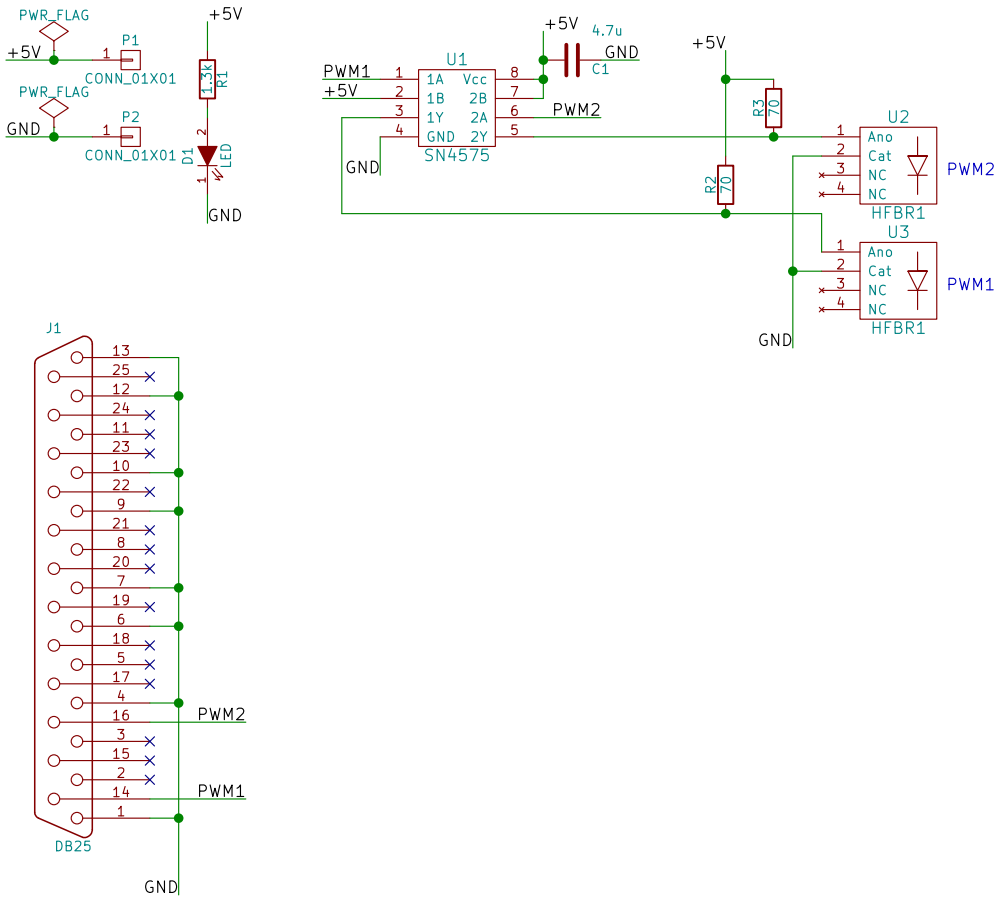


PED4−1045

Sheet: /
File: modular_ND.sch

Title: Non−driven module

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 4.0.1−stable		Id: 1/1



PED4-1045		
Sheet: /		
File: modular_meas.sch		
Title: Driver module		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 4.0.1-stable		Id: 1/1

Appendix E

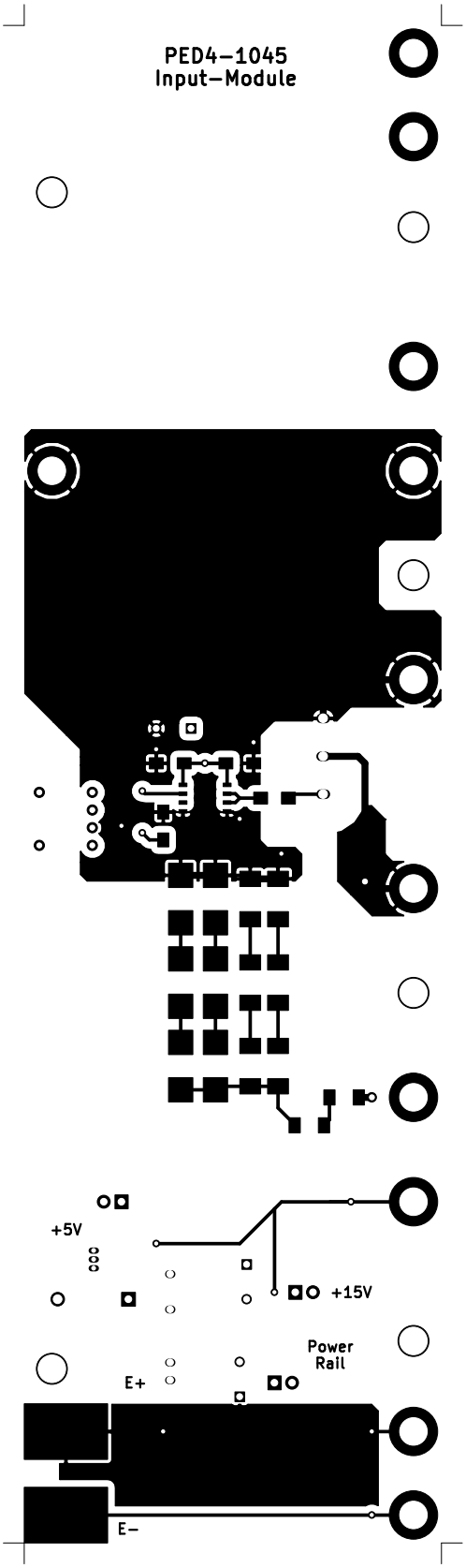
PCB Layouts

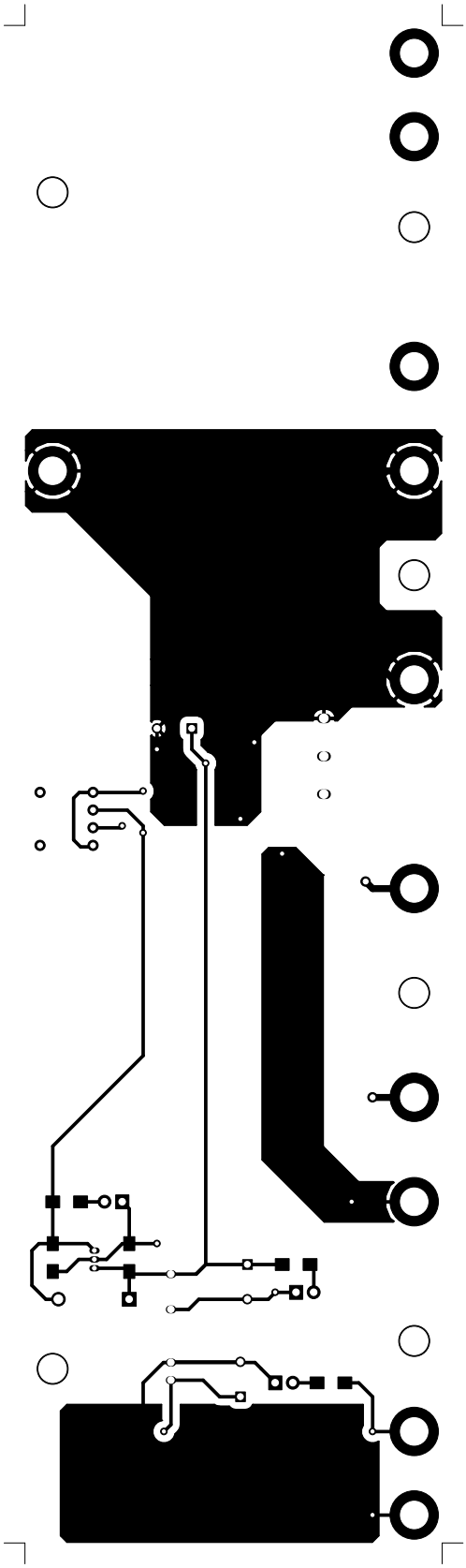
The layouts of the input module, output module, non-driven module and driver module are included in this appendix. The top and bottom PCB layers are separated to give a more clear view of the layout. The layouts are also available on the attached CD [1]

[1] /KiCAD/

Top Layer

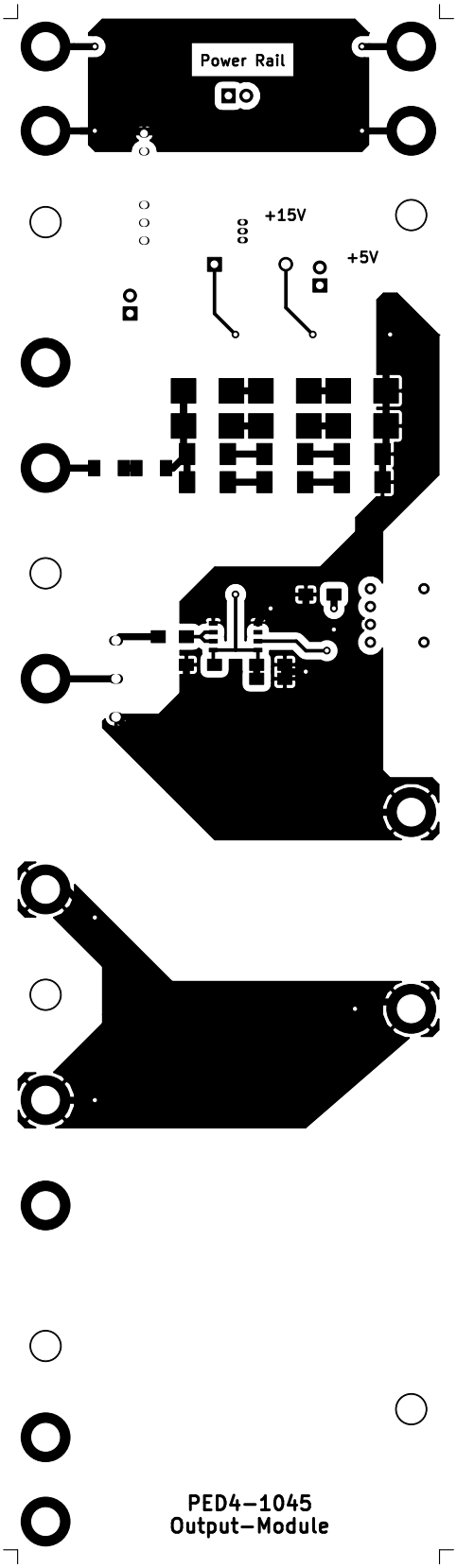
Bottom Layer



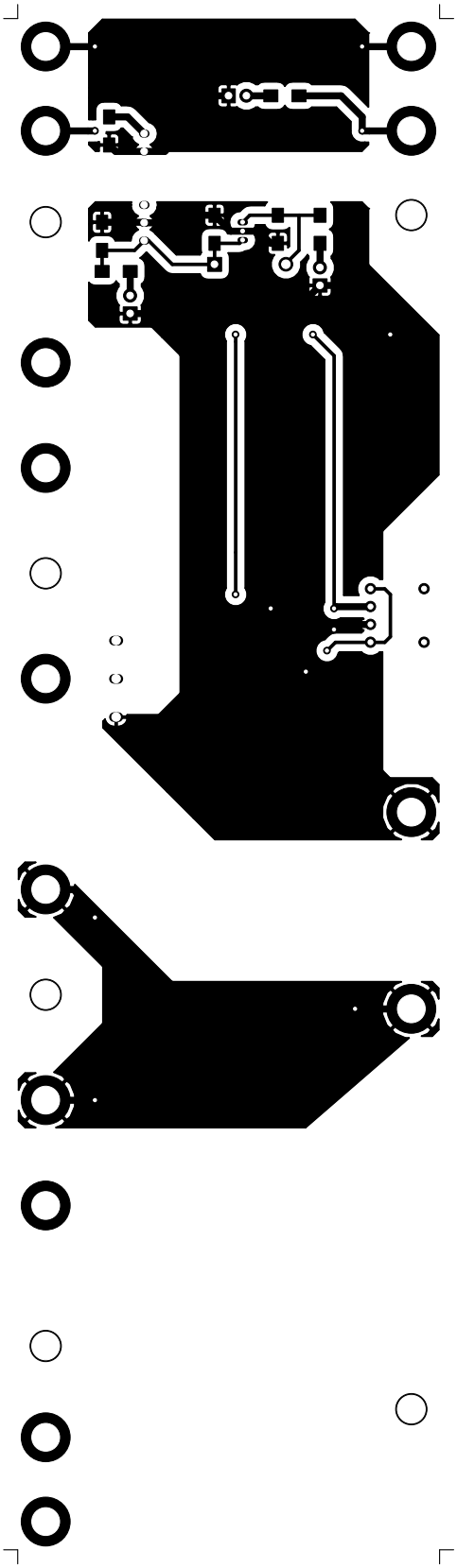


PED4-1045		
Sheet: File: modular_start.kicad_pcb		
Title: Input Module		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 4.0.1-stable		Id: 1/1

Top Layer



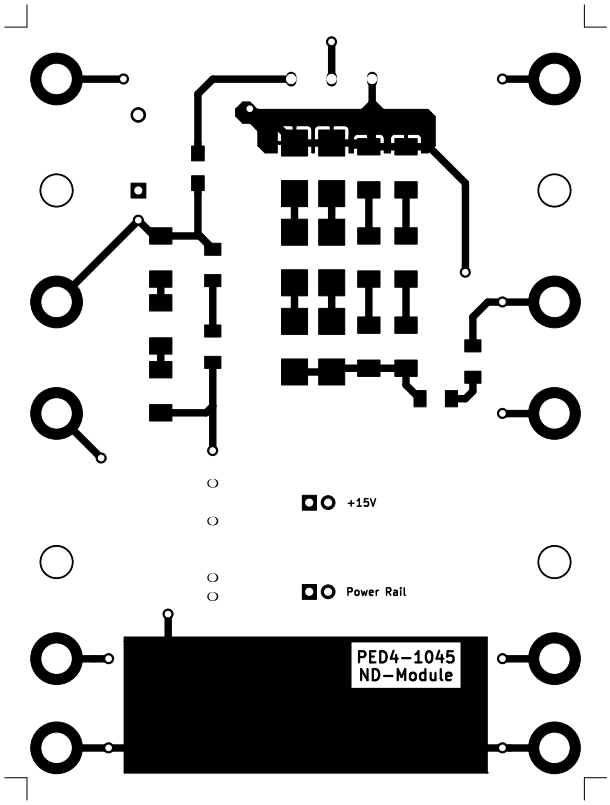
Bottom Layer



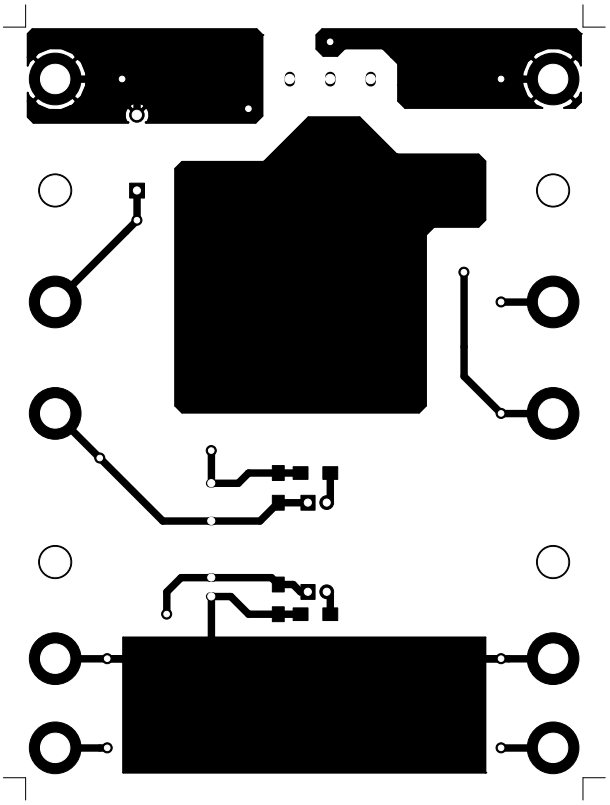
PED4-1045
Output-Module

PED4-1045		
Sheet: File: modular_stop.kicad_pcb		
Title: Output module		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 4.0.1-stable		Id: 1/1

Top Layer

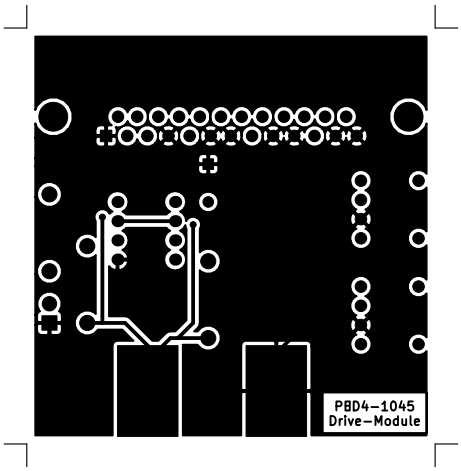


Bottom Layer

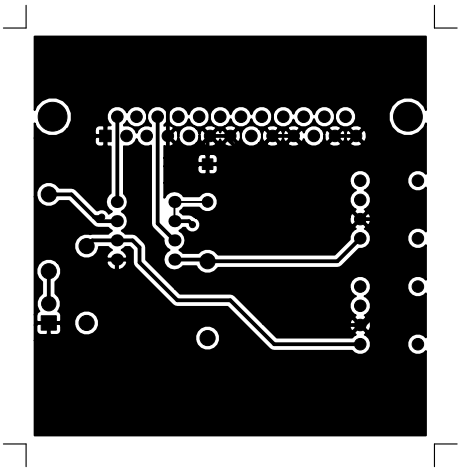


PED4-1045		
Sheet: File: modular_ND.kicad_pcb		
Title: Non-driven Module		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 4.0.1-stable		Id: 1/1

Top Layer



Bottom Layer



PBD4-1045		
Sheet: File: modular_meas.kicad_pcb		
Title: Driver module		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 4.0.1-stable		Id: 1/1

Appendix F

Poster

The following appendix includes a poster presented at the Intelligent and Efficient Power Electronics (IEPE) workshop held 1st-2nd June 2016 at University of Southern Denmark. A digital version of the poster is attached on the CD [1].

[1] `poster.pdf`

www.iepe.et.aau.dk

Serialization of SiC MOSFETs for a medium voltage converter

Asger Bjørn Jørgensen, Simon Dyhr Sønderskov

Supervisors: [1]Szymon Bęczkowski, [2]Benoit Bidoggia

[1]Aalborg University, [2]FLSmidth Airtech

University of Southern Denmark
IEPE Workshop: June 1-2, 2016

Abstract

The emergence of Silicon Carbide (SiC) offers potential benefits in medium voltage power supply design. This requires voltage balancing of series connected SiC MOSFETs, for which only limited research currently exists. Many serialization techniques turn on/off all switches simultaneously. For the fast switching and high blocking voltages of SiC devices, such solutions tend to cause high amounts of overshoot, ringing and difficulty in voltage balancing. In [1] a circuit is proposed, which features a cascaded switching sequence. Compared with the paper, the number of devices connected in series is extended and its capability to balance voltages across all switches is improved.

Serialization technique

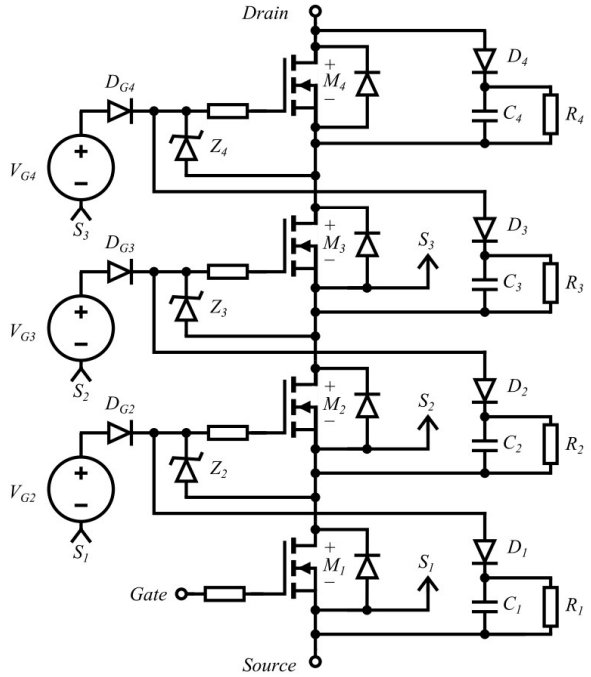


Figure 1: Serialization technique using cascaded turn on/off

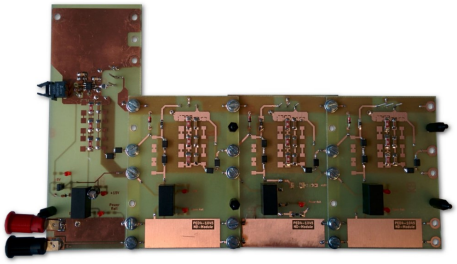


Figure 2: A modular layout enables fast development and replacement

Double pulse test results

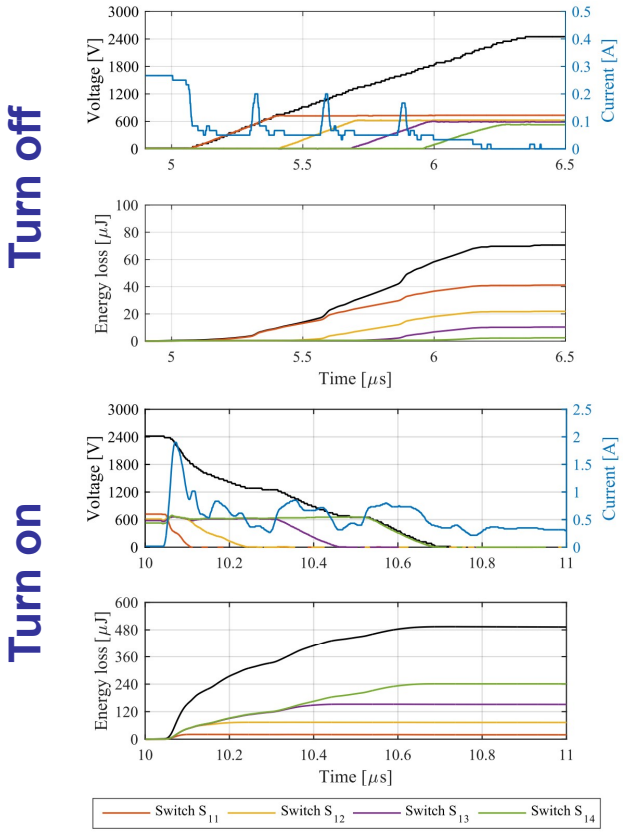


Figure 3: Double pulse test results

- No overshoot or ringing of drain-source voltages
- Good balancing between all four tested SiC MOSFETs
  - Maximum voltage M_1: 730 V (30 % of full voltage)
  - Minimum voltage M_4: 533 V (22 % of full voltage)
- Constant dv/dt similar to the value of a single device
- Comes at the cost of increased switching time

Future work

- Improve voltage balancing during 50 kHz hard switched operation.

- Extend the concept by series-connecting several SiC '*modules*' of the form shown in Figure 1
  - Each *module* consists of three/four SiC MOSFETs
  - Behaves as a single switch with constant dv/dt
  - Requires only a single gate signal per module

References

[1] Xinke Wu, Shidong Cheng, Qiang Xiao and Kuang Sheng. "*A 3600 V/80 A Series–Parallel-Connected Silicon Carbide MOSFETs Module With a Single External Gate Driver*". Power Electronics, IEEE, Transactions on, 29(5), 2296–2306, 2014. ISSN 0885-8993

DEPARTMENT OF ENERGY TECHNOLOGY
AALBORG UNIVERSITY
FLSmidth AIRTECH

Appendix G

CD Attachment

If this space is blank, you are likely to be reading a digital version of the thesis

A zip-file should be attached, including the same material as available on the CD-ROM