Control of Modular Multilevel Converter(MMC) based HVDC application under unbalanced conditions

.

Master Thesis

PED4-940

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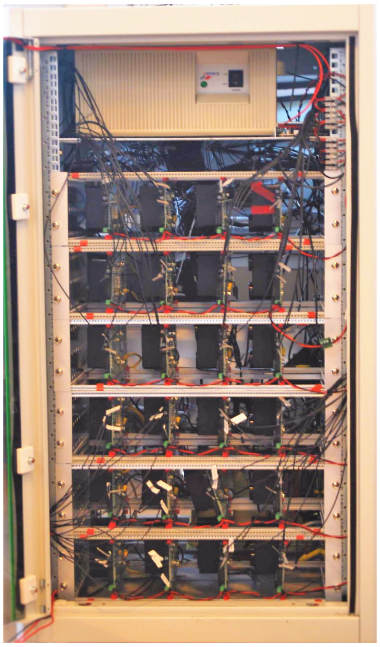

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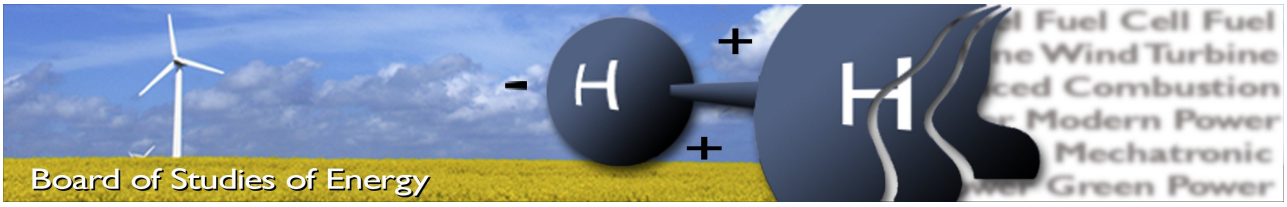

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SYNOPSIS:

MMC is an emerging topology which is able to handle high voltage and power ratings. Such converters are necessary for VSC-HVDC transmission system as it provides several advantages. Being a complex topology, several challenges are needed to be investigated. The purpose of this thesis is to analyze one of those challenges: unbalance conditions in the system which are created internally and during asymmetrical grid faults. Sorting and selection methods with variants: NLC, CTB and RSS has been explained and implemented. Unequal energy storage in the arms and phases of the converter is found to be an important consequence of unbalances in the system. Energy controllers are proposed in order to eliminate the unequal energy distribution among the converter. Since HVDC is required to remain connected during grid fault, an output current injection strategy under fault conditions is presented and simulated with the aim of complying with the grid codes. A systematic approach has been introduced for the effective reduction of the sum capacitor voltage ripple in an MMC application. Finally, a small prototype has been built and experimental results are presented.

Copies:	3
Pages, total:	120
Appendix:	25

By signing this document, each member of the group confirms that all participated in the project work and thereby all members are collectively liable for the content of the report.

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Preface

Control of Modular Multilevel Converter based HVDC application under unbalanced conditions was written as a part of Master thesis conducted at Aalborg University at the department of Energy Technology by group PED4-940 during the period from 1st of September 2015 till 24th of May 2016.

The report has been written in Latex and the simulations are performed in PLECS. The references can be found in the Bibliography and are cited according to the IEEE citation style. The format for the equations, figures and tables is $(A.B)$, where A represents the chapter number and B, its position in the chapter.

Acknowledgements

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Nomenclature

Subscripts, Superscripts and Prefixes

$*$	Reference
u, l	upper, lower arm
i	Submodule index
Σ	Sum
$\triangle$	Difference, imbalance, ripple quantity
$\hat{}$	Peak value
max	Maximum value
min	Minimum value
$+$	Positive sequence
$-$	Negative sequence
0	Zero sequence, dc component
$q = e^{-j\frac{\pi}{2}}$	90° phase shifting operator
$\perp$	Orthogonal component
$s = \frac{\mathrm{d}}{\mathrm{d}t}$	Differential operator
α, β	components of stationary alpha-beta reference frame
d, q	components of rotating DQ reference frame

Control parameters

α_b	PLL LPF bandwidth
α_p	PLL bandwidth
α_{ip}	PLL integrator bandwidth
α_d	DC bus voltage control-loop bandwidth
α_{id}	DC bus voltage integrator bandwidth
α_p	PLL bandwidth
$k_{sogi-pll}$	Input SOGI gain
α_c	Output- current control bandwidth
α_h	Resonant part bandwidth
α_{c0}	Desired bandwidth of the pure integrator
α_{c2}	Desired bandwidth of the resonant integrator
Kp_c	Proportional gain PR controller for i_s
Kh_{c2}	Integral gain of PR for i_s control
α_f	Voltage feed-forward filter bandwidth
R_a	Proportional gain of i_c control
α_2	Circulating current control bandwidth
$K2h_c$	Integral gain for resonant controller for i_c
α_{cr}	Bandwidth of LPF of i_c to get the dc value
G_c	Closed loop system
G_k	Open loop system
t_r	Time constant

List of symbols

M	Number of phases
m	Phase index for phases a,b,c
L	Arm Inductance
R	Parasitic arm resistance
C	Submodule Capacitance
N	Number of submodules per arm
v_d	DC-bus voltage
$v_{du,l}$	Pole-to-ground DC voltage
i_{dc}	DC-bus current
$s = \frac{\mathrm{d}}{\mathrm{d}t}$	Differential operator
$i_{u,l}$	Arm currents
i_s	Output current
i_c	Circulating current
v_s	Output voltage (driving i_s)
v_c	Internal voltage (driving i_c)
$v_{cu,l}^{\Sigma}$	Sum capacitor arm voltages
$n_{u,l}$	Insertion index per arm
v_a	AC-bus voltage
$\hat{V}_s$	Peak value, fundamental component of v_s
$\hat{I}_s$	Peak value, fundamental component of i_s
$W_{\Sigma} = W_u + W_l$	Stored energy per phase
$W_{\triangle} = W_u - W_l$	Imbalance stored energy
f	Fundamental frequency
ω	Fundamental angular frequency
ϕ_i	Load angle
I_{c0}	DC component of i_c
i_{c1m}	Fundamental frequency component of i_c
i_{c2m}	Second harmonic component of i_c
$\Delta v_{c_{u,l}}^{\Sigma}$	Arm voltage ripple
e	Error
$e^{'}$	Modified error
C_d	DC-bus capacitance
P	Active output power
$q = e^{-j\frac{\pi}{2}}$	90° phase shifting operator
k	Droop factor
i_d	Active current
i_q	Reactive current
ϵ_1	Maximum current ripple
ϵ	Maximum voltage ripple
$\pm\delta$	Voltage tolerance band(CTB)
$cos\phi$	Power factor
$m = \frac{\hat{V}_s}{\frac{v_d}{2}}$	Modulation index
f_s	Sampling frequency
T_m	Modulation period

Abbreviations

AAU	**A**alborg **U**niversity
HVDC	**H**igh **V**oltage **D**irect **C**urrent
HVAC	**H**igh **V**oltage **A**lternating **C**urrent
VSC	**V**oltage **S**ource **C**onverters
MMC	**M**odular **M**ultilevel **C**onverters
AC	**A**lternating **C**urrent
DC	**D**irect **C**urrent
ABB	**A**sea **B**rown **B**overi
SM	**S**ub **M**odules
RMS	**R**oot **M**ean **S**quare
KVL	**K**irchhoff's **V**oltage **L**aw
PI	**P**roportional **I**ntegral
PR	**P**roportional **R**esonant
DSP	**D**igital **S**ignal **P**rocessors
FPGA	**F**ield **P**rogrammable **G**ate **A**rrays
PWM	**P**ulse **W**idth **M**odulation
SCR	**S**hort **C**ircuit **R**atio
NLC	**N**earest **L**evel **C**ontrol
CTB	**C**apacitor **T**olerance **B**and
RSS	**R**educed **S**orting **S**witching
DSOGI	**D**ouble **S**econd **O**rder **G**eneralised **I**ntegrator
PNSE	**P**ositive **N**egative **S**equence **E**xtraction
PLL	**P**hase **L**ocked **L**oop
QSG	**Q**uadrature **S**ignal **G**eneration
PCC	**P**oint **C**ommon **C**oupling
LVRT	**L**ow **V**oltage **R**ide **T**hrough
FPNSC	**F**lexible**P**ositive **N**egative **S**equence **C**ontrol
PSI	**P**ositive **S**equence **I**njection
MSI	**M**ixed **S**equence **I**njection
SLG	**S**ingle **L**ine **G**round
IPM	**I**ntelligent **P**ower **M**odules
LPF	**L**ow **P**ass **F**ilter
CPLD	**C**omplex **P**rogrammable **L**ogic **D**evice

Chapter 1

Introduction

1.1 High Voltage Direct Current(HVDC)

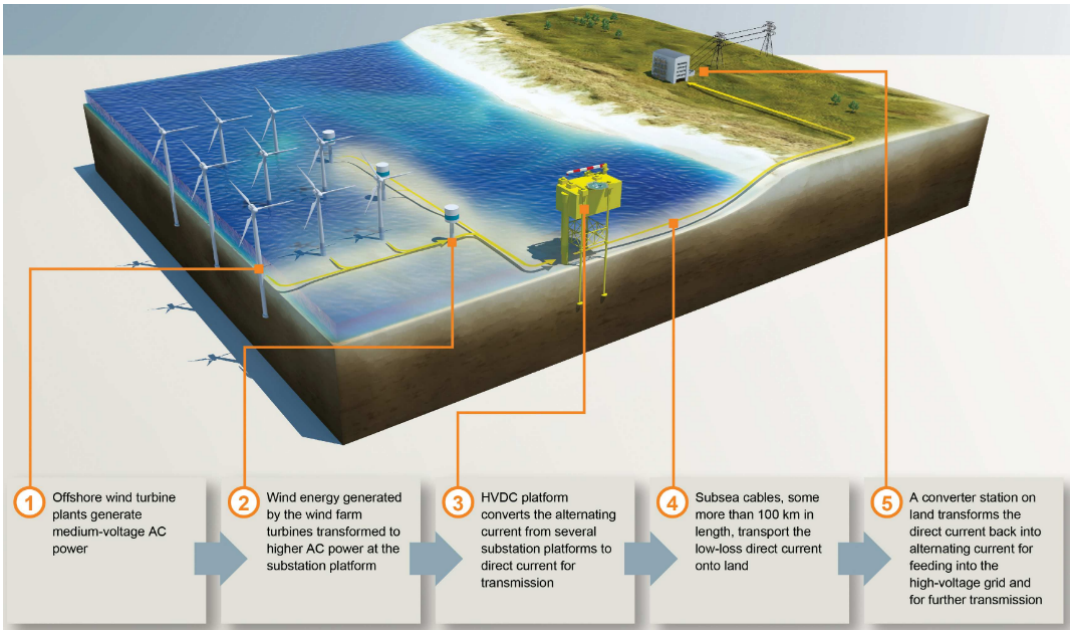

Figure 1.1: HVDC transmission system from an offshore to onshore grid [1].

AC has been the preferred global platform for electrical transmission to homes and businesses for the past 100 years. And yet high-voltage AC transmission has some limitations, starting with transmission capacity and distance constraints, and the impossibility of directly connecting two AC power networks of different frequencies. With the dawn of a new energy era and the need to build a smarter grid, HVDC is expected to grow far beyond its traditional position as a supplement to AC transmission [2].

High Voltage Direct Current (HVDC) is the electric power transmission choice

utilized in large amount of power over long distances with minimal losses. Considering the fact that in a conventional three phase system the power delivered is conformed by its RMS value, HVDC allows transmitting active power with higher voltage range. Moreover, the impedance created in AC transmission systems are avoidable decreasing the power losses. Therefore, the initial installation cost of HVDC is higher than HVAC systems but due to lower losses it becomes cost effective over the time. For example, power delivered from remote offshore wind farms can be efficiently fed into power grids onshore via HVDC technology. Moreover, HVDC systems are useful to interconnect asynchronous AC grids reliably. Using HVDC system allows the possibility of using underground and susea cables. Hence, HVDC is considered as a highly efficient alternative for transmitting large amounts of electricity over long distances and for special purpose applications. As a key enabler in the future energy system based on renewables, HVDC is truly shaping the grid of the future.

This technology consists of a converter station in which the AC system is converted into DC then transmitted through a power transmission cable and then converted back into AC. The cable connection can be overhead or both underground or submarine under water. An HVDC transmission system is depicted in Figure 1.1.

1.2 MMC-HVDC

Modular Multilevel Converters (MMCs) have gained researcher's attention due to their ability to handle high voltage and power ratings. VSC-HVDC is getting increasingly important for integrating renewable energy sources such as large offshore wind farms, providing flexible interconnection between two weak AC grid network using back-to-back configuration, or simply transmitting power using underground cables. The VSC-HVDC also has fast and precise control over the active power-flow as well as it can independently control the reactive power injection at the local ac grid. There are numerous operational MMC-HVDC projects such as HVDC PLUS (Siemens) with an 88 km undersea transmission link between San Francisco's City Centre electrical power grid and a substation near Pittsburg. The main supporting functions HVDC PLUS provides are AC voltage Control, black-start capability, compact converter station space usage, four quadrant operation, compensation of asymmetrical loads, flexible integration into HVDC multi terminal systems or future HVDC grids. Its basic operating principle and other advantages both on the technical as well as on the economical aspect can be described in [3] [4].

Another MMC-HVDC installation named HVDC Light by ABB, is an adaptation of HVDC classic used to transmit electricity in power ranges (50-2500MW) transmitted using overhead lines and enviornmental friendly underground and sub-sea cables. It is used for grid interconnections and offshore links to wind farms. With HVDC Light, it is possible to transmit power in both directions and to support existing AC grids in order to increase robustness, stability, reliability and controllability. HVDC Light offers many other advantages and can be used in different applications which is explained in [5]. As outlined before, the main limitation of the two level converter

is its high switching losses due to relatively high switching frequency which necessitates high insulation requirements of the transformer, as well as filters. The use of modular multilevel converters overcomes many of the aforementioned shortcomings, but at the expense of twice as many semi-conducting devices and a large distributed capacitor for each submodule. The principle idea of the hybrid VSC-HVDC, as used in HVDC MaxSine developed by Alstom, is to use a two level converter as the main switching component with low switching frequency and an MMC to provide a voltage wave shaping function on the AC side in order to eliminate the harmonics [6] [7]. Information about recent and upcoming MMC-HVDC installation plants can be found below in Table 1.1 [3], [4], [5], [8].

Finally, MMCs provides several advantages in comparison to the conventional converter systems featuring:

- Modular design.
- High efficiency.
- Reduced($\frac{\mathrm{d}i}{\mathrm{d}t}$) of the arm currents.
- Low harmonic distortion at the output side and low high-frequency noise.

Project	Year	Power (MW)	AC (kV)	DC (kV)	Main reason for choosing HVDC	Application
East West Interconnector	2013	500	400	± 200	Length of sea and land cables, controllability, black start and P-Q support	Interconnecting grids
Skagerrak Pole 4	2014	700	400	± 500 (HVDC Light)	Length of sea crossing, asynchronous link. For pole 4, HVDC Light was chosen for its premier power quality features.	Interconnecting grids
Kraftnät Åland AB	2015	100	110	± 80	Length of sea crossing, Asynchronous networks, reliable backup power	Interconnecting grids
DolWin1	2015	800	380(Dörpen/West) 155 (Platform DolWin Alpha)	± 320	Length of land and sea cables	Offshore wind connections
Valhall	2011	78	300 (Lista), 11 (Valhall)	150	Reduce costs and improve efficiency. Minimize emissions.	Power from shore
NordLink	2020	1400	400 (Tonstad, Norway 380 (Wilster, Germany)	± 525	Long submarine cable distance, stabilizing features	Interconnecting grids
Kriegers Flak Combined Grid Solutions	2019	410	Germany side:400 Offshore side:150	± 140	Interconnecting asynchronous grids	Interconnecting grids
North Sea Link	2021	1400	420 (Kvilldal, Norway) 400 (Blyth, UK)	± 525	Long submarine cable distance, stabilizing features.	Interconnecting grids
Caithness Moray HVDC Link	2018	1200	Spittal side:275 Blackhillock side: 400	±320	Length of subsea cable, reinforcing AC network, connecting renewables	Interconnecting grids
Maritime Link	2017	500	Newfoundland side:230 kV Nova Scotia side:345 kV	±200	Long distance, stabilizing features	Connecting remote generation and interconnecting grids
Mackinac	2014	200	Both sides: 138 kV	±71	islanded operation, under certain operating conditions, voltage stability and power flow control	DC links in AC grids
NordBalt	2015	700	Swedish side:400 Lithuanian side:330	±300	Length of sea crossing Asynchronous networks	Interconnecting grids
BorWin2	2015	800	380 (onshore side); 155 (offshore side)	± 300 (HVDCPLUS)	Length of land and sea cables	Offshore wind connections
HelWin1	2015	576	380 (onshore side); 155 (offshore side)	±250 (HVDCPLUS)	Length of land and sea cables	Offshore wind connections
SylWin1	2015	864	380 (onshore side); 155 (offshore side)	±320 (HVDCPLUS)	Length of land and sea cables	Offshore wind connections
South West Link	2014	1440	300 between two sites	±300	Black start, Reduce costs and improve efficiency	Balancing the power supply between central and southern Sweden.
ULTRANET	2019	2000	400	±380 (HVDCPLUS)	Black start, integrated DC lines at exisiting pylons, stabilizing functions.	Interconnecting grids
INELFE	2015	2000	400	±320 (HVDCPLUS)	Black start	Interconnecting grids
COBRAcable	2019	700	400	±320	improve cohesion in the European transmission grid by increasing the exchange of surplus wind power with neighbouring countries and strengthen the infrastructure, security of supply and the market.	Interconnecting grids
DolWin 2	2016	916	155 (Platform DolWin beta),380 (Dörpen West)	$pm320$	Length of land and sea cables	Offshore wind connections

Table 1.1: List of installed and planned MMC-HVDC projects

1.3 State of Art and Motivation

The origins of the MMC circuits synthesizing waveform converter topologies and their design and control were patented in 2002 by Marquardt and Lesnicar in [9]. An intense research has been done on all aspects of the system after this innovative finding. During steady state operation, a circulating current is observed flowing through the converter phase-leg [10]. The voltage ripples in the capacitors are studied as a cause for this circulating current component. Later in [11], the circulating current is analyzed and found to have double line-frequency and negative sequence. Having a large number of sub-modules increases the complexity of the control of the MMC. To assure accurate and stable operation, the sub-modules must share the voltage equally. Different control strategies have been proposed aiming to regulate the equal share of charge within the capacitors in the arm. Akagi et al. proposed in [12], a voltage balancing algorithm for the capacitors per phase. The control is performed by adding a balancing component to the modulation index of each sub-module.

Another method to eliminate the circulating current and balance the converter arm voltages is proposed in [13]. The method is based on the control of the stored energy in the converter, and several control loops are added to ensure stable operation. A simplification of this method using open-loop approach for the estimation of the arm energy is proposed in [14], proving to have a better stability. Later in [15] a combination of the energy approach, showing an improved performance for grid connected applications.The MMC topology has the possibility of synthesizing high voltage levels by increasing the number of series connected sub-modules, therefore is especially suitable for HVDC systems. In [16] alternative carrier-less modulation methods compared to conventional modulation carrier based techniques have been discussed to discard the option of adding a extra voltage balancing controller and to reduce the switching losses in MMC and to ensure optimum performance with large number of submodules.

Lately, a lot of research is focused on evaluation of MMC performance in HVDC applications under different grid conditions. In [17] the converter operation under unbalanced grid conditions has been analyzed, using a $\Delta - Y$ transformer to remove the zero sequence current from the converter terminals. The presence of DC-link voltage ripple due to negative sequence components is described and a controller to compensate for the disturbance is proposed. An additional zero sequence current control is proposed for transformerless connections under unbalanced conditions, proving stable HVDC system operation and enhanced fault ride-through capability of the converter [18].

Technical literature and the growing amount of installations show the success and market acceptance of the MMC topology. However, there are very little publications discussing the control of MMC under internal unbalance and its effect on inner dynamics. Motivated by the fast penetration of MMC into the HVDC market and the lack of research published on this topic, the analysis is focused on the need of energy balancing controllers for arm and legs of MMC to ensure stable operation dur-

ing internal imbalances. An mathematical approach has also been described which involves second harmonic injection in the circulating current to reduce the voltage ripple and the size of the capacitors.

1.4 Project Objective

The main goals for this thesis are listed below:

- In-depth understanding of the mathematical modeling, operating principles and internal control of MMC.
- Modeling of MMC-HVDC system, design and implementation of energy balancing control along with circulating current control strategy.
- Analysis of system behavior as response to internal unbalanced conditions.
- Theoretical and analytical approach of the output current controller and the preferred injection strategy during grid faults.
- Second harmonic injection in the circulating current to reduce the voltage ripple and the size of the capacitors.
- Construction of an experimental prototype to implement the developed energy and output controllers for controlling the internal imbalance ensuring that the system remains balanced.

1.5 Project Limitations

Since the main focus of this thesis is to design and implement control for the MMC based HVDC application under unbalanced conditions and a novel start-up procedure, some limitation has been established. The main limitations of this project are:

- No communication and control delays were implemented in the simulations since, average modeling of MMC is considered as a base for the controller design.
- Due to available resources and complexity, a laboratory prototype is built which is a three phase five level MMC(4 SM per arm) with the DC link voltage of 400V.
- No laboratory validation of the energy balancing controllers were implemented due to protection issues in the hardware and security of the converter.
- No focus will be placed on the converter output quality in terms of harmonics and efficiency as the number of submodules are few and the built prototype is operated at low power.

- Only the inverter functionality mode is considered.

1.6 Thesis outline

Based on the knowledge obtained from the studied philosophy and previous subsections describing the introduction and motivation, a working model was built during the thesis tenure. This built model showcases the control for the internal unbalance created in each arm and phase of an MMC and investigation of the effects of grid faults were also carried out.

Chapter 2 explains the average modeling of MMC to understand better its governing equations. After the basics of MMC, the design of internal circulating current control and output-current control has been analyzed. The obtained theoretical results of the design of controllers will be validated through simulations and experimental results. Finally, the different modulation techniques used for hardware implementation will be explained in brief.

Chapter 3 investigates the internal unbalances which are created in the arms and phases of MMC and the ability of the arm balancing and leg energy control to keep the system balanced during internal parameter mismatches. A theoretical analysis of the system unbalance is studied during grid faults and a proposed reference injection strategy is explained for the output current controller design. Finally, a second harmonic injection strategy in the circulating current is proposed for reducing the capacitor voltage ripple and minimizing the energy variation in the leg thereby allowing for a capacitor size reduction.

Chapter 4 and 5 describes the hardware setup design and the component selection criteria for building an MMC prototype for performing experimental results and their validation with the theoretical analysis and the simulation results obtained during this thesis.

Lastly, the thesis concludes with the key findings from this study and summary of the obtained simulation and experimental results along with plans for future work in Chapter 6.

Chapter 2

Dynamics and Control of MMC

In this chapter, fundamentals of MMC dynamics and its control is studied in detail. To ensure proper implementation of all the control system, it is of utmost importance to study the complexity of the internal dynamics and behavior of MMC.

2.1 Component Description and basics of MMC

A single-phase schematic of MMC is displayed in Figure 2.2. The fundamental theory for MMC is general and is applicable for any number of phases, with a three phase converter modeling being the primary interest for this thesis. It consists of several sub-modules (SM) that can be referred as cells, connected in series. The sub-module topology used in this thesis is based on Half-bridges which contains a DC energy storage capacitor (C_{sm}), two controlled semiconductor devices and two anti-parallel diodes. As it can be derived from the sub-module topology, the switches have to operate complementary in order to not short circuit the capacitor. There are two arms per phase forming the leg of the converter, which are referred as the upper and lower arms. The upper arms of the (M) phases are connected to the positive pole and similarly the lower arms are connected to the negative pole of the DC-bus. A transformer with galvanic isolation is generally used between the converter and the AC side. The purpose of this transformer is to step up or step down the grid voltage according to the converter voltage ratings and to trap the zero sequence current. The arm inductors (L) installed on each arm functions as a filter to attenuate the high frequency harmonics in the arm currents and to limit the rate of current rise during faults. Finally, a resistor in parallel with an AC breaker is used to prevent the overvoltages at the converter side when energy transfer takes place from the grid side by closing the AC breaker. It is important to understand the mathematical relations between the voltage and current equations governing the dynamic relations of an MMC.

Analyzing Figure 2.2, the symmetric configuration yields:

$$v_{du} = v_{dl} = \frac{v_d}{2} \tag{2.1}$$

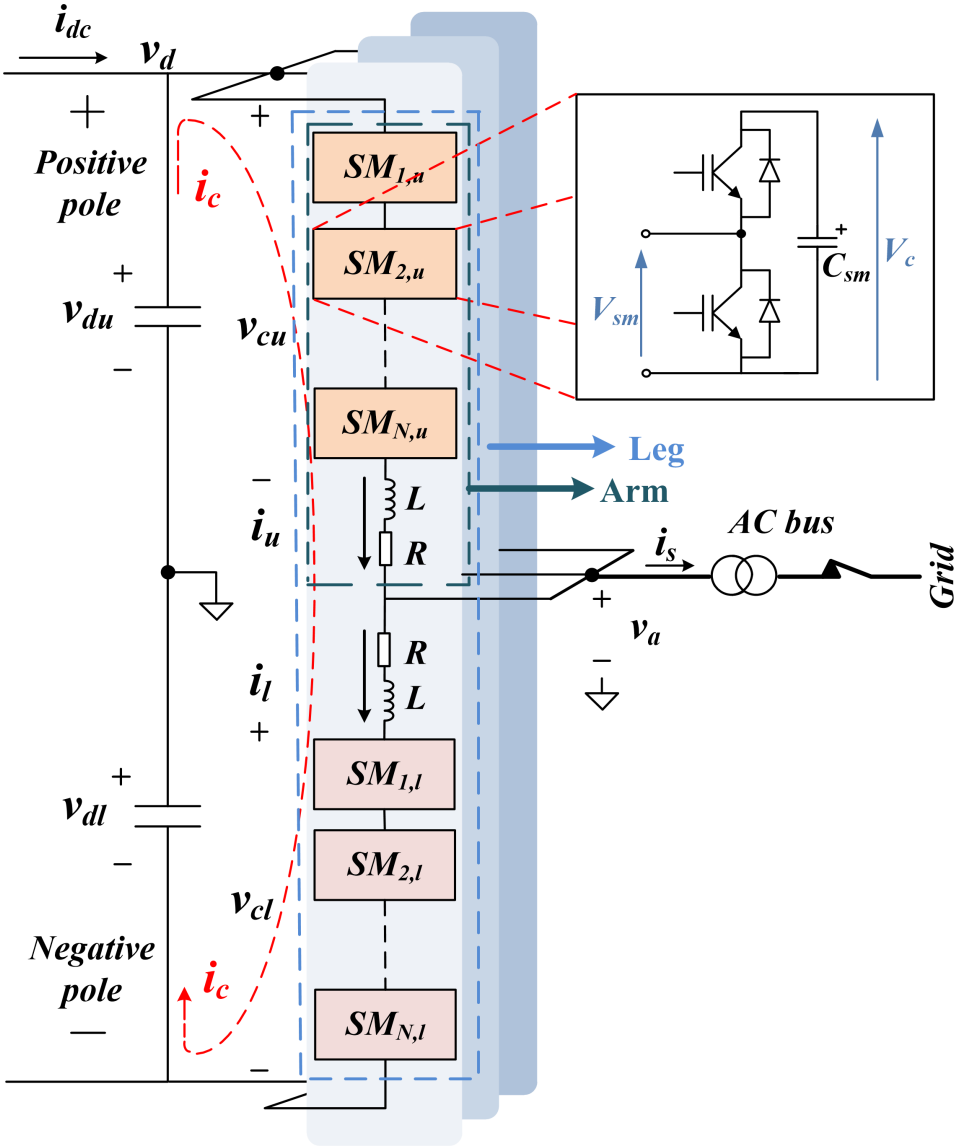

Figure 2.1: Three phase schematic of MMC

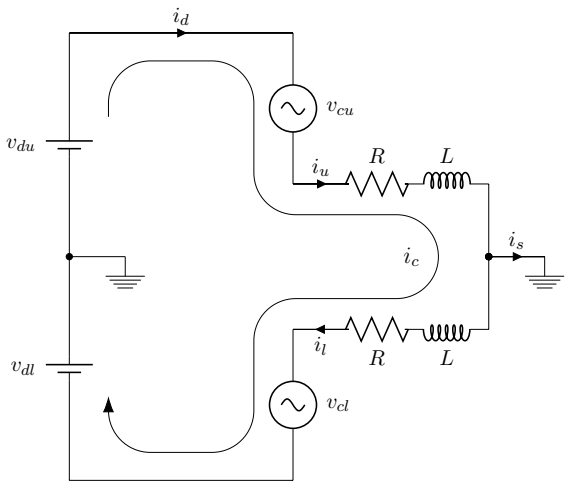

Figure 2.2: Average model of MMC.

and as shown in Figure 2.2 the output and circulating current are defined as:

$$i_s = i_u - i_l \qquad \text{and} \qquad i_c = \frac{i_u + i_l}{2} \tag{2.2}$$

By manipulating the above two equations, a relation between the arm currents with the output and circulating current can be deduced as:

$$i_u = \frac{i_s}{2} + i_c \qquad \text{and} \qquad i_l = -\frac{i_s}{2} + i_c \tag{2.3}$$

In order to obtain a constant DC-bus voltage and to keep the converter losses and RMS value of the arm currents low, the circulating current should only contain a DC component inferring to:

$$\overline{i_u} = \overline{i_l} = \overline{i_c} = \frac{i_{dc}}{M} \tag{2.4}$$

By analyzing the mathematical model and applying KVL to each arm of three phases of MMC, the AC side voltage equation yields to:

$$v_a = \frac{v_d}{2} - v_{cu} - Ri_u - L\frac{di_u}{dt} \tag{2.5}$$

$$v_a = -\frac{v_d}{2} + v_{cl} + Ri_l + L\frac{di_l}{dt} \tag{2.6}$$

By adding Equation 2.5 and Equation 2.6, the output voltage driving the output current (i_s) can be defined as:

$$v_s = \frac{v_{cl} - v_{cu}}{2} \tag{2.7}$$

Similarly, by subtraction of Equation 2.5 and Equation 2.6, the voltage which drives the DC circulating current i_c can be expressed as:

$$v_c = \frac{v_d - v_{cl} - v_{cu}}{2} \tag{2.8}$$

From the above derived equations and depending upon the output requirements the maximum and the minimum output voltage can be achieved by proper insertion-bypassing of the capacitors in the submodules of the legs of the three phases of MMC. Maximum output voltage can be obtained by inserting all the submodules in the lower arm and bypassing all the upper submodules. Similarly, minimum output voltage can be obtained by reversing the aforementioned task [13]. Mathematical equation validating this, can be given by:

$$v_{cu} = 0, v_{cl} = v_{cl}^{\Sigma}, \quad v_s^{max} = \frac{v_{cl}^{\Sigma}}{2} \tag{2.9}$$

$$v_{cl} = 0, v_{cu} = v_{cu}^{\Sigma}, \quad v_s^{min} = -\frac{v_{cu}^{\Sigma}}{2} \tag{2.10}$$

2.2 Average modeling of MMC

Average modeling of MMC aims to realize fast, stable, and reliable MMC simulation with proper accuracy. It can reduce the computation load of simulation platforms. Average modeling is carried out to make the system dynamics and design of the controllers as simple as possible by linearizing the system variables. Designing of a controller is a phenomena where your system output is made to track a reference signal which is constant and the error is sampled with the period and fed back to the controllers often without system delays. The function of this controller is then to adjust the input according to the plant requirement during sampling time where the signal input remains constant in between the sampling period. After understanding the mathematical equations and relations of different currents and voltages in the previous section, this subsection would be considered as the base on which different control strategies would be implemented. It is very important to have correct reference voltage values in order to control the converter.

Ideally, the sum capacitor voltages per arm should be equal to the pole to pole DC-bus voltage and assuming the voltage driving the circulating current to be constant (v_c), by neglecting the parasitics, the sum capacitor voltages should be chosen as:

$$v_{cu,l}^{\Sigma} = v_d \tag{2.11}$$

Thus from Equation 2.11, if the sum capacitor voltages per arm for all the phases of MMC are constant without any ripple i.e. absence of oscillating component, then from Equation 2.7 the maximum and minimum output voltage can be expressed as:

$$v_s^{max} = v_s^{min} = \pm\frac{v_d}{2} \tag{2.12}$$

By noting the inserted arm voltages with:

$$v_{cu,l} = \sum_{i=1}^{N} n_{u,l}^{i} \cdot v_{u,l}^{i} \tag{2.13}$$

where, $n_{u,l}^{i}$ are the submodule insertion indices of the upper and lower arm of three phases of MMC. The main advantage of this averaging model is that it allows to neglect the voltage variation in individual submodule capacitors. Since, it is difficult to measure the voltages in each capacitor of the submodule and due to mathematical computation complexity, a new term called insertion indexes $n_{u,l}$ is introduced which can be used for future theoretical analysis. The voltages in the submodules can be kept to a constant mean value by controlling the insertion indices, and thereby controlling the converter. The submodule insertion indices indicates how many submodules are inserted according to the system requirement, where $n_{u,l} = 0$ indicates that the submodules are bypassed whereas, $n_{u,l} = 1$ indicates the insertion mode.

The average value of the submodule insertion indices can be expressed as:

$$n_{u,l} = \frac{1}{N} \sum_{i=1}^{N} n_{u,l}^{i} \tag{2.14}$$

Thus from the aforementioned details and from Equation 2.13 and Equation 2.14, the inserted arm voltage in terms of insertion index can be inferred as:

$$v_{cu,l} = n_{u,l} \cdot v_{cu,l}^{\Sigma} \tag{2.15}$$

The average dynamic model for the currents and voltages are governed from Equation 2.15, Equation 2.7 and Equation 2.8:

$$\frac{L}{2} \cdot \frac{\mathrm{d}i_s}{\mathrm{d}t} = v_s - v_a - \frac{R}{2} i_s \tag{2.16}$$

where,

$$v_s = \frac{-n_u v_{cu}^{\Sigma} + n_l v_{cl}^{\Sigma}}{2} \tag{2.17}$$

and

$$L \cdot \frac{\mathrm{d}i_c}{\mathrm{d}t} = v_c - R i_c \tag{2.18}$$

where,

$$v_c = \frac{v_d - n_u v_{cu}^{\Sigma} - n_l v_{cl}^{\Sigma}}{2} \tag{2.19}$$

Cell capacitor voltage equation can be expressed as:

$$n_{u,l} \cdot i_{u,l} = \frac{C}{N} \frac{\mathrm{d}v_{cu,l}^{\Sigma}}{\mathrm{d}t} \tag{2.20}$$

The above Equation 2.20 can be simplified in terms of the output and circulating currents resulting:

$$\frac{C}{N}\frac{\mathrm{d}v_{cu}^{\Sigma}}{\mathrm{d}t} = n_u\left(\frac{i_s}{2} + i_c\right) \quad \frac{C}{N}\frac{\mathrm{d}v_{cl}^{\Sigma}}{\mathrm{d}t} = n_l\left(-\frac{i_s}{2} + i_c\right) \tag{2.21}$$

Multiplying Equation 2.21 by v_{cu}^{Σ} and v_{cl}^{Σ} the deducted equations can be expressed as:

$$\frac{dW_{\Sigma}}{dt} = 2v_c i_c - v_s i_s \quad \frac{dW_{\triangle}}{dt} = v_c i_s - 2v_s i_c \tag{2.22}$$

Assuming the circulating current to be constant and considering v_s and i_s to be sinusoidal signals Equation 2.22 can be rewritten as:

$$\frac{dW_{\Sigma}}{dt} = v_d I_{c0} - \frac{\hat{V}_s\hat{I}_s}{2}\cos\phi_i - \frac{\hat{V}_s\hat{I}_s}{2}\cos(2\omega t - \phi_i) \tag{2.23}$$

$$\frac{dW_{\triangle}}{dt} = \frac{v_d\hat{I}_s}{2}\cos(\omega t - \phi_i) - 2\hat{V}_s i_c cos(\omega t) \tag{2.24}$$

Further integrating Equation 2.23 and Equation 2.24 and considering that under balanced conditions the input DC power equals the phase output AC power, the equations can be simplified as:

$$W_{\Sigma} = \frac{C{v_d}^2}{N} - \triangle W_{\Sigma} \tag{2.25}$$

$$W_{\triangle} = W_{\triangle 0} + \triangle W_{\triangle} \tag{2.26}$$

Thus, from above equations governing the dynamics of MMC and after mathematical manipulations, the sum and the difference of the capacitor voltages in a leg can be expressed as:

$$v_c^{\Sigma} = v_{cu}^{\Sigma} + v_{cl}^{\Sigma} = 2v_d + \frac{N}{Cv_d}\triangle W_{\Sigma} \tag{2.27}$$

$$v_c^{\triangle} = v_{cu}^{\Sigma} - v_{cl}^{\Sigma} = \frac{N}{Cv_d}\triangle W_{\triangle} \tag{2.28}$$

2.2.1 Selection of upper and lower arm Insertion Indices

This subsection focuses mainly on proper selection of the insertion indices to cover the system requirements as previously explained. During the work for the thesis, out of different voltage control methods, Direct Voltage Control has been implemented as it gives a inherently asymptotically stable system. Here, the reference is scaled by a constant value v_d in place of the sum capacitor voltages [19] eliminating the use of an extra controller for capacitor voltage ripple estimation.

In this method the equation for the upper and lower arm indices is given by:

$$n_u = \frac{\frac{v_d}{2} - v_s^* - v_c^*}{v_d} \quad n_l = \frac{\frac{v_d}{2} + v_s^* - v_c^*}{v_d} \tag{2.29}$$

A control schematic for the specific implemented method is as shown in Figure 2.3.

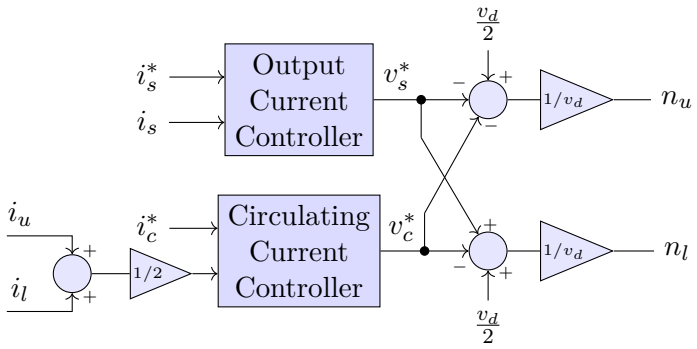

Figure 2.3: Block Diagram representation of Direct Voltage Control.

It can be seen that the reference value of the output voltage is obtained from the measured and reference values of the output current which is then fed to the output current controller. Similarly, the reference value of the voltage driven by the DC circulating current can be obtained from the measured and reference value of the DC circulating current. These output values combined with the dc link voltage are then mathematically manipulated to obtain the desired insertion indices n_u and n_l for the upper and lower arm of three phases of MMC.

2.3 Control of MMC

Previously, both the dynamics and an averaged model of the MMC were presented. Considering the mathematical models of the MMC, the implementation of the necessary controllers are explained below. The controller implementation strategy can be divided in two different but related blocks, called external and internal control. The first one determines the behavior of the converter based on the output current value depending on the load necessities, while the internal control cares about the particularities of the MMC as the circulating current and arm voltage balancing. The aforementioned controllers are necessary to ensure a good performance of the system allowing the converter to carry out its main functions. The controllers for the internal unbalance conditions in an MMC are presented in the next chapter.

In this chapter basics of control are first presented mainly focusing on the utilization of PR over PI controllers. The proposed method discussed and introduced here are only some of the several possible approaches of control analysis.

2.3.1 Limitations of PI controllers

The use of proportional-integral controllers is widely expanded in systems where constant signals are desired to be tracked. To define the functionality of a PI controller, current (i) flowing through an inductor to be controlled is taken as an example. For this purpose a closed-loop system with negligible inner resistance and control time

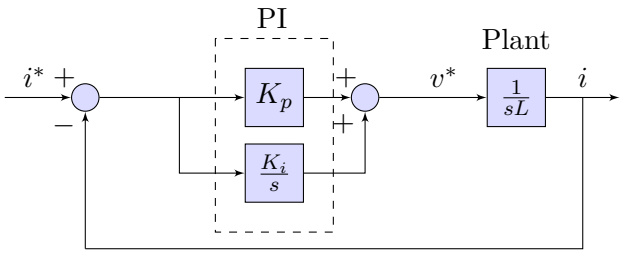

Figure 2.4: Control loop of the current through an inductor by using PI controller.

delay is considered and can be seen in Figure 2.4. The output of the controller is the reference voltage v to be applied across the inductor. Moreover i represents the measured current through the inductor while i^* refers to its sinusoidal reference.

The closed-loop transfer function of the system is given by:

$$G_c(s) = \frac{K_p s + K_i}{s^2 L + K_p s + K_i} \tag{2.30}$$

Analyzing the transfer function, it can be determined that the zero static error can be obtained if $G_c = 1$, as then $i = i^*$. In the frequency domain the transfer function becomes:

$$G_c(j\omega) = \frac{K_i + j\omega K_p}{K_i + j\omega K_p - \omega^2 L} \tag{2.31}$$

Unity gain for the aforementioned transfer function can be obtained only at $\omega = 0$. Hence, it can be concluded that a PI controller can not track a sinusoidal reference without amplitude and phase errors as $|G_c(j\omega)| \neq 1$ and $arg G_c(j\omega) \neq 0$ for $\omega \neq 0$.

2.3.2 PR controller and parameter selection

In the previous section the limitations of PI controllers and its inability to accurately track a sinusoidal reference signal was discussed. Thus as an alternative, one of the options is to use a Proportional-Resonant controller. Using this type of controllers, the resonant component ensures unity gain of the closed-loop transfer function for the designed angular frequency as the PI achieves for $\omega = 0$. Another advantage of using a PR controller is that it can track negative sequence components as well. For this purpose a closed-loop system with negligible inner resistance and control time delay is considered and can be seen in Figure 2.5

The open-loop transfer function can be seen in Equation 2.32, where h indicates the harmonic order of the signal the be tracked.

$$G_k(s) = \frac{K_p[s^2 + (h\omega_1)^2] + K_h s}{[s^2 + (h\omega_1)^2] sL} \tag{2.32}$$

While the closed-loop transfer function becomes:

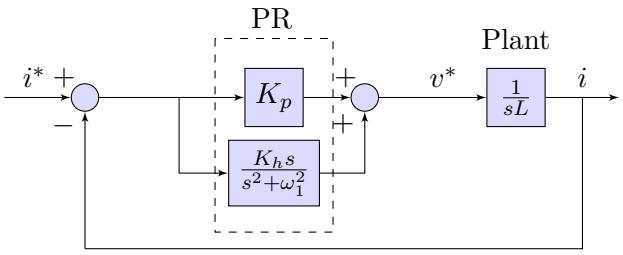

Figure 2.5: Control loop of the current using a PR controller.

$$G_c(s) = \frac{G_{k(s)}}{1 + G_{k(s)}} = \frac{K_p[s^2 + (h\omega_1)^2] + K_h s}{(sL + K_p)[s^2 + (h\omega_1)^2] + K_h s} \tag{2.33}$$

Time Delays of the system

In order to improve the controller derived for ideal conditions, it is necessary to take into account actual system problems in digital control. One of the main problem in digital control are the delays. Therefore, the time delays to be considered are:

- Communication delays, delays in sensors, computation in DSP and FPGA and analog to digital conversion delay typically give a delay in the order of one sampling period T_s.
- There is a delay introduced in the PWM which normally is in the order of half of sampling period $(0.5T_s)$.

Hence, the total delay can be calculated as $T_d = 1.5T_s$.

Parameters Selection of PR controllers

In this section the parametrization of the gains of the controllers is design based on the bode stability criterion where mathematical derivations are provided in order to validate the obtained results.

Selection of P gain

During the design of the controller, both the Resonant and Proportional parts are going to be decoupled in the frequency domain, allowing them to study independently. Therefore, in order to determine the proportional gain of the controller the closed-loop transfer function given previously can be redefined for $K_h = 0$, leading to:

$$G_c(s) = \frac{K_p/L}{s + K_p/L} \tag{2.34}$$

Based on Equation 2.34, the system bandwidth is found to be K_p/L i.e. $|G_c(jK_p/L)|= 1/\sqrt{2}$. This is an important parameter as it defines the exponential convergence rate of the closed-loop system responding to transients. Easier to be understood the system bandwidth defines the range of frequencies the controller is able to handle without attenuation in the output. For the same reason it is closely related with the speed response of the system i.e. step impulse as it ideally requires infinite harmonics for the signal to be reproduced.

Hence, the system bandwidth can be expressed as:

$$\alpha_c = \frac{K_p}{L} \tag{2.35}$$

where, the selection of the proportional gain can be accurately determined as:

$$K_p = \alpha_c L \tag{2.36}$$

Closed-loop system bandwidth selection

The closed-loop system bandwidth is calculated based on bode stability criterion. Thus, the expression for the phase margin is given by:

$$\phi_m = \pi + \arg\left(G_k\left(j\alpha_c\right)\right) \tag{2.37}$$

where the angle of the open-loop transfer function is calculated as the sum of the angles of each individual transfer function $G_k(s)$. Therefore, considering the introduced time delay the open-loop transfer function becomes:

$$G_k(j\alpha_c) = K_p \frac{1}{Ls} e^{-sT_d} \tag{2.38}$$

The proportional gain being positive results in a angle of 0 dB while the inductor introduces $-\frac{\pi}{2}$ and finally the delay produces $-1.5\omega T_s$ giving the expression:

$$\phi_m = \frac{\pi}{2} - 1.5\alpha_c T_s \tag{2.39}$$

Therefore, solving for the desired phase margin the system bandwidth can be calculated as:

$$\alpha_c = \frac{\frac{\pi}{2} - \phi_m}{1.5T_s} \tag{2.40}$$

As the phase margin is calculated for the crossover frequency, solving Eq. 2.38 for $|G_k(j\alpha_c)|= 1$ results in a K_p matching with the one proposed in Equation 2.36.

Selection of R gain

During the proportional gain selection procedure just presented above, the system was approximated as in Equation 2.34 disregarding the impact the resonant term of the controller has over the system stability.

A proper parametrization for the resonant gain calculation can be done as follows:

$$K_h = 2\alpha_h \alpha_c L \tag{2.41}$$

where, α_h represents the resonant part bandwidth.

Substituting Equation 2.41 into Equation 2.33 yields to:

$$G_c(s) = \frac{K_p[s^2 + (h\omega_1)^2] + 2\alpha_h \alpha_c L s}{(sL + K_p)[s^2 + (h\omega_1)^2] + 2\alpha_h \alpha_c L s} \tag{2.42}$$

Moreover, it an be rewritten as:

$$G_c(s) = \frac{K_p[s^2 + 2\alpha_h s + (h\omega_1)^2]}{(sL + K_p)[s^2 + 2\alpha_h s + (h\omega_1)^2] + 2\alpha_h s^2} \tag{2.43}$$

Neglecting the last term in the denominator, Equation 2.43 gets simplified to the closed-loop transfer function with pure proportional gain as in Equation 2.34, yielding to:

$$G_c(s) = \frac{K_p[s^2 + 2\alpha_h s + (h\omega_1)^2]}{(sL + K_p)[s^2 + 2\alpha_h s + (h\omega_1)^2]} \tag{2.44}$$

However, calculating the poles from Equation 2.42 and Equation 2.44 yields to the conclusion that for the aforementioned approximation to be valid, it is needed that:

$$\alpha_h \ll \alpha_c \tag{2.45}$$

Furthermore, in order to determine analytically the resonant component bandwidth (α_h) [20] is considered, which results in an another feasible gain calculation method. Considering the resonant controller open-loop transfer function as:

$$G_k(s) = K_p\left(1 + \frac{1}{t_r}\frac{s}{(s^2 + (hw_1)^2)}\right) \tag{2.46}$$

where, following the aforementioned reference the time constant t_r for the resonant part can be expressed as:

$$t_r = \frac{10}{\alpha_c} \tag{2.47}$$

From Equation 2.46 it can be concluded that:

$$K_h = \frac{K_p}{t_r} \tag{2.48}$$

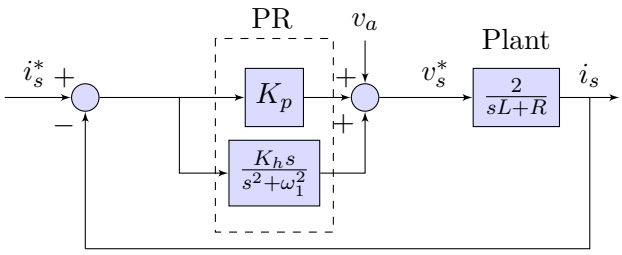

Figure 2.6: Output Current Control Loop.

Finally, combining Equation 2.41 and Equation 2.48 the resonant term bandwidth can be expressed as:

$$\alpha_h = \frac{1}{2t_r} \tag{2.49}$$

Analytically, with the aforementioned control design it is ensured that the effect of the resonant term of the controller does not modify the system stability performed during the design of the proportional controller.

2.3.3 Output Current Controller

Since, i_s is a fundamental frequency sinusoid, and the ability of PR controller to accurately track the sinusoidal reference, the above mentioned designed strategy can be implemented in controlling the output current of an MMC. The output current mathematical expression as presented in Equation 2.16 can be solved for i_s, which results in the plant transfer function as:

$$i_s = \frac{2}{sL + R}(v_s - v_a) \tag{2.50}$$

In the previous equation it can be seen that the output current is driven by the voltage difference $v_s - v_a$. It is ideally a sinusoidal fundamental frequency, however depending on the SCR, v_a will vary as a function of the output current. Moreover, when faults occur in the grid i.e sags, angle jumps appears for a short duration and the AC voltage will contain a negative sequence if the faults are asymmetrical. Therefore, since v_a is a measurable parameter and its effect in the control structure can be compensated by a feed forward.

As aforementioned in subsection 2.2.1, the voltage command v_s^* takes part in the calculation of the insertion indices. Due to malfunctions in the system, the controller output can exceed its limits and a saturation block is needed to be implemented to ensure proper insertion indices calculation and providing proper gate signals to the semi-conducting devices. The output voltage limits are described in Equation 2.17, which can be used to implement the upper and lower limits along with the saturation block implementation.

However, when the reference voltage from the control goes into saturation another issue appears. Due to nonlinearities, the controller accumulates a bigger error than in non-saturated operation. This issue is well known as resonant windup and drives the system into undesired situations once the voltage saturation is gone i.e. over current in the output. Therefore a so-called anti-windup which is able to release the error accumulated during saturated operations in the voltage reference needs to be implemented [21]. The modified error in this case is calculated as:

$$e' = e + \frac{1}{K_p}(v_s^* - v_s^{*0}) \tag{2.51}$$

where, v_s^{*0} corresponds to the voltage reference after the saturation block.

This scheme can be seen in the Appendix A containing the implemented model in PLECS.

2.3.4 Internal Control of Modular Multilevel Converters

The internal variables to be considered and controlled in an MMC are the capacitor voltages of the upper and lower arms in a leg and the circulating current. The equations showing their relations affecting the system dynamics were depicted before and for the readers simplicity are presented once again.

$$\frac{C}{N}\frac{\mathrm{d}v_{cu}^{\Sigma}}{\mathrm{d}t} = n_u\left(\frac{i_s}{2} + i_c\right) \qquad \frac{C}{N}\frac{\mathrm{d}v_{cl}^{\Sigma}}{\mathrm{d}t} = n_l\left(-\frac{i_s}{2} + i_c\right)$$

$$L\frac{\mathrm{d}i_c}{\mathrm{d}t} = v_c - Ri_c$$

According to the analysis done until now and as seen in subsection 2.3.4, it can be inferred that there are three variables per leg to be controlled with only one degree of freedom which is the circulating current. On the other hand, it can be seen how the sum capacitor voltages are directly related with the insertion indexes as well as with the output and circulating currents. It is worthy to mention that the output current controller has to ensure good performance regardless of the internal situation of the controller. Therefore, the insertion indices and the output current control are the variables to be determined in order to ensure control over the three variables mentioned before.

Moreover, individual control of the voltage in each cell has to be implemented, however as it is explained in section 2.4 this goal is achieved by the modulation implemented in the system.

2.3.5 Circulating Current Controller

The circulating current is a physical degree of freedom that account for the internal control of the MMC, in fact as shown before in the equations it is linked with the sum capacitor voltage value and the output of its controller is one of the variables

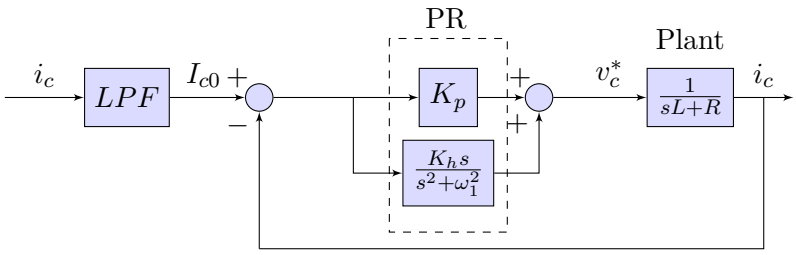

Figure 2.7: Circulating Current Control Loop.

accounting for the insertion indices calculation. Therefore, a proper control for the circulating current needs to be designed as well.

The transfer function can be easily found from Figure 2.7 to be:

$$i_c = \frac{1}{sL + R} v_c \tag{2.52}$$

An analysis of the circulating current signal can be done considering Equation 2.23. The first term of the equation refers to the dc power term what implies that the circulating current DC term is responsible for the power transfer from the DC bus to the internal capacitors of the MMC. This term equals to $I_{c0} = \frac{i_d}{M}$. On the other hand, the last term of the equation shows how a second order harmonic term with mean value 0 appears in the power sum of each leg. Therefore, a parasitic Δv_c containing this second order harmonic term will appear, carrying a current component of the same order into the circulating current.

Hence, the circulating current can be expressed as:

$$i_c = I_{c0} + \hat{I}_{c2} cos(2w_1 t + \phi_{c2}) \tag{2.53}$$

The dc term is not desired to be controlled at the moment as it is in charge of the power exchange between DC-AC which is of utmost importance in HVDC applications. However, the second harmonic component will only increase the rating of the power components without bringing any additional benefit into the system. Thus, a PR controller is implemented as shown in Figure 2.7 where the resonant part is designed to be able to track a second harmonic sinusoid.

The error signal in Figure 2.7 can be expressed as:

$$e = I_{c0} - I_{c0} - \hat{I}_{c2} cos(2w_1 t + \phi_{c2}) \tag{2.54}$$

where, the controller will track a second harmonic component equal in amplitude but shifted by 180º from the one in the circulating current and will eliminate it which can be seen in Figure 2.12.

Finally, it is important to point out that for the circulating current controller there is no necessity of implementing saturation and anti-windup schemes as the contribution of the circulating current control is normally small.

Parameters	Notation	Value
P(MW)	Active Power	1000
N_{arm}	Submodules/arm	40
V_{dc}(kV)	Direct voltage	640
C_{sm}(mF)	Capacitance	1.25
L_{arm}(mH)	Arm Inductance	20
V_g(kV)(l-l)rms	Alternating voltage	400
f(Hz)	Rated frequency	50
fs(Hz)	Sampling frequency	10000

Table 2.1: Simulated Parameters for 1GW plant

2.3.6 Simulations results obtained implementing the controllers

The plant selected for performing simulations in order to validate the gathered theoretical results is presented in Table 2.1 [22].

Output current controller design

The system phase margin is desired to be 45°. As it is observed in Equation 2.50, the output current controller plant inductance equals to $\frac{L}{2}$. Therefore, combining Equation 2.36, Equation 2.40, Equation 2.47 and Equation 2.49 yields to:

$$K_p = \alpha_c \frac{L}{2} = \frac{50\pi}{3} \qquad \alpha_h = \frac{250\pi}{3} \qquad K_h = 2\alpha_h \alpha_c \frac{L}{2} \approx 27415.5$$

The bode plot of the open-loop transfer function as shown in Equation 2.34 for the calculated proportional gain is presented in Figure 2.8. It is proved how the proportional gain is correctly calculated as the phase margin and crossover frequency match with the designed one.

Moreover, Figure 2.9 depicts how the resonant gain is also calculated properly, although the phase margin is slightly modified due to its effect, the system remains stable for the bandwidth.

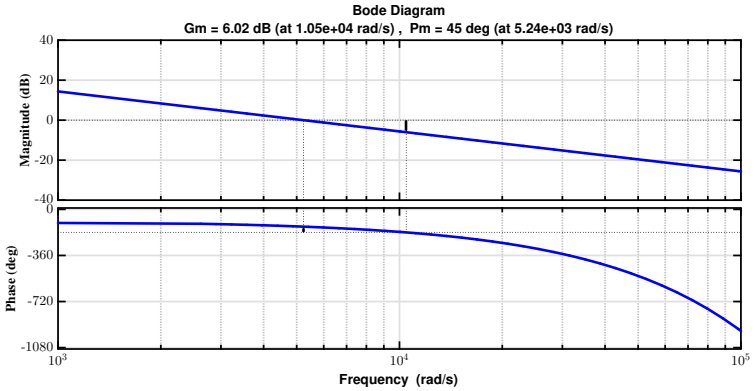

Figure 2.8: Bode plot of the output current controller neglecting the resonant component.

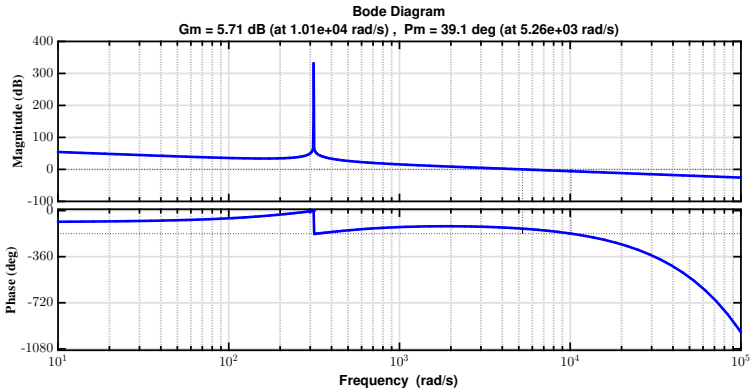

Figure 2.9: Bode plot of the output current controller considering the resonant component.

Circulating current controller design

This controller is designed with the intention of decoupling it in the frequency spectrum from the output current controller. Hence, the circulating current controller is designed to be ten times slower ensuring that the bandwidth of the specific controllers do not interact with each other. Therefore, for the plant parameters already presented in the control design yields to:

$$K_p = w_c L = \frac{10\pi}{3} \qquad \alpha_h = \frac{25\pi}{3} \qquad K_h = 2\alpha_h \alpha_c L \approx 548.3$$

For this parameter selection, the phase margin of the system following Equation 2.40 results in:

$$\phi_m = 85.5^{\circ}$$

As presented for the output current controller, the bode plots neglecting and considering the resonant component are presented in Figure 2.10 and Figure 2.11

respectively. Also in this case the operating point considered in the design process can be verified in the images.

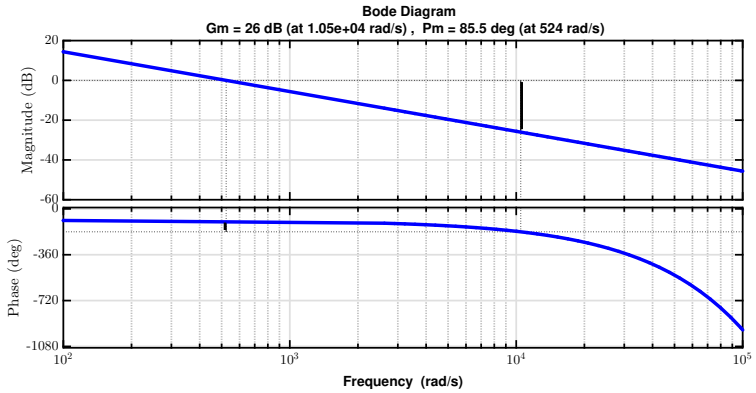

Figure 2.10: Bode plot of the circulating current controller neglecting the resonant component.

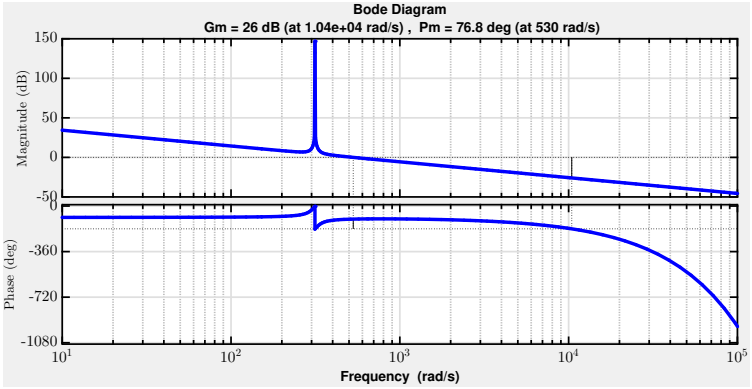

Figure 2.11: Bode plot of the circulating current controller considering the resonant component.

By simulations the effect of the circulating current controller for the purpose of eliminating the second harmonic is depicted in Figure 2.12 where the reduction of this frequency component is clearly shown.

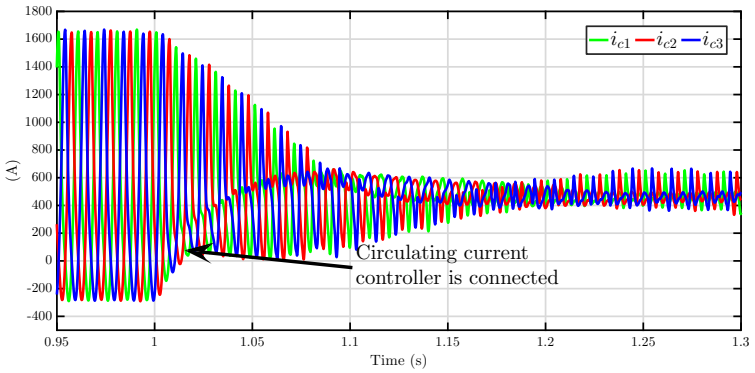

Figure 2.12: Second harmonic reduction in the circulating current when the control is enabled at a time instant of 1s.

2.4 Carrierless Modulation technique

As it has been known from the above study that in MMC with large number of submodules, internal control has to be established ensuring the balance between the cell capacitor voltages along with the control of the circulating current. Different modulation techniques can be used to generate the required reference voltage which is responsible of controlling the transmitted power as desired and also to ensure equal capacitive energy distribution. A carrierless modulation strategy named Nearest Level Control (NLC) with variants:

- Basic Sorting
- Capacitor Tolerance Band(CTB)
- Reduced sorting switching(RSS)

are presented as an alternative of the conventional modulation carrier based techniques for this thesis. The main advantage of using NLC is its easy implementation, it also eliminates the neccesity of employing an extra control for individual cell voltage balancing and since it reduces the switching frequency inferring reducing the switching losses.

2.4.1 Basic Sorting

By sampling the reference signal, referred to each arm of the MMC, with a determined sampling frequency f_s and applying the convenient algorithm it is possible to know the required number of submodules to be inserted. In order to abstract the number of submodules to be inserted in each T_s instant from the reference signal different programming solutions can be used. Here, by dividing the reference voltage by the rated capacitor voltages and further by computing the $round(x)$ function, the required number of submodules is known as a $float$ exactitude variable which can

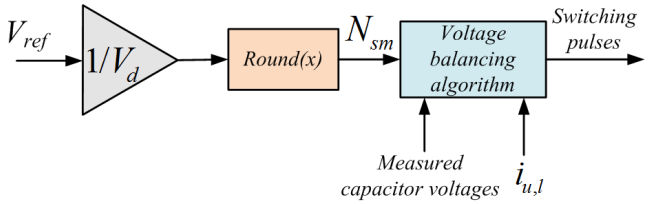

Figure 2.13: Block Diagram representation of Nearest Level Control

be seen in Figure 2.13. Furthermore, a sorting algorithm ranks the cells based on their capacitor voltage levels in ascending/descending order depending on the current direction(positive/negative) and thereafter selects the required number of cells to be inserted from the designed sorted list. This method requires them to capture all measured cell voltages and sort them with a high sampling frequency [23]. A flowchart showcasing the implementation of this basic sorting algorithm can be shown in Figure 2.14.

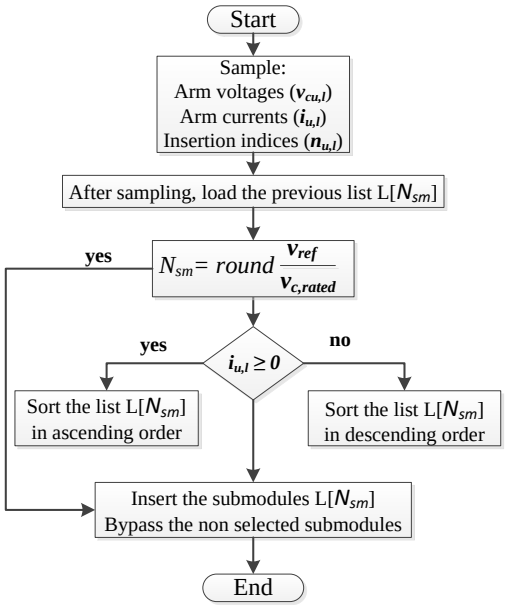

Figure 2.14: Flowchart displaying implementation of Nearest Level Control

Effect and design of Sampling frequency

In carrier-less modulation methods like NLC, the sampling frequency is one of an important factor to be taken into consideration along with number of submodules and modulation index when considering real systems in practice where there are large number of submodules per arm. In order to select an appropriate sampling frequency, two critical values, which significantly influence the output voltage levels

and total harmonic distortion can be seen in [24].

2.4.2 Capacitor tolerance band(CTB)

The basic sorting samples every sampling instant. On the other hand, the switching frequency depends on the updated sampling frequency of the sorted list and it might possibly end up with the high switching frequency depending on the chosen sampling frequency and there is no control over the capacitor voltage ripple. This method as shown in Figure 2.15 ensures that the capacitor voltages stay within the desired limit.

This method inserts the requested number of cells (N_{level}) according to the sorted list which is created when a cell capacitor voltage goes beyond the upper ($V_{cu,l} + \delta$) or lower ($V_{cu,l} - \delta$) voltage limit where, δ is the specified voltage ripple. When cell capacitor voltage hits the limit a new sorted list will be generated and sorting is performed with the updated list during the next time step. The arm current direction decides if the ranking should be done in ascending or descending way. Since, this method only sorts when the capacitor voltages exceeds the specified tolerance band, it reduces the number of sorting actions which is a great advantage from control point of view [16].

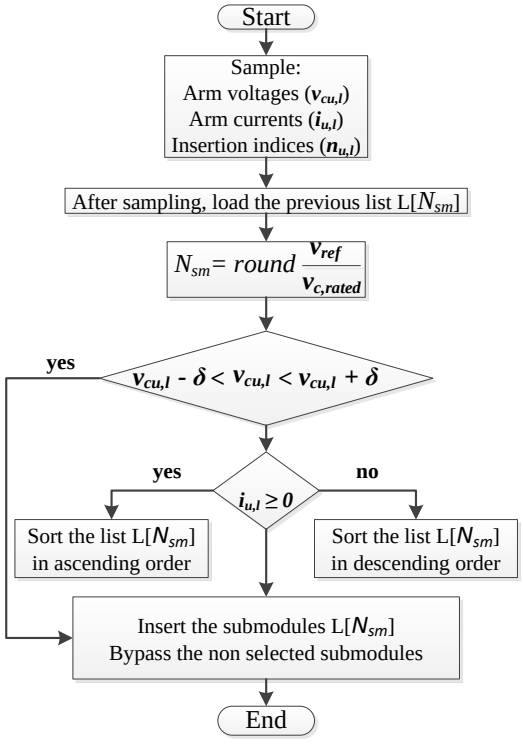

Figure 2.15: Flowchart displaying implementation of NLC-CTB

2.4.3 Reduced sorting switching(RSS)

This enhanced method as shown in Figure 2.16 is implemented to reduce the switching frequency and thus the switching losses in a converter. This method inserts the requested number of cells (N_{level}) according to the sorted list which is created when there is a change in the output voltage level only and sorting is performed with the updated list during the next time step. In other words, when $N_{level}(k) \neq N_{level}(k-1)$. Even here the arm current direction decides if the ranking should be done in ascending or descending way as in the aforementioned methods. Hence, implementation of this method ensures very low switching frequency without taking into consideration the capacitor voltage ripple. Thus, a better approach can be used where an amalgamation of CTB and RSS can be taken into consideration to create a sorting list where aforementioned criteria can be achieved, i.e reduced switching frequency and limiting the capacitor voltage ripple.

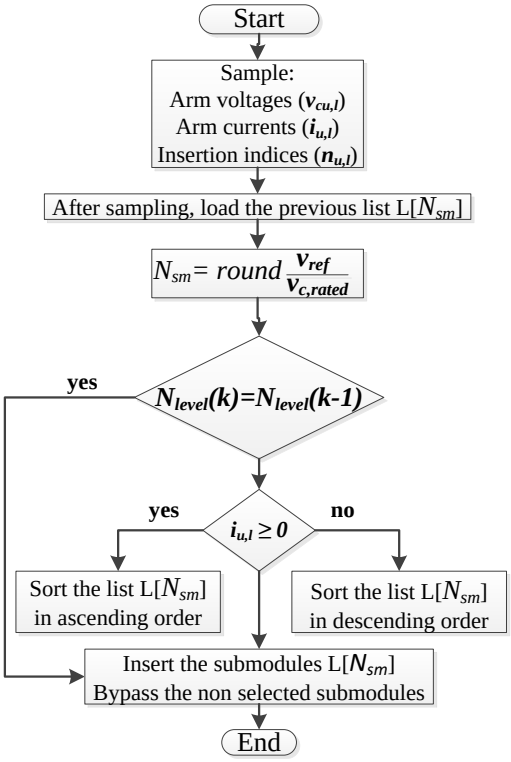

Figure 2.16: Flowchart displaying implementation of NLC-RSS

Summary

This chapter aimed to introduce the internal dynamics of the MMC. Based on the average modeling, the control challenges of the converter are presented and a solution is proposed. As part of the basic needs for the converter to run covering its goal in a HVDC application, the design of internal circulating current control and output-current control is proposed and results validating the theoretical tuning with the simulation implementation has been explained. Finally, the different modulation techniques are explained in brief.

Chapter 3

Control of the MMC Under Unbalanced Conditions

In this chapter, unbalance situations in the MMC dealt during the development of this thesis are presented. Regarding the converter itself, an unbalance refers to the situation where the averaged model as presented in Figure 2.2 varies due to asymmetries in the system or faults in the grid side which mainly focuses about the voltage value of the cell capacitors. Part of the work carried out on this has been published in IECON 2016 conference.

On the other hand, faults in the grid side are also considered as unbalanced situations, the converter faces in its normal operation. During grid faults, a current injection strategy complying with the grid codes is also presented. Furthermore, an important issue the converter faces due to unbalances in the grid side is presented and described in detail.

A section is included showcasing the work performed in relation with an accepted paper sent to IEEE conference(EEEIC 2016). It is related with the study and impact of the system when injecting second order harmonic in the circulating current. Finally, link between control under unbalance conditions and the final section about injection strategy is presented.

3.1 Mitigating the internal unbalance

The internal structure of the MMC is not completely symmetrical due to asymmetries in the components such as inductors, capacitors etc. These asymmetries induce undesired differences in the energy storage between the arms of the converter. Thus, the study of the energy flow inside the converter needs to be carried out in order to propose a suitable solution for the presented challenge where these differences between the voltages and the energy stored in the arms can be eliminated by exchanging energy between the arms and leg of an MMC. A feasible solution to the aforementioned problem is proposed in [25].

3.1.1 Unbalance in the energy storage between arms in the same leg of an MMC

Once the general challenge is introduced, an analytical study is carried out. Solving Equation 2.21 for the voltage in the arms yields to:

$$v_{cu}^{\Sigma} = \frac{1}{C_{arm}} \int n_u \left(\frac{i_s}{2} + i_c \right) dt \quad v_{cl}^{\Sigma} = \frac{1}{C_{arm}} \int n_l \left(-\frac{i_s}{2} + i_c \right) dt \tag{3.1}$$

where the equivalent arm capacitance is referred as C_{arm} for simplicity. The insertion indices expressed in Equation 2.29 are rewritten as:

$$n_u = \frac{\frac{v_d}{2} - v_s^*}{v_d} \quad n_l = \frac{\frac{v_d}{2} + v_s^*}{v_d} \tag{3.2}$$

where, v_c is not considered for simplicity as it is normally very small.

On the other hand, the circulating and output currents are substituted as follows:

$$i_c = I_{c0} \quad i_s = \hat{I}_s cos(wt + \phi_i) \tag{3.3}$$

Inserting the current definitions in Equation 3.1 yields to:

$$v_{cu}^{\Sigma} = \frac{1}{C_{arm}} \int \frac{\frac{v_d}{2} - v_s^*}{v_d} \left(I_{c0} + \hat{I}_s cos\left(wt + \phi_i\right) \right) dt \tag{3.4}$$

$$v_{cl}^{\Sigma} = \frac{1}{C_{arm}} \int \frac{\frac{v_d}{2} + v_s^*}{v_d} \left(I_{c0} - \hat{I}_s cos\left(wt + \phi_i\right) \right) dt \tag{3.5}$$

Multiplying both sides of the Equation 3.4 and Equation 3.5 by $C_{arm} v_{cu}^{\Sigma}/2$, the arm energy expressions are obtained:

$$\frac{C_{arm}}{2} \left(v_{cu}^{\Sigma} \right)^2 = \frac{v_{cu}^{\Sigma}}{2} \int \frac{\frac{v_d}{2} - v_s^*}{v_d} \left(I_{c0} + \hat{I}_s cos(wt + \phi_i) \right) dt \tag{3.6}$$

$$\frac{C_{arm}}{2} \left(v_{cl}^{\Sigma} \right)^2 = \frac{v_{cl}^{\Sigma}}{2} \int \frac{\frac{v_d}{2} + v_s^*}{v_d} \left(I_{c0} - \hat{I}_s cos(wt + \phi_i) \right) dt \tag{3.7}$$

Equating for $\hat{V}_s = v_d/2$ and neglecting the ripple yields to:

$$\frac{C_{arm}}{2} \left(v_{cu}^{\Sigma} \right)^2 = \frac{v_{cu}^{\Sigma} I_{c0}}{4} t - \frac{v_{cu}^{\Sigma} \hat{I}_s}{8} t + W_{u0} \tag{3.8}$$

$$\frac{C_{arm}}{2} \left(v_{cl}^{\Sigma} \right)^2 = \frac{v_{cl}^{\Sigma} I_{c0}}{4} t - \frac{v_{cl}^{\Sigma} \hat{I}_s}{8} t + W_{l0} \tag{3.9}$$

where the constant terms refer to the stored energy in the arms which are normally considered to be equal to $C_{arm} v_d^2/2$, since $v_{cu,l}^{\Sigma}$ is normally desired to be controlled to v_d.

It might be noted that the first two terms on the right hand side of Equation 3.8 and Equation 3.9 cancels out with each other for the energy stored to be constant in the arms.

The gathered results until now gives information about the energy flow in the system, where the balance criterion is mathematically expressed as:

$$W_{u0} = W_{l0} \qquad v_{cu}^{\Sigma} = v_{cl}^{\Sigma} = v_d \tag{3.10}$$

Considering the circulating current to contain a fundamental frequency component as a result of unbalance between the capacitor voltages in the arms results in:

$$i_c = I_{c0} + \hat{I}_c cos(wt + \phi_c) \tag{3.11}$$

Introducing the circulating current as defined in Equation 3.6 and Equation 3.7, Equation 3.8 and Equation 3.9 can be rewritten as:

$$\frac{C_{arm}}{2}\left(v_{cu}^{\Sigma}\right)^2 = -\frac{v_{cu}^{\Sigma}\hat{I}_c}{8}t + W_{u0} \qquad \frac{C_{arm}}{2}\left(v_{cl}^{\Sigma}\right)^2 = \frac{v_{cl}^{\Sigma}\hat{I}_c}{8}t + W_{l0} \tag{3.12}$$

where the ripple is neglected and the first and second right hand terms in Equation 3.8 and Equation 3.9 have been disregarded as assumed to sum up to 0. Therefore, if $v_{cu,l}^{\Sigma}$ is assumed to be v_d and $W_{u0} = W_{l0}$, the energy difference $\Delta W = W_u - W_l$ can be expressed by subtracting Equation 3.12 as:

$$\Delta W = -\frac{v_d \hat{I}_c}{4}t \tag{3.13}$$

Rewriting the Equation 3.13 in Laplace domain yields to:

$$\Delta W = -\frac{v_d \hat{I}_c}{4s} \tag{3.14}$$

It can be concluded that the fundamental frequency component injection in the circulating current allows to transfer energy from the upper to the lower arms in the leg as depicted in Figure 3.1.

Moreover, it is important to mention that the system as presented in Equation 3.12 is non-linear as two state variables are multiplied. However, by linearizing the system and considering the state variable $v_{cu,l}^{\Sigma}$ to be constant v_d as in Equation 3.10, simplifies the analytical study of the system.

Controlling the energy flow between arms: Arm Balancing Control

With the gathered results until now, a controller which is able to ensure energy balance between the arms in each leg is proposed. Its block diagram is depicted in Figure 3.5, where the mean values of the energy stored in the arms are subtracted and controlled to be 0 and the error is then passed through a proportional controller. It is

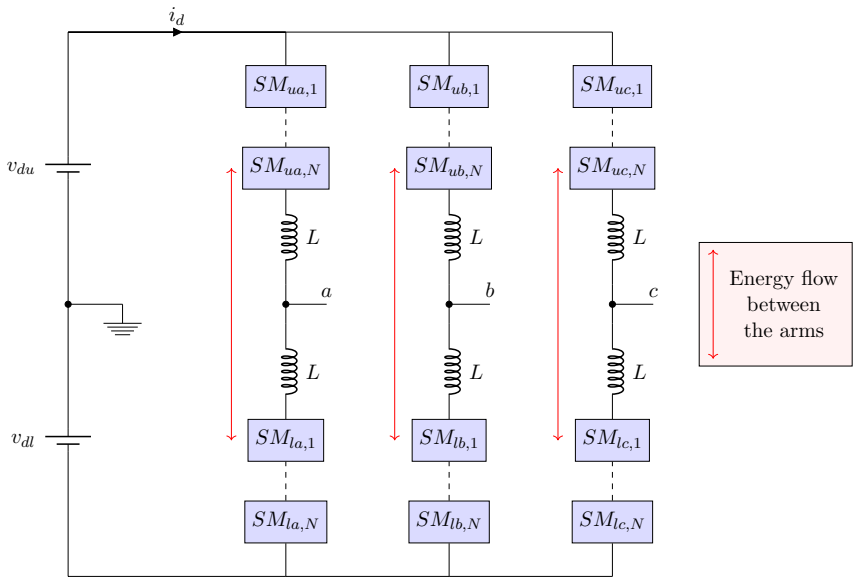

Figure 3.1: Arm Balancing Control Schematic.

to be noted that the integral part can be included in order to eliminate steady state errors. The generated current reference i_c^* is transformed from DC to fundamental frequency component and then fed into the circulating current controller. The plant transfer function as shown in the image is obtained from Equation 3.14.

It has to be noted that an injection of the aforementioned fundamental component current in the circulating current would unavoidably couple with the other phases of the converter, if no further action is taken. In this way, the energy level of each individual leg becomes difficult to be controlled independently since, undesired fundamental frequency components will flow in the rest of the legs, exchanging energy from the upper and lower arms respectively as seen in Figure 3.2. This problem was firstly noted in [26] and [25].

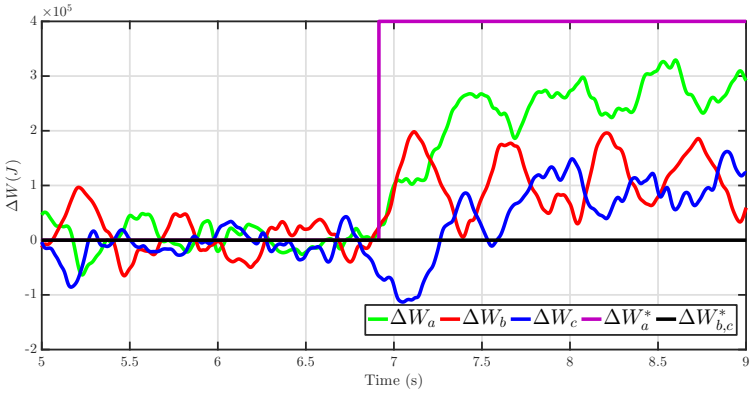

Figure 3.2: Energy difference in each leg when energy balancing controller is implemented

A control system to avoid this active power coupling between the arms was implemented in [26]. The main idea of this implementation is the injection of active current in the phase desired to be balanced and reactive currents in the rest of the phases so the injected currents sum up to 0 in the positive and negative nodes, without flowing into the rest of the phases and ensuring equal energy storage.

Thus, a comprehensive and easy to implement method is presented based on the idea that was done collectively together with master student Georgios Tsolaridis of Aalborg University. Due to symmetries, an unbalance in phase-a is considered as a case study, but the result can be extended to the other two phases as well. Since phase-a is unbalanced, an active current (in phase with the voltage of phase-a) should be applied as shown in Figure 3.3. As noted before, Equation 3.15 gives the sum of the fundamental components of the circulating current:

$$i_{c1a} + i_{c1b} + i_{c1c} = 0 \tag{3.15}$$

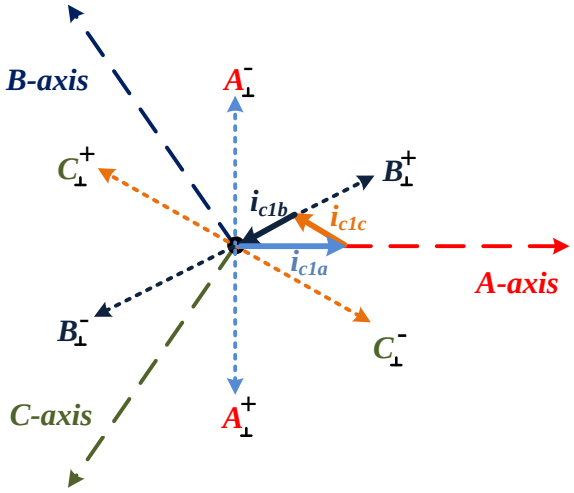

Figure 3.3: Vectorial representation of fundamental component of circulating current for arm balancing strategy

The reactive axes of phase-b and phase-c could be combined to form a vector that is opposite to the active vector of phase-a, as shown in Figure 3.3. Therefore the magnitude of the vectors needs to be determined. Based on basic trigonometry, the amplitude of the vectors of phase-b and phase-c are $\sqrt{3}$ times smaller than the vector of phase-a. In this way, the sum of the three imposed vectors is zero. The final commanded current reference for all phases as shown in Equation 3.16 becomes:

$$
\begin{aligned}
I^*_{c1_a} &= Kv_a cos(\omega t) + \frac{1}{\sqrt{3}} v_b cos\Big(\omega t + \frac{\pi}{2}\Big) + \frac{1}{\sqrt{3}} v_c cos\Big(\omega t - \frac{\pi}{2}\Big) \\
I^*_{c1_b} &= Kv_b cos\Big(\omega t - \frac{2\pi}{3}\Big) + \frac{1}{\sqrt{3}} v_a \cos\Big(\omega t - \frac{2\pi}{3} - \frac{\pi}{2}\Big) + \frac{1}{\sqrt{3}} v_c cos\Big(\omega t - \frac{2\pi}{3} + \frac{\pi}{2}\Big) \\
I^*_{c1_c} &= Kv_c\, cos\Big(\omega t + \frac{2\pi}{3}\Big) + \frac{1}{\sqrt{3}} v_a cos\Big(\omega t + \frac{2\pi}{3} + \frac{\pi}{2}\Big) + \frac{1}{\sqrt{3}} v_b cos\Big(\omega t + \frac{2\pi}{3} - \frac{\pi}{2}\Big)
\end{aligned}
\tag{3.16}
$$

3.1.2 Unbalance in the energy storage between the legs of an MMC

Another common issue in the energy unbalance inside the MMC resides in the current circulating between legs when $v^{\Sigma}_{cu} + v^{\Sigma}_{cl} \neq 2v_d$. It induces the necessity of including a control scheme which is capable of controlling the sum capacitor voltages in each leg to be equal to $v^{\Sigma}_{c} = 2v_d$.

By adding right and left hand side equations in Equation 2.21 and considering the insertion indices as in Equation 2.29 yields to:

$$
v^{\Sigma}_{c} = \frac{1}{C_{arm}} \int \Big(i_c - \frac{v^*_s i_s}{v_d}\Big) dt \tag{3.17}
$$

It can be found that the first and second right hand side expression are the terms responsible for the power exchange per phase. Substituting $\frac{v^*_s i_s}{v_d}$ by $\frac{P}{Mv_d}$ yields to:

$$
v^{\Sigma}_{c} = \frac{1}{C_{arm}} \int \Big(i_c - \frac{P}{Mv_d}\Big) dt \tag{3.18}
$$

It is already shown in Equation 3.8 and Equation 3.9, how the circulating current carries the power into the leg capacitors from the DC side. Moreover, the circulating current is related with the current flowing from the DC-bus as seen in Figure 2.1 where, $i_{dc} = Mi_c$. Normally, the DC-link voltage control is designed based on a fast current control, and the DC-bus dynamics are slower than the ones considered until now for the capacitors in each leg. Therefore, the DC-bus dynamics have to be considered while designing the sum capacitor voltage control [27]. Now, it can be seen from dynamics of MMC that:

$$
v_d = \frac{1}{C_d} \int (i_d - Mi_c)\, dt \tag{3.19}
$$

where i_d is the current carrying the power into the DC-bus capacitor and C_d the DC-bus capacitance.

As previously mentioned, the sum capacitor voltage is desired to be kept at $2v_d$. This conjecture allows to rewrite Equation 3.19 by substituting $v_d = \frac{v^{\Sigma}_c}{2}$:

$$
\frac{v^{\Sigma}_{c}}{2} = \frac{1}{C_d} \int (i_d - Mi_c)\, dt \tag{3.20}
$$

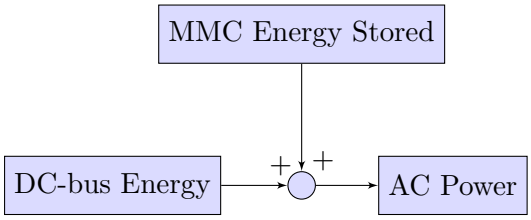

Figure 3.4: Principle of the Sum Capacitor Voltage controller functionality.

Assuming the DC and AC power to be equal infers that $i_d = \frac{P}{v_d}$. Furthermore, solving Equation 3.18 and Equation 3.20 for v_c^{Σ} and i_c yields to:

$$\left(\frac{C_d}{2} + (M+1)\, C_{arm}\right) \frac{dv_c^{\Sigma}}{dt} = i_c - \frac{P}{M v_d} \tag{3.21}$$

The equivalent capacitance value in the left hand side of the equation accounts for the effective leg capacitance dynamics including the DC-bus capacitor.

Therefore, the objective of the proposed controller resides in controlling the constant term of the circulating current in order to change the amount of energy being delivered into the internal capacitors of the MMC. As a consequence, for the same output power required from the load, the energy stored in the submodule capacitors varies resulting in the variation in capacitor voltages. The operating principle of the controller is depicted in Figure 3.4. In normal operation, the full energy from the DC-bus is delivered to the AC side to accomplish for the active power requirement without storing any extra energy in the cell capacitors. In case, when the energy stored in the cell capacitors in the MMC is different from the nominal value i.e corresponding per phase to $2v_d$, I_{c0} can be modified changing the energy stored inside the MMC.

3.1.3 Tuning and Simulation results of the Energy Controllers

Vertical Balancing Controller

Accordingly to Equation 3.14 the first term in the right hand of the equations yields to the controller plant transfer function:

$$\frac{\Delta W}{\hat{I}_c} = \frac{v_d}{4s}$$

It i to be noted that a resonant component able to track a fundamental frequency signal has to be included in the circulating current controller. A well-establish strategy to tune an outer loop controller consists of tuning it slower than the inner loop, making sure that the bandwidth does not interact with the inner loop controller so it is decoupled. If the resonant part of the circulating current controller is not taken into consideration, i.e. the bandwidth is determined by the proportional component, the control diagram of the system can be showcased as in Figure 3.5.

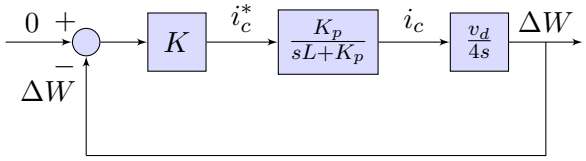

Figure 3.5: Arm Balancing Control Loop.

The open loop-transfer function of the system becomes:

$$G_K(s) = \frac{KK_pV_d}{4s(sL + K_p)} \tag{3.22}$$

yielding to the closed loop transfer function

$$G_c(s) = \frac{\frac{KK_pV_d}{4L}}{s^2 + \frac{K_p}{L}s + \frac{KK_pV_d}{4L}} \tag{3.23}$$

As it can be appreciated Equation 3.23 corresponds to a second order system transfer function which parameters are:

$$2\zeta w_n = \frac{K_p}{L} \qquad w_n^2 = \frac{KK_pV_d}{4L} \tag{3.24}$$

As the controller is desired to be designed slower than the circulating current controller, $\zeta > 1$ is considered ensuring that there is no overshoot under a step input. The function drawn by the step response of the system is determined by:

$$y(t) = K_0\left[1 - \frac{w_n}{2\sqrt{\zeta^2 - 1}}\left(\frac{e^{p_1 t}}{p_1} - \frac{e^{p_2 t}}{p_1}\right)\right] \tag{3.25}$$

where K_0 refers to the system gain and $p_{1,2}$ describes as

$$p_{1,2} = -\zeta w_n \pm w_n\sqrt{\zeta^2 - 1} = -w_n\left(\zeta \pm \sqrt{\zeta^2 - 1}\right) \tag{3.26}$$

Analyzing the mathematical expression yields to non analytical possible solution for t variable. Therefore in order to choose the time response of the system as desired, the solution is found by solving the nonlinear function with Matlab built-in 'fsolve' numerical method, which can be seen in Appendix C.

Simulations have been carried out in order to prove the developed theoretical analysis. The controller is ideally designed for a step response achieving 90 % of its final value in a time of 0.045s. The step response plotted using Matlab is depicted in Figure 3.6.

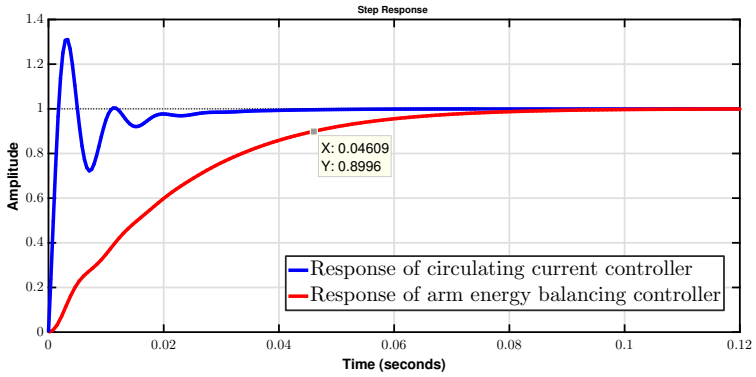

Figure 3.6: Step response of the designed arm balancing controller.

Furthermore, the bode diagram is shown in order to prove stability as seen in Figure 3.7.

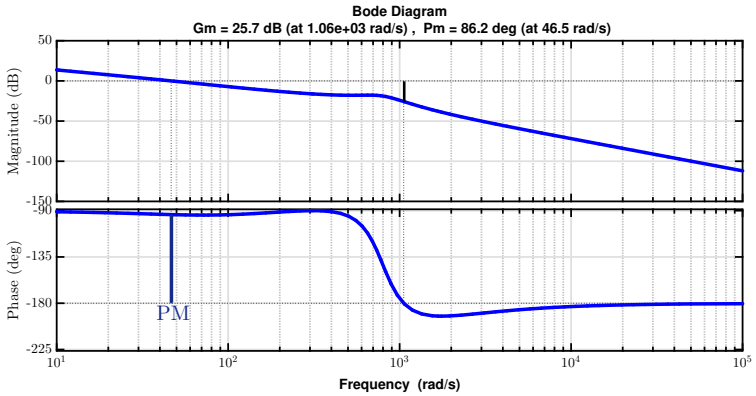

Figure 3.7: Bode plot of the arm balancing controller with a phase margin of 86.2°.

In order to validate the presented theoretical approach, a 20% arm inductor unbalance is simulated where the controller is connected at 5s as shown in Figure 3.8. It can be appreciated that the system achieves 90% of its reference in the expected time but on the other hand, overshoot appears even though the system was designed to be overdamped. It has to be mentioned here that for the controller design a linearized model has been used, thus this might be the reason for the overshoot.

Moreover, the sum capacitor voltages is shown for the upper and lower where the effect of the controller when it is connected can be seen in Figure 3.9. As expected the controller brings together the mean value of sum capacitor voltages.

Finally, a step of 100 kJ is applied in phase-a as depicted in Figure 3.10. It is interesting to note that the coupling effect between phases as seen in Figure 3.2 is compensated by the presented approach. The nature of the variables to be controlled (ΔW) results in the oscillations depicted in Figure 3.10.

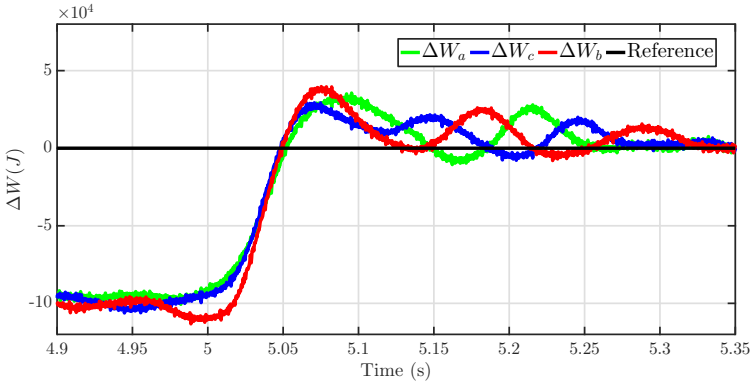

Figure 3.8: Response of the system when the controller is connected at the time instant of 5 seconds.

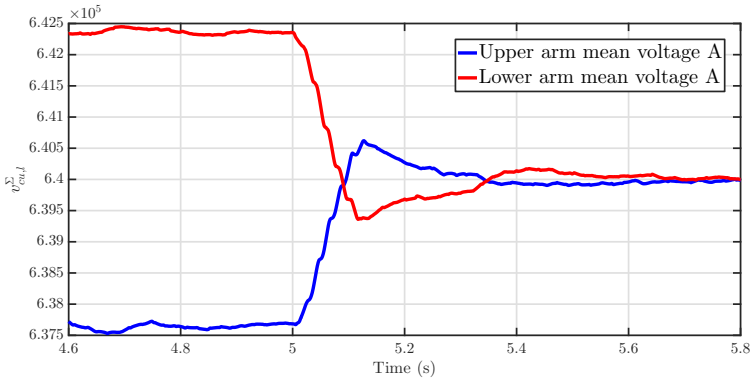

Figure 3.9: Upper and Lower arm mean voltage in phase-a when vertical energy controller is connected to attenuate a 20% arm inductor unbalance.

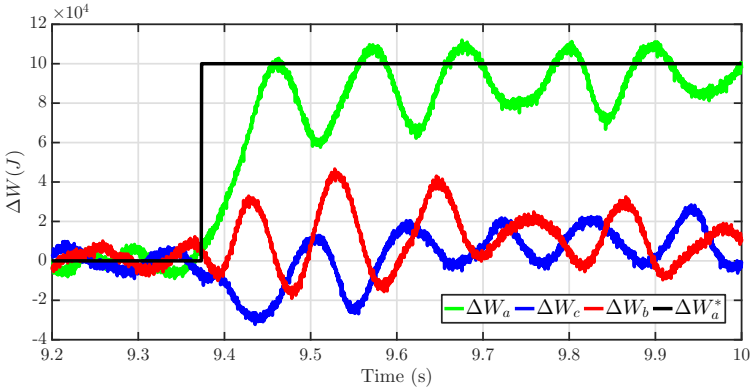

Figure 3.10: Response of the system when step is applied in phase-A.

Sum Capacitor Energy Controller

If in Equation 3.21 the equivalent capacitance is expressed as C_{eq} the first right hand side term in the equation yields to the plant transfer function:

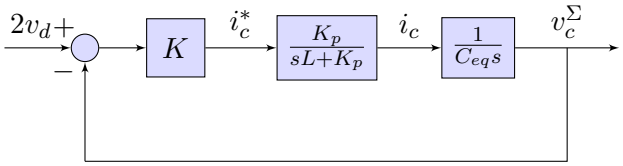

Figure 3.11: Sum Capacitor Energy Control Loop.

$$\frac{v_c^\Sigma}{I_{c0}} = \frac{1}{C_{eq}s}$$

Similarly, as for the arm balancing energy controller, an integrator has to be included in the circulating current controller able to track the constant term is provided from the Sum Capacitor Voltage controller. The control diagram of the Sum Capacitor Voltage Controller is depicted in Figure 3.11, where the reference is set to be $2v_d$ and compared with v_c^Σ. After being passed through a proportional controller, the circulating current reference I_c^* is fed to the aforementioned current controller.

For the case of this controller the closed loop transfer function becomes:

$$G_c(s) = \frac{\frac{KK_p}{C_{eq}L}}{s^2 + \frac{K_p}{L}s + \frac{KK_p}{C_{eq}L}} \tag{3.27}$$

where

$$2\zeta w_n = \frac{K_p}{L} \qquad w_n^2 = \frac{KK_p}{C_{eq}L} \tag{3.28}$$

The system is designed to achieve 90% of its final value in approximately 0.35s. The step response and bode diagram plotted using Matlab can be seen in Figure 3.12 and Figure 3.13 respectively.

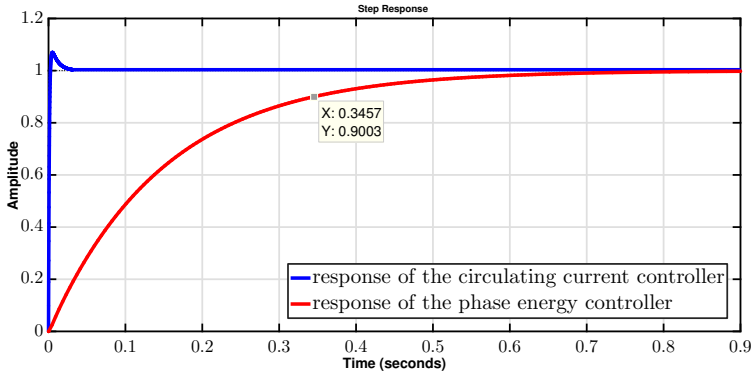

Figure 3.12: Step response of the designed sum capacitor energy controller plotted in Matlab.

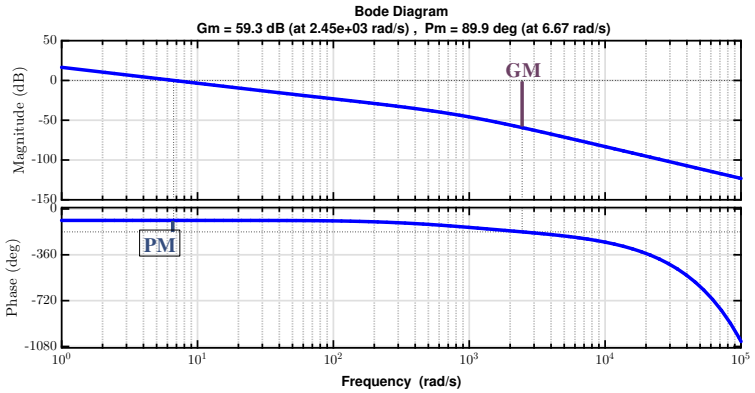

Figure 3.13: Bode plot of the sum capacitor energy controller with a phase margin of 89.9°.

Simulation results depict the concordance between the proposed theoretical analysis and tuning method with the obtained results. In Figure 3.14, v_c^{Σ} for all three phases is shown at the time instant when the controller is connected. As appreciated the system response matches with the desired one.

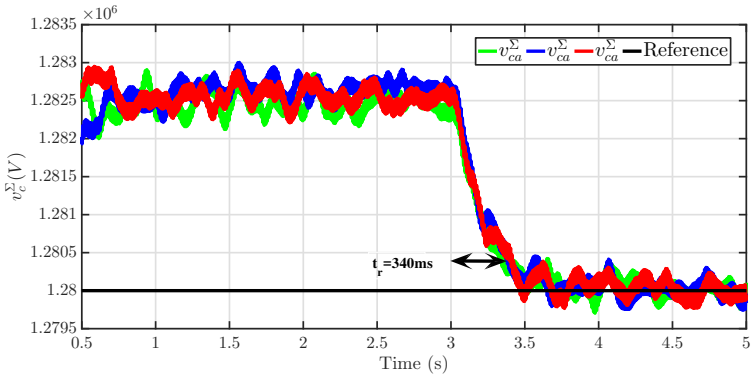

Figure 3.14: Response of the system when the controller is connected at the time instant of 3 seconds.

3.2 Output Current Controller during Grid Faults

In this section, a theoretical analysis of decomposition of a unbalanced system into balanced sequence components has been shown followed by a brief explanation of the Double Second Order generalised integrator(DSOGI) and Positive Negative Sequence Extraction(PNSE) method used for the PLL which is used to track and estimate the angle of the grid [28]. Then, a reference current injection strategy complying the grid codes is studied in detail for obtaining the correct reference for the output current under unbalanced condition.

3.2.1 Theoretical analysis of unbalanced system

According to the method of symmetrical components it can be stated that an unbalanced three phase system can be decomposed in a set of three symmetrical balanced system. These are known as positive, negative and zero sequence components as shown in Figure 3.15

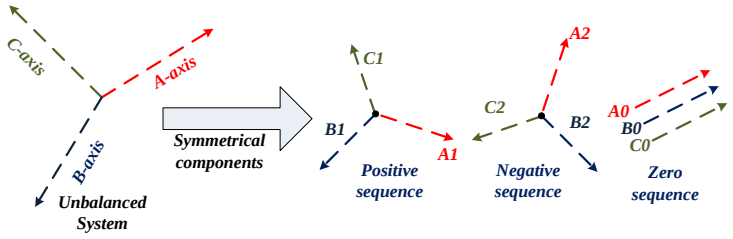

Figure 3.15: Decomposition of unbalanced system into symmetrical network components

$$v^{+}_{abc} = \left[T_{+}\right] v_{abc} \qquad \begin{bmatrix} v^{+}_{a} \\ v^{+}_{b} \\ v^{+}_{c} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$

$$v^{-}_{abc} = \left[T_{-}\right] v_{abc} \qquad \begin{bmatrix} v^{-}_{a} \\ v^{-}_{b} \\ v^{-}_{c} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$

$$v^{0}_{abc} = \left[T_{0}\right] v_{abc} \qquad \begin{bmatrix} v^{0}_{a} \\ v^{0}_{b} \\ v^{0}_{c} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$

the voltage equation for a three phase unbalanced system can be calculated as shown in Equation 3.29, by decomposing it into three symmetrical components and by applying necessary aforementioned transformations.

$$v_{abc} = v^{+}_{abc} + v^{-}_{abc} + v^{0}_{abc} \tag{3.29}$$

The operator $a = e^{(2\pi/3)}$ used in the transformations is a phase shifting term applied over the instantaneous input signals. The three balanced sequence components as shown in Figure 3.15 can be defined as positive-sequence component representing an anticlockwise rotating system displaced by 120° and the three phasors are equal in magnitude, negative-sequence defining a clockwise rotating system and the zero-sequence network as components having the same amplitude and phase. The zero sequence components are trapped by the use of transformer, this common mode term among the phases have been neglected and is not considered for the control purpose [29].

Under balanced conditions, the system only contains positive-sequence components, but during asymmetrical or grid faults negative sequence also appears in the

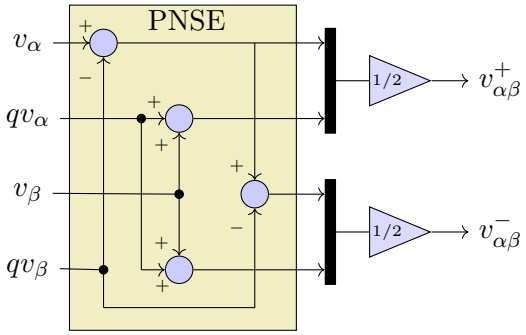

Figure 3.16: Block Diagram representation of PNSE.

grid voltages and thus Positive and Negative Sequence Extraction(PNSE) method is used as shown in Figure 3.16 in order to be able to have access to both the sequence components independently.

3.2.2 Double SOGI Positive Negative Sequence Extraction

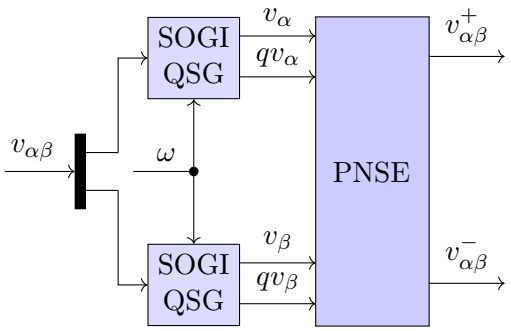

Figure 3.17: Block Diagram representation of DSOGI-PNSE.

Since during asymmetrical or grid faults, the presence of negative sequence components along with positive sequence compels using a double second order generalised integrator(DSOGI). In this strategy the positive- and negative-sequence are extracted using a DSOGI-PNSE in the $\alpha\beta$ stationary reference frame as shown in Figure 3.17. Thus, by Clarke transformations, the quadrature signals for the voltage components are calculated as shown below:

$$v_{\alpha\beta} = \left[T_{\alpha\beta}\right] v_{abc} \qquad \left[T_{\alpha\beta}\right] = \sqrt{\frac{1}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{3.30}$$

$$v^+_{\alpha\beta} = \left[T_{\alpha\beta}\right] v^+_{abc} = \left[T_{\alpha\beta}\right] \left[T_+\right] v_{abc} = \left[T_{\alpha\beta}\right] \left[T_+\right] \left[T_{\alpha\beta}\right]^T v_{\alpha\beta} = \frac{1}{2} \begin{bmatrix} 1 & -q \\ q & 1 \end{bmatrix} v_{\alpha\beta} \tag{3.31}$$

$$v^{-}_{\alpha\beta} = \left[T_{\alpha\beta}\right] v^{-}_{abc} = \left[T_{\alpha\beta}\right] \left[T_{-}\right] v_{abc} = \left[T_{\alpha\beta}\right] \left[T_{-}\right] \left[T_{\alpha\beta}\right]^{T} v_{\alpha\beta} = \frac{1}{2} \begin{bmatrix} 1 & q \\ -q & 1 \end{bmatrix} v_{\alpha\beta} \tag{3.32}$$

Since the SOGI-QSG behaves as a quadrature signal generator it is implemented as depicted below in Figure 3.18:

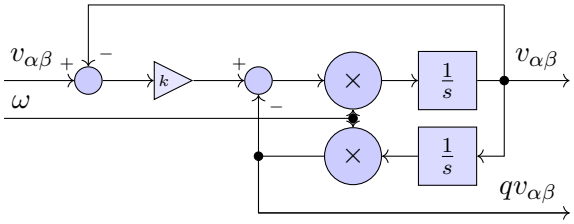

Figure 3.18: Block Diagram representation of SOGI-QSG.

where, $q = e^{-j\frac{\pi}{2}}$ represents a 90°-lagging phase-shifting operator. Finally, The extracted positive sequence voltage from SOGI-PNSE is used to feed the PLL for tracking the angle of the grid. Generally, a feed forward term with the fundamental AC frequency is added to achieve fast tracking of the phase angle.

Since the SOGI-QSG behaves as a quadrature signal generator it is implemented as depicted below. It is to be noted that the system dynamics for the SOGI-QSG are determined by the SOGI gain k as described in the following equations [29]:

$$\frac{v_{\alpha,\beta}{}'(s)}{v_{\alpha,\beta}(s)} = \frac{k\omega_1 s}{s^2 + k\omega_1 s + \omega_1^2} \tag{3.33}$$

$$\frac{qv_{\alpha,\beta}{}'(s)}{v_{\alpha,\beta}(s)} = \frac{k\omega_1^2}{s^2 + k\omega_1 s + \omega_1^2} \tag{3.34}$$

Analyzing the previous expressions it can be determined that if the grid frequency is properly estimated by the PLL and is aligned with the A-phase of the grid voltage, Equation 3.33 becomes unity inferring that the output signal will have the same amplitude and frequency. Similarly, based on Equation 3.34, the quadrature component will be 90° phase shifted and will have the same amplitude as the direct component which can be shown in Figure 3.19.

One of the advantages of using the SOGI is that it has an inherited filtering characteristic which attenuates the effect of the distorting high order harmonics. Since this quadrature signal generation method needs no decoupling network and since is dependent on the estimated frequency predicted by PLL, the DSOGI exhibits flexible adaptiveness during grid disturbances [29].

3.2.3 Reference Injection Strategy

Before understanding the concept of Reference Injection Strategy, it is very important to specify the reason why this Injection Strategy is needed. During unbalanced

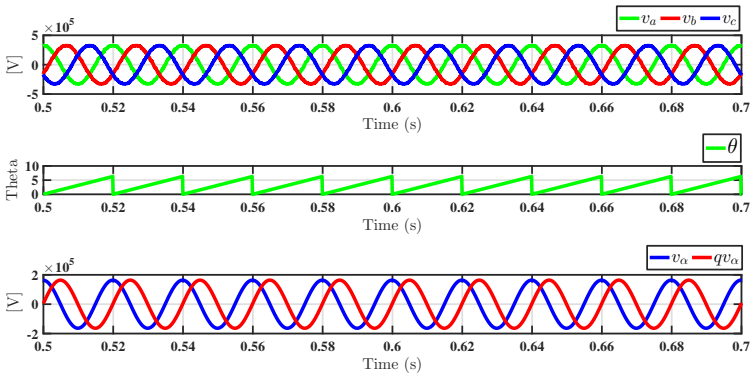

Figure 3.19: (a) Grid Voltages (b) Theta estimated by PLL (c) direct and quadrature voltage component obtained from SOGI-QSG in stationary reference frame.

or fault conditions the sagging of the grid voltage is one of the major issues giving rise to unbalanced grid voltages at the PCC of power converter.The interaction between injected currents and voltages during this period may give rise to uncontrolled oscillations in active and reactive power. One of the main objectives of the control is to provide constant arm voltages, as during unbalanced fault the presences of negative sequence component induces double frequency oscillations which are reflected on the DC-link voltage and output power. These ripples on the DC-link are directly associated with the energy variation in the DC-link capacitor, which is linked with the active power transfer. A sudden shutdown may induce major problems with oscillations on the grid side. Thus, it is important to keep the system running by balancing the injection of active and reactive power(according to the converter rating) fulfilling the LVRT requirement of the system. For the aforementioned reason, it is important to properly set the current reference injected to the grid by the converter to ensure no power oscillations. So according to the Grid Codes proposed in Germany it is advisable to inject the negative sequence current in order to fulfill the specific requirement along with the positive sequence current injection as shown in Figure 3.20. The objective of this positive-negative sequence reference block is to generate the correct reference current during grid faults [30]. The positive and negative reactive current to be injected complying the Grid Code is given by the formula:

$$i_q^+ = k_+ \cdot (0.9 - V_+) \tag{3.35}$$

$$i_q^- = -k_- \cdot (V_- - 0.05) \tag{3.36}$$

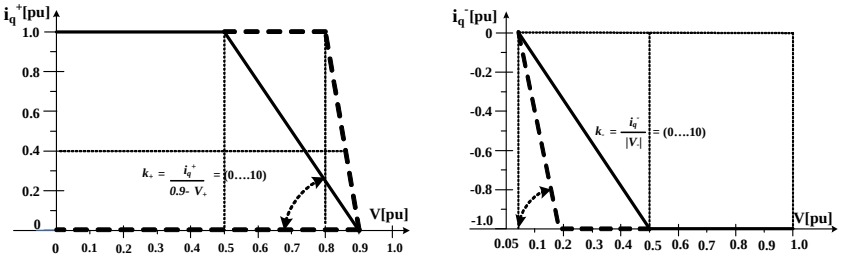

Figure 3.20: Positive and Negative reactive current injection according to Grid Codes

The mean values of the instantaneous active and reactive powers for a normal grid connected system can be expressed as:

$$p = P_o + P_{c2}cos(2\omega t) + P_{s2}sin(2\omega t) \tag{3.37}$$

$$q = Q_o + Q_{c2}cos(2\omega t) + Q_{s2}sin(2\omega t) \tag{3.38}$$

From Equation 3.37 and Equation 3.38 it can be observed that the power equations consist of dc terms i.e.(P_o and Q_o) and double fundamental frequency ac oscillatory terms as (P_{s2},P_{c2},Q_{s2} and Q_{c2}) due to the existence of negative sequence component. Since the unbalance of the capacitor voltages during faults is just associated with active power unbalance, Q_{s2} and Q_{c2} is intentionally kept to zero resulting in four degrees of freedom for the ac currents to be controlled [31]. The remaining power terms in form of matrix can be expressed as:

$$\begin{bmatrix} P \\ Q \\ P_{c2} \\ P_{s2} \end{bmatrix} = \frac{3}{2} \cdot A \begin{bmatrix} i_d^+ \\ i_q^+ \\ i_d^- \\ i_q^- \end{bmatrix} \tag{3.39}$$

where,

$$A = \begin{bmatrix} v_d^+ & v_q^+ & v_d^- & v_q^- \\ v_q^+ & -v_d^+ & v_q^- & -v_d^- \\ v_d^- & v_q^- & v_d^+ & v_q^+ \\ v_q^- & -v_d^- & -v_q^+ & v_d^+ \end{bmatrix} \tag{3.40}$$

where, v_d^+,v_q^+,i_d^+,i_q^+ are the dq components of positive sequence voltage and current. Similarly, v_d^-,v_q^-,i_d^-,i_q^- are the dq negative sequence current and voltages. All this quantities are calculated by means of Park transformation.

It can also be noted that the correct reference current signal needed by the output current controller during fault conditions can be obtained by controlling the four positive and negative d and q sequence current as shown in the above Equation 3.39

which can be expressed as:

$$\begin{bmatrix} i_d^+ \\ i_d^- \\ i_q^+ \\ i_q^- \end{bmatrix} = A^{-1} \cdot \frac{2}{3} \begin{bmatrix} P \\ Q \\ P_{c2} \\ P_{s2} \end{bmatrix} \tag{3.41}$$

As mentioned before since both the positive and negative sequence components have to be injected according to VDE-AR-N 4120:2015-01 technical requirement a Mixed positive and negative sequence injection method is chosen to be implemented for this project. The main advantage of using this method is that the double frequency oscillations in active power is reduced significantly.

From the generic instantaneous active power equation as shown below it can be seen that if the positive and negative sequence currents are not injected, the power injected into ac grid will no longer be constant and would result in ripple at twice the grid frequency.

$$p = v \cdot i \tag{3.42}$$

where, v and i can be decomposed into symmetrical voltage and current components and can be rewritten as

$$p = v^+ \cdot i_p^+ + v^- \cdot i_p^- + v^+ \cdot i_q^- + v^- \cdot i_q^+ = P_o + \widetilde{p_o} \tag{3.43}$$

Mixed Sequence Injection:

The main reason of this strategy is to inject negative sequence component of reactive current(i_q^-) in order to reduce the oscillations in the power which is injected to the grid side, positive sequence component of reactive current(i_q^+) according to the LVRT requirement, and the positive sequence component of active current(i_p^+) for maintaining voltages through the grid,thus ensuring the stability of the system. If the negative sequence of the grid currents is not controlled, the power(P) injected into ac grid is not constant and has oscillations at twice the grid frequency resulting in unbalanced circulating currents in turn resulting in unbalance in the capacitor voltages. It can be noted from the above Equation 3.41 that the positive and negative sequence reactive currents cannot be controlled as they have to be injected according to the requirement as directed in the grid code, thus resulting in just two degrees of freedom(positive and negative active currents) i.e.(i_p^+ and i_p^- in FPNSC strategy)or (i_d^+ and i_d^- in rotational dq frame) [29].

$$v^+ \cdot i_p^+ + v^- \cdot i_p^- = P \tag{3.44}$$

$$v^+ \cdot i_p^- + v^- \cdot i_p^+ = 0$$

$$v^+ \cdot i_p^- = -i_p^+ \cdot v^-$$

$$| v^+ |^2 \cdot i_p^- = -v^+ \cdot i_p^+ \cdot v^-$$

$$i_p^- = \frac{-v^+ \cdot i_p^+ \cdot v^-}{\mid v^+ \mid^2} \tag{3.45}$$

Substituting Equation 3.45 in Equation 3.44 and with further mathematical calculations, positive and negative sequence active currents can be calculated as follows:

$$i_p^+ = \frac{P}{\mid v^+ \mid^2 - \mid v^- \mid^2} \cdot v^+ \tag{3.46}$$

$$i_p^- = \frac{P}{\mid v^+ \mid^2 - \mid v^- \mid^2} \cdot -v^- \tag{3.47}$$

Thus by adding Equation 3.46 and Equation 3.47, i_p^* can be obtained.

$$i_p^* = i_p^+ + i_p^- \tag{3.48}$$

Thus,

$$i_p^* = P \left[\frac{v^+ - v^-}{\mid v^+ \mid^2 - \mid v^- \mid^2} \right]$$

The calculation for the reactive currents cannot be carried out in the same way as it was done for the active currents as in this case the oscillatory terms in the reactive power is not equal to 0, which means two unknown terms have to be calculated from one equation which is not possible. Hence, by using the generic equation for FPNSC and substituting droop factor terms i.e(k_1 and k_2) in the equation, reactive currents can be calculated as:

$$i^* = P \left[\frac{k_1 \cdot v^+ \cdot}{\mid v^+ \mid^2} + \frac{(1-k_1) \cdot v^-}{\mid v^- \mid^2} \right] + Q \left[\frac{k_2 \cdot v_\perp^+}{\mid v^+ \mid^2} + \frac{(1-k_2) \cdot v_\perp^-}{\mid v^- \mid^2} \right] \tag{3.49}$$

$$i_q^+ = \frac{Q}{\mid v^+ \mid^2 + \mid v^- \mid^2} \cdot v_\perp^+ \tag{3.50}$$

$$i_q^- = \frac{Q}{\mid v^+ \mid^2 + \mid v^- \mid^2} \cdot v_\perp^- \tag{3.51}$$

Thus from the above equations, i^* results in:

$$i^* = i_p^\star + i_q^* \tag{3.52}$$

$$i^* = P \left[\frac{v^+ - v^-}{\mid v^+ \mid^2 + \mid v^- \mid^2} \right] + Q \left[\frac{v_\perp^+ + v_\perp^-}{\mid v^+ \mid^2 + \mid v^- \mid^2} \right] \tag{3.53}$$

By monitoring the droop factors, the positive and negative sequence components can be regulated according to the grid code requirement, ensuring a balanced and stabilized system and make the total power delivered to the grid equal to the rated power. After the theoretical analysis of the reference injection strategy, simulations were carried out to verify the reduction in power oscillations with Mixed sequence injection. The simulations were done with a SLG fault on the grid side for $200ms$ at

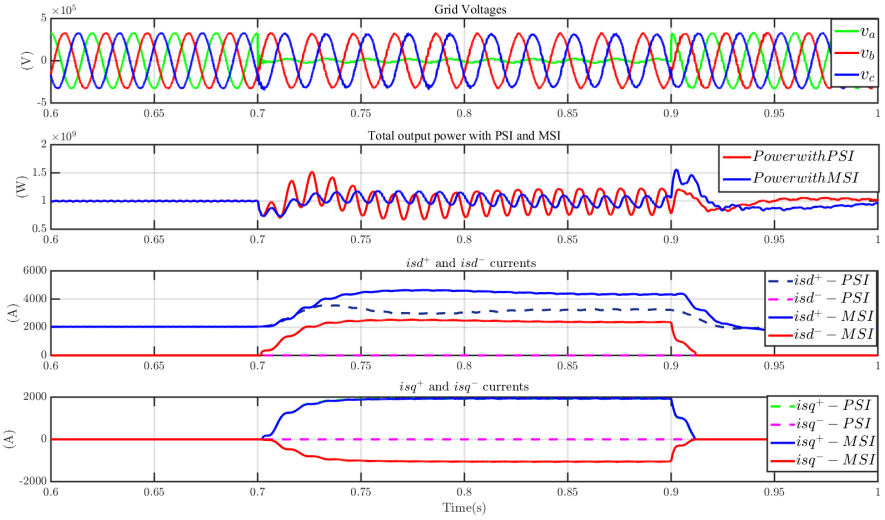

Figure 3.21: (a) Grid voltages (b) Total power with PSI and MSI injection (c) Positive and Negative sequence active currents (d) Positive and Negative sequence reactive currents

a time instant of 0.7s as shown in Figure 3.21. By looking at Figure 3.21, it can be seen that the power oscillations are reduced with MSI resulting in a constant v_dc. Hence it can be concluded that by implementation of Mixed sequence injection i.e when both positive and negative sequence components of active and reactive current are injected ensuring successful LVRT with reduced oscillations in P assuring good overall system performance.

3.3 Injection of Second Harmonics in the Circulating current

This section focuses on an cost effective approach of reducing the capacitor voltage ripple. A strategy of injecting an AC second harmonic component in the circulating current is proposed to ensure the reduction of energy variation between the upper and lower arm.

3.3.1 Minimization of Energy Variation in the Leg

The power in the leg of a MMC should have a zero average value over one fundamental cycle in order to keep the capacitor average voltages constant, implying that the entire power from the DC bus is transferred to the AC bus within one cycle. However, considering the leg power equation from Equation 2.23, it is observed that in order to obtain a zero average power, the two DC terms have to be equal, ensuring the

balance between the DC and AC average power [32].

$$I_{c0m} = \frac{\hat{V}_{sm}\hat{I}_{sm}}{2 \cdot v_d} \tag{3.54}$$

As stated in Equation 2.23, the instantaneous leg power is composed of three terms, where the first two refers to the DC and AC active power components per phase respectively and the third term represents an instantaneous oscillating power component with the second harmonic ($\frac{\hat{V}_s\hat{I}_s}{2}\cos(2\omega t - \phi_i)$), which needs to be canceled out for Equation 2.23 to be zero. This can be achieved by injecting an alternating current with negative sequence to the reference of the circulating current control as shown in Fig.Figure 3.22 [33].

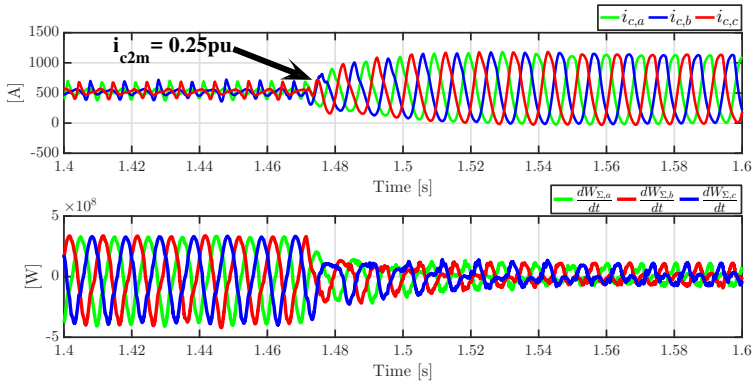

Figure 3.22: (a) Circulating Current (b) Instantaneous leg Power.

The generic form of the injected negative sequence current can be expressed as:

$$i_{c2m} = \hat{I}^{-}_{c2m} cos(2\omega_1 t + \frac{2\pi(m-1)}{3} - \phi^{-}_{c2}) \tag{3.55}$$

Thus, the total circulating current will be:

$$i_{cm} = I_{c0m} + i_{c2m} \tag{3.56}$$

Substituting Equation 3.56 in Equation 2.23 and solving for $\hat{I}^{-}_{c2m}$ yields to:

$$\begin{aligned}\frac{dW_\Sigma}{dt} &= 2 \cdot v_c I_{c0m} + 2 \cdot v_c \hat{I}^{-}_{c2m} cos(2\omega_1 t + \frac{2\pi(m-1)}{3} - \phi^{-}_{c2}) \\ &- [\frac{\hat{V}_{sm}\hat{I}_{sm}}{2} cos\phi_i + \frac{\hat{V}_{sm}\hat{I}_{sm}}{2} cos(2\omega_1 t + \frac{2\pi(m-1)}{3} - \phi_i)]\end{aligned} \tag{3.57}$$

$$\hat{I}^{-}_{c2m} = \frac{\hat{V}_{sm}\hat{I}_{sm} cos(2\omega_1 t + \frac{2\pi(m-1)}{3} - \phi_i)}{2 \cdot v_c cos(2\omega_1 t + \frac{2\pi(m-1)}{3} - \phi^{-}_{c2})} \tag{3.58}$$

In order to eliminate the second order harmonic terms and have an amplitude of $\hat{I}^{-}_{c2m}$ constant, the injected second harmonic signal angle is chosen to be equal to the load angle (ϕ_i=ϕ^{-}_{c2}), resulting in:

$$\hat{I}^{-}_{c2m} = \frac{\hat{V}_{sm}\hat{I}_{sm}}{2 \cdot v_d} \tag{3.59}$$

The effect of the injected negative sequence current can also be seen in the sum capacitor voltage ripple. Substituting Equation 3.56 in Equation 2.24, and with mathematical manipulations shown below, it can be observed that the magnitude of the fundamental component of $v_c^{\triangle}$ is reduced as expressed in Equation 2.28:

$$\begin{aligned}\frac{dW_{\triangle}}{dt} = v_c \cdot \left\{\hat{I}_{sm}cos(\omega_1 t - \frac{2\pi(m-1)}{3} - \phi_i)\right\} - 2 \cdot \hat{V}_{sm} \cdot I_{cm}cos(\omega_1 t - \frac{2\pi(m-1)}{3}) \\ - \hat{V}_{sm} \cdot \hat{I}^{-}_{c2m}cos(3\omega_1 t - \phi^{-}_{c2}) - \hat{V}_{sm} \cdot \hat{I}^{-}_{c2m}cos(\omega_1 t - \frac{2\pi(m-1)}{3} - \phi^{-}_{c2})\end{aligned} \tag{3.60}$$

Thus, on further integration of Equation 3.60 energy imbalance equation can be obtained as:

$$W_{\triangle} = W_{\triangle 0} + \triangle W_{\triangle} \tag{3.61}$$

Choosing (ϕ_i=ϕ^{-}_{c2}) as above and from the aforementioned equation of (3.61), information about $\triangle W_{\triangle}$ can be extracted as expressed below:

$$\triangle W_{\triangle} = \left\{\frac{v_d \cdot \hat{I}_{sm}}{2\omega_1} - \frac{\hat{V}_{sm} \cdot \hat{V}_{sm} \cdot \hat{I}_{sm}}{\omega_1 \cdot v_d} - \frac{\hat{V}_{sm} \cdot \hat{V}_{sm} \cdot \hat{I}_{sm}}{2\omega_1 \cdot v_d}\right\}\left\{sin(\omega_1 t - \frac{2\pi(m-1)}{3})\right\} \tag{3.62}$$

The ripple equation for the upper and lower arm capacitor voltages can be given by:

$$\Delta v^{\Sigma}_{cu} = \frac{N}{2Cv_d}(\Delta W_{\Sigma} + \Delta W_{\Delta}) \tag{3.63}$$

$$\Delta v^{\Sigma}_{cl} = \frac{N}{2Cv_d}(\Delta W_{\Sigma} - \Delta W_{\Delta}) \tag{3.64}$$

Since, $\triangle W_{\triangle}$ is directly proportional to $\Delta v^{\Sigma}_{cu,l}$ as seen in Equation 3.63 and Equation 3.64, it can be concluded that the injected second harmonic signal is not only useful in eliminating the double frequency oscillating term from the leg power, but also is able to reduce the capacitor voltage ripple.

A simulation model of the converter topology presented in Figure 2.1 with the parameters shown in Table 2.1 is built in PLECS in order to validate the above presented mathematical analysis. The effect of the suppression of the AC components from the circulating current are presented in Figure 3.23(b).

It is to be noted that the amplitude of second harmonic injected current as shown in Equation 3.59 and assuming $\hat{V}_{sm} = \frac{v_d}{2}$ is around 0.25 times the peak value of output current($\hat{I}_{sm}$) which is considered to be the optimum injected current. Relating ($\hat{I}_{sm}$)

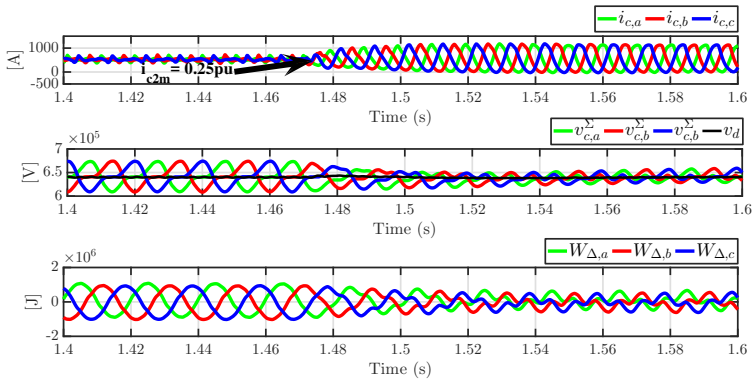

Figure 3.23: (a) Circulating Current (b) Upper arm capacitor voltages (c) Leg energy difference.

with respect to i_c, it can be seen from Fig.3.25 and from mathematical calculations based on Equation 2.2 and Equation 2.3 that with the injected i_{c2m}, the rms value of the arm currents increases by 7% of the peak output current i.e from $0.40pu$ to $0.47pu$ which can be validated in Figure 3.24.

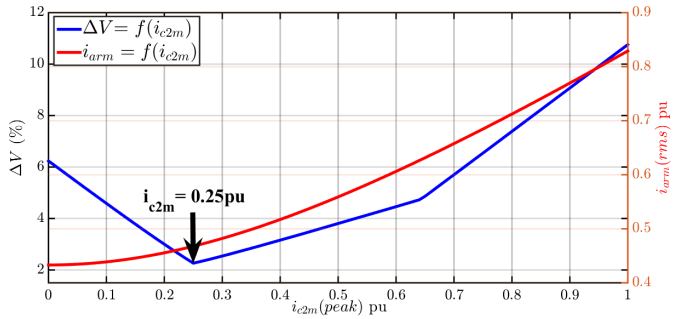

Figure 3.24: Voltage ripple and arm currents as a function of (i_{c2m})

This results in a minor increase in the stress and rating of the switches in the submodules due to an increase in the conduction losses, thus inferring an increase in the operational cost and decrease in efficiency. From Equation 3.65 it can be noted that by injecting a circulating current equivalent to $0.25pu$ of peak output current the second harmonic component term i.e (ΔW_{Σ}) from Equation 3.63 and Equation 3.64 can be eliminated inferring that the $50Hz$ ripple in the cell capacitors only depends on ΔW_{Δ}.

Thus, voltage ripple as function of the injected circulating current can be expressed as:

$$\Delta V = \frac{N}{Cv_d} \cdot \frac{v_d \hat{I}_s}{2\omega}[(X - 0.25)sin(2\omega t) + (0.5 - X)sin(\omega t) + \frac{X}{3}sin(3\omega t)] \quad (3.65)$$

where,

$$i_{c2m} = X \cdot \hat{I}_s \quad (0 < X \leq 0.25)$$

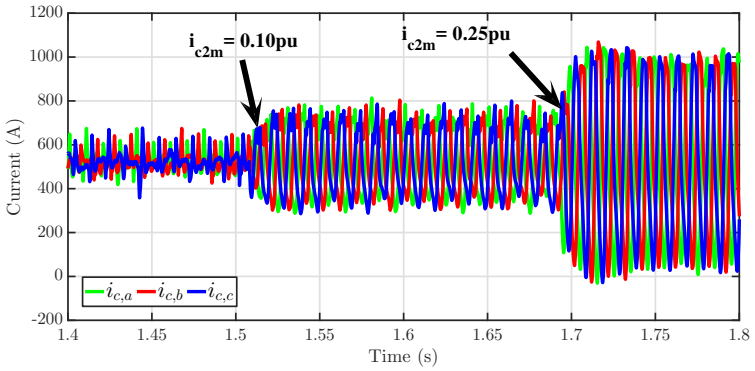

Figure 3.25: Circulating current with and without injection of (i_{c2m}).

From the above proposed conjecture, the minimization of the energy variation and reduction in the voltage ripple of cell capacitors can be done as showcased in Figure 3.27. This makes possible more reduction in the capacitance value which could prove to be size and cost effective. A graph displaying voltage ripple as a function of capacitance can be seen in Figure 3.26 where the system was designed for 5% of voltage ripple as a common design requirement.

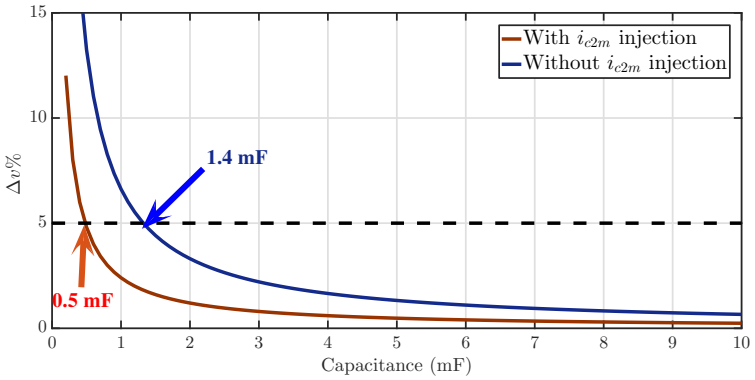

Figure 3.26: Voltage ripple as a function of capacitance.

Thus from the above information, an optimum solution can be obtained taking into consideration the voltage ripple as a function of efficiency i.e. (injection of i_{c2m}) on one hand and capacitor cost and size on the other.

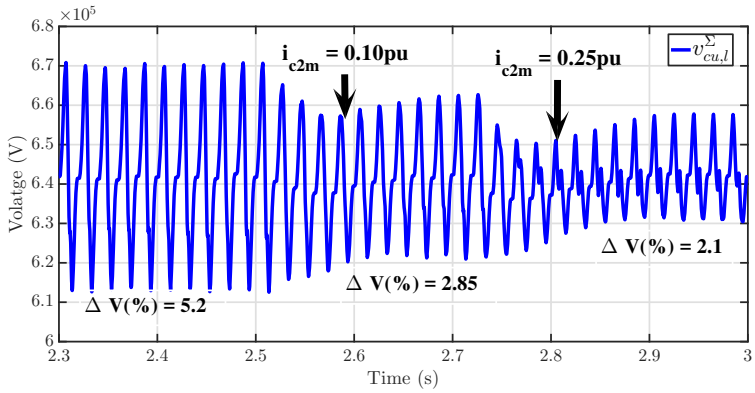

Figure 3.27: Capacitor voltages showcasing ripple with and without (i_{c2m}).

Summary

In this chapter control under unbalance conditions has been developed. Internally in the MMC, unequal energy stored in each arm is considered as unbalance where two controllers are proposed. In each leg the analytical study of the energy exchange between arms is proposed and a controller is shown which allows to avoid unequal energy storage among them. Moreover, a controller is developed which is able to control the total energy stored in each phase of the converter.

Study of the output current injection under grid faults is described. Theoretical analysis of the Mixed Sequence reference injection strategy complying with the grid codes is also presented.

Finally, a systematic approach has been introduced for the effective reduction of the sum capacitor voltage ripple in an MMC application. The injection of a second order harmonic component in the circulating current was proven to be capable of reducing the total capacitor ripple resulting in an reduction in the size of the capacitors by 33% of its initial value in MMC-HVDC.

Chapter 4

Hardware Setup Design

This chapter focuses on the design procedure for developing a laboratory prototype which is used for the thesis for experimental validation.

4.1 MMC prototype overview and prerequisites

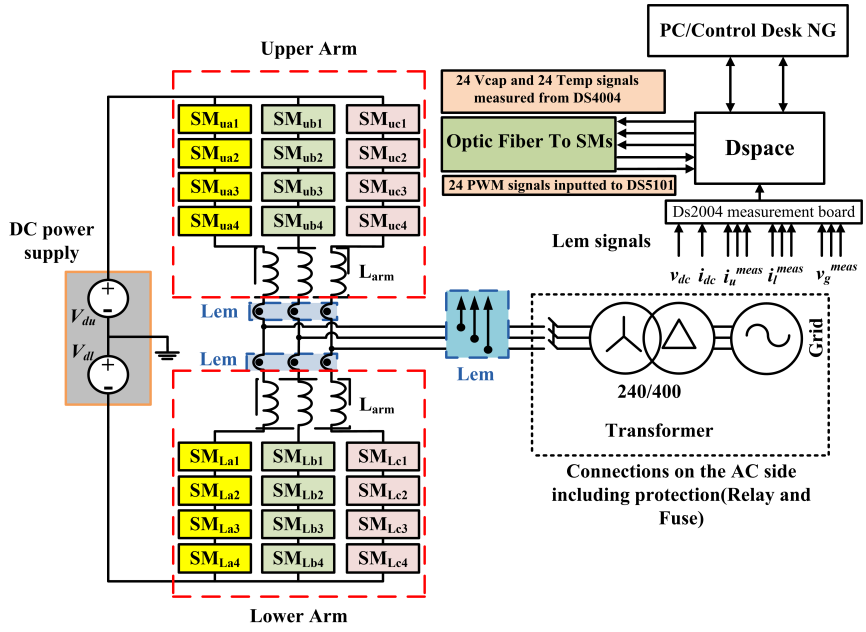

Figure 4.1: MMC Lab Schematic

Figure 4.1 shows a three phase lab schematic of the built hardware. The hardware consists of a three phase system with 4 submodules per arm with a pole-to pole dc link voltage of $400V$. Each submodule board is aligned with a capacitor board which has four capacitors in parallel with 10% tolerance and overall rating of $3.6mF$. Each

Parameters	Notation	Value
P(kW)	Active Power	2.6
N_{arm}	Submodules/arm	4
V_{dc}(V)	Direct voltage	400
C_{sm}(mF)	Capacitance	3.6
L_{arm}(mH)	Arm Inductance	20
V_g(kV)(l-l)rms	Alternating voltage	230
f(Hz)	Rated frequency	50
fs(Hz)	Sampling frequency	10000
i_s(A)rms	Output rated current	6.4

Table 4.1: Simulated Parameters of MMC prototype

arm consists of a specially designed company manufactured arm inductors rated at $15mH$. Several tests were carried out in order to declare the built hardware setup functional and ready for verifying the simulation results. It is to be noted that the design of submodule boards as well as the interface boards used for this hardware setup were already designed. The lab parametric table for which the MMC prototype has been designed to carry out experimental results which will be shown in the next chapter is shown in chapter 5. Other prerequisites for the setup are:

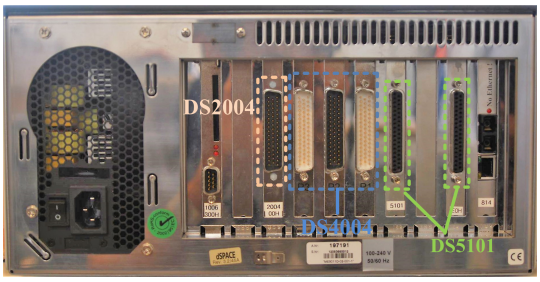

Figure 4.2: Dspace with necessary interface connections

- $5V$ power supply to fed the submodule boards.
- Star-Delta transformer rated at 2.5kVA for galvanic isolation with input:3 $\times$ 230V and output:3 $\times$ 400V
- AC power supply from California Instruments(MX-30) which acts as a grid simulator.
- LEM measurement box consisting of voltage transducers(LV 25-P) and current sensors(LA 25-P)with bandwidth of $DC-200kHz$ for measuring arm currents, DC voltage, input dc current and output voltage.
- DS5101 interface cards for generating and sending the PWM signals to the

submodule boards and DS4004 interface cards for capacitor voltage and temperature measurements.

- DS2004 analogue to digital measurement board for measuring the signals from LEM box with resolution frequency of 50ns and 16 multiplexed channels.
- PC equipped with dSPACE and Control Desk interface for a centralized control connected by means of optic fiber to every SM.

A step by step design procedure of arm inductors, submodule capacitors and all the necessary information right from the hardware to the software will be presented to make this setup functional will be presented in the subsequent subsections.

4.2 Submodule and Component Description used in the setup

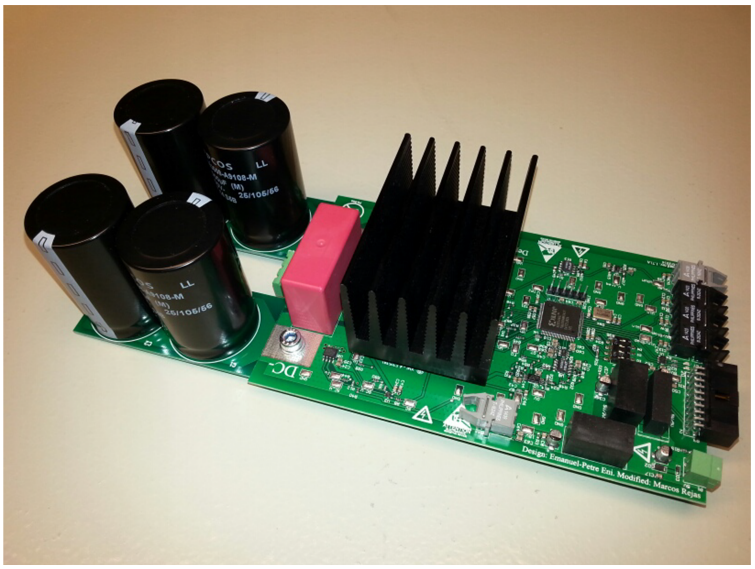

Figure 4.3: Submodule board design

The submodule board as shown in Figure 4.3 consist of a 3 phase intelligent power modules(IPM) rated at 600V/15A with thermal sensors for the semiconductors temperature measurement. The design of submodule board includes blanking time generated module, capacitor voltage measurement along with overcurrent, overvoltage and overtemperature protection in order to condition the signals and avoid any damage.

The board consists of 1 PWM input for each of the 3 Legs(A,B,C). These inputs are used for generating the High and Low sides PWM for each leg with the required $1.25\mu s$ blanking time. After the conditioning of the PWM, it outputs 6 PWM signals,

1 for each switch in the 3 legs. The operation status is signaled by means of 2 LEDs. The board also contains a 4 WAY DIP switch which can be used for the selection of different operation modes. All of the logic circuits are implemented in a Xilinx XC95144XL CPLD with an input clock of 35MHz. The task of the CPLD is to receive the PWM signals from the dSPACE system and generate those received PWM signals for the IPM module with the desired deadtime as mentioned above. It also receives the enable/reset signal from the dSPACE along with the fault signals and stops generating the PWM signals in case of a fault.

4.3 Design of Arm Inductors

Figure 4.4: Inductor for the laboratory prototype

The arm inductor L_{arm} functions as a filter to attenuate the high-frequency harmonics in the arm current. The sizing of the arm inductor depends on the filtering needs and the short-circuit current limit. Due to the series connections as shown in Figure 2.1, the inductors can provide protection in case of both external and internal faults, thus preventing damage to the switching devices.

The arm inductor design is generally carried out based on three possible criteria:

- Reduction of peak value of the circulating current.
- To limit the current rise rate($\frac{\mathrm{d}i}{\mathrm{d}t}$) during faults.
- To mitigate the current ripple

Since for this thesis, a specific controller has been designed to mitigate the circulating current as shown in Figure 2.7. The arm inductors were designed based on limiting the current rise rate during faults and to reduce the current ripple. One of the disadvantages for this approach is that during low voltage application there is a huge voltage drop which might possibly affect the converter efficiency. The analytical explanation of the arm inductor design based on the circulating current mitigation is well explained in [11].

Generally, the arm inductors that limit the fault current rise-rate are selected for the most critical case : DC-link short circuit. The fault current in this case flows through the semiconductor devices and the converter can be damaged if the fault current is not limited to a tolerant level. In order to simplify the analysis, the voltages over the SMs capacitors can be assumed to be constant. At the time of the fault, the voltage across the inserted capacitors will be equal to v_d. Applying Kirchhoff's voltage law at the output point of the leg, the voltage drop across the upper and lower arm inductors is:

$$L\frac{\mathrm{d}i_u}{\mathrm{d}t} + L\frac{\mathrm{d}i_l}{\mathrm{d}t} - v_d = 0 \tag{4.1}$$

After the fault, and once the converter starts operating in steady state condition the upper and the lower arm currents can be considered to be equal, so the fault current rise rate(α) can be defined as:

$$\alpha = \frac{v_d}{2L} \quad i_u = i_l$$

So depending on the rise rate of the fault current during designing of the converter and based on the application, the arm inductor can be designed accordingly which can be expressed as:

$$L = \frac{v_d}{2\alpha} \tag{4.2}$$

Another approach of designing arm inductors is based on the current ripple and is described with the equations mentioned below:

$$L = \frac{0.25 \cdot T_m}{\Delta i_{umax}} \cdot \frac{V_c}{N_{arm}} \tag{4.3}$$

where,

$$\Delta i_{umax} = \epsilon_1 \cdot i_{umax} \qquad \text{and} \qquad i_{umax} = \frac{P_a}{3 \cdot v_d} + \frac{\sqrt{2}\hat{i}_s(rms)}{2}$$

Considering the current ripple to be 15% and modulation period of $1e^{-3}$ with basic sorting the arm inductor can be calculated as shown in Equation 4.3:

$$(\frac{100}{4}) \cdot (\frac{0.25}{4.5}) \cdot (1 \times 10^{-3}) = 2mH \tag{4.4}$$

Thus, based on their ability to limit the rise rate of the fault current and setting the limit of maximum allowable current ripple, the arm inductors were installed with the value of 10mH based on the commercial availability as shown in Figure 4.4.

Test measuring the arm inductance and resistance is important as they play a vital role in proper tuning of the output and circulating current control. AC and DC test were performed to check charging of the capacitors in each submodule and their voltages according to the input supply from the power source. The voltages in the capacitors were measured. From the conducted test, the measured arm inductance and resistance can be shown below in Figure 4.5. The performed tests were:

- Test measuring the arm inductance and resistance
- DC and AC test measuring the capacitor voltages

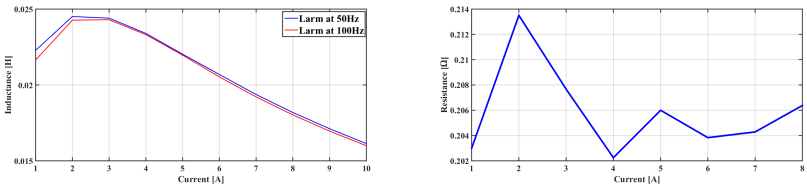

Figure 4.5: (a) Measured Inductance at 50/100Hz (b) Measured Arm resistance

4.4 Design of submodule Capacitance

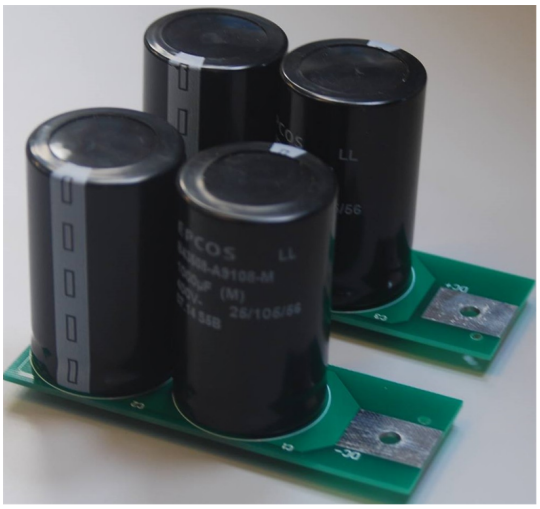

Figure 4.6: Designed capacitor for the laboratory prototype

The main goal of this analysis is to provide a more laconic understanding of how the dimensioning of the submodule capacitors will be valuable for evaluating the operating limits of the converter. Another criterion for the capacitor dimensioning is the DC-link support. Since the DC link capacitor is replaced by the submodule capacitors, they have to be designed to support the stability of the DC-link and transients during faults. This translates into voltage ripple across the capacitors. Thus, sub-module capacitance is designed to suppress the voltage fluctuation as when the sub-module is in the inserted mode, arm currents flow through the capacitor causing the voltage fluctuations.

One of the approach is described in [34] and another approach can be considered while designing the submodule capacitor based on the energy storage requirement

[35]. From the per-phase circuit and all dynamical equations of MMC shown in aforementioned Figure 2.2 and section 2.1, the nominal energy stored in the capacitor of a submodule can be given by:

$$W_{sm} = \frac{1}{2} \cdot C_{sm} \cdot V_{sm}^2 \tag{4.5}$$

where, V_{sm} neglecting any capacitor ripple and assuming that the circulating current equals the direct current can be expressed as:

$$V_{sm} = \frac{v_d}{N_{arm}} \tag{4.6}$$

Generally, total energy storage of the system can be calculated with the below shown formula:

$$W_{total} = \frac{1}{2} \cdot C \cdot V_{sm}^2 \cdot N_c \tag{4.7}$$

where N_c is the total number of capacitors and can be calculated from number of submodules in arm and (M) are number of phases.

$$N_c = N_{arm} \cdot M \cdot 2 \tag{4.8}$$

Practically, the voltages in the submodule varies with time depending on the current direction and charging/discharging of the capacitors. The maximum voltage in the submodule should never exceed the rated limit and in order to specify the upper limit of the instantaneous capacitor voltage value a constant k_{ul} proportional to the maximum allowable voltage ripple(ϵ) has been considered where,

$$v_{caps(u,l)}^i \leq k_{ul} \cdot \frac{v_d}{N_{arm}} \tag{4.9}$$

where, $v_{caps(u,l)}^i$ is the capacitor voltage in i_{th} submodule. Now combining Equation 4.5 and Equation 4.9 gives:

$$W_{caps(u,l)}^i \leq \frac{1}{2} C \cdot (\frac{v_d \cdot k_{ul}}{N_{arm}})^2 \tag{4.10}$$

Thus, from Equation 4.10 the maximum energy that can be stored in each arm without exceeding the rated limit is:

$$W_{max} = \frac{{v_d}^2}{2N_{arm}} \cdot k_{ul}^2 \cdot C \tag{4.11}$$

Assuming N_{arm} submodules per arm in the converter, the energy change in one submodule can be expressed as:

$$\Delta W = \frac{2}{3} \cdot \frac{P_a}{m \cdot \omega_0 \cdot N_{arm}} (1 - (\frac{m \cos \phi}{2})^2)^{\frac{3}{2}} \tag{4.12}$$

where,

$$m = \frac{\hat{V}_s}{\frac{v_d}{2}}$$

Theoretically, from Equation 4.12 the maximum calculated energy deviation that can be stored in a converter arm can be expressed as:

$$\triangle W_{max} = \frac{2}{3} \cdot \frac{P_a}{\omega_0} \tag{4.13}$$

Finally, from aforementioned calculations and Equation 4.13 the minimum value of submodule capacitance can be given as:

$$C_{min} = \frac{2N_{arm} \cdot \triangle W_{max}}{(v_d \cdot \epsilon)^2} \tag{4.14}$$

Similarly, based on the above Equation 4.13 and Equation 4.14 and considering $\epsilon = 10\%$ the submodule capacitance is calculated to be 1.8mF. Since, MMC is preferred for high power applications, a perfect capacitance design is difficult to be designed for low power applications with the aforementioned numerical approach and hence to reduce the voltage fluctuations and available commercial design, the capacitor was chosen to be 4mF as shown in Figure 4.6.

After the design of submodule board and hardware was build as shown in Figure 4.1 and making sure that the connections were done properly the submodules were supplied from a common 5V power supply. Several open loop tests were also performed to check the functionality of the system.

4.5 Synchronization of Hardware design with Software

After checking the functionality of the hardware, optic fibers were prepared which were used for transmitting/receiving data from the dSPACE. PWM signals were generated using 2 DS5101 interface boards(master and slave) which generates the PWM signals for the IPM's and as mentioned above DS4004 interface boards are used for sensing the capacitor voltages and temperature of the semiconductor device. Two reset boards were also made for fault signal detection and also from the objective that all the submodules start from the same state before system execution and implementation. The essential files described below are very important for proper execution and synchronizing the parameters of the simulation model with the hardware for experimental validation.

- Sfcn.c file: It contains the information related with the connectivity between the Simulink model and the DWO code such as number of inputs as well as their initialization and declaration, interruption configuration, functions to update the signals value, flag declaration. There should be one sfcn file for master and slave cards DS5101 interface cards.

- DWO file: Interrupt signals as well as board synchronization are generated through DWO programming. The implementation of a DWO application starts with writing of the DWO program itself. Compilation of the DWO application source file (.src) by using the DWO compiler DWOCOMP results in a C source file(.c) and a related header file(.h). The C file contains the encoded DWO object code and a load routine for downloading the object code to the DS5101 by a master DSP. The interruption is also programmed in the DWO code. Once again there should be one DWO.src file for master and slave cards DS5101 interface cards.

- RTI Data: This block in the Simulink is used by RTI to store internal model dependent data.

- In order to receive a interrupt it has to be acknowledged when transmitted. This is implemented in a s-function triggered by the hardware interrupt block and after receiving the interruption, execution is implemented as indicated in S-function name, where the steps for further execution are mentioned after the generation of an interruption. Moreover, in the Simulink model the period for each signal should be generated and sent to a block in charge of connecting with the DWO code previously generated.

- Control Desk: Finally,the created model in Simulink is built in order to transfer the information to the dSPACE. After implementing the desired generated PWM's with DS5101 dSPACE board a communication is required for debugging the system and for much easy implementation. Control Desk is used for this specific task. With the help of Control Desk, the built model can be validated and also the parameters can be varied/changed without troubling the Simulink Model. Having Control Desk ensures better and fast functioning of the system.

The Figure 4.7 shown below are the two phase output converter voltages with 5 levels with a DC supply of 200V.

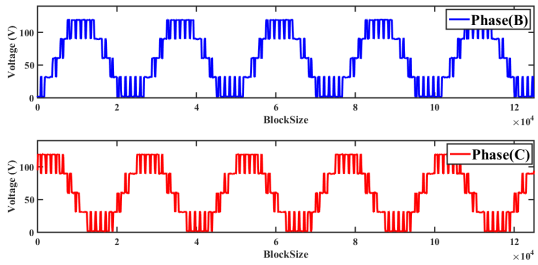

Figure 4.7: Converter voltages: Phase-B and Phase-C

Since the implementation of NLC technique is very much dependent on the current and its direction, it is of utmost importance to make sure that the current

measurement box senses/measures the correct value, so that correct values are inputted on the Control Desk by the DS2004 measurement board. Before running the NLC technique, proper calibration of the current measurement boxes were ensured with proper tuning of gains and offset.

Before implementing the control, the next step was to determine to make sure that the dSPACE board was able to generate the PWM signals properly to the IPM in the submodule. The implemented technique for this thesis is NLC with variants Basic Sorting, CTB and RSS.

Chapter 5

Experimental Results

After all the theoretical analysis and simulations shown for the designed output and internal controllers in subsection 2.3.3 and subsection 2.3.5, this chapter focuses on the obtained experimental results with the simulated parameters as shown in Table 5.1, which were taken on the built prototype to validate the obtained simulation results. Due to some limitations of the prototype as described in section 1.5, the energy controllers could not be implemented by the time the report had to be delivered. Full experimental results of the energy balancing controllers will be later presented in a supplement.

5.0.1 Grid Voltages and alignment of PLL

Before implementing the designed controllers, it is important to check if the angle of the implemented PLL is properly aligned with the phase-A output voltage as it gives the correct reference to all the transformations used for designing the controllers. Hence the measured grid voltages where phase A voltage is aligned with the PLL is shown below in Figure 5.1:

Parameters	**Notation**	**Value**
P(W)	Active Power	700
N_{arm}	Submodules/arm	4
V_{dc}(V)	Direct voltage	200
C_{sm}(mF)	Capacitance	3.6
L_{arm}(mH)	Arm Inductance	20
V_g(V)(l-g)rms	Alternating voltage	70.3
f(Hz)	Rated frequency	50
fs(Hz)	Sampling frequency	10000
$f_{sw}(Hz)$	Equivalent switching frequency	320

Table 5.1: Plant Parameters for experimental validation

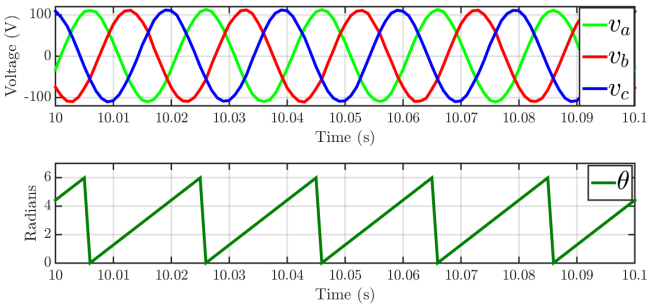

Figure 5.1: Measured grid voltages with aligned θ

5.0.2 Output current control

After verifying that the system is ready for implementing controllers, output current controller has been implemented to make sure that the reference(v_s^*) is correctly given for providing the correct gate signals to the switching devices. Another aspect is to validate the step response and functioning of the implemented design. The response of the measured i_d can be shown in Figure 5.2 with a rise time of 0.002s when a step of 1.5A is given in the reference.

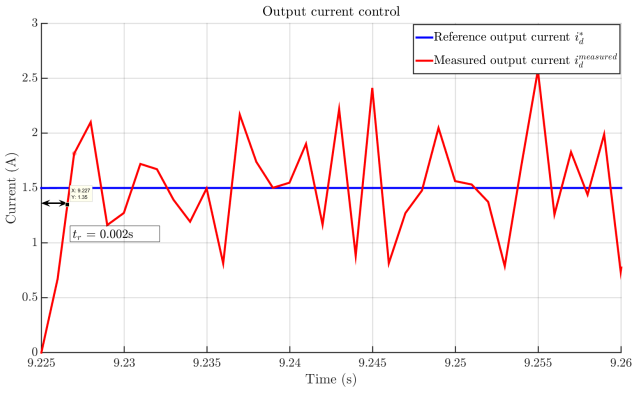

Figure 5.2: Reference and measured output i_d current with a t_r of 0.002s

5.0.3 Circulating current Control

As aforementioned, the circulating current is the current flowing through the three phases of the leg of MMC without flowing through the load. It is originated due to the imbalance between the voltages of the submodules in both arms. Circulating current basically contains an DC component which provides the power transfer from the DC to AC side and a second harmonic plus some minor components created by the multiples of the switching frequency [11]. The circulating current does not affect the output voltages and currents, but if not controlled they increase the peak and

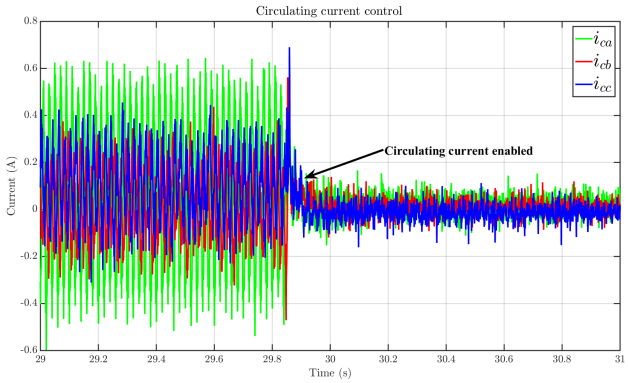

Figure 5.3: Circulating current when the control is enabled at time instant of 29.8s

rms values of phase leg currents, resulting in increase of power losses and increase in ripple magnitude of capacitor voltage in respective submodules. Thus, to eliminate the second harmonic component and ensuring that it contains a pure DC component the designed controller when implemented can be verified with the simulation results as shown in Figure 5.3.

Finally, the measured output current can be seen in Figure 5.4. It is to be noted that low order harmonics can be witnessed in i_s as the experiments were carried out at one-fourth of the rated power and basic NLC modulation was implemented with 4 submodules. Since, NLC does not eliminte the specific low order harmonics it is not recommended for MMC application with low number of levels.

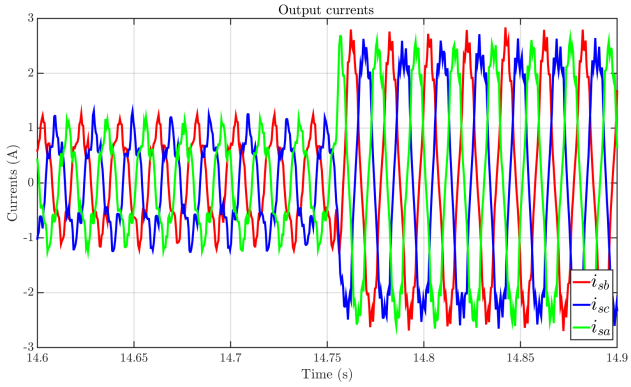

Figure 5.4: Measured output phase currents when a step of 2A in the reference is given at a time instant of 14.75s

Chapter 6

Conclusion and Future Work

6.1 Conclusions

- Analytical study of the internal unbalances in an MMC has been carried out. This unbalance can be a result of the asymmetries, non linearities and difference in the tolerances of the components as for example arm inductors and submodule capacitors used in an MMC. In order to mitigate the internal unbalances, an arm balancing control and sum capacitor energy control is proposed. The main aim of this controllers is to ensure equal energy storage among the arms and phases of an MMC. While implementing the arm balancing controller with the methodology as proposed in [25], it has to be noted that an injection of current within an arm of an MMC leg would unavoidably create coupling between other phases of the converter. In this way, the energy balance of each individual leg becomes difficult to be controlled independently since undesired fundamental frequency components will flow in the rest of the legs, exchanging energy from upper and lower arms respectively. Hence, an arm balancing controller is proposed and demonstrated ensuring energy balance among the arms eliminating the coupling between the other phases.

- Similarly, a sum capacitor energy control is proposed for balancing the energy among the phases. Furthermore, it is of importance to stress that during the theoretical analysis of this controller, it was realized that the DC-bus capacitor affects the system dynamics and needs to be considered during the control design. Furthermore, it is of importance to stress that the energy controllers are non-linear and for simplicity reasons, some assumptions has been made to make them linear based on average modeling. It is also to be noted that the arm balancing and sum capacitor voltage control methods are sensitive to the harmonic distortion of the measured signals.

- The implementation of these aforementioned proposed controllers has been able to ensure the energy balance among the arms and legs of an MMC during internal unbalanced conditions.

- Furthermore, faults on the grid side are also considered. During asymmetrical grid faults negative sequence voltage appears in the grid voltages and thus for proper grid synchronization, DSOGI-PNSE PLL method has been used. During fault conditions, sagging of the voltage is one of the major issues giving rise to unbalanced grid voltages at the PCC. The interaction between the injected currents and voltages during this period may give rise to uncontrolled oscillations in active power. Thus, it is important to keep the system running by balancing the injection of active and reactive power fulfilling the LVRT requirement of the system. Hence, in order to reduce the active power oscillations and assuring good overall system performance, mixed sequence injection has been explained and demonstrated.

- Moreover, a systematic approach has been introduced for the effective reduction of the sum capacitor voltage ripple in an MMC application. The injection of a second order harmonic component in the circulating current was proven to be capable of reducing the total capacitor ripple resulting in an reduction in the size of the capacitors by 33% of its initial value in MMC-HVDC. On the other hand, an increase of 7% of the total rms arm currents is also introduced. The effectiveness of the method in terms of cost and size depends on the application and dimensioning of the power components. As a future scope, an optimization method and an in-depth analysis can be carried out to find an optimum point between reducing the capacitor voltage ripple along with the cost and size of the capacitor to overall operational cost.

- The design and assembly of the MMC prototype has been explained in Chapter 4. Selection for the arm inductors and capacitors has been described based on the specific design criteria and system requirements. Several test had been done to ensure proper functionality of the system. DWO code for generating and sending gate signals to the sub-module boards has been programmed. Thus, the prototype was functional and was ready for the implementation of the designed controllers.

- Finally, after the construction of the prototype, experimental results were taken in order to implement the developed output and circulating current control. The energy balancing controllers were tried to be implemented with Basic sorting algorithm for Nearest Level Control, but due to low power operation and hardware limitations as described in section 1.5, NLC method was considered to be unsuited for multilevel converters with reduced number of levels. With very few number of sub-modules, the voltage error created is big and implementation of the proposed energy controllers normally require small changes in the voltage reference. Hence, with larger number of submodules, the resolution of the output voltage increases inferring in better control ability displayed by the proposed controller. At last, the converter output quality in terms of harmonics were also not taken into consideration.

- After understanding the basics and operating principle of this emerging topology, it is to be noted that the main advantage of this topology is that the output current and the internal circulating current can be treated independently which gives an extra degree of freedom from control point of view. Hence, MMC is considered suitable for HVDC application as it allows to deal with internal unbalances by controlling the circulating current without affecting the output current and is capable of handling the grid faults without affecting the DC-bus.

6.1.1 Future Work

- Analysis of the internal impact on the dynamics of the converter under different types of balanced and unbalanced faults.
- An enhanced non linear control strategy for an MMC based applications.
- Implementation of the proposed energy controllers with PS-PWM and other enhanced NLC modulation techniques in the built prototype.
- Evaluation of delays on the controllability of the converter.

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Appendix A

Developed PLECS Model of 1GW plant for this thesis

Figure A.1 displays the main schematic of the averaging model of Control of Modular Multilevel Converters for HVDC application during unbalanced condition.

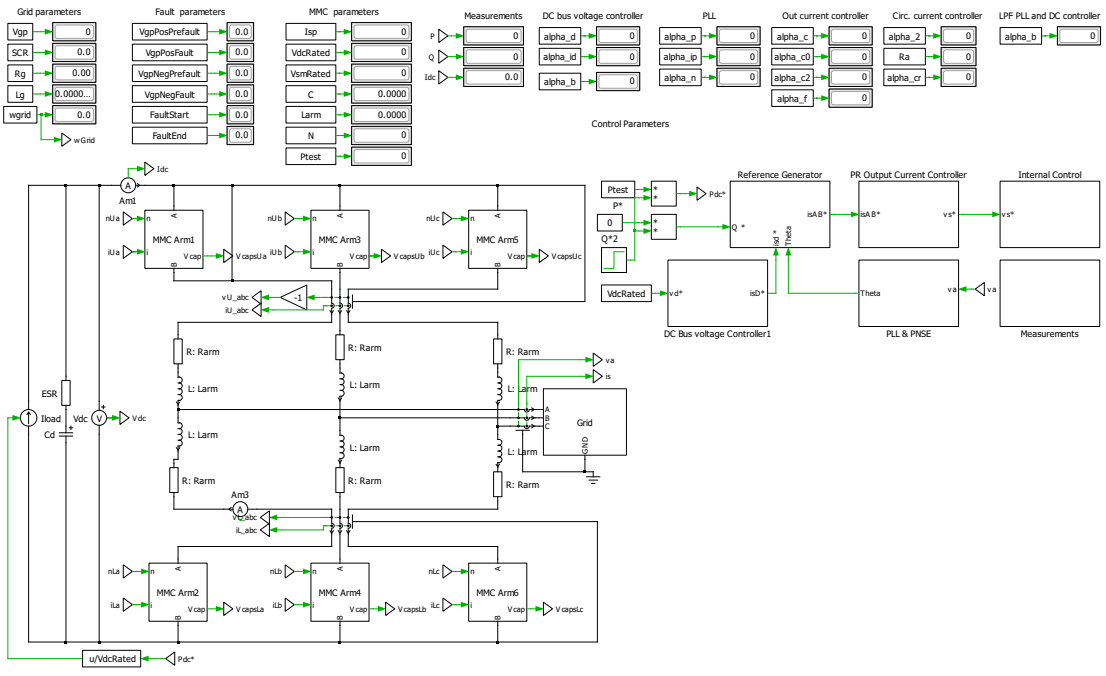


Figure A.1: Plecs Model for MMC-HVDC

It is important to check if the angle of the implemented PLL is properly aligned with the phase-A output voltage as it gives the correct reference to all the transformations used for designing the controllers. Hence the implemented phase locked loop using DSOGI-PNSE can be seen in Figure A.2.

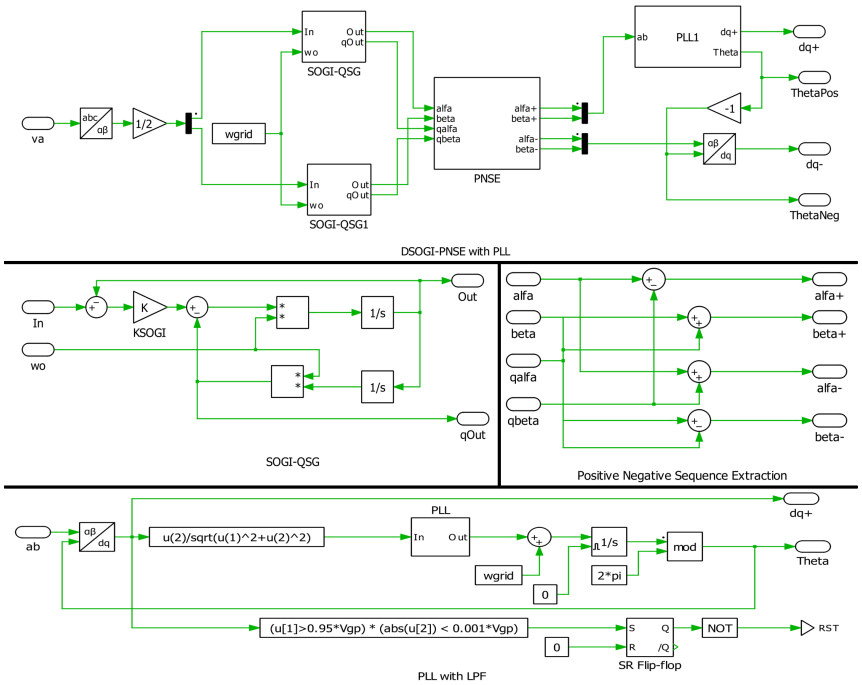


Figure A.2: DSOGI-PLL

The below shown schematics represents the output current control for the simulated model ensuring the correct output voltage reference which is one of the variables for implementing Direct Voltage Control for providing proper gate signals to switching device.

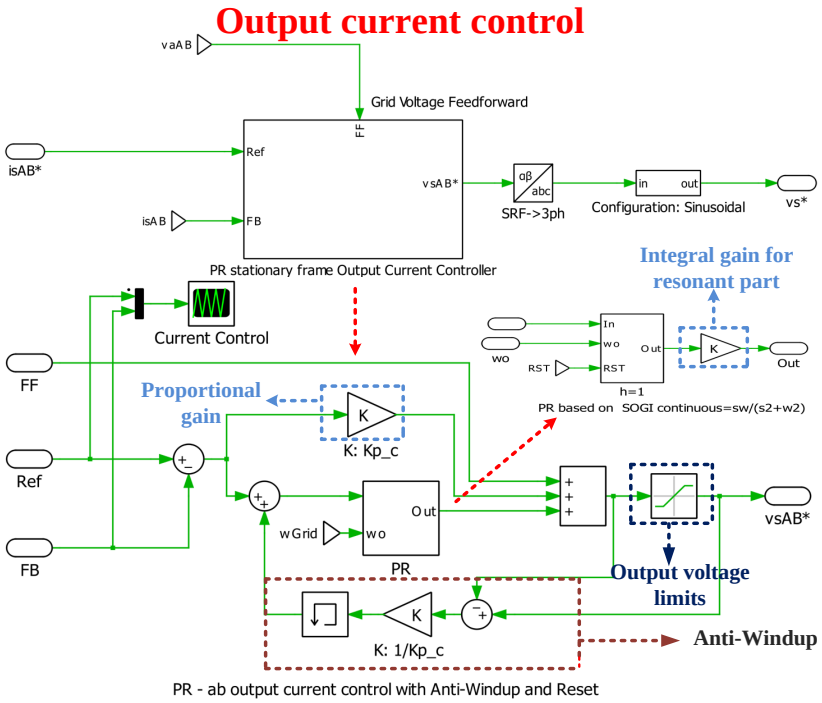


Figure A.3: Output Current Control

The below shown schematics represents the circulating current control for the simulated model to control the increase in peak and rms values of phase leg currents, resulting in reduced power losses and decrease in ripple magnitude of capacitor voltage in respective submodules. The control is capable of eliminating the second order harmonics in circulating current.

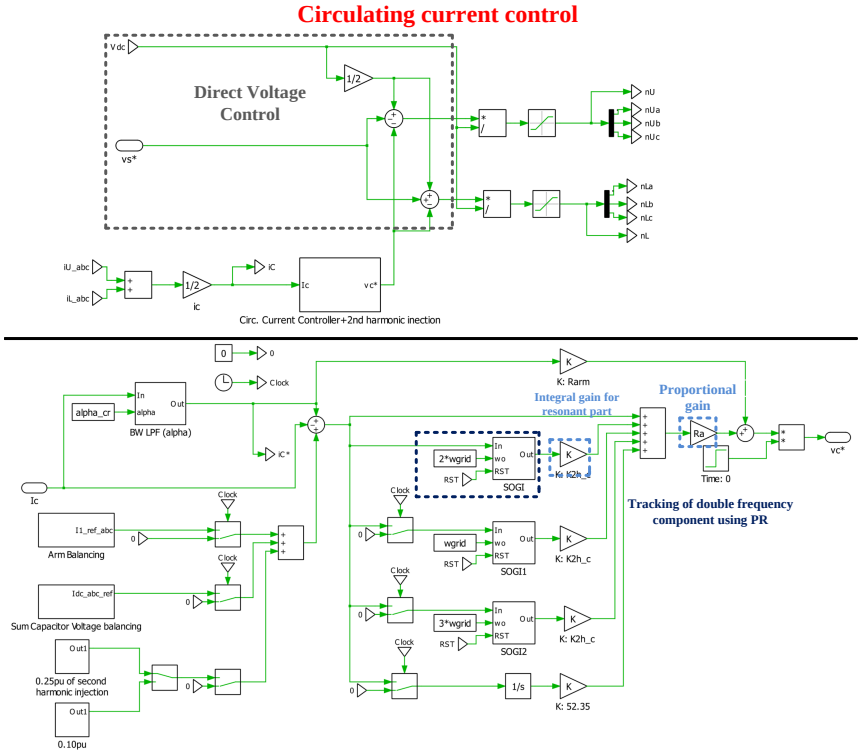


Figure A.4: Circulating current control

The below shown schematic represents the second harmonic injection in the circulating current to reduce the sum capacitor voltage ripple of its initial value and could be used to reduce the size of the capacitors by 33% in MMC-HVDC.

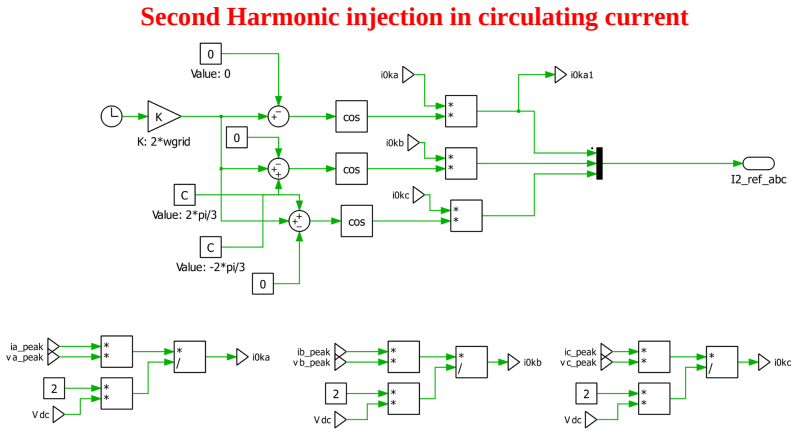


Figure A.5: Second Harmonic injection in the circulating current

The below shown schematic represents the arm balancing controller to ensure that the voltages and energy storage in specific arms remain balanced.

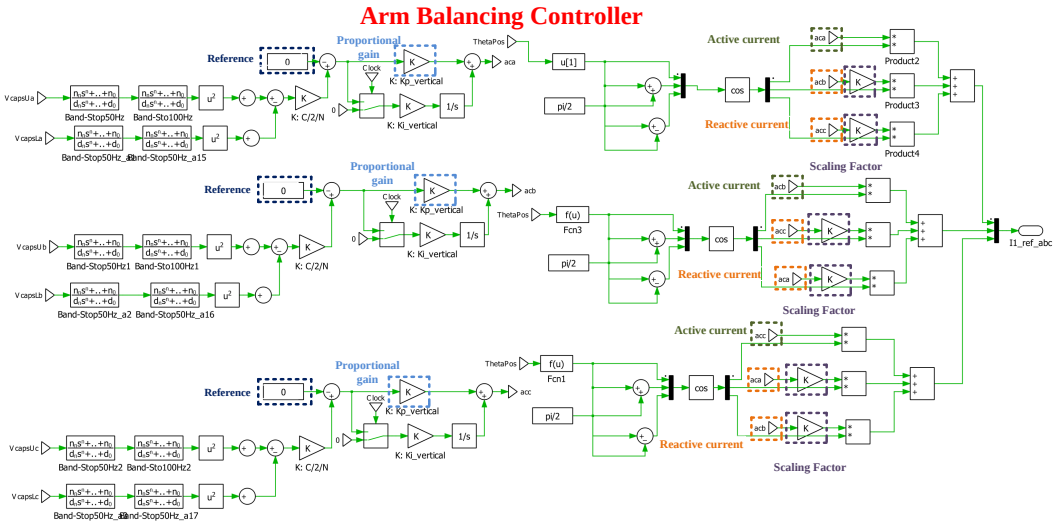


Figure A.6: Arm Balancing Controller

The below shown schematic represents the sum capacitor voltage balancing controller to ensure that the voltages and energy storage in the phases remain equal during internal unbalanced conditions in MMC-HVDC.

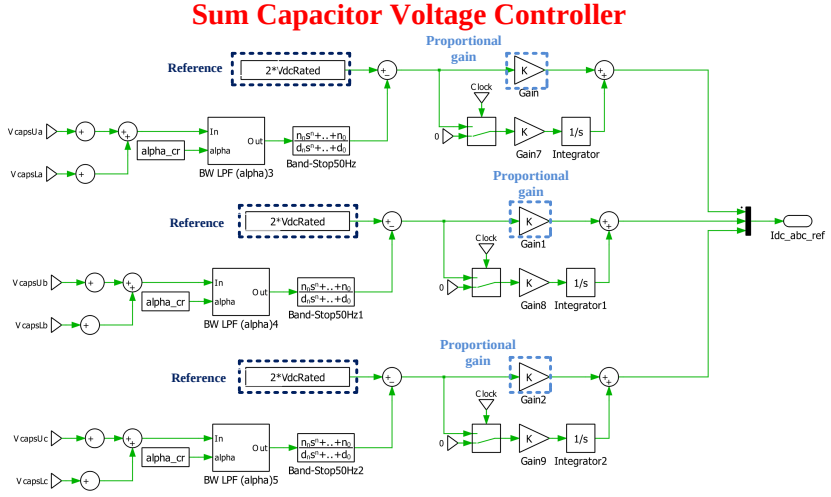


Figure A.7: Sum Capacitor Voltage Balancing Controller

Finally, the below shown schematics represents reference injection strategy for the simulated model which is implemented during grid faults.

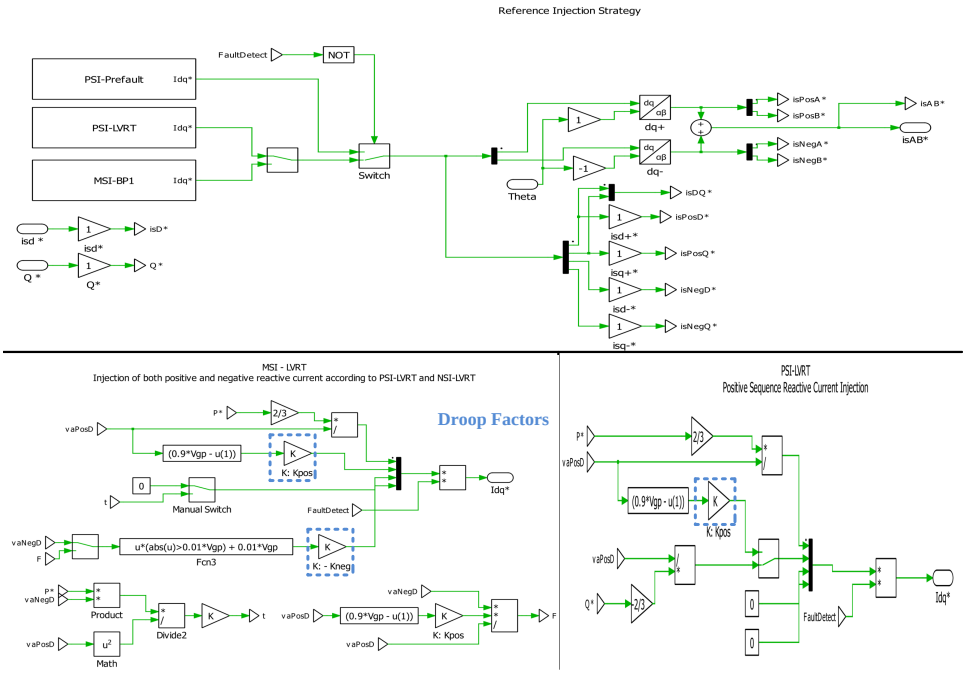


Figure A.8: Reference Injection strategy

The parameters for the simulated plant can be found below:

```
Assumptions:
% All cap voltages are equal (ideal balancing)
% The model is continuous based on ideal voltage source for
ac side and equivalent arm capacitance feeded by n*Iarm
% Memory blocks have been inserted to avoid algebraic loops
% Both output current and circulating current control loop can
be designed by selecting appropriate bandwidth
%The strength of the grid can be set by changing SCR

Grid parameters
fgrid=50; % Grid frequency
wgrid = 2*pi*fgrid;
Vgrid = 400e3; % Grid line lin RMS [V]
Vgp=Vgrid/sqrt(3)*sqrt(2); % peak phase voltage
GridPhaseInit = 0; % initial grid phase angle
Is = 2.05e3; %Output rated current RMS
Srated=sqrt(3)*Vgrid *Is;
Ptest=1000e6;
SCR=10; % SCR of grid at PCC
Lg=(Vgrid^2)/(sqrt(3)*1.1*wgrid*SCR*Srated);
Rg=wgrid*Lg/10;  assuming R = 10% of X

MMC power ratings
VdcRated=640e3;
PF=0.85;
N=40;
VsmRated=VdcRated/N;
Larm=20e 3;
Rarm= 0.1;
```

```
C=1.25e 3;
Carm = C/N;

Grid fault generation
FaultStart= 4;
FaultEnd = 4.2;
VgpPosPrefault=1;
VgpPosFault=0.8;
VgpNegPrefault=0;
VgpNegFault=0.2;
Isp=Is*sqrt(2);
Kneg=Isp/(0.5*Vgp);
Kpos=Isp/(0.4*Vgp);

Total impedance
L = Lg + Larm/2;
R = Rg + Rarm/2;

PLL parameters
KsogiPLL = sqrt(2)/2; %SOGI gain
alpha_p=50; % BW of PLL for tr=1/alpha=20ms
alpha_ip=10; % alpha_ip < alpha_p/2
alpha_b=200; %LPF to PLL

Output current control PR with Anti Windup and Reset
alpha_c=5000/3*pi;
alpha_c0=250/3*pi;
alpha_c2=250/3*pi;
Kp_c=alpha_c*L/2;
Kh_c0=2*alpha_c0*Kp_c;
Kh_c2=2*alpha_c2*Kp_c;
alpha_f = 1000;

Circulating current control
Ra=10/3*pi;%(R<<Ra<Kp)
alpha_2 = 50/3*pi; %  (alpha_c < wgrid)
K2h_c=2*alpha_2;%
alpha_cr=50; %

DC  voltage control
Cd=100e 6; % dc bus capacitance
alpha_d=50; % DC bus voltage control loop bandwidth
alpha_id=25,% Integral bandwidth
Ce=Cd+C*6/N;
Kp_d=alpha_d*Ce/2;% Gain of PI

Measurements
wc=2*pi*50;%  wc=50Hz

Arm balancing and Sum capacitor voltage balancing
Kp_vertical=6.0415e 04;
Kp_horizontal=0.0015;
```

Appendix B

DWO code and S-function file for Hardware and Software synchronization

B.0.2 DWO file

DWO file: Interrupt signals as well as board synchronization are generated through DWO programming. The implementation of a DWO application starts with writing of the DWO program itself. Compilation of the DWO application source file (.src) by using the DWO compiler DWOCOMP results in a C source file(.c) and a related header file(.h). The C file contains the encoded DWO object code and a load routine for downloading the object code to the DS5101 by a master DSP. The interruption is also programmed in the DWO code. Once again there should be one DWO.src file for master and slave cards DS5101 interface cards.

DWO code for the *DS*5101 master interface card:

```
unit ticks  # all delays are given in 25 ns ticks
delay ton  2000
delay toff 2000
%PWM Master Clock   runs at fDWO/2 with fDWO sampling frequency

ch1
reset, ton;
begin:
syncen,
phsint,  generate hardware interrupt on rising edge
tr2, tr3, tr4, tr5, tr6, tr7, tr8, tr9,
tr10, tr11, tr12, tr13, tr15, tr16, set, ton;

phsint,      generate hardware interrupt on falling edge
tr2, tr3, tr4, tr5, tr6, tr7, tr8, tr9,
tr10, tr11, tr12, tr13, tr15, tr16, reset, ton,
goto begin;

%PWM Channels   Ch2 to Ch13
ch2
set, wait;
```

```
begin:
syncen,
if flag2 set, wait, goto begin
else reset, wait, goto begin;

ch3
set, wait;
begin:
syncen,
if flag3 set, wait, goto begin
else reset, wait, goto begin;

ch4
set, wait;
begin:
syncen,
if flag4 set, wait, goto begin
else reset, wait, goto begin;

ch5
set, wait;
begin:
syncen,
if flag5 set, wait, goto begin
else reset, wait, goto begin;

ch6
set, wait;
begin:
syncen,
if flag6 set, wait, goto begin
else reset, wait, goto begin;

ch7
set, wait;
begin:
syncen,
if flag7 set, wait, goto begin
else reset, wait, goto begin;

ch8
set, wait;
begin:
syncen,
if flag8 set, wait, goto begin
else reset, wait, goto begin;

ch9
set, wait;
begin:
syncen,
if flag9 set, wait, goto begin
else reset, wait, goto begin;

ch10
set, wait;
begin:
syncen,
if flag10 set, wait, goto begin
else reset, wait, goto begin;

ch11
```

```
    set, wait;
85  begin:
    syncen,
87  if flag11 set, wait, goto begin
    else reset, wait, goto begin;
89
    ch12
91  set, wait;
    begin:
93  syncen,
    if flag12 set, wait, goto begin
95  else reset, wait, goto begin;

97  ch13
    set, wait;
99  begin:
    syncen,
101 if flag13 set, wait, goto begin
    else reset, wait, goto begin;
103
    %Enable and Reset: Active HIGH  Ch15 and Ch16
105 ch15
    reset, wait;
107 begin:
    syncen,
109 if flag1 set, wait, goto begin
    else reset, wait, goto begin;
111
    ch16
113 reset, wait;
    begin:
115 syncen,
    if flag1 set, wait, goto begin
117 else reset, wait, goto begin;

119 PWM Time Updates
    updfunc all
121 g ton;
    initfunc all
123 g ton;
```

DWO code for the *DS*5101 slave interface card:

```
unit ticks  # all delays are given in 25 ns ticks
delay ton  2000
delay toff 2000
%PWM Master:Clock runs at fDWO/2 with fDWO sampling frequency

ch1
rise, wait;
begin:
tr2, tr3, tr4, tr5, tr6, tr7, tr8, tr9,
tr10, tr11, tr12, tr13, tr15, tr16,

fall, wait;
tr2, tr3, tr4, tr5, tr6, tr7, tr8, tr9,
tr10, tr11, tr12, tr13, tr15, tr16,

rise, wait,
goto begin;

%PWM Channels   Ch2 to Ch13

ch2
set, wait;
begin:
syncen,
if flag2 set, wait, goto begin
else reset, wait, goto begin;

ch3
set, wait;
begin:
syncen,
if flag3 set, wait, goto begin
else reset, wait, goto begin;

ch4
set, wait;
begin:
syncen,
if flag4 set, wait, goto begin
else reset, wait, goto begin;

ch5
set, wait;
begin:
syncen,
if flag5 set, wait, goto begin
else reset, wait, goto begin;

ch6
set, wait;
begin:
syncen,
if flag6 set, wait, goto begin
else reset, wait, goto begin;

ch7
set, wait;
begin:
syncen,
if flag7 set, wait, goto begin
```

```
61 else reset, wait, goto begin;

63 ch8
   set, wait;
65 begin:
   syncen,
67 if flag8 set, wait, goto begin
   else reset, wait, goto begin;
69
   ch9
71 set, wait;
   begin:
73 syncen,
   if flag9 set, wait, goto begin
75 else reset, wait, goto begin;

77 ch10
   set, wait;
79 begin:
   syncen,
81 if flag10 set, wait, goto begin
   else reset, wait, goto begin;
83
   ch11
85 set, wait;
   begin:
87 syncen,
   if flag11 set, wait, goto begin
89 else reset, wait, goto begin;

91 ch12
   set, wait;
93 begin:
   syncen,
95 if flag12 set, wait, goto begin
   else reset, wait, goto begin;
97
   ch13
99 set, wait;
   begin:
101 syncen,
   if flag13 set, wait, goto begin
103 else reset, wait, goto begin;

105 %Enable and Reset  Active HIGH  Ch15 and Ch16

107 ch15
   reset, wait;
109 begin:
   syncen,
111 if flag1 set, wait, goto begin
   else reset, wait, goto begin;
113
   ch16
115 reset, wait;
   begin:
117 syncen,
   if flag1 set, wait, goto begin
119 else reset, wait, goto begin;
```

B.0.3 S-function files

It contains the information related with the connectivity between the Simulink model and the DWO code such as number of inputs as well as their initialization and declaration, interruption configuration, functions to update the signals value, flag declaration. There should be one sfcn file for master and slave cards DS5101 interface cards. S-function files for the master and slave interface card can be seen below:

```
/*********************************************************************\
* File: mmc_pwm_master.c                                              *
*Project: Modular Multilevel Converters AAU 2015                      *
* System: MMC with 24 modules + dSPACE DS5101 DWO                     *
* Description: S function template for DS5101 DWO master board        *
\*********************************************************************/

#ifndef MATLAB_MEX_FILE
# include <ds5101.h>
# include <ap5101.h>
# include <rti_msg_access.h>
# include <rti_common_msg.h>
#endif

/* ================================================================== */
/* ==== PUBLIC PART ================================================= */
/* ================================================================== */
/* ==== This file serves only as a template for the S function laying ==== */
/* ==== behind the DS5101DWO icon.                                    ==== */
/* ==== You must adapt the part below to fit your DS5101 application. ==== */
/* ================================================================== */

/* Set the name of this S function file (without extension). You must save
this file with exactly the name you specify below and specify it also
in the block mask. */

#define S_FUNCTION_LEVEL 2
#define S_FUNCTION_NAME mmc_pwm_master

/* Include the header file and the C file of your DS5101 application.
These are the output files of the DWO compiler. */

#ifndef MATLAB_MEX_FILE

#include "MMC_DWO_MASTER.h"
#include "MMC_DWO_MASTER.c"

/* Specify the number of DWO variables you want to write values to. This
number must match the number of inputs you specify in the icon mask
and the number of inputs of the MUX block driving the icon's input. */

#define NUM_DWOVARS 14

/* Specify the channels your application uses with a channel mask.
You should use the macro defined in your DS5101 application header
file for this. */

#define CHANNELMASK DS5101_MMC_DWO_MASTER_CHANNELS

/* Specify the load function defined in the C file of your
DS5101 application. Simply adapt the name, do not change anything
in the argument list. */
```

```
53
#define DS5101_LOAD() \
55 ds5101_mmc_dwo_master_load(boardBase, CHANNELMASK)

57 /* Specify the initialization function defined in the C file of your
DS5101 application. Adapt the name and specify an initial value for
59 every DWO variables.
If the initialization function is not defined for your application,
61 define DS5101_INIT_ALL as empty.
Do not modify the argument 'boardBase'. */
63
#define DS5101_INIT_ALL() \
65 ds5101_mmc_dwo_master_init_all(boardBase, 0.0)

67 /* Specify the update function defined in the C file of your
DS5101 application. Adapt the name and specify the S function
69 input for every DWO variable. The inputs to the S function
reach from u(0) up to u(NUM_DWOVARS - 1).
71 Do not modify the argument 'boardBase'. */

73 #define DS5101_UPDATE_ALL() \
ds5101_mmc_dwo_master_update_all(boardBase, u(0))
75
#endif
77

79 /**** DWO flags for MMC control ****/
static const int FLAG1 = 0x0001;        // FLAG 1 = ENABLE   1 = enable, 0 =
    stop
81 static const int FLAG2 = 0x0002;       // FLAG 2 = PWM2
static const int FLAG3 = 0x0004;        // FLAG 3 = PWM3
83 static const int FLAG4 = 0x0008;       // FLAG 4 = PWM4
static const int FLAG5 = 0x0010;        // FLAG 5 = PWM5
85 static const int FLAG6 = 0x0020;       // FLAG 6 = PWM6
static const int FLAG7 = 0x0040;        // FLAG 7 = PWM7
87 static const int FLAG8 = 0x0080;       // FLAG 8 = PWM8
static const int FLAG9 = 0x0100;        // FLAG 9 = PWM9
89 static const int FLAG10 = 0x0200;      // FLAG 10 = PWM10
static const int FLAG11 = 0x0400;       // FLAG 11 = PWM11
91 static const int FLAG12 = 0x0800;      // FLAG 12 = PWM12
static const int FLAG13 = 0x1000;       // FLAG 13 = PWM13
93
static const int STOP_MASK = 0xFFFE;    // ALARM/STOP FLAG mask   insert all
    modules
95 static const int INTR_MASK = 0x0001;   // PWM master interrupt for Simulink
    trigger


97
/* ================================================================== */
99 /* ===== END OF PUBLIC PART ========================================= */
/* ================================================================== */
101 /* ===== DO NOT CHANGE ANYTHING BELOW THIS LINE ===================== */
/* ================================================================== */
103

105 #include "simstruc.h"

107 #ifdef MATLAB_MEX_FILE
#include "mex.h"
109 #endif

111 #define u(i) *(real_T*)(u0Pointer[(i)])
```

```
113 /* input argument access macros */
    #define NUM_IN_ARGS              (3)
115 #define BOARD_NO_IDX             (0)
    #define CHANNEL_NUM_OF_IDX       (1)
117 #define SAMPLE_TIME_IDX          (2)
    #define INPUT_PORT_DIRECT_FEEDTHROUGH  (1)
119
    #define NUM_ARGS                  3
121 #define BOARD_NO                 (mxGetPr(ssGetSFcnParam(S, BOARD_NO_IDX))[0])
    #define CHANNEL_NUM_OF           (mxGetPr(ssGetSFcnParam(S,
        CHANNEL_NUM_OF_IDX))[0])
123 #define SAMPLE_TIME              (mxGetPr(ssGetSFcnParam(S,
        SAMPLE_TIME_IDX))[0])

125
    static void mdlInitializeSizes(SimStruct *S)
127 {
    ssSetNumSFcnParams(S, NUM_ARGS);
129 if (ssGetNumSFcnParams(S) != ssGetSFcnParamsCount(S))
    {
131 #   ifndef MATLAB_MEX_FILE
    rti_msg_error_set(RTI_SFUNCTION_PARAM_ERROR);
133 #   endif

135 return;
    }
137
    ssSetNumContStates(S, 0);
139 ssSetNumDiscStates(S, 0);
    ssSetNumInputPorts(S, 1);
141 ssSetInputPortDirectFeedThrough( S, 0, INPUT_PORT_DIRECT_FEEDTHROUGH);
    ssSetNumOutputPorts(S, 0);
143 ssSetInputPortWidth(S, 0, (int)CHANNEL_NUM_OF);
    ssSetNumSampleTimes(S, 1);
145 ssSetNumIWork      (S, 1);
    ssSetNumRWork      (S, 0);
147 ssSetNumPWork      (S, 0);
    ssSetNumModes      (S, 0);
149 ssSetNumNonsampledZCs(S, 0);
    ssSetOptions       (S, SS_OPTION_DISALLOW_CONSTANT_SAMPLE_TIME);
151
    }
153

155 static void mdlInitializeSampleTimes(SimStruct *S)
    {
157 real_T  sampleTime = (real_T) SAMPLE_TIME;

159 /* set sample time from parameter list */
    if (sampleTime == 1.0)          /* inherited */
161 {
    ssSetSampleTime(S, 0, INHERITED_SAMPLE_TIME);
163 ssSetOffsetTime(S, 0, FIXED_IN_MINOR_STEP_OFFSET);
    }
165 else if ((sampleTime == 0.0))    /* continuous */
    {
167 ssSetSampleTime(S, 0, CONTINUOUS_SAMPLE_TIME);
    ssSetOffsetTime(S, 0, FIXED_IN_MINOR_STEP_OFFSET);
169 }
    else                            /* discrete */
171 {
```

```
ssSetSampleTime(S, 0, sampleTime);
ssSetOffsetTime(S, 0, 0.0);
}
}
#define MDL_INITIALIZE_CONDITIONS
#if defined(MDL_INITIALIZE_CONDITIONS)
static void mdlInitializeConditions(SimStruct *S){

#ifndef MATLAB_MEX_FILE
int_T      boardBase;
int_T      boardNo            = (int_T) BOARD_NO;

boardBase = (int_T) get_peripheral_addr(DS5101_BOARD_ID, boardNo);
if (boardBase == 1)
{
rti_msg_error_set(RTI_IOBOARD_NOTFOUND_ERROR_DS5101);
exit(1);
}
ssSetIWorkValue(S, 0, boardBase);
ds5101_init(boardBase);
DS5101_LOAD();
DS5101_INIT_ALL();

ds5101_update_flags(boardBase, STOP_MASK);

ds5101_int_enable(boardBase, 1, DS5101_ENABLE);

ds5101_start(boardBase, CHANNELMASK);

#endif
}
#endif
static void mdlOutputs(SimStruct *S, int_T tid)
{
#ifndef MATLAB_MEX_FILE
long boardBase =   ssGetIWorkValue(S, 0);
InputPtrsType u0Pointer = (InputPtrsType)ssGetInputPortSignalPtrs(S,0);

int FLAG_MASK = 0;
if (u(1))    FLAG_MASK |= FLAG2;
if (u(2))    FLAG_MASK |= FLAG3;
if (u(3))    FLAG_MASK |= FLAG4;
if (u(4))    FLAG_MASK |= FLAG5;
if (u(5))    FLAG_MASK |= FLAG6;
if (u(6))    FLAG_MASK |= FLAG7;
if (u(7))    FLAG_MASK |= FLAG8;
if (u(8))    FLAG_MASK |= FLAG9;
if (u(9))    FLAG_MASK |= FLAG10;
if (u(10))   FLAG_MASK |= FLAG11;
if (u(11))   FLAG_MASK |= FLAG12;
if (u(12))   FLAG_MASK |= FLAG13;
if (u(13))   FLAG_MASK |= FLAG1;      // Enable
else FLAG_MASK = STOP_MASK;       // Stop

ds5101_update_flags(DS5101_1_BASE, FLAG_MASK);

DS5101_UPDATE_ALL();

ds5101_int_clear(DS5101_1_BASE, INTR_MASK);

#endif
}
```

```
235 static void mdlTerminate(SimStruct *S)
    {
237 #ifndef MATLAB_MEX_FILE

239 long boardBase =   ssGetIWorkValue(S, 0);

241 ds5101_stop(boardBase, CHANNELMASK);
    #endif
243 }
    #ifdef  MATLAB_MEX_FILE
245 #include "simulink.c"
    #else
247 #include "cg_sfun.h"
    #endif
```

S-function file for the slave card:

```
    /*********************************************************************\
  2 * File: mmc_pwm_slave.c                                               *
    * Description: S function template for DS5101 DWO slave board
        *\*******************************************************************/
  4
    #ifndef MATLAB_MEX_FILE
  6 # include <ds5101.h>
    # include <ap5101.h>
  8 # include <rti_msg_access.h>
    # include <rti_common_msg.h>
 10 #endif

 12 /* ========================================================================= */
    /* ===== PUBLIC PART ======================================================= */
 14 /* ========================================================================= */
    /* === This file serves only as a template for the S function laying === */
 16 /* === behind the DS5101DWO icon.                                      === */
    /* === You must adapt the part below to fit your DS5101 application. === */
 18 /* ========================================================================= */

 20 /* Set the name of this S function file (without extension). You must save
    this file with exactly the name you specify below and specify it also
 22 in the block mask. */

 24 #define S_FUNCTION_LEVEL 2
    #define S_FUNCTION_NAME mmc_pwm_slave
 26
    /* Include the header file and the C file of your DS5101 application.
 28 These are the output files of the DWO compiler. */

 30 #ifndef MATLAB_MEX_FILE
    #include "MMC_DWO_SLAVE.h"
 32 #include "MMC_DWO_SLAVE.c"

 34 /* Specify the number of DWO variables you want to write values to. This
    number must match the number of inputs you specify in the icon mask
 36 and the number of inputs of the MUX block driving the icon's input. */

 38 #define NUM_DWOVARS 12

 40 /* Specify the channels your application uses with a channel mask.
    You should use the macro defined in your DS5101 application header
 42 file for this. */
```

```
#define CHANNELMASK DS5101_MMC_DWO_SLAVE_CHANNELS

/* Specify the load function defined in the C file of your
DS5101 application. Simply adapt the name, do not change anything
in the argument list. */

#define DS5101_LOAD() \
ds5101_mmc_dwo_slave_load(boardBase, CHANNELMASK)

/* Specify the initialization function defined in the C file of your
DS5101 application. Adapt the name and specify an initial value for
every DWO variables.
If the initialization function is not defined for your application,
define DS5101_INIT_ALL as empty.
Do not modify the argument 'boardBase'. */

#define DS5101_INIT_ALL() \
ds5101_mmc_dwo_slave_init_all(boardBase, 0.0)

/* Specify the update function defined in the C file of your
DS5101 application. Adapt the name and specify the S function
input for every DWO variable. The inputs to the S function
reach from u(0) up to u(NUM_DWOVARS   1).
Do not modify the argument 'boardBase'. */

#define DS5101_UPDATE_ALL() \
ds5101_mmc_dwo_slave_update_all(boardBase, u(0))
#endif
/**** DWO flags for MMC control ****/
static const int FLAG1 = 0x0001;        // FLAG 1 = ENABLE   1 = enable, 0 =
    stop
static const int FLAG2 = 0x0002;        // FLAG 2 = PWM2
static const int FLAG3 = 0x0004;        // FLAG 3 = PWM3
static const int FLAG4 = 0x0008;        // FLAG 4 = PWM4
static const int FLAG5 = 0x0010;        // FLAG 5 = PWM5
static const int FLAG6 = 0x0020;        // FLAG 6 = PWM6
static const int FLAG7 = 0x0040;        // FLAG 7 = PWM7
static const int FLAG8 = 0x0080;        // FLAG 8 = PWM8
static const int FLAG9 = 0x0100;        // FLAG 9 = PWM9
static const int FLAG10 = 0x0200;       // FLAG 10 = PWM10
static const int FLAG11 = 0x0400;       // FLAG 11 = PWM11
static const int FLAG12 = 0x0800;       // FLAG 12 = PWM12
static const int FLAG13 = 0x1000;       // FLAG 13 = PWM13

static const int STOP_MASK = 0xFFFE;    // ALARM/STOP FLAG mask   insert all
    modules
static const int INTR_MASK = 0x0001;    // PWM master interrupt for Simulink
    trigger

/* ========================================================================== */
/* ===== END OF PUBLIC PART ================================================= */
/* ========================================================================== */
/* ===== DO NOT CHANGE ANYTHING BELOW THIS LINE ============================= */
/* ========================================================================== */

Rest of the code in this section is the same as presented above except for
board and flag configurations which can be seen below:
//  DS5101_INIT_ALL();

ds5101_update_flags(boardBase, STOP_MASK);

ds5101_start(boardBase, CHANNELMASK);
```

```
104 #endif
    }
106 #endif

108 static void mdlOutputs(SimStruct *S, int_T tid)
    {
110 #ifndef MATLAB_MEX_FILE

112 long boardBase =   ssGetIWorkValue(S, 0);
    InputPtrsType u0Pointer = (InputPtrsType)ssGetInputPortSignalPtrs(S,0);
114
    int FLAG_MASK = 0;
116 if (u(0))   FLAG_MASK |= FLAG2;
    if (u(1))   FLAG_MASK |= FLAG3;
118 if (u(2))   FLAG_MASK |= FLAG4;
    if (u(3))   FLAG_MASK |= FLAG5;
120 if (u(4))   FLAG_MASK |= FLAG6;
    if (u(5))   FLAG_MASK |= FLAG7;
122 if (u(6))   FLAG_MASK |= FLAG8;
    if (u(7))   FLAG_MASK |= FLAG9;
124 if (u(8))   FLAG_MASK |= FLAG10;
    if (u(9))   FLAG_MASK |= FLAG11;
126 if (u(10))  FLAG_MASK |= FLAG12;
    if (u(11))  FLAG_MASK |= FLAG13;
128
    //    if (u(12))  FLAG_MASK |= FLAG1;      // Enable
130 //        else FLAG_MASK = STOP_MASK;      // Stop

132 ds5101_update_flags(DS5101_2_BASE, FLAG_MASK);

134 //    DS5101_UPDATE_ALL();

136 #endif
    }
138
    static void mdlTerminate(SimStruct *S)
140 {
    #ifndef MATLAB_MEX_FILE
142
    long boardBase =   ssGetIWorkValue(S, 0);
144
    ds5101_stop(boardBase, CHANNELMASK);
146 #endif
    }
148
    #ifdef  MATLAB_MEX_FILE
150 #include "simulink.c"
    #else
152 #include "cg_sfun.h"
    #endif
```

Appendix C

Matlab Scripts for tuning the Energy Controllers:'fsolve' function

```
%Arm Energy Controller.

clearvars
close all

Par.Kp=10/3*pi;
Par.Vdc=640e3;
Par.L=20e 3;

Par.Ko= 1;
Par.tr= 0.9;
Par.ConTime= 0.045;

options =
    optimoptions('fsolve','Display','iter','MaxFunEvals',100000,'MaxIter',100);

X0=[0.5;30]; %Initial Conditions
X=fsolve(@(X) segundo_orden(X,Par),X0,options);

wn=X(2);
psi=Par.Kp/(Par.L*2*wn);
G=tf([Par.Ko*wn^2],[1 2*psi*wn wn^2]);
step(G)
hold on
figure()
bode(G)
X
Kp_Energy=wn^2*4*Par.L/(Par.Vdc*Par.Kp)
```

```
%Sum Capacitor Voltages Energy Controller.

clearvars
close all

Par.Kp=10/3*pi;
Par.Vdc=640e3;
```

```
Par.L=20e-3;
Par.Cd=1.7500e-04; %Equivalent capacitance Ceq


Par.Ko= 1;
Par.tr= 0.9;
Par.ConTime= 0.35;

options =
    optimoptions('fsolve','Display','iter','MaxFunEvals',100000,'MaxIter',100);

X0=[0.5;30]; %Initial Conditions
X=fsolve(@(X) segundo_orden(X,Par),X0,options);

wn=X(2);
psi=Par.Kp/(Par.L*2*wn);
G=tf([Par.Ko*wn^2],[1 2*psi*wn wn^2]);
step(G)
hold on
figure()
bode(G)
X
Kp_Energy=wn^2*Par.Cd*Par.L/Par.Kp
```

```
% 'fsolve' function. Common for both controllers.

function H=segundo_orden(X,Par)

t=X(1);
wn=X(2);
psi=Par.Kp/(Par.L*2*wn);

Ko=Par.Ko;

p1=wn*(psi+sqrt(psi^2-1));
p2=wn*(psi-sqrt(psi^2-1));
y=Ko*(1-wn/(2*sqrt(psi^2-1))*(exp(p1*t)/p1-exp(p2*t)/p2));
H1=y-Par.tr*Ko;
H2=t-Par.ConTime;
H=[H1;H2];
```

Appendix D

Submodule Board Schematic Design

The design of the submodule board with implemented protection can be seen in Figure D.1.

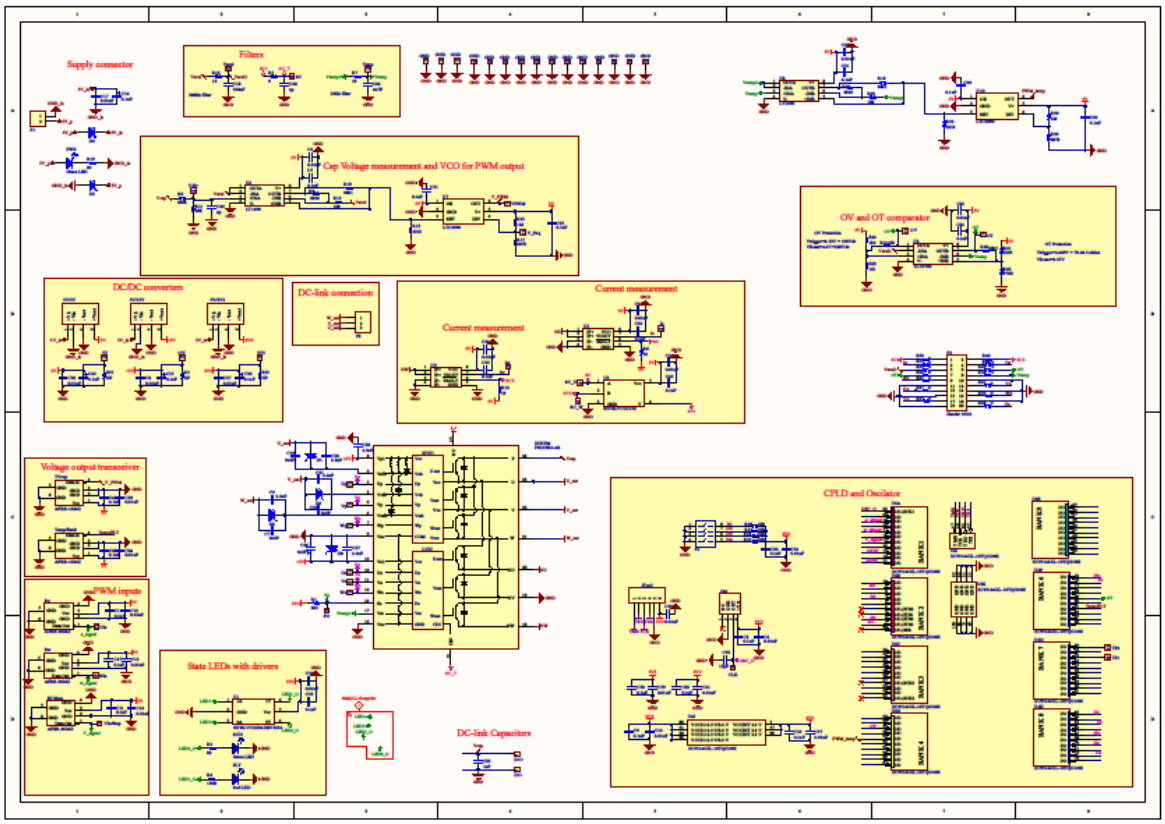
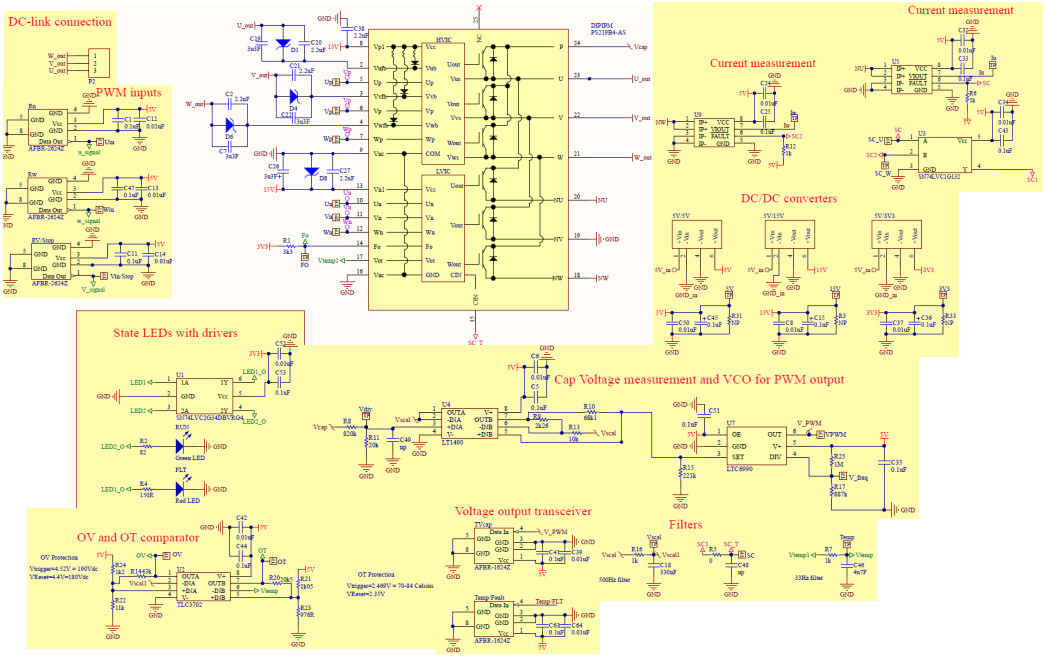
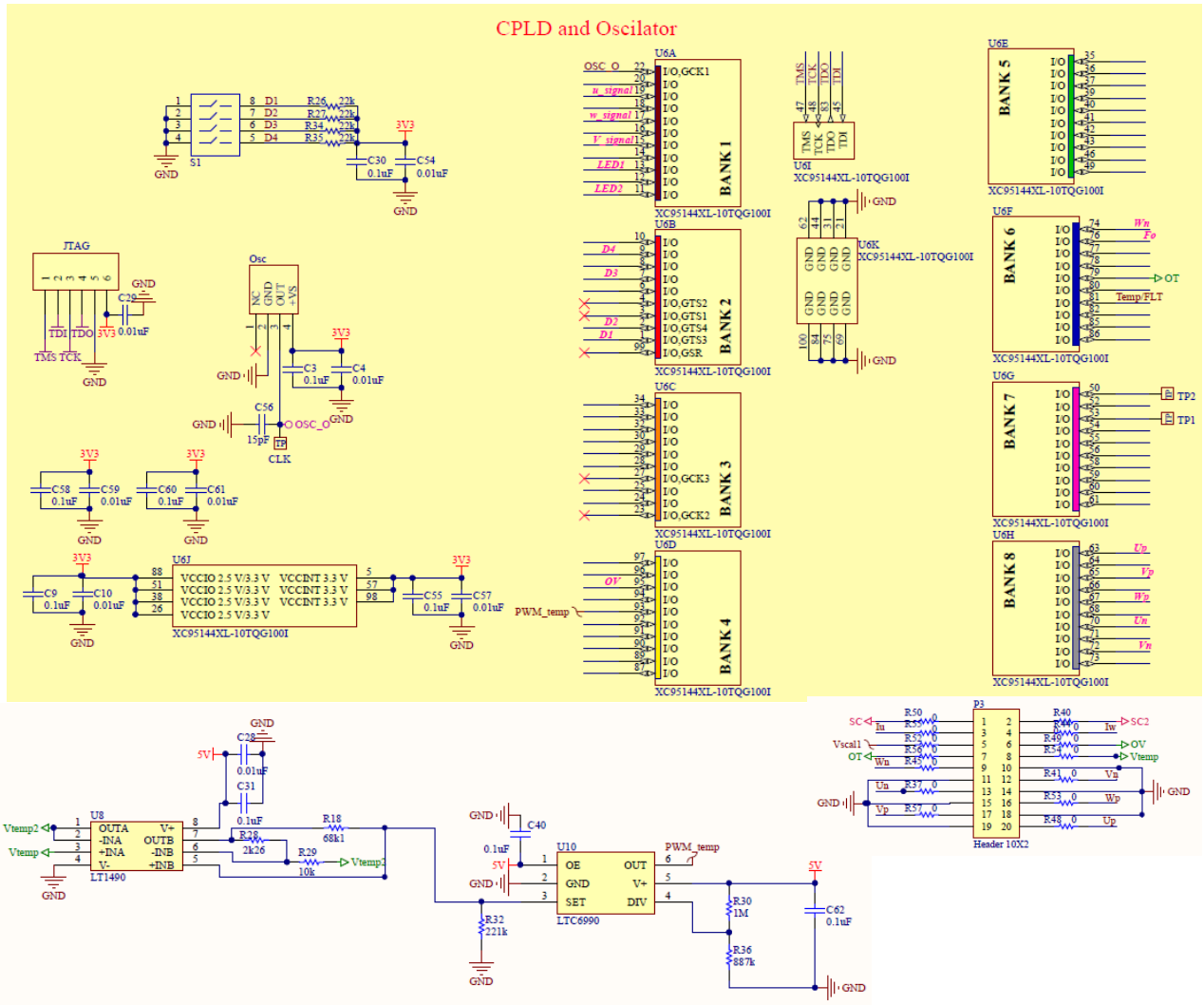


Figure D.1: Submodule board schematic design

Zoomed view of the aforementioned schematic.




CPLD and Oscilator
U6A
U6B
U6C
U6D
U6E
U6F
U6G
U6H
U6I
U6J
U6K
BANK 1
BANK 2
BANK 3
BANK 4
BANK 5
BANK 6
BANK 7
BANK 8
XC95144XL-10TQG100I
JTAG
Osc
S1
CLK
OSC_O
PWM_temp
U8
LT1490
U10
LTC6990
P3
Header 10X2
GND
3V3
5V