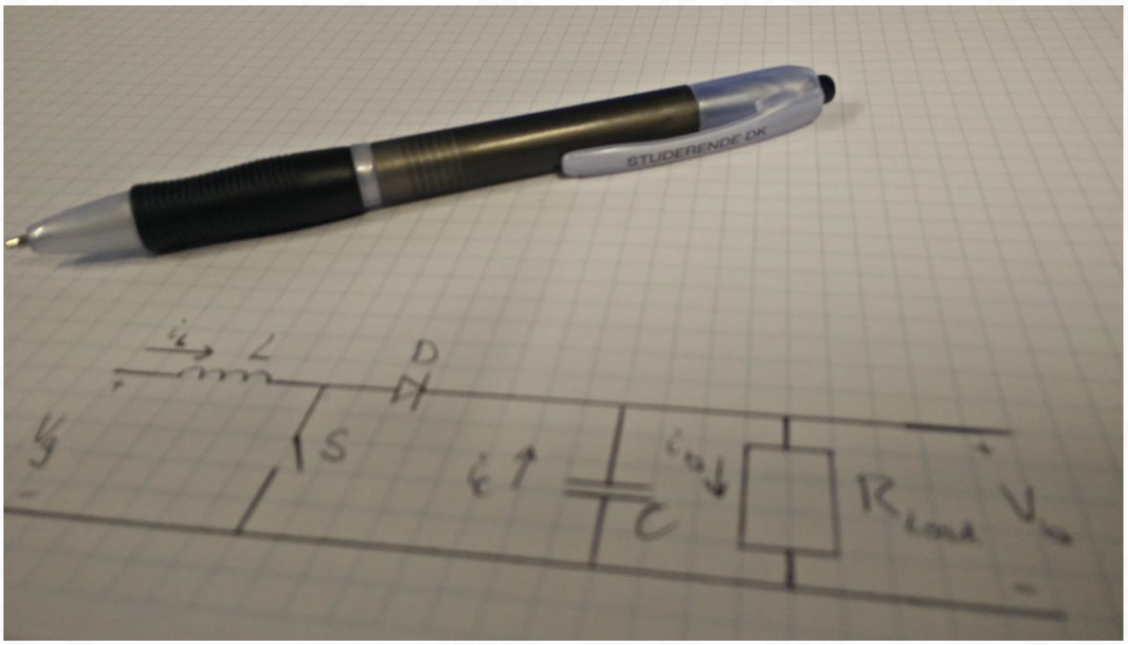
Control of Power Factor Correcting Boost Converter, Supplying an Inverter for an Asynchronus Motor



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STUDENTS STUDYREPORT

Fibigerstræde 16 ▪ DK 9220 Aalborg Ø ▪

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Abstract

In this project an inverter is refitted to use AC grid voltage or DC voltage as input voltage, instead of only DC voltage, by use a boost converter and rectifier. A dynamic model of the boost converter is designed and controlled with a feedfoward scheme for power factor corrector. The boost converter with controller is initially simulated and implemented with resistive load. Subsequently the boost converter is simulated and implemented driving an asynchronous AC motor. The controllers are implemented on a DSP, and tested on a physical system, with the AC motor driving a fan developed for poultry farms. A SVM switching schemes for the inverter is implemented. A complete model, including the boost converter, inverter, AC motor and fan is simulated with good result. The implementation in the physical system however yields poor results.

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Preface

This report reflects the work done by a project group on the 4nd semester under the study of *Electromechanical System Design master programme*, under the department of *Mechanical and manufacturing engineering*, at Aalborg University. The work is carried out in the period from 02.02.2015 to 03.06.2015, by a group of two students. The project concerns the development of a rectifier and boost converter control scheme, which is intended to supply an inverter, supplying a Permanent Magnet synchronous motor, which drives a wall mounted fan intended for drying facilities. Tests are performed on the Eltronic inverter board, and on a DACS ventilation system, fitted with an asynchronous AC motor, intended for poultry farms.

Reading guidelines
Figures, equations, and tables are numbered consecutively in order of appearance. Citations and references are carried out using the Harvard method, and are placed in context in the text. A complete list of references is found at the end of the report.

Software used
Matlab 2015a, Simulink, Altium Designer and Code Composer Studio where used during the simulation, design and control processes during the project.

Speial thanks The project group would like to thank Eltronic for providing the inverter board, and DACS for providing the AC motor and the poultry ventilation setup, that tests are performed on.

The project is supplemented by an annex CD, on the CD is found: Diagrams and component lists of the Eltronic inverter board and the designed rectifier board, plus the c-code script file and mathematical simulation models.

Contents

Nomenclature

Name	Decription	Unit	Name	Decription	Unit
C	Capacitor	F	R	Resistor	Ω
CV	Compare Value	count	R_1	Stator resistance	Ω
D	Duty cycle	-	R'_2	Rotor resistance related to the stator	Ω
Δi_L	Peak to peak deviation of i_L	A	R_C	Capacitor resistance	Ω
E_1	Induced voltage in stator windings	V	R_D	Diode resistance	Ω
e_i	Error to current controller	-	R_L	Inductor resistance	Ω
e_v	Error to voltage controller	V	R_Load	Load resistance	Ω
f_{nom}	Nominal frequency output of SVM	Hz	R_S	Switch resistance	Ω
G_C	Current controller	-	S	Switch	-
G_V	Voltage controller	-	s	Slip	-
i_ϕ	Magnetizing current	A	$sector\theta$	Sector angle	rad
i'_{2A}	Rotor current related to the stator phase A	A	SV_{1-6}	Active space vectors	V
i'_{2B}	Rotor current related to the stator phase B	A	t_{off}	Off time for svitch	s
i'_{2B}	Rotor current related to the stator phase C	A	t_{on}	On time for svitch	s
I_{bB}	Avg i_b at boundary of CCM and DCM	A	T_{peak}	Time of conduction in DCM	s
I_{LB}	Avg i_L at boundary of CCM and DCM	A	t_{ramp}	Ramping time of SVM	s
I_{Lpeak}	Peak value of i_L	A	T_{SV1}	On time for space vector 1	s
i_1	Stator current	A	T_{SV2}	On time for space vector 2	s
i'_2	Rotor current related to the stator	A	T_s	Sample time	s
i_b	Load current	A	τ_{fan}	Fan torque	Nm
i_C	Capacitor current	A	τ_{mech}	Mechanical torque	Nm
i_G	Grid current	A	$\tau_{mech-tot}$	Mechanical torque sum of 3 phases	Nm
i_L	Inductor current	A	TB	Time base	s
$k_{g,1}$	Gain at frequency of ω_z	-	θ_o	Angle of output vector	rad
$K_{I,v}$	I-gain of voltage controller	-	θ_s	Synchronous angle	rad
$K_{P,v}$	P-gain of voltage controller	-	U	IC	-
K_g	P-gain of current P controller	-	V_{1A}	Voltage motor phase A	V
k_g	Gain of current I-Lead controller	-	$V_{control}$	Control output of voltage controller	V
L	Inductor	H	V_{min}	Minimum voltage output of SVM	V
L	Inductance	H	V_{nom}	Nominal voltage output of SVM	V
L_1	Stator inductance	H	V_{U0}	Phase voltage inverter phase U	V
L'_2	Rotor inductance related to the stator	H	V_{V0}	Phase voltage inverter phase V	V
L_G	Grid inductance	H	V_1	Stator voltage	V
L_m	Magnetizing inductance	H	V_b	Boost voltage	V
ω_{mech}	Mechanical rotaional velocity	$\frac{\text{rad}}{\text{s}}$	v_G	Grid voltage	V
ω_p	Frequency of pole of I-Lead controller	Hz	v_g	Rectivied grid voltage	V
ω_s	Synchronous angular velocity	$\frac{\text{rad}}{\text{s}}$	V_m	Magnitude of space vector	V
ω_z	Frequency of zero of I-Lead controller	Hz	V_o	Output vector in SVM	V
P_B	Power at boundary of CCM and DCM	W	V_ref	Reference voltage	V
PR	Period register	count	X	Reactance	Ω

Resumé

I dette project er der udleveret et inveter print med et inverter IC på, fra Eltronik. Ved modtagelsen af inveter printet, var den sat op til at kunne få DC spænding som input og med styring bruge dette, til at drive en tre faset motor. Et program til at styre en motor, er ikke forud installeret på PCB'en.

inveter printet skal udvides til at kunne bruge AC spænding fra nettet med en spænding på 230 V RMS. For at kunne koble inveter printet direkte i nettet er der under projektet implementeret en ensretter og en boost converter. På figur 1 er den over ordnede model struktur set. v_G er net spændingen som er input til ensretteren. Denne outputter v_g som har karaktestikken af en numerisk sinus.

Boost converteren forstærker v_g til V_b ved hjælp at en spole og regulering af en IGBT. Der er også en kondensator til at udjævne V_b. Spolen er bestemt udfra boost converteren ikke må komme i discontinuous conduction mode. IGBT'eren er regulered ved en feedforward control struktur som er først er testet med en simularing af boost converteren og derefter implementeret på DSP. Boost converteren er testet ohmsk modstand. Til denne regulator skal der bruges nogle målinger, som er volt måling af v_g og v_b, og en strøm måling af spole strømmen. Til volt målingerne er det nødvendig at konstruere et PCB med voltmetrene som kan sende propositionelle analoge signal til DSP'en. På dette PCB er spolen og ensrettene også placeret.

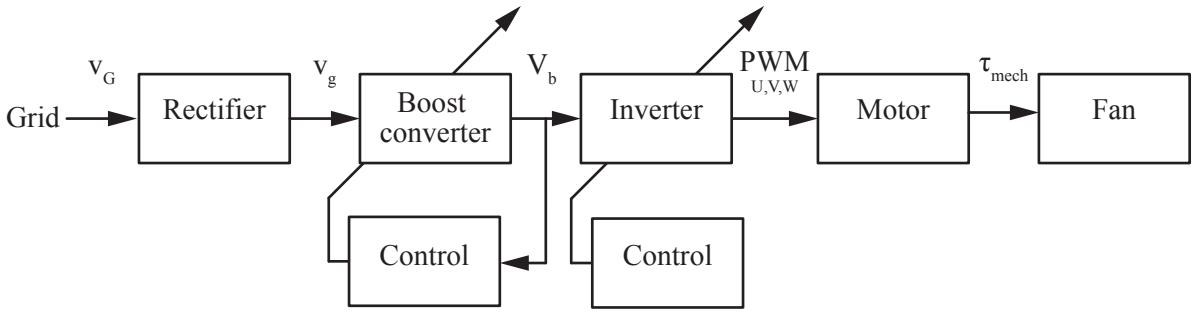

Figure 1: Sketch of the hardware setup.

Inveteren bruges til af styre en AC motor. Denne styring er gjort ved hjælp space vektor modulation, dette giver 15 % støre modulations index end ved sinus modulation. Dette er lige ledes implementeret på DSP'en.

Der er lavet AC motor model, med en blæser som last. Dette er her efter samlet i en komplet

model, med ensretter, boost converter, inverter, AC motor og fan. Denne samlede model giver gode simulerings resultater. Forsøg på det fysiske samlede system giver dårlige, grundet boosten ikke startet korrekt.

Chapter 1

Introduction

The small Danish family owned company DACS, have recently introduced the most efficient wall mounted fans on the marked. The fan is driven by a Permanent Magnet synchronous motor, together with an off-the-shelf inverter. A way to further improve the efficiency, and make the fan even more flexible, is to develop a Power Factor Correction (PFC) front end of the inverter. [Rasmussen et al., 2015]

Eltronic have recently made a full prototype inverter board, with an integrated motor drive IC with PFC, to be used for an automotive application (www.CIPED.dk), where the PFC part is not utilized. [Rasmussen et al., 2015] The Eltronic inverter board is supplied by a DC voltage.

The overall idea behind the project is to merge the fan from DACS and the inverter board from Eltronic. To enable the combination of the two products to be supplied by a grid voltage. It is therefore desired to develop a rectifier and a PFC controller, that is able to supply the inverter.

The main concern of this project is to develop a boost converter controller and to implement PFC control. The primary aim of the project is to develop a robust PFC control structure, that maintains the response of the current drawn from the grid, to show a sine wave characteristic, when exerted to various loads.

Chapter 2

Hardware setup

In the project some equipment is produced prior to the project and some equipment is produced during the project. To get all the equipment to work together, the mode of operation for the equipment is examined. This chapter describes the hardware superficially and describes some of the considerations done to interface with the components. The overall structure of the setup is shown in figure 2.1, from grid voltage to motor control. The boost and inverter is both controlled its own controller (symbolist by the arrow through the boost and inverter).

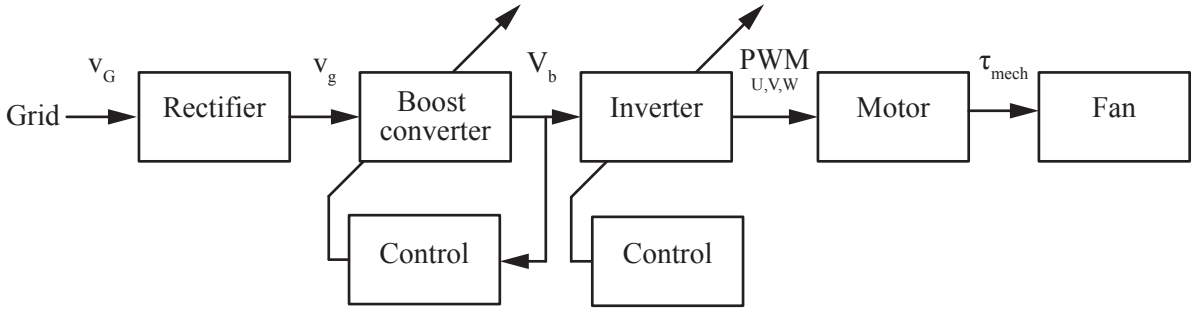

Figure 2.1: Sketch of the hardware setup.

The grid is rectified using a standard bridge rectifier. This is done on the baby board, described in section 2.3. The rectified grid voltage is input to the boost converter, which is used to boost the voltage to a quasi constant DC bus, by controlling the duty cycle of the boost converter switch. The inverter converts the DC bus into 3 phase AC voltage.

Both the boost converter and the inverter are included in the power module, used in the Eltronic inverter. The Eltronic inverter board is described in section 2.1, while the theory of the boost converter is described thoroughly in chapter 3 *Boost converter*, and the inverter in chapter 4 *Inverter*. The 3 phase AC voltage is used to drive an AC motor, which is described in chapter 5 *AC motor*. The inverter and boost converter is controlled by a DSP, considerations and reflections of the DSP programming are described in section 2.2.

2.1 Eltronic inverter board

Through this section, some selected components of the Eltronic inverter is superficially described. That is the implementation of the current sensors plus a rough description of the control signals required to operate the inverter and PFC module.

2.1.1 Current sensors

On the Eltronic inverter board, a number of current sensors are implemented. The diagram of the implementation is shown in figure 2.2. The sensor shown is the sensor measuring the inductor current, or system current (I-SYS).

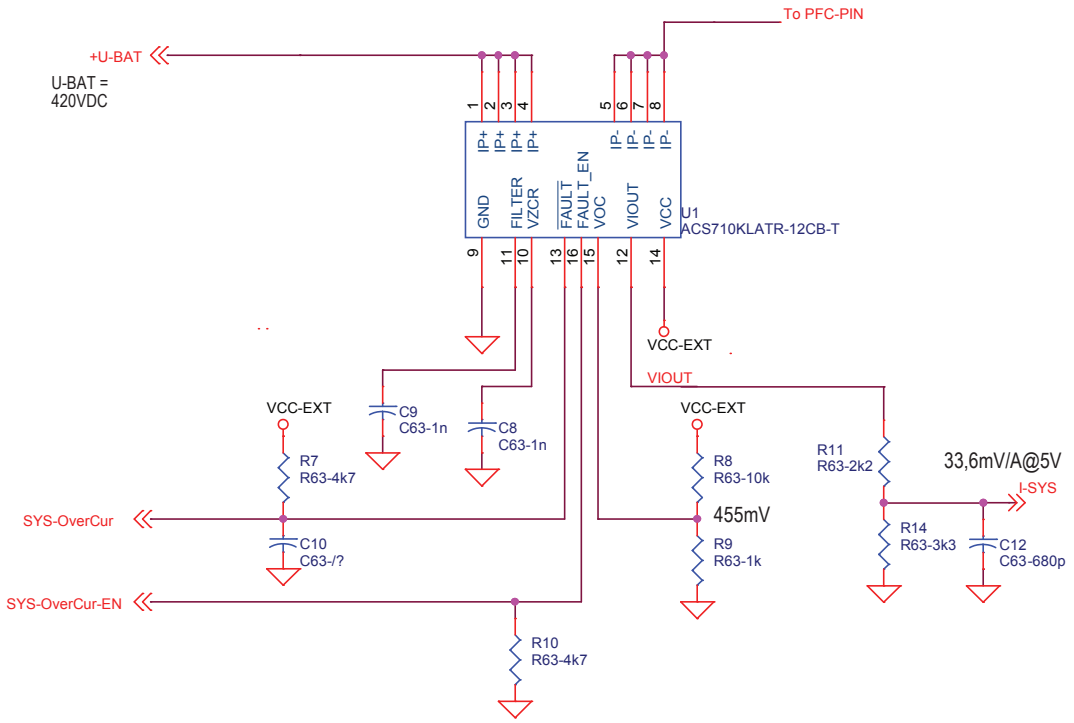

Figure 2.2: Diagram of the implementation of the current sensor measuring the inductor current, or system current (I-SYS), [Eltronic, 2014].

There is a letter and a number, and underneath is the component name. The letter is the type of component. The number is to distinguish between the different components for soldring. The letters means

- R is a resistor.
- C is a capacitor.
- U is a IC.

The IC in figure 2.2 is the current sensor. The pins in the current sensor is:

- IP+ (pin nr. 1-4) and IP- (pin nr. 5-8) senses the current that runs from IP+ to IP- by use of Hall effect.
- GND (pin nr. 9)is ground.
- FILTER (pin nr. 11) sets the bandwidth, by connecting a capacitor. This is done by choosing bandwidth and read off a plot in the data sheet. The bandwidth is set to 80 kHz [Allegro, 2007].
- VZCR (pin nr. 10) is a voltage reference. This not an accurate measurement.
- FAULT (pin nr. 13) outputs logic high if the current is lower than a current threshold and logic low if the current is above the threshold. The threshold is set on the VOC pin.
- FAULT_EN (pin nr. 16) enables the FAULT when high.
- VOC (pin nr. 15) sets the threshold for the FAULT pin. The threshold is calculated with equation 2.1. The sens parameter is set by the data sheet [Allegro, 2007].
- VIOUT (pin nr. 12) outputs the measurement in voltage.
- VCC (pin nr. 14) is the supply voltage ($VCC\_EXT = 5\,\mathrm{V}$).

$$I_{OC} = \frac{VOC}{sens} = \frac{455mV}{56mV/A} \approx 7.9 \tag{2.1}$$

Pins 1 to 8 is galvanic isolated from the pins 9 to 16. Pins 9-16 is the cold side i.e. same ground as the DSP. The VCC_EXT is from the DSP

From the data sheet of the current sensor [Allegro, 2007], it is stated, that the output equals half of the supply voltage $VCC - EXT$ at zero current flow. As seen in the diagram figure 2.2, thereby the output is 2.5 V at a supply of 5 V.

As seen in the diagram, the VIOUT is led to a voltage divider. The voltage divider ensures that by a supply of 5 V the output is maximum 3 V, which is the maximum measurable value of the Analogue to Digital Converter (ADC) in the applied DSP, see equation 2.2.

$$V_{out} = \frac{R_2}{R_1 + R_2} \cdot V_{in} = \frac{3.3kHz}{2.2kHz + 3.3kHz} 5\,\mathrm{V} = 3\,\mathrm{V} \tag{2.2}$$

As further stated in the diagram, the output signal $I - SYS$, deviates from the $\frac{V_{out}}{2}$ with $33.6\frac{\mathrm{mV}}{\mathrm{A}}$. The offset output signal and the voltage divider are encountered for by the program on the DSP, discussed in section 2.2.

The current sensor discussed is similar to current sensors implemented in the Eltronic inverter, measuring the current to the motor terminals, $I - VRU$, $I - VRV$ and $I - VRW$.

2.1.2 Signals to operate power module

The signals, operating the power module i.e. signals the controlling the switches, are on the Eltronic inverter board isolated galvanic isolated by use of optocoulpers. The optocoupler setup for the PFC switch is shown in figure 2.3.

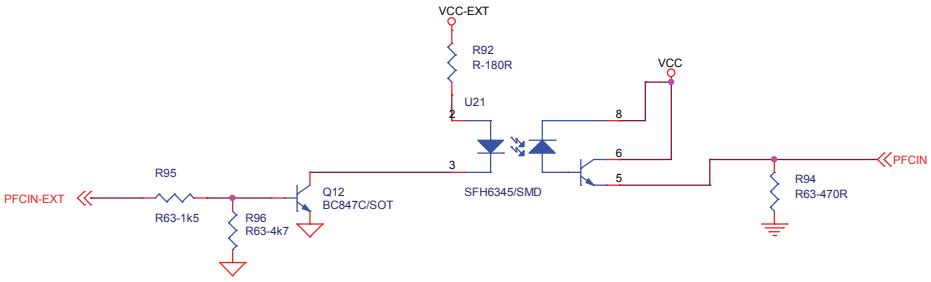

Figure 2.3: Diagram of the implemented optocoupler for the PFC switch, [Eltronic, 2014].

As seen in figure 2.3 the optocoupler is connected to VCC (5 V on the hot side) and the external PFC signal pin $PFCIN - EXT$. When given a high signal on $PFCIN - EXT$ from the DSP, the PFC switch is switched on i.e. conducting.

Similar optocouplers are implemented for the six inverter switches and for the $PFC - TRIP$, $I - TRIP$ and the $\backslash FLT - EXT$ pins. The $PFC - TRIP$ and $I - TRIP$ are signals from the DSP to the power module, to abort operation in case ex. software measurements shows too high currents. The $SYS - OverCur$ from figure 2.2 also the $PFC - TRIP$, and there by giving hardware protection from over current, there are similar arrangements with the $I_T RIP$ from each of teh three phases current sensors. The $\backslash FLT - EXT$ pin is contrary to the other pins a "Read" pin. In operation the pin is set high, and by fault in the power module, it sets the $\backslash FLT - EXT$ low.

The discussed signals and sensor are the main concerns of this project, and no other components of the Eltronic inverter is described in detail.

2.2 DSP programming

This section describes the DSP programming and experiments performed, to verify that measurements of voltage and current is done correctly.

2.2.1 Initial DC experiments

Initial experiments are made, to verify that the measurements of voltage and measurement of current are implemented correctly in the software. Furthermore the software implementation of the boost converter control is verified. These experiments are done at low DC supply voltage, to avoid any damage to the hardware.

To exclude inverter control from the initial experiments, and only examine boost converter, a resistor is soldered across the DC bus as load. As mentioned the experiments are performed at a low DC supply voltage, a 0 - 30 V DC supply is used as source. The experimental setup is shown in figure 2.4, and the voltage measurements are described in section 2.2.2.

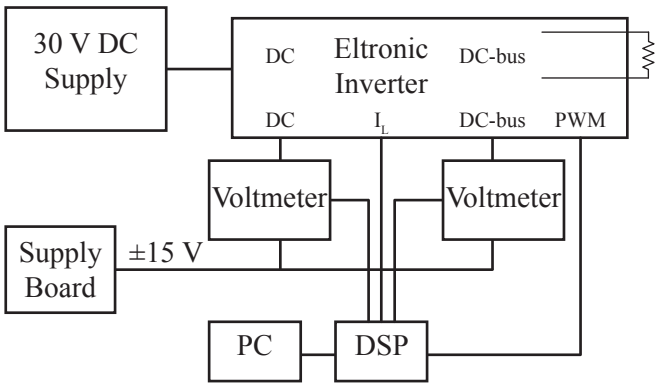

Figure 2.4: Sketch of the experimental setup for testing PWM, voltage measurement and current measurement.

2.2.2 Voltage measurement

To measure the voltage at the DC-bus, the DC input to the inverter, two voltmeter's is added to the inverter. This is done by adding two LEM modules (voltmeter's), which provides galvanic isolation between the primary and secondary side [LEM, 2012].

The LEM module is connected to the DC-bus by soldering a set of wires on to the DC-bus pins of the power module. The LEM module further need a ± 15 V supply, this is solved by using the supply board developed in an earlier project [Christiansen et al., 2014]. A similar module is used to measure the input voltage , since the ATmega chip, incorporated in the Eltronic inverter, not is programmed to measure the voltage, as intended. The measuring output of the LEM modules is read into the DSP by an ADC.

Variable resistor

The resistor across the DC-bus, mentioned, is subsequently replaced by a variable resistor. Thereby the resistance across the DC-bus is varied to test the controllers ability to sustain a constant voltage level at the DC-bus even though the resistance is changing.

2.2.3 Current measurement

The Eltronic inverter has incorporated current sensors to measure the current in each motor phase, and the input current, as described in section 2.1. The current sensor outputs a voltage proportional to the measured current. The voltage is offset by 1.5 V, to allow measurement of a negative current, and the relation between the voltage and current is defined as 33.6 mV/A. In the initial experiments only the current sensor on the input (I-SYS) [Eltronic, 2014] is used. The voltage is measured on a jumper on the inverter, directly into the DSP by an ADC.

2.2.4 Sampling between switching

When operating the PFC switch, noise is observed on the input voltage, when examined with an oscilloscope. The noise is at the same frequency and in phase with the PWM switching. To avoid measuring the disturbance from the switching, it is ensured that the measurement is done between the switching.

This is done by using the same up-down counting interrupt to trigger the PWM switching and to start the ADC conversion to measure voltage and current. The timing is sketched in figure 2.5.

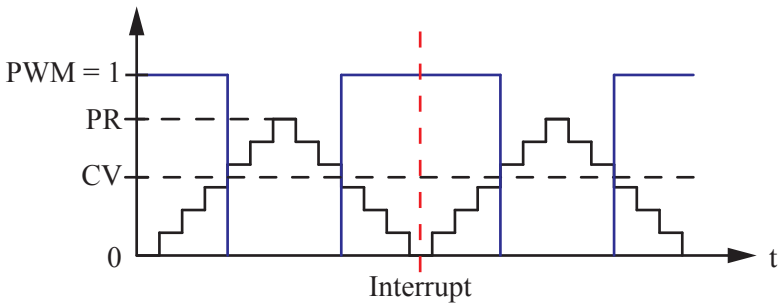

Figure 2.5: Sketch of the timing between the PWM switching and the interrupts.

The counter in the c-programme is an up-down counter, which generates an interrupt when the count is zero and the PWM switch is turned on when the count is above a certain compare value (CV). This yields the effect that the ADC is started at every interrupt and the PWM is switched on and of between the interrupts. Thereby it is avoided to measure voltage or current at the instant of time where the switch is turned on or off, and thereby the switching noise is avoided.

To determine a conservative time for the ADC to measure, the ADC is set to run continuously

and toggle an output pin on the DSP. From the output pin the period is determined with an oscilloscope to be 1.43 μ s for 1 ADC conversation.

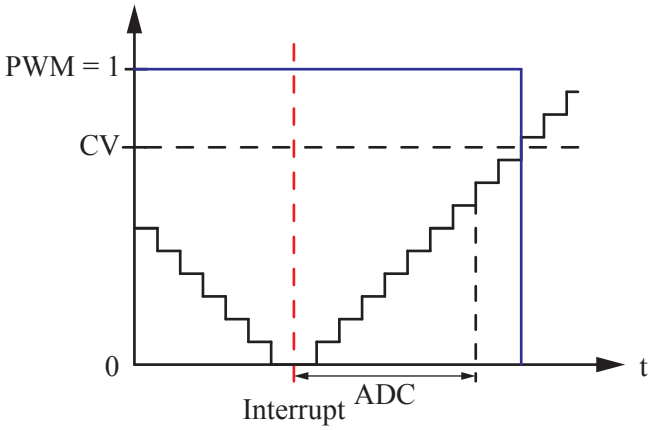

Figure 2.6: Sketch of the timing between the PWM switching and the ADC measurement.

It is desired to determine a value of the duty cycle, where the ADC exactly is through the conversion, by the time the PWM switch is switched. A minimum value for the duty cycle, to avoid measuring the switching noise.

The time value for the continuously running ADC is compared to the timebase (TB), running at the clock frequency of 150 MHz, this yields equation 2.3.

$$TB = \frac{1}{150\,\text{MHz}} = 6.67\,\text{ns} \tag{2.3}$$

It is desired to find a count of TB's equivalent to the time spent on a conversion for the ADC, see equation 2.5.

$$count \cdot TB = ADC \Rightarrow count = \frac{ADC}{TB} \tag{2.4}$$

$$count = \frac{1.43\,\mu\,\text{s}}{6.67\,\text{ns}} = 214 \tag{2.5}$$

With this number a duty cycle is determined, where the ADC is through the conversion, exactly when the PWM switch is turned on.

The Period register (PR) is 3749 in the c-program and the CV is determined as equation 2.6.

$$CV = Dutycycle \cdot PR \tag{2.6}$$

From this the duty cycle that allows the ADC to finish, before switching the PWM, is found by equation 2.7, by setting the CV to the 214 counts, found by equation 2.5.

$$Dutycycle = \frac{CV}{PR} = \frac{214}{3750} = 0.057 = 5.7\% \tag{2.7}$$

This yields that having a dutycycle below 5.7 %, may cause one of the ADC's to measure a value while the PWM is switching.

2.3 Rectifier baby board

To supply the setup by AC a rectifier is needed. Therefore a separate print board is designed to hold rectifier diodes, LEM modules for voltage measurement as discussed in section 2.2.2 and inductors for the PFC circuit. A diagram of the baby board is shown in figure 2.7.

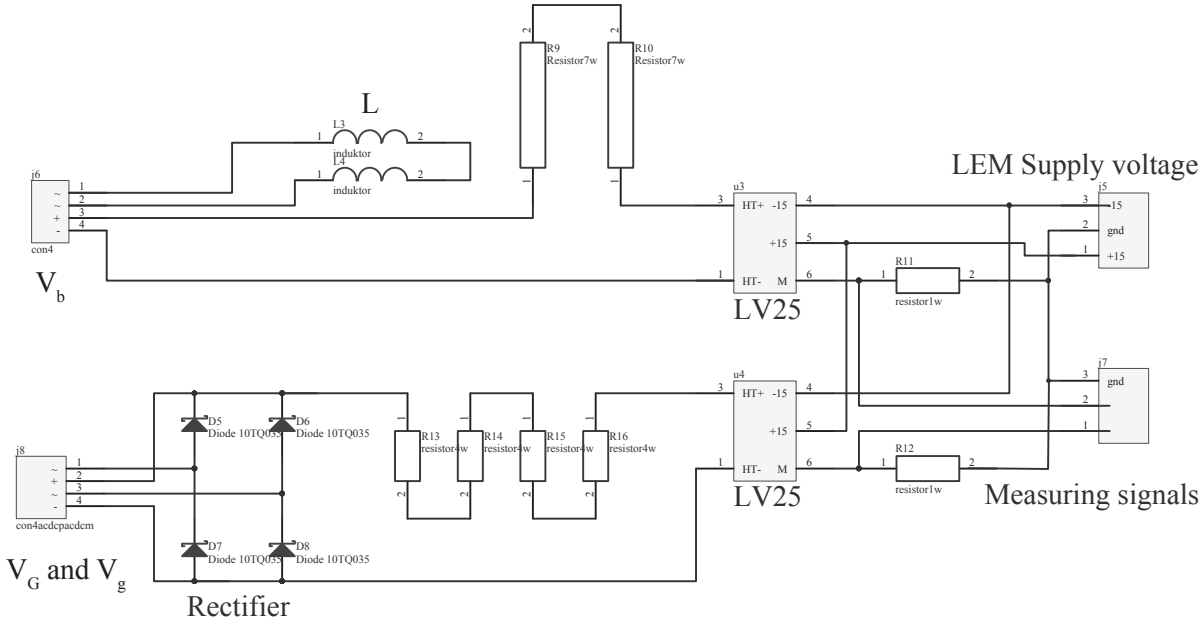

Figure 2.7: Diagram of the implemented rectifier baby board.

The inductors are placed on the board, only because the space on the inverter board is to tight to fit the two inductors reused from [Christiansen et al., 2014]. The diagram and the circuit drawing of the rectifier board is found on the annex CD.

As the hardware is described, the theory of the boost converter is examined and described in chapter 3 *Boost converter*.

Chapter 3

Boost converter

The boost converter function as a variable AC transformer, but for DC voltages. With a boost converter though, it is only possible to make a higher voltages. A electrical diagram of an ideal boost converter is shown in figure figure 3.1.

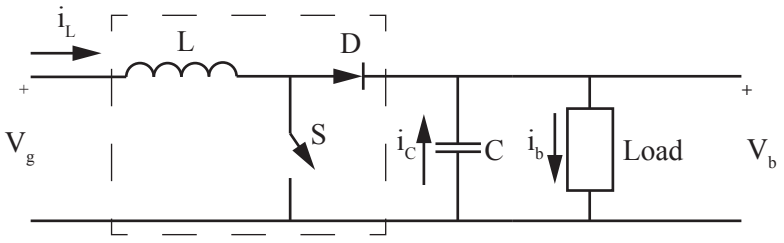

Figure 3.1: Electrical diagram of an ideal boost converter.

Where:

- V_g is the rectified grid voltage.
- V_b is the output from the boost converter i.e. boost voltage.
- S is a switch.
- i_L is inductor current.
- i_C is capacitor current.
- i_b is load current.
- Load is resistance from the inverter and motor.

The switch is assumed to switch instantaneously. This yields two electrical diagrams, one with the switch on and one with the switch off. The two diagrams are shown in figure 3.2. The inductor, switch, diode and capacitor is not considered ideal and thereby each have a resistance, as seen in figure 3.2.

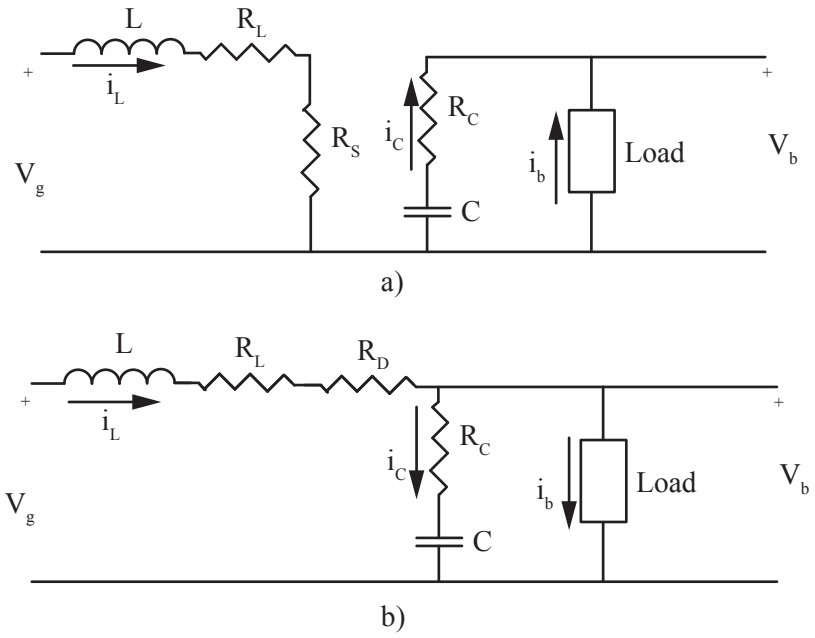

Figure 3.2: Electrical diagrams of a boost converter. a) the electrical diagram with the switch on, and b) with the switch off

In figure 3.2 a) the switch is on. Thereby the on circuit is modeled by the governing equations 3.1 to 3.4.

$$V_g = L\frac{di_L}{dt} + R_L i_L + R_s i_L \tag{3.1}$$

$$V_b = v_C + R_C i_C \tag{3.2}$$

$$i_C = -i_b \tag{3.3}$$

$$v_C = \frac{1}{C}\int i_C dt \tag{3.4}$$

The off circuit is shown in figure 3.2 b). The governing equations for the off circuit is thereby equation 3.5 to 3.8.

$$V_g = L\frac{di_L}{dt} + (R_L + R_D) i_L + V_b \tag{3.5}$$

$$i_L = i_C + i_b \tag{3.6}$$

$$V_b = v_C + i_C R_C \tag{3.7}$$

$$v_C = \frac{1}{C}\int i_C dt \tag{3.8}$$

3.1 Ideal boost converter characteristic

The boost converter is simulated with ideal components i.e. no resistance in inductor, capacitor, switch, or diode, to compare the characteristics of the ideal boost converter in [Mohan, 2003]. V_g is assumed constant during one sample time T_s. The parameters used are:

- $L = 3.6mH$
- $R_L = 0\Omega$
- $C = 2\mu F$
- $R_C = 0$
- $R_D = 0$
- $R_S = 0$
- $R_{Load} = 200$

The capacitor is set very low so it is possible to see the variations in V_b. The boost output V_b in steady state is calculated as a function of the duty cycle for the switch, as described in equation 3.12. Since an inductor is a reactive element, the net consumed energy is zero, i.e. zero net resistance over the inductor. Through equation 3.9 to 3.12 the integral of the inductor voltage is set equal to 0 over one sample time of the PWM. V_g and V_b is assumed constant over one sample time. Terms in the equations are visualised in figure 3.3.

$$0 = \int_t^{t+T_s} v_L dt = \int_t^{t+t_{on}} V_g dt + \int_{t+t_{on}}^{t+T_s} V_g - V_b dt \tag{3.9}$$

$$\Downarrow$$

$$0 = V_g t_{on} + (V_g - V_b) t_{off} \tag{3.10}$$

$$V_b t_{off} = V_g t_{on} + V_g t_{off} \tag{3.11}$$

$$\Downarrow \quad D = \frac{t_{on}}{T_s} \Rightarrow (1-D) = \frac{t_{on}+t_{off}}{t_{on}+t_{off}} - \frac{t_{on}}{t_{on}+t_{off}} = \frac{t_{off}}{t_{on}+t_{off}}$$

$$\frac{V_b}{V_g} = \frac{1}{(1-D)} \tag{3.12}$$

where:

- D is the duty cycle of the switch.
- t_{on} is the time the switch is on.
- t_{off} is the time the switch is off.
- $T_s = t_{on} + t_{off}$ is the sample time.

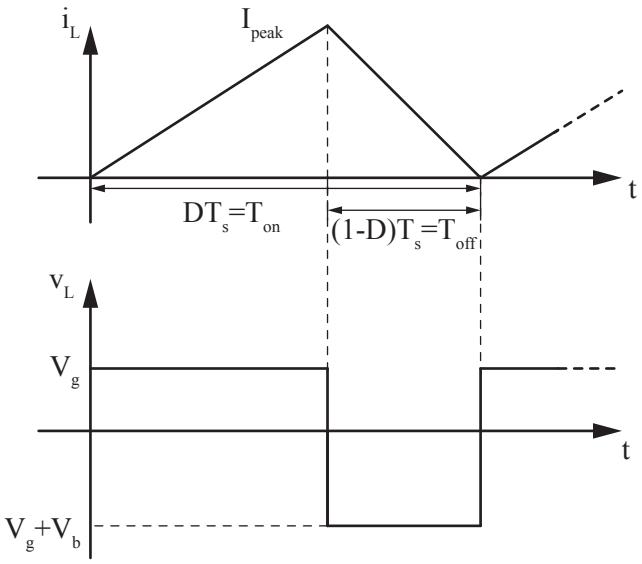

Figure 3.3: Sketch of I_L and V_L in CCM.

By assuming no power loss across the converter:

$$V_g I_L = V_b I_b \tag{3.13}$$

$$\Downarrow$$

$$\frac{I_b}{I_L} = 1 - D \tag{3.14}$$

where:

- I_L is the input current.
- I_b is the output current.

In figure 3.4, the simulated steady state results are shown, for a duty cycle of $D = 1/3$. The plotted results are; output voltage V_b, input voltage V_g, PWM signal, inductor current i_L scaled by 10, inductor voltage v_L, capacitor current i_C scaled by 10, and capacitor voltage v_C. The time axis is shifted to start at zero.

The duty cycle of $D = 1/3$, yields that the V_b is 1.5 times V_g, from accordance with equation 3.12, the PWM is furthermore seen in figure 3.4. The V_b and v_C are equal since there is not simulated any resistance in the capacitor. The V_b has a small ripple with the same frequency as the PWM signal. In the on period (high PWM signal i.e. figure 3.2 a) diagram), V_b is decreasing since the capacitor is discharging, hence the current is negative. V_b is increasing parabolic during the off time period, hence the i_C is positive and linear decreasing. i_C is positive because of equation 3.6 i.e. the stored energy in the inductor is moved to the capacitor.

The ripple of V_b (ΔV_b showm in figure 3.4) is calculated by equation 3.15.

$$\Delta V_b = \frac{1}{C}\int_0^{t_{on}} i_C dt \tag{3.15}$$

$$\Downarrow$$

$$\Delta V_b = \frac{i_C t_{on}}{C} = \frac{V_b D T_s}{R_{Load} C} \tag{3.16}$$

From equation 3.16 it is clear that there is an inverse proportionality between the size of the ripple and the terms R_{Load} and C. In simulation yielding figure 3.4 the capacitor C is chosen very small, to demonstrate the ripple. By choosing the capacitor larger, the ripple decreases.

v_L is equal to the input voltage during the on period and is $(V_g - V_b)$ during the off time, as shown in equation 3.10.

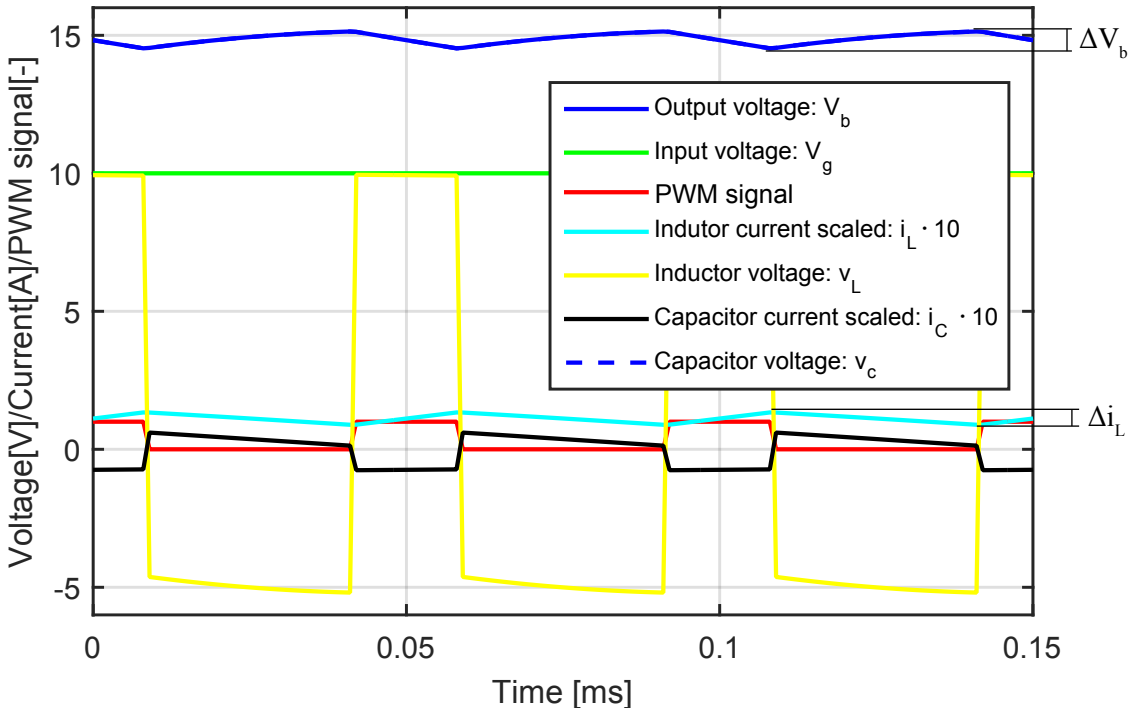

Figure 3.4: Simulation of the an ideal Boost converter

The inductor current i_L, seen in figure 3.4 is positive at all time. This is called Continuous Conduction Mode (CCM). The relation stated in equation 3.12 is only valid for CCM. In Discontinuous Conduction Mode (DCM) part of i_L is zero for a period of time. i_L can not be negative, since this would violate the principle of the diode, or the rectifier, see figure 3.1. The boundary between CCM and DCM occurs, when the mean i_L is equal to half the inductor current ripple Δi_L shown in figure 3.4. $\frac{\Delta i_L}{2}$ is calculated similarly to ΔV_b, by equation 3.18

$$I_{LB} = \frac{\Delta i_L}{2} = \frac{1}{2L}\int_0^{t_{on}} V_g dt \tag{3.17}$$

$$\Downarrow$$

$$I_{LB} = \frac{\Delta i_L}{2} = \frac{V_g t_{on}}{2L} = \frac{V_b(1-D)DT_s}{2L} \tag{3.18}$$

Where:

- Δi_L is the peak to peak deviation of i_L
- I_{LB} is the average inductor current at the boundary between CCM and DCM

Permanent CCM is desired, the size of the inductor, the value of L and T_s, is crucial to ensure this, seen by equation 3.18. The DSP is capable of performing PWM at 20 kHz, which yields a $T_s = \frac{1}{20kHz} = 0.05ms$. Therefore examinations are performed to determine a desirable value of L. Practically this is done by examining the limit between CCM and DCM.

Realising that the inductor current i_L and the input current i_g is the same, isolating I_L in equation 3.14, and substituting for I_{LB} in 3.18. This which yields an expression for the average of the output current i_b, for operation at the boundary between CCM and DCM see equation 3.19.

$$I_{bB} = \frac{T_s V_b D(1-D)^2}{2L} \tag{3.19}$$

Where:

- I_{bB} is the average output current at the boundary between CCM and DCM.

Equation 3.18 and 3.19 are plotted in figure 3.5 with respect to the duty cycle, and with the following constants:

- $V_b = 420\,\mathrm{V}$
- $L = 3.6\,\mathrm{mH}$
- $T_s = 0.05\,\mathrm{ms}$ equivalent to $20\,\mathrm{kHz}$

In reality V_b is not going to be constant, but oscillate. The average of the voltage is referred to as V_b in the further description.

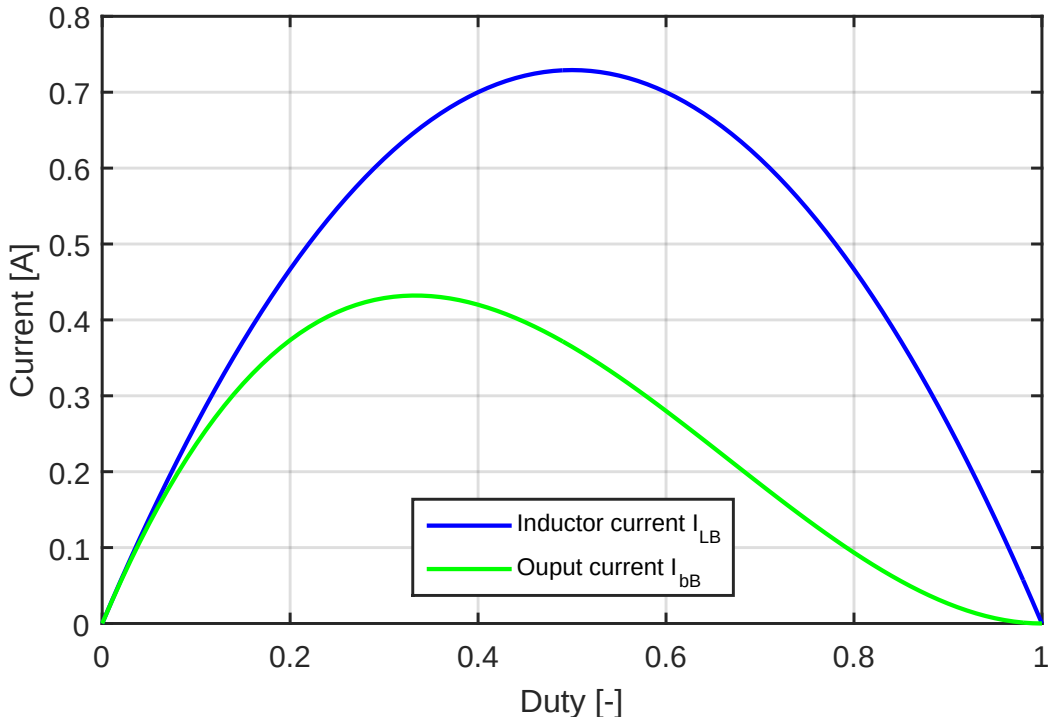

Figure 3.5: Blue is the inductor current and green is the output current respectively, at the boundary between CCM and DCM.

As seen by figure 3.5 there is a crusial point at $D = 1/3$, where the demand of current, that ensures CCM is highest. Since the boost converter is going to drive a AC motor through an inverter. It is interesting to examine the power demand at the boundary between CCM and DCM, to make sure that the AC motor draws more power than the power demand, and thereby ensuring CCM. The output power of the boost converter $P_B = V_b I_{bB}$, is calculated from equation 3.20, rewritten from equation 3.19.

$$P_B = \frac{T_s V_b^2 D(1-D)^2}{2L} \Rightarrow L = \frac{T_s V_b^2 D(1-D)^2}{2P_B} \tag{3.20}$$

V_g is varying as a rectified grid voltage, which causes D to vary. Isolating D in equation 3.12 and inserting in equation 3.20, the equation becomes a function of V_g, and the equation becomes:

$$P_B = \frac{T_s \left(1 - \frac{V_g}{V_b}\right) V_g^2}{2L} \Rightarrow L = \frac{T_s \left(1 - \frac{V_g}{V_b}\right) V_g^2}{2P_B} \tag{3.21}$$

The equations 3.20 and 3.21 are plotted in figure 3.6. Note that the power P_B in the figures, is the power demand, to avoid DCM. The maximum P_B with respect to D is at $D = 1/3$.

By inserting the approximately constant boost voltage $V_b = 420\,\mathrm{V}$, a peak is observed at $V_g = 280\,\mathrm{V}$, determined by equation 3.12, as 3.22.

$$V_g = V_b \cdot \frac{2}{3} \tag{3.22}$$

By plotting for a number of power levels, the only variable left is the inductance. Therefore the plots in figure 3.6 shows the minimum required inductance, that ensures CCM at the plotted power level.

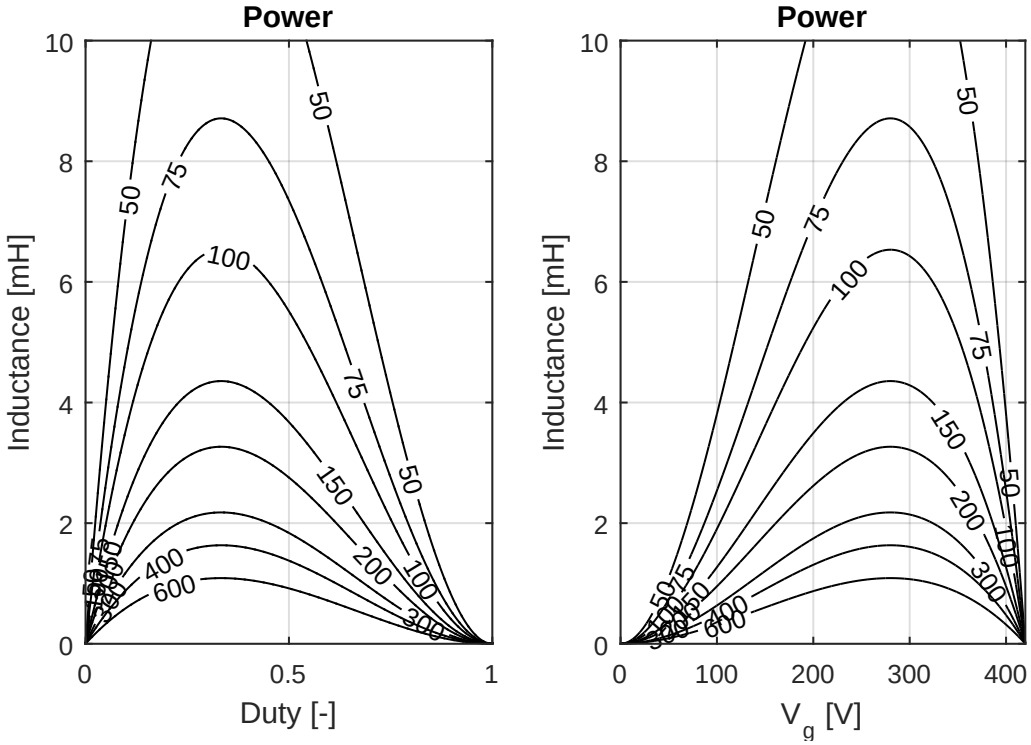

Figure 3.6: a) Plot of the minimum required inductance to ensure CCM (limit of CCM and DCM), at a number of power levels, as a function of the duty cycle. b) Plot of the minimum required inductance to ensure CCM (limit of CCM and DCM), at a number of power levels, as a function of V_g.

From [Christiansen et al., 2014] the same DACS AC motor is used on similar setup but with a different fan, the power drawn is 538 W, at $97.4 rad/s \approx 930 RPM$ it is assumed that the new fan of the same magnitude of power usage. From equation 3.21 (or figure 3.6), the minimum inductance for $P_B = 538\,\mathrm{W}$ is $L_{min} \approx 1.2mH$. A 3.6 mH inductor is available, and is chosen, hence the power demand required to ensure CCM then is calculated to $P_B \approx 180W$.

In figure 3.7 i_L and v_L is sketched in DCM. i_L is rising during the on period, similar to CCM. During the off period $(\Delta_1 T_s + \Delta_2 T_s)$ i_L is decreasing in the time $\Delta_1 T_s$, reaches zero, and remain

zero in the time period $\Delta_2 T_s$. In the $\Delta_2 T_s$ period, the voltage drop over the inductor is also zero, since i_L has zero slope.

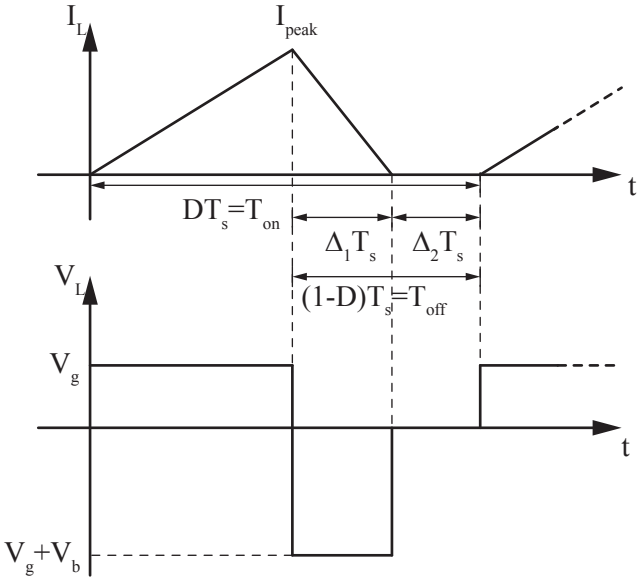

Figure 3.7: Sketch of I_L and V_L in DCM.

Integrating the inductor voltage drop over T_s must also be zero for DCM as for CCM, shown in equation 3.23 and 3.24, similar to equation 3.9 through to 3.12. As $\Delta_1 T_s < T_{off}$, V_b is larger in DCM than in CCM for a given duty cycle.

$$0 = \int_t^{t+T_s} v_L dt = \int_t^{t+DT_s} V_g dt + \int_{t+DT_s}^{t+DT_s+\Delta_1 T_s} (V_g - V_b) dt + 0 \tag{3.23}$$

$$\Downarrow$$

$$0 = V_g D T_s + (V_g - V_b)\Delta_1 T_s \tag{3.24}$$

$$V_b \Delta_1 T_s = V_g D T_s + V_g \Delta_1 T_s; \text{ compare to equation 3.11} \tag{3.25}$$

$$\Downarrow$$

$$\frac{V_g}{V_b} = \frac{\Delta_1}{\Delta_1 + D} \tag{3.26}$$

The energy transferred from the grid to the capacitor and the load is determined in equations 3.27 through to 3.29, the transferred power (described by $V_g \cdot i_L$) is integrated over the time t_{on}. Note that the I_{peak} is given by $2I_{LB}$, described by equation 3.18, this yields equation 3.30.

$$P = V_g i_L \tag{3.27}$$

$$\Downarrow$$

$$\int_0^{t_{on}} P dt = V_g \int_0^{t_{on}} i_L dt \tag{3.28}$$

$$\Downarrow \text{ Note that } i_L \text{ increases linearly to } I_{Lpeak} \text{ at } t_{on}$$

$$P t_{on} = V_g \frac{I_{Lpeak}}{2} t_{on} \tag{3.29}$$

$$\Downarrow \text{ From equation 3.18} I_{Lpeak} = \frac{V_g t_{on}}{L}$$

$$P t_{on} = \frac{(t_{on} V_g)^2}{2L} \tag{3.30}$$

The energy that is not absorbed by the load, is used to rise the capacitor voltage. For a load, sufficiently small, the capacitor voltage keeps increasing, and may cause damage to the capacitor [Mohan, 2003]. This is yet another reason to minimise the time, where the boost converter operates in DCM.

Parasitic elements
In the previous it is assumed that the components are ideal. In reality there are parasitic elements in the form of resistance. This resistances has the effect that when the duty cycle approaches 1, V_b will start to diverge equation 3.12. By having a voltage than the ideal described in equation 3.12. V_b will even starts to drop [Mohan, 2003].

3.2 Calibration and validation of boost converter model

The model is verified, with the intention to use the model for controller design. The model is verified first by first by comparison of the a DC V_g and then with AC voltage.

DC calibration and validation of boost converter model

The simulations constants is found in the following data sheets [Rectifier, 2013], [Chemi-con, 2013] and [Bourns, 2013]. The constants are:

- $L = 3.6mH$
- $R_L = 0.36\Omega$
- $C = 90\mu C$
- $R_C = 0\Omega$
- $R_D = 5\Omega$
- $R_S = 5\Omega$

The V_g is set to 10 V. In figure 3.8 the simulation result is shown to the left and the measured result to the right with the same duty cycle. The measurement is done done with an oscilloscope. The measured result shows some switching noise, which is not simulated, otherwise the model and the simulation show similar response for a DC V_g.

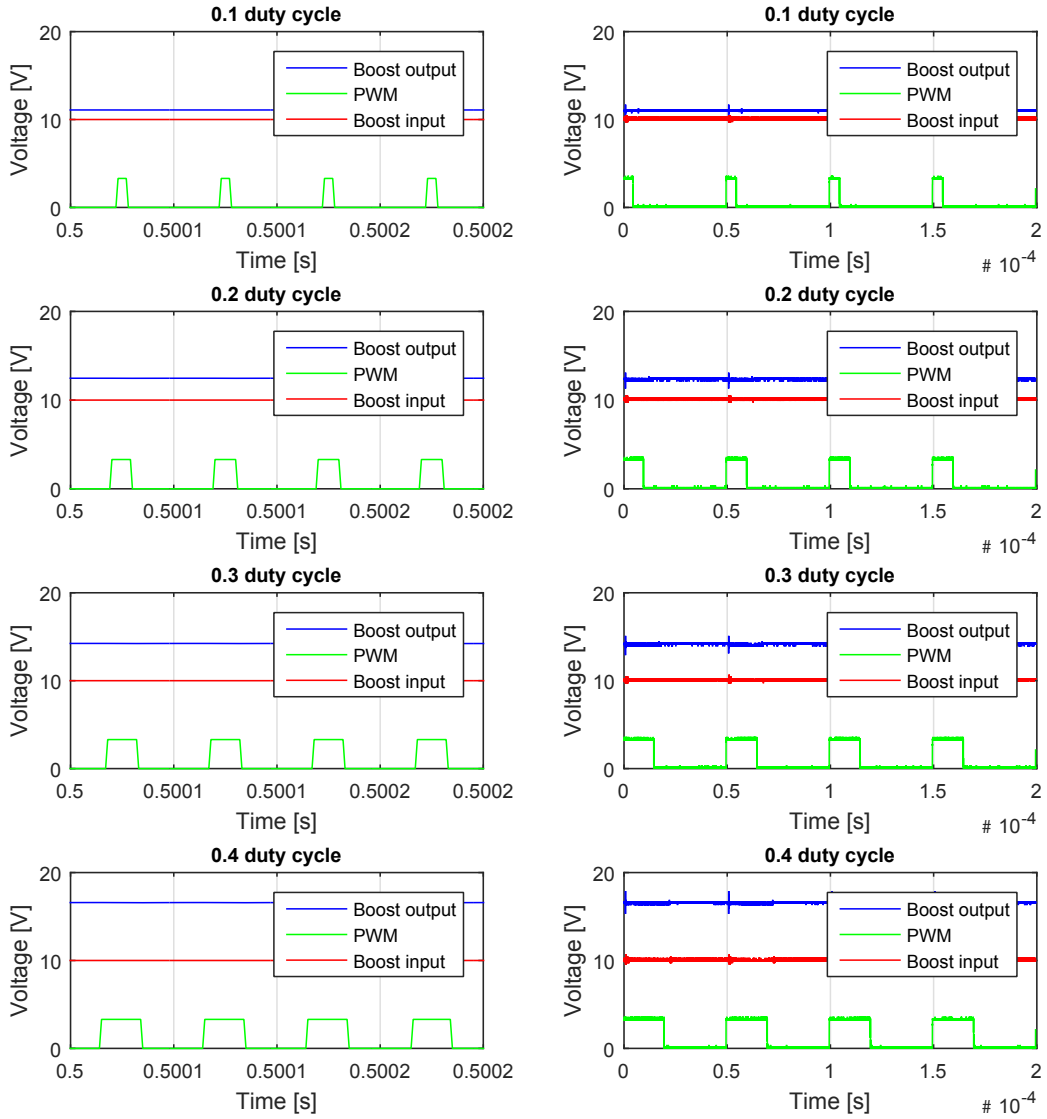

Figure 3.8: Simulation results with DC input voltage, with different duty cycles.

AC calibration and validation of boost converter model

In the following the v_g is the input voltage to the boost converter, as the input is now varying. The verification is done with recertified AC voltage on v_g, with a rms value of 245 V. This is also the order of magnitude of v_g the boost converter will function in ($230V10\% = 253$). The model is verified with a constant duty cycle. To isolate the boost converter from the grid, a 1:1 transformer is implemented, likewise a variable transformer in implemented to be able to

change the input voltage. v_g, v_b and i_L is measured by an oscilloscope.

- $L = 3.6mH$
- $R_L = 0.36\Omega$
- $C = 90\mu C$
- $R_C = 0\Omega$
- $R_D = 5\Omega$
- $R_S = 5\Omega$

The boost converter is tested with a constant duty cycle of 0.1. Comparing the model with the measured results yields figure 3.9, notice that the time scale is the same in the three figures. The top left figure is the input voltage v_G, much more dynamics is observed in the measured grid voltage, than on the simulated grid voltage. This indicates that the grid voltage has a large inductor. In the top right figure the output voltage v_b is shown. The ripple of v_b is the same for both the measurement and the simulated. This indicates that the capacitor has the right size in the model. The noise that is grater during the rising period of v_b is assumed to be measurement noise because it coincides with the grid current peak, which is seen on the bottom figure. The simulated grid current has a larger peak than the measured grid current. A larger inductor will smoothen the grid current and thereby yield a smaller peak current.

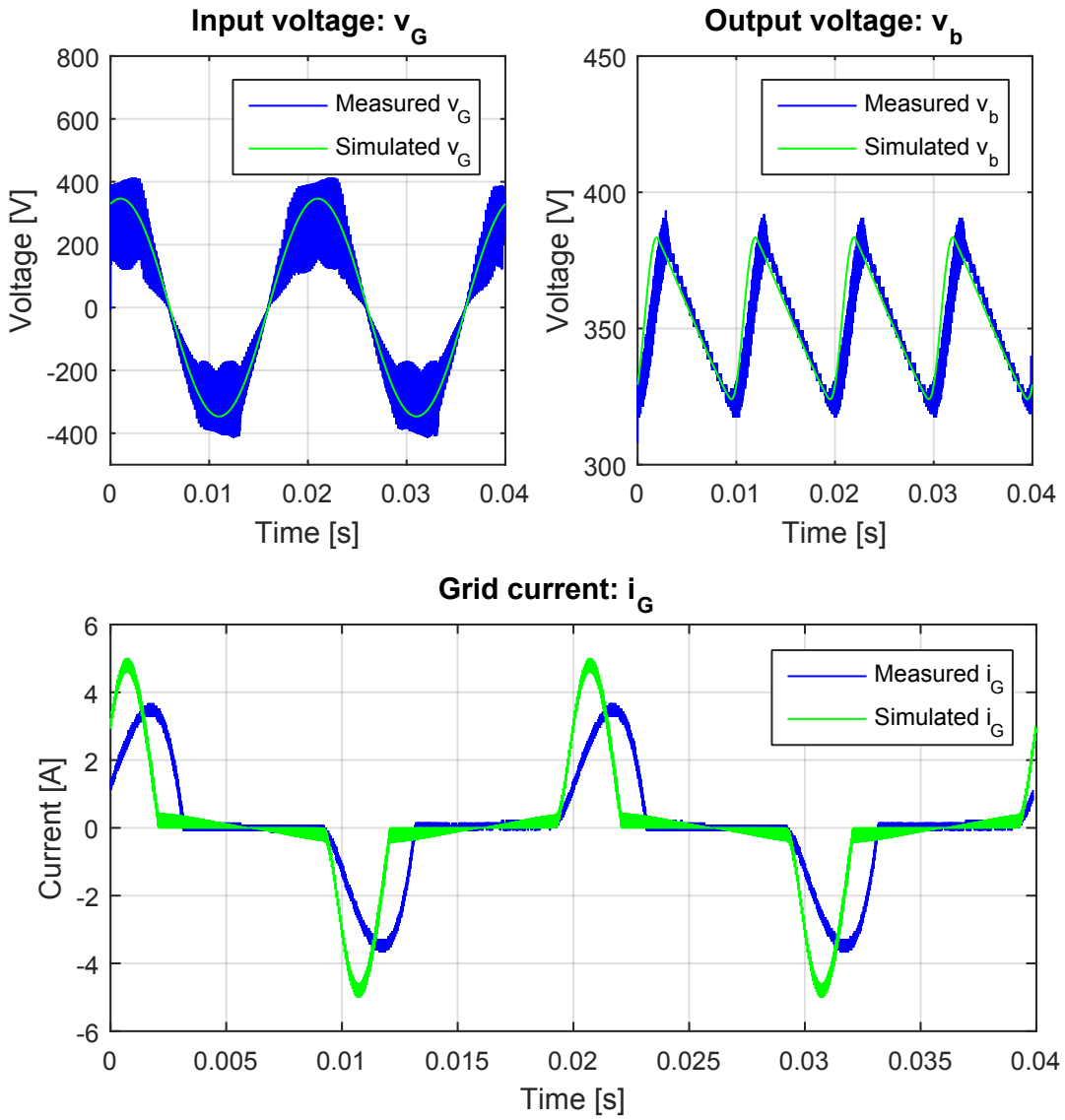

Figure 3.9: Top left figure, the input voltage v_G to the boost converter is shown. Top right figure, the output voltage v_b of the boost converter is shown.Bottom figure, the current over the inductor is shown. Blue is the measurement and green is the simulation.

The inductor L is measured, the measured inductance is 5.2 mH. The simulated result, with the new parameter is shown in figure 3.10. The change in current is from a peak of 5 A, with the 3.6 mH inductor, to 4.75 A, with the 5.2 mH inductor, but the T_{peak} is greater with the 5.2 mH, but there is not much difference . The slope of the rise time of the simulated v_b is lower and closer to the measured v_b. This is because of the larger T_{peak} of the current i.e. v_b only rises when there is drawn power from the grid, i.e. when the i_G is different from zero.

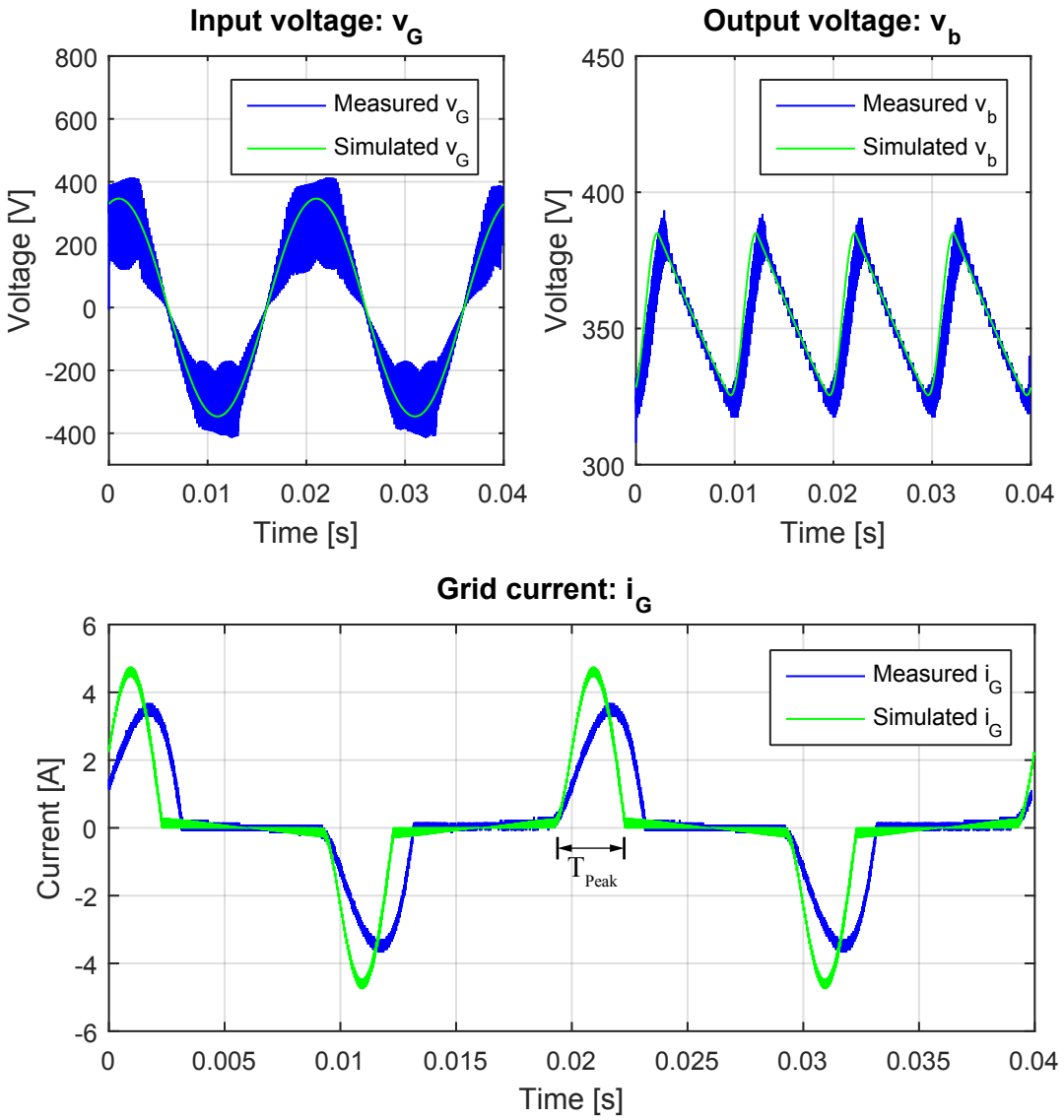

Figure 3.10: Top left figure, the input voltage v_G to the boost converter is shown. Top right figure, the output voltage v_b of the boost converter is shown.Bottom figure, the current over the inductor is shown. Blue is the measurement and green is the simulation.

The dynamics of v_G origins from the inductors in the 1:1 and variable transformer. In figure 3.11 a) the inductance from the 1:1 and the variable transformer is represented by L_G (grid inductor). For ease of implementation in the model, it is assumed that figure 3.11 a) and b) are equal, though this not true. Using figure 3.11 b) v_g is calculated in equation 3.31

$$v_g = |v_G| - L_G \frac{di_G}{dt} \tag{3.31}$$

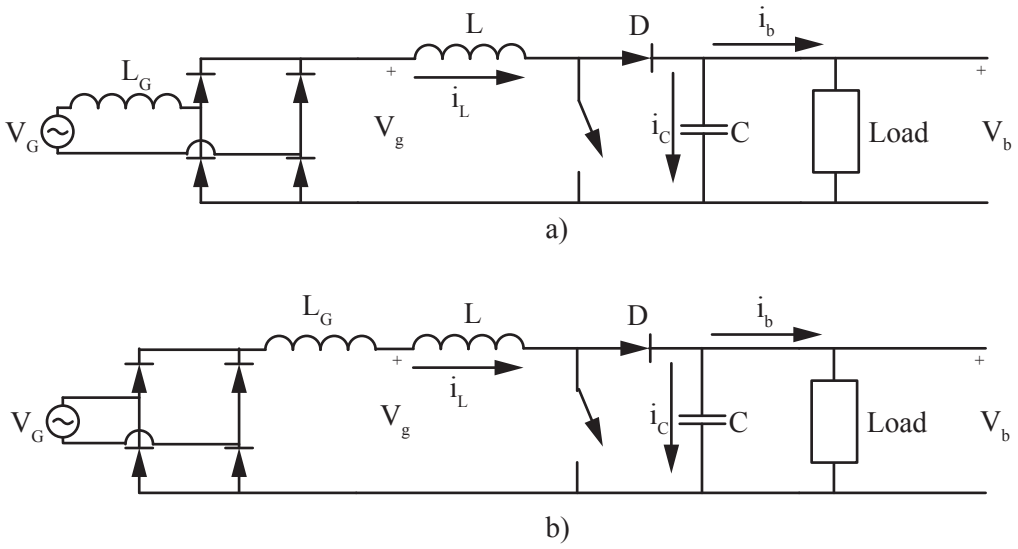

Figure 3.11: Electrical diagram of boost converter with rectifier and grid inductance L_G. In a) L_G is before the rectifier similar to reality, and b) L_G is after the rectifier similar to the model.

Tuning the L_G parameter to 11 mH yields figure 3.12. There is a large ripple on the v_g due to the inductor. In areas where v_g crosses zero. The large sudden vertical shift in the dynamics, which does not a occur in the measurements, is due to the assumption made in figure 3.11. The current i_G and voltage v_b in figure 3.12 are fitted satisfactory.

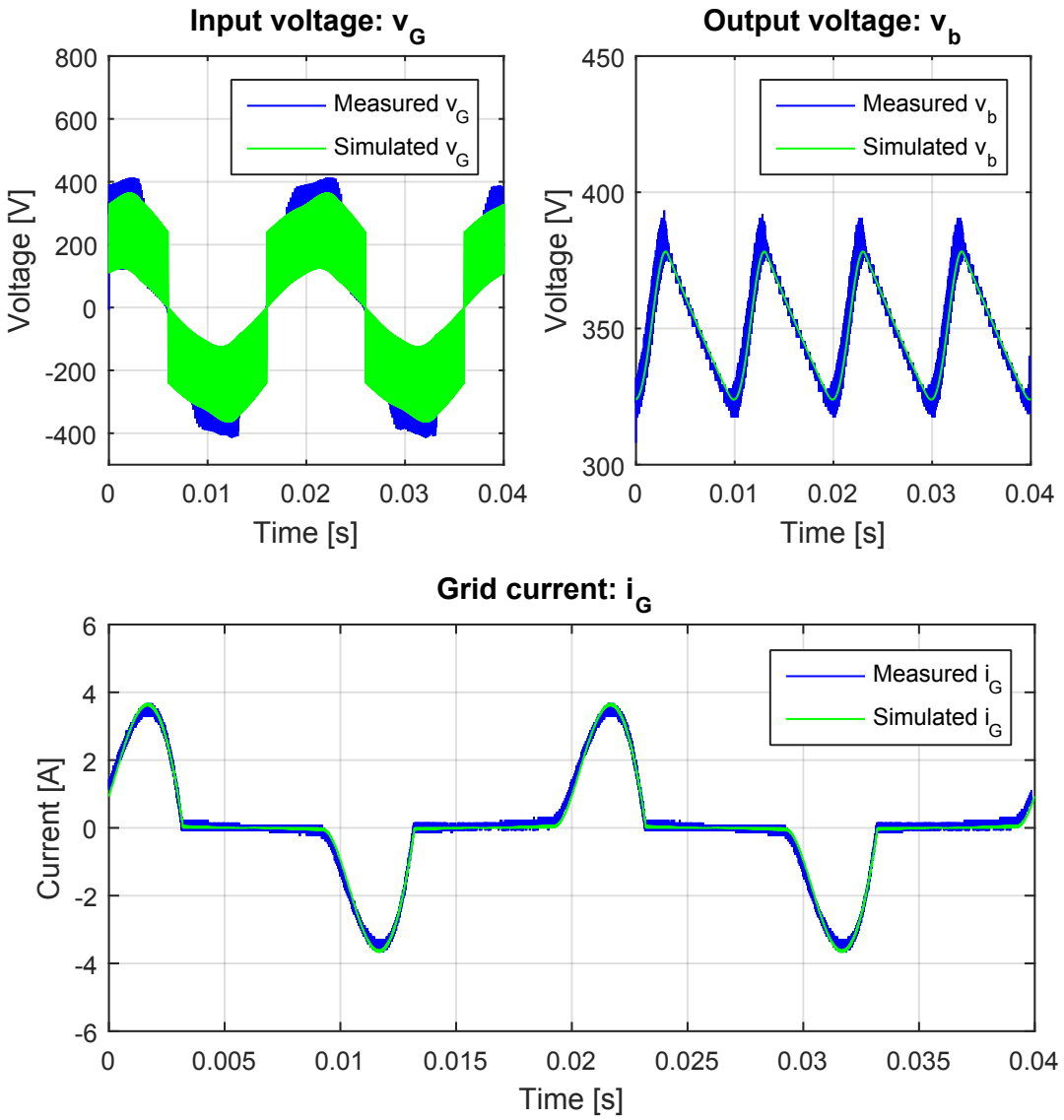

Figure 3.12: Top left figure, the input voltage v_G to the boost converter is shown. Top right figure, the output voltage v_b of the boost converter is shown.Bottom figure, the current over the inductor is shown. Blue is the measurement and green is the simulation.

To verify the model, the measurement and simulation is run again with a duty cycle of 0.35. In figure 3.13 the simulations and measurement results are shown. The simulated results are again seen to fit the measured results satisfactory, with the simulation parameters:

- $L = 5.2mH$
- $L_G = 11mH$
- $R_L = 0.6\Omega$
- $C = 90\mu C$

- $R_C = 0\Omega$
- $R_D = 5\Omega$
- $R_S = 5\Omega$

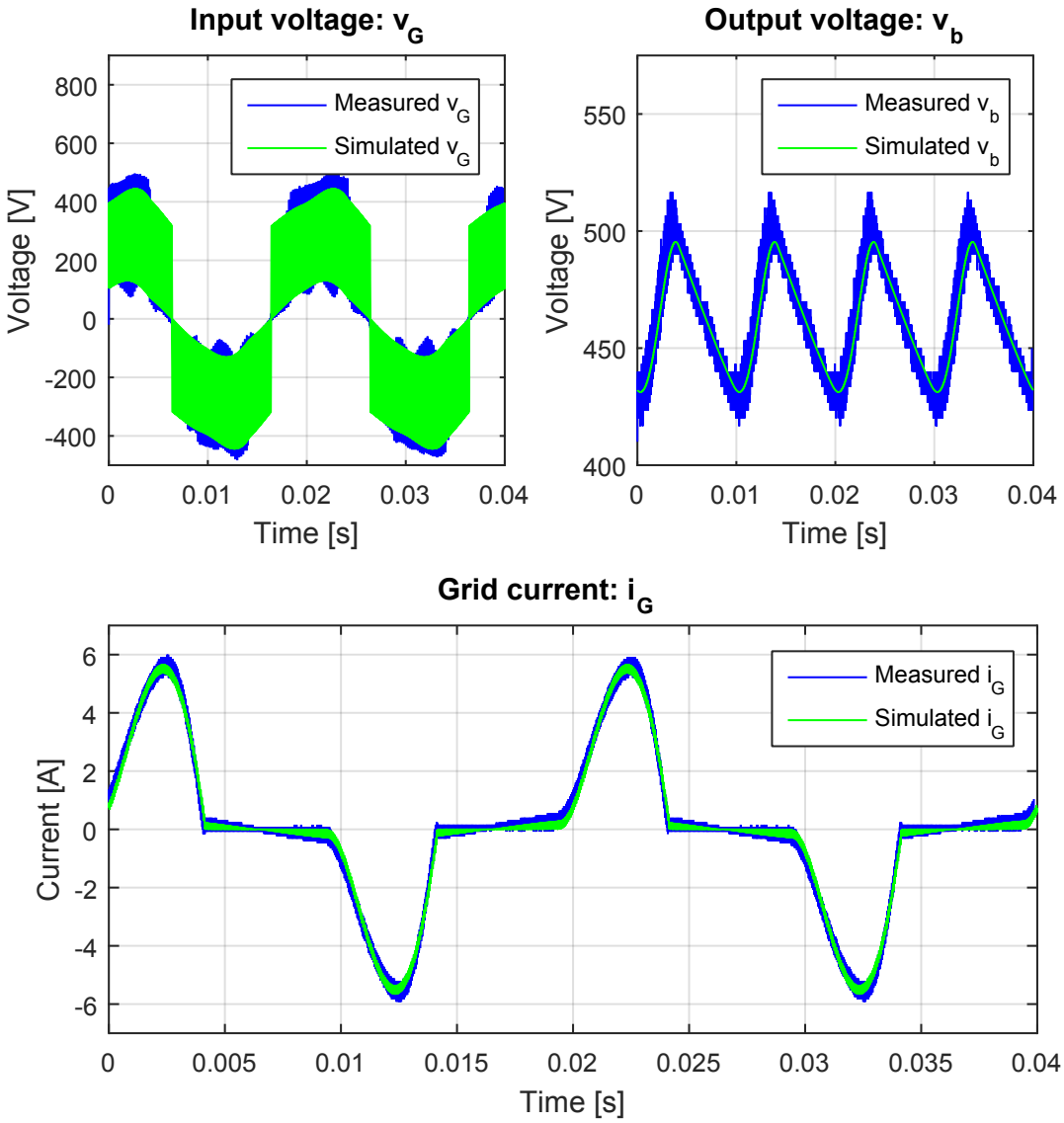

Figure 3.13: Top left figure, the input voltage v_G to the boost converter is shown. Top right figure, the output voltage v_b of the boost converter is shown.Bottom figure, the current over the inductor is shown. Blue is the measurement and green is the simulation.

3.3 Controller design for PFC

Using a boost converter with rectified grid voltage as input, operating at a constant duty cycle, yields a narrow current ripple, as seen in figure 3.13. This narrow current ripple is undesirable,

as it causes all the power drawn by the boost converter, to be drawn in short time periods, yielding a high peak current. The current ripple occur when the capacitor is being charged. A passive method to reduce the current ripple is to enlarge the inductor. This approach will result in a higher DC resistance with the inductor i.e. greater loss, further a larger inductor adds cost and unnecessary weight to the boost converter. The large inductor is therefore not considered further.
It is possible to widen the current ripple by varying the duty cycle, and thereby getting a sinusoidal response. This is called Power Factor Correction PFC. The control structure implemented to use PFC is shown in figure 3.14 [Erickson, 2004].

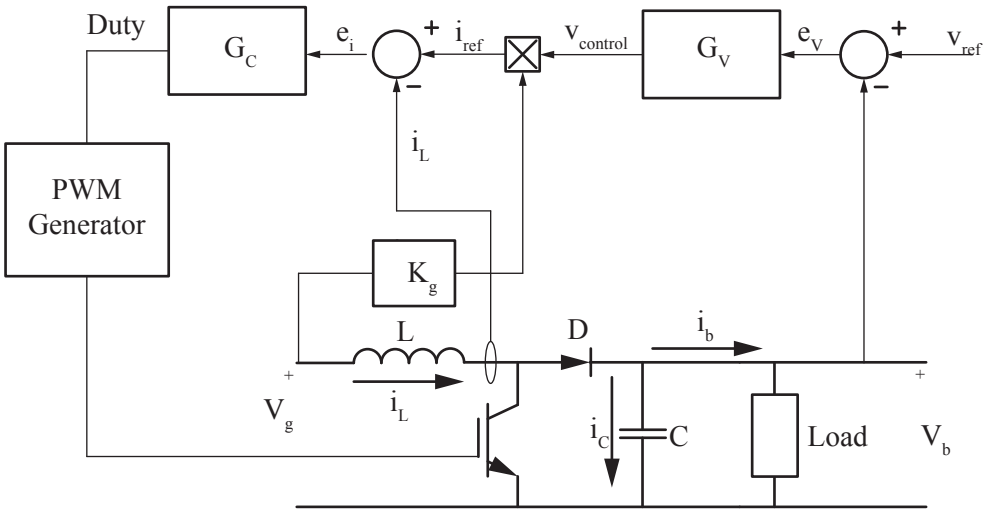

Figure 3.14: Control structure for boost converter with PFC.

In figure 3.14 the boost converter is shown in the bottom, and the control structure above. The control signals are represented by thinner lines. There are 2 controllers, G_v and G_c. The purpose of G_v is to dampen the ripples that are present in v_b and allow v_{ref} to change. A low Pass filter (PI controller) is chosen for G_v. The break frequency is chosen to be half the frequency of v_g, which is 100 Hz i.e. $200\pi\frac{rad}{s}$, as this also is the frequency present in v_b. Thereby the break frequency is $200\pi\frac{rad}{s}$. Through simulations, the gain of 1/500 for the G_v is found to be sufficient, lower gain yields slow response, both for reaching steady state and adapting to disturbances from the ventilator. A larger gain results in a larger ripple on the control output of G_v ($v_{control}$). Equation 3.32 shows the transfer function for G_v. The signal ($v_{control}$) is limited to be positive, as a negative $v_{control}$ would result in a negative reference for the current controller.

$$G_v = \frac{K_{P,v}s + K_{I,v}}{s} \tag{3.32}$$

where:

- $K_{P,v} = \frac{1}{500}$
- $K_{I,v} = \frac{100\pi}{500}$

This does not represent the system bandwidth at The controller is tuned through numerical experiments. The bode plot of the controller G_v is shown in figure 3.15.

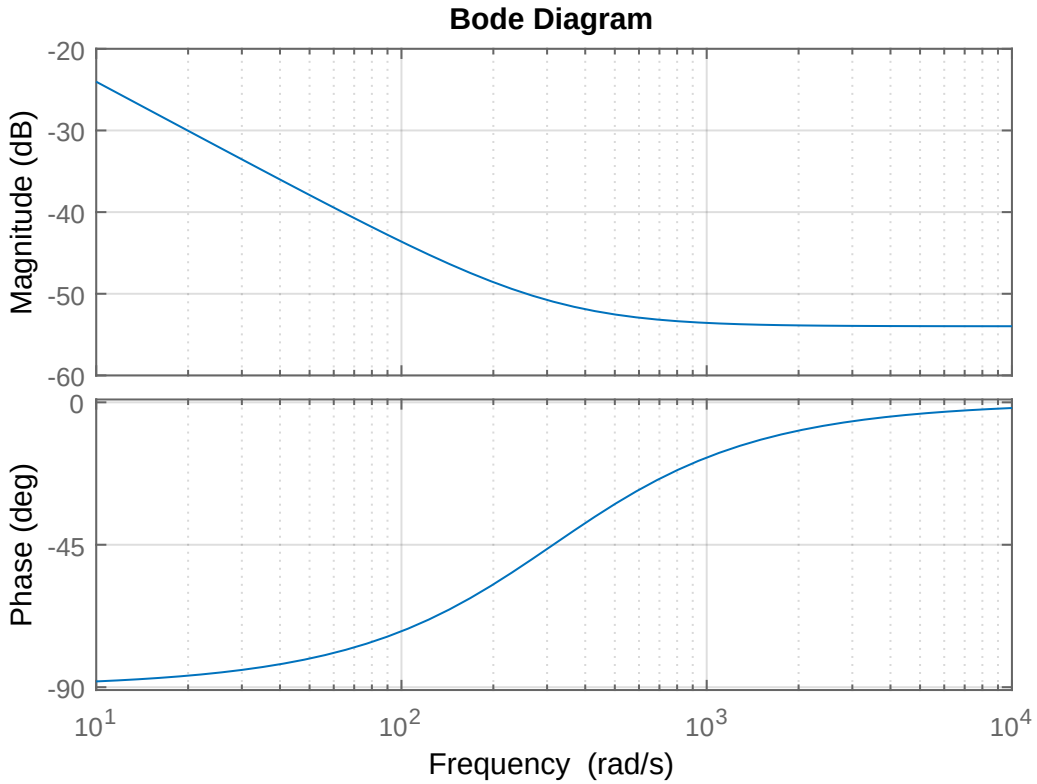

Figure 3.15: Bode plot for the PI voltage controller G_v.

Since a ripple is present in v_b the output of G_v is not perfectly constant, even though v_{ref} is constant.

3.3.1 Control of the inductor current

The current is desired to have the same characteristic as v_g i.e. numerical sine wave. By multiplying the output of G_v ($v_{control}$) with v_g (scaled), a reference for the current controller is found. v_g is normalized to be a maximum of 1, i.e. for grid voltage the K_g is $\frac{1}{230 \cdot \sqrt{2}}$. This constitutes a feed forward controller. The reference signal i_{ref} is thereby ensured to be a numerical sine wave with the same frequency as v_g and a satisfactory controller will have a power factor PF close to 1. A P controller is chosen, the P controller is tuned through simulations. By plotting the maximum value of i_L, figure 3.16 is obtained. The performance of the current controller is evaluated from figure 3.16, as the P gain that yields lowest peak

current, is seen as the optimal gain and the PF is checked after words . It is clear that the optimal P gain is at $K_g = 0.9$.

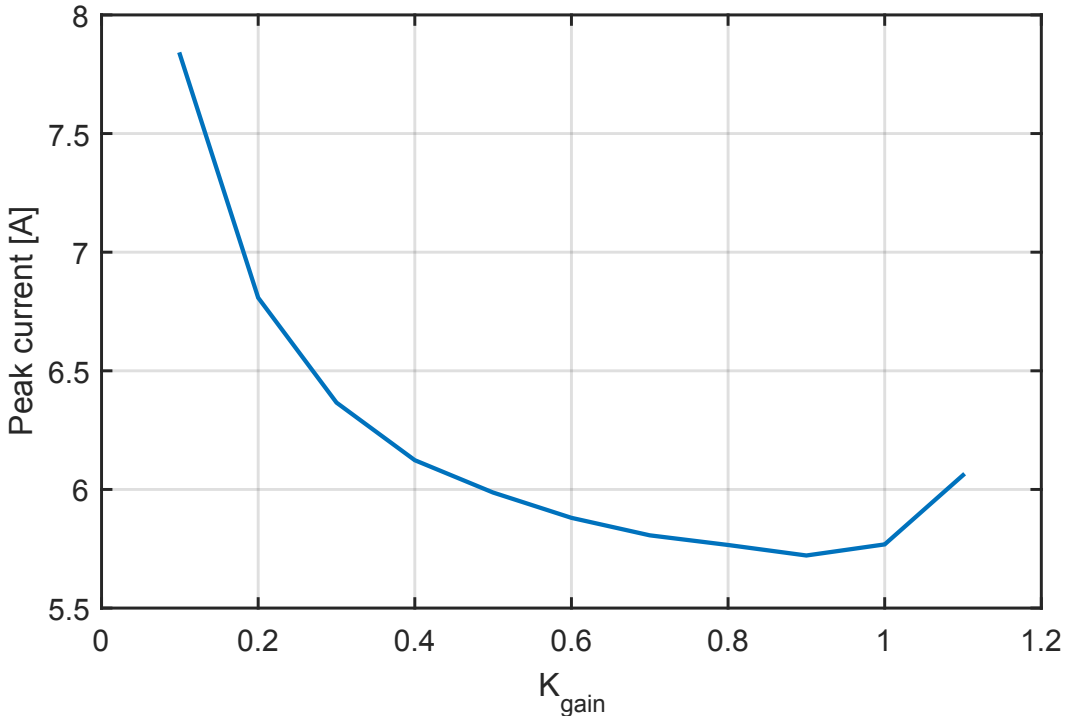

Figure 3.16: Maksimum current for Different values of P controller gain.

In figure 3.17, results of the simulation with the optimal gain $K_g = 0.9$ is shown. The plotted results are; the simulated current, duty cycle and v_g (scaled to fit the amplitude of the current). There is a significant improvement of the current characteristic, compared to the current in figure 3.13.

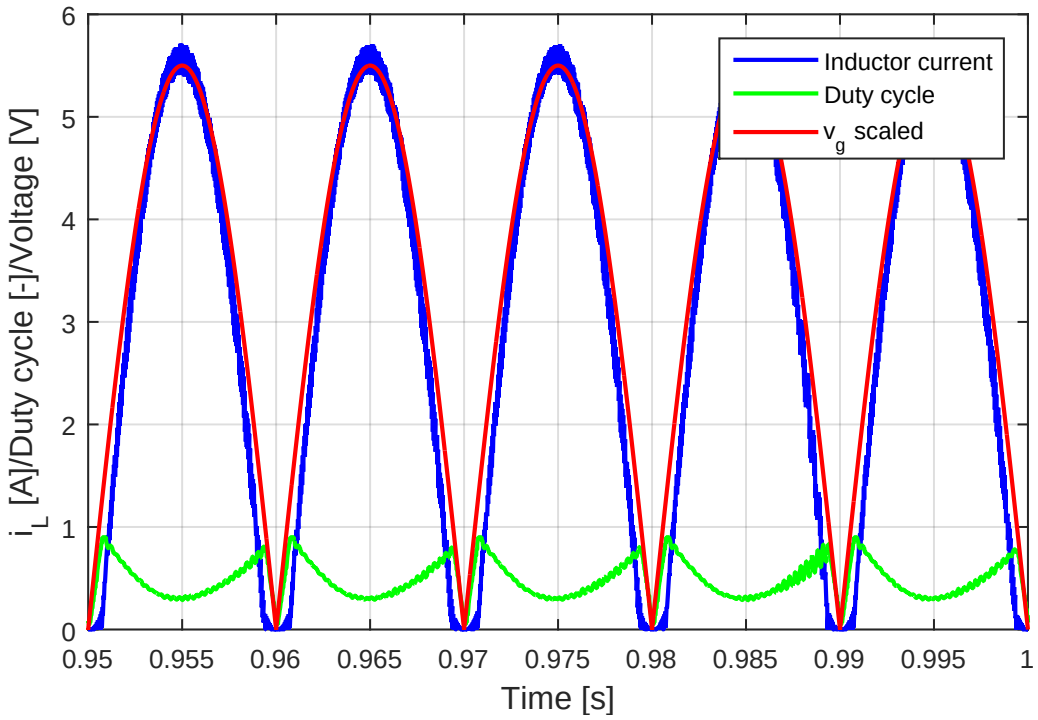

Figure 3.17: The simulated results with the optimal P controller. v_g is scale to fit the amplitude of the current

The peak time T_{peak} for i_L, shown in figure 3.10, is increased by implementing the controller. Despite that, there is still a period of time where the current is zero. This is partly due to the voltage v_g being too small to be boosted high enough to charge the capacitor, and partly due to the duty cycle being small during part of this period. The duty cycle is low, due to the reference signal e_i being low.

The controllers are implemented on the boost converter, with at 230 Ω resistor as R_{load}, which yields a power consumption of $P_b = \frac{v_b^2}{R_{load}} = \frac{400V^2}{230\Omega} = 767W$. It proved through experiments impossible to use the P controller a gain at 0.9, as the duty is fluctuated between the limits. The controller were tuned down to 0.3, the measured grid current is shown in figure 3.18.

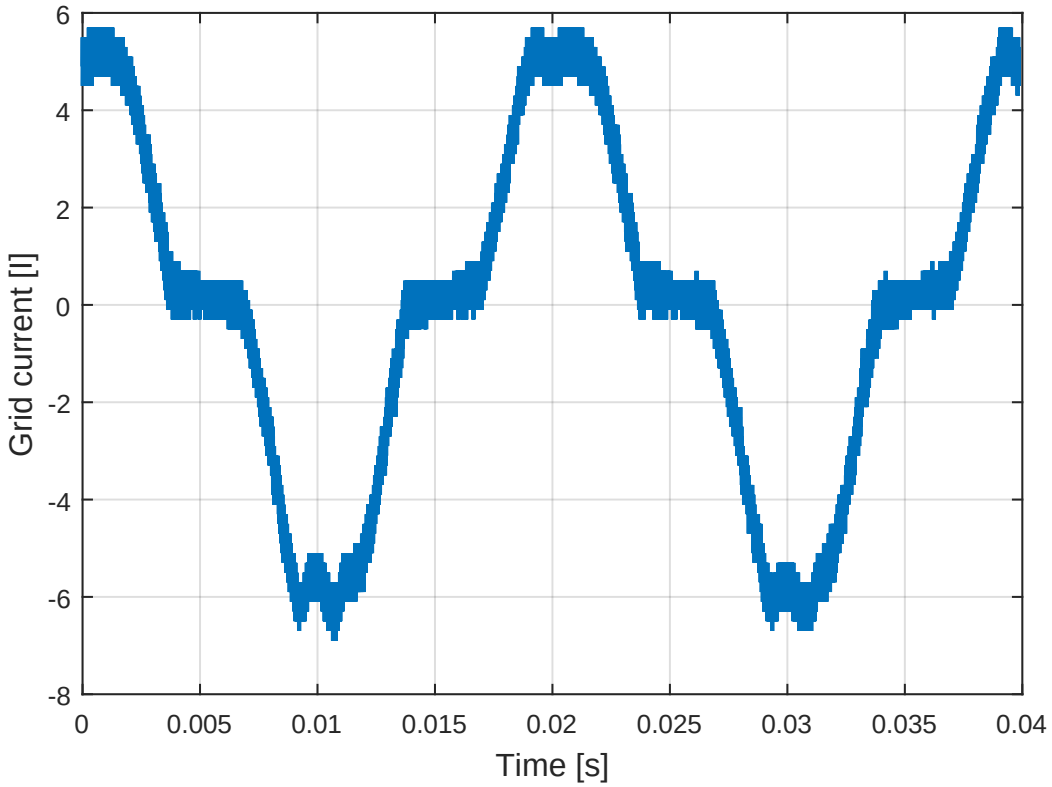

Figure 3.18: The measured I_G with P controller gain at 0.3.

A very large period, where the grid current is zero is observed. This period is unacceptably large, and due to the undesirable duty cycle characteristic observed in figure 3.17, another controller is examined, to implement as G_C, and substitute the P controller.

I-Lead current controller

The P controller is replaced with the controller shown in equation 3.34 [Martins and Cardoso, 2012].

$$G_c = \frac{1}{s}\frac{k_g(s+\omega_z)}{s+\omega_p} \tag{3.33}$$

$$\Downarrow \qquad k_g = k_{g,1}\omega_p$$

$$G_c = \frac{1}{s}\frac{k_{g,1}\omega_p(s+\omega_z)}{s+\omega_p} \tag{3.34}$$

Where:

- ω_z is the zero.

- $\omega_p = \omega_z 10$ is the pole placed one decade greater than ω_z.
- $k_{g,1}$ is the gain at ω_z frequency.

The of the ω_p is to further dampen switching noise. Excluding ω_p, the control is similar to a PI controller. Two tunings tunings parameters are present, $k_{g,1}$, and ω_z. The performance of the controller is again evaluated, by seeking the lowest peak of i_L. In figure 3.19, a contour plot showns the peak currents, as a function of the gain parameters of the boost controllers. The simulation is performed with a v_g of 230 V RMS, a $v_b = 420V$ and $R_{Load} = 230$.

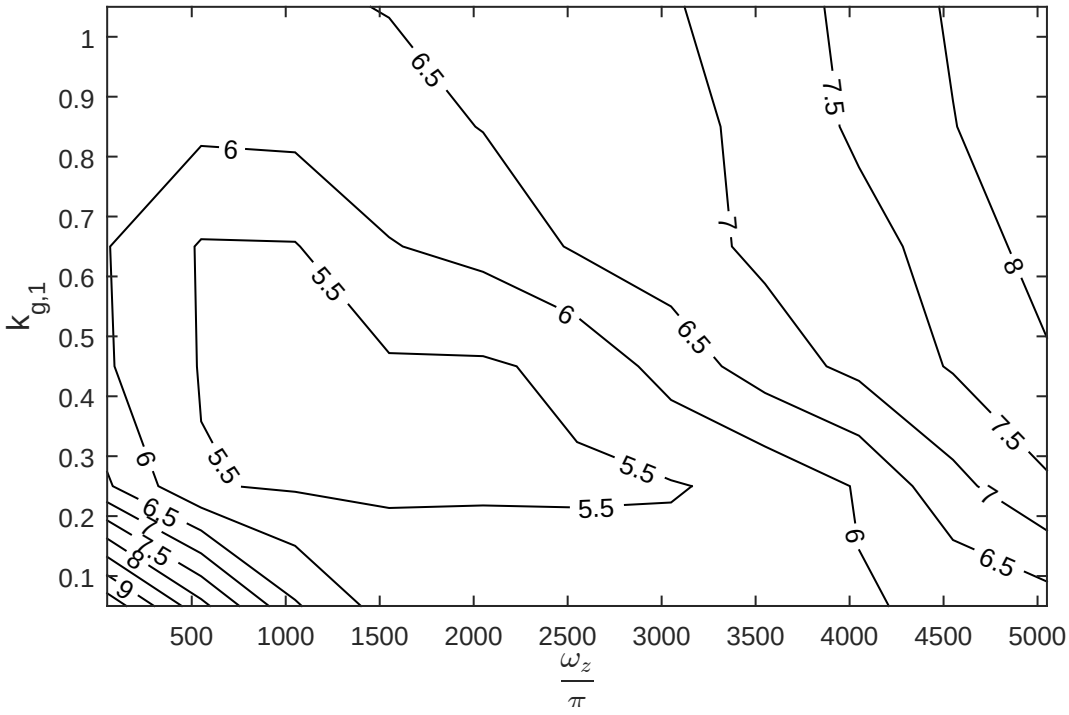

Figure 3.19: The maximum peak of i_L with the I-Lead controller. On the x axis is the ω_z per π and the y axis is $k_{g,1}$

The lowest area is below the 5.5 A. The gains are chosen as:

- $k_{g,1} = 0.4$.
- $\omega_z = 1000\pi$.

In figure 3.20 the bode plot of the controller is shown.

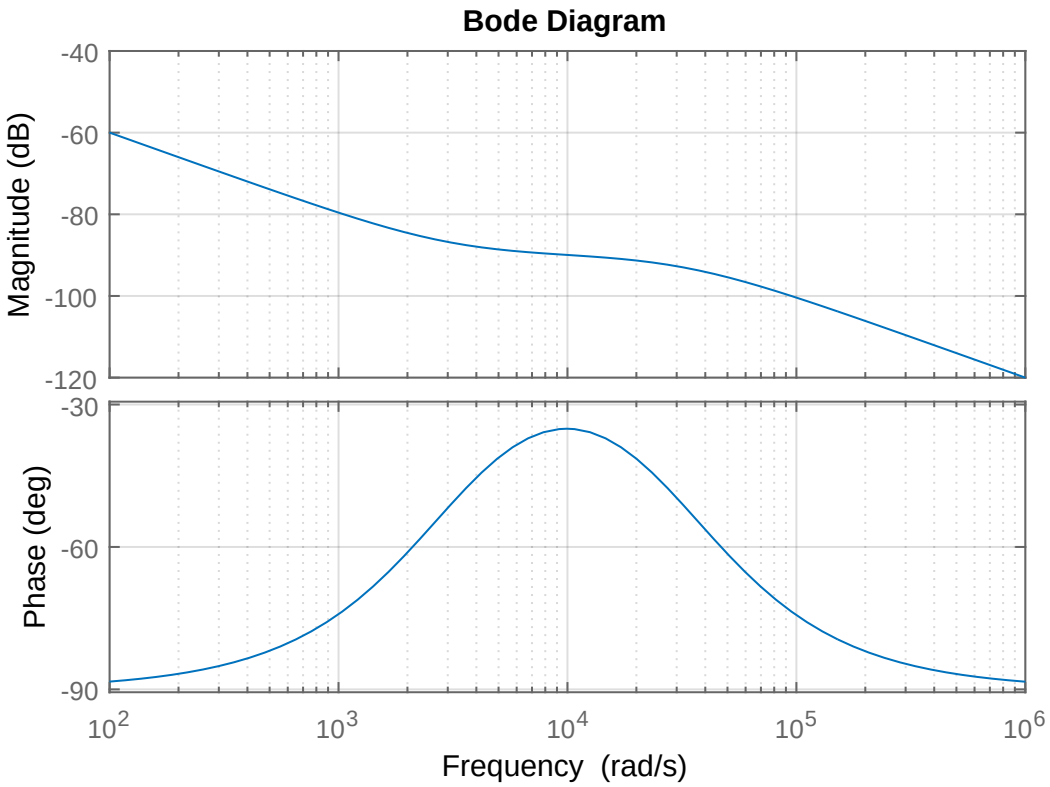

Figure 3.20: Bode plot of the I-Lead controller.

The boost controller is implemented in the physical system. Figure 3.21 shows the measured and simulated grid current on the top figure, and the bottom figure shown the measured and simulated duty cycle. The duty cycle is measured by measuring the PWM signal from the DSP and the logged data is filtered, by using the 'smooth' function in Matlab, where a mean is calculated over 50 measurements. The measured current shows greater dynamics than the simulated response. The difference is suspected to be caused, partly by the model parameters being fitted too coarsely, and partly caused by measurement noise between the inverter board and the DSP. The measurement noise in e.g. the current signal could yield a significant disturbance in the control signal. The duty cycle of both the simulation and the measurement, shows characteristics of reaching the upper saturation limit, when the grid current is zero, which maximizes T_{peak}. The fluctuating dynamics seen in the measured duty cycle is similar to the fluctuating dynamics of the measured current. The peak in the measured current response subsequent to the zero crossing, is due to the duty cycle being saturated.

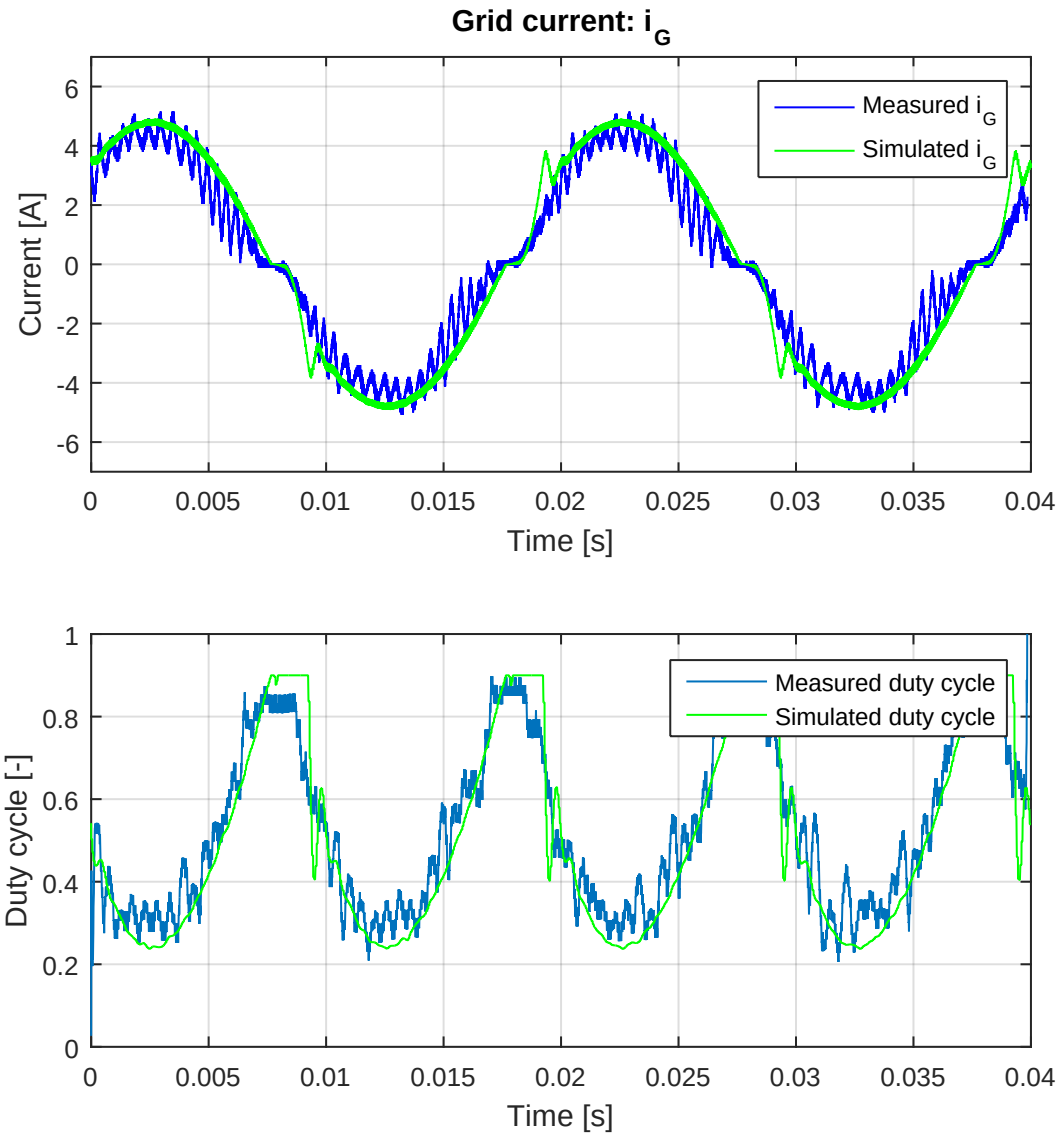

Figure 3.21: Top figure is the measured and simulated grid current. Bottom figure is the measured and the simulated duty cycle.

The response of the current conduction shows satisfactory characteristics, to initiate experiments, applying other loads than the resistive load applied in the conducted experiment.

To apply the load of an asynchronous AC motor, the inverter strategy SVM is examined in the following chapter.

Chapter 4

Inverter

This chapter describes the structure of the inverter model. The setup is described and switch cases of the inverter are discussed. Space Vector Modulation (SVM) is introduced and a V/Hz controller is described, implemented and tested. A general diagram of the inverter is shown in figure 4.1.

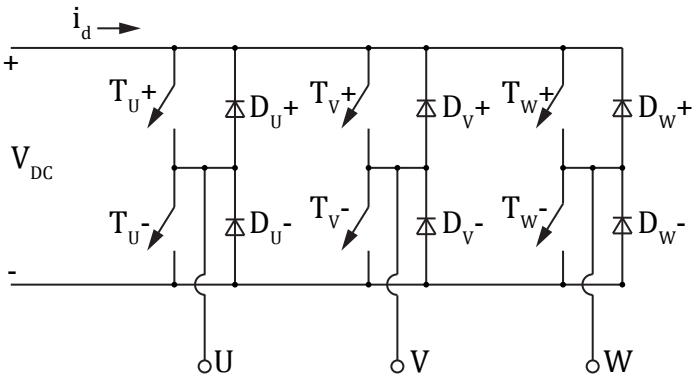

Figure 4.1: Structure of a three phase inverter, [Mohan, 2003].

4.1 Inverter model

In figure 4.1 it is seen that the inverter holds six switches, by these switches a phase is switched to either the positive or negative side of the DC voltage, supplying the inverter. In practice there is some blanking where both switches are off, though this is not accounted for in the model. When the switches of the three phases are seen as switched on to either the high or the low side of the DC supply, they may be seen as high or low (1 or 0). This yields two options per phases, yielding $2^3 = 8$ options for the inverter, including the two cases, where all three phases is switched on to the positive or negative side respectively. The switch cases are in the model contained in a math block, seen in figure 4.3, representing the structure of the inverter model, a sketch of the eight switch cases is seen in figure 4.2.

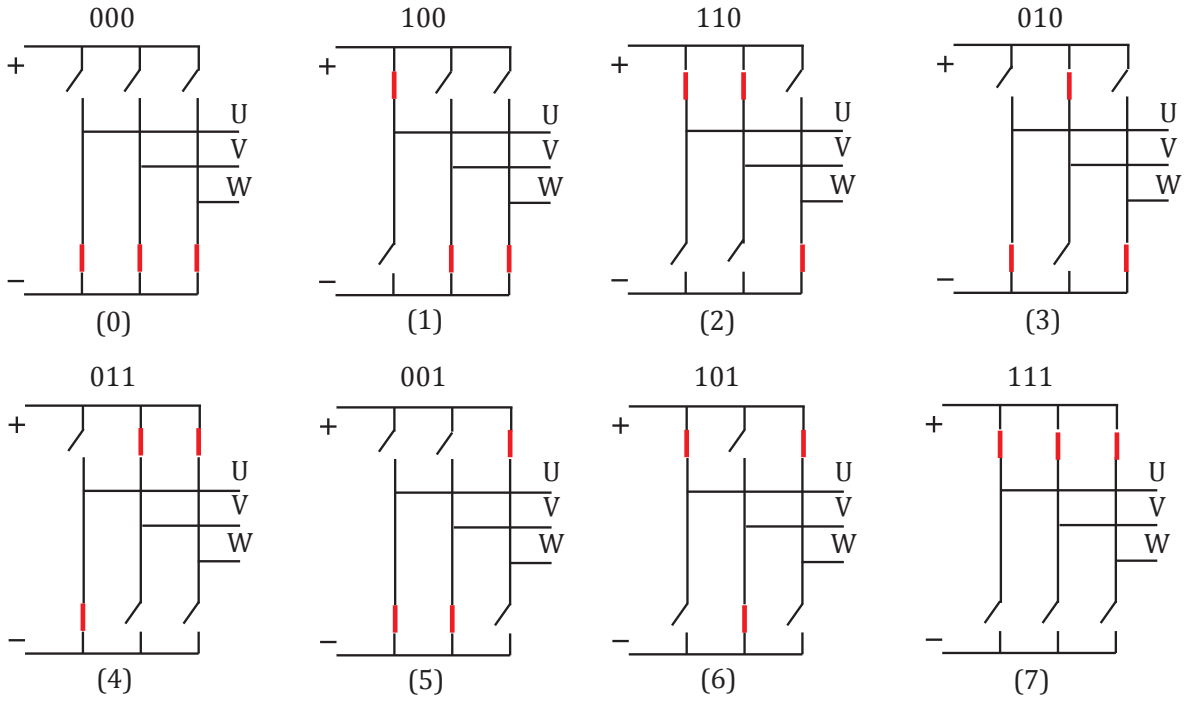

Figure 4.2: The inverter sketched for the eight possible switch cases, [Holmes and Lipo, 2003].

The configuration of the inverter, is determined by the controller. The controller is implemented to obtain the desired voltage output to drive the motor. The controller is described in section 4.3, first the structure of the inverter model is discussed.

4.1.1 Model structure

In the model the calculation of compare values (CV), that practically is done by the DSP, is modelled by a script block. Thereby the calculations is easy implemented on the DSP by only changing the script syntax. The script block calculates the CVs for the three phases on basis of SVM, described in section 4.2.

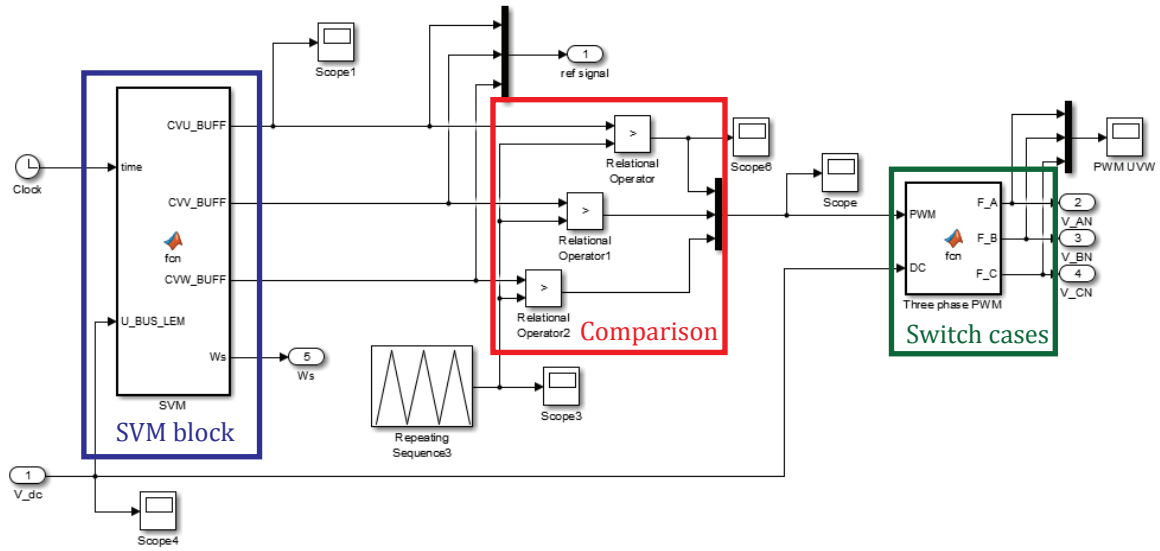

Figure 4.3: Structure of the inverter model.

Figure 4.3 shows the structure of the carrier based modulation. The CVs are compared to a carrier wave, which runs at 20 Hz similar to the DSP. Whenever the CV is of greater value than the carrier wave, the comparator is switched on, yielding a high signal (value of 1). This signal is transferred to the math block, containing the switch cases mentioned in figure 4.1, a high signal yields the phase switched to the high side of the DC bus, and vice versa.

4.2 Space Vector Modulation

This section describes the principle of Space Vector Modulation (SVM), the implementation is described and some response of the implementation is shown. This section is based on [Holmes and Lipo, 2003].

The SVM principle is based on the eight switch cases, or Space Vectors (SVs), mentioned in section 4.1. Where the SV_0 and SV_7 are called zero-vectors. The six active vectors are considered as a stationary angle in the complex ($\alpha\beta$) coordinate system, see figure 4.5. Furthermore each vector corresponds to a synchronus angle, see also figure 4.4.

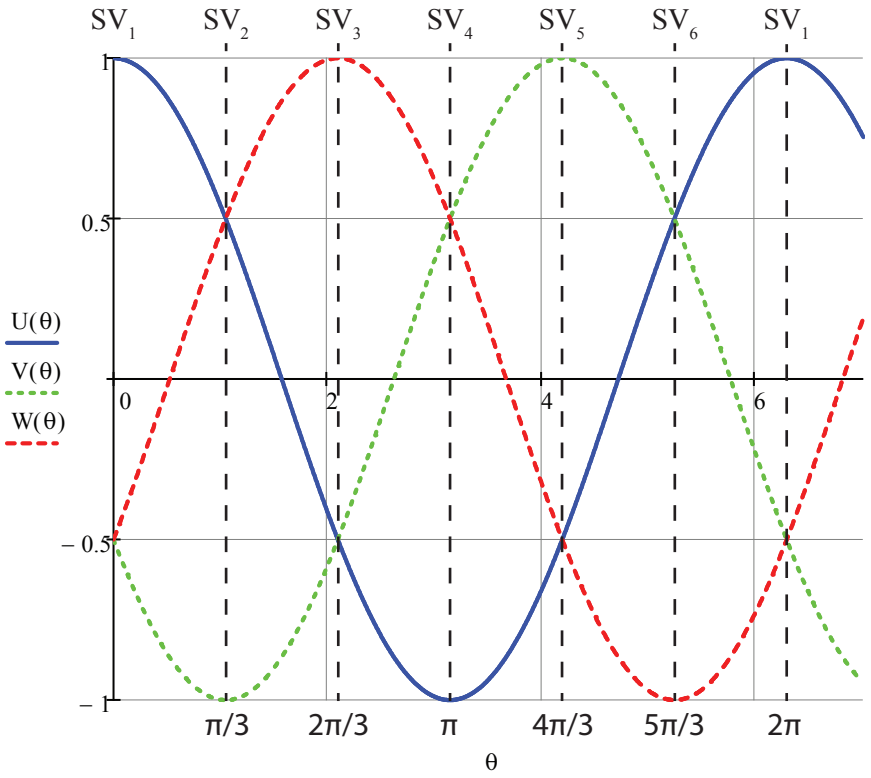

Figure 4.4: Sketch of the phase voltages corresponding to the six active space vectors, [Holmes and Lipo, 2003], notice that SV_1 is shown twice.

The magnitude of each vector is determined by equation 4.1, [Holmes and Lipo, 2003].

$$V_m = \frac{4}{3} \cdot \frac{V_b}{2} \tag{4.1}$$

An arbitrary output voltage vector V_o is formed by the averaging over a number of the six space vectors over one switching period T_s, see figure 4.5. An example is shown for combination of the vectors SV_1 and SV_2 at the angle of θ_o.

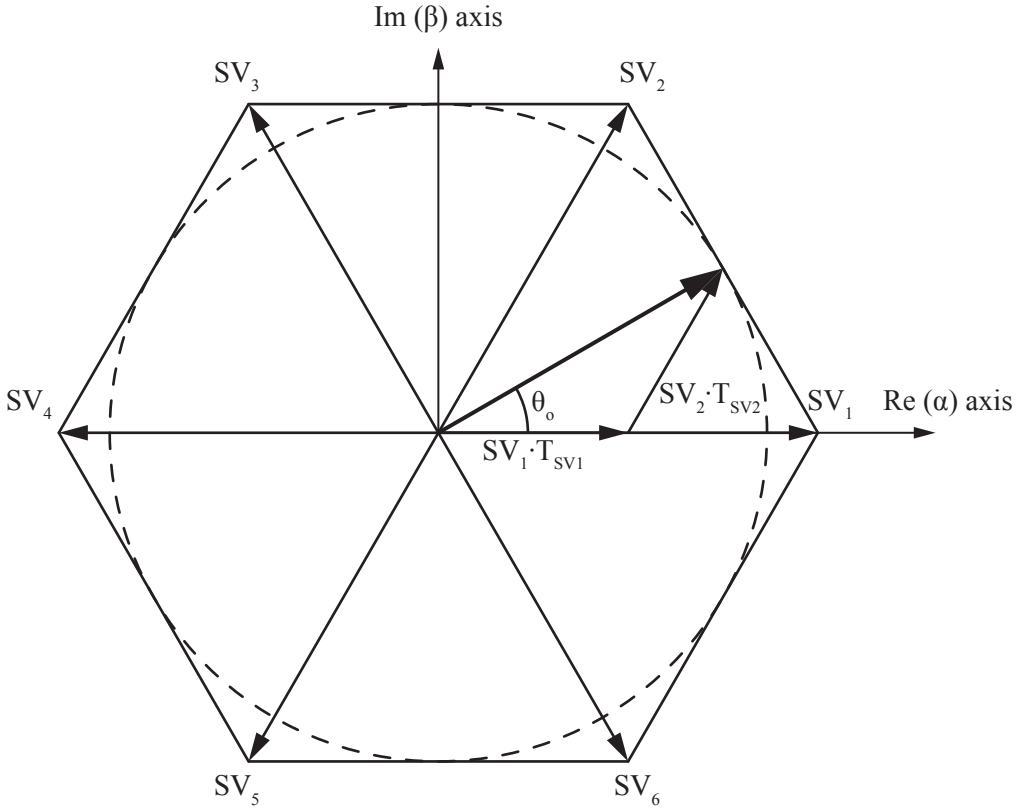

Figure 4.5: Sketch of the six space vectors, represented in the complex ($\alpha\beta$) plane. The resultant of switching half a SV_1 and half a SV_2 vector is shown. Drawn with inspiration from [Holmes and Lipo, 2003].

Representing an output vector in sector 1 $\left(0 - \frac{\pi}{3}\right)$, as the one shown in figure 4.5, in Cartesian form, is done by the expression in equation 4.2, [Holmes and Lipo, 2003].

$$V_o \cdot (cos(\theta_o) + j \cdot sin(\theta_o)) \cdot T_s = T_{SV1} \cdot V_m + T_{SV2} \cdot V_m \cdot \left(cos\left(\frac{\pi}{3}\right) + j \cdot sin\left(\frac{\pi}{3}\right)\right) \tag{4.2}$$

Where T_{SV1} and T_{SV2} is the on-time for space vector 1 and space vector 2, respectively. Calculating the real and imaginary parts and solving for T_{SV1} and T_{SV2} (two equations with two unknowns) yields the expressions seen in equation 4.3 and equation 4.4.

$$T_{SV1} = \frac{V_o \cdot sin\left(\frac{\pi}{3} - \theta_o\right)}{V_m \cdot sin\left(\frac{\pi}{3}\right)} \cdot T_s \tag{4.3}$$

$$T_{SV2} = \frac{V_o \cdot sin(\theta_o)}{V_m \cdot sin\left(\frac{\pi}{3}\right)} \cdot T_s \tag{4.4}$$

The sum of the on-times can not exceed one sampling time T_s. From geometry this is limited

at an output angle of $\theta_o = \frac{\pi}{6}$, from this; equation 4.5 through to 4.7 is obtained.

$$T_{SV1} + T_{SV2} \leq T_s \tag{4.5}$$

From equation 4.3 and 4.4

$$\frac{T_{SV1} + T_{SV2}}{T_s} = \frac{V_o \cdot sin\left(\frac{\pi}{3} - \theta_o\right)}{V_m \cdot sin\left(\frac{\pi}{3}\right)} + \frac{V_o \cdot sin(\theta_o)}{V_m \cdot sin\left(\frac{\pi}{3}\right)} \leq 1 \tag{4.6}$$

At the output angle of $\theta_o = \frac{\pi}{6}$

$$\frac{2 \cdot V_o \cdot sin\left(\frac{\pi}{6}\right)}{V_m \cdot sin\left(\frac{\pi}{3}\right)} \leq 1 \tag{4.7}$$

Isolating the maximum magnitude of V_o and noting that $sin\left(\frac{\pi}{6}\right) = \frac{1}{2}$

$$V_o = V_m \cdot sin\left(\frac{\pi}{3}\right) \tag{4.8}$$

Substituting equation 4.1 into equation 4.8

$$V_o = \frac{4}{3} \cdot \frac{V_b}{2} \cdot \frac{\sqrt{3}}{2} \approx 1.15 \cdot \frac{V_b}{2} \tag{4.9}$$

This yields a phase voltage output increase of up to $\approx$ 15% of a regular sinus modulation, which is a major benefit, and the reason to choose of the SVM.

A modulation index is included in the SVM control scheme. The modulation index is described by equation 4.10.

$$\frac{V_{nom}}{V_b} \tag{4.10}$$

The v_{nom} is the nominal output voltage. By applying the modulation index, the output is levelled, i.e. by measuring a lower boost voltage, the modulation index in increased, thereby the output remains constant.

4.2.1 Implementation of SVM

This section describes the implementation of the SVM performed on the DSP used in this project. As mentioned the modelling of the SVM is done by a script block in Matlab. Therefore the implementation is done by copying the code to the c-program, and changing the syntax.

The structure of the code is inspired by [Mathe, 2013]. The code uses the synchronous angle to determine what sector is present, and thereby which vectors should be put out. The synchronous angle is found from $\theta_s = \omega_s \cdot t$, where t is known from the switching period of the PWM interrupts. In the interrupt the synchronous angle θ_s is corrected by equation 4.11

$$\theta_s += \omega_s \cdot T_s \tag{4.11}$$

Where the $+=$ in the c-program takes the old value of θ_s and adds the right side of the equation to it.

From the synchronous angle an other angle is defined, that is the "$sector\theta$", which follows θ_s, but is reset for every $\frac{\pi}{3}$rad. This is done by the command $fmod$, shown in equation 4.12.

$$sector\theta = fmod\left(\theta_s,\ \frac{\pi}{3}\right) \tag{4.12}$$

The $fmod$ function is a remainder function, that divides θ_s by $\frac{\pi}{3}$, by long divition, and outputs the remainder.

Using this $sector\theta$ lets the program calculate only a $vector1$ and $vector2$ by sinus functions (function of $sector\theta$) and by the θ_s changing which space vector corresponds to the $vector1$ and $vector2$.

Test of SVM

In the implementation the SVM block defines the CVs for the three phases, as a reference for the phase voltage at the respective phase. The output of the section wise sinus functions, defined in the SVM block are plotted in figure 4.6. What is shown in figure 4.6 is only principle of the SVM, and no modulation index in included. Therefore the references vary from 0 to 1.

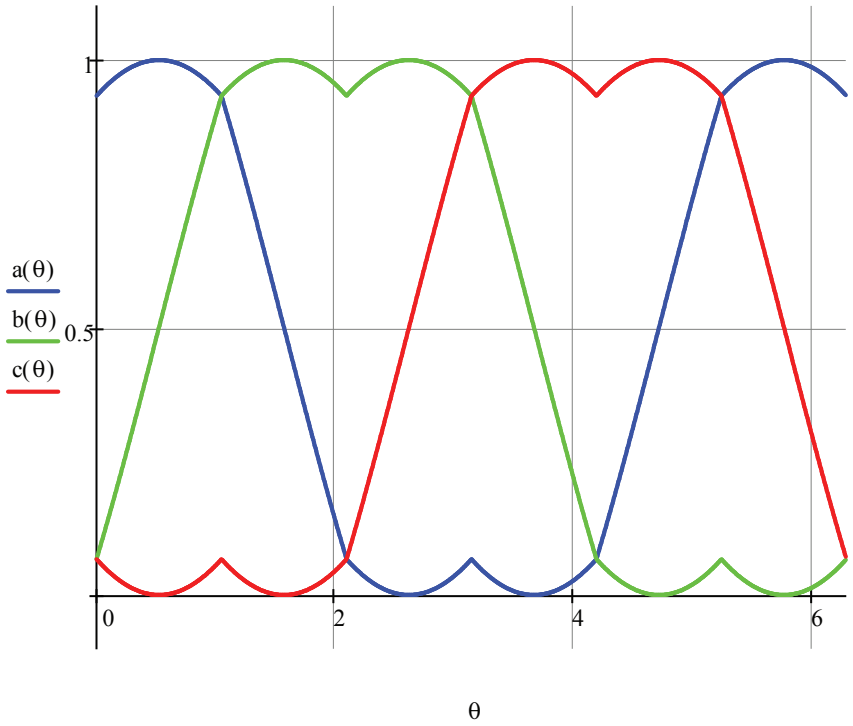

Figure 4.6: Plot of the theoretical compare values, from the SVM block.

The program is converted to c-code and tested on the DSP. During the test, the voltage measurement, measuring the boost voltage is disengaged, and a constant value og $V_b = 420\,\text{V}$ is fed into the calculations. The outputs of the DSP are PWM signals and are difficult to evaluate. Therefore the signals from the DSP are filtered, to obtain a measure for the duty cycle (the CV), comparable to figure 4.6. The measured result are shovn in figure 4.7.

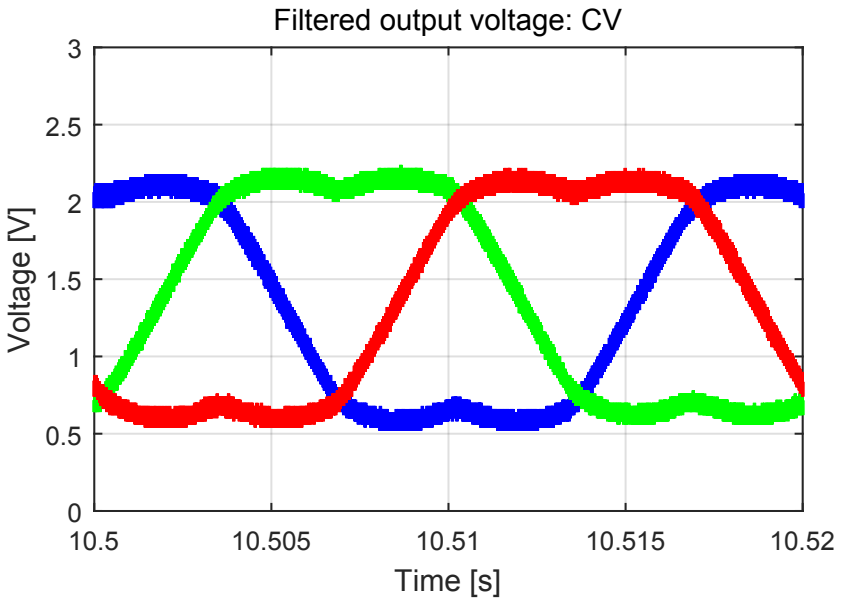

Figure 4.7: Plot of the measured, filtered PWM outputs of the DSP.

Note that the measurement, plotted in figure 4.7, are filtered. Therefore some loss occurs in the filter, and centre of the measurements are not present at half of the PWM output voltage of 3.3 V. Despite that the, characteristics of the signals are seen to be similar to that of figure 4.6, and the SVM is therefore acknowledged as implemented correctly.

4.3 Inverter control

To determine the output of the inverter, an open loop V/Hz controller is implemented. The V/Hz controller is chosen for simplicity, and as the system is to be tested with an asynchronous AC-motor, no feedback from the motor is available without installing an external encoder on the motor.

The V/Hz controller is designed with a constant voltage frequency relation and a minimum voltage, as shown in the sketch in figure 4.8.

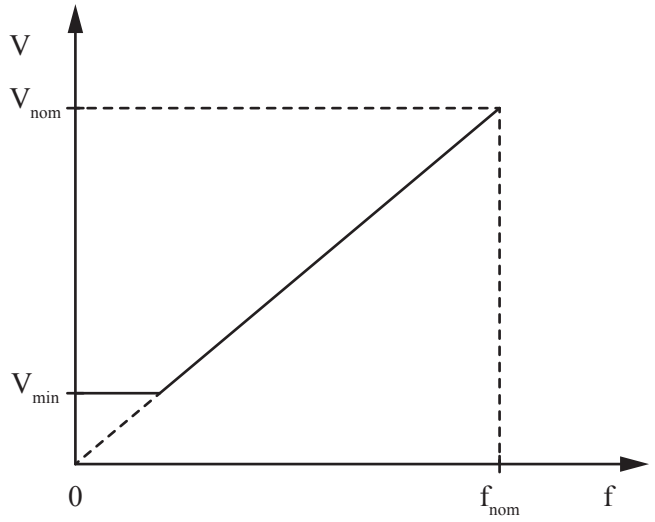

Figure 4.8: Sketch of the characteristics of the implemented V/Hz controller

The V/Hz controller is implemented, both in the model and on the DSP. The implementation includes a value of the start voltage, or minimum voltage V_{min}, the nominal voltage V_{nom}, the nominal frequency f_{nom} and the ramping time t_{ramp}. The nominal values are determined from nameplate values of the AC-motor. The ramping time specifies the time to ramp the output from start (zero) to nominal output. The values of the controller variables are specified as:

- $V_{min} = 10\,\mathrm{V}$
- $V_{nom} = 230\,\mathrm{V}$
- $f_{nom} = 50\,\mathrm{Hz}$
- $t_{ramp} = 10\,\mathrm{s}$

The CVs of the SVM model block is logged and the ramping is plotted in figure 4.9.

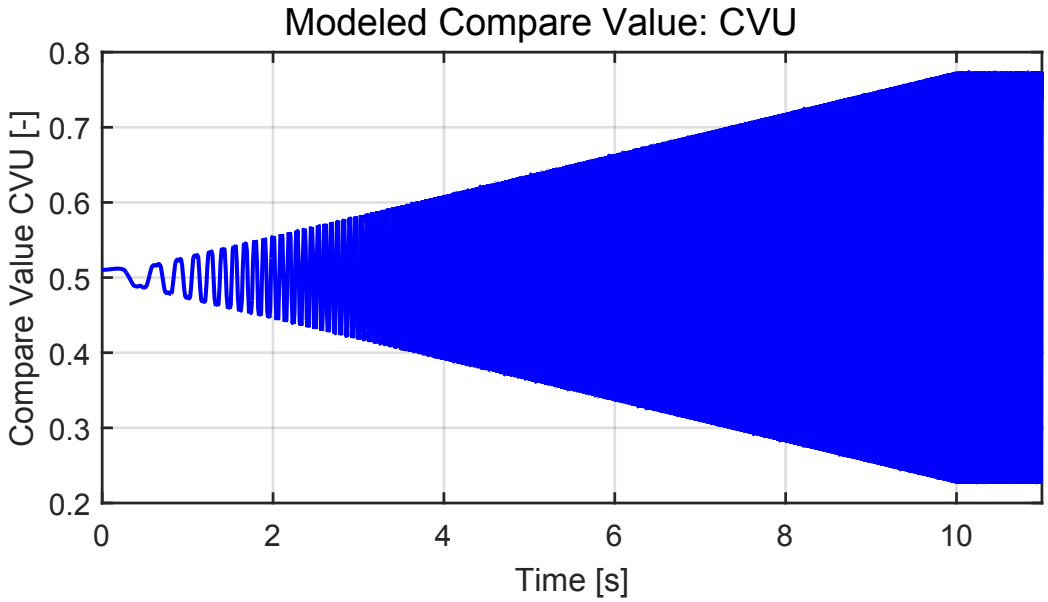

Figure 4.9: Plot of the modeled compare values, CVU from the SVM block.

As seen in figure 4.9 both the output frequency and output voltage reference to the inverter is ramped up gradually from minimum values in the specified 10 s ramping time.

To compare the model to the physical system the output of the DSP is again filtered, measured and compared to the modelled values. The filtered PWM output signal of phase *U* (CVU), from the DSP are plotted in figure 4.10.

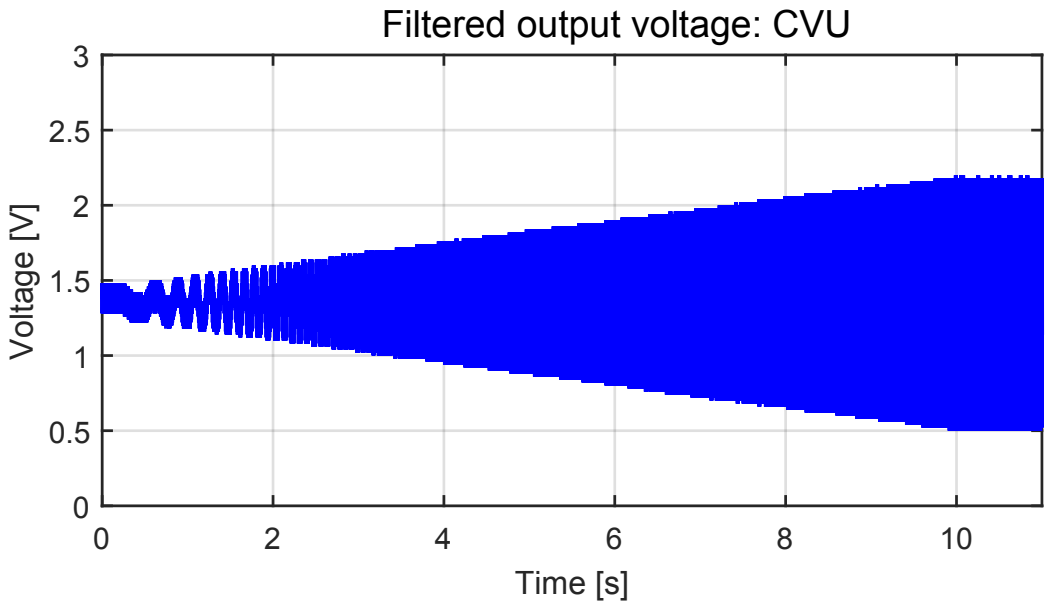

Figure 4.10: Plot of the filtered PWM output signal of phase *U* (CVU) from the DSP.

As seen in figure 4.10 the characteristic of the DSP output in the ramping time, is similar to what is seen in the model in figure 4.9. From the figures presented it is difficult to determine

whether the frequency reaches the specified nominal values, and whether it is a smooth transfer from the ramping to nominal operation. Therefore the measured data around 10 s (end of the ramp) is plotted and compared in figure 4.11.

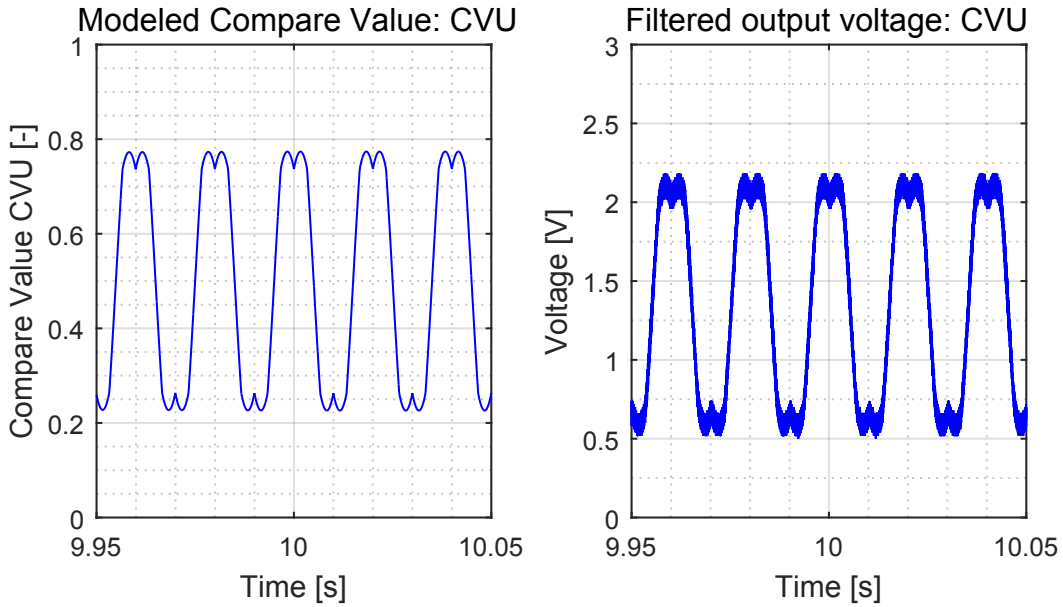

Figure 4.11: Comparing of the modeled CVU and the measured CVU around 10 s, (end of ramping time).

As seen in figure 4.11 the frequency reaches 50 Hz at 10 s, since one period takes 20 ms in the last periods before and likewise after the 10 s mark. Therefore the inverter control is considered to operate satisfactory, and is ready to be implemented on the AC-motor, which is described in chapter 5 *AC motor*.

Chapter 5

AC motor

This chapter describes tests of the complete hardware setup. That includes the boost converter with PFC control, the inverter with SVM and the 3 phase asynchronous AC motor. Initially the model of the AC motor is superficially described, to understand the parameters, used to determine the simulated values of the inductor current.

5.1 AC motor model

The boost converter and inverter is tested on an asynchronous AC motor, to test the characteristics of the inductor current i_L, with a reactive and varying load. The AC motor drives a fan, mounted in an exhaust device, developed for ventilation in poultry farms. The fan setup is reused from [Christiansen et al., 2014], during the project Christiansen et al. [2014] parameters for the motor is derived. A model of the AC motor is developed from the IEEE-recommended equivalent circuit, shown in figure 5.1. The diagram shows only one phase of the three phased AC motor, all three phases are modelled by the principle described.

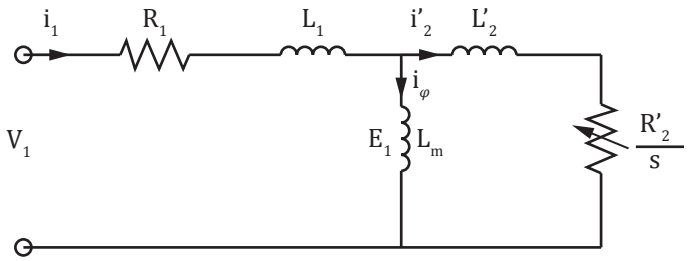

Figure 5.1: Diagram of one phase of the asynchronous AC motor, [Sen, 1996]

The parameters in the diagram are recognised as:

- V_1 is the voltage across the stator terminals for the phase of the motor
- i_1 is the stator current
- R_1 is the stator resistance
- L_1 is the stator inductance
- E_1 is the induced voltage in the stator windings
- L_m is the magnetizing inductance
- i_ϕ is the magnetizing current
- i'_2 is the rotor current, related to the stator side

- L_2' is the rotor inductance, related to the stator side
- $\frac{R_2'}{s}$ is the rotor resistance related to the stator side, as a function of the slip
- s is the slip

The V_1 is the voltage across the phase. As the motor is set up in a Δ connection, each phase is experiencing the line to line voltage between the two phases it is connected to. Therefore the voltage V_1 is calculated by subtracting the two phase voltages, that is connected to the respective phase. Equation 5.1 calculates the voltage across the motor phase A.

$$V_{1A} = V_{U0} - V_{V0} \tag{5.1}$$

From the diagram in figure 5.1, the governing equations, describing voltage and current in the AC motor, are derived as equations 5.2 through to 5.5

$$V_1 = R_1 \cdot i_1 + L_1 \cdot \frac{di_1}{dt} + E_1 \tag{5.2}$$

$$V_1 = R_1 \cdot i_1 + L_1 \cdot \frac{di_1}{dt} + L_2' \cdot \frac{di_2}{dt} + \frac{R_2'}{s} \cdot i_2' \tag{5.3}$$

$$E_1 = \frac{di_\phi}{dt} \cdot L_m \tag{5.4}$$

$$i_1 = i_\phi + i_2' \tag{5.5}$$

In [Christiansen et al., 2014] the parameters of resistance and inductance, shown in the circuit figure 5.1, are determined through tests. The results are shown in table 5.1.

Parameter	Value	Unit
R_1	27.64	Ω
L_1	0.0774	H
L_m	0.6281	H
L_2'	0.0774	H
R_2'	25.25	Ω

Table 5.1: Parameters for the AC motor, determined in [Christiansen et al., 2014].

The mechanical torque output of the motor T_{mech} for one phase is described in equation 5.6, [Sen, 1996].

$$\tau_{mech} = \frac{1}{\omega_{syn}} \cdot I_2'^2 \cdot \frac{R_2'}{s} \tag{5.6}$$

Note that equation 5.6 is the torque for one phase, to determine the total torque, equation 5.7 is used.

$$\tau_{mech-tot} = \frac{1}{\omega_{syn}} \cdot (I'^2_{2A} + I'^2_{2B} + I'^2_{2C}) \cdot \frac{R'_2}{s} \tag{5.7}$$

Where:

- I'_{2A} is the rotor current from phase U related to the stator side
- I'_{2B} is the rotor current from phase V related to the stator side
- I'_{2C} is the rotor current from phase W related to the stator side
- ω_{syn} is the synchronous rotational velocity
- s is the slip, between the rotor speed ω and ω_{syn}

The slip is described by equation 5.8

$$s = \frac{\omega_{syn} - \omega_{mech}}{\omega_{syn}} \tag{5.8}$$

Where:

- ω_{mech} is the mechanical rotaional velocity

The synchronous rotational velocity is described by equation 5.9.

$$\omega_{syn} = 2\pi \cdot f_{syn} \tag{5.9}$$

Where:

- f_{syn} is the synchronous frequency

The synchronous frequency is determined by the inverter control, described in section 4.3.

The torque output of the motor is set equal to the torque characteristics of the fan on the test setup. The parameters of the fan are tested in Bjerregaard et al. [2012], and found to be approximately a quadratic load. The quadratic torque equation for the fan, derived by [Bjerregaard et al., 2012] is shown in equation 5.10

$$\tau_{fan} = 3.05 \cdot 10^{-4} \cdot \omega^2 + 2.98 \cdot 10^{-5} \cdot \omega \tag{5.10}$$

The introduced equations are combined to form the model describing the response of the AC motor, and the combination of the models is described in the following section.

5.2 Joint model

The previously described models (boost converter, inverter and AC motor) are set up and tested individually. When combining the models inputs and outputs are connected, the required data signals, transferred between the models, are shown in figure 5.2.

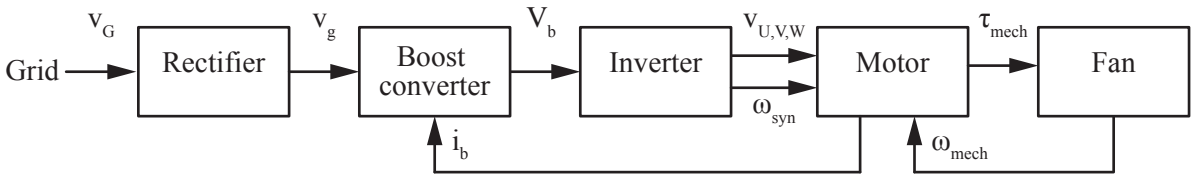

Figure 5.2: Sketch of the required interaction between the separate models of boost converter, inverter and AC motor.

To determine the inductor current i_L, the load current i_b must be known, confer the equations in chapter 3 *Boost converter*. In the complete model, the load current is determined by the three stator currents in the phases A, B and C of the AC motor, see equation 5.11.

$$i_b = \frac{|i_{1A}| + |i_{1B}| + |i_{1C}|}{2} \tag{5.11}$$

As seen in figure 5.2, the load current i_b is fed back from the motor model to the boost converter model. Similarly the synchronous rotational velocity ω_{syn} is fed from the inverter to the AC motor model, and the mechanical rotational velocity ω_{mech} is fed from the fan model to the AC motor model. The rotational velocities are used in the AC motor model to determine the slip of the motor.

Practically the fan and the motor are modelled in the same model file, likewise is the rectifier and the boost converter. Though the components are modeled in the same file, they are sketched as separate modules in figure 5.2, since the only interactions is the once shown. The rest of quantities transferred between the models are recognised as:

- V_G The grid voltage
- V_g The rectified grid voltage
- V_b The boost voltage
- $V_{U,V,W}$ The phase voltages quantities out of the inverter
- τ_{mech} The mechanical torque driving the fan

As the models are connected and incorporated to one joint model, simulation results are developed and presented in the following section.

5.2.1 Simulation results

Through this section simulation results from the joint model, described earlier, are presented. The idea of the joint model is to ramp up the speed of the AC motor and thereby the fan. By ramping the velocity of the fan the required torque is changing, due to the torque equation, see equation 5.10. When changing the load on the motor, it is of interest to examine the inductor current in the boost converter, and thereby evaluate the PFC.

Selected quantities between the models shown in figure 5.2, are examined in the joint model, to examine the cooperation of the models. The supplied grid voltage v_g is not examined, since this is modelled as a perfect sine wave. The boost voltage V_b is plotted in figure 5.3, the reference for the boost controller is 200 V. The reason for the low voltage reference is, that the measurements logged from the physical system, with a lowered voltage level, since the intention of examining the model is to compare the model response, to the response of the physical system, the simulation is performed with the conditions used in the physical system.

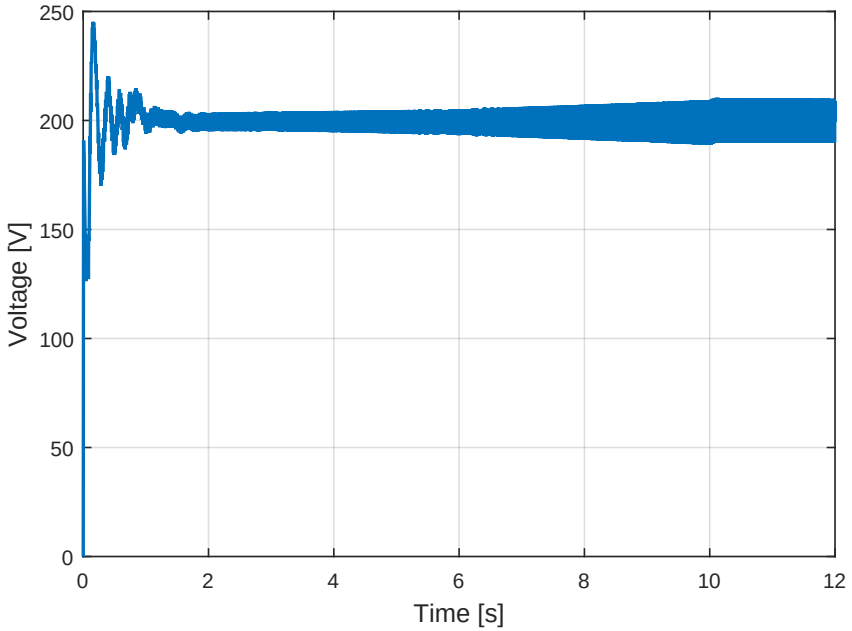

Figure 5.3: Plot of the simulated boost voltage V_b, simulated with a control reference of 200 V.

As seen in figure 5.3, some dynamic response is present during the transient settling. The dynamic response is seen, since the initial conditions in the model is zero, and the start therefore acts as a step input, from zero to the reference. The ripple of the boost voltage is seen to increase during the 10 s ramping time mentioned in section 4.3. Since the ripple is increasing during the ramping time, and remaining constant subsequently, the increasing ripple is caused by the increasing voltage output from the inverter, which yield an increasing load current.

The system is ramped up by the V/Hz controller described in section 4.3, the voltage fed to

the motor is plotted in figure 5.4. The plotted voltage is the line to line voltage that the motor phase A is exposed to, described by equation 5.1, therefore the characteristic of the plotted curve is not similar to what is seen in section 4.2, but has the characteristics of a regular sine curve. Note that despite the ripple seen in the boost voltage V_b, no ripple is observed in the inverter output.

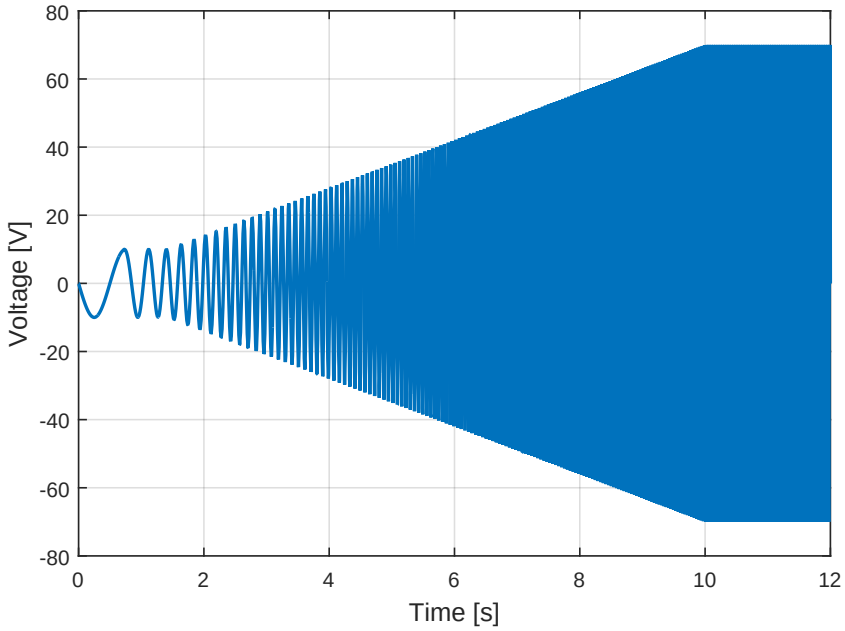

Figure 5.4: Plot of the voltage applied on the motor phase A ($V_{U0} - V_{V0}$), ramped linearly through the ramping time to a nominal voltage of 70 V.

As seen in figure 5.4 the applied voltage has the tendency of a regular sine function and the amplitude is linearly ramped up to a nominal value, through the specified ramping time of 10 s. Furthermore it is seen by figure 5.4, that the amplitude of the line to line voltage is limited to 70 V. The reason to this is again, that measurements logged from the physical system, with a nominal value for the voltage amplitude of 70 V, and a nominal frequency of 28 Hz. The simulation is performed under similar conditions.

By increasing the applied voltage, as shown in figure 5.4, the current conduction in the stator is increasing. The simulated stator current is plotted in figure 5.5.

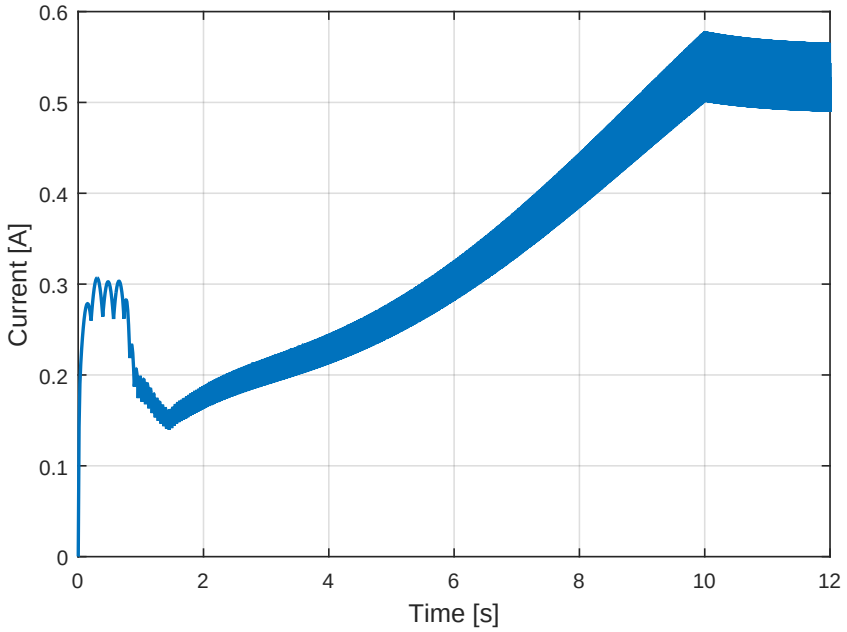

Figure 5.5: Plot of the simulated stator current, when ramping the voltage as shown in figure 5.4.

In figure 5.5 a start current is observed, the higher start current is also an effect of the start step. The current response is seen to settle and subsequently increase gradually. The ripple observed in the current response, is a consequence of adding the numerical value of the three phase currents, as shown in equation 5.11.

To avoid numerical errors in the simulation, a minimum frequency in implemented in the model. The minimum frequency is set to 1 Hz. When running the model the frequency is set to the minimum boundary, until the ramped reference exceeds the threshold. This happens at the time $t = 0.36\,\text{s}$. The change in dynamics seen around this time, expected to be partly caused by the initial step input and partly caused by the transition between a fixed frequency reference and the ramping frequency reference.

The increasing current yield an increasing torque, confer equation 5.6. The simulated mechanical torque output of the motor τ_{mech} is plotted in figure 5.6

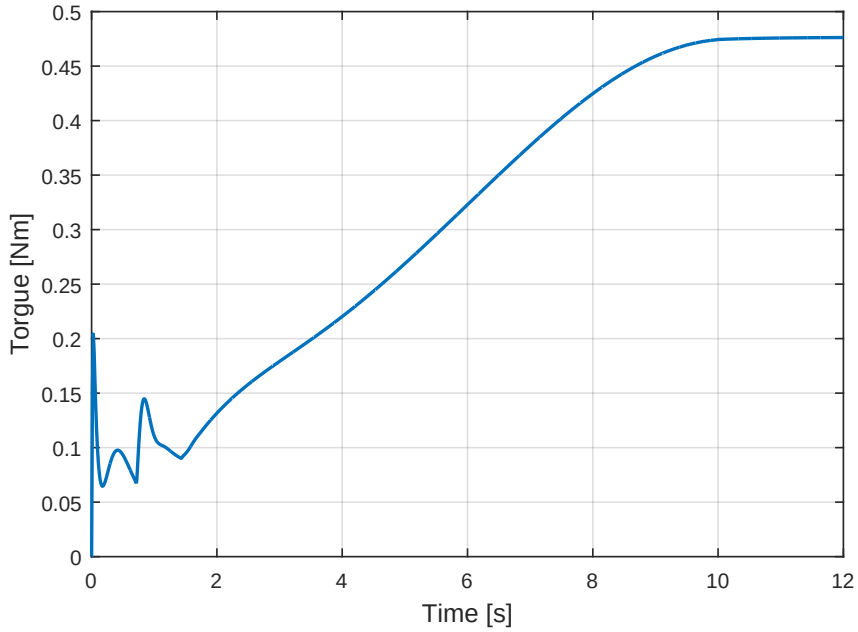

Figure 5.6: Plot of the mechanical torque output of the AC motor τ_{mech}.

The torque is seen to ramp up to a nominal value during the ramping time, as expected. The dynamic torque response at time $t = 0$ is again expected to be caused by the start step input, and the high start current.

The increasing torque should yield a ramping velocity. Due to the mechanical transfer function, operating as a filter, the velocity response is expected to be delayed when comparing to the torque. The angular velocity of the fan is plotted in figure 5.7.

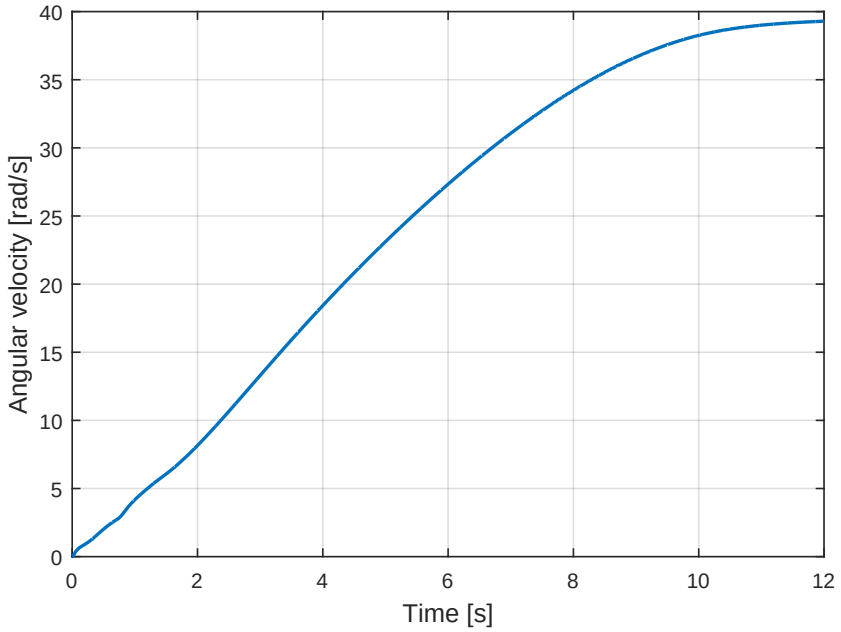

Figure 5.7: Plot of the simulated angular velocity of the fan.

As seen in figure 5.7, the torque dynamics present in the first two seconds of figure 5.6, is filtered to be hardly noticeable in the velocity response. Further it is seen, that even though the torque is constant from $t = 10\,\text{s}$, the velocity is increasing during the full simulation, due to the filtering effect of the transfer function, describing the mechanical velocity.

As mentioned the load current i_b calculated by equation 5.11 determines the load of the boost converter, and is therefore crucial to determining the inductor current i_L. The purpose of the PFC controller is, as discussed in chapter 3 *Boost converter*, to ensure that the voltage and current drawn from the grid are in phase, which yields lower peaks of the inductor current. Figure 5.8 shows how the rectified voltage v_g and inductor current are modelled to be drawn in the same phase. The data shown is enlarged from the time $t = 11\,\text{s}$, to see the rectified sine characteristic of the voltage.

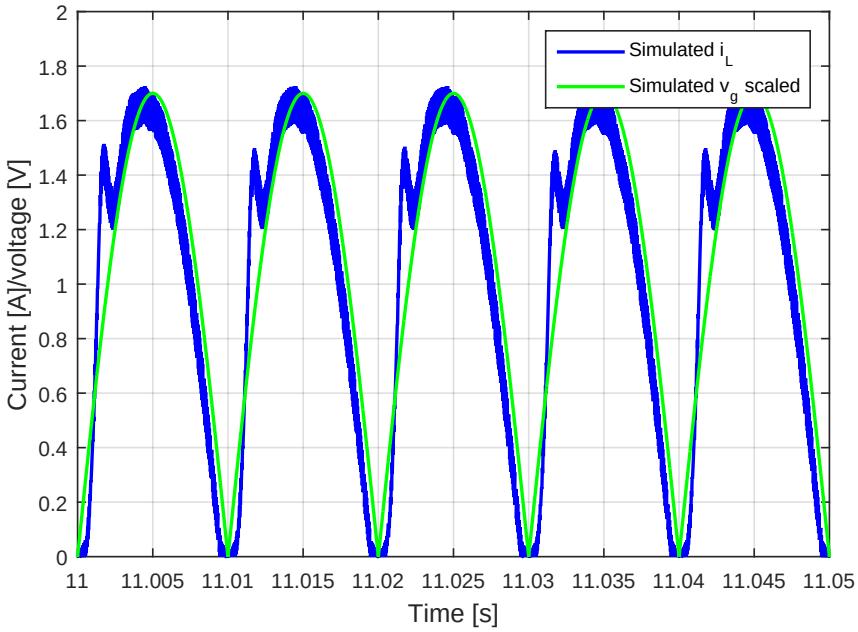

Figure 5.8: Plot of the simulated rectified grid voltage v_g and the inductor current i_L.

As seen in figure 5.8, the current does not show the characteristic of a perfect sine wave rectified. The fact that the current is out of phase of the voltage, yields a power factor lower that one, $PF < 1$. The bulge observed in the current response, is present, since the duty cycle of the boost converter switch, reaches saturation then the voltage approaches zero. The duty cycle signal reaching saturation, causes a wind up of the controller, which is to be wound back down by the controller, before the current response again tracks the shape of the rectified voltage. The undesired characteristic might be reducible by implementing an anti wind up loop to the controller, however this is not examined further.

Figure 5.8 does though show, that the PFC controller is controlling the inductor current, to be in phase with the rectified grid voltage. The fact that the inductor current shows an approximate (rectified) sine characteristic, ensures that the peaks are lowered, compared to operating at a constant duty cycle, as discussed in chapter 3 *Boost converter*. The characteristic of the inductor current over the ramping time is showed in figure 5.9, to examine the trend of the peak currents during ramping of the load.

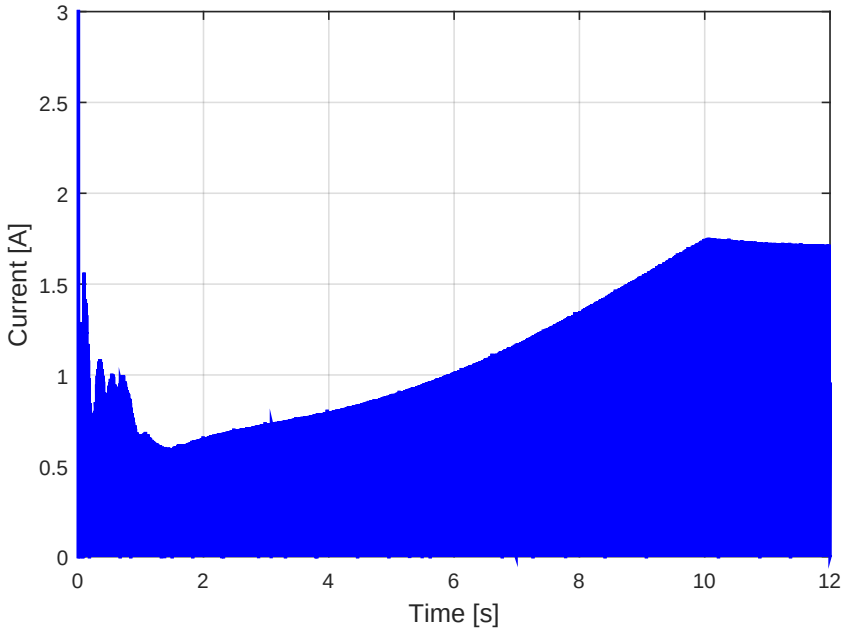

Figure 5.9: Plot of the simulated inductor current i_L, through the full simulated 12 s. The plot shows the overall characteristics of the inductor current, while ramping the load of the motor.

As seen in figure 5.9 there is some dynamic response during the first second of the simulation. This is again assumed to be caused partly by the start step and partly by the reference frequency changing from a constant to a ramping reference. The inductor current response at time $t = 0.5$ s is shown in figure 5.10, to examine whether the response shows the characteristic of a rectified sine wave.

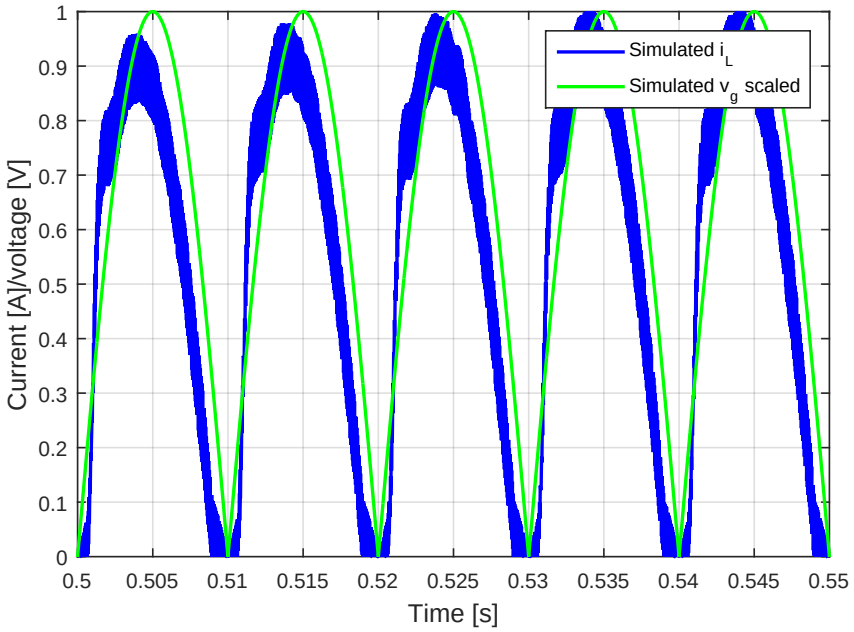

Figure 5.10: Plot of the inductor current response from the time $t = 0.5\,\text{s}$. The response shows the approximated characteristics of a sine wave, though peak values shows fluctuations in figure 5.9.

It is concluded that even though the peak current response, shown in figure 5.9, shows fluctuations, the current approximately shows the response of a rectified sine wave. Since the characteristics of the joint model shows the desired overall response, the control is implemented in the physical system. The response of the physical system is shown and discussed in the following section.

5.3 Response of physical system

Through this section the response of the physical system is shown and discussed. The control, implemented in the physical system, ramps the frequency from $f_{syn} = 0$, since the constant start frequency reference, is implemented in the model, only to avoid singularities. Therefore the behaviour, caused by the change from constant to ramping frequency reference, is expected to be eliminated.

The response of the physical system is plotted with the simulated result, during the 12 s simulated period, to compare the characteristic during the 10 s ramping time.

In figure 5.11 the boost voltage response, of the simulation and the physical system respectively, are compared. The measured response shows an initial step to approximately 150 V, and another step at time $t \approx 1.5\,\text{s}$, after which the voltage oscillates around the reference of 200 V.

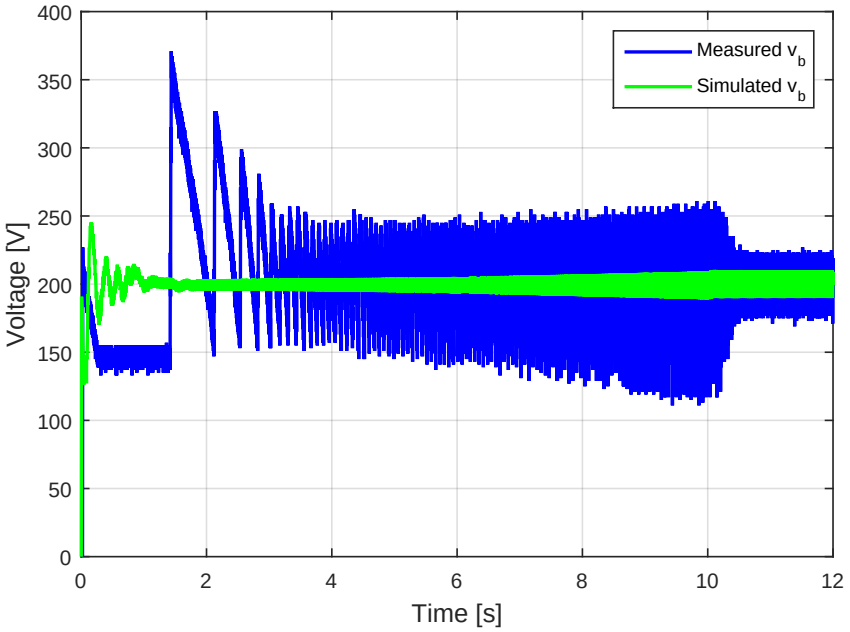

Figure 5.11: Plot of the simulated and measured boost voltage

The initial step is expected to be caused by the controllers running before the power to the system is turned on. This yields the reference to the current controller being zero, since the input voltage v_g is zero. In the controller, a lower saturation limit is implemented, therefore the low reference results in the current controller winding winding up (in a negative value). Therefore the duty cycle of the boost converter switch, remains in the lower limit, until the controller again is wound down.

Since a period of 20 s is logged by an oscilloscope, the resolution of the measurement is poor, therefore no zoom of the measured data is shown. The saw-toothed response of the boost voltage is expected to be caused by the current being drawn in short periods of time, similar to the response seen in section 3.2. The simulated grid current response is compared to the measured grid current response, in figure 5.12.

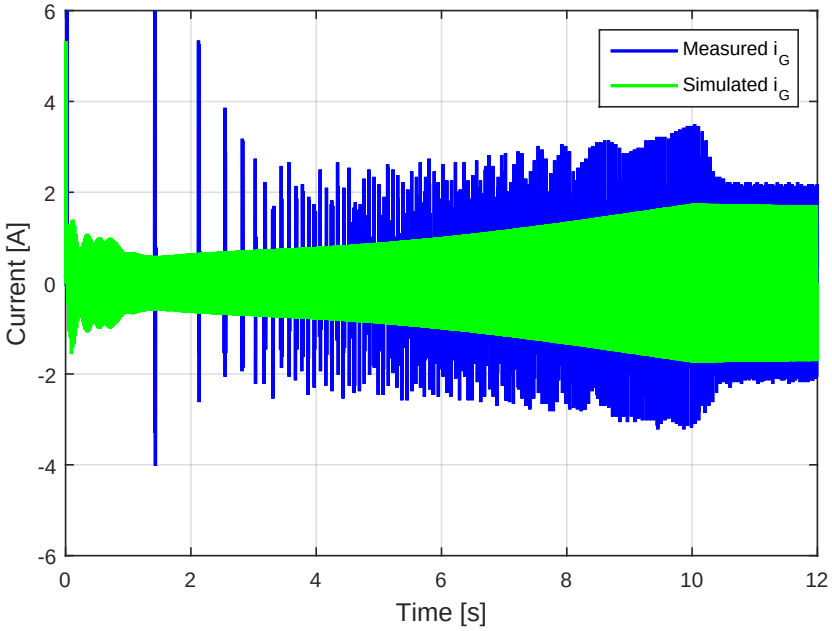

Figure 5.12: Plot of the simulated and measured grid current response.

As seen by figure 5.12 the measured current response shows significantly larger peaks that the simulated response. The generally larger current peaks are similarly expected to be a result of the current being drawn from the grid in short time periods, i.e. operation in DCM. Again the only measurements available is the measurement of the 20 s time period logged by the oscilloscope, therefore the current measurements are likewise of poor resolution, and it is impossible to examine the current characteristics any further.

The current spikes seen in the time interval $t = 1.5\,\text{s}$ to $t = 3\,\text{s}$ is seen to coincide with the voltage spikes shown in figure 5.11, and is expected to be a result of the step in boost voltage, that originates from the wound up controller.

The enlarged current peaks are expected to be a result of testing the setup at low voltage and low frequency. By lowering the frequency and voltage that the motor is exposed to, the power drawn by the motor is decreasing. By lowering the frequency, the reactance in the motor is of less impact, due to equation 5.12.

$$X = \omega \cdot L = 2\pi \cdot f_{syn} \cdot L \tag{5.12}$$

Since the voltage and frequency supplied to the motor is significantly lower than what the boost motor is designed for, the power drawn by the motor is significantly lower than what the model is designed for. The operating point significantly away from field of operation, might explain some of the poor measurements. It is too late discovered that the system operates in DCM, and unfortunately no better measurements are obtained.

Chapter 6

Conclusion

The aim of the project is to design a boost converter, and implement a PFC control structure. The boost converter is intended to be incorporated in a ventilation system, where a permanent magnet synchronous motor (PMSM) is driving a fan, mounted on the wall of a drying facility. However the project explicitly examines the boost converter, and initially applies a resistive load. Secondly the resistive load is substituted with an AC motor driving a fan, intended for ventilation in poultry farms.

An inverter board is given from the engineering company Eltronic. The power module installed on the inverter board, includes the boost converter switch, and the circuit board is prepared for installation of a boost inductor and capacitors. The hardware from Eltronic is examined and tested, regarding use of the installed current measurements and signals driving of the power module.

During the project, the main focus is concentrated on the boost converter. A dynamic model is constructed in Simulink, and verified with the Eltronic inverter board, through laboratory experiments. A controller is designed, to maintain a constant boost voltage and to ensure the current drawn from the grid is in phase with the grid voltage (PFC).

A control structure constructed of a PI controller, controlling the boost voltage, along with a P controller, controlling the inductor current. The control structure shows favourable results in simulation, and is implemented in the physical system. However in the physical system, the current controller shows poor response. Therefore the current controller is redesigned, and a I-Lead controller is implemented as current controller. The I-Lead controller proves to yield a good current response in the model, and similar good response, when implemented in the physical.

To introduce a load different from the resistive load, implemented in initial experiments, the inverter strategy SVM is examined, with the goal to drive an AC motor. The inverter strategy is modelled and implemented in the physical system. To control the AC motor, an open loop V/Hz controller is modelled and implemented. The inverter strategy and the open loop controller is tested and verified, by measuring the signal output of the DSP, utilised to drive the control strategies.

A joint model is obtained by combining the models of the separate systems and results are obtained through simulation. The system is connected to the AC motor, and tested at a

reduced voltage and frequency level. Unfortunately the only data logged from the physical system shows the ramping of the motor, i.e. a logging of 20 s. The large time frame causes the resolution of the log file to be too poor, to examine any response by enlarging the time scale of the data. Furthermore the captured data shows evidence of the controller being wound up, as an effect the control output being saturated for a period of time, before the power to the system is switched on.

6.1 Future Work

This section describes considerations, concerning improvements of the system.

Due to the poor response shown in section 5.3, more attention to the control is required, in order to obtain a robust PFC controller. As mentioned in section 5.3, a considerable amount of the undesired dynamics of the boost voltage, shown in figure 5.11, is suspected to originate from the current controller being wound up, by the time the power is switched on to the system. Therefore attention should be assigned to implementing an anti wind up loop in the controller.

Furthermore, tests should be carried out, where more power is drawn from the boost converter. Test results at a higher load should reveal if the controller needs retuning or even configuration, in form of changing the control strategy. Above all, test results of a better resolution must be captured, in order to determine, whether the current is conducted in a sine wave shape, with a larger amplitude than the simulation result, or whether the boost converter is operating in DCM.

Since the model results shows a significant discrepancy from the measured results, some attention should be directed to refining the model. In particular if the model is intended as a tool for redesigning the control structure.

List of Corrections

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