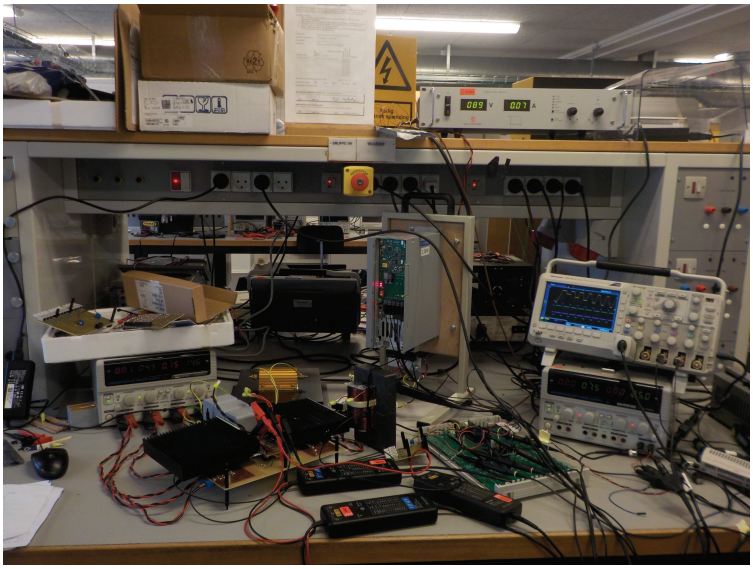
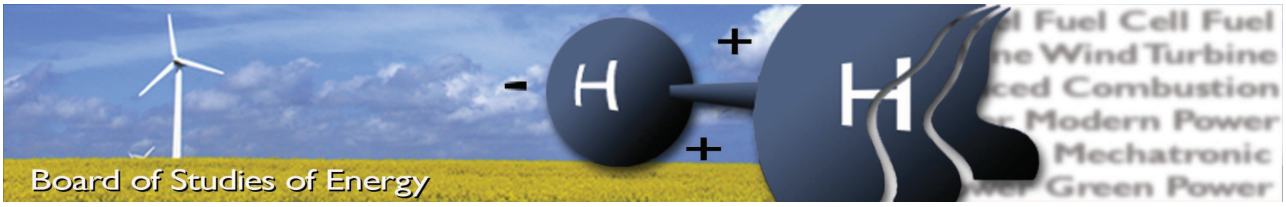
Serial Connection of Three Phase Converters



Master Thesis

WPS4 1054

Aalborg University
Department of Energy Technology
Pontoppidanstræde 101
DK-9220 Aalborg



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Theodoros Kalogiannis

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SYNOPSIS:

This Master thesis deals with the analysis, simulation and implementation of serial connected converters. The focus is laid on the design of a single phase equivalent cell, comprised of a standard three phase - two level voltage source inverter connected in series with a bidirectional full bridge converter via a high frequency transformer. In order to realize the high frequency operation of the transformer a modification in the sinusoidal PWM is implemented. Also, several schemes for commutating the bidirectional full bridge are analyzed, simulated and tested. Transformer design aim on the minimization of leakage inductances and for this reason three prototypes are constructed compared.

By signing this document, each member of the group confirms that all group members have participated in the project work, and thereby all members are collectively liable for the contents of the report. Furthermore, all group members confirm that the report does not include plagiarism.

Preface

The "Serial Connection of three phase Converters" Master thesis was conducted in Aalborg's University (AAU) Institute of Energy Technology as the final part of a total two years Master program entitled 'Wind Power Systems'. The project corresponded to 50 ECTS long Master Thesis and it was written by 10th semester student.

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Theodoros Kalogiannis
<tkalog13@student.aau.dk>

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Part I.

Introduction to the Isolated Modular Cell

1 INTRODUCTION

Over the years, the incrementing demand in power transmission capability in terms of voltage levels, have introduced the power transformers into the distribution and transmission networks. Nowadays, they are used to feed the majority of equipments and apparatus of society's daily use, from personal to public technological environments in the range of several VAs to GVAs, and a few mV to MV. Such flexibility have rendered transformers as one of the most vitals links from transmission and distribution generation to the consumers, while feeding electricity efficiently and reliably. In general, efficiency, costs, weight and dimensions are the main characteristics that determine the overall effectiveness of the transformers, whereas ongoing demands and specifications for a better, stable and interactive power transmission have rendered technological innovations based on smart devices and power electronic transformers to be deployed.

The main principle of this Master thesis is to design an isolated modular converter cell by serial connecting a standard voltage source inverter with a bidirectional full bridge converter via a high frequency transformer. Hence, rather than designing a grid side transformer for the converter based on the grid 50/60Hz, its design can be implemented based on a target kHz frequency. Future research aims on the serialization of several isolated modular cells for upgrading the voltage levels up to MV ranges.

1.1. Background

The two main distribution transformers categories used in the present are the liquid-filled and the dry-type. As air is the basic cooling and insulating system for the latter ones, they are generally larger for the same ratings. Hence, they are preferred for in or closed to building applications, minimizing the impact of environmentally detrimental fluids and complying with fire safety issues in comparison to the former ones, which are a more compact and cost efficient solution. Furthermore, recent advantages in liquid-filled units surpass certain environmental advantages of the dry types. On the other hand, cast coil windings with solid insulation and vacuum pressure impregnation/encapsulation systems allow dry types to be placed in severe applications, once only suitable for liquid filled units. As a result, choosing the proper transformer for a particular application is complicated, mainly based on its operational characteristics as well as the environmental issues, both dominant in the evaluation process [5, 23]. However, in applications where the power ratings exceed 10MVA (more than 11kV) special designs are implemented to cope with increased mechanical requirements, cooling properties and insulation

levels. Liquid-filled power transformers are usually preferred in order to meet those specifications [1].

During the last century, focus was laid on the best technical solution. More in precise, their progress is based on the improved characteristics of the core materials which lead to a significant reduction of their weight and losses, together with the simultaneous advance of design tools and manufacturing processes [3].

Even though the significant contribution of the transformers in energy transmission, yet they have to deal with upcoming requirements settled by the constant rising society's demands. They should cater for the numerous renewable energies sources introduced to the power grid and the consequences of this volatile power flow, as well as help maintain grid quality [1, 25]. Along with the power system evolution, transformers should fit to the upcoming smart grid. As a result, technological innovations have risen, namely smart and solid state transformers.

1.1.1. Smart and Solid state transformers

The modernism of the power distribution network have also risen the need for new transformer technologies capable of providing additional protection functions, such as on demand reactive power support to the grid, voltage regulation and current limiting, power quality and storage management.

Smart transformer scope on the "precaution and detection of failure conditions early" [2]. Sudden failures may occur due to the unpredictable load demands and are able to cause havoc in the network. Utilities aim to monitor the demands in real time, so that operators can remotely interfere before such conditions occur, granting safe operation and simultaneously protection of expensive equipment [1].

The increment of renewable sources on the grid as well as other parameters as the electric vehicles could lead to overloads of distribution transformers, rendering the need of smart devices necessary. Hence, in order the new technology to be incorporated to the future grid, several innovations are being established, few of them are listed below:

- Intelligent electronic devices which monitor the core, the windings, the oil, tap changer and the bushings of the transformers [2].
- Smart-grid-enabled devices, as digital interfaces for easy connection and communication to the smart grid [1].
- Intelligent transformer substations, contributing to an active load management and fast - automatic fault clearance [25].

However, besides those technological advantages in the field, the increment of distribution transformers is inevitable. Concurrently, as an attempt to decrease the cost and the volume of those, Solid State Transformers based on power electronics circuits are being further investigated to determine whereas they appear a profitable and effective solution for the future power distribution infrastructure. These power electronic based transformers combine semiconductors and high frequency transformers in order to provide a high level of flexible control to power distribution networks [9, 17]. Moreover, a smart protection pattern can be elaborated, considering the controllable nature of power electronics switching devices.

1.2. Problem statement

Considering the discussions of the previous section, in order to meet the upcoming requirements in the transformer technology, it is evaluated in this Mater thesis whereas the placement of the transformer on the power converter's side will be an optimal solution, dealing with both efficient and reliable results

as well as with a reduced volume and overall installation and maintenance costs. The idea is based on the usage of conventional three phase - two level inverters, along with high frequency links and bidirectional power electronic circuits.

Regarding the aforementioned concept, the following statement is formulated:

- Is it possible to serial connect three phase converters and introduce the grid side transformer into the converters?

1.3. Isolated modular converter cell

The first step to assess the formulated statement, is to analyze the isolated modular converter cell topology. For this scope, a proposed configuration of a single phase equivalent is presented in Fig. 1.1, which serializes the inverter with a bidirectional converter.

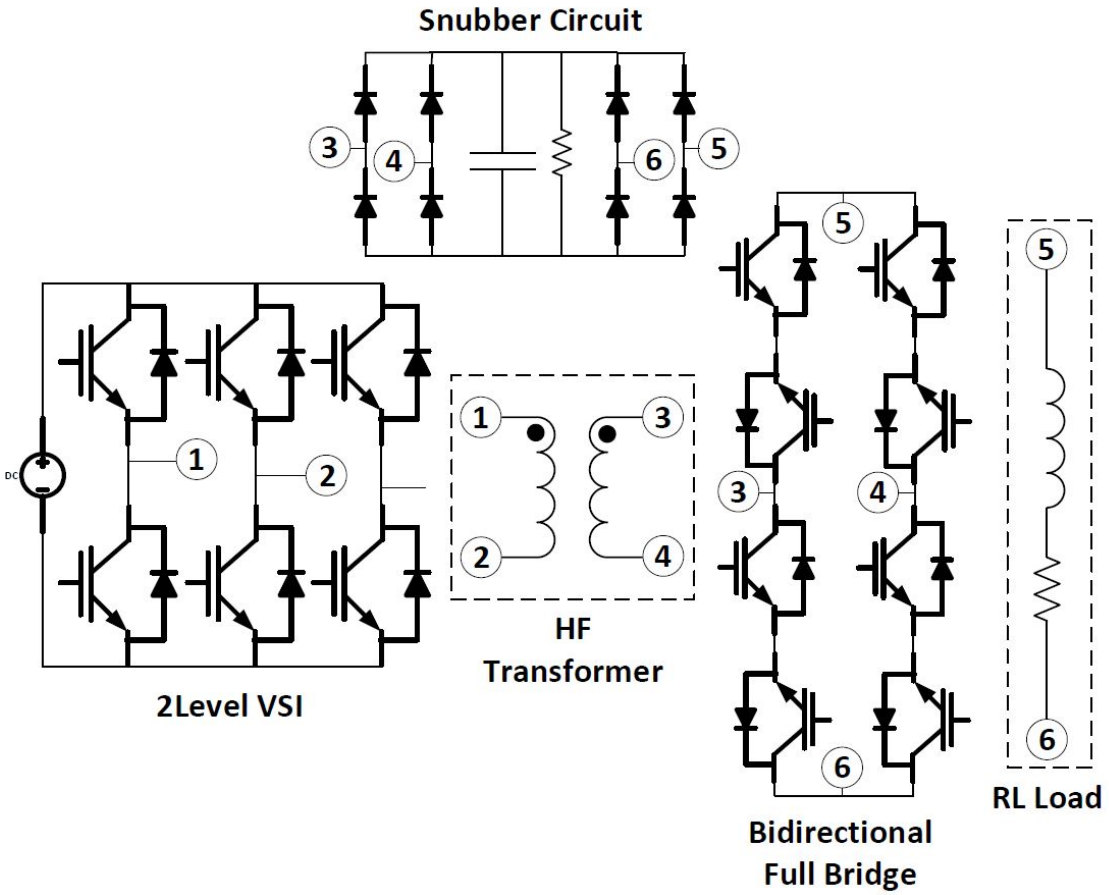

Figure 1.1.: Single phase topology of the isolated modular converter.

The proposed isolated modular cell is composed by a standard 2-level Voltage Source Inverter (VSI), where each of the output phases is connected to a bidirectional Full Bridge (FB - ac FB) converter via a High Frequency (HF) transformer. To achieve that, a modification in the modulation scheme has been performed in order to introduce a HF signal, at the desired frequency, at which the transformer will operate, as it is furthered discussed in the next chapter.

For the single phase isolated cell, the inverter is implemented by using a 2.2kW VLT Drive, which is connected to a dc link voltage up to 300V. The phase voltage of the inverter is supplied to the transformer primary windings, which consequently feed the bidirectional FB. Commutation strategies at the

transistors of the ac FB can lead to overvoltages and overcurrents or at load current discontinuities. To cope with these challenges, a snubber circuit composed of rectifier diode bridge and a clamp capacitor become part of the topology, connected at the input and output of the ac FB as shown in the figure.

The transformer is designed to operate at the switching frequency and tolerate the peak current and voltage ratings at its inputs. Consequently, the absolute power ratings of the transistors of the bidirectional FB converter are defined by the transformer's output voltages and currents.

One of the major design specification of the converter is the selection of the appropriate transistors. The appropriate configuration is based on the four quadrant switches (4QSWs a.k.a. bidirectional or bilateral switches) characteristics, i.e. their ability to conduct currents in both directions and block voltages of either polarities. Those can be implemented by special topologies of the conventional one-quadrant discrete semiconductor devices along with diodes, since such topologies are not currently on the market. Fig. 1.2, shows three different ways of this topology, as well as the general equivalent symbol (b) and the 4QSWs operation area (a).

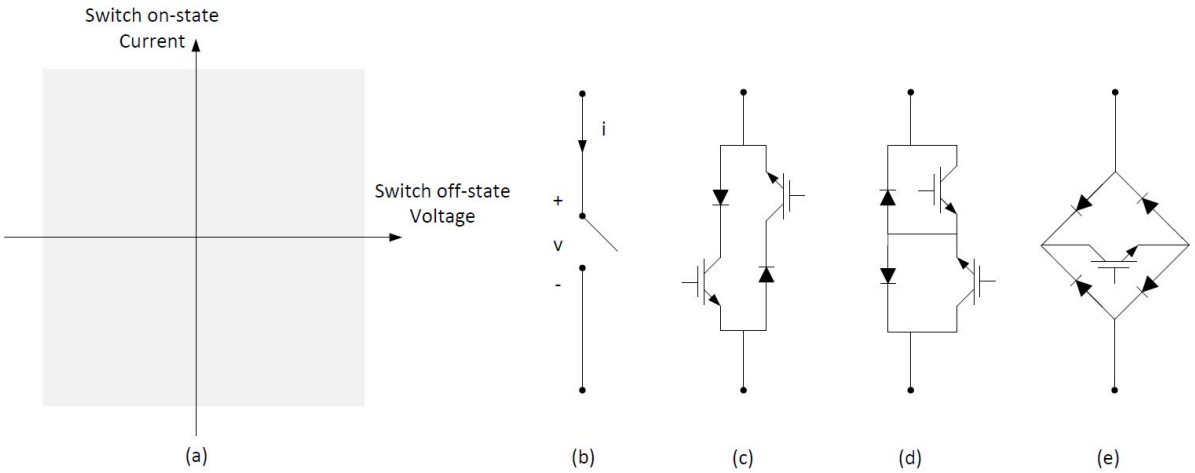

Figure 1.2.: Three ways of implementing a 4QSWs topology [8].

Circuiting the switches as topology (e), also known as diode embedded unidirectional switch [22], requires one discrete transistor and four diodes which facilitates the control procedure since it is requiring only one gate drive per switch, but accounting for higher conduction and switching losses, due to the operation of two diodes and one transistor (three devices) in every instant. Furthermore, the direction of the current through this switch cell cannot be controlled, which accounts as a drawback when commutation strategies require this feedback.

On the other hand, the topologies (c) and (d) come with the same results as far as their control strategy and their losses are concerned, and they are implemented by placing two discrete transistors with common collector or common emitter terminals back to back. Diodes are used to provide the reverse blocking capability of the switch. However, due to the single transistor - diode current path during conduction times, lower on-state losses can be achieved [15]. An advantage of (d) topology is the central common connection, not only because discrete transistors with embedded diodes can be used, but also because it provides transient benefits during switching instances [29]. Hence, topology (d) is being selected.

A drawback of the selected topology could be the necessity of two gate drive circuits for controlling one 4QSW, nevertheless this is overcomed by using half bridge drivers, as it is later discussed in section 5.5.

1.4. Objectives

After the topology of the proposed isolated modular converter cell is presented, and based on the formulated problem statement, the main objectives of this Master thesis are defined as:

1. Design and optimize a single phase transformer operating at the switching frequency of the converter focusing on the minimization of the leakage inductance.
2. Implement a modified PWM scheme for the operation of conventional 2-Level / 3 phase converter by introducing a high frequency component at the switching frequency at which the transformer operates.
3. Implement an optimized modulation scheme for the commutation of the bidirectional full bridge which minimizes the risks of overvoltages and overcurrents.
4. Validate the functionality of the modulation techniques of the converter based on simulations in PLECS and compare microcontroller results.
5. Analyze, design, build and test a single phase cell of the proposed dc-ac isolated modular converter.

1.5. Constraints

The constrains of this thesis are listed below:

- During the implementation of the modified PWM control strategy, it was required and selected, to generate the gate pulse for the inverter using an approximation to the desired method, the influences of which are analytically discussed and compared through simulation models using PLECS software in the section 2.1.
- Voltage levels of the laboratory experiments are limited to 300V for testing the inverter-transformer operation, and to 80V for testing the complete single phase cell due to a short circuit during the start up procedure, as it is further explained in section 6.1.

1.6. Project Outline

Chapter 1 of the Master Thesis, the influence of the grid side transformer and evolutions that take place to incorporate them to the modernized power grid with smart or solid state devices, are stated. Also, the problem statement formulation is defined and a proposed isolated modular converter is introduced with its topology being analyzed. Further, the objectives and constraints for realizing the formulated problem are discussed.

Chapter 2, analyzes the control strategy for serializing the inverter with the high frequency transformer and the bidirectional converter is analytically explained. A modification of the sinusoidal PWM scheme is implemented in order to introduce a high frequency component at which the transformer operates. Then, commutation patterns for the bidirectional FB are presented.

Chapter 3, focus on the analytical design of the high frequency transformer, where several techniques for minimizing the leakage inductance are implemented and compared.

Chapter 4 deal with the generation of the gate pulses and several synchronization challenges for serializing the converters are discussed.

Chapter 5 the design procedure of the converter components takes place. Since the VSI is implemented with a VLT Drive, the chapter analyzes the drive circuit for the bidirectional transistors. The generated pulses for verifying the functionality of the drive circuit are presented.

Chapter 6 test cases are conducted both in simulation models and in laboratory experiments, to validate the functionality and the behavior of the converter.

Chapters 7 and **8**, discuss respectively about the conclusions and the future work of this thesis.

At the **Appendix** part, printed circuit boards of the converter, microcontroller code for both modulation strategies and PLECS models are annexed.

Part II.

Converter Modulation

2
Proposed Converter Modulation

This chapter analyzes the modulation techniques for the VSI and the bidirectional FB. Focus is laid on the modification of the sinusoidal PWM, which is introduced for the transformer operation at high frequency, implemented by introducing a high frequency component in its process. This modification is presented with two different approaches which their ON times and frequency domains are compared to state the functionality and approximate the laboratory results. Further, the commutation of the bidirectional bridge is analyzed, focusing on the 4 steps modulation.

2.1. Control of the VSI

In sinusoidal PWM a reference signal V_{ref} operating at a low frequency, is compared to a carrier-triangular waveform which operates at the desired switching frequency. In order to introduce a high frequency component in the modulation scheme, the reference signal is changed to a high frequency one by undergoing amplitude modulation. More accurately, the procedure followed is based on the Double Side Band - Suppressed Carrier modulation (DSB-SC) where the information is contained only in the sidebands, since the carrier is significantly reduced or ideally completely suppressed.

$$V_{ref} = \widehat{V}_{ref}\, sin\left(2\pi f_{ref}\, t\right) \tag{2.1}$$

This is achieved by multiplying V_{ref} with a square wave function V_{sgn} which alternates between ± 1, operating at a desired switching frequency $f_{sw} = 2kHz$ and is in phase with the carrier i.e. for a positive slope of the carrier the square wave has negative values and vice versa. During the process, the amplitude of the high frequency square signal takes on the shape of the low frequency reference, which forms the so called modulation envelope. The new signal generated from the modification is named denoted as V'_{ref} and is the new reference waveform for the generation of the gate pulses.

Since the carrier square wave signal contains a series of harmonics, the generated waveforms will consequently contain a number of frequencies. Mathematically, this is indicated at the frequency spectrum which based on Fourier Transform and given that the square signal has a fifty percent duty cycle, is the following:

$$V_{sgn}(t) = \frac{4}{\pi} \sum_{n=1,3,5..}^{\infty} \frac{1}{n} sin\left(\frac{n\,2\pi\,t}{T_{sw}}\right) \tag{2.2}$$

where $T_{sw} = \frac{1}{f_{sw}}$ is the switching period.

So, considering that the carrier signal is a series of sine waves, the new signal V'_{ref} is generated at each of those odd harmonics of the carrier frequency, i.e. f_{sw}, $3f_{sw}$, $5f_{sw}$...

The DSB-SC modulated signal is characterized in a general form in time domain, defined in Eq. 2.3. Also, a phase shift might be observed during the zero crossings of the modulation signal in case it occur simultaneously with the zero crossing of the carrier [16].

$$V'_{ref}(t) = A V_{ref}(t) V_{sgn}(t) \tag{2.3}$$

where $A = 1$ is the amplitude of the carrier. By rearrangement:

$$V'_{ref}(t) = \widehat{V}_{ref}\, sin\left(2\pi f_{ref}\, t\right) \frac{4}{\pi} \sum_{n=1,3,5..}^{\infty} \frac{1}{n} sin\left(\frac{n\,2\pi\,t}{T_{sw}}\right) \Longrightarrow$$

$$V'_{ref}(t) = \frac{4\,0.8}{\pi} \left(sin(100\pi t)\right) \sum_{n=1,3,5..}^{\infty} \frac{1}{n} sin\left(n\,2000\,2\pi\,t\right) \Longrightarrow$$

$$V'_{ref}(t) = 1.01 \sum_{n=1,3,5..}^{\infty} \frac{1}{n} \left[sin\left(n\,2000\,2\pi\,t\right) sin(100\pi t)\right] \Longrightarrow$$

$$V'_{ref}(t) = 0.505 \sum_{n=1,3,5..}^{\infty} \frac{1}{n} \left[cos\left(2\pi n(1950)t\right) - cos\left(2\pi n(2050)t\right)\right] \tag{2.4}$$

It can be observed that changes in the switching frequency have no impact on the amplitude of the sidebands. A closer look at the frequency domain shown in Fig. 2.1, highlights the above statements: the new signal operates at the target switching frequency and its harmonics, with two sidebands and a total carrier suppression, achieved by the lack of any dc offsets of the modulation/reference signals.

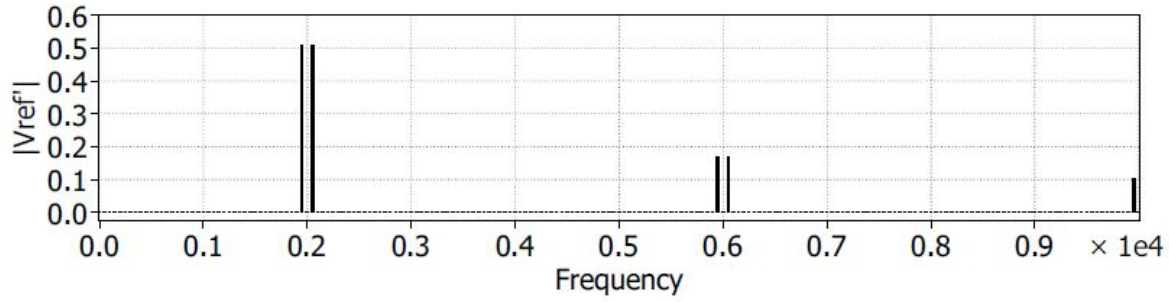

Figure 2.1.: Simulated FFT of the new signal V'_{ref} which is used as reference to generate the pulses for the mPWM. Harmonic magnitude and number in the y- and x-axis respectively, for amplitude modulation ratio 0.8.

2.1.1. modified PWM

In order to derive the control strategy of the VSI and introducing a high frequency component in the modulation (mPWM), the analysis is divided in two main topics i.e the determination of the ON time of the pulses and their frequency spectrum. However, due to the physical operation of the microcontroller (chapter 4) an approximation to the desired scheme is made where the results for both ON times and harmonics are compered.

- ***ON time of the pulses***

The significance in the operation of mPWM is that the compared signals operate at the same frequency, setting the duty cycle of the inverter switches constantly at around fifty percent. To achieve this, the modified modulation can be implemented by comparing the modulation envelope signals i.e. the original signal V_{ref} and its mirrored wave - which has the same amplitude and frequency but a 180^o phase shift, with the triangular carrier. Mathematically, the calculation of ON times can be conducted similarly to the sinusoidal PWM analysis, with the difference that now two low frequency signals are compared to the high frequency carrier. Also, the ON times are determined by the cross section during the down count of the carrier, with V_{ref} and the up count with $V_{ref+180^o}$.

A further analysis should estimate whether or not the same results can be obtained by comparing only one signal. For this purpose, the absolute values of both V_{ref} and the triangular are now compared. If the pulse is toggled for either up or down count, as far as the duty cycle is concerned the exact ON times can be achieved.

A mathematical proof for this statement is described in Eq. (2.5), which follows the equations describing the ON time for a VSI, based on regular sampled sinusoidal PWM [10]. The scope is to derive the ON times firstly for mPWM with two reference signals (DSB-SC), and then verify that the same times for the absolute values occur. Fig. 2.2, shows a graphical approach for the calculation of the ON times.

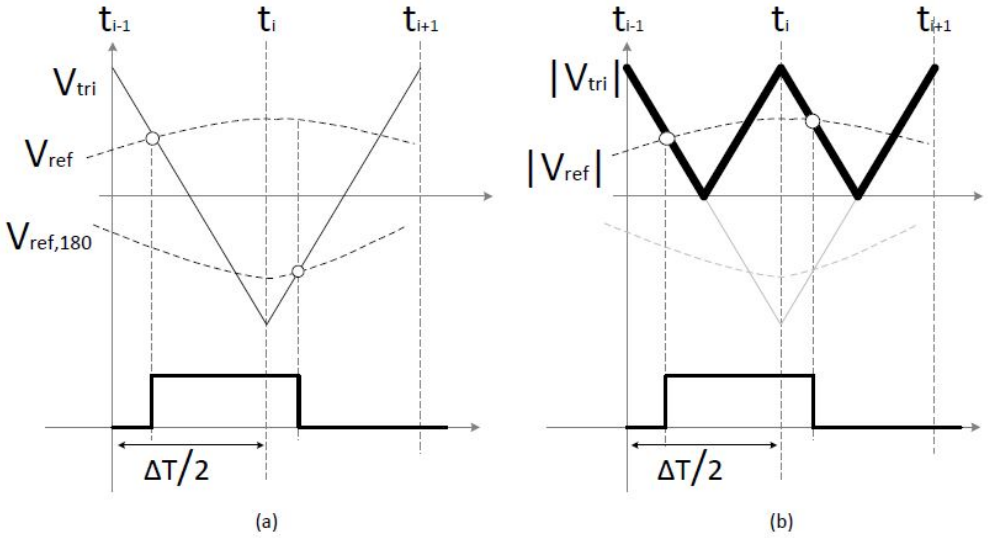

Figure 2.2.: ON times for implementing the mPWM with the DSB-SC (a) and the absolute values (b).

The formula describing for the DSB-SC is the following:

$$T_{on} = \frac{\Delta T}{4}\left[1 + m_a cos\left(\frac{\omega_{ref}\,(t_{i-1} + t_i)}{2}\right)\right] + \frac{\Delta T}{4}\left[1 + m_a cos\left(\frac{\omega_{ref}\,(t_i + t_{i+1})}{2} + \pi\right)\right] \tag{2.5}$$

where T_{on} is the ON time in sec, ΔT is the switching period, $t_{i\pm1}$ are time instances in sec determining the switching period.

As far as the ON times of the absolute values comparison are concerned, since of the toggle operation, the double carrier frequency do not affect their calculation and the $t_{i\pm1}$ intervals remain the same. Also, considering that for a ΔT the comparison is between the same cosine V_{ref} and the opposite values of the cosine $V_{ref+180^o}$, due to $-cos(x) = cos(x+\pi)$, the results are the same. The fifty percent duty cycle can be explained with the same relation. This determines that operating the VSI switches with only one reference signal can derive the same results as for the ON times are concerned.

Identical formulas describing the other two phases of the system can be derived by phase shifting the aforementioned equations by 120^o and 240^o. Notice here that in the example of the figure, the pulses coincides when $|V_{ref}|$ is compared with $|V_{trig}|$ and toggled at the down count instances. This takes place for half load period, and for the other half, the pulse is toggled only at the up count intersectioned instances, while the analysis remains the same.

- ***Frequency spectrum***

The next parameter to examine when modulating with the mPWM is the frequency spectrum. The inverter output phase signal contains voltage components at the harmonic frequencies introduced from the new reference signal V'_{ref} and also incorporates a series of harmonics as a consequence of the switching process [10]. It is necessary to evaluate the harmonic distortion of the modulation and compare the several approaches to assess their effectiveness concerning the unwanted harmonic components that each one introduce. For this scope, simulation models are implemented to generate the FFT of the various approaches to the topic and they are presented in Ap. B.

Fig. 2.3, illustrates the harmonic spectrum of the phase and line to line voltages when mPWM is implemented directly with DSB-SC, together with the signals illustrated in time domain.

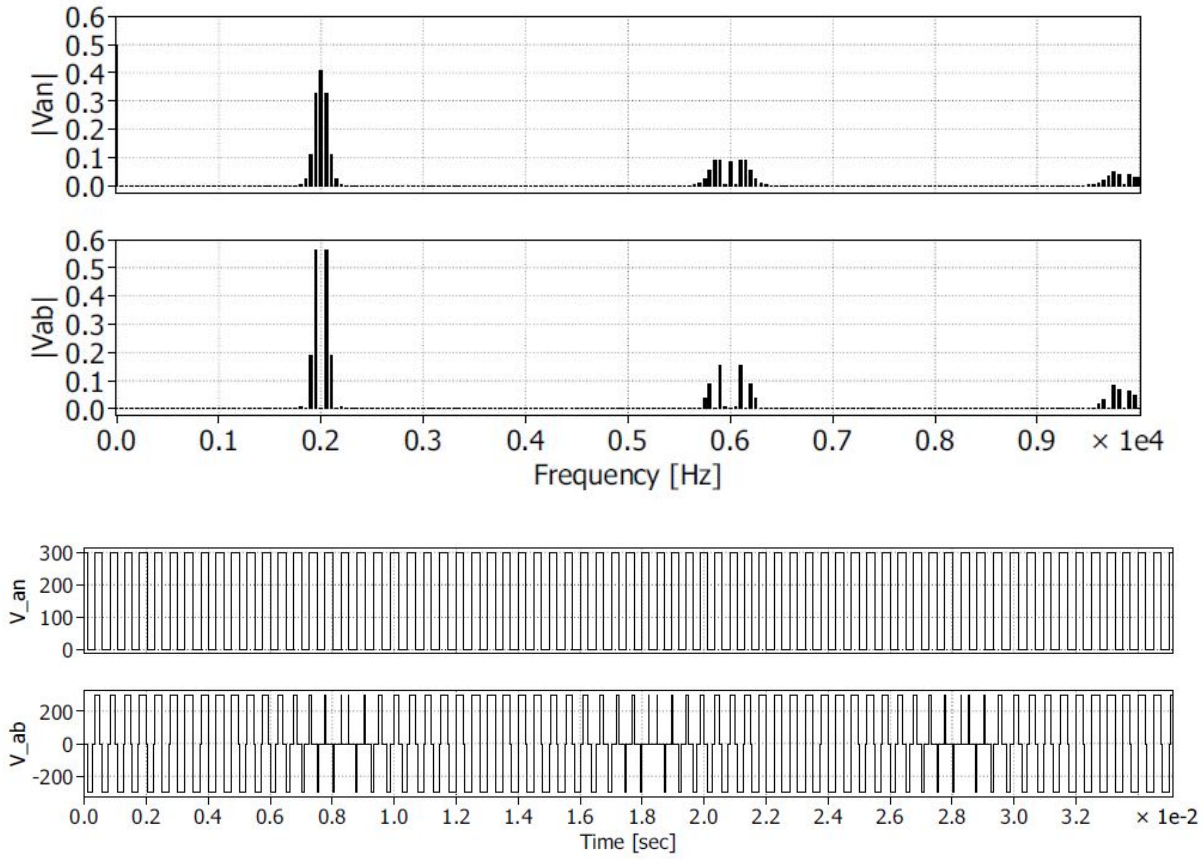

Figure 2.3.: Simulated FFT of the phase V_{an} and the line to line V_{ab} signals (Top) and corresponding time domain (bottom) based on the DSB-SC modulation technique.

It can be observed that the modified modulation varies the duty cycle of the pulses at a high frequency and achieves a high frequency output voltage and current at which the transformer operates. The challenge here is that mPWM deviates from the essential concept of comparing a low and a high frequency signal in order to vary the duty cycle of the pulses. As a result, in order to supply the load with the desired low frequency voltage/current, a rectification of the signals must be implemented. This is the task of the bidirectional FB, and it is later analyzed in section 2.2.

The resulting phase leg output is a train of pulses switching between zero and the dc link value, having a fundamental component at the 2kHz desired frequency. Due to the same switching frequency of the reference and the triangular waves, the phase and accordingly the line voltages have no low frequency harmonics.

The same spectrum results by comparing the absolute values of the carrier and the reference. Nevertheless, since this approach is not applicable via a microcontroller, a similar approach is implemented (with doubling the counter frequency) and it is further explained in "Microcontroller" chapter 4.1.1. Thereafter, two different approaches of this modulation, are shown in Fig. 2.4.

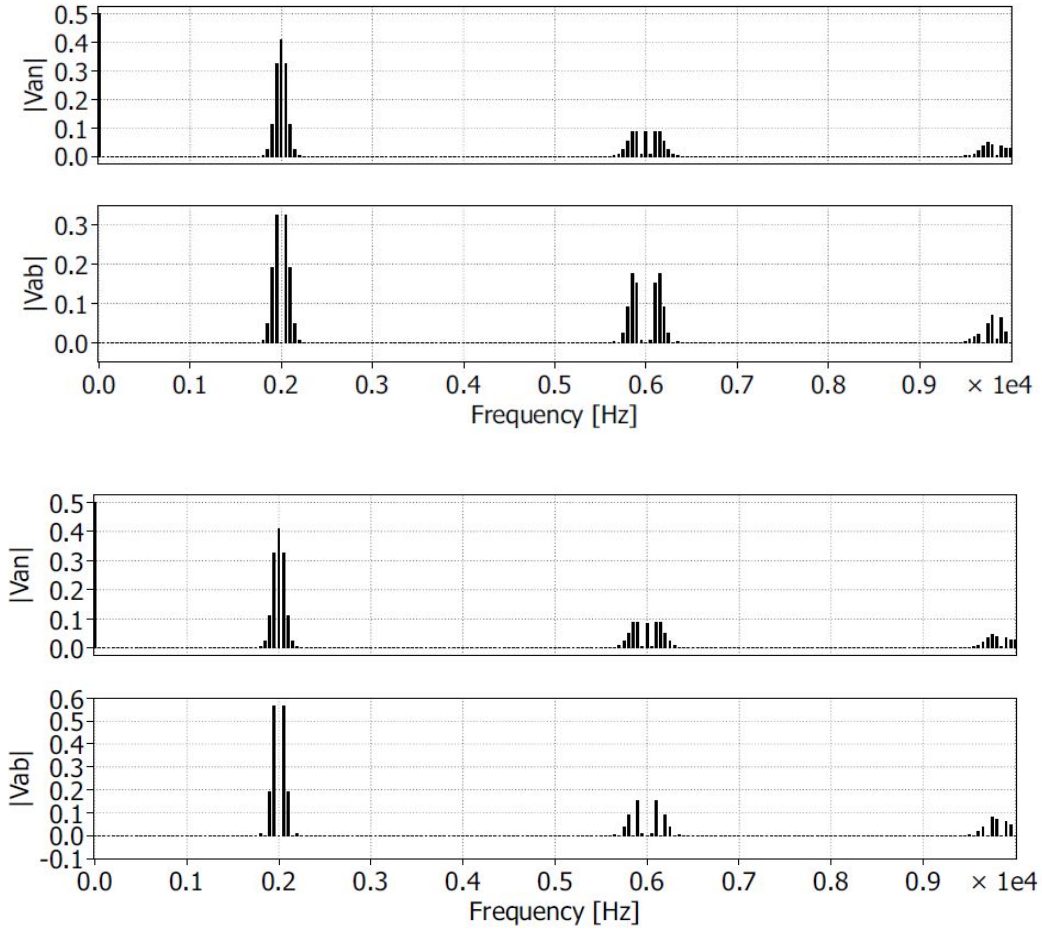

Figure 2.4.: Simulated FFT of the phase V_{an} and line to line V_{ab} signals based on the comparison of the absolute values. Figures illustrate the importance on the correct count registers setting. Top figure without equal separation. Bottom figure with the exact.

The top figure illustrates the harmonic distortion of the signals using an inefficient implementation of the method. As mentioned at the ON times section, the up-down count ought to alternate every half period. Besides the original phase shift of the three phases, a similar shift has to be considered for this alternation. Consequently, the signals in time domain have significant difference, especially the currents. These results are explained analytically in the following chapter 4. Here, Fig. 2.5, illustrates the phase and line voltages in time domain for not having any phase shift between the count modes.

Nevertheless, by comparing the FFT of both approaches (DSB-SC and absolute values with correct-phase shifted counters) the resemblance of the signals is noticeable.

Lastly, Fig. 2.6, shows the FFT of the phase and line voltages, generated from the microcontroller based on the absolute values approach.

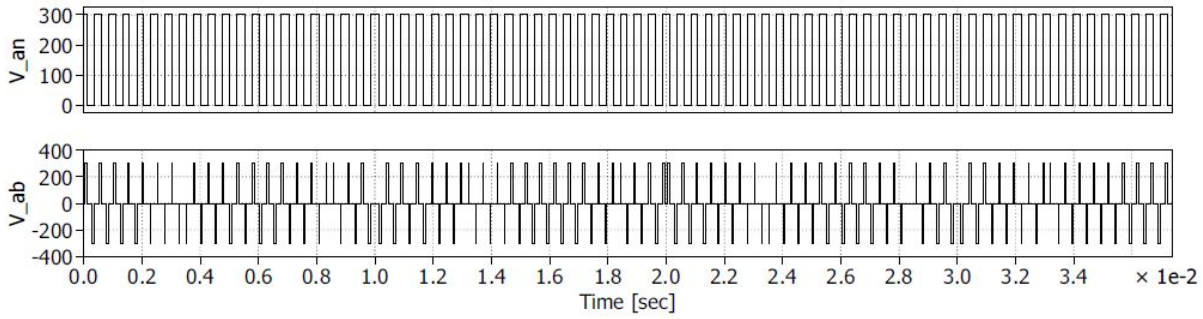

Figure 2.5.: Simulated time domain of phase and line voltages without considering the phase shift on the counters.

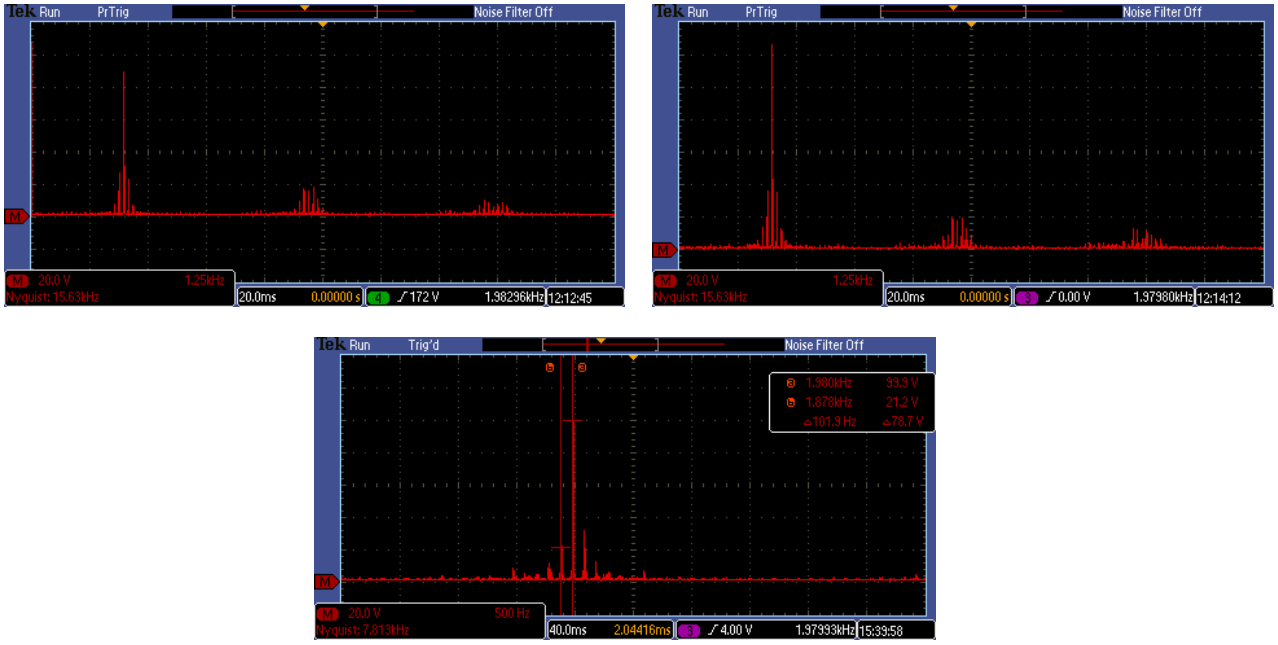

Figure 2.6.: FFT of the phase V_{an} (left) and line to line V_{ab} (right) voltages generated from the dsp. Bottom image focus on the phase voltage to signify the 100Hz spread of the sidebands.

The harmonic distortion of the signals are considered acceptable for driving the inverter and also the transformer. However, a spread on the sidebands at $f_{sw} \pm 100Hz$ is noticed.

2.2. Control of the bidirectional Full Bridge

The bidirectional switches and their control strategies are being analyzed over the years, aiming to implement a variety of power converter circuits for several applications, with the most known being the matrix converters [6, 19, 29].

In the current work though, the purpose of the bidirectional FB is to convert the high frequency input components, to low frequency (50/60 Hz) at its terminals, so that to supply an inductive load, while the rectification of the voltage according to its polarity occur. For this reason, the 4QSW are acquired and they are controlled based on specific strategies. In comparison to the VSI where only dead time commutation pattern is allowed, the bidirectional FB allows a variety of commutation strategies to be implemented due to its tolerance at short circuits of the input phases [18]. Also, since the main

requirements here are to eliminate destructive overvoltages and overcurrents which might occur, a different approach is presented for the control strategy, divided in two sections, the basic and the advance commutation techniques for the bidirectional FB.

2.2.1. Basic commutation strategies: Blanking Time - Overlap

For the primary case, the two transistors of the 4QSWs can be controlled simultaneously with one gave drive. Ideally, on-going and off-going switches (e.g. A and B in Fig. 2.7) commutate at the exact instant. However, in practical cases, the two simplest control patterns to commutate the 4QSWs are either with a blanking time or an overlapping technique.

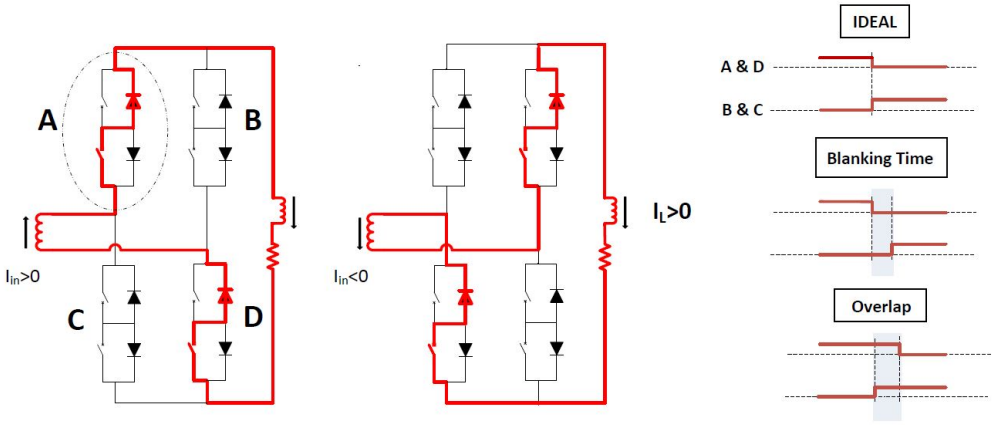

Figure 2.7.: Commutation of the FB 4Q switches. In this configuration the transistors of each switch operate simultaneously.

Nevertheless, these patterns have crucial disadvantages and must be avoided in order to eliminate overcurrents and overvoltages issues at the input and at the load terminals respectively [4, 7, 27]. The former would result in line to line short circuit and converter risk of destruction, however the current continuity at the load is provided in comparison to the latter (overvoltages) which are caused by the absence of this current path and the stored energy at the load which has to be clamped. Fig. 2.8, shows the detailed commutation pattern for the aforementioned cases.

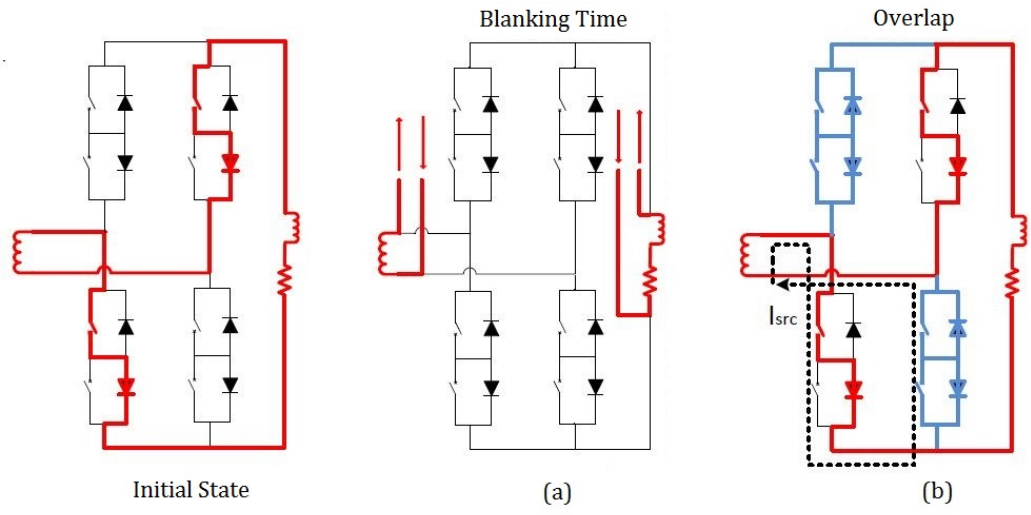

Figure 2.8.: Dead time (a) control and Overlap (b) indicating the need of extra circuitry and the input circulating currents respectively.

The phase current is shown with a red color while the blue is the overlap circulating current I_{src} i.e. the input short circuit current. In the first case, a dead time commutation is introduced to interrupt the operation of the bidirectional FB, causing an instantaneous open circuit of the load, where the current continuity has to be provided by the clamping circuit. In the second case, the on-going switch is turned on before the off-going is set off, overlapping each other. As a result, circulating overcurrents at the inputs during those instances are provoked. A solution to limit these high currents is to add extra chokes in the input terminals. However, this will significantly increase both the losses and the volume of the topology.

2.2.2. Advanced commutation strategies: 4 Steps

In order to overcome these challenges, more reliable control strategies have to be implemented based on current direction or voltage magnitude commutation methods. In comparison to the basic commutation strategies, in this case the two switches of the 4QSW can be turned on and off separately. This advantage results in much less switching losses due to the "semi-soft current commutation" [4, 27, 29]. Such a well known control strategy is the four step commutation in which the current flow through the 4QSW is controlled. Another one is the two step commutation [26, 30], which is a simplest version of the four steps.

More in precise, in the several configurations of matrix converters [12], at a steady state operation both switches are closed, as is shown in Fig. 2.9. When a commutation is required, the current direction is used to determine which of the two switches (of the off-going 4QSW) is non conducting. This is the first step of the control strategy in which the non conductive device is switched off, thereupon disabling the current direction of changing sign.

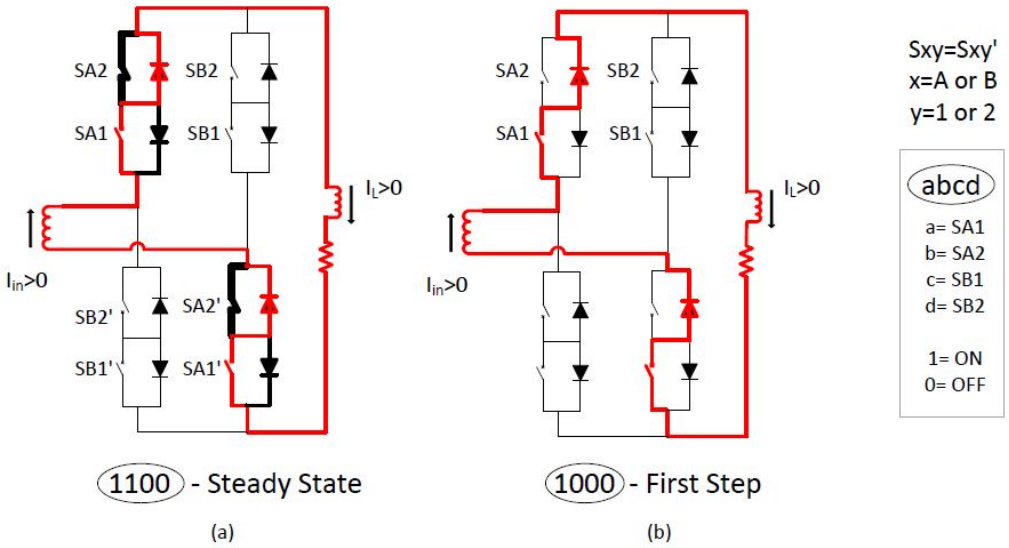

Figure 2.9.: Steady state (a) and First Step (b) of the Four Step Commutation Strategy.

In this example, the input phase current I_{in} is defined positive, as well as the load current I_L. This is arbitrary because similar results as for the frequency and amplitude of the output current can be obtained by reversing the operation of A's and B's devices.

The second step of this strategy requires to fire the on-going switch which will preserve the load current sign. As shown in the following Fig. 2.10, the input current has not changed yet, i.e. this step

follows the overlapping rules, but no circulating currents in the inputs can occur. In the same figure the third step is also shown, which takes place according to the change of the input current sign.

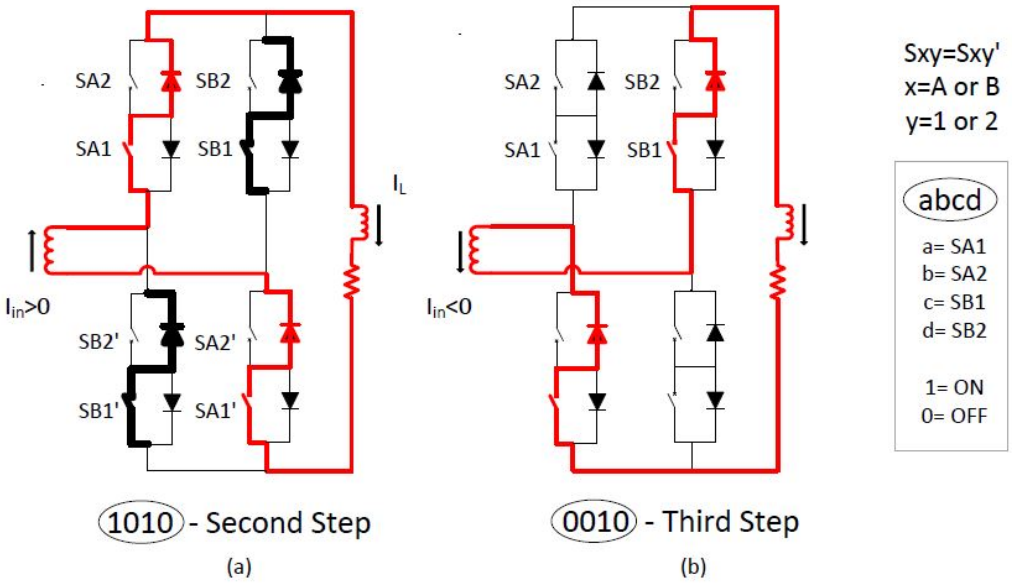

Figure 2.10.: Second step of the strategy (a). Input currents have not changed direction and output current preserves its sign. Third step (b). Only the input current change state.

In this case, the commutation between the off and on-going switches (e.g. from step two to step three) may happen naturally.

The last step includes the firing of the on-going non conductive switch, which is a passive step in order to re-establish the four-quadrant characteristics of the bidirectional switch. Fig. 2.11, illustrates the final process along with a general pattern which includes all the states of the input and output currents, the according states of the switches, within one switching period.

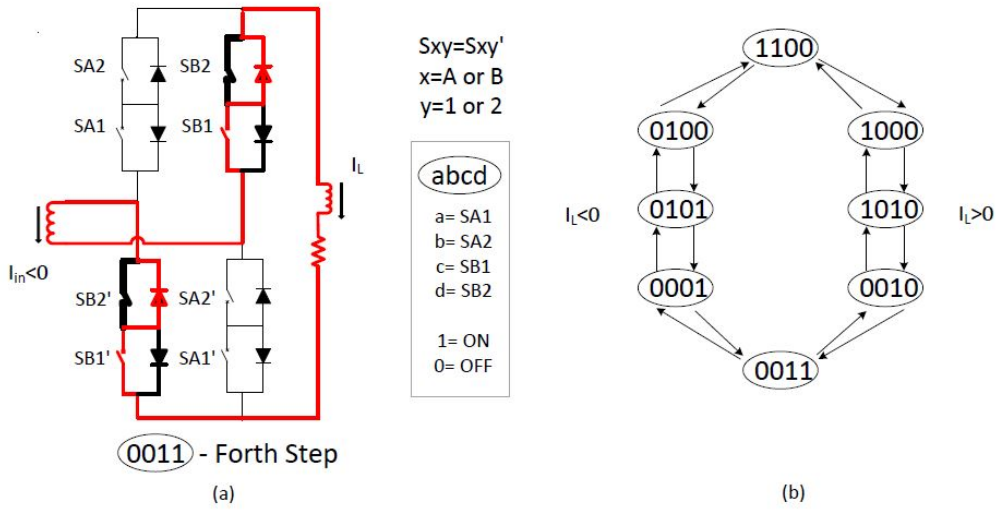

Figure 2.11.: Fourth step (a) and general Four Step commutation strategy (b).

Although the aforementioned steps refer to the operation of the bidirectional FB for a half switching period, a diverse procedure is followed when the load current reverses polarity. Also, steps 1 and 4

are considered passive steps since they do not conduct and so, they might change states faster. On the contrary, the duration of active steps 2 and 3, is critical and must be chosen in agreement with the switching characteristics of the semiconductor devices [28].

By these manners, the general rules for driving the 4QSWs are satisfied [11, 20]. Firstly, by eliminating the risk of overvoltages without open-circuiting the inductive load and secondly by eliminating the risk of short-circuiting the inputs and so protecting from destructive overcurrents.

However, since this control strategy requires a closed loop control with feedback the load current, in some cases where the current levels are low, a reliable determination can be difficult. As an attempt to overcome these uncertainties is to create a "near zero" current zone where commutations are not permitted, technique mainly implemented in the two step strategy. Nevertheless, based on other researches this solution may rise control problems at low current levels and at start-up [29]. Further methods for current detection without using a current transducer are implemented either by measuring the voltage across each switch of the bidirectional based on the on-state and reversed biased values of each device [7], or by measuring the voltage drop across the diodes of the 4QSW connected on the output line [24].

It is crucial in order to construct a reliable matrix converter, to solve the problem of the current commutation between the bidirectional devices. To achieve this it is mainly necessary that

- At any instant, only and at least one switch per leg ought to conduct the current flow, during the positive or negative cycle.

For this reason, the proposed bidirectional FB topology follows a four step control strategy. However, since the topology comprises a single phase cell, it has been selected to commutate the 4QSWs with an open loop control.

Fig. 2.12, shows the theoretical currents flow through the bidirectional switches. It focuses only at the active steps of the modulation. While the load current is positive, the high frequency input current changes polarity and the rectification is accomplished by accordingly commutating SA1 and SB1. Opposite procedure takes place for the negative load current and for its rest half cycle.

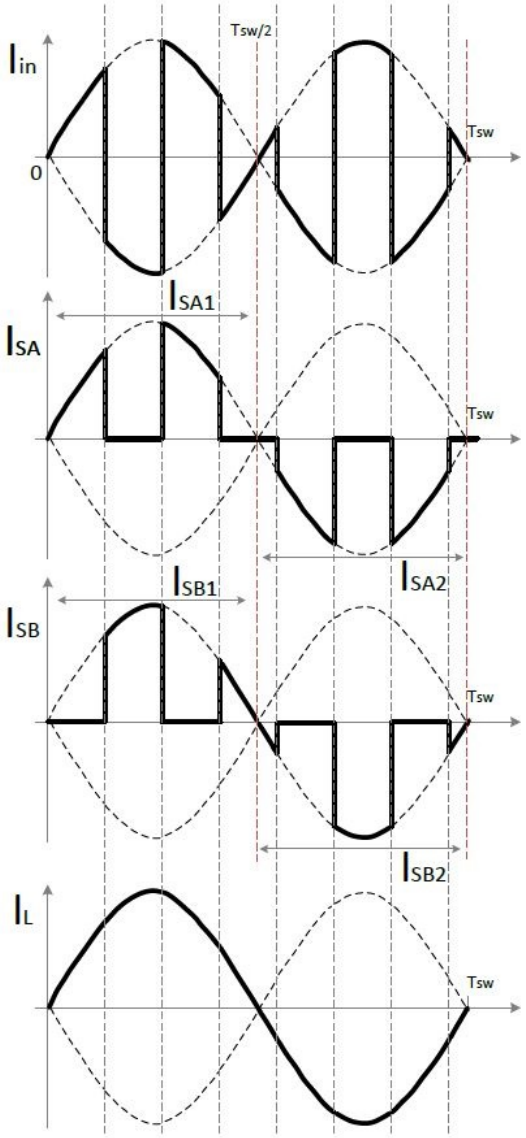

Figure 2.12.: Ideal control scheme of bidirectional FB for one switching period. SA/B are 4QSWs.

2.3. Conclusions

In this chapter, the open loop control patterns for driving the VSI and the bidirectional bridge are analyzed. The focus is laid on implementing the mPWM using one reference signal instead of two, for incorporating with the microcontroller's build in specifications. In order to clarify the resemblance to the desired mPWM, ON times and harmonic distortions of the generated signals have to be examined. For this scope, after defining the functionality according to the ON times, a comparison is made based on simulation models to their frequency spectrum. Thereupon, the microcontroller generated signal are also compared to the simulated, which leads to the decision of accepting them for driving the converter.

The modulation strategies for the bidirectional switches are then analyzed and compared according to their influence on the converters. Overvoltages generated from the blanking time and overcurrents generated form the overlap, impulses to the selection of the 4 steps modulation for driving the transistors of the bidirectional FB.

The following chapter analyzes the generation of those via a microcontroller.

Part III.

Hardware-Software Design Procedure

3
TRANSFORMER DESIGN

In this section, the design of the transformer is analyzed, by firstly choosing the proper core material and shape, and secondly setting the main parameters of the transformer based on the application and the geometrical constant K_{gfe} design method. The proper selection is decided after comparing a wide range of transformer cores, to the ones that comprehend the saturation limits and other important consideration such as the total power losses. Lastly, several techniques for minimizing the leakage inductance are presented and designed.

3.1. Magnetic Core

As far as the core is concerned, both the most suitable material type and volume are determined in the following section.

3.1.1. Magnetic Material

The choice of the magnetic material is of paramount importance in the design of magnetic components. Several of the most know include silicon steel, nickel iron, powdered iron and ferrite [21]. The most appropriate should be determined accounting a number of parameters, such as the saturation flux density B_{sat} of the material, the total power losses P_{tot} and the operating frequency f_{sw} [8].

An important constraint for the design of the transformer is that the peak flux density ΔB is not exceeding the saturation flux limits of the material (B_{sat}). In such a point, further increase of the magnetic field's force causes no increase in the flux density. Considering a transformer, for a constant value of flux, the voltage induced is zero, which leads to a short circuit of the windings.

However, core materials can be among iron alloys and other similar materials which have saturation flux density limits up to 1.5 - 2 Tesla, in comparison to the powdered cores (0.8T max) or to ferrites (0.25 - 0.5 T). On the other hand, core losses are lower for the ferrite cores compared to the good electrical conductors materials, due to their high resistivity which results to the decrement of Joule losses on the core. Precisely, since these losses are proportional to the frequency, silicon steel materials are used in applications with low frequencies in the range of Hz. On the other hand, in the range of a few kHz up to 100kHz powdered cores materials are used and as the resistivity increases further, for

ferrite materials, they are typically used in applications of several kHz up to MHz. However, the final choice of the magnetic material is based on achieving the desired characteristics in accordance to an optimum cost, size and performance of the transformer and hence, for the current work a transformer using ferrite material is chosen. As for the shape of a ferrite core, can be among to almost all shapes (EI,EE,FF,UI,LL,UU). Although the more mean magnetic length path the more total core losses, it is selected to work with a double U topology since it is facilitates the build up procedure and simultaneously complying with all the requirements.

3.1.2. Core Size Selection

According to the core geometrical constant method, the core size can be determined from the following Inequality Constraint:

$$IC = \frac{\rho\, \lambda_1^2\, I_{tot,rms}^2\, K_{fe}^{(2/\beta)}}{4 K_u\, (P_{tot})^{[(\beta+2)/\beta]}}\, 10^8 \tag{3.1}$$

where K_u is the window utilization factor, the part of the core window area that is filled with copper and is assumed 0.4 for the current two winding application. Also, λ_1 are the applied volt-seconds (flux linkages) during the positive portion of the voltage waveform at the transformer's terminals, ρ is the resistivity of the conductor material and equals to $1.724 \cdot 10^{-6}\, \Omega/cm$, K_{fe} - constant of proportionality depended on frequency - and core loss exponent β are determined by fitting Eq. 3.14 to the manufacturer datasheet (typically β value for ferrite materials lies between 2.6 and 2.8), and $I_{tot,rms}$ is the total rms winding current referred to the primary. The total power losses $P_{tot} = 7W$ are considered here one percent of the total active power per phase.

In order to determine the parameters K_{fe} and β, the Power Core Losses characteristic for a ferrite material is shown as an example in the next Fig. 3.1. The procedure followed to derive the parameters is analyzed, as an example for the determination of the most appropriate core.

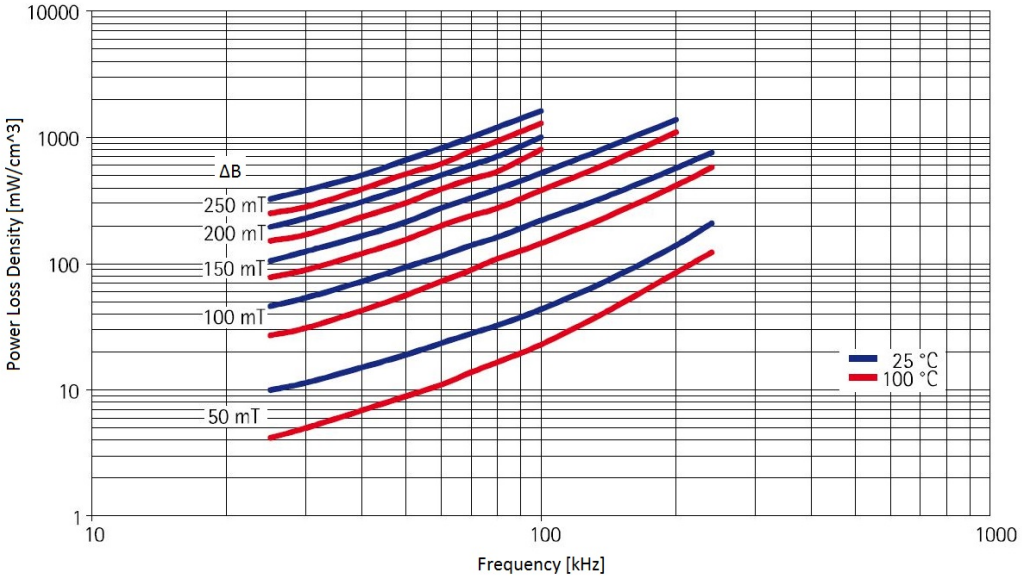

Figure 3.1.: Core loss data for the TRIDELTA Ferrite material Mf196.

Firstly, β is calculated from the slope of the Power Loss Density to the peak flux density ΔB for a given frequency. This slope is defined based on two random data points on the exponential curves as:

$$\beta = \frac{log(90) - log(5)}{log(150) - log(50)} = 2.6309 \tag{3.2}$$

where (5,50) and (90,150) refer to the data for 30 kHz and 100 C degrees. Subsequently, by rearranging Eq. 3.14,

$$K_{fe,at\,30kHz} = \frac{Power\ Loss\ Density}{\Delta B^{\beta}} = \frac{5 \cdot 10^{-3}}{(50 \cdot 10^{-3})^{2.63}} = 13.20 \tag{3.3}$$

Since K_{fe} is directly proportional to the operation frequency, it is scaled to the 2 kHz chosen for this application. To do so, it is once again estimated at 90 kHz.

$$K_{fe,at\,90kHz} = \frac{20 \cdot 10^{-3}}{(50 \cdot 10^{-3})^{2.63}} = 52.81 \tag{3.4}$$

As a result, for a 3 times higher frequency the constant becomes almost 4 times higher. Accordingly for the 2 kHz (i.e. 15 times decreased from the 30 kHz) ought to be 20 times less:

$$K_{fe,at\,2kHz} = 0.66 \tag{3.5}$$

Considering now a UU 103_80_30 core, from the manufacturer datasheets it is obtained:

Parameter	Value
$A_{C,min}$	8.32 cm^2
l_m	38.9 mm
W_A	23.04∗2 cm^2
V_e	327000 mm^3
MLT	∼20 cm

Table 3.1.: UU 103_80_30 core parameters.

To proceed, the applied volt-seconds to the primary during the positive portion of the voltage waveform are estimated according to the subsequent formula:

$$\lambda_1 = \int_{positive\ period} V_{in}(t)\,dt \tag{3.6}$$

According to Faraday's law, the voltage induced to an area is directly proportional to the change of flux passing through the surface of this area over time, which leads to the proportionality of the voltage to the flux density B. Since it is prohibited for the ΔB to overpass the B_{sat}, flux linkage is calculated for the worst case scenario, i.e. for maximum applied voltage value. In the case that B_{sat} is reached due to the excessive applied volt-seconds, the flux density becomes constant and short circuit occurs.

The input to the transformers according to Eq. **??**, is a modified square wave which amplitude is determined by the instantaneous three phase differences. Hence, the maximum applied voltage for a positive period equals to:

$$\lambda_1 \approx 0.0587\ V - sec \tag{3.7}$$

The total rms winding current refereed to the primary $I_{tot,rms}$ is calculated, after approximating the rms input voltage to the transformers, which is the line output voltage of the VSI. Hence, considering a dc link voltage of ∼250V and a three phase rated output power value of the VSI at 2.2 kW:

$$I_{tot,rms} = I_1 + \frac{1}{n} I_2 = 2\,I_1 = 2\,\frac{P_{rated,per\ phase}}{V_{in,rms}} = \frac{2/3 * 2.4\,kW}{250} \approx 7A \tag{3.8}$$

Consequently, Eq. 3.1, can be now calculated for the specific core as:

$$IC = 0.662 \tag{3.9}$$

Based on the K_{gfe} core geometrical constant which equals to:

$$K_{gfe} = \frac{W_A\,(A_c)^{[2(\beta-1)/\beta]}}{(MLT)\,l_m^{(2/\beta)}} \left[\left(\frac{\beta}{2}\right)^{-\left(\frac{\beta}{\beta+2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta+2}\right)} \right]^{-\left(\frac{\beta+2}{\beta}\right)} \tag{3.10}$$

where W_A is the window area of the core, MLT is the core mean length per turn, l_m is the mean magnetic path length, A_c is the core cross section area and l_m is the mean magnetic length path.

The selected core should be large enough to satisfy the inequality:

$$K_{gfe} \geqslant IC \tag{3.11}$$

Evaluation of the peak ac flux density is achieved by the below formula:

$$\Delta B = \left[10^8 \frac{\rho\,\lambda_1^2\,I_{tot}^2}{2K_u} \frac{(MLT)}{W_A A_c^3\,l_m} \frac{1}{\beta\,K_{fe}} \right]^{\left(\frac{1}{\beta+2}\right)} \tag{3.12}$$

In this stage, ΔB should not be greater than B_{sat}, taking into account an adequate safety margin to prevent saturation.

Considering the aforementioned procedure, several magnetic cores with different materials are tested in order to select the most appropriate for the application determined by specific power/voltage levels and switching frequency. Results are shown in the following Tab. 3.2.

UU cores with the respective material		K_{gfe}	$Inequality\ Constraint\ IC$	ΔB
26_22_16	Mf 196	0.0283	0.662	1.3432
	Mf 198	0.0308	0.6043	1.385
	Mf 198a	0.0275	0.429	1.5162
46_40_28	Mf 196b	0.1573	0.6448	0.5037
	Mf 198	0.1618	0.6043	0.5158
	Mf 198a	0.136	0.429	0.5503
93_76_20	Mf 196	0.4492	0.662	0.261
	Mf 198a	0.4257	0.429	0.2915
	Mf 102	0.5869	0.3961	0.3227
103_80_30	Mf 196	0.5903	0.662	0.2031
	Mf 198a	0.557	0.429	0.2264
	Mf 102	0.7884	0.3961	0.2532

Table 3.2.: Different core volumes build with several materials are tested to determine the most appropriate one, based on the K_{gfe} criterion ($K_{gfe} \geqslant IC$, $\Delta B < 0.32\,T$).

Results indicate that a magnetic core who meet the application's requirements is type 103_80_30 with material either Mf 198a or Mf 102. A constraint from the proper selection between these two materials can be the total power loss of the transformer.

As mentioned earlier, P_{tot} is assumed one percent of the total power per phase. The actual power loss however, can be estimated by the aggregation of the copper and core losses, i.e. $P_{tot} = P_{fe} + P_{cu}$.
The copper losses P_{cu} at the windings are:

$$P_{cu} = \left(\frac{\rho\,\lambda_1^2\,I_{tot,rms}^2}{K_u} \frac{MLT}{W_A A_c^2} \frac{10^8}{\Delta B^2} \right) \tag{3.13}$$

where W_A is the window area of the core, MLT is the core mean length per turn.
At a given frequency, core losses P_{fe} can be approximated by:

$$P_{fe} = K_{fe}\,\Delta B^{\beta}\,A_c\,l_m \tag{3.14}$$

Their calculation for Mf 198a is $P_{tot,calc,Mf198a} \approx 16W$ and for Mf 102 $P_{tot,calc,Mf102} \approx 11W$. However, according to the design specification they should not be above 7W. Thus, either a bigger volume core has to be chosen, or the same core (103-80-30) with different material. Since neither option was available it is chosen to work with Mf 102.

3.2. Primary turns and Turns Ratio

The primary turns can now be calculated based on:

$$n_1 = \frac{\lambda_1}{2\,\Delta B A_c}\,10^4 = 159.24 \tag{3.15}$$

The turns ratio of the transformer is one, thus the secondary turns equals to the primary:

$$n_2 = n_1 = 160 \tag{3.16}$$

The above turns refer to the magnetic core material Mf 198a.

3.3. Wire sizes

Consequently, the optimal allocation of each windings on the core window area W_A is estimated. The following Eq. 3.17, describes this fraction a_j of the window area of the j_{th} winding:

$$a_j = \frac{n_j\,I_j}{n_1 \sum_{n=1}^{j} I_j} \tag{3.17}$$

The decisions is made so that the total copper loss of all the windings is minimized. Fraction a is a positive real number with values between 0 and 1. Since the turns ratio is one, both windings require the same fraction of the window, i.e.:

$$a_1 = a_2 = 0.5 \tag{3.18}$$

Thereafter, evaluation of the wire sizes takes place according to the following Eq. 3.19:

$$A_{wj} \leqslant \frac{a_j\,K_u\,W_A}{n_j} \leqslant 0.0579\,cm^2 \tag{3.19}$$

where A_{wj} is the core cross-sectional area of the windings or the wire bare area. Once again, since the unity turns ratio the wire sizes selected for the specific core are the same for primary and secondary windings. According to the American Wire Gauge, the most appropriate wire diameter should be 2.3 mm, AWG#10. Due to the instant availability of the 1.7 mm AWG#14, it is selected instead, with the penalty of increased resistivity of the copper wire and hence the total resistance of the transformer.

3.4. Magnetization & Leakage Inductance

Subsequently, the magnetization inductance L_m is estimated as

$$L_m = \frac{\mu\,n_1^2 A_c}{l_m}\,[H] \tag{3.20}$$

where $\mu = \mu_0\mu_r$ is the permeability of the core material, $\mu_0 = 4\pi 10^{-7} H/m$ is the permeability of free space and $\mu_r = 2 \cdot 10^3$ for 20^oC. From the core datasheet, the permeability for 15^oC can be approximated as $\mu = 1600$.

Based on the above the magnetization inductance is calculated as:

$$L_{m,Mf198a} = 109\, mH \tag{3.21}$$

3.4.1. Winding Leakage Inductance

Leakage inductance causes the secondary voltage not to be directly proportional to the primary as in ideal cases. This is the main reason why it should be minimized and for this purpose, three techniques gradually decreasing its value are introduced.

The main winding configuration shown in Fig. 3.2, and is implemented by simply arranging the secondary on top of the primary, with a small space in between where the high voltage insulation tape is placed. Four layers per turn are needed in order to comply with the calculated voltage ratings.

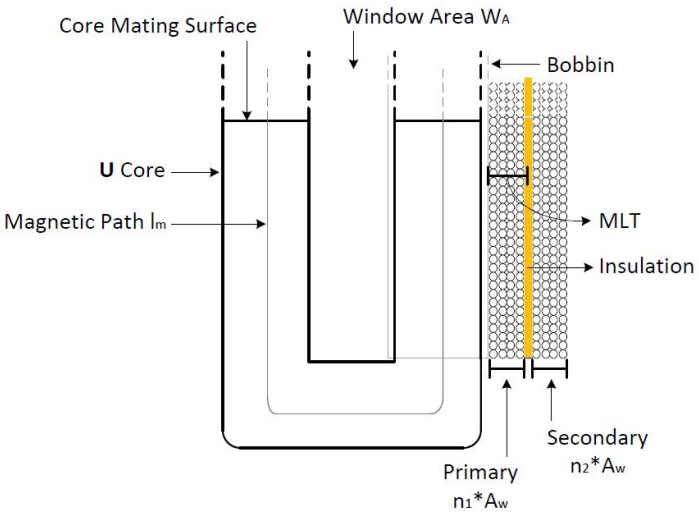

Figure 3.2.: Windings design based on the conventional transformer configuration for implementing transformer#1[21].

Leakage inductance is measured experimentally via a LCR meter, as is seen from both the primary and the secondary to verify the 1:1 configuration. Similarly, the inductance and the total resistance seen from the primary and the secondary are alike. This conventional technique, is a first step for the transformer design, where the parameters are summarized in the following Tab. 3.3.

Parameter	Value primary	Value secondary
L_σ	265 μH	261 μH
R	4.2 Ω	4.2 Ω
Lm	109mH	109mH

Table 3.3.: Main parameters of transformer#1.

The first approach to reduce the leakage is implemented by interleaving the transformer's windings as shown in Fig. 3.3.

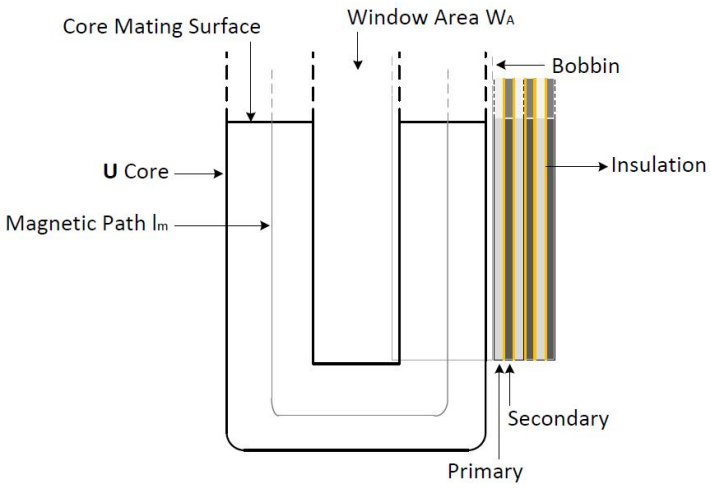

Figure 3.3.: Windings design based on the primary and secondary interleaved configuration for implementing transformer#2[21].

This technique leads to a further reduction of the leakage, which is shown, along with the other main parameters in Tab. 3.4:

Parameter	Value primary	Value secondary
L_σ	$124\,\mu H$	$124\,\mu H$
R	$4.2\,\Omega$	$4.2\,\Omega$
Lm	101mH	101mH

Table 3.4.: Main parameters of transformer#2.

More reduction in the leakage however can be achieved when configuring the windings as shown in Fig. 3.4. Here the primary and the secondary are divided into three same diameter wires, interleaved and sectionalized around the bobbin. This method reduces also the total resistance of the transformer since the current flowing into the wires is divided by three. The flux path should be considered when implementing this configuration since both core legs are used, i.e. the windings should not cancel each other flux path.

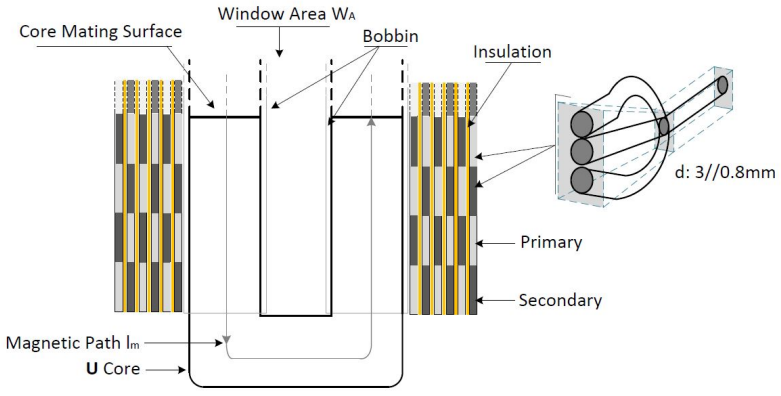

Figure 3.4.: Interleaved and sectionalized windings of the transformer#3.

The main parameters of this configuration are given in Tab. 3.5. It can be noted the significant reduced in both the leakage and resistance of the transformer. The reduce at the magnetization is due

to the less turns per windings implemented without tending to.

Parameter	Value primary	Value secondary
L_σ	$5\,\mu H$	$5\,\mu H$
R	230mOhm	230mOhm
Lm	45mH	45mH

Table 3.5.: Main parameters of transformer#3.

3.5. Conclusions

Based on a Matlab script the parameters obtained from the K_{gfe} criterion are gathered in the following Tab. 3.6. The core size chosen is the TRIDELTA 103-80-30 with the respective characteristics illustrated in this table.

Parameter	Mf 198a	Mf 102	Parameter	Mf 198a	Mf 102
β	2.6	2.79	n_1	160	143
λ	$0.0587\,V-sec$		ΔB	$0.2264\,T$	$0.2532\,T$
ρ	$1.724\cdot 10^{-6}\,\Omega/cm$		L_m	$109\,mH$	$88\,mH$
K_{fe}	0.3858	0.2792	MLT	$\sim 20\,cm$	
K_u	0.4		l_m	$38.9\,cm$	
W_A	$23.04*2\,cm^2$		I_{tot}	$\sim 8.5\,A$	
A_C	$8.32\,cm^2$		f_{sw}	$2\,kHz$	

Table 3.6.: Transformers TRIDELTA 103-80-30 Parameters.

3.5.1. Transformers voltages

Fig. 3.5, shows the voltages at the primary and secondary of the transformers for dc link voltage $V_{dc} = 200V$ and the secondary of the transformers are connected to a low value resistor.

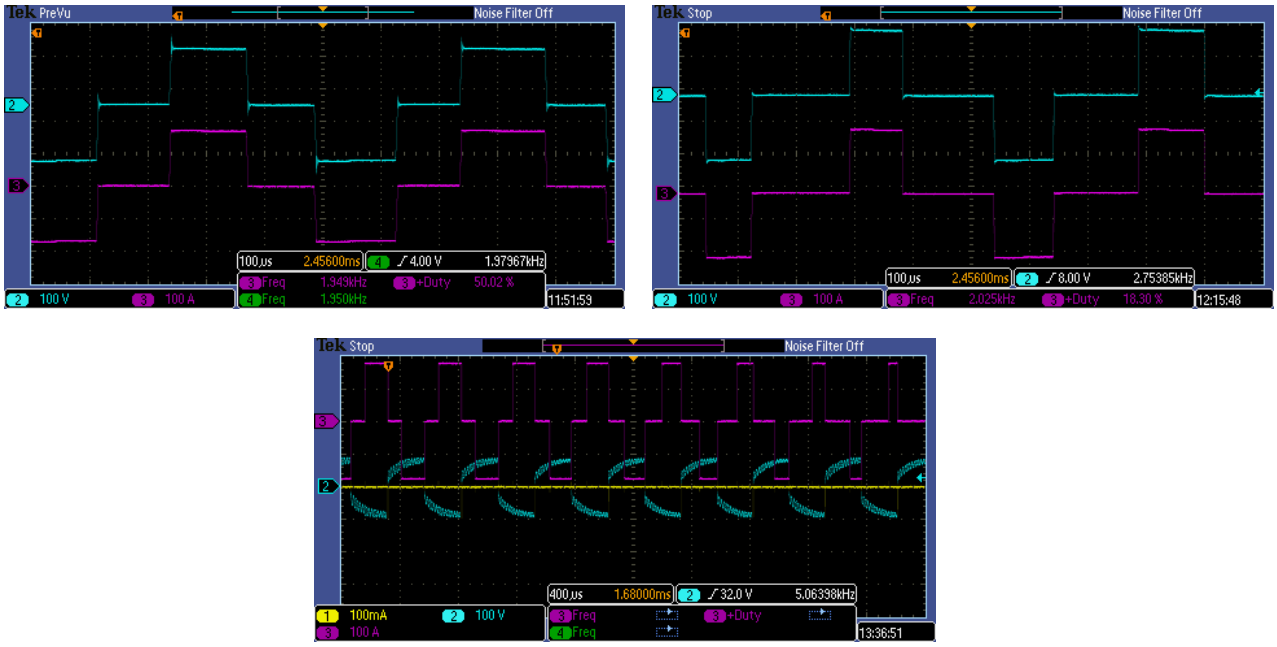

Figure 3.5.: Primary (purple) and secondary (blue) voltages of Transformer#1 (left), Transformer#2 (right), Transformer#3 (bottom) with a resistive load applied to the secondary.

Here, the functionality of transformers#1 and #2 with a inity turns ratio is stated. It can be also noticed the effect of the leakage which creates the spikes at the voltages during the the leading edges. These spikes are caused due to the stored energy and they are proportional to the half value of L_σ times the square of the peak current. As it is observer transformer#1 has the higher leakage hence higher voltage spikes are expected.

However, since the orientation and the spacing of the windings determine the leakage and the capacitance, considering also that these values are reverse proportional, transformer#3 malfunctions due to stray capacitance in the secondary. Unfortunately, it is not a reliable design, thereupon it is not selected for testing the converter.

4 MICROCONTROLLER

In this chapter the methodology for the generation of the code to drive the VSI and the bidirectional FB is analyzed. The modulation pattern follows the mPWM and the 4 Step techniques which are discussed in previous sections. The microcontroller selected for this work belongs to the Texas Instruments C2000 family, i.e. the Delfino F28335 150MHz clock speed, compatible to directly connect and supplied from PC via USB interface and equipped with six individual PWM modules [13, 14]. Each module offers a 16bit time base counter and also two independent output signals making it a preferable solution to drive the VLT drive and the bidirectional switches simultaneously.

4.1. Implementation of the modulation schemes

Each ePWM peripheral represents a PWM channel composed of two individual outputs. All of the modules are identical and able to operate as a single system by a control synchronization scheme. Further, each module consists of seven submodules with the most important to be the counter compare and the action qualifier where the duty cycle and the operation of the PWM are respectively set. The rest are to configure all of the event-timing for the PWM (e.g. period/frequency) and the counter (up/down/up-down), generate dead bands or false tripping actions, and lastly generate interrupts, which can be either internals or externals. However, as mentioned before no observing of the load current direction is held, hence only internal interrupts are acquired to generate the pulses. Also, the up-down count mode for the timer operation is selected, ideal for generating symmetrical PWM waveforms.

4.1.1. mPWM pulses generation

The direct implementation of the mPWM by comparing the modulation envelope signal is not feasible by the psychical construction of the microcontroller. This is due the unavailability of double updating the compare values during both the rising and falling edge of the carrier. However, acceptable results to proceed may be obtained by the absolute values method.

The first step is to generate a sin wave reference signal at the fundamental frequency and then rectify it. The counter of the microcontroller which resembles the carrier waveform, is set to operate at twice of the switching frequency as to also represent a rectified signal. Afterwords, these waveforms are

compared and the pulses change their state with the toggle option. This is the operation for one phase of the VSI. The other two are shifted for 120 and 240 degrees respectively by shifting the carrier.

However, one more shift is required for implementing the change in the count modes every half load period (e.g 10msec), in accordance to the phase shift of each of the VSI phases. In other words, a counting register for phase A starts at $t = 0$ and changes the compare operation from upcount to downcount at $t = 10msec$. Phase B counting register start down counting and at $t = 6.6msec$, which is an 120 phase shift, reverse to up count procedure. Similarly, phase C counting register at $t = 13.3msec$, which is a 240 phase shift, reverse to up count. Because 13.3msec is more than a period, phase C ought to up count for the first 6.6msec.

The last requirement to implement the absolute values comparison is to mirror the sin wave values to the TBPRD axis, where TBPRD is the peak amplitude of the carrier register. This is held in order to precisely approximate the DSB SC modulation, where the triangular and the square wave are in phase, obtaining their peak amplitude at the same time instant. Therefore, the triangular absolute value at $t = 0$ is one, introducing a phase shift compared to the microcontroller counter initial value which is zero. This shift is compensating by mirroring the reference sinusoidal values. Accordingly, the actions of the count registers are reversed.

4.1.2. 4 Steps pulses generation

The implementation of the 4 Steps is achieved by firstly setting the desired overlap for the pulses. Thereafter, two more signals are generated for the passive steps, with a much lower duty cycle. To achieve the overlap two requirements are set:

- the pulses to overlap are shifted from the carrier
- they should have ON times more than half a period

Fig. 4.1, illustrates the operation for getting the 4 steps pulses.

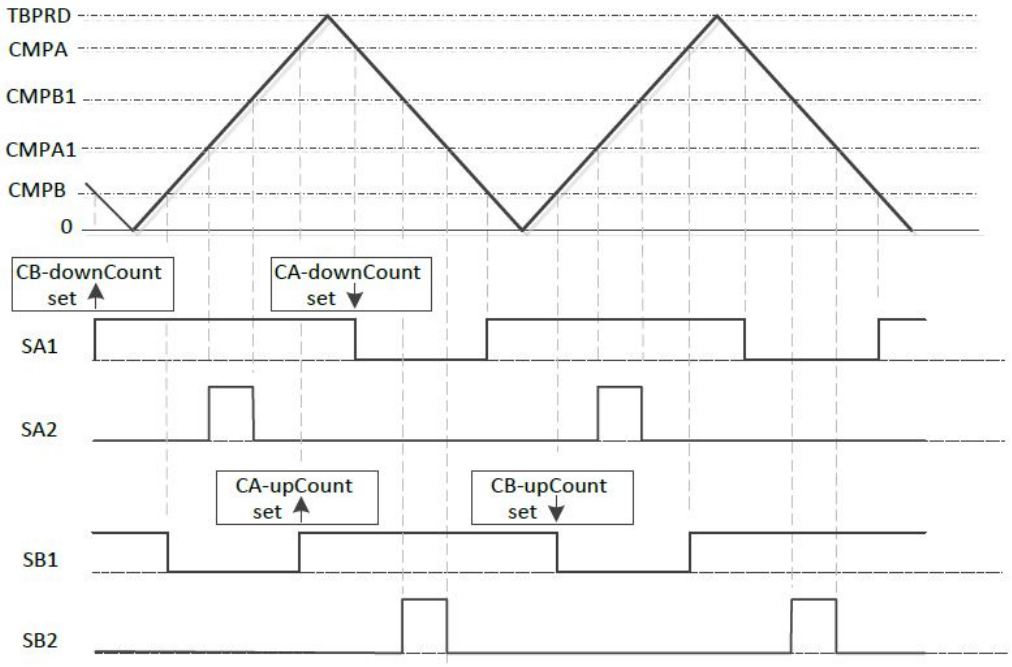

Figure 4.1.: Four steps pulses generation pattern.

Four compared values (CMPA-1, CMPB-1) are set every time the interrupt starts where a pair of them determines the duty cycle of each pulse (SA1-2 & SB1-2). The distance of CMPA and CMPB1 to the

period register TBPRD is equal to the distance to the CMPA1 and CMPB to the zero register, in order to produce the same ON time for all the pulse trains which should be more than half a switching period (0.25msec) in order to fully rectify the current at the outputs.

Moreover, the operation of SA and B1 is reversed to the operation of SA and B2 and vice versa, every 10msec i.e. after every twenty switching periods in order to comply to the 50Hz output demands. Two independent but synchronized interrupts are generated for 4QSW-A and 4QSW-B, in order to have full control of the ON times separately. Care must be taken in order never two conductive switches are open per leg, to avoid the circulating currents.

It was selected that the microcontroller 4 steps code would be responsible for the zero crossing detection of the load current, in order to safely operate the ac FB. However, more challenges of synchronization arise during the debugging process which defined the usage of a current transducer and an external interrupt of the dsp, a more reliable choice.

4.2. Pulses generation pseudocode

A pseudocode has been written, prior to the verification of the C script, which forms and facilitates in general the software procedure of the microcontroller. It is presented below.

// Microcontroller pseudocode
Include the needed libraries

//Prototype statements for functions
Declare main functions
Declare interrupts and compare values
Set variables
Set sin wave (one is enough)
Set switching frequency

//Begin with the Main Loop
Initialize interrupts
Synchronize the epwm clocks
Wait for the interrupts to begin //one interrupt for the mPWM and one for the 4 steps
==for a specific interrupt==
Set the output pins
Phase shift the signal
Set the counter mode to up-down
Set the Action Qualifier
===leave interrupt===
Set when the interrupt occur // at zero or at TBPRD

//mPWM interrupt
Set an angle for the sin wave based on the 50 and 4Khz frequency.
Limit the angle up to 2π.
Give the Compare absolute sin value based on the angle
Synchronize the three phases with the zero crossing of the carrier based on count registers comparison
Increase timers based on the f_sw (4kHz)
Call for the Main

//4Steps interrupt SA1 and SA2
Set the timer to zero if T_sw (2kHz) is reached
if before half period set compare values for SA1

if after, set the compare values for SA2
Synchronize with mPWM pulses
Update counter
Call for Main

//4Steps interrupt SB1 and SB2
Set the timer to zero if T_sw (2kHz) is reached
if before half period set compare values SB1
if after, set the compare values SB2
Synchronize with mPWM pulses
Update counter
Call for Main

4.3. Verification of the code

Experiments where conducted in order to test the functionality of the C code, which is presented in Ap. **??**. Results are concentrated in the generation of the pulses themselves, and at the synchronization issues discussed earlier.

4.3.1. Results for the mPWM

Two tests, a "target frequency test" at 2kHz and a "double frequency test" at 4kHz, are conducted to validate the functionality under variable frequencies applied to the code, in order to assess the interrupts and the conditions set to generate those pulses. Experimental results are summarized in Tab. 4.1.

Test	Switching Frequency	Base Frequency	Number of pulses
Target Frequency Test	2kHz	50Hz	20
Double Frequency Test	4kHz		40

Table 4.1.: Experimental results to validate mPWM for 10msec.

Fig. 4.2, illustrates the experimental results of the tests, verifying the pulse trains for the mPWM are frequency dependant. The time distance for both tests is the same i.e half base period.

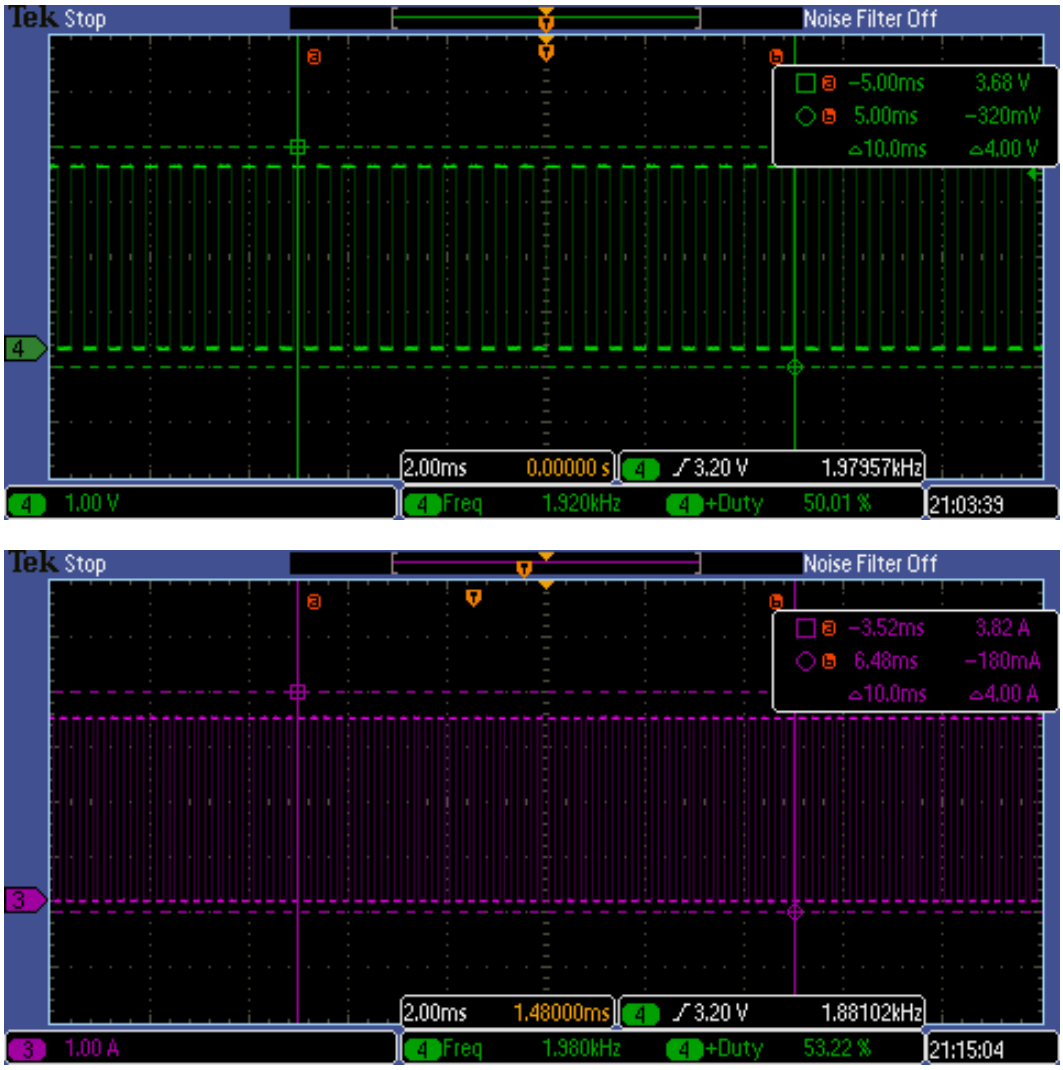

Figure 4.2.: Generation of mPWM pulses for the 2kHz (left) and 4kHz (right) under the same fundamental frequency.

4.3.2. Results for the 4 Steps

Similarly for the 4 steps pulses, it is important to verify that they can change duty cycle for every half base frequency. Due to no external interrupt is implemented, this has to achieved by the microcontroller code. For this scope, two different test are conducted, similarly to the mPWM, for two different load frequencies. The subsequent Tab. 4.2. illustrates their results.

Test	Switching Frequency	Base Frequency	UpCount #pulses	DownCount #pulses
Target Frequency Test	2kHz	50Hz	20	20
Double Frequency Test	4kHz		40	40

Table 4.2.: Experimental results to validate mPWM.

Fig. 4.3, shows the operation of a 4QSW (e.g. green signal is SA1 and magenta is SA2) indicating the frequency dependance and also the complementary operation of the transistors.

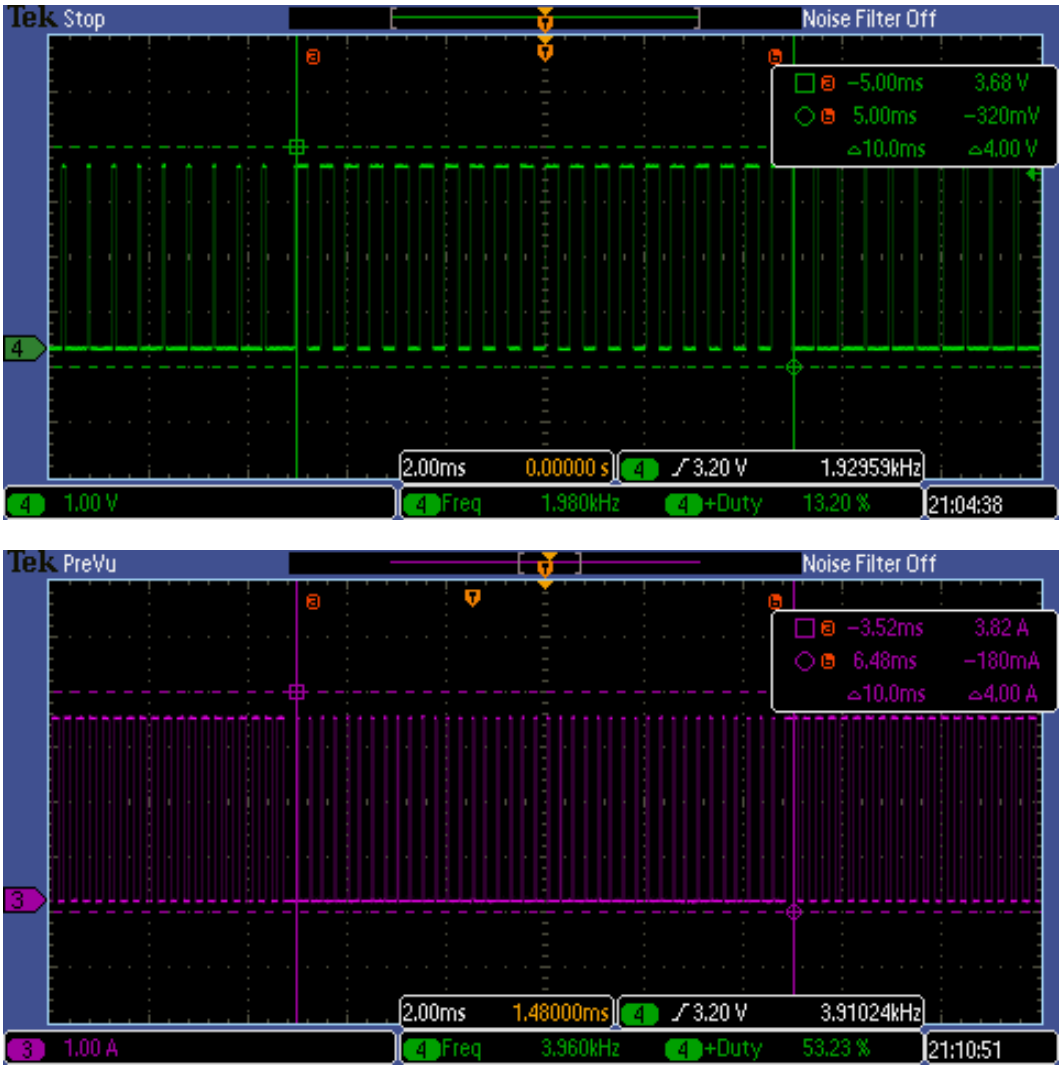

Figure 4.3.: Experimental results of the number of pulses for 2kHz(left) and 4kHz(right) under the same base frequency.

Lastly, the overlap of the pulses has to be validated. A test case of overlapping for 8μsec is shown in the following Fig. 4.4.

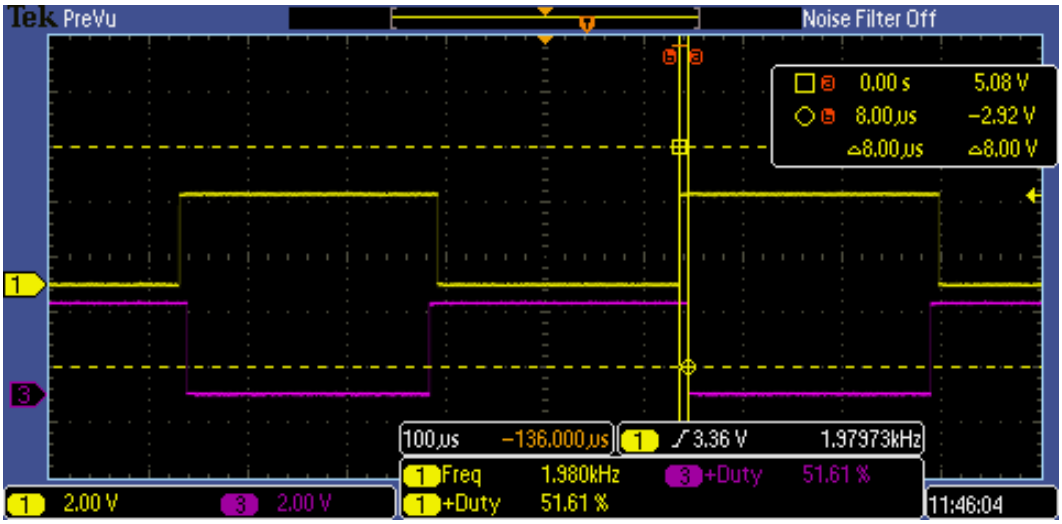

Figure 4.4.: Overlap of the pulses for 2 blanking times.

After validating the correct conditions, the commutation times has to be validated. Fig. 4.5, shows the 4 step procedure of the switches.

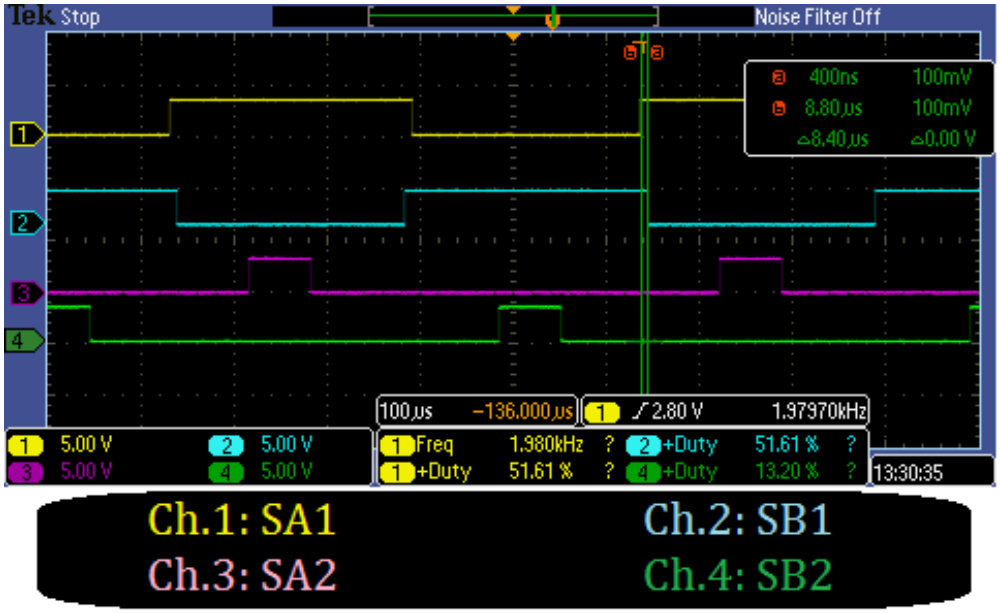

Figure 4.5.: 4 Step procedure of implemented with the microcontroller.

With the yellow anf blue are the switches SA1 and SB1 generating the active steps, whereas the magenta and green signals are the SA2 and SB2 respectively, representing the passive steps.

- During the first step SA1 (yellow signal) is switched on for the proper time period and switch SA2 is turned off to prevent any change of the current direction.
- The second step is to turn on the on-going switch SB2 (blue signal) before the off-going SA1 is turned off.
- Third step is to turn off SA1.
- The fourth step includes the firing of SB2 (green) in order to re-establish the four quadrant characteristic.

At zero crossings of the load current, 4QSWs have their four quadrant operation in order the current can naturally flow from positive to negative. This is achieved by turning on SA1 and SA2 (both IGBTs of the 4QSW) simultaneously for a short period of time. Next Fig. 4.6, illustrates this concept, by showing the gate pulses of SA1 (blue) and SB1 (magenta) which they overlap for half base period, in order to rectify the current at the load. Then the IGBTs SA2 and SB2 ought to operate in order to change the load current sign. With green cursors is specified the time instant where the switch that conducts before the zero crossing (e.g. SA1-blue) is not turned off until the SA2 (green) is on, and for a short time more to ensure the current path (yellow). The same procedure occur for the SB1 and SB2 during the next zero crossing of the load current. Under no circumstances, the green (SA2) and the magenta (SB1) should overlap.

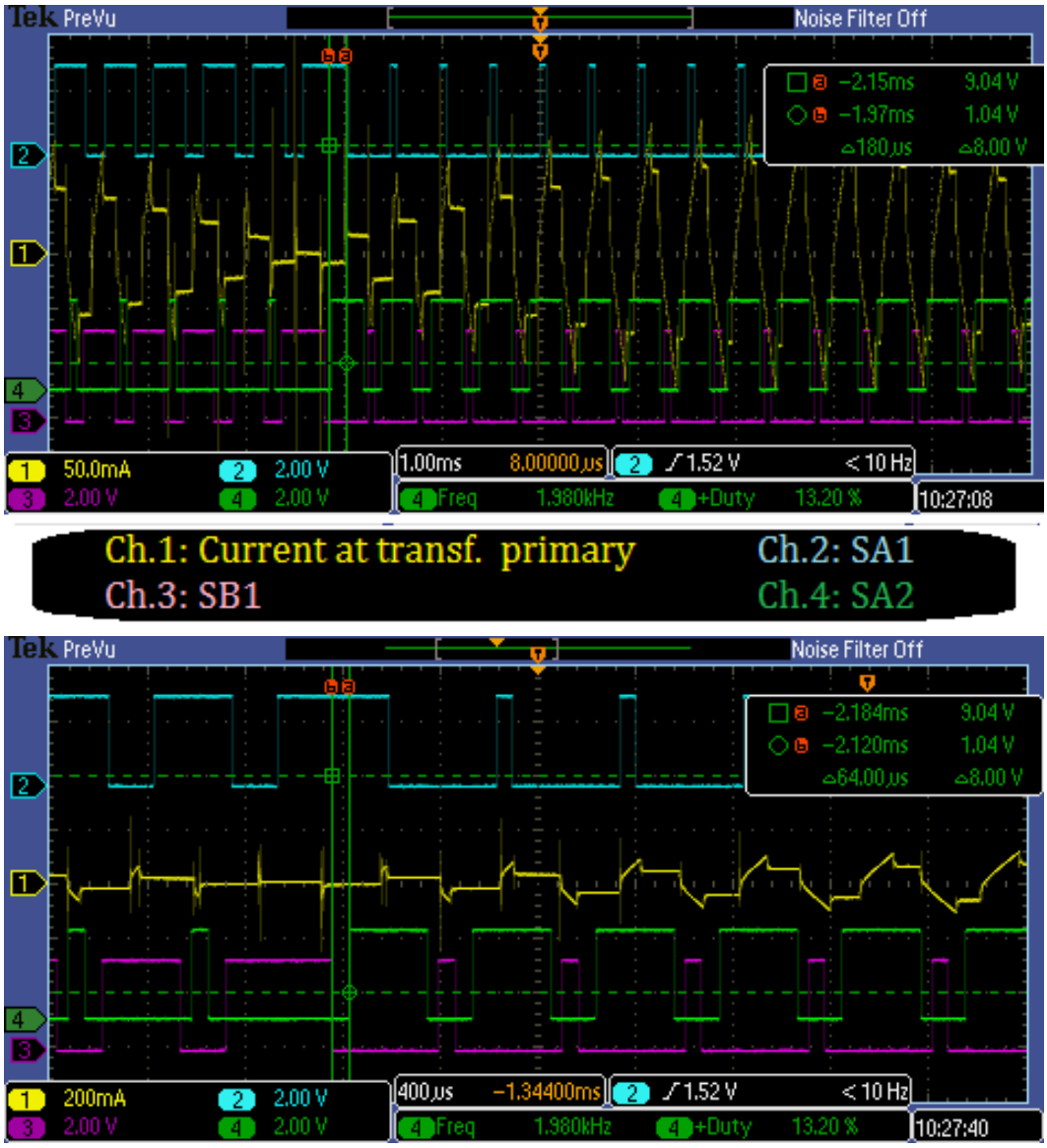

Figure 4.6.: Four quadrant operation of the switches during zero crossings of the load current, i.e. every 10msec. The right picture focus on the zero crossing instant.

4.4. Discussions

The major consideration for implementing the two modulation schemes is concentrated at their synchronization. Fig. 4.7, shows two cases for synchronized and asynchronized pulses indicated inside the yellow cursors area. The reason why the synchronization is important, is to efficiently change the output current direction by changing the operation of the pair pulses SA1-B1 to SA2-B2. By comparing the current and the 4 step pulses, practically a comparison is made between the mPWM and the 4 step.

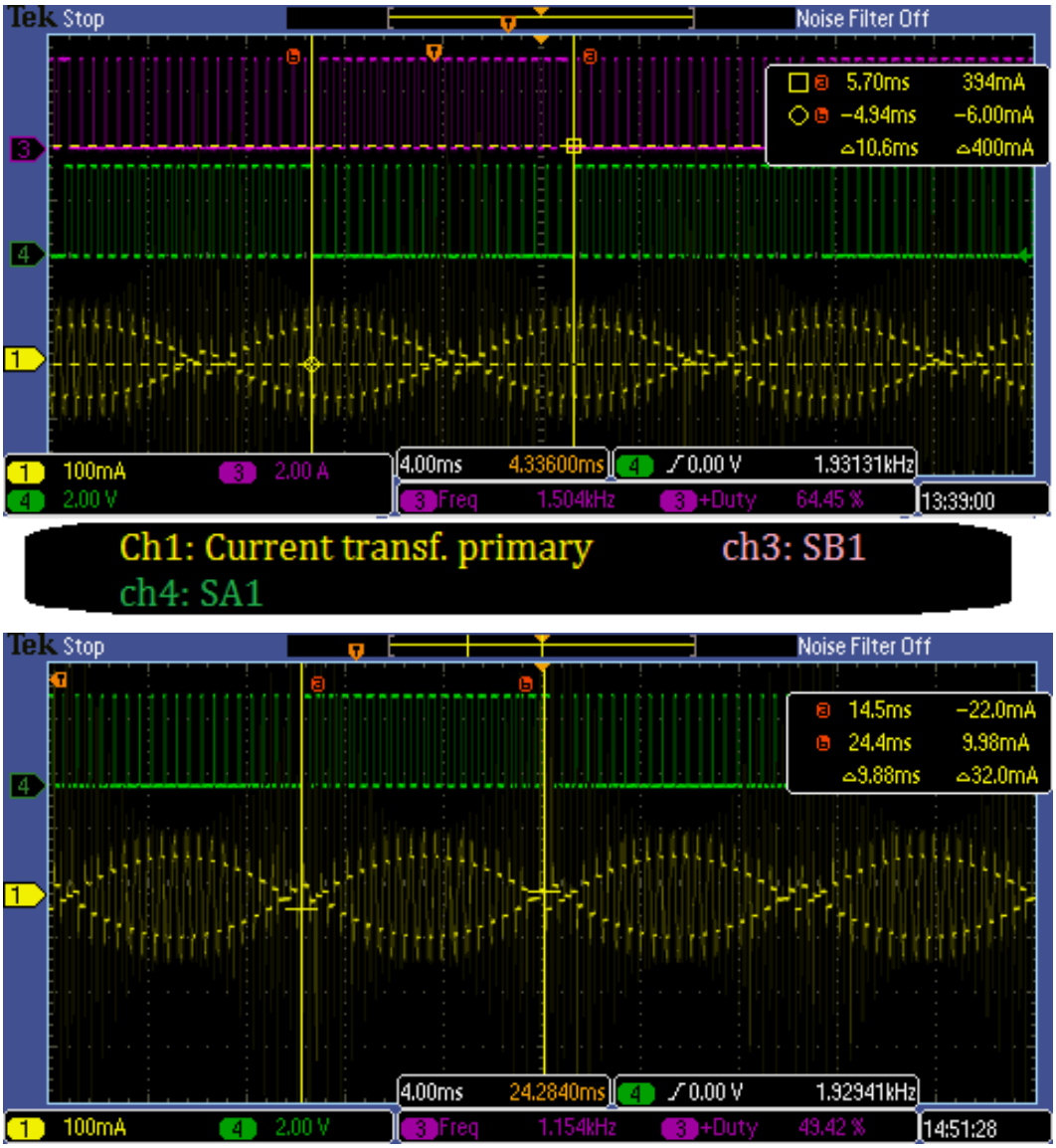

Figure 4.7.: Asynchronized (left) and synchronized (right) pulses of the 4Steps with the current load, based on the fundamental frequency.

This effect can be minimized by the proper commutation of the switches which is feasible by accurately formulating all the conditions for implement the modulation schemes.

Furthermore, synchronization issues might occur at the switching frequency, either the synchronization at the fundamental exist or not. Fig. 4.8, highlights this concept with the magenta cursors area.

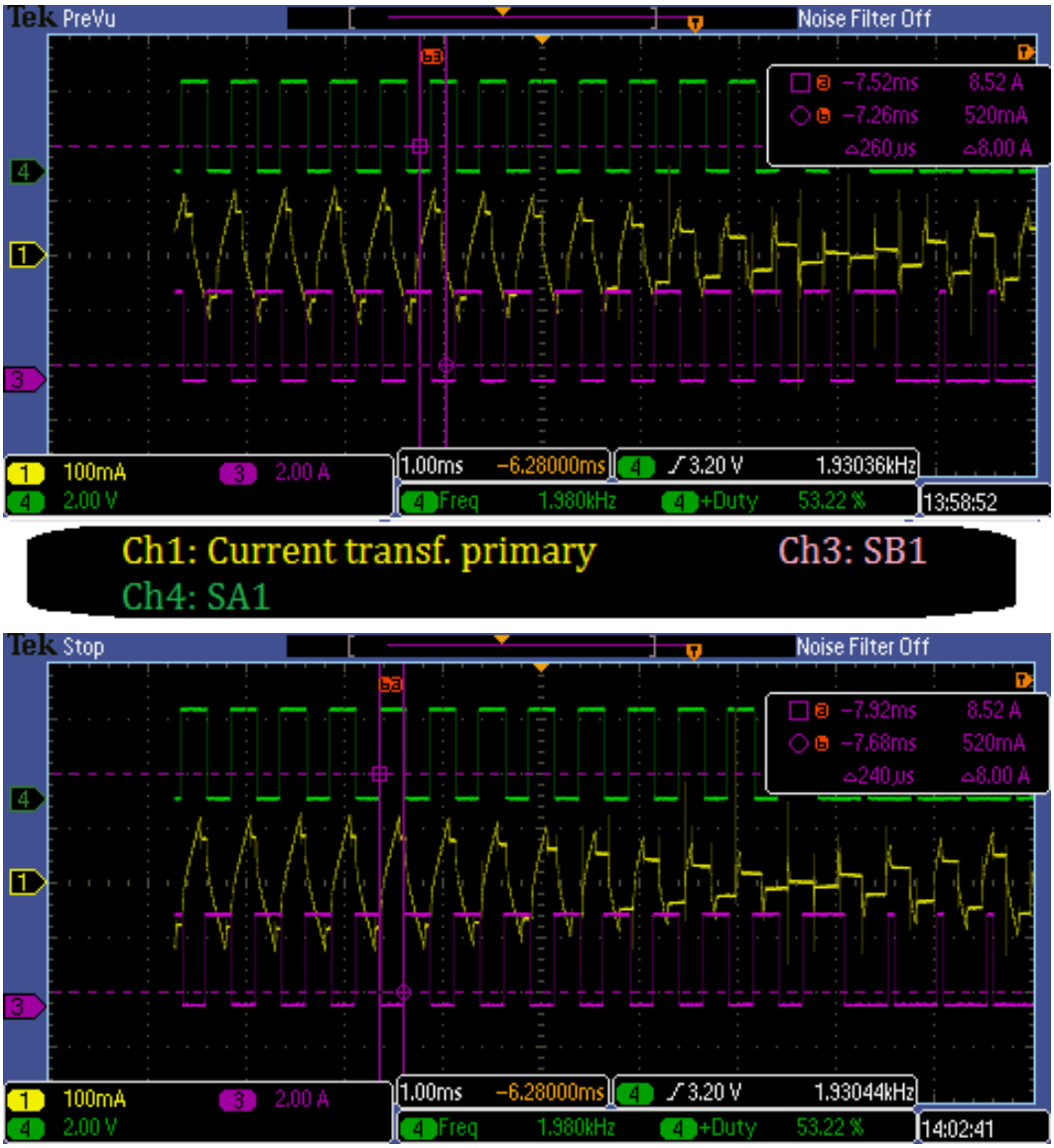

Figure 4.8.: Asynchronization (left) and synchronization (right) of the pulses based on the switching frequency.

Green and magenta signals are the gate pulses of the bidirectional switches, SA1 and SB1 respectively. The yellow signal is the current at the transformer primary while it is connected to a 400ohm resistance.

The scope is the pulses to always turn on the IGBTs of the ac FB before the current reverse its sign and remain on until the current change polarity. Hence, the ON time of the switches must be selected as:

$$t_{ON} = (t_{on,IGBT} + \frac{T_{sw}}{2} + t_{off,IGBT} + t_s) \tag{4.1}$$

where t_s is a margin introduced to the total ON time. According to the characteristics of the selected transistors $t_{ON} = 0.3\,msec$.

The consequences of asynchronized pulses potentially will influence only the shape of the current at the load, or in worst cases a current path from the VSI to the ac FB will be blocked, where snubber has to operate in order to establish the continuity of the load current and cope with the overvoltages.

Another consideration concerning the synchronization of the VSI pulses, is related to the phase shift of the count registers of the mPWM. As mentioned previously, regardless the initial phase shift of

the reference signals, an equivalent shift must also be implemented. The main impact of this shift is significant on the current behavior.

The subsequent Fig. 4.9, illustrates the current at the primary of the transformer when open circuited, without the phase shift on the counters. Simulated results are also illustrated for comparative reasons.

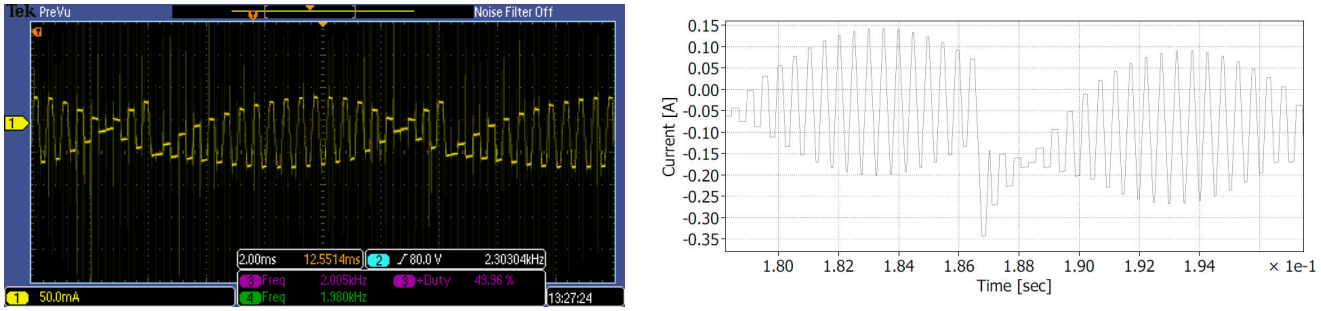

Figure 4.9.: Current behavior without shifting the counters of the three phases. Experimental (left) and simulated (right) results.

This current drop is a direct concequence of the...

By setting the counting registers according to the reference signals the current behavior.... Fig. 4.10, shows the current obtained at the primary of the transformer.

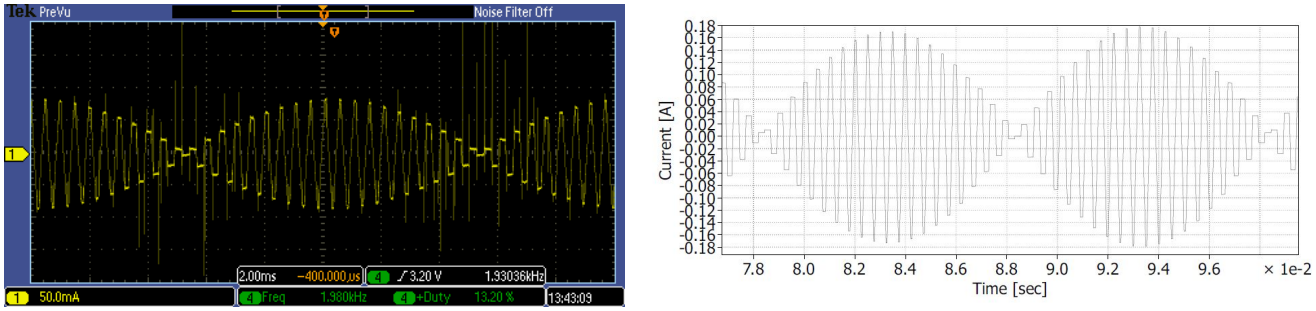

Figure 4.10.: Current behavior when phase shifting the count registers of the three phases. Experimental (left) and simulated (right) results.

In next Fig. 4.11, a more detailed image of the current generated is shown (left), where the operation at the 2kHz with a modulation envelope signal at 50Hz can be noticed. The same current is measured for a light resistive load of 105ohms and voltage 230V, and it is presented in the right figure.

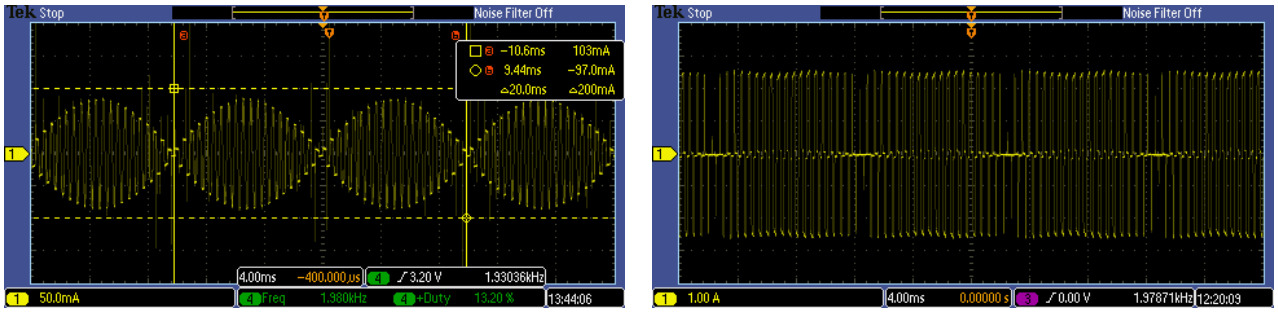

Figure 4.11.: Current shape and frequency at the transformer primary while opened circuited (left) and loaded (right).

The behavior of the current at the primary while open circuiting the secondary of the transformer is determined by the integration of the square voltage as it can be considered as an pure inductive load.

However, when connected to a resistive load, the relation is changed and follows an RL circuit behavior, as shown in the right figure. The correlation between the magnitude of the current and the resistance is reverse proportional whereas the rate of rise to that magnitude depends on the time constant which is reverse proportional to the inductance.

5
HARDWARE DESIGN

This chapter analyzes the design procedure of the converter by specifying the all the hardware acquired. A VLT drive represents the operation of a 2-Level VSI, accompanied with an interface card to modulate its operation. Then, the selection of the transistors for the implementation of the bidirectional FB is discussed, along with the driver circuit. The latter is composed of the buffer interfaces to enhance current levels, fiber optic isolation connection and the half bridge driver for generating the gate pulses to the switches. Experimental results for validating the functionality of the design are also included at the end of this chapter.

5.1. Danfoss VLT Automation Drive FC302

The conventional 2-Level inverter can be implemented by operating the VLT Drive from the dc link input to the three phase output. This powerful frequency converter is used for grid connected motor drive applications, rendering the minimum dc voltage for inverter operation to be 200V. The main characteristics of the frequency converter are shown in Tab. 5.1.

Parameter	Value
Drive	FC302
Rated Power	2.2 kW
Supply ac Voltage	380-500 V ±10%
Frequency	50/60 Hz

Table 5.1.: VLT Drive main characteristics.

The Drive operation is to supply the single phase transformers.

5.1.1. Interface and Protection Card IPC3

The IPC3 replaces the original interface card of the FC302 in order to provide external control to the inverter switches. An optical card is required in order to connect the microcontroller to the IPC3. In the following Fig. 5.1, the block diagram for this purpose is illustrated.

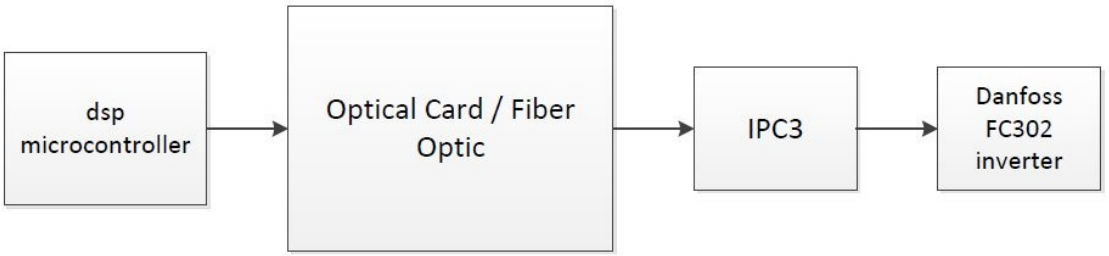

Figure 5.1.: Block Diagram for the control of the FC302 Inverter.

IPC3 besides the control of the VLT, offers protection against short-circuit and overcurrents at the outputs (21A), dc link overvoltages (870V dc), over frequency (for gate signals above 13.5kHz) and over temperature, which are all indicated with status signal LEDs. Also, only the upper IGBTs of the VLT has to be supplied, since it provides dead time selection (2∼4usec) and generation for the bottom leg transistors, minimizing the need of optical fiber interfaces to half. An enable signal is needed in order to permit the gate pulses to feed the IGBTs, which can be implemented either manually or softwarely. During start-up the VLT goes into trip mode and cannot be reset for a few seconds. During a failure the gate pulses are disabled from the VLT, by putting the reset signal high and the enable low.

5.2. Transistors Selection

Four different IGBT which comply to the converters power ratings are compared with their main characteristics being illustrated in the subsequent Tab. 5.2. Regarding the maximum on state current, the switches must withstand a peak current of around 10A. Because of the overcurrents and overvoltages that might occur due to modulation methods, a safety margin of 25A and 1200V is chosen.

Manufacturer	*STMicroelectronics*	*INFINEON*	*INFINEON*	*FAIRCHILD*
Part Number	STGWA25M120DF3	IKW25T120	IKW25N120H3	HGTG11N120CND
Breakdown Voltage V_{CE} [V]	1200	1200	1200	1200
Continuous Current I_C [A]	$25_{at\,100^oC}$	$25_{at\,100^oC}$	$25_{at\,100^oC}$	$22_{at\,110^oC}$
Input Capacitance C_{ies} [nF]	1.55	1.86	1.43	2.2
Switching Characteristics, Inductive Load at T_{vj} =175^{o}C				
Turn-on Delay Time $t_{d(on)}$ [ns]	28	50	26	$24_{at\,25^oC}$
Turn-off Delay Time $t_{d(off)}$ [ns]	155	660	347	$280_{at\,25^oC}$
Current Rise Time t_r [ns]	17	32	35	$16_{at\,25^oC}$
Current Fall Time t_f [ns]	240	130	50	$400_{at\,25^oC}$
Price [euro/each]	8.2	7	4.82	3.17

Table 5.2.: Comparison of several discrete IGBTs.

All the devices have embedded diodes for the bidirectional operation, but they mainly differ on their switching characteristics and price. It is considered that IKW25N120H3 satisfies foremost the converter's power rating and switching requirements and it is selected for the proposed topology.

5.3. Fiber Optic Connection

Over the wide range of galvanic isolation devices, fiber optic links are selected mainly since they offer very high noise immunity in comparison to others equipment such as optocouplers or transformers. The selected devices are the AVAGO SFH756V transmitter and the AVAGO SFH551V receiver, which feature a convenient and cost effective fiber coupling mechanism. Fig. 5.2, illustrates the packaging and the schematic circuit of those.

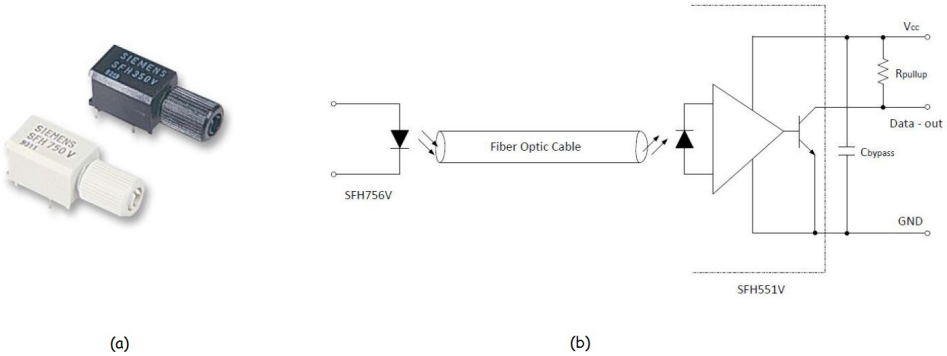

Figure 5.2.: Fiber optics packaging (a) and schematic circuit (b).

Fiber optic cable is a standard 2.2 mm, and is inserted into the plastic housing of the transmitter/receiver.

However, in order to successfully drive the fiber optic devices, and in the same time compromise with the drivers specifications concerning their input current and voltage, the following criteria must be satisfied.

- Transmitter SFH756V forward current and voltage must not exceed the 50mA and 2.8V respectively, for safe operation.
- Receiver SFH551V ought to be supplied with at least 4V and maximum 15V. Considering that this voltage signal will determine the output of the receiver, and hence the input to the driver, it must not exceed 5V in order to compromise with the latter's maximum input characteristics. So, the selected is between $4.1 \leq V_{cc} \leq 4.9\ V$.
- Receiver has an inverted input to output logic.

According the above and taking into account the maximum current supply capability from the microcontroller to be 2mA, is obvious that is not sufficient to drive the fiber optics, and so a buffer circuit in between them is needed. As for the signal inversion, it is compensated by software implementation, directly from the microcontroller's code.

5.4. Buffer Circuit Interface

An optical interface ought to be placed between the microcontroller and the drive circuit in order to provide galvanic isolation between the two circuits. Hence, in order to enhance the current levels and

drive the optic equipment, a buffer circuit is added between the output signals of the microcontroller and the input to the SFH756V optical transmitter.

It is chosen to work with NXP 74LVC541A non inverting buffer and its function diagram is shown in the following Fig. 5.3.

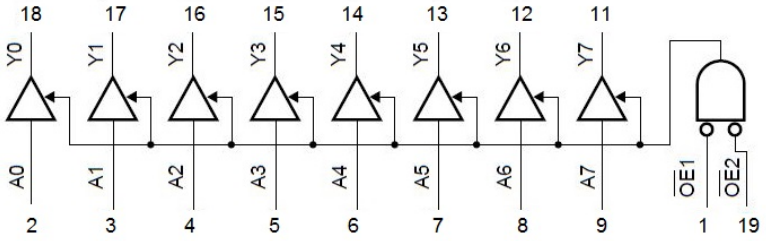

Figure 5.3.: NXP 74LVC541A Buffer, Function diagram.

This device offers a wide range of supply voltage, capable of being directly connected to the 3.3V supply pins of the microcontroller. Also, the range of the input voltage is up to 5.5V making it proper for the connection of the 3.3V dsp signals. Furthermore, it is able to buffer the current at its output terminals up to maximum 50mA. However, consulting the SFH756V datasheet, the maximum input forward voltage should be less than 2.8V and the absolute maximum forward current should not exceed 50mA. A safety margin is then acquired, setting $I_{max} = 40mA$ and $V_F = 2.1V$. For this reason, a current limiting resistance is introduced, determined by the following formula,

$$R = \frac{Vcc - V_F}{I_{max}} \implies R = 30\,ohm \tag{5.1}$$

It is selected to connect the anode with the TT ELECTRONICS SSN16A22R0JSLF thin film resistor network and the cathode with a 10ohm resistance, to ground. This network is composed of several isolated resistors of 22omhs and its schematic is illustrated in Fig. 5.4.

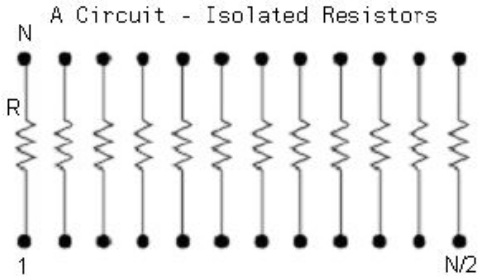

Figure 5.4.: SSN16A22R0JSLF schematic.

In this manner the current is limited at 37.5mA and the voltage at 2.1V, rendering the operation of the fiber optics feasible.

5.5. Half-bridge IGBT Driver

The selected driver for the bidirectional switches is the Semikron SKHI 22B. It features a double drive for half bridge configurations compatible to operate at high voltage levels up to 1200V. Also, it provides isolation between the input and the output side up to 2.5kV and up to 1.5kV from the upper to the lower output circuits. The main feature of the driver for this work is the short circuit protection.

Saturation voltage from the IGBT datasheet, is the on state voltage drop across the collector emitter terminal. For the selected transistor, it is typically ranges from 2.05 to 2.7V, considering the variations on the collector current and on the junction temperatures. The drivers however, offers a short circuit protection by controlling this collector-emitter saturation voltage ($V_{CE,sat}$) to a reference value. According to the transistor datasheet for $V_{GE} = 15V$ and for 175^oC should be around 3V, however, a small margin is given due to its influence on the temperature and current levels, and the selected selected $V_{CE,sat}$ is 4V. In order to implement the short circuit protection, an additional circuit has to be added to the driver circuit comprising of an resistor R_{CE} and a capacitor C_{CE} in parallel at the CCE pin. Those values can be calculated as:

$$V_{CE,sat}(V) = \frac{10\,R_{CE}(Kohm)}{10 + R_{CE}(Kohm)} - 1.4 \tag{5.2}$$

$$t_{min} = \tau_{CE}\, ln \frac{15 - V_{CE,sat}(V)}{10 - V_{CE,sat}(V)} \tag{5.3}$$

$$\tau_{CE}(\mu sec) = C_{CE}(nF)\, \frac{10\,R_{CE}(Kohm)}{10 + R_{CE}(Kohm)} \tag{5.4}$$

where:
$\cdot V_{CE,sat} = 4V$ is the reference saturation collector-emitter voltage
$\cdot t_{min} = 1.5\mu sec$ is the time delay before the saturation control begins
$\cdot R_{CE} = 12k\Omega$ which adjust the saturation voltage to the reference value
$\cdot C_{CE} = 0.45nF$ which influences the delay time from the turn on of the IGBT to the activation of the saturation control

In case of a short circuit, the current rise leads to an increase of the $V_{CE,sat}$ over the reference value, and an error signal is transmitted from the V_{CE} pin to the error memory while the gate pulses are locked, switching the IGBT off. Error memory is reset if simultaneously no error is pending and gate signals are set low for more than 9usec.

5.6. Snubber circuit

The snubber circuit is included in order to protect against faulty commutation of the switches at the bidirectional bridge, safely transfer the stored energy from the transformer leakage to the clamp capacitor and provide a load current path in case of blanking time. Thereupon, it is connected to the input and output of the bidirectional FB through two fast reverse recovery diode rectifiers as shown in Fig. 1.1. Transferring the leakage inductance to the clamp capacitors derives the design specification:

$$W_{L_\sigma} = W_{C_{clamp}} \Longrightarrow \frac{1}{2}\, L_\sigma\, I^2 = \frac{1}{2}\, C_{clamp}\, \Delta V^2 \Longrightarrow C_{clamp} = \frac{L_\sigma\, I^2}{\Delta V^2} \tag{5.5}$$

where $\Delta V^2 = (V_{max} - V_{in})^2$ is the maximum voltage variation across the capacitor, defined by the the maximum allowable overvoltage and the peak phase voltage.

5.7. Verification

The powerful Danfos VLT Drive is operated as a 2 Level inverter by supplying its dc link with voltages of more than 150V. The interface card IPC3 offers a sequence of protection schemes and moreover the possibility of directly modulating the Drive. The maximum power ratings of the VLT are 2.2kW hence the design of the bidirectional bridge implemented accordingly. IGBTs for 1200V and 25A are selected,

where a safety margin is also considered due to the overvoltages and overcurrents that the modulation of the ac FB can generate. The focus is laid on the driver circuit for which the main considerations are summarized as:

- A buffer circuit has to be installed between the microcontroller and the fiber optic transmitter in order to enhance the current levels and establish the operation of the latter ones.
- A 30ohm resistor must be connected at the buffer output in order to comply with certain current limits.
- Fiber optic receiver supply voltage should not exceed the absolute maximum input voltage of the driver.
- Software inversion of the pulses has to be introduced in order to compensate the inversion of the optical receiver.
- Saturation voltage control has to be implemented in order to protect the transistors from the destructive overcurrents.

Fig. 5.5, shows the pulses generated from the microcontroller (blue) to the gate pulse of the driver (green) through the buffer interface (magenta) and the optic fiber connection (yellow).

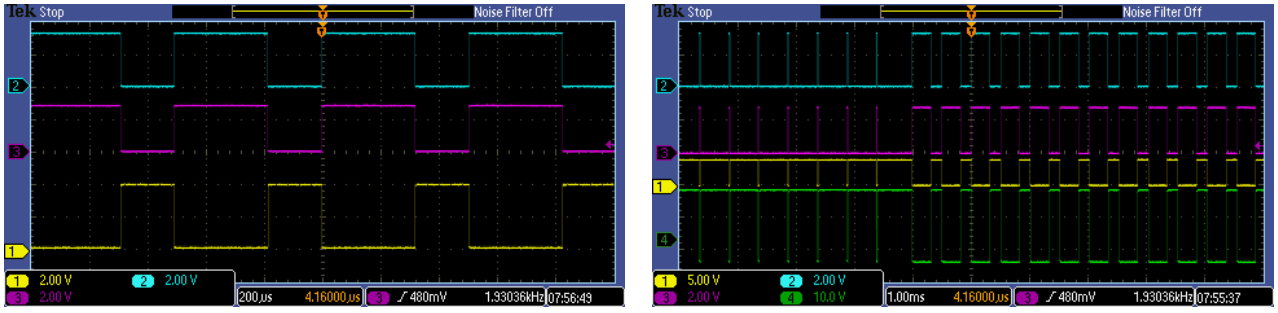

Figure 5.5.: Left image signifies the pulses inversion at the optical receiver (yellow) output. The gate pulses at the IGBTs (green) are illustrated in the right image.

It can be noted that the inversion of the pulses significantly influence the signals sent to the IGBTs. Hence, in order to establish the correct commutation times, the 4 Steps intervals are determined based on that inversion and by following the procedure described in chapter 4.

Fig. 5.6, shows the driving signals to the transistors after compensating the inversion of the fiber optic.

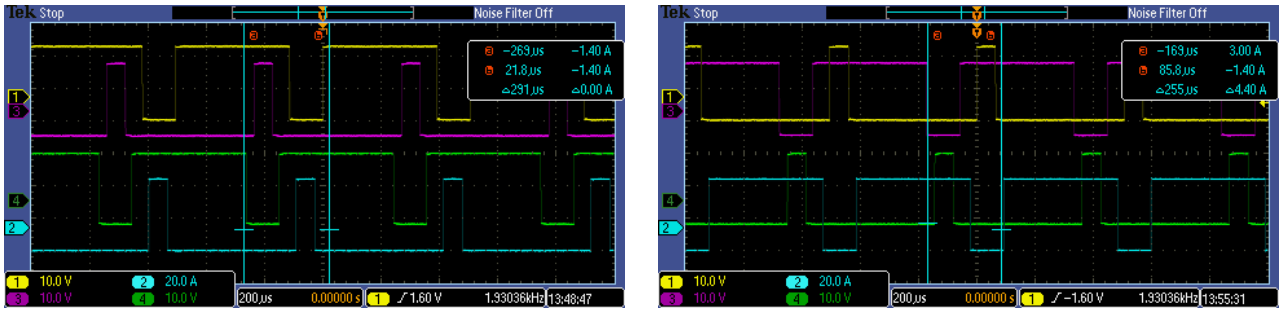

Figure 5.6.: Generated pulses at the driver output. SA1=yellow, SA2=magenta, SB1=green, SB2=blue.

Part IV.

Simulation and Experimental Results

6
RESULTS

During this chapter simulation and experimental tests are presented in order to analyze the operation of the single phase converter cell. An overurrent at the start up procedure sets the VLT..

6.1. Experiments with the proposed converter

After analyzing the the converter behavior with simulation models, laboratory experiments with the designed converter are conducted. Since the operation of the VSI is discussed in previous chapters along with the functionality of the transformers, this section focus on results obtained at the bidirectional FB and at the output load.

6.1.1. Start up procedure

Considering the positive current flow from the secondary of the transformer to coincides with the conduction of the first switch (SA1) the set up is connected to a resistive load of 2kOhm with a dc link voltage at the inverter of 80V. However, during the start up procedure a high current at the output of the VLT triggers its overcurrent protection and put it to trip mode. This high current is generated due to the initial high state of the microcontroller pins, which lead to a short circuit between the switches of the ac FB (SA1-SB2). In the following Fig. 6.1, the overcurrent protection is show, activated at 21A. Also the initial high value of the pins can be noticed.

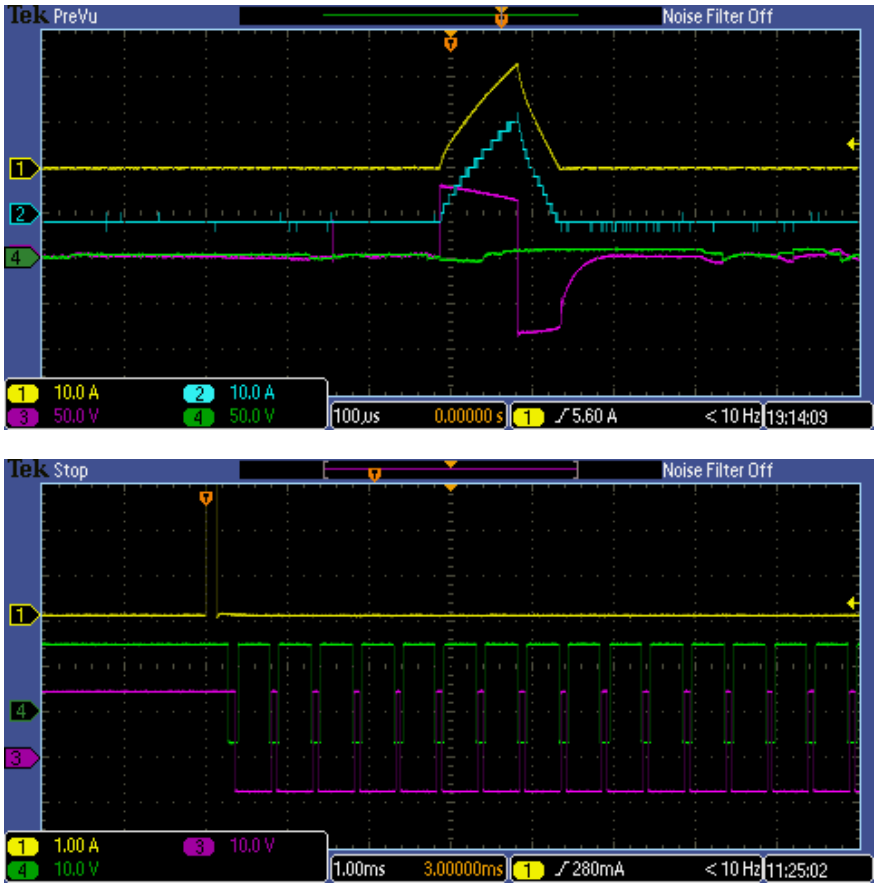

Figure 6.1.: Overcurrent protection of the VLT is activated at 21A (left). Overlapping of switch SA1 with SB2 (right) leads to short circuit of the secondary transformer windings.

Left figure illustrates the short circuit current at the phases R and S of the VLT with yellow and blue signals respectively. Magenta and green are the voltages at the primary and secondary of the transformer. At the right figure, the gate pulses for transistors SA1 and SB2 are shown where during the first cycle, their simultaneous conduction creates a closed branch between the two legs of the ac FB.

A possible solution to cope with this is to change the buffer circuit operation. Since it offers a high impedance - off state output if the enable pins are set high, by programming the microcontroller to set them low after a short period of time the initial gate signals will be low and at the start up procedure and the ac FB will be open circuited, while the current will flow through the snubber. However, this require hardware manipulation of the converter and since this error was reported close to the Master thesis submission date, it has been selected to connect a resistor in series to the secondary of the transformer to limit the current. Nevertheless, the maximum dc link voltage is now limited to the power dissipation ratings of the resistor. Experiments for testing the single phase cell are conducted with a 1kohm series resistor and 80V dc link.

6.1.2. 80V-1500ohm Test

In the following Fig. 6.2, the currents at the transformers primary and secondary are illustrated with the yellow and blue signals respectively. Since the connected load is purely resistive, the current shape at the secondary follows the voltage behavior.

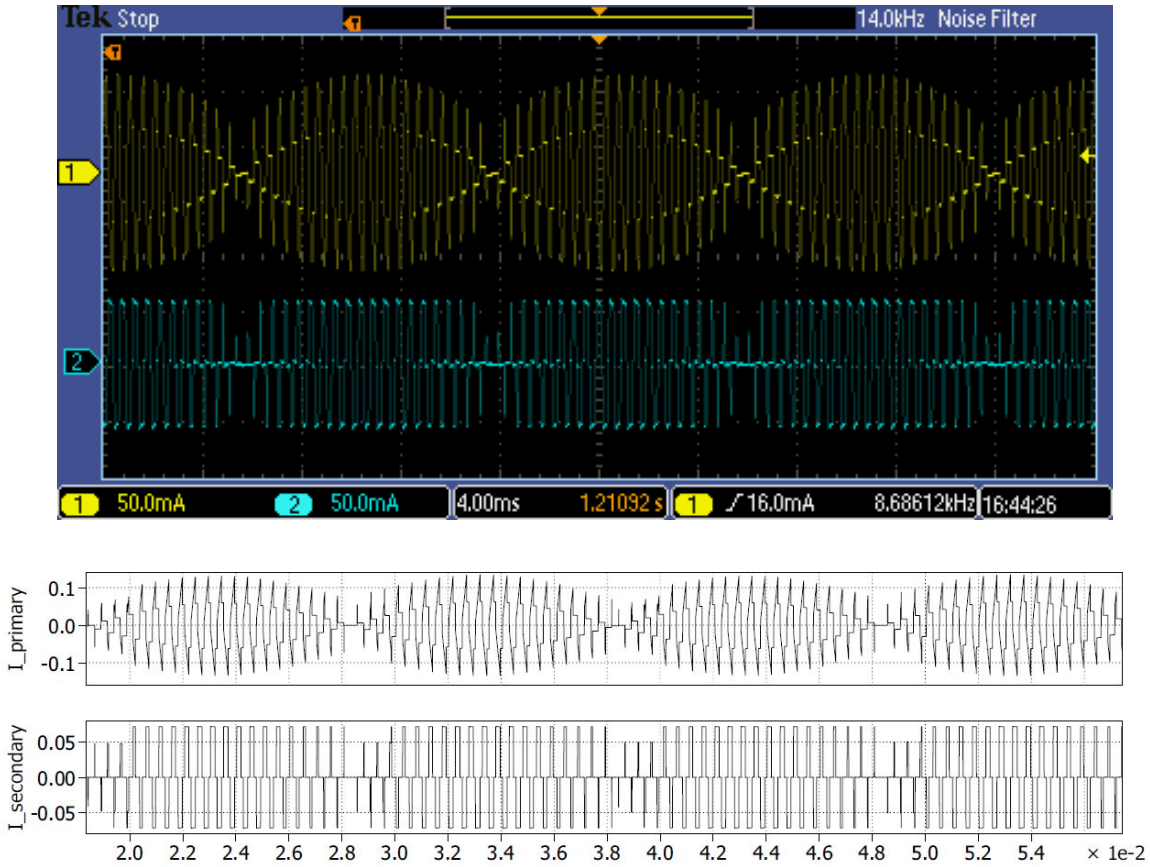

Figure 6.2.: Top figure is the current at the primary of the transformer (yellow) and at the secondary (blue) with a resistive load obtained by experimental measurements while bottom is simulation results.

Subsequently, in the next Fig. 6.3, the same currents are considered with the yellow and green signals respectively, for a shorter period of time. Currents are defined by the operation of the modified PWM. That is, the difference of the phase voltages will determine the voltage induced to the primary of the transformer, and hence the current flow. Net power of the transformer is the same, so the magnitude difference in the currents is compensated by the reverse difference in the voltages. Simulation results validate those statements.

Figure 6.3.: Currents at the primary and secondary of the transformer for a resistive load illustrated for a short period.

The subsequent Fig. 6.4, shows the voltages at the secondary of the transformer (magenta), and at the load (green). The rectification of the latter can be noticed, which changes polarity every half of the load period. This is due to the modulation strategy, where SA1 and SB1 are overlapping and rectifying the signal for the first half (positive output) , while SA2 and SB2 are overlapping for the other half (negative output).

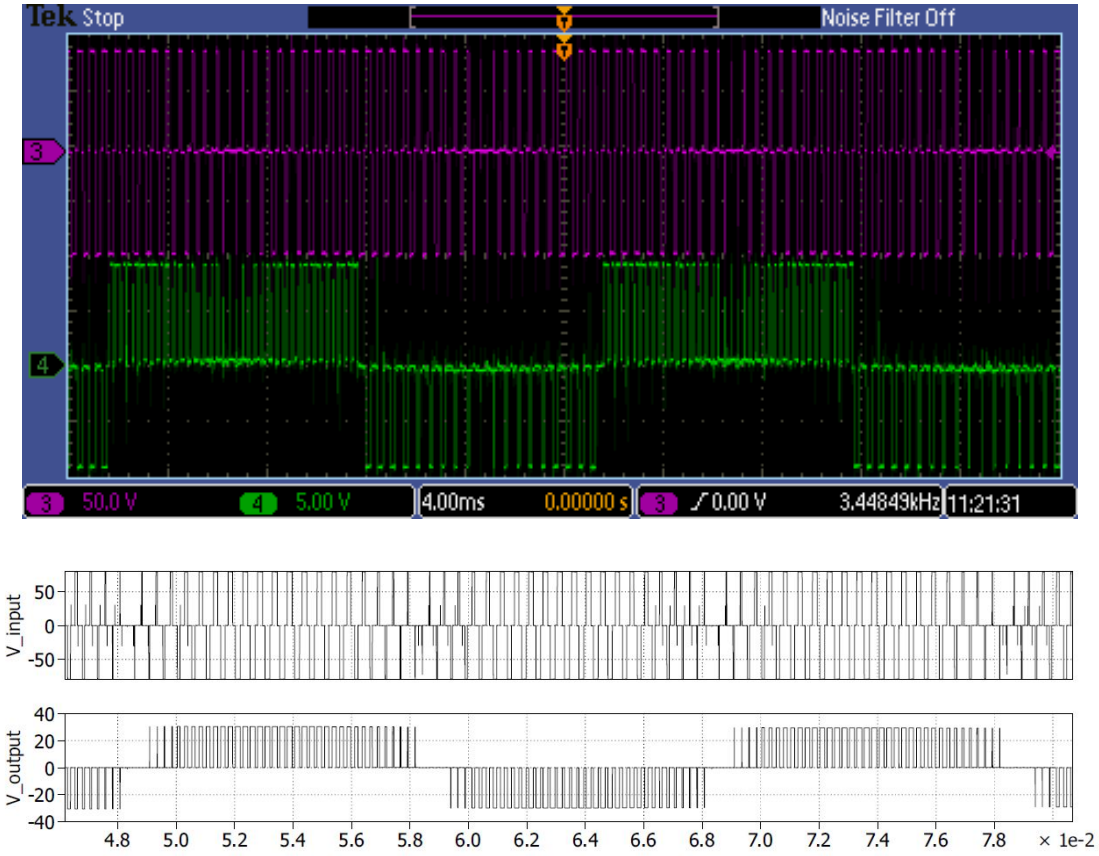

Figure 6.4.: Top figure shows the voltages at the input (magenta) of the bidirectional FB and at the output (green) resistive load. Bottom figure are simulation results.

Also, a phase shift between the two signals is observed which can be explained by lack of synchronization between the two modulation techniques. A more reliable solution dictates a closed loop 4 steps control, to constantly attend the load current polarity. Simulation results signifies this phase shift by comparing the voltage signals at a perfectly synchronized system.

The harmonic distortion of the output signal can be realized in Fig. 6.5.

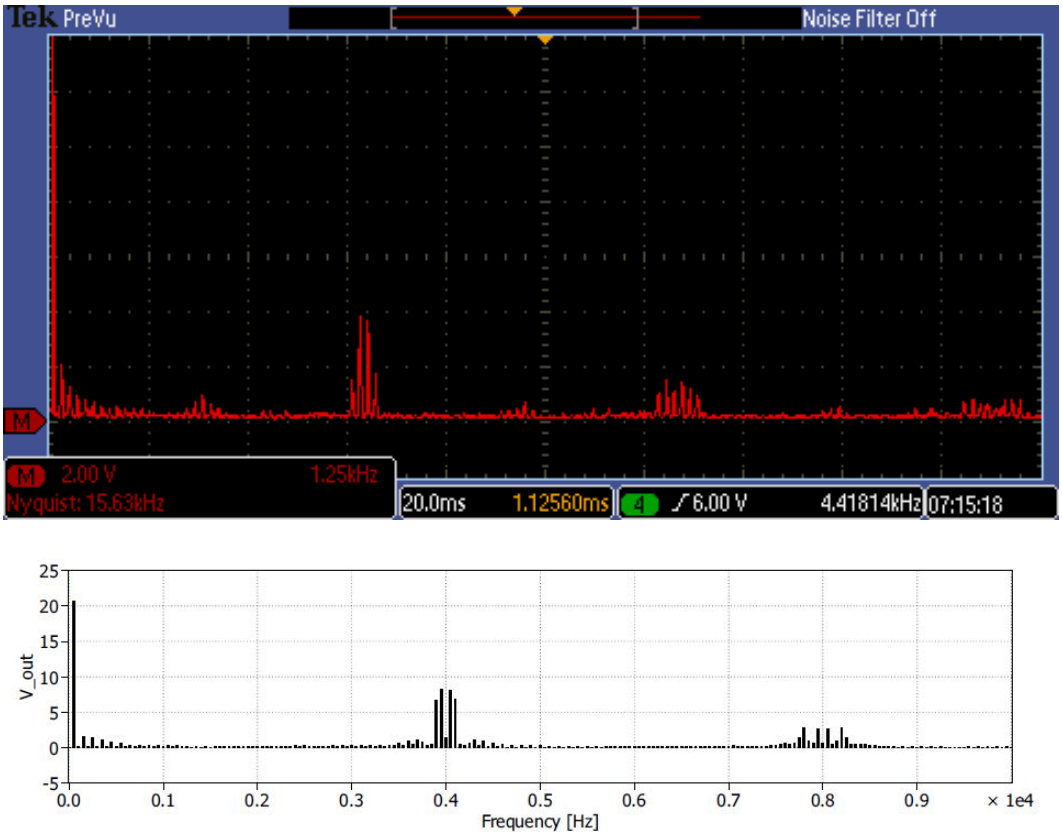

Figure 6.5.: FFT analysis of the output voltage signal.Top is experimental results and bottom simulated.

The doubling of the frequency component can be noticed, as a result of the rectify operation, with the sidebands spread at $\pm 50Hz$, both at simulated and experimental results.

The rectification procedure of transformer high frequency signals, is illustrated in the subsequent Fig. 6.6.

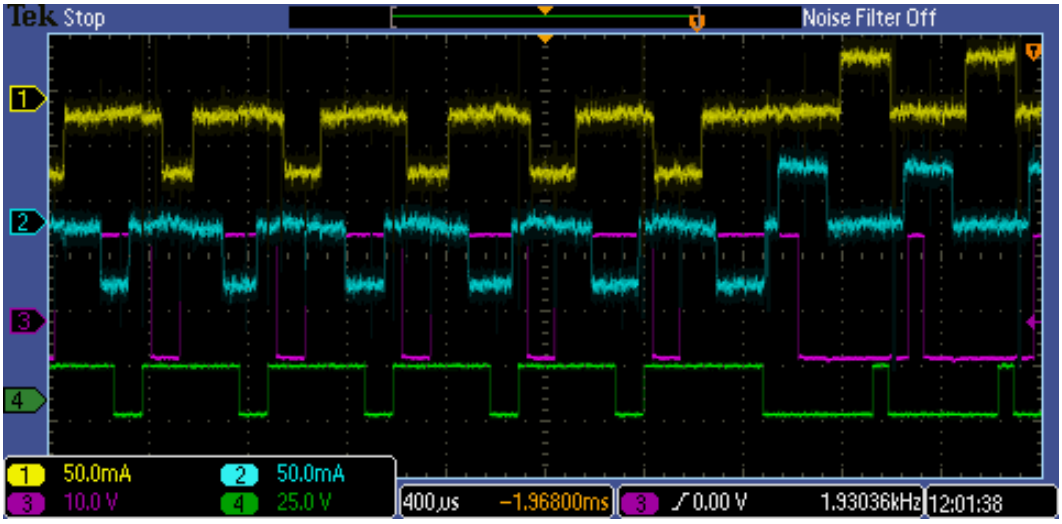

Figure 6.6.: SA1 and SB1 operation for a few switching periods based on the 4 steps modulation.

Currents at both legs of the bidirectional FB are shown with yellow and blue signals. This can be a representation at any time instant, when either SA1 and SB1, or SA2 and SB2 conduct. With green and

magenta are the gate pulses of the IGBTs. The consideration is that when the high frequency current changes polarity the IGBT is already switched on, without allowing circulating currents at the inputs, since the switch at that instant has only its two quadrant characteristics.

6.1.3. Conclusions

In this chapter, results obtained with the single phase cell are estimated and compared to the simulations. However, deeper analysis required as for the synchronization of the inverter with the bidirectional FB for generating the desired signal at the load. Considering the start up procedure short circuit, which is explained by the microcontroller initial high state, the power rating during the experiments is kept low. Although, an estimation on the behavior of the single phase is discussed, further research must be deployed at a higher power operation.

Part V.

Conclusions & Future Work

7 CONCLUSION

In the begging, the problem statement formulation was to investigate whether a serial connection of three phase converters is possible, while introducing the grid side transformer into the converter. For this scope, certain objectives were derived. In this chapter, the conclusions are drawn directly from these objectives.

- *Objective#1*

The first objective was to *Design and optimize a single phase transformer operating at the switching frequency of the converter focusing on the minimization of the leakage inductance.*

In order to achieve the first objective of the thesis, three different designs of the transformers, based on the switching frequency and the absolute maximum power ratings of the inverter are implemented. The topologies main parameter was to reduce the leakage inductance of the circuit as an attempt to reduce the total losses. The models are tested and compered to validate their functionality, however transformer#3 was not considered reliable and it did not acquired in any of the tests.

- *Objective#2 was* to Implement a modified PWM scheme for the operation of conventional 2-Level / 3 phase converter by introducing a high frequency component at the switching frequency at which the transformer operates.

As far as the second objective is concerned, the implementation of the modified PWM was firstly analyzed by means of the duty cycles of the transistors and their harmonic distortion. However, the direct implementation with the microcontroller was not applicable. Hence, an alternative was considered, analyzed and compared to the desired results. It was selected that satisfies the requirements and the procedure continued with this alternative method.

- *Objective#3 was to Implement an optimized modulation scheme for the commutation of the bidirectional full bridge which minimizes the risks of overvoltages and overcurrents.*

Several modulation techniques, categorized to basic and advanced, according to their influence to the converter as far as the current and voltages limits are concerned were presented and compared. It was selected to operate the bidirectional full bridge with the 4 steps commutation as it minimizes the aforementioned considerations.

- *Objective#4 was to Validate the functionality of the modulation techniques of the converter based on simulations in PLECS and compare microcontroller results.*

The modulation patterns had to be validated in order to proceed with the experimental results. Several approaches to obtain the desired high frequency component ware tested and analyzed based on the FFT analysis of the signals.

- *Objective#5 Analyze, design, build and test a single phase cell of the proposed dc-ac isolated modular converter.*

The operation of the designed converter has been estimated with low power rating due to the start up procedure short circuit. A solution to this has been considered by modifying the buffer circuity operation. However, due to the short time until the submission of the thesis, it was selected to operate the converter with a resistor in series as an attempt to estimate its operation. Results analyzed and compared to the simulations to validate the functionality of the converter.

8
FUTURE WORK

This chapter present the future work derived from this thesis. The main considerations are listed below

- Usage of current sensors to constantly measure the load current and acquire a closed loop control to achieve synchronization of the VSI and the bidirectional switches.
- Further reduction of the leakage inductance by using foil coils.
- Analysis and implementation of the three phase model

Part VI.

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Part VII.

Appendix

A
PCB LAYOUTS

In this section, the pcb of the converter are illustrated.

A.1. Buffer Interface

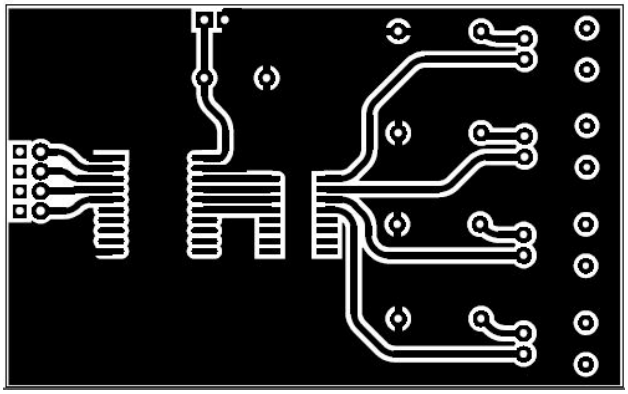

Figure A.1.: Pcb of buffer interface circuit.

A.2. Snubber circuit

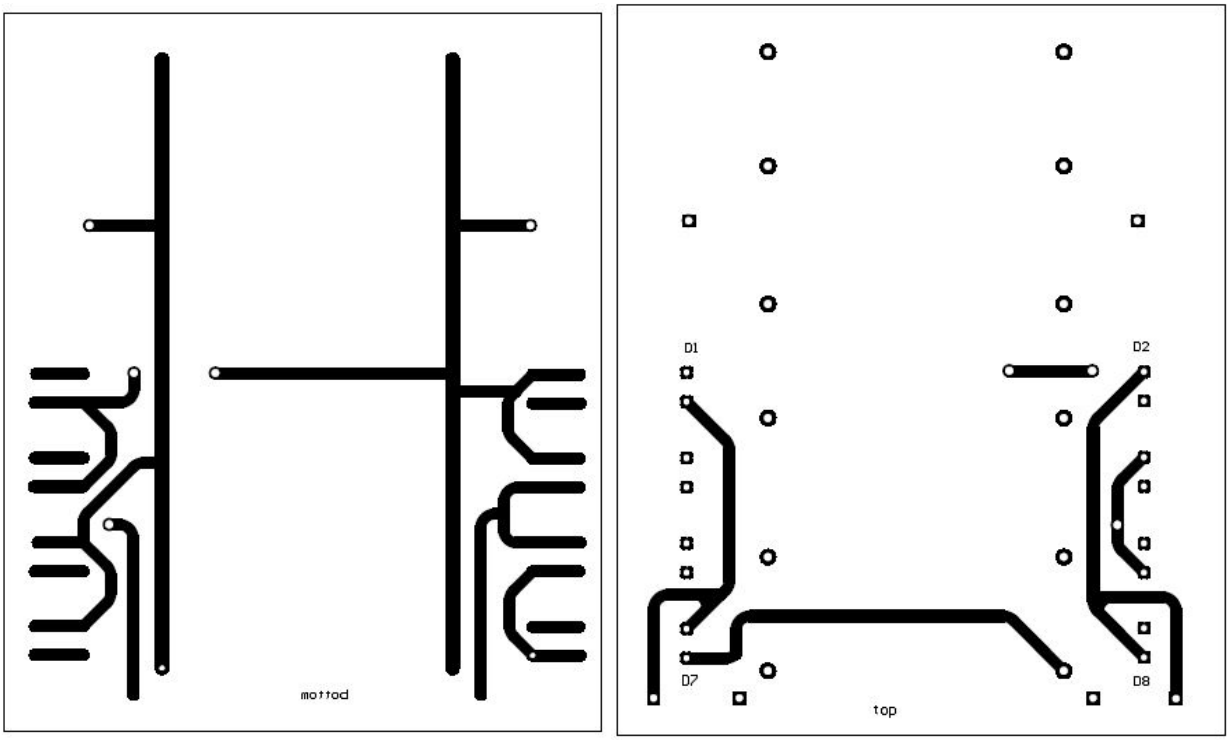

Figure A.2.: Pcb of the snubber circuit top layer and bottom layer.

A.3. Bidirectional Full Bridge

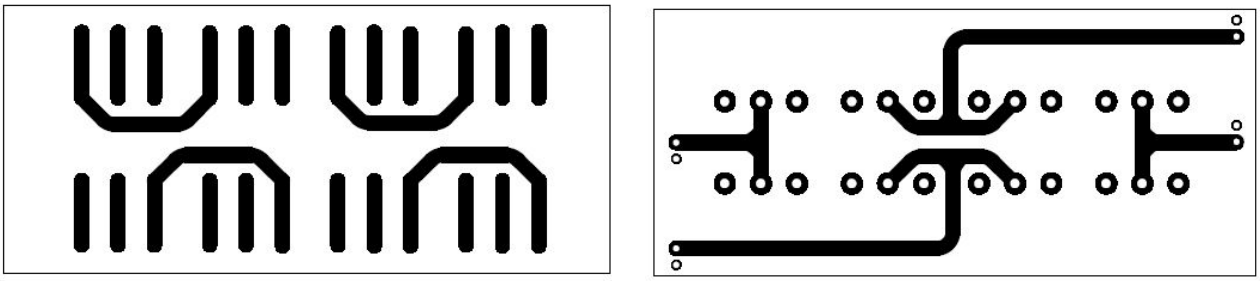

Figure A.3.: Pcb of the bidirectional full bridge, top and bottom layer.

A.4. Driver circuit

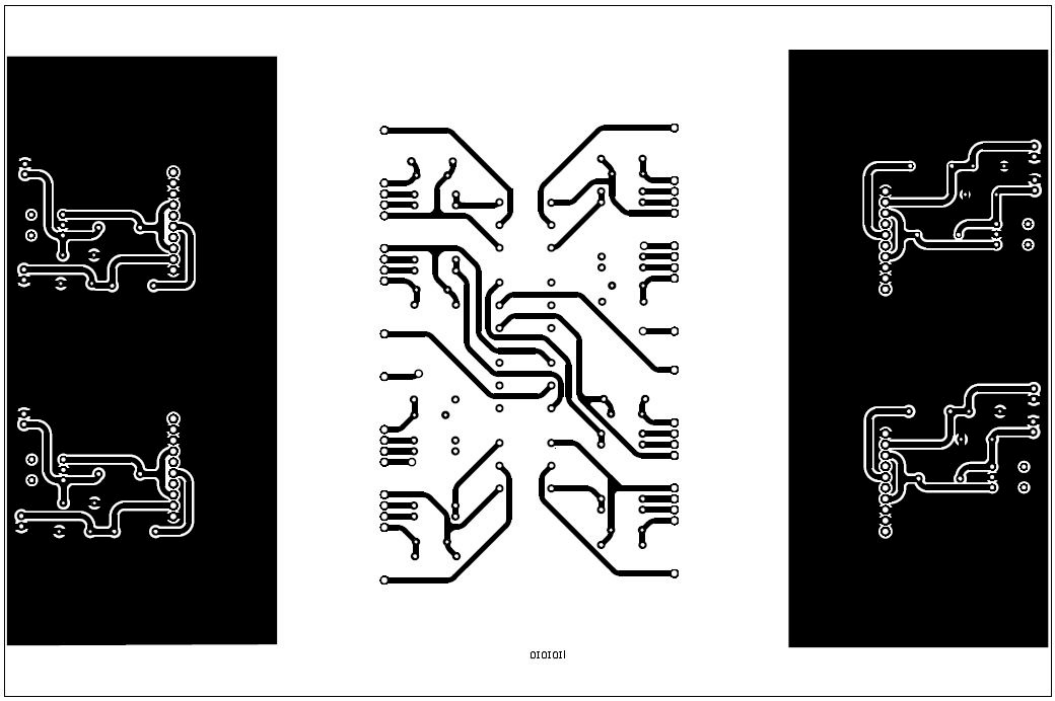

Figure A.4.: Pcb Driver circuit top layer.

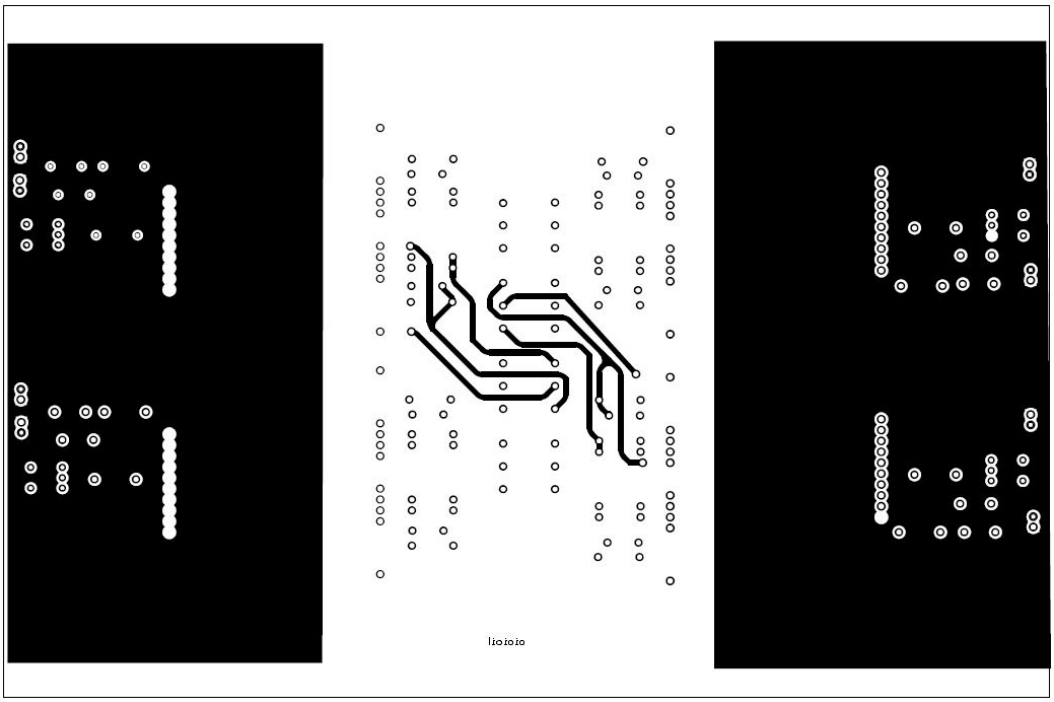

Figure A.5.: Pcs Driver circuit bottom layer.

B

SIMULATION MODEL

Fig. B.1, illustrates a model to estimate the mPWM based on the first approach by direct comparison of the absolute values.

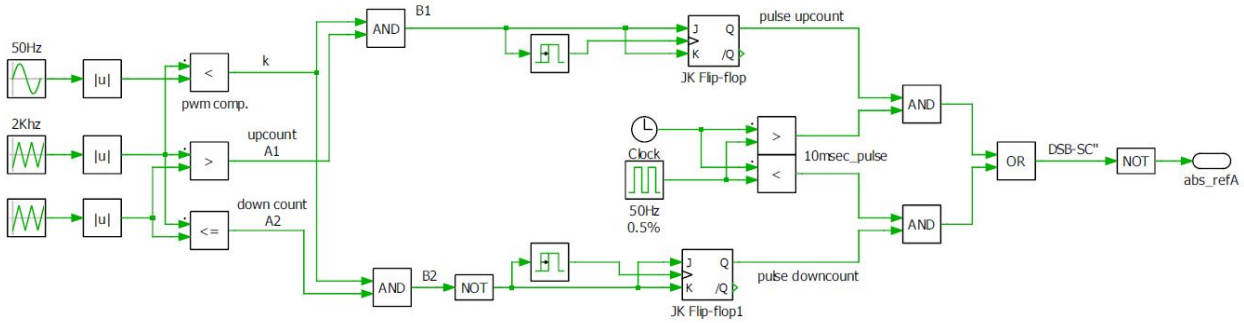

Figure B.1.: PLECS model#1 for estimation of the mPWM using the first approach to the absolute values comparison.

Next Fig. B.2, illustrates the modulation scheme for implementing the mPWM based on a second approach which is the one implemented also with the microcontroller

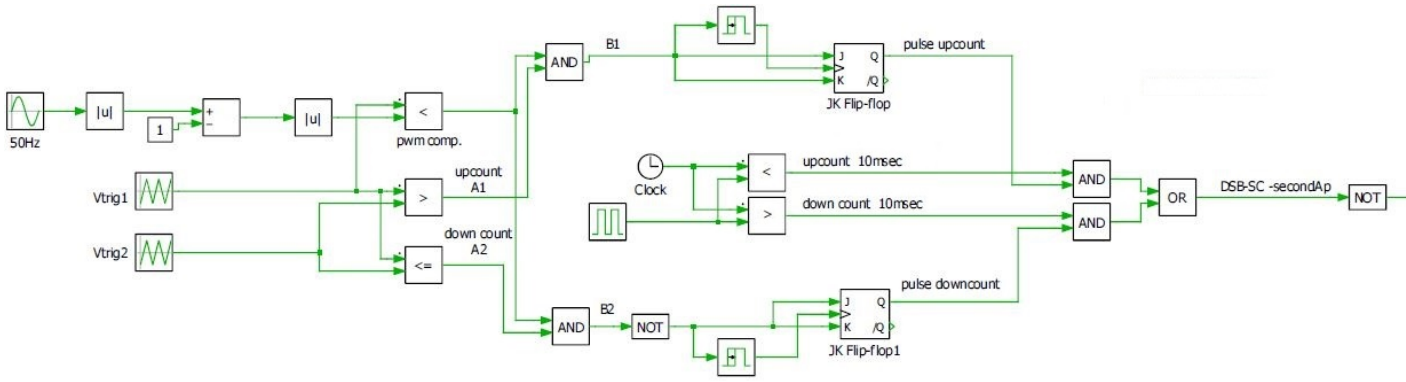

Figure B.2.: PLECS model#2 for estimation of the mPWM using the first approach to the absolute values comparison.